TEXAS
INSTRUMENTS

Amplifiers, Comparators, and Special Functions

Data Book

Volume A

1997

Data Book
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Amplifiers, Comparators,
and Special Functions

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INTRODUCTION

Texas Instruments (TI) offers an extensive line of industry-standard and leadership operational amplifier and comparator products. The technologies represented in this book include traditional bipolar through BiFET, Excalibur, LinCMOS™, Advanced LinCMOS™, and LinBiCMOS™ processes.

The Operational Amplifier/Comparator Data Books (Volumes A and B) provide information on an extensive listing of TI operational amplifier and comparator products:

- Audio Power Amplifiers: Low Voltage, Low Power, High Output Power, and Low Distortion
- Precision, Self-Calibration (Self-Cal]) Amplifiers
- Advanced LinCMOS: Rail-to-Rail Output, High Output Drive, Low Noise, and Low Voltage
- Internally Compensated Amplifiers: Single, Dual, and Quadruple
- Noncompensated Amplifiers: Single and Dual
- Excalibur: High Speed, Low Power, Precision, JFET Input, High Output Drive, and Low Noise
- Various Temperature Ranges: Commercial, Industrial, Automotive, Military, and Extended

AUDIO POWER AMPLIFIERS

Since the release of our last databook, Texas Instruments has introduced several members of our new audio power-amplifier product line. These devices are denoted with the TPA (TI Power Amplifiers) prefix and offer the designer high-fidelity output for low-voltage applications. Several products are optimized for 3-V and 5-V operation and offer shutdown capability for extended life in battery-powered applications. Typical distortion levels are <1% THD+N and along with high ac power supply rejection ratio (PSRR) provide the user with high-fidelity outputs.

FEATURES IN THIS BOOK

- New audio power amplifier product line (TPAxxxx)
- New additions to our low-voltage CMOS rail-to-rail output operational amplifier family
- Amplifier and comparator products available in the SOT-23 package
- Precision Self-Calibration (Self-Cal]) amplifier products
- New family of ultra-fast, low-power comparators
- Expanded product characterization over supply voltage and temperature
- Complete mechanical specifications

The first section of each volume contains an alphanumeric listing, a selection guide, and a cross reference for each type of device. The alphanumeric listing in the book includes all the devices contained in volumes A and B of the Operational Amplifier/Comparator Data Book. The sections in each book are numbered consecutively across volumes (Sections 1, 2, 3, and 4 are in Volume A and sections 5, 6, 7, 8, and 9 are in Volume B). Thus, the reader can easily find the particular volume for a given device.

Due to the great number of devices available from TI, the selection guide for the operational amplifiers is broken down into nine primary categories with a complete alphanumeric listing at the end. The audio power amplifier, comparator and special function selection guides are a complete alphanumeric listing. The cross references in Section 1 help to identify devices that are comparable to other manufacturers and older TI parts.

The last section in each volume contains ordering information and mechanical data for the devices in that particular volume.

While these volumes offer information only on the amplifier and comparator devices available now from TI, complete technical data for upcoming analog or any other TI semiconductor product is available from your nearest TI field sales office, local authorized distributor, or by writing directly to:

Texas Instruments Incorporated
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P.O. Box 809066
Dallas, Texas 75380-9066

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ALPHANUMERIC INDEX

The devices in **BOLD** type are new to this data book.

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AUDIO POWER AMPLIFIERS

DEVICE	V_{DD}/V_{CC} (V) min max	I_{DD}/I_{CC} (mA per channel) typ	OUTPUT POWER (W)	THD + N @ 1 kHz	PSRR (dB)	ISD (µA)	HEAD-PHONE ENABLE	DESCRIPTION	PAGE NO.
TPA0102†	3 to 5.5	1.9	1.5	0.2%	75	1	Yes	1.5-W stereo audio power amplifier	2–3
TPA302	2.7 to 5.5	4	0.3	0.06%	55	0.6	No	300-mW stereo audio power amplifier	2–9
TPA1517†	6 to 18	40	6	1%	62		No	6-W/ch. stereo audio power amplifier	2–29
TPA4860	2.7 to 5.5	3.5	1	0.2%	56	0.6	Yes	1-W audio power amplifier	2–41
TPA4861	2.7 to 5.5	3.5	1	0.2%	56	0.6	No	1-W audio power amplifier	2–67

† This device is in the Advanced Information stage of development.

INTRODUCTION

This selection guide is designed to help you quickly identify which operational amplifiers best suit your needs. This section includes specification tables for each operational amplifier, sorted by the primary performance category; this permits a quick comparison of key specifications, enabling a final decision on which amplifier is best for you. Also included in this section is a complete alphanumerically sorted list of all Texas Instruments advanced linear amplifiers with key specifications.

DEFINITION OF TERMS

This selection guide is broken into eight primary-selection categories:

- DC precision
- Single supply
- Noise
- Low voltage
- High speed
- Low power
- Rail to rail
- High temperature

These categories are then subdivided into secondary and tertiary groups combining performance indices. An understanding of what is meant by each term is helpful when choosing the right amplifier for your application.

DC Precision

Precision refers to an amplifier's inherent dc errors, the input offset voltage (V_{IO}), its temperature coefficient (α_{VIO}), and long-term drift (ΔV_{IO}). In direct-coupled applications, these errors are amplified by the amplifier and carried through the system. The magnitude of the input offset voltage limits the minimum signal level that can be accurately measured. This document defines precision operational amplifiers as those having $V_{IO} \leq 1$ mV. In the precision-operational-amplifiers specification table, these operational amplifiers are sorted in ascending order of V_{IO}max at 25°C; the α_{VIO} specification is also provided for comparison.

Single Supply

Single-supply operational amplifiers are those that are designed to operate well with only one power-supply rail, typically 5 V. They are generally characterized as having a common-mode input voltage range (V_{ICR}) that includes ground and outputs that can swing to or very near ground ($V_{OL} \approx 0$ V). Most single-supply operational amplifiers are manufactured using CMOS technology, although some bipolar single-supply amplifiers are available. Single-supply operational amplifiers can be used in systems with split supplies (e.g., ±5 V), but care must be taken not to exceed the maximum supply voltage across the device. For example, V_{DD}max for CMOS operational amplifiers is 16 V. No more than ±8 V should be applied to these devices in a split-supply system. Also, some single-supply operational amplifier output stages are not designed to both source and sink current; when used with split supplies, they may exhibit some crossover distortion as the signal passes through midsupply.

Rail to Rail

Rail-to-rail operational amplifiers feature outputs that swing close to both the positive and negative supply rails. To achieve expected results, maintain loading conditions within the specified drive capability of the amplifier; output swing decreases as load increases.

Noise

Noise in operational amplifiers typically has two components: voltage noise and current noise. Current noise is primarily a function of input bias currents (I_{IB}) and is negligible in JFET-input (BiFET) and CMOS amplifiers. Voltage noise (V_n) is noise generated by the amplifier due to the thermal noise of the channel resistance in JFET and CMOS amplifiers or the emitter resistance in bipolar amplifiers. Bipolar technology offers the lowest voltage noise and offers the greatest advantage when interfacing to low-impedance sources. As source impedance increases to about 10 kΩ, system noise is dominated by the thermal noise of the source and feedback resistances and selection of an amplifier is usually driven by other characteristics. At higher source impedances, the noise contribution due to the high-input currents of bipolar amplifiers becomes prohibitive and either a CMOS or BiFET amplifier should be chosen. Amplifiers in the low-noise operational amplifier sections have $V_n \leq$ 15 nV/√Hz. Current noise, though not specified, can be approximated by:

$$I_n \approx \sqrt{(2 \times q \times I_{IB})}, \text{ where } q = 1.6 \times 10^{-19}$$

Low Voltage

Low-voltage amplifiers operate with V_{CC} or $V_{DD} \leq 3$ V. Some CMOS amplifiers operate with $V_{DD} = 1.4$ V. When using any supply voltage, you must ensure that input signals are within the common-mode input voltage range (V_{ICR}) of the device. To address the emerging 3-V device market, Texas Instruments has introduced a full line of 3-V operational amplifiers, the TLV series of devices.

High Speed

Speed refers to an operational amplifier's slew rate (SR) and its bandwidth. Slew rate describes the ability of the amplifier's output to follow a large rapidly changing signal at its input, expressed in V/µs. Slew rate is a function of and inversely proportional to supply current (I_{CC} or I_{DD}); increased power consumption must often be traded for faster output response. BiFET amplifiers have traditionally offered the best speed performance, although new complementary bipolar technologies are gaining ground. The high-speed operational amplifiers in this selection guide have a bandwidth ≥ 6 MHz; the amplifiers' slew rate is included in the specification tables for reference.

Low Power

Low power in this document refers to amplifiers whose quiescent currents are less than 500 µA. This category is further broken down to delineate micropower amplifiers, or those with I_{CC} or $I_{DD} \leq 250$ µA. The supply current is specified under no-load conditions; the outputs neither sink nor source current. To minimize power consumption, unused amplifiers should be connected as unity-gain followers with their inputs grounded.

High Temperature

High-temperature operational amplifiers are those manufactured using Texas Instruments patent-pending high temperature and high-reliability process. These operational amplifiers perform reliably at temperatures up to 150°C and are well suited for automotive and geophysical (down-hole) applications where temperatures often exceed the industrial or military temperature ranges.

HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

DEVICE	V_{DD}/V_{CC} (V) min max	I_{DD}/I_{CC} (mA per channel) typ max	V_{IO} (mV) max range	CMRR (dB) typ	I_{IB} (pA) typ	V_n (nV/$\sqrt{Hz}$) typ	Slew Rate (V/μs) typ	GBW (MHz) typ	DESCRIPTION	PAGE NO.
LT1013	4 to 44	0.32 to 0.5	0.25 to 0.95	114	–15000	22	0.4		Dual precision low-power	3–51
TLC251(H)	1.4 to 16	0.675 to 1.6	2 to 10	80	0.6	25	3.6	1.7	Prog. low-voltage: high bias mode	3–357
TLC251(M)	1.4 to 16	0.105 to 0.28	2 to 10	91	0.6	32	0.43	0.525	Prog. low-voltage: medium bias mode	3–357
TLC251(L)	1.4 to 16	0.01 to 0.017	2 to 10	94	0.6	68	0.03	0.085	Prog. low-voltage: low bias mode	3–357
TLC252	1.4 to 16	0.7 to 1.6	2 to 10	80	0.6	25	3.6	1.7	Dual low-voltage	3–375
TLC254	1.4 to 16	0.775 to 1.8	2 to 10	80	0.6	25	3.6	1.7	Quad low-voltage	3–395
TLC25L2	1.4 to 16	0.01 to 0.017	2 to 10	94	0.6	68	0.03	0.085	Dual micropower low-voltage	3–375
TLC25L4	1.4 to 16	0.012 to 0.021	2 to 10	94	0.6	70	0.03	0.085	Quad micropower low-voltage	3–395
TLC25M2	1.4 to 16	0.105 to 0.28	2 to 10	91	0.6	32	0.43	0.525	Dual low-power low-voltage	3–375
TLC25M4	1.4 to 16	0.125 to 0.32	2 to 10	91	0.6	32	0.43	0.525	Quad low-power low-voltage	3–395
TLC271(H)	3 to 16	0.675 to 1.6	2 to 10	80	0.6	25	3.6	1.7	Prog. low-power: high bias mode	3–415
TLC271(M)	3 to 16	0.105 to 0.28	2 to 10	91	0.6	32	0.43	0.525	Prog. low-power: medium bias mode	3–415
TLC271(L)	3 to 16	0.01 to 0.017	2 to 10	94	0.6	68	0.03	0.085	Prog. low-power: low bias mode	3–415
TLC272	3 to 16	0.7 to 1.6	2 to 10	80	0.6	25	3.6	1.7	Dual single supply	3–485
TLC274	3 to 16	0.675 to 1.6	2 to 10	80	0.6	25	3.6	1.7	Quad single supply	3–617
TLC277	3 to 16	0.7 to 1.6	to 0.5	80	0.6	25	3.6	1.7	Dual precision single supply	3–485
TLC279	3 to 16	0.675 to 1.6	to 0.9	80	0.6	25	3.6	1.7	Quad precision single supply	3–617
TLC27L2	3 to 16	0.01 to 0.017	2 to 10	94	0.6	68	0.03	0.085	Dual precision single supply micropower	3–551
TLC27L4	3 to 16	0.01 to 0.017	2 to 10	94	0.6	70	0.03	0.085	Quad precision single supply micropower	3–669
TLC27L7	3 to 16	0.01 to 0.017	to 0.5	94	0.6	68	0.03	0.085	Dual precision single supply micropower	3–551
TLC27L9	3 to 16	0.01 to 0.017	to 0.9	94	0.6	70	0.03	0.085	Quad precision single supply micropower	3–669
TLC27M2	3 to 16	0.105 to 0.28	2 to 10	91	0.6	32	0.43	0.525	Dual precision single supply low-power	3–583
TLC27M4	3 to 16	0.105 to 0.28	2 to 10	91	0.6	32	0.43	0.525	Quad precision single supply low-power	3–705
TLC27M7	3 to 16	0.105 to 0.28	to 0.5	91	0.6	32	0.43	0.525	Dual precision single supply low-power	3–583
TLC27M9	3 to 16	0.105 to 0.28	to 0.9	91	0.6	32	0.43	0.525	Quad precision single supply low-power	3–705
TLC1078	1.4 to 16	0.01 to 0.017	1.6 to 0.45	95	0.6	68	0.032	0.085	Dual micropower precision low-voltage	3–741
TLC1079	1.4 to 16	0.01 to 0.017	1.9 to 0.85	95	0.6	68	0.032	0.085	Quad micropower precision low-voltage	3–741
TLC2201	4.6 to 16	1 to 1.5	0.2 to 0.5	110	1	8	2.5	1.8	Low-noise precision rail-to-rail output	3–767
TLC2202	4.6 to 16	0.85 to 1.3	0.5 to 1	110	1	8	2.5	1.9	Dual low-noise precision rail-to-rail	3–767
TLC2252	4.4 to 16	0.035 to 0.0625	0.85 to 1.5	83	1	19	0.12	0.2	Dual rail-to-rail micropower	3–821
TLC2254	4.4 to 16	0.035 to 0.0625	0.85 to 1.5	83	1	19	0.12	0.2	Quad rail-to-rail micropower	3–821
TLC2262	4.4 to 16	0.2 to 0.25	0.95 to 2.5	83	1	12	0.55	0.82	Dual advanced LinCMOS rail-to-rail	3–875

HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS (continued)

DEVICE	V_{DD}/V_{CC} (V) min max	I_{DD}/I_{CC} (mA per channel) typ max	V_{IO} (mV) max range	CMRR (dB) typ	I_{IB} (pA) typ	V_n (nV/$\sqrt{Hz}$) typ	Slew Rate (V/μs) typ	GBW (MHz) typ	DESCRIPTION	PAGE NO.
TLC2264	4.4 to 16	0.2 to 0.25	0.95 to 2.5	83	1	12	0.55	0.82	Quad advanced LinCMOS rail-to-rail	3–875
TLC2272	4.4 to 16	1.1 to 1.5	0.95 to 2.5	75	1	9	3.6	2.18	Dual low-noise rail-to-rail	3–931
TLC2274	4.4 to 16	1.1 to 1.5	0.95 to 2.5	75	1	9	3.6	2.18	Quad low-noise rail-to-rail	3–931
TLC2654	±2.3 to ±8	1.5 to 2.4	0.01 to 0.02	125	50	13	3.7	1.9	Low-noise chopper-stabilized	3–1007
TLC4501	4 to 6	1 to 1.5	–0.08 to 0.08	100	1	12	2.5	4.7	Single self-calibrating precision	3–1081
TLC4502	4 to 6	1.25 to 1.75	–0.1 to 0.1	100	1	12	2.5	4.7	Dual self-calibrating precision	3–1107
TLE2021	±2 to ±20	0.2 to 0.3	0.2 to 0.5	115	25000	15	0.65	2	Precision low-power single supply	6–3
TLE2022	±2 to ±20	0.275 to 0.35	0.15 to 0.5	106	35000	15	0.65	2.8	Dual precision low-power single supply	6–3
TLE2024	±2 to ±20	0.2625 to 0.35	0.5 to 1	102	50000	15	0.7	2.8	Quad precision low-power single supply	6–3
TLE2027	±4 to ±22	3.8 to 5.3	0.025 to 0.1	131	15000	2.5	2.8	13	Low-noise precision	6–59
TLE2037	±4 to ±19	3.8 to 5.3	0.025 to 0.1	131	15000	2.5	7.5	50	Low-noise high-speed precision decomp.	6–59
TLE2061	±3.5 to ±19	0.29 to 0.35	0.5 to 3	90	4	40	3.4	2	JFET-input high-output-drive micropower	6–93
TLE2062	±3.5 to ±19	0.3125 to 0.345	1 to 4	90	4	40	3.4	2	Dual JFET-input high-output-drive micropower	6–93
TLE2064	±3.5 to ±19	0.3125 to 0.35	2 to 6	90	4	40	3.4	2	Quad JFET-input high-output-drive micropower	6–93
TLE2071	±2.25 to ±19	1.7 to 2.2	2 to 4	98	20	11.6	45	10	Low-noise high-speed JFET-input	6–155
TLE2072	±2.25 to ±19	1.55 to 1.8	3.5 to 6	98	20	11.6	45	10	Dual low-noise high-speed JFET-input	6–155
TLE2074	±2.25 to ±19	1.425 to 1.875	3 to 5	98	25	11.6	45	10	Quad low-noise high-speed JFET-input	6–155
TLE2081	±2.25 to ±19	1.7 to 2.2	3 to 6	98	20	11.6	45	10	high-speed JFET-input	6–225
TLE2082	±2.25 to ±19	1.55 to 1.8	4 to 7	98	20	11.6	45	10	Dual high-speed JFET-input	6–225
TLE2084	±2.25 to ±19	1.625 to 1.875	4 to 7	98	25	11.6	45	10	Quad high-speed JFET-input	6–225
TLE2141	±2 to ±22	3.5 to 4.5	0.5 to 0.9	108	–700000	10.5	45	5.9	Low-noise high-speed precision single supply	6–287
TLE2142	±2 to ±22	3.45 to 4.5	0.75 to 1.2	108	–700000	10.5	45	5.9	Dual low-noise high-speed precision	6–287
TLE2144	±2 to ±22	3.45 to 4.5	1.5 to 2.4	108	–700000	10.5	45	5.9	Quad low-noise high-speed precision	6–287
TLE2161	±3.5 to ±19	0.29 to 0.35	0.5 to 3	90	4	40	10	6.4	JFET-input high-output-drive low-power decompensated	6–347
TLE2227	±4 to ±19	3.65 to 5.3	0.1 to 0.35	115	15000	2.5	2.5	13	Dual low-noise high-speed precision	6–375
TLE2237	±4 to ±22	3.65 to 5.3	0.1 to 0.35	115	15000	2.5	5	50	Dual low-noise high-speed precision decomp.	6–375
TLE2301	±4.5 to ±22	2.2 to 3.5	0.4 to 10	97	260000	44	14	8	Excalibur 3-state-output wide-bandwidth power	6–405
TLE2662	3.5 to 15	0.3125 to 0.345	1 to 5	90	4	40	3.4	2	Dual μpower JFET-input with switching-capacitor voltage converter	6–427
TLE2682	3.5 to 15	1.55 to 1.8	0.9 to 7.5	98	20	11.3	45	10	High-speed JFET-input dual with switching-capacitor voltage converter	6–465
TLV2211	2.7 to 10	0.013 to 0.025	to 3	83	1	22	0.025	0.065	Single rail-to-rail micropower	6–513

HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS (continued)

DEVICE	V_{DD}/V_{CC} (V) min max	I_{DD}/I_{CC} (mA per channel) typ max	V_{IO} (mV) max range	CMRR (dB) typ	I_{IB} (pA) typ	V_n (nV/$\sqrt{Hz}$) typ	Slew Rate (V/µs) typ	GBW (MHz) typ	DESCRIPTION	PAGE NO.
TLV2221	2.7 to 10	0.11 to 0.15	to 3	85	1	19	0.18	0.51	Single rail-to-rail low-power	6–541
TLV2231	2.7 to 10	0.85 to 1.2	to 3	70	1	15	1.6	2	Single rail-to-rail	6–567
TLV2252	2.7 to 8	0.034 to 0.0625	0.85 to 1.5	75	1	19	0.1	0.187	Dual rail-to-rail low-voltage micropower	6–593
TLV2254	2.7 to 8	0.034 to 0.0625	0.85 to 1.5	75	1	19	0.1	0.187	Quad rail-to-rail low-voltage micropower	6–593
TLV2262	2.7 to 8	0.2 to 0.25	0.95 to 2.5	75	1	12	0.55	0.67	Dual rail-to-rail low-voltage low-power	6–639
TLV2264	2.7 to 8	0.2 to 0.25	0.95 to 2.5	75	1	12	0.55	0.67	Quad rail-to-rail low-voltage low-power	6–639
TLV2322	2 to 8	0.006 to 0.017	1.1 to 9	88	0.6	68	0.02	0.027	Dual low-voltage micropower	6–687
TLV2324	2 to 8	0.006 to 0.017	1.1 to 10	88	0.6	68	0.02	0.027	Quad low-voltage micropower	6–687
TLV2332	2 to 8	0.08 to 0.25	1.1 to 9	92	0.6	32	0.38	0.3	Dual low-voltage low-power	6–715
TLV2334	2 to 8	0.08 to 0.25	1.1 to 10	92	0.6	32	0.38	0.3	Quad low-voltage low-power	6–715
TLV2341(H)	2 to 8	0.325 to 1.5	1.1 to 8	78	0.6	25	2.1	0.79	Programmable low-voltage: high bias mode	6–743
TLV2341(M)	2 to 8	0.065 to 0.25	1.1 to 8	92	0.6	32	0.38	0.3	Programmable low-voltage: Med bias mode	6–743
TLV2341(L)	2 to 8	0.005 to 0.017	1.1 to 8	88	0.6	68	0.02	0.027	Programmable low-voltage: low bias mode	6–743
TLV2342	2 to 8	0.325 to 1.5	1.1 to 9	78	0.6	25	2.1	0.79	Dual LinCMOS low-voltage high-speed	6–793
TLV2344	2 to 8	0.325 to 1.5	1.1 to 10	78	0.6	25	2.1	0.79	Quad LinCMOS low-voltage high-speed	6–793
TLV2361	±1 to ±2.5	1.75 to 2.5	1 to 6	85	20000	8	3	7	Single high-performanC, low-voltage	6–823
TLV2362	±1 to ±3.5	1.4 to 2.25	1 to 6	75	20000	9	2.5	6	Dual high-performanC, low-voltage	6–823
TLV2432	2.7 to 10	0.1 to 0.125	0.95 to 2	90	1	18	0.25	0.55	Dual wide-input-voltage, high-output-drive	6–839
TLV2442	2.7 to 10	0.75 to 1.1	0.95 to 2	75	1	16	1.4	1.81	Dual wide-input-voltage, high-output-drive	6–875

PRECISION OPERATIONAL AMPLIFIERS

DEVICE	V_{IO} (μV) typ range	V_{IO} (μV) max range	I_{DD}/I_{CC} (mA per channel) typ max	CMRR (dB) typ	SLEW RATE (V/μs) typ	GBW (MHz) typ	DESCRIPTION	PAGE NO.
TLC4501	–40 to 40	–80 to 80	1 to 1.5	100	2.5	4.7	Single self-calibrating precision	3–1081
TLC4502	–50 to 50	–100 to 100	1.25 to 1.75	100	2.5	4.7	Dual self-calibrating precision	3–1107
TLE2024		500 to 1000	0.2625 to 0.35	102	0.7	2.8	Quad precision low-power single supply	6–3
TLE2027	10 to 20	25 to 100	3.8 to 5.3	131	2.8	13	Low-noise precision	6–59
TLE2037	10 to 20	25 to 100	3.8 to 5.3	131	7.5	50	Low-noise high-speed precision decompensated	6–59
LT1013	60 to 250	250 to 950	0.32 to 0.5	114	0.4		Dual precision low-power	3–51
TLE2022	70 to 150	150 to 500	0.275 to 0.35	106	0.65	2.8	Dual precision low-power single supply	6–3
TLC2201	80 to 100	200 to 500	1 to 1.5	110	2.5	1.8	Low-noise precision rail-to-rail output	3–767
TLC2202	80 to 100	500 to 1000	0.85 to 1.3	110	2.5	1.9	Dual low-noise precision rail-to-rail	3–767
TLE2021	80 to 120	200 to 500	0.2 to 0.3	115	0.65	2	Precision low-power single supply	6–3
TLC1078	160	450	0.01 to 0.017	95	0.032	0.085	Dual micropower precision low-voltage	3–741
TLE2141	175 to 200	500 to 900	3.5 to 4.5	108	45	5.9	Low-noise high-speed precision single supply	6–287
TLC1079	190	850	0.01 to 0.017	95	0.032	0.085	Quad micropower precision low-voltage	3–741
TLC2252	200	850 to 1500	0.035 to 0.0625	83	0.12	0.2	Dual rail-to-rail micropower	3–821
TLC2254	200	850 to 1500	0.035 to 0.0625	83	0.12	0.2	Quad rail-to-rail micropower	3–821
TLV2252	200	850 to 1500	0.034 to 0.0625	75	0.1	0.187	Dual rail-to-rail low-voltage micropower	6–593
TLV2254	200	850 to 1500	0.034 to 0.0625	75	0.1	0.187	Quad rail-to-rail low-voltage micropower	6–593
TLE2142	275 to 290	750 to 1200	3.45 to 4.5	108	45	5.9	Dual low-noise high-speed precision	6–287
TLC2262	300	950 to 2500	0.2 to 0.25	83	0.55	0.82	Dual advanced LinCMOS rail-to-rail	3–875
TLC2264	300	950 to 2500	0.2 to 0.25	83	0.55	0.82	Quad advanced LinCMOS rail-to-rail	3–875
TLC2272	300	950 to 2500	1.1 to 1.5	75	3.6	2.18	Dual low-noise rail-to-rail	3–931
TLC2274	300	950 to 2500	1.1 to 1.5	75	3.6	2.18	Quad low-noise rail-to-rail	3–931
TLE2161	300 to 600	500 to 3000	0.29 to 0.35	90	10	6.4	JFET-input high-output-drive low-power decompensated	6–347
TLV2262	300	950 to 2500	0.2 to 0.25	75	0.55	0.67	Dual rail-to-rail low-voltage low-power	6–639
TLV2264	300	950 to 2500	0.2 to 0.25	75	0.55	0.67	Quad rail-to-rail low-voltage low-power	6–639
TLV2432	300	950 to 2000	0.1 to 0.125	90	0.25	0.55	Dual wide-input-voltage, high-output-drive	6–839
TLV2442	300	950 to 2000	0.75 to 1.1	75	1.4	1.81	Dual wide-input-voltage, high-output-drive	6–875

LOW-NOISE OPERATIONAL AMPLIFIERS

DEVICE	V_n (nV/$\sqrt{Hz}$) typ	I_{DD}/I_{CC} (mA per channel) typ max	I_{IB} (pA) typ	SLEW RATE (V/μs) typ	GBW (MHz) typ	RAIL-TO-RAIL OUTPUT	DESCRIPTION	PAGE NO.
TLE2027	2.5	3.8 to 5.3	15000	2.8	13		Low-noise precision	6–59
TLE2037	2.5	3.8 to 5.3	15000	7.5	50		Low-noise high-speed precision decompensated	6–59
TLE2227	2.5	3.65 to 5.3	15000	2.5	13		Dual low-noise high-speed precision	6–375
TLE2237	2.5	3.65 to 5.3	15000	5	50		Dual low-noise high-speed precision decompensated	6–375
TLC2201	8	1 to 1.5	1	2.5	1.8	X	Low-noise precision rail-to-rail output	3–767
TLC2202	8	0.85 to 1.3	1	2.5	1.9	X	Dual low-noise precision rail-to-rail	3–767
TLV2361	8	1.75 to 2.5	20000	3	7		single high-performanC, low-voltage	6–823
TLC2272	9	1.1 to 1.5	1	3.6	2.18	X	Dual low-noise rail-to-rail	3–931
TLC2274	9	1.1 to 1.5	1	3.6	2.18	X	Quad low-noise rail-to-rail	3–931
TLV2362	9	1.4 to 2.25	20000	2.5	6		Dual high-performanC, low-voltage	6–823
TLE2141	10.5	3.5 to 4.5	–700000	45	5.9		Low-noise high-speed precision single supply	6–287
TLE2142	10.5	3.45 to 4.5	–700000	45	5.9		Dual low-noise high-speed precision	6–287
TLE2144	10.5	3.45 to 4.5	–700000	45	5.9		Quad low-noise high-speed precision	6–287
TLE2071	11.6	1.7 to 2.2	20	45	10		Low-noise high-speed JFET-input	6–155
TLE2072	11.6	1.55 to 1.8	20	45	10		Dual low-noise high-speed JFET-input	6–155
TLE2074	11.6	1.425 to 1.875	25	45	10		Quad low-noise high-speed JFET-input	6–155
TLC2262	12	0.2 to 0.25	1	0.55	0.82	X	Dual advanced LinCMOS rail-to-rail	3–875
TLC2264	12	0.2 to 0.25	1	0.55	0.82	X	Quad advanced LinCMOS rail-to-rail	3–875
TLC4501	12	1 to 1.5	1	2.5	4.7	X	Single self-calibrating precision	3–1081
TLC4502	12	1.25 to 1.75	1	2.5	4.7	X	Dual self-calibrating precision	3–1107
TLV2262	12	0.2 to 0.25	1	0.55	0.67	X	Dual rail-to-rail low-voltage low-power	6–639
TLV2264	12	0.2 to 0.25	1	0.55	0.67	X	Quad rail-to-rail low-voltage low-power	6–639
TLC2654	13	1.5 to 2.4	50	3.7	1.9	X	Low-noise chopper-stabilized	3–1007
TLE2021	15	0.2 to 0.3	25000	0.65	2		Precision low-power single supply	6–3
TLE2022	15	0.275 to 0.35	35000	0.65	2.8		Dual precision low-power single supply	6–3
TLE2024	15	0.2625 to 0.35	50000	0.7	2.8		Quad precision low-power single supply	6–3
TLV2231	15	0.850 to 1.2	1	1.6	2	X	Single rail-to-rail	6–567
TLV2442	16	0.75 to 1.1	1	1.4	1.81	X	Dual wide-input-voltage, high-output-drive	6–875
TLC2252	19	0.035 to 0.0625	1	0.12	0.2	X	Dual rail-to-rail micropower	3–821
TLC2254	19	0.035 to 0.0625	1	0.12	0.2	X	Quad rail-to-rail micropower	3–821

LOW-NOISE OPERATIONAL AMPLIFIERS (continued)

DEVICE	V_n (nV/$\sqrt{Hz}$) typ	I_{DD}/I_{CC} (mA per channel) typ max	I_{IB} (pA) typ	SLEW RATE (V/µs) typ	GBW (MHz) typ	RAIL-TO-RAIL OUTPUT	DESCRIPTION	PAGE NO.
TLV2221	19	0.110 to 0.15	1	0.18	0.51	X	single rail-to-rail low-power	6–541
TLV2252	19	0.034 to 0.0625	1	0.1	0.187	X	Dual rail-to-rail low-voltage micropower	6–593
TLV2254	19	0.034 to 0.0625	1	0.1	0.187	X	Quad rail-to-rail low-voltage micropower	6–593

HIGH-SPEED OPERATIONAL AMPLIFIERS

DEVICE	GBW (Mhz) typ	Slew Rate (V/µs) typ	I_{DD}/I_{CC} (mA per channel) typ max	I_{IB} (pA) typ	V_n (nV/$\sqrt{Hz}$) typ	DESCRIPTION	PAGE NO.
TLE2037	50	7.5	3.8 to 5.3	15000	2.5	Low-noise high-speed precision decomp.	6–59
TLE2237	50	5	3.65 to 5.3	15000	2.5	Dual low-noise high-speed precision decomp.	6–375
TLV2361	7	3	1.75 to 2.5	20000	8	single high-performanC, low-voltage	6–823
TLV2362	6	2.5	1.4 to 2.25	20000	9	Dual high-performanC, low-voltage	6–823
TLE2141	5.9	45	3.5 to 4.5	–700000	10.5	Low-noise high-speed precision single supply	6–287
TLE2142	5.9	45	3.45 to 4.5	–700000	10.5	Dual low-noise high-speed precision	6–287
TLE2144	5.9	45	3.45 to 4.5	–700000	10.5	Quad low-noise high-speed precision	6–287
TLE2682	10	45	1.55 to 1.8	20	11.3	Dual high-speed JFET-input with switched-capacitor voltage converter	6–465
TLE2071	10	45	1.7 to 2.2	20	11.6	Low-noise high-speed JFET-input	6–155
TLE2072	10	45	1.55 to 1.8	20	11.6	Dual low-noise high-speed JFET-input	6–155
TLE2074	10	45	1.425 to 1.875	25	11.6	Quad low-noise high-speed JFET-input	6–155
TLE2081	10	45	1.7 to 2.2	20	11.6	High-speed JFET-input	6–225
TLE2082	10	45	1.55 to 1.8	20	11.6	Dual high-speed JFET-input	6–225
TLE2084	10	45	1.625 to 1.875	25	11.6	Quad high-speed JFET-input	6–225

RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

DEVICE	V_{DD}/V_{CC} (V) min max	I_{DD}/I_{CC} (µA per channel) typ max	V_O (V) typ	Slew Rate (V/µs) typ	GBW (MHz) typ	V_n ($nV/\sqrt{Hz}$) typ	DESCRIPTION	PAGE NO.
TLC2201	4.6 to 16	1000 to 1500	0 to 4.8	2.5	1.8	8	Low-noise precision rail-to-rail output	3–767
TLC2202	4.6 to 16	850 to 1300	0 to 4.8	2.5	1.9	8	Dual low-noise precision rail-to-rail	3–767
TLC2252	4.4 to 16	35 to 62.5	0.01 to 4.98	0.12	0.2	19	Dual rail-to-rail micropower	3–821
TLC2254	4.4 to 16	35 to 62.5	0.01 to 4.98	0.12	0.2	19	Quad rail-to-rail micropower	3–821
TLC2262	4.4 to 16	200 to 250	0.01 to 4.99	0.55	0.82	12	Dual advanced LinCMOS rail-to-rail	3–875
TLC2264	4.4 to 16	200 to 250	0.01 to 4.99	0.55	0.82	12	Quad advanced LinCMOS rail-to-rail	3–875
TLC2272	4.4 to 16	1100 to 1500	0.01 to 4.99	3.6	2.18	9	Dual low-noise rail-to-rail	3–931
TLC2274	4.4 to 16	1100 to 1500	0.01 to 4.99	3.6	2.18	9	Quad low-noise rail-to-rail	3–931
TLC4501	4 to 6	1000 to 1500	0.01 to 4.99	2.5	4.7	12	Single self-calibrating precision	3–1081
TLC4502	4 to 6	1250 to 1750	0.01 to 4.99	2.5	4.7	12	Dual self-calibrating precision	3–1107
TLV2211	2.7 to 10	13 to 25	0.012 to 4.95	0.025	0.065	22	Single rail-to-rail micropower	6–513
TLV2221	2.7 to 10	110 to 150	0.012 to 4.88	0.18	0.51	19	Single rail-to-rail low-power	6–541
TLV2231	2.7 to 10	850 to 1200	0.08 to 4.9	1.6	2	15	Single rail-to-rail	6–567
TLV2252	2.7 to 8	34 to 62.5	0.01 to 2.98	0.1	0.187	19	Dual rail-to-rail low-voltage micropower	6–593
TLV2254	2.7 to 8	34 to 62.5	0.01 to 2.98	0.1	0.187	19	Quad rail-to-rail low-voltage micropower	6–593
TLV2262	2.7 to 8	200 to 250	0.01 to 2.99	0.55	0.67	12	Dual rail-to-rail low-voltage low-power	6–639
TLV2264	2.7 to 8	200 to 250	0.01 to 2.99	0.55	0.67	12	Quad rail-to-rail low-voltage low-power	6–639
TLV2432	2.7 to 10	100 to 125	0.01 to 4.97	0.25	0.55	18	Dual wide-input-voltage, high-output-drive	6–839
TLV2442	2.7 to 10	750 to 1100	0.01 to 4.97	1.4	1.81	16	Dual wide-input-voltage, high-output-drive	6–875

SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

DEVICE	V_{DD}/V_{CC} (V) min max	I_{DD}/I_{CC} (mA per channel) typ max	V_{IO} (mV) typ max	SLEW RATE (V/μs) typ	GBW (MHz) typ	V_n (nV/√Hz) typ	DESCRIPTION	PAGE NO.
TLE2021	±2 to ±20	0.2 to 0.3	0.12 to 0.5	0.65	2	15	Precision low-power single supply	6–3
TLE2022	±2 to ±20	0.275 to 0.35	0.15 to 0.5	0.65	2.8	15	Dual precision low-power single supply	6–3
TLE2024	±2 to ±20	0.2625 to 0.35		0.7	2.8	15	Quad precision low-power single supply	6–3
TLE2141	±2 to ±22	3.5 to 4.5	0.2 to 0.9	45	5.9	10.5	Low-noise high-speed precision single supply	6–287
TLE2142	±2 to ±22	3.45 to 4.5	0.29 to 1.2	45	5.9	10.5	Dual low-noise high-speed precision	6–287
TLE2144	±2 to ±22	3.45 to 4.5	0.6 to 2.4	45	5.9	10.5	Quad low-noise high-speed precision	6–287
TLV2211	2.7 to 10	0.013 to 0.025	0.45 to 3	0.025	0.065	22	Single rail-to-rail micropower	6–513
TLV2221	2.7 to 10	0.11 to 0.15	0.61 to 3	0.18	0.51	19	Single rail-to-rail low-power	6–541
TLV2231	2.7 to 10	0.85 to 1.2	0.71 to 3	1.6	2	15	Single rail-to-rail	6–567
TLV2252	2.7 to 8	0.034 to 0.0625	0.2 to 1.5	0.1	0.187	19	Dual rail-to-rail low-voltage micropower	6–593
TLV2254	2.7 to 8	0.034 to 0.0625	0.2 to 1.5	0.1	0.187	19	Quad rail-to-rail low-voltage micropower	6–593
TLV2262	2.7 to 8	0.2 to 0.25	0.3 to 2.5	0.55	0.67	12	Dual rail-to-rail low-voltage low-power	6–639
TLV2264	2.7 to 8	0.2 to 0.25	0.3 to 2.5	0.55	0.67	12	Quad rail-to-rail low-voltage low-power	6–639
TLV2432	2.7 to 10	0.1 to 0.125	0.300 to 2	0.25	0.55	18	Dual wide-input-voltage, high-output-drive	6–839
TLV2442	2.7 to 10	0.75 to 1.1	0.300 to 2	1.4	1.81	16	Dual wide-input-voltage, high-output-drive	6–875
TLC4501	4 to 6	1 to 1.5	0.04 to 0.08	2.5	4.7	12	Single self-calibrating precision	3–1081
TLC4502	4 to 6	1.25 to 1.75	0.05 to 0.1	2.5	4.7	12	Dual self-calibrating precision	3–1107
TLC2252	4.4 to 16	0.035 to 0.0625	0.2 to 1.5	0.12	0.2	19	Dual rail-to-rail micropower	3–821
TLC2254	4.4 to 16	0.035 to 0.0625	0.2 to 1.5	0.12	0.2	19	Quad rail-to-rail micropower	3–821
TLC2262	4.4 to 16	0.2 to 0.25	0.3 to 2.5	0.55	0.82	12	Dual advanced LinCMOS rail-to-rail	3–875
TLC2264	4.4 to 16	0.2 to 0.25	0.3 to 2.5	0.55	0.82	12	Quad advanced LinCMOS rail-to-rail	3–875
TLC2272	4.4 to 16	1.1 to 1.5	0.3 to 2.5	3.6	2.18	9	Dual low-noise rail-to-rail	3–931
TLC2274	4.4 to 16	1.1 to 1.5	0.3 to 2.5	3.6	2.18	9	Quad low-noise rail-to-rail	3–931
TLC2201	4.6 to 16	1 to 1.5	0.1 to 0.5	2.5	1.8	8	Low-noise precision rail-to-rail output	3–767
TLC2202	4.6 to 16	0.85 to 1.3	0.1 to 1	2.5	1.9	8	Dual low-noise precision rail-to-rail	3–767

LOW-VOLTAGE OPERATIONAL AMPLIFIERS

DEVICE	V_{DD}/V_{CC} (V) min max	I_{DD}/I_{CC} (mA per channel) typ max	V_O (V) typ	SLEW RATE (V/µs) typ	GBW (MHz) typ	V_n (nV/√Hz) typ	DESCRIPTION	PAGE NO.
TLC1078	1.4 to 16	0.01 to 0.017	0 to 4.1	0.032	0.085	68	Dual micropower precision low-voltage	3–741
TLC1079	1.4 to 16	0.01 to 0.017	0 to 4.1	0.032	0.085	68	Quad micropower precision low-voltage	3–741
TLC251(H)	1.4 to 16	0.675 to 1.6	0 to 3.8	3.6	1.7	25	Prog. low-voltage: high bias mode	3–357
TLC251(M)	1.4 to 16	0.105 to 0.28	0 to 3.9	0.43	0.525	32	Prog. low-voltage: medium bias mode	3–357
TLC251(L)	1.4 to 16	0.01 to 0.017	0 to 4.1	0.03	0.085	68	Prog. low-voltage: low bias mode	3–357
TLC252	1.4 to 16	0.7 to 1.6	0 to 3.8	3.6	1.7	25	Dual low-voltage	3–375
TLC254	1.4 to 16	0.775 to 1.8	0 to 3.8	3.6	1.7	25	Quad low-voltage	3–395
TLC25L2	1.4 to 16	0.01 to 0.017	0 to 4.1	0.03	0.085	68	Dual micropower low-voltage	3–375
TLC25L4	1.4 to 16	0.012 to 0.021	0 to 4.1	0.03	0.085	70	Quad micropower low-voltage	3–395
TLC25M2	1.4 to 16	0.105 to 0.28	0 to 3.9	0.43	0.525	32	Dual low-power low-voltage	3–375
TLC25M4	1.4 to 16	0.125 to 0.32	0 to 3.9	0.43	0.525	32	Quad low-power low-voltage	3–395
TLC271(H)	3 to 16	0.675 to 1.6	0 to 3.8	3.6	1.7	25	Prog. low-power: high bias mode	3–415
TLC271(M)	3 to 16	0.105 to 0.28	0 to 3.9	0.43	0.525	32	Prog. low-power: medium bias mode	3–415
TLC271(L)	3 to 16	0.01 to 0.017	0 to 4.1	0.03	0.085	68	Prog. low-power: low bias mode	3–415
TLC272	3 to 16	0.7 to 1.6	0 to 3.8	3.6	1.7	25	Dual single supply	3–485
TLC274	3 to 16	0.675 to 1.6	0 to 3.8	3.6	1.7	25	Quad single supply	3–617
TLC277	3 to 16	0.7 to 1.6	0 to 3.8	3.6	1.7	25	Dual precision single supply	3–485
TLC279	3 to 16	0.675 to 1.6	0 to 3.8	3.6	1.7	25	Quad precision single supply	3–617
TLC27L2	3 to 16	0.01 to 0.017	0 to 4.1	0.03	0.085	68	Dual precision single supply micropower	3–551
TLC27L4	3 to 16	0.01 to 0.017	0 to 4.1	0.03	0.085	70	Quad precision single supply micropower	3–669
TLC27L7	3 to 16	0.01 to 0.017	0 to 4.1	0.03	0.085	68	Dual precision single supply micropower	3–551
TLC27L9	3 to 16	0.01 to 0.017	0 to 4.1	0.03	0.085	70	Quad precision single supply micropower	3–669
TLC27M2	3 to 16	0.105 to 0.28	0 to 3.9	0.43	0.525	32	Dual precision single supply low-power	3–583
TLC27M4	3 to 16	0.105 to 0.28	0 to 3.9	0.43	0.525	32	Quad precision single supply low-power	3–705
TLC27M7	3 to 16	0.105 to 0.28	0 to 3.9	0.43	0.525	32	Dual precision single supply low-power	3–583
TLC27M9	3 to 16	0.105 to 0.28	0 to 3.9	0.43	0.525	32	Quad precision single supply low-power	3–705
TLV2211	2.7 to 10	0.013 to 0.025	0.012 to 4.95	0.025	0.065	22	Single rail-to-rail micropower	6–513
TLV2221	2.7 to 10	0.11 to 0.15	0.012 to 4.88	0.18	0.51	19	Single rail-to-rail low-power	6–541
TLV2231	2.7 to 10	0.85 to 1.2	0.08 to 4.9	1.6	2	15	Single rail-to-rail	6–567
TLV2252	2.7 to 8	0.034 to 0.0625	0.01 to 2.98	0.1	0.187	19	Dual rail-to-rail low-voltage micropower	6–593
TLV2254	2.7 to 8	0.034 to 0.0625	0.01 to 2.98	0.1	0.187	19	Quad rail-to-rail low-voltage micropower	6–593
TLV2262	2.7 to 8	0.2 to 0.25	0.01 to 2.99	0.55	0.67	12	Dual rail-to-rail low-voltage low-power	6–639
TLV2264	2.7 to 8	0.2 to 0.25	0.01 to 2.99	0.55	0.67	12	Quad rail-to-rail low-voltage low-power	6–639

LOW-VOLTAGE OPERATIONAL AMPLIFIERS (continued)

DEVICE	V_{DD}/V_{CC} (V) min max	I_{DD}/I_{CC} (mA per channel) typ max	V_O (V) typ	SLEW RATE (V/µs) typ	GBW (MHz) typ	V_n (nV/√Hz) typ	DESCRIPTION	PAGE NO.
TLV2322	2 to 8	0.006 to 0.017	0.115 to 1.9	0.02	0.027	68	Dual low-voltage micropower	6–687
TLV2324	2 to 8	0.006 to 0.017	0.115 to 1.9	0.02	0.027	68	Quad low-voltage micropower	6–687
TLV2332	2 to 8	0.08 to 0.25	0.115 to 1.9	0.38	0.3	32	Dual low-voltage low-power	6–715
TLV2334	2 to 8	0.08 to 0.25	0.115 to 1.9	0.38	0.3	32	Quad low-voltage low-power	6–715
TLV2341(H)	2 to 8	0.325 to 1.5	0.12 to 1.9	2.1	0.79	25	Programmable low-voltage: high bias mode	6–743
TLV2341(M)	2 to 8	0.065 to 0.25	0.115 to 1.9	0.38	0.3	32	Programmable low-voltage: Med bias mode	6–743
TLV2341(L)	2 to 8	0.005 to 0.017	0.115 to 1.9	0.02	0.027	68	Programmable low-voltage: low bias mode	6–743
TLV2342	2 to 8	0.325 to 1.5	0.12 to 1.9	2.1	0.79	25	Dual LinCMOS low-voltage high-speed	6–793
TLV2344	2 to 8	0.325 to 1.5	0.12 to 1.9	2.1	0.79	25	Quad LinCMOS low-voltage high-speed	6–793
TLV2361	±1 to ±2.5	1.75 to 2.5	–2.4 to 2.4	3	7	8	Single high-performance, low-voltage	6–823
TLV2362	±1 to ±3.5	1.4 to 2.25	–1.4 to 1.4	2.5	6	9	Dual high-performanC, low-voltage	6–823
TLV2432	2.7 to 10	0.1 to 0.125	0.01 to 4.97	0.25	0.55	18	Dual wide-input-voltage, high-output-drive	6–839
TLV2442	2.7 to 10	0.75 to 1.1	0.01 to 4.97	1.4	1.81	16	Dual wide-input-voltage, high-output-drive	6–875

LOW-POWER OPERATIONAL AMPLIFIERS

DEVICE	V_{DD}/V_{CC} (V) min max	I_{DD}/I_{CC} (μA per channel) typ max	V_{IO} (mV) typ max	SLEW RATE (V/μs) typ	GBW (MHz) typ	V_n (nV/$\sqrt{Hz}$) typ	DESCRIPTION	PAGE NO.
TLC27L1	3 to 16	10 to 17	1.1 to 10	0.03	1	68	Single LinCMOS	3–521
TLC2252	4.4 to 16	35 to 62.5	0.2 to 1.5	0.12	0.2	19	Dual rail-to-rail micropower	3–821
TLC2254	4.4 to 16	35 to 62.5	0.2 to 1.5	0.12	0.2	19	Quad rail-to-rail micropower	3–821
TLC2262	4.4 to 16	200 to 250	0.3 to 2.5	0.55	0.82	12	Dual advanced LinCMOS rail-to-rail	3–875
TLC2264	4.4 to 16	200 to 250	0.3 to 2.5	0.55	0.82	12	Quad advanced LinCMOS rail-to-rail	3–875
TLE2021	±2 to ±20	200 to 300	0.12 to 0.5	0.65	2	15	Precision low-power single supply	6–3
TLE2022	±2 to ±20	275 to 350	0.15 to 0.5	0.65	2.8	15	Dual precision low-power single supply	6–3
TLE2024	±2 to ±20	262.5 to 350		0.7	2.8	15	Quad precision low-power single supply	6–3
TLE2061	±3.5 to ±19	290 to 350	0.6 to 3	3.4	2	40	JFET-input high-output-drive micropower	6–93
TLE2062	±3.5 to ±19	312.5 to 345	0.9 to 4	3.4	2	40	Dual JFET-input high-output-drive micropower	6–93
TLE2064	±3.5 to ±19	312.5 to 350	0.9 to 6	3.4	2	40	Quad JFET-input high-output-drive micropower	6–93
TLV2211	2.7 to 10	13 to 25	0.45 to 3	0.025	0.065	22	Single rail-to-rail micropower	6–513
TLV2221	2.7 to 10	110 to 150	0.61 to 3	0.18	0.51	19	Single rail-to-rail low-power	6–541
TLV2252	2.7 to 8	34 to 62.5	0.2 to 1.5	0.1	0.187	19	Dual rail-to-rail low-voltage micropower	6–593
TLV2254	2.7 to 8	34 to 62.5	0.2 to 1.5	0.1	0.187	19	Quad rail-to-rail low-voltage micropower	6–593
TLV2262	2.7 to 8	200 to 250	0.3 to 2.5	0.55	0.67	12	Dual rail-to-rail low-voltage low-power	6–639
TLV2264	2.7 to 8	200 to 250	0.3 to 2.5	0.55	0.67	12	Quad rail-to-rail low-voltage low-power	6–639
TLV2432	2.7 to 10	100 to 125	0.3 to 2	0.25	0.55	18	Dual wide-input-voltage, high-output-drive	6–839

GENERAL-PURPOSE BIPOLAR OPERATIONAL AMPLIFIERS

DEVICE	V_{CC} (V) min max	I_{CC} (mA per channel) typ max	V_{IO} (mV) max range	CMRR (dB) typ	I_{IB} (pA) typ	V_n (nV/√Hz) typ	Slew Rate (V/µs) typ	GBW (MHz) typ	DESCRIPTION	PAGE NO.
LM2902	4 to 26	0.175 to 0.3	7	80	–20000	23	0.25	0.4	Quad general-purpose	3–17
LM2904	4 to 26	0.5 to 1	7	80	–20000	23	0.15	0.4	Dual general-purpose	3–29
LM318	±5 to ±20	5 to 10	10	100	150000	23	70	15	Single high-speed	3–13
LM324	4 to 32	0.175 to 0.3	7	80	–20000	23	0.25	0.4	Quad general-purpose	3–17
LM324x2	4 to 32	0.175 to 0.3	7	80	–20000	23	0.15	0.4	Octal general-purpose	3–39
LM348	±4 to ±18	0.6 to 1.125	6	90	30000	23	0.5	1	Quad general-purpose	3–25
LM358	4 to 32	0.5 to 1	3 to 7	80	–20000	23		0.4	Dual general-purpose	3–29
MC1458	±5 to ±15	1.7 to 2.8	6	90	80000	45	0.5	1	Dual general-purpose	3–75
MC3403	5 to 30	0.7 to 1.75	10	90	–200000		0.6	1	Quad low-power general-purpose	3–79
NE5532	3 to 20	4 to 8	4	100	200000	5	9	10	Dual low-noise high-speed audio	3–85
NE5534	3 to 20	4 to 8	4	100	500000	3.5	13	10	Low-noise high-speed audio	3–89
OP07	±3 to ±18	2.7 to 5	0.15	120	1800	9.8	0.3	0.6	Precision	3–95
RC4136	±5 to ±18	1.25 to 2.825	6	90	140000	8	1.7	3	Quad general-purpose	3–101
RC4558	±5 to ±18	1.25 to 2.8	6	90	150000	8	1.7	3	Dual general-purpose	3–105
TL022	±5 to ±18	0.065 to 0.125	5	72	100000	50	0.5	0.5	Dual low-power general-purpose	3–111
TL2828	4 to 30	0.35 to 0.6	7	80	–15000	23	0.15	0.4	Dual high temperature bipolar	3–337
TL2829	4 to 30	0.3 to 0.4	7	75	–15000	23	0.25	0.4	Quad high temperature bipolar	3–343
µA741	±3.5 to ±18	1.7 to 2.8	6	90	80000		0.5		General-purpose	6–909

GENERAL-PURPOSE LinCMOS OPERATIONAL AMPLIFIERS

DEVICE	V_{DD} (V) min max	I_{DD} (mA per channel) typ max	V_{IO} (mV) max range	CMRR (dB) typ	I_{IB} (pA) typ	V_n (nV/√Hz) typ	SLEW RATE (V/μs) typ	GBW (MHz) typ	DESCRIPTION	PAGE NO.
TLC1078	1.4 to 16	0.01 to 0.017	0.45	95	0.6	68	0.032	0.085	Dual micropower precision low-voltage	3–741
TLC1079	1.4 to 16	0.01 to 0.017	0.85	95	0.6	68	0.032	0.085	Quad micropower precision low-voltage	3–741
TLC251(H)	1.4 to 16	0.675 to 1.6	2 to 10	80	0.6	25	3.6	1.7	Prog. low-voltage: high bias mode	3–357
TLC251(M)	1.4 to 16	0.105 to 0.28	2 to 10	91	0.6	32	0.43	0.525	Prog. low-voltage: medium bias mode	3–357
TLC251(L)	1.4 to 16	0.01 to 0.017	2 to 10	94	0.6	68	0.03	0.085	Prog. low-voltage: low bias mode	3–357
TLC252	1.4 to 16	0.7 to 1.6	2 to 10	80	0.6	25	3.6	1.7	Dual low-voltage	3–375
TLC254	1.4 to 16	0.775 to 1.8	2 to 10	80	0.6	25	3.6	1.7	Quad low-voltage	3–395
TLC25L2	1.4 to 16	0.01 to 0.017	2 to 10	94	0.6	68	0.03	0.085	Dual micropower low-voltage	3–375
TLC25L4	1.4 to 16	0.012 to 0.021	2 to 10	94	0.6	70	0.03	0.085	Quad micropower low-voltage	3–395
TLC25M2	1.4 to 16	0.105 to 0.28	2 to 10	91	0.6	32	0.43	0.525	Dual low-power low-voltage	3–375
TLC25M4	1.4 to 16	0.125 to 0.32	2 to 10	91	0.6	32	0.43	0.525	Quad low-power low-voltage	3–395
TLC271(H)	3 to 16	0.675 to 1.6	2 to 10	80	0.6	25	3.6	1.7	Prog. low-power: high bias mode	3–415
TLC271(M)	3 to 16	0.105 to 0.28	2 to 10	91	0.6	32	0.43	0.525	Prog. low-power: medium bias mode	3–415
TLC271(L)	3 to 16	0.01 to 0.017	2 to 10	94	0.6	68	0.03	0.085	Prog. low-power: low bias mode	3–415
TLC272	3 to 16	0.7 to 1.6	2 to 10	80	0.6	25	3.6	1.7	Dual single supply	3–485
TLC274	3 to 16	0.675 to 1.6	2 to 10	80	0.6	25	3.6	1.7	Quad single supply	3–617
TLC274x2	3 to 16	0.675 to 1.6	10	80	0.6	25	3.6	1.7	Octal single supply	3–653
TLC277	3 to 16	0.7 to 1.6	0.5	80	0.6	25	3.6	1.7	Dual precision single supply	3–485
TLC279	3 to 16	0.675 to 1.6	0.9	80	0.6	25	3.6	1.7	Quad precision single supply	3–617
TLC27L2	3 to 16	0.01 to 0.017	2 to 10	94	0.6	68	0.03	0.085	Dual precision single supply micropower	3–551
TLC27L4	3 to 16	0.01 to 0.017	2 to 10	94	0.6	70	0.03	0.085	Quad precision single supply micropower	3–669
TLC27L7	3 to 16	0.01 to 0.017	0.5	94	0.6	68	0.03	0.085	Dual precision single supply micropower	3–551
TLC27L9	3 to 16	0.01 to 0.017	0.9	94	0.6	70	0.03	0.085	Quad precision single supply micropower	3–669
TLC27M2	3 to 16	0.105 to 0.28	2 to 10	91	0.6	32	0.43	0.525	Dual precision single supply low-power	3–583
TLC27M4	3 to 16	0.105 to 0.28	2 to 10	91	0.6	32	0.43	0.525	Quad precision single supply low-power	3–705
TLC27M7	3 to 16	0.105 to 0.28	0.5	91	0.6	32	0.43	0.525	Dual precision single supply low-power	3–583
TLC27M9	3 to 16	0.105 to 0.28	0.9	91	0.6	32	0.43	0.525	Quad precision single supply low-power	3–705
TLC2801	4.6 to 16	1.1 to 1.5	0.5	110	1	8	2.5	1.8	Low-noise precision high temperature	3–1031
TLC2810	4 to 16	0.5 to 1.6	10	90	7	25	3.6	1.7	Dual high temperature	3–1043
TLC2872	4.4 to 16	1.1 to 1.5	2.5	75	1	9	3.6	2.18	Dual low-noise high temperature	3–1065
TLV2322	2 to 8	0.006 to 0.017	9	88	0.6	68	0.02	0.027	Dual low-voltage micropower	6–687
TLV2324	2 to 8	0.006 to 0.017	10	88	0.6	68	0.02	0.027	Quad low-voltage micropower	6–687

GENERAL-PURPOSE LinCMOS OPERATIONAL AMPLIFIERS (continued)

DEVICE	V_{DD} (V) min max	I_{DD} (mA per channel) typ max	V_{IO} (mV) max range	CMRR (dB) typ	I_{IB} (pA) typ	V_n (nV/$\sqrt{Hz}$) typ	SLEW RATE (V/µs) typ	GBW (MHz) typ	DESCRIPTION	PAGE NO.
TLV2332	2 to 8	0.08 to 0.25	9	92	0.6	32	0.38	0.3	Dual low-voltage low-power	6–715
TLV2334	2 to 8	0.08 to 0.25	10	92	0.6	32	0.38	0.3	Quad low-voltage low-power	6–715
TLV2341(H)	2 to 8	0.325 to 1.5	8	78	0.6	25	2.1	0.79	Programmable low-voltage: high bias mode	6–743
TLV2341(M)	2 to 8	0.065 to 0.25	8	92	0.6	32	0.38	0.3	Programmable low-voltage: Med bias mode	6–743
TLV2341(L)	2 to 8	0.005 to 0.017	8	88	0.6	68	0.02	0.027	Programmable low-voltage: low bias mode	6–743
TLV2342	2 to 8	0.325 to 1.5	9	78	0.6	25	2.1	0.79	Dual LinCMOS low-voltage high-speed	6–793
TLV2344	2 to 8	0.325 to 1.5	10	78	0.6	25	2.1	0.79	Quad LinCMOS low-voltage high-speed	6–793

GENERAL-PURPOSE BiFET OPERATIONAL AMPLIFIERS

DEVICE	V_{CC} (V) min max	I_{CC} (mA per channel) typ max	V_{IO} (mV) max range	CMRR (dB) typ	I_{IB} (pA) typ	V_n (nV/$\sqrt{Hz}$) typ	SLEW RATE (V/µs) typ	GBW (MHz) typ	DESCRIPTION	PAGE NO.
LF347	±3.5 to ±18	2 to 3.75	5 to 10	100	50	18	13	3	Quad general-purpose JFET-input	3–3
LF351	±3.5 to ±18	1.8 to 3.4	10	100	50	18	13	3	General-purpose JFET-input	3–5
LF353	±3.5 to ±18	1.8 to 3.25	10	100	50	18	13	3	Dual general-purpose JFET-input	3–7
LF411	±3.5 to ±18	2 to 3.4	2	100	50	18	13	3	Precision JFET-input	3–9
LF412	±3.5 to ±18	2.25 to 3.4	3	100	50	18	13	3	Dual JFET-input	3–11
TL031	±5 to ±18	0.217 to 0.28	0.8 to 1.5	94	2	41	5.1	1.1	Enhanced JFET low-power precision	3–115
TL032	±5 to ±18	0.111 to 0.28	0.8 to 1.5	94	2	41	5.1	1.1	Dual enhanced JFET low-power precision	3–115
TL034	±5 to ±18	0.2175 to 0.28	1.5 to 4	94	2	43	5.1	1.1	Quad enhanced JFET low-power precision	3–115
TL051	±5 to ±18	2.7 to 3.2	0.8 to 1.5	93	30	18	20	3.1	Enhanced JFET precision	3–169
TL052	±5 to ±18	2.4 to 2.8	0.8 to 1.5	93	30	19	20.7	3	Dual enhanced JFET precision	3–169
TL054	±5 to ±18	2.1 to 2.8	1.5 to 4	92	30	21	17.8	2.7	Quad enhanced JFET precision	3–169
TL061	±3.5 to ±18	0.2 to 0.25	3 to 15	86	30	42	3.5	1	Low-power JFET-input general-purpose	3–233
TL062	±3.5 to ±18	0.2 to 0.25	3 to 15	86	30	42	3.5	1	Dual low-power JFET-input general-purpose	3–233
TL064	±3.5 to ±18	0.2 to 0.25	3 to 15	86	30	42	3.5	1	Quad low-power JFET-input general-purpose	3–233
TL064x2	±3.5 to ±18	0.2 to 0.25	15	86	30	42	3.5	1	Octal low-power JFET-input general-purpose	3–255
TL070	±3.5 to ±18	1.4 to 2.5	10	100	65	18	13	3	Low-noise JFET-input decompensated	3–265
TL071	±3.5 to ±18	1.4 to 2.5	3 to 10	100	65	18	13	3	Low-noise JFET-input general-purpose	3–279
TL072	±3.5 to ±18	1.4 to 2.5	3 to 10	100	65	18	13	3	Dual low-noise JFET-input general-purpose	3–279
TL074	±3.5 to ±18	1.4 to 2.5	3 to 10	100	65	18	13	3	Quad low-noise JFET-input general-purpose	3–279
TL074x2	±3.5 to ±18	1.4 to 2.5	10	100	65	18	13	3	Octal low-noise JFET-input general-purpose	3–295
TL081	±3.5 to ±18	1.4 to 2.8	3 to 15	86	30	18	13	3	JFET-input general-purpose	3–307
TL082	±3.5 to ±18	1.4 to 2.8	3 to 15	86	30	18	13	3	Dual JFET-input general-purpose	3–307
TL084	±3.5 to ±18	1.4 to 2.8	3 to 15	86	30	18	13	3	Quad JFET-input general-purpose	3–307
TL084x2	±3.5 to ±18	1.4 to 2.8	15	76	30	18	13	3	Octal JFET-input general-purpose	3–327

AMPLIFIERS — PACKAGE AND TEMPERATURE AVAILABILITY

DEVICE	D	DB	DBV	DW	FK	J	JG	N	NE	P	PW	U	W	Y(CHIP)
LF347	(14)†							(14)†						
LF347B	(14)†							(14)†						
LF351	(8)†									(8)†				
LF353	(8)†									(8)†				
LF411	(8)C									(8)C				
LF412	(8)C									(8)C				
LM118					(20)□		(8)□							
LM124					(20)□	(14)□							(14)□	
LM148					(20)□	(14)□								
LM158					(20)□		(8)□							
LM218	(8)¶									(8)¶				
LM224	(8)¶									(8)¶				
LM248	(14)¶							(14)¶			(14)¶			
LM258	(8)¶									(8)¶				
LM2900								(14)#						
LM2902	(14)☆	(14)☆						(14)☆			(14)☆			
LM2904	(8)☆	(8)☆								(8)☆	(8)☆			
LM318	(8)†									(8)†				
LM324	(14)†	(14)†						(14)†			(14)†			Y
LM324x2		(30)†												
LM348	(14)†							(14)†			(14)†			
LM358	(8)†	(8)†								(8)†	(14)†			Y
LM3900								(14)†						
LT1013	(8)C,I‡,M				(20)M		(8)M			(8)C,I‡,M				Y
MC1458	(8)C									(8)C				
MC1558					(20)M		(8)M					(10)M		
MC3303	(14)#							(14)#						
MC3403	(14)†							(14)†						
NE5532										(8)†,I				
NE5534	(8)†									(8)†				
OP07	(8)†									(8)†				Y
RC4136	(14)†							(14)†						
RC4558	(8)†	(8)†								(8)†	(8)†			Y

SYMBOLS:
Y = 25°C,
‡ = −40°C to 105°C
C or † = 0°C to 70°C
☆ = −40°C to 125°C
§ = −20°C to 85°C
Z = −40°C to 150°C
¶ = −25°C to 85°C
M or □ = −55°C to 125°C
I or # = −40°C to 85°C

AMPLIFIERS — PACKAGE AND TEMPERATURE AVAILABILITY (continued)

DEVICE	D	DB	DBV	DW	FK	J	JG	N	NE	P	PW	U	W	Y(CHIP)
RM4136					(20)□	(14)□							(14)□	
RM4558							(8)□							
RV4136	(14)#							(14)#						
RV4558	(8)#									(8)#				
SE5534					(20)□		(8)□							
TL022	(8)C						(8)M			(8)C		(10)M		
TL031	(8)C,I,M				(20)M		(8)M			(8)C,I,M				Y
TL032	(8)C,I,M				(20)M		(8)M			(8)C,I,M				Y
TL034	(14)C,I,M				(20)M	(14)M		(14)C,I,M			(14)C			Y
TL051	(8)C,I,M				(20)M		(8)M			(8)C,I,M				Y
TL052	(8)C,I,M				(20)M		(8)M			(8)C,I,M				Y
TL054	(14)C,I,M				(20)M	(14)M		(14)C,I,M						Y
TL061	(8)C,I				(20)M		(8)M			(8)C,I	(8)C	(10)M		Y
TL062	(8)C,I				(20)M		(8)M			(8)C,I	(8)C	(10)M		Y
TL064	(14)C,I				(20)M	(14)M		(14)C,I,M			(14)C			Y
TL064x2		(30)C												
TL070	(8)C,I,M									(8)C,I,M	(8)C			
TL071	(8)C,I				(20)M		(8)M			(8)C,I	(8)C			
TL072	(8)C,I				(20)M		(8)M			(8)C,I	(8)C			
TL074	(14)C,I				(20)M	(14)M		(14)C,I,M			(14)C	(10)M		
TL074x2		(30)C												
TL081	(8)C,I				(20)M		(8)M			(8)C,I	(8)C			
TL082	(8)C,I				(20)M		(8)M			(8)C,I	(8)C			Y
TL084	(14)C,I				(20)M	(14)M		(14)C,I,M			(14)C			Y
TL084x2		(30)C												
TL2828	(8)Z									(8)Z				Y
TL2829	(14)Z							(14)Z						Y
TLC251	(8)C									(8)C				Y
TLC252	(8)C									(8)C				Y
TLC254	(14)C							(14)C			(14)C			Y
TLC25L2	(8)C									(8)C				Y
TLC25L4	(14)C							(14)C			(14)C			Y
TLC25M2	(8)C									(8)C				Y

SYMBOLS:
Y = 25°C,
‡ = −40°C to 105°C
C or † = 0°C to 70°C
☆ = −40°C to 125°C
§ = −20°C to 85°C
Z = −40°C to 150°C
¶ = −25°C to 85°C
M or □ = −55°C to 125°C
I or # = −40°C to 85°C

AMPLIFIERS — PACKAGE AND TEMPERATURE AVAILABILITY (continued)

DEVICE	D	DB	DBV	DW	FK	J	JG	N	NE	P	PW	U	W	Y(CHIP)
TLC25M4	(14)C							(14)C			(14)C			Y
TLC271	(8)C,I,M				(20)M		(8)M			(8)C,I,M				
TLC272	(8)C,I,M				(20)M		(8)M			(8)C,I,M	(8)C			Y
TLC274	(14)C,I,M				(20)M		(8)M	(14)C,I,M			(14)C			Y
TLC274x2		(30)C												
TLC277	(8)C,I,M				(20)M		(8)M			(8)C,I,M				
TLC279	(14)C,I,M				(20)M	(14)M		(14)C,I,M						
TLC27L1	(8)C,I,M									(8)C,I,M				
TLC27L2	(8)C,I,M				(20)M		(8)M			(8)C,I,M				
TLC27L4	(14)C,I,M				(20)M	(14)M		(14)C,I,M			(14)C			Y
TLC27L7	(8)C,I,M				(20)M		(8)M			(8)C,I,M				
TLC27L9	(14)C,I,M				(20)M	(14)M		(14)C,I,M						
TLC27M2	(8)C,I,M				(20)M		(8)M			(8)C,I,M				
TLC27M4	(14)C,I,M				(20)M	(14)M		(14)C,I,M			(14)C			Y
TLC27M7	(8)C,I,M				(20)M		(8)M			(8)C,I,M				
TLC27M9	(14)C,I,M				(20)M	(14)M		(14)C,I,M						
TLC1078	(8)C,I,M				(20)M		(8)M			(8)C,I,M				Y
TLC1079	(14)C,I,M				(20)M	(14)M		(14)C,I,M						Y
TLC2201	(8)C,I,M				(20)M		(8)M			(8)C,I,M				Y
TLC2202	(14)C,I,M				(20)M		(8)M			(8)C,I,M				Y
TLC2252	(8)C,I				(20)M		(8)M			(8)C,I	(8)C,I	(10)M		Y
TLC2254	(14)C,I☆				(20)M	(14)M		(14)C,I☆			(8)C,I☆		(14)M	Y
TLC2262	(8)C,I☆				(20)M		(8)M			(8)C,I☆	(8)C,I☆	(10)M		Y
TLC2264	(14)C,I☆				(20)M	(14)M		(14)C,I☆			(14)C,I☆		(14)M	Y
TLC2272	(8)C,I,M									(8)C,I,M	(8)C			Y
TLC2274	(14)C,I,M				(20)M	(14)M		(14)C,I,M			(14)C,I		(14)M	Y
TLC2652	(8)C,I,M (14)C,I,M				(20)M	(14)M	(8)M	(14)C,I,M		(8)C,I,M				Y
TLC2654	(8)C,I,M (14)C,I,M				(20)M	(14)M	(8)M	(14)C,I,M		(8)C,I,M				Y
TLC2801	(8)Z									(8)Z				Y
TLC2810	(8)Z									(8)Z				Y
TLC2872	(8)Z									(8)Z				Y

SYMBOLS: Y = 25°C, C or † = 0°C to 70°C § = –20°C to 85°C ¶ = –25°C to 85°C I or # = –40°C to 85°C
‡ = –40°C to 105°C ☆ = –40°C to 125°C Z = –40°C to 150°C M or □ = –55°C to 125°C

AMPLIFIERS — PACKAGE AND TEMPERATURE AVAILABILITY (continued)

DEVICE	D	DB	DBV	DW	FK	J	JG	N	NE	P	PW	U	W	Y(CHIP)
TLC4501	(8)C,I													Y
TLC4502	(8)C,I													Y
TLE2021	(8)C,I,M	(8)C			(20)M		(8)M			(8)C,I,M	(8)C			Y
TLE2022	(8)C,I,M	(8)C			(20)M		(8)M			(8)C,I,M	(8)C			Y
TLE2024				(16)C,I,M	(20)M	(14)M		(14)C,I,M						Y
TLE2027	(8)C,I‡,M				(20)M		(8)M			(8)C,I‡,M				Y
TLE2037	(8)C,I‡,M				(20)M		(8)M			(8)C,I‡,M				Y
TLE2061	(8)C,I,M	(8)C			(20)M		(8)M			(8)C,I,M	(8)C			Y
TLE2062	(8)C,I,M				(20)M		(8)M			(8)C,I,M				Y
TLE2064	(14)C,I,M				(20)M	(14)M		(14)C,I,M						Y
TLE2071	(8)C,I				(20)M		(8)M			(8)C,I				Y
TLE2072	(8)C,I				(20)M		(8)M			(8)C,I				Y
TLE2074				(16)C,I	(20)M	(14)M		(14)C,I						Y
TLE2081	(8)C				(20)M		(8)M			(8)C				Y
TLE2082	(8)C,I,M				(20)M		(8)M			(8)C,I,M				Y
TLE2084				(16)C	(20)M	(14)M		(14)C,I						Y
TLE2141	(8)C,I‡,M				(20)M		(8)M			(8)C,I‡,M				Y
TLE2142	(8)C,I‡,M				(20)M		(8)M			(8)C,I‡,M	(8)C			Y
TLE2144				(16)C,I‡,M	(20)M	(14)M		(14)C,I‡,M						Y
TLE2161	(8)C,I,M				(20)M		(8)M			(8)C,I,M				
TLE2227				(16)C						(8)C				Y
TLE2237				(16)C						(8)C				Y
TLE2301									(16)I					
TLE2662				(16)I										
TLE2682				(16)I										
TLV2211			(5)C,I											Y
TLV2221			(5)C,I											Y
TLV2231			(5)C,I											Y
TLV2252	(8)I				(20)M		(8)M			(8)I	(8)I	(10)M		Y
TLV2254	(14)I				(20)M	(14)M		(14)I			(14)I		(14)M	Y
TLV2262	(8)I				(20)M		(8)M			(8)I	(8)I	(10)M		Y
TLV2264	(14)I				(20)M	(14)M		(14)I			(14)I		(14)M	Y
TLV2322	(8)I									(8)I	(8)I			Y

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‡ = −40°C to 105°C ☆ = −40°C to 125°C Z = −40°C to 150°C M or □ = −55°C to 125°C

AMPLIFIERS — PACKAGE AND TEMPERATURE AVAILABILITY (continued)

DEVICE	D	DB	DBV	DW	FK	J	JG	N	NE	P	PW	U	W	Y(CHIP)
TLV2324	(14)I							(14)I			(14)I			Y
TLV2332	(8)I									(8)I	(8)I			Y
TLV2334	(14)I							(14)I			(14)I			Y
TLV2341	(8)I									(8)I	(8)I			Y
TLV2342	(8)I									(8)I	(8)I			Y
TLV2344	(14)I							(14)I			(14)I			Y
TLV2361			(5)C,I											Y
TLV2362	(8)§									(8)§	(8)§			Y
TLV2432	(8)C,I				(20)M		(8)M				(8)C,I	(10)M		Y
TLV2442	(8)C,I				(20)M		(8)M				(8)C,I	(10)M		Y
µA741	(8)C,I				(20)M	(14)M	(8)M			(8)C,I	(8)C	(10)M		Y

SYMBOLS: Y = 25°C, C or † = 0°C to 70°C § = –20°C to 85°C ¶ = –25°C to 85°C I or # = –40°C to 85°C
‡ = –40°C to 105°C ☆ = –40°C to 125°C Z = –40°C to 150°C M or □ = –55°C to 125°C

Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

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ICL7642		TLC27M9	3–705
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α_{IIO} **Average Temperature Coefficient of Input Offset Current**

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \frac{\left(I_{IO}\text{ at }T_{A(1)}\right) - \left(I_{IO}\text{ at }T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

α_{VIO} **Average Temperature Coeffiicient of Input Offset Voltage**

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range. The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.

$$\alpha_{VIO} = \frac{\left(V_{IO}\text{ at }T_{A(1)}\right) - \left(V_{IO}\text{ at }T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

ΔV_{CC}

See k_{SVS}

ΔV_{IO}

See k_{SVS}

ϕ_m **Phase Margin**

The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.

A_m **Gain Margin**

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

A_V **Large-Signal Voltage Amplification**

The ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output

A_{VD} **Differential Voltage Amplification**

The ratio of the change in output to the change in differential input voltage producing it with the common-mode input voltage held constant

B_1 **Unity-Gain Bandwidth**

The range of frequencies within which the maximum output voltage swing is above a specified value.

B_{OM} **Maximum-Output-Swing Bandwidth**

The range of frequencies within which the maximum output voltage swing is above the specified value.

c_i **Input Capacitance**

The capacitance between the input terminals with either input grounded

CMRR, k_{CMR}
Common-Mode Rejection Ratio

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

$\overline{F}$ **Average Noise Figure**

The ratio of an ideal current source (having an internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

I_{CC+}, I_{CC-}
Supply Current

The current into the V_{CC+} or V_{CC-} terminal of an integrated circuit

I_{IB} **Input Bias Current**

The average of the currents into the two input terminals with the output at the specified level

I_{IO} **Input Offset Current**

The difference between the currents into the two input terminals with the output at the specified level

I_n **Equivalent Input Noise Current**

The current of an ideal current source (having internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

I_{OL} **Low-Level Output Current**

The current into an output with input conditions applied that according to the product specification will establish a low level at the output.

I_{OS} **Short-Circuit Output Current**

The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point

k_{CMR}

See CMRR

k_{SVS}, ΔV_{CC}, ΔV_{IO}
Supply Voltage Sensitivity

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

k_{SVR} **Supply Voltage Rejection Ratio**

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

P_D **Total Power Dissipation**

The total dc power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \bullet I_{CC+} + V_{CC-} \bullet I_{CC-}$

r_i	**Input Resistance**	The resistance between the input terminals and either input grounded
r_{id}	**Differential Input Resistance**	The small-signal resistance between two ungrounded input terminals
r_o	**Output Resistance**	The resistance between an output terminal and ground
SR	**Slew Rate**	The average time rate of change of the closed-loop amplifier output voltage for a step-signal input
t_r	**Rise Time**	The time required for an output voltage step to change from 10% to 90% of its final value
t_{tot}	**Total Response Time**	The time between a step-function change of the input signal and the instant at which the magnitude of the output signal reaches for the last time a specified level range ($\pm\varepsilon$) containing the final output signal level.
V_I	**Input Voltage Range**	The range of voltage that if exceeded at either input terminal may cause the operational amplifier to cease functioning properly.
V_{IO}	**Input Offset Voltage**	The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.
V_{IC}	**Common-Mode Input Voltage**	The average of the two input voltages
V_{ICR}	**Common-Mode Input Voltage Range**	The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.
V_n	**Equivalent Input Noise Voltage**	The voltage of an ideal voltage source (having internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.
V_{O1}/V_{O2}	**Crosstalk Attenuation**	The ratio of the change in output voltage of a driven channel to the resulting change in output voltage of another channel
V_{OH}	**High-Level Output Voltage**	The voltage at an output with input conditions applied that according to the product specification will establish a high level at the output.
V_{OL}	**Low-Level Output Voltage**	The voltage at an output with input conditions applied that according to the product specification will establish a low level at the output.

V_{ID} **Differential Input Voltage**

The voltage at the noninverting input with respect to the inverting input

V_{OM} **Maximum Peak Output Voltage Swing**

The maximum positive or negative peak output voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

$V_{O(PP)}$ **Maximum Peak-to-Peak Output Voltage Swing**

The maximum peak-to-peak output voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

z_{ic} **Common-Mode Input Impedance**

The parallel sum of the small-signal impedance between each input terminal and ground

z_o **Output Impedance**

The small-signal impedance between the output terminal and ground

Overshoot Factor

The ratio of the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal to the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal.

COMPARATORS (Listed Alphanumerically)

DEVICE	V_{DD}/V_{CC} (V) min	V_{DD}/V_{CC} (V) max	I_{DD}/I_{CC} (mA per channel) max	V_{IO} (mV) max	V_{ICR} (V) min	V_{ICR} (V) max	I_{OL} (mA) min	t_{RESP} (µs) low-to-high	DESCRIPTION	PAGE NO.
LM111	3.5	30	6	3	–14.7	13.8		0.115	Single, strobed differential	7–3
LM139	3.5	30	0.8	5	0		6	0.3	Quad, general purpose differential	7–19
LM211	3.5	30	6	3	–14.7	13.8		0.115	Single, strobed differential	7–3
LM239	3.5	30	0.8	5	0		6	0.3	Quad, general purpose differential	7–19
LM306	–6	12	6.8	5	–5	5	100	0.028	Single, strobed, high speed differential	7–33
LM311	3.5	30	7.5	7.5	–14.7	13.8		0.115	Single, strobed differential	7–3
LM339	4	30	0.8	5	0		6	0.3	Quad, general purpose differential	7–19
LM339x2	4	30	0.5	5	0	3.5	6	0.3	Octal, general purpose differential	7–41
LM393	4	36	1	5	0		6	0.3	Dual, general purpose differential	7–27
LM2901	4	30	0.8	7	0		6	0.3	Quad, general purpose differential	7–19
LM2903	2	36	1	7	0		6	0.3	Dual, general purpose differential	7–27
LM3302	2	28	0.2	20	0	3.5	6	0.3	Quad, general purpose differential	7–45
LP111	4	30	0.3	7.5	–14.5	13.5		1.2	Single, low–power, strobed differential	7–49
LP211	4	30	0.3	7.5	–14.5	13.5		1.2	Single, low–power, strobed differential	7–49
LP239	5	30	0.1	±5	0			1.3	Quad, low–power, general purpose differential	7–53
LP311	4	30	0.3	7.5	–14.5	13.5		1.2	Single, low–power, strobed differential	7–49
LP339	5	30	0.1	±5	0			1.3	Quad, low–power, general purpose differential	7–53
LP2901	5	30	0.1	±5	0			1.3	Quad, low–power, general purpose differential	7–53
TL193	2	7	0.8	5	0	3.8	6	0.2	Dual, general purpose differential	7–59
TL293	2	7	0.8	5	0	3.8	6	0.2	Dual, general purpose differential	7–59
TL393	2	7	0.8	5	0	3.8	6	0.2	Dual, general purpose differential	7–59
TL712	4.75	5.25	20	5+	0	5	16	0.025	Differential	7–65
TL714	4.75	5.25	12	10+	0	5	16	0.006	High–speed differential	7–69
TL3016†	–7	7	12.5	3	–3.75	3.5			Ultra-fast low-power precision	7–73
TL3116†	–7	7	14.7	3	–5	2.5			Ultra-fast low-power precision	7–83
TLC139	3	16	0.08	5	0				Quad, micropower, LinCMOS	7–93
TLC339	3	16	0.08	5	0				Quad, micropower, LinCMOS	7–93
TLC352	1.4	16	0.15	5	0	4	6	0.2	Dual, low voltage, LinCMOS differential	7–109
TLC354	1.4	16	0.15	5	0	4	6	0.2	Quad, low voltage, LinCMOS differential	7–117
TLC371	3	16	0.15	5	0	4	6	0.2	Single general purpose LinCMOS differential	7–127
TLC372	3	16	0.15	5	0	4	6	0.2	Dual general purpose LinCMOS differential	7–137

† This device is in the Advanced Information stage of development.

COMPARATORS (Listed Alphanumerically) (continued)

DEVICE	V_{DD}/V_{CC} (V) min	V_{DD}/V_{CC} (V) max	I_{DD}/I_{CC} (mA per channel) max	V_{IO} (mV) max	V_{ICR} (V) min	V_{ICR} (V) max	I_{OL} (mA) min	t_{RESP} (µs) low-to-high	DESCRIPTION	PAGE NO.
TLC374	3	16	0.15	5	0	4	6	0.2	Quad general purpose LinCMOS differential	7–149
TLC393	3	16	0.02	5	0	4	6	1.1	Dual, micropower, LinCMOS voltage	7–161
TLC3702	3	16	0.02	5	0	4	4	1.1	Dual, micropower, push–pull outputs, LinCMOS voltage	7–177
TLC3704	3	16	0.02	5	0	4	4	1.1	Quad, micropower, push–pull outputs, LinCMOS voltage	7–199
TLV1391	2	7	0.150	5	0	3.8	0.600	0.65	Single differential	7–223
TLV1393	2	7	0.125	5	0	1.8	0.5	0.7	Dual low–voltage, low power differential	7–235
TLV2352	2	8	0.125	5	0	2	6	0.2	Dual low voltage LinCMOS differential	7–251
TLV2354	2	8	0.125	5	0	2	6	0.2	Quad low voltage LinCMOS differential	7–265
TLV2393	2	7	0.65	5	0	1.8	4	0.45	Dual low voltage differential	7–235

COMPARATORS — PACKAGE AND TEMPERATURE AVAILABILITY

DEVICE	D	DB	DBV	FK	J	JG	N	P	PW	U	W	Y(CHIP)
LM111				(20)□	(14)□	(8)□				(10)□		
LM139	(14)□				(14)□		(14)□				(14)□	
LM139A	(14)□			(20)□	(14)□		(14)□					
LM193	(8)□			(20)□		(8)□		(8)□				
LM211	(8)¶							(8)¶				
LM239	(14)§						(14)§					
LM239A	(14)§						(14)§					
LM2901	(14)☆	(14)☆							(14)☆			
LM2901Q	(14)☆						(14)☆					
LM2903	(8)☆	(8)☆						(8)☆	(8)☆			
LM2903Q	(8)☆							(8)☆				
LM293	(8)§							(8)§				
LM293A	(8)§							(8)§				
LM306	(8)†							(8)†				
LM311	(8)†	(8)†						(8)†	(8)†			Y
LM3302	(14)¶				(14)¶		(14)¶					
LM339	(14)†	(14)†					(14)†		(14)†			Y
LM339A	(14)†						(14)†					Y
LM339x2		(30)†										
LM393	(8)†	(8)†						(8)†	(8)†			Y
LM393A	(8)†							(8)†				Y
LP111				(20)□		(8)□						
LP211	(8)§					(8)§		(8)§				
LP239	(14)§				(14)§		(14)§					
LP2901	(14)¶				(14)¶		(14)¶					
LP311	(8)†					(8)†		(8)†				
LP339	(14)†				(14)†		(14)†					
TL393	(8)#							(8)#	(8)#			Y
TL712	(8)C					(8)C		(8)C	(8)C			
TL714	(8)C							(8)C				
TL3016	(8)C,I								(8)C,I			Y
TL3116	(8)C,I								(8)C,I			Y
TLC139				(20)M	(14)M							

SYMBOLS: Y = 25°C, # = −40°C to 105°C
C or † = 0°C to 70°C
Q or ☆ = −40°C to 125°C
§ = −25°C to 85°C
M or □ = −55°C to 125°C
I or ¶ = −40°C to 85°C

COMPARATORS — PACKAGE AND TEMPERATURE AVAILABILITY (continued)

DEVICE	D	DB	DBV	FK	J	JG	N	P	PW	U	W	Y(CHIP)
TLC339	(14)C,I,Q,M						(14)C,I,Q,M					
TLC352	(8)C,I			(20)M		(8)M		(8)C,I				
TLC354	(14)C,I,M						(14)C,I,M		(14)C			Y
TLC371	(8)C,I,M							(8)C,I,M				Y
TLC372	(8)C,I,Q,M			(20)M		(8)M		(8)C,I,Q,M	(8)C			Y
TLC374	(14)C,I,M,Q			(20)M	(14)M		(14)C,I,M,Q		(14)C			
TLC393	(8)C,I,M			(20)M		(8)M		(8)C,I,M				
TLC3702	(8)C,I			(20)M		(8)Q,M		(8)C,I				
TLC3704	(14)C,I			(20)M	(14)Q,M		(14)C,I					
TLV1391			(5)C,I									Y
TLV1393	(8)#							(8)#	(8)#			Y
TLV2352	(8)I							(8)I	(8)I			Y
TLV2354	(14)I						(14)I		(14)I			Y
TLV2393	(8)#							(8)#	(8)#			Y

SYMBOLS:
Y = 25°C,
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Q or ☆ = −40°C to 125°C
§ = −25°C to 85°C
M or □ = −55°C to 125°C
I or ¶ = −40°C to 85°C

COMPARATOR CROSS-REFERENCE GUIDE

Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and the buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained herein.

Manufacturers are arranged in alphabetical order.

LINEAR TECHNOLOGY			
PART NO.	**DIRECT TI REPLACEMENT**	**SUGGESTED TI REPLACEMENT**	**PAGE NO.**
LT1017		TLC352	7–109
		TLC3702	7–177
LT1018		TLC352	7–109
		TLC3702	7–177
NATIONAL			
LM311	LM311		7–3
LM339	LM339		7–19
		TLC339	7–93
LM393	LM393		7–27
		TLC393	7–161
LM2901	LM2901		7–19
		TLC339	7–93
LM3302	LM3302		7–45
LP339	LP339		7–53
		TLC339	7–93
PMI			
CMP04F		LM339	7–19
		LM2901	7–19
		LM3302	7–45
		TLC339	7–93

COMPARATOR GLOSSARY

α_{IIO} **Average Temperature Coefficient of Input Offset Current**

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \frac{\left(I_{IO} \text{ at } T_{A(1)}\right) - \left(I_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

α_{VIO} **Average Temperature Coefficient of Input Offset Voltage**

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \frac{\left(V_{IO} \text{ at } T_{A(1)}\right) - \left(V_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

A_{VD} **Differential Voltage Amplification**

The ratio of the change in output to the change in differential input voltage producing it with the common-mode input voltage held constant

CMRR

See k_{CMR}

I_{CC+}, I_{CC-} **Supply Current**

The current into the V_{CC+} or V_{CC-} terminal of an integrated circuit

$I_{IH(S)}$ **High-Level Strobe Current**

The current flowing into or out of† the strobe at a high-level voltage

I_{IB} **Input Bias Current**

The average of the currents into the two input terminals with the output at the specified level

$I_{IL(S)}$ **Low-Level Strobe Current**

The current flowing out of† the strobe at a low-level voltage

I_{IO} **Input Offset Current**

The difference between the currents into the two input terminals with the output at the specified level

I_{OH} **High-Level Output Current**

The current into an output with input conditions applied that according to the product specification will establish a high level at the output.

I_{OL} **Low-Level Output Current**

The current into an output with input conditions applied that according to the product specification will establish a low level at the output.

k_{CMR} or CMRR
Common-Mode Rejection Ratio

The ratio of differential voltage amplification to common-mode voltage amplification.

NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

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† Current out of a terminal is given as a negative value.

P_D	**Total Power Dissipation** The total dc power supplied to the device less any power delivered from the device to a load. NOTE: At no load: $P_D = V_{CC+} \bullet I_{CC+} + V_{CC-} \bullet I_{CC-}$.
r_o	**Output Resistance** The resistance between an output terminal and ground
V_{IC}	**Common-Mode Input Voltage** The average of the two input voltages
V_{ICR}	**Common-Mode Input Voltage Range** The range of common-mode input voltage that if exceeded may cause the comparator to cease functioning properly.
V_{ID}	**Differential Input Voltage** The voltage at the noninverting input with respect to the inverting input
V_{ID}	**Differential Input Voltage Range** The range of voltage between the two input terminals that if exceeded may cause the comparator to cease functioning properly.
V_I	**Input Voltage Range** The range of voltage that if exceeded at either input terminal may cause the comparator to cease functioning properly.
$V_{IH(S)}$	**High-Level Strobe Voltage** For a device having an active-low strobe, a voltage within that range is guaranteed not to interfere with the operation of the comparator.
$V_{IL(S)}$	**Low-Level Strobe Voltage** For a device having an active-low strobe, a voltage within the range that is guaranteed to force the output high or low, as specified, independently of the differential inputs.
V_{IO}	**Input Offset Voltage** The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to the specified level.
V_{OH}	**High-Level Output Voltage** The voltage at an output with input conditions applied that according to the product specification will establish a high level at the output.
V_{OL}	**Low-Level Output Voltage** The voltage at an output with input conditions applied that according to the product specification will establish a low level at the output.
	Response Time The interval between the application of an input step function and the instant the output crosses the logic threshold voltage. NOTE: The input step drives the comparator from some initial condition sufficient to saturate the output (or in the case of high-to-low-level response time, to turn the output off) to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.
	Strobe Release Time The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from its active logic level to its inactive logic level.

PRECISION TIMERS

DEVICE	I_{DD}/I_{CC} (mA)	TIMING		T_A	PACKAGES	DESCRIPTION	PAGE NO.
		TO	FROM				
NE555	±200	10 µs	Hours	0°C to 70°C	D, P, Y	Single bipolar timer	
NE556	±200	10 µs	Hours	0°C to 70°C	D, N	Dual bipolar timer	
SA555	±200	10 µs	Hours	−40°C to 85°C	D, P	Single bipolar timer	
SA556	±200	10 µs	Hours	−40°C to 85°C	D, N	Dual bipolar timer	
SE555	±200	1 µs	Hours	−55°C to 125°C	D, FK, JG, P	Single bipolar timer	
SE555C	±200	1 µs	Hours	−55°C to 125°C	D, FK, JG, P	Single bipolar timer	
SE556	±200	1 µs	Hours	−55°C to 125°C	D, FK, J, N	Dual bipolar timer	
SE556C	±200	1 µs	Hours	−55°C to 125°C	D, FK, J, N	Dual bipolar timer	
TLC551	100 −10†	1 µs	Hours	0°C to 70°C	D, P, Y	Single LinCMOS high-speed timer	
TLC552	100 −10†	1 µs	Hours	0°C to 70°C	D, N	Dual LinCMOS high-speed timer	
TLC555	100 −10	1 µs	Hours	0°C to 70°C −40°C to 85°C −55°C to 125°C	D, FK, JG, P, Y	Single LinCMOS high-speed timer	
TLC556	100 −10	1 µs	Hours	0°C to 70°C −40°C to 85°C −55°C to 125°C	D, FK, J, N	Dual LinCMOS high-speed timer	

† This parameter is at 1-V operation.

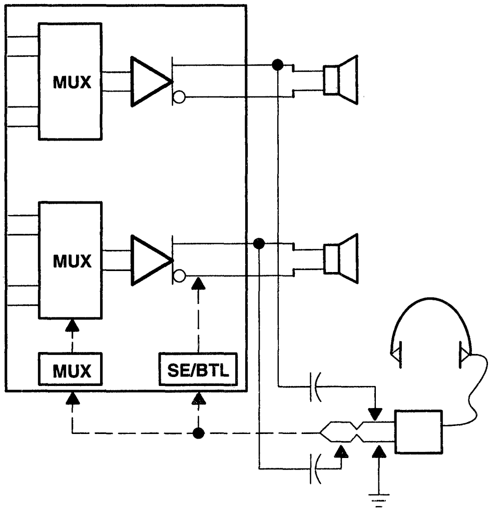
VIDEO AMPLIFIERS

DEVICE	V_{DD}/V_{CC} (V) min max	I_{DD}/I_{CC} (mA per channel) typ	BW (MHz)	$t_{r(video)}$ / $t_{f(video)}$ (ns)	AV (V/V) (max)	DESCRIPTION	PAGE NO.
TLS1233	11 to 13	84	100	3.5	7.8	video preamplifier system	
TLS1255	11 to 13	110	100	3.5	7.6	Video preamplifier system	
µA733			200	2.5	12	Video amplifier with internal frequency compensation	

TPA0102
STEREO 1.5-W AUDIO POWER AMPLIFIER

SLOS166 – MARCH1997

- **High Power with PC Power Supply**
  - **1.5 W/Ch at 5 V**
  - **600 mW/Ch at 3 V**
- **Ultra-Low Distortion**
  < 0.05% THD+N at 1.5 W and 4-Ω Load
- **Bridge-Tied Load (BTL) or Single Ended (SE) Modes**
- **Stereo Input MUX**
- **Surface Mount Power Package**
  24-Pin TSSOP
- **Uncompensated Gains of 1 to 10**
- **Shutdown Control . . . $-I_{DD} < 1\ \mu A$**



description

The TPA0102 is a stereo audio power amplifier in a 24-pin TSSOP thermal package capable of delivering greater than 1.5 W of continuous RMS power per channel into 4-Ω loads. This functionality provides a very efficient upgrade path from the TPA4860 and TPA4861 mono amplifiers where two separate devices are required for stereo speaker-driver applications plus a third device for headphone drive. This implementation simplifies design and frees up board space for other features. Full power distortion levels of 200 m% THD+N from a 5-V supply voltage are typical. This provides significant improvement in fidelity for speech and music over the popular TPA4860/61 series. Low-voltage applications are also well served by the TPA0102 providing 600-mW per channel into 4-Ω loads with a 3.3-V supply voltage.

Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 2 to 20 in BTL mode (1 to 10 in SE mode). An input MUX circuit is integrated to allow two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line (often headphone drive) outputs are required to be SE, the TPA0102 automatically switches into SE mode when SE/BTL input activated. Connection of the SE/BTL control signal to the HP/LINE select input accomplishes automatic selection of different audio paths for headphone or internal-speaker drive. Using the TPA0102 to drive line outputs, up to 500 mW/Ch into external 4 Ω loads at 200 m% THD is ideal for small non-powered external speakers in portable multimedia systems. The TPA0102 also features a showdown function for power sensitive applications holding the bias current below 1 μA. In speakerphone or other monaural applications, the TPA0102 is configured through the power supply terminals to activate only half of the amplifier which reduces quiescent current by approximately 1/2 for the given voltage.

AVAILABLE OPTIONS

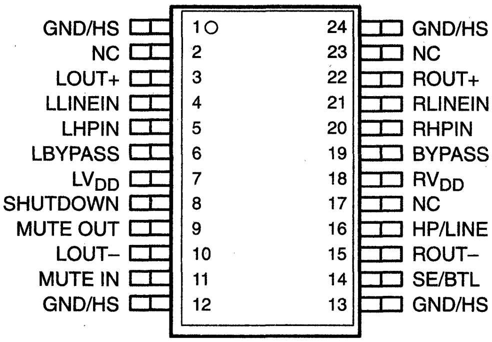
T_A	PACKAGE
	TSSOP† (PWP)
–20°C to 85°C	TPA0102PWP

† See the special instructions for PWP packages.

ADVANCE INFORMATION

ADVANCE INFORMATION

PWP PACKAGE
(TOP VIEW)



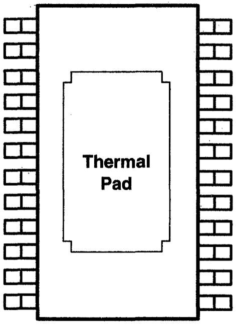


Figure 1. Bottom View of PWP Package, Showing the Thermal Pad

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND/HS	1		Provides ground connection for circuitry, directly connected to heat sink pad.
NC	2		No internal connection.
L Out +	3	O	Left channel + output in BTL mode, + output in SE mode.
L Line In	4	I	Left channel line input, selected when UP/Line pin (16) is held low.
L HP In	5	I	Left channel headphone input, selected when IIP/Line pin (16) is held high.
L Bypass	6		Tap to voltage divider for left channel internal mid-supply bias.
L V_{DD}	7	I	Supply voltage input for left channel and for primary bias circuits.
Shutdown	8	I	Places entire IC in shutdown mode when held high, I_{DD} < I uA.
Mute Out	9	O	Follows Mute In pin (14), provides buffered output.
L Out –	10	O	Left channel – output in BTL mode, high impedance state in SE mode.
Mute In	11	I	Mute all amplifiers, hold low for normal operation, hold high to mute.
GND/HS	12, 13		Provides ground connection for circuitry, directly connected to heat sink pad.
SE/BTL*	14	I	Hold low for BTL modc, hold high for SE mode.
R Out –	15	O	Left channel – output in BTL mode, high impedance state in SE mode.
BP/Line	16	I	Input mux control input, hold high to select L/R BP In (5, 20), hold low to select L/R Line In (4, 2 1).
NC	17		No internal connection.
R V_{DD}	18	I	Supply voltage input for right channel.
R Bypass	19		Tap to voltage divider for right channel internal mid–supply bias.
RBPIn	20	I	Right channel headphone input, selected when HP/Line pin (16) is held high.
R Line In	21	I	Fight channel line input, selected when BP/Line pin (16) is held low.
R Out +	22	O	Right channel + output in BTL mode, + output in SE mode.
NC	23		No internal connection.
GND/HS	24		Provides ground connection for circuitry, directly connected to heat sink pad.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} . . . . 6 V
Continuous total power dissipation . . . . internally limited

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}		3	5	5.5	V
Operating free-air temperature, T_A		–20	85		°C
Common mode input voltage, V_{ICM}	V_{DD} = 5 V	1.25	4.5		V
	V_{DD} = 3.3 V	1.25	2.7		

DC electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
I_{DD}	Quiescent current	V_{DD} = 5 V	ST, BTL		17	25	mA
			ST, SE		9	15	mA
			Mono, BTL		9	15	mA
			Mono, SE		5	10	mA
		V_{DD} = 3.3 V	ST, BTL		5.5	10	mA
			ST, SE		3.1	5	mA
			Mono, BTL		3.1	5	mA
			Mono, SE		1.9	3	mA
V_{odiff}	DC different output voltage	Gain = 2,	See Note 1		5	11	mV
$I_{DD(MUTE)}$	Supply current in Mute mode	V_{DD} = 5 V			670		µA
		V_{DD} = 3.3 V			450		
I_{SD}	I_{DD} in shutdown				1	10	µA

AC operating characteristic, $V_{DD} = 5$ V, $T_A = 25°C$, $R_L = 4\ \Omega$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$P_{(OUT)}$	Output power (each channel) see Note 2	THD = 0.2%,	BTL		1.25		W
		THD = 1%,	BTL		1.5		
		THD = 0.2%,	SE		500		mW
		THD = 1%,	SE		600		
THD+N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 – 20 kHz		200		m%
B_{OM}	Maximum output power bandwidth	G = 10,	THD < 5 %		>20		kHz
	Phase margin	BTL		66°	72°		
		Open Load		56°	71°		
		SE		46°	52°		
PSRR	Power supply ripple rejection	f = 1 kHz,		70	75		dB
		f = 20 – 20 kHz,		55	60		
	Mute attenuation				85		dB
	Channel-to-channel output separation				65		dB
	Line/HP input separation				100		dB
	BTL attenuation in SE mode				100		dB
Z_I	Input impendance						MΩ
V_n	Output noise voltage				25		uV(rms)

NOTES: 1. At 3 V < V_{DD} < 5 V the DC output voltage is approximately $V_{DD}/2$.
2. Output power is measured at the output pins of the IC at 1 kHz.

AC operating characteristic, $V_{DD} = 3.3$ V, $T_A = 25°C$, $R_L = 4\ \Omega$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$P_{(OUT)}$	Output power (each channel) see Note 2	THD = 0.2%	BTL		600		mW
		THD = 1%	BTL		750		
		THD = 0.2%,	SE		200		
		THD = 1%,	SE		250		
THD+N	Total harmonic distortion plus noise	P_O = 600 mW,	f = 20 – 20 kHz		250		m%
B_{OM}	Maximum output power bandwidth	G = 10,	THD < 5 %		>20		kHz
	Phase margin	BTL		78°	92°		deg
		Open Load		49°	70°		
		SE		52°	57°		
PSRR	Power supply ripple rejection	f = 1 kHz,		65	70		dB
		f = 20 – 20 kHz,		50	55		
	Mute attenuation				85		dB
	Channel-to-channel output separation				65		dB
	Line/HP input separation				100		dB
	BTL attenuation in SE mode				100		dB
Z_I	Input impendance						MΩ
V_n	Output noise voltage				25		uV(rms)

NOTES: 1. At 3 V < V_{DD} < 5 V the DC output voltage is approximately $V_{DD}/2$.
2. Output power is measured at the output pins of the 1 C at 1 kHz.

APPLICATION INFORMATION

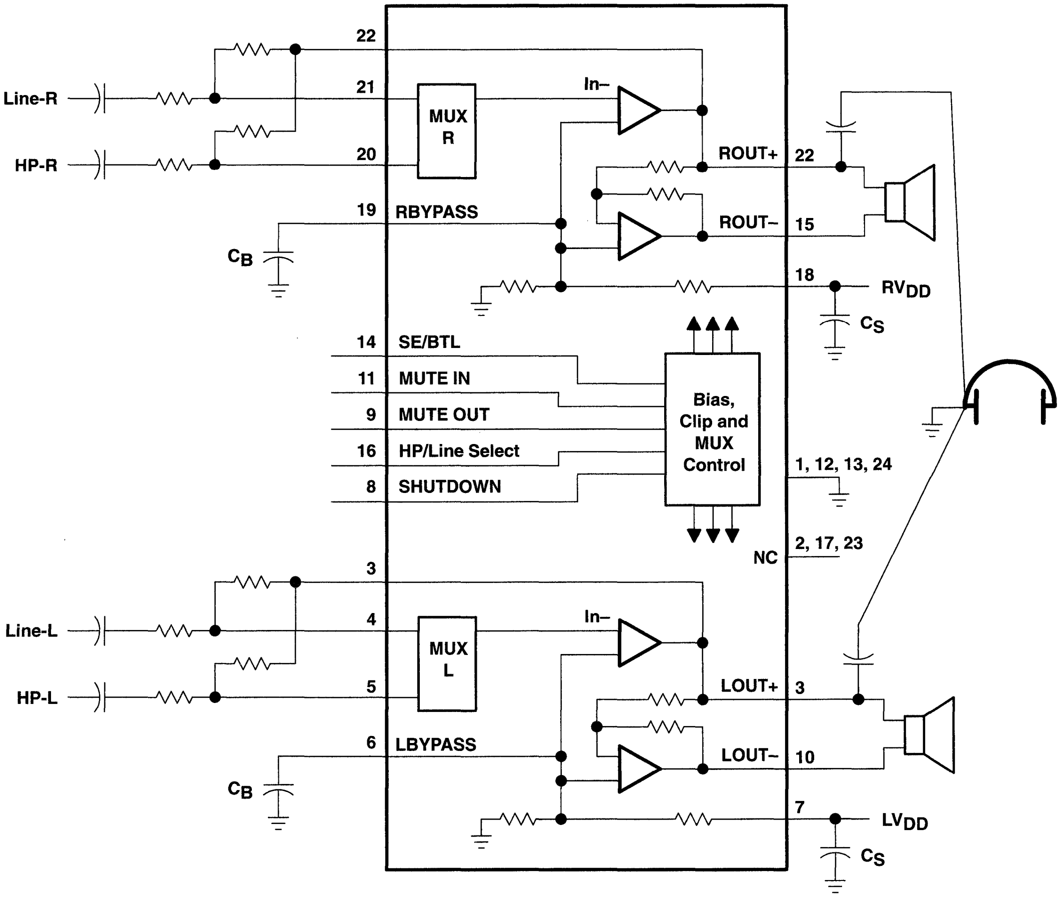


Figure 2. Typical Application Circuit

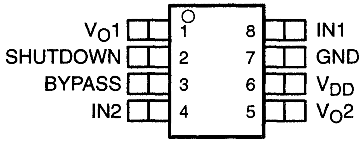
ADVANCE INFORMATION

TPA302, TPA302Y
300-mW STEREO AUDIO POWER AMPLIFIER

SLOS174A – JANUARY 1997 – REVISED MARCH 1997

- **300-mW Stereo Output**
- **PC Power Supply Compatibility 5-V and 3.3-V Specified Operation**
- **Shutdown Control**
- **Internal Mid-Rail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
- **Functional Equivalent of the LM4880**

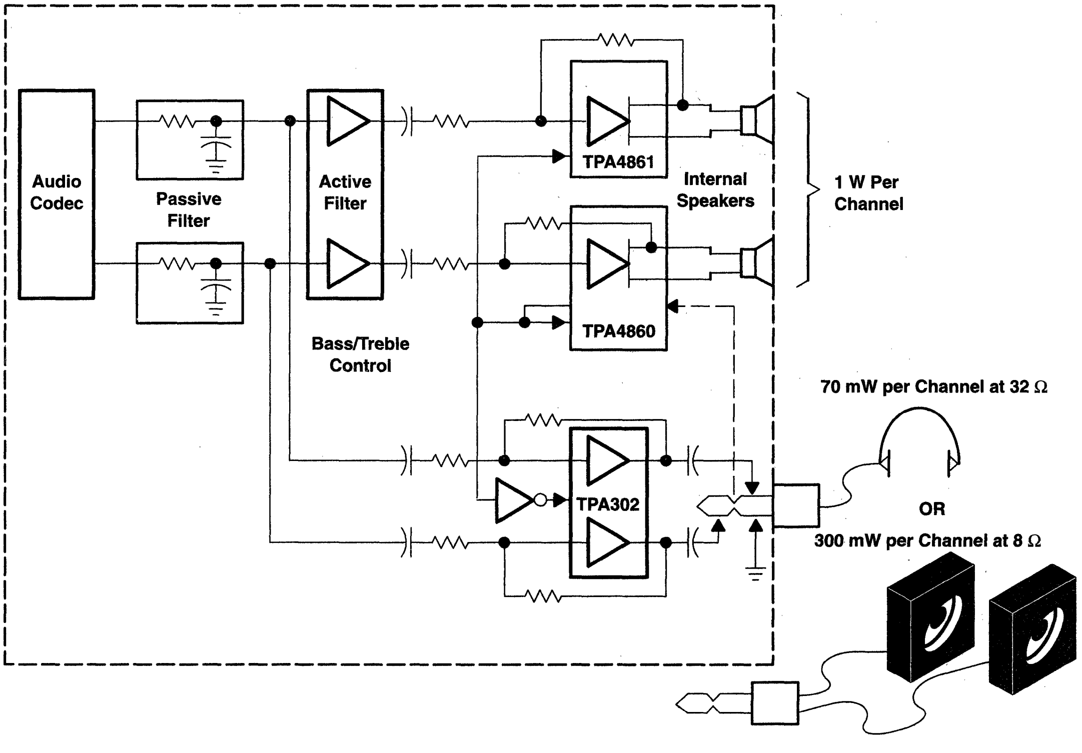
D PACKAGE
(TOP VIEW)



description

The TPA302 is a stereo audio power amplifier capable of delivering 250 mW of continuous average power into an 8-Ω load at less than 0.06% THD + N from a 5-V power supply or up to 300 mW at 1% THD + N. The TPA302 has high current outputs for driving small unpowered speakers at 8 Ω or headphones at 32 Ω. For headphone applications driving 32-Ω loads, the TPA302 delivers 60 mW of continuous average power at less than 0.06% THD + N. The amplifier features a shutdown function for power-sensitive applications as well as internal thermal and short-circuit protection. The amplifier is available in an 8-pin SOIC (D) package that reduces board space and facilitates automated assembly.

typical application circuit



AVAILABLE OPTIONS

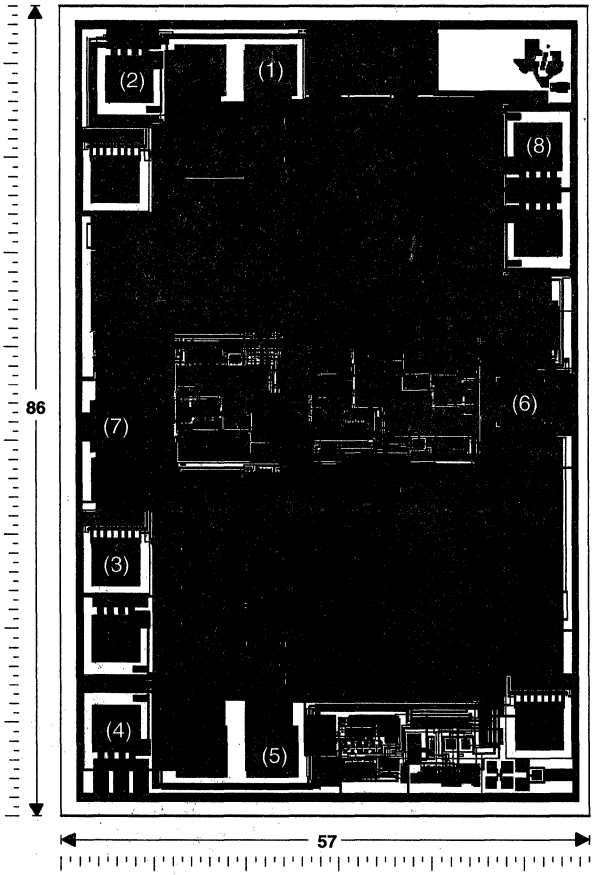
T_A	PACKAGED DEVICES	CHIP FORM
	SMALL OUTLINE† (D)	
−20°C to 85°C	TPA302D	TPA302Y

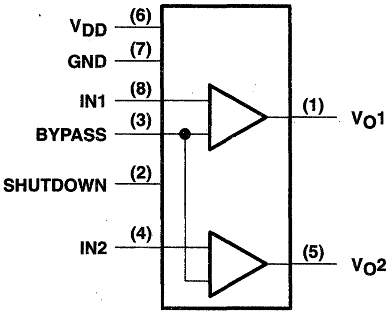
† The D packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TPA302DR)

TPA302Y chip information

This chip, when properly assembled, display characteristics similar to the TPA302. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (7) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{DD} .... 6 V
Input voltage , V_I .... –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation .... Internally Limited (See Dissipation Rating Table)
Operating junction temperature range, T_J .... –20°C to 150° C
Storage temperature range, T_{stg} .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	731 mW	5.8 mW/°C	460 mW	380 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.7	5.5	V
Operating free-air temperature, T_A	–20	85	°C

dc electrical characteristics at specified free-air temperature, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Quiescent current			2.25	5	mA
V_{IO}	Offset voltage			5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		55		dB
I_{SD}	Quiescent current in shutdown			0.6	20	µA

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
P_O	Output power	Gain = –1, f = 1 kHz	THD < 0.08%		100		mW
			THD < 1%		125		
			THD < 0.08%, R_L = 32 Ω		25		
			THD < 1%, R_L = 32 Ω		35		
B_{OM}	Maximum output power bandwidth	Gain = 10,	1% THD		20		kHz
B_1	Unity gain bandwidth	Open loop			1.5		MHz
	Channel separation	f = 1 kHz			75		dB
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz			45		dB
V_n	Noise output voltage	Gain = –1			10		µVrms

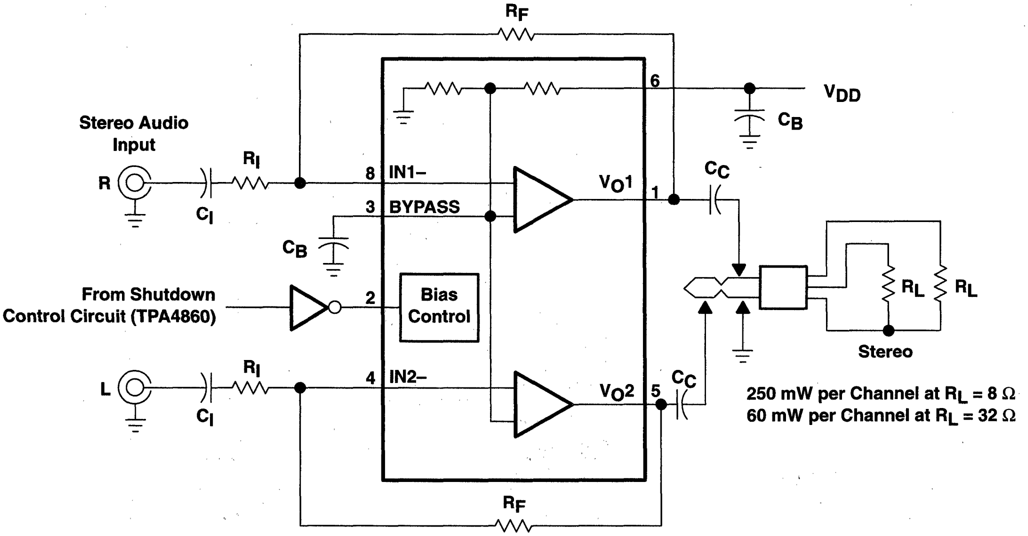
dc electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Quiescent current			4	10	mA
V_{IO}	Offset voltage	See Note 1		5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		65		dB
I_{SD}	Quiescent current in shutdown			0.6		µA

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
P_O	Output power	Gain = –1, f = 1 kHz	THD < 0.06%		250		mW
			THD < 1%		300		
			THD < 0.06%, R_L = 32 Ω		60		
			THD < 1%, R_L = 32 Ω		80		
B_{OM}	Maximum output power bandwidth	Gain = 10,	1% THD		20		kHz
B_1	Unity gain bandwidth	Open loop			1.5		MHz
	Channel separation	f = 1 kHz			75		dB
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz			45		dB
V_n	Noise output voltage	Gain = –1			10		µVrms

typical application



250 mW per Channel at R_L = 8 Ω
60 mW per Channel at R_L = 32 Ω

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1–3, 7–9, 13–15, 19–21
		vs Output power	4–6, 10–12 16–18, 22–24
I_{DD}	Supply current Supply current distribution	vs Supply voltage vs Free-air temperature	25 26
V_n	Output noise voltage	vs Frequency	27, 28
	Maximum package power dissipation	vs Free-air temperature	29
	Power dissipation	vs Output power	30, 31
$P_{O}max$	Maximum output power	vs Free-air temperature	32, 33
P_O	Output power	vs Load resistance vs Supply voltage	34 35
	Open loop response	vs Frequency	36
	Closed loop response	vs Frequency	37
	Crosstalk	vs Frequency	38, 39
PSRR	Power supply rejection ratio	vs Frequency	40, 41

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

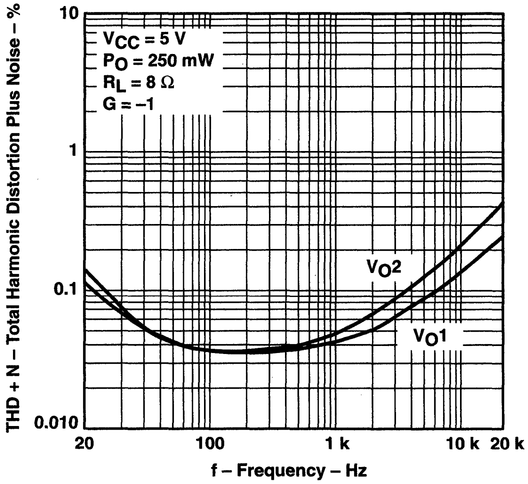


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

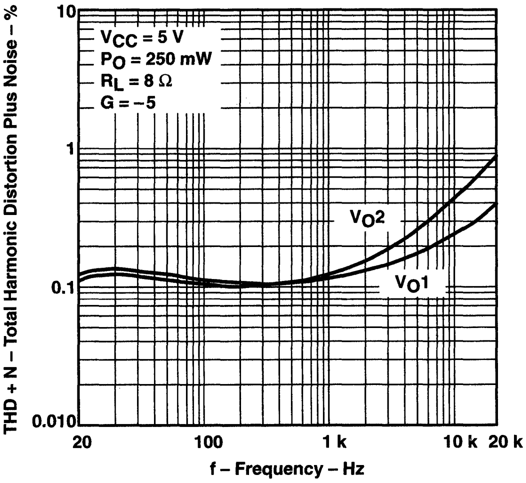


Figure 2

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

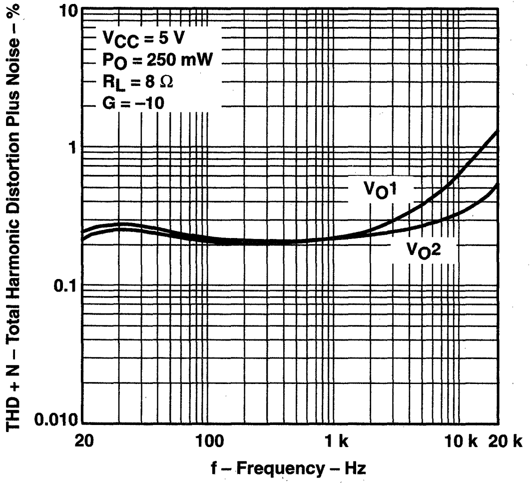


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

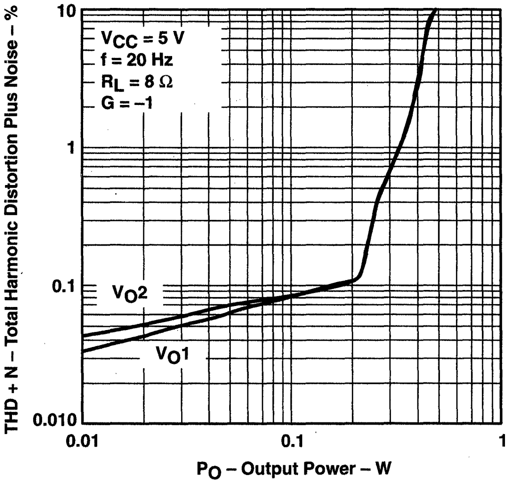


Figure 4

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

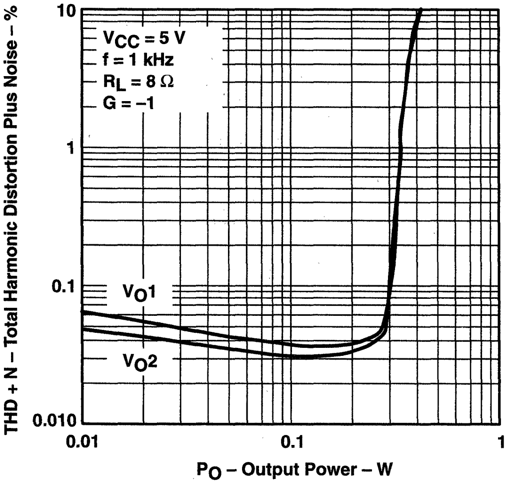


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

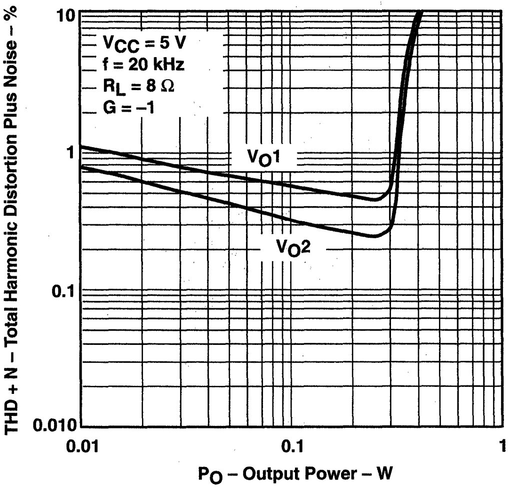


Figure 6

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

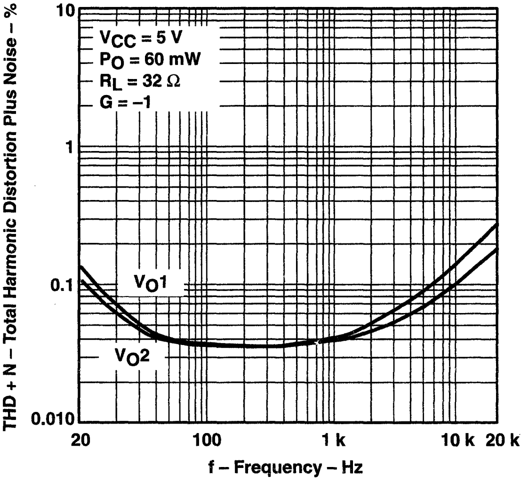


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

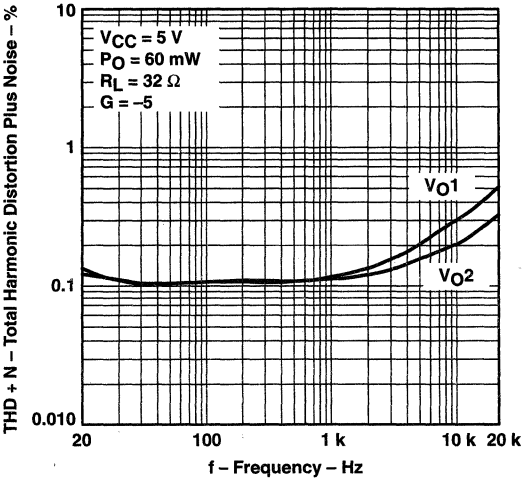


Figure 8

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

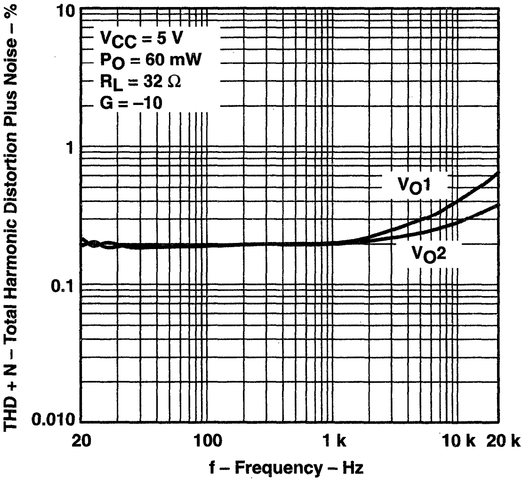


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

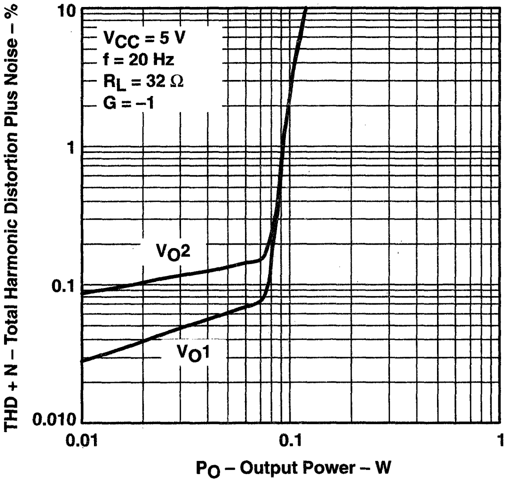


Figure 10

TYPICAL CHARACTERISTICS

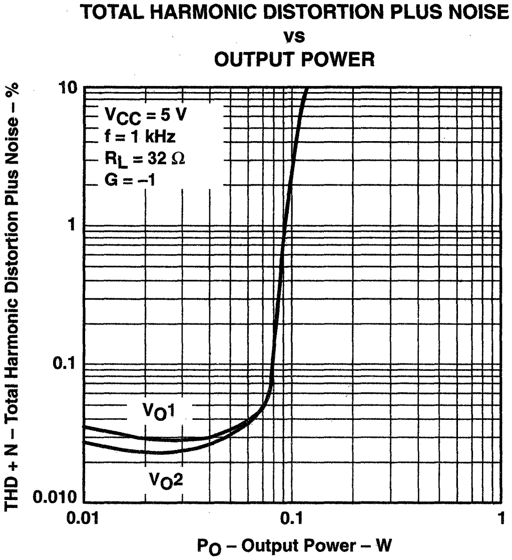


Figure 11

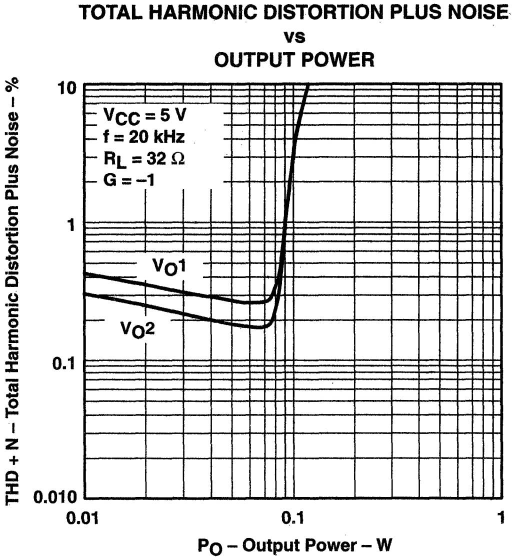


Figure 12

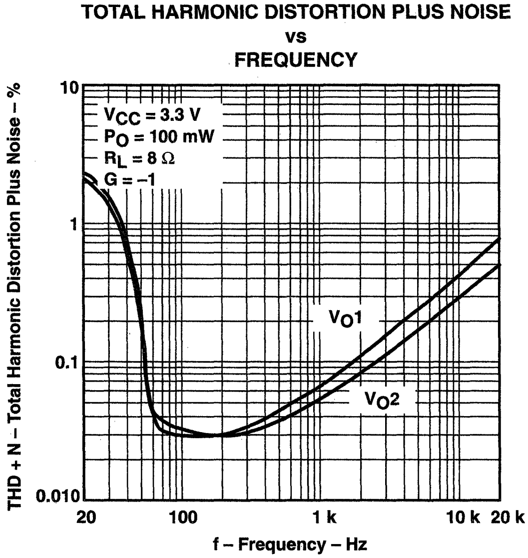


Figure 13

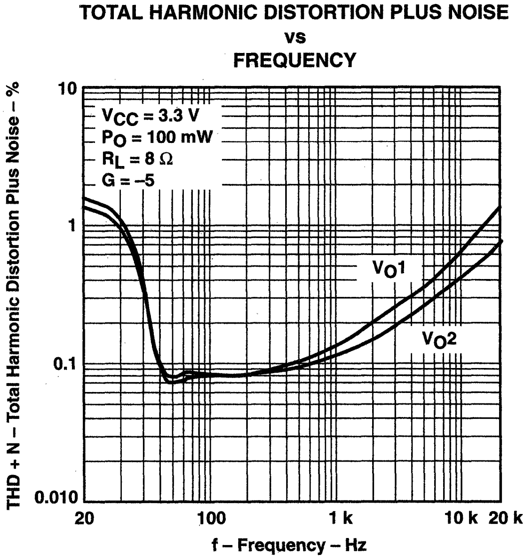


Figure 14

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

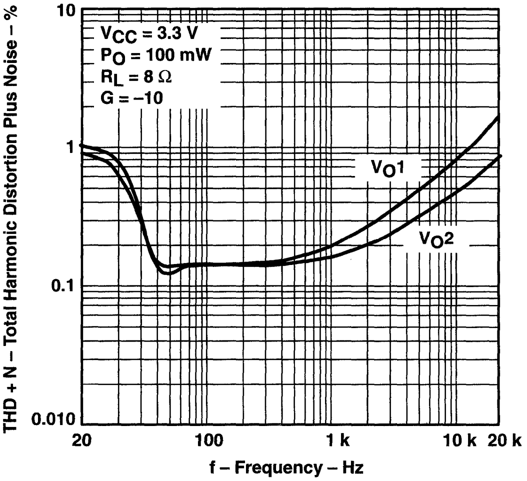


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

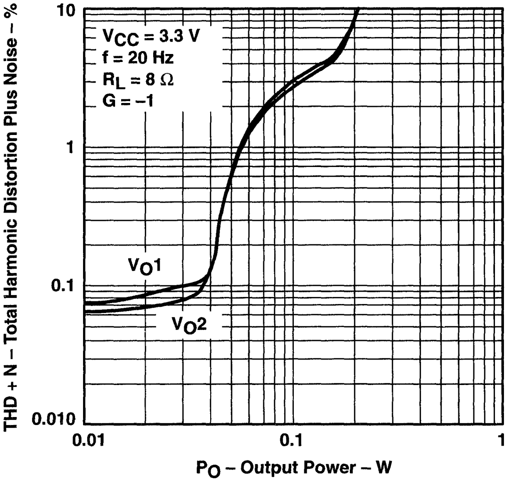


Figure 16

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

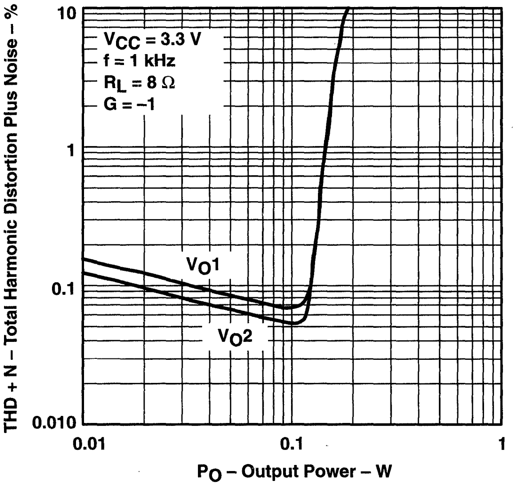


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

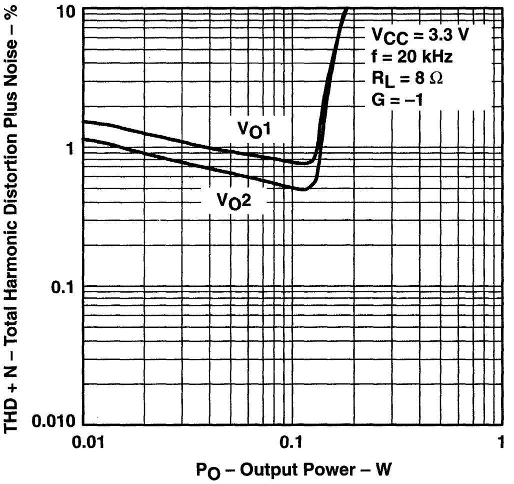


Figure 18

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

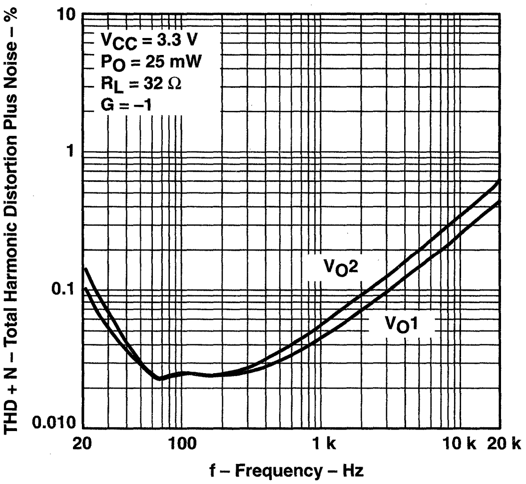


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

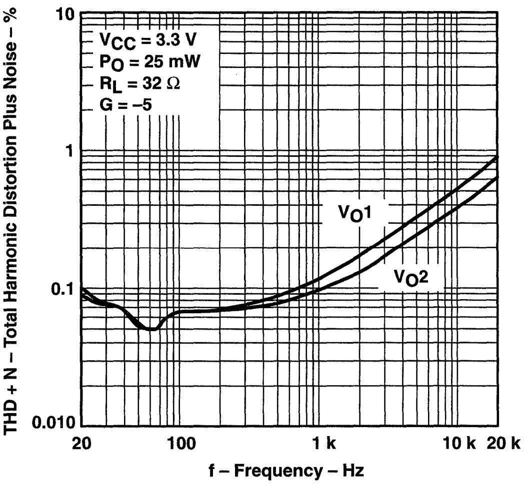


Figure 20

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

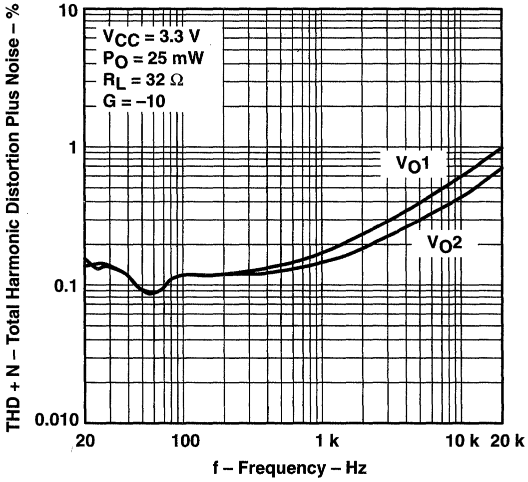


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

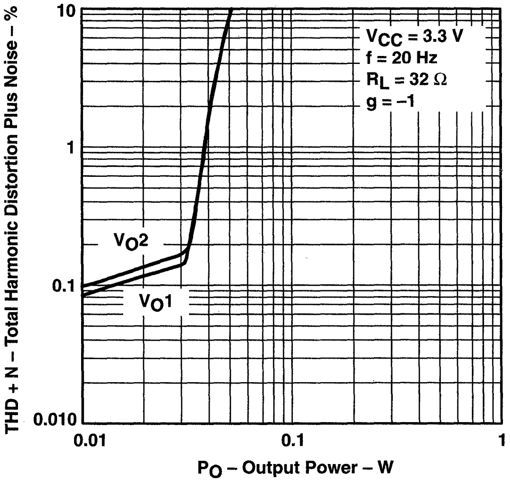


Figure 22

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

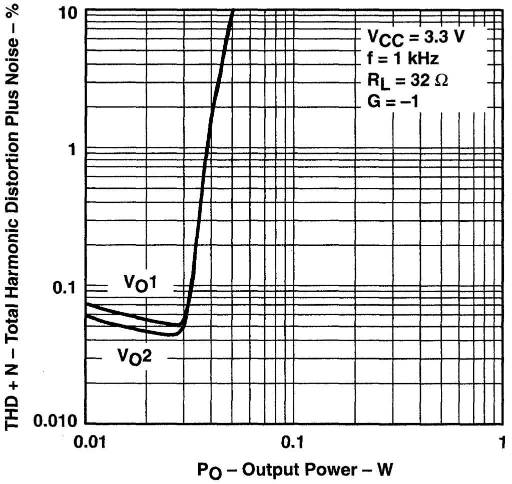


Figure 23

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

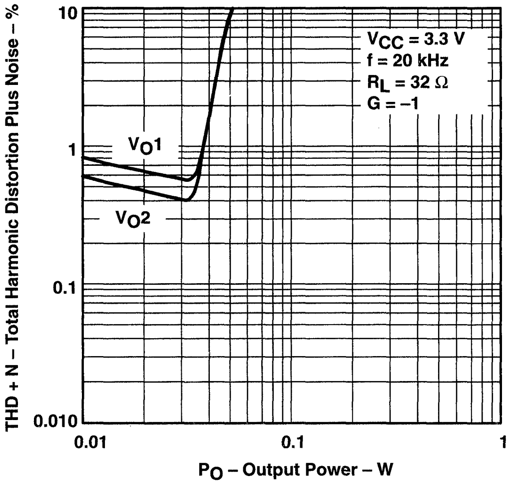


Figure 24

SUPPLY CURRENT vs SUPPLY VOLTAGE

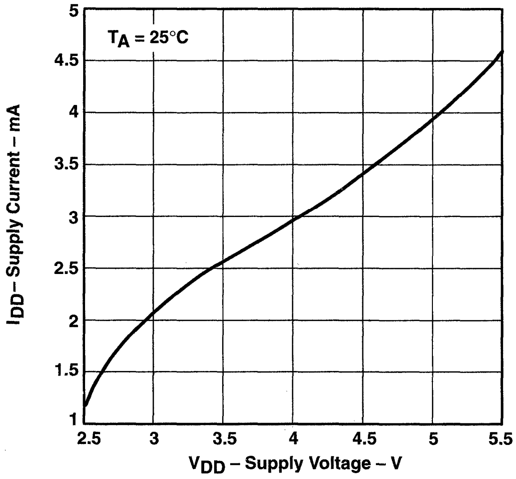


Figure 25

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

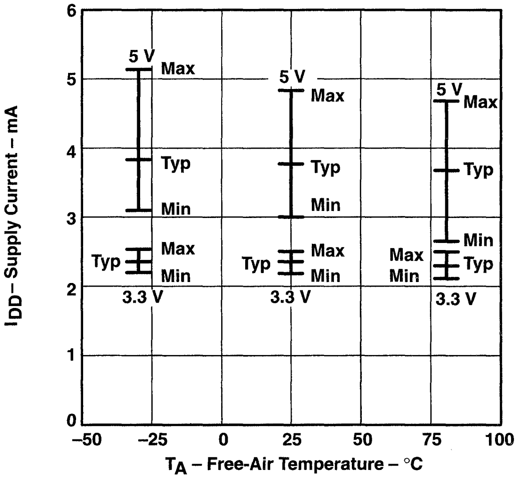


Figure 26

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE vs FREQUENCY

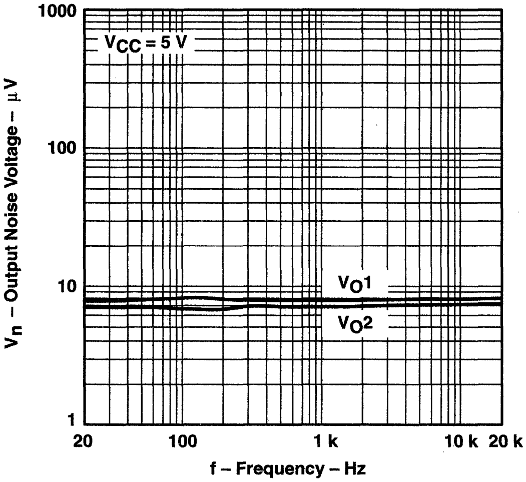


Figure 27

OUTPUT NOISE VOLTAGE vs FREQUENCY

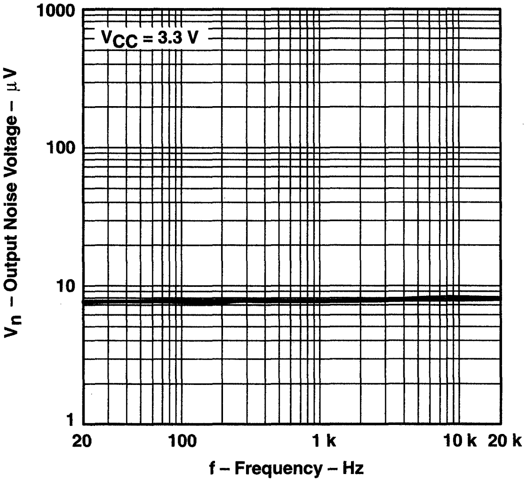


Figure 28

MAXIMUM PACKAGE POWER DISSIPATION vs FREE-AIR TEMPERATURE

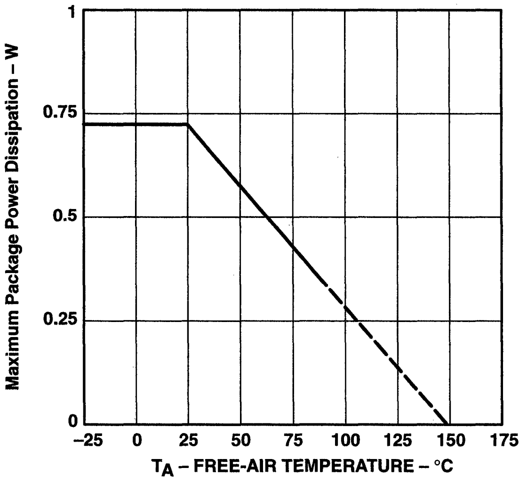


Figure 29

POWER DISSIPATION vs OUTPUT POWER

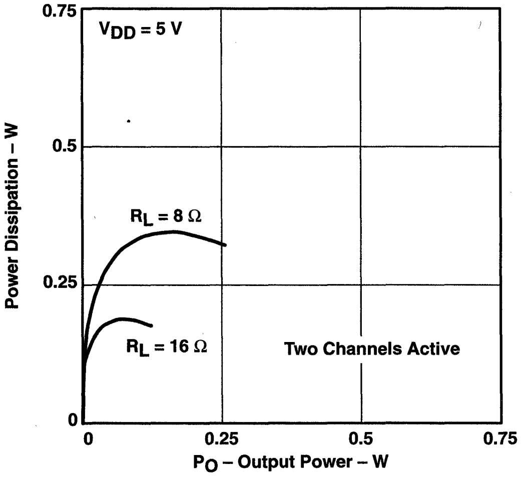


Figure 30

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs OUTPUT POWER

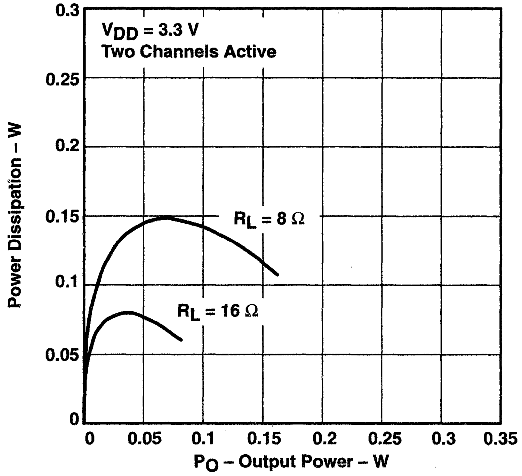


Figure 31

FREE-AIR TEMPERATURE vs MAXIMUM OUTPUT POWER

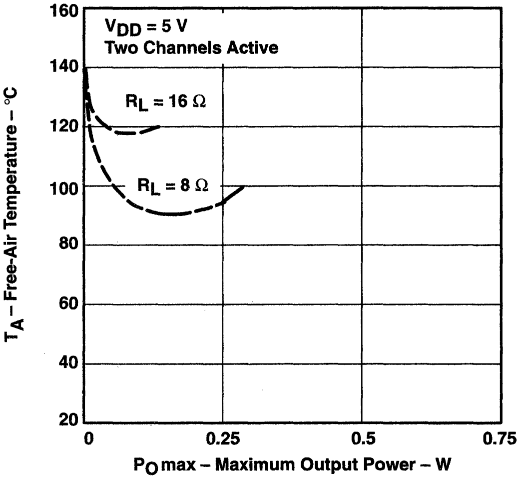


Figure 32

FREE-AIR TEMPERATURE vs MAXIMUM OUTPUT POWER

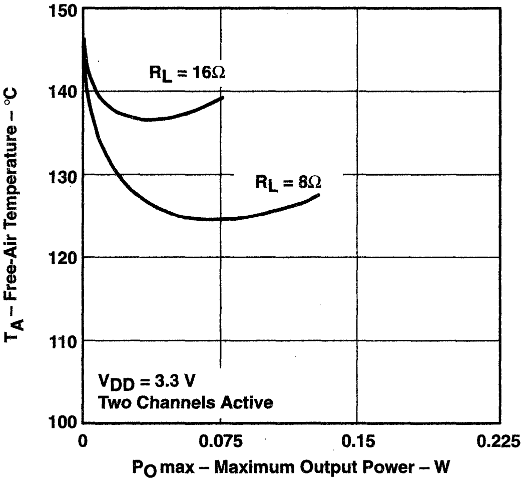


Figure 33

OUTPUT POWER vs LOAD RESISTANCE

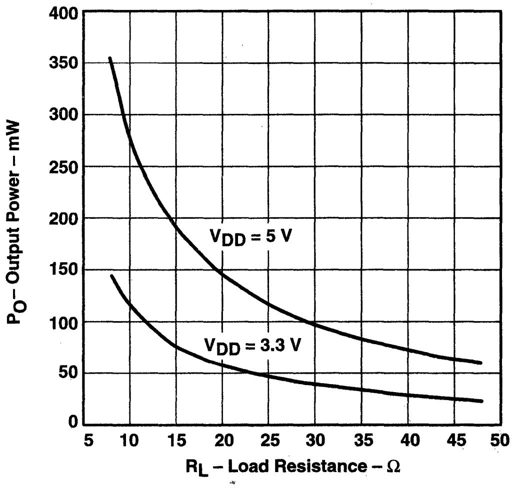


Figure 34

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
SUPPLY VOLTAGE

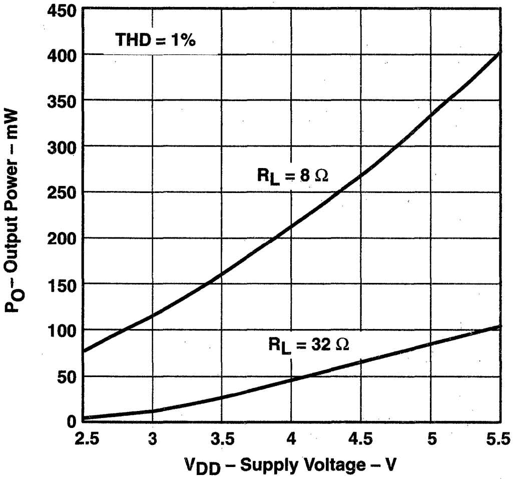


Figure 35

OPEN LOOP RESPONSE

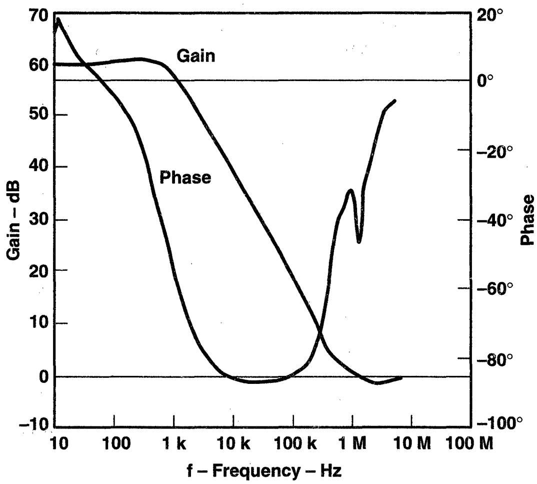


Figure 36

CLOSED LOOP RESPONSE

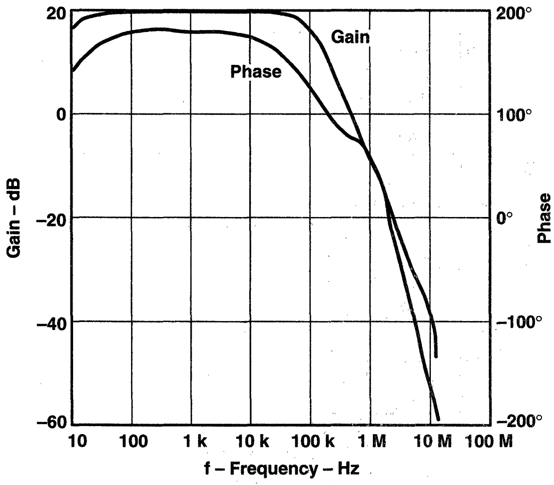


Figure 37

CROSSTALK
vs
FREQUENCY

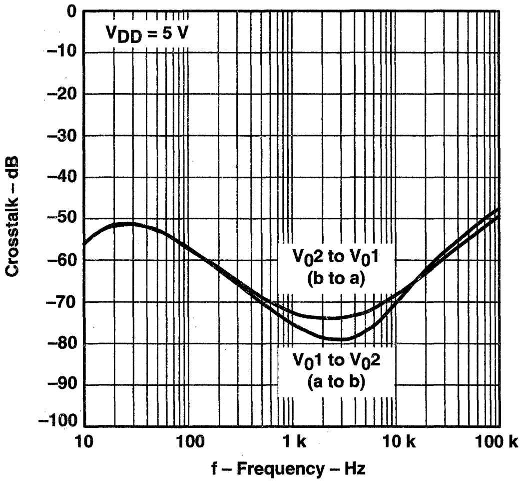


Figure 38

TYPICAL CHARACTERISTICS

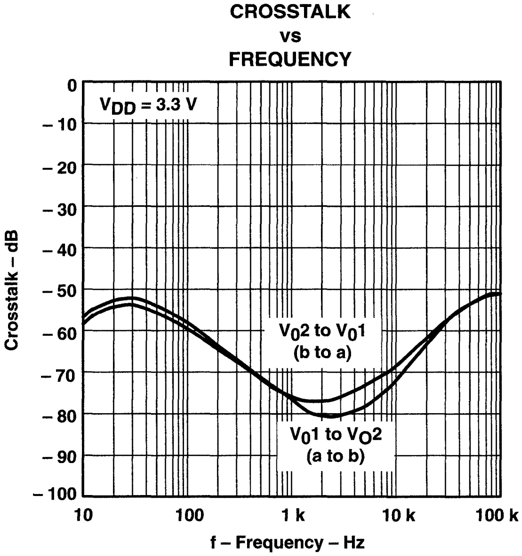


Figure 39

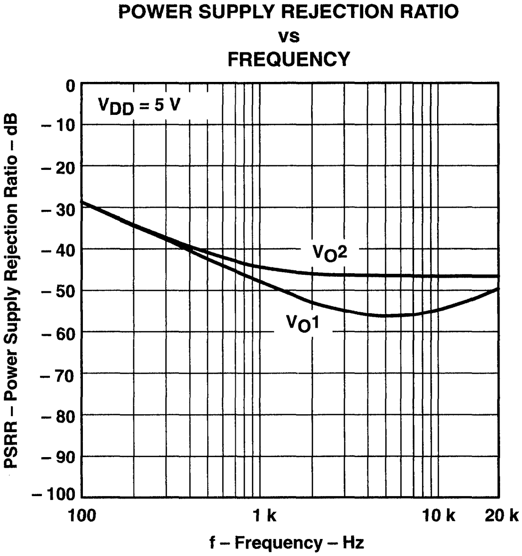


Figure 40

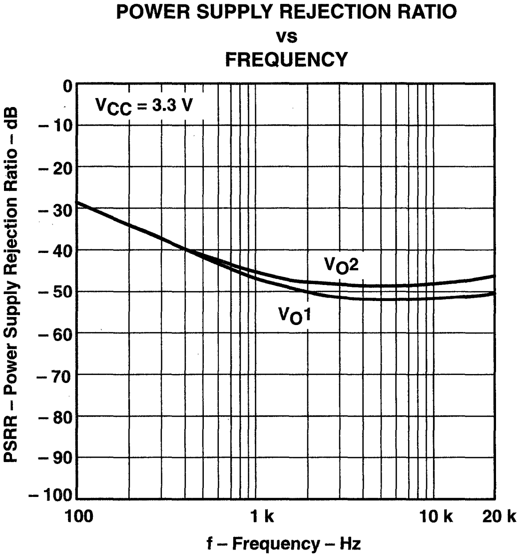
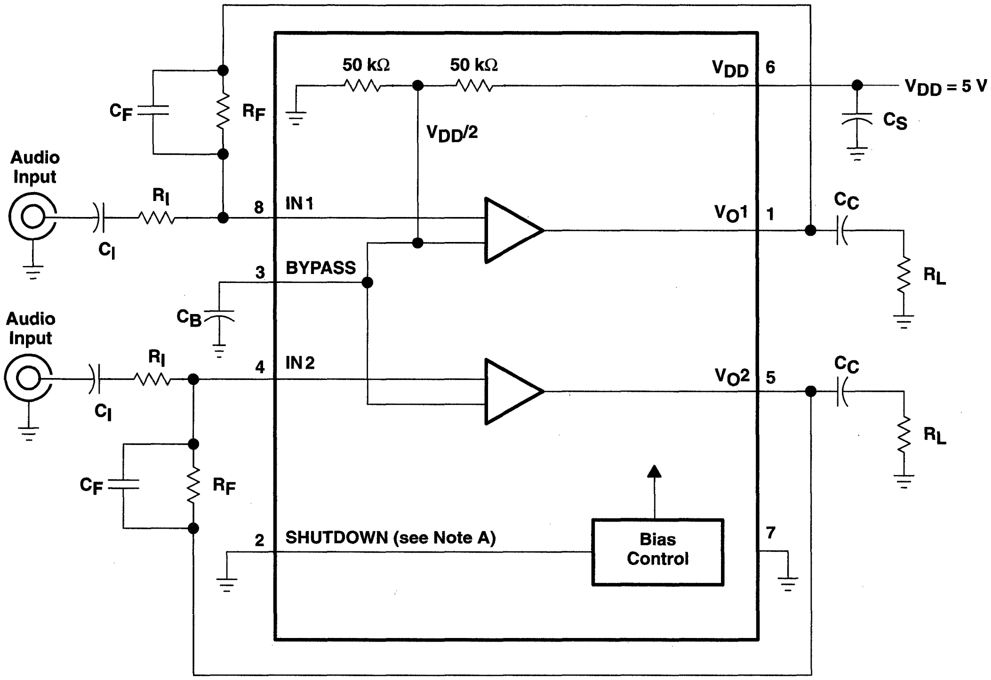


Figure 41

APPLICATION INFORMATION

selection of components

Figure 42 is a schematic diagram of a typical application circuit.



NOTE A: SHUTDOWN must be held low for normal operation and asserted high for shutdown mode.

Figure 42. TPA302 Typical Notebook Computer Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA302 is set by resistors R_F and R_I according to equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{1}$$

Given that the TPA302 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 2.

$$\begin{matrix}\text{Effective}\\ \text{Impedance}\end{matrix} = \frac{R_F R_I}{R_F + R_I} \tag{2}$$

As an example, consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The gain of the amplifier would be −5 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 3.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{3}$$

For example if R_F is 100 kΩ and C_F is 5 pF then $f_{co(lowpass)}$ is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 4.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \tag{4}$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 4 is reconfigured as equation 5.

$$C_I = \frac{1}{2\pi R_I f_{co(highpass)}} \tag{5}$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA302 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 6 should be maintained.

$$\frac{1}{\left(C_B \times 25\text{k}\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \tag{6}$$

As an example, consider a circuit where C_B is 0.1 µF, C_I is 0.22 µF and R_I is 10 kΩ. Inserting these values into the equation 9 results in:

$$400 \le 454$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 7.

$$f_{(\text{out high})} = \frac{1}{2\pi R_L C_C} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the load impedances are typically small, which drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 8 Ω, 32 Ω, and 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

Table 1. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
8 Ω	68 μF	293 Hz
32 Ω	68 μF	73 Hz
47,000 Ω	68 μF	0.05 Hz

As Table 1 indicates, most of the bass response is attenuated into 8-Ω loads while headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{1}{\left(C_B \times 25\ \text{k}\Omega\right)} \leq \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \tag{8}$$

shutdown mode

The TPA302 employs a shutdown mode of operation designed to reduce quiescent supply current, $I_{DD(q)}$, to the absolute minimum level during periods of nonuse for battery-power conservation. For example, during device sleep modes or when other audio-drive currents are used (i.e., headphone mode), the speaker drive is not required. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD(q)} < 1\ \mu A$. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

thermal considerations

A prime consideration when designing an audio amplifier circuit is internal power dissipation in the device. The curve in Figure 43 provides an easy way to determine what output power can be expected out of the TPA302 for a given system ambient temperature in designs using 5-V supplies. This curve assumes no forced airflow or additional heat sinking.

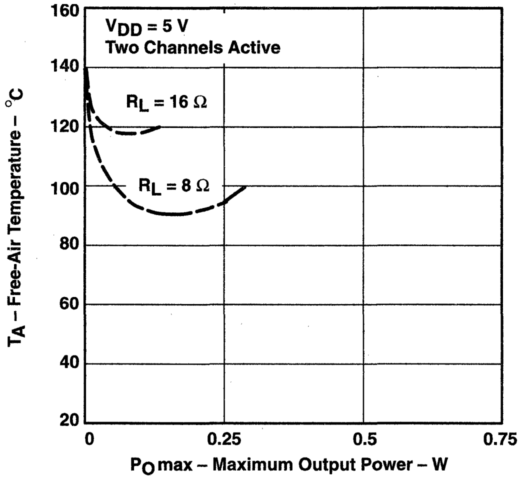


Figure 43. Free-Air Temperature Versus Maximum Output Power

5-V versus 3.3-V operation

The TPA302 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation since are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in the TPA302 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

TPA1517, TPA1517Y
6 WATT/CHANNEL STEREO AUDIO POWER AMPLIFIER

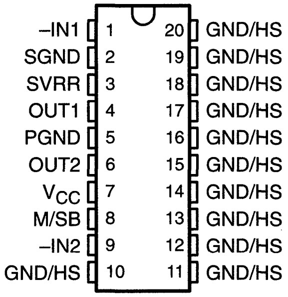
SLOS162 – MARCH 1997

- **TDA1517P Compatible**
- **Surface Mount Availability**
- **6-W Stereo Output (10% THD+N)**
- **Fixed Gain (20 dB)**
- **Mute and Standby Operation**
- **Thermal Protection**
- **Wide Supply Range (9.5 V – 18 V)**
- **High Power Supply Rejection (65-dB PSRR)**

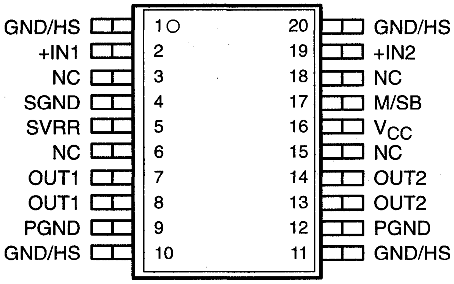
description

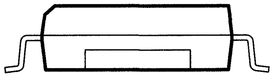
The TPA1517 is a stereo audio power amplifier that contains two identical amplifiers capable of delivering 6-W per channel of continuous average power into a 4-Ω load at 10% THD+N or 5-W per channel at 1% THD+N. The gain of each channel is fixed at 20-dB. The amplifier features a mute/standby function for power sensitive applications. The amplifier is available in a special 20-pin surface-mount thermally-enhanced package (DWP) that reduces board space and facilitates automated assembly while maintaining exceptional thermal characteristics.

NE PACKAGE
(TOP VIEW)



DWP PACKAGE
(TOP VIEW)





Cross Section View Showing Heat Sink

NC – No internal connection

AVAILABLE OPTIONS

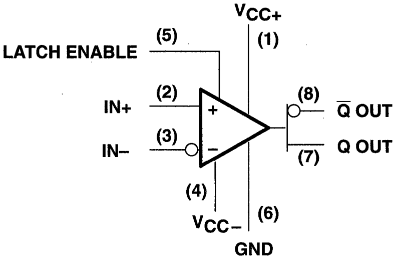
T_A	PACKAGED DEVICES		CHIP FORM (Y)
	THERMALLY ENHANCED PLASTIC DIP	THERMALLY ENHANCED SURFACE MOUNT	
0°C to 70°C	TPA1517NE	TPA1517DWP	TPA1517Y

ADVANCE INFORMATION

TPA1517Y chip information

This chip, when properly assembled, displays characteristics similar to the TPA1517C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . 22 V
Continuous total power dissipation . . . . Internally limited (See Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DWP	1930 mW	15.5 mW/°C	1233 mW	1000 mW

‡ With recommended copper heat sink pattern on PCB

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	6		18	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified free-air temperature, V_{CC} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Quiescent current			40		mA

NOTE 1: At 6 V < V_{CC} < 18 V the DC output voltage is approximately $V_{CC}/2$.

ADVANCE INFORMATION

operating characteristic, V_{CC} = 12 V, R_L = 4 Ω, f = 1 kHz, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power, see Note 2	THD = 0.2%	2.5	3	3.5	W
		THD < 10%	3.75	4	4.25	W
$I_{O(SM)}$	Non-repetitive peak output current			4		A
$I_{O(RM)}$	Repetitive peak output current			2.5		A
	Low-frequency roll-off	–3 dB		45		Hz
	High-frequency roll-off	–1 dB	20			kHz
	Supply voltage rejection	M/SB = On	48			dB
z_I	Input impedance			60		kΩ
V_n	Noise output voltage, see Note 3	R_S = 0, M/SB = On		50		µV(rms)
		R_S = 10 kΩ, M/SB = On		70	100	µV(rms)
		M/SB = Mute		50		µV(rms)
	Channel separation	R_S = 10 kΩ	40	60		dB
	Channel balance			0.1	1	dB

NOTES: 2. Output power is measured at the output pins of the IC.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

operating characteristic, V_{CC} = 12 V, R_L = 4 Ω, f = 1 kHz, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power, see Note 2	THD = 0.2%	4	4.5	5	W
		THD < 10%	5.5	6	6.5	W
$I_{O(SM)}$	Non-repetitive peak output current			4		A
$I_{O(RM)}$	Repetitive peak output current			2.5		A
	Low-frequency roll-off	–3 dB		45		Hz
	High-frequency roll-off	–1 dB	20			kHz
	Supply voltage rejection	M/SB = On	48			dB
z_I	Input impedance			60		kΩ
V_n	Noise output voltage, see Note 3	R_S = 0, M/SB = On		50		µV(rms)
		R_S = 10 kΩ, M/SB = On		70	100	µV(rms)
		M/SB = Mute		50		µV(rms)
	Channel separation	R_S = 10 kΩ	40	60		dB
	Channel balance			0.1	1	dB

NOTES: 3. Output power is measured at the output pins of the IC.
4. Noise voltage is mesured in a bandwidth of 20 Hz to 20 kHz.

ADVANCE INFORMATION

TYPICAL CHARACTERISTICS

Table of Graphs

				FIGURE
I_{CC}	Supply current		vs Supply voltage	1
PSSR	Power supply rejection ratio		vs Frequency	2, 3
THD + N	Total harmonic distortion plus noise	V_{CC} = 12 V	vs Frequency vs Power output	4, 5, 6 10, 11
		V_{CC} = 14.5 V	vs Frequency vs Power output	7, 8, 9 12, 13
	Crosstalk		vs Frequency	14, 15
	Gain margin		vs Frequency	16
	Phase shift		vs Frequency	16
V_N	Noise voltage		vs Frequency	17, 18
P_O	Output power		vs Supply voltage vs Load resistance	19 20
P_D	Power dissipation		vs Output power	21, 22

ADVANCE INFORMATION

ADVANCE INFORMATION

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

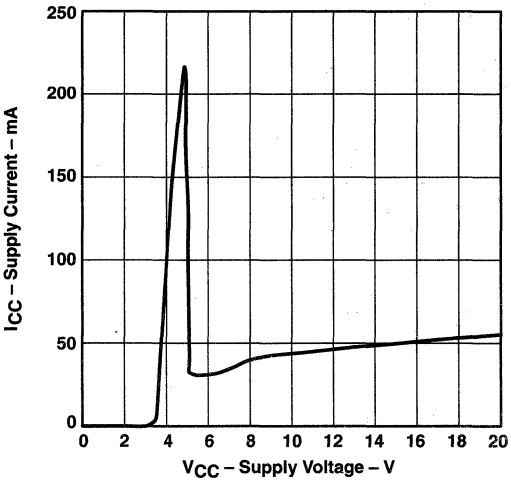


Figure 1

POWER SUPPLY REJECTION RATIO vs FREQUENCY

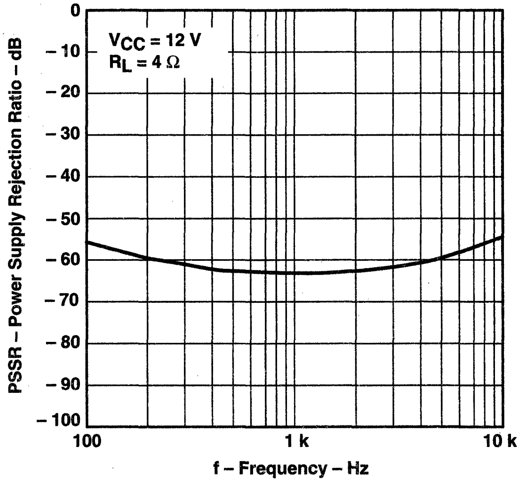


Figure 2

POWER SUPPLY REJECTION RATIO vs FREQUENCY

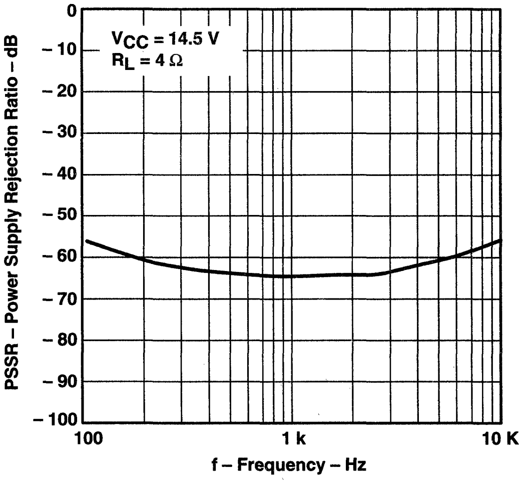


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

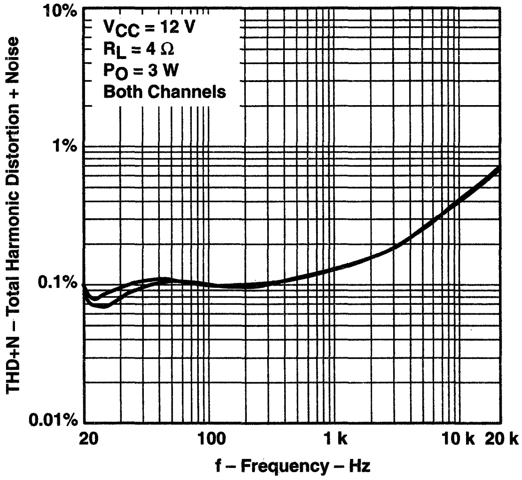


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

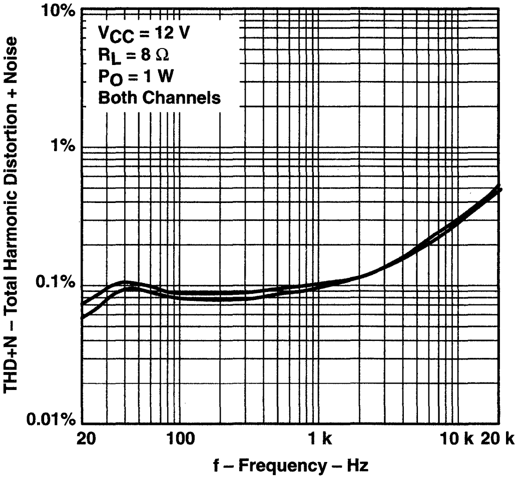


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

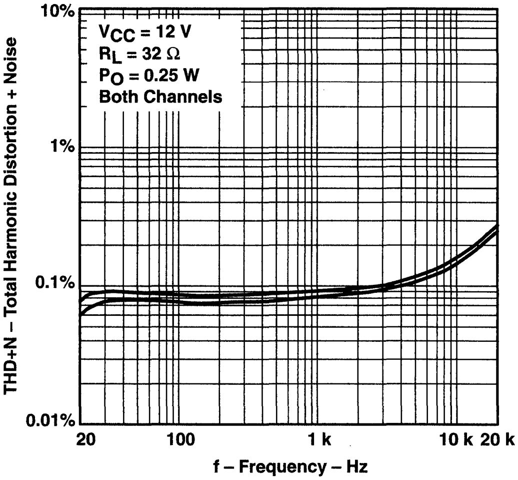


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

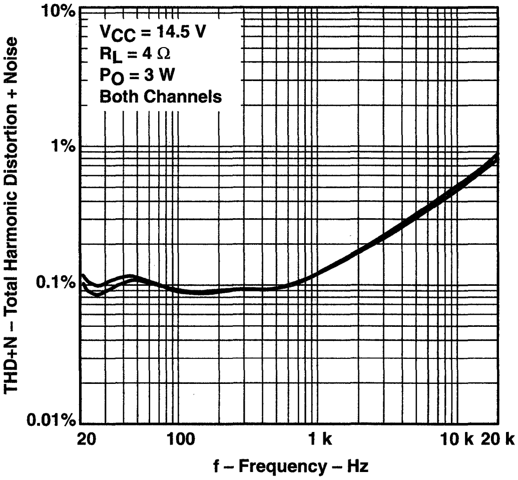


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

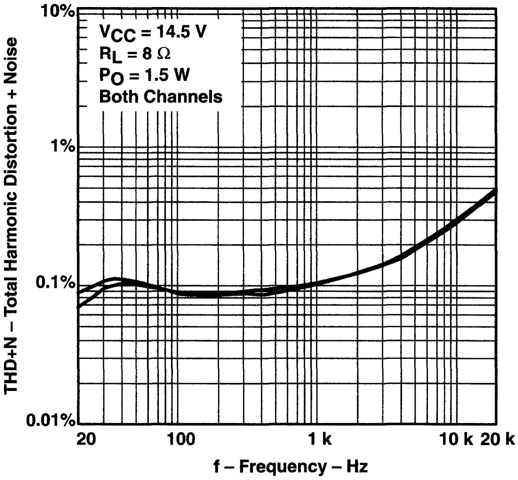


Figure 8

ADVANCE INFORMATION

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

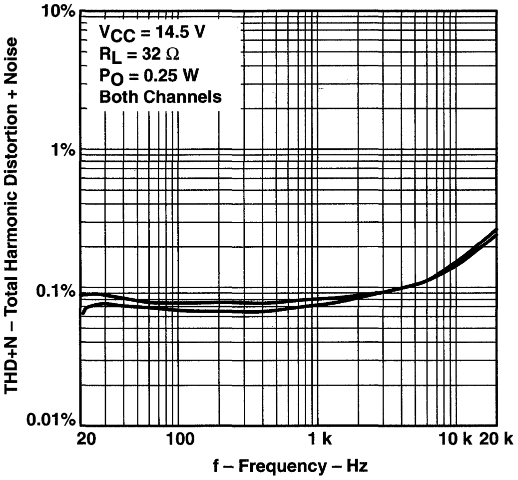


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs POWER OUTPUT

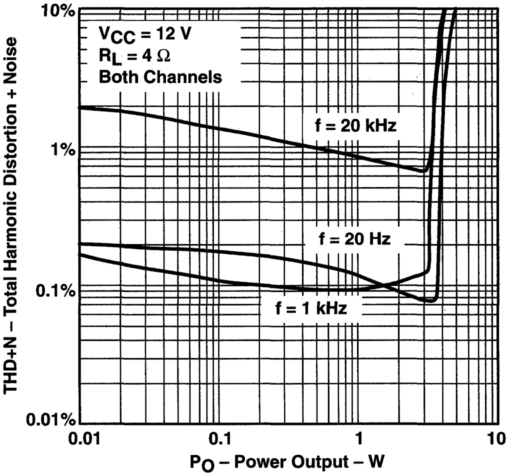


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs POWER OUTPUT

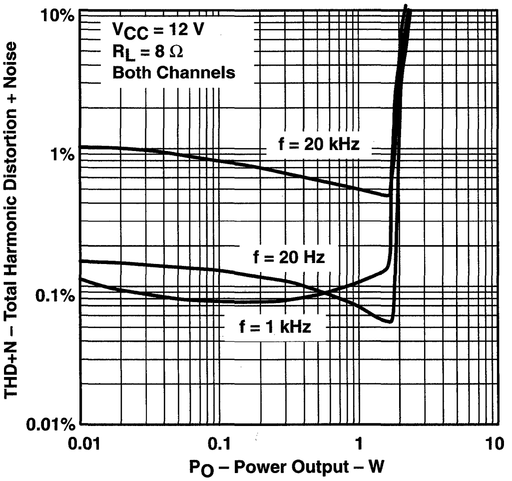


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs POWER OUTPUT

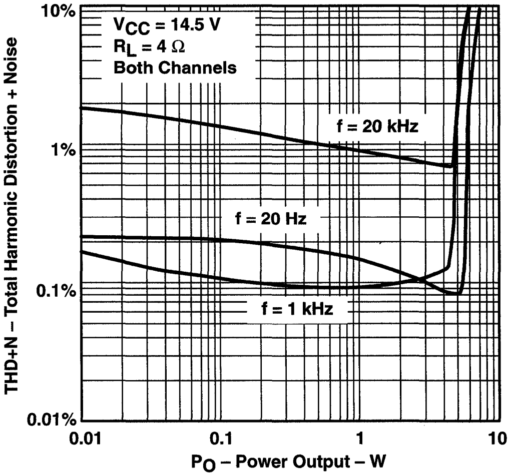


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs POWER OUTPUT

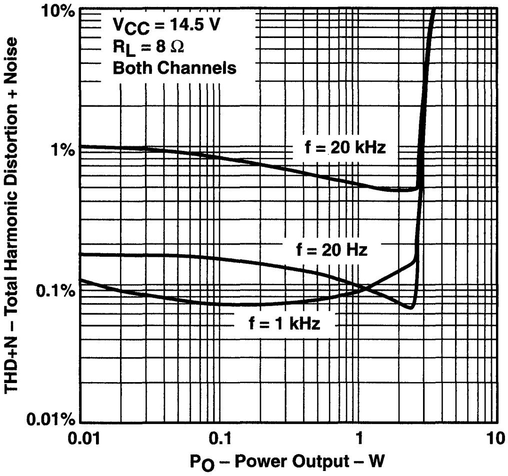


Figure 13

CROSSTALK vs FREQUENCY

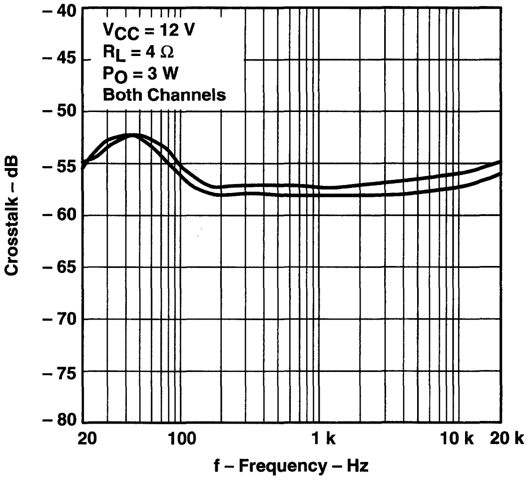


Figure 14

CROSSTALK vs FREQUENCY

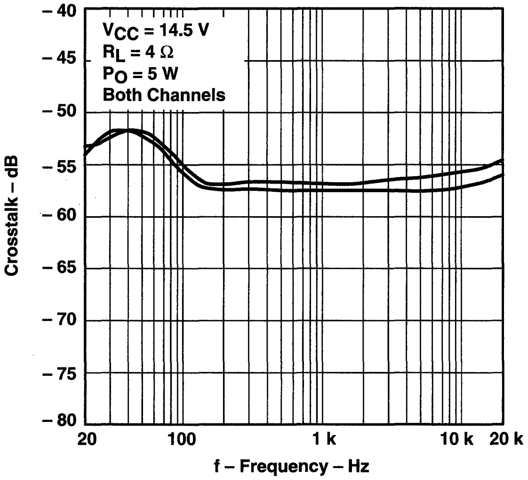


Figure 15

ADVANCE INFORMATION

TYPICAL CHARACTERISTICS

GAIN AND PHASE SHIFT vs FREQUENCY

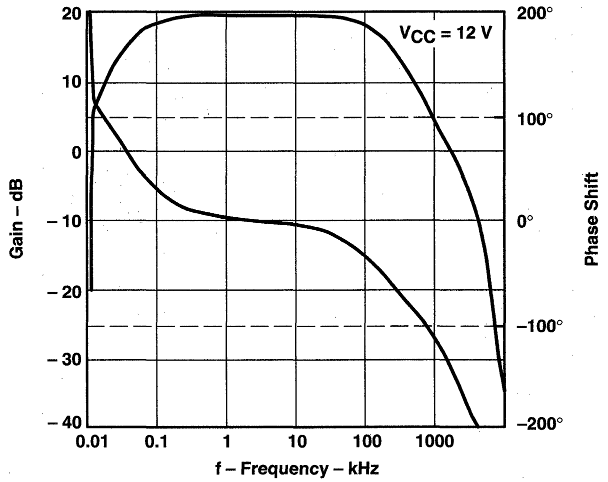


Figure 16

NOISE VOLTAGE vs FREQUENCY

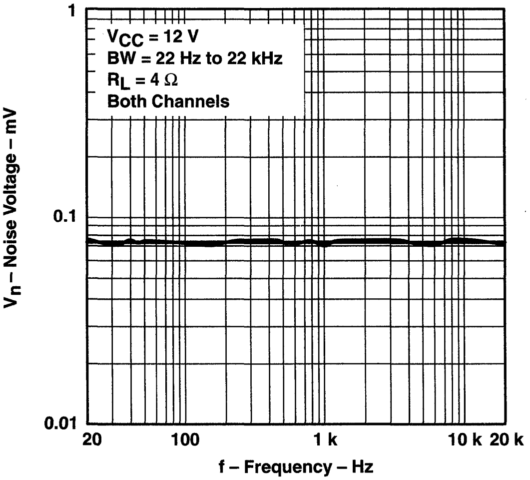


Figure 17

NOISE VOLTAGE vs FREQUENCY

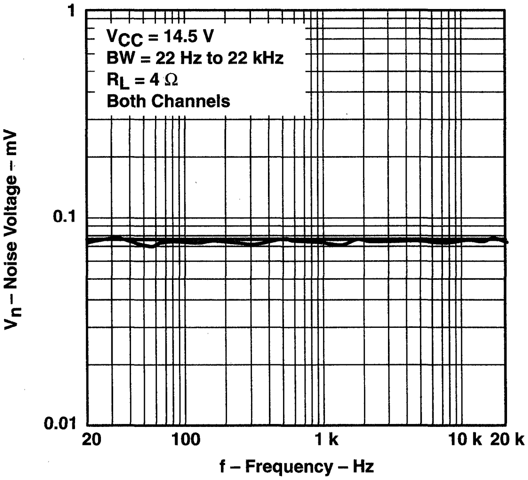


Figure 18

TYPICAL CHARACTERISTICS

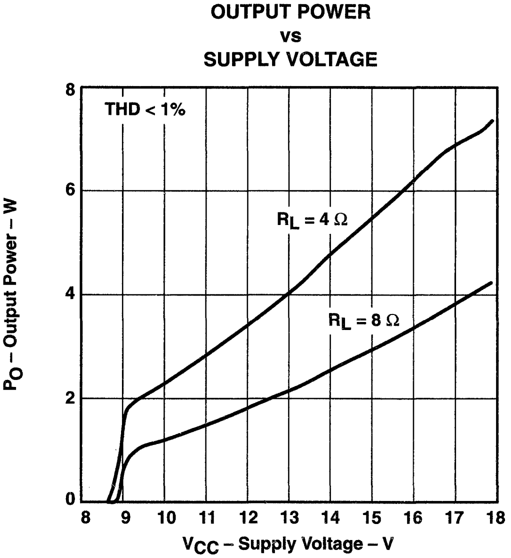


Figure 19

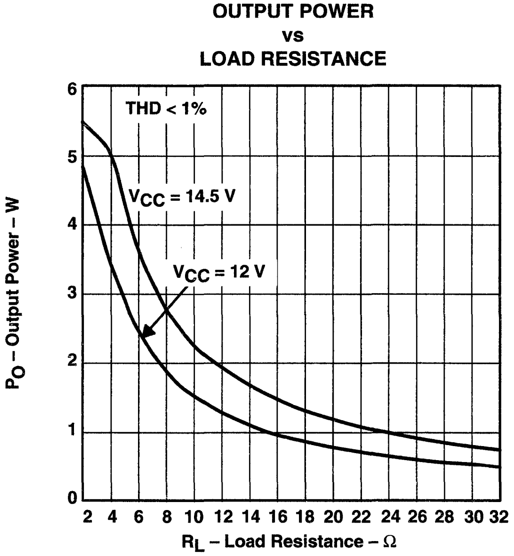


Figure 20

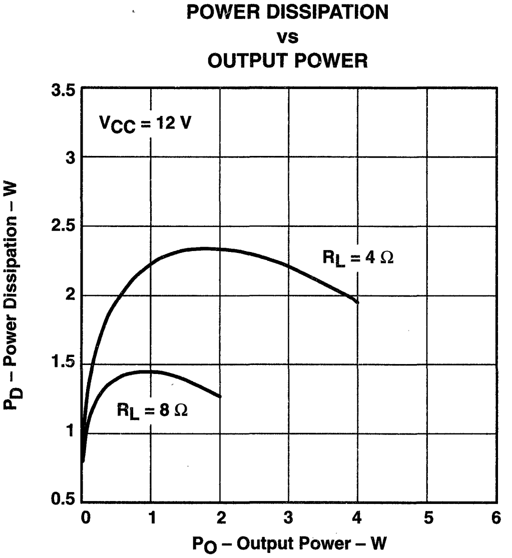


Figure 21

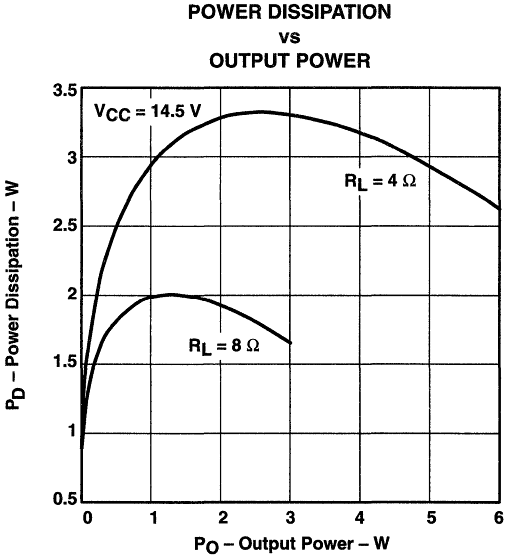


Figure 22

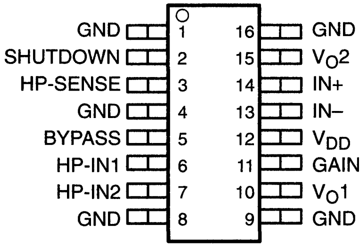
ADVANCE INFORMATION

TPA4860, TPA4860Y
1-WATT AUDIO POWER AMPLIFIER

SLOS164 – SEPTEMBER 1996

- **1-W BTL Output (5 V, 0.2 % THD+N)**
- **3.3-V and 5-V Operation**
- **No Output Coupling Capacitors Required**
- **Shutdown Control (I_{DD} = 0.6 μA)**
- **Headphone Interface Logic**
- **Uncompensated Gains of 2 to 20 (BTL Mode)**
- **Surface Mount Packaging**
- **Thermal and Short-Circuit Protection**
- **High Power Supply Rejection (56-dB at 1 kHz)**
- **LM4860 Drop-In Compatible**

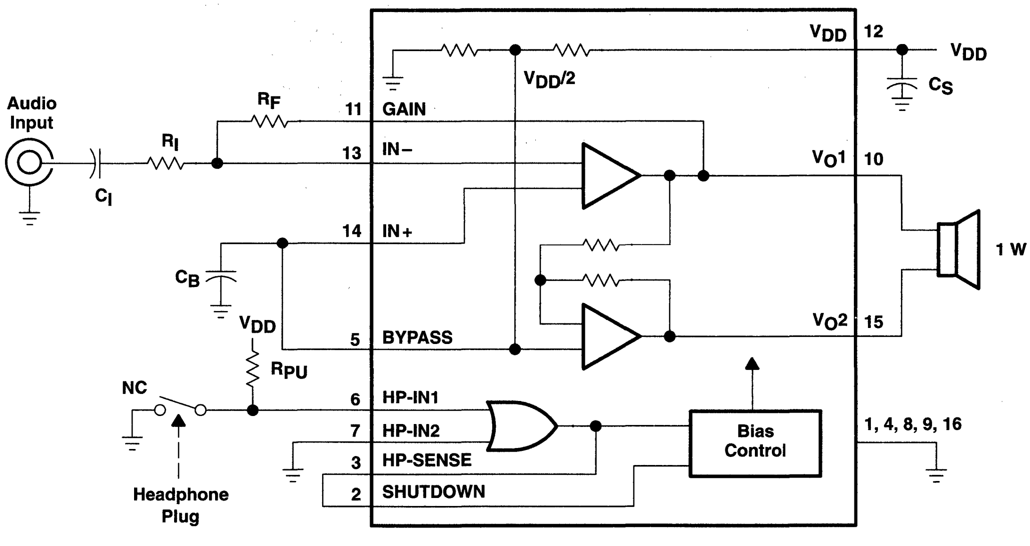
D PACKAGE
(TOP VIEW)



description

The TPA4860 is a bridge-tied load (BTL) audio power amplifier capable of delivering 1 W of continuous average power into an 8-Ω load at 0.4 % THD+N from a 5-V power supply in voiceband frequencies (f < 5 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output in most applications. Gain is externally configured by means of two resistors and does not require compensation for settings of 2 to 20. Features of this amplifier are a shutdown function for power-sensitive applications as well as headphone interface logic that mutes the output when the speaker drive is not required. Internal thermal and short-circuit protection increases device reliability. It also includes headphone interface logic circuitry to facilitate headphone applications. The amplifier is available in a 16-pin SOIC surface-mount package that reduces board space and facilitates automated assembly.

typical application circuit



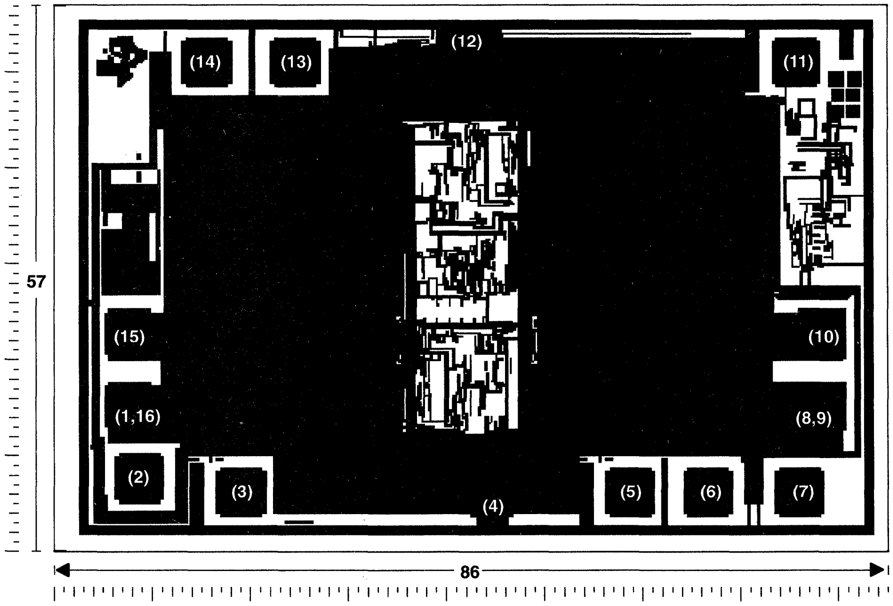
AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	CHIP FORM
	SMALL OUTLINE (D)	
−20°C to 85°C	TPA4860D	TPA4860Y

TPA4860Y chip information

This chip, when properly assembled, displays characteristics similar to the TPA4860C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINAL (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD}	6 V
Input voltage, V_I	–0.3 V to V_{DD} +0.3 V
Continuous total power dissipation	internally limited (See Dissipation Rating Table)
Operating free-air temperature range, T_A	–20°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

---

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
D	1250 mW	10 mW/°C	800 mW	650 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2.7	5.5	V
Common-mode input voltage, V_{IC}	V_{DD} = 3.3 V	1.25	2.7	V
	V_{DD} = 5 V	1.25	4.5	V
Operating free-air temperature, T_A		–20	85	°C

electrical characteristics at specified free-air temperature range, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4860			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1		5	20	mV
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{OO}$)	V_{DD} = 3.2 V to 3.4 V		75		dB
$I_{DD(q)}$	Quiescent current			2.5		mA
$I_{DD(m)}$	Quiescent current, mute mode			750		µA
$I_{DD(sd)}$	Quiescent current, shutdown mode			0.6		µA
V_{IH}	High-level input voltage (HP-IN)			1.7		V
V_{IL}	Low-level input voltage (HP-IN)			1.7		V
V_{OH}	High-level output voltage (HP-SENSE)	I_O = 100 µA	2.5	2.8		V
V_{OL}	Low-level output voltage (HP-SENSE)	I_O = –100 µA		0.2	0.8	V

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4860			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = 2		350		mW
			THD = 2%, f = 1 kHz, A_V = 2		500		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 3		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

electrical characteristics at specified free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4860 MIN	TPA4860 TYP	TPA4860 MAX	UNIT
V_{OO}	Output offset voltage	See Note 1		5	20	mV
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{OO}$)	V_{DD} = 4.9 V to 5.1 V		70		dB
$I_{DD(q)}$	Quiescent current			3.5		mA
$I_{DD(m)}$	Quiescent current, mute mode			750		µA
$I_{DD(sd)}$	Quiescent current, shutdown mode			0.6		µA
V_{IH}	High-level input voltage (HP-IN)			2.5		V
V_{IL}	Low-level input voltage (HP-IN)			2.5		V
V_{OH}	High-level output voltage (HP-SENSE)	I_O = 500 µA	2.5	2.8		V
V_{OL}	Low-level output voltage (HP-SENSE)	I_O = −500 µA		0.2	0.8	V

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristic, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4860 MIN	TPA4860 TYP	TPA4860 MAX	UNIT
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = 2		1000		mW
			THD = 2%, f = 1 kHz, A_V = 2		1100		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 3		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

electrical characteristics at specified free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4860Y			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1		5		mV
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{OO}$)	V_{DD} = 4.9 V to 5.1 V		70		dB
$I_{DD(q)}$	Quiescent current			3.5		mA
$I_{DD(m)}$	Quiescent current, mute mode			750		µA
$I_{DD(sd)}$	Quiescent current, shutdown mode			0.6		µA
V_{IH}	High-level input voltage (HP-IN)			2.5		V
V_{IL}	Low-level input voltage (HP-IN)			2.5		V
V_{OH}	High-level output voltage (HP-SENSE)	I_O = 500 µA		2.8		V
V_{OL}	Low-level output voltage (HP-SENSE)	I_O = –500 µA		0.2		V

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristic, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4860Y			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = 2		1000		mW
			THD = 2%, f = 1 kHz, A_V = 2		1100		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 4		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OO}	Output offset voltage	Distribution	1,2
I_{DD}	Supply current distribution	vs Free-air temperature	3,4
THD+N	Total harmonic distortion plus noise	vs Frequency	5,6,7,8,9, 10,11,15, 16,17,18
		vs Output power	12,13,14, 19,20,21
I_{DD}	Supply current	vs Supply voltage	22
V_n	Output noise voltage	vs Frequency	23,24
	Maximum package power dissipation	vs Free-air temperature	25
	Power dissipation	vs Output power	26,27
	Maximum output power	vs Free-air temperature	28
	Output power	vs Load Resistance	29
		vs Supply Voltage	30
	Open loop frequency response	vs Frequency	31
PSRR	Power supply rejection ratio	vs Frequency	32,33

TYPICAL CHARACTERISTICS

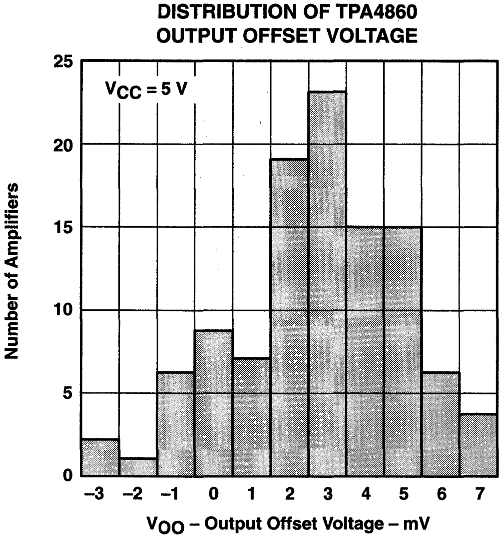


Figure 1

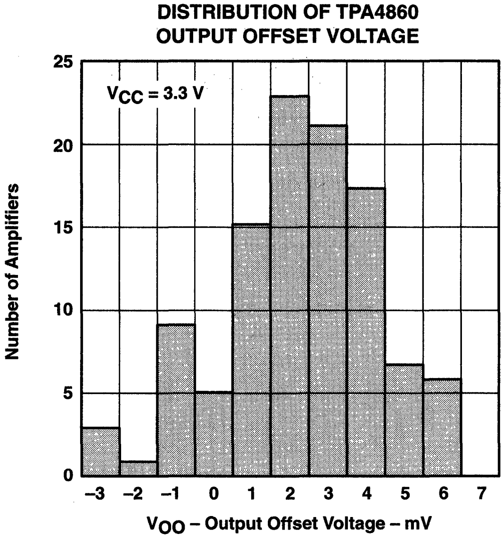


Figure 2

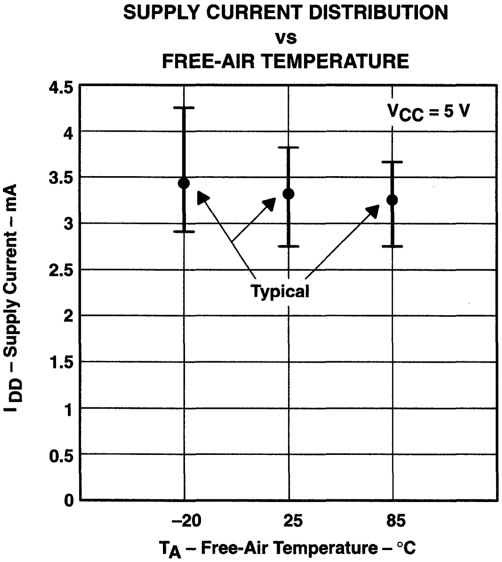


Figure 3

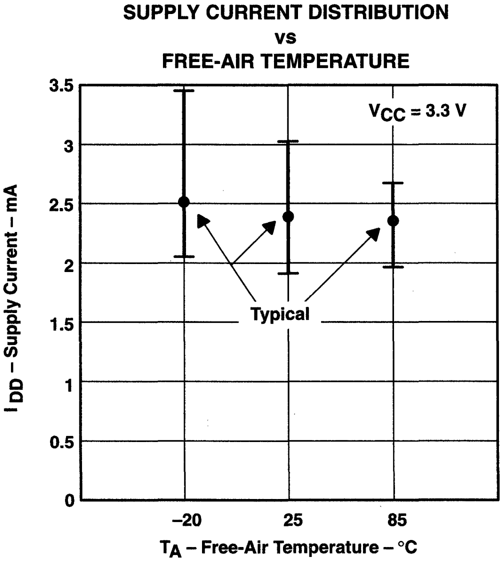


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

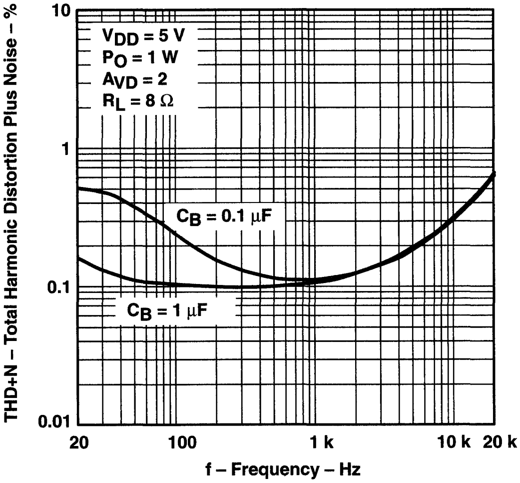


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

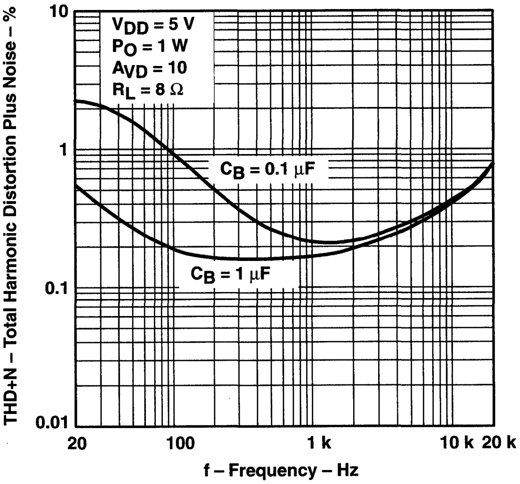


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

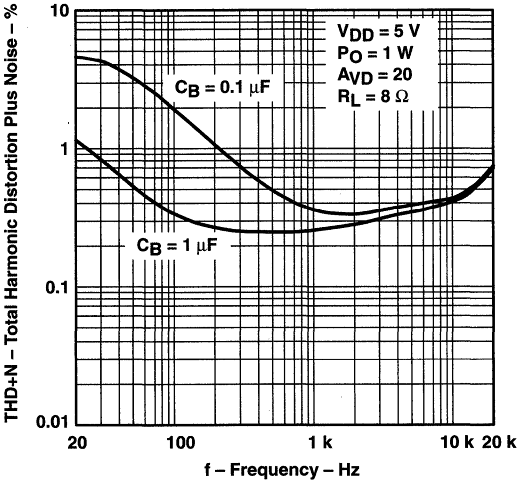


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

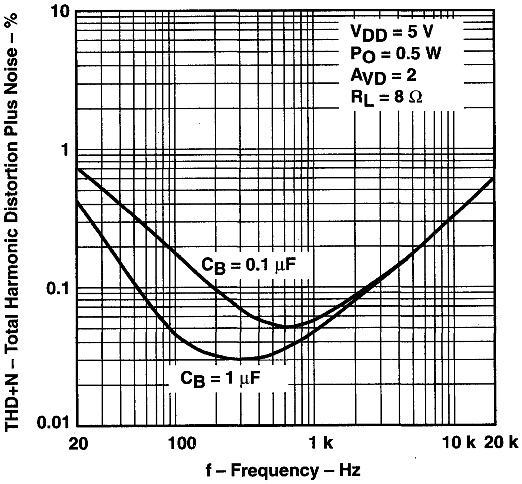


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

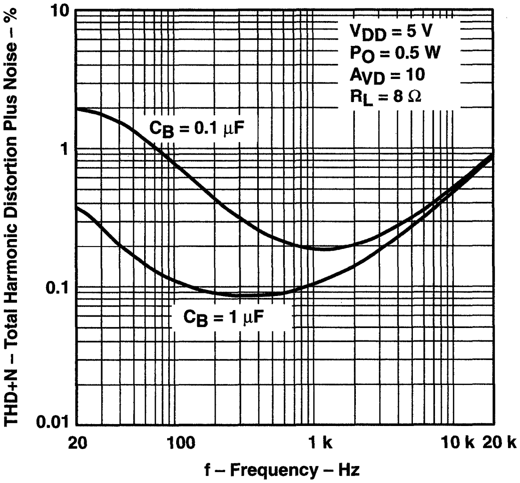


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

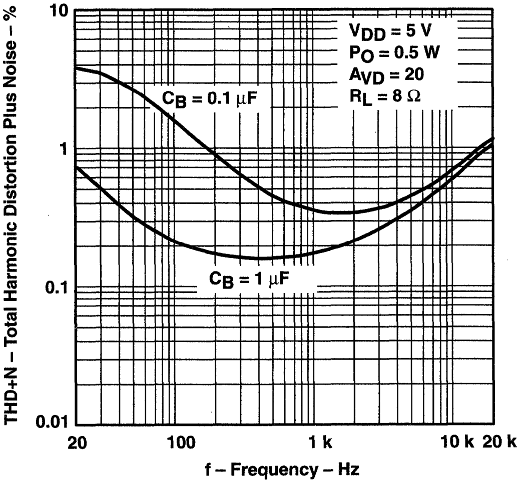


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

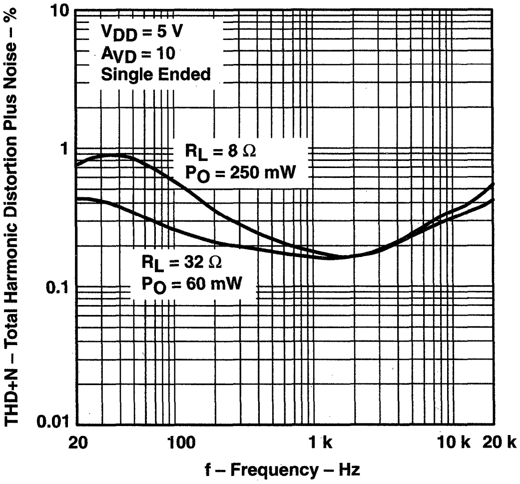


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

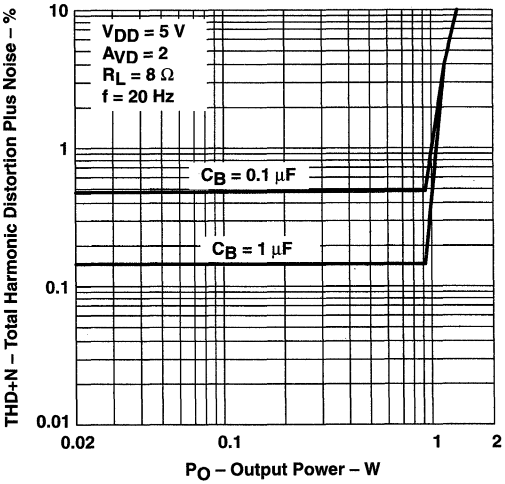


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

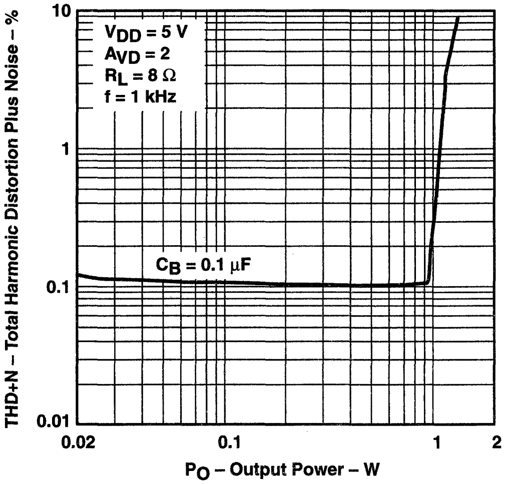


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

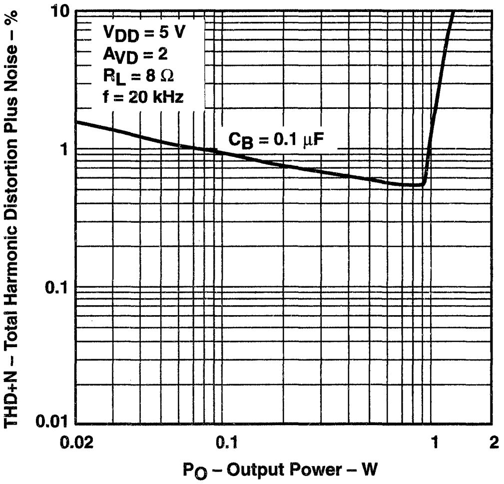


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

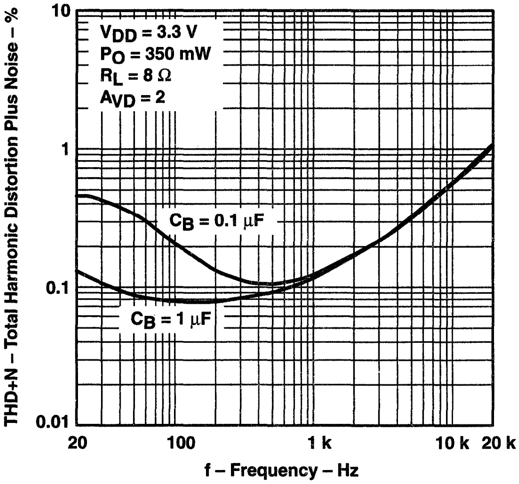


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

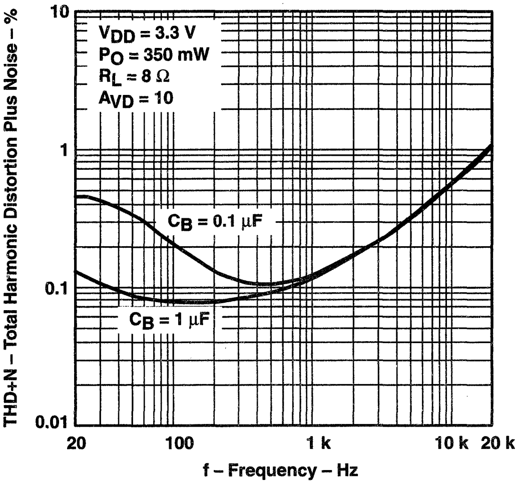


Figure 16

TYPICAL CHARACTERISTICS

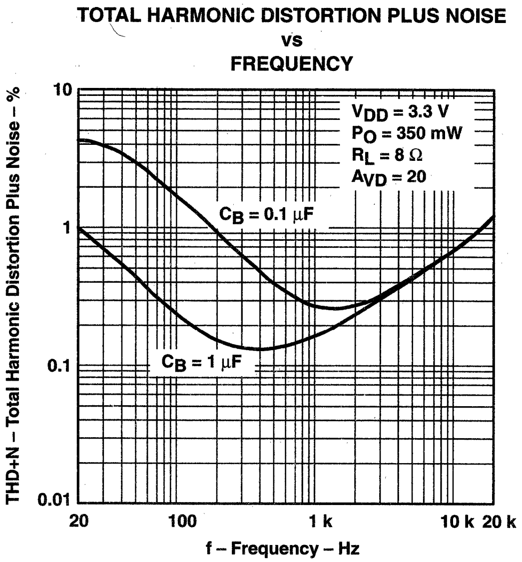

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 17

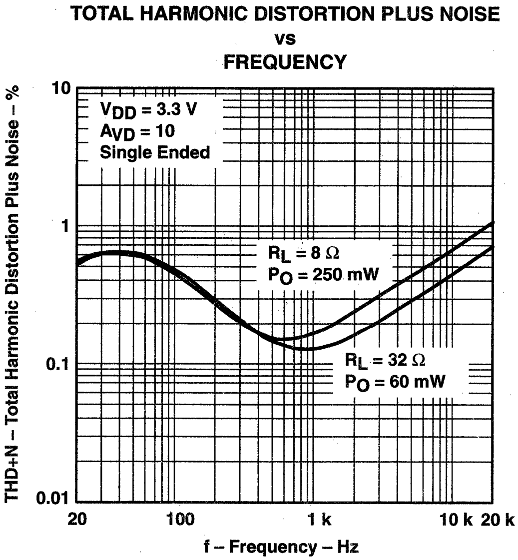

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 18

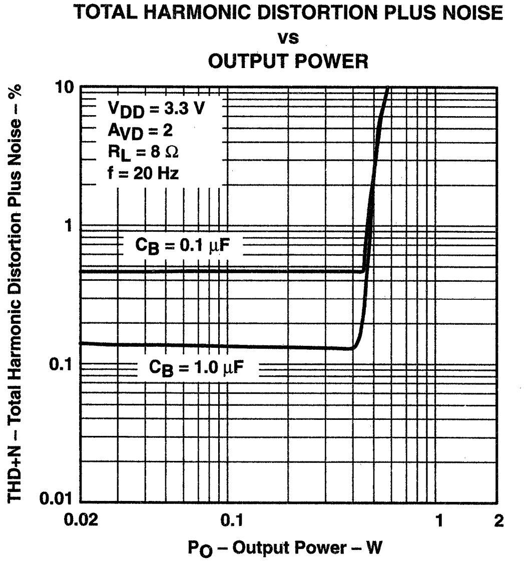

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 19

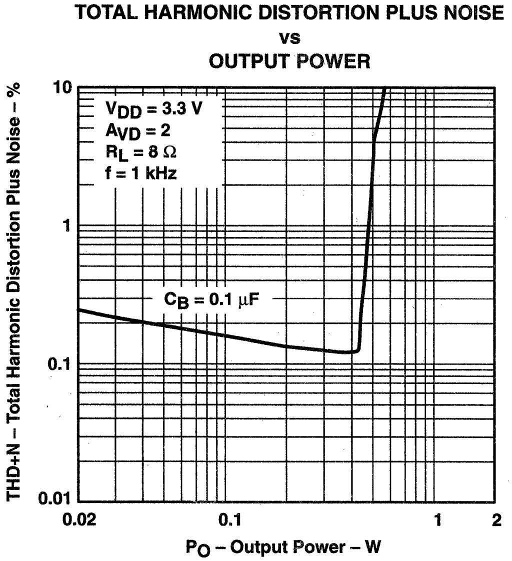

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

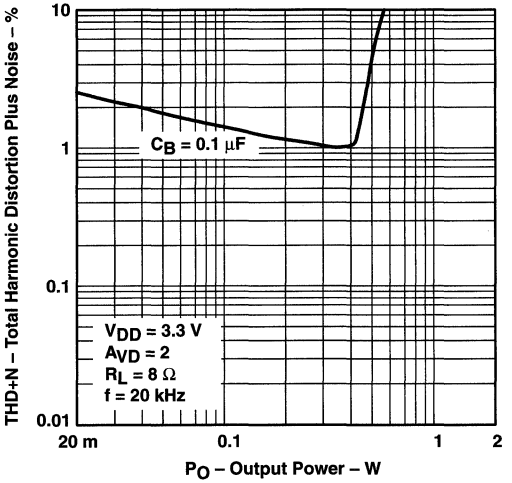


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

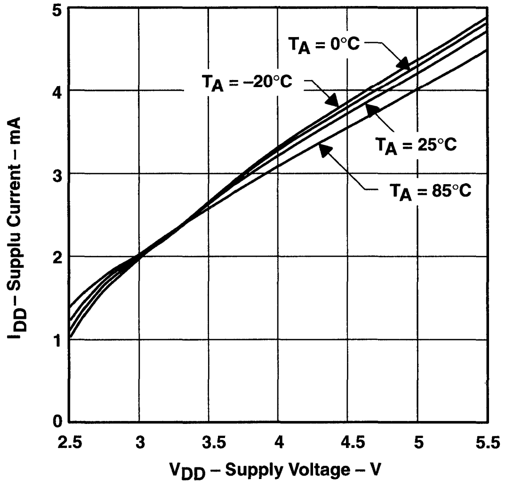


Figure 22

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

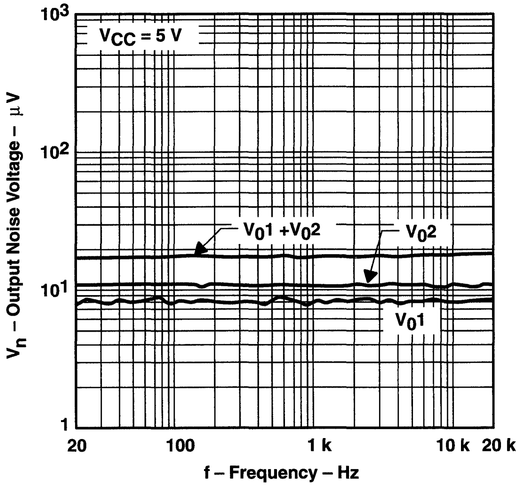


Figure 23

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

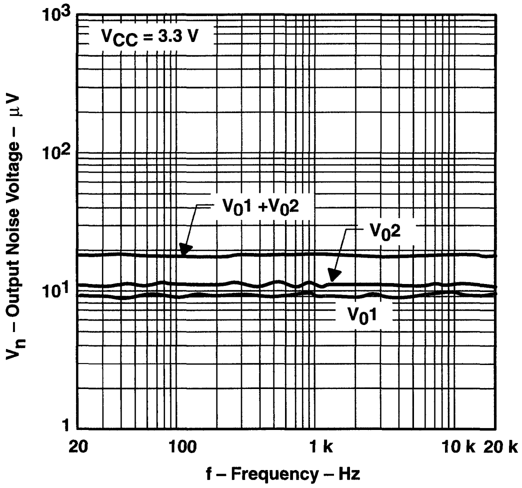


Figure 24

TYPICAL CHARACTERISTICS

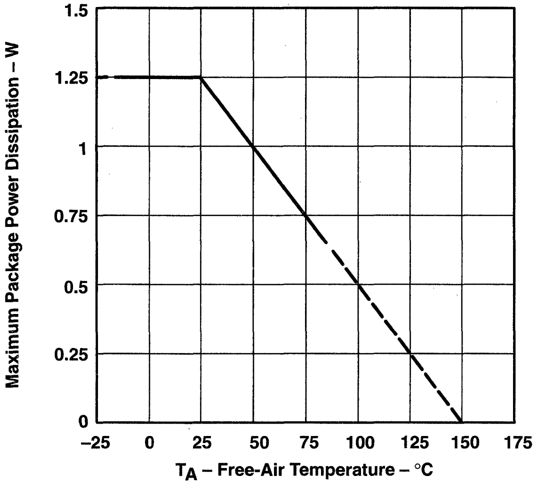

MAXIMUM PACKAGE POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

Figure 25

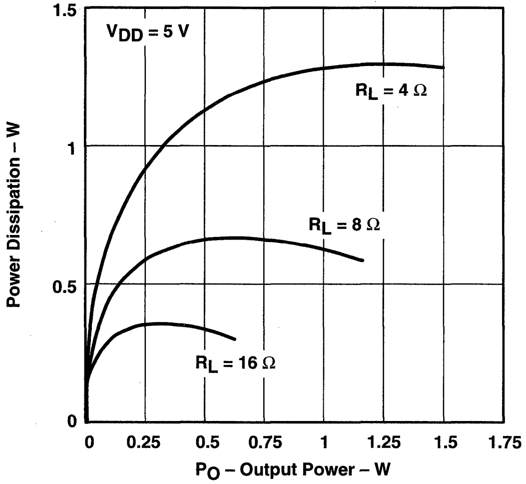

POWER DISSIPATION
vs
OUTPUT POWER

Figure 26

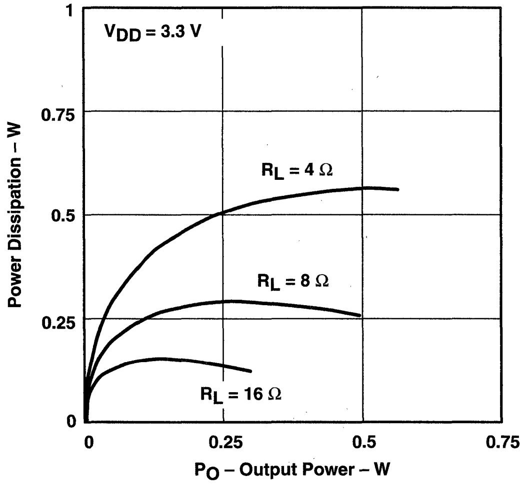

POWER DISSIPATION
vs
OUTPUT POWER

Figure 27

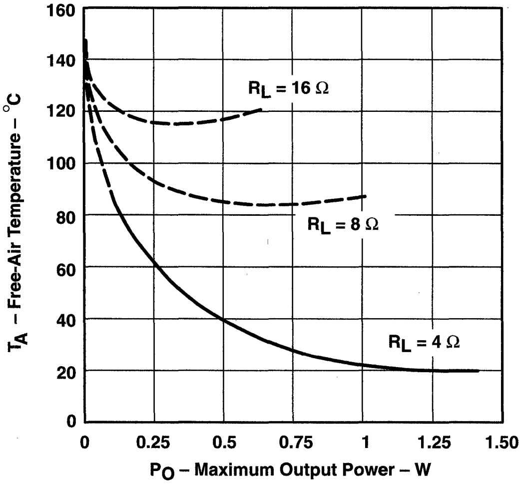

MAXIMUM OUTPUT POWER
vs
FREE-AIR TEMPERATURE

Figure 28

TYPICAL CHARACTERISTICS

OUTPUT POWER vs LOAD RESISTANCE

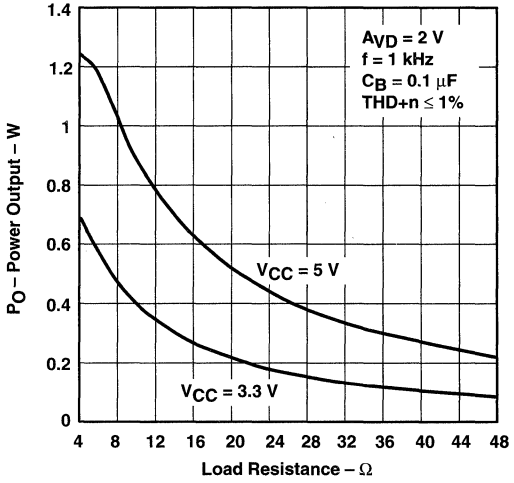


Figure 29

OUTPUT POWER vs SUPPLY VOLTAGE

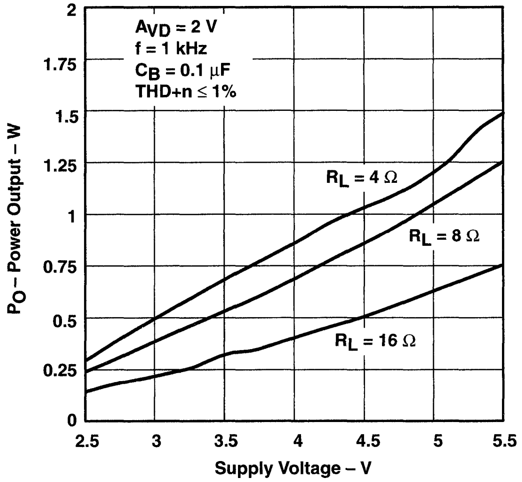


Figure 30

OPEN LOOP FREQUENCY RESPONSE

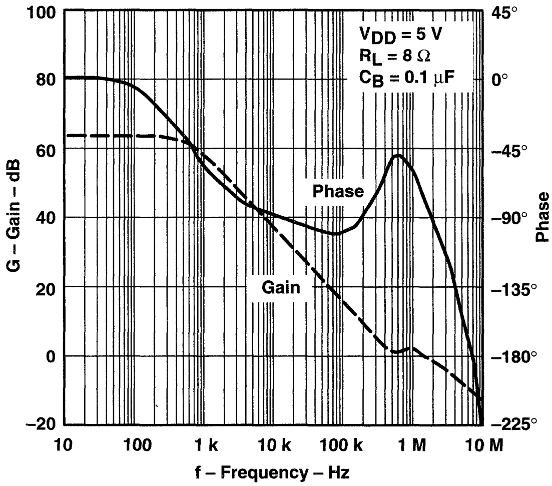


Figure 31

POWER SUPPLY REJECTION RATIO vs FREQUENCY

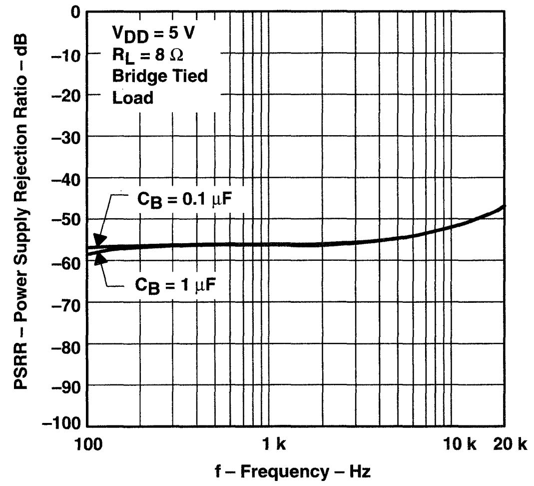


Figure 32

TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

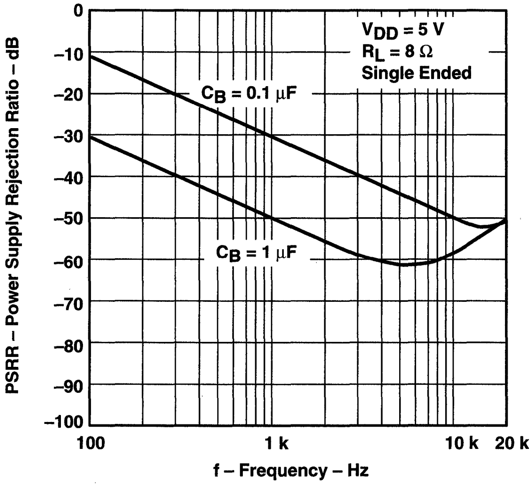


Figure 33

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 34 shows a linear audio power amplifier (APA) in a bridge tied load (BTL) configuration. A BTL amplifier actually consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially let us consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging twice the voltage into the power equation, where voltage is squared, yields 4 times the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^{2}}{R_L} \qquad (1)$$

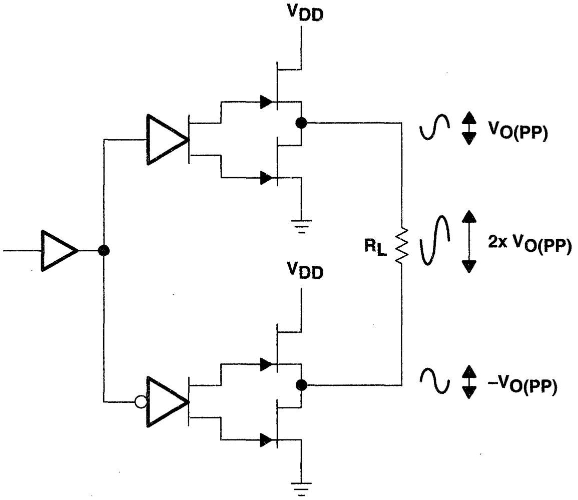


Figure 34. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into a 8-Ω speaker from a singled-ended (SE) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns, consider the single-supply SE configuration shown in Figure 35. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 40 µF to 1000 µF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

APPLICATION INFORMATION

$$f_{(corner)} = \frac{1}{2\pi R_L C_C} \qquad (2)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

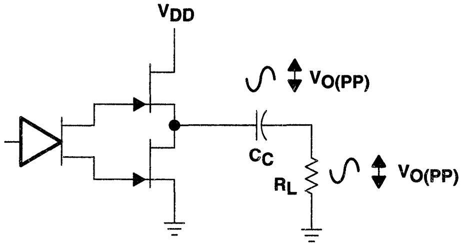


Figure 35. Single-Ended Configuration

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4 times the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy to use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 36).

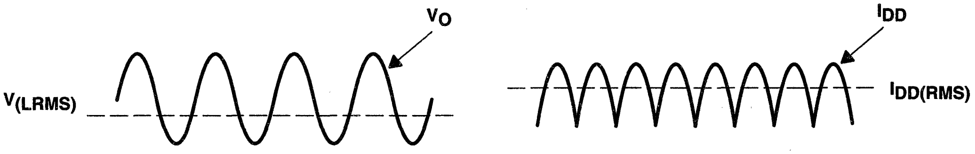


Figure 36. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistor are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

APPLICATION INFORMATION

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

where:

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_P{}^2}{2R_L}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\begin{array}{c}\text{Effiency of a}\\ \text{BTL Configuration}\end{array} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi\left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak-to-Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about linear amplifiers whether they are SE or BTL configured is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

For example, if the 5-V supply is replaced with a 10-V supply (TPA4860 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1 then efficiency at 1 W would fall to 31% and internal power dissipation would rise to 2.18 W from 0.59 W at 5 V. Then for a stereo 1-W system from a 10-V supply, the maximum draw would be almost 6.5 W. Choose the correct supply voltage and speaker impedance for the application.

APPLICATION INFORMATION

selection of components

Figure 37 is a schematic diagram of a typical notebook computer application circuit.

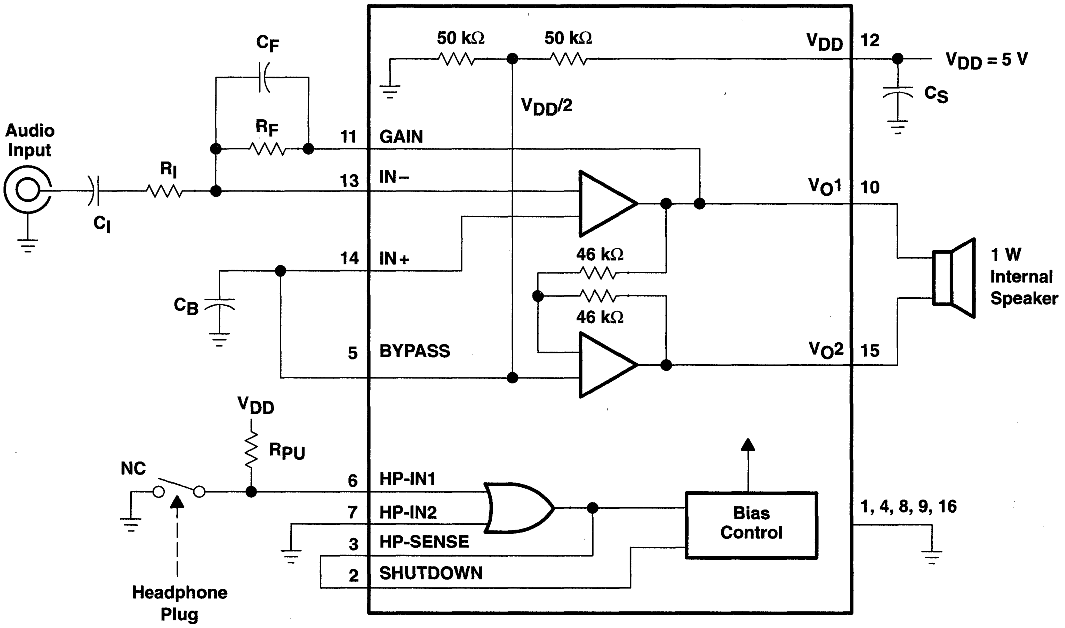


Figure 37. TPA4860 Typical Notebook Computer Application Circuit

gain setting resistors, R_F and R_I

The gain for the TPA4860 is set by resistors R_F and R_I according to equation 5.

$$\text{Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA4860 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\begin{array}{c}\text{Effective}\\\text{Impedance}\end{array} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

APPLICATION INFORMATION

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{7}$$

For example, if R_F is 100 kΩ and Cf is 5 pF then f_{co} is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \tag{8}$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_{co}} \tag{9}$$

In this example, C_I is 0.40 µF so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA4860 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

APPLICATION INFORMATION

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained.

$$\frac{1}{\left(C_B \times 25k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \tag{10}$$

As an example, consider a circuit where C_B is 0.1 µF, C_I is 0.22 µF and R_I is 10 kΩ. Inserting these values into the equation 9 we get:

$$400 \le 454$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

single-ended operation

Figure 38 is a schematic diagram of the recommended SE configuration. In SE mode configurations, the load should be driven from the primary amplifier output (OUT1, terminal 10).

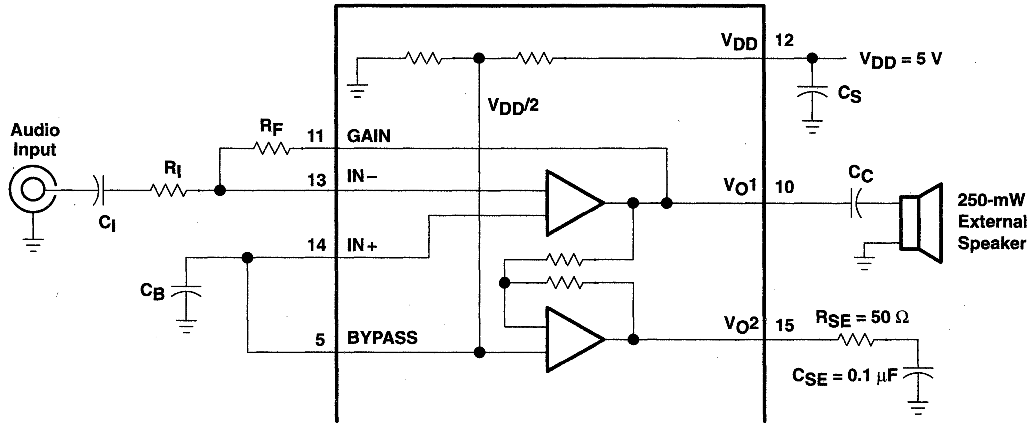


Figure 38. Singled-Ended Mode

Gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2 is not included.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

The phase margin of the inverting amplifier into an open circuit is not adequate to ensure stability, so a termination load should be connected to V_O2. This consists of a 50-Ω resistor in series with a 0.1-µF capacitor to ground. It is important to avoid oscillation of the inverting output to minimize noise and power dissipation.

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The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{1}{\left(C_B \times 25k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \qquad (12)$$

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.

$$f_{\text{out high}} = \frac{1}{2\pi R_L C_C} \qquad (13)$$

The main disadvantage, from a performance standpoint, is that the load impedances are typically small, which drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 8 Ω, 32 Ω, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
8 Ω	68 µF	293 Hz
32 Ω	68 µF	73 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 2 indicates, most of the bass response is attenuated into 8-Ω loads while headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

headphone sense circuitry, R_{pu}

The TPA4860 is commonly used in systems where there is an internal speaker and a jack for driving external loads (i.e., headphones). In these applications, it is usually desirable to mute the internal speaker(s) when the external load is in use. The headphone inputs (HP-1, HP-2) and headphone output (HP-SENSE) of the TPA4860 were specifically designed for this purpose. Many standard headphone jacks are available with an internal single-pole single-throw (SPST) switch that makes or breaks a circuit when the headphone plug is inserted. Asserting either or both HP-1 and/or HP-2 high mutes the output stage of the amplifier and causes HP-SENSE to go high. In battery-powered applications where power conservation is critical HP-SENSE can be connected to the shutdown input as shown in Figure 39. This places the amplifier in a very low current state for maximum power savings. Pullup resistors in the range from 1 kΩ to 10 kΩ are recommended for 5-V and 3.3-V operation.

APPLICATION INFORMATION

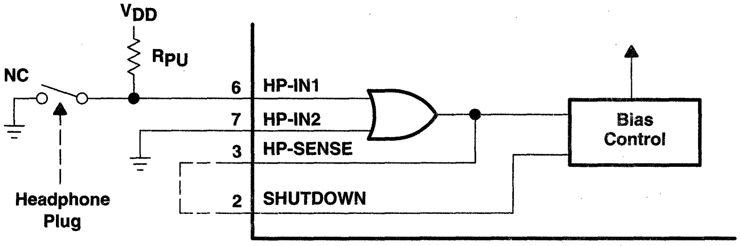


Figure 39. Schematic Diagram of Typical Headphone Sense Application

Table 3 details the logic for the mute function of the TPA4860.

Table 3. Truth table for Headphone Sense and Shutdown Functions

INPUTS†			OUTPUT	AMPLIFIER STATE
HP-1	HP-2	SHUTDOWN	HP-SENSE	
Low	Low	Low	Low	Active
Low	High	Low	High	Mute
High	Low	Low	High	Mute
High	High	Low	High	Mute
X	X	High	X	Shutdown

† Inputs should never be left unconnected.
X = do not care

shutdown mode

The TPA4860 employs a shutdown mode of operation designed to reduce quiescent supply current, $I_{DD(q)}$, to the absolute minimum level during periods of nonuse for battery-power conservation. For example, during device sleep modes or when other audio-drive currents are used (i.e., headphone mode), the speaker drive is not required. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD(q)} < 1\ \mu A$. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

thermal considerations

A prime consideration when designing an audio amplifier circuit is internal power dissipation in the device. The curve in Figure 40 provides an easy way to determine what output power can be expected out of the TPA4860 for a given system ambient temperature in designs using 5-V supplies. This curve assumes no forced airflow or additional heat sinking.

APPLICATION INFORMATION

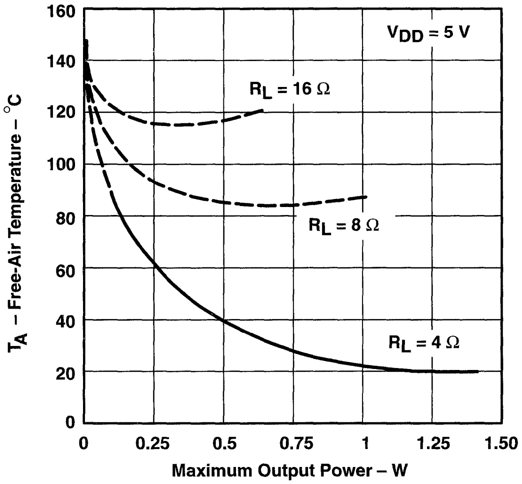


Figure 40. Free-Air Temperature Versus Maximum Continuous Output Power

5-V versus 3.3-V operation

The TPA4860 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in TPA4860 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load to less than 0.33 W before distortion begins to become significant.

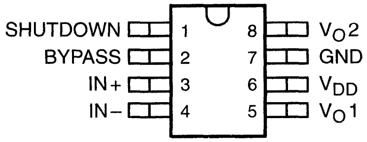
Operation at 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications.

TPA4861, TPA4861Y
1-WATT AUDIO POWER AMPLIFIER

SLOS163 – SEPTEMBER 1996

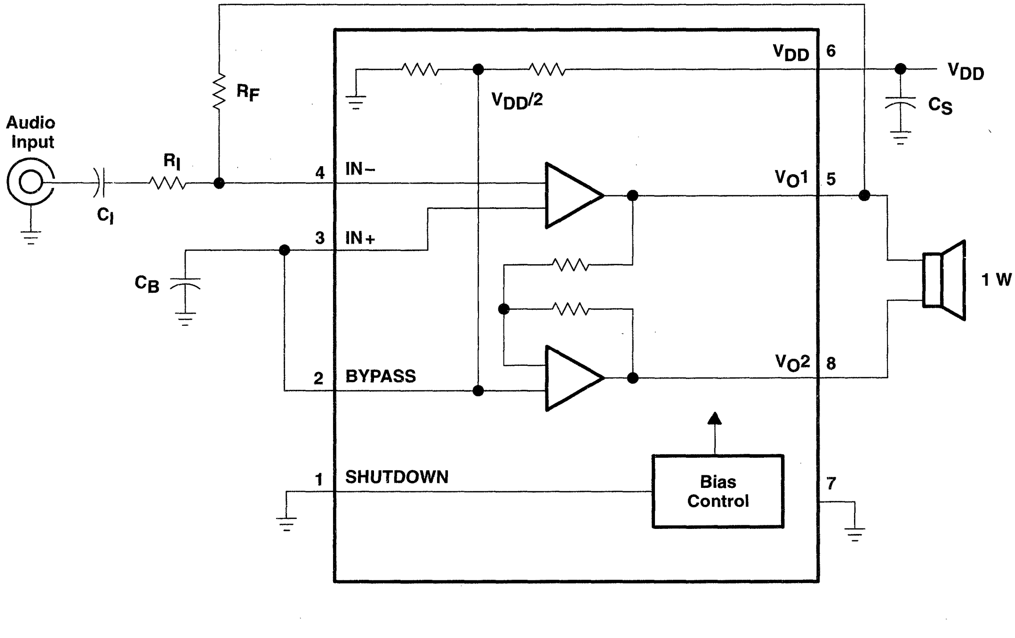
- **1-W BTL Output (5 V, 0.2 % THD+N)**
- **3.3-V and 5-V Operation**
- **No Output Coupling Capacitors Required**
- **Shutdown Control (I_{DD} = 0.6 μA)**
- **Uncompensated Gains of 2 to 20 (BTL Mode)**
- **Surface Mount Packaging**
- **Thermal and Short-Circuit Protection**
- **High Power Supply Rejection (56 dB at 1 kHz)**
- **LM4861 Drop-In Compatible**

D PACKAGE
(TOP VIEW)



description

The TPA4861 is a bridge-tied load (BTL) audio power amplifier capable of delivering 1 W of continuous average power into an 8-Ω load at 0.4 % THD+N from a 5-V power supply in voiceband frequencies (f < 5 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output in most applications. Gain is externally configured by means of two resistors and does not require compensation for settings of 2 to 20. Features of the amplifier are a shutdown function for power-sensitive applications as well as internal thermal and short-circuit protection. The TPA4861 works seamlessly with TI's TPA4860 in stereo applications. The amplifier is available in an 8-pin SOIC surface-mount package that reduces board space and facilitates automated assembly.



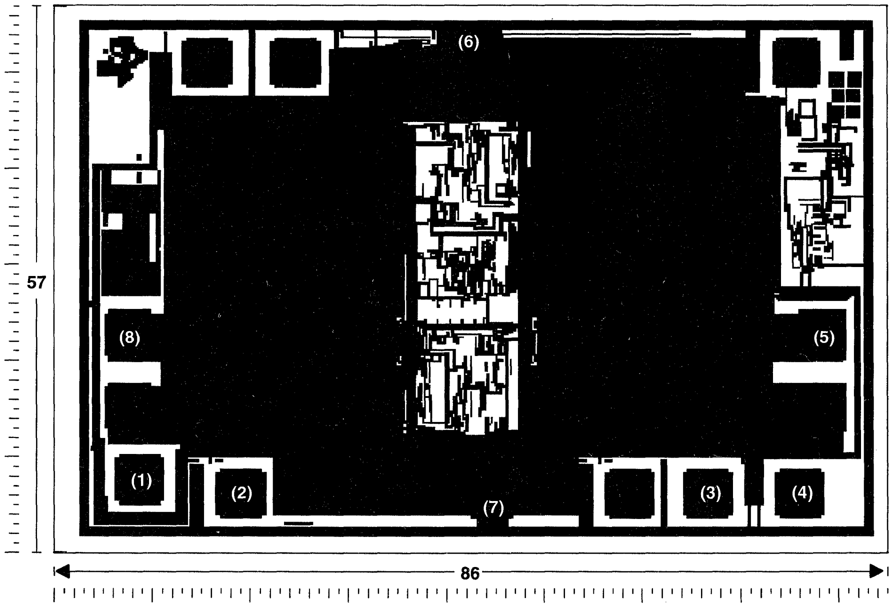
AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	CHIP FORM
	SMALL OUTLINE (D)	
−20°C to 85°C	TPA4861D	TPA4861Y

TPA4861Y chip information

This chip, when properly assembled, displays characteristics similar to the TPA4861C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINAL (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD}	6 V
Input voltage, V_I	–0.3 V to V_{DD} +0.3 V
Continuous total power dissipation	internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A	–20°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
D	731 mW	5.8 mW/°C	470 mW	383 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2.7	5.5	V
Common-mode input voltage, V_{IC}	$V_{CC} = 3$ V	1.25	2.7	V
	$V_{CC} = 5$ V	1.25	4.5	V
Operating free-air temperature, T_A		–20	85	°C

electrical characteristics at specified free-air temperature, V_{CC} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4861			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1		5	20	mV
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{OO}$)	V_{DD} = 3.2 V to 3.4 V		75		dB
$I_{DD(q)}$	Quiescent current			2.5		mA
$I_{DD(sd)}$	Quiescent current, shutdown mode			0.6		µA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4861			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, $A_V = 2$		350		mW
			THD = 2%, f = 1 kHz, $A_V = 2$		500		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 3		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

electrical characteristics at specified free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	TPA4861			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1		5	20	mV
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{OO}$)	V_{DD} = 4.9 V to 5.1 V		70		dB
$I_{DD(q)}$	Quiescent current			3.5		mA
$I_{DD(sd)}$	Quiescent current, shutdown mode			0.6		µA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristic, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4861			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = 2		1000		mW
			THD = 2%, f = 1 kHz, A_V = 2		1100		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 3		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

electrical characteristics at specified free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4861Y			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1		5		mV
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{OO}$)	V_{DD} = 4.9 V to 5.1 V		70		dB
$I_{DD(q)}$	Quiescent current			3.5		mA
$I_{DD(sd)}$	Quiescent current, shutdown mode			0.6		µA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristic, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4861Y			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = 2		1000		mW
			THD = 2%, f = 1 kHz, A_V = 2		1100		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 4		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output pins of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OO}	Output offset voltage	Distribution	1,2
I_{DD}	Supply current distribution	vs Free-air temperature	3,4
THD+N	Total harmonic distortion plus noise	vs Frequency	5,6,7,8,9, 10,11,15, 16,17,18
		vs Output power	12,13,14, 19,20,21
I_{DD}	Supply current	vs Supply voltage	22
V_n	Output noise voltage	vs Frequency	23,24
	Package power dissipation	vs Free-air temperature	25
	Power dissipation	vs Output power	26,27
	Maximum power output	vs Free-air temperature	28
	Output power	vs Load Resistance	29
		vs Supply Voltage	30
	Open loop frequency response	vs Frequency	31
	Power supply rejection ratio	vs Frequency	32,33

TYPICAL CHARACTERISTICS

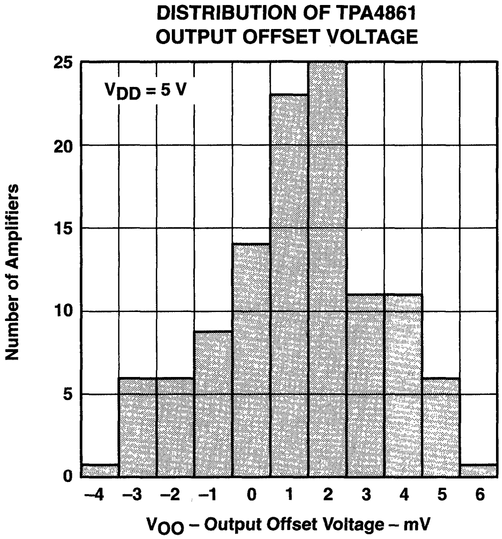


Figure 1

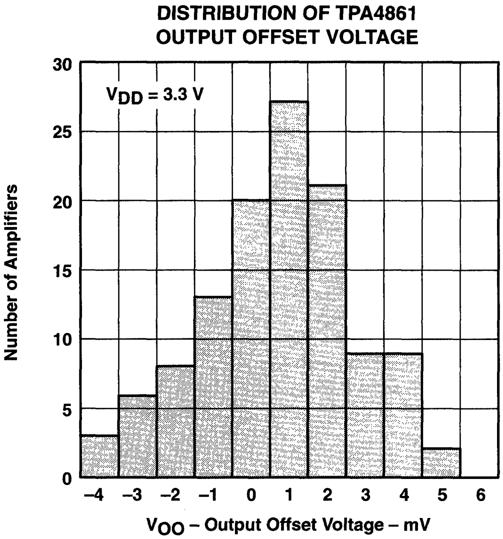


Figure 2

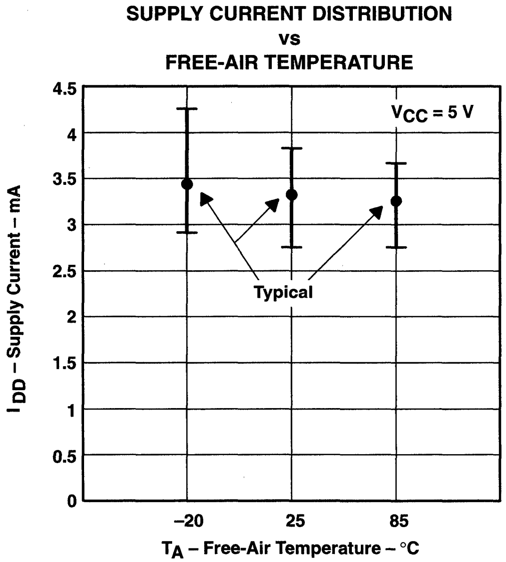


Figure 3

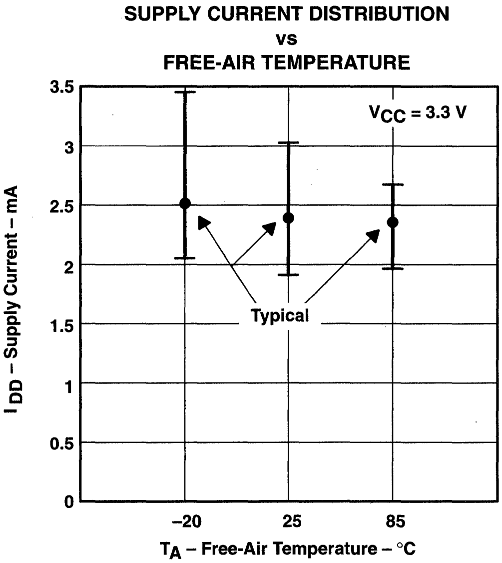


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

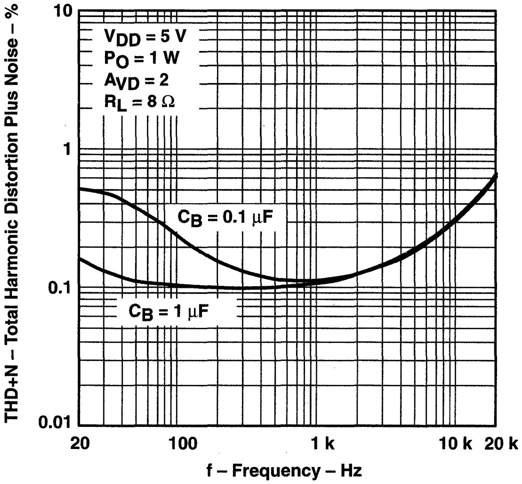


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

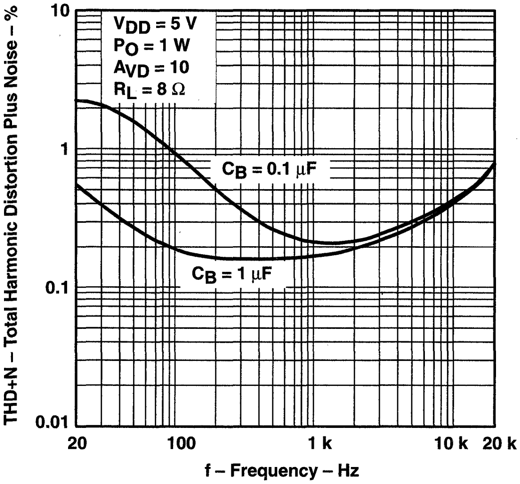


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

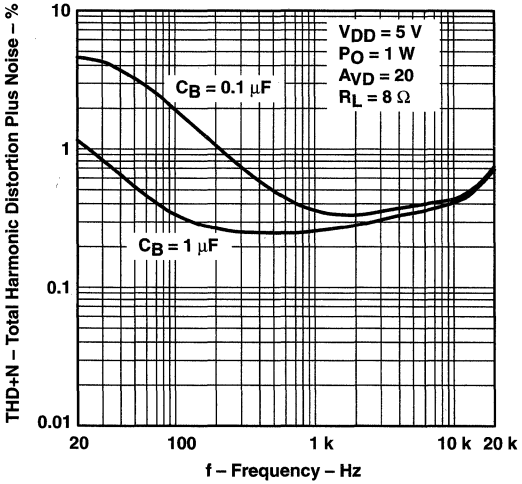


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

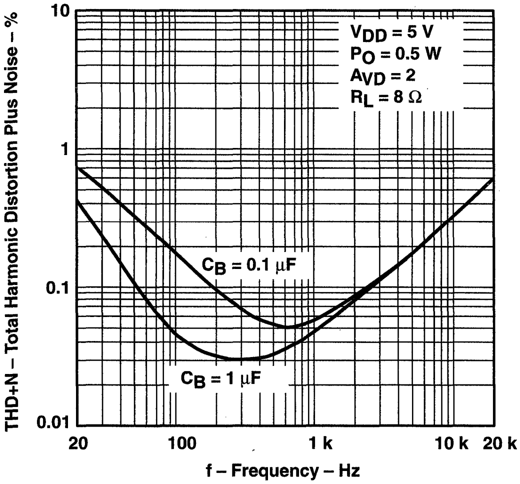


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

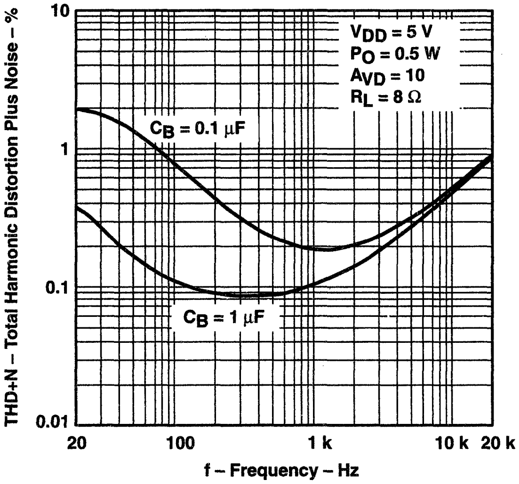


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

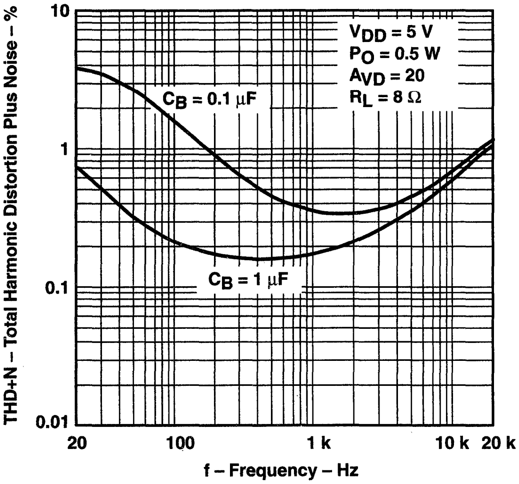


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

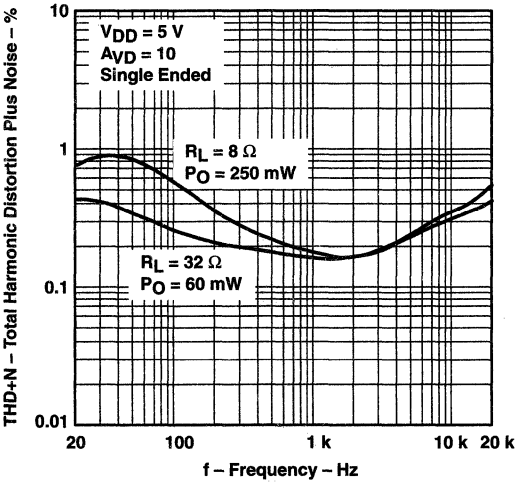


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

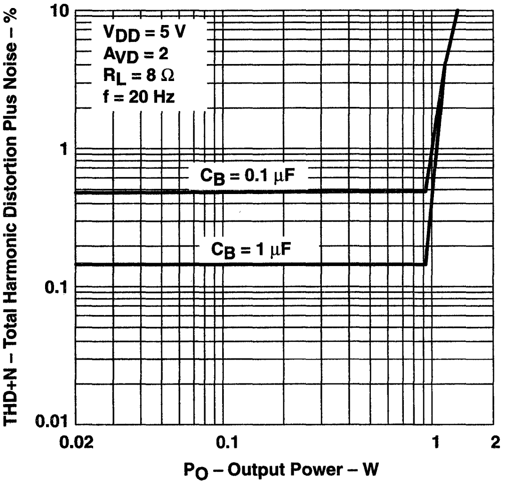


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

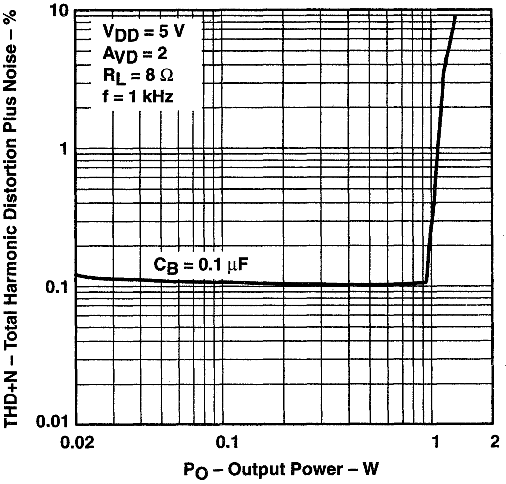


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

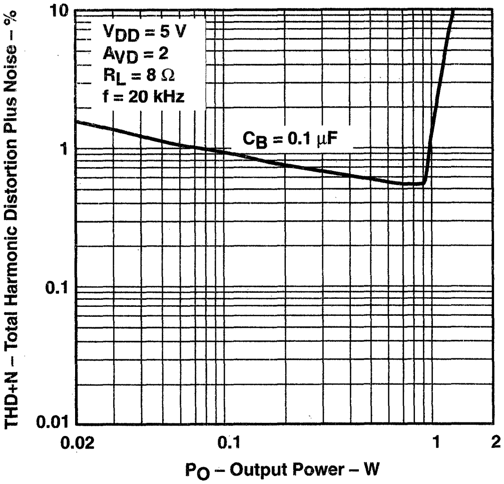


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

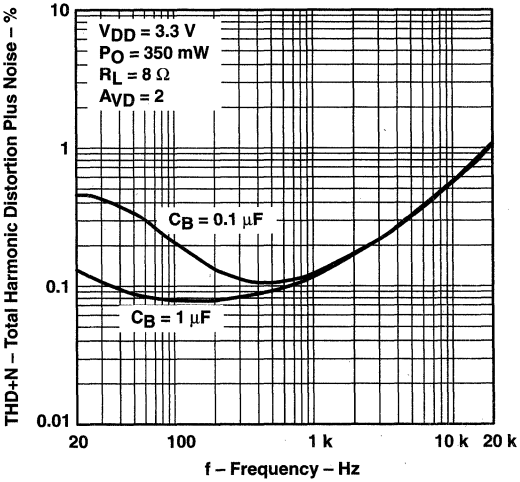


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

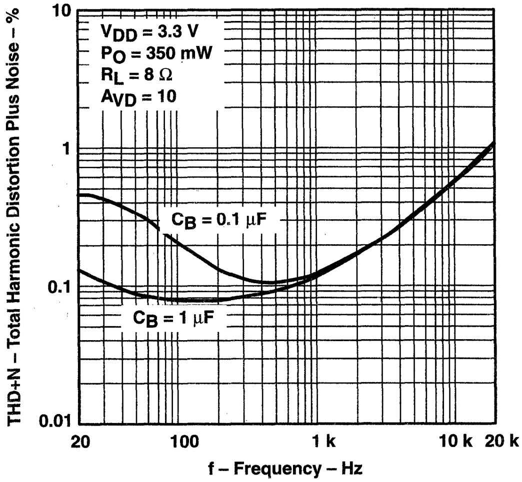


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

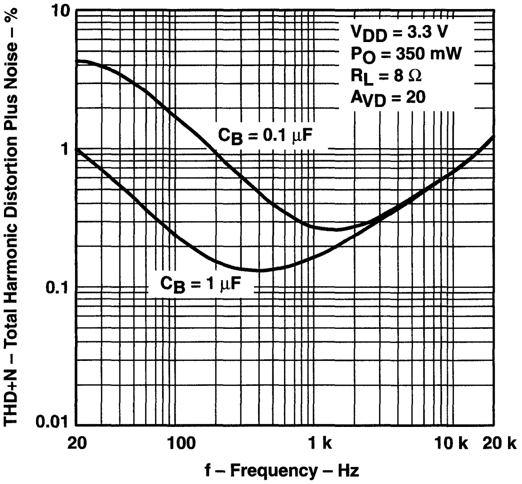


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

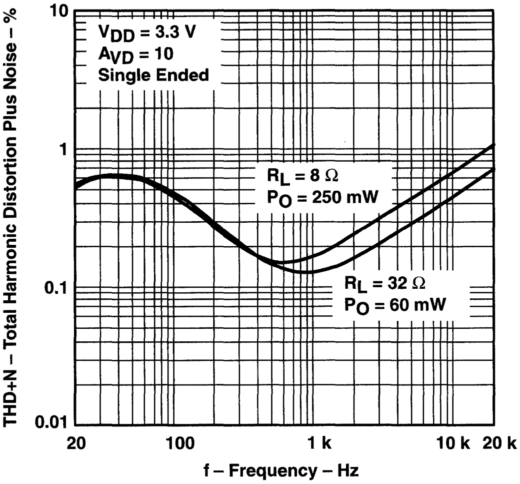


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

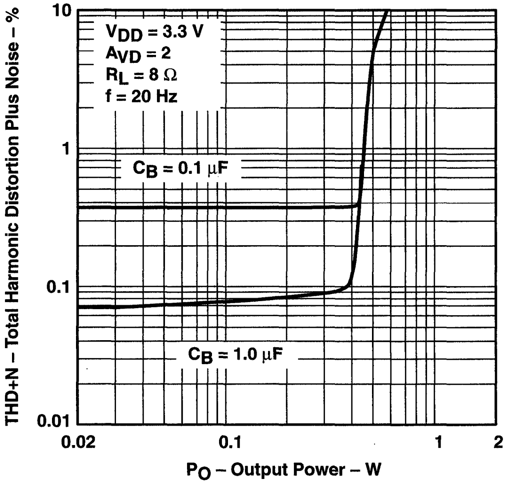


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

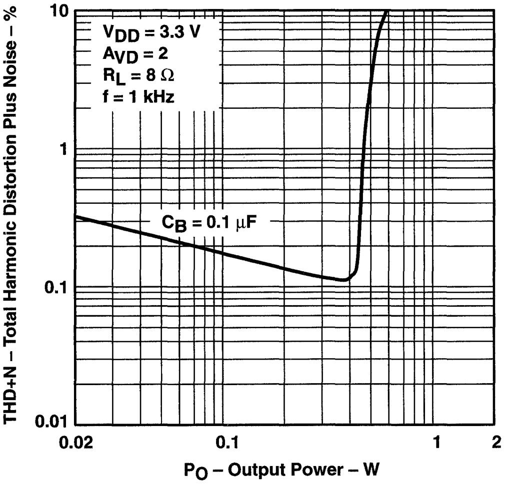


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

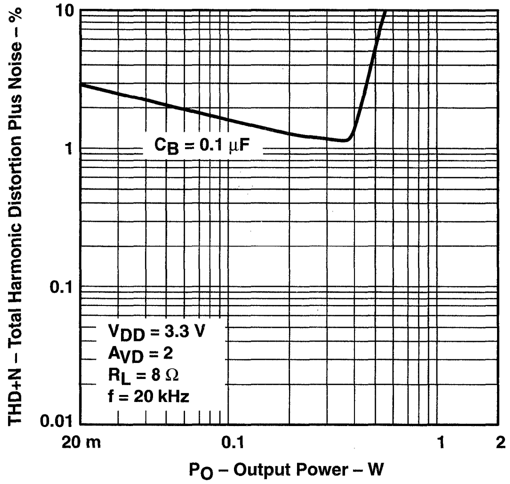


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

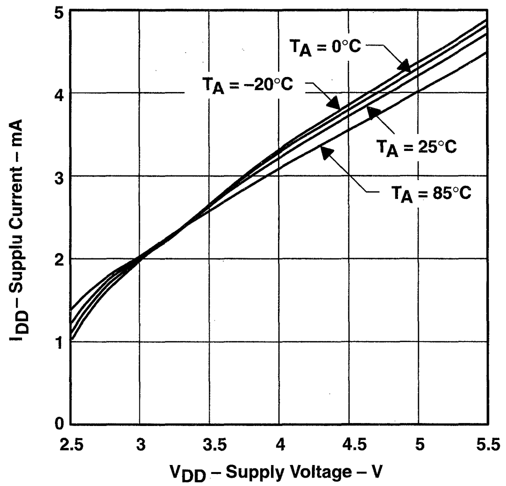


Figure 22

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

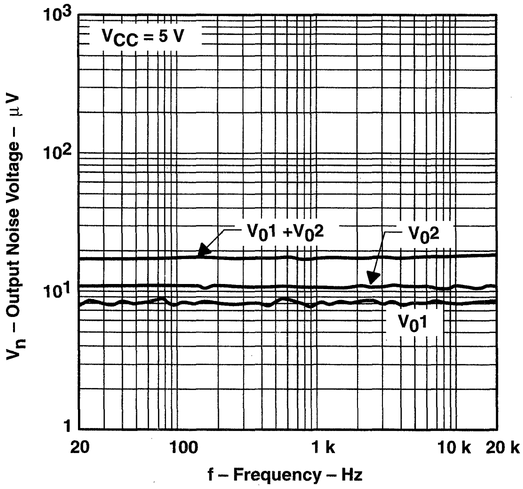


Figure 23

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

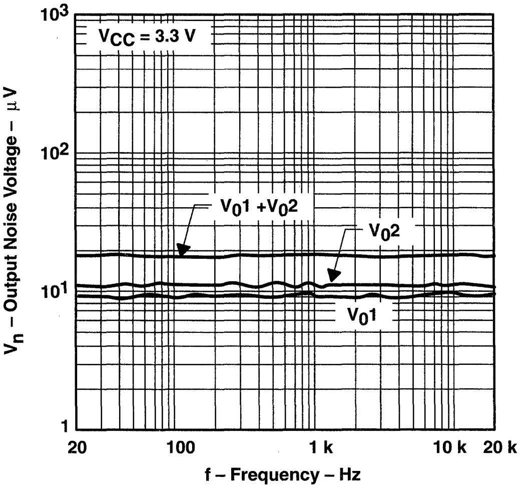


Figure 24

TYPICAL CHARACTERISTICS

MAXIMUM PACKAGE POWER DISSIPATION vs FREE-AIR TEMPERATURE

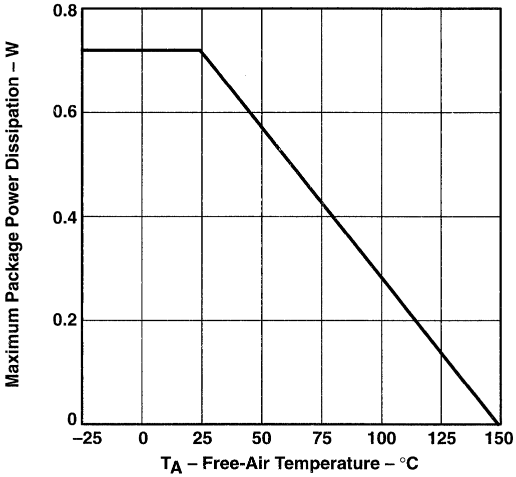


Figure 25

POWER DISSIPATION vs OUTPUT POWER

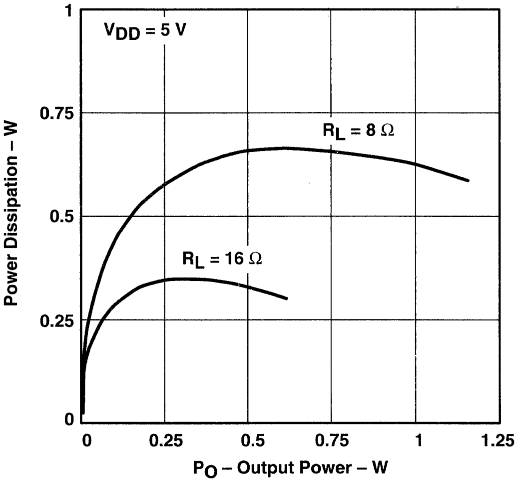


Figure 26

POWER DISSIPATION vs OUTPUT POWER

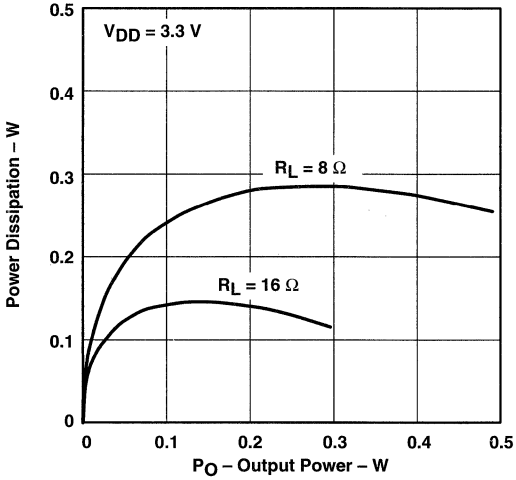


Figure 27

MAXIMUM OUTPUT POWER vs FREE-AIR TEMPERATURE

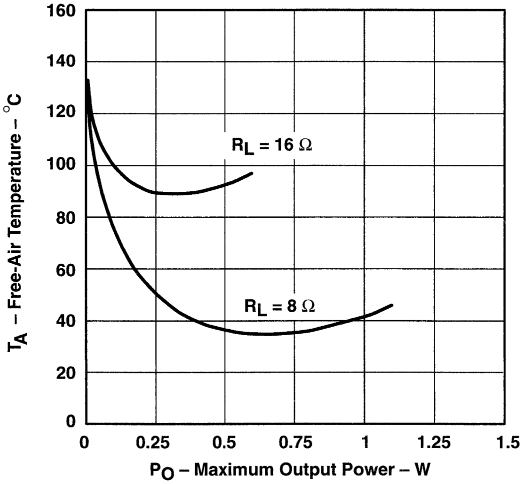


Figure 28

TYPICAL CHARACTERISTICS

OUTPUT POWER vs LOAD RESISTANCE

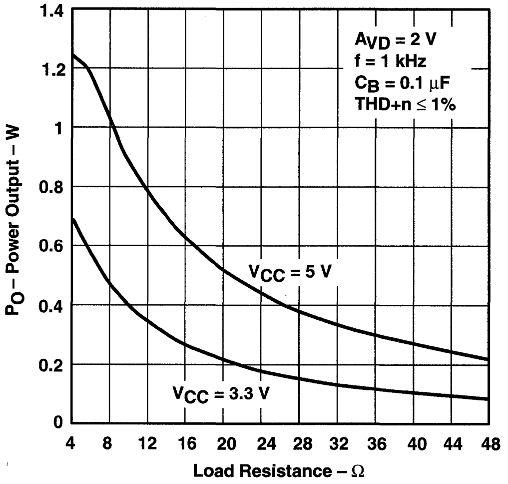


Figure 29

OUTPUT POWER vs SUPPLY VOLTAGE

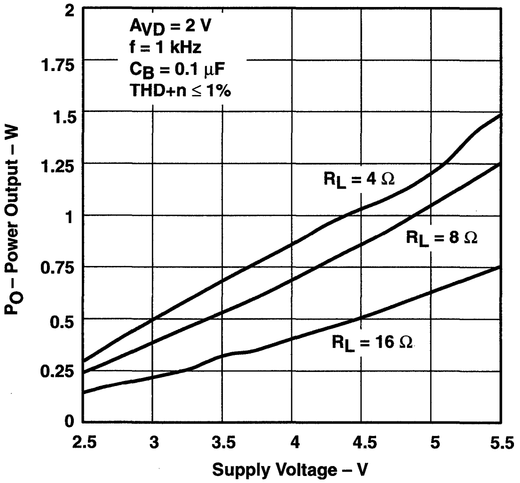


Figure 30

OPEN LOOP FREQUENCY RESPONSE

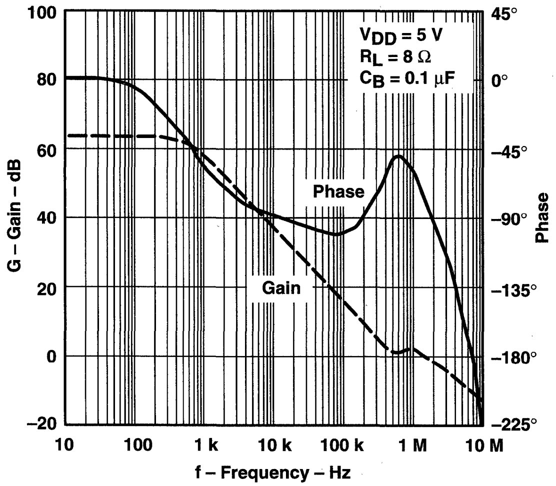


Figure 31

POWER SUPPLY REJECTION RATIO vs FREQUENCY

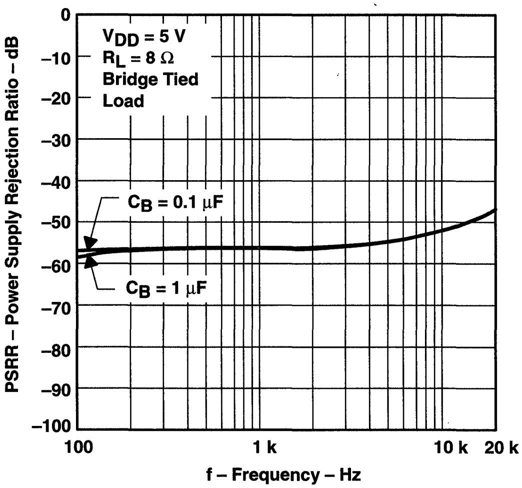


Figure 32

TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

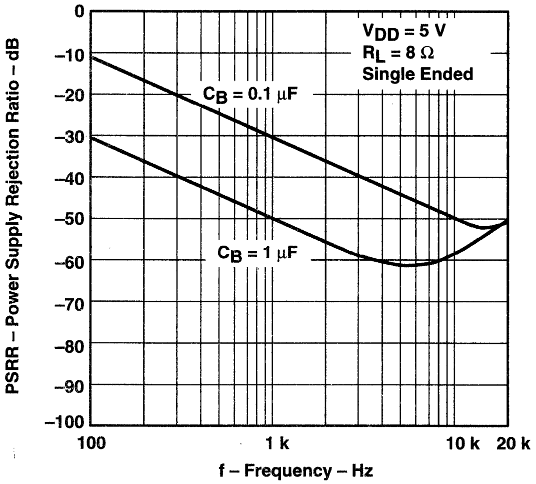


Figure 33

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 34 shows a linear audio power amplifier (APA) in a bridge tied load (BTL) configuration. A BTL amplifier actually consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially let us consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging twice the voltage into the power equation, where voltage is squared, yields 4 times the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^{2}}{R_L} \qquad (1)$$

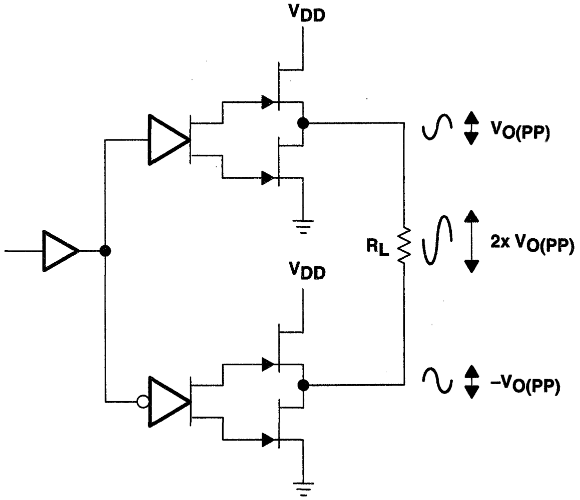


Figure 34. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into a 8-Ω speaker from a singled-ended (SE) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns, consider the single-supply SE configuration shown in Figure 35. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 40 µF to 1000 µF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

$$f_{(corner)} = \frac{1}{2\pi R_L C_C} \qquad (2)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

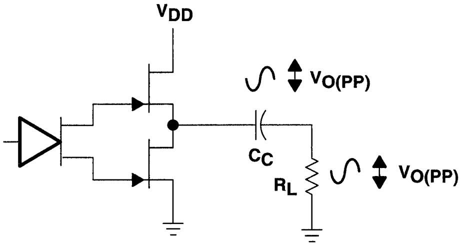


Figure 35. Single-Ended Configuration

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4 times the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, $I_{DD}rms$, determines the internal power dissipation of the amplifier.

An easy to use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 36).

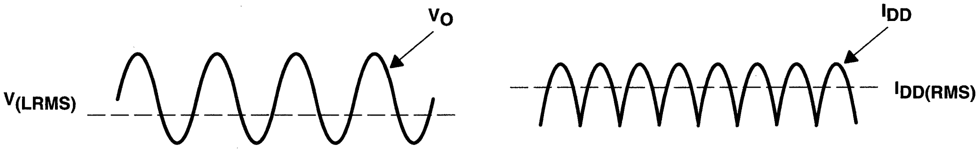


Figure 36. Voltage and Current Waveforms for BTL Amplifiers

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistor are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

where:

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_P{}^2}{2R_L}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\begin{array}{c}\text{Effiency of a}\\ \text{BTL Configuration}\end{array} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak-to-Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

APPLICATION INFORMATION

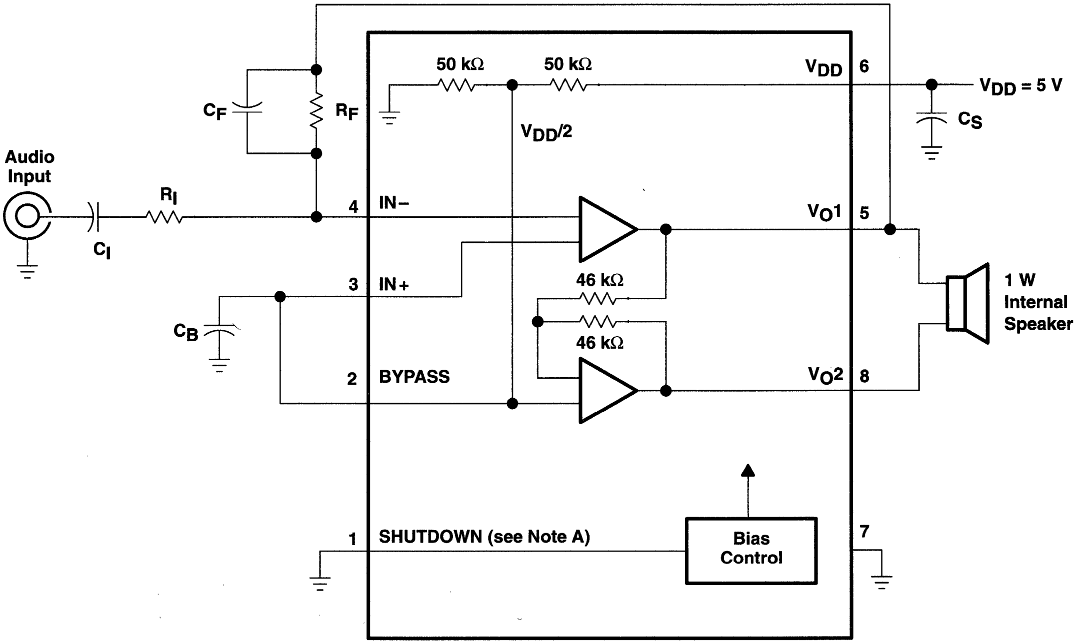
BTL amplifier efficiency (continued)

A final point to remember about linear amplifiers whether they are SE or BTL configured is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

For example, if the 5-V supply is replaced with a 10-V supply (TPA4861 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1 then efficiency at 1 W would fall to 31% and internal power dissipation would rise to 2.18 W from 0.59 W at 5 V. Then for a stereo 1-W system from a 10-V supply, the maximum draw would be almost 6.5 W. Choose the correct supply voltage and speaker impedance for the application.

selection of components

Figure 37 is a schematic diagram of a typical notebook computer application circuit.



NOTE A: SHUTDOWN must be held low for normal operation and asserted high for shutdown mode.

Figure 37. TPA4861 Typical Notebook Computer Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA4861 is set by resistors R_F and R_I according to equation 5.

$$\text{Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA4861 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\begin{matrix}\text{Effective}\\ \text{Impedance}\end{matrix} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{7}$$

For example if R_F is 100 kΩ and Cf is 5 pF then f_{co} is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \tag{8}$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_{co}} \tag{9}$$

In this example, C_I is 0.40 µF so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA4861 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained.

$$\frac{1}{\left(C_B \times 25k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \tag{10}$$

As an example, consider a circuit where C_B is 0.1 µF, C_I is 0.22 µF and R_I is 10 kΩ. Inserting these values into the equation 9 we get:

$$400 \le 454$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

APPLICATION INFORMATION

single-ended operation

Figure 38 is a schematic diagram of the recommended SE configuration. In SE mode configurations, the load should be driven from the primary amplifier output (OUT1, terminal 10).

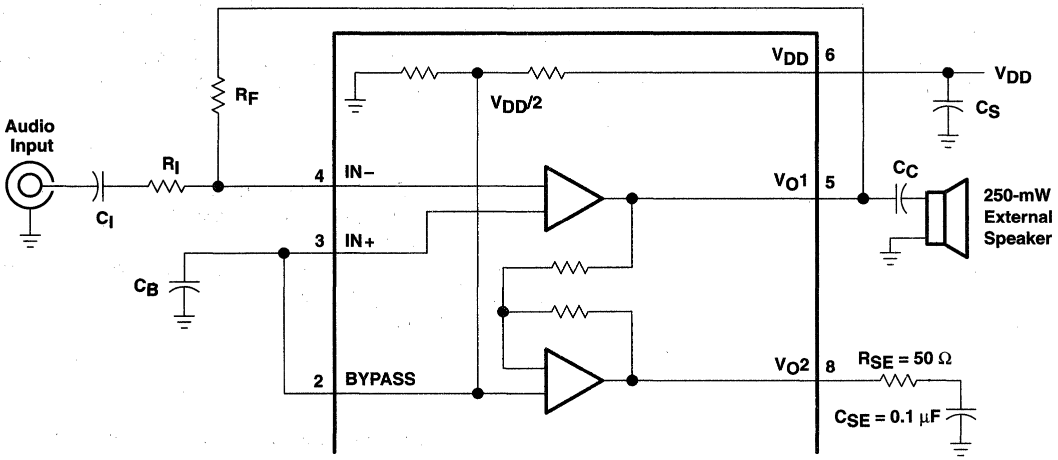


Figure 38. Singled-Ended Mode

Gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2 is not included.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

The phase margin of the inverting amplifier into an open circuit is not adequate to ensure stability, so a termination load should be connected to V_O2. This consists of a 50-Ω resistor in series with a 0.1-μF capacitor to ground. It is important to avoid oscillation of the inverting output to minimize noise and power dissipation.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{1}{\left(C_B \times 25k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \tag{12}$$

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.

$$f_{\text{out high}} = \frac{1}{2\pi R_L C_C} \tag{13}$$

The main disadvantage, from a performance standpoint, is that the load impedances are typically small, which drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 μF is chosen and loads vary from 8 Ω, 32 Ω, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
8 Ω	68 μF	293 Hz
32 Ω	68 μF	73 Hz
47,000 Ω	68 μF	0.05 Hz

As Table 2 indicates, most of the bass response is attenuated into 8-Ω loads while headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

shutdown mode

The TPA4861 employs a shutdown mode of operation designed to reduce quiescent supply current, $I_{DD(q)}$, to the absolute minimum level during periods of nonuse for battery-power conservation. For example, during device sleep modes or when other audio-drive currents are used (i.e., headphone mode), the speaker drive is not required. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD(q)} < 1$ μA. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

thermal considerations

A prime consideration when designing an audio amplifier circuit is internal power dissipation in the device. The curve in NO TAG provides an easy way to determine what output power can be expected out of the TPA4861 for a given system ambient temperature in designs using 5-V supplies. This curve assumes no forced airflow or additional heat sinking.

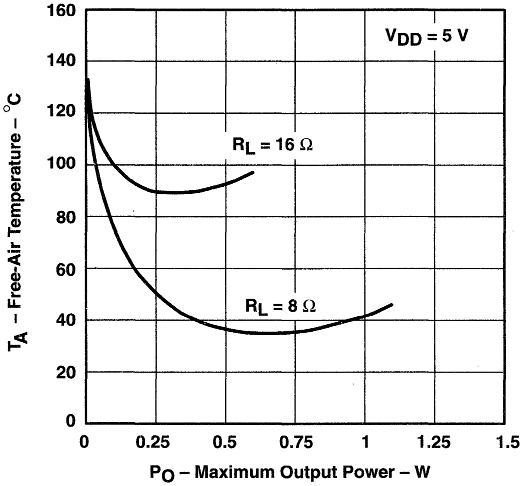


Figure 39. Free-Air Temperature Versus Maximum Continuous Output Power

5-V versus 3.3-V operation

The TPA4861 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in TPA4861 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load to less than 0.33 W before distortion begins to become significant.

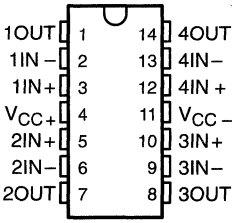
Operation at 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds of the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications.

LF347, LF347B
JFET-INPUT
QUAD OPERATIONAL AMPLIFIERS

SLOS013B – MARCH 1987 – REVISED AUGUST 1994

- **Low Input Bias Current . . . 50 pA Typ**
- **Low Input Noise Current**
  0.01 pA/$\sqrt{\text{Hz}}$ Typ
- **Low Total Harmonic Distortion**
- **Low Supply Current . . . 8 mA Typ**
- **Gain Bandwidth . . . 3 MHz Typ**
- **High Slew Rate . . . 13 V/μs Typ**
- **Pin Compatible With the LM348**

D OR N PACKAGE
(TOP VIEW)



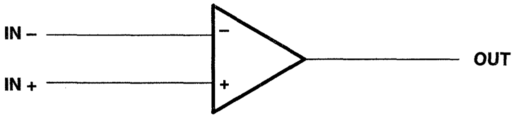
description

These devices are low-cost, high-speed, JFET-input operational amplifiers. They require low supply current yet maintain a large gain-bandwidth product and a fast slew rate. In addition, their matched high-voltage JFET inputs provide very low input bias and offset current.

The LF347 and LF347B can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF347 and LF347B are characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	10 mV	LF347D	LF347N
	5 mV	LF347BD	LF347BN

The D packages are available taped and reeled. Add R suffix to the device type (e.g., LF347DR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID}	±30 V
Input voltage, V_I (see Note 1)	±15 V
Duration of output short circuit	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	608 mW	7.6 mW/°C	61°C	608 mW
N	680 mW	N/A	N/A	680 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A†	LF347			LF347B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ	25°C		5	10		3	5	mV
			Full range			13			7	
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ			18			18		μV/°C
I_{IO}	Input offset current‡	$V_{IC} = 0$	25°C		25	100		25	100	pA
			70°C			4			4	nA
I_{IB}	Input bias current‡	$V_{IC} = 0$	25°C		50	200		50	200	pA
			70°C			8			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	±13.5		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ kΩ	25°C	25	100		50	100		V/mV
			Full range	15			25			
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2$ kΩ		70	100		80	100		dB
k_{SVR}	Supply-voltage rejection ratio	See Note 2		70	100		80	100		dB
I_{CC}	Supply current				8	11		8	11	mA

† Full range is 0°C to 70°C.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

NOTE 2: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

operating characteristics, $V_{CC\pm} = \pm 15$ V

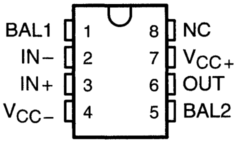
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attentuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 20\ \Omega$		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

LF351
JFET-INPUT
OPERATIONAL AMPLIFIER

SLOS014B – MARCH 1987 – REVISED AUGUST 1994

- **Low Input Bias Current . . . 50 pA Typ**
- **Low Input Noise Voltage . . . 18 nV/√Hz Typ**
- **Low Input Noise Current**
  0.01 pA/√Hz Typ
- **Low Supply Current . . . 1.8 mA Typ**
- **High Input impedance . . . 10^{12} Ω Typ**
- **Low Total Harmonic Distortion**
- **Internally Trimmed Offset Voltage**
  10 mV Typ
- **High Slew Rate . . . 13 V/μs Typ**
- **Gain Bandwidth . . . 3 MHz**
- **Pin Compatible With Standard 741**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

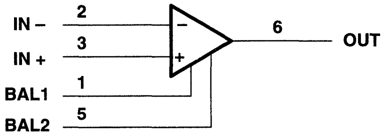
description

This device is a low-cost, high-speed, JFET-input operational amplifier with an internally trimmed input offset voltage. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents. It uses the same offset voltage adjustment circuits as the 741.

The LF351 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF351 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	10 mV	LF351D	LF351P

The D packages are available taped and reeled. Add the suffix R to the device type (i.e., LF351DR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID}	±30 V
Input voltage, V_I (see Note 1)	±15 V
Duration of output short circuit	unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ	25°C		5	10	mV
			Full range			13	
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ			10		µV/°C
I_{IO}	Input offset current‡	V_{IC} = 0	25°C		25	100	pA
			70°C			4	nA
I_{IB}	Input bias current‡	V_{IC} = 0	25°C		50	200	pA
			70°C			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	25°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	T_J = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq$ 10 kΩ		70	100		dB
k_{SVR}	Supply-voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				1.8	3.4	mA

† Full range is 0°C to 70°C.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
NOTE 2: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

operating characteristics, $V_{CC\pm}$ = ±15 V

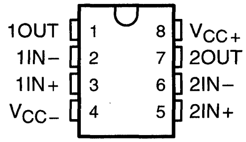
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/µs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

LF353
JFET-INPUT
DUAL OPERATIONAL AMPLIFIER

SLOS012B – MARCH 1987 – REVISED AUGUST 1994

- **Low Input Bias Current . . . 50 pA Typ**
- **Low Input Noise Current**
  0.01 pA/√Hz Typ
- **Low Input Noise Voltage . . . 18 nV/√Hz Typ**
- **Low Supply Current . . . 3.6 mA Typ**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Internally Trimmed Offset Voltage**
- **Gain Bandwidth . . . 3 MHz Typ**
- **High Slew Rate . . . 13 V/μs Typ**

D OR P PACKAGE
(TOP VIEW)



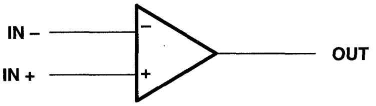
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF353 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF353 is characterized for operation from 0°C to 70°C.

symbol (each amplifier



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	10 mV	LF353D	LF353P

The D packages are available taped and reeled. Add the suffix R to the device type (ie., LF353DR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	–18 V
Differential input voltage, V_{ID}	±30 V
Input voltage, V_I (see Note 1)	±15 V
Duration of output short circuit	unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ	25°C		5	10	mV
			Full range			13	
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ			10		μV/°C
I_{IO}	Input offset current‡	$V_{IC} = 0$	25°C		25	100	pA
			70°C			4	nA
I_{IB}	Input bias current‡	$V_{IC} = 0$	25°C		50	200	pA
			70°C			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ kΩ	25°C	25	100		V/mV
			Full range	15			
r_i	Input resistance	$T_J = 25$°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \le 10$ kΩ		70	100		dB
k_{SVR}	Supply-voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				3.6	6.5	mA

† Full range is 0°C to 70°C.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

NOTE 2: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25$°C

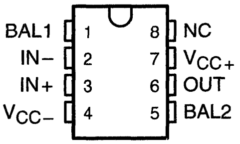
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attentuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 20$ Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

LF411C
JFET-INPUT OPERATIONAL AMPLIFIER

SLOS011B – MARCH 1987 – REVISED AUGUST 1994

- **Low Input Bias Current . . . 50 pA Typ**
- **Low Input Noise Current**
  0.01 pA/√Hz Typ
- **Low Supply Current . . . 2 mA Typ**
- **High Input impedance . . . 10^{12} Ω Typ**
- **Low Total Harmonic Distortion**
- **Low 1/f Noise Corner . . . 50 Hz Typ**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

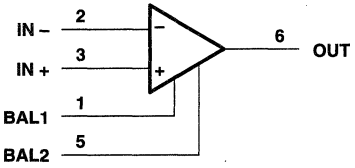
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a maximum input offset voltage drift. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF411C can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF411C is characterized for operation from 0°C to 70°C.

symbol



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	2 mV	LF411CD	LF411CP

The D packages are available taped and reeled. Add the suffix R to the device type (ie., LF411CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID}	±30 V
Input voltage, V_I (see Note 1)	±15 V
Duration of output short circuit	unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ	25°C		0.8	2	mV
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ			10	20‡	μV/°C
I_{IO}	Input offset current§	$V_{IC} = 0$	25°C		25	100	pA
			70°C			2	nA
I_{IB}	Input bias current§	$V_{IC} = 0$	25°C		50	200	pA
			70°C			4	nA
V_{ICR}	Common-mode input voltage range			±11	−11.5 to 14.5		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm10$ V, $R_L = 2$ kΩ	25°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	$T_J = 25°C$			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		70	100		dB
k_{SVR}	Supply-voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				2	3.4	mA

† Full range is 0°C to 70°C.

‡ At least 90% of the devices meet this limit for α_{VIO}.

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

NOTE 2: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

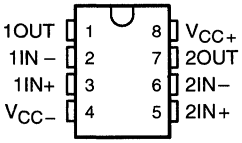
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 20$ Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

LF412C
DUAL JFET-INPUT OPERATIONAL AMPLIFIER

SLOS010B – MARCH 1987 – REVISED AUGUST 1994

- **Low Input Bias Current . . . 50 pA Typ**
- **Low Input Noise Current**
  0.01 pA/$\sqrt{Hz}$ Typ
- **Low Supply Current . . . 4.5 mA Typ**
- **High Input impedance . . . 10^{12} Ω Typ**
- **Internally Trimmed Offset Voltage**
- **Wide Gain Bandwidth . . . 3 MHz Typ**
- **High Slew Rate . . . 13 V/μs Typ**

D OR P PACKAGE
(TOP VIEW)



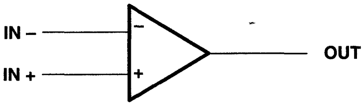
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a specified maximum input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF412C can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF412C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	3 mV	LF412CD	LF412CP

The D packages are available taped and reeled. Add the suffix R to the device type (ie., LF412CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	–18 V
Differential input voltage, V_{ID}	±30 V
Input voltage, V_I (see Note 1)	±15 V
Duration of output short circuit	unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ	25°C		1	3	mV
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ			10	20‡	μV/°C
I_{IO}	Input offset current§	$V_{IC} = 0$	25°C		25	100	pA
			70°C			4	nA
I_{IB}	Input bias current§	$V_{IC} = 0$	25°C		50	200	pA
			70°C			8	nA
V_{ICR}	Common-mode input voltage range			±11	−11.5 to 14.5		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ kΩ	25°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	$T_A = 25$°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		70	100		dB
k_{SVR}	Supply-voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				4.5	6.8	mA

† Full range is 0°C to 70°C.

‡ At least 90% of the devices meet this limit for α_{VIO}.

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

NOTE 2: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25$°C

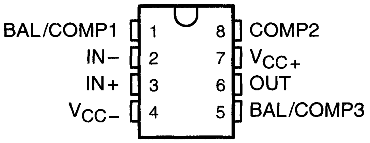
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 20\Omega$		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

LM118, LM218, LM318
FAST GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

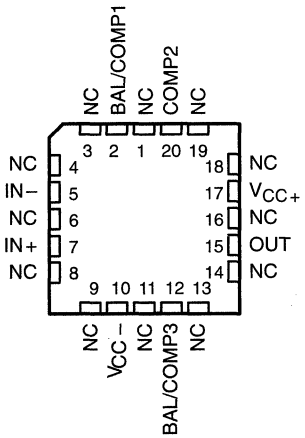
SLOS063A – JUNE 1976 – REVISED APRIL 1994

- **Small-Signal Bandwidth . . . 15 MHz Typ**
- **Slew Rate . . . 50 V/μs Min**
- **Bias Current . . . 250 nA Max (LM118, LM218)**
- **Supply Voltage Range . . . ±5 V to ±20 V**
- **Internal Frequency Compensation**
- **Input and Output Overload Protection**
- **Same Pin Assignments as General-Purpose Operational Amplifiers**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

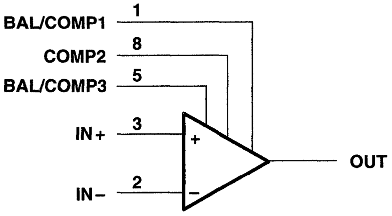
The LM118, LM218, and LM318 are precision, fast operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor-of-ten increase in speed over general-purpose devices without sacrificing dc performance.

These operational amplifiers have internal unity-gain frequency compensation. This considerably simplifies their application, since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation boosts the slew rate to over 150 V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor may be added to reduce the settling time for 0.1% error band to under 1 μs.

The high speed and fast settling time of these operational amplifiers make them useful in A/D converters, oscillators, active filters, sample-and-hold circuits, and general-purpose amplifiers.

The LM118 is characterized for operation from −55°C to 125°C. The LM218 is characterized for operation from −25°C to 85°C, and the LM318 is characterized for operation from 0°C to 70°C.

symbol



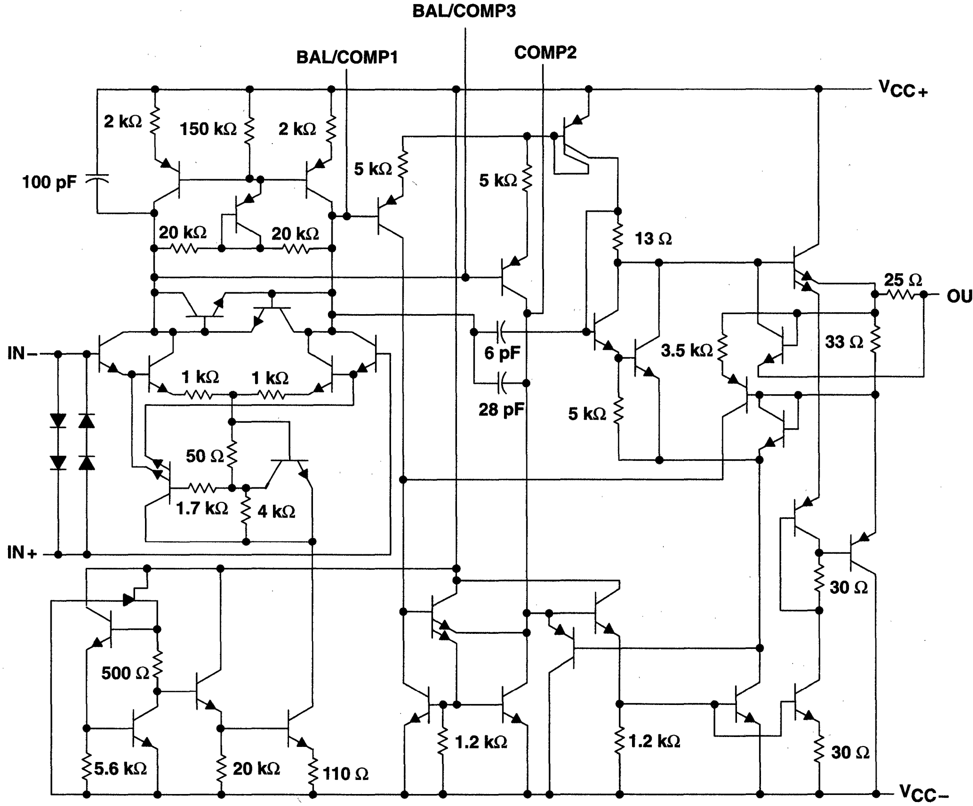
Pin numbers shown are for the D, JG, and P packages.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	10 mV	LM318D	—	—	LM318P
−25°C to 85°C	4 mV	LM218D	—	—	LM218P
−55°C to 125°C	4 mV	LM118D	LM118FK	LM118JG	LM118P

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM318DR).

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM118	LM218	LM318	UNIT
Supply voltage, V_{CC+} (see Note 1)		20	20	20	V
Supply voltage, V_{CC-} (see Note 1)		−20	−20	−20	V
Input voltage, V_I (either input, see Notes 1 and 2)		±15	±15	±15	V
Differential input current, V_{ID} (see Note 3)		±10	±10	±10	mA
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range, T_A		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 50	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300			°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for overvoltage protection. Therefore, excessive current flows if a different input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. The output can be shorted to ground or either power supply. For the LM118 and LM218 only, the unlimited duration of the short circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mV	5.8 mW/°C	64°C	464 mW	377 mW	145 mW
FK	500 mV	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mV	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mV	8.0 mW/°C	88°C	500 mW	500 mW	200 mW

electrical characteristics at specified free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS†	T_A‡	LM118, LM218			LM318			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		2	4		4	10	mV
			Full range			6			15	
I_{IO}	Input offset current	$V_O = 0$	25°C		6	50		30	200	nA
			Full range			100			300	
I_{IB}	Input bias current	$V_O = 0$	25°C		120	250		150	500	nA
			Full range			500			750	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm} = \pm15$ V	Full range	± 11.5			±11.5			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm} = \pm15$ V, $R_L = 2$ kΩ	Full range	±12	±13		±12	±13		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V, $R_L \geq 2$ kΩ	25°C	50	200		25	200		V/mV
			Full range	25			20			
B_1	Unity-gain bandwidth	$V_{CC\pm} = \pm15$ V	25°C		15			15		MHz
r_i	Input resistance		25°C	1*	3		0.5	3		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	Full range	80	100		70	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		Full range	70	80		65	80		dB
I_{CC}	Supply current	$V_O = 0$, No load	25°C		5	8		5	10	mA

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† All characteristics are measured under open-loop conditions with common-mode input voltage unless otherwise specified.

‡ Full range for LM118 is −55°C to 125°C, full range for LM218 is −25°C to 85°C, and full range for LM318 is 0°C to 70°C.

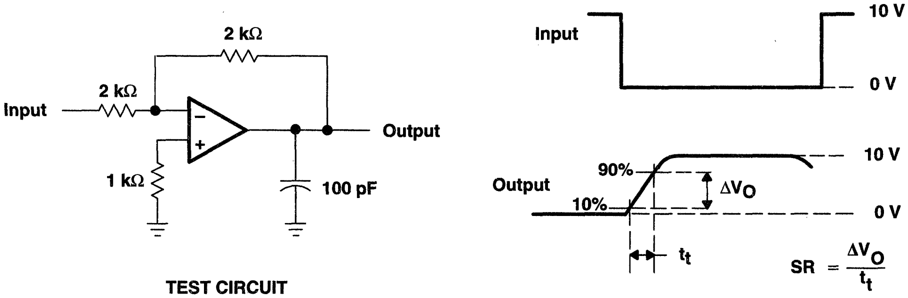
NOTE 5: Unless otherwise noted, $V_{CC} = \pm5$ V to ±20 V. All typical values are at $V_{CC\pm} = \pm15$ V and $T_A = 25°C$.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$\Delta V_I = 10$ V, $C_L = 100$ pF, See Figure 1	50*	70		V/μs

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

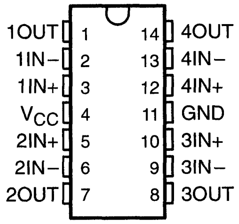
Figure 1. Slew Rate

LM124, LM124A, LM224, LM224A
LM324, LM324A, LM324Y, LM2902, LM2902Q
QUADRUPLE OPERATIONAL AMPLIFIERS

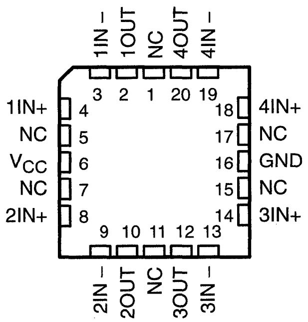
SLOS066E– SEPTEMBER 1975 – REVISED FEBRUARY1997

- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V
  (LM2902 and LM2902Q
  3 V to 26 V), or Dual Supplies
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing Near Ground**
- **Low Input Bias and Offset Parameters:**
  Input Offset Voltage . . . 3 mV Typ
  A Versions . . . 2 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 20 nA Typ
  A Versions . . . 15 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 32 V (26 V for LM2902 and LM2902Q)**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

LM124, LM124A . . . J OR W PACKAGE
ALL OTHERS . . . D, DB, N OR PW PACKAGE
(TOP VIEW)



LM124, LM124A . . . FK PACKAGE
(TOP VIEW)

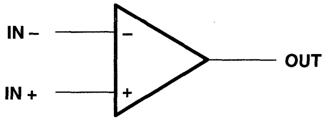


NC – No internal connection

description

These devices consist of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible when the difference between the two supplies is 3 V to 30 V (for the LM2902 and LM2902Q, 3 V to 26 V) and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

symbol (each amplifier)



Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM124 can be operated directly from the standard 5-V supply that is used in digital systems and easily provides the required interface electronics without requiring additional ±15-V supplies.

The LM2902Q is manufactured to demanding automotive requirements.

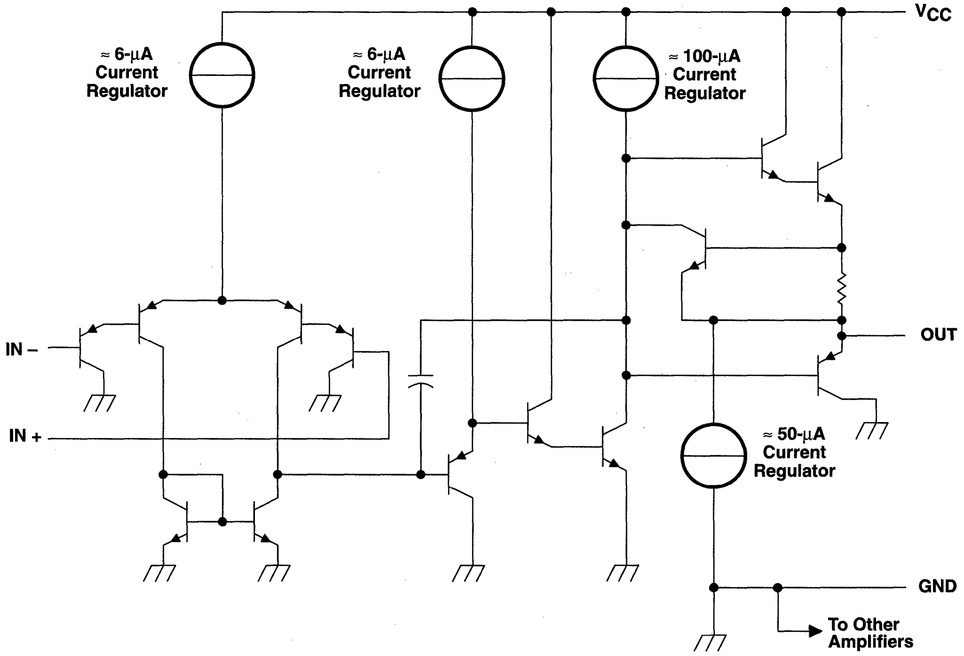
The LM124 and LM124A are characterized for operation over the full military temperature range of −55°C to 125°C. The LM224 and LM224A are characterized for operation from −25°C to 85°C. The LM324 and LM324A are characterized for operation from 0°C to 70°C. The LM2902 and LM2902Q are characterized for operation from −40°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES							CHIP FORM (Y)
		SMALL OUTLINE (D)†	VERY SMALL OUTLINE (DB)‡	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)‡	FLAT PACK (W)	
0°C to 70°C	7 mV	LM324D	LM324DBLE	—	—	LM324N	LM324PWLE	—	LM324Y
	3 mV	LM324AD	—	—	—	LM324AN	LM324APWLE	—	
−25°C to 85°C	5 mV	LM224D	—	—	—	LM224N	—	—	—
	3 mV	LM224AD	—	—	—	LM224AN	—	—	
−40°C to 125°C	7 mV	LM2902D	LM2902DBLE	—	—	LM2902N	LM2902PWLE	—	—
		LM2902QD		—	—	LM2902QN		—	
−55°C to 125°C	5 mV	—	—	LM124FK	LM124J	—	—	LM124W	—
	2 mV	—	—	LM124AFK	LM124AJ	—	—		

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM324DR).
‡ The DB and PW packages are only available left-end taped and reeled.

schematic (each amplifier)

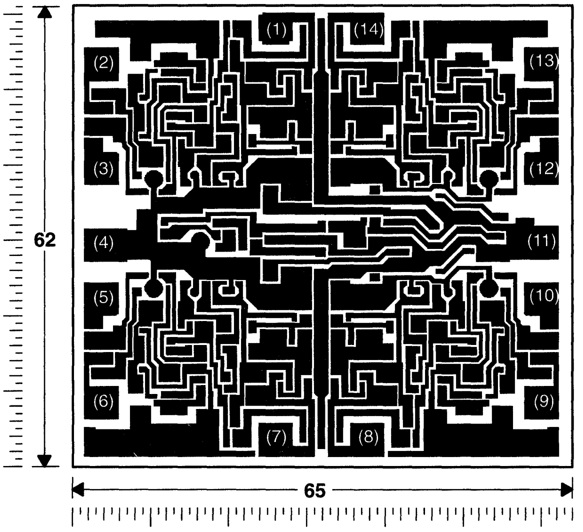


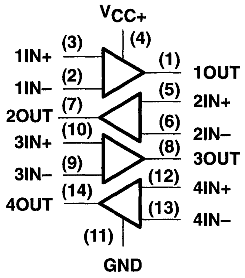
COMPONENT COUNT (total device)	
Epi-FET	1
Transistors	95
Diodes	4
Resistors	11
Capacitors	4

LM324Y chip information

This chip, when properly assembled, displays characteristics similar to the LM324. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ± 10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		LM124, LM124A LM224, LM224A LM324, LM324A	LM2902, LM2902Q	UNIT
Supply voltage, V_{CC} (see Note 1)		32	26	V
Differential input voltage, V_{ID} (see Note 2)		±32	±26	V
Input voltage, V_I (either input)		−0.3 to 32	−0.3 to 26	V
Duration of output short circuit (one amplifier) to ground at (or below) T_A = 25°C, $V_{CC} \leq 15$ V (see Note 3)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range, T_A	LM124, LM124A	−55 to 125		°C
	LM224, LM224A	−25 to 85		
	LM324, LM324A	0 to 70		
	LM2902, LM2902Q		−40 to 125	
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, DB, N, or PW package	260	260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
2. Differential voltages are at IN + with respect to IN −.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	900 mW	7.6 mW/°C	32°C	611 mW	497 mW	N/A
DB	775 mW	6.2 mW/°C	25°C	496 mW	403 mW	N/A
FK	900 mW	11.0 mW/°C	68°C	878 mW	713 mW	273 mW
J (LM124_)	900 mW	11.0 mW/°C	68°C	878 mW	713 mW	273 mW
J (all others)	900 mW	8.2 mW/°C	40°C	654 mW	531 mW	N/A
N	900 mW	9.2 mW/°C	52°C	734 mW	596 mW	N/A
PW	700 mW	5.6 mW/°C	25°C	448 mW	364 mW	N/A
W	900 mW	8.0 mW/°C	37°C	636 mW	516 mW	196 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	LM124, LM224			LM324			LM2902, LM2902Q			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR}min, V_O = 1.4 V	25°C		3	5		3	7		3	7	mV
			Full range			7			9			10	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	30		2	50		2	50	nA
			Full range			100			150			300	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−20	−150		−20	−250		−20	−250	nA
			Full range			−300			−500			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
			Full range	0 to V_{CC}−2			0 to V_{CC}−2			0 to V_{CC}−2			
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	V_{CC}−1.5			V_{CC}−1.5						V
		R_L = 10 kΩ	25°C							V_{CC}−1.5			
		V_{CC} = MAX, R_L = 2 kΩ	Full range	26			26			22			
		V_{CC} = MAX, R_L ≥ 10 kΩ	Full range	27	28		27	28		23	24		
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ	Full range		5	20		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L = ≥ 2 kΩ	25°C	50	100		25	100			100		V/mV
			Full range	25			15			15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	70	80		65	80		50	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		50	100		dB
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30	−60	−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30			30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load	Full range		1.4	3		1.4	3		1.4	3	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. MAX V_{CC} for testing purposes is 26 V for LM2902 and LM2902Q, 30 V for the others.

‡ Full range is −55°C to 125°C for LM124, −25°C to 85°C for LM224, 0°C to 70°C for LM324, and −40°C to 125°C for LM2902 and LM2902Q.

§ All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	LM124A			LM224A			LM324A			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$min, V_O = 1.4 V	25°C			2		2	3		2	3	mV
			Full range			4			4			5	
I_{IO}	Input offset current	V_O = 1.4 V	25°C			10			2	15	2	30	nA
			Full range			30			30			75	
I_{IB}	Input bias current	V_O = 1.4 V	25°C			−50		−15	−80		−15	−100	nA
			Full range			−100			−100			−200	
V_{ICR}	Common-mode input voltage range	V_{CC} = 30 V	25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
			Full range	0 to V_{CC}−2			0 to V_{CC}−2			0 to V_{CC}−2			
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	V_{CC}−1.5			V_{CC}−1.5			V_{CC}−1.5			V
		V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			26			
		V_{CC} = 30 V, R_L ≥ 10 kΩ	Full range	27			27	28		27	28		
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ	Full range			20		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L = ≥ 2 kΩ	Full range	25			25			15			V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	70			70	80		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65			65	100		65	100		dB
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20			−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10			10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12			12	30		12	30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = 30 V, V_O = 15 V, No load	Full range		1.4	3		1.4	3		1.4	3	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

‡ Full range is −55°C to 125°C for LM124A, −25°C to 85°C for LM224A, and 0°C to 70°C for LM324A.

§ All typical values are at T_A = 25°C.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	LM324Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, $V_{IC} = V_{ICR}$min, V_O = 1.4 V		3	7	mV
I_{IO}	Input offset current			2	50	nA
I_{IB}	Input bias current			−20	−250	nA
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	0 to V_{CC}−1.5			V
V_{OH}	High-level output voltage	R_L = 10 kΩ	V_{CC}−1.5			V
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ	15	100		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		65	100		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	−20	−30	−60	mA
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	10	20		
		V_{ID} = 1 V, V_O = 200 mV	12	30		
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V_{CC}, No load		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load		1.1	3	

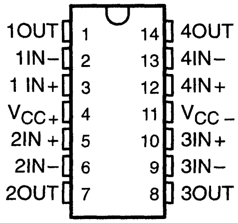
† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. MAX V_{CC} for testing purposes is 30 V.

LM148, LM248, LM348
QUADRUPLE OPERATIONAL AMPLIFIERS

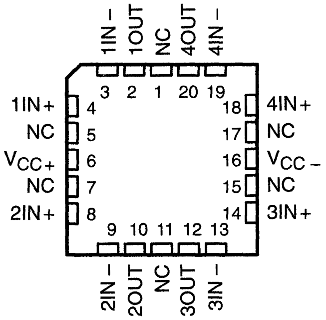
SLOS058B – OCTOBER 1979 – REVISED AUGUST 1996

- **μA741 Operating Characteristics**
- **Low Supply Current Drain . . . 0.6 mA Typ (per amplifier)**
- **Low Input Offset Voltage**
- **Low Input Offset Current**
- **Class AB Output Stage**
- **Input/Output Overload Protection**
- **Designed to Be Interchangeable With National LM148, LM248, and LM348**

LM148 . . . J PACKAGE
LM248, LM348 . . . D, N, OR PW PACKAGE
(TOP VIEW)



LM148 . . . FK PACKAGE
(TOP VIEW)



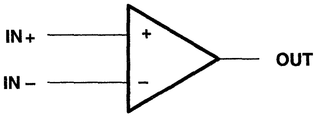
NC – No internal connection

description

The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the μA741. These amplifiers exhibit low supply current drain, and input bias and offset currents that are much less than those of the μA741.

The LM148 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM248 is characterized for operation from −25°C to 85°C, and the LM348 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	6 mV	LM348D	—	—	LM348N	LM348PW
−25°C to 85°C	6 mV	LM248D	—	—	LM248N	—
−55°C to 125°C	5 mV	—	LM148FK	LM148J	—	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM348DR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM148	LM248	LM348	UNIT
Supply voltage, V_{CC+} (see Note 1)		22	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−22	−18	−18	V
Differential input voltage, V_{ID} (see Note 2)		44	36	36	V
Input voltage, V_I (either input, see Notes 1 and 3)		±22	±18	±18	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range, T_A		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or PW package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	900 mW	7.6 mW/°C	32°C	611 mW	497 mW	N/A
FK	900 mW	11.0 mW/°C	68°C	878 mW	713 mW	273 mW
J	900 mW	11.0 mW/°C	68°C	878 mW	713 mW	273 mW
N	900 mW	9.2 mW/°C	52°C	734 mW	596 mW	N/A
PW	700 mW	5.6 mW/°C	N/A	448 mW	N/A	N/A

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	4	18	V
Supply voltage, V_{CC-}	−4	−18	V

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM148			LM248			LM348			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$		25°C		1	5		1	6		1	6	mV
				Full range			6			7.5			7.5	
I_{IO}	Input offset current	$V_O = 0$		25°C		4	25		4	50		4	50	nA
				Full range			75			125			100	
I_{IB}	Input bias current	$V_O = 0$		25°C		30	100		30	200		30	200	nA
				Full range			325			500			400	
V_{ICR}	Common-mode input voltage range			Full range	±12			±12			±12			V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		25°C	±12	±13		±12	±13		±12	±13		V
		$R_L \geq 10$ kΩ		Full range	±12			±12			±12			
		$R_L = 2$ kΩ		25°C	±10	±12		±10	±12		±10	±12		
		$R_L \geq 2$ kΩ		Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = \geq 2$ kΩ		25°C	50	160		25	160		25	160		V/mV
				Full range	25			15			15			
r_i	Input resistance‡			25°C	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
B_1	Unity-gain bandwidth	$A_{VD} = 1$		25°C		1			1			1		MHz
ϕ_m	Phase margin	$A_{VD} = 1$		25°C		60°			60°			60°		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $V_O = 0$		25°C	70	90		70	90		70	90		dB
				Full range	70			70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm9$ V to ±15 V, $V_O = 0$		25°C	77	96		77	96		77	96		dB
				Full range	77			77			77			
I_{OS}	Short-circuit output current			25°C		±25			±25			±25		mA
I_{CC}	Supply current (four amplifiers)	No load	$V_O = 0$	25°C					2.4	4.5		2.4	4.5	mA
			$V_O = V_{OM}$			2.4	3.6							
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 Hz to 20 kHz		25°C		120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55°C to 125°C for LM148, −25°C to 85°C for LM248, and 0°C to 70°C for LM348.

‡ This parameter is not production tested.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.5		V/µs

PARAMETER MEASUREMENT INFORMATION

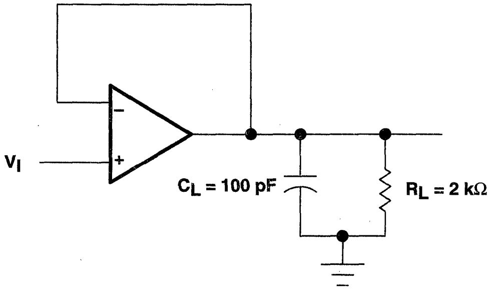


Figure 1. Unity-Gain Amplifier

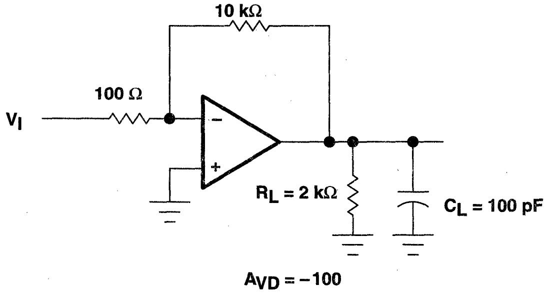


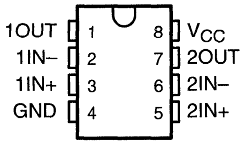
Figure 2. Inverting Amplifier

LM158, LM158A, LM258, LM358
LM258A, LM358A, LM358Y, LM2904, LM2904Q
DUAL OPERATIONAL AMPLIFIERS

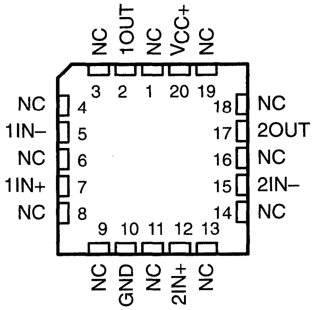
SLOS068B – JUNE 1976 – REVISED NOVEMBER 1996

- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V
  (LM2904 and LM2904Q
  3 V to 26 V) or Dual Supplies
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.7 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing Near Ground**
- **Low Input Bias and Offset Parameters:**
  Input Offset Voltage . . . 3 mV Typ
  A Versions . . . 2 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 20 nA Typ
  A Versions . . . 15 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±32 V (±26 V for LM2904 and LM2904Q)**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



LM158, LM158A . . . FK PACKAGE
(TOP VIEW)

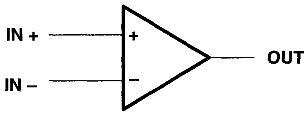


NC – No internal connection

description

These devices consist of two independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supply is also possible so long as the difference between the two supplies is 3 V to 30 V (3 V to 26 V for the LM2904 and LM2904Q), and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

symbol (each amplifier)



Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, these devices can be operated directly off of the standard 5-V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±5-V supplies.

The LM2904Q is manufactured to demanding automotive requirements.

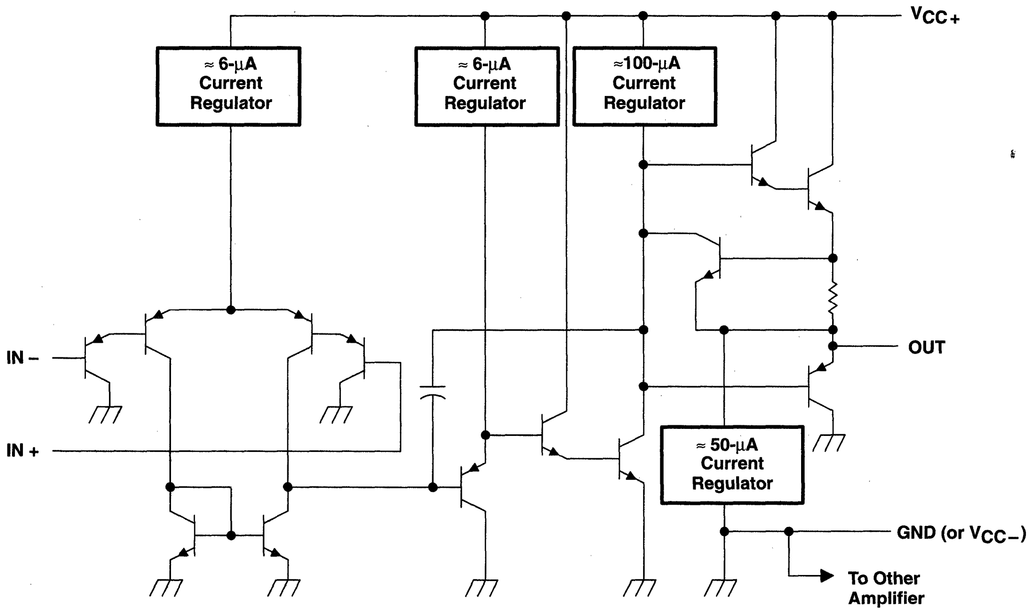
The LM158 and LM158A are characterized for operation over the full military temperature range of −55°C to 125°C. The LM258 and LM258A are characterized for operation from −25°C to 85°C, the LM358 and LM358A from 0°C to 70°C, and the LM2904 and LM2904Q from −40°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D)†	SSOP (DB)‡	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)‡	
0°C to 70°C	7 mV 3 mV	LM358D	LM358DB			LM358P LM358AP	LM358PW	LM358Y
−25°C to 85°C	5 mV 3 mV	LM258D				LM258P LM258AP		
−40°C to 125°C	7 mV	LM2904D LM2904QD	LM2904DB —			LM2904P LM2904QP	LM2904PW —	
−55°C to 125°C	5 mV 2 mV	LM158D		LM158FK LM158AFK	LM158JG LM158AJG	LM158P		

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM358DR).
‡ The DB and PW packages are only available left-end taped and reeled. Add the suffix LE to the device type (e.g., LM358DBLE).

schematic (each amplifier)

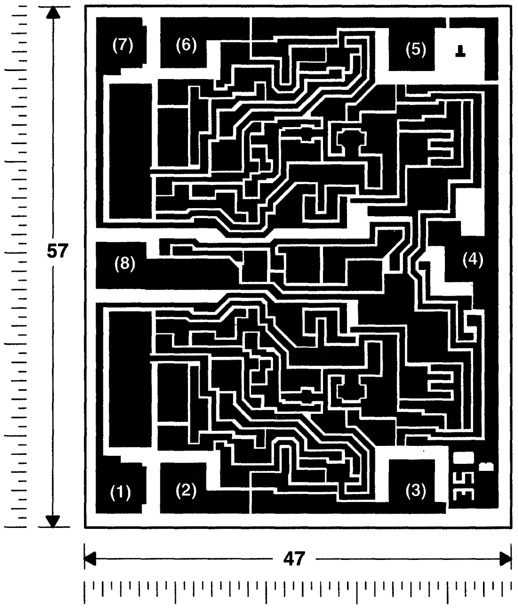


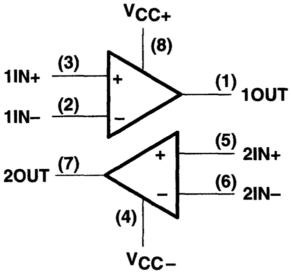
COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	7
Transistors	51
Capacitors	2

LM358Y chip information

These chips, when properly assembled, display characteristics similar to the LM358. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ± 10 %.

ALL DIMENSIONS ARE IN MILS.

NO BACKSIDE METALLIZATION

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM158, LM158A LM258, LM258A LM358, LM358A	LM2904, LM2904Q	UNIT
Supply voltage V_{CC} (see Note 1)		32	26	V
Differential input voltage (see Note 2)		±32	±26	V
Input voltage (either input)		–0.3 to 32	–0.3 to 26	V
Duration of output short circuit (one amplifier) to ground at (or below) 25°C free-air temperature ($V_{CC} \leq 15$ V) (see Note 3)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range	LM158, LM158A	−55 to 125		°C
	LM258, LM258A	−25 to 85		
	LM358, LM358A	0 to 70		
	LM2904, LM2904Q		−40 to 125	
Storage tempereture range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead tempeature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead tempeature 1,6 mm (1/16 inch) from case for 10 seconds	D, DB, P, or PW package	260	260	°C

NOTES: 1. All voltage values, except differential voltages and V_{CC} specified for measurement of I_{OS}, are with respect to the network ground terminal.

2. Differential voltages are at IN+ with respect to IN–.

3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB	525 mW	4.2 mW/°C	336 mW	273 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	–

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	LM158, LM258			LM358			LM2904, LM2904Q			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR}min, V_O = 1.4 V	25°C		3	5		3	7		3	7	mV
			Full range			7			9			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		7			7			7		μV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	30		2	50		2	50	nA
			Full range			100			150			300	
α_{IIO}	Average temperature coefficient of input offset current		Full range		10			10			10		pA/°C
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−20	−150		−20	−250		−20	−250	nA
			Full range			−300			−500			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	$R_L \geq 2$ kΩ	25°C	$V_{CC}-1.5$			$V_{CC}-1.5$						V
		$R_L \geq 10$ kΩ	25°C									$V_{CC}-1.5$	
		V_{CC} = MAX, R_L = 2 kΩ	Full range	26			26			26			
		V_{CC} = MAX, $R_L \geq 10$ kΩ	Full range	27	28		27	28		23	24		
V_{OL}	Low-level output voltage	$R_L \leq 10$ kΩ	Full range		5	20		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L = \geq 2$ kΩ	25°C	50	100		25	100		25	100		V/mV
			Full range	25			15			15			
CMRR	Common-mode rejection ratio	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min	25°C	70	80		65	80		50	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{CC} = 5 V to MAX	25°C	65	100		65	100		65	100		dB
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB

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† All characterisctics are measured under open-loop conditions with zero common-mode input voltage unless otherwise speicifed. MAX V_{CC} for testing purposes is 26 V for LM 2904 and 30 V for others.

‡ Full range is −55°C to 125°C for LM158, −25°C to 85°C for LM258, 0°C to 70°C for LM358, and −40°C to 125°C for LM2904 and LM2904Q.

§ All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		T_A‡	LM158, LM258			LM358			LM2904, LM2904Q			UNIT
					MIN	TYP§	MAX	MIN	TYP§	MAX	MIN	TYP§	MAX	
I_O	Output current	V_{CC} = 15 V, V_O = 0	V_{ID} = 1 V,	25°C	−20	−30		−20	−30		−20	−30		mA
				Full range	−10			−10			−10			
		V_{CC} = 15 V, V_O = 15 V	V_{ID} = −1 V,	25°C	10	20		10	20		10	20		
				Full range	5			5			5			
		V_{ID} = −1 V,	V_O = 200 mV	25°C	12	30		12	30			30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, V_O = 0	GND at −5 V,	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V,	No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, No load	V_O = 0.5 V,	Full range		1	2		1	2		1	2	

† All characterisctics are measured under open-loop conditions with zero common-mode input voltage unless otherwise speicifed. MAX V_{CC} for testing purposes is 26 V for LM 2904 and 30 V for others.

‡ Full range is −55°C to 125°C for LM158, −25°C to 85°C for LM258, 0°C to 70°C for LM358, and −40°C to 125°C for LM2904 and LM2904Q.

§ All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	LM158A			LM258A			LM358A			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$min, V_O = 1.4 V	25°C			2		2	3		2	3	mV
			Full range			4			4			5	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		7	15*		7	15		7	20	µV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	10		2	15		2	30	nA
			Full range			30			30			75	
α_{IIO}	Average temperature coefficient of input offset current		Full range		10	200		10	200		10	300	pA/°C
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−15	−50		−15	−80		−15	−100	nA
			Full range			−100			−100			−200	
V_{ICR}	Common-mode input voltage range	V_{CC} = 30 V	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	$R_L \geq 2$ kΩ	25°C	$V_{CC}-1.5$			$V_{CC}-1.5$			$V_{CC}-1.5$			V
		V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			26			
		V_{CC} = 30 V, $R_L \geq 10$ kΩ	Full range	27	28		27	28		27	28		
V_{OL}	Low-level output voltage	$R_L \leq 10$ kΩ	Full range		5	20		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L = \geq 2$ kΩ	25°C	50	100		50	100		25	100		V/mV
			Full range	25			25			15			
CMRR	Common-mode rejection ratio		25°C	70	80		70	80		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		25°C	65	100		65	100		65	100		dB
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

‡ Full range is −55°C to 125°C for LM158A, −25°C to 85°C for LM258A, and 0°C to 70°C for LM358A.

§ All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†	T_A‡	LM158A			LM258A			LM358A			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	MIN	TYP§	MAX	
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30	−60	−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30			30		µA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V, No load	Full range		1	2		1	2		1	2	

† All characterisctics are measured under open-loop conditions with zero common-mode input voltage unless otherwise speicifed. MAX V_{CC} for testing purposes is 26 V for LM 2904 and 30 V for others.

‡ Full range is −55°C to 125°C for LM158, −25°C to 85°C for LM258, 0°C to 70°C for LM358, and −40°C to 125°C for LM2904 and LM2904Q.

§ All typical values are at T_A = 25°C.

electrical characteristics V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	LM358Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, $V_{IC} = V_{ICR}$min, V_O = 1.4 V		3	7	mV
I_{IO}	Input offset current			2	50	nA
I_{IB}	Input bias current			–20	–250	nA
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	0 to V_{CC}–1.5			V
V_{OH+}	High-level output voltage	R_L ≥ 10 kΩ	V_{CC}–1.5			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L = ≥ 2 kΩ	15	100		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		65	100		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	–20	–30	–60	mA
		V_{CC} = 15 V, V_{ID} = –1 V, V_O = 15 V	10	20		
		V_{ID} = 1 V, V_O = 200 mV	12	30		
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at –5 V, V_O = 0		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V, No load		1	2	

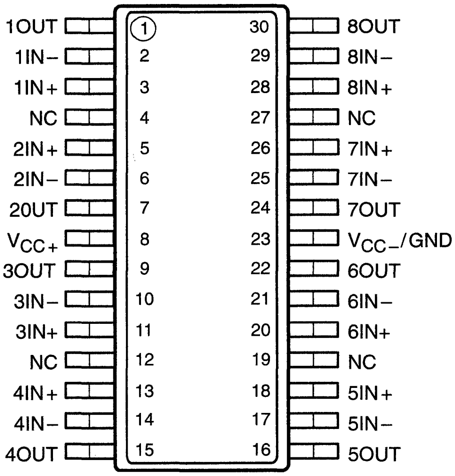
† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. MAX V_{CC} for testing purposes is 30 V.

LM324x2
OCTAL OPERATIONAL AMPLIFIER

SLOS133A – APRIL 1994 – REVISED AUGUST 1996

- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V
  or Dual Supplies
- **Low Supply-Current Drain Independent of Supply Voltage . . . 1.4 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing Near Ground**
- **Low Input Bias and Offset Parameters:**
  Input Offset Voltage . . . 3 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . –20 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 32 V**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

DB PACKAGE
(TOP VIEW)

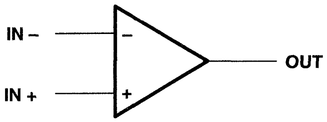


NC – No internal connection

description

The LM324x2 device consists of eight independent, high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible when the difference between the two supplies is 3 V to 30 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

symbol (each amplifier)



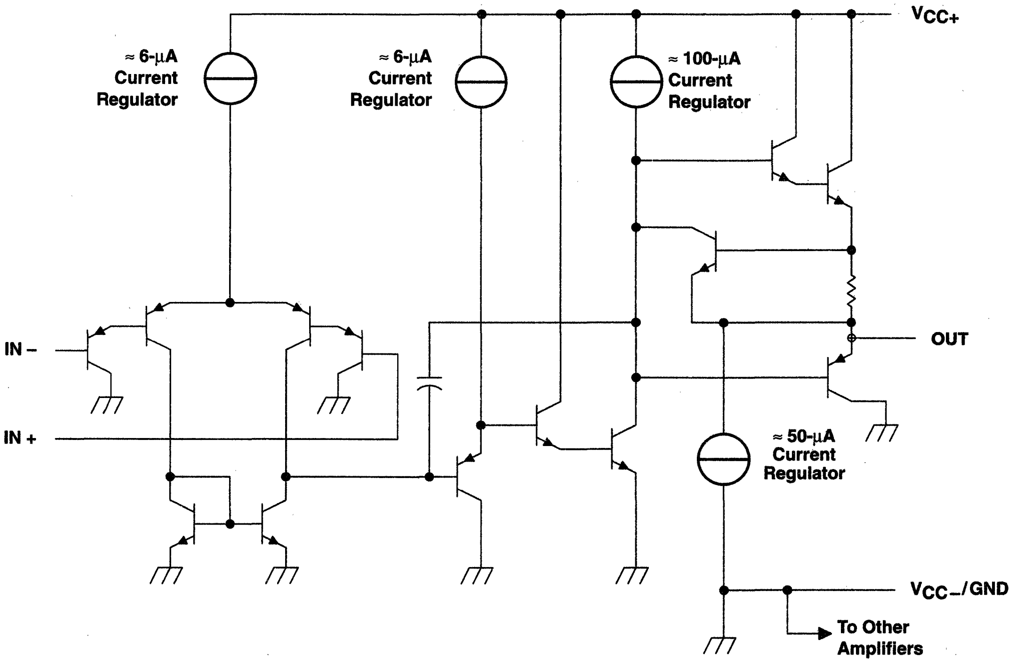
Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational-amplifier circuits that now can be more easily implemented in single-supply-voltage systems.

AVAILABLE OPTION

T_A	V_{IO}max AT 25°C	PACKAGE SMALL OUTLINE (DB)†
0°C to 70°C	7 mV	LM324x2DBLE

† The DB package is only available left-end taped and reeled.

schematic (each amplifier)



COMPONENT COUNT (total device)	
Epi-FET	2
Transistors	190
Diodes	8
Resistors	22
Capacitors	8

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	32 V
Differential input voltage, V_{ID} (see Note 2)	±32 V
Input voltage range, V_I (any input)	−0.3 V to 32 V
Duration of output short circuit to ground (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages and V_{CC} specified for the measurement of I_{OS}, are with respect to GND.
2. Differential voltages are at IN + with respect to IN −.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	1024 mW	8.2 mW/°C	655 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A‡	MIN	TYP§	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR}min,	V_O = 1.4 V	25°C		3	7	mV
				Full range			9	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		2	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−20	−250	nA
				Full range			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX		25°C	0 to $V_{CC}-1.5$			V
				Full range	0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L = 2 kΩ		25°C	$V_{CC}-1.5$			V
		V_{CC} = MAX,	R_L = 2 kΩ	Full range	26			
		V_{CC} = MAX,	$R_L \geq 10$ kΩ	Full range	27	28		
V_{OL}	Low-level output voltage	$R_L \leq 10$ kΩ		Full range		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, R_L = ≥ 2 kΩ	V_O = 1 V to 11 V,	25°C	25	100		V/mV
				Full range	15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C	65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)			25°C	65	100		dB
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120		dB
I_O	Output current	V_{CC} = 15 V, V_O = 0	V_{ID} = 1 V,	25°C	−20	−30	−60	mA
				Full range	−10			
		V_{CC} = 15 V, V_O = 15 V	V_{ID} = −1 V,	25°C	10	20		
				Full range	5			
		V_{ID} = −1 V,	V_O = 200 mV	25°C	12	30		μA
I_{OS}	Short-circuit output current	V_O = 0,	GND = −5 V	25°C		±40	±60	mA
I_{CC}	Supply current (eight amplifiers)	V_O = 2.5 V,	No load	Full range		1.4	2.4	mA
		V_{CC} = MAX, No load	V_O = 0.5 V_{CC},	Full range		2.2	6	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. MAX V_{CC} for testing purposes is 30 V.

‡ Full range is 0°C to 70°C.

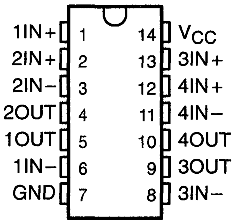
§ All typical values are at T_A = 25°C.

LM2900, LM3900
QUADRUPLE NORTON OPERATIONAL AMPLIFIERS

SLOS059 – JULY 1979 – REVISED SEPTEMBER 1990

- **Wide Range of Supply Voltages, Single or Dual Supplies**
- **Wide Bandwidth**
- **Large Output Voltage Swing**
- **Output Short-Circuit Protection**
- **Internal Frequency Compensation**
- **Low Input Bias Current**
- **Designed to Be Interchangeable With National Semiconductor LM2900 and LM3900, Respectively**

N PACKAGE
(TOP VIEW)

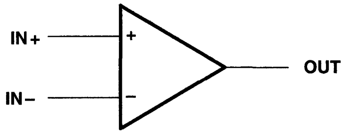


description

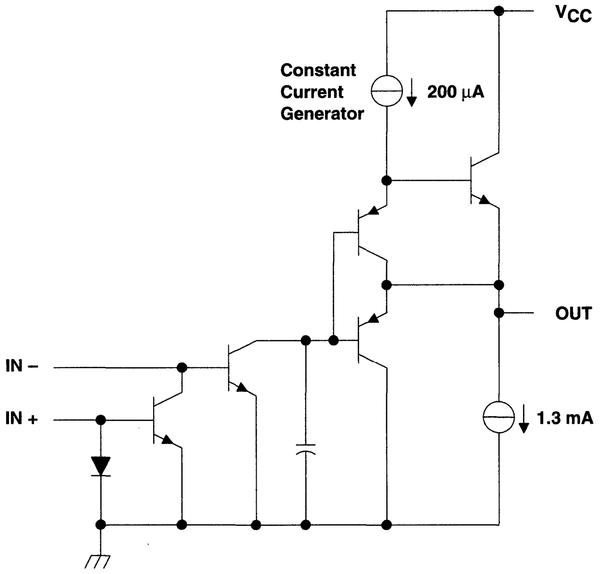
These devices consist of four independent, high-gain frequency-compensated Norton operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible. The low supply current drain is essentially independent of the magnitude of the supply voltage. These devices provide wide bandwidth and large output voltage swing.

The LM2900 is characterized for operation from −40°C to 85°C, and the LM3900 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



schematic (each amplifier)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	LM2900	LM3900	UNIT
Supply voltage, V_{CC} (see Note 1)	36	36	V
Input current	20	20	mA
Duration of output short circuit (one amplifier) to ground at (or below) 25°C free-air temperature (see Note 2)	unlimited	unlimited	
Continuous total dissipation	See Dissipation Rating Table		
Operating free-air temperature range	−40 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	LM2900		LM3900		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC} (single supply)	4.5	32	4.5	32	V
Supply voltage, V_{CC+} (dual supply)	2.2	16	2.2	16	V
Supply voltage, V_{CC-} (dual supply)	−2.2	−16	−2.2	−16	V
Input current (see Note 3)		−1		−1	mA
Operating free-air temperature, T_A	−40	85	0	70	°C

NOTE 3: Clamp transistors are included that prevent the input voltages from swinging below ground more than approximately −0.3 V. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately −1 mA. Negative input currents in excess of −4 mA causes the output voltage to drop to a low voltage. These values apply for any one of the input terminals. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common-mode current biasing can be used to prevent negative input voltages.

electrical characteristics, V_{CC} = 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM2900			LM3900			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IB}	Input bias current (inverting input)	I_{I+} = 0	T_A = 25°C		30	200		30	200	nA
			T_A = Full range		300			300		
	Mirror gain	I_{I+} = 20 µA to 200 µA T_A = Full range, See Note 4		0.9		1.1	0.9		1.1	µA/µA
	Change in mirror gain				2%	5%		2%	5%	
	Mirror current	$V_{I+} = V_{I-}$, T_A = Full range, See Note 4			10	500		10	500	µA
A_{VD}	Large-signal differential voltage amplification	V_O = 10 V, R_L = 10 kΩ, f = 100 Hz		1.2	2.8		1.2	2.8		V/mV
r_i	Input resistance (inverting input)				1			1		MΩ
r_o	Output resistance				8			8		kΩ
B_1	Unity-gain bandwidth (inverting input)				2.5			2.5		MHz
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)				70			70		dB
V_{OH}	High-level output voltage	I_{I+} = 0, I_{I-} = 0	R_L = 2 kΩ	13.5			13.5			V
			V_{CC} = 30 V, No load		29.5			29.5		
V_{OL}	Low-level output voltage	I_{I+} = 0, I_{I-} = 10 µA, R_L = 2 kΩ			0.09	0.2		0.09	0.2	V
I_{OS}	Short-circuit output current (output internally high)	I_{I+} = 0, I_{I-} = 0, V_O = 0		−6	−18		−6	−10		mA
	Pulldown current			0.5	1.3		0.5	1.3		mA
I_{OL}	Low-level output current‡	I_{I-} = 5 µA V_{OL} = 1 V			5			5		mA
I_{CC}	Supply current (four amplifiers)	No load			6.2	10		6.2	10	mA

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for LM2900 and 0°C to 70°C for LM3900.

‡ The output current-sink capability can be increased for large-signal conditions by overdriving the inverting input.

NOTE 4: These parameters are measured with the output balanced midway between V_{CC} and GND.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	Low-to-high output	V_O = 10 V, C_L = 100 pF, R_L = 2 kΩ		0.5		V/µs
		High-to-low output			20		

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT (INVERTING INPUT) vs FREE-AIR TEMPERATURE

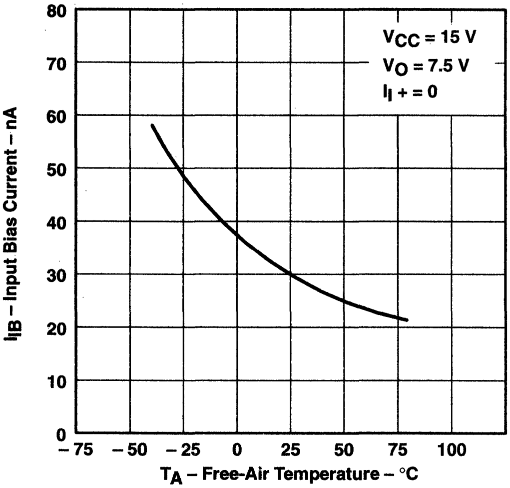


Figure 1

MIRROR GAIN vs FREE-AIR TEMPERATURE

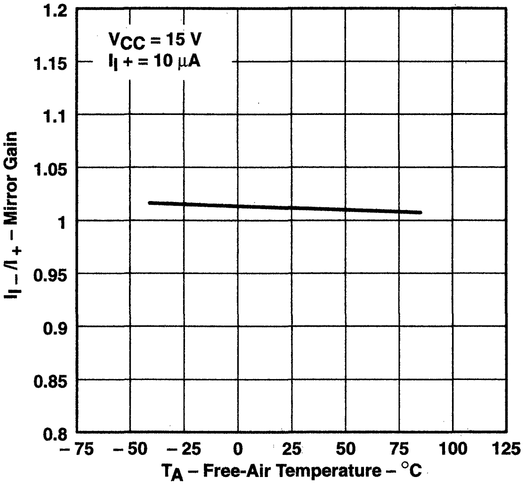


Figure 2

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

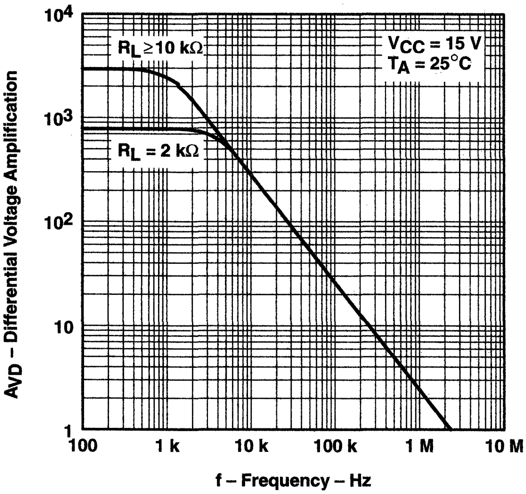


Figure 3

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

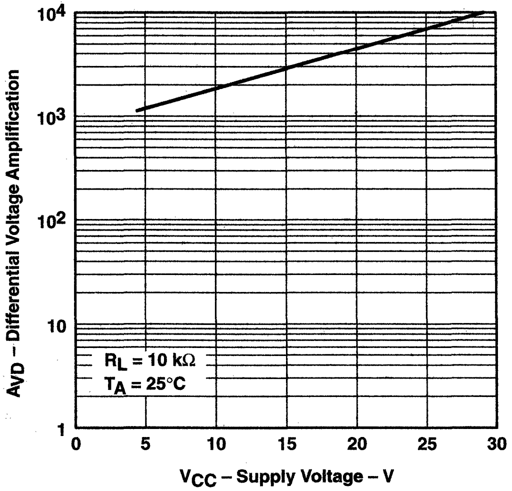


Figure 4

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

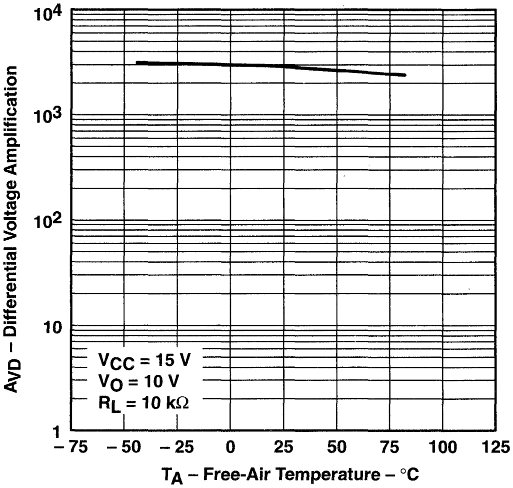

Figure 5

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

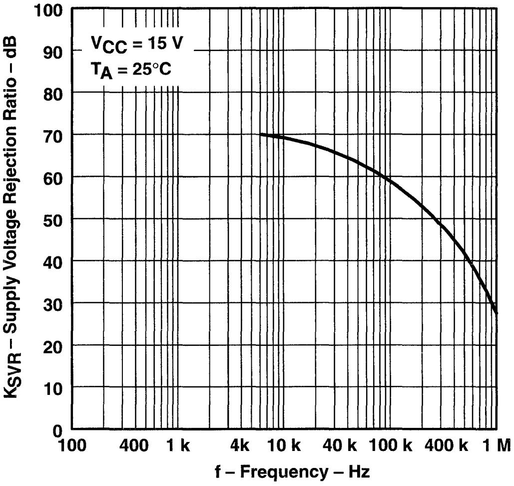

Figure 6

PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

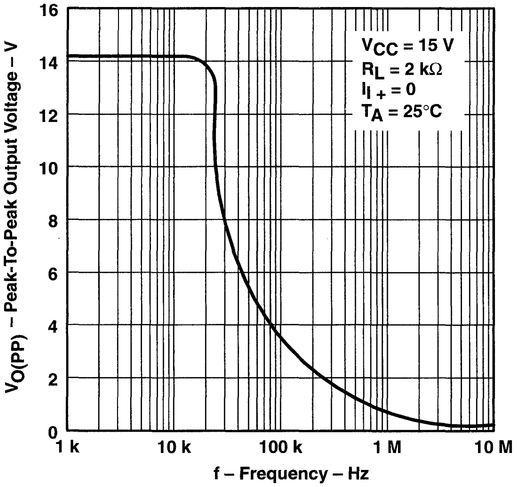

Figure 7

SHORT-CIRCUIT OUTPUT CURRENT (OUTPUT INTERNALLY HIGH) vs SUPPLY VOLTAGE

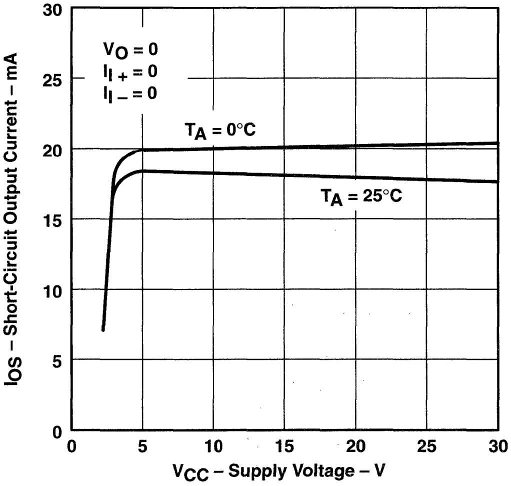

Figure 8

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

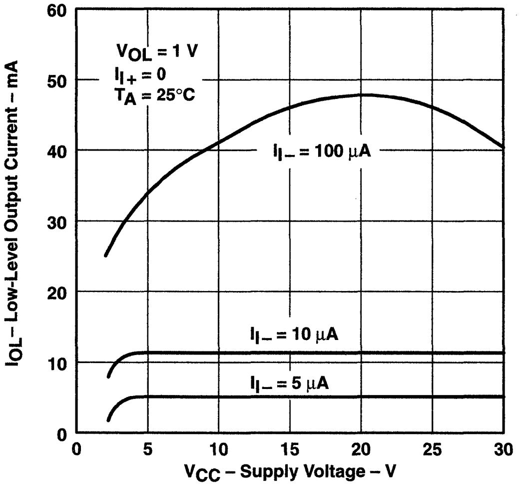

Figure 9

PULLDOWN CURRENT
vs
SUPPLY VOLTAGE

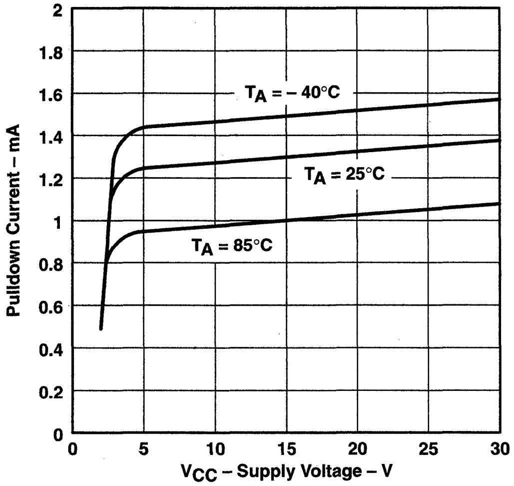

Figure 10

PULLDOWN CURRENT
vs
FREE-AIR TEMPERATURE

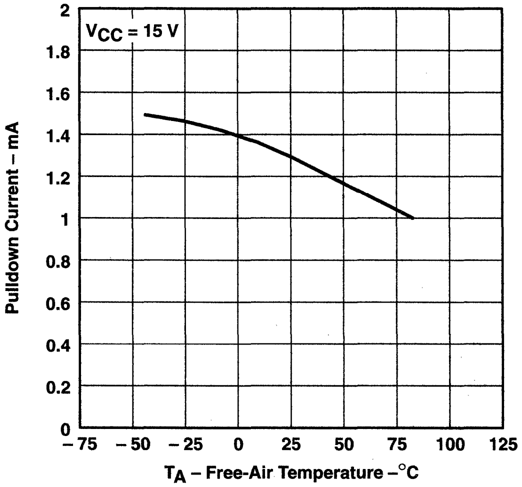

Figure 11

TOTAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE

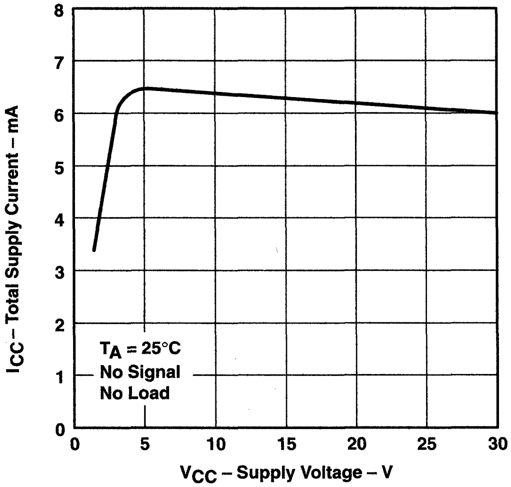

Figure 12

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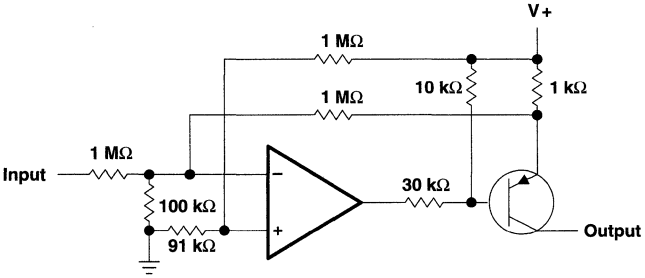
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

Norton (or current-differencing) amplifiers can be used in most standard general-purpose operational amplifier applications. Performance as a dc amplifier in a single-power-supply mode is not as precise as a standard integrated-circuit operational amplifier operating from dual supplies. Operation of the amplifier can best be understood by noting that input currents are differenced at the inverting input terminal and this current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near (or even below) ground.

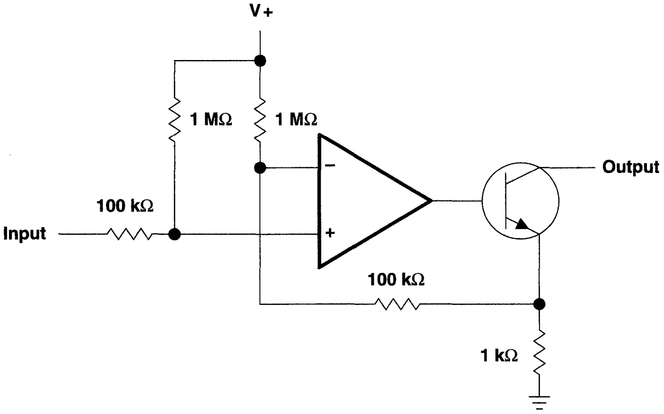
Internal transistors clamp negative input voltages at approximately −0.3 V but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately −100 μA.

Noise immunity of a Norton amplifier is less than that of standard bipolar amplifiers. Circuit layout is more critical since coupling from the output to the noninverting input can cause oscillations. Care must also be exercised when driving either input from a low-impedance source. A limiting resistor should be placed in series with the input lead to limit the peak input current. Current up to 20 mA will not damage the device, but the current mirror on the noninverting input will saturate and cause a loss of mirror gain at higher current levels, especially at high operating temperatures.



$I_O \approx$ 1 mA per input volt

Figure 13. Voltage-Controlled Current Source



$I_O \approx$ 1 mA per input volt

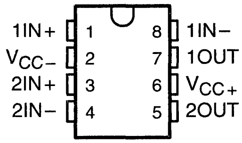
Figure 14. Voltage-Controlled Current Sink

LT1013, LT1013A, LT1013D, LT1013Y
DUAL PRECISION OPERATIONAL AMPLIFIERS

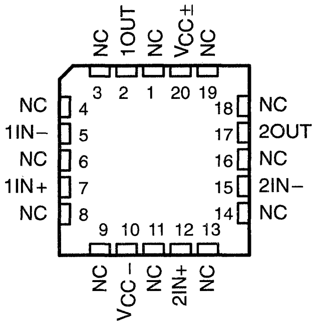
SLOS018B – MAY 1988 – REVISED OCTOBER 1996

- **Single-Supply Operation:**
  Input Voltage Range Extends to Ground
  Output Swings to Ground While Sinking Current
- **Input Offset Voltage**
  150 µV Max at 25°C for LT1013A
- **Offset Voltage Temperature Coefficient**
  2.5 µV/°C Max for LT1013A
- **Input Offset Current**
  0.8 nA Max at 25°C for LT1013A
- **High Gain . . . 1.5 V/µV Min (R_L = 2 kΩ), 0.8 V/µV Min (R_L = 600 kΩ) for LT1013A**
- **Low Supply Current . . . 0.5 mA Max at T_A = 25°C for LT1013A**
- **Low Peak-to-Peak Noise Voltage**
  0.55 µV Typ
- **Low Current Noise . . . 0.07 pA/$\sqrt{\text{HZ}}$ Typ**

D PACKAGE
(TOP VIEW)

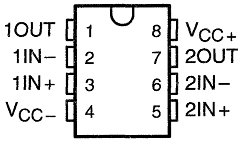


FK PACKAGE
(TOP VIEW)



NC – No internal connection

JG OR P PACKAGE
(TOP VIEW)



description

The LT1013 is a dual precision operational amplifier featuring low offset voltage temperature coefficient, high gain, low supply current, and low noise.

The LT1013 can be operated from a single 5-V power supply; the common-mode input voltage range includes ground, and the output can also swing to within a few millivolts of ground. Crossover distortion is eliminated. The LT1013 can be operated with both dual ±15-V and single 5-V supplies.

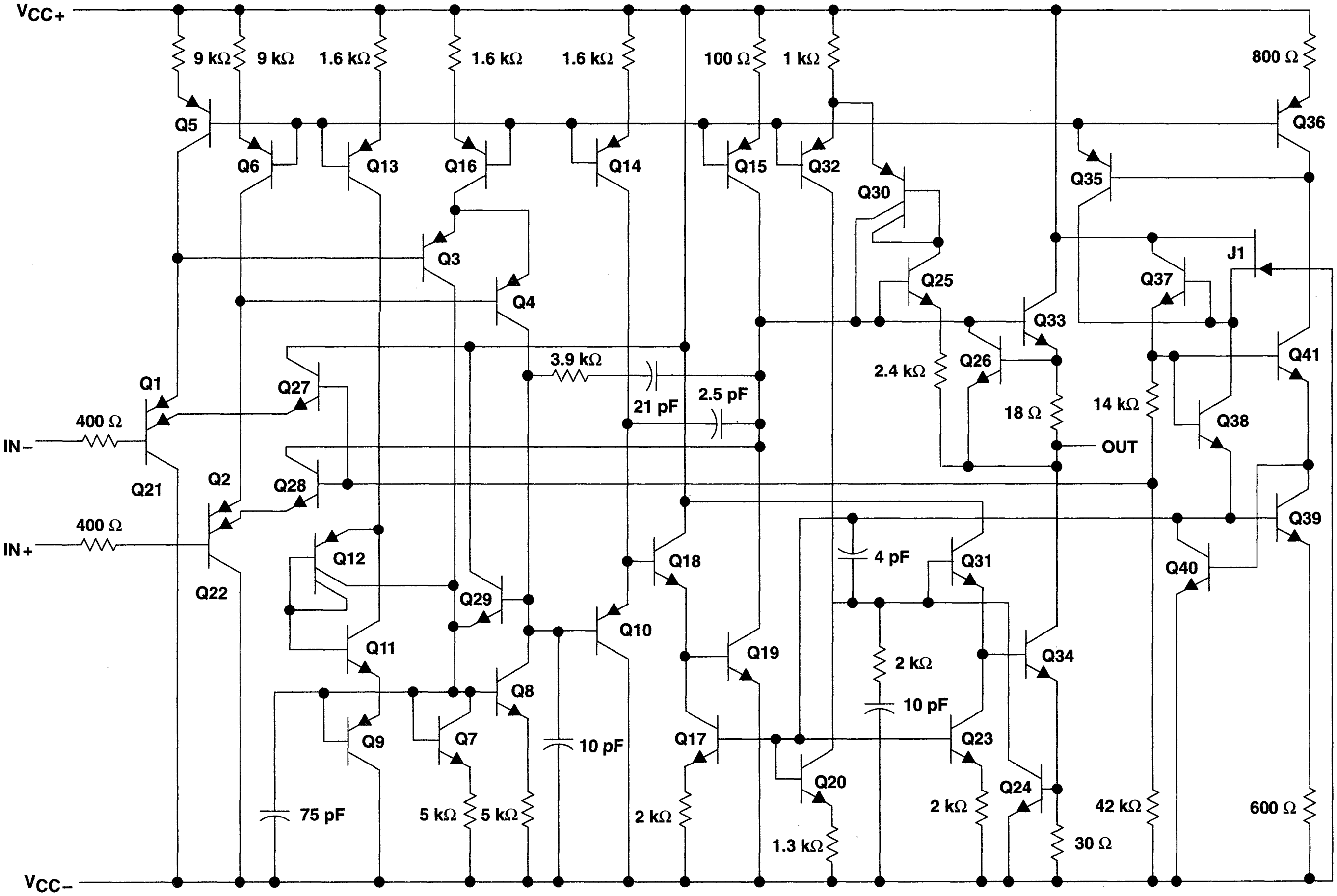
The LT1013C and LT1013AC, and LT1013D are characterized for operation from 0°C to 70°C. The LT1013I and LT1013AI, and LT1013DI are characterized for operation from –40°C to 105°C. The LT1013M and LT1013AM, and LT1013DM are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	150 µV 300 µV 800 µV	— — LT1013DD	— — —	— — —	LT1013ACP LT1013CP LT1013DP	LT1013Y
−40°C to 105°C	150 µV 300 µV 800 µV	— — LT1013DID	— — —	— — —	LT1013AIP LT1013IP LT1013DIP	—
−55°C to 125°C	150 µV 300 µV 800 µV	— — LT1013DMD	LT1013AMFK LT1013MFK —	— LT1013MJG LT1013DMJG	LT1013AMP LT1013MP LT1013DMP	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LT1013DDR).

schematic (each amplifier)

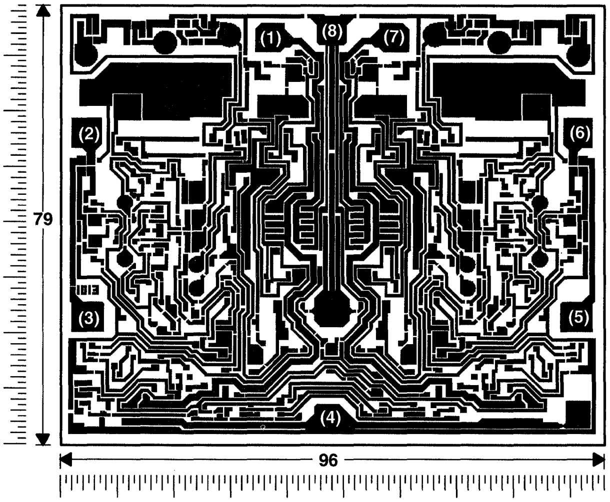


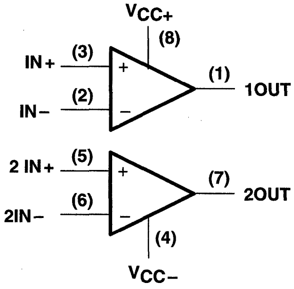
Component values are nominal.

LT1013Y chip information

This chip, when properly assembled, displays characteristics similar to the LT1013. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Differential input voltage (see Note 2)	±30 V
Input voltage range, V_I (any input, see Note 1)	V_{CC-} −5 V to V_{CC+}
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Operating free-air temperature range, T_A: LT1013C, LT1013AC, LT1013D	−0 °C to 70°C
LT1013I, LT1013AI, LT1013DI	−40°C to 105°C
LT1013M, LT1013AM, LT1013DM	−55 °C to 125°C
Storage temperature range	−65 °C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013C			LT1013AC			LT1013DC			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$	25°C		60	300		40	150		200	800	µV
			Full range			400			240			1000	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	2.5		0.3	2		0.7	5	µV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.4			0.5		µV/mo
I_{IO}	Input offset current		25°C		0.2	1.5		0.15	0.8		0.2	1.5	nA
			Full range			2.8			1.5			2.8	
I_{IB}	Input bias current		25°C		−15	−30		−12	−20		−15	−30	nA
			Full range			−38			−25			−38	
V_{ICR}	Common-mode input voltage range		25°C	−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		V
			Full range	−15 to 13			−15 to 13			−15 to 13			
V_{OM}	Maximum peak output voltage swing	$R_L = 2\ k\Omega$	25°C	±12.5	±14		±13	±14		±12.5	±14		V
			Full range	±12			±12.5			±12			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 600\ \Omega$	25°C	0.5	0.2		0.8	2.5		0.5	2		V/µV
		$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	1.2	7		1.5	8		1.2	7		
			Full range	0.7			1			0.7			
CMRR	Common-mode rejection ratio	$V_{IC} = -15$ V to 13.5 V	25°C	97	114		100	117		97	114		dB
		$V_{IC} = -14.9$ V to 13 V	Full range	94			98			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC+} = \pm2$ V to ±18 V	25°C	100	117		103	120		100	117		dB
			Full range	97			101			97			
	Channel separation	$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	120	137		123	140		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		100	400		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			5			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.5		0.35	0.55	mA
			Full range			0.7			0.55			0.6	

† Full range is 0°C to 70°C.
‡ All typical values are at $T_A = 25°C$.

electrical characteristics at specified free-air temperature, $V_{CC+} = 5$ V, $V_{CC-} = 0$, $V_O = 1.4$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013C			LT1013AC			LT1013DC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$	25°C		90	450		60	250		250	950	µV
			Full range			570			350			1200	
I_{IO}	Input offset current		25°C		0.3	2		0.2	1.3		0.3	2	nA
			Full range			6			3.5			6	
I_{IB}	Input bias current		25°C		−18	−50		−15	−35		−18	−50	nA
			Full range			−90			−55			−90	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		0 to 3.5	0.3 to 3.8		V
			Full range	0 to 3			0 to 3			0 to 3			
V_{OM}	Maximum-peak output voltage swing	Output low, No load	25°C		15	25		15	25		15	25	mV
		Output low, $R_L = 600\ \Omega$ to GND	25°C		5	10		5	10		5	10	
			Full range			13			13			13	
		Output low, $I_{sink} = 1$ mA	25°C		220	350		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		4	4.4		V
		Output high, $R_L = 600\ \Omega$ to GND	25°C	3.4	4		3.4	4		3.4	4		
			Full range	3.2			3.3			3.2			
A_{VD}	Large-signal differential voltage amplification	$V_O = 5$ mV to 4 V, $R_L = 500\ \Omega$	25°C		1			1			1		V/µV
I_{CC}	Supply current per amplifier		25°C		0.32	0.5		0.31	0.45		0.32	0.5	mA
			Full range			0.55			0.5			0.55	

† Full range is −0°C to 70°C.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $V_{IC} = 0$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		µV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013I MIN	LT1013I TYP‡	LT1013I MAX	LT1013AI MIN	LT1013AI TYP‡	LT1013AI MAX	LT1013DI MIN	LT1013DI TYP‡	LT1013DI MAX	UNIT
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$	25°C		60	300		40	150		200	800	µV
			Full range			550			300			1000	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	2.5		0.3	2		0.7	5	µV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.4			0.5		µV/mo
I_{IO}	Input offset current		25°C		0.2	1.5		0.15	0.8		0.2	1.5	nA
			Full range			2.8			1.5			2.8	
I_{IB}	Input bias current		25°C		−15	−30		−12	−20		−15	−30	nA
			Full range			−38			−25			−38	
V_{ICR}	Common-mode input voltage range		25°C	−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		V
			Full range	−15 to 13			−15 to 13			−15 to 13			
V_{OM}	Maximum peak output voltage swing	$R_L = 2\ k\Omega$	25°C	±12.5	±14		±13	±14		±12.5	±14		V
			Full range	±12			±12.5			±12			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 600\ \Omega$	25°C	0.5	0.2		0.8	2.5		0.5	2		V/µV
		$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	1.2	7		1.5	8		1.2	7		
			Full range	0.7			1			0.7			
CMRR	Common-mode rejection ratio	$V_{IC} = -15$ V to 13.5 V	25°C	97	114		100	117		97	114		dB
		$V_{IC} = -14.9$ V to 13 V	Full range	94			97			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm2$ V to ±18 V	25°C	100	117		103	120		100	117		dB
			Full range	97			101			97			
	Channel separation	$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	120	137		123	140		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		100	400		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			5			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.5		0.35	0.55	mA
			Full range			0.7			0.55			0.6	

† Full range is −40°C to 105°C.
‡ All typical values are at $T_A = 25$°C.

electrical characteristics at specified free-air temperature, V_{CC+} = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013I			LT1013AI			LT1013DI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		90	450		60	250		250	950	µV
			Full range			570			350			1200	
I_{IO}	Input offset current		25°C		0.3	2		0.2	1.3		0.3	2	nA
			Full range			6			3.5			6	
I_{IB}	Input bias current		25°C		–18	–50		–15	–35		–18	–50	nA
			Full range			–90			–55			–90	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	–0.3 to 3.8		0 to 3.5	–0.3 to 3.8		0 to 3.5	0.3 to 3.8		V
			Full range	0 to 3			0 to 3			0 to 3			
V_{OM}	Maximum-peak output voltage swing	Output low, No load	25°C		15	25		15	25		15	25	mV
		Output low, R_L = 600 Ω to GND	25°C		5	10		5	10		5	10	
			Full range			13			13			13	
		Output low, I_{sink} = 1 mA	25°C		220	350		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		4	4.4		V
		Output high, R_L = 600 Ω to GND	25°C	3.4	4		3.4	4		3.4	4		
			Full range	3.2			3.3			3.2			
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500 Ω	25°C		1			1			1		V/µV
I_{CC}	Supply current per amplifier		25°C		0.32	0.5		0.31	0.45		0.32	0.5	mA
			Full range			0.55			0.5			0.55	

† Full range is –40°C to 105°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		µV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013M			LT1013AM			LT1013DM			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$	25°C		60	300		40	150		200	800	μV
			Full range			550			300			1000	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5	2.5*		0.4	2*		0.5	2.5*	μV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.4			0.5		μV/mo
I_{IO}	Input offset current		25°C		0.2	1.5		0.15	0.8		0.2	1.5	nA
			Full range			5			2.5			5	
I_{IB}	Input bias current		25°C		−15	−30		−12	−20		−15	−30	nA
			Full range			−45			−30			−45	
V_{ICR}	Common-mode input voltage range		25°C	−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		V
			Full range	−14.9 to 13			−14.9 to 13			−14.9 to 13			
V_{OM}	Maximum peak output voltage swing	$R_L = 2\ k\Omega$	25°C	±12.5	±14		±13	±14		±12.5	±14		V
			Full range	±11.5			±12			±11.5			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 600\ \Omega$	25°C	0.5	2		0.8	2.5		0.5	2		V/μV
		$V_O = +10$ V, $R_L = 2\ k\Omega$	25°C	1.2	7		1.5	8		1.2	7		
			Full range	0.25			0.5			0.25			
CMRR	Common-mode rejection ratio	$V_{IC} = -15$ V to 13.5 V	25°C	97	117		100	117		97	114		dB
		$V_{IC} = -14.9$ V to 13 V	Full range	94			97			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm2$ V to ±18 V	25°C	100	117		103	120		100	117		dB
			Full range	97			100			97			
	Channel separation	$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	120	137		123	140		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		100	400		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			5			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.5		0.35	0.55	mA
			Full range			0.7			0.6			0.7	

* On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.
‡ All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, $V_{CC+} = 5$ V, $V_{CC-} = 0$, $V_O = 1.4$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013M			LT1013AM			LT1013DM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$	25°C		90	450		60	250		250	950	µV
			Full range		400	1500		250	900		800	2000	
		$R_S = 50\ \Omega$, $V_{IC} = 0.1$ V	125°C		200	750		120	450		560	1200	
I_{IO}	Input offset current		25°C		0.3	2		0.2	1.3		0.3	2	nA
			Full range			10			6			10	
I_{IB}	Input bias current		25°C		−18	−50		−15	−35		−18	−50	nA
			Full range			−120			−80			−120	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		V
			Full range	0 to 3			0 to 3			0 to 3			
V_{OM}	Maximum-peak output voltage swing	Output low, No load	25°C		15	25		15	25		15	25	mV
		Output low, $R_L = 600\ \Omega$ to GND	25°C		5	10		5	10		5	10	
			Full range			18			15			18	
		Output low, $I_{sink} = 1$ mA	25°C		220	350		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		4	4.4		V/µV
		Output high, $R_L = 600\ \Omega$ to GND	25°C	3.4	4		3.4	4		3.4	4		
			Full range	3.1			3.2			3.1			
A_{VD}	Large-signal differential voltage amplification	$V_O = 5$ mV to 4 V, $R_L = 500\ \Omega$	25°C		1			1			1		mA
I_{CC}	Supply current per amplifier		25°C		0.32	0.5		0.31	0.45		0.32	0.5	
			Full range			0.65			0.55			0.65	

† Full range is −55°C to 125°C.

operating characteristics, $V_{CC\pm} = \pm15$ V, $V_{IC} = 0$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		24		$nV/\sqrt{Hz}$
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		µV
I_n	Equivalent input noise current	f = 10 Hz		0.07		$pA/\sqrt{Hz}$

electrical characteristics at V_{CC+} = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	LT1013Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω		250	950	µV
I_{IO}	Input offset current			0.3	2	nA
I_{IB}	Input bias current			−18	−50	nA
V_{ICR}	Common-mode input voltage range		0 to 3.5	0.3 to 3.8		V
V_{OM}	Maximum peak output voltage swing	Output low, No load		15	25	mV
		Output low, R_L = 600 Ω to GND		5	10	
		Output low, I_{sink} = 1 mA		220	350	
		Output high, No load	4	4.4		V
		Output high, R_L = 600 Ω to GND	3.4	4		
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500 Ω		1		V/µV
I_{CC}	Supply current per amplifier			0.32	0.5	mA

electrical characteristics at V_{CC+}= ±15 V, V_{IC} = 0, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LT1013Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω			200	800	µV
	Long-term drift of input offset voltage				0.5		µV/mo
I_{IO}	Input offset current				0.2	1.5	nA
I_{IB}	Input bias current				−15	−30	nA
V_{ICR}	Common-mode input voltage range			−15 to 13.5	−15.3 to 13.8		V
V_{OM}	Maximum peak output voltage swing	R_L = 2 kΩ		±12.5	±14		V
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 600 Ω	0.5	2		V/µV
			R_L = 2 Ω	1.2	7		dB
CMRR	Common-mode rejection ratio	V_{IC} = −15 V to 13.5 V		97	114		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{CC} /ΔV_{IO})	$V_{CC\pm}$ = ±2 V to ±18 V		100	117		dB
	Channel separation	V_O = ±10 V, R_L = 2 Ω		120	137		dB
r_{id}	Differential input resistance			70	300		MΩ
r_{ic}	Common-mode input resistance				4		GΩ
I_{CC}	Supply current per amplifier				0.35	0.55	mA

operating characteristics, $V_{CC}\pm$ = ±15 V, V_{IC} = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	LT1013Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate		0.2	0.4		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		µV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Source resistance vs Temperature	1 2
ΔV_{IO}	Change in input offset voltage	vs Time	3
I_{IO}	Input offset current	vs Temperature	4
I_{IB}	Input bias current	vs Temperature	5
V_{IC}	Common-mode input voltage	vs Input bias current	6
A_{VD}	Differential voltage amplification	vs Load resistance vs Frequency	7, 8 9, 10
	Channel separation	vs Frequency	11
	Output saturation voltage	vs Temperature	12
CMRR	Common-mode rejection ratio	vs Frequency	13
k_{SVR}	Supply voltage rejection ratio	vs Frequency	14
I_{CC}	Supply current	vs Temperature	15
I_{OS}	Short-circuit output current	vs Time	16
V_n	Equivalent input noise voltage	vs Frequency	17
I_n	Equivalent input noise current	vs Frequency	17
$V_{n(PP)}$	Peak-to-peak input noise voltage	vs Time	18
	Pulse response	Small signal Large signal	19, 21 20, 22, 23
	Phase shift	vs Frequency	9

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
vs
SUPPLY VOLTAGE

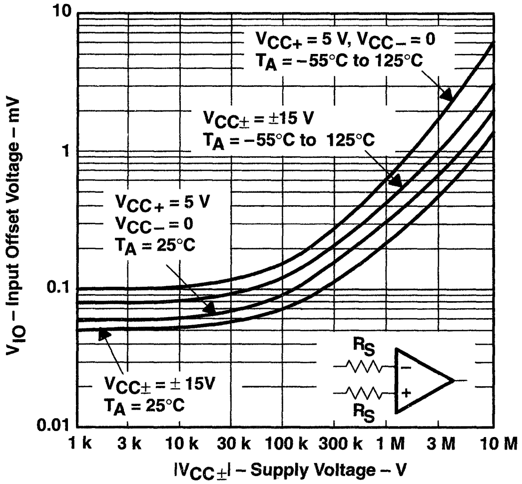


Figure 1

INPUT OFFSET VOLTAGE
OF REPRESENTITIVE UNITS
vs
FREE-AIR TEMPERATURE

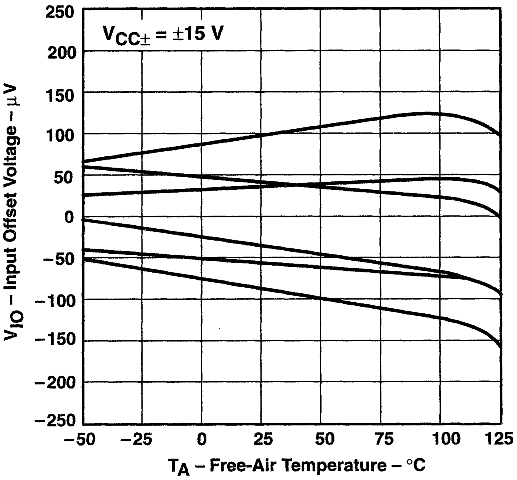


Figure 2

WARM-UP CHANGE
IN INPUT OFFSET VOLTAGE
vs
TIME AFTER POWER-ON

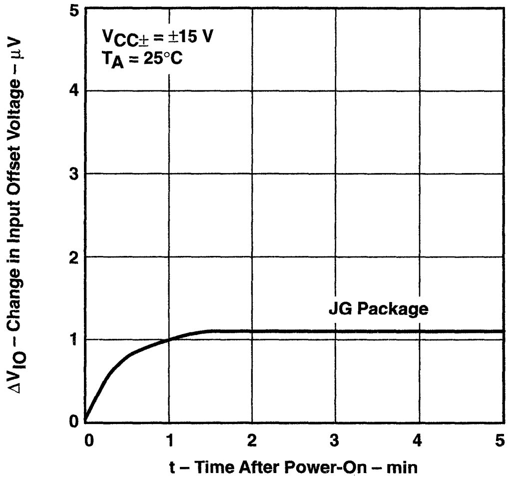


Figure 3

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

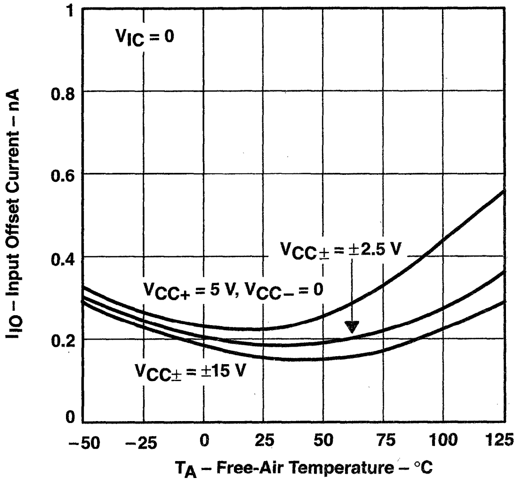


Figure 4

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

**INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE**

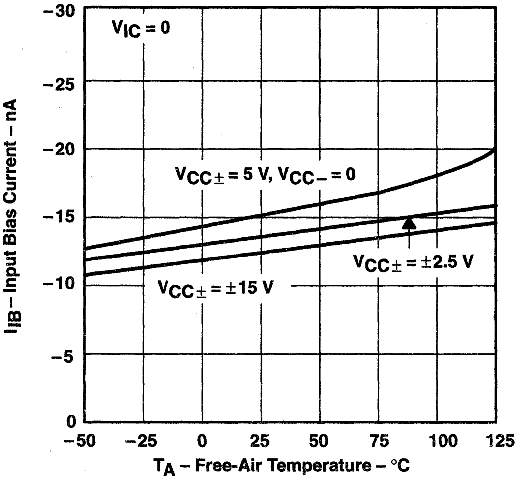

Figure 5

**COMMON-MODE INPUT VOLTAGE
vs
INPUT BIAS CURRENT**

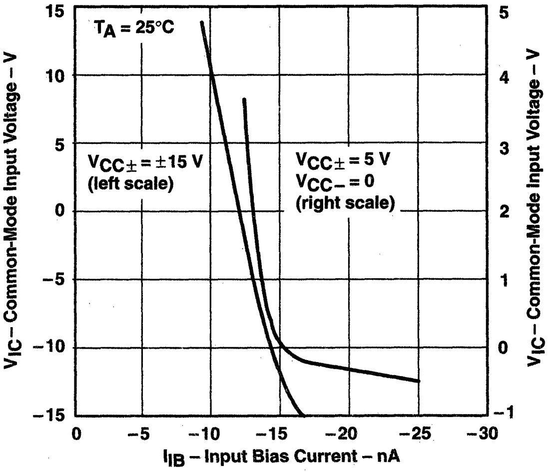

Figure 6

**DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE**

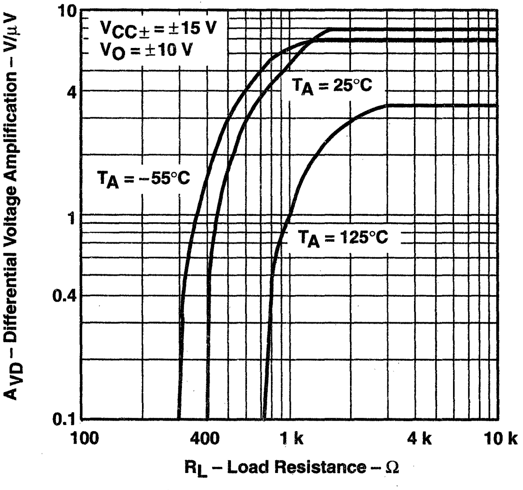

Figure 7

**DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE**

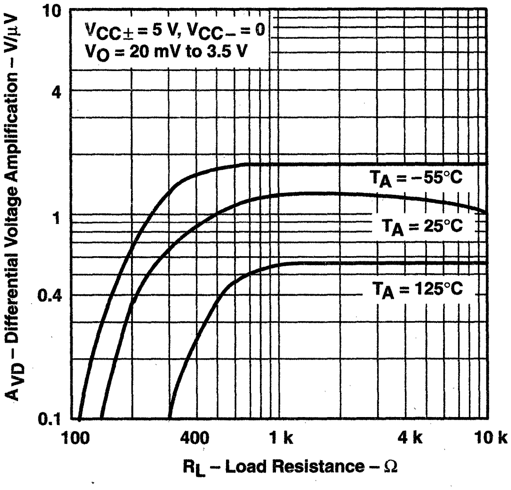

Figure 8

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

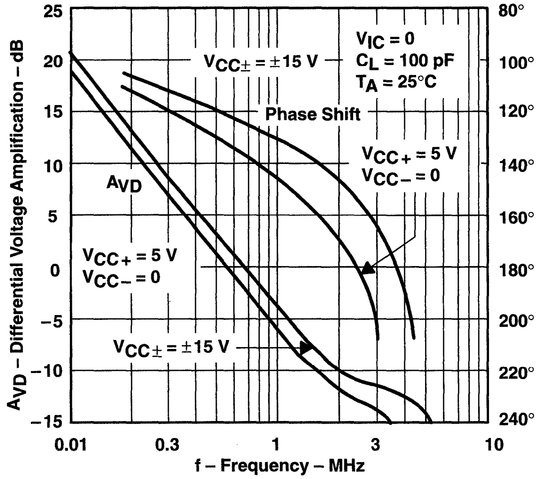

Figure 9

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

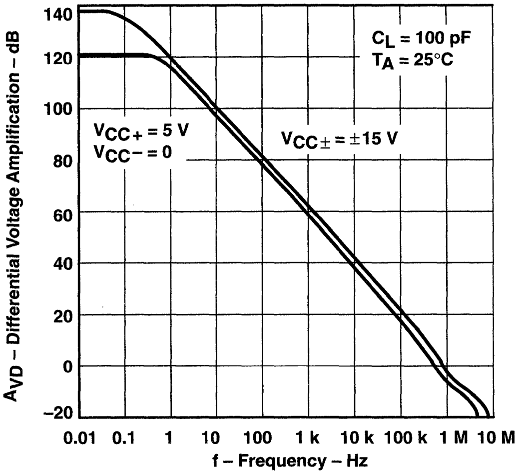

Figure 10

CHANNEL SEPARATION vs FREQUENCY

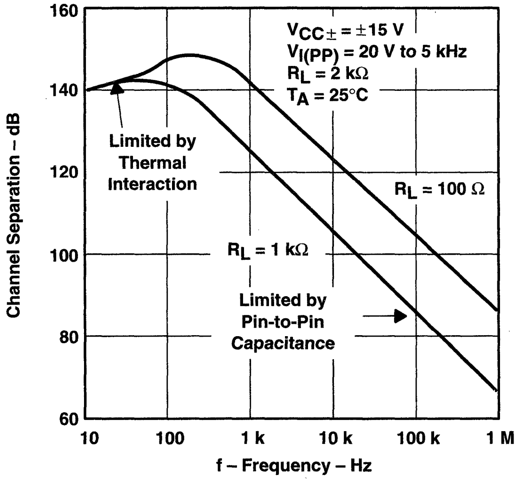

Figure 11

OUTPUT SATURATION VOLTAGE vs FREE-AIR TEMPERATURE

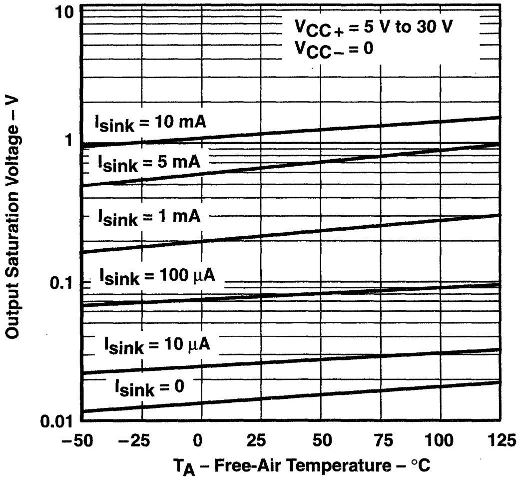

Figure 12

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

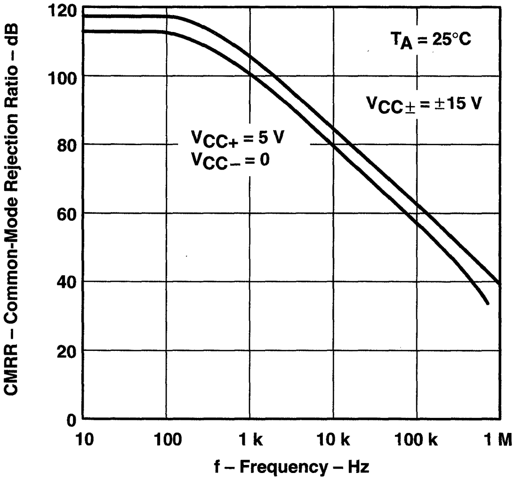

Figure 13

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

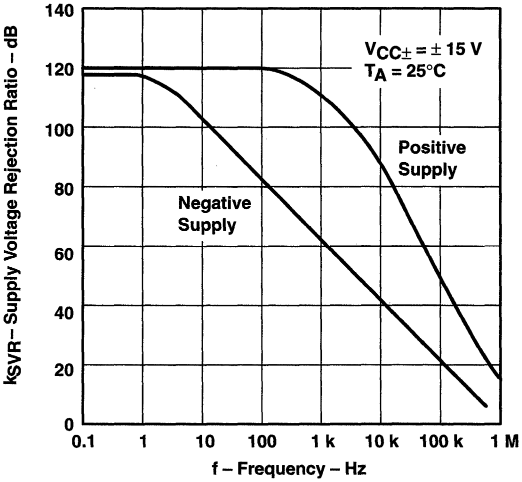

Figure 14

SUPPLY CURRENT
vs
FREQUENCY AIR TEMPERATURE

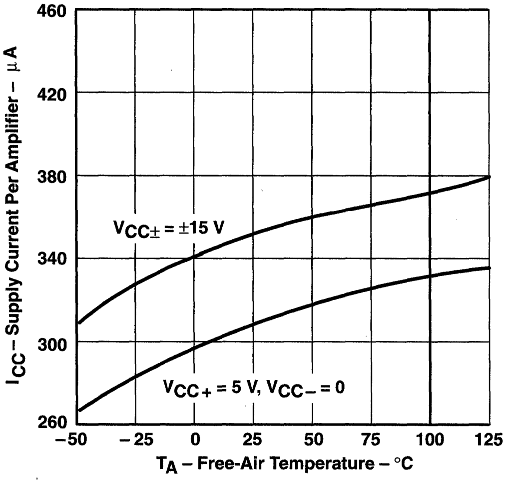

Figure 15

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

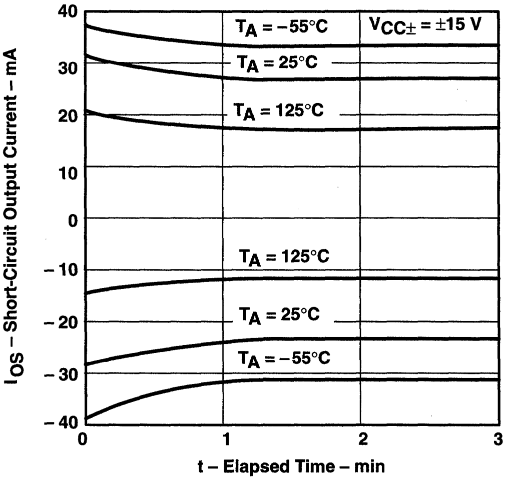

Figure 16

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE AND EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

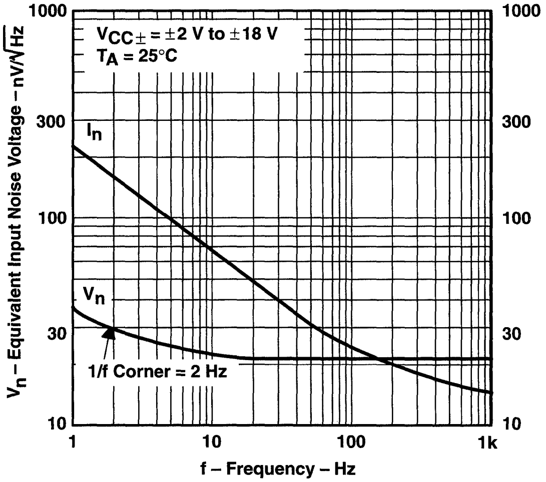


Figure 17

PEAK-TO-PEAK INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

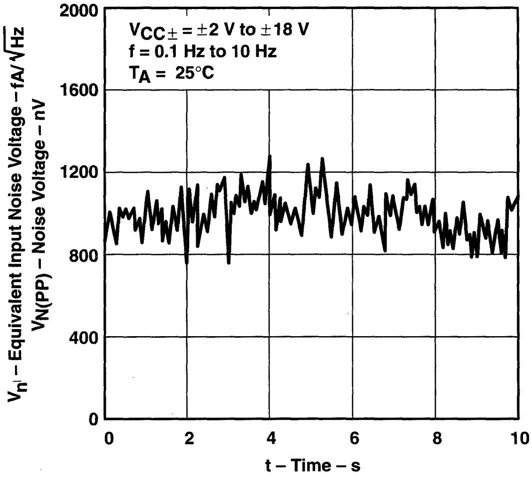


Figure 18

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

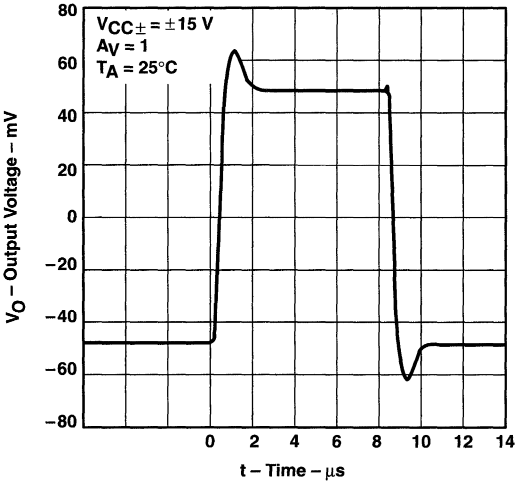


Figure 19

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE-RESPONSE

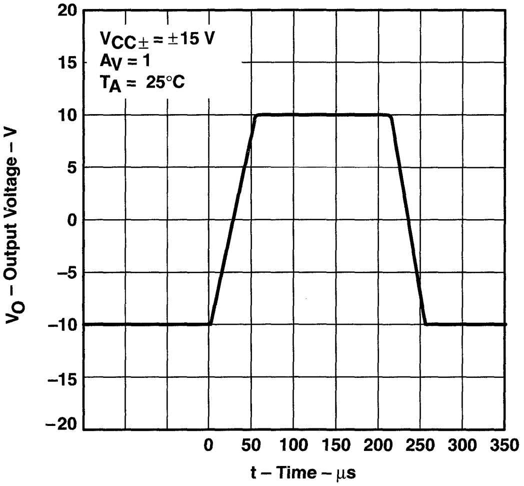


Figure 20

TYPICAL CHARACTERISTICS

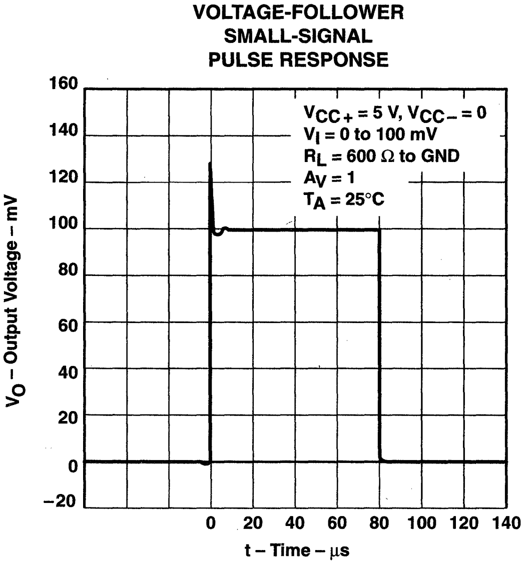


Figure 21

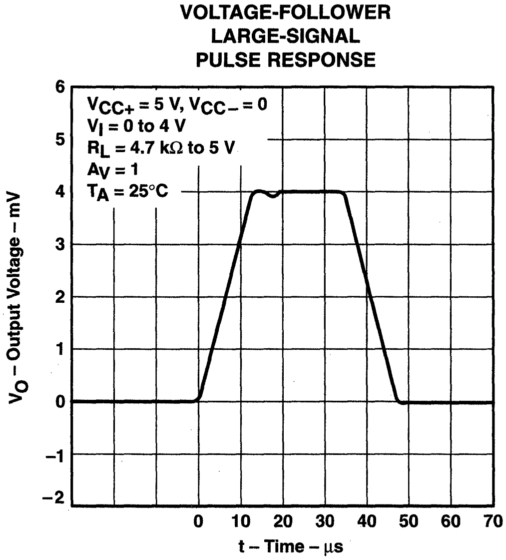


Figure 22

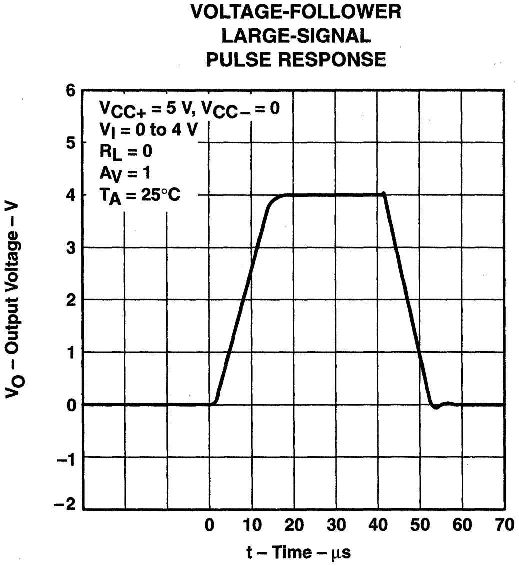


Figure 23

APPLICATION INFORMATION

single-supply operation

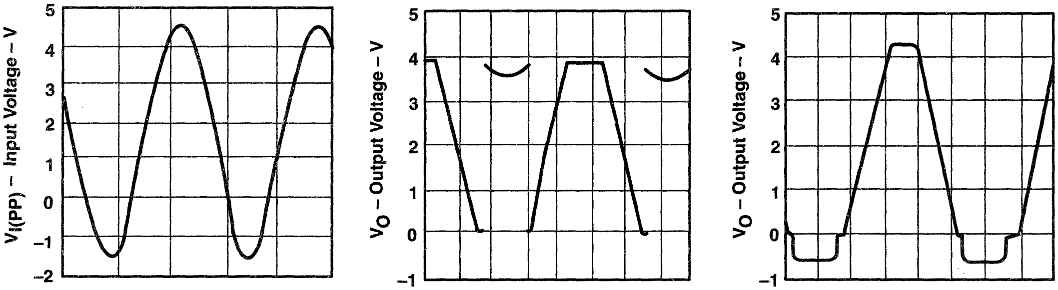
The LT1013 is fully specified for single-supply operation ($V_{CC-} = 0$). The common-mode input voltage range includes ground, and the output swings to within a few millivolts of ground.

Furthermore, the LT1013 has specific circuitry that addresses the difficulties of single-supply operation, both at the input and at the output. At the input, the driving signal can fall below 0 V, either inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, the LT1013 is designed to deal with the following two problems that can occur:

1. On many other operational amplifiers, when the input is more than a diode drop below ground, unlimited current will flow from the substrate (V_{CC-} terminal) to the input, which can destroy the unit. On the LT1013, the 400-Ω resistors in series with the input (see schematic) protect the device even when the input is 5 V below ground.
2. When the input is more than 400 mV below ground (at T_A = 25°C), the input stage of similar type operational amplifiers saturates and phase reversal occurs at the output. This can cause lock up in servo systems. Because of a unique phase-reversal protection circuitry (Q21, Q22, Q27, and Q28), the LT1013 outputs do not reverse, even when the inputs are at −1.5 V (see Figure 24).

This phase-reversal protection circuitry does not function when the other operational amplifier on the LT1013 is driven hard into negative saturation at the output. Phase-reversal protection does not work on amplifier 1 when 2's output is in negative saturation or on amplifier 2 when 1's output is in negative saturation.

At the output, other single-supply designs either cannot swing to within 600 mV of ground or cannot sink more than a few microproamperes while swinging to ground. The all-NPN output stage of the LT1013 maintains its low output resistance and high gain characteristics until the output is saturated. In dual-supply operations, the output stage is free of crossover distortion.



(a) $V_{I(PP)}$ = −1.5 V TO 4.5 V

(b) OUTPUT PHASE REVERSAL EXHIBITED BY LM358

(c) NO PHASE REVERSAL EXHIBITED BY LT1013

Figure 24. Voltage-Follower Response With Input Exceeding the Negative Common-Mode Input Voltage Range

APPLICATION INFORMATION

comparator applications

The single-supply operation of the LT1013 lends itself for use as a precision comparator with TTL-compatible output. In systems using both operational amplifiers and comparators, the LT1013 can perform multiple duties. Refer to Figures 25 and 26.

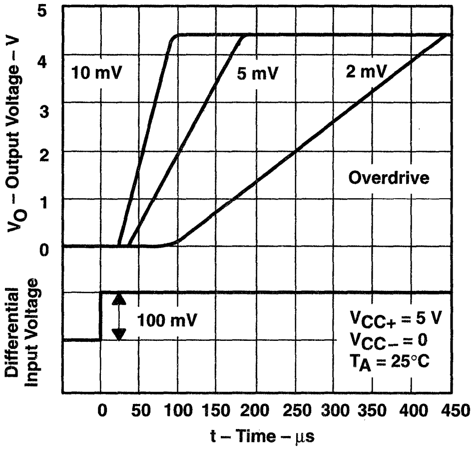


Figure 25. Low-to-High-Level Output Response for Various Input Overdrives

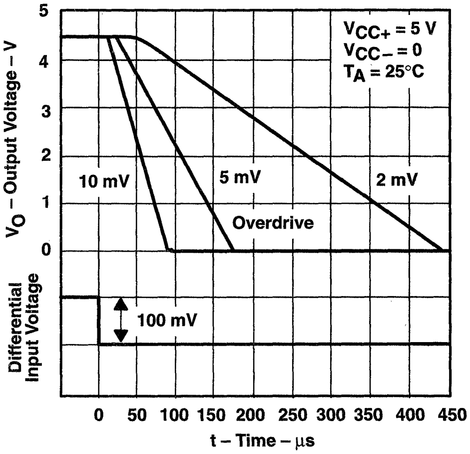


Figure 26. High-to-Low-Level Output Response for Various Input Overdrives

low-supply operation

The minimum supply voltage for proper operation of the LT1013 is 3.4 V (three Ni-Cad batteries). Typical supply current at this voltage is 290 µA; therefore, power dissipation is only 1 mW per amplifier.

offset voltage and noise testing

The test circuit for measuring input offset voltage and its temperature coefficient is shown in Figure 30. This circuit with supply voltages increased to ±20 V is also used as the burn-in configuration.

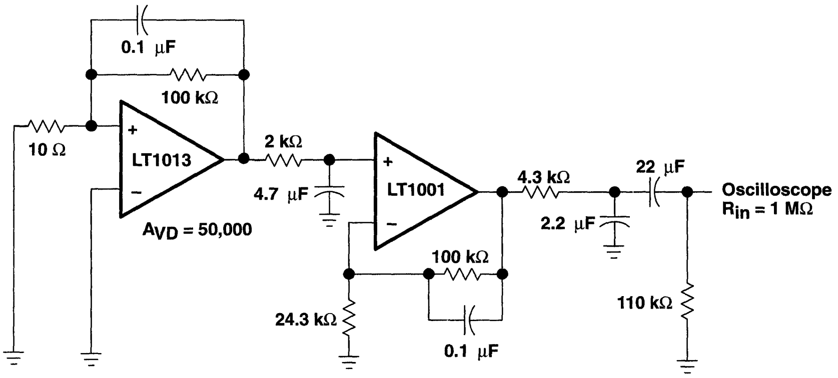
The peak-to-peak equivalent input noise voltage of the LT1013 is measured using the test circuit shown in Figure 27. The frequency response of the noise tester indicates that the 0.1-Hz corner is defined by only one zero. The test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contribution from the frequency band below 0.1 Hz.

An input noise voltage test is recommended when measuring the noise of a large number of units. A 10-Hz input noise voltage measurement correlates well with a 0.1-Hz peak-to-peak noise reading because both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured by the circuit and formula shown in Figure 28. The noise of the source resistors is subtracted.

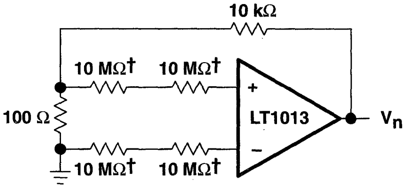
APPLICATION INFORMATION

offset voltage and noise testing (continued)



NOTE A: All capacitor values are for nonpolarized capacitors only.

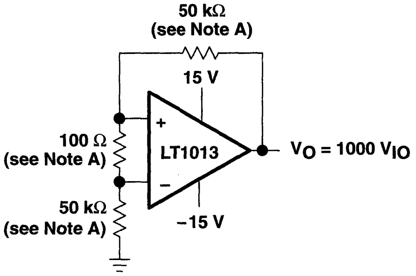
Figure 27. 0.1-Hz to 10-Hz Peak-to-Peak Noise Test Circuit



$$I_n = \frac{[V_{no}{}^2 - (820\ nV)^2]^{1/2}}{40\ M\Omega 100}$$

† Metal-film resistor

Figure 28. Noise-Current Test Circuit and Formula

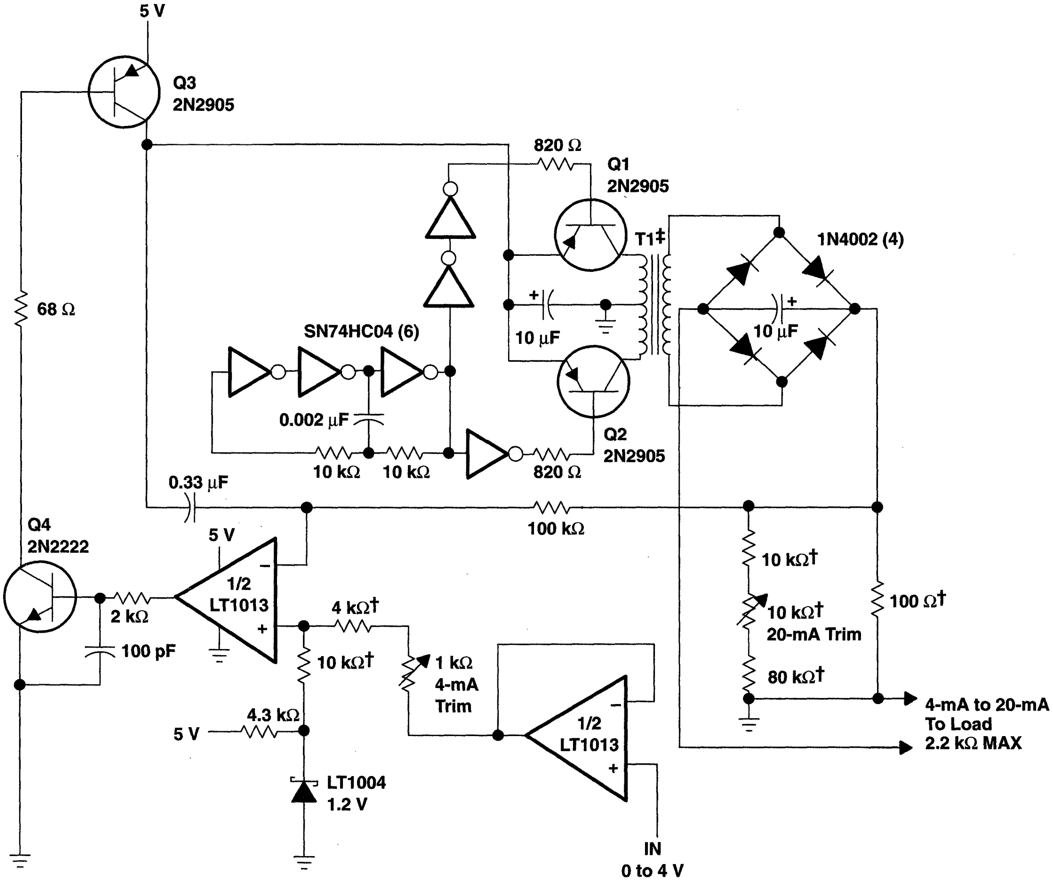


NOTE A: Resistors must have low thermoelectric potential.

Figure 29. Test Circuit for V_{IO} and αV_{IO}

APPLICATION INFORMATION

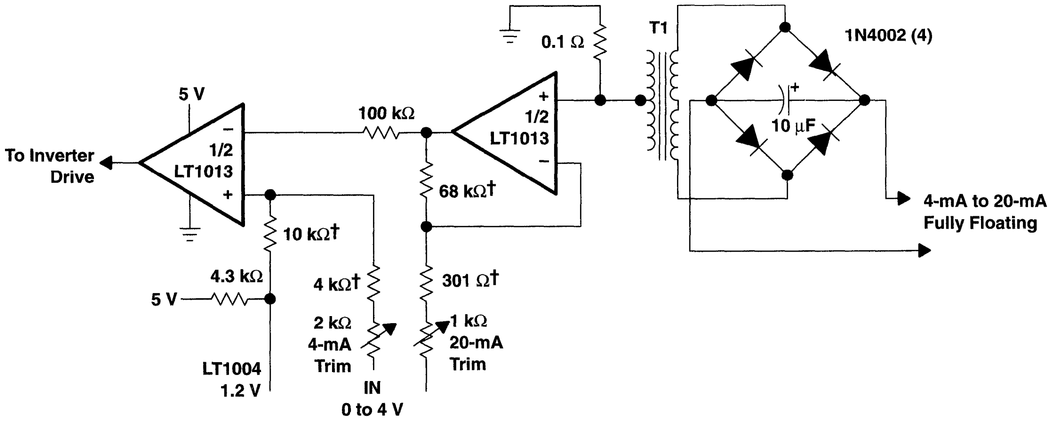
typical applications



† 1% film resistor. Match 10-kΩ resistors 0.05%.
‡ T1 = PICO-31080

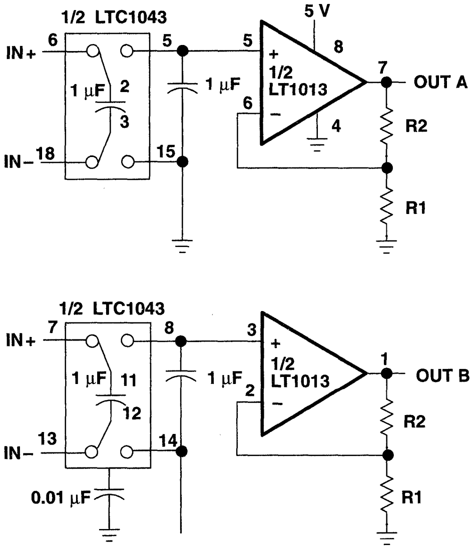
Figure 30. 5-V 4-mA – 20-mA Current Loop Transmitter With 12-Bit Accuracy

APPLICATION INFORMATION



† 1% film resistor

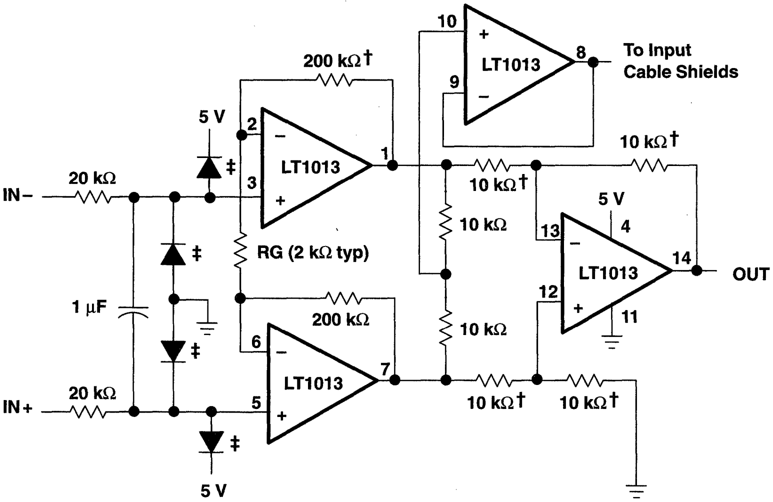
Figure 31. Fully Floating Modification to 4-mA – 20-mA Current Loop Transmitter With 8-Bit Accuracy



NOTE A: V_{IO} = 150 µV, A_{VD} = (R1/R2) + 1, CMRR = 120 dB, V_{ICR} = 0 to 5 V

Figure 32. 5-V Single-Supply Dual Instrumentation Amplifier

APPLICATION INFORMATION



† 1% film resistor. Match 10-kΩ resistors 0.05%.
‡ For high source impedances, use 2N2222 as diodes.
NOTE A: A_{VD} = (400,000/RG) + 1

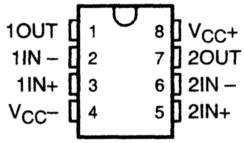
Figure 33. 5-V Precision Instrumentation Amplifier

MC1458, MC1558
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

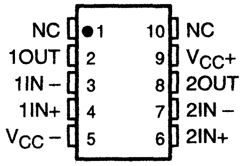
SLOS069 – FEBRUARY 1971 – REVISED OCTOBER 1990

- **Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Designed to Be Interchangeable With Motorola MC1558/MC1458 and Signetics S5558/N5558**

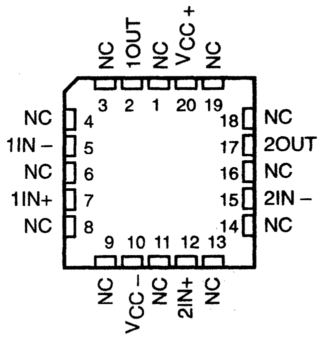
MC1458 . . . D OR P PACKAGE
MC1558 . . . JG PACKAGE
(TOP VIEW)



MC1558 . . . U PACKAGE
(TOP VIEW)



MC1558 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

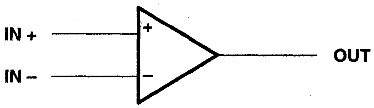
description

The MC1458 and MC1558 are dual general-purpose operational amplifiers with each half electrically similar to the µA741 except that offset null capability is not provided.

The high-common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The MC1458 is characterized for operation from 0°C to 70°C. The MC1558 is characterized for operation over the full military temperature range of –55°C to 125°C.

symbol (each amplifier)



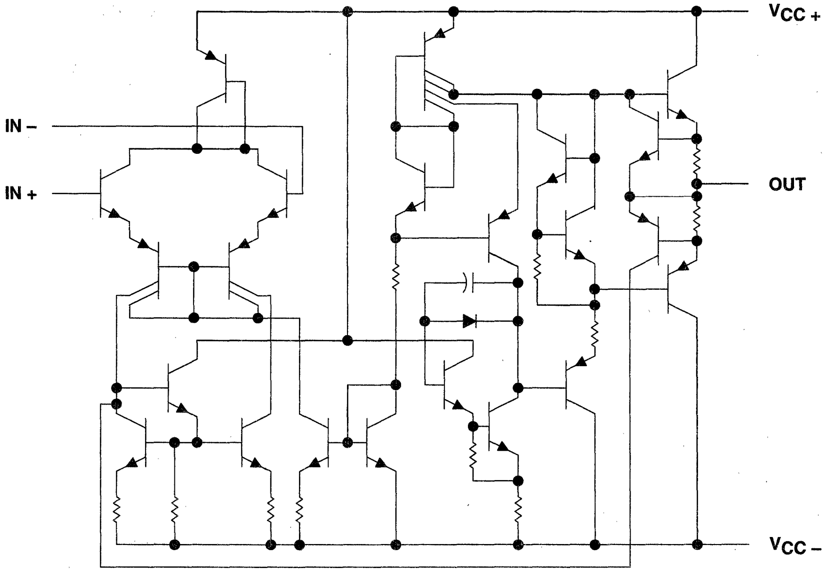
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CERAMIC FLAT PACK (U)
0°C to 70°C	6 mV	MC1458CD	—	—	MC1458CP	—
–55°C to 125°C	5 mV	—	MC1558MFK	MC1558MSG	—	MC1558MU

The D packages are available taped and reeled. Add the suffix R to the device type (i.e., MC1458DR)

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		MC1458	MC1558	UNIT
Supply voltage V_{CC+} (see Note 1)		18	22	V
Supply voltage V_{CC-} (see Note 1)		−18	−22	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage at either input (see Notes 1 and 3)		±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	−55 to 125	°C
Storage temperature range		65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260		°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output can be shorted to ground or either power supply. For the MC1558 only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 70°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	—
FK	680 mW	11.0 mW/°C	88°C	880 mW	275 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	210 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	—
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC\pm}$	±5		±15	V

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

	PARAMETER	TEST CONDITIONS†		MC1458			MC1558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	6		1	5	mV
			Full range			7.5			6	
I_{IO}	Input offset current	$V_O = 0$	25°C		20	200		20	200	nA
			Full range			300			500	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±14		±12	±14		V
		$R_L \geq 10$ kΩ	Full range	±12			±12			
		$R_L = 2$ kΩ	25°C	±10	±13		±10	±13		
		$R_L \geq 2$ kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	20	200		50	200		V/mV
			Full range	15			25			
B_{OM}	Maximum-output-swing bandwidth (closed loop)	$R_L = 2$ kΩ, $V_O \geq \pm 10$ V, $A_{VD} = 1$, THD ≥ 5%	25°C		14			14		kHz
B_1	Unity-gain bandwidth		25°C		1			1		MHz
ϕm	Phase margin	$A_{VD} = 1$	25°C		65			65		°C
	Gain margin		25°C		11			11		dB
r_i	Input resistance		25°C	0.3*	2		0.3*	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
z_{ic}	Common-mode input impedance	f = 20 Hz	25°C		200			200		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ±15 V, $V_O = 0$	25°C		30	150		30	150	µV/V
			Full range			150			150	
V_n	Equivalent input noise voltage (closed loop)	$A_{VD} = 100$, $R_S = 0$, f = 1 kHz, BW = 1 Hz	25°C		45			45		nV/√Hz

*This parameter is not production tested.

† All characteristics are specified under open-loop operating conditions with zero common-mode input voltage unless otherwise specified. Full range for MC1458 is 0°C to 70°C and for MC1558 is −55°C to 125°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effect of drift and thermal feedback.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (continued)

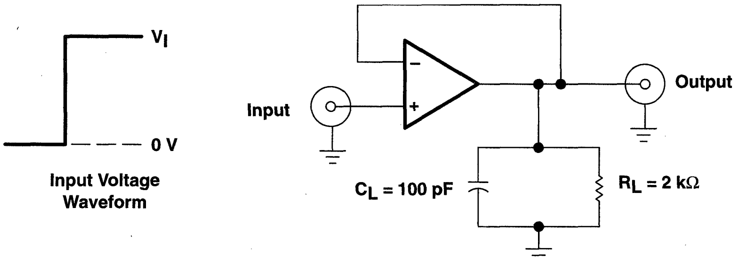
PARAMETER		TEST CONDITIONS†		MC1458			MC1558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (both amplifiers)	$V_O = 0$, No load	25°C		3.4	5.6		3.4	5	mA
			Full range			6.6			6.6	
P_D	Total power dissipation (both amplifiers)	$V_O = 0$, No load	25°C		100	170		100	150	mW
			Full range			200			200	
V_{O1}/V_{O2}	Crosstalk attenuation		25°C		120			120		dB

† All characteristics are specified under open-loop operating conditions with zero common-mode input voltage unless otherwise specified. Full range for MC1458 is 0°C to 70°C and for MC1558 is –55°C to 125°C.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MC1458			MC1558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1		0.3			0.3		μs
	Overshoot factor				5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION



Input Voltage Waveform

Test Circuit

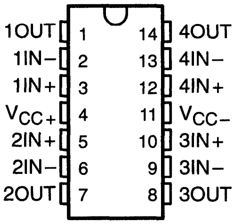
Figure 1. Rise Time, Overshoot, and Slew Rate Waveform and Test Circuit

MC3303, MC3403
QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

SLOS101 – FEBRUARY 1979 – REVISED SEPTEMBER 1990

- **Wide Range of Supply Voltages Single Supply . . . 3 V to 36 V or Dual Supplies**
- **Class AB Output Stage**
- **True Differential Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**
- **Designed to Be Interchangeable With Motorola MC3303, MC3403**

D OR N PACKAGE
(TOP VIEW)

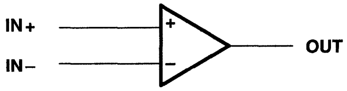


description

The MC3303 and the MC3403 are quadruple operational amplifiers similar in performance to the µA741 but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies is also possible provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to V_{CC} − 1.5 V. Quiescent supply currents are less than one-half those of the µA741.

The MC3303 is characterized for operation from −40°C to 85°C, and the MC3403 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)

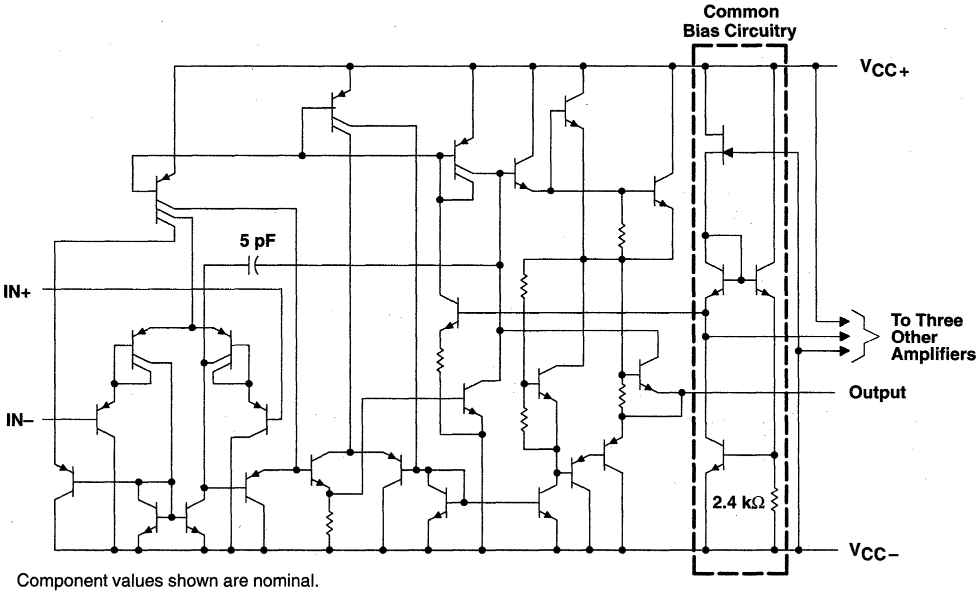


AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	10 mV	MC3403D	MC3403N
−40°C to 85°C	8 mV	MC3303D	MC3303N

The D packages are available taped and reeled. Add R suffix to the device type (e.g., MC3403DR).

schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	MC3303	MC3403	UNIT
Supply voltage V_{CC+} (see Note 1)	18	18	V
Supply voltage V_{CC-} (see Note 1)	−18	−18	V
Supply voltage V_{CC+} with respect to V_{CC-}	36	36	V
Differential input voltage (see Note 2)	±36	±36	V
Input voltage (see Notes 1 and 3)	±18	±18	V
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range	– 40 to 85	0 to 70	°C
Storage temperature range	– 65 to 150	– 65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. Neither input must ever be more positive then V_{CC+} or more negative than V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	MIN	MAX	UNIT
Single-supply voltage, V_{CC}	5	30	V
Dual-supply voltage, V_{CC+}	2.5	15	V
Dual-supply voltage, V_{CC-}	−2.5	−15	V

electrical characteristics at specified free-air temperature, V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303, $V_{CC\pm}$ = ±15 V for MC3403 (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MC3303			MC3403			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 4	25°C		2	8		2	10	mV
			Full range			10			12	
α_{VIO}	Temperature coefficient of input offset voltage	See Note 4	Full range		10			10		µV/°C
I_{IO}	Input offset current	See Note 4	25°C		30	75		30	50	nA
			Full range			250			200	
α_{IIO}	Temperture coefficient of input offset current	See Note 4	Full range		50			50		pA/C
I_{IB}	Input bias current	See Note 4	25°C		−0.2	−0.5		−0.2	−0.5	µA
			Full range			−1			−0.8	
V_{ICR}	Common-mode input voltage range‡		25°C	V_{CC-} to 12	V_{CC-} to 12.5		V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output voltage swing	R_L = 10 kΩ	25°C	12	12.5		±12	±13.5		V
		R_L = 2 kΩ	25°C	10	12		±10	±13		
		R_L = 2 kΩ	Full range	10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ	25°C	20	200		20	200		V/mV
			Full range	15			15			
B_{OM}	Maximum-output-swing bandwidth	V_{OPP} = 20 V, A_{VD} = 1, THD ≤ 5%, R_L = 2 kΩ	25°C		9			9		kHz
B_1	Unity-gain bandwidth	V_O = 50 mV, R_L = 10 kΩ	25°C		1			1		MHz
ϕ_m	Phase margin	C_L = 200 pF, R_L = 2 kΩ	25°C		60°			60°		
r_i	Input resistance	f = 20 Hz	25°C	0.3	1		0.3	1		MΩ
r_o	Output resistance	f = 20 Hz	25°C		75			75		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm}$ = ±2.5 to ±15 V	25°C		30	150		30	150	µV/V
I_{OS}	Short-circuit output current§		25°C	±10	±30	±45	±10	±30	±45	mA
I_{CC}	Total supply current	No load, See Note 4	25°C		2.8	7		2.8	7	mA

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for MC3303, and 0°C to 70°C for MC3403.

‡ The V_{ICR} limits are directly linked volt-for-volt to supply voltage; the positive limit is 2 V less than V_{CC+}.

§ Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

NOTE 4: V_{IO}, I_{IO}, I_{IB}, and I_{CC} are defined at V_O = 0 for MC3403 and V_O = 7 V for MC3303.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MC3303			MC3403			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V			10		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V			75		30	50	nA
I_{IB}	Input bias current	V_O = 2.5 V			−0.5		−0.2	−0.5	pA
V_{OM}	Peak output voltage swing‡	R_L = 10 kΩ	3.3	3.5		3.3	3.5		V
		R_L = 10 kΩ, V_{CC+} = 5 V to 30 V	V_{CC+} −1.7			V_{CC+} −1.7			
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		20	200		V/mV
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	$V_{CC\pm}$ = ± 2.5 V to ±15 V			150			150	µV/V
I_{CC}	Supply current	V_O = 2.5 V, No load		2.5	7		2.5	7	mA
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡ Output will swing essentially to ground.

operating characteristics, V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303, $V_{CC\pm}$ = ±15 V for MC3403, T_A = 25°C, A_{VD} = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V, C_L = 100 pF, R_L = 2 kΩ, See Figure 1		0.6		V/µs
t_r	Rise time	ΔV_O = 50 mV, C_L = 100 pF, R_L = 10 kΩ, See Figure 1		0.35		µs
t_f	Fall time			0.35		µs
	Overshoot factor			20%		
	Crossover distortion	$V_{I(PP)}$ = 30 mV, V_{OPP} = 2 V, f = 10 kHz		1%		

PARAMETER MEASUREMENT INFORMATION

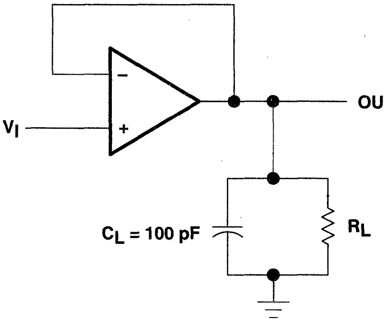


Figure 1. Unity-Gain Amplifier

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	2
		vs Supply voltage	3
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Supply voltage	4
		vs Frequency	5
A_{VD}	Large-signal differential voltage amplification	vs Frequency	6
	Large-signal pulse response	vs Time	7

INPUT BIAS CURRENT†
vs
FREE-AIR TEMPERATURE

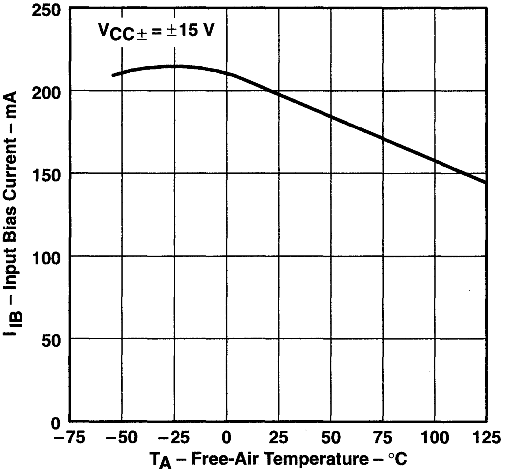


Figure 2

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

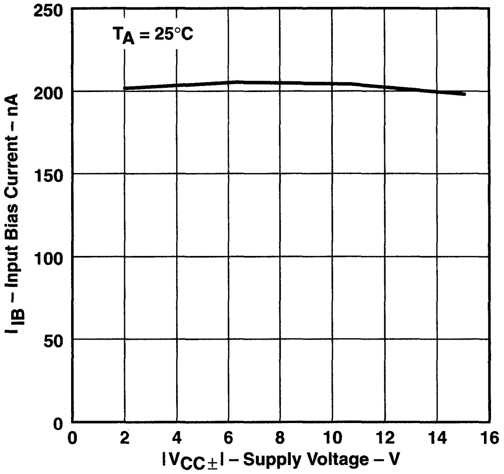


Figure 3

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

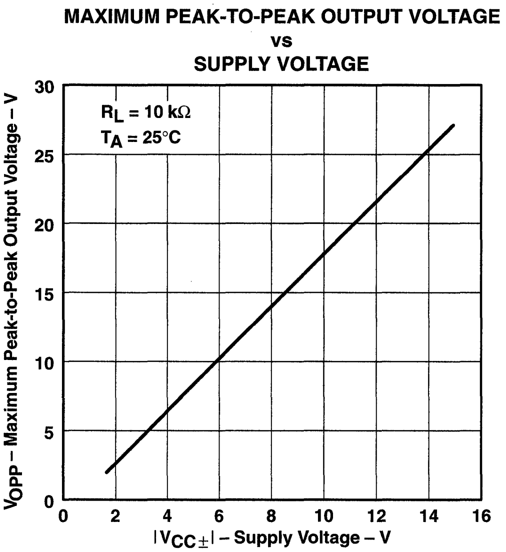


Figure 4

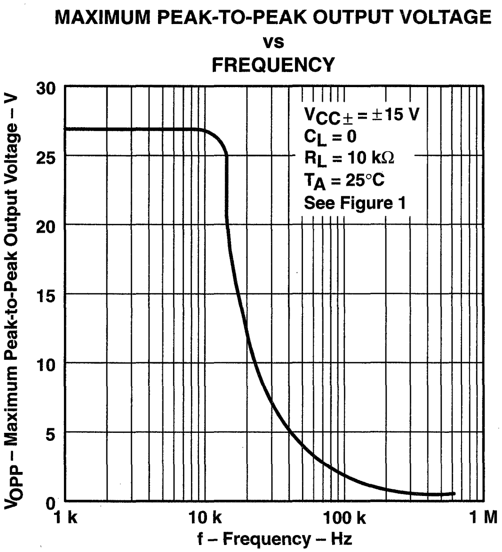


Figure 5

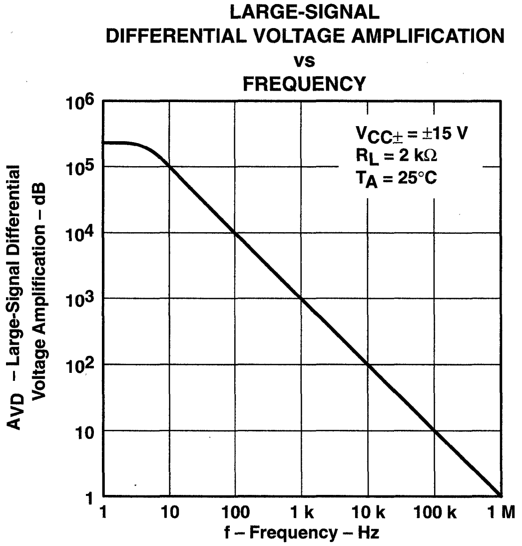


Figure 6

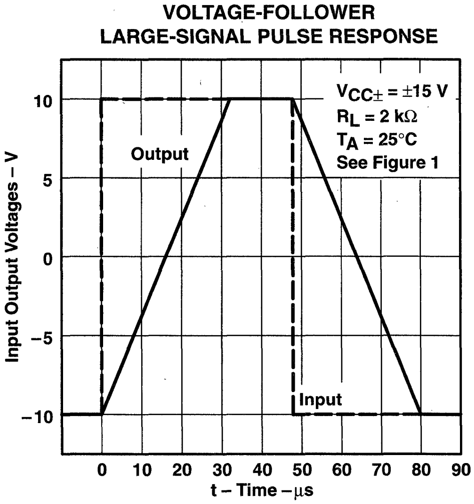


Figure 7

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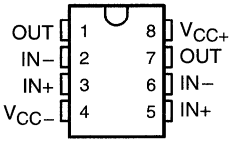
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NE5532, NE5532A, NE5532I, NE5532AI
DUAL LOW-NOISE OPERATIONAL AMPLIFIERS

SLOS075A – NOVEMBER 1979 – REVISED SEPTEMBER 1990

- **Equivalent Input Noise Voltage**
  5 nv/√Hz Typ at 1 kHz
- **Unity-Gain Bandwidth . . . 10 MHz Typ**
- **Common-Mode Rejection Ratio**
  100 dB Typ
- **High DC Voltage Gain . . . 100 V/mV Typ**
- **Peak-to-Peak Output Voltage Swing**
  32 V Typ With $V_{CC\pm} = \pm 18$ V and
  $R_L = 600\ \Omega$
- **High Slew Rate . . . 9 V/μs Typ**
- **Wide Supply Voltage Range . . . ±3 V to ±20 V**
- **Designed to Be Interchangeable With Signetics NE5532 and NE5532A**

P PACKAGE
(TOP VIEW)

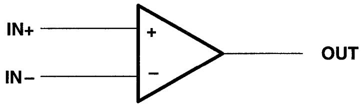


description

The NE5532 and NE5532A are monolithic high-performance operational amplifiers combining excellent dc and ac characteristics. They feature very low noise, high output drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are internally compensated for unity-gain operation. The NE5532A has specified maximum limits for equivalent input noise voltage.

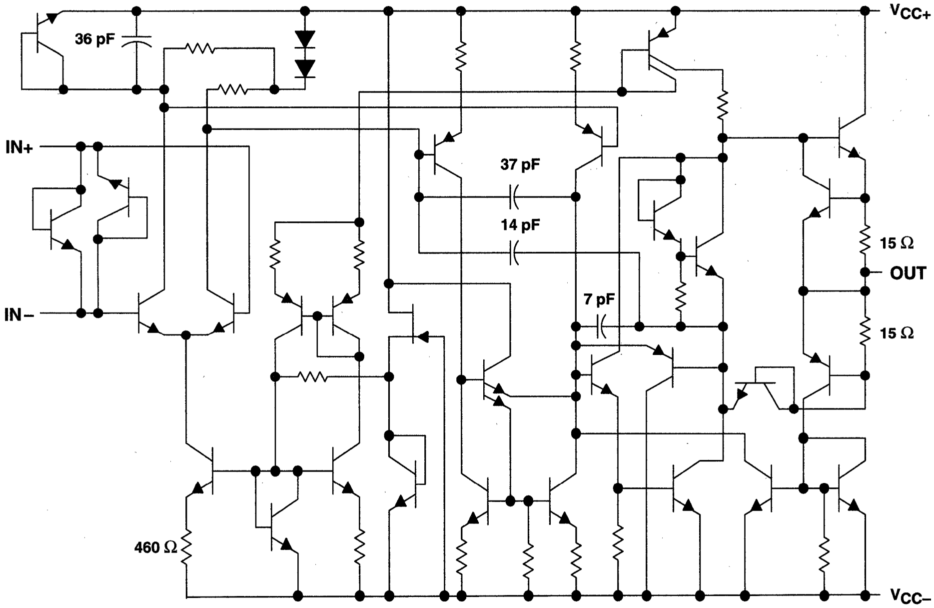
The NE5532 and NE5532A are characterized for operation from 0°C to 70°C. The NE5532I and NE5532AI are characterized for operation from −40°C to 85°C.

symbol (each amplifier)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Input voltage, either input (see Notes 1 and 2)	$V_{CC\pm}$
Input current (see Note 3)	±10 mA
Duration of output short circuit (see Note 4)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range: NE5532, NE5532A	0°C to 70°C
NE5532I, NE5532AI	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
P	1000 mW	8 mW/°C	640 mW	520 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	5		15	V
Supply voltage, V_{CC-}	−5		−15	V

electrical characteristics, $V_{CC\pm}$ = +15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	T_A = 25°C		0.5	4	mV
			T_A = Full range			5	
I_{IO}	Input offset current	T_A = 25°C			10	150	nA
		T_A = Full range				200	
I_{IB}	Input bias current	T_A = 25°C			200	800	nA
		T_A = Full range				1000	
V_{ICR}	Common-mode input voltage range			±12	±13		V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L ≥ 600 Ω	$V_{CC\pm}$ = ±15 V	24	26		V
			$V_{CC\pm}$ = ±18 V	30	32		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 600 Ω, V_O = ±10 V	T_A = 25°C	15	50		V/mV
			T_A = Full range	10			
		R_L ≥ 2 kΩ, V_O = ±10 V	T_A = 25°C	25	100		
			T_A = Full range	15			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz			2.2		V/mV
B_{OM}	Maximum-output-swing bandwidth	R_L = 600 Ω	V_O = ±10 V		140		kHz
			$V_{CC\pm}$ = ±18 V, V_O = ±14 V		100		
B_1	Unity-gain bandwidth	R_L = 600 Ω, C_L = 100 pF			10		MHz
r_i	Input resistance			30	300		kΩ
z_o	Output impedance	A_{VD} = 30 dB, R_L = 600 Ω, f = 10 kHz			0.3		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		80	100		dB
I_{OS}	Output short-circuit current				38		mA
I_{CC}	Total supply curent	V_O = 0, No load			8	16	mA
	Crosstalk attenuation (V_{O1}/V_{O2})	V_{01} = 10 V peak, f = 1 kHz			110		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for NE5532/NE5532A and −40°C to 85°C for NE5532I/NE5532AI.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	NE5532/NE5532I			NE5532A/NE5532AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain			9			9		V/µs
	Overshoot factor	V_I = 100 mV, A_{VD} = 1, R_L = 600 Ω, C_L = 100 pF		10%			10%		
V_n	Equivalent input noise voltage	f = 30 Hz		8			8	10	nV/√Hz
		f = 1 kHz		5			5	6	
I_n	Equivalent input noise current	f = 30 Hz		2.7			2.7		pA/√Hz
		f = 1 kHz		0.7			0.7		

NE5534, NE5534A, SE5534, SE5534A
LOW-NOISE OPERATIONAL AMPLIFIERS

SLOS070 – JULY 1979 – REVISED SEPTEMBER 1990

- **Equivalent Input Noise Voltage 3.5 nV/√Hz**
- **Unity-Gain Bandwidth . . . 10 MHz Typ**
- **Common-Mode Rejection Ratio 100 dB Typ**
- **High DC Voltage Gain . . . 100 V/mV Typ**
- **Peak-to-Peak Output Voltage Swing 32 V Typ With $V_{CC\pm} = \pm 18$ V and $R_L = 600\ \Omega$**
- **High Slew Rate . . . 13 V/μs Typ**
- **Wide Supply Voltage Range ±3 V to ±20 V**
- **Low Harmonic Distortion**
- **Designed to Be Interchangeable With Signetics NE5534, NE5534A, SE5534, and SE5534A**

description

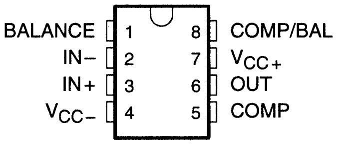
The NE5534, NE5534A, SE5534, and SE5534A are monolithic high-performance operational amplifiers combining excellent dc and ac characteristics. Some of the features include very low noise, high output drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, and high slew rate.

These operational amplifiers are internally compensated for a gain equal to or greater than three. Optimization of the frequency response for various applications can be obtained by use of an external compensation capacitor between COMP and COMP/BAL. The devices feature input-protection diodes, output short-circuit protection, and offset-voltage nulling capability.

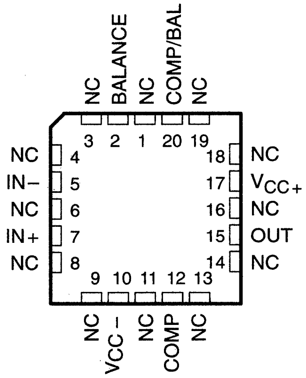
For the NE5534A, a maximum limit is specified for equivalent input noise voltage.

The NE5534 and NE5534A are characterized for operation from 0°C to 70°C. The SE5534 and SE5534A are characterized for operation over the full military temperature range of – 55°C to 125°C.

NE5534, NE5534A . . . D OR P PACKAGE
SE5534, SE5534A . . . JG PACKAGE
(TOP VIEW)

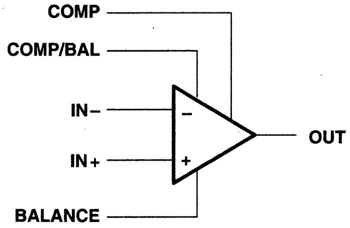


SE5534, SE5534A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

symbol



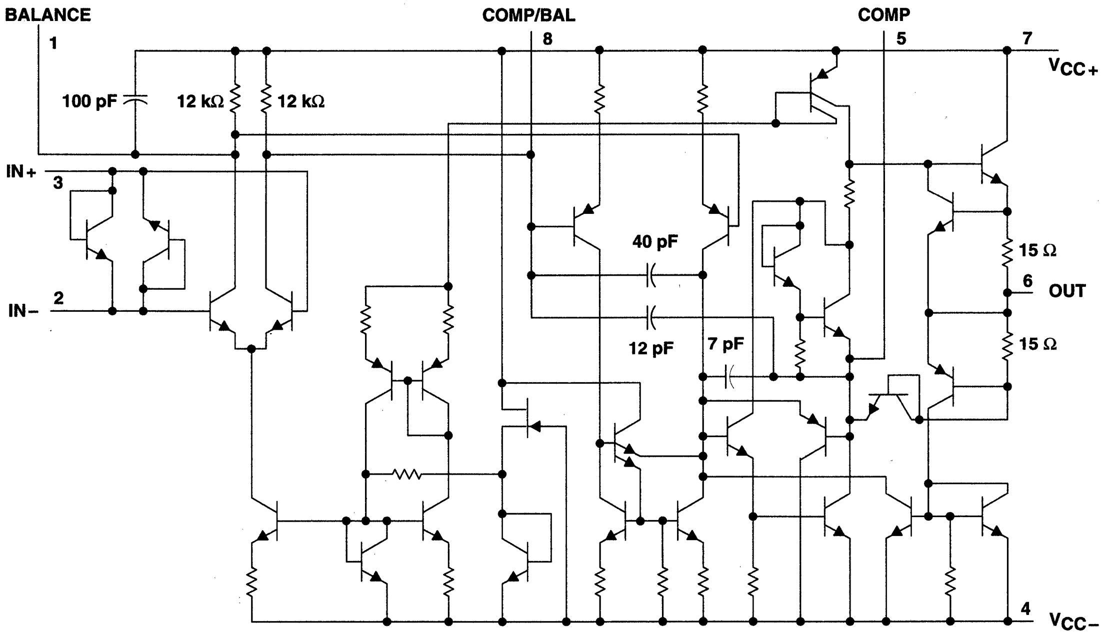
SE5534A FROM TI NOT RECOMMENDED FOR NEW DESIGNS

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	4 mV	NE5534D NE5534AD	— —	— —	NE5534P NE5534AP
– 55°C to 125°C	2 mV	— —	SE5534FK SE5534AFK	SE5534JG SE5534AJG	— —

The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE5534DR).

schematic



All component values shown are nominal.
Pin numbers shown are for D, JG, and P packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)		22 V
Supply voltage, V_{CC-} (see Note 1)		− 22 V
Input voltage either input (see Notes 1 and 2)		V_{CC+}
Input current (see Note 3)		±10 mA
Duration of output short circuit (see Note 4)		unlimited
Continuous total power dissipation		See Dissipation Rating Table
Operating free-air temperature range:	NE5534, NE5534A	0°C to 70°C
	SE5534, SE5534A	− 55°C to 125°C
Storage temperature range		− 65°C to 150°C
Case temperature for 60 seconds: FK package		260°C
Lead temperature range 1,6 mm (1/16 inch) from case for 60 seconds: JG package		300°C
Lead temperature range 1,6 mm (1/16 inch) from case for 10 seconds: D or P package		260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or to either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	N/A
FK (see Note 5)	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	N/A

NOTE 5: For the FK package, power rating and derating factor will vary with actual mounting technique used. The values stated here are believed to be conservative.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	5		15	V
Supply voltage, V_{CC-}	– 5		– 15	V

electrical characteristics, $V_{CC}\pm = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		NE5534, NE5534A			SE5534, SE5534A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		0.5	4		0.5	2	mV
			T_A = Full range			5			3	
I_{IO}	Input offset current	$V_O = 0$	$T_A = 25°C$		20	300		10	200	nA
			T_A = Full range			400			500	
I_{IB}	Input bias current	$V_O = 0$	$T_A = 25°C$		500	1500		400	800	nA
			T_A = Full range			2000			1500	
V_{ICR}	Common-mode input voltage range			±12	±13		±12	±13		V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	$R_L \ge 600\ \Omega$	$V_{CC\pm} = \pm 15$ V	24	26		24	26		V
			$V_{CC\pm} = \pm 18$ V	30	32		30	32		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \ge 600\ \Omega$	$T_A = 25°C$	25	100		50	100		V/mV
			T_A = Full range	15			25			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz	$C_C = 0$		6			6		V/mV
			$C_C = 22$ pF		2.2			2.2		
B_{OM}	Maximum-output-swing bandwidth	$V_O = \pm 10$ V,	$C_C = 0$		200			200		kHz
		$V_O = \pm 10$ V,	$C_C = 22$ pF		95			95		
		$V_{CC\pm} = \pm 18$ V, $R_L \ge 600\ \Omega$,	$V_O = \pm 14$ V, $C_C = 22$ pF		70			70		
B_1	Unity-gain bandwidth	$C_C = 22$ pF,	$C_L = 100$ pF		10			10		MHz
r_i	Input resistance			30	100		50	100		kΩ
z_o	Output impedance	$A_{VD} = 30$ dB, $C_C = 22$ pF,	$R_L \ge 600\ \Omega$, f = 10 kHz		0.3			0.3		Ω
CMRR	Common-mode rejection ratio	$V_O = 0$, $R_S = 50\ \Omega$	$V_{IC} = V_{ICR}$min,	70	100		80	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC+} = \pm 9$ V to ± 15 V, $V_O = 0$,	$R_S = 50\ \Omega$	80	100		86	100		dB
I_{OS}	Output short-circuit current				38			38		mA
I_{CC}	Supply current	$V_O = 0$, No load	$T_A = 25°C$		4	8		4	6.5	mA
			T_A = Full range						9	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is T_A = 0°C to 70°C for NE5534 and NE5534A and – 55°C to 125°C for SE5534 and SE5534A.

operating characteristics, $V_{CC}\pm = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	SE5534, NE5534			SE5534A, NE5534A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$C_C = 0$		13			13		V/µs
		$C_C = 22$ pF		6			6		
t_r	Rise time	$V_I = 50$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_C = 22$ pF, $C_L = 100$ pF		20			20		ns
	Overshoot factor			20%			20%		
t_r	Rise time	$V_I = 50$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_C = 47$ pF, $C_L = 500$ pF		50			50		ns
	Overshoot factor			35%			35%		
V_n	Equivalent input noise voltage	f = 30 Hz		7			5.5	7	nV/√Hz
		f = 1 kHz		4			3.5	4.5	
I_n	Equivalent input noise current	f = 30 Hz		2.5			1.5		pA/√Hz
		f = 1 kHz		0.6			0.4		
$\overline{F}$	Average noise figure	$R_S = 5$ kΩ, f = 10 Hz to 20 kHz					0.9		dB

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

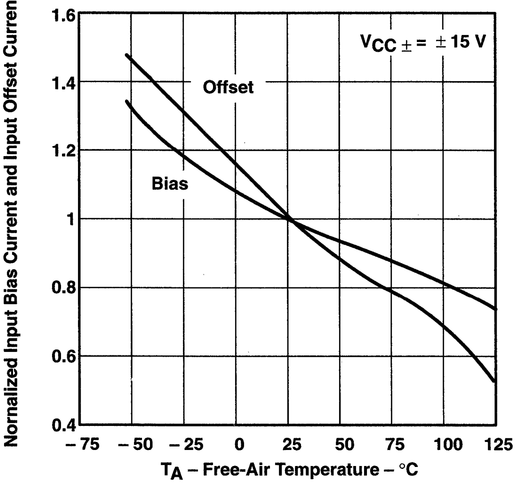


Figure 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

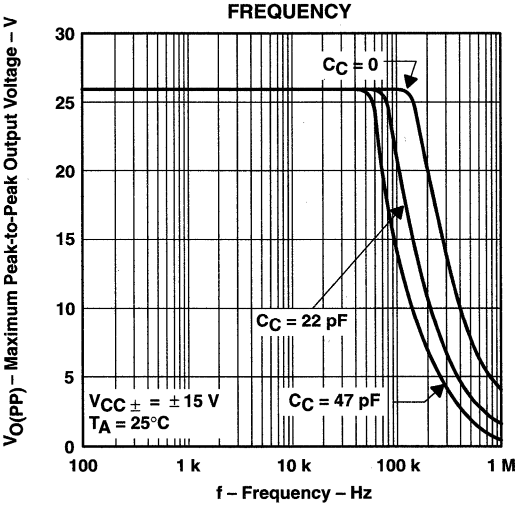


Figure 2

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

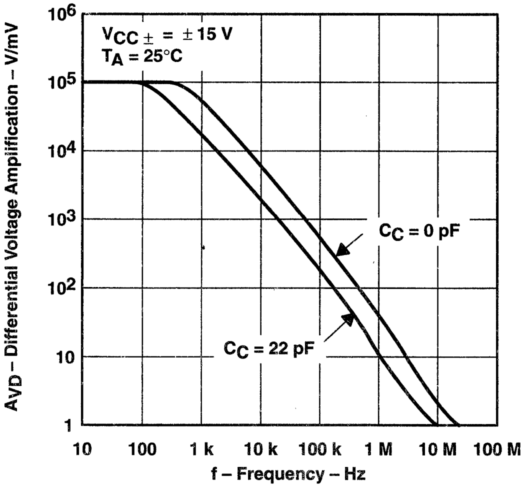

Figure 3

NORMALIZED SLEW RATE AND UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

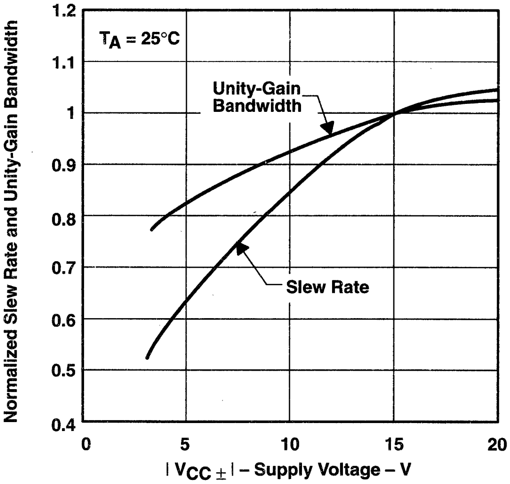

Figure 4

NORMALIZED SLEW RATE AND UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

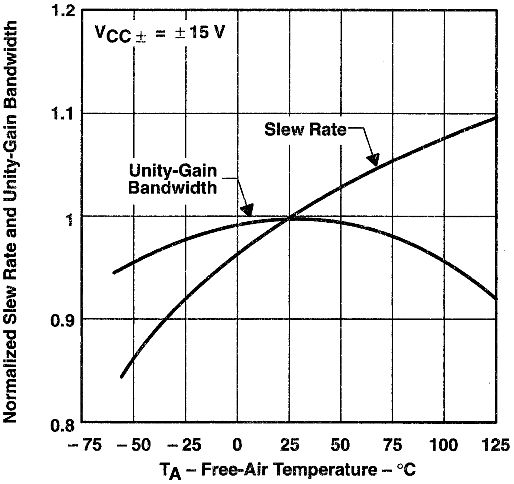

Figure 5

TOTAL HARMONIC DISTORTION vs FREQUENCY

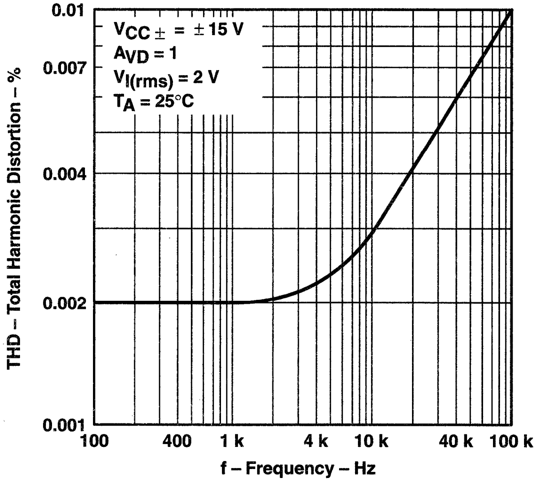

Figure 6

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

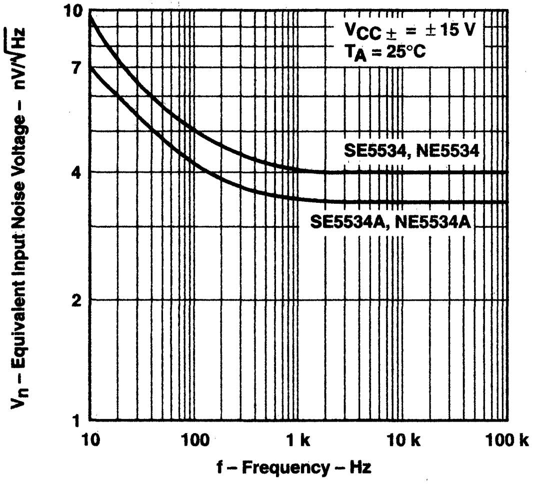


Figure 7

EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

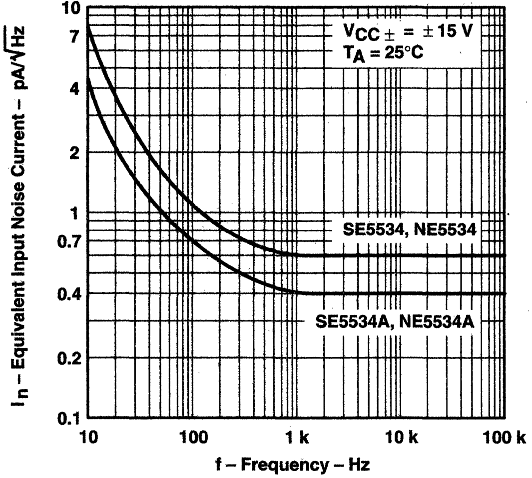


Figure 8

TOTAL EQUIVALENT INPUT NOISE VOLTAGE vs SOURCE RESISTANCE

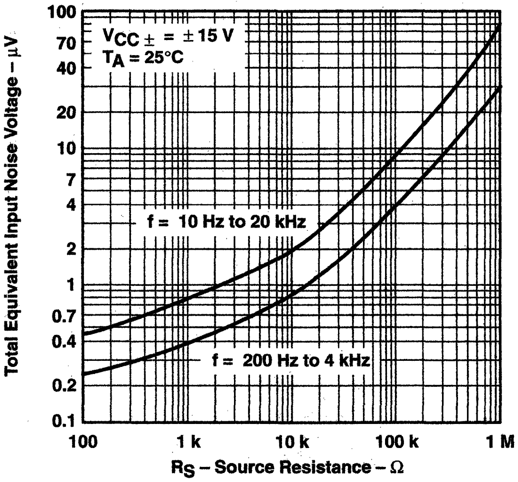


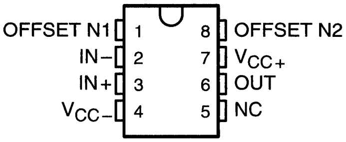
Figure 9

OP07C, OP07D, OP07Y
PRECISION OPERATIONAL AMPLIFIERS

SLOS099B – OCTOBER 1983 – REVISED AUGUST 1996

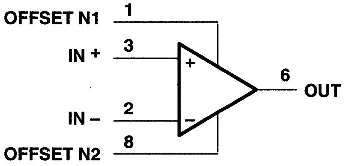
- **Low Noise**
- **No External Components Required**
- **Replaces Chopper Amplifiers at a Lower Cost**
- **Single-Chip Monolithic Fabrication**
- **Wide Input Voltage Range**
  0 to ±14 V Typ
- **Wide Supply Voltage Range**
  ±3 V to ±18 V
- **Essentially Equivalent to Fairchild μA714 Operational Amplifiers**
- **Direct Replacement for PMI OP07C and OP07D**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

symbol



description

These devices represent a breakthrough in operational amplifier performance. Low offset and long-term stability are achieved by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP07 is unsurpassed for low-noise, high-accuracy amplification of very low-level signals.

These devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

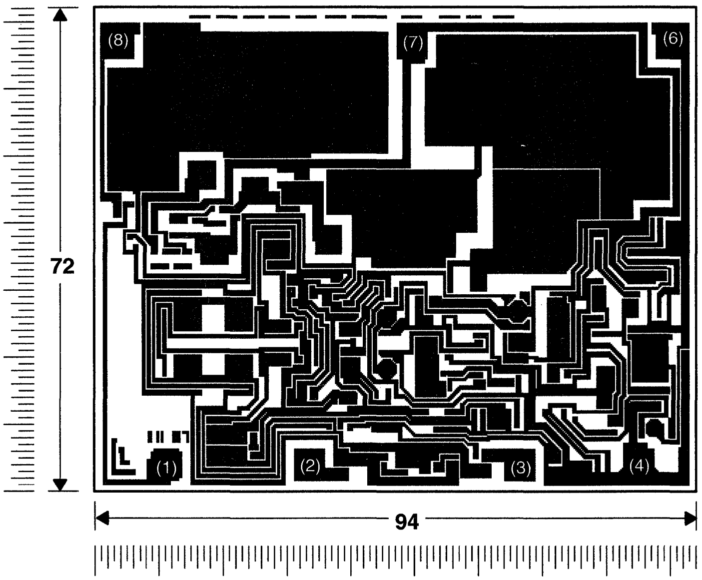
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	150 μV	OP07CD OP07DD	OP07CP OP07DP	OP07Y

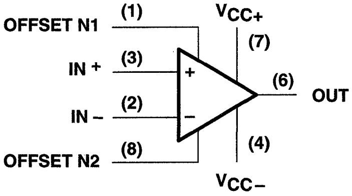
The D package is available taped and reeled. Add the suffix R to the device type (e.g., OP07CDR). The chip form is tested at T_A = 25°C.

OP07Y chip information

These chips, properly assembled, display characteristics similar to the OP07. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

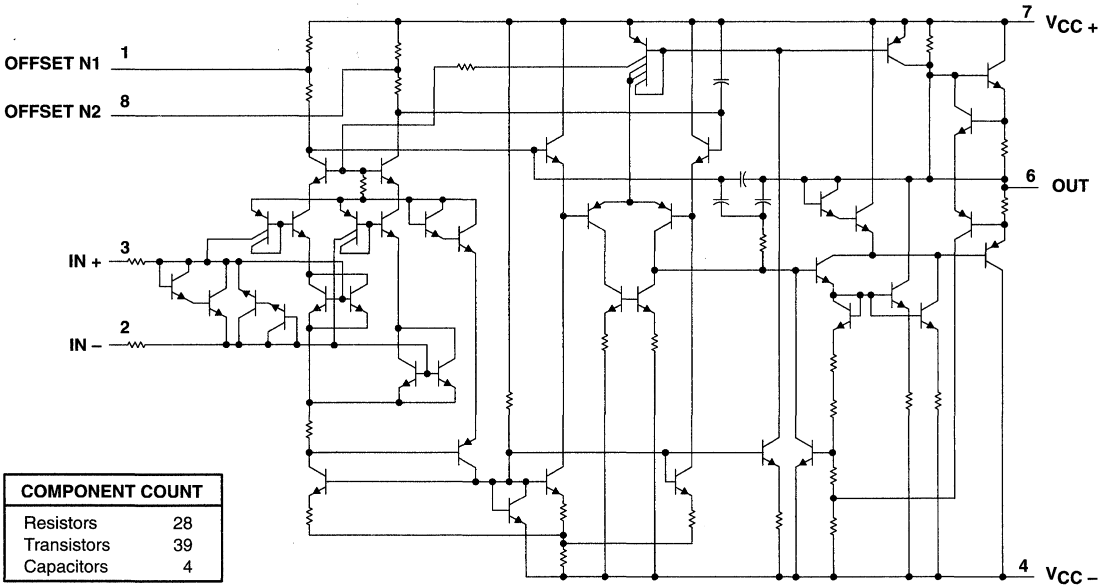
$T_J$max = 150°C

TOLERANCES ARE ± 10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

schematic



COMPONENT COUNT	
Resistors	28
Transistors	39
Capacitors	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	–22 V
Differential input voltage (see Note 2)	±30 V
Input voltage, V_I (either input, see Note 3)	±22 V
Duration of output short circuit (see Note 4)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	500 mW
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation above 64°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±3	±18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 15$ V	–13	13	V
Operating free-air temperature, T_A		0	70	°C

electrical characteristics at specified free-air temperature, $V_{CC}\pm = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	OP07C MIN	OP07C TYP	OP07C MAX	OP07D MIN	OP07D TYP	OP07D MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		60	150		60	150	µV
			0°C to 70°C		85	250		85	250	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	0°C to 70°C		0.5	1.8		0.7	2.5	µV/°C
	Long-term drift of input offset voltage	See Note 6			0.4			0.5		µV/mo
	Offset adjustment range	$R_S = 20$ kΩ, See Figure 1	25°C		±4			±4		mV
I_{IO}	Input offset current		25°C		0.8	6		0.8	6	nA
			0°C to 70°C		1.6	8		1.6	8	
α_{IIO}	Temperature coefficient of input offset current		0°C to 70°C		12	50		12	50	pA/°C
I_{IB}	Input bias current		25°C		±1.8	±7		±2	±12	nA
			0°C to 70°C		±2.2	±9		±3	±14	
α_{IIB}	Temperature coefficient of input bias current		0°C to 70°C		18	50		18	50	pA/°C
V_{ICR}	Common-mode input voltge range		25°C	±13	±14		±13	±14		V
			0°C to 70°C	±13	±13.5		±13	±13.5		
V_{OM}	Peak output voltage	$R_L \geq 10$ kΩ	25°C	±12	±13		±12	±13		V
		$R_L \geq 2$ kΩ		±11.5	±12.8		±11.5	±12.8		
		$R_L \geq 1$ kΩ			±12			±12		
		$R_L \geq 2$ kΩ	0°C to 70°C	±11	±12.6		±11	±12.6		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm3$ V, $V_O = \pm0.5$ V, $R_L \geq 500$ kΩ	25°C	100	400			400		V/mV
		$V_O = \pm10$ V, $R_L = 2$ kΩ	25°C	120	400		120	400		
			0°C to 70°C	100	400		100	400		
B_1	Unity-gain bandwidth		25°C	0.4	0.6		0.4	0.6		MHz
r_i	Input resistance		25°C	8	33		7	31		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = \pm13$ V, $R_S = 50\ \Omega$	25°C	100	120		94	110		dB
			0°C to 70°C	97	120		94	106		
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm} = \pm3$ V to ±18 V, $R_S = 50\ \Omega$	25°C		7	32		7	32	µV/V
			0°C to 70°C		10	51		10	51	
P_D	Power dissipation	$V_O = 0$, No load	25°C		80	150		80	150	mW
		$V_{CC\pm} = \pm3$ V, $V_O = 0$, No load			4	8		4	8	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS†	OP07C			OP07D			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_n	Equivalent input noise voltage	f = 10 Hz		10.5			10.5		nV/√Hz
		f = 100 Hz		10.2			10.3		
		f = 1 kHz		9.8			9.8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.38			0.38		µV
I_n	Equivalent input noise current	f = 10 Hz		0.35			0.35		pA/√Hz
		f = 100 Hz		0.15			0.15		
		f = 1 kHz		0.13			0.13		
$I_{N(PP)}$	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz		15			15		pA
SR	Slew rate	$R_L \geq 2$ kΩ		0.3			0.3		V/µs

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

electrical characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	OP07Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω		60	150	µV
	Long-term drift of input offset voltage	See Note 6		0.5		µV/mo
	Offset adjustment range	R_S = 20 kΩ, See Figure 1		±4		mV
I_{IO}	Input offset current			0.8	6	nA
I_{IB}	Input bias current			±2	±12	nA
V_{ICR}	Common-mode input voltage range		±13	±14		V
V_{OM}	Peak output voltage	$R_L \leq 10$ kΩ	±12	±13		V
		$R_L \leq 2$ kΩ	±11.5	±12.8		
		$R_L \leq 1$ kΩ		±12		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±3 V, V_O = ±0.5 V, $R_L \leq 500$ kΩ		400		
		V_O = ±10 V, R_L = 2 kΩ	120	400		
B_1	Unity-gain bandwidth		0.4	0.6		MHz
r_i	Input resistance		7	31		MΩ
CMRR	Common-mode input resistance	V_{IC} = ±13 V, R_S = 50 Ω	94	110		dB
k_{SVS}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±3 V to ±18 V, R_S = 50 Ω		7	32	µV/V
P_D	Power dissipation	V_O = 0, No load		80	150	MΩ
		$V_{CC\pm}$ = ±3 V, V_O = 0, No load		4	8	

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS†	OP07Y			UNIT
			MIN	TYP	MAX	
V_n	Equivalent input noise voltage	f = 10 Hz		10.5		nV/√Hz
		f = 1 kHz		10.3		
		f = 0.1 Hz to 10 Hz		9.8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.38		µV
I_n	Equivalent input noise current	f = 10 Hz		0.35		pA/√Hz
		f = 100 Hz		0.15		
		f = 1 kHz		0.13		
$I_{N(PP)}$	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz		15		pA
SR	Slew rate	R_L = 2 kΩ		0.3		V/µs

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

APPLICATION INFORMATION

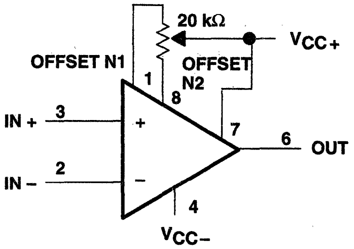


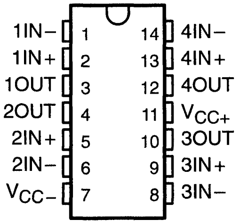
Figure 1. Input Offset Voltage Null Circuit

RC4136, RM4136, RV4136
QUAD GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

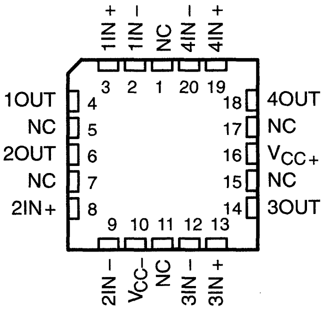
SLOS072 – MARCH 1978 – REVISED SEPTEMBER 1990

- **Continuous-Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Unity Gain Bandwidth . . . 3 MHz Typ**
- **Gain and Phase Match Between Amplifiers**
- **Designed To Be Interchangeable With Raytheon RC4136, RM4136, and RV4136**
- **Low Noise . . . 8 nV/$\sqrt{Hz}$ Typ at 1 kHz**

RM4136 . . . J OR W PACKAGE
ALL OTHERS . . . D OR N PACKAGE
(TOP VIEW)



RM4136 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

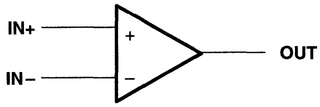
description

The RC4136, RM4136, and RV4136 are quad general-purpose operational amplifiers with each amplifier electrically similar to the µA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short circuit protected and the internal frequency compensation ensures stability without external components.

The RC4136 is characterized for operation from 0°C to 70°C, the RM4136 is characterized for operation over the full military temperature range of –55°C to 125°C, and the RV4136 is characterized for operation from –40°C to 85°C.

symbol (each amplifier)



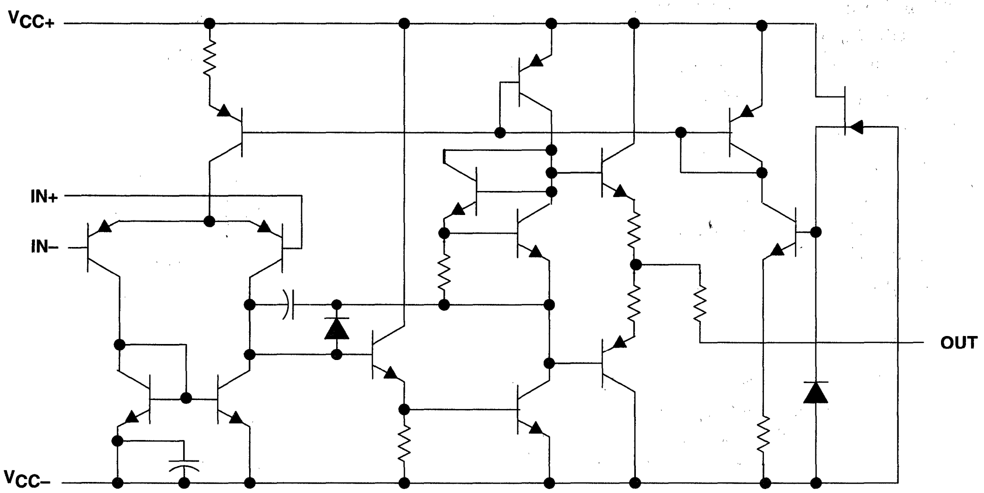
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT (W)
0°C to 70°C	6 mV	RC4136D	—	—	RC4136N	—
–40°C to 85°C	6 mV	RV4136D	—	—	RV4136N	—
–55°C to 125°C	4 mV	—	RM4136FK	RM4136J	—	RM4136W

The D packages are available taped and reeled. Add the suffix R to the device type (e.g., RC4136DR).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		RC4136	RM4136	RV4136	UNIT
Supply voltage V_{CC+} (see Note 1)		18	22	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−22	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit to ground, one amplifier at a time (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	−55 to 125	−40 to 85	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	—	260	—	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	—	300	—	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260	—	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	800 mW	7.6 mW/°C	45°C	608 mW	494 mW	—
FK	800 mW	11.0 mW/°C	77°C	800 mW	715 mW	275 mW
J	800 mW	11.0 mW/°C	77°C	800 mW	715 mW	275 mW
N	800 mW	9.2 mW/°C	63°C	736 mW	598 mW	—
W	800 mW	8.0 mW/°C	50°C	640 mW	520 mW	200 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	5	15	V
Supply voltage, V_{CC-}	−5	−15	V

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		RC4136			RM4136			RV4136			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Input offset voltage	$V_O = 0$	25°C		0.5	6		0.5	4		0.5	6	mV
			Full range			7.5			6			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	200		5	1.50		5	200	nA
			Full range			300			500			500	
I_{IB}	Input bias current	$V_O = 0$	25°C		140	500		140	400		140	500	nA
			Full range			800			1500			1500	
V_i	Input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±14		±12	±14		±12	±14		V
		$R_L = 2\ k\Omega$	25°C	±10	±13		±10	±13		±10	±13		
		$R_L \geq 2\ k\Omega$	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25°C	20	300		50	350		20	300		V/mV
			Full range	15			25			15			
B_1	Unity-gain bandwith		25°C		3			3.5			3		MHz
r_i	Input resistance		25°C	0.3*	5		0.3*	5		0.3*	5		MΩ
CMRR	Common-mode rejection ratio	$V_O = 0$, $R_S = 50\ \Omega$	25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ±15 V, $V_O = 0$	25°C		30	150		30	150		30	150	µV/V
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, BW = 1 Hz, f = 1 kHz, $R_S = 100\ \Omega$	25°C		8			8			8		nV√Hz
I_{CC}	Supply current (all four amplifiers)	$V_O = 0$, No load	25°C		5	11.3		5	11.3		5	11.3	mA
			MIN T_A		6	13.7		6	13.3		6	13.7	
			MAX T_A		4.5	10		4.5	10		4.5	10	
P_D	Total power dissipation (all four amplifiers)	$V_O = 0$, No load	25°C		150	340		150	340		150	340	mW
			MIN T_A		180	400		180	400		180	400	
			MAX T_A		135	300		135	300		135	300	
	Crosstalk attenuation (V_{O1}/V_{O2})	$A_{VD} = 100$, f = 10 kHz, $R_S = 1\ k\Omega$	25°C		105			105			105		dB

* This parameter is not production tested.

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is 0°C to 70°C for RC4136, −55°C to 125°C for RM4136, and −40°C to 85°C for RV4136. Minimum T_A is 0°C for RC4136, −55°C for RM4136, and −40°C for RV4136. Maximum T_A is 70°C for RC4136, 125°C for RM4136, and 85°C for RV4136.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

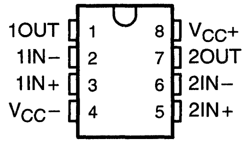
PARAMETER		TEST CONDITIONS	RC4136, RV4136			RM4136			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF		0.13			0.13		µs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF		1.7			1.7		V/µs

RC4558, RC4558Y, RM4558, RV4558
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

SLOS073 – MARCH 1976 – REVISED AUGUST 1991

- **Continuous-Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Unity Gain Bandwidth . . . 3 MHz Typ**
- **Gain and Phase Match Between Amplifiers**
- **Low Noise . . . 8 nV/√Hz Typ at 1 kHz**
- **Designed To Be Interchangeable With Raytheon RC4558, RM4558, and RV4558**

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



description

The RC4558, RM4558, and RV4558 are dual general-purpose operational amplifiers with each half electrically similar to the µA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RC4558 is characterized for operation from 0°C to 70°C, the RM4558 is characterized for operation over the full military temperature range of −55°C to 125°C, and the RV4558 is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

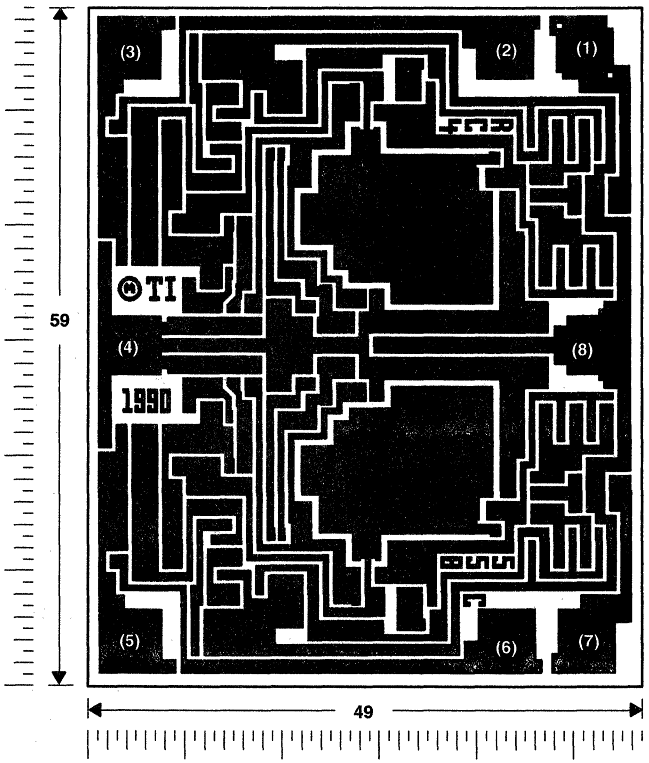
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	SSOP (DBLE)	CERAMIC DIP (JG)	PLASTIC DIP (P)	SSOP (PWLE)	
0°C to 70°C	6 mV	RC4558D	RC4558DBLE	—	RC4558P	RC4558PWLE	RC4558Y
−40°C to 85°C	6 mV	RV4558D	—	—	RV4558P	—	—
−55°C to 125°C	6 mV	—	—	RM4558JG	—	—	—

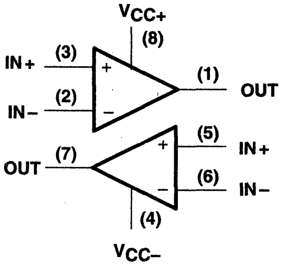
The D package is available taped and reeled. Add the suffix R to the device type (e.g., RC4558DR). The DB and PW packages are available only left-end taped and reeled. RC4558Y is tested at 25°C.

RC4558Y chip information

These chips, properly assembled, display characteristics similar to the RC4558. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

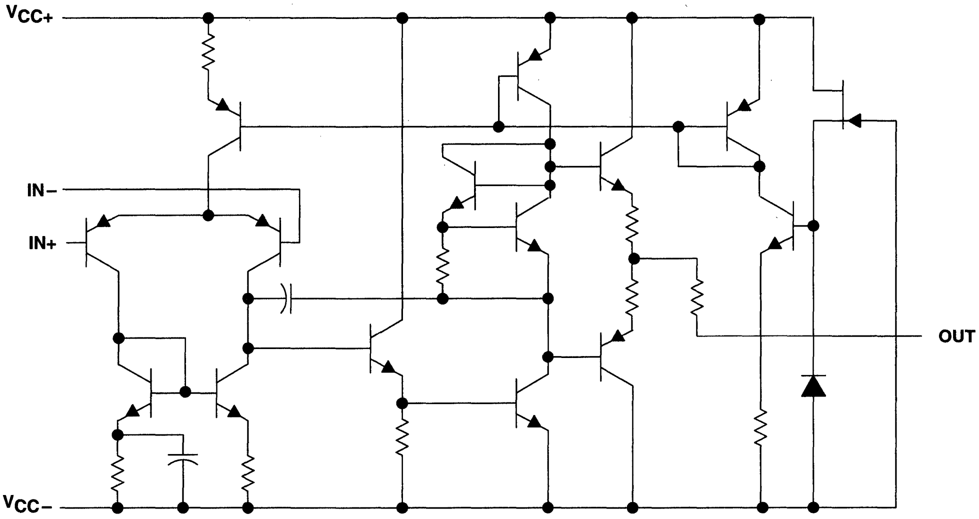
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	RC4558	RM4558	RV4558	UNIT
Supply voltage V_{CC+} (see Note 1)	18	22	18	V
Supply voltage V_{CC-} (see Note 1)	–18	–22	–18	V
Differential input voltage (see Note 2)	±30	±30	±30	V
Input voltage (any input, see Notes 1 and 3)	±15	±15	±15	V
Duration of output short circuit to ground, one amplifier at a time (see Note 4)	unlimited	unlimited	unlimited	
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	0 to 70	–55 to 125	–40 to 85	°C
Storage temperature range	–65 to 150	–65 to 150	–65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package		300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package	260		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
DB or PW	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	5	15	V
Supply voltage, V_{CC-}	−5	−15	V

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		RC4558			RM4558			RV4558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		0.5	6		0.5	5		0.5	6	mV
			Full range			7.5			6			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	200		5	200		5	200	nA
			Full range			300			500			500	
I_{IB}	Input bias current	V_O = 0	25°C		150	500		140	500		140	500	nA
			Full range			800			1500			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM}	Maximum output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		±12	±14		V
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		±10	±13		
		$R_L \geq$ 2 kΩ	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	20	300		50	350		20	300		V/mV
			Full range	15			25			15			
B_1	Unity-gain bandwith		25°C		3		2	3.5			3		MHz
r_i	Input resistance		25°C	0.3	5		0.3	5		0.3	5		MΩ
CMRR	Common-mode rejection ratio		25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±15 V to ±9 V	25°C		30	150		30	150		30	150	µV/V
V_n	Equivalent input noise voltage (closed loop)	A_{VD} = 100, R_S = 100 Ω, f = 1 kHz, BW = 1 Hz	25°C		8			8			8		nV/√Hz
I_{CC}	Supply current (both amplifiers)	V_O = 0, No load	25°C		2.5	5.6		2.5	5.6		2.5	5.6	mA
			MIN T_A		3	6.6		3	6.6		3	6.6	
			MAX T_A		2.3	5		2	5		2.3	5	
P_D	Total power dissipation (both amplifiers)	V_O = 0, No load	25°C		75	170		75	170		75	170	mW
			MIN T_A		90	200		90	200		90	200	
			MAX T_A		70	150		60	150		70	150	
V_{O1}/V_{O2}	Crosstalk attenuation Open loop	R_S = 1 kΩ, f = 10 kHz	25°C		85			85			85		dB
	A_{VD} = 100				105			105			105		

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is 0°C to 70°C for RC4558, −55°C to 125°C for RM4558, and −40°C to 85°C for RV4558. Minimum T_A is 0°C for RC4558, −55°C for RM4558, and −40°C for RV4558. Maximum T_A is 70°C for RC4558, 125°C for RM4558, and 85°C for RV4558.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF		0.13		ns
	Overshoot			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF	1.1	1.7		V/µs

electrical characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	RC4558Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage		V_O = 0		0.5	6	mV
I_{IO}	Input offset current		V_O = 0		5	200	nA
I_{IB}	Input bias current		V_O = 0		150	500	nA
V_{ICR}	Common-mode input voltage range			±12	±14		V
V_{OM}	Maximum output voltage swing		R_L = 10 kΩ	±12	±14		V
			R_L = 2 kΩ	±12	±13		
A_{VD}	Large-signal differential voltage amplification		R_L = 2 kΩ, V_O = ±10 V	20	300		V/mV
B_1	Unity-gain bandwidth				3		MHz
r_i	Input resistance			0.3	5		MΩ
CMRR	Common-mode rejection ratio			70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)		V_{CC} = ±15 V to ±9 V		30	150	µV/V
V_n	Equivalent input noise voltage (closed-loop)		A_{VD} = 100, R_S = 100 Ω, f = 1 kHz, BW = 1 Hz		8		nV$\sqrt{\text{Hz}}$
I_{CC}	Supply current (both amplifiers)		V_O = 0, No load		2.5	5.6	mA
P_D	Total power dissipation (both amplifiers)		V_O = 0, No load		75	170	mW
V_{O1}/V_{O2}	Crosstalk attentuation	Open loop	R_S = 1 kΩ, f = 10 kHz		85		dB
		A_{VD} = 100			105		

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

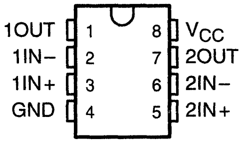
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF		0.13		ns
	Overshoot			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF	1.1	1.7		V/µs

TL022C, TL022M
DUAL LOW-POWER OPERATIONAL AMPLIFIERS

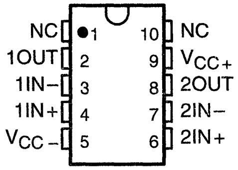
SLOS076 – SEPTEMBER 1973 – REVISED SEPTEMBER 1990

- **Very Low Power Consumption**
- **Power Dissipation With ±2-V Supplies 170 μW Typ**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Input Offset Voltage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **Popular Dual Operational Amplifier Pinout**

TL022M . . . JG PACKAGE
TL022C . . . D OR P PACKAGE
(TOP VIEW)



TL022M . . . U PACKAGE
(TOP VIEW)



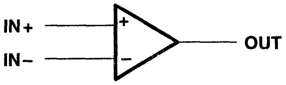
TL022M IS NOT RECOMMENDED FOR NEW DESIGNS

description

The TL022 is a dual low-power operational amplifier designed to replace higher power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use.

The TL022C is characterized for operation from 0°C to 70°C. The TL022M is characterized for operation over the full military temperature range of −55°C to 125°C.

symbol (each amplifier)

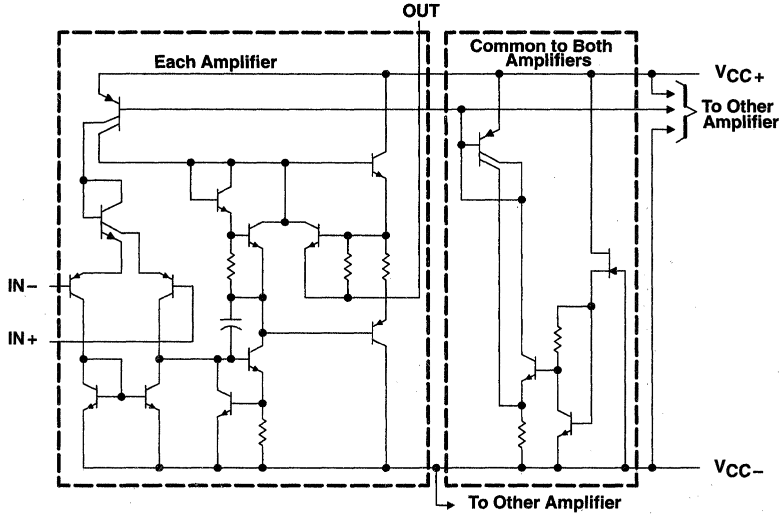


AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CERAMIC FLAT PACK (U)
0°C to 70°C	5 mV	TL022CD	—	TL022CP	—
−55°C to 125°C	5 mV	—	TL022MJG	—	TL022MU

The D package is available taped and reeled. Add the suffix R to the device type (i.e. TL022CDR).

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL022C	TL022M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	22	V
Supply voltage, V_{CC-} (see Note 1)		−18	−22	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260		°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL022M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	—
JG	680 mW	8.4 mW/°C	69°C	672 mW	210 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	—
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	5	15	V
Supply voltage, V_{CC-}	−5	−15	V

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL022C			TL022M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		1	5		1	5	mV
			Full range			7.5			6	
I_{IO}	Input offset current	$V_O = 0$	25°C		15	80		5	40	nA
			Full range			200			100	
I_{IB}	Input bias current	$V_O = 0$	25°C		100	250		50	100	nA
			Full range			400			250	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	$R_L = 10\ k\Omega$	25°C	20	26		20	26		V
		$R_L \geq 10\ k\Omega$	Full range	20			20			
A_{VD}	Large-signal differehtial voltage amplification	$R_L \geq 10\ k\Omega$, $V_O = \pm10$ V	25°C	60	80		72	86		dB
			Full range	60			66			
B_1	Unity-gain bandwidth		25°C		0.5			0.5		MHz
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $R_S = 50\ \Omega$	25°C	60	72		60	72		dB
			Full range	60			60			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm9$ V to ±15 V, $R_S = 50\ \Omega$	25°C		30	200		30	150	µV/V
			Full range			200			150	
V_n	Equivalent input noise voltage	$A_{VD} = 20$ dB, $B = 1$ Hz, f = 1 kHz	25°C		50			50		nV/Hz
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (both amplifiers)	$V_O = 0$, No load	25°C		130	250		130	250	µA
			Full range			250			250	
P_D	Total dissipation (both amplifiers)	$V_O = 0$, No load	25°C		3.9	7.5		3.9	6	mW
			Full range			7.5			6	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for TL022C is 0°C to 70°C and for TL022M is −55°C to 125°C.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	$V_I = 20$ mV, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.5		V/µs

PARAMETER MEASUREMENT INFORMATION

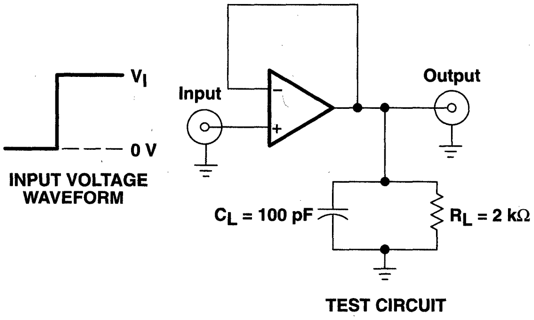


Figure 1. Rise Time, Overshoot Factor, and Slew Rate

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION vs SUPPLY RATE

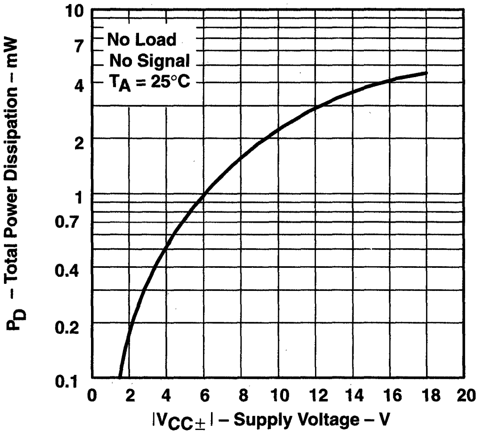


Figure 2

TL03x, TL03xA, TL03xY
ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180 – FEBRUARY 1997

- **Direct Upgrades for the TL06x Low-Power BiFETs**
- **Low Power Consumption 6.5 mW/Channel Typ**
- **On-Chip Offset Voltage Trimming For Improved DC Performance (1.5 mV, TL031A)**
- **Higher Slew Rate And Bandwidth Without Increased Power Consumption**
- **Available in TSSOP For Small Form-Factor Designs**

description

The TL03x series of JFET-input operational amplifiers offer improved dc and ac characteristics over the TL06x family of low power BiFET operational amplifiers. On-chip zener trimming of offset voltage yields precision grades as low as 1.5 mV (TL031A) for greater accuracy in dc-coupled applications. Texas Instruments improved BiFET process and optimized designs also yield improved bandwidths and slew rates without increased power consumption. The TL03x devices are pin-compatible with the TL06x and can be used to upgrade existing circuits or for optimal performance in new designs.

BiFET operational amplifiers offer the inherently higher input impedance of the JFET-input transistors, without sacrificing the output drive associated with bipolar amplifiers. This higher input impedance makes the TL3x amplifiers better suited for interfacing with high-impedance sensors or very low-level ac signals. These devices also feature inherently better ac response than bipolar or CMOS devices having comparable power consumption.

The TL03x family has been optimized for micropower operation, while improving on the performance of the TL06x series. Designers requiring significantly faster ac response should consider the Excalibur TLE206x family of low power BiFET operational amplifiers.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES							CHIP FORM‡ (Y)
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	0.8 mV	TL031ACD TL032ACD	—	—	—	—	TL031ACP TL032ACP	—	TL031Y TL032Y TL034Y
	1.5 mV	TL031CD TL032CD TL034ACD	—	—	—	TL034ACN	TL031CP TL032CP	—	
	4 mV	TL034CD	—	—	—	TL034CN		TL034CPW	
−40°C t0 85°C	0.8 mV	TL031AID TL032AID	—	—	—	—	TL031AIP TL032AIP	—	—
	1.5 mV	TL031ID TL032ID TL034AID	—	—	—	TL034AIN	TL031IP TL032IP	—	—
	4 mV	TL034ID	—	—	—	TL034IN	—	—	—
−55°C to 125°C	0.8 mV	TL031AMD TL032AMD	TL031AMFK TL032AMFK	—	TL031AMJG TL032AMJG	—	TL031AMP TL032AMP	—	—
	1.5 mV	TL031MD TL032MD TL034AMD	TL031MFK TL032MFK TL034AMFK	TL034AMJ	TL031MJG TL032MJG	TL034AMN	TL031MP TL032MP	—	—
	4 mV	TL034MD	TL034MFK	TL034MJ	—	TL034MN	—	—	—

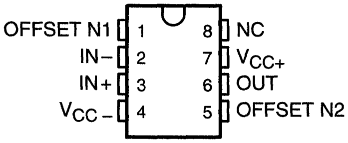
† The D packages are available taped and reeled and is indicated by adding an R suffix to device type (e.g., TL034CDR).
‡ Chip forms are tested at 25°C.

description (continued)

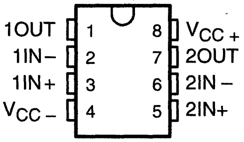
Because BiFET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required and loads should be terminated to a virtual ground node at mid-supply. Texas Instruments TLE2426 integrated virtual ground generator is useful when operating BiFET amplifiers from single supplies.

The TL03x are fully specified at ±15 V and ±5 V. For operation in low-voltage and/or single-supply systems, Texas Instruments LinCMOS families of operational amplifiers (TLC-prefix) are recommended. When moving from BiFET to CMOS amplifiers, particular attention should be paid to slew rate and bandwidth requirements, and output loading.

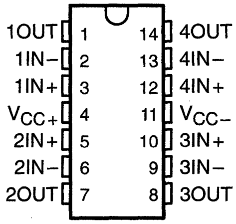
TL031x, TL031Ax
D, JG, OR P PACKAGE
(TOP VIEW)



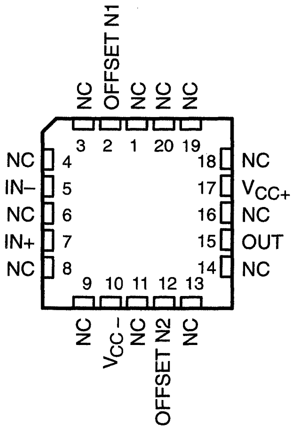
TL032x, TL032Ax
D, JG, OR P PACKAGE
(TOP VIEW)



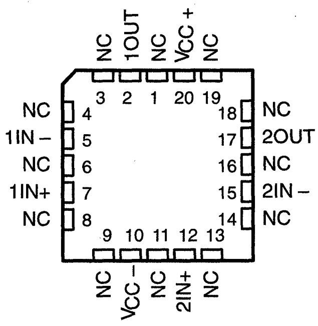
TL034x, TL034Ax
D, J, N, OR PW PACKAGE
(TOP VIEW)



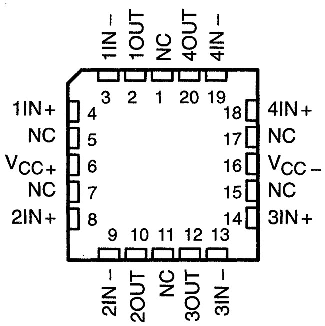
TL031M, TL031AM
FK PACKAGE
(TOP VIEW)



TL032M, TL032AM
FK PACKAGE
(TOP VIEW)

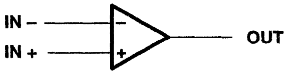


TL034M, TL034AM
FK PACKAGE
(TOP VIEW)

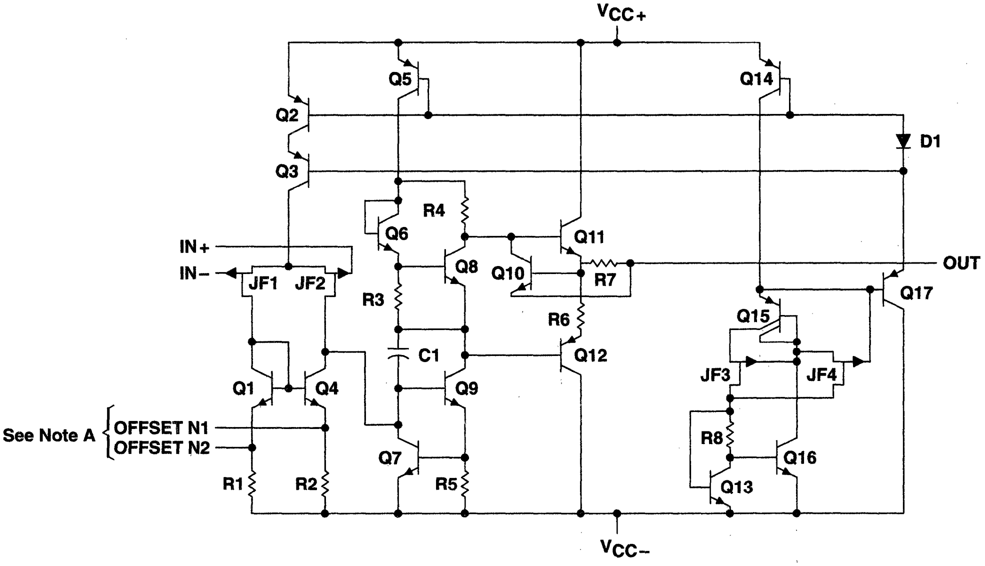


NC – No internal connection

symbol (each amplifier)



equivalent schematic (each amplifier)

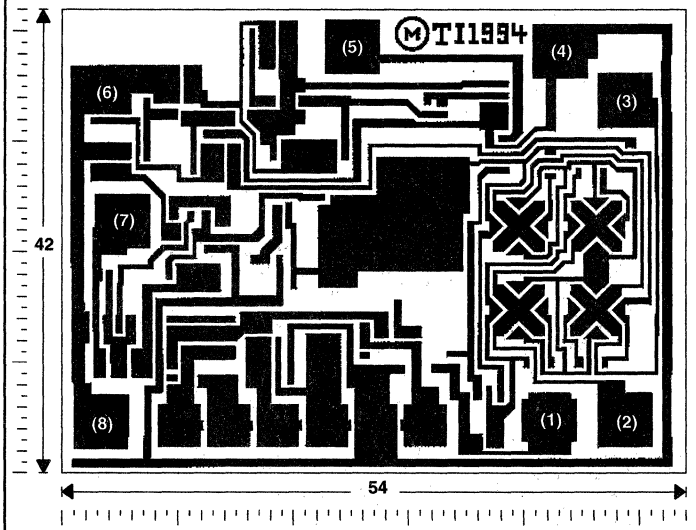


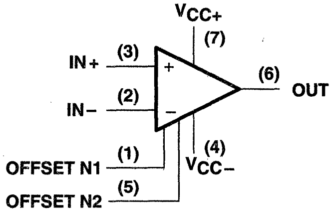
NOTE A: OFFSET N1 and OFFSET N2 are only available on the TL031.

TL031Y chip information

This chip, when properly assembled, displays characteristics similar to the TL031C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. These chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

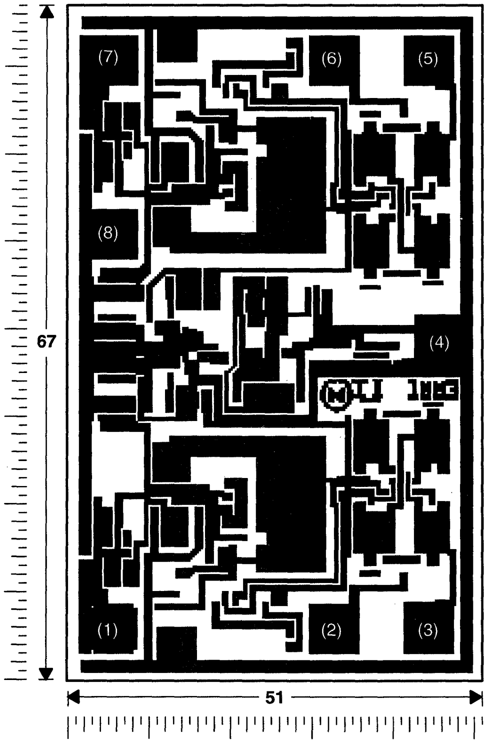
ALL DIMENSIONS ARE IN MILS.

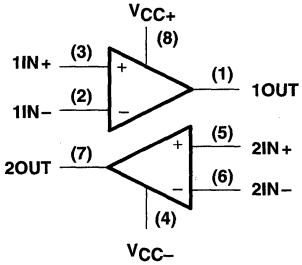
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

TL032Y chip information

This chip, when properly assembled, displays characteristics similar to the TL032C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. These chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

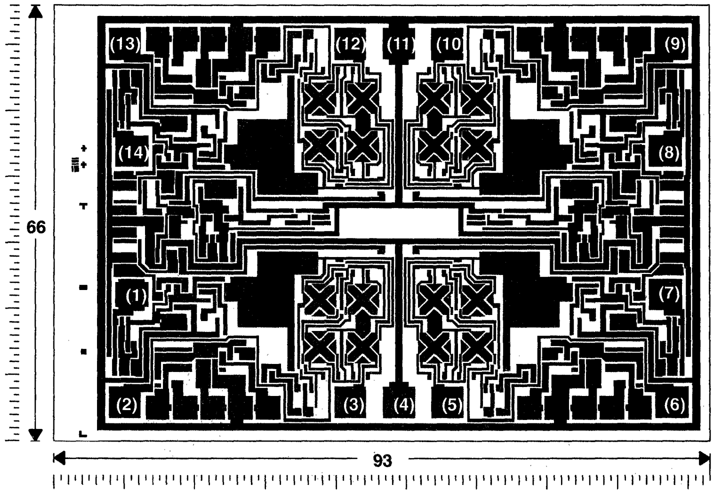
ALL DIMENSIONS ARE IN MILS.

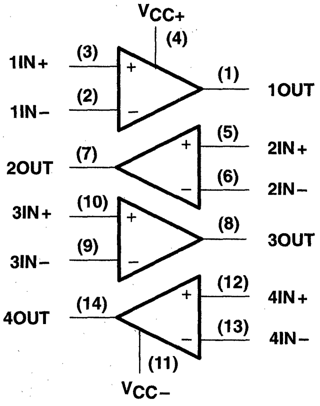
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TL034Y chip information

This chip, when properly assembled, displays characteristics similar to the TL034C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. These chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	−18 V
Differential input voltage, V_{ID} (see Note 2)	±30 V
Input voltage, V_I (any input) (see Notes 1 and 3)	±15 V
Input current, I_I (each input)	±1 mA
Output current, I_O (each output)	±40 mA
Total current into V_{CC+}	160 mA
Total current out of V_{CC-}	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1 /16 inch) from case for 10 seconds: D, N, P, or PW package	260°C
Lead temperature 1,6 mm (1 /16 inch) from case for 60 seconds: J or JG package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1100 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	700 mW	5.6 mW/°C	448 mW	N/A	N/A

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±5	±15	±5	±15	±5	±15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	−1.5	4	−1.5	4	−1.5	4	V
	$V_{CC\pm} = \pm 15$ V	−11.5	14	−11.5	14	−11.5	14	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

TL031C and TL031AC electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL031C, TL031AC						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL031C	25°C		0.54	3.5		0.5	1.5	mV
				Full range			4.5			2.5	
			TL031AC	25°C		0.41	2.8		0.34	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage‡		TL031C	25°C to 70°C		7.1			5.9		µV/°C
			TL031AC	25°C to 70°C		7.1			5.9	25	
	Input offset voltage long-term drift§			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to .4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification¶	$R_L = 10\ k\Omega$		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\min$, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		

† Full range is 0°C to 70°C.

‡ This parameter is tested on a sample basis for the TL031A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TL031C and TL031AC electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS		T_A	TL031C, TL031AC						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
P_D	Total power dissipation	$V_O = 0$,	No load	25°C		1.9	2.5		6.5	8.4	mW
				0°C		1.8	2.5		6.3	8.4	
				70°C		1.9	2.5		6.3	8.4	
I_{CC}	Supply current	$V_O = 0$,	No load	25°C		192	250		217	280	µA
				0°C		184	250		211	280	
				70°C		189	250		210	280	

TL031C and TL031AC operating characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL031C, TL031AC						UNIT
						$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain†		$R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1		25°C		2		1.5	2.9		V/µs
					0°C		1.8		1	2.6		
					70°C		2.2		1.5	3.2		
SR–	Negative slew rate at unity gain†				25°C		3.9		1.5	5.1		V/µs
					0°C		3.7		1.5	5		
					70°C		4		1.5	5		
t_r	Rise time		$V_{I(PP)} = \pm10$ mV, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
t_f	Fall time		$V_{I(PP)} = \pm10$ mV, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
	Overshoot factor		$V_{I(PP)} = \pm10$ mV, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2		25°C		11%			5%		
					0°C		10%			4%		
					70°C		12%			6%		
V_n	Equivalent input noise voltage‡	TL031C	$R_S = 20\ \Omega$, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
				f = 1 kHz			41			41		
		TL031AC		f = 10 Hz	25°C		61			61		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B_1	Unity-gain bandwidth		$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4		25°C		1			1.1		MHz
					0°C		1			1.1		
					70°C		1			1		
ϕ_m	Phase margin at unity gain		$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4		25°C		61°			65°		
					0°C		61°			65°		
					70°C		60°			64°		

† For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.
‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TL031I and TL031AI electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL031I, TL031AI						UNIT
					$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL031I	25°C		0.54	3.5		0.5	1.5	mV
				Full range			5.3			3.3	
			TL031AI	25°C		0.41	2.8		0.34	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage‡		TL031I	25°C to 85°C		6.5			6.2		µV/°C
			TL031AI	25°C to 85°C		6.5			6.2	25	
	Input offset voltage long-term drift§			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.2	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification¶	R_L = 10 kΩ		25°C	4	12		5	14.3		V/mV
				−40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		

† Full range is −40°C to 85°C.

‡ This parameter is tested on a sample basis for the TL031A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

TL031I and TL031AI electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS	T_A	TL031I, TL031AI						UNIT
				$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
P_D	Total power dissipation	V_O = 0, No load	25°C		1.9	2.5		6.5	8.4	mW
			−40°C		1.4	2.5		5.4	8.4	
			85°C		1.9	2.5		6.2	8.4	
I_{CC}	Supply current	V_O = 0, No load	25°C		192	250		217	280	µA
			−40°C		144	250		181	280	
			85°C		189	250		207	280	

TL031I and TL031AI operating characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL031I, TL031AI						UNIT
						$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain†		R_L = 10 kΩ, C_L = 100 pF, See Figure 1		25°C		2		1.5	2.9		V/µs
					−40°C		1.6		1	2.1		
					85°C		2.3		1.5	3.3		
SR−	Negative slew rate at unity gain†				25°C		3.9		1.5	5.1		V/µs
					−40°C		3.3		1.5	4.8		
					85°C		4.1		1.5	4.9		
t_r	Rise time		$V_{I(PP)}$ = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
t_f	Fall time		$V_{I(PP)}$ = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figure 1		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
	Overshoot factor		$V_{I(PP)}$ = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		11%			5%		
					−40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage‡	TL031I	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
				f = 1 kHz			41			41		
		TL031AI		f = 10 Hz	25°C		61			61		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B_1	Unity-gain bandwidth		V_I = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		V_I = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−40°C		60°			65°		
					85°C		60°			64°		

† For $V_{CC\pm}$ = ±5 V, $V_{I(PP)}$ = ±1 V; for $V_{CC\pm}$ = ±15 V, $V_{I(PP)}$ = ±5 V.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TL031M and TL031AM electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL031M, TL031AM						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL031M	25°C		0.54	3.5		0.5	1.5	mV
				Full range			6.5			4.5	
			TL031AM	25°C		0.41	2.8		0.34	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL031M	25°C to 125°C		5.1			4.3		µV/°C
			TL031AM	25°C to 125°C		5.1			4.3		
	Input offset voltage long-term drift‡			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification§	$R_L = 10\ k\Omega$		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−55°C	75	96		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation	$V_O = 0$, No load		25°C		1.9	2.5		6.5	8.4	mW
				−55°C		1.1	2.5		4.7	8.4	
				125°C		1.8	2.5		5.8	8.4	

† Full range is – 55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TL031M and TL031AM electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS		T_A	TL031M, TL031AM						UNIT
					$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	$V_O = 0$,	No load	25°C		192	250		217	280	μA
				−55°C		114	250		156	280	
				125°C		178	250		197	280	

TL031M and TL031AM operating characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL031M, TL031AM						UNIT
						$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain†		$R_L = 10$ kΩ, $C_L = 100$ pF, See Figure 1		25°C		2		1.5	2.9		V/μs
					−55°C		1.4		1	1.9		
					125°C		2.4		1	3.5		
SR−	Negative slew rate at unity gain†				25°C		3.9		1.5	5.1		V/μs
					−55°C		3.2		1	4.6		
					125°C		4.1		1	4.7		
t_r	Rise time		$V_{I(PP)} = \pm 10$ mV, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
t_f	Fall time		$V_{I(PP)} = \pm 10$ mV, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figure 1		25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
	Overshoot factor		$V_{I(PP)} = \pm 10$ mV, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		11%			5%		
					−55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL031M	$R_S = 20$ Ω, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
				f = 1 kHz			41			41		
		TL031AM		f = 10 Hz	25°C		61			61		
				f = 1 kHz			41			41		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B_1	Unity-gain bandwidth		$V_I = 10$ mV, $R_L = 10$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		1			1.1		MHz
					−55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		$V_I = 10$ mV, $R_L = 10$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		61°			65°		
					−55°C		57°			64°		
					125°C		59°			62°		

† For $V_{CC\pm} = \pm 5$ V, $V_{I(PP)} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{I(PP)} = \pm 5$ V.

TL031Y electrical characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TL031Y						UNIT
			$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$		0.54			0.5		mV
α_{VIO}	Temperature coefficient of input offset voltage			7.1			5.9		μV/°C
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		1			1		pA
I_{IB}	Input bias current			2			2		pA
V_{ICR}	Common-mode input voltage range			−3.4 to 5.4			−13.4 to 15.4		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		4.3			14		V
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		−4.2			−13.9		V
A_{VD}	Large-signal differential voltage amplification†	$R_L = 10\ k\Omega$		12			14.3		V/mV
r_i	Input resistance			10^{12}			10^{12}		Ω
c_i	Input capacitance			5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$		87			94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		96			96		dB
P_D	Total power dissipation	$V_O = 0$, No load		1.9			6.5		mW
I_{CC}	Supply current			192			217		μA

† At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TL031Y operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL031Y						UNIT
				$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain†	$R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1			2			2.9		V/μs
SR−	Negative slew rate at unity gain†				3.9			5.1		V/μs
t_r	Rise time	$V_{I(PP)} = \pm10$ mV, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2			138			132		ns
t_f	Fall time				138			132		ns
	Overshoot factor				11%			5%		
V_n	Equivalent input noise voltage‡	$R_S = 20\ \Omega$, See Figure 3	f = 10 Hz		61			61		nV/√Hz
			f = 1 kHz		41			41		
I_n	Equivalent input noise current	f = 1 kHz			0.003			0.003		pA/√Hz
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4			1			1.1		MHz
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4			61°			65°		

† For $V_{CC\pm} = \pm 5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm 5$ V.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TL032C and TL032AC electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL032C, TL032AC						UNIT
					$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL032C	25°C		0.69	3.5		0.57	1.5	mV
				Full range			4.5			2.5	
			TL032AC	25°C		0.53	2.8		0.39	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage‡		TL032C	25°C to 70°C		11.5			10.8		μV/°C
			TL032AC	25°C to 70°C		11.5			10.8	25	
	Input offset voltage long-term drift§			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification¶	R_L = 10 kΩ		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		5			14		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		

† Full range is 0°C to 70°C.

‡ This parameter is tested on a sample basis for the TL032A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ At $V_{CC\pm}$ = ±5 V, V_O = 2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

TL032C and TL032AC electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS		T_A	TL032C, TL032AC						UNIT
					$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
P_D	Total power dissipation (two amplifiers)	$V_O = 0$,	No load	25°C		3.8	5		13	17	mW
				0°C		3.7	5		12.7	17	
				70°C		3.8	5		12.6	17	
I_{CC}	Supply current (two amplifiers)	$V_O = 0$,	No load	0°C		368	500		422	560	mA
				70°C		378	500		420	560	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$ dB		25°C		120			120		dB

TL032C and TL032AC operating characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL032C, TL032AC						UNIT
						$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain†		$R_L = 10$ kΩ, $C_L = 100$ pF, See Figure 1		25°C		12		1.5	2.9		V/µs
					0°C		1.8		1	2.6		
					70°C		2.2		1.5	3.2		
SR–	Negative slew rate at unity gain†				25°C		3.9		1.5	5.1		V/µs
					0°C		3.7		1.5	5		
					70°C		4		1.5	5		
t_r	Rise time		$V_{I(PP)} = \pm 10$ V, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
t_f	Fall time				25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
	Overshoot factor				25°C		11%			5%		
					0°C		10%			4%		
					70°C		12%			6%		
V_n	Equivalent input noise voltage‡	TL032C	$R_S = 20$ Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AC		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B_1	Unity-gain bandwidth		$V_I = 10$ mV, $R_L = 10$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		1			1.1		MHz
					0°C		1			1.1		
					70°C		1			1		
ϕ_m	Phase margin at unity gain		$V_I = 10$ mV, $R_L = 10$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		61°			65°		
					0°C		61°			65°		
					70°C		60°			64°		

† For $V_{CC\pm} = \pm 5$ V, $V_{I(PP)} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{I(PP)} = \pm 5$ V.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TL032I and TL032AI electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL032I, TL032AI						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL032I	25°C		0.69	3.5		0.57	1.5	mV
				Full range			5.3			3.3	
			TL032AI	25°C		0.53	2.8		0.39	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage‡		TL032I	25°C to 85°C		11.4			10.8		µV/°C
			TL032AI	25°C to 85°C		11.4			10.8	25	
	Input offset voltage long-term drift§			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−40°C	3	4.2		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification¶	$R_L = 10\ k\Omega$		−40°C	3	8.4		4	11.6		V/mV
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		

† Full range is −40°C to 85°C.

‡ This parameter is tested on a sample basis for the TL032A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ At $V_{CC\pm} = \pm5$ V, $V_O = 2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TL032I and TL032AI electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS		T_A	TL032I, TL032AI						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
P_D	Total power dissipation (two amplifiers)	$V_O = 0$,	No load	25°C		3.8	5		13	17	mW
				−40°C		2.9	5		10.9	17	
				85°C		3.7	5		12.4	17	
I_{CC}	Supply current (two amplifiers)	$V_O = 0$,	No load	25°C		384	500		434	560	µA
				−40°C		288	500		362	560	
				85°C		372	500		414	560	
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100 dB		25°C		120			120		dB

TL032I and TL032AI operating characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL032I, TL032AI						UNIT
						$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain†		R_L = 10 kΩ,	C_L = 100 pF	25°C		2		1.5	2.9		V/µs
					−40°C		1.6		1	2.1		
					85°C		2.3		1.5	3.3		
SR−	Negative slew rate at unity gain†				25°C		3.9		1.5	5.1		V/µs
					−40°C		3.3		1.5	4.8		
					85°C		4.1		1.5	4.9		
t_r	Rise time		$V_{I(PP)} = \pm10$ V, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
t_f	Fall time		$V_{I(PP)} = \pm10$ V, R_L = 10 kΩ, C_L = 100 pF, See Figure 1		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
	Overshoot factor		$V_{I(PP)} = \pm10$ V, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		11%			5%		
					−40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage‡	TL032I	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AI		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B_1	Unity-gain bandwidth		V_I = 10 mV, C_L = 25 pF,	R_L = 10 kΩ, See Figure 4	25°C		1			1.1		MHz
					−40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		V_I = 10 mV, C_L = 25 pF,	R_L = 10 kΩ, See Figure 4	25°C		61°			65°		
					−40°C		61°			65°		
					85°C		60°			64°		

† For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TL032M and TL032AM electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL032M, TL032AM						UNIT
					$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL032M	25°C		0.69	3.5		0.57	1.5	mV
				Full range			6.5			4.5	
			TL032AM	25°C		0.53	2.8		0.39	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL032M	25°C to 125°C		9.7			9.7		µV/°C
			TL032AM	25°C to 125°C		9.7			9.7		
	Input offset voltage long-term drift‡			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification§	R_L = 10 kΩ		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		

† Full range is −55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At $V_{CC\pm}$ = ±5 V, V_O = 2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

TL032M and TL032AM electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS	T_A	TL032M, TL032AM						UNIT
				$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
				MIN	TYP	MAX	MIN	TYP	MAX	
P_D	Total power dissipation (two amplifiers)	$V_O = 0$, No load	25°C		3.8	5		13	17	mW
			−55°C		2.3	5		9.4	17	
			125°C		3.6	5		11.8	17	
I_{CC}	Supply current (two amplifiers)	$V_O = 0$, No load	25°C		384	500		434	560	µA
			−55°C		228	500		312	560	
			125°C		356	500		394	560	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$ dB	25°C		120			120		dB

TL032M and TL032AM operating characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL032M, TL032AM						UNIT
						$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain†		$R_L = 10$ kΩ, $C_L = 100$ pF, See and Figure 1		25°C		2		1.5	2.9		V/µs
					−55°C		1.4		1	1.9		
					125°C		2.4		1	3.5		
SR–	Negative slew rate at unity gain†				25°C		3.9		1.5	5.1		V/µs
					−55°C		3.2		1	4.6		
					125°C		4.1		1	4.7		
t_r	Rise time		$V_{I(PP)} = \pm10$ V, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		138			132		ns
					−55°C		142			123		
					125°C		166			58		
t_f	Fall time		$V_{I(PP)} = \pm10$ V, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figure 1		25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
	Overshoot factor		$V_{I(PP)} = \pm10$ V, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		11%			5%		
					−55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL032M	$R_S = 20\ \Omega$, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AM		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		$V_I = 10$ mV, $R_L = 10$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		1			1.1		MHz
					−55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		$V_I = 10$ mV, $R_L = 10$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		61°			65°		
					−55°C		57°			64°		
					125°C		59°			62°		

† For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

TL032Y electrical characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TL032Y						UNIT
			$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$		0.69			0.57		mV
α_{VIO}	Temperature coefficient of input offset voltage			11.5			10.8		µV/°C
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		1			1		pA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		2			2		pA
V_{ICR}	Common-mode input voltage range			−3.4 to 5.4			−13.4 to 15.4		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		4.3			14		V
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		−4.2			−13.9		V
A_{VD}	Large-signal differential voltage amplification†	$R_L = 10\ k\Omega$		12			14.3		V/mV
r_i	Input resistance			10^{12}			10^{12}		Ω
c_i	Input capacitance			5			14		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$		87			94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		96			96		dB
P_D	Total power dissipation (two amplifiers)	$V_O = 0$, No load		3.8			13		mW
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$ dB		120			120		dB

† At $V_{CC\pm} = \pm 5$ V, $V_O = 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

TL032Y operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TL032Y						UNIT
			$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain†	$R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1 and Note 8		12			2.9		V/µs
SR−	Negative slew rate at unity gain†			3.9			5.1		V/µs
t_r	Rise time	$V_{I(PP)} = \pm 10$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2		138			132		ns
t_f	Fall time			138			132		ns
	Overshoot factor			11%			5%		
V_n	Equivalent input noise voltage‡	$R_S = 20\ \Omega$, See Figure 3; f = 10 Hz		49			49		nV/√Hz
		f = 1 kHz		41			41		
I_n	Equivalent input noise current	f = 1 kHz		0.003			0.003		pA/√Hz
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4		1			1.1		MHz
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4		61°			65°		

† For $V_{CC\pm} = \pm 5$ V, $V_{I(PP)} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{I(PP)} = \pm 5$ V.
‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TL034C and TL034AC electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL034C, TL034AC						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034C	25°C		0.91	6		0.79	4	mV
				Full range			8.2			6.2	
			TL034AC	25°C		0.7	3.5		0.58	1.5	
				Full range			5.7			3.7	
α_{VIO}	Temperature coefficient of input offset voltage‡		TL034C	25°C to 70°C		11.6			12		µV/°C
			TL034AC	25°C to 70°C		11.6			12	25	
	Input offset voltage long-term drift§			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification¶	$R_L = 10\ k\Omega$		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		5			14		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\mathrm{min}$, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		

† Full range is 0°C to 70°C.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TL034C and TL034AC electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS	T_A	TL034C, TL034AC						UNIT
				$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
				MIN	TYP	MAX	MIN	TYP	MAX	
P_D	Total power dissipation (two amplifiers)	$V_O = 0$, No load	25°C		7.7	10		26	34	mW
			0°C		7.4	10		25.3	34	
			70°C		7.6	10		25.2	34	
I_{CC}	Supply current (four amplifiers)	$V_O = 0$, No load	25°C		0.77	1		0.87	1.12	mA
			0°C		0.74	1		0.85	1.12	
			70°C		0.76	1		0.84	1.12	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

TL034C and TL034AC operating characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL034C, TL034AC						UNIT
						$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain[†]		$R_L = 10$ kΩ, $C_L = 100$ pF, See Figure 1		25°C		2		1.5	2.9		V/μs
					0°C		1.8		1	2.6		
					70°C		2.2		1.5	3.2		
SR–	Negative slew rate at unity gain[†]				25°C		3.9		1.5	5.1		V/μs
					0°C		3.7		1.5	5		
					70°C		4		1.5	5		
t_r	Rise time		$V_{I(PP)} = \pm10$ V, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
t_f	Fall time		$V_{I(PP)} = \pm10$ V, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figure 1		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
	Overshoot factor		$V_{I(PP)} = \pm10$ V, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		11%			5%		
					0°C		10%			4%		
					70°C		12%			6%		
V_n	Equivalent input noise voltage[‡]	TL034C	$R_S = 20$ Ω, See Figure 3	f = 10 Hz	25°C		83			83		nV/√Hz
				f = 1 kHz			43			43		
		TL034AC		f = 10 Hz	25°C		83			83		
				f = 1 kHz			43			43	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B_1	Unity-gain bandwidth		$V_I = 10$ mV, $R_L = 10$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		1			1.1		MHz
					0°C		1			1.1		
					70°C		1			1		
ϕ_m	Phase margin at unity gain		$V_I = 10$ mV, $R_L = 10$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		61°			65°		
					0°C		61°			65°		
					70°C		60°			64°		

[†] For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

[‡] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TL034I and TL034AI electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL034I, TL034AI						UNIT
					$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034I	25°C		0.91	36		0.79	4	mV
				Full range			9.3			7.3	
			TL034AI	25°C		0.7	3.5		0.58	1.5	
				Full range			6.8			4.8	
α_{VIO}	Temperature coefficient of input offset voltage‡		TL034I	25°C to 85°C		11.5			11.6		µV/°C
			TL034AI	25°C to 85°C		11.5			11.6	25	
	Input offset voltage long-term drift§			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification¶	$R_L = 10\ k\Omega$		−40°C	4	12		5	14.3		V/mV
				85°C	3	8.4		4	11.6		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		

† Full range is −40°C to 85°C.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

TL034I and TL034AI electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS	T_A	TL034I, TL034AI						UNIT
				$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
				MIN	TYP	MAX	MIN	TYP	MAX	
P_D	Total power dissipation (four amplifiers)	$V_O = 0$, No load	25°C		7.7	10		26	34	mW
			−40°C		5.8	10		21.7	34	
			85°C		7.4	10		24.8	34	
I_{CC}	Supply current (four amplifiers)	$V_O = 0$, No load	25°C		0.77	1		0.87	1.12	mA
			−40°C		0.58	1		0.72	1.12	
			85°C		0.74	1		0.83	1.12	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

TL034I and TL034AI operating characteristics

PARAMETER			TEST CONDITIONS		T_A	TL034I, TL034AI						UNIT
						$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain†		$R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1		25°C		2		1.5	2.9		V/μs
					−40°C		1.6		1	2.1		
					85°C		2.3		1.5	3.3		
SR−	Negative slew rate at unity gain†				25°C		3.9		1.5	5.1		V/μs
					−40°C		3.3		1.5	4.8		
					85°C		4.1		1.5	4.9		
t_r	Rise time		$V_{I(PP)} = \pm10$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
t_f	Fall time				25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
	Overshoot factor				25°C		11%			5%		
					−40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage‡	TL034I	$R_S = 20\ \Omega$, See Figure 3	f = 10 Hz	25°C		83			83		nV/√Hz
				f = 1 kHz			43			43		
		TL034AI		f = 10 Hz	25°C		83			83		
				f = 1 kHz			43			43	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B_1	Unity-gain bandwidth		$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4		25°C		1			1.1		MHz
					−40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4		25°C		61°			65°		
					−40°C		61°			65°		
					85°C		60°			64°		

† For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TL034M and TL034AM electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL034M, TL034AM						UNIT
					$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034M	25°C		0.91	3.6		0.78	4	mV
				Full range			11			9	
			TL034AM	25°C		0.7	3.5		0.58	1.5	
				Full range			8.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage		TL034M	25°C to 125°C		10.6			10.9		µV/°C
			TL034AM	25°C to 125°C		10.6			10.9		
	Input offset voltage long-term drift‡			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification§	$R_L = 10\ k\Omega$		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		

† Full range is −55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

TL034M and TL034AM electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS		T_A	TL034M, TL034AM						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
P_D	Total power dissipation (two amplifiers)	$V_O = 0$,	No load	25°C		7.7	10		26	34	mW
				–55°C		4.6	12		18.7	45	
				125°C		7.1	12		23.6	45	
I_{CC}	Supply current (two amplifiers)	$V_O = 0$,	No load	25°C		0.77	1		0.87	1.12	mA
				–55°C		0.46	1.2		0.62	1.5	
				125°C		0.71	1.2		0.79	1.5	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

TL034M and TL034AM operating characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL034M, TL034AM						UNIT
						$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain†		$R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1		25°C		2		1.5	2.9		V/μs
					–55°C		1.4		1	1.9		
					125°C		2.4		1	3.5		
SR–	Negative slew rate at unity gain†				25°C		3.9		1.5	5.1		V/μs
					–55°C		3.2		1	4.6		
					125°C		4.1		1	4.7		
t_r	Rise time		$V_{I(PP)} = \pm10$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2		25°C		138			132		ns
					–55°C		142			123		
					125°C		166			58		
t_f	Fall time		$V_{I(PP)} = \pm10$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1		25°C		138			132		ns
					–55°C		142			123		
					125°C		166			158		
	Overshoot factor		$V_{I(PP)} = \pm10$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2		25°C		11%			5%		
					–55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL034M	$R_S = 20\ \Omega$, See Figure 3	f = 10 Hz	25°C		83			83		nV/√Hz
				f = 1 kHz			43			43		
		TL034AM		f = 10 Hz	25°C		83			83		
				f = 1 kHz			43			43		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4		25°C		1			1.1		MHz
					–55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4		25°C		61°			65°		
					–55°C		57°			64°		
					125°C		59°			62°		

† For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

TL034Y electrical characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TL034Y						UNIT
			$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$		0.91			0.79		mV
α_{VIO}	Temperature coefficient of input offset voltage			11.6			12		µV/°C
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		1			1		pA
				2			2		pA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		2			2		pA
				7			8		nA
V_{ICR}	Common-mode input voltage range			−3.4 to 5.4			−13.4 to 15.4		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		4.3			14		V
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		−4.2			−13.9		V
A_{VD}	Large-signal differential voltage amplification†	$R_L = 10\ k\Omega$		12			14.3		V/mV
r_i	Input resistance			10^{12}			10^{12}		Ω
c_i	Input capacitance			5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$		87			94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		96			96		dB
P_D	Total power dissipation (four amplifiers)	$V_O = 0$, No load		7.7			26		mW
I_{CC}	Supply current (four amplifiers)	$V_O = 0$, No load		0.77			0.87		mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		120			120		dB

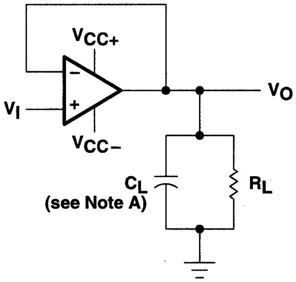
† At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TL034Y operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL034Y						UNIT
				$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1			2		1.5	2.9		V/µs
SR–	Negative slew rate at unity gain				3.9		1.5	5.1		V/µs
t_r	Rise time	$V_{I(PP)} = \pm10$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2			138			132		ns
t_f	Fall time				138			132		ns
	Overshoot factor				11%			5%		
V_n	Equivalent input noise voltage†	$R_S = 20\ \Omega$, See Figure 3	f = 10 kHz		83			83		nV/√Hz
			f = kHz		43			43		
I_n	Equivalent input noise current	f = 1 kHz			0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4			1			1.1		MHz
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 25$ pF, See Figure 4			61°			65°		

† This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate and Overshoot Test Circuit

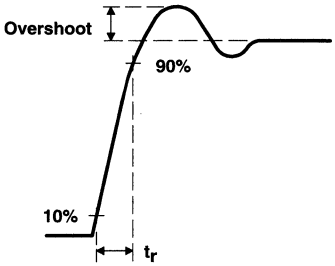


Figure 2. Rise Time and Overshoot Waveform

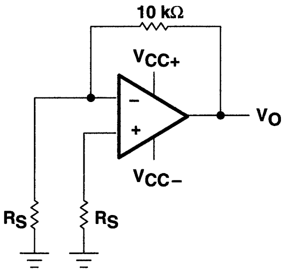
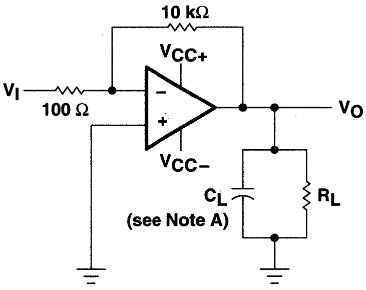


Figure 3. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Unity-Gain Bandwidth and Phase-Margin Test Circuit

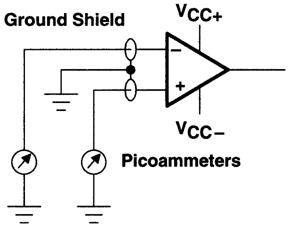


Figure 5. Input-Bias and Offset-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias current level typical of the TL03x and TL03xA, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Contact the factory for details.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6 – 11
α_{VIO}	Input offset voltage temperature coefficient	Distribution	12, 13, 14
I_{IO}	Input offset current	vs Free-air temperature	15
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	15 16
V_{IC}	Common-mode input voltage range	vs Supply voltage vs Free-air temperature	17 18
V_{ID}	Output voltage	vs Differential input voltage	19, 20
V_{OM}	Maximum peak output voltage	vs Supply voltage vs Output current vs Free-air temperature	21 23, 24 25, 26
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	22
A_{VD}	Large-signal differential voltage amplification	vs Load resistance vs Frequency vs Free-air temperature	27 28 29
z_o	Output impedance	vs Frequency	30
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	31, 32 33
k_{SVR}	Supply voltage rejection ratio	vs Free-air temperature	34
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	35 36 37
V_n	Equivalent input noise voltage	vs Frequency	38, 39, 40
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	41, 42, 43 44, 45, 46
SR	Slew rate	vs Load resistance vs Free-air temperature	47, 48 49, 50
	Overshoot factor	vs Load capacitance	51
THD	Total harmonic distortion	vs Frequency	52
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	53 54
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	55 56 57
	Voltage-follower small signal pulse response	vs Time	58
	Voltage-follower large-signal pulse response	vs Time	59, 60
	Phase shift	vs Frequency	28

TYPICAL CHARACTERISTICS

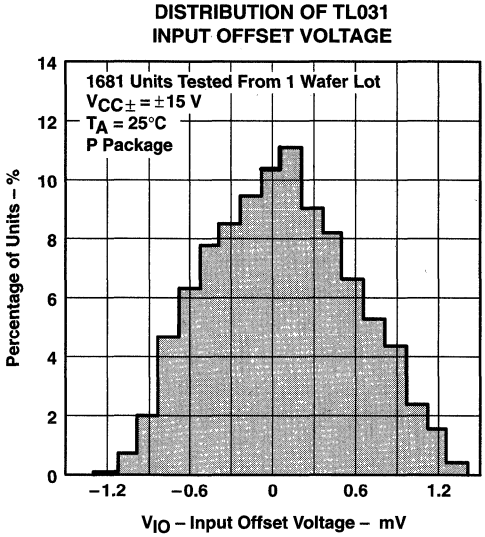


Figure 6

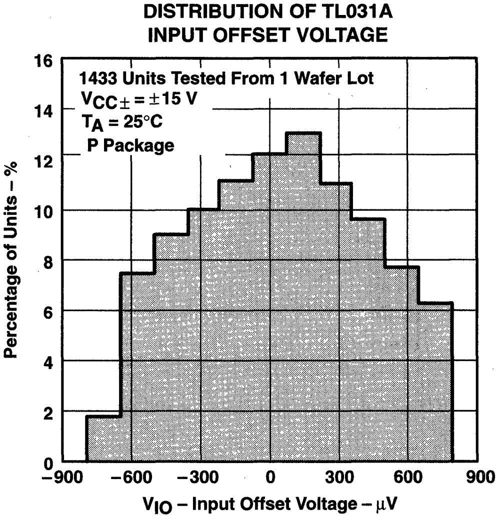


Figure 7

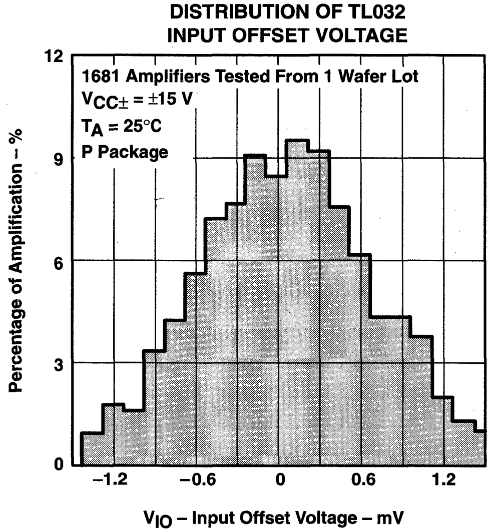


Figure 8

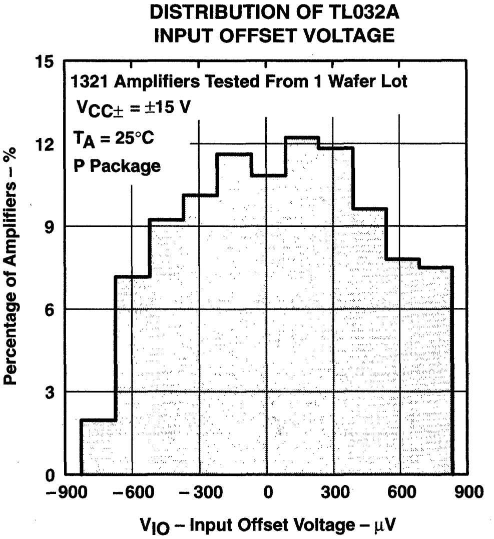


Figure 9

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE

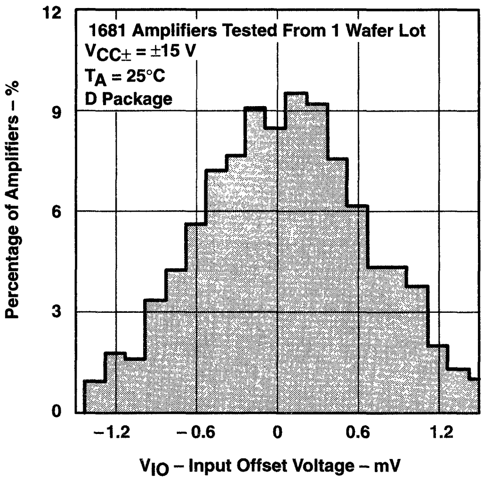


Figure 10

DISTRIBUTION OF TL034A
INPUT OFFSET VOLTAGE

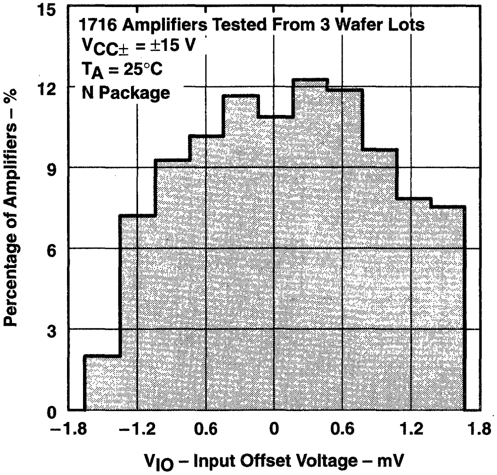


Figure 11

DISTRIBUTION OF TL031
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

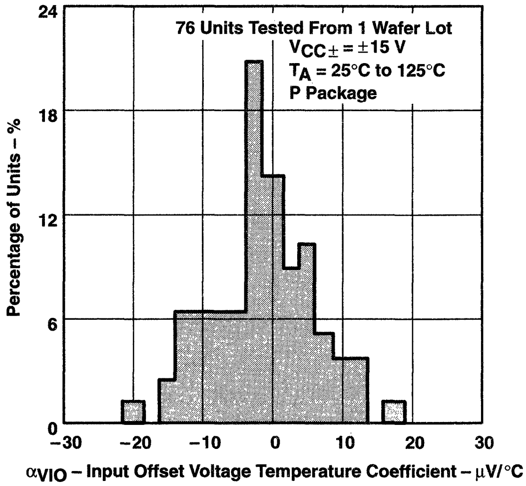


Figure 12

DISTRIBUTION OF TL032
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

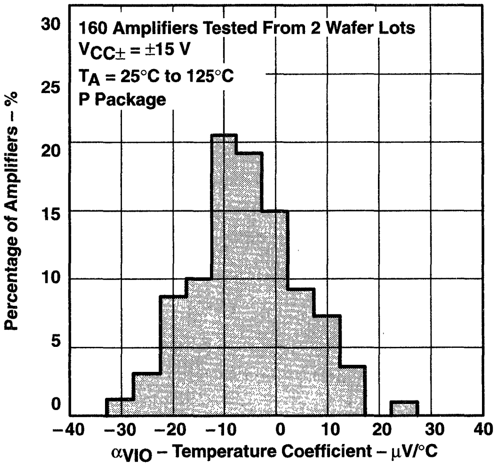


Figure 13

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

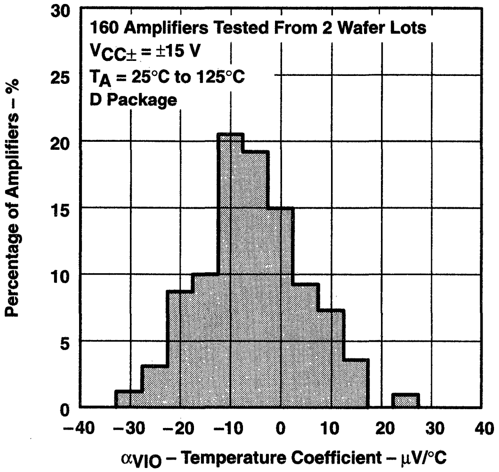


Figure 14

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

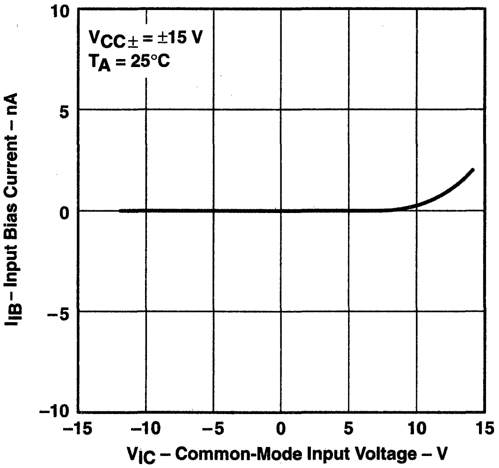


Figure 15

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT†
vs
FREE-AIR TEMPERATURE

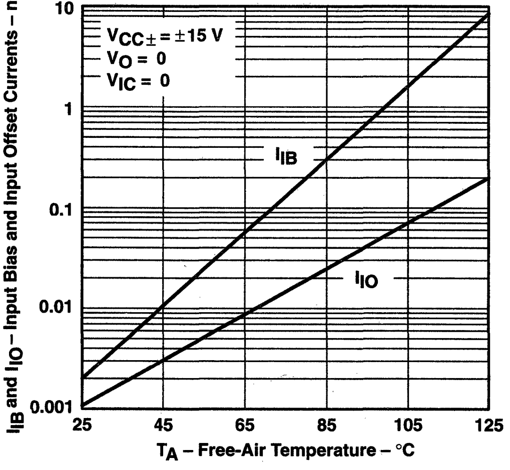


Figure 16

COMMON-MODE INPUT VOLTAGE
vs
SUPPLY VOLTAGE

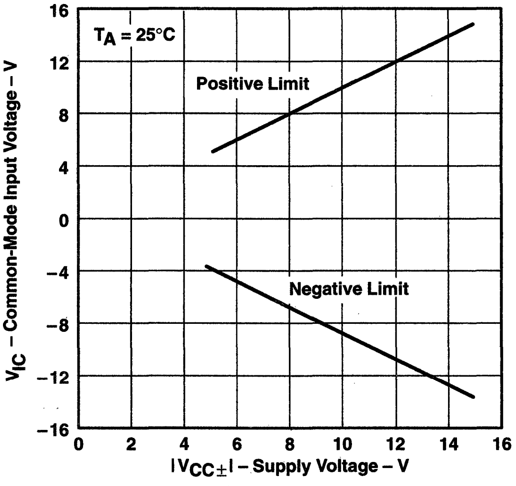


Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

COMMON-MODE INPUT VOLTAGE RANGE†
vs
FREE-AIR TEMPERATURE

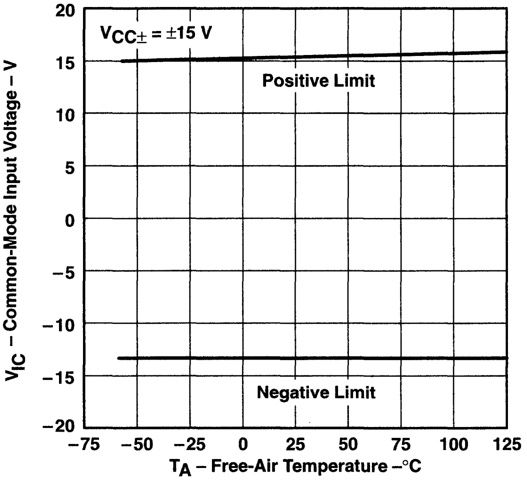

Figure 18

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

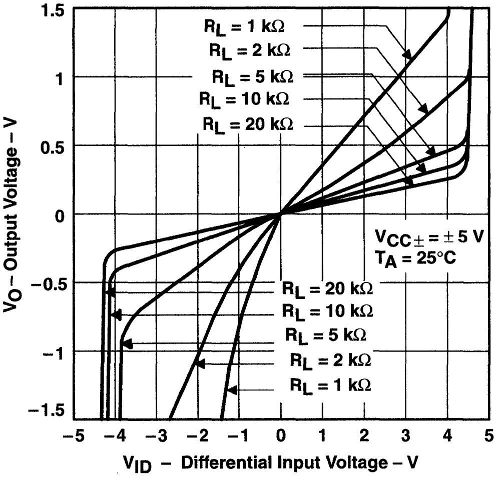

Figure 19

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

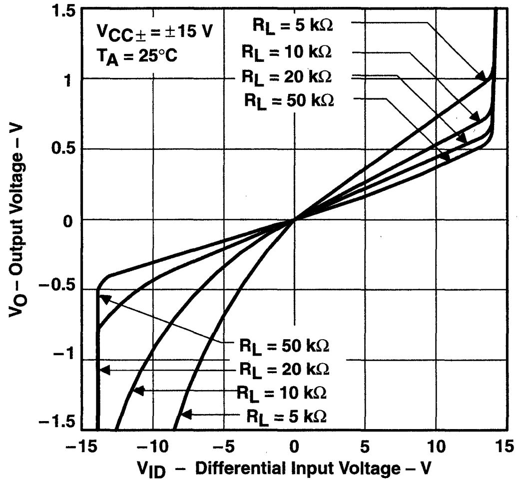

Figure 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

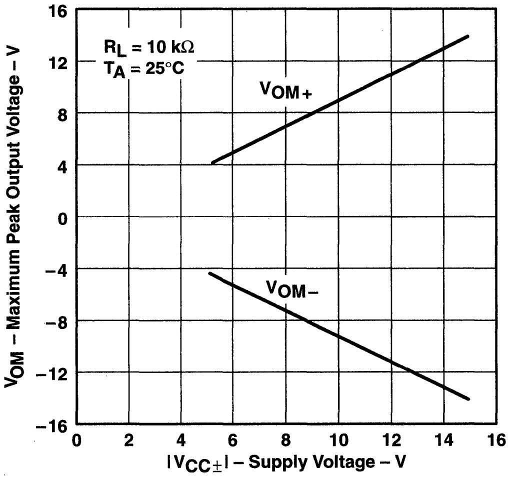

Figure 21

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

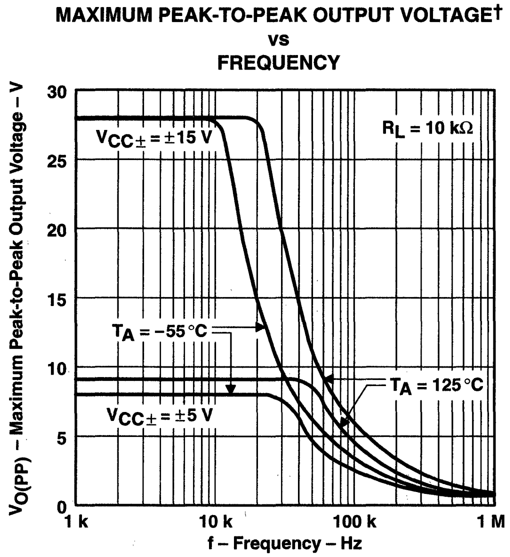

Figure 22

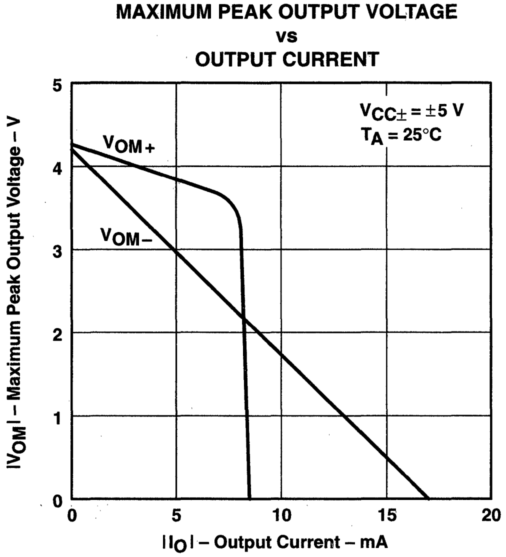

Figure 23

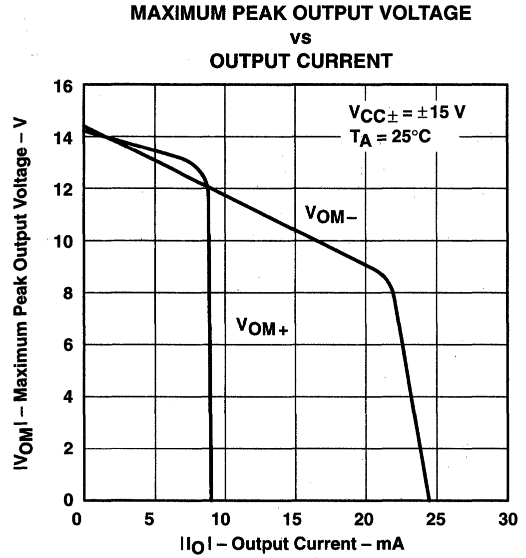

Figure 24

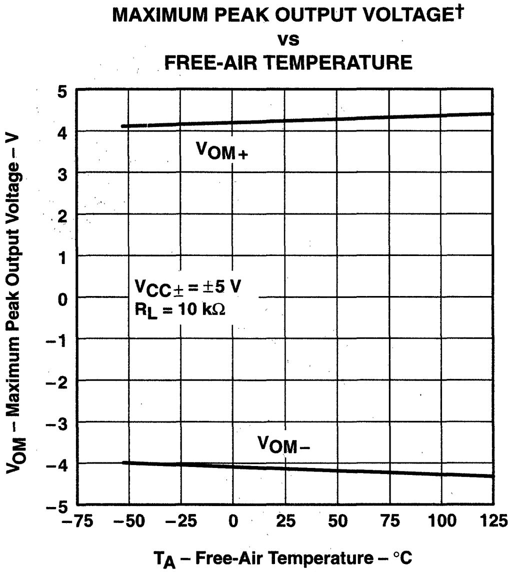

Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE

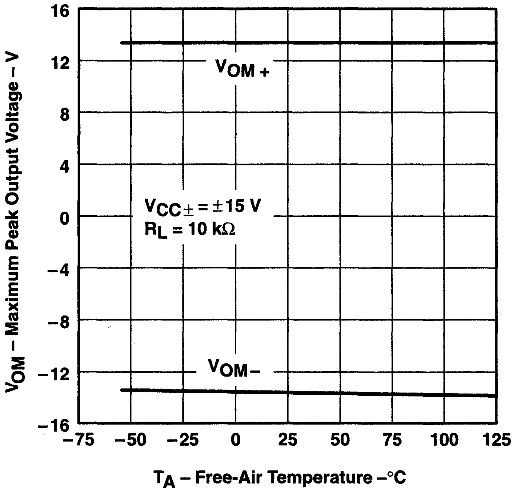

Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

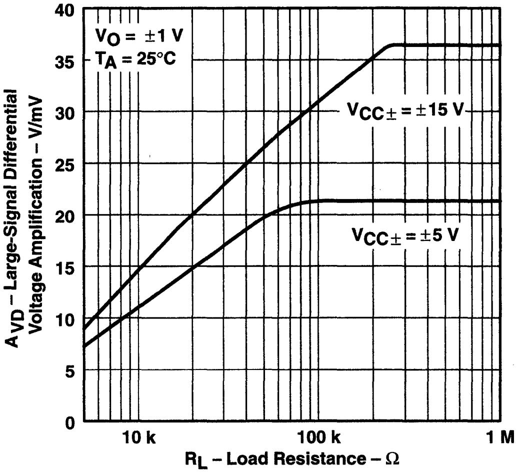

Figure 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

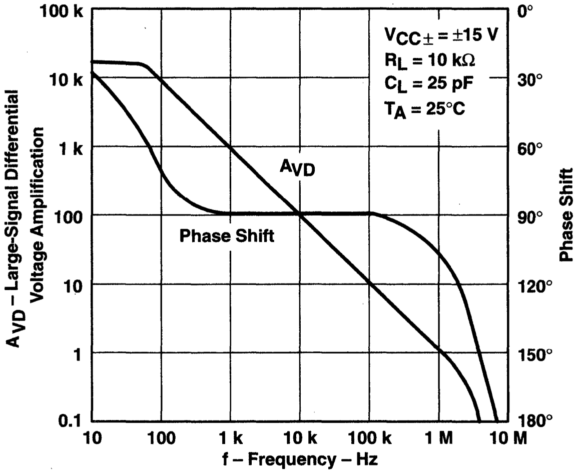

Figure 28

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†
vs
FREE-AIR TEMPERATURE

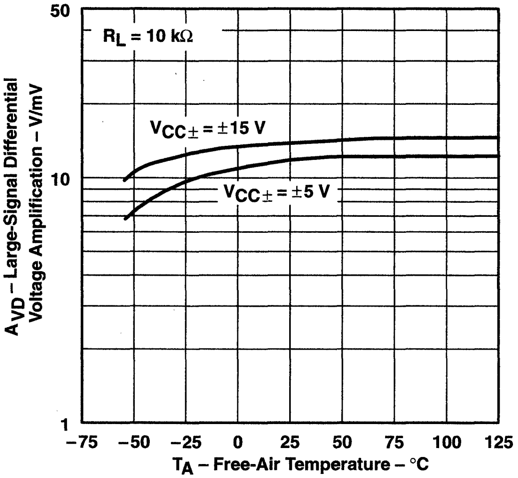

Figure 29

OUTPUT IMPEDANCE
vs
FREQUENCY

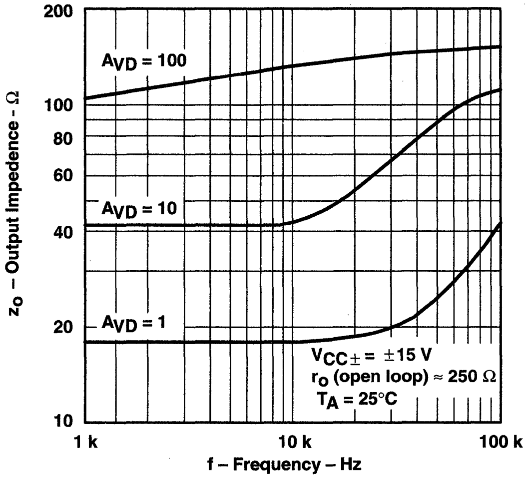

Figure 30

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

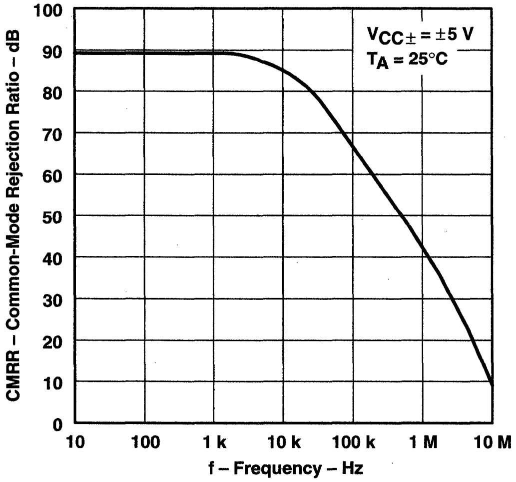

Figure 31

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

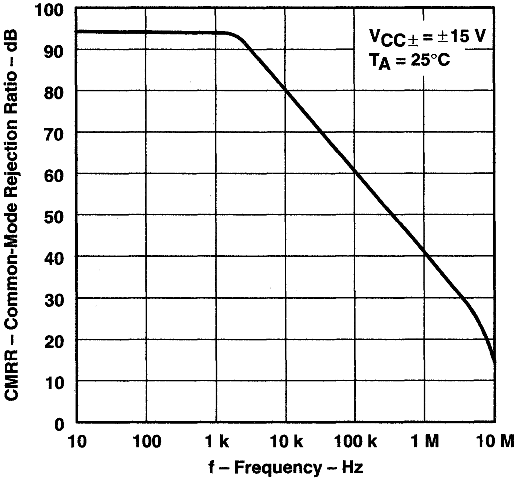

Figure 32

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

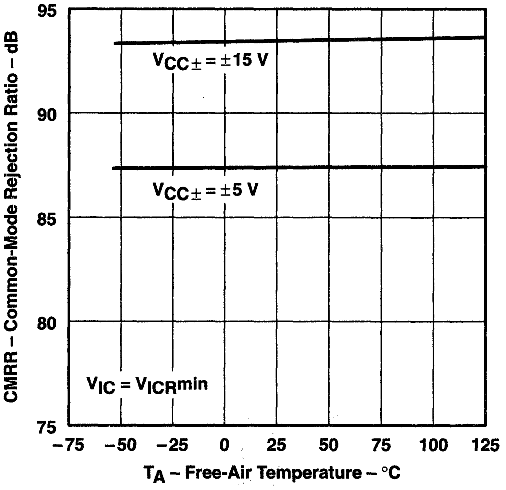
COMMON-MODE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

Figure 33

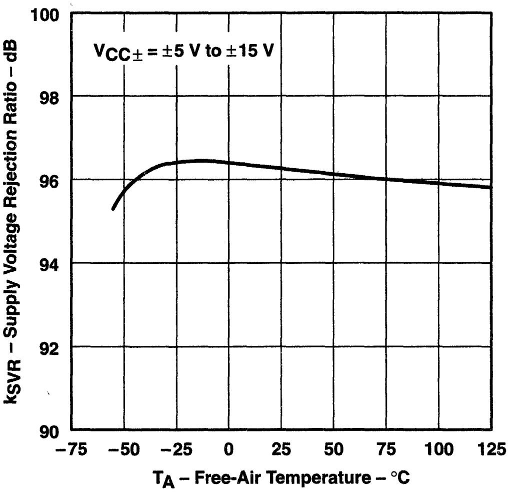
SUPPLY VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

Figure 34

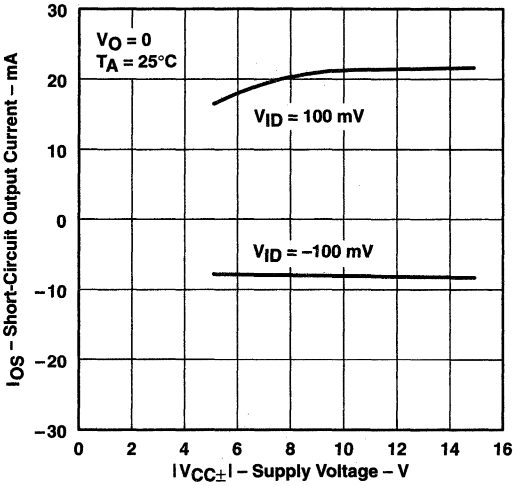
SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

Figure 35

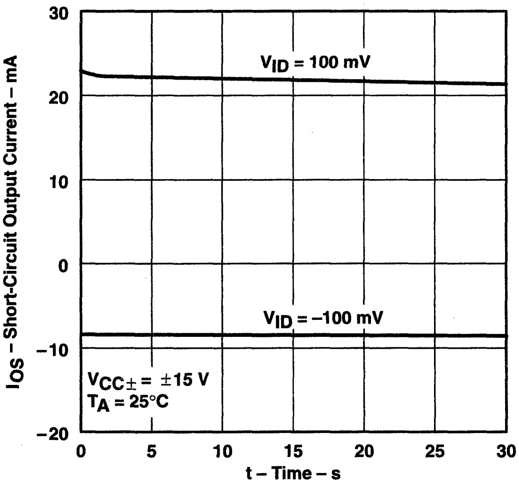
SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

Figure 36

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

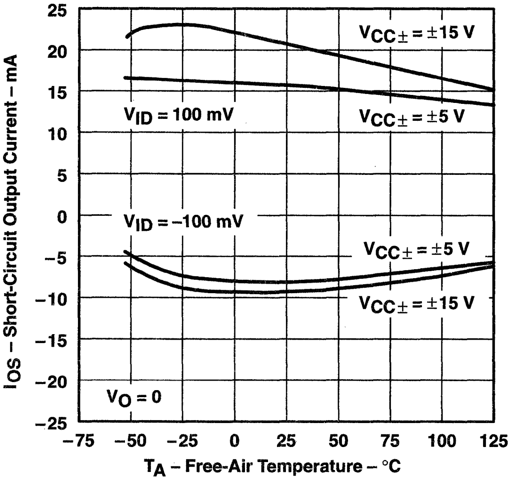

Figure 37

TL031 and TL031A
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

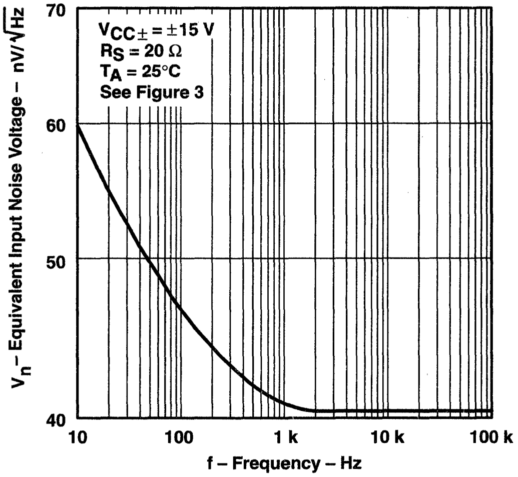

Figure 38

TL032 and TL032A
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

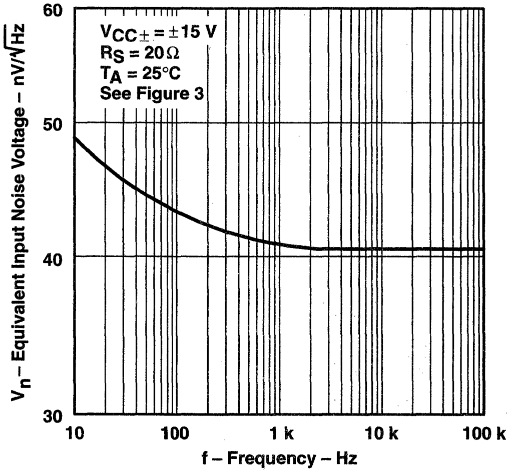

Figure 39

TL034 and TL034A
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

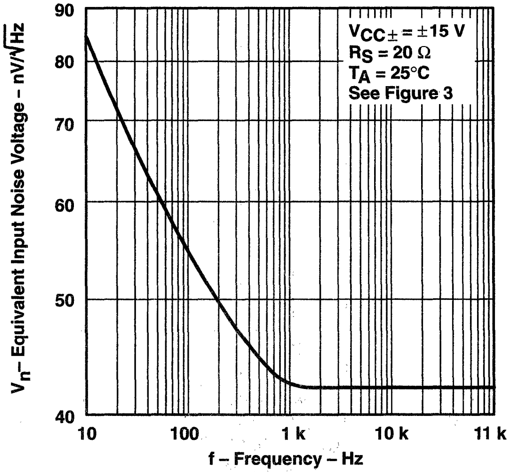

Figure 40

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TL031
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

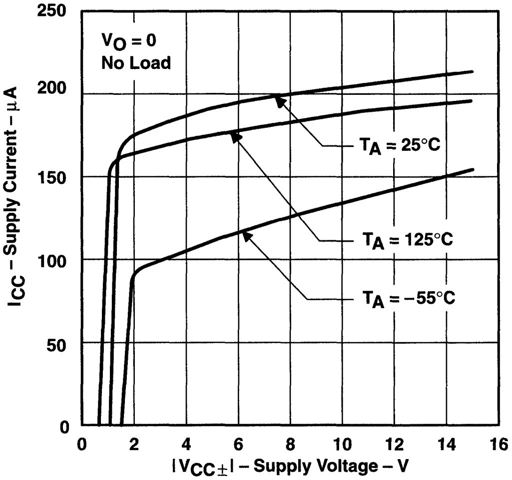

Figure 41

TL032
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

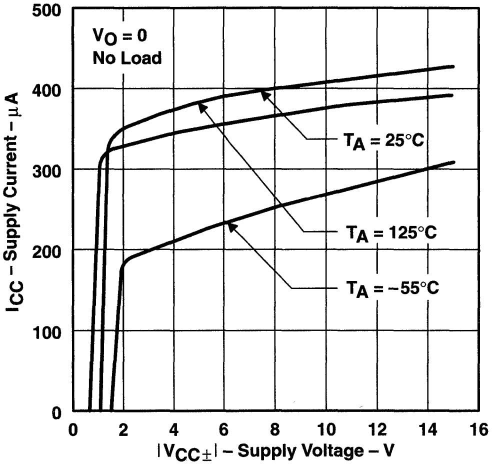

Figure 42

TL034
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

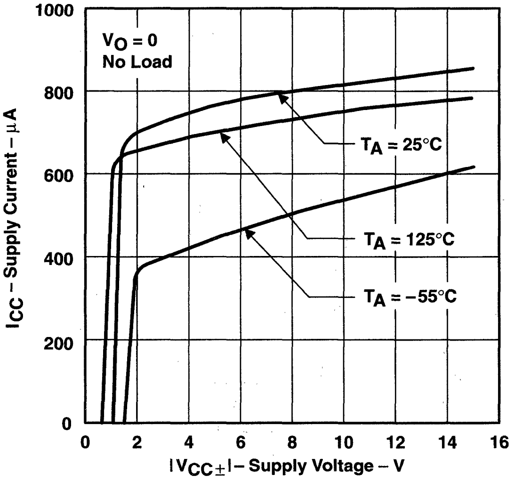

Figure 43

TL031
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

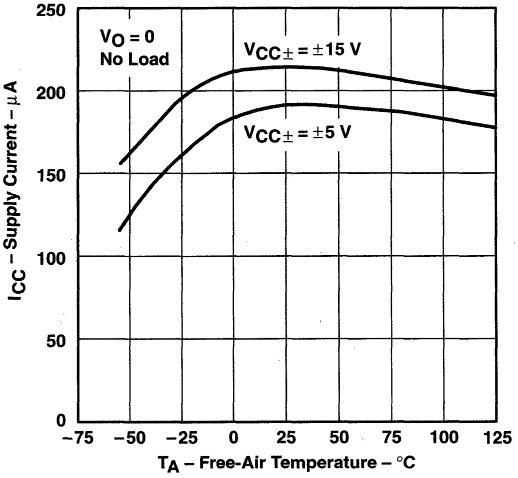

Figure 44

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TL032
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

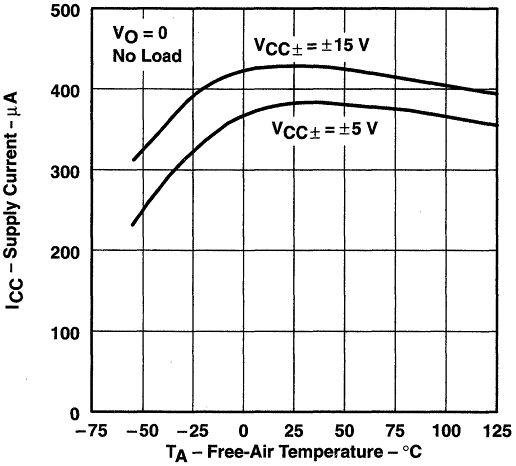

Figure 45

TL034
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

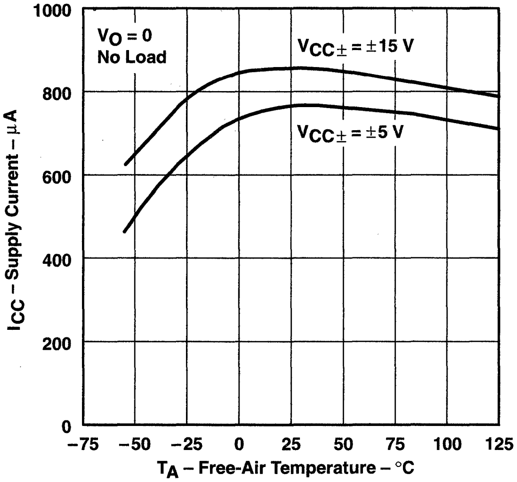

Figure 46

SLEW RATE
vs
LOAD RESISTANCE

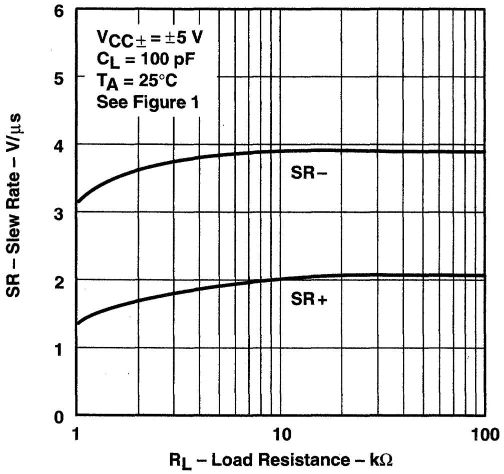

Figure 47

SLEW RATE
vs
LOAD RESISTANCE

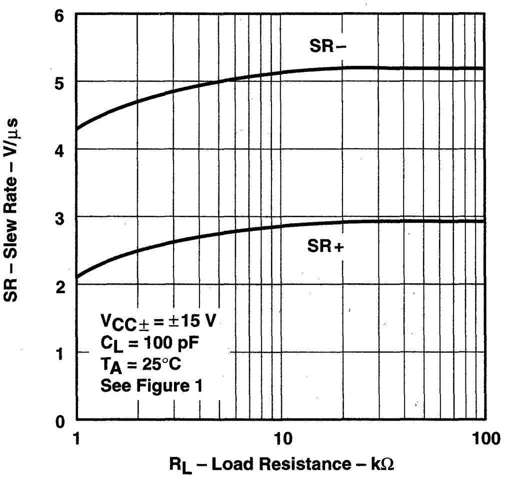

Figure 48

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SLEW RATE†
vs
FREE-AIR TEMPERATURE

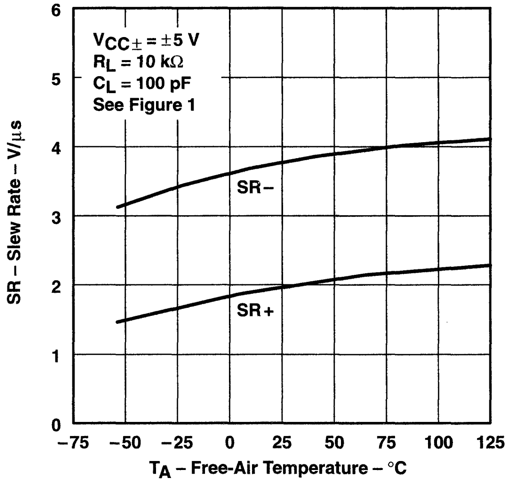

Figure 49

SLEW RATE†
vs
FREE-AIR TEMPERATURE

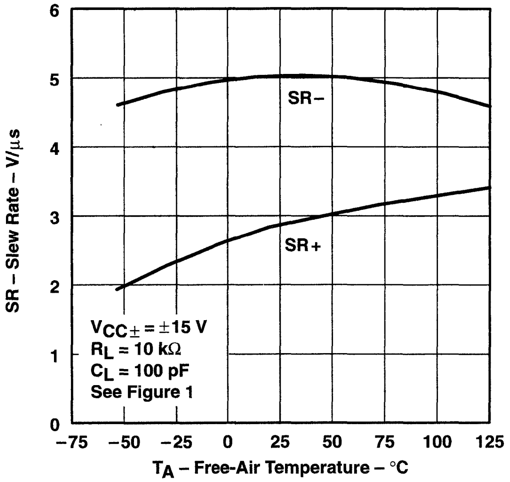

Figure 50

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

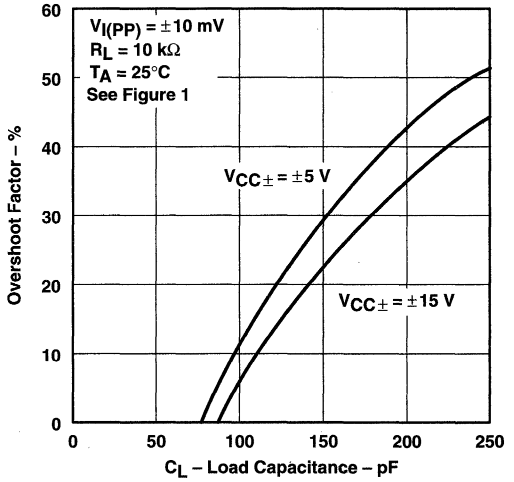

Figure 51

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

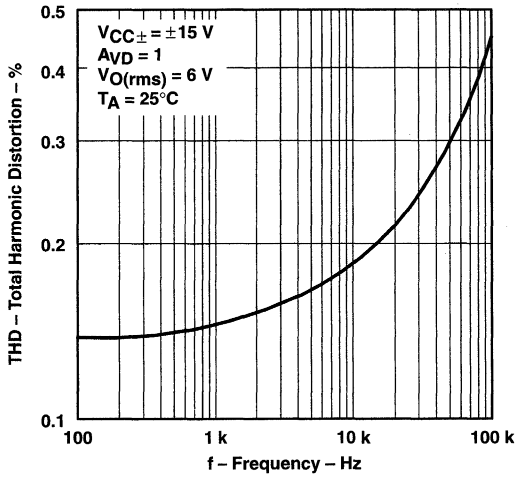

Figure 52

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

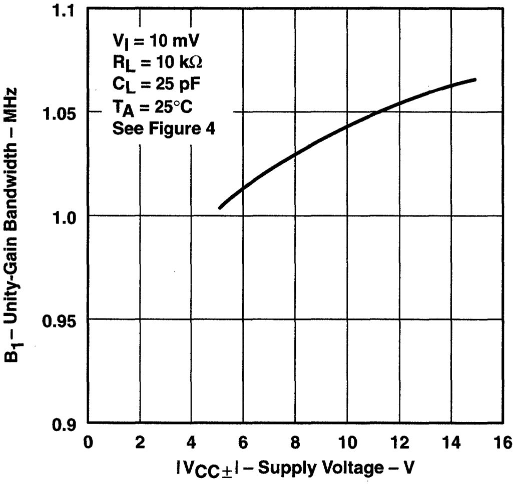


Figure 53

UNITY-GAIN BANDWIDTH†
vs
FREE-AIR TEMPERATURE

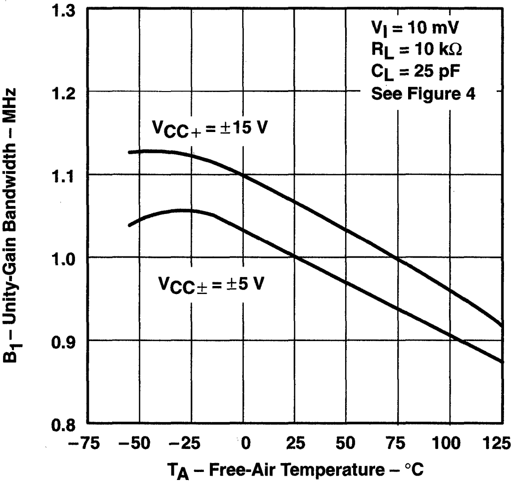


Figure 54

PHASE MARGIN
vs
SUPPLY VOLTAGE

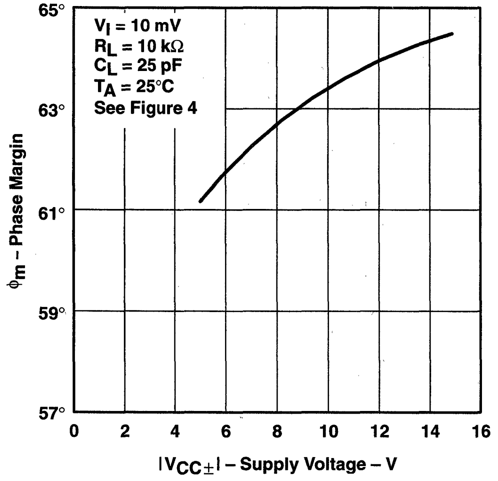
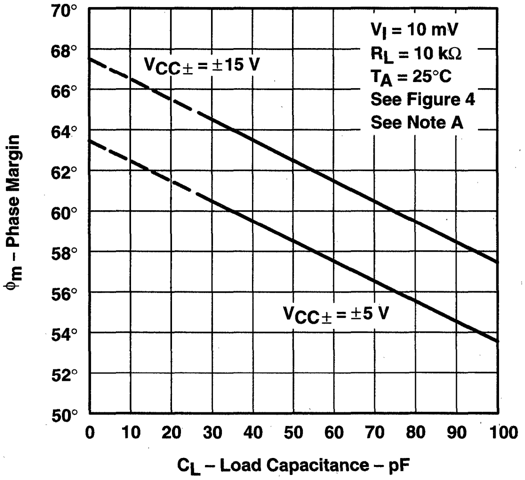


Figure 55

PHASE MARGIN
vs
LOAD CAPACITANCE



NOTE A: Values of phase margin below a load capacitance of 25 pF were estimated.

Figure 56

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN† vs FREE-AIR TEMPERATURE

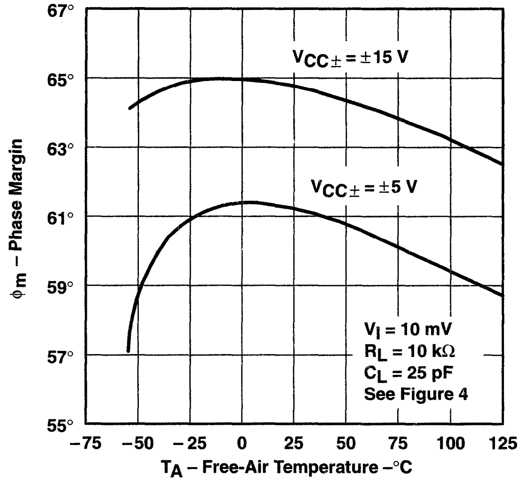

Figure 57

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

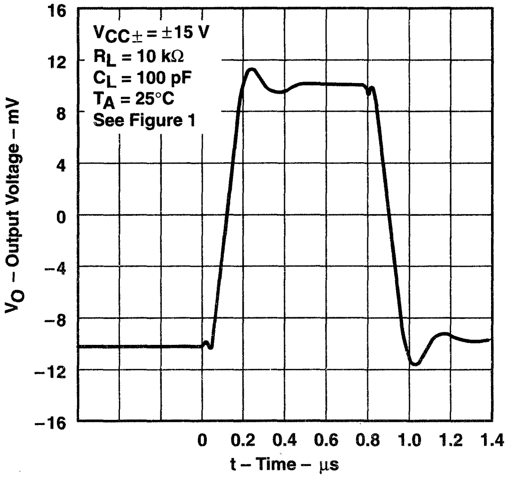

Figure 58

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

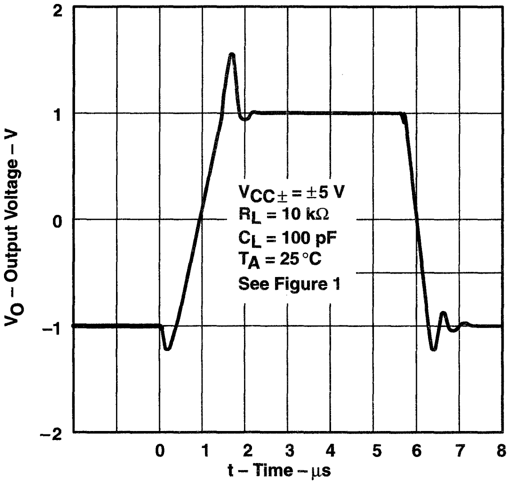

Figure 59

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

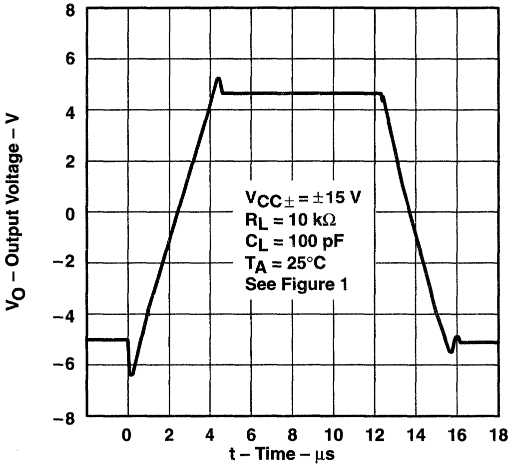

Figure 60

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

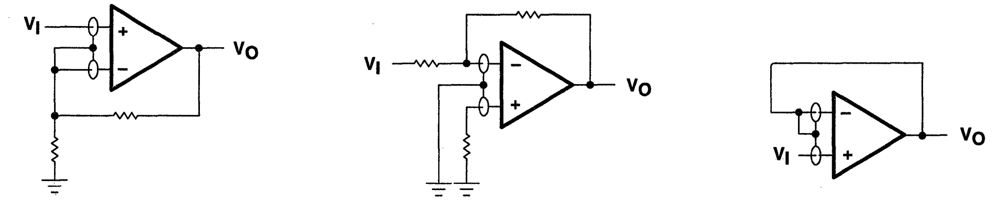
APPLICATION INFORMATION

input characteristics

The TL03x and TL03xA are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Due to of the extremely high input impedance and resulting low bias current requirements, the TL03x and TL03xA are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 61). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.



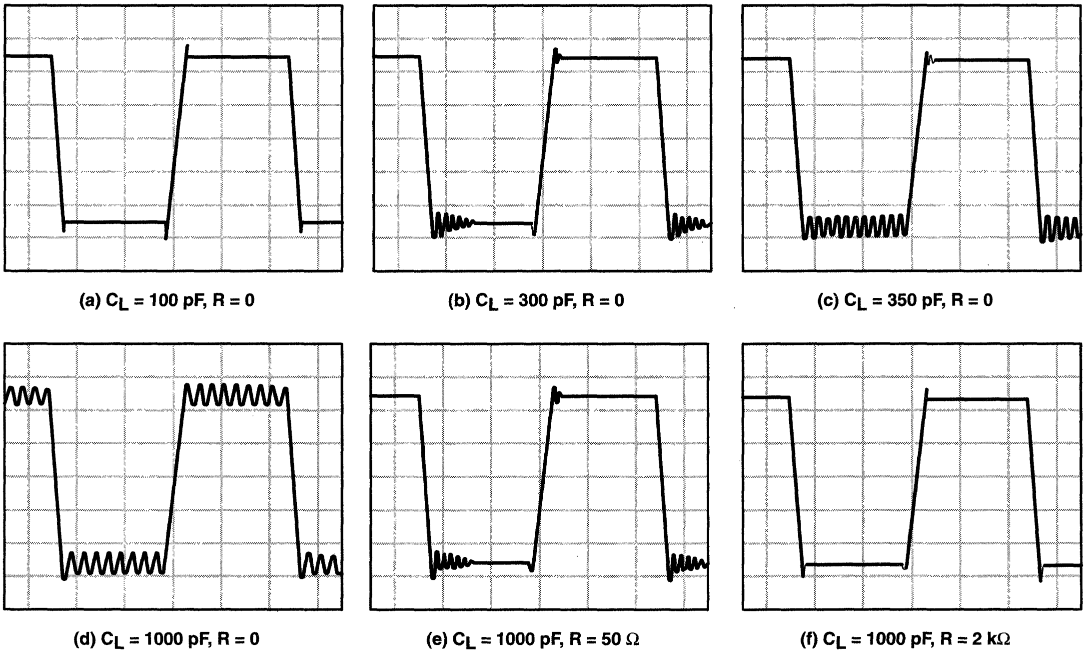
(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 61. Use of Guard Rings

APPLICATION INFORMATION

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL03x and TL03xA drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem (see Figure 63). Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 62).


(a) C_L = 100 pF, R = 0

(b) C_L = 300 pF, R = 0

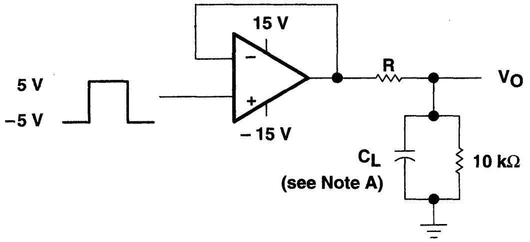
(c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0

(e) C_L = 1000 pF, R = 50 Ω

(f) C_L = 1000 pF, R = 2 kΩ

Figure 62. Effect of Capacitive Loads



NOTE A: C_L includes fixture capacitance.

Figure 63. Test Circuit for Output Characteristics

APPLICATION INFORMATION

high-Q notch filter

In general, Texas Instruments enhanced-JFET operational amplifiers serve as excellent filters. The circuit in Figure 64 provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that are interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_O = \frac{1}{2\pi R1C1}$$

With the resistors and capacitors shown in Figure 64, the center frequency is 1 kHz. C1 = C3 = C2 + 2 and R1 = R3 = 2 x R2. The center frequency can be modified by varying these values. When adjusting the center frequency, ensure that the operational amplifier has sufficient gain at the frequency required.

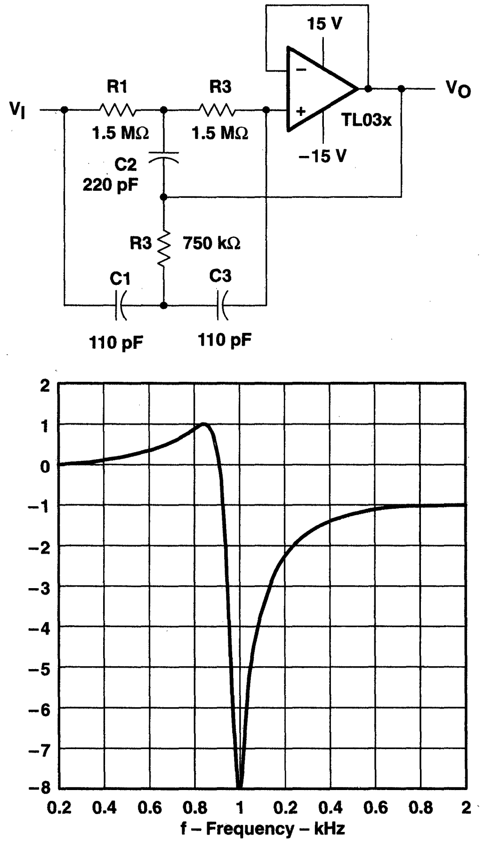


Figure 64. High-Q Notch Filter

APPLICATION INFORMATION

transimpedance amplifier

The low-power precision TL03x allows accurate measurement of low currents. The high input impedance and low offset voltage of the TL03xA greatly simplify the design of a transimpedance amplifier. At room temperature, this design achieves 10-bit accuracy with an error of less than 1/2 LSB.

Assuming that R2 is much less than R1 and ignoring error terms, the output voltage can be expressed as:

$$V_O = -I_{IN} \times R_F\left(\frac{R1 + R2}{R2}\right)$$

Using the resistor values shown in the schematic for a 1-nA input current, the output voltage equals −0.1 V. If the V_O limit for the TL03xA is measured at ± 12 V, the maximum input current for these resistor values is ± 120 nA. Similarly, one LSB on a 10-bit scale corresponds to 12 mV of output voltage, or 120 pA of input current.

The following equation shows the effect of input offset voltage and input bias current on the output voltage:

$$V_O = -\left[V_{IO} + R_F\left(I_{IO} + I_{IB}\right)\right]\left(\frac{R1 + R2}{R2}\right)$$

If the application requires input protection for the transimpedance amplifier, do not use standard PN diodes. Instead, use low-leakage Siliconix SN4117 JFETs (or equivalent) connected as diodes across the TL03xA inputs as shown in Figure 65.

As with all precision applications, special care must be taken to eliminate external sources of leakage and interference. Other precautions include using high-quality insulation, cleaning insulating surfaces to remove fluxes and other residue, and enclosing the application within a protective box.

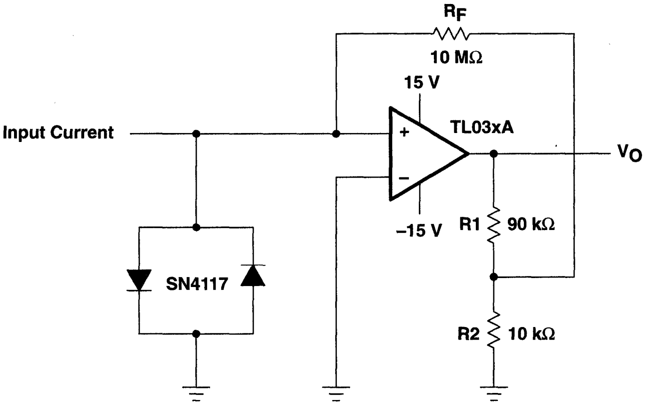


Figure 65. Transimpedance Amplifier

APPLICATION INFORMATION

4-mA to 20-mA current loops

Often, information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The following circuits give two variations of low-power current loops. The circuit in Figure 66 requires three wires from the transmitting to receiving circuitry while the second variation in Figure 67 requires only two wires but includes an extra integrated circuit. Both circuits benefit from the high input impedance of the TL03xA since many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the noninverting input of the TL03xA is zero, the following equation determines the output current:

$$I_O = V_I\left(\frac{R3}{R1 \times R_S}\right) + 5V\left(\frac{R3}{R2 \times R_S}\right) = 0.16 \times V_I + 4mA$$

The circuits presently provide 4-mA to 20-mA output for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3, the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL03xA was chosen:

$$\begin{aligned} I_O &= V_I\left(\frac{R3}{R1 \times R_S}\right) + 5V\left(\frac{R3}{R2 \times R_S}\right) - V_I\left(\frac{R3}{R1 \times R_S} + \frac{R3}{R2 \times R_S} + \frac{R1}{R_S}\right) \\ &= 0.16 \times V_I + 4mA - 0.17 \times V_I \end{aligned}$$

For example, an offset voltage of 1 mV decreases the output current by 0.17 mA.

Due to the low power consumption of the TL03xA, both circuits have at least 2 mA available to drive the actual sensor from the 5-V reference node.

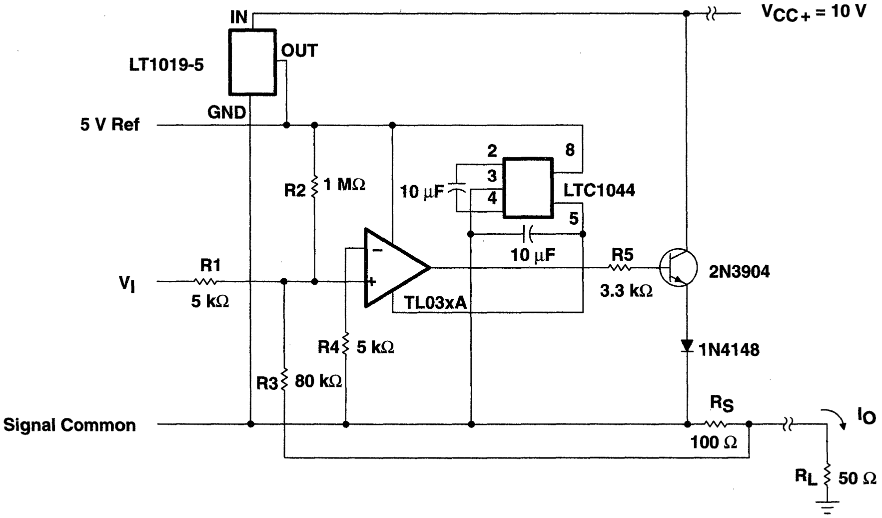


Figure 66. Two-Wire 4-mA to 20-mA Current Loop

APPLICATION INFORMATION

4-mA to 20-mA current loops (continued)

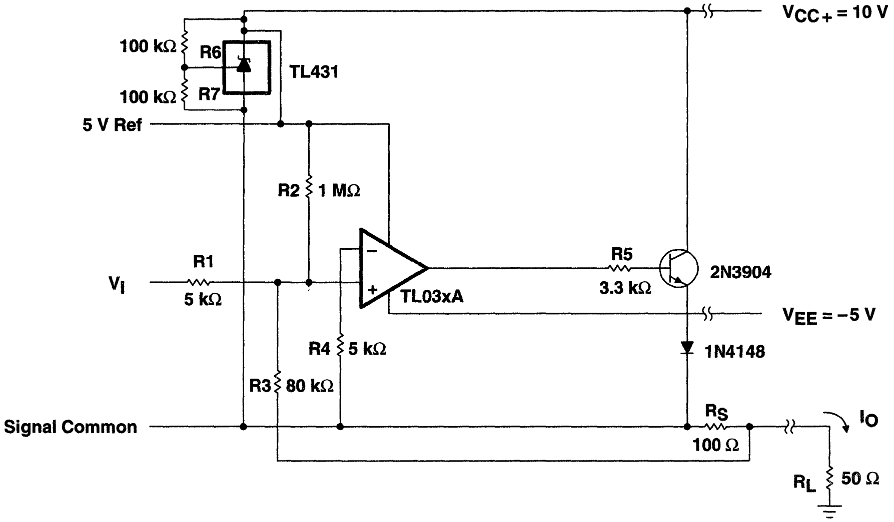


Figure 67. Three-Wire 4-mA to 20-mA Current Loop

APPLICATION INFORMATION

low-level light detector preamplifier

Applications that need to detect small currents require high input-impedance operational amplifiers; otherwise, the bias currents of the operational amplifier camouflage the current being monitored. Phototransistors provide a current that is proportional to the light reaching the transistor. The TL03x allows even the small currents resulting from low-level light to be detected.

In Figure 68, if there is no light, the phototransistor is off and the output is high. As light is detected, the operational amplifier output begins pulling low. Adjusting R4 both compensates for offset voltage of the amplifier and adjusts the point of light detection by the amplifier.

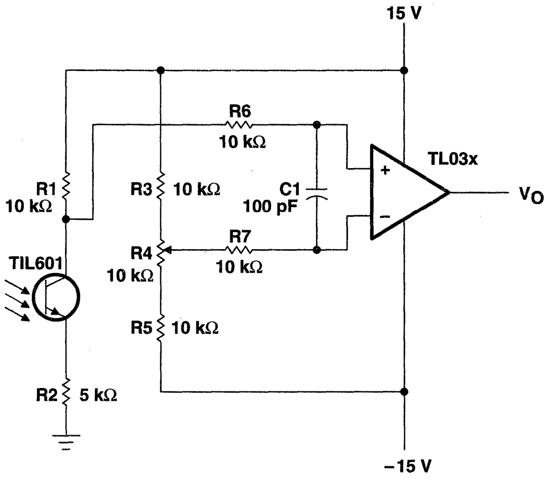
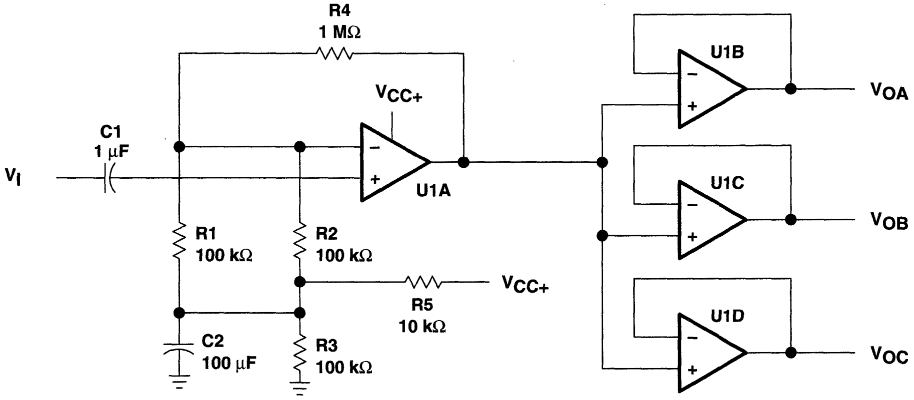


Figure 68. Low-Level Light Detector Preamplifier

APPLICATION INFORMATION

audio-distribution amplifier

This audio-distribution amplifier (see Figure 69) feeds the input signal to three separate output channels. U1A amplifies the input signal with a gain of 10, while U1B, U1C, and U1D serve as buffers to the output channels. The gain response of this circuit is very flat from 20 Hz to 20 kHz. The TL03x allows quick response to the input signal while maintaining low power consumption.



NOTE A: U1A through U1D = TL03x; V_{CC+} = 5 V.

Figure 69. Audio-Distribution Amplifier Circuit

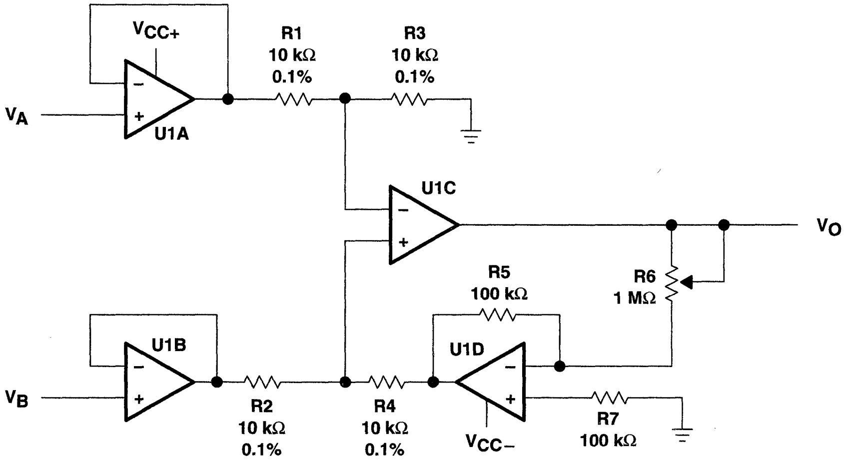
APPLICATION INFORMATION

instrumentation amplifier with linear gain adjust

The low offset voltage and low power consumption of the TL03x provide an accurate but inexpensive instrumentation amplifier (see Figure 70). This particular configuration offers the advantage that the gain can be linearly set by one resistor:

$$V_O = \frac{R6}{R5} \times (V_B - V_A)$$

Adjusting R6 varies the gain. The value of R6 should always be greater or equal to the value of R5 in order to ensure stability. The disadvantage of this instrumentation amplifier topology is the high degree of CMRR degradation resulting from mismatches between R1, R2, R3, and R4. For this reason, these four resistors should be 0.1% tolerance resistors.



NOTE A: U1A through U1D = TL03x; $V_{CC\pm} = \pm 15$ V.

Figure 70. Instrumentation Amplifier With Linear Gain-Adjust Circuit

TL05x, TL05xA, TL05xY
ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS178 – FEBRUARY 1997

- **Direct Upgrades to TL07x and TL08x BiFET Operational Amplifiers**
- **Faster Slew Rate (20 V/μs Typ) Without Increased Power Consumption**
- **On-Chip Offset Voltage Trimming for Improved DC Performance and Precision Grades Are Available (1.5 mV, TL051A)**
- **Available in TSSOP for Small Form-Factor Designs**

description

The TL05x series of JFET-input operational amplifiers offers improved dc and ac characteristics over the TL07x and TL08x families of BiFET operational amplifiers. On-chip zener trimming of offset voltage yields precision grades as low as 1.5 mV (TL051A) for greater accuracy in dc-coupled applications. Texas Instruments improved BiFET process and optimized designs also yield improved bandwidth and slew rate without increased power consumption. The TL05x devices are pin-compatible with the TL07x and TL08x and can be used to upgrade existing circuits or for optimal performance in new designs.

BiFET operational amplifiers offer the inherently higher input impedance of the JFET-input transistors, without sacrificing the output drive associated with bipolar amplifiers. This makes them better suited for interfacing with high-impedance sensors or very low-level ac signals. They also feature inherently better ac response than bipolar or CMOS devices having comparable power consumption.

The TL05x family was designed to offer higher precision and better ac response than the TL08x with the low noise floor of the TL07x. Designers requiring significantly faster ac response or ensured lower noise should consider the Excalibur TLE208x and TLE207x families of BiFET operational amplifiers.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES						CHIP FORM‡ (Y)
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	
0°C to 70°C	800 μV	TL051ACD TL052ACD	—	—	—	—	TL051ACP TL052ACP	TL051Y TL052Y TL054Y
	1.5 mV	TL051CD TL052CD TL054ACD	—	—	—	TL054ACN	TL051CP TL052CP	
	4 mV	TL054CD	—	—	—	TL054CN	—	
−40°C to 85°C	800 μV	TL051AID TL052AID	—	—	—	—	TL051AIP TL052AIP	—
	1.5 mV	TL051ID TL052ID TL054AID	—	—	—	TL054AIN	TL051IP TL052IP	
	4 mV	TL054ID	—		—	TL054IN	—	
−55°C to 125°C	800 μV	TL051AMD TL052AMD	TL051AMFK TL052AMFK	—	TL051AMJG TL052AMJG	—	TL051AMP TL052AMP	—
	1.5 mV	TL051MD TL052MD TL054AMD	TL051MFK TL052MFK TL054AMFK	TL054AMJ	TL051MJG TL052MJG	TL054AMN	TL051MP TL052MP	
	4 mV	TL054MD	TL054MFK	TL054MJ	—	TL054MN	—	

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TL054CDR).

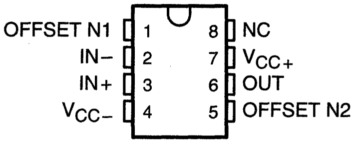
‡ Chip forms are tested at 25°C.

description (continued)

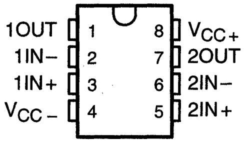
Because BiFET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required and loads should be terminated to a virtual-ground node at midsupply. Texas Instruments TLE2426 integrated virtual ground generator is useful when operating BiFET amplifiers from single supplies.

The TL05x are fully specified at ±15 V and ±5 V. For operation in low-voltage and/or single-supply systems, Texas Instruments LinCMOS families of operational amplifiers (TLC-prefix) are recommended. When moving from BiFET to CMOS amplifiers, particular attention should be paid to the slew rate and bandwidth requirements, and also the output loading.

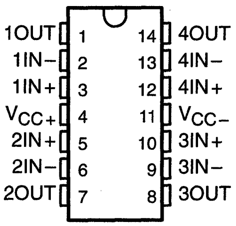
TL051
D, JG, OR P PACKAGE
(TOP VIEW)



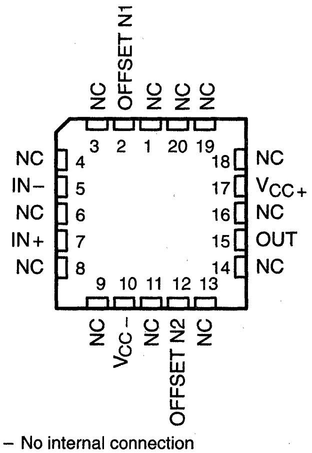
TL052
D, JG, OR P PACKAGE
(TOP VIEW)



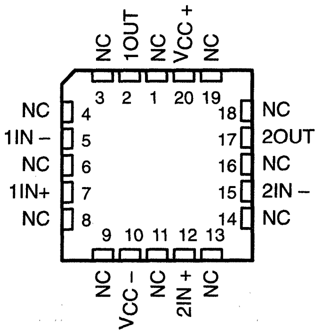
TL054
D, J, OR N PACKAGE
(TOP VIEW)



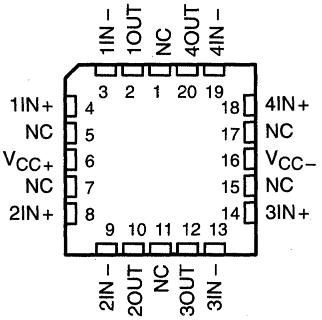
TL051
FK PACKAGE
(TOP VIEW)



TL052
FK PACKAGE
(TOP VIEW)

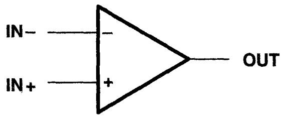


TL054
FK PACKAGE
(TOP VIEW)

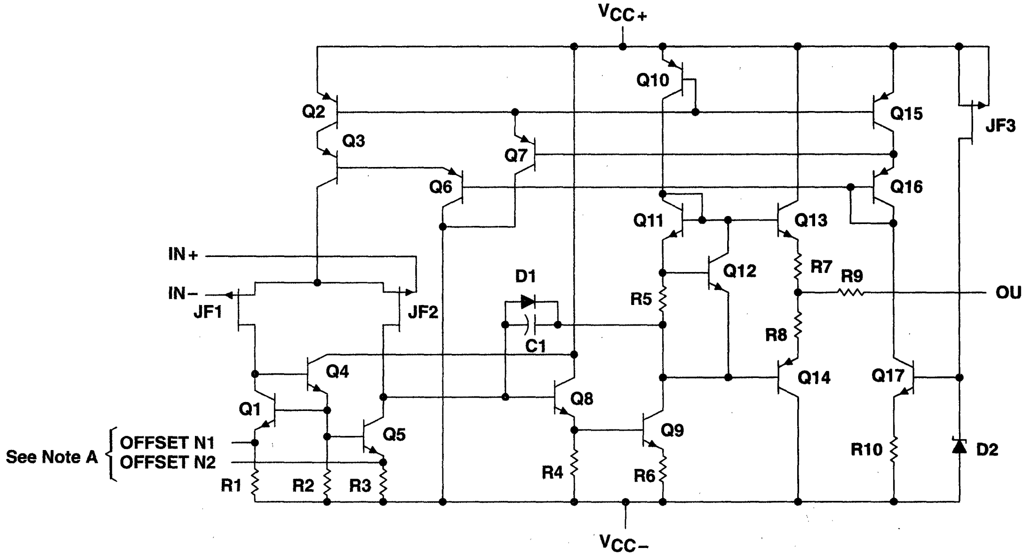


NC – No internal connection

symbol (each amplifier)



equivalent schematic (each amplifier)



NOTE A: OFFSET N1 and OFFSET N2 are only available on the TL051x.

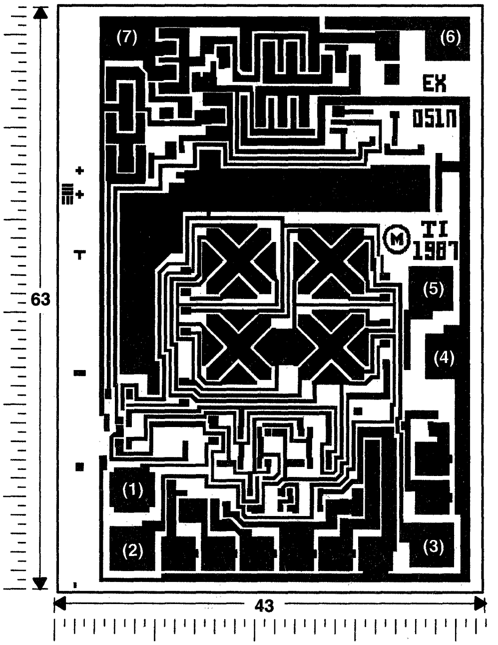
ACTUAL DEVICE COMPONENT COUNT†			
COMPONENT	**TL051**	**TL052**	**TL054**
Transistors	20	34	62
Resistors	10	19	37
Diodes	2	3	5
Capacitors	1	2	4

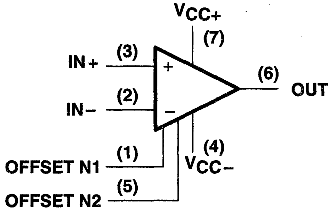
† These figures include all four amplifiers and all ESD, bias, and trim circuitry.

TL051Y chip information

This chip, when properly assembled, displays characteristics similar to the TL051. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

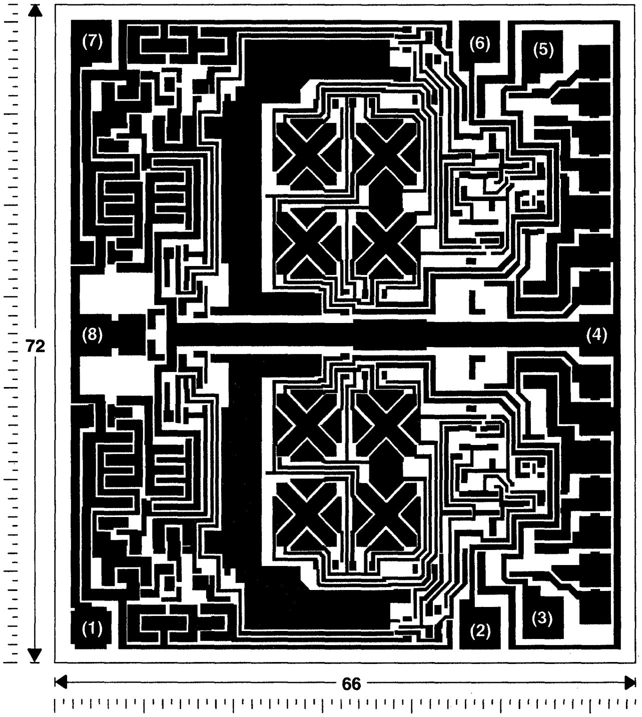
ALL DIMENSIONS ARE IN MILS.

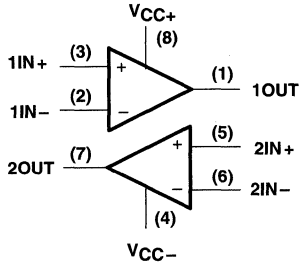
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TL052Y chip information

This chip, when properly assembled, displays characteristics similar to the TL052. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

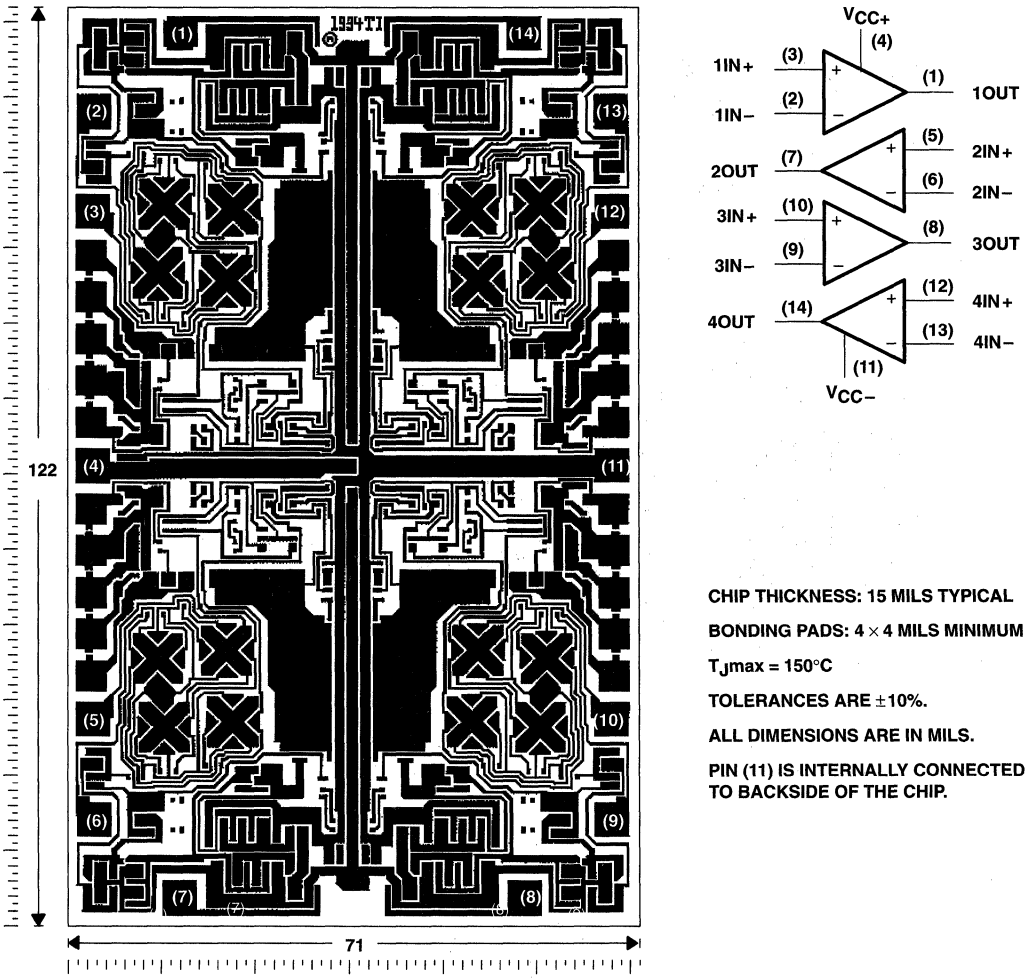
ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TL054 chip information

This chip, when properly assembled, displays characteristics similar to the TL054C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. These chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	−18 V
Differential input voltage (see Note 2)	±30 V
Input voltage range, V_I (any input, see Notes 1 and 3)	±15 V
Input current, I_I (each input)	±1 mA
Output current, I_O (each output)	±80 mA
Total current into V_{CC+}	160 mA
Total current out of V_{CC-}	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16inch) from case for 10 seconds: D, N, or P package	260°C
Lead temperature 1,6 mm (1/16inch) from case for 60 seconds: J or JG package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	315 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±5	±15	±5	±15	±5	±15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm5$ V	−1	4	−1	4	−1	4	V
	$V_{CC\pm} = \pm15$ V	−11	11	−11	11	−11	11	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

TEXAS INSTRUMENTS

TL051C and TL051AC electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL051C, TL051AC						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051C	25°C		0.75	3.5		0.59	1.5	mV
				Full range			4.5			2.5	
			TL051AC	25°C		0.55	2.8		0.35	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage‡		TL051C	25°C to 70°C		8			8		µV/°C
			TL051AC	25°C to 70°C		8			8	25	
	Input offset voltage long-term drift§			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification¶	$R_L = 2\ k\Omega$		25°C	25	59		50	105		V/mV
				0°C	30	65		60	129		
				70°C	20	46		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	98		75	98		
				70°C	75	97		75	97		
I_{CC}	Supply current	$V_O = 0$, No load		25°C		2.6	3.2		2.7	3.2	mA
				0°C		2.7	3.2		2.8	3.2	
				70°C		2.6	3.2		2.7	3.2	

† Full range is 0°C to 70°C.

‡ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ For $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V, or for $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TL051C and TL051AC operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL051C, TL051AC						UNIT
					$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain‡	R_L = 2 kΩ, See Figure 1	C_L = 100 pF,	25°C		16		13	20		V/µs
				Full range		16.4		11	22.6		
SR−	Negative slew rate at unity gain‡			25°C		15		13	18		
				Full range		16		11	19.3		
t_r	Rise time	$V_{I(PP)}$ = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage§	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			18	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion¶	R_S = 1 kΩ, f = 1 kHz	R_L = 2 kΩ,	25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 4	25°C		3			3.1		MHz
				0°C		3.2			3.3		
				70°C		2.7			2.8		
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 4	25°C		59°			62°		
				0°C		58°			62°		
				70°C		59°			62°		

† Full range is 0°C to 70°C.

‡ For $V_{CC\pm}$ = ±5 V, $V_{I(PP)}$ = ±1 V; for $V_{CC\pm}$ = ±15 V, $V_{I(PP)}$ = ±5 V.

§ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For $V_{CC\pm}$ = ±5 V, V_{Orms} = 1 V; for $V_{CC\pm}$ = ±15 V, V_{Orms} = 6 V.

TL051I and TL051AI electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL051I, TL051AI						UNIT
					$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL051I	25°C		0.75	3.5		0.59	1.5	mV
				Full range			5.3			3.3	
			TL051AI	25°C		0.55	2.8		0.35	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage‡		TL051I	25°C to 85°C		7			8		μV/°C
			TL051AI	25°C to 85°C		8			8	25	
	Input offset voltage long-term drift§			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification¶	R_L = 2 kΩ		25°C	25	59		50	105		V/mV
				−40°C	30	74		60	145		
				85°C	20	43		30	76		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω		25°C	65	85		75	93		dB
				−40°C	65	83		75	90		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current	V_O = 0,	No load	25°C		2.6	3.2		2.7	3.2	mA
				−40°C		2.4	3.2		2.6	3.2	
				85°C		2.5	3.2		2.6	3.2	

† Full range is −40°C to 85°C

‡ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V, or for $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

TL051I and TL051AI operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TL051I, TL051AI						UNIT
				$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain‡	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1	25°C		16		13	20		V/µs
			Full range				11			
SR−	Negative slew rate at unity gain‡		25°C		15		13	18		
			Full range				11			
t_r	Rise time	$V_{I(PP)} = \pm10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2	25°C		55			56		ns
			−40°C		52			53		
			85°C		64			65		
t_f	Fall time		25°C		55			57		
			−40°C		51			53		
			85°C		64			65		
	Overshoot factor		25°C		24%			19%		
			−40°C		24%			19%		
			85°C		24%			19%		
V_n	Equivalent input noise voltage§	$R_S = 20$ Ω, See Figure 3, f = 10 Hz	25°C		75			75		nV/√Hz
		$R_S = 20$ Ω, See Figure 3, f = 1 kHz	25°C		18			18	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$R_S = 20$ Ω, See Figure 3, f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion¶	$R_S = 1$ kΩ, $R_L = 2$ kΩ, f = 1 kHz	25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4	25°C		3			3.1		MHz
			−40°C		3.5			3.6		
			85°C		2.6			2.7		
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4	25°C		59°			62°		
			−40°C		58°			61°		
			85°C		59°			62°		

† Full range is −40°C to 85°C.

‡ For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

§ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For $V_{CC\pm} = \pm5$ V, $V_{Orms} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{Orms} = 6$ V.

TL051M and TL051AM electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL051M, TL051AM						UNIT
					$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051M	25C		0.75	3.5		0.59	1.5	mV
				Full range			6.5			4.5	
			TL051AM	25°C		0.55	2.8		0.35	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL051M	25°C to 125°C		8			8		µV/°C
			TL051AM	25°C to 125°C		8			8		
	Input offset voltage long-term drift‡			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification§	$R_L = 2\ k\Omega$		25°C	25	59		50	105		V/mV
				−55°C	30	76		60	149		
				125°C	10	32		15	49		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$,	$R_S = 50\ \Omega$	25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current	$V_O = 0$,	No load	25°C		2.6	3.2		2.7	3.2	mA
				−55°C		2.3	3.2		2.4	3.2	
				125°C		2.4	3.2		2.5	3.2	

† Full range is −55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V, or for $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

TL051M and TL051AM operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TL051M, TL051AM						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain[†]	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		25°C		16		13	20		V/μs
SR−	Negative slew rate at unity gain[†]			25°C		15		13			
t_r	Rise time	$V_{I(PP)} = \pm10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		55			56		ns
				−55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				−55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				−55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage[‡]	$R_S = 20$ Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion[§]	$R_S = 1$ kΩ, $R_L = 2$kΩ, f = 1 kHz		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		3			3.1		MHz
				−55°C		3.6			3.7		
				125°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		59°			62°		
				−55°C		57°			61°		
				125°C		59°			62°		

[†] For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

[‡] This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[§] For $V_{CC\pm} = \pm5$ V, V_{O}rms = 1 V; for $V_{CC\pm} = \pm15$ V, V_{O}rms = 6 V.

TL051Y electrical characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TL051Y $V_{CC\pm} = \pm 5$ V MIN	TYP	MAX	TL051Y $V_{CC\pm} = \pm 15$ V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$		0.75			0.59		mV
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		4			5		pA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		20			30		pA
V_{ICR}	Common-mode input voltage range			−2.3 to 5.6			−12.3 to 15.6		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		4.2			13.9		V
		$R_L = 2\ k\Omega$		3.8			12.7		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		−3.5			−13.2		V
		$R_L = 2\ k\Omega$		−3.2			−12		
A_{VD}	Large-signal differential voltage amplification†	$R_L = 2\ k\Omega$		59			105		V/mV
r_i	Input resistance			10^{12}			10^{12}		Ω
c_i	Input capacitance			10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $V_O = 0$, $R_S = 50\ \Omega$		85			93		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		99			99		dB
I_{CC}	Supply current	$V_O = 0$, No load		2.6			2.7		mA

† For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V, or for $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

TL051Y operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TL051Y						UNIT
				$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain[†]	R_L = 2 kΩ, C_L = 100 pF, See Figure 1			16			20		V/μs
SR−	Negative slew rate at unity gain[†]				15			18		
t_r	Rise time	$V_{I(PP)}$ = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2			55			56		ns
t_f	Fall time				55			57		
	Overshoot factor				24%			19%		
V_n	Equivalent input noise voltage[‡]	R_S = 20 Ω, See Figure 3	f = 10 Hz		75			75		nV/√Hz
			f = 1 kHz		18			18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz			0.01			0.01		pA/√Hz
THD	Total harmonic distortion[§]	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz			0.003%			0.003%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4			3			3.1		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4			59°			62°		

[†] For $V_{CC\pm}$ = ±5 V, $V_{I(PP)}$ = ±1 V; for $V_{CC\pm}$ = ±15 V, $V_{I(PP)}$ = ±5 V.

[‡] This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[§] For $V_{CC\pm}$ = ±5 V, V_{O}rms = 1 V; for $V_{CC\pm}$ = ±15 V, V_{O}rms = 6 V.

TL052C and TL052AC electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL052C, TL052AC						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052C	25°C		0.73	3.5		0.65	1.5	mV
				Full range			4.5			2.5	
			TL052AC	25°C		0.51	2.8		0.4	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage‡		TL052C	25°C to 70°C		8			8		µV/°C
			TL052AC	25°C to 70°C		8			6	25	
	Input offset voltage long-term drift§	$V_O = 0$, $R_S = 50\ \Omega$	$V_{IC} = 0$,	25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, See Figure 5	$V_{IC} = 0$,	25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, See Figure 5	$V_{IC} = 0$,	25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification¶	$R_L = 2\ k\Omega$		25°C	25	59		50	105		V/mV
				0°C	30	65		60	129		
				70°C	20	46		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$,	$R_S = 50\ \Omega$	25°C	65	85		75	93		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		

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† Full range is 0°C to 70°C.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ For $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TL052C and TL052AC electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS	T_A	TL052C, TL052AC $V_{CC\pm} = \pm5$ V MIN	TYP	MAX	TL052C, TL052AC $V_{CC\pm} = \pm15$ V MIN	TYP	MAX	UNIT
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$	25°C	75	99		75	99		dB
			0°C	75	98		75	98		
			70°C	75	97		75	97		
I_{CC}	Supply current (two amplifiers)	$V_O = 0$, No load	25°C		4.6	5.6		4.8	5.6	mA
			0°C		4.7	6.4		4.8	6.4	
			70°C		4.4	6.4		4.6	6.4	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

TL052C and TL052AC operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TL052C, TL052AC $V_{CC\pm} = \pm5$ V MIN	TYP	MAX	TL052C, TL052AC $V_{CC\pm} = \pm15$ V MIN	TYP	MAX	UNIT
SR +	Slew rate at unity gain	$R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1	25°C		17.8		9	20.7		V/μs
			Full range				8			
SR –	Negative slew rate at unity gain‡		25°C		15.4		9	17.8		
			Full range				8			
t_r	Rise time	$V_{I(PP)} = \pm10$ mV, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2	25°C		55			56		ns
			0°C		54			55		
			70°C		63			63		
t_f	Fall time		25°C		55			57		
			0°C		54			56		
			70°C		62			64		
	Overshoot factor		25°C		24%			19%		
			0°C		24%			19%		
			70°C		24%			19%		
V_n	Equivalent input noise voltage§	$R_S = 20\ \Omega$, See Figure 3; f = 10 Hz	25°C		71			71		nV/√Hz
		f = 1 kHz	25°C		19			19	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise current	f = 10 Hz t 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion¶	$R_S = 1\ k\Omega$, $R_L = 2\ k\Omega$, f = 1 kHz	25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $R_L = 2\ k\Omega$, $C_L = 25$ pF, See Figure 4	25°C		3			3		MHz
			0°C		3.2			3.2		
			70°C		2.6			2.7		
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 2\ k\Omega$, $C_L = 25$ pF, See Figure 4	25°C		60°			63°		
			0°C		59°			63°		
			70°C		60°			63°		

† Full range is 0°C to 70°C.

‡ For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

§ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For $V_{CC\pm} = \pm5$ V, $V_{O(RMS)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{O(RMS)} = 6$ V.

TEXAS INSTRUMENTS

TL052I and TL052AI electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL052I, TL052AI						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052I	25°C		0.73	3.5		0.65	1.5	mV
				Full range			5.3			3.3	
			TL052AI	25°C		0.51	2.8		0.4	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient‡		TL052I	25°C to 85°C		7			6		μV/°C
			TL052AI	25°C to 85°C		6			6	25	
	Input offset voltage long-term drift§	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$		25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification¶	$R_L = 2\ k\Omega$		25°C	25	59		50	105		V/mV
				−40°C	30	74		60	145		
				85°C	20	43		30	76		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−40°C	65	83		75	90		
				85°C	65	84		75	93		

† Full range is −40°C to 85°C.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters

§ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

¶ At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TL052I and TL052AI electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS		T_A	TL052I, TL052AI						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$,	$R_S = 50\ \Omega$	25°C	75	99		75	99		dB
				–40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current (two amplifiers)	$V_O = 0$,	No load	25°C		4.6	5.6		4.8	5.6	mA
				–40°C		4.5	6.4		4.7	6.4	
				85°C		4.4	6.4		4.6	6.4	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

TL052I and TL052AI operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A[†]	TL052I, TL052AI						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Slew rate at unity gain[‡]	$R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		25°C		17.8		9	20.7		V/μs
				Full range				8			
SR –	Negative slew rate at unity gain[‡]			25°C		15.4		9	17.8		
				Full range				8			
t_r	Rise time	$V_{I(PP)} = \pm10$ mV, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figures 1 and 2		25°C		55			56		ns
				–40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				–40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				–40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage[§]	$R_S = 20\ \Omega$, See Figure 3	f = 10 Hz	25°C		71			71		
			f = 1 kHz	25°C		19			19	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise current		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion[¶]	$R_S = 1\ k\Omega$, $R_L = 2\ k\Omega$, f = 1 kHz		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $R_L = 2\ k\Omega$, $C_L = 25$ pF, See Figure 4		25°C		3			3		MHz
				–40°C		3.5			3.6		
				85°C		2.5			2.6		
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 2\ k\Omega$, $C_L = 25$ pF, See Figure 4		25°C		60°			63°		
				–40°C		58°			61°		
				85°C		60°			63°		

[†] Full range is –40°C to 85°C.
[‡] For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.
[§] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.
[¶] For $V_{CC\pm} = \pm5$ V, $V_{O(RMS)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{O(RMS)} = 6$ V.

TL052M and TL052AM electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL052M, TL052AM						UNIT
					$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052M	25°C		0.73	3.5		0.65	1.5	mV
				Full range			6.5			4.5	
			TL052AM	25°C		0.51	2.8		0.4	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL052M	25°C to 125°C		10			9		μV/°C
			TL052AM	25°C to 125°C		9			8		
	Input offset voltage long-term drift‡	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$		25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification§	$R_L = 2\ k\Omega$		25°C	25	59		50	105		V/mV
				−55°C	30	76		60	149		
				125°C	10	32		15	49		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (two amplifiers)	$V_O = 0$, No load		25°C		4.6	5.6		4.8	5.6	mA
				−55°C		4.4	6.4		4.5	6.4	
				125°C		4.2	6.4		4.4	6.4	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is – 55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

TL052M and TL052AM operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL052M, TL052AM						UNIT
					$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain‡	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		25°C		17.8		9	20.7		V/μs
				Full range				8			
SR –	Negative slew rate at unity gain‡			25°C		15.4		9	17.8		
				Full range				8			
t_r	Rise time	$V_{I(PP)} = \pm 10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		55			56		ns
				–55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				–55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				–55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage§	$R_S = 20$ Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise current		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion¶	$R_S = 1$ kΩ, $R_L = 2$ kΩ, f = 1 kHz		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		3			3		MHz
				–55°C		3.6			3.7		
				125°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		60°			63°		
				–55°C		57°			61°		
				125°C		60°			63°		

† Full range is – 55°C to 125°C.
‡ For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.
§ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.
¶ For $V_{CC\pm} = \pm5$ V, $V_{O(RMS)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{O(RMS)} = 6$ V.

TL052Y electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL052Y						UNIT
			$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$		0.73			0.65		mV
	Input offset voltage long-term drift			0.04			0.04		μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		4			5		pA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		20			30		pA
V_{ICR}	Common-mode input voltage range			−2.3 to 5.6			−12.3 to 15.6		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ		4.2			13.9		V
		$R_L = 2$ kΩ		3.8			12.7		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ		−3.5			−13.2		
		$R_L = 2$ kΩ		−3.2			−12		
A_{VD}	Large-signal differential voltage amplification†	$R_L = 2$ kΩ		59			105		V/mV
r_i	Input resistance			10^{12}			10^{12}		Ω
c_i	Input capacitance			10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $R_S = 50\ \Omega$, $V_O = 0$,		85			93		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_O = 0$, $R_S = 50\ \Omega$		99			99		dB
I_{CC}	Supply current (two amplifiers)	$V_O = 0$, No load		4.6			4.8		mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		120			120		dB

† For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

TL052Y operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL052Y						UNIT
				$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain[†]	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1			17.8			20.7		V/µs
SR –	Negative slew rate at unity gain[†]				15.4			17.8		
t_r	Rise time	$V_{I(PP)} = \pm10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2			55			56		ns
t_f	Fall time				55			57		
	Overshoot factor				24%			19%		
V_n	Equivalent input noise voltage[‡]	$R_S = 20$ Ω, See Figure 3	f = 10 Hz		71			71		nV/√Hz
			f = 1 kHz		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise current		f = 10 Hz to 10 kHz		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz			0.01			0.01		pA/√Hz
THD	Total harmonic distortion[§]	$R_S = 1$ kΩ, $R_L = 2$ kΩ, f = 1 kHz			0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4			3			3		MHz
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4			60°			63°		

[†] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[‡] For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

[§] For $V_{CC\pm} = \pm5$ V, $V_{O(RMS)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{O(RMS)} = 6$ V.

TL054C and TL054AC electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL054C, TL054AC						UNIT
					$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054C	25°C		0.64	5.5		0.56	4	mV
				Full range			7.7			6.2	
			TL054AC	25°C		0.57	3.5		0.5	1.5	
				Full range			5.7			3.7	
α_{VIO}	Temperature coefficient of input offset voltage		TL054C	25°C to 70°C		25			23		µV/°C
			TL054AC	25°C to 70°C		24			23		
	Input offset voltage long-term drift‡			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification§	$R_L = 2\ k\Omega$		25°C	25	72		50	133		V/mV
				0°C	30	88		60	173		
				70°C	20	57		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				0°C	65	84		75	92		
				70°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	99		75	99		
				70°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	$V_O = 0$, No load		25°C		8.1	11.2		8.4	11.2	mA
				0°C		8.2	12.8		8.5	12.8	
				70°C		7.9	11.2		8.2	11.2	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

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† Full range is 0°C to 70°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V, at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.B

TL054C and TL054AC operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL054C, TL054C						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		15.4		10	17.8		V/μs
				0°C		15.7		8	17.9		
SR–	Negative slew rate at unity gain‡			70°C		14.4		8	17.5		
				25°C		13.9		10	15.9		
				0°C		14.3		8	16.1		
				70°C		13.3		8	15.5		
t_r	Rise time	$V_{I(PP)}$ = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage§	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21	45	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion¶	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				0°C		3			3		
				70°C		2.4			2.4		
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				0°C		60°			64°		
				70°C		61°			63°		

† Full range is 0°C to 70°C.

‡ For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

§ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For $V_{CC\pm} = \pm5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{O(rms)} = 6$ V.

TL054I and TL054AI electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL054I, TL054AI						UNIT
					$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL054I	25°C		0.64	5.5		0.56	4	mV
				Full range			8.8			7.3	
			TL054AI	25°C		0.57	3.5		0.5	1.5	
				Full range			6.8			4.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL054I	25°C to 85°C		25			24		µV/°C
			TL054AI	25°C to 85°C		25			23		
	Input offset voltage long-term drift‡			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification§	R_L = 2 kΩ		25°C	25	72		50	133		V/mV
				−40°C	30	101		60	212		
				85°C	20	50		30	70		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω		25°C	65	84		75	92		dB
				−40°C	65	83		75	92		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				−40°C	75	98		75	99		
				85°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	V_O = 0, No load		25°C		8.1	11.2		8.4	11.2	mA
				−40°C		7.9	12.8		8.2	12.8	
				85°C		7.6	11.2		7.9	11.2	
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is −40°C to 85°C.
‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
§ For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V, at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

TL054I and TL054AI operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	TL054I, TL054AI						UNIT
					$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1		25°C		15.4		10	17.8		V/μs
				–40°C		16.4		8	18		
				85°C		14		8	17.3		
SR–	Negative slew rate at unity gain‡			25°C		13.9		10	15.9		
				–40°C		14.7		8	16.1		
				85°C		13		8	15.3		
t_r	Rise time	$V_{I(PP)}$ = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				–40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				–40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				–40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage§	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21	45	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion¶	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				–40°C		3.3			3.3		
				85°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				–40°C		59°			62°		
				85°C		61°			64°		

† Full range is –40°C to 85°C.

‡ For $V_{CC\pm}$ = ±5 V, $V_{I(PP)}$ = ±1 V; for $V_{CC\pm}$ = ±15 V, $V_{I(PP)}$ = ±5 V.

§ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For $V_{CC\pm}$ = ±5 V, $V_{O(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{O(rms)}$ = 6 V.

TL054M and TL054AM electrical characteristics at specified free-air temperature

	PARAMETER	TEST CONDITIONS		T_A†	TL054M, TL054AM						UNIT
					$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054M	25°C		0.64	5.5		0.56	4	mV
				Full range			10.5			9	
			TL054AM	25°C		0.57	3.5		0.5	1.5	
				Full range			8.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage		TL054M	25°C to 85°C		21			20		µV/°C
			TL054AM	25°C to 85°C		21			20		
	Input offset voltage long-term drift‡			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification§	$R_L = 2\ k\Omega$		25°C	25	72		50	133		V/mV
				−55°C	30	99		60	209		
				125°C	10	35		15	35		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		
				85°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	$V_O = 0$,	No load	25°C		8.1	11.2		8.4	11.2	mA
				−55°C		7.8	12.8		8.1	12.8	
				125°C		7.1	11.2		7.5	11.2	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is −55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ For $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V, at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

TL054M and TL054AM operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A[†]	TL054M, TL054AM						UNIT
				$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1	25°C		15.4		10	17.8		V/µs
			–55°C		16.7			18.3		
			125°C		12.9			16.7		
SR–	Negative slew rate at unity gain[‡]		25°C		13.9		10	15.9		
			–55°C		14.7			16.3		
			125°C		12.2			14.5		
t_r	Rise time	$V_{I(PP)} = \pm10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2	25°C		55			56		ns
			–55°C		51			52		
			125°C		68			68		
t_f	Fall time		25°C		55			57		
			–55°C		51			52		
			125°C		68			69		
	Overshoot factor		25°C		24%			19%		
			–55°C		25%			19%		
			125°C		25%			19%		
V_n	Equivalent input noise voltage[§]	$R_S = 20$ Ω, See Figure 3; f = 10 Hz	25°C		75			75		nV/√Hz
		f = 1 kHz	25°C		21			21	45	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion[¶]	$R_S = 1$ kΩ, $R_L = 2$ kΩ, f = 1 kHz	25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4	25°C		2.7			2.7		MHz
			–55°C		3.4			3.4		
			125°C		2.1			2.1		
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4	25°C		61°			64°		
			–55°C		58°			62°		
			125°C		60°			64°		

[†] Full range is –55°C to 125°C.

[‡] For $V_{CC\pm} = \pm5$ V, $V_{I(PP)} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{I(PP)} = \pm5$ V.

[§] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[¶] For $V_{CC\pm} = \pm5$ V, $V_{Orms} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{Orms} = 6$ V.

TL054Y electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL054Y						UNIT
			$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$		0.64			0.56		mV
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		4			5		pA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		20			30		pA
V_{ICR}	Common-mode input voltage range			−2.3 to 5.6			−12.3 to 15.6		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		4.2			13.9		V
		$R_L = 2\ k\Omega$		3.8			12.7		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		−3.5			−13.2		V
		$R_L = 2\ k\Omega$		−3.2			−12		
A_{VD}	Large-signal differential voltage amplification†	$R_L = 2\ k\Omega$,		72			133		V/mV
r_i	Input resistance			10^{12}			10^{12}		Ω
c_i	Input capacitance			10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\min$, $V_O = 0$, $R_S = 50\ \Omega$		84			92		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		99			99		dB
I_{CC}	Supply current (four amplifiers)	$V_O = 0$, No load		8.1			8.4		mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		120			120		dB

† For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V, at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

TL054Y operating characteristics, T_A = 25°C

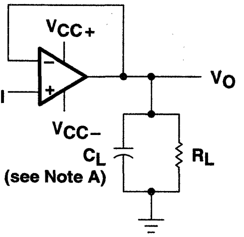
PARAMETER		TEST CONDITIONS		TL054Y						UNIT
				$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain[†]	R_L = 2 kΩ, C_L = 100 pF, See Figure 1			15.4			17.8		V/µs
SR–	Negative slew rate at unity gain				13.9			15.9		
t_r	Rise time	$V_{I(PP)}$ = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2			55			56		ns
t_f	Fall time				55			57		
	Overshoot factor				24%			19%		
V_n	Equivalent input noise voltage[‡]	R_S = 20 Ω, See Figure 3	f = 10 Hz		75			75		nV/√Hz
			f = 1 kHz		21			21		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz			0.01			0.01		pA/√Hz
THD	Total harmonic distortion[§]	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz			0.003%			0.003%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4			2.7			2.7		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4			61°			64°		

[†] For $V_{CC\pm}$ = ±5 V, $V_{I(PP)}$ = ±1 V; for $V_{CC\pm}$ = ±15 V, $V_{I(PP)}$ = ±5 V.

[‡] This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

[§] For $V_{CC\pm}$ = ±5 V, $V_{O(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{O(rms)}$ = 6 V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1 . Slew Rate, Rise/Fall Time, and Overshoot Test Circuit

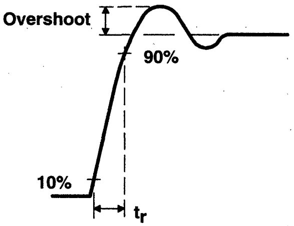


Figure 2 . Rise Time and Overshoot Waveform

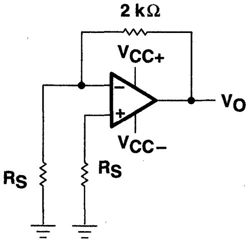
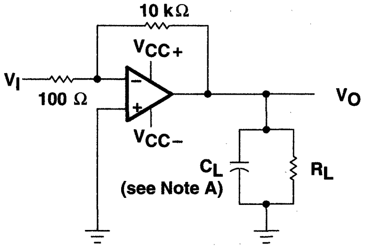


Figure 3 . Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4 . Unity-Gain Bandwidth and Phase-Margin Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

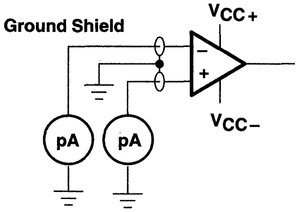


Figure 5. Input-Bias and Offset-Current Test Circuit

At the picoamp-bias-current level typical of the TL05x and TL05xA, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actualdevice bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket, and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6 – 11
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	12, 13, 14
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	15 16
I_{IO}	Input offset current	vs Free-air temperature	16
V_{IC}	Common-mode input voltage range limits	vs Supply voltage vs Free-air temperature	17 18
V_O	Output voltage	vs Differential input voltage	19, 20
V_{OM}	Maximum peak output voltage	vs Supply voltage vs Output current vs Free-air temperature	21 25, 26 27, 28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	22, 23, 24
A_{VD}	Large-signal differential voltage amplification	vs Load resistance vs Frequency vs Free-air temperature	29 30 31, 32, 33
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	34, 35 36
z_o	Output impedance	vs Frequency	37
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	38
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	39 40 41
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	42, 43, 44 45, 46, 47
SR	Slew rate	vs Load resistance vs Free-air temperature	48 – 53 54 –59
	Overshoot factor	vs Load capacitance	60
V_n	Equivalent input noise voltage	vs Frequency	61, 62
THD	Total harmonic distortion	vs Frequency	63
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	64, 65, 66 67, 68, 69
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	70, 71, 72 73, 74, 75 76, 77, 78
	Phase shift	vs Frequency	30
	Voltage-follower small-signal pulse response	vs Time	79
	Voltage-follower large-signal pulse response	vs Time	80

TYPICAL CHARACTERISTICS

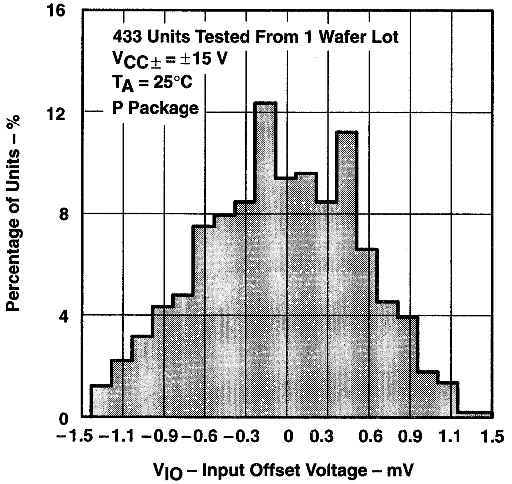

DISTRIBUTION OF TL051
INPUT OFFSET VOLTAGE

Figure 6

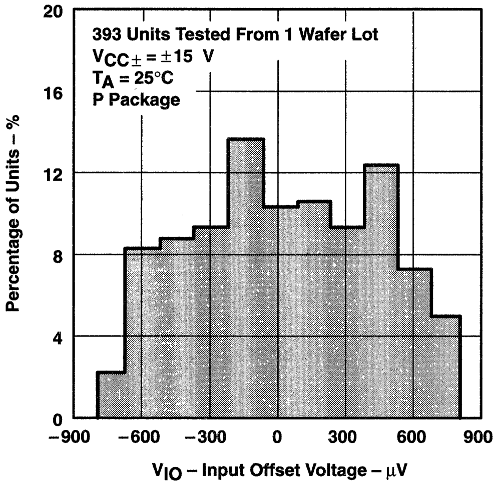

DISTRIBUTION OF TL051A
INPUT OFFSET VOLTAGE

Figure 7

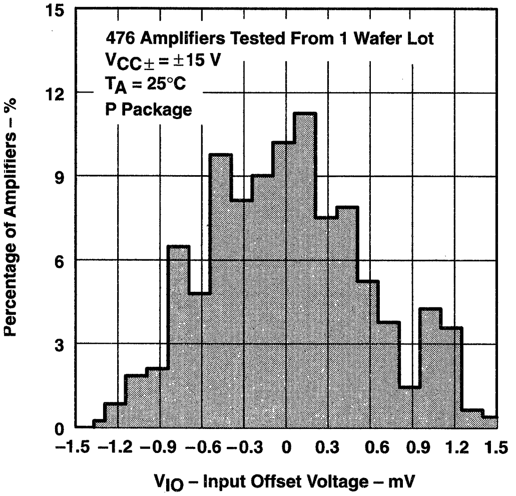

DISTRIBUTION OF TL052
INPUT OFFSET VOLTAGE

Figure 8

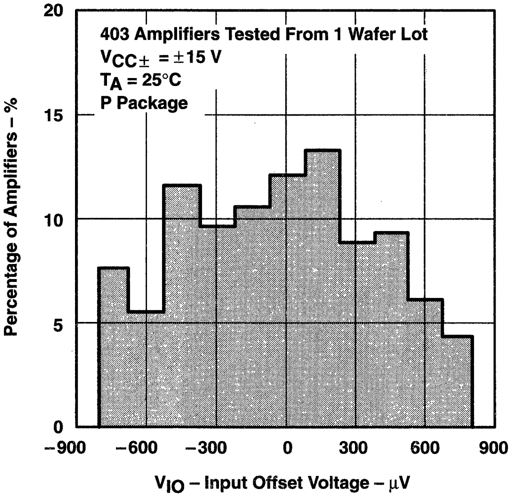

DISTRIBUTION OF TL052A
INPUT OFFSET VOLTAGE

Figure 9

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TL054
INPUT OFFSET VOLTAGE**

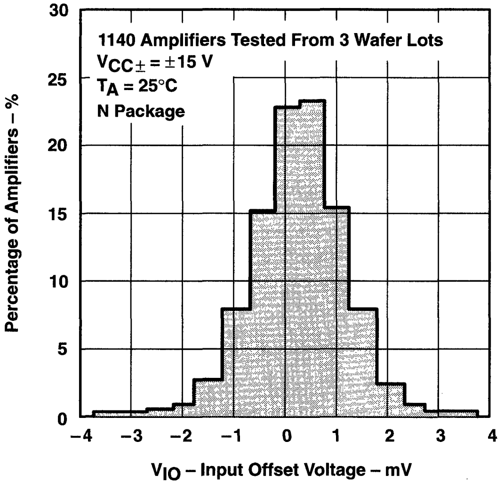


Figure 10

**DISTRIBUTION OF TL054A
INPUT OFFSET VOLTAGE**

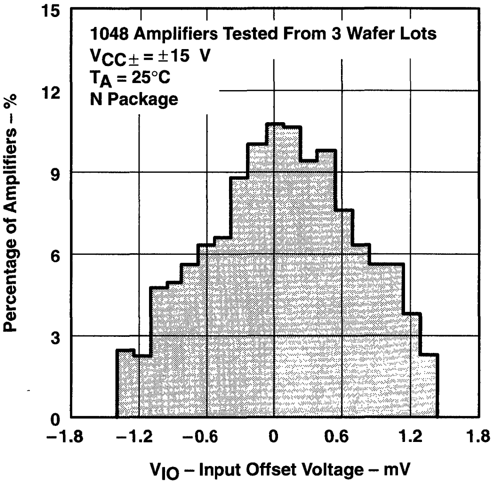


Figure 11

**DISTRIBUTION OF TL051
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

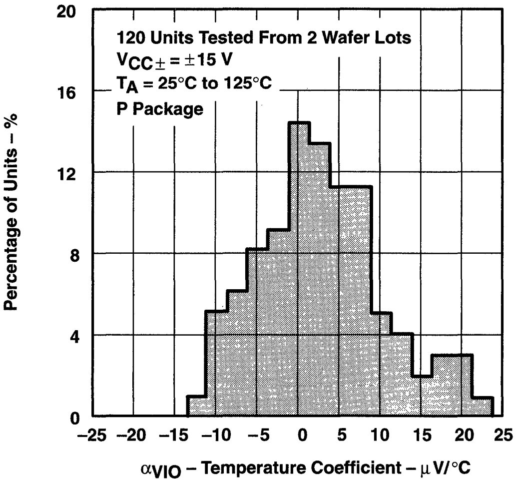


Figure 12

**DISTRIBUTION OF TL052
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

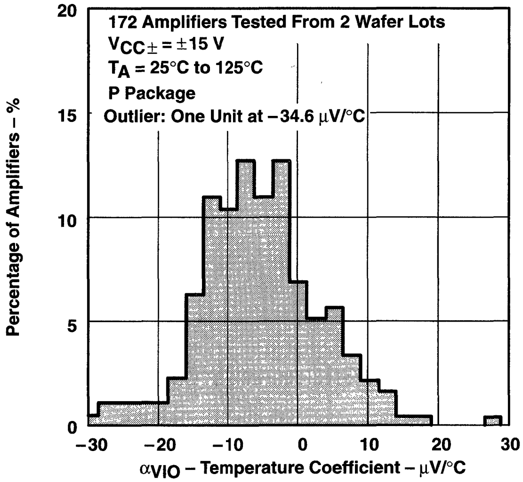


Figure 13

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL054 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

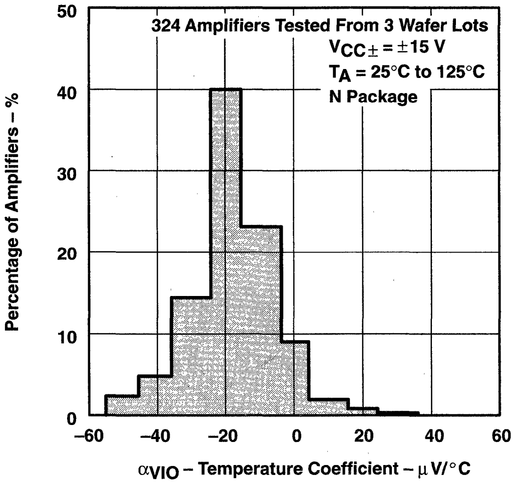


Figure 14

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

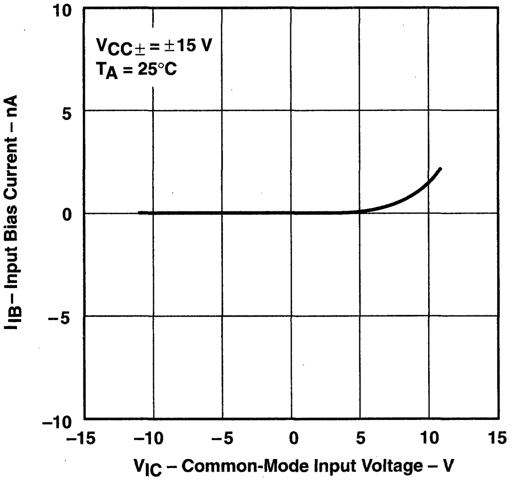


Figure 15

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT† vs FREE-AIR TEMPERATURE

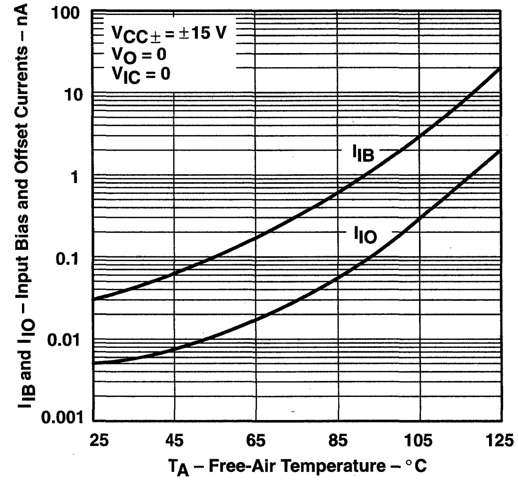


Figure 16

COMMON-MODE INPUT VOLTAGE RANGE LIMITS vs SUPPLY VOLTAGE

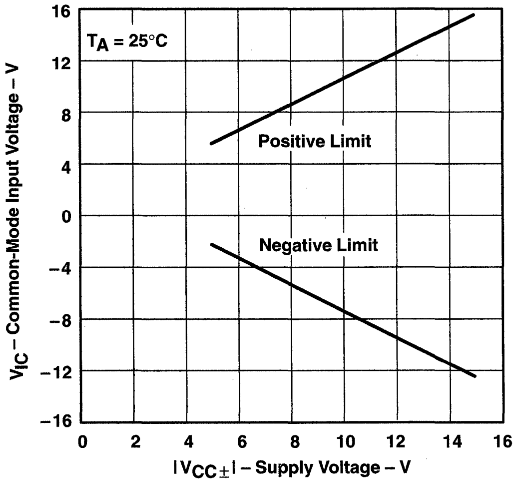


Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS†
vs
FREE-AIR TEMPERATURE

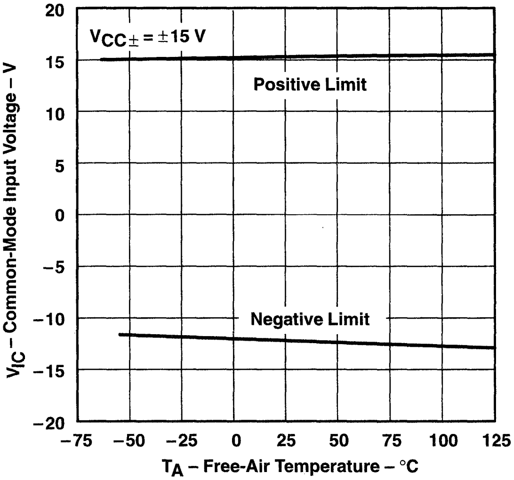

Figure 18

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

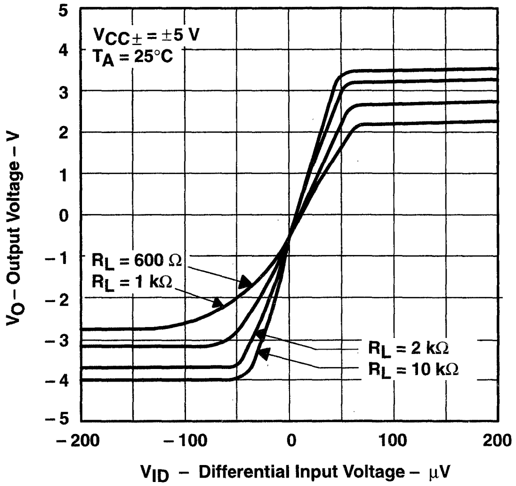

Figure 19

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

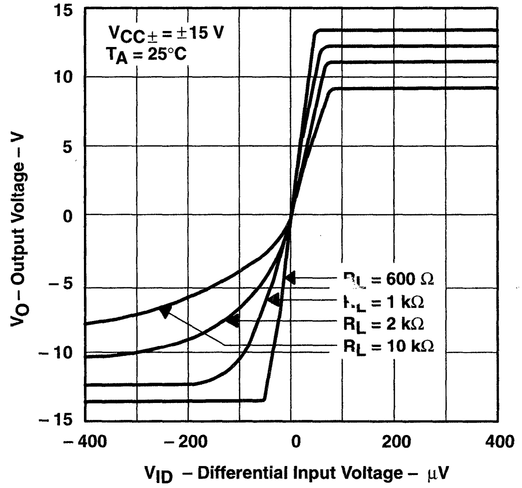

Figure 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

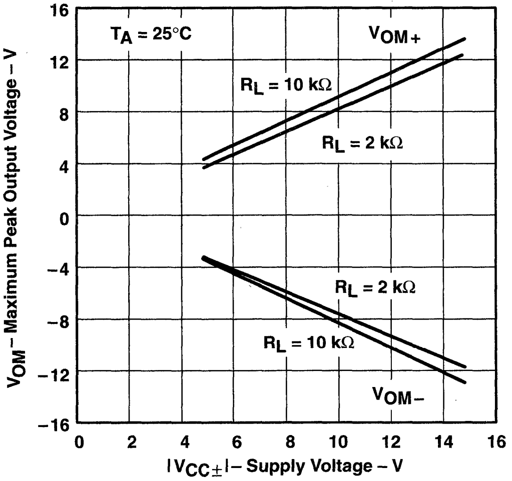

Figure 21

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE† vs FREQUENCY

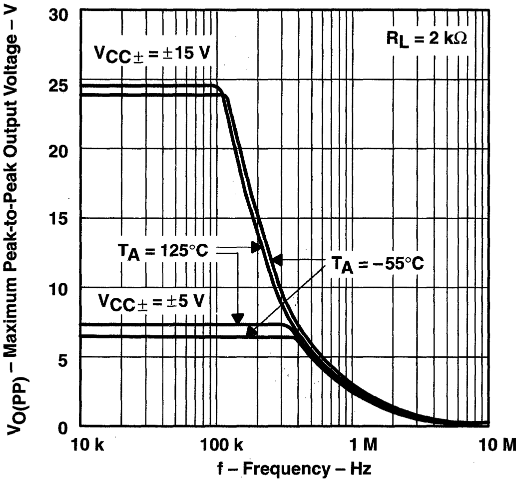

Figure 22

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

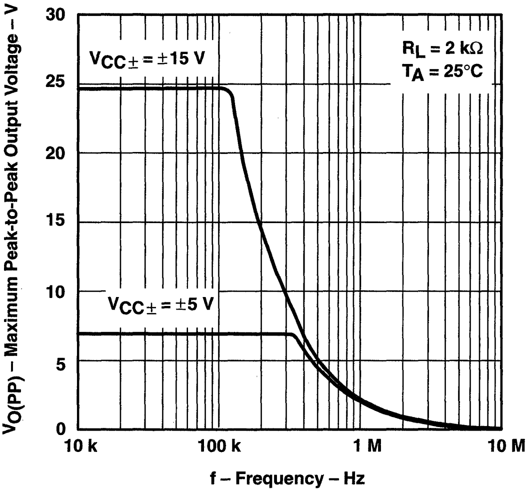

Figure 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

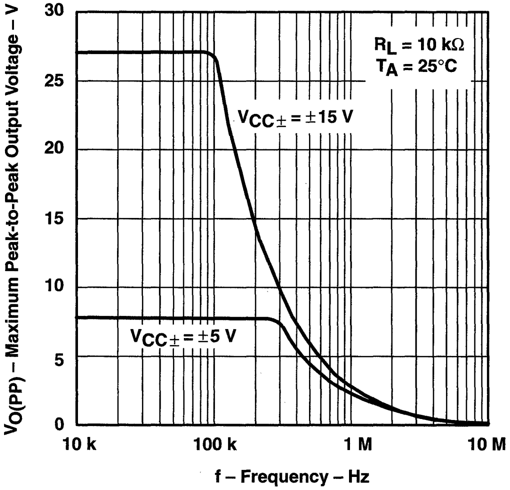

Figure 24

MAXIMUM PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

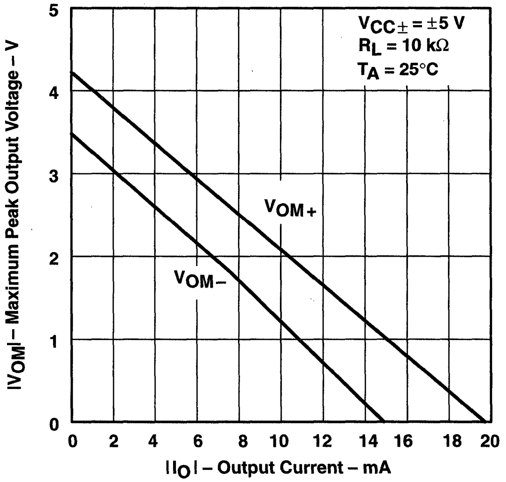

Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

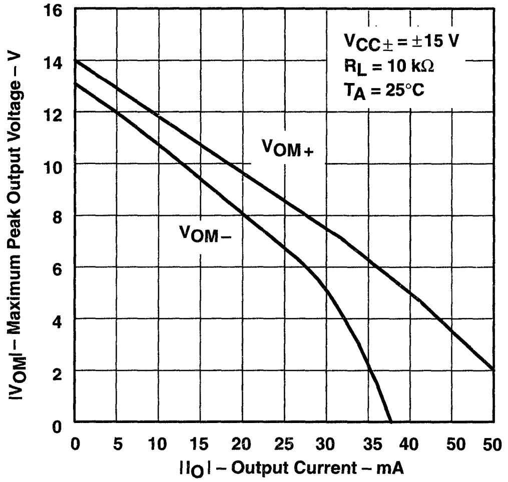

Figure 26

MAXIMUM PEAK OUTPUT VOLTAGE†
vs
FREE-AIR TEMPERATURE

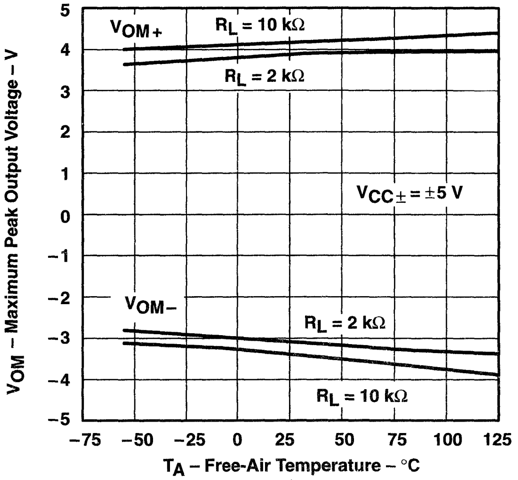

Figure 27

MAXIMUM PEAK OUTPUT VOLTAGE†
vs
FREE-AIR TEMPERATURE

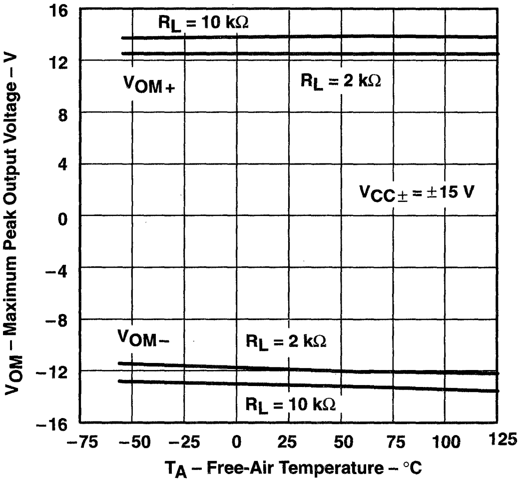

Figure 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

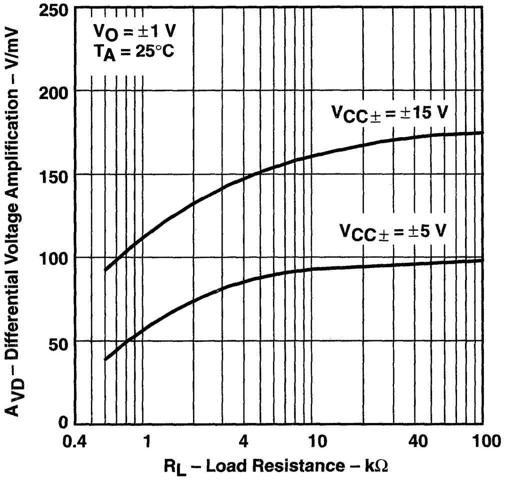

Figure 29

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

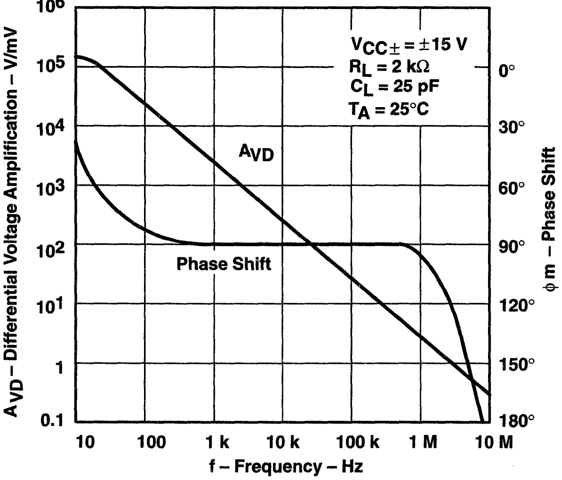

Figure 30

TL051 AND TL052
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†
vs
FREE-AIR TEMPERATURE

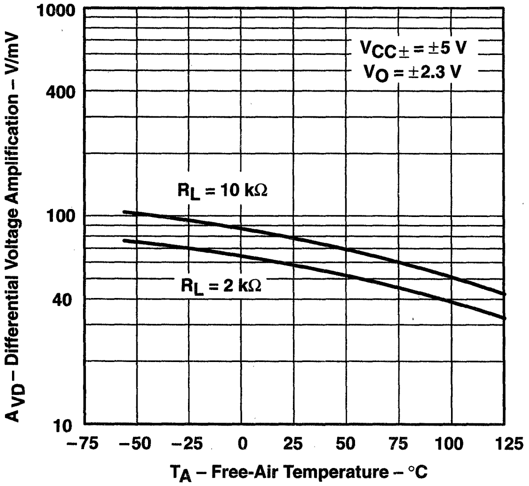

Figure 31

TL054
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†
vs
FREE-AIR TEMPERATURE

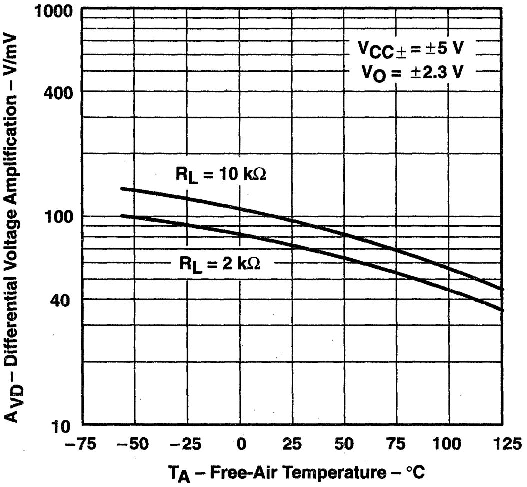

Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†
vs
FREE-AIR TEMPERATURE

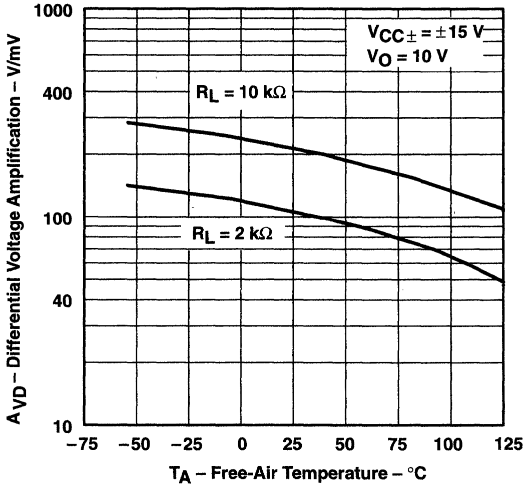

Figure 33

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

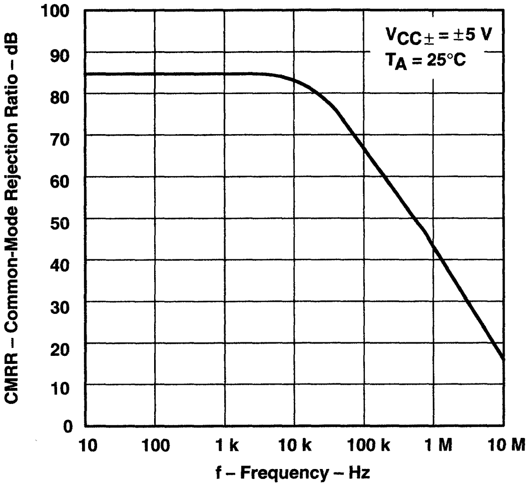

Figure 34

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

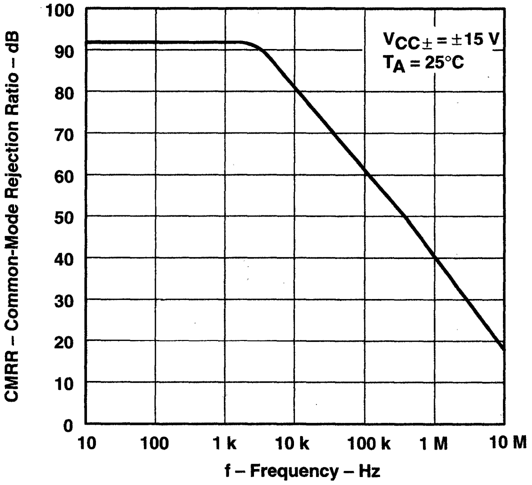

Figure 35

COMMON-MODE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

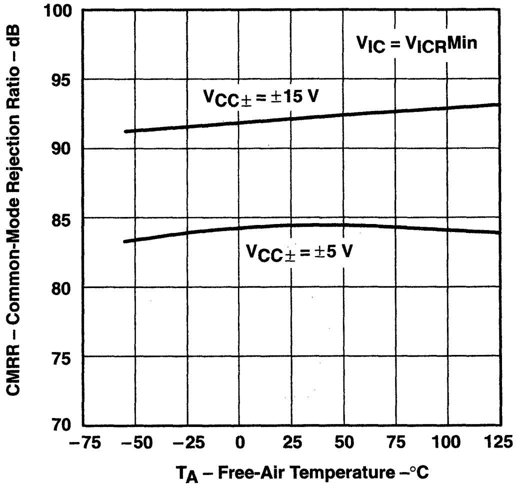

Figure 36

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

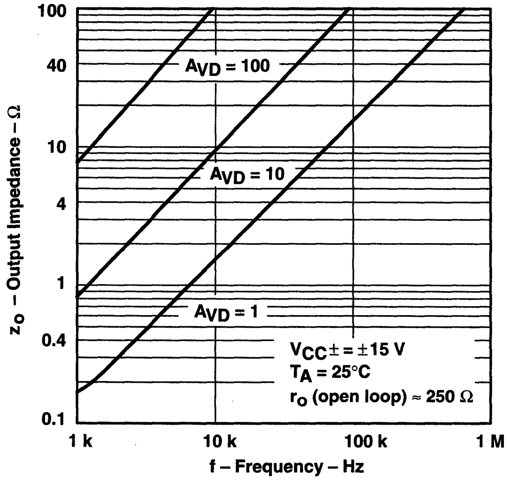

Figure 37

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

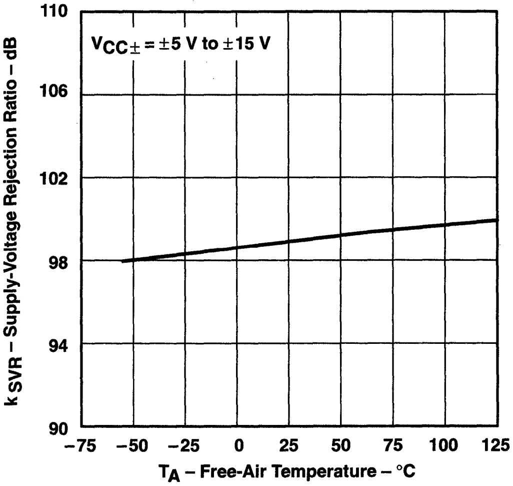

Figure 38

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

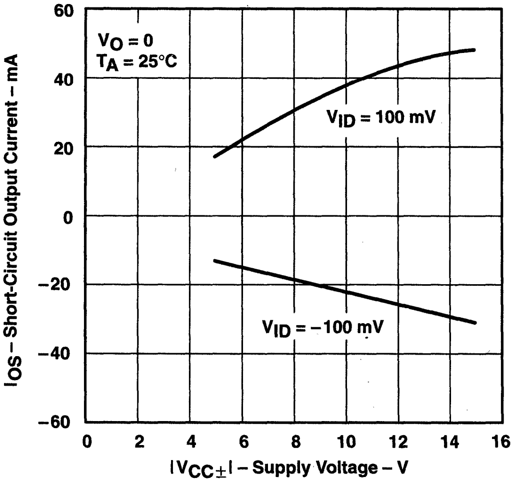

Figure 39

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

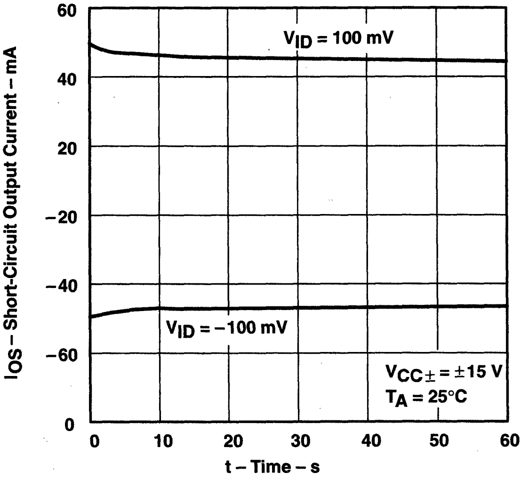

Figure 40

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

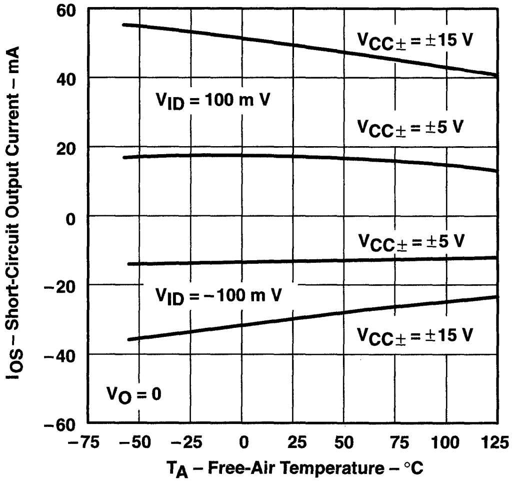

Figure 41

TL051
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

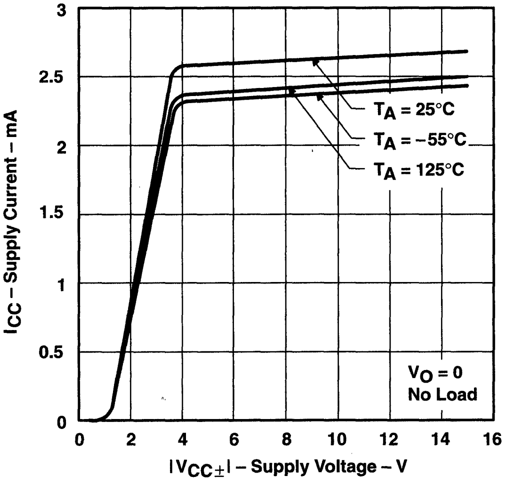

Figure 42

TL052
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

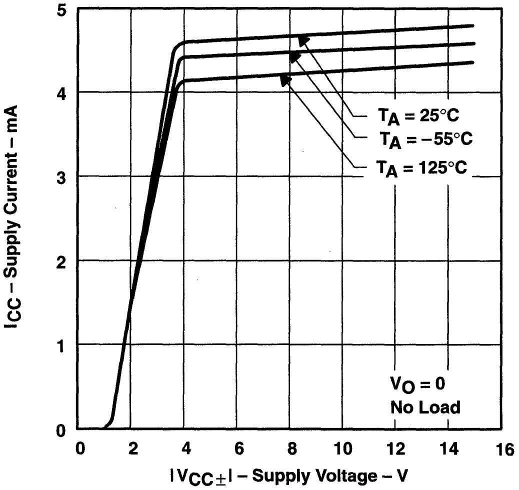

Figure 43

TL054
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

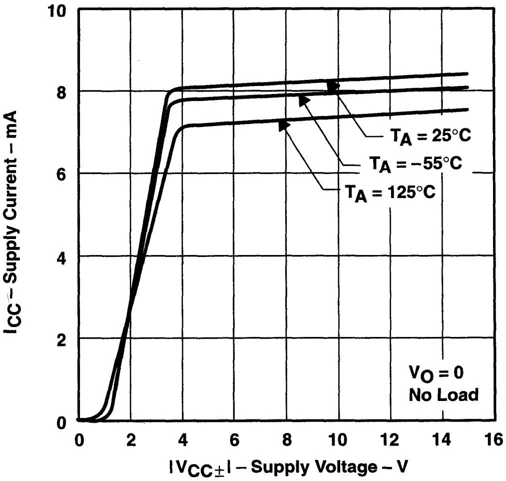

Figure 44

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TL051
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

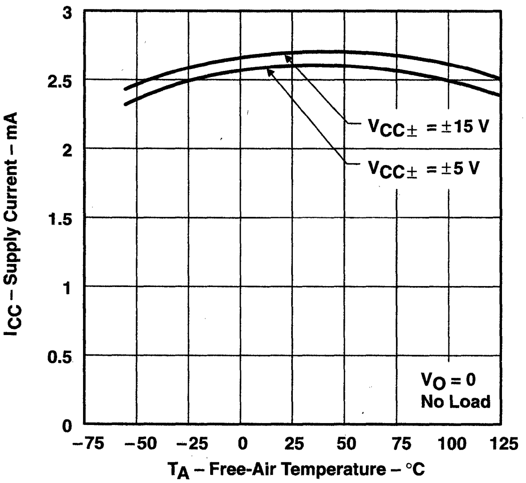

Figure 45

TL052
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

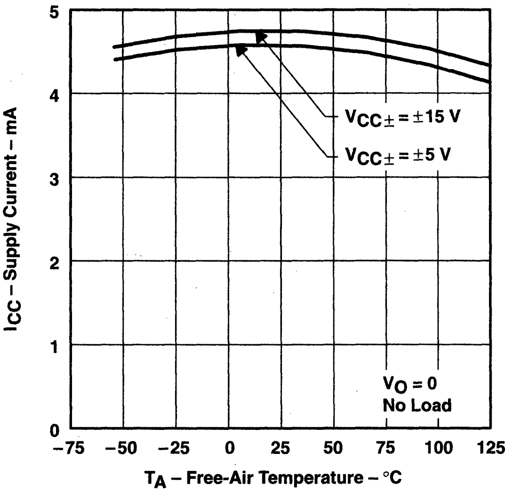

Figure 46

TL054
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

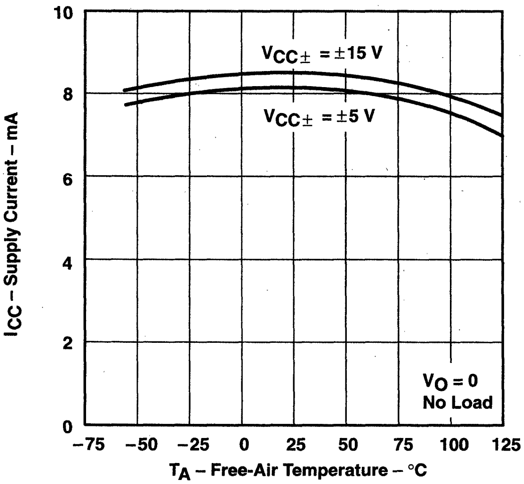

Figure 47

TL051
SLEW RATE
vs
LOAD RESISTANCE

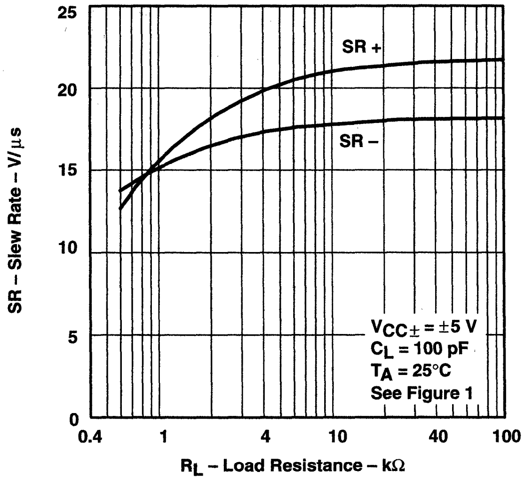

Figure 48

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

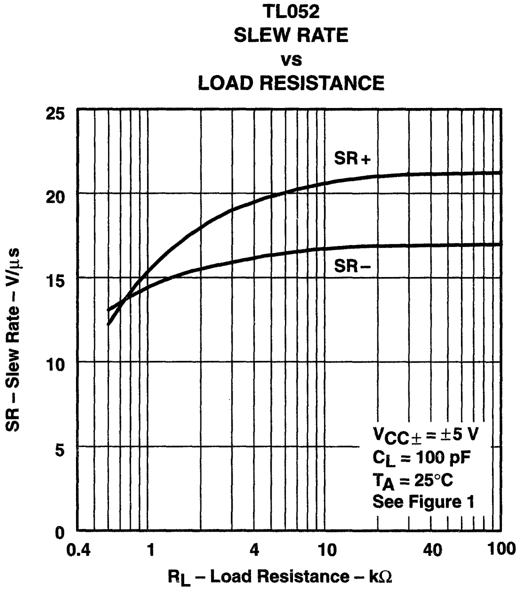

Figure 49

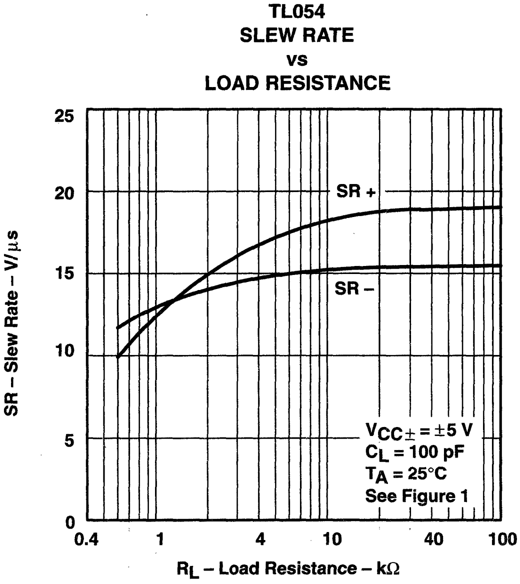

Figure 50

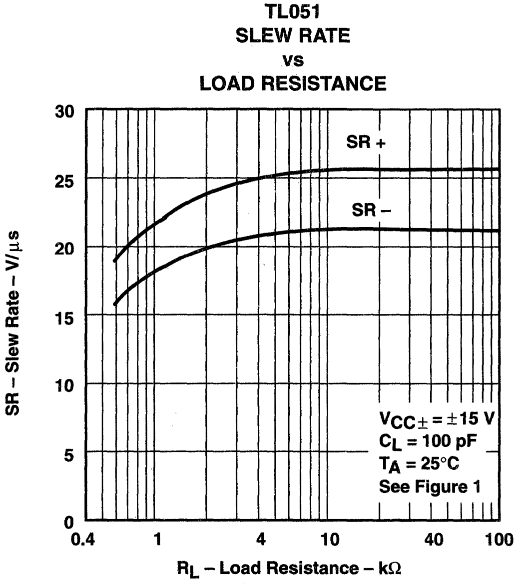

Figure 51

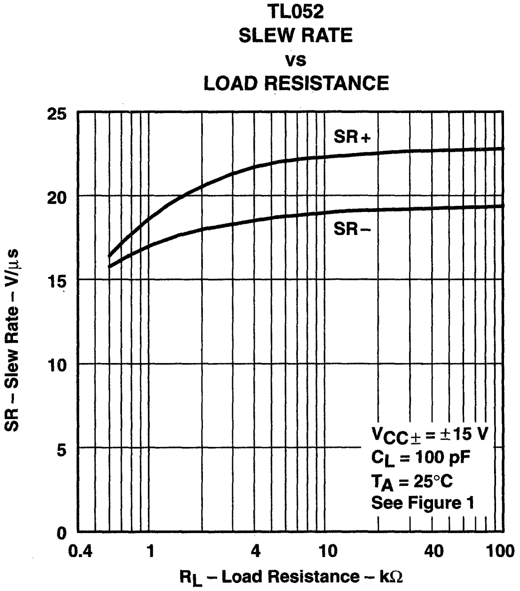

Figure 52

TYPICAL CHARACTERISTICS

TL054
SLEW RATE
vs
LOAD RESISTANCE

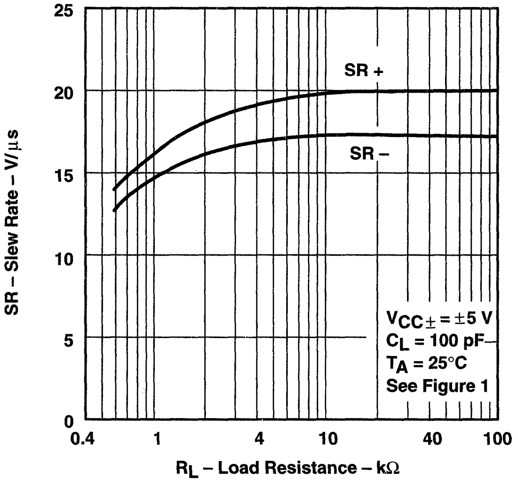

Figure 53

TL051
SLEW RATE†
vs
FREE-AIR TEMPERATURE

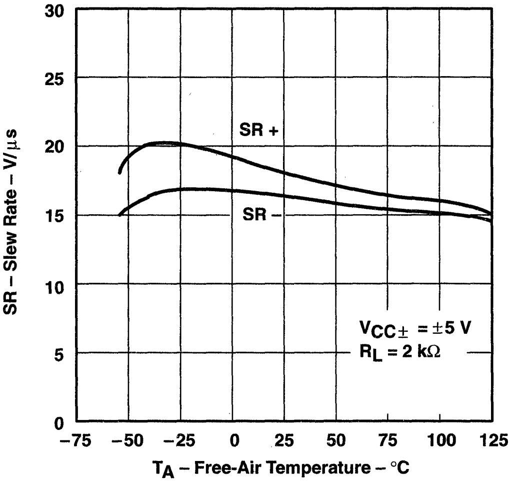

Figure 54

TL052
SLEW RATE†
vs
FREE-AIR TEMPERATURE

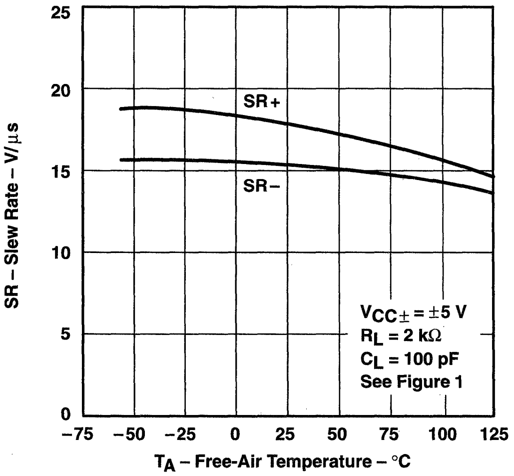

Figure 55

TL054
SLEW RATE†
vs
FREE-AIR TEMPERATURE

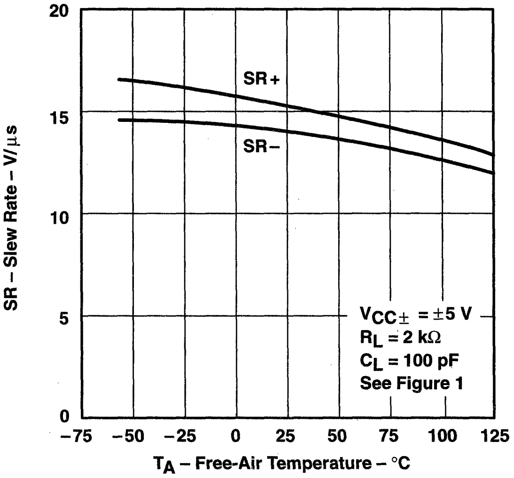

Figure 56

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

**TL051
SLEW RATE†
vs
FREE-AIR TEMPERATURE**

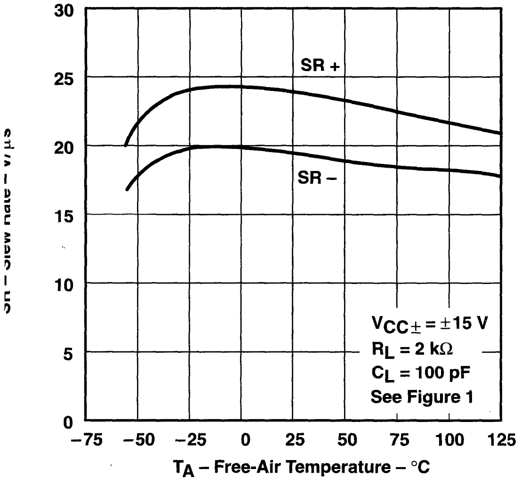

Figure 57

**TL052
SLEW RATE†
vs
FREE-AIR TEMPERATURE**

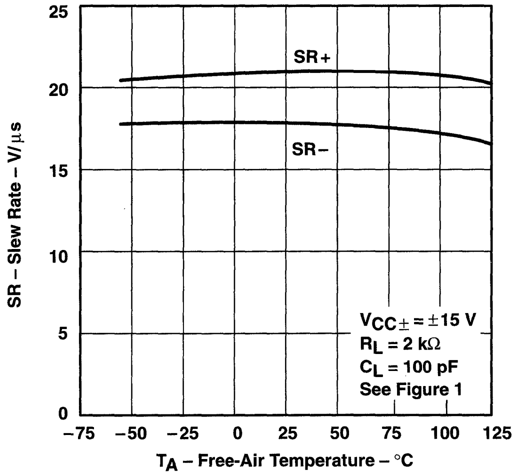

Figure 58

**TL054
SLEW RATE†
vs
FREE-AIR TEMPERATURE**

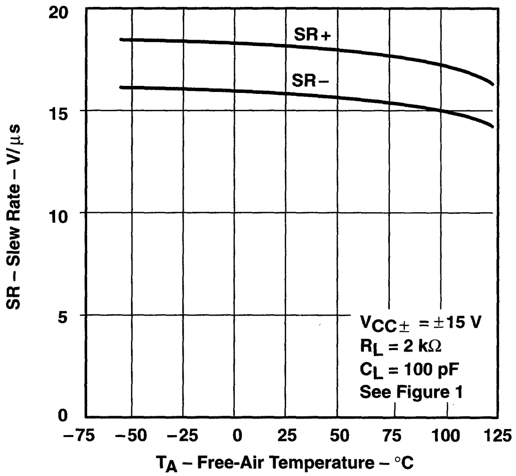

Figure 59

**OVERSHOOT FACTOR
vs
LOAD CAPACITANCE**

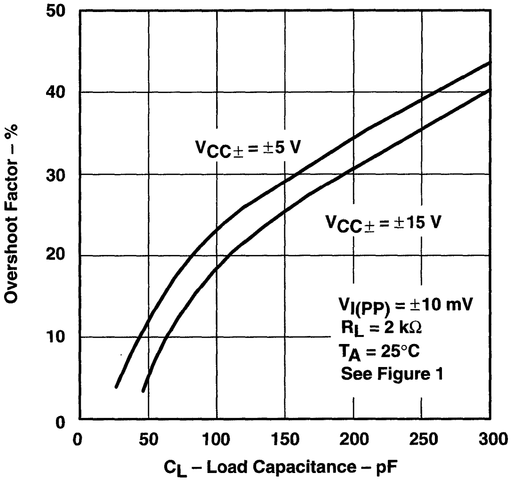

Figure 60

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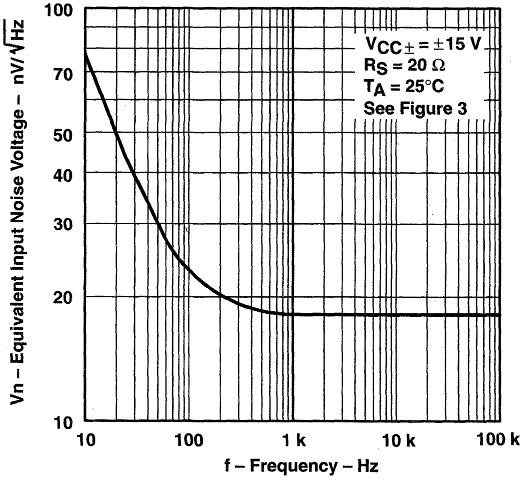
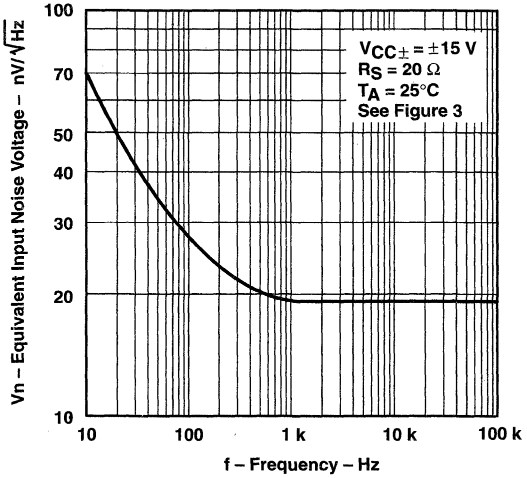
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



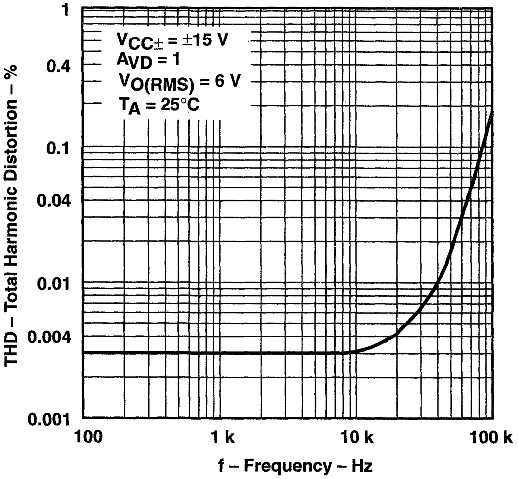
TL051
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 61



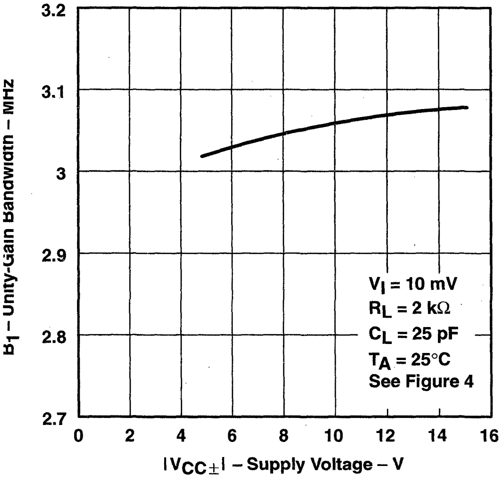
TL052 AND TL054
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 62



TOTAL HARMONIC DISTORTION
vs
FREQUENCY

Figure 63



TL051
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

Figure 64

TYPICAL CHARACTERISTICS

TL052
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

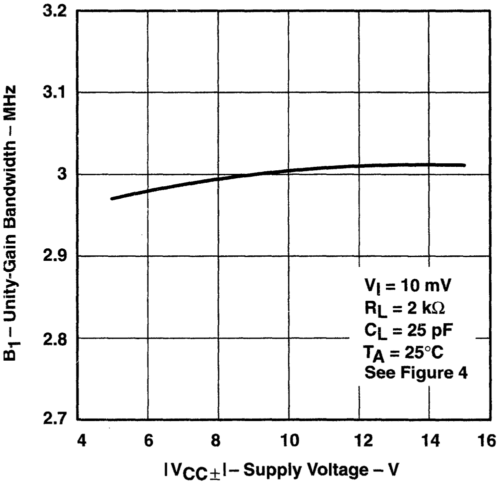


Figure 65

TL054
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

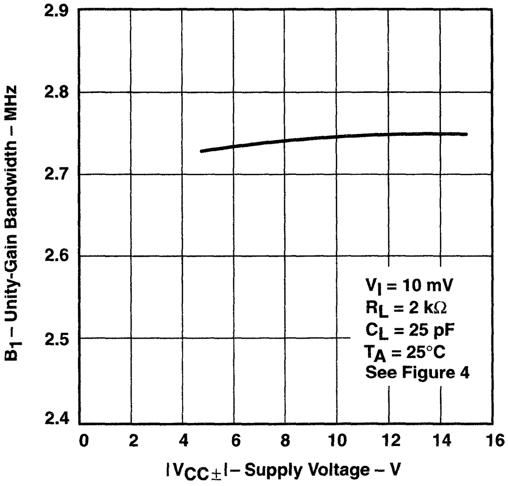


Figure 66

TL051
UNITY-GAIN BANDWIDTH†
vs
FREE-AIR TEMPERATURE

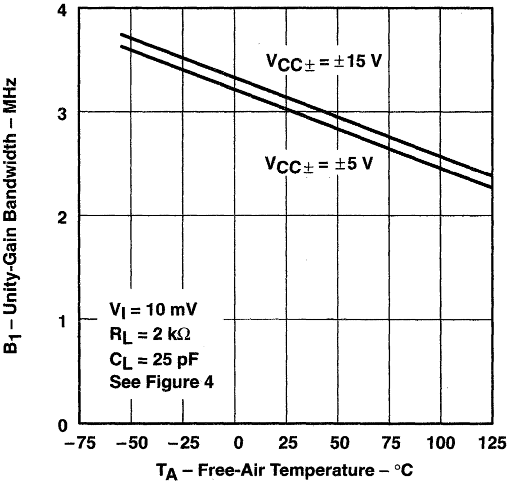


Figure 67

TL052
UNITY-GAIN BANDWIDTH†
vs
FREE-AIR TEMPERATURE

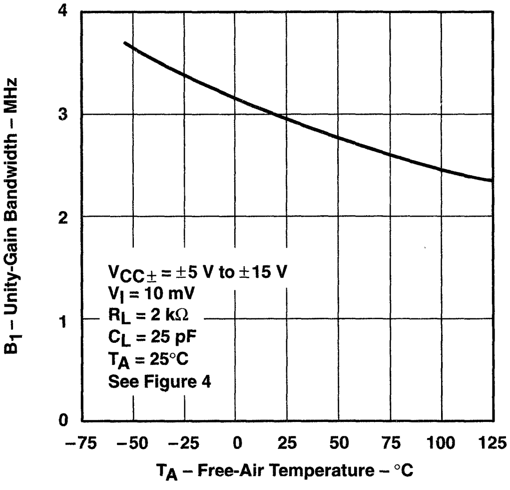


Figure 68

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

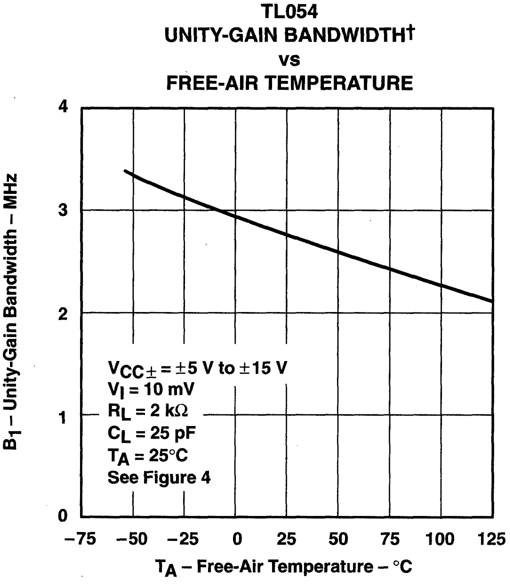

Figure 69

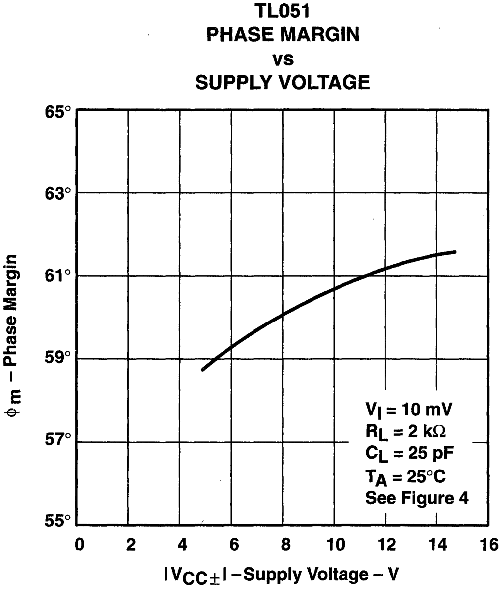

Figure 70

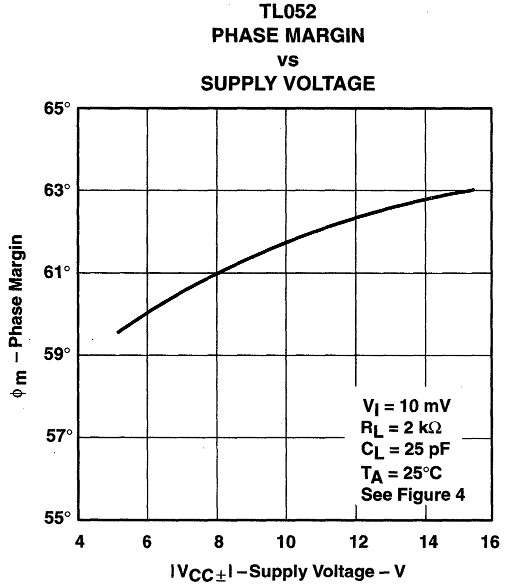

Figure 71

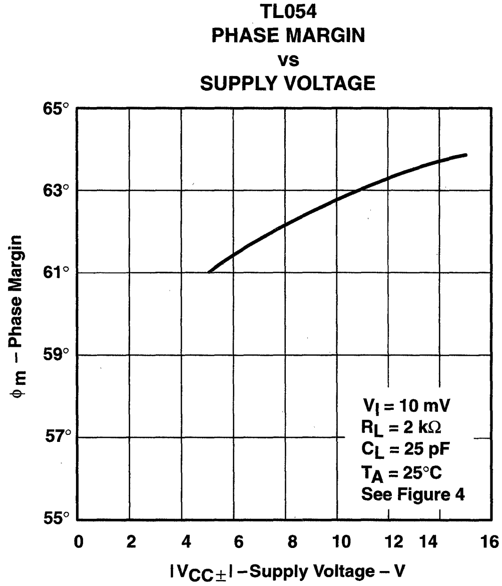

Figure 72

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TL051
PHASE MARGIN†
vs
LOAD CAPACITANCE

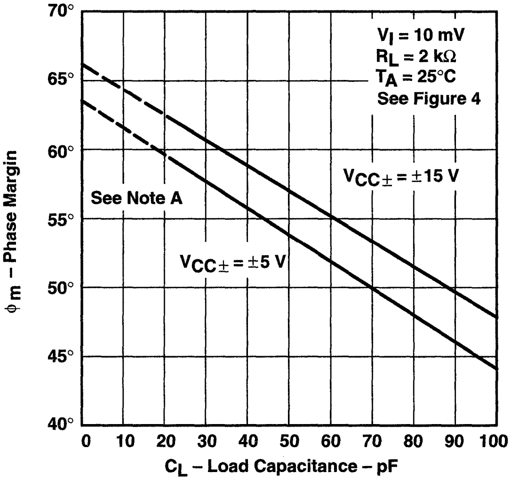

Figure 73

TL052
PHASE MARGIN†
vs
LOAD CAPACITANCE

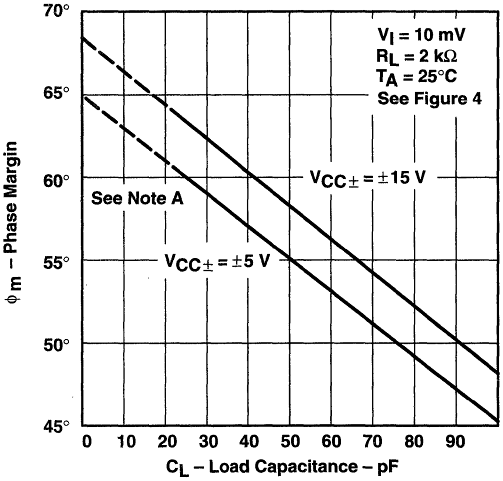

Figure 74

TL054
PHASE MARGIN†
vs
LOAD CAPACITANCE

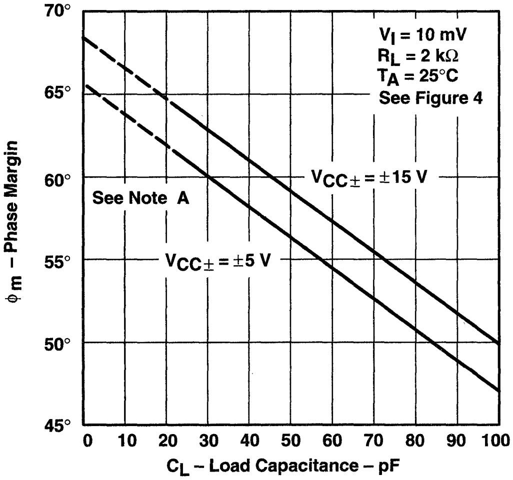

Figure 75

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† Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

TL051
PHASE MARGIN†
vs
FREE-AIR TEMPERATURE

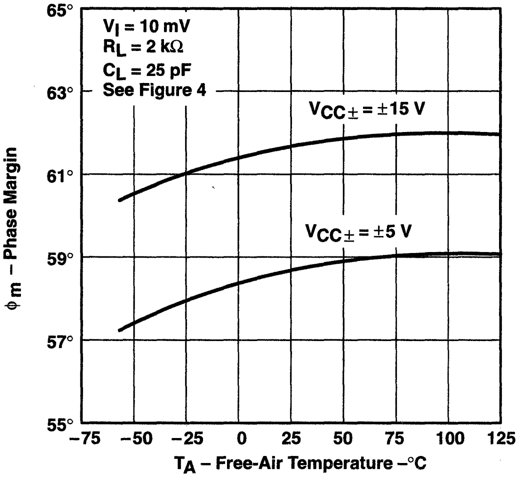

Figure 76

TL052
PHASE MARGIN†
vs
FREE-AIR TEMPERATURE

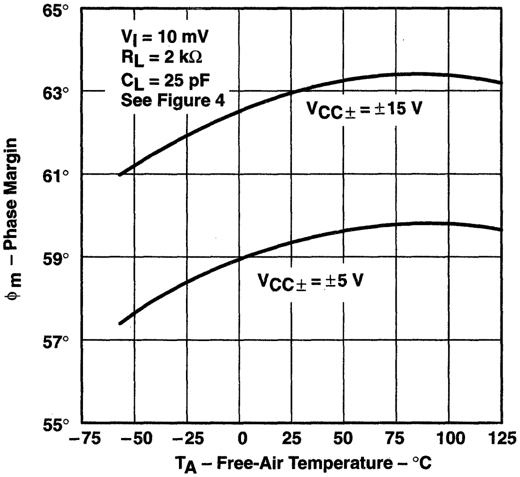

Figure 77

TL054
PHASE MARGIN†
vs
FREE-AIR TEMPERATURE

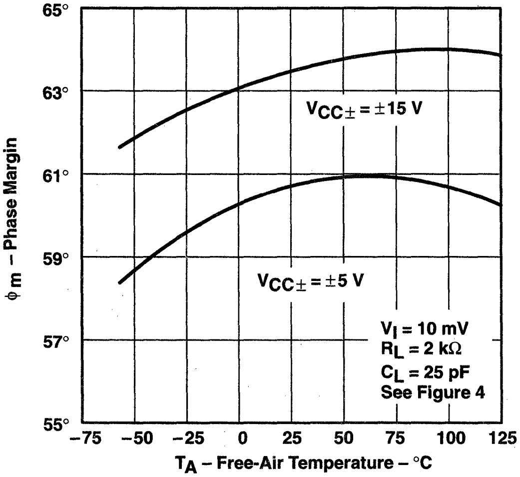

Figure 78

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

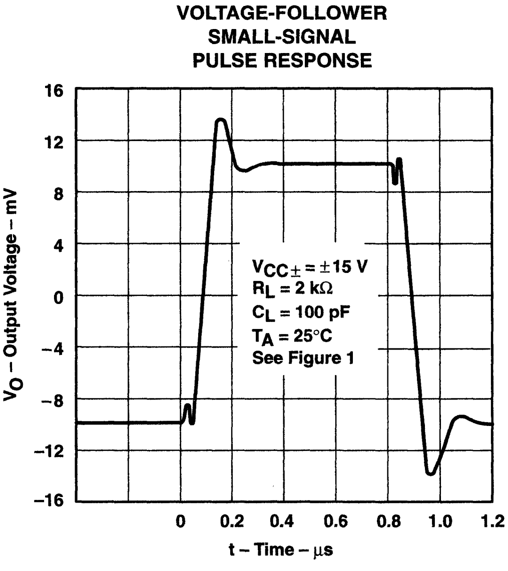


Figure 79

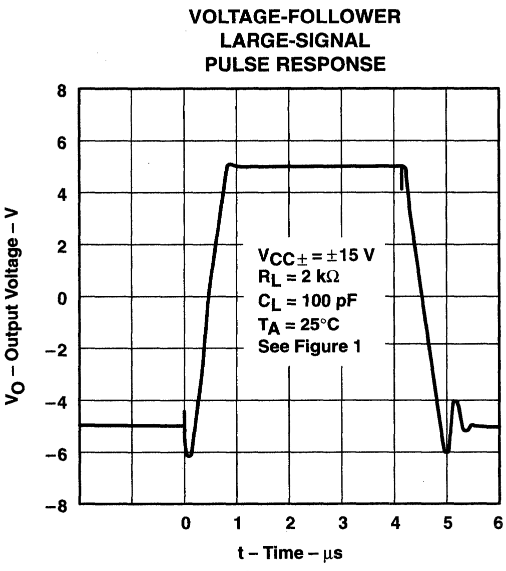
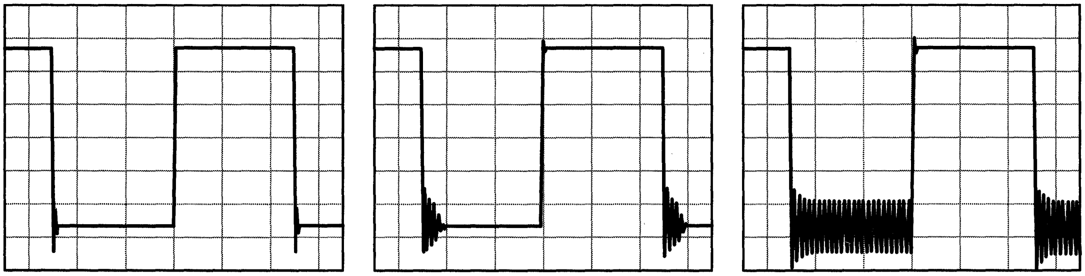


Figure 80

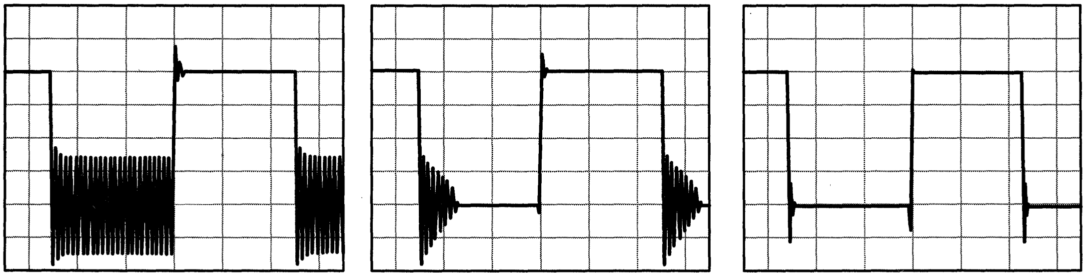
APPLICATION INFORMATION

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL05x and TL05xA drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 81 and Figure 82).

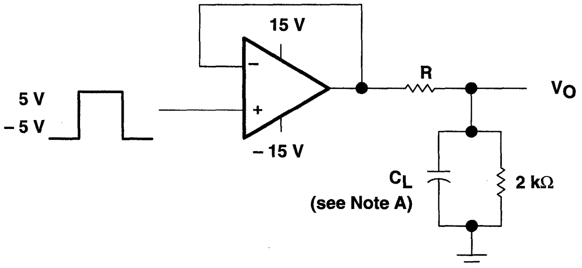


(a) C_L = 100 pF, R = 0 **(b) C_L = 300 pF, R = 0** **(c) C_L = 350 pF, R = 0**



(d) C_L = 1000 pF, R = 0 **(e) C_L 1000 pF, R = 50 Ω** **(f) C_L = 1000 pF, R = 2 kΩ**

Figure 81. Effect of Capacitive Loads



NOTE A: C_L includes fixture capacitance.

Figure 82. Test Circuit for Output Characteristics

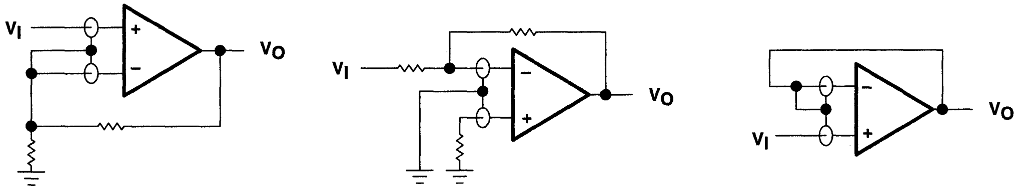
APPLICATION INFORMATION

input characteristics

The TL05x and TL05xA are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL05x and TL05xA are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 83). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 83. Use of Guard Rings

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL05x and TL05xA result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

APPLICATION INFORMATION

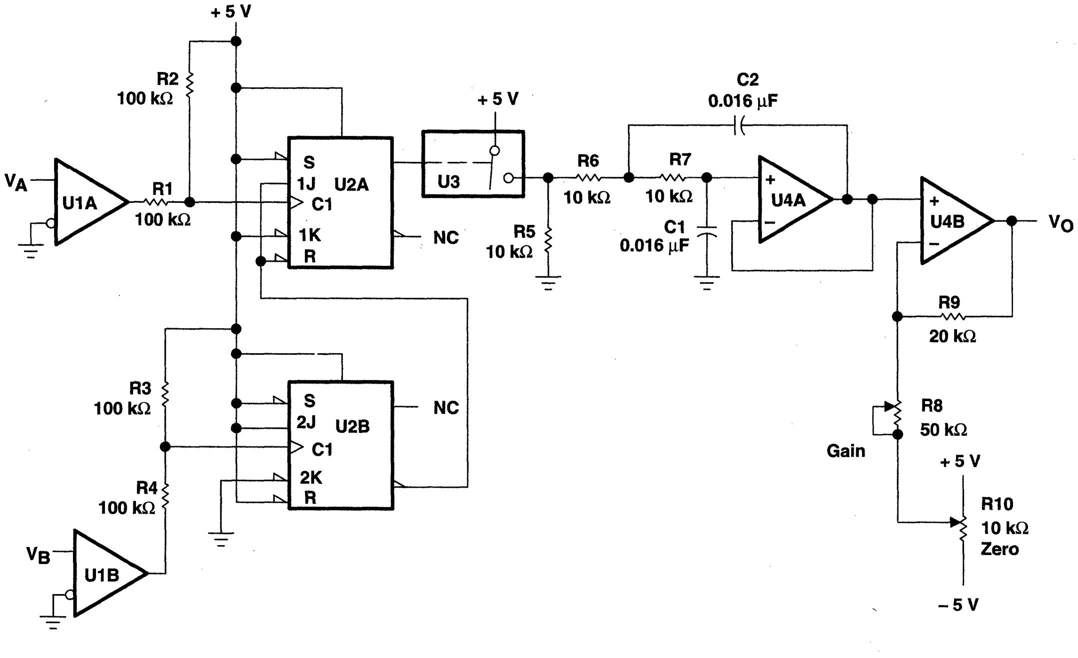
phase meter

The phase meter in Figure 84 produces an output voltage of 10 mV per degree of phase delay between the two input signals V_A and V_B. The reference signal V_A must be the same frequency as V_B. The TLC3702 comparators (U1) convert these two input sine waves into ±5-V square waves. Then R1 and R4 provide level shifting prior to the SN74HC109 dual J-K flip flops.

Flip-flop U2B is connected as a toggle flip-flop and generates a square wave at half the frequency of V_B. Flip-flop U2A also produces a square wave at half the input frequency. The pulse duration of U2A varies from zero to half the period, where zero corresponds to zero phase delay between V_A and V_B and half the period corresponds to V_B lagging V_A by 360 degrees.

The output pulse from U2A causes the TLC4066 (U3) switch to charge the TL05x (U4) integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of U4A approximates a square wave and U2A has an output of almost 2.5 V. U4B acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0- to 2.5-V integrator output to a 0- to 3.6-V output range.

R8 and R10 provide output gain and zero-level calibration. This circuit operates over a 100-Hz to 10-kHz frequency range.



NOTE A: U1 = TLC3702; $V_{CC\pm} = \pm 5$ V
U2 = SN74HC109
U3 = TLC4066
U4, U5 = TL05x; $V_{CC\pm} = \pm 5$ V

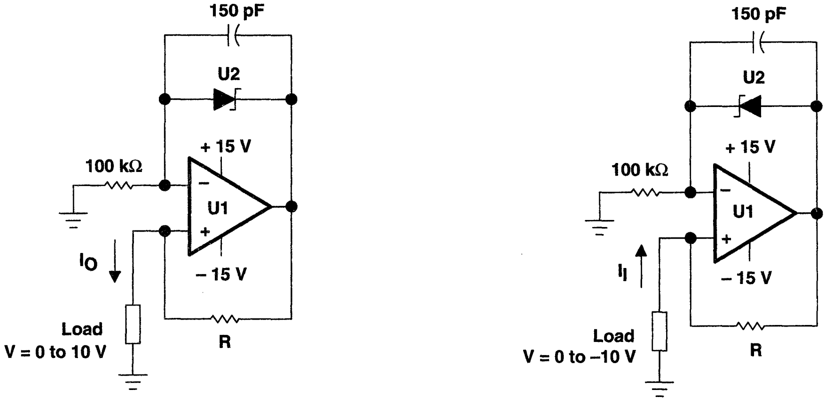
Figure 84. Phase Meter

APPLICATION INFORMATION

precision constant-current source over temperature

A precision current source (see Figure 85) benefits from the high input impedance and stability of Texas Instruments enhanced-JFET process. A low-current shunt regulator maintains 2.5 V between the inverting input and the output of the TL05x. The negative feedback then forces 2.5 V across the current setting resistor R; therefore, the current to the load is simply 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. If the regulator's cathode connects to the operational amplifier output, this circuit sources load current. Similarly, if the cathode connects to the inverting input, the circuit sinks current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split-voltage supplies.



(a) SOURCE CURRENT LOAD (b) SINK CURRENT LOAD

NOTE B: U1 = 1/2 TL05x
U2 = LM385, LT1004, or LT1009 voltage reference
$I = \frac{2.5\text{ V}}{R}$, R = Low temperature coefficient metal film resistor

Figure 85. Precision Constant-Current Source

APPLICATION INFORMATION

instrumentation amplifier with adjustable gain/null

The instrumentation amplifier in Figure 86 benefits greatly from the high input impedance and stable input offset voltage of the TL05xA. Amplifiers U1A, U1B, and U2A form the actual instrumentation amplifier, while U2B provides offset null. Potentiometer R1 provides gain adjust. With R1 = 2 kΩ, the circuit gain equals 100, while with R1 = 200 kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

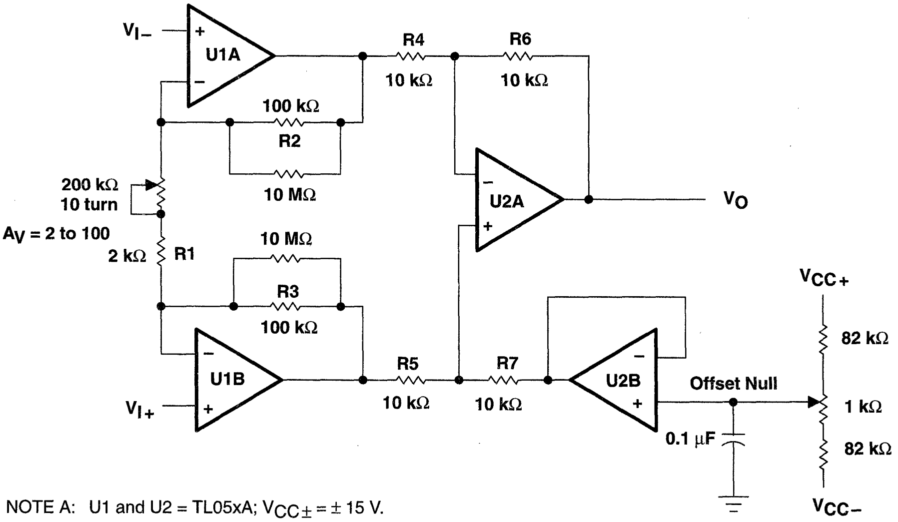
$$A_V = 1 + \left(\frac{R2 + R3}{R1}\right)$$

Readjusting the offset null is necessary whenever the circuit gain is changed. If U2B is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL05xA minimizes the dc error of the circuit. For best matching, all resistors should be one percent tolerance. The matching between R4, R5, R6, and R7 controls the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This dc error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature also creates an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs minimizes the error resulting from change in input offset voltage with time. Assuming V_I equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2}\left[\left(1 + \frac{R3}{R1}\right)\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R2}{R1}\left(\frac{R6}{R4}\right)\right]$$

$$-V_{IO1}\left[\frac{R3}{R1}\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R6}{R4}\left(1 + \frac{R2}{R1}\right)\right] + V_{IO3}\left(1 + \frac{R6}{R4}\right)$$



NOTE A: U1 and U2 = TL05xA; $V_{CC\pm} = \pm 15$ V.

Figure 86. Instrumentation Amplifier

APPLICATION INFORMATION

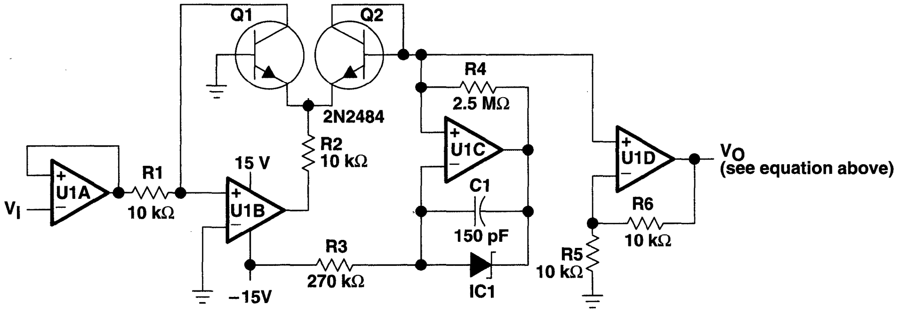
high input impedance log amplifier

The low input offset voltage and high input impedance of the TL05xA creates a precision log amplifier (see Figure 87). IC1 is a 2.5-V, low-current precision, shunt regulator. Transistors Q1 and Q2 must be a closely matched NPN pair. For best performance over temperature, R4 should be a metal film resistor with a low temperature coefficient.

In this circuit, U1A serves as a high-impedance unity-gain buffer. Amplifier U1B converts the input voltage to a current through R1 and Q1. Amplifier U1C, IC1, and R4 form a 1-µA temperature-stable current source that sets the base-emitter voltage of Q2. U1D amplifies the difference between the base-emitter voltage of Q1 and Q2 (see Figure 88). The output voltage is given by the following equation:

$$V_O = -\left[1 + \frac{R6}{R5}\right] \frac{kT}{q} \left[\ln \frac{V_I}{\left(R1 \times 1 \times 10^{-6}\right)}\right]$$

where k = 1.38 × 10^{-23}, q = 1.602 × 10^{-19}, and T is in degrees kelvin.



NOTE A: U1A through U1D = TL05xA. IC1 = LM385, LT1004, or LT1009 voltage reference.

Figure 87. Log Amplifier

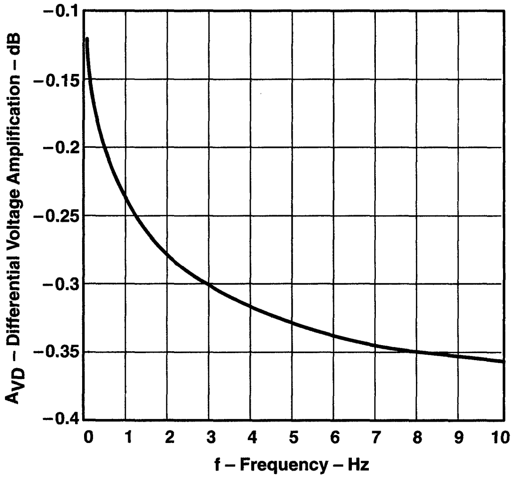


Figure 88. Output Voltage vs Input Voltage for Log Amplifier

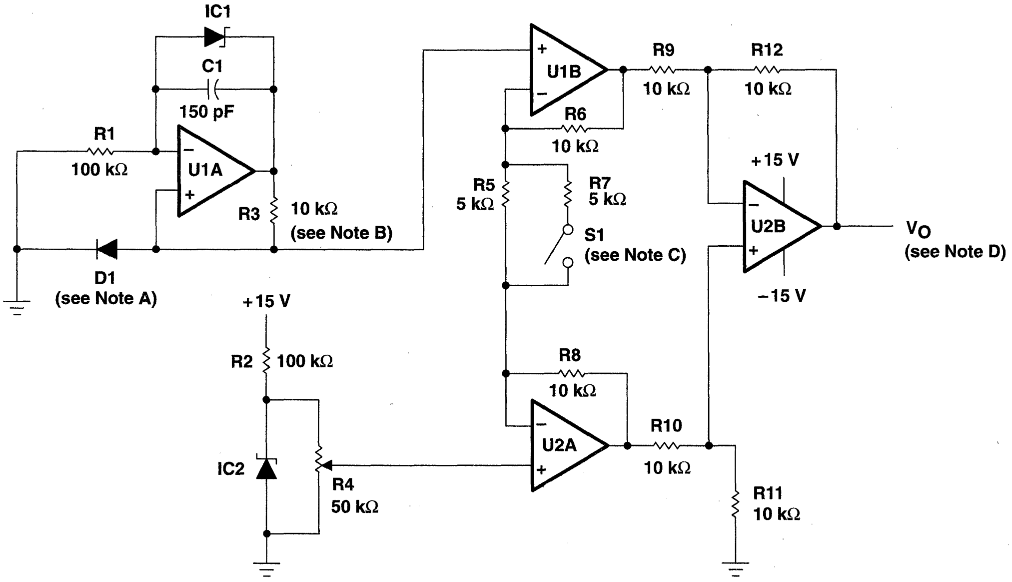
APPLICATION INFORMATION

analog thermometer

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precise analog thermometer can be built (see Figure 89). Amplifier U1A and IC1 establish a constant current through the temperature-sensing diode D1. For this section of the circuit to operate correctly, the TL05x must use split supplies and R3 must be a metal-film resistor with a low temperature coefficient.

The temperature-sensitive voltage from the diode is compared to a temperature-stable voltage reference set by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperature. Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer remains constant.

Amplifiers U1B, U2A, and U2B form the instrumentation amplifier that converts the difference between the diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifier gain equals 5 and the output voltage is proportional to temperature in degrees Celsius. With S1 open, the amplifier gain is 9 and the output is proportional to temperature in degrees Fahrenheit. Every time that S1 is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degree (C or F).



NOTES: A. Temperature-sensing diode ≈ (–2 mV/°C)
B. Metal-film resistor (low temperature coefficient)
C. Switch open for °F and closed for °C
D. V_O α temperature; 10 mV/°C or 10 mV/°F
E. U1, U2 = TL05x. IC1, IC2 = LM385, LT1004, or LT1009 voltage reference

Figure 89. Analog Thermometer

APPLICATION INFORMATION

voltage-ratio-to-dB converter

The application in Figure 90 measures the amplitude ratio of two signals and then converts the ratio to decibels (see Figure 91). The output voltage provides a resolution of 100 mV/dB. The two inputs can be either dc or sinusoidal ac signals. When using ac signals, both signals should be the same frequency or output glitches will occur. For measuring two input signals of different frequencies, extra filtering should be added after the rectifiers.

The circuit contains three low-offset TL05xA devices. Two of these devices provide the rectification and logarithmic conversion of the inputs. The third TL05xA forms an instrumentation amplifier. The stage performing the logarithmic conversion also requires two well-matched npn transistors.

The input signal first passes through a high impedance unity-gain buffer U1A (U2A). Then U1B (U2B) rectifies the input signal at a gain of 0.5, and U1C (U2C) provides a noninverting gain of 2 so that the system gain is still one. U1D (U2D), R6 (R13), and Q1 (Q2) perform the logarithmic conversion of the rectified input signal. The instrumentation amplifier formed by U3A, U3B, U3D scales the difference of the two logarithmic voltages by a gain of 33.6. As a result, the output voltage equals 100 mV/dB. The 1-kΩ potentiometer on the input of U3C calibrates the zero dB reference level. The following equations are used to derive the relationship between the input voltage ratio expressed in decibels and the output voltage.

$$X\ \text{dB} = 20\ \log\left[\frac{V_A}{V_B}\right] = 20\left[\frac{\ln\left(V_A\right) - \left(V_B\right)}{\ln\ (10)}\right]$$

$$X\ \text{dB} = 8.686\left[\ln\left(V_A\right) - \ln\left(V_B\right)\right]$$

$$V_{BE(Q1)} = \frac{kT}{q}\ \ln\left[\frac{V_A}{R \times I_S}\right] \qquad V_{BE(Q2)} = \frac{kT}{q}\ \ln\left[\frac{V_B}{R \times I_S}\right]$$

$$\Delta V_{BE} = V_{BE(Q1)} - V_{BE(Q2)} = \frac{kT}{q}\left[\ln\left(V_A\right) - \ln\left(V_B\right)\right]$$

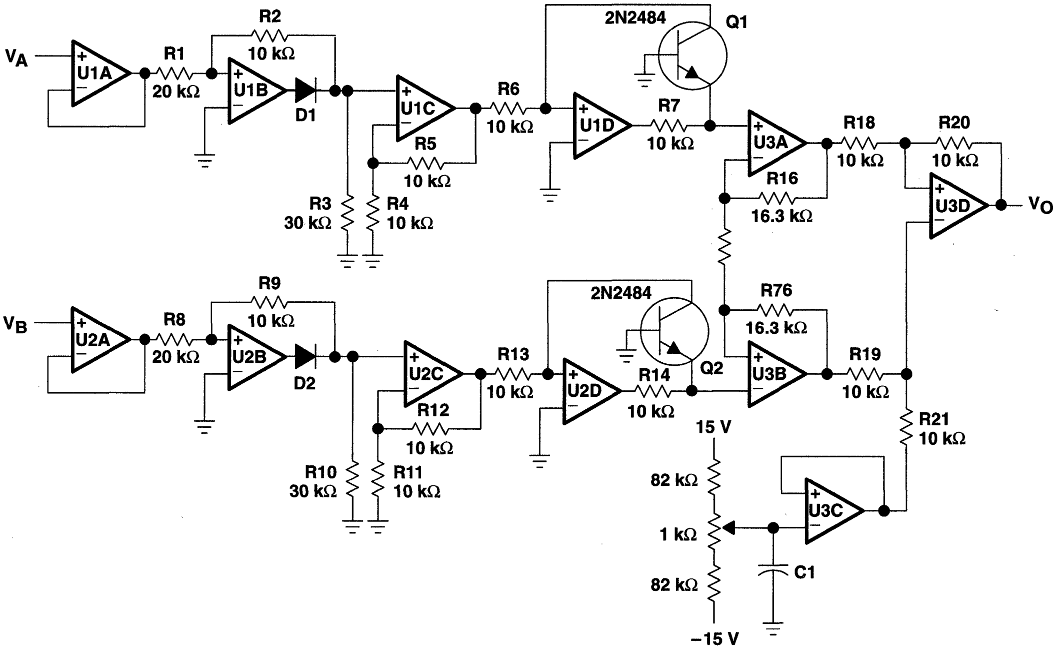
$$X\ \text{dB} = \frac{8.686}{kT/q}\left[V_{BE(Q1)} - V_{BE(Q2)}\right] = 336\left[V_{BE(Q1)} - V_{BE(Q2)}\right]\ \text{at } 25^\circ\text{C}$$

where

$k = 1.38 \times 10^{-23}$, $q = 1.602 \times 10^{-19}$, and T is in kelvins.

This would give a resolution of 1 V/dB. Therefore, the gain of the instrumentation amplifier is set at 33.6 to obtain 100 mV/dB.

APPLICATION INFORMATION



NOTE A: U1A through U3D = TL05xA, $V_{CC\pm} = \pm 15$ V. D1 and D2 = 1N914.

Figure 90. Voltage-Ratio-to-dB Converter

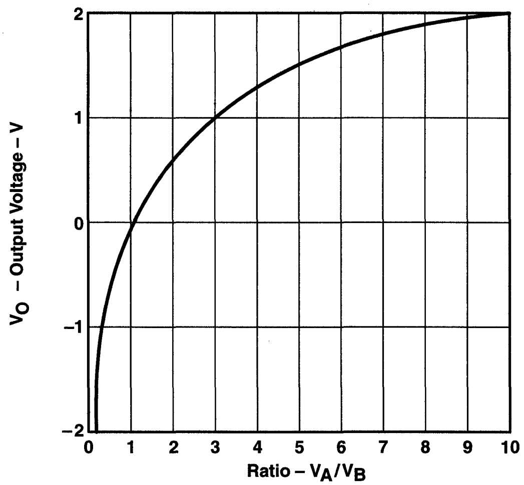


Figure 91. Output Voltage vs the Ratio of the Input Voltages for Voltage-to-dB Converter

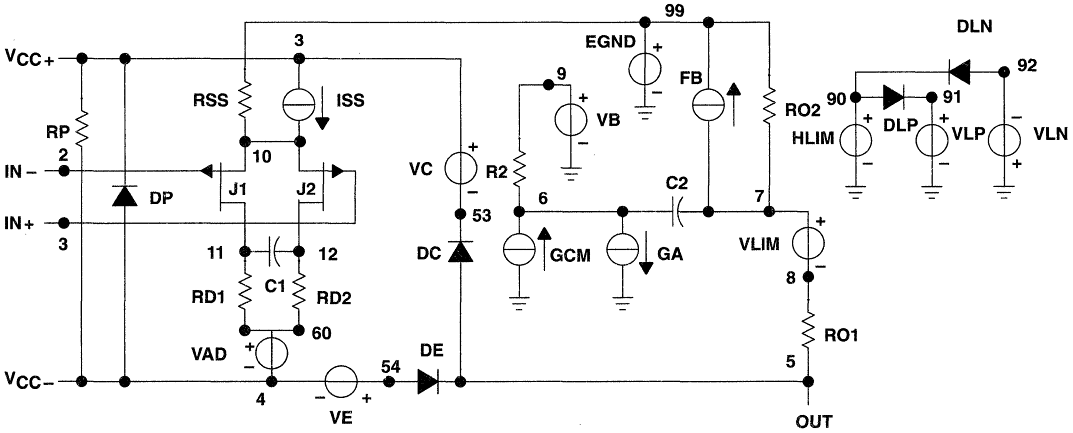
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit Figure 92 are generated using the TL05x typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



```
.SUBCKT TL05x 1 2 3 4 5
        C1      11     12     3.988E–12
        C2      6      7      15.00E–12
        DC      5      53     DX
        DE      54     5      DX
        DLP     90     91     DX
        DLN     92     90     DX
        DP      4      3      DX
        EGND    99     0      POLY (2) (3,0) (4,0) 0 .5 .5
        FB      7      99     POLY (5) VB VC VE VLP
        + VLN 0 2.875E6 –3E6 3E6 3E6 –3E6
        GA      6      0      11     12 292.2E–6
        GCM     0      6      10     99 6.542E–9
        ISS     3      10     DC 300.0E–6
        HLIM    90     0      VLIM 1K
        J1      11     2      10 JX
        J2      12     1      10 JX
        R2      6      9      100.0E3
RD1     4      11     3.422E3
RD2     4      12     3.422E3
R01     8      5      125
R02     7      99     125
RP      3      4      11.11E3
RSS     10     99     666.7E6
VB      9      0      DC 0
VC      3      53     DC 3
VE      54     4      DC 3.7
VLIM    7      8      DC 0
VLP     91     0      DC 28
VLN     0      92     DC 28
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=15.00E–12 BETA=185.2E–6
+ VTO=–.1)
.ENDS
```

Figure 92. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

TL061, TL061A, TL061B, TL061Y, TL062, TL062A TL062B, TL062Y, TL064, TL064A, TL064B, TL064Y LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS078C – NOVEMBER 1978 – REVISED AUGUST 1996

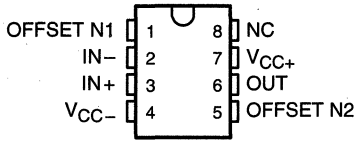
- **Very Low Power Consumption**
- **Typical Supply Current . . . 200 μA (per Amplifier)**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Common-Mode Input Voltage Range Includes V_{CC+}**
- **Output Short-Circuit Protection**
- **High Input impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 3.5 V/μs Typ**

description

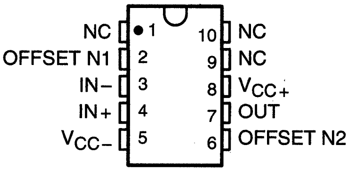
The JFET-input operational amplifiers of the TL06_ series are designed as low-power versions of the TL08_ series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The TL06_ series feature the same terminal assignments as the TL07_ and TL08_ series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and the M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

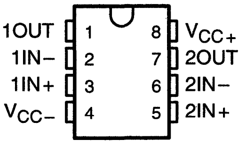
TL061, TL061A, TL061B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



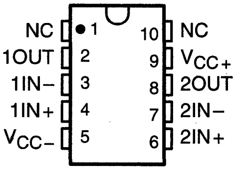
TL061 . . . U PACKAGE
(TOP VIEW)



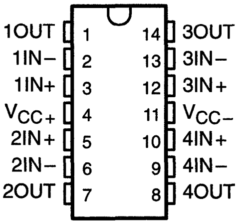
TL062, TL062A, TL062B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



TL062 . . . U PACKAGE
(TOP VIEW)

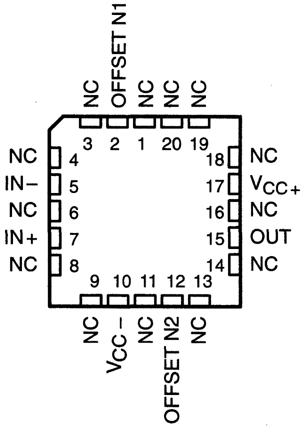


TL064 . . . D, J, N, PW, OR W PACKAGE
TL064A, TL064B . . . D OR N PACKAGE
(TOP VIEW)

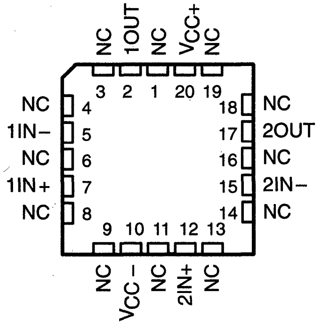


NC – No internal connection

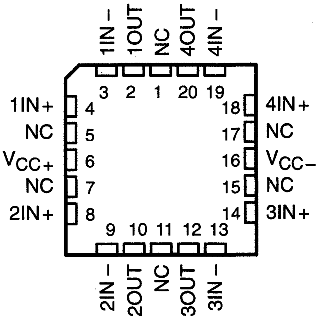
TL061 . . . FK PACKAGE
(TOP VIEW)



TL062 . . . FK PACKAGE
(TOP VIEW)



TL064 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

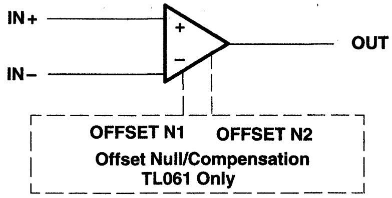
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D008)†	**SMALL OUTLINE (D014)†**	**PLASTIC DIP (N)**	**PLASTIC DIP (P)**	**TSSOP (PW)**	
0°C to 70°C	15 mV	TL061CD			TL061CP	TL061CPW	TL061Y
	6 mV	TL061ACD			TL061ACP		
	3 mV	TL061BCD			TL061BCP		
	15 mV	TL062CD			TL062CP	TL062CPW	TL062Y
	6 mV	TL062ACD			TL062ACP		
	3 mV	TL062BCD			TL062BCP		
	15 mV		TL064CD	TL064CN		TL064CPW	TL064Y
	6 mV		TL064ACD	TL064ACN			
	3 mV		TL064BCD	TL064BCN			

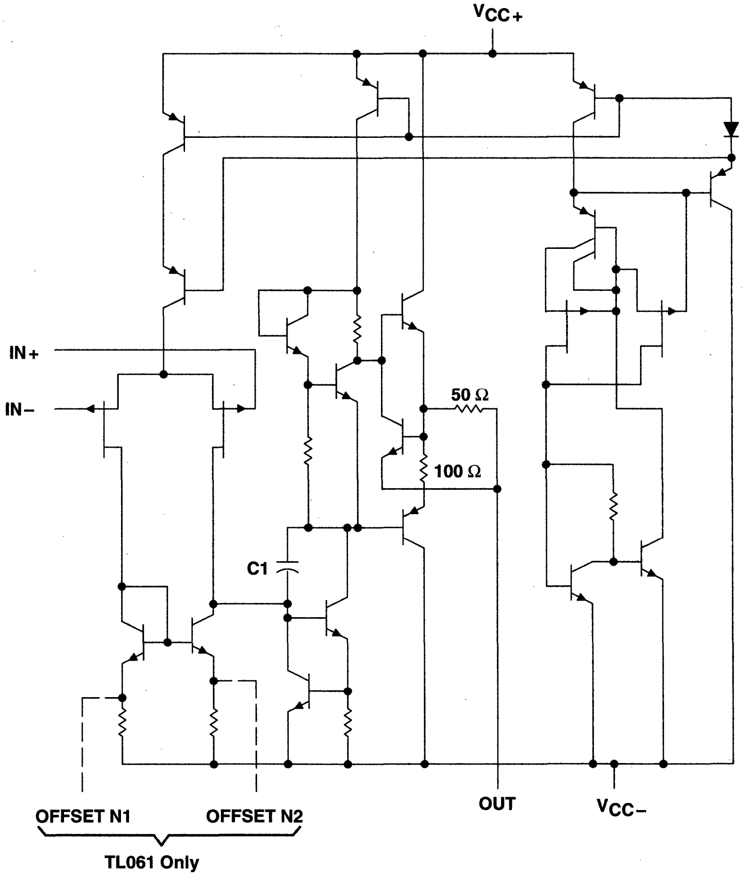
T_A	V_{IO}max AT 25°C	PACKAGE								
		SMALL OUTLINE (D008)†	**SMALL OUTLINE (D014)†**	**CHIP CARRIER (FK)**	**CERAMIC DIP (J)**	**CERAMIC DIP (JG)**	**PLASTIC DIP (N)**	**PLASTIC DIP (P)**	**FLAT PACK (U)**	**FLAT PACK (W)**
−40°C to 85°C	6 mV	TL061ID TL062ID	TL064ID				TL064IN	TL061IP TL062IP		
−55°C to 125°C	6 mV			TL061MFK		TL061MJG			TL061MU	
	6 mV			TL062MFK		TL062MJG			TL062MU	
	9 mV			TL064MFK	TL064MJ					TL064MW

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL061CDR).

symbol (each amplifier)



schematic (each amplifier)

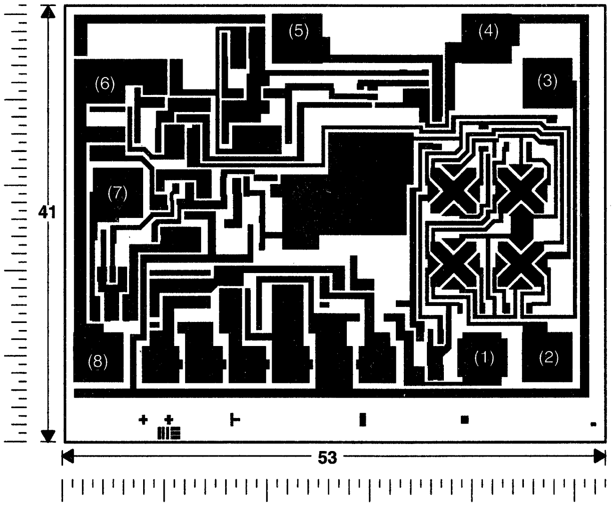


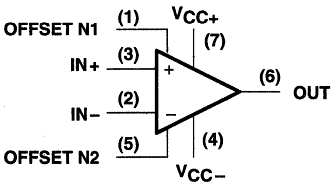
C1 = 10 pF on TL061, TL062, and TL064
Component values shown are nominal.

TL061Y chip information

This chip, when properly assembled, displays characteristics similar to the TL061. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

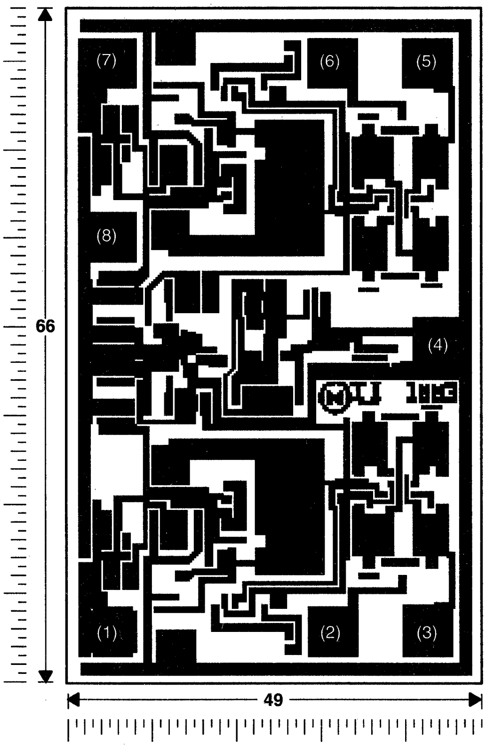
ALL DIMENSIONS ARE IN MILS.

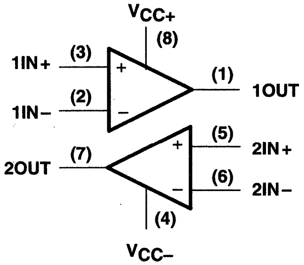
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TL062Y chip information

This chip, when properly assembled, displays characteristics similar to the TL062. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

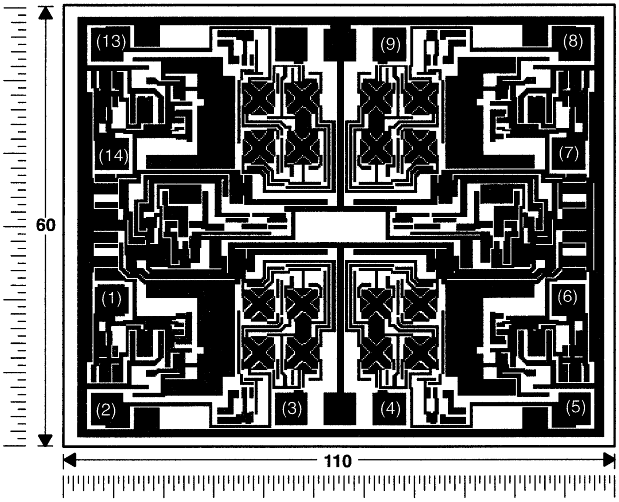
ALL DIMENSIONS ARE IN MILS.

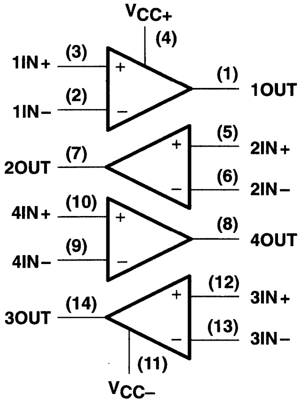
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TL064Y chip information

This chip, when properly assembled, displays characteristics similar to the TL064. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		TL06_C TL06_AC TL06_BC	TL06_I	TL06_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage, V_{ID} (see Note 2)		±30	±30	±30	V
Input voltage, V_I (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	−40 to 85	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package			300	°C
Lead temperature 1,6 mm (1/6 inch) from case for 10 seconds	D, N, P, or PW package	260	260		°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values except differential voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	33°C	465 mW	378 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	25°C	448 mW	N/A	N/A
U	675 mW	5.4 mW/°C	25°C	432 mW	351 m/W	135 mW
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL061C TL062C TL064C			TL061AC TL062AC TL064AC			TL061BC TL062BC TL064BC			TL061I TL062I TL064I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	15		3	6		2	3		3	6	mV
			T_A = Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = Full range			10			10			10			10		µV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	200		5	100		5	100		5	100	pA
			T_A = Full range			5			3			3			10	nA
I_{IB}	Input bias current‡	V_O = 0	T_A = 25°C		30	400		30	200		30	200		30	200	pA
			T_A = Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ,	T_A = 25°C	±10	±13.5		±10	±13.5		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ,	T_A = Full range	±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L ≥ 10 kΩ	T_A = 25°C	3	6		4	6		4	6		4	6		V/mV
			T_A = Full range	3			4			4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ,	T_A = 25°C		1			1			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω, T_A = 25°C		70	86		80	86		80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ± 9 V to ± 15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		70	95		80	95		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	V_O = 0, T_A = 25°C, No load			6	7.5		6	7.5		6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	V_O = 0, T_A = 25°C, No load			200	250		200	250		200	250		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100,	T_A = 25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06_C, TL06_AC, and TL06_BC and −40°C to 85°C for TL06_I.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 15. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL061M TL062M			TL064M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	6		3	9	mV
			$T_A = -55°C$ to $125°C$			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, $T_A = -55°C$ to $125°C$			10			10		µV/°C
I_{IO}	Input offset current	$V_O = 0$	$T_A = 25°C$		5	100		5	100	pA
			$T_A = -55°C$ to $125°C$			20			20	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		30	200		30	200	pA
			$T_A = -55°C$ to $125°C$			50			50	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11.5	−12 to 15		±11.5	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$, $T_A = 25°C$		±10	±13.5		±10	±13.5		V
		$R_L \geq 10\ k\Omega$, $T_A = -55°C$ to $125°C$		±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L \geq 10\ k\Omega$	$T_A = 25°C$	4	6		4	6		V/mV
			$T_A = -55°C$ to $125°C$	4			4			
B_1	Unity-gain bandwidth	$R_L = 10\ k\Omega$, $T_A = 25°C$								MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm9$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	$V_O = 0$, $T_A = 25°C$, No load			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	$V_O = 0$, $T_A = 25°C$, No load			200	250		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25°C$			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 15. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Note 5)	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 10\ k\Omega$, See Figure 1	1.5	3.5		V/µs
t_r	Rise time	$V_I = 20$ V, $C_L = 100$ pF,	$R_L = 10\ k\Omega$, See Figure 1		0.2		µs
	Overshoot factor				10%		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$,	f = 1 kHz		42		nV/√Hz

NOTE 5: Slew rate at −55°C to 125°C is 0.7 V/µs min.

electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL061Y TL062Y TL064Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$		3	15	mV
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$		10		µV/°C
I_{IO}	Input offset current	$V_O = 0$		5	200	pA
I_{IB}	Input bias current‡	$V_O = 0$		30	400	pA
V_{ICR}	Common-mode input voltage range		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	±10	±13.5		V
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	3	6		V/mV
B_1	Unity-gain bandwidth	$R_L = 10\ k\Omega$		1		MHz
r_i	Input resistance			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	70	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$	70	95		dB
P_D	Total power dissipation (each amplifier)	$V_O = 0$, No load		6	7.5	mW
I_{CC}	Supply current (per amplifier)	$V_O = 0$, No load		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 15. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TL061Y TL062Y TL064Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_I = 10$ mV, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1	1.5	3.5		V/µs
t_r	Rise time	$V_I = 20$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.2		µs
	Overshoot factor			10%		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$, $f = 1$ kHz		42		nV/√Hz

PARAMETER MEASUREMENT INFORMATION

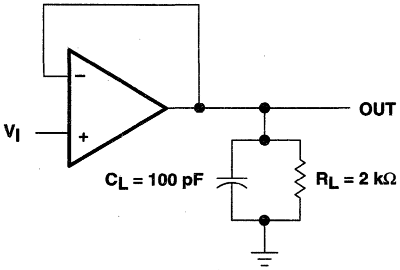


Figure 1. Unity-Gain Amplifier

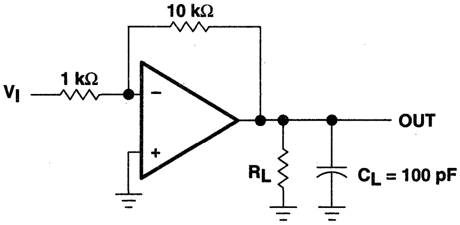


Figure 2. Gain-of-10 Inverting Amplifier

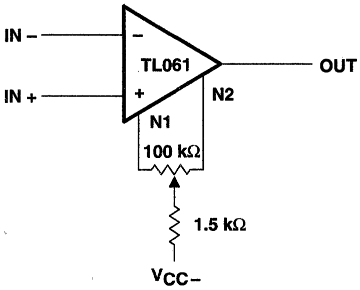


Figure 3. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OM}	Maximum output voltage	vs Supply voltage vs Free-air temperature vs Load resistance vs Frequency	4 5 6 7
A_{VD}	Differential voltage amplification	vs Free-air temperature	8
A_{VD}	Large-signal differential voltage amplification	vs Frequency	9
	Phase shift	vs Frequency	9
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	10 11
P_D	Total power dissipation	vs Free-air temperature	12
CMRR	Common-mode rejection ratio	vs Free-air temperature	13
	Normalized unity-gain bandwidth	vs Free-air temperature	14
	Normalized slew rate	vs Free-air temperature	14
	Normalized phase shift	vs Free-air temperature	14
I_{IB}	Input bias current	vs Free-air temperature	15
	Large-signal pulse response	vs Time	16
V_O	Output voltage	vs Elapsed time	17
V_n	Equivalent input noise voltage	vs Frequency	18

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

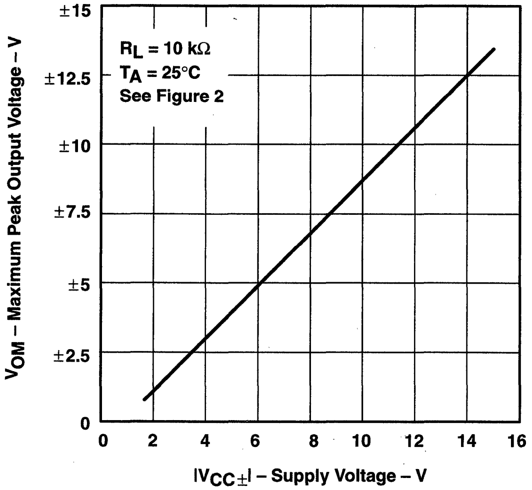


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

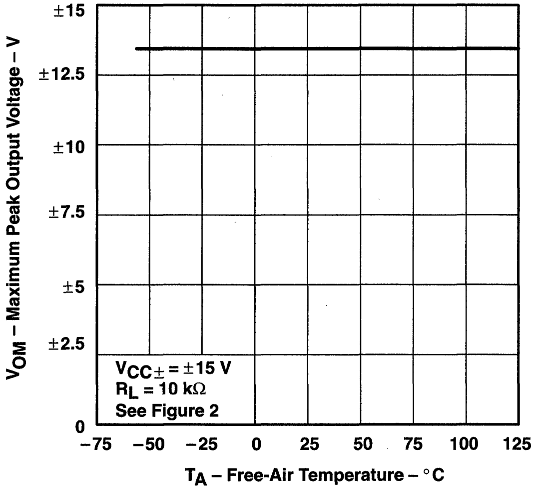


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

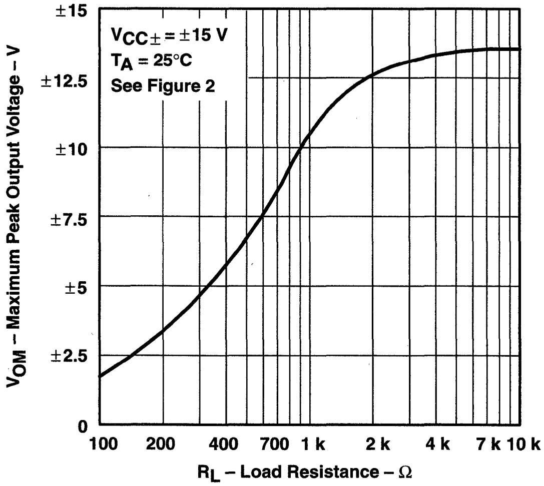


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

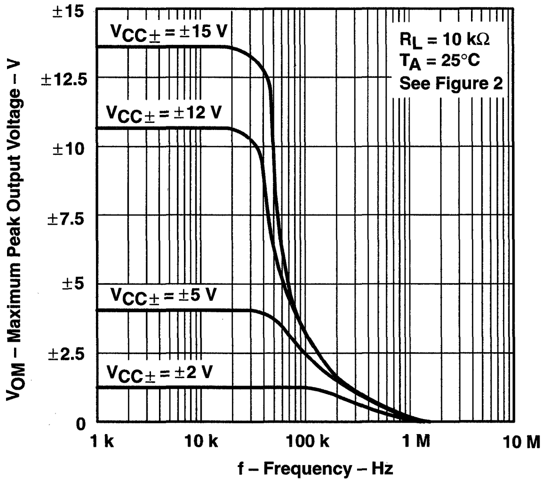


Figure 7

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

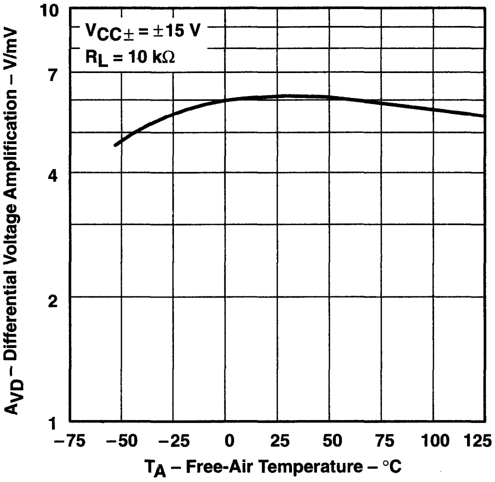

Figure 8

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

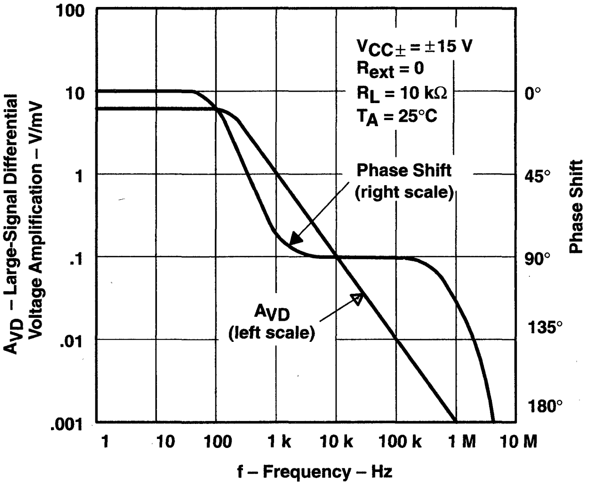

Figure 9

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

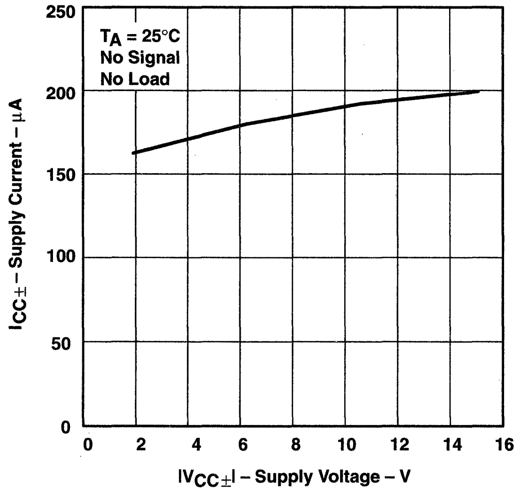


Figure 10

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

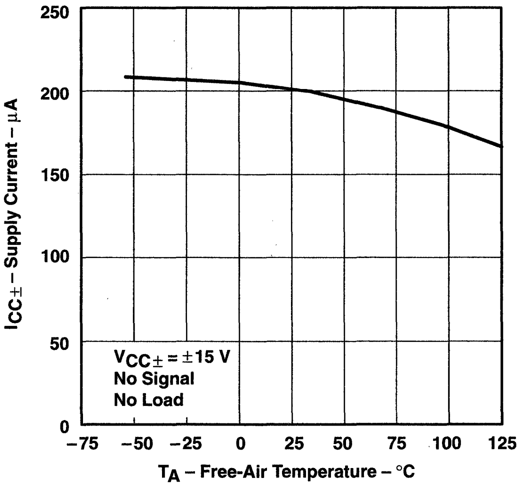


Figure 11

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

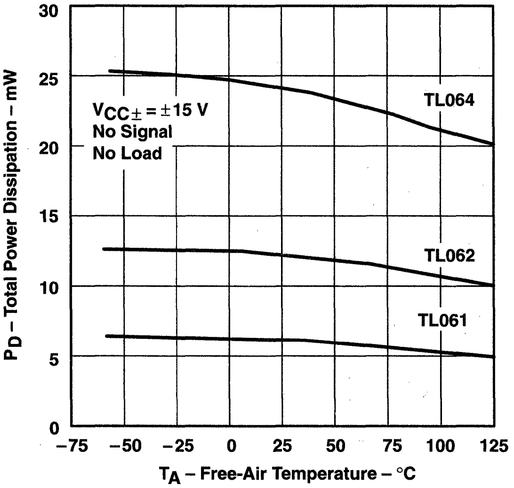


Figure 12

ALL EXCEPT TL06_C
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

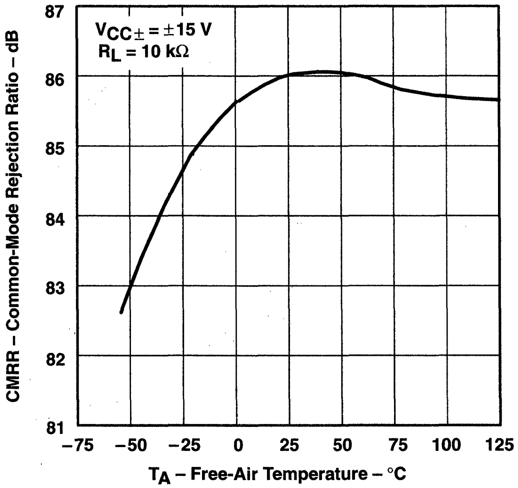


Figure 13

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

NORMALIZED UNITY GAIN BANDWIDTH SLEW RATE, AND PHASE SHIFT vs FREE-AIR TEMPERATURE

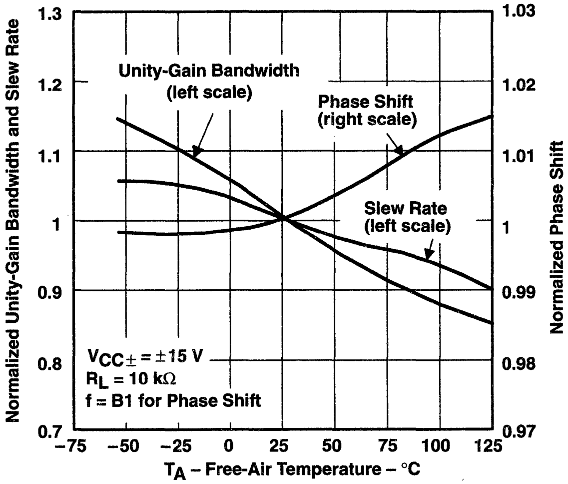


Figure 14

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

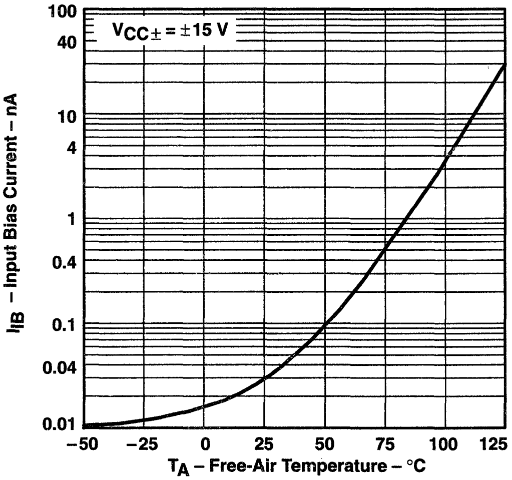


Figure 15

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

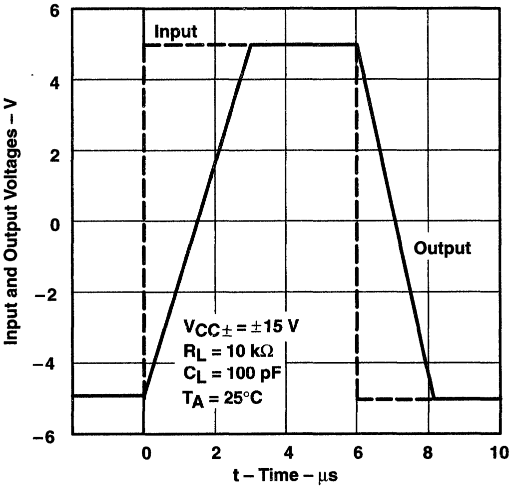


Figure 16

TYPICAL CHARACTERISTICS

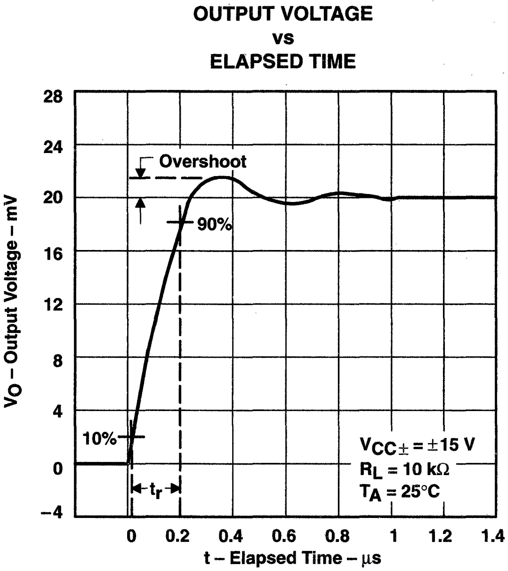


Figure 17

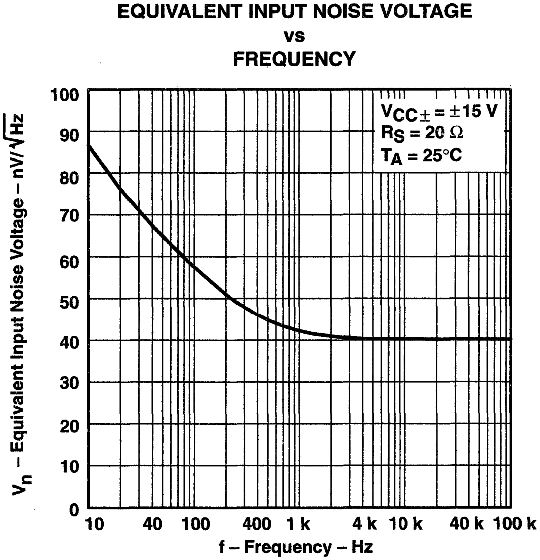


Figure 18

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
Instrumentation filter	TL064	19
0.5-Hz square-wave oscillator	TL061	20
High-Q notch filter	TL061	21
Audio-distribution amplifier	TL064	22
Low-level light detector preamplifier	TL061	23
AC amplifier	TL061	24
Microphone preamplifier with tone control	TL061	25
Instrumentation amplifier	TL062	26
IC preamplifier	TL062	27

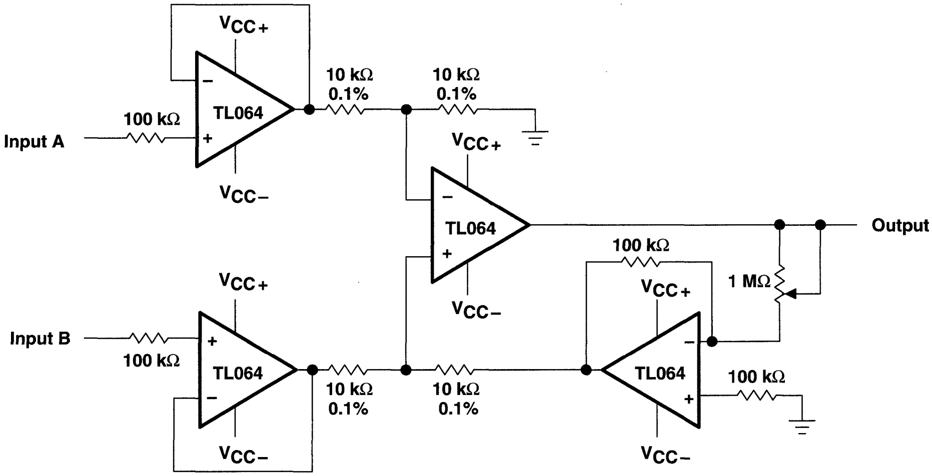
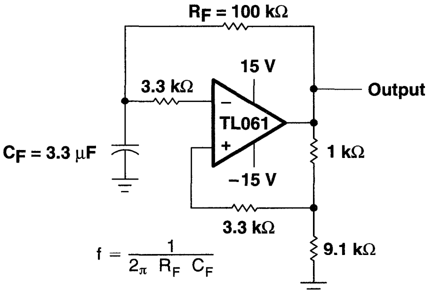
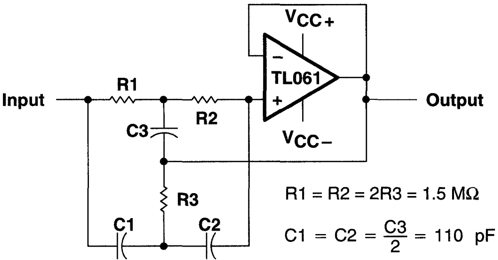


Figure 19. Instrumentation Amplifier



$$f = \frac{1}{2\pi\ R_F\ C_F}$$

Figure 20. A 0.5-Hz Square-Wave Oscillator



$R1 = R2 = 2R3 = 1.5\ M\Omega$

$C1 = C2 = \frac{C3}{2} = 110\ pF$

$f_o = \frac{1}{2\pi\ R1\ C1} = 1\ kHz$

Figure 21. High-Q Nothc Filter

APPLICATION INFORMATION

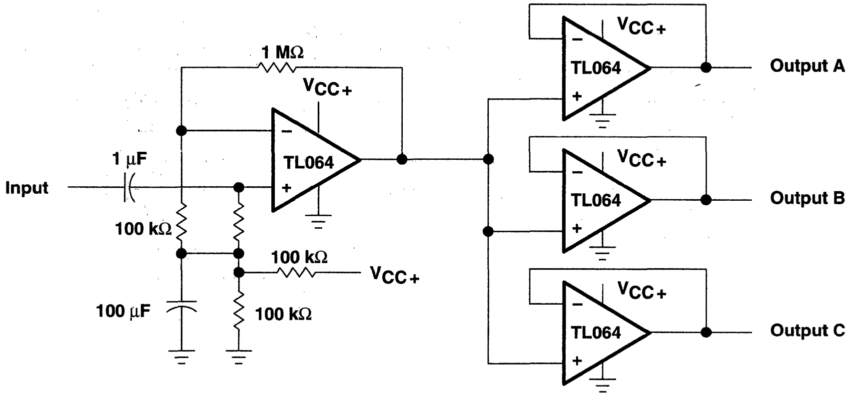


Figure 22. Audio-Distribution Amplifier

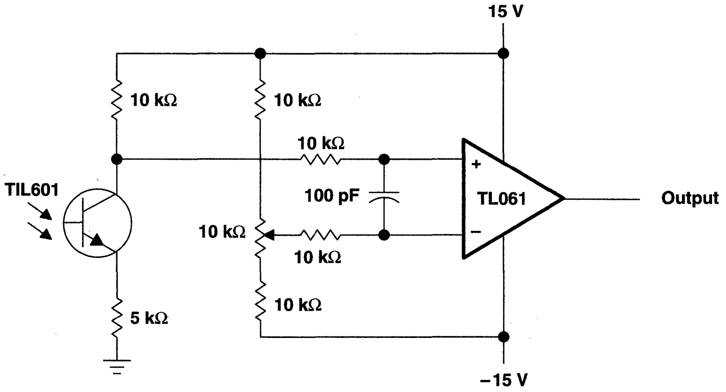


Figure 23. Low-Level Light-Detector Preamplifier

APPLICATION INFORMATION

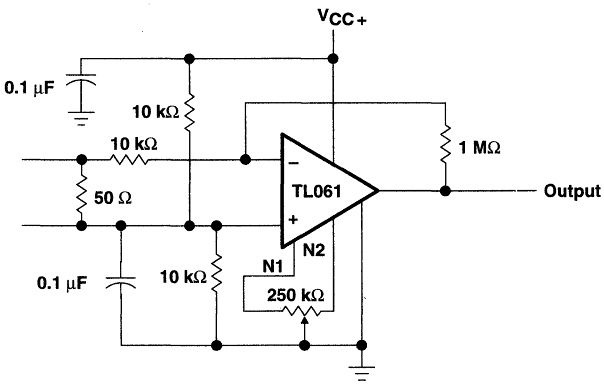


Figure 24. AC Amplifier

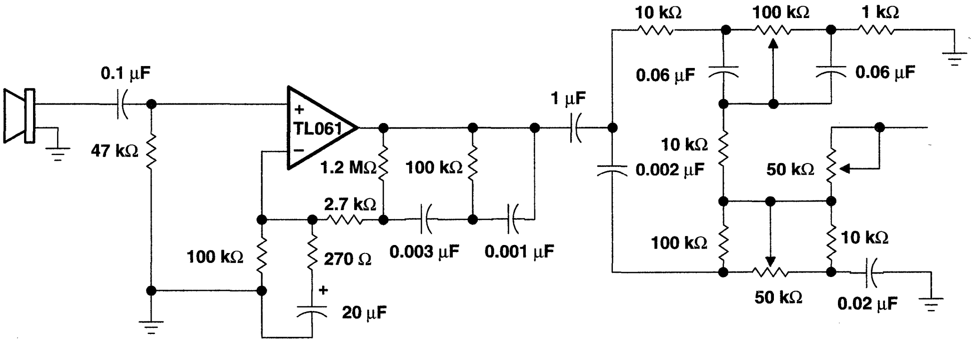


Figure 25. Microphone Preamplifier With Tone Control

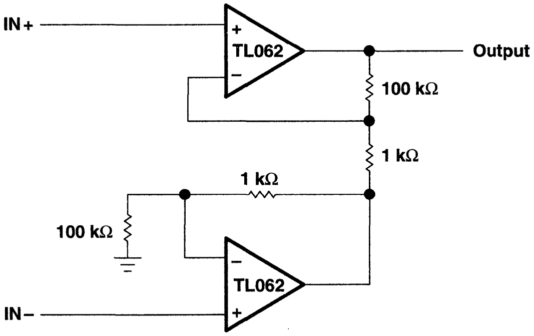
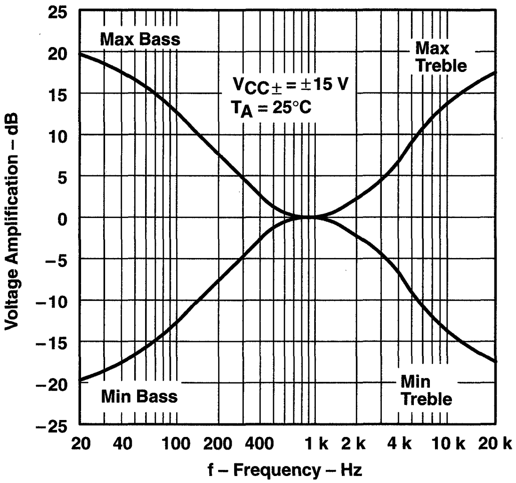


Figure 26. Instrumentation Amplifier

APPLICATION INFORMATION

IC PREAMPLIFIER RESPONSE CHARACTERISTICS



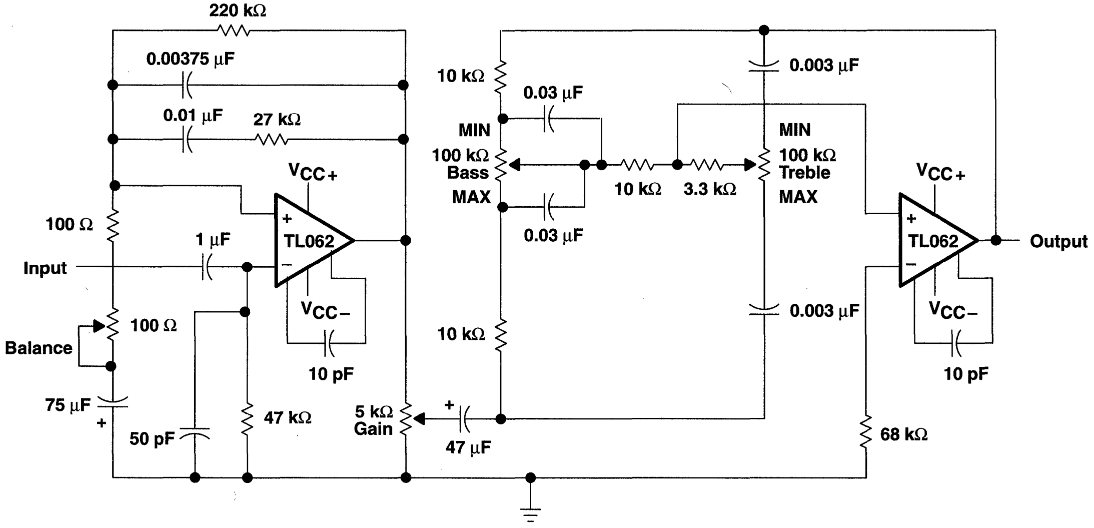


Figure 27. IC Preamplifier

TL064x2
LOW-POWER JFET-INPUT
OCTAL OPERATIONAL AMPLIFIER

SLOS134 – APRIL 1994

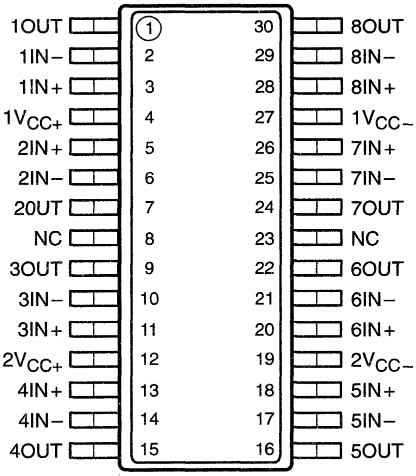
- **Very Low Power Consumption**
- **Typical Supply Current . . . 200 μA (Per Amplifier)**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Common-Mode Input Voltage Range Includes V_{CC+}**
- **Output Short-Circuit Protection**
- **High Input Impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 3.5 V/μs Typ**

description

The TL064x2 JFET-input operational amplifier is designed as a low-power version of the TL084x2 amplifier. It features high input impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The TL064x2 features the same terminal assignments as the TL074x2 and TL084x2. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

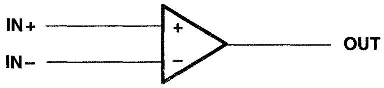
The TL064x2 is characterized for operation from 0°C to 70°C.

DB PACKAGE
(TOP VIEW)



NC – No internal connection

symbol (each amplifier)

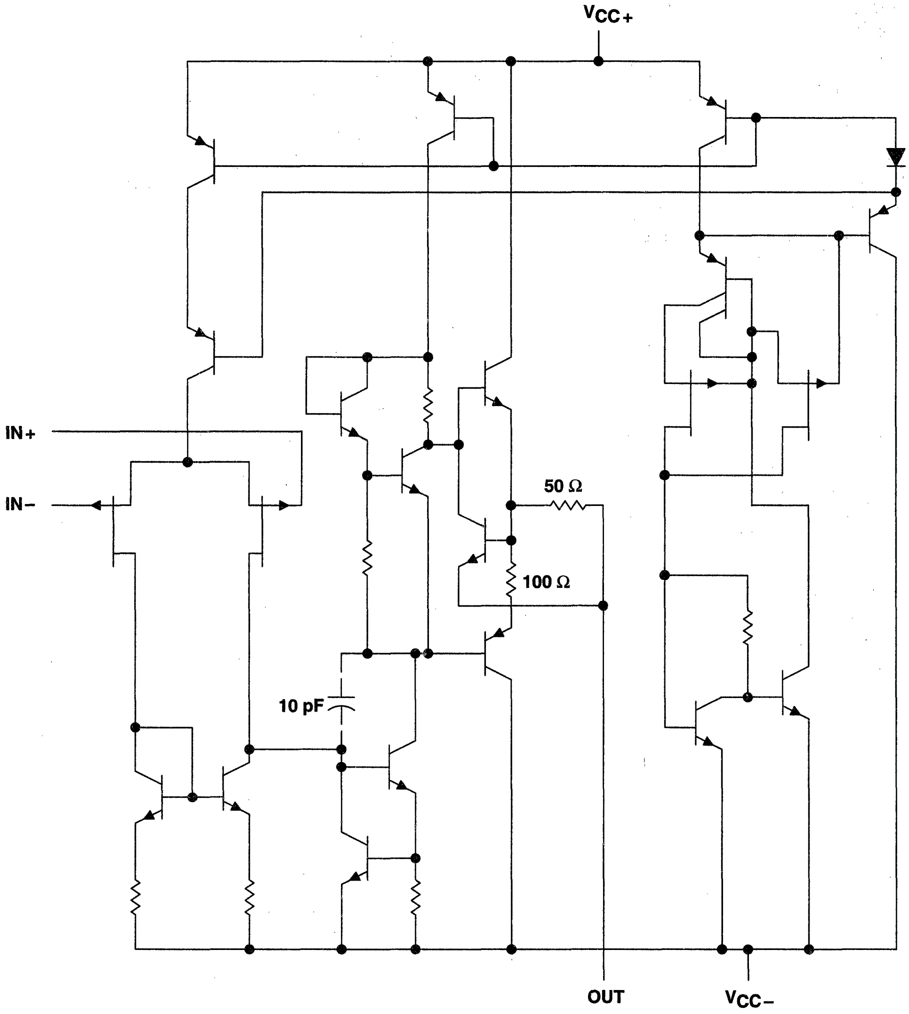


AVAILABLE OPTION

T_A	V_{IO}max AT 25°C	PACKAGE
		SMALL OUTLINE (DB)†
0°C to 70°C	7 mV	TL064x2DBLE

† The DB package is only available left-end taped and reeled.

schematic (each amplifier)



All component values shown are nominal.

ACTUAL DEVICE COMPONENT COUNT	
Transistors	116
Resistors	60
JFET	24
Capacitors	8
Diodes	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	–18 V
Differential input voltage, V_{ID} (see Note 2)	±30 V
Input voltage, V_I (any input) (see Notes 1 and 3)	±15 V
Duration of output short circuit to ground (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages and V_{CC} specified for the measurement of I_{OS}, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN + with respect to IN –.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output can be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	1024 mW	8.2 mW/°C	655 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$	25°C		3	15	mV
				Full range			20	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$	Full range		10		μV/°C
I_{IO}	Input offset current	$V_O = 0$		25°C		5	200	pA
				Full range			5	nA
I_{IB}	Input bias current§	$V_O = 0$		25°C		30	400	pA
				Full range			10	nA
V_{ICR}	Common-mode input voltage range			25°C	±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$		25°C	±10	±13.5		V
		$R_L \geq 10\ k\Omega$		Full range	±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V,	$R_L \geq 10\ k\Omega$	25°C	3	6		V/mV
				Full range	3			
B_1	Unity-gain bandwidth	$R_L = 10\ k\Omega$,		25°C		1		MHz
r_1	Input resistance			25°C		10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $R_S = 50\ \Omega$	$V_O = 0$,	25°C	70	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ± 15 V, $R_S = 50\ \Omega$	$V_O = 0$,	25°C	70	95		dB
P_D	Total power dissipation (each amplifier)	$V_O = 0$,	No load	25°C		6	7.5	mW
I_{CC}	Supply current (each amplifier)	$V_O = 0$,	No load	25°C		200	250	μA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

‡ Full range is 0°C to 70°C.

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 13. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ mV, $C_L = 100$ pF,	$R_L = 10\ k\Omega$, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	$V_I = 20$ V, $C_L = 100$ pF,	$R_L = 10\ k\Omega$, See Figure 1		0.2		μs
	Overshoot factor				10%		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$,	f = 1 kHz		42		nV/√Hz

PARAMETER MEASUREMENT INFORMATION

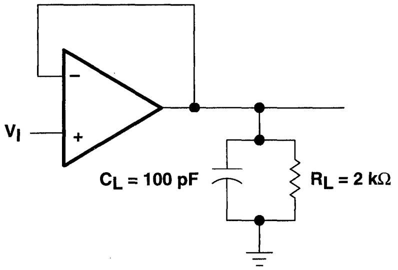


Figure 1. Unity-Gain Amplifier

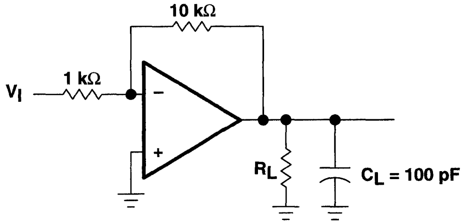


Figure 2. Gain-of-10 Inverting Amplifier

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OM}	Maximum peak output voltage	vs Supply voltage vs Free-air temperature vs Load resistance vs Frequency	3 4 5 6
A_{VD}	Differential voltage amplification	vs Free-air temperature	7
A_{VD}	Large-signal differential voltage amplification	vs Frequency	8
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	9 10
P_D	Total power dissipation	vs Free-air temperature	11
	Normalized unity-gain bandwidth	vs Free-air temperature	12
	Normalized slew rate	vs Free-air temperature	12
I_{IB}	Input bias current	vs Free-air temperature	13
	Pulse response	Large signal	14
V_O	Output voltage	vs Time	15
V_n	Equivalent input noise voltage	vs Frequency	16
	Normalized phase shift	vs Free-air temperature	12

TYPICAL CHARACTERISTICS

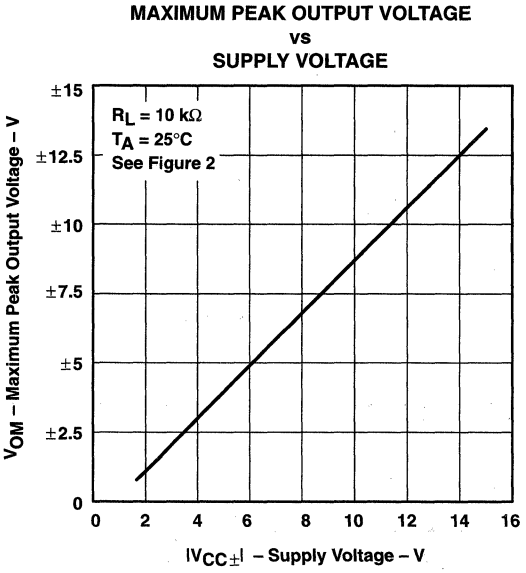


Figure 3

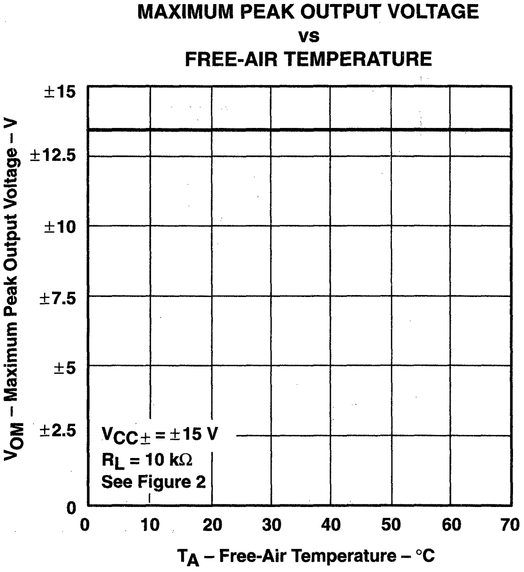


Figure 4

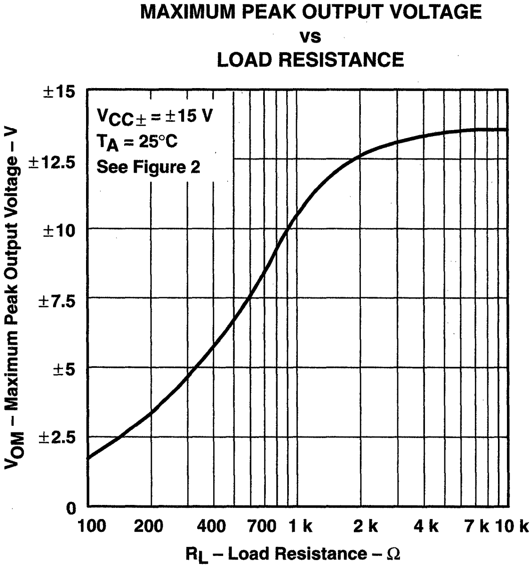


Figure 5

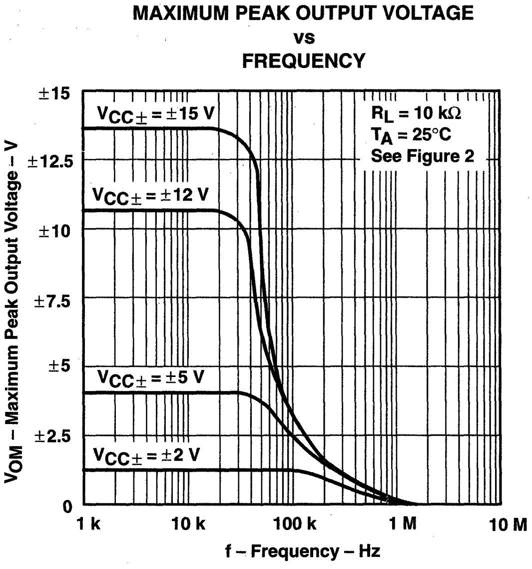


Figure 6

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

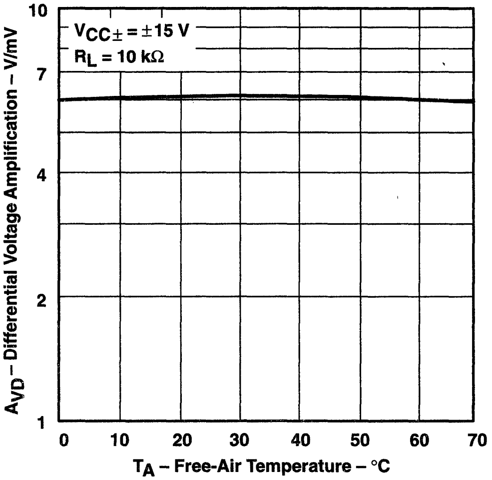


Figure 7

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

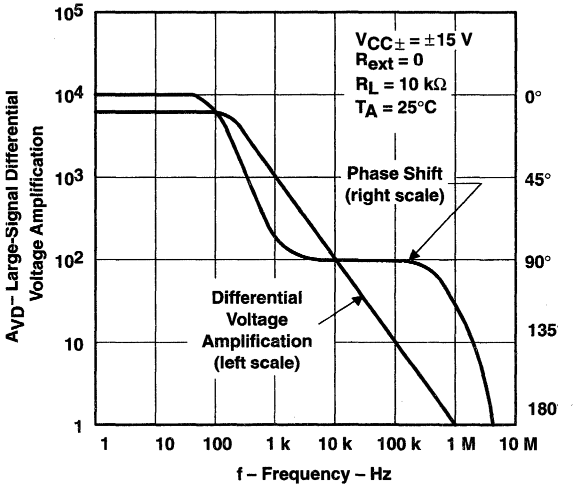


Figure 8

SUPPLY CURRENT vs SUPPLY VOLTAGE

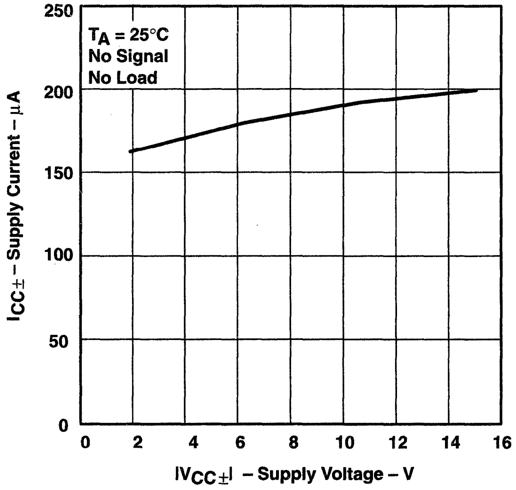


Figure 9

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

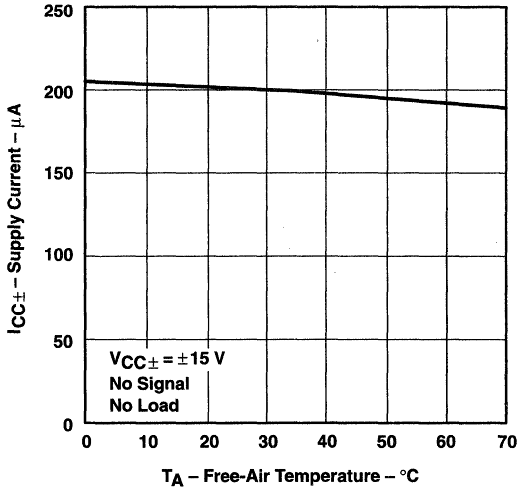


Figure 10

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

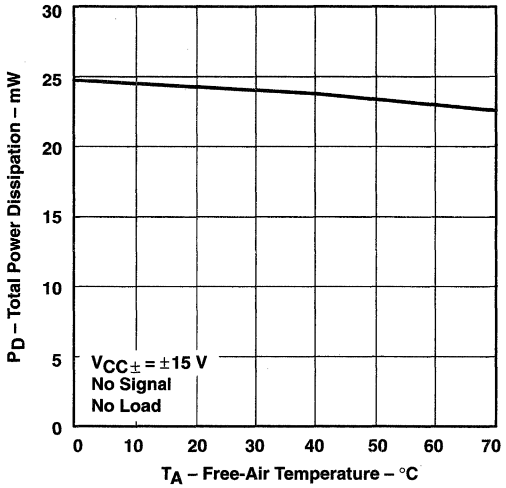


Figure 11

NORMALIZED UNITY-GAIN BANDWIDTH,
NORMALIZED SLEW RATE, AND
NORMALIZED PHASE SHIFT
vs
FREE-AIR TEMPERATURE

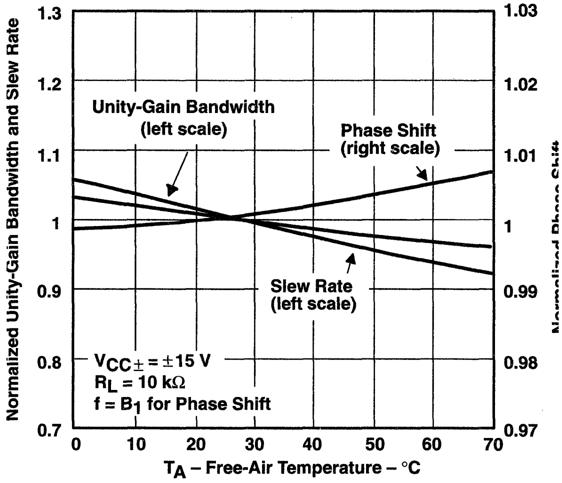


Figure 12

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

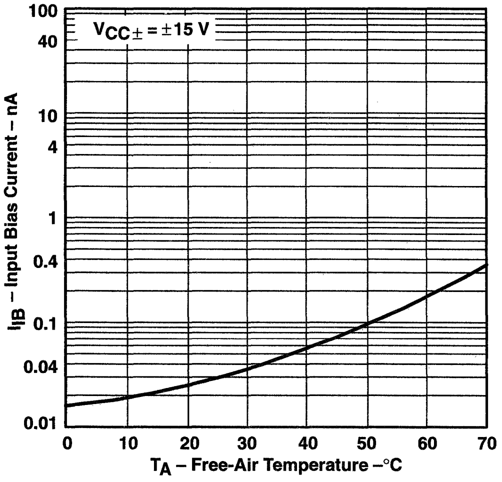


Figure 13

VOLTAGE FOLLOWER
LARGE SIGNAL PULSE RESPONSE

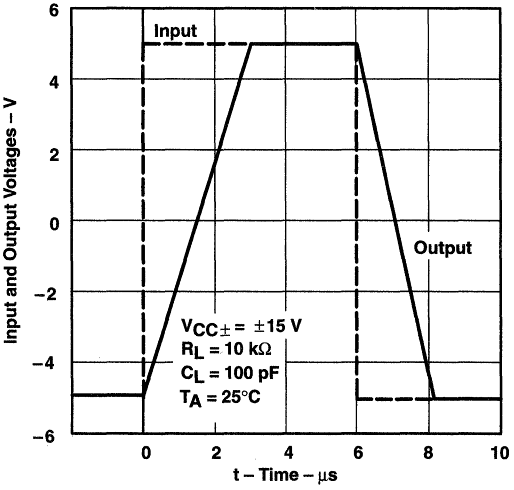


Figure 14

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
TIME

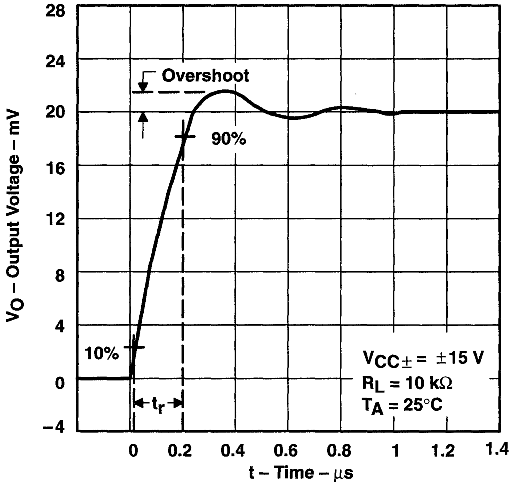


Figure 15

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

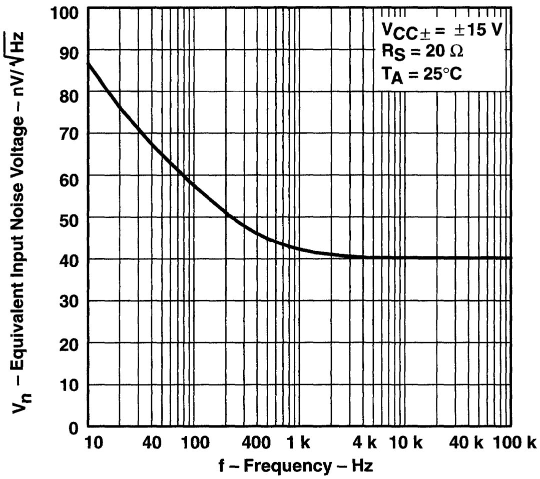


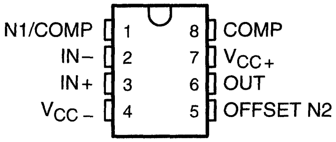
Figure 16

TL070
JFET-INPUT
OPERATIONAL AMPLIFIER

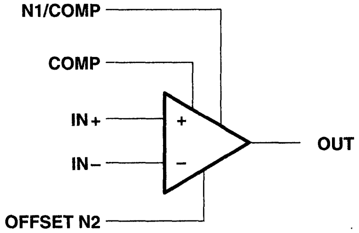
SLOS121A – NOVEMBER 1993 – REVISED AUGUST 1994

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion 0.003% Typ**
- **Low Noise $V_n = 18\ nV/\sqrt{Hz}$ Typ at f = 1 kHz**
- **High Input Impedance . . . JFET Input Stage**
- **Common-Mode Input Voltage Range Includes V_{CC+}**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**

D, P, OR PW PACKAGE
(TOP VIEW)



symbol



description

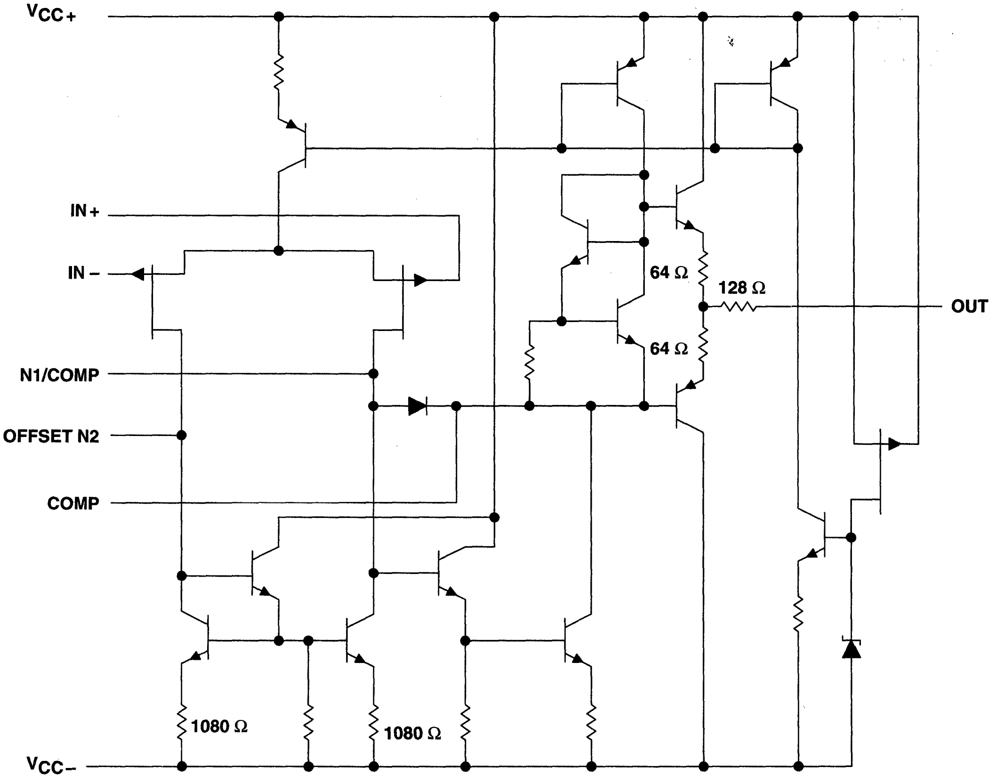
The JFET-input TL070 operational amplifier is designed as the lower-noise version of the TL080 amplifier with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL070 ideally suited for high-fidelity and audio preamplifier applications. This amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The TL070C device is characterized for operation from 0°C to 70°C. The TL070I device is characterized for operation from –40°C to 85°C. The TL070M device is characterized for operation from –55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE		
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)
0°C to 70°C	10 mV	TL070CD	TL070CP	TL070CPW
–40°C to 85°C	10 mV	TL070ID	TL070IP	—
–55°C to 125°C	10 mV	TL070MD	TL070MP	—

schematic



All component values shown are nominal.

COMPONENT COUNT†	
Transistors	13
Diodes	2
Resistors	10
epi-FET	1
JFET	2

† Includes all bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID} (see Note 2)	±30 V
Input voltage, V_I (see Notes 1 and 3)	±15 V
Duration of short-circuit current (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	145 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	70°C	336 mW	N/A	N/A

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL070C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	10	mV
			Full range			13	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18		µV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100	pA
			Full range			10	nA
I_{IB}	Input bias current‡	$V_O = 0$	25°C		65	200	pA
			Full range			7	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		V
V_{OM}	Maimum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		V
		$R_L \geq 10\ k\Omega$	Full range	±12			
		$R_L \geq 2\ k\Omega$		±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25°C	25	200		V/mV
			Full range	15			
B_1	Unity-gain bandwidth		25°C		3		MHz
r_i	Input resistance		25°C		10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	100		dB
I_{CC}	Supply current	$V_O = 0$, No load	25°C		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is 0°C to 70°C.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 5. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL070I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	10	mV
			Full range			13	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18		μV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100	pA
			Full range			10	nA
I_{IB}	Input bias current‡	$V_O = 0$	25°C		65	200	pA
			Full range			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		V
		$R_L \geq 10\ k\Omega$	Full range	±12			
		$R_L \geq 2\ k\Omega$		±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25°C	25	200		V/mV
			Full range	15			
B_1	Unity-gain bandwidth		25°C		3		MHz
r_i	Input resistance		25°C		10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	100		dB
I_{CC}	Supply current	$V_O = 0$, No load	25°C		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 5. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL070M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	10	mV
			Full range			13	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18		µV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100	pA
			Full range			20	nA
I_{IB}	Input bias current‡	$V_O = 0$	25°C		65	200	pA
			Full range			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		V
		$R_L \geq 10\ k\Omega$	Full range	±12			
		$R_L \geq 2\ k\Omega$		±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25°C	25	200		V/mV
			Full range	15			
B_1	Unity-gain bandwidth		25°C		3		MHz
r_i	Input resistance		25°C		10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	100		dB
I_{CC}	Supply current	$V_O = 0$, No load	25°C		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120		dB

---

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −55°C to 125°C.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 5. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2\ k\Omega$, See Figure 1	8	13		V/µs
t_r	Rise time overshoot factor	$V_I = 20$ mV, $C_L = 100$ pF,	$R_L = 2\ k\Omega$, See Figure 1		0.1		µs
					20		%
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		µV
I_n	Equivalent input noise current	$R_S = 20\ \Omega$,	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(rms)} = 10$ V, $R_L \geq 2\ k\Omega$,	$R_S \leq 1\ k\Omega$, f = 1 kHz		0.003		%

PARAMETER MEASUREMENT INFORMATION

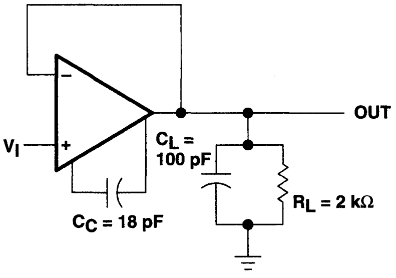


Figure 1. Unity-Gain Amplifier

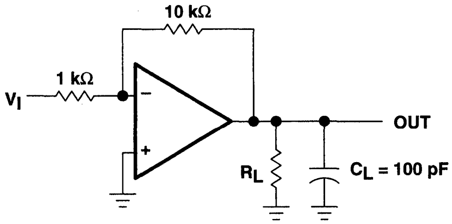


Figure 2. Gain-of-10 Inverting Amplifier

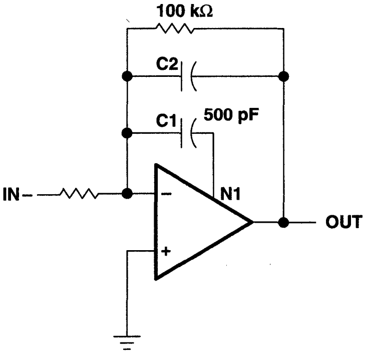


Figure 3. Feed-Forward Compensation

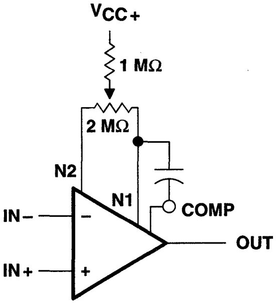


Figure 4. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	5
V_{OM}	Maximum output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	6, 7, 8 9 10 11
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	12 14
A_{VD}	Differential voltage amplification	vs Frequency	13
	Phase shift	vs Frequency	14
	Normalized unity-gain bandwidth	vs Free-air temperature	15
	Normalized phase shift	vs Free-air temperature	15
CMRR	Common-mode rejection ratio	vs Free-air temperature	16
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	17 18
P_D	Total power dissipation	vs Free-air temperature	19
	Normalized slew rate	vs Free-air temperature	20
V_n	Equivalent input noise voltage	vs Frequency	21
THD	Total harmonic distortion	vs Frequency	22
	Large-signal pulse response	vs Time	23
V_O	Output voltage	vs Elapsed time	24

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

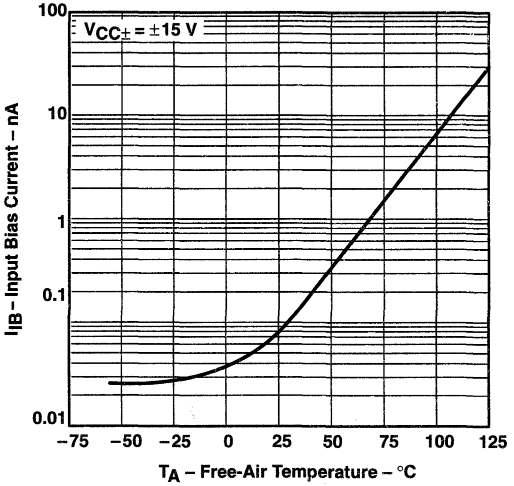


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

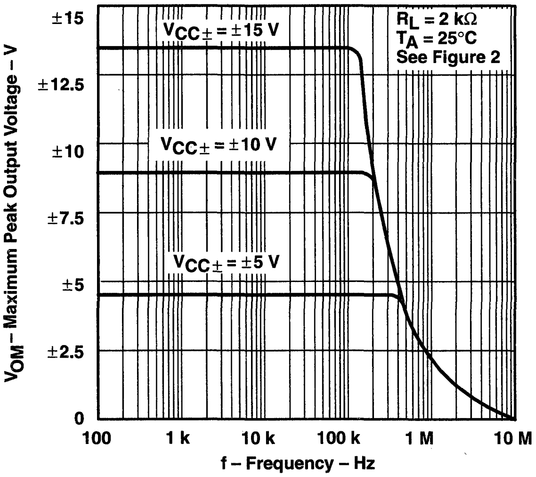


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

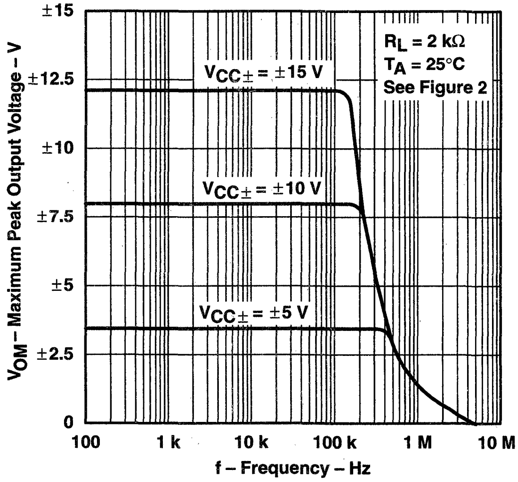


Figure 7

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

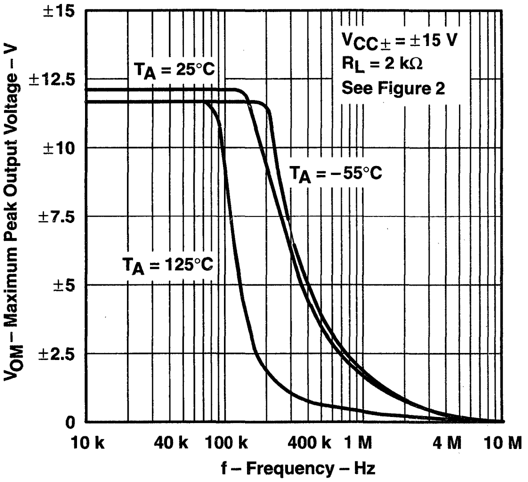


Figure 8

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

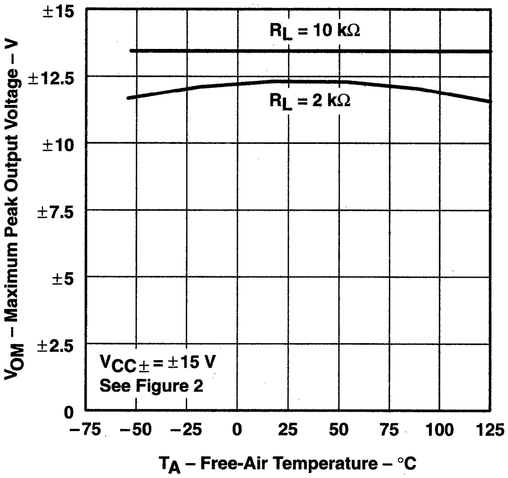

Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

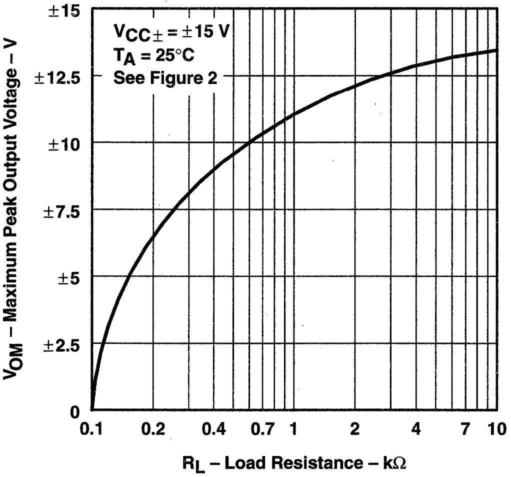

Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

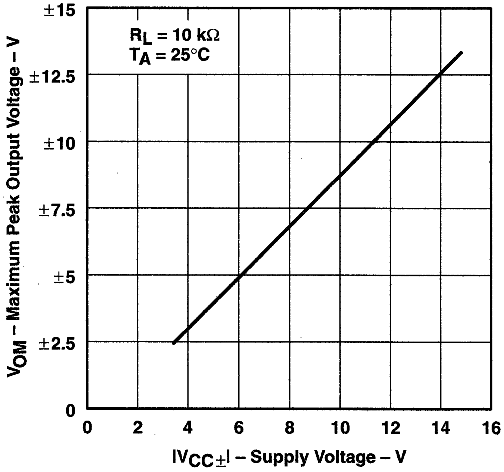

Figure 11

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VS FREE-AIR TEMPERATURE

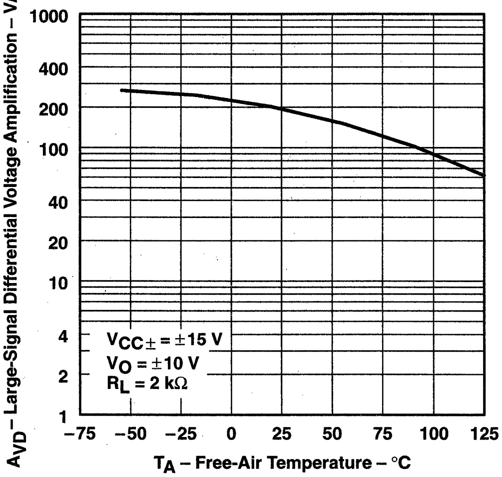

Figure 12

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY WITH FEED-FORWARD COMPENSATION

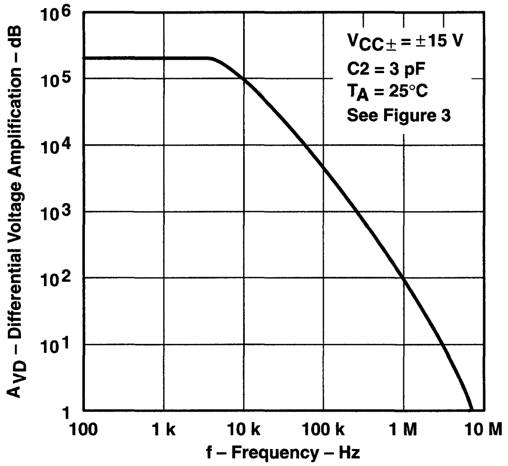

Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

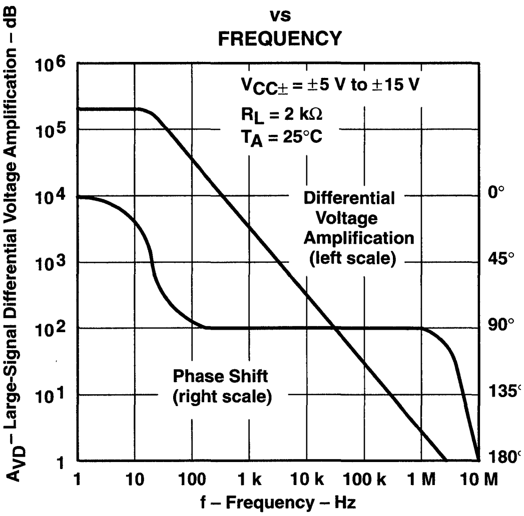

Figure 14

NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREE-AIR TEMPERATURE

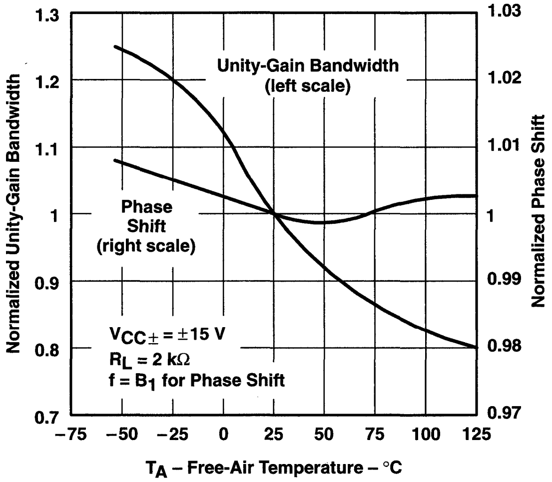

Figure 15

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

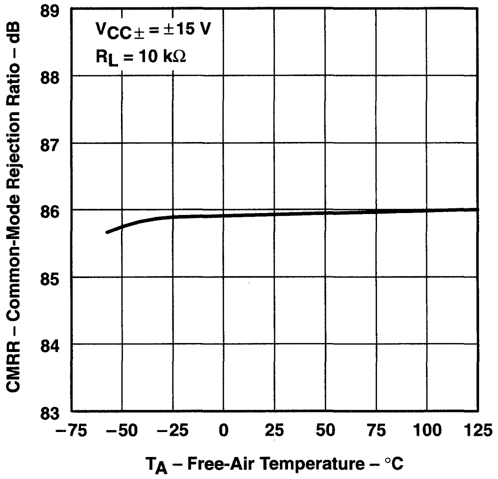

Figure 16

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

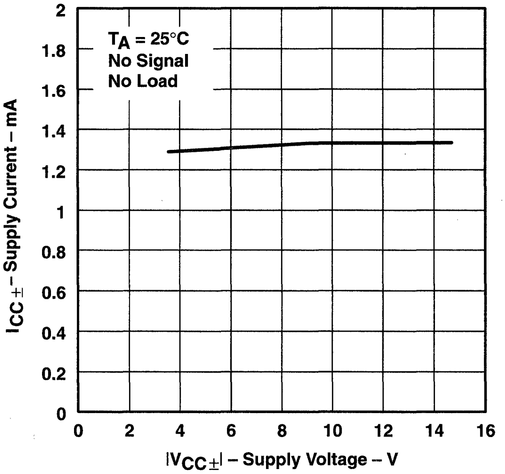

Figure 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

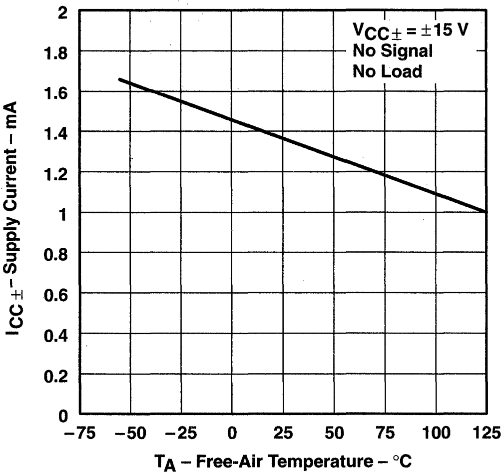

Figure 18

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

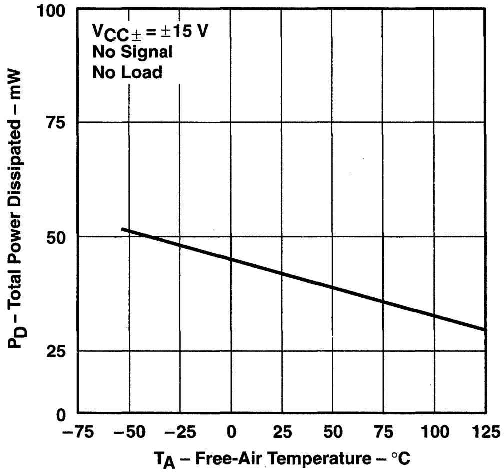

Figure 19

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

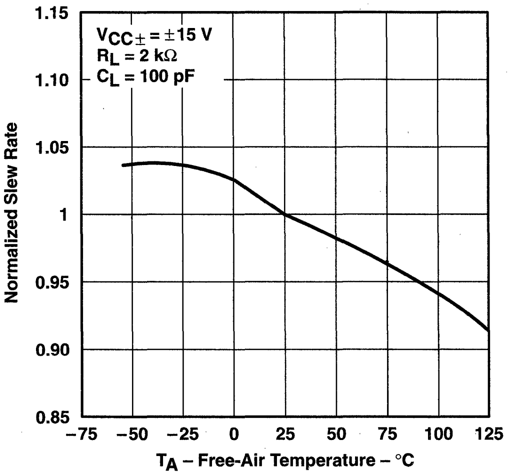

Figure 20

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used.

TYPICAL CHARACTERISTICS

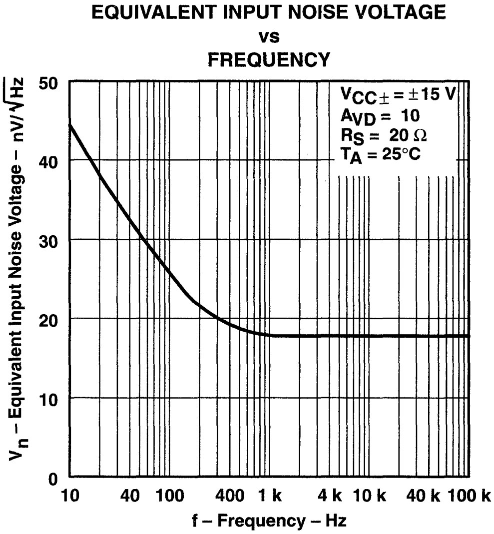


Figure 21

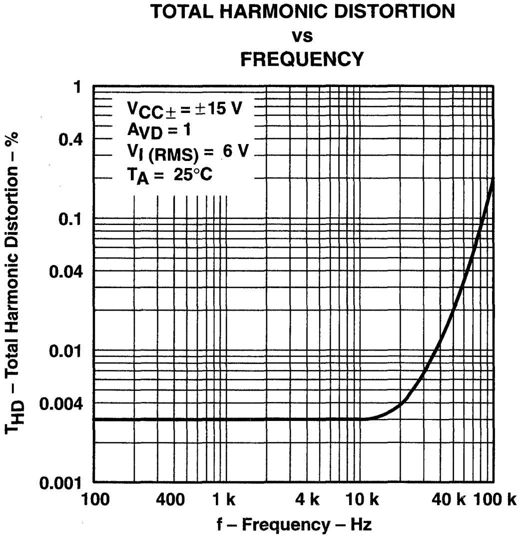


Figure 22

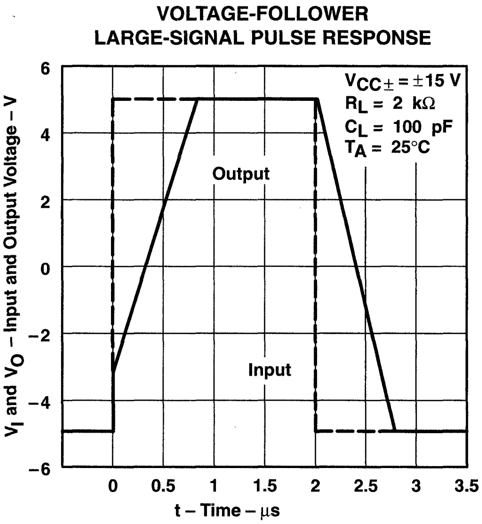


Figure 23

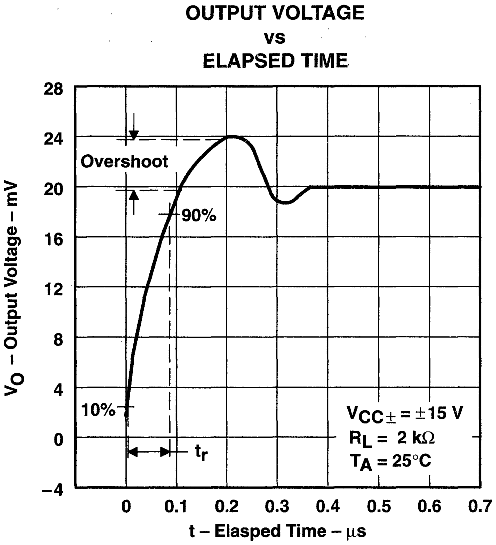


Figure 24

APPLICATION INFORMATION

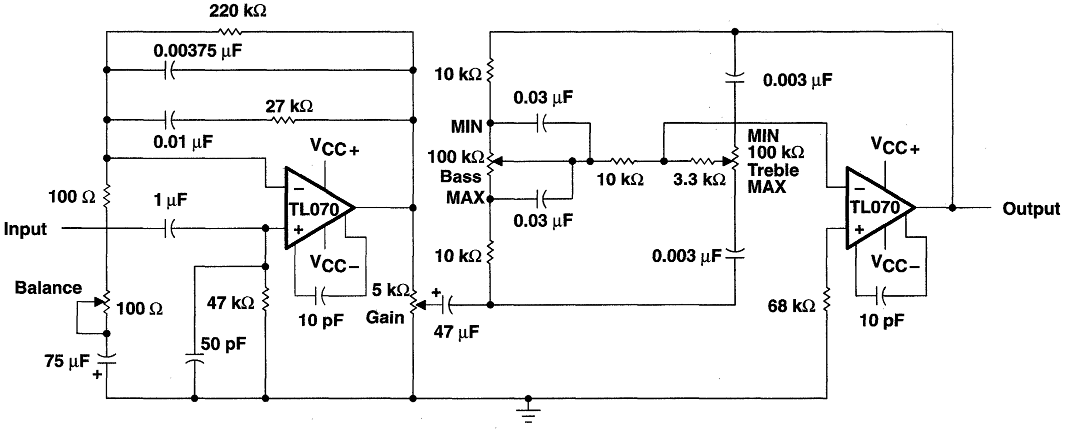


Figure 25. IC Preamplifier

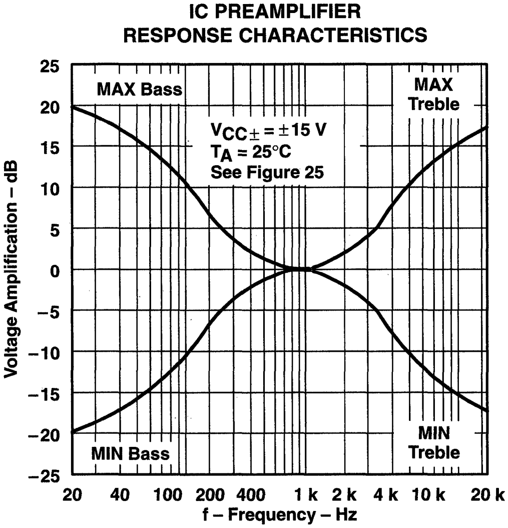


Figure 26

TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080D – SEPTEMBER 1978 – REVISED AUGUST 1996

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion 0.003% Typ**
- **Low Noise V_n = 18 nV/$\sqrt{\text{Hz}}$ Typ at f = 1 kHz**
- **High Input Impedance . . . JFET Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

description

The JFET-input operational amplifiers in the TL07_ series are designed as low-noise versions of the TL08_ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07_ series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

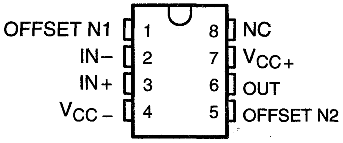
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

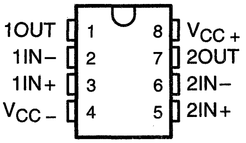
T_A	V_{IO}max AT 25°C	PACKAGE							
		SMALL OUTLINE (D)†	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP PACKAGE (PW)	FLAT PACKAGE (W)
0°C to 70°C	10 mV 6 mV 3 mV	TL071CD TL071ACD TL071BCD	—	—	—	—	TL071CP TL071ACP TL071BCP	TL071CPWLE — —	—
	10 mV 6 mV 3 mV	TL072CD TL072ACD TL072BCD	—	—	—	—	TL072CP TL072ACP TL072BCP	TL072CPWLE — —	—
	10 mV 6 mV 3 mV	TL074CD TL074ACD TL074BCD	—	—	—	TL074CN TL074ACN TL074BCN	—	TL074CPWLE — —	—
−40°C to 85°C	6 mV	TL071ID TL072ID TL074ID	—	—	—	— — TL074IN	TL071IP TL072IP —	—	—
−55°C to 125°C	6 mV 6 mV 9 mV	—	TL071MFK TL072MFK TL074MFK	— — TL074MJ	TL071MJG TL072MJG —	— — TL074MN	— TL072MP —	—	— — TL074MW

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR). The PW package is only available left-ended taped and reeled (e.g., TL072CPWLE).

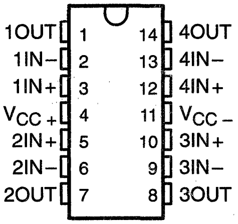
TL071, TL071A, TL071B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



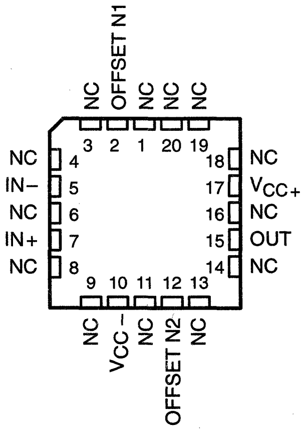
TL072, TL072A, TL072B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



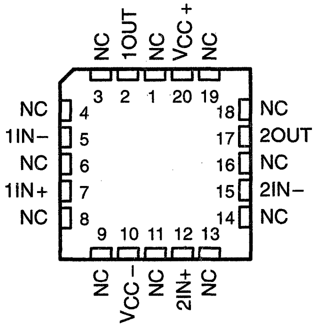
TL074, TL074A, TL074B
D, J, N, OR PW PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)



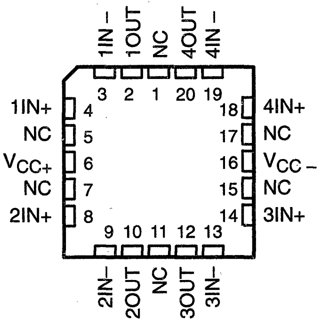
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



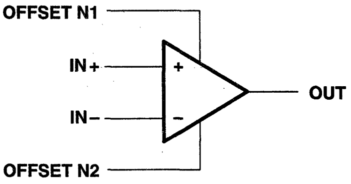
TL074
FK PACKAGE
(TOP VIEW)



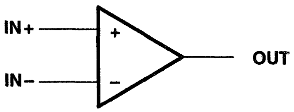
NC – No internal connection

symbols

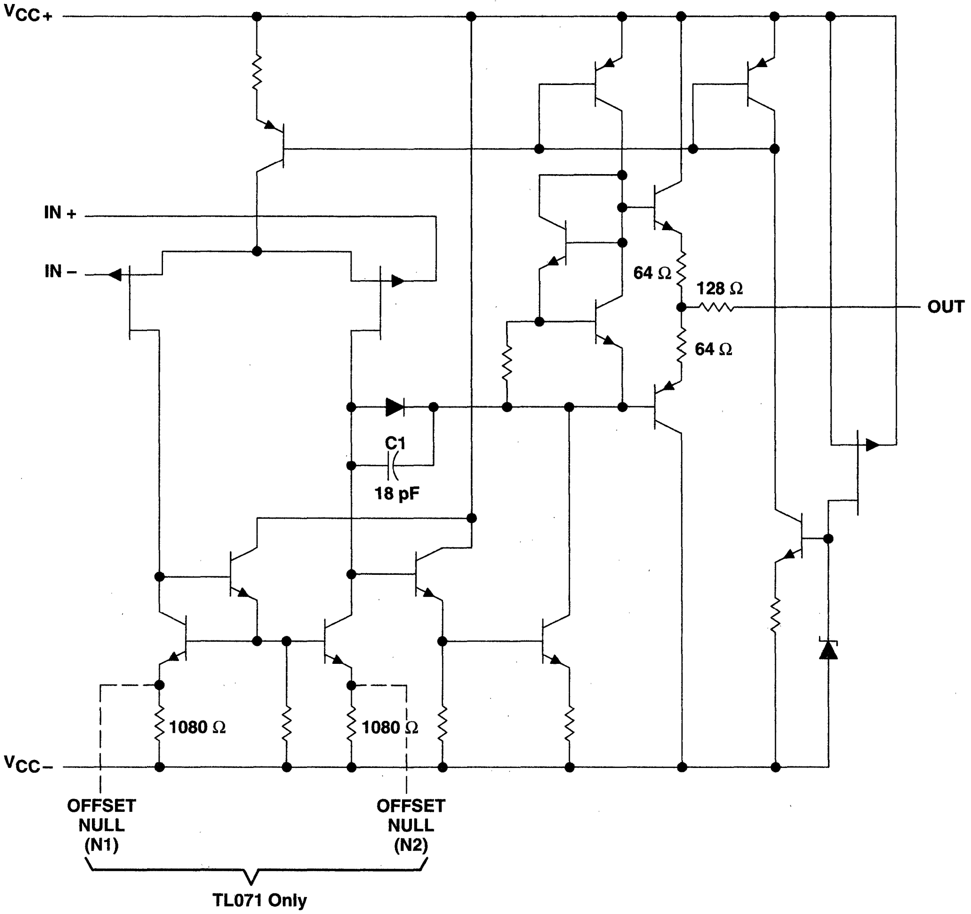
TL071



TL072 (each amplifier)
TL074 (each amplifier)



schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	−18 V
Differential input voltage, V_{ID} (see Note 2)	±30 V
Input voltage, V_I (see Notes 1 and 3)	±15 V
Duration of output short circuit (see Note 4)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, or PW package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	33°C	465 mW	378 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	70°C	525 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	70°C	700 mW	N/A	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	10		3	6		2	3		3	6	mV
			Full range			13			7.5			5			8	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100		5	100		5	100	pA
			Full range			10			2			2			2	nA
I_{IB}	Input bias current§	V_O = 0	25°C		65	200		65	200		65	200		65	200	pA
			Full range			7			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			25			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω	25°C	70	100		75	100		75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	70	100		80	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

‡ Full range is T_A = 0°C to 70°C for TL07_C,TL07_AC, TL07_BC and is T_A = −40°C to 85°C for TL07_I.

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18			18		μV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current‡	$V_O = 0$	25°C		65	200		65	200	pA
						50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		±12	±13.5		V
		$R_L \geq 10\ k\Omega$	Full range	±12			±12			
		$R_L \geq 2\ k\Omega$		±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range is $T_A = -55°C$ to 125°C.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07xM			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1	5	13		8	13		V/µs
t_r	Rise time overshoot factor	$V_I = 20$ mV, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1		0.1			0.1		µs
					20%			20%		
V_n	Equivalent input noise voltage	$R_S = 20$ Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		µV
I_n	Equivalent input noise current	$R_S = 20$ Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_{Irms} = 6$ V, $R_L \geq 2$ kΩ, f = 1 kHz	$A_{VD} = 1$, $R_S \leq 1$ kΩ,		0.003%			0.003%		

PARAMETER MEASUREMENT INFORMATION

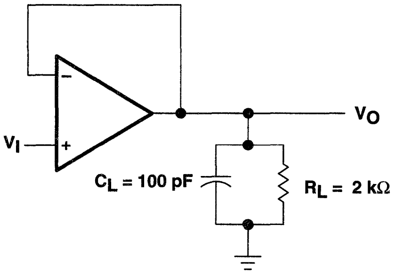


Figure 1. Unity-Gain Amplifier

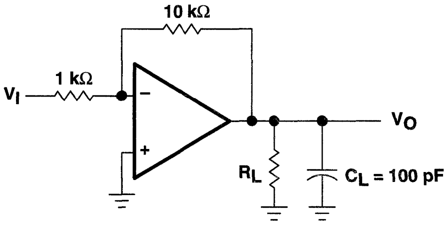


Figure 2. Gain-of-10 Inverting Amplifier

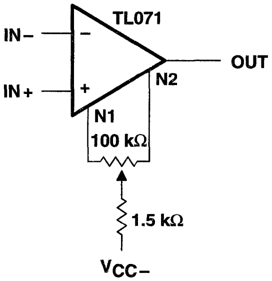


Figure 3. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	4
V_{OM}	Maximum output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
CMRR	Common-mode rejection ratio	vs Free-air temperature	14
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	15 16
P_D	Total power dissipation	vs Free-air temperature	17
	Normalized slew rate	vs Free-air temperature	18
V_n	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
	Large-signal pulse response	vs Time	21
V_O	Output voltage	vs Elapsed time	22

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

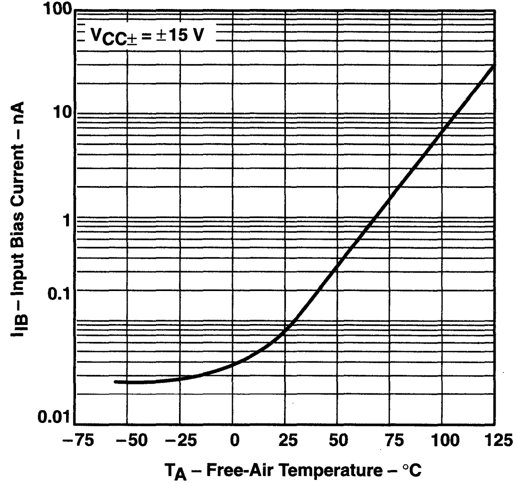


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

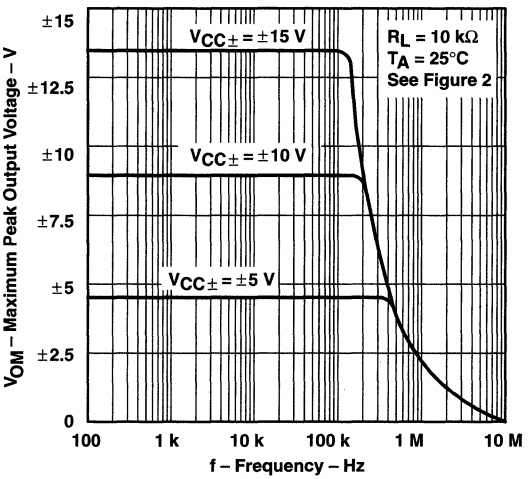


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

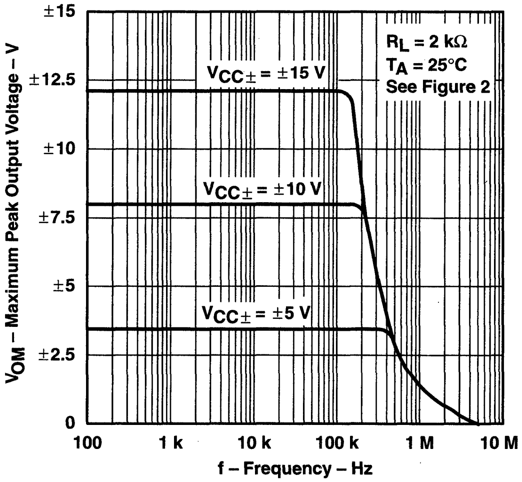


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

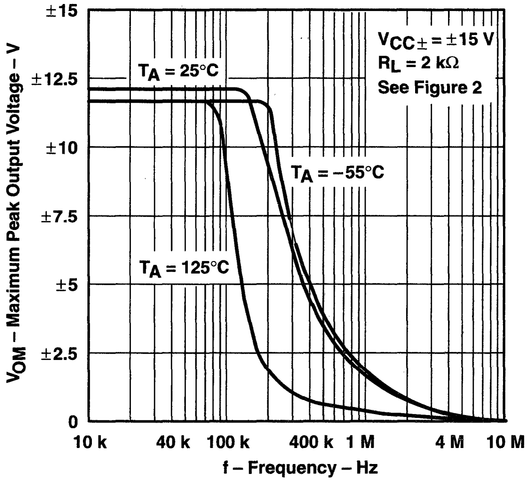


Figure 7

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

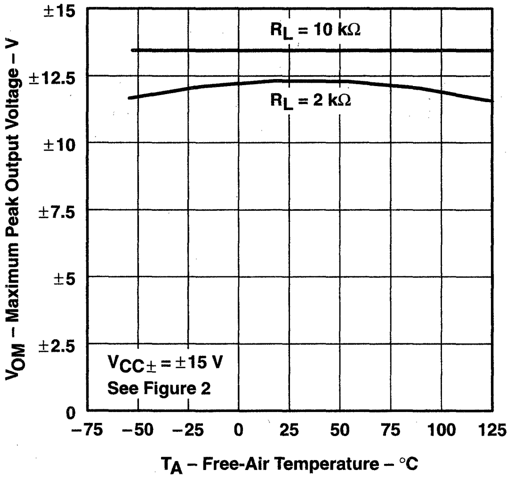

Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

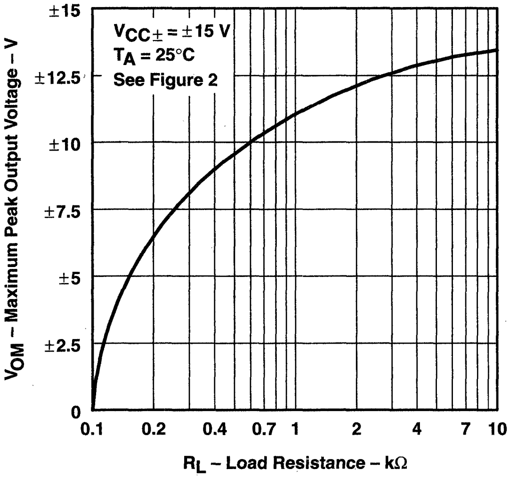

Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

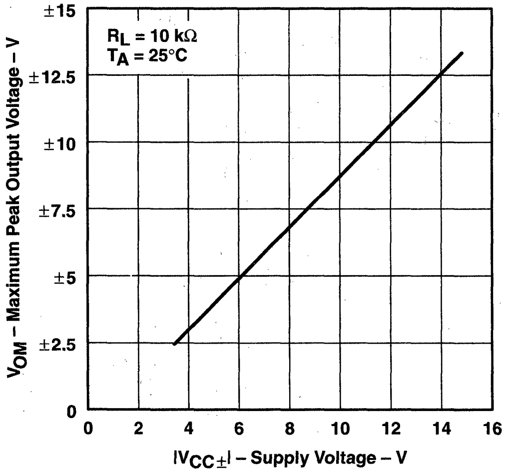

Figure 10

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

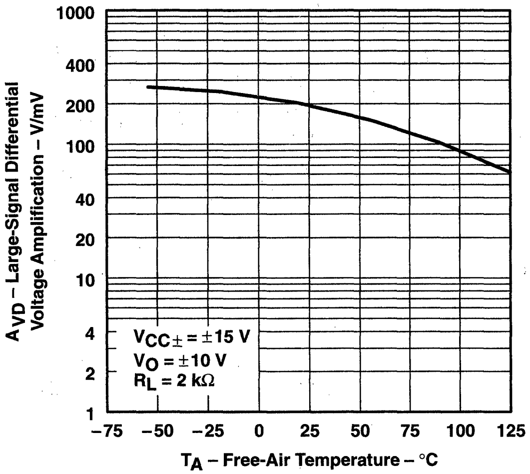

Figure 11

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

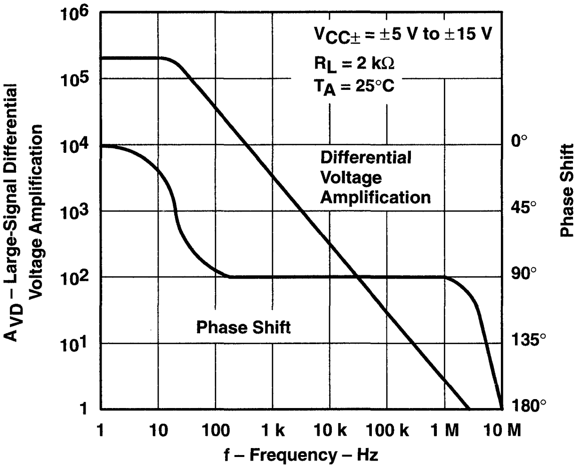

Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREQUENCY FREE-AIR TEMPERATURE

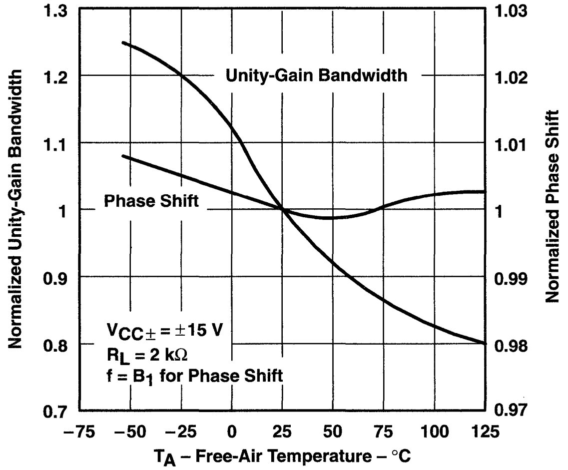

Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

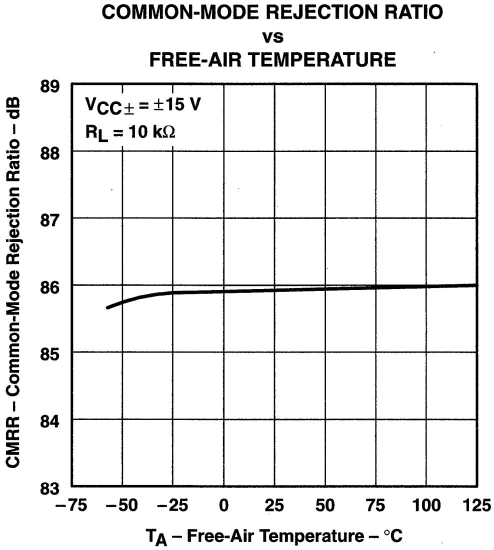

Figure 14

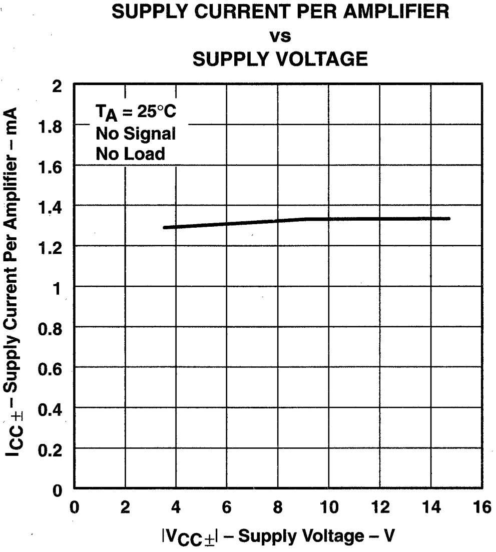

Figure 15

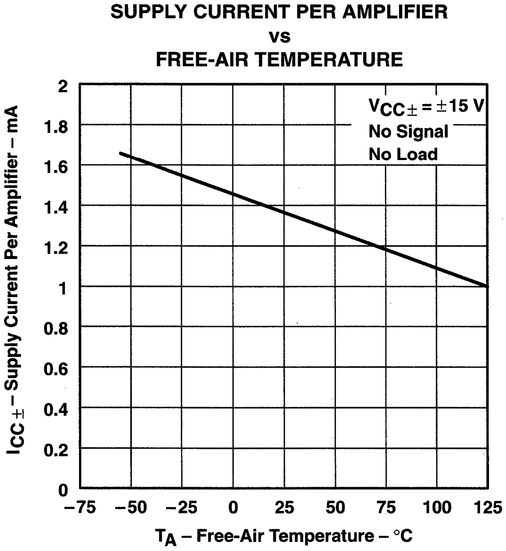

Figure 16

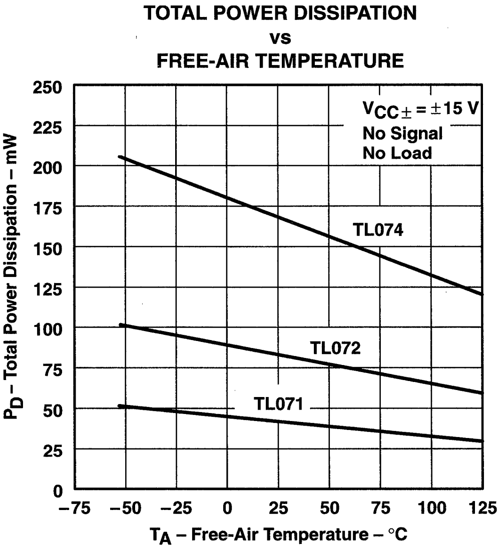

Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

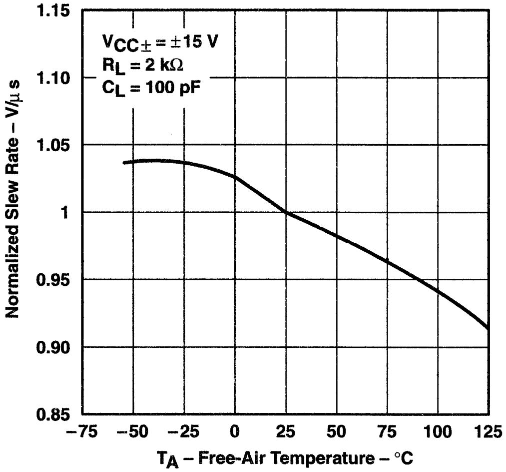

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 18

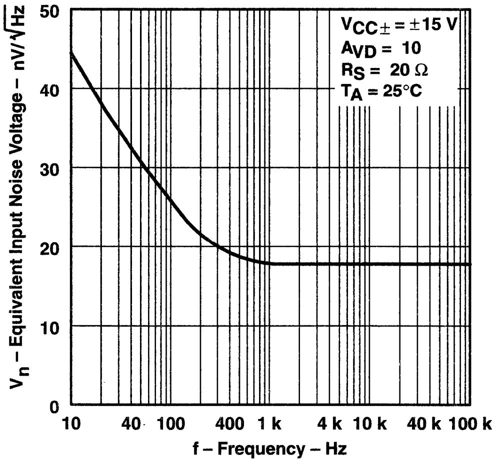

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 19

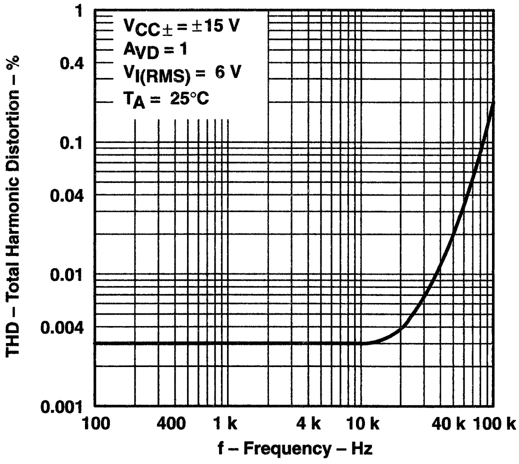

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

Figure 20

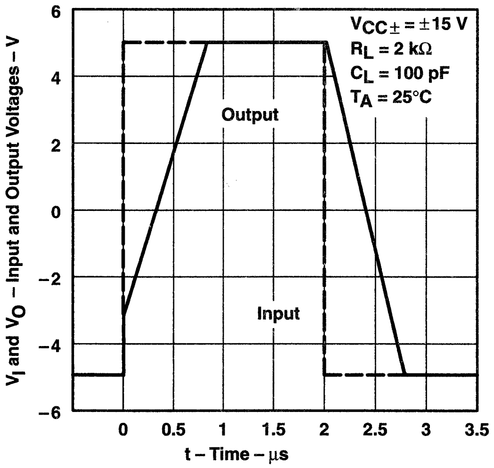

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

Figure 21

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ELAPSED TIME

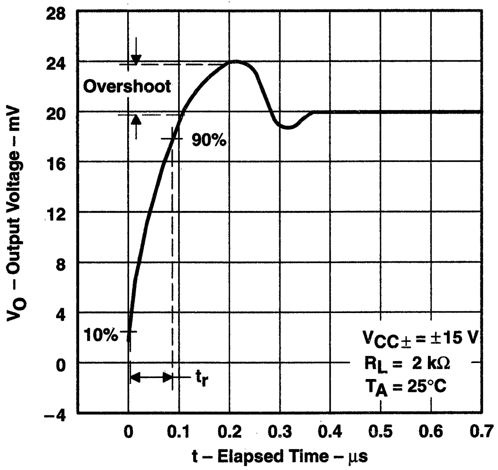
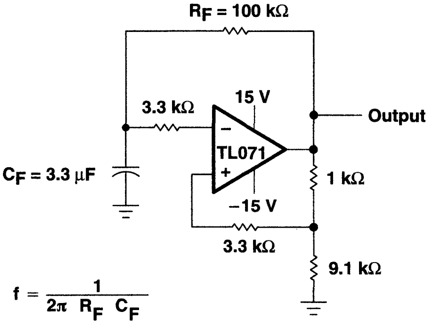


Figure 22

APPLICATION INFORMATION

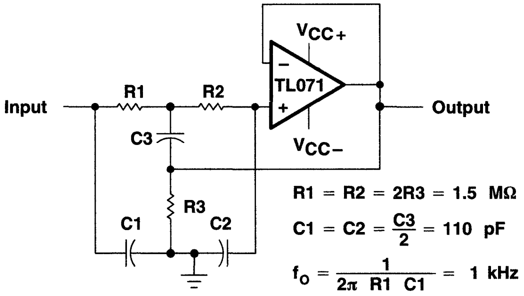
Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
0.5-Hz square-wave oscillator	TL071	23
High-Q notch filter	TL071	24
Audio-distribution amplifier	TL074	25
100-kHz quadrature oscillator	TL072	26
AC amplifier	TL071	27



$$f = \frac{1}{2\pi\ R_F\ C_F}$$

Figure 23. 0.5-Hz Square-Wave Oscillator



$$R1 = R2 = 2R3 = 1.5\ M\Omega$$

$$C1 = C2 = \frac{C3}{2} = 110\ pF$$

$$f_o = \frac{1}{2\pi\ R1\ C1} = 1\ kHz$$

Figure 24. High-Q Notch Filter

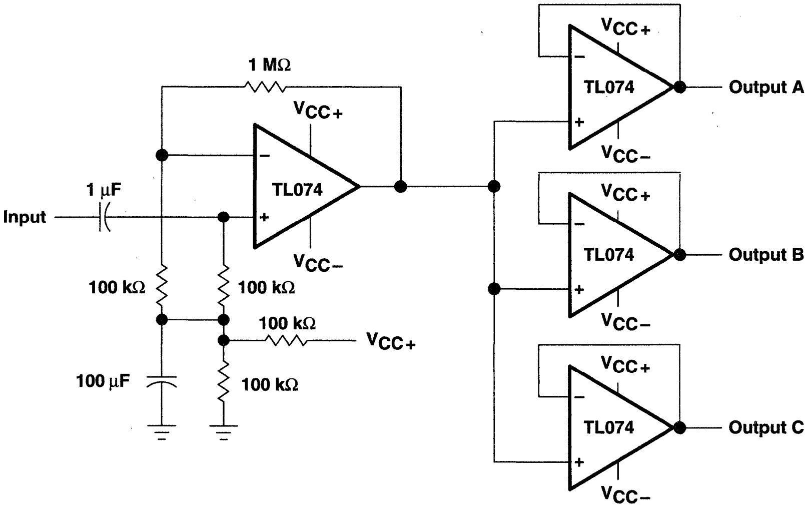
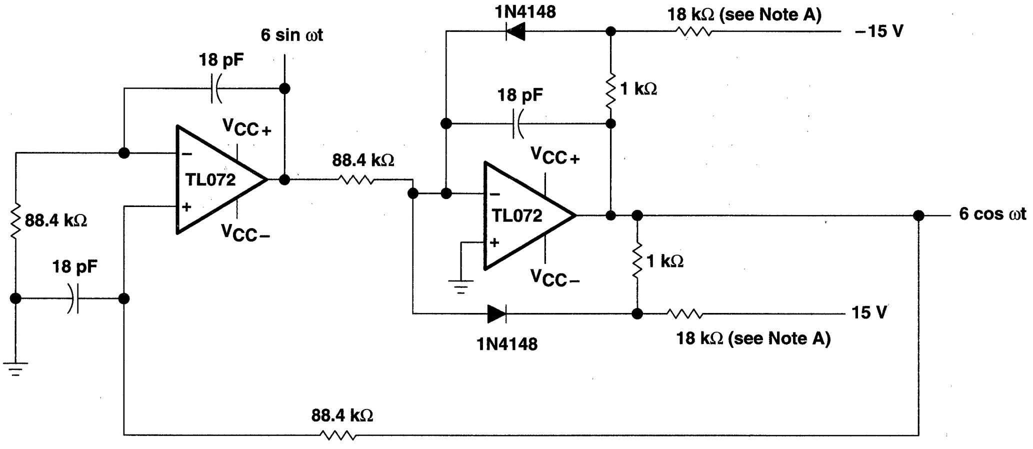


Figure 25. Audio-Distribution Amplifier

APPLICATION INFORMATION



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-kHz Quadrature Oscillator

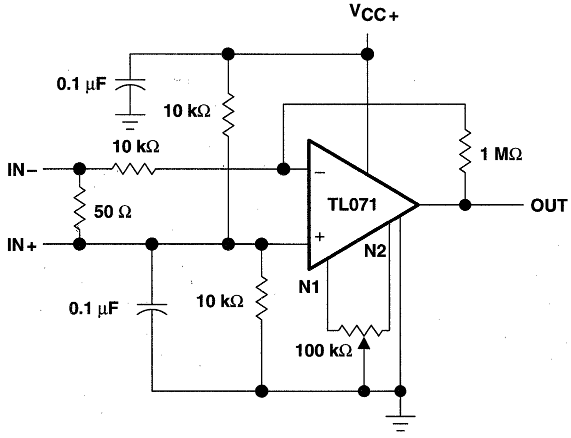


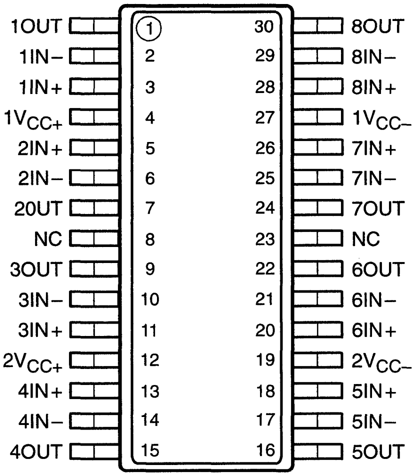
Figure 27. AC Amplifier

TL074x2
JFET-INPUT
OCTAL OPERATIONAL AMPLIFIER

SLOS135 – APRIL 1994

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion 0.003% Typ**
- **Low Noise $V_n = 18\ nV/\sqrt{Hz}$ Typ at f = 1 kHz**
- **High Input Impedance . . . JFET Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

DB PACKAGE
(TOP VIEW)



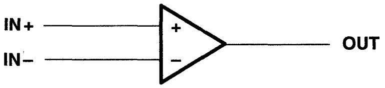
NC – No internal connection

description

The TL074x2 JFET-input operational amplifier is designed as a lower-noise version of the TL084x2 amplifier with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL074x2 ideally suited for high-fidelity and audio-preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The TL074x2 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)

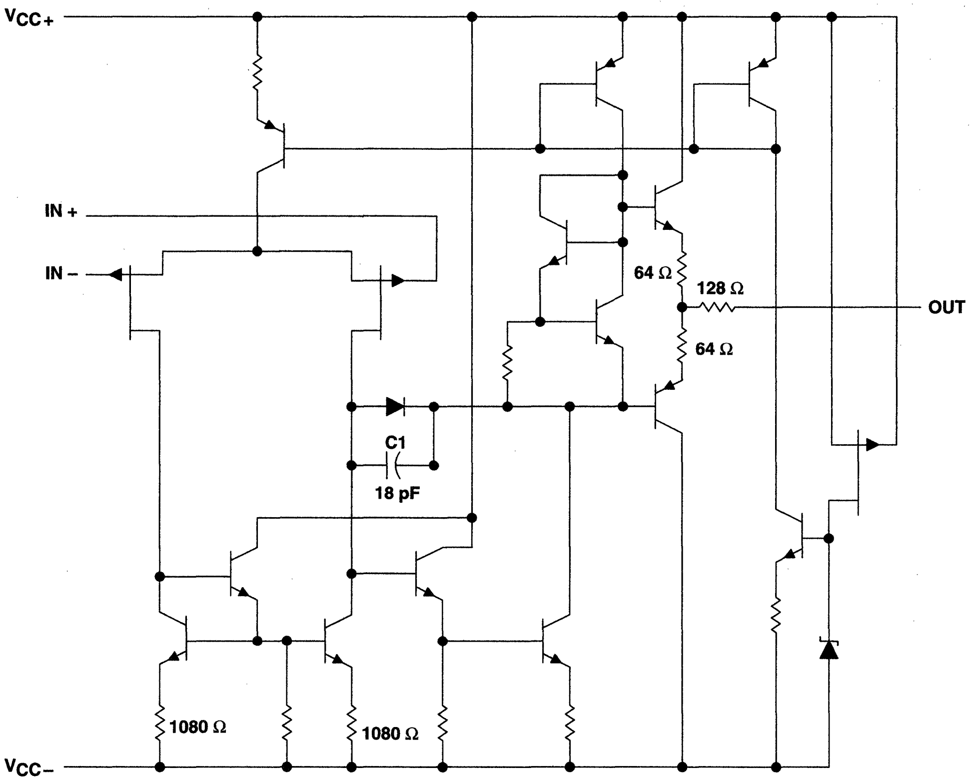


AVAILABLE OPTION

T_A	V_{IO}max AT 25°C	PACKAGE SMALL OUTLINE (DB)†
0°C to 70°C	10 mV	TL074x2DBLE

† The DB package is only available left-end taped and reeled.

schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†	
Resistors	88
Transistors	112
JFET	20
Diodes	12
Capacitors	8

† Includes bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	–18 V
Differential input voltage, V_{ID} (see Note 2)	±30 V
Input voltage range, V_I (see Notes 1 and 3)	±15 V
Duration of output short circuit (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output can be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	1024 mW	8.2 mW/°C	655 mW

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = \Omega$, $R_S = 50\ \Omega$	25°C		3	10	mV
			Full range			13	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18		µV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100	pA
			Full range			10	nA
I_{IB}	Input bias current§	$V_O = 0$	25°C		65	200	pA
			Full range			7	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		V
		$R_L \geq 10\ k\Omega$	Full range	±12			
		$R_L \geq 2\ k\Omega$		±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25°C	25	200		V/mV
			Full range	15			
B_1	Unity-gain bandwidth		25°C		3		MHz
r_i	Input resistance		25°C		10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	100		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$, No load	25°C		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

‡ Full range is T_A = 0°C to 70°C.

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 2. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2\ k\Omega$, See Figure 1	8	13		V/µs
t_r	Overshoot factor rise time	$V_I = 20$ mV, $C_L = 100$ pF,	$R_L = 2\ k\Omega$, See Figure 1		0.1		µs
					20%		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		µV
I_n	Equivalent input noise current	$R_S = 20\ \Omega$,	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_{Orms} = 10$ V, $R_L \geq 2\ k\Omega$,	$R_S \leq 1\ k\Omega$, f = 1 kHz		0.003%		

PARAMETER MEASUREMENT INFORMATION

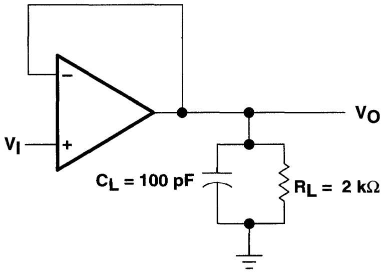


Figure 1. Unity-Gain Amplifier

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	2
V_{OM}	Maximum peak output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	3, 4, 5 6 7 8
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	9 10
	Normalized unity-gain bandwidth	vs Free-air temperature	11
CMRR	Common-mode rejection ratio	vs Free-air temperature	12
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	13 14
P_D	Total power dissipation	vs Free-air temperature	15
	Normalized slew rate	vs Free-air temperature	16
V_n	Equivalent input noise voltage	vs Frequency	17
THD	Total harmonic distortion	vs Frequency	18
	Pulse response	Large signal	19
V_O	Output voltage	vs Time	20
	Normalized phase shift	vs Free-air temperature	11

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

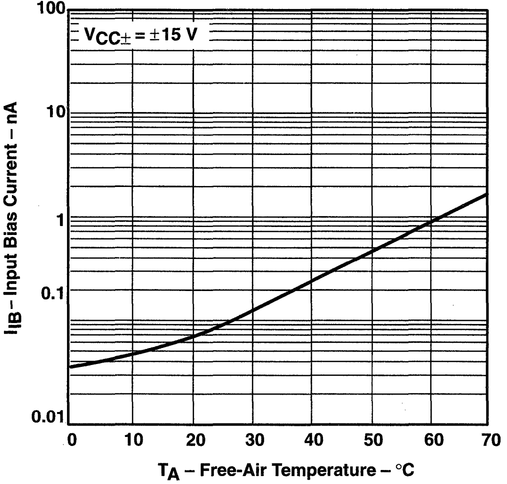


Figure 2

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

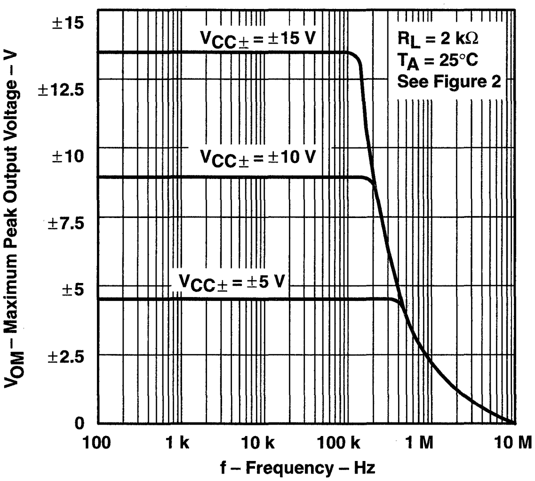


Figure 3

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

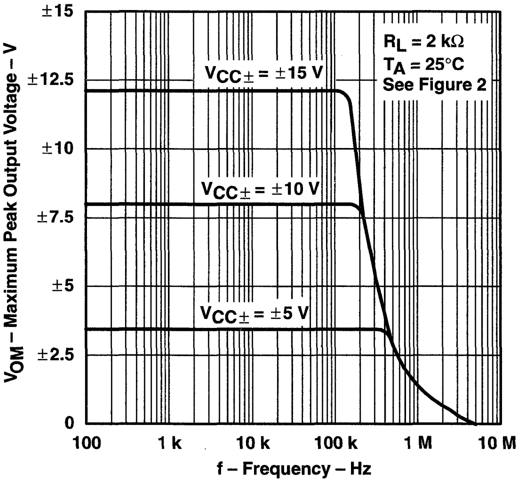


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

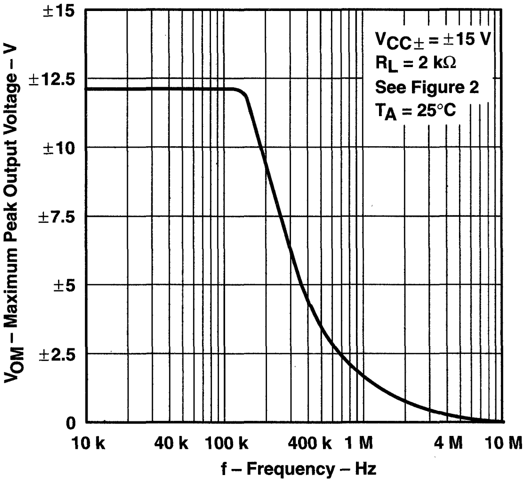


Figure 5

TYPICAL CHARACTERISTICS

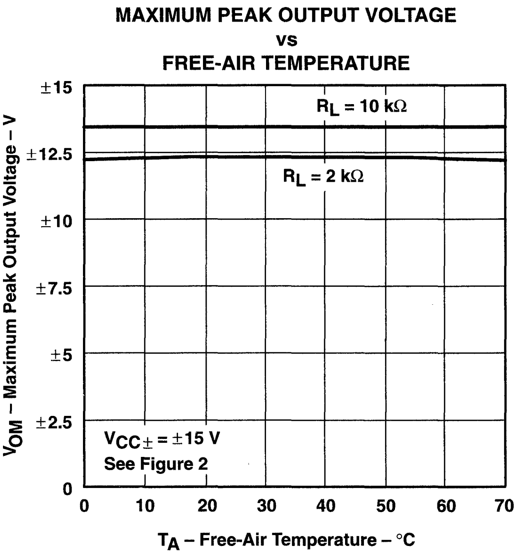


Figure 6

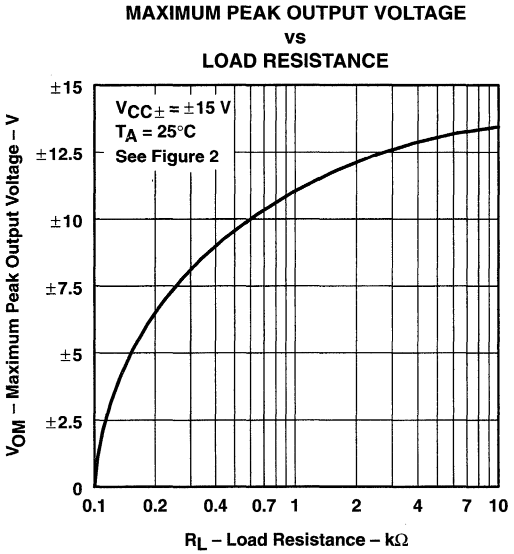


Figure 7

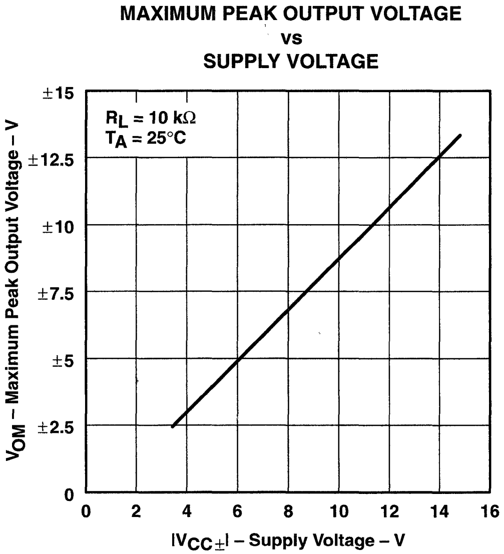


Figure 8

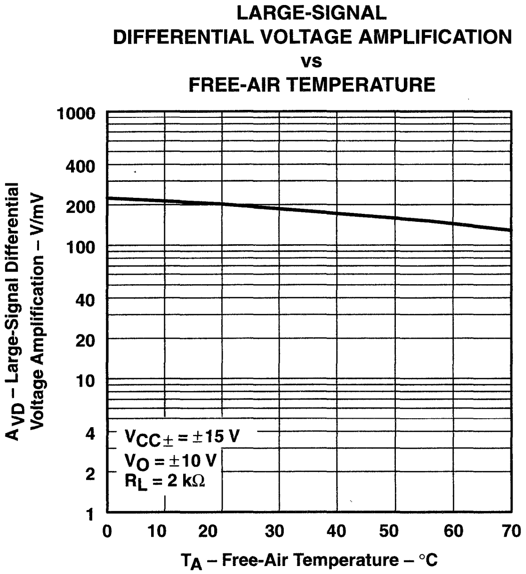


Figure 9

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

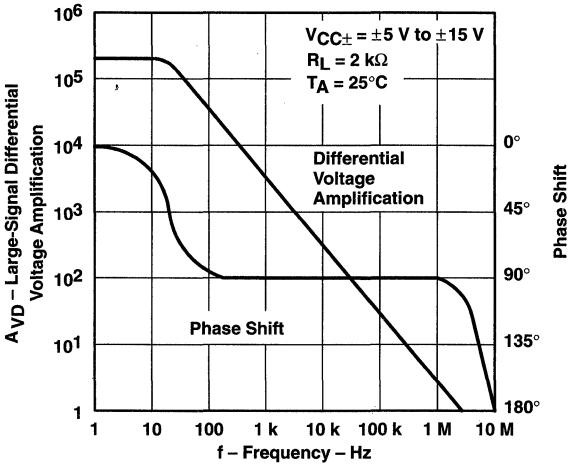


Figure 10

NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREE-AIR TEMPERATURE

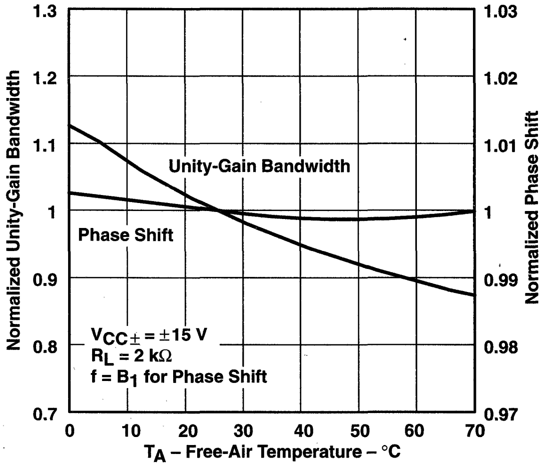


Figure 11

TYPICAL CHARACTERISTICS

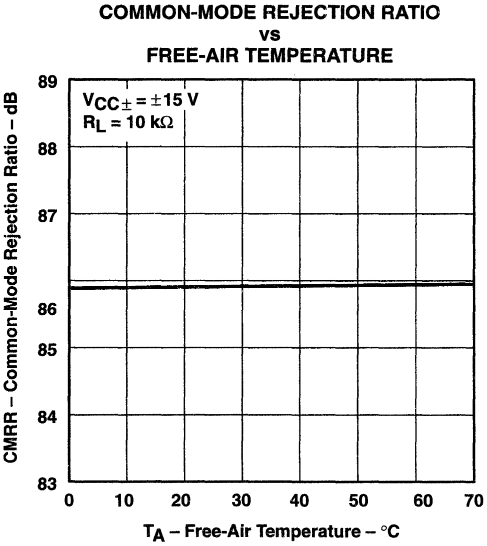


Figure 12

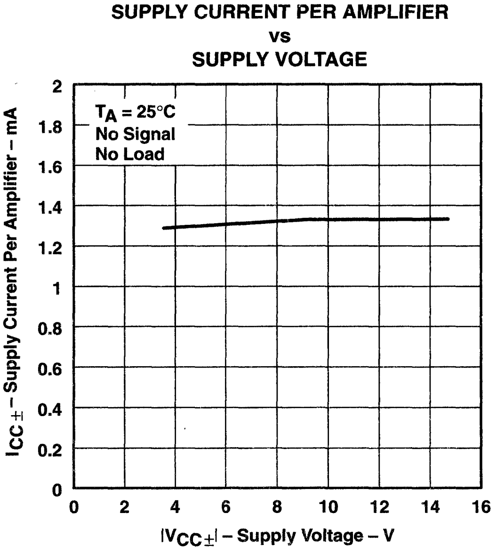


Figure 13

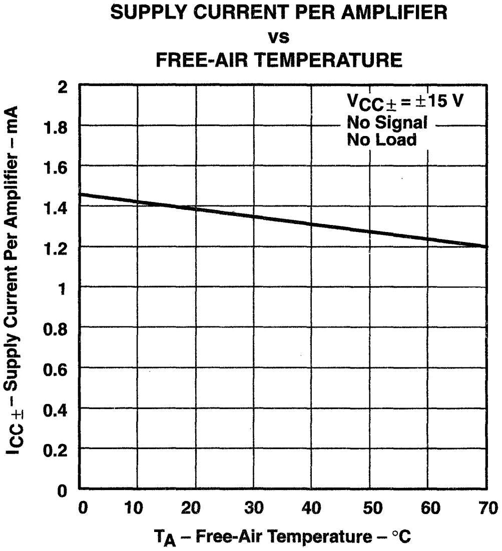


Figure 14

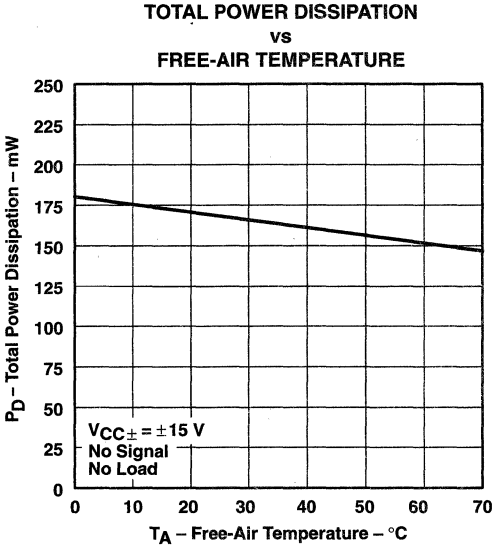


Figure 15

TYPICAL CHARACTERISTICS

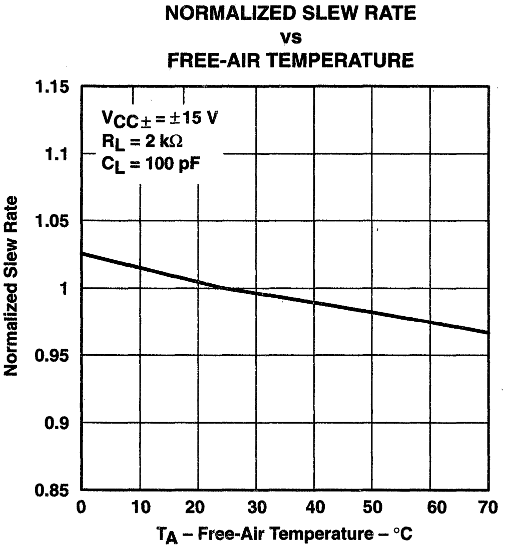


Figure 16

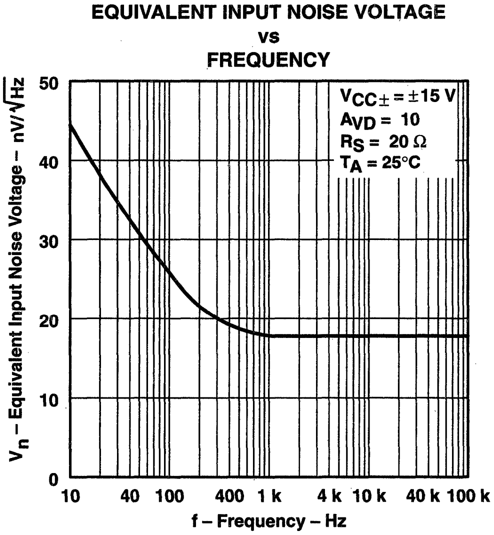


Figure 17

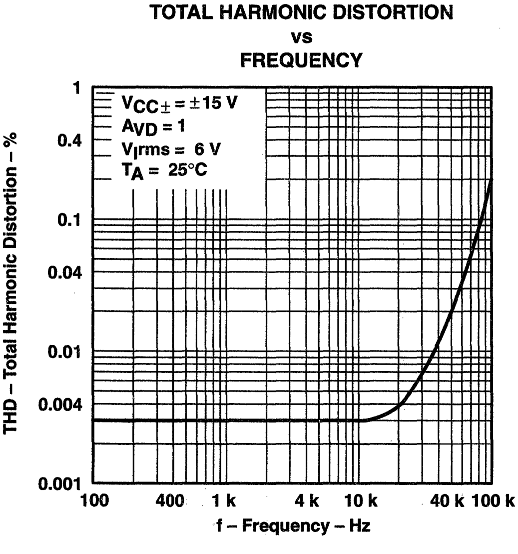


Figure 18

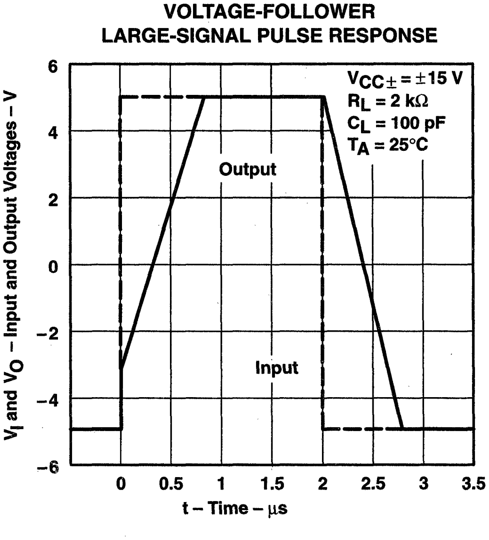


Figure 19

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
TIME

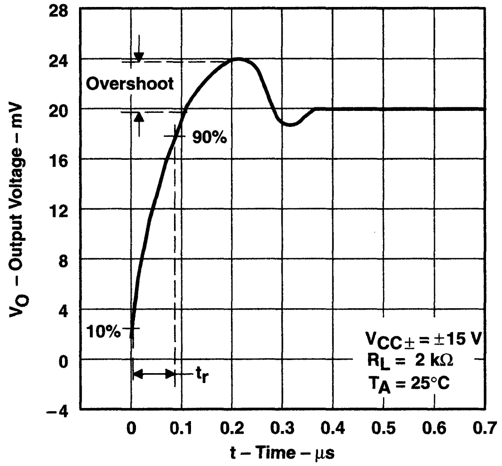


Figure 20

TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081D – FEBRUARY 1977 – REVISED FEBRUARY 1997

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **High Input Impedance . . . JFET-Input Stage**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

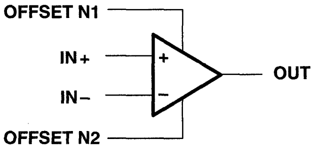
description

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

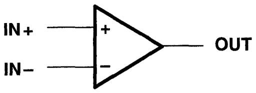
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

symbols

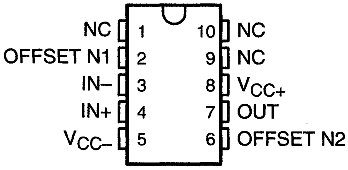
TL081



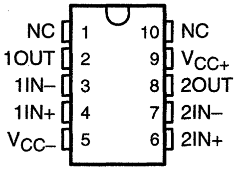
TL082 (EACH AMPLIFIER)
TL084 (EACH AMPLIFIER)



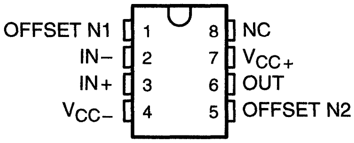
TL081M
U PACKAGE
(TOP VIEW)



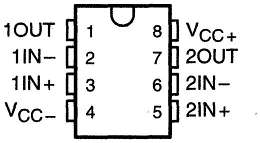
TL082M
U PACKAGE
(TOP VIEW)



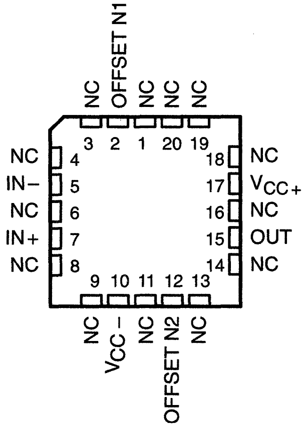
TL081, TL081A, TL081B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



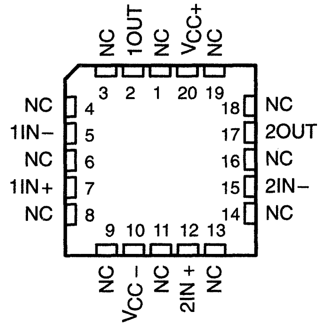
TL082, TL082A, TL082B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



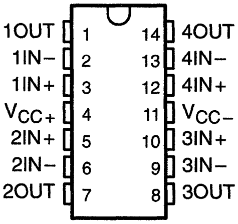
TL081M . . . FK PACKAGE
(TOP VIEW)



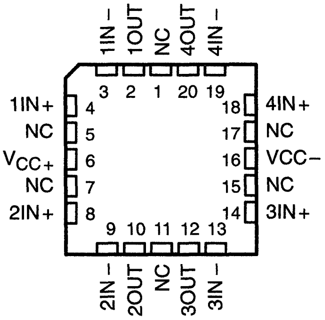
TL082M . . . FK PACKAGE
(TOP VIEW)



TL084, TL084A, TL084B
D, J, N, PW, OR W PACKAGE
(TOP VIEW)



TL084M . . . FK PACKAGE
(TOP VIEW)



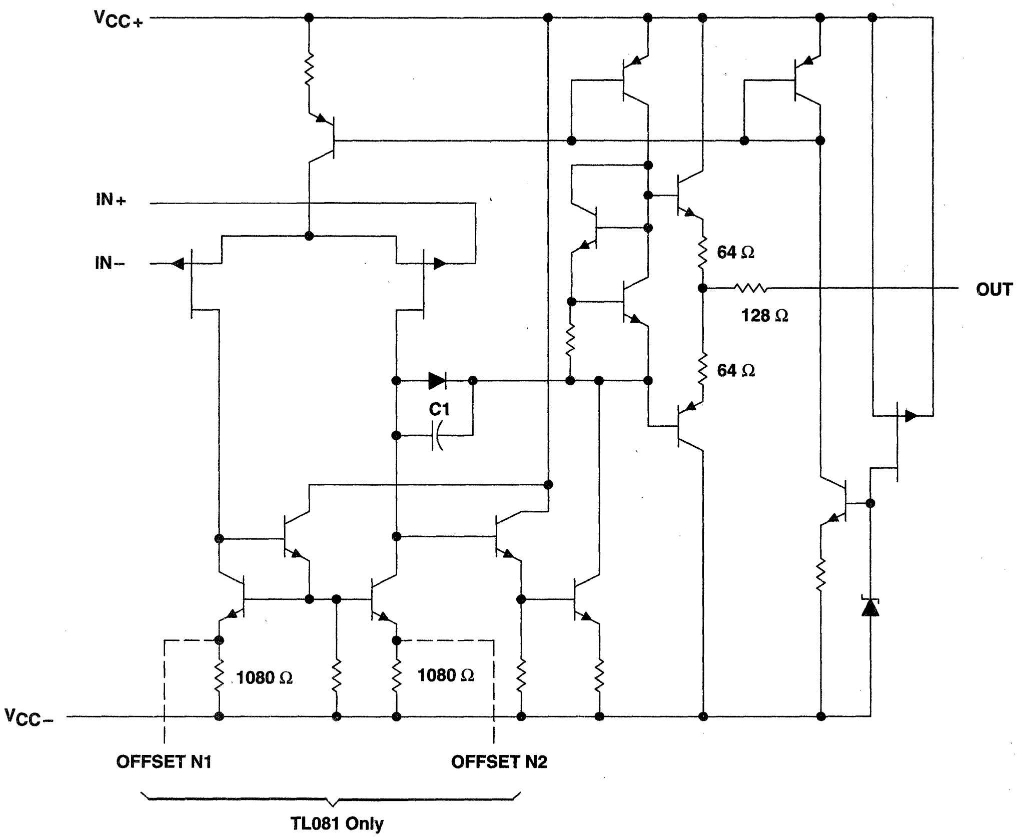
NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES										CHIP FORM (Y)
		SMALL OUTLINE (D008)	SMALL OUTLINE (D014)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP (PW)	FLAT PACK (U)	FLAT PACK (W)	
0°C to 70°C	15 mV 6 mV 3 mV	TL081CD TL081ACD TL081BCD	—	—	—	—	—	TL081CP TL081ACP TL081BCP	TL081CPW	—	—	—
	15 mV 6 mV 3 mV	TL082CD TL082ACD TL082BCD	—	—	—	—	—	TL082CP TL082ACP TL082BCP	TL082CPW	—	—	TL082Y
	15 mV 6 mV 3 mV	—	TL084CD TL084ACD TL084BCD	—	—	—	TL084CN TL084ACN TL084BCN	—	TL084CPW	—	—	TL084Y
−40°C to 85°C	6 mV 6 mV 6 mV	TL081ID TL082ID TL084ID	TL084ID	—	—	—	TL084IN	TL081IP TL082IP	—	—	—	—
−55°C to 125°C	6 mV 6 mV 9 mV	—	—	TL081MFK TL082MFK TL084MFK	TL084MJ	TL081MJG TL082MJG	—	—	—	TL081MU TL082MU	TL084MW	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TL081CDR).

schematic (each amplifier)

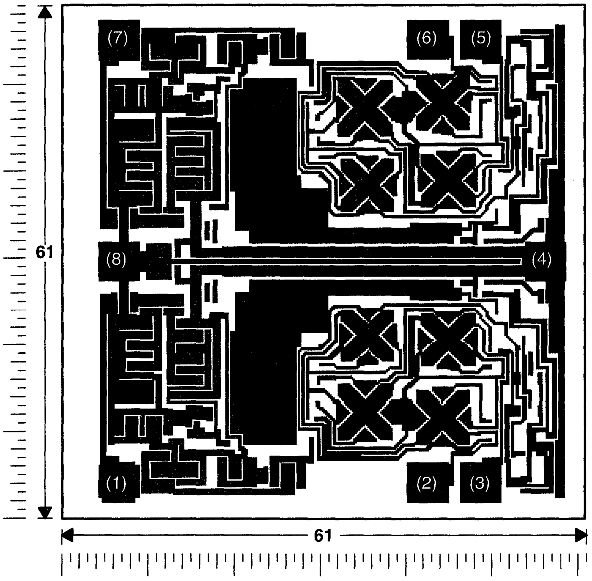


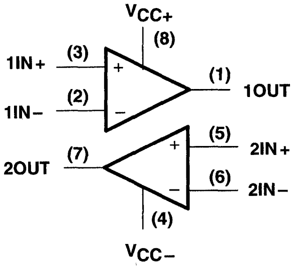
Component values shown are nominal.

TL082Y chip information

These chips, when properly assembled, display characteristics similar to the TL082. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

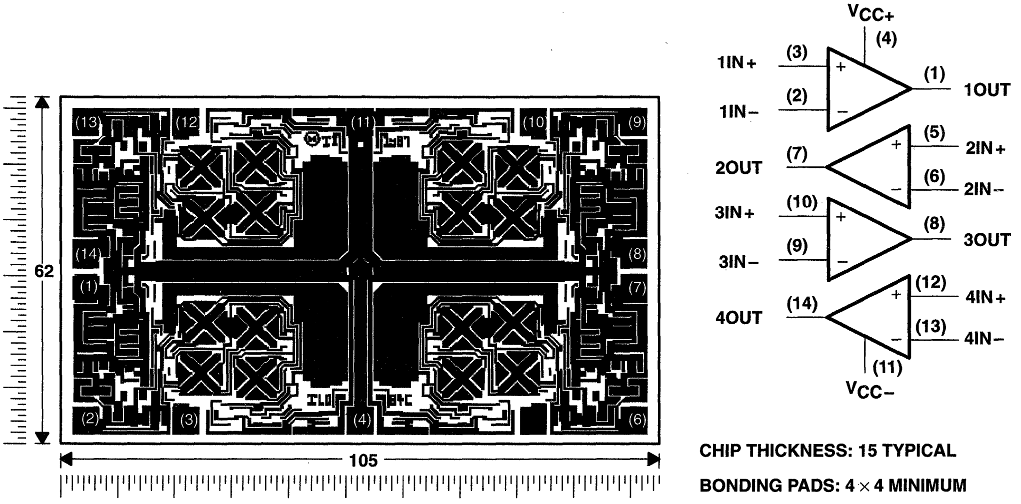
ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TL084Y chip information

These chips, when properly assembled, display characteristics similar to the TL084. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		TL08_C TL08_AC TL08_BC	TL08_I	TL08_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage, V_{ID} (see Note 2)		± 30	± 30	± 30	V
Input voltage, V_I (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range, T_A		0 to 70	– 40 to 85	– 55 to 125	°C
Storage temperature range, T_{stg}		– 65 to 150	– 65 to 150	– 65 to 150	°C
Case temperature for 60 seconds, T_C	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or JG package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, P, or PW package	260	260		°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	32°C	460 mW	373 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	25°C	448 mW	N/A	N/A
U	675 mW	5.4 mW/°C	25°C	432 mW	351 mW	135 mW
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL081C TL082C TL084C			TL081AC TL082AC TL084AC			TL081BC TL082BC TL084BC			TL081I TL082I TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	15		3	6		2	3		3	6	mV
			Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current‡	$V_O = 0$	25°C		5	200		5	100		5	100		5	100	pA
			Full range			2			2			2			10	nA
I_{IB}	Input bias current‡	$V_O = 0$	25°C		30	400		30	200		30	200		30	200	pA
			Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		$R_L \geq 10\ k\Omega$	Full range	±12			±12			±12			±12			
		$R_L \geq 2\ k\Omega$		±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25°C	25	200		50	200		50	200		50	200		V/mV
		$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	Full range	15			25			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	86		75	86		75	86		75	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ± 9 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	86		80	86		80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	$V_O = 0$, No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and −40°C to 85°C for TL08_I.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TL081M, TL082M			TL084M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	6		3	9	mV
			−55°C to 125°C			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	−55°C to 125°C		18			18		µV/°C
I_{IO}	Input offset current‡	$V_O = 0$	25°C		5	100		5	100	pA
			125°C			20			20	nA
I_{IB}	Input bias current‡	$V_O = 0$	25°C		30	200		30	200	pA
			125°C			50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	±12 to 15		±11	± 12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		±12	±13.5		V
		$R_L \geq 10\ k\Omega$	−55°C to 125°C	±12			±12			
		$R_L \geq 2\ k\Omega$		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25°C	25	200		25	200		V/mV
		$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	−55°C to 125°C	15			15			
B_1	Unity-gain bandwidth		25°C		3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ± 9 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	$V_O = 0$, No load	25°C		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1	8*	13		V/µs
		$V_I = 10$ V, $R_L = 2\ k\Omega$, $C_L = 100$ pF, $T_A = -55°C$ to 125°C, See Figure 1	5*			
t_r	Rise time	$V_I = 20$ mV, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.05		µs
	Overshoot factor			20%		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$ f = 1 kHz		18		nV/√Hz
		f = 10 Hz to 10 kHz		4		µV
I_n	Equivalent input noise current	$R_S = 20\ \Omega$, f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_{Irms} = 6$ V, $A_{VD} = 1$, $R_S \leq 1\ k\Omega$, $R_L \geq 2\ k\Omega$, f = 1 kHz		0.003%		

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL082Y, TL084Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$		3	15	mV
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$		18		μV/°C
I_{IO}	Input offset current‡	$V_O = 0$,			5	200	pA
I_{IB}	Input bias current‡	$V_O = 0$,			30	400	pA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$,		±12	±13.5		V
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V,	$R_L \geq 2\ k\Omega$	25	200		V/mV
B_1	Unity-gain bandwidth				3		MHz
r_i	Input resistance				10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $R_S = 50\ \Omega$	$V_O = 0$,	70 70	86 86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ±9 V, $V_O = 0$,	 $R_S = 50\ \Omega$	70 70	86 86		dB
I_{CC}	Supply current (per amplifier)	$V_O = 0$,	No load		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V,	$R_L = 2\ k\Omega$,	$C_L = 100$ pF,	See Figure 1	8	13		V/μs
t_r	Rise time	$V_I = 20$ mV,	$R_L = 2\ k\Omega$,	$C_L = 100$ pF,	See Figure 1		0.05		μs
	Overshoot factor						20%		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	f = 1 kHz				18		nV/√Hz
			f = 10 Hz to 10 kHz				4		μV
I_n	Equivalent input noise current	$R_S = 20\ \Omega$,	f = 1 kHz				0.01		pA/√Hz
THD	Total harmonic distortion	$V_I rms = 6$ V, f = 1 kHz	$A_{VD} = 1$,	$R_S \leq 1\ k\Omega$,	$R_L \geq 2\ k\Omega$,		0.003%		

PARAMETER MEASUREMENT INFORMATION

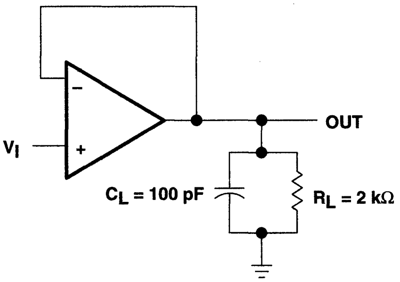


Figure 1

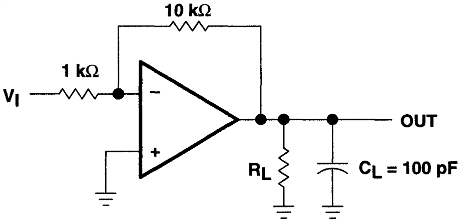


Figure 2

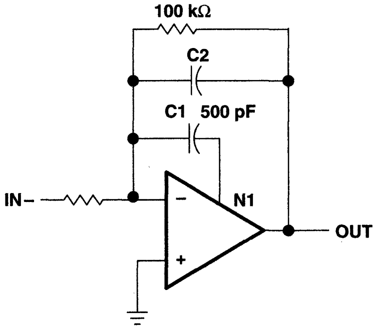


Figure 3

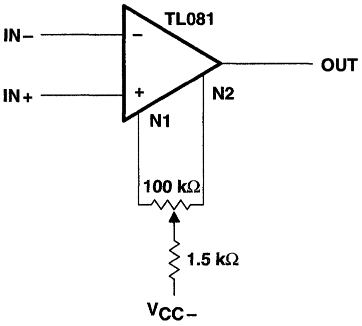


Figure 4

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OM}	Maximum peak output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Differential voltage amplification	vs Frequency with feed-forward compensation	13
P_D	Total power dissipation	vs Free-air temperature	14
I_{CC}	Supply current	vs Free-air temperature vs Supply voltage	15 16
I_{IB}	Input bias current	vs Free-air temperature	17
	Large-signal pulse response	vs Time	18
V_O	Output voltage	vs Elapsed time	19
CMRR	Common-mode rejection ratio	vs Free-air temperature	20
V_n	Equivalent input noise voltage	vs Frequency	21
THD	Total harmonic distortion	vs Frequency	22

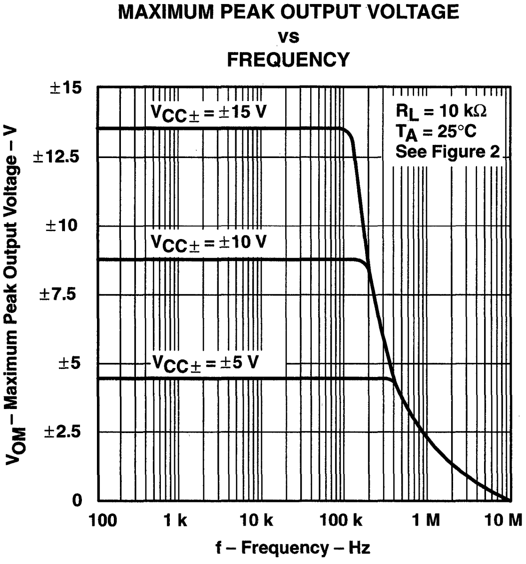


Figure 5

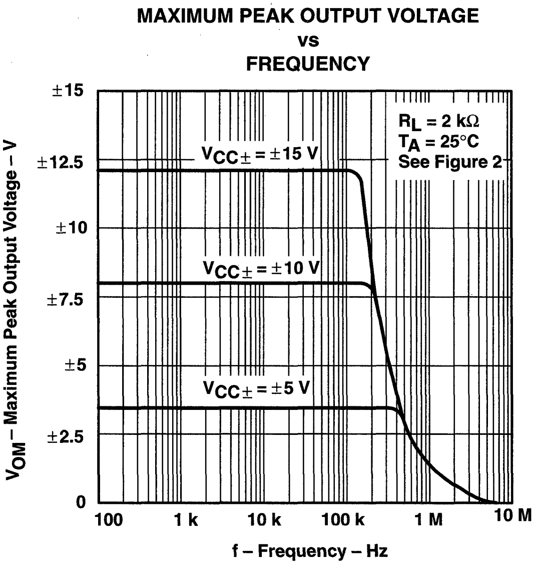


Figure 6

TYPICAL CHARACTERISTICS†

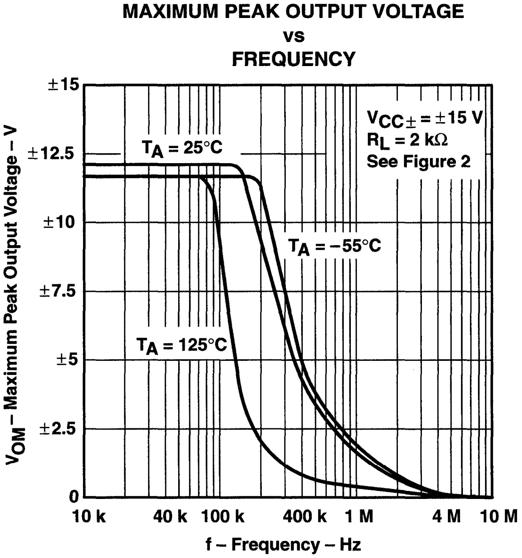


Figure 7

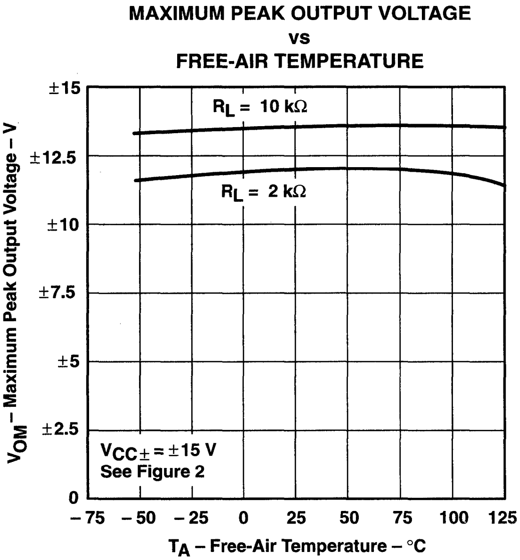


Figure 8

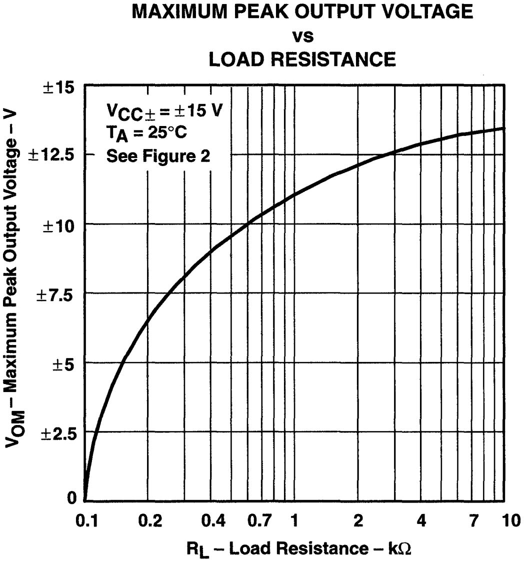


Figure 9

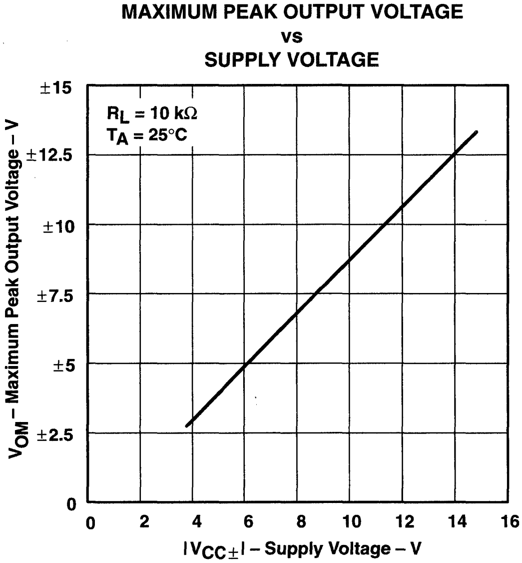


Figure 10

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

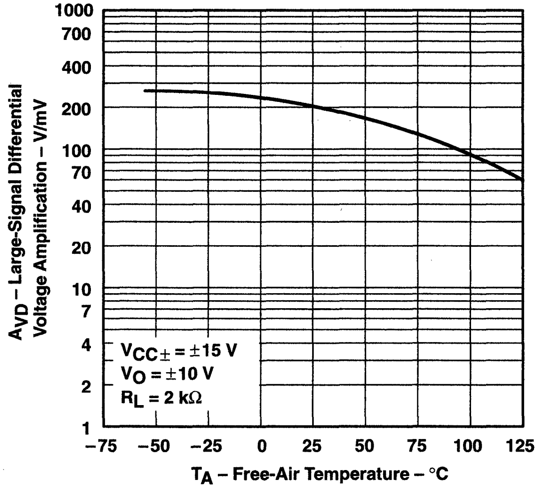

Figure 11

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

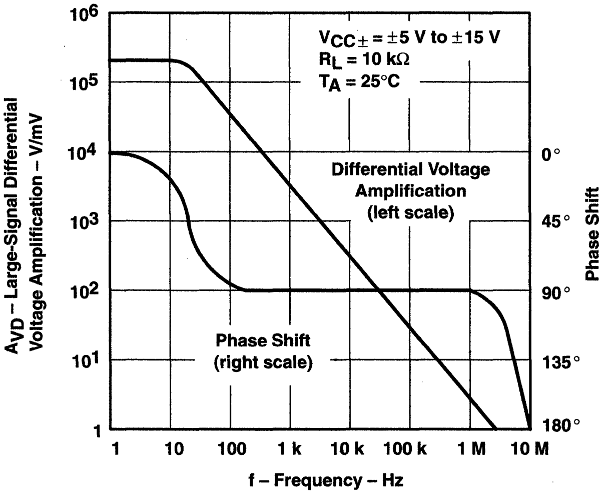

Figure 12

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

**DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY WITH FEED-FORWARD COMPENSATION**

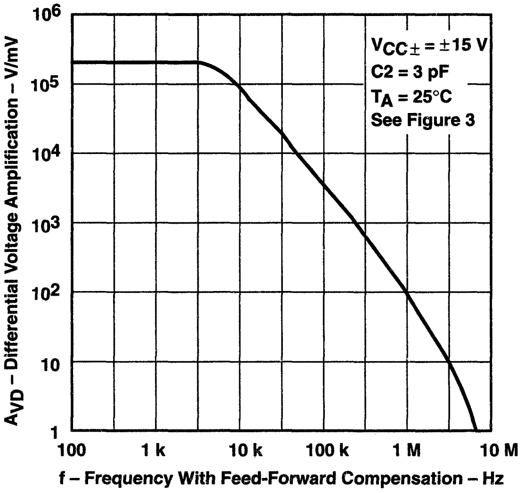

Figure 13

**TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE**

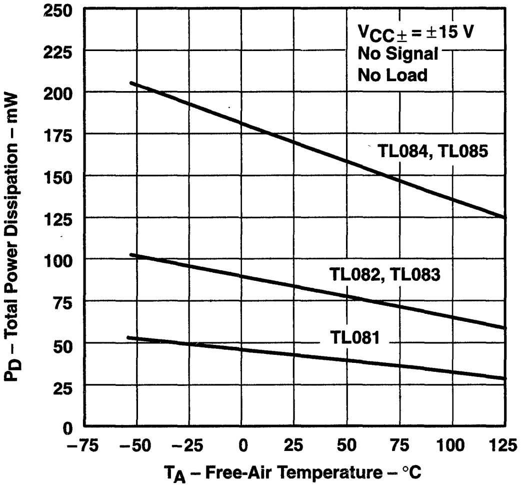

Figure 14

**SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE**

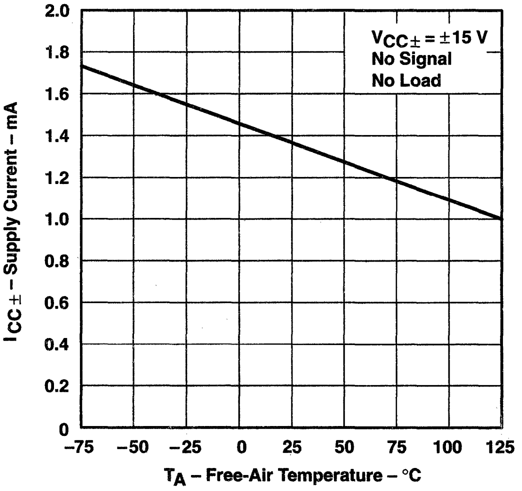

Figure 15

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

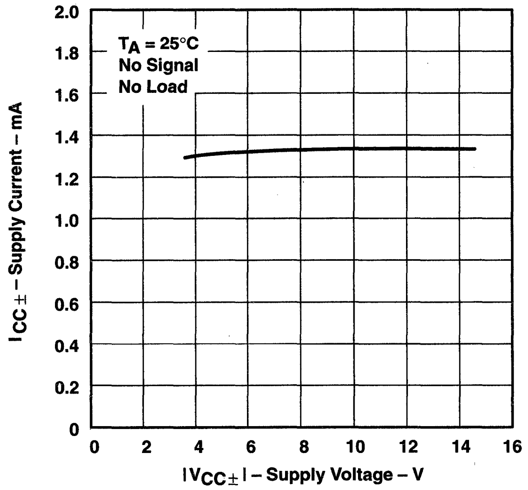

Figure 16

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

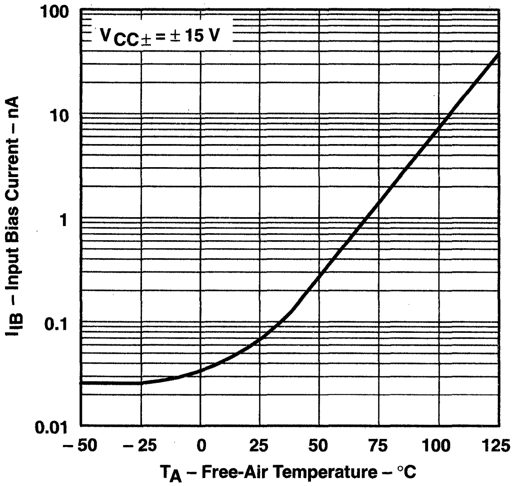

Figure 17

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

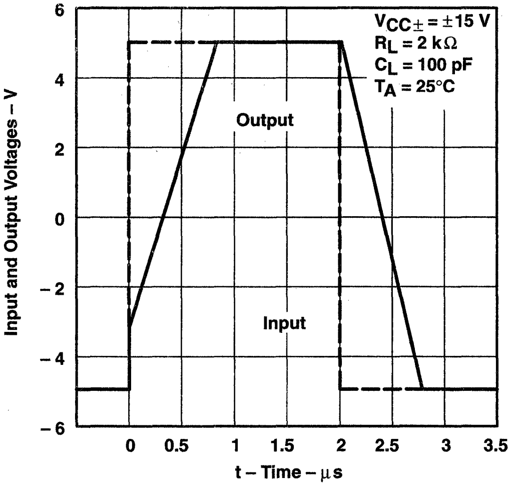

Figure 18

OUTPUT VOLTAGE vs ELAPSED TIME

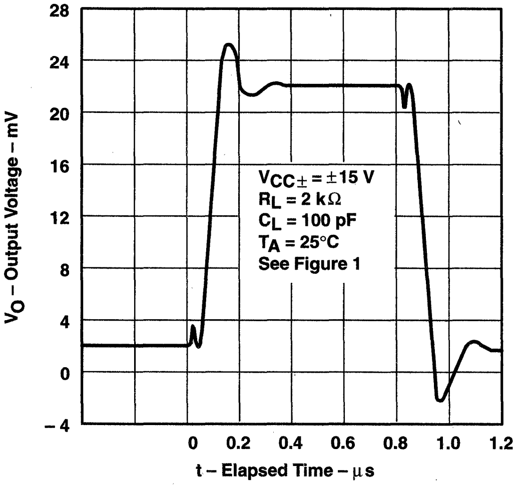

Figure 19

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

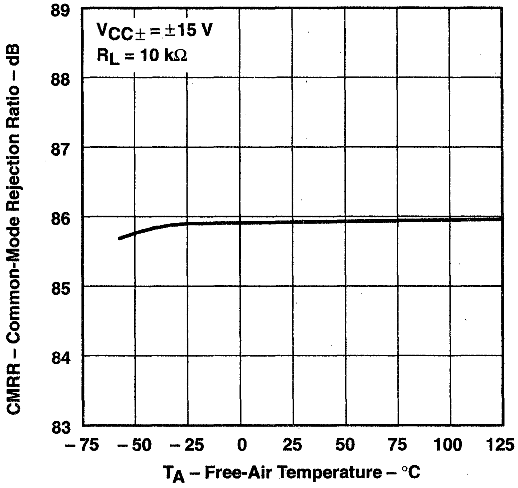

Figure 20

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

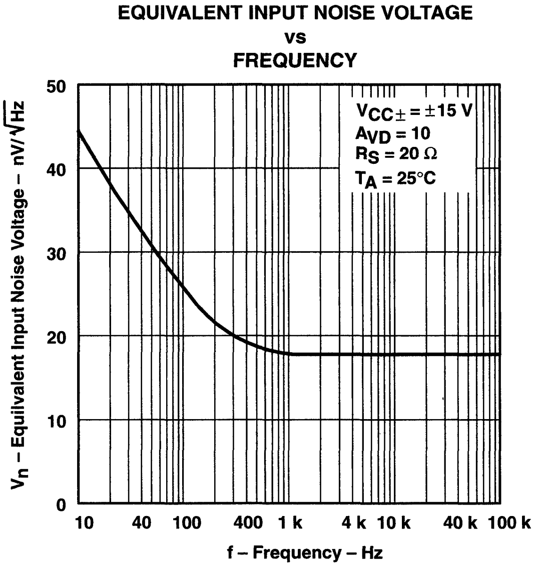


Figure 21

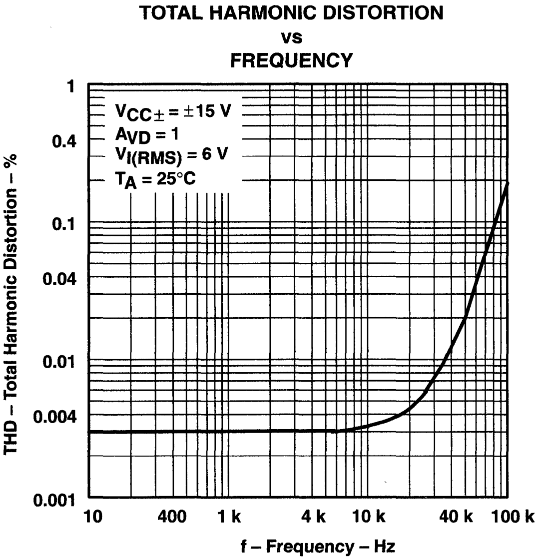
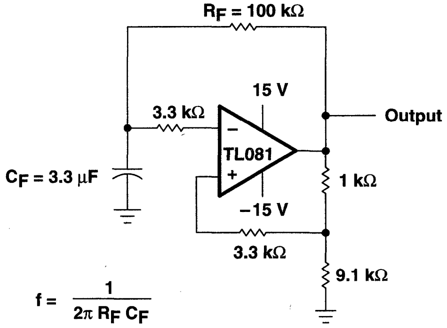


Figure 22

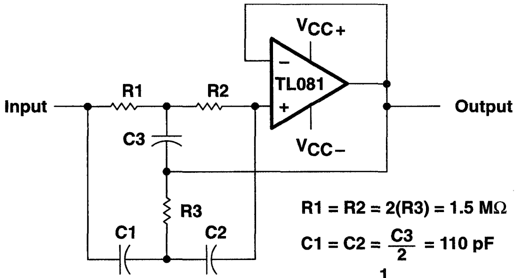
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION



$$f = \frac{1}{2\pi R_F C_F}$$

Figure 23



R1 = R2 = 2(R3) = 1.5 MΩ

$$C1 = C2 = \frac{C3}{2} = 110\ pF$$

$$f_o = \frac{1}{2\pi\ R1\ C1} = 1\ kHz$$

Figure 24

APPLICATION INFORMATION

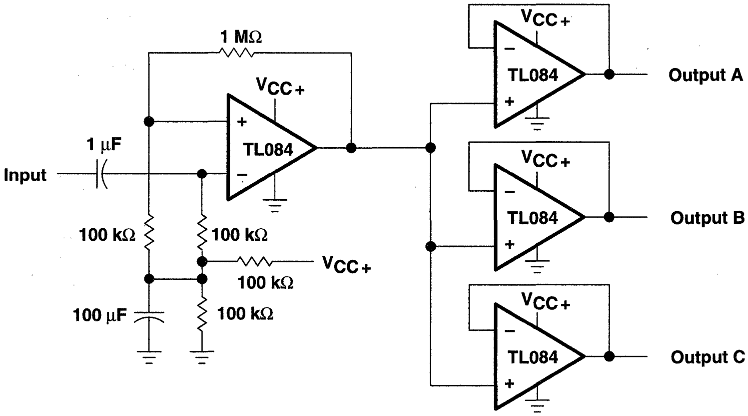
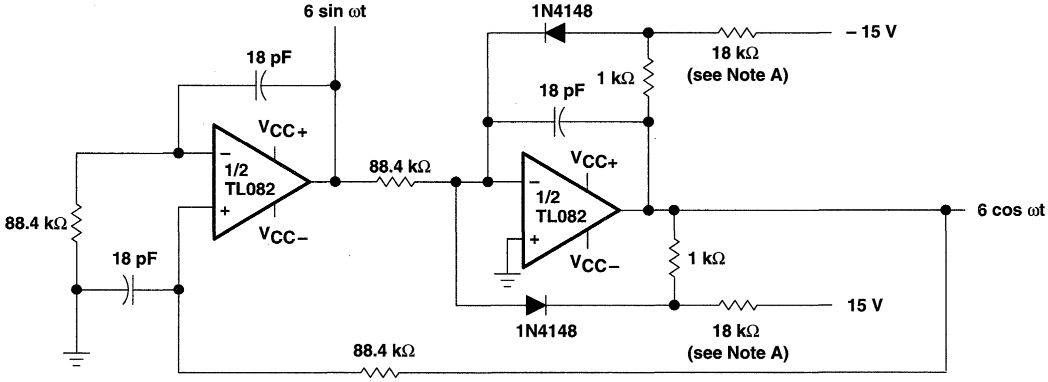


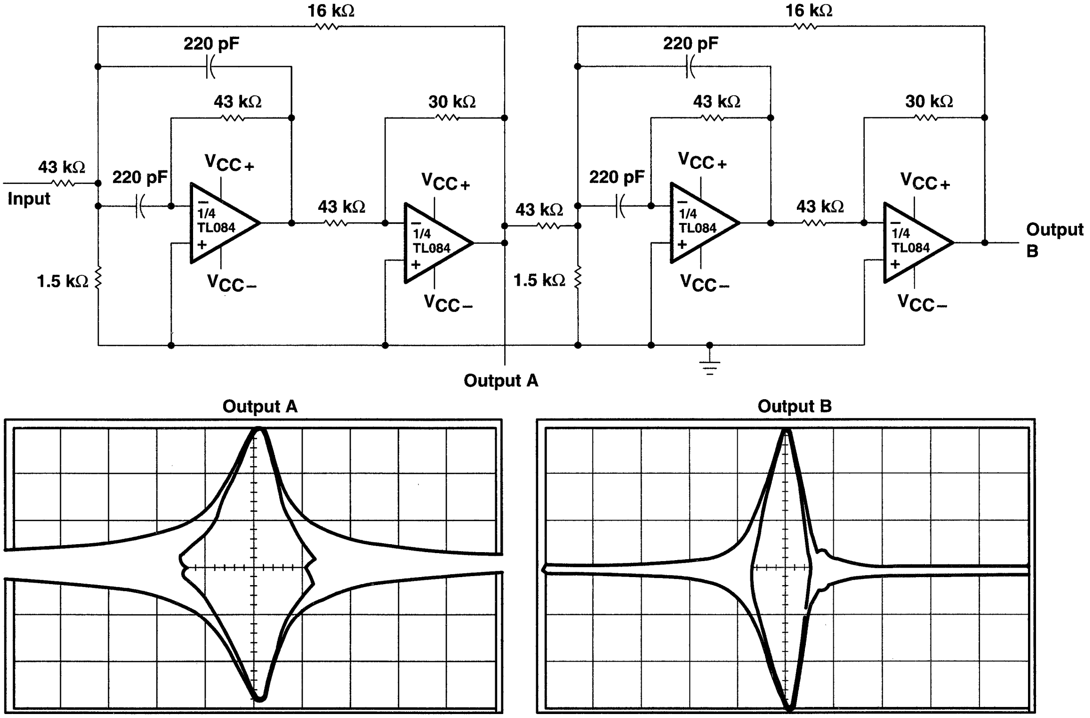
Figure 25. Audio-Distribution Amplifier



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-KHz Quadrature Oscillator

APPLICATION INFORMATION



2 kHz/div
Second-Order Bandpass Filter
f_O = 100 kHz, Q = 30, GAIN = 4

2 kHz/div
Cascaded Bandpass Filter
f_O = 100 kHz, Q = 69, GAIN = 16

Figure 27. Positive-Feedback Bandpass Filter

TL084x2
JFET-INPUT OCTAL OPERATIONAL AMPLIFIER

SLOS136 – APRIL 1994

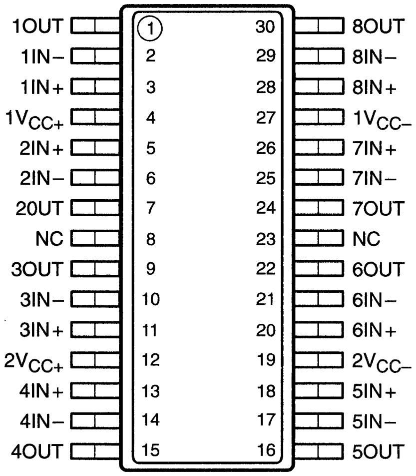
- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **High Input Impedance . . . JFET-Input Stage**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

description

The TL084x2 JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The device features high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

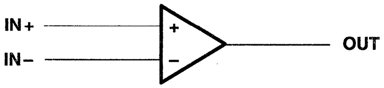
The TL084x2 is characterized for operation from 0°C to 70°C.

DB PACKAGE
(TOP VIEW)



NC – No internal connection

symbol (each amplifier)

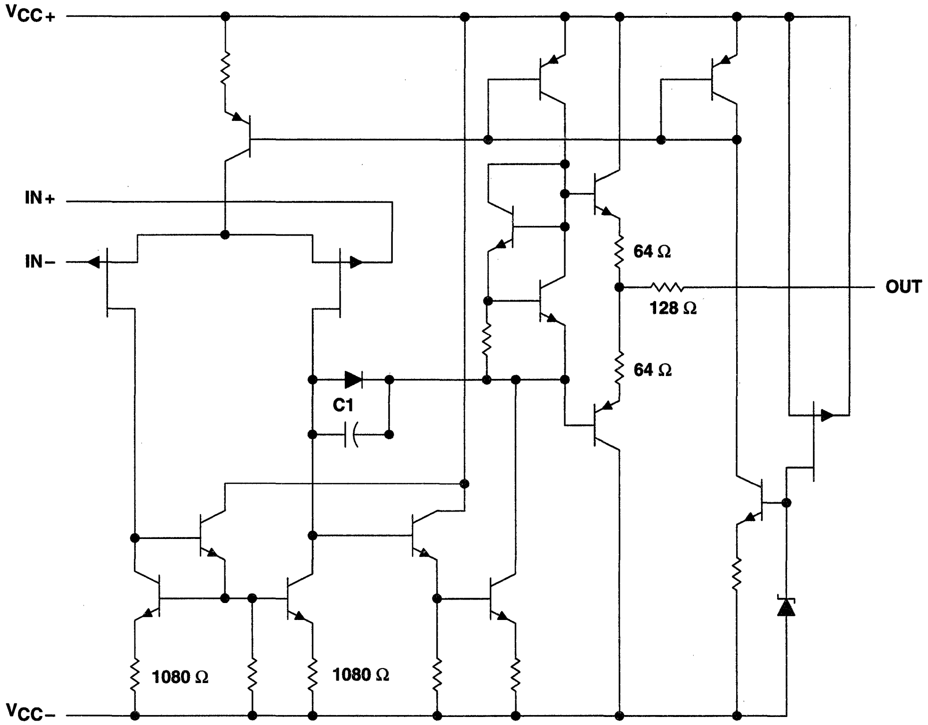


AVAILABLE OPTION

T_A	V_{IO}max AT 25°C	PACKAGE
		SMALL OUTLINE (DB)†
0°C to 70°C	15 mV	TL084x2DBLE

† The DB package is only available left-end taped and reeled.

schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT	
Resistors	76
Transistors	120
JFET	20
Diodes	12
Capacitors	8

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	–18 V
Differential input voltage, V_{ID} (see Note 2)	±30 V
Input voltage, V_I (any input) (see Notes 1 and 3)	±15 V
Duration of output short circuit to ground (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages and V_{CC} specified for the measurement of I_{OS}, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN + with respect to IN –.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output can be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	1024 mW	8.2 mW/°C	655 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$	25°C		5	15	mV
				Full range			20	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$	Full range		10		μV/°C
I_{IO}	Input offset current	$V_O = 0$		25°C		5	200	pA
				Full range			5	nA
I_{IB}	Input bias current§	$V_O = 0$		25°C		30	400	pA
				Full range			10	nA
V_{ICR}	Common-mode input voltage range			25°C	±10	±11		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$		25°C	±12	±13.5		V
		$R_L \geq 10\ k\Omega$		Full range	±12			
		$R_L \geq 2\ k\Omega$			±10	±12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V,	$R_L \geq 2\ k\Omega$	25°C	25	200		V/mV
		$V_O = \pm 10$ V,	$R_L \geq 2\ k\Omega$	Full range	15			
B_1	Unity-gain bandwidth			25°C		3		MHz
r_i	Input resistance			25°C		10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $R_S = 50\ \Omega$	$V_O = 0$,	25°C	70	76		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ± 9 V, $R_S = 50\ \Omega$	$V_O = 0$,	25°C	70	76		dB
I_{CC}	Supply current (per amplifier)	$V_O = 0$,	No load	25°C		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡ Full range is 0°C to 70°C.
§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 14. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		13		V/μs
t_r	Rise time	$V_I = 20$ mV, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.05		μs
	Overshoot factor			20%		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$, f = 1 kHz		18		nV/√Hz

PARAMETER MEASUREMENT INFORMATION

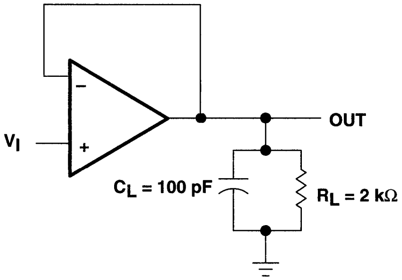


Figure 1. Unity-Gain Amplifier

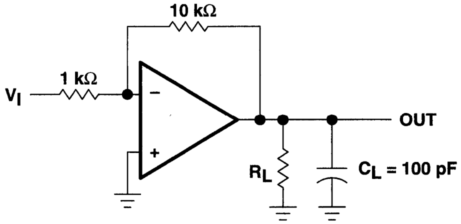


Figure 2. Gain-of-10 Inverting Amplifier

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OM}	Maximum peak output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	3, 4, 5 6 7 8
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	9 10
P_D	Total power dissipation	vs Free-air temperature	11
I_{CC}	Supply current	vs Free-air temperature vs Supply voltage	12 13
I_{IB}	Input bias current	vs Free-air temperature	14
	Pulse response	Large signal	15
V_O	Output voltage	vs Elasped time	16
CMRR	Common-mode rejection ratio	vs Free-air temperature	17
V_n	Equivalent input noise voltage	vs Frequency	18
THD	Total harmonic distortion	vs Frequency	19
	Phase shift	vs Free-air temperature	10

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

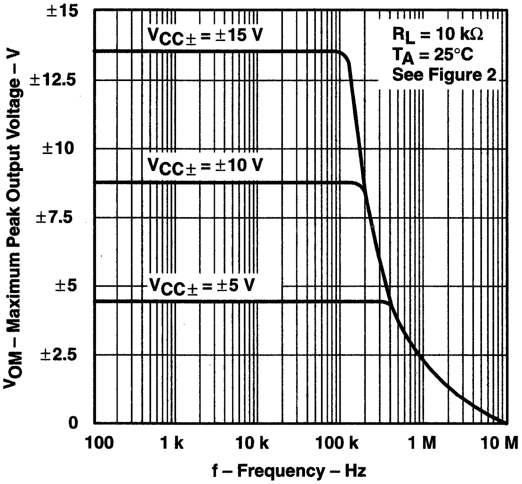


Figure 3

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

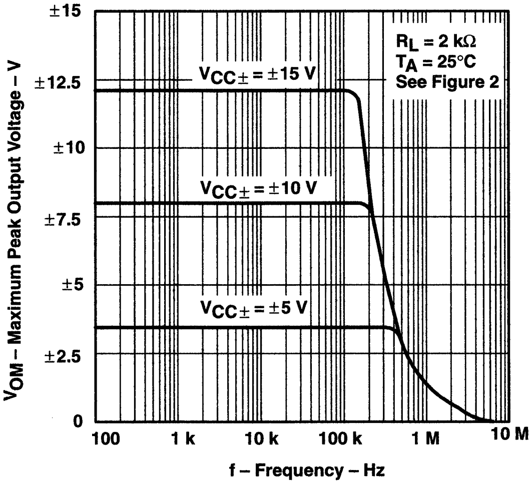


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

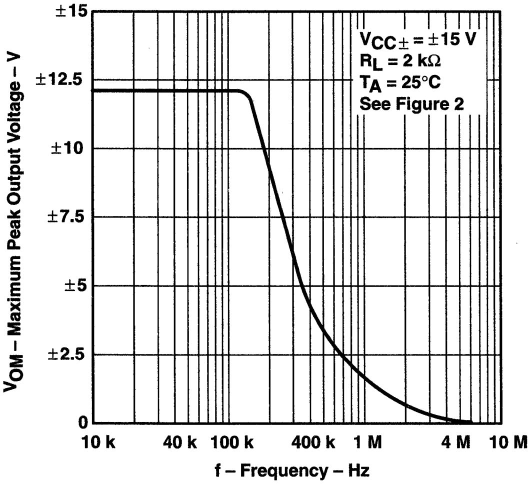


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

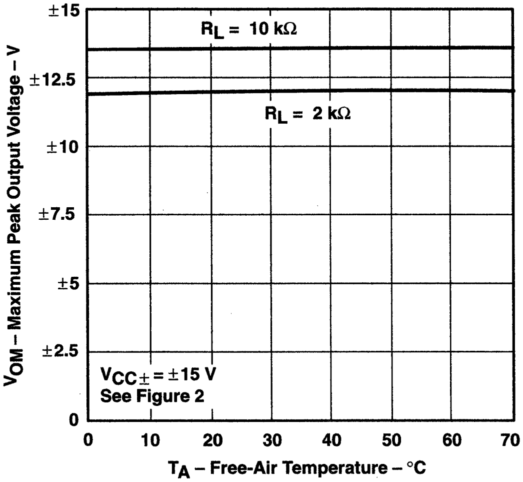


Figure 6

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

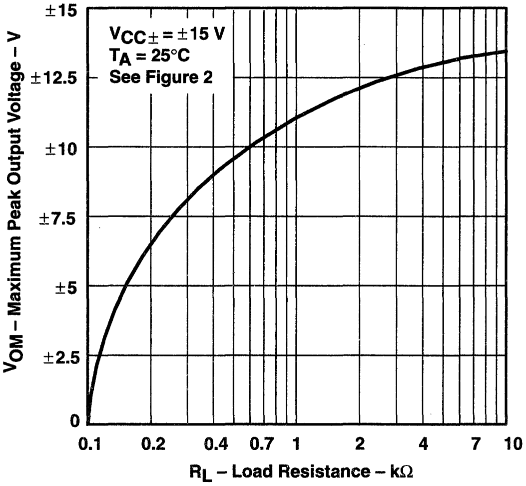


Figure 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

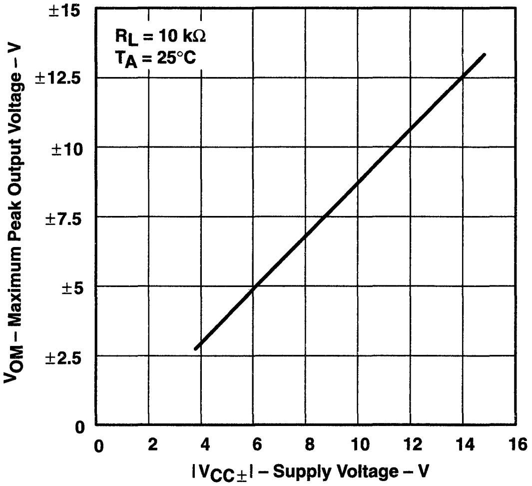


Figure 8

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

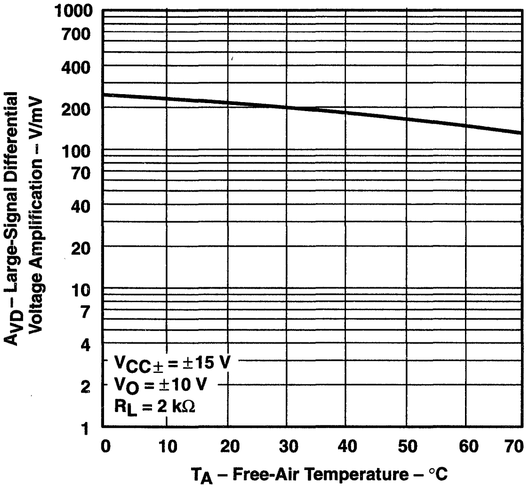


Figure 9

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

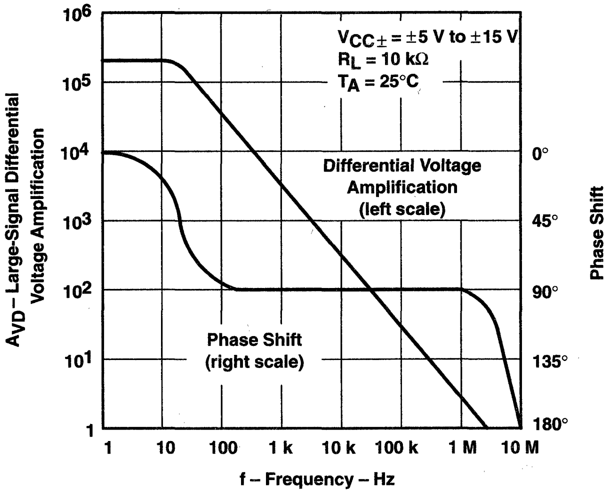


Figure 10

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

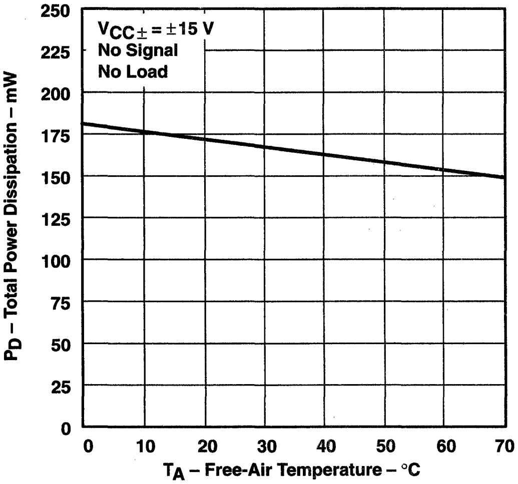


Figure 11

SUPPLY CURRENT (PER AMPLIFIER) vs FREE-AIR TEMPERATURE

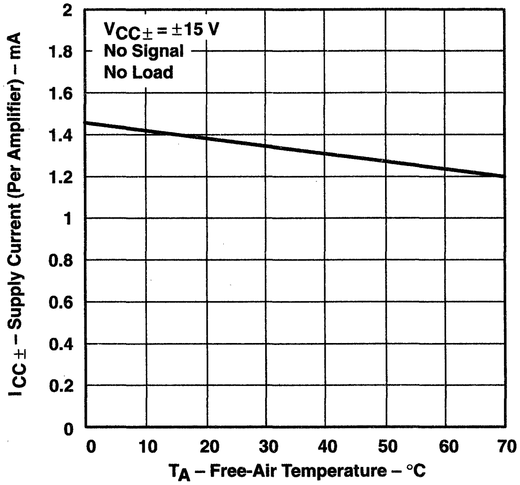


Figure 12

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

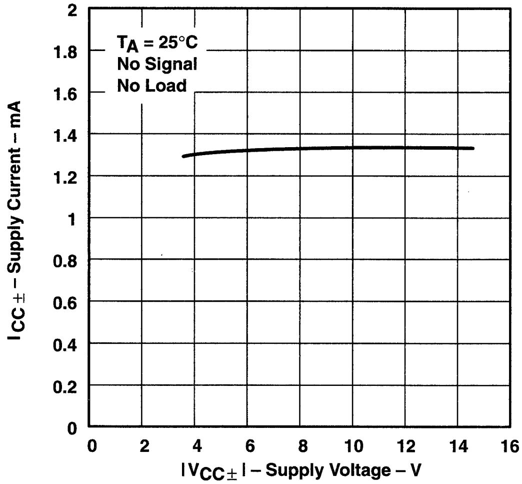


Figure 13

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

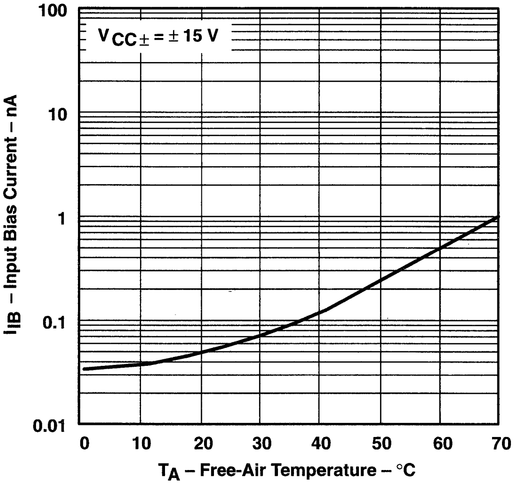


Figure 14

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

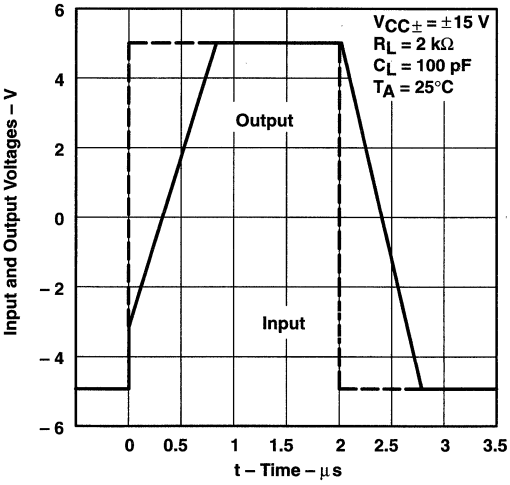


Figure 15

OUTPUT VOLTAGE vs ELAPSED TIME

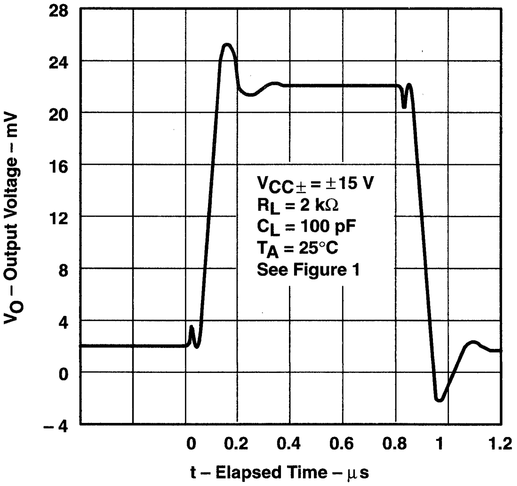


Figure 16

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

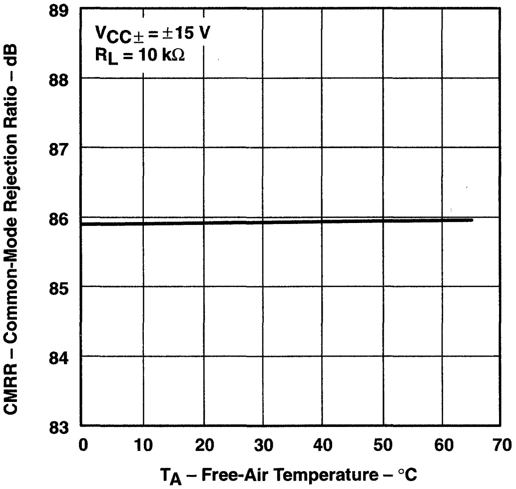


Figure 17

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

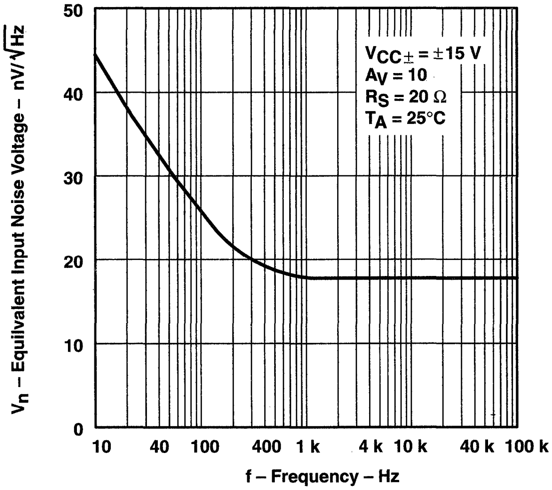


Figure 18

TOTAL HARMONIC DISTORTION vs FREQUENCY

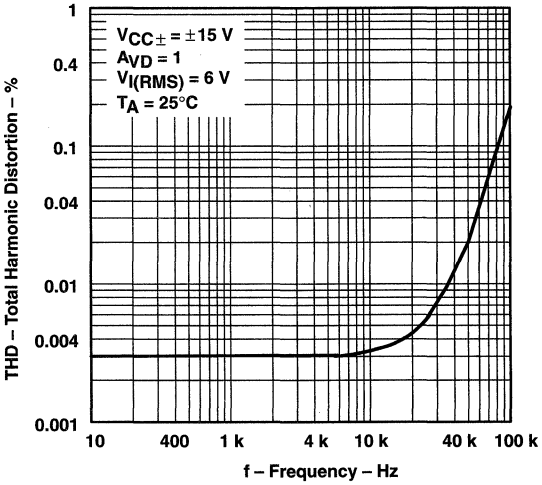


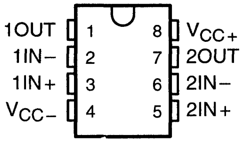
Figure 19

TL2828Z, TL2828Y
HIGH-TEMPERATURE DUAL OPERATIONAL AMPLIFIERS

SLOS104 – DECEMBER 1991

- **Operating Free-Air Temperature Range −40°C to 150°C**
- **Wide Range of Supply Voltages:**
  - **Single Supply**
  - **or Dual Supply . . . 4 V to 30 V**
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.7 mA Typ**
- **Internal Frequency Compensation**
- **Low Input Bias and Offset Parameters**
  - **Input Offset Voltage . . . 3 mV Typ**
  - **Input Offset Current . . . 2 nA Typ**
  - **Input Bias Current . . . 15 nA Typ**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 30 V**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**

TL2828Z . . . D OR P PACKAGE
(TOP VIEW)



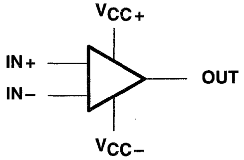
description

The TL2828Z and TL2828Y devices consist of two independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate over a wide range of voltages from a single supply. Operation from split supplies is also possible as long as the difference between the two supplies is 4 V to 30 V, and V_{CC} is at least 1.5 V more positive than the common-mode input voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply voltage systems. For example, the TL2828Z can be operated on automotive engine blocks directly off the standard 12-V supply with minimal electrical protection.

The TL2828Z is characterized for operation over the extended temperature range of −40°C to 150°C.

symbol (each amplifier)

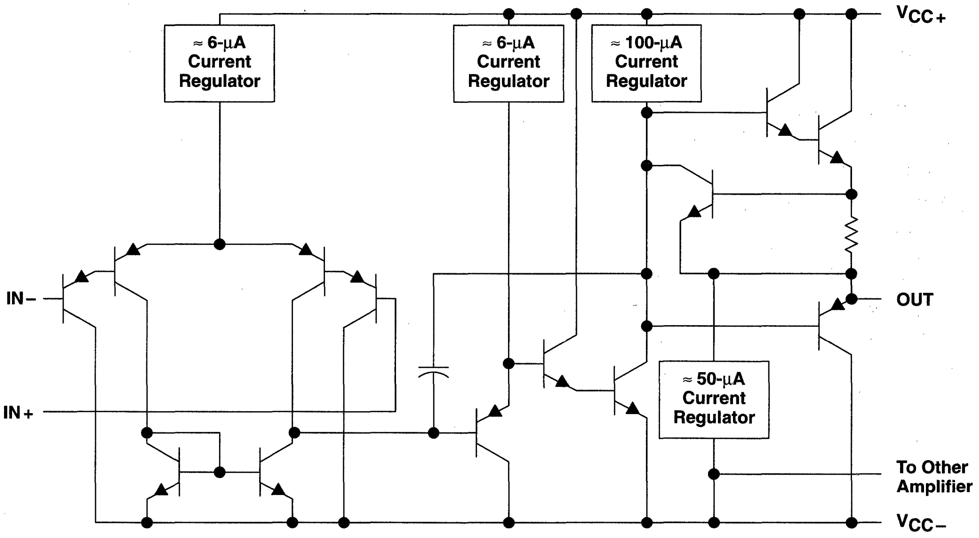


AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
−40°C to 150°C	7 mV	TL2828ZD	TL2828ZP	TL2828Y

The D packages are available taped and reeled. Add R suffix to device type (i.e., TL2828ZDR).
The chip form is tested at T_A = 25°C.

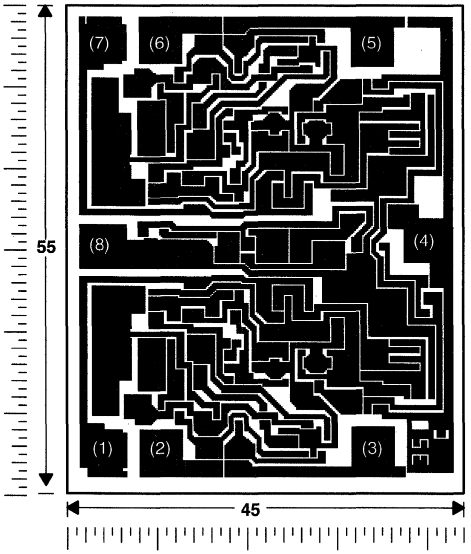
equivalent schematic (each amplifier)

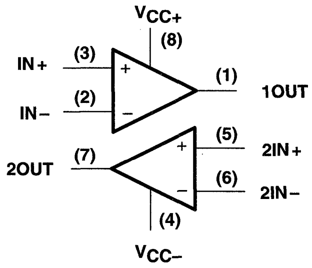


TL2828Y chip information

This chip, when properly assembled, displays characteristics similar to the TL2828Z. Thermal compression bonding may be used on the gold bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	16 V
Supply voltage, V_{CC-}	−16 V
Differential input voltage, V_{ID} (see Note 2)	±32 V
Input voltage range, V_I (any input)	−16 V to 16 V
Input current, I_I (each input)	±1 mA
Output current, I_O	±40 mA
Total current into V_{CC+}	60 mA
Total current out of V_{CC-}	60 mA
Duration of short-circuit at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−40°C to 150°C
Storage temperature range	−65°C to 165°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} when dual supplies are specified (e.g., $V_{CC\pm} = \pm 15$ V) and with respect to V_{CC-} when a single supply is specified (e.g., $V_{CC} = 5$ V).
2. Differential voltages are at the noninverting input with respect to the noninverting input. Excessive current will flow if the input is below V_{CC-}.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING	$T_A = 150°C$ POWER RATING
D	812 mV	5.8 mW/°C	551 mW	348 mW	232 mW	87 mW
P	1120 mV	8.0 mW/°C	760 mW	480 mW	320 mW	120 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±2	±15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 2.5$ V	−2.5	0.5	V
	$V_{CC\pm} = \pm 15$ V	−15	13	
Input voltage range, V_I	$V_{CC\pm} = \pm 2.5$ V	−2.5	0.5	V
	$V_{CC\pm} = \pm 15$ V	−15	13	
Operating free-air temperature, T_A		−40	150	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL2828Z			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 1.4 V, R_S = 50 Ω	25°C		3	7	mV
			Full range			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		15		µV/°C
I_{IO}	Input offset current		25°C		2	30	nA
			Full range			200	
I_{IB}	Input bias current		25°C		−15	−100	nA
			Full range			−500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	0 to 3.5		V
			Full range	0 to 3			
V_{OH}	High-level output voltage	I_{OH} = 0.1 mA	25°C	3.3	3.7		V
			Full range	3.2			
		I_{OH} = 1 mA	25°C	3.3	3.6		
			Full range	3.2			
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA	25°C	0.8	0.6		V
			Full range	1			
		I_{OL} = 1 mA	25°C	0.9	0.7		
			Full range	1.1			
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 3.5 V, R_L = 2 kΩ	25°C	25	100		V/mV
			Full range	0.7			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 1.4 V, R_S = 50 Ω	25°C	65	80		dB
			Full range	45			
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_L = 10 kΩ	25°C	65	100		dB
			Full range	65			
I_{CC}	Supply current (total package)	V_{IC} = 0, V_O = 2.5 V, No load	25°C		0.7	1.2	mA
			Full range			1.2	
ΔI_{CC}	Supply current change over operating temperature range		Full range		140		µA

† Full range is −40°C to 150°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL2828Z			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		3	7	mV
			Full range			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		15		µV/°C
I_{IO}	Input offset current		25°C		2	30	nA
			Full range			200	
I_{IB}	Input bias current		25°C		−15	−100	nA
			Full range			−500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−15 to 13.5			V
			Full range	−15 to 13			
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -0.1$ mA	25°C	13.2	14.1		V
			Full range	13.1			
		$I_O = -1$ mA	25°C	13.1	14		
			Full range	13			
		$I_O = -10$ mA	25°C	12.8	−13.6		
			Full range	12.7			
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 0.1$ mA	25°C	−13.7	−14.4		V
			Full range	−13.1			
		$I_O = 1$ mA	25°C	−13.6	−14.3		
			Full range	−13			
		$I_O = 7$ mA	25°C	−12.9	−13.8		
			Full range	−12.5			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, $V_O = -5$ V to 5 V	25°C	25	100		V/mV
			Full range	0.8			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 1.4$ V, $R_S = 50\ \Omega$	25°C	65	75		dB
			Full range	50			
k_{SVR}	Supply-voltage rejection ratio	$V_{CC} = 5$ V to 30 V, $R_L = 50\ k\Omega$	25°C	65	100		dB
			Full range	65			
I_{CC}	Supply current (total package)	$V_{IC} = 0$, $V_O = 0$, No load	25°C		0.7	2	mA
			Full range			2	
ΔI_{CC}	Supply current change over operating temperature range		Full range		140		µA

† Full range is −40°C to 150°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TL2828Z			UNIT
				MIN	TYP	MAX	
SR+	Positive slew rate	V_O = 1 V to 4.5 V, A_{VD} = 1, R_L = 2 k Ω‡, C_L = 100 pF	25°C	0.15			V/μs
			Full range	0.1			
SR–	Negative slew rate		25°C	0.15			
			Full range	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		39		nV/√Hz
		f = 10 kHz			23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		0.9		μV
B_1	Unity-gain bandwidth	R_L = 10 kΩ‡, C_L = 100 pF	25°C		400		kHz
ϕ_m	Phase margin	R_L = 10 kΩ‡, C_L = 100 pF	25°C		60°		

† Full range is –40°C to 150°C.
‡ R_L terminates at 0 V.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS				UNIT
				TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		3	7	mV
I_{IO}	Input offset current			2	30	nA
I_{IB}	Input bias current			–15	–100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	–15 to 13.5			V
V_{OM+}	Maximum positive peak output voltage swing	I_O = –0.1 mA	13.2	14.1		V
		I_O = –1 mA	13.1	14		
		I_O = –10 mA	12.8	13.6		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 0.1 mA	–13.7	–14.4		V
		I_O = 1 mA	–13.6	–14.3		
		I_O = 10 mA	–12.9	–13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to –1.5 V, R_L = 2 kΩ	25	100		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 28 V, V_O = 1.4 V, R_S = 50 Ω	65	75		dB
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_L = 10 kΩ	65	100		dB
I_{CC}	Supply-current (total package)	V_{IC} = 0, V_O = 0, No load		0.7	2	mA

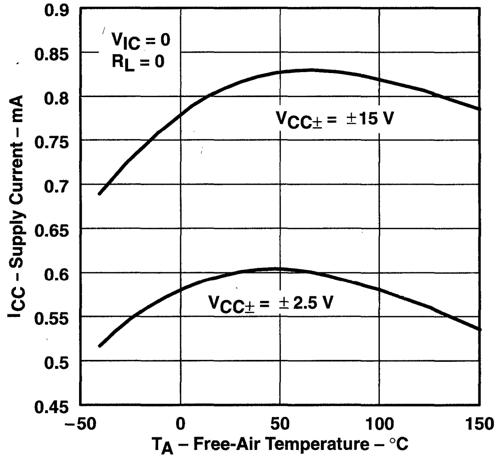
TL2829Z, TL2829Y
HIGH-TEMPERATURE QUADRUPLE OPERATIONAL AMPLIFIERS

SLOS067A – APRIL 1991 – REVISED MARCH 1993

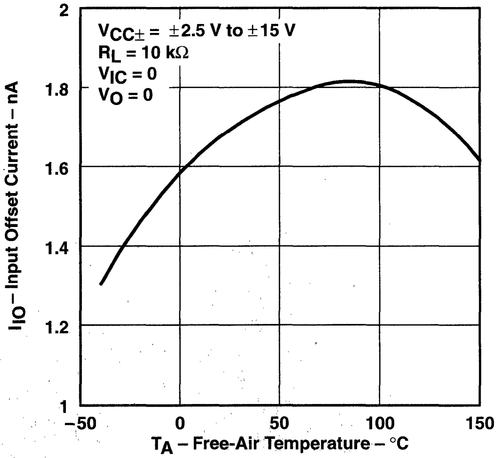
- **Free-Air Operating Temperature Range −40°C to 150°C**
- **Wide Range of Supply Voltages:**
  - **Single Supply . . . 4 V to 30 V**
  - **or Dual Supplies**
- **Low Supply Current Drain independent of Supply Voltage . . . 0.8 mA**
- **Internal Frequency Compensation**
- **Low Input Bias and Offset Parameters at 25°C**
  - **Input Offset Voltage . . . 3 mV Typ**
  - **Input Offset Current . . . 2 nA Typ**
  - **Input Bias Current . . . 15 nA Typ**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 30 V**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ at 25°C**

description

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



description

These devices consist of four independent, high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible as long as the difference between the two supplies is 4 V to 30 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, the TL2829 can be operated on automotive engine blocks directly off the standard 12-V supply with minimal electrical protection.

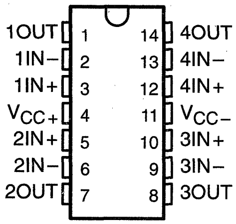
The TL2829 is characterized for operation over the extended temperature range of −40°C to 150°C.

AVAILABLE OPTIONS

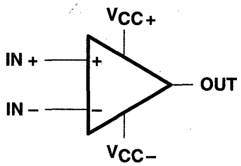
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	
−40°C to 150°C	7 mV	TL2829ZD	TL2829ZN	TL2829Y

The D packages are available taped and reeled. Add R suffix to device type (i.e., TL2829ZDR).

TL2829Z . . . D OR N PACKAGE
(TOP VIEW)



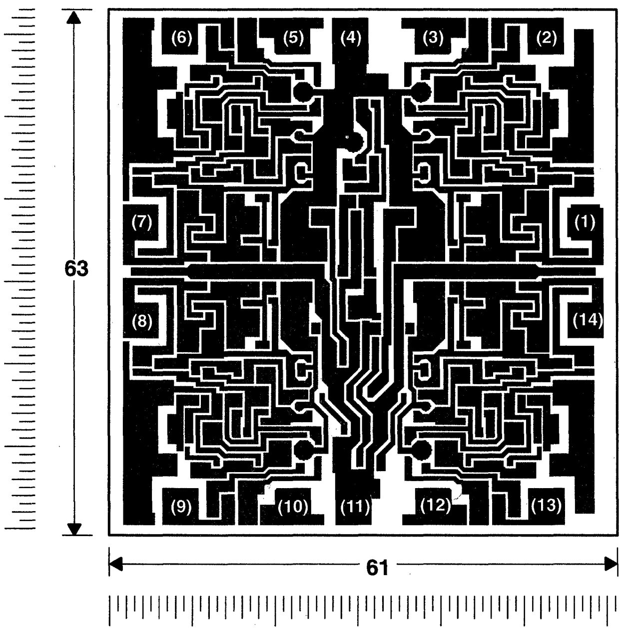
symbol (each amplifier)

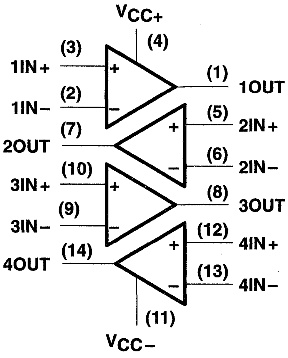


TL2829Y chip information

This chip, properly assembled, displays characteristics similar to the TL2829. Thermal compression bonding may be used on the gold bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

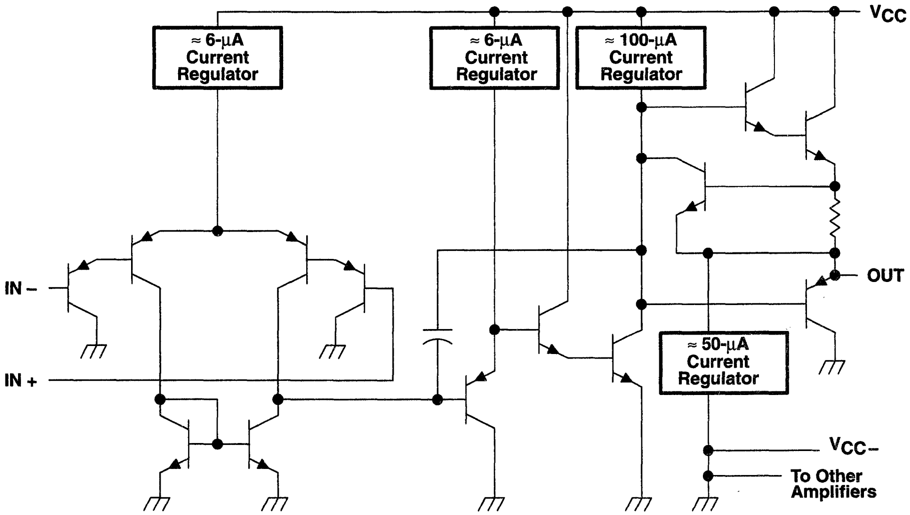
BONDING PADS: 4 X 4 MINIMUM

$T_J$max = 165°C

TOLERANCES ARE ± 10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (each amplifier)



COMPONENT COUNT (total device)	
Epi-FET	1
Diodes	4
Resistors	11
Transistors	95
Capacitors	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	16 V
Supply voltage, V_{CC-} (see Note 1)	−16 V
Differential input voltage, V_{ID} (see Note 2)	±32 V
Input voltage range, V_I (any input)	−16 to 16 V
Input current, I_I (each input)	±1 mA
Output current, I_O	±40 mA
Total current into V_{CC+}	60 mA
Total current out of V_{CC-}	60 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−40°C to 150°C
Storage temperature range	−65°C to 165°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} when dual supplies are specified (e.g., $V_{CC\pm} = \pm 15$ V) and with respect to V_{CC-} when a single supply is specified (e.g., $V_{CC} = 5$ V).
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if input is brought below V_{CC}.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 100°C$ POWER RATING	$T_A = 125°C$ POWER RATING	$T_A = 150°C$ POWER RATING
D	1064 mW	7.6 mW/°C	722 mW	494 mW	304 mW	114 mW
N	1764 mW	12.6 mW/°C	1197 mW	819 mW	504 mW	189 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±2	±15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 2.5$ V	−2.5	0.5	V
	$V_{CC\pm} = \pm 15$ V	−15	13	
Input voltage range, V_I	$V_{CC\pm} = \pm 2.5$ V	−2.5	0.5	V
	$V_{CC\pm} = \pm 15$ V	−15	13	
Operating free-air temperature, T_A		−40	150	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL2829Z			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω	25°C		3	7	mV
			Full range			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		15		µV/°C
I_{IO}	Input offset current		25°C		2.0	30	nA
			Full range			200	
I_{IB}	Input bias current		25°C		−12	−100	nA
			Full range			−500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	0 to 3.5		V
			Full range	0 to 3			
V_{OH}	High-level output voltage	I_{OH} = 0.1 mA	25°C	3.3	3.7		V
			Full range	3.2			
		I_{OH} = 1 mA	25°C	3.3	3.6		
			Full range	3.2			
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA	25°C	0.8	0.6		V
			Full range	1			
		I_{OL} = 1 mA	25°C	0.9	0.7		
			Full range	1.1			
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 3.5 V, R_L = 2 kΩ	25°C	25	60		V/mV
			Full range	0.8			
CMRR	Common-mode rejection ratio	V_O = 1.4 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	81		dB
			Full range	50			
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_L = 10 kΩ	25°C	65	103		dB
			Full range	65			
I_{CC}	Supply current (total package)	V_O = 2.5 V, V_{IC} = 0, No load	25°C		0.6	1.2	mA
			Full range			1.2	
ΔI_{CC}	Supply current change over operating temperature range		Full range		140		µA

† Full range is −40°C to 150°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL2829Z			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$,	25°C		3	7	mV
			Full range			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		15		µV/°C
I_{IO}	Input offset current		25°C		2	30	nA
			Full range			200	
I_{IB}	Input bias current		25°C		−15	−100	nA
			Full range			−500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−15 to 13.5			V
			Full range	−15 to 13			
V_{OM+}	Maximum positive peak output voltage range	$I_O = -0.1$ mA	25°C	13.2	14.1		V
			Full range	13.1			
		$I_O = -1$ mA	25°C	13.1	14		
			Full range	13			
		$I_O = -10$ mA	25°C	12.8	13.6		
			Full range	12.7			
V_{OM-}	Maximum negative peak output voltage range	$I_O = 0.1$ mA	25°C	−13.7	−14.4		V
			Full range	−13.1			
		$I_O = 1$ mA	25°C	−13	−14.3		
			Full range	−13			
		$I_O = 10$ mA	25°C	−12.9	−13.8		
			Full range	−12.9			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, $V_O = -5$ V to 5 V	25°C	25	210		V/mV
			Full range	5			
CMRR	Common-mode rejection ratio	$V_O = 1.4$ V, $V_{IC} = V_{ICR}min$, $R_S = 50\ \Omega$,	25°C	65	75		dB
			Full range	50			
k_{SVR}	Supply-voltage rejection ratio	$V_{CC} = 5$ V to 30 V, $V_O = 1.4$ V, $R_L = 10\ k\Omega$,,	25°C	65	103		dB
			Full range	65			
I_{CC}	Supply current (total package)	$V_O = 0$, $V_{IC} = 0$, No load	25°C		0.8	3	mA
			Full range			3	
ΔI_{CC}	Supply current change over operating temperature range		Full range		140		µA

† Full range is −40°C to 150°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL2829Z			UNIT
				MIN	TYP	MAX	
SR+	Positive slew rate	V_O = 1 V to 4.5 V, A_{VD} = 1, R_L = 2 kΩ‡ C_L = 100 pF	25°C	0.2			V/µs
			Full range	0.1			
SR–	Negative slew rate		25°C	0.25			
			Full range	0.2			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		39		nV/√Hz
		f = 10 kHz	25°C		23		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		0.9		µV
B_n	Unity-gain bandwidth	R_L = 10 kΩ‡, C_L = 100 pF	25°C		400		kHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF	25°C		60°		

† Full range is −40°C to 150°C.
‡ R_L terminates at 0 V.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL2829Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S= 50 Ω		3	7	mV
I_{IO}	Input offset current			2	30	nA
I_{IB}	Input bias current			−15	−100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	−15 to 13.5			V
V_{OM+}	Maximum positive peak output voltage range	I_O = −0.1 mA	13.2	14.1		V
		I_O = −1 mA	13.1	14		
		I_O = −10 mA	12.8	13.6		
V_{OM-}	Maximum negative peak output voltage range	I_O = 0.1 mA	−13.7	−14.4		V
		I_O = 1 mA	−13.6	−14.3		
		I_O = 10 mA	−12.9	−13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to −1.5 V, R_L = 2 kΩ	25	210		V/mV
CMRR	Common-mode rejection ratio	V_O = 1.4 V, V_{IC} = 0 V to 28 V, R_S = 50 Ω	65	75		dB
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_L = 10 kΩ	65	103		dB
I_{CC}	Supply current (total package)	V_O = 0, V_{IC} = 0, No load		0.8	3	mA

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IO}	Input offset current	vs Free-air temperature	1
I_{IB}	Input bias current	vs Free-air temperature ($V_{CC} = \pm 2.5$ V)	2
		vs Free-air temperature ($V_{CC} = \pm 15$ V)	3
V_{OM+}	Maximum positive peak output voltage swing	vs Free-air temperature ($V_{CC} = \pm 2.5$ V)	4
		vs Free-air temperature ($V_{CC} = \pm 15$ V)	5
V_{OM-}	Maximum negative peak output voltage swing	vs Free-air temperature ($V_{CC} = \pm 2.5$ V)	6
		vs Free-air temperature ($V_{CC} = \pm 15$ V)	7
I_{OS}	Short-circuit output current	vs Free-air temperature ($V_{ID} = 1$ V)	8
		vs Free-air temperature ($V_{ID} = -1$ V)	9
A_{VD}	Differential voltage amplification	vs Free-air temperature	10
CMRR	Common-mode rejection ratio	vs Free-air temperature	11
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	12
I_{CC}	Supply current	vs Free-air temperature	13
SR+	Positive slew rate	vs Free-air temperature	14
SR–	Negative slew rate	vs Free-air temperature	15
	Equivalent input noise voltage	Over a 10-second period	16

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

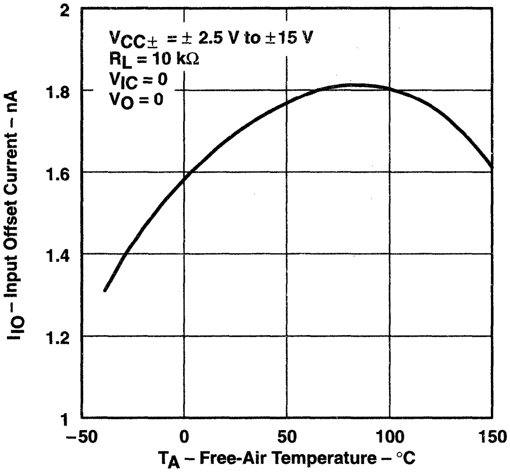


Figure 1

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

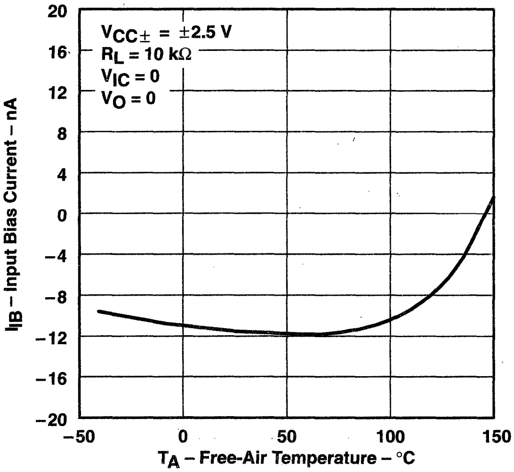


Figure 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

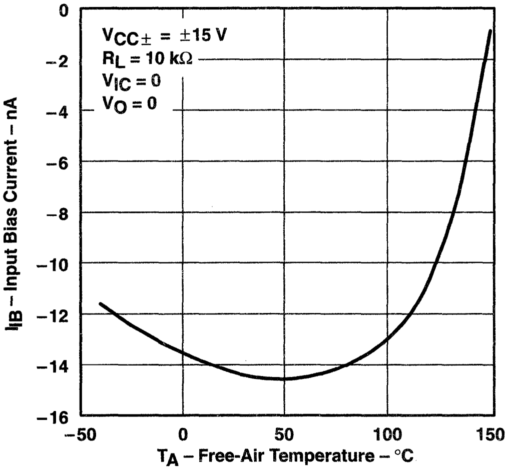


Figure 3

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

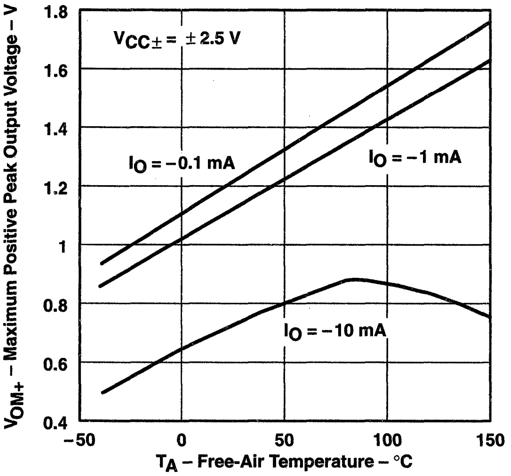


Figure 4

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

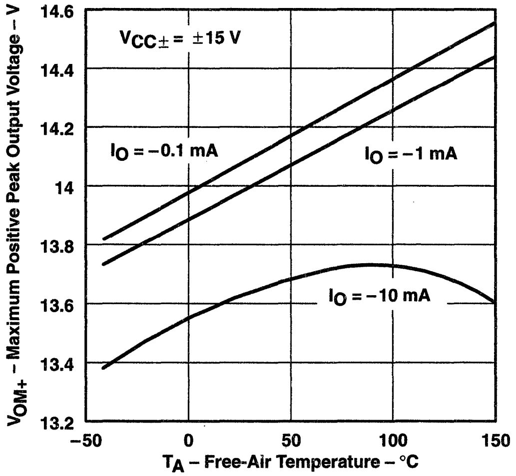


Figure 5

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

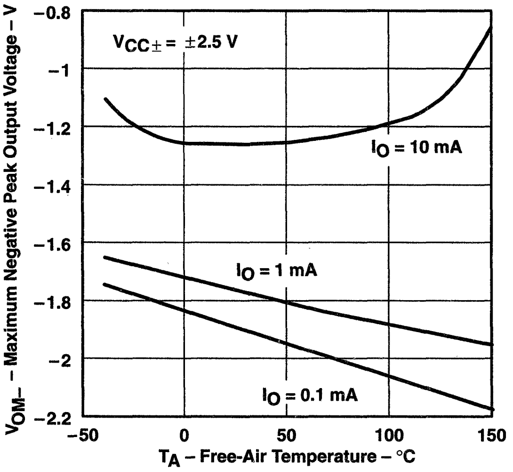


Figure 6

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

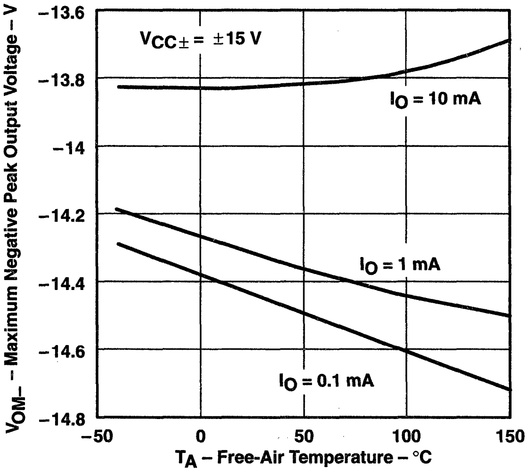


Figure 7

TYPICAL CHARACTERISTICS

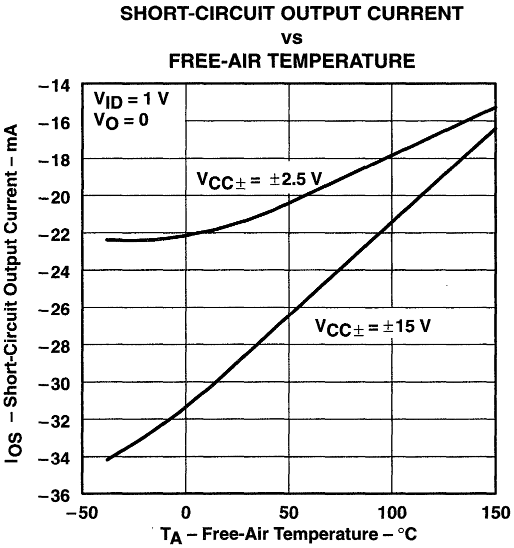


Figure 8

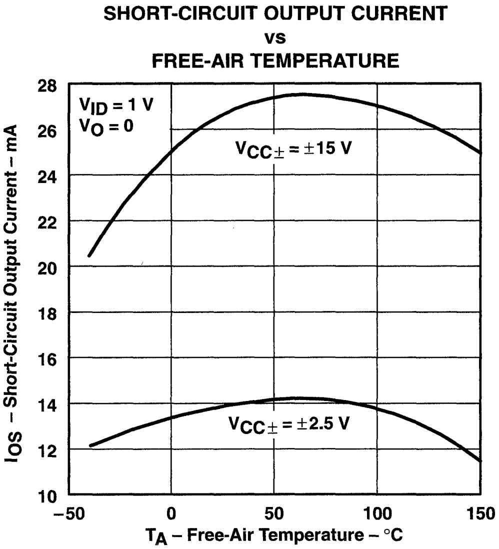


Figure 9

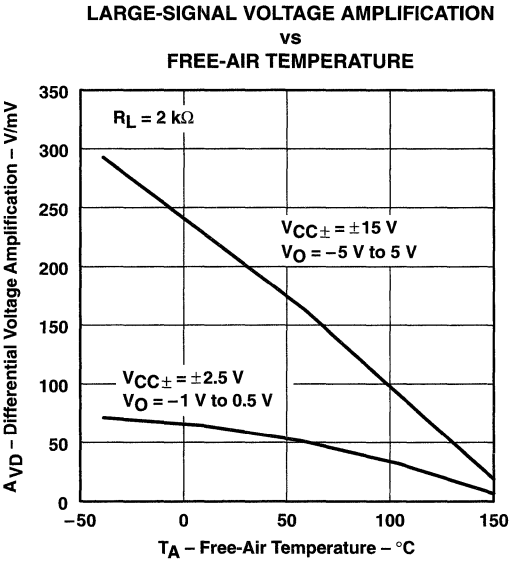


Figure 10

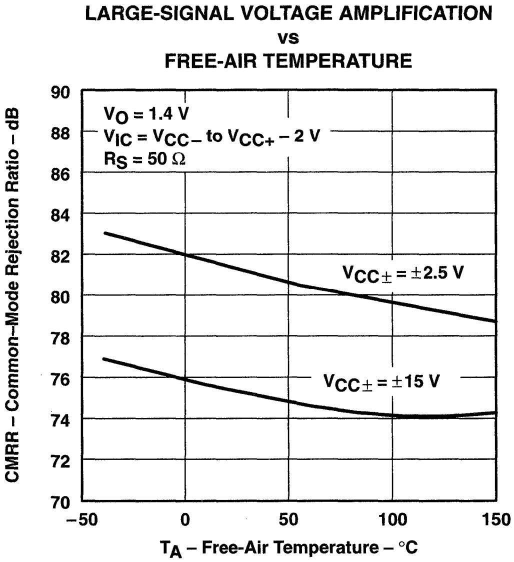


Figure 11

TYPICAL CHARACTERISTICS

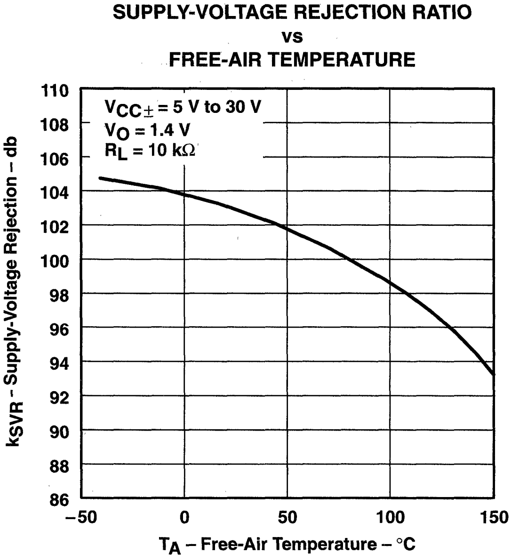


Figure 12

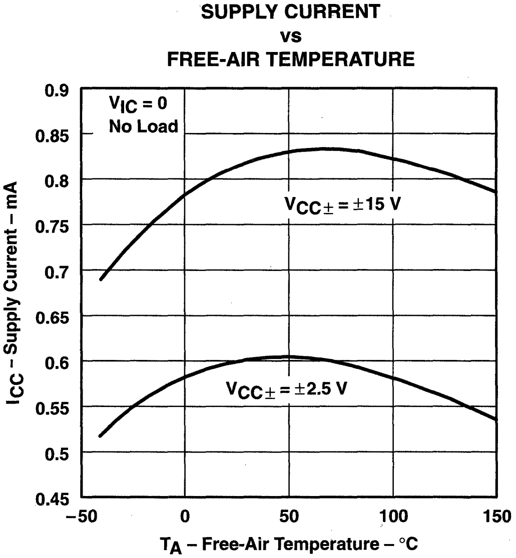


Figure 13

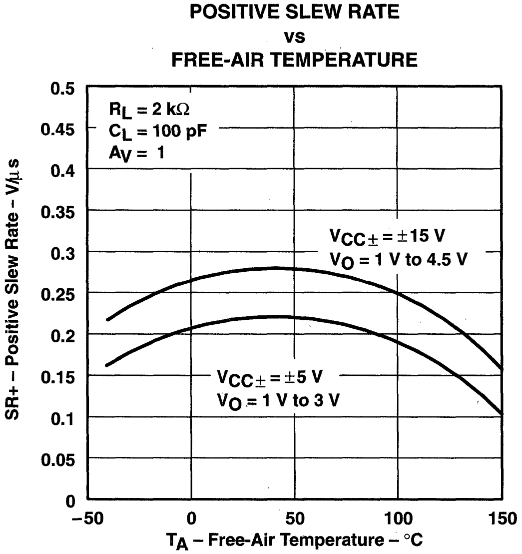


Figure 14

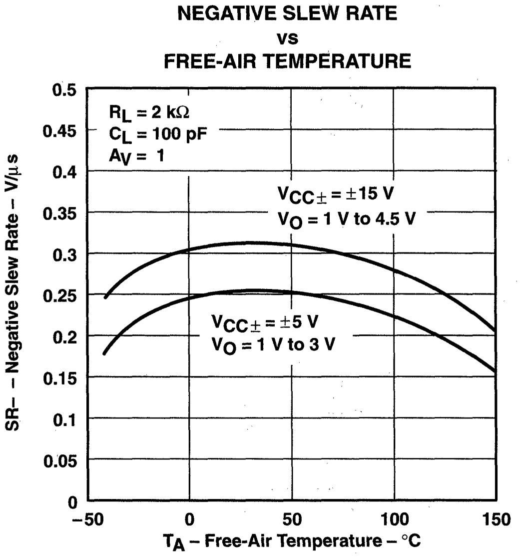


Figure 15

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

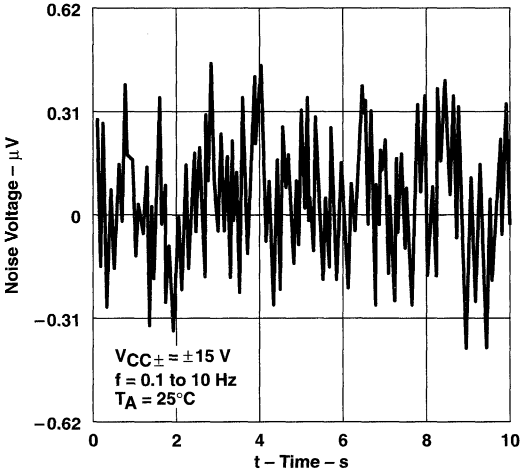


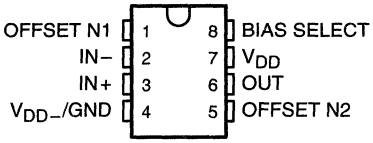
Figure 16

TLC251, TLC251A, TLC251B, TLC251Y
LinCMOS™ PROGRAMMABLE
LOW-POWER OPERATIONAL AMPLIFIERS

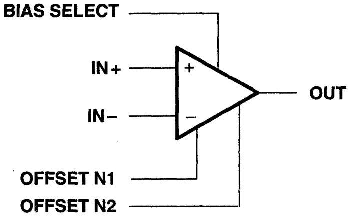
SLOS001E – JULY 1983 – REVISED AUGUST 1994

- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **Low Noise . . . 30 nV/√Hz Typ at 1 kHz (High Bias)**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833C, Method 3015.1**

D OR P PACKAGE
(TOP VIEW)



symbol



description

The TLC251C, TLC251AC, and TLC251BC are low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike traditional metal-gate CMOS operational amplifiers, these devices utilize Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages without sacrificing the advantages of metal-gate CMOS. This series of parts is available in selected grades of input offset voltage and can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this family is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels to suit the application. The series features operation down to a 1.4-V supply and is stable at unity gain.

These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC251C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC251C series.

In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption. The TLC251C series is well suited to solve the difficult problems associated with single battery and solar cell-powered applications.

The TLC251C series is characterized for operation from 0°C to 70°C.

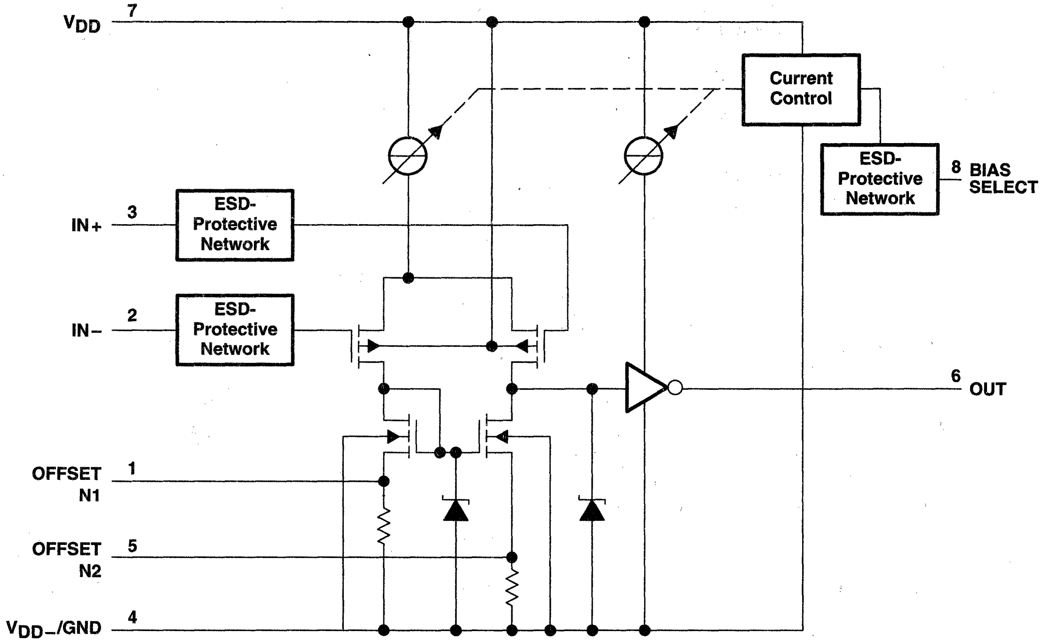
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	10 mV	TLC251CD	TLC251CP	TLC251Y
	5 mV	TLC251ACD	TLC251ACP	—
	2 mV	TLC251BCD	TLC251BCP	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC251CDR). Chips are tested at 25°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

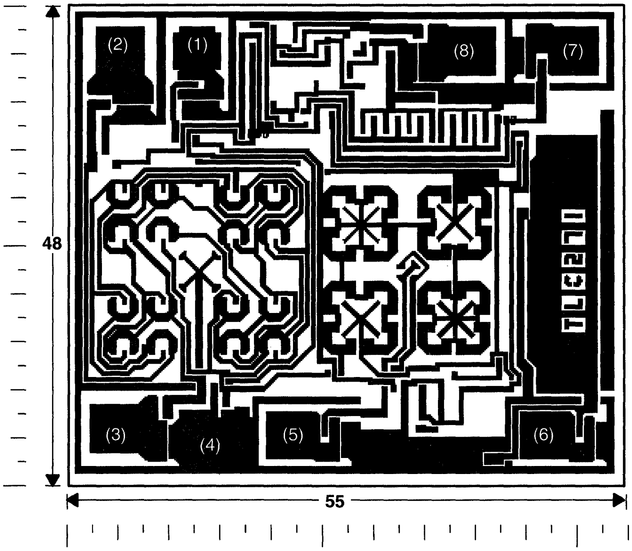
schematic

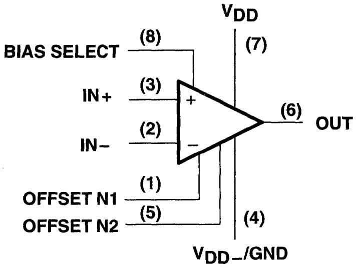

VDD
7
Current Control
ESD-Protective Network
8
BIAS SELECT
IN+
3
ESD-Protective Network
IN−
2
ESD-Protective Network
6
OUT
OFFSET N1
1
OFFSET N2
5
VDD−/GND
4

TLC251Y chip information

These chips, properly assembled, display characteristics similar to the TLC251C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) .... 18 V
Differential input voltage, V_{ID} (see Note 2) .... ±18 V
Input voltage range, V_I (any input) .... −0.3 V to 18 V
Duration of short circuit at (or below) 25°C free-air temperature (see Note 3) .... unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		1.4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0	0.2	V
	V_{DD} = 5 V	−0.2	4	
	V_{DD} = 10 V	−0.2	9	
	V_{DD} = 16 V	−0.2	14	
Operating free-air temperature, T_A		0	70	°C
Bias-select voltage		See Application Information		

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS	T_A†	TLC251C, TLC251AC, TLC251BC						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC251C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC251AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC251BC		25°C		0.34	2		0.39	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				0°C	3	3.8		7.8	8.5		
				70°C	3	3.8		7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
				0°C	4	27		7.5	42		
				70°C	4	20		7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
				0°C	60	84		60	88		
				70°C	60	85		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				0°C	60	94		60	94		
				70°C	60	96		60	96		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		675	1600		950	2000	μA
				0°C		775	1800		1125	2200	
				70°C		575	1300		750	1700	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC251C, TLC251AC, TLC251BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω		25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ		25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC251C, TLC251AC, TLC251BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			$V_{I(PP)}$ = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω		25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ		25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		49°		
				0°C		50°		
				70°C		46°		

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS	T_A†	TLC251C, TLC251AC, TLC251BC						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC251C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC251AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC251BC		25°C		0.34	2		0.39	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.9		8	8.7		V
				0°C	3	3.9		7.8	8.7		
				70°C	3	4		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	25	170		25	275		V/mV
				0°C	15	200		15	320		
				70°C	15	140		15	230		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	91		65	94		dB
				0°C	60	91		60	94		
				70°C	60	92		60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				0°C	60	92		60	92		
				70°C	60	94		60	94		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)} = V_{DD}/2$	25°C		−130			−160		nA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		105	280		143	300	µA
				0°C		125	320		173	400	
				70°C		85	220		110	280	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC251C, TLC251AC, TLC251BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		0.43		V/µs
				0°C		0.46		
				70°C		0.36		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω		25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ		25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		525		kHz
				0°C		600		
				70°C		400		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC251C, TLC251AC, TLC251BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		0.62		V/µs
				0°C		0.67		
				70°C		0.51		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω		25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ		25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		43°		
				0°C		44°		
				70°C		42°		

LOW-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS	T_A†	TLC251C, TLC251AC, TLC251BC						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC251C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC251AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC251BC		25°C		0.24	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				0°C	3	4.1		7.8	8.9		
				70°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
				0°C	50	700		50	1030		
				70°C	50	380		50	660		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	94		65	97		dB
				0°C	60	95		60	97		
				70°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				0°C	60	97		60	97		
				70°C	60	98		60	98		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		10	17		14	23	μA
				0°C		12	21		18	33	
				70°C		8	14		11	20	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC251C, TLC251AC, TLC251BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ		25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC251C, TLC251AC, TLC251BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ		25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		38°		
				0°C		40°		
				70°C		34°		

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V

PARAMETER			TEST CONDITIONS†	T_A‡	BIAS	TLC251C, TLC251AC, TLC251BC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC251C	V_O = 0.2 V, R_S = 50 Ω	25°C	Any			10	mV
				Full range				12	
		TLC251AC		25°C	Any			5	
				Full range				6.5	
		TLC251BC		25°C	Any			2	
				Full range				3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	Any		1		µV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C	Any		1		pA
				Full range				300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C	Any		1		pA
				Full range				600	
V_{ICR}	Common-mode input voltage range			25°C	Any	0 to 0.2			V
V_{OM}	Peak output voltage swing§		V_{ID} = 100 mV	25°C	Any	450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C	Low		20		
					High		10		
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_O = 0.2 V, $V_{IC} = V_{ICR}$min	25°C	Any	60	77		dB
I_{DD}	Supply current		V_O = 0.2 V, No load	25°C	Low		5	17	µA
					High		150	190	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias, R_L = 1 MΩ, for medium bias, R_L = 100 kΩ, and for high bias, R_L = 10 kΩ.

‡ Full range is 0°C to 70°C.

§ The output swings to the potential of V_{DD-}/GND.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	BIAS	TLC251C, TLC251AC, TLC251BC			UNIT
				MIN	TYP	MAX	
B_1	Unity-gain bandwidth	C_L = 100 pF	Low		12		kHz
			High		12		
SR	Slew rate at unity gain	See Figure 1	Low		0.001		V/µs
			High		0.1		
	Overshoot factor	See Figure 1	Low		35%		
			High		30%		

electrical characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC251Y									UNIT
			HIGH-BIAS MODE			MEDIUM-BIAS MODE			LOW-BIAS MODE			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L†		1.1	10		1.1	10		1.1	10	mV
α_{VIO}	Average temperature coefficient of input offset voltage			1.8			1.7			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$		0.1			0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$		0.6			0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L†	3.2	3.8		3.2	3.9		3.2	4.1		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0		0	50		0	50		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V, R_L†	5	23		25	170		50	480		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$	65	80		65	91		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	65	95		70	93		70	97		dB
$I_{I(SEL)}$	Input current (BIAS SELECT)	$V_{I(SEL)} = V_{DD}/2$		−1.4			−0.13			0.065		μA
I_{DD}	Supply current	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load		675	1600		105	280		10	17	μA

† For high-bias mode, R_L = 10 kΩ; for medium-bias mode, R_L = 100 kΩ; and for low-bias mode, R_L = 1 MΩ.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC251Y									UNIT
				HIGH-BIAS MODE			MEDIUM-BIAS MODE			LOW-BIAS MODE			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L†, C_L = 20 pF	$V_{I(PP)}$ = 1 V		3.6			0.43			0.03		V/μs
			$V_{I(PP)}$ = 2.5 V		2.9			0.40			0.03		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω		25			32			68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ	C_L = 20 pF,		320			55			4.5		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF		1700			525			65		kHz
ϕ_m	Phase margin	f = B_1, C_L = 20 pF	V_I = 10 mV,		46°			40°			34°		

† For high-bias mode, R_L = 10 kΩ; for medium-bias mode, R_L = 100 kΩ; and for low-bias mode, R_L = 1 MΩ.

PARAMETER MEASUREMENT INFORMATION

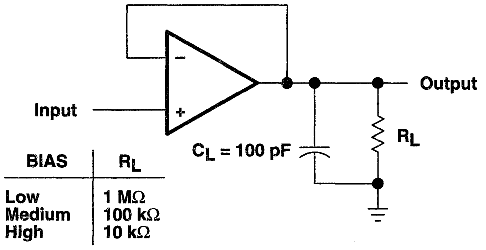


Figure 1. Unity-Gain Amplifier

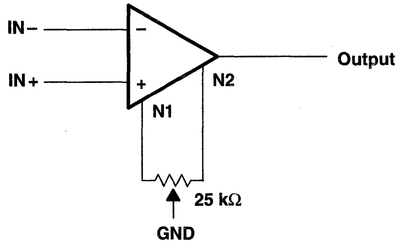


Figure 2. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

				FIGURE
I_{DD}	Supply current		vs Bias-select voltage vs Supply voltage vs Free-air temperature	3 4 5
A_{VD}	Large-signal differential voltage amplification	Low bias	vs Frequency	6
		Medium bias	vs Frequency	7
		High bias	vs Frequency	8
	Phase shift	Low bias	vs Frequency	6
		Medium bias	vs Frequency	7
		High bias	vs Frequency	8

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
BIAS-SELECT VOLTAGE

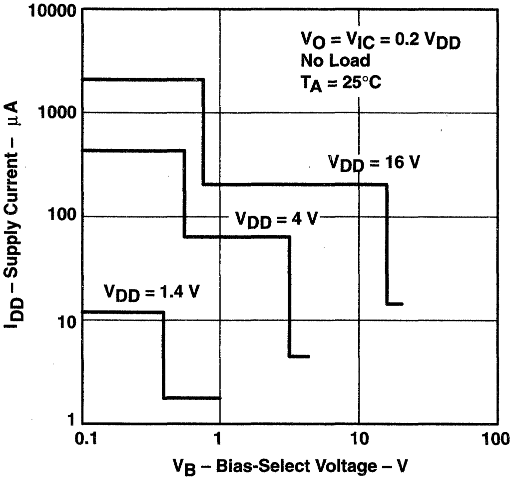


Figure 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

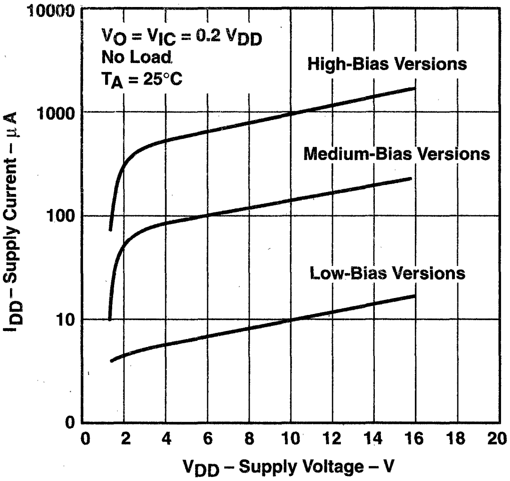


Figure 4

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

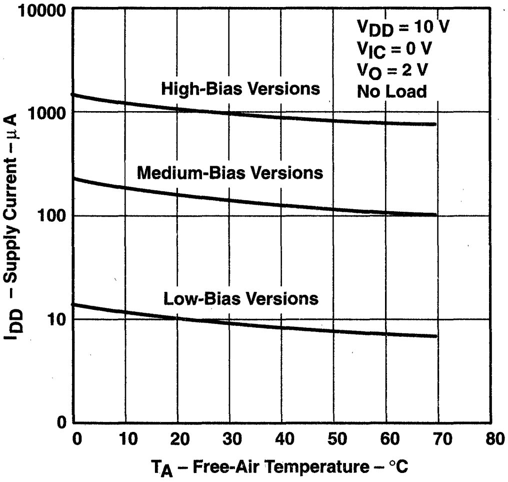


Figure 5

TYPICAL CHARACTERISTICS

LOW-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

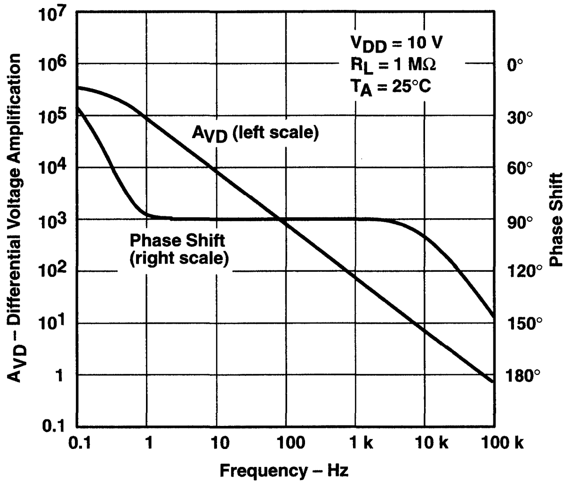


Figure 6

MEDIUM-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

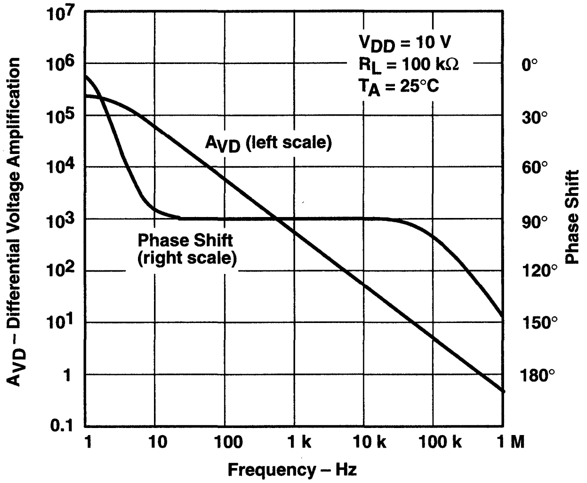


Figure 7

TYPICAL CHARACTERISTICS

HIGH-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

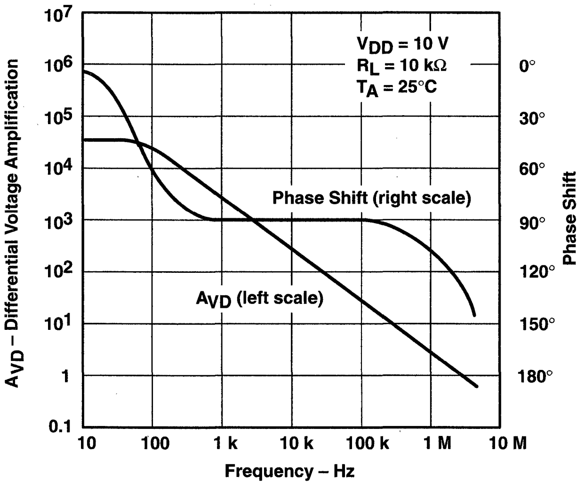


Figure 8

APPLICATION INFORMATION

latch-up avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the operational amplifier supplies should be applied simultaneously with, or before, application of any input signals.

APPLICATION INFORMATION

using BIAS SELECT

The TLC251 has a terminal called BIAS SELECT that allows the selection of one of three I_{DD} conditions (10, 150, and 1000 µA typical). This allows the user to trade-off power and ac performance. As shown in the typical supply current (I_{DD}) versus supply voltage (V_{DD}) curves (Figure 4), the I_{DD} varies only slightly from 4 V to 16 V. Below 4 V, the I_{DD} varies more significantly. Note that the I_{DD} values in the medium- and low-bias modes at V_{DD} = 1.4 V are typically 2 µA, and in the high mode are typically 12 µA. The following table shows the recommended BIAS SELECT connections at V_{DD} = 10 V.

BIAS MODE	AC PERFORMANCE	BIAS SELECT CONNECTION†	TYPICAL I_{DD}‡
Low	Low	V_{DD}	10 µA
Medium	Medium	0.8 V to 9.2 V	150 µA
High	High	Ground pin	1000 µA

† Bias selection may also be controlled by external circuitry to conserve power, etc. For information regarding BIAS SELECT, see Figure 3 in the typical characteristics curves.

‡ For I_{DD} characteristics at voltages other than 10 V, see Figure 4 in the typical characteristics curves.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the potential of V_{DD-}/GND.

input offset nulling

The TLC251C series offers external offset null control. Nulling may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected to the device V_{DD-}/GND pin as shown in Figure 2. The amount of nulling range varies with the bias selection. At an I_{DD} setting of 1000 µA (high bias), the nulling range allows the maximum offset specified to be trimmed to zero. In low or medium bias or when the amplifier is used below 4 V, total nulling may not be possible for all units.

supply configurations

Even though the TLC251C series is characterized for single-supply operation, it can be used effectively in a split-supply configuration when the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

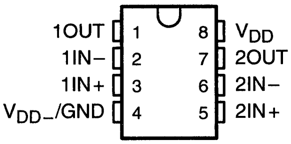
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

TLC252, TLC252A, TLC252B, TLC252Y, TLC25L2, TLC25L2A, TLC25L2B TLC25L2Y, TLC25M2, TLC25M2A, TLC25M2B, TLC25M2Y LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

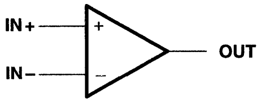
SLOS002G – JUNE 1983 – REVISED AUGUST 1996

- **A-Suffix Versions Offer 5-mV V_{IO}**
- **B-Suffix Versions Offer 2-mV V_{IO}**
- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 30 nV/√Hz Typ at f = 1 kHz (High-Bias Versions)**

D OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The TLC252, TLC25L2, and TLC25M2 are low-cost, low-power dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	10 mV 5 mV 2 mV	TLC252CD TLC252ACD TLC252BCD	TLC252CP TLC252ACP TLC252BCP	TLC252Y — —
	10 mV 5 mV 2 mV	TLC25L2CD TLC25L2ACD TLC25L2BCD	TLC25L2CP TLC25L2ACP TLC25L2BCP	TLC25L2Y — —
	10 mV 5 mV 2 mV	TLC25M2CD TLC25M2ACD TLC25M2BCD	TLC25M2CP TLC25M2ACP TLC25M2BCP	TLC25M2Y — —

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC252CDR). Chips are tested at 25°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

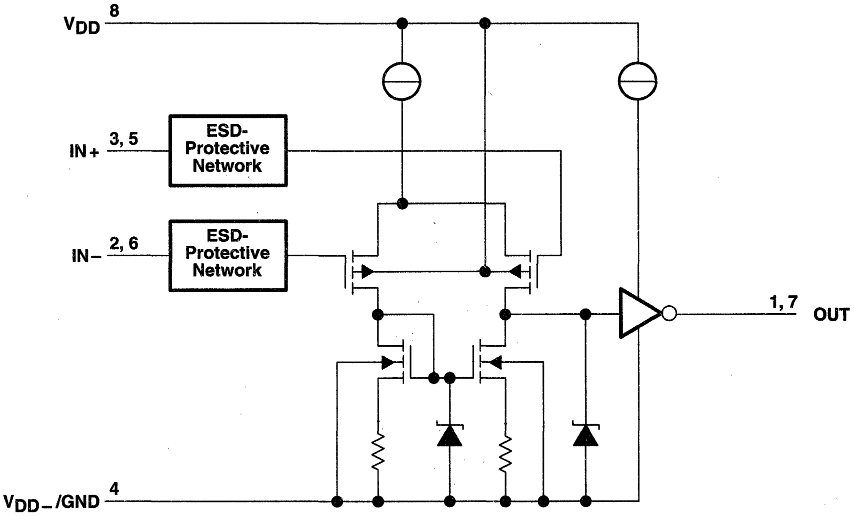
TEXAS INSTRUMENTS

description (continued)

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC252/25_2 series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC252/25_2 series devices. Remote and inaccessible equipment applications are possible using their low-voltage and low-power capabilities. The TLC252/25_2 series is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 8-pin plastic dip and the small-outline package. The device is also available in chip form.

The TLC252/25_2 series is characterized for operation from 0°C to 70°C.

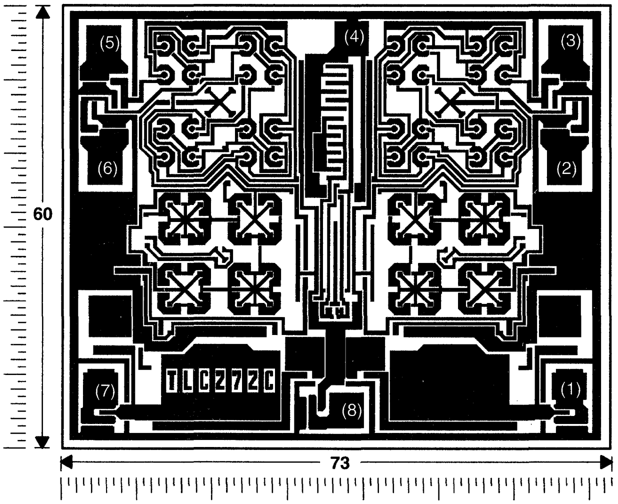
equivalent schematic (each amplifier)

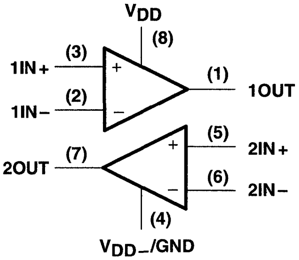


TLC252Y, TLC25L2Y, and TLC25M2Y chip information

These chips, properly assembled, display characteristics similar to the TLC252/25_2. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . ±18 V
Input voltage range, V_I (any input) . . . . −0.3 V to 18 V
Duration of short circuit at (or below) 25°C free-air temperature (see Note 3) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND.
2. Differential voltages are at IN+, with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		1.4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0	0.2	V
	V_{DD} = 5 V	−0.2	4	
	V_{DD} = 10 V	−0.2	9	
	V_{DD} = 16 V	−0.2	14	
Operating free-air temperature, T_A		0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_2C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_2BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	450	700		450	700		450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, $V_{IC} = V_{ICR}min$	25°C	60	77		60	77		60	77		dB
I_{DD}	Supply current		V_O = 0.2 V, No load	25°C		300	375		25	34		200	250	μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡ The output swings to the potential of V_{DD-}/GND.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		12			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.1			0.001			0.01		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC252C, TLC252AC, TLC252BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC252C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC252AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC252BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.23	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				0°C	3	3.8		
				70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				0°C	4	27		
				70°C	4	20		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		dB
				0°C	60	84		
				70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{DD}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		1.4	3.2	mA
				0°C		1.6	3.6	
				70°C		1.2	2.6	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC252C, TLC252AC, TLC252BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC252C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC252AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC252BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.29	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				0°C	8	8.5		
				70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				0°C	7.5	42		
				70°C	7.5	32		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	85		dB
				0°C	60	88		
				70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{DD}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		1.9	4	mA
				0°C		2.3	4.4	
				70°C		1.6	3.4	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC252C, TLC252AC, TLC252BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure		25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		46°		
				0°C		47°		
				70°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC252C, TLC252AC, TLC252BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			$V_{I(PP)}$ = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		49°		
				0°C		50°		
				70°C		46°		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC25L2C TLC25L2AC TLC25L2BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC252C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC252AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC252BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.204	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				0°C	3	4.1		
				70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	700		V/mV
				0°C	50	700		
				70°C	50	380		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	94		dB
				0°C	60	95		
				70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		20	34	μA
				0°C		24	42	
				70°C		16	28	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC25L2C TLC25L2AC TLC25L2BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC252C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC252AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC252BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.235	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		8	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				0°C	7.8	8.9		
				70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	860		V/mV
				0°C	50	1025		
				70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	97		dB
				0°C	60	97		
				70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{DD}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		29	46	µA
				0°C		36	66	
				70°C		22	40	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC25L2C TLC25L2AC TLC25L2BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure		25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		MHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC25L2C TLC25L2AC TLC25L2BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		MHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		38°		
				0°C		40°		
				70°C		34°		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC25M2C TLC25M2AC TLC25M2BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC252C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC252AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC252BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.22	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				0°C	3	3.9		
				70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				0°C	15	200		
				70°C	15	140		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	91		dB
				0°C	60	91		
				70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{DD}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		
				70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		210	560	μA
				0°C		250	640	
				70°C		170	440	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC25M2C TLC25M2AC TLC25M2BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC252C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC252AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC252BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.224	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				0°C	7.8	8.7		
				70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				0°C	15	320		
				70°C	15	230		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	94		dB
				0°C	60	94		
				70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{DD}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		
				70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		285	600	μA
				0°C		345	800	
				70°C		220	560	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC25M2C TLC25M2AC TLC25M2BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.43		V/µs
				0°C		0.46		
				70°C		0.36		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure		25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		MHz
				0°C		600		
				70°C		400		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC25M2C TLC25M2AC TLC25M2BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.62		V/µs
				0°C		0.67		
				70°C		0.51		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		MHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		43°		
				0°C		44°		
				70°C		42°		

electrical characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252Y			TLC25L2Y			TLC25M2Y			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, See Note 6		1.1	10		1.1	10		1.1	10	mV
α_{VIO}	Average temperature coefficient of input offset voltage			1.8			1.1			1.7		µV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$		0.1			0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$		0.6			0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, See Note 6	3.2	3.8		3.2	4.1		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0		0	50		0	50		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V, See Note 6	5	23		50	700		25	170		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$	65	80		65	94		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	65	95		70	97		70	93		dB
I_{DD}	Supply current	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load		1.4	3.2		0.02	0.034		0.21	0.56	mA

operating characteristics, V_{DD} = 5 V, T_A = 25°C

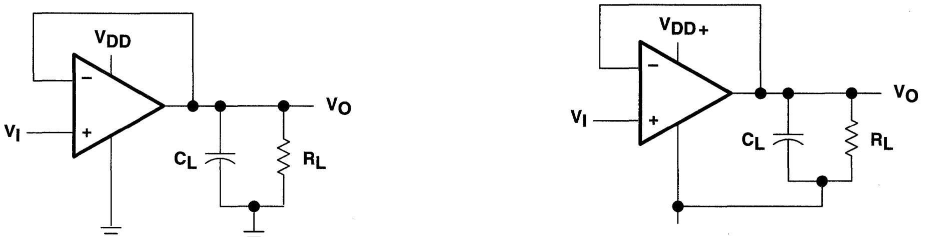
PARAMETER		TEST CONDITIONS		TLC252Y			TLC25L2Y			TLC25M2Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Slew rate at unity gain	C_L = 20 pF, See Note 6	$V_{I(PP)}$ = 1 V		3.6			0.03			0.43		V/µs
			$V_{I(PP)}$ = 2.5 V		2.9			0.03			0.40		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω		2.5			68			32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ	C_L = 20 pF,		320			5			55		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF		1.7			0.085			0.525		MHz
ϕ_m	Phase margin	$f = B_1$, C_L = 20 pF	V_I = 10 mV,		46°			34°			40°		

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. For low-bias mode, R_L = 1 MΩ; for medium-bias mode, R_L = 100 kΩ, and for high-bias mode, R_L = 10 kΩ.

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

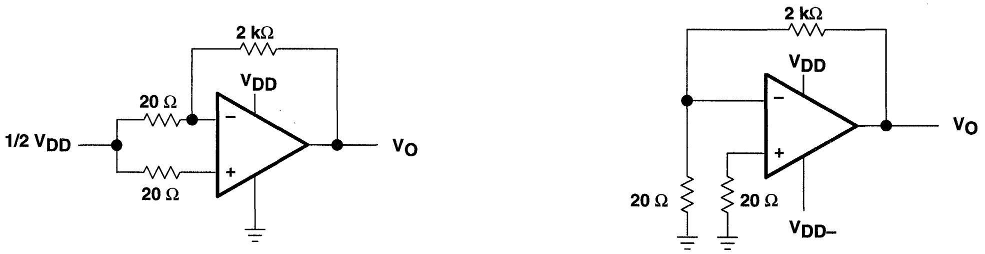
Because the TLC252, TLC25L2, and TLC25M2 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

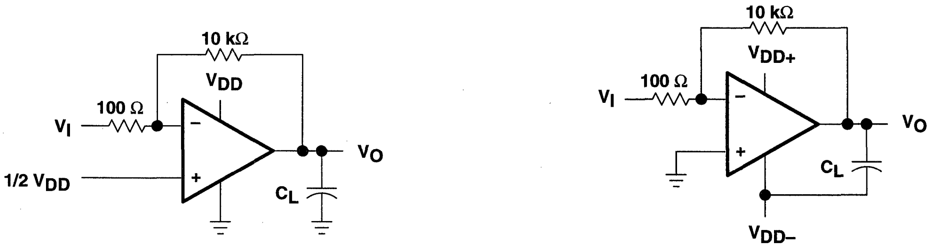
Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY

(a) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY

(a) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

TYPICAL CHARACTERISTICS

Table of Graphs

				FIGURE
I_{DD}	Supply current		vs Supply voltage vs Free-air temperature	4 5
A_{VD}	Large-signal differential voltage amplification	Low bias	vs Frequency	6
		Medium bias	vs Frequency	7
		High bias	vs Frequency	8
	Phase shift	Low bias	vs Frequency	6
		Medium bias	vs Frequency	7
		High bias	vs Frequency	8

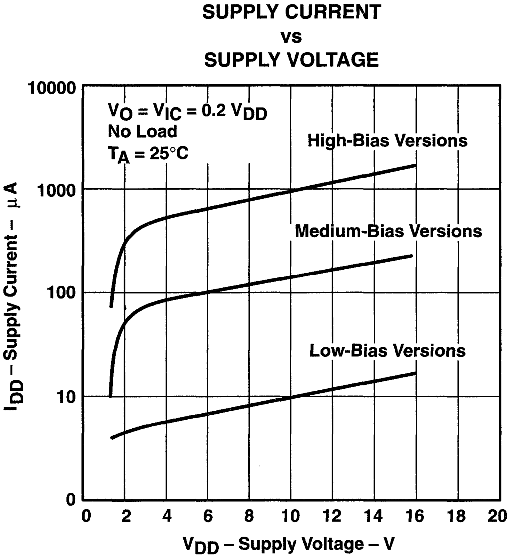


Figure 4

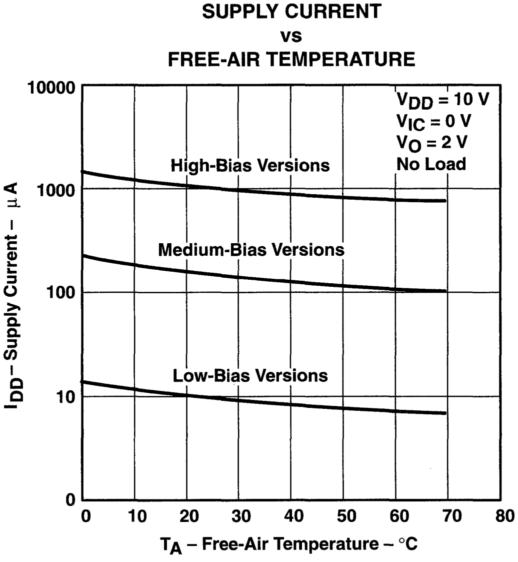


Figure 5

TYPICAL CHARACTERISTICS

LOW-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

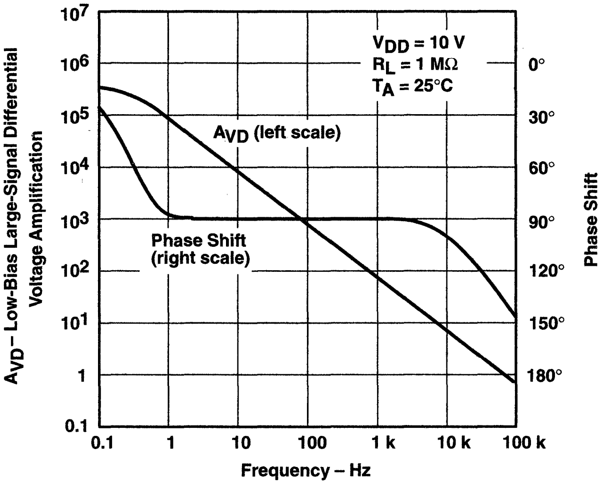


Figure 6

MEDIUM-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

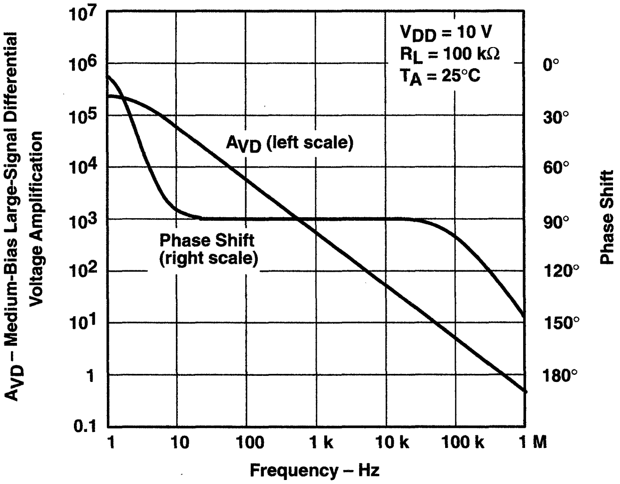


Figure 7

TYPICAL CHARACTERISTICS

HIGH-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

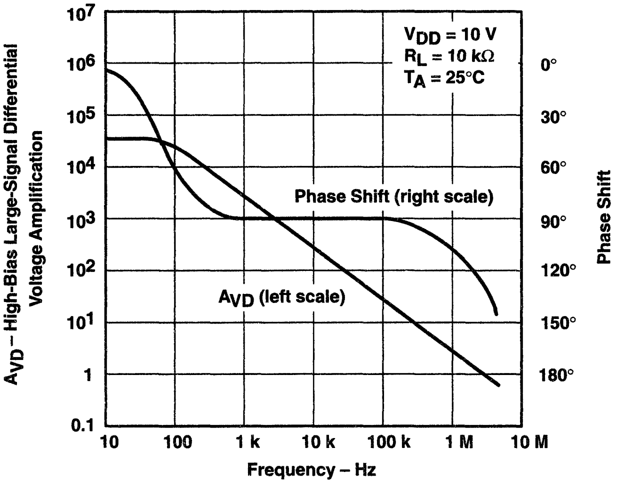


Figure 8

APPLICATION INFORMATION

latch-up avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the operational amplifier supplies should be applied simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the potential of V_{DD-}/GND.

supply configurations

Even though the TLC252/25_2C series is characterized for single-supply operation, it can be used effectively in a split-supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

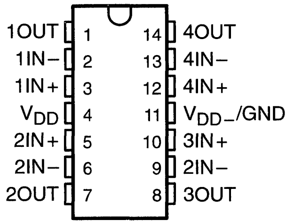
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

SLOS003F – JUNE 1983 – REVISED AUGUST 1994

- **A-Suffix Versions Offer 5-mV V_{IO}**
- **B-Suffix Versions Offer 2-mV V_{IO}**
- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 25 nV/√Hz Typ at f = 1 kHz (High-Bias Version)**

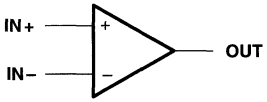
D, N, OR PW PACKAGE
(TOP VIEW)



description

The TLC254, TLC254A, TLC254B, TLC25L4, TLC254L4A, TLC254L4B, TLC25M4, TLC25M4A and TL25M4B are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input-offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

symbol (each amplifier)



These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for these devices include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS operational amplifiers without the power penalties of traditional bipolar devices.

Available options

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	10 mV	TLC254CD	TLC254CN	TLC254CPW	TLC254Y
	5 mV	TLC254ACD	TLC254ACN	—	—
	2 mV	TLC254BCD	TLC254BCN	—	—
	10 mV	TLC25L4CD	TLC25L4CN	TLC25L4CPW	TLC25L4Y
	5 mV	TLC25L4ACD	TLC25L4ACN	—	—
	2 mV	TLC25L2BCD	TLC25L4BCN	—	—
	10 mV	TLC25M4CD	TLC25M4CN	TLC25M4CPW	TLC25M4Y
	5 mV	TLC25M4ACD	TLC25M4ACN	—	—
	2 mV	TLC25M4BCD	TLC25M4BCN	—	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC254CDR). Chips are tested at 25°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with these devices. Remote and inaccessible equipment applications are possible using their low-voltage and low-power capabilities. These devices are well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 14-pin plastic dip and the small-outline packages. The device is also available in chip form.

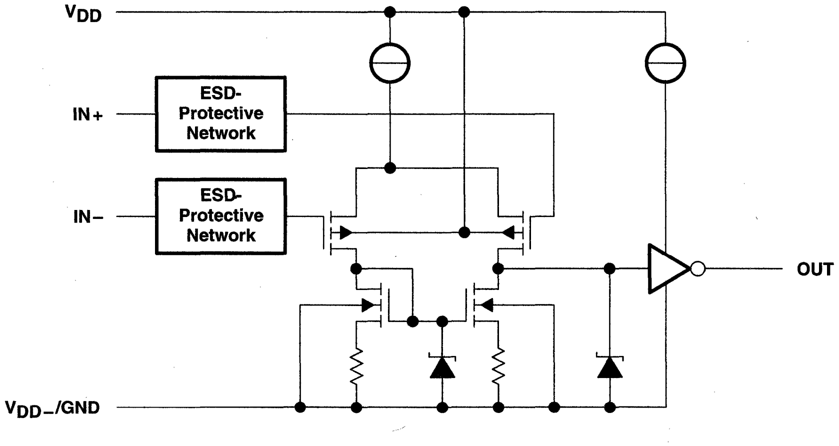
These devices are characterized for operation from 0°C to 70°C.

DEVICE FEATURES

PARAMETER	TLC25L4_C (LOW BIAS)	TLC25M4_C (MEDIUM BIAS)	TLC254_C (HIGH BIAS)
Supply current (Typ)	40 μA	600 μA	4000 μA
Slew rate (Typ)	0.04 V/μA	0.6 V/μA	4.5 V/μA
Input offset voltage (Max)			
TLC254C, TLC25L4C, TLC25M4C	10 mV	10 mV	10 mV
TLC254AC, TLC25L4AC, TLC25M4AC	5 mV	5 mV	5 mV
TLC254BC, TLC25L4BC, TLC25M4BC	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

† The long-term drift value applies after the first month.

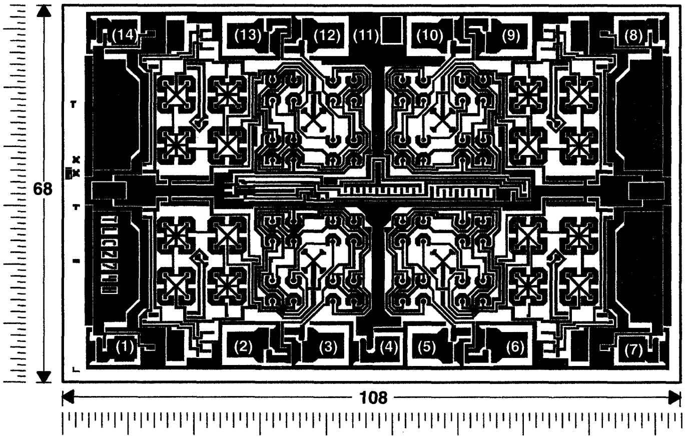
equivalent schematic (each amplifier)

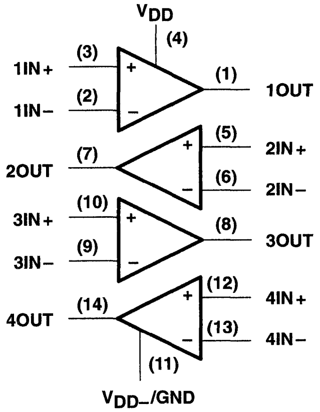


chip information

These chips, when properly assembled, display characteristics similar to the TLC25_4C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) .... 18 V
Differential input voltage (see Note 2) .... ±18 V
Input voltage range (any input) .... −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) .... unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature range .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND.
2. Differential voltages are at IN+, with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
N	1050 mW	9.2 mW/°C	736 mW
PW	700 mW	5.6 mW/°C	448 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		1.4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0	0.2	V
	V_{DD} = 5 V	−0.2	4	
	V_{DD} = 10 V	−0.2	9	
	V_{DD} = 16 V	−0.2	14	
Operating free-air temperature, T_A		0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	T_A	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_4C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1			1			1		µV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	450	700		450	700		450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, $V_{IC} = V_{ICR}$min	25°C	60	77		60	77		60	77		dB
I_{DD}	Supply current		V_O = 0.2 V, No load	25°C		600	750		50	68		400	500	µA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: for low bias, R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡ The output swings to the potential of V_{DD-}/GND.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	See Figure 1			0.1			0.001			0.01		V/µs
B_1	Unity-gain bandwidth	A_V = 40 dB, R_S = 50 Ω,	C_L = 10 pF, See Figure 1		12			12			12		kHz
	Overshoot factor	See Figure 1			30%			35%			35%		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC254, TLC254AC, TLC254BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC254C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC254AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC254BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.34	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	0°C	3	3.8		V
				25°C	3.2	3.8		
				70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	0°C		0	50	mV
				25°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	0°C	4	27		V/mV
				25°C	5	23		
				70°C	4	20		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	0°C	60	84		dB
				25°C	65	80		
				70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	0°C	60	94		dB
				25°C	65	95		
				70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	0°C		3.1	7.2	mA
				25°C		2.7	6.4	
				70°C		2.3	5.2	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC254C, TLC254AC, TLC254BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC254C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC254AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC254BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.39	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	0°C	7.8	8.5		V
				25°C	8	8.5		
				70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	0°C		0	50	mV
				25°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	0°C	7.5	42		V/mV
				25°C	10	36		
				70°C	7.5	32		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	0°C	60	88		dB
				25°C	65	85		
				70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	0°C	60	94		dB
				25°C	65	95		
				70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	0°C		4.5	8.8	mA
				25°C		3.8	8	
				70°C		3.2	6.8	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC254C, TLC254AC, TLC254BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	0°C		4		V/μs
				25°C		3.6		
			$V_{I(PP)}$ = 1 V	70°C		3		
			$V_{I(PP)}$ = 2.5 V	0°C		3.1		
				25°C		2.9		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2		25°C		25		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		0°C		340		kHz
				25°C		320		
				70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 1		0°C		2		MHz
				25°C		1.7		
				70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		0°C		47°		
				25°C		46°		
				70°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC254C, TLC254AC, TLC254BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	0°C		5.9		V/μs
				25°C		5.3		
				70°C		4.3		
			$V_{I(PP)}$ = 5.5 V	0°C		5.1		
				25°C		4.6		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2		25°C		25		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		0°C		220		kHz
				25°C		200		
				70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 1		0°C		2.5		MHz
				25°C		2.2		
				70°C		1.8		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		0°C		50°		
				25°C		49°		
				70°C		46°		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25L4C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC25L4AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC25L4BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.24	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	0°C	3	4.1		V
				25°C	3.2	4.1		
				70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	0°C		0	50	mV
				25°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	0°C	50	680		V/mV
				25°C	50	520		
				70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	0°C	60	95		dB
				25°C	65	94		
				70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	0°C	60	97		dB
				25°C	70	98		
				70°C	60	97		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	0°C		48	84	µA
				25°C		40	68	
				70°C		31	56	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25L4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC25L4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC25L4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.26	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	0°C	7.8	8.9		V
					25°C	8	8.9		
					70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	0°C		0	50	mV
					25°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	0°C	50	1025		V/mV
					25°C	50	870		
					70°C	50	660		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\min$		0°C	60	97		dB
					25°C	65	97		
					70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	0°C	60	97		dB
					25°C	70	97		
					70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	0°C		72	132	µA
					25°C		57	92	
					70°C		44	80	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	0°C		0.04		V/µs
				25°C		0.03		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	0°C		0.03		
				25°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2		25°C		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		0°C		6		kHz
				25°C		5		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 1		0°C		100		kHz
				25°C		85		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		0°C		36°		
				25°C		34°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	0°C		0.05		V/µs
				25°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	0°C		0.05		
				25°C		0.04		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2		25°C		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		0°C		1.3		kHz
				25°C		1		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 1		0°C		125		kHz
				25°C		110		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		0°C		40°		
				25°C		38°		
				70°C		34°		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25M4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC25M4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC25M4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.25	2	
					Full range			3	
∝VIO	Average temperature coefficient of input offset voltage				25°C to 70°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 t0 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	0°C	3	3.9		V
					25°C	3.2	3.9		
					70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	0°C		0	50	mV
					25°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	0°C	15	200		V/mV
					25°C	25	170		
					70°C	15	140		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min		0°C	60	91		dB
					25°C	65	91		
					70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	0°C	60	92		dB
					25°C	70	93		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	0°C		500	1280	µA
					25°C		420	1120	
					70°C		340	880	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25M4C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC25M4AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC25M4BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.26	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	0°C	7.8	8.7		V
				25°C	8	8.7		
				70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	0°C		0	50	mV
				25°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	0°C	15	320		V/mV
				25°C	25	275		
				70°C	15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	0°C	60	94		dB
				25°C	65	94		
				70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	0°C	60	92		dB
				25°C	70	93		
				70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	0°C		690	1600	μA
				25°C		570	1200	
				70°C		440	1120	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, $V_{DD} = 5$ V

PARAMETER		TEST CONDITIONS		T_A	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 100$ kΩ, $C_L = 20$ pF, See Figure 1	$V_{I(PP)} = 1$ V	0°C		0.46		V/µs
				25°C		0.43		V/µs
				70°C		0.36		V/µs
			$V_{I(PP)} = 2.5$ V	0°C		0.43		
				25°C		0.40		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 20\ \Omega$, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $C_L = 20$ pF, $R_L = 100$ kΩ, See Figure 1		0°C		60		kHz
				25°C		55		
				70°C		50		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $C_L = 20$ pF, See Figure 1		0°C		610		kHz
				25°C		525		
				70°C		400		
ϕ_m	Phase margin	$V_I = 10$ mV, $f = B_1$, $C_L = 20$ pF, See Figure 3		0°C		41°		
				25°C		40°		
				70°C		39°		

operating characteristics, $V_{DD} = 10$ V

PARAMETER		TEST CONDITIONS		T_A	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 100$ kΩ, $C_L = 20$ pF, See Figure 1	$V_{I(PP)} = 1$ V	0°C		0.67		V/µs
				25°C		0.62		
				70°C		0.51		
			$V_{I(PP)} = 5.5$ V	0°C		0.61		
				25°C		0.56		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 20\ \Omega$, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $C_L = 20$ pF, $R_L = 100$ kΩ, See Figure 1		0°C		40		kHz
				25°C		35		
				70°C		30		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, $C_L = 20$ pF, See Figure 1		0°C		710		kHz
				25°C		635		
				70°C		510		
ϕ_m	Phase margin	$V_I = 10$ mV, $f = B_1$, $C_L = 20$ pF, See Figure 3		0°C		44°		
				25°C		43°		
				70°C		42°		

electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC254Y			TLC25L4Y			TLC25M4Y			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, See Note 6		1.1	10		1.1	10		1.1	10	mV
α_{VIO}	Average temperature coefficient of input offset voltage			1.8			1.1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$		0.1			0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$		0.6			0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 100 kΩ	3.2	3.8		3.2	4.1		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0		0	50		0	50		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V, See Note 6	5	23		50	520		25	170		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	65	80		65	94		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	65	95		70	97		70	93		dB
I_{DD}	Supply current	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load		2.7	6.4		0.04	0.068		0.42	1.12	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. For low-bias mode, R_L = 1 MΩ, for medium-bias mode, R_L = 100 kΩ, and for high-bias mode, R_L = 10 kΩ.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

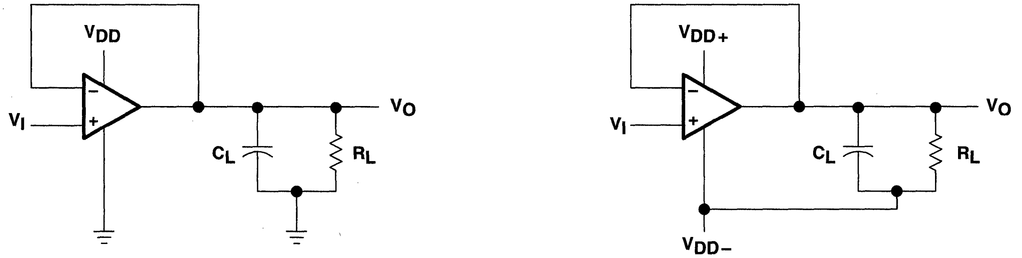
PARAMETER		TEST CONDITIONS		TLC254Y			TLC25L4Y			TLC25M4Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	C_L = 20 pF, See Note 6	$V_{I(PP)}$ = 1 V		3.6			0.03			0.43		V/μs
			$V_{I(PP)}$ = 2.5 V		2.9			0.03			0.40		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω		2.5			70			32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ	C_L = 20 pF,		320			5			55		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF		1.7			0.085			0.525		MHz
ϕ_m	Phase margin	f = B_1, C_L = 20 pF	V_I = 10 mV,		46°			34°			40°		

NOTE 6: For low-bias mode, R_L = 1 MΩ, for medium-bias mode, R_L = 100 kΩ, and for high-bias mode, R_L = 10 kΩ.

PARAMETER MEASUREMENT INFORMATION

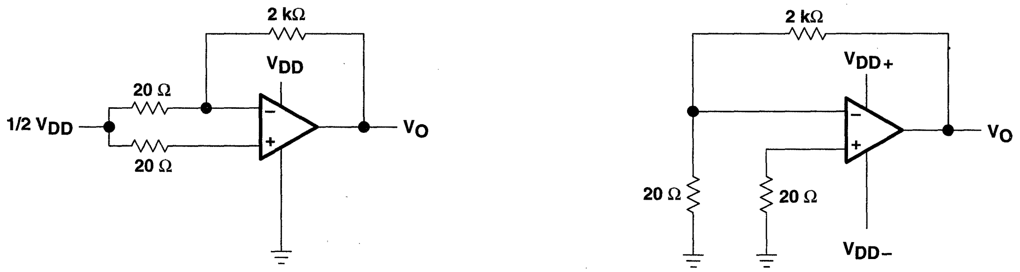
single-supply versus split-supply test circuits

Because the TLC25_4, TLC25_4A, and TLC25_4B are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



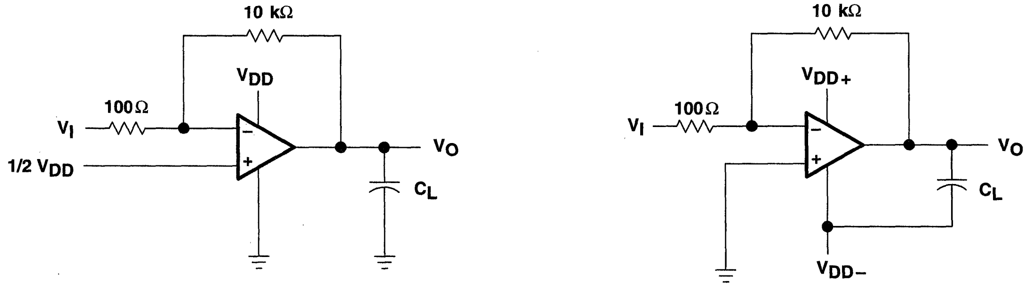
(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 1. Unity-Gain Amplifier



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

TYPICAL CHARACTERISTICS

Table of Graphs

				FIGURE
I_{DD}	Supply current		vs Supply voltage vs Free-air temperature	4 5
A_{VD}	Large-signal differential voltage amplification	Low bias	vs Frequency	6
		Medium bias	vs Frequency	7
		High bias	vs Frequency	8
	Phase shift	Low bias	vs Frequency	6
		Medium bias	vs Frequency	7
		High bias	vs Frequency	8

SUPPLY CURRENT vs SUPPLY VOLTAGE

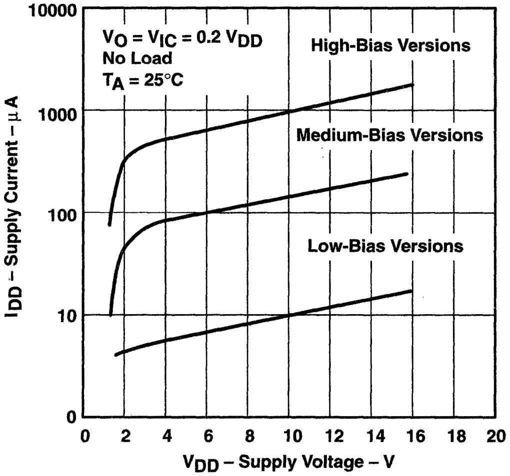


Figure 4

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

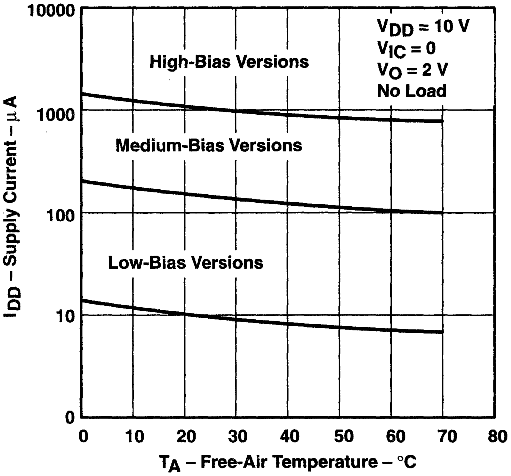


Figure 5

TYPICAL CHARACTERISTICS

LOW-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

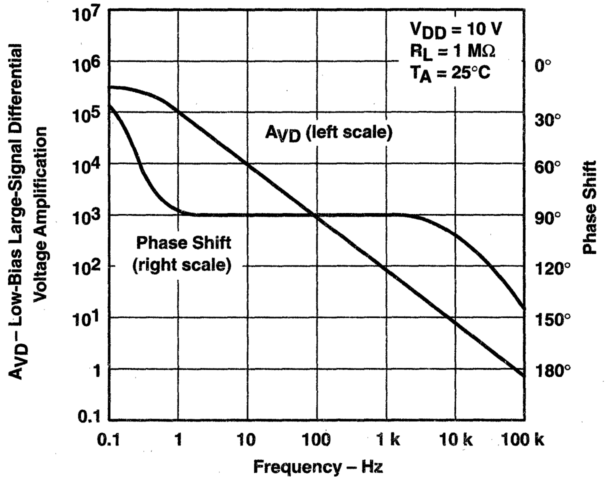


Figure 6

MEDIUM-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

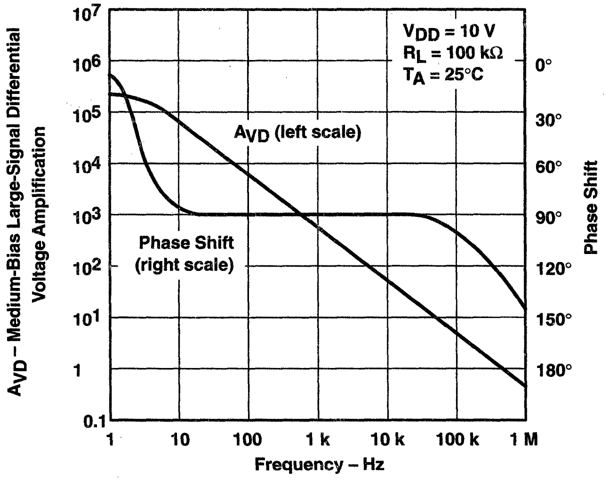


Figure 7

TYPICAL CHARACTERISTICS

HIGH-BIAS LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

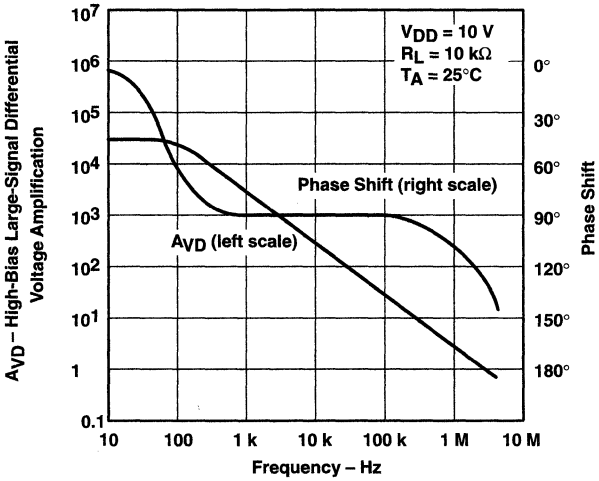


Figure 8

APPLICATION INFORMATION

latch-up avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the operational amplifiers supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the potential of V_{DD-}/GND.

supply configurations

Even though the TLC25_4C series is are characterized for single-supply operation, they can be used effectively in a split-supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

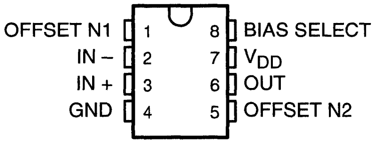
Whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup as well as excessive dc leakages.

TLC271, TLC271A, TLC271B
LinCMOS™ PROGRAMMABLE LOW-POWER OPERATIONAL AMPLIFIERS

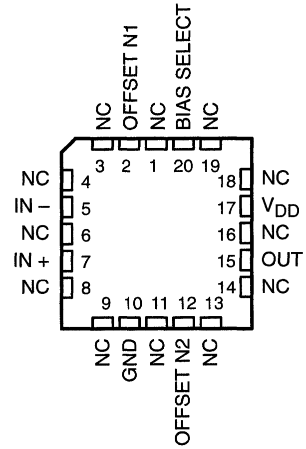
SLOS090B – NOVEMBER 1987 – REVISED AUGUST 1996

- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  - **0°C to 70°C . . . 3 V to 16 V**
  - **−40°C to 85°C . . . 4 V to 16 V**
  - **−55°C to 125°C . . . 5 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix and I-Suffix Types)**
- **Low Noise . . . 25 $nV/\sqrt{Hz}$ Typically at f = 1 kHz (High-Bias Mode)**
- **Output Voltage Range includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC271 operational amplifier combines a wide range of input offset voltage grades with low offset voltage drift and high input impedance. In addition, the TLC271 offers a bias-select mode that allows the user to select the best combination of power dissipation and ac performance for a particular application. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	2 mV 5 mV 10 mV	TLC271BCD TLC271ACD TLC271CD	—	—	TLC271BCP TLC271ACP TLC271CP
−40°C to 85°C	2 mV 5 mV 10 mV	TLC271BID TLC271AID TLC271ID	—	—	TLC271BIP TLC271AIP TLC271IP
−55°C to 125°C	10 mV	TLC271MD	TLC271MFK	TLC271MJG	TLC271MP

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC271BCDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

DEVICE FEATURES

PARAMETER†	BIAS-SELECT MODE			UNIT
	HIGH	MEDIUM	LOW	
P_D	3375	525	50	µW
SR	3.6	0.4	0.03	V/µs
V_n	25	32	68	nV/√Hz
B_1	1.7	0.5	0.09	MHz
A_{VD}	23	170	480	V/mV

† Typical at V_{DD} = 5 V, T_A = 25°C

description (continued)

Using the bias-select option, these cost-effective devices can be programmed to span a wide range of applications that previously required BiFET, NFET or bipolar technology. Three offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC271 (10 mV) to the TLC271B (2 mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC271. The devices also exhibit low-voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC271 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

bias-select feature

The TLC271 offers a bias-select feature that allows the user to select any one of three bias levels depending on the level of performance desired. The tradeoffs between bias levels involve ac performance and power dissipation (see Table 1).

bias-select feature (continued)

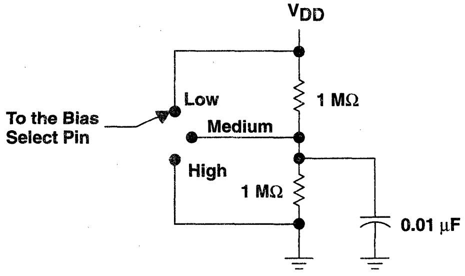
Table 1. Effect of Bias Selection on Performance

TYPICAL PARAMETER VALUES T_A = 25°C, V_{DD} = 5 V		MODE			UNIT
		HIGH BIAS R_L = 10 kΩ	MEDIUM BIAS R_L = 100 kΩ	LOW BIAS R_L = 1 MΩ	
P_D	Power dissipation	3.4	0.5	0.05	mW
SR	Slew rate	3.6	0.4	0.03	V/µs
V_n	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/√Hz
B_1	Unity-gain bandwidth	1.7	0.5	0.09	MHz
ϕ_m	Phase margin	46°	40°	34°	
A_{VD}	Large-signal differential voltage amplification	23	170	480	V/mV

bias selection

Bias selection is achieved by connecting the bias select pin to one of three voltage levels (see Figure 1). For medium-bias applications, it is recommended that the bias select pin be connected to the midpoint between the supply rails. This procedure is simple in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated in Figure 1. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint can be used if it is within the voltages specified in Figure 1.

bias selection (continued)



BIAS MODE	BIAS-SELECT VOLTAGE (single supply)
Low	V_{DD}
Medium	1 V to V_{DD} – 1 V
High	GND

Figure 1. Bias Selection for Single-Supply Applications

high-bias mode

In the high-bias mode, the TLC271 series features low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices but at only a fraction of the power dissipation. Unity-gain bandwidth is typically greater than 1 MHz.

medium-bias mode

The TLC271 in the medium-bias mode features low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices but power dissipation is only a fraction of that consumed by bipolar devices.

low-bias mode

In the low-bias mode, the TLC271 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

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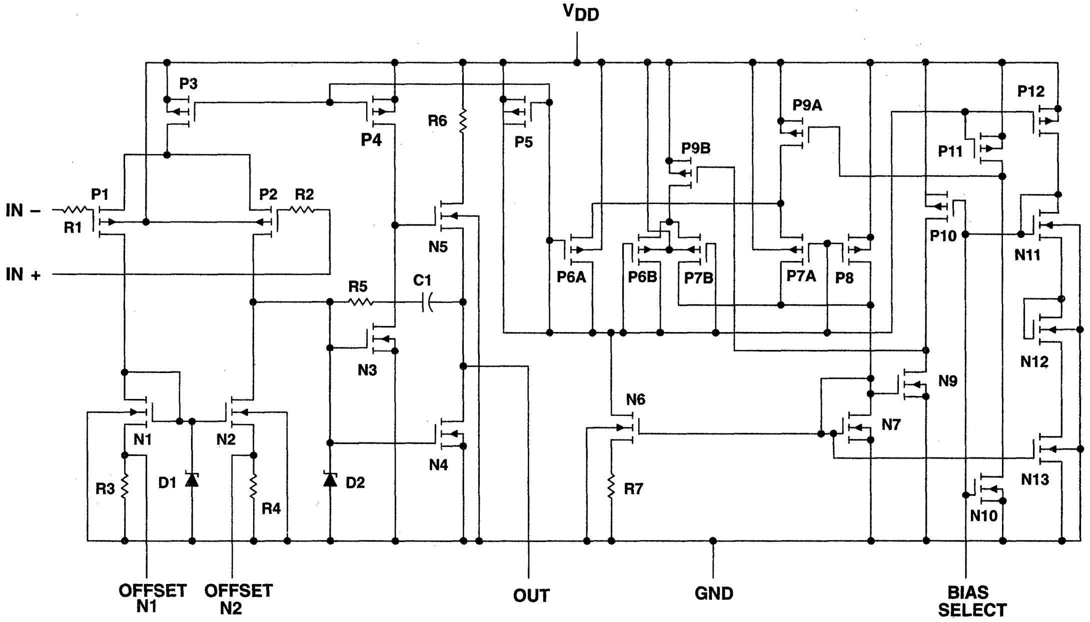
electrical characteristics operating characteristics typical characteristics	medium (Figures 34 – 65)
electrical characteristics operating characteristics typical characteristics	low (Figures 66 – 97)
parameter measurement information	all
application information	all

equivalent schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . ±V_{DD}
Input voltage range, V_I (any input) . . . . – 0.3 V to V_{DD}
Input current, I_I . . . . ±5 mA
Output current, I_O . . . . ±30 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . Unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix . . . . 0°C to 70°C
I suffix . . . . – 40°C to 85°C
M suffix . . . . – 55°C to 125°C
Storage temperature range . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	5	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	−0.2	3.5	−0.2	3.5	0	3.5	V
	V_{DD} = 10 V	−0.2	8.5	−0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC271C, TLC271AC, TLC271BC						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.34	2		0.39	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8			2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				0°C	3	3.8		7.8	8.5		
				70°C	3	3.8		7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
				0°C	4	27		7.5	42		
				70°C	4	20		7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
				0°C	60	84		60	88		
				70°C	60	85		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V V_O = 1.4 V	25°C	65	95		65	95		dB
				0°C	60	94		60	94		
				70°C	60	96		60	96		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		µA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		675	1600		950	2000	µA
				0°C		775	1800		1125	2200	
				70°C		575	1300		750	1700	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC271I, TLC271AI, TLC271BI						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.34	2		0.39	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8			2		µV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				−40°C	3	3.8		7.8	8.5		
				85°C	3	3.8		7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
				−40°C	3.5	32		7	46		
				85°C	3.5	19		7	31		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	80		65	85		dB
				−40°C	60	81		60	87		
				85°C	60	86		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V V_O = 1.4 V	25°C	65	95		65	95		dB
				−40°C	60	92		60	92		
				85°C	60	96		60	96		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		µA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		675	1600		950	2000	µA
				−40°C		950	2200		1375	2500	
				85°C		525	1200		725	1600	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC271M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		2.1			2.2		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
			−55°C	3	3.8		7.8	8.5		
			125°C	3	3.8		7.8	8.4		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
			−55°C	3.5	35		7	50		
			125°C	3.5	16		7	27		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
			−55°C	60	81		60	87		
			125°C	60	84		60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V V_O = 1.4 V	25°C	65	95		65	95		dB
			−55°C	60	90		60	90		
			125°C	60	97		60	97		
$I_{I(SEL)}$	Input current (BIAS SELECT)	$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		µA
I_{DD}	Supply current	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$, No load	25°C		675	1600		950	2000	µA
			−55°C		1000	2500		1475	3000	
			125°C		475	1100		625	1400	

† Full range is −55°C to 125°C.

NOTES:
4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC271C, TLC271AC, TLC271BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH} , R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC271C, TLC271AC, TLC271BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			$V_{I(PP)}$ = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	f = B_1, C_L = 20 pF,	V_I = 10 mV, See Figure 100	25°C		49°		
				0°C		50°		
				70°C		46°		

HIGH-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC271I, TLC271AI, TLC271BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		3.6		V/µs
				–40°C		4.5		
				85°C		2.8		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				–40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		320		kHz
				–40°C		380		
				85°C		250		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		1.7		MHz
				–40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		46°		
				–40°C		49°		
				85°C		43°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC271I, TLC271AI, TLC271BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		5.3		V/µs
				–40°C		6.8		
				85°C		4		
			$V_{I(PP)}$ = 5.5 V	25°C		4.6		
				–40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		200		kHz
				–40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		2.2		MHz
				–40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f= B_1, See Figure 100	25°C		49°		
				–40°C		52°		
				85°C		46°		

HIGH-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC271M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		320		kHz
				−55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC271M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			$V_{I(PP)}$ = 5.5 V	25°C		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	f = B_1, C_L = 20 pF,	V_I = 10 mV, See Figure 100	25°C		49°		
				−55°C		52°		
				125°C		44°		

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	2, 3
α_{VIO}	Temperature coefficient	Distribution	4, 5
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	6, 7 8 9
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	10, 11 12 13 14, 15
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	16 17 28, 29
I_{IB}	Input bias current	vs Free-air temperature	18
I_{IO}	Input offset current	vs Free-air temperature	18
V_{IC}	Common-mode input voltage	vs Supply voltage	19
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	20 21
SR	Slew rate	vs Supply voltage vs Free-air temperature	22 23
	Bias-select current	vs Supply voltage	24
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	25
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	26 27
A_{VD}	Large-signal differential voltage amplification	vs Frequency	28, 29
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	30 31 32
V_n	Equivalent input noise voltage	vs Frequency	33
	Phase shift	vs Frequency	28, 29

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

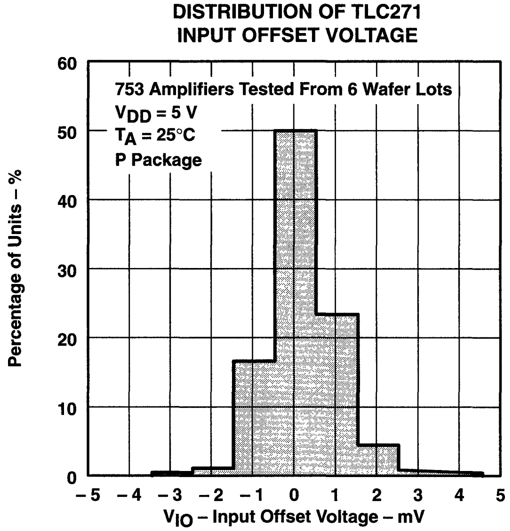

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

Figure 2

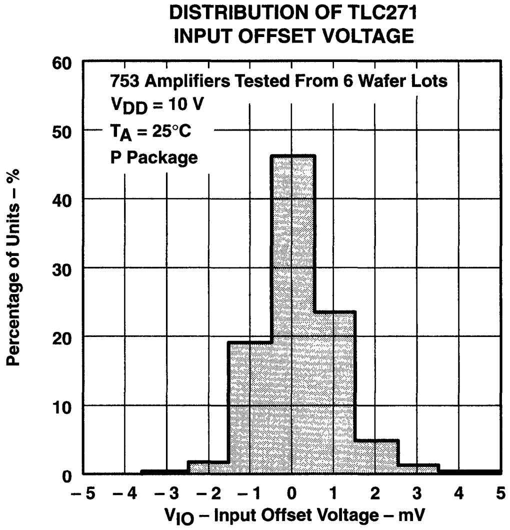

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

Figure 3

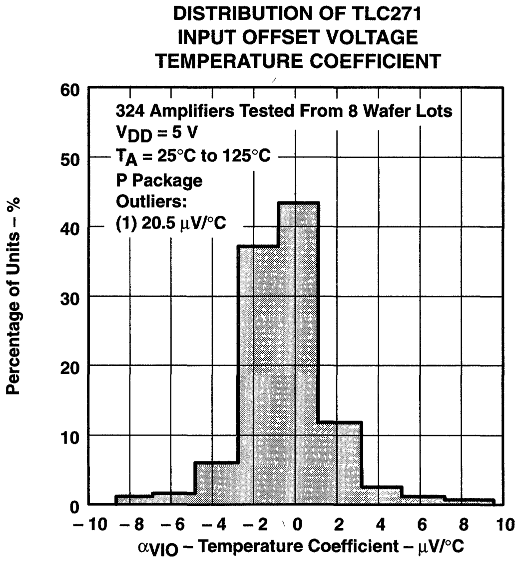

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

Figure 4

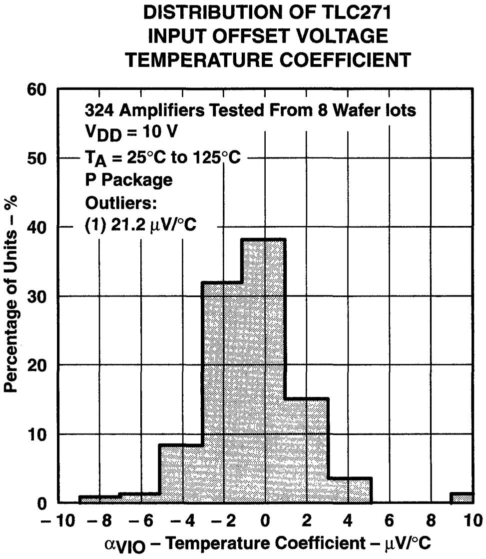

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

Figure 5

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

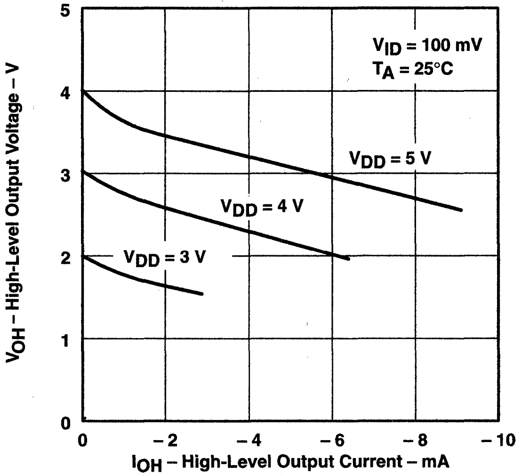

Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

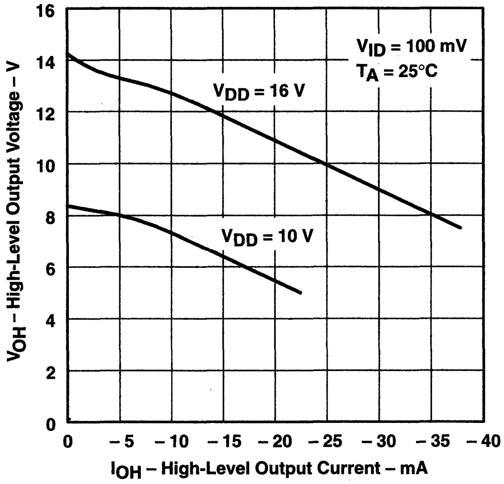

Figure 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

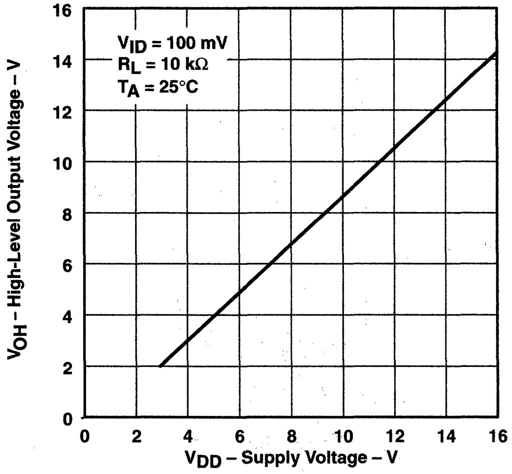

Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

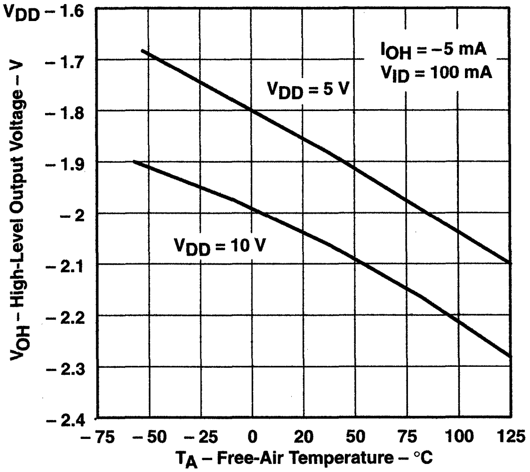

Figure 9

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

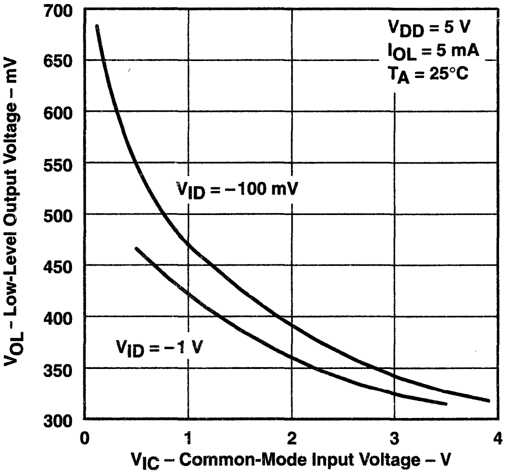

Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

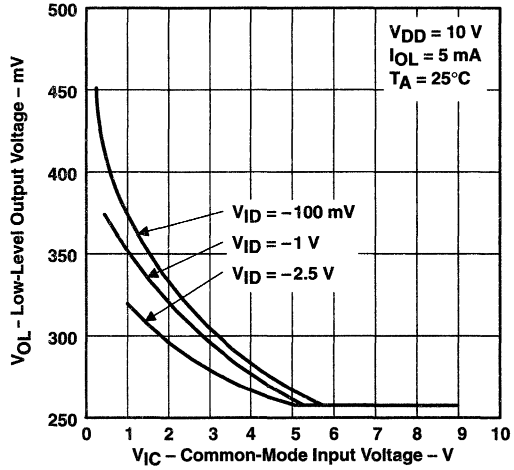

Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

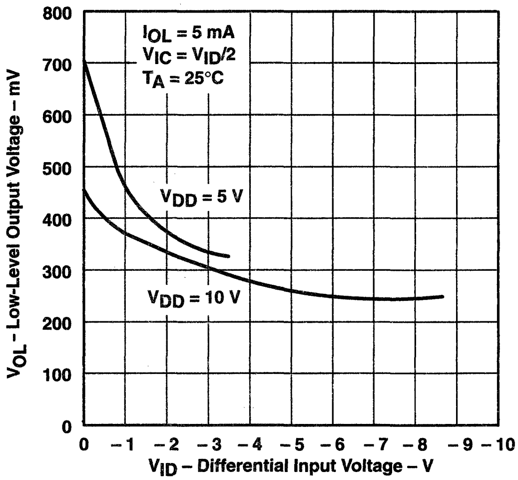

Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

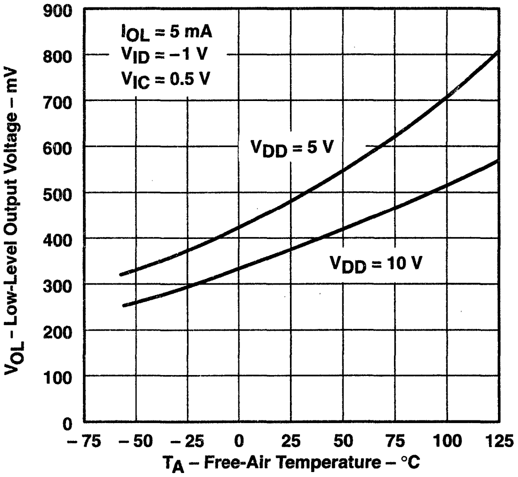

Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

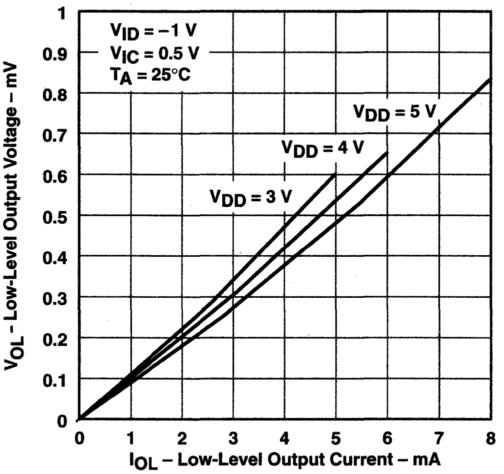

Figure 14

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

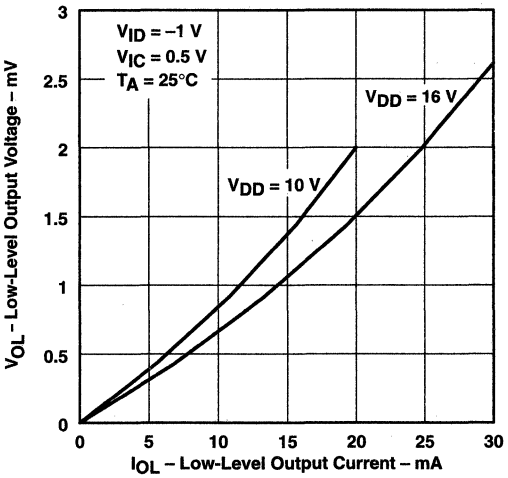

Figure 15

**LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE**

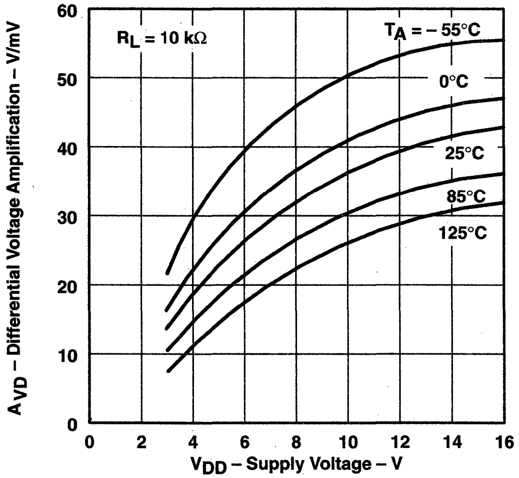

Figure 16

**LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE**

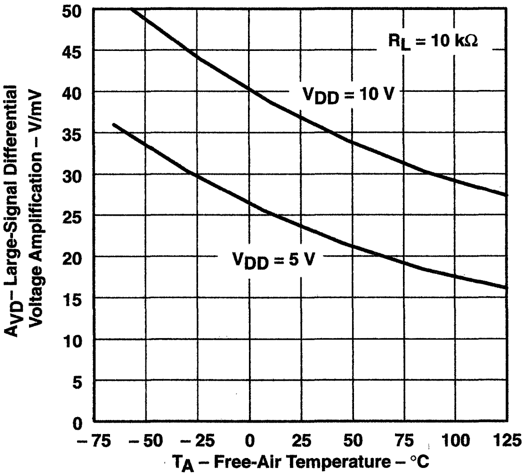

Figure 17

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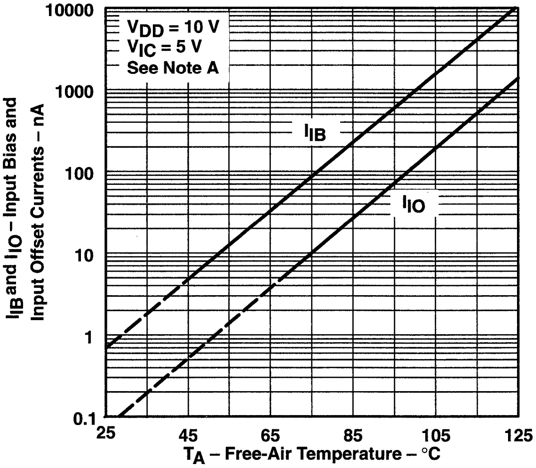
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 18

COMMON-MODE INPUT VOLTAGE (POSITIVE LIMIT) vs SUPPLY VOLTAGE

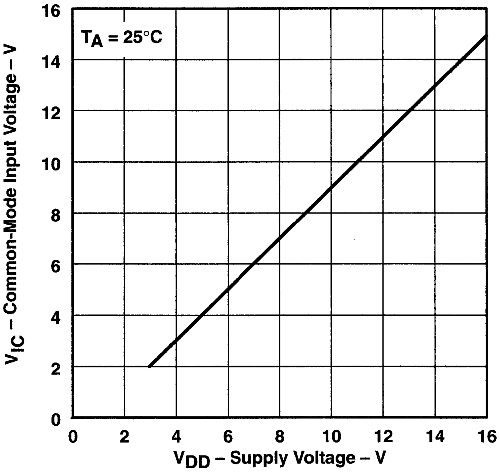


Figure 19

SUPPLY CURRENT vs SUPPLY VOLTAGE

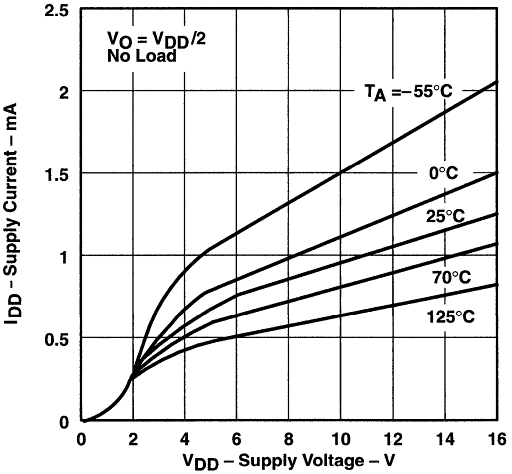


Figure 20

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

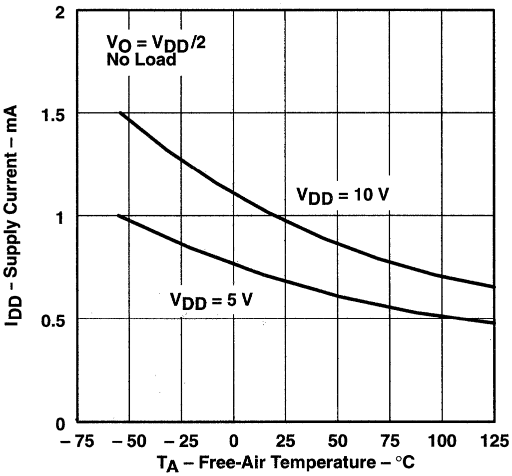


Figure 21

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

SLEW RATE
vs
SUPPLY VOLTAGE

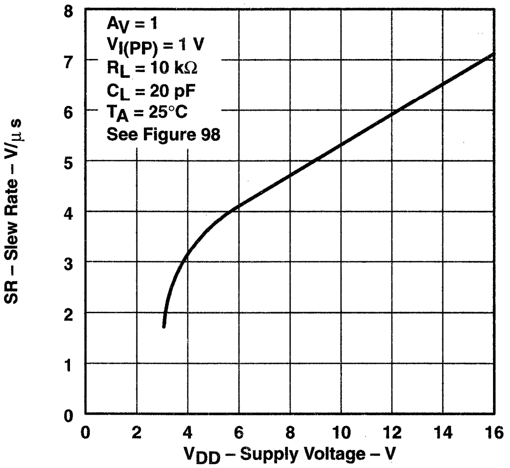

Figure 22

SLEW RATE
vs
FREE-AIR TEMPERATURE

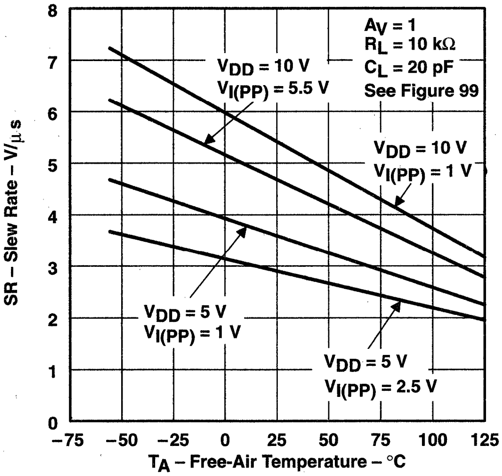

Figure 23

BIAS-SELECT CURRENT
vs
SUPPLY VOLTAGE

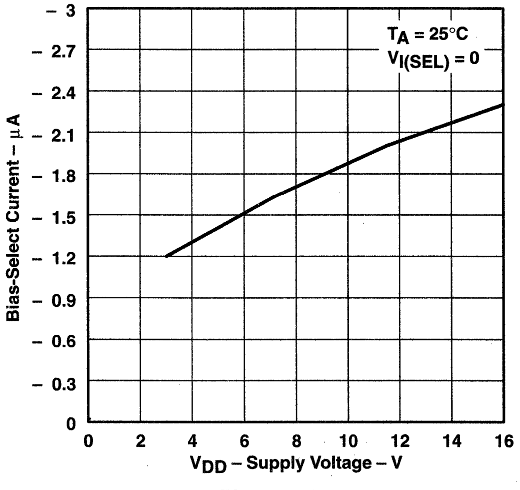

Figure 24

MAXIMUM PEAK-TO-PEAK OUTPUT
VOLTAGE
vs
FREQUENCY

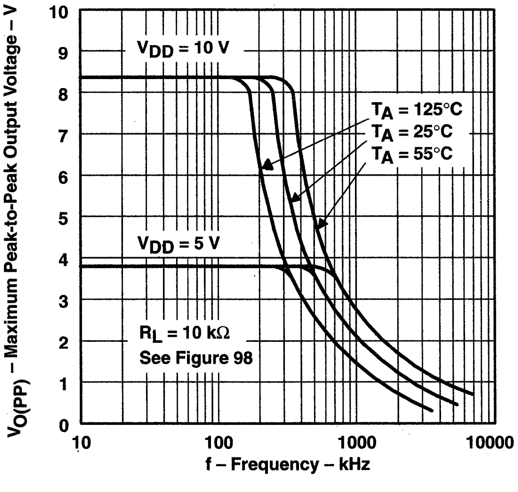

Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

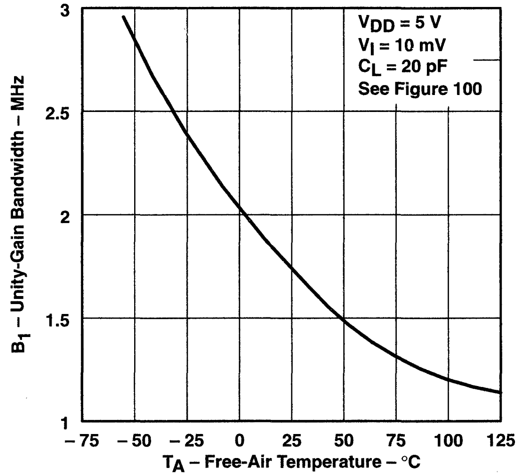

Figure 26

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

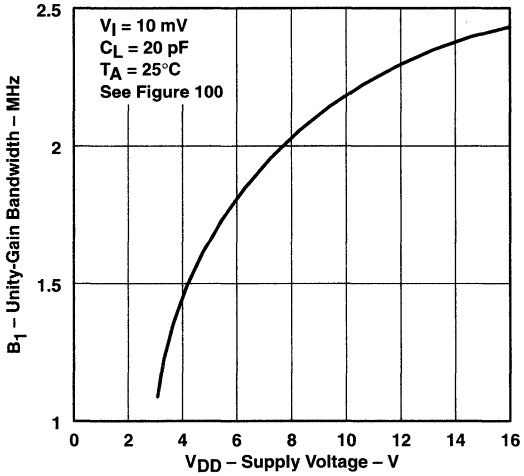

Figure 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

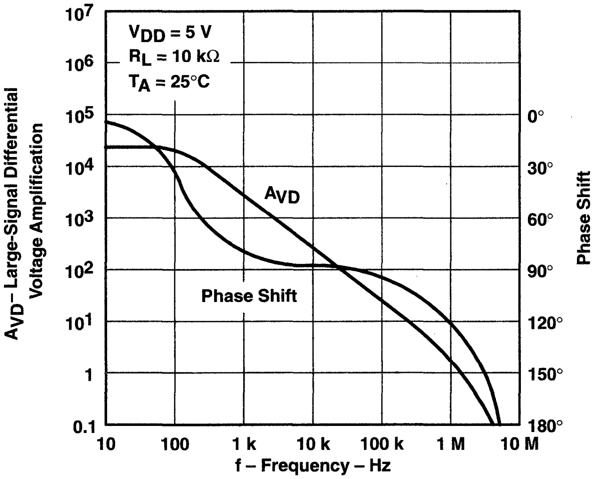

Figure 28

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

LARGE-SCALE DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

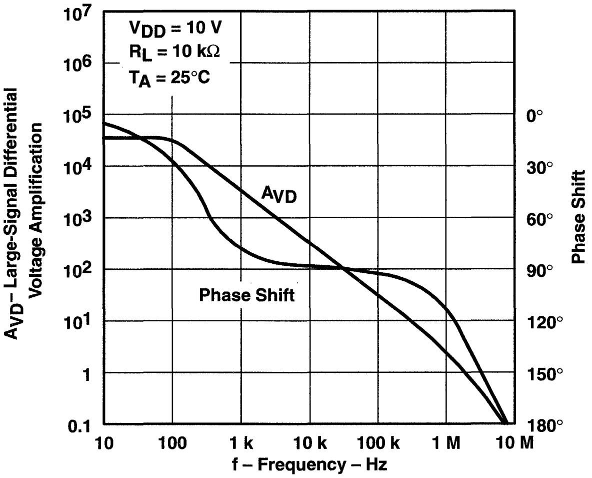

Figure 29

PHASE MARGIN vs SUPPLY VOLTAGE

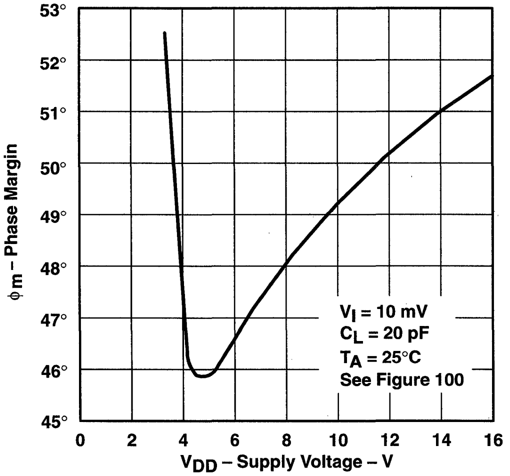

Figure 30

PHASE MARGIN vs FREE-AIR TEMPERATURE

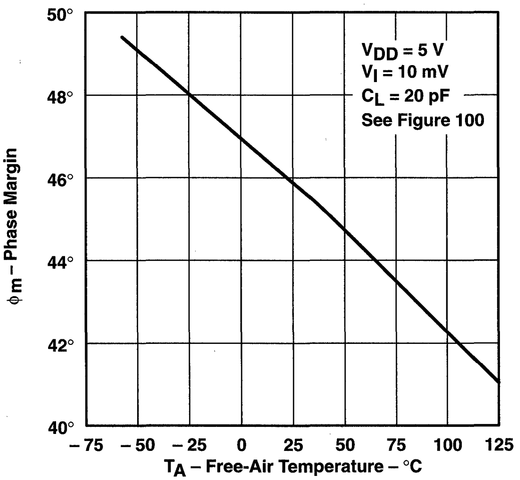

Figure 31

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

PHASE MARGIN
vs
CAPACITIVE LOAD

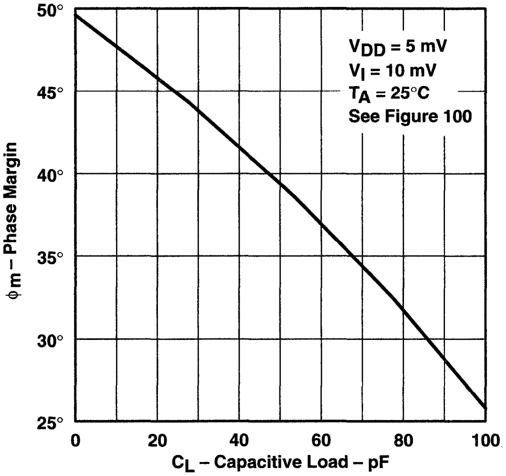

Figure 32

EQUIVALENT NOISE VOLTAGE
vs
FREQUENCY

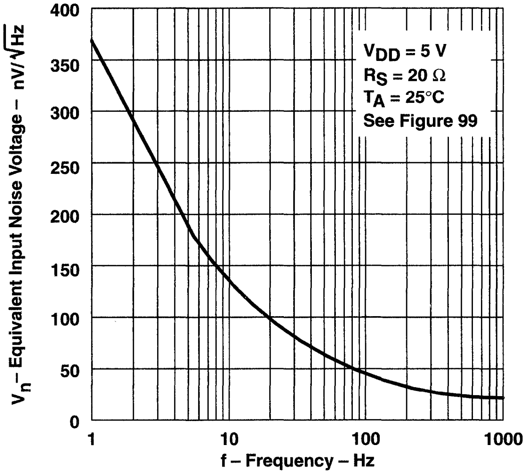

Figure 33

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC271C, TLC271AC, TLC271BC						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 R_S = 50 Ω, R_I = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.25	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7			2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				0°C	3	3.9		7.8	8.7		
				70°C	3	4		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
				0°C	15	200		15	320		
				70°C	15	140		15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
				0°C	60	91		60	94		
				70°C	60	92		60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V V_O = 1.4 V	25°C	70	93		70	93		dB
				0°C	60	92		60	92		
				70°C	60	94		60	94		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)}$ = V_{DD}/2	25°C		−130			−160		nA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		105	280		143	300	μA
				0°C		125	320		173	400	
				70°C		85	220		110	280	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC271I, TLC271AI, TLC271BI						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.25	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				−40°C	3	3.9		7.8	8.7		
				85°C	3	4		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
				−40°C	15	270		15	390		
				85°C	15	130		15	220		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
				−40°C	60	90		60	93		
				85°C	60	90		60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				−40°C	60	91		60	91		
				85°C	60	94		60	94		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)}$ = $V_{DD}/2$	25°C		−130			−160		nA
I_{DD}	Supply current		V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$, No load	25°C		105	280		143	300	µA
				−40°C		158	400		225	450	
				85°C		80	200		103	260	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC271M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
			−55°C	3	3.9		7.8	8.6		
			125°C	3	4		7.8	8.6		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ See Note 6	25°C	25	170		25	275		V/mV
			−55°C	15	290		15	420		
			125°C	15	120		15	190		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
			−55°C	60	89		60	93		
			125°C	60	91		60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V V_O = 1.4 V	25°C	70	93		70	93		dB
			−55°C	60	91		60	91		
			125°C	60	94		60	94		
$I_{I(SEL)}$	Input current (BIAS SELECT)	$V_{I(SEL)}$ = $V_{DD}/2$	25°C		−130			−160		nA
I_{DD}	Supply current	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$, No load	25°C		105	280		143	300	µA
			−55°C		170	440		245	500	
			125°C		70	180		90	240	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC271C, TLC271AC, TLC271BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		525		kHz
				0°C		600		
				70°C		400		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC271C, TLC271AC, TLC271BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		43°		
				0°C		44°		
				70°C		42°		

MEDIUM-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC271I, TLC271AI, TLC271BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				−40°C		0.51		
				85°C		0.35		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		525		MHz
				−40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC271I, TLC271AI, TLC271BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.62		V/μs
				−40°C		0.77		
				85°C		0.47		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH},3 R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		635		kHz
				−40°C		880		
				85°C		480		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		43°		
				−40°C		46°		
				85°C		41°		

MEDIUM-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC271M MIN	TLC271M TYP	TLC271M MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				−55°C		0.50		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		525		kHz
				−55°C		850		
				125°C		330		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		40°		
				−55°C		43°		
				125°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC271M MIN	TLC271M TYP	TLC271M MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		35		kHz
				−55°C		50		
				125°C		20		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		635		kHz
				−55°C		960		
				125°C		440		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		43°		
				−55°C		47°		
				125°C		39°		

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

Table of Graphs

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V_{IO}	Input offset voltage	Distribution	34, 35
αV_{IO}	Temperature coefficient	Distribution	36, 37
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	38, 39 40 41
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A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	48 49 60, 61
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V_I	Maximum Input voltage	vs Supply voltage	51
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	52 53
SR	Slew rate	vs Supply voltage vs Free-air temperature	54 55
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$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	57
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	58 59
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V_n	Equivalent input noise voltage	vs Frequency	65
	Phase shift	vs Frequency	60, 61

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

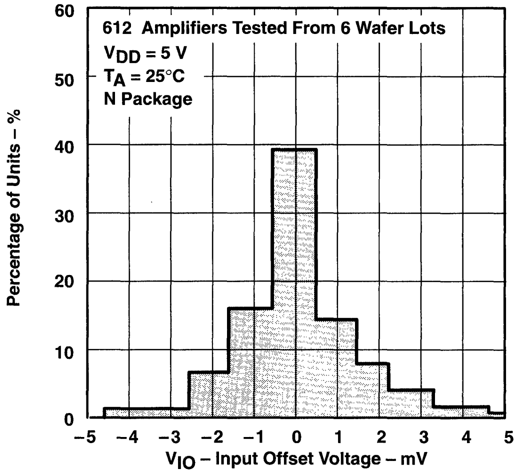

Figure 34

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

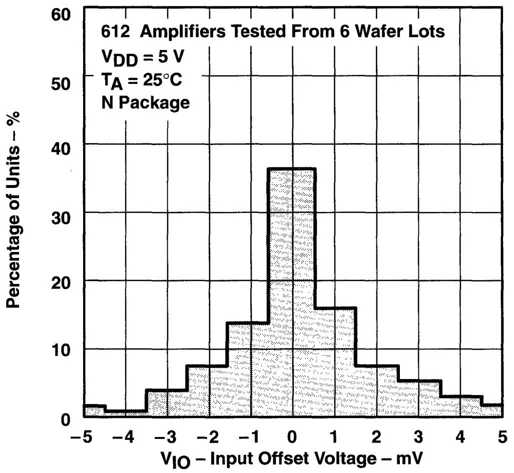

Figure 35

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

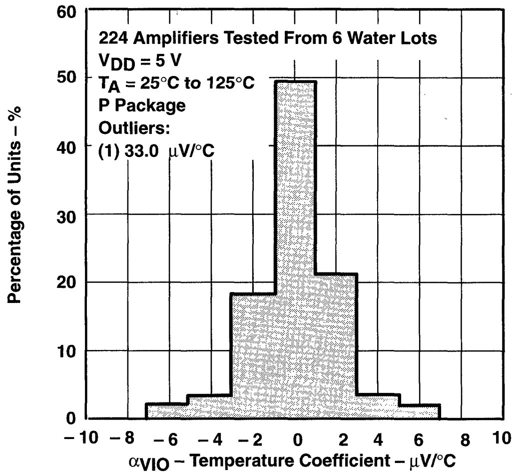

Figure 36

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

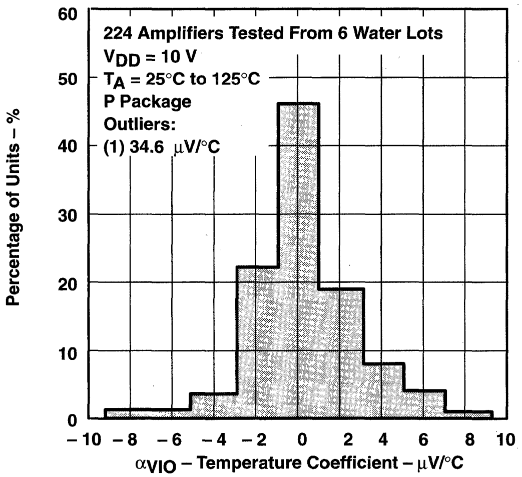

Figure 37

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

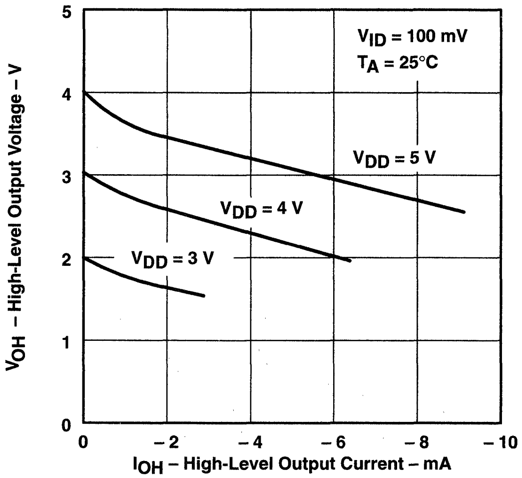

Figure 38

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

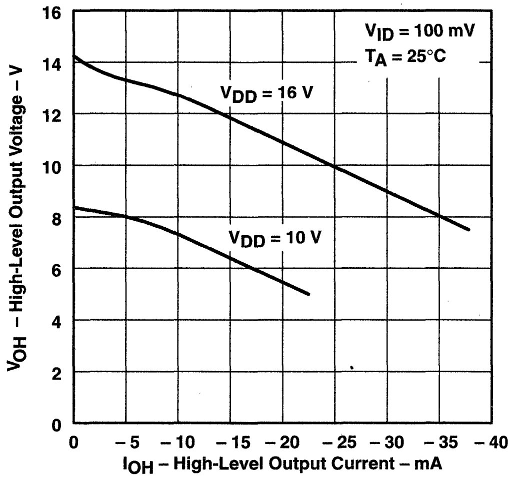

Figure 39

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

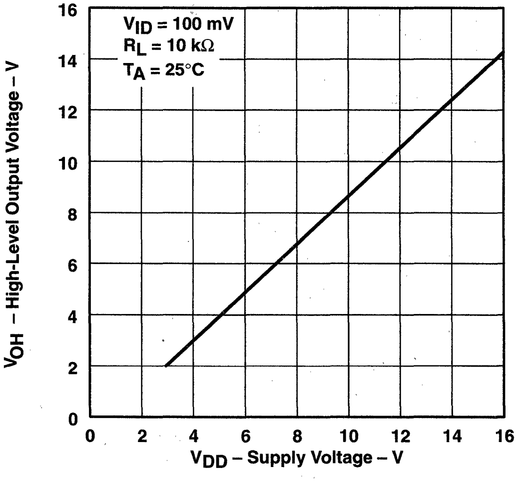

Figure 40

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

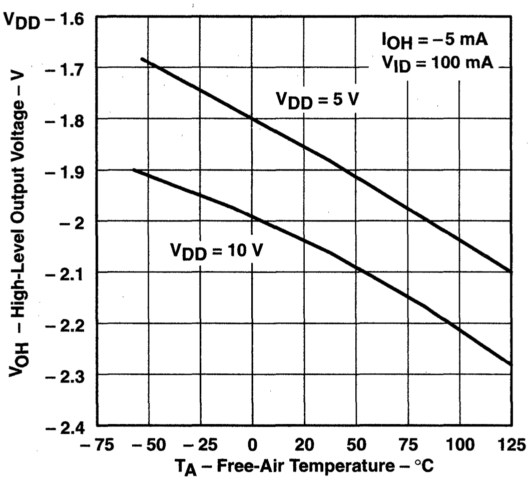

Figure 41

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

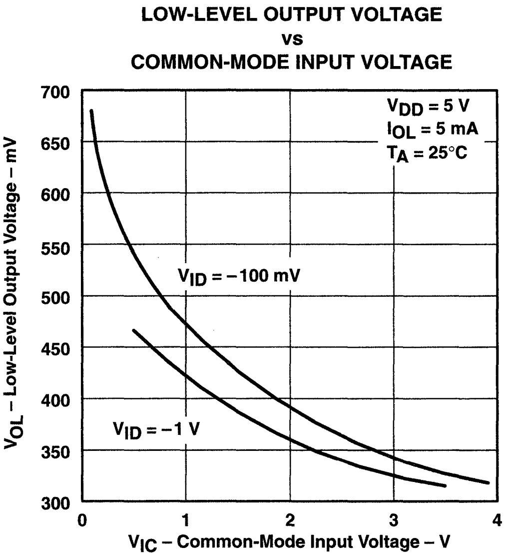

Figure 42

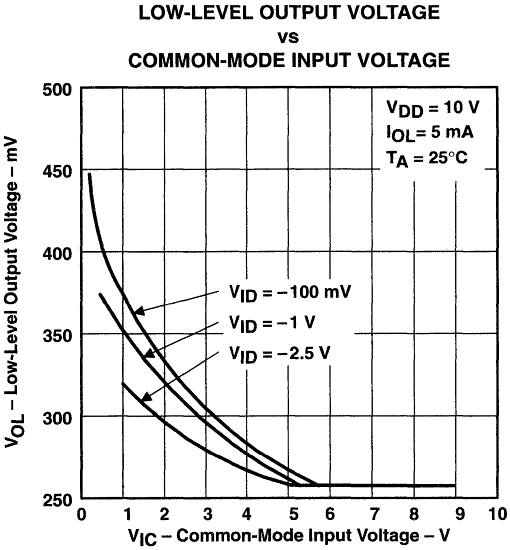

Figure 43

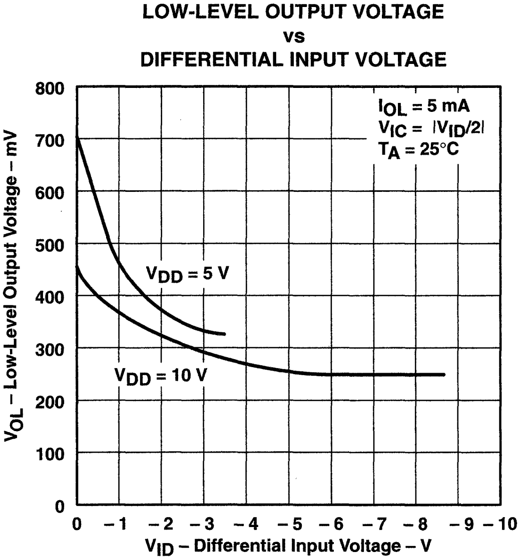

Figure 44

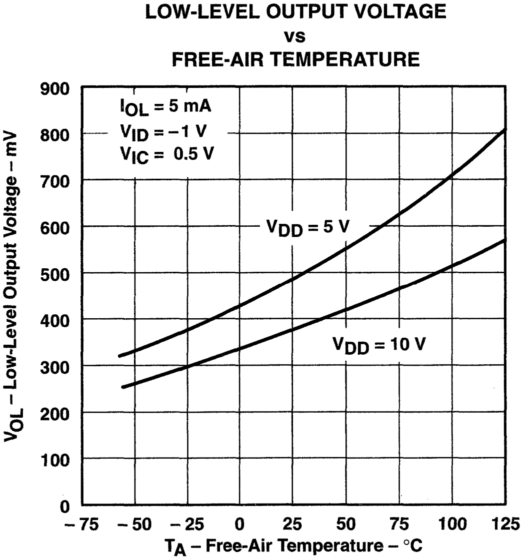

Figure 45

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

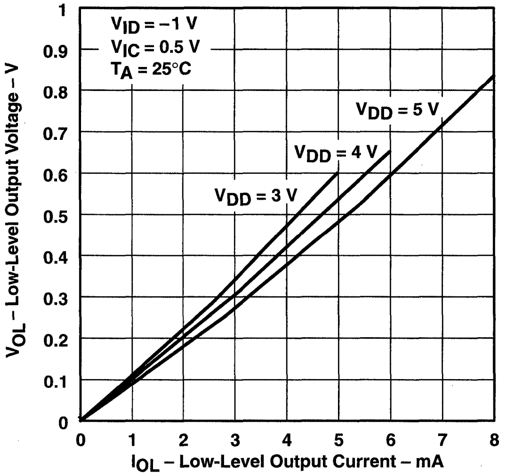
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 46

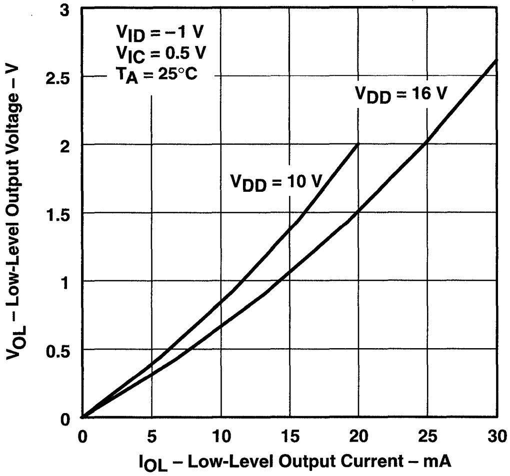
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 47

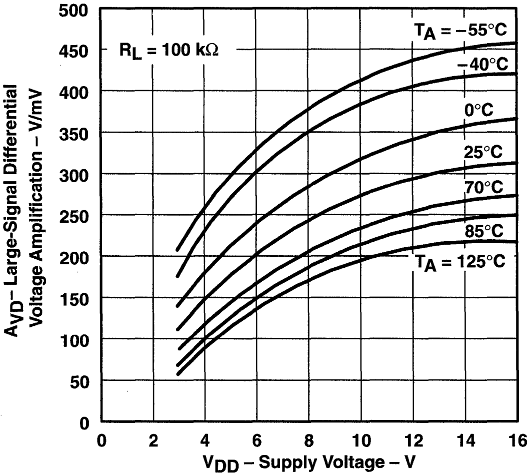
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

Figure 48

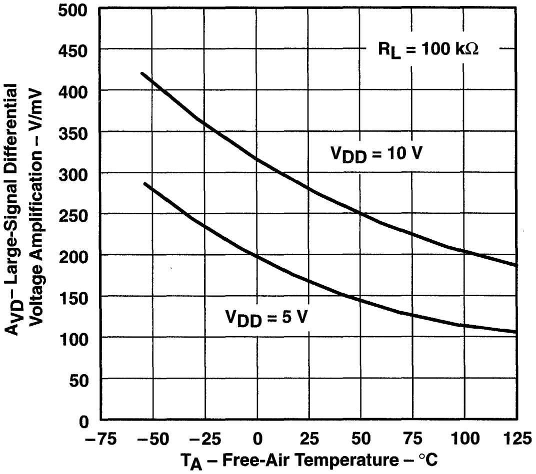
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

Figure 49

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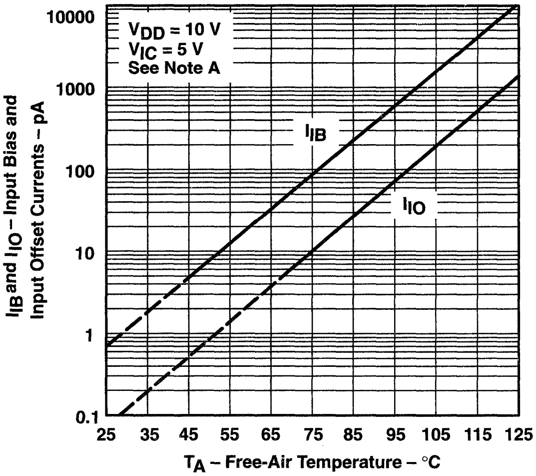
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 50

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

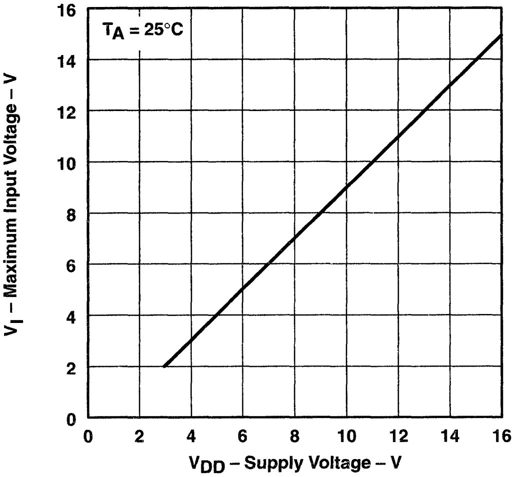


Figure 51

SUPPLY CURRENT vs SUPPLY VOLTAGE

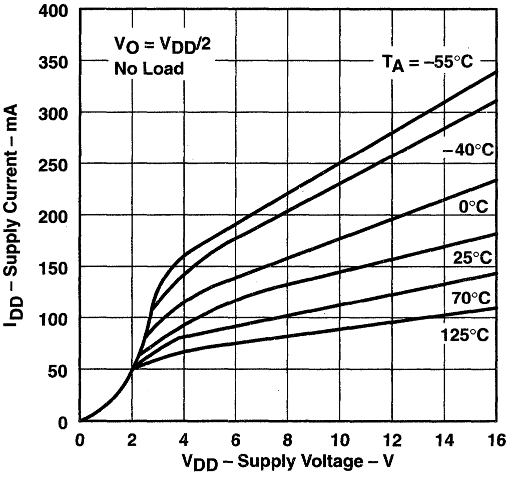


Figure 52

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

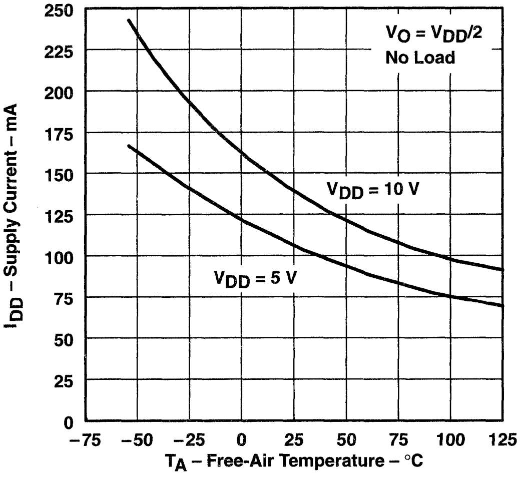


Figure 53

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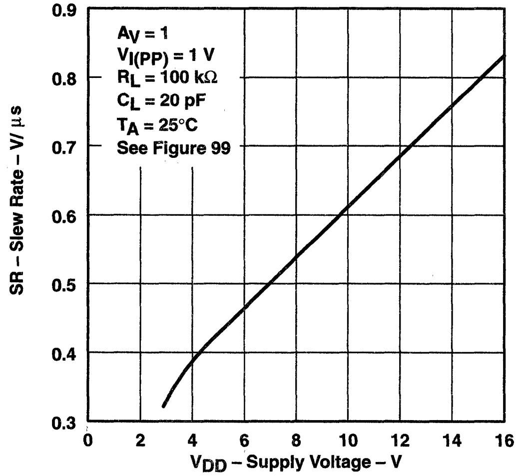
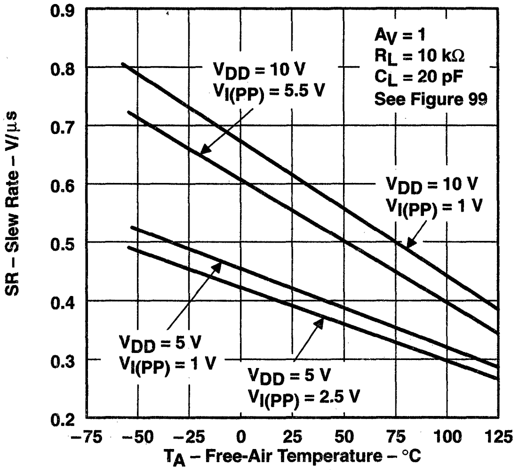
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†



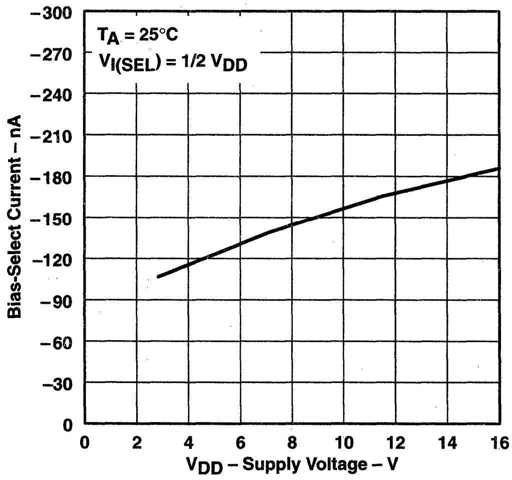
SLEW RATE
vs
SUPPLY VOLTAGE

Figure 54



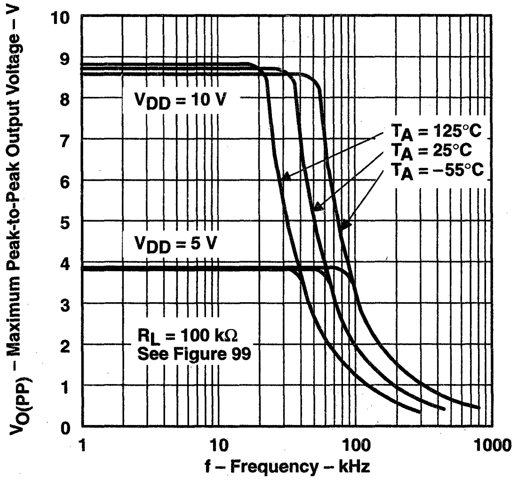
SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 55



BIAS-SELECT CURRENT
vs
SUPPLY VOLTAGE

Figure 56



MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

Figure 57

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

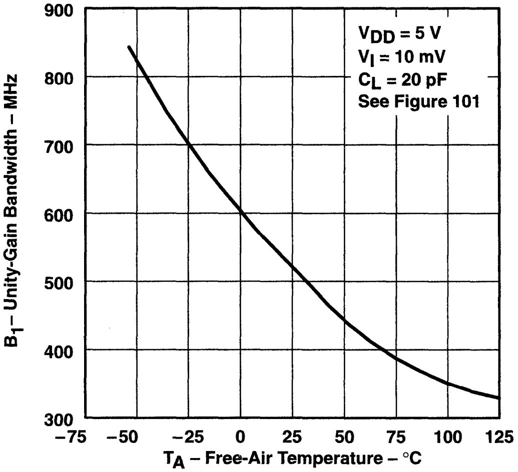

Figure 58

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

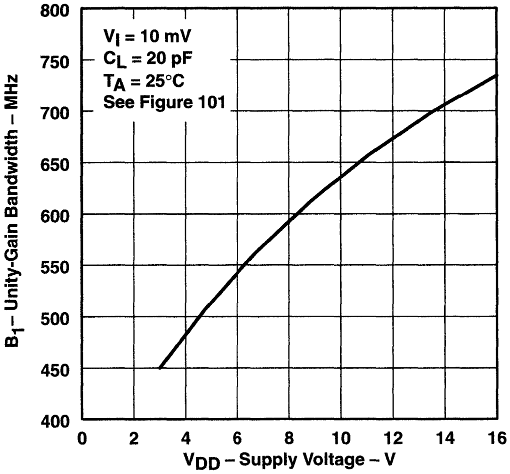

Figure 59

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

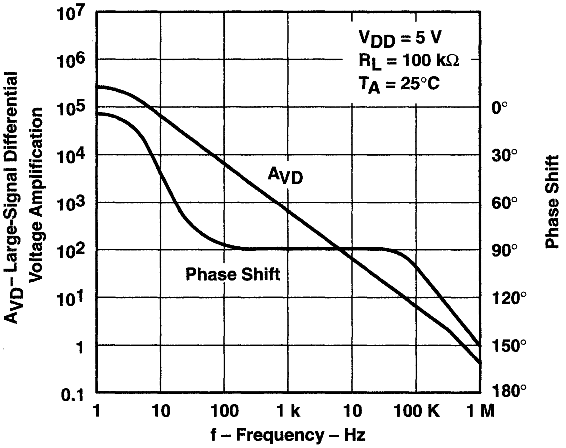

Figure 60

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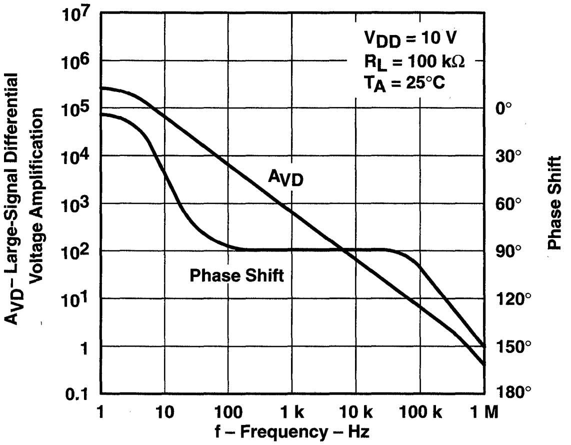
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY



PHASE MARGIN vs SUPPLY VOLTAGE

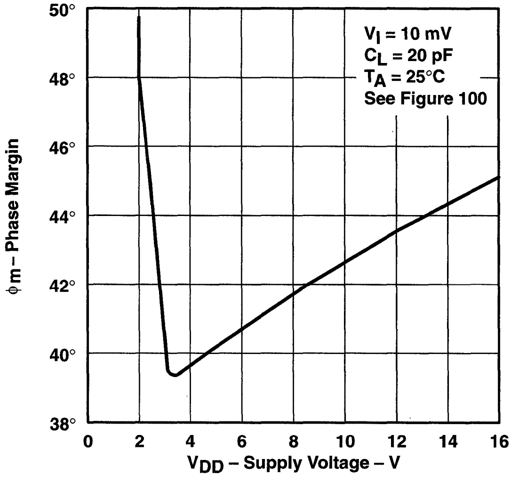


Figure 61

PHASE MARGIN vs FREE-AIR TEMPERATURE

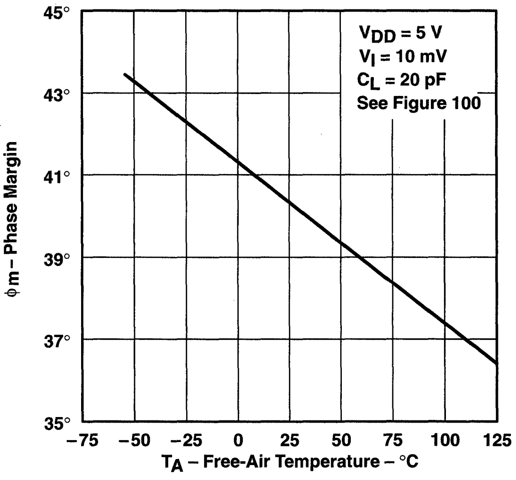


Figure 62

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

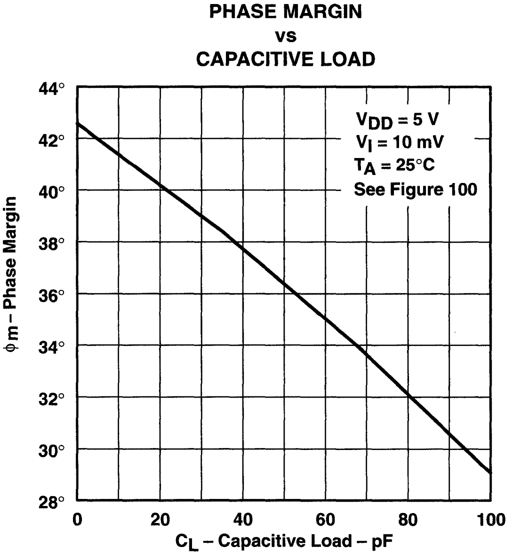

Figure 63

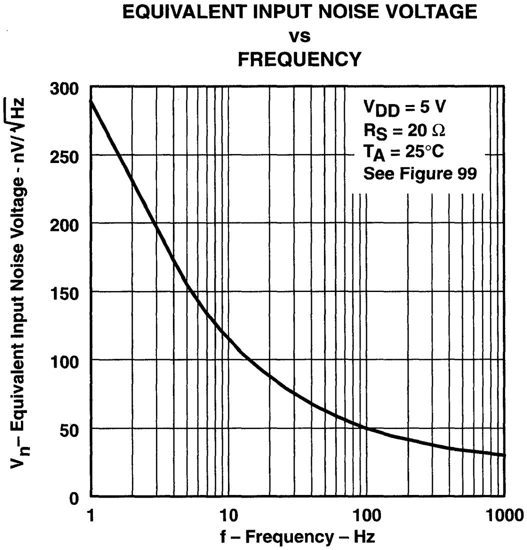

Figure 64

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

LOW-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC271C, TLC271AC, TLC271BC						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_I = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.24	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				0°C	3	4.1		7.8	8.9		
				70°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
				0°C	50	700		50	1030		
				70°C	50	380		50	660		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	94		65	97		dB
				0°C	60	95		60	97		
				70°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V V_O = 1.4 V	25°C	70	97		70	97		dB
				0°C	60	97		60	97		
				70°C	60	98		60	98		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		10	17		14	23	μA
				0°C		12	21		18	33	
				70°C		8	14		11	20	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC271I, TLC271AI, TLC271BI						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.24	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L= 1 MΩ	25°C	3	4.1		8	8.9		V
				−40°C	3	4.1		7.8	8.9		
				85°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L= 1 MΩ See Note 6	25°C	50	520		50	870		V/mV
				−40°C	50	900		50	1550		
				85°C	50	330		50	585		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	94		65	97		dB
				−40°C	60	95		60	97		
				85°C	60	95		60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V V_O = 1.4 V	25°C	70	97		70	97		dB
				−40°C	60	97		60	97		
				85°C	60	98		60	98		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		10	17		14	23	μA
				−40°C		16	27		25	43	
				85°C		17	13		10	18	

† Full range is −40 to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC271M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
			−55°C	3	4.1		7.8	8.8		
			125°C	3	4.2		7.8	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
			−55°C	25	1000		25	1775		
			125°C	25	200		25	380		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	94		65	97		dB
			−55°C	60	95		60	97		
			125°C	60	85		60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V V_O = 1.4 V	25°C	70	97		70	97		dB
			−55°C	60	97		60	97		
			125°C	60	98		60	98		
$I_{I(SEL)}$	Input current (BIAS SELECT)	$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$, No load	25°C		10	17		14	23	µA
			−55°C		17	30		28	48	
			125°C		7	12		9	15	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC271C, TLC271AC, TLC271BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC271C, TLC271AC, TLC271BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		38°		
				0°C		40°		
				70°C		34°		

LOW-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC271I, TLC271AI, TLC271BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.03		V/µs
				–40°C		0.04		
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				–40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		68		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		5		kHz
				–40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		85		MHz
				–40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		34°		
				–40°C		38°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC271C, TLC271AC, TLC271BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.05		V/µs
				–40°C		0.06		
				85°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				–40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		68		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		1		kHz
				–40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		110		MHz
				–40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_I = 10 mV,l C_L = 20 pF,	f = B_1, See Figure 100	25°C		38°		
				–40°C		42°		
				85°C		32°		

LOW-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC271M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		34°		
				−55°C		39°		
				125°C		25°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC271M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 100	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		38°		
				−55°C		43°		
				125°C		29°		

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

Table of Graphs

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TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

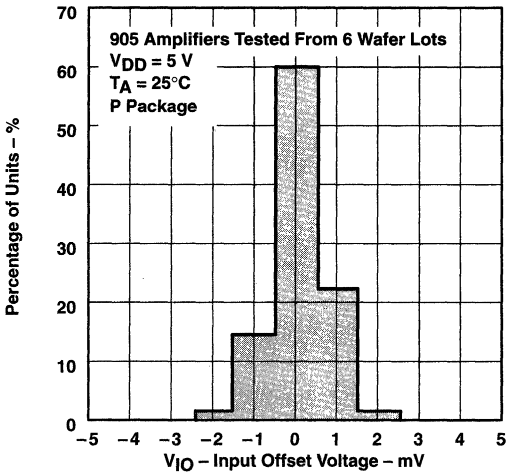
DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

Figure 65

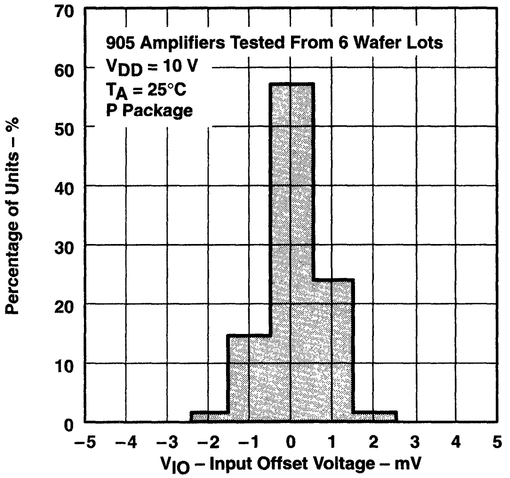
DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

Figure 66

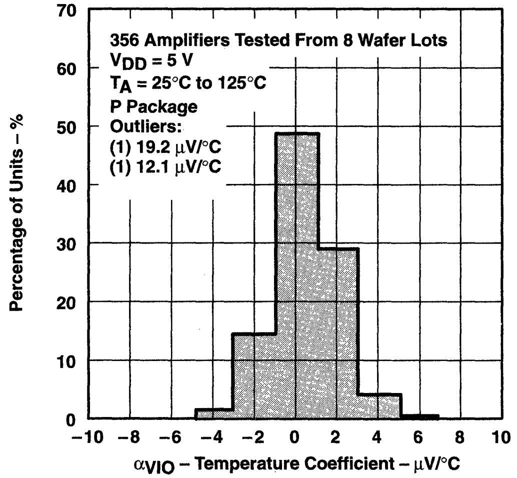
DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

Figure 67

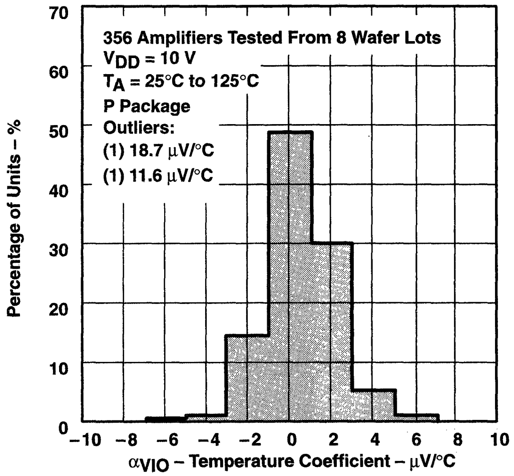
DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

Figure 68

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

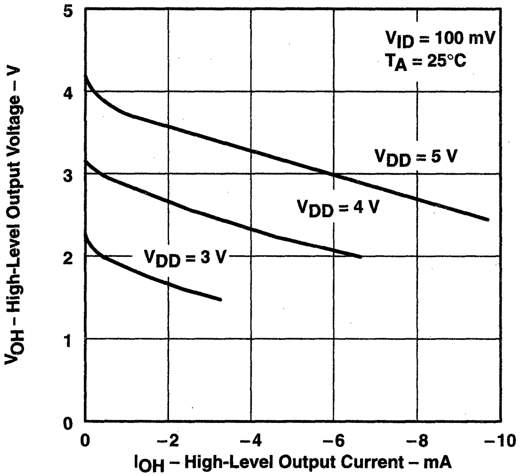

Figure 69

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

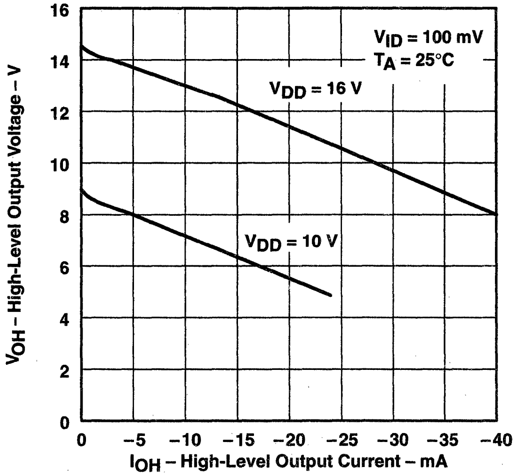

Figure 70

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

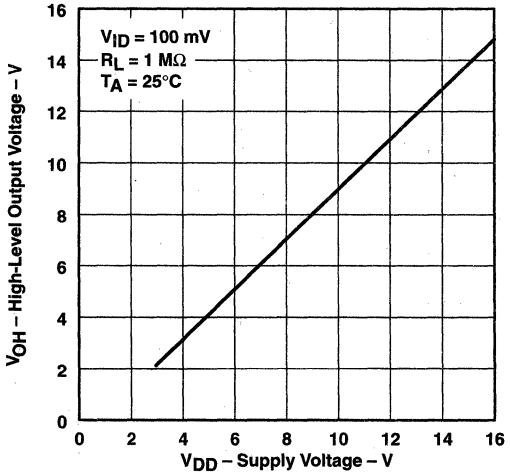

Figure 71

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

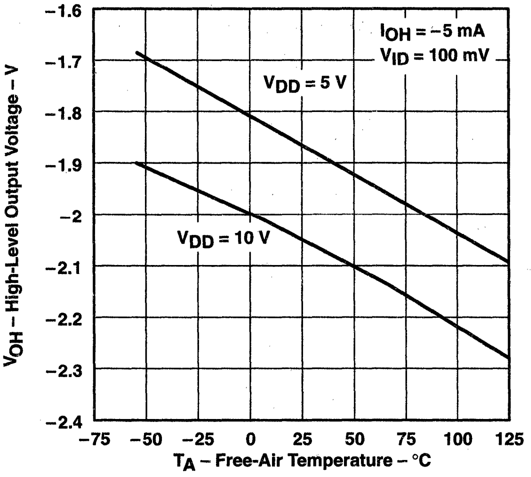

Figure 72

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

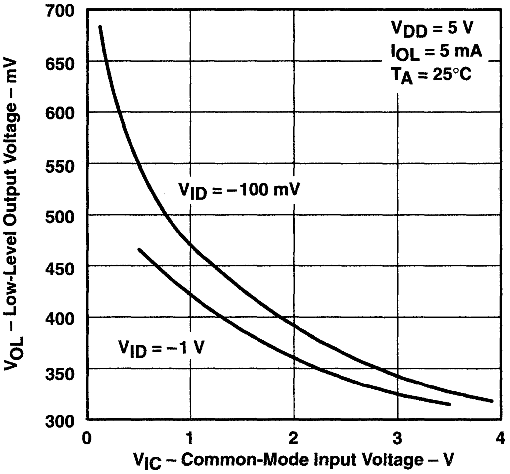

Figure 73

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

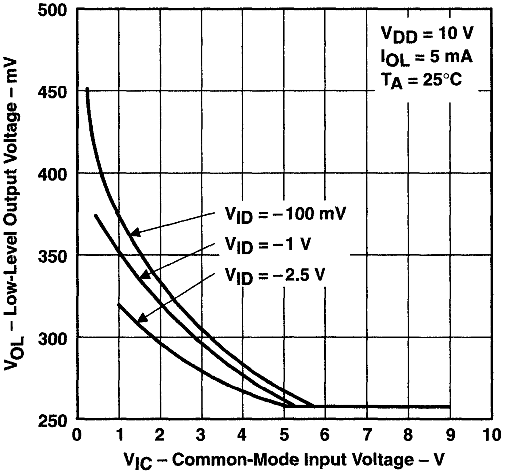

Figure 74

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

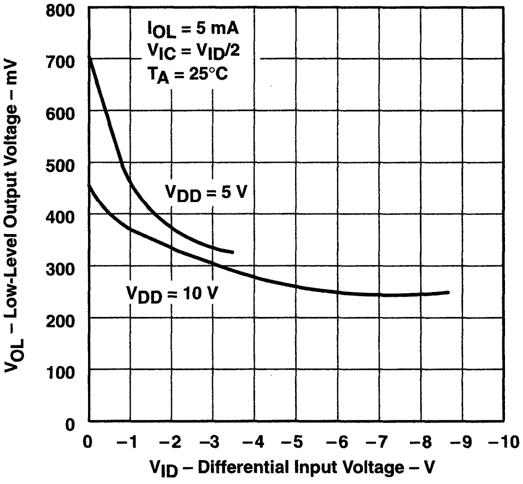

Figure 75

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

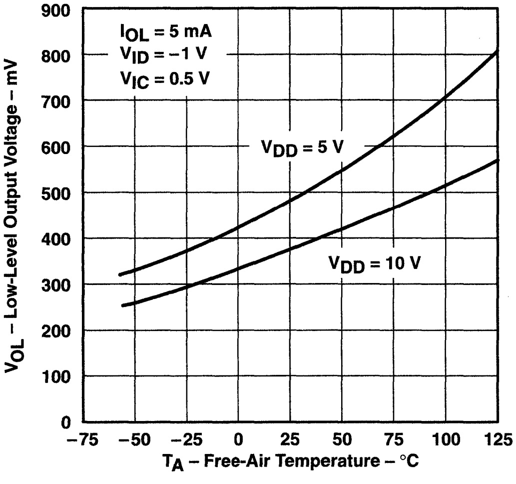

Figure 76

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

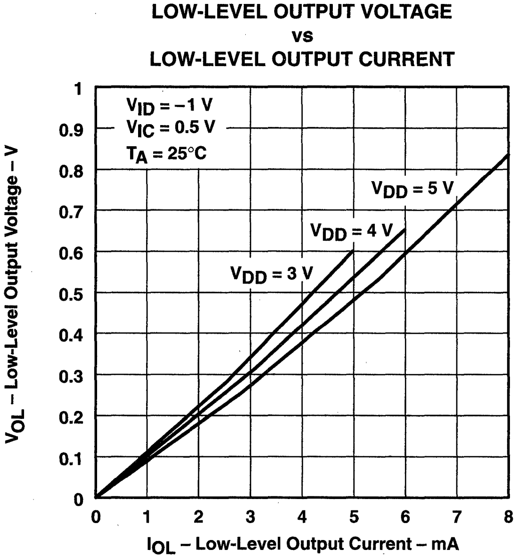

Figure 77

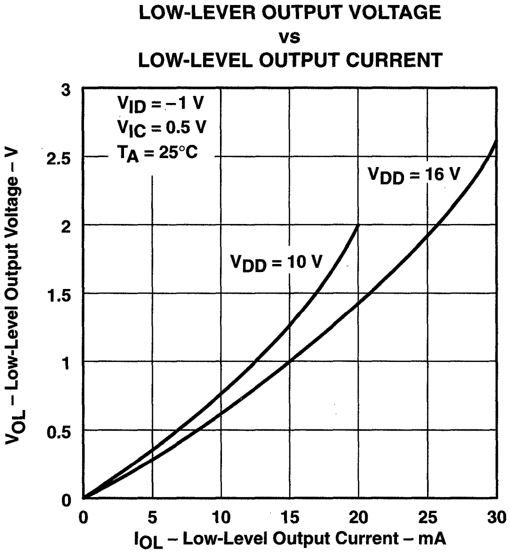

Figure 78

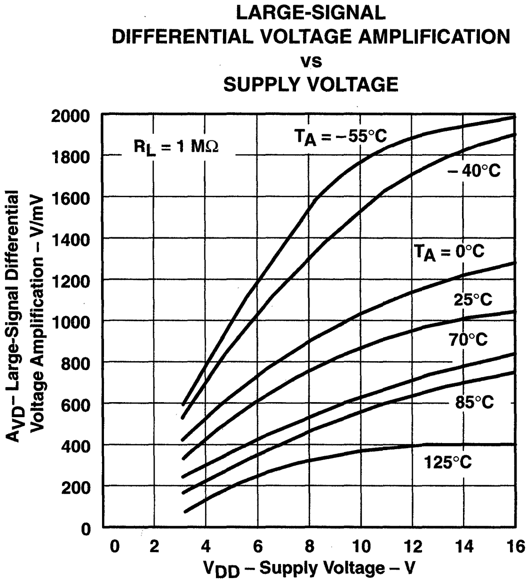

Figure 79

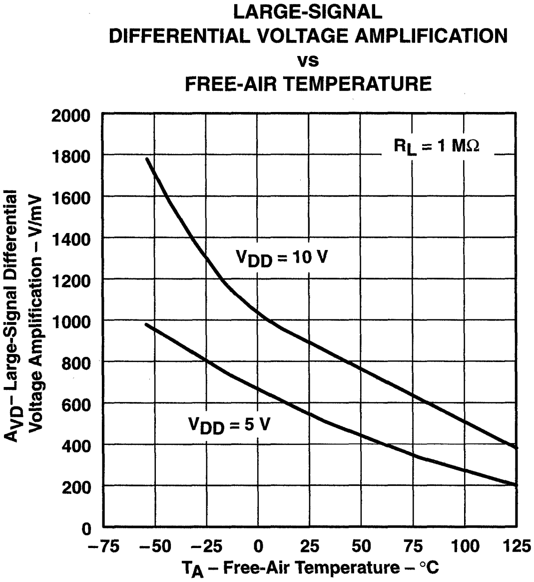

Figure 80

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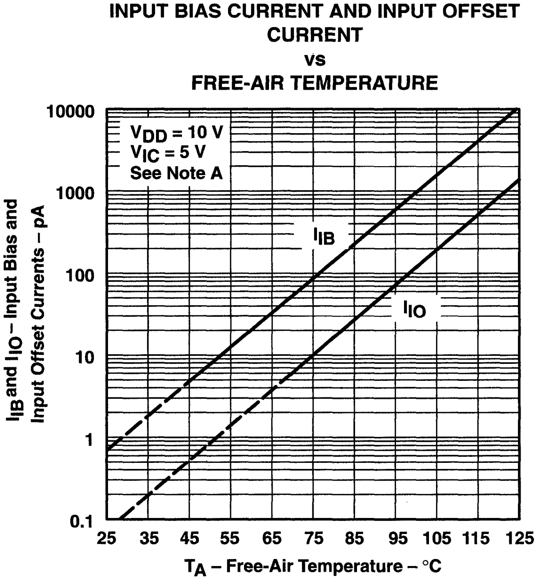
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 81

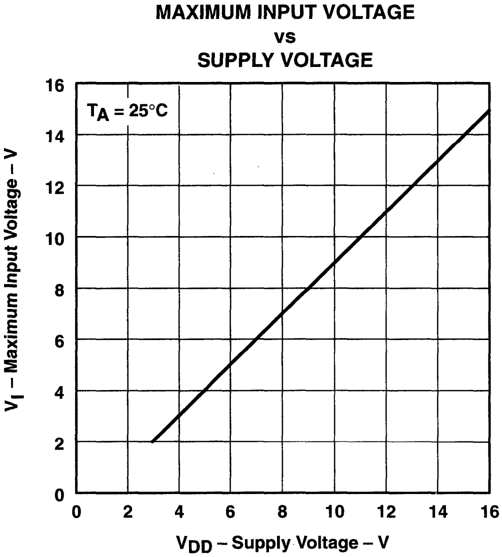


Figure 82

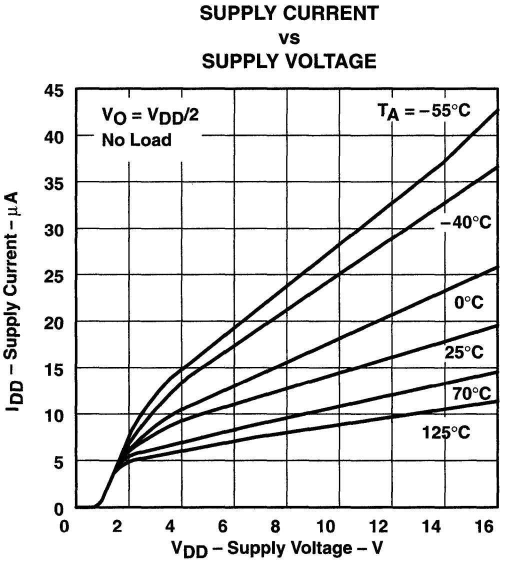


Figure 83

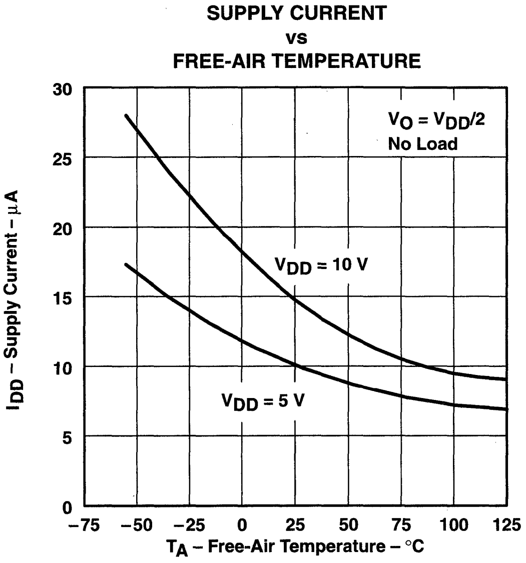


Figure 84

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

SLEW RATE
vs
SUPPLY VOLTAGE

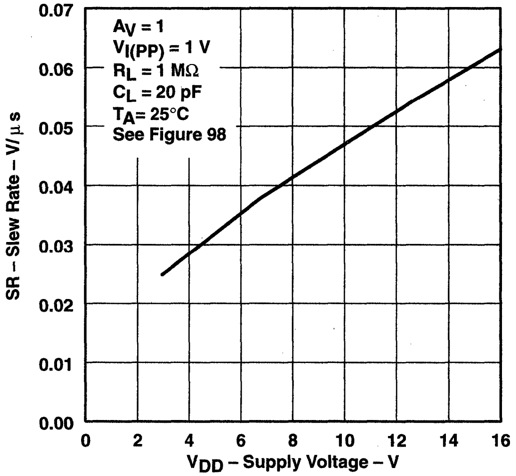

Figure 85

SLEW RATE
vs
FREE-AIR TEMPERATURE

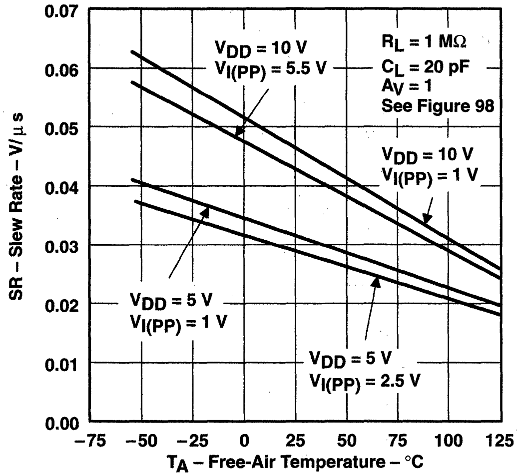

Figure 86

BIAS-SELECT CURRENT
vs
SUPPLY VOLTAGE

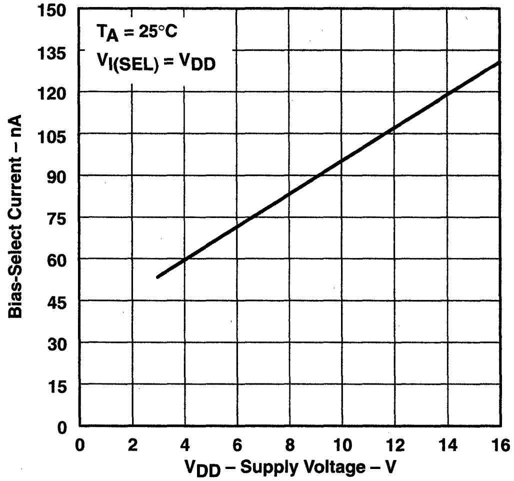

Figure 87

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

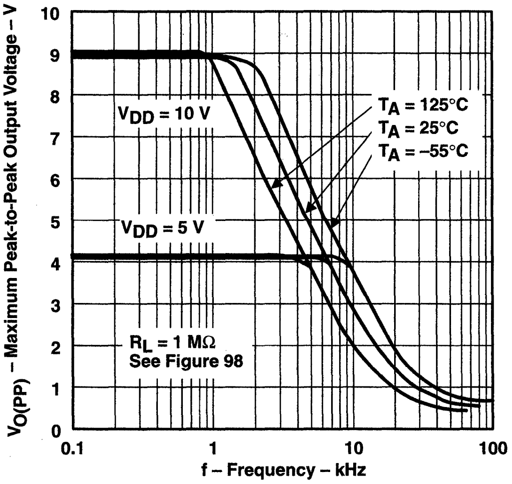

Figure 88

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

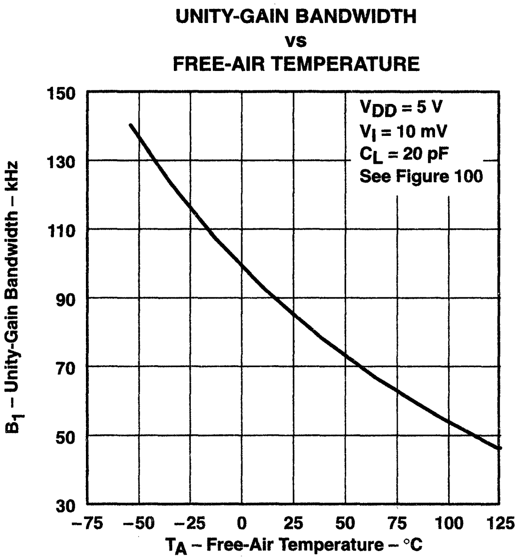

Figure 89

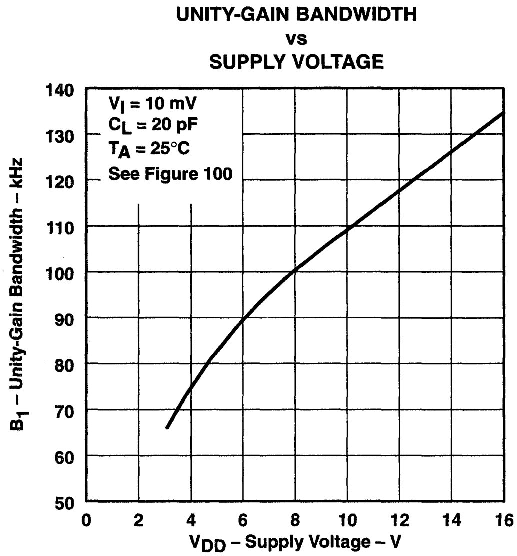

Figure 90

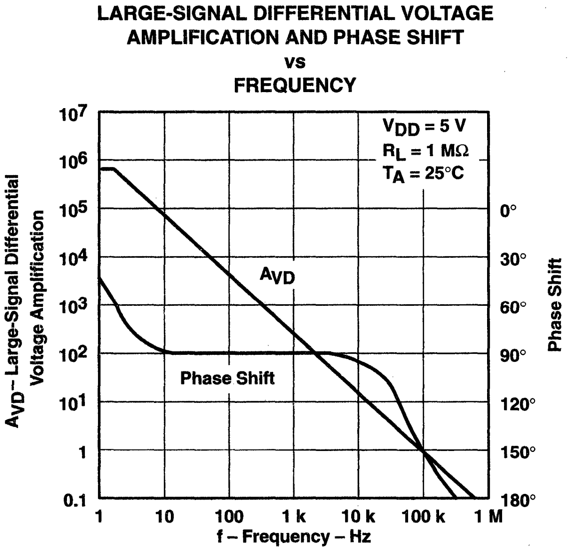

Figure 91

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

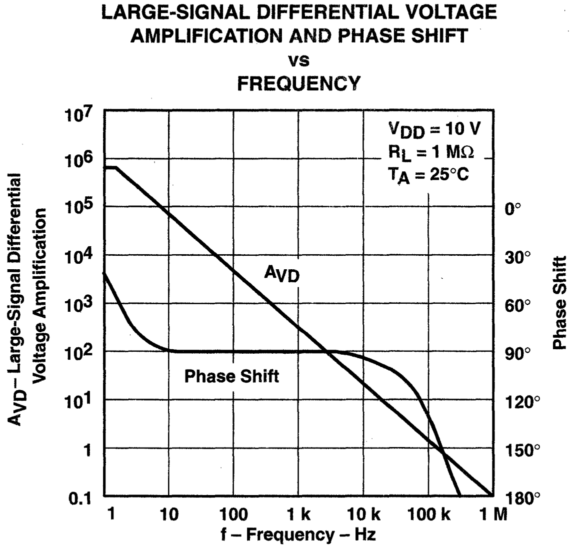

Figure 92

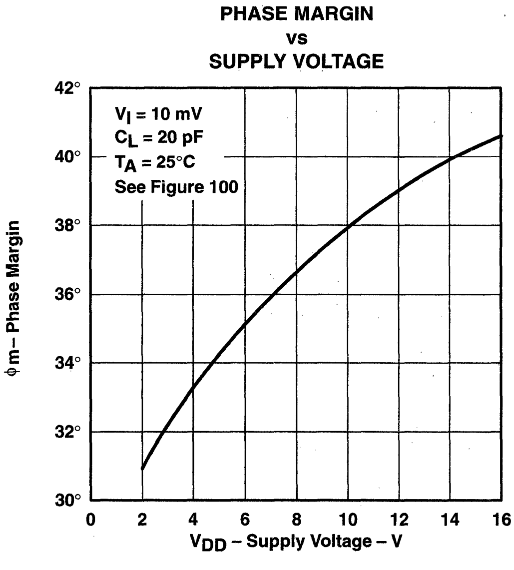

Figure 93

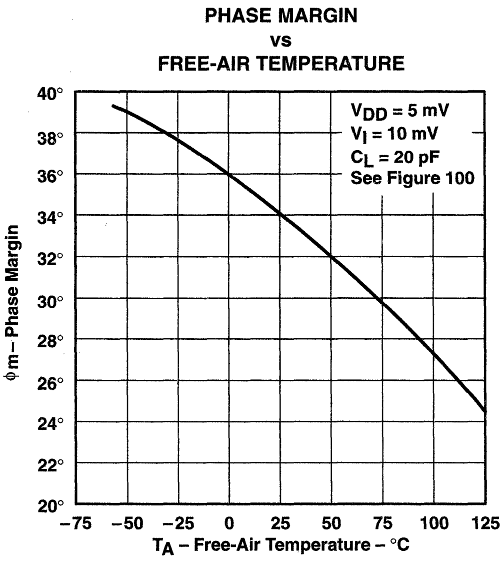

Figure 94

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

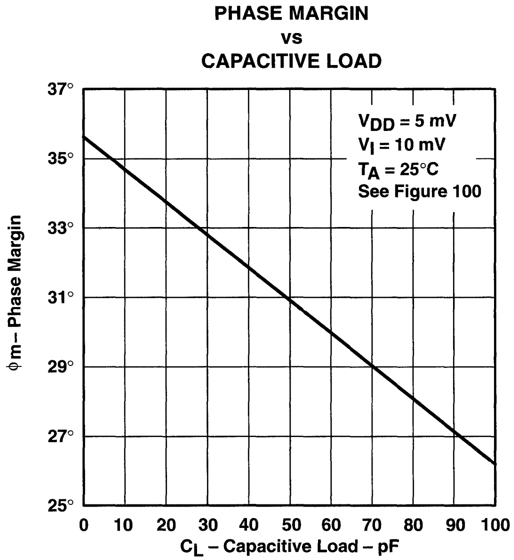

Figure 95

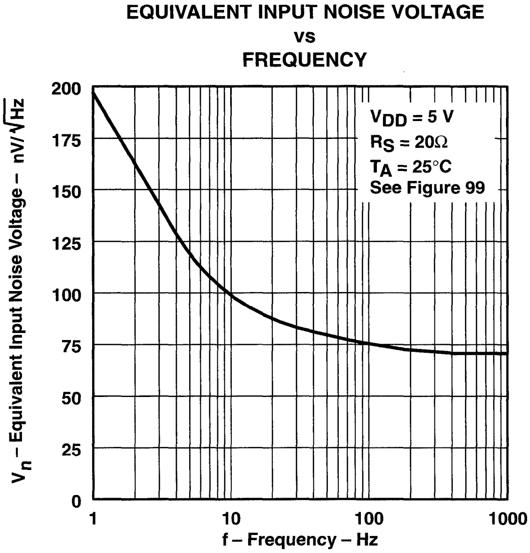

Figure 96

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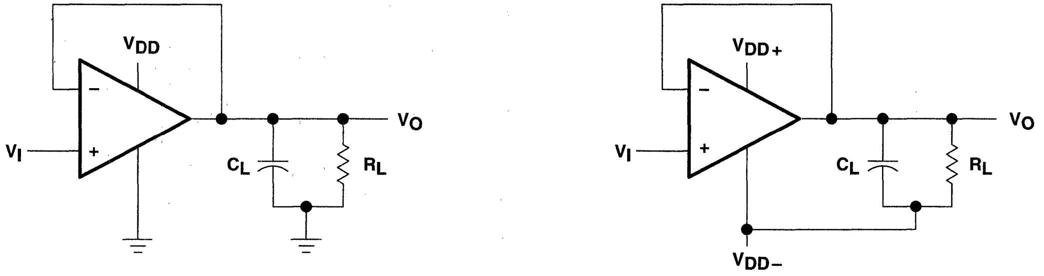
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PARAMETER MEASUREMENT INFORMATION

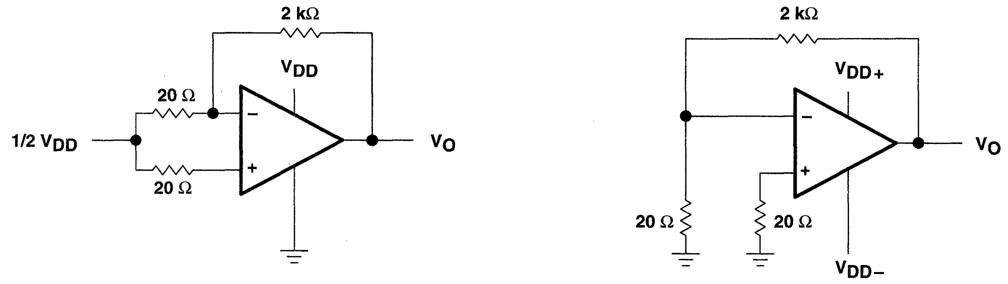
single-supply versus split-supply test circuits

Because the TLC271 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



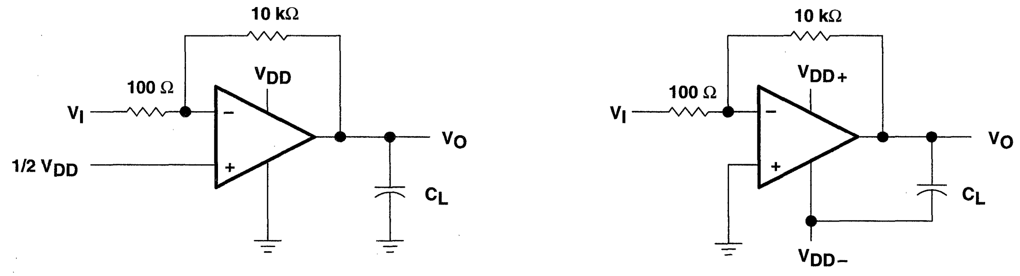
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 97. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 98. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 99. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC271 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 101). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers us the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

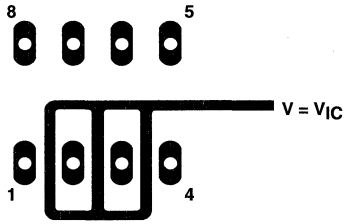


Figure 100. Isolation Metal Around Device inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measuredby monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 98. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 102). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

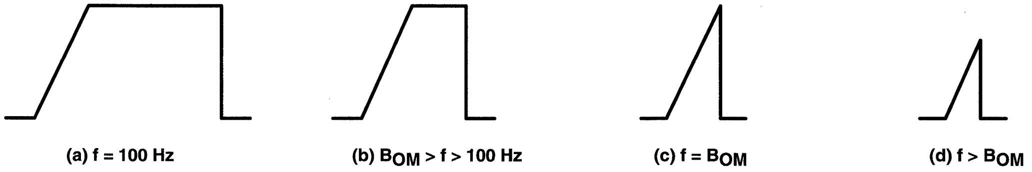

(a) f = 100 Hz　(b) $B_{OM} > f > 100$ Hz　(c) f = B_{OM}　(d) f > B_{OM}

Figure 101. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLC271 performs well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

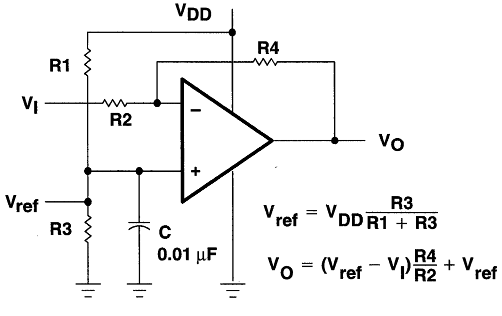


Figure 102. Inverting Amplifier With Voltage Reference

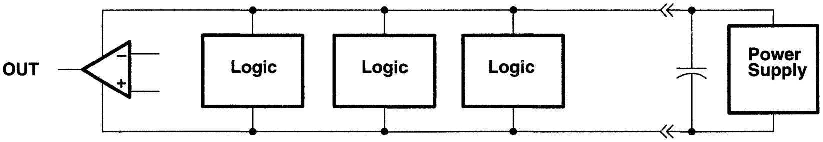
APPLICATION INFORMATION

single-supply operation (continued)

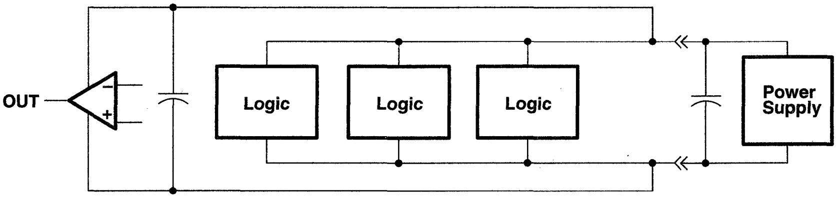
Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 103). The low input bias current consumption of the TLC271 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC271 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 104); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) COMMON SUPPLY RAILS



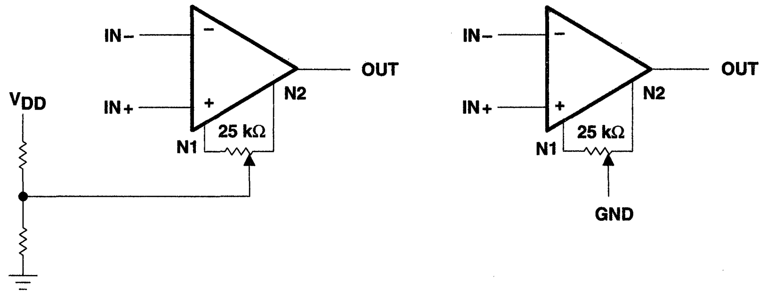
(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 103. Common Versus Separate Supply Rails

APPLICATION INFORMATION

input offset voltage nulling

The TLC271 offers external input offset null control. Nulling of the input off set voltage may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper Connected as shown in Figure 105. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range allows the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.

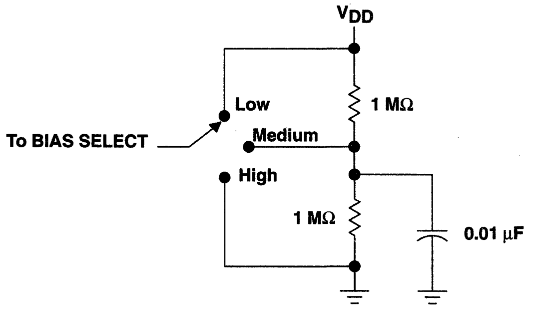


(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 104. Input Offset Voltage Null Circuit

bias selection

Bias selection is achieved by connecting the bias select pin to one of the three voltage levels (see Figure 106). For medium-bias applications, R is recommended that the bias select pin be connected to the mid-point between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor requires significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the table of Figure 106.



BIAS MODE	BIAS-SELECT VOLTAGE (single supply)
Low	V_{DD}
Medium	1 V to V_{DD} – 1 V
High	GND

Figure 105. Bias Selection for Single-Supply Applications

APPLICATION INFORMATION

input characteristics

The TLC271 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

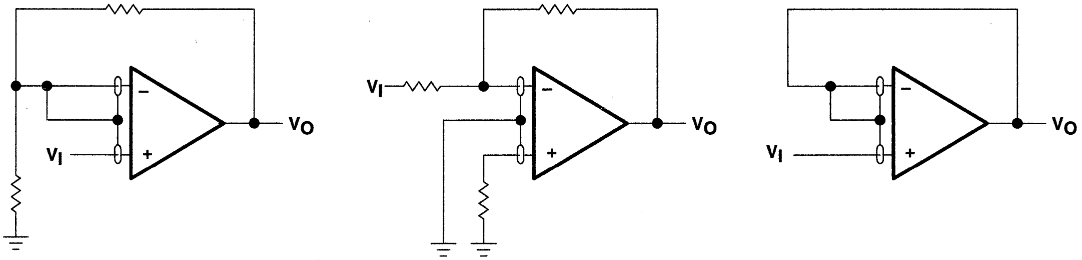
The use of the polysilicon-gate process and the careful input circuit design gives the TLC271 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC271 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 101 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 107).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC271 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 106. Guard-Ring Schemes

APPLICATION INFORMATION

feedback

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 108). The value of this capacitor is optimized empirically.

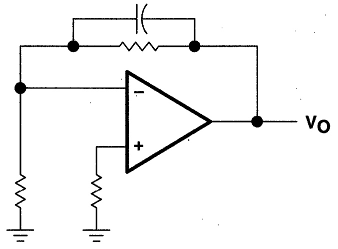


Figure 107. Compensation for Input Capacitance

electrostatic discharge protection

The TLC271 incorporates an internal electrostatic-discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC271 inputs and output were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLC271 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

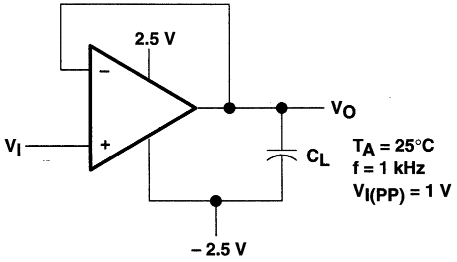
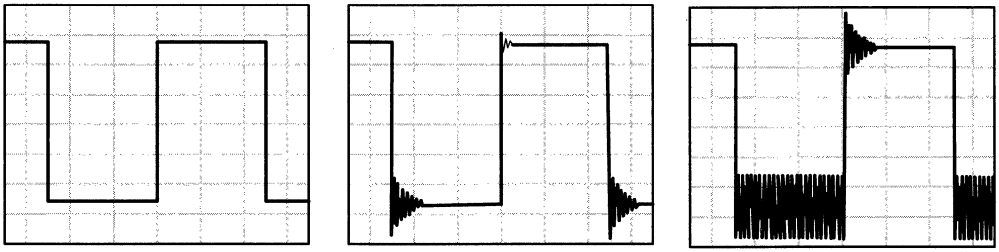


Figure 108. Test Circuit for Output Characteristics

APPLICATION INFORMATION

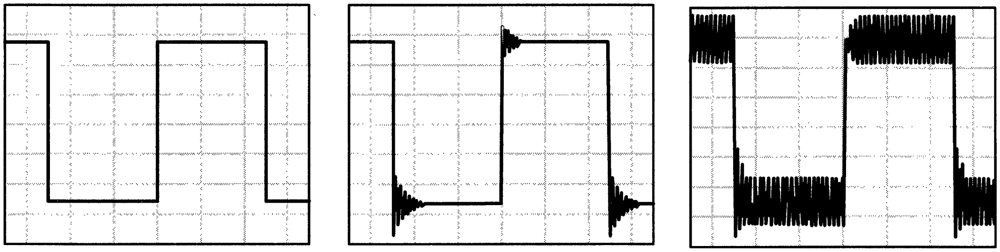
output characteristics (continued)

All operating characteristics of the TLC271 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 110, 111, and 112). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.



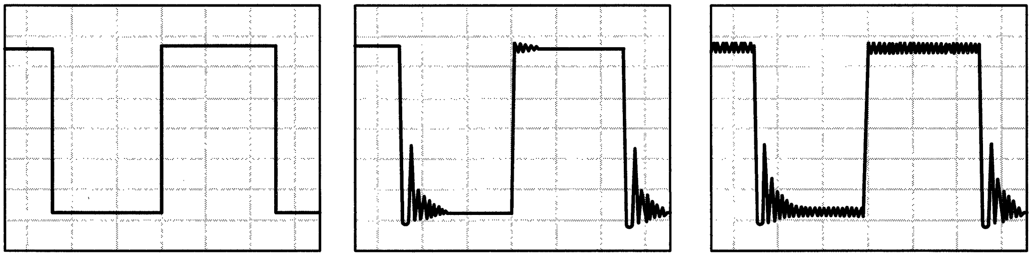
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

Figure 109. Effect of Capacitive Loads in High-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

Figure 110. Effect of Capacitive Loads in Medium-Bias Mode



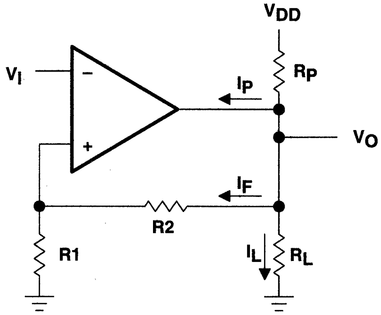
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

Figure 111. Effect of Capacitive Loads in Low-Bias Mode

APPLICATION INFORMATION

output characteristics (continued)

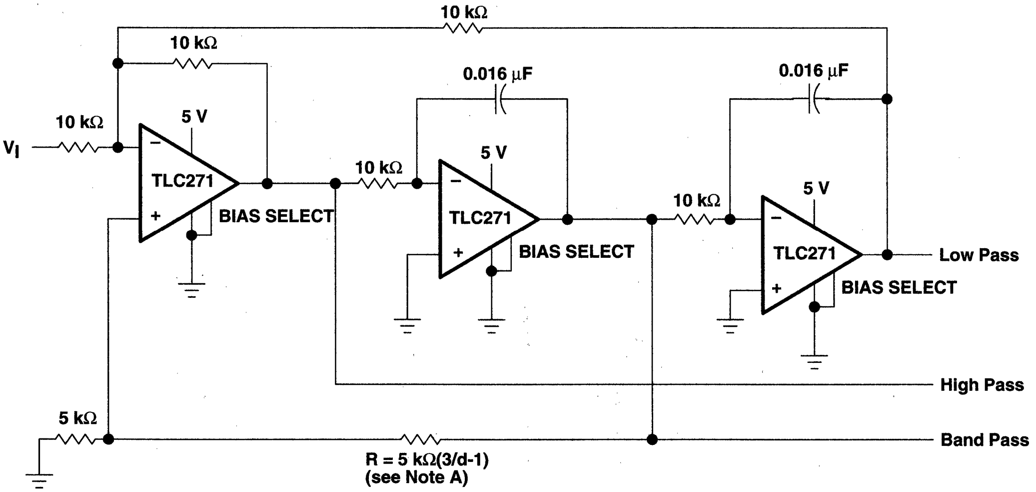
Although the TLC271 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 113). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor RP acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 μA)

Figure 112. Resistive Pullup to Increase V_{OH}

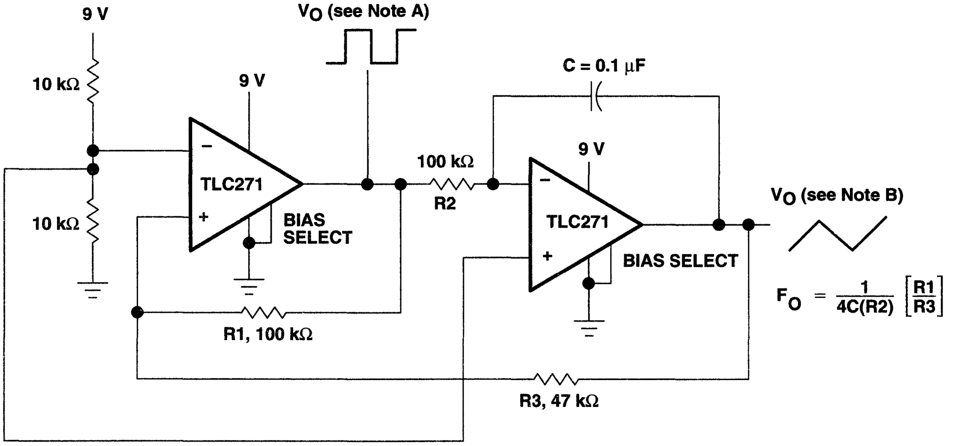


NOTE B: d = damping factor, I/O

Figure 113. State-Variable Filter

APPLICATION INFORMATION

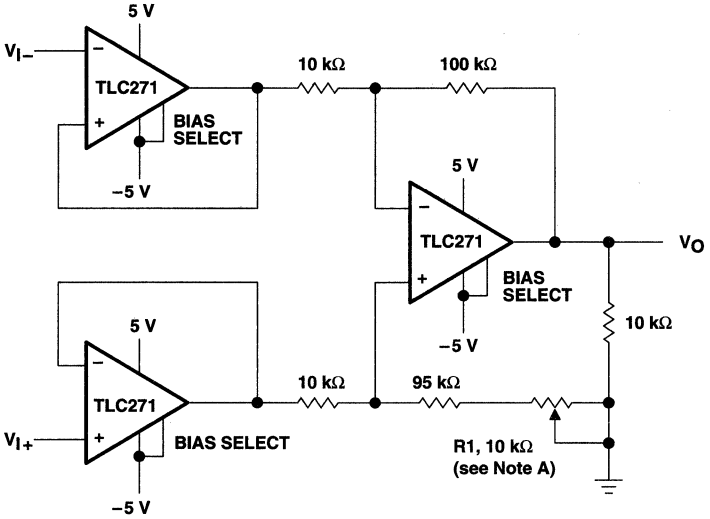
output characteristics (continued)



NOTES: A. $V_{O(PP)} = 8$ V
B. $V_{O(PP)} = 4$ V

Figure 114. Single-Supply Function Generator

APPLICATION INFORMATION (HIGH-BIAS MODE)



NOTE A: CMRR adjustment must be noninductive.

Figure 115. Low-Power Instrumentation Amplifier

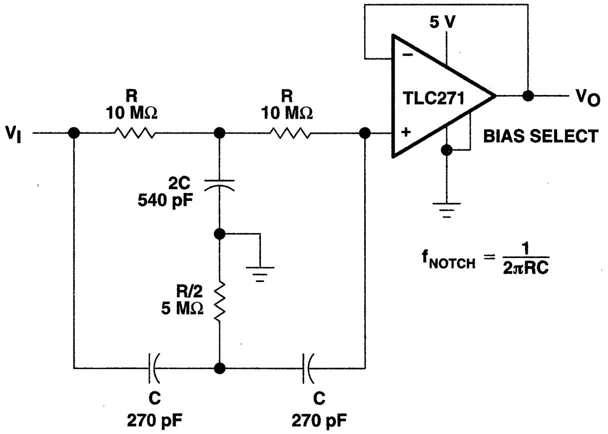
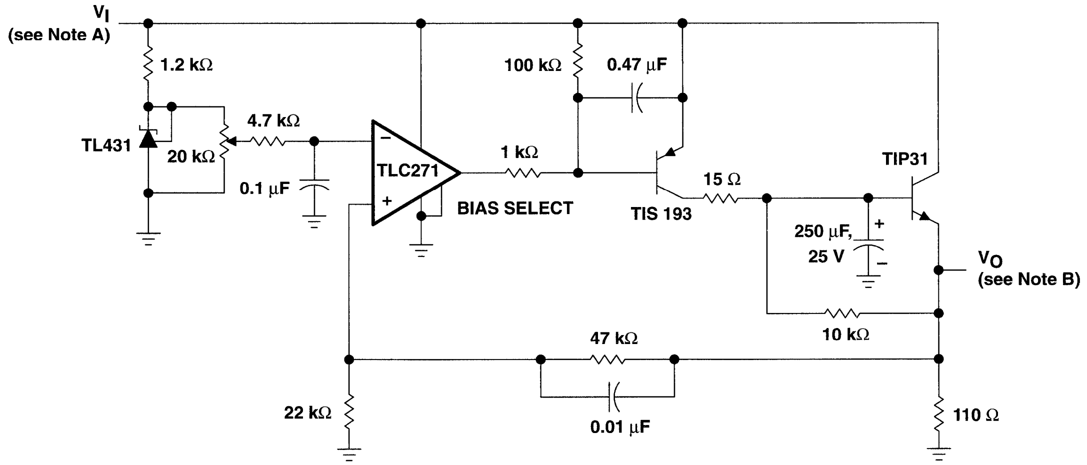


Figure 116. Single-Supply Twin-T Notch Filter

APPLICATION INFORMATION (HIGH-BIAS MODE)



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

Figure 117. Logic-Array Power Supply

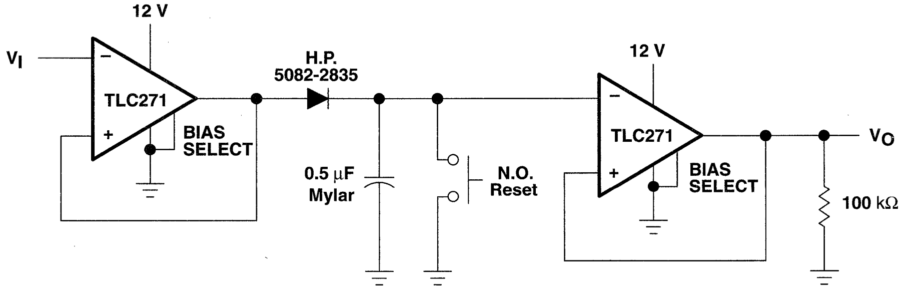
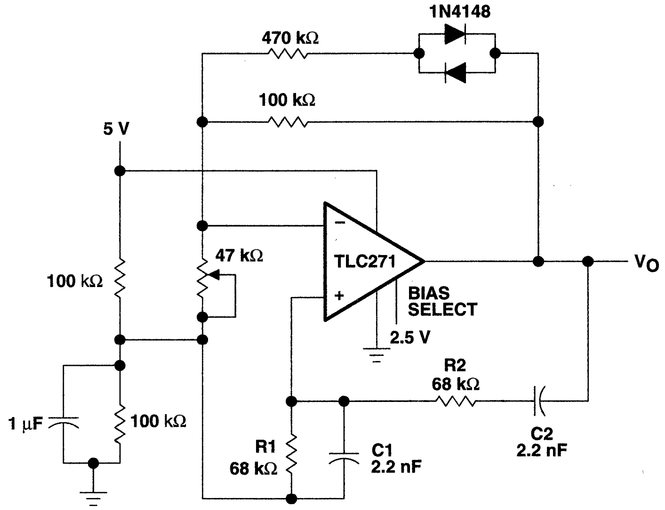


Figure 118. Positive-Peak Detector

APPLICATION INFORMATION (MEDIUM-BIAS MODE)



NOTES: A. $V_{O(PP)} = 2\text{ V}$

B. $f_o = \dfrac{1}{2\pi\sqrt{R1R2C1C2}}$

Figure 119. Wein Oscillator

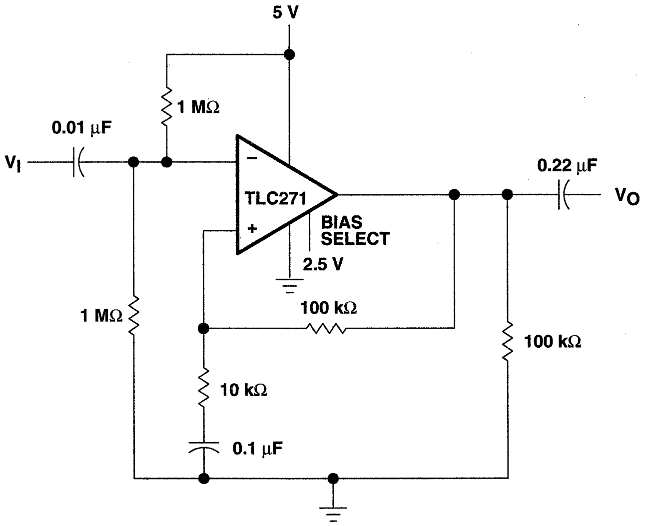
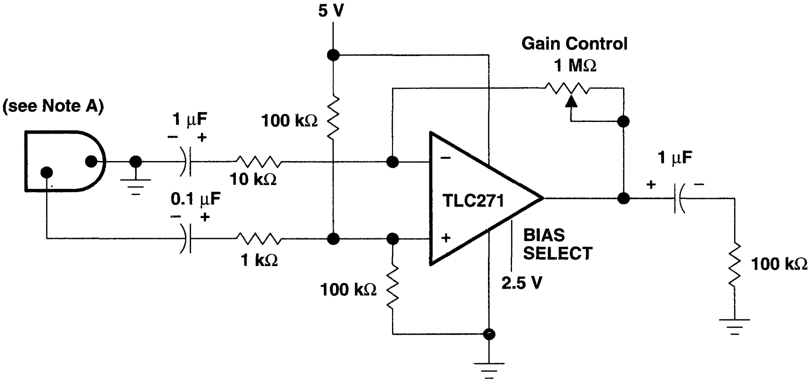


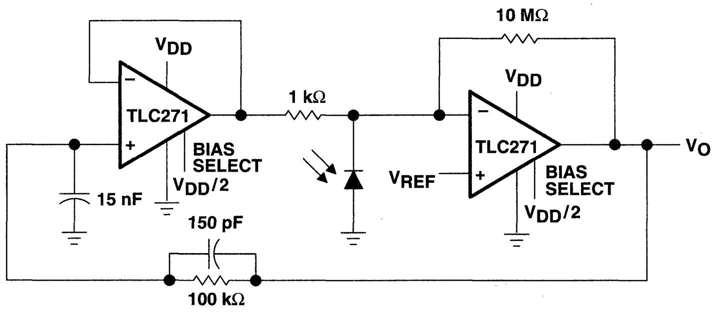
Figure 120. Single-Supply AC Amplifier

APPLICATION INFORMATION (MEDIUM-BIAS MODE)



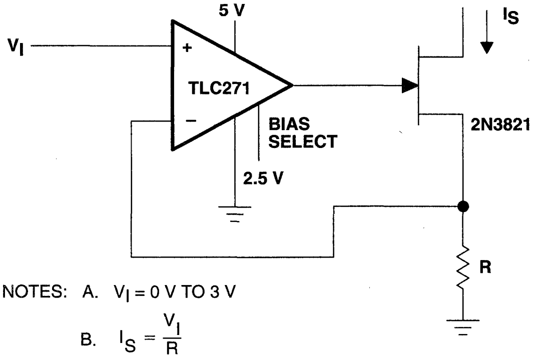
NOTE A: Low to medium impedance dynamic mike

Figure 121. Microphone Preamplifier



NOTES: A. NOTES: V_{DD} = 4 V to 15 V
B. V_{ref} = 0 V to V_{DD}−2 V

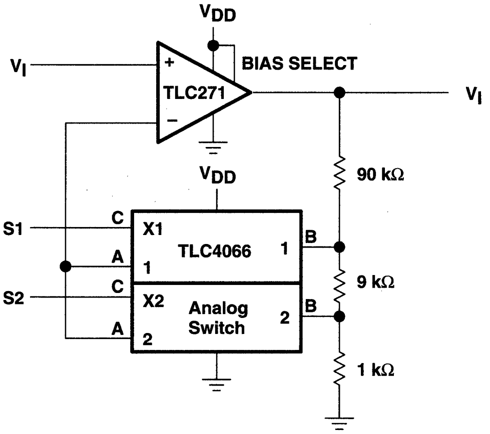
Figure 122. Photo-Diode Amplifier With Ambient Light Rejection



NOTES: A. V_I = 0 V TO 3 V
B. $I_S = \frac{V_I}{R}$

Figure 123. Precision Low-Current Sink

APPLICATION INFORMATION (LOW-BIAS MODE)



Select	S_1	S_2
A_V	10	100

NOTE A: V_{DD} = 5 V to 12 V

Figure 124. Amplifier With Digital Gain Selection

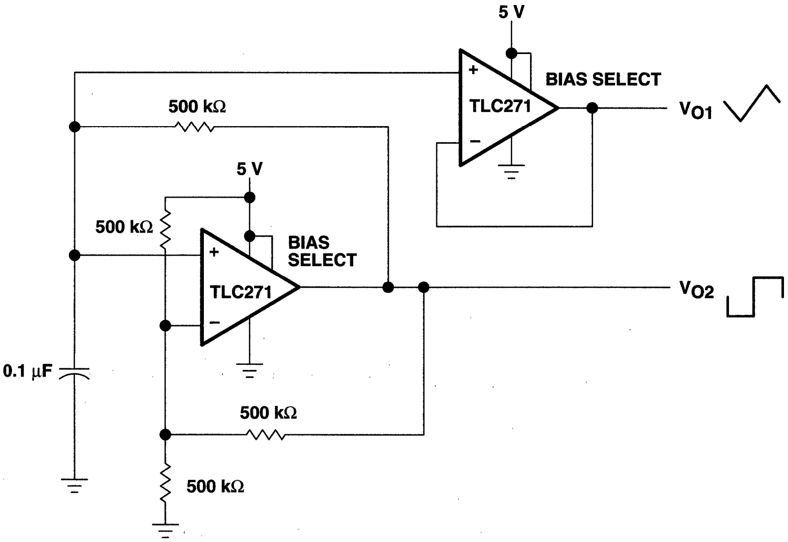
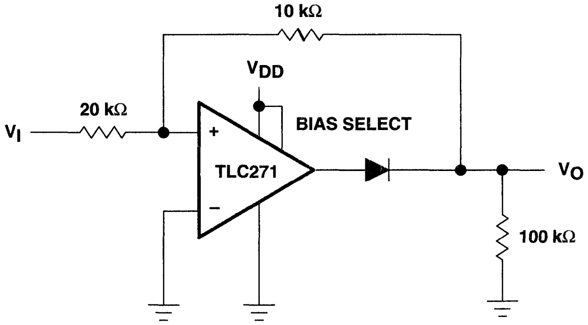


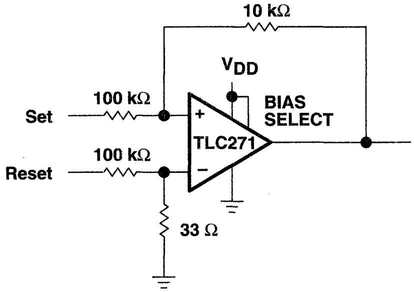
Figure 125. Multivibrator

APPLICATION INFORMATION (LOW-BIAS MODE)



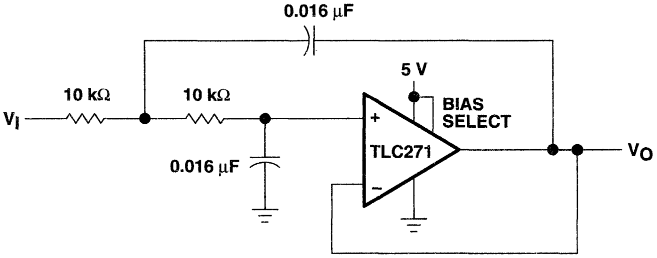
NOTE A: V_{DD} = 5 V to 16 V

Figure 126. Full-Wave Rectifier



NOTE A: V_{DD} = 5 V to 16 V

Figure 127. Set/Reset Flip-Flop



NOTE A: Normalized to F_C = 1 kHz and R_L = 10 kΩ

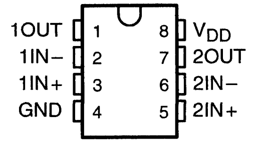
Figure 128. Two-Pole Low-Pass Butterworth Filter

TLC272, TLC272A, TLC272B, TLC272Y, TLC277
LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

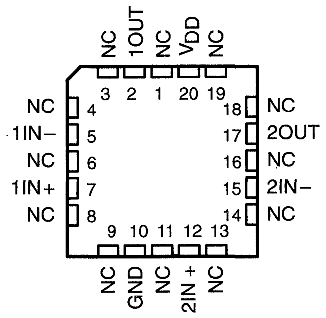
SLOS091B – OCTOBER 1987 – REVISED AUGUST 1994

- **Trimmed Offset Voltage:**
  TLC277 . . . 500 µV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 µV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  −55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-in Latch-Up Immunity**

D, JG, P, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

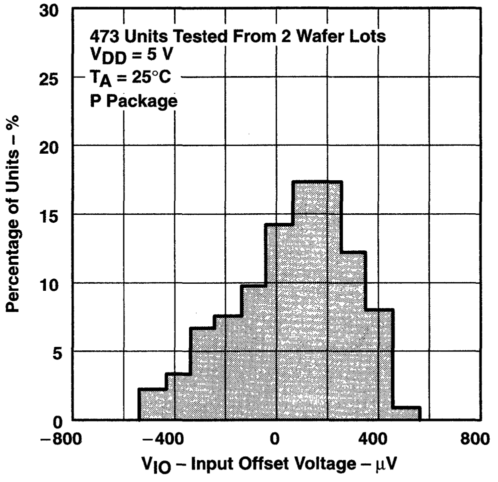
description

The TLC272 and TLC277 precision dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 µV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

DISTRIBUTION OF TLC277
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°c	500 µV 2 mV 5 mV 10mV	TLC277CD TLC272BCD TLC272ACD TLC272CD	— — — —	— — — —	TLC277CP TLC272BCP TLC272ACP TLC272CP	— — — TLC272CPW	— — — TLC272Y
−40°C to 85°C	500 µV 2 mV 5 mV 10 mV	TLC277ID TLC272BID TLC272AID TLC272ID	— — — —	— — — —	TLC277IP TLC272BIP TLC272AIP TLC272IP	— — — —	— — — —
−55°C to 125°C	500 µV 10 mV	TLC277MD TLC272MD	TLC277MFK TLC272MFK	TLC277MJG TLC272MJG	TLC277MP TLC272MP	— —	— —

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

description (continued)

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

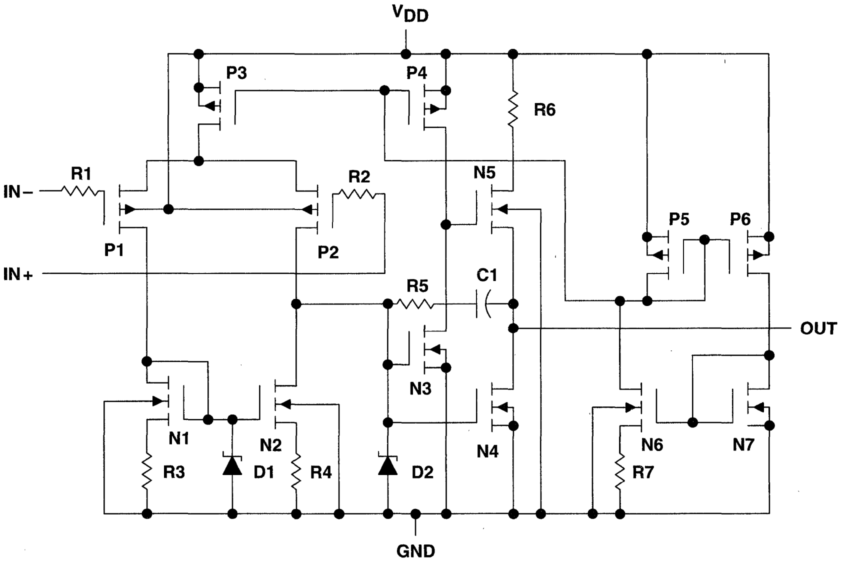
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

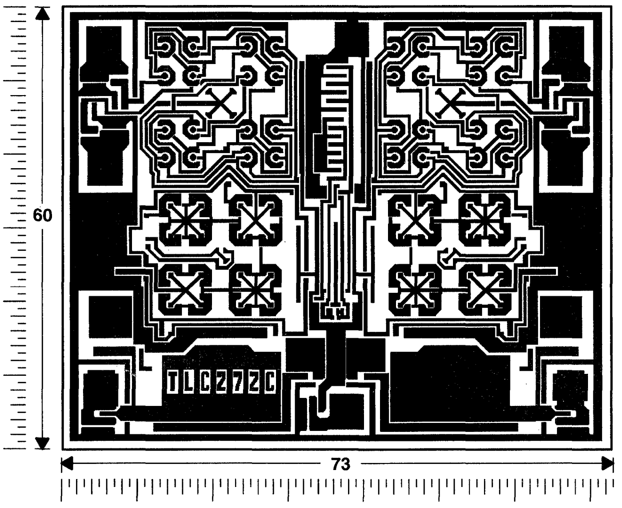
equivalent schematic (each amplifier)

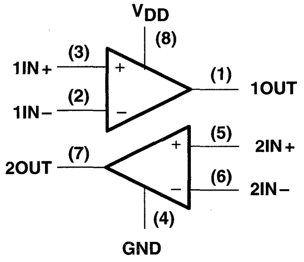


TLC272Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC272C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I	±5 mA
output current, I_O (each output)	±30 mA
Total current into V_{DD}	45 mA
Total current out of GND	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A
PW	525 mW	4.2 mW/°C	336 mW	N/A	N/A

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	−0.2	3.5	−0.2	3.5	0	3.5	V
	$V_{DD} = 10$ V	−0.2	8.5	−0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC272AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC272BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		230	2000	µV
				Full range			3000	
		TLC277C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		200	500	
				Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				0°C	3	3.8		
				70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				0°C	4	27		
				70°C	4	20		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	80		dB
				0°C	60	84		
				70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 5 V, No load	25°C		1.4	3.2	mA
				0°C		1.6	3.6	
				70°C		1.2	2.6	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC272AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC272BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		290	2000	µV
				Full range			3000	
		TLC277C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		250	800	
				Full range			1900	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				0°C	7.8	8.5		
				70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				0°C	7.5	42		
				70°C	7.5	32		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	85		dB
				0°C	60	88		
				70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 5 V, No load	25°C		1.9	4	mA
				0°C		2.3	4.4	
				70°C		1.6	3.4	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC272AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			7	
		TLC272BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		230	2000	μV
				Full range			3500	
		TLC277I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		200	500	
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	15	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	35	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				−40°C	3	3.8		
				85°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	5	23		V/mV
				−40°C	3.5	32		
				85°C	3.5	19		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	80		dB
				−40°C	60	81		
				85°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−40°C	60	92		
				85°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		1.4	3.2	mA
				−40°C		1.9	4.4	
				85°C		1.1	2.4	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC272AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			7	
		TLC272BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		290	2000	µV
				Full range			3500	
		TLC277I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		250	800	
				Full range			2900	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				−40°C	7.8	8.5		
				85°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				−40°C	7	46		
				85°C	7	31		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	85		dB
				−40°C	60	87		
				85°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−40°C	60	92		
				85°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		1.4	4	mA
				−40°C		2.8	5	
				85°C		1.5	3.2	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, $V_{DD} = 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC272M, TLC277M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272M	$V_O = 1.4$ V, $V_{IC} = 0$, $R_S = 50\ \Omega$, $R_L = 10\ k\Omega$	25°C		1.1	10	mV
				Full range			12	
		TLC277M	$V_O = 1.4$ V, $V_{IC} = 0$, $R_S = 50\ \Omega$, $R_L = 10\ k\Omega$	25°C		200	500	µV
				Full range			3750	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = 2.5$ V $V_{IC} = 2.5$ V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		$V_O = 2.5$ V $V_{IC} = 2.5$ V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		$V_{ID} = 100$ mV, $R_L = 10\ k\Omega$	25°C	3.2	3.8		V
				−55°C	3	3.8		
				125°C	3	3.8		
V_{OL}	Low-level output voltage		$V_{ID} = -100$ mV, $I_{OL} = 0$	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		$V_O = 0.25$ V to 2 V $R_L = 10\ k\Omega$	25°C	5	23		V/mV
				−55°C	3.5	35		
				125°C	3.5	16		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	80		dB
				−55°C	60	81		
				125°C	60	84		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 5$ V to 10 V, $V_O = 1.4$ V	25°C	65	95		dB
				−55°C	60	90		
				125°C	60	97		
I_{DD}	Supply current (two amplifiers)		$V_O = 2.5$ V, $V_{IC} = 2.5$ V, No load	25°C		1.4	3.2	mA
				−55°C		2	5	
				125°C		1	2.2	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC272M, TLC277M			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V,	V_{IC} = 0,	25°C		1.1	10	mV
			R_S = 50 Ω,	R_L = 10 kΩ	Full range			12	
		TLC277M	V_O = 1.4 V,	V_{IC} = 0,	25°C		250	800	µV
			R_S = 50 Ω,	R_L = 10 kΩ	Full range			4300	
α_{VIO}	Temperature coefficient of input offset voltage				25°C to 125°C		2.2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−55°C	7.8	8.5		
					125°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−55°C	7	50		
					125°C	7	27		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min		25°C	65	85		dB
					−55°C	60	87		
					125°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−55°C	60	90		
					125°C	60	97		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					−55°C		3	6	
					125°C		1.3	2.8	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC272Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage				1.8		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 2.5 V,	V_{IC} = 2.5 V		0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 2.5 V,	V_{IC} = 2.5 V		0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 10 kΩ	3.2	3.8		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V to 2 V	R_L = 10 kΩ	5	23		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V,	V_O = 1.4 V	65	95		dB
I_{DD}	Supply current (two amplifiers)	V_O = 2.5 V, No load	V_{IC} = 2.5 V,		1.4	3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC272Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage				1.8		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 5 V,	V_{IC} = 5 V		0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 5 V,	V_{IC} = 5 V		0.7		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 9	−0.3 to 9.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 10 kΩ	8	8.5		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 6 V,	R_L = 10 kΩ	10	36		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		65	85		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V,	V_O = 1.4 V	65	95		dB
I_{DD}	Supply current (two amplifiers)	V_O = 5 V, No load	V_{IC} = 5 V,		1.9	4	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				0°C		47°		
				70°C		43°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				0°C		50°		
				70°C		46°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−40°C		4.5		
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				−40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−40°C		380		
				85°C		250		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−40°C		49°		
				85°C		43°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−40°C		6.8		
				85°C		4		
			V_{IPP} = 5.5 V	25°C		4.6		
				−40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−40°C		52°		
				85°C		46°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC272M, TLC277M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC272M, TLC277M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−55°C		52°		
				125°C		44°		

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC272Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V		3.6		V/μs
			V_{IPP} = 2.5 V		2.9		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2			25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1			320		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3			1.7		MHz
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3			46°		

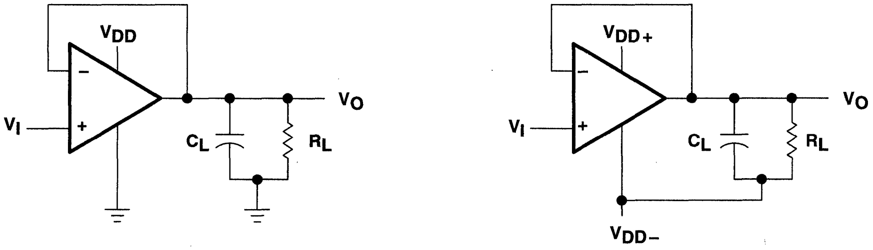
operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC272Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V		5.3		V/μs
			V_{IPP} = 5.5 V		4.6		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω, See Figure 2			25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1			200		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3			2.2		MHz
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3			49°		

PARAMETER MEASUREMENT INFORMATION

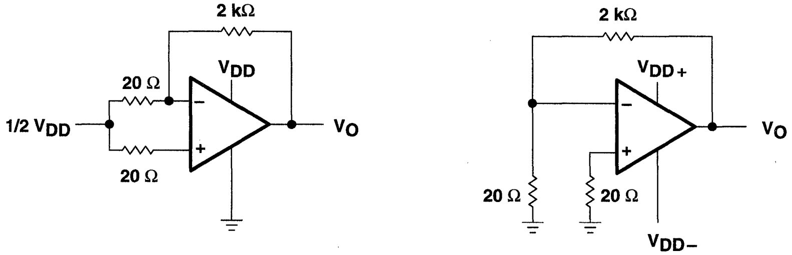
single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



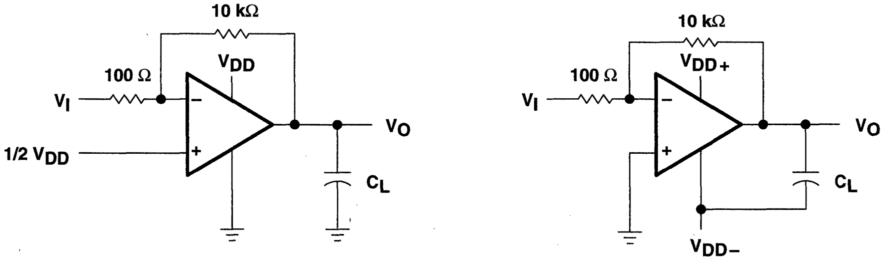
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC272 and TLC277 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

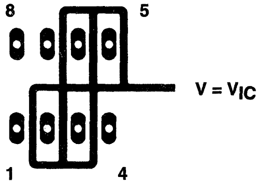


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

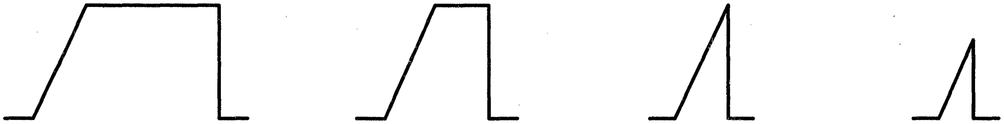
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 1 kHz (b) B_{OM} > f > 1 kHz (c) f = B_{OM} (d) f > B_{OM}

Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I_{IB}	Input bias current	vs Free-air temperature	22
I_{IO}	Input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
V_n	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC272 INPUT OFFSET VOLTAGE

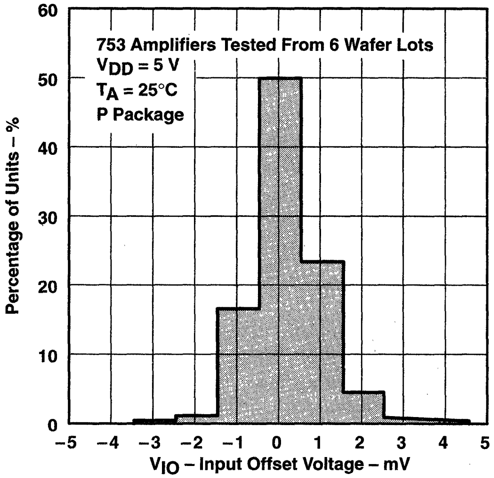


Figure 6

DISTRIBUTION OF TLC272 INPUT OFFSET VOLTAGE

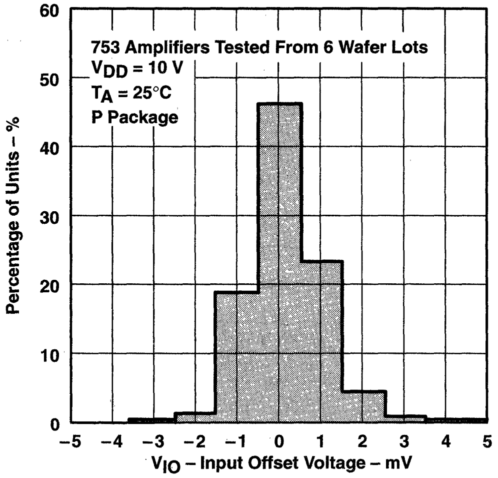


Figure 7

DISTRIBUTION OF TLC272 AND TLC277 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

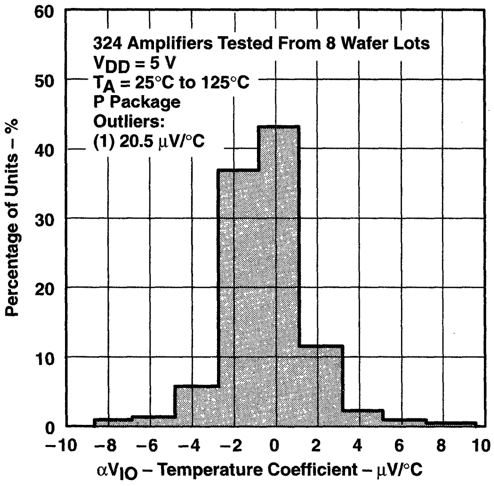


Figure 8

DISTRIBUTION OF TLC272 AND TLC277 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

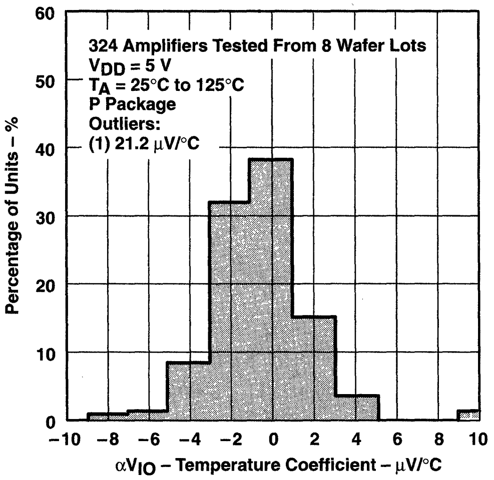
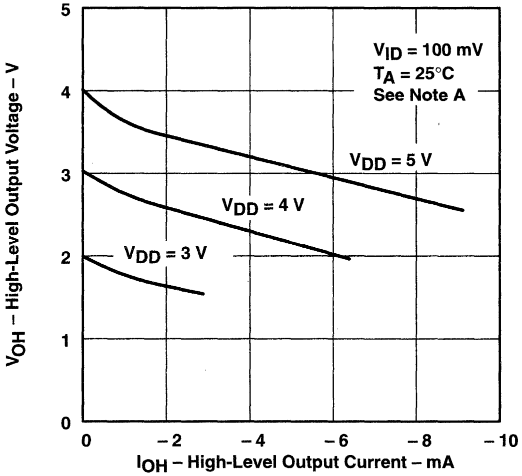


Figure 9

TYPICAL CHARACTERISTICS†

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**



NOTE A: The 3-V curve only applies to the C version.

Figure 10

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

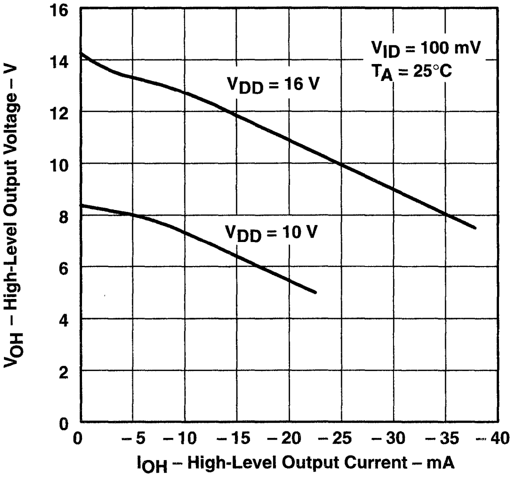


Figure 11

**HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE**

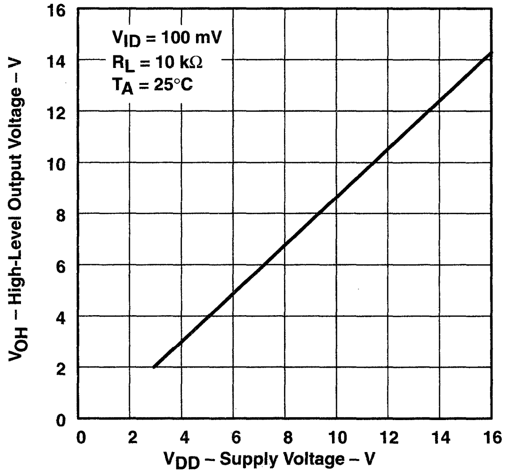


Figure 12

**HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

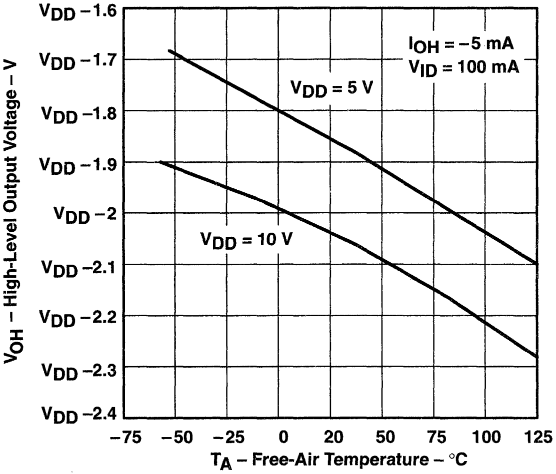


Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

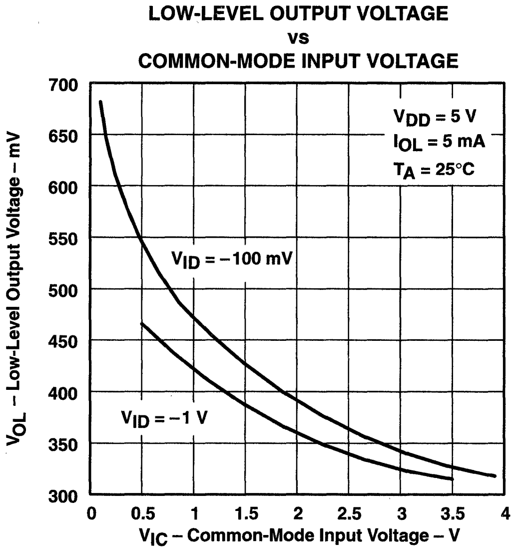

Figure 14

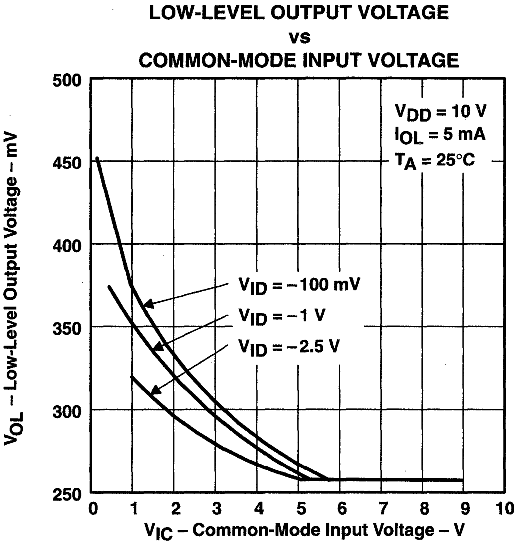

Figure 15

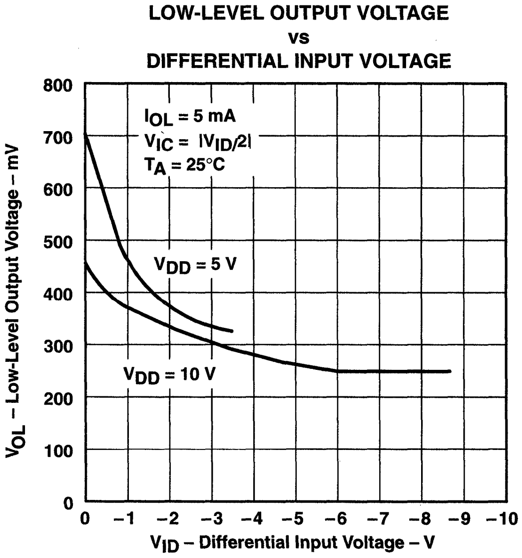

Figure 16

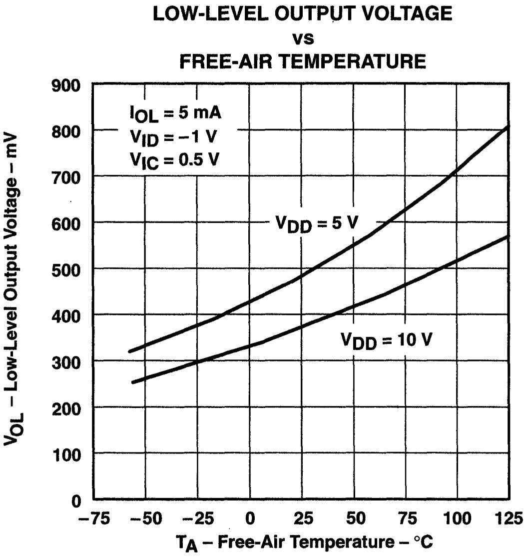

Figure 17

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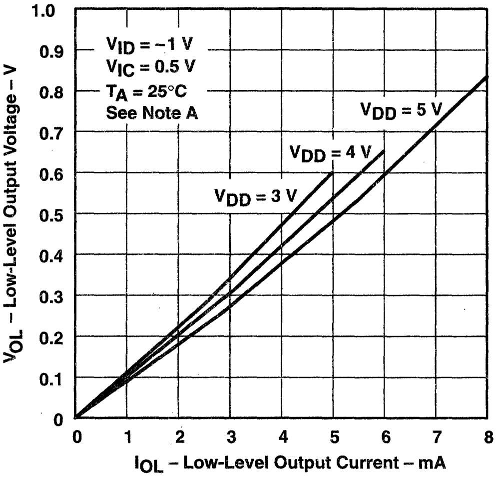
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT



NOTE A: The 3-V curve only applies to the C version.

Figure 18

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

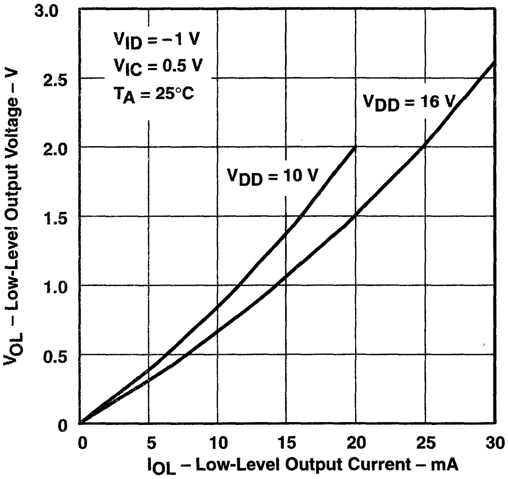


Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

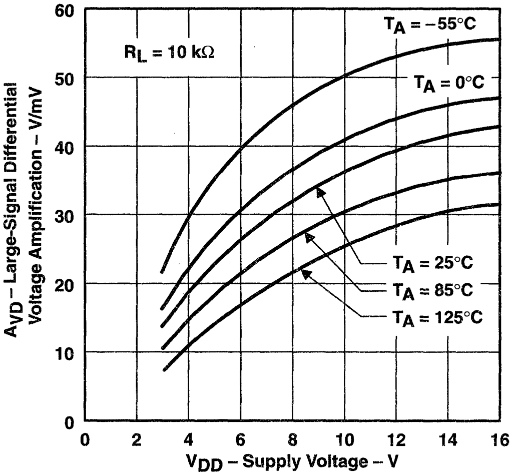


Figure 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

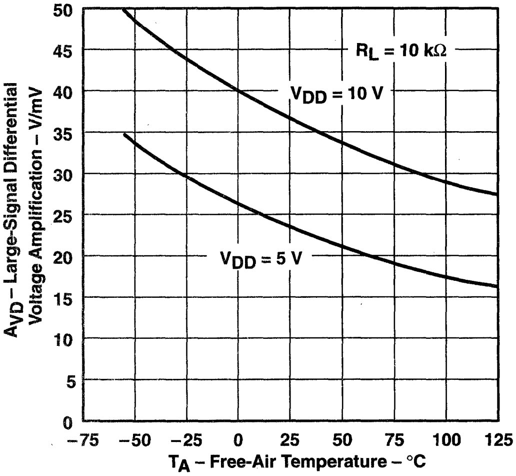


Figure 21

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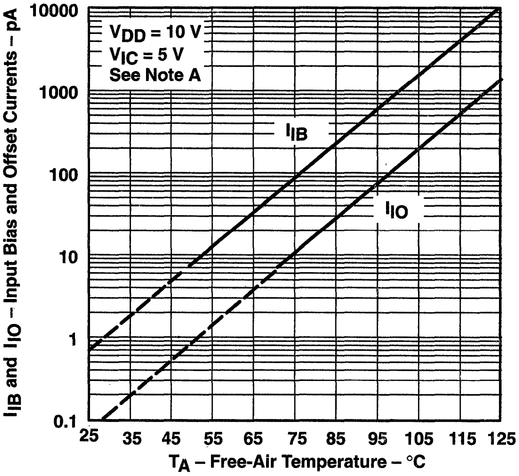
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

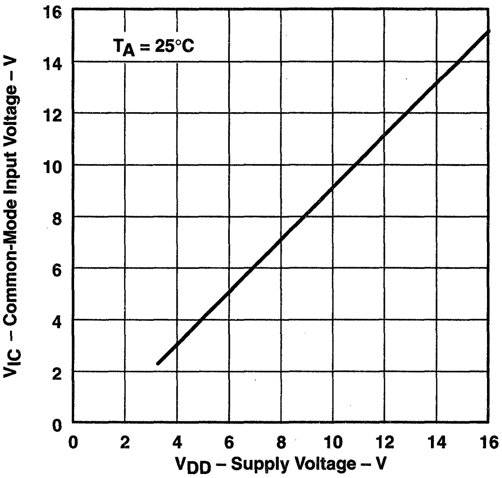


Figure 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

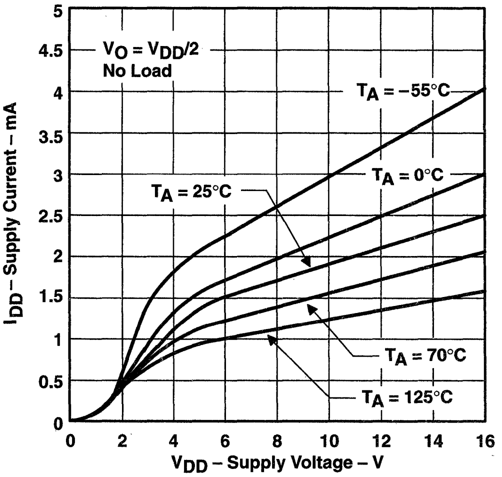


Figure 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

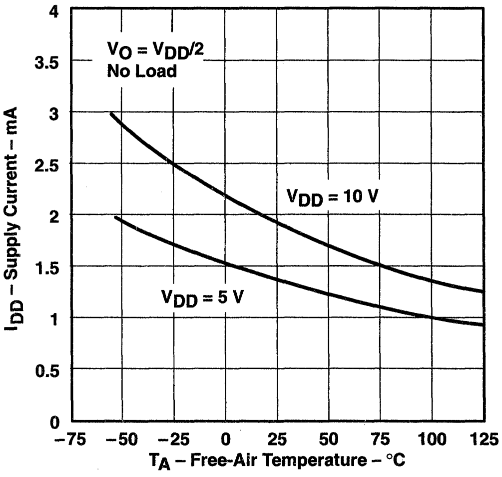


Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

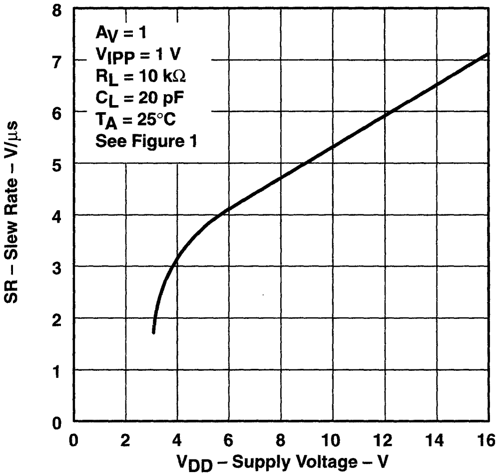

Figure 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

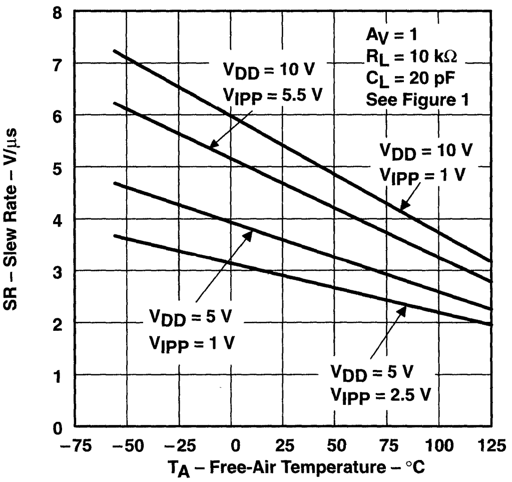

Figure 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

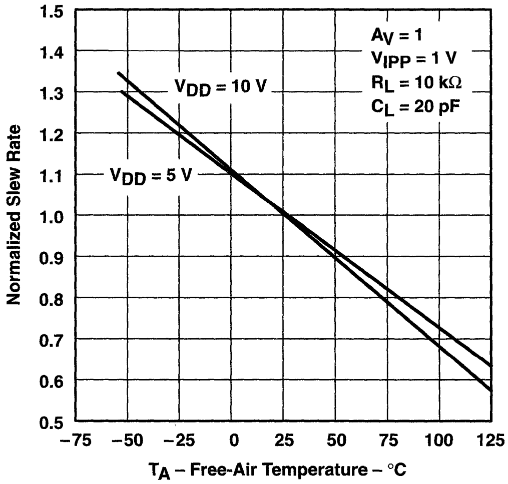

Figure 28

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

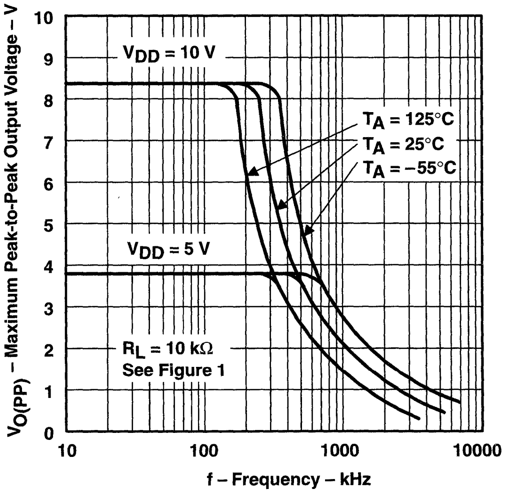

Figure 29

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

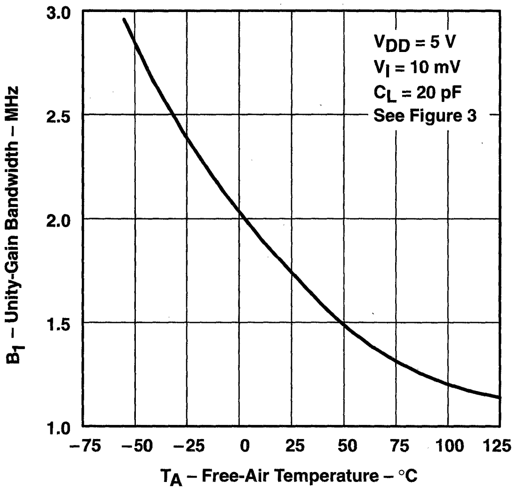

Figure 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

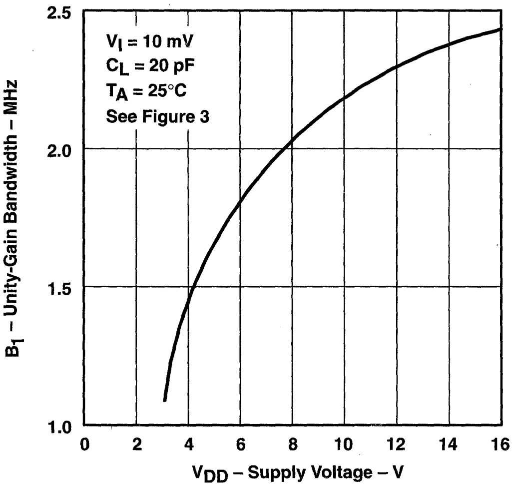

Figure 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

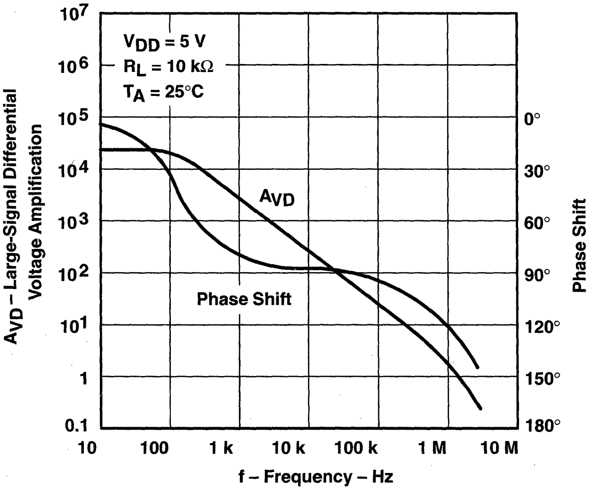

Figure 32

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

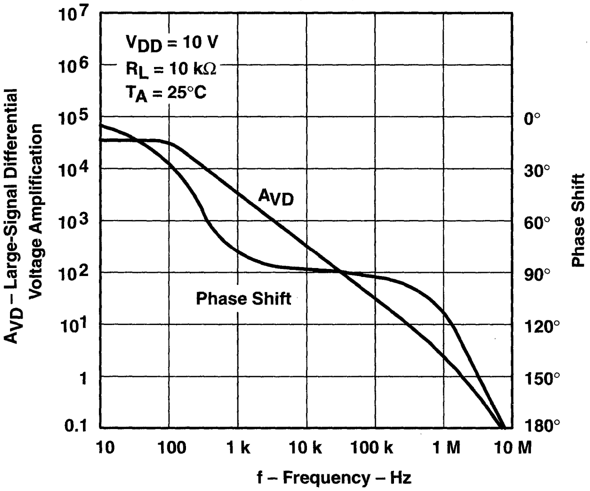

Figure 33

PHASE MARGIN vs SUPPLY VOLTAGE

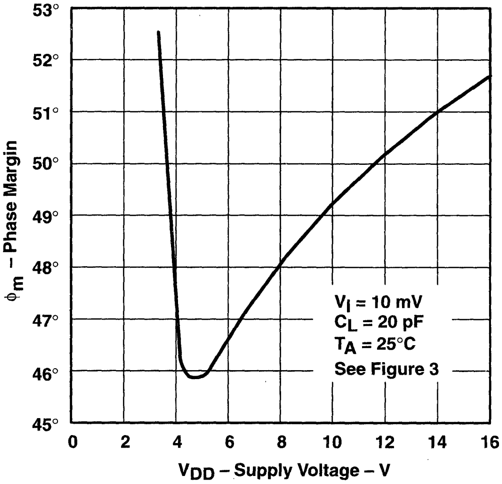

Figure 34

PHASE MARGIN vs FREE-AIR TEMPERATURE

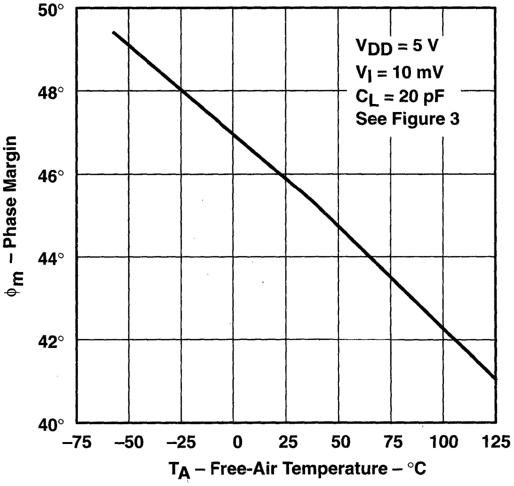

Figure 35

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

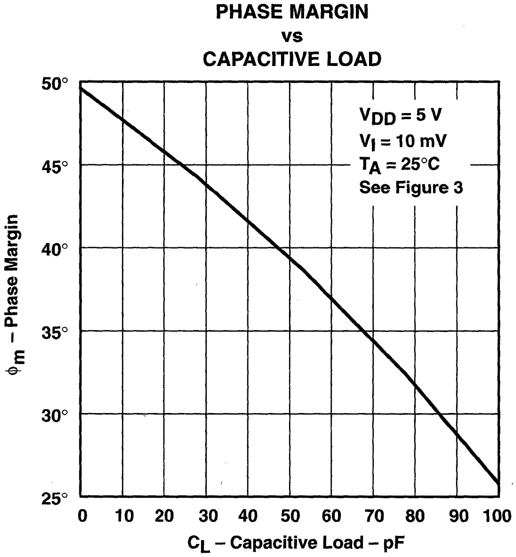


Figure 36

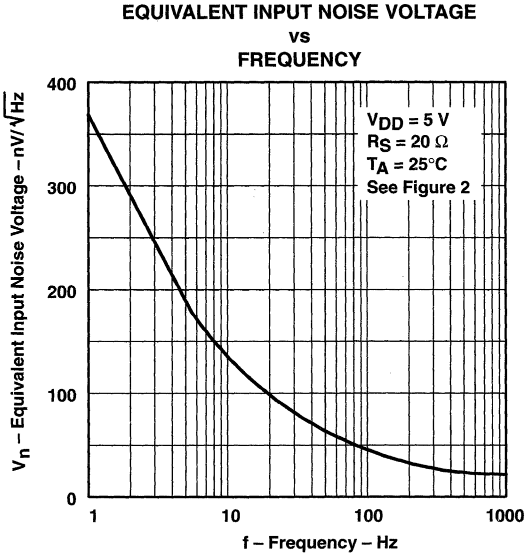


Figure 37

APPLICATION INFORMATION

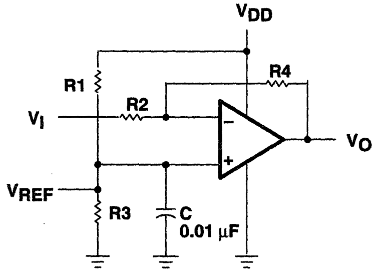
single-supply operation

While the TLC272 and TLC277 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

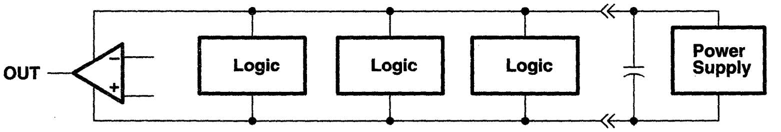
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



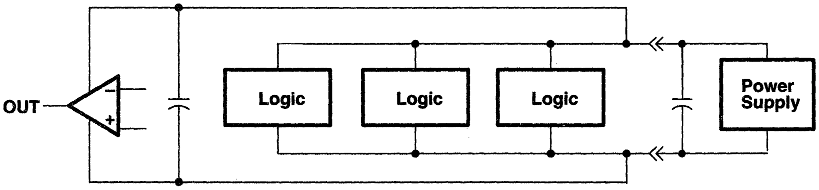
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = (V_{REF} - V_I)\frac{R4}{R2} + V_{REF}$$

Figure 38. Inverting Amplifier With Voltage Reference



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common vs Separate Supply Rails

APPLICATION INFORMATION

input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

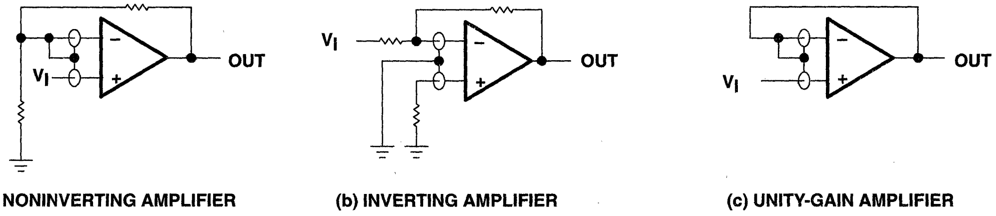
The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 40. Guard-Ring Schemes

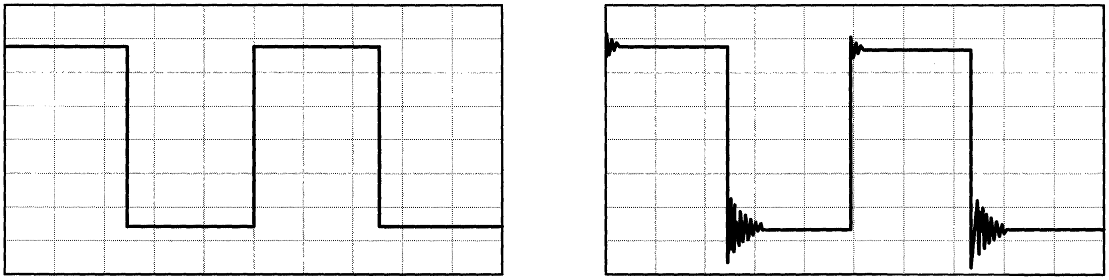
output characteristics

The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC272 and TLC277 are measured using a 20-pF load. The devices can drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

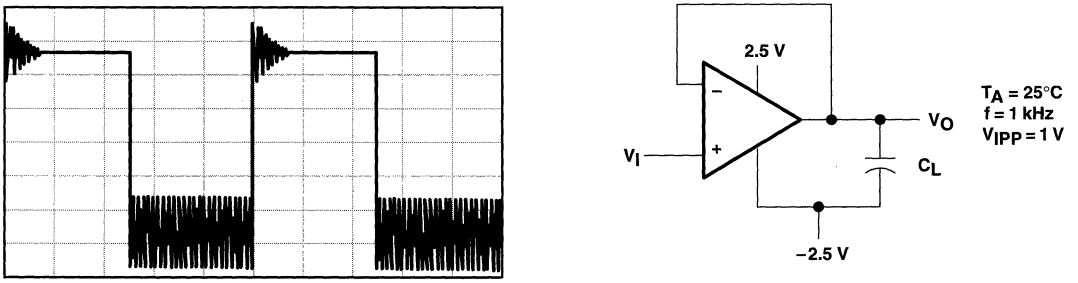
APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 130 pF, R_L = NO LOAD



(c) C_L = 150 pF, R_L = NO LOAD

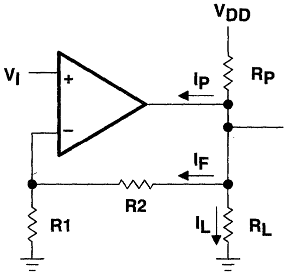
(d) TEST CIRCUIT

Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

APPLICATION INFORMATION

output characteristics (continued)



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 μA)

Figure 42. Resistive Pullup to Increase V_{OH}

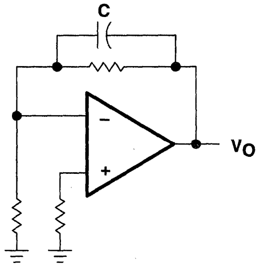


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

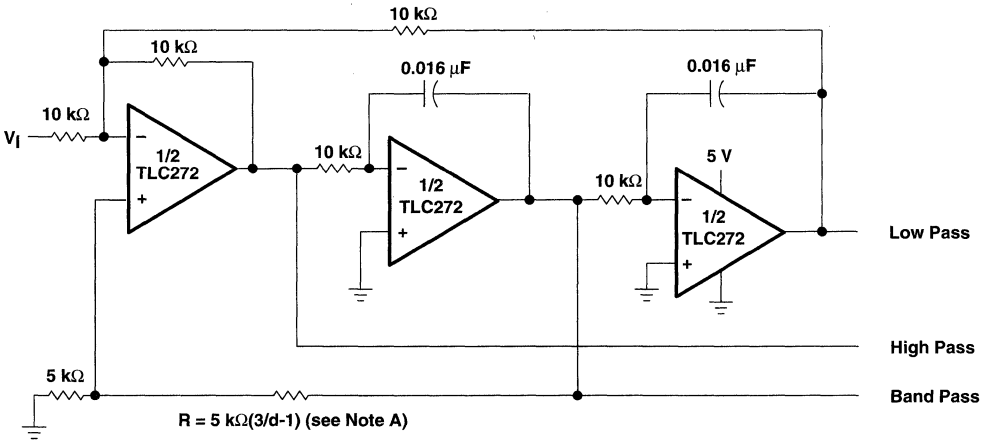
The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

APPLICATION INFORMATION



NOTE A: d = damping factor, 1/Q

Figure 44. State-Variable Filter

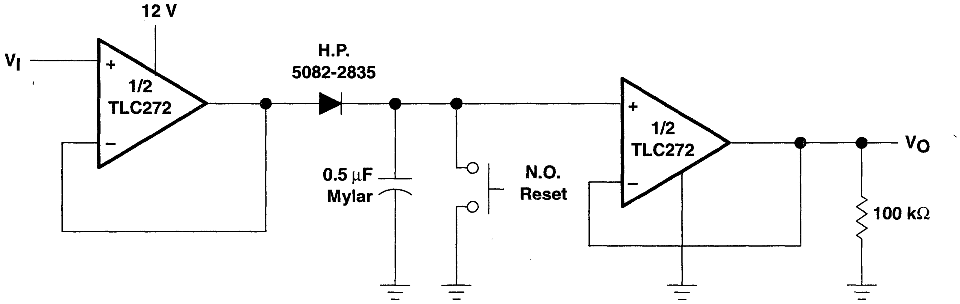
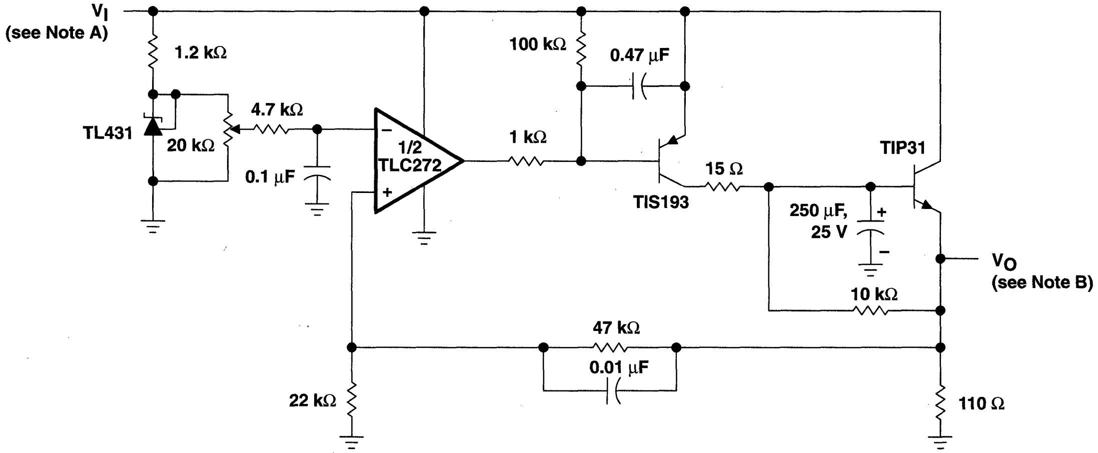


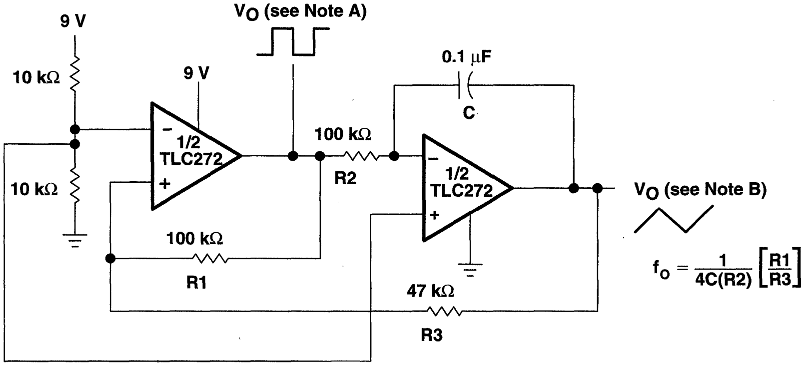
Figure 45. Positive-Peak Detector

APPLICATION INFORMATION



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2 V, 0 to 1 A

Figure 46. Logic-Array Power Supply

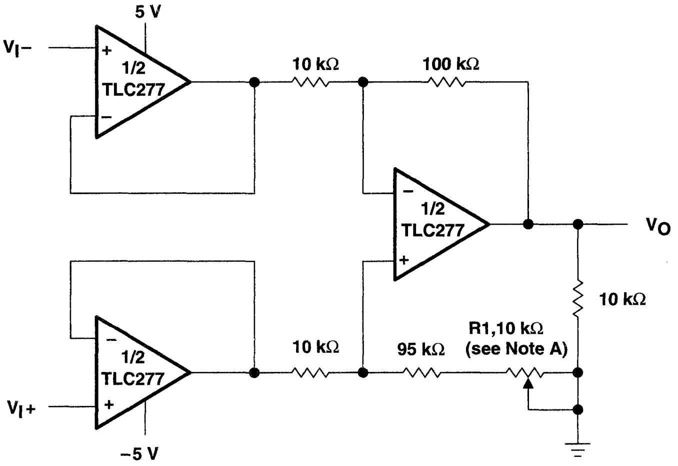


$$f_o = \frac{1}{4C(R2)}\left[\frac{R1}{R3}\right]$$

NOTES: A. $V_{O(PP)}$ = 8 V
B. $V_{O(PP)}$ = 4 V

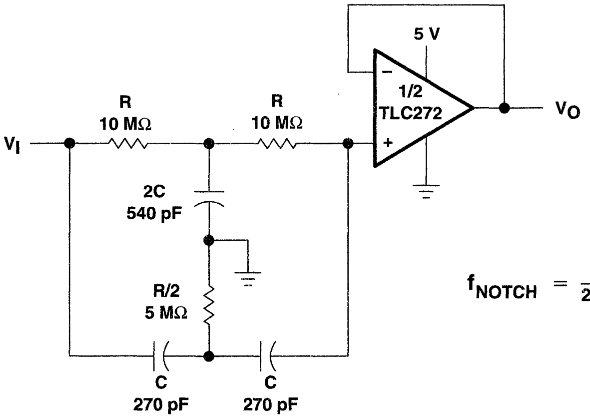
Figure 47. Single-Supply Function Generator

APPLICATION INFORMATION



NOTE B: CMRR adjustment must be noninductive.

Figure 48. Low-Power Instrumentation Amplifier



$$f_{NOTCH} = \frac{1}{2\pi RC}$$

Figure 49. Single-Supply Twin-T Notch Filter

TLC27L1, TLC27L1A, TLC27L1B
LinCMOS™ LOW-POWER
OPERATIONAL AMPLIFIERS

SLOS154 – DECEMBER 1995

- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  - **0°C to 70°C . . . 3 V to 16 V**
  - **–40°C to 85°C . . . 4 V to 16 V**
  - **–55°C to 125°C . . . 5 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix and I-Suffix Types)**
- **Low Noise . . . 68 nV/$\sqrt{\text{Hz}}$ Typically at f = 1 kHz**
- **Output Voltage Range includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

description

The TLC27L1 operational amplifier combines a wide range of input offset-voltage grades with low offset-voltage drift and high input impedance. In addition, the TLC27L1 is a low-bias version of the TLC271 programmable amplifier. These devices use the Texas Instruments silicon-gate LinCMOS™ technology, which provides offset-voltage stability far exceeding the stability available with conventional metal-gate processes.

Three offset-voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L1 (10 mV) to the TLC27L1B (2 mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27L1. The devices also exhibit low-voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input-voltage range includes the negative rail.

The device inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up.

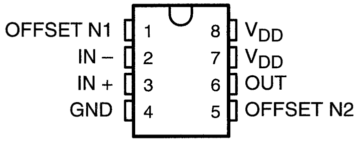
The TLC27L1 incorporates internal electrostatic-discharge (ESD) protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	2 mV 5 mV 10 mV	TLC27L1BCD TLC27L1ACD TLC27L1CD	TLC27L1BCP TLC27L1ACP TLC27L1CP
–40°C to 85°C	2 mV 5 mV 10 mV	TLC27L1BID TLC27L1AID TLC27L1ID	TLC27L1BIP TLC27L1AIP TLC27L1IP
–55°C to 125°C	10 mV	TLC27L1MD	TLC27L1MP

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L1BCDR).

D OR P PACKAGE
(TOP VIEW)

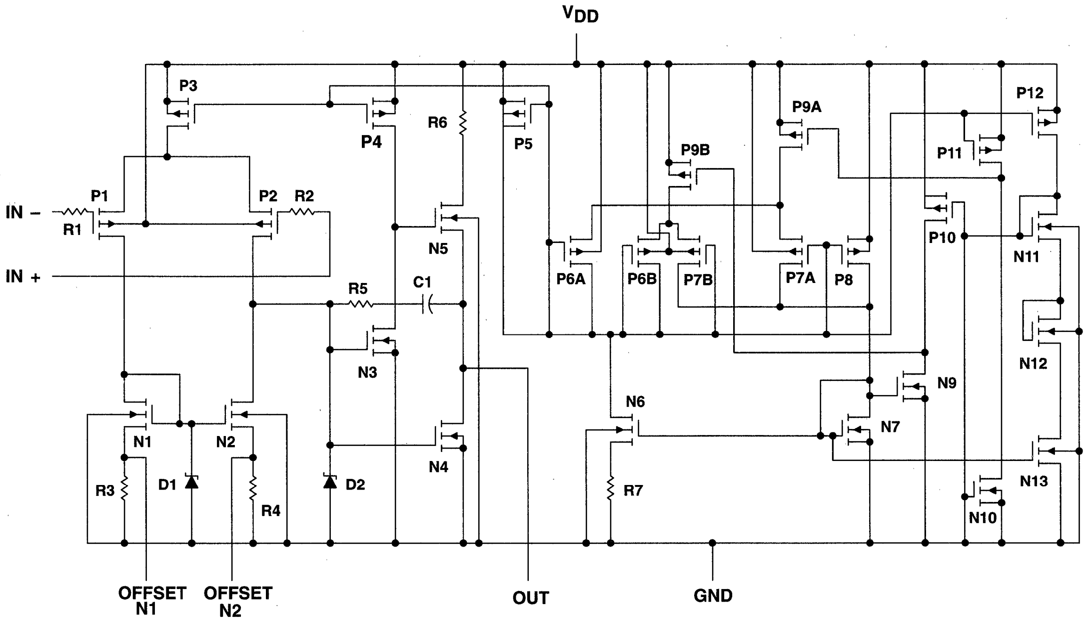


LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

equivalent schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	8 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O	±30 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 60 seconds, T_C: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	5	16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	−0.2	3.5	−0.2	3.5	0	3.5	V
	$V_{DD} = 10$ V	−0.2	8.5	−0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27L1C, TLC27L1AC, TLC27L1BC						UNIT
					$V_{DD} = 5$ V			$V_{DD} = 10$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L1C	$V_O = 1.4$ V, $V_{IC} = 0$ V, $R_S = 50\ \Omega$, $R_I = 1\ M\Omega$	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC27L1AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC27L1BC		25°C		0.24	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		$V_{ID} = 100$ mV, $R_L = 1\ M\Omega$	25°C	3.2	4.1		8	8.9		V
				0°C	3	4.1		7.8	8.9		
				70°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		$V_{ID} = -100$ mV, $I_{OL} = 0$	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		$R_L = 1\ M\Omega$, See Note 6	25°C	50	520		50	870		V/mV
				0°C	50	700		50	1030		
				70°C	50	380		50	660		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	94		65	97		dB
				0°C	60	95		60	97		
				70°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 5$ V to 10 V, $V_O = 1.4$ V	25°C	70	97		70	97		dB
				0°C	60	97		60	97		
				70°C	60	98		60	98		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		10	17		14	23	µA
				0°C		12	21		18	33	
				70°C		8	14		11	20	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At $V_{DD} = 5$ V, $V_O = 0.25$ V to 2 V; at $V_{DD} = 10$ V, $V_O = 1$ V to 6 V.

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27L1I, TLC27L1AI, TLC27L1BI						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L1I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC27L1AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC27L1BI		25°C		0.24	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3	4.1		8	8.9		V
				−40°C	3	4.1		7.8	8.9		
				85°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ See Note 6	25°C	50	520		50	870		V/mV
				−40°C	50	900		50	1550		
				85°C	50	330		50	585		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	94		65	97		dB
				−40°C	60	95		60	97		
				85°C	60	95		60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				−40°C	60	97		60	97		
				85°C	60	98		60	98		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		10	17		14	23	μA
				−40°C		16	27		25	43	
				85°C		17	13		10	18	

† Full range is −40 to 85°C.

NOTES:
4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC27L1M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		µV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
			−55°C	3	4.1		7.8	8.8		
			125°C	3	4.2		7.8	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
			−55°C	25	1000		25	1775		
			125°C	25	200		25	380		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	65	94		65	97		dB
			−55°C	60	95		60	97		
			125°C	60	85		60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
			−55°C	60	97		60	97		
			125°C	60	98		60	98		
$I_{I(SEL)}$	Input current (BIAS SELECT)	$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		10	17		14	23	µA
			−55°C		17	30		28	48	
			125°C		7	12		9	15	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1C, TLC27L1AC, TLC27L1BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1C, TLC27L1AC, TLC27L1BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		38°		
				0°C		40°		
				70°C		34°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1I, TLC27L1AI, TLC27L1BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		85		MHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		34°		
				−40°C		38°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1C, TLC27L1AC, TLC27L1BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		110		MHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		38°		
				−40°C		42°		
				85°C		32°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		34°		
				−55°C		39°		
				125°C		25°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		38°		
				−55°C		43°		
				125°C		29°		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	5, 6 7 8
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	9, 10 11 12 13, 14
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	15 16 27, 28
I_{IB}	Input bias current	vs Free-air temperature	17
I_{IO}	Input offset current	vs Free-air temperature	17
V_I	Maximum input voltage	vs Supply voltage	18
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	19 20
SR	Slew rate	vs Supply voltage vs Free-air temperature	21 22
	Bias-select current	vs Supply voltage	23
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	24
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	25 26
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitance load	29 30 31
V_n	Equivalent input noise voltage	vs Frequency	32
	Phase shift	vs Frequency	27, 28

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC27L1
INPUT OFFSET VOLTAGE

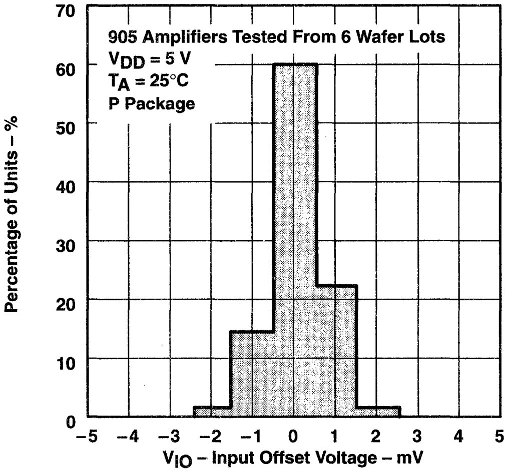


Figure 1

DISTRIBUTION OF TLC27L1
INPUT OFFSET VOLTAGE

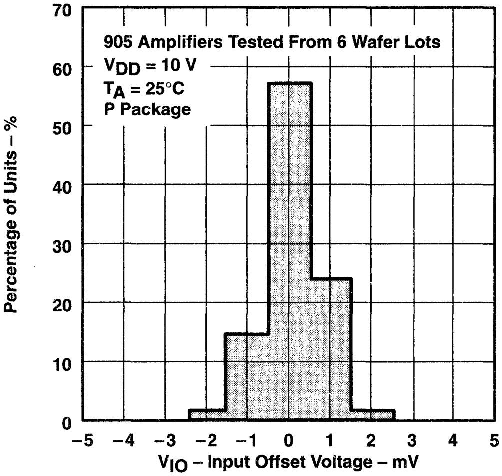


Figure 2

DISTRIBUTION OF TLC27L1
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

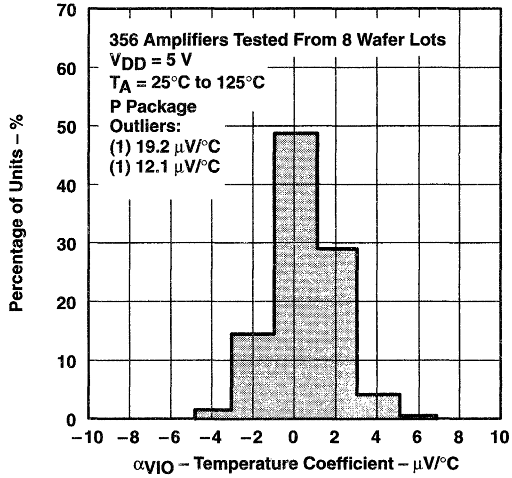


Figure 3

DISTRIBUTION OF TLC27L1
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

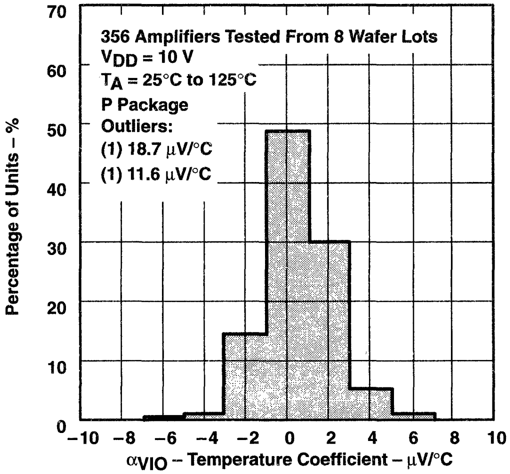


Figure 4

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

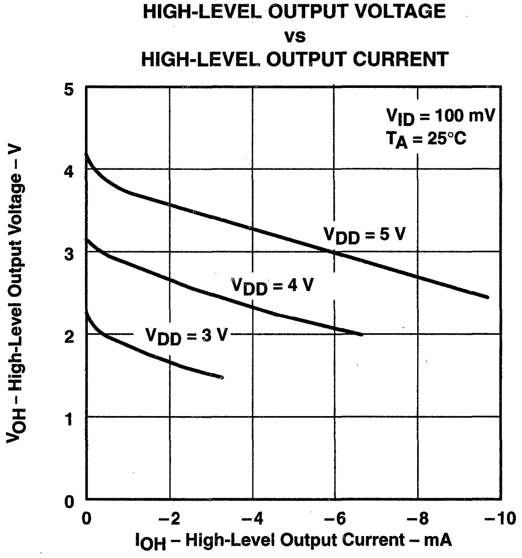

Figure 5

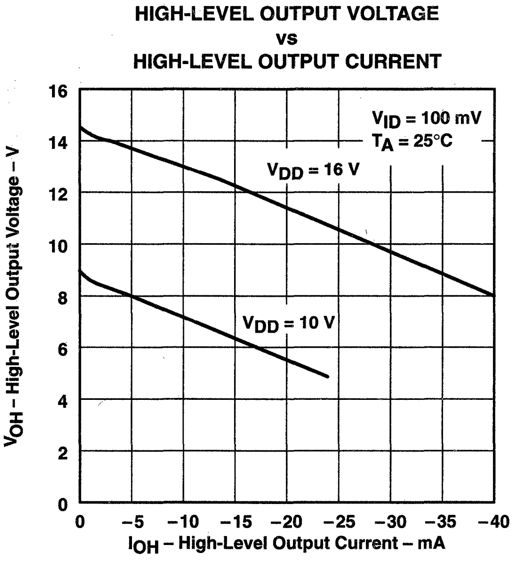

Figure 6

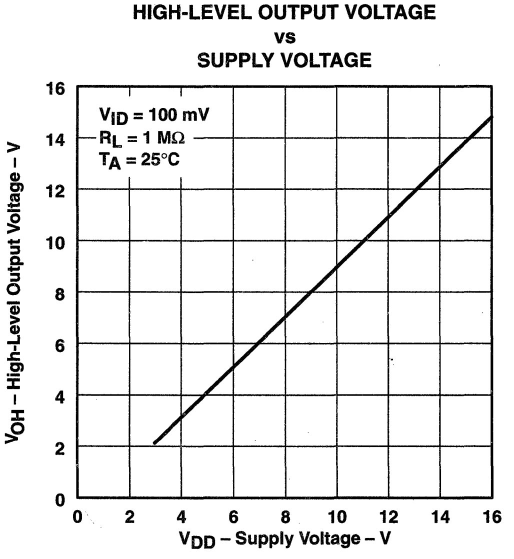

Figure 7

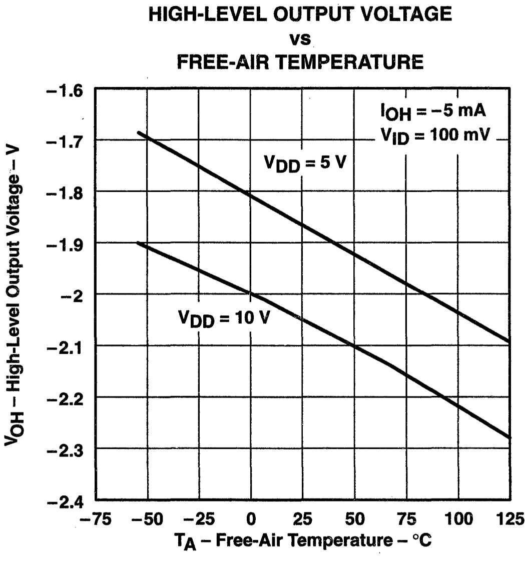

Figure 8

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

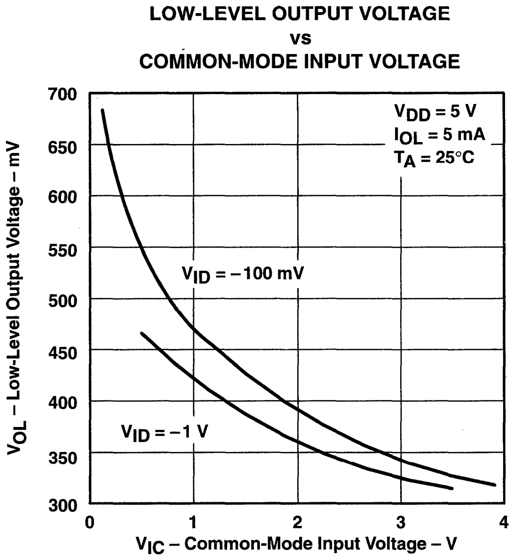

Figure 9

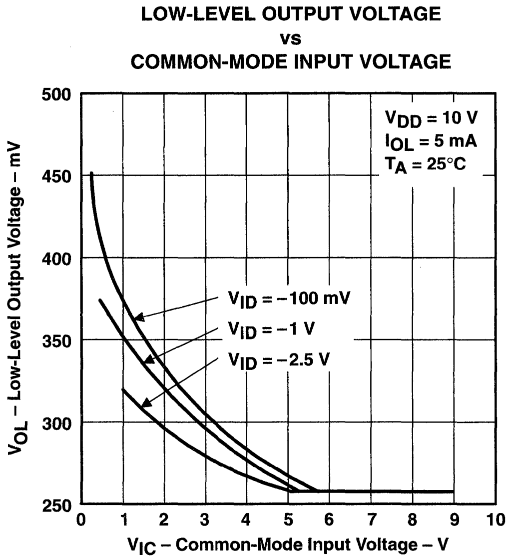

Figure 10

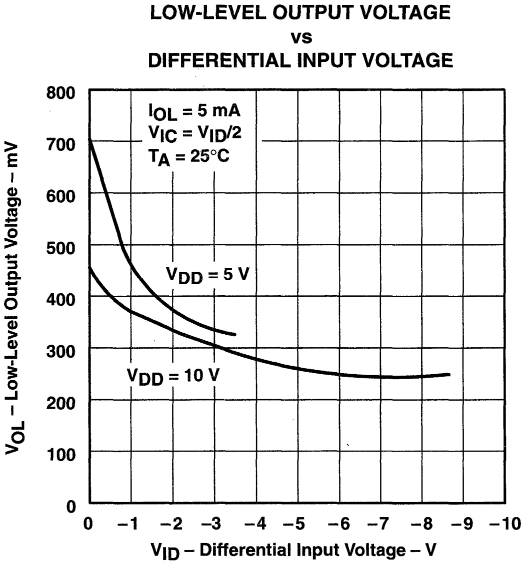

Figure 11

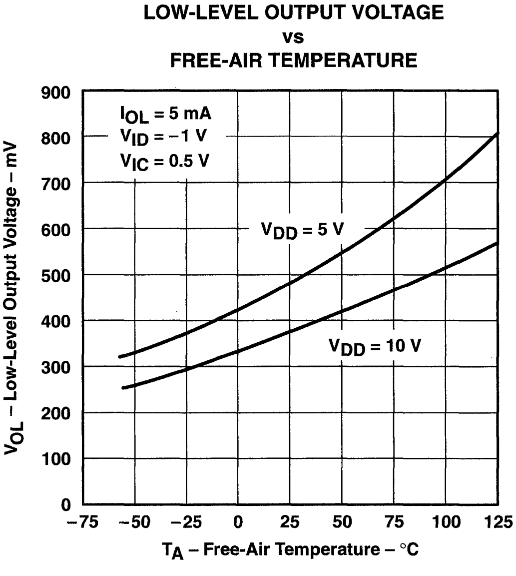

Figure 12

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

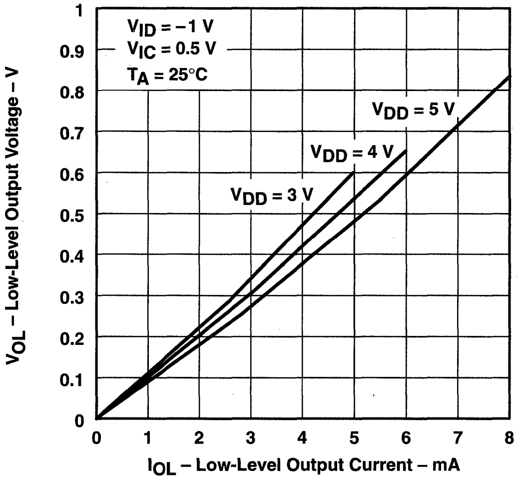

Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

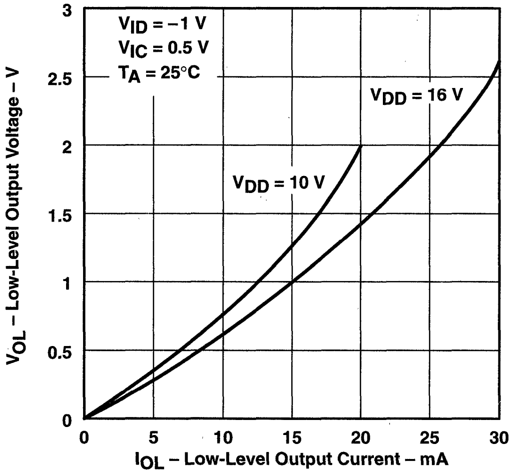

Figure 14

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

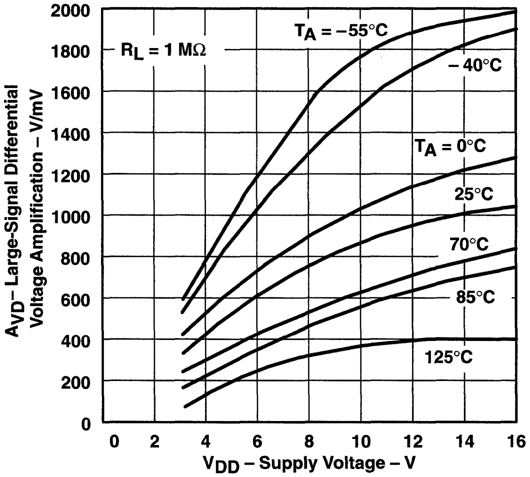

Figure 15

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

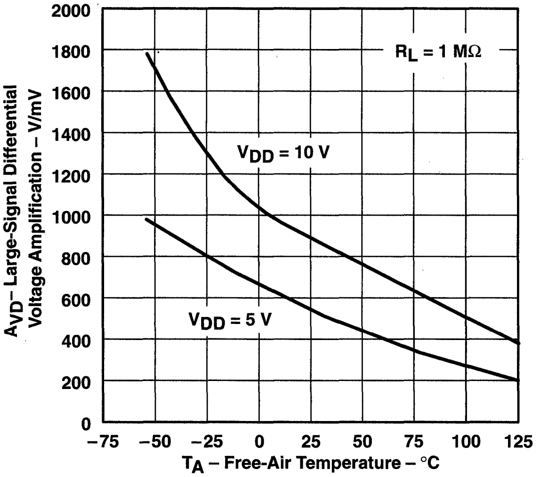

Figure 16

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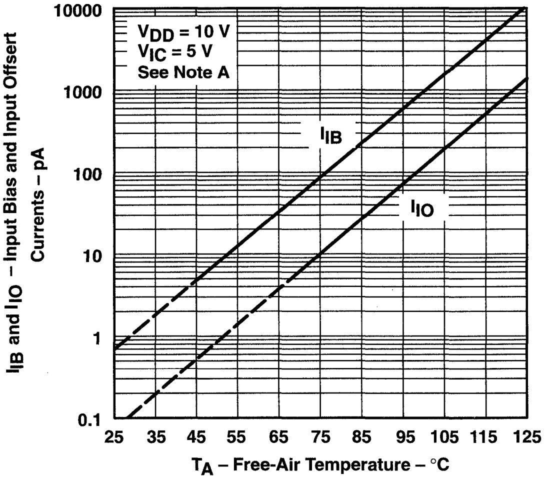
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 17

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

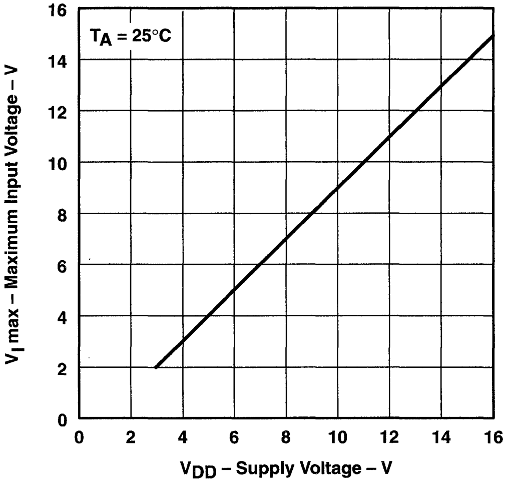


Figure 18

SUPPLY CURRENT vs SUPPLY VOLTAGE

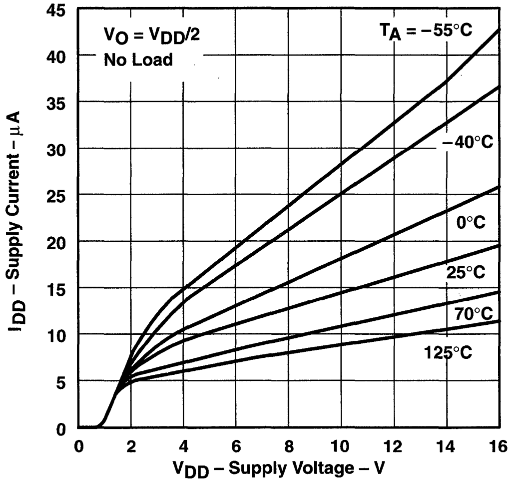


Figure 19

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

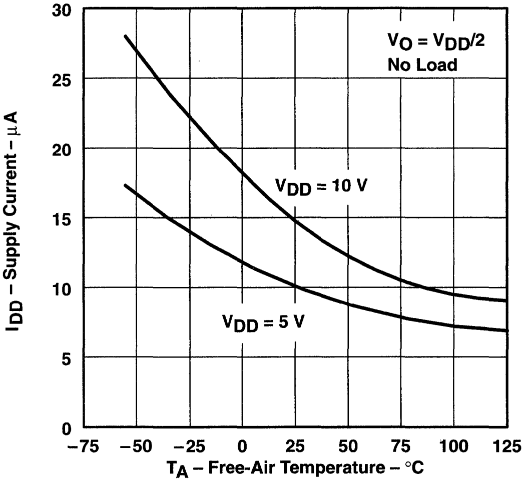


Figure 20

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs SUPPLY VOLTAGE

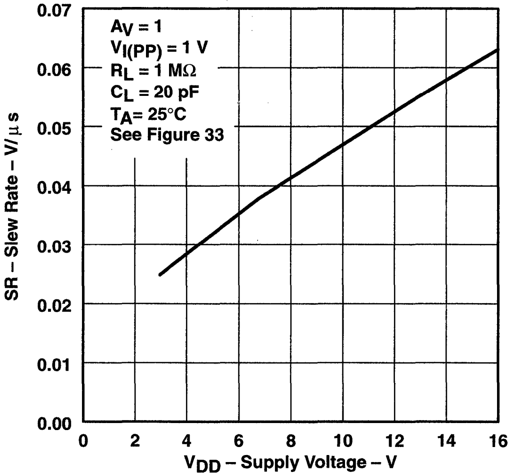

Figure 21

SLEW RATE vs FREE-AIR TEMPERATURE

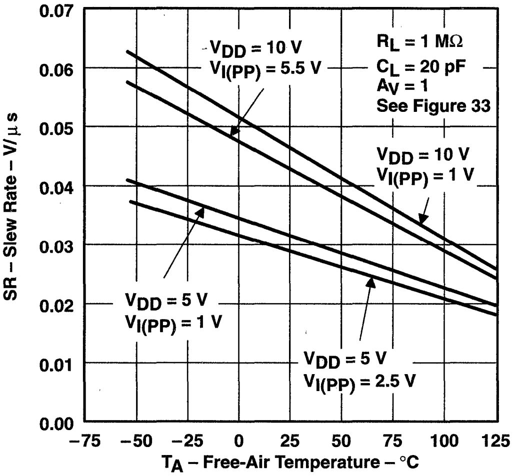

Figure 22

BIAS-SELECT CURRENT vs SUPPLY VOLTAGE

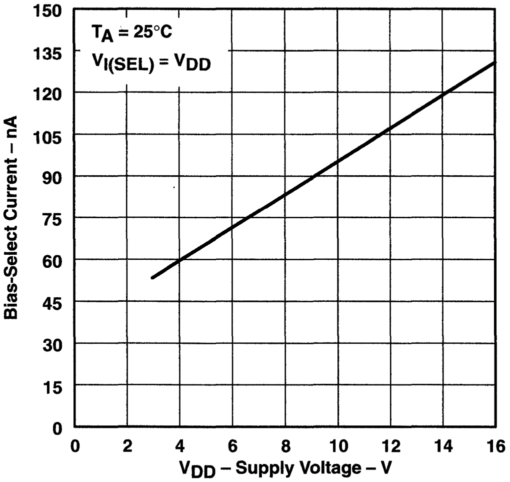

Figure 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

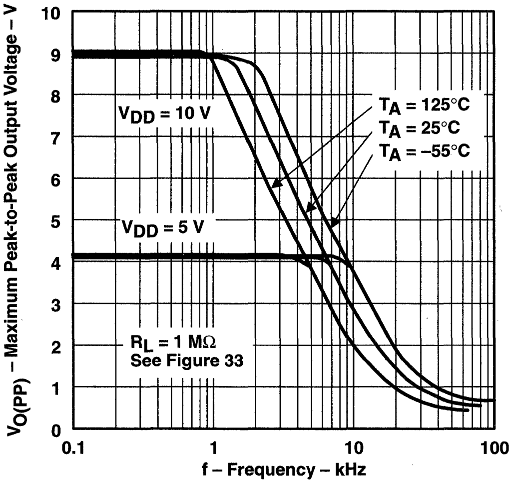

Figure 24

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

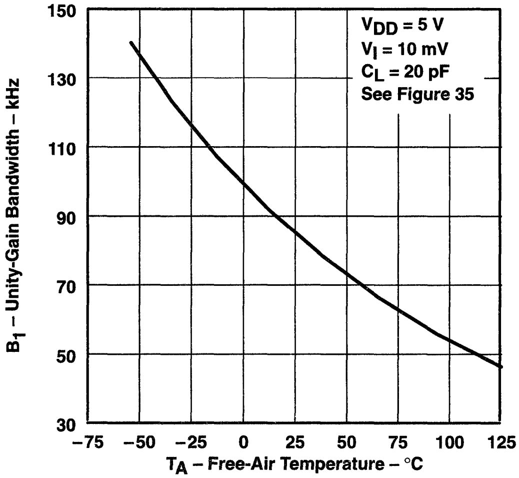

Figure 25

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

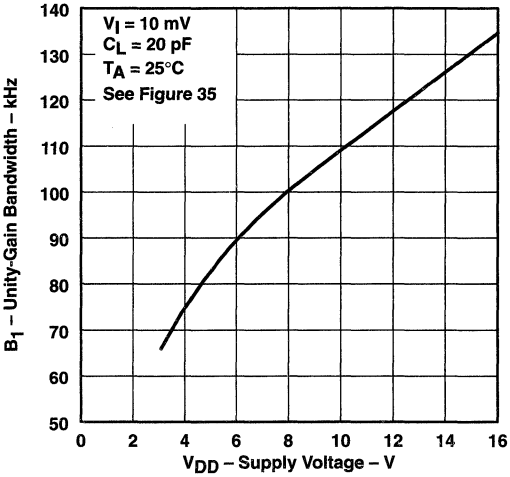

Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

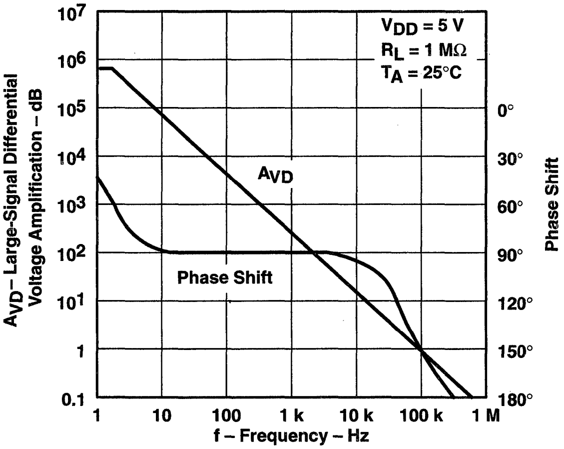

Figure 27

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

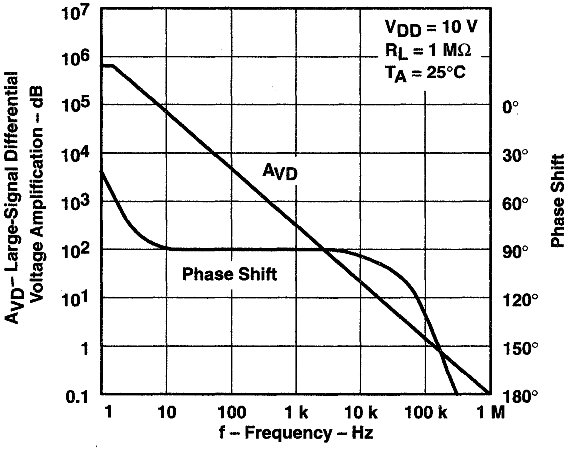

Figure 28

PHASE MARGIN vs SUPPLY VOLTAGE

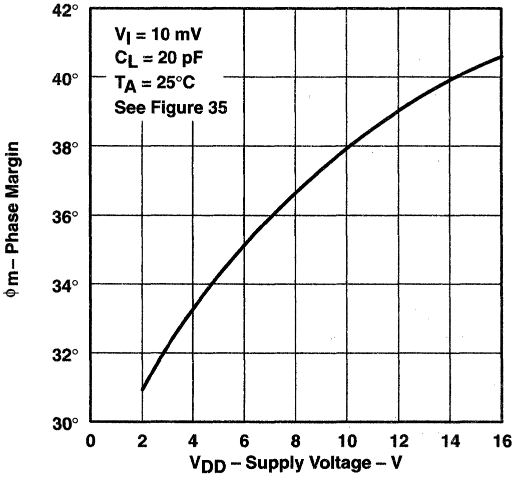

Figure 29

PHASE MARGIN vs FREE-AIR TEMPERATURE

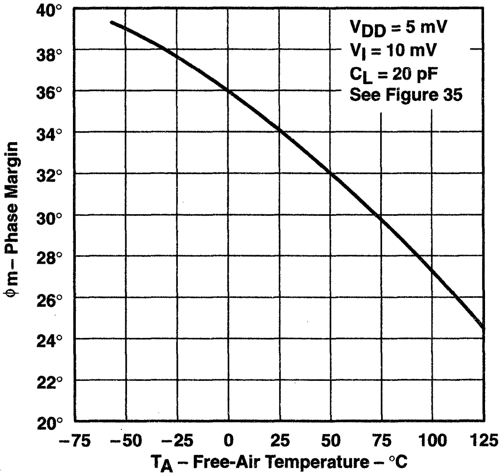

Figure 30

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

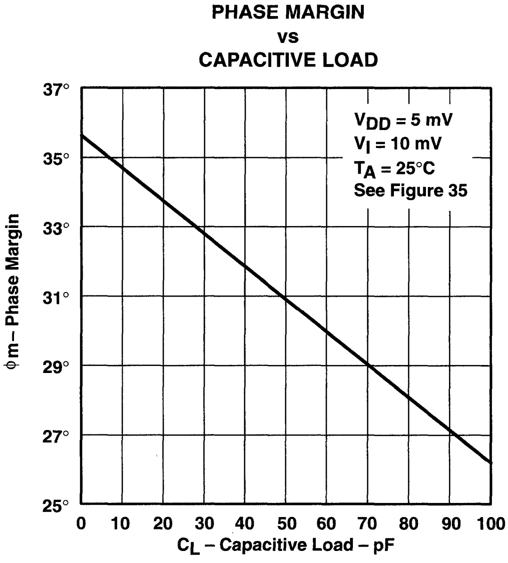

Figure 31

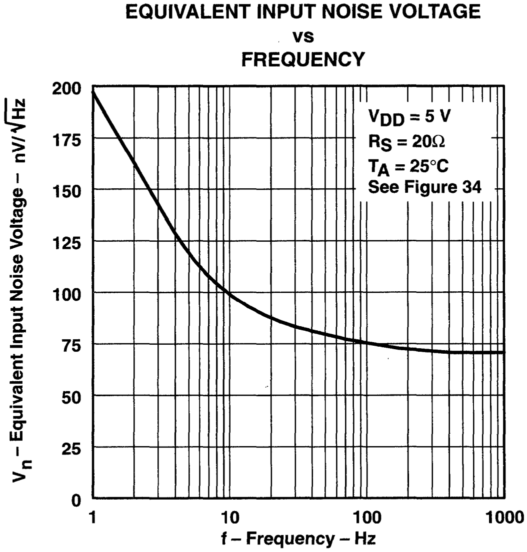

Figure 32

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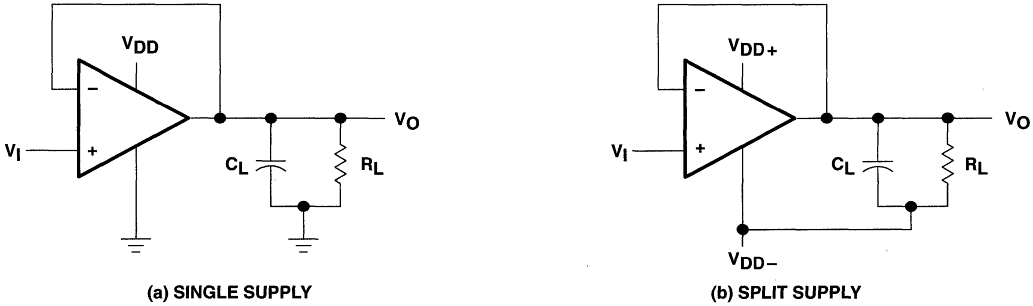
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27L1 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



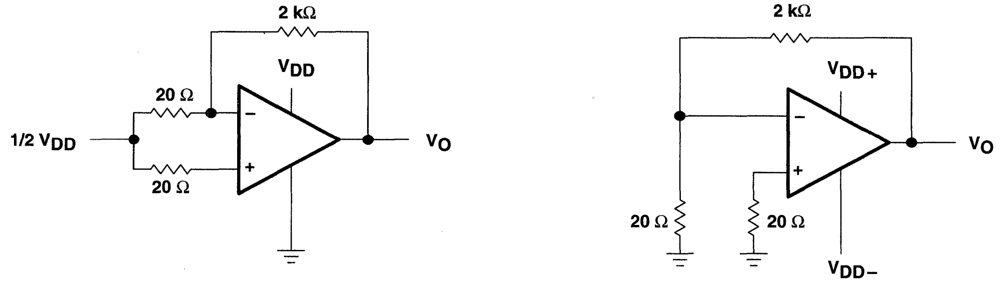
(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 33. Unity-Gain Amplifier

PARAMETER MEASUREMENT INFORMATION

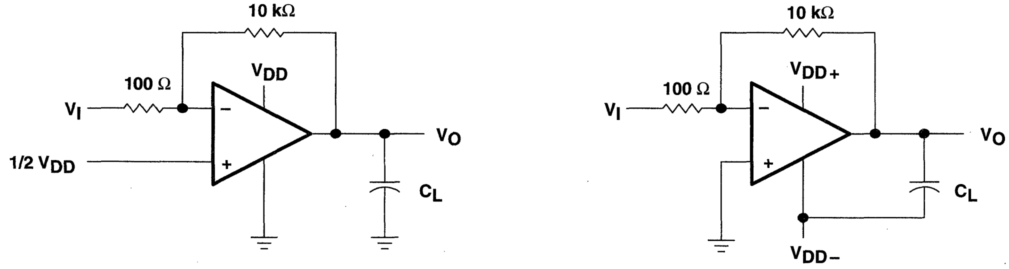
single-supply versus split-supply test circuits (continued)



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 34. Noise-Test Circuit



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 35. Gain-of-100 Inverting Amplifier

input bias current

Due to the high input impedance of the TLC27L1 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 36). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias-current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

PARAMETER MEASUREMENT INFORMATION

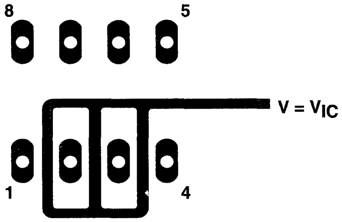


Figure 36. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. When conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset-voltage temperature coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset-voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset-voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

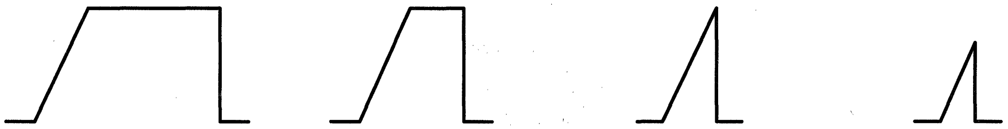
full-power response

Full-power response, the frequency above which the amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Since there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit in Figure 33. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 37). A square wave allows a more accurate determination of the point at which the maximum peak-to-peak output is reached.

PARAMETER MEASUREMENT INFORMATION

full-power response (continued)



(a) f = 100 Hz (b) B_{OM} > f > 100 Hz (c) f = B_{OM} (d) f > B_{OM}

Figure 37. Full-Power-Response Output Signal

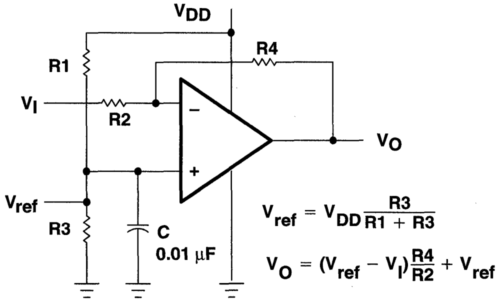
test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLC27L1 performs well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.



$$V_{ref} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = (V_{ref} - V_I)\frac{R4}{R2} + V_{ref}$$

Figure 38. Inverting Amplifier With Voltage Reference

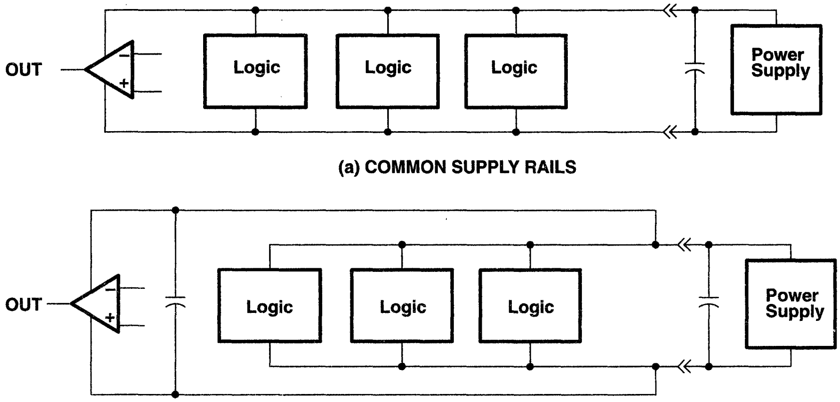
Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low-input bias-current consumption of the TLC27L1 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L1 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

APPLICATION INFORMATION

single-supply operation (continuted)

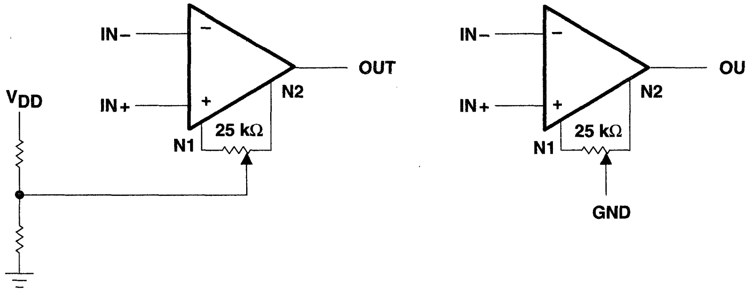


(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common Versus Separate Supply Rails

input offset voltage nulling

The TLC27L1 offers external input-offset null control. Nulling of the input-offset voltage may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 40. Total nulling may not be possible.



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 40. Input Offset-Voltage Null Circuit

input characteristics

The TLC27L1 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

APPLICATION INFORMATION

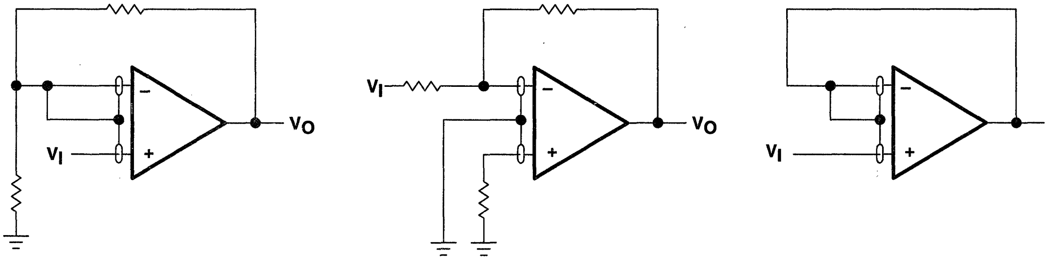
input characteristics (continued)

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L1 very good input offset-voltage drift characteristics relative to conventional metal-gate processes. Offset-voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset-voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLC27L1 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 36 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 41).

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low-input bias-current requirements of the TLC27L1 results in a very-low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 41. Guard-Ring Schemes

APPLICATION INFORMATION

feedback

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 42). The value of this capacitor is optimized empirically.

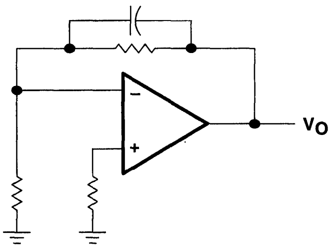


Figure 42. Compensation for Input Capacitance

electrostatic discharge protection

The TLC27L1 incorporates an internal ESD protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L1 inputs and output were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established when latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

APPLICATION INFORMATION

output characteristics

The output stage of the TLC27L1 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage (see Figure 43).

All operating characteristics of the TLC27L1 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 44). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

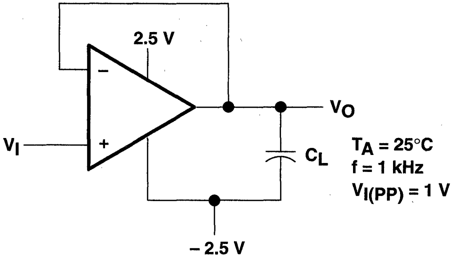
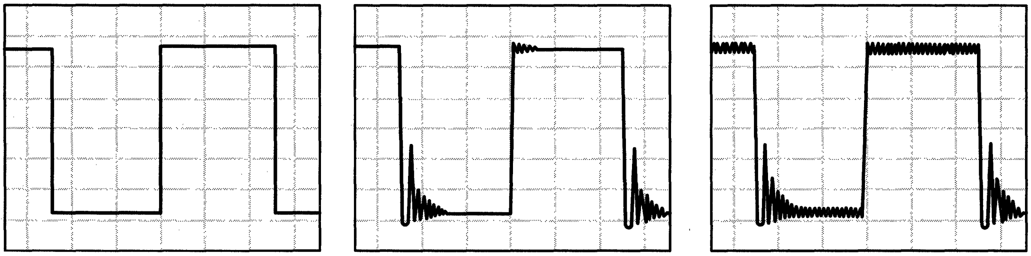


Figure 43. Test Circuit for Output Characteristics



(a) C_L = 20 pF, R_L = NO LOAD

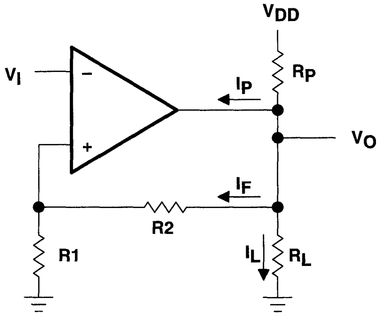
(b) C_L = 260 pF, R_L = NO LOAD

(c) C_L = 310 pF, R_L = NO LOAD

Figure 44. Effect of Capacitive Loads in Low-Bias Mode

Although the TLC27L1 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 45). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

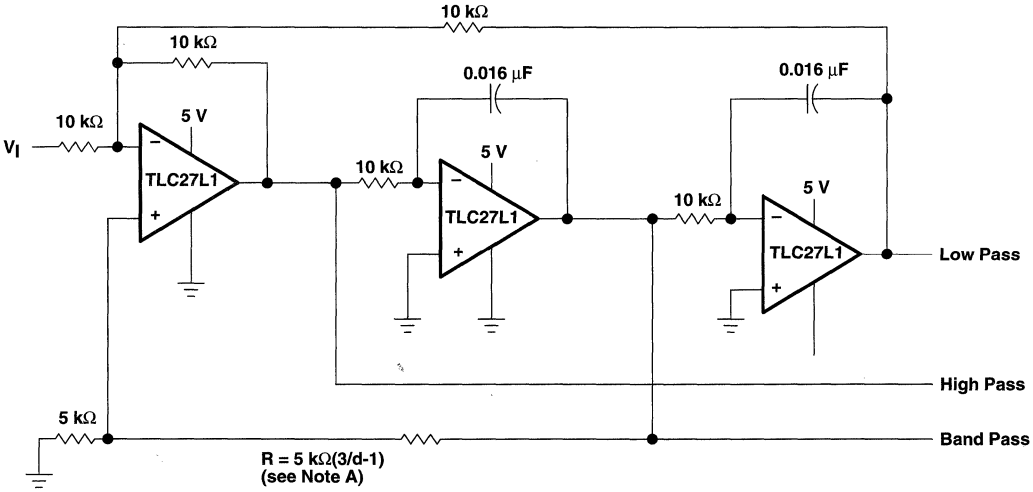
APPLICATION INFORMATION



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 mA)

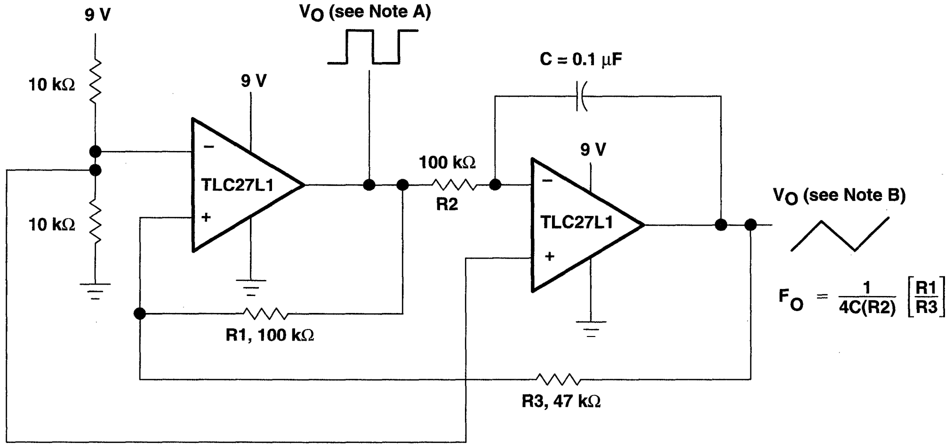
Figure 45. Resistive Pullup to Increase V_{OH}



NOTE A: d = damping factor, I/O

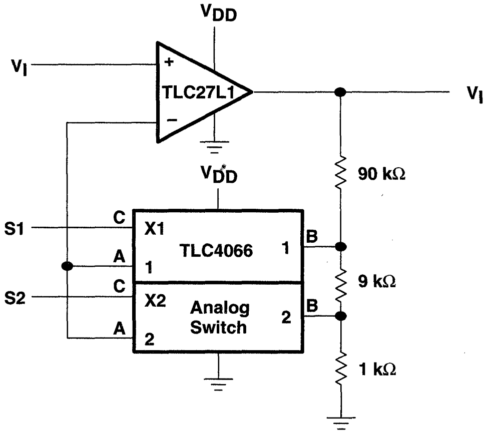
Figure 46. State-Variable Filter

APPLICATION INFORMATION



NOTES: A. $V_{O(PP)} = 8\ V$
B. $V_{O(PP)} = 4\ V$

Figure 47. Single-Supply Function Generator



Select	S_1	S_2
A_V	10	100

NOTE A: $V_{DD} = 5\ V$ to $12\ V$

Figure 48. Amplifier With Digital-Gain Selection

APPLICATION INFORMATION

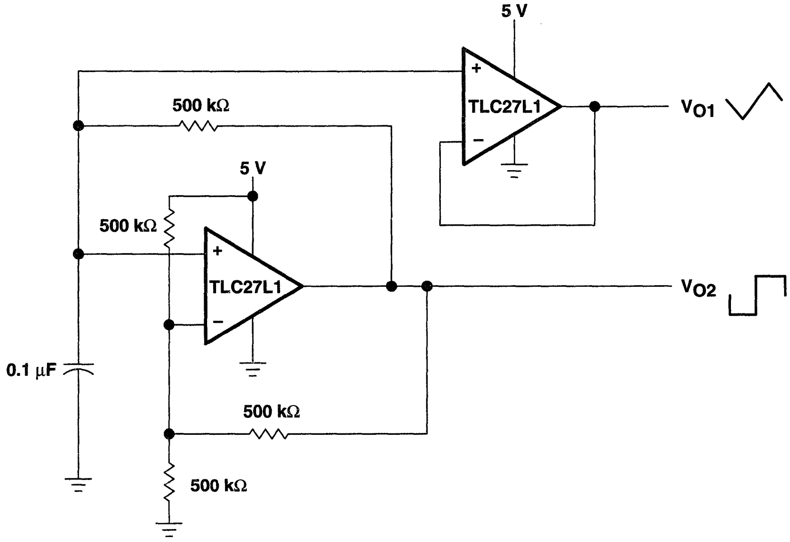
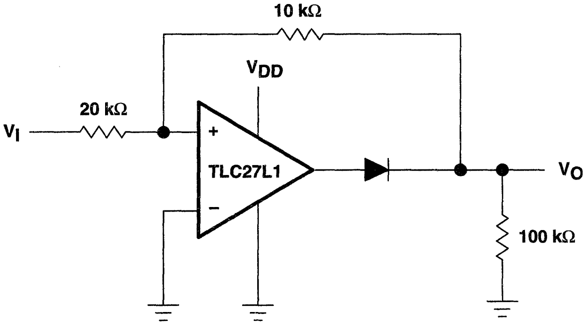


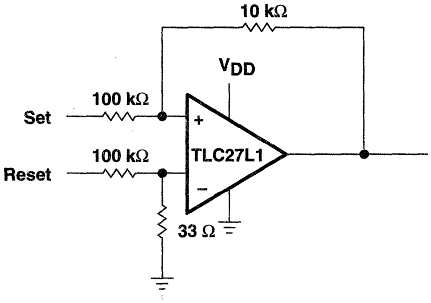
Figure 49. Multivibrator



NOTE A: V_{DD} = 5 V to 16 V

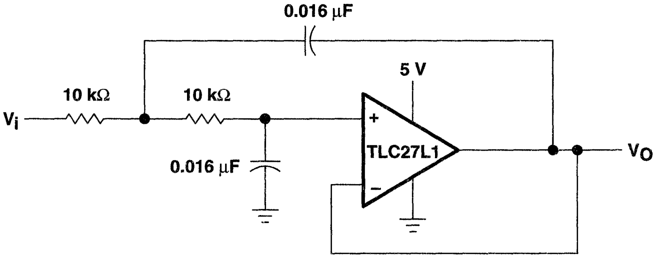
Figure 50. Full-Wave Rectifier

APPLICATION INFORMATION



NOTE A: V_{DD} = 5 V to 16 V

Figure 51. Set/Reset Flip-Flop



NOTE A: Normalized to F_C = 1 kHz and R_L = 10 kΩ

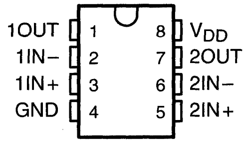
Figure 52. Two-Pole Low-Pass Butterworth Filter

TLC27L2, TLC27L2A, TLC27L2B, TLC27L7
LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

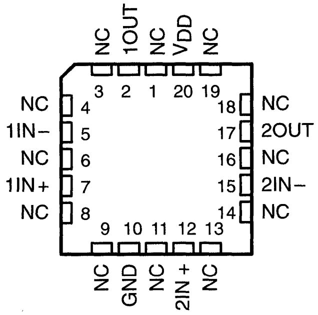
SLOS052B – OCTOBER 1987 – REVISED AUGUST 1994

- **Trimmed Offset Voltage: TLC27L7 . . . 500 μV Max at 25°C, V_{DD} = 5 V**
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  - **0°C to 70°C . . . 3 V to 16 V**
  - **−40°C to 85°C . . . 4 V to 16 V**
  - **−55°C to 125°C . . . 4 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Ultra-Low Power . . . Typically 95 μW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up immunity**

D, JG, OR P PACKAGE
(TOP VIEW)

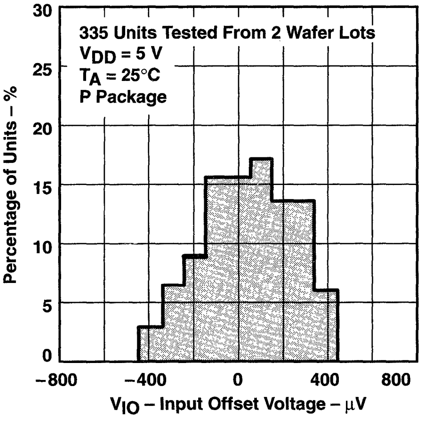


FK PACKAGE
(TOP VIEW)



NC – No internal connection

DISTRIBUTION OF TLC27L7
INPUT OFFSET VOLTAGE



description

The TLC27L2 and TLC27L7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV	TLC27L7CD	—	—	TLC27L7CP
	2 mV	TLC27L2BCD			TLC27L2BCP
	5 mV	TLC27L2ACD			TLC27L2ACP
	10 mV	TLC27L2CD			TLC27L2CP
−40°C to 85°C	500 μV	TLC27L7ID	—	—	TLC27L7IP
	2 mV	TLC27L2BID			TLC27L2BIP
	5 mV	TLC27L2AID			TLC27L2AIP
	10 mV	TLC27L2ID			TLC27L2IP
−55°C to 125°C	500 μV	TLC27L7MD	TLC27L7MFK	TLC27L7MJG	TLC27L7MP
	10 mV	TLC27L2MD	TLC27L2MFK	TLC27L2MJG	TLC27L2MP

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L7CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L2 (10 mV) to the high-precision TLC27L7 (500 µV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L2 and TLC27L7. The devices also exhibit low voltage single-supply operation and ultra-low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

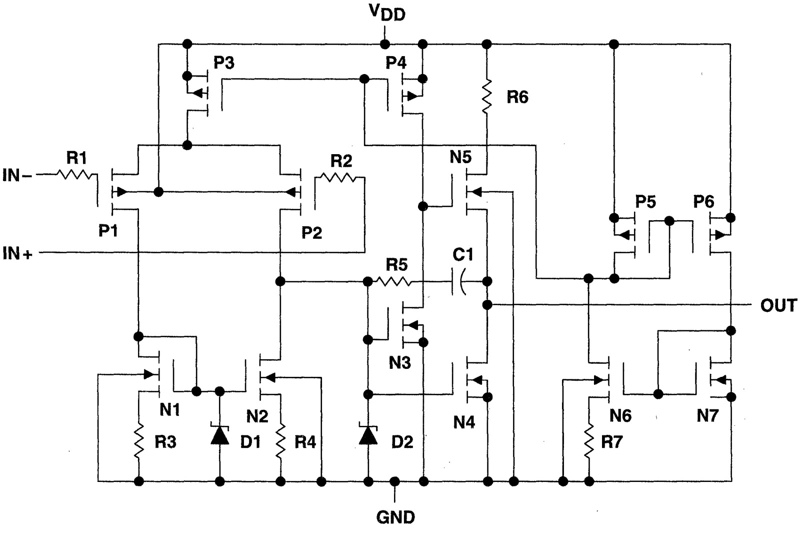
A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC27L2 and TLC27L7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-Suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD}	45 mA
Total current out of GND	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	−0.2	3.5	−0.2	3.5	0	3.5	V
	$V_{DD} = 10$ V	−0.2	8.5	−0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2C TLC27L2AC TLC27L2BC TLC27L7C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		204	2000	μV
					Full range			3000	
		TLC27L7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		170	500	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					0°C	3	4.1		
					70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	700		V/mV
					0°C	50	700		
					70°C	50	380		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min		25°C	65	94		dB
					0°C	60	95		
					70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		20	34	μA
					0°C		24	42	
					70°C		16	28	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2C TLC27L2AC TLC27L2BC TLC27L7C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		235	2000	μV
					Full range			3000	
		TLC27L7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		190	800	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		8	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					0°C	7.8	8.9		
					70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					0°C	50	1025		
					70°C	50	660		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$		25°C	65	97		dB
					0°C	60	97		
					70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	μA
					0°C		36	66	
					70°C		22	40	

† Full range is 0°C to 70°C.

NOTES: 4 The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5 This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L2AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L2BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		240	2000	µV
				Full range			3500	
		TLC27L7I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		170	500	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				−40°C	3	4.1		
				85°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				−40°C	50	900		
				85°C	50	330		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	94		dB
				−40°C	60	95		
				85°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		20	34	µA
				−40°C		31	54	
				85°C		15	26	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L2AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L2BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		235	2000	μV
				Full range			3500	
		TLC27L7I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	800	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				−40°C	7.8	8.9		
				85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	860		V/mV
				−40°C	50	1550		
				85°C	50	585		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	97		dB
				−40°C	60	97		
				85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		29	46	μA
				−40°C		49	86	
				85°C		20	36	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L2M TLC27L7M			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		170	500	µV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					−55°C	3	4.1		
					125°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	500		V/mV
					−55°C	25	1000		
					125°C	25	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	94		dB
					−55°C	60	95		
					125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		20	34	µA
					−55°C		35	60	
					125°C		14	24	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27L2M TLC27L7M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L7M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	800	µV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				−55°C	7.8	8.8		
				125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	860		V/mV
				−55°C	25	1750		
				125°C	25	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	97		dB
				−55°C	60	97		
				125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−55°C	60	97		
				125°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		29	46	µA
				−55°C		56	96	
				125°C		18	30	

† Full range is −55 °C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2C TLC27L2AC TLC27L2BC TLC27L7C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/µs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2C TLC27L2AC TLC27L2BC TLC27L7C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/µs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−40°C		38°		
				85°C		29°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2I TLC27L2AI TLC27L2BI TLC27L7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−40°C		42°		
				85°C		32°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2M TLC27L7M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 1\ M\Omega$, $C_L = 20\ pF$, See Figure 1	$V_{I(PP)} = 1\ V$	25°C		0.03		V/µs
				−55°C		0.04		
				125°C		0.02		
			$V_{I(PP)} = 2.5\ V$	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20\ \Omega$,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 1\ M\Omega$,	$C_L = 20\ pF$, See Figure 1	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	$V_I = 10\ mV$, See Figure 3	$C_L = 20\ pF$,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	$V_I = 10\ mV$, $C_L = 20\ pF$,	$f = B_1$, See Figure 3	25°C		34°		
				−55°C		39°		
				125°C		25°		

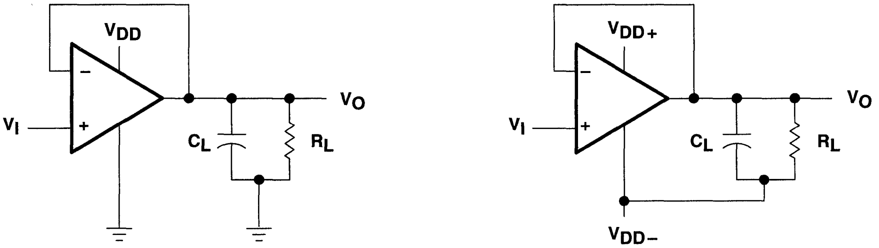
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L2M TLC27L7M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 1\ M\Omega$, $C_L = 20\ pF$, See Figure 1	$V_{I(PP)} = 1\ V$	25°C		0.05		V/µs
				−55°C		0.06		
				125°C		0.03		
			$V_{I(PP)} = 5.5\ V$	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20\ \Omega$,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 1\ M\Omega$,	$C_L = 20\ pF$, See Figure 1	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	$V_I = 10\ mV$, See Figure 3	$C_L = 20\ pF$,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	$V_I = 10\ mV$, $C_L = 20\ pF$,	$f = B_1$, See Figure 3	25°C		38°		
				−55°C		43°		
				125°C		29°		

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

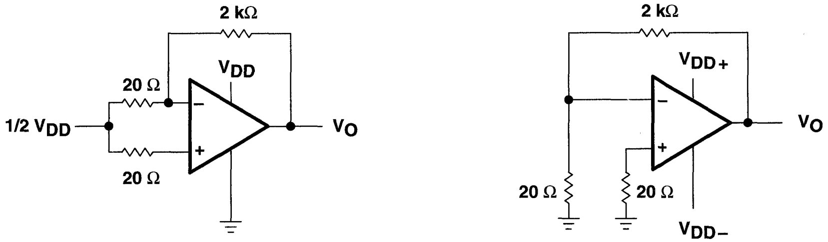
Because the TLC27L2 and TLC27L7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

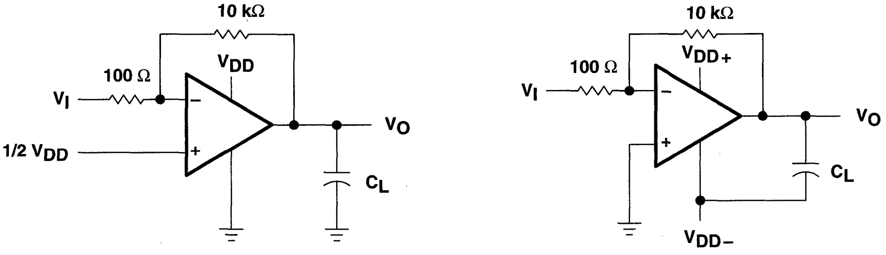
Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L2 and TLC27L7 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources.Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

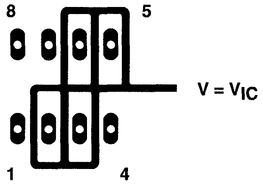


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

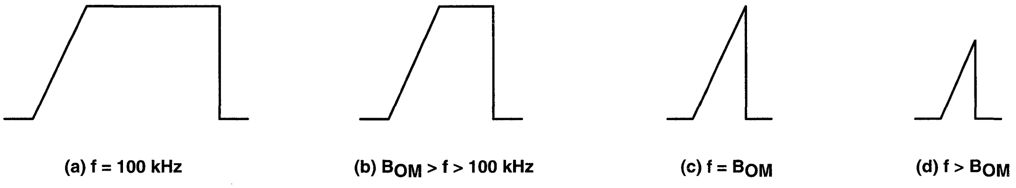

(a) f = 100 kHz (b) B_{OM} > f > 100 kHz (c) f = B_{OM} (d) f > B_{OM}

Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
V_{IO} Input offset voltage	Distribution	6, 7
αV_{IO} Temperature coefficient of input offset voltage	Distribution	8, 9
V_{OH} High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL} Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A_{VD} Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I_{IB} Input bias current	vs Free-air temperature	22
I_{IO} Input offset current	vs Free-air temperature	22
V_{IC} Common-mode input voltage	vs Supply voltage	23
I_{DD} Supply current	vs Supply voltage vs Free-air temperature	24 25
SR Slew rate	vs Supply voltage vs Free-air temperature	26 27
Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$ Maximum peak-to-peak output voltage	vs Frequency	29
B_1 Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
ϕ_m Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
V_n Equivalent input noise voltage	vs Frequency	37
Phase shift	vs Frequency	32, 33

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L2 INPUT OFFSET VOLTAGE

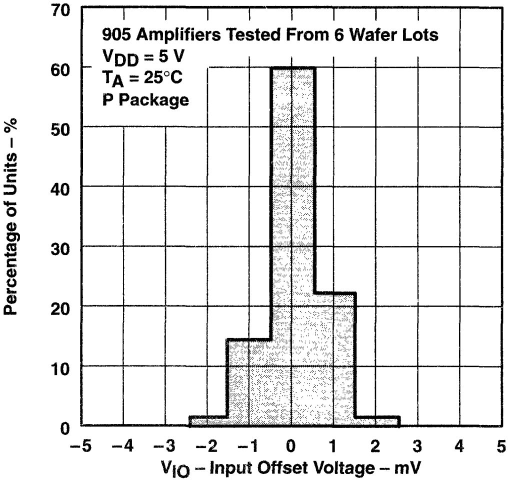


Figure 6

DISTRIBUTION OF TLC27L2 INPUT OFFSET VOLTAGE

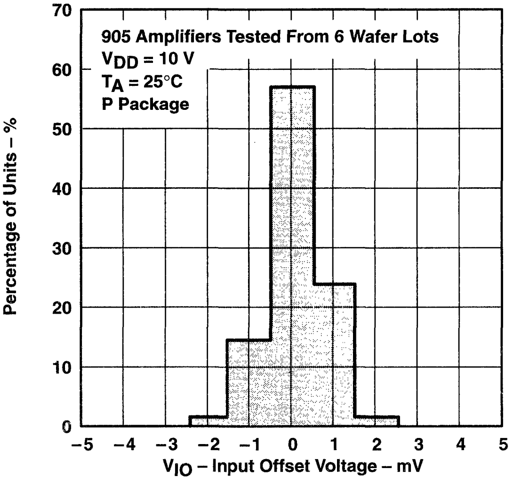


Figure 7

DISTRIBUTION OF TLC27LC AND TLC27L7 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

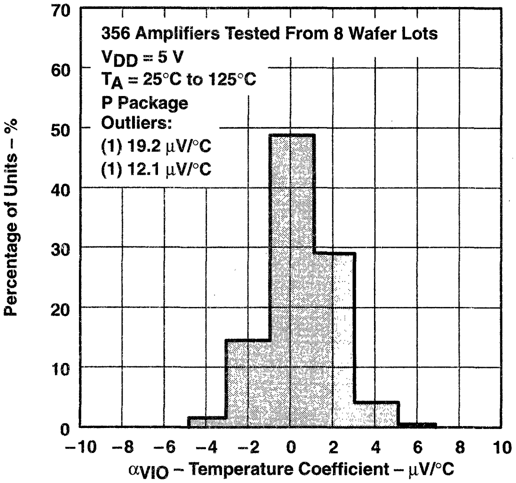


Figure 8

DISTRIBUTION OF TLC27LC AND TLC27L7 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

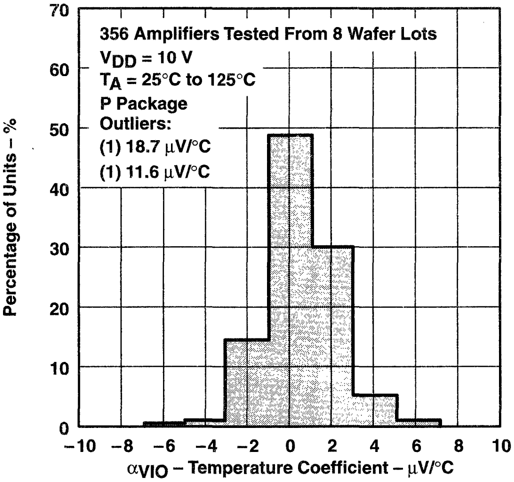


Figure 9

TYPICAL CHARACTERISTICS†

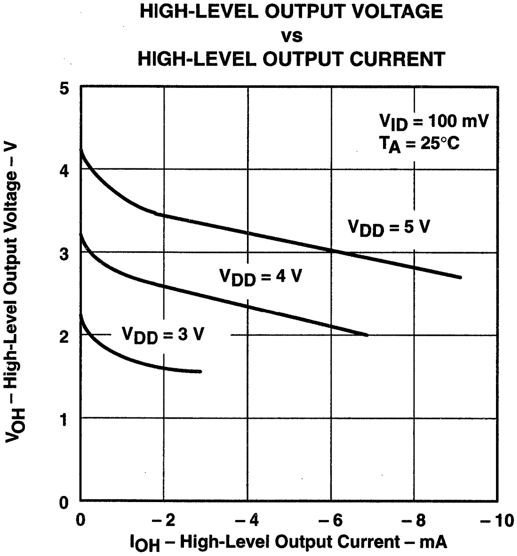


Figure 10

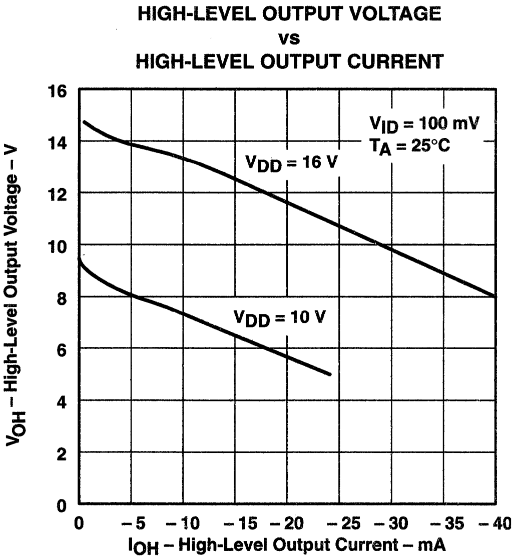


Figure 11

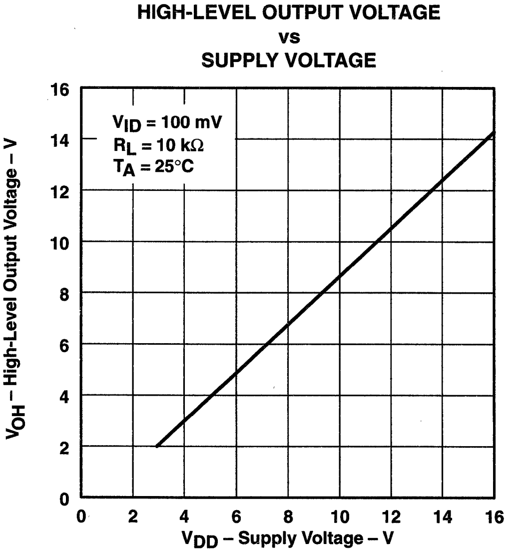


Figure 12

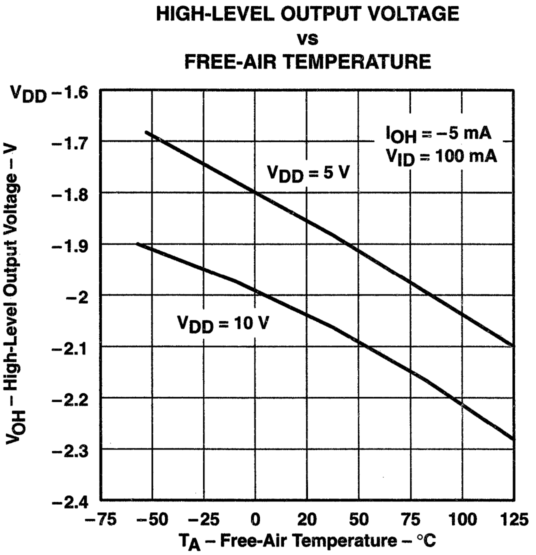


Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

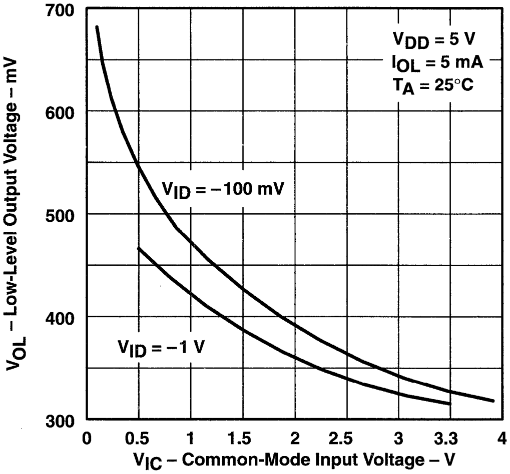

Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

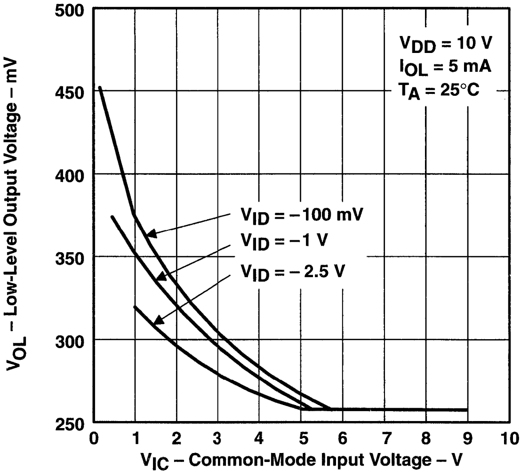

Figure 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

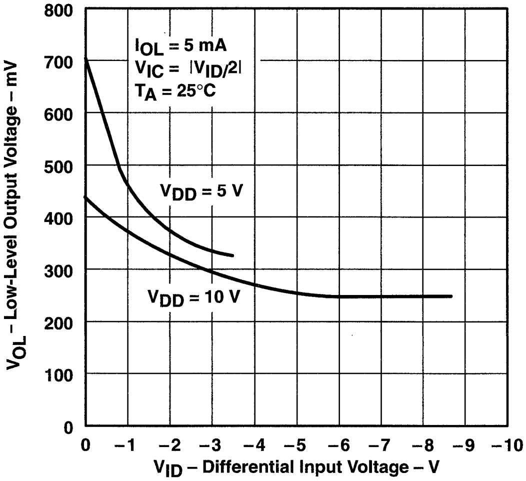

Figure 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

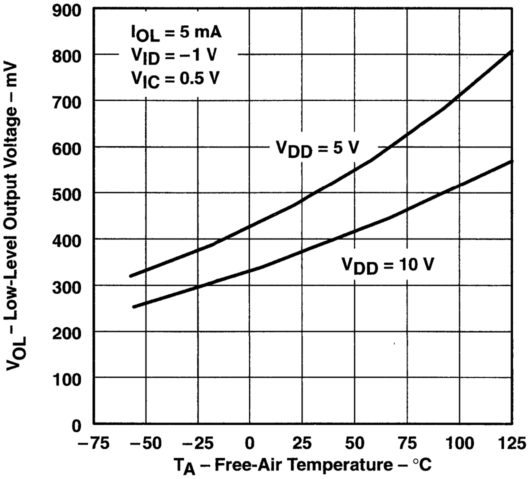

Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

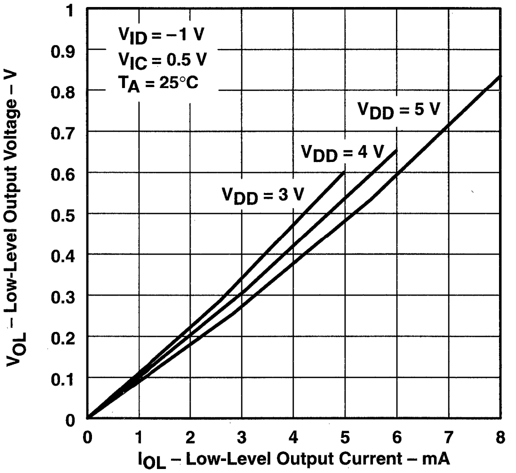


Figure 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

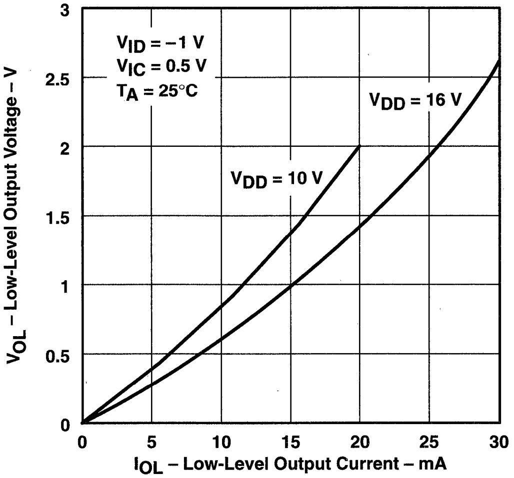


Figure 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

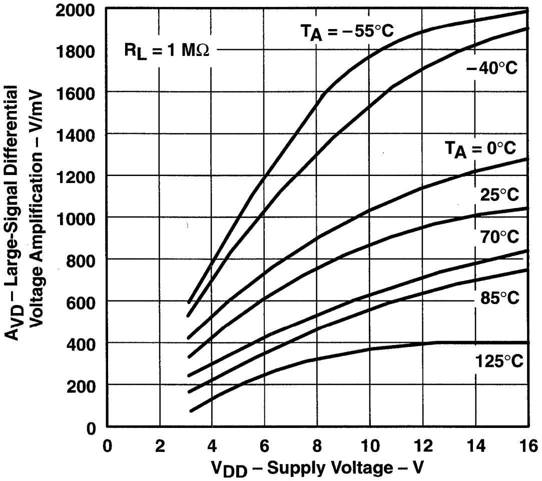


Figure 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

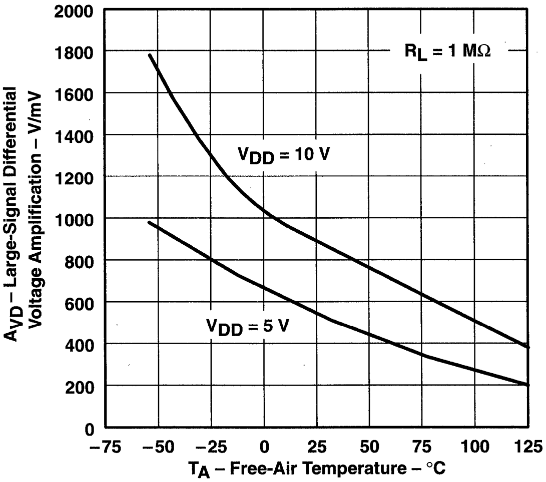


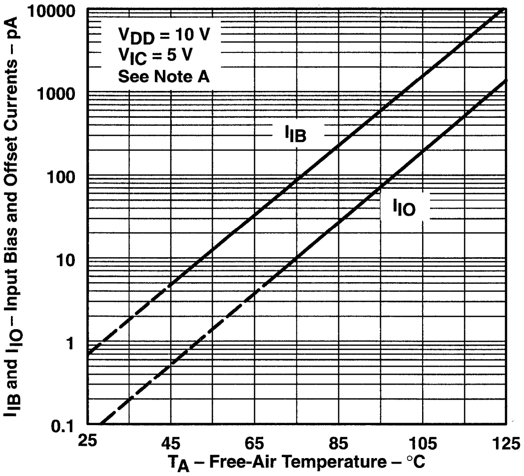
Figure 21

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

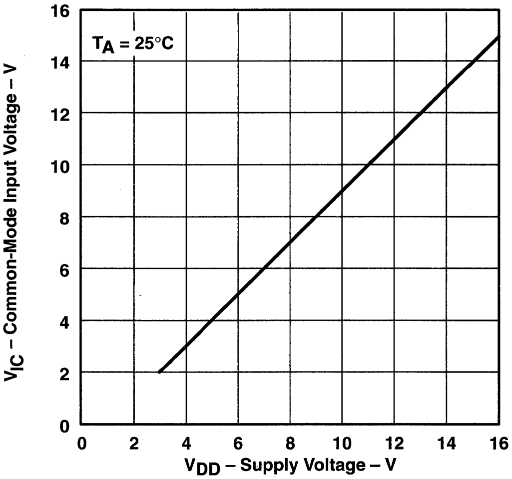


Figure 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

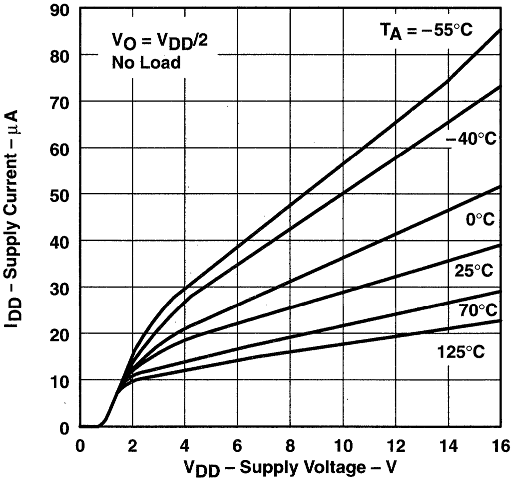


Figure 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

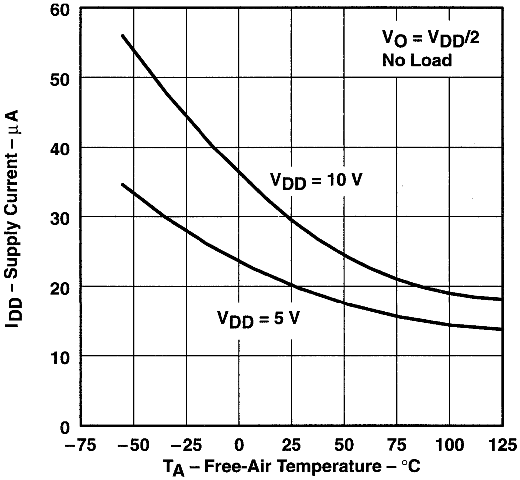


Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

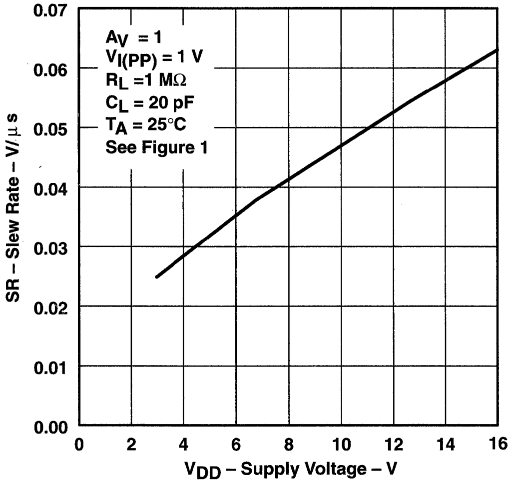

Figure 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

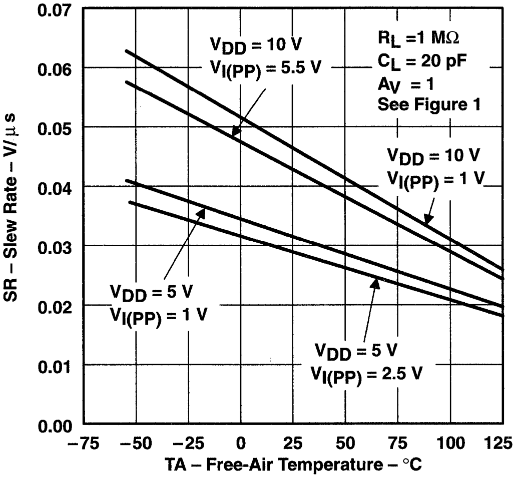

Figure 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

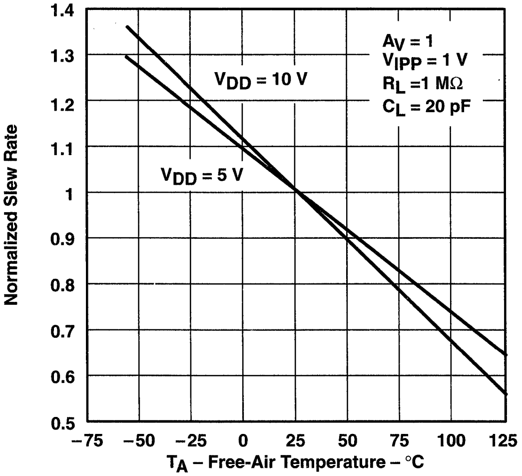

Figure 28

MAXIMUM-PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

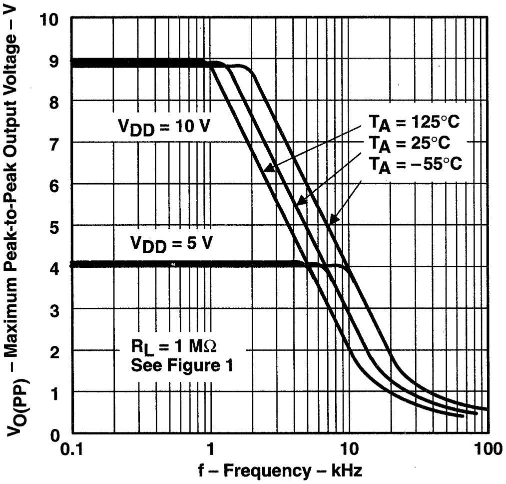

Figure 29

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

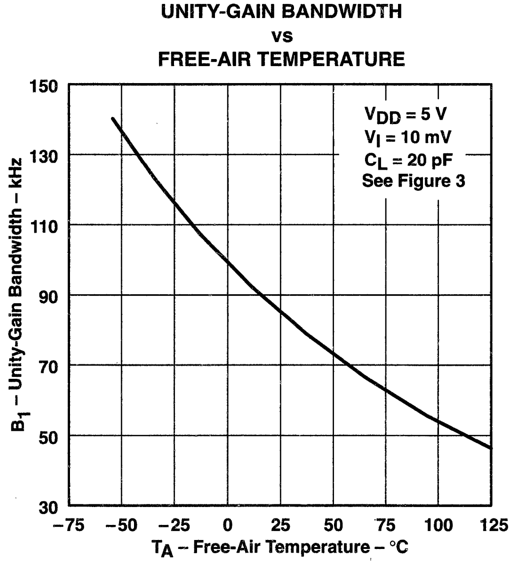

Figure 30

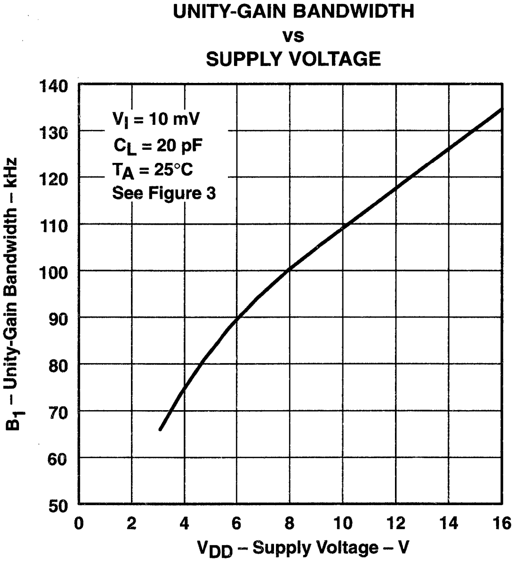

Figure 31

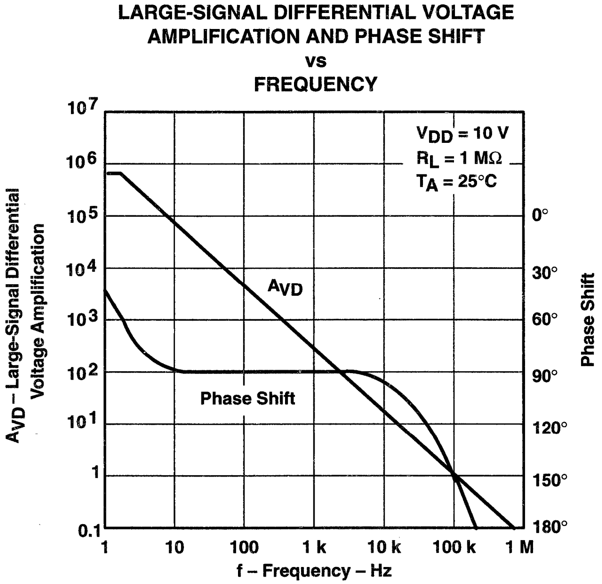

Figure 32

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

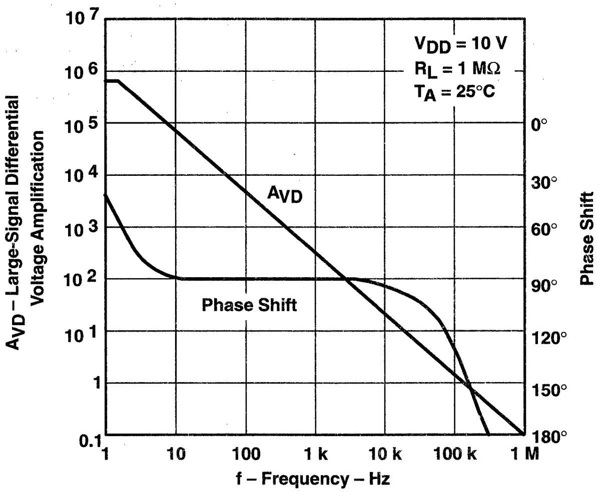

Figure 33

PHASE MARGIN vs SUPPLY VOLTAGE

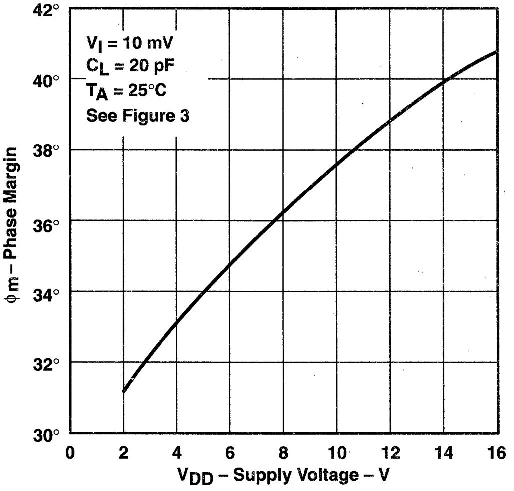

Figure 34

PHASE MARGIN vs FREE-AIR TEMPERATURE

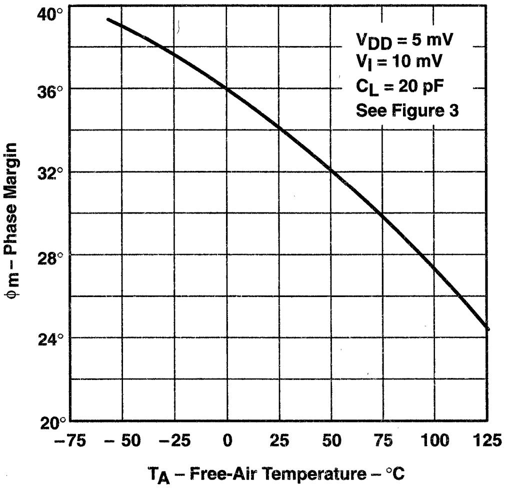

Figure 35

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN vs CAPACITIVE LOAD

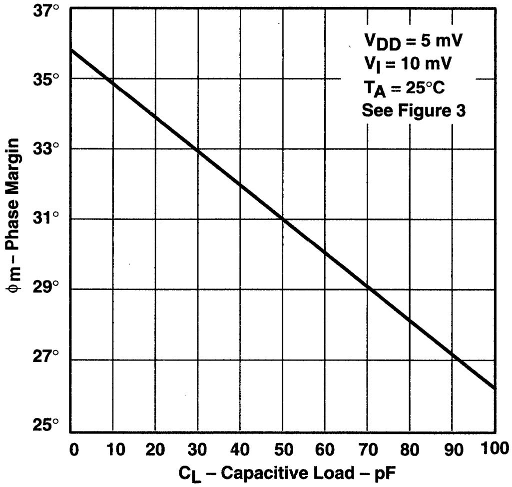


Figure 36

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

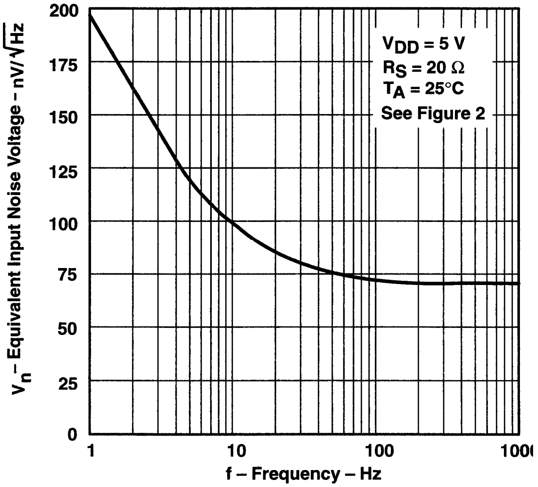


Figure 37

APPLICATION INFORMATION

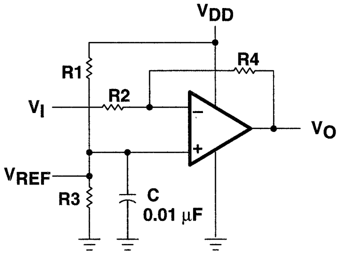
single-supply operation

While the TLC27L2 and TLC27L7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L2 and TLC27L7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L2 and TLC27L7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

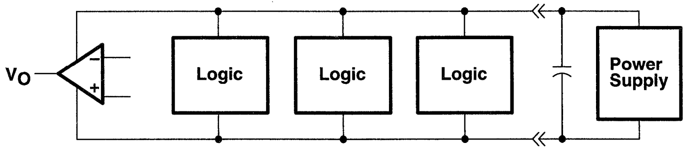
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



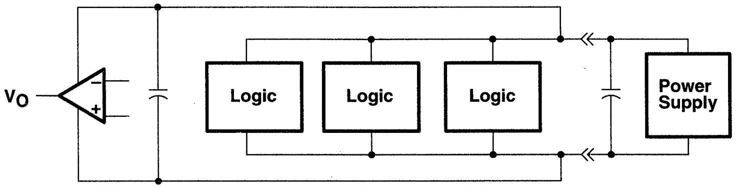
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

Figure 38. Inverting Amplifier With Voltage Reference



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common Versus Separate Supply Rails

APPLICATION INFORMATION

input characteristics

The TLC27L2 and TLC27L7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

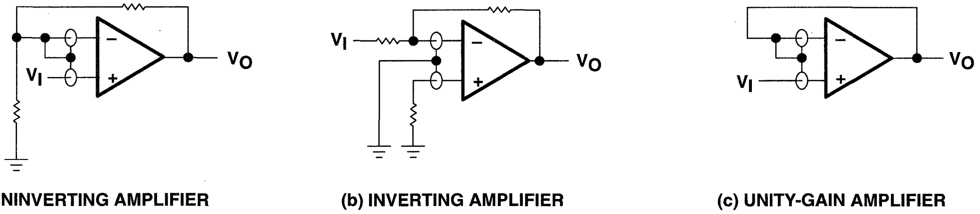
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L2 and TLC27L7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L2 and TLC27L7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L2 and TLC27L7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER **(b) INVERTING AMPLIFIER** **(c) UNITY-GAIN AMPLIFIER**

Figure 40. Guard-Ring Schemes

output characteristics

The output stage of the TLC27L2 and TLC27L7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27L2 and TLC27L7 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

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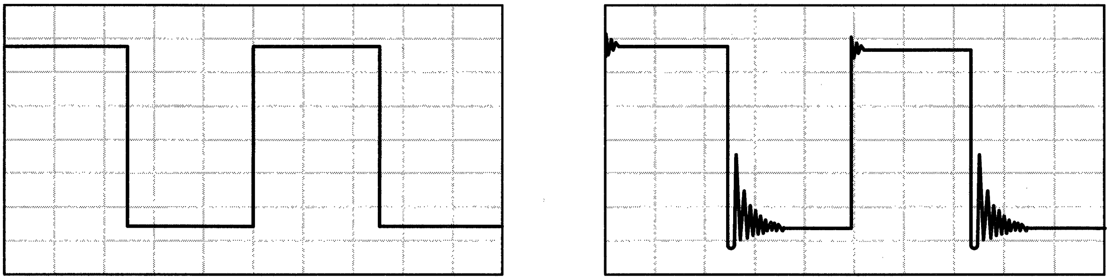
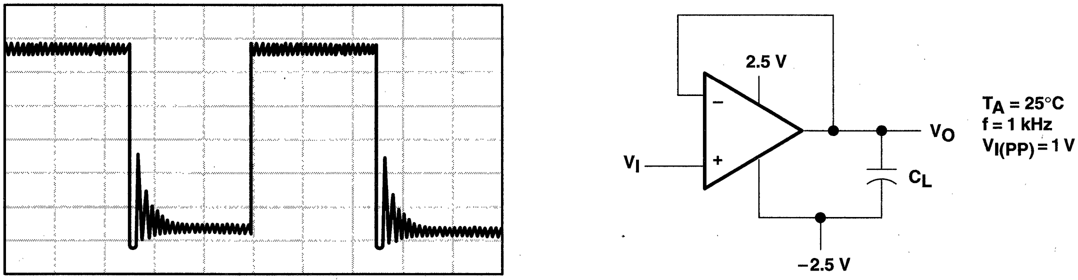
APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 260 pF, R_L = NO LOAD



(c) C_L = 310 pF, R_L = NO LOAD

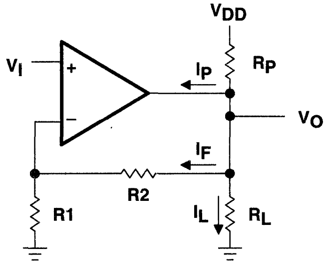
(d) TEST CIRCUIT

Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC27L2 and TLC27L7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

APPLICATION INFORMATION

output characteristics (continued)



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

Ip = Pullup current required by the operational amplifier (typically 500 μA)

Figure 42. Resistive Pullup to Increase V_{OH}

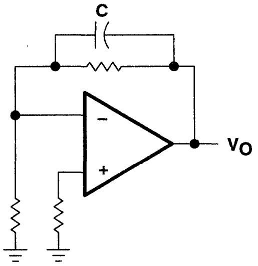


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27L2 and TLC27L7 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L2 and TLC27L7 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

APPLICATION INFORMATION

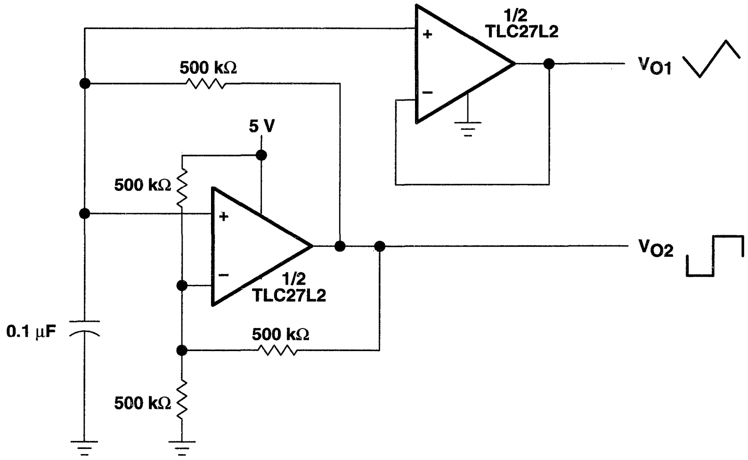
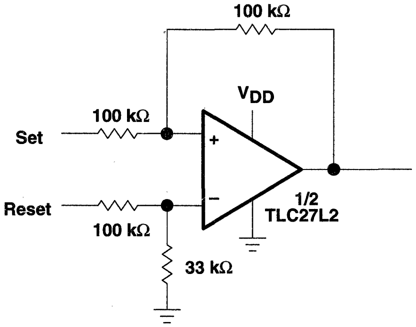


Figure 44. Multivibrator

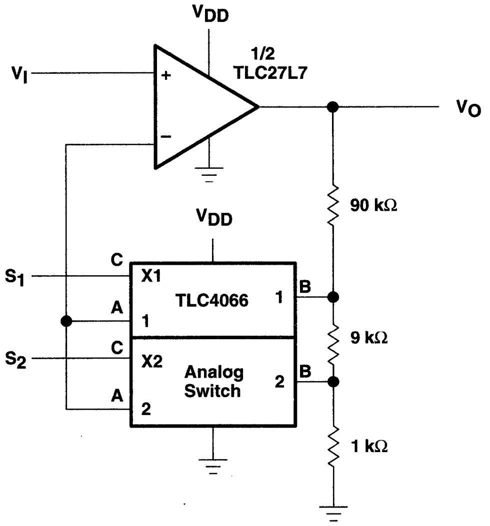


NOTE: V_{DD} = 5 V to 16 V

Figure 45. Set/Reset Flip-Flop

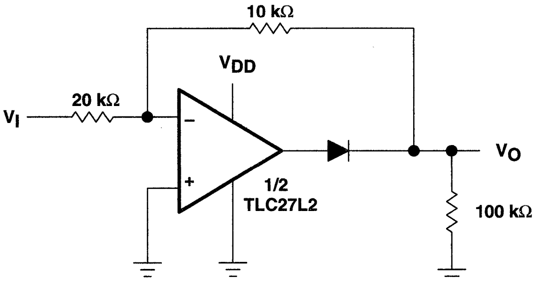
APPLICATION INFORMATION

SELECT:	S_1	S_2
A_V	10	100



NOTE: V_{DD} = 5 V to 12 V

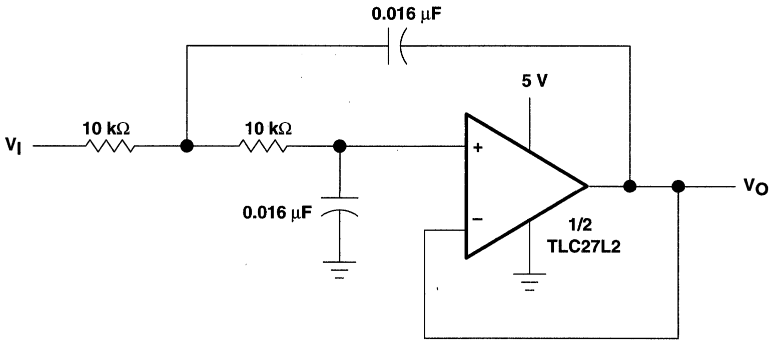
Figure 46. Amplifier With Digital Gain Selection



NOTE: V_{DD} = 5 V to 16 V

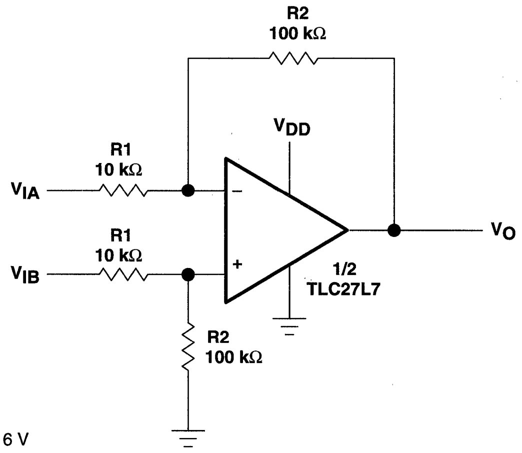
Figure 47. Full-Wave Rectifier

APPLICATION INFORMATION



NOTE: Normalized to f_C = 1 kHz and R_L = 10 kΩ

Figure 48. Two-Pole Low-Pass Butterworth Filter



NOTE: V_{DD} = 5 V to 16 V

$$V_O = \frac{R2}{R1}\left(V_{IB} - V_{IA}\right)$$

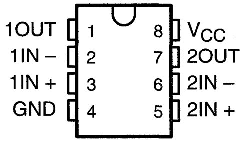
Figure 49. Difference Amplifier

TLC27M2, TLC27M2A, TLC27M2B, TLC27M7
LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

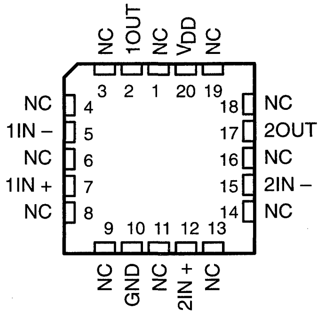
SLOS051B – OCTOBER 1987 – REVISED AUGUST 1994

- **Trimmed Offset Voltage:**
  TLC27M7 . . . 500 µV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 µV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Ranges:**
  - **0°C to 70°C . . . 3 V to 16 V**
  - **−40°C to 85°C . . . 4 V to 16 V**
  - **−55°C to 125°C . . . 4 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Low Noise . . . Typically 32 nV/$\sqrt{\text{Hz}}$ at f = 1 kHz**
- **Low Power . . . Typically 2.1 mW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, JG, OR P PACKAGE
(TOP VIEW)

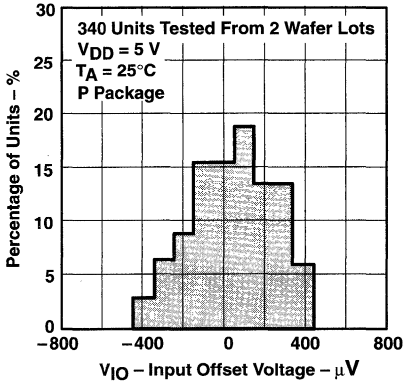


FK PACKAGE
(TOP VIEW)



NC – No internal connection

DISTRIBUTION OF TLC27M7
INPUT OFFSET VOLTAGE



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 µV	TLC27M7CD	—	—	TLC27M7CP
	2 mV	TLC27M2BCD	—	—	TLC27M2BCP
	5 mV	TLC27M2ACD	—	—	TLC27M2ACP
	10 mV	TLC27M2CD	—	—	TLC27M2CP
−40°C to 85°C	500 µV	TLC27M7ID	—	—	TLC27M7IP
	2 mV	TLC27M2BID	—	—	TLC27M2BIP
	5 mV	TLC27M2AID	—	—	TLC27M2AIP
	10 mV	TLC27M2ID	—	—	TLC27M2IP
−55°C to 125°C	500 µV	TLC27M7MD	TLC27M7MFK	TLC27M7MJG	TLC27M7MP
	10 mV	TLC27M2MD	TLC27M2MFK	TLC27M2MJG	TLC27M2MP

The D package is available taped and reeled. Add R suffix to the device type (e.g.,TLC27M7CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

description

The TLC27M2 and TLC27M7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose bipolar devices.These devices use Texas instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for general-purpose bipolar products,but with only a fraction of the power consumption. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M2 (10 mV) to the high-precision TLC27M7 (500 µV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M2 and TLC27M7. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

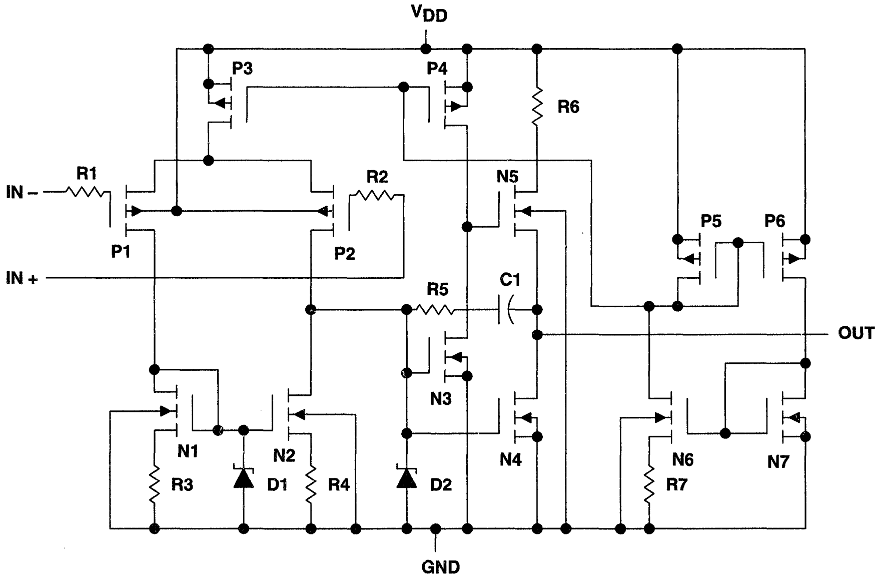
A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC27M2 and TLC27M7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	– 0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD}	45 mA
Total current out of GND	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix	0°C to 70°C
I suffix	–40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	–0.2	3.5	–0.2	3.5	0	3.5	V
	V_{DD} = 10 V	–0.2	8.5	–0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27M2C TLC27M2AC TLC27M2BC TLC27M7C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M2AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27M2BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 100 kΩ	25°C		220	2000	μV
				Full range			3000	
		TLC27M7C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 100 kΩ	25°C		185	500	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				0°C	3	3.9		
				70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				0°C	15	200		
				70°C	15	140		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		dB
				0°C	60	91		
				70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		
				70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		210	560	μA
				0°C		250	640	
				70°C		170	440	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27M2C TLC27M2AC TLC27M2BC TLC27M7C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27M2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		224	2000	µV
					Full range			3000	
		TLC27M7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		190	800	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					0°C	7.8	8.7		
					70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					0°C	15	320		
					70°C	15	230		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min		25°C	65	94		dB
					0°C	60	94		
					70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		285	600	µA
					0°C		345	800	
					70°C		220	560	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27M2I TLC27M2AI TLC27M2BI TLC27M7I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27M2AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			7	
		TLC27M2BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		220	2000	µV
					Full range			3500	
		TLC27M7I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		185	500	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					−40°C	3	3.9		
					85°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					−40°C	15	270		
					85°C	15	130		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min		25°C	65	91		dB
					−40°C	60	90		
					85°C	60	90		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−40°C	60	91		
					85°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		210	560	µA
					−40°C		315	800	
					85°C		160	400	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27M2I TLC27M2AI TLC27M2BI TLC27M7I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M2AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M2BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		224	2000	µV
				Full range			3500	
		TLC27M7I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		190	800	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				−40°C	7.8	8.7		
				85°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				−40°C	15	390		
				85°C	15	220		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	94		dB
				−40°C	60	93		
				85°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−40°C	60	91		
				85°C	60	94		
I_{DD}	Supply current		V_O = 5 V, V_{IC} = 5 V, No load	25°C		285	600	µA
				−40°C		450	900	
				85°C		205	520	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27M2M TLC27M7M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M7M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				−55°C	3	3.9		
				125°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				−55°C	15	290		
				125°C	15	120		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	91		dB
				−55°C	60	89		
				125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−55°C	60	91		
				125°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		210	560	μA
				−55°C		340	880	
				125°C		140	360	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27M2M TLC27M7M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M7M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		190	800	
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				125°C		1.8	15	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				125°C		10	35	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				−55°C	7.8	8.6		
				125°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				−55°C	15	420		
				125°C	15	190		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$	25°C	65	94		dB
				−55°C	60	93		
				125°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−55°C	60	91		
				125°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		285	600	µA
				−55°C		490	1000	
				125°C		180	480	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M2C TLC27M2AC TLC27M2BC TLC27M7C MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.43		V/µs
				0°C		0.46		
				70°C		0.36		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				0°C		600		
				70°C		400		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M2C TLC27M2AC TLC27M2BC TLC27M7C MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.62		V/µs
				0°C		0.67		
				70°C		0.51		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				0°C		44°		
				70°C		42°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M2I TLC27M2AI TLC27M2BI TLC27M7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.43		V/µs
				−40°C		0.51		
				85°C		0.35		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		MHz
				−40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M2I TLC27M2AI TLC27M2BI TLC27M7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.62		V/µs
				−40°C		0.77		
				85°C		0.47		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		MHz
				−40°C		880		
				85°C		480		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−40°C		46°		
				85°C		41°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M2M TLC27M7M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				−55°C		0.49		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−55°C		850		
				125°C		330		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−55°C		44°		
				125°C		36°		

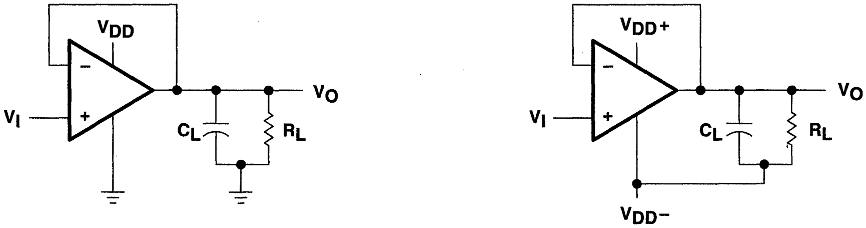
operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M2M TLC27M7M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−55°C		50		
				125°C		20		
B_1	Unity gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−55°C		960		
				125°C		440		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−55°C		47°		
				125°C		39°		

PARAMETER MEASUREMENT INFORMATION

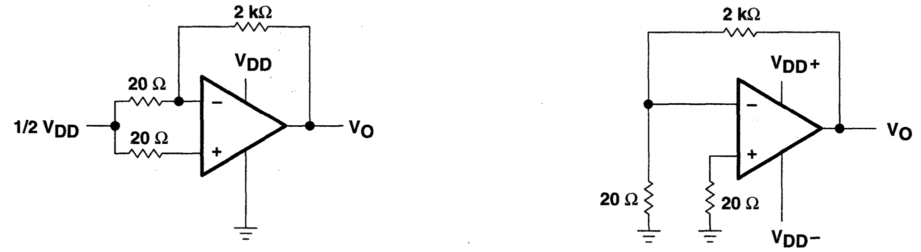
single-supply versus split-supply test circuits

Because the TLC27M2 and TLC27M7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



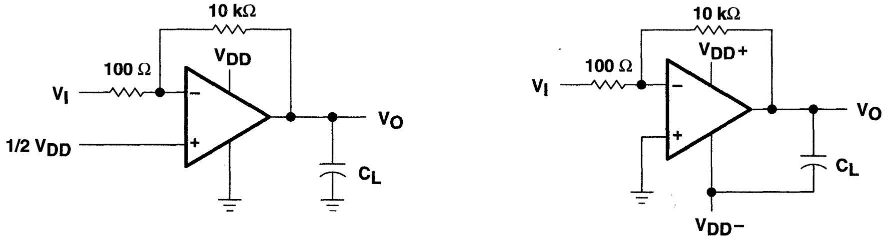
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27M2 and TLC27M7 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution ... many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

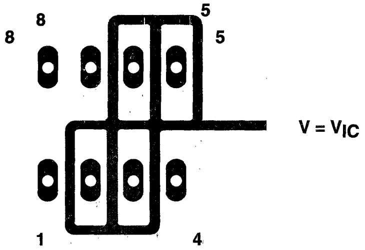


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

PARAMETER MEASUREMENT INFORMATION

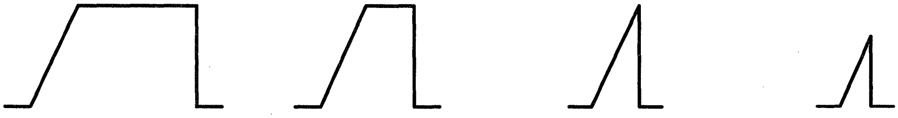
input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 1 kHz (b) B_{OM} > f > 1 kHz (c) f = B_{OM} (d) f > B_{OM}

Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
α_{VIO}	Temperature coefficient	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A_{VD}	Differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I_{IB}/I_{IO}	Input bias and input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitive loads	34 35 36
V_n	Equivalent input noise voltage	vs Frequency	37
ϕ	Phase shift	vs Frequency	32, 33

TYPICAL CHARACTERISTICS

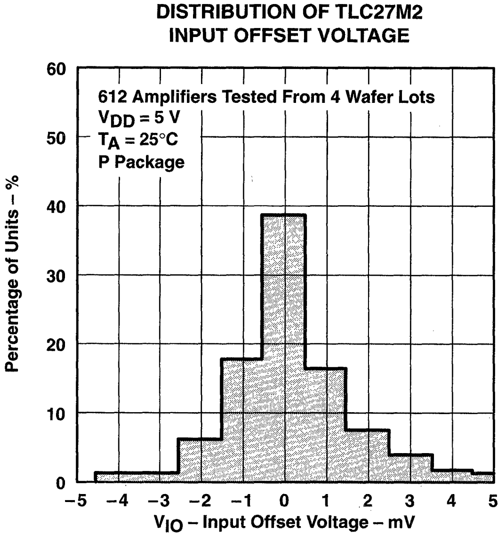


Figure 6

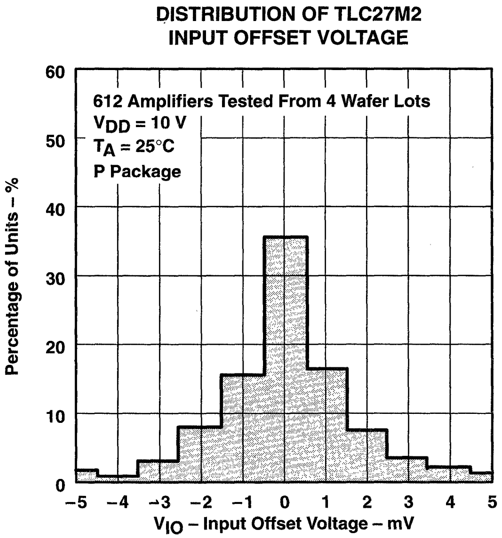


Figure 7

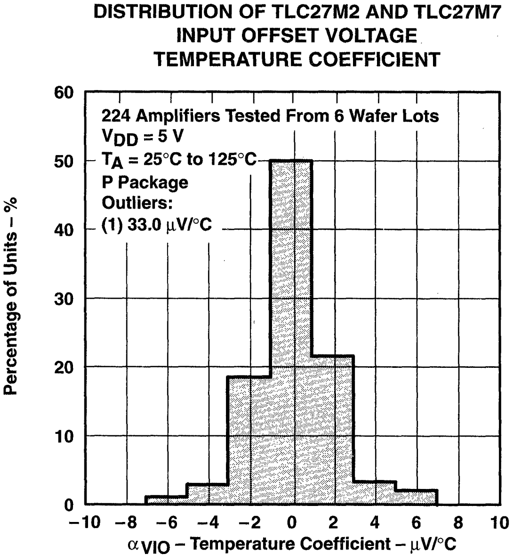


Figure 8

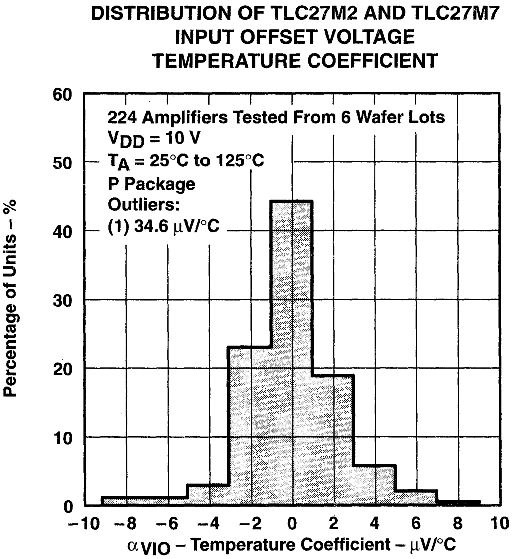


Figure 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

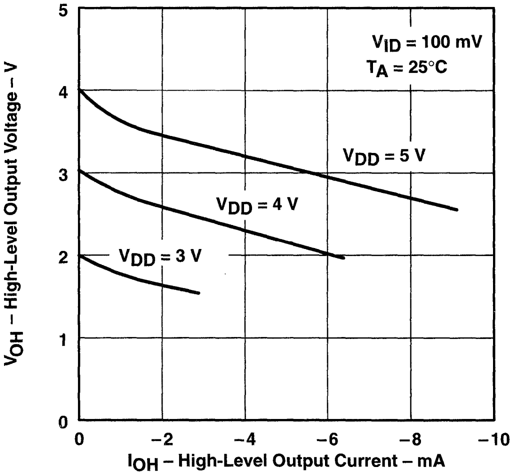


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

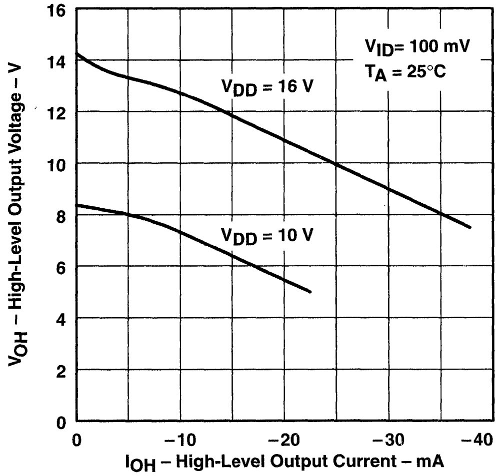


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

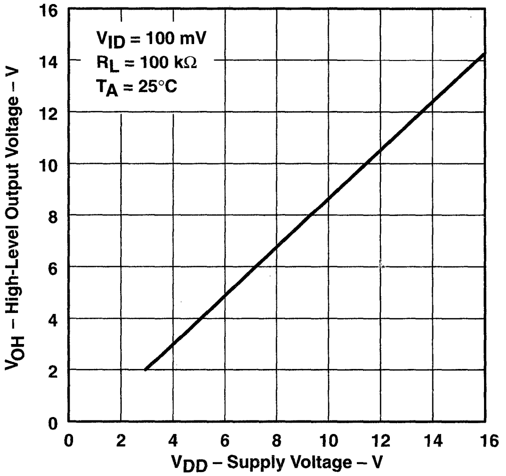


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

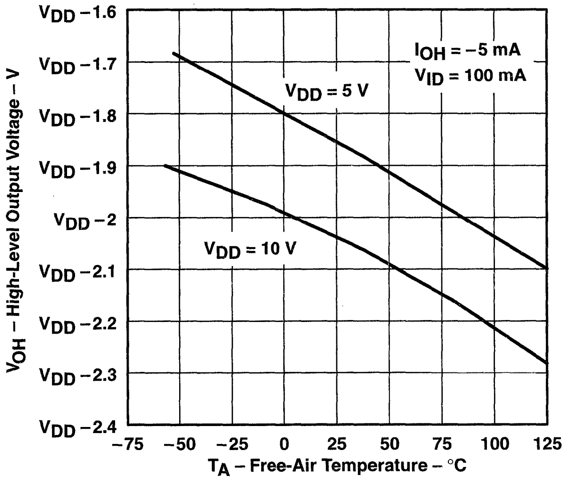


Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

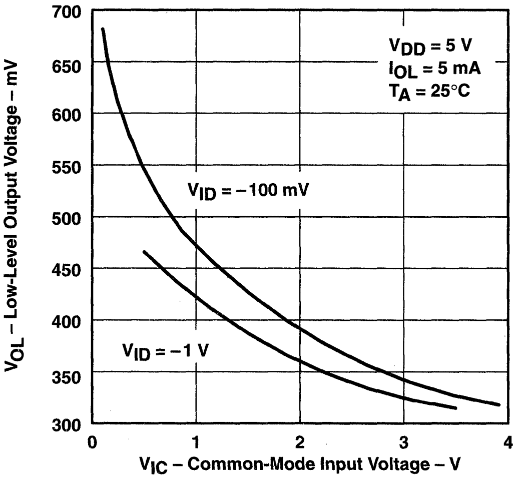

Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

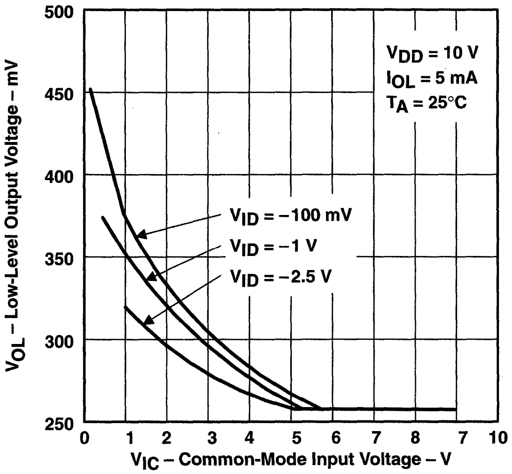

Figure 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

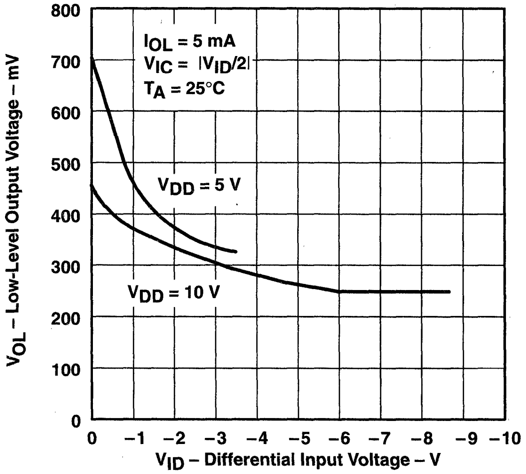

Figure 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

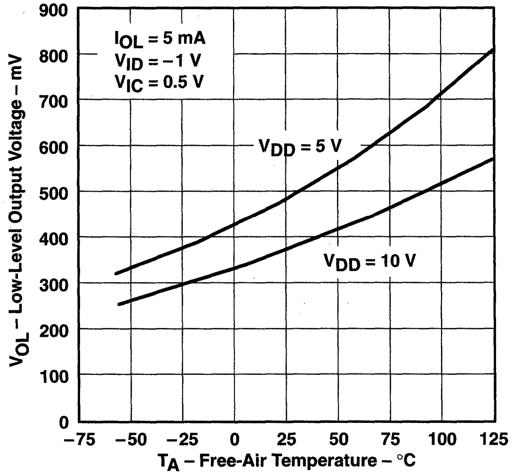

Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

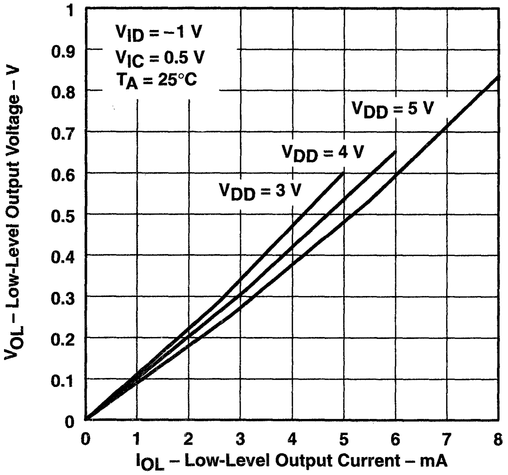

Figure 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

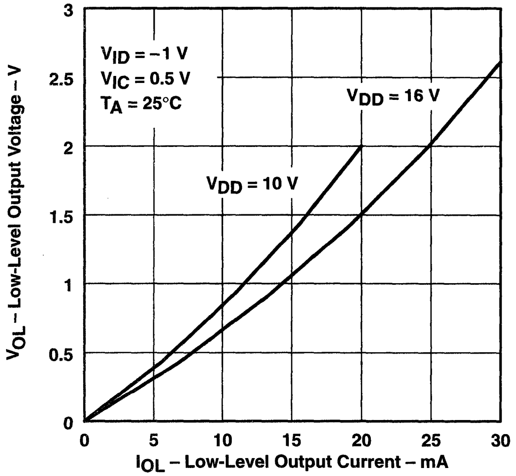

Figure 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

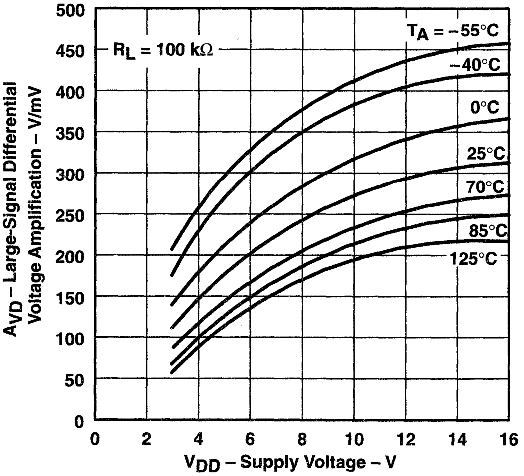

Figure 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

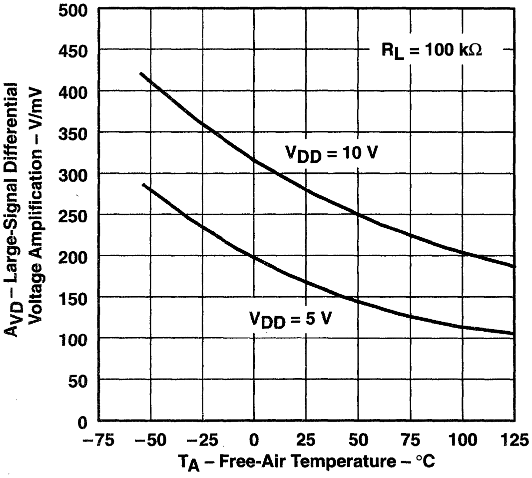

Figure 21

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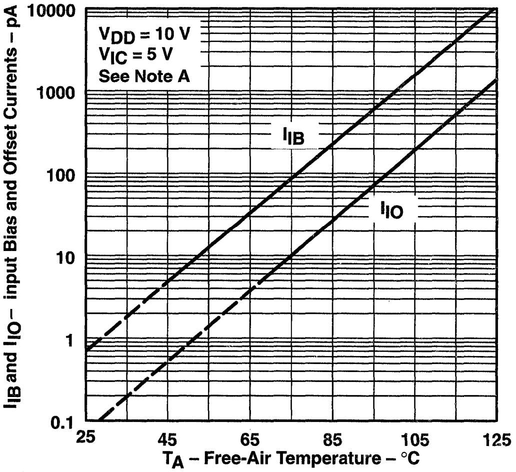
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

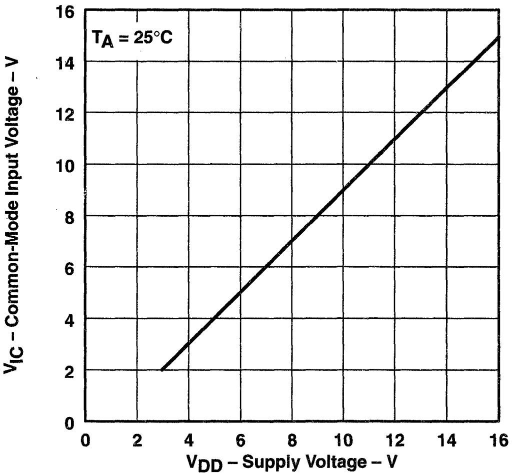


Figure 23

SUPPLY CURRENT vs SUPPLY VOLTAGE

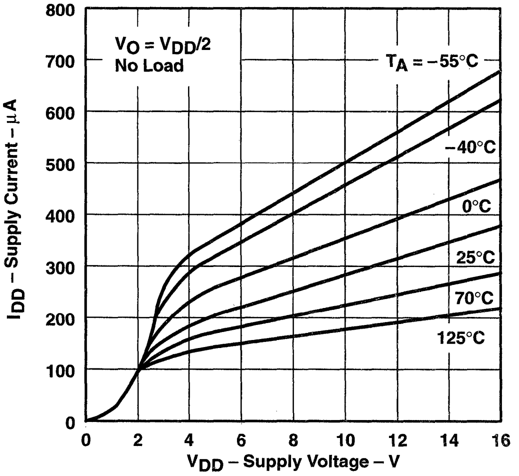


Figure 24

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

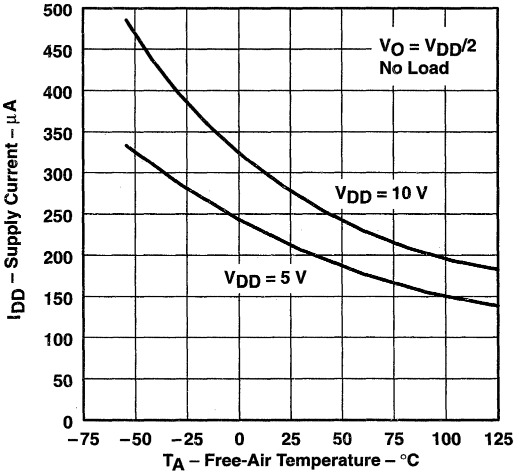


Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

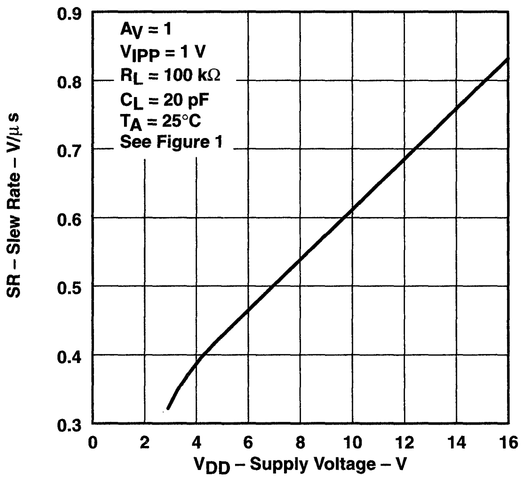

Figure 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

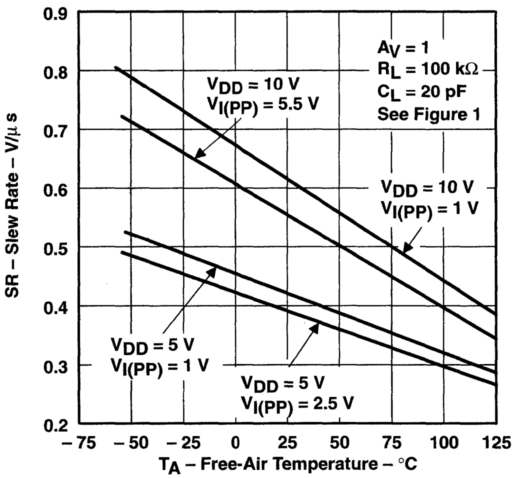

Figure 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

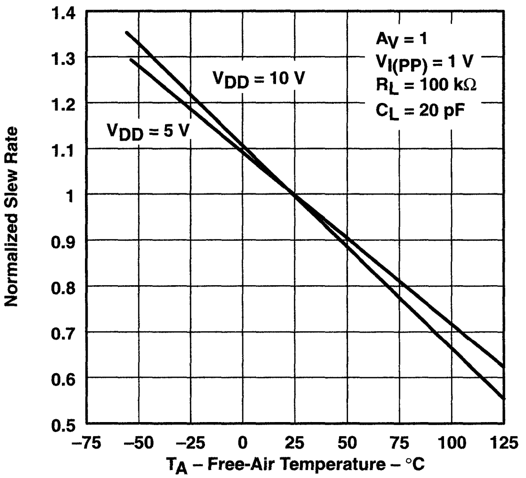

Figure 28

MAXIMUM PEAK-TO-PEAK OUTPUT
VOLTAGE
vs
FREQUENCY

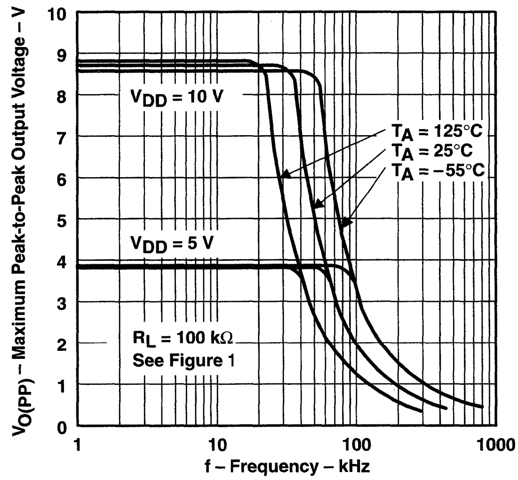

Figure 29

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

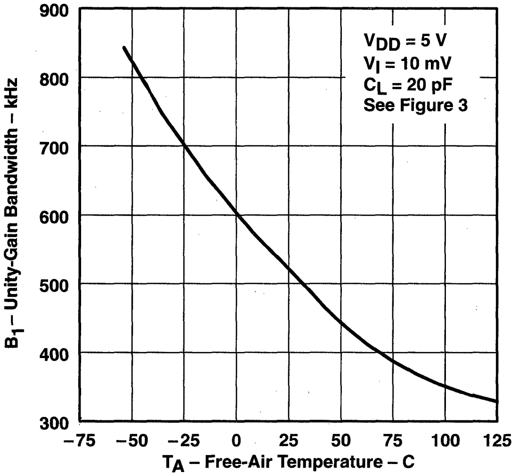
UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

Figure 30

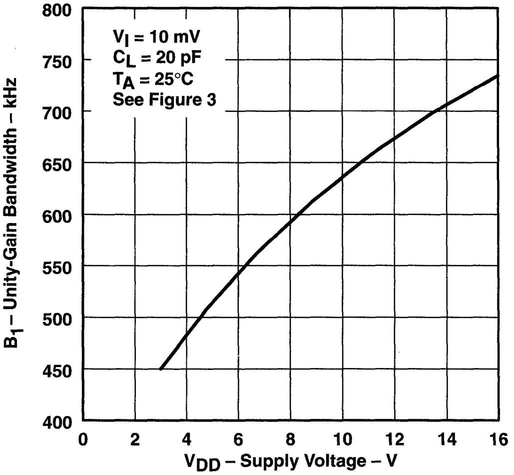
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

Figure 31

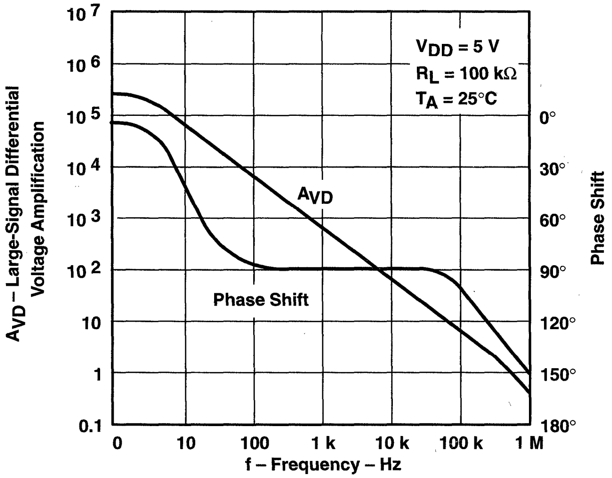
LARGE-SCALE DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

Figure 32

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SCALE DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

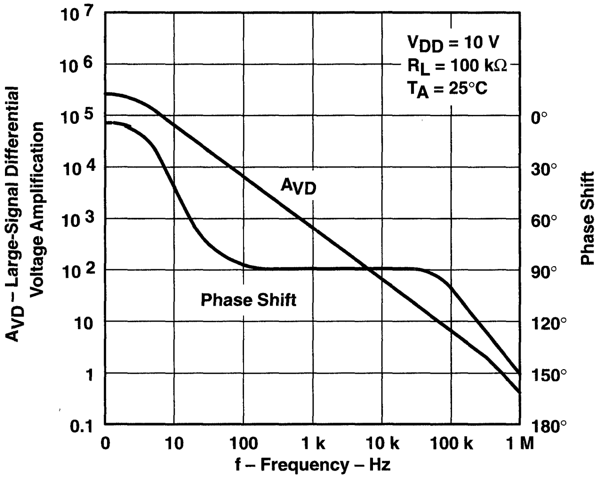

Figure 33

PHASE MARGIN vs SUPPLY VOLTAGE

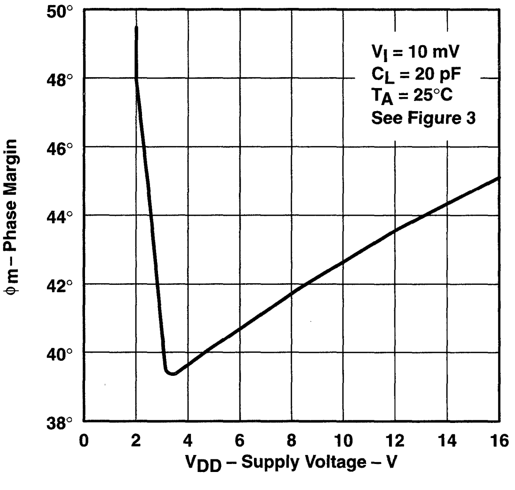

Figure 34

PHASE MARGIN vs FREE-AIR TEMPERATURE

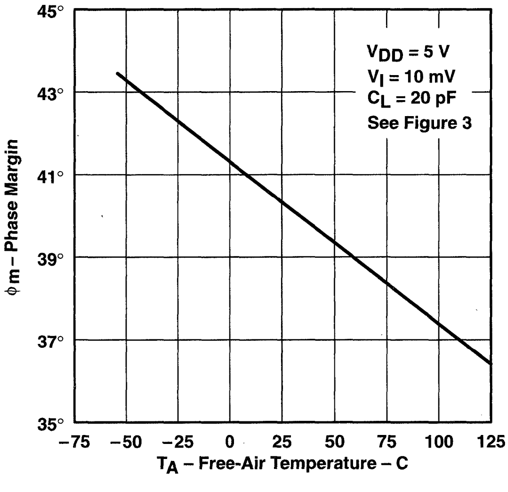

Figure 35

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN vs CAPACITIVE LOAD

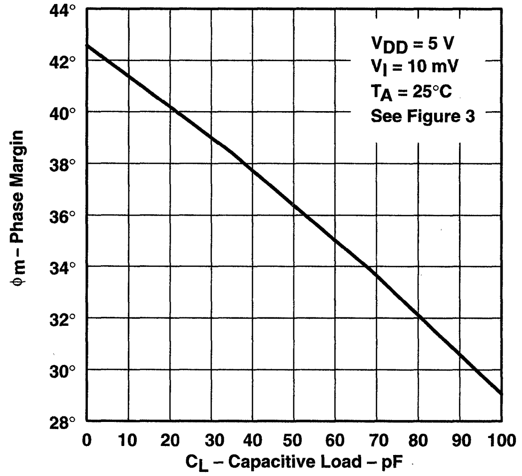


Figure 36

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

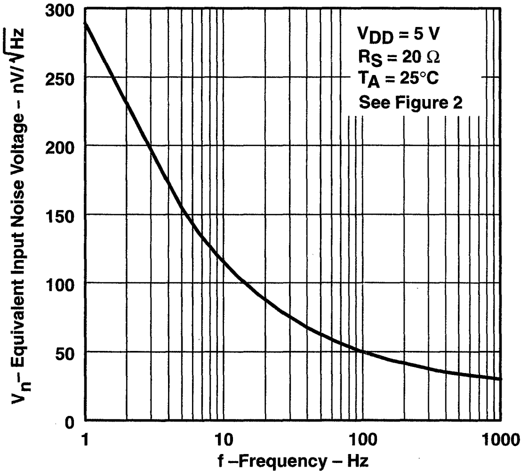


Figure 37

APPLICATION INFORMATION

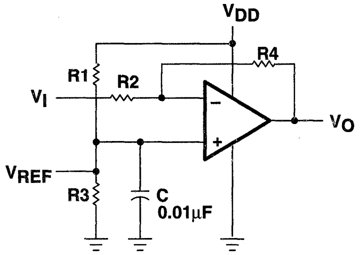
single-supply operation

While the TLC27M2 and TLC27M7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M2 and TLC27M7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M2 and TLC27M7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

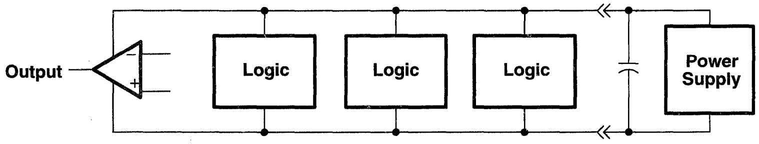
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



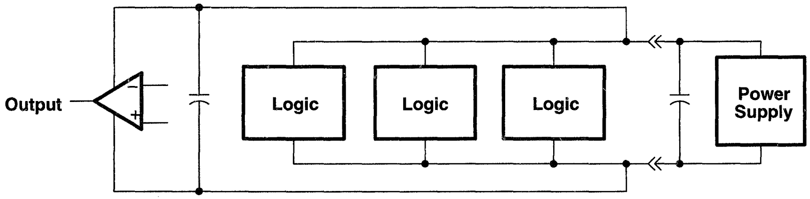
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

Figure 38. Inverting Amplifier With Voltage Reference



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common Versus Separate Supply Rails

APPLICATION INFORMATION

input characteristics

The TLC27M2 and TLC27M7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

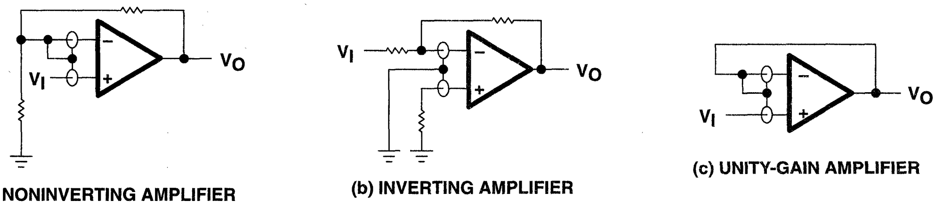
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M2 and TLC27M7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M2 and TLC27M7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M2 and TLC27M7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

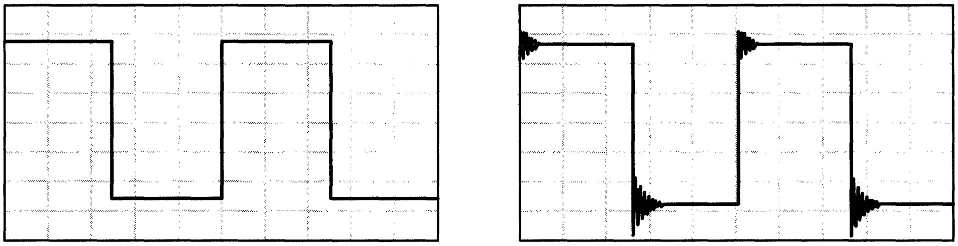
Figure 40. Guard-Ring Schemes

output characteristics

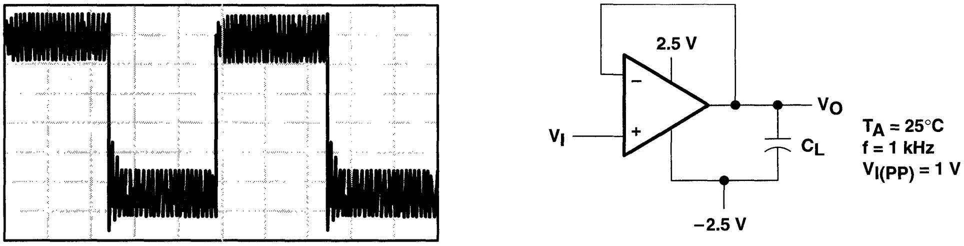
The output stage of the TLC27M2 and TLC27M7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M2 and TLC27M7 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

APPLICATION INFORMATION



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD



(c) C_L = 190 pF, R_L = NO LOAD (d) TEST CIRCUIT

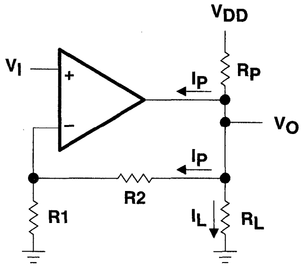
Figure 41. Effect of Capacitive Loads and Test Circuit

output characteristics (continued)

Although the TLC27M2 and TLC27M7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

APPLICATION INFORMATION

output characteristics (continued)



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

Ip = Pullup current required by the operational amplifier (typically 500 µA)

Figure 42. Resistive Pullup to Increase V_{OH}

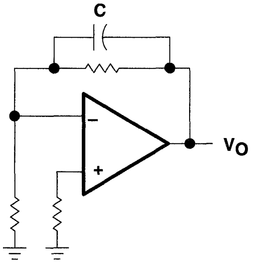


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic-discharge protection

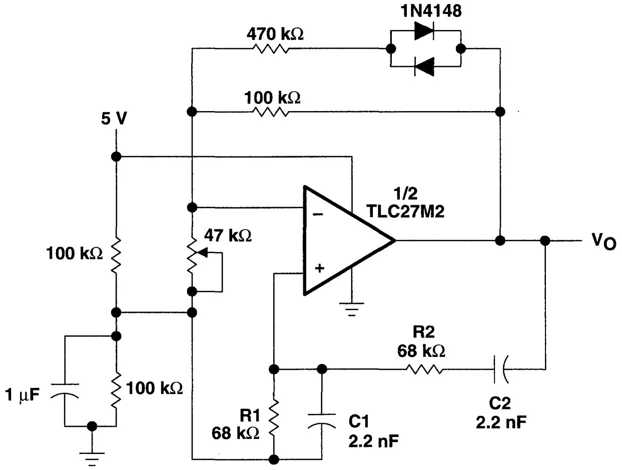
The TLC27M2 and TLC27M7 incorporate an internal electrostatic-discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27M2 and TLC27M7 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

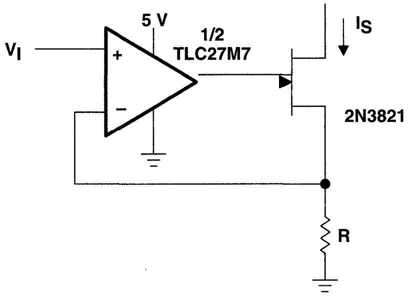
APPLICATION INFORMATION



NOTES: $V_{O(PP)} \approx 2\ V$

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

Figure 44. Wien Oscillator

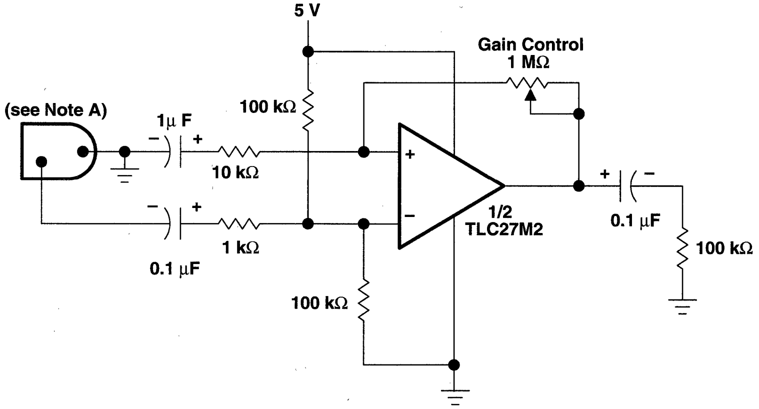


NOTES: $V_I = 0\ V\ to\ 3\ V$

$$I_S = \frac{V_I}{R}$$

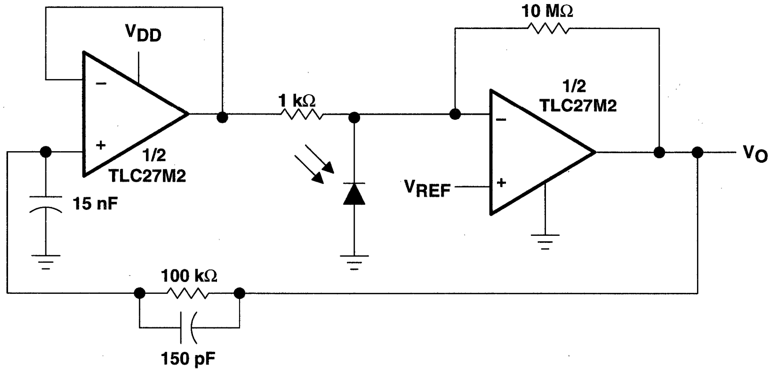
Figure 45. Precision Low-Current Sink

APPLICATION INFORMATION



NOTE A: Low to medium impedance dynamic mike

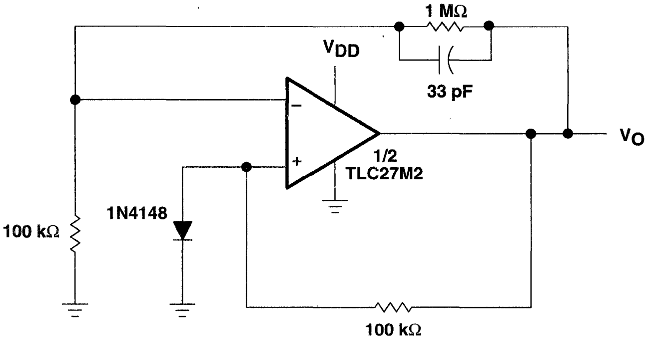
Figure 46. Microphone Preamplifier



NOTES: V_{DD} = 4 V to 15 V
V_{ref} = 0 V to V_{DD} – 2 V

Figure 47. Photo-Diode Amplifier With Ambient Light Rejection

APPLICATION INFORMATION



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

Figure 48. 5-V Low-Power Voltage Regulator

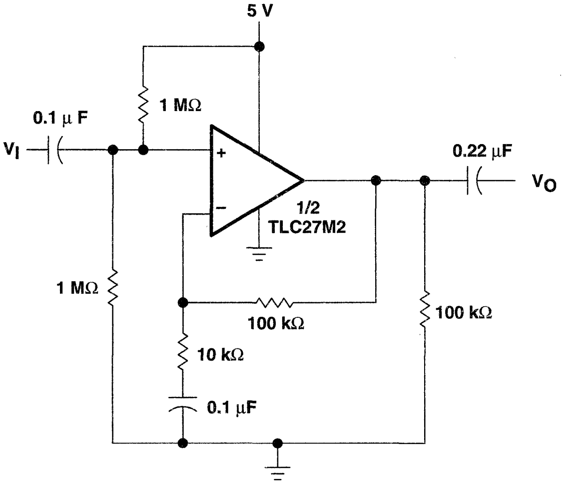


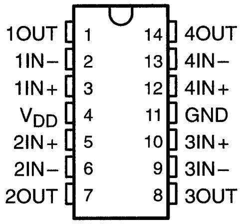
Figure 49. Single-Rail AC Amplifiers

TLC274, TLC274A, TLC274B, TLC274Y, TLC279
LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

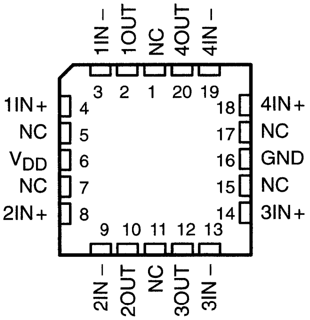
SLOS092B – SEPTEMBER 1987 – REVISED AUGUST 1994

- **Trimmed Offset Voltage:**
  TLC279 . . . 900 μV Max at 25°C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  −55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix and I-Suffix Versions)**
- **Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, J, N, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

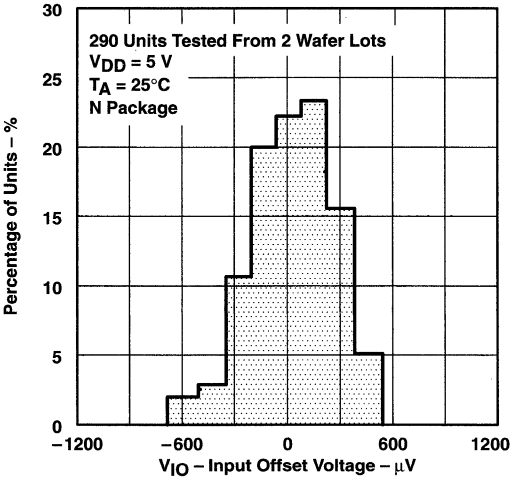
description

The TLC274 and TLC279 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC274 (10 μV) to the high-precision TLC279 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

DISTRIBUTION OF TLC279
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

description (continued)

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC274 and TLC279. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC274 and TLC279 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

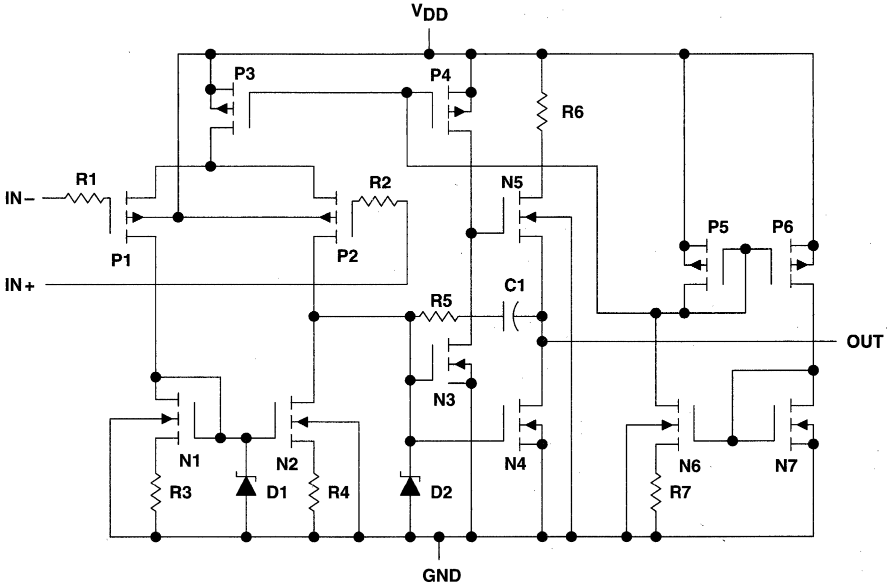
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	900 μV 2 mV 5 mV 10 mV	TLC279CD TLC274BCD TLC274ACD TLC274CD	— — — —	— — — —	TLC279CN TLC274BCN TLC274ACN TLC274CN	— — — TLC274CPW	— — — TLC274Y
–40°C to 85°C	900 μV 2 mV 5 mV 10 mV	TLC279ID TLC274BID TLC274AID TLC274ID	— — — —	— — — —	TLC279IN TLC274BIN TLC274AIN TLC274IN	— — — —	— — — —
–55°C to 125°C	900 μV 10 mV	TLC279MD TLC274MD	TLC279MFK TLC274MFK	TLC279MJ TLC274MJ	TLC279MN TLC274MN	— —	— —

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC279CDR).

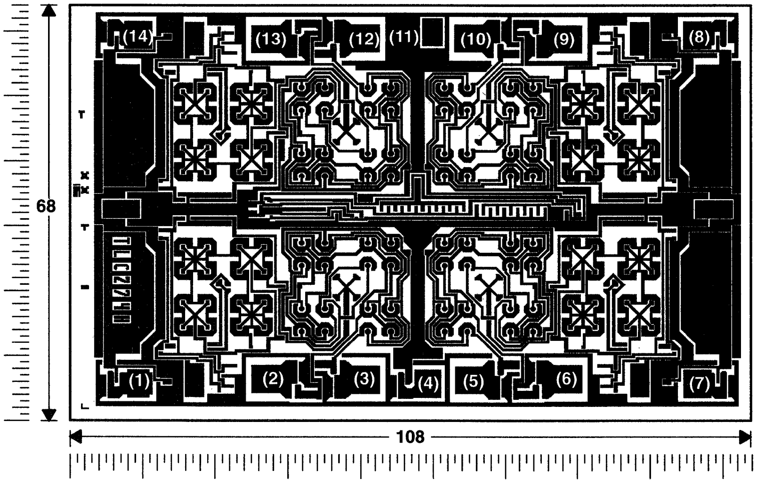
equivalent schematic (each amplifier)

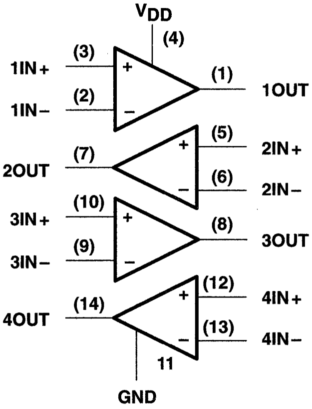


TLC274Y chip information

These chips, when properly assembled, display characteristics similar to the TLC274C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD}	45 mA
Total current out of GND	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	—
PW	700 mW	5.6 mW/°C	448 mW	—	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	−0.2	3.5	−0.2	3.5	0	3.5	V
	$V_{DD} = 10$ V	−0.2	8.5	−0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC274C, TLC274AC, TLC274BC, TLC279C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC274AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC274BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		340	2000	µV
				Full range			3000	
		TLC279C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				0°C	3	3.8		
				70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				0°C	4	27		
				70°C	4	20		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	80		dB
				0°C	60	84		
				70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		2.7	6.4	mA
				0°C		3.1	7.2	
				70°C		2.3	5.2	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC274C, TLC274AC, TLC274BC, TLC279C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC274AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC274BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		390	2000	µV
				Full range			3000	
		TLC279C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O =.5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				0°C	7.8	8.5		
				70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				0°C	7.5	42		
				70°C	7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	85		dB
				0°C	60	88		
				70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		3.8	8	mA
				0°C		4.5	8.8	
				70°C		3.2	6.8	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC274I, TLC274AI, TLC274BI, TLC279I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC274AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			7	
		TLC274BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		340	2000	μV
				Full range			3500	
		TLC279I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				−40°C	3	3.8		
				85°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				−40°C	3.5	32		
				85°C	3.5	19		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		dB
				−40°C	60	81		
				85°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−40°C	60	92		
				85°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		2.7	6.4	mA
				−40°C		3.8	8.8	
				85°C		2.1	4.8	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC274I, TLC274AI, TLC274BI, TLC279I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC274AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			7	
		TLC274BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		390	2000	µV
				Full range			3500	
		TLC279I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				−40°C	7.8	8.5		
				85°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				−40°C	7	47		
				85°C	7	31		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	85		dB
				−40°C	60	87		
				85°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−40°C	60	92		
				85°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		3.8	8	mA
				−40°C		5.5	10	
				85°C		2.9	6.4	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC274M, TLC279M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC279M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				−55°C	3	3.8		
				125°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				−55°C	3.5	35		
				125°C	3.5	16		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	80		dB
				−55°C	60	81		
				125°C	60	84		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−55°C	60	90		
				125°C	60	97		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		2.7	6.4	mA
				−55°C		4	10	
				125°C		1.9	4.4	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless) otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC274M, TLC279M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC279M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	µV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				−55°C	7.8	8.5		
				125°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				−55°C	7	50		
				125°C	7	27		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	85		dB
				−55°C	60	87		
				125°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−55°C	60	90		
				125°C	60	97		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		3.8	8	mA
				−55°C		6.0	12	
				125°C		2.5	5.6	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC274C, TLC274AC, TLC274AC, TLC274BC, TLC279C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 10\ \Omega$, $C_L = 20$ pF, See Figure 1	$V_{IPP} = 1$ V	25°C		3.6		V/µs
				0°C		4		
				70°C		3		
			$V_{IPP} = 2.5$ V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20\ \Omega$,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10$ kΩ,	$C_L = 20$ pF, See Figure 1	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, See Figure 3	$C_L = 20$ pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	$V_I = 10$ mV, $C_L = 20$ pF,	$f = B_1$,	25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC274C, TLC274AC, TLC274AC, TLC274BC, TLC279C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 10\ \Omega$, $C_L = 20$ pF, See Figure 1	$V_{IPP} = 1$ V	25°C		5.3		V/µs
				0°C		5.9		
				70°C		4.3		
			$V_{IPP} = 5.5$ V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20\ \Omega$,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10$ kΩ,	$C_L = 20$ pF, See Figure 1	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, See Figure 3	$C_L = 20$ pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	$V_I = 10$ mV, $C_L = 20$ pF,	$f = B_1$, See Figure 3	25°C		49°		
				0°C		50°		
				70°C		46°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC274I, TLC274AI, TLC274BI, TLC279I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−40°C		4.5		
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				−40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−40°C		380		
				85°C		250		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−40°C		49°		
				85°C		43°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC274I, TLC274AI, TLC274BI, TLC279I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 Ω, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−40°C		6.7		
				85°C		4		
			V_{IPP} = 5.5 V	25°C		4.6		
				−40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−40°C		52°		
				85°C		46°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC274M, TLC279M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC274M, TLC279M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 Ω , C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−55°C		52°		
				125°C		44°		

electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC274Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 2.5 V, V_{IC} = 2.5 V		0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 2.5 V, V_{IC} = 2.5 V		0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 10 kΩ	3.2	3.8		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V to 2 V, R_L = 10 kΩ	5	23		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	65	95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, V_{IC} = 2.5 V, No load		2.7	6.4	mA

electrical characteristics, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC274Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 5 V, V_{IC} = 5 V		0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 5 V, V_{IC} = 5 V		0.7		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 9	−0.3 to 9.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 10 kΩ	8	8.5		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 6 V, R_L = 10 kΩ	10	36		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	65	85		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	65	95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 5 V, V_{IC} = 5 V, No load		3.8	8	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TLC274Y			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, See Figure 1	C_L = 20 pF,	V_{IPP} = 1 V		3.6		V/μs
				V_{IPP} = 2.5 V		2.9		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω,	See Figure 2		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, See Figure 1	C_L = 20 pF,	R_L = 10 kΩ,		320		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF,	See Figure 3		1.7		MHz
ϕ_m	Phase margin	V_I = 10 mV, See Figure 3	f = B_1,	C_L = 20 pF,		46°		

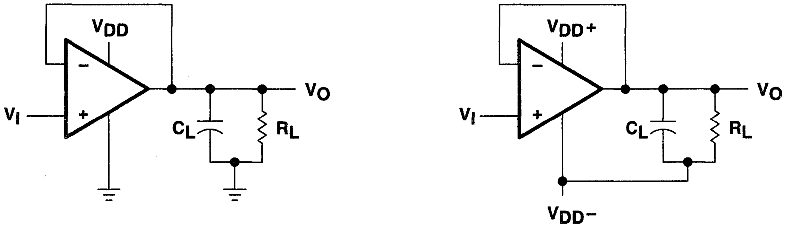
operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TLC274Y			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, See Figure 1	C_L = 20 pF,	V_{IPP} = 1 V		5.3		V/μs
				V_{IPP} = 5.5 V		4.6		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω,	See Figure 2		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, See Figure 1	C_L = 20 pF,	R_L = 10 kΩ,		200		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF,	See Figure 3		2.2		MHz
ϕ_m	Phase margin	V_I = 10 mV, See Figure 3	f = B_1,	C_L = 20 pF,		49°		

PARAMETER MEASUREMENT INFORMATION

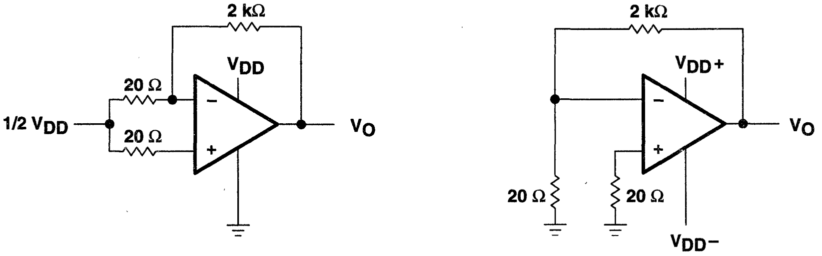
single-supply versus split-supply test circuits

Because the TLC274 and TLC279 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



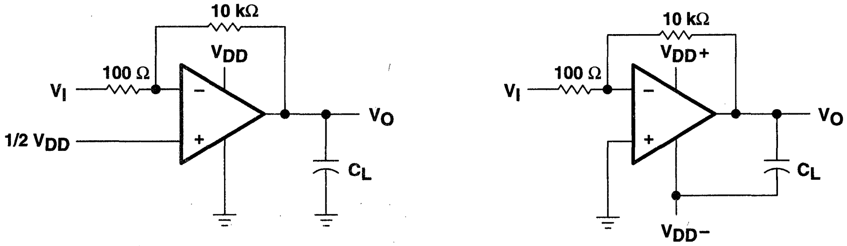
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC274 and TLC279 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

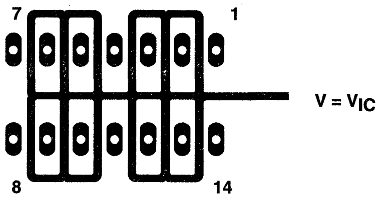


Figure 4. Isolation Metal Around Device Inputs (J and N packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

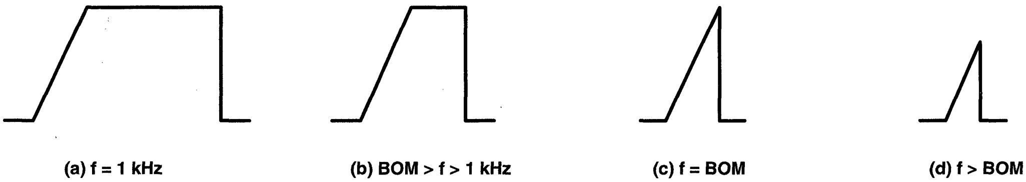
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.


(a) f = 1 kHz

(b) BOM > f > 1 kHz

(c) f = BOM

(d) f > BOM

Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
αV_{IO}	Temperature coefficient of input offset voltage	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I_{IB}	Input bias current	vs Free-air temperature	22
I_{IO}	Input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
V_n	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33

TYPICAL CHARACTERISTICS

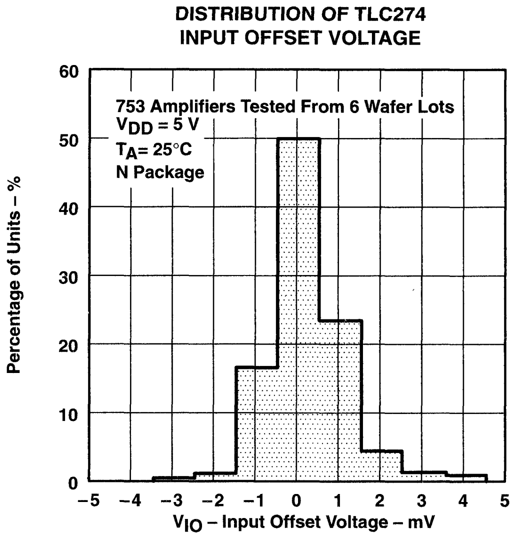


Figure 6

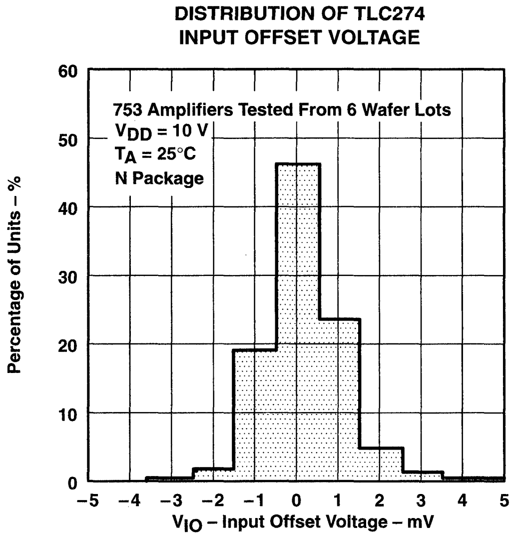


Figure 7

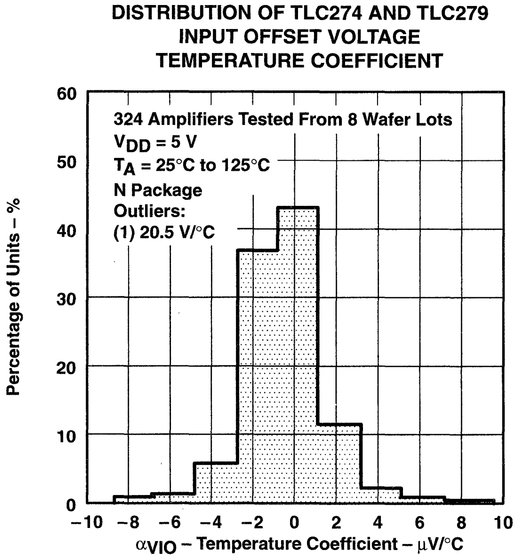


Figure 8

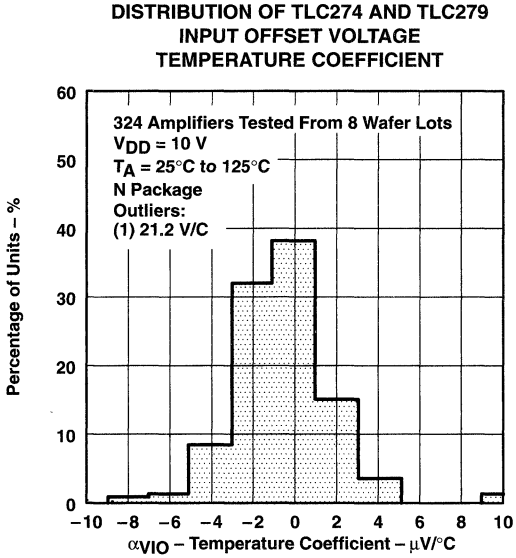


Figure 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

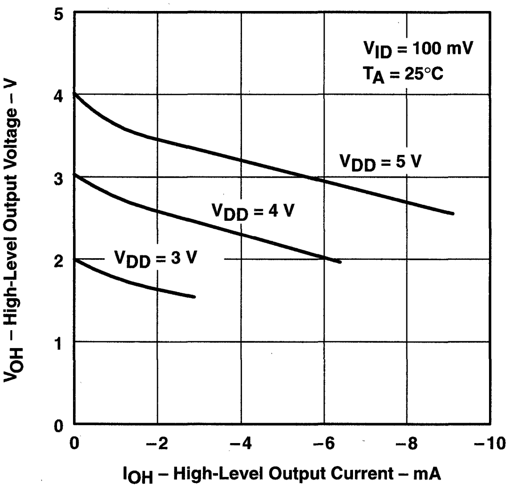


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

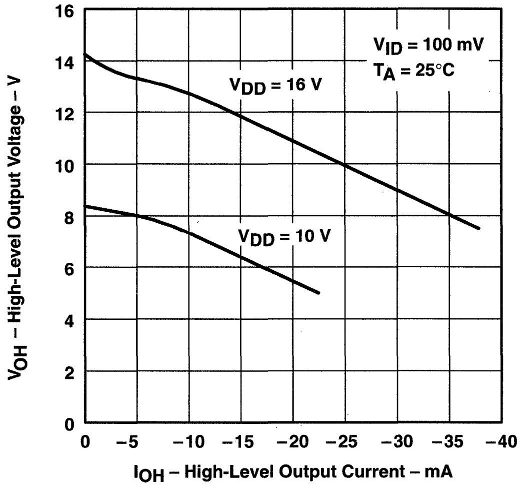


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

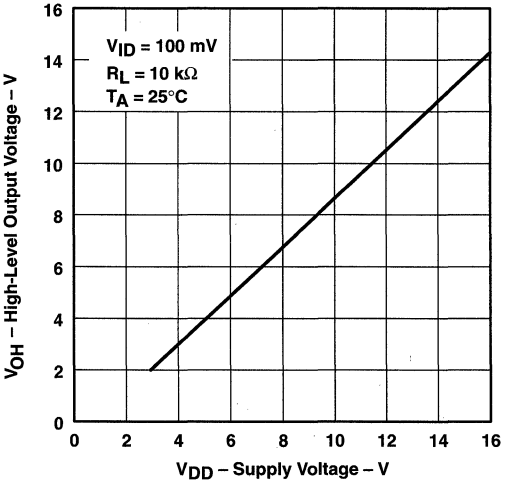


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

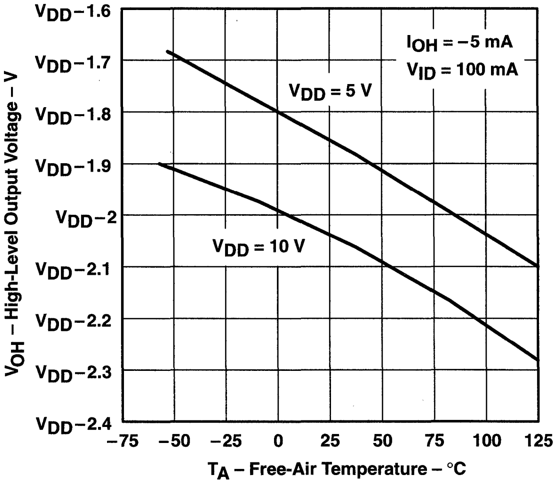


Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

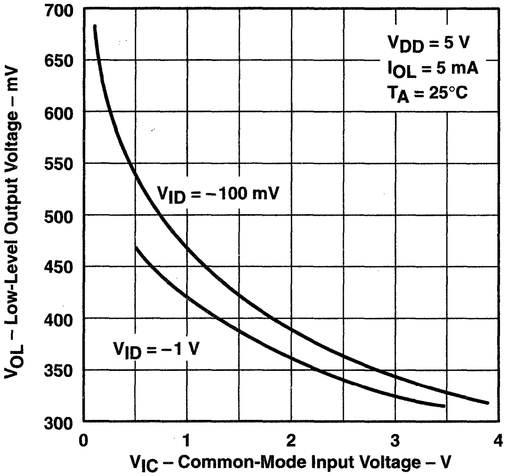

Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

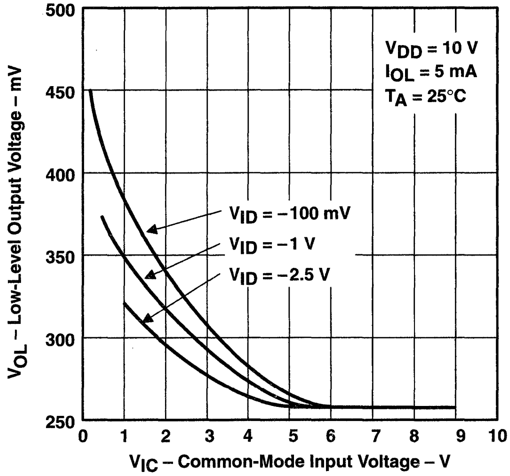

Figure 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

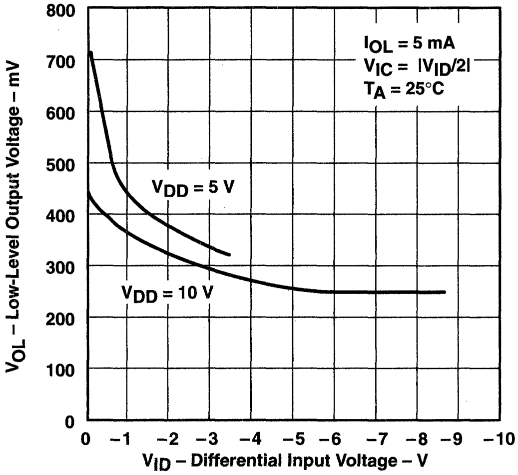

Figure 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

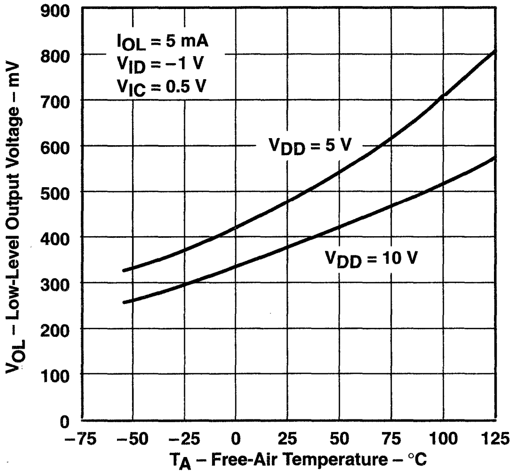

Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

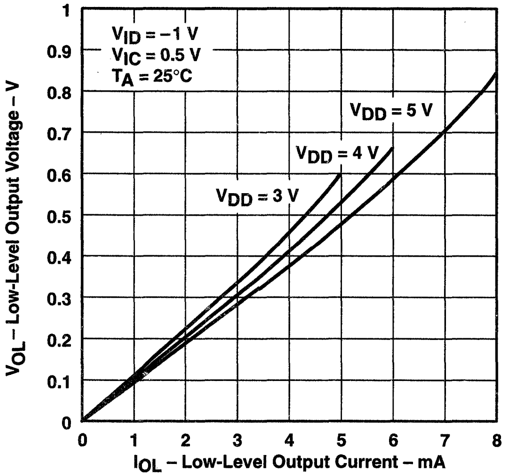

Figure 18

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

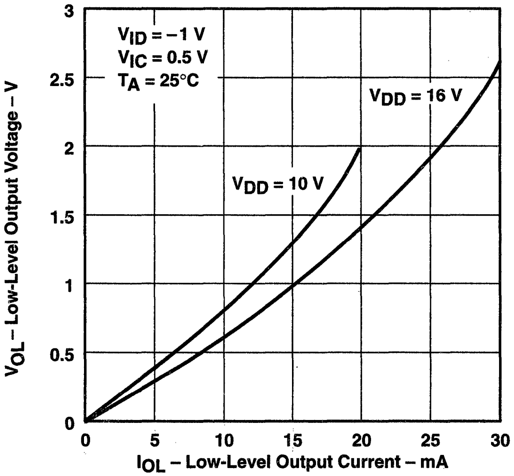

Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

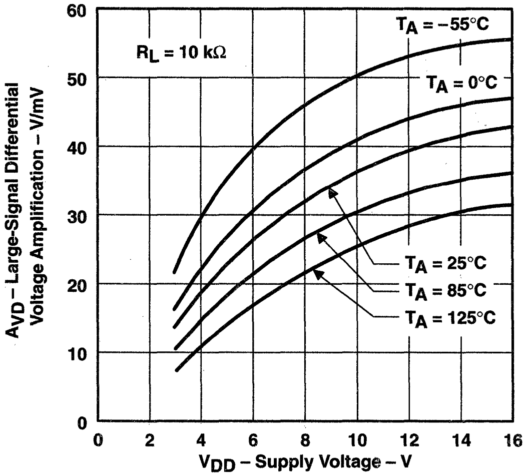

Figure 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

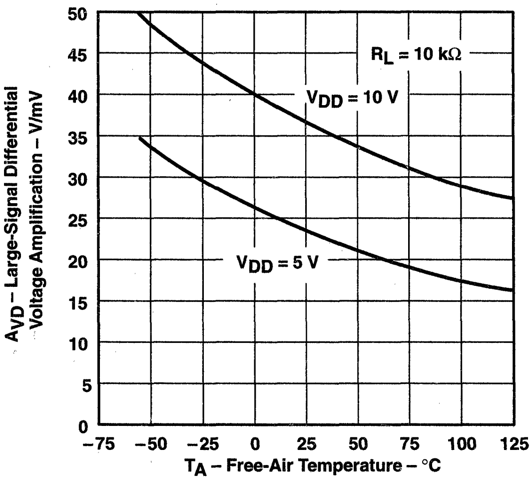

Figure 21

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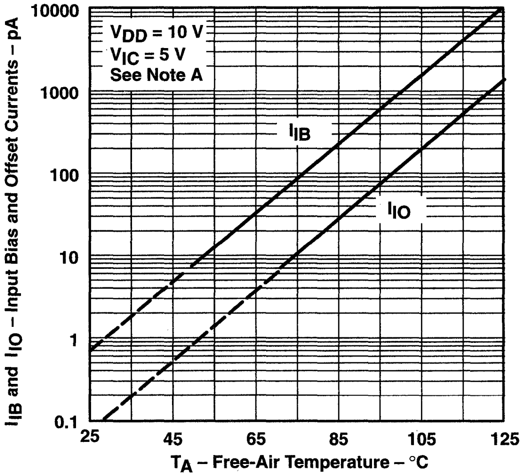
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

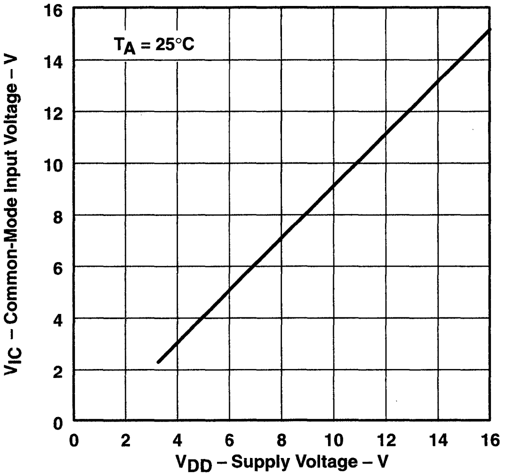


Figure 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

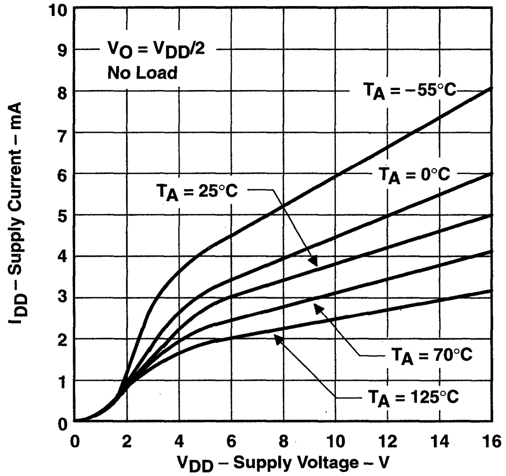


Figure 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

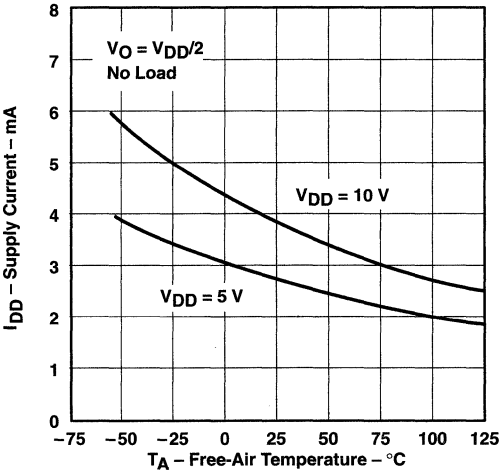


Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs SUPPLY VOLTAGE

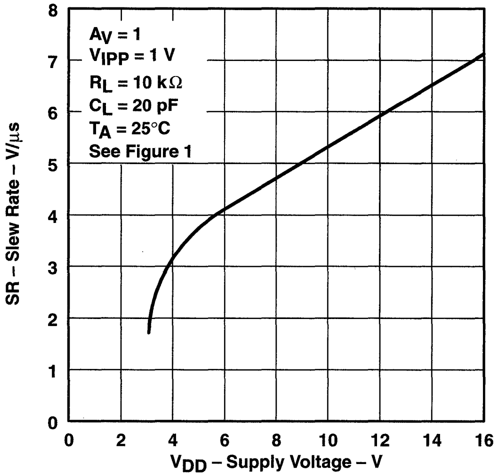

Figure 26

SLEW RATE vs FREE-AIR TEMPERATURE

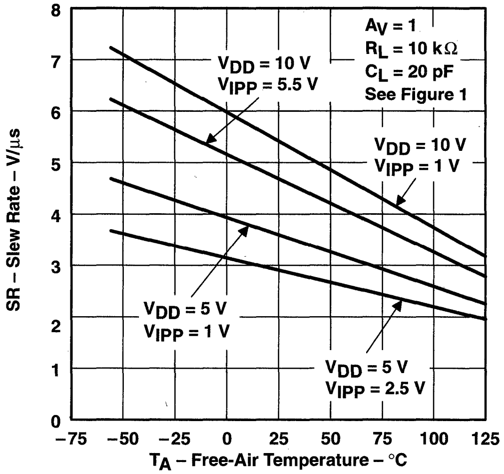

Figure 27

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

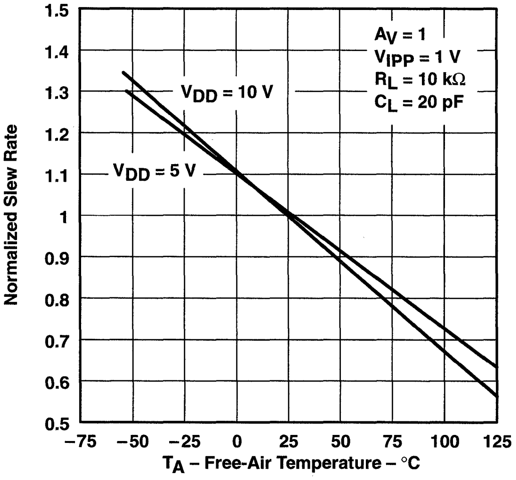

Figure 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

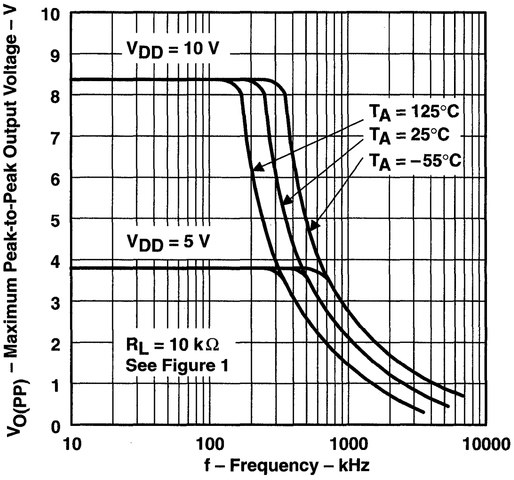

Figure 29

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

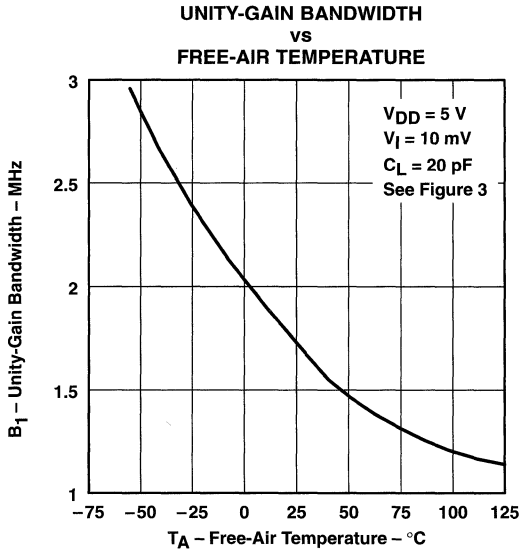

Figure 30

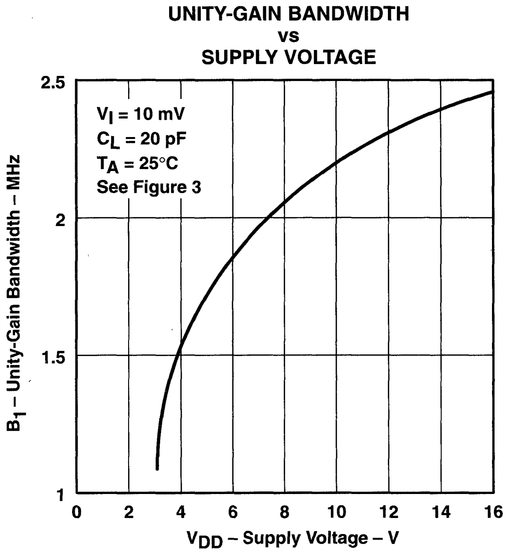

Figure 31

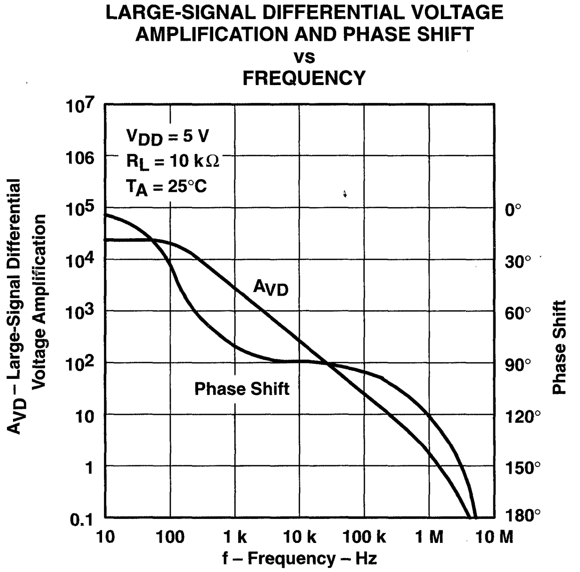

Figure 32

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

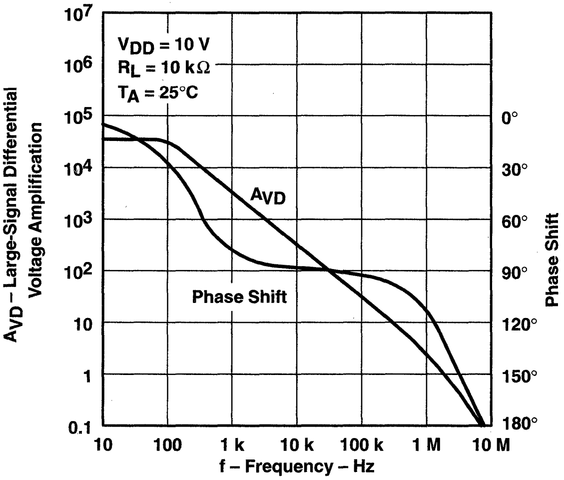

Figure 33

PHASE MARGIN vs SUPPLY VOLTAGE

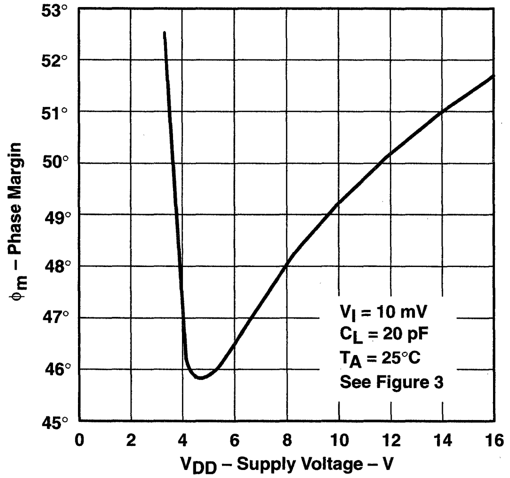

Figure 34

PHASE MARGIN vs FREE-AIR TEMPERATURE

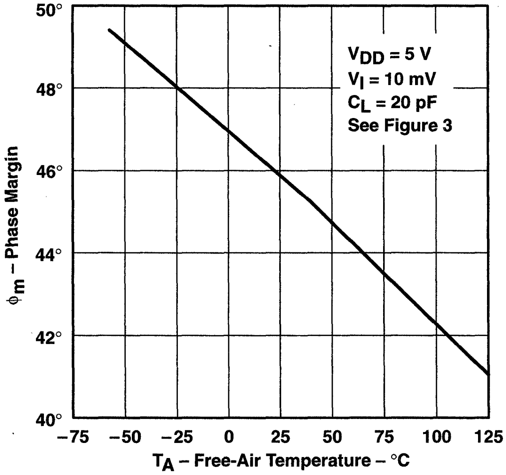

Figure 35

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
CAPACITIVE LOAD

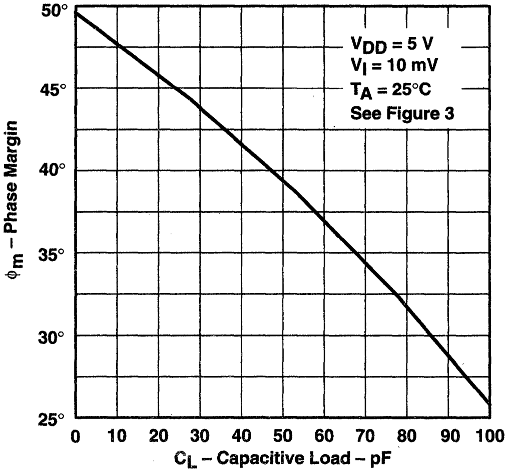


Figure 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

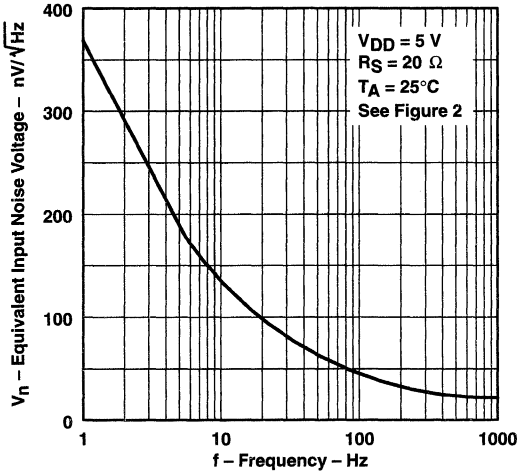


Figure 37

APPLICATION INFORMATION

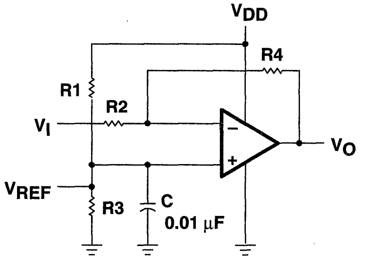
single-supply operation

While the TLC274 and TLC279 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC274 and TLC279 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC274 and TLC279 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

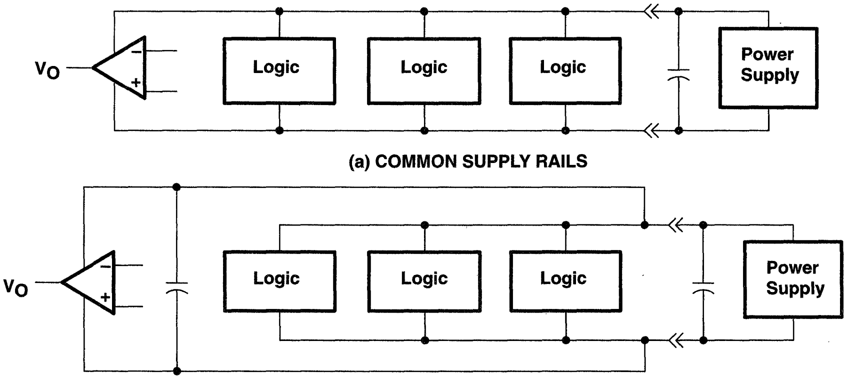
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require R_C decoupling.



$$V_{REF} = V_{DD}\,\frac{R3}{R1 + R3}$$

$$V_O = (V_{REF} - V_I)\,\frac{R4}{R2} + V_{REF}$$

Figure 38. Inverting Amplifier With Voltage Reference



(a) COMMON SUPPLY RAILS

(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common Versus Separate Supply Rails

APPLICATION INFORMATION

input characteristics

The TLC274 and TLC279 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

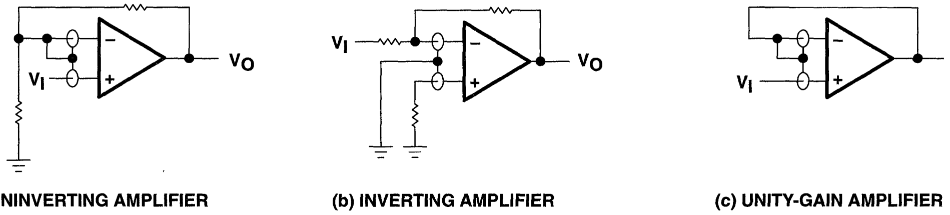
The use of the polysilicon-gate process and the careful input circuit design gives the TLC274 and TLC279 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC274 and TLC279 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC274 and TLC279 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 40. Guard-Ring Schemes

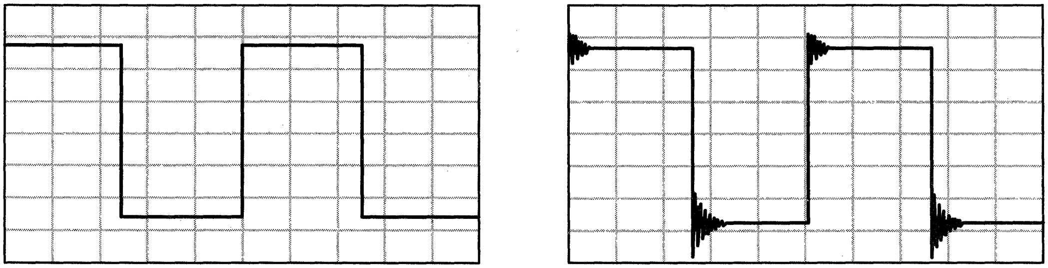
output characteristics

The output stage of the TLC274 and TLC279 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC274 and TLC279 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

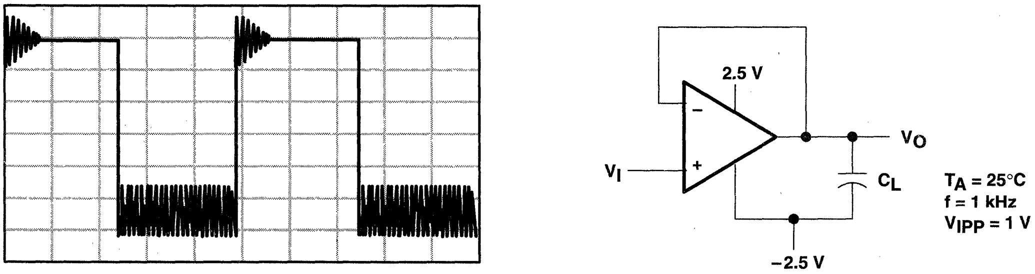
APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 130 pF, R_L = NO LOAD



(c) C_L = 150 pF, R_L = NO LOAD

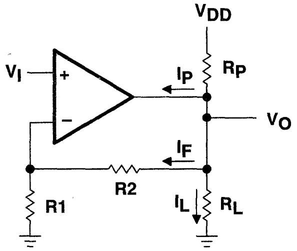
(d) TEST CIRCUIT

Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC274 and TLC279 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

APPLICATION INFORMATION

output characteristics (continued)



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 μA)

Figure 42. Resistive Pullup to Increase V_{OH}

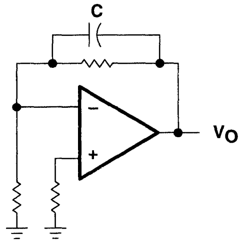


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

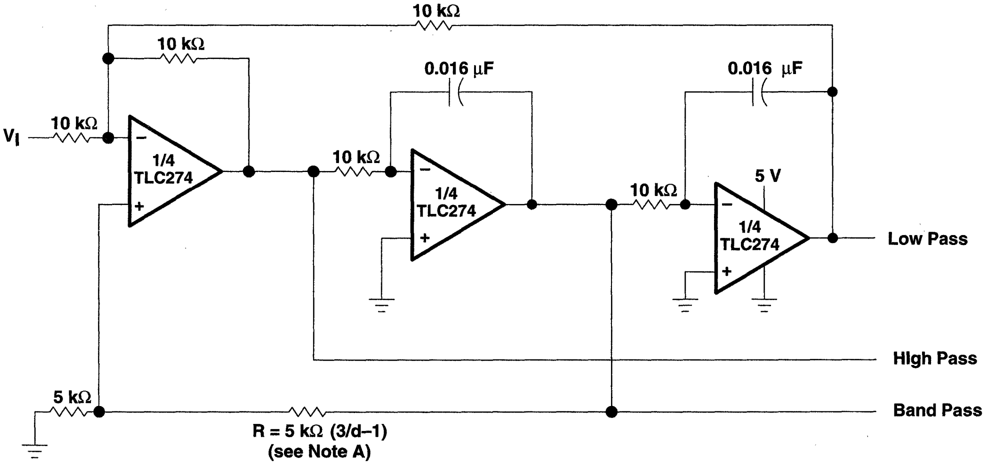
The TLC274 and TLC279 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature-dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC274 and TLC279 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

APPLICATION INFORMATION



NOTE A: d = damping factor, 1/Q

Figure 44. State-Variable Filter

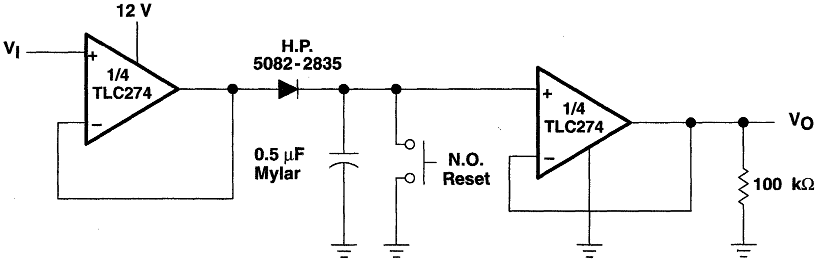
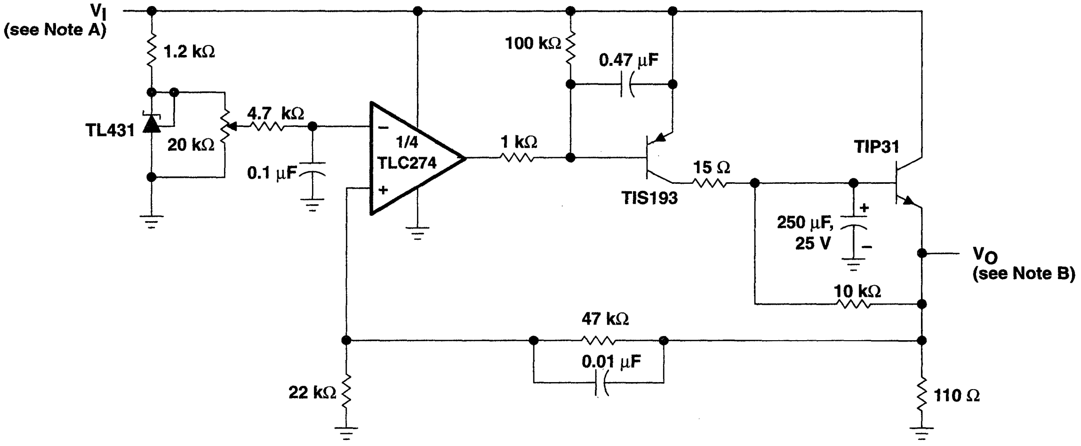


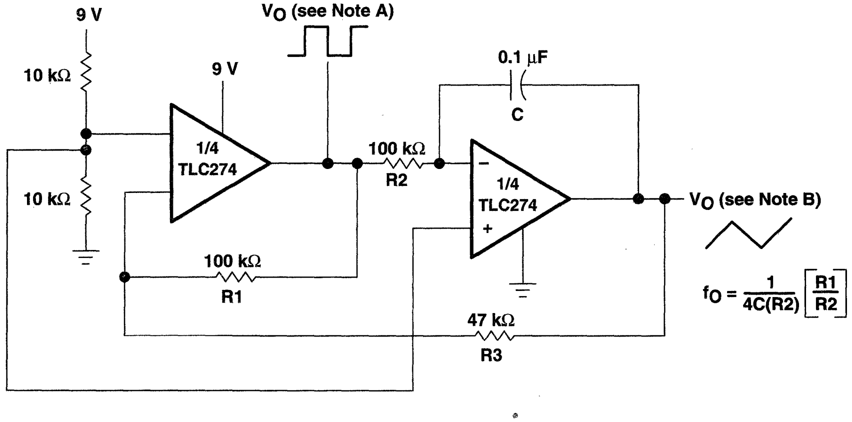
Figure 45. Positive-Peak Detector

APPLICATION INFORMATION



NOTES: B. V_I = 3.5 V to 15 V
C. V_O = 2 V, 0 to 1 A

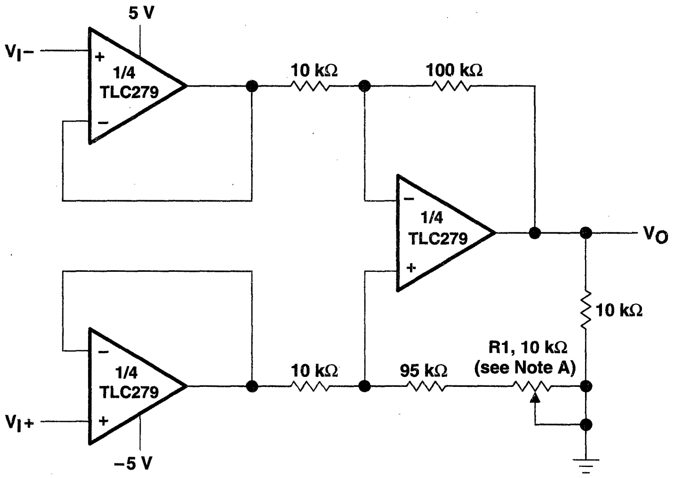
Figure 46. Logic-Array Power Supply



NOTES: A. $V_{O(PP)}$ = 8 V
B. $V_{O(PP)}$ = 4 V

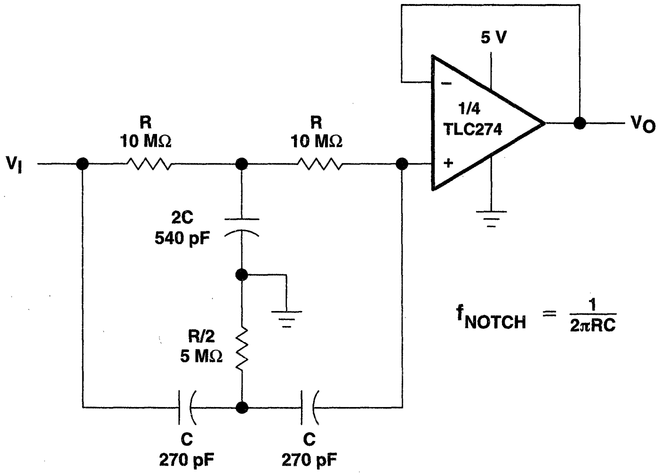
Figure 47. Single-Supply Function Generator

APPLICATION INFORMATION



NOTE C: CMRR adjustment must be noninductive.

Figure 48. Low-Power Instrumentation Amplifier



$$f_{NOTCH} = \frac{1}{2\pi RC}$$

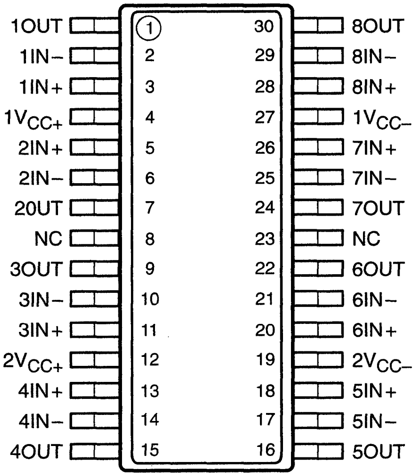
Figure 49. Single-Supply Twin-T Notch Filter

TLC274x2
LinCMOS™ PRECISION
OCTAL OPERATIONAL AMPLIFIER

SLOS137 – JULY 1994

- **Trimmed Offset Voltage**
  10 mV Max at T_A = 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages**
  3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

DB PACKAGE
(TOP VIEW)

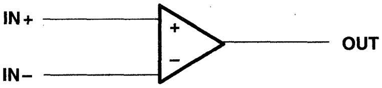


NC – No internal connection

description

The TLC274x2 octal operational amplifier incorporates low offset-voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices into a single package. This device uses Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

symbol (each amplifier)



The extremely high input impedance, low bias currents, and high slew rates make this a cost-effective device ideal for applications that have previously been reserved for BiFET and NFET products. These advantages, in combination with good common-mode rejection and supply-voltage rejection, make this device a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC274x2. The device also exhibits low-voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail. The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

AVAILABLE OPTION

T_A	V_{IO}max AT 25°C	PACKAGE
		SMALL OUTLINE (DB)†
0°C to 70°C	10 mV	TLC274x2DBLE

† The DB package is only available left-end taped and reeled.

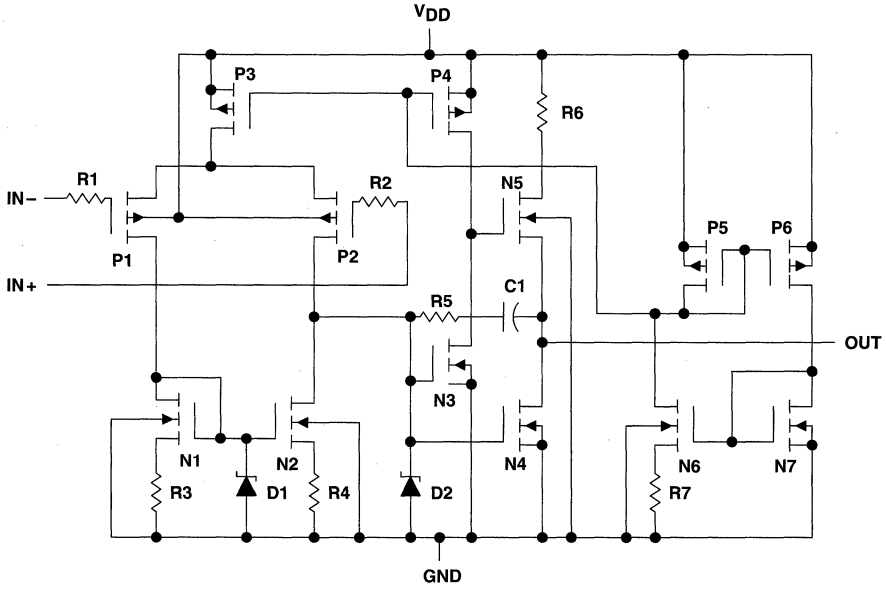
LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

The TLC274x2 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, exercise care in handling this device as exposure to ESD can result in the degradation of the device parametric performance.

The TLC274x2 is characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



COMPONENT COUNT	
Resistors	56
Transistors	80
Diodes	16
Capacitors	8

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	$V_{DD}\pm$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD}	45 mA
Total current out of GND	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	1024 mW	8.2 mW/°C	655 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		3	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	−0.2	3.5	V
	V_{DD} = 10 V	−0.2	8.5	
Operating free-air temperature, T_A		0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
			Full range			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
			70°C		7	300	
I_{IB}	Input bias current (see Note 4)	V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
			70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
			0°C	3	3.8		
			70°C	3	3.8		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
			0°C		0	50	
			70°C		0	50	
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
			0°C	4	27		
			70°C	4	20		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	65	80		dB
			0°C	60	84		
			70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
			0°C	60	94		
			70°C	60	96		
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		2.7	6.4	mA
			0°C		3.1	7.2	
			70°C		2.3	5.2	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 0.5 V,	V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)	V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
				0°C	7.8	8.5		
				70°C	7.8	8.4		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
				0°C	7.5	42		
				70°C	7.5	32		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$		25°C	65	85		dB
				0°C	60	88		
				70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (four amplifiers)	V_O = 5 V, No load	V_{IC} = 5 V,	25°C		3.8	8	mA
				0°C		4.5	8.8	
				70°C		3.2	6.8	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 Ω, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1,	25°C		46°		
				0°C		47°		
				70°C		44°		

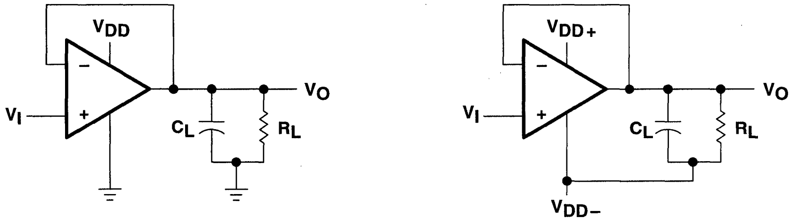
operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 Ω, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			$V_{I(PP)}$ = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				0°C		50°		
				70°C		46°		

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

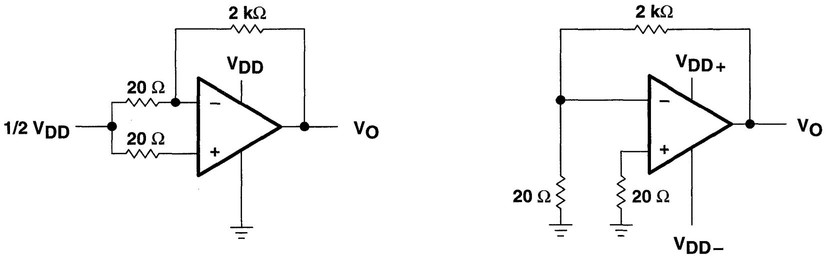
Because the TLC274x2 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

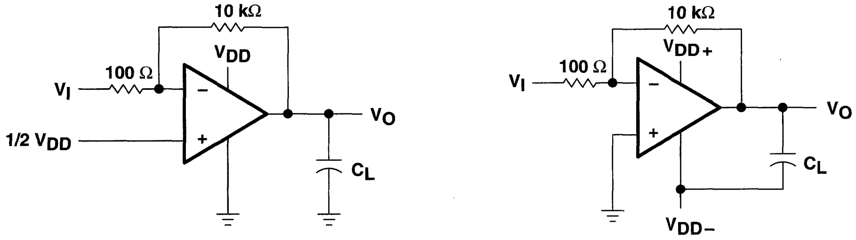
Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	4, 5 6 7
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	8, 9 10 11 12, 13
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	14 15 26, 27
I_{IB}	Input bias current	vs Free-air temperature	16
I_{IO}	Input offset current	vs Free-air temperature	16
V_{IC}	Common-mode input voltage	vs Supply voltage	17
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	18 19
SR	Slew rate	vs Supply voltage vs Free-air temperature	20 21
	Normalized slew rate	vs Free-air temperature	22
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	23
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	24 25
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	28 29 30
V_n	Equivalent input noise voltage	vs Frequency	31
	Phase shift	vs Frequency	26, 27

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

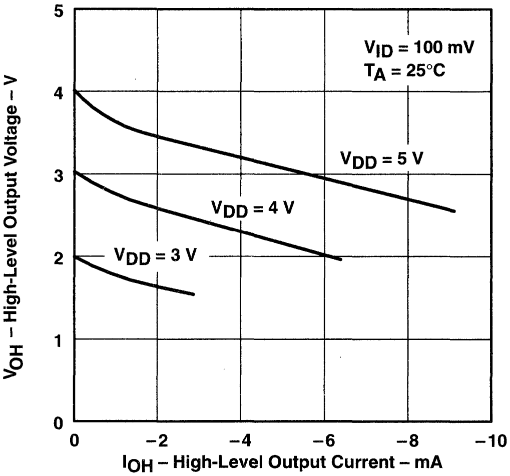


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

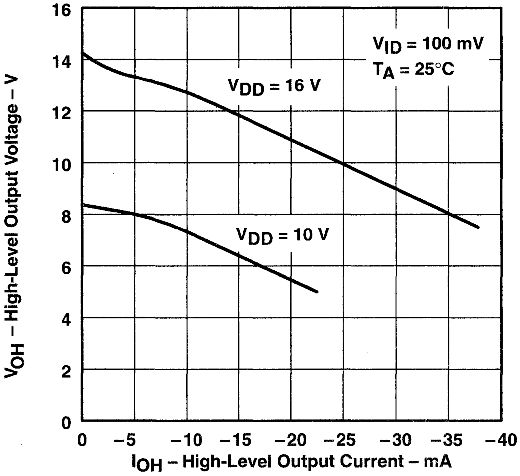


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

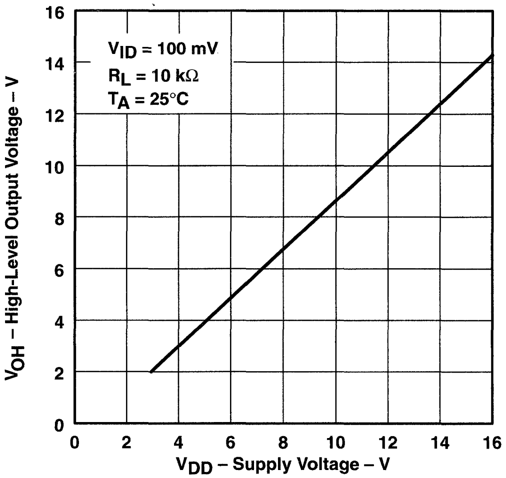


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

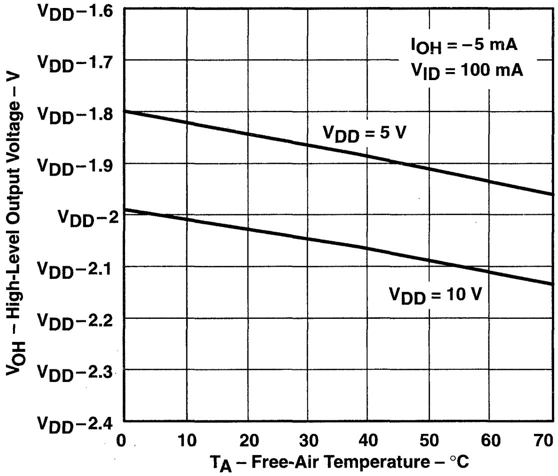


Figure 7

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

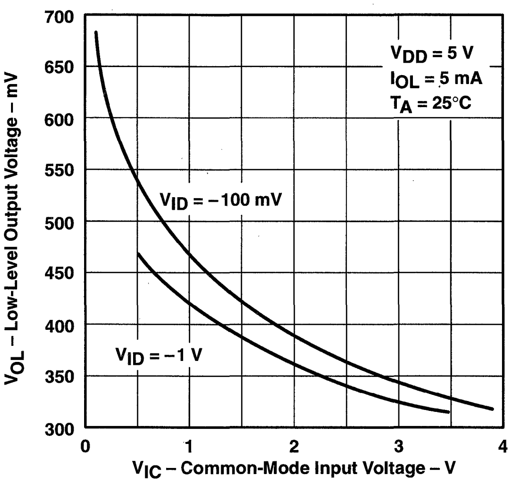


Figure 8

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

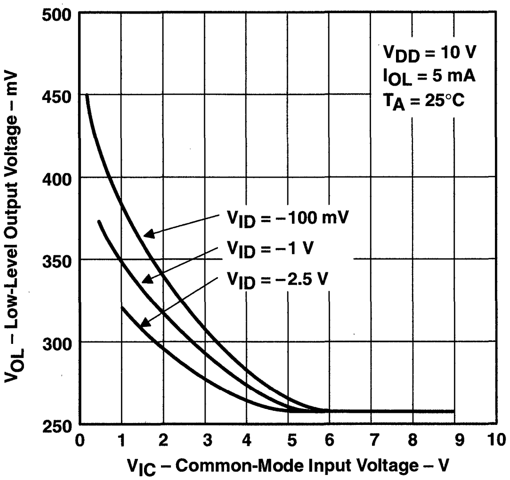


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

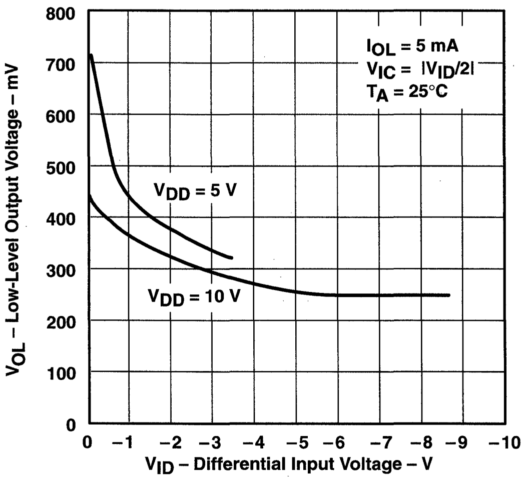


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

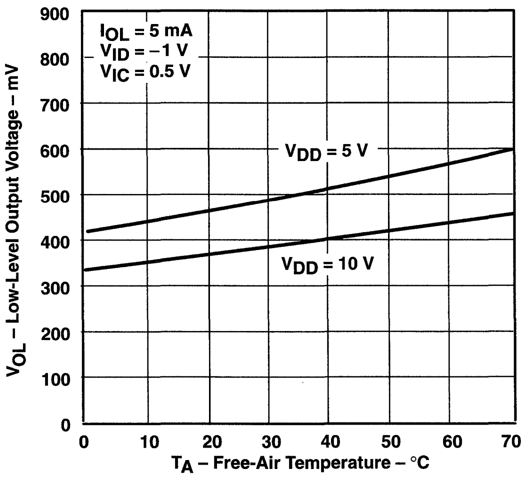


Figure 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

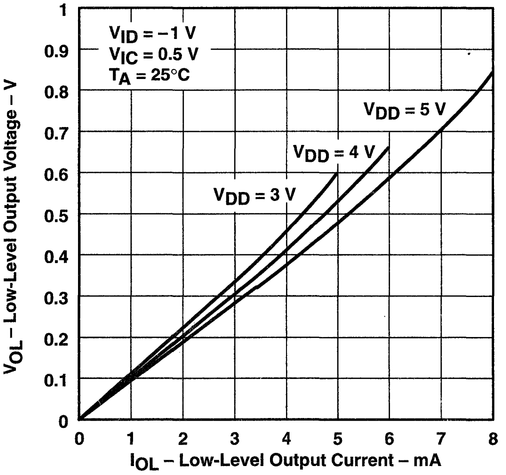


Figure 12

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

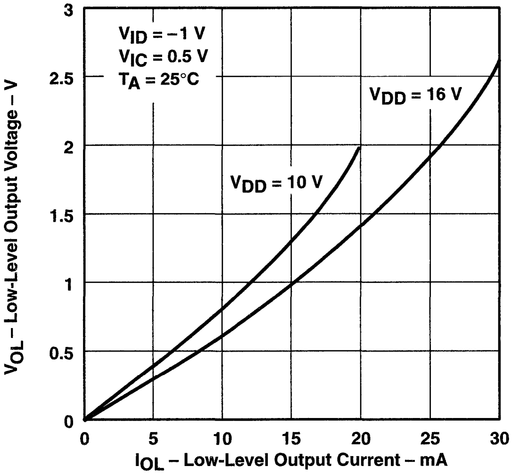


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

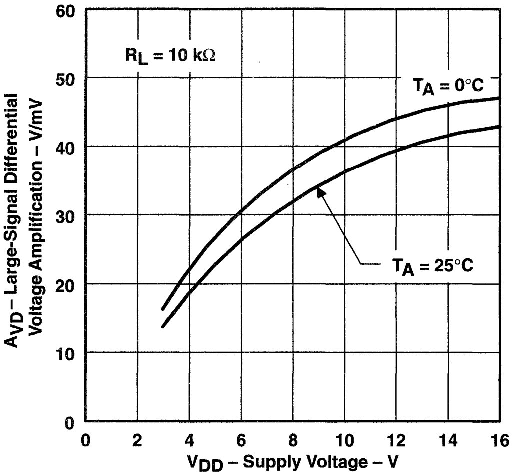


Figure 14

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

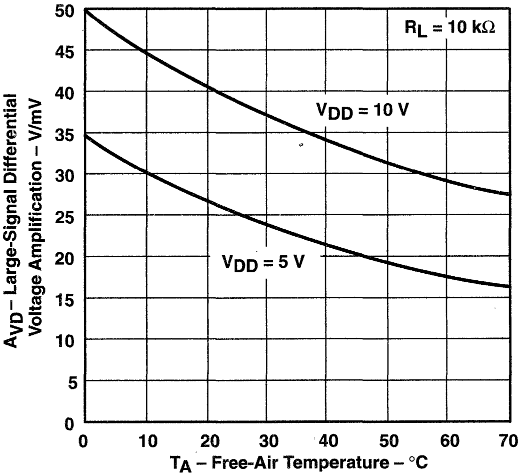
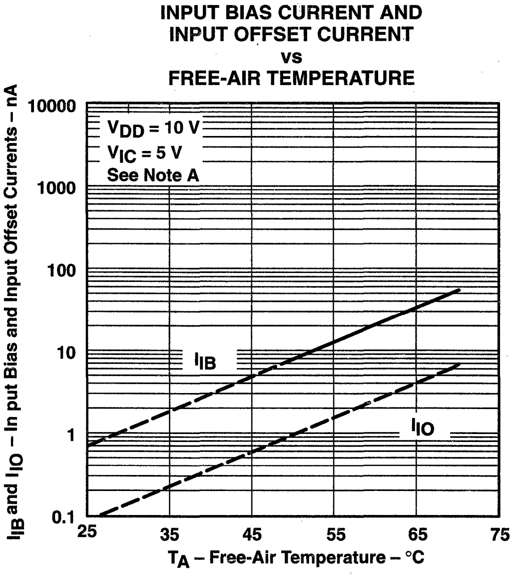


Figure 15

TYPICAL CHARACTERISTICS



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 16

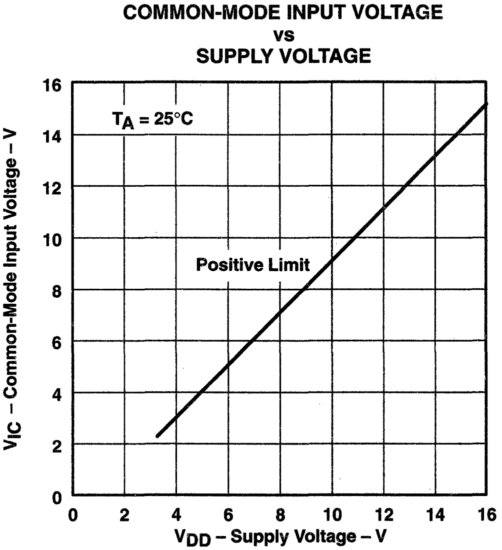


Figure 17

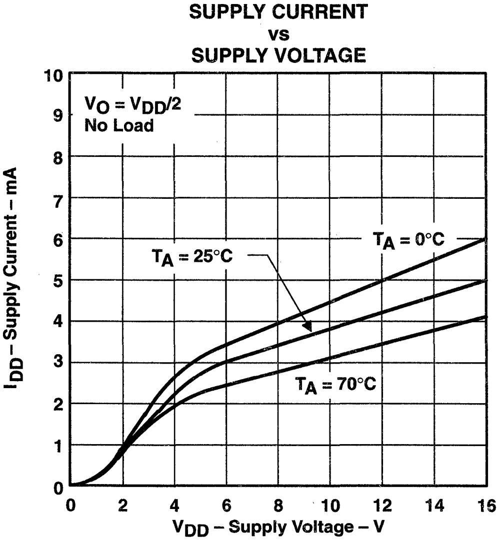


Figure 18

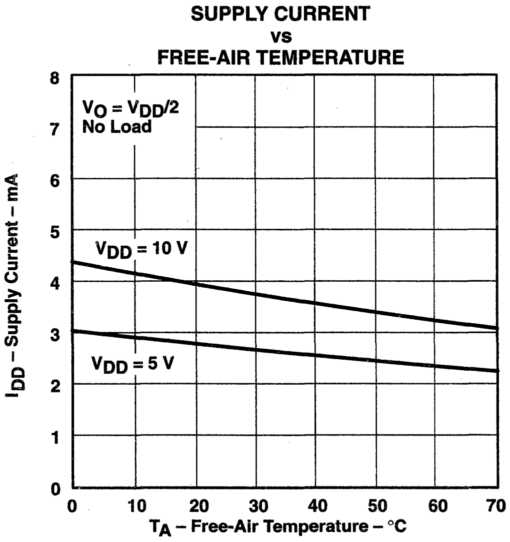


Figure 19

TYPICAL CHARACTERISTICS

SLEW RATE vs SUPPLY VOLTAGE

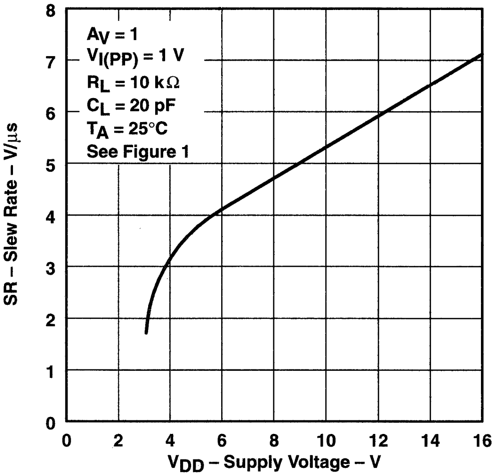


Figure 20

SLEW RATE vs FREE-AIR TEMPERATURE

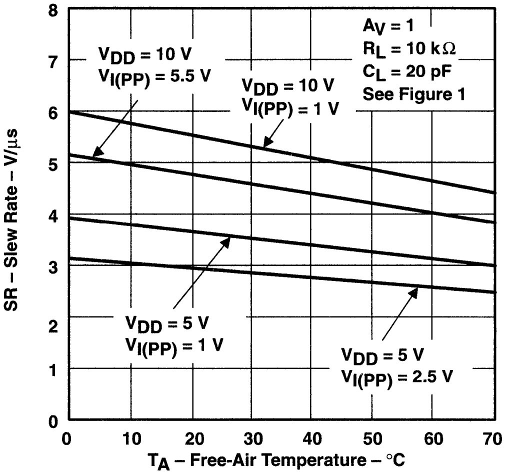


Figure 21

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

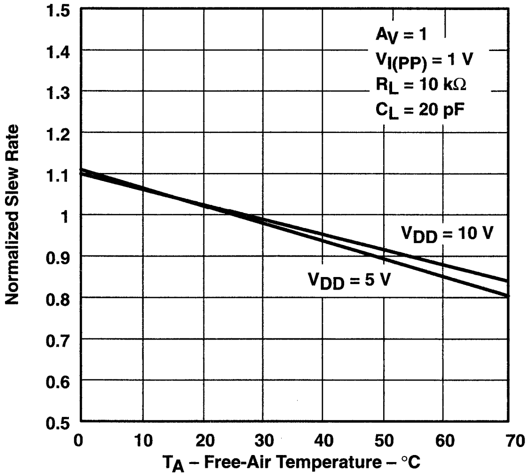


Figure 22

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

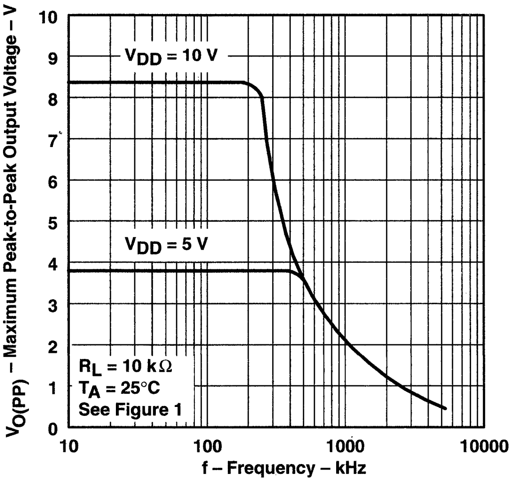


Figure 23

TYPICAL CHARACTERISTICS

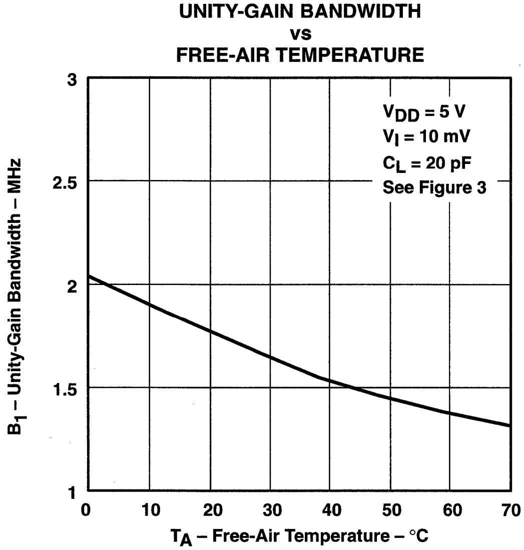


Figure 24

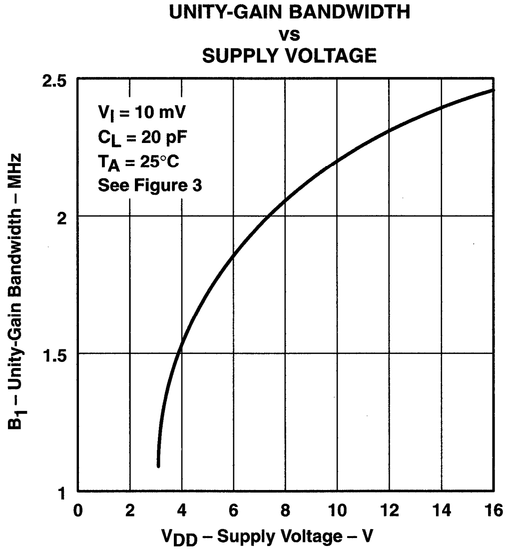


Figure 25

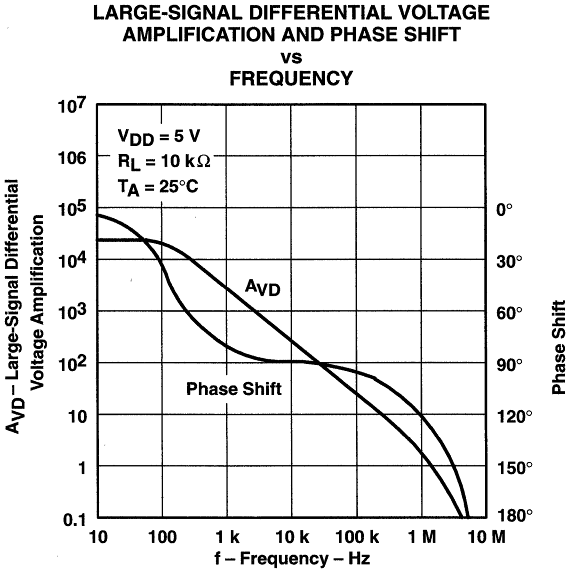


Figure 26

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

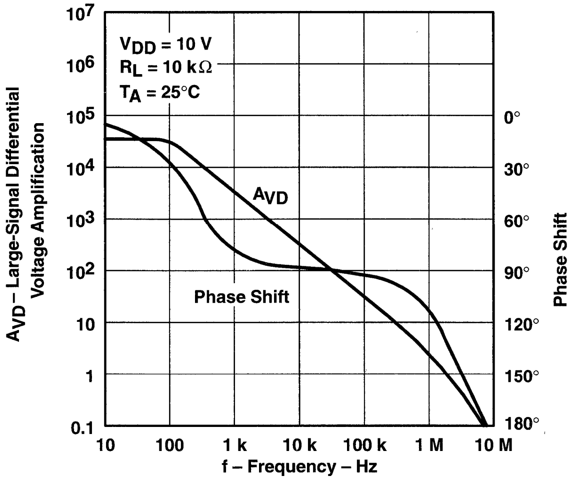


Figure 27

PHASE MARGIN vs SUPPLY VOLTAGE

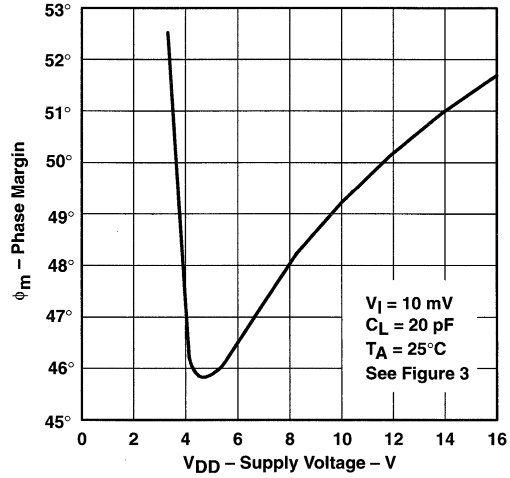


Figure 28

PHASE MARGIN vs FREE-AIR TEMPERATURE

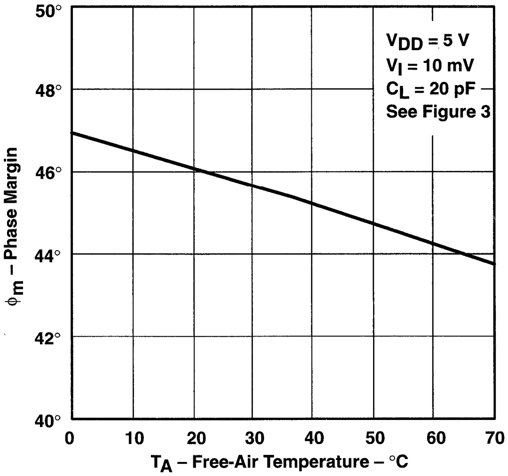


Figure 29

TYPICAL CHARACTERISTICS

PHASE MARGIN vs CAPACITIVE LOAD

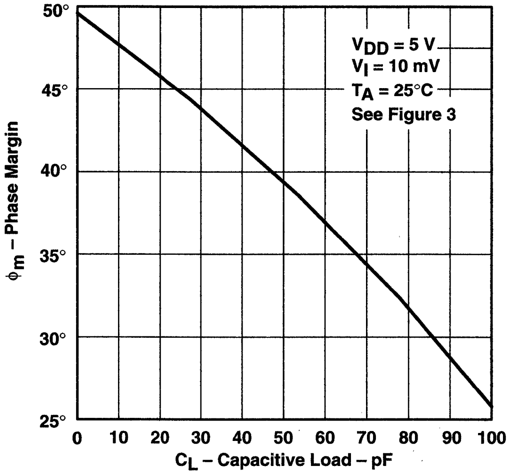


Figure 30

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

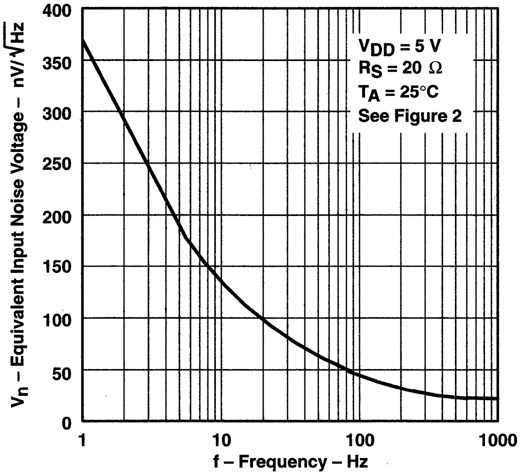


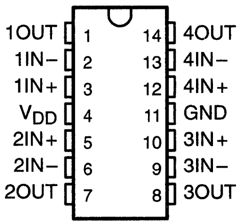
Figure 31

TLC27L4, TLC27L4A, TLC27L4B, TLC27L4Y, TLC27L9
LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

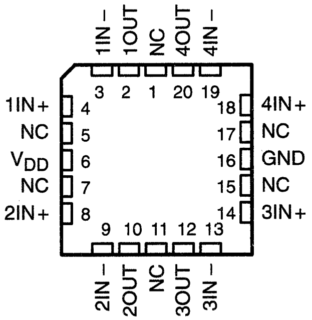
SLOS053C – OCTOBER 1987 – REVISED AUGUST 1994

- **Trimmed Offset Voltage:**
  TLC27L9 . . . 900 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  −55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Ultra-Low Power . . . Typically 195 μW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, J, N, OR PW PACKAGE
(TOP VIEW)

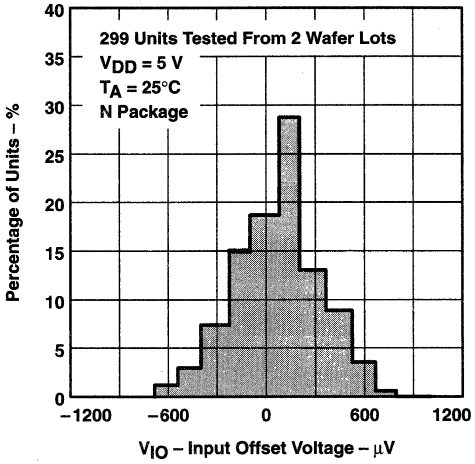


FK PACKAGE
(TOP VIEW)



NC – No internal connection

DISTRIBUTION OF TLC27L9
INPUT OFFSET VOLTAGE



description

The TLC27L4 and TLC27L9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

These devices use Texas instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low-power consumption make these cost-effective devices ideal for high-gain, low- frequency, low-power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L4 (10 mV) to the high-precision TLC27L9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L4 and TLC27L9. The devices also exhibit low voltage single-supply operation and ultra-low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC27L4 and TLC27L9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.

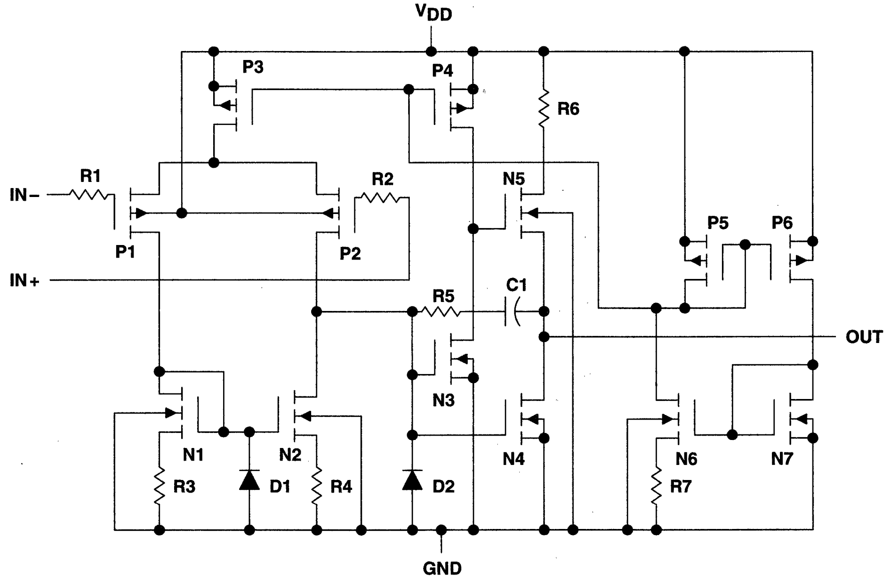
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation from –55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	900 µV	TLC27L9CD	—	—	TLC27L9CN	—	—
	2 mV	TLC27L4BCD	—	—	TLC27L4BCN	—	—
	5 mV	TLC27L4ACD	—	—	TLC27L4ACN	—	—
	10 mV	TLC27L4CD	—	—	TLC27L4CN	TLC27L4CPW	TLC27L4Y
–40°C to 85°C	900 µV	TLC27L9ID	—	—	TLC27L9IN	—	—
	2 mV	TLC27L4BID	—	—	TLC27L4BIN	—	—
	5 mV	TLC27L4AID	—	—	TLC27L4AIN	—	—
	10 mV	TLC27L4ID	—	—	TLC27L4IN	—	—
–55°C to 125°C	900 µV	TLC27L9MD	TLC27L9MFK	TLC27L9MJ	TLC27L9MN	—	—
	10 mV	TLC27L4MD	TLC27L4MFK	TLC27L4MJ	TLC27L4MN	—	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L9CDR).

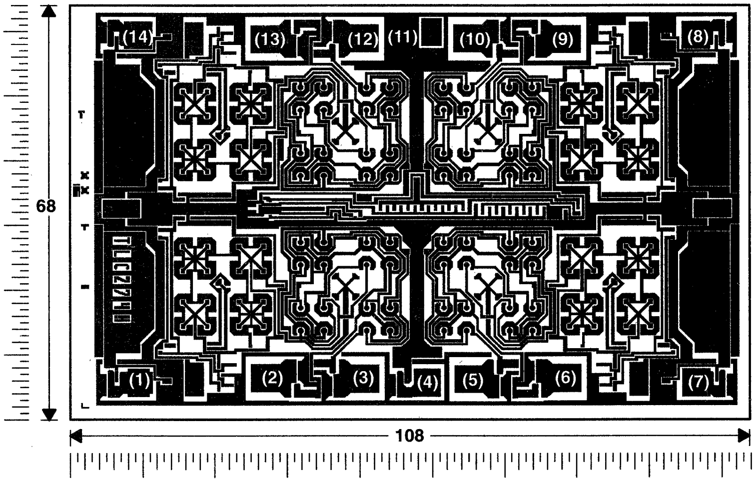
equivalent schematic (each amplifier)

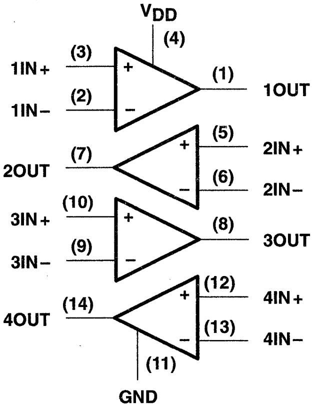


TLC27L4Y chip information

These chips, when properly assembled, display characteristics similar to the TLC27L4C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD}	45 mA
Total current out of GND	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	—
PW	700 mW	5.6 mW/°C	448 mW	—	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	−0.2	3.5	−0.2	3.5	0	3.5	V
	V_{DD} = 10 V	−0.2	8.5	−0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L4C TLC27L4AC TLC27L4BC TLC27L9C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		240	2000	µV
					Full range			3000	
		TLC27L9C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		200	900	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					0°C	3	4.1		
					70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 2.5 V to 2 V,	R_L = 1 MΩ	25°C	50	520		V/mV
					0°C	50	680		
					70°C	50	380		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min		25°C	65	94		dB
					0°C	60	95		
					70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		40	68	µA
					0°C		48	84	
					70°C		31	56	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27L4C TLC27L4AC TLC27L4BC TLC27L9C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L4AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L4BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		260	2000	µV
				Full range			3000	
		TLC27L9C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				0°C	7.8	8.9		
				70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	870		V/mV
				0°C	50	1020		
				70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	97		dB
				0°C	60	97		
				70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		57	92	µA
				0°C		72	132	
				70°C		44	80	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L4I TLC27L4AI TLC27L4BI TLC27L9I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27L4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			7	
		TLC27L4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		240	2000	µV
					Full range			3500	
		TLC27L9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		200	900	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					−40°C	3	4.1		
					85°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	480		V/mV
					−40°C	50	900		
					85°C	50	330		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$		25°C	65	94		dB
					−40°C	60	95		
					85°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		39	68	µA
					−40°C		62	108	
					85°C		29	52	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27L4I TLC27L4AI TLC27L4BI TLC27L9I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L4AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L4BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		260	2000	µV
				Full range			3500	
		TLC27L9I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} =.5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				−40°C	7.8	8.9		
				85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				−40°C	50	1550		
				85°C	50	585		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	97		dB
				−40°C	60	97		
				85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		57	92	µA
				−40°C		98	172	
				85°C		40	72	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27L4M TLC27L9M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L9M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				−55°C	3	4.1		
				125°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				−55°C	25	950		
				125°C	25	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		dB
				−55°C	60	95		
				125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−55°C	60	97		
				125°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		39	68	µA
				−55°C		69	120	
				125°C		27	48	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27L4M TLC27L9M			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		210	1200	μV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−55°C	7.8	8.8		
					125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	800		V/mV
					−55°C	25	1750		
					125°C	25	380		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min		25°C	65	97		dB
					−55°C	60	97		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		57	92	μA
					−55°C		111	192	
					125°C		35	60	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and Input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC27L4Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ		1.1	10	mV
α_{VIO}	Average temperature coefficient of input offset voltage	T_A = 25°C to 70°C			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 2.5 V,	V_{IC} = 2.5 V		0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 2.5 V,	V_{IC} = 2.5 V		0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 1 MΩ	3.2	4.1		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V to 2 V,	R_L = 1 MΩ	50	520		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V,	V_O = 1.4 V	70	97		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, No load	V_{IC} = 2.5 V,		40	68	μA

electrical characteristics at specified free-air temperature, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC27L4Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ		1.1	10	mV
α_{VIO}	Average temperature coefficient of input offset voltage	T_A = 25°C to 70°C			1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 5 V,	V_{IC} = 5 V		0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 5 V,	V_{IC} = 5 V		0.7		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 9	−0.3 to 9.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 1 MΩ	8	8.9		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 6 V,	R_L = 1 MΩ	50	870		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$		65	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V,	V_O = 1.4 V	70	97		dB
I_{DD}	Supply current (four amplifiers)	V_O = 5 V, No load	V_{IC} = 5 V,		57	92	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L4C TLC27L4AC TLC27L4BC TLC27L9C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/µs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHZ, See Figure 2	R_S = 20 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L4C TLC27L4AC TLC27L4BC TLC27L9C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/µs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L4I TLC27L4AI TLC27L4BI TLC27L9I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 HZ, See Figure 2	R_S = 20 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−40°C		38°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L4I TLC27L4AI TLC27L4BI TLC27L9I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 HZ, See Figure 2	R_S = 20 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−40°C		42°		
				85°C		32°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L4M TLC27L9M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−55°C		39°		
				125°C		25°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L4M TLC27L9M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−55°C		43°		
				125°C		29°		

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC27L4Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V		0.03		V/μs
			V_{IPP} = 2.5 V		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1		5		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,		85		kHz
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3		34°		

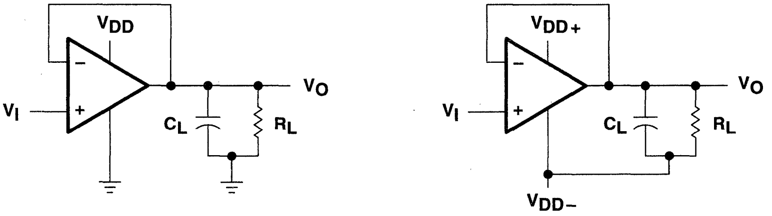
operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC27L4Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V		0.05		V/μs
			V_{IPP} = 5.5 V		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,		70		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1		1		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,		110		kHz
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3		38°		

PARAMETER MEASUREMENT INFORMATION

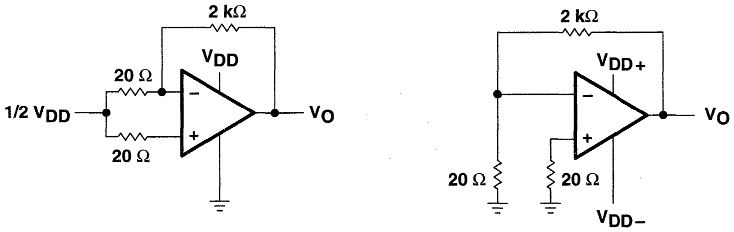
single-supply versus split-supply test circuits

Because the TLC27L4 and TLC27L9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



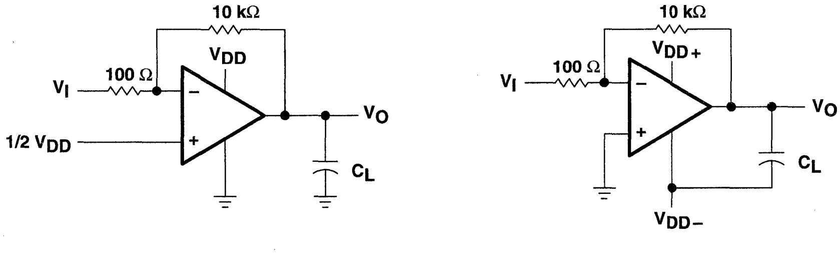
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L4 and TLC27L9 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

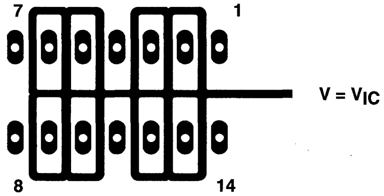


Figure 4. Isolation Metal Around Device Inputs (J and N packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

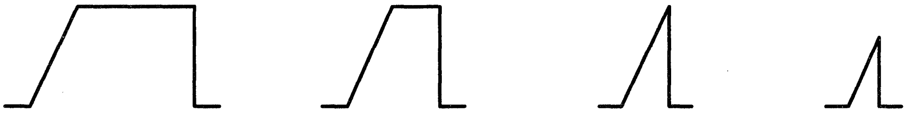
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 Hz (b) B_{OM} > f > 100 Hz (c) f = B_{OM} (d) f > B_{OM}

Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
α_{VIO}	Temperature coefficient	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A_{VD}	Differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I_{IB}/I_{IO}	Input bias and input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitive loads	34 35 36
V_n	Equivalent input noise voltage	vs Frequency	37
ϕ	Phase shift	vs Frequency	32, 33

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L4 INPUT OFFSET VOLTAGE

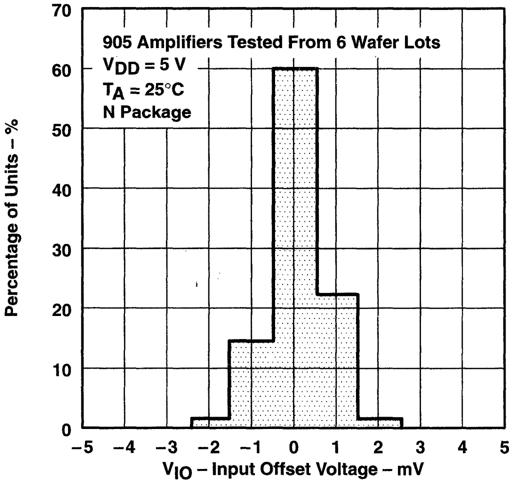


Figure 6

DISTRIBUTION OF TLC27L4 INPUT OFFSET VOLTAGE

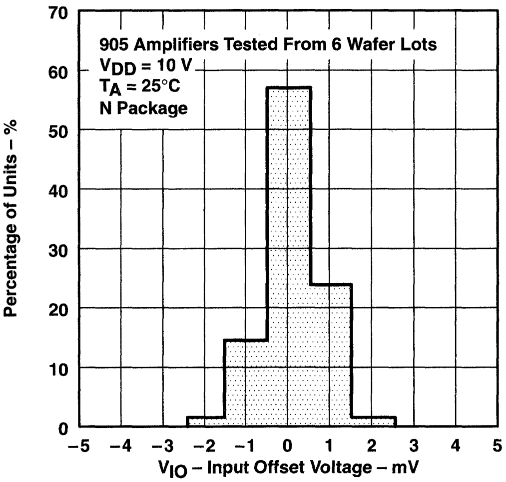


Figure 7

DISTRIBUTION OF TLC27L4 AND TLC27L9 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

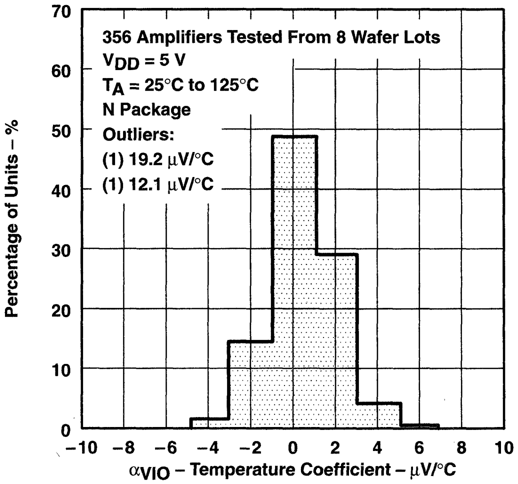


Figure 8

DISTRIBUTION OF TLC27L4 AND TLC27L9 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

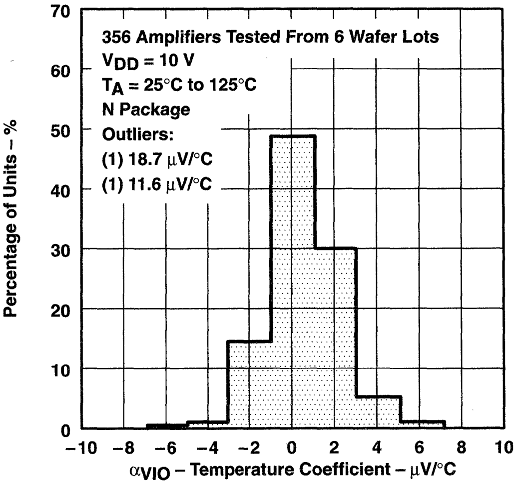
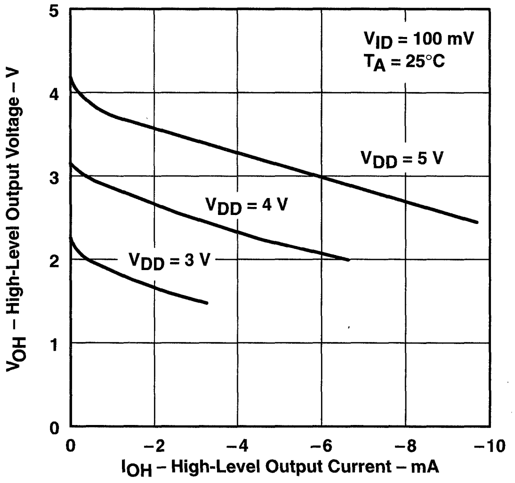


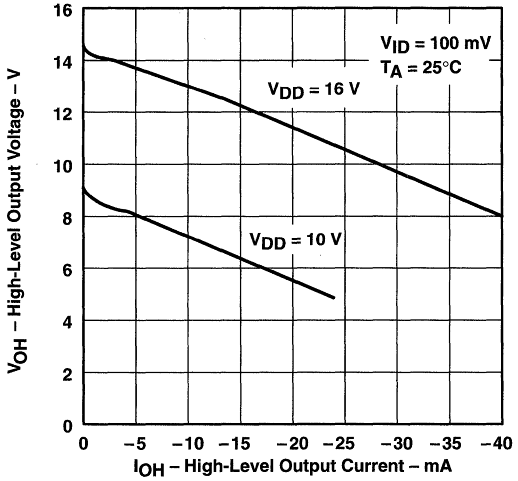
Figure 9

TYPICAL CHARACTERISTICS†



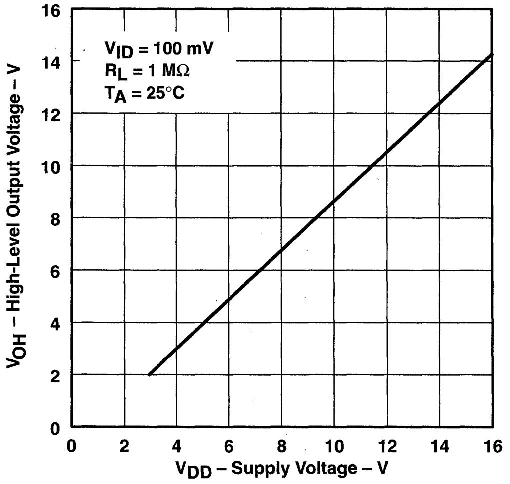
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 10



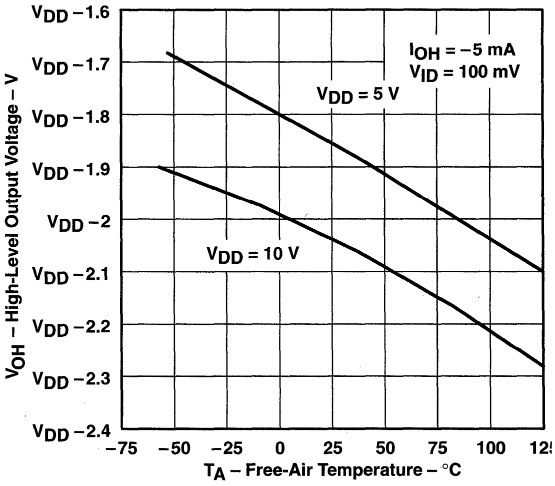
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 11



HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

Figure 12



HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

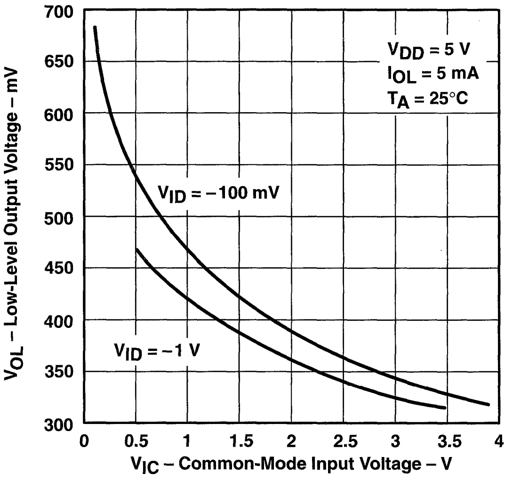
LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 14

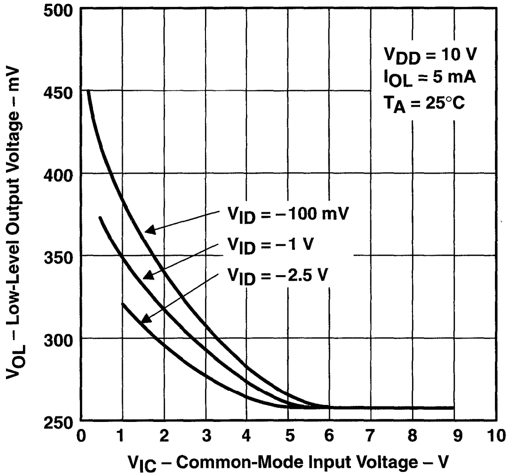
LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 15

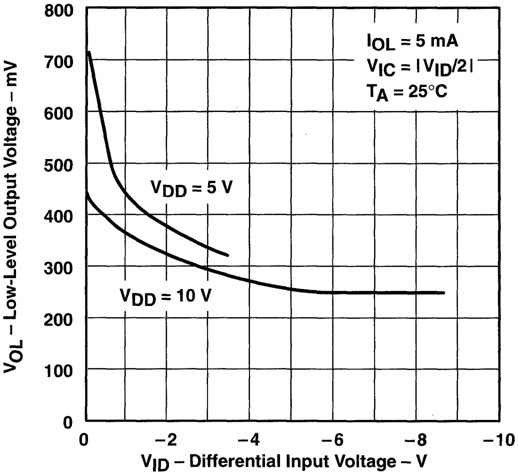
LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 16

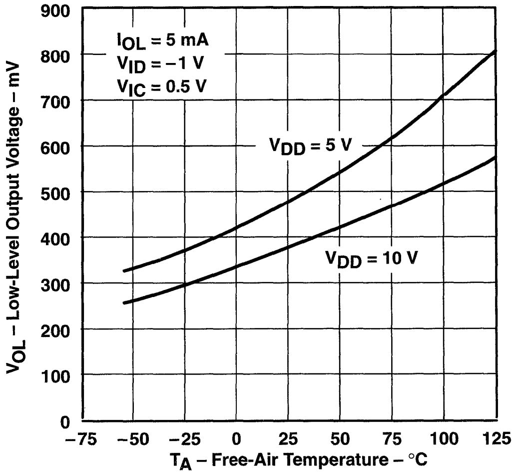
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

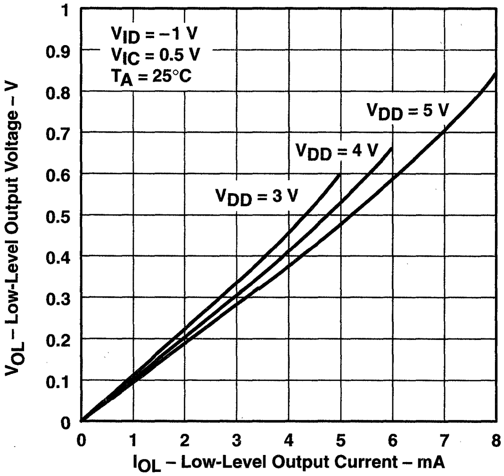

Figure 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

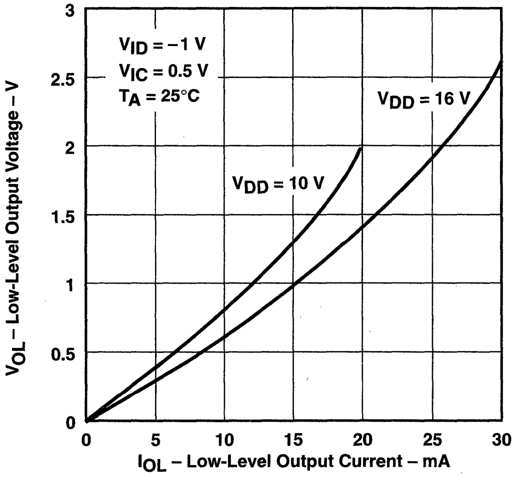

Figure 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

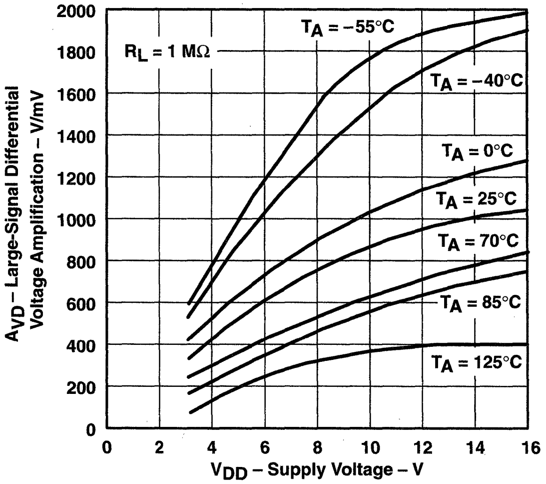

Figure 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

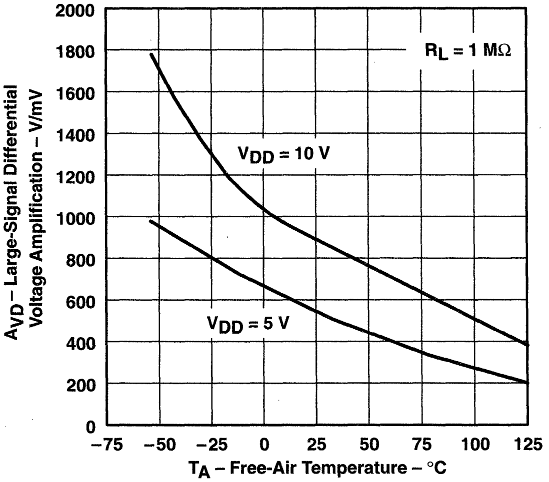

Figure 21

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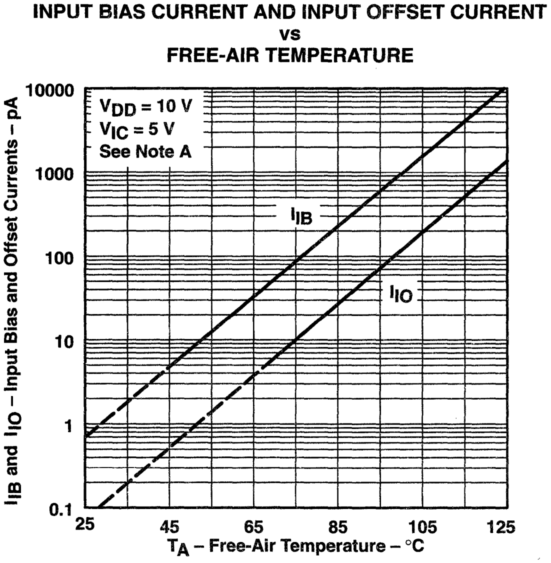
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

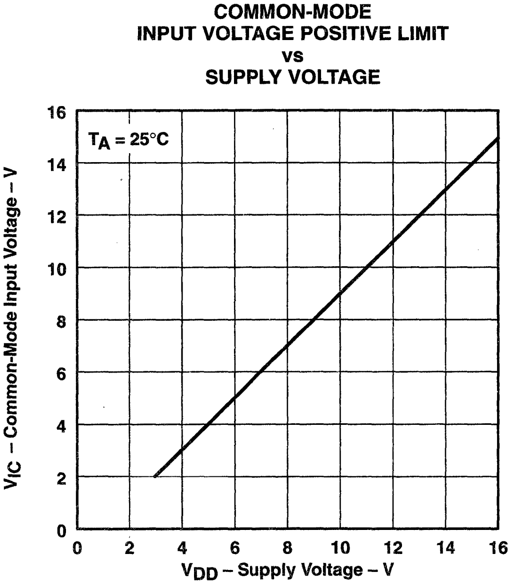


Figure 23

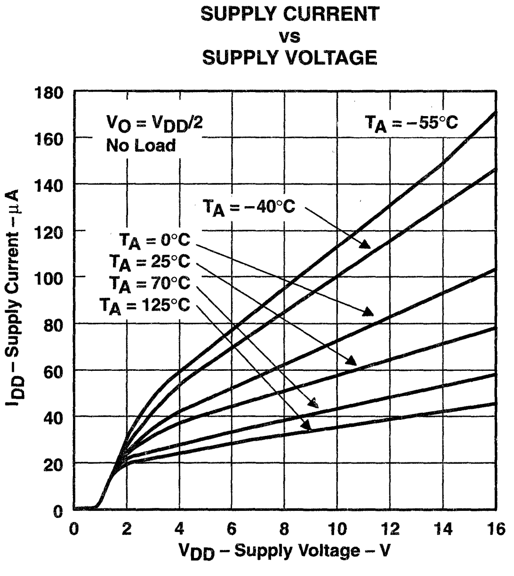


Figure 24

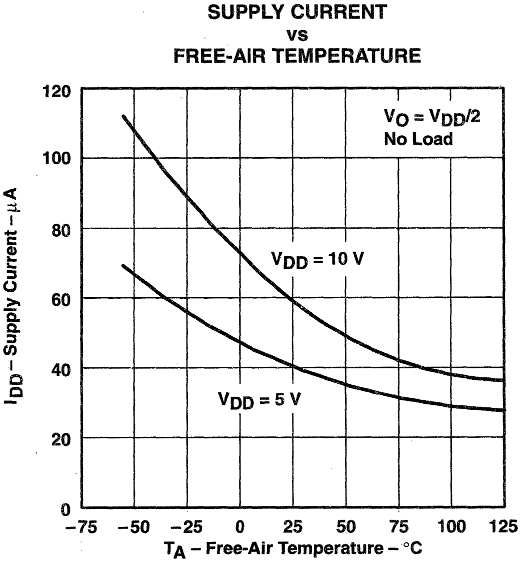


Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

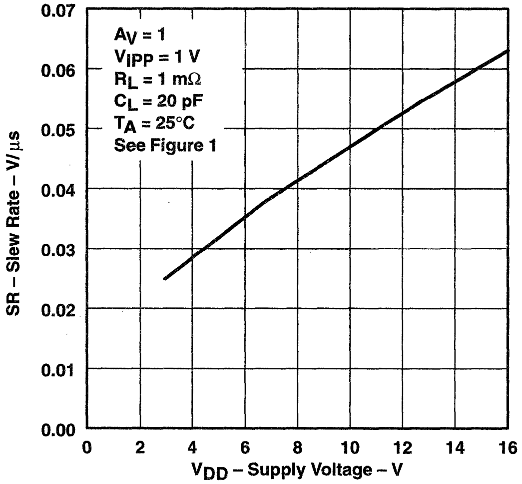

Figure 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

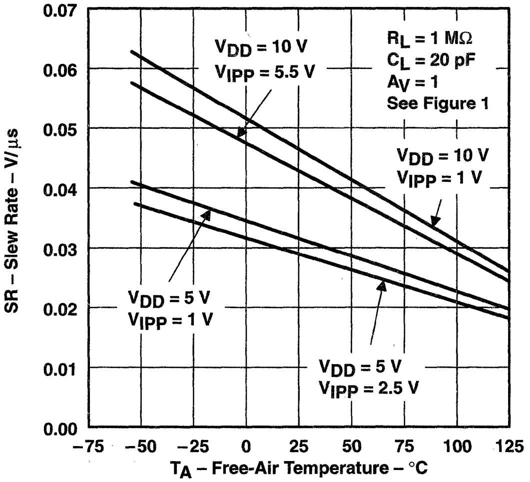

Figure 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

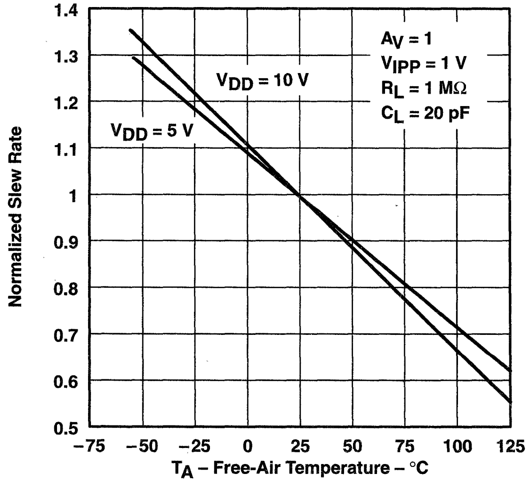

Figure 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

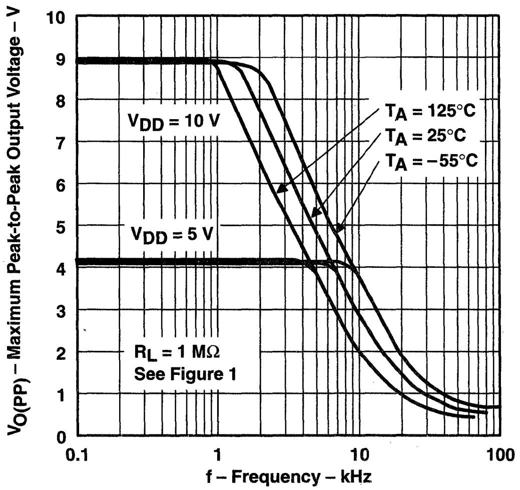

Figure 29

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

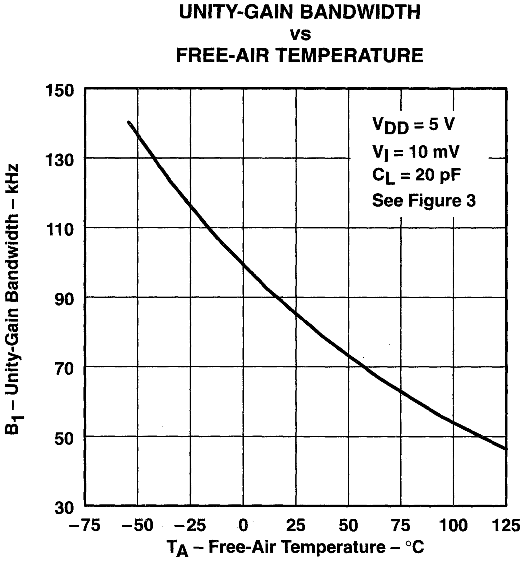

Figure 30

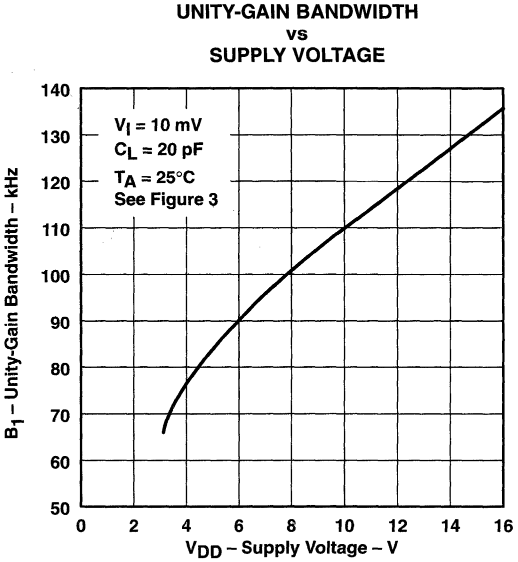

Figure 31

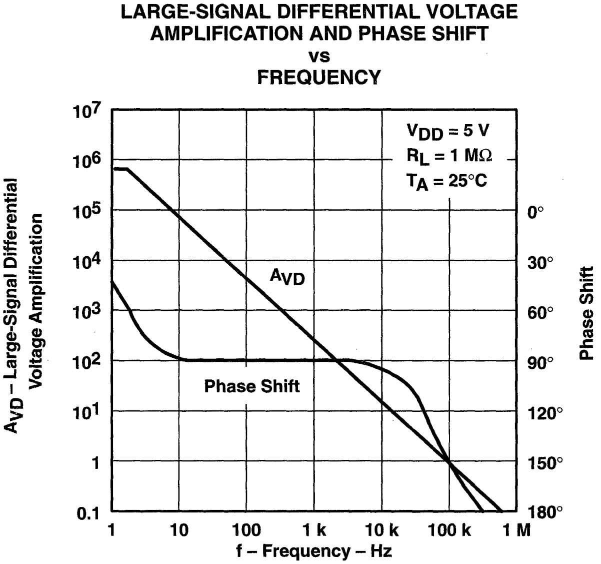

Figure 32

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

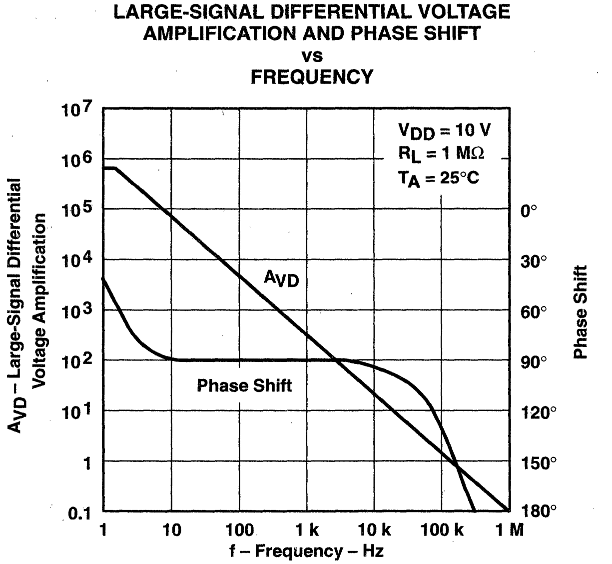

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

Figure 33

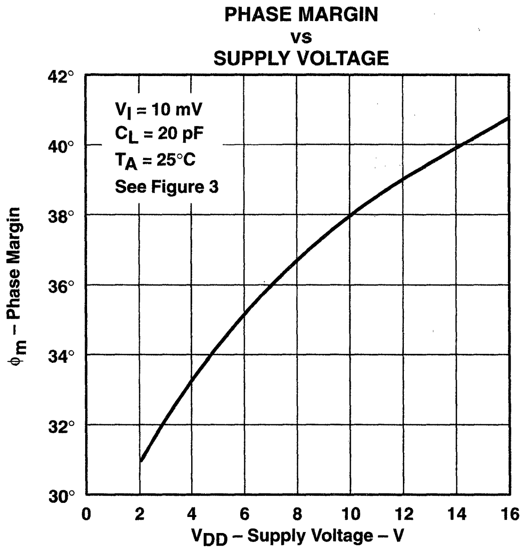

PHASE MARGIN
vs
SUPPLY VOLTAGE

Figure 34

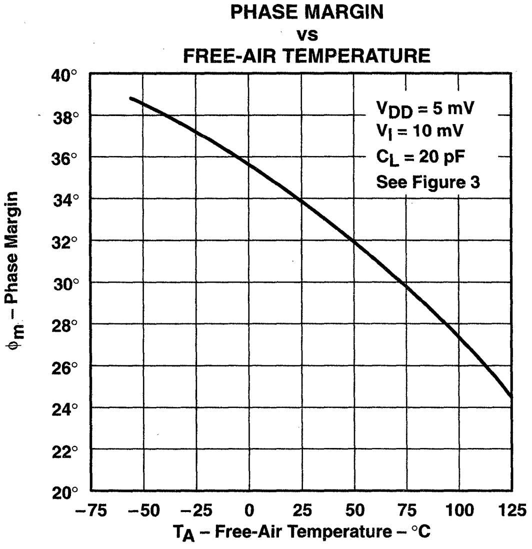

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

Figure 35

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
CAPACITIVE LOAD

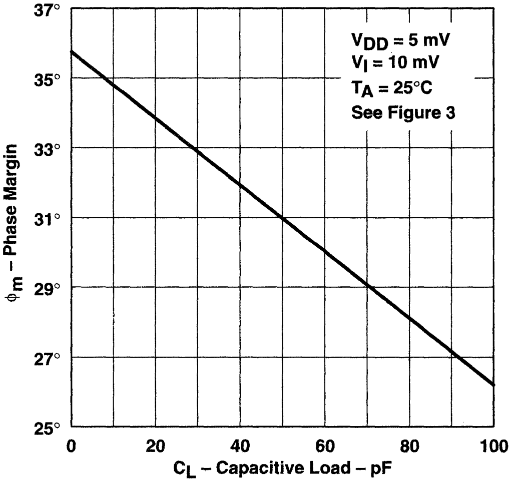


Figure 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

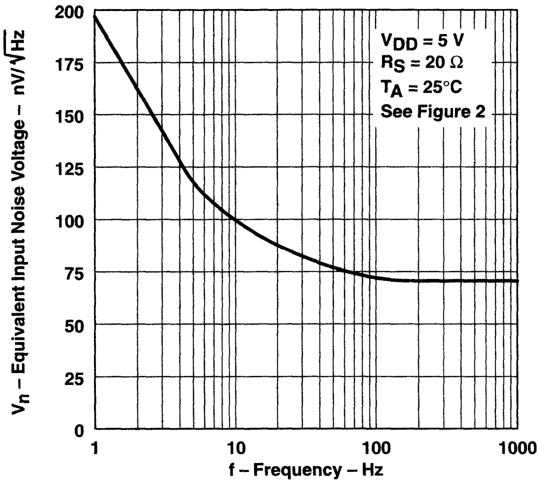


Figure 37

APPLICATION INFORMATION

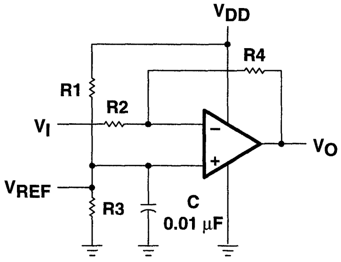
single-supply operation

While the TLC27L4 and TLC27L9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L4 and TLC27L9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L4 and TLC27L9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



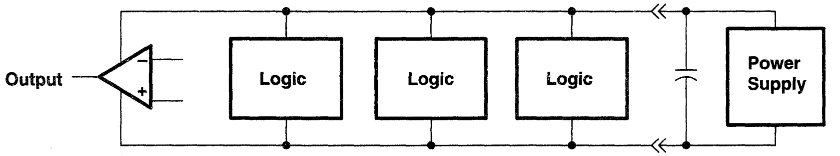
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = (V_{REF} - V_I) \frac{R4}{R2} + V_{REF}$$

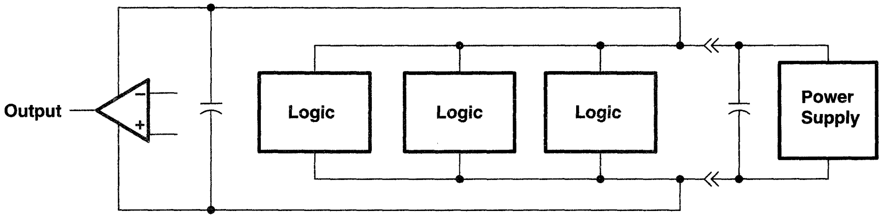
Figure 38. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common Versus Separate Supply Rails

input characteristics

The TLC27L4 and TLC27L9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L4 and TLC27L9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L4 and TLC27L9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

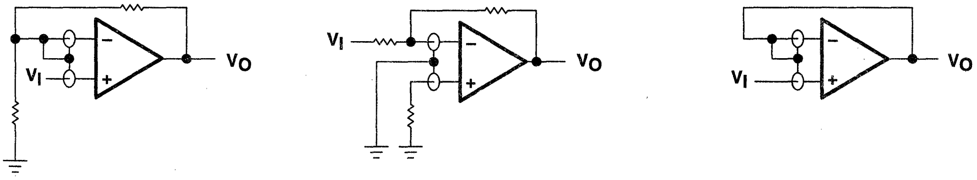
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L4 and TLC27L9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

APPLICATION INFORMATION

noise performance (continued)



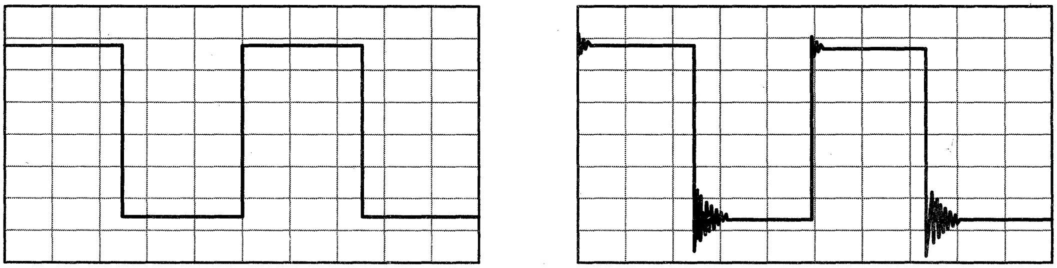
(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 40. Guard-Ring Schemes

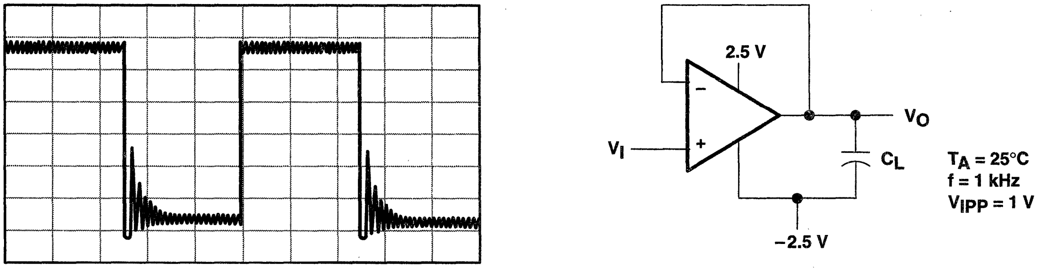
output characteristics

The output stage of the TLC27L4 and TLC27L9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27L4 and TLC27L9 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD



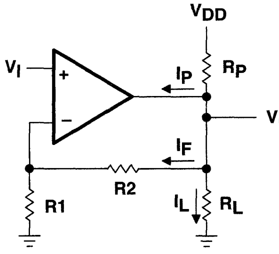
(c) C_L = 310 pF, R_L = NO LOAD (d) TEST CIRCUIT

Figure 41. Effect of Capacitive Loads and Test Circuit

APPLICATION INFORMATION

output characteristics (continued)

Although the TLC27L4 and TLC27L9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (Rb) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 µA)

Figure 42. Resistive Pullup to Increase V_{OH}

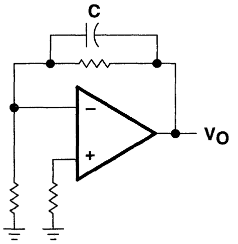


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27L4 and TLC27L9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L4 and TLC27L9 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

APPLICATION INFORMATION

latch-up (continued)

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

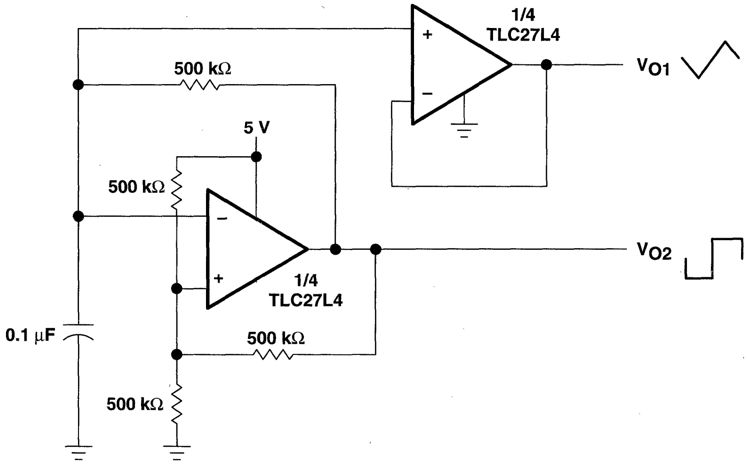
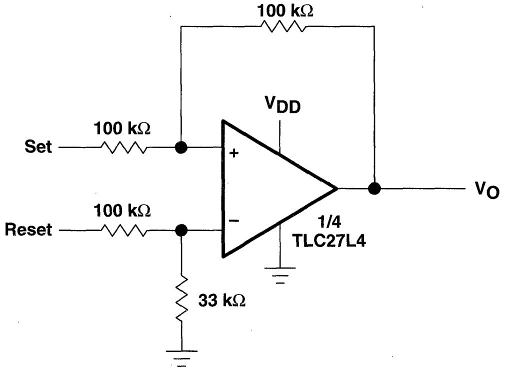


Figure 44. Multivibrator

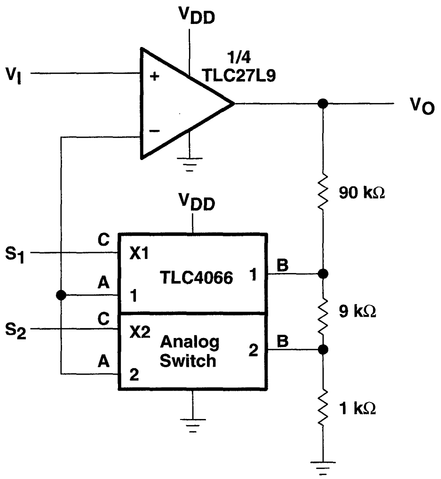


NOTE: V_{DD} = 5 V to 16 V

Figure 45. Set/Reset Flip-Flop

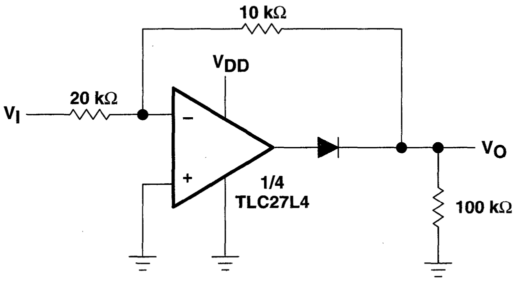
APPLICATION INFORMATION

SELECT	S_1	S_2
A_V	10	100



NOTE: V_{DD} = 5 V to 12 V

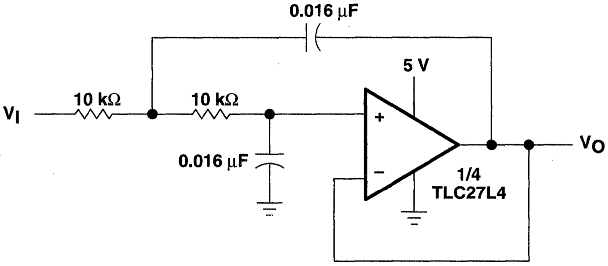
Figure 46. Amplifier With Digital Gain Selection



NOTE: V_{DD} = 5 V to 16 V

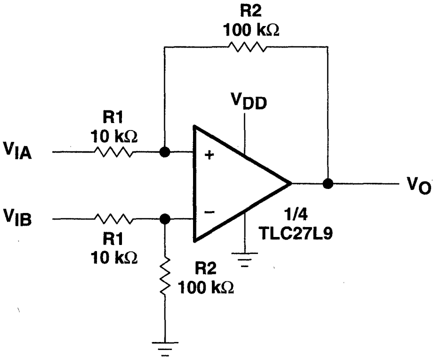
Figure 47. Full-Wave Rectifier

APPLICATION INFORMATION



NOTE: Normalized to $F_C = 1$ kHz and $R_L = 10$ kΩ

Figure 48. Two-Pole Low-Pass Butterworth Filter



NOTE: $V_{DD} = 5$ V to 16 V

$$V_O = \frac{R2}{R1}\left(V_{IB} - V_{IA}\right)$$

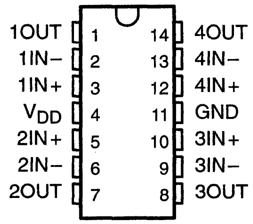
Figure 49. Difference Amplifier

TLC27M4, TLC27M4A, TLC27M4B, TLC27M4Y, TLC27M9
LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

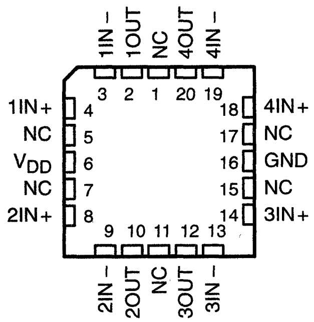
SLOS093B – OCTOBER 1987 – REVISED AUGUST 1994

- **Trimmed Offset Voltage:**
  TLC27M9 . . . 900 μV Max at T_A = 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  - **0°C to 70°C . . . 3 V to 16 V**
  - **–40°C to 85°C . . . 4 V to 16 V**
  - **–55°C to 125°C . . . 4 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Low Noise . . . Typically 32 nV/√Hz at f = 1 kHz**
- **Low Power . . . Typically 2.1 mW at T_A = 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, J, N, OR PW PACKAGE
(TOP VIEW)

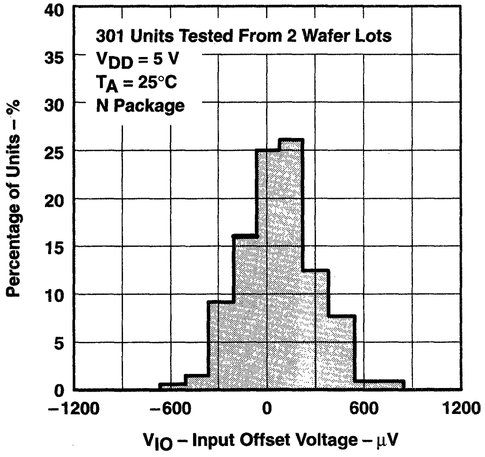


FK PACKAGE
(TOP VIEW)



NC – No internal connection

DISTRIBUTION OF TLC27M9
INPUT OFFSET VOLTAGE



description

The TLC27M4 and TLC27M9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, make these cost-effective devices ideal for applications that have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption.

Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M4 (10 mV) to the high-precision TLC27M9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M4 and TLC27M9. The devices also exhibit low voltage single-supply operation, and low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC27M4 and TLC27M9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

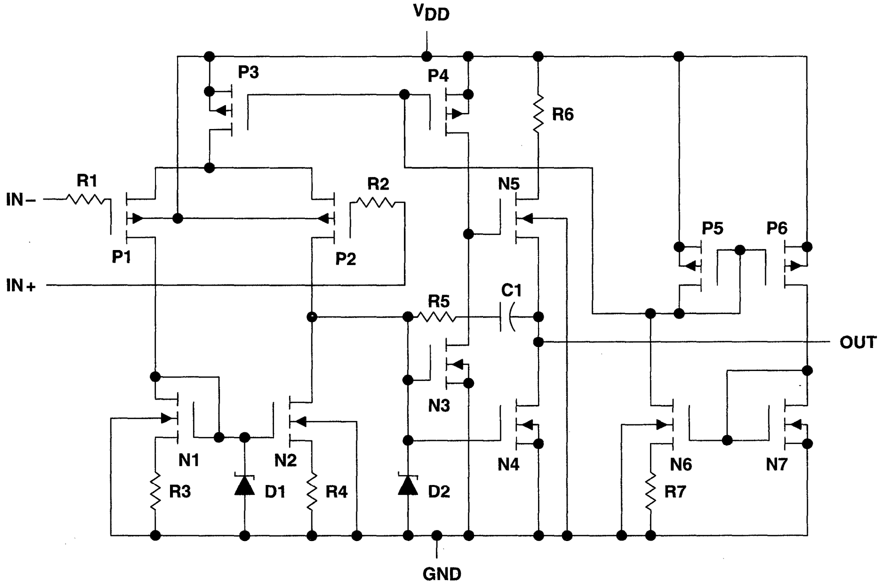
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	900 µV	TLC27M9CD	—	—	TLC27M9CN	—	—
	2 mV	TLC27M4BCD	—	—	TLC27M4BCN	—	—
	5 mV	TLC27M4ACD	—	—	TLC27M4ACN	—	—
	10 mV	TLC27M4CD	—	—	TLC27M4CN	TLC27M4CPW	TLC27M4Y
–40°C to 85°C	900 µV	TLC27M9ID	—	—	TLC27M9IN	—	—
	2 mV	TLC27M4BID	—	—	TLC27M4BIN	—	—
	5 mV	TLC27M4AID	—	—	TLC27M4AIN	—	—
	10 mV	TLC27M4ID	—	—	TLC27M4IN	—	—
–55°C to 125°C	900 µV	TLC27M9MD	TLC27M9MFK	TLC27M9MJ	TLC27M9MN	—	—
	10 mV	TLC27M4MD	TLC27M4MFK	TLC27M4MJ	TLC27M4MN	—	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC279CDR).

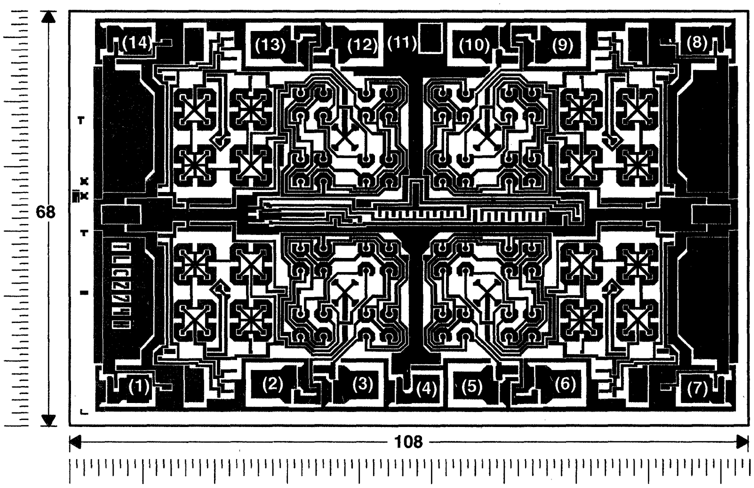
equivalent schematic (each amplifier)

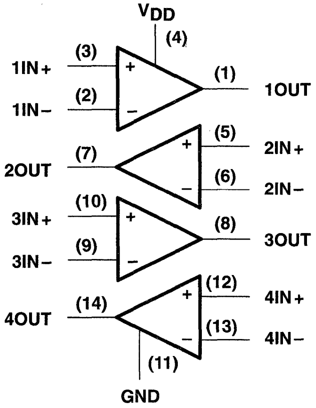


TLC27M4Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC27M4C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD}	45 mA
Total current out of GND	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	—
PW	700 mW	5.6 mW/°C	448 mW	—	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	−0.2	3.5	−0.2	3.5	0	3.5	V
	V_{DD} = 10 V	−0.2	8.5	−0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27M4C TLC27M4AC TLC27M4BC TLC27M9C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC274BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		250	2000	µV
					Full range			3000	
		TLC279C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		210	900	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					0°C	3	3.9		
					70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					0°C	15	200		
					70°C	15	140		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	91		dB
					0°C	60	91		
					70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		420	1120	µA
					0°C		500	1280	
					70°C		340	880	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27M4C TLC27M4AC TLC27M4BC TLC27M9C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M4AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27M4BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		260	2000	µV
				Full range			3000	
		TLC27M9C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				0°C	7.8	8.7		
				70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				0°C	15	320		
				70°C	15	230		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	94		dB
				0°C	60	94		
				70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		
				70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		570	1200	µA
				0°C		690	1600	
				70°C		440	1120	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC27M4I TLC27M4AI TLC27M4BI TLC27M9I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27M4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27M4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		250	2000	µV
					Full range			3000	
		TLC27M9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		210	900	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					−40°C	3	3.9		
					85°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					−40°C	15	270		
					85°C	15	130		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$		25°C	65	91		dB
					−40°C	60	90		
					85°C	60	90		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−40°C	60	91		
					85°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		420	1120	µA
					−40°C		630	1600	
					85°C		320	800	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27M4I TLC27M4AI TLC27M4BI TLC27M9I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M4AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M4BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		260	2000	µV
				Full range			3500	
		TLC27M9I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				−40°C	7.8	8.7		
				85°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				−40°C	15	390		
				85°C	15	220		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	94		dB
				−40°C	60	93		
				85°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−40°C	60	91		
				85°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		570	1200	µA
				−40°C		900	1800	
				85°C		410	1040	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC27M4M TLC27M9M			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	TLC27M4M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
			Full range			12	
	TLC27M9M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		210	900	µV
			Full range			3750	
α_{VIO} Average temperature coefficient of input offset voltage			25°C to 125°C		1.7		µV/°C
I_{IO} Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
			125°C		1.4	15	nA
I_{IB} Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
			125°C		9	35	nA
V_{ICR} Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			V
V_{OH} High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
			−55°C	3	3.9		
			125°C	3	4		
V_{OL} Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
			−55°C		0	50	
			125°C		0	50	
A_{VD} Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
			−55°C	15	290		
			125°C	15	120		
CMRR Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		dB
			−55°C	60	89		
			125°C	60	91		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
			−55°C	60	91		
			125°C	60	94		
I_{DD} Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		420	1120	µA
			−55°C		680	1760	
			125°C		280	720	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27M4M TLC27M9M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M9M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	µV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				−55°C	7.8	8.6		
				125°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				−55°C	15	420		
				125°C	15	190		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	94		dB
				−55°C	60	93		
				125°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−55°C	60	91		
				125°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		570	1200	µA
				−55°C		980	2000	
				125°C		360	960	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC27M4Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage	T_A = 25°C to 70°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 2.5 V, V_{IC} = 2.5 V		0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 2.5 V, V_{IC} = 2.5 V		0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 100 kΩ	3.2	3.9		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V to 2 V, R_L= 100 kΩ	25	170		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	70	93		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, V_{IC} = 2.5 V, No load		420	1120	µA

electrical characteristics, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC27M4Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage	T_A = 25°C to 70°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 5 V, V_{IC} = 5 V		0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 5 V, V_{IC} = 5 V		0.7		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 9	−0.3 to 9.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 100 kΩ	8	8.7		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 6 V, R_L = 100 kΩ	25	275		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	70	93		dB
I_{DD}	Supply current (four amplifiers)	V_O = 5 V, V_{IC} = 5 V, No load		570	1200	µA

NOTES:4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4C TLC27M4AC TLC27M4BC TLC27M9C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 100\ \Omega$, $C_L = 20$ pF, See Figure 1	$V_{IPP} = 1$ V	25°C		0.43		V/µs
				0°C		0.46		
				70°C		0.36		
			$V_{IPP} = 2.5$ V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20\ \Omega$	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 100$ kΩ,	$C_L = 20$ pF, See Figure 1	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, See Figure 3	$C_L = 20$ pF,	25°C		525		kHz
				0°C		610		
				70°C		400		
ϕ_m	Phase margin	$V_I = 10$ mV, $C_L = 20$ pF,	$f = B_1$, See Figure 3	25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4C TLC27M4AC TLC27M4BC TLC27M9C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 100\ \Omega$, $C_L = 20$ pF, See Figure 1	$V_{IPP} = 1$ V	25°C		0.62		V/µs
				0°C		0.67		
				70°C		0.51		
			$V_{IPP} = 5.5$ V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20\ \Omega$,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 100$ kΩ,	$C_L = 20$ pF, See Figure 1	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	$V_I = 10$ mV, See Figure 3	$C_L = 20$ pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	$V_I = 10$ mV, $C_L = 20$ pF,	$f = B_1$, See Figure 3	25°C		43°		
				0°C		44°		
				70°C		42°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4I TLC27M4AI TLC27M4BI TLC27M9I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 Ω, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4I TLC27M4AI TLC27M4BI TLC27M9I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 Ω, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−40°C		880		
				85°C		480		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−40°C		46°		
				85°C		41°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4M TLC27M9M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 Ω, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				−55°C		0.50		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		32		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−55°C		850		
				125°C		330		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−55°C		44°		
				125°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27M4M TLC27M9M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 Ω, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		32		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−55°C		50		
				125°C		20		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−55°C		960		
				125°C		440		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−55°C		47°		
				125°C		39°		

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC27M4Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V		0.43		V/μs
			V_{IPP} = 2.5 V		0.40		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1		55		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,		525		kHz
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3		40°		

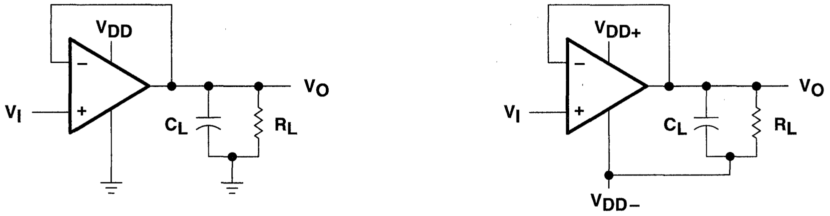
operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC27M4Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V		0.62		V/μs
			V_{IPP} = 5.5 V		0.56		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1		35		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,		635		kHz
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3		43°		

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

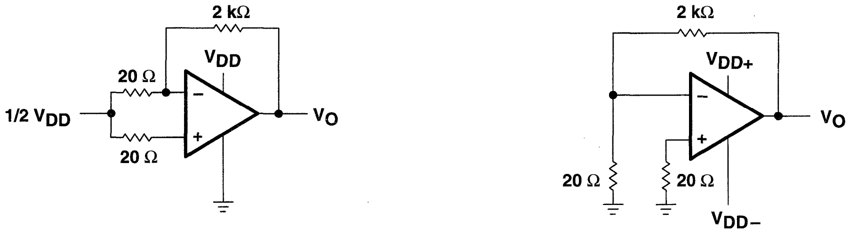
Because the TLC27M4 and TLC27M9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

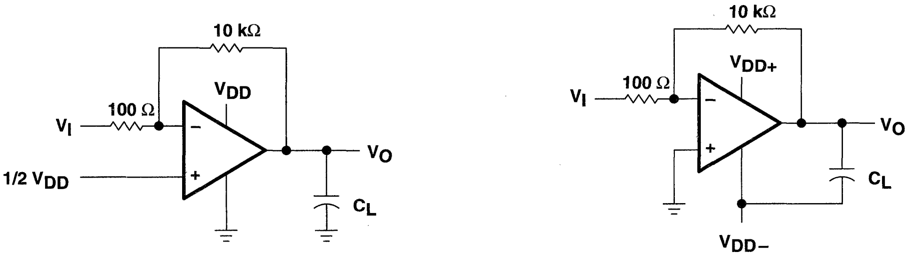
Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27M4 and TLC27M9 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution ... many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

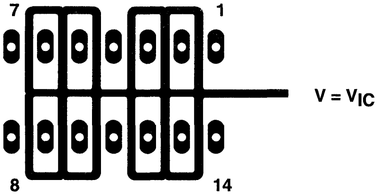


Figure 4. Isolation Metal Around Device Inputs (J and N packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

PARAMETER MEASUREMENT INFORMATION

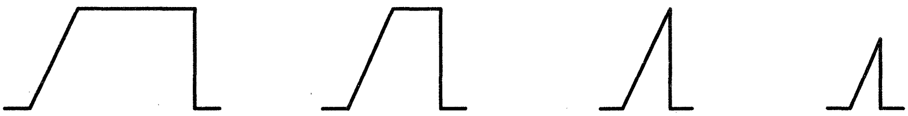
input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 1 kHz (b) 1 kHz < f < B_{OM} (c) f = B_{OM} (d) f > B_{OM}

Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A_{VD}	Differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I_{IB}	Input bias current	vs Free-air temperature	22
I_{IO}	Input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
	Phase shift	vs Frequency	32, 33
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
V_n	Equivalent input noise voltage	vs Frequency	37

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M4 INPUT OFFSET VOLTAGE

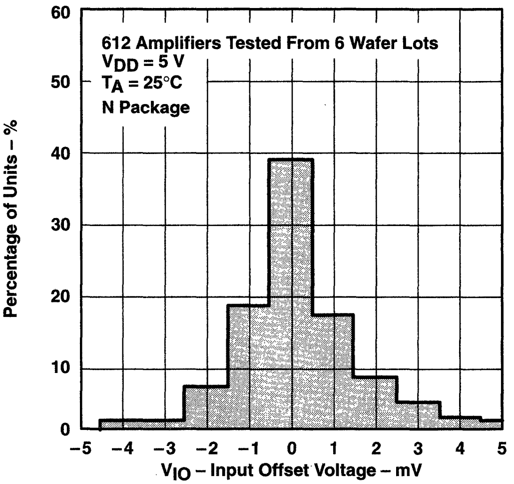


Figure 6

DISTRIBUTION OF TLC27M4 INPUT OFFSET VOLTAGE

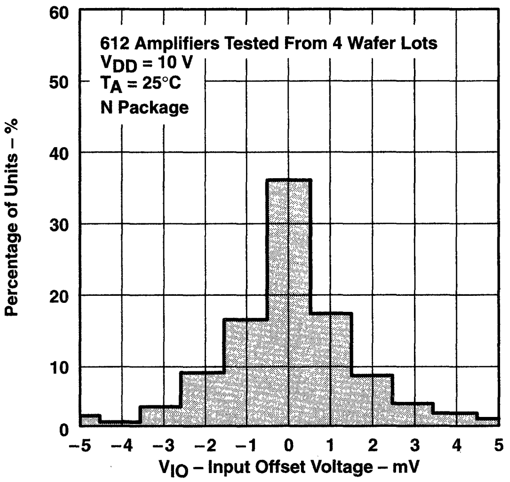


Figure 7

DISTRIBUTION OF TLC27M4 AND TLC27M9 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

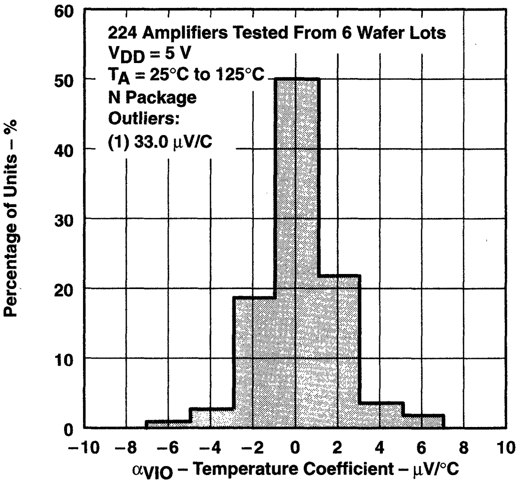


Figure 8

DISTRIBUTION OF TLC27M4 AND TLC27M9 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

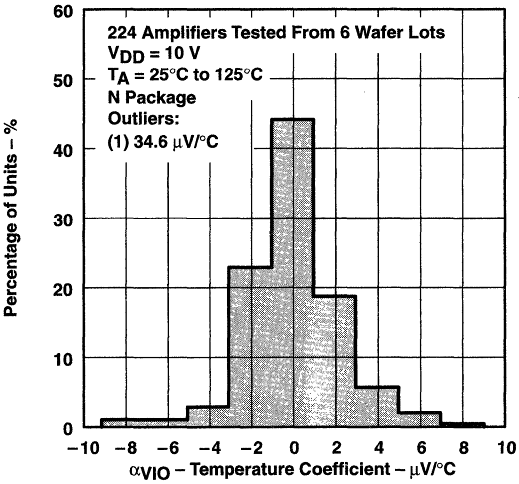


Figure 9

TYPICAL CHARACTERISTICS†

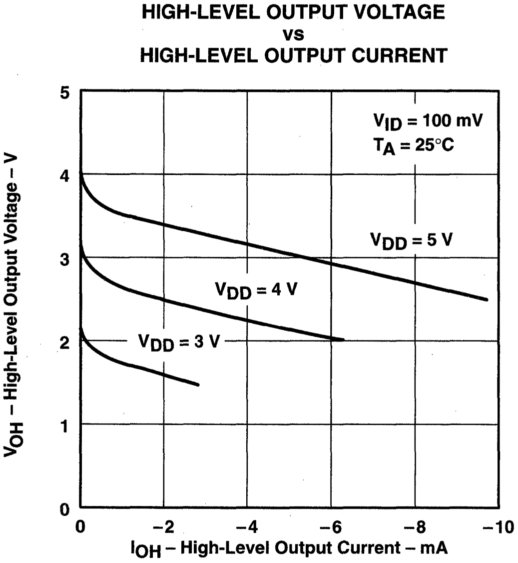


Figure 10

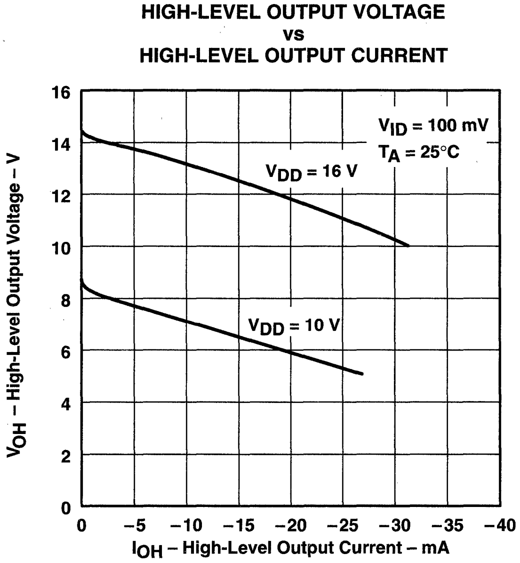


Figure 11

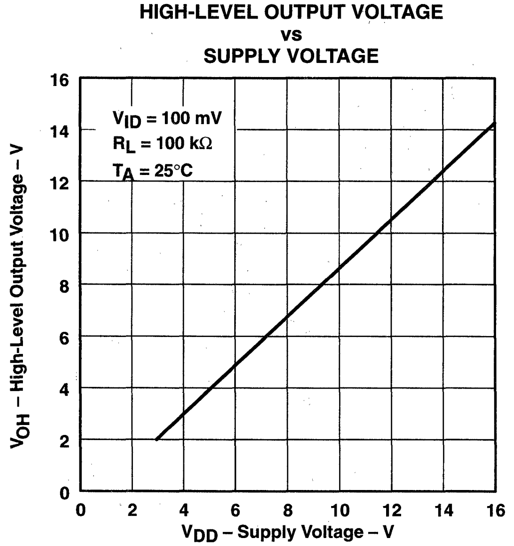


Figure 12

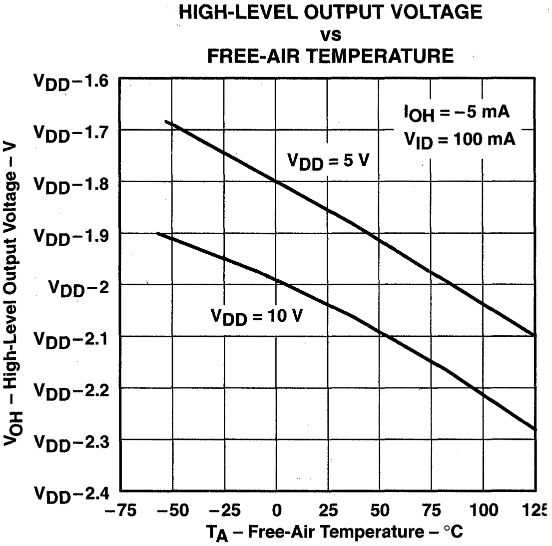


Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

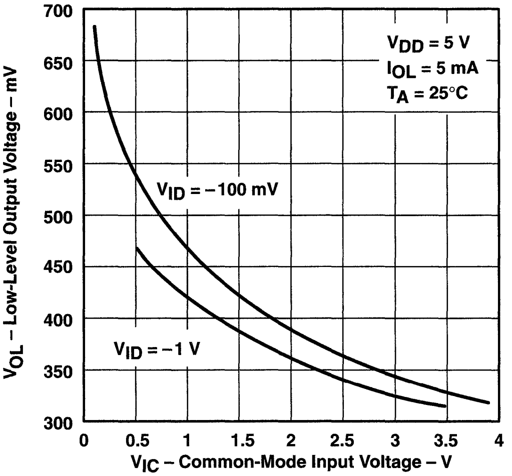

Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

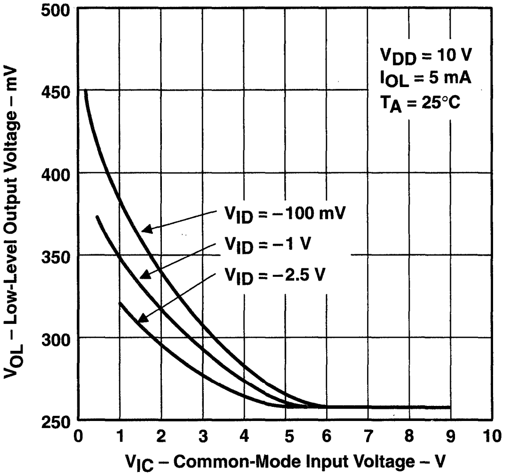

Figure 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

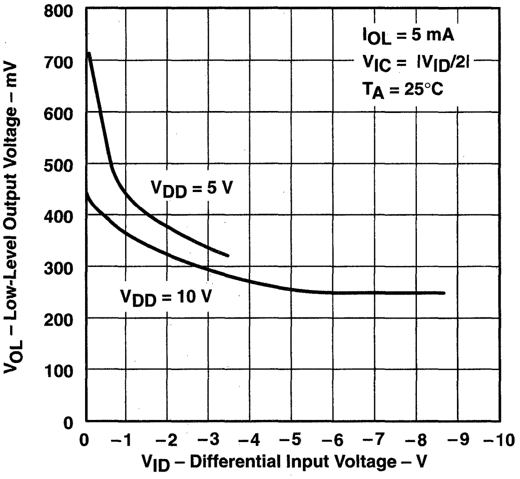

Figure 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

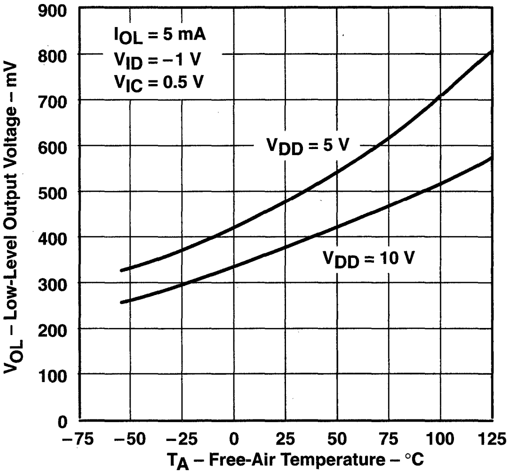

Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

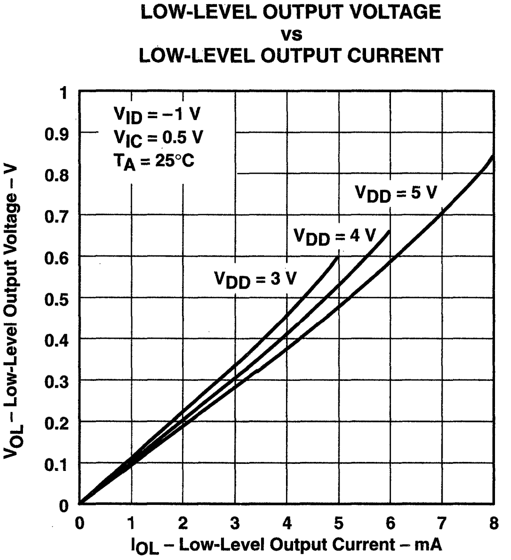

Figure 18

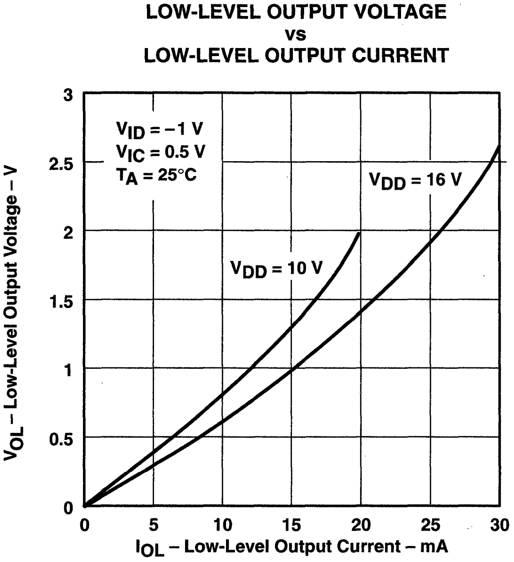

Figure 19

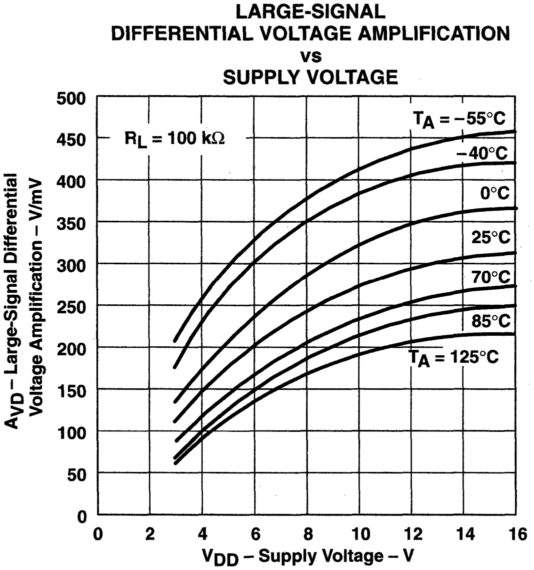

Figure 20

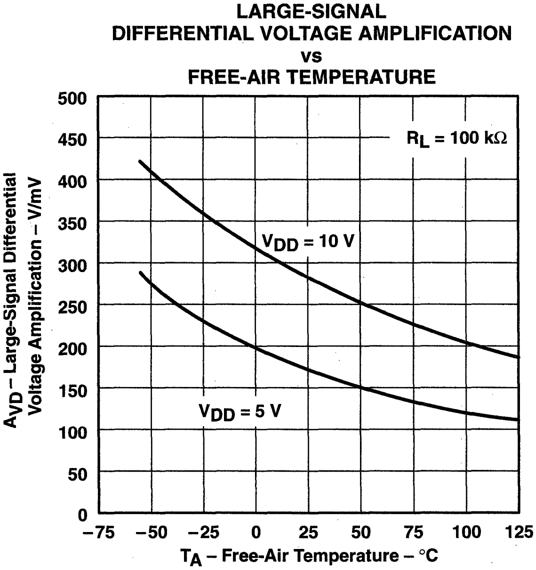

Figure 21

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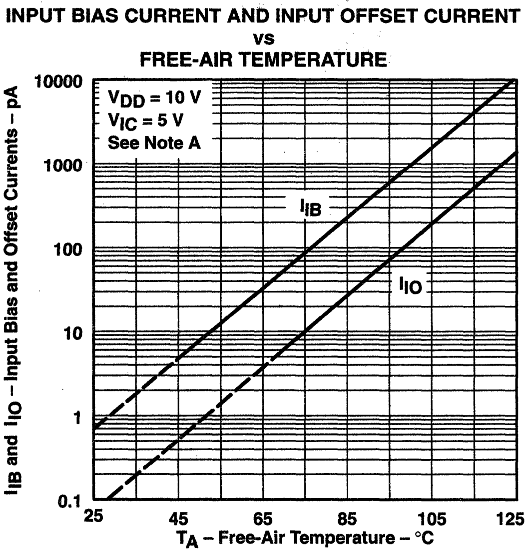
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

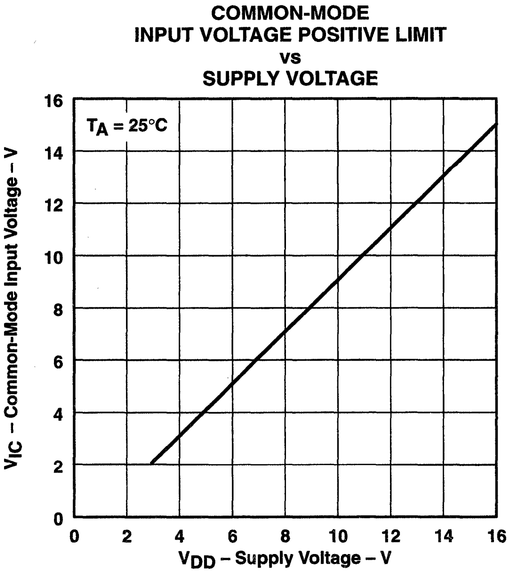


Figure 23

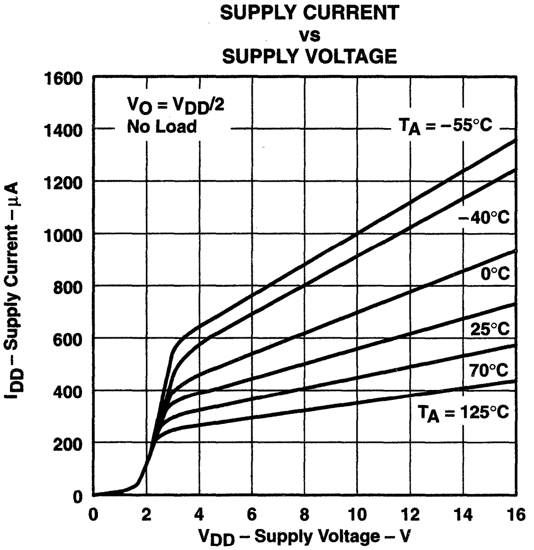


Figure 24

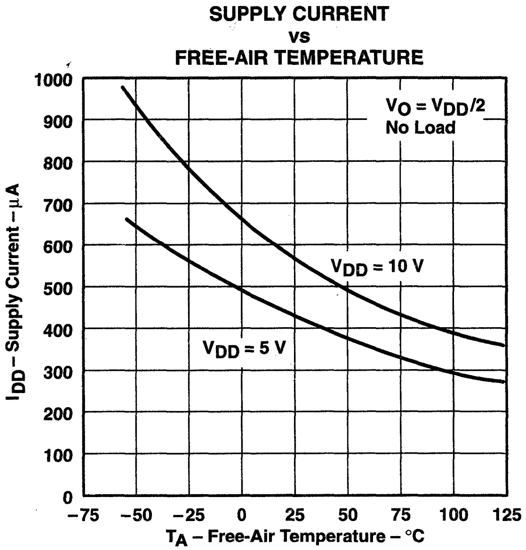


Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

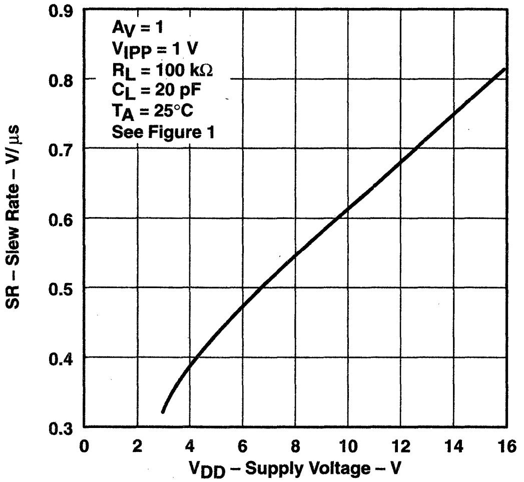

Figure 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

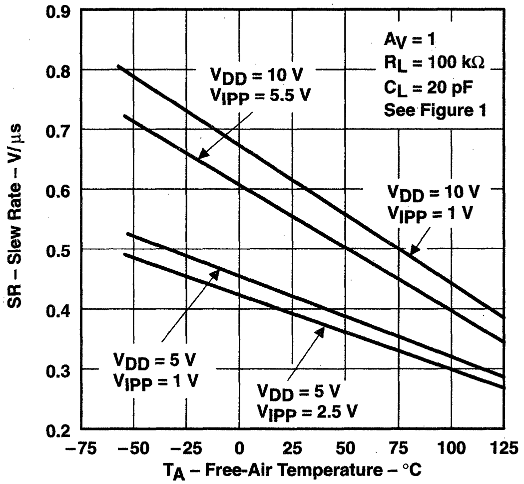

Figure 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

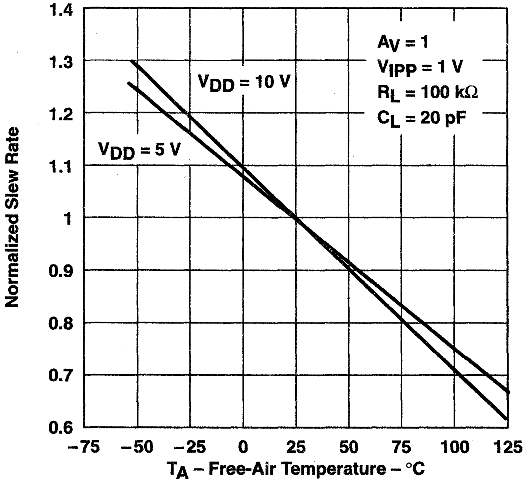

Figure 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

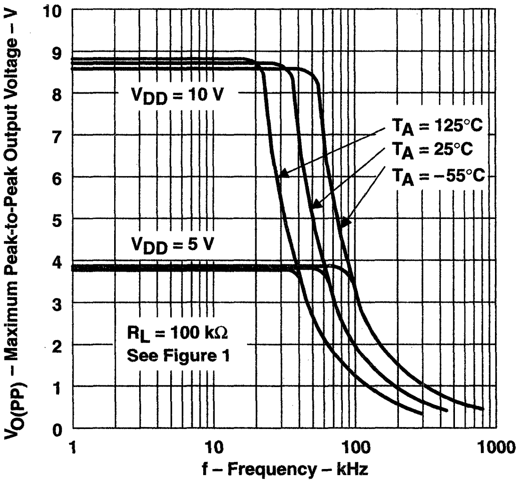

Figure 29

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

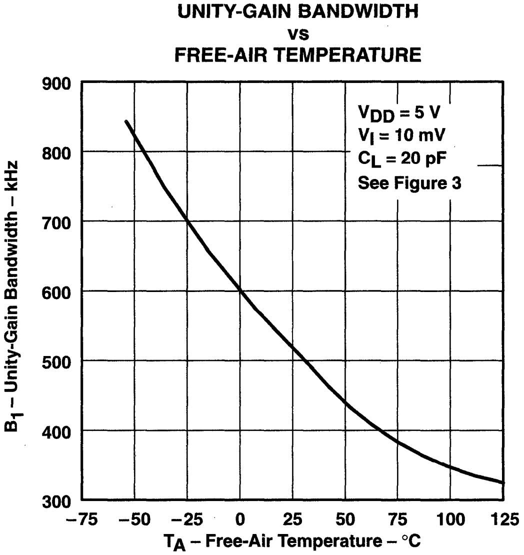

Figure 30

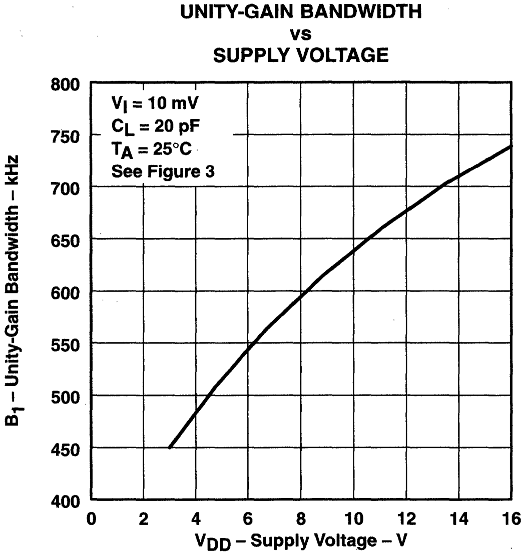

Figure 31

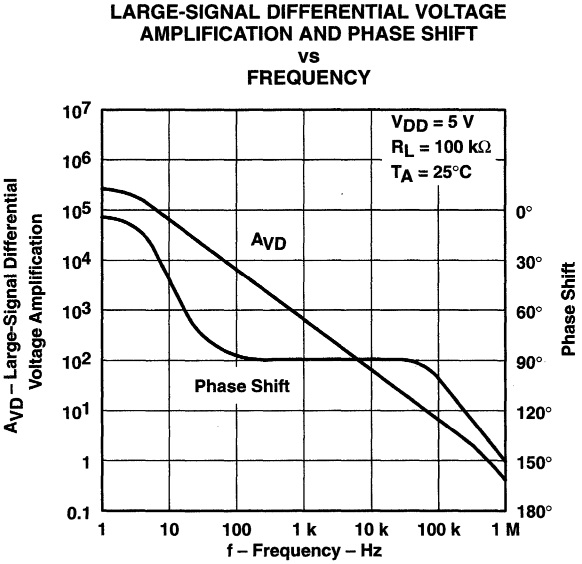

Figure 32

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

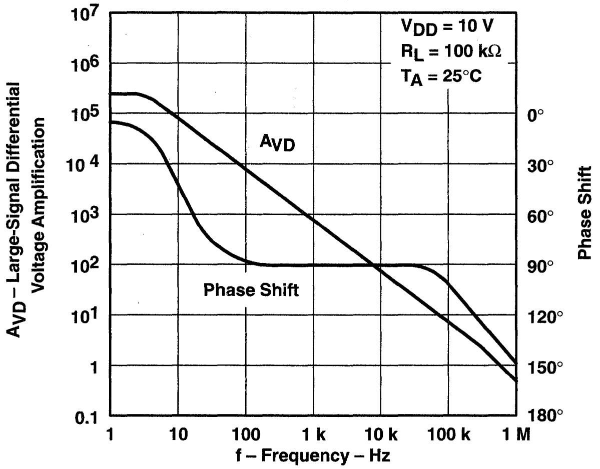

Figure 33

PHASE MARGIN vs SUPPLY VOLTAGE

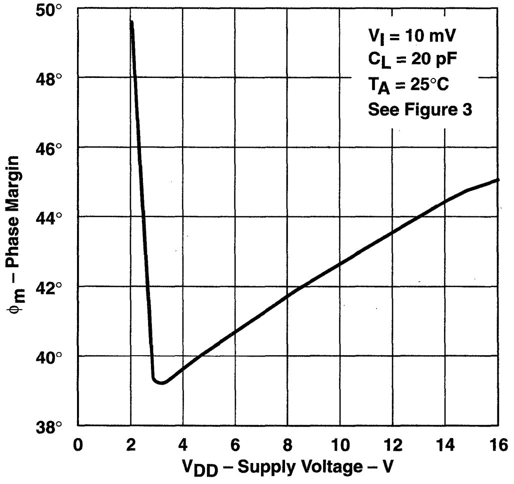

Figure 34

PHASE MARGIN vs FREE-AIR TEMPERATURE

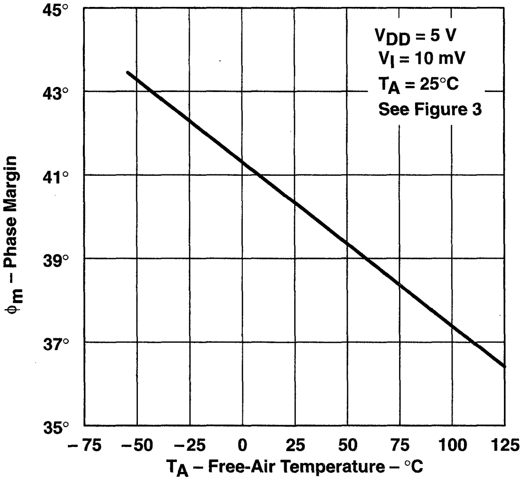

Figure 35

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN vs CAPACITIVE LOAD

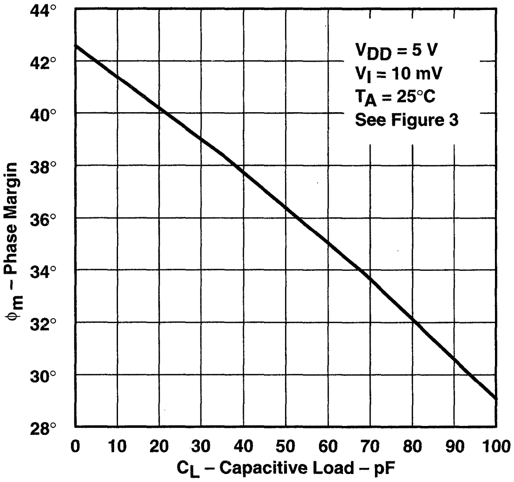


Figure 36

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

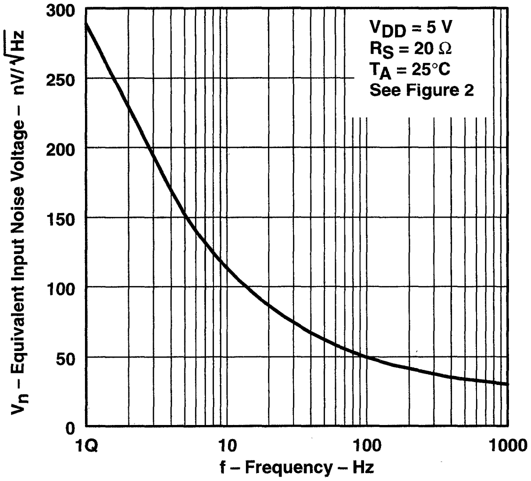


Figure 37

APPLICATION INFORMATION

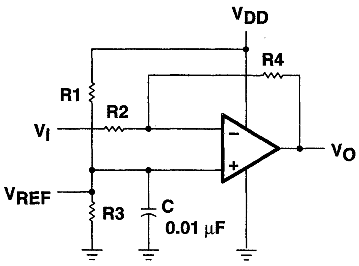
single-supply operation

While the TLC27M4 and TLC27M9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M4 and TLC27M9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M4 and TLC27M9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



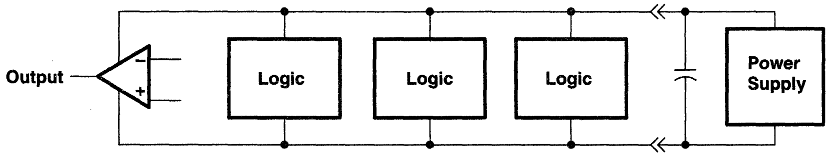
$$V_{REF} = V_{DD}\,\frac{R3}{R1 + R3}$$

$$V_O = (V_{REF} - V_I)\,\frac{R4}{R2} + V_{REF}$$

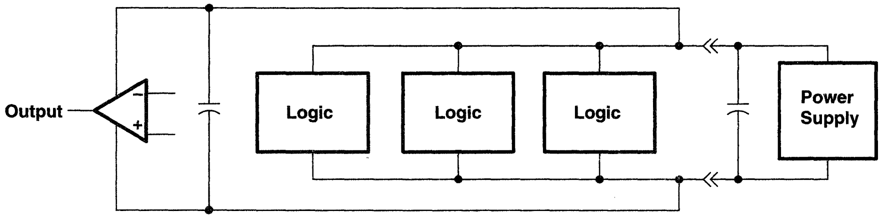
Figure 38. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common Versus Separate Supply Rails

input characteristics

The TLC27M4 and TLC27M9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M4 and TLC27M9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M4 and TLC27M9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

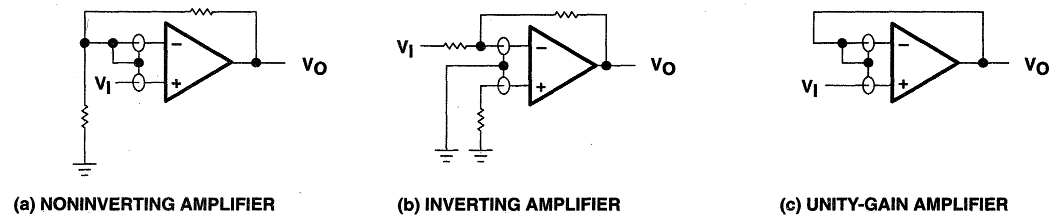
Unused amplifiers should be connected as unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M4 and TLC27M9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

APPLICATION INFORMATION

noise performance (continued)



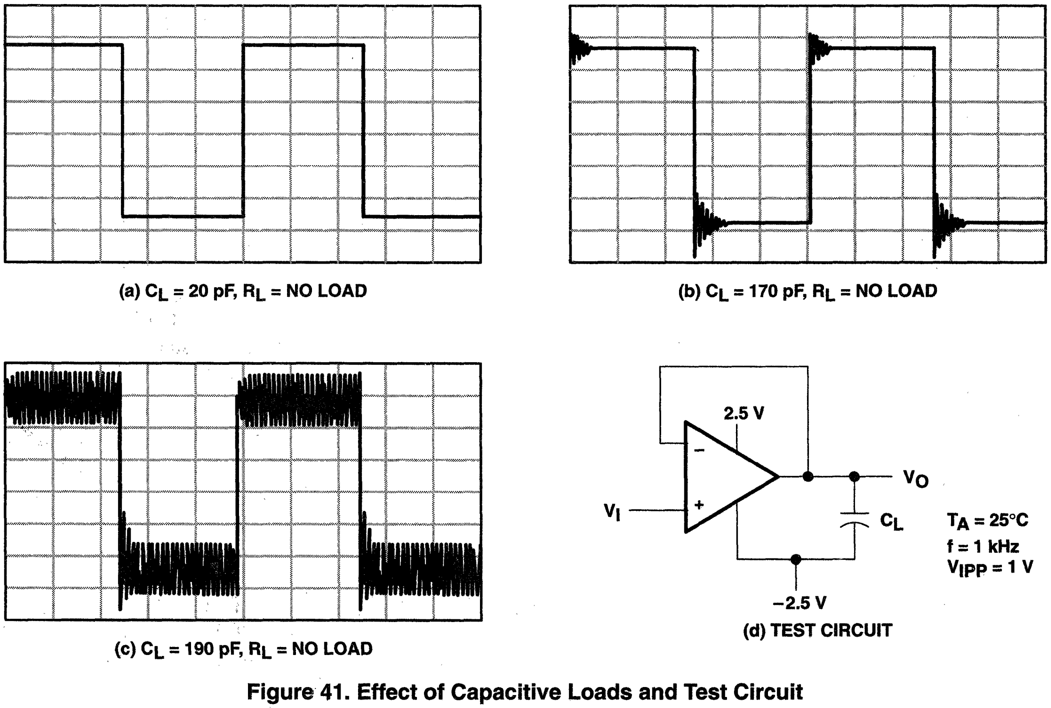
(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 40. Guard-Ring Schemes

output characteristics

The output stage of the TLC27M4 and TLC27M9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M4 and TLC27M9 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.



(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 170 pF, R_L = NO LOAD

(c) C_L = 190 pF, R_L = NO LOAD

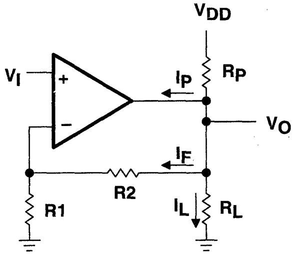
(d) TEST CIRCUIT

Figure 41. Effect of Capacitive Loads and Test Circuit

APPLICATION INFORMATION

output characteristics (continued)

Although the TLC27M4 and TLC27M9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational ampl (typically 500 µA)

Figure 42. Resistive Pullup to Increase V_{OH}

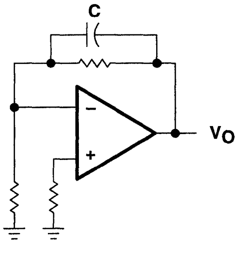


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27M4 and TLC27M9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature-dependent and have the characteristics of a reverse-biased diode.

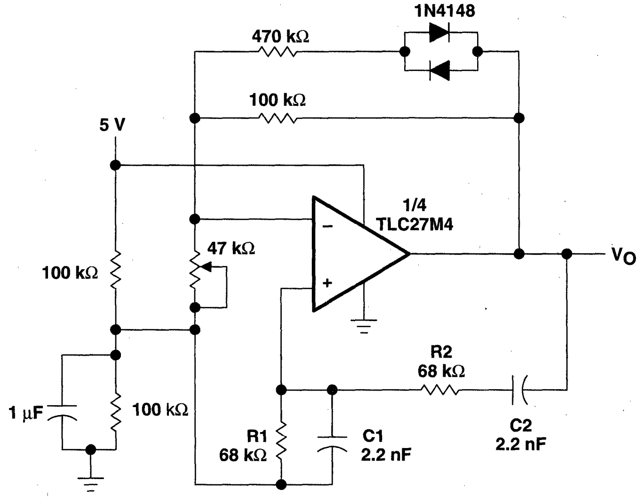
latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27M4 and TLC27M9 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

APPLICATION INFORMATION

latch-up (continued)

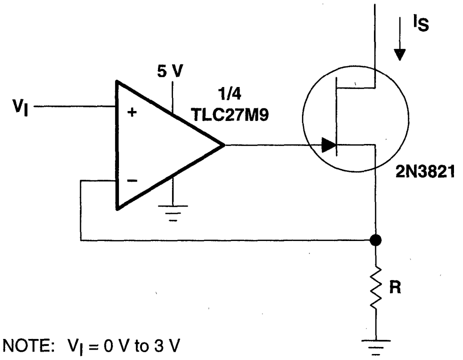
The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.



NOTE: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

Figure 44. Wien Oscillator

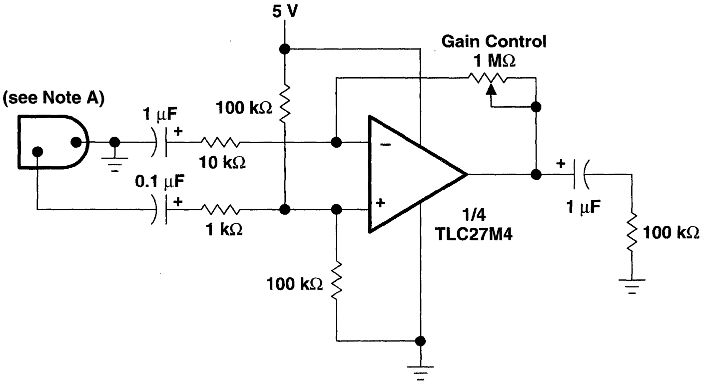


NOTE: $V_I = 0$ V to 3 V

$$I_S = \frac{V_I}{R}$$

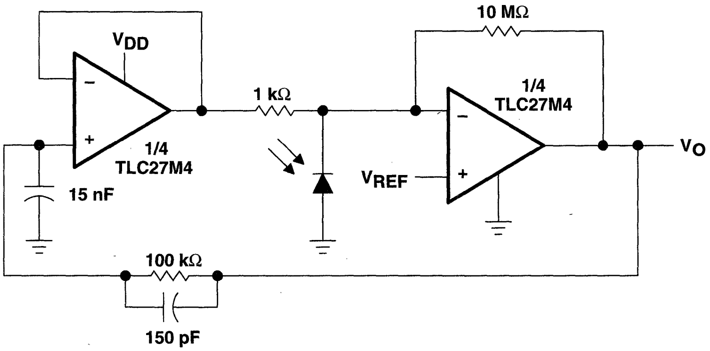
Figure 45. Precision Low-Current Sink

APPLICATION INFORMATION



NOTE A: Low to medium impedance dynamic mike

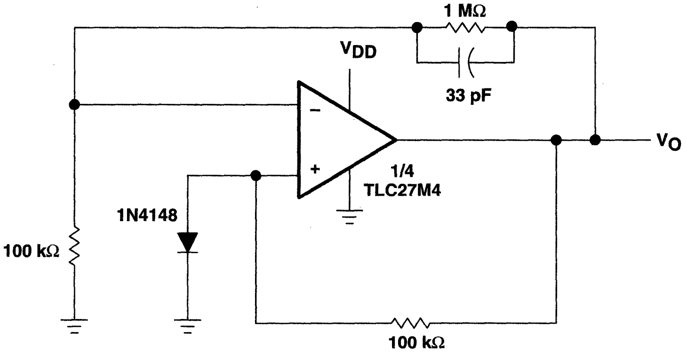
Figure 46. Microphone Preamplifier



NOTE: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} – 2 V

Figure 47. Photo-Diode Amplifier With Ambient Light Rejection

TYPICAL APPLICATION DATA



NOTE: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

Figure 48. Low-Power Voltage Regulator

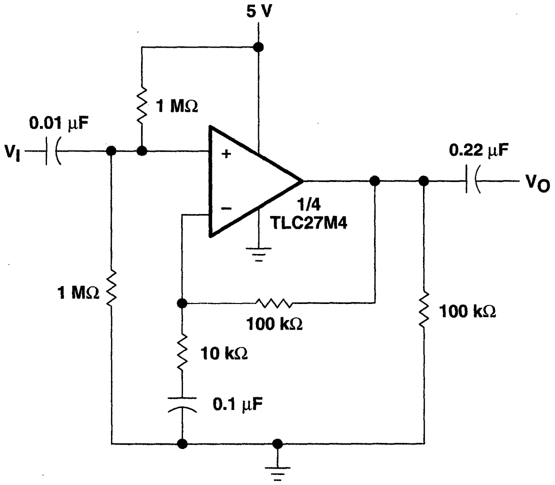


Figure 49. Single-Rail AC Amplifier

TLC1078, TLC1078Y, TLC1079, TLC1079Y
LinCMOS™ µPOWER PRECISION OPERATIONAL AMPLIFIERS

SLOS179 – FEBRUARY 1997

- **Power Dissipation as Low as 10 µW Typ Per Amplifier**
- **Operates on a Single Silver-Oxide Watch Battery, V_{DD} = 1.4 V Min**
- **V_{IO} . . . 450 µV/850 µV Max in DIP and Small-Outline Package (TLC1078/79)**
- **Input Offset Voltage Drift . . . 0.1 µV/Month Typ, Including the First 30 Days**
- **High-impedance LinCMOS™ Inputs I_{IB} = 0.6 pA Typ**
- **High Open-Loop Gain . . . 800000 Typ**
- **Output Drive Capability > 20 mA**
- **Slew Rate . . . 47 V/ms Typ**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative Rail**
- **On-Chip ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**

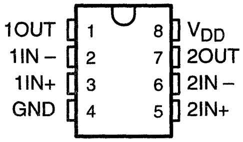
description

The TLC107x operational amplifiers offer ultra-low offset voltage, high gain, 110-kHz bandwidth, 47-V/ms slew rate, and just 150-µW power dissipation per amplifier.

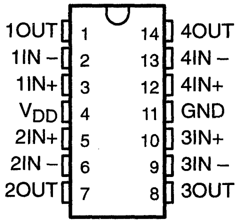
With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC107xC is an ideal solution for low-voltage battery-operated systems. The 20-mA output drive capability means that the TLC107x can easily drive small resistive and large capacitive loads when needed, while maintaining ultra-low standby power dissipation.

Since this device is functionally compatible as well as pin compatible with the TLC27L2/4 and TLC27L7/9, the TLC107x easily upgrades existing designs that can benefit from its improved performance.

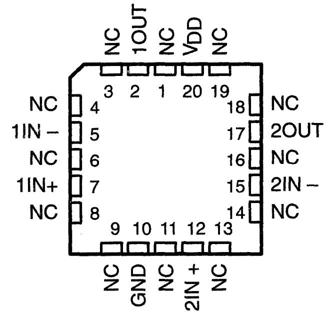
TLC1078
D, JG, OR P PACKAGE
(TOP VIEW)



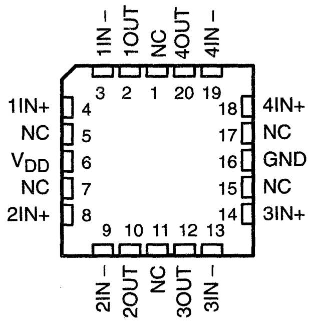
TLC1079
D, J, OR N PACKAGE
(TOP VIEW)



TLC1078
FK PACKAGE
(TOP VIEW)



TLC1079
FK PACKAGE
(TOP VIEW)



NC – No internal connection

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

The TLC107x incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-PRF-38535, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC107x design also inhibits latch-up of the device inputs and outputs even with surge currents as large 100 mA.

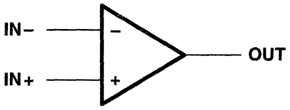
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The wide range of packaging options includes small-outline and chip-carrier versions for high-density system applications.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES						CHIP FORM‡ (Y)
	SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	
0°C to 70°C	TLC1078CD TLC1079CD	—	—	—	TLC1079CN	TLC1078CP	TLC1078Y TLC1079Y
−40°C to 85°C	TLC1078ID TLC1079ID	—	—	—	TLC1079IN	TLC1078IP	—
−55°C to 125°C	TLC1078MD TLC1079MD	TLC1078MFK TLC1079MFK	TLC1079MJ	TLC1078MJG	TLC1079MN	TLC1078MP	—

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC1078CDR).
‡ Chip forms are tested 25°C only.

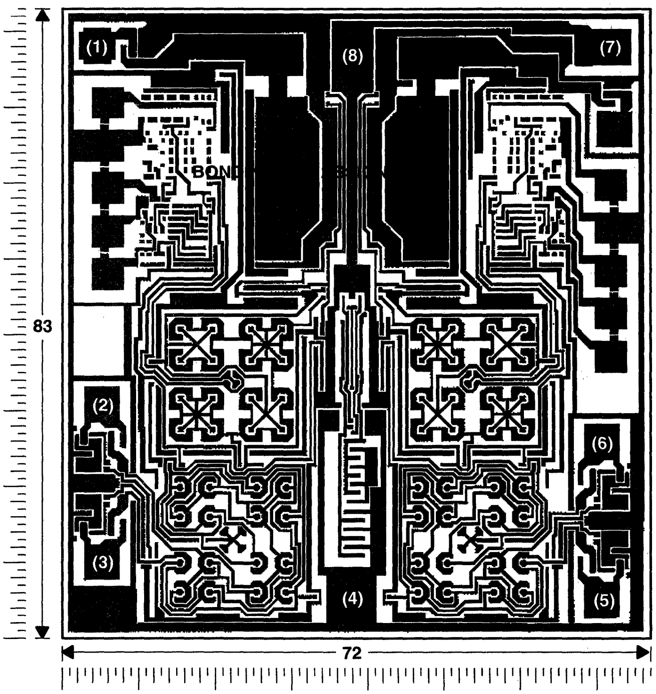
symbol (each amplifier)

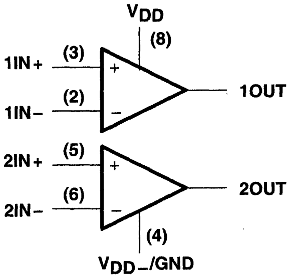


TLC1087Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC1078C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

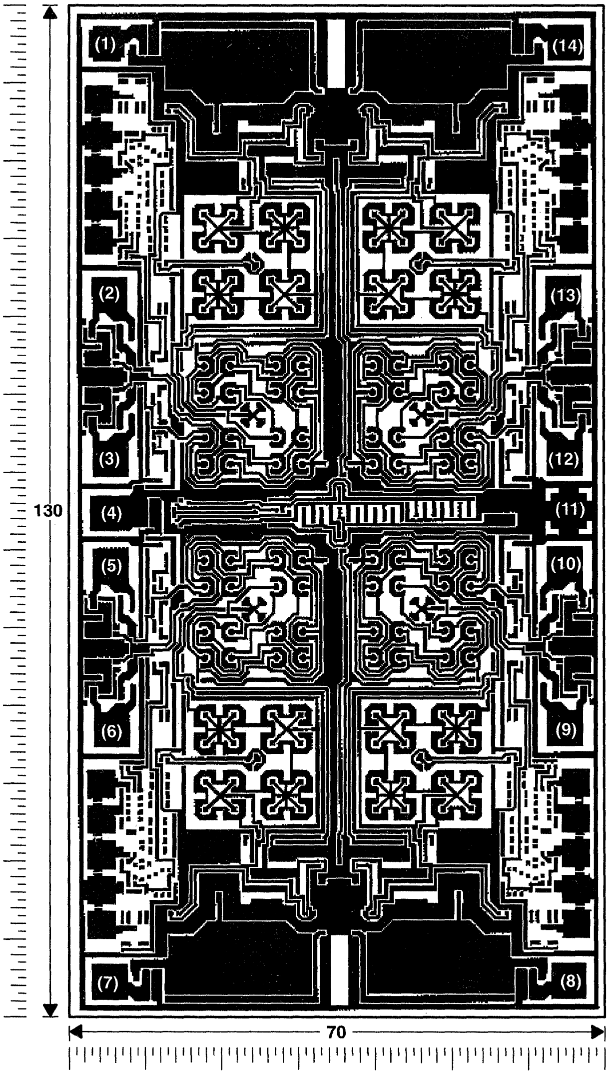
TOLERANCES ARE ±10%.

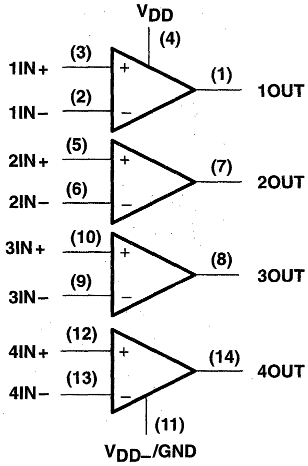
ALL DIMENSIONS ARE IN MILS.

TLC1079Y chip information

This chip, when properly assembled, display characteristics similar to the TLC1079C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

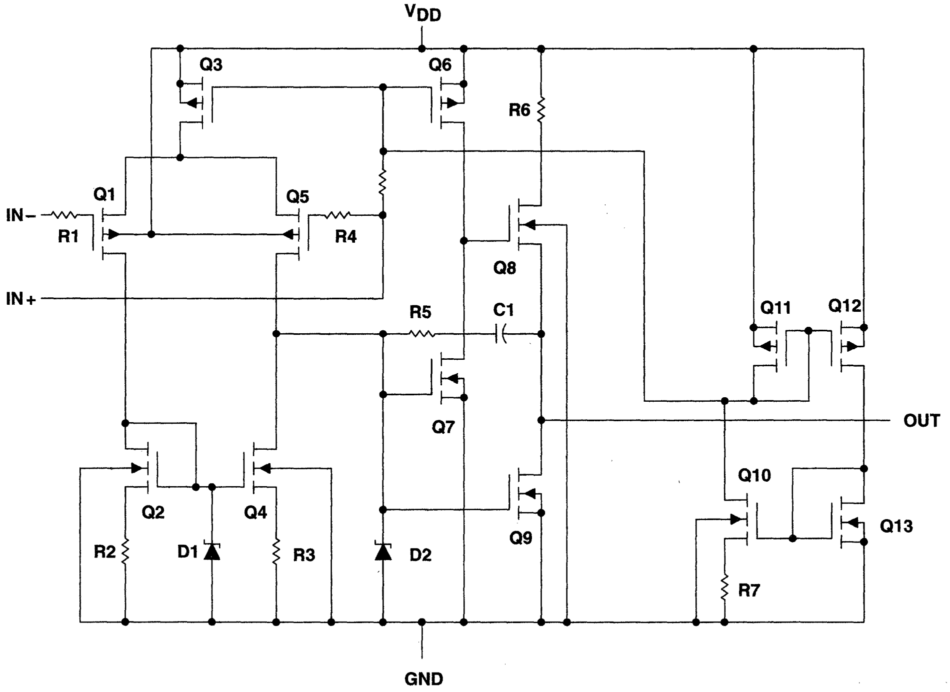
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT		
COMPONENT	**TLC1078**	**TLC1079**
Transistors	38	76
Resistors	16	32
Diodes	12	24
Capacitors	2	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	–0.3 V to V_{DD}
Input current, I_I (each input)	± 5 mA
Output current, I_O (each output)	± 30 mA
Total current into V_{DD} (see Note 3)	45 mA
Duration of short-circuit at (or below) T_A = 25°C (see Note 3)	unlimited
Continuous total power dissipation	see Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	–40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation ratings are not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		1.4	16	3	16	4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	–0.2	4	–0.2	4	0	4	V
	V_{DD} = 10 V	–0.2	9	–0.2	9	0	9	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1078C						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω, V_{IC} = 0, R_I = 1 MΩ	25°C		160	450		180	600	µV
			Full range			800			950	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L= 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L= 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			0°C	250	680		500	1010		
			70°C	200	380		350	660		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		20	34		29	46	µA
			0°C		24	42		36	66	
			70°C		16	28		22	40	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V. V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1079C						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1200			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			70°C		40	600		50	600	
V_{ICR}	Common mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			0°C	250	700		500	1010		
			70°C	200	380		350	660		
CMRR	Common mode rejection ratio	V_{IC} = V_{ICR}min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		40	68		57	92	μA
			0°C		48	84		72	132	
			70°C		31	56		44	80	

† Full range is 0°C to 70°C.

NOTES:
4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A	TLC1078C						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, $V_{I(PP)}$ = 1 V, See Figure 1	25°C		32			47		V/ms
			0°C		35			51		
			70°C		27			38		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			0°C		100			125		
			70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			0°C		36°			40°		
			70°C		30°			34°		

operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A	TLC1079C						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, $V_{I(PP)}$ = 1 V, See Figure 1	25°C		32			47		V/ms
			0°C		35			51		
			70°C		27			38		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			0°C		100			125		
			70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			0°C		36°			40°		
			70°C		30°			34°		

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1078I						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω, V_{IC} = 0, R_I = 1 MΩ	25°C		160	450		180	600	µV
			Full range			950			1100	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			−40°C	250	900		500	1550		
			85°C	150	300		250	585		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\mathrm{min}$	25°C	70	95		75	97		dB
			−40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_O = 1.4 V	25°C	75	98		75	98		dB
			−40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		20	34		29	46	µA
			−40°C		31	54		50	86	
			85°C		15	26		20	36	

† Full range is −40°C to 80°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1079I						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	µV
			Full range			1350			1650	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			−40°C	250	900		500	1550		
			85°C	150	330		250	585		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	70	95		75	97		dB
			−40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		40	68		57	92	µA
			−40°C		62	108		98	172	
			85°C		29	52		40	72	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A	TLC1078I						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, $V_{I(PP)}$ = 1 V, See Figure 1	25°C		32			47		V/ms
			−40°C		39			59		
			85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−40°C		130			155		
			85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−40°C		38°			40°		
			85°C		28°			32°		

operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A	TLC1079I						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, $V_{I(PP)}$ = 1 V, See Figure 1	25°C		32			47		V/ms
			−40°C		39			59		
			85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−40°C		130			155		
			85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−40°C		38°			42°		
			85°C		28°			32°		

electrical characteristics at specified operating free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1078M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		160	450		180	600	µV
			Full range			1250			1400	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L= 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−55°C	3.2	4.1		8.2	8.8		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L= 1 MΩ , See Note 6	25°C	250	525		500	850		V/mV
			−55°C	250	950		500	1750		
			125°C	35	200		75	380		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	70	95		75	97		dB
			−55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_O = 1.4 V	25°C	75	98		75	98		dB
			−55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		20	34		29	46	µA
			−55°C		35	60		56	96	
			125°C		14	24		18	30	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1079M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1600			1900	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−55°C	3.2	4.1		8.2	8.9		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			−55°C	250	950		500	1750		
			125°C	35	200		75	380		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	70	95		75	97		dB
			−55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		40	68		57	92	μA
			−55°C		69	120		111	192	
			125°C		27	48		35	60	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

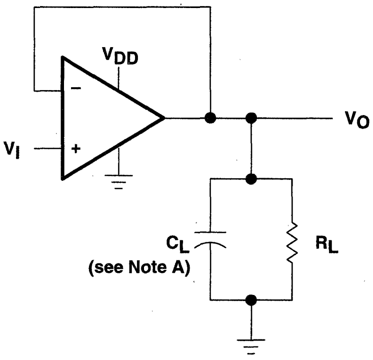
operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A	TLC1078M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, $V_{I(PP)}$ = 1 V, See Figure 1	25°C		32			47		V/ms
			−55°C		41			63		
			125°C		20			27		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−55°C		140			165		
			125°C		45			70		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−55°C		39°			43°		
			125°C		25°			29°		

operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A	TLC1079M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, $V_{I(PP)}$ = 1 V, See Figure 1	25°C		32			47		V/ms
			−55°C		41			63		
			125°C		20			27		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−55°C		140			165		
			125°C		45			70		
			25°C		34°			38°		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	−55°C		39°			43°		
			125°C		25°			29°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

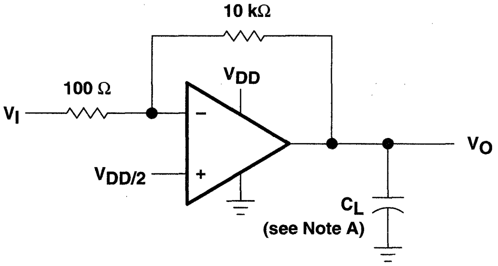


Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

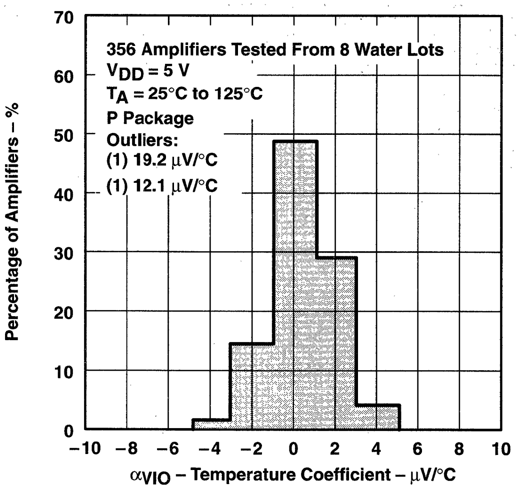


Figure 3

DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

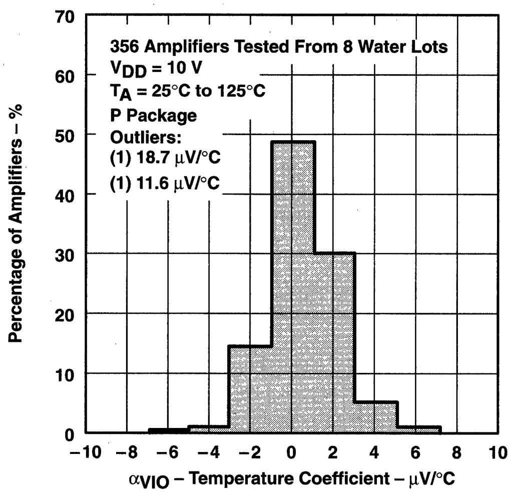


Figure 4

DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

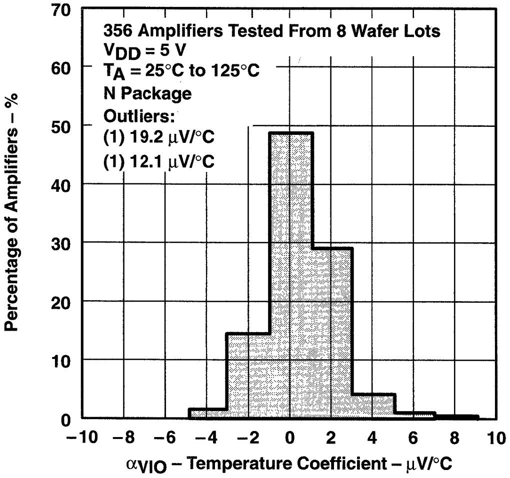


Figure 5

DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

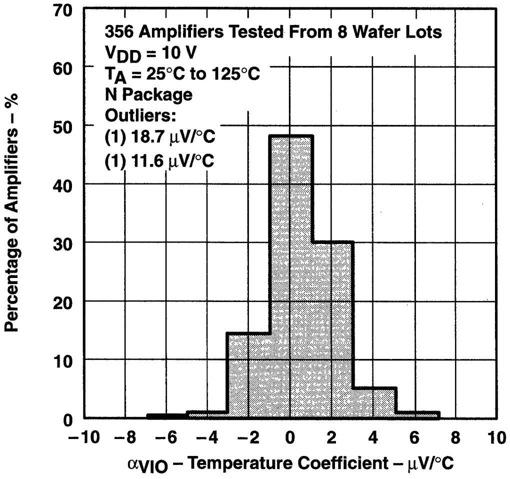
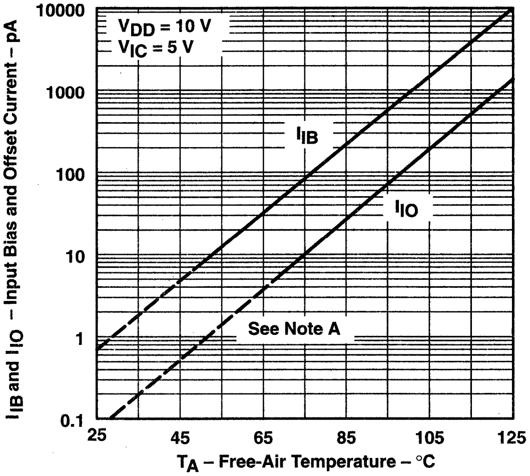


Figure 6

TYPICAL CHARACTERISTICS

INPUT BIAS AND OFFSET CURRENT†
vs
FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 7

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

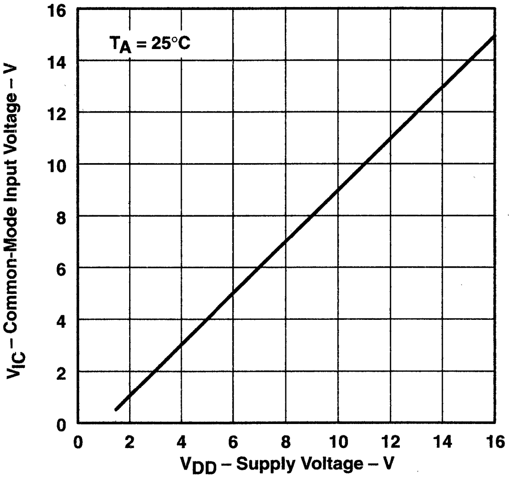


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

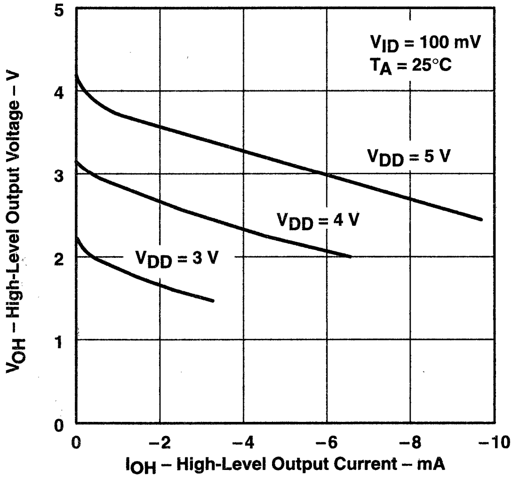


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

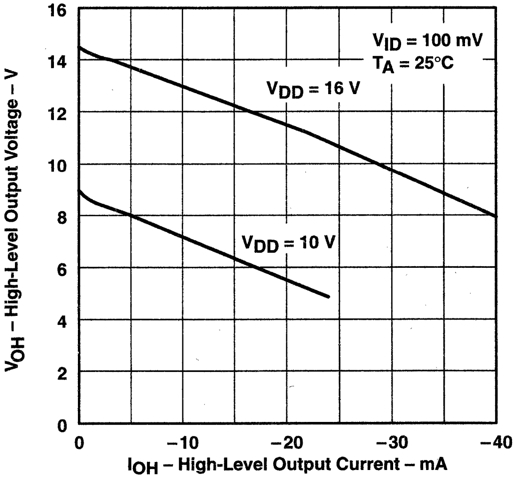


Figure 10

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
† The V_{DD} = 3 V curve does not apply to the TLC107xM.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

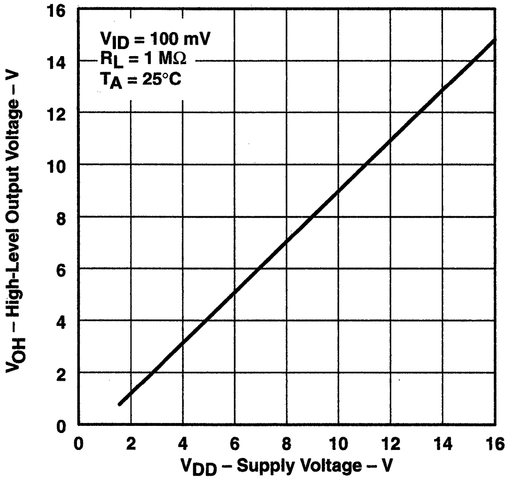

Figure 11

HIGH-LEVEL OUTPUT VOLTAGE†
vs
FREE-AIR TEMPERATURE

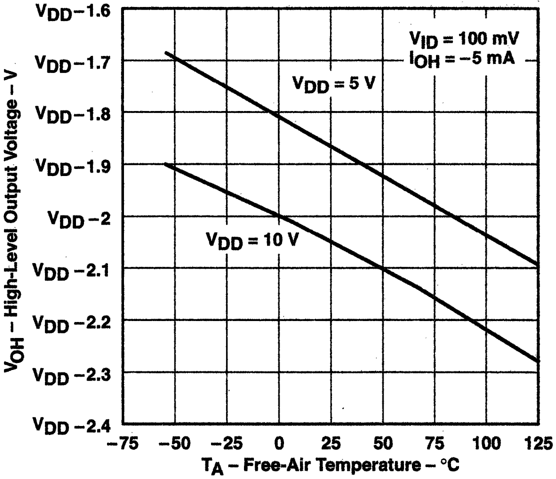

Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

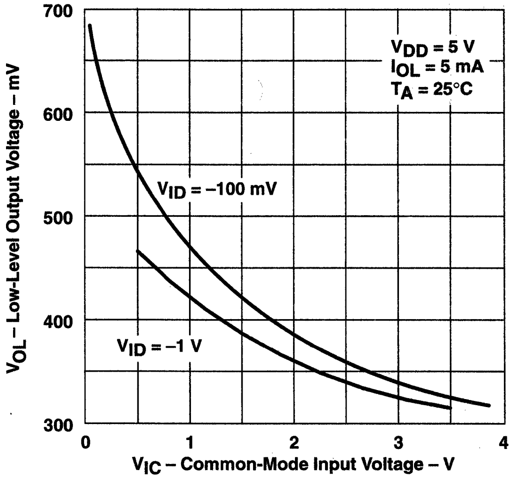

Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

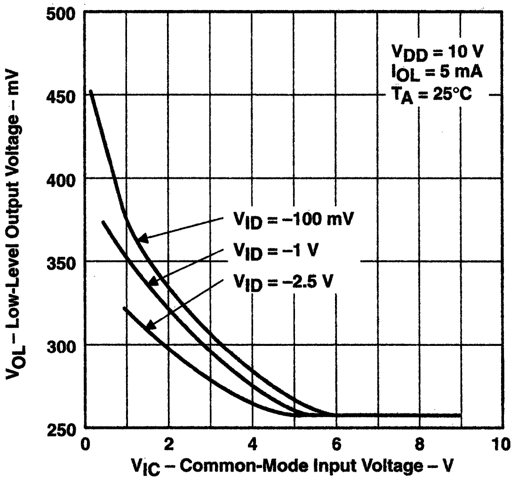

Figure 14

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

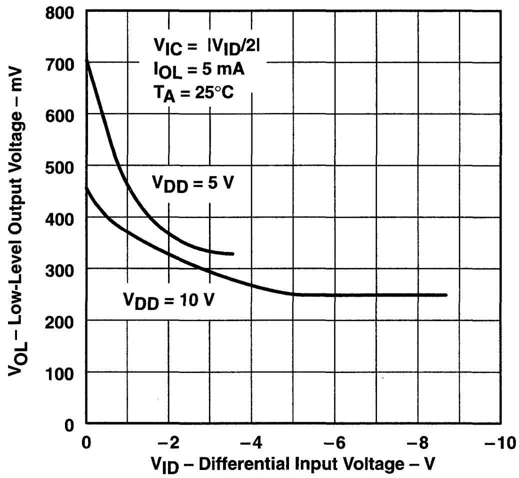

Figure 15

LOW-LEVEL OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE

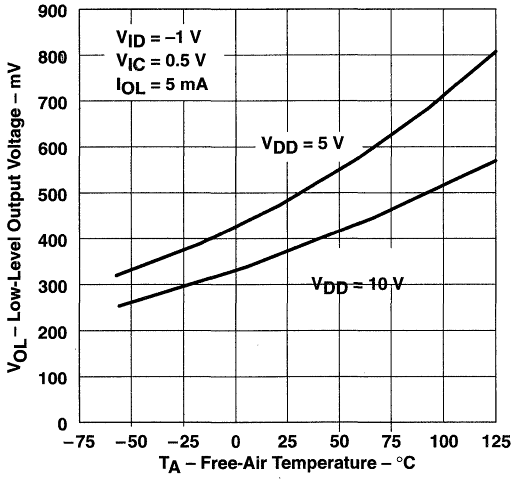

Figure 16

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

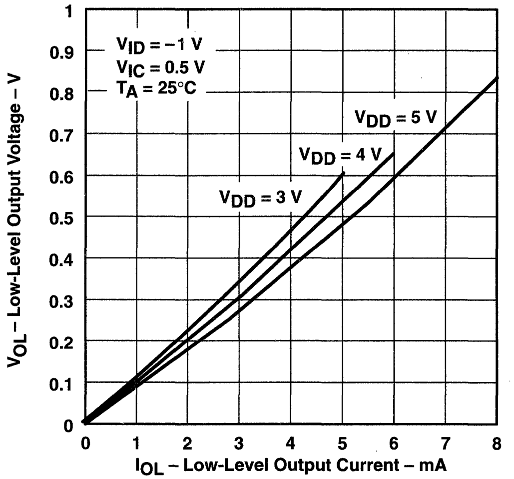

Figure 17

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

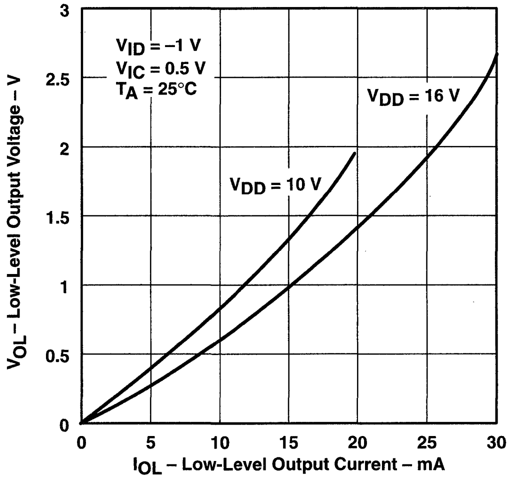

Figure 18

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs SUPPLY VOLTAGE

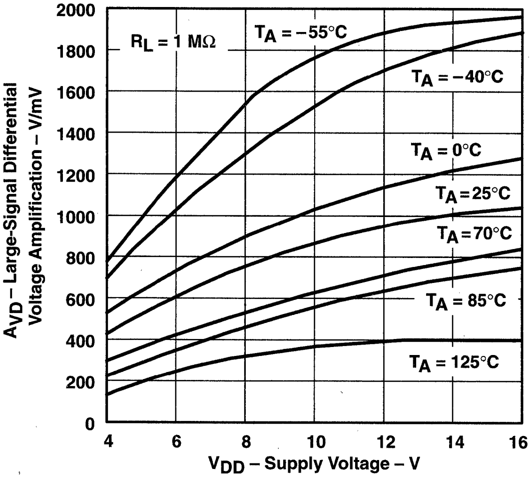

Figure 19

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

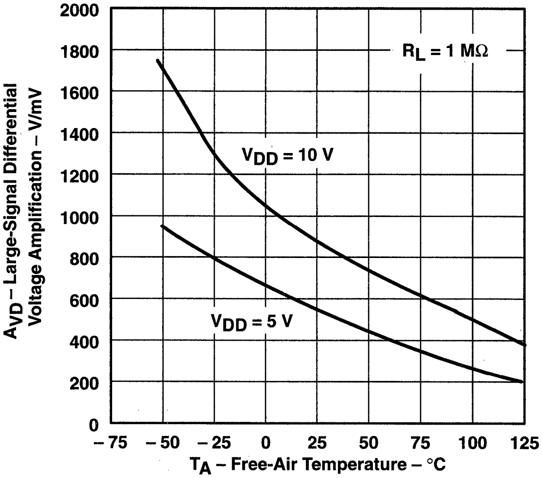

Figure 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

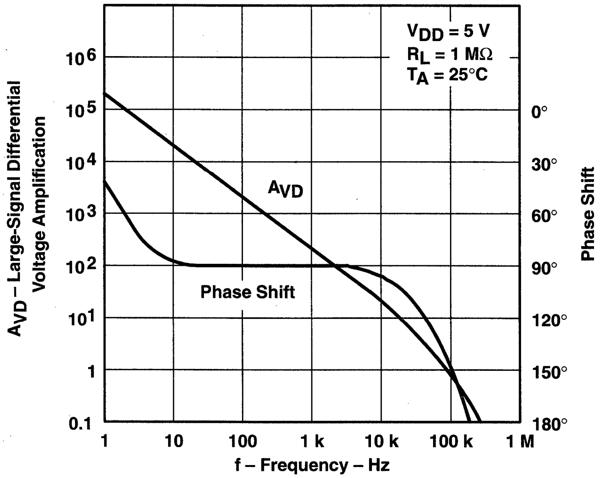

Figure 21

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

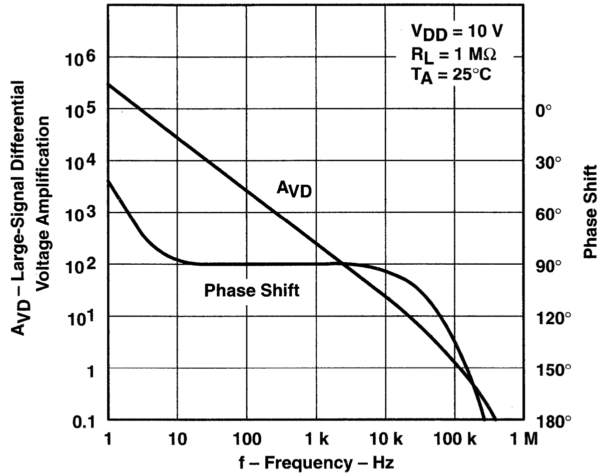

Figure 22

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

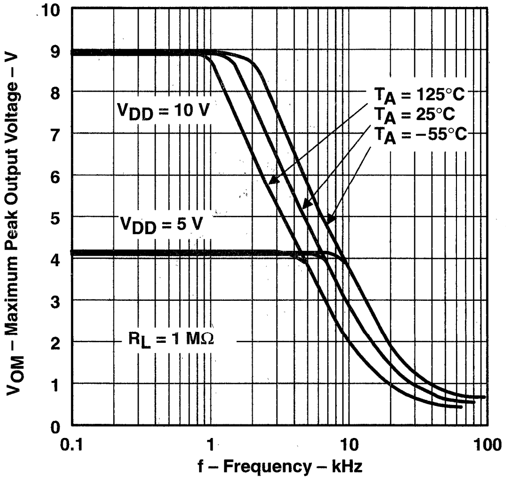

Figure 23

SUPPLY CURRENT† vs SUPPLY VOLTAGE

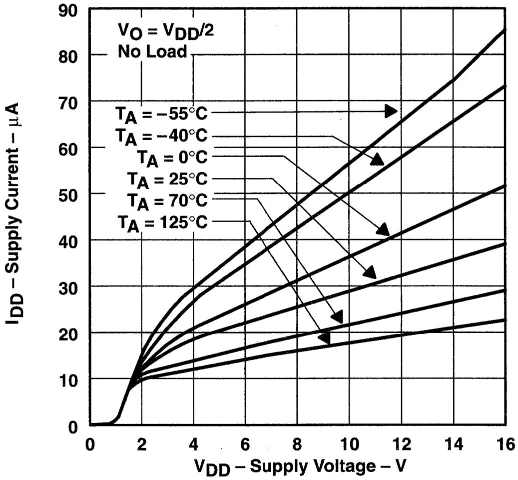

Figure 24

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

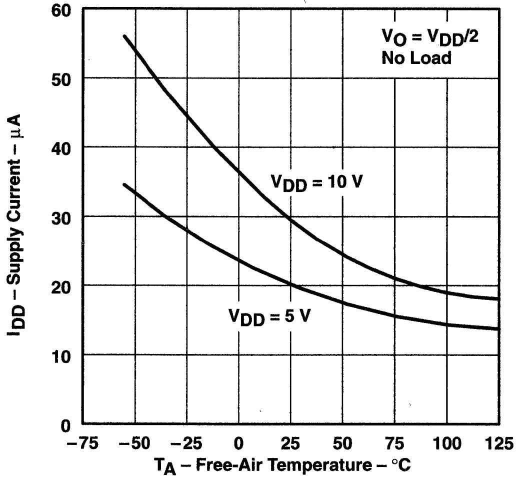

Figure 25

SLEW RATE
vs
SUPPLY VOLTAGE

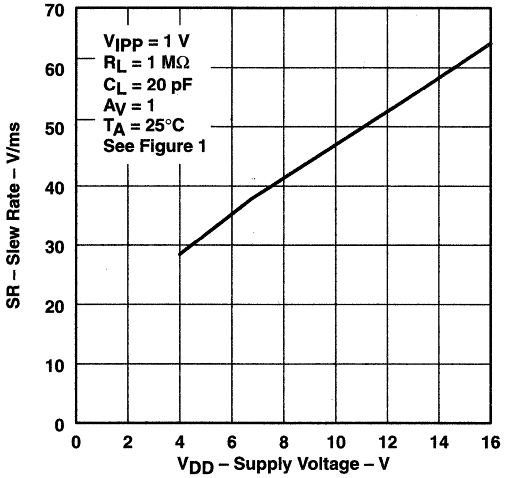

Figure 26

SLEW RATE†
vs
FREE-AIR TEMPERATURE

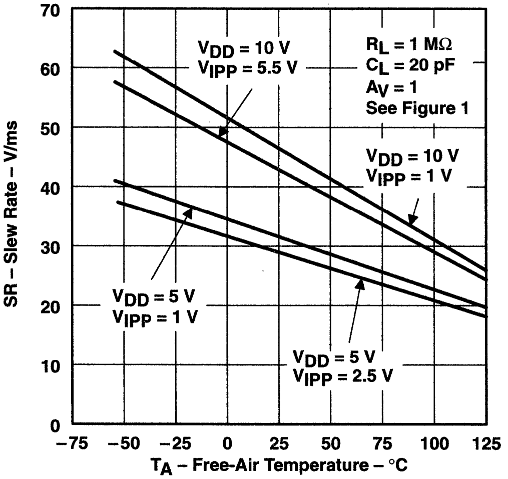

Figure 27

NORMALIZED SLEW RATE†
vs
FREE-AIR TEMPERATURE

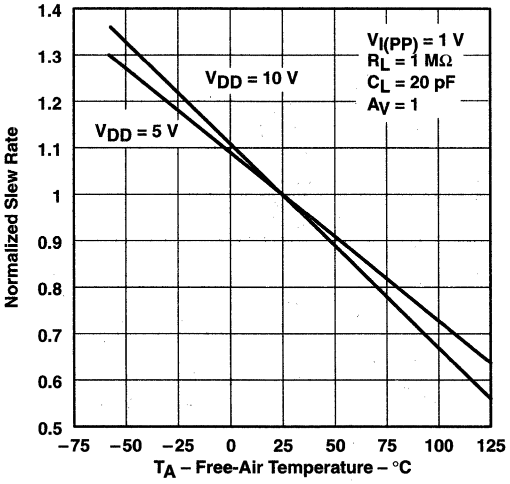

Figure 28

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

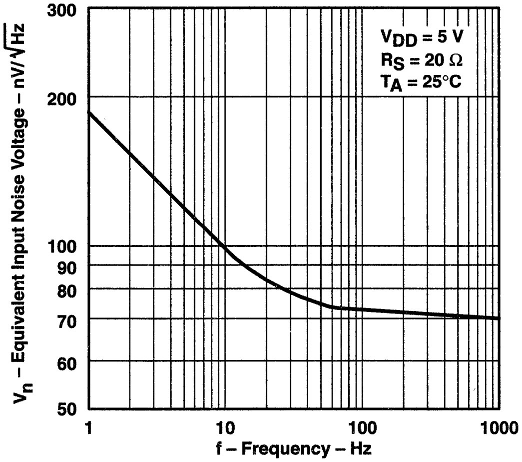

Figure 29

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

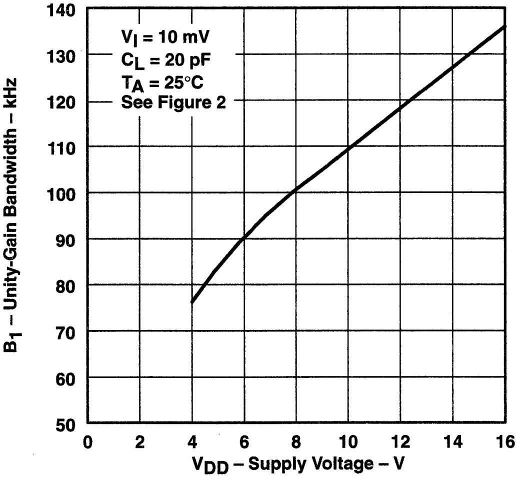

Figure 30

UNITY-GAIN BANDWIDTH† vs FREE-AIR TEMPERATURE

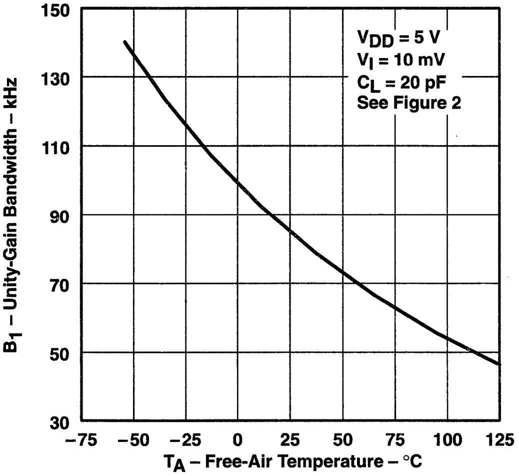

Figure 31

PHASE MARGIN vs SUPPLY VOLTAGE

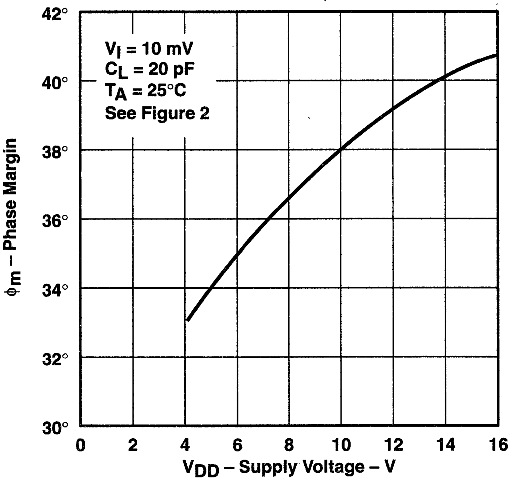

Figure 32

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

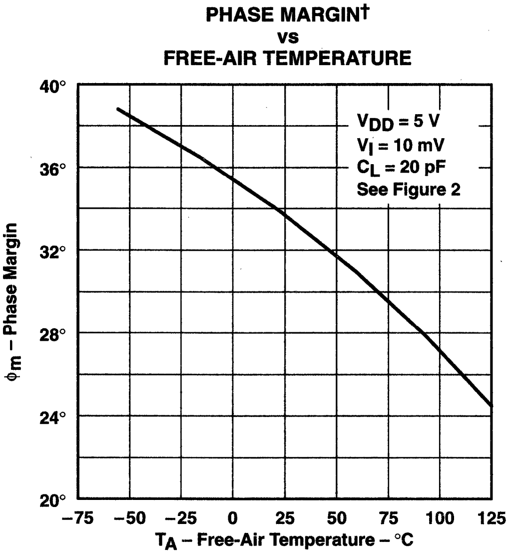

Figure 33

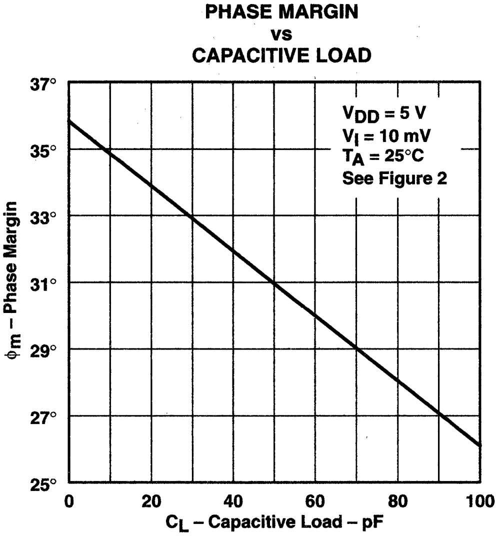

Figure 34

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC220x, TLC220xA, TLC220xB, TLC220xY
Advanced LinCMOS™ LOW-NOISE PRECISION OPERATIONAL AMPLIFIERS

SLOS175 – FEBRUARY 1997

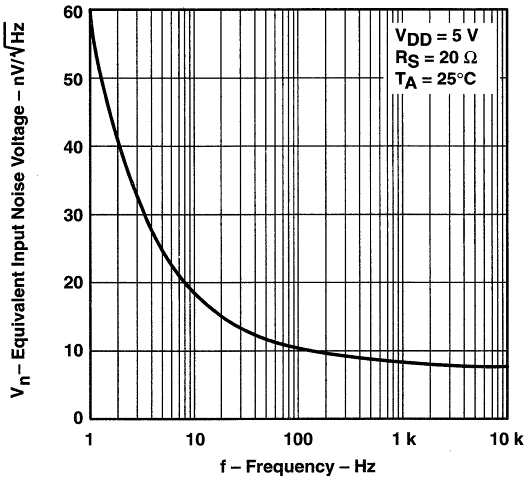
- **B Grade Is 100% Tested for Noise**
  30 nV/√Hz Max at f = 10 Hz
  12 nV/√Hz Max at f = 1 kHz
- **Low Input Offset Voltage . . . 500 μV Max**
- **Excellent Offset Voltage Stability With Temperature . . . 0.5 μV/°C Typ**
- **Rail-to-Rail Output Swing**
- **Low Input Bias Current**
  1 pA Typ at T_A = 25°C
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **Fully Specified For Both Single-Supply and Split-Supply Operation**

description

The TLC220x, TLC220xA, TLC220xB, and TLC220xY are precision, low-noise operational amplifiers using Texas Instruments Advanced LinCMOS™ process. These devices combine the noise performance of the lowest-noise JFET amplifiers with the dc precision available previously only in bipolar amplifiers. The Advanced LinCMOS™ process uses silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. In addition, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The combination of excellent dc and noise performance with a common-mode input voltage range that includes the negative rail makes these devices an ideal choice for high-impedance, low-level signal-conditioning applications in either single-supply or split-supply configurations.

TYPICAL EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY



The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures at voltages up to 2000 V as tested under MIL-PRF-38535, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TLC2201 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	$V_n$max f = 10 Hz AT 25°C	$V_n$max f = 1 kHz AT 25°C	PACKAGED DEVICES				CHIP FORM‡ (Y)
				SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	200 μV 200 μV 500 μV	35 nV/√Hz 30 nV/√Hz —	15 nV/√Hz 12 nV/√Hz —	TLC2201ACD TLC2201BCD TLC2201CD	—	—	TLC2201ACP TLC2201BCP TLC2201CP	TLC2201Y
−40°C to 85°C	200 μV 200 μV 500 μV	35 nV/√Hz 30 nV/√Hz —	15 nV/√Hz 12 nV/√Hz —	TLC2201AID TLC2201BID TLC2201ID	—	—	TLC2201AIP TLC2201BIP TLC2201IP	—
−55°C to 125°C	200 μV 200 μV 500 μV	35 nV/√Hz 30 nV/√Hz —	15 nV/√Hz 12 nV/√Hz —	TLC2201AMD TLC2201BMD TLC2201MD	TLC2201AMFK TLC2201BMFK TLC2201MFK	TLC2201AMJG TLC2201BMJG TLC2201MJG	TLC2201AMP TLC2201BMP TLC2201MP	—

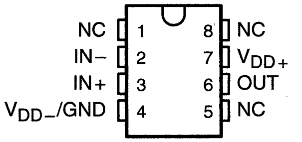
† The D packages are available taped and reeled. Add R suffix to device type (e.g. TLC220xBCDR).
‡ Chip forms are tested at 25°C only.

TLC2202 AVAILABLE OPTIONS

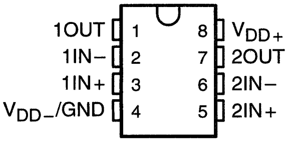
T_A	V_{IO}max AT 25°C	$V_n$max f = 10 Hz AT 25°C	$V_n$max f = 1 kHz AT 25°C	PACKAGED DEVICES				CHIP FORM‡ (Y)
				SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	500 μV 500 μV 1 mV	30 nV/√Hz 35 nV/√Hz —	12 nV/√Hz 15 nV/√Hz —	TLC2202BCD TLC2202ACD TLC2202CD	— — —	— — —	TLC2202BCP TLC2202ACP TLC2202CP	TLC2202Y
−40°C to 85°C	500 μV 500 μV 1 mV	30 nV/√Hz 35 nV/√Hz —	12 nV/√Hz 15 nV/√Hz —	TLC2202BID TLC2202AID TLC2202ID	— — —	— — —	TLC2202BIP TLC2202AIP TLC2202IP	—
−55°C to 125°C	500 μV 500 μV 1 mV	30 nV/√Hz 35 nV/√Hz —	12 nV/√Hz 15 nV/√Hz —	TLC2202BMD TLC2202AMD TLC2202MD	TLC2202BMFK TLC2202AMFK TLC2202MFK	TLC2202BMJG TLC2202AMJG TLC2202MJG	TLC2202BMP TLC2202AMP TLC2202MP	—

† The D packages are available taped and reeled. Add R suffix to device type (e.g. TLC220xBCDR).
‡ Chip forms are tested at 25°C only.

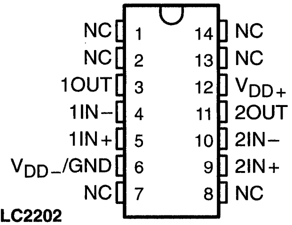
TLC2201
D, JG, OR P PACKAGE
(TOP VIEW)



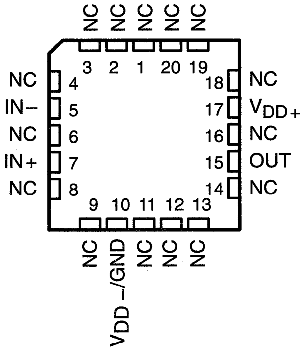
TLC2202
JG OR P PACKAGE
(TOP VIEW)



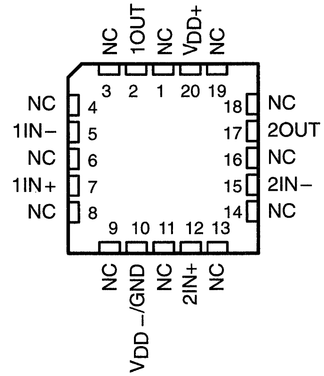
TLC2202
D PACKAGE
(TOP VIEW)



TLC2201
FK PACKAGE
(TOP VIEW)

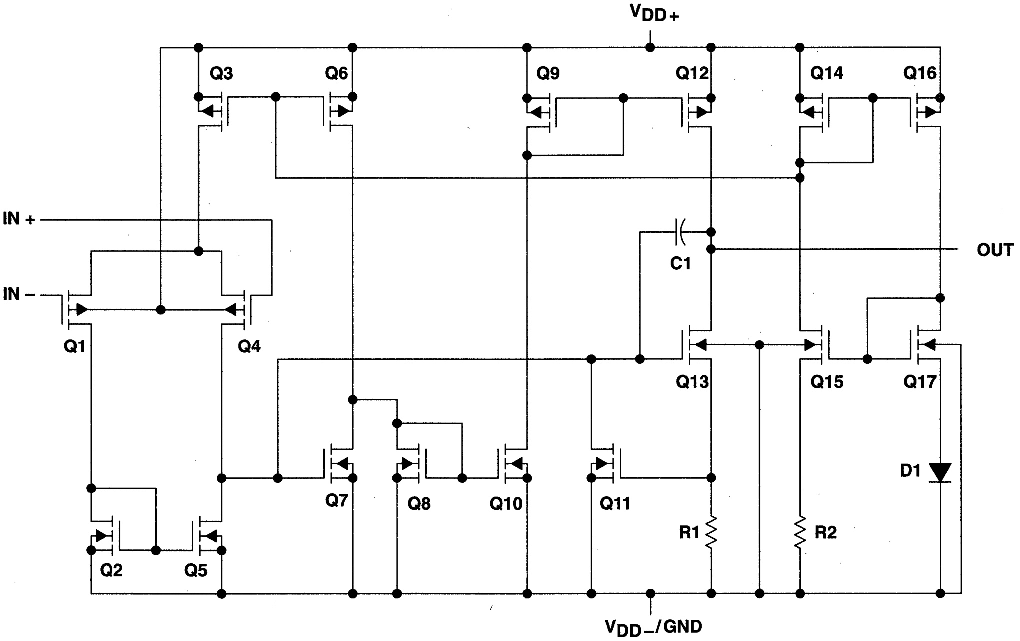


TLC2202
FK PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic (each amplifier)

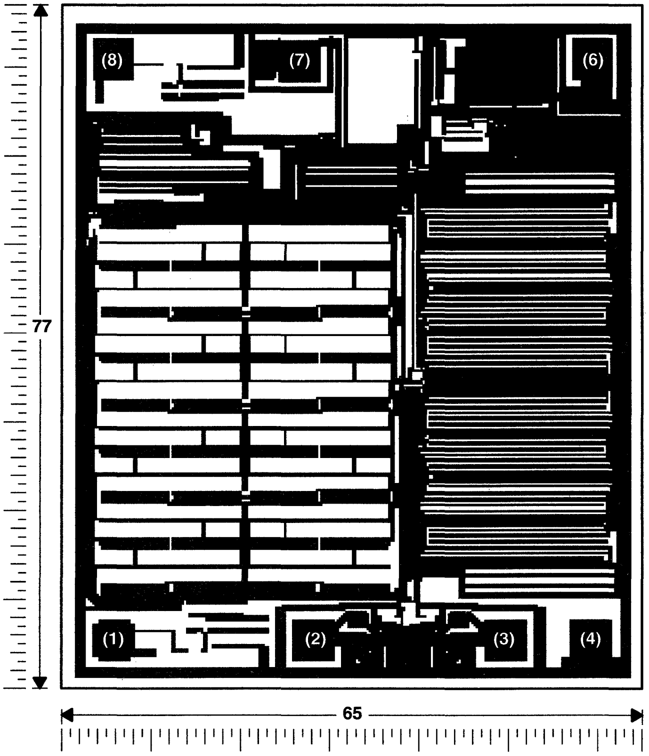


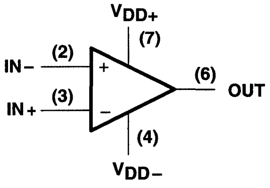
ACTUAL DEVICE COMPONENT COUNT		
COMPONENT	TLC2201	TLC2202
Transistors	17	34
Resistors	2	2
Diodes	1	4
Capacitors	1	2

TLC2201Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2201C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding path. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

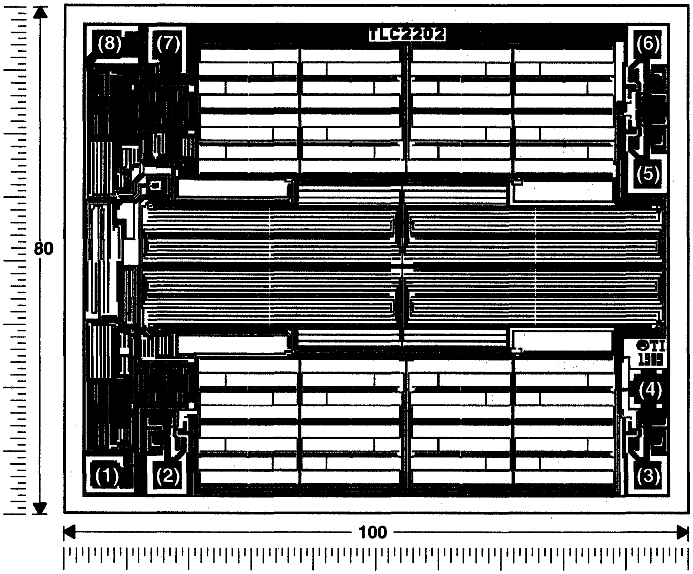
PIN (4) IS INTERNALLY CONNECTED TO BACK SIDE OF CHIP.

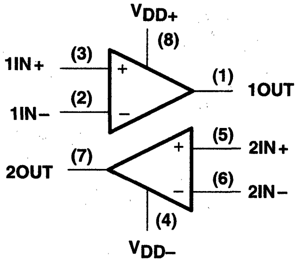
TERMINAL NUMBERS ARE FOR THE D, JG, AND P PACKAGES.

TLC2202Y chip formation

This chip, when properly assembled, displays characteristics similar to the TLC2202C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-}	−8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input)	±8 V
Input current, I_I (each input)	±5 mA
Output current, I_O (each output)	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values except differential voltages are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating in not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD}\pm$	±2.3	±8	±2.3	±8	±2.3	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-2.3$	V_{DD-}	$V_{DD+}-2.3$	V_{DD-}	$V_{DD+}-2.3$	V
Operating free-air temperature, T_A	0	70	−40	85	−55	125	°C

TLC2201C electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			600	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		V/mV
			Full range	300			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		
			Full range	70			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	Full range	85			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5	mA
			Full range			1.5	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150 °C extrapolated to T_A = 25 °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201C operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		V/µs
			Full range	1.5			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

† Full range is 0°C to 70°C.

TLC2201C electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			300			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		400	560		V/mV
			Full range	300			300			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		90	100		
			Full range	70			70			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150 °C extrapolated to T_A = 25 °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AC			TLC2210BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.7		2	2.7		V/µs
			Full range	1.5			1.5			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	30	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

† Full range is 0°C to 70°C.

NOTE 5: This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2201C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			600	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201C			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/μs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

† Full range is 0°C to 70°C.

TLC2201C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			300			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AC			TLC2210BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/µs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	30	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

† Full range is 0°C to 70°C.

NOTE 5: This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2202C electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	1000	µV
			Full range			1150	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		
			Full range	−4.7			V
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	300	560		V/mV
			Full range	200			
		V_O = ±4 V, R_L = 10 kΩ	25°C	50	100		
			Full range	25			
CMRR	Common-mode rejection ratio	V_O = 0, $V_{IC} = V_{ICR}\text{min}$, R_S = 50 Ω	25°C	80	115		dB
			Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.8	2.7	mA
			Full range			2.7	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202C operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202C			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.7		V/µs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

† Full range is 0°C to 70°C.

TLC2202C electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AC			TLC2202BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	500		80	500	μV
			Full range			650			650	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	μV/mo
I_{IO}	Input offset current	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$	25°C	300	560		300	560		V/mV
			Full range	200			200			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	50	100		50	100		
			Full range	25			25			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	115		80	115		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.8	2.7		1.8	2.7	mA
			Full range			2.7			2.7	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AC			TLC2202BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	1.8	2.7		1.8	2.7		V/μs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	30	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°			48°		

† Full range is 0°C to 70°C.

NOTE 5: This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2202C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	1000	μV
			Full range			1150	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	Full range			100	pA
I_{IB}	Input bias current		25°C		1		
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O =1 V to 4 V, R_L = 500 kΩ	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, $V_{IC} = V_{ICR}$min, R_S = 50 Ω	25°C	75	110		dB
			Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD}= 4.6 V to 16 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.7	2.6	mA
			Full range			2.6	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202C			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.6	2.5		V/μs
			Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		47°		

† Full range is 0°C to 70°C.

TLC2202C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AC			TLC2202BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	500		80	500	µV
			Full range			650			650	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, V_O = 0, R_S = 50 Ω	25°C	75	110		75	110		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.7	2.6		1.7	2.6	mA
			Full range			2.6			2.6	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AC			TLC2202BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.6	2.5		1.6	2.5		V/µs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	30	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		47°			47°		

† Full range is 0°C to 70°C.

NOTE 5: This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2201I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	500	µV
			Full range			650	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			150	
I_{IB}	Input bias current		25°C		1		pA
			Full range			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 500\ k\Omega$	25°C	400	560		V/mV
			Full range	250			
		$V_O = \pm4$ V, $R_L = 10\ k\Omega$	25°C	90	100		
			Full range	65			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.3$ V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5	mA
			Full range			1.5	

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$ °C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201I			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	2	2.7		V/µs
			Full range	1.4			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°		

† Full range is −40°C to 85°C.

TLC2201I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AI			TLC2210BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	200		80	200	µV
			Full range			350			350	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$	25°C	400	560		400	560		V/mV
			Full range	250			250			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	90	100		90	100		
			Full range	65			65			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$ °C extrapolated to $T_A = 25$°C using the Arrhenius equation assuming an activation energy of 0.96 eV.

TLC2201I operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AI			TLC2210BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		2	2.7		V/μs
			Full range	1.4			1.4			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	30	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

† Full range is –40°C to 85°C.

NOTE 5: This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2201I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			650	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			150	
I_{IB}	Input bias current		25°C		1		pA
			Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

† Full range is –40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201I			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ,, C_L = 100 pF	25°C	1.8	2.5		V/µs
			Full range	1.2			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

† Full range is –40°C to 85°C.

TLC2201I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µA
			Full range			350			350	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AI			TLC2210BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/μs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	30	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

† Full range is −40°C to 85°C.

NOTE 5: This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2202I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	1000	µV
			Full range			1200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current	$V_{IC} = 0$, $R_S = 50\ \Omega$	Full range			150	pA
I_{IB}	Input bias current		25°C		1		
			Full range			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		
			Full range	−4.7			V
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$	25°C	300	560		V/mV
			Full range	150			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	50	100		
			Full range	25			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}\text{min}$, $R_S = 50\ \Omega$	25°C	80	115		dB
			Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = \pm 2.3$ V to ± 8 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.8	2.7	mA
			Full range			2.7	

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202I			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	1.8	2.7		V/µs
			Full range	1.2			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°		

† Full range is −40°C to 85°C.

TLC2202I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AI			TLC2202BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	500		80	500	µV
			Full range			700			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 500\ k\Omega$	25°C	300	560		300	560		V/mV
			Full range	150			150			
		$V_O = \pm4$ V, $R_L = 10\ k\Omega$	25°C	50	100		50	100		
			Full range	25			25			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	115		80	115		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ ±2.3 V to ±8 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.8	2.7		1.8	2.7	mA
			Full range			2.7			2.7	

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AI			TLC2202BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	1.8	2.7		1.8	2.7		V/µs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	30	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°			48°		

† Full range is −40°C to 85°C.

NOTE 5: This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2202I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	1000	µV
			Full range			1200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	Full range			150	pA
I_{IB}	Input bias current		25°C		1		
			Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O =1 V to 4 V, R_L = 500 kΩ	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, $V_{IC} = V_{ICR}$min, R_S = 50 Ω	25°C	75	110		dB
			Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD}= 4.6 V to 16 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.7	2.6	mA
			Full range			2.6	

† Full range is –40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202I			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.6	2.5		V/µs
			Full range	1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		47°		

† Full range is –40°C to 85°C.

TLC2202I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AI			TLC2202BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	500		80	500	µV
			Full range			700			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O =1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, V_O = 0, R_S = 50 Ω	25°C	75	110		75	110		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.7	2.6		1.7	2.6	mA
			Full range			2.6			2.6	

† Full range is −40°C to 85°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AI			TLC2202BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.6	2.5		1.6	2.5		V/µs
			Full range	1			1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	30	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		47°			47°		

† Full range is −40°C to 85°C

NOTE 5: This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2201M electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		V/mV
			Full range	200			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		
			Full range	45			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, V_O = 0, R_S = 50 Ω	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5	mA
			Full range			1.5	

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201M operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201M			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		V/µs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

† Full range is −55°C to 125°C.

TLC2201M electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AM			TLC2210BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	200		80	200	µV
			Full range			400			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 500\ k\Omega$	25°C	400	560		400	560		V/mV
			Full range	200			200			
		$V_O = \pm4$ V, $R_L = 10\ k\Omega$	25°C	90	100		90	100		
			Full range	45			45			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.3$ V to ±8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observable through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201M operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.7		2	2.7		V/μs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	30	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

† Full range is −55°C to 125°C.

NOTE 5: This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2201M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	500	µV
			Full range			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005*	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	$I_O = 0$	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	$V_O = 1$ V to 4 V, $R_L = 500\ k\Omega$	25°C	150	315		V/mV
			Full range	75			
		$V_O = 1$ V to 4 V, $R_L = 10\ k\Omega$	25°C	25	55		
			Full range	10			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = 4.6$ V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	$V_O = 2.5$ V, No load	25°C		1	1.5	mA
			Full range			1.5	

*On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201M			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 0.5$ V to 2.5 V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	1.8	2.5		V/µs
			Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		45°		

† Full range is −55°C to 125°C.

TLC2201M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AM			TLC2210BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			400			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	V
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	75			75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	10			10			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

† Full range is –55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observable through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/µs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	30	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

† Full range is −55°C to 125°C.

NOTE 5: This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2202M electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	1000	µV
			Full range			1250	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005*	µV/mo
I_{IO}	Input offset current	$V_{IC} = 0$, $R_S = 50\ \Omega$	Full range			500	pA
I_{IB}	Input bias current		25°C		1		
			Full range			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		
			Full range	−4.7			V
A_{VD}	Large-signal differential voltage amplification	$V_O = 1$ V to 4 V, $R_L = 500\ k\Omega$	25°C	300	560		V/mV
			Full range	100			
		$V_O = 1$ V to 4 V, $R_L = 10\ k\Omega$	25°C	50	100		
			Full range	25			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}min$, $R_S = 50\ \Omega$	25°C	80	115		dB
			Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = \pm2.3$ V to ±8 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.8	2.7	mA
			Full range			2.7	

* On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202M operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202M			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	1.8	2.7		V/µs
			Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°		

† Full range is −55°C to 125°C.

TLC2202M electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AM			TLC2202BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	500		80	500	µV
			Full range			750			750	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005*		0.001	0.005*	µV/mo
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 4 V, R_L = 500 kΩ	25°C	300	560		300	560		V/mV
			Full range	100			100			
		V_O = ± 4 V, R_L = 10 kΩ	25°C	50	100		50	100		
			Full range	25			25			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	80	115		80	115		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.8	2.7		1.8	2.7	mA
			Full range			2.7			2.7	

*On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202M operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AM			TLC2202BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	1.8	2.7		1.8	2.7		V/µs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35*		18	30*	nV/√Hz
		f = 1 kHz	25°C		8	15*		8	12*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

*On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.

† Full range is −55°C to 125°C.

NOTE 5: This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2202M electrical characteristics at specified free-air temperatures, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	1000	µV
			Full range			1250	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005*	µV/mo
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	Full range			500	pA
I_{IB}	Input bias current		25°C		1		
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		V/mV
			Full range	75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	10			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	75	110		dB
			Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.7	2.6	mA
			Full range			2.6	

*On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202M			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.6	2.5		V/µs
			Full range	0.9			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		47°		

† Full range is −55°C to 125°C.

TLC2202M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AM			TLC2202BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	500		80	500	µV
			Full range			750			750	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005*		0.001	0.005*	µV/mo
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	75			75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	10			10			
CMRR	Common-mode rejection ratio	V_O = 0, $V_{IC} = V_{ICR}$min, R_S = 50 Ω	25°C	75	110		75	110		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.7	2.6		1.7	2.6	mA
			Full range			2.6			2.6	

*On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.

† Full range is −55°C to 125°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2202AM			TLC2202BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.6	2.5		1.6	2.5		V/μs
			Full range	0.9			1.1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35*		18	30*	nV/√Hz
		f = 1 kHz	25°C		8	15*		8	12*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		47°			47°		

* On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.

† Full range is −55°C to 125°C

NOTE 5: This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TLC2201Y electrical characteristics at $V_{DD\pm} = \pm5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2201Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$,	$R_S = 50\ \Omega$		100		µV
	Input offset voltage long-term drift (see Note 4)				0.001		µV/mo
I_{IO}	Input offset current				0.5		pA
I_{IB}	Input bias current				1		pA
V_{OH}	Maximum high-level output voltage	$R_L = 10\ k\Omega$			4.8		V
V_{OL}	Maximum low-level output voltage	$I_O = 0$			0		mV
A_{VD}	Large-signal differential voltage amplification	$V_O = 1$ V to 4 V,	$R_L = 500\ \Omega$		55		V/mV
		$V_O = 1$ V to 4 V,	$R_L = 10\ \Omega$		55		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	$V_O = 0$,		110		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = 4.6$ to 16 V			110		dB
I_{DD}	Supply current per amplifier	$V_O = 2.5$ V,	No load		1		mA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2201Y operating characteristics at $V_{DD\pm} = \pm 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TLC2201Y			UNIT
			MIN	TYP	MAX	
SR	Positive slew rate at unity gain	$V_O = \pm0.5$ to 2.5 V, $R_L = 10\ k\Omega$, $C_L = 100$ pF		2.5		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		18		nV/√Hz
		f = 1 kHz		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.5		µV
		f = 0.1 to 10 Hz		0.7		
I_n	Equivalent input noise current			0.6		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF		1.8		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF		48°		

TLC2202Y electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2202Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		100		µV
	Input offset voltage long-term drift (see Note 4)				0.001		µV/mo
I_{IO}	Input offset current				0.5		pA
I_{IB}	Input bias current				1		pA
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ			4.8		V
V_{OL}	Maximum low-level output voltage	I_O = 0			0		mV
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V,	R_L = 500 Ω		315		V/mV
		V_O = 1 V to 4 V,	R_L = 10 Ω		55		
CMRR	Common-mode rejection ratio	V_O = 0, V_{ICR}min,	R_S = 50 Ω		110		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DCC}/\Delta V_{IO}$)	V_{DD} = 4.6 to 16 V			110		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		1.7		mA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2202Y operating characteristics at V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC2202Y			UNIT
				MIN	TYP	MAX	
SR	Positive slew rate at unity gain	V_O = 0.5 V to 2.5 V, C_L = 100 pF	R_L = 10 kΩ,		2.5		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			18		nV/√Hz
		f = 10 kHz			8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			0.5		µV
		f = 0.1 to 10 Hz			0.7		
I_n	Equivalent input noise current				0.6		pA/√Hz
B_1	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 10 kΩ,		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 100 pF		47°		

PARAMETER MEASUREMENT INFORMATION

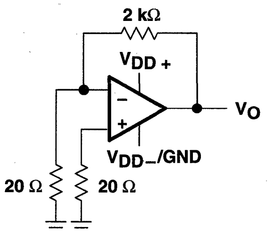
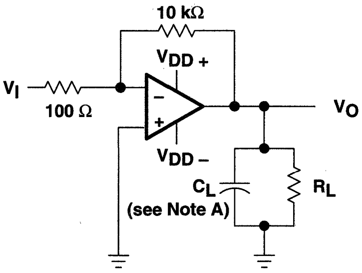
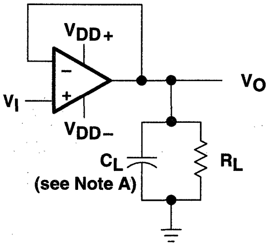


Figure 1. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 2. Phase-Margin Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Slew-Rate Test Circuit

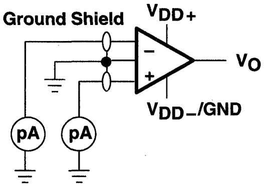


Figure 4. Input-Bias and Offset-Current Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level of the TLC220x, TLC220xA, and TLC220xB, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket, and a second test measuring both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Texas Instruments offers automated production noise testing to meet individual application requirements. Noise voltage at f = 10 Hz and f = 1 kHz is 100% tested on every TLC2201B device, while lot sample testing is performed on the TLC220xA. For other noise requirements, please contact the factory.

TYPICAL CHARACTERISTICS

Table of Graphs

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I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	7 8
V_{OM}	Maximum peak output voltage	vs Output current vs Free-air temperature	9 10
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	11
V_{OH}	High-level output voltage	vs Frequency vs High-level output current vs Free-air temperature	12 13 14
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	15 16
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	17 18
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	19 20
CMRR	Common-mode rejection ratio	vs Frequency	21
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	22 23, 24
	Pulse response	Small signal Large signal	25, 26 27, 28
SR	Slew rate	vs Supply voltage vs Free-air temperature	29 30
	Noise voltage (referred to input)	0.1 to 1 Hz 0.1 to 10 Hz	31 32
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	33, 34 35
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature	36, 37 38, 39
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2201
INPUT OFFSET VOLTAGE

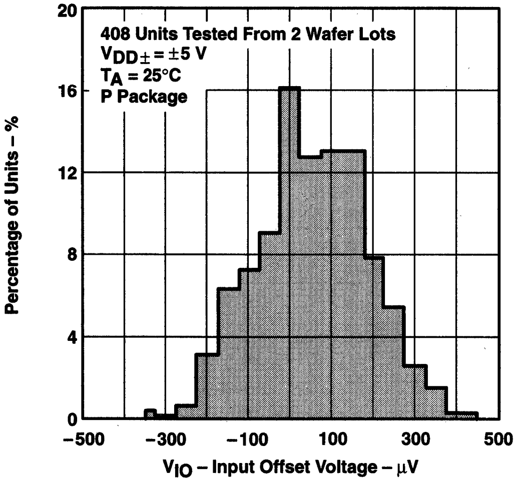

Figure 5

TLC2202
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

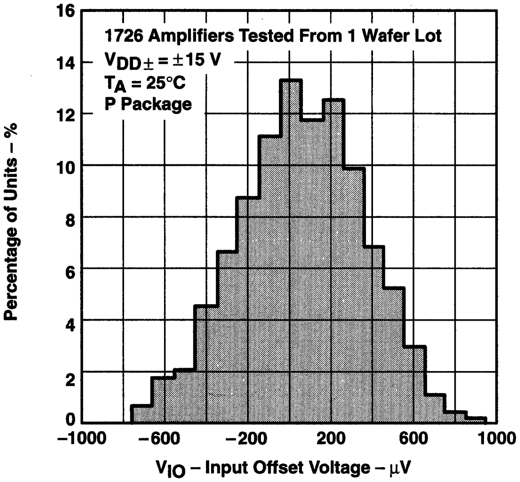

Figure 6

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

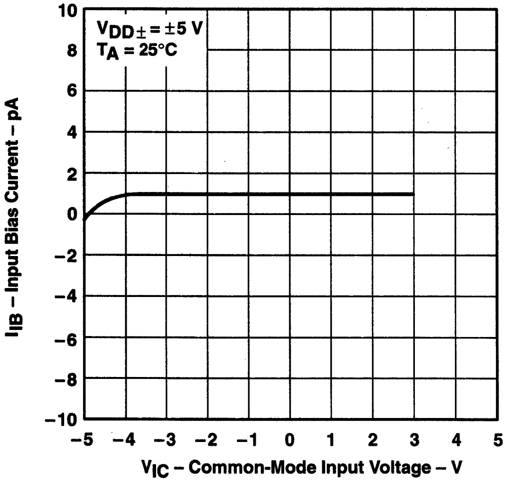

Figure 7

INPUT BIAS CURRENT†
vs
FREE-AIR TEMPERATURE

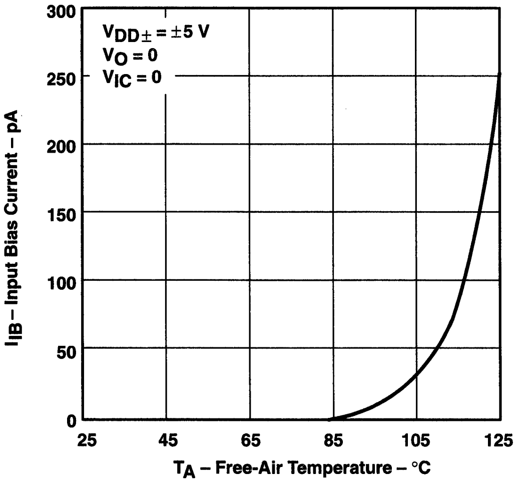

Figure 8

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

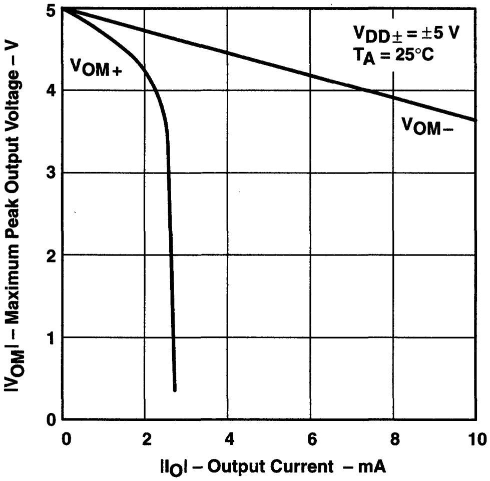

Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE

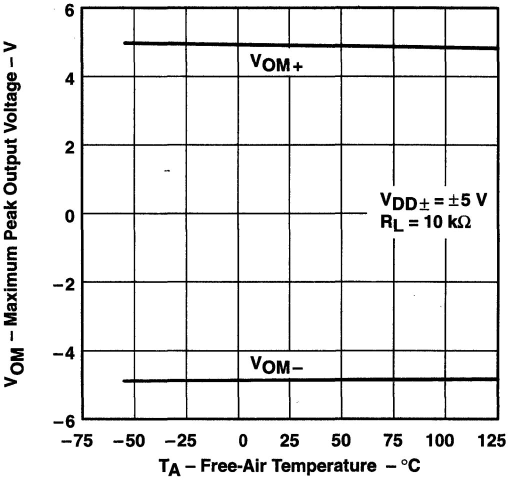

Figure 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE† vs FREQUENCY

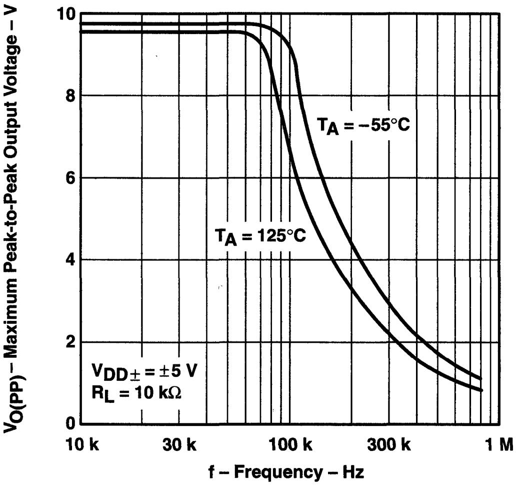

Figure 11

HIGH-LEVEL OUTPUT VOLTAGE† vs FREQUENCY

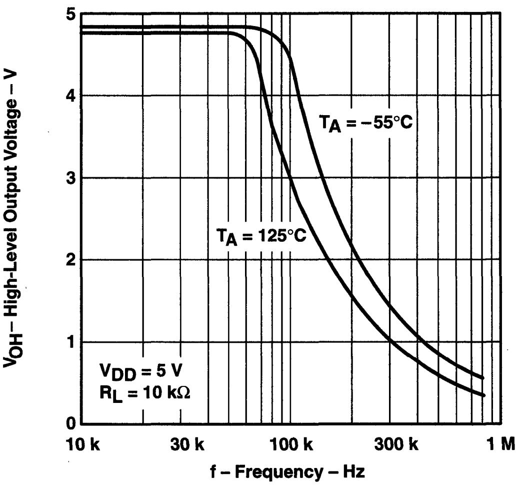

Figure 12

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

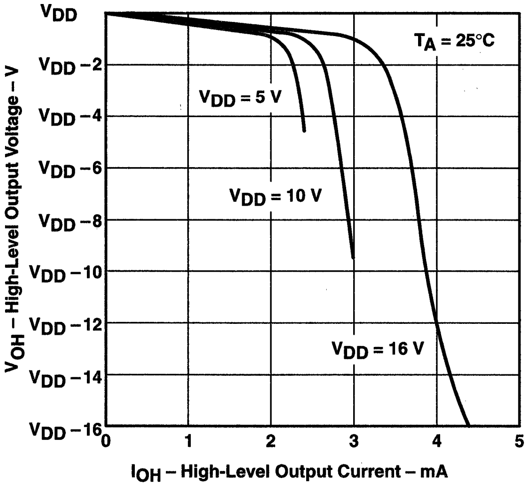

Figure 13

HIGH-LEVEL OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE

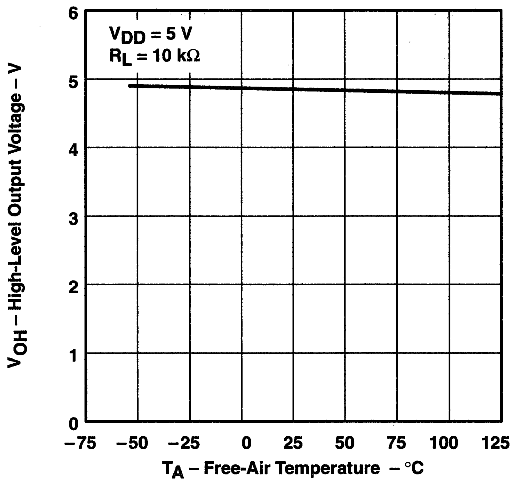

Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

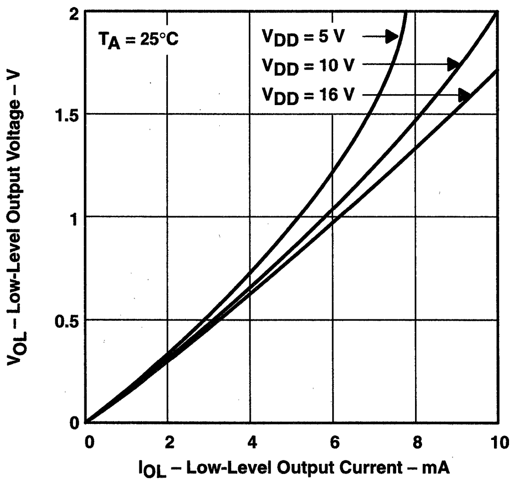

Figure 15

LOW-LEVEL OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE

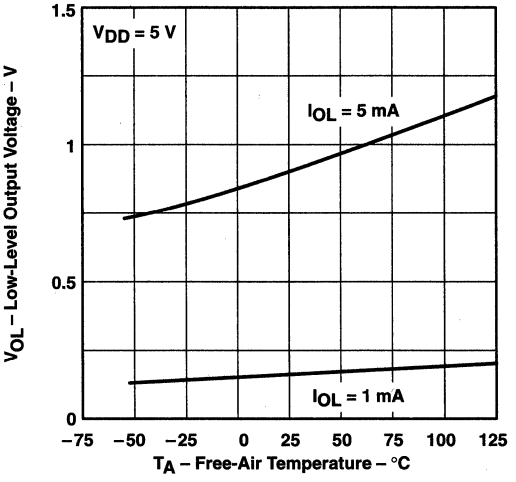

Figure 16

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

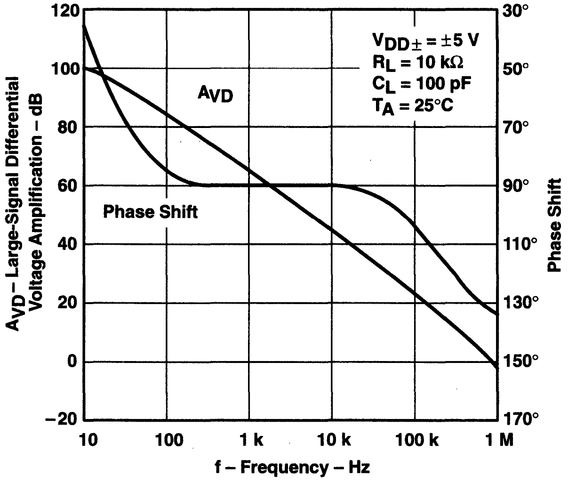

Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

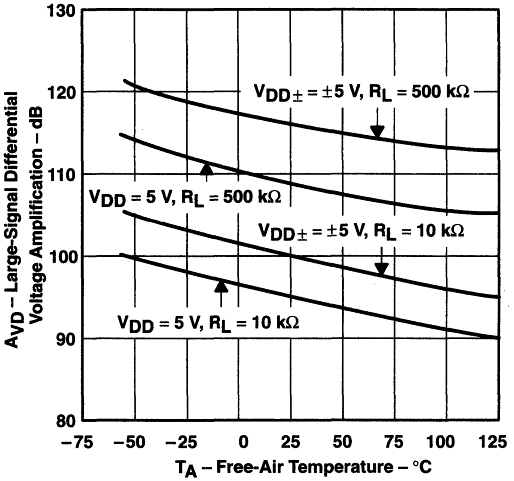

Figure 18

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

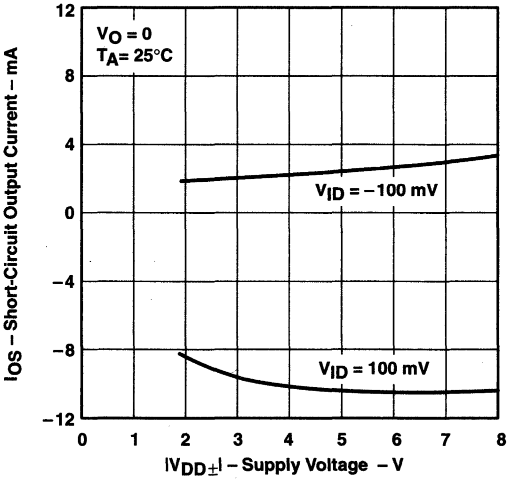

Figure 19

SHORT-CIRCUIT OUTPUT CURRENT† vs FREE-AIR TEMPERATURE

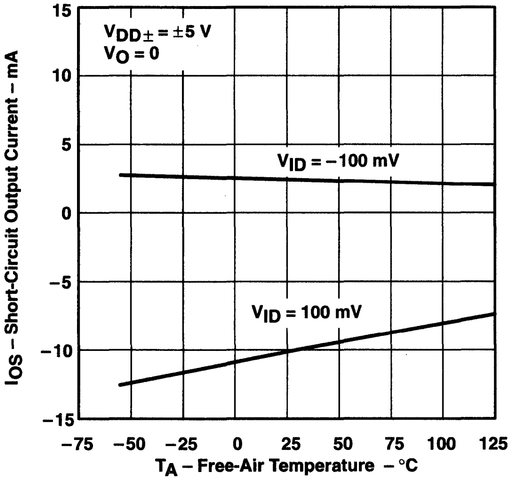

Figure 20

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

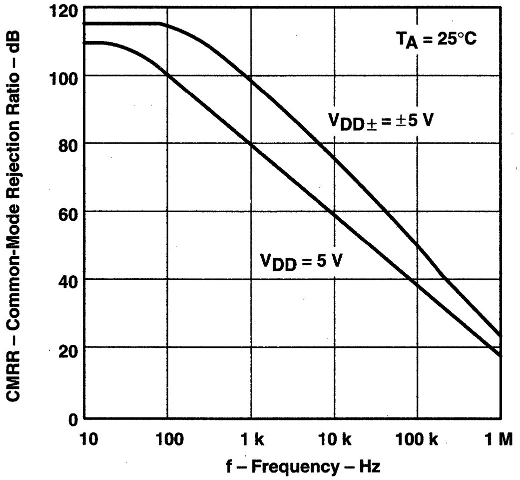

Figure 21

SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

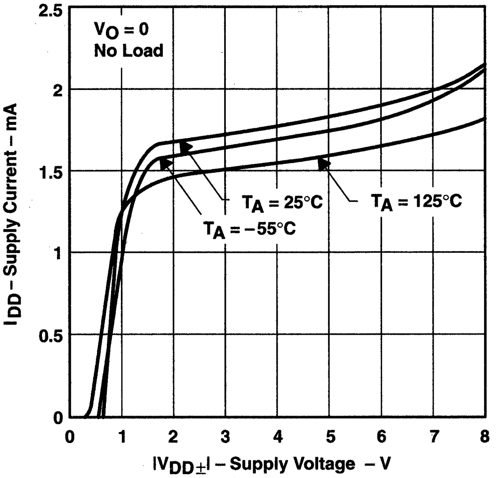

Figure 22

TLC2201
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

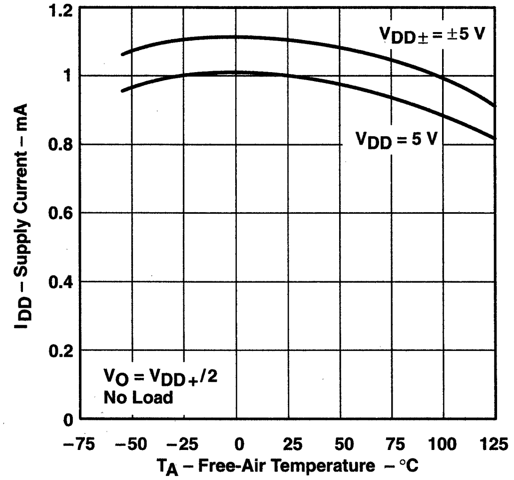

Figure 23

TLC2202
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

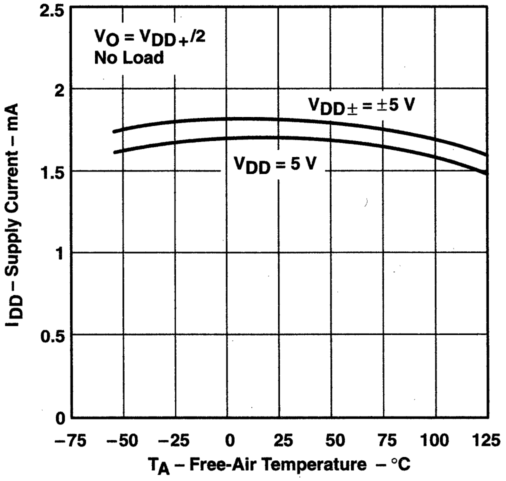

Figure 24

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

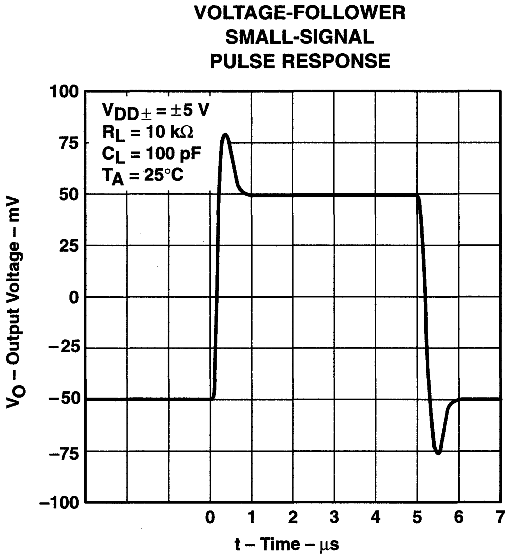

Figure 25

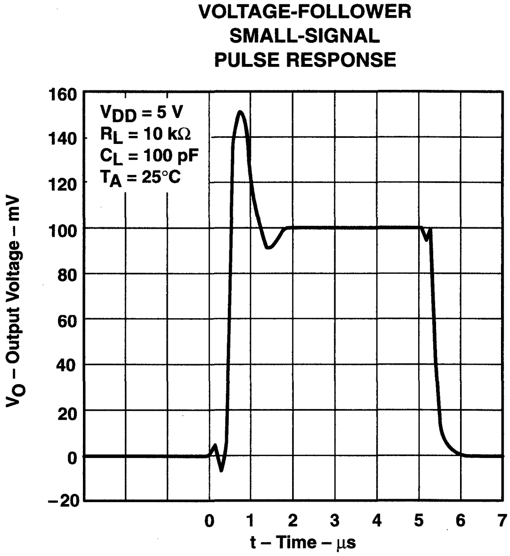

Figure 26

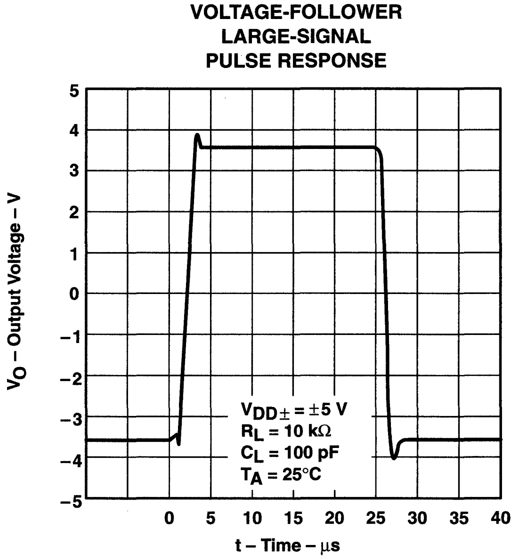

Figure 27

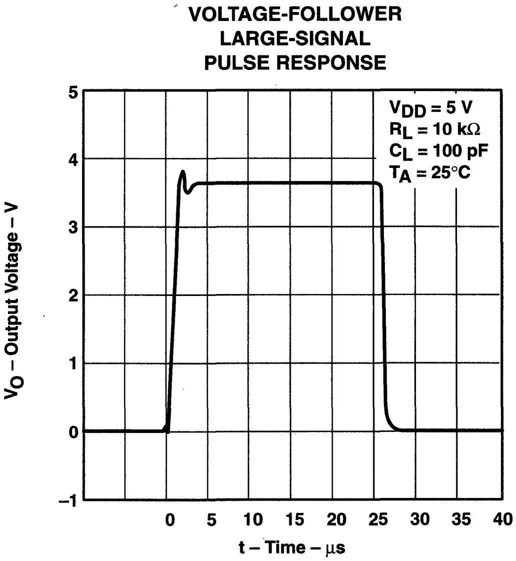

Figure 28

TYPICAL CHARACTERISTICS

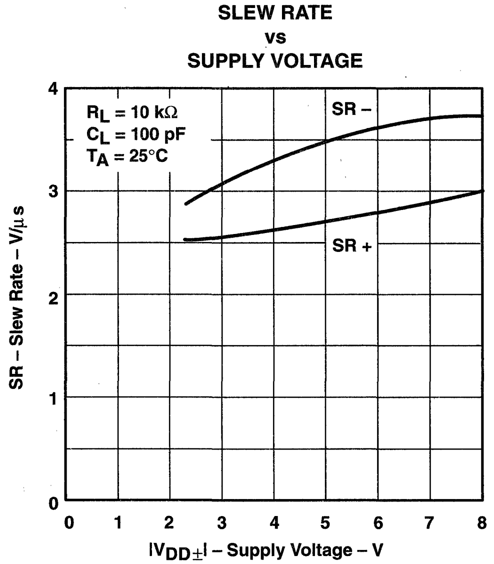

Figure 29

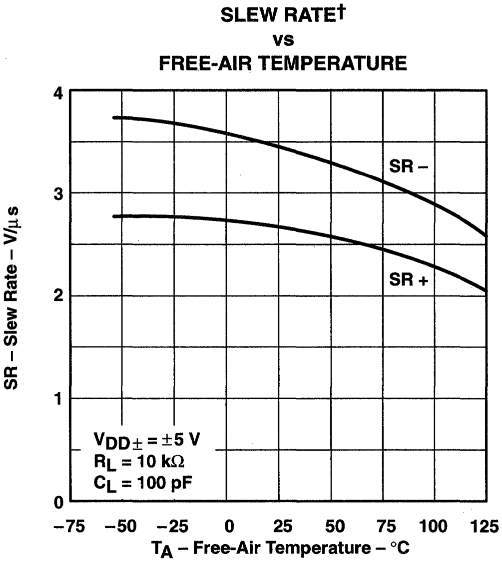

Figure 30

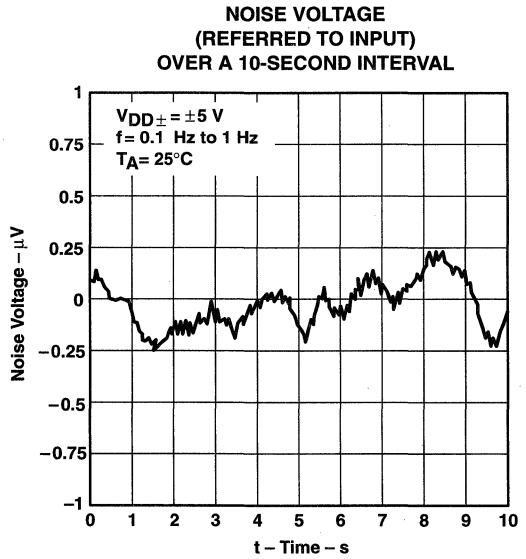

Figure 31

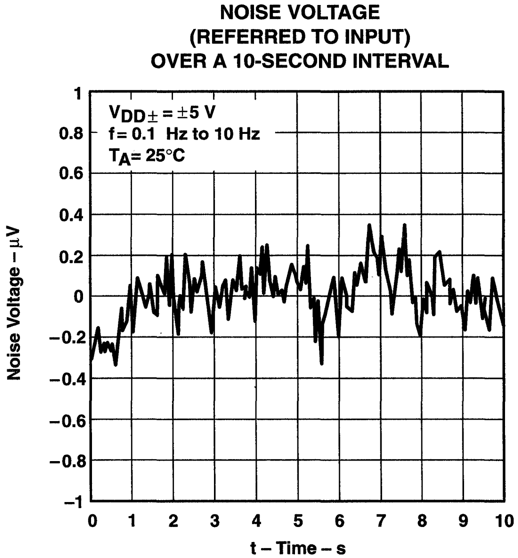

Figure 32

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TLC2201
GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

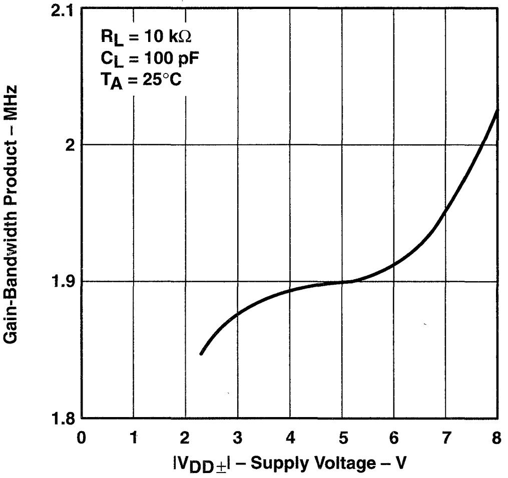

Figure 33

TLC2202
GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

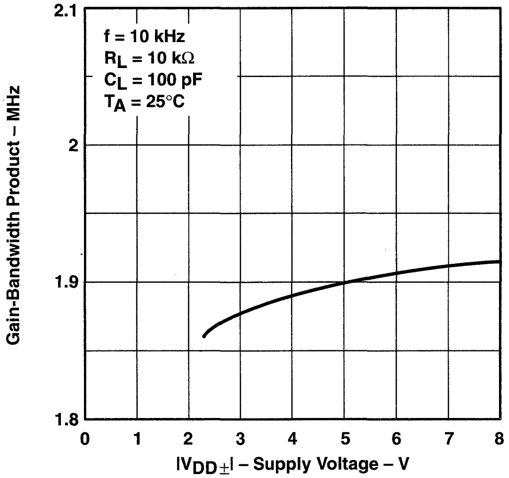

Figure 34

GAIN-BANDWIDTH PRODUCT†
vs
FREE-AIR TEMPERATURE

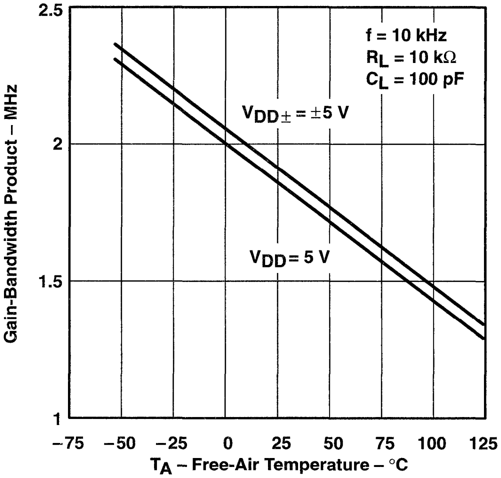

Figure 35

TLC2201
PHASE MARGIN
vs
SUPPLY VOLTAGE

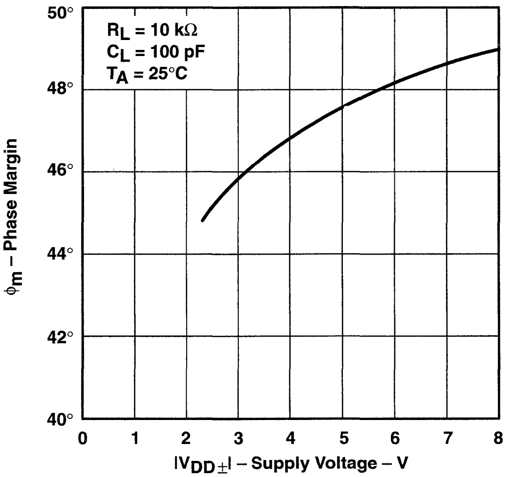

Figure 36

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TLC2202
PHASE MARGIN
vs
SUPPLY VOLTAGE

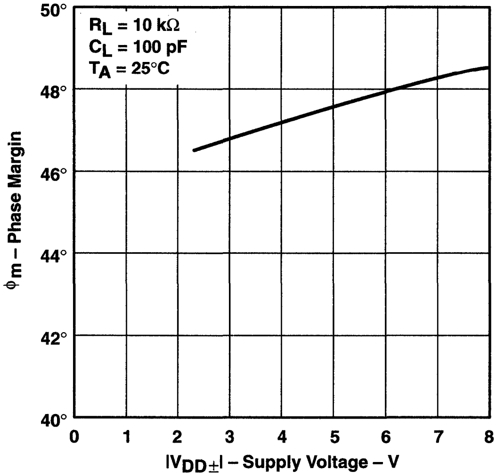

Figure 37

TLC2201
PHASE MARGIN†
vs
FREE-AIR TEMPERATURE

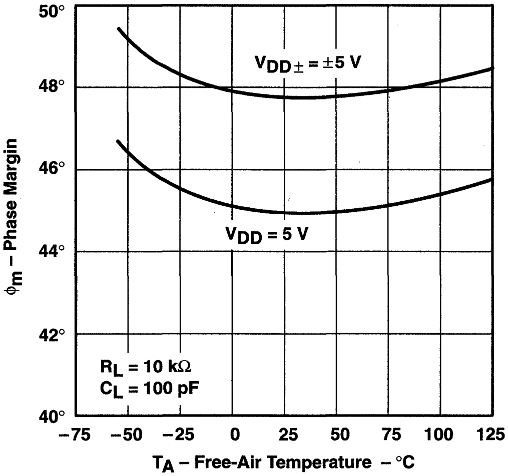

Figure 38

TLC2202
PHASE MARGIN†
vs
FREE-AIR TEMPERATURE

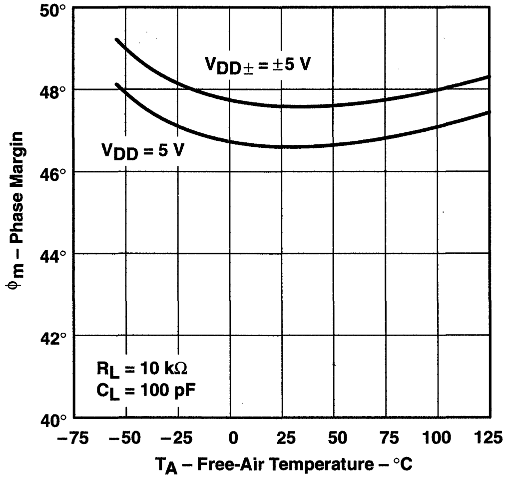

Figure 39

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

latch-up avoidance

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC220x, TLC220xA, and TLC220xB inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques reducing the chance of latch-up should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

electrostatic discharge protection

These devices use internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 40 were generated using the TLC220x typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).

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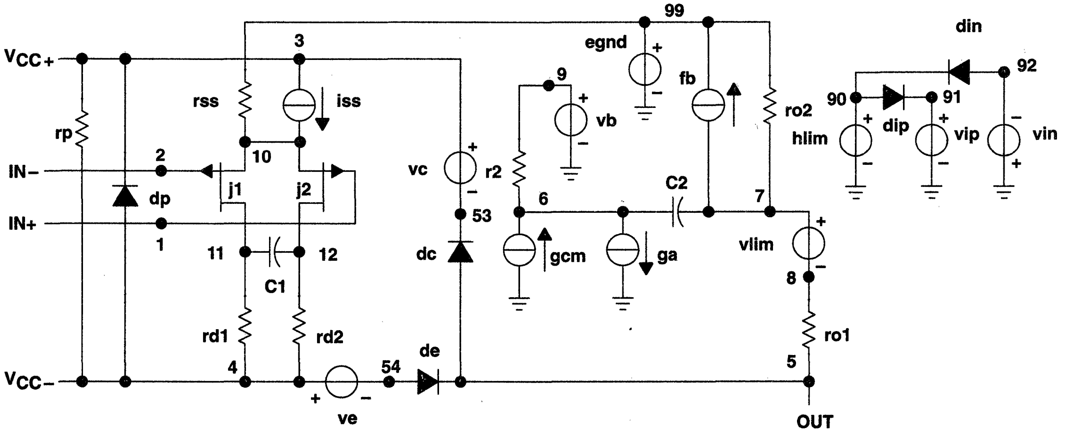
APPLICATION INFORMATION

macromodel information (continued)



```
.subckt TLC220x  1 2 3 4 5
*
  c1   1   12 8.51E-12
  c2   6   7  50.00E-12
  cpsr 85  86 79.6E-9
  dcm+ 81  82 dx
  dcm- 83  81 dx
  dc   5   53 dx
  de   54  5  dx
  dlp  90  91 dx
  dln  92  90 dx
  dp   4   3  dx
  ecmr 84  99 (2,99) 1
  egnd 99  0  poly(2) (3,0) (4,0) 0 .5 .5
  epsr 85  0  poly(1) (3,4) -200E-6 20E-6
  ense 89  2  poly(1) (88,0) 100E-6 1
  fb   7   99 poly(6) vb vc ve vlp vln
+  vpsr 0 +    895.9E3 -90E3 90E3 90E3 -90E3 895E3
  ga   6   0  11 12 314.2E-6
  gcm  0   6  10 99 1.295E-9
  gpsr 85  86 (85,86) 100E-6
  grd1 60  11 (60,11) 3.141E-4
  grd2 60  12 (60,12) 3.141E-4
  hlim 90  0  vlim 1k
  hcmr 80  1  poly(2) vcm+ vcm- 0 1E2 1E2
  irp  3   4  965E-6
```

```
  iss  3   10 dc 135.0E-6
  iio  2   0  .5E-12
  i1   88  0  1E-21
  j1   11  89 10 jx
  j2   12  80 10 jx
  r2   6   9  100.0E3
  rcm  84  81 1k
  rn1  88  0  1500
  ro1  8   5  188
  ro2  7   99 187
  rss  10  99 1.481E6
  vad  60  4  -.3v
  vcm+ 82  99 2.2
  vcm- 83  99 -4.5
  vb   9   0  dc 0
  vc   3   53 dc .9
  ve   54  4  dc .8
  vlim 7   8  dc 0
  vlp  91  0  dc 2.8
  vln  0   92 dc 2.8
  vpsr 0   86 dc 0
.model dx  d(is=800.0E-18)
.model jx pjf(is=500.0E-15 beta=1.462E-3
+ vto=-.155 kf=1E-17)
.endsx
```

Figure 40. Boyle Macromodel and Subcircuit

TLC225x, TLC225xA, TLC225xY
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176 – FEBRUARY 1997

- **Output Swing includes Both Supply Rails**
- **Low Noise . . . 19 nV/$\sqrt{Hz}$ Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Very Low Power . . . 35 µA Per Channel Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 850 µV Max at T_A = 25°C (TLC225xA)**
- **Macromodel Included**
- **Performance Upgrades for the TS27L2/L4 and TLC27L2/L4**

description

The TLC2252 and TLC2254 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC225x family consumes only 35 µA of supply current per channel. This micropower operation makes them good choices for battery-powered applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Looking at Figure 1, the TLC225x has a noise level of 19 nV/$\sqrt{Hz}$ at 1kHz; four times lower than competitive micropower solutions.

The TLC225x amplifiers, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC225xA family is available and has a maximum input offset voltage of 850 µV. This family is fully characterized at 5 V and ±5 V.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

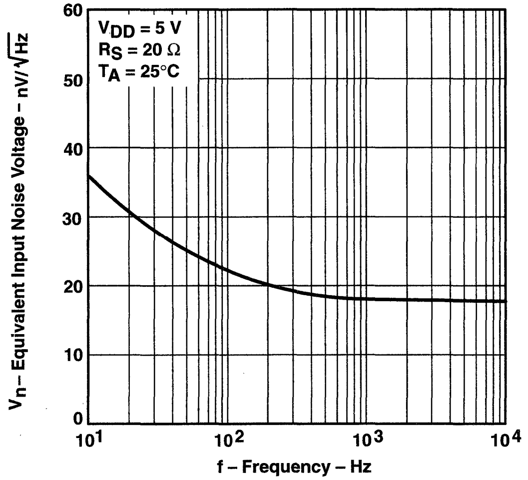


Figure 1

The TLC2252/4 also makes great upgrades to the TLC27L2/L4 or TS27L2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage ranges, see the TLV2432 and TLV2442 devices. If the design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

TLC2252 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES						CHIP FORM§ (Y)
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLATPACK (U)	
0°C to 70°C	1500 μV	TLC2252CD	—	—	TLC2252CP	TLC2252CPWLE	—	TLC2252Y
–40°C to 85°C	850 μV 1500 μV	TLC2252AID TLC2252ID	— —	— —	TLC2252AIP TLC2252IP	TLC2252AIPWLE —	— —	
–55°C to 125°C	850 μV 1500 μV	— —	TLC2252AMFK TLC2252MFK	TLC2252AMJG TLC2252MJG	— —	— —	TLC2252AMU TLC2252MU	

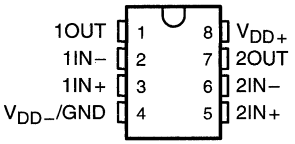
† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2262CDR).
‡ The PW package is available only left-ended taped and reeled.
§ Chip forms are tested at 25°C only.

TLC2254 AVAILABLE OPTIONS

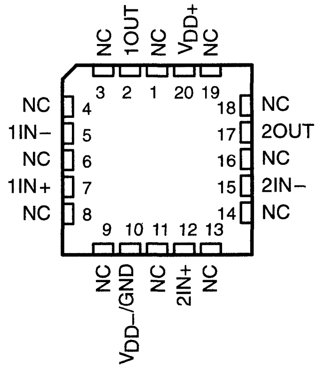
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES						CHIP FORM§ (Y)
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP‡ (PW)	CERAMIC FLATPACK (W)	
0°C to 70°C	1500 μV	TLC2254CD	—	—	TLC2254CN	TLC2254CPWLE	—	TLC2254Y
–40°C to 125°C	850 μV 1500 μV	TLC2254AID TLC2254ID	— —	— —	TLC2254AIN TLC2254IN	TLC2254AIPWLE —	— —	—
–55°C to 125°C	850 μV 1500 μV	— —	TLC2254AMFK TLC2254MFK	TLC2254AMJ TLC2254MJ	— —	— —	TLC2254AMW TLC2254MW	—

† The D packages are available taped and reeled. Add R suffix to the device type (e.g., TLC2254CDR).
‡ The PW package is available only left-end taped and reeled. Chips are tested at 25°C.
§ Chip forms are tested at 25°C only.

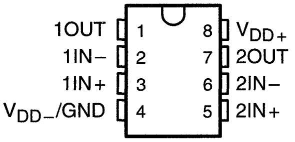
TLC2252C, TLC2252AC
TLC2252I, TLC2252AI
D, P, OR PW PACKAGE
(TOP VIEW)



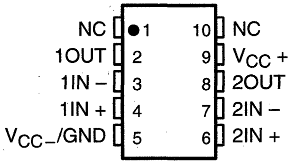
TLC2252M, TLC2252AM . . . FK PACKAGE
(TOP VIEW)



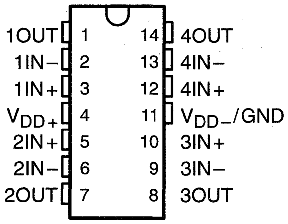
TLC2252M, TLC2252AM . . . JG PACKAGE
(TOP VIEW)



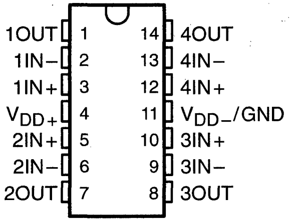
TLC2262M, TLC2252AM . . . U PACKAGE
(TOP VIEW)



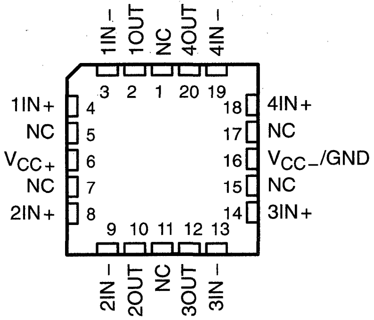
TLC2254C, TLC2254AC
TLC2254I, TLC2254AI
D, N, OR PW PACKAGE
(TOP VIEW)



TLC2254M, TLC2254AM
J OR W PACKAGE
(TOP VIEW)



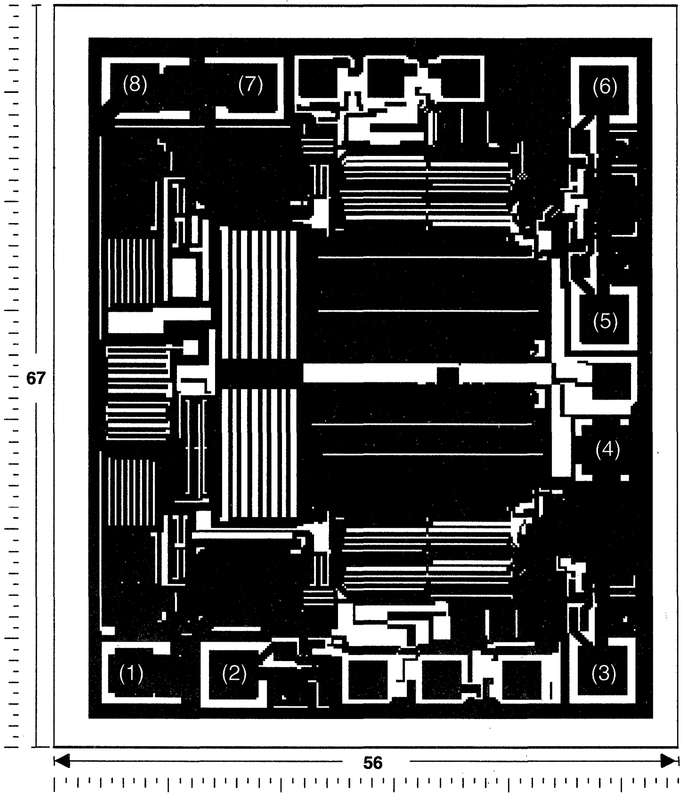
TLC2254M, TLC2254AM
FK PACKAGE
(TOP VIEW)

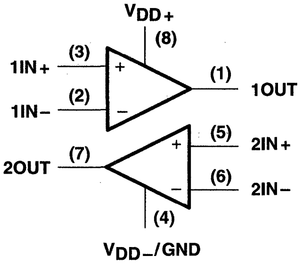


TLC2252Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2252C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

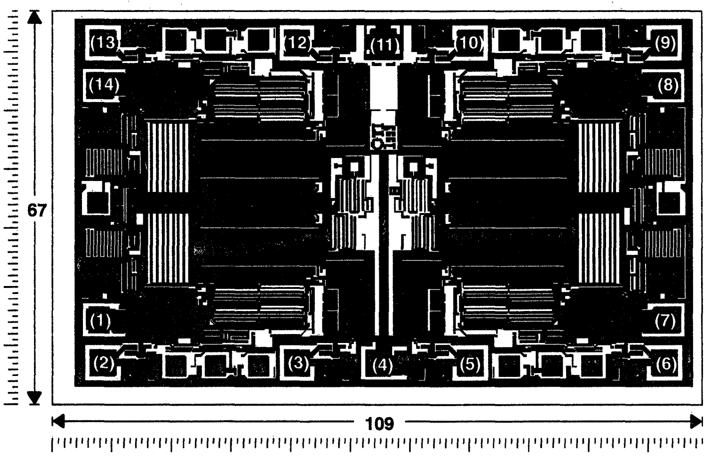
ALL DIMENSIONS ARE IN MILS.

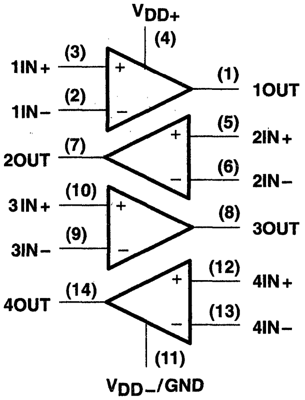
TERMINAL (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TLC2254Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2254C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

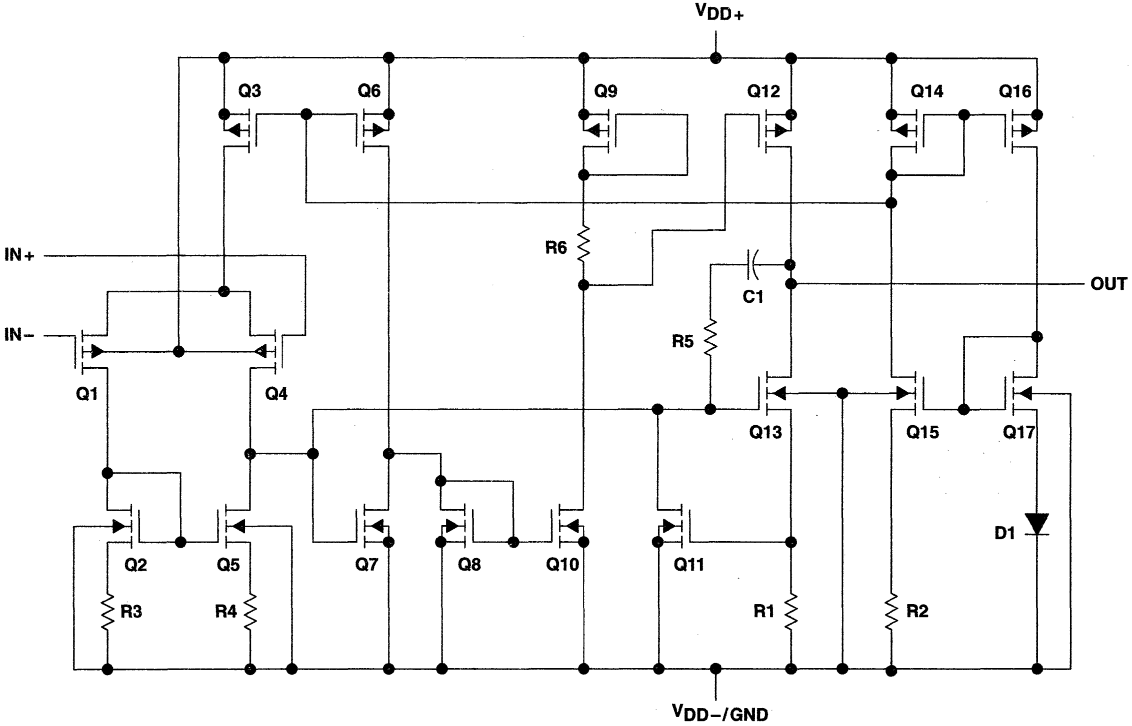
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2252	TLC2254
Transistors	38	76
Resistors	30	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	±8 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	–40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current flows when input is brought below V_{DD-} – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D–8	724 mW	5.8 mW/°C	464 mW	377 mW	—
D–14	950 mW	7.6 mW/°C	608 mW	450 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	736 mW	—
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—
PW–8	525 mW	4.2 mW/°C	336 mW	273 mW	—
PW–14	700 mW	5.6 mW/°C	448 mW	448 mW	—
U	700 mW	5.5 mW/°C	246 mW	330 mW	150 mW
W	700 mW	5.5 mW/°C	246 mW	330 mW	150 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V
Operating free-air temperature, T_A	0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2252C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	V_{DD}± = ±2.5 V, R_S = 50 Ω	25°C		200	1500	µV
				Full range			1750	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	|V_{IO}| ≤ 5 mV	25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.98		V
		I_{OH} = −75 µA		25°C	4.9	4.94		
				Full range	4.8			
		I_{OH} = −150 µA		25°C	4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15	
				Full range			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3	
				Full range			0.3	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.7	1	
				Full range			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		V/mV
				Full range	10			
			R_L = 1 MΩ‡	25°C		1700		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		70	125	µA
				Full range			150	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, R_L = 100 kΩ‡, C_L = 100 pF‡		25°C	0.07	0.12		V/μs
				Full range	0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36		nV/√Hz
		f = 1 kHz		25°C		19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%		
			A_V = 10			1%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°		
	Gain margin			25°C		15		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A†	TLC2252C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		200	1500	µV
			Full range			1750	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert \le 5$ mV, $R_S = 50\ \Omega$	25°C	−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.98		V
		$I_O = -100\ \mu A$	25°C	4.9	4.93		
			Full range	4.7			
		$I_O = -200\ \mu A$	25°C	4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		
			Full range	−4.85			
		$V_{IC} = 0$, $I_O = 1$ mA	25°C	−4.7	−4.8		
			Full range	−4.7			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		
			Full range	−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 100\ k\Omega$	25°C	45	650		V/mV
			Full range	10			
		$V_O = \pm 4$ V, $R_L = 1\ M\Omega$	25°C		3000		
r_{id}	Differential input resistance		25°C		10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 25 kHz, $A_V = 10$	25°C		190		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		dB
			Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = 2.2$ V to ±8 V, $V_{IC} = 0$, No load	25°C	80	95		dB
			Full range	80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		80	125	µA
			Full range			150	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±1.9 V, C_L = 100 pF	R_L = 100 kΩ,	25°C	0.07	0.12		V/μs
				Full range	0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		38		nV/√Hz
		f = 1 kHz		25°C		19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion pulse duration	V_O = ±2.3 V, f = 10 kHz, R_L = 50 kΩ	A_V = 1	25°C		0.2%		
			A_V = 10			1%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.21		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		14		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		63°		
	Gain margin			25°C		15		dB

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2254C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD\pm}$ = ±2.5 V, V_O = 0, R_S = 50 Ω	25°C		200	1500	µV
			Full range			1750	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA	25°C		4.98		V
		I_{OH} = −75 µA	25°C	4.9	4.94		
			Full range	4.8			
		I_{OH} = −150 µA	25°C	4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 µA	25°C		0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		0.09	0.15	
			Full range			0.15	
		V_{IC} = 2.5 V, I_{OL} = 1 mA	25°C		0.2	0.3	
			Full range			0.3	
		V_{IC} = 2.5 V, I_{OL} = 4 mA	25°C		0.7	1	
			Full range			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 100 kΩ‡	25°C	100	350		V/mV
			Full range	10			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ‡	25°C		1700		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10	25°C		200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		dB
			Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		dB
			Full range	80			
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, No load	25°C		140	250	µA
			Full range			300	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2254C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 100 kΩ‡,	25°C	0.07	0.12		V/μs
				Full range	0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36		nV/√Hz
		f = 1 kHz		25°C		19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%		
			A_V = 10			1%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°		
	Gain margin			25°C		15		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		T_A†	TLC2254C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		200	1500	µV
				Full range			1750	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert$ ≤5 mV, R_S = 50 Ω		25°C	−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.98		V
		I_O = −100 µA		25°C	4.9	4.93		
				Full range	4.7			
		I_O = −200 µA		25°C	4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0,	I_O = 50 µA	25°C		−4.99		V
		V_{IC} = 0,	I_O = 500 µA	25°C	−4.85	−4.91		
				Full range	−4.85			
		V_{IC} = 0,	I_O = 1 mA	25°C	−4.7	−4.8		
				Full range	−4.7			
		V_{IC} = 0,	I_O = 4 mA	25°C	−4	−4.3		
				Full range	−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 100 kΩ	25°C	40	150		V/mV
				Full range	10			
			R_L = 1 MΩ	25°C		3000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		190		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0,	R_S = 50 Ω	25°C	75	88		dB
				Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, V_{IC} = 0,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		160	250	µA
				Full range			300	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2254C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9$ V, $R_L = 100$ kΩ, $C_L = 100$ pF		25°C	0.07	0.12		V/µs
				Full range	0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		38		nV/√Hz
		f = 1 kHz		25°C		19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.1		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, f = 20 kHz, $R_L = 50$ kΩ	$A_V = 1$	25°C		0.2%		
			$A_V = 10$			1%		
	Gain-bandwidth product	f = 10 kHz, $R_L = 50$ kΩ, $C_L = 100$ pF		25°C		0.21		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $A_V = 1$, $R_L = 50$ kΩ, $C_L = 100$ pF		25°C		14		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ, $C_L = 100$ pF		25°C		63°		
	Gain margin			25°C		15		dB

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2252I			TLC2252AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0, V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	µV
			Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			1000			1000	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			1000			1000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA	25°C		4.98			4.98		V
		I_{OH} = −75 µA	25°C	4.9	4.94		4.9	4.94		
			Full range	4.8			4.8			
		I_{OH} = −150 µA	25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
			Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
			Full range	10			10			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ‡	25°C		1700			1700		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = $V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		70	125		70	125	µA
			Full range			150			150	

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, R_L = 100 kΩ‡, C_L = 100 pF‡		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, R_L = 50 kΩ‡,	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2252I			TLC2252AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		200	1500		200	850	µV
			Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			1000			1000	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			1000			1000	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \leq 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.98			4.98		V
		$I_O = -100\ \mu A$	25°C	4.9	4.93		4.9	4.93		
			Full range	4.7			4.7			
		$I_O = -200\ \mu A$	25°C	4.8	4.86		4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 50$ kΩ	25°C	40	150		40	150		V/mV
			Full range	10			10			
		$V_O = \pm 4$ V, $R_L = 1$ MΩ	25°C		3000			3000		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, $A_V = 10$	25°C		190			190		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5$ V, No load	25°C		80	125		80	125	µA
			Full range			150			150	

† Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2252I			TLC2252AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±1.9 V, R_L = 100 kΩ, C_L = 100 pF	25°C	0.07	0.12		0.07	0.12		V/μs
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		38			38		nV/√Hz
		f = 1 kHz	25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.8			0.8		μV
		f = 0.1 Hz to 10 Hz	25°C		1.1			1.1		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 50 kΩ, f = 10 kHz, A_V = 1	25°C		0.2%			0.2%		
		A_V = 10			1%			1%		
	Gain-bandwidth product	f = 10 kHz, R_L = 50 kΩ, C_L = 100 pF	25°C		0.21			0.21		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 50 kΩ, C_L = 100 pF	25°C		14			14		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ, C_L = 100 pF	25°C		63°			63°		
	Gain margin		25°C		15			15		dB

† Full range is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2254I			TLC2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		200	1500		200	850	µV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			1000			1000	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			1000			1000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\| \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.98			4.98		V
		I_{OH} = −75 µA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		I_{OH} = −150 µA		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		1700			1700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = $V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		140	250		140	250	µA
				Full range			300			300	

† Full range is – 40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2254I			TLC2254AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, R_L = 100 kΩ‡, C_L = 100 pF‡	25°C	0.07	0.12		0.07	0.12		V/μs
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		36			36		nV/√Hz
		f = 1 kHz	25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz	25°C		1.1			1.1		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡ A_V = 1	25°C		0.2%			0.2%		
		A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		63°			63°		
	Gain margin		25°C		15			15		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2254I			TLC2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		200	1500		200	850	µV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			1000			1000	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			1000			1000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert \le 5$ mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.98			4.98		V
		I_O = −100 µA		25°C	4.9	4.93		4.9	4.93		
				Full range	4.7			4.7			
		I_O = −200 µA		25°C	4.8	4.86		4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 µA		25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 µA		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = 4 mA		25°C	−4	−4.3		−4	−4.3		
				Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 100 kΩ	25°C	40	150		40	150		V/mV
				Full range	10			10			
			R_L = 1 MΩ	25°C		3000			3000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10		25°C		190			190		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω		25°C	75	88		75	88		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, $V_{IC} = V_{DD}/2$, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 0, No load		25°C		160	250		160	250	µA
				Full range			300			300	

† Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2254I			TLC2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm1.9$ V, $C_L = 100$ pF	$R_L = 100$ kΩ,	25°C	0.07	0.12		0.07	0.12		V/µs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		38			38		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm2.3$ V, $R_L = 50$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.2%			0.2%		
			$A_V = 10$			1%			1%		
	Gain-bandwidth product	f =10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.21			0.21		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		14			14		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is –40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2252M			TLC2252AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		200	1500		200	850	µV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\| \le 5$ mV		25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.98			4.98		V
		I_{OH} = −75 µA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		I_{OH} = −150 µA		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 µA		25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA		25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 4 mA		25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		1700			1700		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, f = 10 kHz,		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10		25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, $V_{IC} = V_{DD}/2$, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load		25°C		70	125		70	125	µA
				Full range			150			150	

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252M			TLC2252AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, R_L = 100 kΩ‡, C_L = 100 pF‡		25°C	0.07	0.12		0.07	0.12		V/µs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2252M			TLC2252AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		200	1500		200	850	µV
			Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, |V_{IO}| ≤5 mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA	25°C		4.98			4.98		V
		I_O = −100 µA	25°C	4.9	4.93		4.9	4.93		
			Full range	4.7			4.7			
		I_O = −200 µA	25°C	4.8	4.86		4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 µA	25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 µA	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = 4 mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 100 kΩ	25°C	40	150		40	150		V/mV
			Full range	10			10			
		V_O = ±4 V, R_L = 1 MΩ	25°C		3000			3000		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10	25°C		190			190		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = ±2.2 V to ±8 V, V_{IC} = 0, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		80	125		80	125	µA
			Full range			150			150	

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252M			TLC2252AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2$ V, $R_L = 100$ kΩ, $C_L = 100$ pF		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		38			38		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, $R_L = 50$ kΩ, f = 10 kHz	$A_V = 1$	25°C		0.2%			0.2%		
			$A_V = 10$			1%			1%		
	Gain-bandwidth product	f = 10 kHz, $R_L = 50$ kΩ, $C_L = 100$ pF		25°C		0.21			0.21		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $A_V = 1$, $R_L = 50$ kΩ, $C_L = 100$ pF		25°C		14			14		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ, $C_L = 100$ pF		25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is –55°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2254M			TLC2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		25°C		200	1500		200	850	µV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				125°C			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				125°C			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV		25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20$ µA		25°C		4.98			4.98		V
		$I_{OH} = -75$ µA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		$I_{OH} = -150$ µA		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V, $I_{OL} = 50$ µA		25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V, $I_{OL} = 500$ µA		25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		$V_{IC} = 2.5$ V, $I_{OL} = 4$ mA		25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 100$ kΩ‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			$R_L = 1$ MΩ‡	25°C		1700			1700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, $A_V = 10$		25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 50\ \Omega$		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 2.5$ V, No load		25°C		140	250		140	250	µA
				Full range			300			300	

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2254M			TLC2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, R_L = 100 kΩ‡, C_L = 100 pF‡		25°C	0.07	0.12		0.07	0.12		V/µs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2254M MIN	TLC2254M TYP	TLC2254M MAX	TLC2254AM MIN	TLC2254AM TYP	TLC2254AM MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		200	1500		200	850	µV
			Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20$ µA	25°C		4.98			4.98		V
		$I_O = -100$ µA	25°C	4.9	4.93		4.9	4.93		
			Full range	4.7			4.7			
		$I_O = -200$ µA	25°C	4.8	4.86		4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50$ µA	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500$ µA	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 100$ kΩ	25°C	40	150		40	150		V/mV
			Full range	10			10			
		$V_O = \pm4$ V, $R_L = 1$ MΩ	25°C		3000			3000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, $A_V = 10$	25°C		190			190		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.2$ V to ±8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 0$, No load	25°C		160	250		160	250	µA
			Full range			300			300	

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2254M			TLC2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2$ V, $C_L = 100$ pF	$R_L = 100$ kΩ,	25°C	0.07	0.12		0.07	0.12		V/µs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		38			38		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, $R_L = 50$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.2%			0.2%		
			$A_V = 10$			1%			1%		
	Gain-bandwidth product	f = 10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.21			0.21		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		14			14		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is −55°C to 125°C.

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2252Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω		200		µV
I_{IO}	Input offset current				0.5		pA
I_{IB}	Input bias current				1		pA
V_{ICR}	Common-mode input voltage range	$\mid V_{IO} \mid \le 5$ mV,	R_S = 50 Ω		−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 µA			4.98		V
		I_{OH} = −75 µA			4.94		
		I_{OH} = −150 µA			4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA		0.09		
		V_{IC} = 2.5 V,	I_{OL} = 4 mA		0.8		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ†		350		V/mV
			R_L = 1 MΩ†		1700		
r_{id}	Differential input resistance				10^{12}		Ω
r_{ic}	Common-mode input resistance				10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10		200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,		83		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, No load	$V_{IC} = V_{DD}/2$,		95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		70		µA

† Referenced to 2.5 V

electrical characteristics at $V_{DD\pm} = \pm5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2252Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	$V_O = 0$,		200		µV
I_{IO}	Input offset current				0.5		pA
I_{IB}	Input bias current				1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert \le 5$ mV,	$R_S = 50\ \Omega$		–5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	$I_O = -20$ µA			4.99		V
		$I_O = -100$ µA			4.93		
		$I_O = -200$ µA			4.86		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$,	$I_{OL} = 50$ µA		–4.99		V
		$V_{IC} = 0$,	$I_{OL} = 500$ µA		–4.91		
		$V_{IC} = 0$,	$I_{OL} = 4$ mA		–4.1		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V	$R_L = 100$ kΩ		150		V/mV
			$R_L = 1$ MΩ		3000		
r_{id}	Differential input resistance				10^{12}		Ω
r_{ic}	Common-mode input resistance				10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	$A_V = 10$		190		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $R_S = 50\ \Omega$	$V_O = 0$,		88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.2$ V to ±8 V, No load	$V_{IC} = 0$,		95		dB
I_{DD}	Supply current	$V_O = 0$,	No load		80		µA

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2254Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD\pm}$ = ±2.5 V, V_O = 0, R_S = 50 Ω			200		µV
I_{IO}	Input offset current				0.5		pA
I_{IB}	Input bias current				1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert \le 5$ mV, R_S = 50 Ω			−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 µA			4.98		V
		I_{OH} = −75 µA			4.94		
		I_{OH} = −150 µA			4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 µA			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA			0.09		
		V_{IC} = 2.5 V, I_{OL} = 4 mA			0.8		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ†		350		V/mV
			R_L = 1 MΩ†		1700		
$r_{i(d)}$	Differential input resistance				10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance				10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω			83		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load			95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, No load			140		µA

† Referenced to 2.5 V

electrical characteristics at $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2254Y		UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω, V_O = 0,		200		µV
I_{IO}	Input offset current			0.5		pA
I_{IB}	Input bias current			1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert \le 5$ mV, R_S = 50 Ω		−5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		4.99		V
		I_O = −100 µA		4.93		
		I_O = −200 µA		4.86		
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_{OL} = 50 µA		−4.99		V
		V_{IC} = 0, I_{OL} = 500 µA		−4.91		
		V_{IC} = 0, I_{OL} = 4 mA		−4.1		
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 100 kΩ		150		V/mV
		V_O = ±4 V, R_L = 1 MΩ		3000		
$r_{i(d)}$	Differential input resistance			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10		190		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω		88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, V_{IC} = 0, No load		95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 0, No load		160		µA

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLC2252
INPUT OFFSET VOLTAGE**

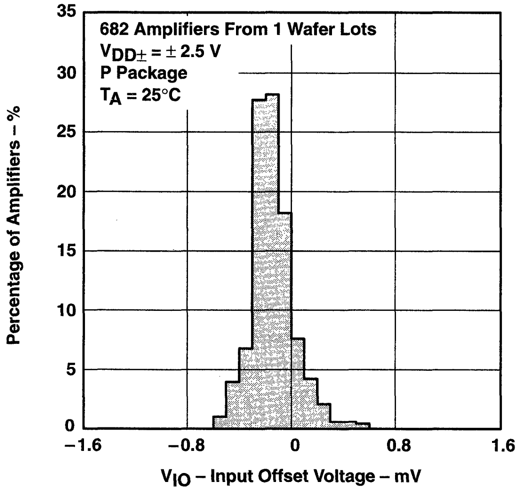

Figure 2

**DISTRIBUTION OF TLC2252
INPUT OFFSET VOLTAGE**

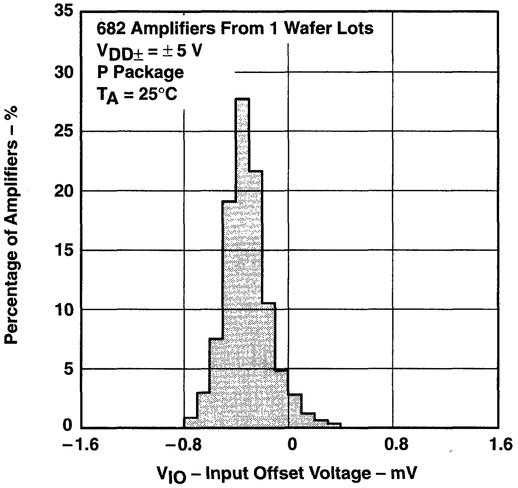

Figure 3

**DISTRIBUTION OF TLC2254
INPUT OFFSET VOLTAGE**

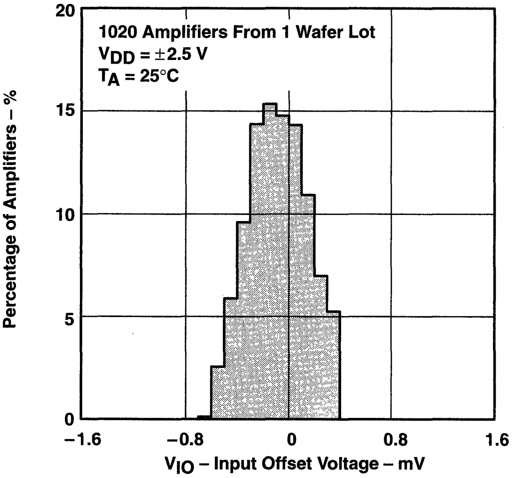

Figure 4

**DISTRIBUTION OF TLC2254
INPUT OFFSET VOLTAGE**

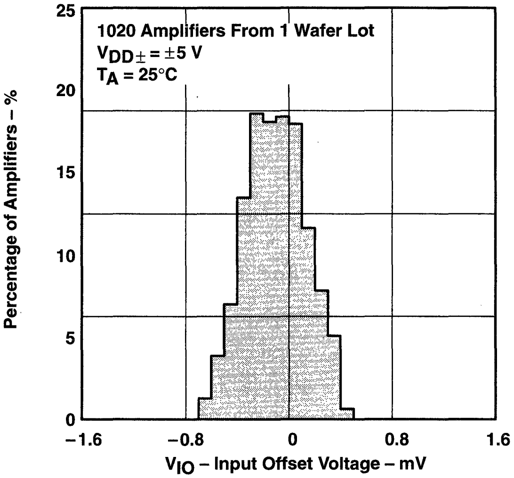

Figure 5

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE

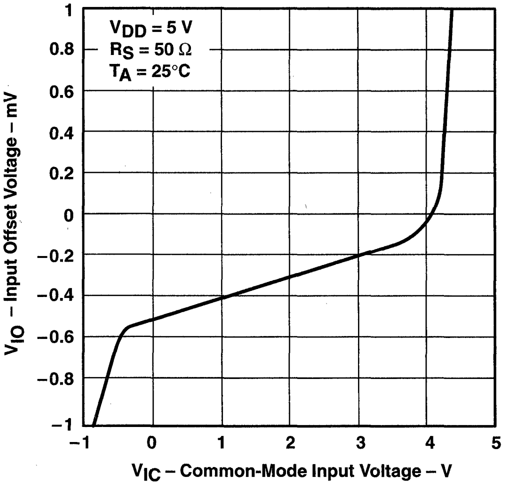

Figure 6

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

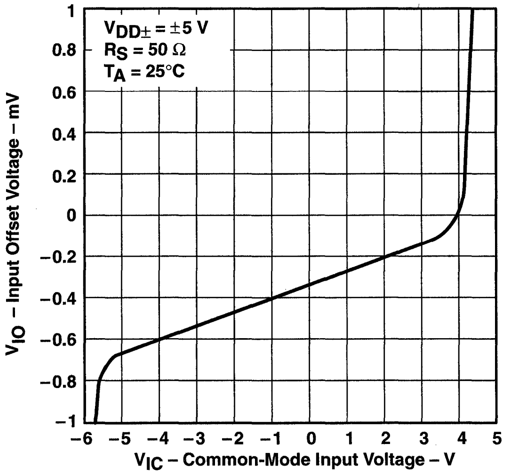

Figure 7

DISTRIBUTION OF TLC2252 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

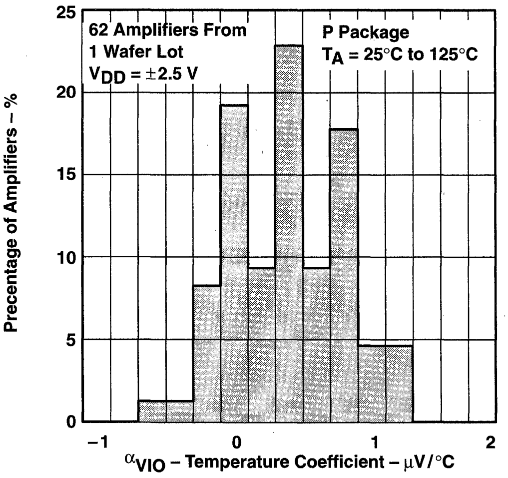

Figure 8

DISTRIBUTION OF TLC2252 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

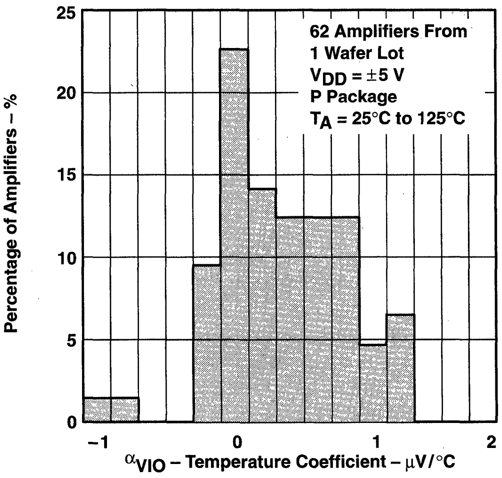

Figure 9

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† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2254 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

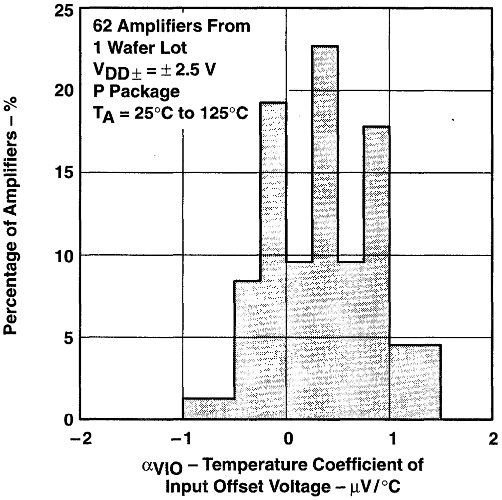

Figure 10

DISTRIBUTION OF TLC2254 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

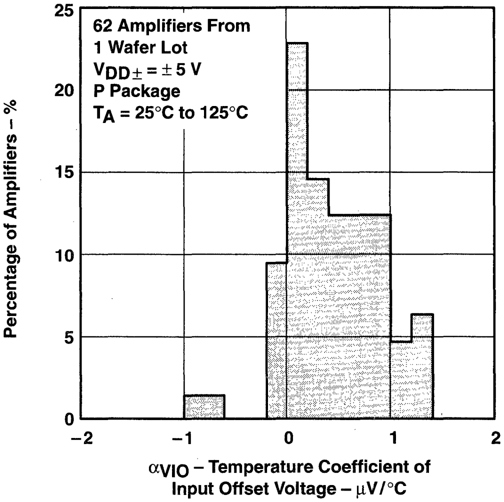

Figure 11

INPUT BIAS AND INPUT OFFSET CURRENTS† vs FREE-AIR TEMPERATURE

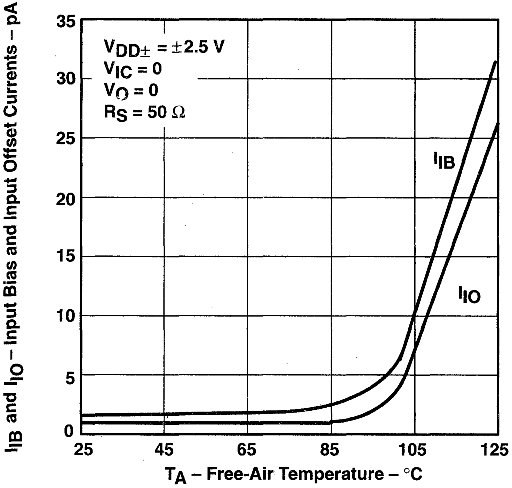

Figure 12

INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

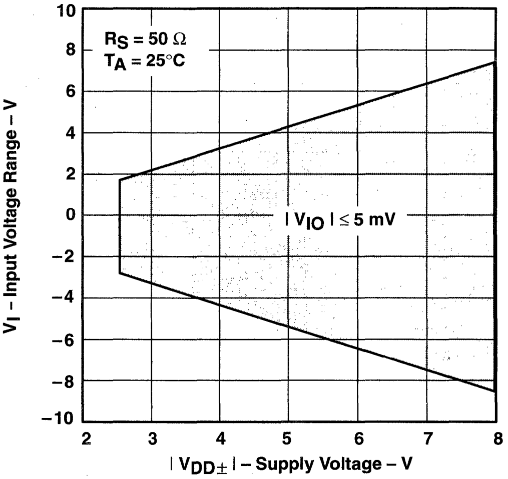

Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

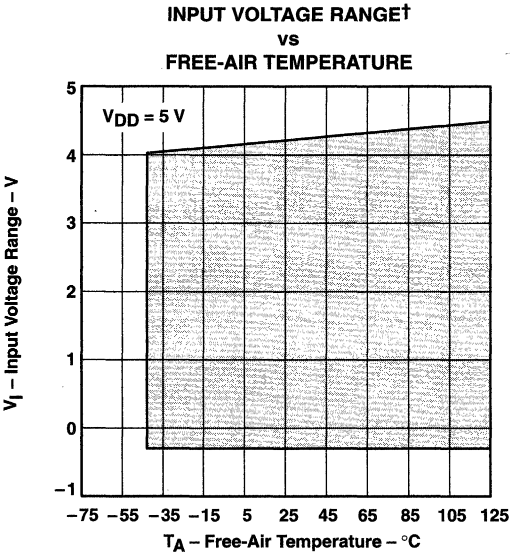

Figure 14

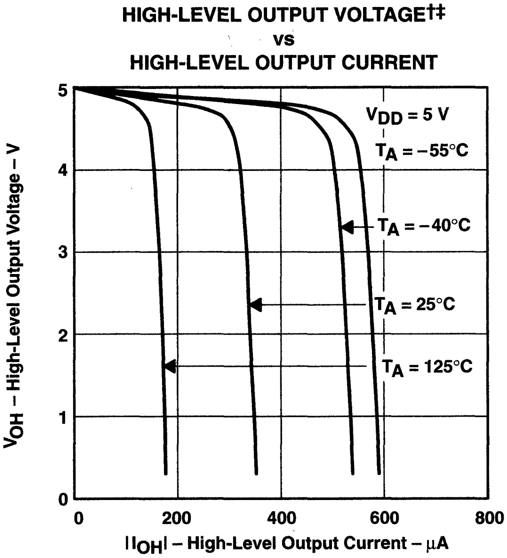

Figure 15

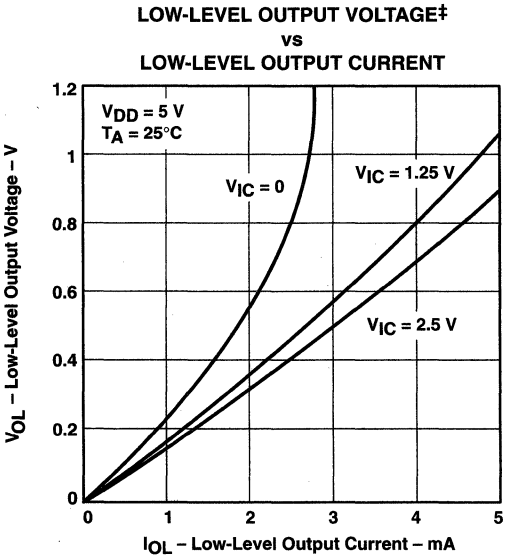

Figure 16

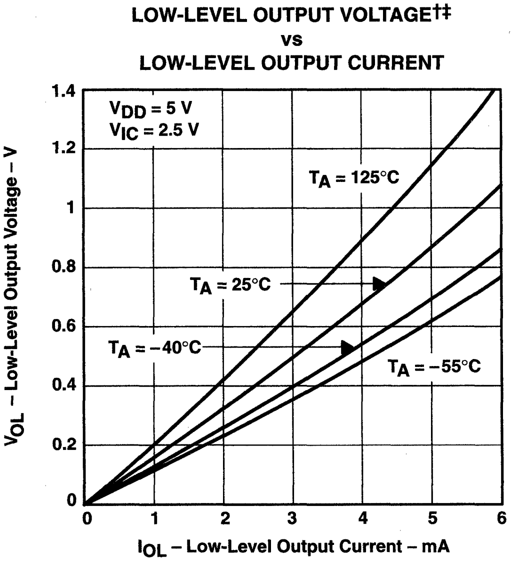

Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE† vs OUTPUT CURRENT

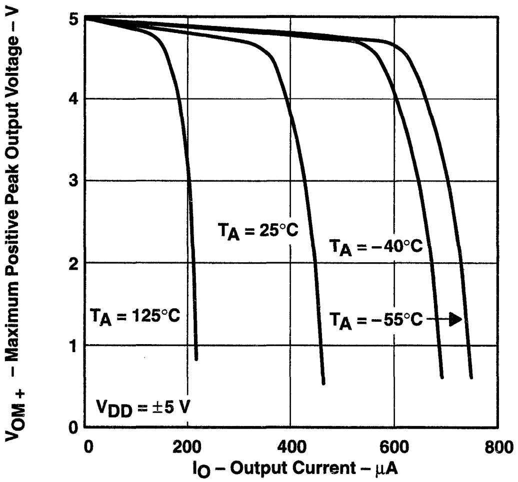

Figure 18

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE† vs OUTPUT CURRENT

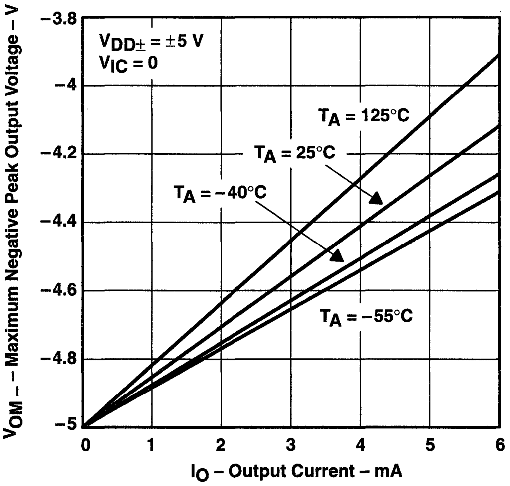

Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡ vs FREQUENCY

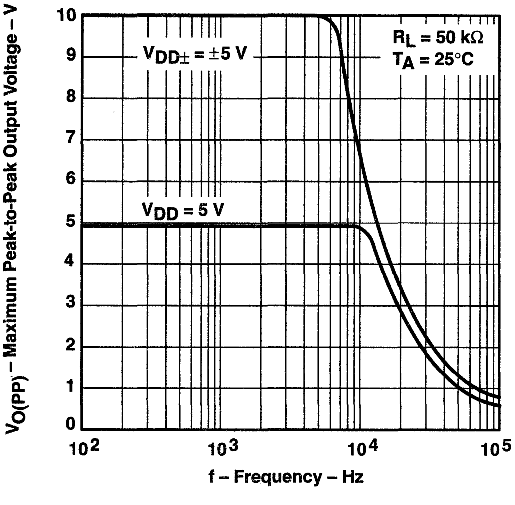

Figure 20

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

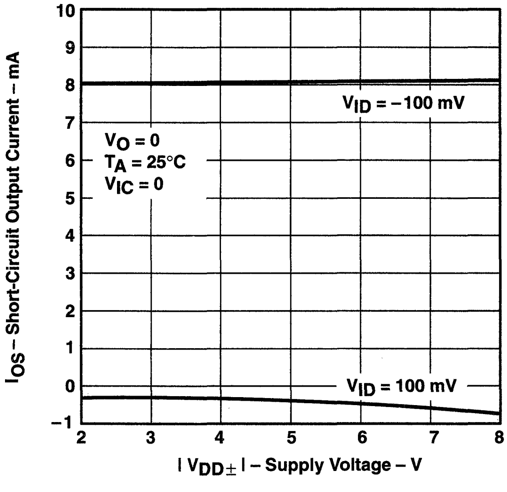

Figure 21

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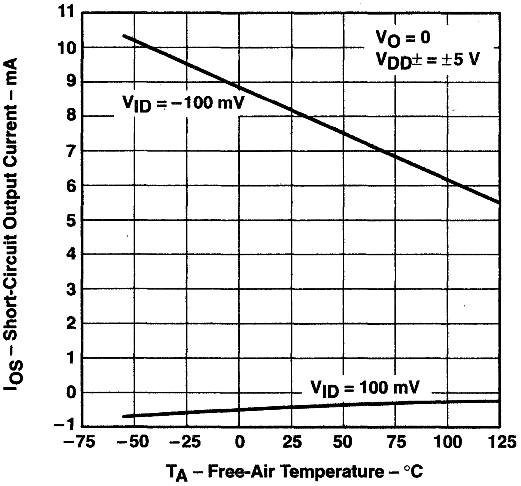
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

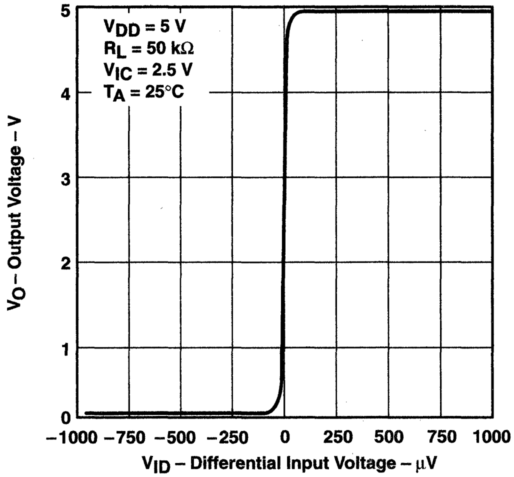
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



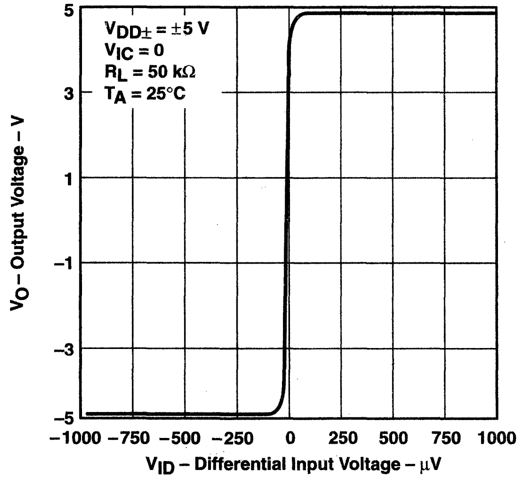
SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

Figure 22



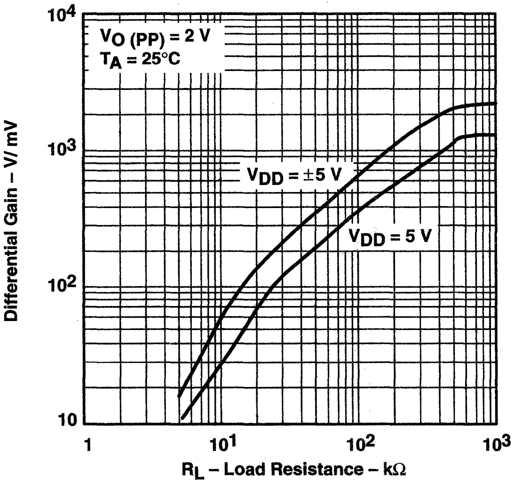
OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 23



OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 24



DIFFERENTIAL GAIN‡
vs
LOAD RESISTANCE

Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN† vs FREQUENCY

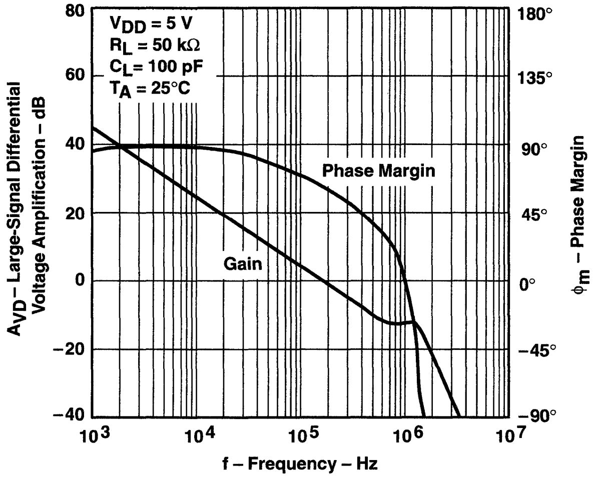

Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

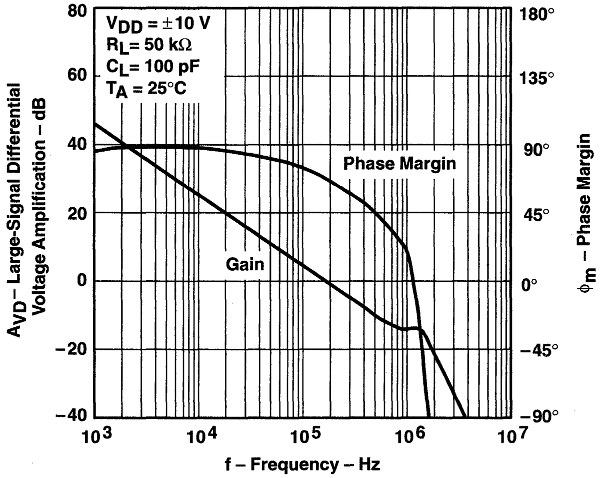

Figure 27

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† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡ vs FREE-AIR TEMPERATURE

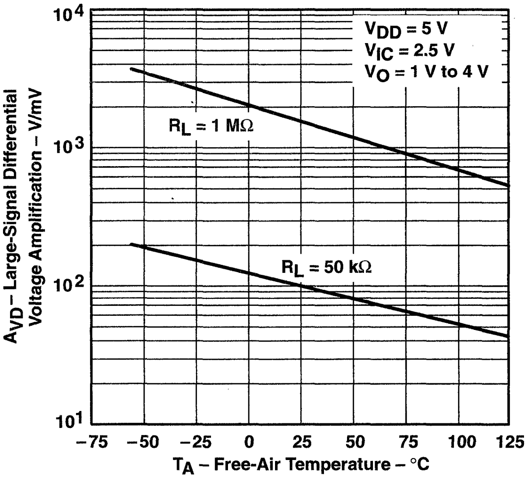

Figure 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

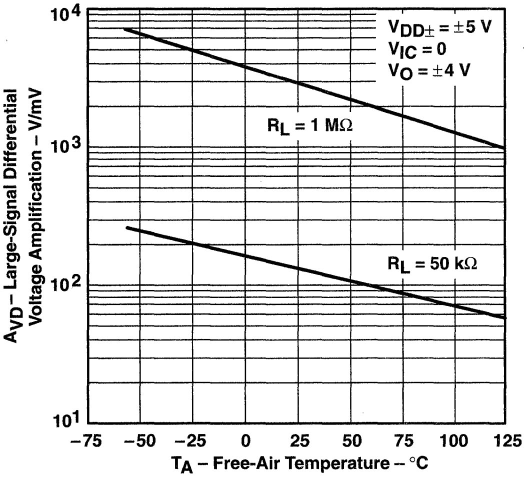

Figure 29

OUTPUT IMPEDANCE‡ vs FREQUENCY

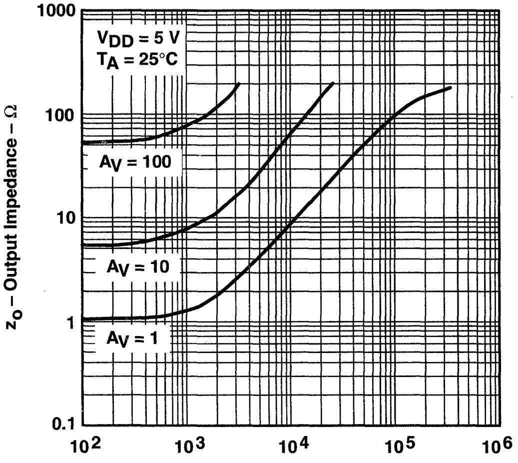

Figure 30

OUTPUT IMPEDANCE vs FREQUENCY

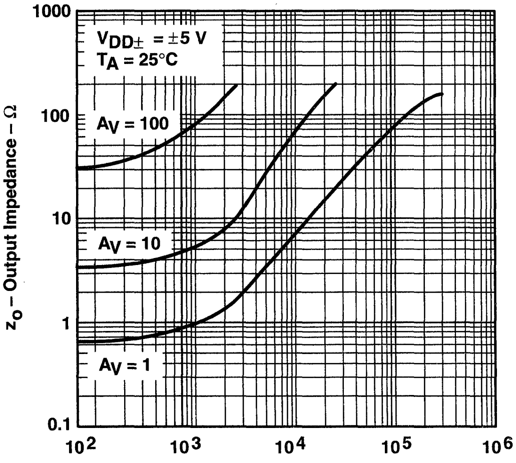

Figure 31

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO†
vs
FREQUENCY

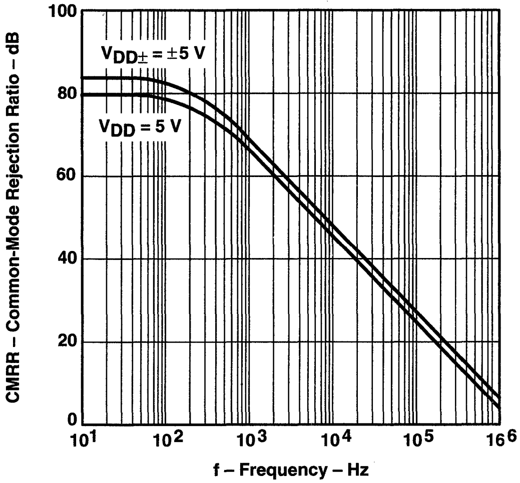

Figure 32

COMMON-MODE REJECTION RATIO†‡
vs
FREE-AIR TEMPERATURE

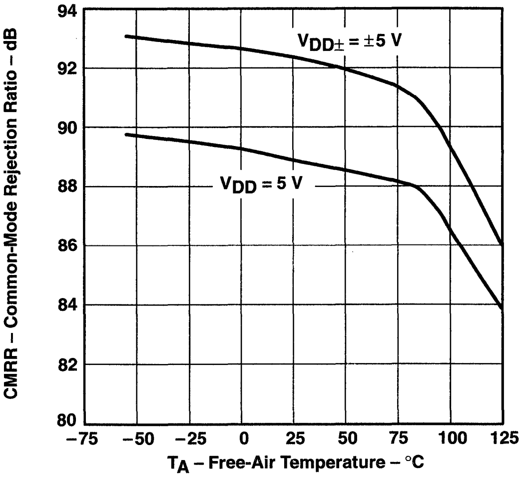

Figure 33

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREQUENCY

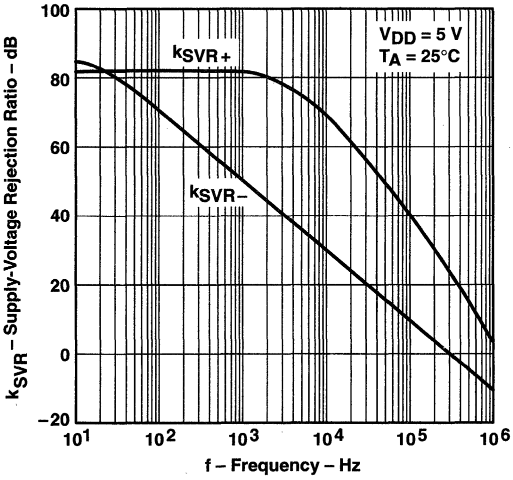

Figure 34

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

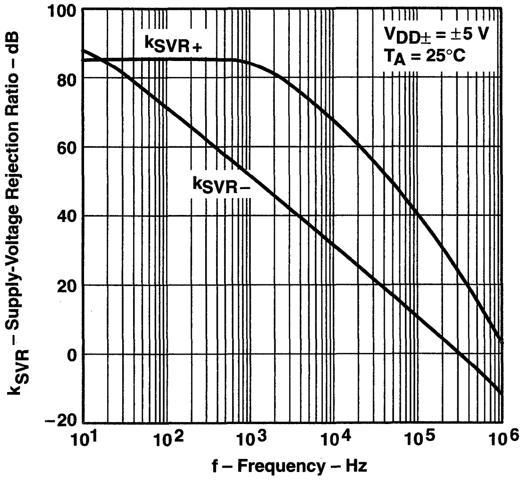

Figure 35

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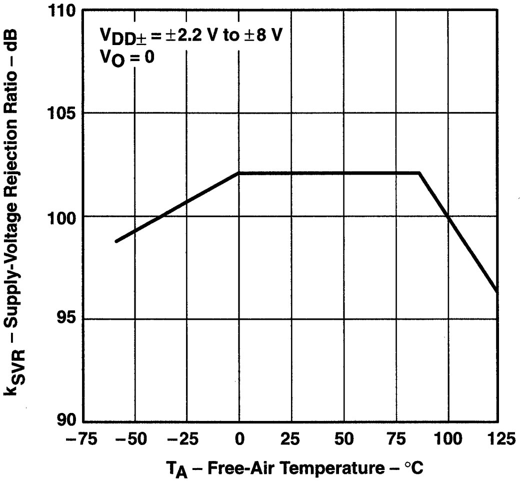
† For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

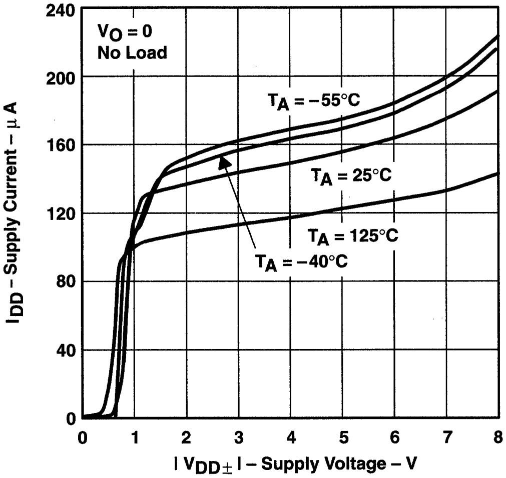
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



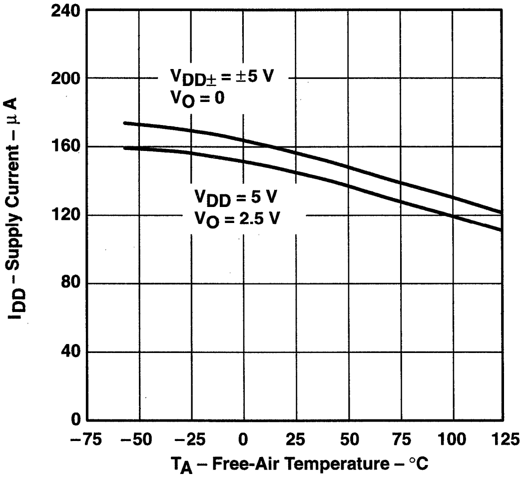
SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

Figure 36



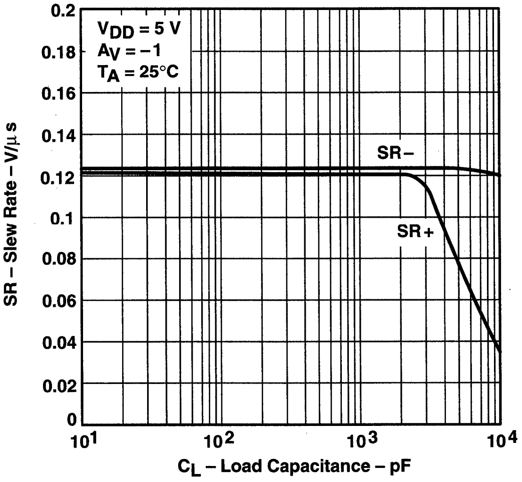
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

Figure 37



SUPPLY CURRENT†‡
vs
FREE-AIR TEMPERATURE

Figure 38



SLEW RATE‡
vs
LOAD CAPACITANCE

Figure 39

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

SLEW RATE†‡ vs FREE-AIR TEMPERATURE

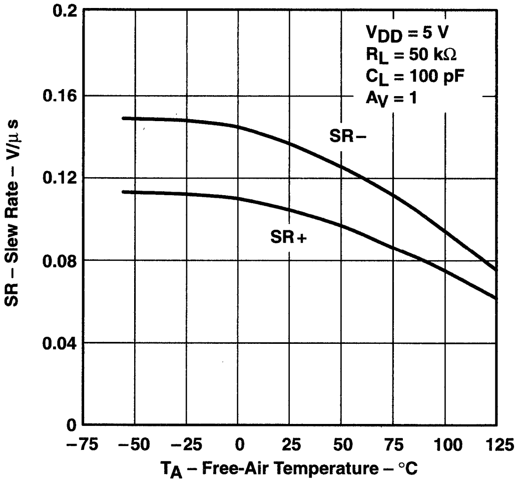

Figure 40

INVERTING LARGE-SIGNAL PULSE RESPONSE‡

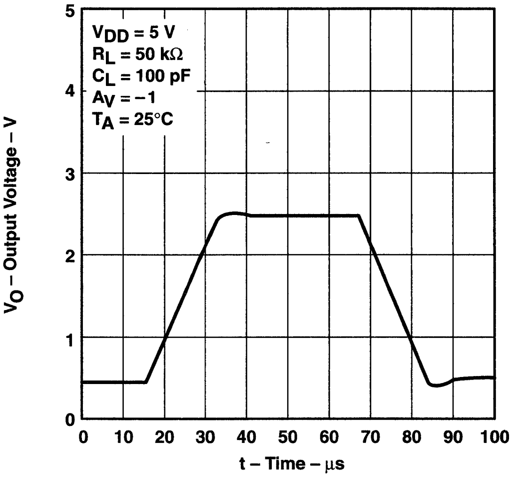

Figure 41

INVERTING LARGE-SIGNAL PULSE RESPONSE

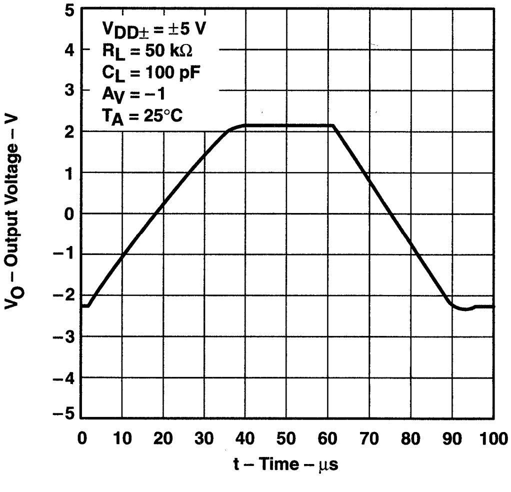

Figure 42

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE‡

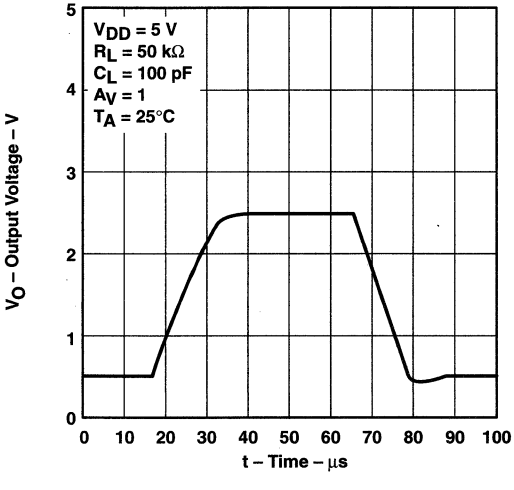

Figure 43

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

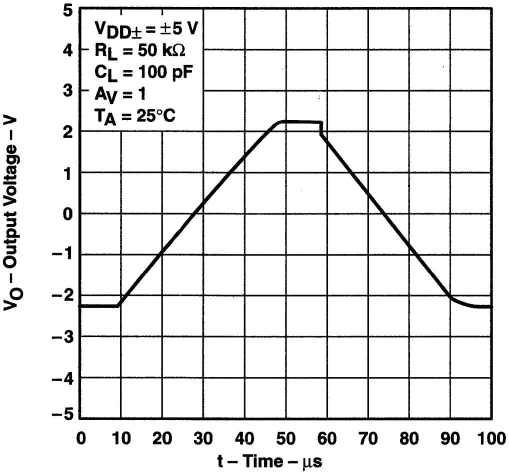

Figure 44

INVERTING SMALL-SIGNAL PULSE RESPONSE†

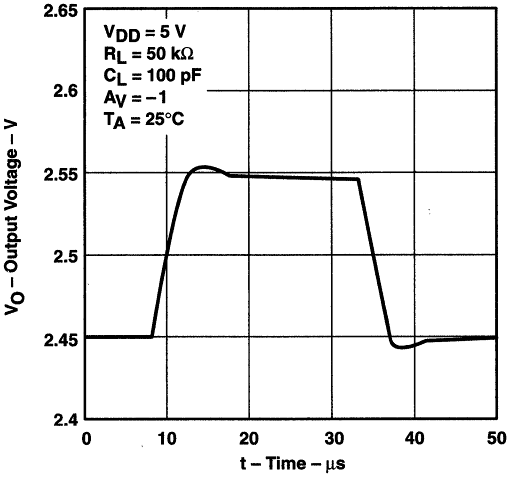

Figure 45

INVERTING SMALL-SIGNAL PULSE RESPONSE

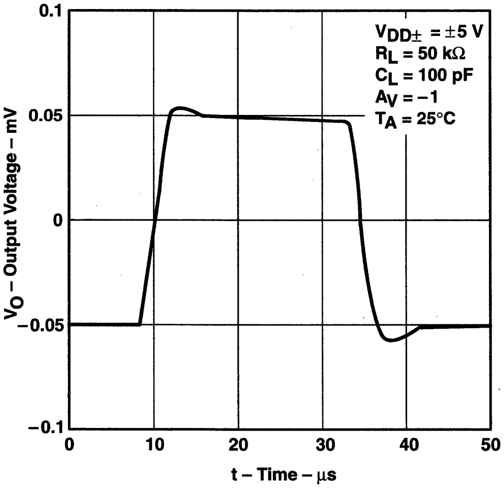

Figure 46

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

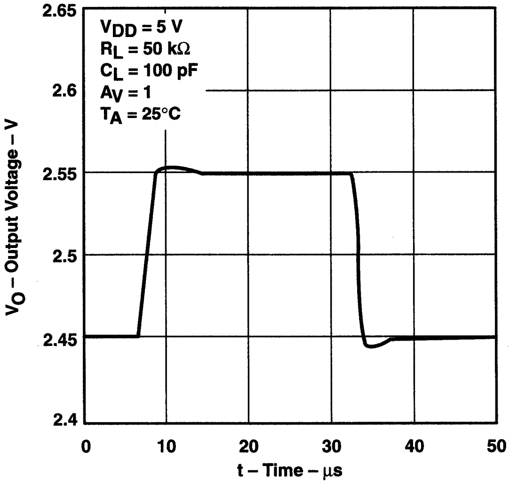

Figure 47

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† For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

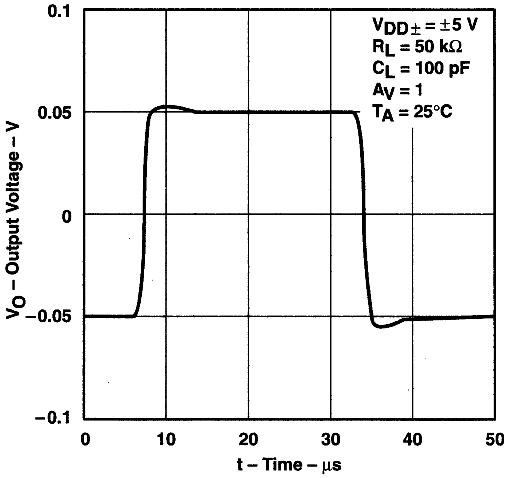

Figure 48

EQUIVALENT INPUT NOISE VOLTAGE† vs FREQUENCY

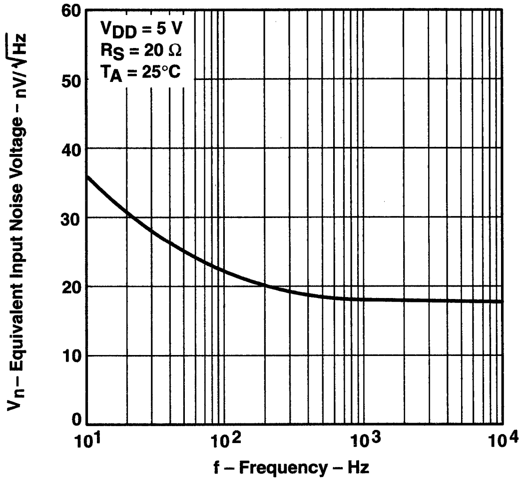

Figure 49

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

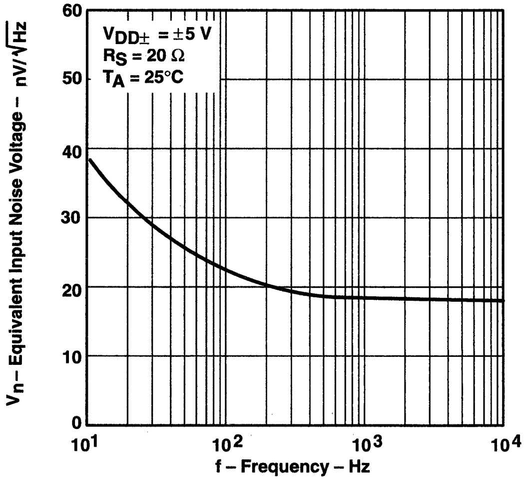

Figure 50

EQUIVALENT INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD†

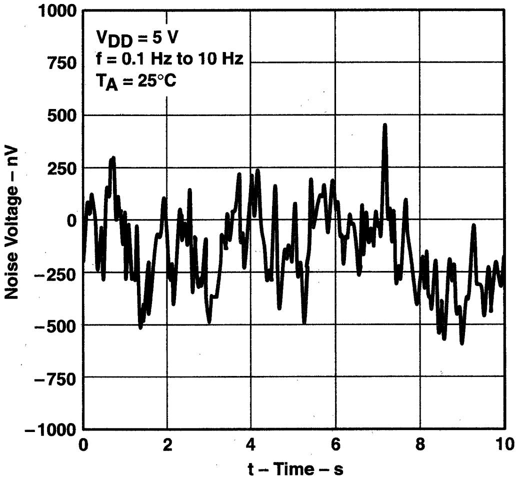

Figure 51

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† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

INTEGRATED NOISE VOLTAGE
vs
FREQUENCY

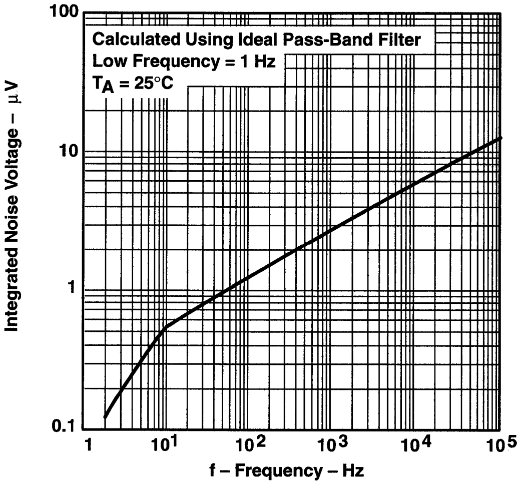

Figure 52

TOTAL HARMONIC DISTORTION PLUS NOISE†
vs
FREQUENCY

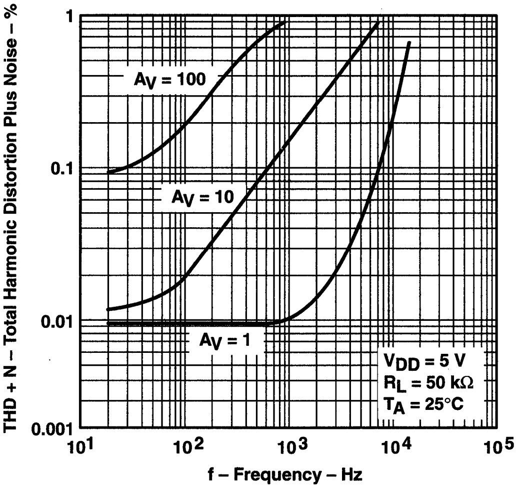

Figure 53

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

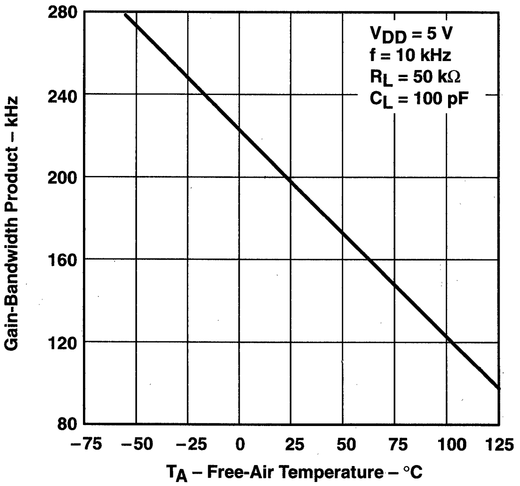

Figure 54

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

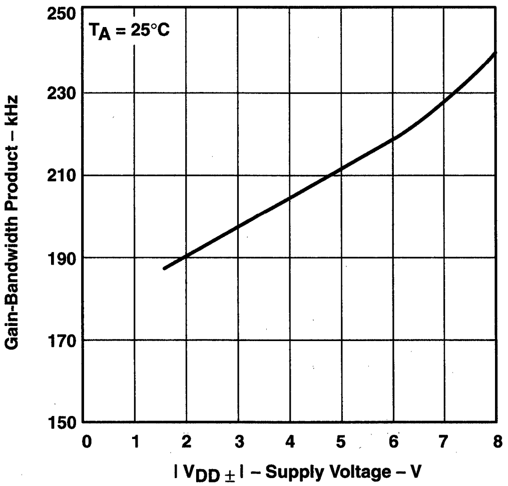

Figure 55

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† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

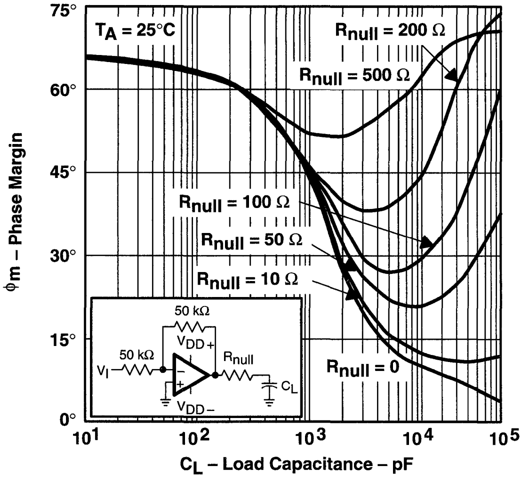

Figure 56

GAIN MARGIN
vs
LOAD CAPACITANCE

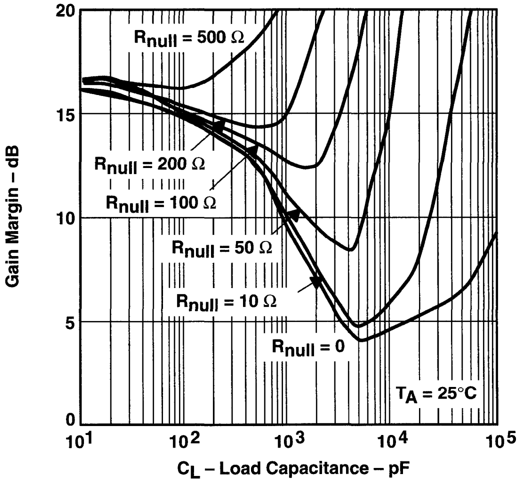

Figure 57

UNITY-GAIN BANDWIDTH†
vs
LOAD CAPACITANCE

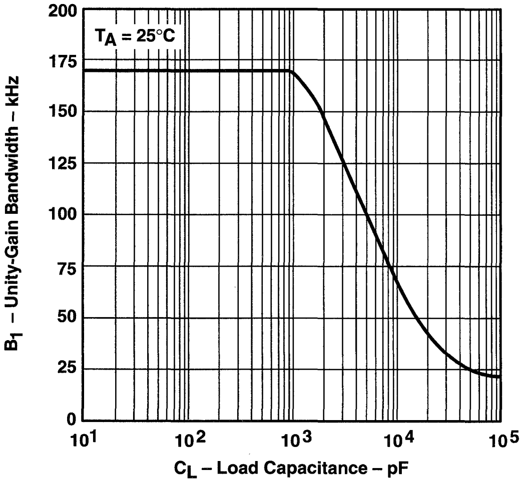

Figure 58

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE

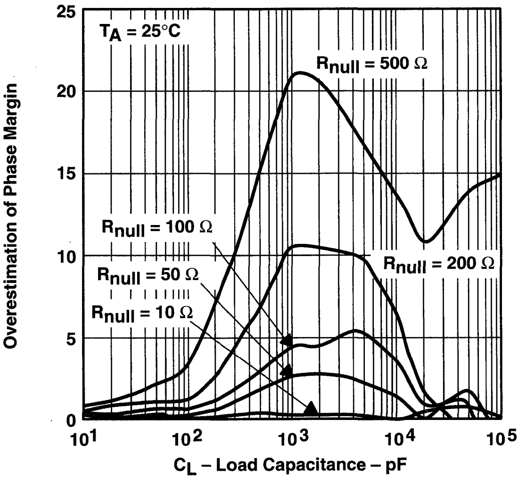

Figure 59

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† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC225x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 56 and Figure 57 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 60) improves the gain and phase margins when driving large capacitive loads. Figure 56 and Figure 57 show the effects of adding series resistances of 10 Ω, 50 Ω, 100 Ω, 200 Ω, and 500 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \tag{1}$$

where :

$\Delta\phi_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 58). To use equation 1, UGBW must be approximated from Figure 58.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 60, with equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

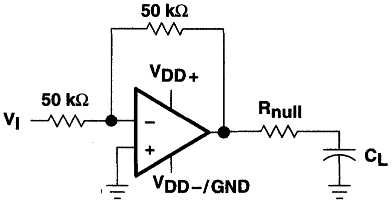


Figure 60. Series-Resistance Circuit

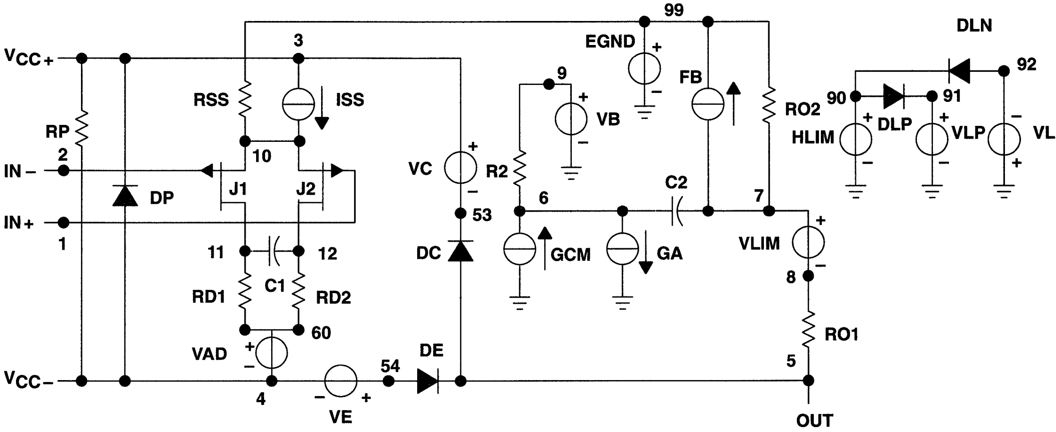
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 61 are generated using the TLC225x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



```
.SUBCKT TLC225x 1 2 3 4 5
   C1      11    12    6.369E–12
   C2      6     7     25.00E–12
   DC      5     53    DX
   DE      54    5     DX
   DLP     90    91    DX
   DLN     92    90    DX
   DP      4     3     DX
   EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
   FB      7     99    POLY (5) VB VC VE VLP
   + VLN 0 57.62E6 –60E6 60E6 60E6 –60E6
   GA      6     0     11    12 26.86E–6
   GCM     0     6     10    99 2.686E–9
   ISS     3     10    DC 3.1E–6
   HLIM    90    0     VLIM 1K
   J1      11    2     10 JX
   J2      12    1     10 JX
   R2      6     9     100.0E3
RD1     60    11    37.23E3
RD2     60    12    37.23E3
R01     8     5     84
R02     7     99    84
RP      3     4     71.43E3
RSS     10    99    64.52E6
VAD     60    4     –.5
VB      9     0     DC 0
VC      3     53    DC .605
VE      54    4     DC .605
VLIM    7     8     DC 0
VLP     91    0     DC –.235
VLN     0     92    DC 7.5
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=139E–6
+ VTO=–.05)
.ENDS
```

Figure 61. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

- **Output Swing includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage**
  950 μV Max at T_A = 25°C (TLC2262A)
- **Macromodel Included**
- **Performance Upgrade for the TS27M2/M4 and TLC27M2/M4**

description

The TLC2262 and TLC2264 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC226x family offers a compromise between the micropower TLC225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 μA (typ) of supply current per amplifier.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

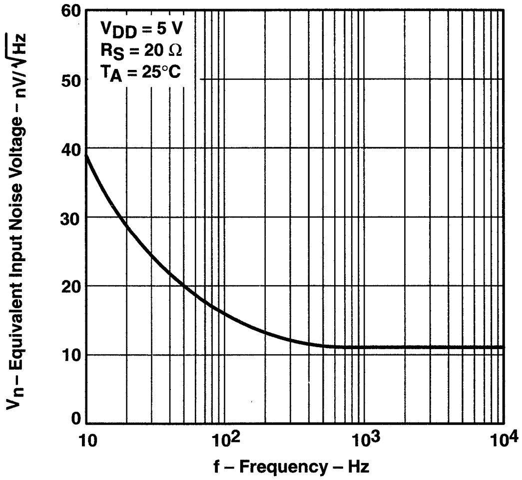


Figure 1

The TLC226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC226xA family is available and has a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2262/4 also makes great upgrades to the TLC27M2/L4 or TS27M2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

TLC2262 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CERAMIC FLATPACK (U)	
0°C to 70°C	2.5 mV	TLC2262CD	—	—	TLC2262CP	TLC2262CPWLE	—	TLC2262Y
−40°C to 125°C	950 μV 2.5 mV	TLC2262AID TLC2262ID	— —	— —	TLC2262AIP TLC2262IP	TLC2262AIPWLE —	— —	
−55°C to 125°C	950 μV 2.5 mV	— —	TLC2262AMFK TLC2262MFK	TLC2262AMJG TLC2262MJG	— —	— —	TLC2262AMU TLC2262MU	

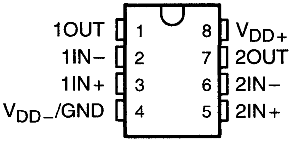
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2262CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

TLC2264 AVAILABLE OPTIONS

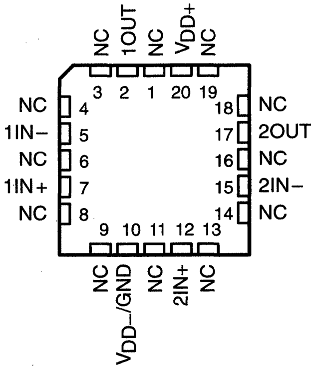
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	CERAMIC FLATPACK (W)	
0°C to 70°C	2.5 mV	TLC2264CD	—	—	TLC2264CN	TLC2264CPWLE	—	TLC2262Y
−40°C to 125°C	950 μV 2.5 mV	TLC2264AID TLC2264ID	— —	— —	TLC2264AIN TLC2264IN	TLC2264AIPWLE —	— —	
−55°C to 125°C	950 μV 2.5 mV	— —	TLC2264AMFK TLC2264MFK	TLC2264AMJ TLC2264MJ	— —	— —	TLC2264AMW TLC2264MW	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2264CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

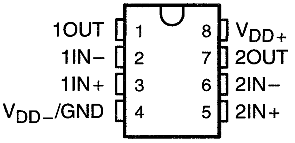
TLC2262C, TLC2262AC
TLC2262I, TLC2262AI
D, P, OR PW PACKAGE
(TOP VIEW)



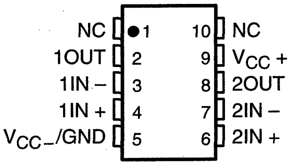
TLC2262M, TLC2262AM . . . FK PACKAGE
(TOP VIEW)



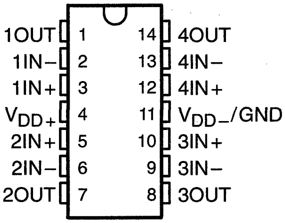
TLC2262M, TLC2262AM . . . JG PACKAGE
(TOP VIEW)



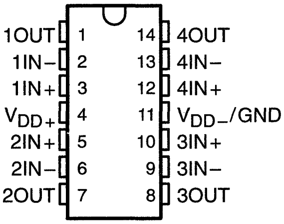
TLC2262M, TLC2262AM . . . U PACKAGE
(TOP VIEW)



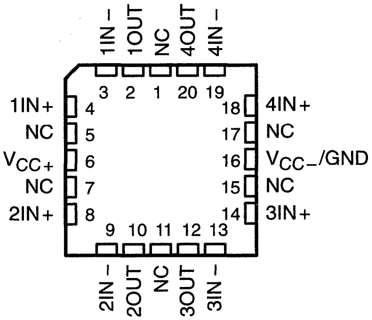
TLC2264C, TLC2264AC
TLC2264I, TLC2264AI
D, N, OR PW PACKAGE
(TOP VIEW)



TLC2264M, TLC2264AM . . . J OR W PACKAGE
(TOP VIEW)



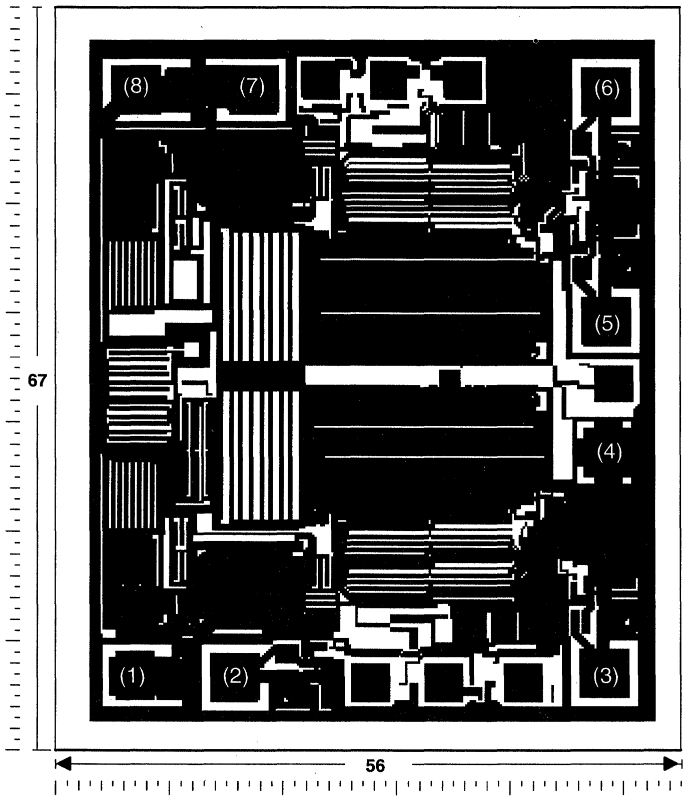
TLC2264M, TLC2264AM . . . FK PACKAGE
(TOP VIEW)

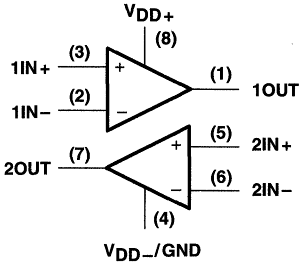


TLC2262Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2262C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

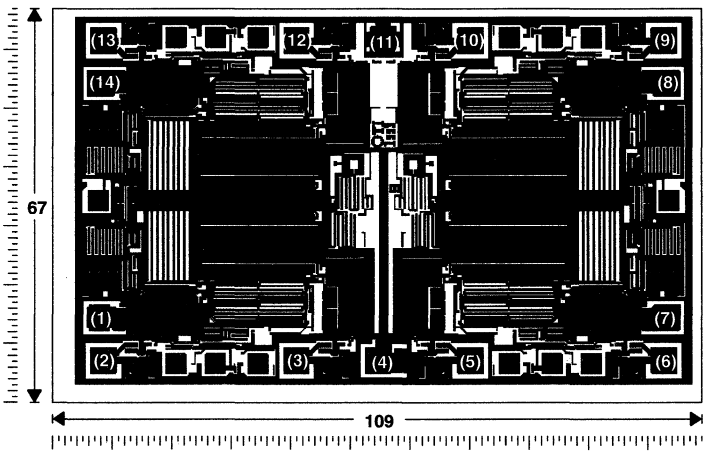
ALL DIMENSIONS ARE IN MILS.

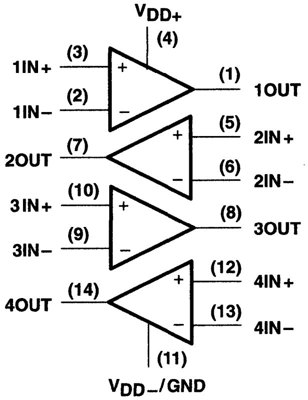
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TLC2264Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2264C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

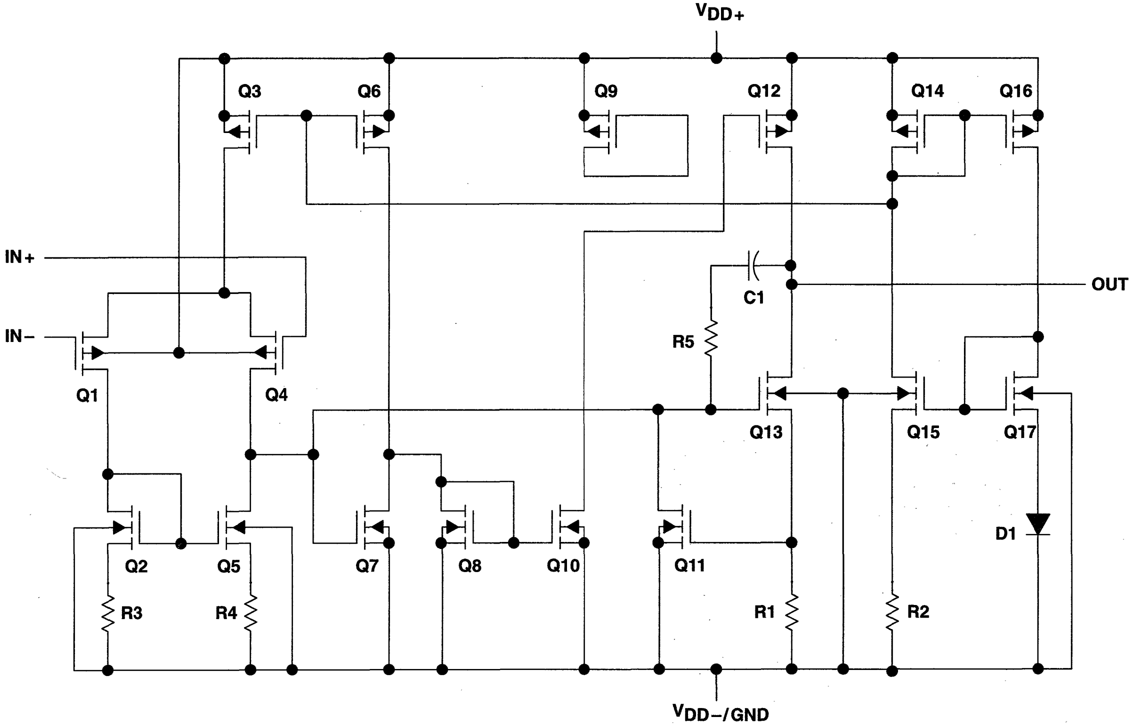
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2262	TLC2264
Transistors	38	76
Resistors	28	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	V_{DD-} – 0.3 V to V_{DD+}
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	–40°C to 125°C
M suffix	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, and PW packages	260°C
J, JG, U, and W packages	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current flows if input is brought below V_{DD-} – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW–8	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW–14	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW
U	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V
Operating free-air temperature, T_A	0	70	–40	125	–55	125	°C

TLC2262C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2262C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD\pm}$ = ±2.5 V, V_O = 0, R_S = 50 Ω	25°C		300	2500	µV
			Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA	25°C		4.99		V
		I_{OH} = −100 µA	25°C	4.85	4.94		
			Full range	4.82			
		I_{OH} = −400 µA	25°C	4.70	4.85		
			Full range	4.60			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 µA	25°C		0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		0.09	0.15	
			Full range			0.15	
		V_{IC} = 2.5 V, I_{OL} = 1 mA	25°C		0.2	0.3	
			Full range			0.3	
		V_{IC} = 2.5 V, I_{OL} = 4 mA	25°C		0.7	1	
			Full range			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 50 kΩ‡	25°C	80	170		V/mV
			Full range	55			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ‡	25°C		550		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		dB
			Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = $V_{DD}/2$, No load	25°C	80	95		dB
			Full range	80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		400	500	µA
			Full range			500	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C	0.35	0.55		V/µs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		$\mathrm{fA}\sqrt{\mathrm{Hz}}$
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4		µs
			To 0.01%			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		56°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

TLC2262C electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	$V_O = 0$,	25°C		300	2500	µV
				Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le 5$ mV,	$R_S = 50\ \Omega$	25°C	−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$		25°C		4.99		V
		$I_O = -100\ \mu A$		25°C	4.85	4.94		
				Full range	4.82			
		$I_O = -400\ \mu A$		25°C	4.7	4.85		
				Full range	4.6			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$,	$I_O = 50\ \mu A$	25°C		−4.99		V
		$V_{IC} = 0$,	$I_O = 500\ \mu A$	25°C	−4.85	−4.91		
				Full range	−4.85			
		$V_{IC} = 0$,	$I_O = 1$ mA	25°C	−4.7	−4.8		
				Full range	−4.7			
		$V_{IC} = 0$,	$I_O = 4$ mA	25°C	−4	−4.3		
				Full range	−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V	$R_L = 50\ k\Omega$	25°C	80	200		V/mV
				Full range	55			
			$R_L = 1\ M\Omega$	25°C		1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$	25°C		220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$ V,	$R_S = 50\ \Omega$	25°C	75	88		dB
				Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = 2.2$ V to ±8 V, $V_{IC} = 0$,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	$V_O = 0$ V,	No load	25°C		425	500	µA
				Full range			500	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9$ V, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C	0.35	0.55		V/μs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion pulse duration	$V_O = \pm 2.3$ V, f = 20 kHz, $R_L = 50$ kΩ	$A_V = 1$	25°C		0.014%		
			$A_V = 10$			0.024%		
	Gain-bandwidth product	f = 10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		85		kHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 50$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		7.1		μs
			To 0.01%			16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		57°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.

TLC2264C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2264C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω	25°C		300	2500	µV
				Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.99		V
		I_{OH} = −100 µA		25°C	4.85	4.94		
				Full range	4.82			
		I_{OH} = −400 µA		25°C	4.70	4.85		
				Full range	4.60			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15	
				Full range			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3	
				Full range			0.3	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.7	1	
				Full range			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		V/mV
				Full range	55			
			R_L = 1 MΩ‡	25°C		550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1	mA
				Full range			1	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V
NOTE 4. Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		V/µs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4		µs
			To 0.01%			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

TLC2264C electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise specified)

	PARAMETER	TEST CONDITIONS	T_A†	TLC2264C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500	µV
			Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le 5$ mV, $R_S = 50\ \Omega$	25°C	−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99		V
		$I_O = -100\ \mu A$	25°C	4.85	4.94		
			Full range	4.82			
		$I_O = -400\ \mu A$	25°C	4.7	4.85		
			Full range	4.6			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		
			Full range	−4.85			
		$V_{IC} = 0$, $I_O = 1$ mA	25°C	−4.7	−4.8		
			Full range	−4.7			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		
			Full range	−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 50\ k\Omega$	25°C	80	200		V/mV
			Full range	55			
		$V_O = \pm4$ V, $R_L = 1\ M\Omega$	25°C		1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		dB
			Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.2$ V to ±8 V, $V_{IC} = 0$, No load	25°C	80	95		dB
			Full range	80			
I_{DD}	Supply current (four amplifiers)	$V_O = 0$, No load	25°C		0.85	1	mA
			Full range			1	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9$ V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		V/μs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, f = 20 kHz, R_L = 50 kΩ	A_V = 1	25°C		0.014%		
			A_V = 10			0.024%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		70		kHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1		μs
			To 0.01%			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		57°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.

TLC2262I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I			TLC2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$,	$\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20\ \mu A$		25°C		4.99			4.99		V
		$I_{OH} = -100\ \mu A$		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		$I_{OH} = -400\ \mu A$		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 50\ \mu A$	25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V,	$I_{OL} = 500\ \mu A$	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		$V_{IC} = 2.5$ V,	$I_{OL} = 4$ mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 50\ k\Omega$‡	25°C	80	100		80	170		V/mV
				Full range	50			50			
			$R_L = 1\ M\Omega$‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $R_S = 50\ \Omega$	$V_O = 2.5$ V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5$ V,	No load	25°C		400	500		400	500	µA
				Full range			500			500	

† Full range is – 40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I			TLC2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.82			0.82		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

TLC2262I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2262I			TLC2262AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99			4.99		V
		$I_O = -100\ \mu A$	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_O = -400\ \mu A$	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 50$ kΩ	25°C	80	200		80	200		V/mV
			Full range	50			50			
		$V_O = \pm4$ V, $R_L = 1$ MΩ	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5$ V, No load	25°C		425	500		425	500	µA
			Full range			500			500	

† Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262I operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262I			TLC2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±1.9 V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 50 kΩ, f = 20 kHz	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		85			85		kHz
t_s	Settling time	A_V = –1, Step = –2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1			7.1		μs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C.

TLC2264I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2264I			TLC2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO} \rvert \leq 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −400 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	100		80	170		V/mV
				Full range	50			50			
			R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1		0.8	1	mA
				Full range			1			1	

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264I			TLC2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 125°C.

‡ Referenced to 2.5 V

TLC2264I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264I			TLC2264AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO}\rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99			4.99		V
		$I_O = -100\ \mu A$	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_O = -400\ \mu A$	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 50\ k\Omega$	25°C	80	200		80	200		V/mV
			Full range	50			50			
		$V_O = \pm4$ V, $R_L = 1\ M\Omega$	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.2$ V to ±8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 0$, No load	25°C		0.85	1		0.85	1	mA
			Full range			1			1	

† Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264I			TLC2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm1.9$ V, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm2.3$ V, $R_L = 50$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.014%			0.014%		
			$A_V = 10$			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		70			70		kHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 50$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		7.1			7.1		μs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C.

TLC2262M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2262M			TLC2262AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		5			5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20$ μA	25°C		4.99			4.99		V
		$I_{OH} = -100$ μA	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_{OH} = -400$ μA	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V, $I_{OL} = 50$ μA	25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V, $I_{OL} = 500$ μA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		$V_{IC} = 2.5$ V, $I_{OL} = 4$ mA	25°C		0.8	1		0.7	1	
			Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 50$ kΩ‡	25°C	80	100		80	170		V/mV
			Full range	50			50			
		$R_L = 1$ MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 50\ \Omega$	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5$ V, No load	25°C		400	500		400	500	μA
			Full range			500			500	

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262M			TLC2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		0.82			0.82		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V

TLC2262M electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2262M			TLC2262AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		5			5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99			4.99		V
		$I_O = -100\ \mu A$	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_O = -400\ \mu A$	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 50$ kΩ	25°C	80	200		80	200		V/mV
			Full range	50			50			
		$V_O = \pm 4$ V, $R_L = 1$ MΩ	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		425	500		425	500	µA
			Full range			500			500	

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262M operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262M			TLC2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm2$ V, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm2.3$ V, $R_L = 50$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.014%			0.014%		
			$A_V = 10$			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		85			85		kHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 50$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		7.1			7.1		µs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is –55°C to 125°C.

TLC2264M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2264M			TLC2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				125°C			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				125°C			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\|$ ≤5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.99			4.99		V
		I_{OH} = −100 µA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −400 µA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	100		80	170		V/mV
				Full range	50			50			
			R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1		0.8	1	mA
				Full range			1			1	

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264M			TLC2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V

TLC2264M electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264M			TLC2264AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA	25°C		4.99			4.99		V
		I_O = −100 µA	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		I_O = −400 µA	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 µA	25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 µA	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = 4 mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 50 kΩ	25°C	80	200		80	200		V/mV
			Full range	50			50			
		V_O = ±4 V, R_L = 1 MΩ	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 0, No load	25°C		0.85	1		0.85	1	mA
			Full range			1			1	

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264M operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264M			TLC2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2 V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 50 kΩ, f = 20 kHz	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		70			70		kHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1			7.1		µs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is −55°C to 125°C.

TLC2262Y electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2262Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD\pm}$ = ±2.5 V, V_O = 0, R_S = 50 Ω			300		μV
I_{IO}	Input offset current				0.5		pA
I_{IB}	Input bias current				1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert \le 5$ mV, R_S = 50 Ω			−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA			4.99		V
		I_{OH} = −100 μA			4.94		
		I_{OH} = −400 μA			4.85		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA			0.09		
		V_{IC} = 2.5 V, I_{OL} = 4 mA			0.8		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ†		170		V/mV
			R_L = 1 MΩ†		550		
$r_{i(d)}$	Differential input resistance				10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance				10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω			83		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load			95		dB
I_{DD}	Supply current	V_O = 2.5 V, No load			400		μA

† Referenced to 2.5 V

TLC2262Y electrical characteristics at $V_{DD\pm} = \pm 5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2262Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$	$R_S = 50\ \Omega$,		300		µV
I_{IO}	Input offset current				0.5		pA
I_{IB}	Input bias current				1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert \le 5$ mV,	$R_S = 50\ \Omega$		−5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$			4.99		V
		$I_O = -100\ \mu A$			4.94		
		$I_O = -400\ \mu A$			4.85		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$,	$I_{OL} = 50\ \mu A$		−4.99		V
		$V_{IC} = 0$,	$I_{OL} = 500\ \mu A$		−4.91		
		$V_{IC} = 0$,	$I_{OL} = 4$ mA		−4.1		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V	$R_L = 50\ k\Omega$		200		V/mV
			$R_L = 1\ M\Omega$		1000		
$r_{i(d)}$	Differential input resistance				10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance				10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$		220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V,	$V_O = 0$, $R_S = 50\ \Omega$		88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ±8 V,	$V_{IC} = 0$, No load		95		dB
I_{DD}	Supply current	$V_O = 0$,	No load		425		µA

TLC2264Y electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLC2264Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$,	$V_{DD\pm} = \pm 2.5$ V, $R_S = 50\ \Omega$			300		µV
I_{IO}	Input offset current					0.5		pA
I_{IB}	Input bias current					1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert \le 5$ mV,	$R_S = 50\ \Omega$			−0.3 to 4.2		V
V_{OH}	High-level output voltage	$I_{OH} = -20$ µA				4.99		V
		$I_{OH} = -100$ µA				4.94		
		$I_{OH} = -400$ µA				4.85		
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 50$ µA			0.01		V
		$V_{IC} = 2.5$ V,	$I_{OL} = 500$ µA			0.09		
		$V_{IC} = 2.5$ V,	$I_{OL} = 4$ mA			0.8		
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 50$ kΩ†			170		V/mV
			$R_L = 1$ MΩ†			550		
$r_{i(d)}$	Differential input resistance					10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance					10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$			240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V,	$V_O = 2.5$ V,	$R_S = 50\ \Omega$		83		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V,	$V_{IC} = V_{DD}/2$,	No load		95		dB
I_{DD}	Supply current (four amplifiers)	$V_O = 2.5$ V,	No load			0.8		mA

† Referenced to 2.5 V

TLC2264Y electrical characteristics at $V_{DD\pm} = \pm5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLC2264Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$	$R_S = 50\ \Omega$,			300		µV
I_{IO}	Input offset current					0.5		pA
I_{IB}	Input bias current					1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert \le 5$ mV,	$R_S = 50\ \Omega$			−5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	$I_O = -20$ µA				4.99		V
		$I_O = -100$ µA				4.94		
		$I_O = -400$ µA				4.85		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$,	$I_{OL} = 50$ µA			−4.99		V
		$V_{IC} = 0$,	$I_{OL} = 500$ µA			−4.91		
		$V_{IC} = 0$,	$I_{OL} = 4$ mA			−4.1		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V	$R_L = 50$ kΩ			200		V/mV
			$R_L = 1$ MΩ			1000		
$r_{i(d)}$	Differential input resistance					10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance					10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V,	$V_O = 0$,	$R_S = 50\ \Omega$		88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.2$ V to ±8 V,	$V_{IC} = 0$,	No load		95		dB
I_{DD}	Supply current (four amplifiers)	$V_O = 0$,	No load			0.85		mA

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

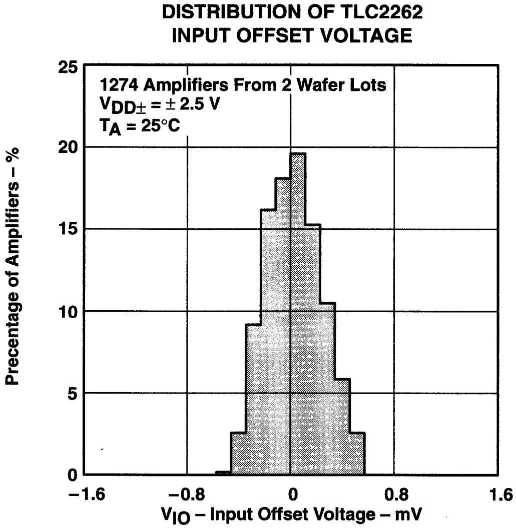


Figure 2

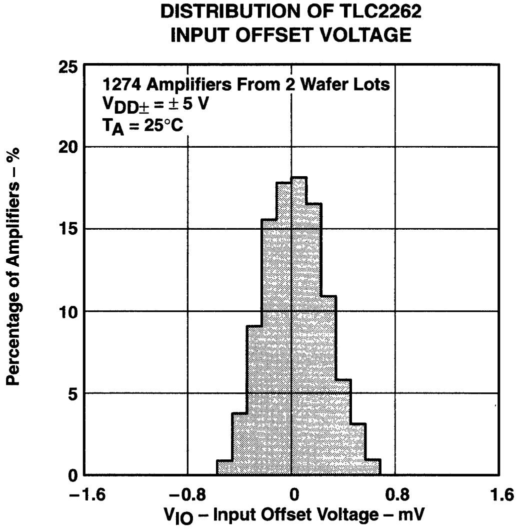


Figure 3

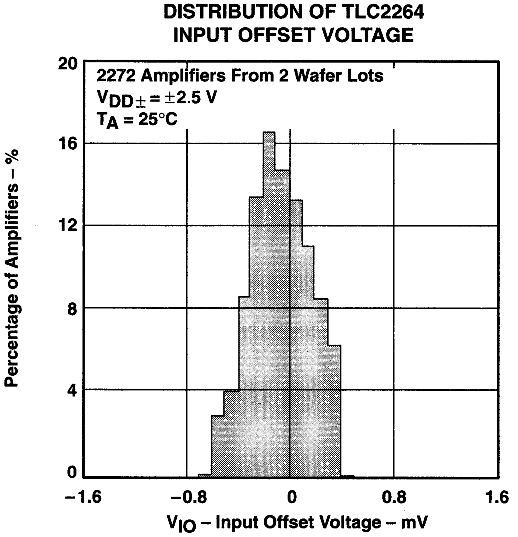


Figure 4

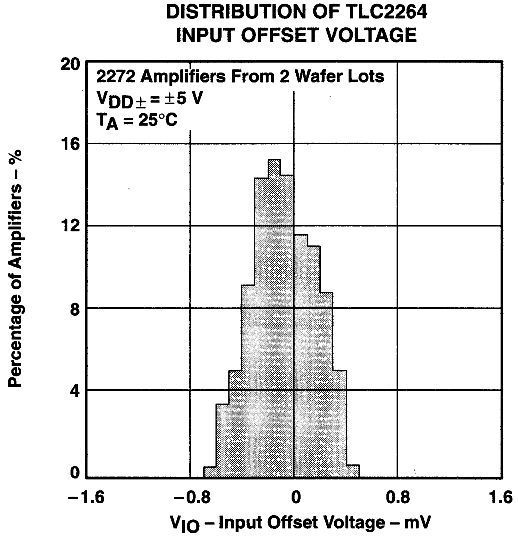
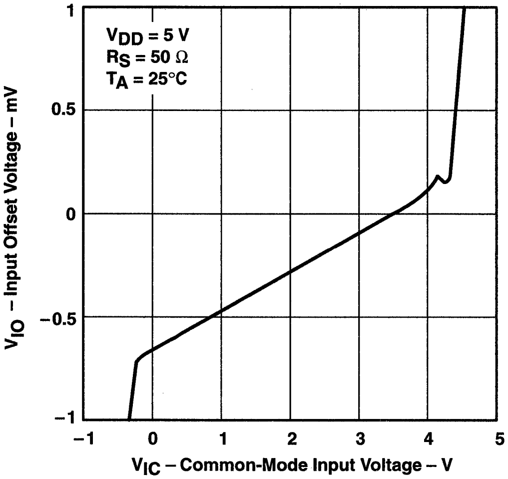


Figure 5

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 6

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

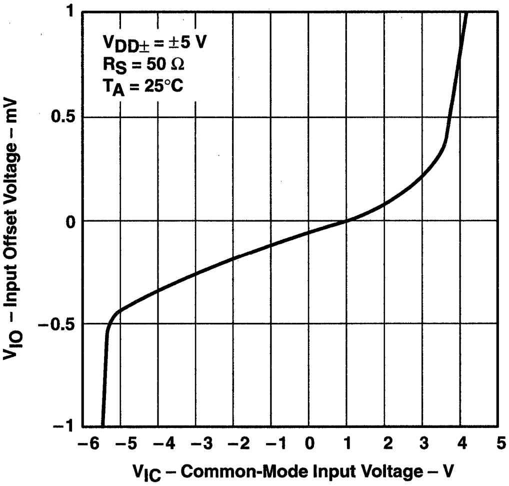


Figure 7

DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

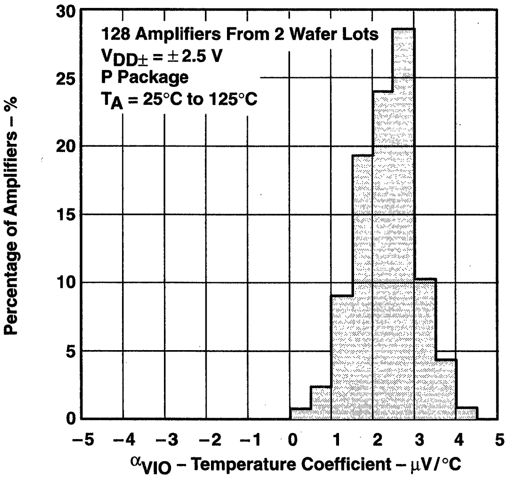


Figure 8

DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

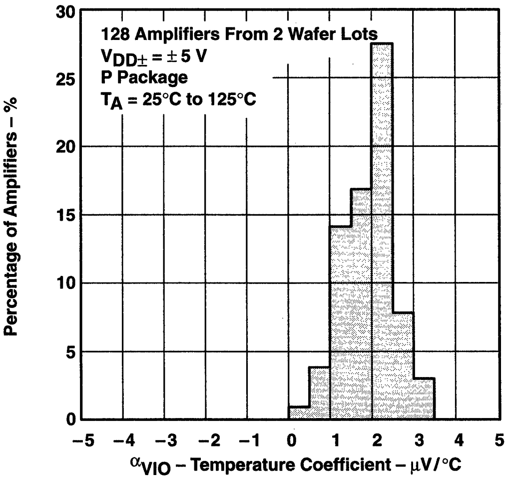


Figure 9

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

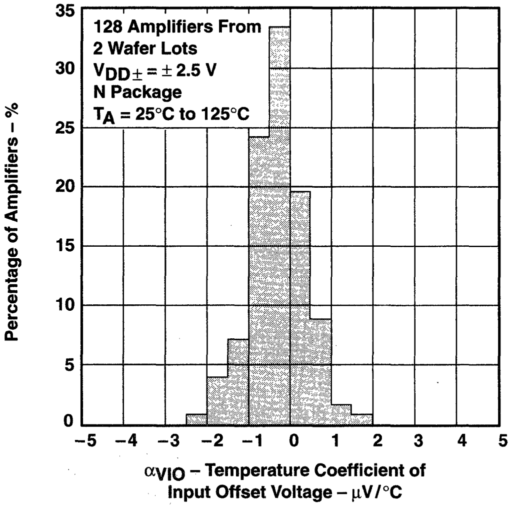

Figure 10

DISTRIBUTION OF TLC2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

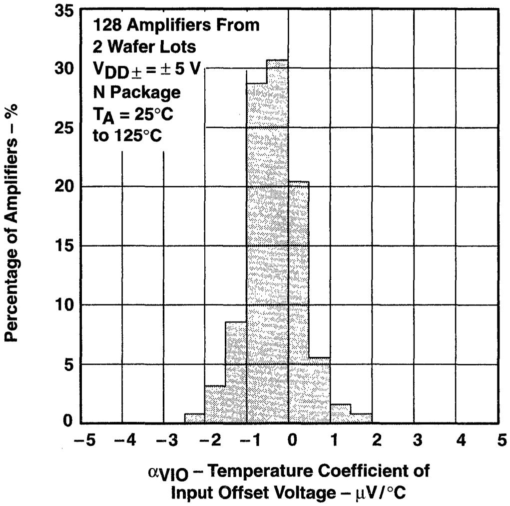

Figure 11

INPUT BIAS AND INPUT OFFSET CURRENTS†
vs
FREE-AIR TEMPERATURE

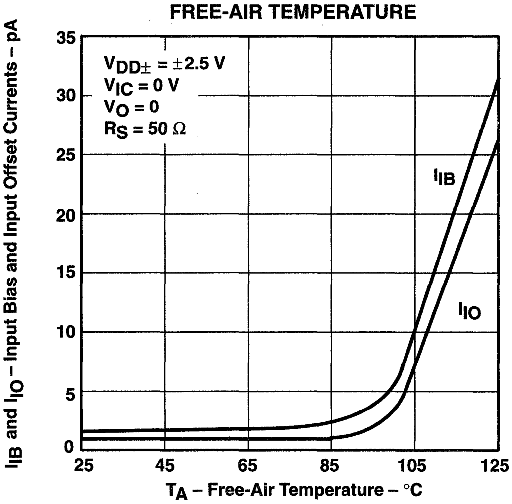

Figure 12

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

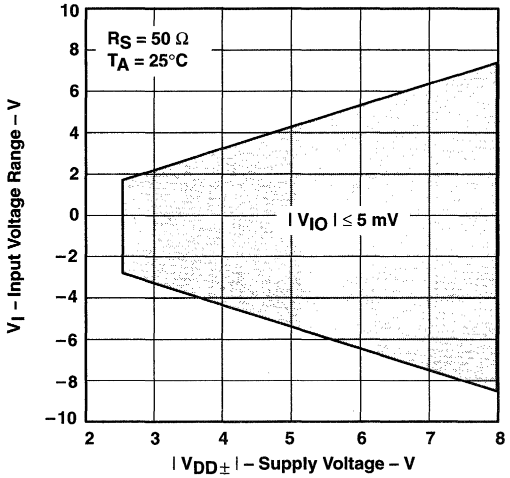

Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE†‡
vs
FREE-AIR TEMPERATURE

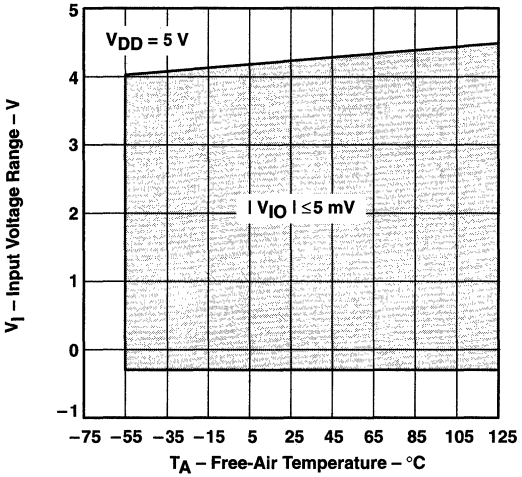

Figure 14

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

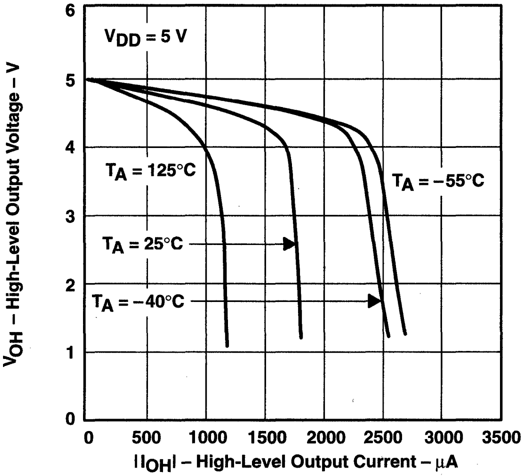

Figure 15

LOW-LEVEL OUTPUT VOLTAGE‡
vs
LOW-LEVEL OUTPUT CURRENT

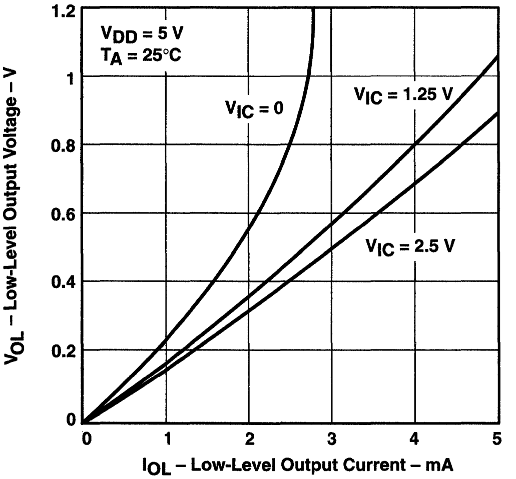

Figure 16

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

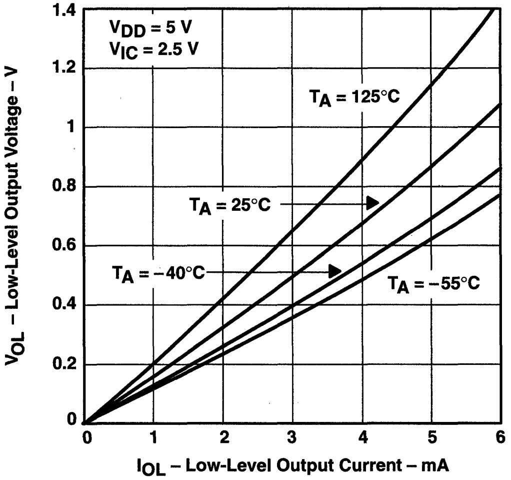

Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE OUTPUT VOLTAGE† vs OUTPUT CURRENT

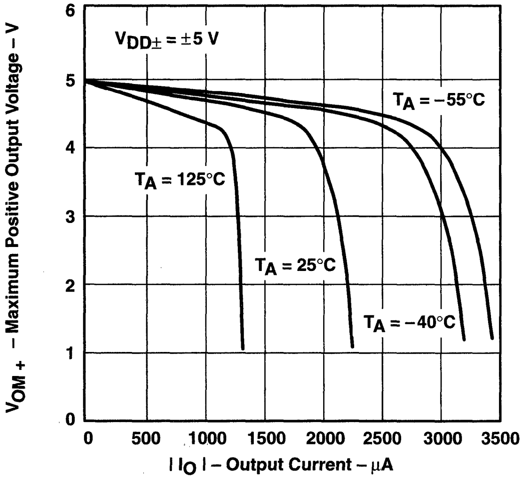


Figure 18

MAXIMUM NEGATIVE OUTPUT VOLTAGE† vs OUTPUT CURRENT

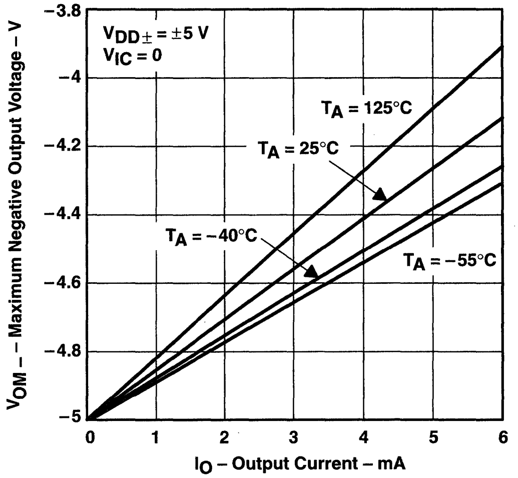
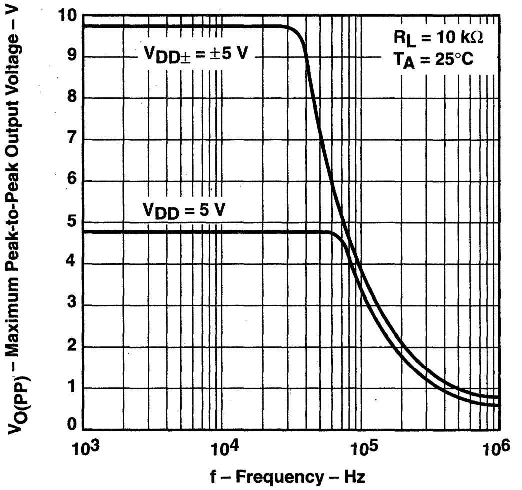


Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE†‡ vs FREQUENCY



‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

Figure 20

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

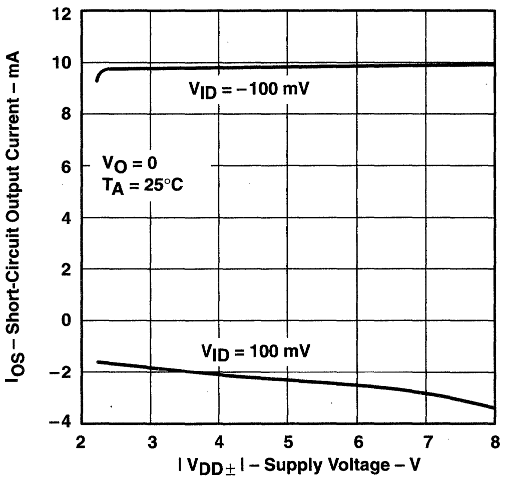


Figure 21

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT† vs FREE-AIR TEMPERATURE

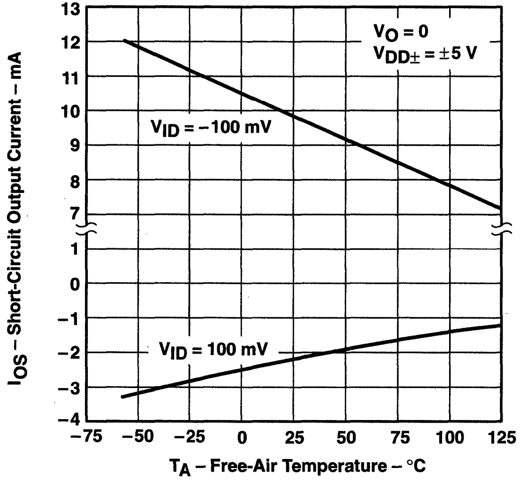

Figure 22

OUTPUT VOLTAGE‡ vs DIFFERENTIAL INPUT VOLTAGE

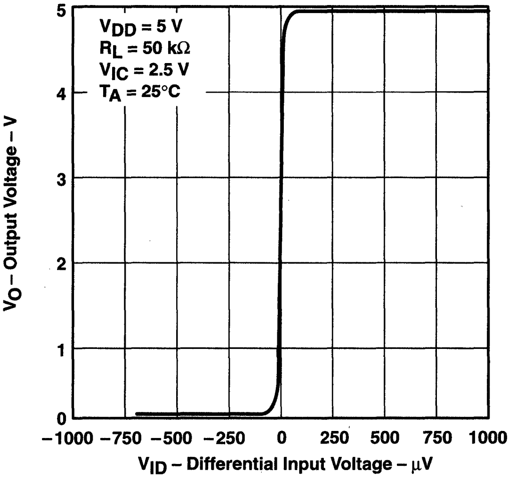

Figure 23

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

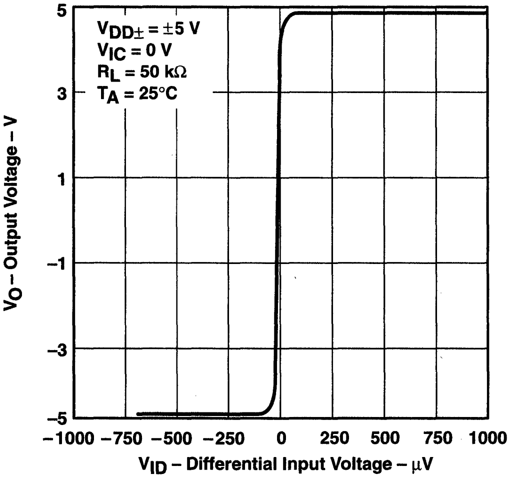

Figure 24

DIFFERENTIAL GAIN‡ vs LOAD RESISTANCE

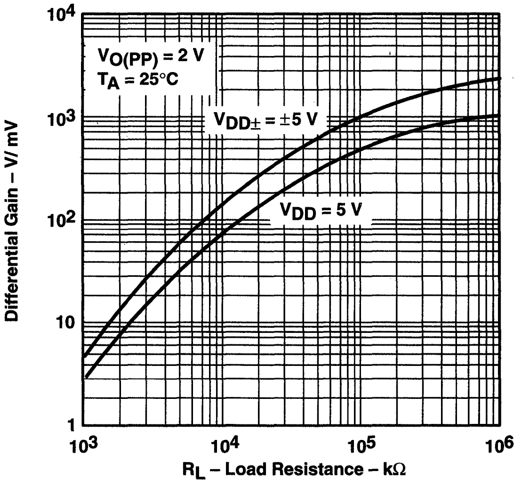

Figure 25

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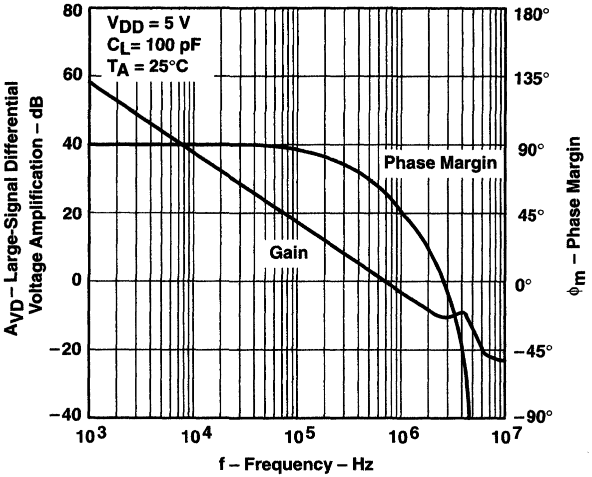
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

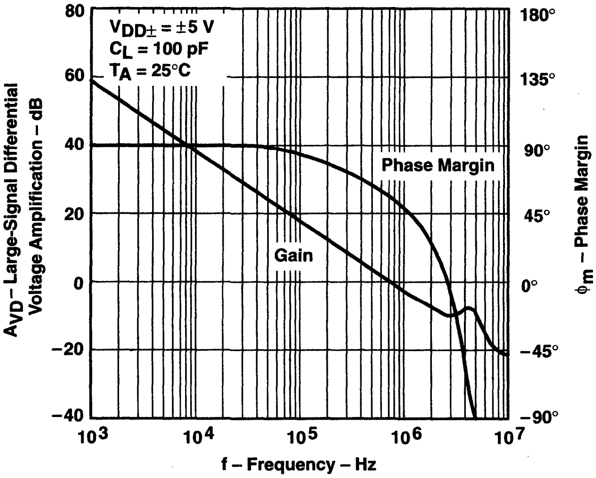


Figure 27

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡ vs FREE-AIR TEMPERATURE

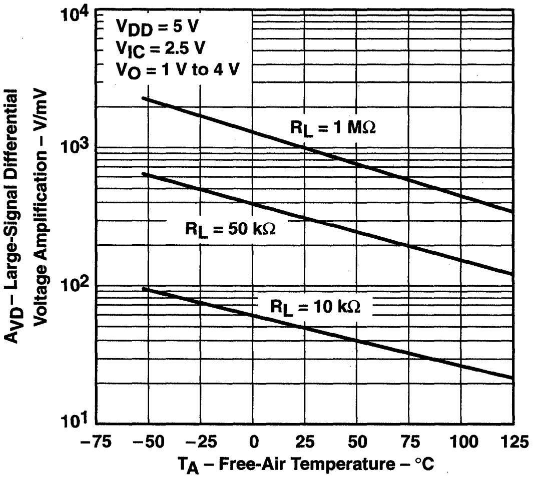


Figure 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

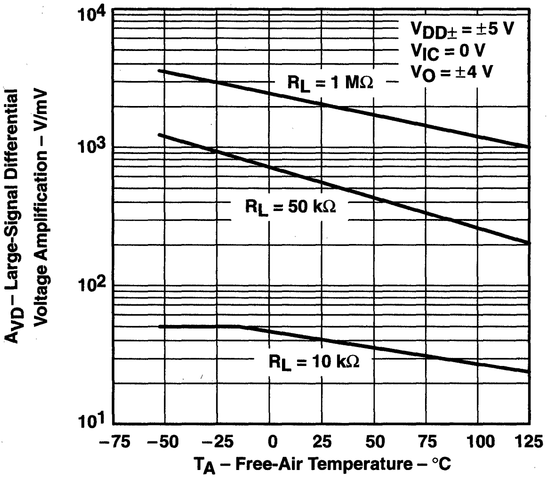


Figure 29

OUTPUT IMPEDANCE‡ vs FREQUENCY

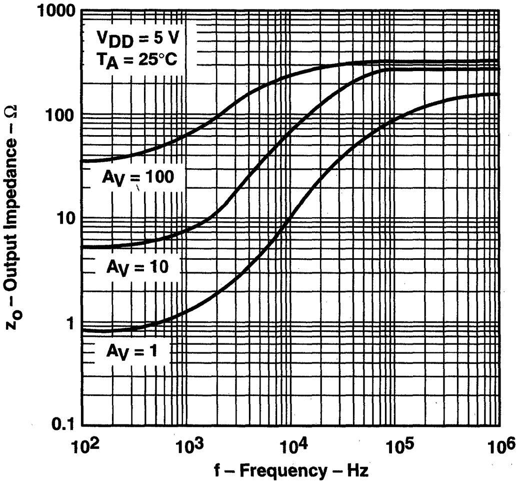


Figure 30

OUTPUT IMPEDANCE vs FREQUENCY

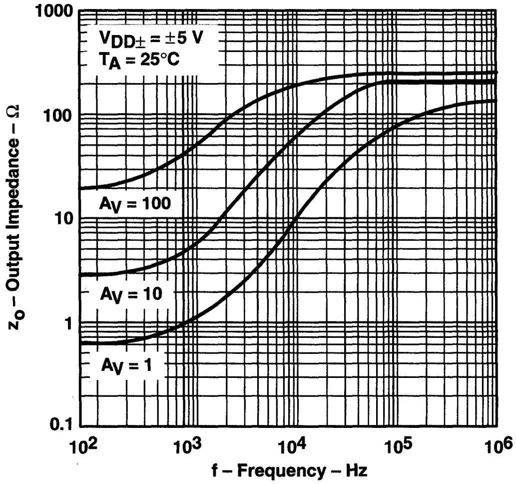


Figure 31

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO† vs FREQUENCY

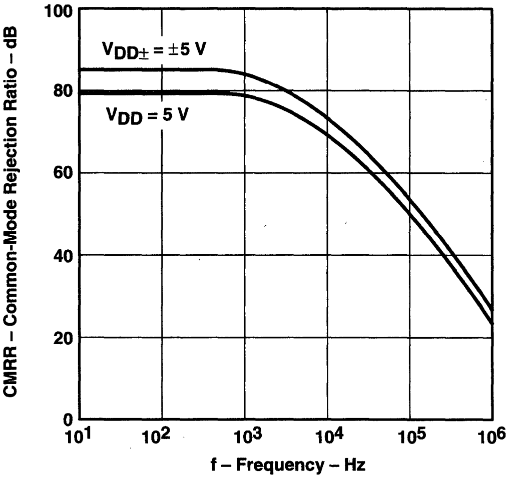

Figure 32

COMMON-MODE REJECTION RATIO†‡ vs FREE-AIR TEMPERATURE

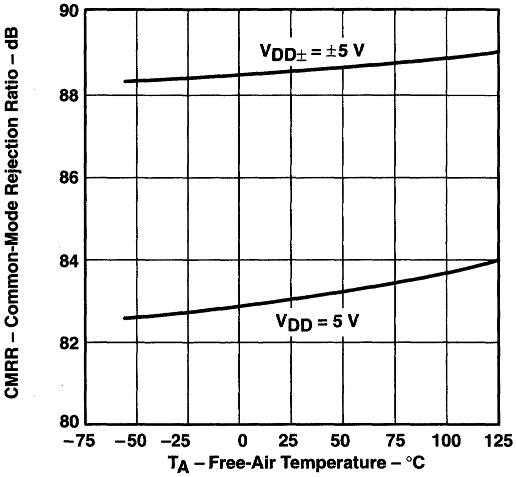

Figure 33

SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY

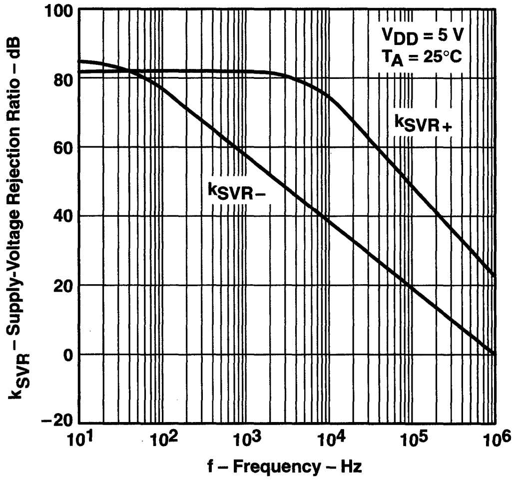

Figure 34

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

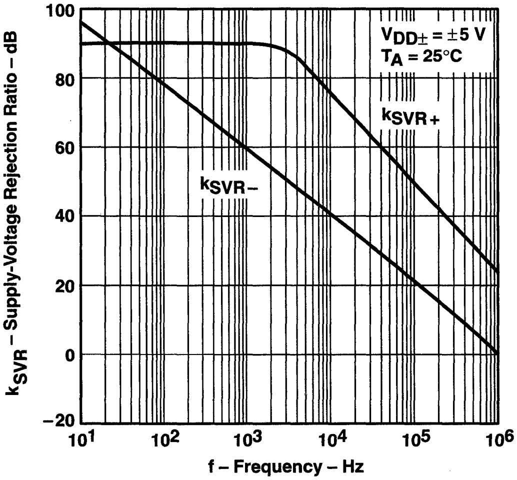

Figure 35

† For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

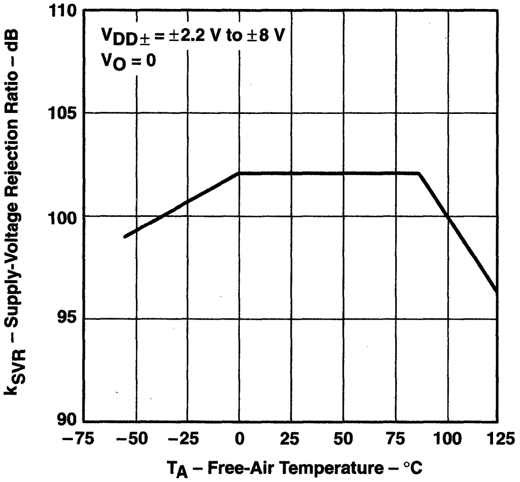

Figure 36

TLC2262
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

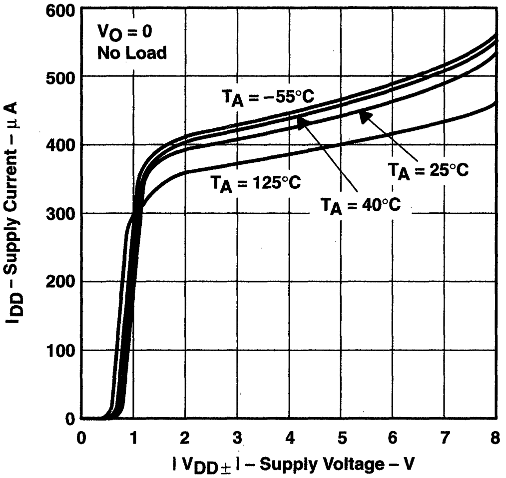

Figure 37

TLC2264
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

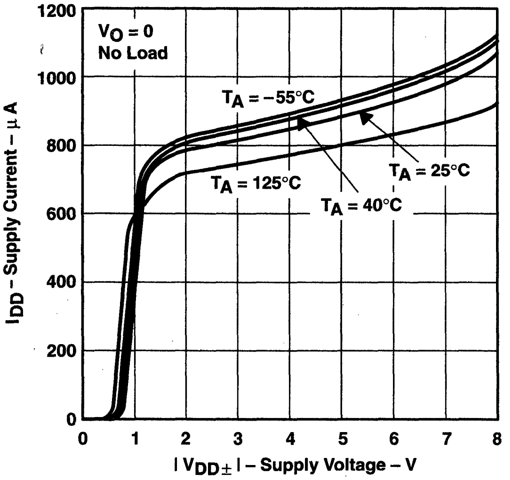

Figure 38

TLC2262
SUPPLY CURRENT†‡
vs
FREE-AIR TEMPERATURE

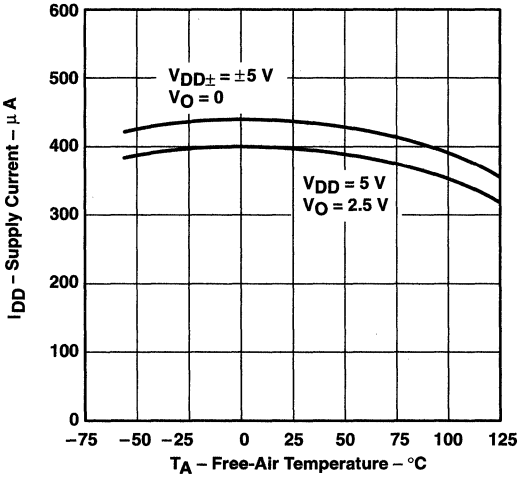

Figure 39

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

TLC2264
SUPPLY CURRENT†‡
vs
FREE-AIR TEMPERATURE

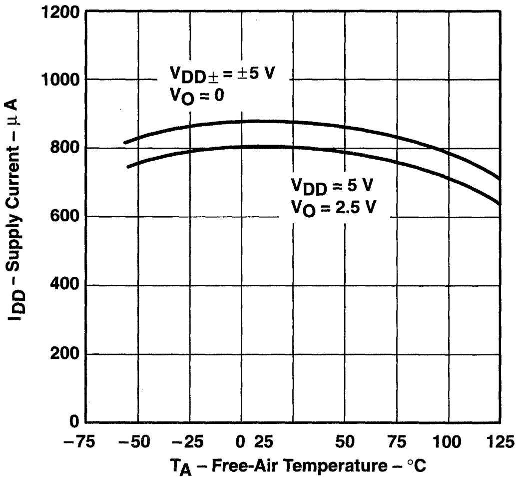

Figure 40

SLEW RATE‡
vs
LOAD CAPACITANCE

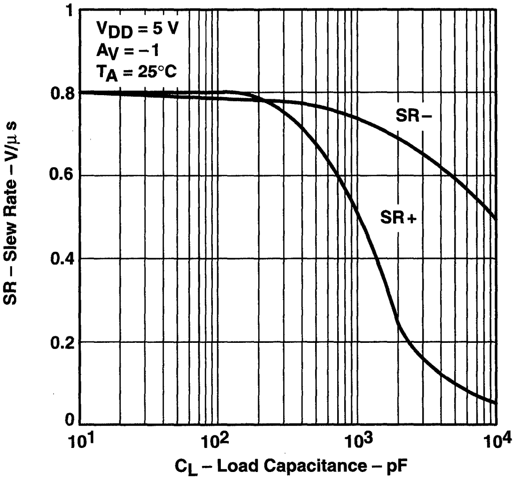

Figure 41

SLEW RATE†‡
vs
FREE-AIR TEMPERATURE

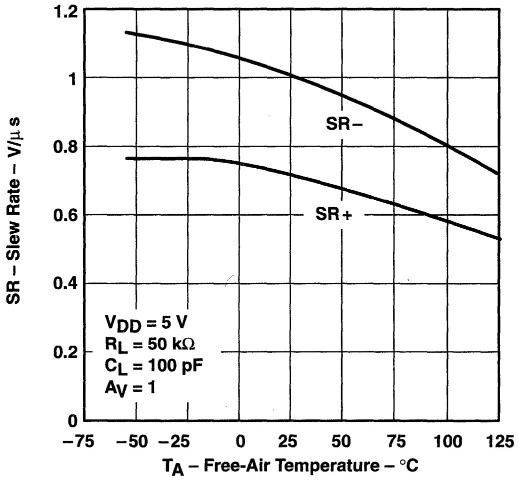

Figure 42

INVERTING LARGE-SIGNAL PULSE RESPONSE‡

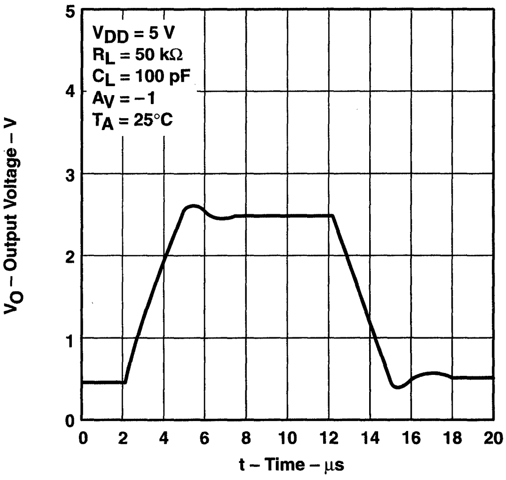

Figure 43

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

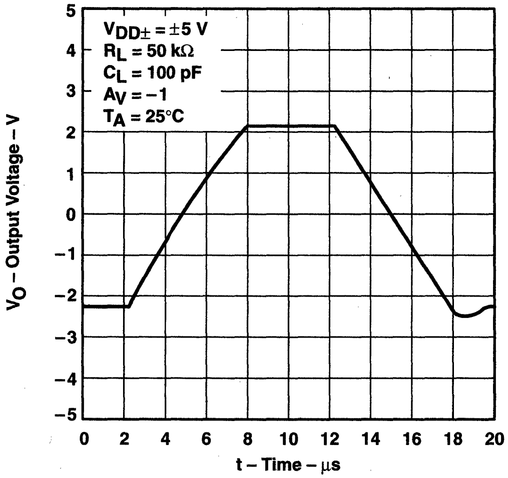

Figure 44

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

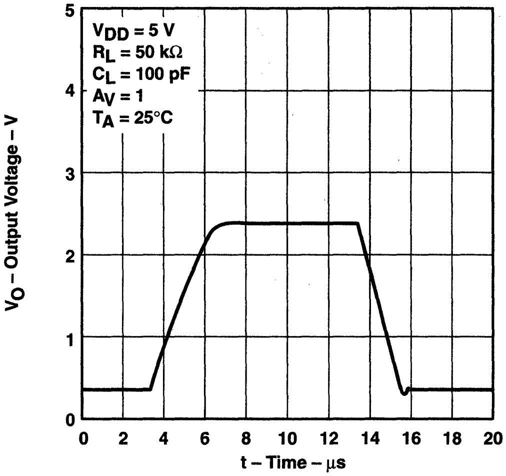

Figure 45

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

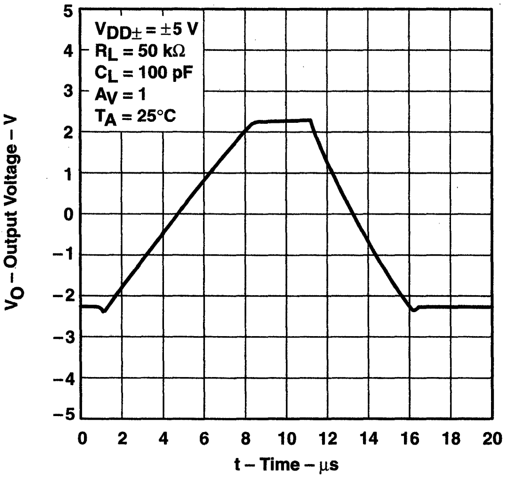

Figure 46

INVERTING SMALL-SIGNAL PULSE RESPONSE†

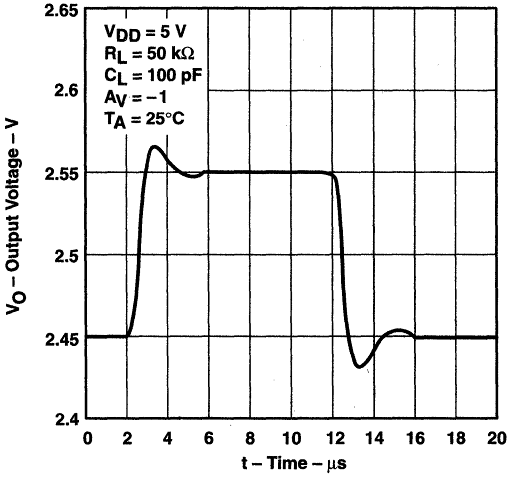

Figure 47

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† For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

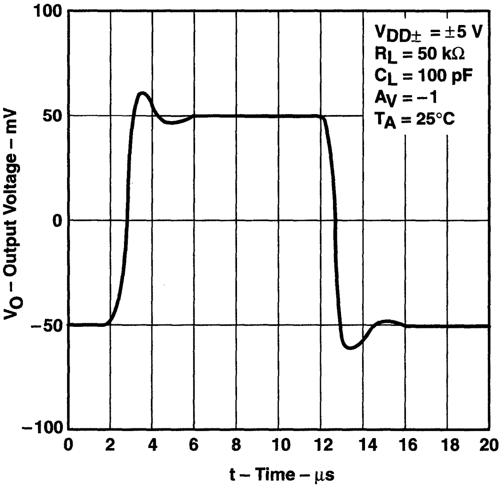

Figure 48

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

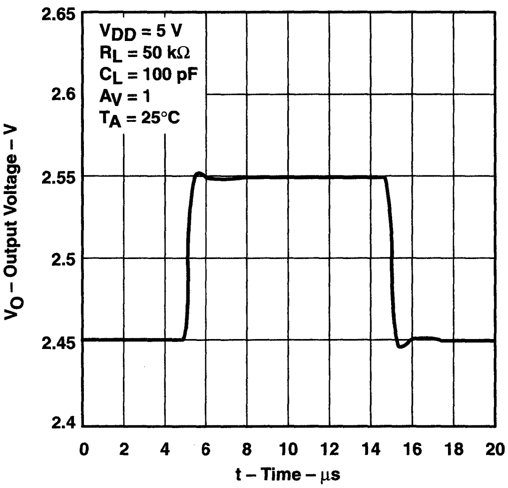

Figure 49

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

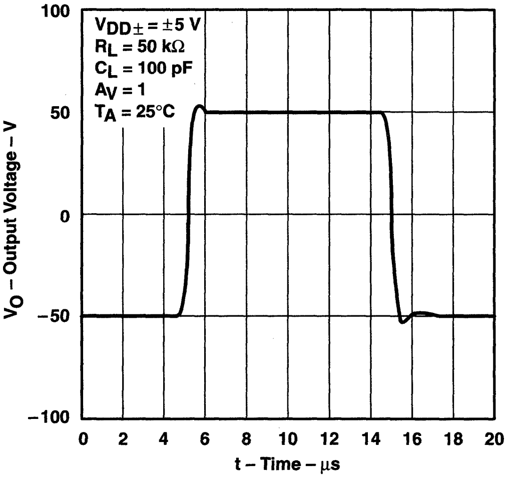

Figure 50

EQUIVALENT INPUT NOISE VOLTAGE† vs FREQUENCY

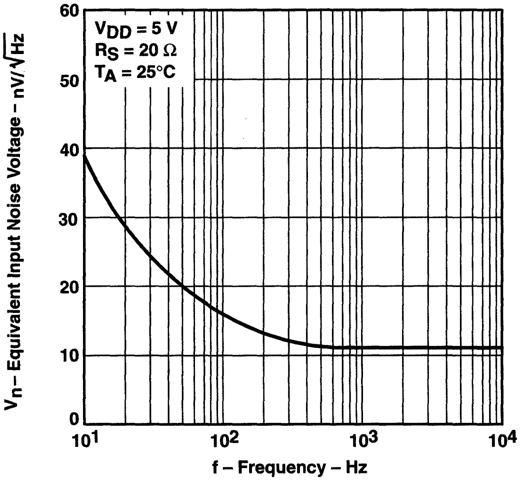

Figure 51

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† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

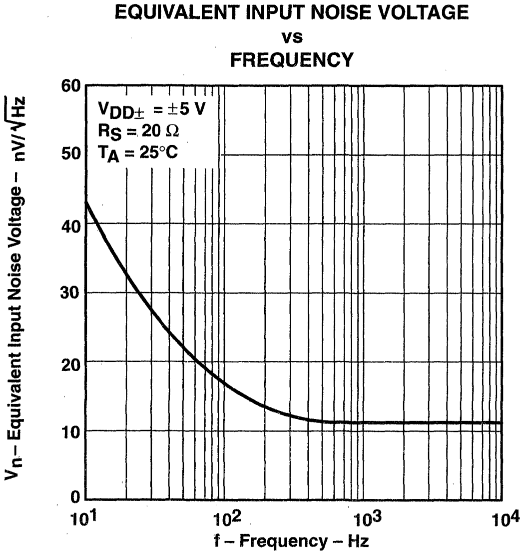

Figure 52

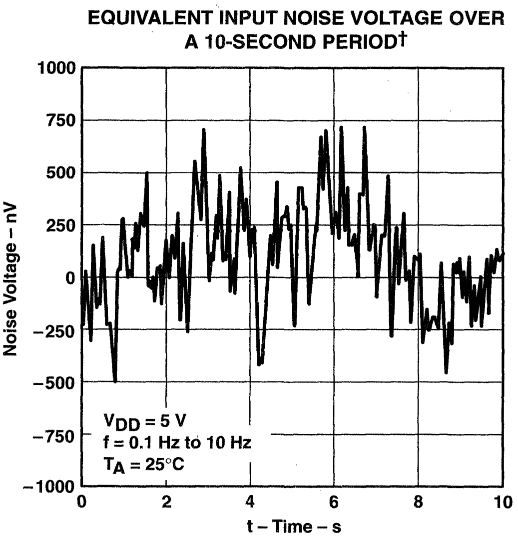

Figure 53

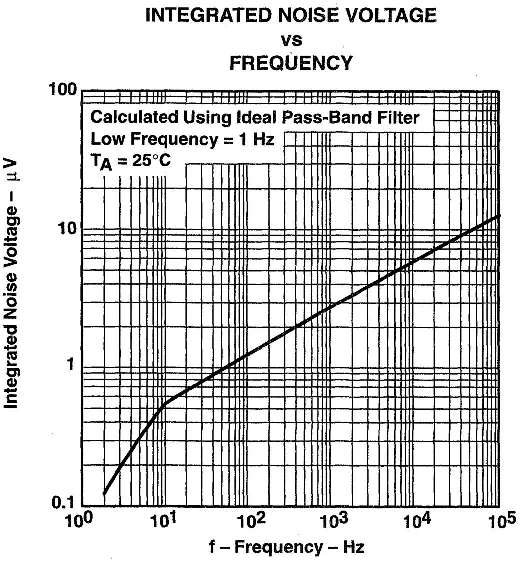

Figure 54

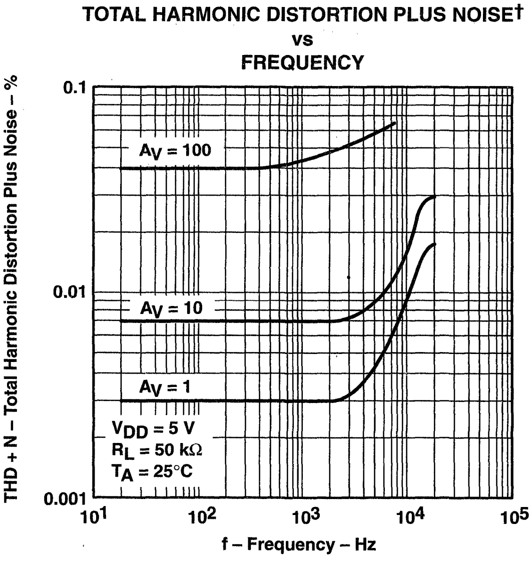

Figure 55

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† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

**GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE**

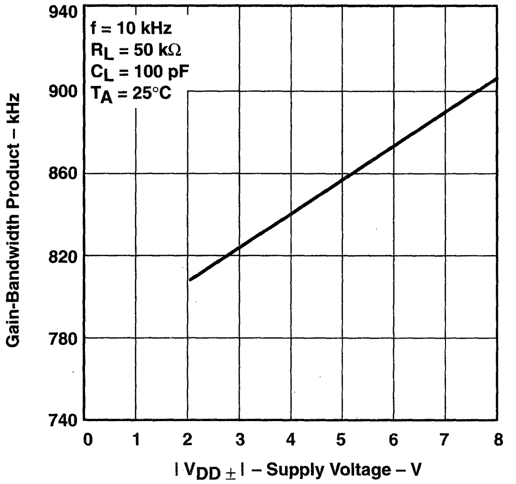

Figure 56

**GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE**

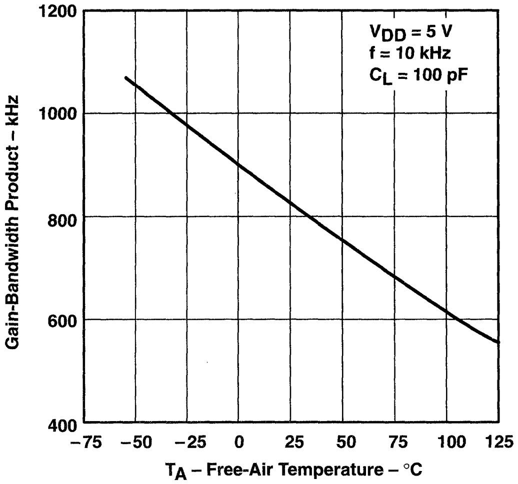

Figure 57

**PHASE MARGIN
vs
LOAD CAPACITANCE**

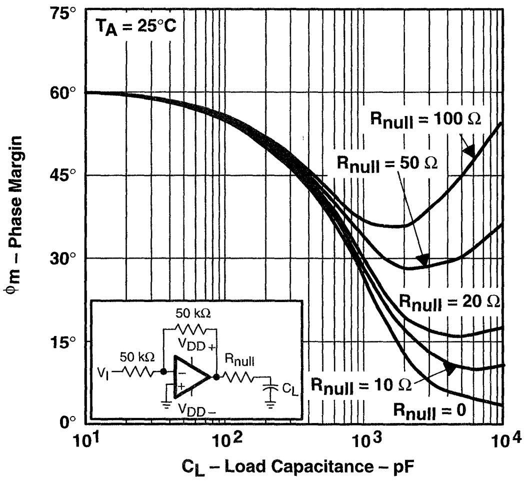

Figure 58

**GAIN MARGIN
vs
LOAD CAPACITANCE**

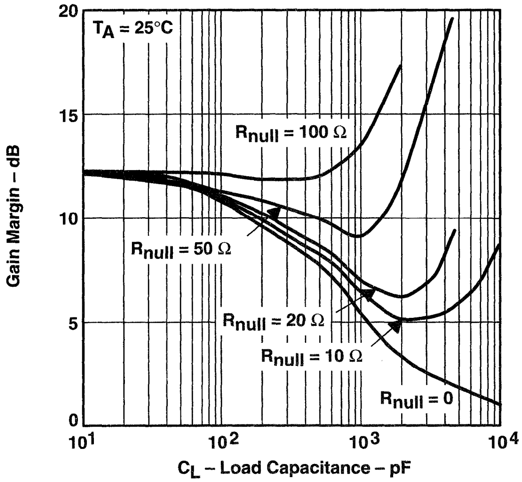

Figure 59

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH†
vs
LOAD CAPACITANCE

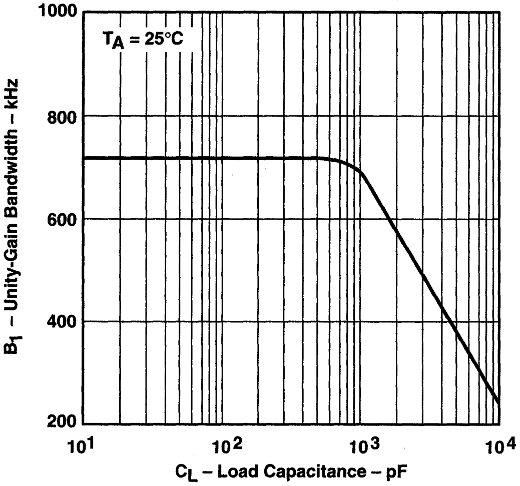

Figure 60

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE

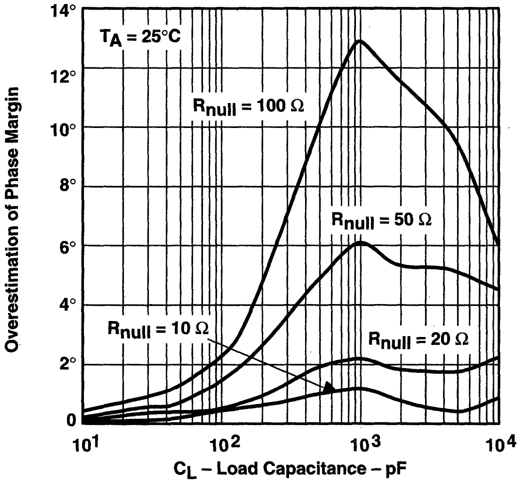

Figure 61

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† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 52 and Figure 53 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 56) improves the gain and phase margins when driving large capacitive loads. Figure 52 and Figure 53 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\Theta_{m1} = \tan^{-1}\left(2 \times \pi \times \mathrm{UGBW} \times R_{null} \times C_L\right) \qquad (1)$$

where :

$\Delta\Theta_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 54). To use equation 1, UGBW must be approximated from Figure 54.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 55. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation 2.

$$F = \frac{1}{1 + g_m \times R_{null}} \qquad (2)$$

where :

F = factor reducing frequency of pole
g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
R_{null} = output series resistance

For the TLC226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with C_L: at $C_L = 10$ pF, use 70 MHz, at $C_L = 1000$ pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation in equation 1 to better approximate the improvement in phase margin.

APPLICATION INFORMATION

driving large capacitive loads (continued)

$$\Delta\Theta_{m2} = \tan^{-1}\left[\frac{UGBW}{(F \times P_2)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \tag{3}$$

where :

$\Delta\Theta_{m2}$ = reduction in phase margin
UGBW = unity-gain bandwidth frequency
F = factor from equation 2
P_2 = unadjusted pole (70 MHz @ 10 pF, 7 MHz @ 100 pF, etc.)

Using these equations with Figure 54 and Figure 55 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

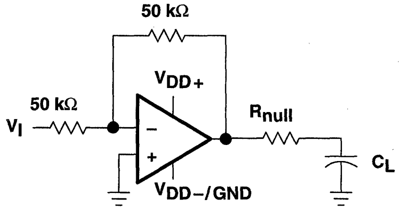


Figure 62. Series-Resistance Circuit

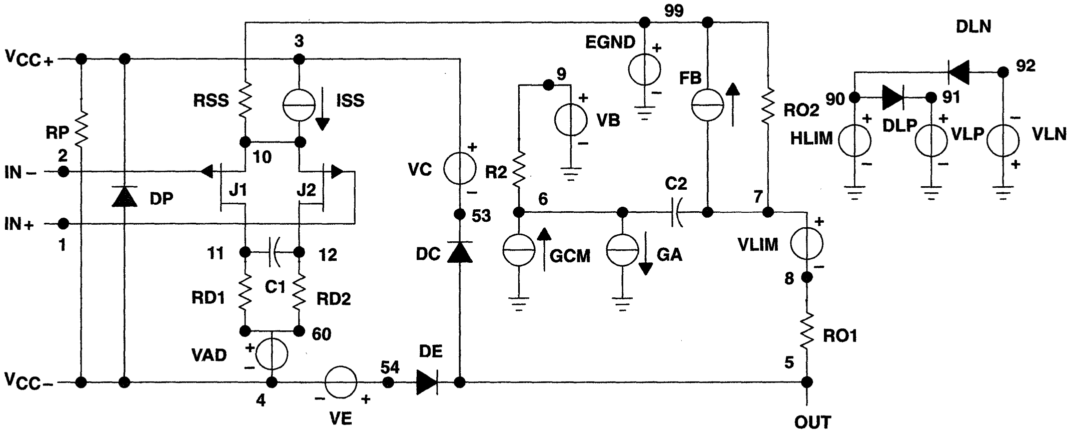
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 57 are generated using the TLC226x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



```
.SUBCKT TLC226x 1 2 3 4 5
        C1      11   12   3.560E–12
        C2      6    7    15.00E–12
        DC      5    53   DX
        DE      54   5    DX
        DLP     90   91   DX
        DLN     92   90   DX
        DP      4    3    DX
        EGND    99   0    POLY (2) (3,0) (4,0) 0 .5 .5
        FB      7    99   POLY (5) VB VC VE VLP
        + VLN 0 21.04E6 –30E6 30E6 30E6 –30E6
        GA      6    0    11     12 47.12E–6
        GCM     0    6    10     99 4.9E–9
        ISS     3    10   DC 8.250E–6
        HLIM    90   0    VLIM 1K
        J1      11   2    10 JX
        J2      12   1    10 JX
        R2      6    9    100.0E3
        RD1     60   11   21.22E3
        RD2     60   12   21.22E3
        R01     8    5    120
        R02     7    99   120
        RP      3    4    26.04E3
        RSS     10   99   24.24E6
        VAD     60   4    –.6
        VB      9    0    DC 0
        VC      3    53   DC .65
        VE      54   4    DC .65
        VLIM    7    8    DC 0
        VLP     91   0    DC 1.4
        VLN     0    92   DC 9.4
        .MODEL DX D (IS=800.0E–18)
        .MODEL JX PJF (IS=500.0E–15 BETA=281E–6
        + VTO=–.065)
        .ENDS
```

Figure 63. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

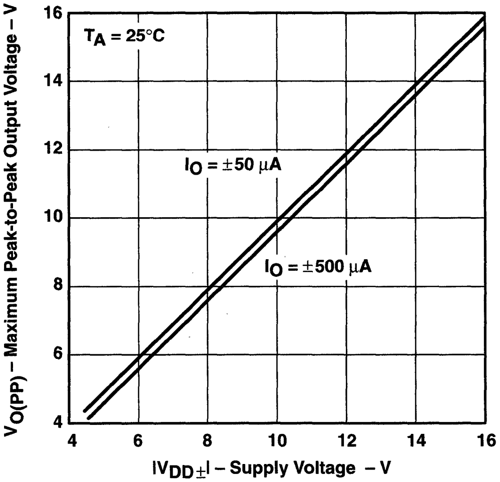
TLC227x, TLC227xA, TLC227xY
Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS190 – FEBRUARY 1997

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 9 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **High-Gain Bandwidth . . . 2.2 MHz Typ**
- **High Slew Rate . . . 3.6 V/μs Typ**
- **Low Input Offset Voltage**
  950 μV Max at T_A = 25°C
- **Macromodel Included**
- **Performance Upgrades for the TS272, TS274, TLC272, and TLC274**

description

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE



The TLC2272 and TLC2274 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC227x family offers 2 MHz of bandwidth and 3 V/μs of slew rate for higher speed applications. These devices offer comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC227x has a noise voltage of 9 nV/√Hz; two times lower than competitive solutions.

The TLC227x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA family is available and has a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2272/4 also makes great upgrades to the TLC272/4 or TS272/4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see TLV2432 and TLV2442 devices. If the design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

TLC2272 AVAILABLE OPTIONS

T_A	V_{IO}max At 25°C	PACKAGED DEVICES			CHIP FORM§ (Y)
		SMALL OUTLINE† (D)	PLASTIC DIP (P)	TSSOP‡ (PW)	
0°C to 70°C	950 µV 2.5 mV	TLC2272ACD TLC2272CD	TLC2272ACP TLC2272CP	TLC2272CPWLE	TLC2272Y
−40°C to 85°C	950 µV 2.5 mV	TLC2272AID TLC2272ID	TLC2272AIP TLC2272IP	—	—
−55°C to 125°C	950 µV 2.5 mV	TLC2272AMD TLC2272MD	TLC2272AMP TLC2272MP	—	—

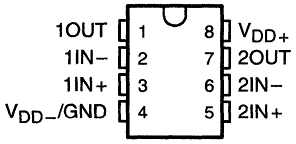
† The D packages are available taped and reeled. Add R suffix to the device type (e.g., TLC2272CDR).
‡ The PW package is available only left-end taped and reeled.
§ Chips are tested at 25°C.

TLC2274 AVAILABLE OPTIONS

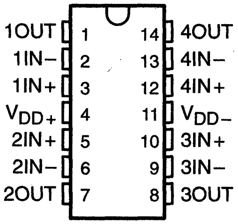
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM§ (Y)
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP‡ (PW)	
0°C to 70°C	950 µV 2.5 mV	TLC2274ACD TLC2274CD	—	—	TLC2274ACN TLC2274CN	— TLC2274CPWLE	TLC2274Y
−40°C to 85°C	950 µV 2.5 mV	TLC2274AID TLC2274ID	—	—	TLC2274AIN TLC2274IN	— TLC2274IPWLE	—
−55°C to 125°C	950 µV 2.5 mV	TLC2274AMD TLC2274MD	TLC2274AMFK TLC2274MFK	TLC2274AMJ TLC2274MJ	TLC2274AMN TLC2274MN	—	—

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2274CDR).
‡ The PW package is available only left-end taped and reeled.
§ Chips are tested at 25°C.

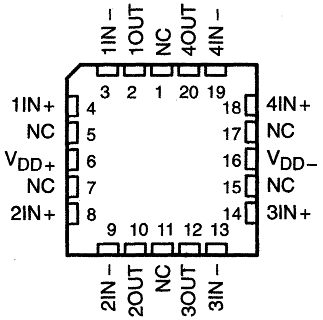
TLC2272
D, P, OR PW PACKAGE
(TOP VIEW)



TLC2274
D, J, N, OR PW PACKAGE
(TOP VIEW)



TLC2274
FK PACKAGE
(TOP VIEW)

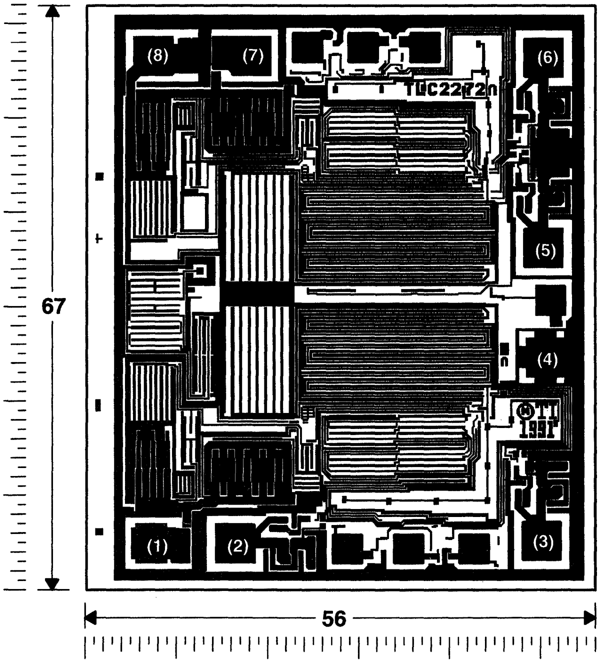


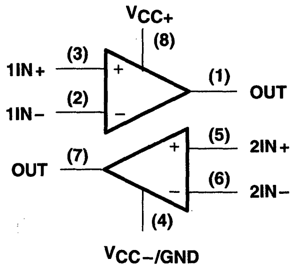
NC – No internal connection

TLC2272Y chip information

These chips, when properly assembled, display characteristics similar to the TLC2272C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

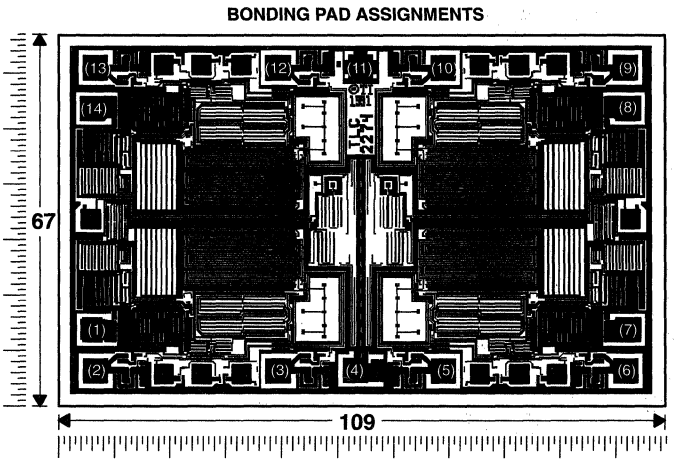
TOLERANCES ARE ±10%.

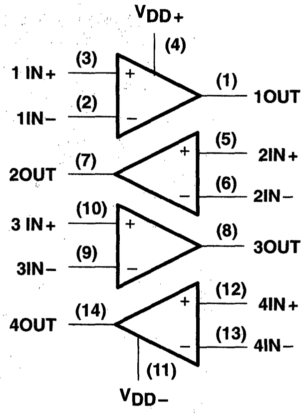
ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TLC2274Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2274C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

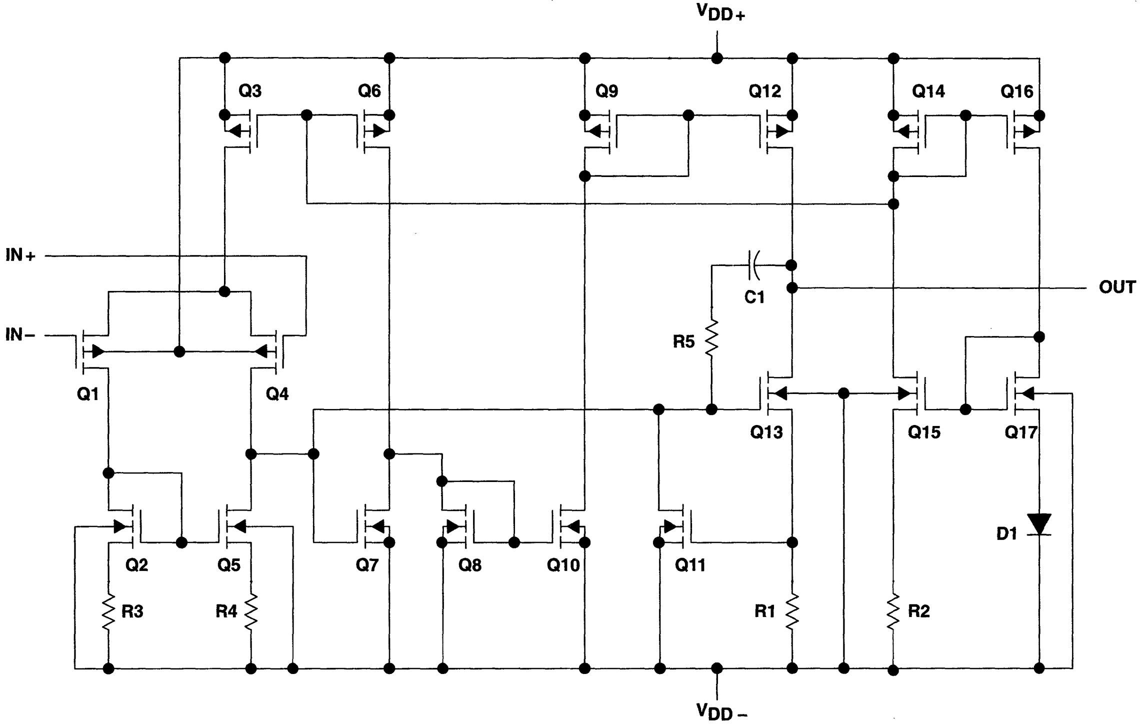
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	**TLC2272**	**TLC2274**
Transistors	38	76
Resistors	26	52
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1) .... 8 V
Supply voltage, V_{DD-} (see Note 1) .... –8 V
Differential input voltage, V_{ID} (see Note 2) .... ±16 V
Input voltage, V_I (any input, see Note 1) .... V_{DD-} – 0.3 V to V_{DD+}
Input current, I_I (any input) .... ±5 mA
Output current, I_O .... ±50 mA
Total current into V_{DD+} .... ±50 mA
Total current out of V_{DD-} .... ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix .... 0°C to 70°C
I suffix .... –40°C to 85°C
M suffix .... –55°C to 125°C
Storage temperature range .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P or PW package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package .... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current will flow if input is brought below V_{DD-} – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	337 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW–8	525 mW	4.2 mW/°C	336 mW	—	—
PW–14	700 mW	5.6 mW/°C	448 mW	364 mW	—

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-1.5$	V_{DD-}	$V_{DD+}-1.5$	V_{DD-}	$V_{DD+}-1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-1.5$	V_{DD-}	$V_{DD+}-1.5$	V_{DD-}	$V_{DD+}-1.5$	V
Operating free-air temperature, T_A	0	70	–40	85	–55	125	°C

TLC2272C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2272C			TLC2272AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD±}$ = ±2.5 V, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, |V_{IO}| ≤ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA	25°C		4.99			4.99		V
		I_{OH} = −200 µA	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		I_{OH} = −1 mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
			Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 10 kΩ‡	25°C	15	35		15	35		V/mV
			Full range	15			15			
		R_L = 1 mΩ‡	25°C		175			175		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	75		70	75		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		2.2	3		2.2	3	mA
			Full range			3			3	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡,	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

TLC2272C electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A†	TLC2272C			TLC2272AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA	25°C		4.99			4.99		V
		I_O = −200 µA	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		I_O = −1 mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 µA	25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 µA	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = 5 mA	25°C	−3.5	−4.1		−3.5	−4.1		
			Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	25	50		25	50		V/mV
			Full range	25			25			
		V_O = ±4 V, R_L = 1 mΩ	25°C		300			300		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 to 2.7 V, V_O = 0 V, R_S = 50 Ω	25°C	75	80		75	80		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = 2.2 V to ±8 V, V_{IC} = 0, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 0 V, No load	25°C		2.4	3		2.4	3	mA
			Full range			3			3	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion pulse duration	$V_O = \pm 2.3$ V, f = 20 kHz, $R_L = 10$ kΩ	$A_V = 1$	25°C		0.0011%			0.0011%		
			$A_V = 10$			0.004%			0.004%		
			$A_V = 100$			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $A_V = 1$, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		0.54			0.54		MHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 10$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is 0°C to 70°C.

TLC2274C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2274C			TLC2274AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50Ω, $\lvert V_{IO}\rvert \le$ 5 m V,	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA	25°C		4.99			4.99		V
		I_{OH} = −200 µA	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		I_{OH} = −1 mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
			Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 10 kΩ‡	25°C	15	35		15	35		V/mV
			Full range	15			15			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 mΩ‡	25°C		175			175		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50Ω	25°C	70	75		70	75		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		4.4	6		4.4	6	mA
			Full range			6			6	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274C			TLC2274AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C	2.3	3.6		2.3	3.6		V/µs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1			1		µV
		f = 0.1 to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		1			1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		µs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

TLC2274C electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2274C			TLC2274AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO}\rvert \le$ 5 mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA	25°C		4.99			4.99		V
		I_O = −200 µA	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		I_O = −1 mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 µA	25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 µA	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = −5 mA	25°C	−3.5	−4.1		−3.5	−4.1		
			Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	25	50		25	50		V/mV
			Full range	25			25			
		V_O = ±4 V, R_L = 1 MΩ	25°C		300			300		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω	25°C	75	80		75	80		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, V_{IC} = 0, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 0, No load	25°C		4.8	6		4.8	6	mA
			Full range			6			6	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2274C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274C			TLC2274AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 Hz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, f = 20 kHz, $R_L = 10$ kΩ	$A_V = 1$	25°C		0.0011%			0.0011%		
			$A_V = 10$			0.004%			0.004%		
			$A_V = 100$			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $A_V = 1$, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		0.54			0.54		MHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 10$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is 0°C to 70°C.

TLC2272I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5V R_S = 50 Ω	25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.99			4.99		V
		I_{OH} = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_{OH} = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
				Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	15	35		15	35		V/mV
				Full range	15			15			
			R_L = 1 mΩ‡	25°C		175			175		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		2.2	3		2.2	3	mA
				Full range			3			3	

† Full range is – 40°C to 85°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.3	3.6		2.3	3.6		V/µs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		µV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		µs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

TLC2272I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO} \rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.99			4.99		V
		I_O = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0,	I_O = 50 µA	25°C		−4.99			−4.99		V
		V_{IC} = 0,	I_O = 500 µA	25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0,	I_O = 5 mA	25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25°C	25	50		25	50		V/mV
				Full range	25			25			
			R_L = 1 mΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = $V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		2.4	3		2.4	3	mA
				Full range			3			3	

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C	2.3	3.6		2.3	3.6		V/µs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		$nV\sqrt{Hz}$
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		µV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		$fA\sqrt{Hz}$
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V $R_L = 10$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.0011%			0.0011%		
			$A_V = 10$			0.004%			0.004%		
			$A_V = 100$			0.03%			0.03%		
	Gain-bandwidth product	f =10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $A_V = 1$, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		0.54			0.54		MHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 10$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		1.5			1.5		µs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is −40°C to 85°C.

TLC2274I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2274I			TLC2274AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20$ µA	25°C		4.99			4.99		V
		$I_{OH} = -200$ µA	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		$I_{OH} = -1$ mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V, $I_{OL} = 50$ µA	25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V, $I_{OL} = 500$ µA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		$V_{IC} = 2.5$ V, $I_{OL} = 5$ mA	25°C		0.9	1.5		0.9	1.5	
			Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 10$ kΩ‡	25°C	15	35		15	35		V/mV
			Full range	15			15			
		$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 1$ MΩ‡	25°C		175			175		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, $A_V = 10$	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 50\ \Omega$	25°C	70	75		70	75		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5$ V, No load	25°C		4.4	6		4.4	6	mA
			Full range			6			6	

† Full range is – 40°C to 85°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274I			TLC2274AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.3	3.6		2.3	3.6		V/µs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		µV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		µs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

TLC2274I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2274I			TLC2274AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99			4.99		V
		$I_O = -200\ \mu A$	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		$I_O = -1$ mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 5$ mA	25°C	−3.5	−4.1		−3.5	−4.1		
			Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	25	50		25	50		V/mV
			Full range	25			25			
		$V_O = \pm 4$ V, $R_L = 1\ M\Omega$	25°C		300			300		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, $A_V = 10$	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	80		75	80		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ±8 V, $V_{IC} = 0$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		4.8	6		4.8	6	mA
			Full range			6			6	

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274I			TLC2274AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm2.3$ V, $R_L = 10$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.0011%			0.0011%		
			$A_V = 10$			0.004%			0.004%		
			$A_V = 100$			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $A_V = 1$, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		0.54			0.54		MHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 10$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is −40°C to 85°C.

TLC2272M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272M			TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω	25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\|$ ≤5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.99			4.99		V
		I_{OH} = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_{OH} = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
				Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	10	35		10	35		V/mV
				Full range	10			10			
			R_L = 1 mΩ‡	25°C		175			175		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		2.2	3		2.2	3	mA
				Full range			3			3	

† Full range is – 55°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272M			TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡ C_L = 100 pF‡		25°C	2.3	3.6		2.3	3.6		V/µs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		µV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡,	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f =10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		µs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is – 55°C to 125°C.

‡ Referenced to 2.5 V

TLC2272M electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2272M			TLC2272AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert$ ≤5 mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA	25°C		4.99			4.99		V
		I_O = −200 µA	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		I_O = −1 mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0, I_O = 50 µA	25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 µA	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		V_{IC} = 0, I_O = 5 mA	25°C	−3.5	−4.1		−3.5	−4.1		
			Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	20	50		20	50		V/mV
			Full range	20			20			
		V_O = ±4 V, R_L = 1 mΩ	25°C		300			300		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	75	80		75	80		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = 0, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		2.4	3		2.4	3	mA
			Full range			3			3	

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272M operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272M			TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C	2.3	3.6		2.3	3.6		V/µs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		µV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V $R_L = 10$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.0011%			0.0011%		
			$A_V = 10$			0.004%			0.004%		
			$A_V = 100$			0.03%			0.03%		
	Gain-bandwidth product	f =10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $A_V = 1$, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		0.54			0.54		MHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 10$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		1.5			1.5		µs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is −55°C to 125°C.

TLC2274M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2274M			TLC2274AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20$ µA	25°C		4.99			4.99		V
		$I_{OH} = -200$ µA	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		$I_{OH} = -1$ mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V, $I_{OL} = 50$ µA	25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V, $I_{OL} = 500$ µA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		$V_{IC} = 2.5$ V, $I_{OL} = 5$ mA	25°C		0.9	1.5		0.9	1.5	
			Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 10$ kΩ‡	25°C	10	35		10	35		V/mV
			Full range	10			10			
		$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 1$ MΩ‡	25°C		175			175		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, $A_V = 10$	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 50\ \Omega$	25°C	70	75		70	75		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5$ V, No load	25°C		4.4	6		4.4	6	mA
			Full range			6			6	

† Full range is – 55°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274M			TLC2274AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.3	3.6		2.3	3.6		V/µs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		µV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		µs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V

TLC2274M electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2274M			TLC2274AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99			4.99		V
		$I_O = -200\ \mu A$	25°C	4.85	4.93		4.85	4.93		
			Full range	4.85			4.85			
		$I_O = -1$ mA	25°C	4.25	4.65		4.25	4.65		
			Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 5$ mA	25°C	−3.5	−4.1		−3.5	−4.1		
			Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 10\ k\Omega$	25°C	20	50		20	50		V/mV
			Full range	20			20			
		$V_O = \pm4$ V, $R_L = 1\ M\Omega$	25°C		300			300		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, $A_V = 10$	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	80		75	80		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm$ 2.2 V to $\pm$8 V, $V_{IC} = 0$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		4.8	6		4.8	6	mA
			Full range			6			6	

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274M operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274M			TLC2274AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C	2.3	3.6		2.3	3.6		V/µs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		µV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.0011%			0.0011%		
			$A_V = 10$			0.004%			0.004%		
			$A_V = 100$			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $A_V = 1$, $R_L = 10$ kΩ, $C_L = 100$ pF		25°C		0.54			0.54		MHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 10$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		1.5			1.5		µs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unit gain	$R_L = 10$ kΩ, $C_L = 100$ pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is −55°C to 125°C.

TLC2272Y electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2274Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω		300	2500	μV
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	$\lvert V_{IO} \rvert \le 5$ mV			4.99		V
		I_{OH} = −20 μA		4.85	4.93		
		I_{OH} = −200 μA		4.25	4.65		
V_{OL}	Low-level output voltage	I_{OL} = −1 mA			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 50 μA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.9	1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, I_{OL} = 5 mA	R_L = 10 kΩ†	15	35		V/mV
			R_L = 1 MΩ†		175		
r_{id}	Differential input resistance	V_O = 1 V to 4 V			10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10		140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	70	75		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, No load	$V_{IC} = V_{DD}/2$,	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		4.4	6	mA

† Referenced to 2.5 V

TLC2272Y electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2272Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω		300	2500	µV
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO} \rvert \le 5$ mV	0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 µA			4.99		V
		I_{OH} = −200 µA		4.85	4.93		
		I_{OH} = −1 mA		4.25	4.65		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA		0.9	1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ†	15	35		V/mV
			R_L = 1 MΩ†		175		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10		140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V, R_S = 50 Ω	70	75		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V,	V_{IC} = V_{DD}/2, No load	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		2.2	3	mA

† Referenced to 2.5 V

TLC2272Y electrical characteristics at $V_{DD\pm} = \pm5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2272Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$, $V_O = 0$			300	2500	µV
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV		−5 to 4	−5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$			4.99		V
		$I_O = -200\ \mu A$		4.85	4.93		
		$I_O = -1$ mA		4.25	4.65		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_{OL} = 50\ \mu A$			−4.99		V
		$V_{IC} = 0$, $I_{OL} = 500\ \mu A$		−4.85	−4.91		
		$V_{IC} = 0$, $I_{OL} = 5$ mA		−3.5	−4.1		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V	$R_L = 10\ k\Omega$	25	50		V/mV
			$R_L = 1\ M\Omega$		300		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, $A_V = 10$			130		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$		75	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.2$ V to ±8 V, $V_{IC} = 0$, No load		80	95		dB
I_{DD}	Supply current	$V_O = 0$, No load			2.4	3	mA

TLC2274Y electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2274Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω		300	2500	μV
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	$\lvert V_{IO} \rvert \le 5$ mV			4.99		V
		I_{OH} = −20 μA		4.85	4.93		
		I_{OH} = −200 μA		4.25	4.65		
V_{OL}	Low-level output voltage	I_{OL} = −1 mA			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 50 μA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.9	1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, I_{OL} = 5 mA	R_L = 10 kΩ†	15	35		V/mV
			R_L = 1 MΩ†		175		
r_{id}	Differential input resistance	V_O = 1 V to 4 V			10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10		140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	70	75		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, No load	$V_{IC} = V_{DD}/2$,	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		4.4	6	mA

† Referenced to 2.5 V

TLC2274Y electrical characteristics at $V_{DD\pm} = \pm 5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2274Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	$V_O = 0$,		300	2500	µV
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$,	$\lvert V_{IO} \rvert \le 5$ mV	−5 to 4	−5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$			4.99		V
		$I_O = -200\ \mu A$		4.85	4.93		
		$I_O = -1$ mA		4.25	4.65		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$,	$I_{OL} = 50\ \mu A$		−4.99		V
		$V_{IC} = 0$,	$I_{OL} = 500\ \mu A$	−4.85	−4.91		
		$V_{IC} = 0$,	$I_{OL} = 5$ mA	−3.5	−4.1		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V	$R_L = 10\ k\Omega$	25	50		V/mV
			$R_L = 1\ M\Omega$		300		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	$A_V = 10$		130		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $R_S = 50\ \Omega$	$V_O = 0$,	75	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ± 8 V,	$V_{IC} = 0$	80	95		dB
I_{DD}	Supply current	$V_O = 0$,	No load		4.8	6	mA

TYPICAL CHARACTERISTICS

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NOTE: For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE

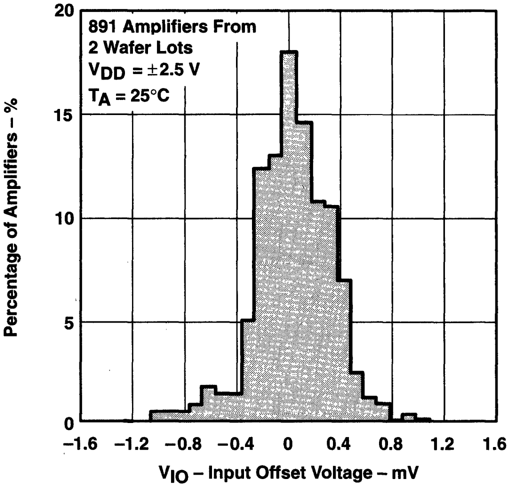

Figure 1

DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE

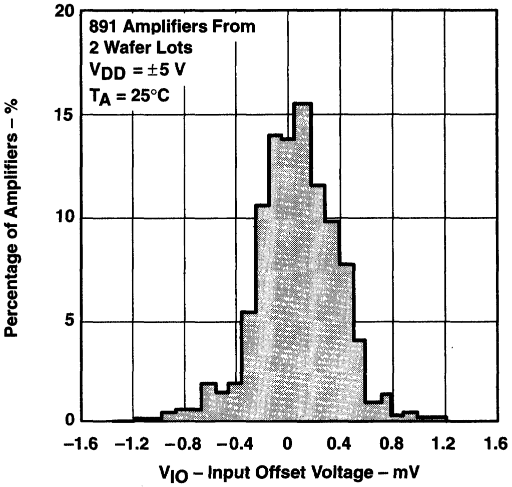

Figure 2

DISTRIBUTION OF TLC2274
INPUT OFFSET VOLTAGE

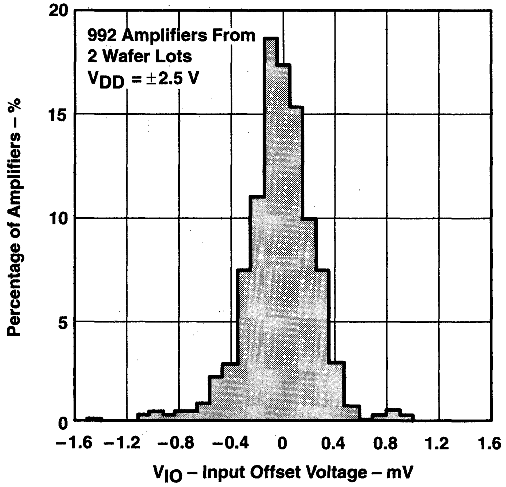

Figure 3

DISTRIBUTION OF TLC2274
INPUT OFFSET VOLTAGE

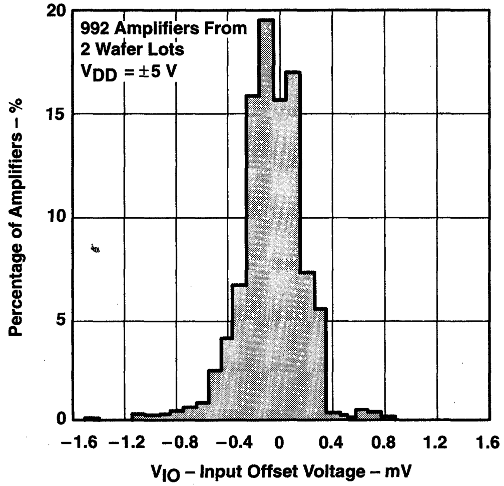

Figure 4

TYPICAL CHARACTERISTICS

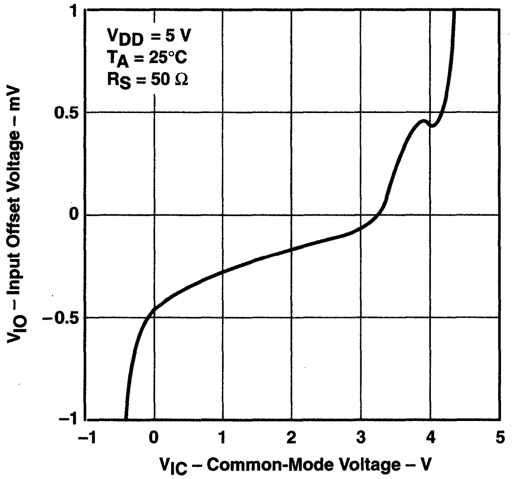
INPUT OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

Figure 5

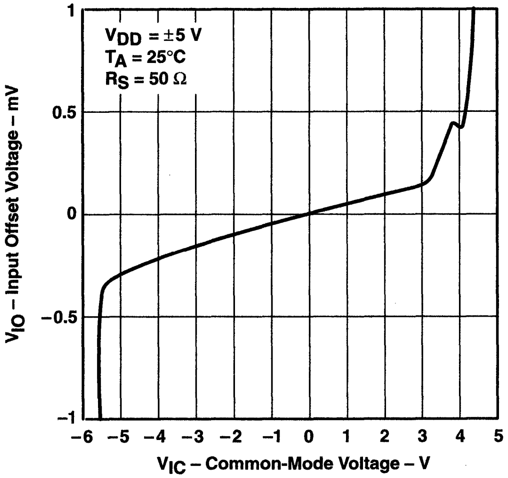
INPUT OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

Figure 6

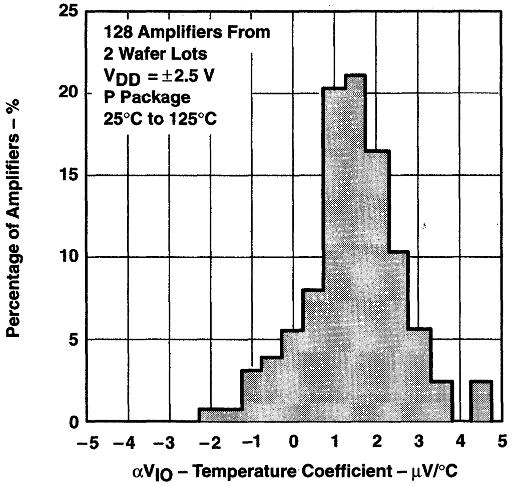
DISTRIBUTION OF TLC2272 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

Figure 7

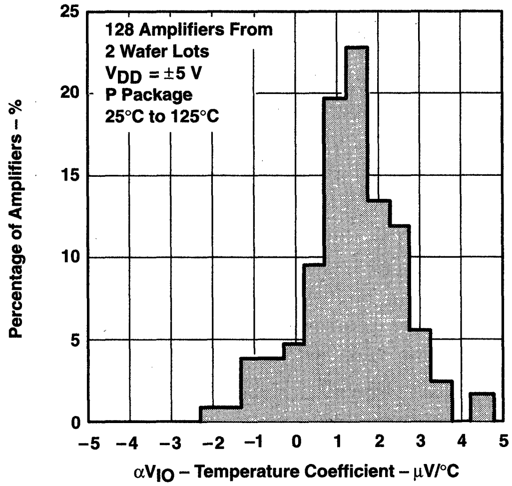
DISTRIBUTION OF TLC2272 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

Figure 8

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2274 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

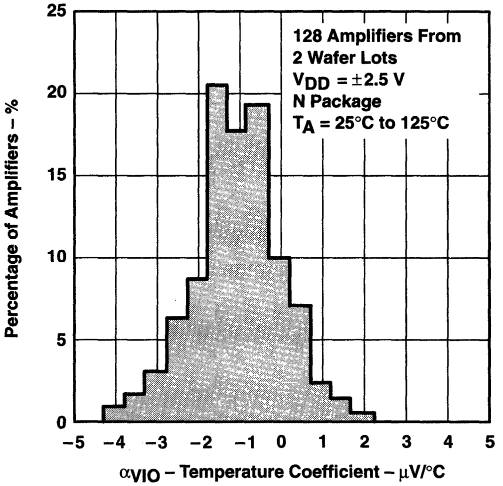

Figure 9

DISTRIBUTION OF TLC2274 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

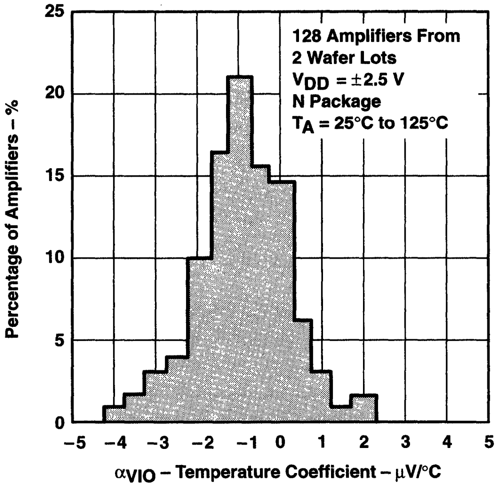

Figure 10

INPUT BIAS AND OFFSET CURRENT†
vs
FREE-AIR TEMPERATURE

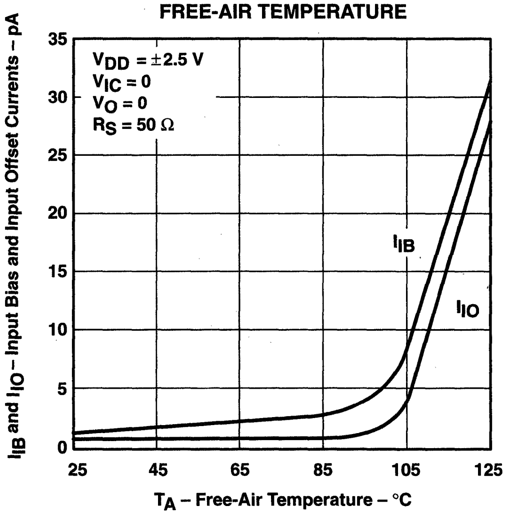

Figure 11

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

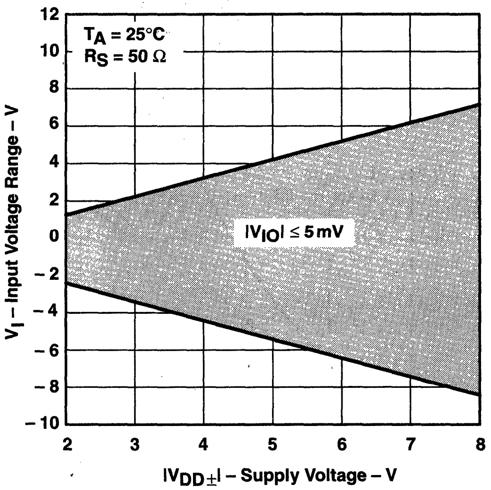

Figure 12

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE† vs FREE-AIR TEMPERATURE

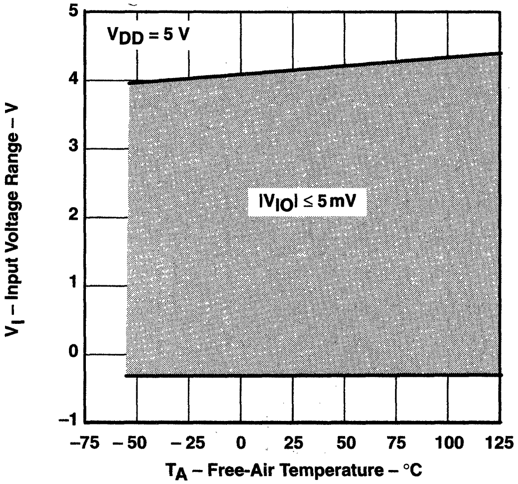

Figure 13

HIGH-LEVEL OUTPUT VOLTAGE† vs HIGH-LEVEL OUTPUT CURRENT

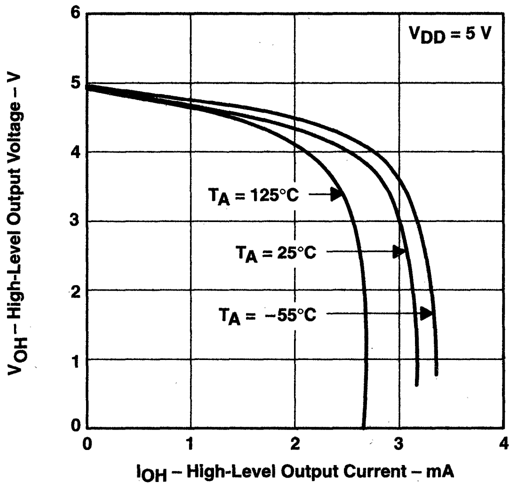

Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

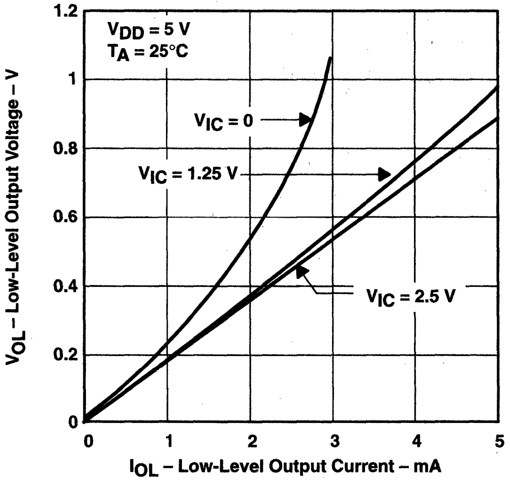

Figure 15

LOW-LEVEL OUTPUT VOLTAGE† vs LOW-LEVEL OUTPUT CURRENT

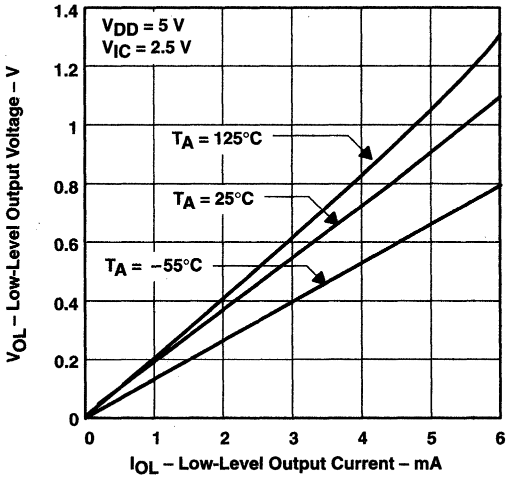

Figure 16

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE† vs OUTPUT CURRENT

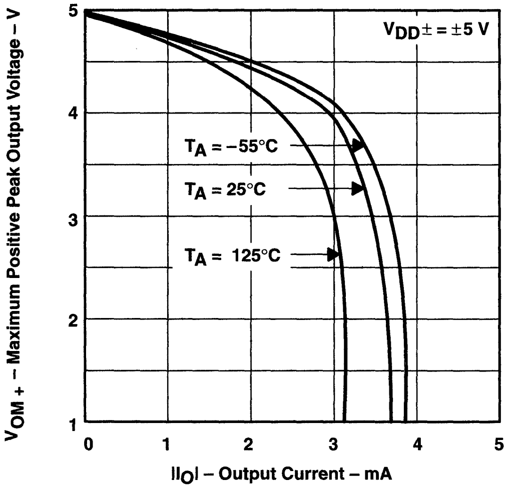

Figure 17

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE† vs OUTPUT CURRENT

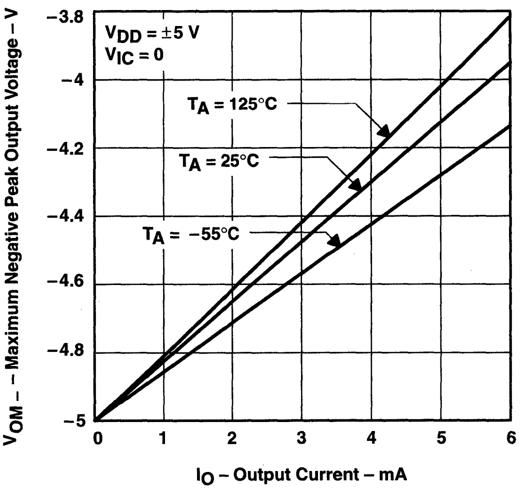

Figure 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

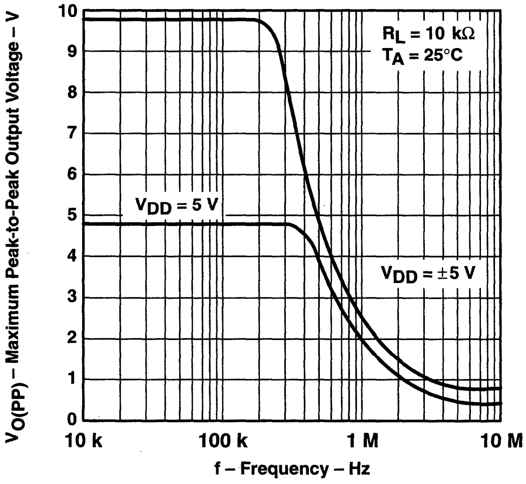

Figure 19

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

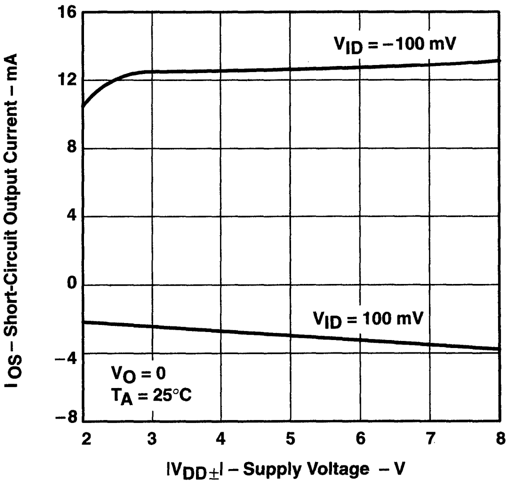

Figure 20

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

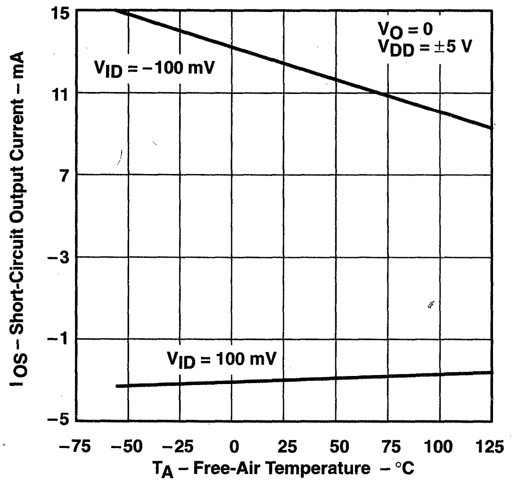

Figure 21

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

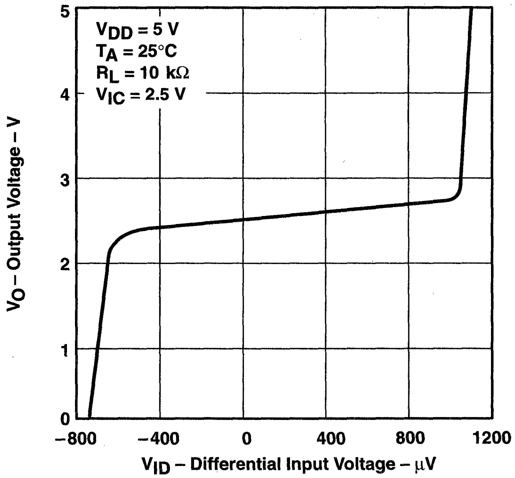

Figure 22

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

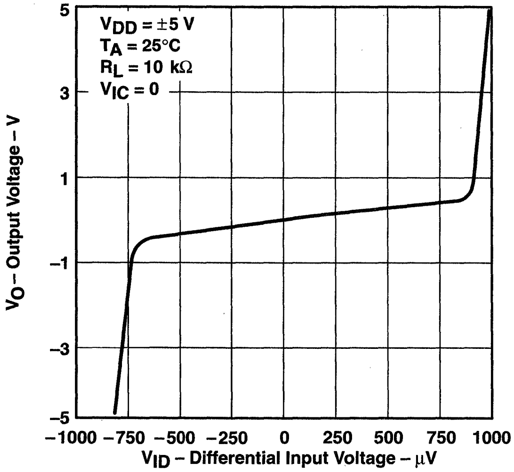

Figure 23

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

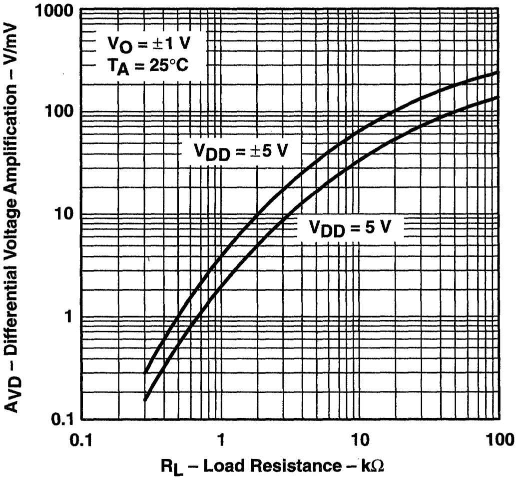

Figure 24

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

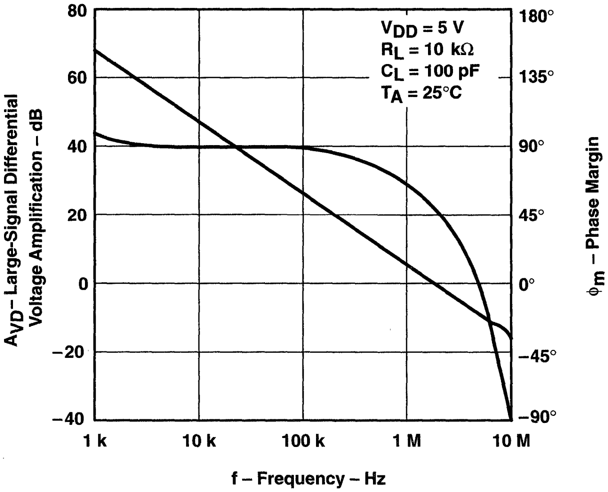

Figure 25

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

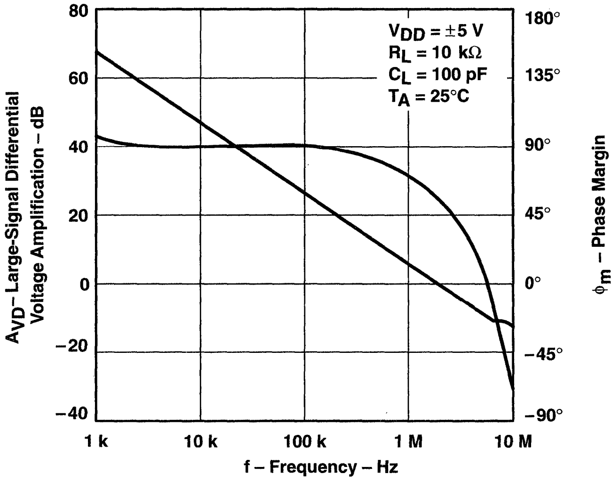

Figure 26

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

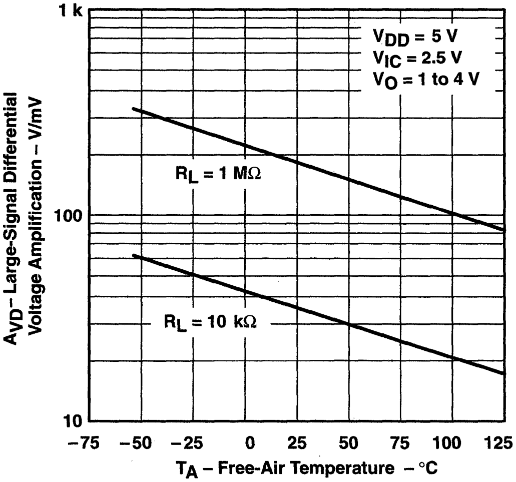

Figure 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

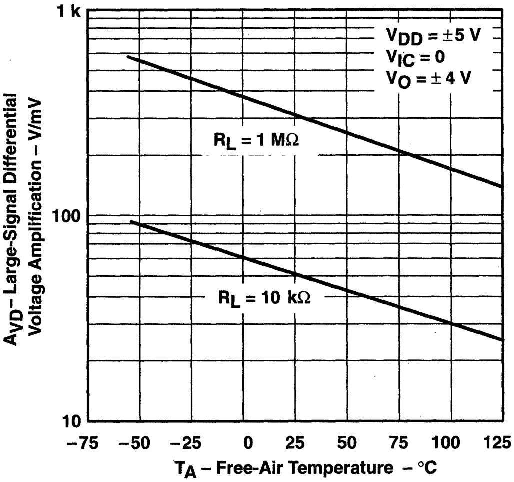

Figure 28

OUTPUT IMPEDANCE vs FREQUENCY

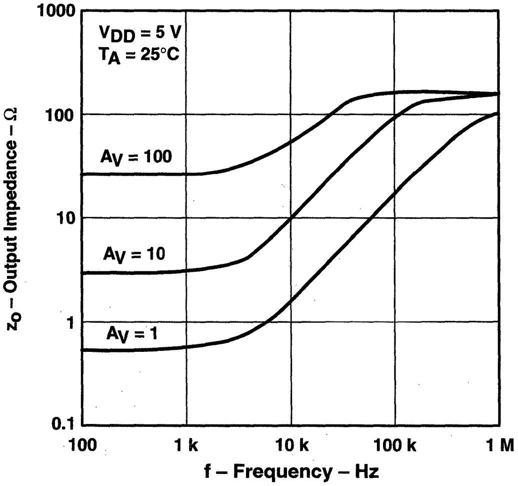

Figure 29

OUTPUT IMPEDANCE vs FREQUENCY

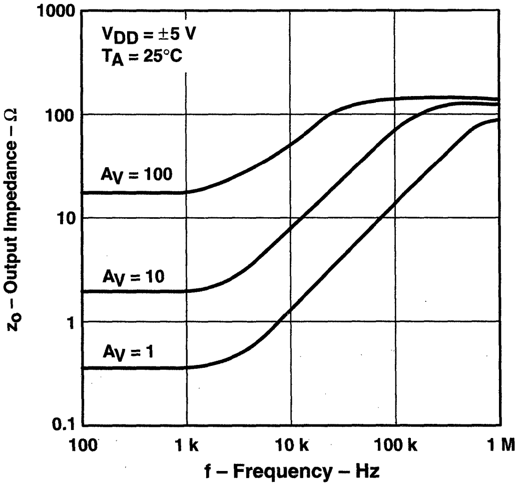

Figure 30

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

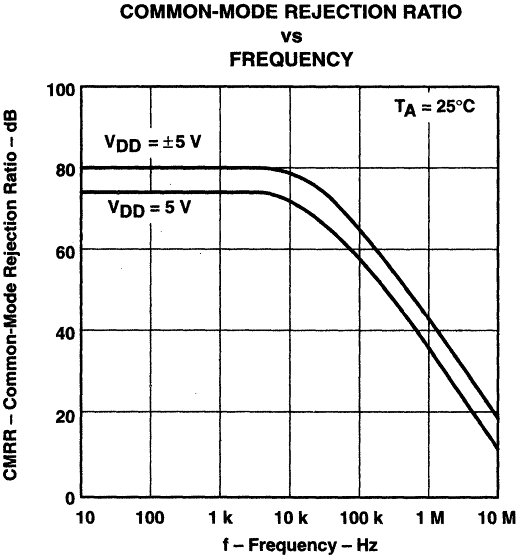


Figure 31

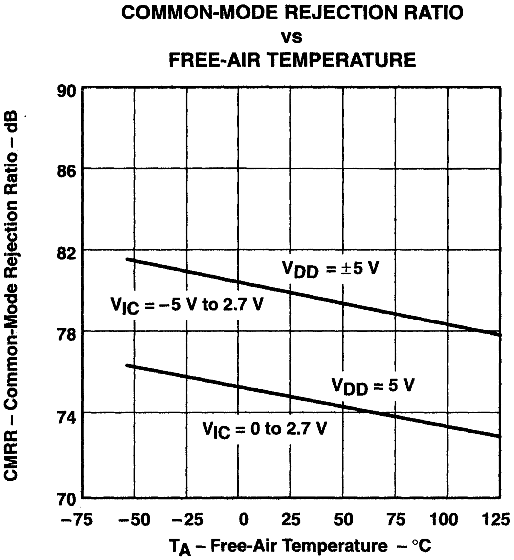


Figure 32

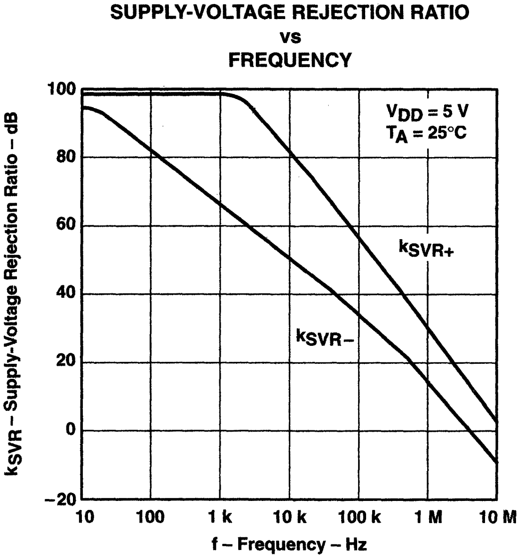


Figure 33

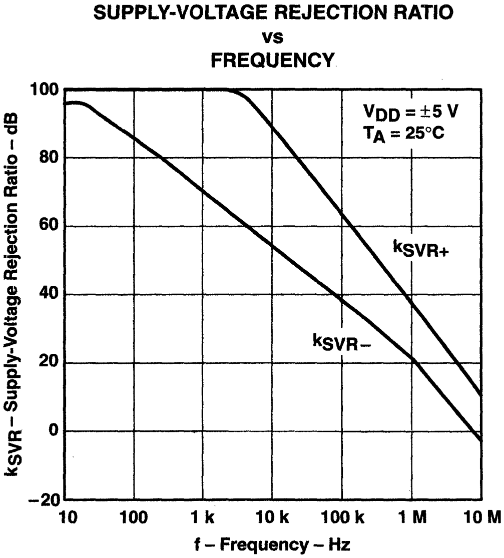
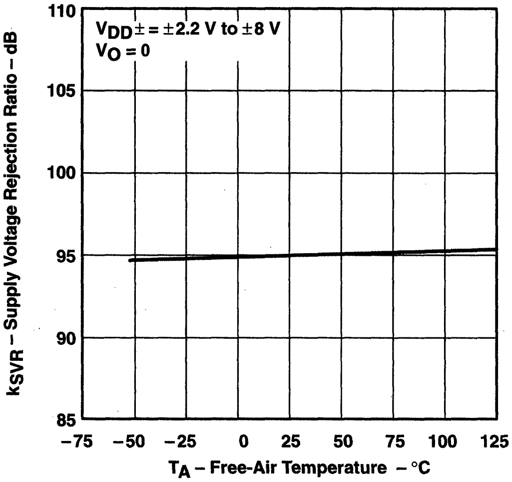


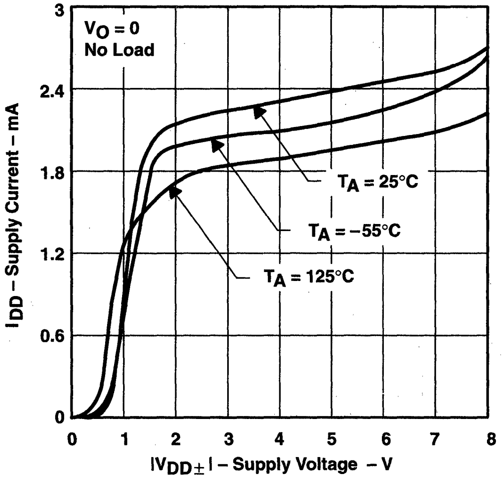
Figure 34

TYPICAL CHARACTERISTICS



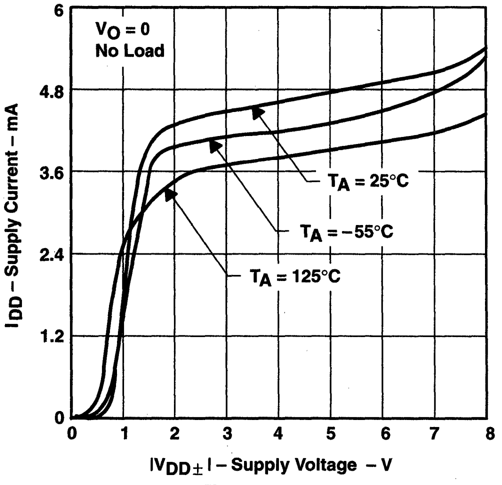
SUPPLY VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

Figure 35



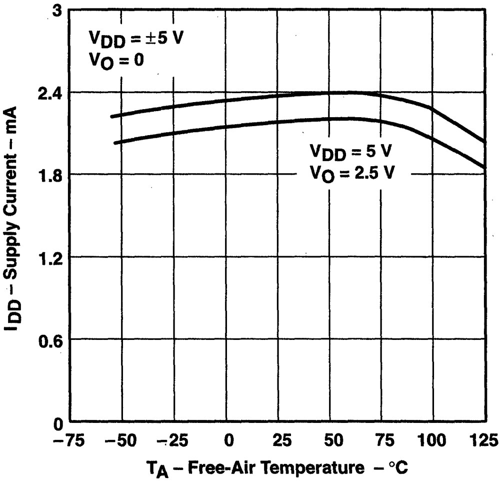
TLC2272
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

Figure 36



TLC2274
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

Figure 37



TLC2272
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

Figure 38

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TLC2274
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

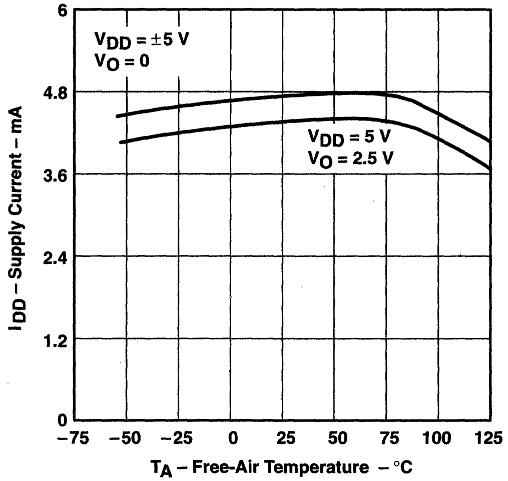

Figure 39

SLEW RATE
vs
LOAD CAPACITANCE

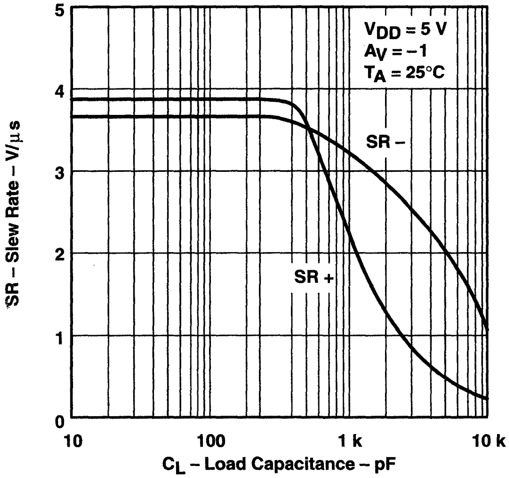

Figure 40

SLEW RATE†
vs
FREE-AIR TEMPERATURE

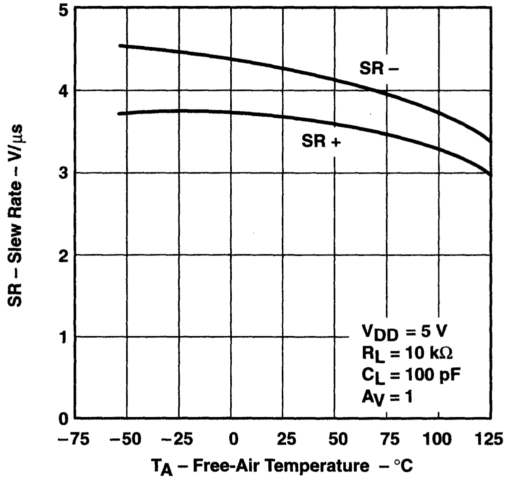

Figure 41

INVERTING LARGE-SIGNAL PULSE RESPONSE

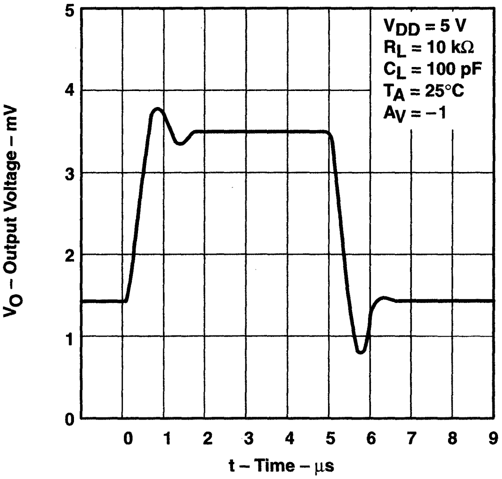

Figure 42

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

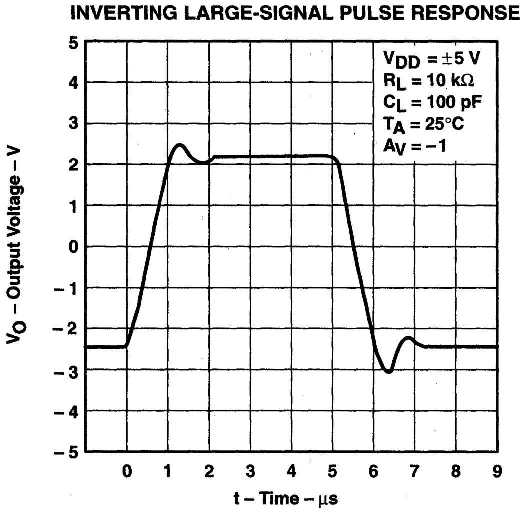
INVERTING LARGE-SIGNAL PULSE RESPONSE

Figure 43

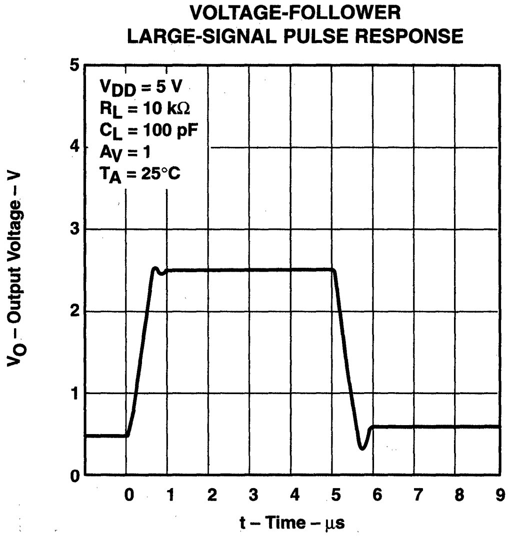
VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

Figure 44

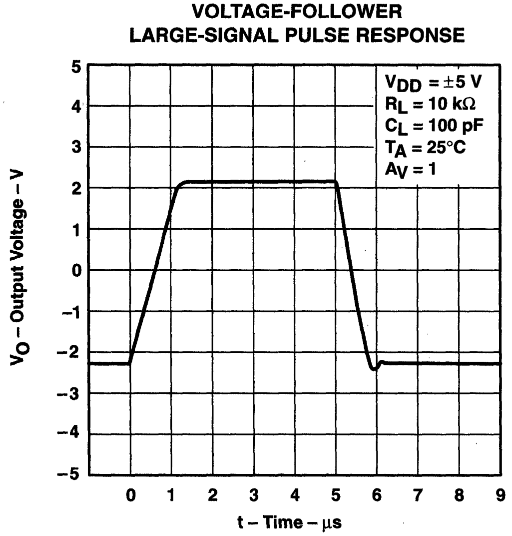
VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

Figure 45

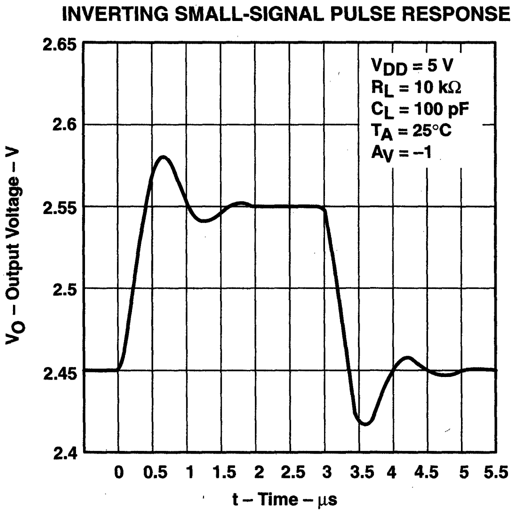
INVERTING SMALL-SIGNAL PULSE RESPONSE

Figure 46

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

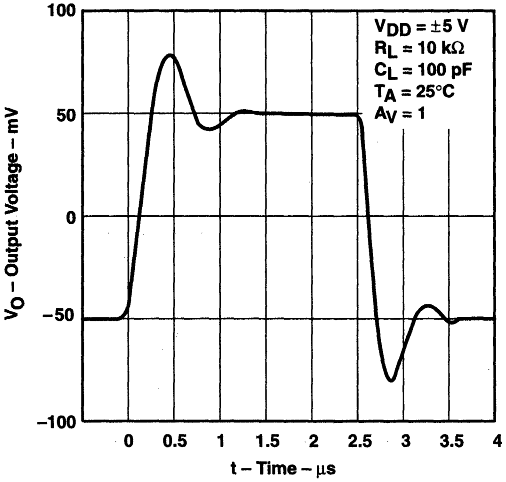

Figure 47

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

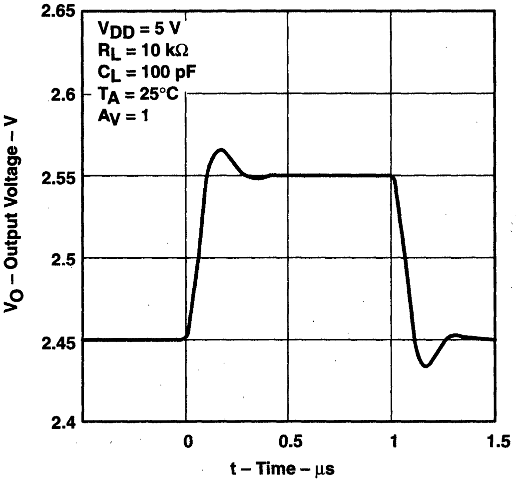

Figure 48

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

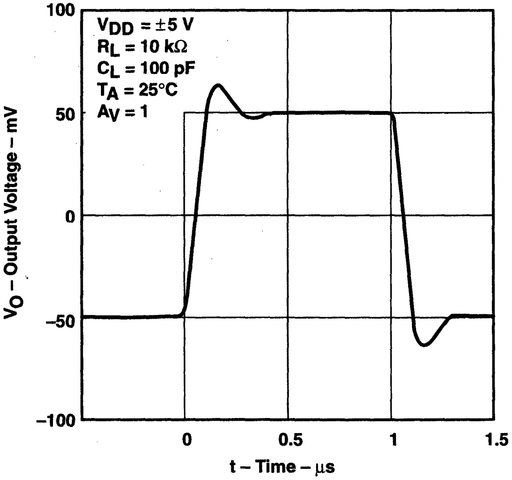

Figure 49

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

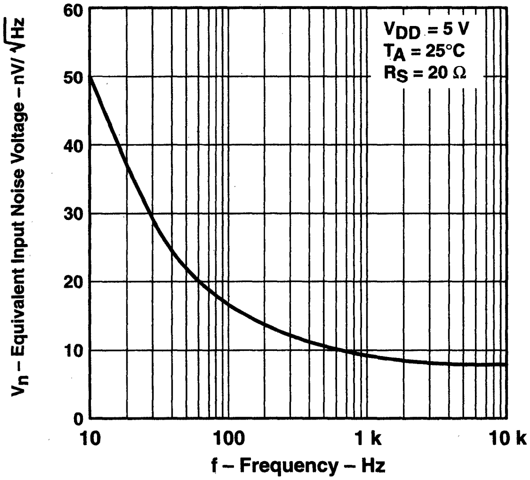

Figure 50

TYPICAL CHARACTERISTICS

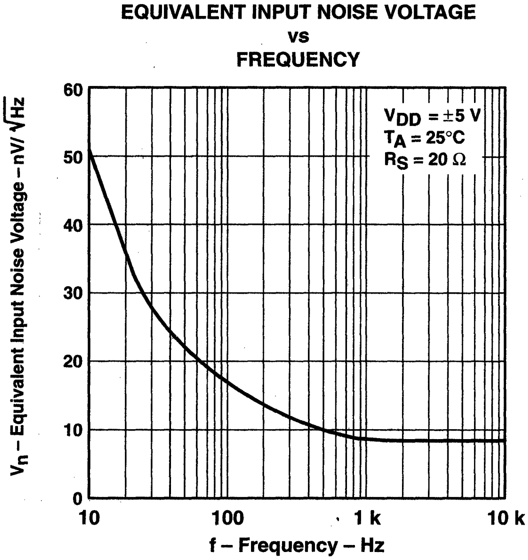

Figure 51

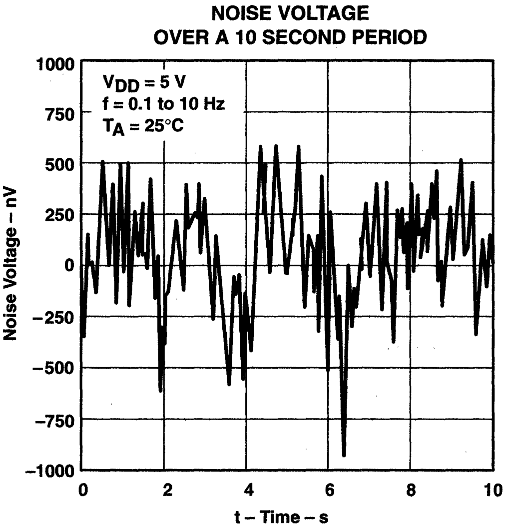

Figure 52

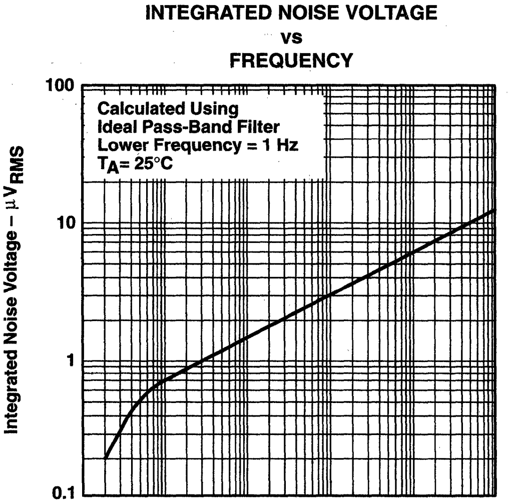

Figure 53

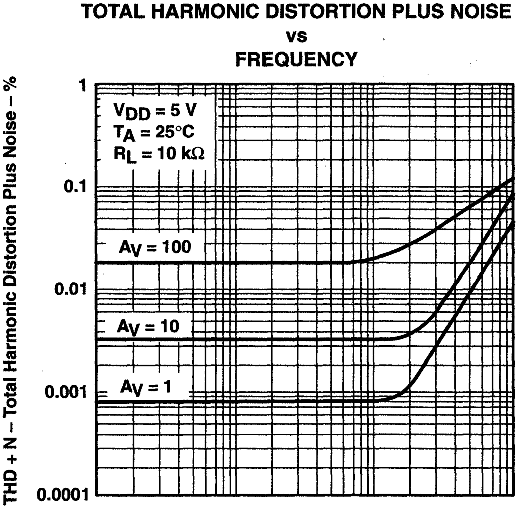

Figure 54

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

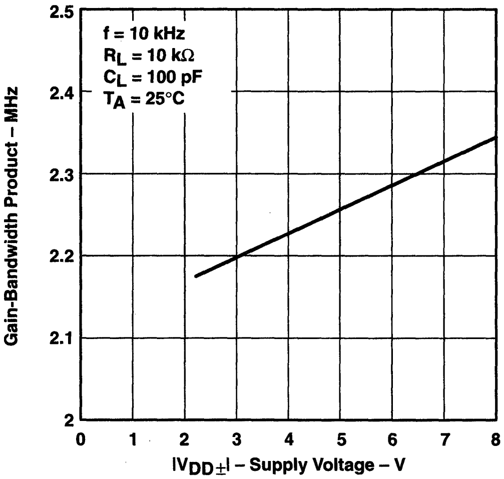

Figure 55

GAIN-BANDWIDTH PRODUCT†
vs
FREE-AIR TEMPERATURE

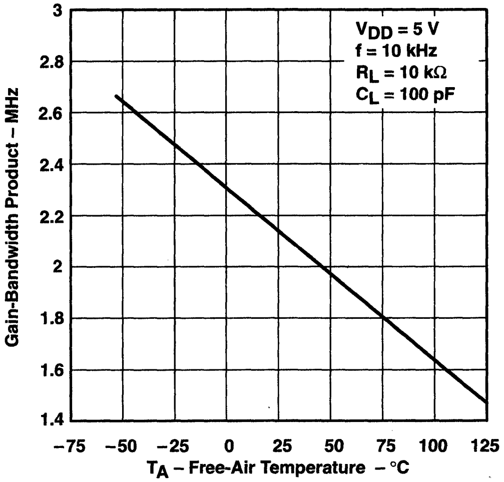

Figure 56

PHASE MARGIN
vs
LOAD CAPACITANCE

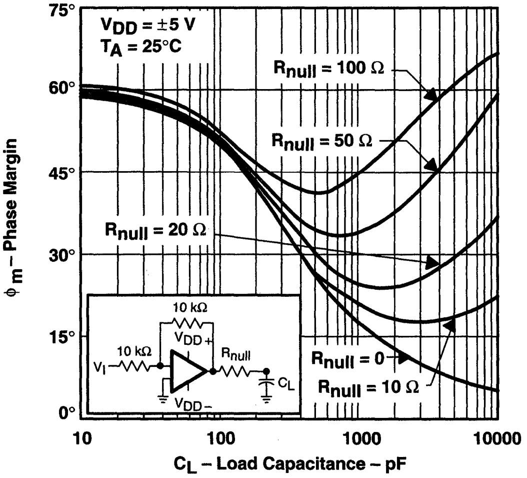

Figure 57

GAIN MARGIN
vs
LOAD CAPACITANCE

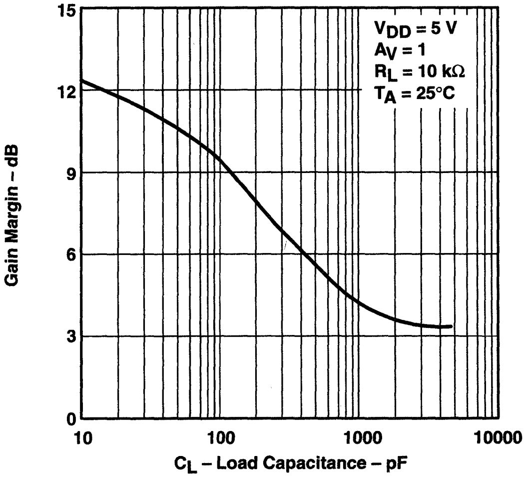

Figure 58

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

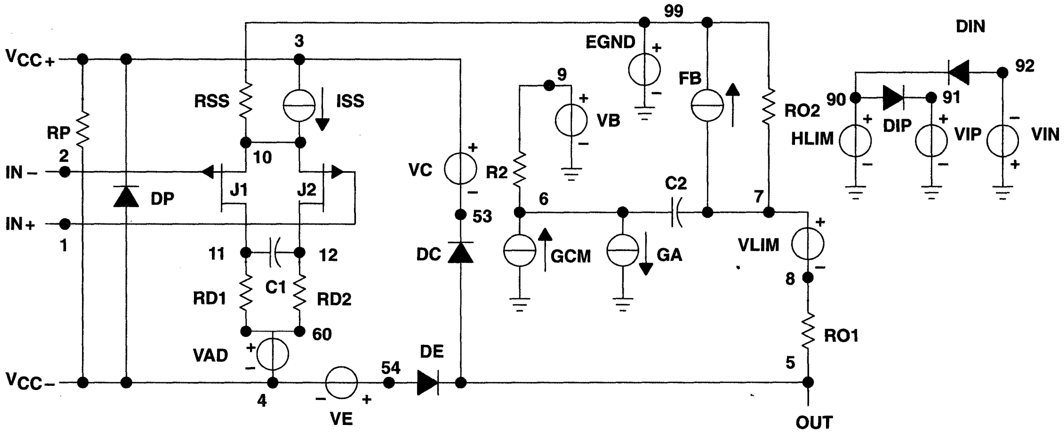
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 59 were generated using the TLC227x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Intergrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



```
.SUBCKT TLC227x 1 2 3 4 5
        C1      11      1214E–12
        C2      6       760.00E–12
        DC      5       53DX
        DE      54      5DX
        DLP     90      91DX
        DLN     92      90DX
        DP      4       3DX
        EGND    99      0POLY (2) (3,0) (4,) 0 .5 .5
        FB      99      0POLY (5) VB VC VE VLP VLN 0
        + 984.9E3 –1E6 1E6 1E6 –1E6
        GA      6       011 12 377.0E–6
        GCM 0 6 10 99 134E–9
        ISS     3       10DC 216.OE–6
        HLIM    90      0VLIM 1K
        J1      11      210 JX
        J2      12      110 JX
        R2      6       9100.OE3
RD1     60      112.653E3
RD2     60      122.653E3
R01     8       550
R02     7       9950
RP      3       44.310E3
RSS     10      99925.9E3
VAD     60      4–.5
VB      9       0DC 0
VC 3 53 DC .78
VE      54      4DC .78
VLIM    7       8DC 0
VLP     91      0DC 1.9
VLN     0       92DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=1.500E–12BETA=1.316E-3
+ VTO=–.270)
.ENDS
```

Figure 59. Boyle Macromodel and Subcircuit

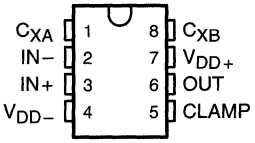
PSpice and *Parts* are trademarks of MicroSim Corporation.

TLC2652, TLC2652A, TLC2652Y
Advanced LinCMOS™ PRECISION CHOPPER-STABILIZED OPERATIONAL AMPLIFIERS

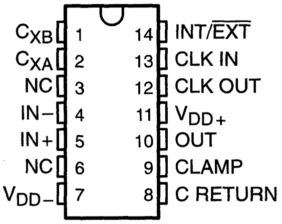
SLOS019B – SEPTEMBER 1988 – REVISED AUGUST 1994

- **Extremely Low Offset Voltage . . . 1 μV Max**
- **Extremely Low Change on Offset Voltage With Temperature . . . 0.003 μV/°C Typ**
- **Low Input Offset Current**
  500 pA Max at T_A = – 55°C to 125°C
- **A_{VD} . . . 135 dB Min**
- **CMRR and k_{SVR} . . . 120 dB Min**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **No Noise Degradation With External Capacitors Connected to V_{DD-}**

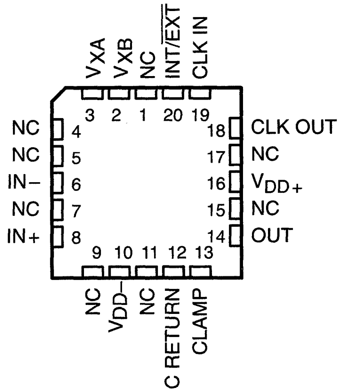
D008, JG, OR P PACKAGE
(TOP VIEW)



D014, JG, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC2652 and TLC2652A are high-precision chopper-stabilized operational amplifiers using Texas Instruments Advanced LinCMOS™ process. This process in conjunction with unique chopper-stabilization circuitry produces operational amplifiers whose performance matches or exceeds that of similar devices available today.

Chopper-stabilization techniques make possible extremely high dc precision by continuously nulling input offset voltage even during variation in temperature, time, common-mode voltage, and power supply voltage. In addition, low-frequency noise voltage is significantly reduced. This high precision, coupled with the extremely high input impedance of the CMOS input stage, makes the

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES							CHIP FORM (Y)
		8 PIN			14 PIN			20 PIN	
		SMALL OUTLINE (D008)	CERAMIC DIP (JG)	PLASTIC DIP (P)	SMALL OUTLINE (D014)	CERAMIC DIP (J)	PLASTIC DIP (N)	CHIP CARRIER (FK)	
0°C to 70°C	1 μV 3 μV	TLC2652AC-8D TLC2652C-8D	— —	TLC2652ACP TLC2652CP	TLC2652AC-14D TLC2652C-14D	— —	TLC2652ACN TLC2652CN	— —	TLC2652Y
−40°C to 85°C	1 μV 3 μV	TLC2652AI-8D TLC2652A-8D	— —	TLC2652AIP TLC2652IP	TLC2652AI-14D TLC2652I-14D	— —	TLC2652AIN TLC2652IN	— —	—
−55°C to 125°C	1 μV 3 μV	TLC2652AM-8D TLC2652M-8D	TLC2652AMJG TLC2652MJG	TLC2652AMP TLC2652MP	TLC2652AM-14D TLC2652M-14D	TLC2652AMJ TLC2652MJ	TLC2652AMN TLC2652MN	TLC2652AMFK TLC2652MFK	—

The D008 and D014 packages are available taped and reeled. Add R suffix to the device type (e.g., TLC2652AC-8DR). Chips are tested at 25°C.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

TLC2652 and TLC2652A an ideal choice for low-level signal processing applications such as strain gauges, thermocouples, and other transducer amplifiers. For applications that require extremely low noise and higher usable bandwidth, use the TLC2654 or TLC2654A device, which has a chopping frequency of 10 kHz.

The TLC2652 and TLC2652A input common-mode range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±1.9 V.

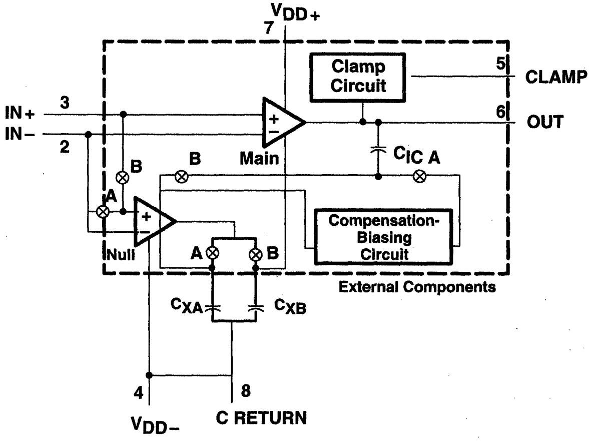
Two external capacitors are required for operation of the device; however, the on-chip chopper control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is made accessible to allow the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold level of the TLC2652 and TLC2652A require no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques are used on the TLC2652 and TLC2652A to allow exceptionally fast overload recovery time. If desired, an output clamp pin is available to reduce the recovery time even further.

The device inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up. Additionally the TLC2652 and TLC2652A incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

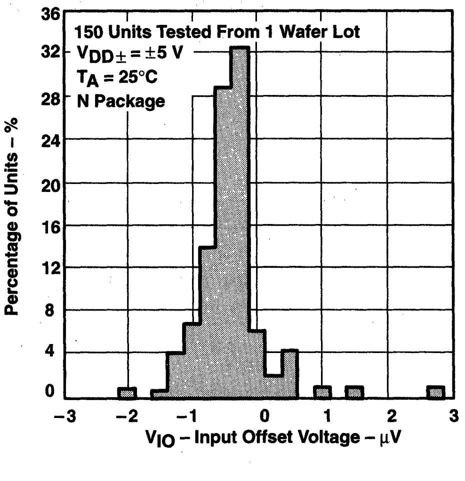
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to125°C.

functional block diagram



Pin numbers shown are for the D (14 pin), JG, and N packages.

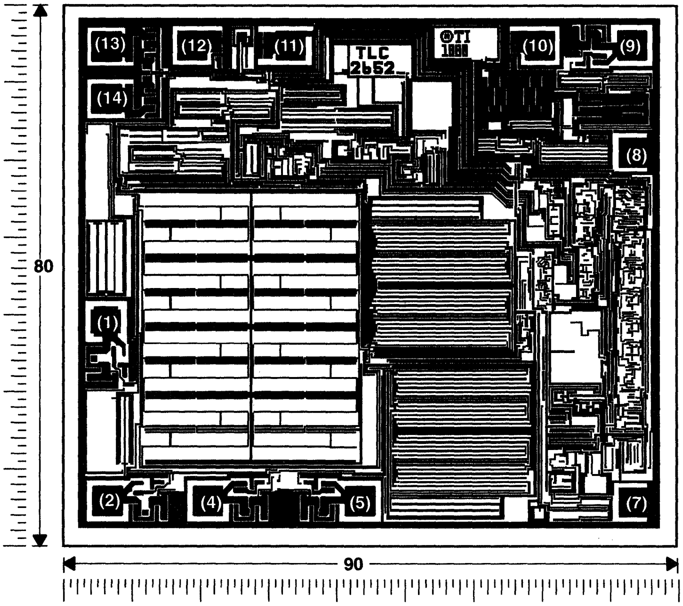
DISTRIBUTION OF TLC2652
INPUT OFFSET VOLTAGE



TLC2652Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2652C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (7) IS INTERNALLY CONNECTED
TO BACKSIDE OF CHIP.

FOR THE PINOUTS, SEE THE FUNCTIONAL BLOCK
DIAGRAM.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage V_{DD+} (see Note 1)	8 V
Supply voltage V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	±8 V
Voltage range on CLK IN and INT/$\overline{\text{EXT}}$	V_{DD} – to V_{DD-} + 5.2 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Current into CLK IN and INT/$\overline{\text{EXT}}$	±5 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	–40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or JG package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D008	725 mV	5.8 mW/°C	464 mW	377 mW	145 mW
D014	950 mV	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mV	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mV	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mV	8.4 mW/°C	672 mW	546 mW	210 mW
N	1575 mV	12.6 mW/°C	1008 mW	819 mW	315 mW
P	1000 mV	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±1.9	±8	±1.9	±8	±1.9	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.9$	V_{DD-}	$V_{DD+} - 1.9$	V_{DD-}	$V_{DD+} - 1.9$	V
Clock input voltage	V_{DD-}	$V_{DD-} + 5$	V_{DD-}	$V_{DD-} + 5$	V_{DD-}	$V_{DD-} + 5$	V
Operating free-air temperature, T_A	0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, $V_{DD}\pm = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2652C			TLC2652AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3		0.5	1	μV
			Full range			4.35			2.35	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.003	0.03		0.003	0.03	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.06		0.003	0.02	μV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	120	150		135	150		dB
			Full range	120			130			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current		25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

† Full range is 0° to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated at $T_A = 25$° using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2652C			TLC2652AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		2	2.8		V/µs
			Full range	1.5			1.5			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/µs
			Full range	1.8			1.8			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94			94	140	nV/√Hz
		f = 1 kHz	25°C		23			23	35	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		µV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 10 kHz	25°C		0.004			0.004		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕm	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

† Full range is 0° to 70°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD}\pm = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2652I			TLC2652AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3		0.5	1	µV
			Full range			4.95			2.95	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.003	0.03		0.003	0.03	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.06		0.003	0.02	µV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 10\ k\Omega$	25°C	120	150		135	150		dB
			Full range	120			125			
	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}\text{min}$, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm1.9$ V to ±8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

† Full range is −40° to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated at $T_A = 25$° using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2652I			TLC2652AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		2	2.8		V/µs
			Full range	1.4			1.4			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/µs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94			94	140	nV/√Hz
		f = 1 kHz	25°C		23			23	35	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		µV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

† Full range is –40° to 85°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD}\pm = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2652M			TLC2652AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 7)	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3.5		0.5	3	µV
			Full range			10			8	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.003	0.03*		0.003	0.03*	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.06*		0.003	0.02*	µV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	120	150		135	150		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			500			500	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}\text{min}$, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

* On products complaint to MIL-STD-883, Class B, this parameter is not production tested.

† Full range is −55° to 125°C

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated at $T_A = 25$° using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

7. This parameter is not production tested. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.

operating characteristics specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2652M TLC2652AM MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		V/µs
			Full range	1.3			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		V/µs
			Full range	1.6			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		94		nV/√Hz
		f = 1 kHz	25°C		23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8		µV
		f = 0 to 10 Hz	25°C		2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°		

† Full range is −55° to 125°C.

electrical characteristics at $V_{DD\pm} = \pm5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2652Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$,	$R_S = 50\ \Omega$		0.6	3	µV
	Input offset voltage long-term drift (see Note 4)				0.003	0.006	µV/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ,	See Note 5	4.7	4.8		V
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ,	See Note 5	−4.7	−4.9		V
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V,	$R_L = 10$ kΩ	120	150		dB
f_{ch}	Internal chopping frequency				450		Hz
	Clamp on-state current	$R_L = 100$ kΩ		25			µA
	Clamp off-state current	$V_O = -4$ V to 4 V				100	pA
CMRR	Common-mode rejection ratio	$V_O = 0$, $R_S = 50\ \Omega$	$V_{IC} = V_{ICR}$min,	120	140		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm1.9$ V to ±8 V, $R_S = 50\ \Omega$	$V_O = 0$,	120	135		dB
I_{DD}	Supply current	$V_O = 0$,	No load		1.5	2.4	mA

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated at $T_A = 25°$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5. Output clamp is not connected.

operating characteristics at $V_{DD\pm} = \pm5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TLC2652Y			UNIT
				MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	$V_O = \pm2.3$ V, $C_L = 100$ pF	$R_L = 10$ kΩ,	2	2.8		V/µs
SR−	Negative slew rate at unity gain			2.3	3.1		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			94		nV/√Hz
		f = 1 kHz			23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz			0.8		µV
		f = 0 to 10 Hz			2.8		
I_n	Equivalent input noise current	f = 1 kHz					pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $C_L = 100$ pF	$R_L = 10$ kΩ,		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ,	$C_L = 100$ pF		48°		

TYPICAL CHARACTERISTICS

Table of Graphs

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V_{IO}	Normalized input offset voltage	vs Chopping frequency	1
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ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	30 31 32
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TYPICAL CHARACTERISTICS†

NORMALIZED INPUT OFFSET VOLTAGE
vs
CHOPPING FREQUENCY

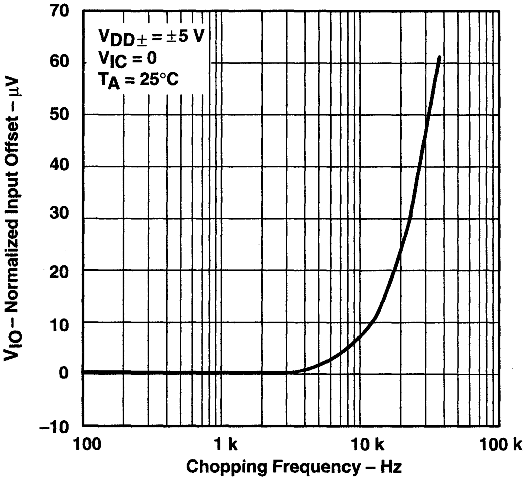

Figure 1

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

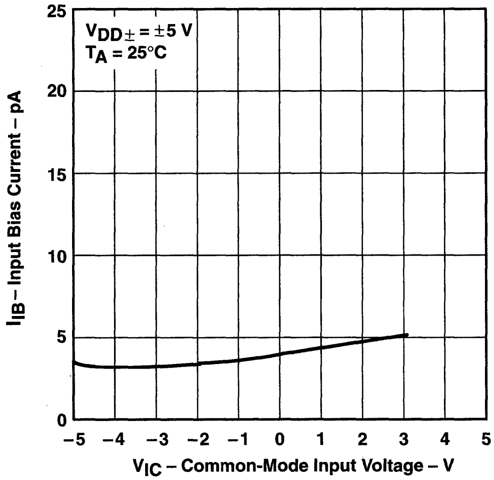

Figure 2

INPUT BIAS CURRENT
vs
CHOPPING FREQUENCY

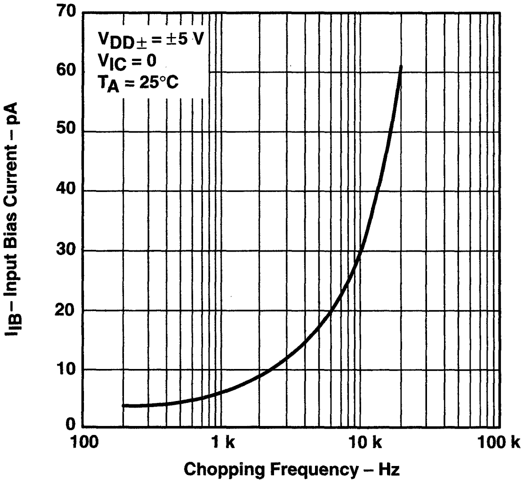

Figure 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

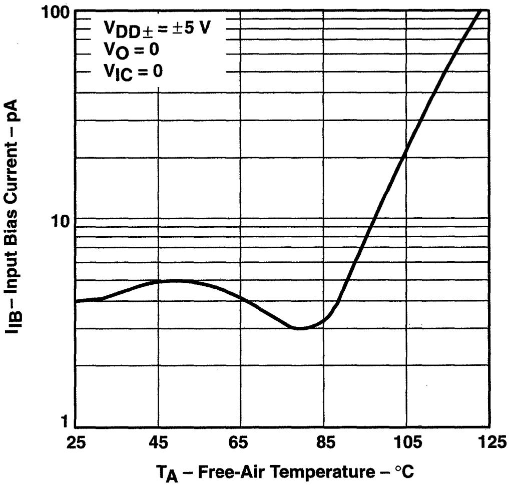

Figure 4

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

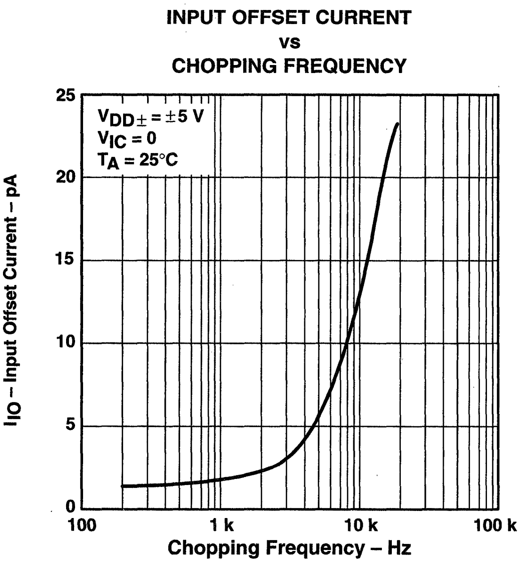

Figure 5

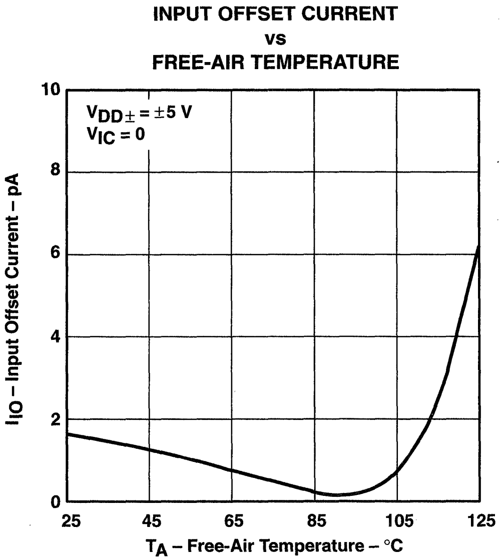

Figure 6

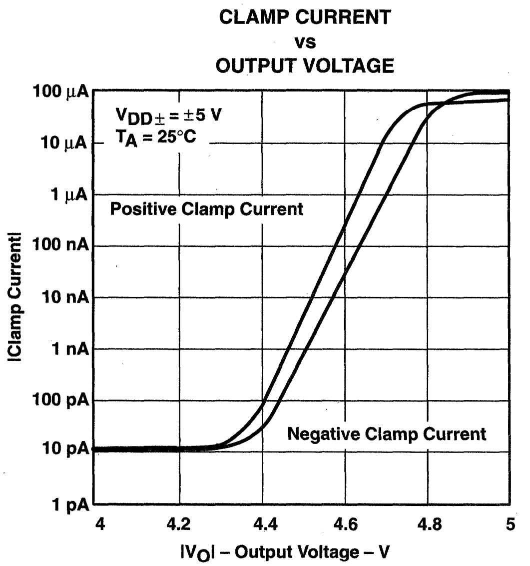

Figure 7

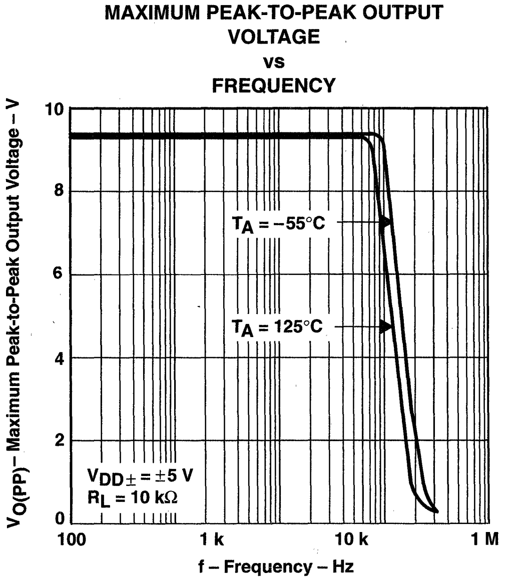

Figure 8

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

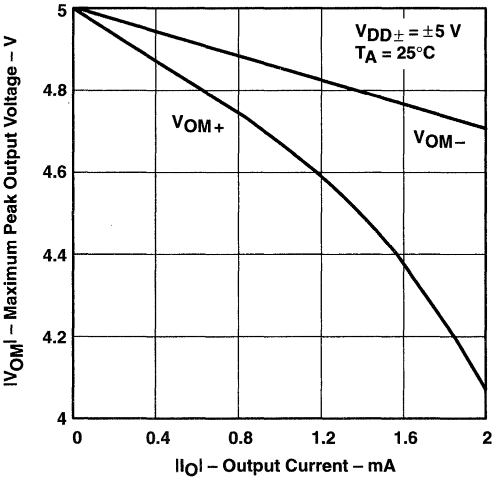

Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

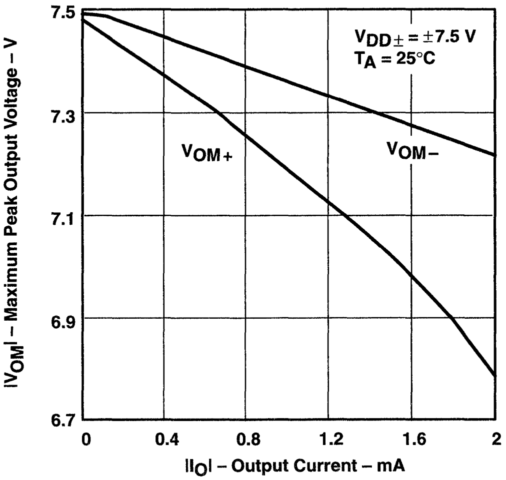

Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

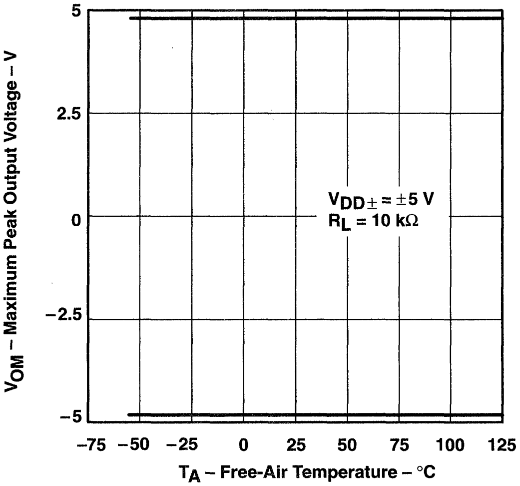

Figure 11

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

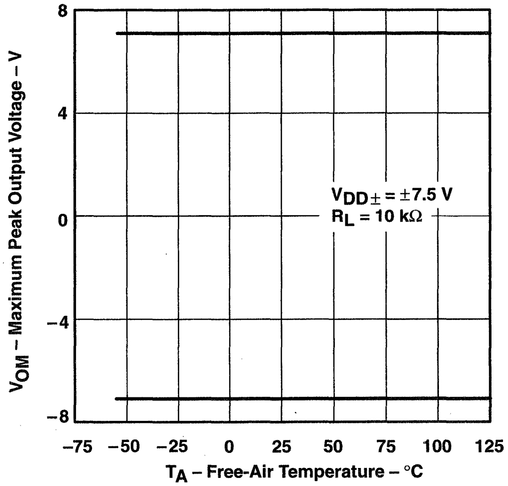

Figure 12

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

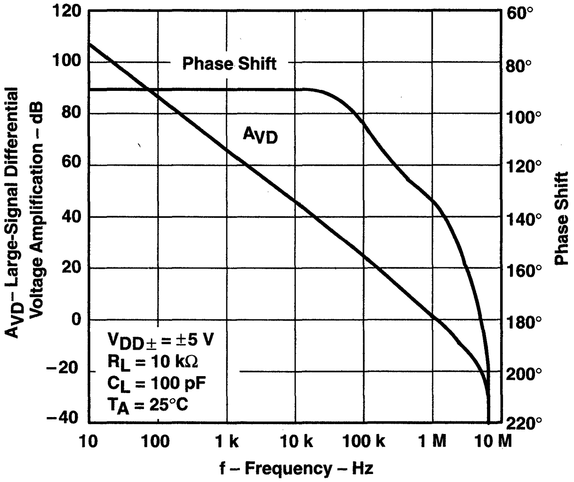

Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY FREE-AIR TEMPERATURE

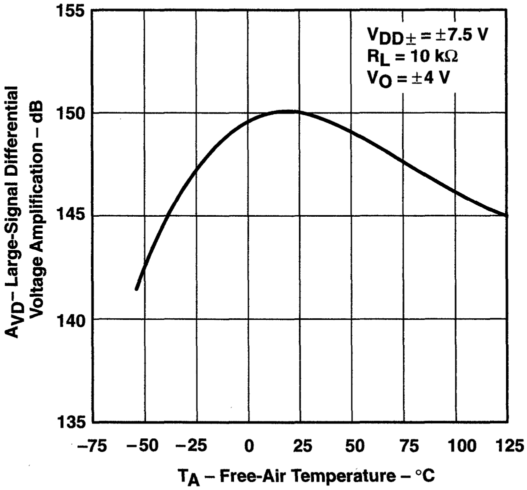

Figure 14

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

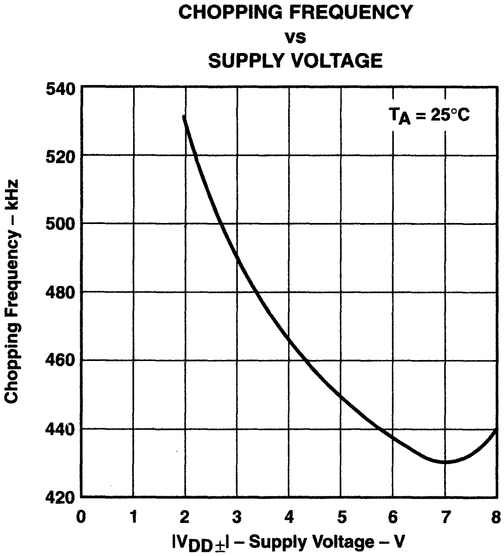

Figure 15

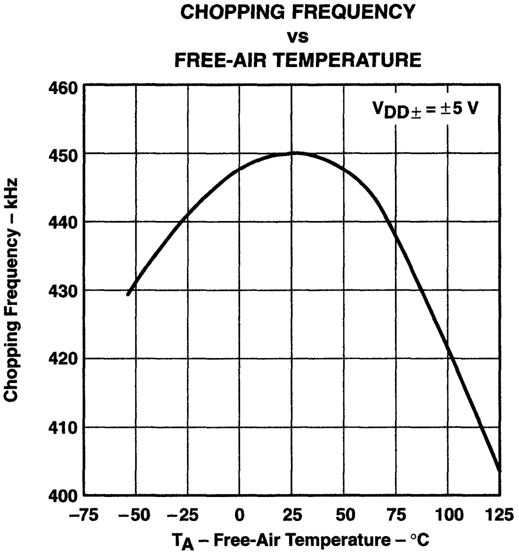

Figure 16

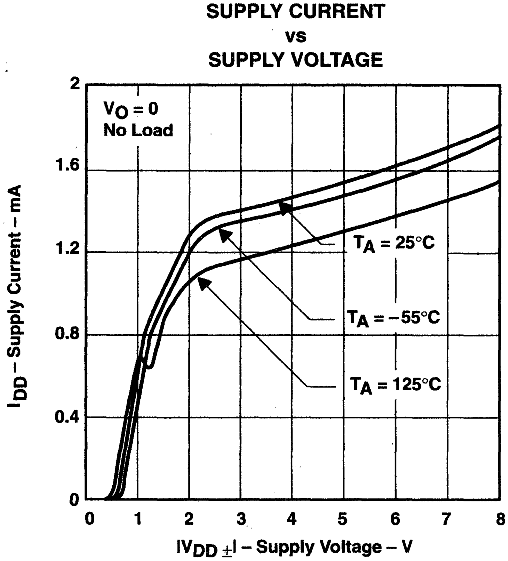

Figure 17

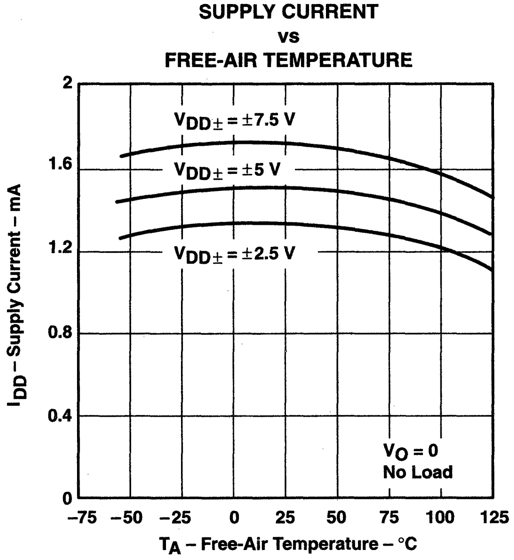

Figure 18

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

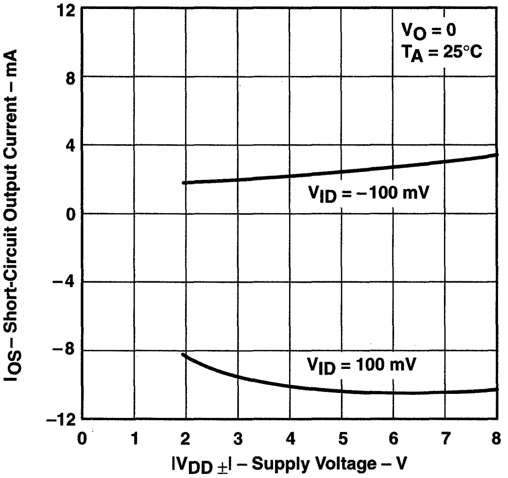

Figure 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

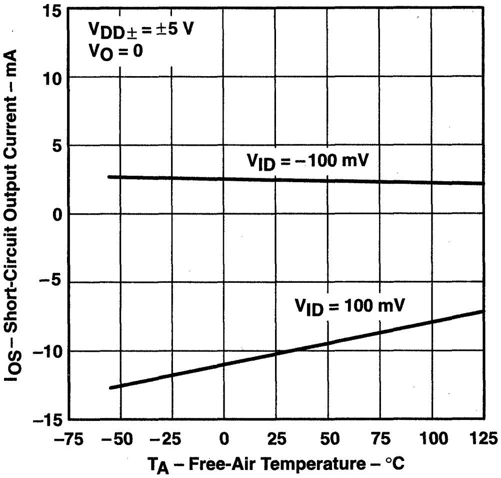

Figure 20

SLEW RATE
vs
SUPPLY VOLTAGE

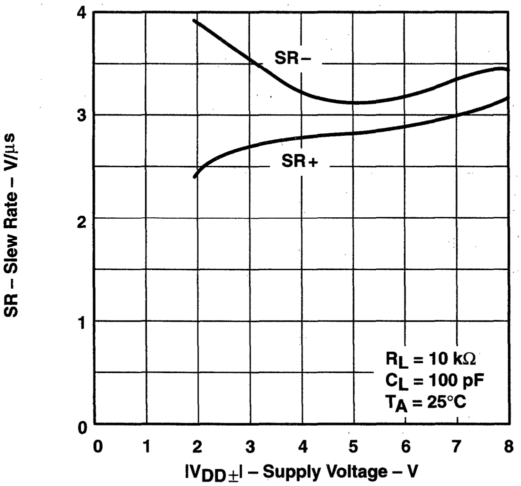

Figure 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

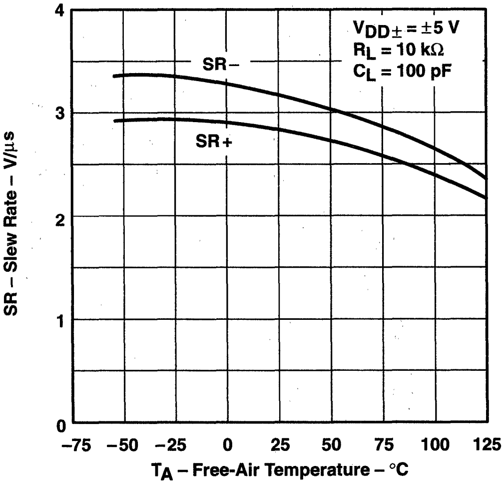

Figure 22

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

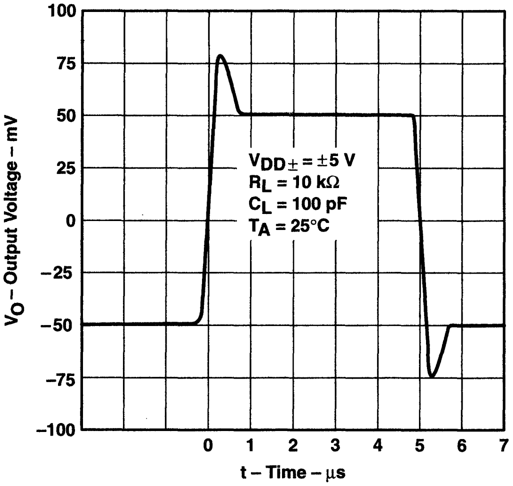

Figure 23

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

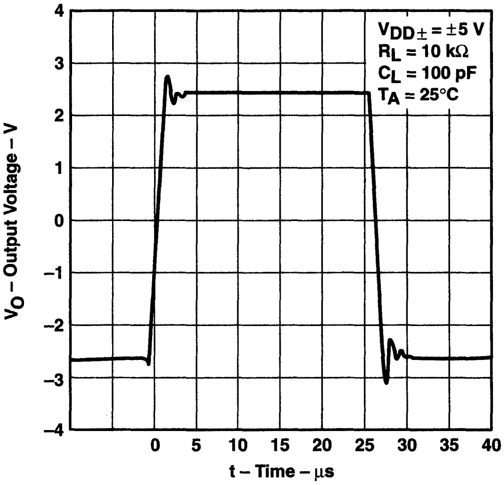

Figure 24

PEAK-TO-PEAK INPUT NOISE VOLTAGE vs CHOPPING FREQUENCY

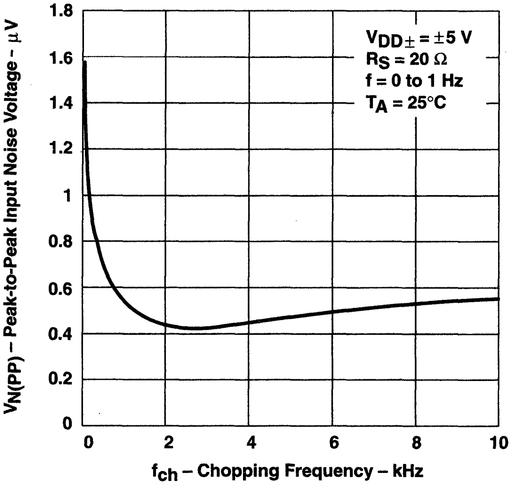

Figure 25

PEAK-TO-PEAK INPUT NOISE VOLTAGE vs CHOPPING FREQUENCY

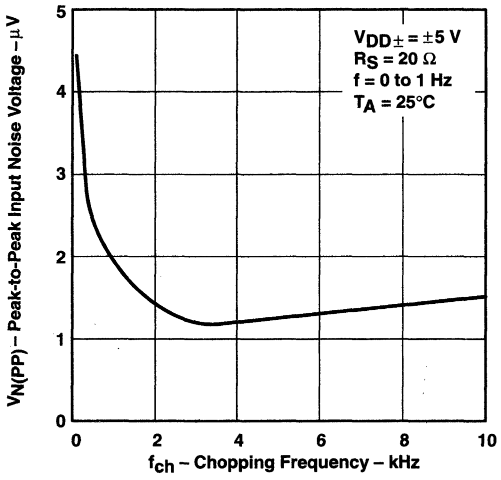

Figure 26

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

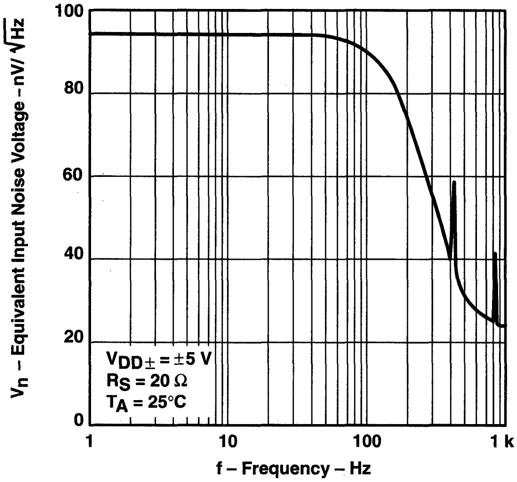

Figure 27

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

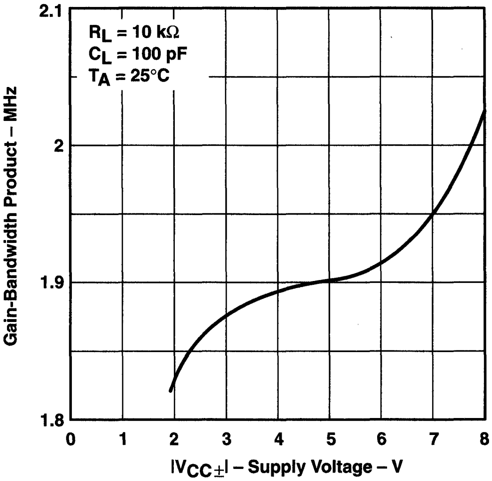

Figure 28

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

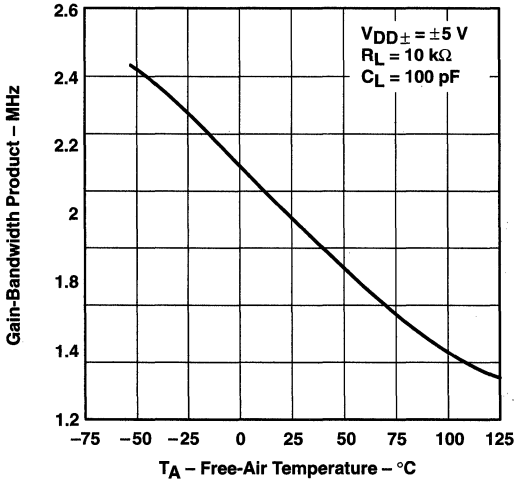

Figure 29

PHASE MARGIN vs SUPPLY VOLTAGE

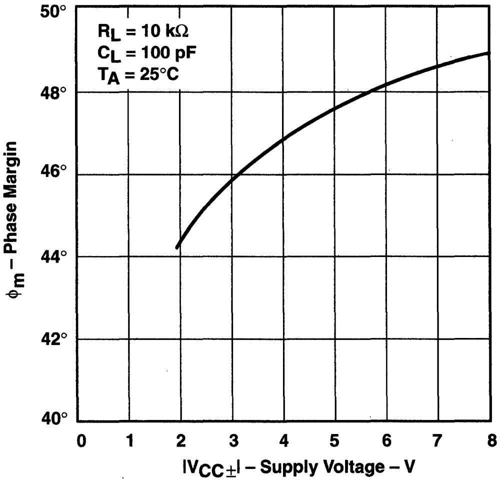

Figure 30

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

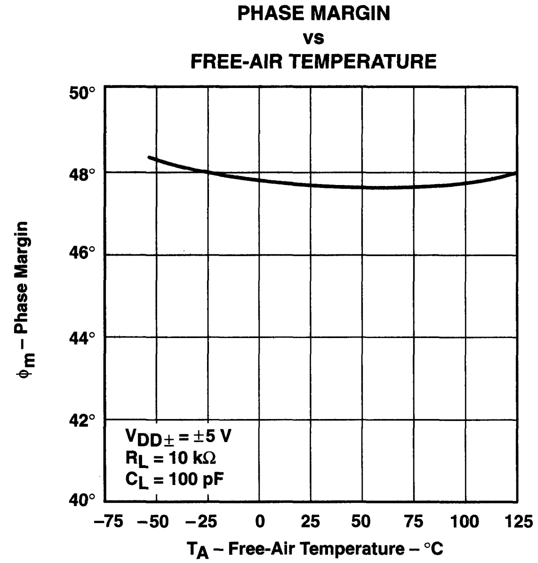

Figure 31

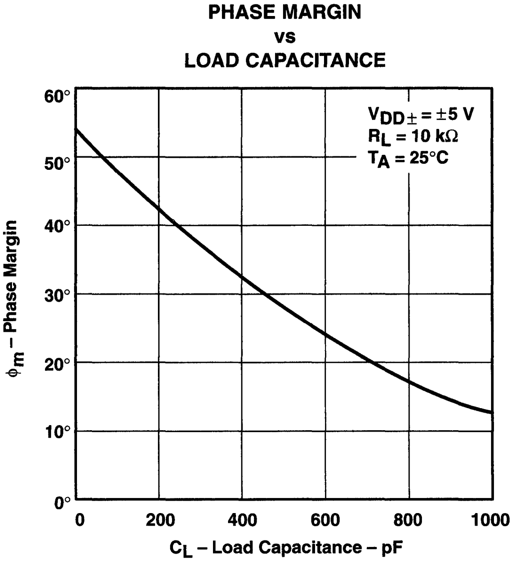

Figure 32

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

capacitor selection and placement

The two important factors to consider when selecting external capacitors C_{XA} and C_{XB} are leakage and dielectric absorption. Both factors can cause system degradation, negating the performance advantages realized by using the TLC2652.

Degradation from capacitor leakage becomes more apparent with the increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guard bands are recommended around the capacitor connections on both sides of the printed circuit board to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications where fast settling of input offset voltage is needed, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor can suffice.

Unlike many choppers available today, the TLC2652 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either V_{DD-} or C RETURN. On many choppers, connecting these capacitors to V_{DD-} causes degradation in noise performance. This problem is eliminated on the TLC2652.

internal/external clock

The TLC2652 has an internal clock that sets the chopping frequency to a nominal value of 450 Hz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package, the device chopping frequency can be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN pins. To use the internal 450-Hz clock, no connection is necessary. If external clocking is desired, connect INT/$\overline{\text{EXT}}$ to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, CLK IN can be driven from the negative rail to 5 V above the negative rail. If this level is exceeded, damage could occur to the device unless the current into CLK IN is limited to ±5 mA. When operating in the single-supply configuration, this feature allows the TLC2652 to be driven directly by 5-V TTL and CMOS logic. A divide-by-two frequency divider interfaces with CLK IN and sets the clock chopping frequency. The duty cycle of the external is not critical but should be kept between 30% and 60%.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2652, the nulling loop attempts to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time for the TLC2652 is significantly faster than competitive products; however, if required, this time can be reduced further by use of internal clamp circuitry accessible through CLAMP if required.

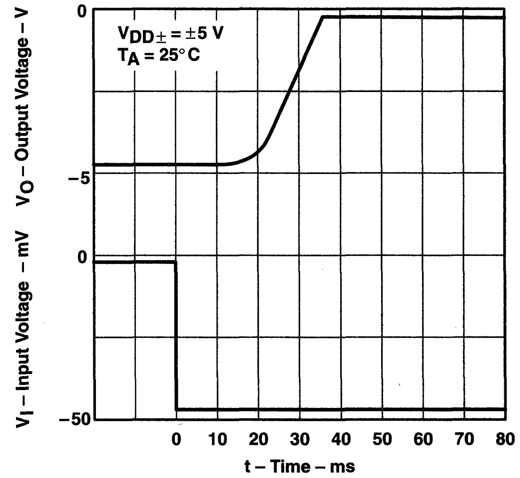


Figure 33. Overload Recovery

APPLICATION INFORMATION

overload recovery/output clamp (continued)

The clamp is a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced, and the TLC2652 output is prevented from going into saturation. Since the output must source sink current through the switch (see Figure 7), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage drift of the TLC2652, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). Dissimilar metal junctions can produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01-μV/°C typical of the TLC2652).

To help minimize thermoelectric effects, careful attention should be paid to component selection and circuit-board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latch-up avoidance

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2652 inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques to reduce the chance of latch-up should be used whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latch-up occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2652 incorporates internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers, a main amplifier and a nulling amplifier, plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2652 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2652 on-chip control logic produces two dominant clock phases: a nulling phase and an amplifying phase. The term chopper-stabilized derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2652. Switches A and B are make-before-break types.

APPLICATION INFORMATION

theory of operation (continued)

During the nulling phase, switch A is closed shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

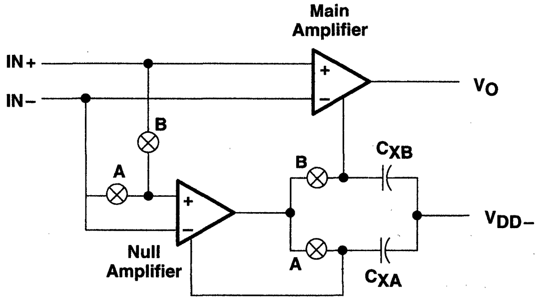


Figure 34. TLC2652 Simplified Block Diagram

During the amplifying phase, switch B is closed connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature over the common-mode input voltage range and power supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process, with its low-noise analog MOS transistors and patent-pending input stage design, significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches. As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2652 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

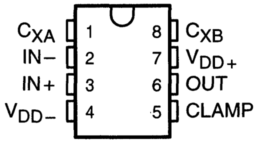
The TLC2652 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

TLC2654, TLC2654A, TLC2654Y
Advanced LinCMOS™ LOW-NOISE CHOPPER-STABILIZED OPERATIONAL AMPLIFIERS

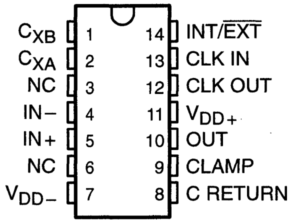
SLOS020D – NOVEMBER 1988 – REVISED AUGUTST 1994

- **Input Noise Voltage**
  0.5 μV (Peak-to-Peak) Typ, f = 0 to 1 Hz
  1.5 μV (Peak-to-Peak) Typ, f = 0 to 10 Hz
  47 nV/√Hz Typ, f = 10 Hz
  13 nV/√Hz Typ, f = 1 kHz
- **High Chopping Frequency . . . 10 kHz Typ**
- **No Clock Noise Below 10 kHz**
- **No Intermodulation Error Below 5 kHz**
- **Low Input Offset Voltage**
  10 μV Max (TLC2654A)
- **Excellent Offset Voltage Stability With Temperature . . . 0.05 μV/°C Max**
- **A_{VD} . . . 135 dB Min (TLC2654A)**
- **CMRR . . . 110 dB Min (TLC2654A)**
- **k_{SVR} . . . 120 dB Min (TLC2654A)**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **No Noise Degradation With External Capacitors Connected to V_{DD-}**

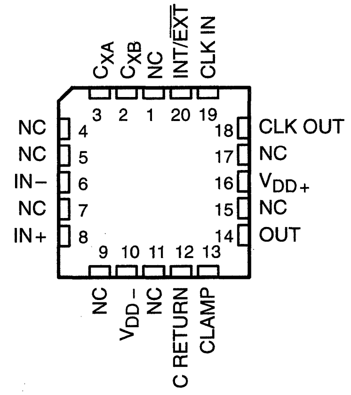
D, JG, OR P PACKAGE
(TOP VIEW)



D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC2654 and TLC2654A are low-noise chopper-stabilized operational amplifiers using the Advanced LinCMOS™ process. Combining this process with chopper-stabilization circuitry makes excellent dc precision possible. In addition, circuit techniques are added that give the TLC2654 and TLC2654A noise performance unsurpassed by similar devices.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES							CHIP FORM (Y)
		8 PIN			14 PIN			20 PIN	
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)	SMALL OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)	CERAMIC DIP (FK)	
0°C to 70°C	10 μV 20 mV	TLC2654AC-8D TLC2654C-8D	— —	TLC2654ACP TLC2654CP	TLC2654AC-14D TLC2654C-14D	— —	TLC2654ACN TLC2654CN	— —	TLC2654Y
–40°C to 85°C	10 μV 20 μV	TLC2654AI-8D TLC2654I-8D	— —	TLC2654AIP TLC2654IP	TLC2654AI-14D TLC2654I-14D	— —	TLC2654AIN TLC2654IN	— —	—
–55°C to 125°C	10 μV 20 μV	TLC2654AM-8D TLC2654M-8D	TLC2654AMJG TLC2654MJG	TLC2654AMP TLC2654MP	TLC2654AM-14D TLC2654M-14D	TLC2654AMJ TLC2654MJ	TLC2654AMN TLC2654MN	TLC2654AMFK TLC2654MFK	—

The 8-pin and 14-pin D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2654AC-8DR).

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

Chopper-stabilization techniques provide for extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power-supply voltage. The high chopping frequency of the TLC2654 and TLC2654A (see Figure 1) provides excellent noise performance in a frequency spectrum from near dc to 10 kHz. In addition, intermodulation or aliasing error is eliminated from frequencies up to 5 kHz.

This high dc precision and low noise, coupled with the extremely high input impedance of the CMOS input stage, makes the TLC2654 and TLC2654A ideal choices for a broad range of applications such as low-level, low-frequency thermocouple amplifiers and strain gauges and wide-bandwidth and subsonic circuits. For applications requiring even greater dc precision, use the TLC2652 or TLC2652A devices, which have a chopping frequency of 450 Hz.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

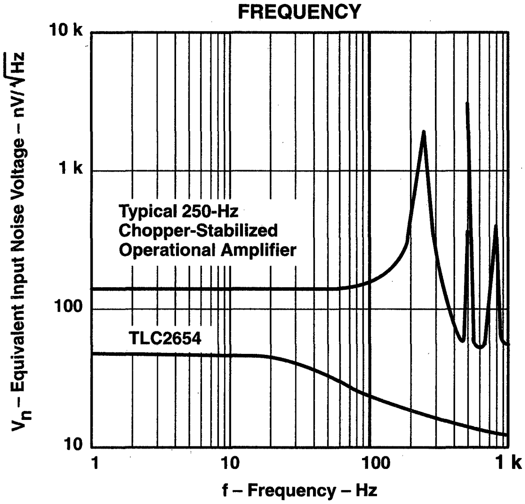


Figure 1

The TLC2654 and TLC2654A common-mode input voltage range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±2.3 V.

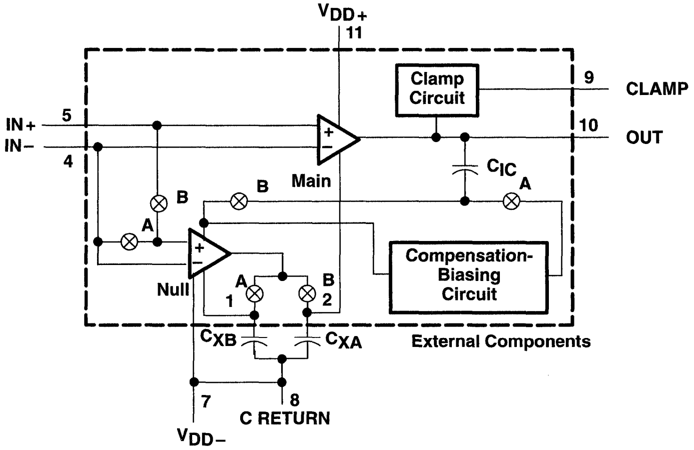
Two external capacitors are required to operate the device; however, the on-chip chopper-control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is accessible, allowing the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold of the TLC2554 and TLC2654A requires no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques used on the TLC2654 and TLC2654A allow exceptionally fast overload recovery time. An output clamp pin is available to reduce the recovery time even further.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up. In addition, the TLC2654 and TLC2654A incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, exercise care in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to125°C.

functional block diagram

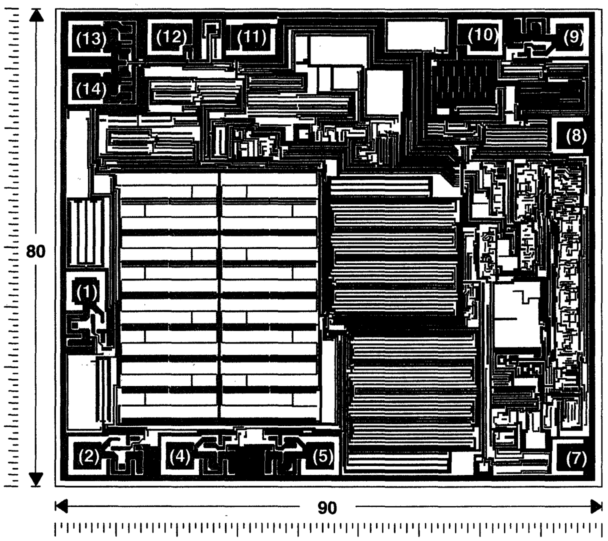


Pin numbers shown are for the D (14 pin), J, and N packages.

TLC2654Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2654C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (7) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

FOR THE PINOUT, SEE THE FUNCTIONAL BLOCK DIAGRAM.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	±8 V
Voltage range on CLK IN and INT/$\overline{\text{EXT}}$	V_{DD-} to V_{DD-} + 5.2 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Current into CLK IN and INT/$\overline{\text{EXT}}$	±5 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	–40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or JG package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (8 pin)	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D (14 pin)	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.3	±8	±2.3	±8	±2.3	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} –2.3	V_{DD-}	V_{DD+} –2.3	V_{DD-}	V_{DD+} –2.3	V
Clock input voltage	V_{DD-}	V_{DD-} +5	V_{DD-}	V_{DD-} +5	V_{DD-}	V_{DD-} +5	V
Operating free-air temperature, T_A	0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2654C			TLC2654AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 4)	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		5	20		4	10	µV
			Full range			34			24	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.01	0.05		0.01	0.05	µV/°C
	Input offset voltage long-term drift (see Note 5)		25°C		0.003	0.06		0.003	0.02	µV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 6	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 6	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 10\ k\Omega$	25°C	120	155		135	155		dB
			Full range	120			130			
	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}\min$, $R_S = 50\ \Omega$	25°C	105	125		110	125		dB
			Full range	105			110			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.3$ V to ±8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	110	125		120	125		dB
			Full range	110			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

† Full range is 0°C to 70°C.

NOTES:
4. This parameter is not production tested full range. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high-speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.
5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$° using the Arrhenius equation and assuming an activation energy of 0.96 eV.
6. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2654C			TLC2654AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.3			1.3			
SR−	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 7)	f = 10 Hz	25°C		47			47	75	nV/√Hz
		f = 1 kHz			13			13	20	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		μV
		f = 0 to 10 Hz			1.5			1.5		
I_n	Equivalent input noise current	f = 10 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

† Full range is 0°C to 70°C.

NOTE 7: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2654I			TLC2654AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 4)	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		5	20		4	10	µV
			Full range			40			30	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.01	0.05		0.01	0.05	µV/°C
	Input offset voltage long-term drift (see Note 5)		25°C		0.003	0.06		0.003	0.02	µV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			200			200	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			200			200	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 6	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 6	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	120	155		135	155		dB
			Full range	120			125			
	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	105	125		110	125		dB
			Full range	105			110			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	110	125		120	125		dB
			Full range	110			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

† Full range is −40°C to 85°C

NOTES: 4. This parameter is not production tested full range. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high-speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.

5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2654I			TLC2654AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	1.5	2		1.5	2		V/µs
			Full range	1.2			1.2			
SR−	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/µs
			Full range	1.5			1.5			
V_n	Equivalent input noise voltage (see Note 7)	f = 10 Hz	25°C		47			47	75	nV/√Hz
		f = 1 kHz			13			13	20	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		µV
		f = 0 to 10 Hz			1.5			1.5		
I_n	Equivalent input noise current	f = 10 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

† Full range is −40°C to 85°C.

NOTE 7: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2654M			TLC2654AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 4)	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		5	20		4	10	µV
			Full range			50			40	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.01	0.05*		0.01	0.05*	µV/°C
	Input offset voltage long-term drift (see Note 5)		25°C		0.003	0.06*		0.003	0.02*	µV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 6	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 6	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	120	155		135	155		dB
			Full range	120			120			
	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			500			500	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	105	125		110	125		dB
			Full range	105			110			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	110	125		120	125		dB
			Full range	105			115			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

∗ On products complaint to MIL-STD-883, Class B, this parameter is not production tested.

† Full range is −55°C to 125°C.

NOTES: 4. This parameter is not production tested full range. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high-speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.

5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2654M TLC2654AM MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	1.5	2		V/μs
			Full range	1.1			
SR–	Negative slew rate at unity gain		25°C	2.3	3.7		V/μs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		47		nV/√Hz
		f = 1 kHz	25°C		13		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5		μV
		f = 0 to 10 Hz	25°C		1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°		

† Full range is –55°C to 125°C.

electrical characteristics, $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC2654Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 4)	V_{IC} = 0, R_S = 50 Ω		5	20	μV
	Input offset voltage long-term drift (see Note 5)			0.003	0.06	μV/mo
I_{IO}	Input offset current			30		pA
I_{IB}	Input bias current			50		pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 5	4.7	4.8		V
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 5	−4.7	−4.9		V
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	120	155		dB
f_{ch}	Internal chopping frequency			10		Hz
	Clamp on-state current	R_L = 100 kΩ	25			μA
	Clamp off-state current	V_O = −4 V to 4 V			100	pA
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω	105	125		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V, V_O = 0, R_S = 50 Ω	110	125		dB
I_{DD}	Supply current	V_O = 0, No load		1.5	2.4	mA

NOTES: 4. This parameter is not production tested full range. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high-speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.

5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, $V_{DD\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC2654Y			UNIT
			MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	1.5	2		V/μs
SR−	Negative slew rate at unity gain		2.3	3.7		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz		47		nV/√Hz
		f = 1 kHz		13		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz		0.5		μV
		f = 0 to 10 Hz		1.5		
I_n	Equivalent input noise current	f = 1 kHz		0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF		48°		

TYPICAL CHARACTERISTICS

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V_{IO}	Input offset voltage	Distribution	1
	Normalized input offset voltage	vs Chopping frequency	2
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$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	13 14
	Chopping frequency	vs Supply voltage vs Free-air temperature	15 16
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$V_{N(PP)}$	Peak-to-peak input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
k_{SVR}	Supply voltage rejection ratio	vs Frequency	28
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	29 30
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance	31 32
	Phase shift	vs Frequency	13

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2654 INPUT OFFSET VOLTAGE

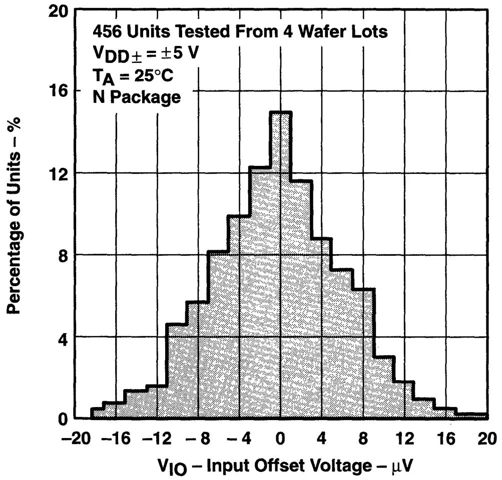

Figure 2

NORMALIZED INPUT OFFSET VOLTAGE vs CHOPPING FREQUENCY

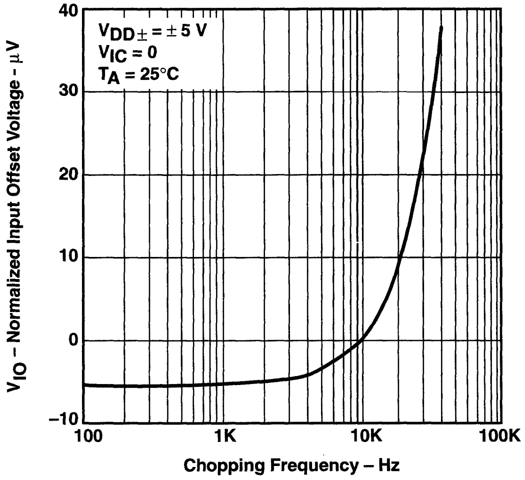

Figure 3

INPUT OFFSET CURRENT vs CHOPPING FREQUENCY

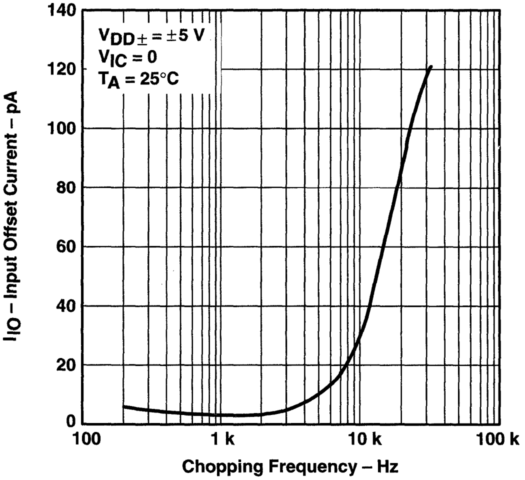

Figure 4

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

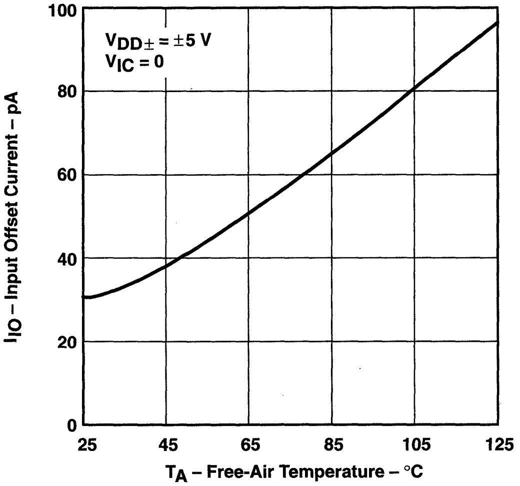

Figure 5

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

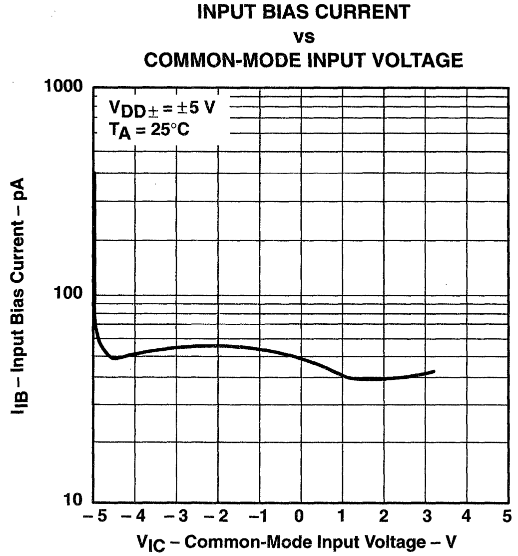

Figure 6

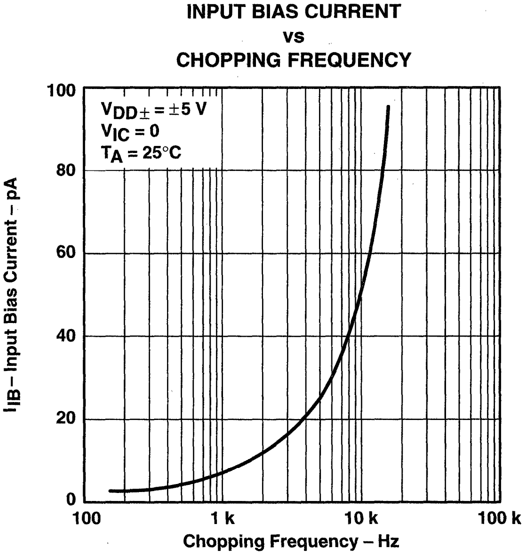

Figure 7

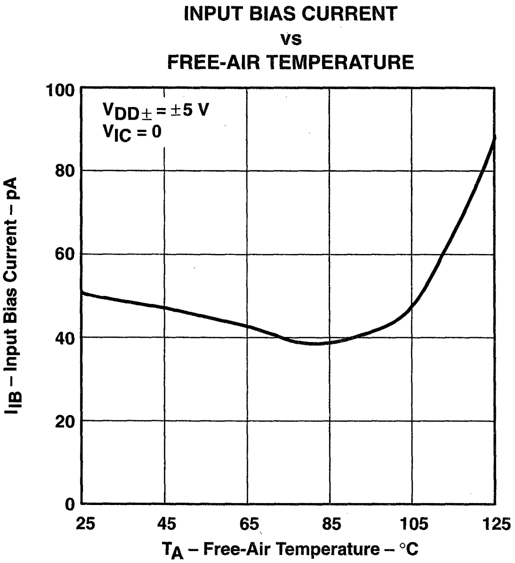

Figure 8

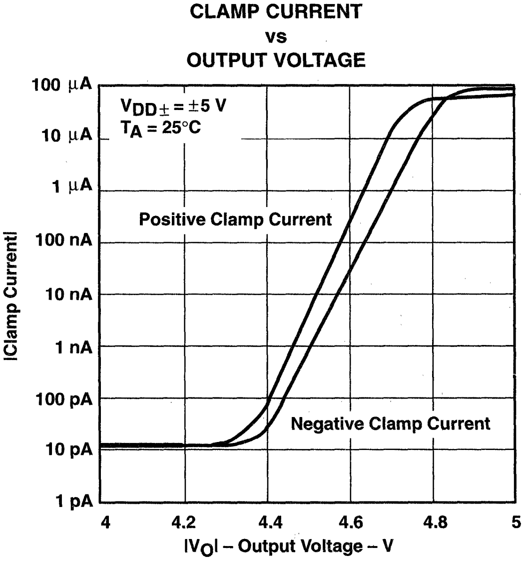

Figure 9

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

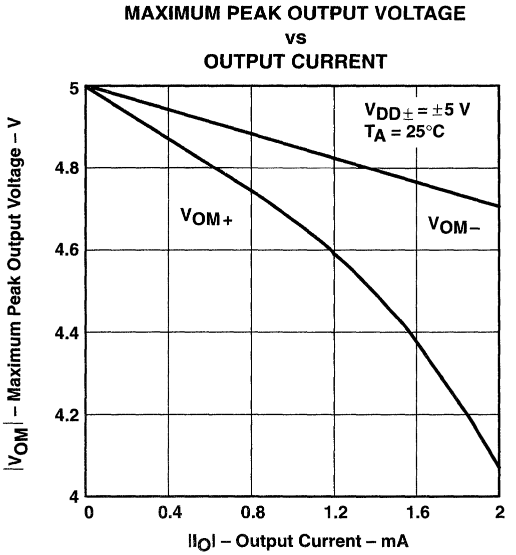

Figure 10

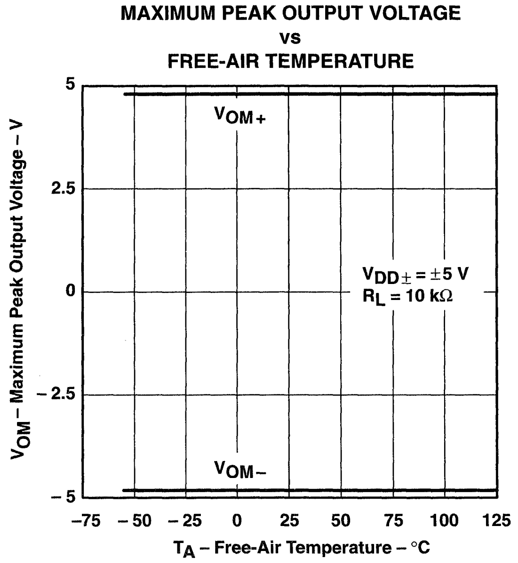

Figure 11

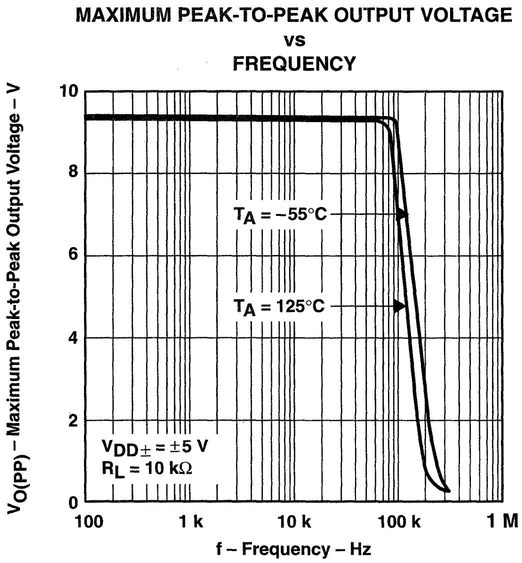

Figure 12

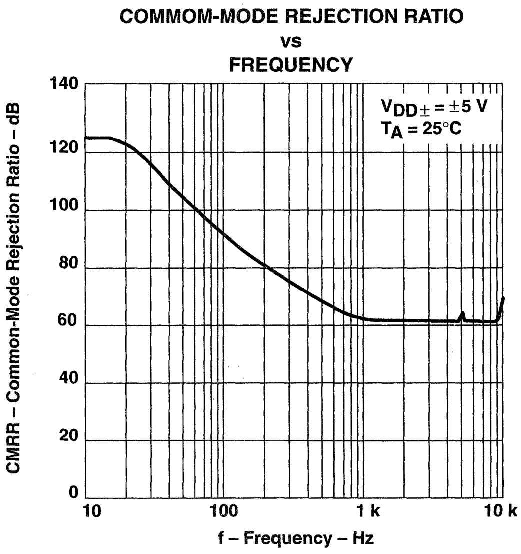

Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

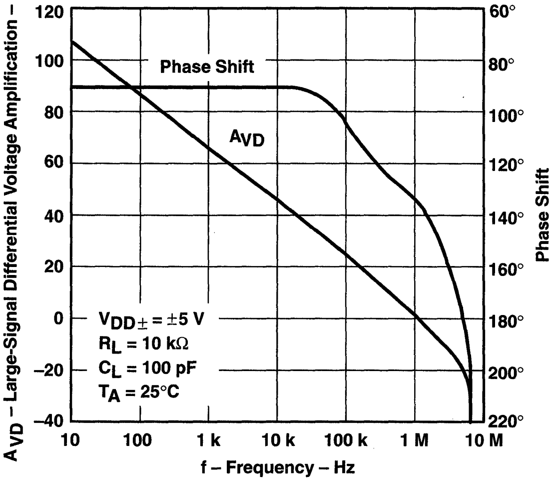

Figure 14

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

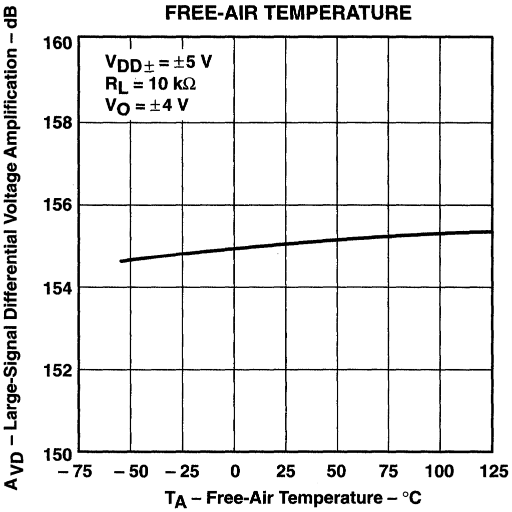

Figure 15

CHOPPING FREQUENCY
vs
SUPPLY VOLTAGE

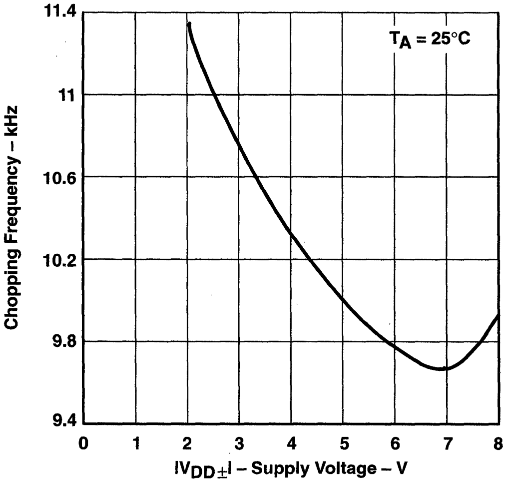

Figure 16

CHOPPING FREQUENCY
vs
FREE-AIR TEMPERATURE

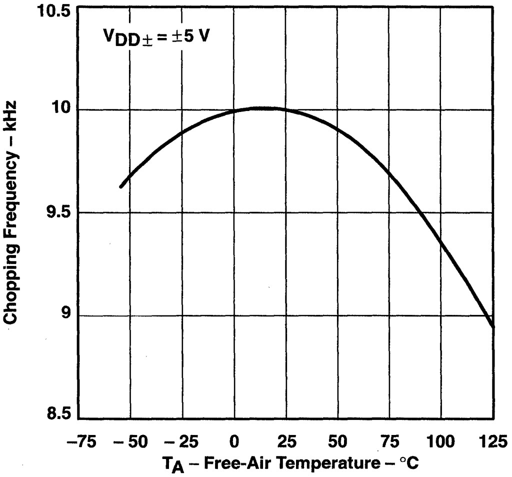

Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT vs SUPPLY VOLTAGE

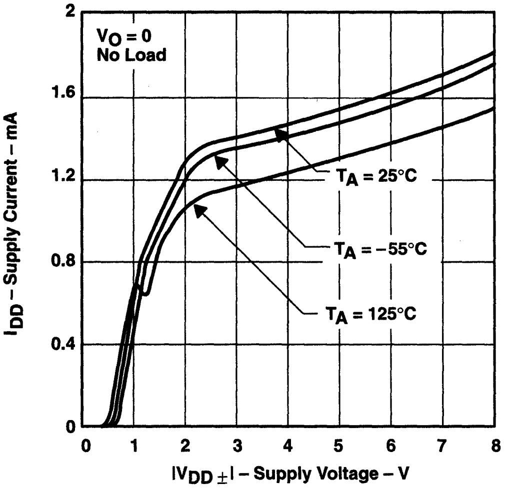

Figure 18

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

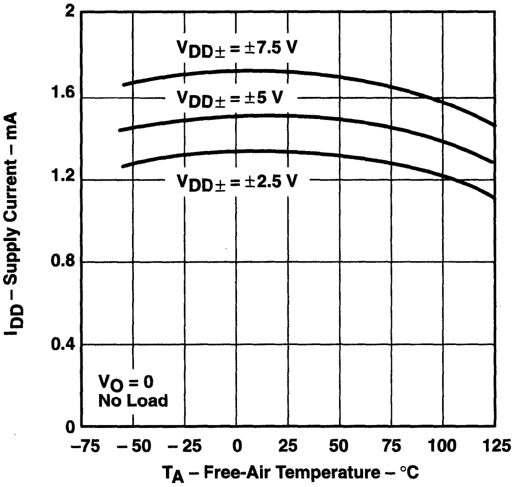

Figure 19

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

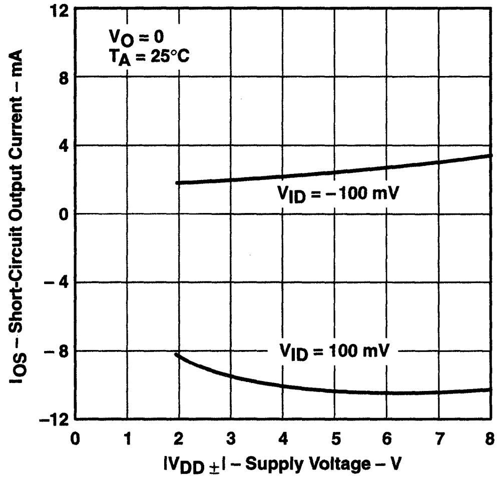

Figure 20

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

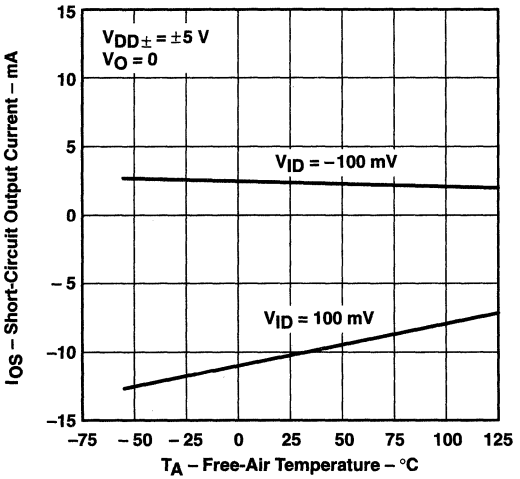

Figure 21

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

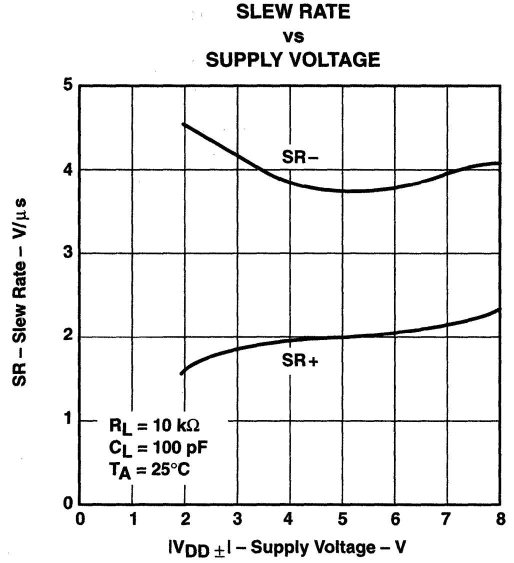

Figure 22

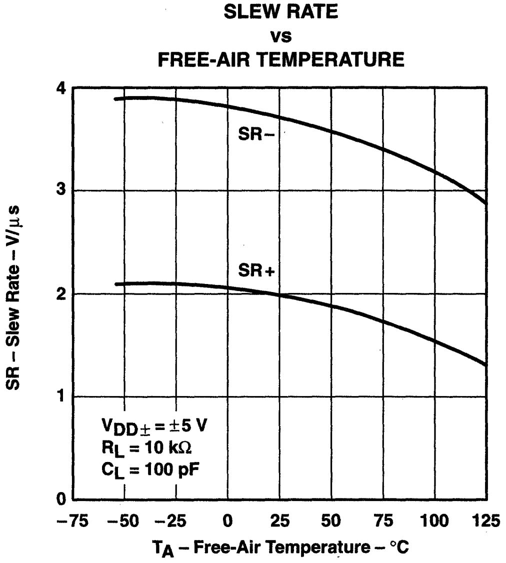

Figure 23

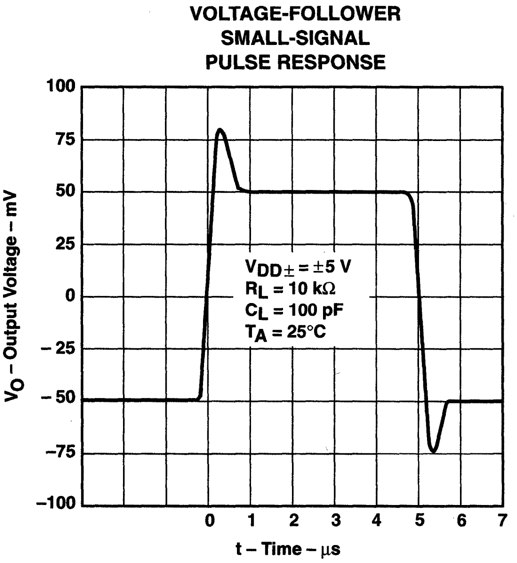

Figure 24

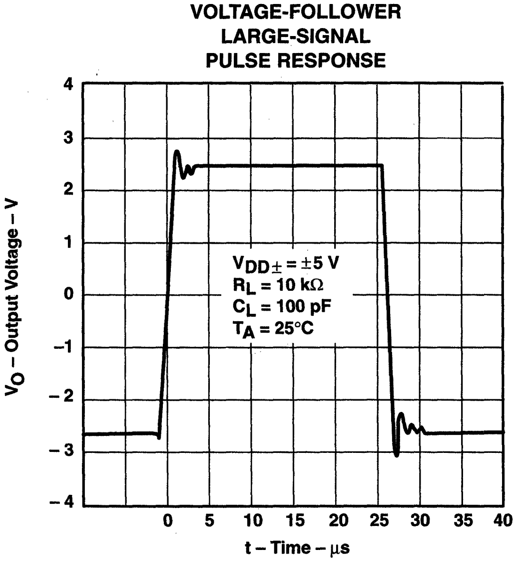

Figure 25

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

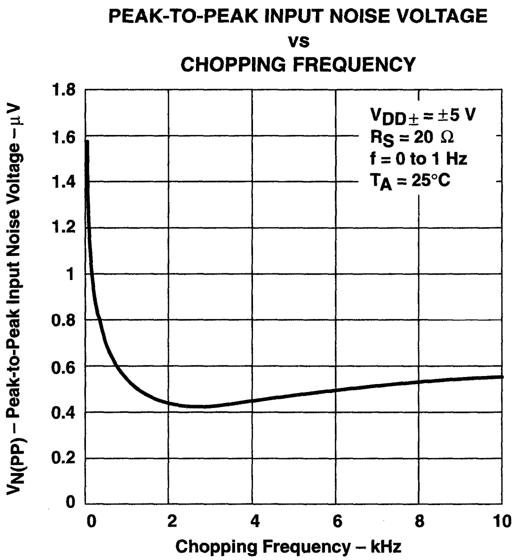

Figure 26

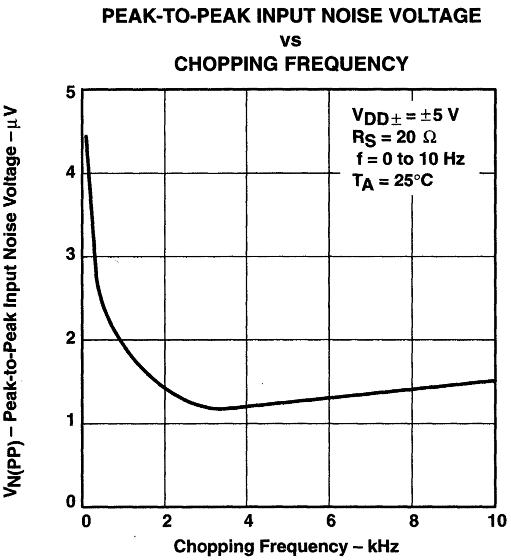

Figure 27

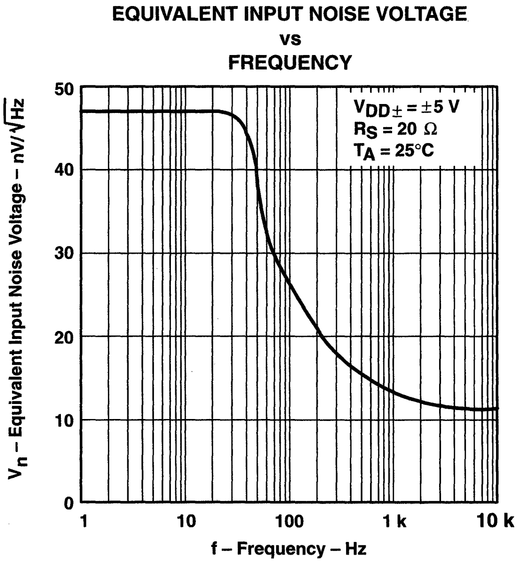

Figure 28

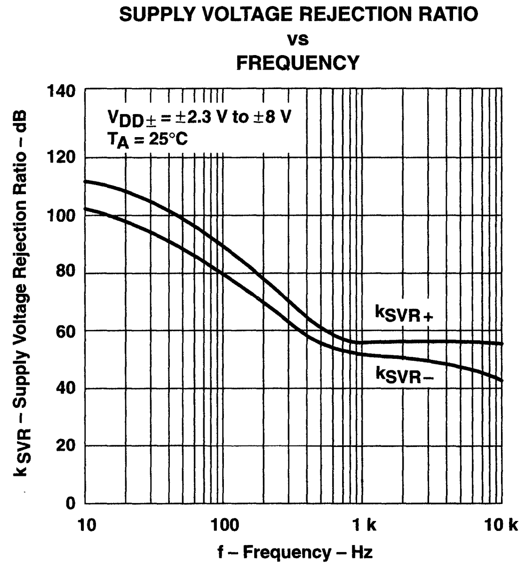

Figure 29

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

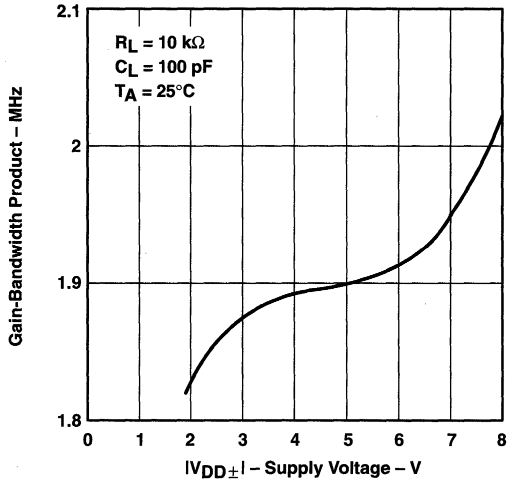

Figure 30

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

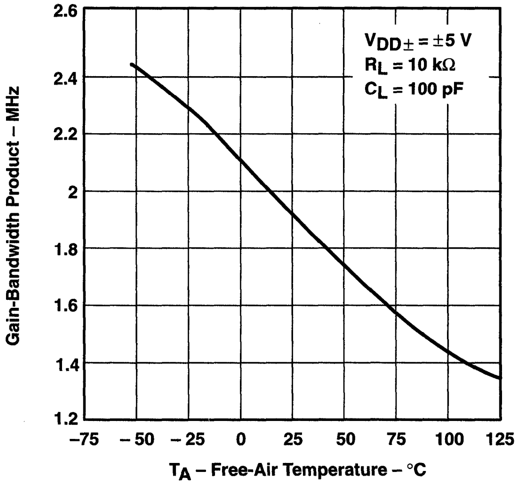

Figure 31

PHASE MARGIN
vs
SUPPLY VOLTAGE

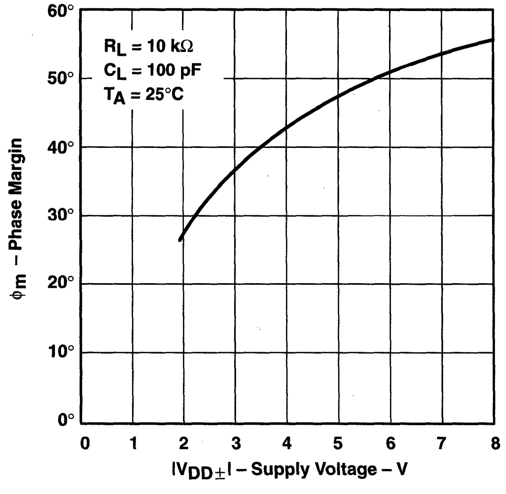

Figure 32

PHASE MARGIN
vs
LOAD CAPACITANCE

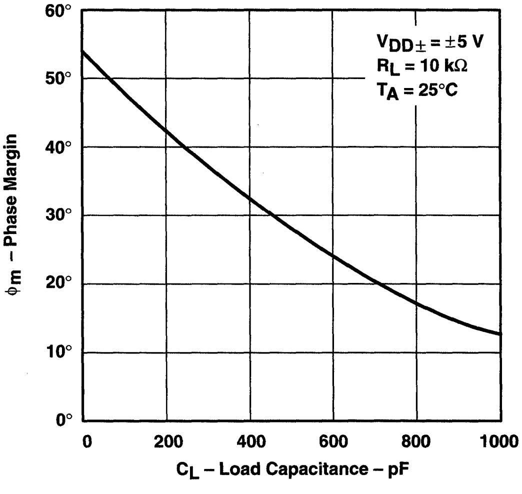

Figure 33

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

capacitor selection and placement

Leakage and dielectric absorption are the two important factors to consider when selecting external capacitors C_{XA} and C_{XB}. Both factors can cause system degradation, negating the performance advantages realized by using the TLC2654.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guard bands are recommended around the capacitor connections on both sides of the printed-circuit board to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications needing fast settling of input voltage, high-quality film capacitors such as mylar, polystyrene, or polypropylene should be used. In other applications, a ceramic or other low-grade capacitor can suffice.

Unlike many choppers available today, the TLC2654 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to C_{XA} and C_{XB} and return to either V_{DD-} or C RETURN. On many choppers, connecting these capacitors to V_{DD-} causes degradation in noise performance; this problem is eliminated on the TLC2654.

internal/external clock

The TLC2654 has an internal clock that sets the chopping frequency to a nominal value of 10 kHz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package the device chopping frequency can be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN. To use the internal 10-kHz clock, no connection is necessary. If external clocking is desired, connect INT/$\overline{\text{EXT}}$ to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, CLK IN can be driven from the negative rail to 5 V above the negative rail. This allows the TLC2654 to be driven directly by 5-V TTL and CMOS logic when operating in the single-supply configuration. If this 5-V level is exceeded, damage could occur to the device unless the current into CLK IN is limited to ±5 mA. A divide-by-two frequency divider interfaces with CLK IN and sets the chopping frequency. The chopping frequency appears on CLK OUT.

overload recovery/output clamp

When large differential-input-voltage conditions are applied to the TLC2654, the nulling loop attempts to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 34). Typical overload recovery time for the TLC2654 is significantly faster than competitive products; however, this time can be reduced further by use of internal clamp circuitry accessible through CLAMP if required.

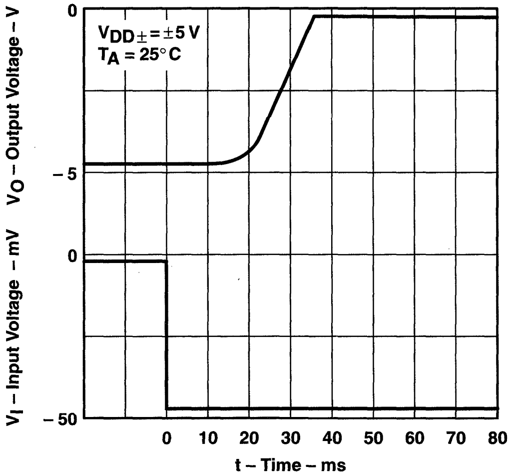


Figure 34. Overload Recovery

APPLICATION INFORMATION

overload recovery/output clamp (continued)

The clamp is a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced and the TLC2654 output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 9), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage temperature coefficient of the TLC2654, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed-circuit board). It is not uncommon for dissimilar metal junctions to produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01 µV/°C typical of the TLC2654).

To help minimize thermoelectric effects, pay careful attention to component selection and circuit-board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latch-up avoidance

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2654 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques to reduce the chance of latch-up should be used whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be stunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latch-up occurring increases with increasing temperature and supply voltage.

electrostatic-discharge protection

The TLC2654 incorporates internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

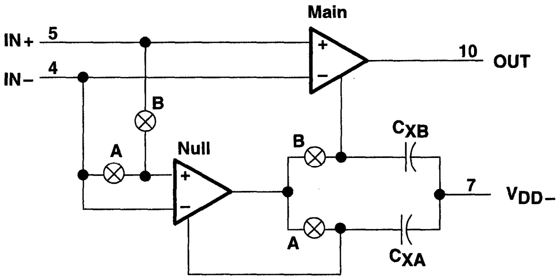
Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2654 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2654 on-chip control logic produces two dominant clock phases: a nulling phase and an amplifying phase. The term chopper-stabilized derives from the process of switching between these two clock phases. Figure 35 shows a simplified block diagram of the TLC2654. Switches A and B are make-before-break types.

APPLICATION INFORMATION

theory of operation (continued)

During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.



Pin numbers shown are for the D (14 pin), J, and N packages.

Figure 35. TLC2654 Simplified Block Diagram

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common-mode input voltage range and power supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process, with its low-noise analog MOS transistors and patent-pending input stage design, significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches. As charge imbalance accumulates on critical nodes, input offset voltage can increase especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2654 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

The TLC2654 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

The primary limitation on ac performance is the chopping frequency. As the input signal frequency approaches the chopper's clock frequency, intermodulation (or aliasing) errors result from the mixing of these frequencies. To avoid these error signals, the input frequency must be less than half the clock frequency. Most choppers available today limit the internal chopping frequency to less than 500 Hz in order to eliminate errors due to the charge imbalancing phenomenon mentioned previously. However, to avoid intermodulation errors on a 500-Hz chopper, the input signal frequency must be limited to less than 250 Hz.

APPLICATION INFORMATION

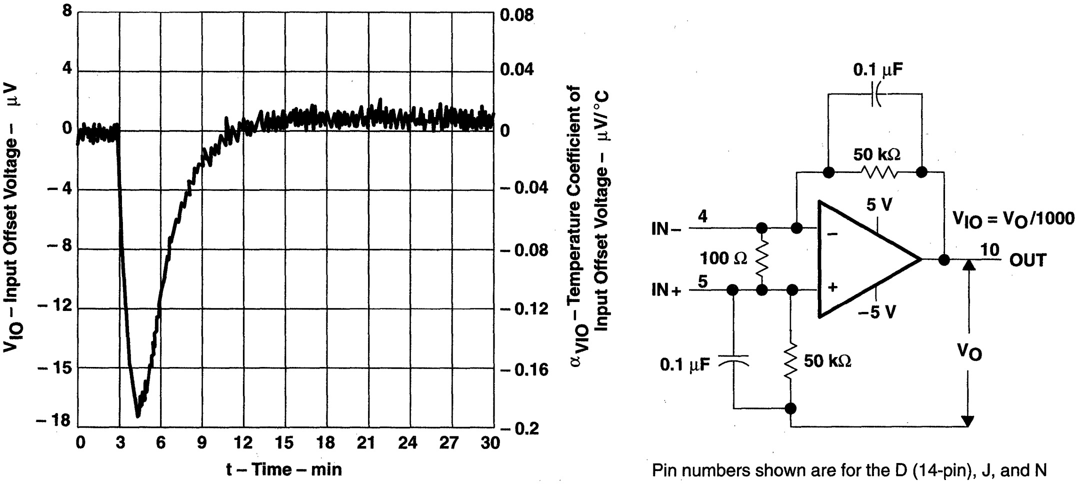
theory of operation (continued)

The TLC2654 removes this restriction on ac performance by using a 10-kHz internal clock frequency. This high chopping frequency allows amplification of input signals up to 5 kHz without errors due to intermodulation and greatly reduces low-frequency noise.

THERMAL INFORMATION

temperature coefficient of input offset voltage

Figure 36 shows the effects of package-included thermal EMF. The TLC2654 can null only the offset voltage within its nulling loop. There are metal-to-metal junctions outside the nulling loop (bonding wires, solder joints, etc.) that produce EMF. In Figure 36, a TLC2654 packaged in a 14-pin plastic package (N package) was placed in an oven at 25°C at t = 0, biased up, and allowed to stabilize. At t = 3 min, the oven was turned on and allowed to rise in temperature to 125°C. As evidenced by the curve, the overall change in input offset voltage with temperature is less than the specified maximum limit of 0.05 µV/°C.



Pin numbers shown are for the D (14-pin), J, and N packages.

Figure 36. Effects of Package-Induced Thermal EMF

TLC2801Z, TLC2801Y
Advanced LinCMOS™ LOW-NOISE PRECISION OPERATIONAL AMPLIFIERS

SLOS116B – JULY 1982 – REVISED SEPTEMBER 1996

- **Low Input Noise Voltage:**
  35 nV/√Hz Max at f = 10 Hz
  15 nV/√Hz Max at f = 1 kHz
- **Low Input Offset Voltage:**
  500 µV Max at T_A = 25°C
  1.5 mV Max at T_A = Full Range
- **Excellent Offset Voltage Stability With Temperature . . . 4 µV/°C Typ**
- **Low Input Bias Current:**
  1 pA Typ at T_A = 25°C
  250 pA Typ at T_A = 150°C
- **Specified for Both Single-Supply and Split-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**

description

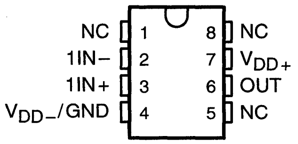
The TLC2801 is a precision, low-noise operational amplifier manufactured using Texas Instruments Advanced LinCMOS™ process. The TLC2801 combines the noise performance of the lowest-noise JFET amplifiers with the dc precision available previously only in bipolar amplifiers. The Advanced LinCMOS™ process uses silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. In addition, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The combination of excellent dc and noise performance with a common-mode input voltage range that includes the negative rail makes the TLC2801 an ideal choice for high-impedance, low-level signal conditioning applications in either single-supply or split-supply configurations.

The device inputs and output are designed to withstand −100-mA surge currents without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

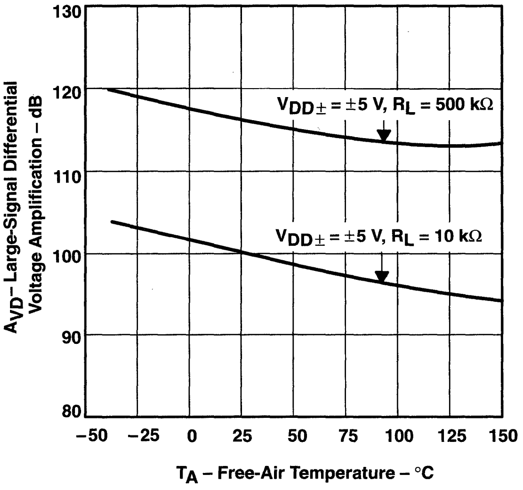
The TLC2801 is characterized for operation over the temperature range of −40°C to 150°C.

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE



AVAILABLE OPTIONS

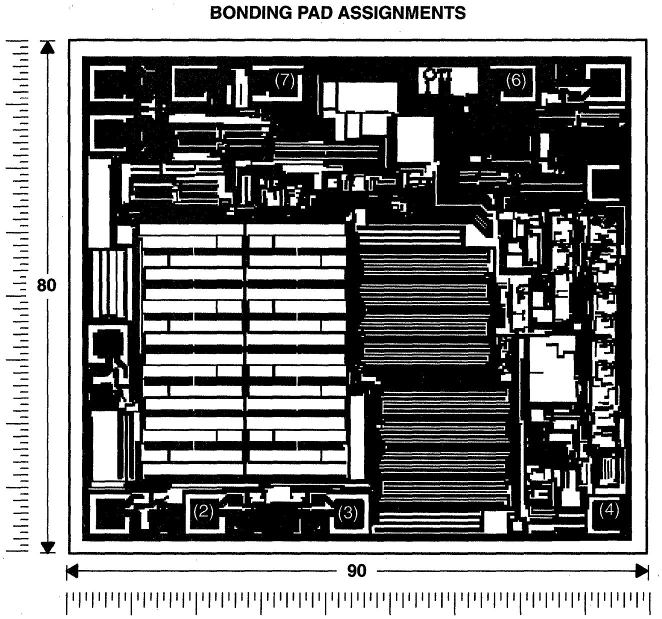
T_A	V_{IO}max AT 150°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
−40°C to 150°C	1.5 mV	TLC2801ZD	TLC2801ZP	TLC2801Y

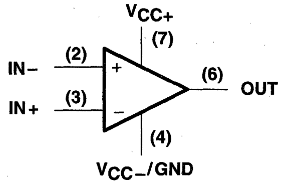
The D packages are available taped and reeled. Add R suffix to the device type when ordering (e.g., TLC2801ZDR).

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

TLC2801Y chip information

This chip, properly assembled, displays characteristics similar to the TLC2801. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

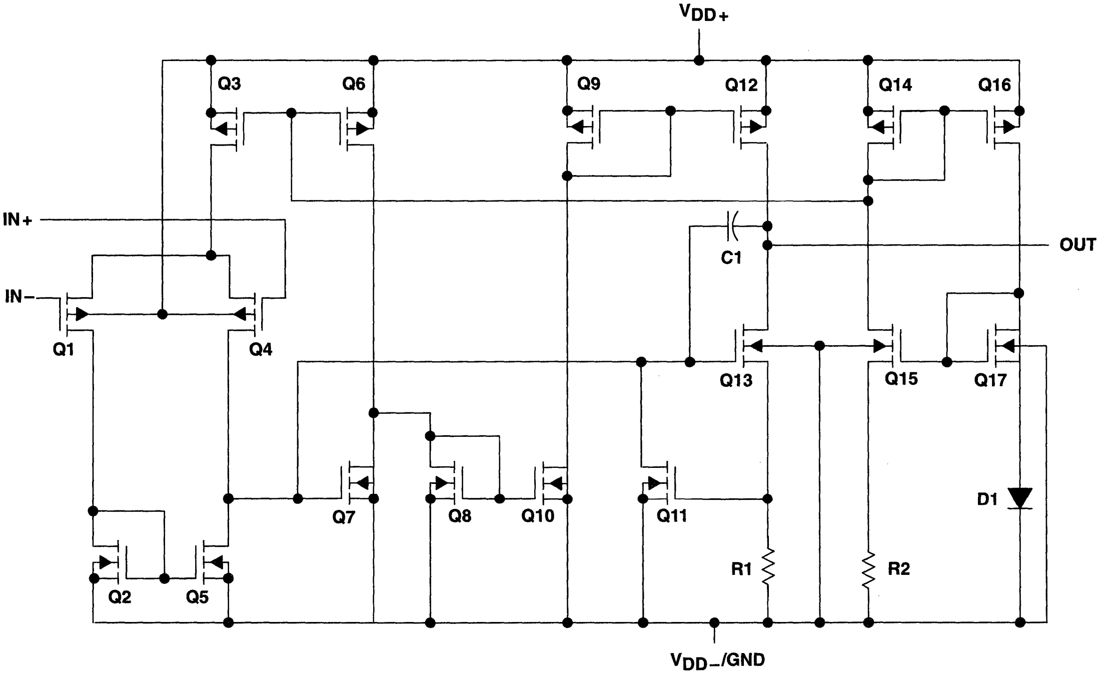
$T_J$max= 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	−8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage range, V_I (any input, see Note 1)	±8 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Operating free-air temperature range, T_A	−40°C to 150°C
Storage temperature range	−65°C to 175°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between $V_{DD\pm}$ and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting point.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	±2.3	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-2.3$	V
Operating free-air temperature, T_A	−40	150	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2801Z			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	500	µV
			Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage		−55°C to 150°C		4		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			3	nA
I_{IB}	Input bias current		25°C		1		pA
			Full range			30	nA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.5			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.5			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 500\ k\Omega$	25°C	300	460		V/mV
			Full range	100			
		$V_O = \pm4$ V, $R_L = 10\ k\Omega$	25°C	50	100		
			Full range	15			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.3$ V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2801Z			UNIT
				MIN	TYP	MAX	
SR	Slew rate unity gain	$V_O = \pm2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	2	2.7		V/µs
			Full range	1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18	35	nV/√Hz
		f = 1 kHz			8	15	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz			0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°		

† Full range is −40°C to 150°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2801Z MIN	TLC2801Z TYP	TLC2801Z MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		4		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			3	
I_{IB}	Input bias current		25°C		1		pA
			Full range			30	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.4			
V_{OL}	Maximum low-level output voltage		25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		V/mV
			Full range	50			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	5			
CMRR	Common-mode rejection ratio	V_O = 0, $V_{IC} = V_{ICR}$min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2801Z MIN	TLC2801Z TYP	TLC2801Z MAX	UNIT
SR	Slew rate unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/µs
			Full range	0.8			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18	35	nV/√Hz
		f = 1 kHz	25°C		8	15	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

† Full range is −40°C to 150°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2801Z			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC}= 0,	R_S = 50 Ω		100	500	µV
	Input offset voltage long-term drift (see Note 4)				0.001	0.005	µV/mo
I_{IO}	Input offset current				0.5		pA
I_{IB}	Input bias current				1		pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	R_S = 50 Ω	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	R_L = 10 kΩ	4.7	4.8		V
V_{OL}	Maximum low-level output voltage	I_O = 0	I_O = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V,	R_L = 500 kΩ	150	315		V/mV
		V_O = 1 V to 4 V,	R_L = 10 kΩ	25	55		
CMRR	Common-mode rejection ratio	V_O = 0, R_S = 50 Ω	$V_{IC} = V_{ICR}$min, R_S = 50 Ω	90	110		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	V_{DD} = 4.6 V to 16 V	90	110		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		1	1.5	mA

operating characteristics at V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC2801Z			UNIT
				MIN	TYP	MAX	
SR	Positive slew rate at unity gain	V_O = 0.5 V to 2.5 V, C_L = 100 pF	R_L = 10 kΩ,	1.8	2.5		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			18		nV/√Hz
		f = 1 kHz			8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			0.5		µV
		f = 0.1 to 10 Hz			0.7		
I_n	Equivalent input noise current				0.6		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 10 kΩ,		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 100 pF		45°		

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

PARAMETER MEASUREMENT INFORMATION

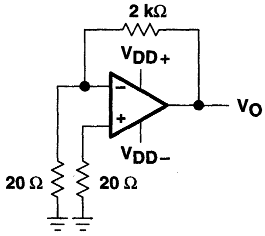
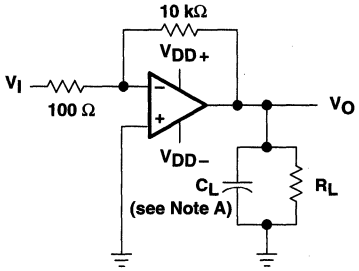
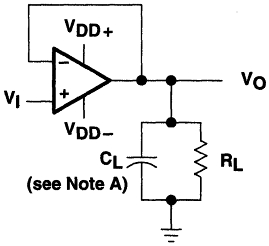


Figure 1. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 2. Phase-Margin Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Slew-Rate Test Circuit

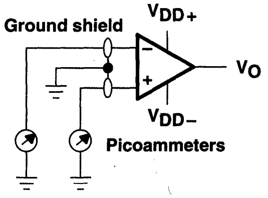


Figure 4. Input-Bias and Offset-Current Test Circuit

typical values

Typical values as presented in this data sheet represents the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias-current level typical of the TLC2801, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltage applied but with no device in the socket. The device is then inserted in the socket and a second test measuring both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	5
V_{OM}	Maximum peak output voltage	vs Free-air temperature	6
V_{OH}	High-level output voltage	vs Free-air temperature	7
V_{OL}	Low-level output voltage	vs Free-air temperature	8
A_{VD}	Differential voltage amplification	vs Free-air temperature	9
I_{OS}	Short-circuit output current	vs Free-air temperature	10
I_{DD}	Supply current	vs Free-air temperature	11
SR	Slew rate	vs Free-air temperature	12
	Gain-bandwidth product	vs Free-air temperature	13

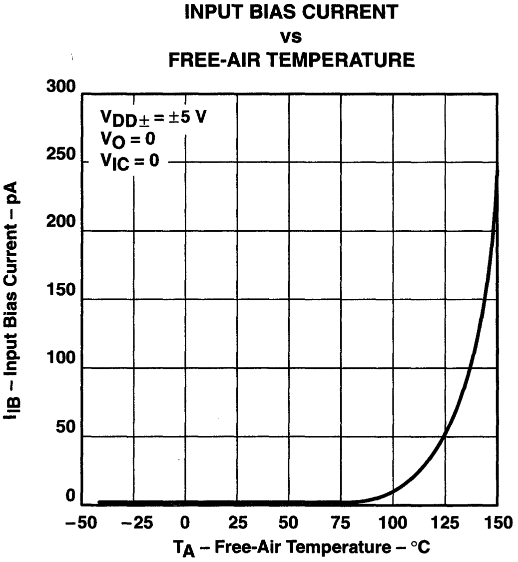


Figure 5

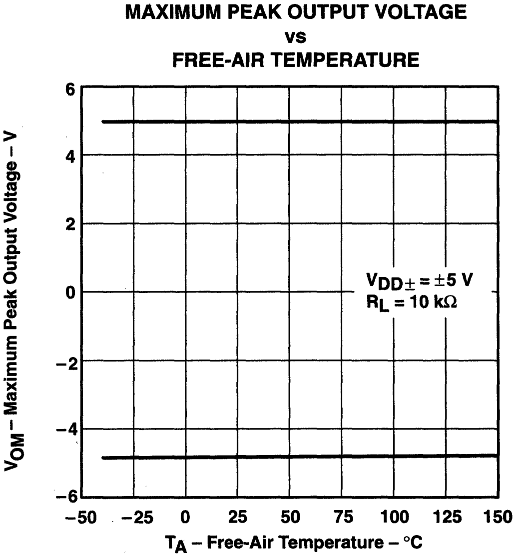


Figure 6

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

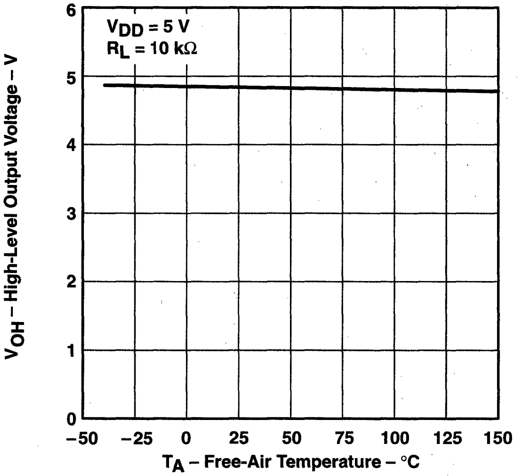


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

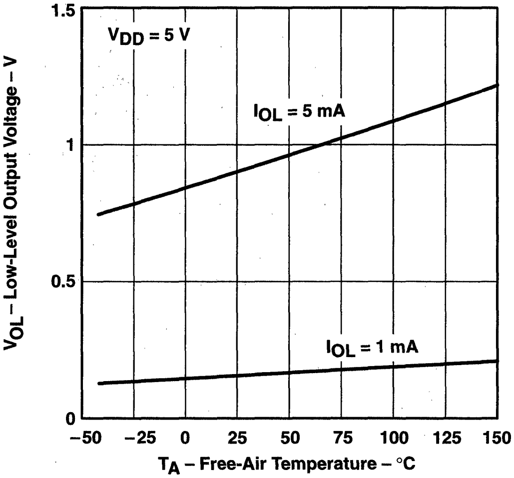


Figure 8

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

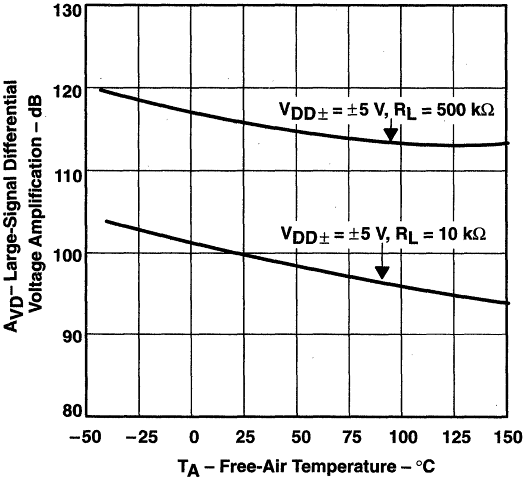


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

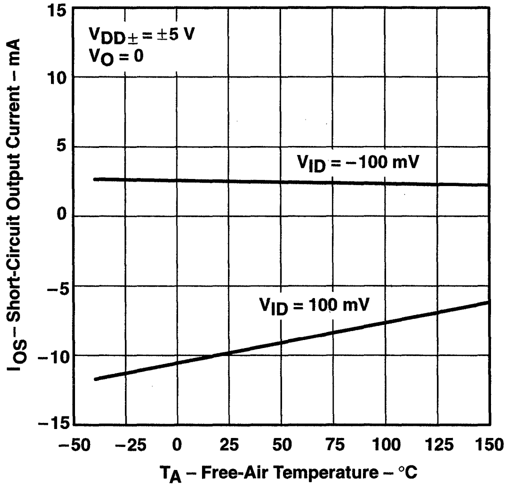


Figure 10

TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

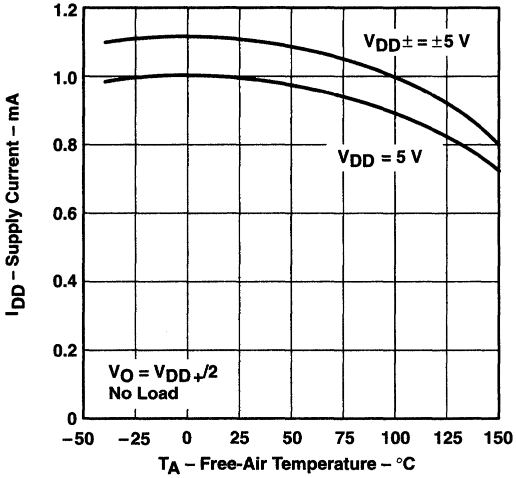


Figure 11

**SLEW RATE
vs
FREE-AIR TEMPERATURE**

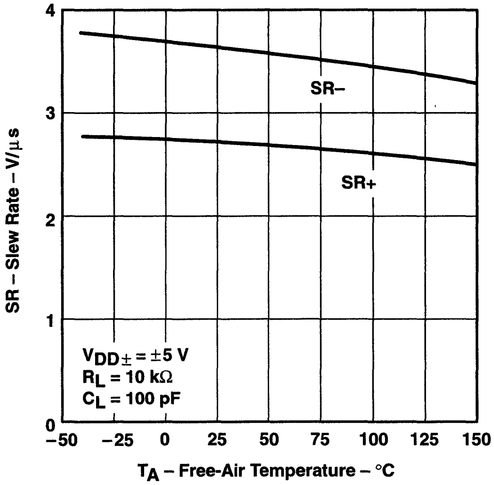


Figure 12

**GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE**

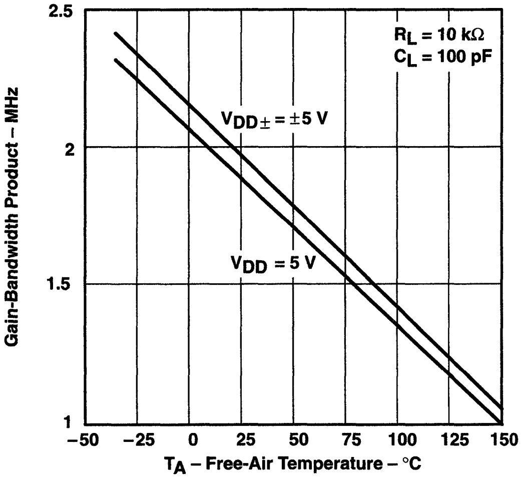


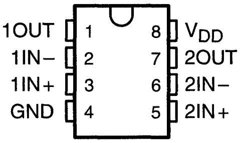
Figure 13

TLC2810Z, TLC2810Y
LinCMOS™ PRECISION
DUAL OPERATIONAL AMPLIFIERS

SLOS120A – AUGUST 1993 – REVISED AUGUST 1994

- **Trimmed Input Offset Voltage:**
  10 mV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically 0.1 µV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  –40°C to 150°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends to the Negative Rail**
- **Low Noise . . . 25 nV/√Hz Typ at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D OR P PACKAGE
(TOP VIEW)



description

The TLC2810Z dual operational amplifiers combine low offset voltage drift with high input impedance, low noise, and speeds approaching that of general-purpose JFET devices. In addition, the use of Texas Instruments silicon-gate LinCMOS technology assures offset stability that greatly exceeds the stability available with conventional metal-gate processes.

The high input impedance, low bias current, and high slew rate make the TLC2810Z ideal for applications that have previously been reserved for JFET and NFET products. These advantages, in combination with an upper operating temperature of 150°C, make the TLC2810Z an ideal choice for precision, extremely high-temperature applications.

In general, many features associated with bipolar technology are available on the TLC2810Z without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are designed easily with the TLC2810Z.

The TLC2810Z package options include a small-outline version for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up at 25°C. The TLC2810Z incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2. However, care should be exercised in handling the TLC2810Z as exposure to ESD may result in the degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD} supply line transients under power conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so can result in a latched condition and device failure.

The TLC2810Z is characterized for operation over the extended temperature range from –40°C to 150°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)†	PLASTIC DIP (P)	
–40°C to 150°C	TLC2810ZD	TLC2810ZP	TLC2810Y

† The D packages are available taped and reeled. Add R suffix to the device type when ordering (e.g., TLC2810ZDR).

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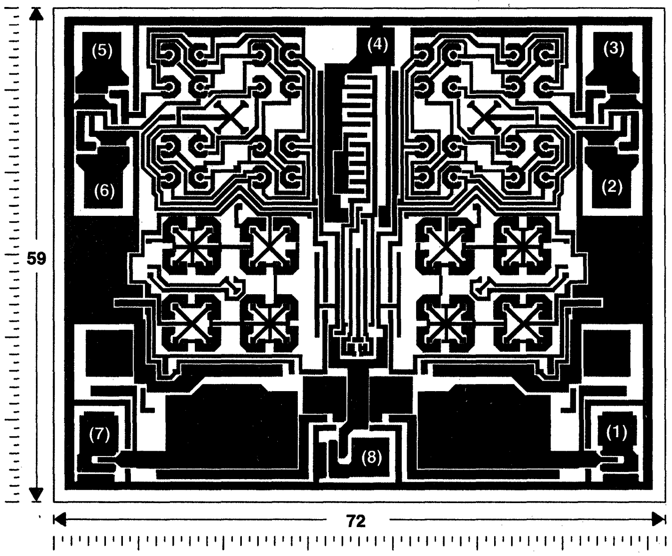
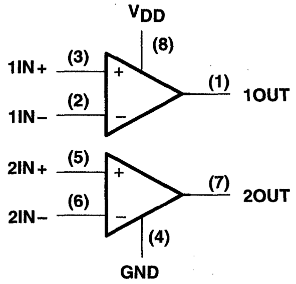
TLC2810Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2810Z. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

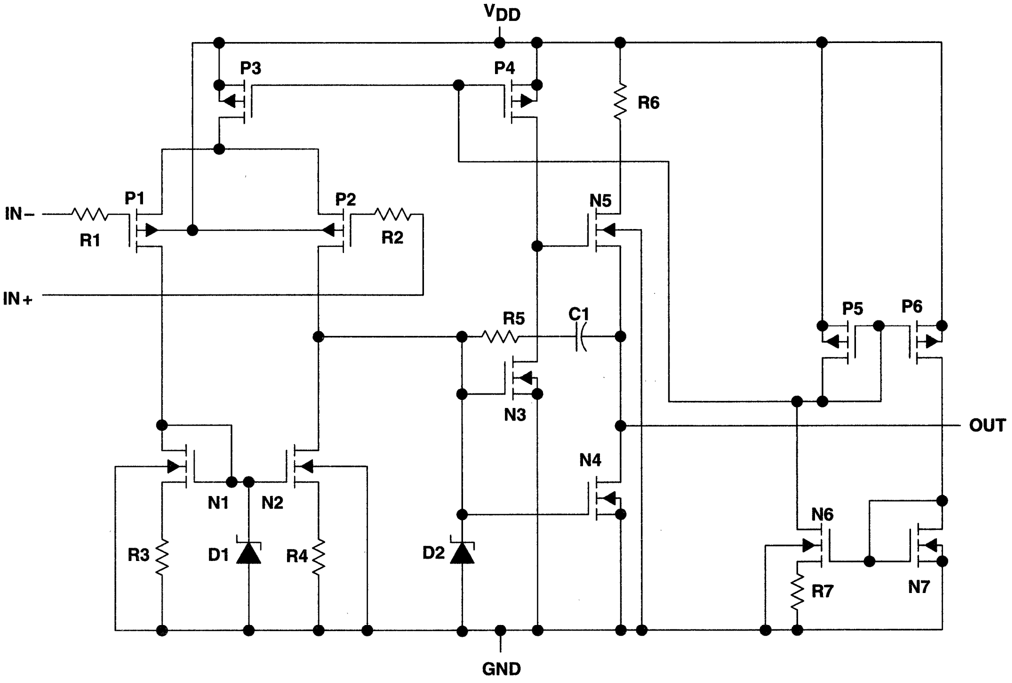
$T_J$max = 165°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	26
Diodes	4
Resistors	14
Capacitors	2

† Includes both amplifiers

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	16 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I	±2 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD}	45 mA
Total current out of GND	45 mA
Duration of short-circuit current at (or below) $T_A = 25°C$ (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−40°C to 150°C
Storage temperature range	−65°C to 165°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application selection).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING	$T_A = 150°C$ POWER RATING
D	812 mV	5.8 mW/°C	551 mW	348 mW	232 mW	87 mW
P	1120 mV	8.0 mW/°C	760 mW	480 mW	320 mW	120 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4	16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V, $T_A = 25°C$	−0.2	3.5	V
Input voltage, V_I	$V_{DD} = 5$ V	−0.2	3.5	V
Operating free-air temperature, T_A		−40	150	°C

electrical characteristics, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2810Z			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.8	10	mV
			Full range			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 150°C		3.5		μV/°C
I_{IO}	Input offset current (see Note 4)	V_{IC} = 1 V, V_O = 1 V	25°C		2.4	100	pA
			150°C		5.2	30	nA
I_{IB}	Input bias current (see Note 4)	V_{IC} = 1 V, V_O = 1 V	25°C		7	100	pA
			150°C		50	150	nA
V_{ICR}	Common-mode input voltage range (see Note 5)	R_S = 50 Ω	25°C	−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	3.2	3.8		V
			Full range	3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		80	150	mV
			Full range			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	25		V/mV
			Full range	4			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	90		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4 V to 16 V, V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	25°C	65	75		dB
			Full range	60			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		1	3.2	mA
			Full range			4.4	

† Full range is −40°C to 150°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC2810Z			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 26	$V_{I(PP)}$ = 1 V	25°C		3.6		V/µs
				150°C		2.8		
			$V_{I(PP)}$ = 2.5 V	25°C		2.2		
				150°C		2.1		
V_n	Equivalent input noise voltage	f =1 kHz, See Figure 27	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 26	25°C		320		kHz
				150°C		200		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 28	C_L = 20 pF,	25°C		1.7		MHz
				150°C		0.8		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 28	25°C		46°		
				150°C		40°		

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC2810Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω			10	mV
I_{IO}	Input offset current (see Note 4)				100	pA
I_{IB}	Input bias current (see Note 4)				100	pA
V_{ICR}	Common-mode input voltage range (see Note 5)	R_S = 50 Ω	−0.2 to 4			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	3.2			V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA			150	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V to 2 V, R_L = 10 kΩ, V_{IC} = 1 V	5			V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, $V_{IC} = V_{ICR}min$, R_S = 50 Ω	65			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4 V to 16 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	65			dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load			3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC2810Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 26	$V_{I(PP)}$ = 1 V		3.6		V/µs
			$V_{I(PP)}$ = 2.5 V		2.9		
V_n	Equivalent input noise voltage	f =1 kHz, R_S = 20 Ω, See Figure 27			25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 26			320		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 28			1.7		MHz
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 28			46°		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1
α_{VIO}	Input offset voltage temperature coefficient	Distribution	2
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Free-air temperature	3 4 5
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	6 7 8 9
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	10 11 21
I_{IB}/I_{IO}	Input bias and offset current	vs Free-air temperature	12
V_{IC}	Common-mode input voltage	vs Supply voltage	13
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	14 15
SR	Slew rate	vs Supply voltage vs Free-air temperature	16 17
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	18
B_1	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	19 20
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	22 23 24
V_n	Equivalent input noise voltage	vs Frequency	25
	Phase shift	vs Frequency	21

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2810Z INPUT OFFSET VOLTAGE

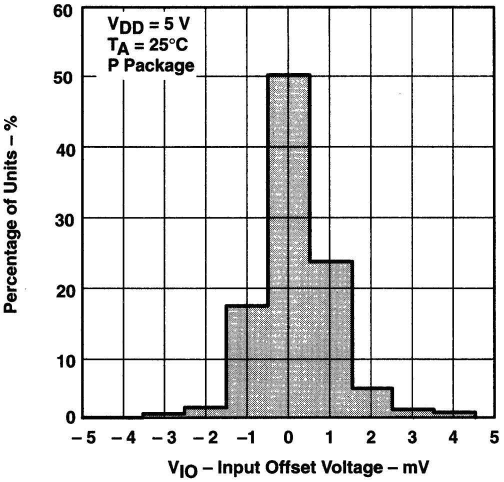


Figure 1

DISTRIBUTION OF TLC2810Z INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

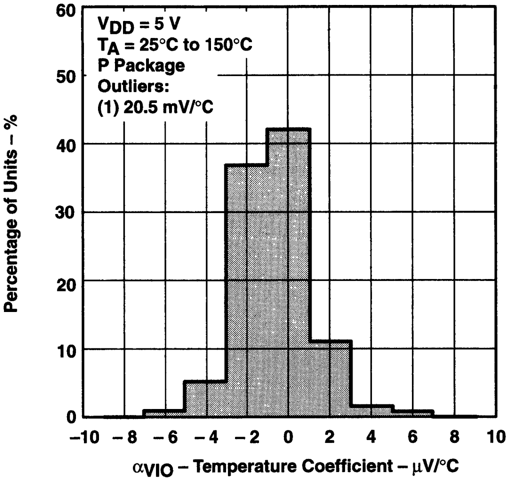


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

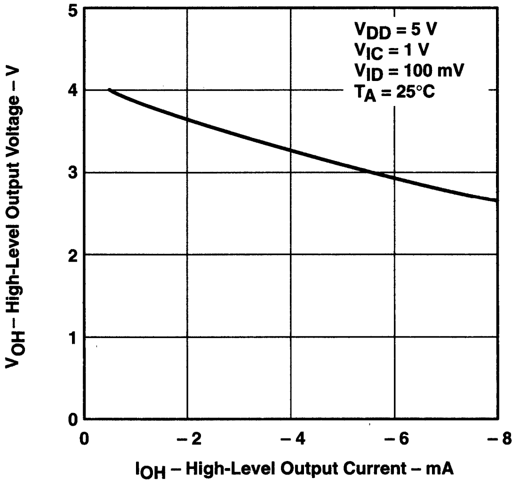


Figure 3

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

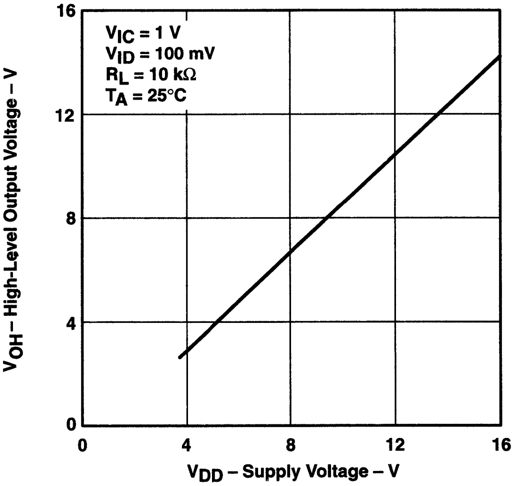


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

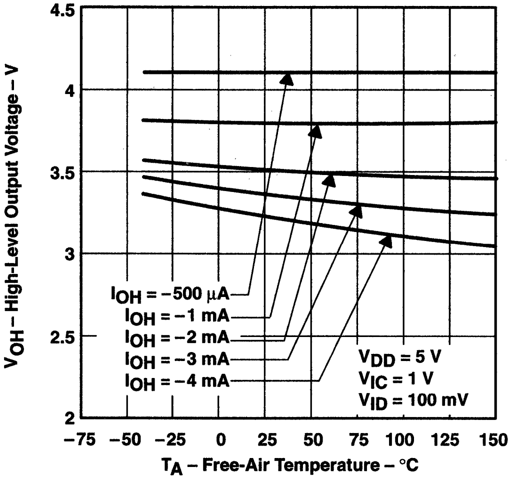


Figure 5

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

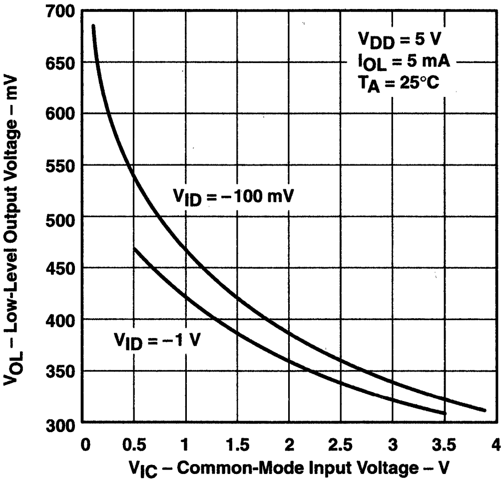


Figure 6

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

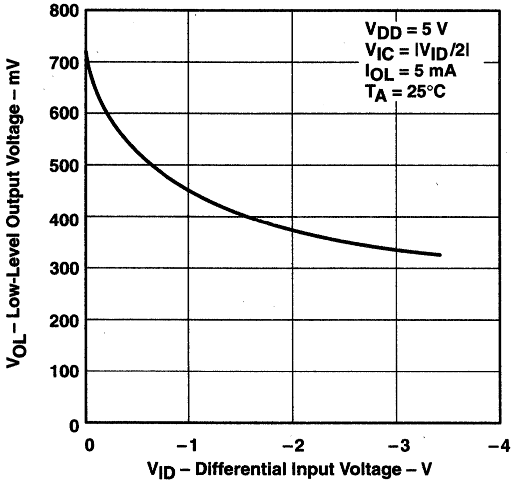


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

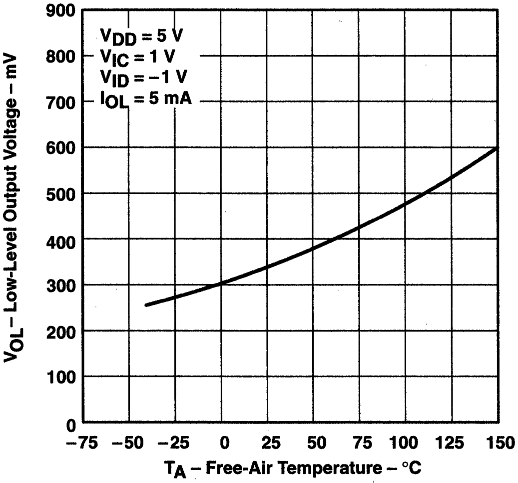


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

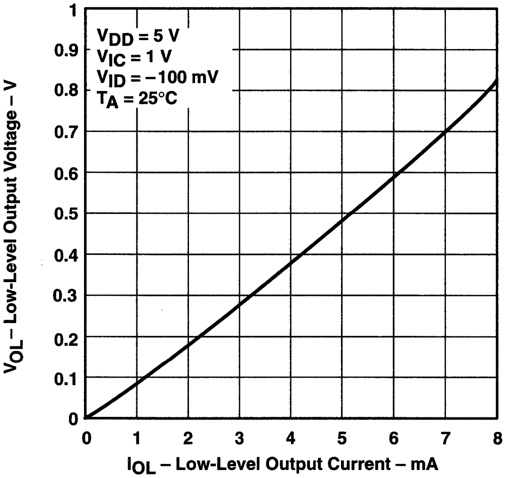


Figure 9

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

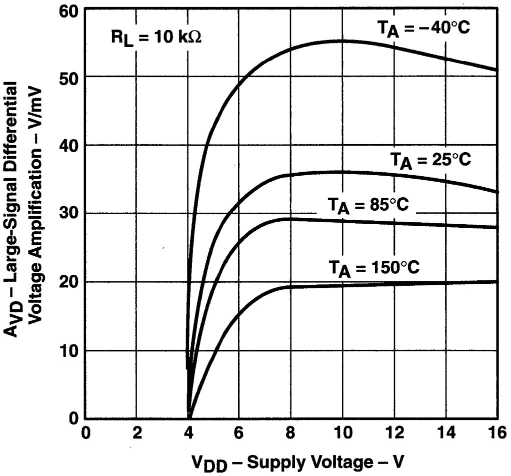


Figure 10

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

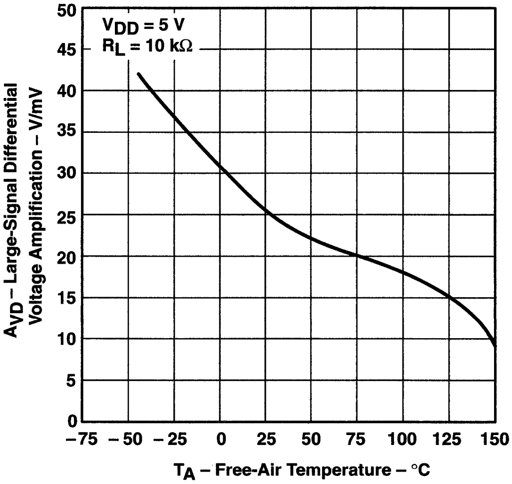
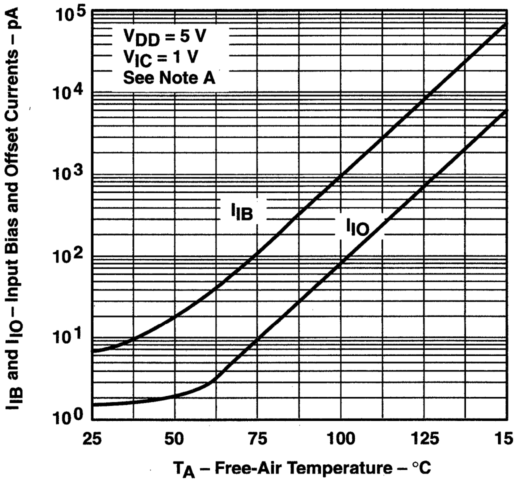


Figure 11

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 12

TYPICAL CHARACTERISTICS

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

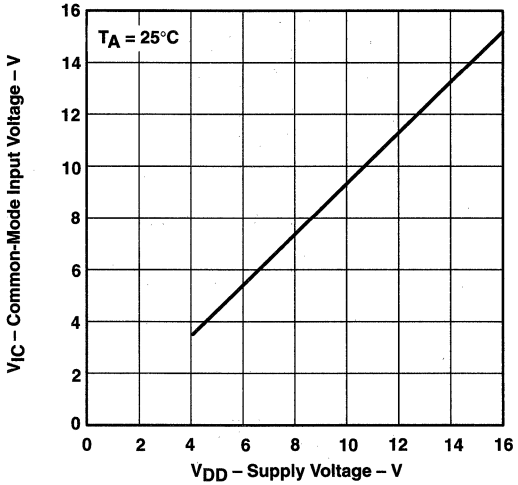


Figure 13

SUPPLY CURRENT vs SUPPLY VOLTAGE

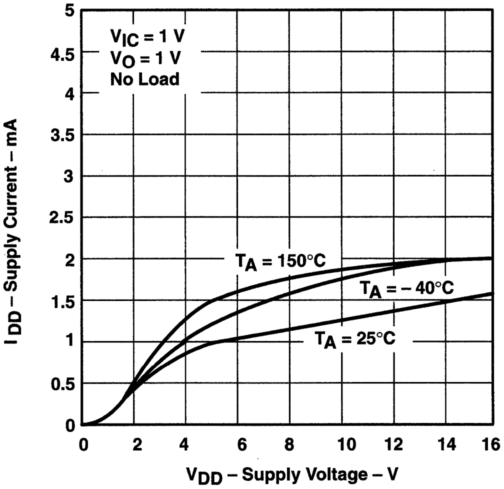


Figure 14

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

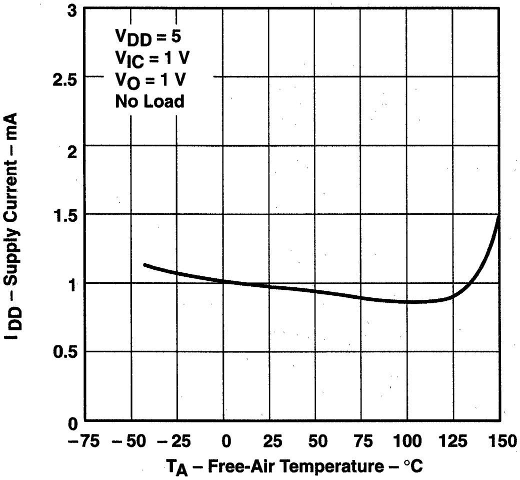


Figure 15

SLEW RATE vs SUPPLY VOLTAGE

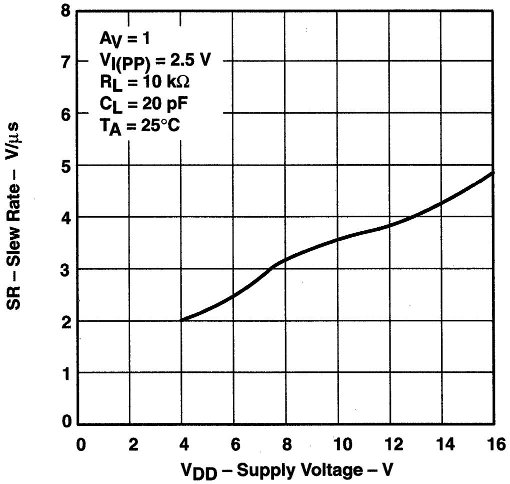


Figure 16

TYPICAL CHARACTERISTICS

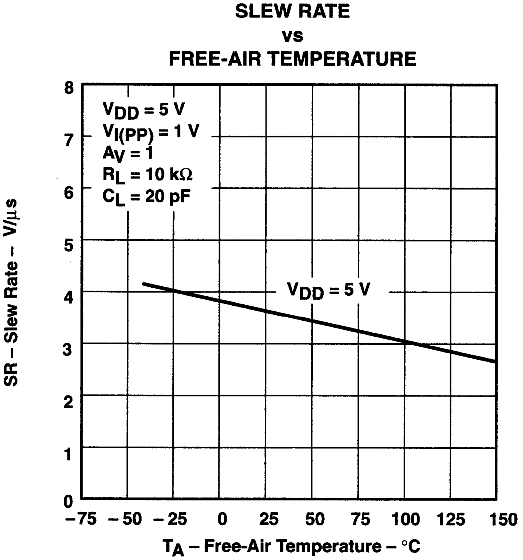


Figure 17

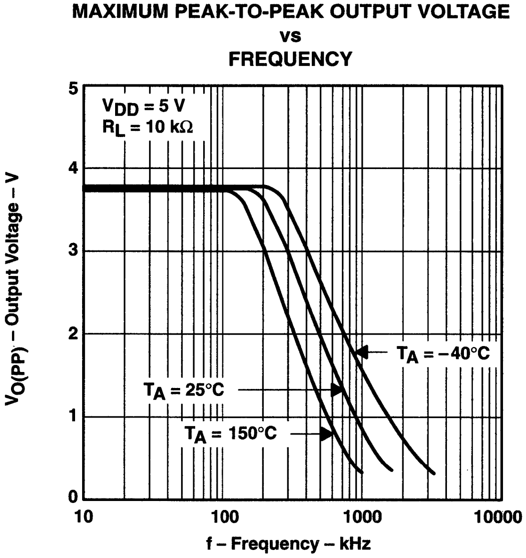


Figure 18

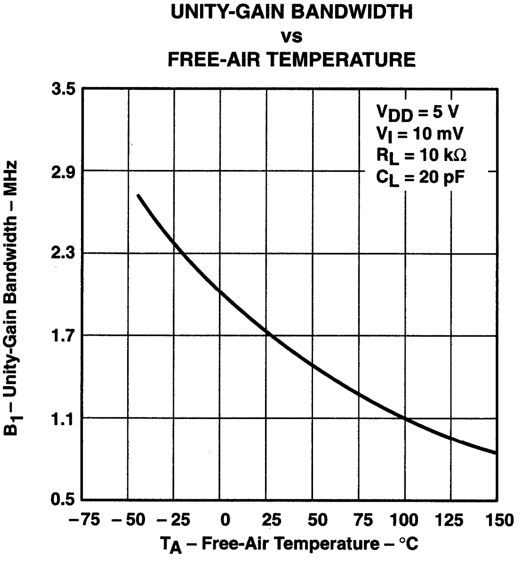


Figure 19

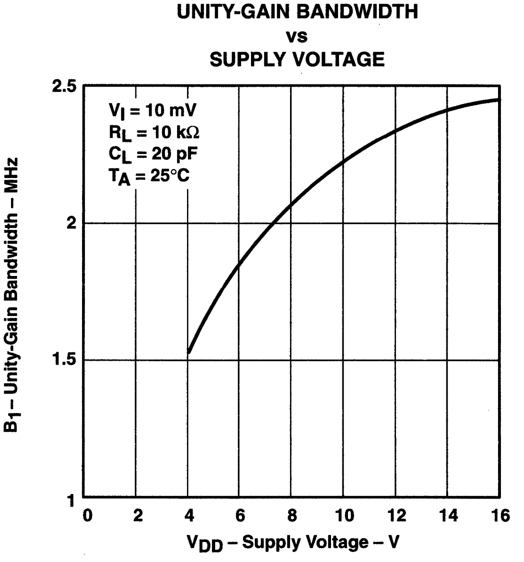


Figure 20

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

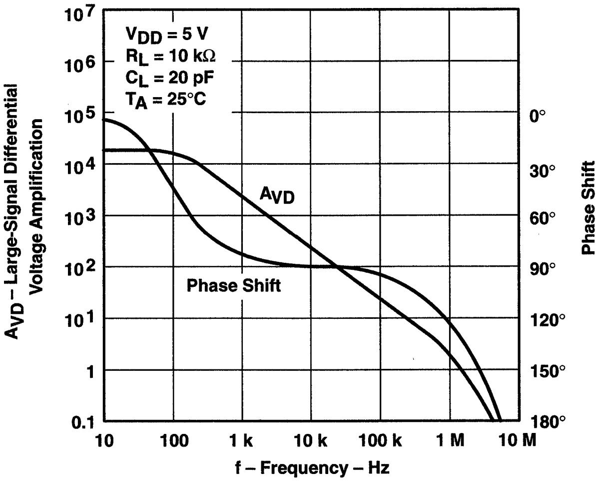


Figure 21

PHASE MARGIN vs SUPPLY VOLTAGE

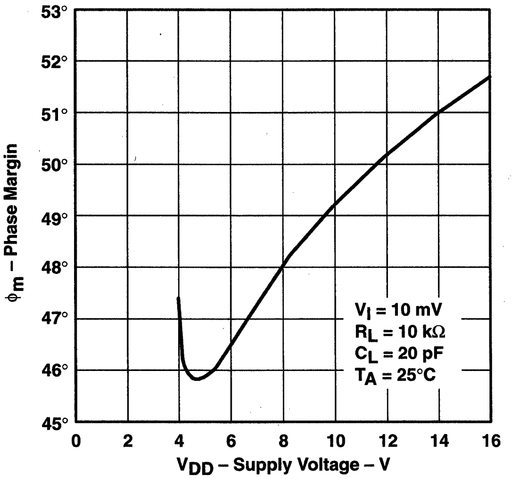


Figure 22

PHASE MARGIN vs FREE-AIR TEMPERATURE

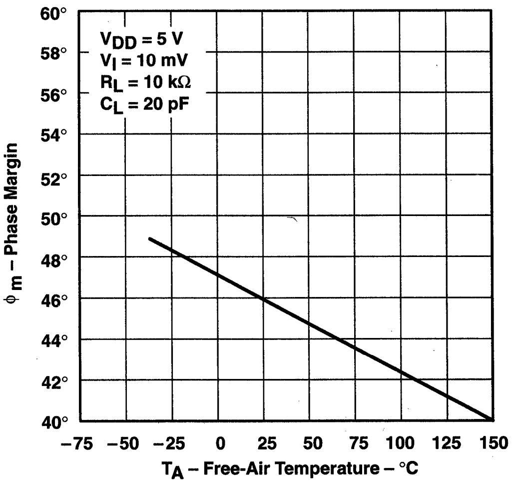


Figure 23

TYPICAL CHARACTERISTICS

PHASE MARGIN vs LOAD CAPACITANCE

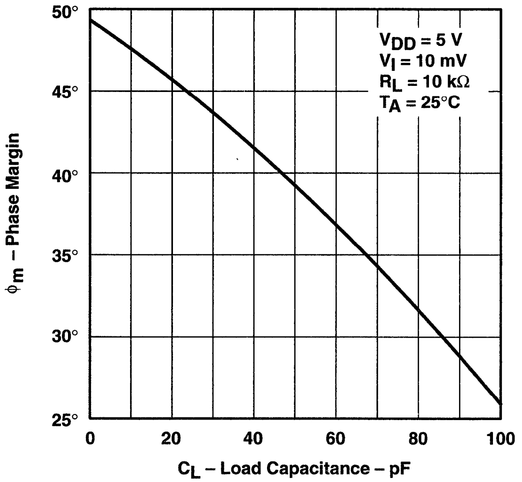


Figure 24

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

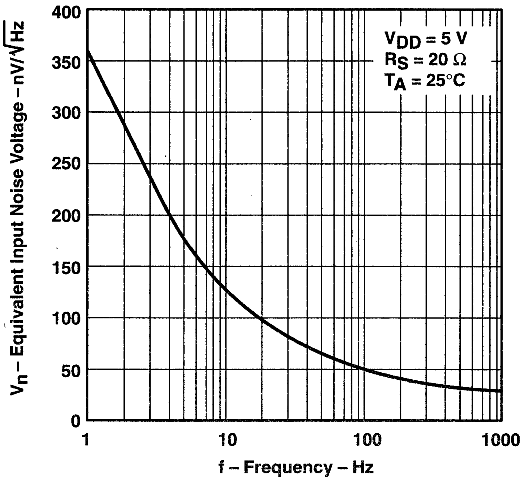
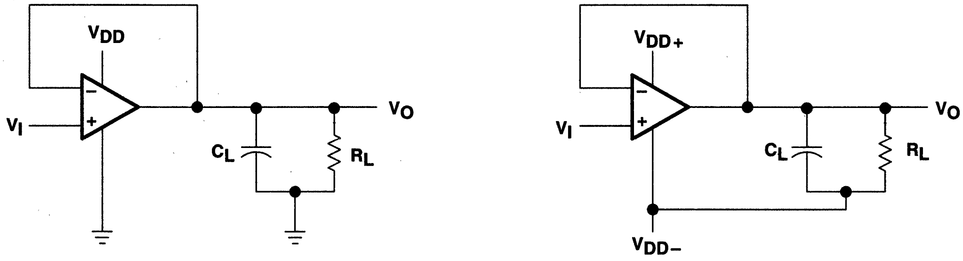


Figure 25

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

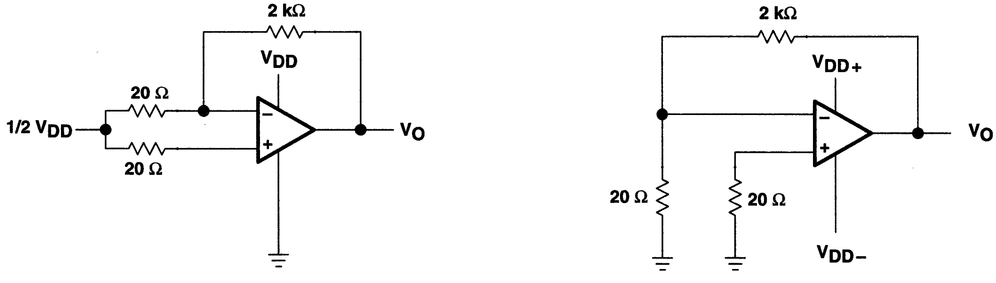
Because the TLC2810Z is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply and split-supply test circuits is shown below. The use of either circuit gives the same result.



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

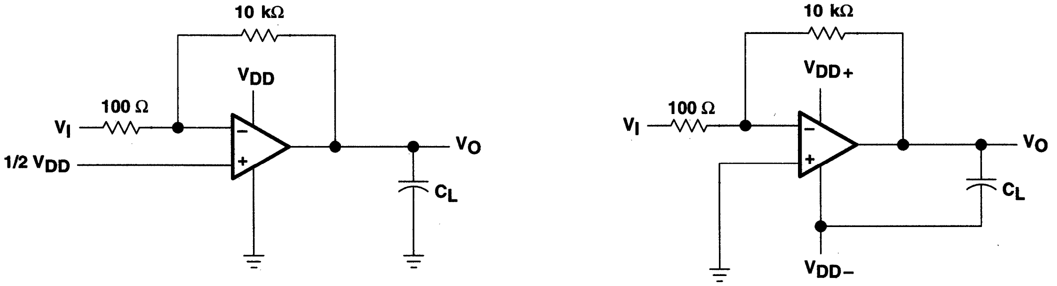
Figure 26. Unity-Gain Amplifier



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 27. Noise-Test Circuit



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 28. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC2810Z operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 29). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading: therefore, an open-socket reading is not feasible using this method.

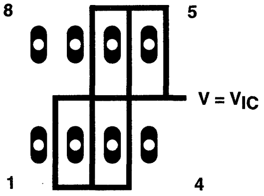


Figure 29. Isolation Metal Around Device Inputs (P package)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance that can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal

full-power response (continued)

input signal until the maximum frequency above which the output contains significant distortion is found. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 26. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 30). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

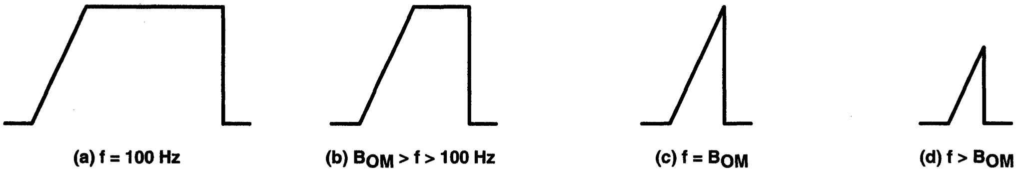

(a) f = 100 Hz (b) $B_{OM} > f > 100$ Hz (c) f = B_{OM} (d) f > B_{OM}

Figure 30. Full-Power-Response Output Signal

test time

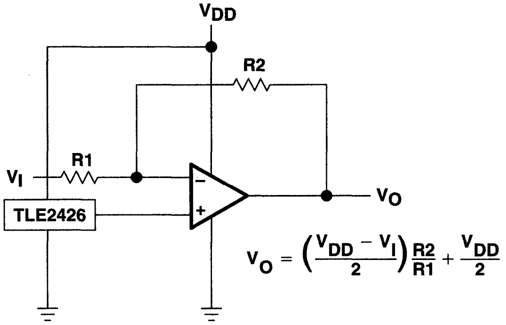
Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices; hence, CMOS devices require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced power supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLC2810Z performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 4 V, thus allowing operation with supply levels commonly available for TTL and CMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual ground generator such as the TLE2426 (see Figure 31). The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

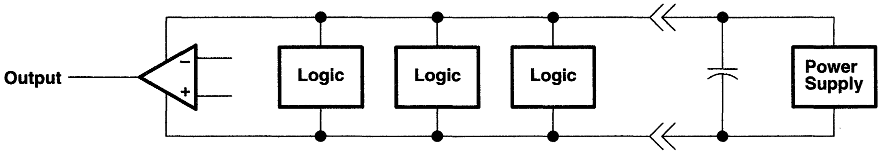


$$V_O = \left(\frac{V_{DD} - V_I}{2}\right)\frac{R2}{R1} + \frac{V_{DD}}{2}$$

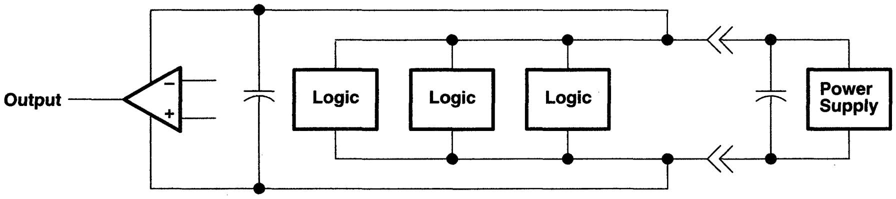
Figure 31. Inverting Amplifier With Voltage Reference

The TLC2810Z works well in conjunction with digital logic. However, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 32). Otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate. However, RC decoupling may be necessary in high-frequency applications.



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 32. Common Versus Separate Supply Rails

APPLICATION INFORMATION

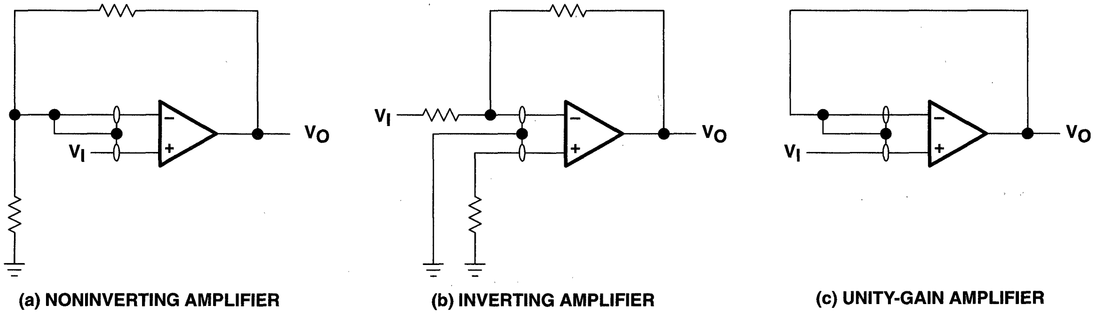
input characteristics

The TLC2810Z is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} –1 V at T_A = 25°C and at V_{DD}– 1.2 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design give the TLC2810Z very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low-bias current requirements, the TLC2810Z is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 29 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 33).

Unused amplifiers should be connected as grounded voltage followers to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 33. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC2810Z results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ since bipolar devices exhibit greater noise currents.

APPLICATION INFORMATION

feedback

Operational amplifier circuits nearly always employ feedback and, since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 34). The value of this capacitor is optimized empirically.

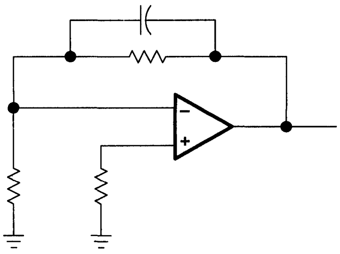


Figure 34. Compensation for Input Capacitance

electrostatic discharge protection

The TLC2810Z incorporates an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2810Z inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

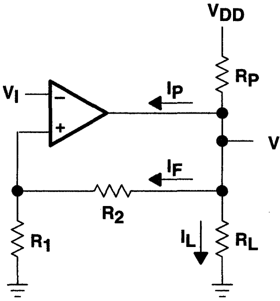
The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

APPLICATION INFORMATION

output characteristics

The output stage of the TLC2810Z is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLC2810Z possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 35). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic), must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4, and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup Current Required by the Operational Amplifier (typically 500 μA)

Figure 35. Resistive Pullup to Increase V_{OH}

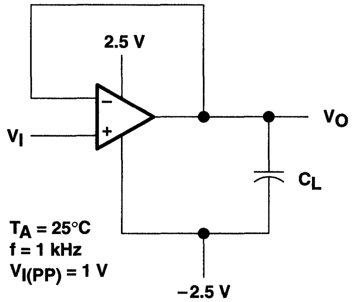
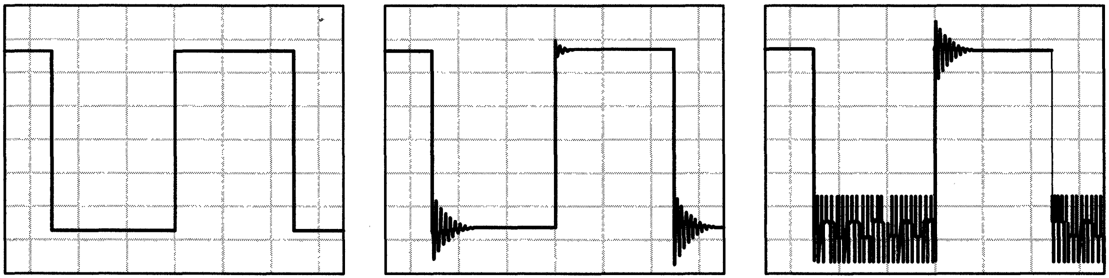


Figure 36. Test Circuit for Output Characteristics

All operating characteristics of the TLC2810Z are measured using a 20-pF load. The devices can drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 37). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

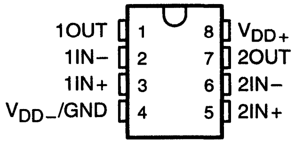
Figure 37. Effect of Capacitive Loads

TLC2872Z, TLC2872Y
Advanced LinCMOS™ RAIL-TO-RAIL DUAL OPERATIONAL AMPLIFIERS

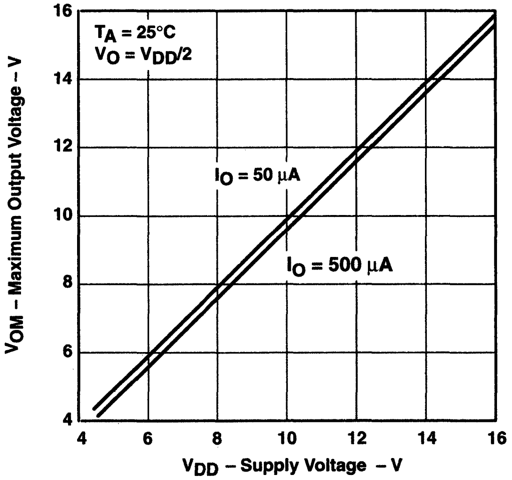
SLOS117 – OCTOBER 1992

- **Free-Air Operating Temperature −40°C to 150°C**
- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 9 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **High Unity-Gain Bandwidth . . . 2.2 MHz Typ**
- **High Slew Rate . . . 3.6 V/μs Typ**
- **Low Input Offset Voltage 300 μV Typ at T_A = 25°C**
- **Macromodel Included**

D OR P PACKAGE
(TOP VIEW)



MAXIMUM OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE



description

The TLC2872Z is a dual rail-to-rail output operational amplifier manufactured using Texas Instruments Advanced LinCMOS™ process. These devices offer comparable ac performance while having better noise, input offset voltage and power dissipation than existing CMOS operational amplifiers. In addition, the common-mode input voltage range is wider than typical standard CMOS type amplifiers. To take advantage of this improvement in performance, making this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ±5 mV. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. Also, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The TLC2872Z, manufactured using Texas Instruments high-temperature process flow, allows extended temperature operation up to 150°C in a plastic package. This adds extra reliability at the extended temperature and reduces the need for expensive hermetically sealed ceramic packages.

The TLC2872Z, which exhibits high input impedance and low noise, is excellent for small signal conditioning of high impedance sources, such as piezoelectric transducers. In addition, the rail-to-rail output feature with single or split supplies makes this device a great choice for inputs to ADCs in either the unipolar or bipolar mode of operation. This feature, combined with its temperature performance, makes the TLC2872Z ideal for sonobuoys, pressure sensors, temperature controls, active VR sensors, accelerometers, and many other applications.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
−40°C to 150°C	2.5 mV	TLC2872ZD	TLC2872ZP	TLC2872Y

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2872DR).

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

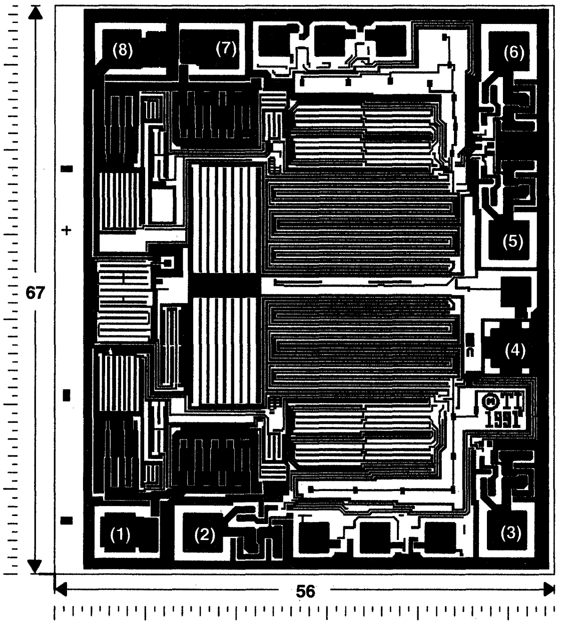
description (continued)

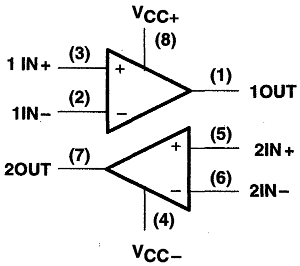
The inputs and outputs of this device are designed to withstand 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V. The device is characterized for operation over the extended (Z) temperature range of −40°C to 150°C.

TLC2872Y chip information

This chip, when properly assembled, displays characteristics similar to TLC2872Z. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

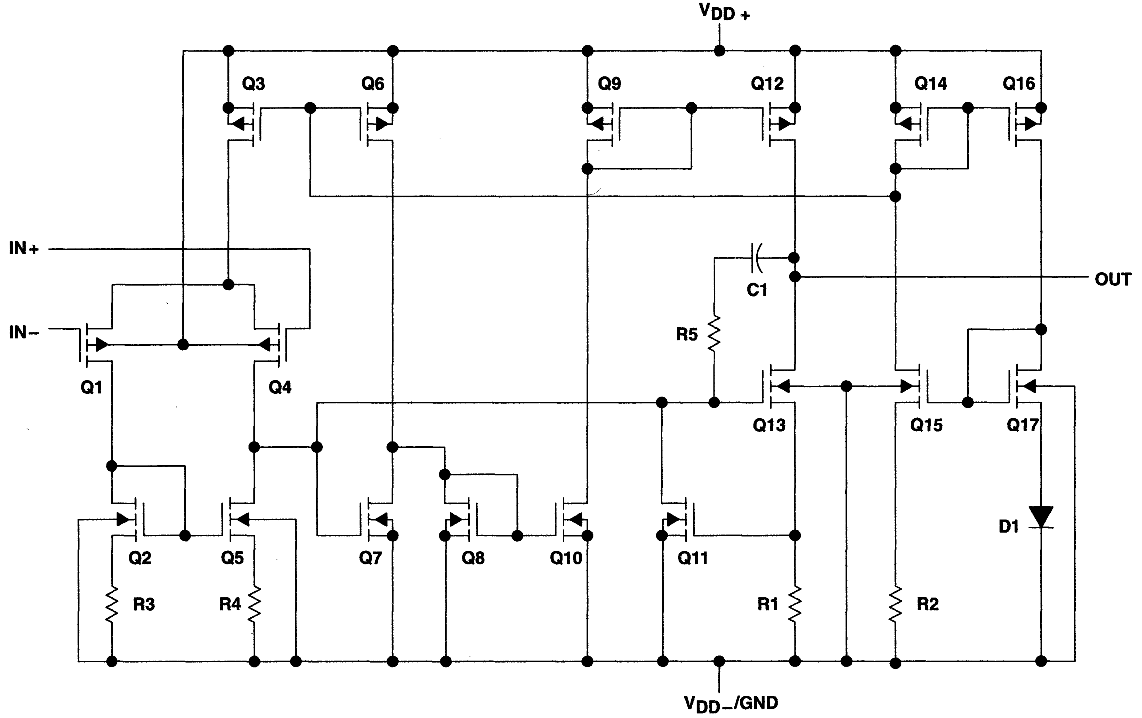
T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT	COUNT†
Transistors	38
Diodes	9
Resistors	26
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+}	8 V
Supply voltage, V_{DD-}	−8 V
Differential input voltage, V_{ID} (see Note 1)	±16 V
Input voltage range, V_I (any input, see Note 2)	±8 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−40°C to 150°C
Storage temperature range	−65°C to 165°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. Differential voltages are at IN+ with respect to IN−. Excessive current will flow if input is brought below V_{DD-} − 0.3 V.
2. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING	$T_A = 150°C$ POWER RATING
D	812 mW	5.8 mW/°C	551 mW	348 mW	232 mW	87 mW
P	1120 mW	8 mW/°C	760 mW	480 mW	320 mW	120 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	−40	150	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2872Z			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500	µV
			Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 150°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002		µV/mo
I_{IO}	Input offset current		25°C		0.0005		nA
			Full range			3	
I_{IB}	Input bias current		25°C		0.001		nA
			Full range			5	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20\ \mu A$	25°C	4.95	4.99		V
		$I_{OH} = -200\ \mu A$	25°C	4.85	4.93		
			Full range	4.75			
		$I_{OH} = -1$ mA	25°C	4.25	4.65		
			Full range	4.25			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V, $I_{OL} = 50\ \mu A$	25°C		0.01	0.02	V
		$V_{IC} = 2.5$ V, $I_{OL} = 500\ \mu A$	25°C		0.09	0.15	
			Full range			0.2	
		$V_{IC} = 2.5$ V, $I_{OL} = 5$ mA	25°C		0.9	1.5	
			Full range			2	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 10\ k\Omega$‡	25°C	15	35		V/mV
			Full range	10			
		$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 1\ M\Omega$‡	25°C		175		
r_{id}	Differential input resistance		25°C		10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 1 MHz, $A_V = 10$	25°C		140		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 50\ \Omega$	25°C	70	75		dB
			Full range	70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		dB
			Full range	80			
I_{DD}	Supply current	$V_O = 2.5$ V, No load	25°C		2.2	3	mA
			Full range			3	

† Full range is −40°C to 150°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2872Z			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C	2.3	3.6		V/µs
				Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50		nV/√Hz
		f = 1 kHz		25°C		9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1		µV
		f = 0.1 to 10 Hz		25°C		1.4		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%		
			A_V = 10			0.004%		
			A_V = 100			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C		2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		1		MHz
	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5		µs
			To 0.01%			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		50°		
	Gain margin			25°C		10		dB

† Full range is −40°C to 150°C.
‡ Referenced to 2.5 V

electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2872Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,		300	2500	µV
	Input offset voltage long-term drift (see Note 4)				0.002		µV/mo
I_{IO}	Input offset current				0.0005		nA
I_{IB}	Input bias current				0.001		nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\| \le 5$ mV	0 to 4	−0.3 to 4.2		V
				0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		4.95	4.99		V
		I_{OH} = −200 µA		4.85	4.93		
		I_{OH} = −1 mA		4.25	4.65		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA		0.01	0.02	V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA		0.9	1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ†	15	35		V/mV
			R_L = 1 MΩ†		175		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package		8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10		140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	70	75		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, No load	$V_{IC} = V_{DD}/2$,	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		2.2	3	mA

† Referenced to 2.5 V

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC2872Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ†, C_L = 100 pF†		2.3	3.6		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			50		nV/√Hz
		f = 1 kHz			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			1		µV
		f = 0.1 to 10 Hz			1.4		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ†	A_V = 1		0.0013%		
			A_V = 10		0.004%		
			A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ†, C_L = 100 pF†			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ†, C_L = 100 pF†			1		MHz
	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ†, C_L = 100 pF†	To 0.1%		1.5		µs
			To 0.01%		2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ†, C_L = 100 pF†			50°		
	Gain margin				10		dB

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1
α_{VIO}	Input offset voltage temperature coefficient	Distribution	2
I_{IB}/I_{IO}	Input bias and offset currents	vs Free-air temperature	3
V_I	Input voltage range	vs Free-air temperature	4
V_{OH}	High-level output voltage	vs Output current	5
V_{OL}	Low-level output voltage	vs Output current	6, 7
V_{OM}	Maximum output voltage	vs Frequency	8
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	9 10
A_{VD}	Large-signal differential voltage amplification	vs Load resistance vs Frequency vs Free-air temperature	11 12 13
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	14 15
SR	Slew rate	vs Load capacitance vs Free-air temperature	16 17
ϕ_m	Phase margin	vs Frequency vs Load capacitance	12 18
	Gain margin	vs Load capacitance	19

NOTE: All loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2872Z INPUT OFFSET VOLTAGE

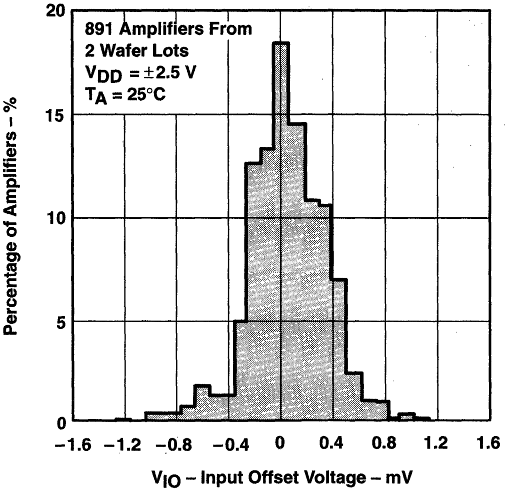


Figure 1

DISTRIBUTION OF TLC2872Z TEMPERATURE COEFFICIENT

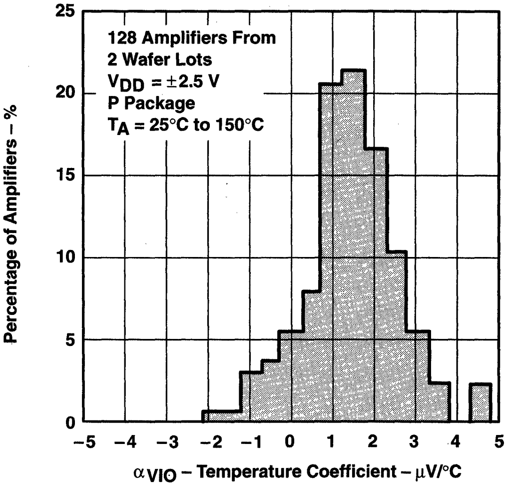


Figure 2

INPUT BIAS AND OFFSET CURRENTS vs FREE-AIR TEMPERATURE

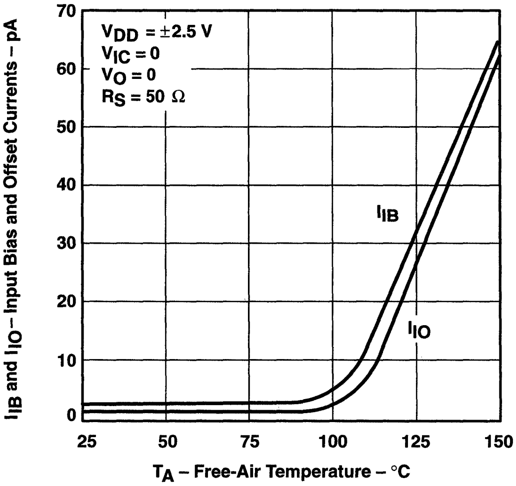


Figure 3

INPUT VOLTAGE RANGE vs FREE-AIR TEMPERATURE

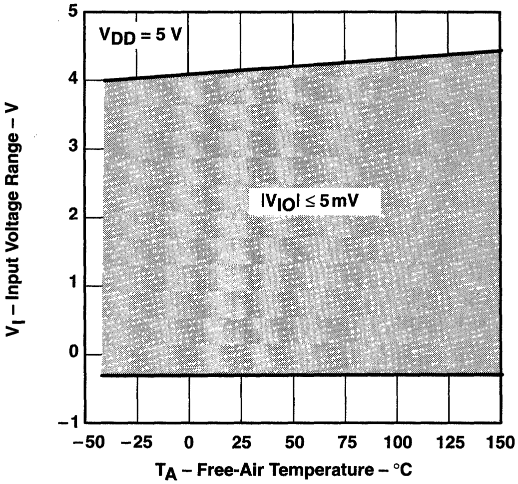


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

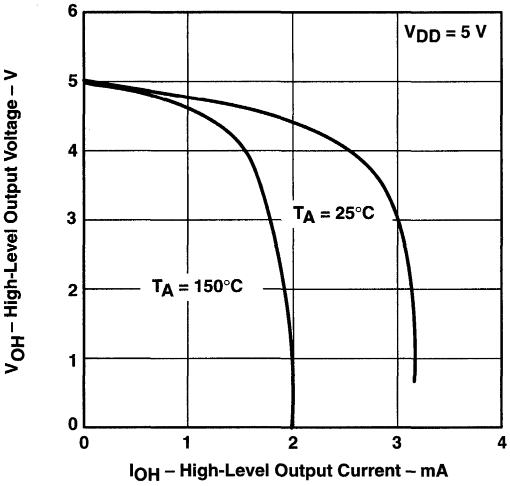


Figure 5

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

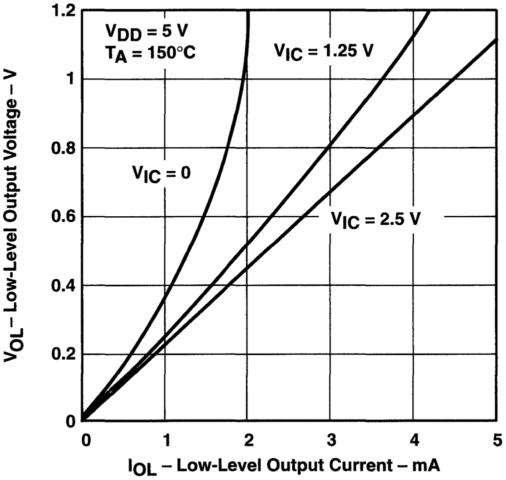


Figure 6

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

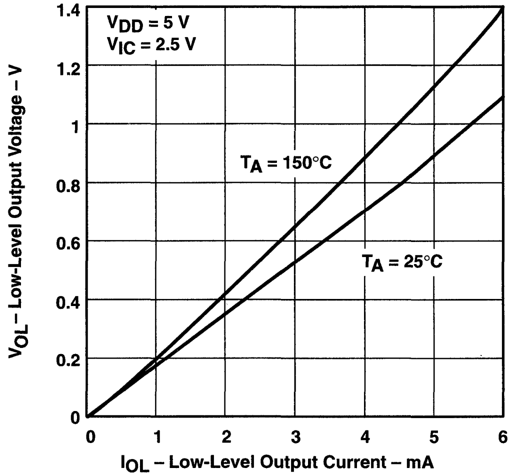


Figure 7

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

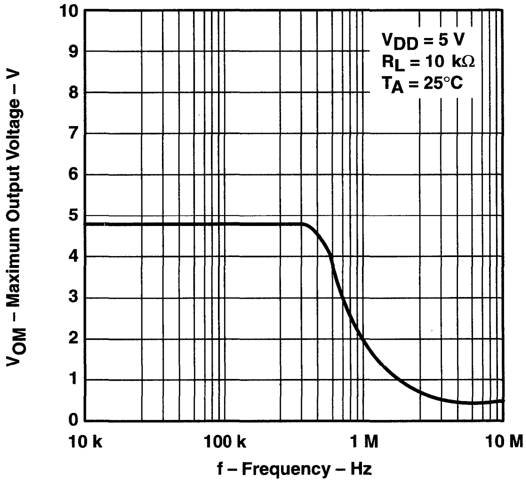


Figure 8

TYPICAL CHARACTERISTICS

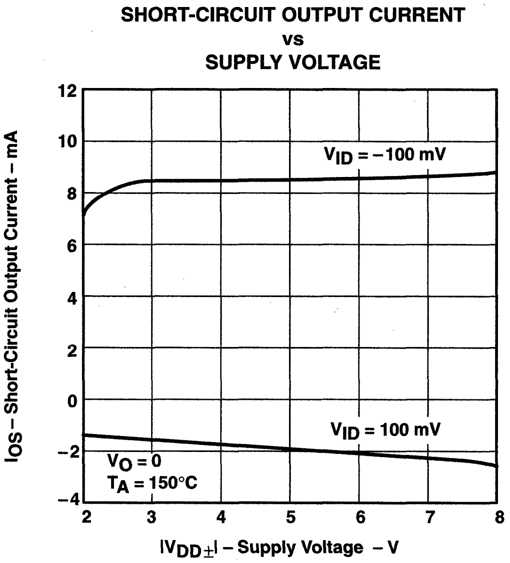


Figure 9

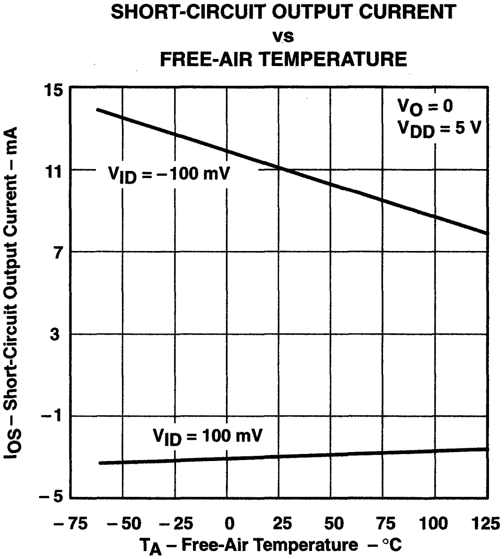


Figure 10

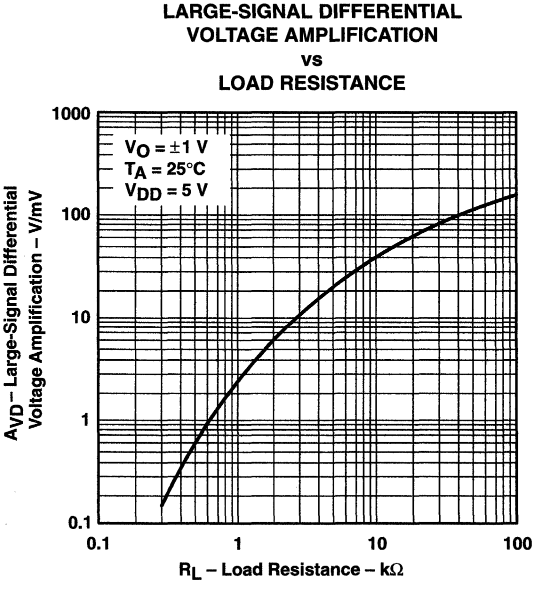


Figure 11

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE MARGIN vs FREQUENCY

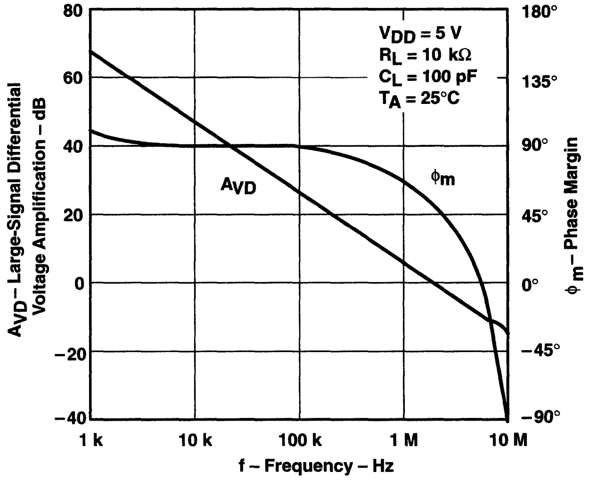


Figure 12

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

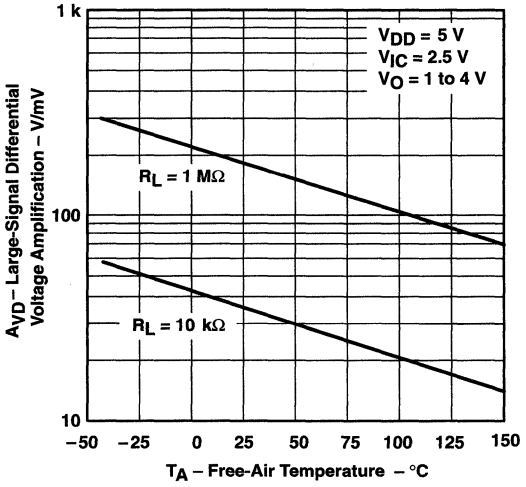


Figure 13

SUPPLY CURRENT vs SUPPLY VOLTAGE

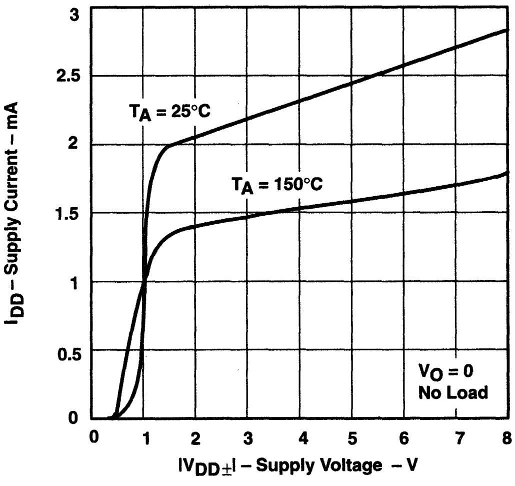


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

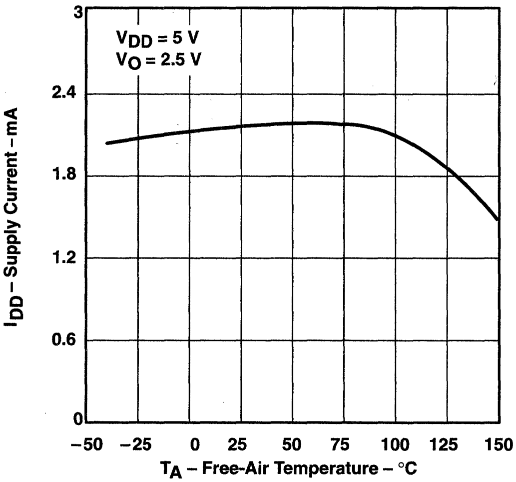


Figure 15

SLEW RATE
vs
LOAD CAPACITANCE

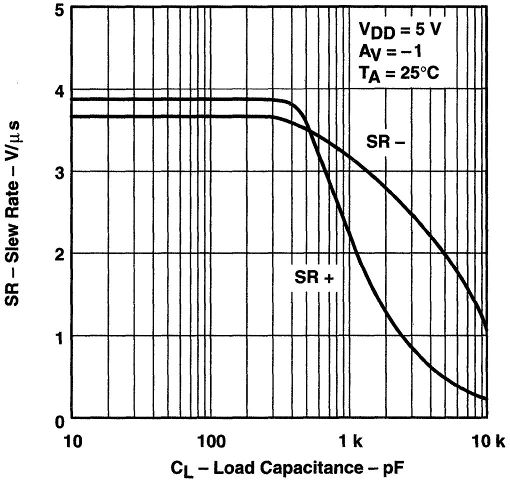


Figure 16

SLEW RATE
vs
FREE-AIR TEMPERATURE

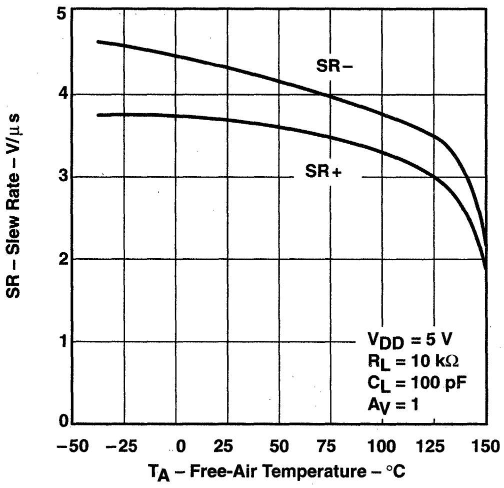


Figure 17

PHASE MARGIN
vs
LOAD CAPACITANCE

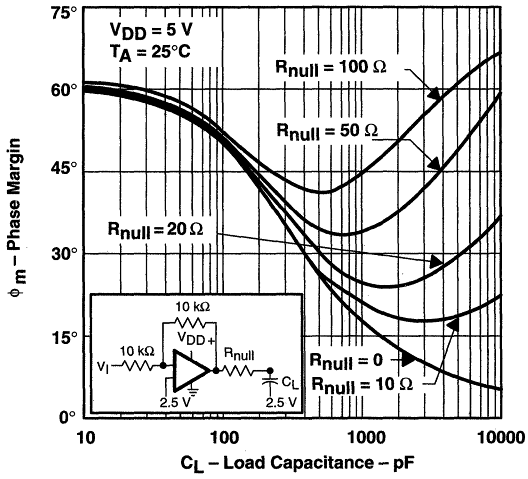


Figure 18

TYPICAL CHARACTERISTICS†

GAIN MARGIN vs LOAD CAPACITANCE

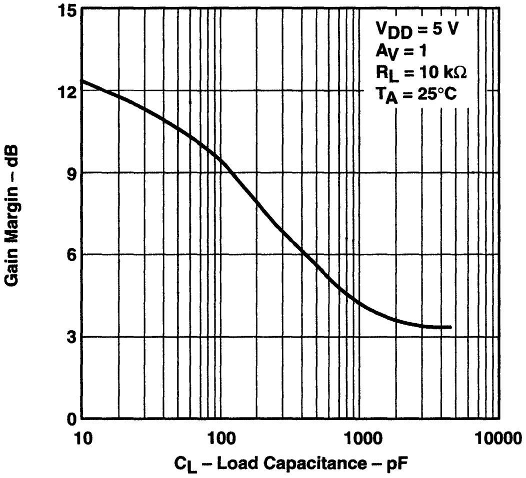


Figure 19

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

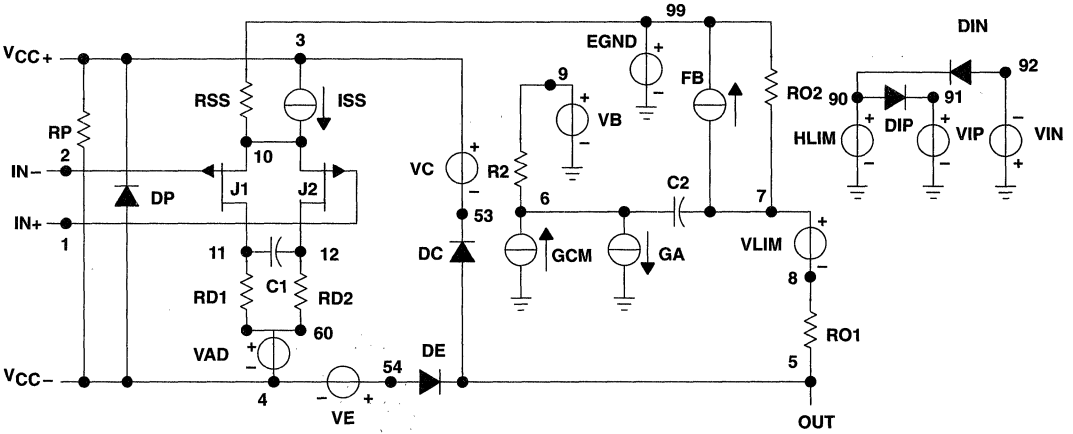
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 20 were generated using the TLC2872Z typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



```
.SUBCKT TLC2872 1 2 3 4 5
   C1    11   12   14E–12
   C2    6    7    60.00E–12
   DC    5    53   DX
   DE    54   5    DX
   DLP   90   91   DX
   DLN   92   90   DX
   DP    4    3    DX
   EGND99    0    POLY (2) (3,0) (4,0) 0 .5 .5
   FB 7  99   POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 –1E6 1E6 1E6 –1E6
   GA    6    0    11 12 377.0E–6
   GCM 0 6 10 99 134E–9
   ISS   3    10   DC 216.OE–6
   HLIM  90   0    VLIM 1K
   J1    11   2    10 JX
   J2    12   1    10 JX
   R2    6    9    100.OE3
```

```
   RD1  60   11   2.653E3
   RD2  60   12   2.653E3
   R01  8    5    50
   R02  7    99   50
   RP   3    4    4.310E3
   RSS  10   99   925.9E3
   VAD  60   4    -.5
   VB   9    0    DC 0
   VC 3  53  DC  .78
   VE   54   4    DC .78
   VLIM 7    8    DC 0
   VLP  91   0    DC 1.9
   VLN  0    92   DC 9.4
.MODEL DX D(IS=800.0E-18)
.MODELJXPJF(IS=1.500E-12BETA=1.316E3
+ VTO=-.270)
.ENDS
```

Figure 20. Boyle Macromodel and Subcircuit

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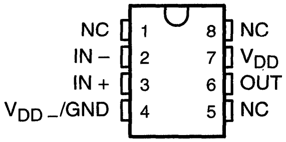
TLC4501, TLC4501A, TLC4501Y
Advanced LinEPIC™ SELF-CALIBRATING (Self-Cal™) PRECISION OPERATIONAL AMPLIFIERS

SLOS188 – JANRUARY 1997

- **Power-On Calibration of Input Offset Voltage**
- **Low Input Offset Voltage . . . < 40 μV Max (TLC4501A)**
- **Low Input Offset Voltage Drift . . . < 1 μV/°C**
- **Low Input Bias Current**
- **High Output Drive Capability $C_L < 1$ nF and $R_L > 1$ kΩ**
- **High Open Loop Gain . . . > 120 dB**
- **Rail-To-Rail Output Voltage Swing**
- **Low Distortion . . . < 0.01% at 10 kHz**
- **Low Noise . . . 12 nV/√Hz at 1 kHz**
- **High Slew Rate . . . 2.5 V/μs**
- **Low Power Consumption . . . < 1.5 mA (Typical)**
- **Short Calibration Time . . . 300 ms Typ**

D PACKAGE
(TOP VIEW)



description

The TLC4501 self-calibrating operational amplifier utilizes the recent availability of on-chip digital and analog signal processing to automatically null the input offset voltage at powerup. This *self-calibrating* feature requires typically 300 ms to complete and is repeatable to within ±3 μV on successive calibrations. The technique involves the extraction and digital storage of the key offset-nulling information. This information is retained without degradation as long as the circuit is powered. This eliminates the need for continuous chopping of the input signal to refresh the offset information. Once the process is complete, the bulk of the calibration circuitry drops out of the signal path and shuts down. This minimizes or eliminates any effect the calibration circuitry might have on the desired signal path. It also allows the TLC4501 to be used exactly like any other operational amplifier after the calibration cycle is complete.

The TLC4501 is a high-performance operational amplifier fabricated in a 1-μm 5-V digital CMOS technology. It achieves very high dc gain, as well as excellent power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR). It uses a mixed-mode (analog/digital) internal compensation loop with digital storage of the offset information and a current-mode output to reduce its input offset to < 40 μV. The TLC4501 also features a rail-to-rail output structure capable of driving loads to 1 kΩ and 1 nF. Unlike existing commercially available low-offset high-precision amplifiers, the TLC4501 needs only a single 5-V supply, requires no trimming, and uses no bipolar transistors or JFETs.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICE† SMALL OUTLINE (D)	CHIP FORM (Y)
0°C to 70°C	40 μV	TLC4501ACDR	TLC4501Y
	80 μV	TLC4501CDR	
–40°C to 85°C	40 μV	TLC4501AIDR	
	80 μV	TLC4501IDR	

† The D package is also available taped and reeled.

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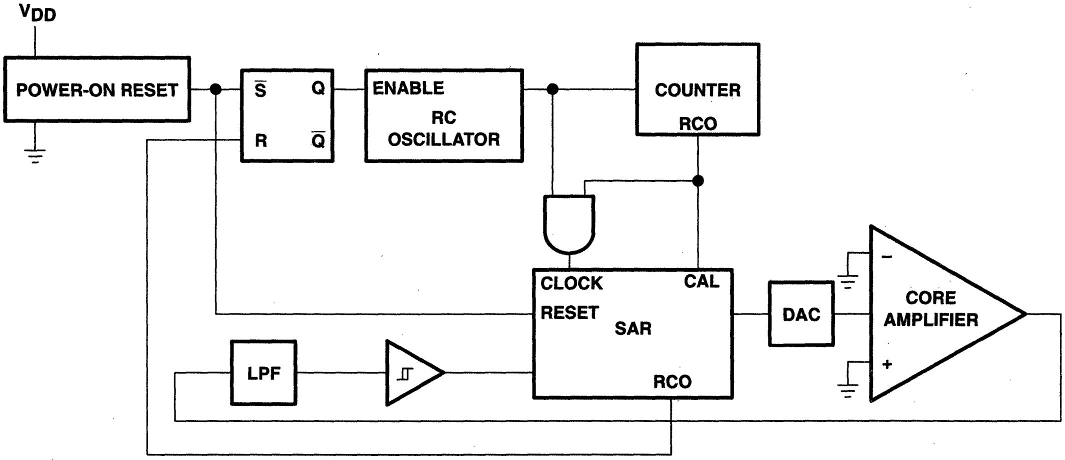
TEXAS INSTRUMENTS

description (continued)

To achieve high dc gain, large bandwidth, high CMRR and PSRR, as well as good output drive capability, the TLC4501 is built around a 3-stage topology: two gain stages, one rail-to-rail, and a class-AB output stage. A nested Miller topology is used for frequency compensation.

functional block diagram (during calibration)



During the calibration procedure, the operational amplifier is removed from the signal path and both inputs are tied to GND.

The class AB output stage features rail-to-rail voltage swing and incorporates additional switches to put the output node into a high-impedance mode during the calibration cycle. Small-replica output transistors (matched to the main output transistors) provide the amplifier output signal for the calibration circuit. The TLC4501 also features built-in output short-circuit protection. The output current flowing through the main output transistors is continuously being sensed. If the current through either of these transistors exceeds the preset limit (60 mA – 70 mA) for more than about 1 µs, the output transistors are shut down to essentially their quiescent operating point for approximately 5 ms. The device is then returned to normal operation. If the short circuit is still in place, it is detected in less than 1 µs and the device is shutdown for another 5 ms.

The offset cancellation uses a current-mode digital-to-analog converter (DAC), whose full-scale current allows for an adjustment of approximately ±5 mV to the input offset voltage. The digital code producing the cancellation current is stored in the successive-approximation register (SAR).

During power up, when the offset cancellation procedure is initiated, an on-chip RC oscillator is activated to provide the timing of the successive-approximation algorithm. To prevent wide-band noise from interfering with the calibration procedure, an analog low-pass filter followed by a Schmidt trigger is used in the decision chain to implement an averaging process. Once the calibration procedure is complete, the RC oscillator is deactivated to reduce supply current and the associated noise.

The key operational-amplifier parameters CMRR, PSRR, and offset drift were optimized to achieve superior offset performance. The TLC4501 calibration DAC is implemented by a binary-weighted current array using a pseudo-R-2R MOSFET ladder architecture, which minimizes the silicon area required for the calibration circuitry, and thereby reduces the cost of the TLC4501.

description (continued)

Due to the performance (precision, PSRR, CMRR, gain, output drive, and ac performance) of the TLC4501, it is ideal for applications like:

- Data acquisition systems
- Medical equipment
- Portable digital scales
- Strain gauges
- Automotive sensors
- Digital audio circuits
- Industrial control applications

It is also ideal in circuits like:

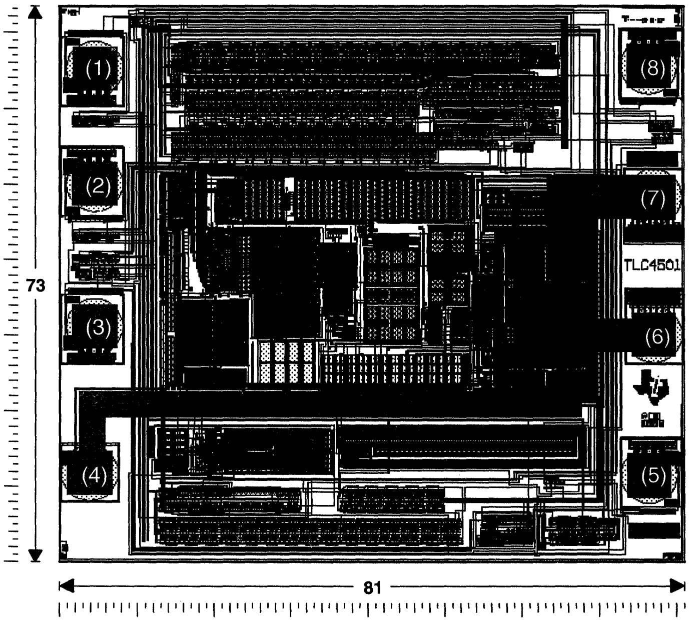
- A precision buffer for current-to-voltage converters, a/d buffers, or bridge applications
- High-impedance buffers or preamplifiers
- Long term integration
- Sample-and-hold circuits
- Peak detectors

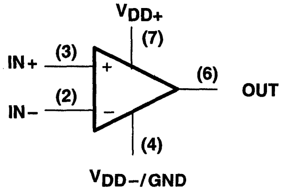
The TLC4501 self-calibrating operational amplifier is manufactured using Texas instruments LinEPIC process technology and is available in an 8-pin SOIC (D) Package. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C.

TLC4501Y chip information

This chip, when properly assembled, display characteristics similar to the TLC4501C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	7 V
Differential input voltage, V_{ID} (see Note 2)	±7 V
Input voltage range, V_I (any input, see Note 1)	−0.3 V to 7 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±100 mA
Total current into V_{DD+}	±100 mA
Total current out of V_{DD-}/GND	±100 mA
Electrostatic discharge (ESD)	> 2 kV
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC4501C	0°C to 70°C
TLC4501I	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 60 seconds, T_C: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows when an input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions

	TLC4501C		TLC4501I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	4	6	4	6	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Operating free-air temperature, T_A	0	70	−40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, GND = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC4501C			TLC4501AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±2.5 V, V_O = 0, V_{IC} = 0, R_S = 50 Ω	25°C	–80		80	–40		40	µV
			Full range	–80		80	–40		40	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1			1		µV/°C
I_{IO}	Input offset current		25°C		1			1		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{OH}	High-level output voltage	I_{OH} = – 500 µA	25°C		4.99			4.99		V
		I_{OH} = – 5 mA	25°C		4.9			4.9		
			Full range	4.7			4.7			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.1			0.1		
			Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 kΩ, See Note 4	25°C	200	1000		200	1000		V/mV
			Full range	200			200			
$R_{I(D)}$	Differential input resistance		25°C		10			10		kΩ
R_L	Input resistance	See Note 4	25°C		10^{12}			10^{12}		Ω
C_L	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_O	Closed-loop output impedance	A_V = 10, f = 100 kHz	25°C		1			1		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 1 kΩ	25°C	90	100		90	100		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} \pm / \Delta V_{IO}$)	V_{DD} = 4 V to 6 V, V_{IC} = 0, No load	25°C	90	100		90	100		dB
			Full range	90			90			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			2			2	
$V_{IT(CAL)}$	Calibration input threshold voltage		Full range	4			4			V

† Full range is 0°C to 70°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, GND = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC4501I			TLC4501AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±2.5 V, V_O = 0, V_{IC} = 0, R_S = 50 Ω	25°C	–80		80	–40		40	µV
			Full range	–80		80	–40		40	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1			1		µV/°C
I_{IO}	Input offset current		25°C		1			1		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{OH}	High-level output voltage	I_{OH} = – 500 µA	25°C		4.99			4.99		V
		I_{OH} = – 5 mA	25°C		4.9			4.9		
			Full range	4.7			4.7			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.1			0.1		
			Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 kΩ, See Note 4	25°C	200	1000		200	1000		V/mV
			Full range	200			200			
$R_{I(D)}$	Differential input resistance		25°C		10			10		kΩ
R_L	Input resistance	See Note 4	25°C		10^{12}			10^{12}		Ω
C_L	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_O	Closed-loop output impedance	A_V = 10, f = 100 kHz	25°C		1			1		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 1 kΩ	25°C	90	100		90	100		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} \pm / \Delta V_{IO}$)	V_{DD} = 4 V to 6 V, V_{IC} = 0, No load	25°C	90	100		90	100		dB
			Full range	90			90			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			2			2	
$V_{IT(CAL)}$	Calibration input threshold voltage		Full range	4			4			V

† Full range is –40°C to 85°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC4501C, TLC4501AC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V,	C_L = 100 pF	25°C	1.5	2.5		V/µs
				Full range	1			V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		70		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1		µV
		f = 0.1 to 10 Hz		25°C		1.5		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 1 kΩ, C_L = 100 pF	A_V = 1	25°C		0.02%		
			A_V = 10	25°C		0.08%		
			A_V = 100	25°C		0.55%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 1 kΩ,	25°C		4.7		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 1 kΩ,	A_V = 1, C_L = 100 pF	25°C		1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 1 kΩ, C_L = 100 pF	to 0.1%	25°C		1.6		µs
			to 0.01%	25°C		2.2		
ϕ_m	Phase margin at unity gain	R_L = 1 kΩ,	C_L = 100 pF	25°C		74		
	Calibration time			25°C		300		ms

† Full range is 0°C to 70°C.
NOTE 4: R_L and C_L values are referenced to 2.5 V.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC4501I, TLC4501AI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V,	C_L = 100 pF	25°C	1.5	2.5		V/μs
				Full range	1			V/μs
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		70		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1		μV
		f = 0.1 to 10 Hz		25°C		1.5		
I_n	Equivalent input noise current			25°C		0.6		$\mathrm{fA}/\sqrt{\mathrm{Hz}}$
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 1 kΩ, C_L = 100 pF	A_V = 1	25°C		0.02%		
			A_V = 10	25°C		0.08%		
			A_V = 100	25°C		0.55%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 1 kΩ,	25°C		4.7		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 1 kΩ,	A_V = 1, C_L = 100 pF	25°C		1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 1 kΩ, C_L = 100 pF	to 0.1%	25°C		1.6		μs
			to 0.01%	25°C		2.2		
ϕ_m	Phase margin at unity gain	R_L = 1 kΩ,	C_L = 100 pF	25°C		74		
	Calibration time			25°C		300		ms

† Full range is −40°C to 85°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, GND = 0, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC4501Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±2.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω		10		μV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				1		pA
V_{OH}	High-level output voltage	I_{OH} = – 500 μA			4.99		V
		I_{OH} = – 5 mA			4.9		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 5 mA		0.1		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, R_L = 1 kΩ,	V_O = 1 V to 4 V, See Note 4		1000		V/mV
$R_{I(D)}$	Differential input resistance				10		kΩ
R_L	Input resistance	See Note 4			10^{12}		Ω
C_L	Common-mode input capacitance	f = 10 kHz,	P package		8		pF
z_O	Closed-loop output impedance	A_V = 10,	f = 100 kHz		1		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 1 kΩ	V_O = 2.5 V,		100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\,\pm}/\Delta V_{IO}$)	V_{DD} = ±2 V to ±3 V, No load	V_{IC} = 0,		100		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		1		mA

NOTE 4: R_L and C_L values are referenced to 2.5 V.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC4501Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V,	C_L = 100 pF		2.5		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz			70		nV/√Hz
		f = 1 kHz			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			1		μV
		f = 0.1 to 10 Hz			1.5		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 1 kΩ, C_L = 100 pF	A_V = 1		0.02%		
			A_V = 10		0.08%		
			A_V = 100		0.55%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 1 kΩ,		4.7		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 1 kΩ,	A_V = 1, C_L = 100 pF		1		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 1 kΩ, C_L = 100 pF	to 0.1%		1.6		μs
			to 0.01%		2.2		
ϕ_m	Phase margin at unity gain	R_L = 1 kΩ,	C_L = 100 pF		74		
	Calibration time				300		ms

NOTE 4: R_L and C_L values are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2, 3
		vs Common-mode input voltage	4
α^{VIO}	Input offset voltage temperature coefficient	Distribution	5, 6
V_{OH}	High-level output voltage	vs High-level output current	7
V_{OL}	Low-level output voltage	vs Low-level output current	8
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	9
I_{OS}	Short-circuit output current	vs Free-air temperature	10
V_O	Output voltage	vs Differential input voltage	11
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	12 13
z_o	Output impedance	vs Frequency	14
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	15 16
SR	Slew rate	vs Load capacitance vs Free-air temperature	17 18
	Inverting large-signal pulse response	vs Time	19
	Voltage-follower large-signal pulse response	vs Time	20
	Inverting small-signal pulse response	vs Time	21
	Voltage-follower small-signal pulse response	vs Time	22
V_n	Equivalent input noise voltage	vs Frequency	23
	Input noise voltage	Over a 10-second period	24
THD + N	Total harmonic distortion plus noise	vs Frequency	25
	Gain-bandwidth product	vs Free-air temperature	26
ϕ_m	Phase margin	vs Load capacitance	27, 28
		vs Frequency	13
PSRR	Power-supply rejection ratio	vs Free-air temperature	29
	Calibration time at −40°C	vs Time	30
	Calibration time at 25°C	vs Time	31
	Calibration time at 85°C	vs Time	32

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC4501 INPUT OFFSET VOLTAGE

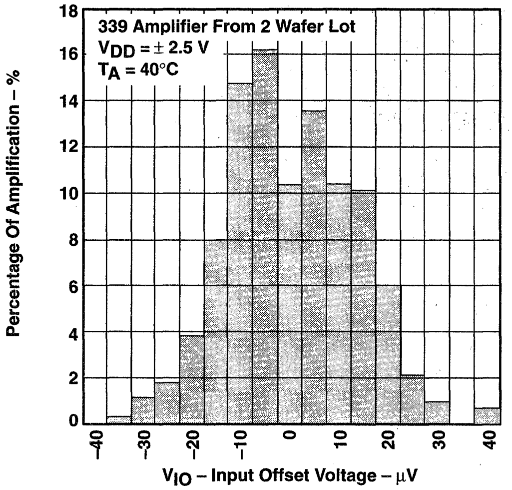


Figure 1

DISTRIBUTION OF TLC4501 INPUT OFFSET VOLTAGE

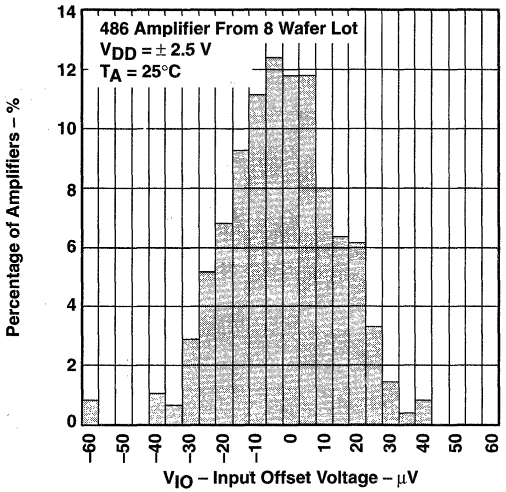


Figure 2

DISTRIBUTION OF TLC4501 INPUT OFFSET VOLTAGE

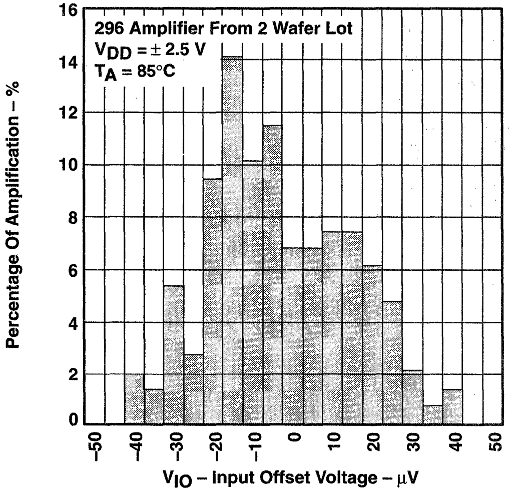


Figure 3

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

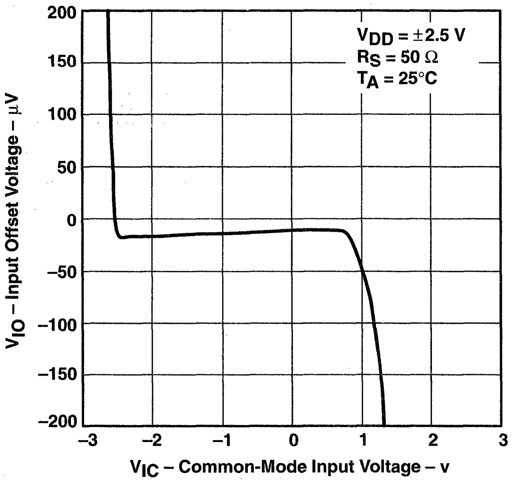


Figure 4

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC4501 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

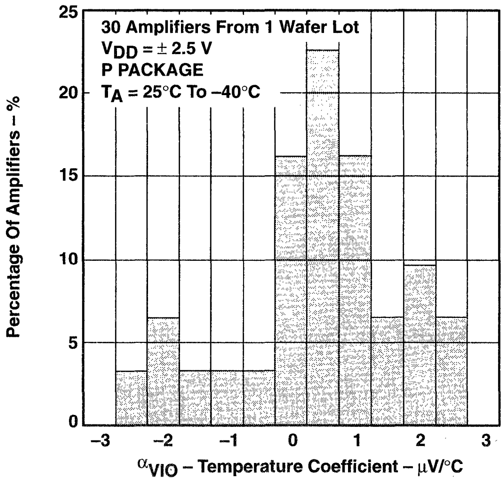


Figure 5

DISTRIBUTION OF TLC4501 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

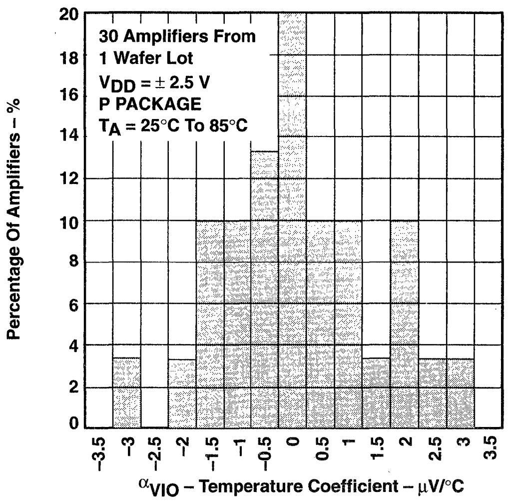


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

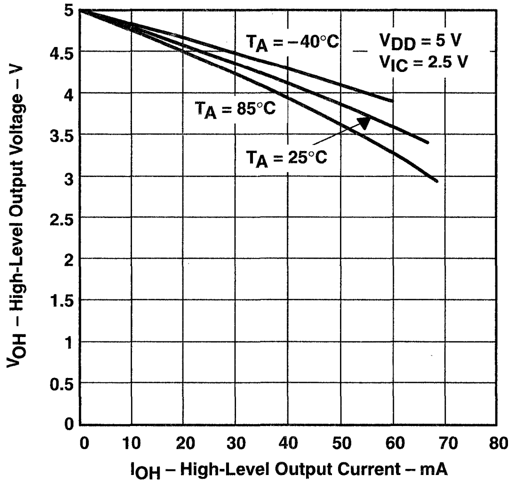


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

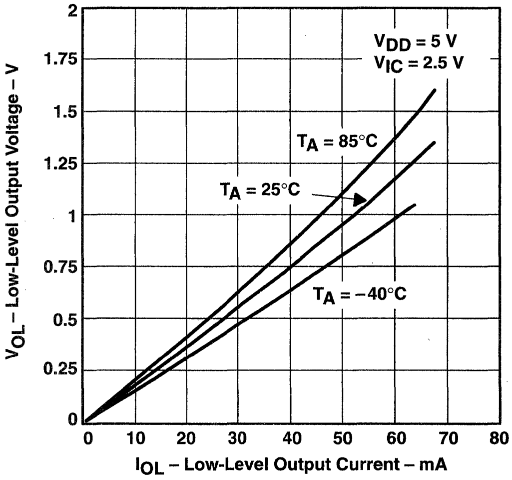


Figure 8

TYPICAL CHARACTERISTICS

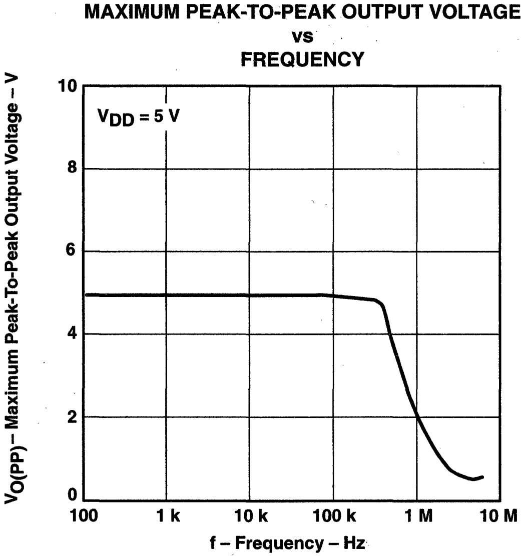


Figure 9

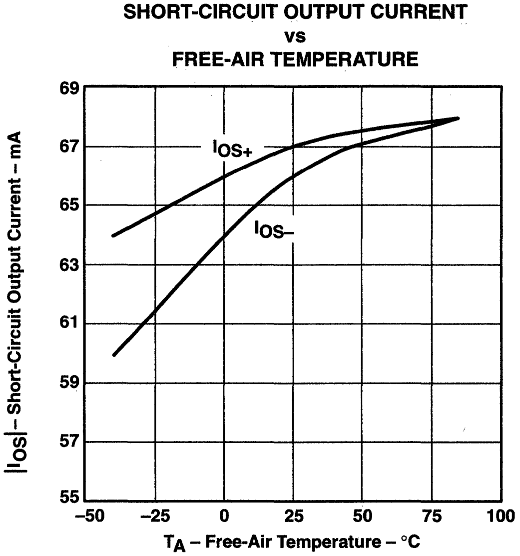


Figure 10

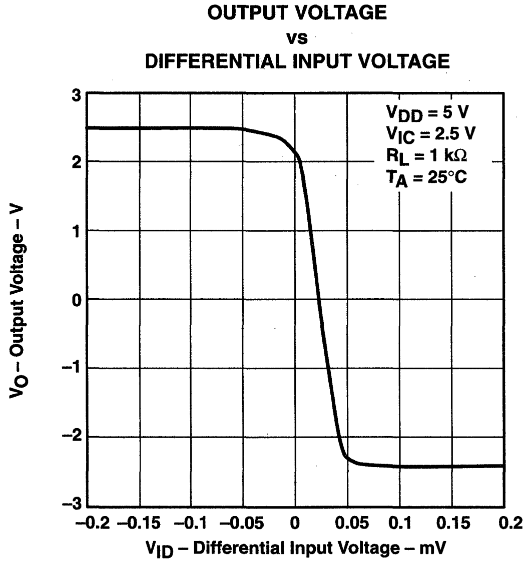


Figure 11

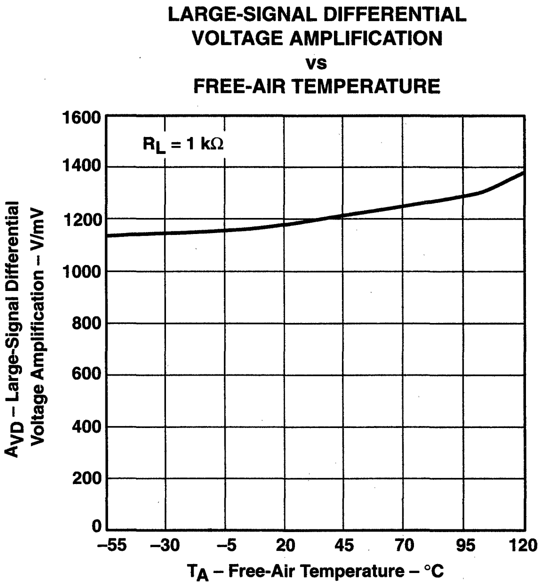


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

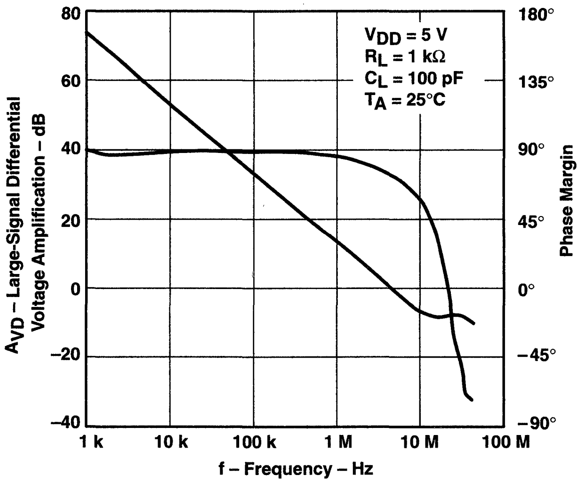


Figure 13

OUTPUT IMPEDANCE vs FREQUENCY

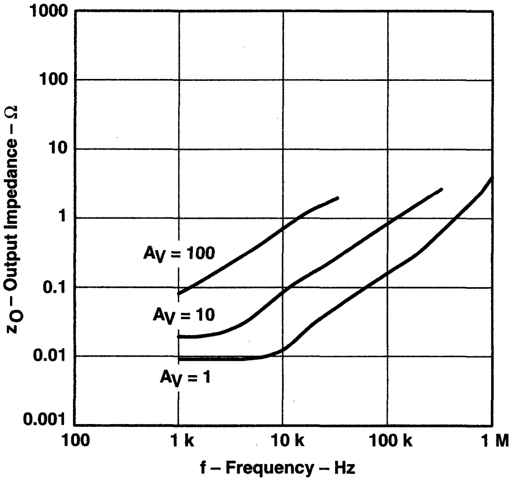


Figure 14

COMMON-MODE REJECTION RATIO vs FREQUENCY

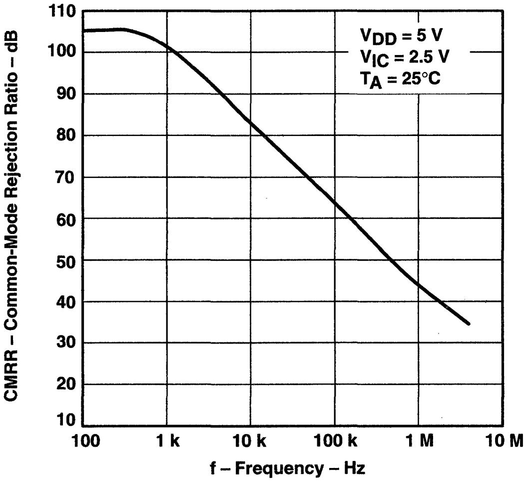


Figure 15

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

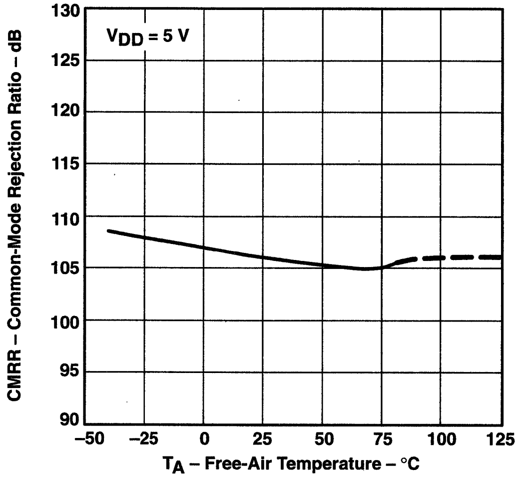


Figure 16

SLEW RATE vs LOAD CAPACITANCE

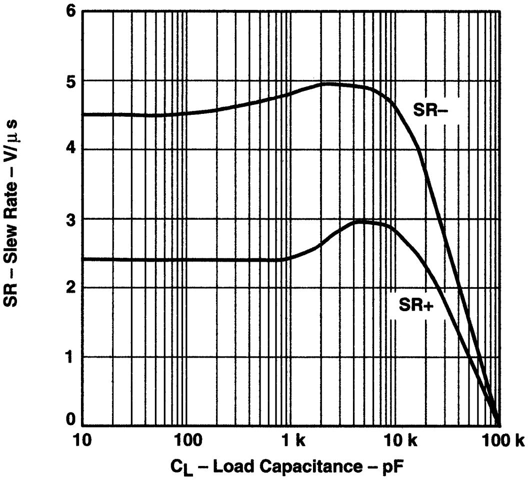


Figure 17

SLEW RATE vs FREE-AIR TEMPERATURE

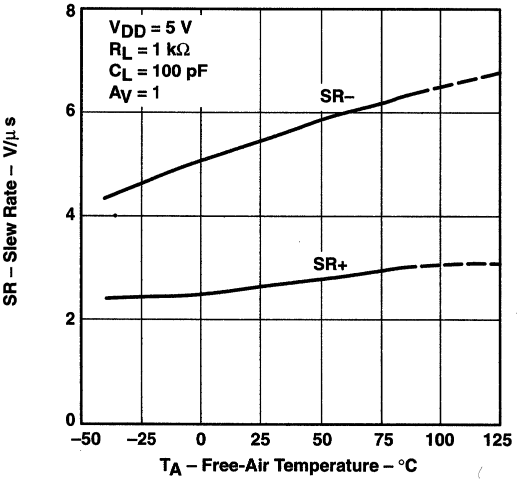


Figure 18

INVERTING LARGE-SIGNAL PULSE RESPONSE

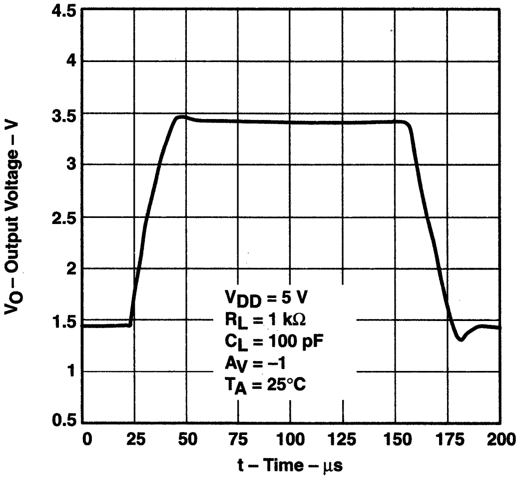


Figure 19

TYPICAL CHARACTERISTICS

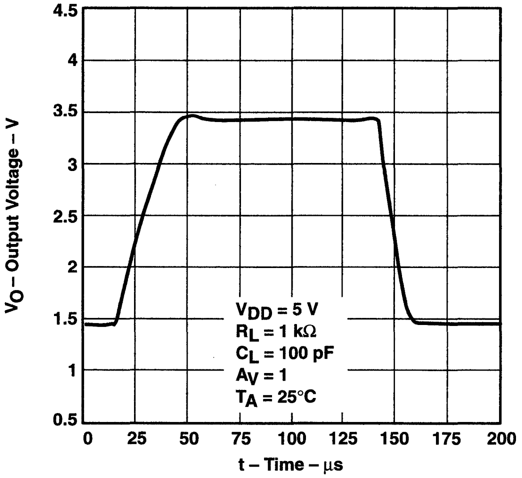

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

Figure 20

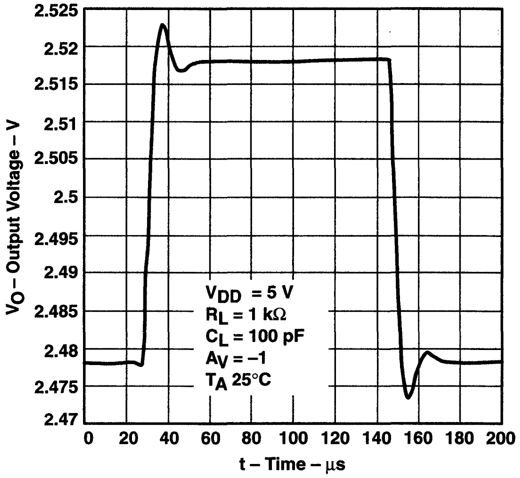

INVERTING SMALL-SIGNAL PULSE RESPONSE

Figure 21

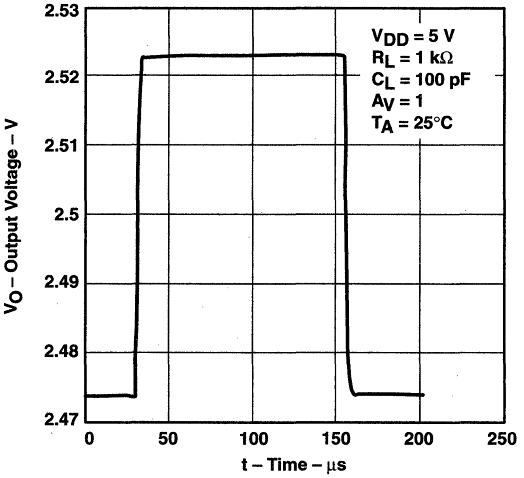

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

Figure 22

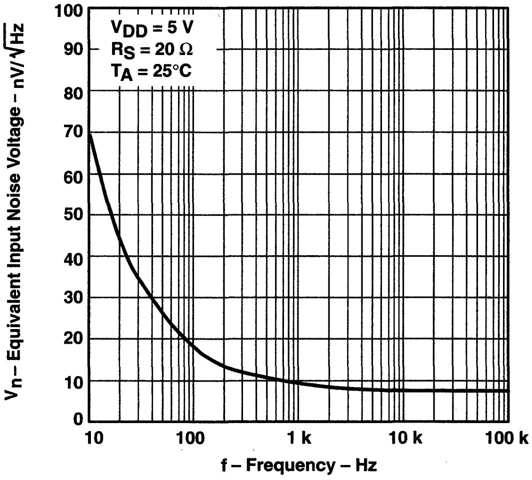

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

Figure 23

TYPICAL CHARACTERISTICS

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

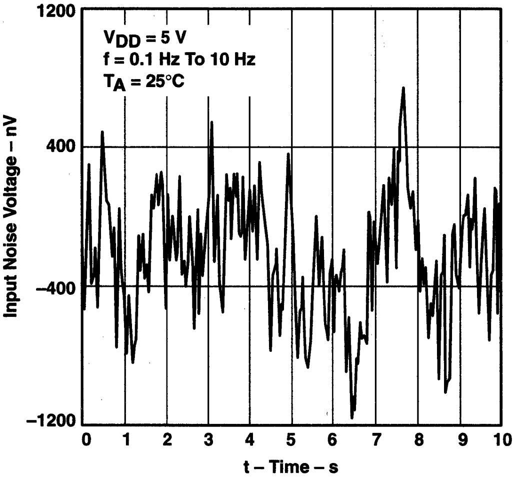


Figure 24

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

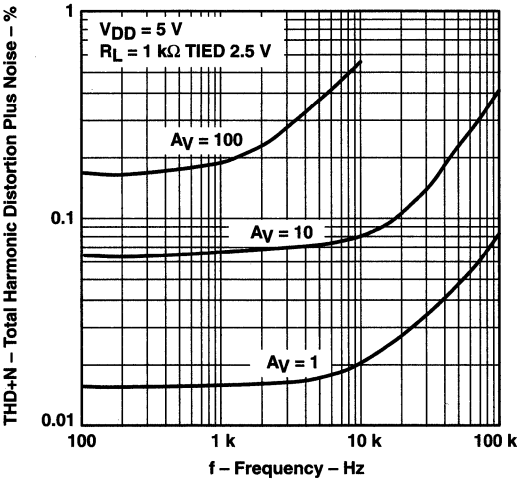


Figure 25

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

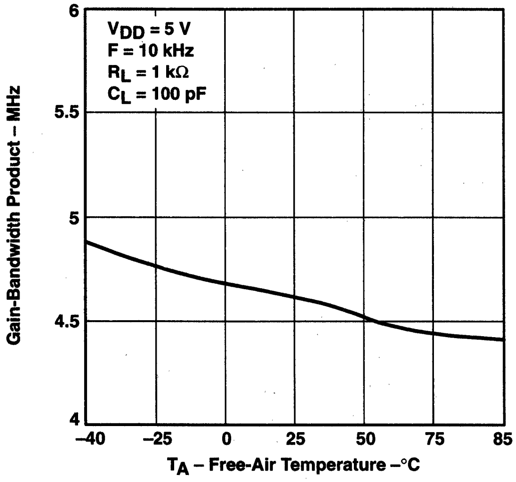


Figure 26

PHASE MARGIN vs LOAD CAPACITANCE

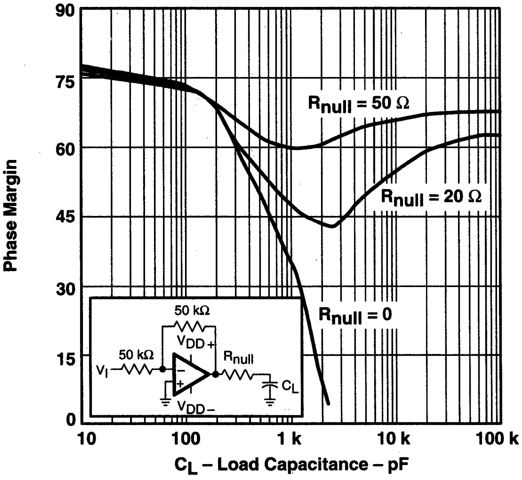


Figure 27

TYPICAL CHARACTERISTICS

GAIN MARGIN
vs
LOAD CAPACITANCE

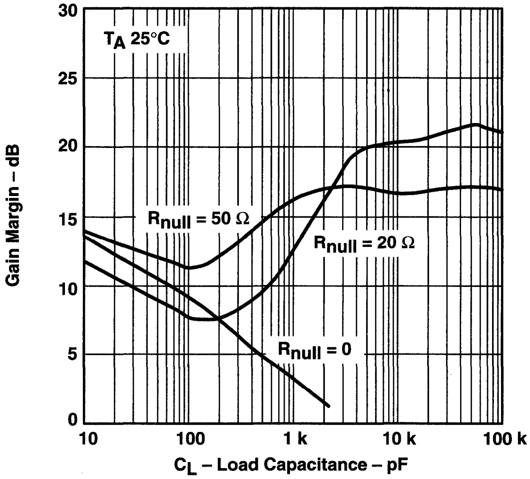


Figure 28

POWER SUPPLY REJECTION RATIO
vs
FREE-AIR TEMPERATURE

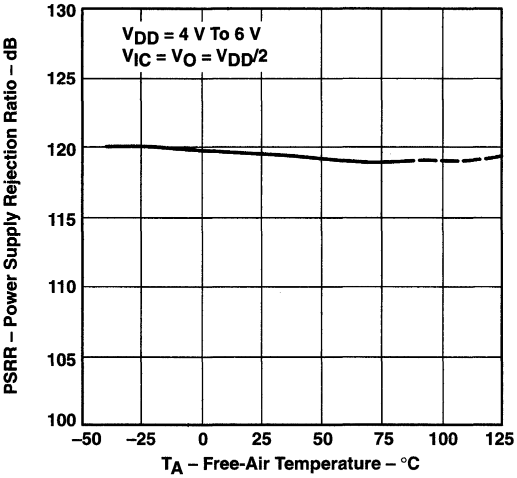


Figure 29

CALIBRATION TIME AT –40°C

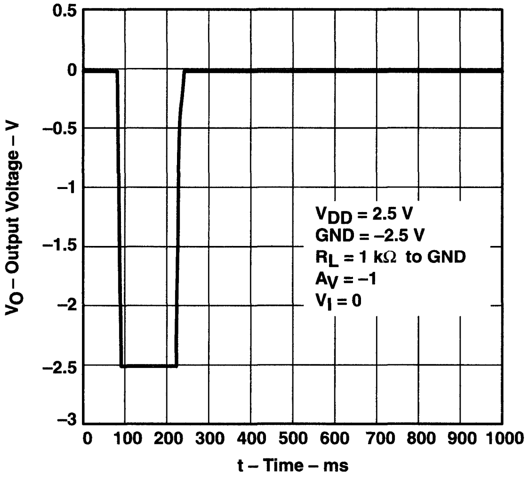


Figure 30

CALIBRATION TIME AT 25°C

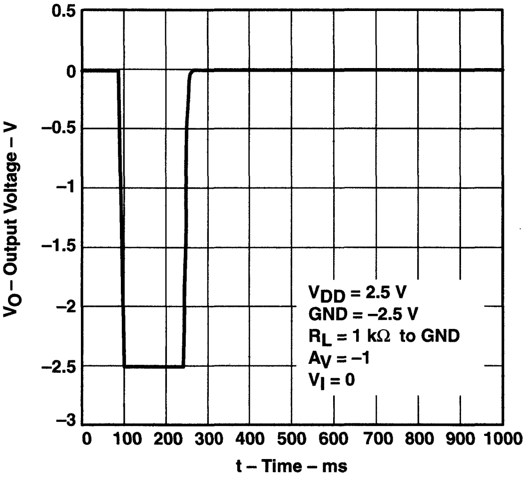


Figure 31

TYPICAL CHARACTERISTICS

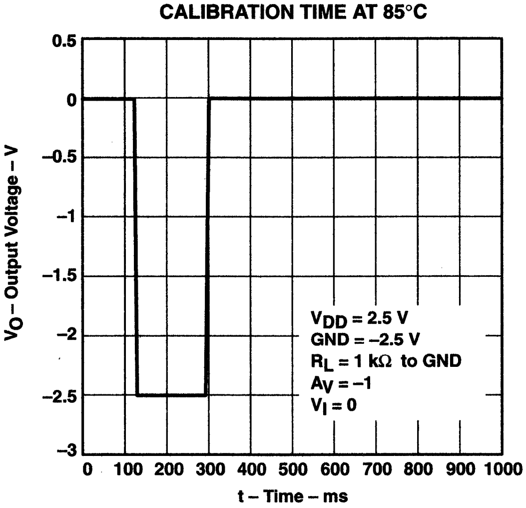


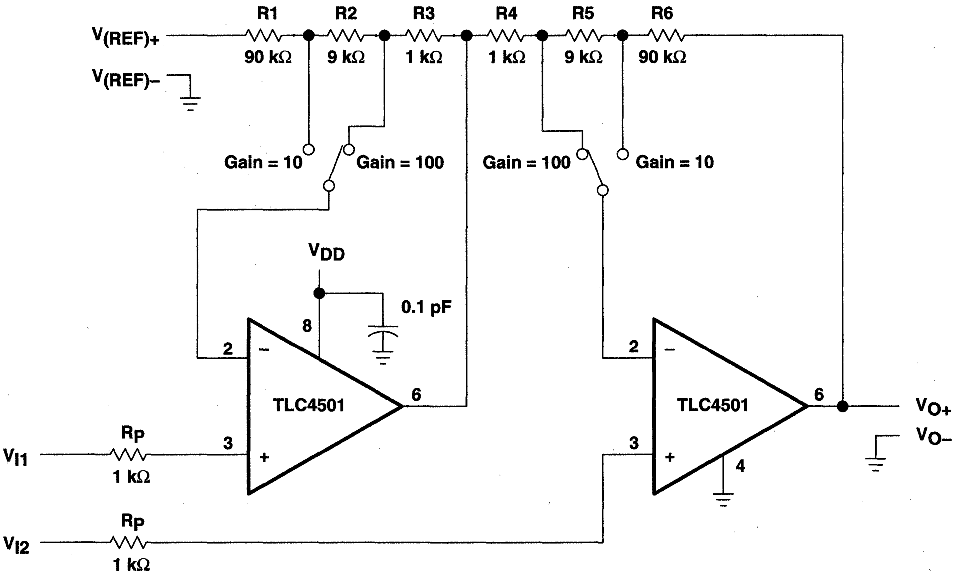
Figure 32

APPLICATION INFORMATION

- The TLC4501 is designed to operate with only a single 5-V power supply, have true differential inputs, and remain in the linear mode with an input common-mode voltage of 0.
- The TLC4501 has a standard single-amplifier pinout allowing for easy design upgrades.
- Large differential input voltages can be easily accommodated and, as input differential-voltage protection diodes are not needed, no large input currents result from large differential input voltage. Protection should be provided to prevent the input voltages from going negative more than −0.3 V at 25°C. An input clamp diode with a resistor to the device input terminal can be used for this purpose.
- For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor can be used from the output of the amplifier to ground. This increases the class-A bias current and prevents crossover distortion. Where the load is directly coupled, for example dc applications, there is no crossover distortion.
- Capacitive loads, which are applied directly to the output of the amplifier, reduce the loop stability margin. Values of 500 pF can be accommodated using the worst-case noninverting unity-gain connection. Resistive isolation should be considered when larger load capacitance must be driven by the amplifier.

The following typical application circuits emphasize operation on only a single power supply. When complementary power supplies are available, the TLC4501 can be used in all of the standard operational amplifier circuits. In general, introducing a pseudo-ground (a bias voltage of $V_I/2$ like that generated by the TLE2426) allows operation above and below this value in a single-supply system. Many application circuits are shown which take advantage of the wide common-mode input-voltage range of the TLC4501, which includes ground. In most cases, input biasing is not required and input voltages that range to ground can easily be accommodated.

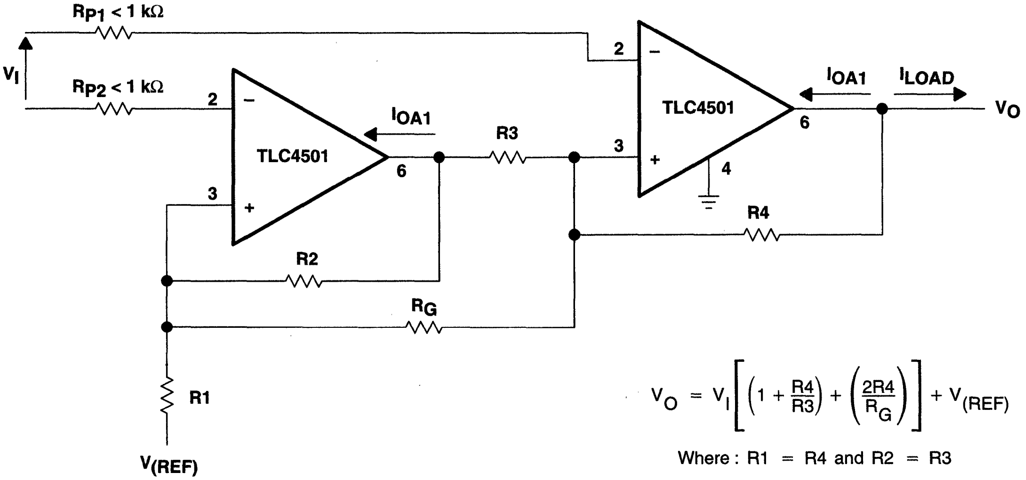
APPLICATION INFORMATION



$$(\text{Gain} = 10)\quad V_O = \left(V_{I1} - V_{I2}\right)\left(1 + \frac{R6}{R4 + R5}\right) + V_{(REF)}\quad \text{Where R1} = \text{R6, R2} = \text{R5, and R3} = \text{R4}$$

$$(\text{Gain} = 100)\quad V_O = \left(V_{I1} - V_{I2}\right)\left(1 + \frac{R5 + R6}{R4}\right) + V_{(REF)}\quad \text{Where R1} = \text{R6, R2} = \text{R5, and R3} = \text{R4}$$

Figure 33. Single-Supply Programmable Instrumentation Amplifier Circuit

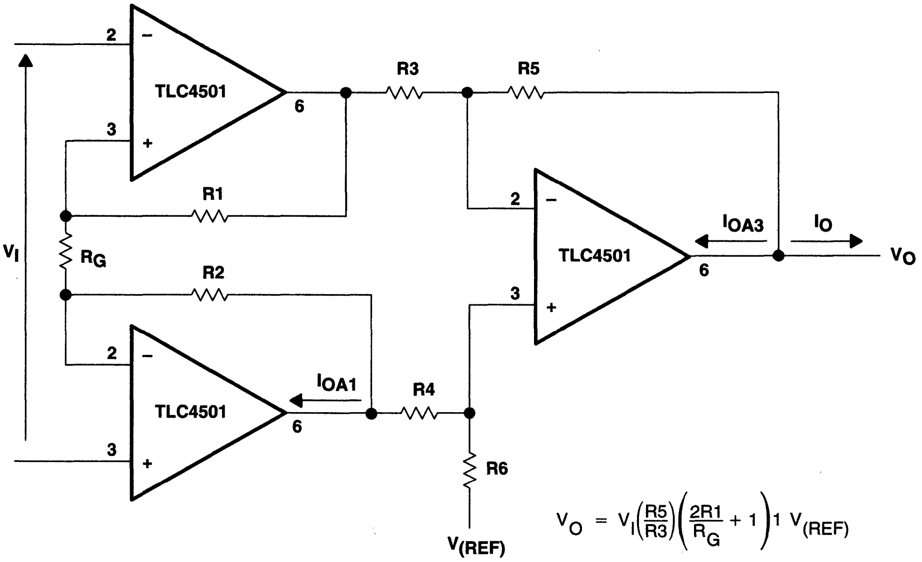


$$V_O = V_I\left[\left(1 + \frac{R4}{R3}\right) + \left(\frac{2R4}{R_G}\right)\right] + V_{(REF)}$$

Where : R1 = R4 and R2 = R3

Figure 34. Two Operational-Amplifier Instrumentation Amplifier Circuit

APPLICATION INFORMATION



$$V_O = V_I\left(\frac{R5}{R3}\right)\left(\frac{2R1}{R_G} + 1\right) 1\ V_{(REF)}$$

Where : R1 = R2, R3 = R4, and R5 = R6

Figure 35. Three Operational-Amplifier Instrumentation Amplifier Circuit

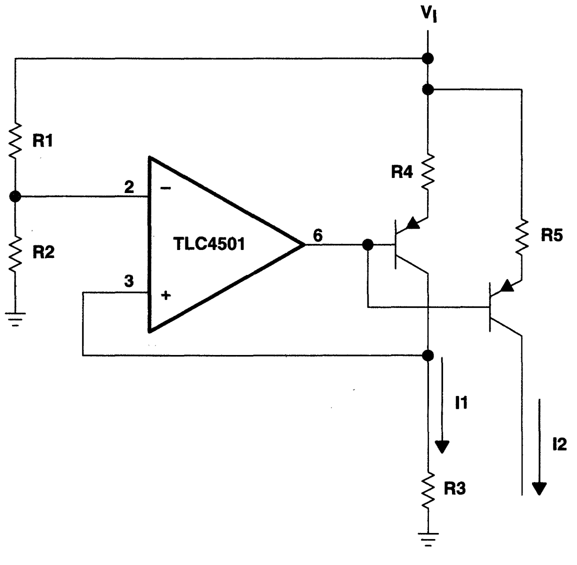


Figure 36. Fixed Current-Source Circuit

APPLICATION INFORMATION

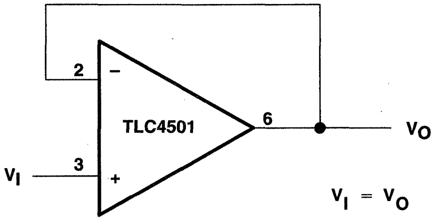


Figure 37. Voltage-Follower Circuit

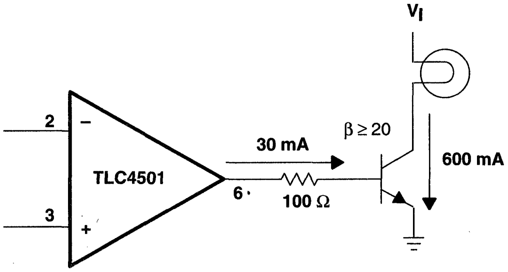


Figure 38. Lamp-Driver Circuit

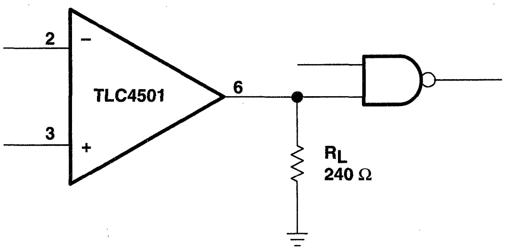


Figure 39. TTL-Driver Circuit

APPLICATION INFORMATION

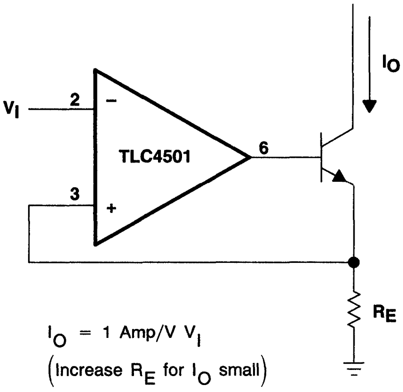


Figure 40. High-Compliance Current-Sink Circuit

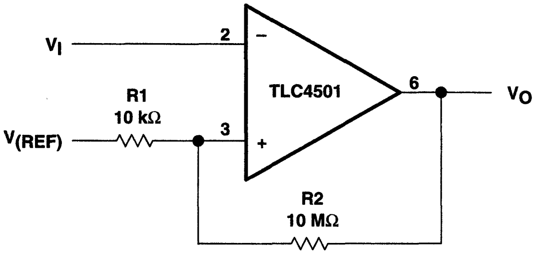


Figure 41. Comparator With Hysteresis Circuit

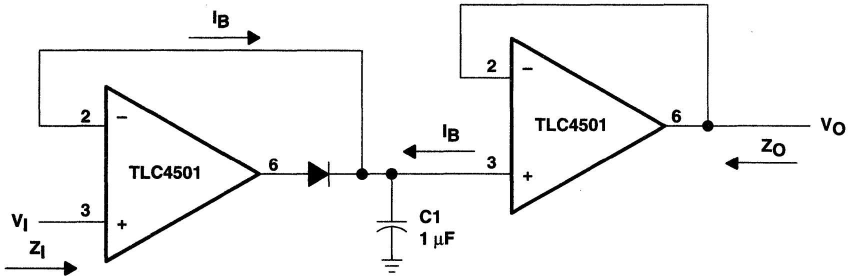


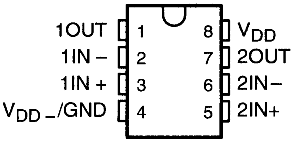
Figure 42. Low-Drift Detector Circuit

TLC4502, TLC4502A, TLC4502Y
Advanced LinEPIC™ SELF-CALIBRATING (Self-Cal™) PRECISION DUAL OPERATIONAL AMPLIFIERS

SLOS161A – OCTOBER 1996 – REVISED NOVEMBER 1996

- **Power On Calibration of Input Offset Voltage**
- **Low Input Offset Voltage . . . < 50 μV Max (TLC4502A)**
- **Low Input Offset Voltage Drift . . . < 1 μV/°C**
- **Low Input Bias Current**
- **High Output Drive Capability C_L < 1 nF and R_L > 1 kΩ**
- **High Open Loop Gain . . . > 120 dB**
- **Rail-To-Rail Output Voltage Swing**
- **Low Distortion . . . < 0.01% at 10 kHz**
- **Low Noise . . . 12 nV/√Hz at 1 kHz**
- **High Slew Rate . . . 2.5 V/μs**
- **Low Power Consumption . . . < 1.5 mA (Typical) Per Amplifier**
- **Short Calibration Time . . . 300 ms Typ**

D PACKAGE
(TOP VIEW)



description

The TLC4502 self-calibrating operational amplifier utilizes the recent availability of on-chip digital and analog signal processing to automatically null the input offset voltage at power-up. This *self-calibrating* feature requires typically 300 ms to complete and is repeatable to within ±3 μV on successive calibrations. The technique involves the extraction and digital storage of the key offset-nulling information. This information is retained without degradation as long as the circuit is powered. This eliminates the need for continuous chopping of the input signal to refresh the offset information. Once the process is complete, the bulk of the calibration circuitry drops out of the signal path and shuts down. This minimizes or eliminates any effect the calibration circuitry might have on the desired signal path. It also allows the TLC4502 to be used exactly like any other operational amplifier after the calibration cycle is complete.

The TLC4502 is a high-performance operational amplifier fabricated in a 1-μm 5-V digital CMOS technology. It achieves very high dc gain, as well as excellent power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR). It uses a mixed-mode (analog/digital) internal compensation loop with digital storage of the offset information and a current-mode output to reduce its input offset to < 50 μV. The TLC4502 also features a rail-to-rail output structure capable of driving loads to 1 kΩ and 1 nF. Unlike existing commercially available low-offset high-precision amplifiers, the TLC4502 needs only a single 5-V supply, requires no trimming, and uses no bipolar transistors or JFETs.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICE†	CHIP FORM (Y)
		SMALL OUTLINE (D)	
0°C to 70°C	50 μV	TLC4502ACDR	TLC4502Y
	100 μV	TLC4502CDR	
–40°C to 85°C	50 μV	TLC4502AIDR	
	100 μV	TLC4502IDR	

† The D package is also available taped and reeled.

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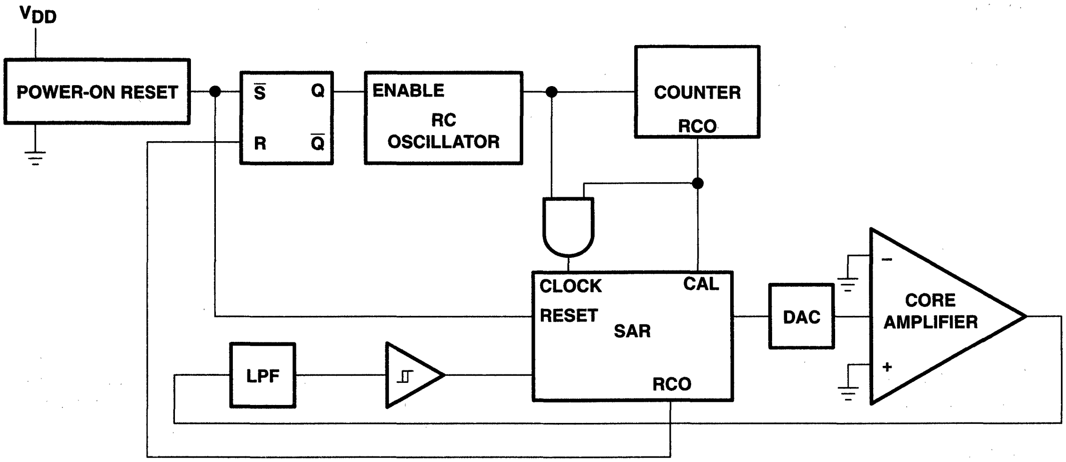
description (continued)

To achieve high dc gain, large bandwidth, high CMRR and PSRR, as well as good output drive capability, the TLC4502 is built around a 3-stage topology: two gain stages, one rail-to-rail, and a class-AB output stage. A nested Miller topology is used for frequency compensation.

functional block diagram (during calibration)



During the calibration procedure, the operational amplifier is removed from the signal path and both inputs are tied to GND.

The class AB output stage features rail-to-rail voltage swing and incorporates additional switches to put the output node into a high-impedance mode during the calibration cycle. Small-replica output transistors (matched to the main output transistors) provide the amplifier output signal for the calibration circuit. The TLC4502 also features built-in output short-circuit protection. The output current flowing through the main output transistors is continuously being sensed. If the current through either of these transistors exceeds the preset limit (60 mA – 70 mA) for more than about 1 μs, the output transistors are shut down to essentially their quiescent operating point for approximately 5 ms. The device is then returned to normal operation. If the short circuit is still in place, it is detected in less than 1 μs and the device is shutdown for another 5 ms.

The offset cancellation uses a current-mode digital-to-analog converter (DAC), whose full-scale current allows for an adjustment of approximately ±5 mV to the input offset voltage. The digital code producing the cancellation current is stored in the successive-approximation register (SAR).

During power up, when the offset cancellation procedure is initiated, an on-chip RC oscillator is activated to provide the timing of the successive-approximation algorithm. To prevent wide-band noise from interfering with the calibration procedure, an analog low-pass filter followed by a Schmidt trigger is used in the decision chain to implement an averaging process. Once the calibration procedure is complete, the RC oscillator is deactivated to reduce supply current and the associated noise.

The key operational-amplifier parameters CMRR, PSRR, and offset drift were optimized to achieve superior offset performance. The TLC4502 calibration DAC is implemented by a binary-weighted current array using a pseudo-R-2R MOSFET ladder architecture, which minimizes the silicon area required for the calibration circuitry, and thereby reduces the cost of the TLC4502.

description (continued)

Due to the performance (precision, PSRR, CMRR, gain, output drive, and ac performance) of the TLC4502, it is ideal for applications like:

- Data acquisition systems
- Medical equipment
- Portable digital scales
- Strain gauges
- Automotive sensors
- Digital audio circuits
- Industrial control applications

It is also ideal in circuits like:

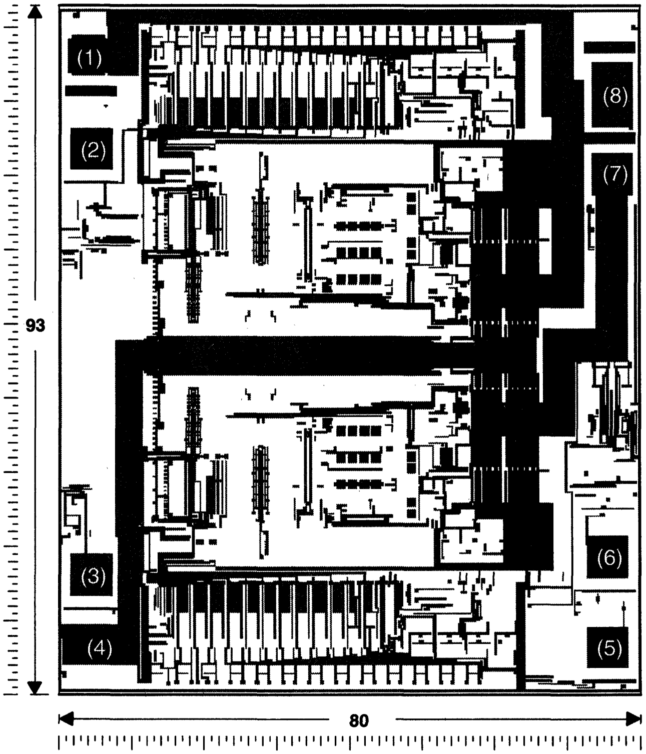
- A precision buffer for current-to-voltage converters, a/d buffers, or bridge applications
- High-impedance buffers or preamplifiers
- Long term integration
- Sample-and-hold circuits
- Peak detectors

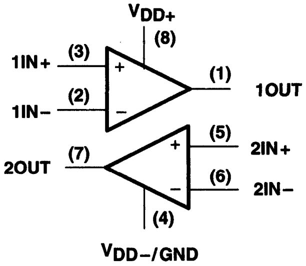
The TLC4502 self-calibrating operational amplifier is manufactured using Texas instruments LinEPIC process technology and is available in an 8-pin SOIC (D) Package. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C.

TLC4502Y chip information

This chip, when properly assembled, display characteristics similar to the TLC4502C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	7 V
Differential input voltage, V_{ID} (see Note 2)	±7 V
Input voltage range, V_I (any input, see Note 1)	–0.3 V to 7 V
Input current, I_I (each input)	±5 mA
Output current, I_O (each output)	±100 mA
Total current into V_{DD+}	±100 mA
Total current out of V_{DD-}/GND	±100 mA
Electrostatic discharge (ESD)	> 2 kV
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC4502C	0°C to 70°C
TLC4502I	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 60 seconds, T_C: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND.
2. Differential voltages are at IN+ with respect to IN–. Excessive current flows when an input is brought below V_{DD-} – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions

	TLC4502C		TLC4502I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	4	6	4	6	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Operating free-air temperature, T_A	0	70	–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, GND = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC4502C			TLC4502AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±2.5 V, V_O = 0, V_{IC} = 0, R_S = 50 Ω	25°C	–100		100	–50		50	μV
			Full range	–100		100	–50		50	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1			1		μV/°C
I_{IO}	Input offset current		25°C		1			1		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{OH}	High-level output voltage	I_{OH} = – 500 μA	25°C		4.99			4.99		V
		I_{OH} = – 5 mA	25°C		4.9			4.9		
			Full range	4.7			4.7			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.1			0.1		
			Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 kΩ, See Note 4	25°C	200	1000		200	1000		V/mV
			Full range	200			200			
$R_{I(D)}$	Differential input resistance		25°C		10			10		kΩ
R_L	Input resistance	See Note 4	25°C		10^{12}			10^{12}		Ω
C_L	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_O	Closed-loop output impedance	A_V = 10, f = 100 kHz	25°C		1			1		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 1 kΩ	25°C	90	100		90	100		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4 V to 6 V, V_{IC} = 0, No load	25°C	90	100		90	100		dB
			Full range	90			90			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		2.5	3.5		2.5	3.5	mA
			Full range			4			4	
$V_{IT(CAL)}$	Calibration input threshold voltage		Full range	4			4			V

† Full range is 0°C to 70°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, GND = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC4502I			TLC4502AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±2.5 V, V_O = 0, V_{IC} = 0, R_S = 50 Ω	25°C	–100		100	–50		50	µV
			Full range	–100		100	–50		50	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1			1		µV/°C
I_{IO}	Input offset current		25°C		1			1		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{OH}	High-level output voltage	I_{OH} = – 500 µA	25°C		4.99			4.99		V
		I_{OH} = – 5 mA	25°C		4.9			4.9		
			Full range	4.7			4.7			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.1			0.1		
			Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 kΩ, See Note 4	25°C	200	1000		200	1000		V/mV
			Full range	200			200			
$R_{I(D)}$	Differential input resistance		25°C		10			10		kΩ
R_L	Input resistance	See Note 4	25°C		10^{12}			10^{12}		Ω
C_L	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_O	Closed-loop output impedance	A_V = 10, f = 100 kHz	25°C		1			1		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 1 kΩ	25°C	90	100		90	100		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} \pm / \Delta V_{IO}$)	V_{DD} = 4 V to 6 V, V_{IC} = 0, No load	25°C	90	100		90	100		dB
			Full range	90			90			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		2.5	3.5		2.5	3.5	mA
			Full range			4			4	
$V_{IT(CAL)}$	Calibration input threshold voltage		Full range	4			4			V

† Full range is –40°C to 85°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC4502C, TLC4502AC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, C_L = 100 pF		25°C	1.5	2.5		V/μs
				Full range	1			V/μs
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		70		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1		μV
		f = 0.1 to 10 Hz		25°C		1.5		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 1 kΩ, C_L = 100 pF	A_V = 1	25°C		0.02%		
			A_V = 10	25°C		0.08%		
			A_V = 100	25°C		0.55%		
	Gain-bandwidth product	f = 10 kHz, R_L = 1 kΩ, C_L = 100 pF		25°C		4.7		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 1 kΩ, C_L = 100 pF		25°C		1		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 1 kΩ, C_L = 100 pF	to 0.1%	25°C		1.6		μs
			to 0.01%	25°C		2.2		
ϕ_m	Phase margin at unity gain	R_L = 1 kΩ, C_L = 100 pF		25°C		74		
	Calibration time			25°C		300		ms

† Full range is 0°C to 70°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC4502I, TLC4502AI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V,	C_L = 100 pF	25°C	1.5	2.5		V/µs
				Full range	1			V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		70		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1		µV
		f = 0.1 to 10 Hz		25°C		1.5		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 1 kΩ, C_L = 100 pF	A_V = 1	25°C		0.02%		
			A_V = 10	25°C		0.08%		
			A_V = 100	25°C		0.55%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 1 kΩ,	25°C		4.7		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 1 kΩ,	A_V = 1, C_L = 100 pF	25°C		1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 1 kΩ, C_L = 100 pF	to 0.1%	25°C		1.6		µs
			to 0.01%	25°C		2.2		
ϕ_m	Phase margin at unity gain	R_L = 1 kΩ,	C_L = 100 pF	25°C		74		
	Calibration time			25°C		300		ms

† Full range is −40°C to 85°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, GND = 0, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC4502Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±2.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω		10		μV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				1		pA
V_{OH}	High-level output voltage	I_{OH} = – 500 μA			4.99		V
		I_{OH} = – 5 mA			4.9		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 5 mA		0.1		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, R_L = 1 kΩ,	V_O = 1 V to 4 V, See Note 4		1000		V/mV
$R_{I(D)}$	Differential input resistance				10		kΩ
R_L	Input resistance	See Note 4			10^{12}		Ω
C_L	Common-mode input capacitance	f = 10 kHz,	P package		8		pF
z_O	Closed-loop output impedance	A_V = 10,	f = 100 kHz		1		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 1 kΩ	V_O = 2.5 V,		100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = ±2 V to ±3 V, No load	V_{IC} = 0,		100		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		2.5		mA

NOTE 4: R_L and C_L values are referenced to 2.5 V.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC4502Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V,	C_L = 100 pF		2.5		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz			70		nV/√Hz
		f = 1 kHz			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			1		μV
		f = 0.1 to 10 Hz			1.5		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 1 kΩ, C_L = 100 pF	A_V = 1		0.02%		
			A_V = 10		0.08%		
			A_V = 100		0.55%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 1 kΩ,		4.7		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 1 kΩ,	A_V = 1, C_L = 100 pF		1		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 1 kΩ, C_L = 100 pF	to 0.1%		1.6		μs
			to 0.01%		2.2		
ϕ_m	Phase margin at unity gain	R_L = 1 kΩ,	C_L = 100 pF		74		
	Calibration time				300		ms

NOTE 4: R_L and C_L values are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

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	Calibration time at 25°C	vs Time	31
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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC4502 INPUT OFFSET VOLTAGE

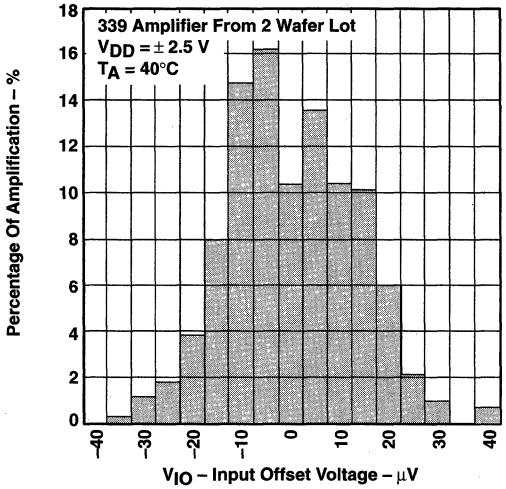


Figure 1

DISTRIBUTION OF TLC4502 INPUT OFFSET VOLTAGE

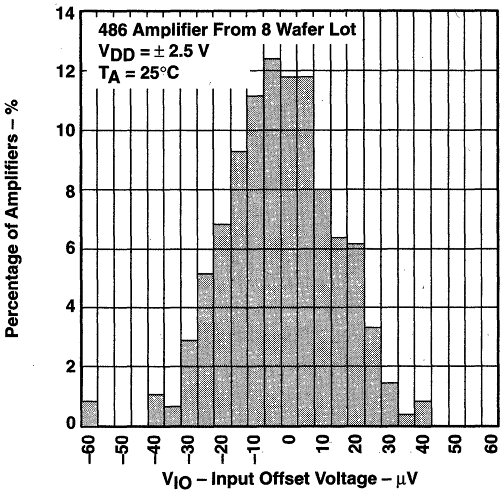


Figure 2

DISTRIBUTION OF TLC4502 INPUT OFFSET VOLTAGE

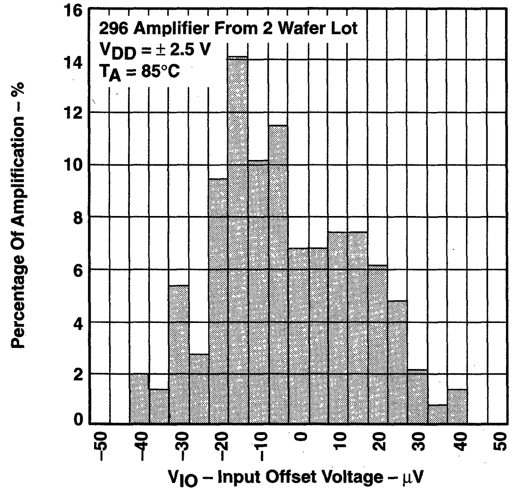


Figure 3

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

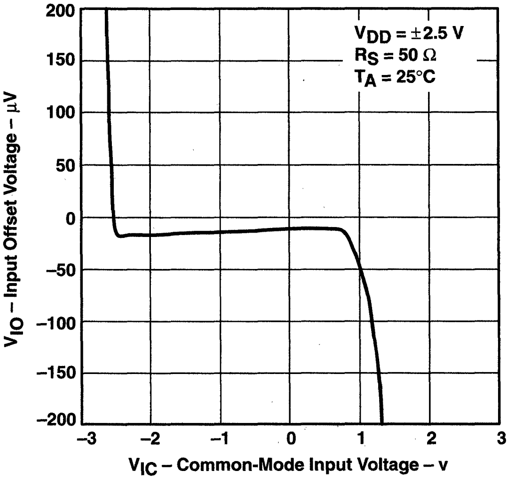


Figure 4

TYPICAL CHARACTERISTICS

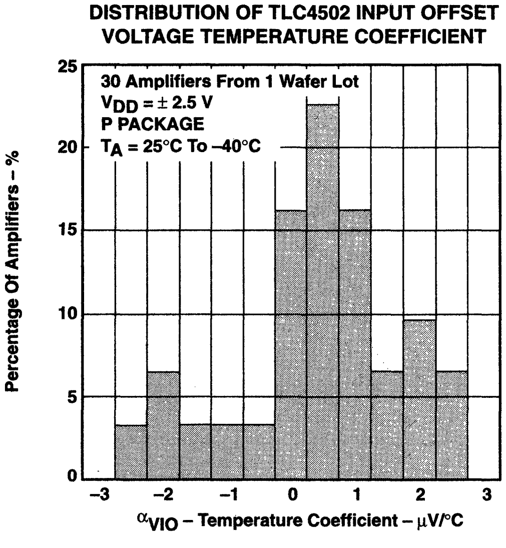


Figure 5

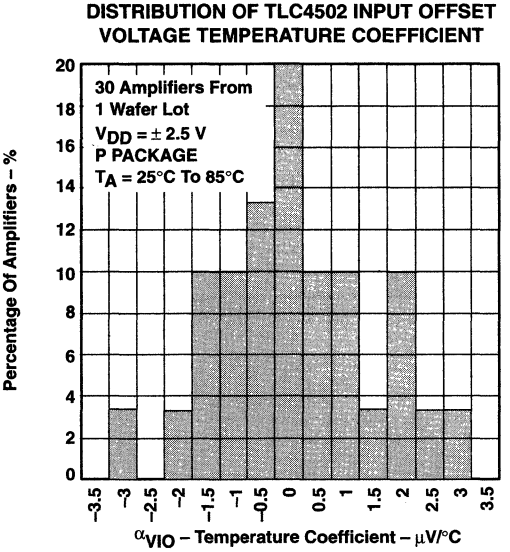


Figure 6

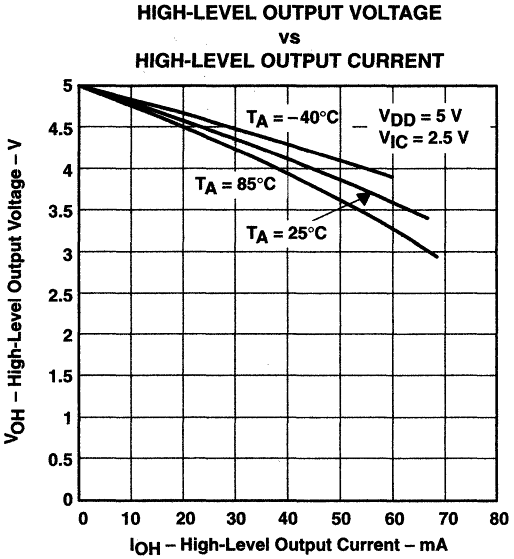


Figure 7

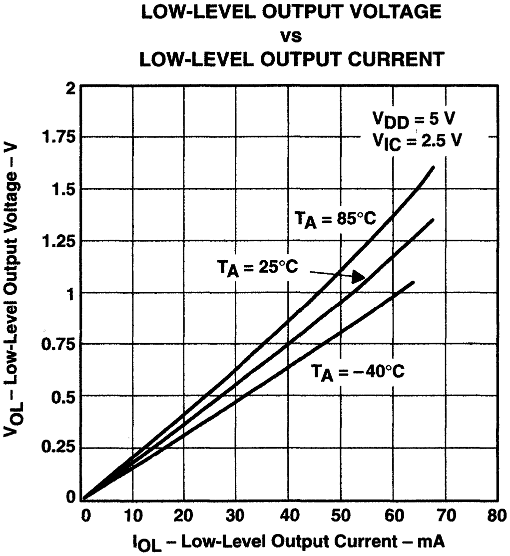


Figure 8

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

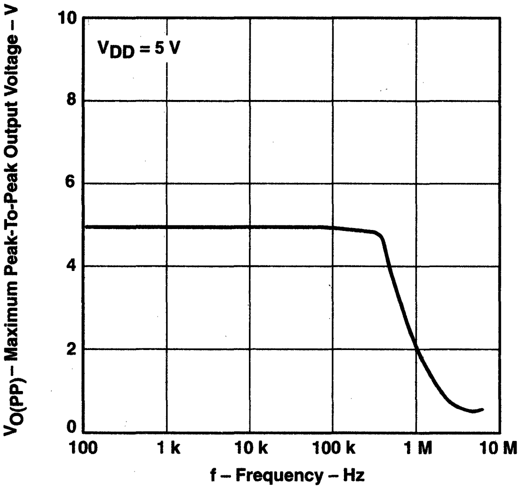


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

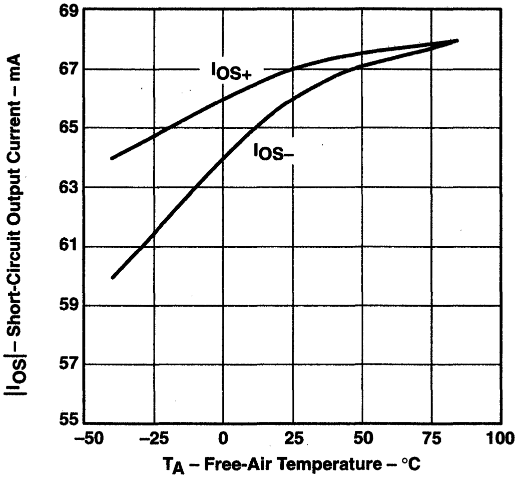


Figure 10

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

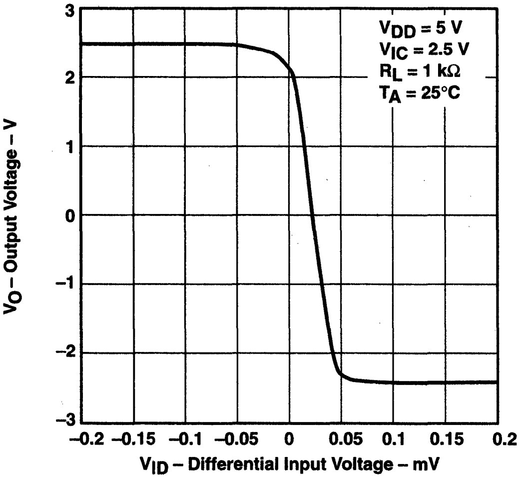


Figure 11

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

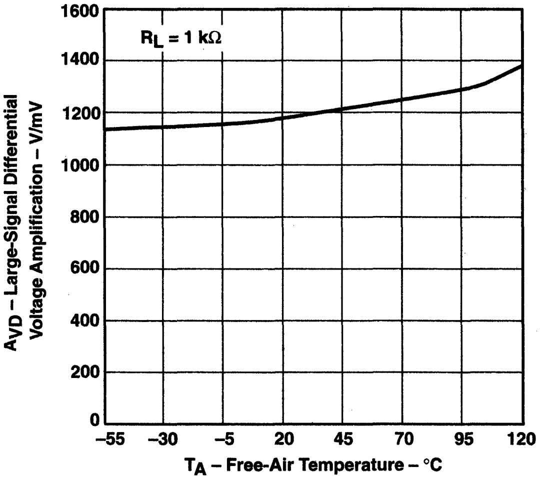


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

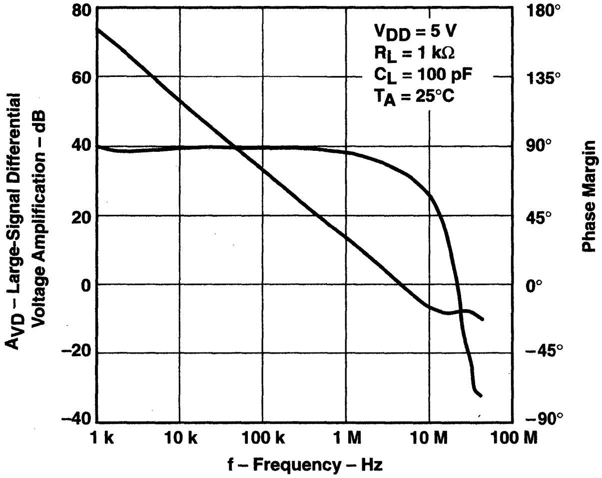


Figure 13

OUTPUT IMPEDANCE vs FREQUENCY

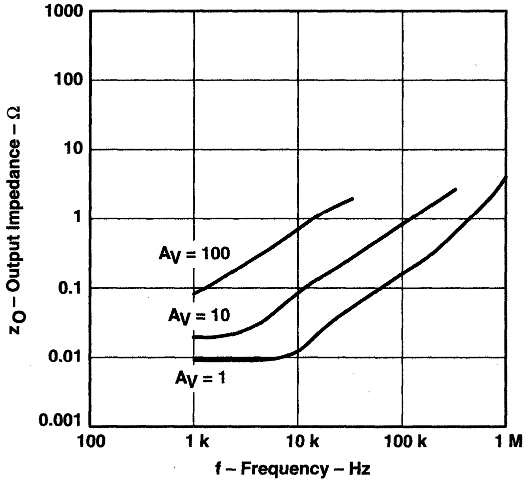


Figure 14

TYPICAL CHARACTERISTICS

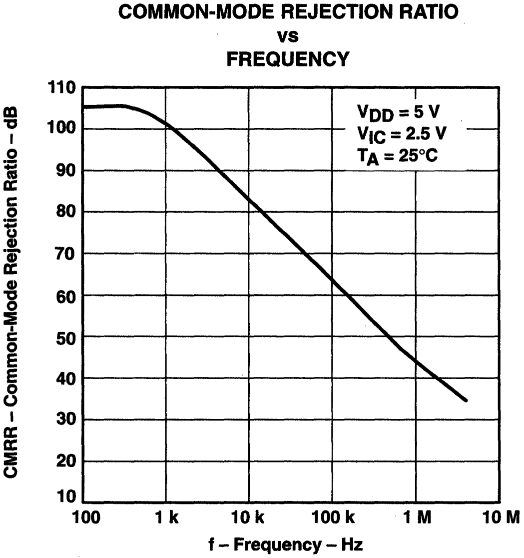


Figure 15

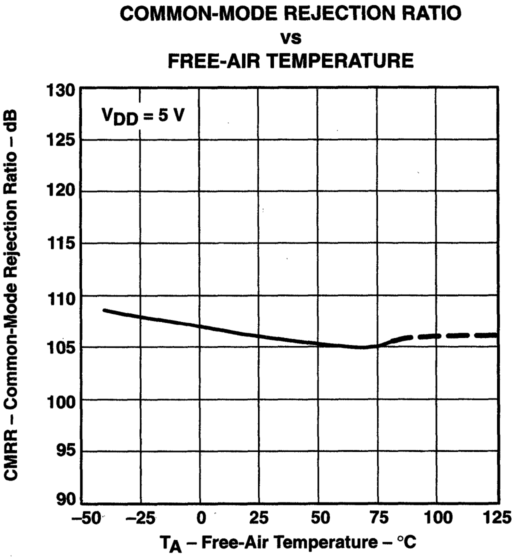


Figure 16

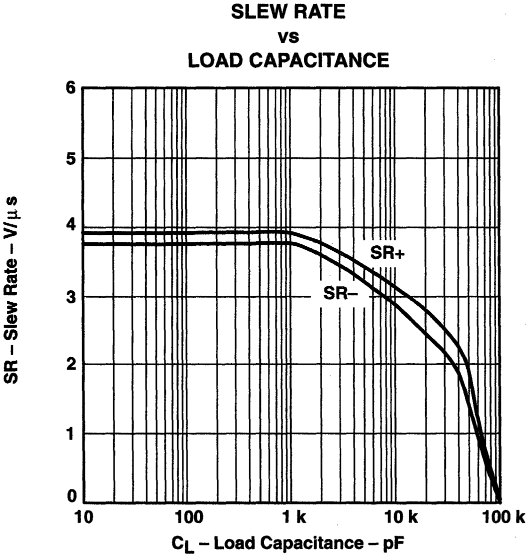


Figure 17

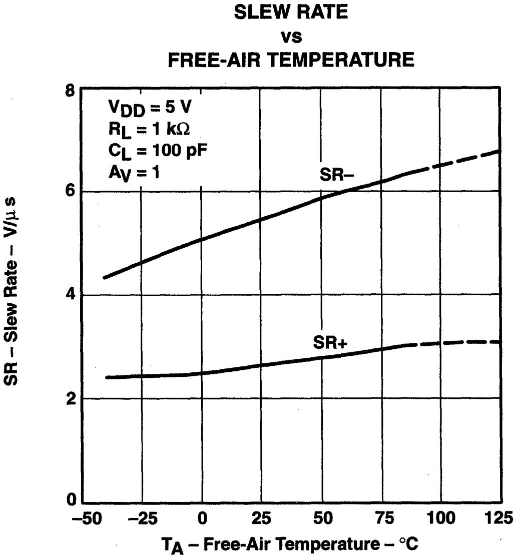


Figure 18

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

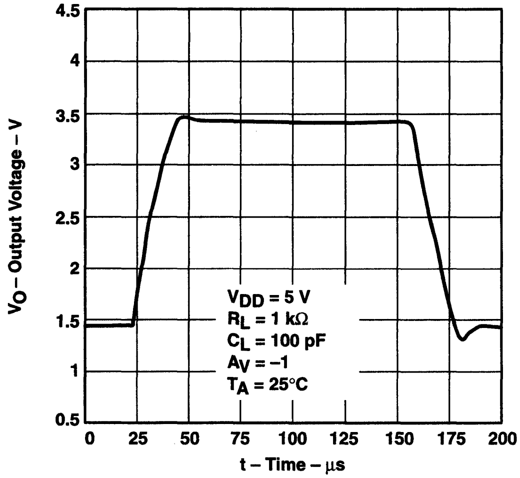


Figure 19

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

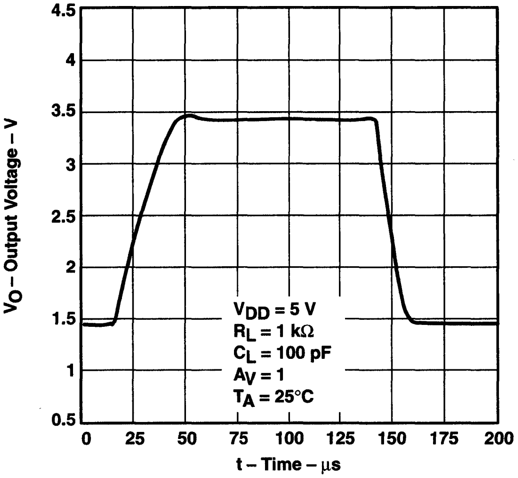


Figure 20

INVERTING SMALL-SIGNAL PULSE RESPONSE

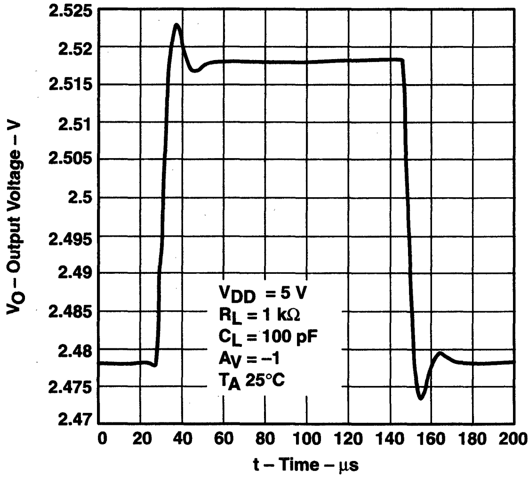


Figure 21

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

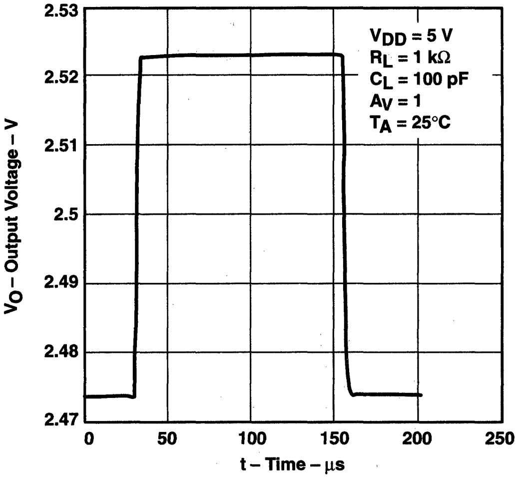


Figure 22

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

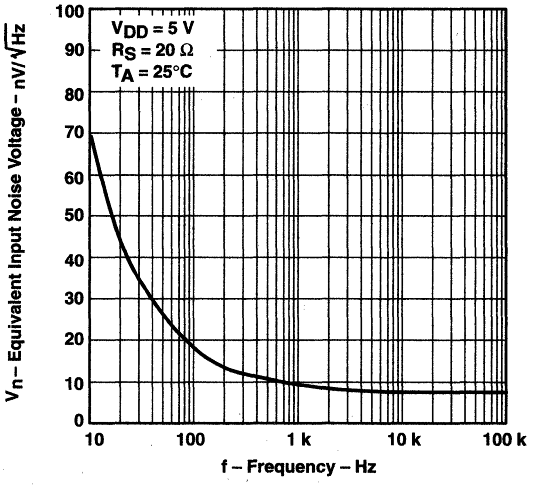


Figure 23

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

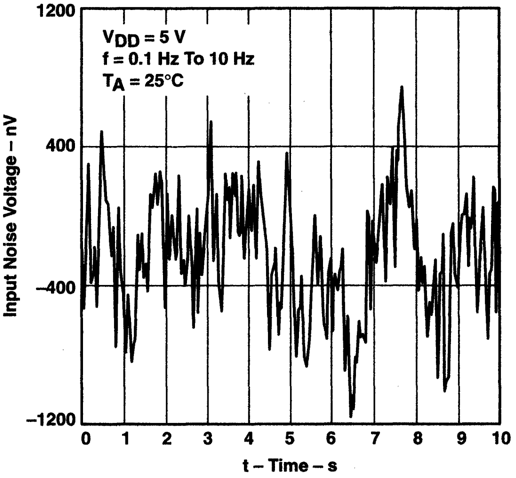


Figure 24

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

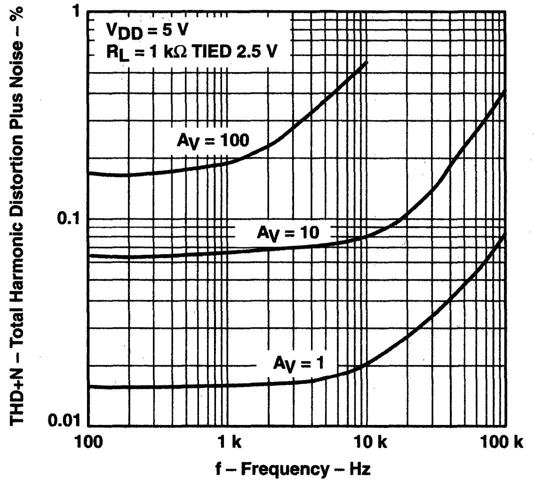


Figure 25

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

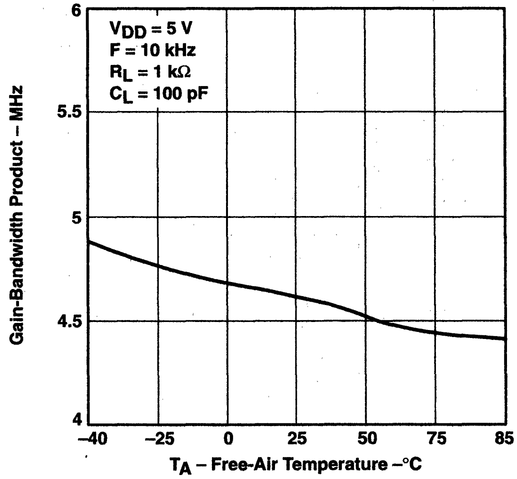


Figure 26

TYPICAL CHARACTERISTICS

PHASE MARGIN vs LOAD CAPACITANCE

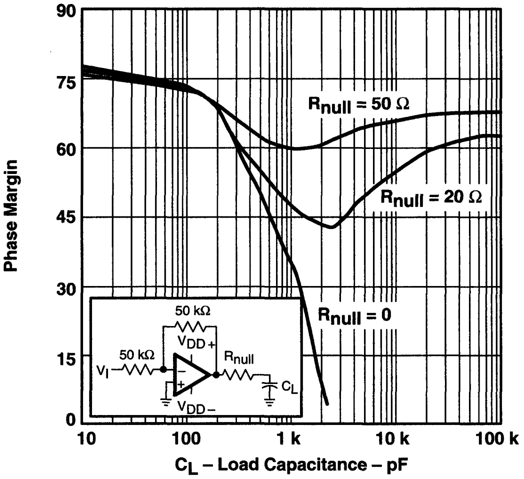


Figure 27

GAIN MARGIN vs LOAD CAPACITANCE

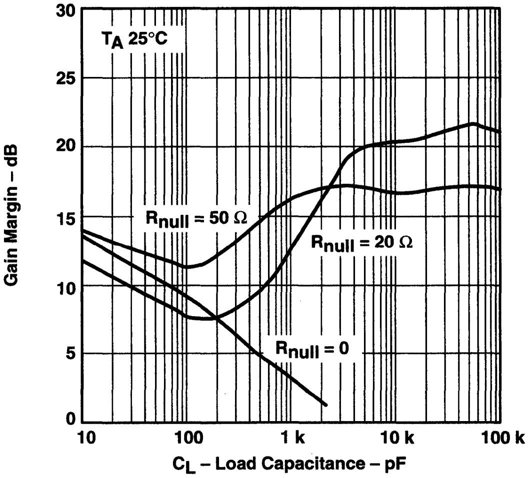


Figure 28

POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

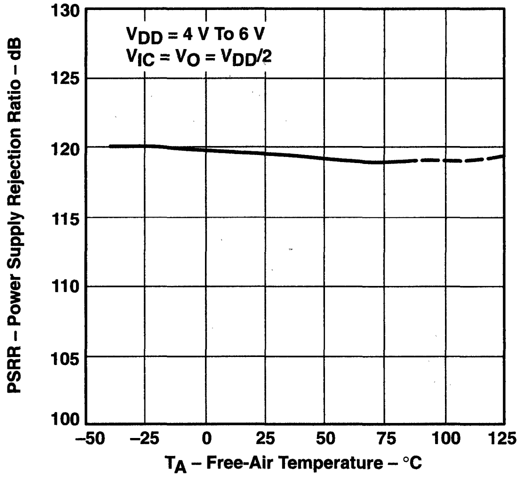


Figure 29

CALIBRATION TIME AT –40°C

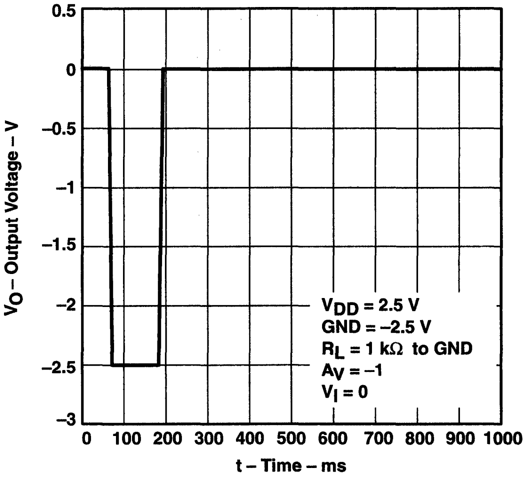


Figure 30

TYPICAL CHARACTERISTICS

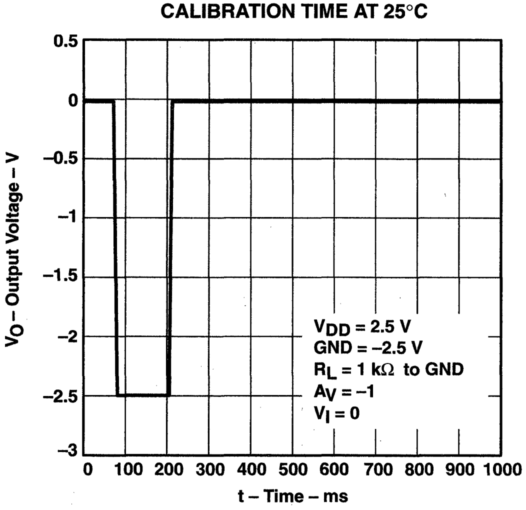


Figure 31

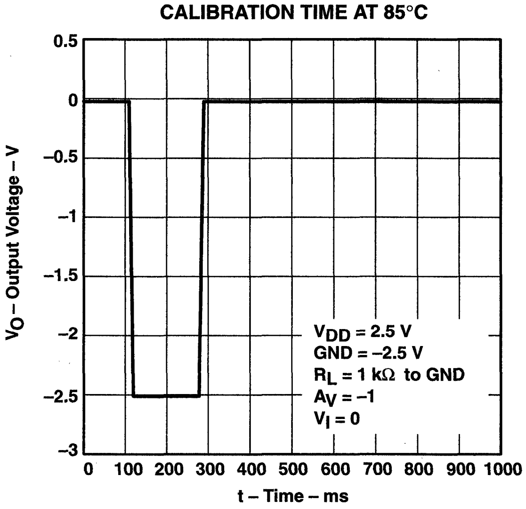


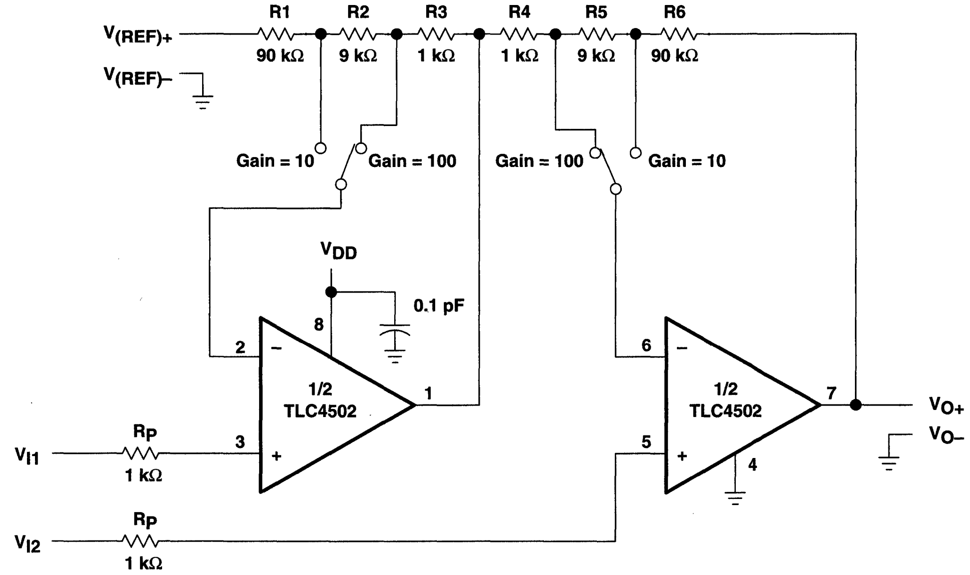
Figure 32

APPLICATION INFORMATION

- The TLC4502 is designed to operate with only a single 5-V power supply, have true differential inputs, and remain in the linear mode with an input common-mode voltage of 0.
- The TLC4502 has a standard dual-amplifier pinout allowing for easy design upgrades.
- Large differential input voltages can be easily accommodated and, as input differential-voltage protection diodes are not needed, no large input currents result from large differential input voltage. Protection should be provided to prevent the input voltages from going negative more than –0.3 V at 25°C. An input clamp diode with a resistor to the device input terminal can be used for this purpose.
- For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor can be used from the output of the amplifier to ground. This increases the class-A bias current and prevents crossover distortion. Where the load is directly coupled, for example dc applications, there is no crossover distortion.
- Capacitive loads, which are applied directly to the output of the amplifier, reduce the loop stability margin. Values of 500 pF can be accommodated using the worst-case noninverting unity-gain connection. Resistive isolation should be considered when larger load capacitance must be driven by the amplifier.

The following typical application circuits emphasize operation on only a single power supply. When complementary power supplies are available, the TLC4502 can be used in all of the standard operational amplifier circuits. In general, introducing a pseudo-ground (a bias voltage of $V_I/2$ like that generated by the TLE2426) allows operation above and below this value in a single-supply system. Many application circuits are shown which take advantage of the wide common-mode input-voltage range of the TLC4502, which includes ground. In most cases, input biasing is not required and input voltages that range to ground can easily be accommodated.

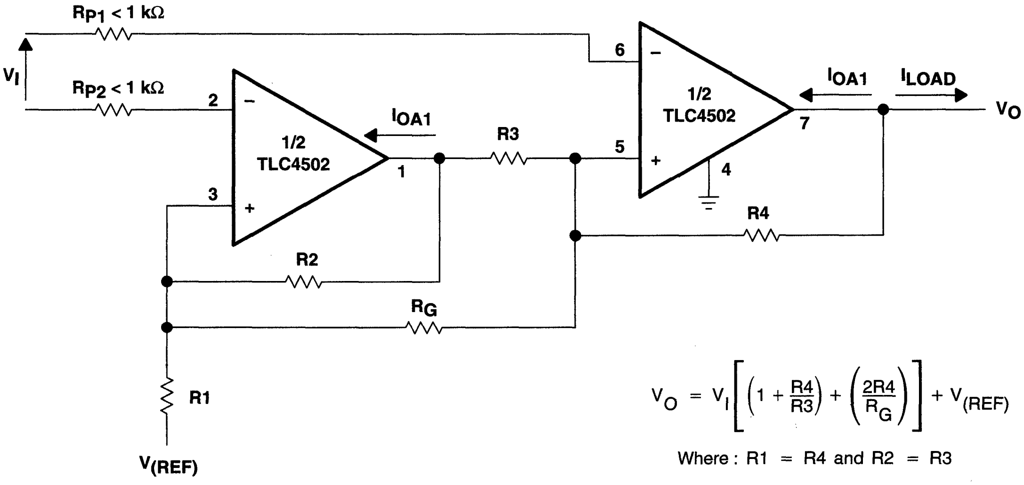
APPLICATION INFORMATION



(Gain = 10) $V_O = \left(V_{I1} - V_{I2}\right)\left(1 + \frac{R6}{R4 + R5}\right) + V_{(REF)}$ Where R1 = R6, R2 = R5, and R3 = R4

(Gain = 100) $V_O = \left(V_{I1} - V_{I2}\right)\left(1 + \frac{R5 + R6}{R4}\right) + V_{(REF)}$ Where R1 = R6, R2 = R5, and R3 = R4

Figure 33. Single-Supply Programmable Instrumentation Amplifier Circuit

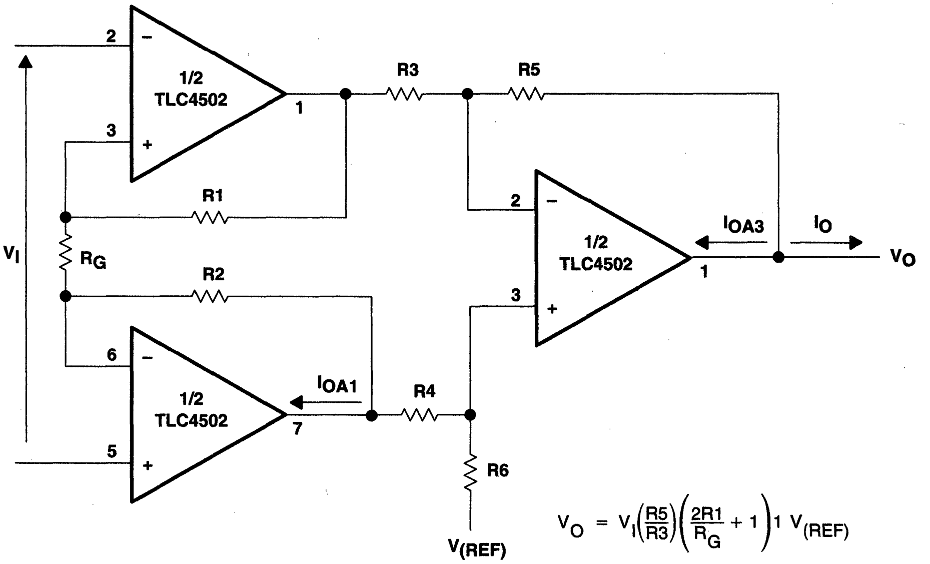


$$V_O = V_I\left[\left(1 + \frac{R4}{R3}\right) + \left(\frac{2R4}{R_G}\right)\right] + V_{(REF)}$$

Where : R1 = R4 and R2 = R3

Figure 34. Two Operational-Amplifier Instrumentation Amplifier Circuit

APPLICATION INFORMATION



$$V_O = V_I\left(\frac{R5}{R3}\right)\left(\frac{2R1}{R_G} + 1\right)1\ V_{(REF)}$$

Where : R1 = R2, R3 = R4, and R5 = R6

Figure 35. Three Operational-Amplifier Instrumentation Amplifier Circuit

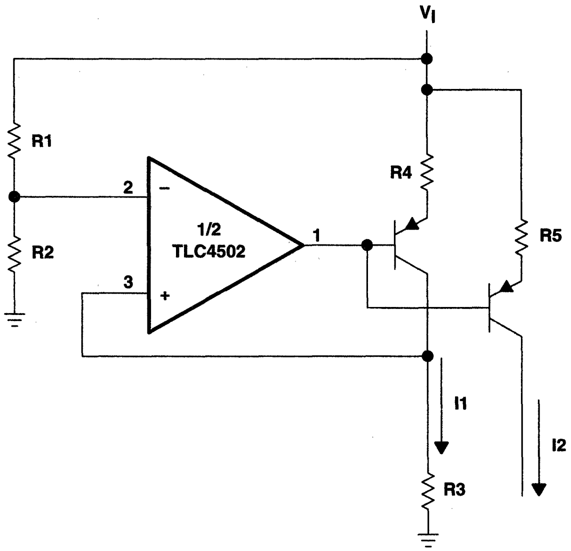


Figure 36. Fixed Current-Source Circuit

APPLICATION INFORMATION

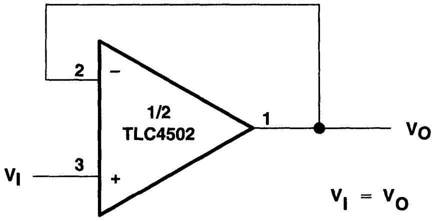


Figure 37. Voltage-Follower Circuit

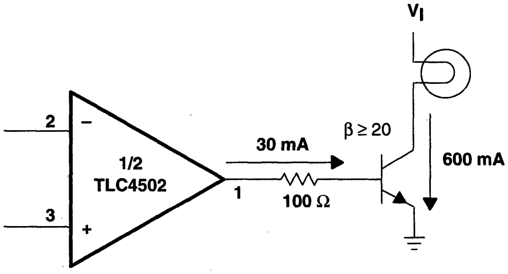


Figure 38. Lamp-Driver Circuit

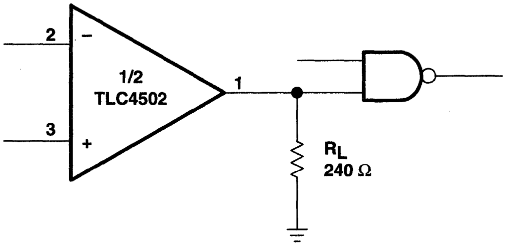


Figure 39. TTL-Driver Circuit

APPLICATION INFORMATION

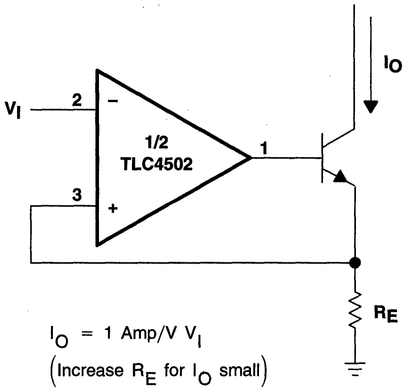


Figure 40. High-Compliance Current-Sink Circuit

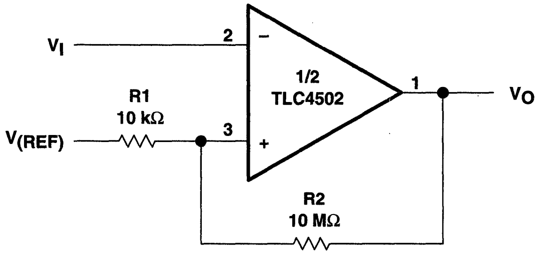


Figure 41. Comparator With Hysteresis Circuit

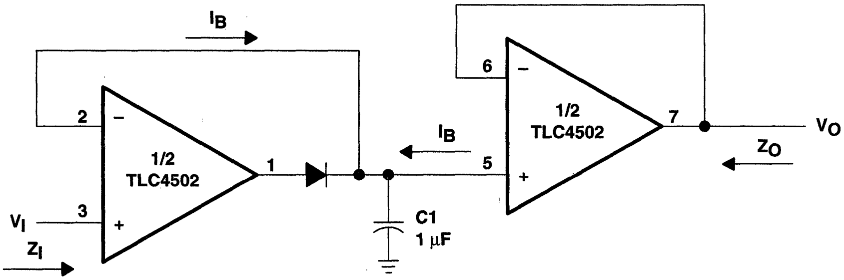


Figure 42. Low-Drift Detector Circuit

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as shown in the following example.

Example: **TLE** **2022** **PW** **LE**

Prefix

MUST CONTAIN TWO OR THREE LETTERS

TL, TLE	TI Linear Products
TLC	TI Linear Silicon-Gate CMOS Products

STANDARD SECOND-SOURCE PREFIXES

AD	Analog Devices
LF, LM, or LP	National
LT	Linear Technology
MC	Motorola
NE, SA, or SE	Signetics
OP	PMI
RC, RM, or RV	Raytheon
uA	Fairchild/National

Unique Circuit Description Including Temperature Range

MUST CONTAIN TWO OR MORE CHARACTERS
(from individual data sheets)

Examples:		
	10	34070
	592	1451AC
	7757	2217-285

Package

MUST CONTAIN ONE, TWO, OR THREE LETTERS

D, DB, DBV, DW, DWP, FK, J, JG, N, NE, P, PW, U, W
(from pin-connection diagrams on individual data sheet)

Available Taped and Reeled or Left-Ended Taped and Reeled

R – Available Taped and Reeled
LE – Available Only Left-Ended Taped and Reeled

ORDERING INSTRUCTIONS

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (J, JG, N, NE, P)
- A-Channel Antistatic or Conductive Plastic Tubing

Small Outline (D, DW, DWP)
- Tape and Reel
- Antistatic or Conductive Plastic Tubing

Shrink Small Outline (DB, DBV)
- Tape and Reel

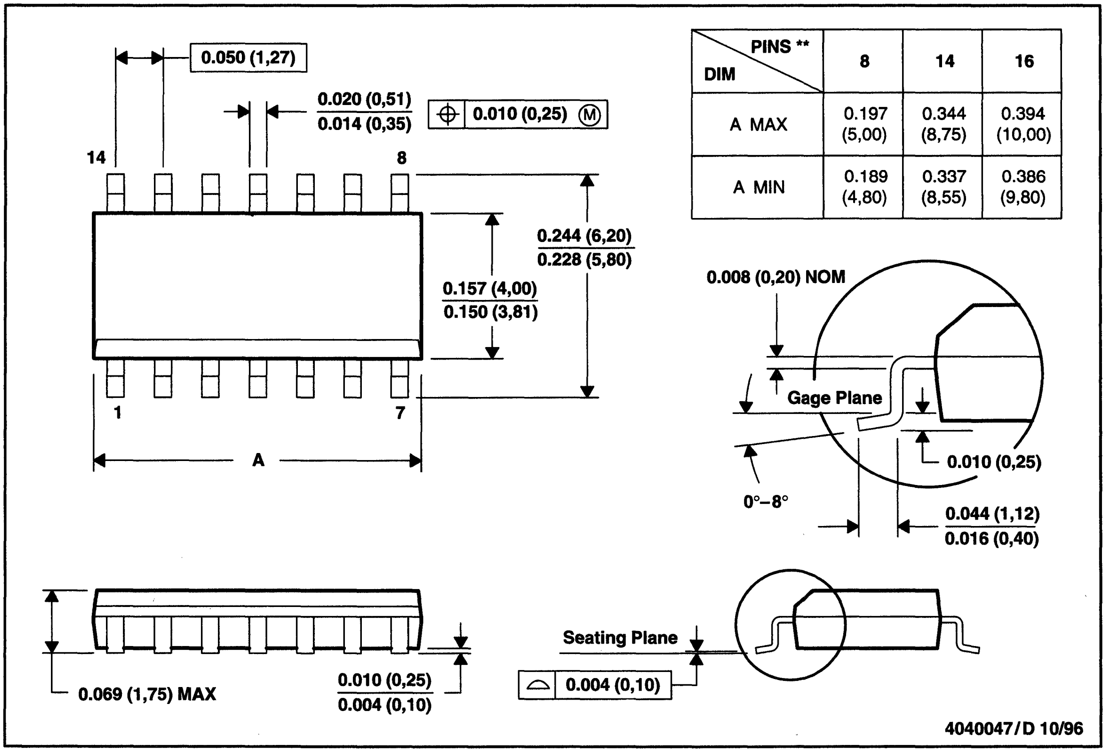
Thin Shrink Small Outline (PW)
- Tape and Reel

Chip Carriers (FK)
- Antistatic or Conductive Plastic Tubing

Flat (U, W)
- Milton Ross Carriers

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

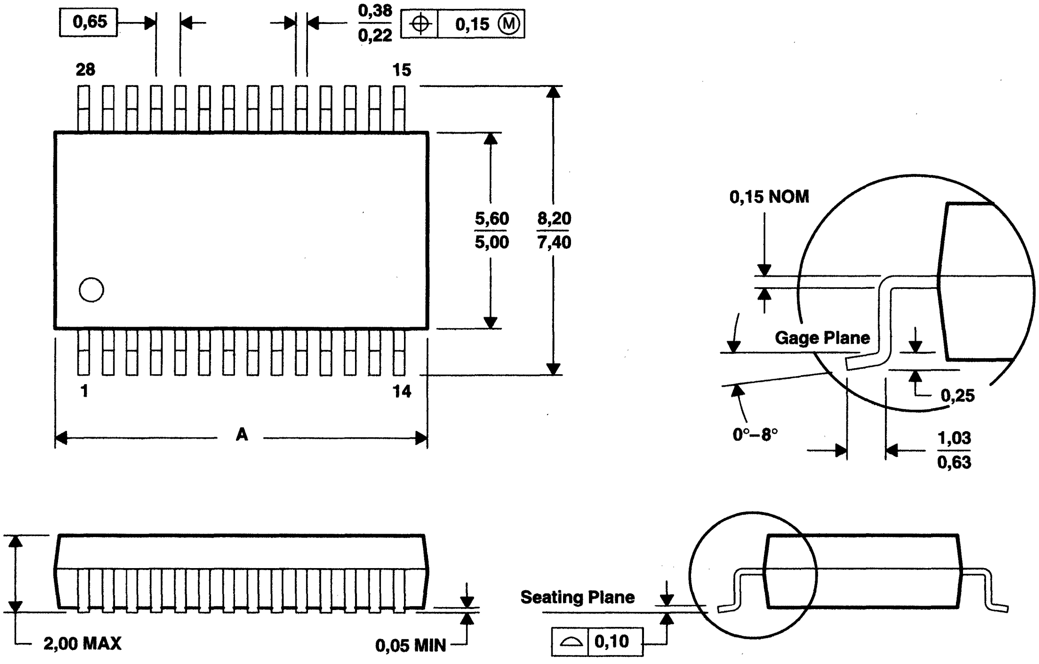


PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

28 PIN SHOWN

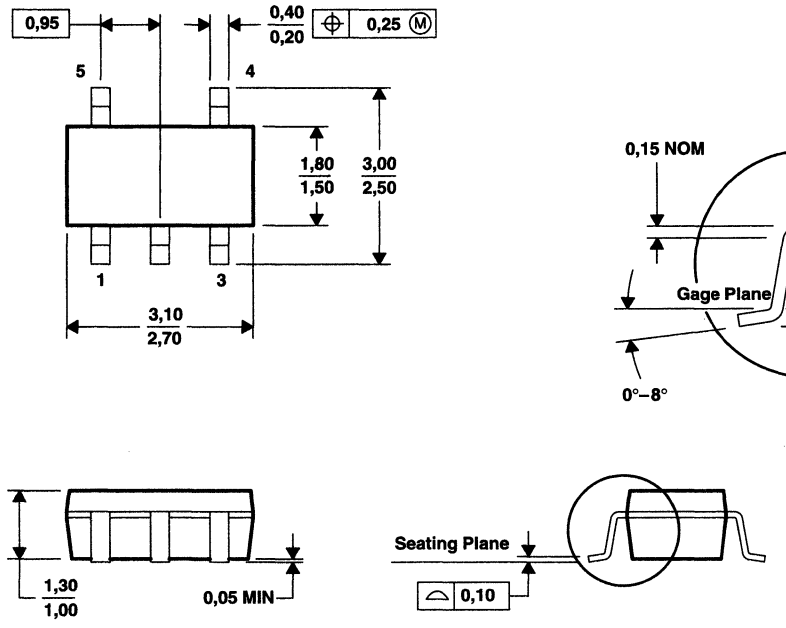


PINS ** DIM	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

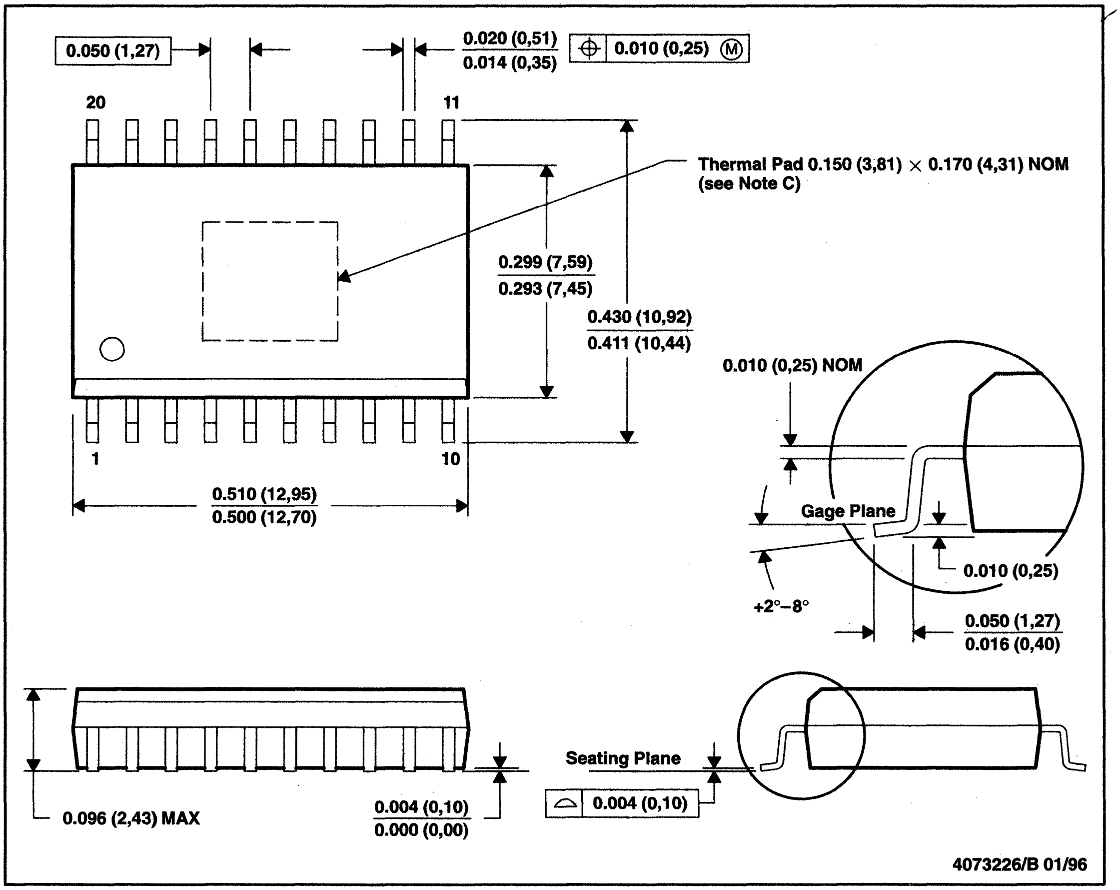
DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



4073253-4/B 11/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

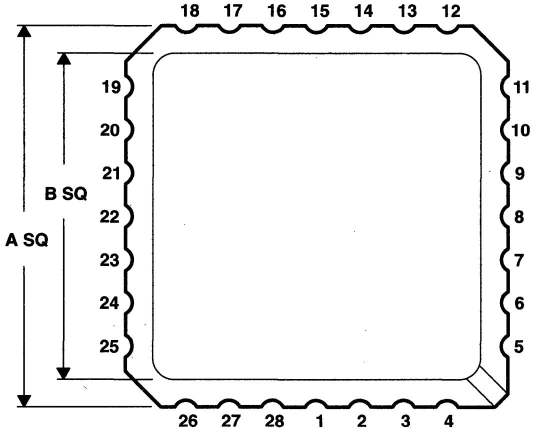
DWP (R-PDSO-G20) **PLASTIC SMALL-OUTLINE PACKAGE**



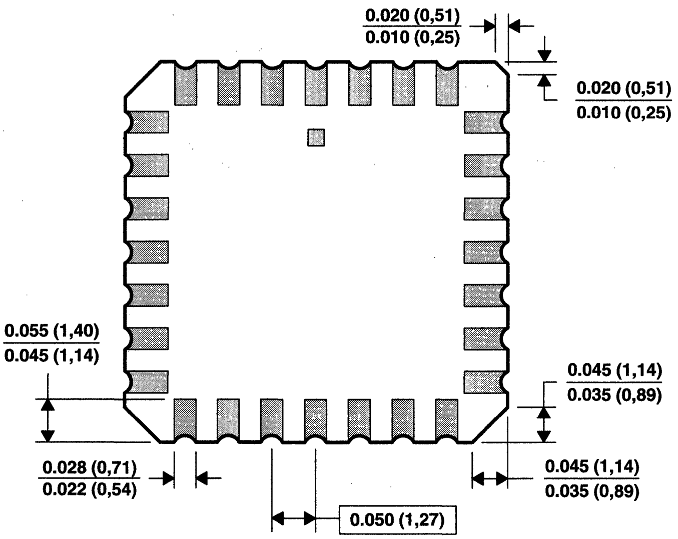
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This solderable pad is electrically and thermally connected to the backside of the die and leads 1, 10, 11 and 20.

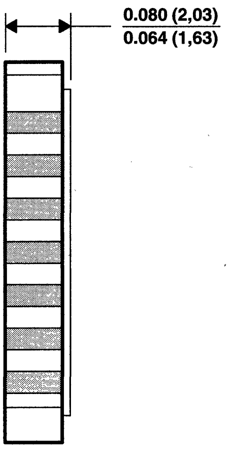
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



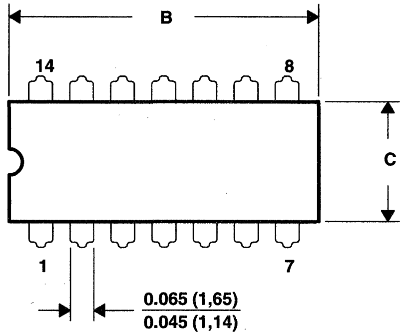


4040140/D 10/96

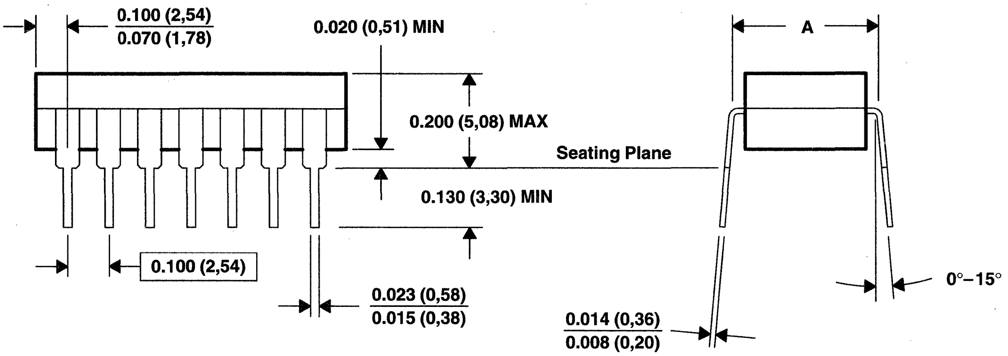
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

J (R-GDIP-T**) CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



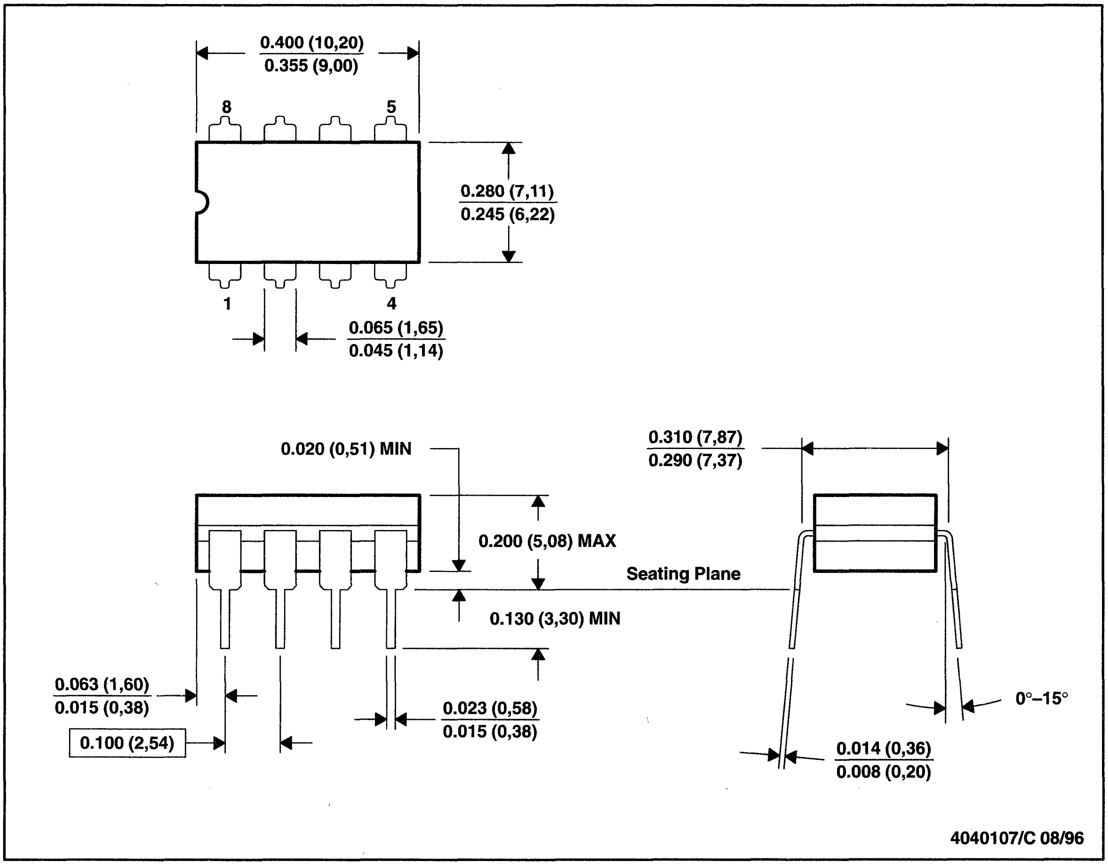
DIM \ PINS **	14	16	18	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)



4040083/C 08/96

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, and GDIP1-T20

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**

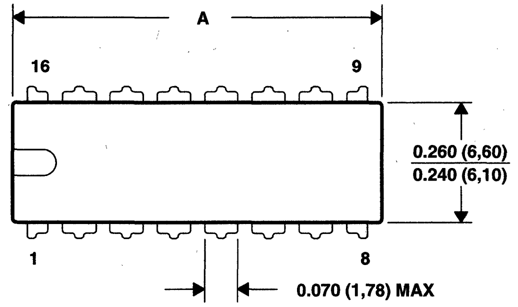


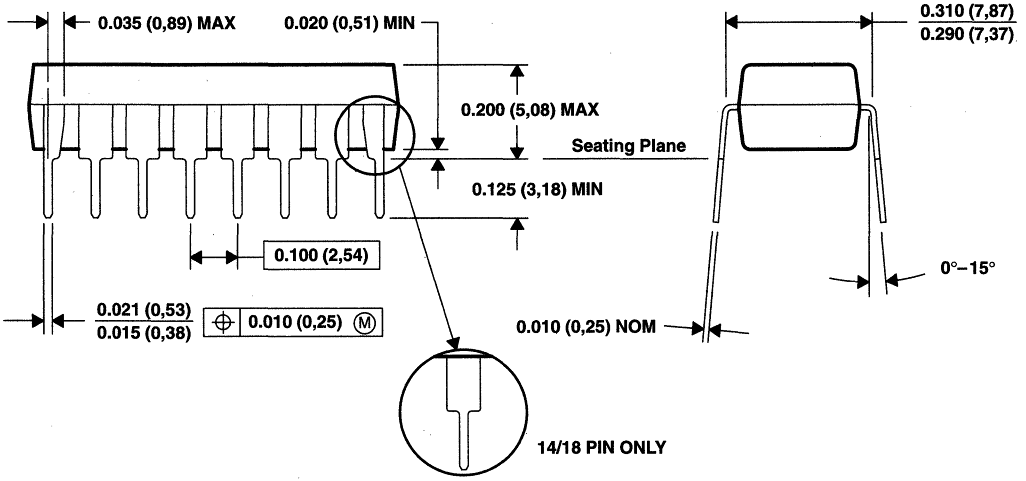
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL-STD-1835 GDIP1-T8

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



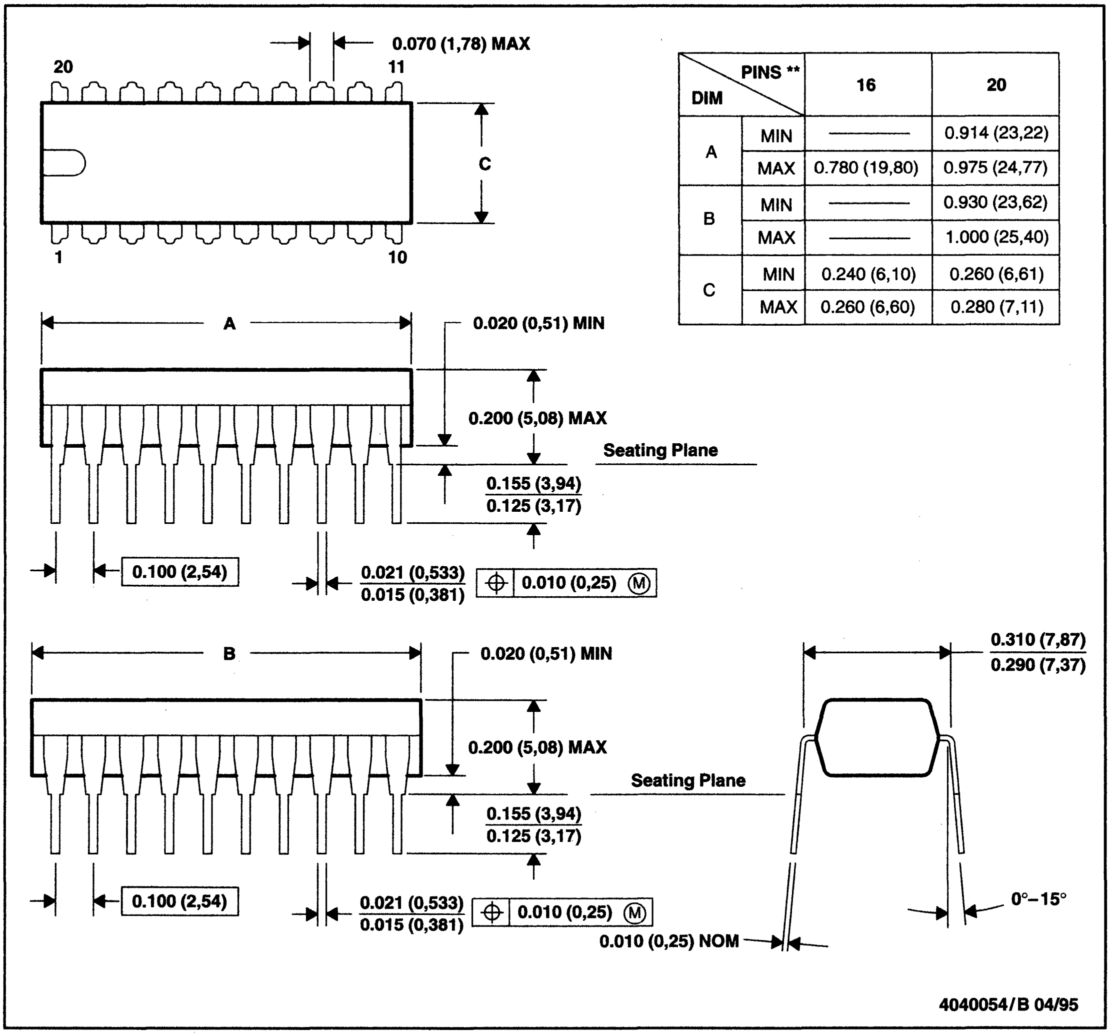


4040049/C 08/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

NE (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

20 PIN SHOWN

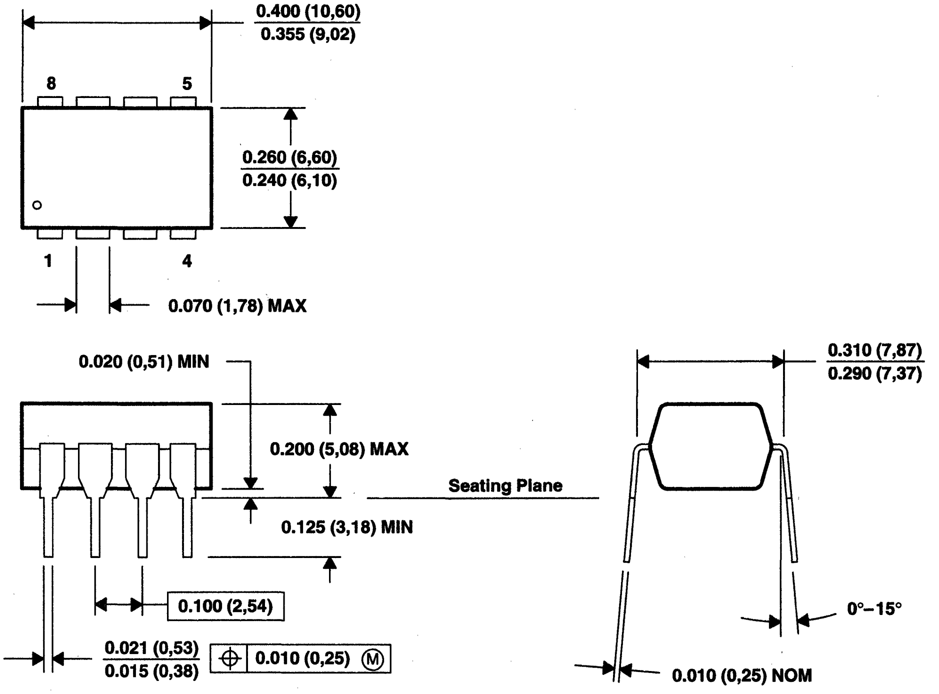


DIM	PINS **	16	20
A	MIN	———	0.914 (23,22)
	MAX	0.780 (19,80)	0.975 (24,77)
B	MIN	———	0.930 (23,62)
	MAX	———	1.000 (25,40)
C	MIN	0.240 (6,10)	0.260 (6,61)
	MAX	0.260 (6,60)	0.280 (7,11)

4040054/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (16 pin only)

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

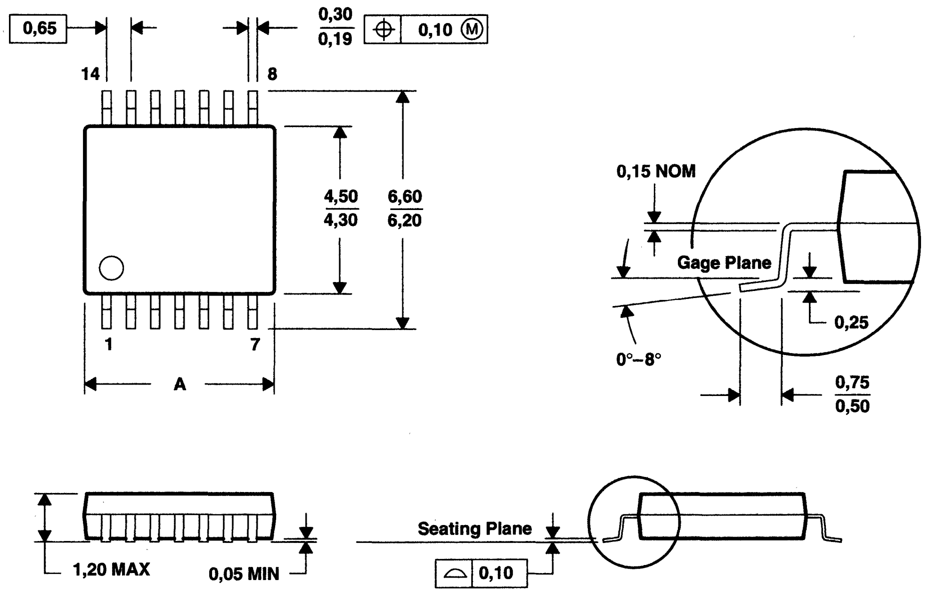


4040082/B 03/95

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

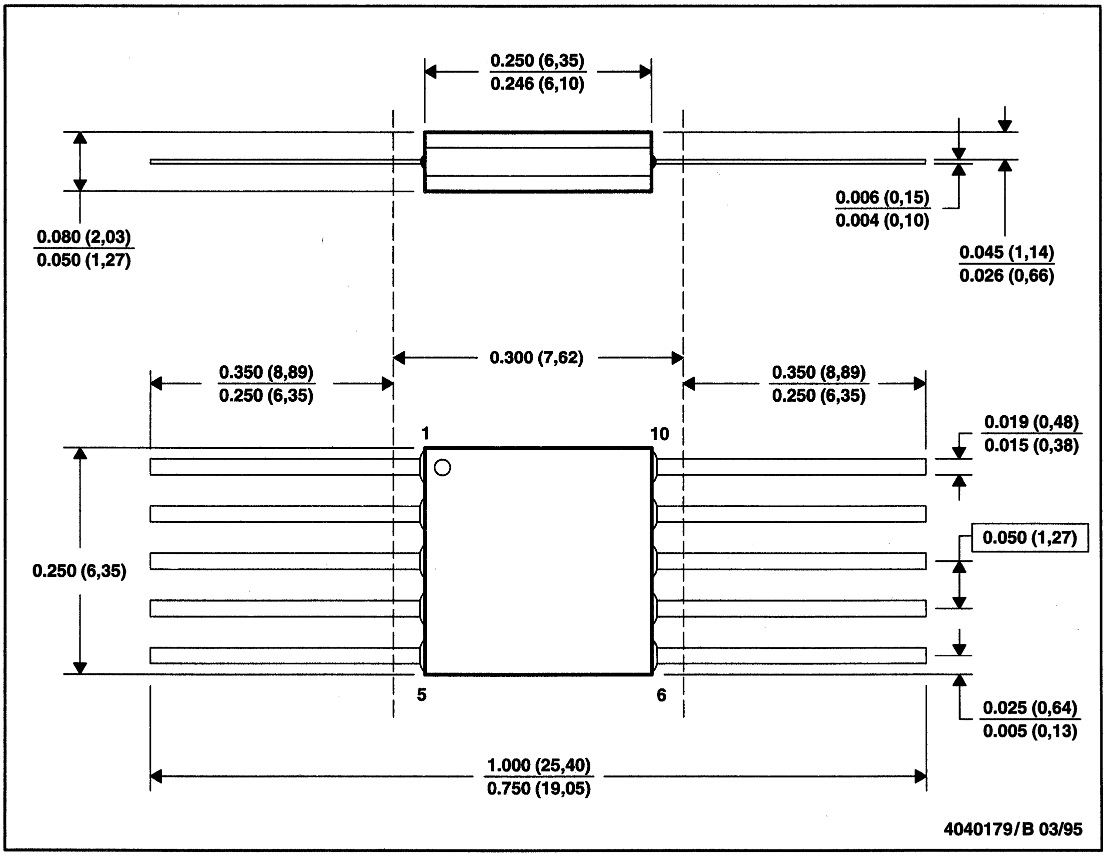


PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/E 08/96

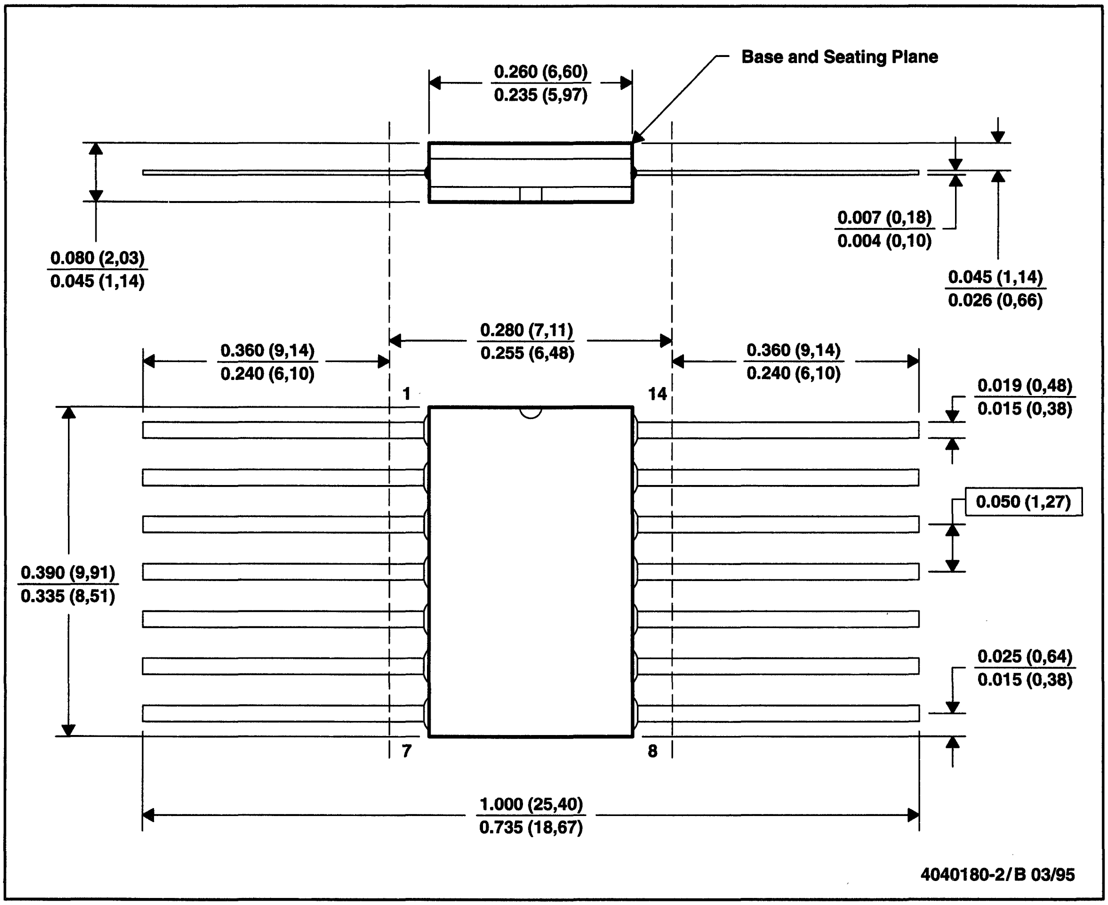
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

U (S-GDFP-F10) **CERAMIC DUAL FLATPACK**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

NOTES

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Japan

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Korea

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