# Boundary-Scan Logic IEEE Std 1149.1 (JTAG)

## 5-V and 3.3-V Bus-Interface and Scan-Support Products

## Data Book

1997

Advanced System Logic Products

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# Boundary-Scan Logic
# IEEE Std 1149.1 (JTAG)
# Data Book

## *5-V and 3.3-V Bus-Interface and Scan-Support Products*

Printed on Recycled Paper

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## INTRODUCTION

Today's designs are based on increasingly complex integrated circuits, fine-pitch packaging, and very dense board layouts. These factors limit test access and greatly complicate traditional methods of functional and in-circuit testing. The IEEE 1149.1 (JTAG) boundary-scan test standard was created to address this issue. Texas Instruments (TI) has taken a leading role in the industry in supplying silicon products that integrate IEEE 1149.1 boundary-scan test features.

TI presents the 1997 Boundary-Scan Logic IEEE Std 1149.1 (JTAG) Data Book. Included in this issue is the broadest range of silicon solutions for system-level test in the industry.

- Popular BiCMOS (BCT) and advanced BiCMOS (ABT) octal buffers/transceivers
- A full family of ABT/ABTH Widebus™ (18- and 20-bit) transceivers and universal bus transceivers (UBT™)
- The industry's first 3.3-V boundary-scan logic products, LVTH Widebus (18- and 20-bit) transceivers and UBTs
- A family of scan-support functions for controlling the test bus, adapting the test bus to backplane/multidrop configuration, and managing multiple scan paths

Features of the boundary-scan logic family include:

- Compatibility with IEEE Std 1149.1-1990 (JTAG) boundary-scan architecture
- Under 6-ns maximum propagation delays
- Bus-hold and series-resistor options
- EIAJ TSSOP, JEDEC SSOP, and EIAJ TQFP fine-pitch surface-mount packaging
- 18-bit and 20-bit UBT architectures

Most of the products in this data book are available in production quantities. Please contact your TI representative or local authorized distributor for details on any of these devices. Information on products not yet available in production quantities is presented in this data book as Product Preview. Contact the TI Semiconductor Product Information Center at (972) 644-5580 to learn more about plans for these devices.

The data book also contains other useful sections, including mechanical data and technical information.

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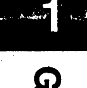



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## INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

### operating conditions and characteristics (in sequence by letter symbols)

$C_i$ **Input capacitance**
The internal capacitance at an input of the device

$C_{io}$ **Input/output capacitance**
Input-to-output internal capacitance; transcapacitance

$C_o$ **Output capacitance**
The internal capacitance at an output of the device

$C_{pd}$ **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):
$P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

$f_{max}$ **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

$I_{CC}$ **Supply current**
The current into* the $V_{CC}$ supply terminal of an integrated circuit

$\Delta I_{CC}$ **Supply current change**
The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$

$I_{CEX}$ **Output high leakage current**
The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_O = 5.5$ V

$I_{I(hold)}$ **Input hold current**
Input current that holds the input at the previous state when the driving device goes to a high-impedance state

$I_{IH}$ **High-level input current**
The current into* an input when a high-level voltage is applied to that input

$I_{IL}$ **Low-level input current**
The current into* an input when a low-level voltage is applied to that input

$I_{off}$ **Input/output power-off leakage current**
The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and $V_{CC} = 0$ V

$I_{OH}$ **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, establishes a high level at the output

*Current out of a terminal is given as a negative value.

$I_{OL}$ **Low-level output current**

The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output

$I_{OZPU/PD}$ **Off-state (high-impedance-state) output current (of a 3-state output)**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, establishes the high-impedance state at the output

$t_a$ **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output

$t_c$ **Clock cycle time**

Clock cycle time is $1/f_{max}$.

$t_{dis}$ **Disable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or $t_{PLZ}$. Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

$t_{en}$ **Enable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or $t_{PZL}$. Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

$t_h$ **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

$t_{pd}$ **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or $t_{PLH}$)

$t_{PHL}$ **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

$t_{PHZ}$ **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

*Current out of a terminal is given as a negative value.

$t_{PLH}$ **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

$t_{PLZ}$ **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

$t_{PZH}$ **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

$t_{PZL}$ **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

$t_{sk(o)}$ **Output Skew**

The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching output. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

$t_{su}$ **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

$t_w$ **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

$V_{IH}$ **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

$V_{IL}$ **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

$V_{OH}$ **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output

$V_{OL}$ **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output

$V_{IT+}$ **Positive-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, $V_{IT-}$

$V_{IT-}$ **Negative-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, $V_{IT+}$

The following symbols are used in function tables on TI data sheets:

| Symbol | | Meaning |
|---|---|---|
| H | = | high level (steady state) |
| L | = | low level (steady state) |
| ↑ | = | transition from low to high level |
| ↓ | = | transition from high to low level |
| ⟶ | = | value/level or resulting value/level is routed to indicated destination |
| ↶ | = | value/level is re-entered |
| X | = | irrelevant (any input, including transitions) |
| Z | = | off (high-impedance) state of a 3-state output |
| a . . . h | = | the level of steady-state inputs A through H, respectively |
| $Q_0$ | = | level of Q before the indicated steady-state input conditions were established |
| $\overline{Q}_0$ | = | complement of $Q_0$ or level of $\overline{Q}$ before the indicated steady-state input conditions were established |
| $Q_n$ | = | level of Q before the most recent active transition indicated by ↓ or ↑ |
| _⊓_ | = | one high-level pulse |
| ‾⊔‾ | = | one low-level pulse |
| Toggle | = | each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑ |

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, $Q_0$, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, _⊓_ or ‾⊔‾, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

# EXPLANATION OF FUNCTION TABLES

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register.

**FUNCTION TABLE**

| INPUTS | | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLEAR | MODE | | CLOCK | SERIAL | | PARALLEL | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| | S1 | S0 | | LEFT | RIGHT | A | B | C | D | | | | |
| L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| H | X | X | L | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | H | H | ↑ | X | X | a | b | c | d | a | b | c | d |
| H | L | H | ↑ | X | H | H | H | H | H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | L | H | ↑ | X | L | L | L | L | L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | H | L | ↑ | H | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | H |
| H | H | L | ↑ | L | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | L |
| H | L | L | X | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A is at output $Q_A$, data entered at B is at $Q_B$, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at $Q_A$ is now at $Q_B$, the previous levels of $Q_B$ and $Q_C$ are now at $Q_C$ and $Q_D$, respectively, and the data previously at $Q_D$ is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at $Q_B$ is now at $Q_A$, the previous levels of $Q_C$ and $Q_D$ are now at $Q_B$ and $Q_C$, respectively, and the data previously at $Q_A$ is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

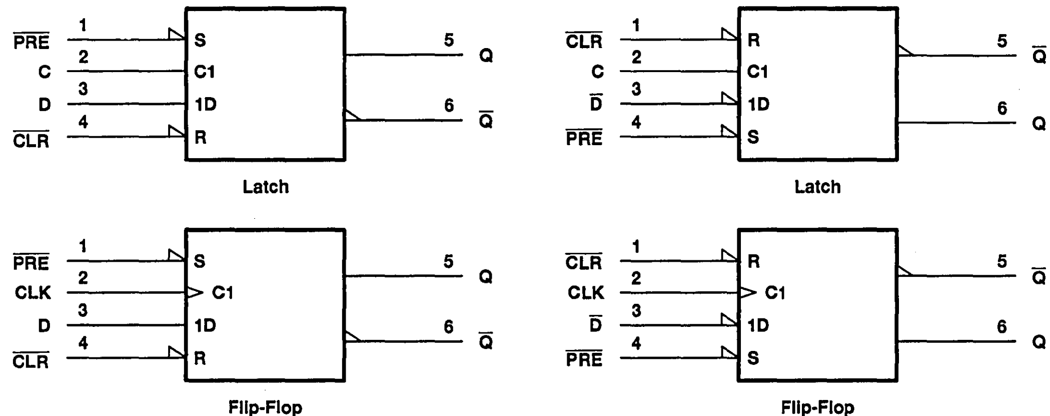
The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

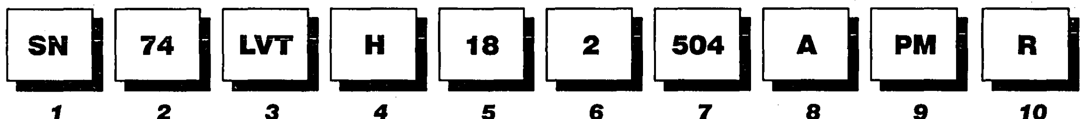
The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.




The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊵) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

***Example:***




### 1 Standard Prefix

Example: SNJ – Conforms to MIL-PRF-38535 (QML)

### 2 Military (54) or Commercial (74)

### 3 Family

Example: Blank – Transistor-Transistor Logic
ABT – Advanced BiCMOS Technology
ABTE – Advanced BiCMOS Technology/ Enhanced Transceiver Logic
AC/ACT – Advanced CMOS Logic
AHC/AHCT – Advanced High-Speed CMOS Logic
ALS – Advanced Low-Power Schottky Logic
AS – Advanced Schottky Logic
ALVC – Advanced Low-Voltage CMOS Technology
BCT – BiCMOS Bus-Interface Technology
CBT – Crossbar Technology
CDC – Clock-Distribution Circuits
F – F Logic
FB – Backplane Transceiver Logic/Futurebus+
GTL – Gunning-Transceiver Logic
HC/HCT – High-Speed CMOS Logic
LS – Low-Power Schottky Logic
LV – Low-Voltage HCMOS Technology
LVC – Low-Voltage CMOS Technology
LVT – Low-Voltage BiCMOS Technology
S – Schottky Logic
SSTL – Series-Stub Terminated Logic

### 4 Special Features

Example: Blank = No Special Features
D – Level-Shifting Diode (CBTD)
H – Bus Hold (ALVCH)
R – Damping Resistor on Inputs/Outputs (LVCR)
S – Schottky Clamping Diode (CBTS)
U – Unbuffered Output (AHCU)

### 5 Bit Width

Example: Blank = Gates, MSI, and Octals
1G – MicroGate (Single Gate)
8 – Octal IEEE 1149.1 (JTAG)
16 – Widebus™ (16, 18, and 20 Bit)
18 – Widebus™ IEEE 1149.1 (JTAG)
32 – Widebus+™ (32 and 36 Bit)

### 6 Options

Example: Blank = No Options
2 – Series-Damping Resistor on Outputs
4 – Level Shifter
25 – 25-Ω Line Driver

### 7 Function

Example: 244 – Noninverting Octal Buffer/Driver
374 – Octal D-Type Flip-Flop
573 – D-Type Transparent Latch
640 – Inverting Octal Transceiver

### 8 Device Revision

Example: Blank = No Revision
Letter Designator A–Z

### 9 Packages

Example: D, DW – Small-Outline Integrated Circuit (SOIC)
DB, DL – Shrink Small-Outline Package (SSOP)
DBB, DGV – Thin Very Small-Outline Package (TVSOP)
DBV – Small-Outline Transistor Package
DGG, PW – Thin Shrink Small-Outline Package (TSSOP)
FK – Leadless Ceramic Chip Carrier
FN – Plastic Leaded Chip Carrier
GB – Ceramic Pin Grid Array
HFP, HS, HT, HV – Ceramic Quad Flat Package
J, JT – Ceramic Dual-In-Line Package
N, NT – Plastic Dual-In-Line Package (DIP)
PH, PQ, RC – Plastic Quad Flat Package
PAG, PAH, PCA, PCB, PM, PN, PZ – Plastic Thin Quad Flat Package
W, WA, WD – Ceramic Flat Package

### 10 Tape and Reel

Example: LE – Left Embossed (Required for DB and PW Packages)
R – Standard (Required for DGG, DBB, DGV, and DBV; Optional for D, DL, and DW Packages)

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using the following equation:

$$T_J = R_{\theta JA} \times P_T + T_A$$

where:

$T_J$ = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
$P_T$ = total power dissipation of the device
$T_A$ = free-air temperature

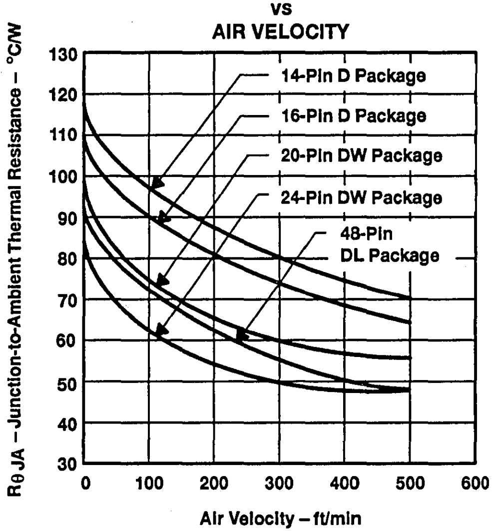



Figure 1

Derating curves for 56-pin thin shrink small-outline package are shown in Figure 2, 56-pin thin shrink small-outline package are shown in Figure 3, 64-pin thin quad flat package are shown in Figure 4, and 24-pin thin shrink small-outline package are shown in Figure 5.

## DERATING CURVES

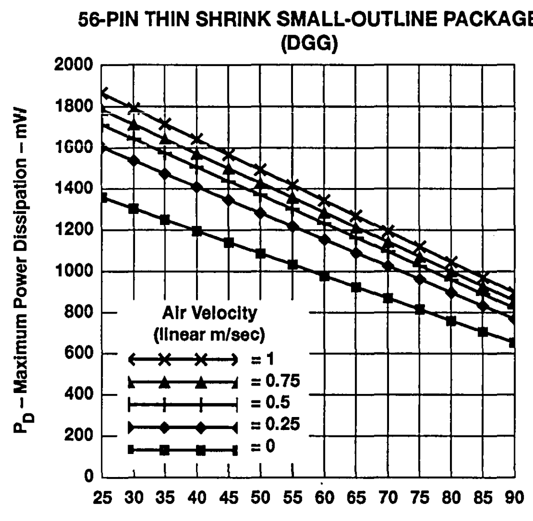



Figure 2

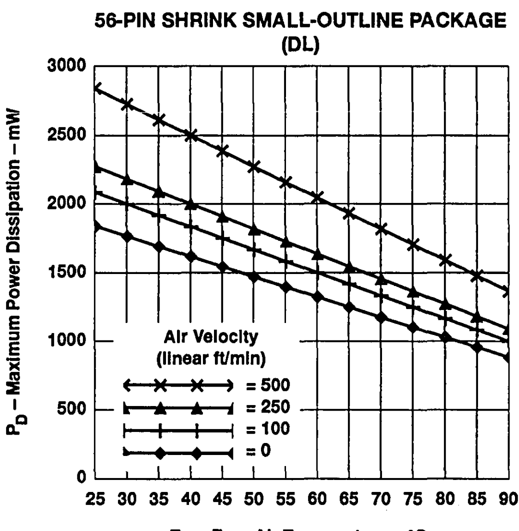



Figure 3

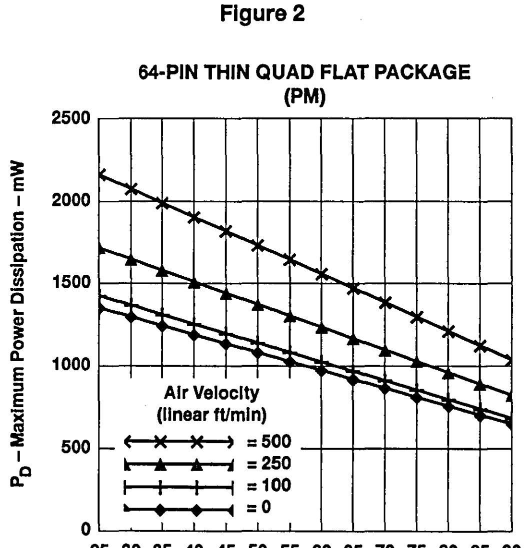



Figure 4

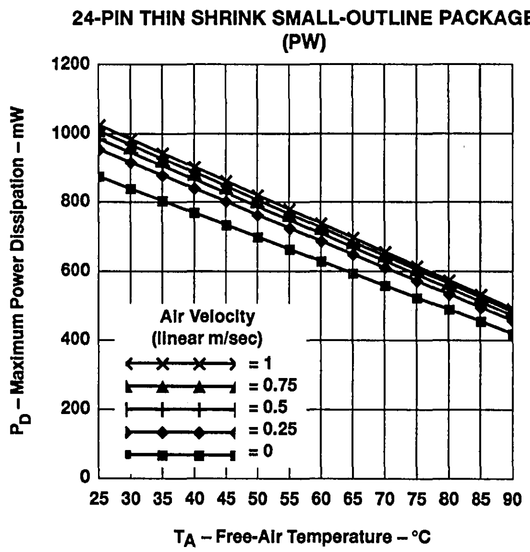



Figure 5

# IEEE 1149.1 (JTAG) BOUNDARY-SCAN LOGIC

## IEEE 1149.1 (JTAG) Octal Bus Interface

| DESCRIPTION | NO. OF BITS | OUTPUT | TYPE | TECHNOLOGY | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | ABT | BCT | LVT | ACT | OTHER |
| Inverting Buffers/Drivers | 8 | 3S | '8240 | | ✔ | | | |
| Noninverting Buffers/Drivers | 8 | 3S | '8244 | | ✔ | | | |
| Transceivers | 8 | 3S | '8245 | ✔ | ✔ | | | |
| Registered Transceivers | 8 | 3S | '8543 | ✔ | | | | |
| | | | '8646 | ✔ | | | | |
| | | | '8652 | ✔ | | | | |
| | | | '8952 | ✔ | | | | |
| D-Type Transparent Latches | 8 | 3S | '8373 | | ✔ | | | |
| D-Type Flip-Flops | 8 | 3S | '8374 | | ✔ | | | |

3S = 3-State
✔ Product available in technology indicated + New product planned in technology indicated

## IEEE 1149.1 (JTAG) Widebus™ With Dual-Sided Terminals

| DESCRIPTION | NO. OF BITS | OUTPUT | TYPE | TECHNOLOGY | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | ABT | BCT | LVT | ACT | OTHER |
| Noninverting Transceivers | 18 | 3S | '18245 | ✔ | | + | | + Bus Hold |
| Inverting Transceivers | 18 | 3S | '18640 | ✔ | | + | | + Bus Hold |
| Noninverting Transceivers With Series Resistors on B Port | 18 | 3S | '182245 | | | + | | + Bus Hold |
| Inverting Transceivers With Series Resistors on B Port | 18 | 3S | '182640 | | | + | | + Bus Hold |
| Universal Bus Transceivers (UBT™) | 18 | 3S | '18512 | | | + | | + Bus Hold |
| | | | '18516 | | | + | | + Bus Hold |
| | 20 | 3S | '18514 | | | + | | + Bus Hold |
| Universal Bus Transceivers (UBT™) With Series Resistors on B Port | 18 | 3S | '182512 | | | + | | + Bus Hold |
| | | | '182516 | | | + | | + Bus Hold |
| | 20 | 3S | '182514 | | | + | | + Bus Hold |

3S = 3-State
✔ Product available in technology indicated + New product planned in technology indicated

# IEEE 1149.1 (JTAG) BOUNDARY-SCAN LOGIC

## IEEE 1149.1 (JTAG) Widebus™ With Quad-Sided Terminals

| DESCRIPTION | NO. OF BITS | OUTPUT | TYPE | TECHNOLOGY | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | ABT | BCT | LVT | ACT | OTHER |
| Registered Transceivers | 18 | 3S | '18646 | ✔ | | + | | ✔ Bus Hold |
| | | | '18652 | ✔ | | + | | ✔ Bus Hold |
| Registered Transceivers With Series Resistors on B Port | 18 | 3S | '182646 | ✔ | | + | | ✔ Bus Hold |
| | | | '182652 | ✔ | | + | | ✔ Bus Hold |
| Universal Bus Transceivers (UBT™) | 18 | 3S | '18502 | ✔ | | ✔ | | ✔ Bus Hold |
| | 20 | 3S | '18504 | ✔ | | ✔ | | ✔ Bus Hold |
| Universal Bus Transceivers (UBT™) With Series Resistors on B Port | 18 | 3S | '182502 | ✔ | | ✔ | | ✔ Bus Hold |
| | 20 | 3S | '182504 | ✔ | | ✔ | | ✔ Bus Hold |

3S = 3-State
✔ Product available in technology indicated + New product planned in technology indicated

## IEEE 1149.1 (JTAG) Scan Support

| DESCRIPTION | TYPE | TECHNOLOGY | | | | |
|---|---|---|---|---|---|---|
| | | ABT | BCT | LVT | ACT | OTHER |
| Test Bus Controllers | '8980 | | | ✔ | | |
| | '8990 | | | | ✔ | |
| Digital Bus Monitors | '8994 | | | | ✔ | |
| Addressable Scan Port Devices | '8996 | ✔ | | | | |
| Scan-Path Linkers | '8997 | | | | ✔ | |
| Scan-Path Selectors | '8999 | | | | ✔ | |

3S = 3-State
✔ Product available in technology indicated + New product planned in technology indicated

General Information 1

SN54/74BCT Octals 2

SN54/74ABT Octals 3

SN54/74ABT Widebus™ With Dual-Sided Terminals 4

SN54/74ABT Widebus™ With Quad-Sided Terminals 5

SN54/74LVT Widebus™ With Dual-Sided Terminals 6

SN54/74LVT Widebus™ With Quad-Sided Terminals 7

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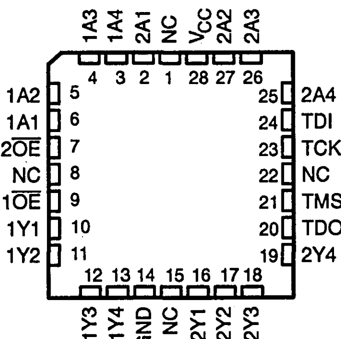
| 'BCT8244A | Scan Test Devices With Octal Buffers | 2–23 |
| 'BCT8245A | Scan Test Devices With Octal Bus Transceivers | 2–43 |
| 'BCT8373A | Scan Test Devices With Octal D-Type Latches | 2–65 |
| 'BCT8374A | Scan Test Devices With Octal D-Type Edge-Triggered Flip-Flops | 2–85 |

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Octal Test-Integrated Circuits**
- **Functionally Equivalent to 'F240 and 'BCT240 in the Normal-Function Mode**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Test Operation Synchronous to Test Access Port (TAP)**
- **Implement Optional Test Reset Signal by Recognizing a Double-High-Level Voltage (10 V) on TMS Pin**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP, and HIGHZ**
  - **Parallel-Signature Analysis at Inputs**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)**

**SN54BCT8240A . . . JT PACKAGE**
**SN74BCT8240A . . . DW OR NT PACKAGE**
**(TOP VIEW)**

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| $\overline{1OE}$ | 1 | 24 | $\overline{2OE}$ |
| 1Y1 | 2 | 23 | 1A1 |
| 1Y2 | 3 | 22 | 1A2 |
| 1Y3 | 4 | 21 | 1A3 |
| 1Y4 | 5 | 20 | 1A4 |
| GND | 6 | 19 | 2A1 |
| 2Y1 | 7 | 18 | $V_{CC}$ |
| 2Y2 | 8 | 17 | 2A2 |
| 2Y3 | 9 | 16 | 2A3 |
| 2Y4 | 10 | 15 | 2A4 |
| TDO | 11 | 14 | TDI |
| TMS | 12 | 13 | TCK |

**SN54BCT8240A . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'BCT8240A scan test devices with octal buffers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the 'F240 and 'BCT240 octal buffers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device terminals or to perform a self test on the boundary-test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal buffers.

In the test mode, the normal operation of the SCOPE™ octal buffers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary-scan test operations, as described in IEEE Standard 1149.1-1990.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

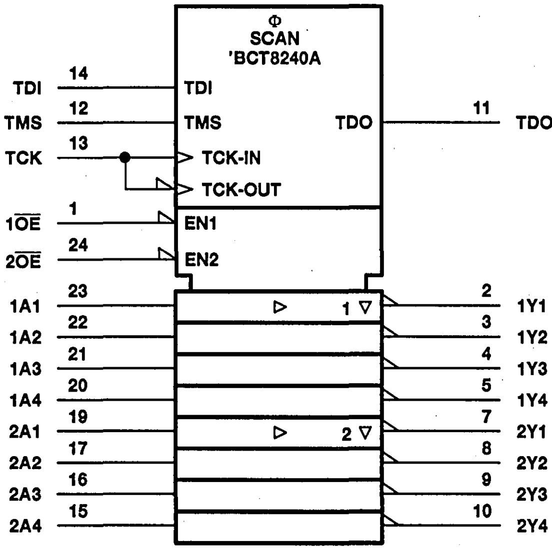
Four dedicated test terminals control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8240A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT8240A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(normal mode, each buffer)**

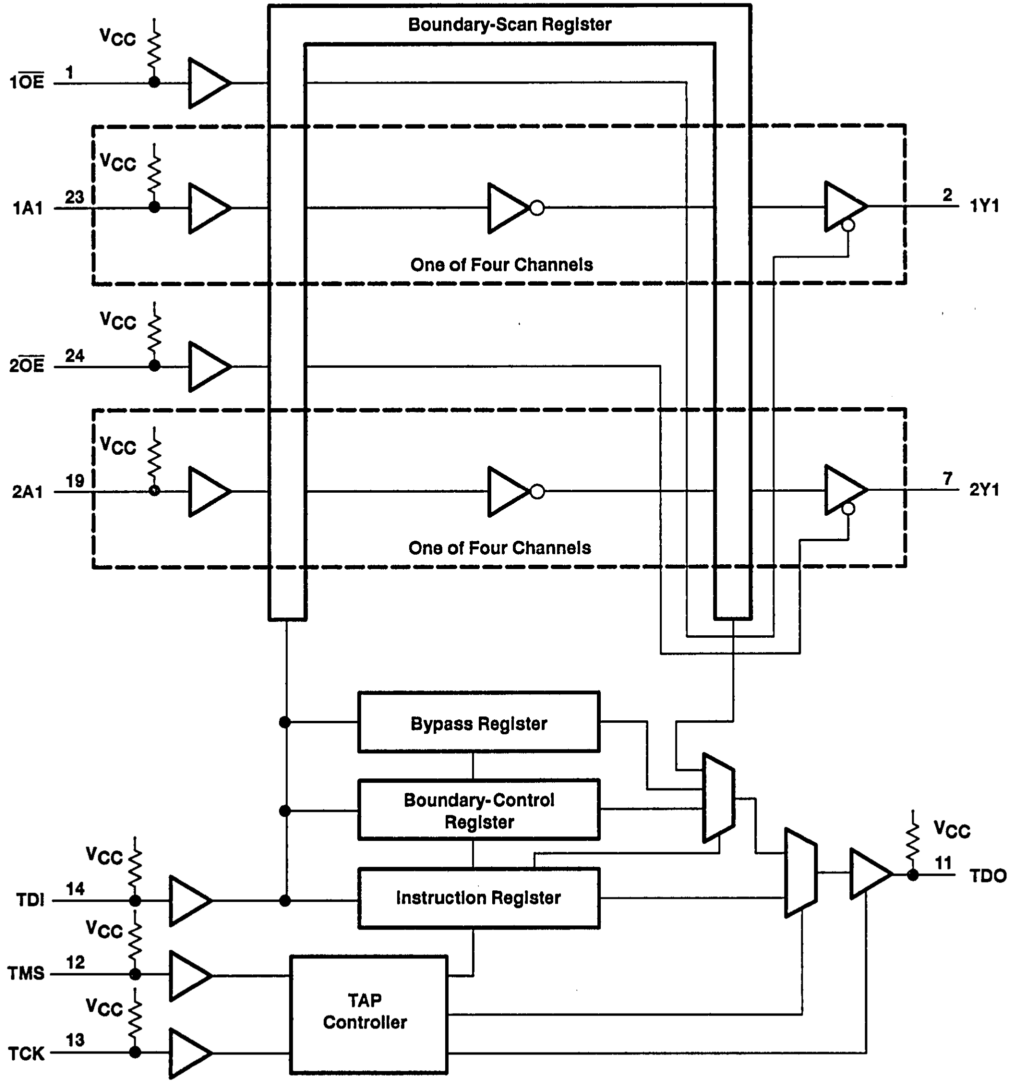
| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| H | X | Z |
| L | L | H |
| L | H | L |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

## functional block diagram




Pin numbers shown are for the DW, JT, and NT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A4, 2A1–2A4 | Normal-function data inputs. See function table for normal-mode logic. Internal pullups force these inputs to a high level if left unconnected. |
| GND | Ground |
| $1\overline{OE}$, $2\overline{OE}$ | Normal-function output-enable inputs. See function table for normal-mode logic. Internal pullups force these inputs to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. An internal pullup forces TCK to a high level if left unconnected. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. An internal pullup forces TDO to a high level when it is not active and is not driven from an external source. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP-controller states. An internal pullup forces TMS to a high level if left unconnected. TMS also provides the optional test reset signal of IEEE Standard 1149.1-1990. This is implemented by recognizing a third logic level, double high ($V_{IHH}$), at TMS. |
| $V_{CC}$ | Supply voltage |
| 1Y1–1Y4, 2Y1–2Y4 | Normal-function data outputs. See function table for normal-mode logic. |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus, or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK, and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and three test-data registers: an 18-bit boundary-scan register, a 2-bit boundary-control register, and a 1-bit bypass register.

Test-Logic-Reset
TMS = H
TMS = L
Run-Test/Idle
TMS = L
TMS = H
Select-DR-Scan
TMS = H
Select-IR-Scan
TMS = H
TMS = L
TMS = L
Capture-DR
TMS = H
TMS = H
Capture-IR
TMS = L
TMS = L
Shift-DR
TMS = L
Shift-IR
TMS = L
TMS = H
TMS = H
TMS = H
Exit1-DR
Exit1-IR
TMS = H
TMS = L
TMS = L
Pause-DR
TMS = L
Pause-IR
TMS = L
TMS = H
TMS = H
TMS = L
Exit2-DR
TMS = L
Exit2-IR
TMS = H
TMS = H
Update-DR
Update-IR
TMS = H
TMS = L
TMS = H
TMS = L

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register may be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuted.

For the 'BCT8240A, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. The boundary-control register is reset to the binary value 10, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic may be actively running a test or may be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected-data register may capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state.

For the 'BCT8240A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass register, any test register may be thought of as a serial-shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register may be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 2 lists the instructions supported by the 'BCT8240A. The even-parity feature specified for SCOPE™ devices is not supported in this device. Bit 7 of the instruction opcode is a don't-care bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR order of scan is shown in Figure 2.

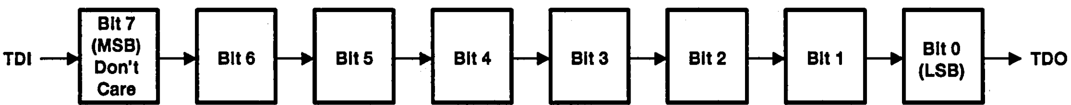



**Figure 2. Instruction Register Order of Scan**

## data-register description

### boundary-scan register

The boundary-scan register (BSR) is 18 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function output pin. The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output terminals, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input terminals.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR may change during Run-Test/Idle as determined by the current instruction. The contents of the BSR are not changed in Test-Logic-Reset.

The BSR order of scan is from TDI through bits 17–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

Table 1. Boundary-Scan Register Configuration

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 17 | $1\overline{OE}$ | 15 | 1A1 | 7 | 1Y1 |
| 16 | $2\overline{OE}$ | 14 | 1A2 | 6 | 1Y2 |
| — | — | 13 | 1A3 | 5 | 1Y3 |
| — | — | 12 | 1A4 | 4 | 1Y4 |
| — | — | 11 | 2A1 | 3 | 2Y1 |
| — | — | 10 | 2A2 | 2 | 2Y2 |
| — | — | 9 | 2A3 | 1 | 2Y3 |
| — | — | 8 | 2A4 | 0 | 2Y4 |

### boundary-control register

The boundary-control register (BCR) is two bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG and PSA. Table 3 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 10, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

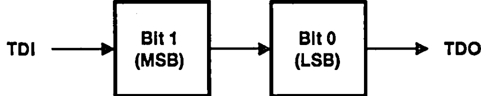



Figure 3. Boundary-Control Register Order of Scan

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

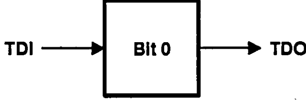



Figure 4. Bypass Register Order of Scan

## instruction-register opcode description

The instruction-register opcodes are shown in Table 2. The following descriptions detail the operation of each instruction.

Table 2. Instruction-Register Opcodes

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| X0000000 | EXTEST/INTEST | Boundary scan | Boundary scan | Test |
| X0000001 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| X0000011 | INTEST/EXTEST | Boundary scan | Boundary scan | Test |
| X0000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000110 | HIGHZ (TRIBYP) | Control boundary to high impedance | Bypass | Modified test |
| X0000111 | CLAMP (SETBYP) | Control boundary to 1/0 | Bypass | Test |
| X0001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0001001 | RUNT | Boundary run test | Bypass | Test |
| X0001010 | READBN | Boundary read | Boundary scan | Normal |
| X0001011 | READBT | Boundary read | Boundary scan | Test |
| X0001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| X0001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| X0001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| X0001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is a don't-care bit; X = don't care.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'BCT8240A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output terminals. The device operates in the test mode.

### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device output terminals are placed in the high-impedance state, the device input terminals remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output terminals. The device operates in the test mode.

**boundary run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The four test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, and simultaneous PSA and PRPG (PSA/PRPG).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches may be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device output terminals on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input terminals is not captured in the input BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

### boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 1–0, as shown in Table 3. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 3. Boundary-Control Register Opcodes**

| BINARY CODE BIT 1 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| 00 | Sample inputs/toggle outputs (TOPSIP) |
| 01 | Pseudo-random pattern generation/16-bit mode (PRPG) |
| 10 | Parallel-signature analysis/16-bit mode (PSA) |
| 11 | Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG) |

It should be noted, in general, that while the control input BSCs (bits 17–16) are not included in the sample, toggle, PSA, or PRPG algorithms, the output-enable BSCs (bits 17–16 of the BSR) do control the drive state (active or high impedance) of the selected device output terminals.

### sample inputs/toggle outputs (TOPSIP)

Data appearing at the device input terminals is captured in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the BSCs on each rising edge of TCK and then updated in the shadow latches and applied to the device output terminals on each falling edge of TCK. This data also is updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Figure 5 shows the 16-bit linear-feedback shift-register algorithm through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

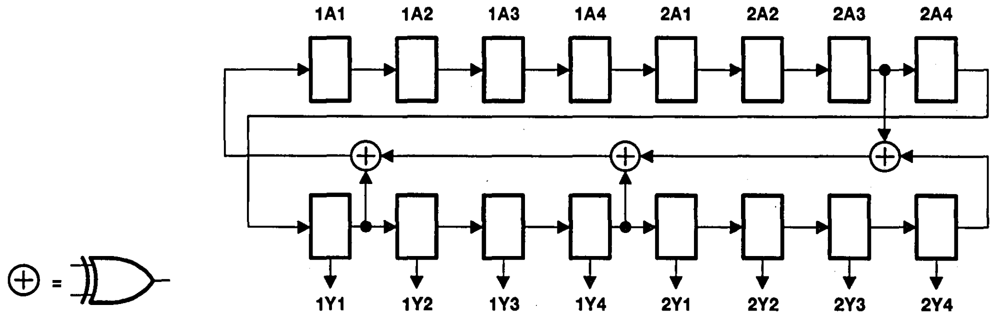



**Figure 5. 16-Bit PRPG Configuration**

### parallel-signature analysis (PSA)

Data appearing at the device input terminals is compressed into a 16-bit parallel signature in the shift-register elements of the BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the output BSCs remains constant and is applied to the device outputs. Figure 6 shows the 16-bit linear-feedback shift-register algorithm through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

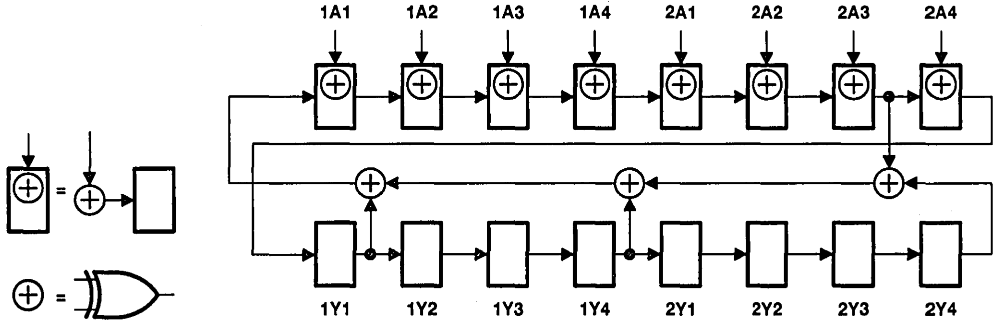



**Figure 6. 16-Bit PSA Configuration**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the device input terminals is compressed into an 8-bit parallel signature in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK. Figure 7 shows the 8-bit linear-feedback shift-register algorithm through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

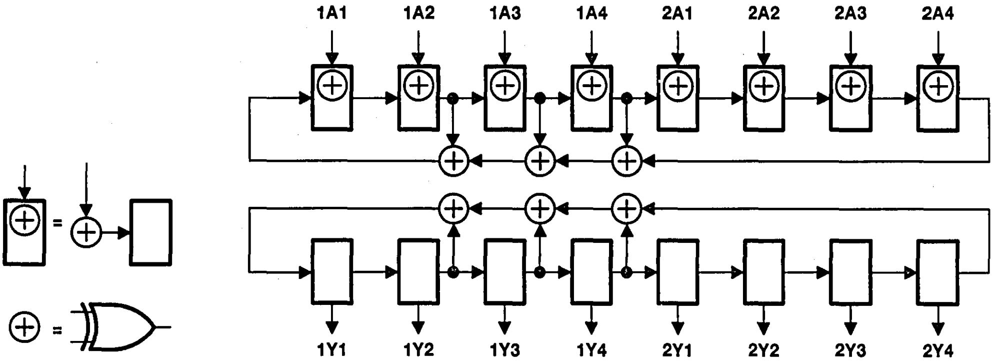



**Figure 7. 8-Bit PSA/PRPG Configuration**

## timing description

All test operations of the 'BCT8240A are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output terminals on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 8. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, as necessary, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 4 details the operation of the test circuitry during each TCK cycle.

**Table 4. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

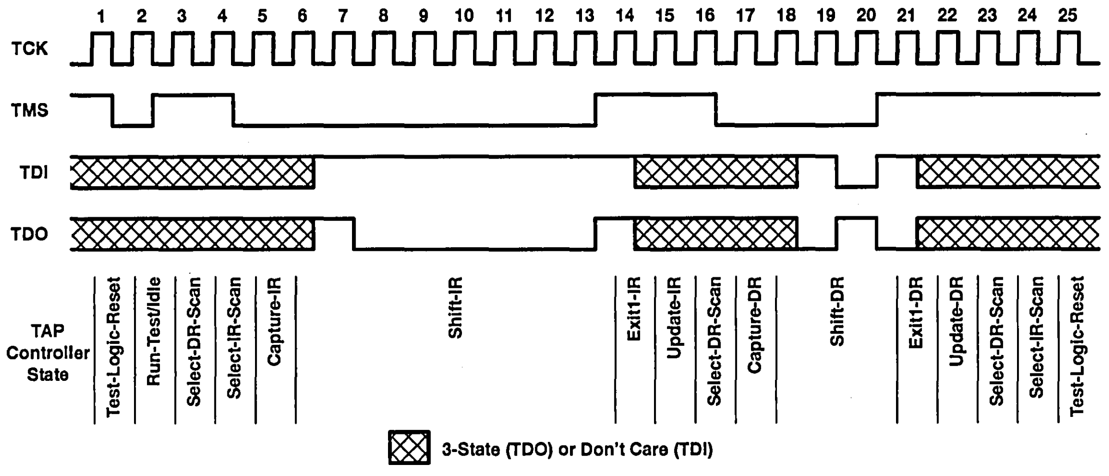



**Figure 8. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$: except TMS (see Note 1) | –0.5 V to 7 V |
| TMS (see Note 1) | –0.5 V to 12 V |
| Voltage range applied to any output in the disabled or power-off state | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state | –0.5 V to $V_{CC}$ |
| Input clamp current, $I_{IK}$ | –30 mA |
| Current into any output in the low state: SN54BCT8240A (TDO) | 40 mA |
| SN54BCT8240A (any Y) | 96 mA |
| SN74BCT8240A (TDO) | 48 mA |
| SN74BCT8240A (any Y) | 128 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DW package | 1.7 W |
| NT package | 1.3 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage rating may be exceeded if the input clamp-current rating is observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book,* literature number SCBD002.

## recommended operating conditions

| | | | SN54BCT8240A | | | SN74BCT8240A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IHH}$ | Double-high-level input voltage | TMS | 10 | | 12 | 10 | | 12 | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | –18 | | | –18 | mA |
| $I_{OH}$ | High-level output current | TDO | | | –3 | | | –3 | mA |
| | | Any Y | | | –12 | | | –15 | |
| $I_{OL}$ | Low-level output current | TDO | | | 20 | | | 24 | mA |
| | | Any Y | | | 48 | | | 64 | |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | 0 | | 70 | °C |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | | SN54BCT8240A | | | SN74BCT8240A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | Any Y | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –3 mA | | 2.7 | 3.4 | | 2.7 | 3.4 | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | | 2.4 | 3.4 | | 2.4 | 3.4 | | |
| | | | $I_{OH}$ = –12 mA | | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = –15 mA | | | | | 2 | 3.1 | | |
| | TDO | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –1 mA | | 2.7 | 3.4 | | 2.7 | 3.4 | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –1 mA | | 2.5 | 3.4 | | 2.5 | 3.4 | | |
| | | | $I_{OH}$ = –3 mA | | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| $V_{OL}$ | Any Y | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.38 | 0.55 | | | | V |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.42 | 0.55 | |
| | TDO | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | | 0.3 | 0.5 | | | | |
| | | | $I_{OL}$ = 24 mA | | | | | | 0.35 | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | –1 | –35 | –100 | –1 | –35 | –100 | μA |
| $I_{IHH}$ | TMS | $V_{CC}$ = 5.5 V, | $V_I$ = 10 V | | | | 1 | | | 1 | mA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | –30 | –70 | –200 | –30 | –70 | –200 | μA |
| $I_{OZH}$ | Any Y | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 50 | | | 50 | μA |
| | TDO | | | | –1 | –35 | –100 | –1 | –35 | –100 | |
| $I_{OZL}$ | Any Y | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | –50 | | | –50 | μA |
| | TDO | | | | –30 | –70 | –200 | –30 | –70 | –200 | |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 2 V, | $V_O$ = 0.5 V or 2.7 V | | | | ±250 | | | ±250 | μA |
| $I_{OZPD}$ | | $V_{CC}$ = 2 V to 0, | $V_O$ = 0.5 V or 2.7 V | | | | ±250 | | | ±250 | μA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \leq$ 4.5 V | | | | ±250 | | | ±250 | μA |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | | –100 | | –225 | –100 | | –225 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | Outputs open | Outputs high | | 3.5 | 7.5 | | 3.5 | 7.5 | mA |
| | | | | Outputs low | | 35 | 52 | | 35 | 52 | |
| | | | | Outputs disabled | | 1.5 | 3.5 | | 1.5 | 3.5 | |
| $C_i$ | | $V_{CC}$ = 5 V, | $V_I$ = 2.5 V or 0.5 V | | | 10 | | | 10 | | pF |
| $C_o$ | | $V_{CC}$ = 5 V, | $V_O$ = 2.5 V or 0.5 V | | | 18 | | | 18 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54BCT8240A | | SN74BCT8240A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 20 | 0 | 20 | 0 | 20 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 25 | | 25 | | 25 | | ns |
| | | TMS double high | 50* | | 50* | | 50 | | |
| $t_{su}$ | Setup time | Any A before TCK↑ | 6 | | 6 | | 6 | | ns |
| | | Any $\overline{OE}$ before TCK↑ | 6 | | 6 | | 6 | | |
| | | TDI before TCK↑ | 6 | | 6 | | 6 | | |
| | | TMS before TCK↑ | 12 | | 12 | | 12 | | |
| $t_h$ | Hold time | Any A after TCK↑ | 4.5 | | 4.5 | | 4.5 | | ns |
| | | Any $\overline{OE}$ after TCK↑ | 4.5 | | 4.5 | | 4.5 | | |
| | | TDI after TCK↑ | 4.5 | | 4.5 | | 4.5 | | |
| | | TMS after TCK↑ | 0 | | 0 | | 0 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 100* | | 100* | | 100 | | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 9)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54BCT8240A | | SN74BCT8240A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 2.5 | 5.7 | 7.5 | 2.5 | 10 | 2.5 | 9 | ns |
| $t_{PHL}$ | | | 2.5 | 5.2 | 7 | 2.5 | 9 | 2.5 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 3 | 6 | 8 | 3 | 10 | 3 | 9.5 | ns |
| $t_{PZL}$ | | | 3.5 | 7 | 9 | 3.5 | 12 | 3.5 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 2.5 | 6 | 8 | 2.5 | 10 | 2.5 | 9 | ns |
| $t_{PLZ}$ | | | 2.5 | 5.5 | 8 | 2.5 | 10 | 2.5 | 9 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54BCT8240A | | SN74BCT8240A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 20 | | | 20 | | 20 | | MHz |
| $t_{PLH}$ | TCK↓ | Y | 6 | 13 | 15.5 | 6 | 21.5 | 6 | 20 | ns |
| $t_{PHL}$ | | | 6 | 12.5 | 15.5 | 6 | 21.5 | 6 | 20 | |
| $t_{PLH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 14 | 3.5 | 13 | ns |
| $t_{PHL}$ | | | 3.5 | 8 | 10.5 | 3.5 | 13 | 3.5 | 12 | |
| $t_{PLH}$ | TCK↑ | Y | 7.5 | 16.5 | 20 | 7.5 | 28 | 7.5 | 24 | ns |
| $t_{PHL}$ | | | 7.5 | 17 | 21 | 7.5 | 29 | 7.5 | 25 | |
| $t_{PZH}$ | TCK↓ | Y | 6.5 | 14 | 17 | 6.5 | 24 | 6.5 | 21 | ns |
| $t_{PZL}$ | | | 7 | 15 | 20 | 7 | 26 | 7 | 23 | |
| $t_{PZH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 11.5 | 3.5 | 11 | ns |
| $t_{PZL}$ | | | 4 | 8.5 | 11 | 4 | 13.5 | 4 | 12.5 | |
| $t_{PZH}$ | TCK↑ | Y | 8 | 18 | 22 | 8 | 30 | 8 | 27 | ns |
| $t_{PZL}$ | | | 8 | 19 | 25 | 8 | 32 | 8 | 29 | |
| $t_{PHZ}$ | TCK↓ | Y | 6 | 14 | 18 | 6 | 24 | 6 | 22 | ns |
| $t_{PLZ}$ | | | 6 | 14 | 17 | 6 | 23 | 6 | 21 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 8 | 11.5 | 3 | 13 | 3 | 12.5 | ns |
| $t_{PLZ}$ | | | 3 | 7.5 | 10 | 3 | 13 | 3 | 12 | |
| $t_{PHZ}$ | TCK↑ | Y | 8 | 18.5 | 22 | 8 | 31 | 8 | 27 | ns |
| $t_{PLZ}$ | | | 8 | 18.5 | 22 | 8 | 31 | 8 | 27 | |

## PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)

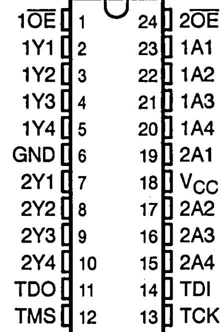
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. $C_L$ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \le 2.5$ ns, duty cycle = 50%.
- D. The outputs are measured one at a time with one transition per measurement.
- E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

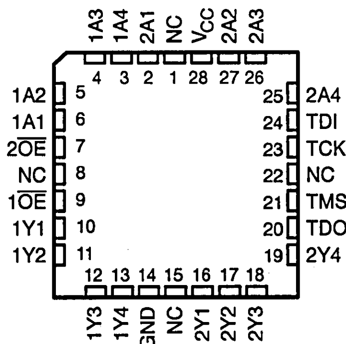
**Figure 9. Load Circuits and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Octal Test-Integrated Circuits
- Functionally Equivalent to 'F244 and 'BCT244 in the Normal-Function Mode
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Test Operation Synchronous to Test Access Port (TAP)
- Implement Optional Test Reset Signal by Recognizing a Double-High-Level Voltage (10 V) on TMS Pin
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

SN54BCT8244A . . . JT PACKAGE
SN74BCT8244A . . . DW OR NT PACKAGE
(TOP VIEW)




SN54BCT8244A . . . FK PACKAGE
(TOP VIEW)




NC – No internal connection

## description

The 'BCT8244A scan test devices with octal buffers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the 'F244 and 'BCT244 octal buffers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device terminals or to perform a self test on the boundary-test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal buffers.

In the test mode, the normal operation of the SCOPE™ octal buffers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary-scan test operations, as described in IEEE Standard 1149.1-1990.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

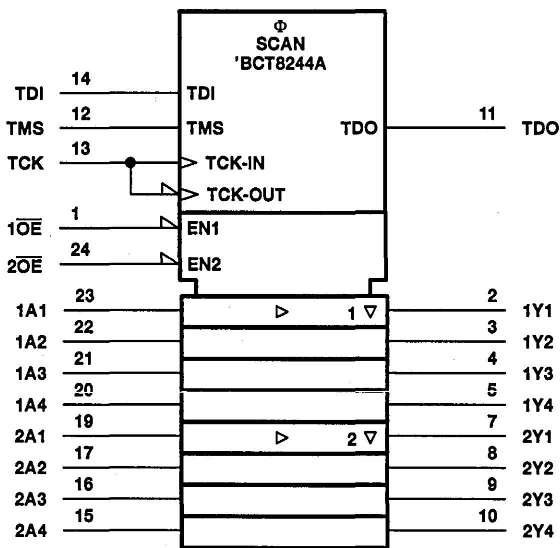
Four dedicated test terminals control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8244A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT8244A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(normal mode, each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| H | X | Z |
| L | L | L |
| L | H | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

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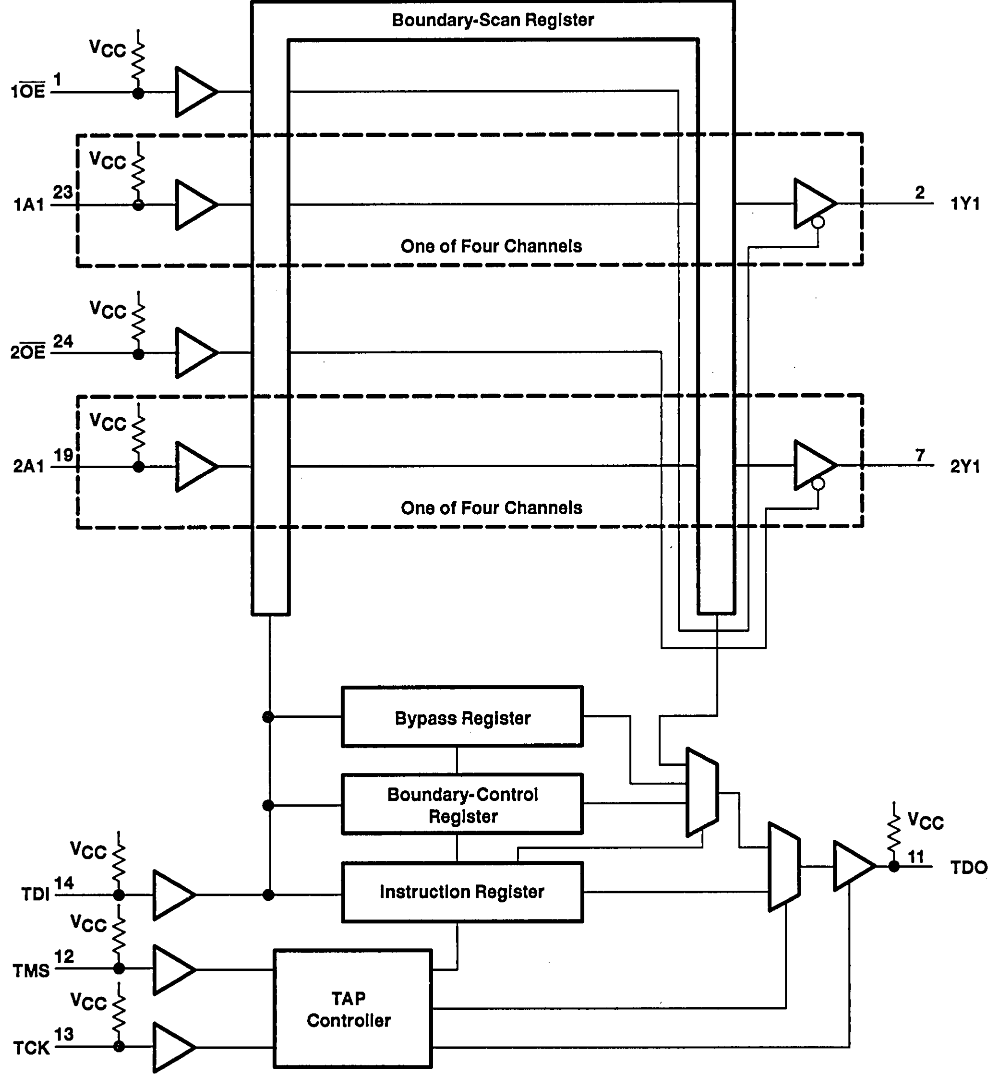
## functional block diagram




Pin numbers shown are for the DW, JT, and NT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A4, 2A1–2A4 | Normal-function data inputs. See function table for normal-mode logic. Internal pullups force these inputs high if left unconnected. |
| GND | Ground |
| $1\overline{OE}$, $2\overline{OE}$ | Normal-function output-enable inputs. See function table for normal-mode logic. Internal pullups force these inputs high if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. An internal pullup forces TCK to a high level if left unconnected. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. An internal pullup forces TDO to a high level when it is not active and is not driven from an external source. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. TMS also provides the optional test reset signal of IEEE Standard 1149.1-1990. This is implemented by recognizing a third logic level, double high ($V_{IHH}$), at TMS. |
| $V_{CC}$ | Supply voltage |
| 1Y1–1Y4, 2Y1–2Y4 | Normal-function data outputs. See function table for normal-mode logic. |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus, or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK, and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and three test-data registers: an 18-bit boundary-scan register, a 2-bit boundary-control register, and a 1-bit bypass register.

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'BCT8244A, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. The boundary-control register is reset to the binary value 10, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic may be actively running a test or may be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register may capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state.

For the 'BCT8244A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass register, any test register may be thought of as a serial-shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register may be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 2 lists the instructions supported by the 'BCT8244A. The even-parity feature specified for SCOPE™ devices is not supported in this device. Bit 7 of the instruction opcode is a don't-care bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR order of scan is shown in Figure 2.

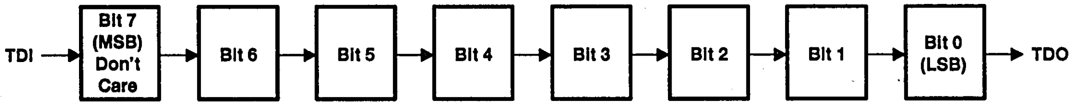



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 18 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function output pin. The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output terminals, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input terminals.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR may change during Run-Test/Idle as determined by the current instruction. The contents of the BSR are not changed in Test-Logic-Reset.

The BSR order of scan is from TDI through bits 17–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

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Table 1. Boundary-Scan Register Configuration

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 17 | 1$\overline{OE}$ | 15 | 1A1 | 7 | 1Y1 |
| 16 | 2$\overline{OE}$ | 14 | 1A2 | 6 | 1Y2 |
| – | – | 13 | 1A3 | 5 | 1Y3 |
| – | – | 12 | 1A4 | 4 | 1Y4 |
| – | – | 11 | 2A1 | 3 | 2Y1 |
| – | – | 10 | 2A2 | 2 | 2Y2 |
| – | – | 9 | 2A3 | 1 | 2Y3 |
| – | – | 8 | 2A4 | 0 | 2Y4 |

### boundary-control register

The boundary-control register (BCR) is two bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG and PSA. Table 3 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 10, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

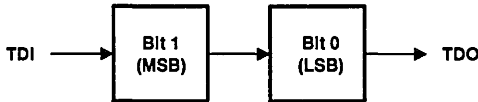



Figure 3. Boundary-Control Register Order of Scan

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

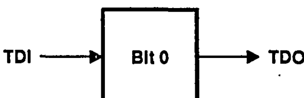



Figure 4. Bypass Register Order of Scan

## instruction-register opcode description

The instruction-register opcodes are shown in Table 2. The following descriptions detail the operation of each instruction.

**Table 2. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| X0000000 | EXTEST/INTEST | Boundary scan | Boundary scan | Test |
| X0000001 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| X0000011 | INTEST/EXTEST | Boundary scan | Boundary scan | Test |
| X0000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000110 | HIGHZ (TRIBYP) | Control boundary to high impedance | Bypass | Modified test |
| X0000111 | CLAMP (SETBYP) | Control boundary to 1/0 | Bypass | Test |
| X0001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0001001 | RUNT | Boundary run test | Bypass | Test |
| X0001010 | READBN | Boundary read | Boundary scan | Normal |
| X0001011 | READBT | Boundary read | Boundary scan | Test |
| X0001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| X0001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| X0001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| X0001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is a don't-care bit; X = don't care.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'BCT8244A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output terminals. The device operates in the test mode.

### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device output terminals are placed in the high-impedance state, the device input terminals remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output terminals. The device operates in the test mode.

**boundary run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The four test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, and simultaneous PSA and PRPG (PSA/PRPG).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches may be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device output terminals on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input terminals is not captured in the input BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control register opcode description

The BCR opcodes are decoded from BCR bits 1–0, as shown in Table 3. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and show the associated PSA and PRPG algorithms.

**Table 3. Boundary-Control Register Opcodes**

| BINARY CODE BIT 1 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| 00 | Sample inputs/toggle outputs (TOPSIP) |
| 01 | Pseudo-random pattern generation/16-bit mode (PRPG) |
| 10 | Parallel-signature analysis/16-bit mode (PSA) |
| 11 | Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG) |

It should be noted, in general, that while the control input BSCs (bits 17–16) are not included in the sample, toggle, PSA, or PRPG algorithms, the output-enable BSCs (bits 17–16 of the BSR) do control the drive state (active or high impedance) of the selected device output terminals.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the device input terminals is captured in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift register elements of the output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK.

## pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the BSCs on each rising edge of TCK and then updated in the shadow latches and applied to the device output terminals on each falling edge of TCK. This data also is updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Figure 5 shows the 16-bit linear-feedback shift-register algorithm through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

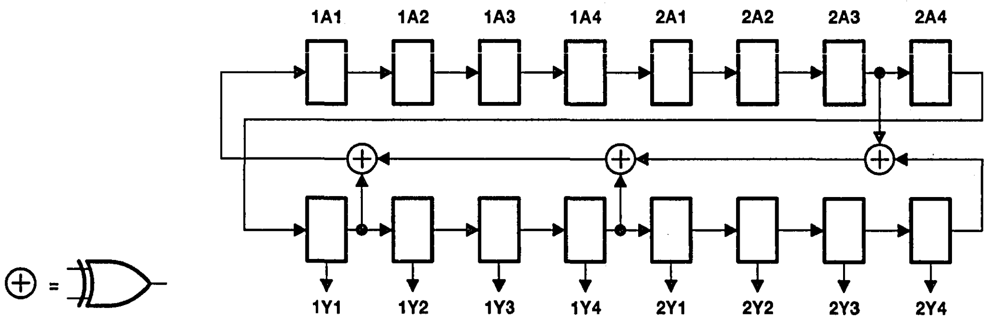



**Figure 5. 16-Bit PRPG Configuration**

**parallel-signature analysis (PSA)**

Data appearing at the device input terminals is compressed into a 16-bit parallel signature in the shift-register elements of the BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the output BSCs remains constant and is applied to the device outputs. Figure 6 shows the 16-bit linear-feedback shift-register algorithm through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

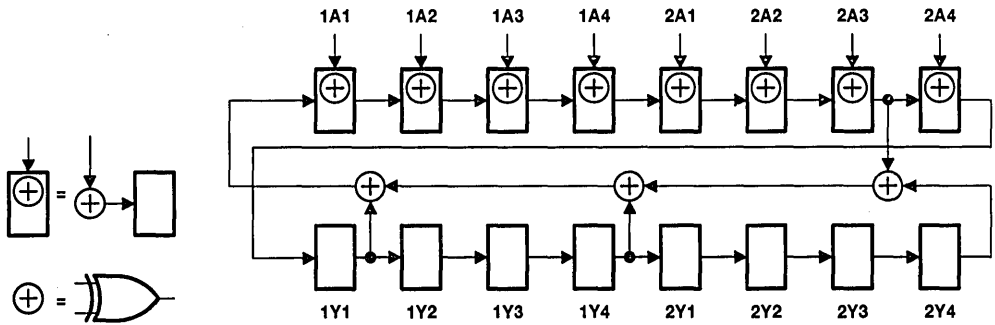



**Figure 6. 16-Bit PSA Configuration**

**simultaneous PSA and PRPG (PSA/PRPG)**

Data appearing at the device input terminals is compressed into an 8-bit parallel signature in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK. Figure 7 shows the 8-bit linear-feedback shift-register algorithm through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

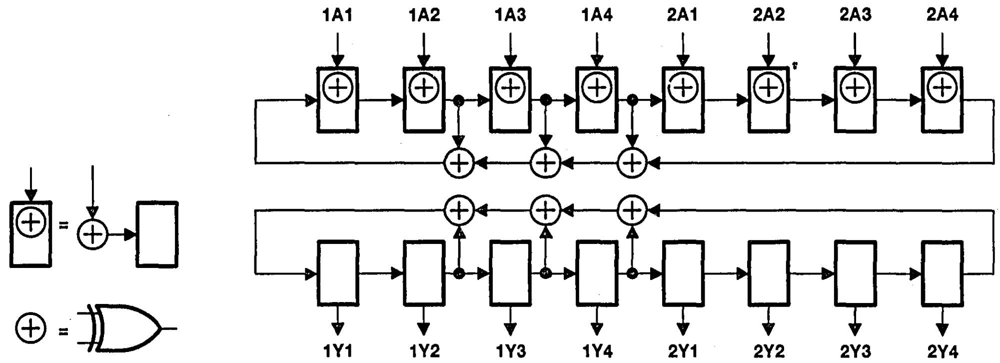



**Figure 7. 8-Bit PSA/PRPG Configuration**

## timing description

All test operations of the 'BCT8244A are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output terminals on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 8. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, as necessary, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 4 details the operation of the test circuitry during each TCK cycle.

**Table 4. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

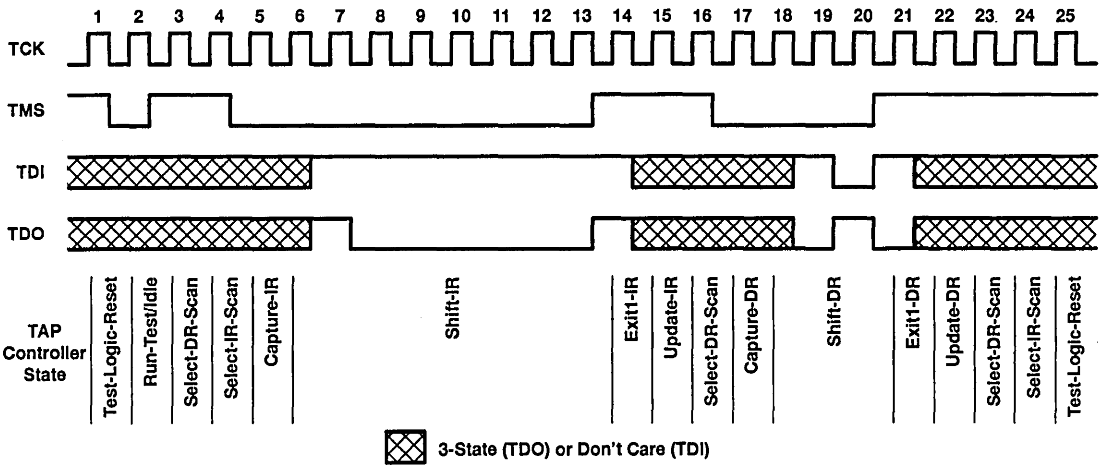



**Figure 8. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$: except TMS (see Note 1) | –0.5 V to 7 V |
| TMS (see Note 1) | –0.5 V to 12 V |
| Voltage range applied to any output in the disabled or power-off state | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state | –0.5 V to $V_{CC}$ |
| Input clamp current, $I_{IK}$ | –30 mA |
| Current into any output in the low state: SN54BCT8244A (TDO) | 40 mA |
| SN54BCT8244A (any Y) | 96 mA |
| SN74BCT8244A (TDO) | 48 mA |
| SN74BCT8244A (any Y) | 128 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DW package | 1.7 W |
| NT package | 1.3 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage rating may be exceeded if the input clamp-current rating is observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54BCT8244A | | | SN74BCT8244A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IHH}$ | Double-high-level input voltage | TMS | 10 | | 12 | 10 | | 12 | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | –18 | | | –18 | mA |
| $I_{OH}$ | High-level output current | TDO | | | –3 | | | –3 | mA |
| | | Any Y | | | –12 | | | –15 | |
| $I_{OL}$ | Low-level output current | TDO | | | 20 | | | 24 | mA |
| | | Any Y | | | 48 | | | 64 | |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | SN54BCT8244A | | | SN74BCT8244A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | Any Y | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –3 mA | | 2.7 | 3.4 | | 2.7 | 3.4 | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | | 2.4 | 3.4 | | 2.4 | 3.4 | | |
| | | | $I_{OH}$ = –12 mA | | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = –15 mA | | | | | 2 | 3.1 | | |
| | TDO | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –1 mA | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –1 mA | | 2.5 | 3.4 | | 2.5 | 3.4 | | |
| | | | $I_{OH}$ = –3 mA | | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| $V_{OL}$ | Any Y | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.38 | 0.55 | | | | V |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.42 | 0.55 | |
| | TDO | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | | 0.3 | 0.5 | | | | |
| | | | $I_{OL}$ = 24 mA | | | | | | 0.35 | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | –1 | –35 | –100 | –1 | –35 | –100 | µA |
| $I_{IHH}$ | TMS | $V_{CC}$ = 5.5 V, | $V_I$ = 10 V | | | | 1 | | | 1 | mA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | –30 | –70 | –200 | –30 | –70 | –200 | µA |
| $I_{OZH}$ | Any Y | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 50 | | | 50 | µA |
| | TDO | | | | –1 | –35 | –100 | –1 | –35 | –100 | |
| $I_{OZL}$ | Any Y | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | –50 | | | –50 | µA |
| | TDO | | | | –30 | –70 | –200 | –30 | –70 | –200 | |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 2 V, | $V_O$ = 0.5 V or 2.7 V | | | | ±250 | | | ±250 | µA |
| $I_{OZPD}$ | | $V_{CC}$ = 2 V to 0, | $V_O$ = 0.5 V or 2.7 V | | | | ±250 | | | ±250 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \leq$ 4.5 V | | | | ±250 | | | ±250 | µA |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | | –100 | | –225 | –100 | | –225 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | Outputs open | Outputs high | | 3.5 | 7.5 | | 3.5 | 7.5 | mA |
| | | | | Outputs low | | 35 | 52 | | 35 | 52 | |
| | | | | Outputs disabled | | 1.5 | 3.5 | | 1.5 | 3.5 | |
| $C_i$ | | $V_{CC}$ = 5 V, | $V_I$ = 2.5 V or 0.5 V | | | 10 | | | 10 | | pF |
| $C_o$ | | $V_{CC}$ = 5 V, | $V_O$ = 2.5 V or 0.5 V | | | 18 | | | 18 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)**

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54BCT8244A | | SN74BCT8244A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 20 | 0 | 20 | 0 | 20 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 25 | | 25 | | 25 | | ns |
| | | TMS double high | 50* | | 50* | | 50 | | |
| $t_{su}$ | Setup time | Any A before TCK↑ | 6 | | 6 | | 6 | | ns |
| | | Any $\overline{OE}$ before TCK↑ | 6 | | 6 | | 6 | | |
| | | TDI before TCK↑ | 6 | | 6 | | 6 | | |
| | | TMS before TCK↑ | 12 | | 12 | | 12 | | |
| $t_h$ | Hold time | Any A after TCK↑ | 4.5 | | 4.5 | | 4.5 | | ns |
| | | Any $\overline{OE}$ after TCK↑ | 4.5 | | 4.5 | | 4.5 | | |
| | | TDI after TCK↑ | 4.5 | | 4.5 | | 4.5 | | |
| | | TMS after TCK↑ | 0 | | 0 | | 0 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 100* | | 100* | | 100 | | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 9)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54BCT8244A | | SN74BCT8244A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 2 | 5.4 | 7 | 2 | 9 | 2 | 8.5 | ns |
| $t_{PHL}$ | | | 2 | 5.2 | 7 | 2 | 9 | 2 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 3 | 6 | 8 | 3 | 10 | 3 | 9.5 | ns |
| $t_{PZL}$ | | | 3.5 | 7 | 9 | 3.5 | 12 | 3.5 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 2.5 | 6 | 8 | 2.5 | 10 | 2.5 | 9 | ns |
| $t_{PLZ}$ | | | 2.5 | 5.5 | 8 | 2.5 | 10 | 2.5 | 9 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54BCT8244A | | SN74BCT8244A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 20 | | | 20 | | 20 | | MHz |
| $t_{PLH}$ | TCK↓ | Y | 6 | 13 | 15.5 | 6 | 21.5 | 6 | 20 | ns |
| $t_{PHL}$ | | | 6 | 12.5 | 15.5 | 6 | 21.5 | 6 | 20 | |
| $t_{PLH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 14 | 3.5 | 13 | ns |
| $t_{PHL}$ | | | 3.5 | 8 | 10.5 | 3.5 | 13 | 3.5 | 12 | |
| $t_{PLH}$ | TCK↑ | Y | 7.5 | 16.5 | 20 | 7.5 | 28 | 7.5 | 24 | ns |
| $t_{PHL}$ | | | 7.5 | 17 | 21 | 7.5 | 29 | 7.5 | 25 | |
| $t_{PZH}$ | TCK↓ | Y | 6.5 | 14 | 17 | 6.5 | 24 | 6.5 | 21 | ns |
| $t_{PZL}$ | | | 7 | 15 | 20 | 7 | 26 | 7 | 23 | |
| $t_{PZH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 11.5 | 3.5 | 11 | ns |
| $t_{PZL}$ | | | 4 | 8.5 | 11 | 4 | 13.5 | 4 | 12.5 | |
| $t_{PZH}$ | TCK↑ | Y | 8 | 18 | 22 | 8 | 30 | 8 | 27 | ns |
| $t_{PZL}$ | | | 8 | 19 | 25 | 8 | 32 | 8 | 29 | |
| $t_{PHZ}$ | TCK↓ | Y | 6 | 14 | 18 | 6 | 24 | 6 | 22 | ns |
| $t_{PLZ}$ | | | 6 | 14 | 17 | 6 | 23 | 6 | 21 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 8 | 11.5 | 3 | 13 | 3 | 12.5 | ns |
| $t_{PLZ}$ | | | 3 | 7.5 | 10 | 3 | 13 | 3 | 12 | |
| $t_{PHZ}$ | TCK↑ | Y | 8 | 18.5 | 22 | 8 | 31 | 8 | 27 | ns |
| $t_{PLZ}$ | | | 8 | 18.5 | 22 | 8 | 31 | 8 | 27 | |

## PARAMETER MEASUREMENT INFORMATION

7 V ($t_{PZL}$, $t_{PLZ}$, O.C.) — Open (all others) — S1 — R1 — From Output Under Test — Test Point — $C_L$ (see Note A) — R2 — $R_L$ = R1 = R2

LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS

From Output Under Test — Test Point — $C_L$ (see Note A) — R1

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

Timing Input — 3 V — 1.5 V — 0 V — $t_{su}$ — $t_h$ — Data Input — 1.5 V — 1.5 V — 3 V — 0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

High-Level Pulse — 1.5 V — 1.5 V — 3 V — 0 V — $t_w$ — Low-Level Pulse — 1.5 V — 1.5 V — 3 V — 0 V

VOLTAGE WAVEFORMS
PULSE DURATION

Input — 1.5 V — 1.5 V — 3 V — 0 V — $t_{PLH}$ — $t_{PHL}$ — In-Phase Output — 1.5 V — 1.5 V — $V_{OH}$ — $V_{OL}$ — $t_{PHL}$ — $t_{PLH}$ — Out-of-Phase Output — 1.5 V — 1.5 V — $V_{OH}$ — $V_{OL}$

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)

Output Control (low-level enable) — 1.5 V — 1.5 V — 3 V — 0 V — $t_{PZL}$ — $t_{PLZ}$ — Waveform 1 (see Note B) — 1.5 V — 3.5 V — $V_{OL}$ — 0.3 V — $t_{PZH}$ — $t_{PHZ}$ — Waveform 2 (see Note B) — 1.5 V — $V_{OH}$ — 0.3 V — 0 V

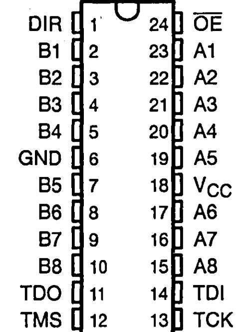
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq$ 2.5 ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

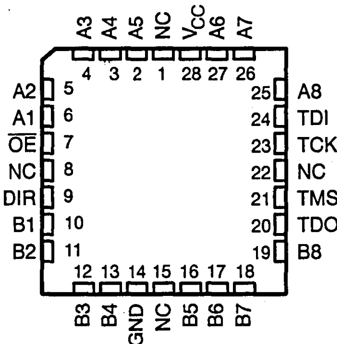
**Figure 9. Load Circuits and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Octal Test-Integrated Circuits
- Functionally Equivalent to 'F245 and 'BCT245 in the Normal-Function Mode
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Test Operation Synchronous to Test Access Port (TAP)
- Implement Optional Test Reset Signal by Recognizing a Double-High-Level Voltage (10 V) on TMS Pin
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP, and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

SN54BCT8245A . . . JT PACKAGE
SN74BCT8245A . . . DW OR NT PACKAGE
(TOP VIEW)




SN54BCT8245A . . . FK PACKAGE
(TOP VIEW)




NC – No internal connection

## description

The 'BCT8245A scan test devices with octal bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the 'F245 and 'BCT245 octal bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device terminals or to perform a self test on the boundary-test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers.

In the test mode, the normal operation of the SCOPE™ octal bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary-scan test operations as described in IEEE Standard 1149.1-1990.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

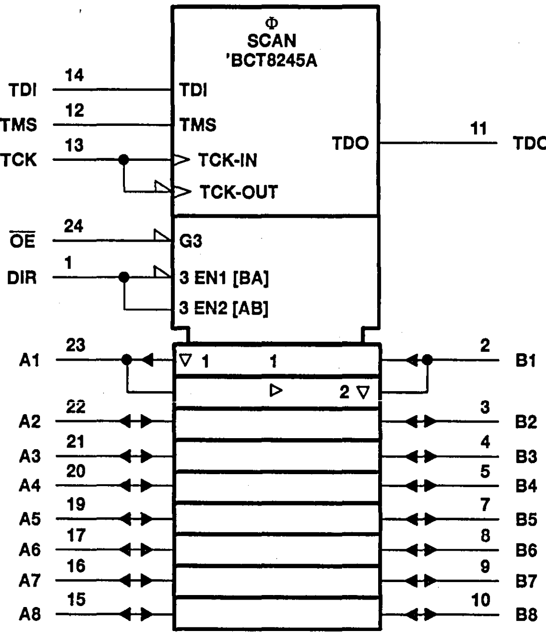
Four dedicated test terminals control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8245A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT8245A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(normal mode)**

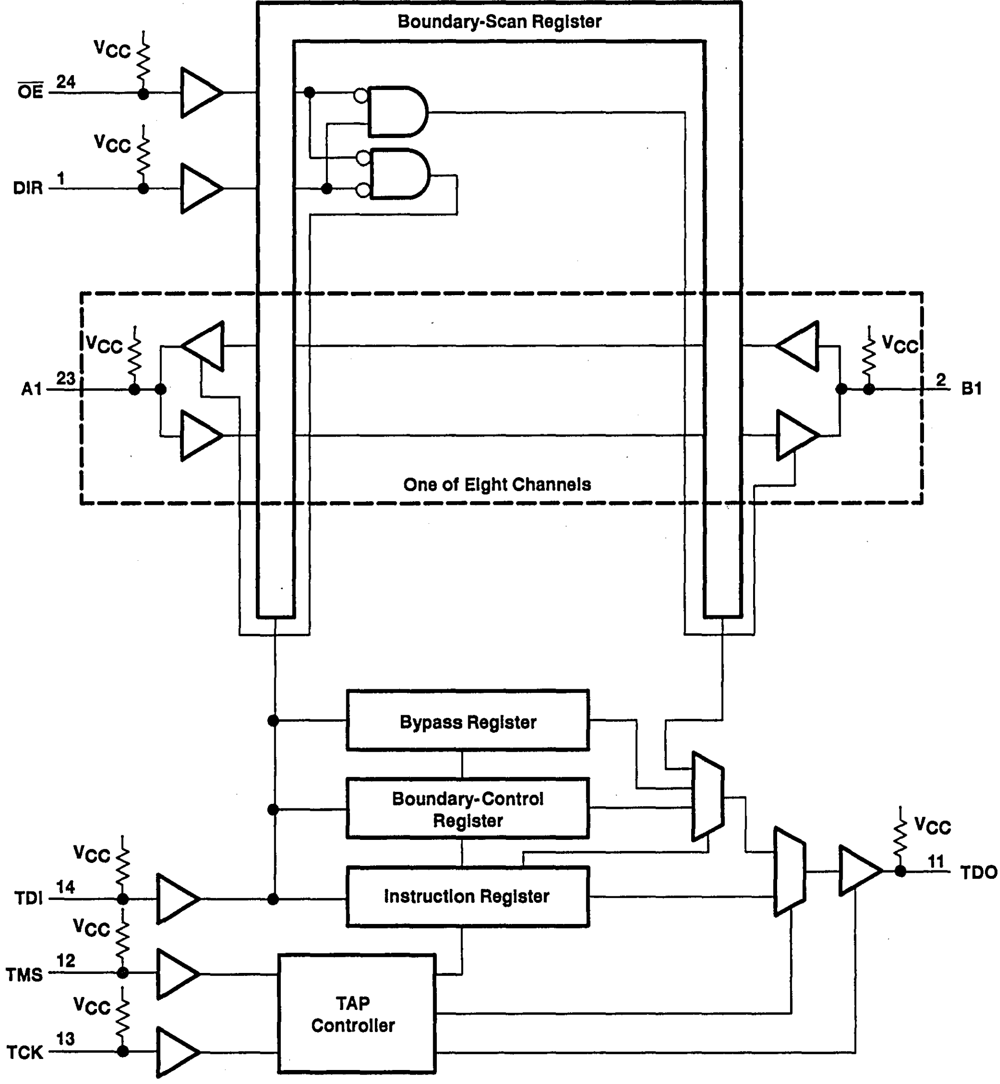
| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

## functional block diagram




Pin numbers shown are for the DW, JT, and NT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A1–A8 | A-bus I/O ports. See function table for normal-mode logic. Internal pullups force these I/O ports to a high level if left unconnected. |
| B1–B8 | B-bus I/O ports. See function table for normal-mode logic. Internal pullups force these I/O ports to a high level if left unconnected. |
| DIR | Normal-function direction-control input. See function table for normal-mode logic. An internal pullup forces DIR to a high level if left unconnected. |
| GND | Ground |
| $\overline{OE}$ | Normal-function output-enable input. See function table for normal-mode logic. An internal pullup forces $\overline{OE}$ to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. An internal pullup forces TCK to a high level if left unconnected. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. An internal pullup forces TDO to a high level when it is not active and is not driven from an external source. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. TMS also provides the optional test reset signal of IEEE Standard 1149.1-1990. This is implemented by recognizing a third logic level, double high ($V_{IHH}$), at TMS. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus, or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK, and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and three test-data registers: an 18-bit boundary-scan register, a 2-bit boundary-control register, and a 1-bit bypass register.

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'BCT8245A, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. The boundary-control register is reset to the binary value 10, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic may be actively running a test or may be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected-data register may capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK, after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state.

For the 'BCT8245A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

### register overview

With the exception of the bypass register, any test register may be thought of as a serial-shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register may be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

### instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 2 lists the instructions supported by the 'BCT8245A. The even-parity feature specified for SCOPE™ devices is not supported in this device. Bit 7 of the instruction opcode is a don't-care bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR order of scan is shown in Figure 2.

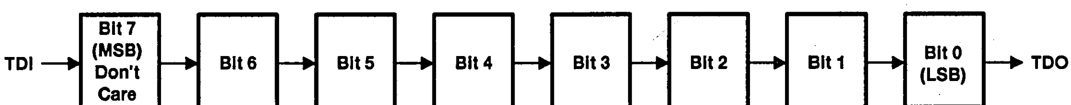



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 18 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function output pin. Which I/O ports, A or B, function as input terminals and which function as output terminals is determined by the DIR signal (BSC17) as described below. The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output terminals, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input terminals.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR may change during Run-Test/Idle, as determined by the current instruction. The contents of the BSR are not changed in Test-Logic-Reset.

The BSR order of scan is from TDI through bits 17–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals. The device signals I1–I8 and O1–O8 represent data input signals and data output signals, respectively. The direction control signal (DIR) as output by BSC17 determines which port, A or B, is considered an input and which is considered an output. When the output of BSC17 is logic 0, the device signals I1–I8 are associated with I/O ports B1–B8, while device signals O1–O8 are associated with I/O ports A1–A8. When the output of BSC17 is logic 1, the converse is true (that is, I1–I8 are associated with A1–A8, while O1–O8 are associated with B1–B8). In normal-function mode, the output of the BSC17 input is equivalent to the input signal present at the DIR input pin.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 17 | DIR | 15 | I1 | 7 | O1 |
| 16 | $\overline{OE}$ | 14 | I2 | 6 | O2 |
| – | – | 13 | I3 | 5 | O3 |
| – | – | 12 | I4 | 4 | O4 |
| – | – | 11 | I5 | 3 | O5 |
| – | – | 10 | I6 | 2 | O6 |
| – | – | 9 | I7 | 1 | O7 |
| – | – | 8 | I8 | 0 | O8 |

### boundary-control register

The boundary-control register (BCR) is two bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG and PSA. Table 3 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 10, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

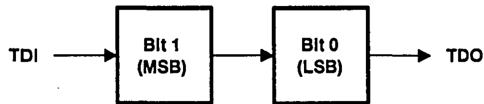



**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

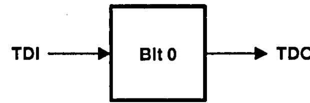



**Figure 4. Bypass Register Order of Scan**

## instruction-register opcode description

The instruction-register opcodes are shown in Table 2. The following descriptions detail the operation of each instruction.

**Table 2. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| X0000000 | EXTEST/INTEST | Boundary scan | Boundary scan | Test |
| X0000001 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| X0000011 | INTEST/EXTEST | Boundary scan | Boundary scan | Test |
| X0000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000110 | HIGHZ (TRIBYP) | Control boundary to high impedance | Bypass | Modified test |
| X0000111 | CLAMP (SETBYP) | Control boundary to 1/0 | Bypass | Test |
| X0001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0001001 | RUNT | Boundary run test | Bypass | Test |
| X0001010 | READBN | Boundary read | Boundary scan | Normal |
| X0001011 | READBT | Boundary read | Boundary scan | Test |
| X0001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| X0001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| X0001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| X0001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is a don't-care bit; X = don't care.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'BCT8245A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output terminals. The device operates in the test mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**sample boundary**

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device output terminals are placed in the high-impedance state, the device input terminals remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output terminals. The device operates in the test mode.

**boundary run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The four test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, and simultaneous PSA and PRPG (PSA/PRPG).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches may be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device output terminals on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input terminals is not captured in the input BSCs. The device operates in the test mode.

**boundary-control register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control register opcode description

The BCR opcodes are decoded from BCR bits 1–0, as shown in Table 3. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 3. Boundary-Control Register Opcodes**

| BINARY CODE BIT 1 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| 00 | Sample inputs/toggle outputs (TOPSIP) |
| 01 | Pseudo-random pattern generation/16-bit mode (PRPG) |
| 10 | Parallel-signature analysis/16-bit mode (PSA) |
| 11 | Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG) |

It should be noted, in general, that while the control input BSCs (bits 17–16) are not included in the sample, toggle, PSA, or PRPG algorithms, the output-enable BSC (bit 16 of the BSR) does control the drive state (active or high impedance) of the device output terminals while the direction-control BSC (bit 17) controls which I/O ports, A or B, are considered input terminals and which are considered output terminals.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the device input terminals is captured in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift register elements of the output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK.

## pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the BSCs on each rising edge of TCK and then updated in the shadow latches and applied to the device output terminals on each falling edge of TCK. This data also is updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Figure 5 illustrates the 16-bit linear-feedback shift-register algorithm through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

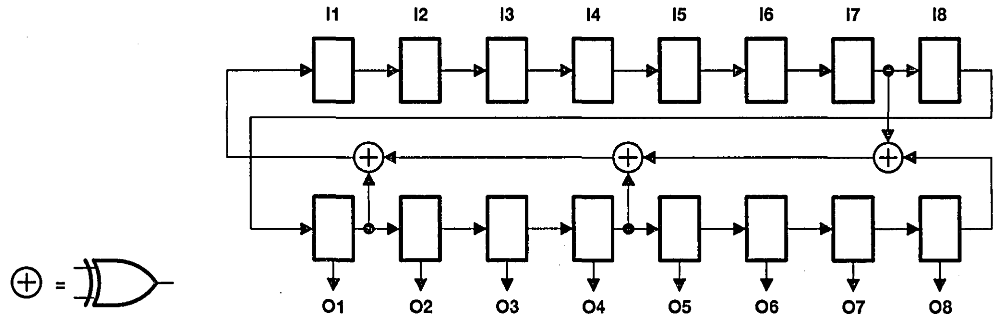



**Figure 5. 16-Bit PRPG Configuration**

**parallel-signature analysis (PSA)**

Data appearing at the device input terminals is compressed into a 16-bit parallel signature in the shift-register elements of the BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the output BSCs remains constant and is applied to the device outputs. Figure 6 illustrates the 16-bit linear-feedback shift-register algorithm through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

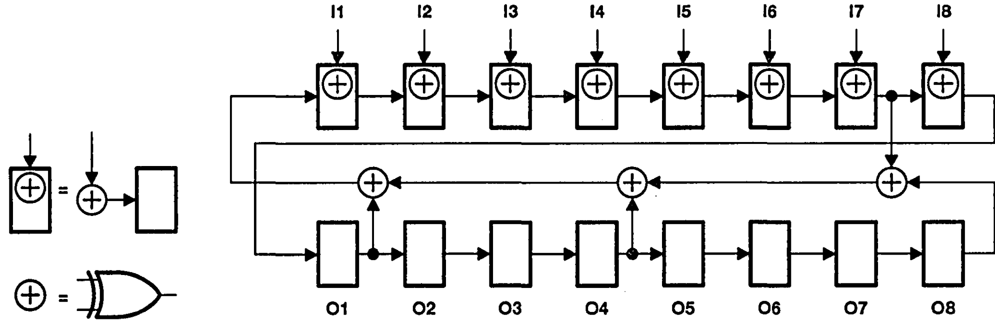



**Figure 6. 16-Bit PSA Configuration**

**simultaneous PSA and PRPG (PSA/PRPG)**

Data appearing at the device input terminals is compressed into an 8-bit parallel signature in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK. Figure 7 illustrates the 8-bit linear-feedback shift-register algorithm through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

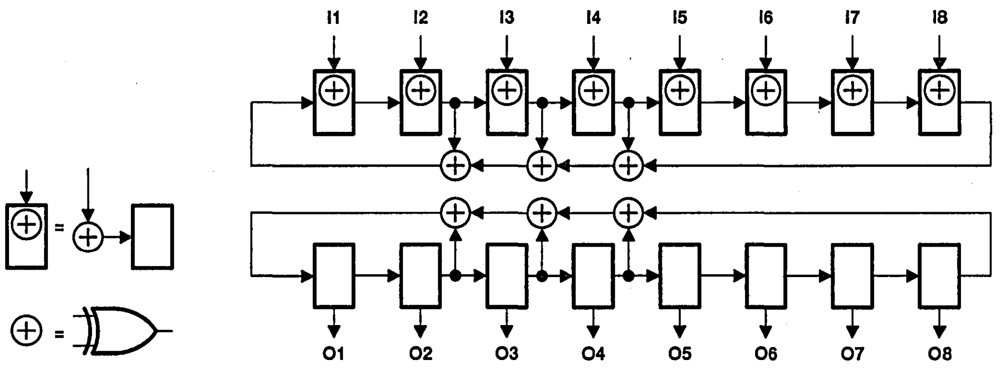



**Figure 7. 8-Bit PSA/PRPG Configuration**

## timing description

All test operations of the 'BCT8245A are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output terminals on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 8. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 4 details the operation of the test circuitry during each TCK cycle.

**Table 4. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

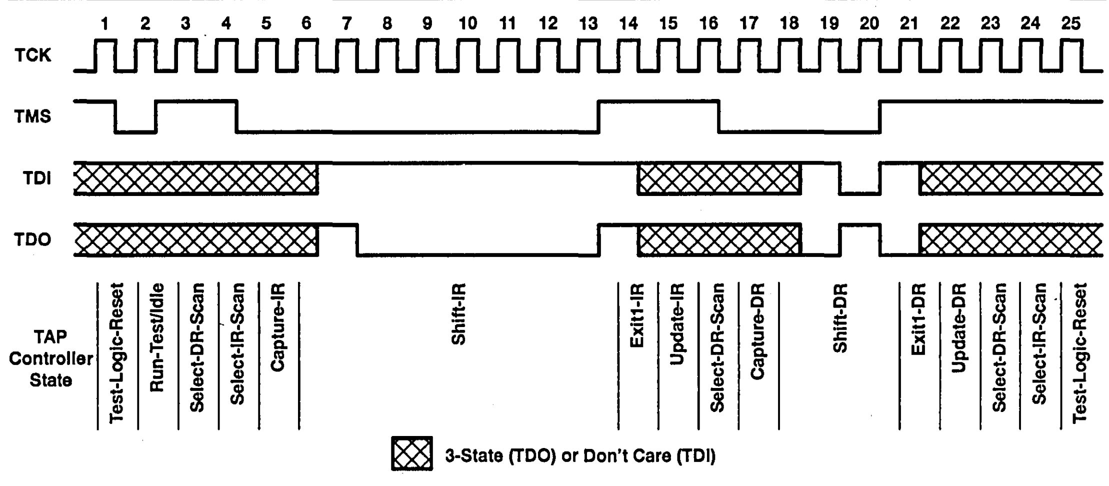



**Figure 8. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .......... –0.5 V to 7 V
Input voltage range, $V_I$: I/O ports (see Note 1) .......... –0.5 V to 5.5 V
except I/O ports and TMS (see Note 1) .......... –0.5 V to 7 V
Input voltage range (TMS) (see Note 1) .......... –0.5 V to 12 V
Voltage range applied to any output in the disabled or power-off state .......... –0.5 V to 5.5 V
Voltage range applied to any output in the high state .......... –0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ .......... –30 mA
Current into any output in the low state: SN54BCT8245A (any A, TDO) .......... 40 mA
SN54BCT8245A (any B) .......... 96 mA
SN74BCT8245A (any A, TDO) .......... 48 mA
SN74BCT8245A (any B) .......... 128 mA
Maximum power dissipation at $T_A$ = 55° C (in still air) (see Note 2): DW package .......... 1.7 W
NT package .......... 1.3 W
Storage temperature range, $T_{stg}$ .......... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage rating may be exceeded if the input clamp-current rating is observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54BCT8245A | | | SN74BCT8245A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IHH}$ | Double-high-level input voltage | TMS | 10 | | 12 | 10 | | 12 | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | –18 | | | –18 | mA |
| $I_{OH}$ | High-level output current | Any A, TDO | | | –3 | | | –3 | mA |
| | | Any B | | | –12 | | | –15 | |
| $I_{OL}$ | Low-level output current | Any A, TDO | | | 20 | | | 24 | mA |
| | | Any B | | | 48 | | | 64 | |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54BCT8245A MIN | SN54BCT8245A TYP† | SN54BCT8245A MAX | SN74BCT8245A MIN | SN74BCT8245A TYP† | SN74BCT8245A MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | Any A, TDO | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –1 mA | 2.7 | 3.4 | | 2.7 | 3.4 | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | |
| | | | $I_{OH}$ = –3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | Any B | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –3 mA | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | |
| | | | $I_{OH}$ = –12 mA | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = –15 mA | | | | 2 | 3.1 | | |
| $V_{OL}$ | Any A, TDO | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| | Any B | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_I$ | Except A or B | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | 0.1 | | | 0.1 | mA |
| | Any A or B | | | | | 0.25 | | | 0.25 | |
| $I_{IH}$‡ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | –1 | –35 | –100 | –1 | –35 | –100 | µA |
| $I_{IHH}$ | TMS | $V_{CC}$ = 5.5 V, | $V_I$ = 10 V | | | 1 | | | 1 | mA |
| $I_{IL}$‡ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | –30 | –70 | –200 | –30 | –70 | –200 | µA |
| $I_{OZH}$ | TDO | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | –1 | –35 | –100 | –1 | –35 | –100 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | –30 | –70 | –200 | –30 | –70 | –200 | µA |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 2 V, | $V_O$ = 0.5 V or 2.7 V | | | ±250 | | | ±250 | µA |
| $I_{OZPD}$ | | $V_{CC}$ = 2 V to 0, | $V_O$ = 0.5 V or 2.7 V | | | ±250 | | | ±250 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±250 | | | ±250 | µA |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | –100 | | –225 | –100 | | –225 | mA |
| $I_{CC}$¶ | | $V_{CC}$ = 5.5 V, Outputs open | Outputs high | | 3.6 | 7.5 | | 3.6 | 7.5 | mA |
| | | | Outputs low | | 35 | 52 | | 35 | 52 | |
| | | | Outputs disabled | | 1.5 | 3.5 | | 1.5 | 3.5 | |
| $C_i$ | | $V_{CC}$ = 5 V, | $V_I$ = 2.5 V or 0.5 V | | 8 | | | 8 | | pF |
| $C_{io}$ | | $V_{CC}$ = 5 V, | $V_O$ = 2.5 V or 0.5 V | | 14 | | | 14 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ $I_{CCH}$ and $I_{CCL}$ are measured in the A-data to B-bus operational mode.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)**

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54BCT8245A | | SN74BCT8245A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 20 | 0 | 20 | 0 | 20 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 25 | | 25 | | 25 | | ns |
| | | TMS double high | 50* | | 50* | | 50 | | |
| $t_{su}$ | Setup time | Any A or B before TCK↑ | 6 | | 6 | | 6 | | ns |
| | | DIR or $\overline{OE}$ before TCK↑ | 6 | | 6 | | 6 | | |
| | | TDI before TCK↑ | 6 | | 6 | | 6 | | |
| | | TMS before TCK↑ | 12 | | 12 | | 12 | | |
| $t_h$ | Hold time | Any A or B after TCK↑ | 4.5 | | 4.5 | | 4.5 | | ns |
| | | DIR or $\overline{OE}$ after TCK↑ | 4.5 | | 4.5 | | 4.5 | | |
| | | TDI after TCK↑ | 4.5 | | 4.5 | | 4.5 | | |
| | | TMS after TCK↑ | 0 | | 0 | | 0 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 100* | | 100* | | 100 | | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 9)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54BCT8245A | | SN74BCT8245A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 2 | 5.8 | 7.8 | 2 | 9.6 | 2 | 8.7 | ns |
| $t_{PHL}$ | | | 2 | 6.1 | 8.7 | 2 | 11 | 2 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | 3 | 6.8 | 9.5 | 3 | 11.5 | 3 | 10.6 | ns |
| $t_{PZL}$ | | | 3 | 8.8 | 12.5 | 3 | 14.3 | 3 | 13.8 | |
| $t_{PHZ}$ | OE | B or A | 3 | 6.2 | 8.6 | 3 | 10.2 | 3 | 9.6 | ns |
| $t_{PLZ}$ | | | 2.5 | 6 | 8 | 2.5 | 10.5 | 2.5 | 9.5 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54BCT8245A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | TCK | | 20 | | | 20 | | MHz |
| $t_{PLH}$ | TCK↓ | B or A | 6 | 13 | 15.5 | 6 | 21.5 | ns |
| $t_{PHL}$ | | | 6 | 12.5 | 15.5 | 6 | 21.5 | |
| $t_{PLH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 14 | ns |
| $t_{PHL}$ | | | 3.5 | 8 | 10.5 | 3.5 | 13 | |
| $t_{PLH}$ | TCK↑ | B or A | 7.5 | 16.5 | 20 | 7.5 | 28 | ns |
| $t_{PHL}$ | | | 7.5 | 17 | 21 | 7.5 | 29 | |
| $t_{PZH}$ | TCK↓ | B or A | 6.5 | 14 | 17 | 6.5 | 24 | ns |
| $t_{PZL}$ | | | 7 | 15 | 20 | 7 | 26 | |
| $t_{PZH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 11.5 | ns |
| $t_{PZL}$ | | | 4 | 8.5 | 12 | 4 | 17.5 | |
| $t_{PZH}$ | TCK↑ | B or A | 8 | 18 | 22 | 8 | 30 | ns |
| $t_{PZL}$ | | | 8 | 19 | 25 | 8 | 32 | |
| $t_{PHZ}$ | TCK↓ | B or A | 6 | 14 | 18 | 6 | 24 | ns |
| $t_{PLZ}$ | | | 6 | 14 | 18 | 6 | 23 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 8 | 11.5 | 3 | 13 | ns |
| $t_{PLZ}$ | | | 3 | 7.5 | 10 | 3 | 13 | |
| $t_{PHZ}$ | TCK↑ | B or A | 8 | 18.5 | 22 | 8 | 31 | ns |
| $t_{PLZ}$ | | | 8 | 18.5 | 22 | 8 | 31 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74BCT8245A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | TCK | | 20 | | | 20 | | MHz |
| $t_{PLH}$ | TCK↓ | B or A | 6 | 13 | 15.5 | 6 | 20 | ns |
| $t_{PHL}$ | | | 6 | 12.5 | 15.5 | 6 | 20 | |
| $t_{PLH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 13 | ns |
| $t_{PHL}$ | | | 3.5 | 8 | 10.5 | 3.5 | 12 | |
| $t_{PLH}$ | TCK↑ | B or A | 7.5 | 16.5 | 20 | 7.5 | 24 | ns |
| $t_{PHL}$ | | | 7.5 | 17 | 21 | 7.5 | 25 | |
| $t_{PZH}$ | TCK↓ | B or A | 6.5 | 14 | 17 | 6.5 | 21 | ns |
| $t_{PZL}$ | | | 7 | 15 | 20 | 7 | 23 | |
| $t_{PZH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 11 | ns |
| $t_{PZL}$ | | | 4 | 8.5 | 11 | 4 | 12.5 | |
| $t_{PZH}$ | TCK↑ | B or A | 8 | 18 | 22 | 8 | 27 | ns |
| $t_{PZL}$ | | | 8 | 19 | 25 | 8 | 29 | |
| $t_{PHZ}$ | TCK↓ | B or A | 6 | 14 | 18 | 6 | 22 | ns |
| $t_{PLZ}$ | | | 6 | 14 | 17 | 6 | 21 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 8 | 11.5 | 3 | 12.5 | ns |
| $t_{PLZ}$ | | | 3 | 7.5 | 10 | 3 | 12 | |
| $t_{PHZ}$ | TCK↑ | B or A | 8 | 18.5 | 22 | 8 | 27 | ns |
| $t_{PLZ}$ | | | 8 | 18.5 | 22 | 8 | 27 | |

## PARAMETER MEASUREMENT INFORMATION

7 V ($t_{PZL}$, $t_{PLZ}$, O.C.)
Open (all others)
S1
R1
From Output Under Test
Test Point
$C_L$ (see Note A)
R2
$R_L$ = R1 = R2

LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS

From Output Under Test
Test Point
$C_L$ (see Note A)
R1

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

Timing Input
Data Input
1.5 V
3 V
0 V
$t_{su}$
$t_h$

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

High-Level Pulse
Low-Level Pulse
1.5 V
3 V
0 V
$t_w$

VOLTAGE WAVEFORMS
PULSE DURATION

Input
In-Phase Output
Out-of-Phase Output
1.5 V
3 V
0 V
$V_{OH}$
$V_{OL}$
$t_{PLH}$
$t_{PHL}$

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)

Output Control (low-level enable)
Waveform 1 (see Notes B)
Waveform 2 (see Notes B)
1.5 V
3 V
0 V
3.5 V
$V_{OL}$
0.3 V
$V_{OH}$
$t_{PZL}$
$t_{PLZ}$
$t_{PHZ}$
$t_{PZH}$

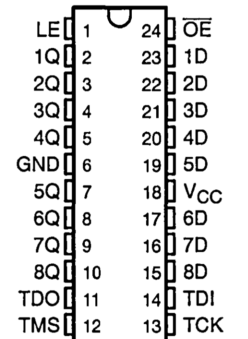
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq$ 2.5 ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

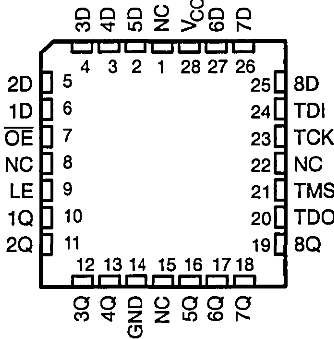
**Figure 9. Load Circuits and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Octal Test-Integrated Circuits
- Functionally Equivalent to 'F373 and 'BCT373 in the Normal-Function Mode
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Test Operation Synchronous to Test Access Port (TAP)
- Implement Optional Test Reset Signal by Recognizing a Double-High-Level Voltage (10 V) on TMS Pin
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP, and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

SN54BCT8373A . . . JT PACKAGE
SN74BCT8373A . . . DW OR NT PACKAGE
(TOP VIEW)




SN54BCT8373A . . . FK PACKAGE
(TOP VIEW)




NC – No internal connection

## description

The 'BCT8373A scan test devices with octal D-type latches are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the 'F373 and 'BCT373 octal D-type latches. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device terminals or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal latches.

In the test mode, the normal operation of the SCOPE™ octal latches is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations, as described in IEEE Standard 1149.1-1990.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

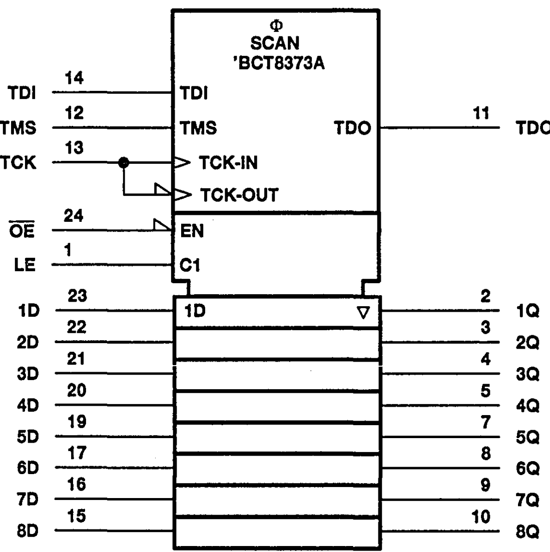
Four dedicated test terminals are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8373A is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74BCT8373A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(normal mode, each latch)**

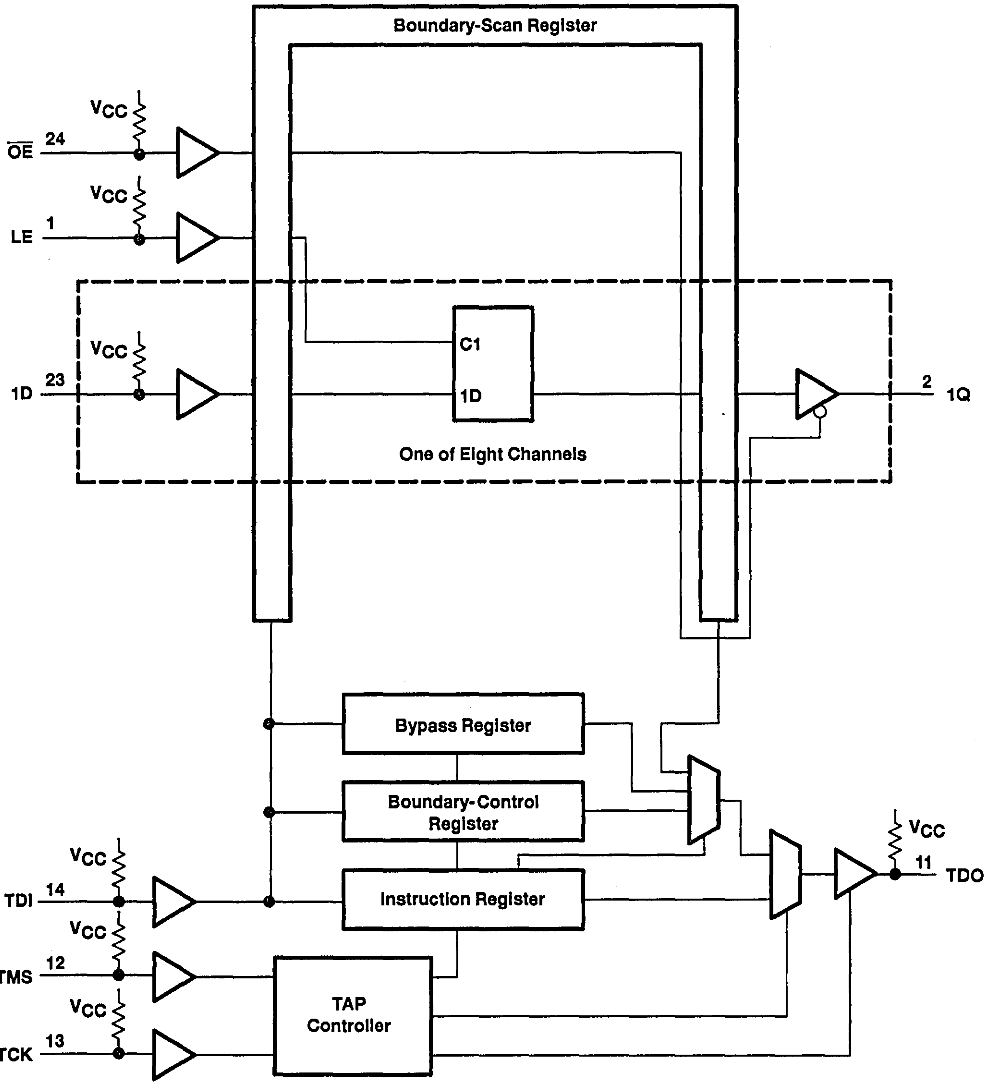
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

## functional block diagram




Pin numbers shown are for the DW, JT, and NT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1D–8D | Normal-function data inputs. See function table for normal-mode logic. Internal pullups force these inputs to a high level if left unconnected. |
| GND | Ground |
| LE | Normal-function latch-enable input. See function table for normal-mode logic. An internal pullup forces LE to a high level if left unconnected. |
| $\overline{OE}$ | Normal-function output-enable input. See function table for normal-mode logic. An internal pullup forces $\overline{OE}$ to a high level if left unconnected. |
| 1Q–8Q | Normal-function data outputs. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. An internal pullup forces TCK to a high level if left unconnected. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. An internal pullup forces TDO to a high level when it is not active and is not driven from an external source. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. The TMS pin also provides the optional test reset signal of IEEE Standard 1149.1-1990. This is implemented by recognizing a third logic level, double-high ($V_{IHH}$), at TMS. |
| $V_{CC}$ | Supply voltage |

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## test architecture

Serial test information is conveyed by means of a 4-wire test bus, or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK, and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and three test data registers: an 18-bit boundary-scan register, a 2-bit boundary-control register, and a 1-bit bypass register.

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes is to be open circuited.

For the 'BCT8373A, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. The boundary-control register is reset to the binary value 10, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered, following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic may be actively running a test or may be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register may capture a data value, as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle, in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state.

For the 'BCT8373A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle, in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass register, any test register may be thought of as a serial shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register may be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 2 lists the instructions supported by the 'BCT8373A. The even-parity feature specified for SCOPE™ devices is not supported in this device. Bit 7 of the instruction opcode is a don't-care bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR order of scan is shown in Figure 2.

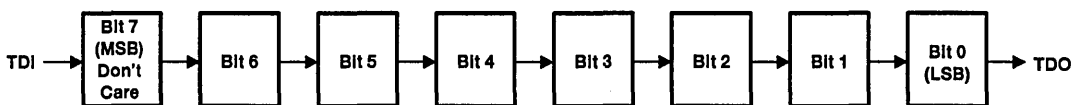



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 18 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function output pin. The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR may change during Run-Test/Idle as determined by the current instruction. The contents of the BSR are not changed in Test-Logic-Reset.

The BSR order of scan is from TDI through bits 17–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 17 | LE | 15 | 1D | 7 | 1Q |
| 16 | $\overline{OE}$ | 14 | 2D | 6 | 2Q |
| – | – | 13 | 3D | 5 | 3Q |
| – | – | 12 | 4D | 4 | 4Q |
| – | – | 11 | 5D | 3 | 5Q |
| – | – | 10 | 6D | 2 | 6Q |
| – | – | 9 | 7D | 1 | 7Q |
| – | – | 8 | 8D | 0 | 8Q |

### boundary-control register

The boundary-control register (BCR) is two bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG and PSA. Table 3 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 10, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

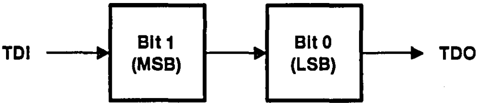



**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

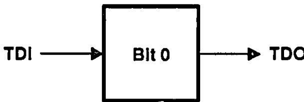



**Figure 4. Bypass Register Order of Scan**

## instruction register opcode description

The instruction register opcodes are shown in Table 2. The following descriptions detail the operation of each instruction.

**Table 2. Instruction Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| X0000000 | EXTEST/INTEST | Boundary scan | Boundary scan | Test |
| X0000001 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| X0000011 | INTEST/EXTEST | Boundary scan | Boundary scan | Test |
| X0000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000110 | HIGHZ (TRIBYP) | Control boundary to high impedance | Bypass | Modified test |
| X0000111 | CLAMP (SETBYP) | Control boundary to 1/0 | Bypass | Test |
| X0001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0001001 | RUNT | Boundary run test | Bypass | Test |
| X0001010 | READBN | Boundary read | Boundary scan | Normal |
| X0001011 | READBT | Boundary read | Boundary scan | Test |
| X0001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| X0001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| X0001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| X0001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is a don't-care bit; X = don't care.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'BCT8373A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output terminals. The device operates in the test mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**sample boundary**

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device output terminals are placed in the high-impedance state, the device input terminals remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output terminals. The device operates in the test mode.

**boundary run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The four test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, and simultaneous PSA and PRPG (PSA/PRPG).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches may be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device output terminals on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input terminals is not captured in the input BSCs. The device operates in the test mode.

**boundary-control register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary run test operation in order to specify which test operation is to be executed.

## boundary-control register opcode description

The BCR opcodes are decoded from BCR bits 1–0 as shown in Table 3. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 3. Boundary-Control Register Opcodes**

| BINARY CODE BIT 1 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| 00 | Sample inputs/toggle outputs (TOPSIP) |
| 01 | Pseudo-random pattern generation/16-bit mode (PRPG) |
| 10 | Parallel signature analysis/16-bit mode (PSA) |
| 11 | Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG) |

It should be noted, in general, that while the control input BSCs (bits 17–16) are not included in the sample, toggle, PSA, or PRPG algorithms, the output-enable BSC (bit 16 of the BSR) does control the drive state (active or high impedance) of the device output terminals.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the device input terminals is captured in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK.

## pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the BSCs on each rising edge of TCK and then updated in the shadow latches and applied to the device output terminals on each falling edge of TCK. This data is also updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Figure 5 illustrates the 16-bit linear-feedback shift-register algorithm through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

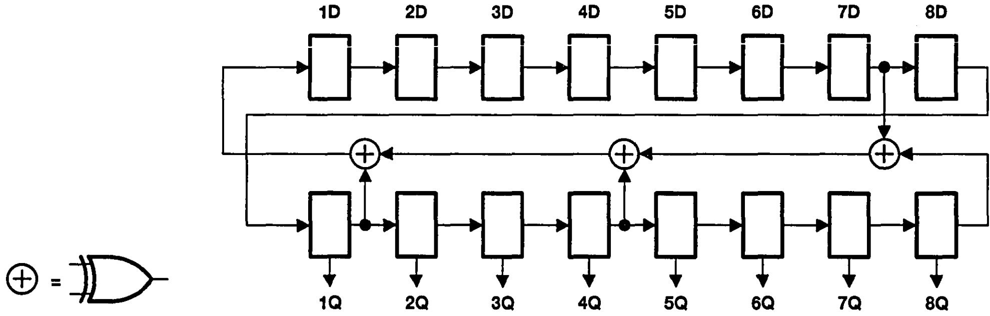



**Figure 5. 16-Bit PRPG Configuration**

### parallel signature analysis (PSA)

Data appearing at the device input terminals is compressed into a 16-bit parallel signature in the shift-register elements of the BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the output BSCs remains constant and is applied to the device outputs. Figure 6 illustrates the 16-bit linear-feedback shift-register algorithm through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

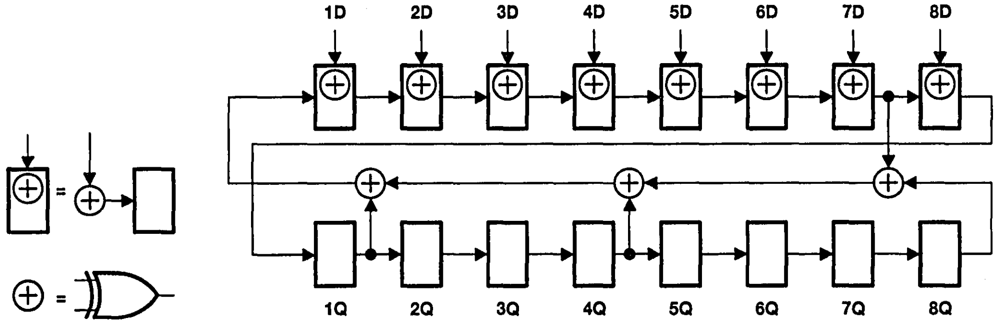



**Figure 6. 16-Bit PSA Configuration**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the device input terminals is compressed into an 8-bit parallel signature in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK. Figure 7 illustrates the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

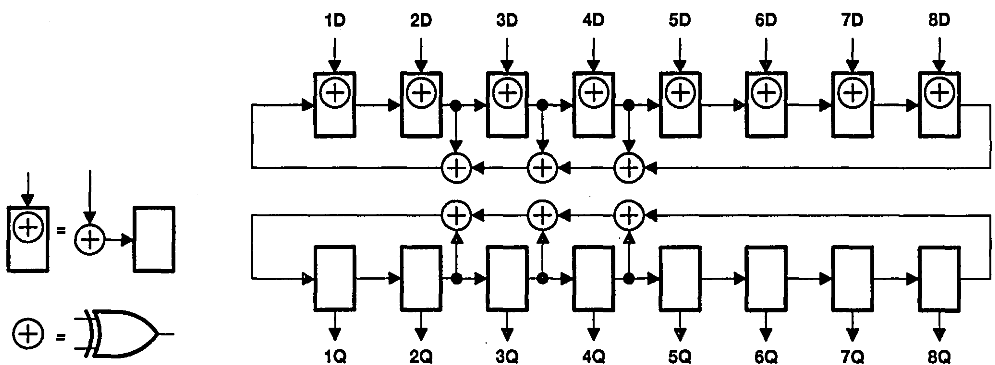



**Figure 7. 8-Bit PSA/PRPG Configuration**

## timing description

All test operations of the 'BCT8373A are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output terminals on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 8. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, as necessary, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 4 details the operation of the test circuitry during each TCK cycle.

**Table 4. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active, and TDI is made valid, on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

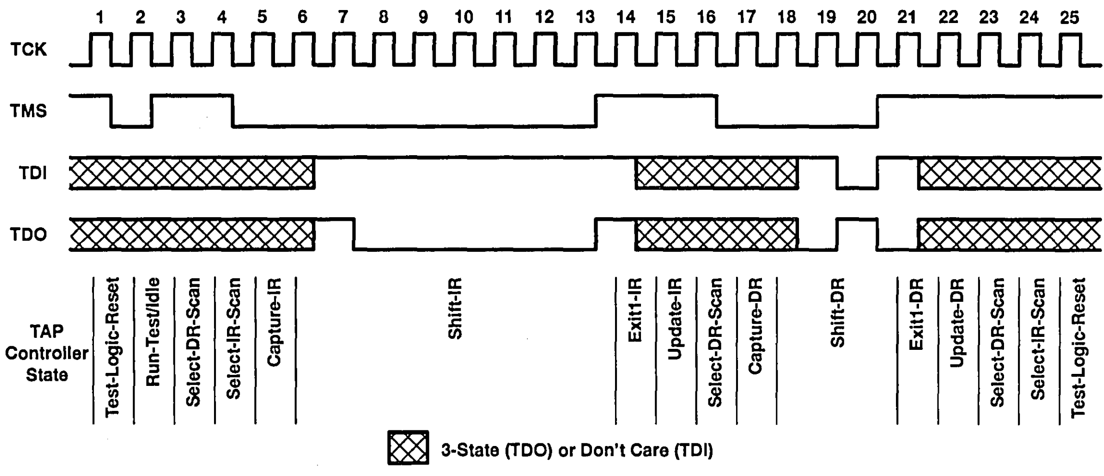



**Figure 8. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | −0.5 V to 7 V |
| Input voltage range, $V_I$: Except TMS (see Note 1) | −0.5 V to 7 V |
| TMS (see Note 1) | −0.5 V to 12 V |
| Voltage range applied to any output in the disabled or power-off state | −0.5 V to 5.5 V |
| Voltage range applied to any output in the high state | −0.5 V to $V_{CC}$ |
| Input clamp current | −30 mA |
| Current into any output in the low state: SN54BCT8373A (TDO) | 40 mA |
| SN54BCT8373A (Any Q) | 96 mA |
| SN74BCT8373A (TDO) | 48 mA |
| SN74BCT8373A (Any Q) | 128 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DW package | 1.7 W |
| NT package | 1.3 W |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage rating may be exceeded if the input clamp-current rating is observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54BCT8373A | | | SN74BCT8373A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IHH}$ | Double-high-level input voltage | TMS | 10 | | 12 | 10 | | 12 | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | –18 | | | –18 | mA |
| $I_{OH}$ | High-level output current | TDO | | | –3 | | | –3 | mA |
| | | Any Q | | | –12 | | | –15 | |
| $I_{OL}$ | Low-level output current | TDO | | | 20 | | | 24 | mA |
| | | Any Q | | | 48 | | | 64 | |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | SN54BCT8373A MIN | SN54BCT8373A TYP† | SN54BCT8373A MAX | SN74BCT8373A MIN | SN74BCT8373A TYP† | SN74BCT8373A MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | Any Q | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −3 mA | | 2.7 | 3.4 | | 2.7 | 3.4 | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −3 mA | | 2.4 | 3.4 | | 2.4 | 3.4 | | |
| | | | $I_{OH}$ = −12 mA | | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = −15 mA | | | | | 2 | 3.1 | | |
| | TDO | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | | 2.5 | 3.4 | | 2.5 | 3.4 | | |
| | | | $I_{OH}$ = −3 mA | | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| $V_{OL}$ | Any Q | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.38 | 0.55 | | | | V |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.42 | 0.55 | |
| | TDO | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | | 0.3 | 0.5 | | | | |
| | | | $I_{OL}$ = 24 mA | | | | | | 0.35 | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | −1 | −35 | −100 | −1 | −35 | −100 | µA |
| $I_{IHH}$ | TMS | $V_{CC}$ = 5.5 V, | $V_I$ = 10 V | | | | 1 | | | 1 | mA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | −30 | −70 | −200 | −30 | −70 | −200 | µA |
| $I_{OZH}$ | Any Q | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 50 | | | 50 | µA |
| | TDO | | | | −1 | −35 | −100 | −1 | −35 | −100 | |
| $I_{OZL}$ | Any Q | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | −50 | | | −50 | µA |
| | TDO | | | | −30 | −70 | −200 | −30 | −70 | −200 | |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 2 V, | $V_O$ = 0.5 V or 2.7 V | | | | ±250 | | | ±250 | µA |
| $I_{OZPD}$ | | $V_{CC}$ = 2 V to 0, | $V_O$ = 0.5 V or 2.7 V | | | | ±250 | | | ±250 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \le$ 4.5 V | | | | ±250 | | | ±250 | µA |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | | −100 | | −225 | −100 | | −225 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | Outputs open | Outputs high | | 3.5 | 7.5 | | 3.5 | 7.5 | mA |
| | | | | Outputs low | | 35 | 52 | | 35 | 52 | |
| | | | | Outputs disabled | | 1.5 | 3.5 | | 1.5 | 3.5 | |
| $C_i$ | | $V_{CC}$ = 5 V, | $V_I$ = 2.5 V or 0.5 V | | | 10 | | | 10 | | pF |
| $C_o$ | | $V_{CC}$ = 5 V, | $V_O$ = 2.5 V or 0.5 V | | | 14 | | | 14 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 9)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54BCT8373A | | SN74BCT8373A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time | Data before LE↓ | 3 | | 3 | | 3 | | ns |
| $t_h$ | Hold time | Data after LE↓ | 2 | | 2 | | 2 | | ns |

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54BCT8373A | | SN74BCT8373A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 20 | 0 | 20 | 0 | 20 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 25 | | 25 | | 25 | | ns |
| | | TMS double high | 50* | | 50* | | 50 | | |
| $t_{su}$ | Setup time | Any D before TCK↑ | 6 | | 6 | | 6 | | ns |
| | | LE or $\overline{OE}$ before TCK↑ | 6 | | 6 | | 6 | | |
| | | TDI before TCK↑ | 6 | | 6 | | 6 | | |
| | | TMS before TCK↑ | 12 | | 12 | | 12 | | |
| $t_h$ | Hold time | Any D after TCK↑ | 4.5 | | 4.5 | | 4.5 | | ns |
| | | LE or $\overline{OE}$ after TCK↑ | 4.5 | | 4.5 | | 4.5 | | |
| | | TDI after TCK↑ | 4.5 | | 4.5 | | 4.5 | | |
| | | TMS after TCK↑ | 0 | | 0 | | 0 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 100* | | 100* | | 100 | | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

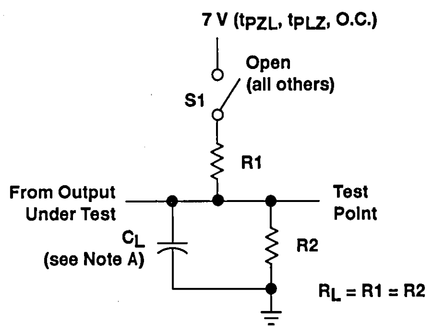
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 9)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54BCT8373A | | SN74BCT8373A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | Q | 3 | 6.5 | 8.5 | 3 | 10.5 | 3 | 9.5 | ns |
| $t_{PHL}$ | | | 3 | 6.2 | 8 | 3 | 10.5 | 3 | 9.5 | |
| $t_{PLH}$ | LE | Q | 3 | 6.8 | 9 | 3 | 11 | 3 | 10 | ns |
| $t_{PHL}$ | | | 3 | 6.7 | 8.5 | 3 | 11 | 3 | 10 | |
| $t_{PZH}$ | OE | Q | 3 | 6.5 | 8.5 | 3 | 10.5 | 3 | 10 | ns |
| $t_{PZL}$ | | | 3.5 | 7.5 | 9.5 | 3.5 | 11.5 | 3.5 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 3 | 6.1 | 8 | 3 | 10 | 3 | 9 | ns |
| $t_{PLZ}$ | | | 2.5 | 5.8 | 7.5 | 2.5 | 9.5 | 2.5 | 8.5 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54BCT8373A | | SN74BCT8373A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 20 | | | 20 | | 20 | | MHz |
| $t_{PLH}$ | TCK↓ | Q | 6 | 13 | 15.5 | 6 | 21.5 | 6 | 20 | ns |
| $t_{PHL}$ | | | 6 | 12.5 | 15.5 | 6 | 21.5 | 6 | 20 | ns |
| $t_{PLH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 14 | 3.5 | 13 | ns |
| $t_{PHL}$ | | | 3.5 | 8 | 10.5 | 3.5 | 13 | 3.5 | 12 | |
| $t_{PLH}$ | TCK↑ | Q | 7.5 | 16.5 | 20 | 7.5 | 28 | 7.5 | 24 | ns |
| $t_{PHL}$ | | | 7.5 | 17 | 21 | 7.5 | 29 | 7.5 | 25 | |
| $t_{PZH}$ | TCK↓ | Q | 6.5 | 14 | 17 | 6.5 | 24 | 6.5 | 21 | ns |
| $t_{PZL}$ | | | 7 | 15 | 20 | 7 | 26 | 7 | 23 | |
| $t_{PZH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 11.5 | 3.5 | 11 | ns |
| $t_{PZL}$ | | | 4 | 8.5 | 11 | 4 | 13.5 | 4 | 12.5 | |
| $t_{PZH}$ | TCK↑ | Q | 8 | 18 | 22 | 8 | 30 | 8 | 27 | ns |
| $t_{PZL}$ | | | 8 | 19 | 25 | 8 | 32 | 8 | 29 | |
| $t_{PHZ}$ | TCK↓ | Q | 6 | 14 | 18 | 6 | 24 | 6 | 22 | ns |
| $t_{PLZ}$ | | | 6 | 14 | 17 | 6 | 23 | 6 | 21 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 8 | 11.5 | 3 | 13 | 3 | 12.5 | ns |
| $t_{PLZ}$ | | | 3 | 7.5 | 10 | 3 | 13 | 3 | 12 | |
| $t_{PHZ}$ | TCK↑ | Q | 8 | 18.5 | 22 | 8 | 31 | 8 | 27 | ns |
| $t_{PLZ}$ | | | 8 | 18.5 | 22 | 8 | 31 | 8 | 27 | |

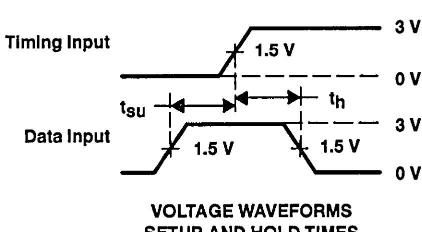
## PARAMETER MEASUREMENT INFORMATION



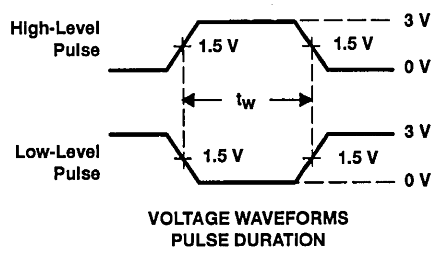

LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS

From Output Under Test — Test Point — $C_L$ (see Note A) — R1

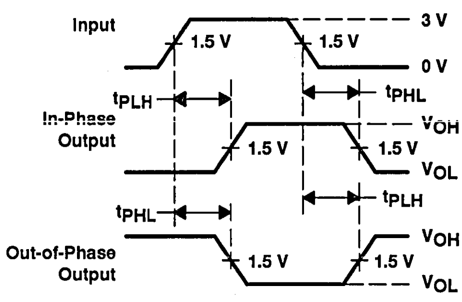
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



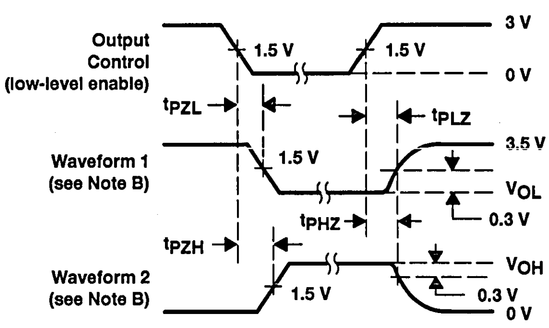

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



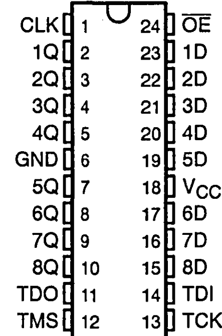

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq$ 2.5 ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

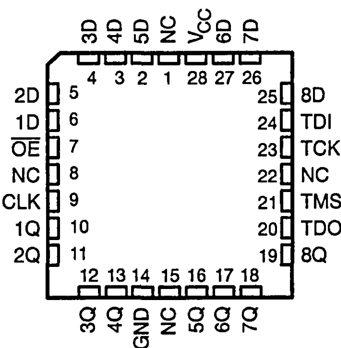
**Figure 9. Load Circuits and Voltage Waveforms**

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Octal Test-Integrated Circuits**
- **Functionally Equivalent to 'F374 and 'BCT374 in the Normal-Function Mode**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Test Operation Synchronous to Test Access Port (TAP)**
- **Implement Optional Test Reset Signal by Recognizing a Double-High-Level Voltage (10 V) on TMS Pin**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP, and HIGHZ**
  - **Parallel-Signature Analysis at Inputs**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

**SN54BCT8374A . . . JT PACKAGE**
**SN74BCT8374A . . . DW OR NT PACKAGE**
**(TOP VIEW)**




**SN54BCT8374A . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'BCT8374A scan test devices with octal edge-triggered D-type flip-flops are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the 'F374 and 'BCT374 octal D-type flip-flops. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device terminals or to perform a self test on the boundary-test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal flip-flops.

In the test mode, the normal operation of the SCOPE™ octal flip-flops is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary-scan test operations as described in IEEE Standard 1149.1-1990.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

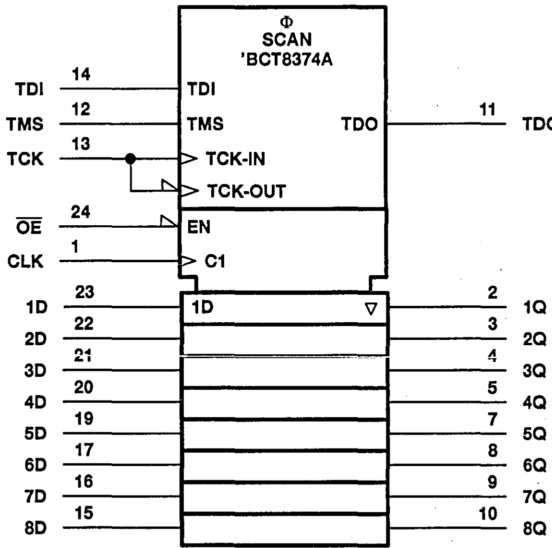
Four dedicated test terminals control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8374A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT8374A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(normal mode, each flip-flop)**

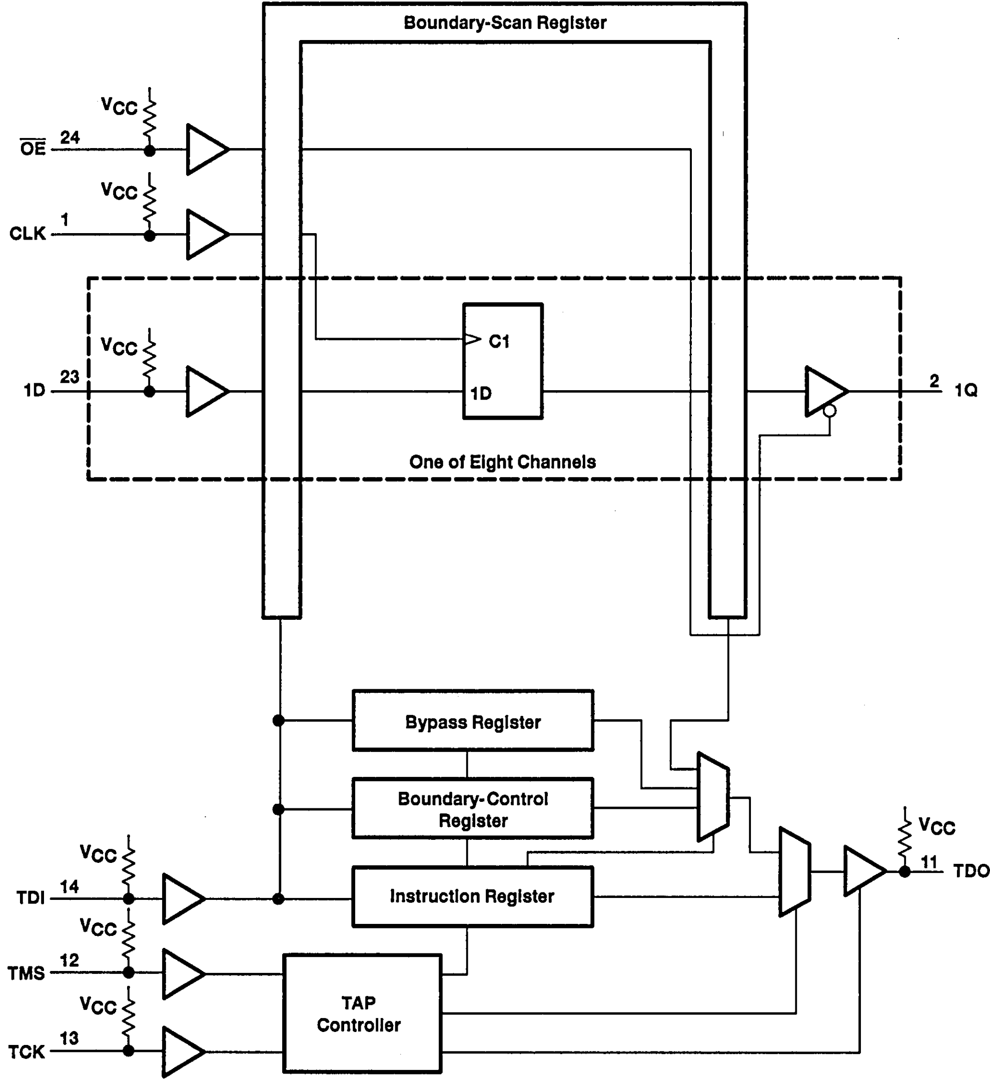
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

## functional block diagram




Pin numbers shown are for the DW, JT, and NT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| CLK | Normal-function clock input. See function table for normal-mode logic. An internal pullup forces CLK to a high level if left unconnected. |
| 1D–8D | Normal-function data inputs. See function table for normal-mode logic. Internal pullups force these inputs to a high level if left unconnected. |
| GND | Ground |
| $\overline{OE}$ | Normal-function output-enable input. See function table for normal-mode logic. An internal pullup forces $\overline{OE}$ to a high level if left unconnected. |
| 1Q–8Q | Normal-function data outputs. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. An internal pullup forces TCK to a high level if left unconnected. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. An internal pullup forces TDO to a high level when it is not active and is not driven from an external source. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. TMS also provides the optional test reset signal of IEEE Standard 1149.1-1990. This is implemented by recognizing a third logic level, double high ($V_{IHH}$), at TMS. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus, or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK, and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and three test-data registers: an 18-bit boundary-scan register, a 2-bit boundary-control register, and a 1-bit bypass register.

Test-Logic-Reset
TMS = H
TMS = L
Run-Test/Idle
TMS = L
TMS = H
Select-DR-Scan
TMS = H
Select-IR-Scan
TMS = H
TMS = L
TMS = L
Capture-DR
TMS = H
TMS = H
Capture-IR
TMS = L
TMS = L
Shift-DR
TMS = L
Shift-IR
TMS = L
TMS = H
TMS = H
TMS = H
Exit1-DR
Exit1-IR
TMS = H
TMS = L
TMS = L
Pause-DR
TMS = L
Pause-IR
TMS = L
TMS = H
TMS = H
TMS = L
Exit2-DR
TMS = L
Exit2-IR
TMS = H
TMS = H
Update-DR
Update-IR
TMS = H
TMS = L
TMS = H
TMS = L

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the ’BCT8374A, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. The boundary-control register is reset to the binary value 10, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic may be actively running a test or may be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register may capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state.

For the 'BCT8374A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

## register overview

With the exception of the bypass register, any test register may be thought of as a serial-shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register may be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 2 lists the instructions supported by the 'BCT8374A. The even-parity feature specified for SCOPE™ devices is not supported in this device. Bit 7 of the instruction opcode is a don't-care bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR order of scan is shown in Figure 2.

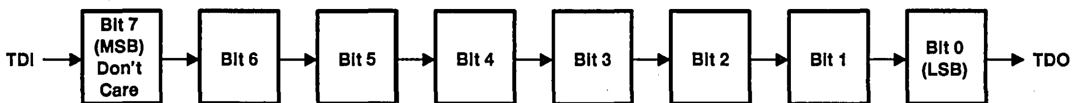



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 18 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function output pin. The BSR is used to 1) store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output terminals, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input terminals.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR may change during Run-Test/Idle as determined by the current instruction. The contents of the BSR are not changed in Test-Logic-Reset.

The BSR order of scan is from TDI through bits 17–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 17 | CLK | 15 | 1D | 7 | 1Q |
| 16 | $\overline{OE}$ | 14 | 2D | 6 | 2Q |
| – | – | 13 | 3D | 5 | 3Q |
| – | – | 12 | 4D | 4 | 4Q |
| – | – | 11 | 5D | 3 | 5Q |
| – | – | 10 | 6D | 2 | 6Q |
| – | – | 9 | 7D | 1 | 7Q |
| – | – | 8 | 8D | 0 | 8Q |

### boundary-control register

The boundary-control register (BCR) is two bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG and PSA. Table 3 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 10, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

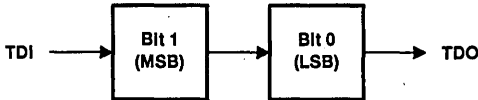



**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

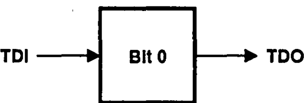



**Figure 4. Bypass Register Order of Scan**

## instruction-register opcode description

The instruction-register opcodes are shown in Table 2. The following descriptions detail the operation of each instruction.

**Table 2. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| X0000000 | EXTEST/INTEST | Boundary scan | Boundary scan | Test |
| X0000001 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| X0000011 | INTEST/EXTEST | Boundary scan | Boundary scan | Test |
| X0000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0000110 | HIGHZ (TRIBYP) | Control boundary to high impedance | Bypass | Modified test |
| X0000111 | CLAMP (SETBYP) | Control boundary to 1/0 | Bypass | Test |
| X0001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| X0001001 | RUNT | Boundary run test | Bypass | Test |
| X0001010 | READBN | Boundary read | Boundary scan | Normal |
| X0001011 | READBT | Boundary read | Boundary scan | Test |
| X0001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| X0001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| X0001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| X0001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is a don't-care bit; X = don't care.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'BCT8374A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output terminals. The device operates in the test mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**sample boundary**

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device output terminals are placed in the high-impedance state, the device input terminals remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output terminals. The device operates in the test mode.

**boundary run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The four test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, and simultaneous PSA and PRPG (PSA/PRPG).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches may be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device output terminals on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input terminals is not captured in the input BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 1–0 as shown in Table 3. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 3. Boundary-Control Register Opcodes**

| BINARY CODE BIT 1 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| 00 | Sample inputs/toggle outputs (TOPSIP) |
| 01 | Pseudo-random pattern generation/16-bit mode (PRPG) |
| 10 | Parallel-signature analysis/16-bit mode (PSA) |
| 11 | Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG) |

It should be noted, in general, that while the control input BSCs (bits 17–16) are not included in the sample, toggle, PSA, or PRPG algorithms, the output-enable BSC (bit 16 of the BSR) does control the drive state (active or high impedance) of the device output terminals.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the device input terminals is captured in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift register elements of the output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK.

## pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the BSCs on each rising edge of TCK and then updated in the shadow latches and applied to the device output terminals on each falling edge of TCK. This data also is updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Figure 5 shows the 16-bit linear-feedback shift-register algorithm through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

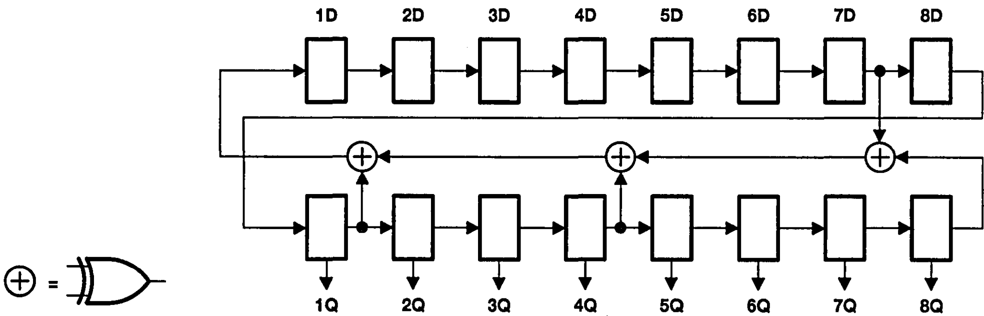



**Figure 5. 16-Bit PRPG Configuration**

### parallel-signature analysis (PSA)

Data appearing at the device input terminals is compressed into a 16-bit parallel signature in the shift-register elements of the BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the output BSCs remains constant and is applied to the device outputs. Figure 6 shows the 16-bit linear-feedback shift-register algorithm through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

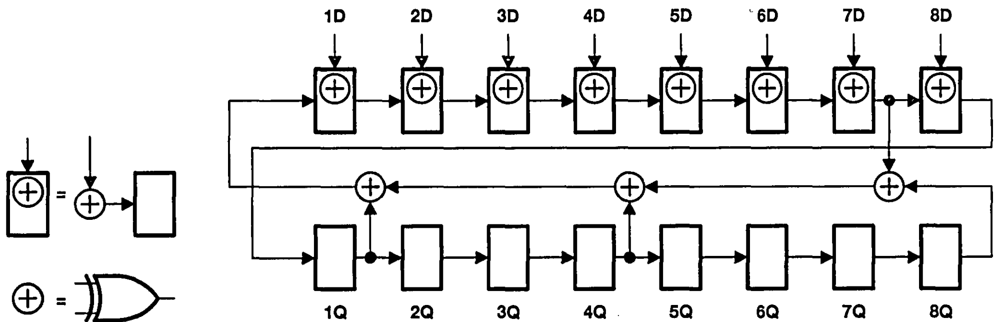



**Figure 6. 16-Bit PSA Configuration**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the device input terminals is compressed into an 8-bit parallel signature in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the device output terminals on each falling edge of TCK. Figure 7 shows the 8-bit linear-feedback shift-register algorithm through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

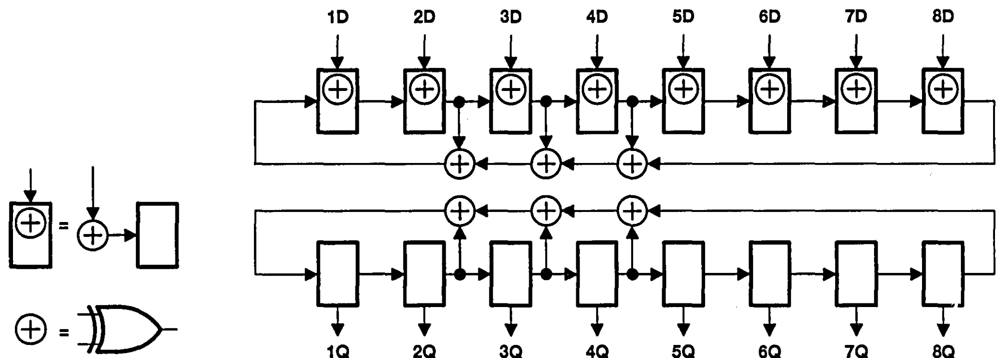



**Figure 7. 8-Bit PSA/PRPG Configuration**

## timing description

All test operations of the 'BCT8374A are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output terminals on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 8. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 4 explains the operation of the test circuitry during each TCK cycle.

**Table 4. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

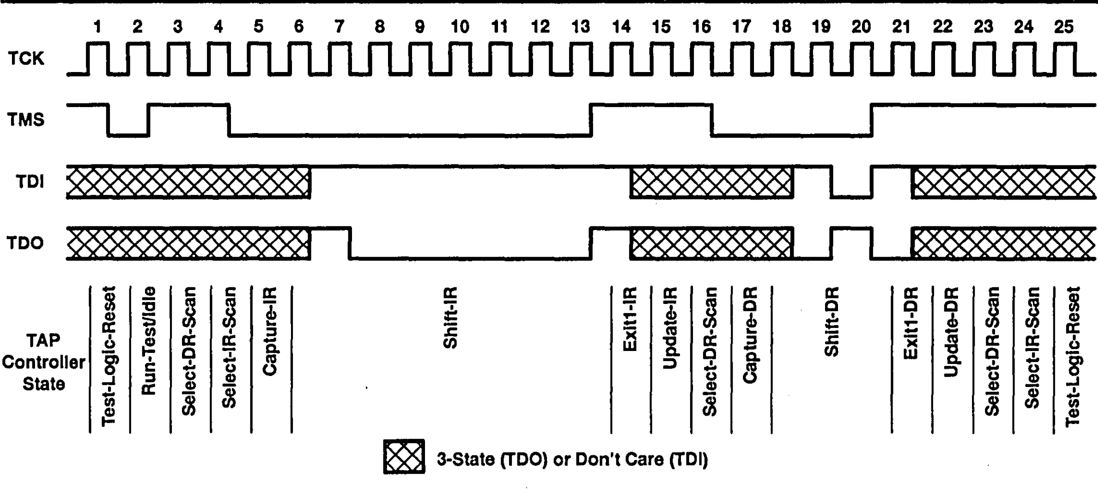



Figure 8. Timing Example

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$: except TMS (see Note 1) | –0.5 V to 7 V |
| TMS (see Note 1) | –0.5 V to 12 V |
| Voltage range applied to any output in the disabled or power-off state | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state | –0.5 V to $V_{CC}$ |
| Input clamp current, $I_{IK}$ | –30 mA |
| Current into any output in the low state: SN54BCT8374A (TDO) | 40 mA |
| SN54BCT8374A (any Q) | 96 mA |
| SN74BCT8374A (TDO) | 48 mA |
| SN74BCT8374A (any Q) | 128 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DW package | 1.7 W |
| NT package | 1.3 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage rating may be exceeded if the input clamp-current rating is observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54BCT8374A | | | SN74BCT8374A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IHH}$ | Double-high-level input voltage | TMS | 10 | | 12 | 10 | | 12 | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | –18 | | | –18 | mA |
| $I_{OH}$ | High-level output current | TDO | | | –3 | | | –3 | mA |
| | | Any Q | | | –12 | | | –15 | |
| $I_{OL}$ | Low-level output current | TDO | | | 20 | | | 24 | mA |
| | | Any Q | | | 48 | | | 64 | |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | SN54BCT8374A MIN | SN54BCT8374A TYP† | SN54BCT8374A MAX | SN74BCT8374A MIN | SN74BCT8374A TYP† | SN74BCT8374A MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | Any Q | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –3 mA | | 2.7 | 3.4 | | 2.7 | 3.4 | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | | 2.4 | 3.4 | | 2.4 | 3.4 | | |
| | | | $I_{OH}$ = –12 mA | | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = –15 mA | | | | | 2 | 3.1 | | |
| | TDO | $V_{CC}$ = 4.75 V, | $I_{OH}$ = –1 mA | | 2.7 | 3.4 | | 2.7 | 3.4 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –1 mA | | 2.5 | 3.4 | | 2.5 | 3.4 | | |
| | | | $I_{OH}$ = –3 mA | | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| $V_{OL}$ | Any Q | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.38 | 0.55 | | | | V |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.42 | 0.55 | |
| | TDO | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | | 0.3 | 0.5 | | | | |
| | | | $I_{OL}$ = 24 mA | | | | | | 0.35 | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | –1 | –35 | –100 | –1 | –35 | –100 | μA |
| $I_{IHH}$ | TMS | $V_{CC}$ = 5.5 V, | $V_I$ = 10 V | | | | 1 | | | 1 | mA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | –30 | –70 | –200 | –30 | –70 | –200 | μA |
| $I_{OZH}$ | Any Q | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 50 | | | 50 | μA |
| | TDO | | | | –1 | –35 | –100 | –1 | –35 | –100 | |
| $I_{OZL}$ | Any Q | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | –50 | | | –50 | μA |
| | TDO | | | | –30 | –70 | –200 | –30 | –70 | –200 | |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 2 V, | $V_O$ = 0.5 V or 2.7 V | | | | ±250 | | | ±250 | μA |
| $I_{OZPD}$ | | $V_{CC}$ = 2 V to 0, | $V_O$ = 0.5 V or 2.7 V | | | | ±250 | | | ±250 | μA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \leq$ 4.5 V | | | | ±250 | | | ±250 | μA |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | | –100 | | –225 | –100 | | –225 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | Outputs open | Outputs high | | 3.5 | 7 | | 3.5 | 7 | mA |
| | | | | Outputs low | | 35 | 52 | | 35 | 52 | |
| | | | | Outputs disabled | | 1.5 | 3.5 | | 1.5 | 3.5 | |
| $C_i$ | | $V_{CC}$ = 5 V, | $V_I$ = 2.5 V or 0.5 V | | | 10 | | | 10 | | pF |
| $C_o$ | | $V_{CC}$ = 5 V, | $V_O$ = 2.5 V or 0.5 V | | | 14 | | | 14 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 9)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54BCT8374A | | SN74BCT8374A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLK | 0 | 70 | 0 | 70 | 0 | 70 | MHz |
| $t_w$ | Pulse duration | CLK high or low | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time | Data before CLK↑ | 3 | | 3 | | 3 | | ns |
| $t_h$ | Hold time | Data after CLK↑ | 2 | | 2 | | 2 | | ns |

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54BCT8374A | | SN74BCT8374A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 20 | 0 | 20 | 0 | 20 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 25 | | 25 | | 25 | | ns |
| | | TMS double high | 50* | | 50* | | 50 | | |
| $t_{su}$ | Setup time | Any D before TCK↑ | 6 | | 6 | | 6 | | ns |
| | | CLK or $\overline{OE}$ before TCK↑ | 6 | | 6 | | 6 | | |
| | | TDI before TCK↑ | 6 | | 6 | | 6 | | |
| | | TMS before TCK↑ | 12 | | 12 | | 12 | | |
| $t_h$ | Hold time | Any D after TCK↑ | 4.5 | | 4.5 | | 4.5 | | ns |
| | | CLK or $\overline{OE}$ after TCK↑ | 4.5 | | 4.5 | | 4.5 | | |
| | | TDI after TCK↑ | 4.5 | | 4.5 | | 4.5 | | |
| | | TMS after TCK↑ | 0 | | 0 | | 0 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 100* | | 100* | | 100 | | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 9)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54BCT8374A | | SN74BCT8374A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLK | | 70 | | | 70 | | 70 | | MHz |
| $t_{PLH}$ | CLK | Q | 3 | 6.7 | 8.5 | 3 | 10.5 | 3 | 10 | ns |
| $t_{PHL}$ | | | 3 | 6.4 | 8 | 3 | 10 | 3 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 3 | 6.5 | 8.5 | 3 | 10.5 | 3 | 10 | ns |
| $t_{PZL}$ | | | 3.5 | 7.5 | 9.5 | 3.5 | 12.5 | 3.5 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 3 | 6.1 | 8 | 3 | 10 | 3 | 9 | ns |
| $t_{PLZ}$ | | | 2.5 | 5.8 | 7.5 | 2.5 | 9.5 | 2.5 | 8.5 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 9)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54BCT8374A | | SN74BCT8374A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 20 | | | 20 | | 20 | | MHz |
| $t_{PLH}$ | TCK↓ | Q | 6 | 13 | 15.5 | 6 | 21.5 | 6 | 20 | ns |
| $t_{PHL}$ | | | 6 | 12.5 | 15.5 | 6 | 21.5 | 6 | 20 | |
| $t_{PLH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 14 | 3.5 | 13 | ns |
| $t_{PHL}$ | | | 3.5 | 8 | 10.5 | 3.5 | 13 | 3.5 | 12 | |
| $t_{PLH}$ | TCK↑ | Q | 7.5 | 16.5 | 20 | 7.5 | 28 | 7.5 | 24 | ns |
| $t_{PHL}$ | | | 7.5 | 17 | 21 | 7.5 | 29 | 7.5 | 25 | |
| $t_{PZH}$ | TCK↓ | Q | 6.5 | 14 | 17 | 6.5 | 24 | 6.5 | 21 | ns |
| $t_{PZL}$ | | | 7 | 15 | 20 | 7 | 26 | 7 | 23 | |
| $t_{PZH}$ | TCK↓ | TDO | 3.5 | 7.6 | 10.5 | 3.5 | 11.5 | 3.5 | 11 | ns |
| $t_{PZL}$ | | | 4 | 8.5 | 11 | 4 | 13.5 | 4 | 12.5 | |
| $t_{PZH}$ | TCK↑ | Q | 8 | 18 | 22 | 8 | 30 | 8 | 27 | ns |
| $t_{PZL}$ | | | 8 | 19 | 25 | 8 | 32 | 8 | 29 | |
| $t_{PHZ}$ | TCK↓ | Q | 6 | 14 | 18 | 6 | 24 | 6 | 22 | ns |
| $t_{PLZ}$ | | | 6 | 14 | 17 | 6 | 23 | 6 | 21 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 8 | 11.5 | 3 | 13 | 3 | 12.5 | ns |
| $t_{PLZ}$ | | | 3 | 7.5 | 10 | 3 | 13 | 3 | 12 | |
| $t_{PHZ}$ | TCK↑ | Q | 8 | 18.5 | 22 | 8 | 31 | 8 | 27 | ns |
| $t_{PLZ}$ | | | 8 | 18.5 | 22 | 8 | 31 | 8 | 27 | |

## PARAMETER MEASUREMENT INFORMATION



NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \le$ 2.5 ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

**Figure 9. Load Circuits and Voltage Waveforms**

General Information 1

SN54/74BCT Octals 2

SN54/74ABT Octals 3

SN54/74ABT Widebus™ With Dual-Sided Terminals 4

SN54/74ABT Widebus™ With Quad-Sided Terminals 5

SN54/74LVT Widebus™ With Dual-Sided Terminals 6

SN54/74LVT Widebus™ With Quad-Sided Terminals 7

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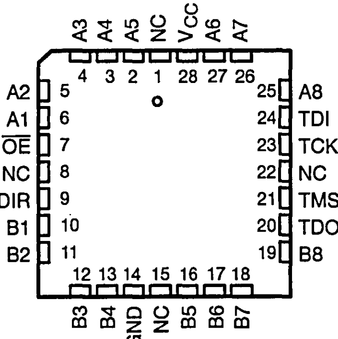
- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to 'F245 and 'ABT245 in the Normal-Function Mode**
- ***SCOPE*™ Instruction Set:**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP, and HIGHZ**
  - **Parallel-Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline Packages (DW), Ceramic Chip Carriers(FK), and Standard Ceramic DIPs (JT)**

**SN54ABT8245 . . . JT PACKAGE**
**SN74ABT8245 . . . DW PACKAGE**
**(TOP VIEW)**

| Pin name | Pin | Pin | Pin name |
|---|---|---|---|
| DIR | 1 | 24 | $\overline{OE}$ |
| B1 | 2 | 23 | A1 |
| B2 | 3 | 22 | A2 |
| B3 | 4 | 21 | A3 |
| B4 | 5 | 20 | A4 |
| GND | 6 | 19 | A5 |
| B5 | 7 | 18 | $V_{CC}$ |
| B6 | 8 | 17 | A6 |
| B7 | 9 | 16 | A7 |
| B8 | 10 | 15 | A8 |
| TDO | 11 | 14 | TDI |
| TMS | 12 | 13 | TCK |

**SN54ABT8245 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'ABT8245 scan test devices with octal bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the 'F245 and 'ABT245 octal bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at DIR. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary-scan test operations as described in IEEE Standard 1149.1-1990.

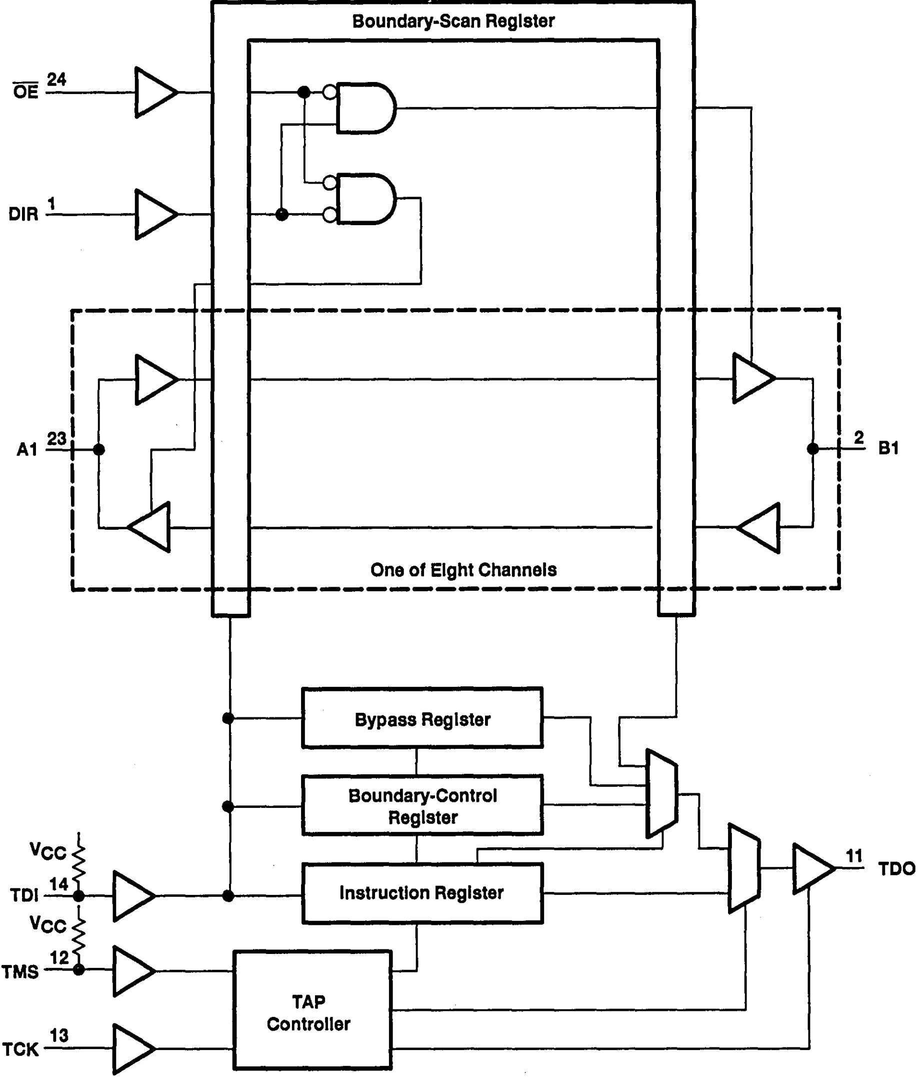
Four dedicated test pins control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8245 is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74ABT8245 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(normal mode)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## functional block diagram




Pin numbers shown are for the DW and JT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A1–A8 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| B1–B8 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| DIR | Normal-function direction-control input. See function table for normal-mode logic. |
| GND | Ground |
| $\overline{OE}$ | Normal-function output-enable input. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS input directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and three test-data registers: a 36-bit boundary-scan register, an 11-bit boundary-control register, and a 1-bit bypass register.

Test-Logic-Reset
TMS = H
TMS = L
Run-Test/Idle
TMS = L
TMS = H
Select-DR-Scan
TMS = H
Select-IR-Scan
TMS = H
TMS = L
Capture-DR
TMS = H
TMS = H
Capture-IR
TMS = L
TMS = L
Shift-DR
TMS = L
Shift-IR
TMS = L
TMS = H
TMS = H
TMS = H
Exit1-DR
TMS = H
Exit1-IR
TMS = L
TMS = L
Pause-DR
TMS = L
Pause-IR
TMS = L
TMS = H
TMS = H
TMS = L
Exit2-DR
TMS = L
Exit2-IR
TMS = H
TMS = H
Update-DR
Update-IR
TMS = H
TMS = L
TMS = H
TMS = L

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8245, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0. The boundary-control register is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state can also be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state.

For the 'ABT8245, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

## register overview

With the exception of the bypass register, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8245. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction.

The IR order of scan is shown in Figure 2.

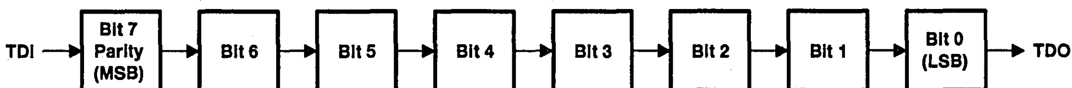



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 36 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, two BSCs for each normal-function I/O pin (one for input data and one for output data), and one BSC for each of the internally decoded output-enable signals (OEA and OEB). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0.

When external data is to be captured, the BSCs for signals OEA and OEB capture logic values determined by the following positive-logic equations: OEA = $\overline{OE}$ • $\overline{DIR}$, and OEB = $\overline{OE}$ • DIR. When data is to be applied externally, these BSCs control the drive state (active or high-impedance) of their respective outputs.

The BSR order of scan is from TDI through bits 35–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|---|---|---|---|
| 35 | OEB | 31 | B8-I | 23 | B8-O | 15 | A8-I | 7 | A8-O |
| 34 | OEA | 30 | B7-I | 22 | B7-O | 14 | A7-I | 6 | A7-O |
| 33 | DIR | 29 | B6-I | 21 | B6-O | 13 | A6-I | 5 | A6-O |
| 32 | $\overline{OE}$ | 28 | B5-I | 20 | B5-O | 12 | A5-I | 4 | A5-O |
| — | — | 27 | B4-I | 19 | B4-O | 11 | A4-I | 3 | A4-O |
| — | — | 26 | B3-I | 18 | B3-O | 10 | A3-I | 2 | A3-O |
| — | — | 25 | B2-I | 17 | B2-O | 9 | A2-I | 1 | A2-O |
| — | — | 24 | B1-I | 16 | B1-O | 8 | A1-I | 0 | A1-O |

### boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA with input masking, and binary count up (COUNT). Table 4 shows the test operations decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The BCR order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the BCR bits and their associated test control signals.

**Table 2. Boundary-Control Register Configuration**

| BCR BIT NUMBER | TEST CONTROL SIGNAL | BCR BIT NUMBER | TEST CONTROL SIGNAL | BCR BIT NUMBER | TEST CONTROL SIGNAL |
|---|---|---|---|---|---|
| 10 | MASK8 | 6 | MASK4 | 2 | OPCODE2 |
| 9 | MASK7 | 5 | MASK3 | 1 | OPCODE1 |
| 8 | MASK6 | 4 | MASK2 | 0 | OPCODE0 |
| 7 | MASK5 | 3 | MASK1 | — | — |

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 3.

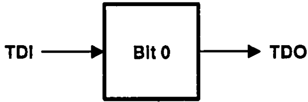



**Figure 3. Bypass Register Order of Scan**

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST/INTEST | Boundary scan | Boundary scan | Test |
| 10000001 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | INTEST/EXTEST | Boundary scan | Boundary scan | Test |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT8245.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

### control boundary to high impedance

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

### control boundary to 1/0

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

### boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

### boundary read

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

### boundary self test

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

### boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

### boundary-control register scan

The BCR is selected in the scan path. The value in the boundary-control register remains unchanged during Capture-DR. This operation must be performed before a boundary run test operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/16-bit mode (PRPG) |
| X10 | Parallel-signature analysis/16-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT) |

It should be noted, in general, that while the control input BSCs (bits 35–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 35–34 of the BSR) do control the drive state (active or high impedance) of the selected device output pins. It also should be noted that these BCR instructions are only valid when the device is operating in one direction of data flow (that is, $\overline{OEA} \neq \overline{OEB}$). Otherwise, the bypass instruction is operated.

### PSA input masking

Bits 10–3 of the BCR specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins, in order, from most significant to least significant, as indicated in Table 3. When the mask bit that corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

### sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. This data also is updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Figures 4 and 5 illustrate the 16-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. Note that a seed value of all zeroes does not produce additional patterns.

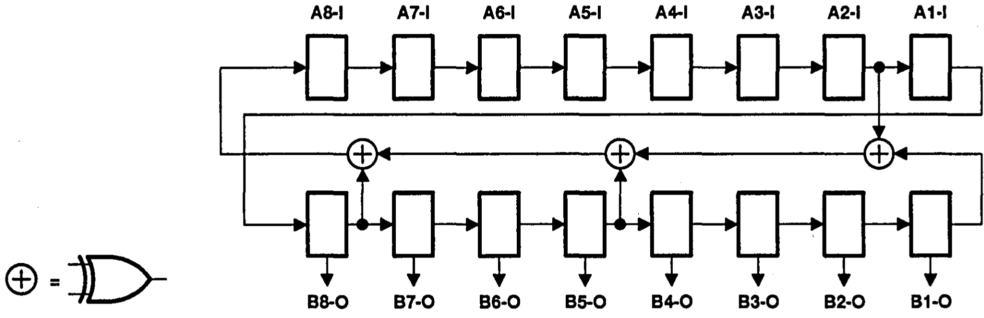



Figure 4. 16-Bit PRPG Configuration (OEA = 0, OEB = 1)

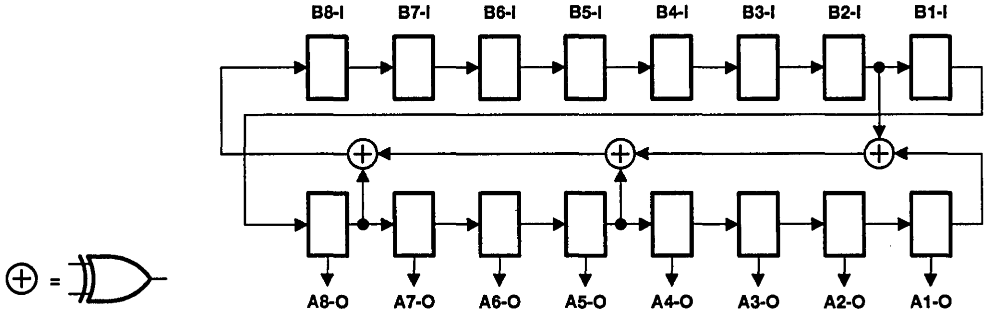



Figure 5. 16-Bit PRPG Configuration (OEA = 1, OEB = 0)

### parallel-signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 6 and 7 illustrate the 16-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

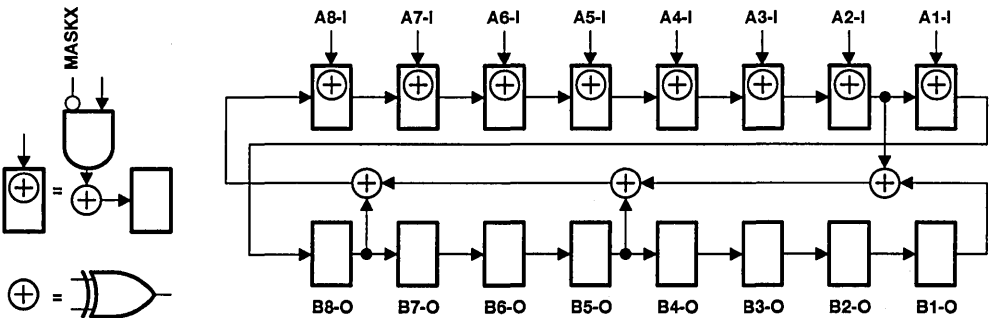



**Figure 6. 16-Bit PSA Configuration (OEA = 0, OEB = 1)**

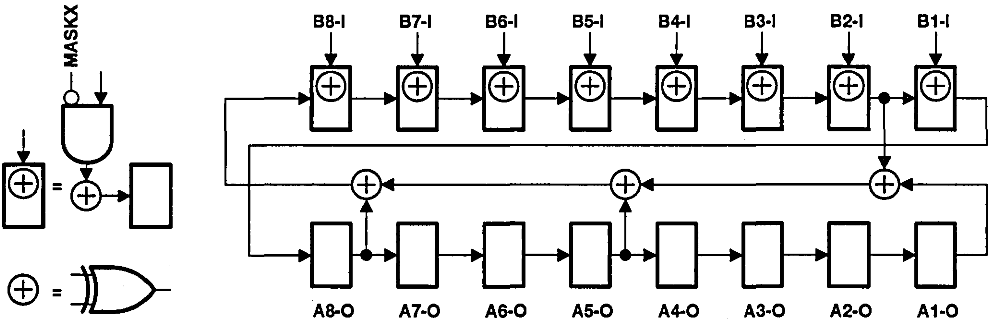



**Figure 7. 16-Bit PSA Configuration (OEA = 1, OEB = 0)**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. Figures 8 and 9 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. Note that a seed value of all zeroes does not produce additional patterns.

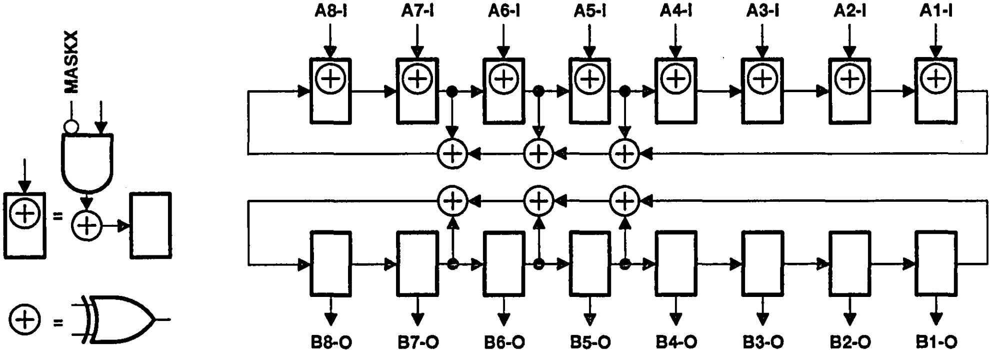



**Figure 8. 8-Bit PSA/PRPG Configuration (OEA = 0, OEB = 1)**

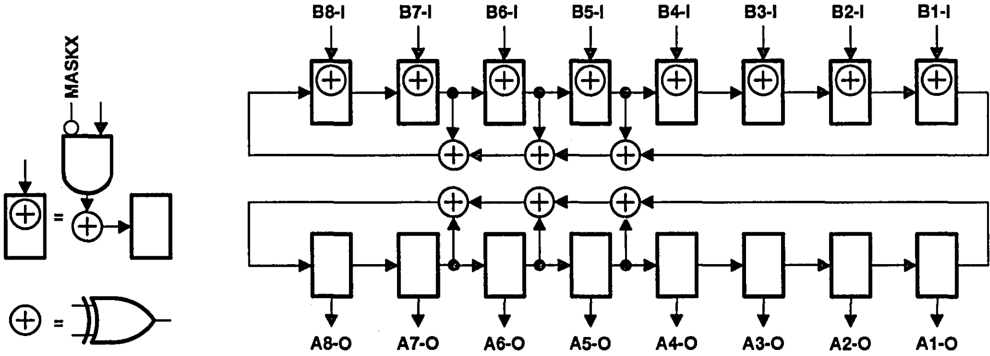



**Figure 9. 8-Bit PSA/PRPG Configuration (OEA = 1, OEB = 0)**

**simultaneous PSA and binary count up (PSA/COUNT)**

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. In addition, the shift-register elements of the opposite output BSCs are used to count carries out of the selected output BSCs and, thereby, extend the count to 16 bits. Figures 10 and 11 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

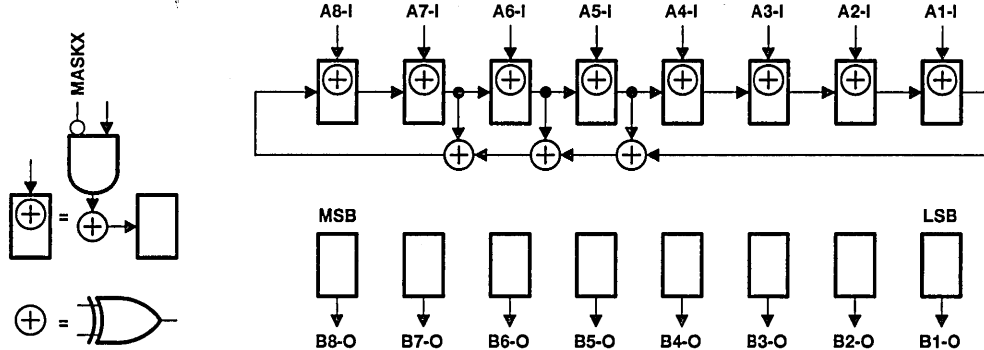



**Figure 10. 8-Bit PSA/COUNT Configuration (OEA = 0, OEB = 1)**

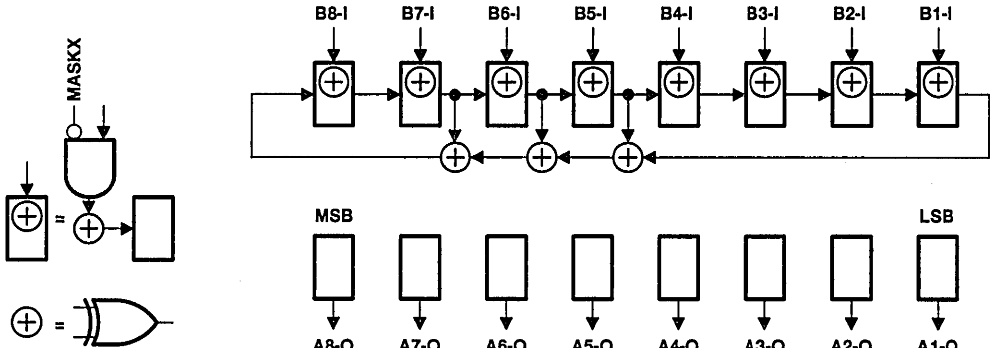



**Figure 11. 8-Bit PSA/COUNT Configuration (OEA = 1, OEB = 0)**

## timing description

All test operations of the 'ABT8245 are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 12. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

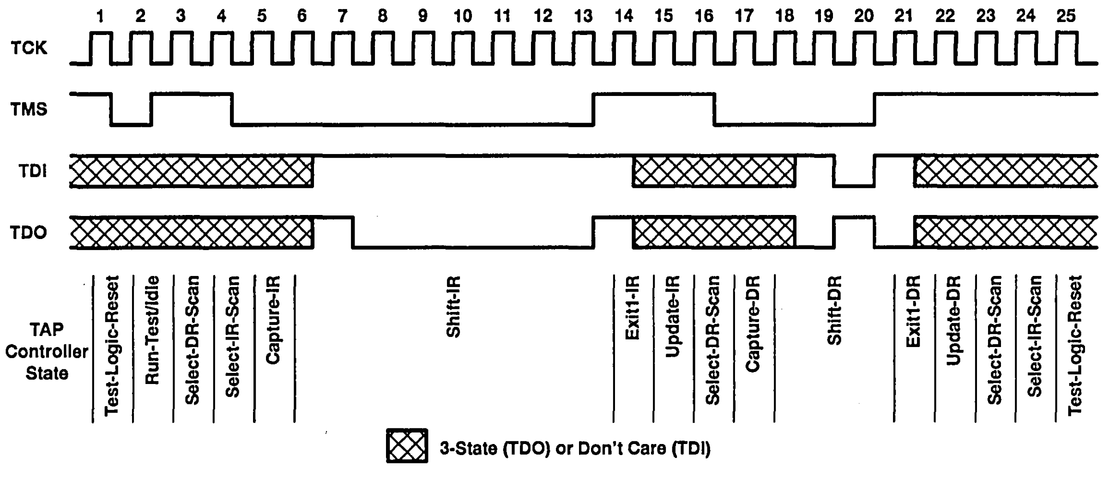



**Figure 12. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$ (except I/O ports) (see Note 1) | –0.5 V to 7 V |
| Input voltage range, $V_I$ (I/O ports) (see Note 1) | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$: SN54ABT8245 | 96 mA |
| SN74ABT8245 | 128 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | –18 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | –50 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DW package | 1.7 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions (see Note 3)

| | | SN54ABT8245 | | SN74ABT8245 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | $T_A$ = 25°C | | | SN54ABT8245 | | SN74ABT8245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 3 mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | $V_{CC}$ = 5 V, | $I_{OH}$ = – 3 mA | | 3 | | | 3 | | 3 | | |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 24 mA | | 2 | | | 2 | | | | |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 32 mA | | 2* | | | | | 2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | | | 0.55 | | 0.55 | | | V |
| | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 64 mA | | | | 0.55* | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | DIR, $\overline{OE}$, TCK | | | ±1 | | ±1 | | ±1 | µA |
| | | | A or B ports | | | ±100 | | ±100 | | ±100 | |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | TDI, TMS | | | 10 | | 10 | | 10 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = GND | TDI, TMS | –40 | | –160 | –40 | –160 | –40 | –160 | µA |
| $I_{OZH}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | –50 | | –50 | | –50 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 2 V, | $V_O$ = 0.5 V or 2.7 V | | | | ±50 | | ±50 | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 2 V or 0, | $V_O$ = 0.5 V or 2.7 V | | | | ±50 | | ±50 | | ±50 | µA |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | | –50 | –100 | –180 | –50 | –180 | –50 | –180 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | Outputs high | | 0.9 | 2 | | 2 | | 2 | mA |
| | | | Outputs low | | 30 | 38 | | 38 | | 38 | |
| | | | Outputs disabled | | 0.9 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = 2.5 V or 0.5 V | | Control inputs | | 3 | | | | | | pF |
| $C_{io}$ | $V_O$ = 2.5 V or 0.5 V | | A or B ports | | 10 | | | | | | pF |
| $C_o$ | $V_O$ = 2.5 V or 0.5 V | | TDO | | 8 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed 1 second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

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## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

| | | | SN54ABT8245 | | SN74ABT8245 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 5 | | 5 | | ns |
| $t_{su}$ | Setup time | A or B or DIR or $\overline{OE}$ before TCK↑ | 7 | | 5 | | ns |
| | | TDI before TCK↑ | 6 | | 6 | | |
| | | TMS before TCK↑ | 6 | | 6 | | |
| $t_h$ | Hold time | A or B or DIR or $\overline{OE}$ after TCK↑ | 0 | | 0 | | ns |
| | | TDI after TCK↑ | 0 | | 0 | | |
| | | TMS after TCK↑ | 0 | | 0 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50* | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1* | | 1 | | µs |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT8245 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | 2 | 3.5 | 4.6 | 2 | 5.8 | ns |
| $t_{PHL}$ | | | 2 | 3.4 | 4.5 | 2 | 5.5 | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | 2.5 | 4.5 | 5.8 | 2.5 | 6.9 | ns |
| $t_{PZL}$ | | | 3 | 5.2 | 6.6 | 3 | 8.1 | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | 3 | 6.1 | 7.6 | 3 | 8.9 | ns |
| $t_{PLZ}$ | | | 3 | 5.5 | 6.9 | 3 | 8 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT8245 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | 2 | 3.5 | 4.3 | 2 | 4.8 | ns |
| $t_{PHL}$ | | | 2 | 3.4 | 4.2 | 2 | 5.1 | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | 2.5 | 4.5 | 5.5 | 2.5 | 6.8 | ns |
| $t_{PZL}$ | | | 3 | 5.2 | 6 | 3 | 7.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | 3 | 6.1 | 7.1 | 3 | 8.4 | ns |
| $t_{PLZ}$ | | | 3 | 5.5 | 6.6 | 3 | 7.5 | |

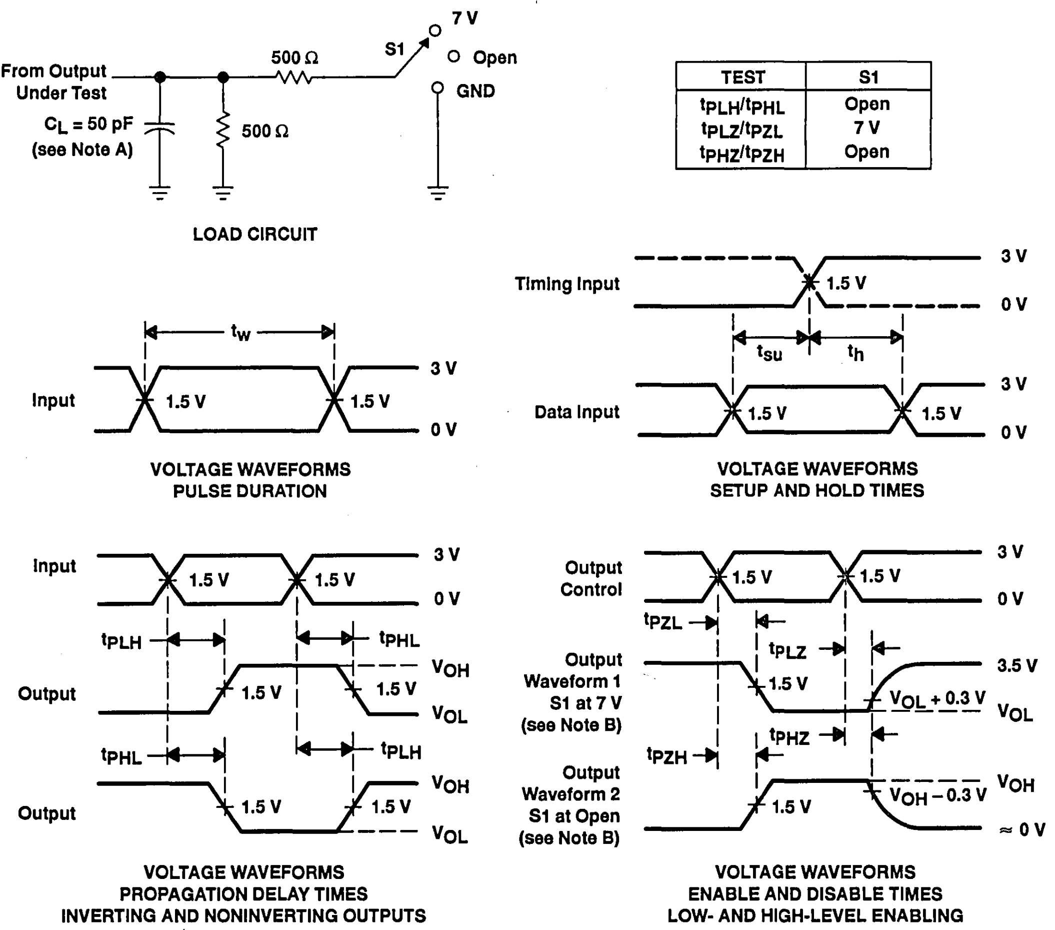
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT8245 $V_{CC}$ = 5 V, $T_A$ = 25°C MIN | TYP | MAX | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3.5 | 8 | 9.5 | 3.5 | 12.5 | ns |
| $t_{PHL}$ | | | 3 | 7.7 | 9 | 3 | 12 | |
| $t_{PLH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 7 | ns |
| $t_{PHL}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 7 | |
| $t_{PZH}$ | TCK↓ | A or B | 4.5 | 8.2 | 9.8 | 4.5 | 12.5 | ns |
| $t_{PZL}$ | | | 4.5 | 9 | 10.5 | 4.5 | 13.5 | |
| $t_{PZH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 7 | ns |
| $t_{PZL}$ | | | 2.5 | 4.9 | 6.3 | 2.5 | 7.8 | |
| $t_{PHZ}$ | TCK↓ | A or B | 3.5 | 8.4 | 11.2 | 3.5 | 14.2 | ns |
| $t_{PLZ}$ | | | 3 | 8 | 10.5 | 3 | 13.5 | |
| $t_{PHZ}$ | TCK↓ | TDO | 2 | 5.9 | 7 | 2 | 9 | ns |
| $t_{PLZ}$ | | | 3 | 5 | 6.5 | 3 | 8 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)**

| PARAMETER | FROM (INPUT) FROM (INPUT) | TO (OUTPUT) TO (OUTPUT) | SN74ABT8245 $V_{CC}$ = 5 V, $T_A$ = 25°C MIN | TYP | MAX | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3.5 | 8 | 9.5 | 3.5 | 12 | ns |
| $t_{PHL}$ | | | 3 | 7.7 | 9 | 3 | 11.5 | |
| $t_{PLH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 6.5 | ns |
| $t_{PHL}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 6.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4.5 | 8.2 | 9.5 | 4.5 | 12 | ns |
| $t_{PZL}$ | | | 4.5 | 9 | 10.5 | 4.5 | 13 | |
| $t_{PZH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 6.5 | ns |
| $t_{PZL}$ | | | 2.5 | 4.9 | 6 | 2.5 | 7 | |
| $t_{PHZ}$ | TCK↓ | A or B | 3.5 | 8.4 | 10.5 | 3.5 | 13.5 | ns |
| $t_{PLZ}$ | | | 3 | 8 | 10.5 | 3 | 13 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.9 | 7 | 3 | 8.5 | ns |
| $t_{PLZ}$ | | | 3 | 5 | 6.5 | 3 | 7.5 | |

## PARAMETER MEASUREMENT INFORMATION

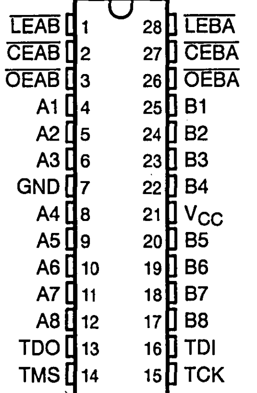



NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

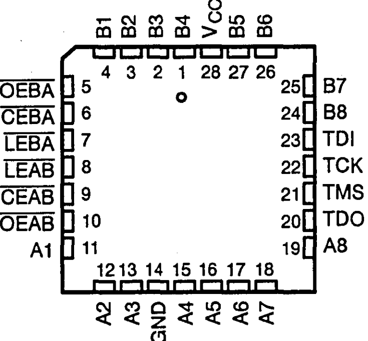
**Figure 13. Load Circuit and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Functionally Equivalent to 'F543 and 'ABT543 in the Normal-Function Mode
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP, and HIGHZ
  - Parallel-Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Even-Parity Opcodes
- Two Boundary-Scan Cells Per I/O for Greater Flexibility
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DL) Packages, Ceramic Chip Carriers (FK), and Standard Ceramic DIPs (JT)

SN54ABT8543 . . . JT PACKAGE
SN74ABT8543 . . . DL OR DW PACKAGE
(TOP VIEW)




SN54ABT8543 . . . FK PACKAGE
(TOP VIEW)




## description

The 'ABT8543 scan test devices with octal registered bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the 'F543 and 'ABT543 octal registered bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self-test on the boundary-test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal registered bus transceivers.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

Data flow in each direction is controlled by latch-enable (LEAB and LEBA), chip-enable (CEAB and CEBA), and output-enable (OEAB and OEBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB and CEAB are both low. When either LEAB or CEAB is high, the A data is latched. The B outputs are active when OEAB and CEAB are both low. When either OEAB or CEAB is high, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B, but uses LEBA, CEBA, and OEBA.

In the test mode, the normal operation of the SCOPE™ registered bus transceiver is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8543 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE†**
**(normal mode, each register)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| CEAB | OEAB | LEAB | A | B |
| L | L | L | L | L |
| L | L | L | H | H |
| L | L | H | X | $B_0$‡ |
| L | H | X | X | Z |
| H | X | X | X | Z |

† A-to-B data flow is shown. B-to-A data flow is similar but uses CEBA, OEBA, and LEBA.
‡ Output level before the indicated steady-state input conditions were established

## functional block diagram

Boundary-Scan Register

OEBA 26
CEBA 27
LEBA 28
OEAB 3
CEAB 2
LEAB 1

C1
1D

A1 4

C1
1D

25 B1

One of Eight Channels

Bypass Register

Boundary-Control Register

VCC
TDI 16
VCC
TMS 14
TCK 15

Instruction Register

TAP Controller

13 TDO

Pin numbers shown are for the DL, DW, and JT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A1–A8 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| B1–B8 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| $\overline{CEAB}$, $\overline{CEBA}$ | Normal-function chip-enable inputs. See function table for normal-mode logic. |
| GND | Ground |
| $\overline{LEAB}$, $\overline{LEBA}$ | Normal-function latch-enable inputs. See function table for normal-mode logic. |
| $\overline{OEAB}$, $\overline{OEBA}$ | Normal-function output-enable inputs. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and three test-data registers: a 40-bit boundary-scan register, an 11-bit boundary-control register, and a 1-bit bypass register.

Test-Logic-Reset
TMS = H
TMS = L
Run-Test/Idle
TMS = L
TMS = H
Select-DR-Scan
TMS = H
Select-IR-Scan
TMS = H
TMS = L
Capture-DR
TMS = H
TMS = H
Capture-IR
TMS = L
Shift-DR
TMS = L
Shift-IR
TMS = L
TMS = H
Exit1-DR
TMS = H
Exit1-IR
TMS = H
TMS = L
Pause-DR
TMS = L
Pause-IR
TMS = L
TMS = H
Exit2-DR
TMS = L
TMS = L
Exit2-IR
TMS = H
Update-DR
Update-IR
TMS = H
TMS = L
TMS = H
TMS = L

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8543, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0. The boundary-control register is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state.

For the 'ABT8543, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass register, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8543. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR order of scan is shown in Figure 2.

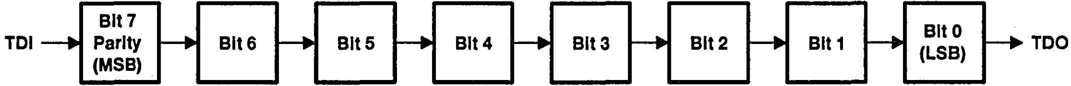



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 40 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, two BSCs for each normal-function I/O pin (one for input data and one for output data), and one BSC for each of the internally decoded output-enable signals (OEA and OEB). The BSR is used to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0.

When external data is to be captured, the BSCs for signals OEA and OEB capture logic values determined by the following positive-logic equations: $OEA = \overline{\overline{OEBA} + \overline{CEBA}}$, and $OEB = \overline{\overline{OEAB} + \overline{CEAB}}$. When data is to be applied externally, these BSCs control the drive state (active or high-impedance) of their respective outputs.

The BSR order of scan is from TDI through bits 39–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|---|---|---|---|
| 39 | OEB | 31 | A8-I | 23 | A8-O | 15 | B8-I | 7 | B8-O |
| 38 | OEA | 30 | A7-I | 22 | A7-O | 14 | B7-I | 6 | B7-O |
| 37 | $\overline{OEAB}$ | 29 | A6-I | 21 | A6-O | 13 | B6-I | 5 | B6-O |
| 36 | $\overline{OEBA}$ | 28 | A5-I | 20 | A5-O | 12 | B5-I | 4 | B5-O |
| 35 | $\overline{LEAB}$ | 27 | A4-I | 19 | A4-O | 11 | B4-I | 3 | B4-O |
| 34 | $\overline{LEBA}$ | 26 | A3-I | 18 | A3-O | 10 | B3-I | 2 | B3-O |
| 33 | $\overline{CEAB}$ | 25 | A2-I | 17 | A2-O | 9 | B2-I | 1 | B2-O |
| 32 | $\overline{CEBA}$ | 24 | A1-I | 16 | A1-O | 8 | B1-I | 0 | B1-O |

### boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The BCR order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the BCR bits and their associated test control signals.

**Table 2. Boundary-Control Register Configuration**

| BCR BIT NUMBER | TEST CONTROL SIGNAL | BCR BIT NUMBER | TEST CONTROL SIGNAL | BCR BIT NUMBER | TEST CONTROL SIGNAL |
|---|---|---|---|---|---|
| 10 | MASK8 | 6 | MASK4 | 2 | OPCODE2 |
| 9 | MASK7 | 5 | MASK3 | 1 | OPCODE1 |
| 8 | MASK6 | 4 | MASK2 | 0 | OPCODE0 |
| 7 | MASK5 | 3 | MASK1 | — | — |

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 3.

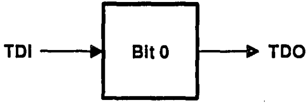



**Figure 3. Bypass Register Order of Scan**

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST/INTEST | Boundary scan | Boundary scan | Test |
| 10000001 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | INTEST/EXTEST | Boundary scan | Boundary scan | Test |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT8543.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

### control boundary to high impedance

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

### control boundary to 1/0

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

### boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

### boundary read

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

### boundary self test

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

### boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

### boundary-control-register scan

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/16-bit mode (PRPG) |
| X10 | Parallel-signature analysis/16-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT) |

In general, while the control input BSCs (bits 39–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 39–38 of the BSR) do control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when the device is operating in one direction of data flow (that is, OEA ≠ OEB). Otherwise, the bypass instruction is operated.

### PSA input masking

Bits 10–3 of the BCR specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins, in order, from most significant to least significant, as indicated in Table 3. When the mask bit that corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, i.e., the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

### sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. This data also is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Figures 4 and 5 show the 16-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

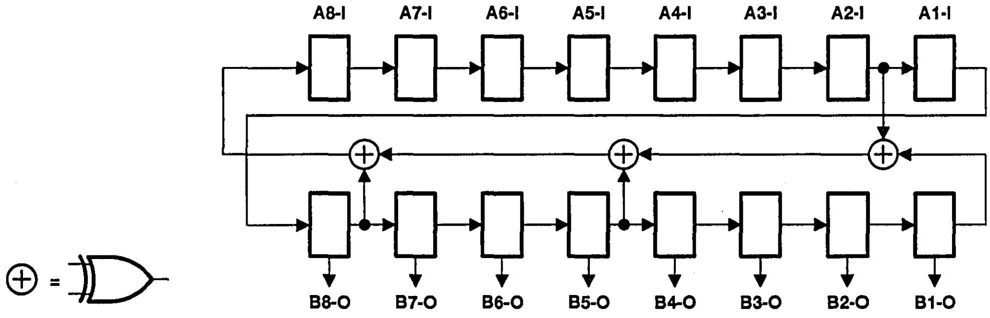



**Figure 4. 16-Bit PRPG Configuration (OEA = 0, OEB = 1)**

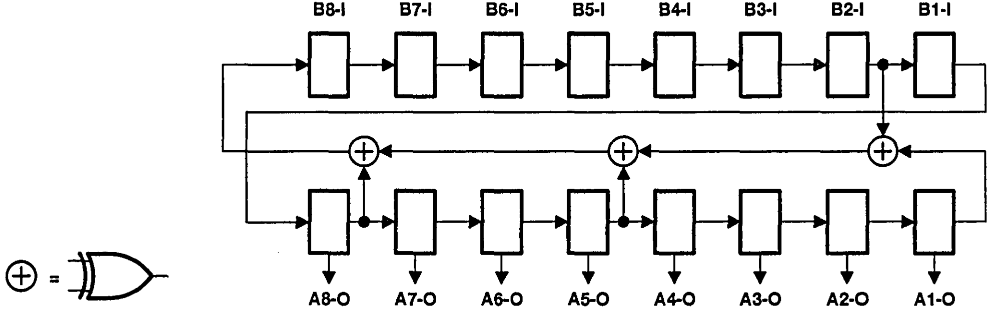



**Figure 5. 16-Bit PRPG Configuration (OEA=1, OEB= 0)**

### parallel-signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 6 and 7 show the 16-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

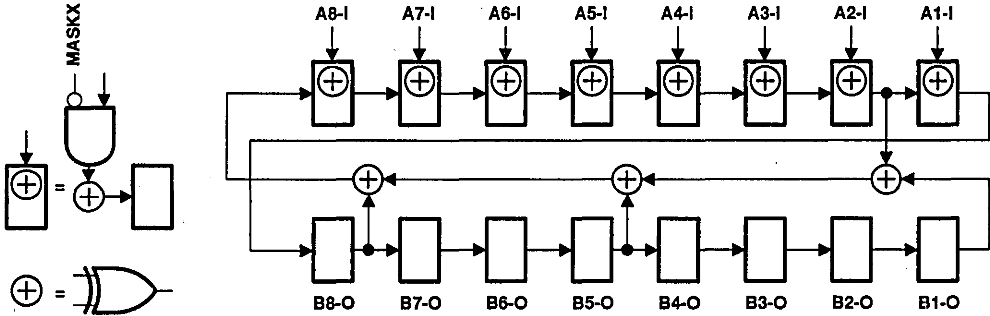



**Figure 6. 16-Bit PSA Configuration (OEA = 0, OEB = 1)**

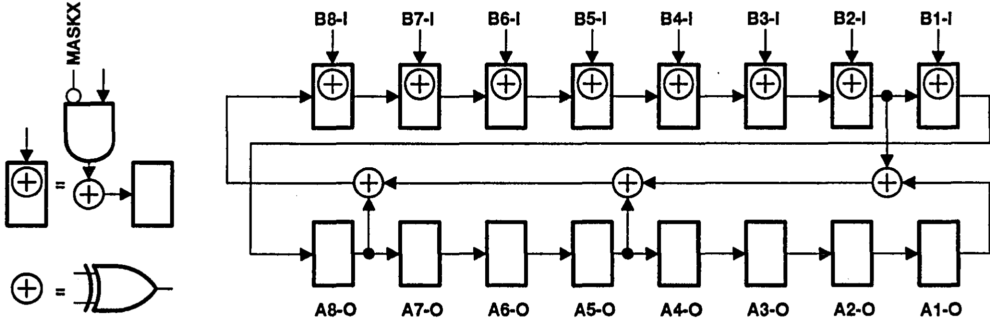



**Figure 7. 16-Bit PSA Configuration (OEA = 1, OEB = 0)**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. Figures 8 and 9 show the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

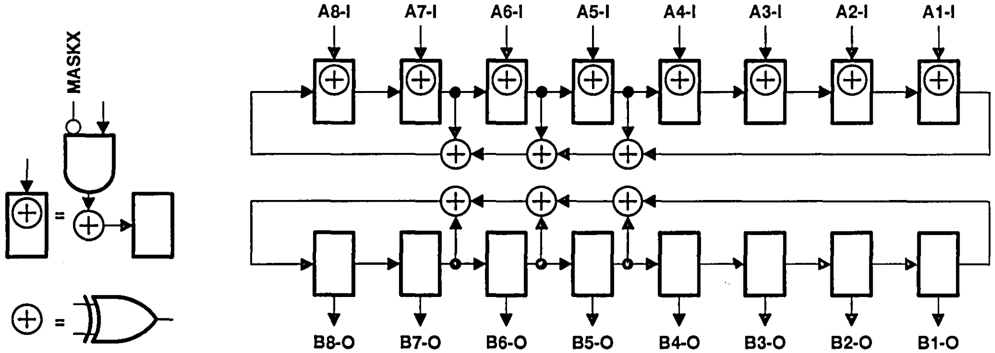



**Figure 8. 8-Bit PSA/PRPG Configuration (OEA = 0, OEB = 1)**

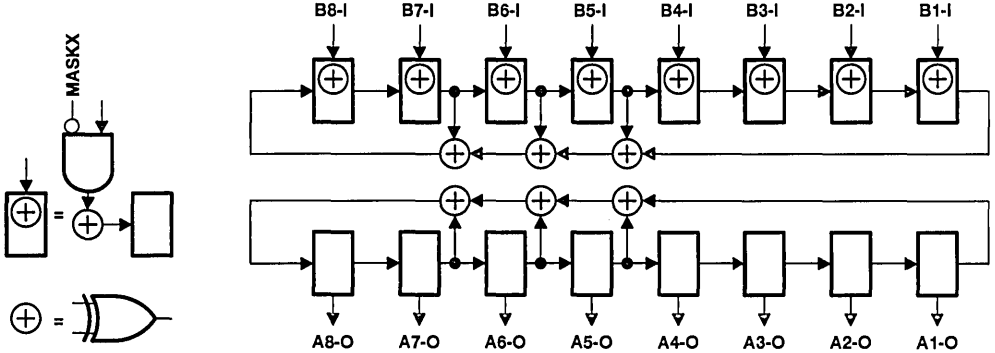



**Figure 9. 8-Bit PSA/PRPG Configuration (OEA = 1, OEB = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. The shift-register elements of the opposite output BSCs count carries out of the selected output BSCs, extending the count to 16 bits. Figures 10 and 11 show the 8-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

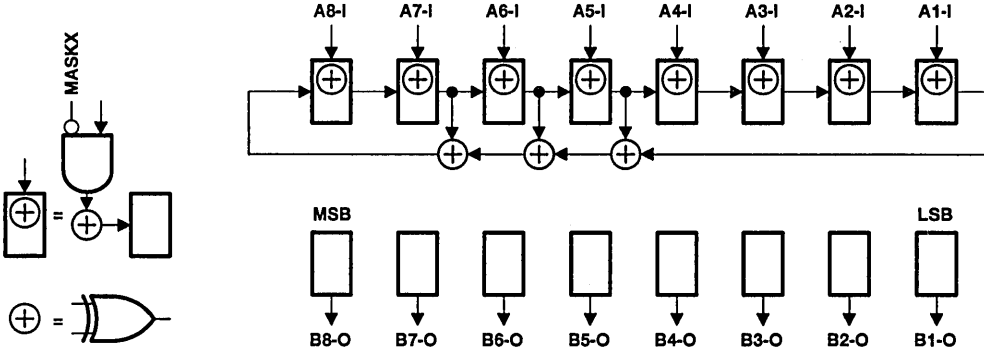



**Figure 10. 8-Bit PSA/COUNT Configuration (OEA = 0, OEB = 1)**

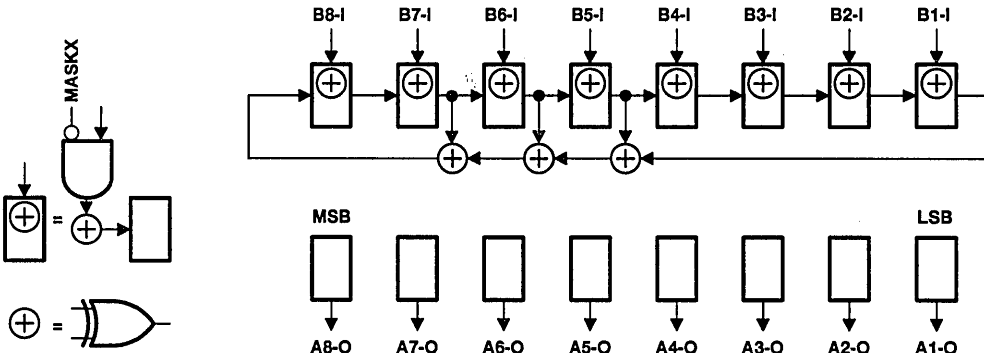



**Figure 11. 8-Bit PSA/COUNT Configuration (OEA = 1, OEB = 0)**

## timing description

All test operations of the 'ABT8543 are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 12. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, as necessary, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

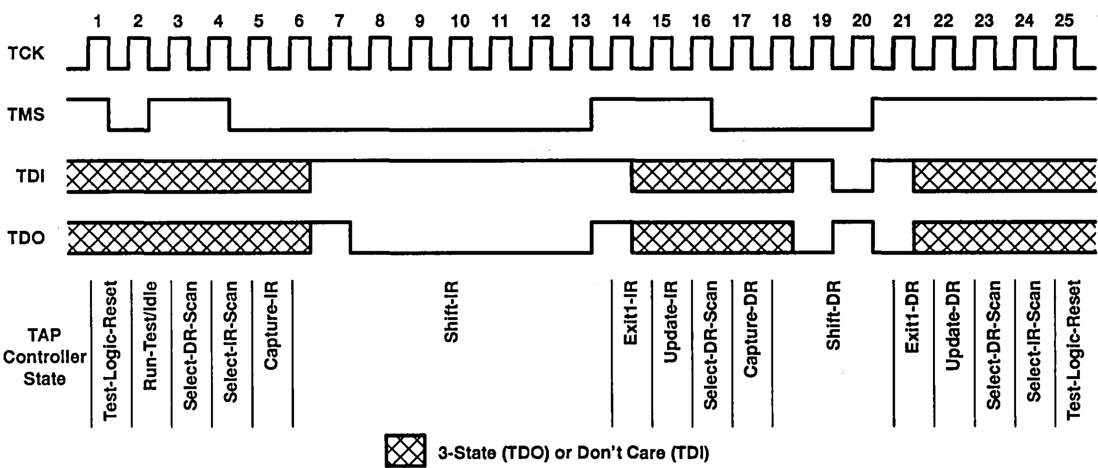



**Figure 12. Timing Example**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$: except I/O ports (see Note 1) | –0.5 V to 7 V |
| I/O ports (see Note 1) | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$: SN54ABT8543 | 96 mA |
| SN74ABT8543 | 128 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | –18 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | –50 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DL package | 0.7 W |
| DW package | 1.7 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions (see Note 3)

| | | SN54ABT8543 | | SN74ABT8543 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT8543 | | SN74ABT8543 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $I_I$ | $\overline{CE}$, $\overline{LE}$, $\overline{OE}$, TCK | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±100 | | ±100 | | ±100 | |
| $I_{IH}$ | TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | | 10 | µA |
| $I_{IL}$ | TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –160 | –40 | –160 | –40 | –160 | µA |
| $I_{OZH}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | | –50 | | –50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±100 | | | | ±100 | µA |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 2 V, | $V_O$ = 0.5 V or 2.7 V | | | ±50 | | ±50 | | ±50 | µA |
| $I_{OZPD}$ | | $V_{CC}$ = 2 V to 0, | $V_O$ = 0.5 V or 2.7 V | | | ±50 | | ±50 | | ±50 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –100 | –180 | –50 | –180 | –50 | –180 | mA |
| $I_{CC}$ | A or B ports | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.9 | 2 | | 2 | | 2 | mA |
| | | | Outputs low | | 30 | 38 | | 38 | | 38 | |
| | | | Outputs disabled | | 0.9 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 3 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

| | | | SN54ABT8543 | | SN74ABT8543 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | LEAB or LEBA high or low | 3 | | 3 | | ns |
| $t_{su}$ | Setup time | A before $\overline{LEAB}$↑ or B before $\overline{LEBA}$↑ | 3.5 | | 3 | | ns |
| $t_h$ | Hold time | A after $\overline{LEAB}$↑ or B after $\overline{LEBA}$↑ | 1.5 | | 0.5 | | ns |

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

| | | | SN54ABT8543 | | SN74ABT8543 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 5 | | 5 | | ns |
| $t_{su}$ | Setup time | A or B or $\overline{CE}$ or $\overline{LE}$ or $\overline{OE}$ before TCK↑ | 6 | | 5 | | ns |
| | | TDI before TCK↑ | 6.5 | | 6 | | |
| | | TMS before TCK↑ | 6 | | 6 | | |
| $t_h$ | Hold time | A or B or $\overline{CE}$ or $\overline{LE}$ or $\overline{OE}$ after TCK↑ | 0.5 | | 0 | | ns |
| | | TDI after TCK↑ | 0 | | 0 | | |
| | | TMS after TCK↑ | 0 | | 0 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50* | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1* | | 1 | | µs |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT8543 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | 2 | 3.7 | 4.7 | 2 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.5 | 4.4 | 1.5 | 5.8 | |
| $t_{PLH}$ | $\overline{LEAB}$ or $\overline{LEBA}$ | B or A | 2 | 4.7 | 5.6 | 2 | 8.1 | ns |
| $t_{PHL}$ | | | 1.5 | 4.1 | 5 | 1.5 | 7.3 | |
| $t_{PZH}$ | $\overline{CEAB}$ or $\overline{CEBA}$ | B or A | 2 | 4.2 | 5.2 | 2 | 7.5 | ns |
| $t_{PZL}$ | | | 2 | 4.7 | 6.1 | 2 | 8.4 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2 | 4.4 | 5.4 | 2 | 6.7 | ns |
| $t_{PZL}$ | | | 2 | 5.2 | 7.4 | 2 | 7.6 | |
| $t_{PHZ}$ | $\overline{CEAB}$ or $\overline{CEBA}$ | B or A | 2.5 | 5.8 | 6.8 | 2.5 | 9.1 | ns |
| $t_{PLZ}$ | | | 2.5 | 5.3 | 6.3 | 2.5 | 8.7 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2 | 5.9 | 6.9 | 2 | 8.3 | ns |
| $t_{PLZ}$ | | | 2 | 5.2 | 6.2 | 2 | 7.8 | |

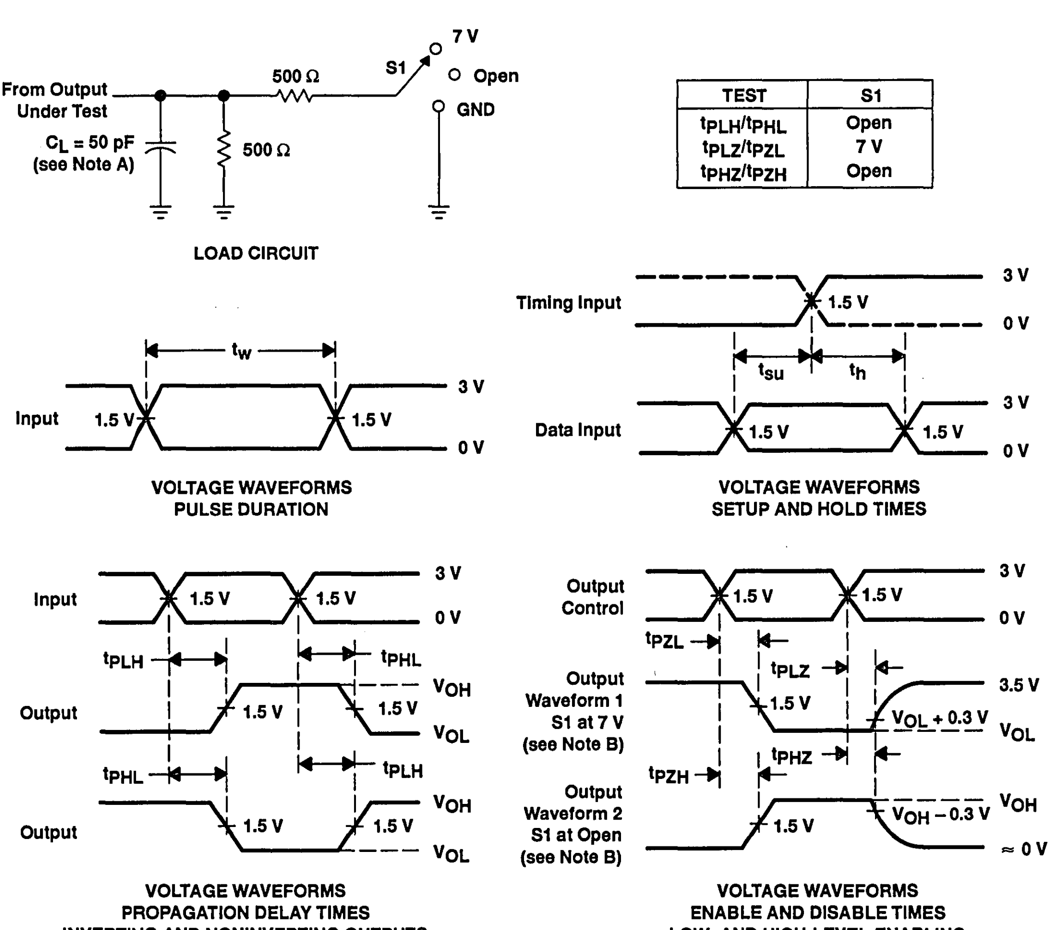
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT8543 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | 2 | 3.7 | 4.5 | 2 | 5.2 | ns |
| $t_{PHL}$ | | | 1.5 | 3.5 | 4.4 | 1.5 | 5.5 | |
| $t_{PLH}$ | $\overline{LEAB}$ or $\overline{LEBA}$ | B or A | 2 | 4.7 | 5.6 | 2 | 7.8 | ns |
| $t_{PHL}$ | | | 1.5 | 4.1 | 5 | 1.5 | 6.9 | |
| $t_{PZH}$ | $\overline{CEAB}$ or $\overline{CEBA}$ | B or A | 2 | 4.2 | 5.2 | 2 | 7.2 | ns |
| $t_{PZL}$ | | | 2 | 4.7 | 5.7 | 2 | 8.3 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2 | 4.4 | 5.4 | 2 | 6.5 | ns |
| $t_{PZL}$ | | | 2 | 5.2 | 6.2 | 2 | 7.5 | |
| $t_{PHZ}$ | $\overline{CEAB}$ or $\overline{CEBA}$ | B or A | 2.5 | 5.8 | 6.8 | 2.5 | 8.8 | ns |
| $t_{PLZ}$ | | | 2.5 | 5.3 | 6.3 | 2.5 | 8 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2 | 5.9 | 6.9 | 2 | 7.9 | ns |
| $t_{PLZ}$ | | | 2 | 5.2 | 6.2 | 2 | 7.4 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT8543 | | SN74ABT8543 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3.5 | 8 | 9.5 | 3.5 | 12.7 | 3.5 | 12 | ns |
| $t_{PHL}$ | | | 3 | 7.7 | 9 | 3 | 12 | 3 | 11.5 | |
| $t_{PLH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 7 | 2.5 | 6.5 | ns |
| $t_{PHL}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 7 | 2.5 | 6.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4.5 | 8.2 | 9.5 | 4.5 | 12.5 | 4.5 | 12 | ns |
| $t_{PZL}$ | | | 4.5 | 9 | 10.5 | 4.1 | 13.5 | 4.5 | 13 | |
| $t_{PZH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 7 | 2.5 | 6.5 | ns |
| $t_{PZL}$ | | | 2.5 | 4.9 | 6 | 2.5 | 7.5 | 2.5 | 7 | |
| $t_{PHZ}$ | TCK↓ | A or B | 3.5 | 8.4 | 10.5 | 3.5 | 14 | 3.5 | 13.5 | ns |
| $t_{PLZ}$ | | | 3 | 8 | 10.5 | 3 | 13.5 | 3 | 13 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.9 | 7 | 3 | 9 | 3 | 8.5 | ns |
| $t_{PLZ}$ | | | 3 | 5 | 6.5 | 3 | 8 | 3 | 7.5 | |

## PARAMETER MEASUREMENT INFORMATION



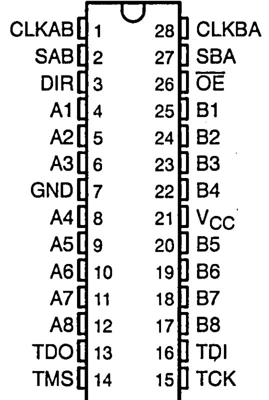

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

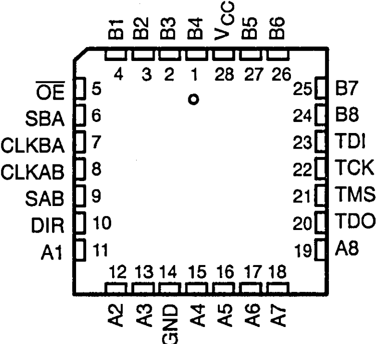
**Figure 13. Load Circuit and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Functionally Equivalent to 'F646 and 'ABT646 in the Normal-Function Mode
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP, and HIGHZ
  - Parallel-Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Even-Parity Opcodes
- Two Boundary-Scan Cells Per I/O for Greater Flexibility
- State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DL) Packages, Ceramic Chip Carriers (FK), and Standard Ceramic DIPs (JT)

SN54ABT8646 . . . JT PACKAGE
SN74ABT8646 . . . DL OR DW PACKAGE
(TOP VIEW)




SN54ABT8646 . . . FK PACKAGE
(TOP VIEW)




## description

The 'ABT8646 and scan test devices with octal bus transceivers and registers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the 'F646 and 'ABT646 octal bus transceivers and registers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers and registers.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

Transceiver function is controlled by output-enable ($\overline{OE}$) and direction (DIR) inputs. When $\overline{OE}$ is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When $\overline{OE}$ is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 shows the four fundamental bus-management functions that can be performed with the 'ABT8646.

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8646 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| X | X | ↑ | X | X | X | Input | Unspecified† | Store A, B unspecified† |
| X | X | X | ↑ | X | X | Unspecified† | Input | Store B, A unspecified† |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| H | X | L | L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | X | X | H | Output | Input disabled | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | X | X | H | X | Input disabled | Output | Stored A data to B bus |

† The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data-input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

| 26 | 3 | 1 | 28 | 2 | 27 |
|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | L | X | X | X | L |

**REAL-TIME TRANSFER BUS B TO BUS A**



| 26 | 3 | 1 | 28 | 2 | 27 |
|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | H | X | X | L | X |

**REAL-TIME TRANSFER BUS A TO BUS B**



| 26 | 3 | 1 | 28 | 2 | 27 |
|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| H | X | ↑ | ↑ | X | X |

**STORAGE FROM A, B, OR A AND B**



| 26 | 3 | 1 | 28 | 2 | 27 |
|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | L | X | X | X | H |
| L | H | X | X | H | X |

**TRANSFER STORED DATA TO A AND/OR B**

Pin numbers shown are for the DL, DW, and JT packages.

**Figure 1. Bus-Management Functions**

## functional block diagram

Boundary-Scan Register
$\overline{OE}$ 26
DIR 3
CLKBA 28
SBA 27
CLKAB 1
SAB 2
C1
1D
A1 4
C1
1D
25 B1
One of Eight Channels
Bypass Register
Boundary-Control Register
$V_{CC}$
TDI 16
$V_{CC}$
TMS 14
TCK 15
Instruction Register
TAP Controller
13 TDO

Pin numbers shown for the DL, DW, and JT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A1–A8 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| B1–B8 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| CLKAB, CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| DIR | Normal-function direction-control input. See function table for normal-mode logic. |
| GND | Ground |
| $\overline{OE}$ | Normal-function output-enable input. See function table for normal-mode logic. |
| SAB, SBA | Normal-function select inputs. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS input directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 2 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and three test-data registers: a 40-bit boundary-scan register, an 11-bit boundary-control register, and a 1-bit bypass register.

**Figure 2. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 2 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8646, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0. The boundary-control register is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon, which the TAP controller exits the Capture-IR state.

For the 'ABT8646, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass register, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8646. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR of scan is shown in Figure 3.

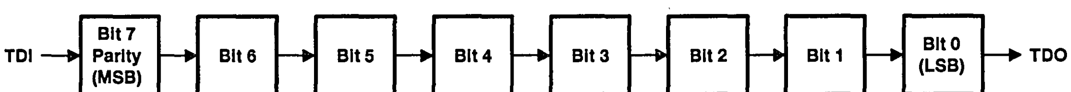



**Figure 3. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 40 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, two BSCs for each normal-function I/O pin (one for input data and one for output data), and one BSC for each of the internally decoded output-enable signals (OEA and OEB). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0.

When external data is to be captured, the BSCs for signals OEA and OEB capture logic values determined by the following positive-logic equations: $OEA = \overline{\overline{OE}} \bullet \overline{DIR}$, and $OEB = \overline{\overline{OE}} \bullet DIR$. When data is to be applied externally, these BSCs control the drive state (active or high-impedance) of their respective outputs.

The BSR order of scan is from TDI through bits 39–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|---|---|---|---|
| 39 | OEB | 31 | A8-I | 23 | A8-O | 15 | B8-I | 7 | B8-O |
| 38 | OEA | 30 | A7-I | 22 | A7-O | 14 | B7-I | 6 | B7-O |
| 37 | DIR | 29 | A6-I | 21 | A6-O | 13 | B6-I | 5 | B6-O |
| 36 | $\overline{OE}$ | 28 | A5-I | 20 | A5-O | 12 | B5-I | 4 | B5-O |
| 35 | CLKAB | 27 | A4-I | 19 | A4-O | 11 | B4-I | 3 | B4-O |
| 34 | CLKBA | 26 | A3-I | 18 | A3-O | 10 | B3-I | 2 | B3-O |
| 33 | SAB | 25 | A2-I | 17 | A2-O | 9 | B2-I | 1 | B2-O |
| 32 | SBA | 24 | A1-I | 16 | A1-O | 8 | B1-I | 0 | B1-O |

### boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The BCR order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the BCR bits and their associated test control signals.

**Table 2. Boundary-Control Register Configuration**

| BCR BIT NUMBER | TEST CONTROL SIGNAL | BCR BIT NUMBER | TEST CONTROL SIGNAL | BCR BIT NUMBER | TEST CONTROL SIGNAL |
|---|---|---|---|---|---|
| 10 | MASK8 | 6 | MASK4 | 2 | OPCODE2 |
| 9 | MASK7 | 5 | MASK3 | 1 | OPCODE1 |
| 8 | MASK6 | 4 | MASK2 | 0 | OPCODE0 |
| 7 | MASK5 | 3 | MASK1 | — | — |

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

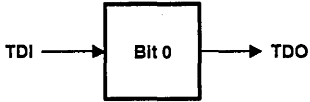



**Figure 4. Bypass Register Order of Scan**

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST/INTEST | Boundary scan | Boundary scan | Test |
| 10000001 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | INTEST/EXTEST | Boundary scan | Boundary scan | Test |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the ’ABT8646.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

**boundary run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/16-bit mode (PRPG) |
| X10 | Parallel-signature analysis/16-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT) |

In general, while the control input BSCs (bits 39–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 39–38 of the BSR) do control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when the device is operating in one direction of data flow (that is, OEA ≠ OEB). Otherwise, the bypass instruction is operated.

### PSA input masking

Bits 10–3 of the BCR specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins, in order, from most significant to least significant, as indicated in Table 3. When the mask bit that corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, i.e., the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

### sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. This data also is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Figures 5 and 6 show the 16-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

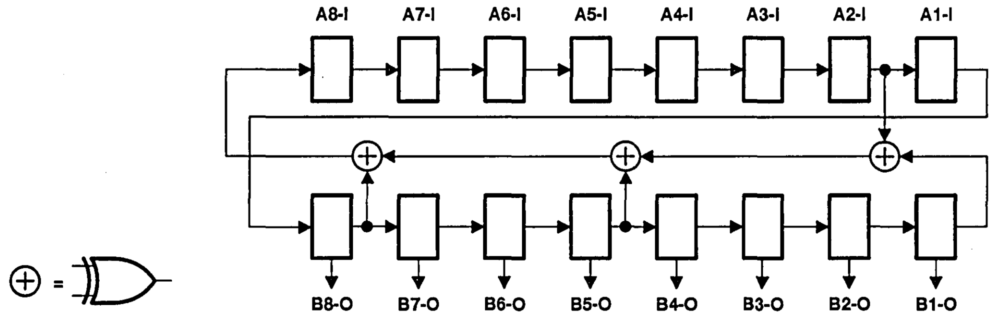



Figure 5. 16-Bit PRPG Configuration (OEA = 0, OEB = 1)

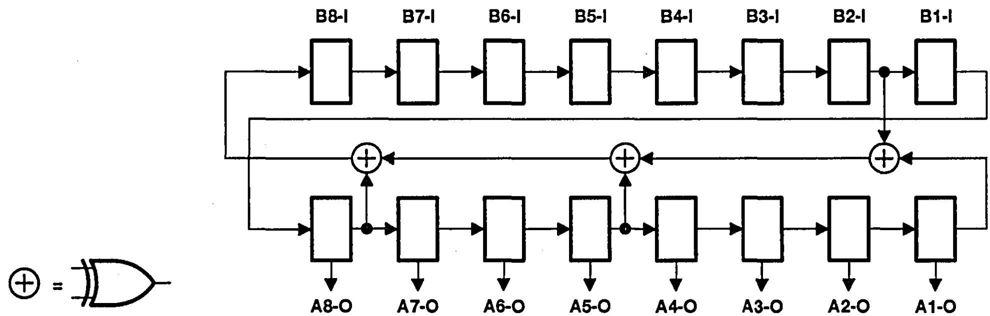



Figure 6. 16-Bit PRPG Configuration (OEA=1, OEB= 0)

### parallel-signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 7 and 8 show the 16-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

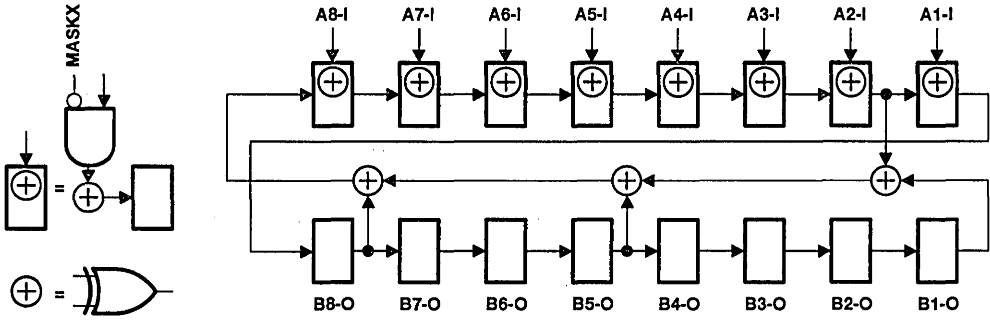



**Figure 7. 16-Bit PSA Configuration (OEA = 0, OEB = 1)**

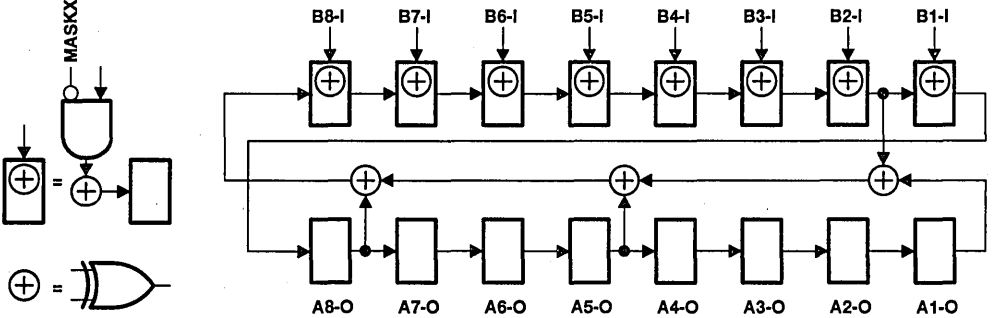



**Figure 8. 16-Bit PSA Configuration (OEA = 1, OEB = 0)**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. Figures 9 and 10 show the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

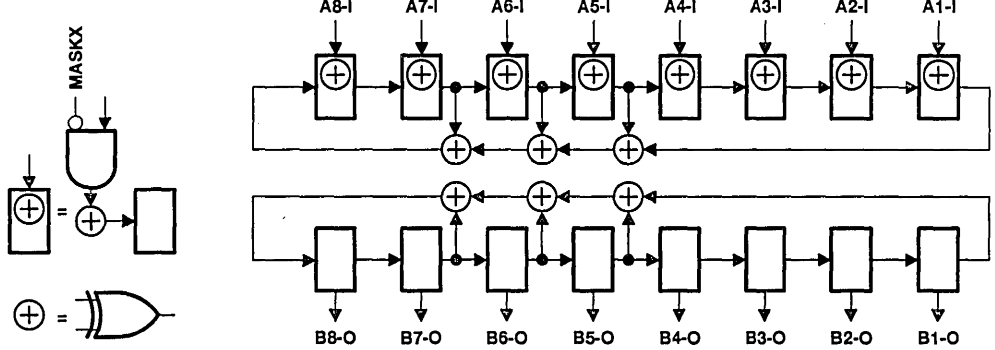



Figure 9. 8-Bit PSA/PRPG Configuration (OEA = 0, OEB = 1)

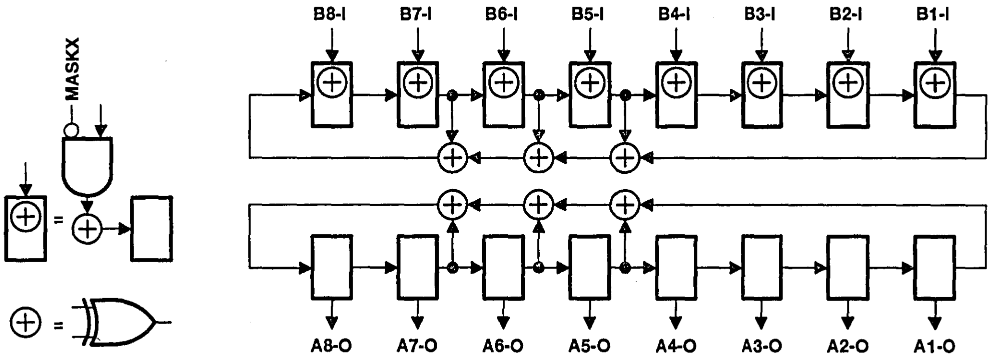



Figure 10. 8-Bit PSA/PRPG Configuration (OEA = 1, OEB = 0)

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. In addition, the shift-register elements of the opposite output BSCs count carries out of the selected output BSCs extending the count to 16 bits. Figures 11 and 12 show the 8-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

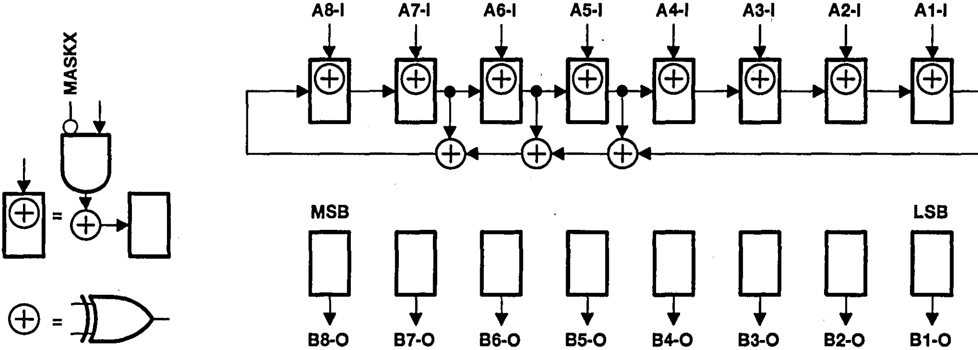



Figure 11. 8-Bit PSA/COUNT Configuration (OEA = 0, OEB = 1)

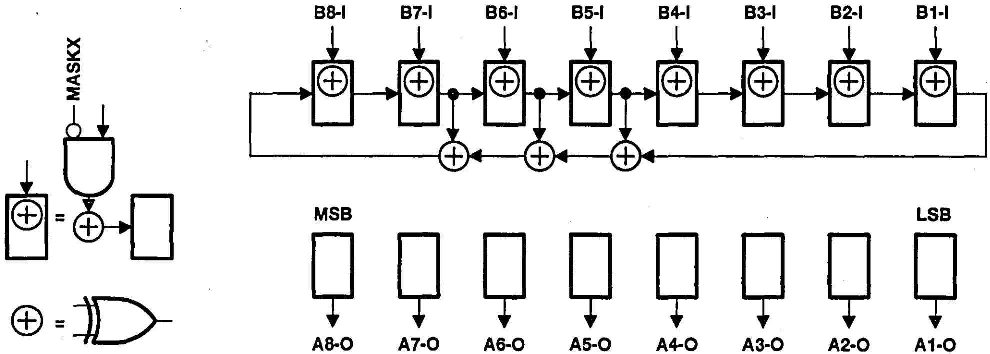



Figure 12. 8-Bit PSA/COUNT Configuration (OEA = 1, OEB = 0)

## timing description

All test operations of the 'ABT8646 are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 2) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

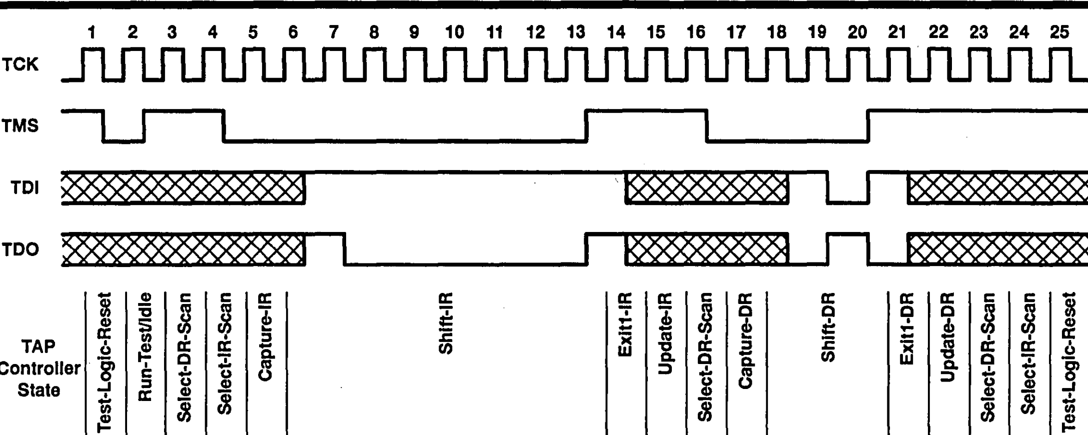



**Figure 13. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ........ –0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) ........ –0.5 V to 7 V
Input voltage range, $V_I$ (I/O ports) (see Note 1) ........ –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, $V_O$ ........ –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT8646 ........ 96 mA
SN74ABT8646 ........ 128 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) ........ –18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) ........ –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DL package ........ 0.7 W
DW package ........ 1.7 W
Storage temperature range, $T_{stg}$ ........ –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions (see Note 3)

| | | SN54ABT8646 | | SN74ABT8646 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT8646 | | SN74ABT8646 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $I_I$ | CLK, DIR, $\overline{OE}$, S, TCK | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | | | | | ±100 | | ±100 | | ±100 | |
| $I_{IH}$ | TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | | 10 | µA |
| $I_{IL}$ | TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –160 | –40 | –160 | –40 | –160 | µA |
| $I_{OZH}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | | –50 | | –50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \le$ 4.5 V | | | ±100 | | | | ±100 | µA |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 2 V, | $V_O$ = 0.5 V or 2.7 V | | | ±50 | | ±50 | | ±50 | µA |
| $I_{OZPD}$ | | $V_{CC}$ = 2 V to 0, | $V_O$ = 0.5 V or 2.7 V | | | ±50 | | ±50 | | ±50 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –100 | –180 | –50 | –180 | –50 | –180 | mA |
| $I_{CC}$ | A or B ports | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.9 | 2 | | 2 | | 2 | mA |
| | | | Outputs low | | 30 | 38 | | 38 | | 38 | |
| | | | Outputs disabled | | 0.9 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 3 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)**

| | | | SN54ABT8646 | | SN74ABT8646 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | 3 | | 3 | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | 4.7 | | 4.5 | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | 0 | | 0 | | ns |

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)**

| | | | SN54ABT8646 | | SN74ABT8646 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 5 | | 5 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, DIR, $\overline{OE}$, or S before TCK↑ | 7 | | 5 | | ns |
| | | TDI before TCK↑ | 6 | | 6 | | |
| | | TMS before TCK↑ | 6 | | 6 | | |
| $t_h$ | Hold time | A, B, CLK, DIR, $\overline{OE}$, or S after TCK↑ | 0 | | 0 | | ns |
| | | TDI after TCK↑ | 0 | | 0 | | |
| | | TMS after TCK↑ | 0 | | 0 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50* | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1* | | 1 | | µs |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT8646 $V_{CC}$ = 5 V, $T_A$ = 25°C MIN | TYP | MAX | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | 2 | 3.7 | 4.5 | 2 | 5.5 | ns |
| $t_{PHL}$ | | | 2 | 3.5 | 4.6 | 2 | 5.8 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 3 | 4.4 | 5.3 | 3 | 6.3 | ns |
| $t_{PHL}$ | | | 2.5 | 4.3 | 5.2 | 2.5 | 6.7 | |
| $t_{PLH}$ | SAB or SBA | B or A | 2 | 4.8 | 6 | 2 | 7.5 | ns |
| $t_{PHL}$ | | | 2 | 4.7 | 5.9 | 2 | 7.8 | |
| $t_{PZH}$ | DIR | B or A | 2.5 | 4.4 | 5.4 | 2.5 | 6.6 | ns |
| $t_{PZL}$ | | | 3 | 4.8 | 6.2 | 3 | 8.1 | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | 2.5 | 4.4 | 5.4 | 2.5 | 6.7 | ns |
| $t_{PZL}$ | | | 3 | 5.2 | 6.2 | 3 | 7.6 | |
| $t_{PHZ}$ | DIR | B or A | 3 | 6 | 7.9 | 3 | 8.9 | ns |
| $t_{PLZ}$ | | | 3 | 5.2 | 6.6 | 3 | 8.1 | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | 2 | 5.9 | 7.7 | 2.8 | 8.6 | ns |
| $t_{PLZ}$ | | | 3 | 5.2 | 6.2 | 3 | 8.3 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT8646 $V_{CC}$ = 5 V, $T_A$ = 25°C MIN | TYP | MAX | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | 2 | 3.7 | 4.5 | 2 | 5.2 | ns |
| $t_{PHL}$ | | | 2 | 3.5 | 4.4 | 2 | 5.5 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 3 | 4.4 | 5.3 | 3 | 6 | ns |
| $t_{PHL}$ | | | 2.5 | 4.3 | 5.2 | 2.5 | 6.2 | |
| $t_{PLH}$ | SAB or SBA | B or A | 2 | 4.8 | 6 | 2 | 7.3 | ns |
| $t_{PHL}$ | | | 2 | 4.7 | 5.9 | 2 | 7.4 | |
| $t_{PZH}$ | DIR | B or A | 2.5 | 4.4 | 5.3 | 2.5 | 6.5 | ns |
| $t_{PZL}$ | | | 3 | 4.8 | 6.2 | 3 | 7.1 | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | 2.5 | 4.4 | 5.4 | 2.5 | 6.5 | ns |
| $t_{PZL}$ | | | 3 | 5.2 | 6.2 | 3 | 7.5 | |
| $t_{PHZ}$ | DIR | B or A | 3 | 6 | 7 | 3 | 8.6 | ns |
| $t_{PLZ}$ | | | 3 | 5.2 | 6.2 | 3 | 7.9 | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | 3 | 5.9 | 6.9 | 3 | 7.9 | ns |
| $t_{PLZ}$ | | | 3 | 5.2 | 6.2 | 3 | 7.4 | |

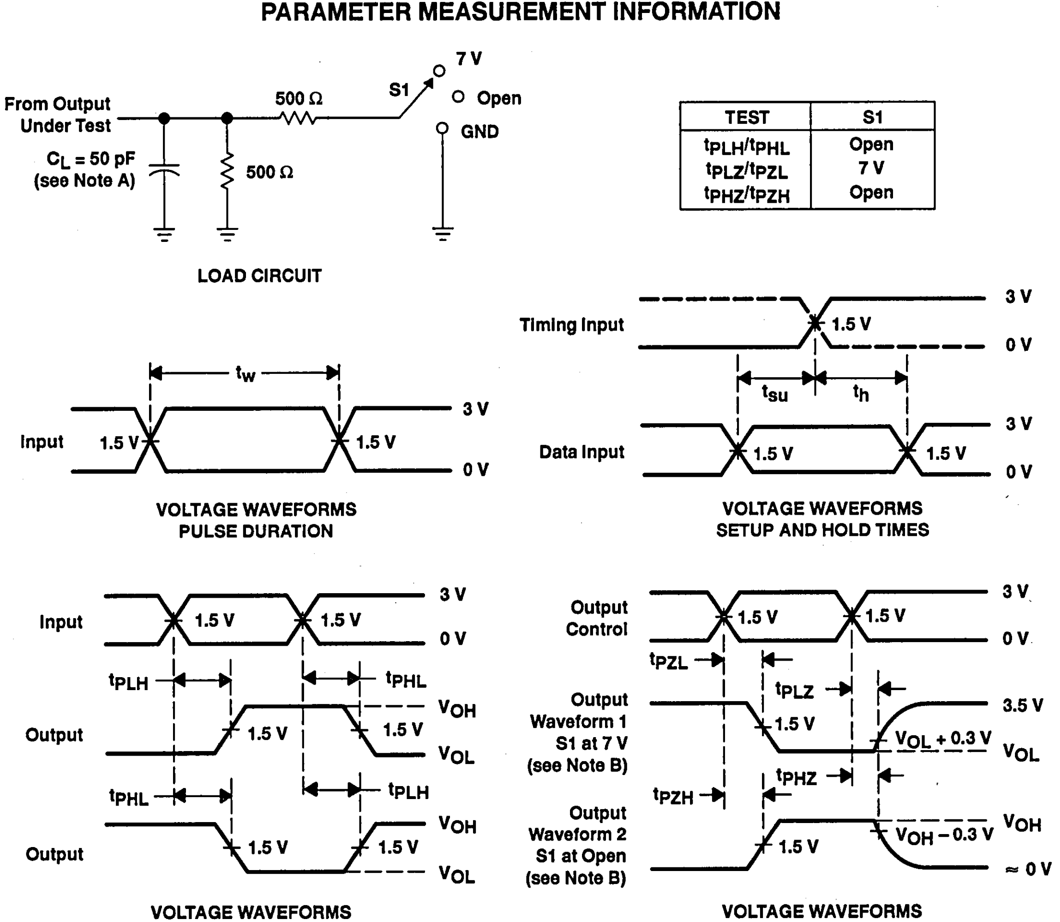
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT8646 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3.5 | 8 | 9.5 | 3.5 | 13.4 | ns |
| $t_{PHL}$ | | | 3 | 7.7 | 10 | 3 | 12 | |
| $t_{PLH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 7 | ns |
| $t_{PHL}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 7 | |
| $t_{PZH}$ | TCK↓ | A or B | 4.5 | 8.2 | 9.7 | 4.5 | 12.5 | ns |
| $t_{PZL}$ | | | 4.5 | 9 | 11.2 | 4.5 | 13.5 | |
| $t_{PZH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 7 | ns |
| $t_{PZL}$ | | | 2.5 | 4.9 | 6 | 2.5 | 7.5 | |
| $t_{PHZ}$ | TCK↓ | A or B | 3.5 | 8.4 | 13 | 3.5 | 14.5 | ns |
| $t_{PLZ}$ | | | 3 | 8 | 10.5 | 3 | 13.5 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.9 | 7 | 3 | 9 | ns |
| $t_{PLZ}$ | | | 3 | 5 | 6.5 | 3 | 8 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT8646 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3.5 | 8 | 9.5 | 3.5 | 12 | ns |
| $t_{PHL}$ | | | 3 | 7.7 | 9 | 3 | 11.5 | |
| $t_{PLH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 6.5 | ns |
| $t_{PHL}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 6.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4.5 | 8.2 | 9.5 | 4.5 | 12 | ns |
| $t_{PZL}$ | | | 4.5 | 9 | 10.5 | 4.5 | 13 | |
| $t_{PZH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 6.5 | ns |
| $t_{PZL}$ | | | 2.5 | 4.9 | 6 | 2.5 | 7 | |
| $t_{PHZ}$ | TCK↓ | A or B | 3.5 | 8.4 | 10.5 | 3.5 | 13.5 | ns |
| $t_{PLZ}$ | | | 3 | 8 | 10.5 | 3 | 13 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.9 | 7 | 3 | 8.5 | ns |
| $t_{PLZ}$ | | | 3 | 5 | 6.5 | 3 | 7.5 | |

## PARAMETER MEASUREMENT INFORMATION



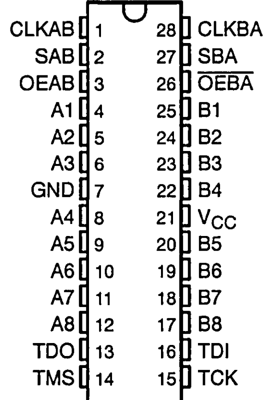

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

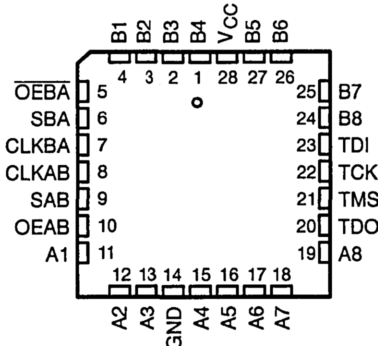
**Figure 14. Load Circuit and Voltage Waveforms**

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Functionally Equivalent to 'F652 and 'ABT652 in the Normal-Function Mode**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP, and HIGHZ**
  - **Parallel-Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Even-Parity Opcodes**
- **Two Boundary-Scan Cells Per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Shrink Small-Outline (DL) and Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Ceramic DIPs (JT)**

**SN54ABT8652 . . . JT PACKAGE**
**SN74ABT8652 . . . DL OR DW PACKAGE**
**(TOP VIEW)**




**SN54ABT8652 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The 'ABT8652 scan test devices with octal bus transceivers and registers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the 'F652 and 'ABT652 octal bus transceivers and registers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers and registers.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and $\overline{\text{OEBA}}$ inputs. Since the $\overline{\text{OEBA}}$ input is active low, the A outputs are active when $\overline{\text{OEBA}}$ is low and are in the high-impedance state when $\overline{\text{OEBA}}$ is high. Figure 1 shows the four fundamental bus-management functions that can be performed with the 'ABT8652.

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8652 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| L | H | X | X | X | X | Input disabled | Input disabled | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | L | X | X | Input | Unspecified† | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | L | ↑ | X | X | Unspecified† | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | X | X | H | Output | Input | Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | X | X | H | X | Input | Output | Stored A data to B bus |
| H | L | L | L | H | H | Output | Output | Stored A data to B bus and stored B data to A bus |

† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

BUS A BUS B

| 3 OEAB | 26 $\overline{OEBA}$ | 1 CLKAB | 28 CLKBA | 2 SAB | 27 SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER BUS B TO BUS A**

BUS A BUS B

| 3 OEAB | 26 $\overline{OEBA}$ | 1 CLKAB | 28 CLKBA | 2 SAB | 27 SBA |
|---|---|---|---|---|---|
| H | H | X | X | L | X |

**REAL-TIME TRANSFER BUS A TO BUS B**

BUS A BUS B

| 3 OEAB | 26 $\overline{OEBA}$ | 1 CLKAB | 28 CLKBA | 2 SAB | 27 SBA |
|---|---|---|---|---|---|
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**STORAGE FROM A, B, OR A AND B**

BUS A BUS B

| 3 OEAB | 26 $\overline{OEBA}$ | 1 CLKAB | 28 CLKBA | 2 SAB | 27 SBA |
|---|---|---|---|---|---|
| H | L | X | X | H | H |

**TRANSFER STORED DATA TO A AND/OR B**

Pin numbers shown are for the DL, DW, and JT packages.

**Figure 1. Bus-Management Functions**

## functional block diagram

Boundary-Scan Register

OEAB 3
$\overline{OEBA}$ 26
CLKBA 28
SBA 27
CLKAB 1
SAB 2

C1
1D

A1 4

C1
1D

25 B1

One of Eight Channels

Bypass Register

Boundary-Control Register

Instruction Register

$V_{CC}$
TDI 16
$V_{CC}$
TMS 14
TCK 15

TAP Controller

13 TDO

Pin numbers shown are for the DL, DW, and JT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A1–A8 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| B1–B8 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| CLKAB, CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| GND | Ground |
| OEAB, $\overline{OEBA}$ | Normal-function output-enable inputs. See function table for normal-mode logic. |
| SAB, SBA | Normal-function select inputs. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 2 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and three test-data registers: a 38-bit boundary-scan register, an 11-bit boundary-control register, and a 1-bit bypass register.

**Figure 2. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 2 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. TMS has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8652, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0 except bit 36, which is reset to logic 1. The boundary-control register is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'ABT8652, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass register, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8652. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR order of scan is shown in Figure 3.

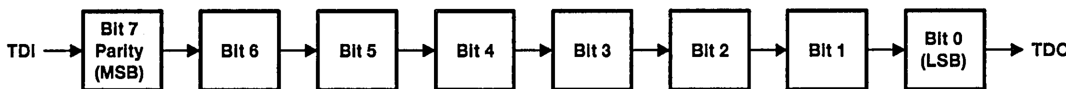



**Figure 3. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 38 bits long. It contains one boundary-scan cell (BSC) for each normal-function input and two BSCs for each normal-function I/O (one for input data and one for output data). The BSR is used to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output terminals, and/or to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input terminals.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0 except BSC 36, which is reset to logic 1.

The BSR order of scan is from TDI through bits 37–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|---|---|---|---|
| 37 | OEAB | 31 | A8-I | 23 | A8-O | 15 | B8-I | 7 | B8-O |
| 36 | $\overline{\text{OEBA}}$ | 30 | A7-I | 22 | A7-O | 14 | B7-I | 6 | B7-O |
| 35 | CLKAB | 29 | A6-I | 21 | A6-O | 13 | B6-I | 5 | B6-O |
| 34 | CLKBA | 28 | A5-I | 20 | A5-O | 12 | B5-I | 4 | B5-O |
| 33 | SAB | 27 | A4-I | 19 | A4-O | 11 | B4-I | 3 | B4-O |
| 32 | SBA | 26 | A3-I | 18 | A3-O | 10 | B3-I | 2 | B3-O |
| — | — | 25 | A2-I | 17 | A2-O | 9 | B2-I | 1 | B2-O |
| — | — | 24 | A1-I | 16 | A1-O | 8 | B1-I | 0 | B1-O |

### boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The BCR order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the BCR bits and their associated test control signals.

**Table 2. Boundary-Control Register Configuration**

| BCR BIT NUMBER | TEST CONTROL SIGNAL | BCR BIT NUMBER | TEST CONTROL SIGNAL | BCR BIT NUMBER | TEST CONTROL SIGNAL |
|---|---|---|---|---|---|
| 10 | MASK8 | 6 | MASK4 | 2 | OPCODE2 |
| 9 | MASK7 | 5 | MASK3 | 1 | OPCODE1 |
| 8 | MASK6 | 4 | MASK2 | 0 | OPCODE0 |
| 7 | MASK5 | 3 | MASK1 | — | — |

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

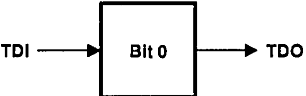



**Figure 4. Bypass Register Order of Scan**

### instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST/INTEST | Boundary scan | Boundary scan | Test |
| 10000001 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | INTEST/EXTEST | Boundary scan | Boundary scan | Test |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT8652.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output terminals. The device operates in the test mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**sample boundary**

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input terminals is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O terminals are placed in the high-impedance state, the device input terminals remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output terminals. The device operates in the test mode.

**boundary run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device output terminals on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input terminals is not captured in the input BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/16-bit mode (PRPG) |
| X10 | Parallel-signature analysis/16-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT) |

In general, while the control input BSCs (bits 37–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 37–36 of the BSR) do control the drive state (active or high impedance) of the selected device output terminals. These BCR instructions are valid only when the device is operating in one direction of data flow (that is, OEAB = $\overline{\text{OEBA}}$). Otherwise, the bypass instruction is operated.

## PSA input masking

Bits 10–3 of the BCR specify device input terminals to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input terminals A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input terminals in order, from most significant to least significant, as indicated in Table 3. When the mask bit that corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, i.e., the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input terminals is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output terminals on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output terminals on each falling edge of TCK. This data also is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Figures 5 and 6 show the 16-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

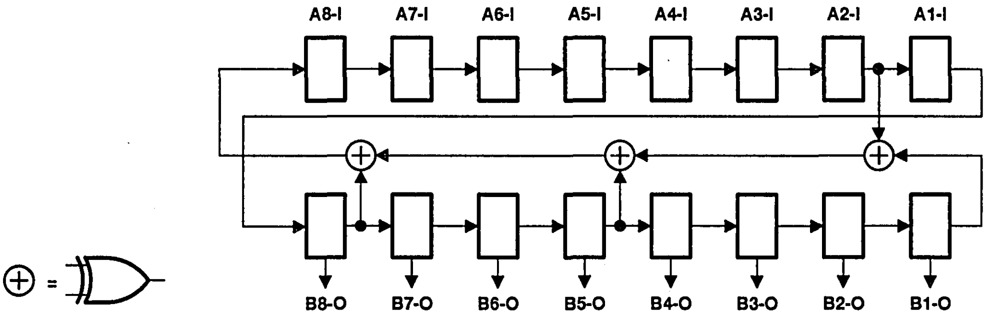



**Figure 5. 16-Bit PRPG Configuration (OEAB = 1, $\overline{\text{OEBA}}$ = 1)**

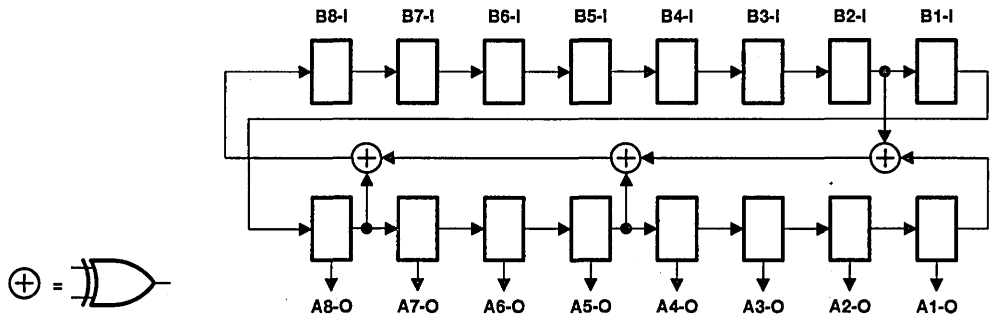



**Figure 6. 16-Bit PRPG Configuration (OEAB = 0, $\overline{\text{OEBA}}$ = 0)**

**parallel-signature analysis (PSA)**

Data appearing at the selected device input terminals is compressed into a 16-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 7 and 8 show the 16-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

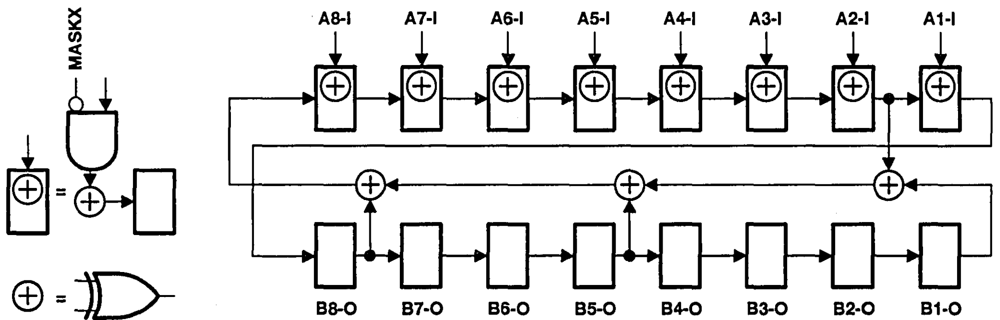



Figure 7. 16-Bit PSA Configuration (OEAB = 1, $\overline{OEBA}$ = 1)

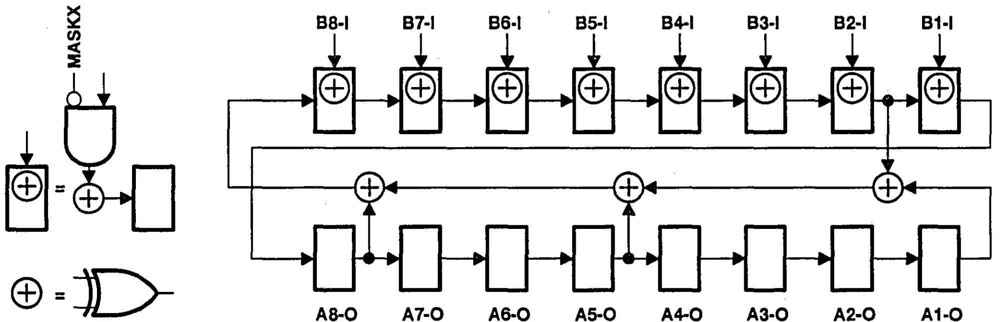



Figure 8. 16-Bit PSA Configuration (OEAB = 0, $\overline{OEBA}$ = 0)

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input terminals is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output terminals on each falling edge of TCK. Figures 9 and 10 show the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

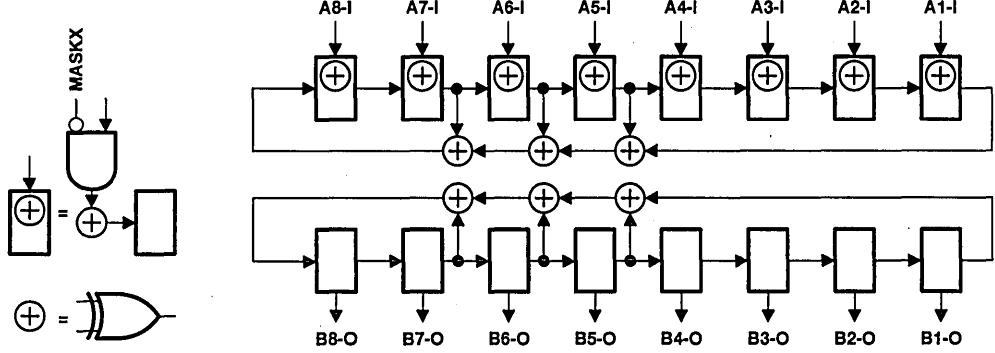



**Figure 9. 8-Bit PSA/PRPG Configuration (OEAB = 1, $\overline{\text{OEBA}}$ = 1)**

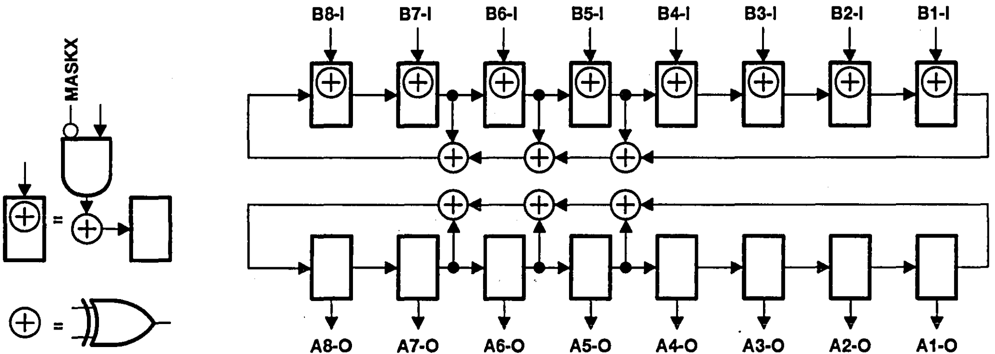



**Figure 10. 8-Bit PSA/PRPG Configuration (OEAB = 0, $\overline{\text{OEBA}}$ = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input terminals is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output terminals on each falling edge of TCK. In addition, the shift-register elements of the opposite output BSCs count carries out of the selected output BSCs extending the count to 16 bits. Figures 11 and 12 show the 8-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

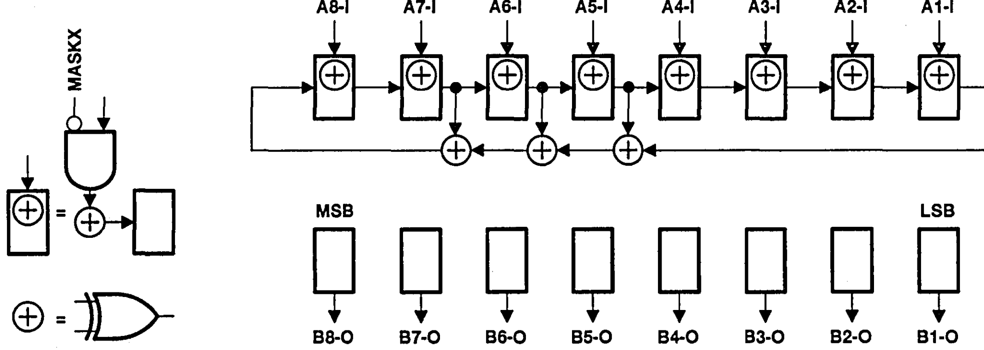



**Figure 11. 8-Bit PSA/COUNT Configuration (OEAB = 1, $\overline{\text{OEBA}}$ = 1)**

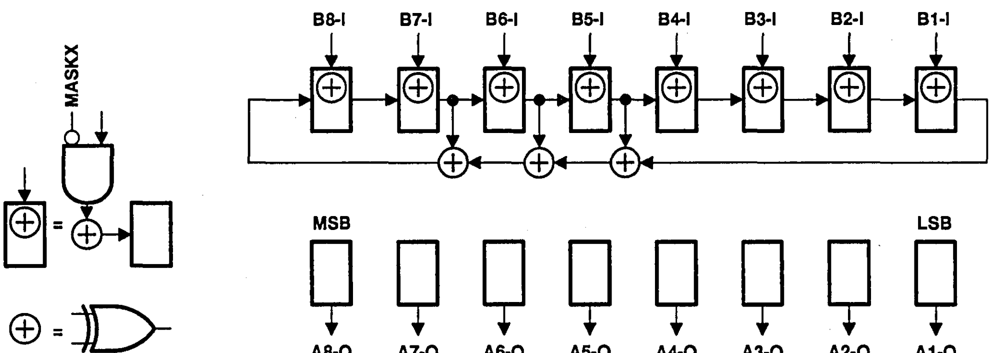



**Figure 12. 8-Bit PSA/COUNT Configuration (OEAB = 0, $\overline{\text{OEBA}}$ = 0)**

## timing description

All test operations of the 'ABT8652 are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output terminals on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 2) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

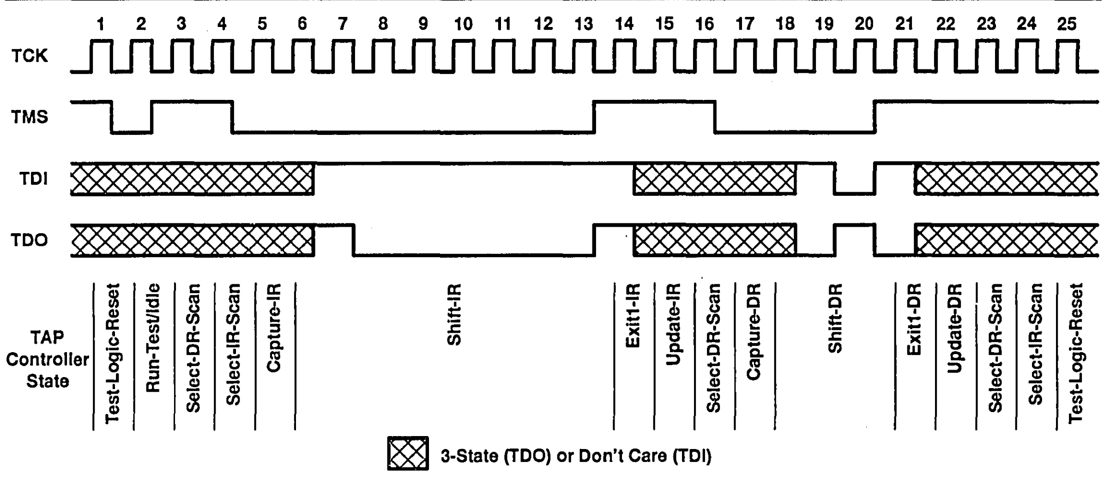



**Figure 13. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ........ –0.5 V to 7 V
Input voltage range, $V_I$: except I/O ports (see Note 1) ........ –0.5 V to 7 V
I/O ports (see Note 1) ........ –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, $V_O$ ........ –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT8652 ........ 96 mA
SN74ABT8652 ........ 128 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) ........ –18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) ........ –50 mA
Maximum package power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DL package ........ 0.7 W
DW package ........ 1.7 W
Storage temperature range, $T_{stg}$ ........ –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions (see Note 3)

| | | SN54ABT8652 | | SN74ABT8652 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT8652 | | SN74ABT8652 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $I_I$ | CLK, OEAB, $\overline{OEBA}$, S, TCK | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | μA |
| | A or B ports | | | | | ±100 | | ±100 | | ±100 | |
| $I_{IH}$ | TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | | 10 | μA |
| $I_{IL}$ | TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –160 | –40 | –160 | –40 | –160 | μA |
| $I_{OZH}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | 50 | | 50 | μA |
| $I_{OZL}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | | –50 | | –50 | μA |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 2 V, $V_O$ = 0.5 V or 2.7 V | | | | ±50 | | ±50 | | ±50 | μA |
| $I_{OZPD}$ | | $V_{CC}$ = 2 V to 0, $V_O$ = 0.5 V or 2.7 V | | | | ±50 | | ±50 | | ±50 | μA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±100 | | | | ±100 | μA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | | 50 | μA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –100 | –180 | –50 | –180 | –50 | –180 | mA |
| $I_{CC}$ | A or B ports | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.9 | 2 | | 2 | | 2 | mA |
| | | | Outputs low | | 30 | 38 | | 38 | | 38 | |
| | | | Outputs disabled | | 0.9 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 3 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)**

| | | | SN54ABT8652 | | SN74ABT8652 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | 3 | | 3 | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | 5.1 | | 4.5 | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | 0.5 | | 0 | | ns |

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)**

| | | | SN54ABT8652 | | SN74ABT8652 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 5 | | 5 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, OEAB, $\overline{OEBA}$, or S before TCK↑ | 5.1 | | 5 | | ns |
| | | TDI before TCK↑ | 6 | | 6 | | |
| | | TMS before TCK↑ | 6 | | 6 | | |
| $t_h$ | Hold time | A, B, CLK, OEAB, $\overline{OEBA}$, or S after TCK↑ | 0.6 | | 0 | | ns |
| | | TDI after TCK↑ | 0.9 | | 0 | | |
| | | TMS after TCK↑ | 0.9 | | 0 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50* | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1* | | 1 | | µs |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT8652 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | 2 | 3.7 | 5.1 | 2 | 6 | ns |
| $t_{PHL}$ | | | 1.5 | 3.5 | 4.4 | 1.5 | 5.8 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 2.5 | 4.4 | 5.3 | 2.5 | 6.3 | ns |
| $t_{PHL}$ | | | 2.5 | 4.3 | 5.4 | 2.5 | 6.7 | |
| $t_{PLH}$ | SAB or SBA | B or A | 2 | 4.8 | 6.1 | 2 | 7.5 | ns |
| $t_{PHL}$ | | | 2 | 4.7 | 6.7 | 2 | 7.8 | |
| $t_{PZH}$ | OEAB or $\overline{OEBA}$ | B or A | 1.7 | 4.4 | 5.4 | 1.7 | 6.7 | ns |
| $t_{PZL}$ | | | 2 | 5.2 | 6.2 | 2 | 7.6 | |
| $t_{PHZ}$ | OEAB or $\overline{OEBA}$ | B or A | 2 | 5.9 | 6.9 | 2 | 8.3 | ns |
| $t_{PLZ}$ | | | 2 | 5.2 | 6.2 | 2 | 7.8 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT8652 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | 2 | 3.7 | 4.5 | 2 | 5.2 | ns |
| $t_{PHL}$ | | | 1.5 | 3.5 | 4.4 | 1.5 | 5.5 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 2.5 | 4.4 | 5.3 | 2.5 | 6 | ns |
| $t_{PHL}$ | | | 2.5 | 4.3 | 5.2 | 2.5 | 6.2 | |
| $t_{PLH}$ | SAB or SBA | B or A | 2 | 4.8 | 6 | 2 | 7.3 | ns |
| $t_{PHL}$ | | | 2 | 4.7 | 5.9 | 2 | 7.4 | |
| $t_{PZH}$ | OEAB or $\overline{OEBA}$ | B or A | 2 | 4.4 | 5.4 | 2 | 6.5 | ns |
| $t_{PZL}$ | | | 2 | 5.2 | 6.2 | 2 | 7.5 | |
| $t_{PHZ}$ | OEAB or $\overline{OEBA}$ | B or A | 2 | 5.9 | 6.9 | 2 | 7.9 | ns |
| $t_{PLZ}$ | | | 2 | 5.2 | 6.2 | 2 | 7.4 | |

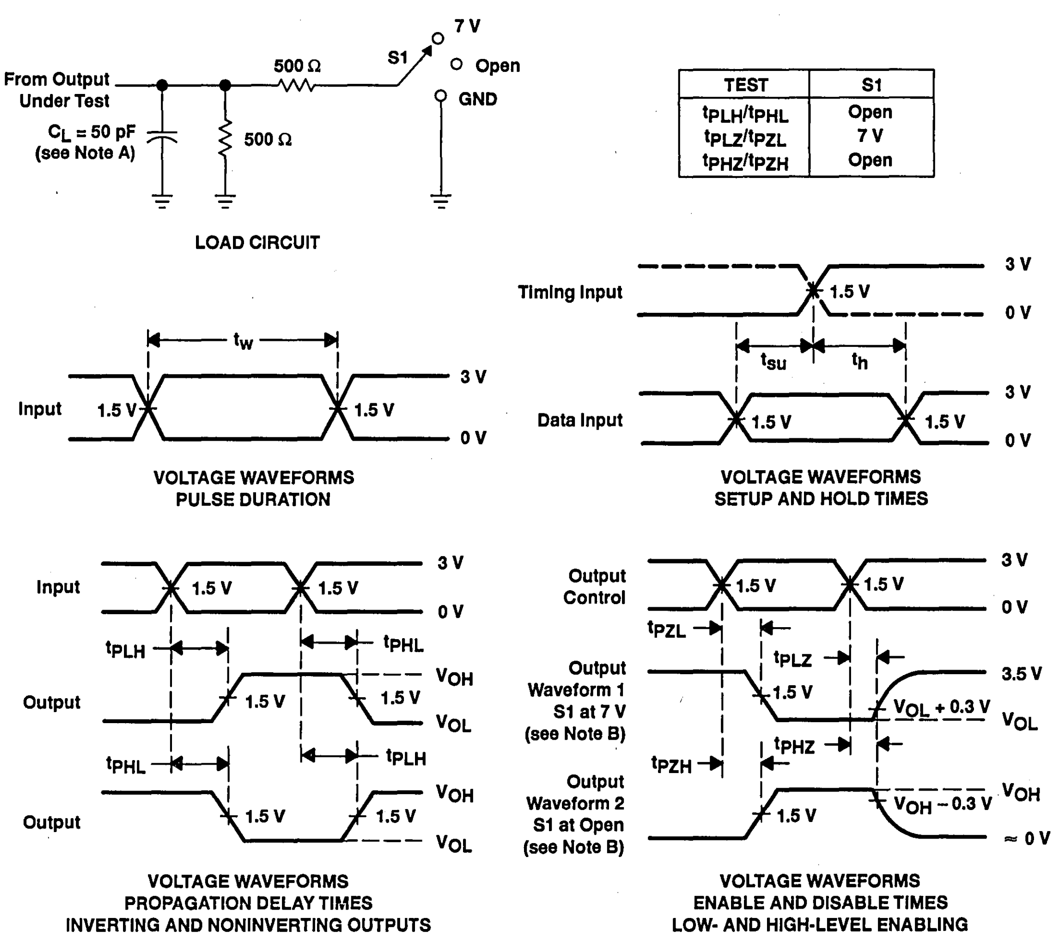
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT8652 $V_{CC}$ = 5 V, $T_A$ = 25°C MIN | TYP | MAX | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3.5 | 8 | 10.2 | 3.3 | 13.7 | ns |
| $t_{PHL}$ | | | 3 | 7.7 | 9 | 3 | 12 | |
| $t_{PLH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 7 | ns |
| $t_{PHL}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 7 | |
| $t_{PZH}$ | TCK↓ | A or B | 4.5 | 8.2 | 9.5 | 4.3 | 12.5 | ns |
| $t_{PZL}$ | | | 4.5 | 9 | 10.5 | 4.5 | 13.5 | |
| $t_{PZH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 7 | ns |
| $t_{PZL}$ | | | 2.5 | 4.9 | 6 | 2.5 | 7.5 | |
| $t_{PHZ}$ | TCK↓ | A or B | 3.5 | 8.4 | 12.9 | 3.5 | 14 | ns |
| $t_{PLZ}$ | | | 3 | 8 | 10.5 | 3 | 13.5 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.9 | 7 | 3 | 9 | ns |
| $t_{PLZ}$ | | | 3 | 5 | 6.5 | 3 | 8 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT8652 $V_{CC}$ = 5 V, $T_A$ = 25°C MIN | TYP | MAX | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3.5 | 8 | 9.5 | 3.5 | 12 | ns |
| $t_{PHL}$ | | | 3 | 7.7 | 9 | 3 | 11.5 | |
| $t_{PLH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 6.5 | ns |
| $t_{PHL}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 6.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4.5 | 8.2 | 9.5 | 4.5 | 12 | ns |
| $t_{PZL}$ | | | 4.5 | 9 | 10.5 | 4.5 | 13 | |
| $t_{PZH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 6.5 | ns |
| $t_{PZL}$ | | | 2.5 | 4.9 | 6 | 2.5 | 7 | |
| $t_{PHZ}$ | TCK↓ | A or B | 3.5 | 8.4 | 10.5 | 3.5 | 13.5 | ns |
| $t_{PLZ}$ | | | 3 | 8 | 10.5 | 3 | 13 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.9 | 7 | 3 | 8.5 | ns |
| $t_{PLZ}$ | | | 3 | 5 | 6.5 | 3 | 7.5 | |

## PARAMETER MEASUREMENT INFORMATION

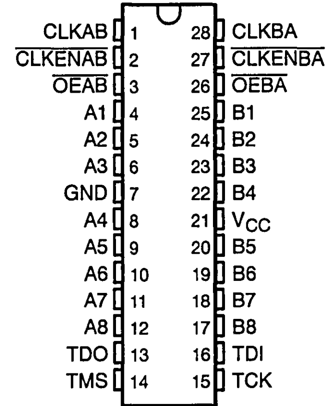



NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

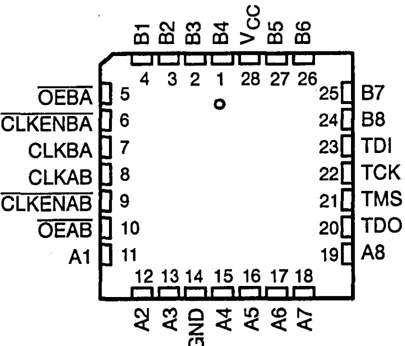
**Figure 14. Load Circuit and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Functionally Equivalent to 'BCT2952 and 'ABT2952 in the Normal-Function Mode
- *SCOPE* ™ Instruction Set
- IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP, and HIGHZ
- Parallel-Signature Analysis at Inputs With Masking Option
- Pseudo-Random Pattern Generation From Outputs
- Sample Inputs/Toggle Outputs
- Binary Count From Outputs
- Even-Parity Opcodes
- Two Boundary-Scan Cells Per I/O for Greater Flexibility
- State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Shrink Small-Outline (DL) and Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Ceramic DIPs (JT)

SN54ABT8952 . . . JT PACKAGE
SN74ABT8952 . . . DL OR DW PACKAGE
(TOP VIEW)




SN54ABT8952 . . . FK PACKAGE
(TOP VIEW)




## description

The 'ABT8952 scan test devices with octal registered bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the 'BCT2952 and 'ABT2952 octal registered bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self-test on the boundary-test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal registered bus transceivers.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

Data flow in each direction is controlled by clock (CLKAB and CLKBA), clock-enable ($\overline{\text{CLKENAB}}$ and $\overline{\text{CLKENBA}}$), and output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, A-bus data is stored in the associated registers on the low-to-high transition of CLKAB, provided that $\overline{\text{CLKENAB}}$ is low. Otherwise, if $\overline{\text{CLKENAB}}$ is high or CLKAB remains at a static low or high level, the register contents are not changed. When $\overline{\text{OEAB}}$ is low, the B outputs are active. When $\overline{\text{OEAB}}$ is high, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B, but uses CLKBA, $\overline{\text{CLKENBA}}$, and $\overline{\text{OEBA}}$.

In the test mode, the normal operation of the SCOPE™ registered bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8952 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8952 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE†**
**(normal mode, each register)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{\text{OEAB}}$ | $\overline{\text{CLKENAB}}$ | CLKAB | A | B |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | H | X | X | $B_0$ |
| L | X | L | X | $B_0$ |
| H | X | X | X | Z |

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, $\overline{\text{CLKENBA}}$, and CLKBA.

## functional block diagram

Pin numbers shown are for the DL, DW, and JT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A1–A8 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| B1–B8 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| CLKAB, CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| $\overline{\text{CLKENAB}}$, $\overline{\text{CLKENBA}}$ | Normal-function clock-enable inputs. See function table for normal-mode logic. |
| GND | Ground |
| $\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$ | Normal-function output-enable inputs. See function table for normal-mode logic. |
| TCK | Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four pins required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four pins required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four pins required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and three test-data registers: a 38-bit boundary-scan register, an 11-bit boundary-control register, and a 1-bit bypass register.

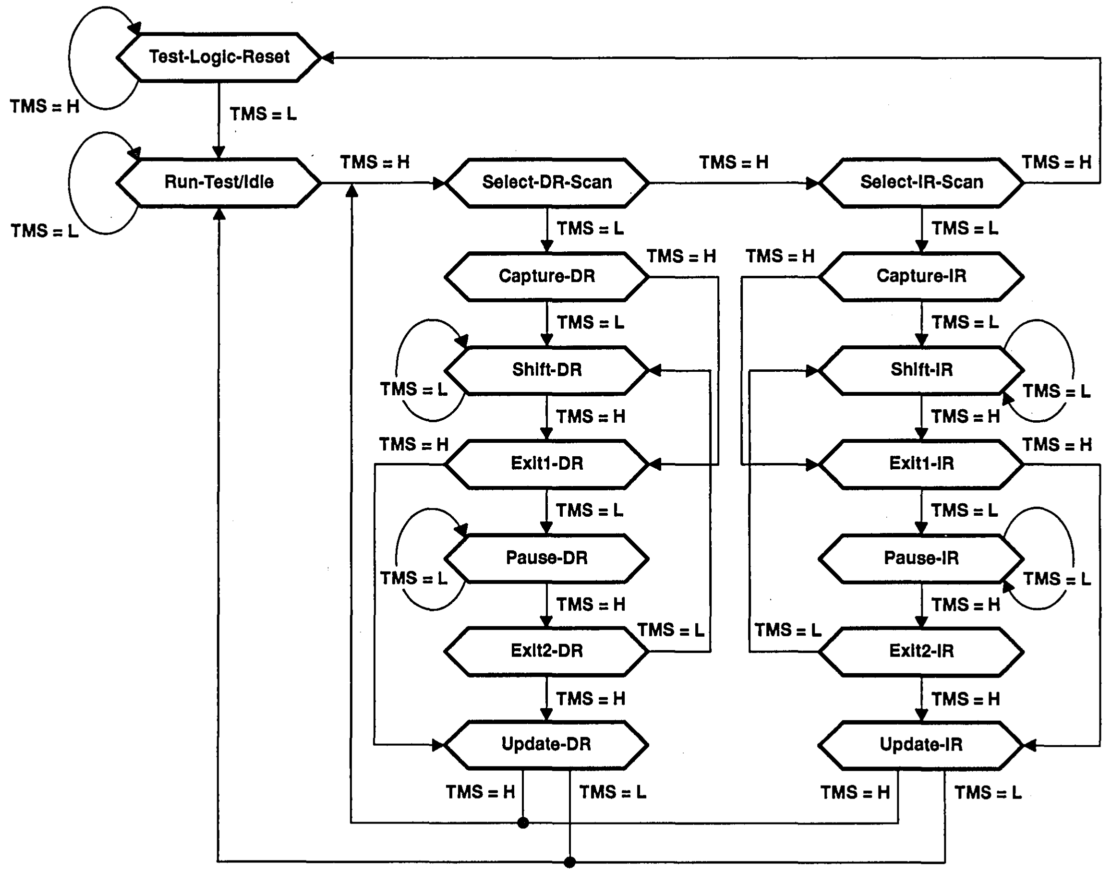


Figure 1. TAP-Controller State Diagram

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8952, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0 except bits 37–36, which are reset to logic 1. The boundary-control register is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

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### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state.

For the 'ABT8952, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass register, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8952. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR order of scan is shown in Figure 2.

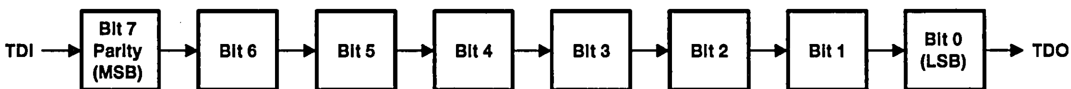


**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 38 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and two BSCs for each normal-function I/O pin (one for input data and one for output data). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0 except BSCs 37–36, which are reset to logic 1.

The BSR order of scan is from TDI through bits 37–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|---|---|---|---|
| 37 | OEAB | 31 | A8-I | 23 | A8-O | 15 | B8-I | 7 | B8-O |
| 36 | OEBA | 30 | A7-I | 22 | A7-O | 14 | B7-I | 6 | B7-O |
| 35 | CLKAB | 29 | A6-I | 21 | A6-O | 13 | B6-I | 5 | B6-O |
| 34 | CLKBA | 28 | A5-I | 20 | A5-O | 12 | B5-I | 4 | B5-O |
| 33 | CLKENAB | 27 | A4-I | 19 | A4-O | 11 | B4-I | 3 | B4-O |
| 32 | CLKENBA | 26 | A3-I | 18 | A3-O | 10 | B3-I | 2 | B3-O |
| — | — | 25 | A2-I | 17 | A2-O | 9 | B2-I | 1 | B2-O |
| — | — | 24 | A1-I | 16 | A1-O | 8 | B1-I | 0 | B1-O |

### boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The BCR order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the BCR bits and their associated test control signals.

**Table 2. Boundary-Control Register Configuration**

| BCR BIT NUMBER | TEST CONTROL SIGNAL | BCR BIT NUMBER | TEST CONTROL SIGNAL | BCR BIT NUMBER | TEST CONTROL SIGNAL |
|---|---|---|---|---|---|
| 10 | MASK8 | 6 | MASK4 | 2 | OPCODE2 |
| 9 | MASK7 | 5 | MASK3 | 1 | OPCODE1 |
| 8 | MASK6 | 4 | MASK2 | 0 | OPCODE0 |
| 7 | MASK5 | 3 | MASK1 | — | — |

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 3.

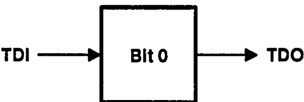


**Figure 3. Bypass Register Order of Scan**

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST/INTEST | Boundary scan | Boundary scan | Test |
| 10000001 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | INTEST/EXTEST | Boundary scan | Boundary scan | Test |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT8952.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

**boundary run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary run test operation to specify which test operation is to be executed.

## boundary-control register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/16-bit mode (PRPG) |
| X10 | Parallel-signature analysis/16-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT) |

In general, while the control input BSCs (bits 37–32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 37–36 of the BSR) do control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when the device is operating in one direction of data flow (that is, $\overline{OEAB} \neq \overline{OEBA}$). Otherwise, the bypass instruction is operated.

## PSA input masking

Bits 10–3 of the BCR specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in Table 3. When the mask bit that corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, i.e., that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. This data also is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Figures 4 and 5 illustrate the 16-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

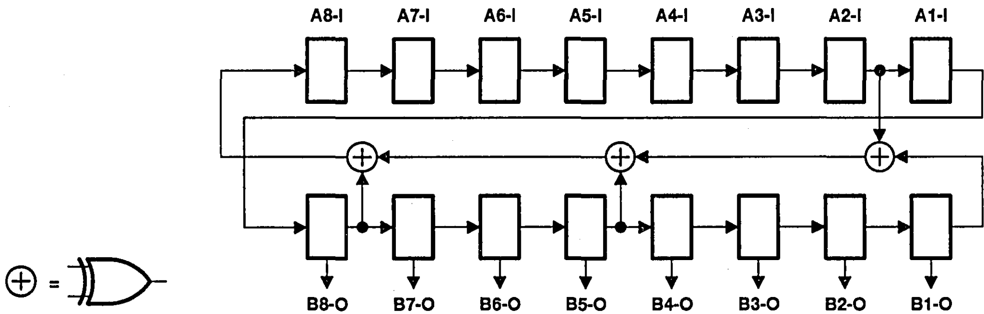


Figure 4. 16-Bit PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

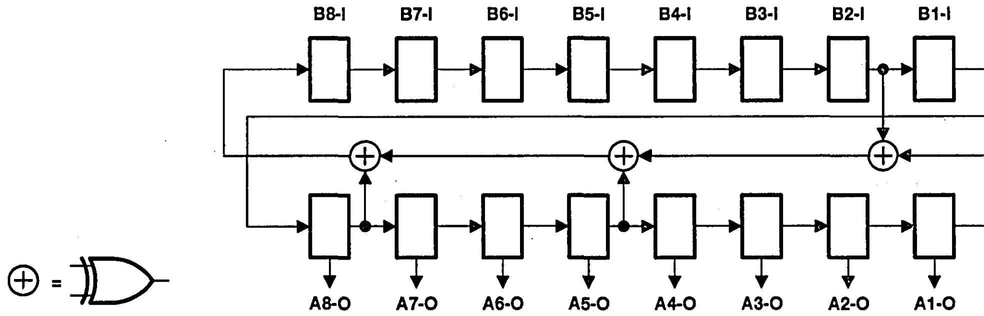


Figure 5. 16-Bit PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

### parallel-signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 6 and 7 illustrate the 16-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

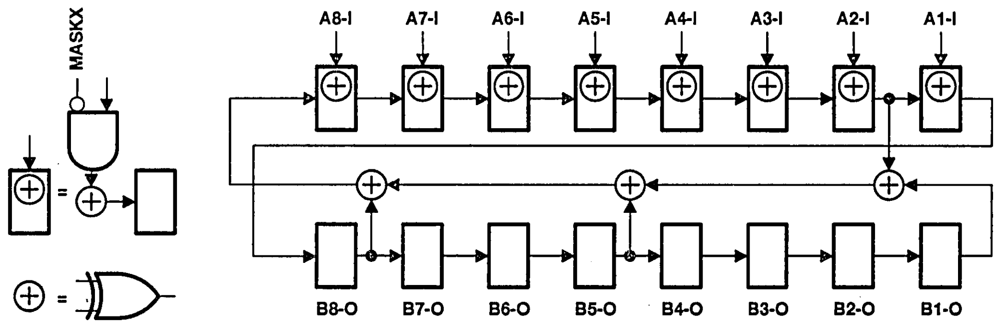


**Figure 6. 16-Bit PSA Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

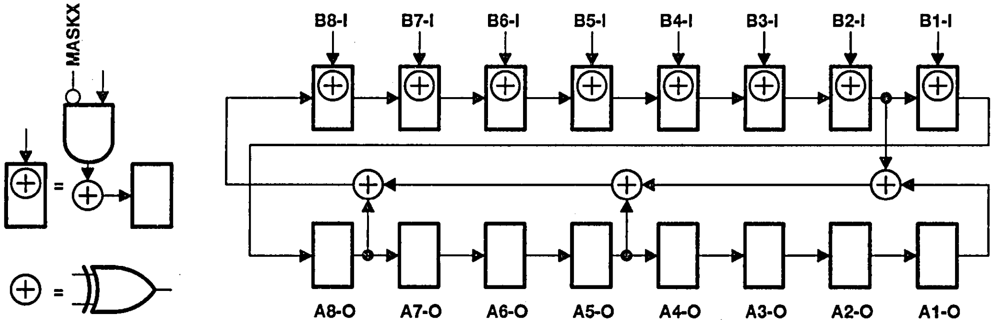


**Figure 7. 16-Bit PSA Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. Figures 8 and 9 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

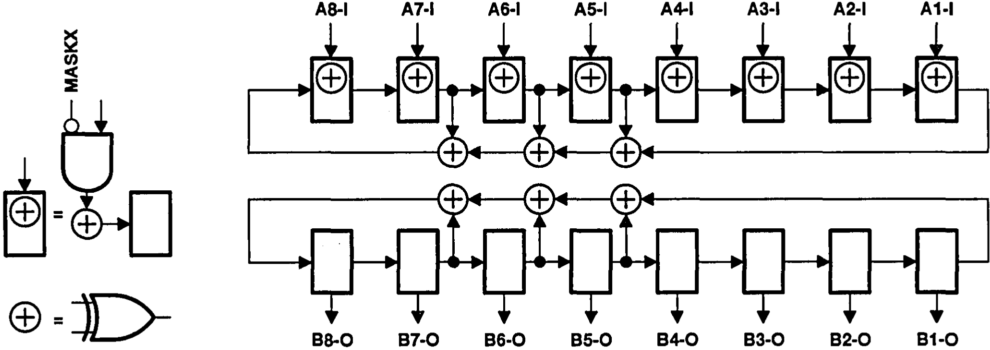


**Figure 8. 8-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

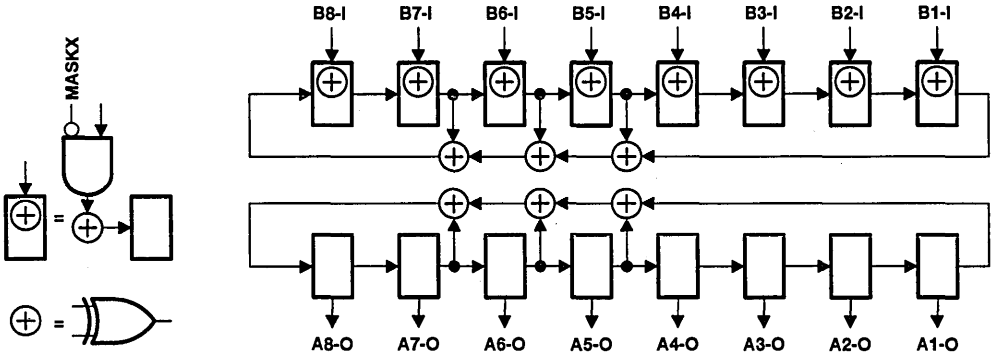


**Figure 9. 8-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. In addition, the shift-register elements of the opposite output BSCs count carries out of the selected output BSCs extending the count to 16 bits. Figures 10 and 11 illustrate the 8-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

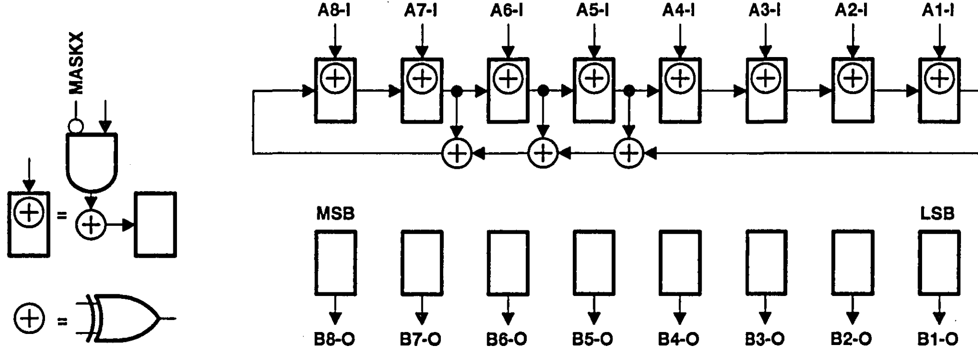


**Figure 10. 8-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

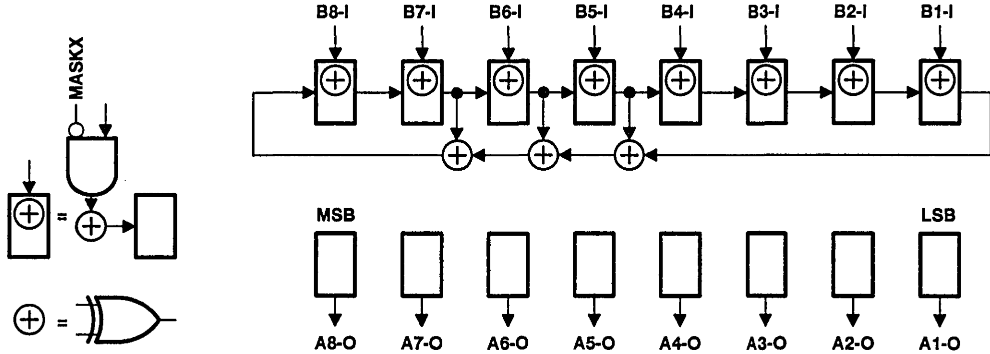


**Figure 11. 8-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

## timing description

All test operations of the 'ABT8952 are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 12. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

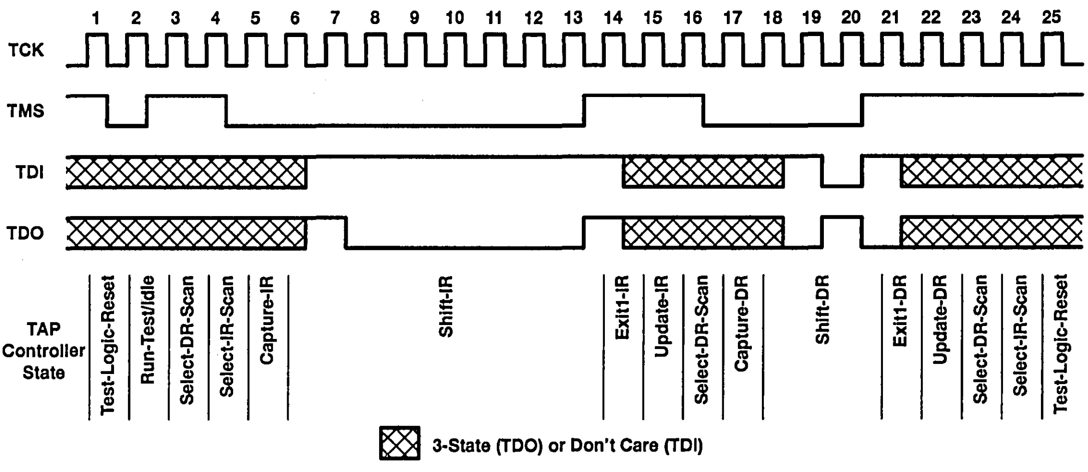


**Figure 12. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .......... –0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .......... –0.5 V to 7 V
Input voltage range, $V_I$ (I/O ports) (see Note 1) .......... –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, $V_O$ .......... –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT8952 .......... 96 mA
SN74ABT8952 .......... 128 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) .......... –18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) .......... –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DL package .......... 0.7 W
DW package .......... 1.7 W
Storage temperature range, $T_{stg}$ .......... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions (see Note 3)

| | | SN54ABT8952 | | SN74ABT8952 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

PRODUCT PREVIEW

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | $T_A$ = 25°C | | | SN54ABT8952 | | SN74ABT8952 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | | 3 | | | 3 | | 3 | | |
| | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | | 2 | | | 2 | | | | |
| | | $I_{OH}$ = –32 mA | | 2* | | | | | 2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | | 0.55 | | 0.55 | | | V |
| | | $I_{OL}$ = 64 mA | | | | 0.55* | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | CLK, $\overline{CLKEN}$, $\overline{OE}$, TCK | | | ±1 | | ±1 | | ±1 | µA |
| | | | A or B ports | | | ±100 | | ±100 | | ±100 | |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | TDI, TMS | | | 10 | | 10 | | 10 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = GND | TDI, TMS | –40 | | –160 | –40 | –160 | –40 | –160 | µA |
| $I_{OZH}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | –50 | | –50 | | –50 | µA |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | | ±100 | | | | ±100 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 2 V, | $V_O$ = 0.5 V or 2.7 V | | | | ±50 | | ±50 | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 2 V to 0, | $V_O$ = 0.5 V or 2.7 V | | | | ±50 | | ±50 | | ±50 | µA |
| $I_{CEX}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | | –50 | –100 | –180 | –50 | –180 | –50 | –180 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | Outputs high | | 0.9 | 2 | | 2 | | 2 | mA |
| | | | Outputs low | | 30 | 38 | | 38 | | 38 | |
| | | | Outputs disabled | | 0.9 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = 2.5 V or 0.5 V | | Control inputs | | 3 | | | | | | pF |
| $C_{io}$ | $V_O$ = 2.5 V or 0.5 V | | A or B ports | | 10 | | | | | | pF |
| $C_o$ | $V_O$ = 2.5 V or 0.5 V | | TDO | | 8 | | | | | | pF |

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

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## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

| | | | SN54ABT8952 | | SN74ABT8952 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | 3 | | 3 | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | 4.5 | | 4.5 | | ns |
| | | $\overline{CLKEN}$ before CLK↑ | 4.5 | | 4.5 | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | 0 | | 0 | | ns |
| | | $\overline{CLKEN}$ after CLK↑ | 0 | | 0 | | |

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

| | | | SN54ABT8952 | | SN74ABT8952 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 5 | | 5 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, $\overline{CLKEN}$, or $\overline{OE}$ before TCK↑ | 5 | | 5 | | ns |
| | | TDI before TCK↑ | 6 | | 6 | | |
| | | TMS before TCK↑ | 6 | | 6 | | |
| $t_h$ | Hold time | A, B, CLK, $\overline{CLKEN}$, or $\overline{OE}$ after TCK↑ | 0 | | 0 | | ns |
| | | TDI after TCK↑ | 0 | | 0 | | |
| | | TMS after TCK↑ | 0 | | 0 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50* | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1* | | 1 | | µs |

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

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### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT8952 | | SN74ABT8952 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLK | A or B | 100 | 130 | | 100 | | 100 | | MHz |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 3 | 4.6 | 5.4 | 3 | 6.5 | 3 | 6.3 | ns |
| $t_{PHL}$ | | | 2.5 | 3.8 | 4.6 | 2.5 | 5.5 | 2.5 | 5.3 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2 | 4.1 | 4.9 | 2 | 5.9 | 2 | 5.8 | ns |
| $t_{PZL}$ | | | 2.5 | 4.7 | 5.5 | 2.5 | 7.1 | 2.5 | 6.9 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2.5 | 5.3 | 6.1 | 2.5 | 7.5 | 2.5 | 7.3 | ns |
| $t_{PLZ}$ | | | 3 | 4.5 | 5.3 | 3 | 6.3 | 3 | 6.1 | |

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT8952 | | SN74ABT8952 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3.5 | 8 | 9.5 | 3.5 | 12.5 | 3.5 | 12 | ns |
| $t_{PHL}$ | | | 3 | 7.7 | 9 | 3 | 12 | 3 | 11.5 | |
| $t_{PLH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 7 | 2.5 | 6.5 | ns |
| $t_{PHL}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 7 | 2.5 | 6.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4.5 | 8.2 | 9.5 | 4.5 | 12.5 | 4.5 | 12 | ns |
| $t_{PZL}$ | | | 4.5 | 9 | 10.5 | 4.5 | 13.5 | 4.5 | 13 | |
| $t_{PZH}$ | TCK↓ | TDO | 2.5 | 4.3 | 5.5 | 2.5 | 7 | 2.5 | 6.5 | ns |
| $t_{PZL}$ | | | 2.5 | 4.9 | 6 | 2.5 | 7.5 | 2.5 | 7 | |
| $t_{PHZ}$ | TCK↓ | A or B | 3.5 | 8.4 | 10.5 | 3.5 | 14 | 3.5 | 13.5 | ns |
| $t_{PLZ}$ | | | 3 | 8 | 10.5 | 3 | 13.5 | 3 | 13 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.9 | 7 | 3 | 9 | 3 | 8.5 | ns |
| $t_{PLZ}$ | | | 3 | 5 | 6.5 | 3 | 8 | 3 | 7.5 | |

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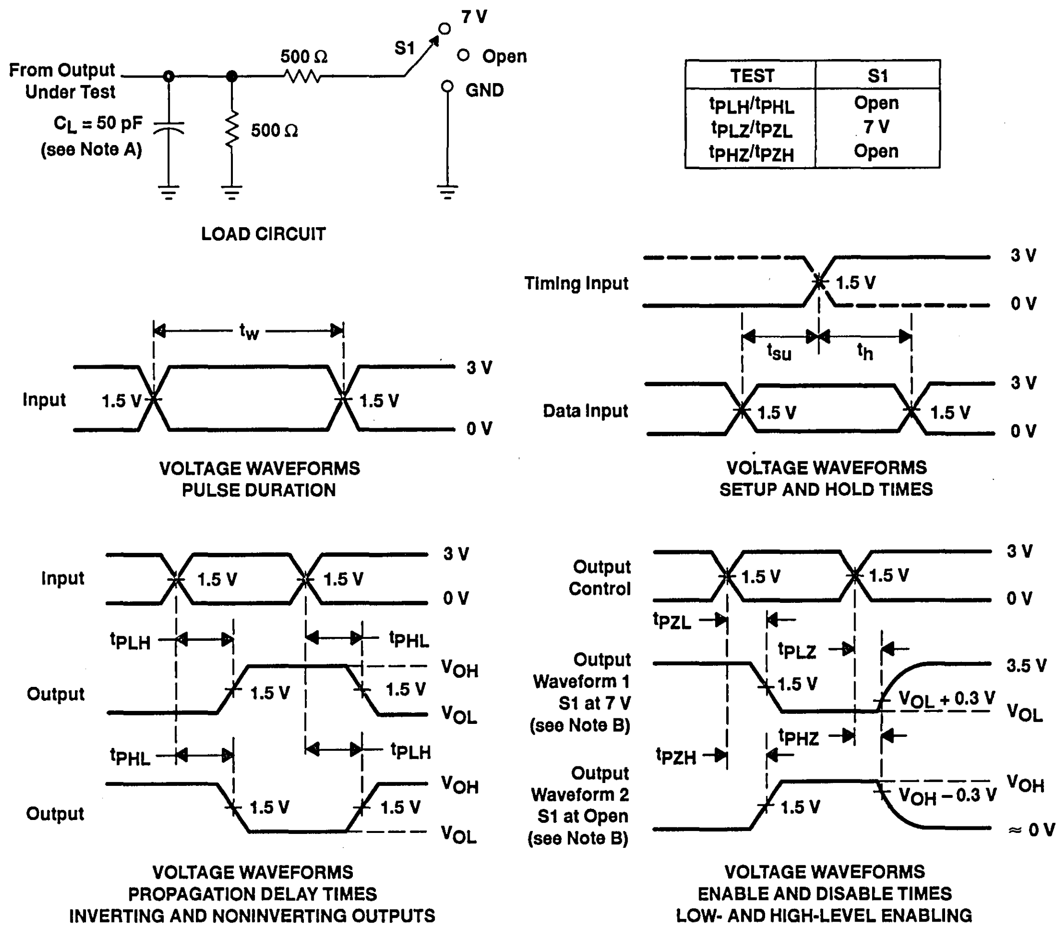
## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 13. Load Circuit and Voltage Waveforms**

General Information 1

SN54/74BCT Octals 2

SN54/74ABT Octals 3

SN54/74ABT Widebus™ With Dual-Sided Terminals 4

SN54/74ABT Widebus™ With Quad-Sided Terminals 5

SN54/74LVT Widebus™ With Dual-Sided Terminals 6

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- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages

SN54ABT18245A . . . WD PACKAGE
SN74ABT18245A . . . DGG OR DL PACKAGE
(TOP VIEW)

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| 1DIR | 1 | 56 | 1$\overline{\text{OE}}$ |
| 1B1 | 2 | 55 | 1A1 |
| 1B2 | 3 | 54 | 1A2 |
| GND | 4 | 53 | GND |
| 1B3 | 5 | 52 | 1A3 |
| 1B4 | 6 | 51 | 1A4 |
| $V_{CC}$ | 7 | 50 | $V_{CC}$ |
| 1B5 | 8 | 49 | 1A5 |
| 1B6 | 9 | 48 | 1A6 |
| 1B7 | 10 | 47 | 1A7 |
| GND | 11 | 46 | GND |
| 1B8 | 12 | 45 | 1A8 |
| 1B9 | 13 | 44 | 1A9 |
| 2B1 | 14 | 43 | 2A1 |
| 2B2 | 15 | 42 | 2A2 |
| 2B3 | 16 | 41 | 2A3 |
| 2B4 | 17 | 40 | 2A4 |
| GND | 18 | 39 | GND |
| 2B5 | 19 | 38 | 2A5 |
| 2B6 | 20 | 37 | 2A6 |
| 2B7 | 21 | 36 | 2A7 |
| $V_{CC}$ | 22 | 35 | $V_{CC}$ |
| 2B8 | 23 | 34 | 2A8 |
| 2B9 | 24 | 33 | 2A9 |
| GND | 25 | 32 | GND |
| 2DIR | 26 | 31 | 2$\overline{\text{OE}}$ |
| TDO | 27 | 30 | TDI |
| TMS | 28 | 29 | TCK |

## description

The 'ABT18245A scan test devices with 18-bit bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit noninverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{\text{OE}}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at DIR. $\overline{\text{OE}}$ can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the input/output (I/O) boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

Four dedicated test pins observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN74ABT18245A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT18245A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT18245A is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(normal mode, each 9-bit section)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## functional block diagram

Boundary-Scan Register

1DIR 1
1OE 56
1A1 55
2 1B1
One of Nine Channels
2DIR 26
2OE 31
2A1 43
14 2B1
One of Nine Channels
Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller
VCC
TDI 30
VCC
TMS 28
TCK 29
27 TDO

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1DIR, 2DIR | Normal-function direction controls. See function table for normal-mode logic. |
| GND | Ground |
| $1\overline{OE}$, $2\overline{OE}$ | Normal-function output enables. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and four test-data registers: a 44-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. TMS has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT18245A, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 43–40 in the boundary-scan register are reset to logic 0, ensuring that these cells, which control the A-port and B-port outputs are set to benign values (i.e., if test mode were invoked, the outputs would be at the high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, such updates occur on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'ABT18245A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT18245A. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

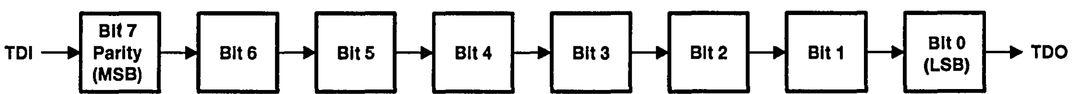



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 44 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, one BSC for each normal-function I/O pin (one single cell for both input data and output data), and one BSC for each of the internally decoded output-enable signals (1OEA, 2OEA, 1OEB, 2OEB). The BSR is used to store test data that is to be applied externally to the device output pins, and/or to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle, as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 43–40 are reset to logic 0, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at the high-impedance state). Reset values of other BSCs should be considered indeterminate.

When external data is to be captured, the BSCs for signals 1OEA, 2OEA, 1OEB, and 2OEB capture logic values determined by the following positive-logic equations: $1OEA = \overline{1OE} \bullet \overline{1DIR}$, $2OEA = \overline{2OE} \bullet \overline{2DIR}$, $1OEB = \overline{1OE} \bullet DIR$, and $2OEB = \overline{2OE} \bullet DIR$. When data is to be applied externally, these BSCs control the drive state (active or high impedance) of their respective outputs.

The BSR order of scan is from TDI through bits 43–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|---|---|---|---|
| 43 | 2OEB | 35 | 2A9-I/O | 26 | 1A9-I/O | 17 | 2B9-I/O | 8 | 1B9-I/O |
| 42 | 1OEB | 34 | 2A8-I/O | 25 | 1A8-I/O | 16 | 2B8-I/O | 7 | 1B8-I/O |
| 41 | 2OEA | 33 | 2A7-I/O | 24 | 1A7-I/O | 15 | 2B7-I/O | 6 | 1B7-I/O |
| 40 | 1OEA | 32 | 2A6-I/O | 23 | 1A6-I/O | 14 | 2B6-I/O | 5 | 1B6-I/O |
| 39 | 2DIR | 31 | 2A5-I/O | 22 | 1A5-I/O | 13 | 2B5-I/O | 4 | 1B5-I/O |
| 38 | 1DIR | 30 | 2A4-I/O | 21 | 1A4-I/O | 12 | 2B4-I/O | 3 | 1B4-I/O |
| 37 | $\overline{2OE}$ | 29 | 2A3-I/O | 20 | 1A3-I/O | 11 | 2B3-I/O | 2 | 1B3-I/O |
| 36 | $\overline{1OE}$ | 28 | 2A2-I/O | 19 | 1A2-I/O | 10 | 2B2-I/O | 1 | 1B2-I/O |
| — | — | 27 | 2A1-I/O | 18 | 1A1-I/O | 9 | 2B1-I/O | 0 | 1B1-I/O |

### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run test (RUNT) instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

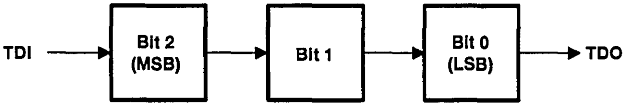



**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

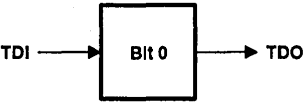



**Figure 4. Bypass Register Order of Scan**

### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

During Capture-DR, the binary value 00010000000000000101000000101111 (1000502F, hex) is captured in the IDR to identify this device as Texas Instruments SN54/74ABT18245A. The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary-run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT18245A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device I/O pins is passed through the I/O BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 43–40 of the BSR). When a given output enable is active (logic 1), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

### control boundary to high impedance

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

### control boundary to 1/0

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

### boundary-run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

### boundary read

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

### boundary self test

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

### boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

### boundary-control-register scan

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 43–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 43–40 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when both bytes of the device are operating in one direction of data flow (i.e., 1OEA ≠ 1OEB and 2OEA ≠ 2OEB) and in the same direction of data flow (i.e., 1OEA = 2OEA and 1OEB = 2OEB). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 illustrate the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

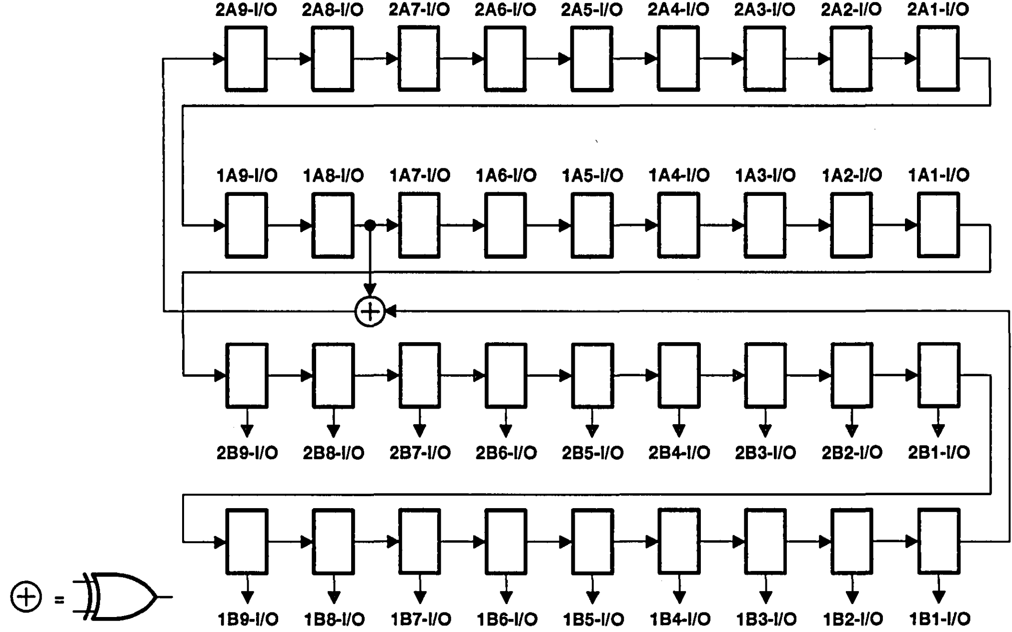



**Figure 5. 36-Bit PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

**pseudo-random pattern generation (PRPG) (continued)**

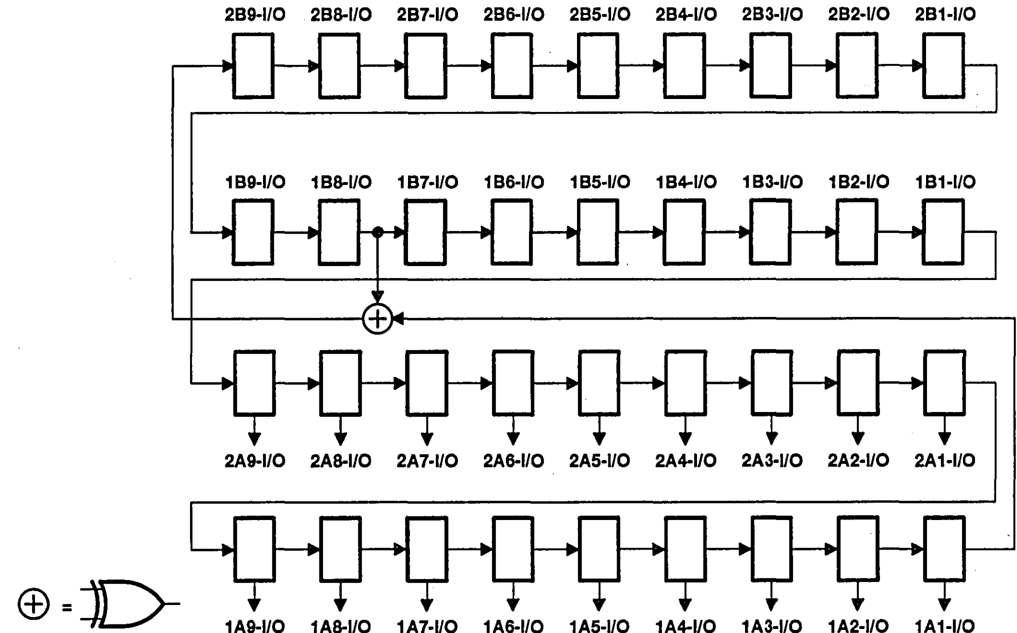



**Figure 6. 36-Bit PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 illustrate the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

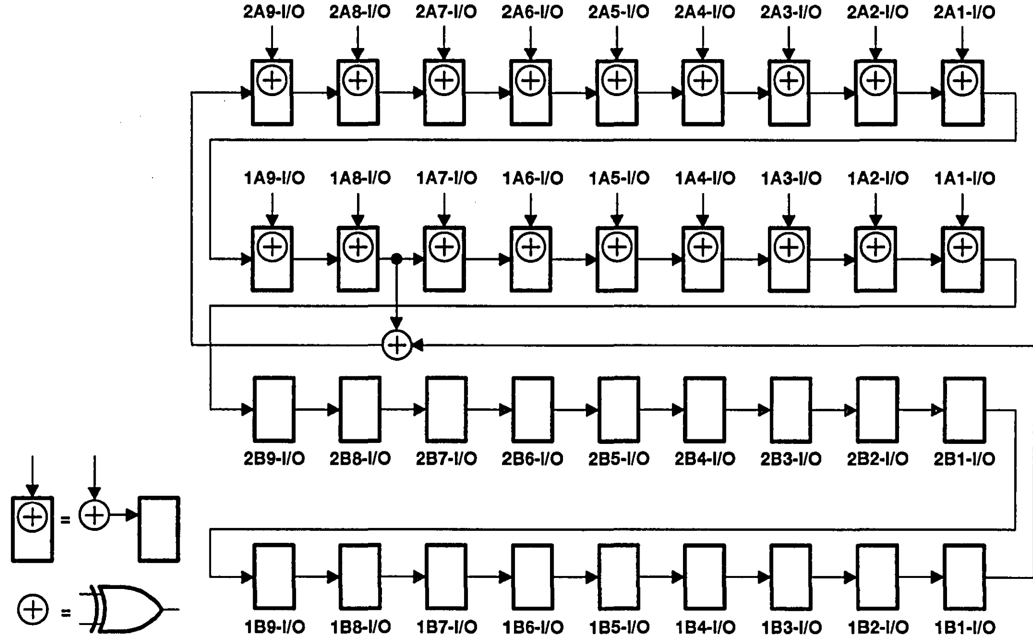



**Figure 7. 36-Bit PSA Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

**parallel-signature analysis (PSA) (continued)**

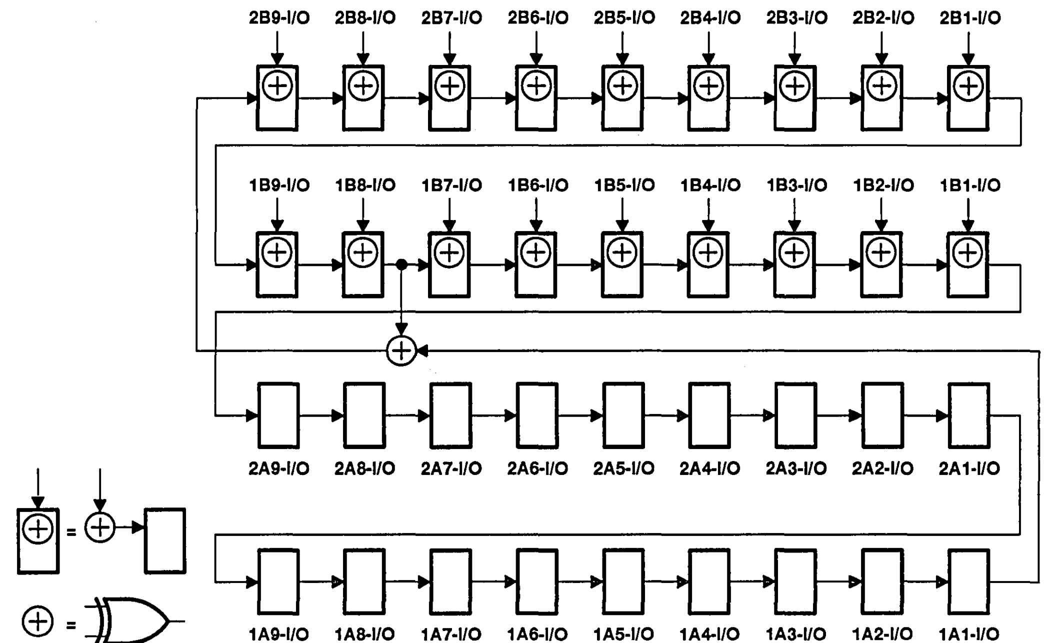



**Figure 8. 36-Bit PSA Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

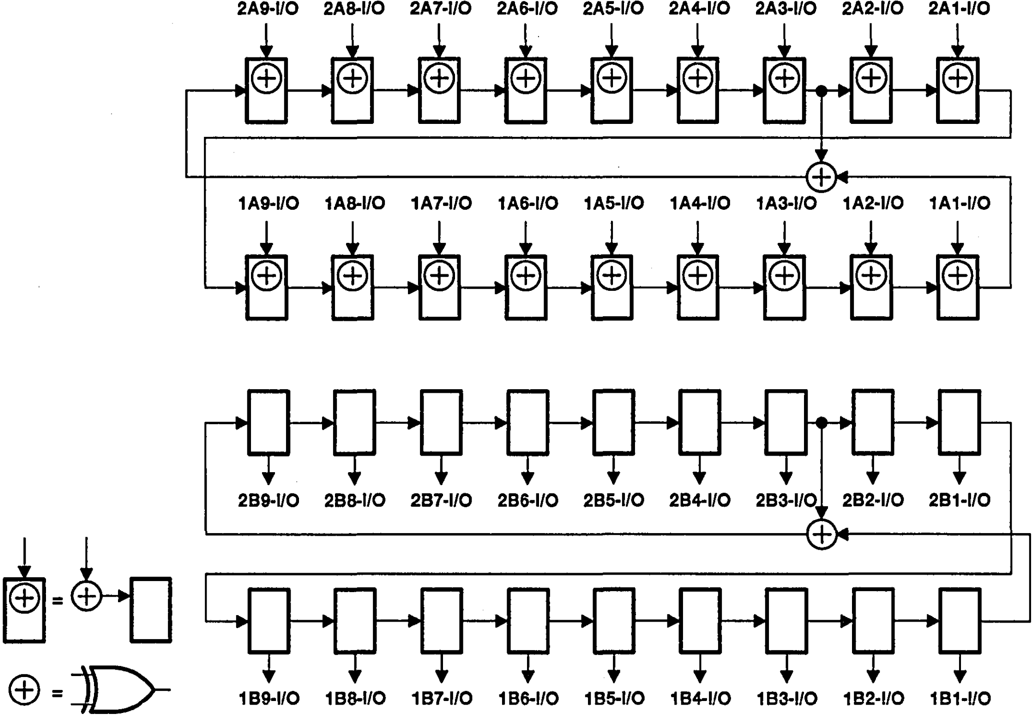



**Figure 9. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

**simultaneous PSA and PRPG (PSA/PRPG) (continued)**

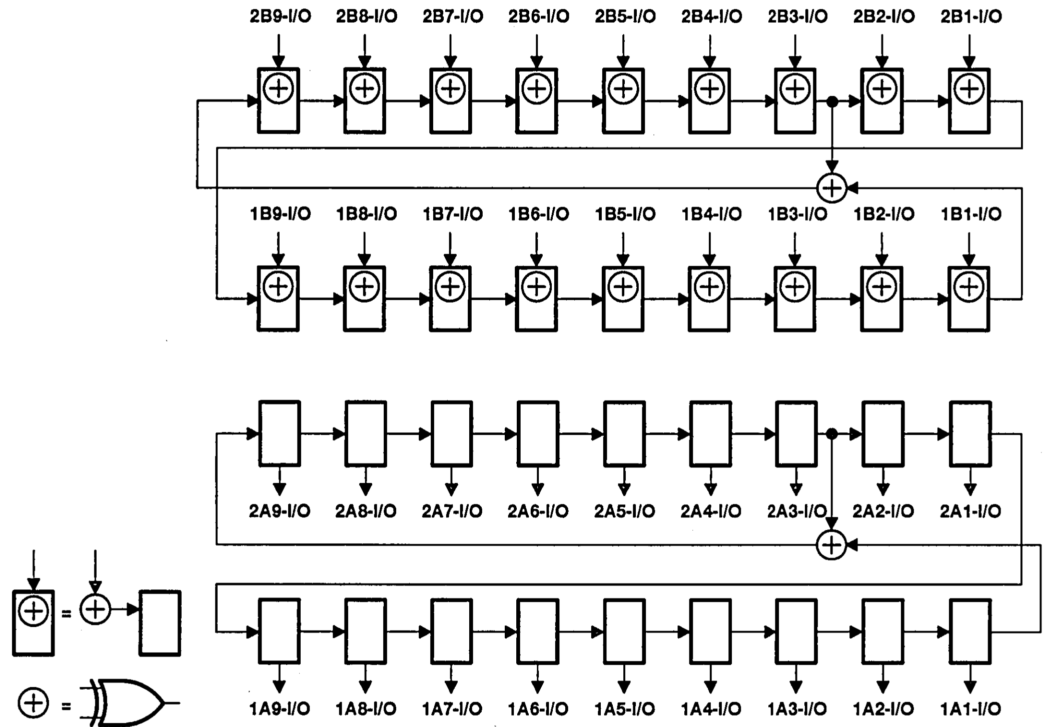



**Figure 10. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

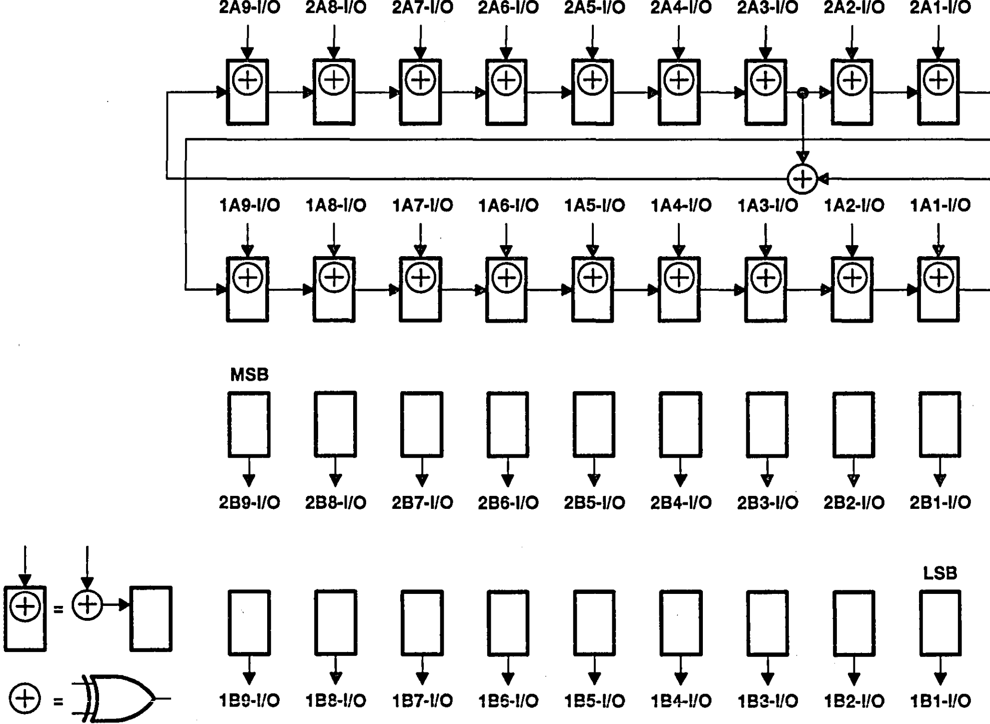



**Figure 11. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

**simultaneous PSA and binary count up (PSA/COUNT) (continued)**

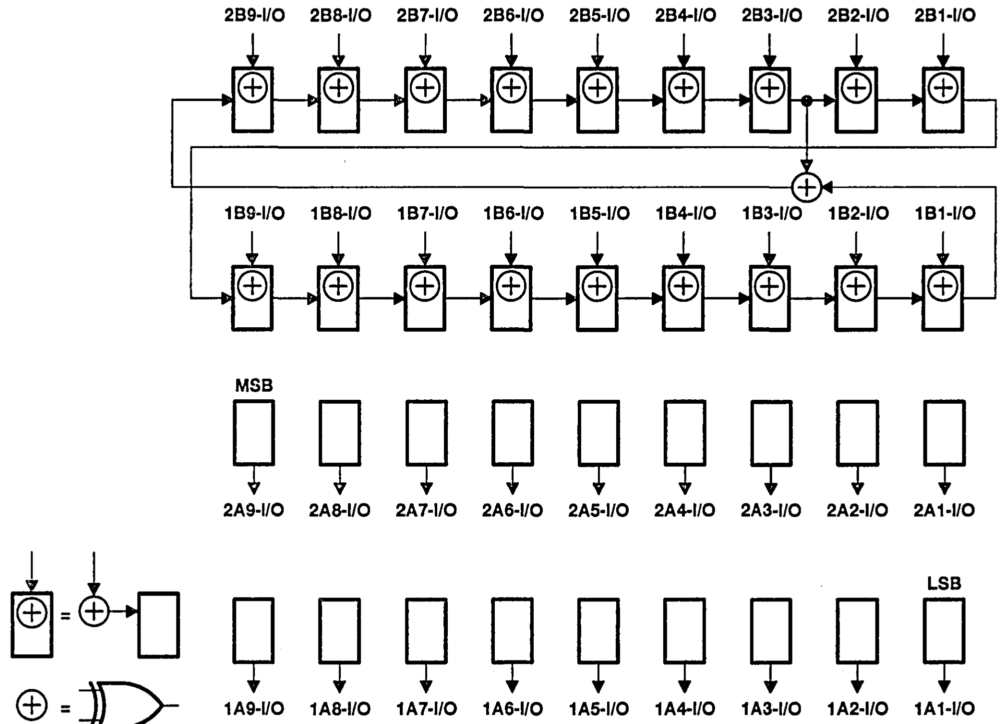



**Figure 12. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

## timing description

All test operations of the 'ABT18245A are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | The selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

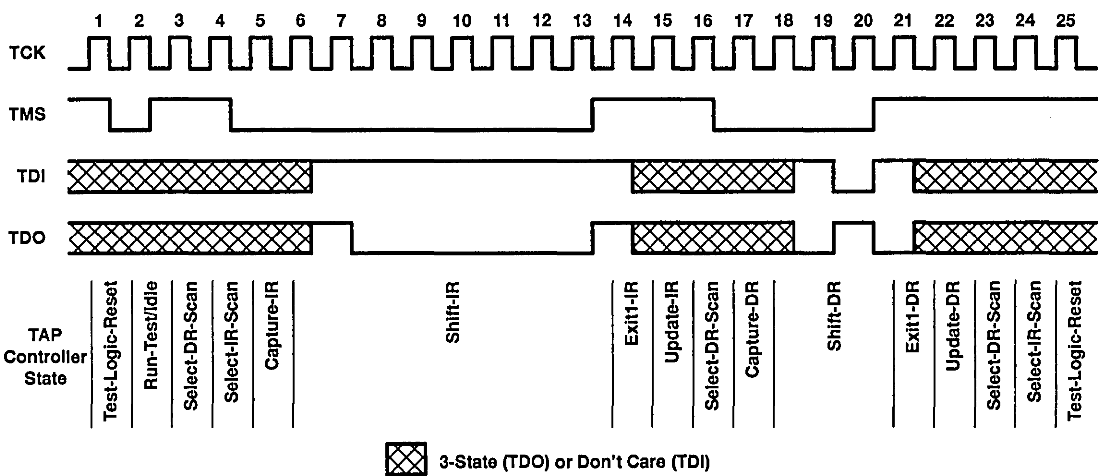



**Figure 13. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$ (except I/O ports) (see Note 1) | –0.5 V to 7 V |
| Input voltage range, $V_I$ (I/O ports) (see Note 1) | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$: SN54ABT18245A | 96 mA |
| SN74ABT18245A | 128 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | –18 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | –50 mA |
| Continuous current through $V_{CC}$ | 576 mA |
| Continuous current through GND | 1152 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DGG package | 1 W |
| DL package | 1.4 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions (see Note 3)

| | | SN54ABT18245A | | SN74ABT18245A | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT18245A | | SN74ABT18245A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, $I_I$ = –18 mA | | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, $I_{OH}$ = –3 mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | $V_{CC}$ = 5 V, $I_{OH}$ = –3 mA | | 3 | | | 3 | | 3 | | |
| | $V_{CC}$ = 4.5 V, $I_{OH}$ = –24 mA | | 2 | | | 2 | | | | |
| | $V_{CC}$ = 4.5 V, $I_{OH}$ = –32 mA | | 2* | | | | | 2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | DIR, $\overline{OE}$, TCK | | | ±1 | | ±1 | | ±1 | µA |
| | | A or B ports | | | ±100 | | ±100 | | ±100 | |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ | TDI, TMS | | | 10 | | 10 | | 10 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, $V_I$ = GND | TDI, TMS | –40 | | –150 | –40 | –150 | –40 | –150 | µA |
| $I_{OZH}$‡ | $V_{CC}$ = 5.5 V, $V_O$ = 2.7 V | | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$‡ | $V_{CC}$ = 5.5 V, $V_O$ = 0.5 V | | | | –50 | | –50 | | –50 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 2 V, $V_O$ = 2.7 V or 0.5 V | $\overline{OE}$ = 0.8 V | | | ±50 | | ±50 | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 2 V to 0, $V_O$ = 2.7 V or 0.5 V | $\overline{OE}$ = 0.8 V | | | ±50 | | ±50 | | ±50 | µA |
| $I_{off}$ | $V_{CC}$ = 0, $V_I$ or $V_O$ ≤ 4.5 V | | | | ±100 | | ±450 | | ±100 | µA |
| $I_{CEX}$ | $V_{CC}$ = 5.5 V, $V_O$ = 5.5 V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | $V_{CC}$ = 5.5 V, $V_O$ = 2.5 V | | –50 | –110 | –200 | –50 | –200 | –50 | –200 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND; A or B ports | Outputs high | | 3.5 | 5 | | 5 | | 5 | mA |
| | | Outputs low | | 33 | 38 | | 38 | | 38 | |
| | | Outputs disabled | | 2.9 | 4.5 | | 4.5 | | 4.5 | |
| $\Delta I_{CC}$¶ | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 50 | | 50 | | 50 | µA |
| $C_i$ | $V_I$ = 2.5 V or 0.5 V | Control inputs | | 3 | | | 9.8 | | | pF |
| $C_{io}$ | $V_O$ = 2.5 V or 0.5 V | A or B ports | | 10 | | | 12.6 | | | pF |
| $C_o$ | $V_O$ = 2.5 V or 0.5 V | TDO | | 8 | | | 11.4 | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| | | | SN54ABT18245A | | SN74ABT18245A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 8.1 | | 8.1 | | ns |
| $t_{su}$ | Setup time | A, B, DIR, or $\overline{OE}$ before TCK↑ | 9.5 | | 7 | | ns |
| | | TDI before TCK↑ | 4.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3.6 | | 3.6 | | |
| $t_h$ | Hold time | A, B, DIR, or $\overline{OE}$ after TCK↑ | 0.7 | | 0 | | ns |
| | | TDI after TCK↑ | 0 | | 0 | | |
| | | TMS after TCK↑ | 0.5 | | 0.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50* | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1* | | 1 | | µs |

* On products compliant to MIL-PRF-38535, these parameters are not production tested.

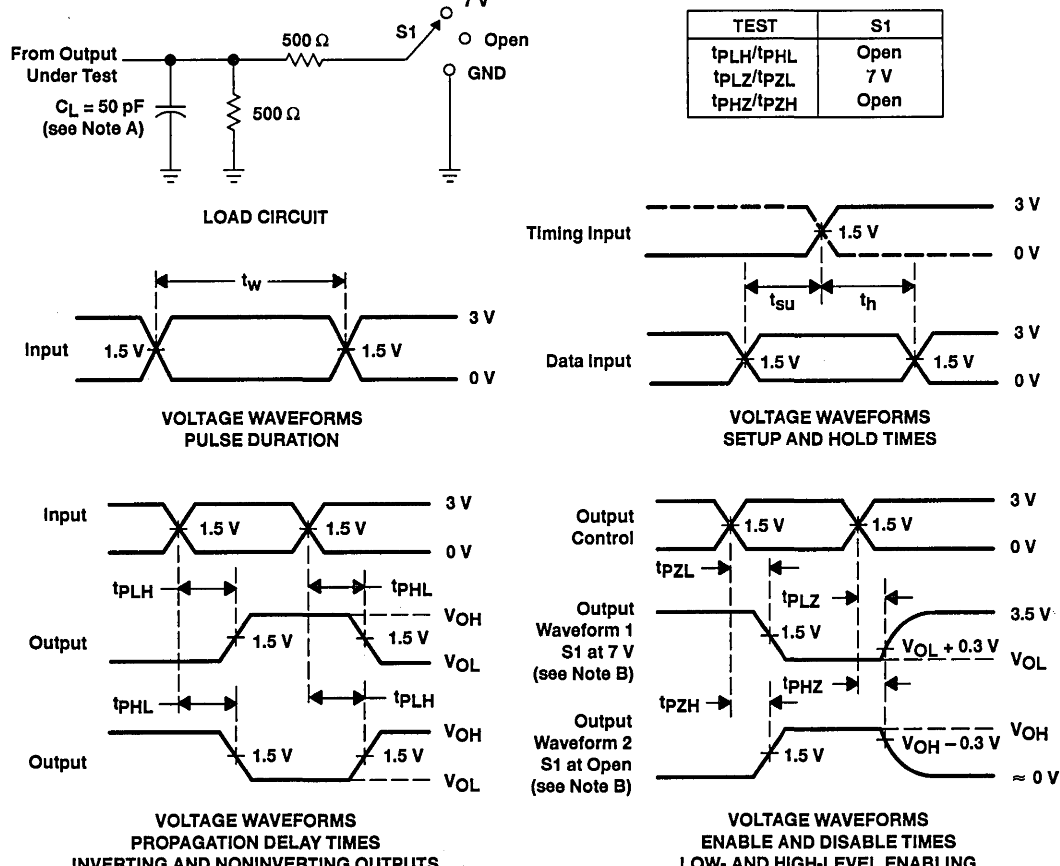
### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT18245A | | SN74ABT18245A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1.5 | 2.8 | 4.1 | 1.5 | 5.1 | 1.5 | 4.8 | ns |
| $t_{PHL}$ | | | 1.5 | 3.1 | 4.6 | 1.5 | 5.8 | 1.5 | 5.4 | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | 2 | 4.7 | 5.8 | 2 | 8.1 | 2 | 7.5 | ns |
| $t_{PZL}$ | | | 2 | 4.5 | 6.2 | 2 | 8.5 | 2 | 8 | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | 2.5 | 5.8 | 6.8 | 2.5 | 9.5 | 2.5 | 8.5 | ns |
| $t_{PLZ}$ | | | 2.5 | 4.8 | 6 | 2.5 | 8.5 | 2.5 | 7.5 | |

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT18245A | | SN74ABT18245A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK↓ | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3 | 7.1 | 10.1 | 3 | 14 | 3 | 13.1 | ns |
| $t_{PHL}$ | | | 3 | 7 | 10.1 | 2.8 | 13.8 | 3 | 12.8 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.4 | 5 | 2 | 6.4 | 2 | 6.1 | ns |
| $t_{PHL}$ | | | 2 | 3.9 | 5.6 | 2 | 7 | 2 | 6.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 7.5 | 10.6 | 4 | 14.1 | 4 | 13.4 | ns |
| $t_{PZL}$ | | | 4 | 7.6 | 10.5 | 4 | 14.3 | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.8 | 5.5 | 2 | 7 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2.5 | 4 | 5.7 | 2.3 | 7.3 | 2.5 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 3.5 | 7.7 | 10.8 | 2.9 | 14.4 | 3.5 | 13.6 | ns |
| $t_{PLZ}$ | | | 2.5 | 7.1 | 10.1 | 2.5 | 13.8 | 2.5 | 12.7 | |
| $t_{PHZ}$ | TCK↓ | TDO | 2 | 3.9 | 5.7 | 2 | 7.5 | 2 | 7.2 | ns |
| $t_{PLZ}$ | | | 1.5 | 3.5 | 5.4 | 1.5 | 6.7 | 1.5 | 6.3 | |

## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ**
  - **Parallel-Signature Analysis at Inputs**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages**

**SN54ABT18640 . . . WD PACKAGE**
**SN74ABT18640 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**

| Pin name | Pin | Pin | Pin name |
|---|---|---|---|
| 1DIR | 1 | 56 | $1\overline{OE}$ |
| 1B1 | 2 | 55 | 1A1 |
| 1B2 | 3 | 54 | 1A2 |
| GND | 4 | 53 | GND |
| 1B3 | 5 | 52 | 1A3 |
| 1B4 | 6 | 51 | 1A4 |
| $V_{CC}$ | 7 | 50 | $V_{CC}$ |
| 1B5 | 8 | 49 | 1A5 |
| 1B6 | 9 | 48 | 1A6 |
| 1B7 | 10 | 47 | 1A7 |
| GND | 11 | 46 | GND |
| 1B8 | 12 | 45 | 1A8 |
| 1B9 | 13 | 44 | 1A9 |
| 2B1 | 14 | 43 | 2A1 |
| 2B2 | 15 | 42 | 2A2 |
| 2B3 | 16 | 41 | 2A3 |
| 2B4 | 17 | 40 | 2A4 |
| GND | 18 | 39 | GND |
| 2B5 | 19 | 38 | 2A5 |
| 2B6 | 20 | 37 | 2A6 |
| 2B7 | 21 | 36 | 2A7 |
| $V_{CC}$ | 22 | 35 | $V_{CC}$ |
| 2B8 | 23 | 34 | 2A8 |
| 2B9 | 24 | 33 | 2A9 |
| GND | 25 | 32 | GND |
| 2DIR | 26 | 31 | $2\overline{OE}$ |
| TDO | 27 | 30 | TDI |
| TMS | 28 | 29 | TCK |

## description

The ’ABT18640 scan test devices with 18-bit inverting bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit inverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at DIR. $\overline{OE}$ can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

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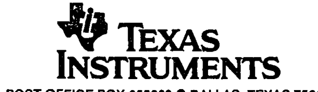



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

Four dedicated test pins observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN74ABT18640 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT18640 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT18640 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(normal mode, each 9-bit section)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | $\overline{B}$ data to A bus |
| L | H | $\overline{A}$ data to B bus |
| H | X | Isolation |

## functional block diagram

Boundary-Scan Register

1DIR 1
1OE 56
1A1 55
2 1B1
One of Nine Channels
2DIR 26
2OE 31
2A1 43
14 2B1
One of Nine Channels

Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller

$V_{CC}$
TDI 30
$V_{CC}$
TMS 28
TCK 29
27 TDO

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1DIR, 2DIR | Normal-function direction controls. See function table for normal-mode logic. |
| GND | Ground |
| $1\overline{OE}$, $2\overline{OE}$ | Normal-function output enables. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test-data registers: a 44-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

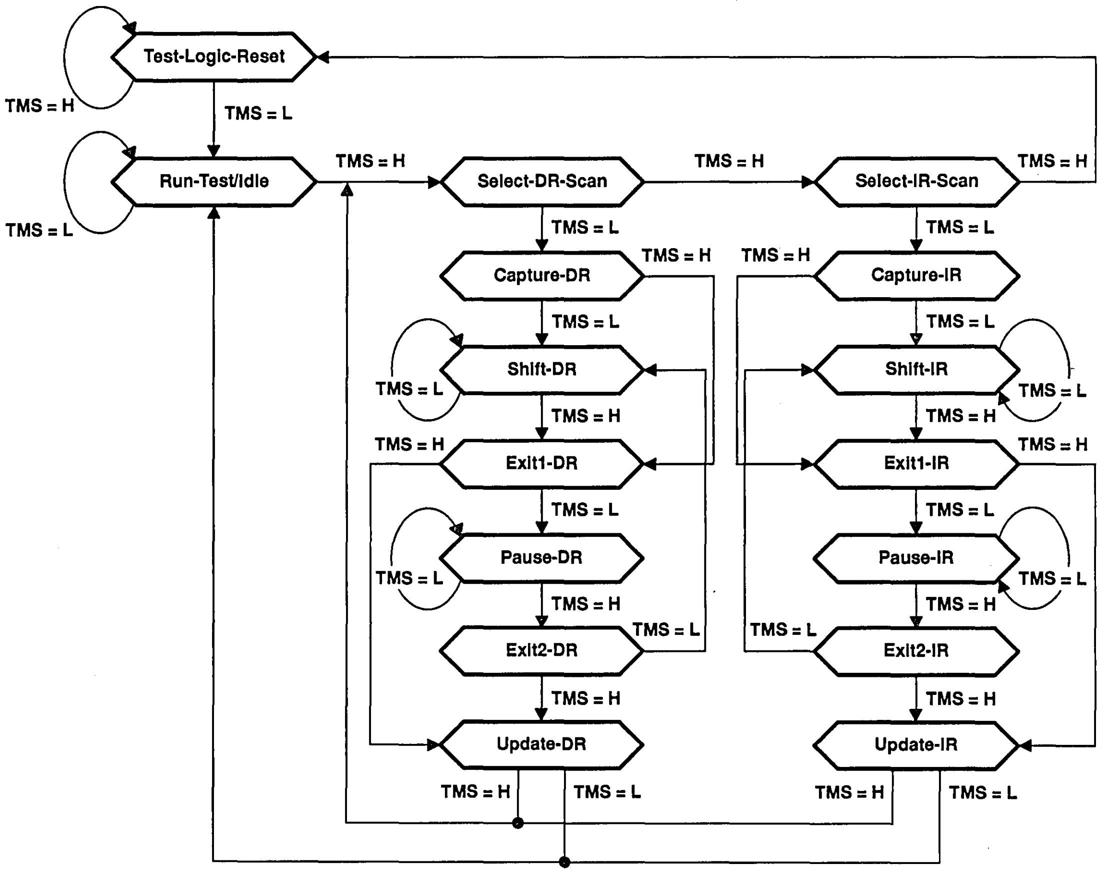


Figure 1. TAP-Controller State Diagram

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT18640, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 43–44 in the boundary-scan register are reset to logic 0, ensuring that these cells which control the A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at the high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register captures a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

**Shift-DR**

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO is enabled to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'ABT18640, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO is enabled to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT18640. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

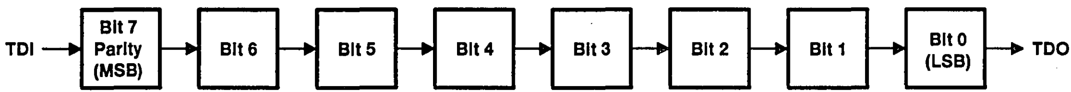


**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 44 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, one BSC for each normal-function I/O pin (one single cell for both input data and output data), and one BSC for each of the internally decoded output-enable signals (1OEA, 2OEA, 1OEB, 2OEB). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 43–40 are reset to logic 0, ensuring that these cells, which contol A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at the high-impedance state). Reset values of other BSCs should be considered indeterminate.

### boundary-scan register (continued)

When external data is to be captured, the BSCs for signals 1OEA, 2OEA, 1OEB, and 2OEB capture logic values determined by the following positive-logic equations:

$1OEA = \overline{1OE} \bullet \overline{1DIR}$, $2OEA = \overline{2OE} \bullet \overline{2DIR}$, $1OEB = \overline{1OE} \bullet DIR$, and $2OEB = \overline{2OE} \bullet DIR$

When data is to be applied externally, these BSCs control the drive state (active or high impedance) of their respective outputs.

The BSR order of scan is from TDI through bits 43–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|---|---|---|---|
| 43 | 2OEB | 35 | 2A9-I/O | 26 | 1A9-I/O | 17 | 2B9-I/O | 8 | 1B9-I/O |
| 42 | 1OEB | 34 | 2A8-I/O | 25 | 1A8-I/O | 16 | 2B8-I/O | 7 | 1B8-I/O |
| 41 | 2OEA | 33 | 2A7-I/O | 24 | 1A7-I/O | 15 | 2B7-I/O | 6 | 1B7-I/O |
| 40 | 1OEA | 32 | 2A6-I/O | 23 | 1A6-I/O | 14 | 2B6-I/O | 5 | 1B6-I/O |
| 39 | 2DIR | 31 | 2A5-I/O | 22 | 1A5-I/O | 13 | 2B5-I/O | 4 | 1B5-I/O |
| 38 | 1DIR | 30 | 2A4-I/O | 21 | 1A4-I/O | 12 | 2B4-I/O | 3 | 1B4-I/O |
| 37 | $\overline{2OE}$ | 29 | 2A3-I/O | 20 | 1A3-I/O | 11 | 2B3-I/O | 2 | 1B3-I/O |
| 36 | $\overline{1OE}$ | 28 | 2A2-I/O | 19 | 1A2-I/O | 10 | 2B2-I/O | 1 | 1B2-I/O |
| — | — | 27 | 2A1-I/O | 18 | 1A1-I/O | 9 | 2B1-I/O | 0 | 1B1-I/O |

### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run test (RUNT) instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

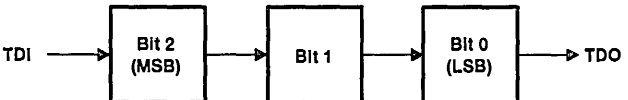


**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

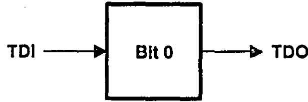


**Figure 4. Bypass Register Order of Scan**

### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

During Capture-DR, the binary value 00000000000000001110000000101111 (0000E02F, hex) is captured in the IDR to identify this device as Texas Instruments SN54/74ABT18640. The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary-run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABT18640.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device I/O pins is passed through the I/O BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 43–40 of the BSR). When a given output enable is active (logic 1), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE<br>BIT 2 → BIT 0<br>MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 43–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 43–40 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when both bytes of the device are operating in one direction of data flow (that is, 1OEA ≠ 1OEB and 2OEA ≠ 2OEB) and in the same direction of data flow (that is, 1OEA = 2OEA and 1OEB = 2OEB). Otherwise, the bypass instruction is performed.

### sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 show the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

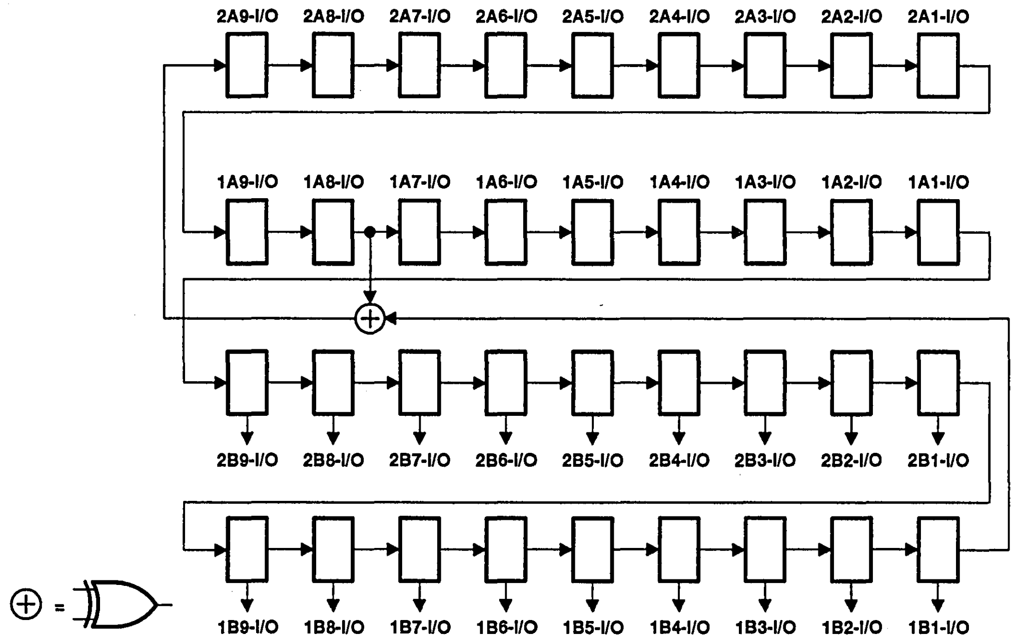


**Figure 5. 36-Bit PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

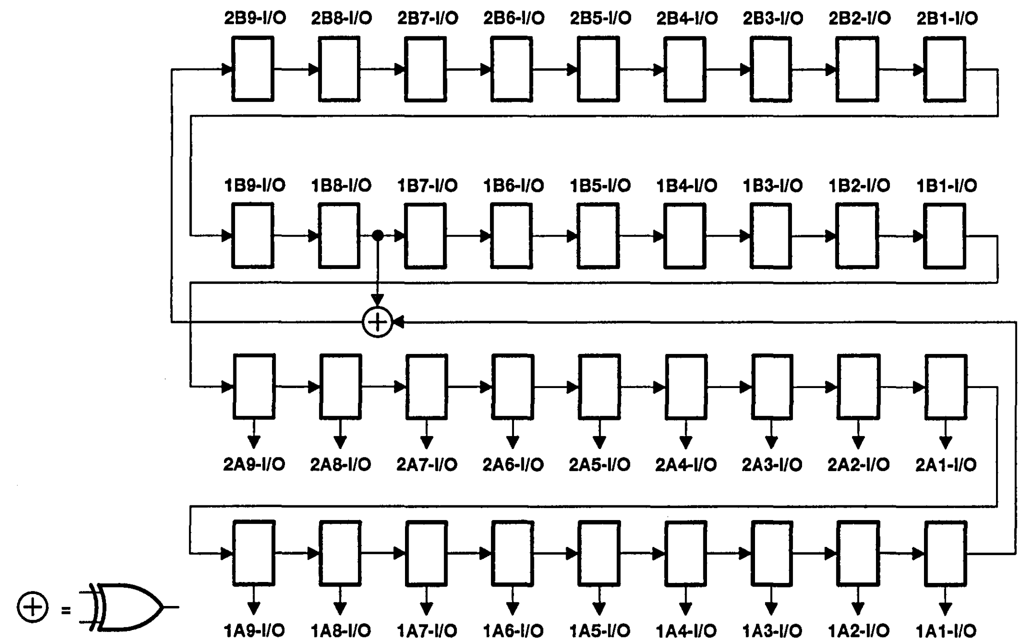


**Figure 6. 36-Bit PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

**parallel-signature analysis (PSA)**

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 show the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

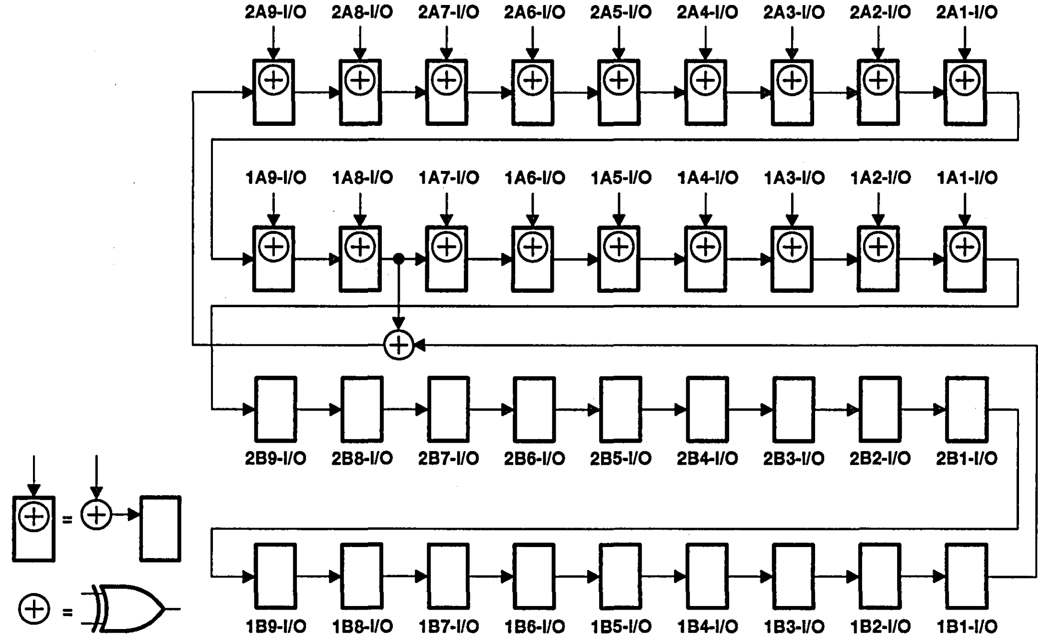


**Figure 7. 36-Bit PSA Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

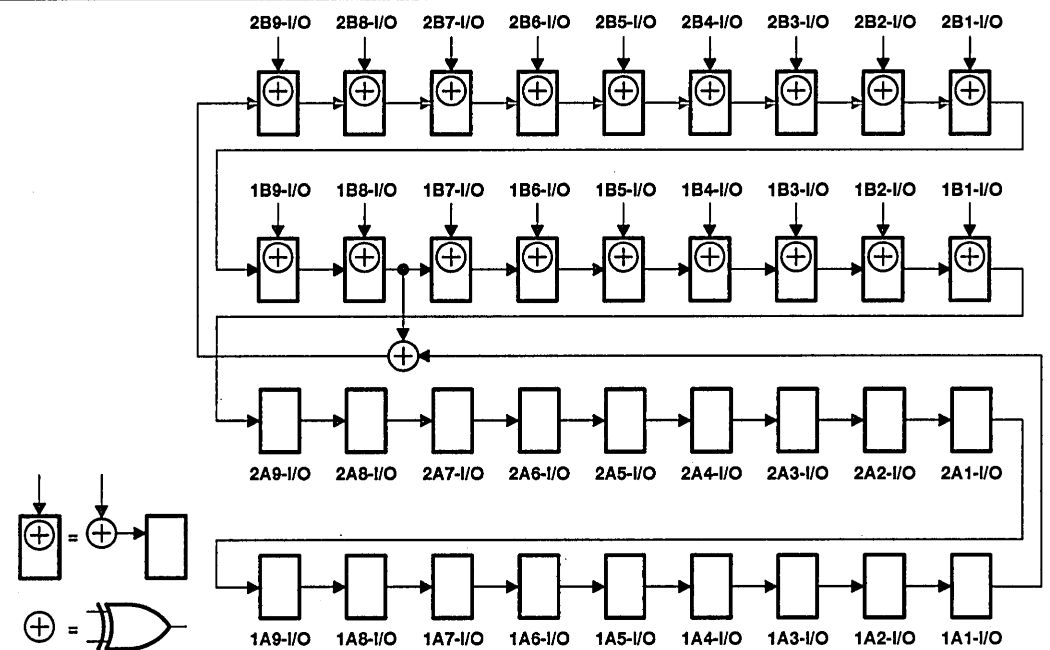


Figure 8. 36-Bit PSA Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 show the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

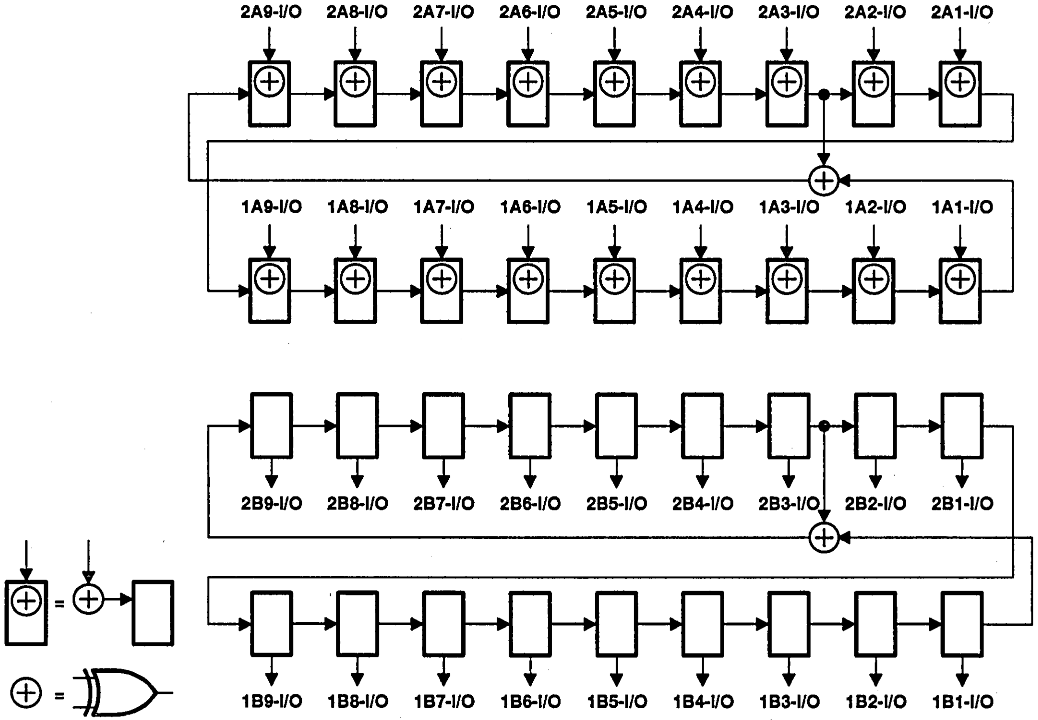


**Figure 9. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

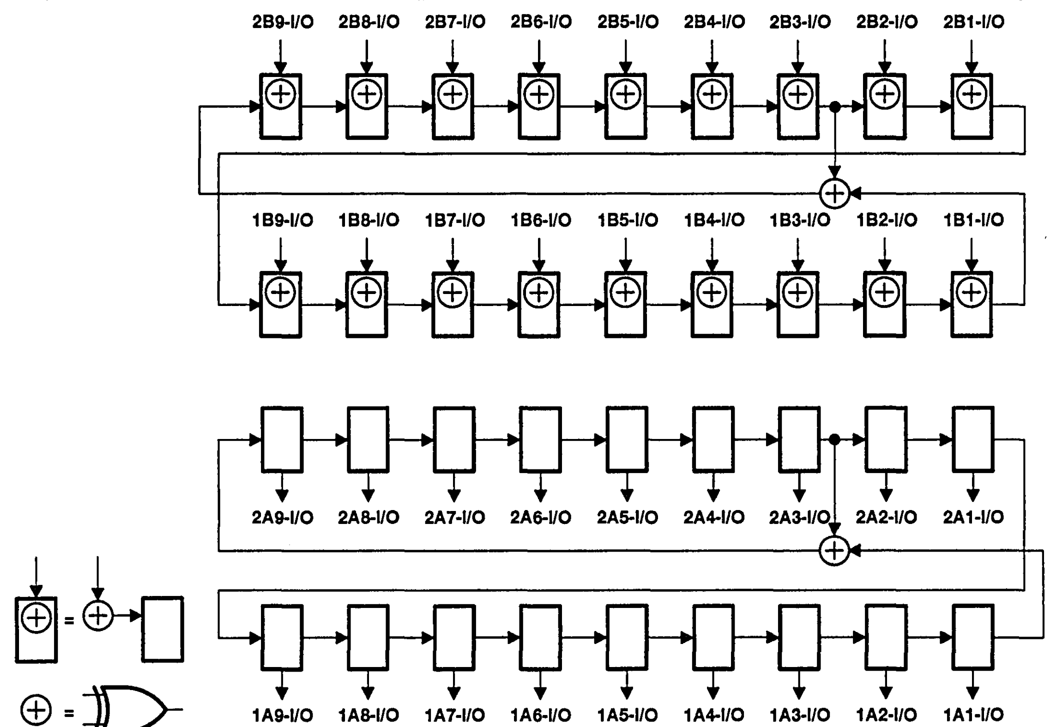


**Figure 10. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 show the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

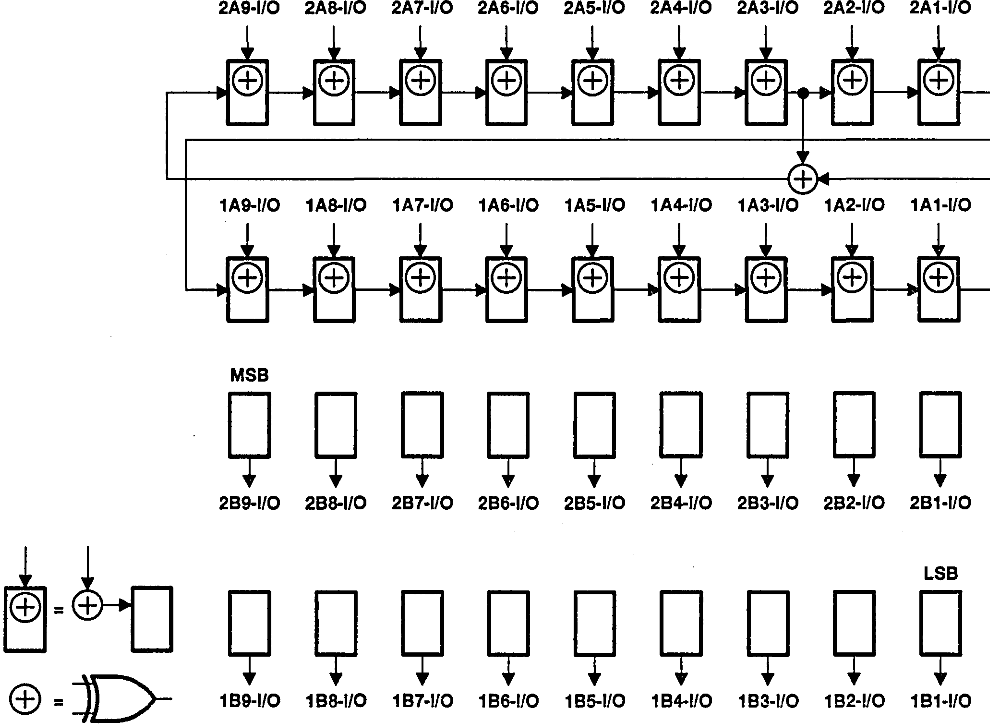


**Figure 11. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

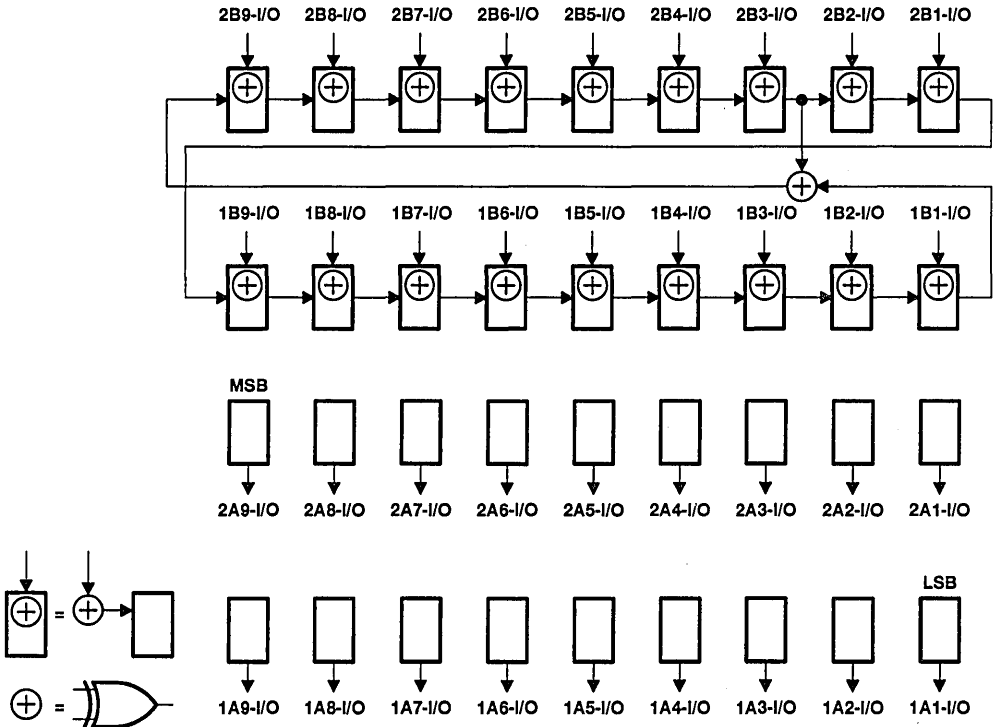


Figure 12. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

## timing description

All test operations of the 'ABT18640 are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | The selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

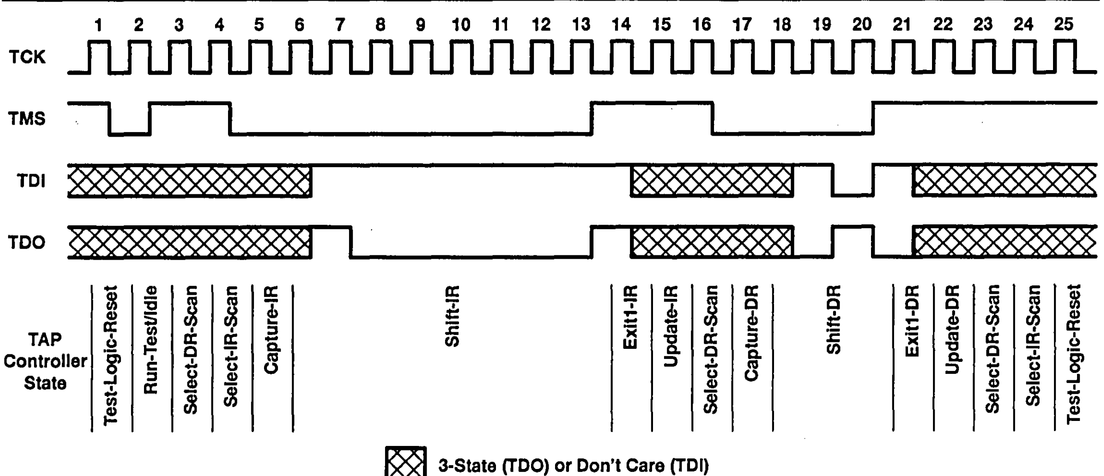


**Figure 13. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$ (except I/O ports) (see Note 1) | –0.5 V to 7 V |
| Input voltage range, $V_I$ (I/O ports) (see Note 1) | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$: SN54ABT18640 | 96 mA |
| SN74ABT18640 | 128 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | –18 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | –50 mA |
| Continuous current through $V_{CC}$ | 576 mA |
| Continuous current through GND | 1152 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DGG package | 1 W |
| DL package | 1.4 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions (see Note 3)

| | | SN54ABT18640 | | SN74ABT18640 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

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NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT18640 | | SN74ABT18640 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $I_I$ | DIR, $\overline{OE}$, TCK | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | | | | | ±100 | | ±100 | | ±100 | |
| $I_{IH}$ | TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | | 10 | µA |
| $I_{IL}$ | TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –150 | –40 | –150 | –40 | –150 | µA |
| $I_{OZH}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | | –50 | | –50 | µA |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 2 V, $V_O$ = 2.7 V or 0.5 V | | | | ±50 | | ±50 | | ±50 | µA |
| $I_{OZPD}$ | | $V_{CC}$ = 2 V to 0, $V_O$ = 2.7 V or 0.5 V | | | | ±50 | | ±50 | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \leq$ 4.5 V | | | ±100 | | ±450 | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –110 | –200 | –50 | –200 | –50 | –200 | mA |
| $I_{CC}$ | A or B ports | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 3.5 | 5 | | 5 | | 5 | mA |
| | | | Outputs low | | 33 | 38 | | 38 | | 38 | |
| | | | Outputs disabled | | 2.9 | 4.5 | | 4.5 | | 4.5 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 50 | | 50 | | 50 | µA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 3 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | | | | pF |

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* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

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## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| | | | SN54ABT18640 | | SN74ABT18640 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 8.1 | | 8.1 | | ns |
| $t_{su}$ | Setup time | A, B, DIR, or $\overline{OE}$ before TCK↑ | 9.5 | | 7 | | ns |
| | | TDI before TCK↑ | 4.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3.6 | | 3.6 | | |
| $t_h$ | Hold time | A, B, DIR, or $\overline{OE}$ after TCK↑ | 0.7 | | 0 | | ns |
| | | TDI after TCK↑ | 0 | | 0 | | |
| | | TMS after TCK↑ | 0.5 | | 0.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | µs |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT18640 | | SN74ABT18640 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1.5 | 2.8 | 4.1 | 1.5 | 5.1 | 1.5 | 4.8 | ns |
| $t_{PHL}$ | | | 1.5 | 3.1 | 4.6 | 1.5 | 5.8 | 1.5 | 5.4 | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | 2 | 4.7 | 5.8 | 2 | 8.1 | 2 | 7.5 | ns |
| $t_{PZL}$ | | | 2 | 4.5 | 6.2 | 2 | 8.5 | 2 | 8 | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | 2.5 | 5.8 | 6.8 | 2.5 | 9.5 | 2.5 | 8.5 | ns |
| $t_{PLZ}$ | | | 2.5 | 4.8 | 6 | 2.5 | 8.5 | 2.5 | 7.5 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT18640 | | SN74ABT18640 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK↓ | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3 | 7.1 | 10.1 | 3 | 14 | 3 | 13.1 | ns |
| $t_{PHL}$ | | | 3 | 7 | 10.1 | 2.8 | 13.8 | 3 | 12.8 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.4 | 5 | 2 | 6.4 | 2 | 6.1 | ns |
| $t_{PHL}$ | | | 2 | 3.9 | 5.6 | 2 | 7 | 2 | 6.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 7.5 | 10.6 | 4 | 14.1 | 4 | 13.4 | ns |
| $t_{PZL}$ | | | 4 | 7.6 | 10.5 | 4 | 14.3 | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.8 | 5.5 | 2 | 7 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2.5 | 4 | 5.7 | 2.3 | 7.3 | 2.5 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 3.5 | 7.7 | 10.8 | 2.9 | 14.4 | 3.5 | 13.6 | ns |
| $t_{PLZ}$ | | | 2.5 | 7.1 | 10.1 | 2.5 | 13.8 | 2.5 | 12.7 | |
| $t_{PHZ}$ | TCK↓ | TDO | 2 | 3.9 | 5.7 | 2 | 7.5 | 2 | 7.2 | ns |
| $t_{PLZ}$ | | | 1.5 | 3.5 | 5.4 | 1.5 | 6.7 | 1.5 | 6.3 | |

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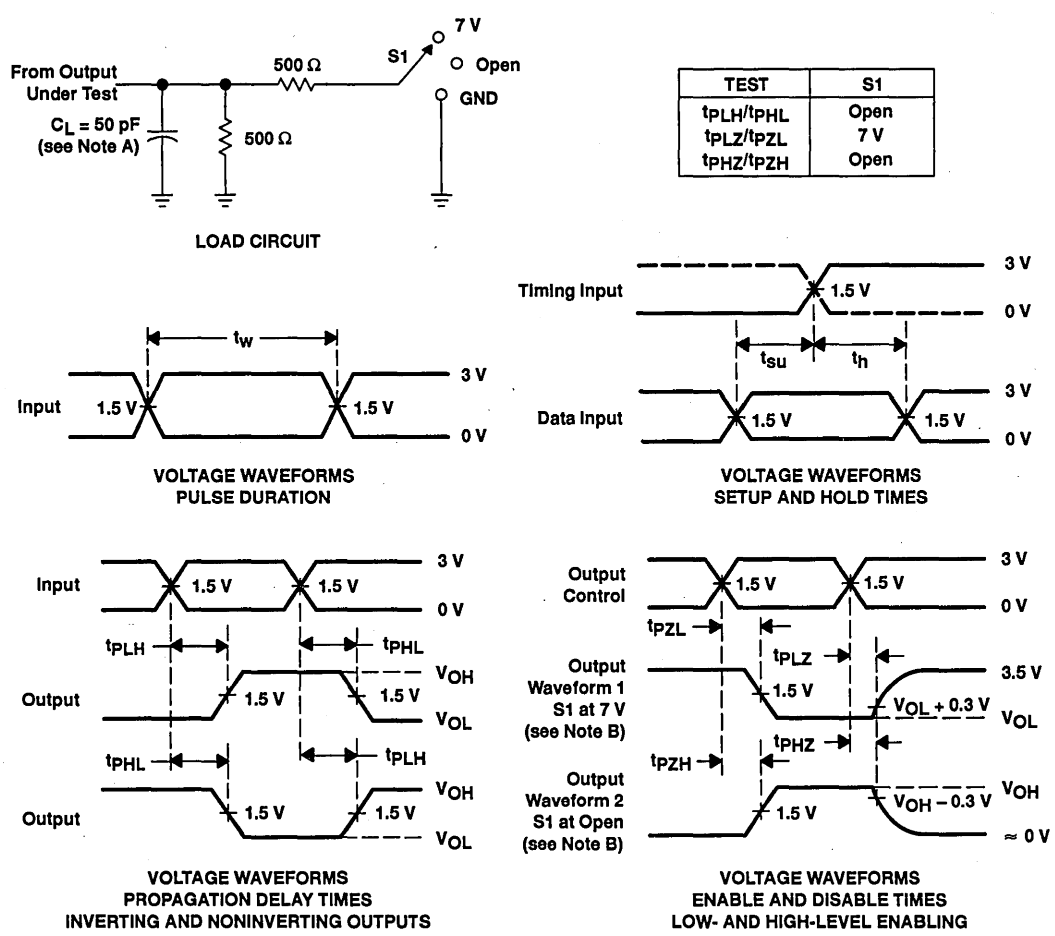
## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

General Information 1

SN54/74BCT Octals 2

SN54/74ABT Octals 3

SN54/74ABT Widebus™ With Dual-Sided Terminals 4

SN54/74ABT Widebus™ With Quad-Sided Terminals 5

SN54/74LVT Widebus™ With Dual-Sided Terminals 6

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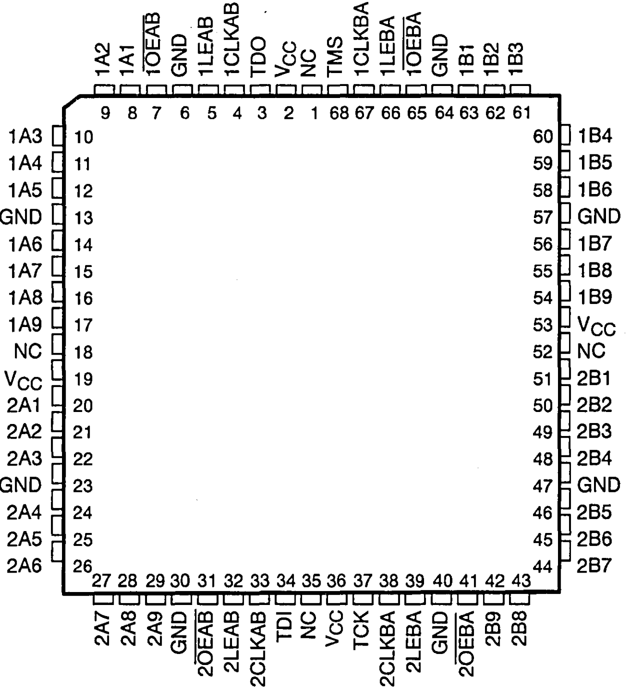
- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- B-Port Outputs of 'ABTH182502A Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC*-IIB™ BiCMOS Design
- One Boundary-Scan Cell Per I/O Architecture Improves Scan Efficiency
- *SCOPE* Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54ABTH18502A, SN54ABTH182502A . . . HV PACKAGE
(TOP VIEW)




NC – No internal connection

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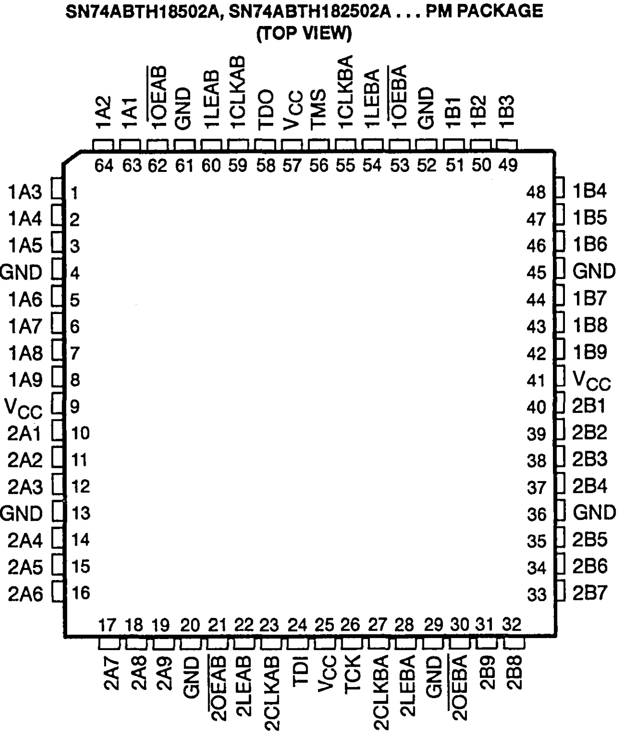
SN74ABTH18502A, SN74ABTH182502A . . . PM PACKAGE
(TOP VIEW)




## description

The 'ABTH18502A and 'ABTH182502A scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE universal bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

## description (continued)

Four dedicated test pins observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Improved scan efficiency is accomplished through the adoption of a one boundary-scan cell (BSC) per I/O pin architecture. This architecture is implemented in such a way as to capture the most pertinent test data. A PSA/COUNT instruction also is included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The B-port outputs of 'ABTH182502A, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54ABTH18502A and SN54ABTH182502A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH18502A and SN74ABTH182502A are characterized for operation from –40°C to 85°C.

**FUNCTION TABLE†**
**(normal mode, each register)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OEAB}$ | LEAB | CLKAB | A | B |
| L | L | L | X | $B_0$‡ |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | H | X | L | L |
| L | H | X | H | H |
| H | X | X | X | Z |

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established

## functional block diagram

Boundary-Scan Register

1LEAB 60
1CLKAB 59
$V_{CC}$
$1\overline{OEAB}$ 62
1LEBA 54
1CLKBA 55
$V_{CC}$
$1\overline{OEBA}$ 53
1A1 63
C1 1D
C1 1D
C1 1D
C1 1D
51 1B1
One of Nine Channels

2LEAB 22
2CLKAB 23
$V_{CC}$
$2\overline{OEAB}$ 21
2LEBA 28
2CLKBA 27
$V_{CC}$
$2\overline{OEBA}$ 30
2A1 10
C1 1D
C1 1D
C1 1D
C1 1D
40 2B1
One of Nine Channels

Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller
$V_{CC}$
TDI 24
$V_{CC}$
TMS 56
TCK 26
58 TDO

Pin numbers shown are for the PM package.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| GND | Ground |
| 1LEAB, 1LEBA, 2LEAB, 2LEBA | Normal-function latch enables. See function table for normal-mode logic. |
| 1$\overline{OEAB}$, 1$\overline{OEBA}$, 2$\overline{OEAB}$, 2$\overline{OEBA}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and four test-data registers: a 48-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

Test-Logic-Reset
TMS = H
TMS = L
Run-Test/Idle
TMS = L
TMS = H
Select-DR-Scan
TMS = H
Select-IR-Scan
TMS = H
TMS = L
Capture-DR
TMS = H
TMS = H
TMS = L
Capture-IR
TMS = L
Shift-DR
TMS = L
TMS = L
Shift-IR
TMS = L
TMS = H
Exit1-DR
TMS = H
TMS = H
Exit1-IR
TMS = H
TMS = L
Pause-DR
TMS = L
TMS = L
Pause-IR
TMS = L
TMS = H
Exit2-DR
TMS = L
TMS = H
TMS = L
Exit2-IR
TMS = H
Update-DR
TMS = H
Update-IR
TMS = H
TMS = L
TMS = H
TMS = L

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. TMS has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABTH18502A and 'ABTH182502A, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–44 in the boundary-scan register are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

### Shift-DR (continued)

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state can suspend and resume data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'ABTH18502A and 'ABTH182502A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state can suspend and resume instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABTH18502A and 'ABTH182502A. The even-parity feature specified for SCOPE devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

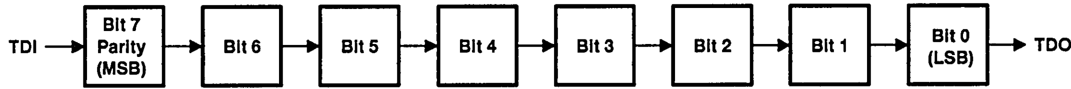



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used to store test data that is to be applied externally to the device output pins, and/or to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | 2$\overline{OEAB}$ | 35 | 2A9-I/O | 17 | 2B9-I/O |
| 46 | 1$\overline{OEAB}$ | 34 | 2A8-I/O | 16 | 2B8-I/O |
| 45 | 2$\overline{OEBA}$ | 33 | 2A7-I/O | 15 | 2B7-I/O |
| 44 | 1$\overline{OEBA}$ | 32 | 2A6-I/O | 14 | 2B6-I/O |
| 43 | 2CLKAB | 31 | 2A5-I/O | 13 | 2B5-I/O |
| 42 | 1CLKAB | 30 | 2A4-I/O | 12 | 2B4-I/O |
| 41 | 2CLKBA | 29 | 2A3-I/O | 11 | 2B3-I/O |
| 40 | 1CLKBA | 28 | 2A2-I/O | 10 | 2B2-I/O |
| 39 | 2LEAB | 27 | 2A1-I/O | 9 | 2B1-I/O |
| 38 | 1LEAB | 26 | 1A9-I/O | 8 | 1B9-I/O |
| 37 | 2LEBA | 25 | 1A8-I/O | 7 | 1B8-I/O |
| 36 | 1LEBA | 24 | 1A7-I/O | 6 | 1B7-I/O |
| — | — | 23 | 1A6-I/O | 5 | 1B6-I/O |
| — | — | 22 | 1A5-I/O | 4 | 1B5-I/O |
| — | — | 21 | 1A4-I/O | 3 | 1B4-I/O |
| — | — | 20 | 1A3-I/O | 2 | 1B3-I/O |
| — | — | 19 | 1A2-I/O | 1 | 1B2-I/O |
| — | — | 18 | 1A1-I/O | 0 | 1B1-I/O |

### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run test (RUNT) instruction to implement additional test operations not included in the basic SCOPE instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

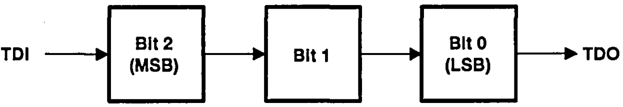



**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

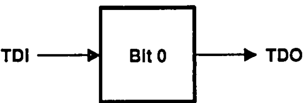



**Figure 4. Bypass Register Order of Scan**

### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'ABTH18502A , the binary value 00000000000000100111000000101111 (0002702F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74ABTH18502A.

For the 'ABTH182502A , the binary value 00000000000000101011000000101111 (0002B02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74ABTH182502A.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary-run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE instruction that is not supported in the 'ABTH18502A or 'ABTH182502A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output-enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–44 of the BSR). When a given output enable is active (logic 0), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a RUNT operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 47–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 47–44 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when both bytes of the device are operating in one direction of data flow (that is, $1\overline{OEAB} \neq 1\overline{OEBA}$ and $2\overline{OEAB} \neq 2\overline{OEBA}$) and in the same direction of data flow (that is, $1\overline{OEAB} = 2\overline{OEAB}$ and $1\overline{OEBA} = 2\overline{OEBA}$). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 illustrate the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

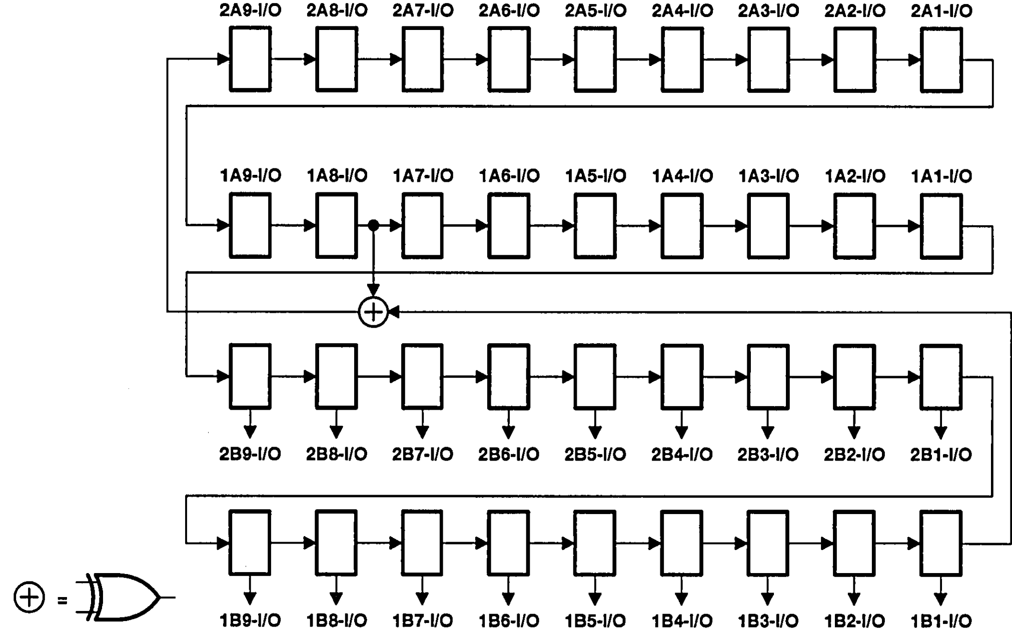



**Figure 5. 36-Bit PRPG Configuration (1$\overline{\text{OEAB}}$ = 2$\overline{\text{OEAB}}$ = 0, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 1)**

**pseudo-random pattern generation (PRPG) (continued)**

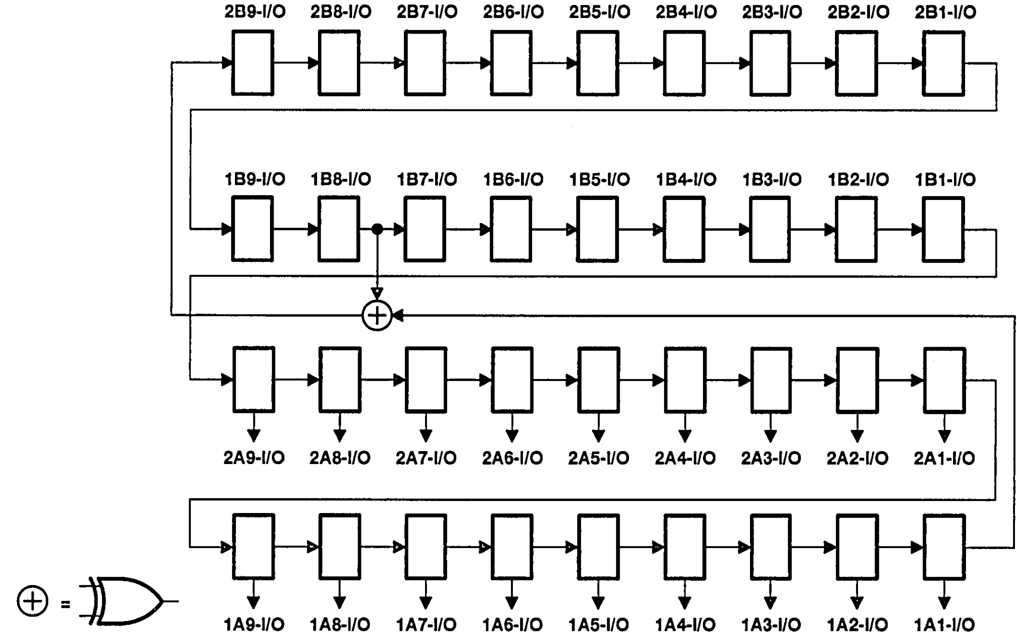



**Figure 6. 36-Bit PRPG Configuration ($1\overline{OEAB} = 2\overline{OEAB} = 1$, $1\overline{OEBA} = 2\overline{OEBA} = 0$)**

### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 illustrate the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

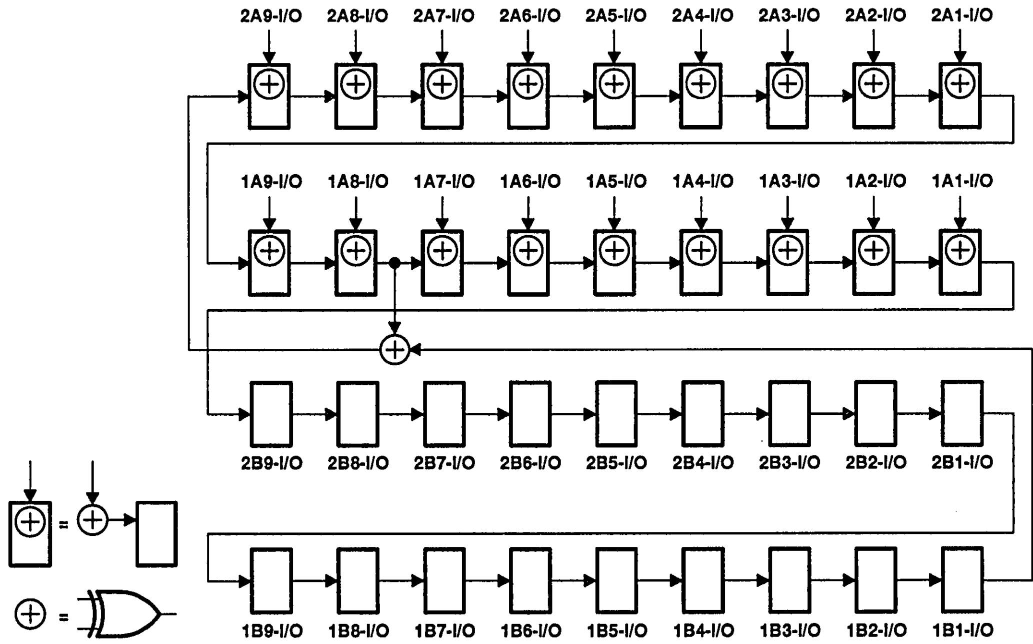



**Figure 7. 36-Bit PSA Configuration ($1\overline{OEAB}$ = $2\overline{OEAB}$ = 0, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 1)**

**parallel-signature analysis (PSA) (continued)**

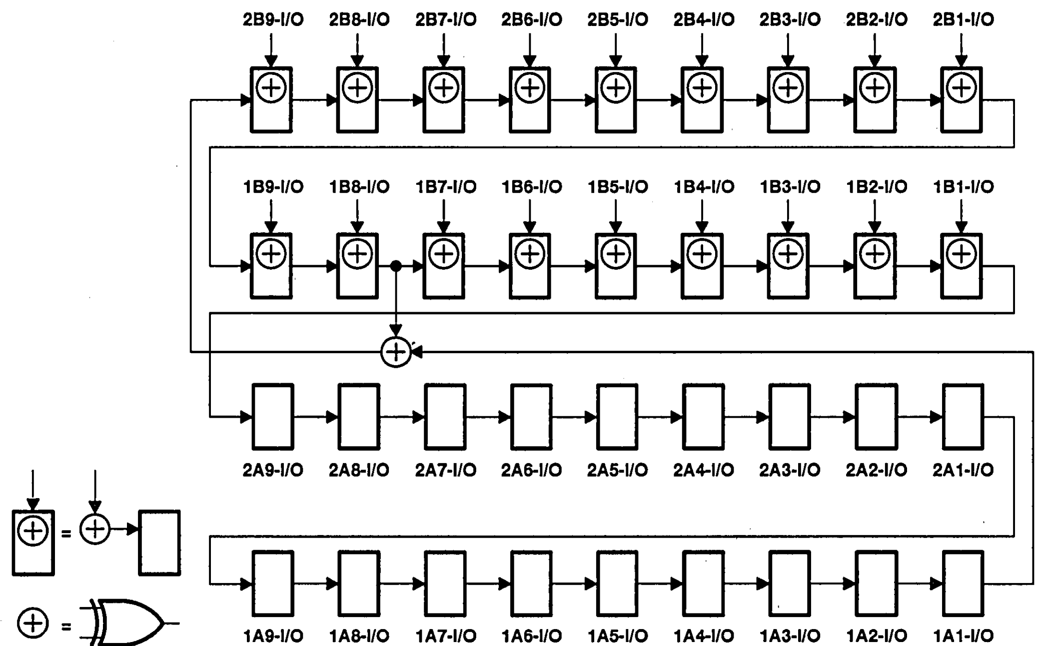



**Figure 8. 36-Bit PSA Configuration ($1\overline{OEAB} = 2\overline{OEAB} = 1$, $1\overline{OEBA} = 2\overline{OEBA} = 0$)**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

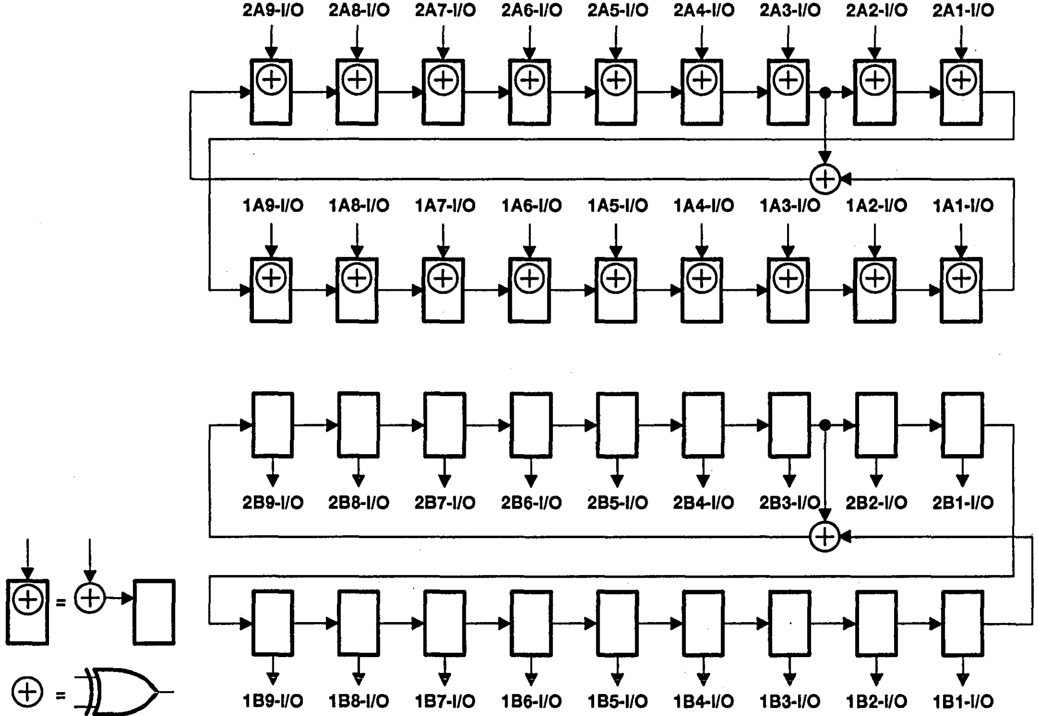



**Figure 9. 18-Bit PSA/PRPG Configuration ($1\overline{OEAB}$ = $2\overline{OEAB}$ = 0, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 1)**

**simultaneous PSA and PRPG (PSA/PRPG) (continued)**

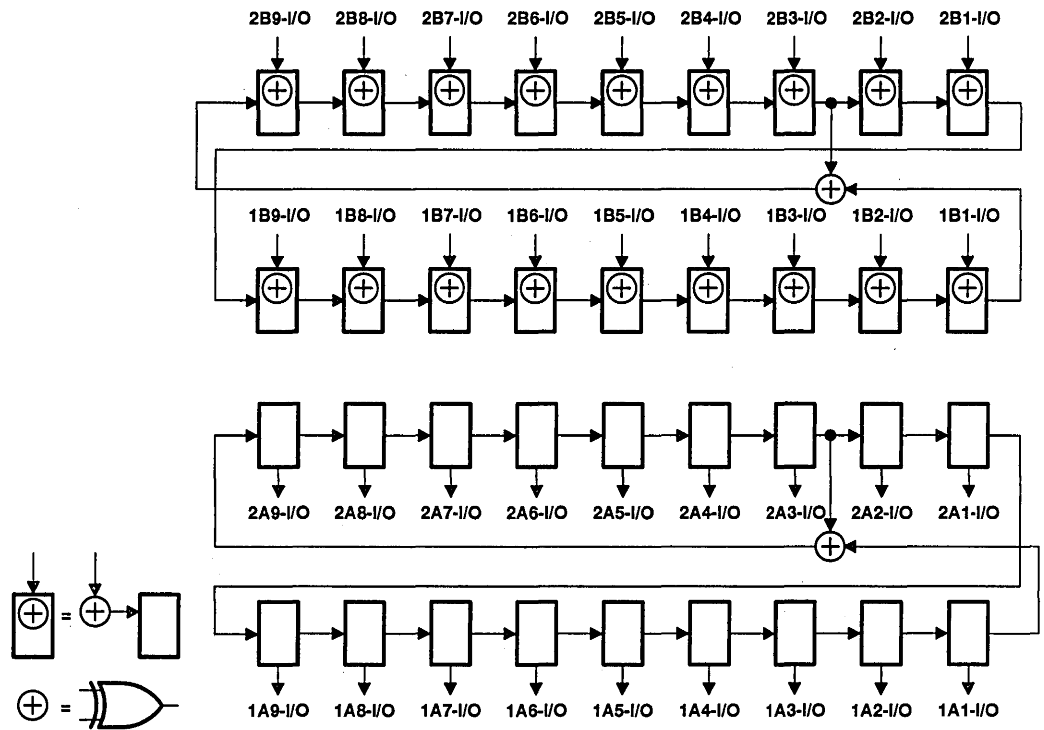



**Figure 10. 18-Bit PSA/PRPG Configuration (1$\overline{\text{OEAB}}$ = 2$\overline{\text{OEAB}}$ = 1, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

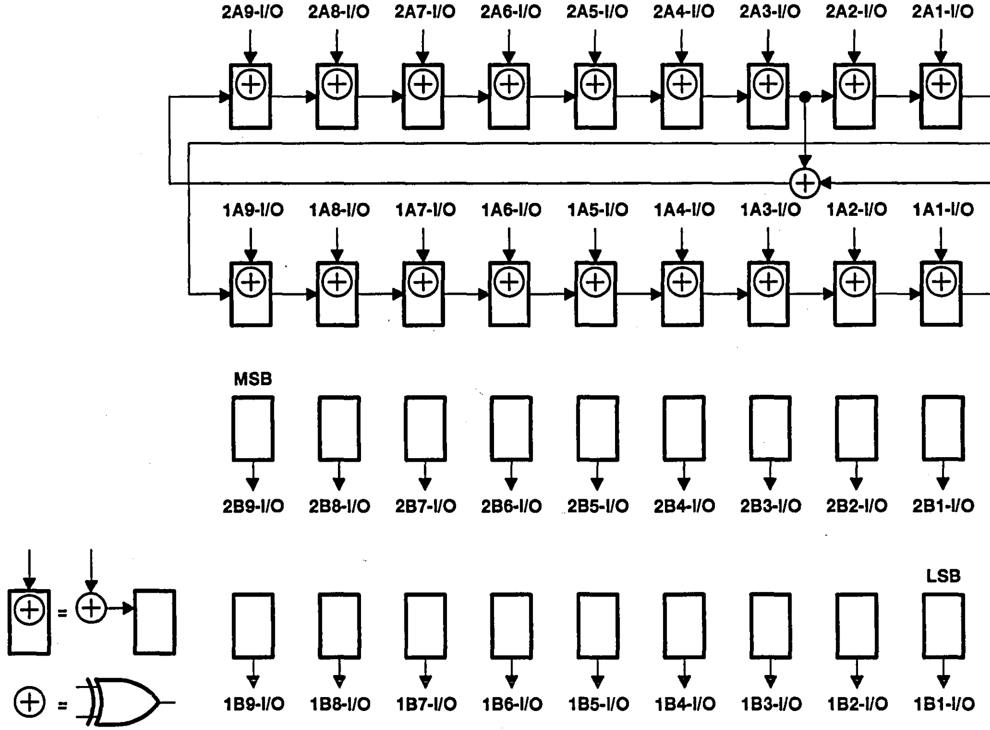



**Figure 11. 18-Bit PSA/COUNT Configuration ($1\overline{OEAB} = 2\overline{OEAB} = 0$, $1\overline{OEBA} = 2\overline{OEBA} = 1$)**

**simultaneous PSA and binary count up (PSA/COUNT) (continued)**

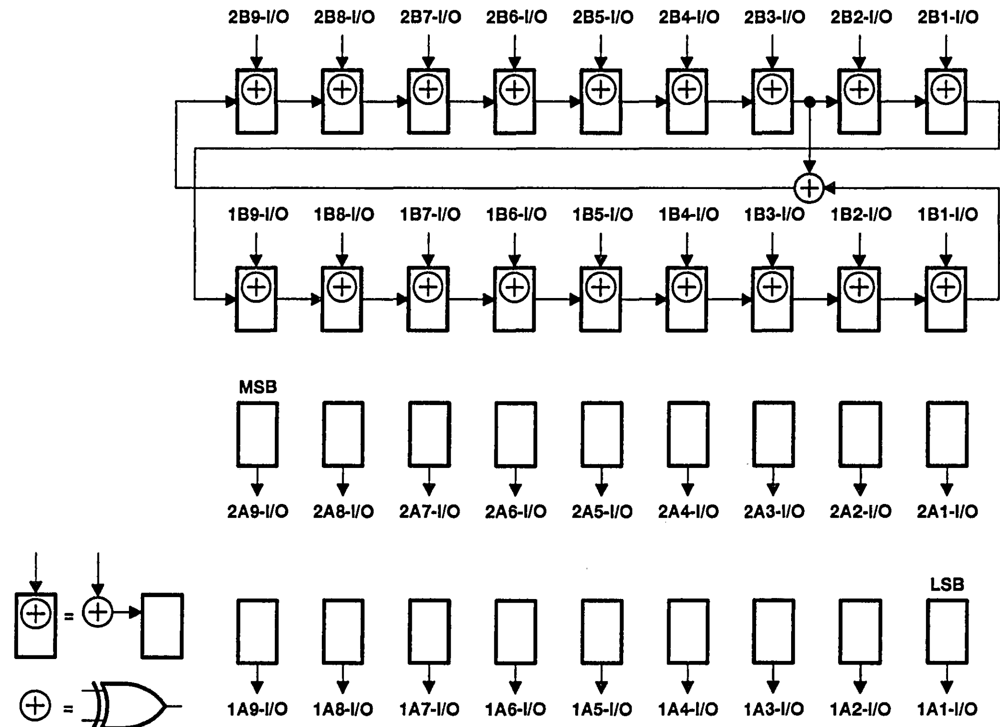



**Figure 12. 18-Bit PSA/COUNT Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)**

## timing description

All test operations of the 'ABTH18502A and 'ABTH182502A are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

## timing description (continued)

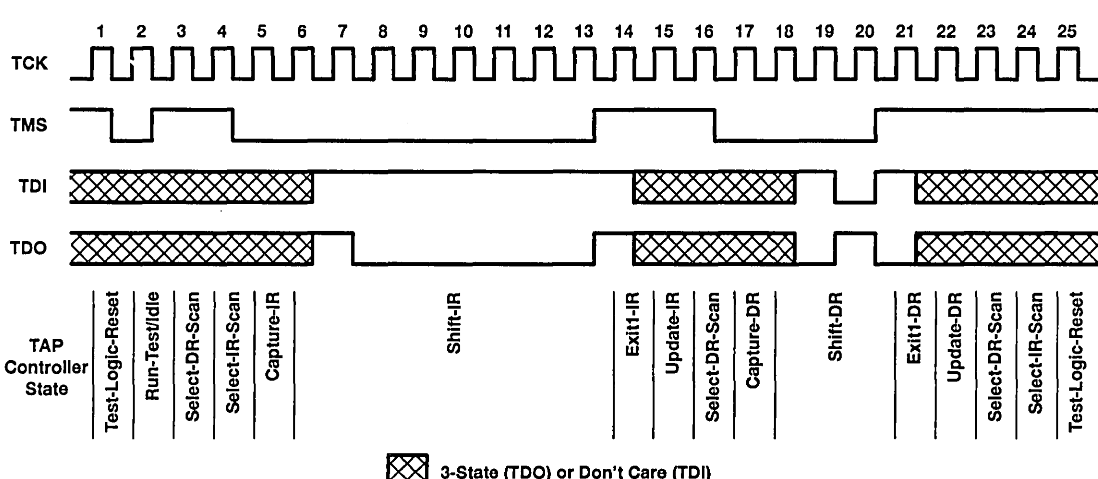



**Figure 13. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$: except I/O ports (see Note 1) | –0.5 V to 7 V |
| I/O ports (see Note 1) | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$: SN54ABTH18502A | 96 mA |
| SN54ABTH182502A (A port or TDO) | 96 mA |
| SN54ABTH182502A (B port) | 30 mA |
| SN74ABTH18502A | 128 mA |
| SN74ABTH182502A (A port or TDO) | 128 mA |
| SN74ABTH182502A (B port) | 30 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | –18 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | –50 mA |
| Continuous current through $V_{CC}$ | 576 mA |
| Continuous current through GND | 1152 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): PM package | 1 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | SN54ABTH18502A | | SN74ABTH18502A | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ABTH18502A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | $T_A$ = –55°C to 125°C | | |
| | | | | MIN | TYP† | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –24 mA | 2 | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | V |
| $I_I$ | CLK, LE, TCK $V_{CC}$ = 0 to 5.5 V, | $V_{CC}$ = 0 to 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±20 | | ±20 | |
| $I_{IH}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | µA |
| $I_{IL}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –150 | –40 | –150 | µA |
| $I_{I(hold)}$‡ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 75 | 220 | 500 | 75 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | –180 | –500 | –75 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 2.7 V, $\overline{OE}$ = 2 V | | | | 10 | | 10 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 0.5 V, $\overline{OE}$ = 2 V | | | | –10 | | –10 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \leq$ 4.5 V | | | ±100 | | | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –110 | –200 | –50 | –200 | mA |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | | 1.6 | 5.5 | | 5.5 | mA |
| | Outputs low | | | | 19 | 24 | | 24 | |
| | Outputs disabled | | | | 0.9 | 3.6 | | 3.6 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | | 7 | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | | 10 | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | | | 7 | | | pF |

† All typical values are at $V_{CC}$ = 5 V.
‡ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN74ABTH18502A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | |
| | | | | MIN | TYP† | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | | | |
| | | | $I_{OH}$ = –32 mA | 2 | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55 | | 0.55 | |
| $I_I$ | CLK, LE, TCK | $V_{CC}$ = 0 to 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±20 | | ±20 | |
| $I_{IH}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | µA |
| $I_{IL}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –150 | –40 | –150 | µA |
| $I_{I(hold)}$‡ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 75 | 220 | 500 | 75 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | –180 | –500 | –75 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 2.7 V, $\overline{OE}$ = 2 V | | | | 10 | | 10 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 0.5 V, $\overline{OE}$ = 2 V | | | | –10 | | –10 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±100 | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –110 | –200 | –50 | –200 | mA |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | | 1.6 | 2.2 | | 2.2 | mA |
| | Outputs low | | | | 19 | 24 | | 24 | |
| | Outputs disabled | | | | 0.9 | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 5 | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 10 | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | | pF |

† All typical values are at $V_{CC}$ = 5 V.
‡ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

| | | | | SN54ABTH18502A | | SN74ABTH18502A | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | 3.8 | | 3.5 | | ns |
| | | LEAB or LEBA high | | 3.5 | | 3.5 | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | 3.5 | | 3.5 | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | 4.0 | | 3.5 | | |
| | | | CLK low | 2 | | 2 | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | 2.9 | | 0.5 | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | 4.0 | | 3 | | |

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| | | | SN54ABTH18502A | | SN74ABTH18502A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 8 | | 8 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, LE, or $\overline{OE}$ before TCK↑ | 6 | | 6 | | ns |
| | | TDI before TCK↑ | 4.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3 | | 3 | | |
| $t_h$ | Hold time | A, B, CLK, LE, or $\overline{OE}$ after TCK↑ | 2.9 | | 1.5 | | ns |
| | | TDI after TCK↑ | 1 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50* | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1* | | 1 | | µs |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABTH18502A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –55°C to 125°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | 1.5 | 3.1 | 5 | 1.5 | 6 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 5 | 1.5 | 6 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 1.5 | 3.7 | 5.2 | 1.5 | 6.4 | ns |
| $t_{PHL}$ | | | 1.5 | 3.8 | 5.2 | 1.5 | 6.4 | |
| $t_{PLH}$ | LEAB or LEBA | B or A | 1.5 | 3.9 | 5.5 | 1.5 | 6.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 5.5 | 1.5 | 6.5 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 1.5 | 4 | 5.8 | 1.5 | 7.5 | ns |
| $t_{PZL}$ | | | 1.5 | 4.2 | 5.8 | 1.5 | 7.5 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2.8 | 5.9 | 7.2 | 2.8 | 8.9 | ns |
| $t_{PLZ}$ | | | 2 | 4.5 | 6 | 2 | 7.5 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABTH18502A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | 1.5 | 3.1 | 5 | 1.5 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 5 | 1.5 | 5.5 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 1.5 | 3.7 | 5 | 1.5 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.8 | 5 | 1.5 | 5.5 | |
| $t_{PLH}$ | LEAB or LEBA | B or A | 1.5 | 3.9 | 5.5 | 1.5 | 6 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 5.5 | 1.5 | 6 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 1.5 | 4 | 5.8 | 1.5 | 7 | ns |
| $t_{PZL}$ | | | 1.5 | 4.2 | 5.8 | 1.5 | 7 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 3 | 5.9 | 7 | 3 | 8 | ns |
| $t_{PLZ}$ | | | 2 | 4.5 | 6 | 2 | 7 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH18502A | | SN74ABTH18502A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 7.4 | 11 | 2.5 | 14.5 | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | 2.5 | 7.6 | 10.8 | 2.5 | 14 | 2.5 | 12.4 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.8 | 5.1 | 2 | 7 | 2 | 5.6 | ns |
| $t_{PHL}$ | | | 2 | 4 | 5.1 | 2 | 7 | 2 | 5.6 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 8 | 11.5 | 4 | 14.5 | 4 | 13.4 | ns |
| $t_{PZL}$ | | | 4 | 8 | 11.8 | 4 | 15 | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.9 | 5.7 | 2 | 7.5 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2 | 4.2 | 6.2 | 2 | 8 | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 10.8 | 13 | 4 | 18 | 4 | 15 | ns |
| $t_{PLZ}$ | | | 3 | 9.1 | 13.3 | 3 | 17.5 | 3 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.3 | 6.8 | 3 | 8 | 3 | 7.2 | ns |
| $t_{PLZ}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 8 | 2.5 | 6.3 | |

## recommended operating conditions

| | | | SN54ABTH182502A | | SN74ABTH182502A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| | | B port | | 12 | | 12 | |
| Δt/Δv | Input transition rise or fall rate | | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABTH182502A | | SN74ABTH182502A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, $I_I$ = –18 mA | | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | A port, TDO | $V_{CC}$ = 4.5 V, $I_{OH}$ = –3 mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, $I_{OH}$ = –3 mA | | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| | B port | $V_{CC}$ = 4.5 V, $I_{OH}$ = –1 mA | | 3.35 | | | 3.3 | | 3.35 | | |
| | | $V_{CC}$ = 5 V, $I_{OH}$ = –1 mA | | 3.85 | | | 3.8 | | 3.85 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | 3.1 | | | 3 | | 3.1 | | |
| | | | $I_{OH}$ = –12 mA | 2.6* | | | | | 2.6 | | |
| $V_{OL}$ | A port, TDO | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| | B port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 8 mA | | | 0.8 | | 0.8 | | 0.65 | |
| | | | $I_{OL}$ = 12 mA | | | 0.8* | | | | 0.8 | |
| $I_I$ | CLK, LE, TCK | $V_{CC}$ = 0 to 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±20 | | ±20 | | ±20 | |
| $I_{IH}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ | | | | 10 | | 10 | | 10 | µA |
| $I_{IL}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, $V_I$ = GND | | –40 | | –150 | –40 | –150 | –40 | –150 | µA |
| $I_{I(hold)}$‡ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 75 | 220 | 500 | | | 75 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | –180 | –500 | | | –75 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 2.7 V, $\overline{OE}$ = 2 V | | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 0.5 V, $\overline{OE}$ = 2 V | | | | –10 | | –10 | | –10 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, $V_I$ or $V_O$ ≤ 4.5 V | | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, $V_O$ = 5.5 V | | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | A port, TDO | $V_{CC}$ = 5.5 V, $V_O$ = 2.5 V | | –50 | –110 | –200 | –50 | –200 | –50 | –200 | mA |
| | B port | $V_{CC}$ = 5.5 V, $V_O$ = 2.5 V | | –25 | –55 | –100 | –25 | –100 | –25 | –100 | |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | | 1.6 | 2.2 | | 2.2 | | 2.2 | mA |
| | Outputs low | | | | 21 | 27 | | 27 | | 27 | |
| | Outputs disabled | | | | 0.9 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS | $T_A$ = 25°C | | | SN54ABTH182502A | | SN74ABTH182502A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | 5 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | 8 | | | | | | pF |

† All typical values are at $V_{CC}$ = 5 V.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

| | | | | SN54ABTH182502A | | SN74ABTH182502A | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | 3.5 | | 3.5 | | ns |
| | | LEAB or LEBA high | | 3.5 | | 3.5 | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | 3.5 | | 3.5 | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | 3.5 | | 3.5 | | |
| | | | CLK low | 2 | | 2 | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | 0.5 | | 0.5 | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | 3 | | 3 | | |

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| | | | SN54ABTH182502A | | SN74ABTH182502A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 8 | | 8 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, LE, or $\overline{OE}$ before TCK↑ | 6 | | 6 | | ns |
| | | TDI before TCK↑ | 4.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3 | | 3 | | |
| $t_h$ | Hold time | A, B, CLK, LE, or $\overline{OE}$ after TCK↑ | 1.5 | | 1.5 | | ns |
| | | TDI after TCK↑ | 1 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | µs |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

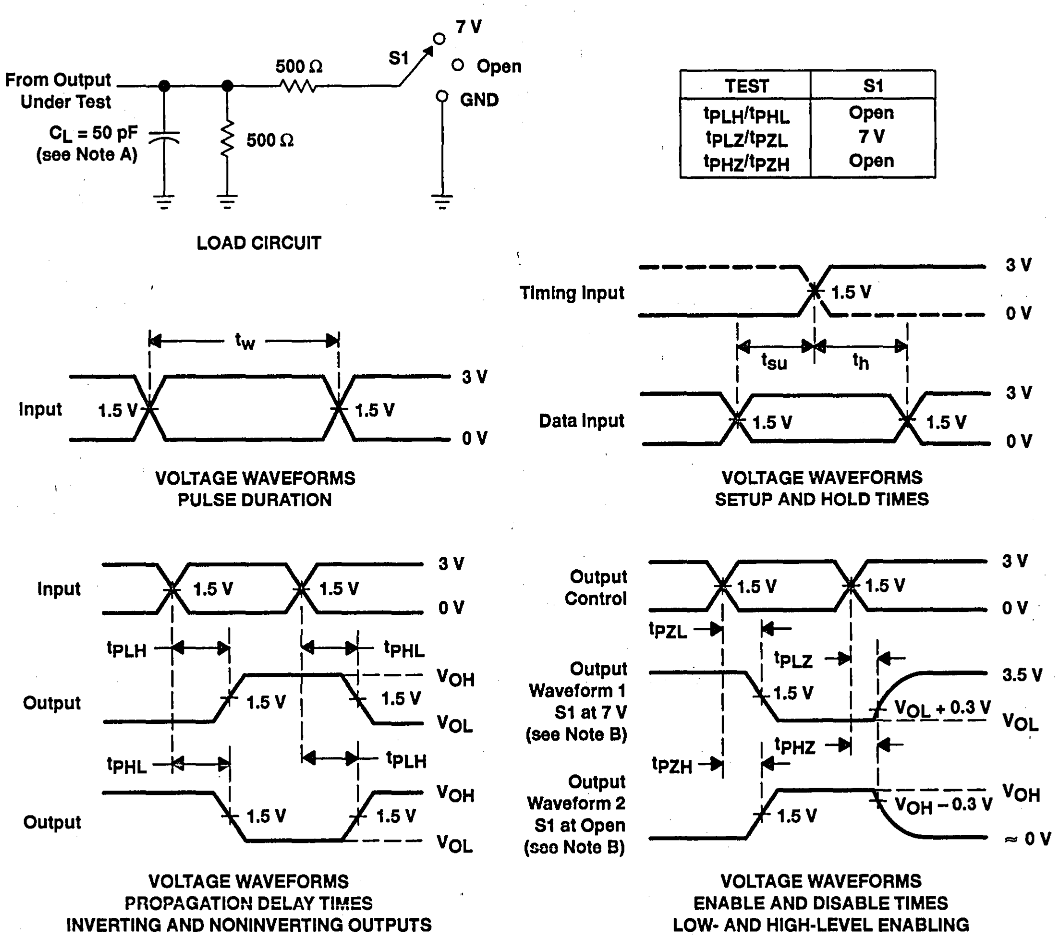
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH182502A | | SN74ABTH182502A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | 100 | | MHz |
| $t_{PLH}$ | A | B | 1.5 | 3.1 | 5 | 1.5 | 6 | 1.5 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 5.6 | 1.5 | 6.4 | 1.5 | 6.2 | |
| $t_{PLH}$ | B | A | 1.5 | 3.1 | 5 | 1.5 | 6 | 1.5 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 5 | 1.5 | 6 | 1.5 | 5.5 | |
| $t_{PLH}$ | CLKAB | B | 1.5 | 3.7 | 5.4 | 1.5 | 6.2 | 1.5 | 6.1 | ns |
| $t_{PHL}$ | | | 1.5 | 4 | 5.8 | 1.5 | 6.4 | 1.5 | 6.2 | |
| $t_{PLH}$ | CLKBA | A | 1.5 | 3.7 | 5 | 1.5 | 6 | 1.5 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.8 | 5 | 1.5 | 6 | 1.5 | 5.5 | |
| $t_{PLH}$ | LEAB | B | 1.5 | 3.9 | 5.6 | 1.5 | 6.5 | 1.5 | 6.3 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 5.6 | 1.5 | 6.5 | 1.5 | 6.2 | |
| $t_{PLH}$ | LEBA | A | 1.5 | 3.9 | 5.5 | 1.5 | 6.5 | 1.5 | 6 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 5.5 | 1.5 | 6.5 | 1.5 | 6 | |
| $t_{PZH}$ | OEAB or OEBA | B or A | 1.5 | 4 | 5.8 | 1.5 | 7.5 | 1.5 | 7 | ns |
| $t_{PZL}$ | | | 1.5 | 4.2 | 5.8 | 1.5 | 7.5 | 1.5 | 7 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 3 | 5.9 | 7 | 3 | 8.5 | 3 | 8 | ns |
| $t_{PLZ}$ | | | 2 | 4.5 | 6 | 2 | 7.5 | 2 | 7 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH182502A | | SN74ABTH182502A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 7.4 | 11 | 2.5 | 14.5 | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | 2.5 | 7.6 | 10.8 | 2.5 | 14 | 2.5 | 12.4 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.8 | 5.1 | 2 | 7 | 2 | 5.6 | ns |
| $t_{PHL}$ | | | 2 | 4 | 5.1 | 2 | 7 | 2 | 5.6 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 8 | 11.5 | 4 | 14.5 | 4 | 13.4 | ns |
| $t_{PZL}$ | | | 4 | 8 | 11.8 | 4 | 15 | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.9 | 5.7 | 2 | 7.5 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2 | 4.2 | 6.2 | 2 | 8 | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 10.8 | 13 | 4 | 18 | 4 | 15 | ns |
| $t_{PLZ}$ | | | 3 | 9.1 | 13.3 | 3 | 17.5 | 3 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.3 | 6.8 | 3 | 8 | 3 | 7.2 | ns |
| $t_{PLZ}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 8 | 2.5 | 6.3 | |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## PARAMETER MEASUREMENT INFORMATION



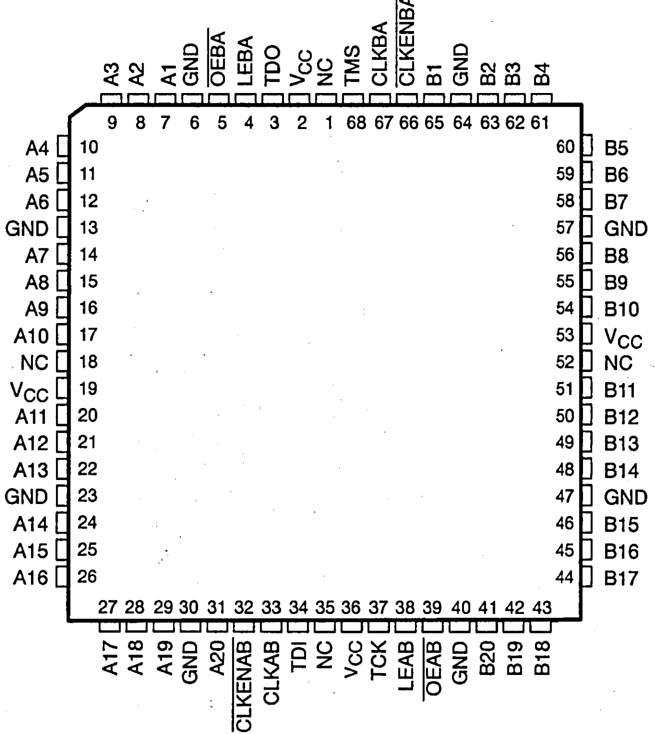

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors**
- **B-Port Outputs of 'ABTH182504A Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design**
- **One Boundary-Scan Cell Per I/O Architecture Improves Scan Efficiency**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ**
  - **Parallel-Signature Analysis at Inputs**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**
- **Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings**

**SN54ABTH18504A, SN54ABTH182504A . . . HV PACKAGE**
**(TOP VIEW)**




NC – No internal connection

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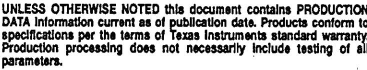
UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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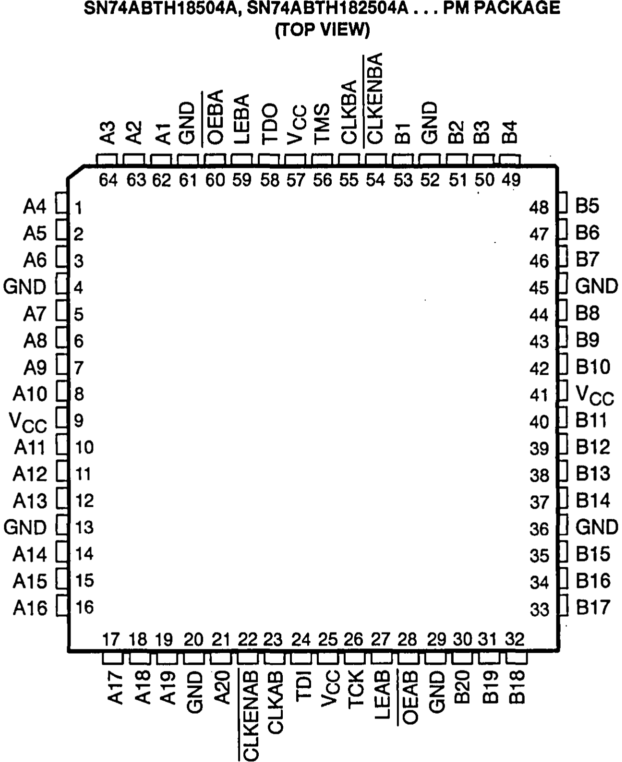
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN74ABTH18504A, SN74ABTH182504A . . . PM PACKAGE
(TOP VIEW)




## description

The 'ABTH18504A and 'ABTH182504A scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), clock-enable ($\overline{\text{CLKENAB}}$ and $\overline{\text{CLKENBA}}$), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while $\overline{\text{CLKENAB}}$ is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and $\overline{\text{CLKENAB}}$ is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{\text{OEAB}}$ is low, the B outputs are active. When $\overline{\text{OEAB}}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow, but uses the $\overline{\text{OEBA}}$, LEBA, $\overline{\text{CLKENBA}}$, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

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## description (continued)

Four dedicated test pins observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Improved scan efficiency is accomplished through the adoption of a one boundary-scan cell (BSC) per I/O pin architecture. This architecture is implemented in such a way as to capture the most pertinent test data. A PSA/COUNT instruction also is included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The B-port outputs of 'ABTH182504A, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54ABTH18504A and SN54ABTH182504A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH18504A and SN74ABTH182504A are characterized for operation from –40°C to 85°C.

**FUNCTION TABLE†**
**(normal mode, each register)**

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{OEAB}$ | LEAB | $\overline{CLKENAB}$ | CLKAB | A | B |
| L | L | L | L | X | $B_0$‡ |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | H | X | X | $B_0$‡ |
| L | H | X | X | L | L |
| L | H | X | X | H | H |
| H | X | X | X | X | Z |

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established

## functional block diagram

Pin numbers shown are for the PM package.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A1–A20 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| B1–B20 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| CLKAB, CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| $\overline{\text{CLKENAB}}$, $\overline{\text{CLKENBA}}$ | Normal-function clock enables. See function table for normal-mode logic. |
| GND | Ground |
| LEAB, LEBA | Normal-function latch enables. See function table for normal-mode logic. |
| $\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. All test instructions, test data, and test control signals are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test-data registers: a 48-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

Test-Logic-Reset
TMS = H
TMS = L
Run-Test/Idle
TMS = L
TMS = H
Select-DR-Scan
TMS = H
Select-IR-Scan
TMS = H
TMS = L
Capture-DR
TMS = H
TMS = H
TMS = L
Capture-IR
TMS = L
Shift-DR
TMS = L
TMS = L
Shift-IR
TMS = L
TMS = H
TMS = H
TMS = H
Exit1-DR
TMS = H
Exit1-IR
TMS = L
TMS = L
Pause-DR
TMS = L
Pause-IR
TMS = L
TMS = H
TMS = H
TMS = L
Exit2-DR
TMS = L
Exit2-IR
TMS = H
TMS = H
Update-DR
Update-IR
TMS = H
TMS = L
TMS = H
TMS = L

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. TMS has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABTH18504A and 'ABTH182504A, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–46 in the boundary-scan register are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

### Shift-DR (continued)

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state can suspend and resume data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'ABTH18504A and 'ABTH182504A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle, in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state can suspend and resume instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the ’ABTH18504A and ’ABTH182504A. The even-parity feature specified for SCOPE™ devices is supported in these devices. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by these devices default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

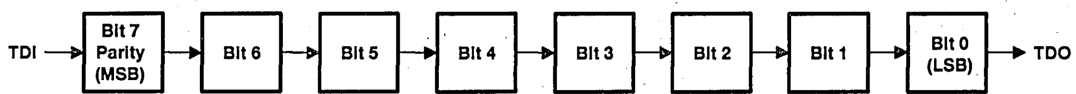


**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–46 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | $\overline{\text{OEAB}}$ | 39 | A20-I/O | 19 | B20-I/O |
| 46 | $\overline{\text{OEBA}}$ | 38 | A19-I/O | 18 | B19-I/O |
| 45 | CLKAB | 37 | A18-I/O | 17 | B18-I/O |
| 44 | CLKBA | 36 | A17-I/O | 16 | B17-I/O |
| 43 | $\overline{\text{CLKENAB}}$ | 35 | A16-I/O | 15 | B16-I/O |
| 42 | $\overline{\text{CLKENBA}}$ | 34 | A15-I/O | 14 | B15-I/O |
| 41 | LEAB | 33 | A14-I/O | 13 | B14-I/O |
| 40 | LEBA | 32 | A13-I/O | 12 | B13-I/O |
| — | — | 31 | A12-I/O | 11 | B12-I/O |
| — | — | 30 | A11-I/O | 10 | B11-I/O |
| — | — | 29 | A10-I/O | 9 | B10-I/O |
| — | — | 28 | A9-I/O | 8 | B9-I/O |
| — | — | 27 | A8-I/O | 7 | B8-I/O |
| — | — | 26 | A7-I/O | 6 | B7-I/O |
| — | — | 25 | A6-I/O | 5 | B6-I/O |
| — | — | 24 | A5-I/O | 4 | B5-I/O |
| — | — | 23 | A4-I/O | 3 | B4-I/O |
| — | — | 22 | A3-I/O | 2 | B3-I/O |
| — | — | 21 | A2-I/O | 1 | B2-I/O |
| — | — | 20 | A1-I/O | 0 | B1-I/O |

### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run (RUNT) instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

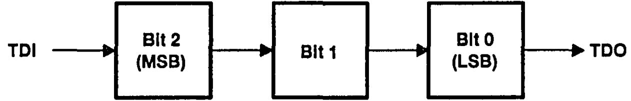


**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

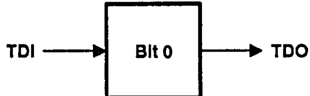


**Figure 4. Bypass Register Order of Scan**

### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'ABTH18504A , the binary value 00000000000000101000000000101111 (0002802F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74ABTH18504A.

For the 'ABTH182504A , the binary value 00000000000000101100000000101111 (0002C02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74ABTH182504A.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABTH18504A or 'ABTH182504A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output-enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–46 of the BSR). When a given output enable is active (logic 0), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a RUNT operation to specify which test operation is to be executed.

## boundary-control register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/40-bit mode (PRPG) |
| X10 | Parallel-signature analysis/40-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/20-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/20-bit mode (PSA/COUNT) |

While the control input BSCs (bits 47–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 47–46 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when the device is operating in one direction of data flow (that is, $\overline{OEAB} \neq \overline{OEBA}$). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 show the 40-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

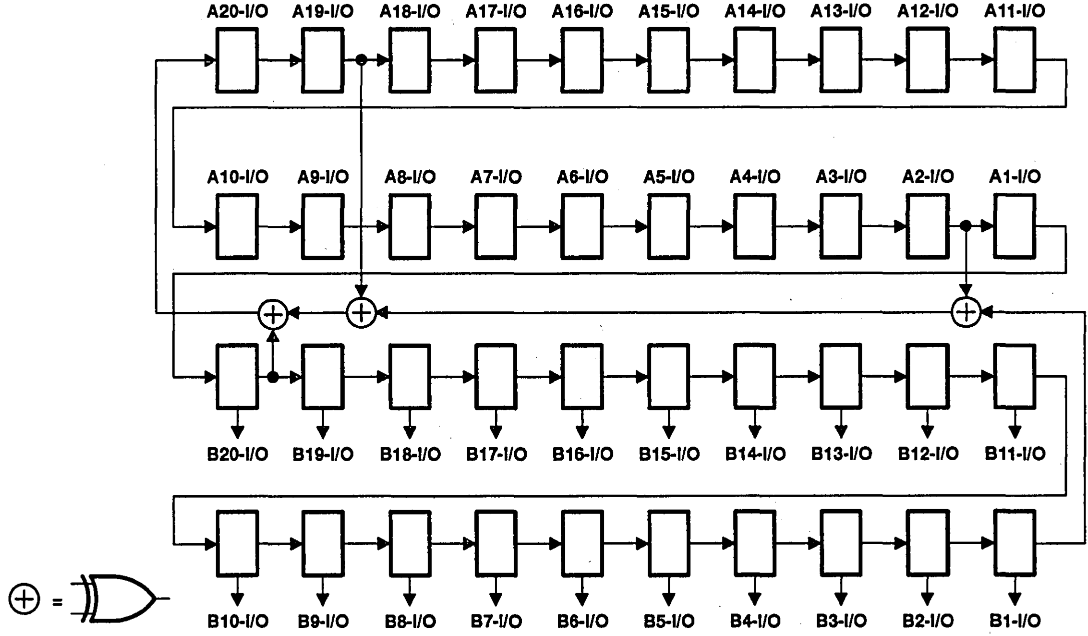


**Figure 5. 40-Bit PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

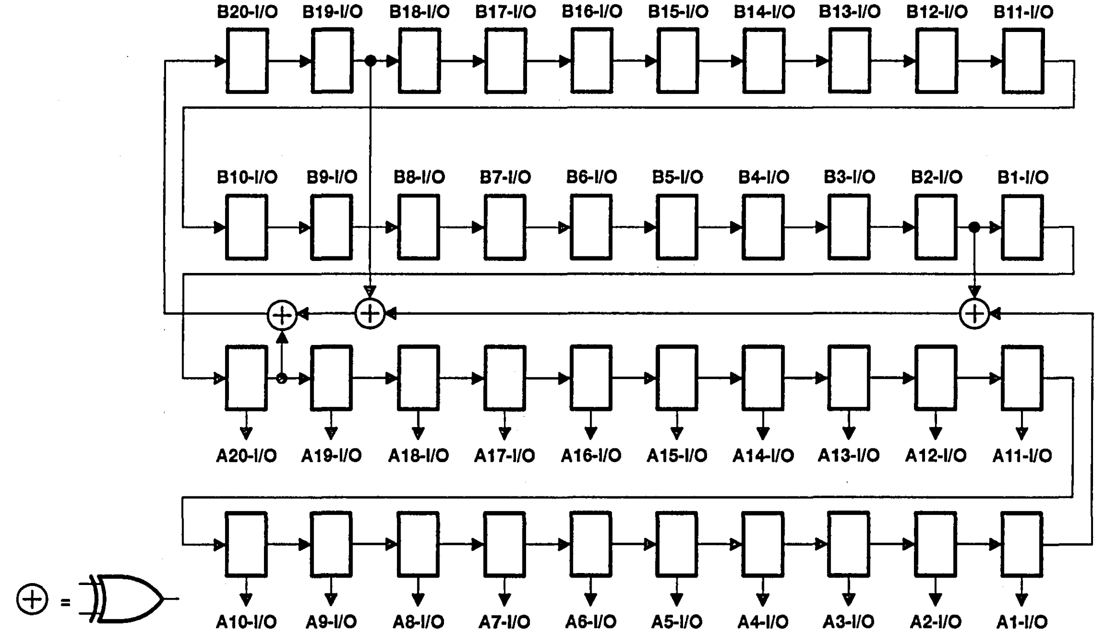


**Figure 6. 40-Bit PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

**parallel-signature analysis (PSA)**

Data appearing at the selected device input-mode I/O pins is compressed into a 40-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 show the 40-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

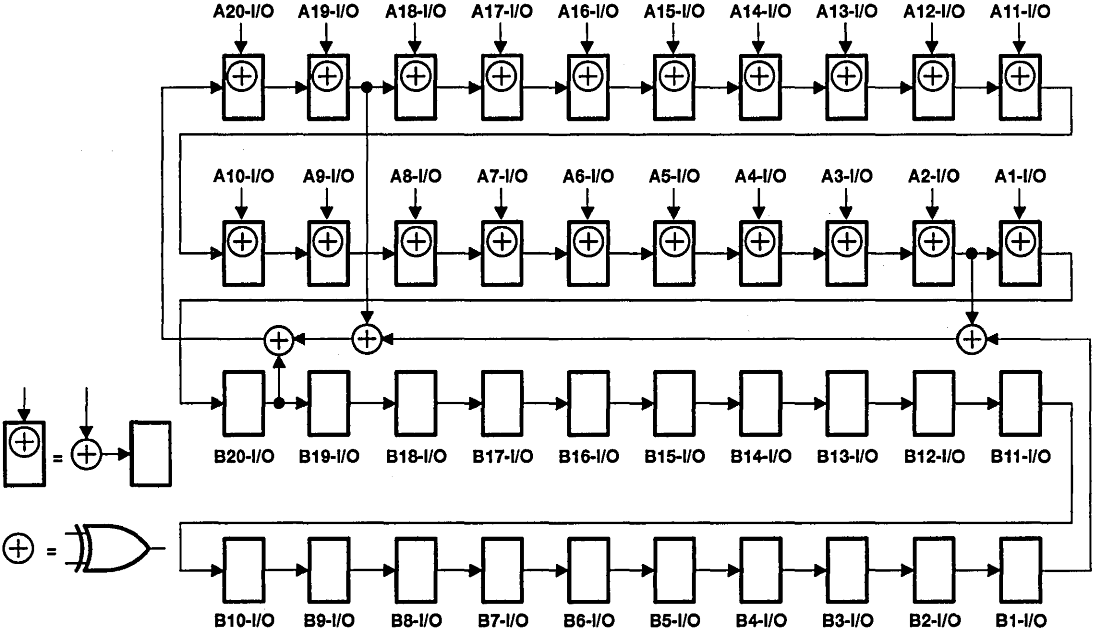


**Figure 7. 40-Bit PSA Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

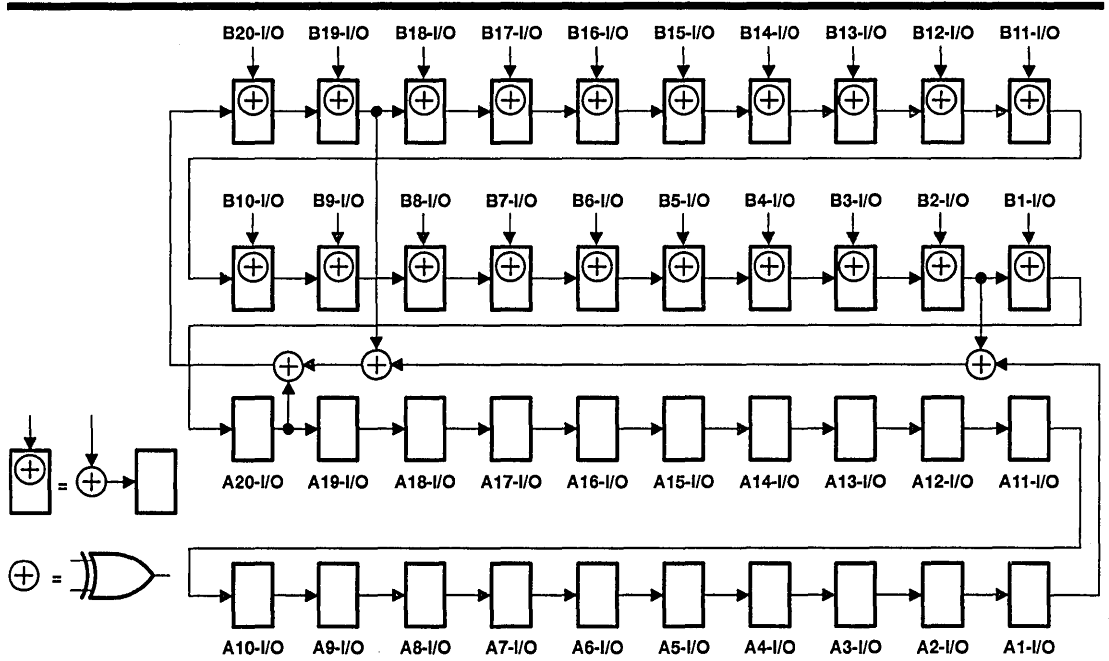


**Figure 8. 40-Bit PSA Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into a 20-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, a 20-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 show the 20-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

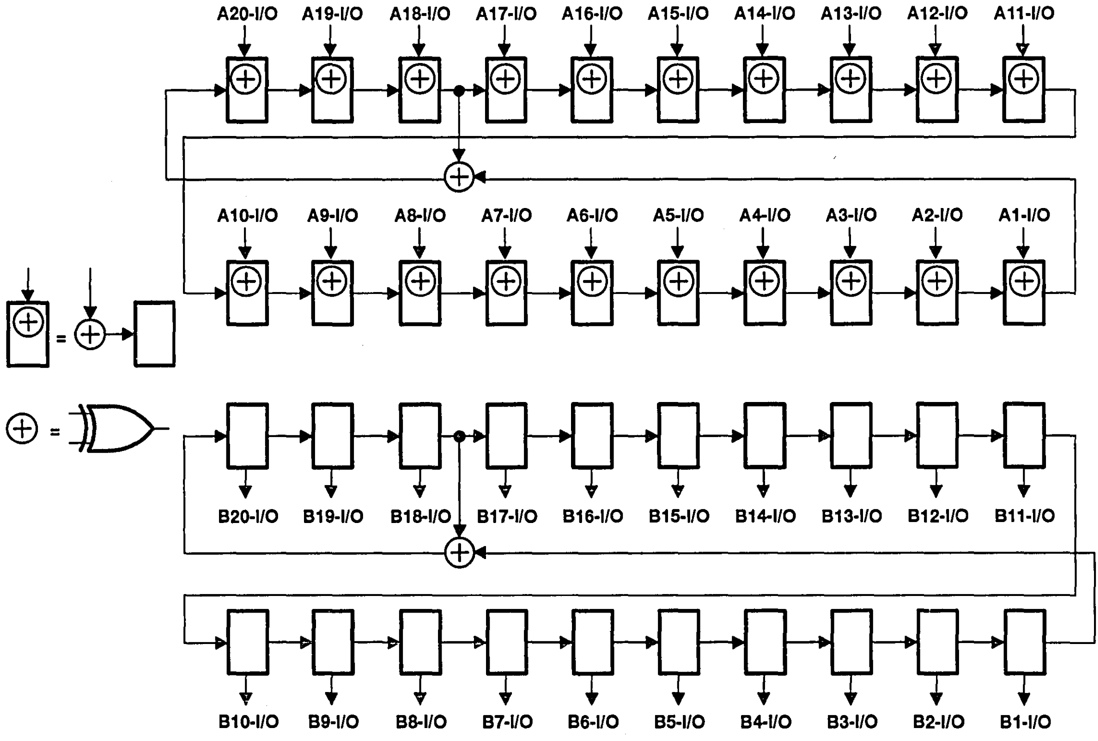


**Figure 9. 20-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

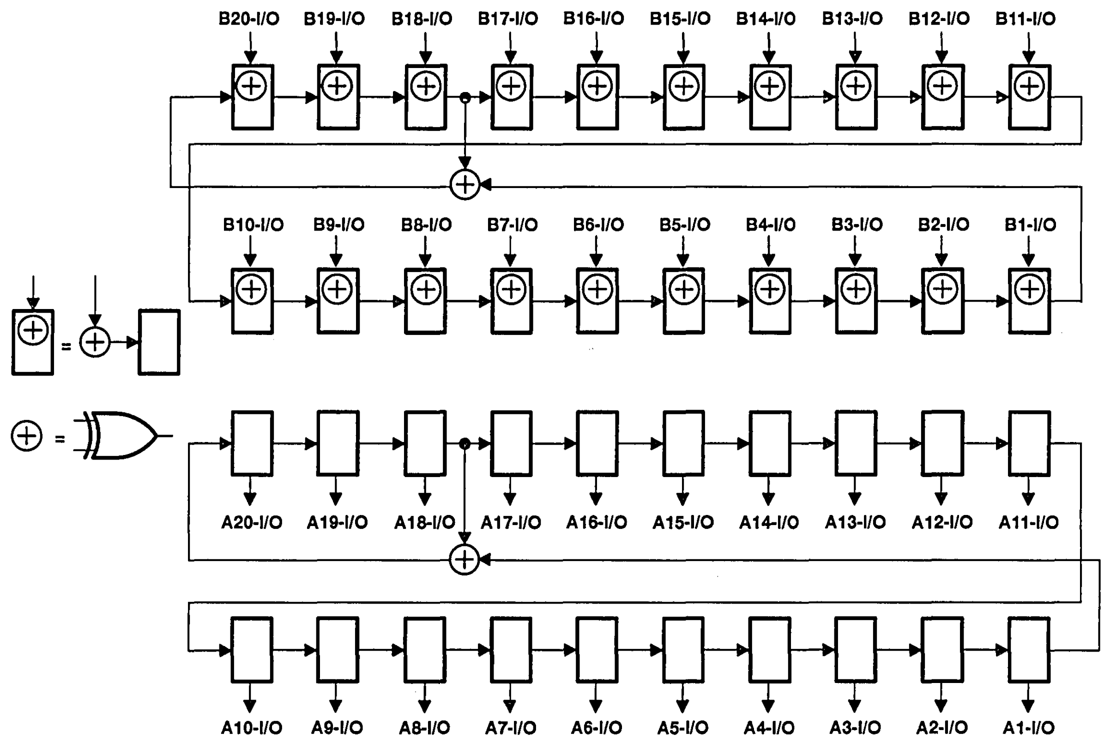


**Figure 10. 20-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into a 20-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, a 20-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 show the 20-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

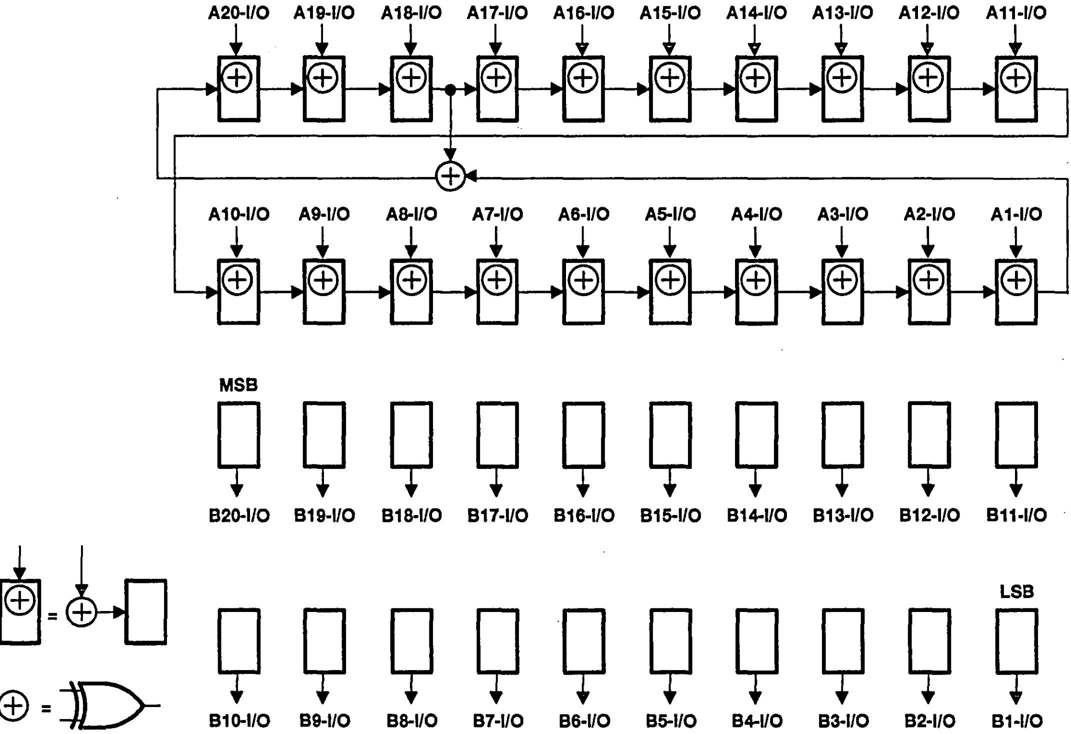


**Figure 11. 20-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

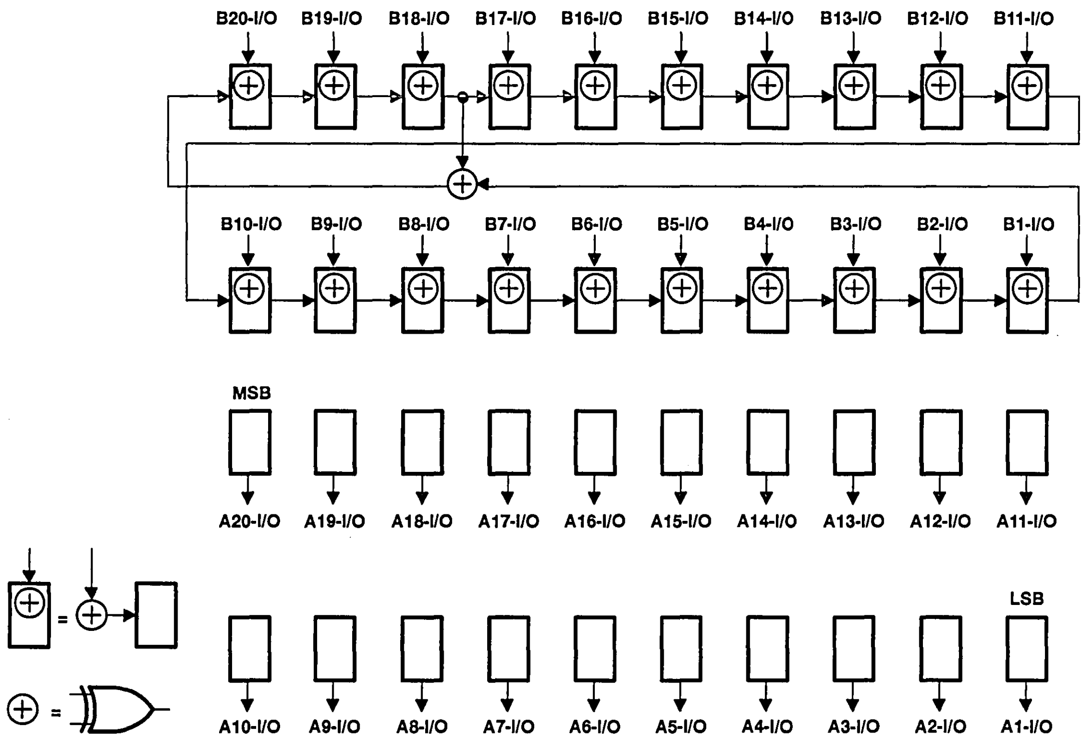


**Figure 12. 20-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

## timing description

All test operations of the 'ABTH18504A and 'ABTH182504A are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

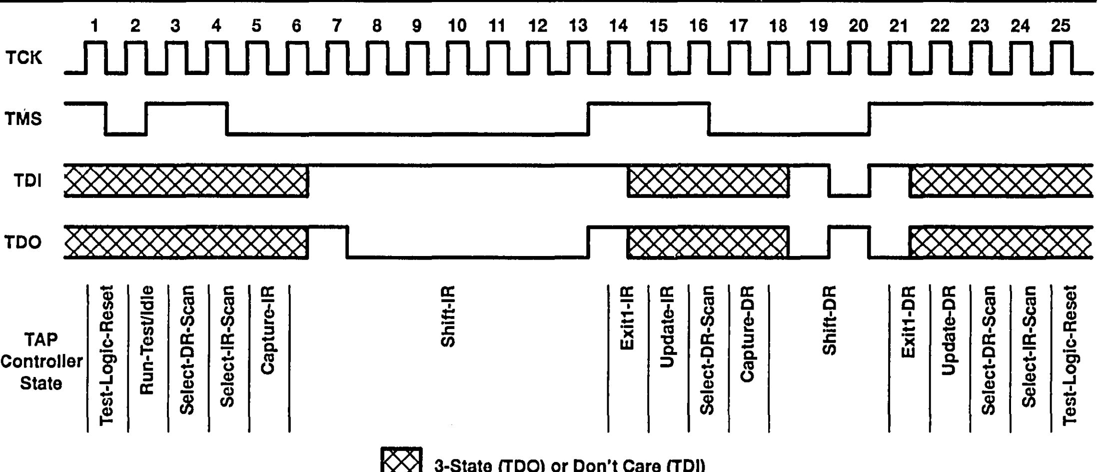


**Figure 13. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 7 V |
| Input voltage range, $V_I$: except I/O ports (see Note 1) | –0.5 V to 7 V |
| I/O ports (see Note 1) | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$: SN54ABTH18504A | 96 mA |
| SN54ABTH182504A (A port or TDO) | 96 mA |
| SN54ABTH182504A (B port) | 30 mA |
| SN74ABTH18504A | 128 mA |
| SN74ABTH182504A (A port or TDO) | 128 mA |
| SN74ABTH182504A (B port) | 30 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | –18 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | –50 mA |
| Continuous current through $V_{CC}$ | 576 mA |
| Continuous current through GND | 1152 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): PM package | 1 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | SN54ABTH18504A | | SN74ABTH18504A | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABTH18504A | | SN74ABTH18504A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $I_I$ | CLK, $\overline{CLKEN}$, LE, TCK | $V_{CC}$ = 0 to 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±20 | | ±20 | | ±20 | |
| $I_{IH}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | | 10 | µA |
| $I_{IL}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –150 | –40 | –150 | –40 | –150 | µA |
| $I_{I(hold)}$‡ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 75 | 220 | 500 | | | 75 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | –180 | –500 | | | –75 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 2.7 V, $\overline{OE}$ = 2 V | | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 0.5 V, $\overline{OE}$ = 2 V | | | | –10 | | –10 | | –10 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, $V_I$ or $V_O$ ≤ 4.5 V | | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –110 | –200 | –50 | –200 | –50 | –200 | mA |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | | 1.6 | 2.2 | | 2.2 | | 2.2 | mA |
| | Outputs low | | | | 19 | 27 | | 27 | | 27 | |
| | Outputs disabled | | | | 0.9 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 5 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | | | | pF |

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

| | | | | SN54ABTH18504A | | SN74ABTH18504A | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | 4.5 | | 4.5 | | ns |
| | | LEAB or LEBA | CLK high or low | 3.5 | | 3.5 | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | 3.5 | | 3.5 | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | 3.5 | | 3.5 | | |
| | | | CLK low | 2 | | 2 | | |
| | | $\overline{CLKEN}$ before CLK↑ | | 4 | | 4 | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | 0.5 | | 0.5 | | ns |
| | | A after LEAB↓ or B after LEBA↓ | CLK high or low | 4 | | 4 | | |
| | | $\overline{CLKEN}$ after CLK↑ | | 0.5 | | 0.5 | | |

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| | | | SN54ABTH18504A | | SN74ABTH18504A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 8 | | 8 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, LE, or $\overline{OE}$ before TCK↑ | 6 | | 6 | | ns |
| | | TDI before TCK↑ | 4.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3 | | 3 | | |
| $t_h$ | Hold time | A, B, CLK, LE, or $\overline{OE}$ after TCK↑ | 1.5 | | 1.5 | | ns |
| | | TDI after TCK↑ | 1 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | µs |

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### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH18504A | | SN74ABTH18504A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | 1.5 | 3.1 | 5 | 1.5 | 6 | 1.5 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 5 | 1.5 | 6 | 1.5 | 5.5 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 1.5 | 3.7 | 5 | 1.5 | 6 | 1.5 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.8 | 5 | 1.5 | 6 | 1.5 | 5.5 | |
| $t_{PLH}$ | LEAB or LEBA | B or A | 1.5 | 3.9 | 5.5 | 1.5 | 6.5 | 1.5 | 6 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 5.5 | 1.5 | 6.5 | 1.5 | 6 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 1.5 | 4.6 | 5.8 | 1.5 | 7.5 | 1.5 | 7 | ns |
| $t_{PZL}$ | | | 1.5 | 4.8 | 5.8 | 1.5 | 7.5 | 1.5 | 7 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 3 | 7.1 | 8.4 | 3 | 9.9 | 3 | 9.6 | ns |
| $t_{PLZ}$ | | | 2 | 5 | 6.3 | 2 | 8.9 | 2 | 7.2 | |

PRODUCT PREVIEW

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH18504A | | SN74ABTH18504A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 7.4 | 11 | 2.5 | 14.5 | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | 2.5 | 7.6 | 10.8 | 2.5 | 14 | 2.5 | 12.4 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.8 | 5.1 | 2 | 7 | 2 | 5.6 | ns |
| $t_{PHL}$ | | | 2 | 4 | 5.1 | 2 | 7 | 2 | 5.6 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 8 | 11.5 | 4 | 14.5 | 4 | 13.4 | ns |
| $t_{PZL}$ | | | 4 | 8 | 11.8 | 4 | 15 | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.9 | 5.7 | 2 | 7.5 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2 | 4.2 | 6.2 | 2 | 8 | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 10.8 | 13 | 4 | 18 | 4 | 15 | ns |
| $t_{PLZ}$ | | | 3 | 9.1 | 13.3 | 3 | 17.5 | 3 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.3 | 6.8 | 3 | 8 | 3 | 7.2 | ns |
| $t_{PLZ}$ | | | 2.5 | 4.2 | 5.5 | 2.5 | 8 | 2.5 | 6.3 | |

PRODUCT PREVIEW

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## recommended operating conditions

| | | | SN54ABTH182504A | | SN74ABTH182504A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| | | B port | | 12 | | 12 | |
| Δt/Δv | Input transition rise or fall rate | | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

PRODUCT PREVIEW

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### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABTH182504A | | SN74ABTH182504A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | A port, TDO | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| | B port | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –1 mA | 3.35 | | | 3.3 | | 3.35 | | |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –1 mA | 3.85 | | | 3.8 | | 3.85 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | 3.1 | | | 3 | | 3.1 | | |
| | | | $I_{OH}$ = –12 mA | 2.6* | | | | | 2.6 | | |
| $V_{OL}$ | A port, TDO | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| | B port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 8 mA | | | 0.8 | | 0.8 | | 0.65 | |
| | | | $I_{OL}$ = 12 mA | | | 0.8* | | | | 0.8 | |
| $I_I$ | CLK, $\overline{CLKEN}$, LE, TCK | $V_{CC}$ = 0 to 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±20 | | ±20 | | ±20 | |
| $I_{IH}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | | 10 | µA |
| $I_{IL}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –150 | –40 | –150 | –40 | –150 | µA |
| $I_{I(hold)}$‡ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 75 | 220 | 500 | | | 75 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | –180 | –500 | | | –75 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 2.7 V, $\overline{OE}$ = 2 V | | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 0.5 V, $\overline{OE}$ = 2 V | | | | –10 | | –10 | | –10 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, $V_I$ or $V_O$ ≤ 4.5 V | | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | A port, TDO | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –110 | –200 | –50 | –200 | –50 | –200 | mA |
| | B port | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –25 | –55 | –100 | –25 | –100 | –25 | –100 | |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | | 1.4 | 2.2 | | 2.2 | | 2.2 | mA |
| | Outputs low | | | | 25 | 30 | | 30 | | 30 | |
| | Outputs disabled | | | | 0.9 | 2 | | 2 | | 2 | |

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS | $T_A$ = 25°C | | | SN54ABTH182504A | | SN74ABTH182504A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $\Delta I_{CC}$‡ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | 5 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | 8 | | | | | | pF |

† All typical values are at $V_{CC}$ = 5 V.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

| | | | | SN54ABTH182504A | | SN74ABTH182504A | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | 4.5 | | 4.5 | | ns |
| | | LEAB or LEBA | CLK high or low | 3.5 | | 3.5 | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | 3.5 | | 3.5 | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | 3.5 | | 3.5 | | |
| | | | CLK low | 2 | | 2 | | |
| | | $\overline{CLKEN}$ before CLK↑ | | 4 | | 4 | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | 0.5 | | 0.5 | | ns |
| | | A after LEAB↓ or B after LEBA↓ | CLK high or low | 4 | | 4 | | |
| | | $\overline{CLKEN}$ after CLK↑ | | 0.5 | | 0.5 | | |

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| | | | SN54ABTH182504A | | SN74ABTH182504A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 8 | | 8 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, LE, or $\overline{OE}$ before TCK↑ | 6 | | 6 | | ns |
| | | TDI before TCK↑ | 4.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3 | | 3 | | |
| $t_h$ | Hold time | A, B, CLK, LE, or $\overline{OE}$ after TCK↑ | 1.5 | | 1.5 | | ns |
| | | TDI after TCK↑ | 1 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | µs |

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## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH182504A | | SN74ABTH182504A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | 100 | | MHz |
| $t_{PLH}$ | A | B | 1.5 | 3.5 | 5 | 1.5 | 6 | 1.5 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 4.1 | 5.6 | 1.5 | 6.4 | 1.5 | 6.2 | |
| $t_{PLH}$ | B | A | 1.5 | 3.2 | 5 | 1.5 | 6 | 1.5 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.4 | 5 | 1.5 | 6 | 1.5 | 5.5 | |
| $t_{PLH}$ | CLKAB | B | 1.5 | 3.9 | 5.4 | 1.5 | 6.2 | 1.5 | 6.1 | ns |
| $t_{PHL}$ | | | 1.5 | 4.2 | 5.8 | 1.5 | 6.4 | 1.5 | 6.2 | |
| $t_{PLH}$ | CLKBA | A | 1.5 | 4 | 5 | 1.5 | 6 | 1.5 | 5.5 | ns |
| $t_{PHL}$ | | | 1.5 | 4.2 | 5 | 1.5 | 6 | 1.5 | 5.5 | |
| $t_{PLH}$ | LEAB | B | 1.5 | 4.1 | 5.6 | 1.5 | 6.5 | 1.5 | 6.3 | ns |
| $t_{PHL}$ | | | 1.5 | 4.1 | 5.6 | 1.5 | 6.5 | 1.5 | 6.2 | |
| $t_{PLH}$ | LEBA | A | 1.5 | 4.1 | 5.5 | 1.5 | 6.5 | 1.5 | 6 | ns |
| $t_{PHL}$ | | | 1.5 | 3.9 | 5.5 | 1.5 | 6.5 | 1.5 | 6 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 1.5 | 4.5 | 5.8 | 1.5 | 7.5 | 1.5 | 7 | ns |
| $t_{PZL}$ | | | 1.5 | 4.5 | 5.8 | 1.5 | 7.5 | 1.5 | 7 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 3 | 5.5 | 8.4 | 3 | 9.9 | 3 | 9.6 | ns |
| $t_{PLZ}$ | | | 2 | 4.6 | 6.3 | 2 | 8.9 | 2 | 7.2 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH182504A | | SN74ABTH182504A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 6.8 | 11 | 2.5 | 14.5 | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | 2.5 | 7.2 | 10.8 | 2.5 | 14 | 2.5 | 12.4 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.6 | 5.1 | 2 | 7 | 2 | 5.6 | ns |
| $t_{PHL}$ | | | 2 | 3.8 | 5.1 | 2 | 7 | 2 | 5.6 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 7.8 | 11.5 | 4 | 14.5 | 4 | 13.4 | ns |
| $t_{PZL}$ | | | 4 | 7.8 | 11.8 | 4 | 15 | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.7 | 5.7 | 2 | 7.5 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2 | 3.9 | 6.2 | 2 | 8 | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 8.6 | 13 | 4 | 18 | 4 | 15 | ns |
| $t_{PLZ}$ | | | 3 | 7.9 | 13.3 | 3 | 17.5 | 3 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.2 | 6.8 | 3 | 8 | 3 | 7.2 | ns |
| $t_{PLZ}$ | | | 2.5 | 4 | 5.5 | 2.5 | 8 | 2.5 | 6.3 | |

PRODUCT PREVIEW

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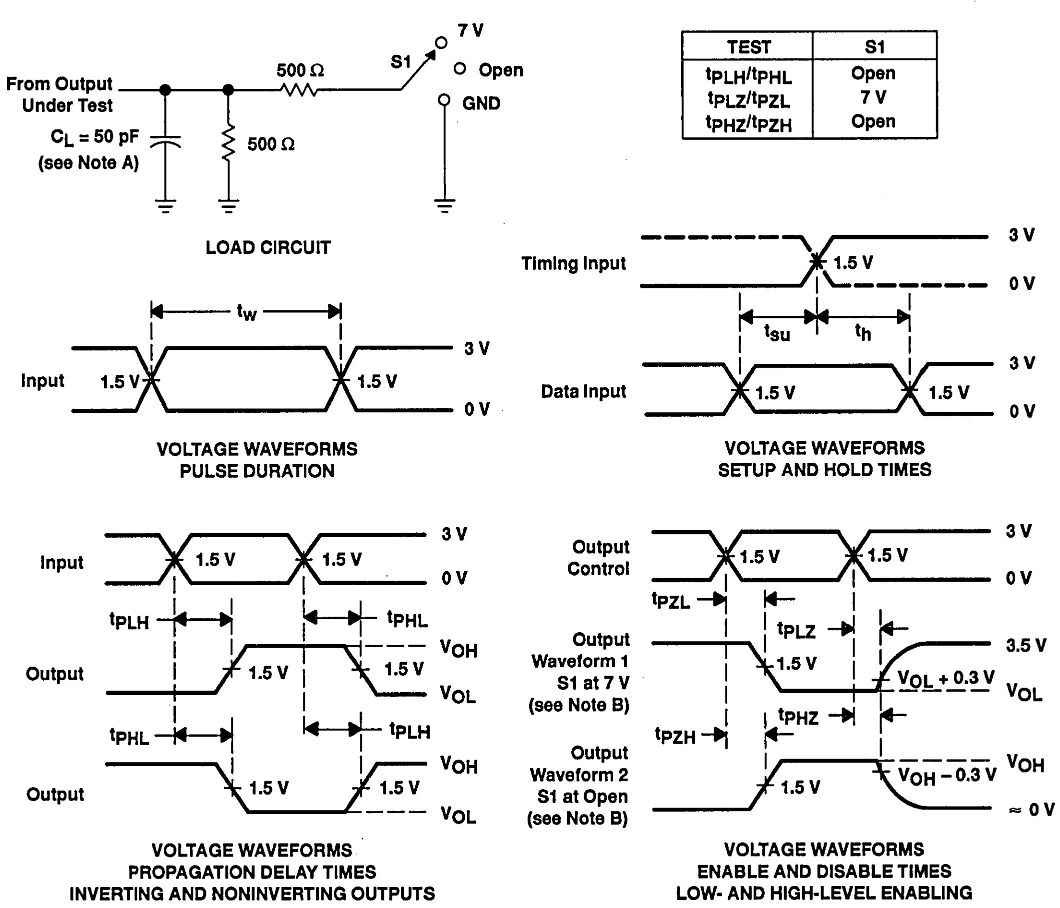
## PARAMETER MEASUREMENT INFORMATION

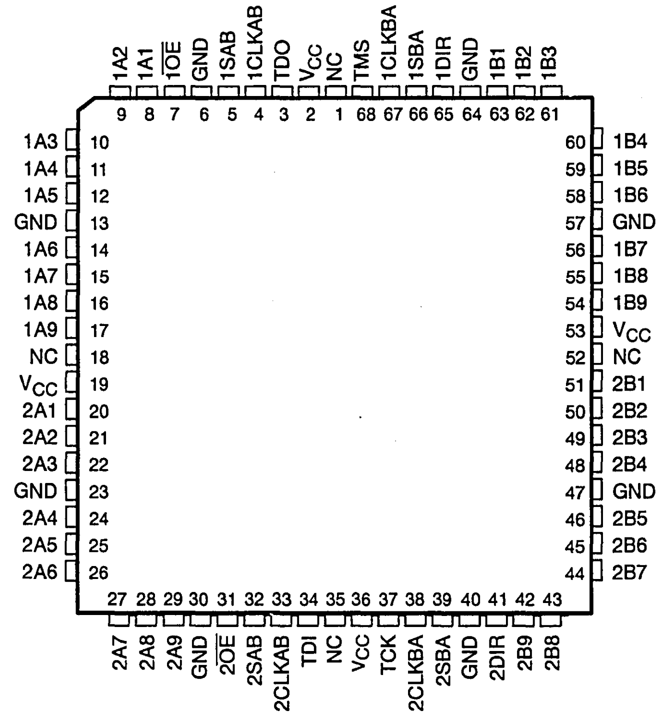



NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- B-Port Outputs of 'ABTH182646A Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC*-IIB™ BiCMOS Design
- One Boundary-Scan Cell Per I/O Architecture Improves Scan Efficiency
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54ABTH18646A, SN54ABTH182646A . . . HV PACKAGE
(TOP VIEW)




NC – No internal connection

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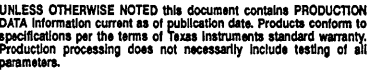

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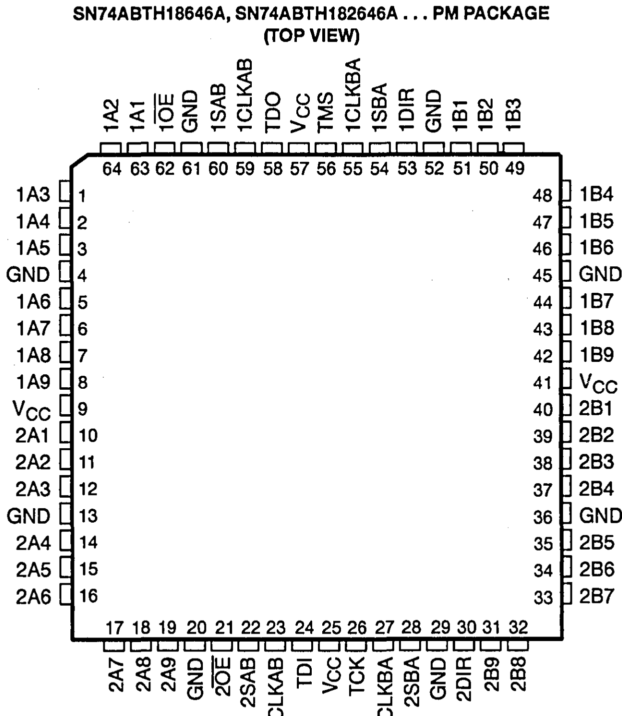
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN74ABTH18646A, SN74ABTH182646A . . . PM PACKAGE
(TOP VIEW)




## description

The 'ABTH18646A and 'ABTH182646A scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Transceiver function is controlled by output-enable ($\overline{OE}$) and direction (DIR) inputs. When $\overline{OE}$ is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When $\overline{OE}$ is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 shows the four fundamental bus-management functions that are performed with the 'ABTH18646A and 'ABTH182646A.

## description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Improved scan efficiency is accomplished through the adoption of a one boundary-scan cell (BSC) per I/O pin architecture. This architecture is implemented in such a way as to capture the most pertinent test data. A PSA/COUNT instruction also is included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The B-port outputs of 'ABTH182646A, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54ABTH18646A and SN54ABTH182646A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH18646A and SN74ABTH182646A are characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(normal mode, each 9-bit section)**

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA | A1 – A9 | B1 – B9 | |
| X | X | ↑ | X | X | X | Input | Unspecified† | Store A, B unspecified† |
| X | X | X | ↑ | X | X | Unspecified† | Input | Store B, A unspecified† |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| H | X | L | L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | X | X | H | Output | Input disabled | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | X | X | H | X | Input disabled | Output | Stored A data to B bus |

† The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data-input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

BUS A BUS B

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER BUS B TO BUS A**

BUS A BUS B

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | H | X | X | L | X |

**REAL-TIME TRANSFER BUS A TO BUS B**

BUS A BUS B

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| H | X | ↑ | ↑ | X | X |

**STORAGE FROM A, B, OR A AND B**

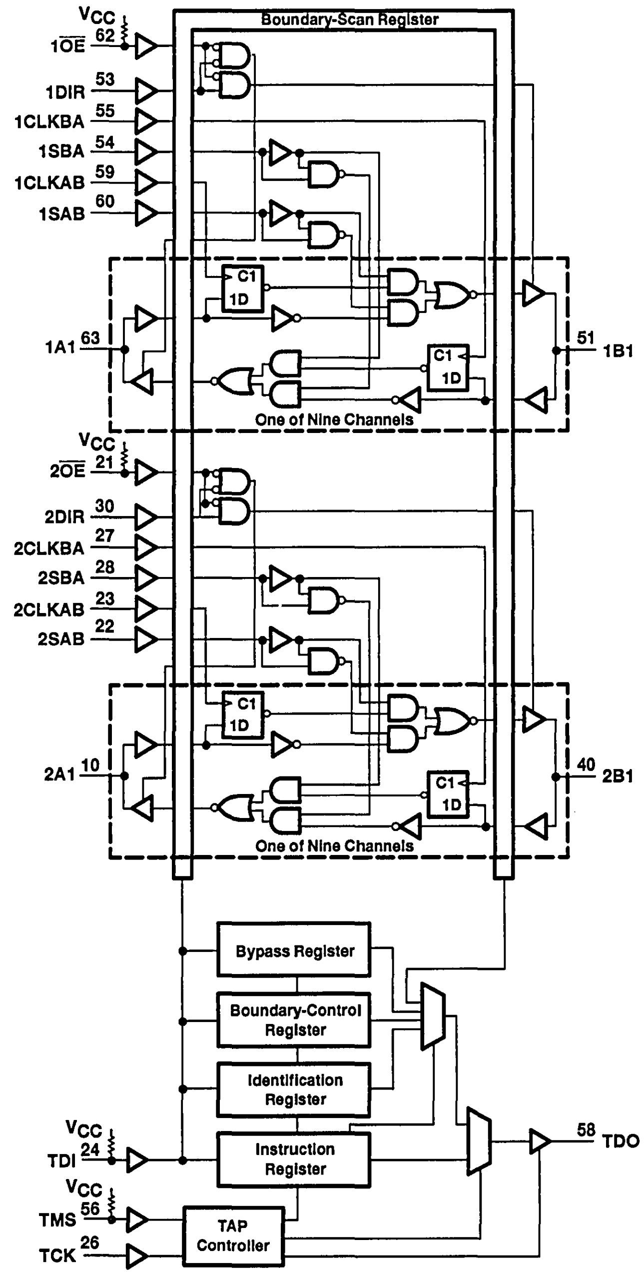
BUS A BUS B

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | H |
| L | H | X | X | H | X |

**TRANSFER STORED DATA TO A AND/OR B**

**Figure 1. Bus-Management Functions**

## functional block diagram




Pin numbers shown are for the PM package.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| 1DIR, 2DIR | Normal-function direction controls. See function table for normal-mode logic. |
| GND | Ground |
| $1\overline{OE}$, $2\overline{OE}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| 1SAB, 1SBA, 2SAB, 2SBA | Normal-function select controls. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. All test instructions, test data, and test control signals are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. Figure 2 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test-data registers: a 52-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

Test-Logic-Reset
TMS = H
TMS = L
Run-Test/Idle
TMS = L
TMS = H
Select-DR-Scan
TMS = H
Select-IR-Scan
TMS = H
TMS = L
Capture-DR
TMS = H
TMS = H
Capture-IR
TMS = L
Shift-DR
TMS = L
Shift-IR
TMS = L
TMS = H
Exit1-DR
TMS = H
Exit1-IR
TMS = H
TMS = L
Pause-DR
TMS = L
Pause-IR
TMS = L
TMS = H
Exit2-DR
TMS = L
TMS = L
Exit2-IR
TMS = H
Update-DR
Update-IR
TMS = H
TMS = L
TMS = H
TMS = L

**Figure 2. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 2 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABTH18646A and 'ABTH182646A, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 51–48 in the boundary-scan register are reset to logic 0, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following-data register or instruction-register scans. Run-Test/Idle is provided as a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

### Shift-DR (continued)

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state can suspend and resume data register-scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'ABTH18646A and 'ABTH182646A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle, in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state can suspend and resume instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABTH18646A and 'ABTH182646A. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 3.

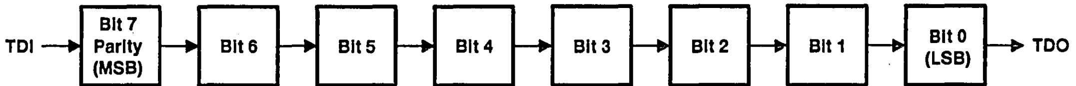



**Figure 3. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 52 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, one BSC for each normal-function I/O pin (one single cell for both input data and output data), and one BSC for each of the internally decoded output-enable signals (1OEA, 2OEA, 1OEB, 2OEB). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 51–48 are reset to logic 0, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

When external data is to be captured, the BSCs for signals 1OEA, 2OEA, 1OEB, and 2OEB capture logic values determined by the following positive-logic equations: 1OEA = 1$\overline{OE}$ • $\overline{1DIR}$, 2OEA = 2$\overline{OE}$ • $\overline{2DIR}$, 1OEB = 1$\overline{OE}$ • DIR, and 2OEB = 2$\overline{OE}$ • DIR. When data is to be applied externally, these BSCs control the drive state (active or high impedance) of their respective outputs.

The BSR order of scan is from TDI through bits 51–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 51 | 2OEB | 35 | 2A9-I/O | 17 | 2B9-I/O |
| 50 | 1OEB | 34 | 2A8-I/O | 16 | 2B8-I/O |
| 49 | 2OEA | 33 | 2A7-I/O | 15 | 2B7-I/O |
| 48 | 1OEA | 32 | 2A6-I/O | 14 | 2B6-I/O |
| 47 | 2DIR | 31 | 2A5-I/O | 13 | 2B5-I/O |
| 46 | 1DIR | 30 | 2A4-I/O | 12 | 2B4-I/O |
| 45 | 2$\overline{OE}$ | 29 | 2A3-I/O | 11 | 2B3-I/O |
| 44 | 1$\overline{OE}$ | 28 | 2A2-I/O | 10 | 2B2-I/O |
| 43 | 2CLKAB | 27 | 2A1-I/O | 9 | 2B1-I/O |
| 42 | 1CLKAB | 26 | 1A9-I/O | 8 | 1B9-I/O |
| 41 | 2CLKBA | 25 | 1A8-I/O | 7 | 1B8-I/O |
| 40 | 1CLKBA | 24 | 1A7-I/O | 6 | 1B7-I/O |
| 39 | 2SAB | 23 | 1A6-I/O | 5 | 1B6-I/O |
| 38 | 1SAB | 22 | 1A5-I/O | 4 | 1B5-I/O |
| 37 | 2SBA | 21 | 1A4-I/O | 3 | 1B4-I/O |
| 36 | 1SBA | 20 | 1A3-I/O | 2 | 1B3-I/O |
| — | — | 19 | 1A2-I/O | 1 | 1B2-I/O |
| — | — | 18 | 1A1-I/O | 0 | 1B1-I/O |

### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run test (RUNT) instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 4.

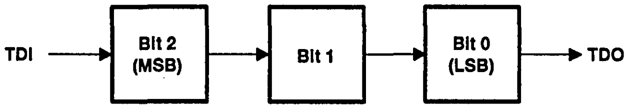



**Figure 4. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 5.

**Figure 5. Bypass Register Order of Scan**

### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'ABTH18646A, the binary value 00000000000000101001000000101111 (0002902F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74ABTH18646A.

For the 'ABTH182646A, the binary value 00000000000000101101000000101111 (0002D02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74ABTH182646A.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary-run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABTH18646A or 'ABTH182646A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 51–48 of the BSR). When a given output enable is active (logic 1), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 51–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 51–48 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when both bytes of the device are operating in one direction of data flow (that is, 1OEA ≠ 1OEB and 2OEA ≠ 2OEB) and in the same direction of data flow (that is, 1OEA = 2OEA and 1OEB = 2OEB). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

**pseudo-random pattern generation (PRPG)**

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 6 and 7 illustrate the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

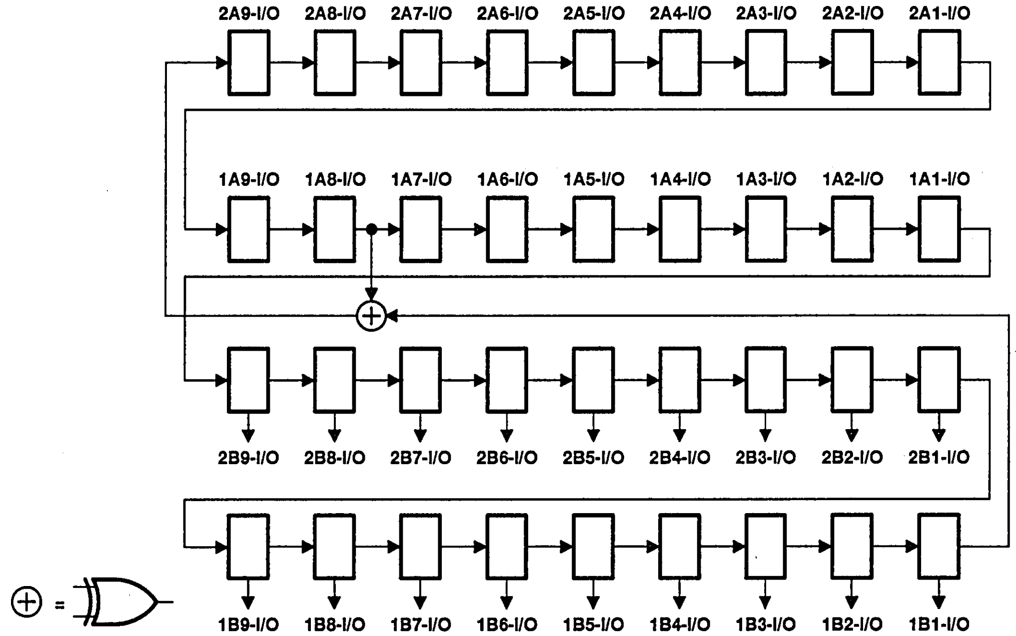



**Figure 6. 36-Bit PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

**pseudo-random pattern generation (PRPG) (continued)**

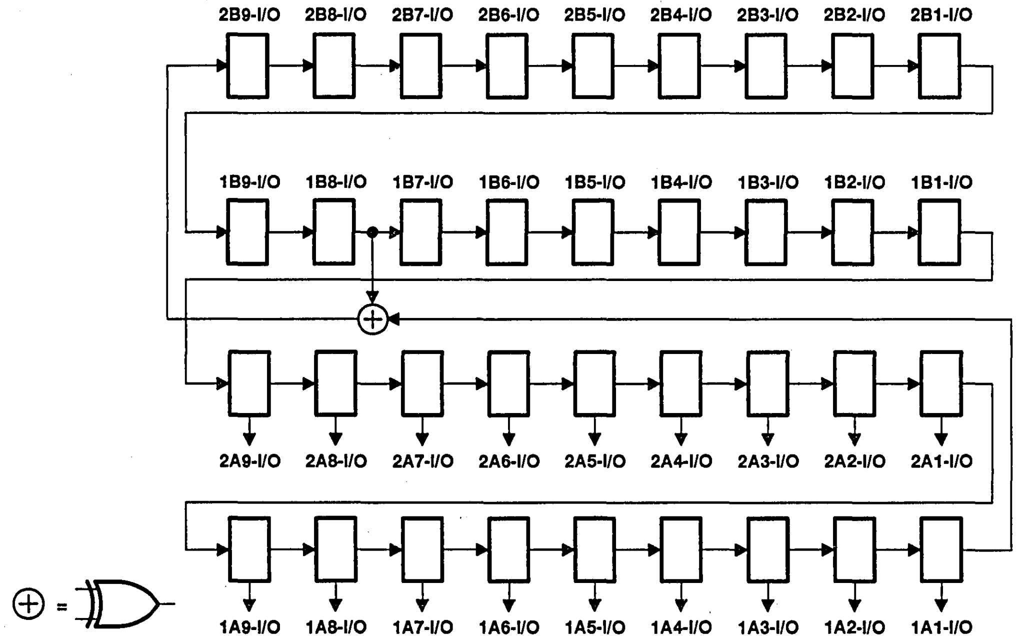



**Figure 7. 36-Bit PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 8 and 9 illustrate the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

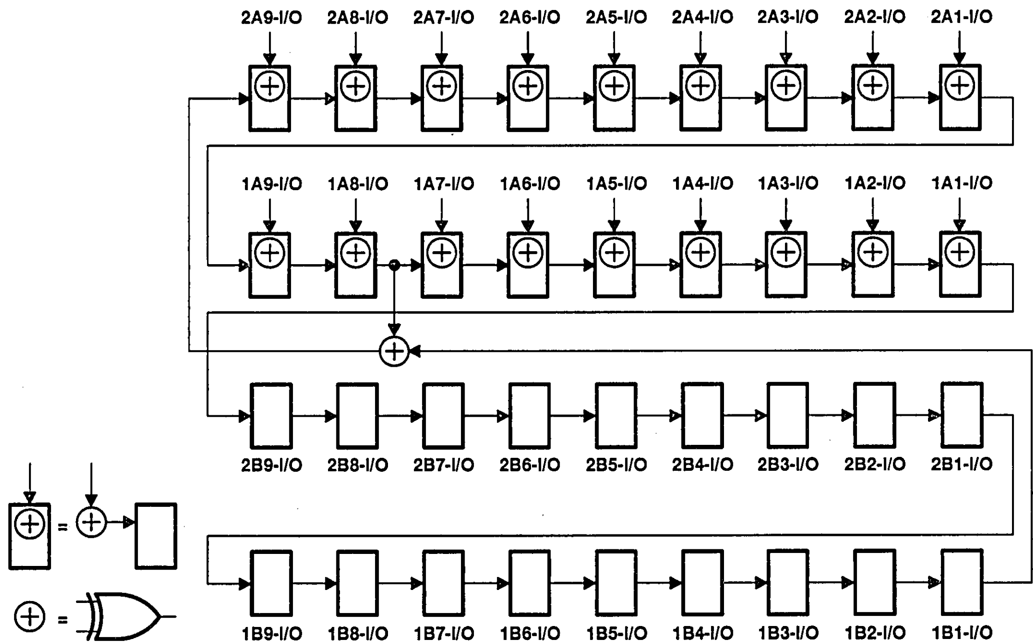



**Figure 8. 36-Bit PSA Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

**parallel-signature analysis (PSA) (continued)**

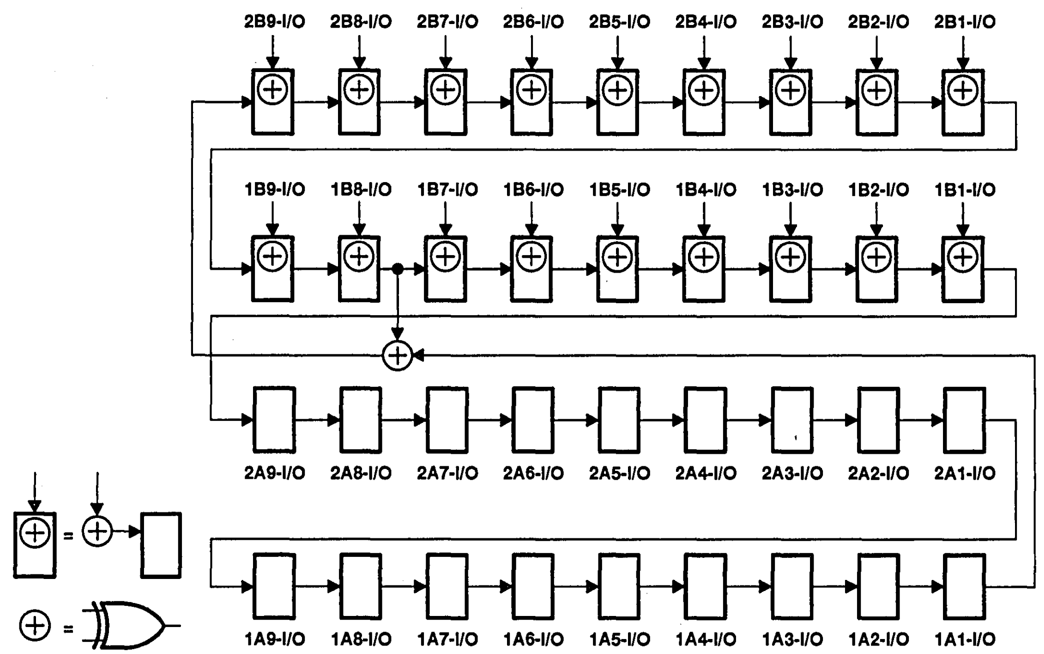



**Figure 9. 36-Bit PSA Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 10 and 11 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

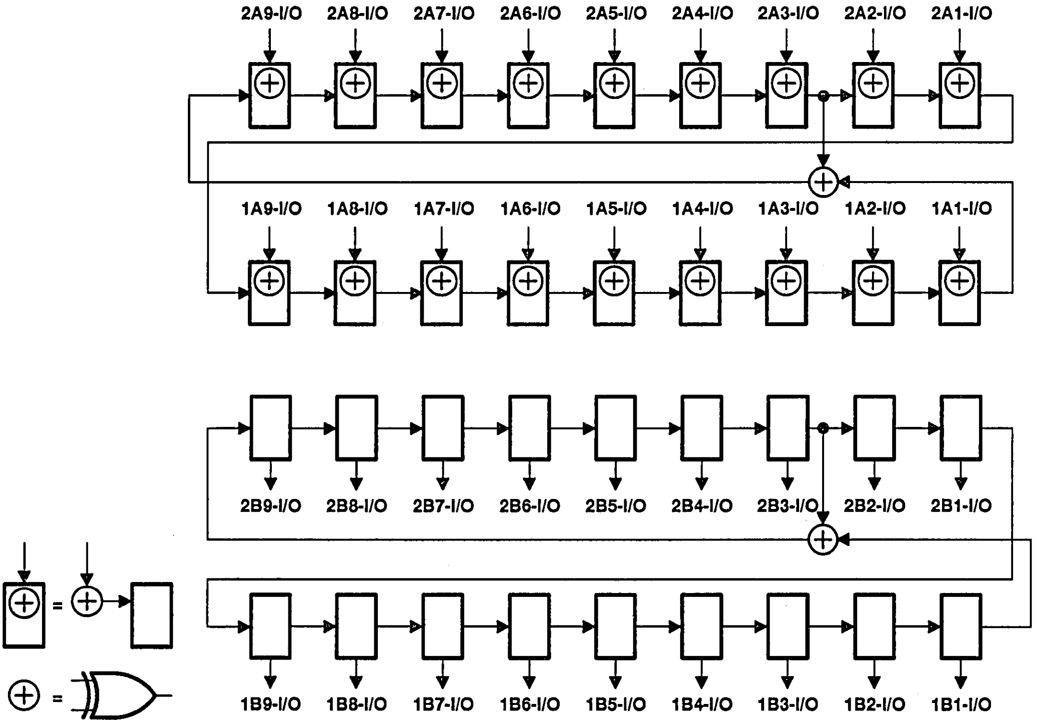



**Figure 10. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

**simultaneous PSA and PRPG (PSA/PRPG) (continued)**

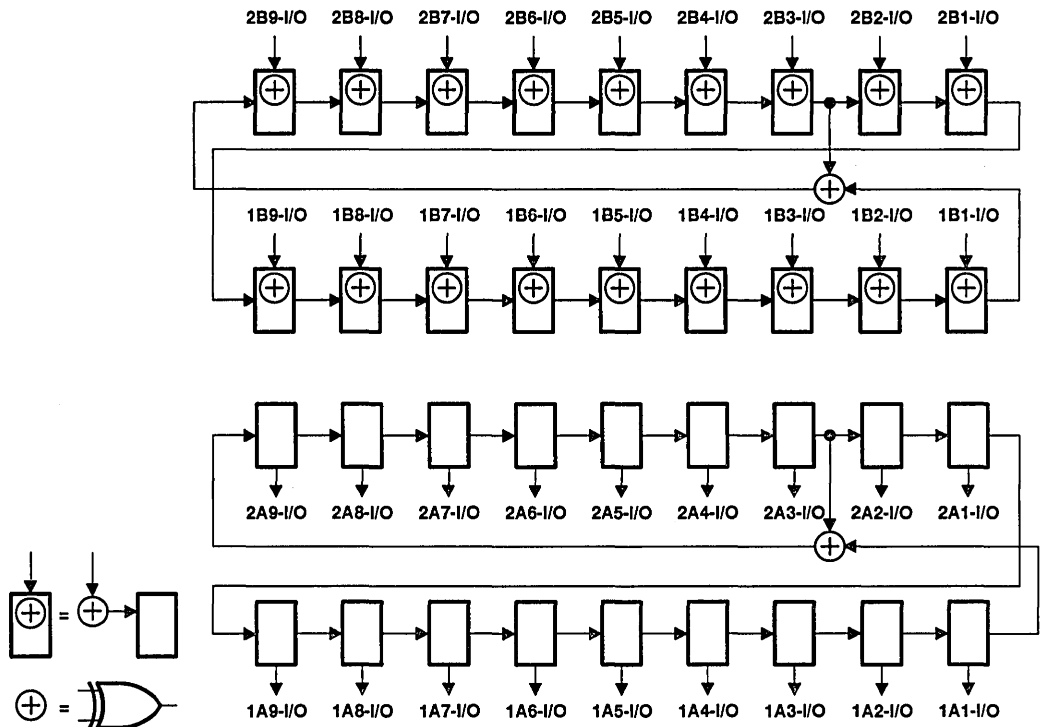



**Figure 11. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 12 and 13 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

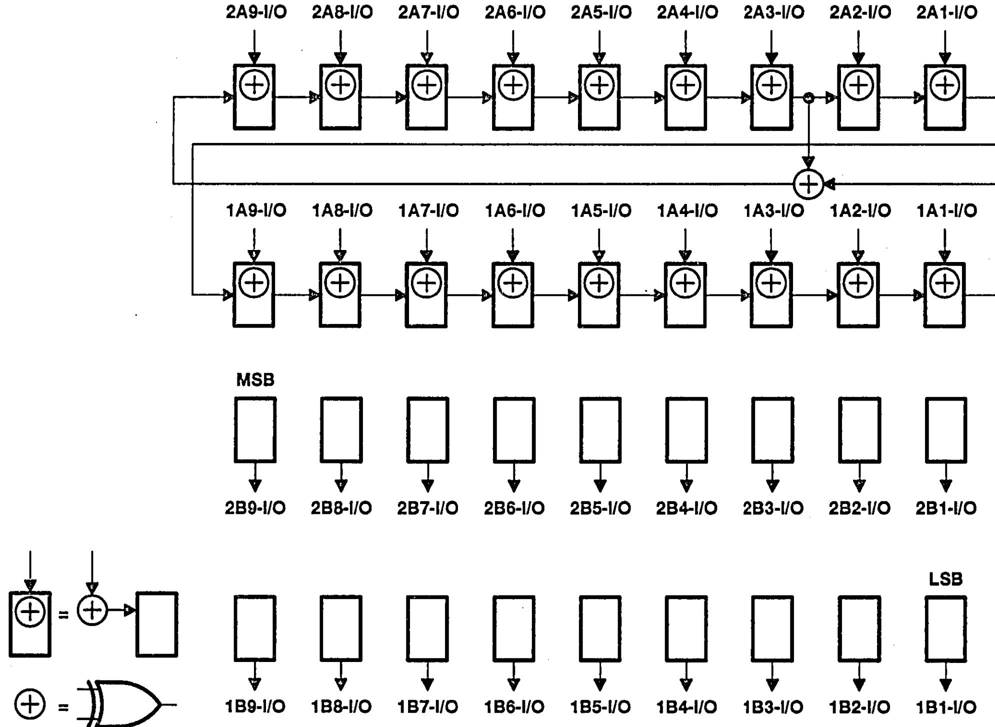



**Figure 12. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

**simultaneous PSA and binary count up (PSA/COUNT) (continued)**

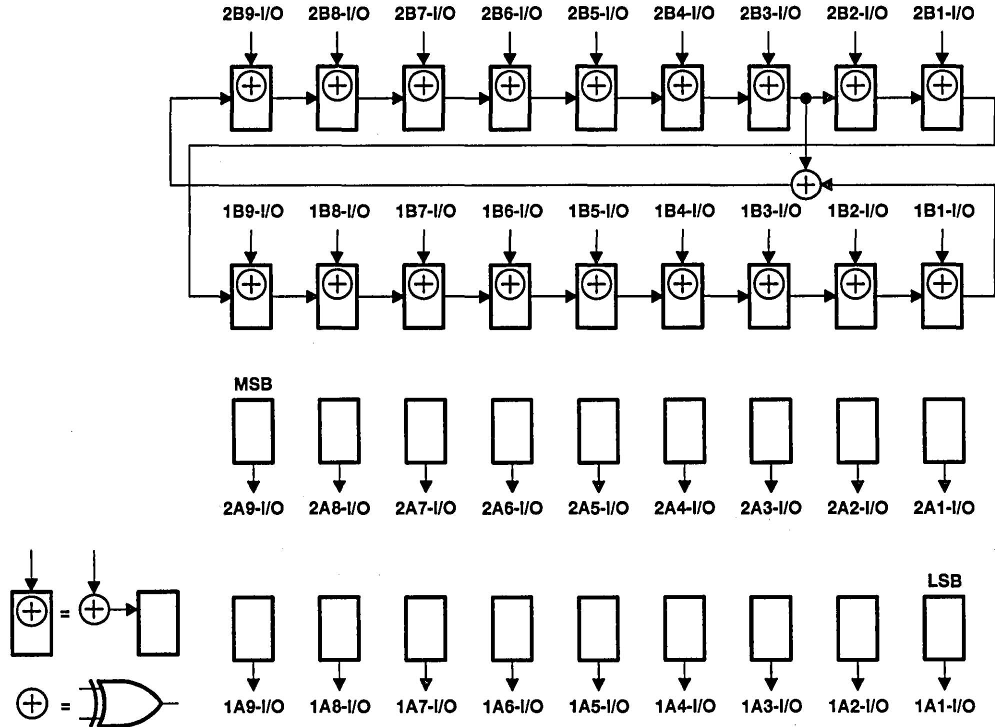



**Figure 13. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

## timing description

All test operations of the 'ABTH18646A and 'ABTH182646A are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 2) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 14. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, as necessary, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

### timing description (continued)

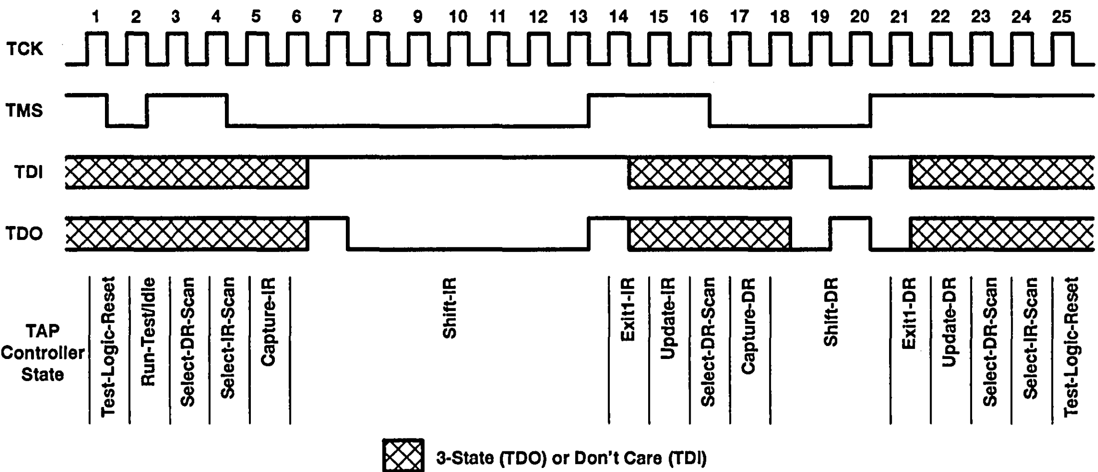



**Figure 14. Timing Example**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .......... –0.5 V to 7 V
Input voltage range, $V_I$: except I/O ports (see Note 1) .......... –0.5 V to 7 V
I/O ports (see Note 1) .......... –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, $V_O$ .......... –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABTH18646A .......... 96 mA
SN54ABTH182646A (A port or TDO) .......... 96 mA
SN54ABTH182646A (B port) .......... 30 mA
SN74ABTH18646A .......... 128 mA
SN74ABTH182646A (A port or TDO) .......... 128 mA
SN74ABTH182646A (B port) .......... 30 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) .......... –18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) .......... –50 mA
Maximum package power dissipation at $T_A$ = 55°C (in still air) (see Note 2): PM package .......... 1 W
Storage temperature range, $T_{stg}$ .......... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | SN54ABTH18646A | | SN74ABTH18646A | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ABTH18646A $T_A$ = 25°C MIN | TYP† | MAX | $T_A$ = –55°C to 125°C MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –24 mA | 2 | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | V |
| $I_I$ | CLK, DIR, S, TCK $V_{CC}$ = 0 to 5.5 V, | $V_{CC}$ = 0 to 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±20 | | ±20 | |
| $I_{IH}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | µA |
| $I_{IL}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –150 | –40 | –150 | µA |
| $I_{I(hold)}$‡ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 75 | 220 | 500 | | | µA |
| | | | $V_I$ = 2 V | –75 | –180 | –500 | | | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 5.5 V, $V_O$ = 2.7 V, | $\overline{OE}$ = 2 V | | | 10 | | 10 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 5.5 V, $V_O$ = 0.5 V, | $\overline{OE}$ = 2 V | | | –10 | | –10 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 2.7 V or 0.5 V, | $\overline{OE}$ = 0.8 V | | | ±50 | | | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, | $\overline{OE}$ = 0.8 V | | | ±50 | | | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±100 | | | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –110 | –200 | –50 | –200 | mA |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | | 1.7 | 3.9 | | 3.9 | mA |
| | Outputs low | | | | 20 | 24 | | 24 | |
| | Outputs disabled | | | | 1 | 3 | | 3 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 5 | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 10 | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | | pF |

† All typical values are at $V_{CC}$ = 5 V.
‡ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN74ABTH18646A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | |
| | | | | MIN | TYP† | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | | | |
| | | | $I_{OH}$ = –32 mA | 2 | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55 | | 0.55 | |
| $I_I$ | CLK, DIR, S, TCK $V_{CC}$ = 0 to 5.5 V, | $V_{CC}$ = 0 to 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±20 | | ±20 | |
| $I_{IH}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | µA |
| $I_{IL}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –150 | –40 | –150 | µA |
| $I_{I(hold)}$‡ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 75 | 220 | 500 | 75 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | –180 | –500 | –75 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 2.7 V, $\overline{OE}$ = 2 V | | | | 10 | | 10 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 0.5 V, $\overline{OE}$ = 2 V | | | | –10 | | –10 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \le$ 4.5 V | | | ±100 | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –110 | –200 | –50 | –200 | mA |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | | 1.7 | 2.2 | | 2.2 | mA |
| | Outputs low | | | | 20 | 24 | | 24 | |
| | Outputs disabled | | | | 1 | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 5 | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 10 | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | | pF |

† All typical values are at $V_{CC}$ = 5 V.
‡ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 15)

| | | | SN54ABTH18646A | | SN74ABTH18646A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | 3 | | 3 | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | 3 | | 3 | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | 0.9 | | 0.5 | | ns |

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 15)

| | | | SN54ABTH18646A | | SN74ABTH18646A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 8 | | 8 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, DIR, $\overline{OE}$, or S before TCK↑ | 6 | | 6 | | ns |
| | | TDI before TCK↑ | 4.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3 | | 3 | | |
| $t_h$ | Hold time | A, B, CLK, DIR, $\overline{OE}$, or S after TCK↑ | 1.5 | | 1.5 | | ns |
| | | TDI after TCK↑ | 1 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50* | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1* | | 1 | | µs |

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABTH18646A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –55°C to 125°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 150 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | 1.5 | 3.1 | 4.7 | 1.5 | 5.2 | ns |
| $t_{PHL}$ | | | 1.5 | 3.3 | 5.0 | 1.5 | 6 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 1.5 | 3.6 | 5.6 | 1.5 | 6.8 | ns |
| $t_{PHL}$ | | | 1.5 | 3.8 | 5.8 | 1.5 | 7 | |
| $t_{PLH}$ | SAB or SBA | B or A | 1.5 | 3.8 | 6.0 | 1.5 | 7.8 | ns |
| $t_{PHL}$ | | | 1.5 | 3.9 | 6.5 | 1.5 | 8.2 | |
| $t_{PZH}$ | DIR | B or A | 1.5 | 3.9 | 6.3 | 1.5 | 7.5 | ns |
| $t_{PZL}$ | | | 1.5 | 4 | 6.5 | 1.5 | 7.8 | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | 1.5 | 4.2 | 6.7 | 1.5 | 7.6 | ns |
| $t_{PZL}$ | | | 1.5 | 4.3 | 6.9 | 1.5 | 7.7 | |
| $t_{PHZ}$ | DIR | B or A | 2 | 5.9 | 8.8 | 2 | 10.3 | ns |
| $t_{PLZ}$ | | | 2 | 4.7 | 6.9 | 2 | 9.1 | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | 2 | 6 | 9 | 2 | 10.2 | ns |
| $t_{PLZ}$ | | | 2 | 4.8 | 7.1 | 2 | 9.4 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABTH18646A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 150 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | 1.5 | 3.1 | 4.7 | 1.5 | 5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.3 | 5.0 | 1.5 | 5.4 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 1.5 | 3.6 | 5.6 | 1.5 | 5.9 | ns |
| $t_{PHL}$ | | | 1.5 | 3.8 | 5.8 | 1.5 | 6.1 | |
| $t_{PLH}$ | SAB or SBA | B or A | 1.5 | 3.8 | 6.0 | 1.5 | 6.6 | ns |
| $t_{PHL}$ | | | 1.5 | 3.9 | 6.5 | 1.5 | 6.8 | |
| $t_{PZH}$ | DIR | B or A | 1.5 | 3.9 | 6.3 | 1.5 | 7 | ns |
| $t_{PZL}$ | | | 1.5 | 4 | 6.5 | 1.5 | 7.2 | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | 1.5 | 4.2 | 6.7 | 1.5 | 7.4 | ns |
| $t_{PZL}$ | | | 1.5 | 4.3 | 6.9 | 1.5 | 7.6 | |
| $t_{PHZ}$ | DIR | B or A | 2 | 5.9 | 8.8 | 2 | 10 | ns |
| $t_{PLZ}$ | | | 2 | 4.7 | 6.9 | 2 | 8.1 | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | 2 | 6 | 9 | 2 | 9.7 | ns |
| $t_{PLZ}$ | | | 2 | 4.8 | 7.1 | 2 | 7.6 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABTH18646A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 6.1 | 11 | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | 2.5 | 6.5 | 10.8 | 2.5 | 12.6 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.6 | 5.1 | 2 | 5.8 | ns |
| $t_{PHL}$ | | | 2 | 3.7 | 5.1 | 2 | 7 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 7.1 | 11.5 | 4 | 13.9 | ns |
| $t_{PZL}$ | | | 4 | 7.2 | 11.8 | 4 | 14.2 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.7 | 5.7 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2 | 3.9 | 6.2 | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 8.5 | 14.2 | 4 | 18 | ns |
| $t_{PLZ}$ | | | 3 | 7.2 | 13.3 | 3 | 17.5 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.1 | 6.8 | 3 | 7.4 | ns |
| $t_{PLZ}$ | | | 2.5 | 4 | 5.5 | 2.5 | 6.4 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABTH18646A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 6.1 | 11 | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | 2.5 | 6.5 | 10.8 | 2.5 | 12.4 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.6 | 5.1 | 2 | 5.6 | ns |
| $t_{PHL}$ | | | 2 | 3.7 | 5.1 | 2 | 5.6 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 7.1 | 11.5 | 4 | 13.4 | ns |
| $t_{PZL}$ | | | 4 | 7.2 | 11.8 | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.7 | 5.7 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2 | 3.9 | 6.2 | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 8.5 | 13 | 4 | 15 | ns |
| $t_{PLZ}$ | | | 3 | 7.2 | 13.3 | 3 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.1 | 6.8 | 3 | 7.2 | ns |
| $t_{PLZ}$ | | | 2.5 | 4 | 5.5 | 2.5 | 6.3 | |

## recommended operating conditions

| | | | SN54ABTH182646A | | SN74ABTH182646A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| | | B port | | 12 | | 12 | |
| Δt/Δv | Input transition rise or fall rate | | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

PRODUCT PREVIEW

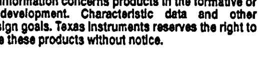
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABTH182646A | | SN74ABTH182646A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | A port, TDO | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | | | | | 2 | | |
| | B port | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –1 mA | 3.35 | | | 3.3 | | 3.35 | | |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –1 mA | 3.85 | | | 3.8 | | 3.85 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | 3.1 | | | 3 | | 3.1 | | |
| | | | $I_{OH}$ = –12 mA | 2.6* | | | | | 2.6 | | |
| $V_{OL}$ | A port, TDO | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| | B port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 8 mA | | | 0.8 | | 0.8 | | 0.65 | |
| | | | $I_{OL}$ = 12 mA | | | 0.8* | | | | 0.8 | |
| $I_I$ | CLK, DIR, S, TCK | $V_{CC}$ = 0 to 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±20 | | ±20 | | ±20 | |
| $I_{IH}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | 10 | | 10 | | 10 | µA |
| $I_{IL}$ | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | –40 | | –150 | –40 | –150 | –40 | –150 | µA |
| $I_{I(hold)}$‡ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 75 | 220 | 500 | | | 75 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | –180 | –500 | | | –75 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 5.5 V, $V_O$ = 2.7 V, | $\overline{OE}$ = 2 V | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 5.5 V, $V_O$ = 0.5 V, | $\overline{OE}$ = 2 V | | | –10 | | –10 | | –10 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | A port, TDO | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –110 | –200 | –50 | –200 | –50 | –200 | mA |
| | B port | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –25 | –55 | –100 | –25 | –100 | –25 | –100 | |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | | 1.7 | 2.2 | | 2.2 | | 2.2 | mA |
| | Outputs low | | | | 23 | 27 | | 27 | | 27 | |
| | Outputs disabled | | | | 1 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.


PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS | $T_A$ = 25°C | | | SN54ABTH182646A | | SN74ABTH182646A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | 5 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | 8 | | | | | | pF |

† All typical values are at $V_{CC}$ = 5 V.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 15)

| | | | SN54ABTH182646A | | SN74ABTH182646A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | 3 | | 3 | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | 3 | | 3 | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | 0.5 | | 0.5 | | ns |

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 15)

| | | | SN54ABTH182646A | | SN74ABTH182646A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 8 | | 8 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, DIR, $\overline{OE}$, or S before TCK↑ | 6 | | 6 | | ns |
| | | TDI before TCK↑ | 4.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3 | | 3 | | |
| $t_h$ | Hold time | A, B, CLK, DIR, $\overline{OE}$, or S after TCK↑ | 1.5 | | 1.5 | | ns |
| | | TDI after TCK↑ | 1 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | µs |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 15)

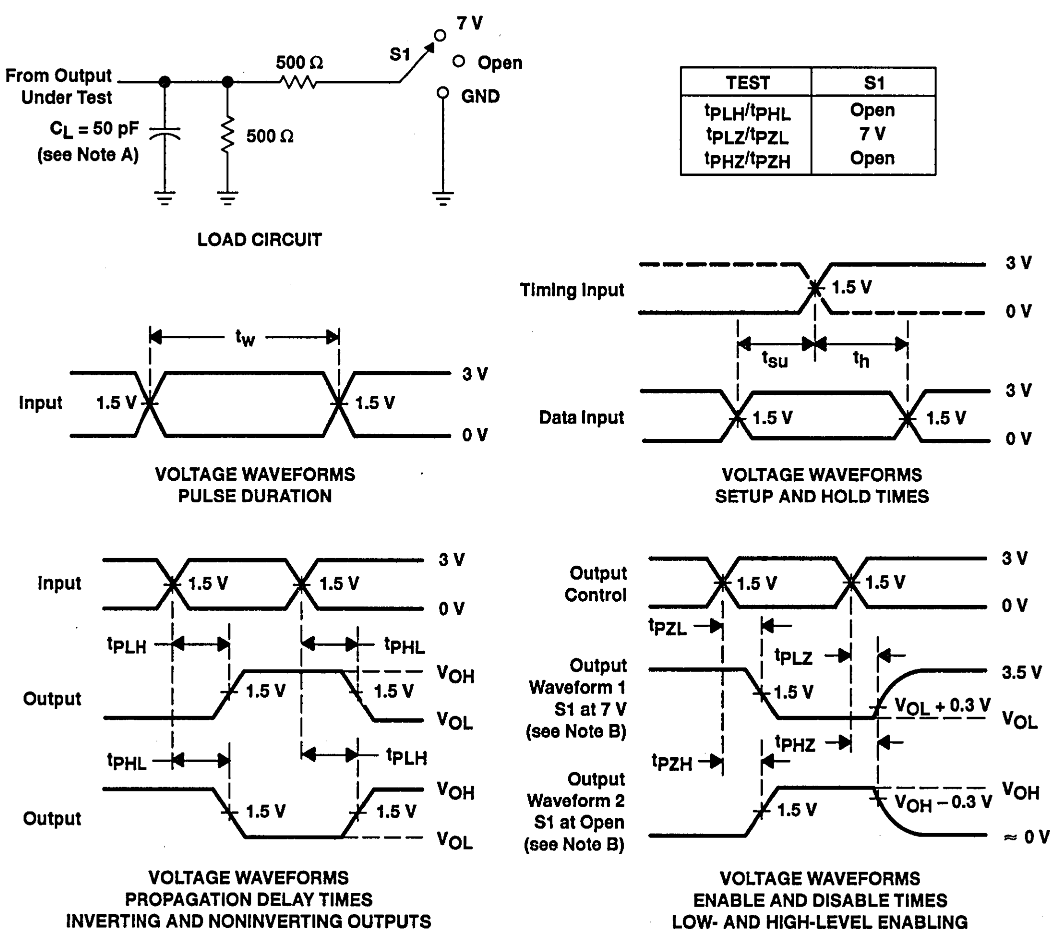
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH182646A | | SN74ABTH182646A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 150 | | 100 | | 100 | | MHz |
| $t_{PLH}$ | A | B | 1.5 | 3.5 | 5.1 | 1.5 | 5.8 | 1.5 | 5.3 | ns |
| $t_{PHL}$ | | | 1.5 | 4.1 | 5.8 | 1.5 | 6.4 | 1.5 | 6.1 | |
| $t_{PLH}$ | B | A | 1.5 | 3.1 | 4.7 | 1.5 | 5.2 | 1.5 | 5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.3 | 5 | 1.5 | 5.6 | 1.5 | 5.4 | |
| $t_{PLH}$ | CLKAB | B | 1.5 | 4.3 | 6.2 | 1.5 | 7 | 1.5 | 6.5 | ns |
| $t_{PHL}$ | | | 1.5 | 4.9 | 7 | 1.5 | 8.1 | 1.5 | 7.4 | |
| $t_{PLH}$ | CLKBA | A | 1.5 | 3.6 | 5.2 | 1.5 | 6.2 | 1.5 | 5.9 | ns |
| $t_{PHL}$ | | | 1.5 | 3.8 | 5.5 | 1.5 | 6.5 | 1.5 | 6.1 | |
| $t_{PLH}$ | SAB | B | 1.5 | 4.4 | 6.9 | 1.5 | 7.6 | 1.5 | 7.2 | ns |
| $t_{PHL}$ | | | 1.5 | 4.8 | 7.4 | 1.5 | 8.3 | 1.5 | 7.8 | |
| $t_{PLH}$ | SBA | A | 1.5 | 3.8 | 5.6 | 1.5 | 6.8 | 1.5 | 6.6 | ns |
| $t_{PHL}$ | | | 1.5 | 3.9 | 6 | 1.5 | 7.2 | 1.5 | 6.8 | |
| $t_{PZH}$ | DIR | B or A | 1.5 | 3.9 | 6.3 | 1.5 | 7.5 | 1.5 | 7 | ns |
| $t_{PZL}$ | | | 1.5 | 4 | 6.5 | 1.5 | 7.7 | 1.5 | 7.2 | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | 1.5 | 4.2 | 6.7 | 1.5 | 8.1 | 1.5 | 7.4 | ns |
| $t_{PZL}$ | | | 1.5 | 4.3 | 6.9 | 1.5 | 8.4 | 1.5 | 7.6 | |
| $t_{PHZ}$ | DIR | B or A | 2 | 5.9 | 8.8 | 2 | 10.3 | 2 | 10 | ns |
| $t_{PLZ}$ | | | 2 | 4.7 | 6.9 | 2 | 8.7 | 2 | 8.1 | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | 2 | 6 | 9 | 2 | 10.5 | 2 | 9.7 | ns |
| $t_{PLZ}$ | | | 2 | 4.8 | 7.1 | 2 | 8.7 | 2 | 7.6 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH182646A | | SN74ABTH182646A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 6.1 | 11 | 2.5 | 14.5 | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | 2.5 | 6.5 | 10.8 | 2.5 | 14 | 2.5 | 12.4 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.6 | 5.1 | 2 | 7 | 2 | 5.6 | ns |
| $t_{PHL}$ | | | 2 | 3.7 | 5.1 | 2 | 7 | 2 | 5.6 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 7.1 | 11.5 | 4 | 14.5 | 4 | 13.4 | ns |
| $t_{PZL}$ | | | 4 | 7.2 | 11.8 | 4 | 15 | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.7 | 5.7 | 2 | 7.5 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2 | 3.9 | 6.2 | 2 | 8 | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 8.5 | 13 | 4 | 18 | 4 | 15 | ns |
| $t_{PLZ}$ | | | 3 | 7.2 | 13.3 | 3 | 17.5 | 3 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5.1 | 6.8 | 3 | 8 | 3 | 7.2 | ns |
| $t_{PLZ}$ | | | 2.5 | 4 | 5.5 | 2.5 | 8 | 2.5 | 6.3 | |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## PARAMETER MEASUREMENT INFORMATION



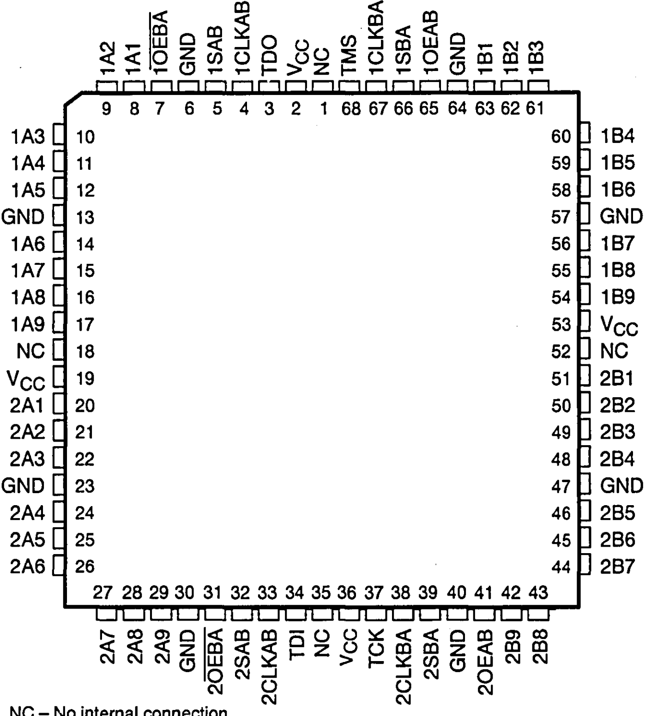

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 15. Load Circuit and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- B-Port Outputs of ’ABTH182652A Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC*-II*B*™ BiCMOS Design
- One Boundary-Scan Cell Per I/O Architecture Improves Scan Efficiency
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54ABTH18652A, SN54ABTH182652A . . . HV PACKAGE
(TOP VIEW)




NC – No internal connection

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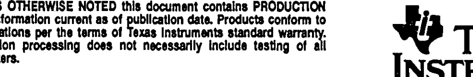
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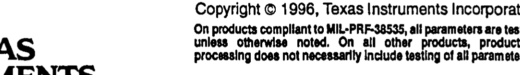
TEXAS INSTRUMENTS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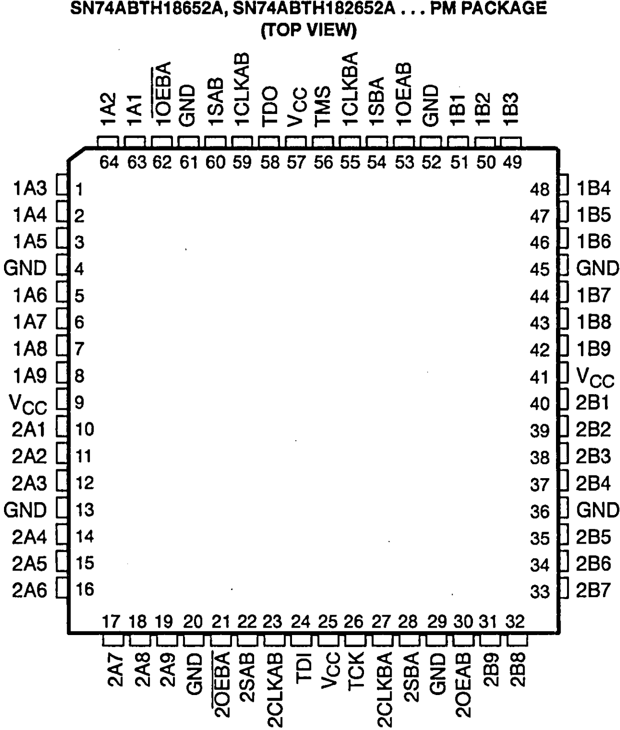
**SN74ABTH18652A, SN74ABTH182652A . . . PM PACKAGE**
**(TOP VIEW)**




## description

The 'ABTH18652A and 'ABTH182652A scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B data flow, but uses CLKBA, SBA, and $\overline{\text{OEBA}}$ inputs. Since the $\overline{\text{OEBA}}$ input is active-low, the A outputs are active when $\overline{\text{OEBA}}$ is low and are in the high-impedance state when $\overline{\text{OEBA}}$ is high. Figure 1 illustrates the four fundamental bus-management functions that are performed with the 'ABTH18652A and 'ABTH182652A.

## description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Improved scan efficiency is accomplished through the adoption of a one boundary-scan cell (BSC) per I/O pin architecture. This architecture is implemented in such a way as to capture the most pertinent test data. A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The B-port outputs of 'ABTH182652A, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54ABTH18652A and SN54ABTH182652A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABTH18652A and SN74ABTH182652A are characterized for operation from −40°C to 85°C.

**FUNCTION TABLE**
**(normal mode, each 9-bit section)**

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA | A1 – A9 | B1 – B9 | |
| L | H | L | L | X | X | Input disabled | Input disabled | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | L | X | X | Input | Unspecified† | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | L | ↑ | X | X | Unspecified† | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | X | X | H | Output | Input | Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | X | X | H | X | Input | Output | Stored A data to B bus |
| H | L | X | X | H | H | Output | Output | Stored A data to B bus and stored B data to A bus |

† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or $\overline{OEBA}$. Data-input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered to load both registers.

BUS A BUS B

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER BUS B TO BUS A**

BUS A BUS B

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | H | X | X | L | X |

**REAL-TIME TRANSFER BUS A TO BUS B**

BUS A BUS B

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**STORAGE FROM A, B, OR A AND B**

BUS A BUS B

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | L | X | X | H | H |

**TRANSFER STORED DATA TO A AND/OR B**

**Figure 1. Bus-Management Functions**

## functional block diagram

Boundary-Scan Register

1OEAB 53
$V_{CC}$ GND
1$\overline{OEBA}$ 62
1CLKBA 55
1SBA 54
1CLKAB 59
1SAB 60
C1
1D
1A1 63
51 1B1
One of Nine Channels

2OEAB 30
$V_{CC}$ GND
2$\overline{OEBA}$ 21
2CLKBA 27
2SBA 28
2CLKAB 23
2SAB 22
2A1 10
40 2B1
One of Nine Channels

Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller
$V_{CC}$
TDI 24
$V_{CC}$
TMS 56
TCK 26
58 TDO

Pin numbers shown are for the PM package.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| GND | Ground |
| 1OEAB, 2OEAB | Normal-function active-high output enables. See function table for normal-mode logic. An internal pulldown at each terminal forces the terminal to a high level if left unconnected. |
| $1\overline{OEBA}$, $2\overline{OEBA}$ | Normal-function active-low output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| 1SAB, 1SBA, 2SAB, 2SBA | Normal-function select controls. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 2 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test-data registers: a 48-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

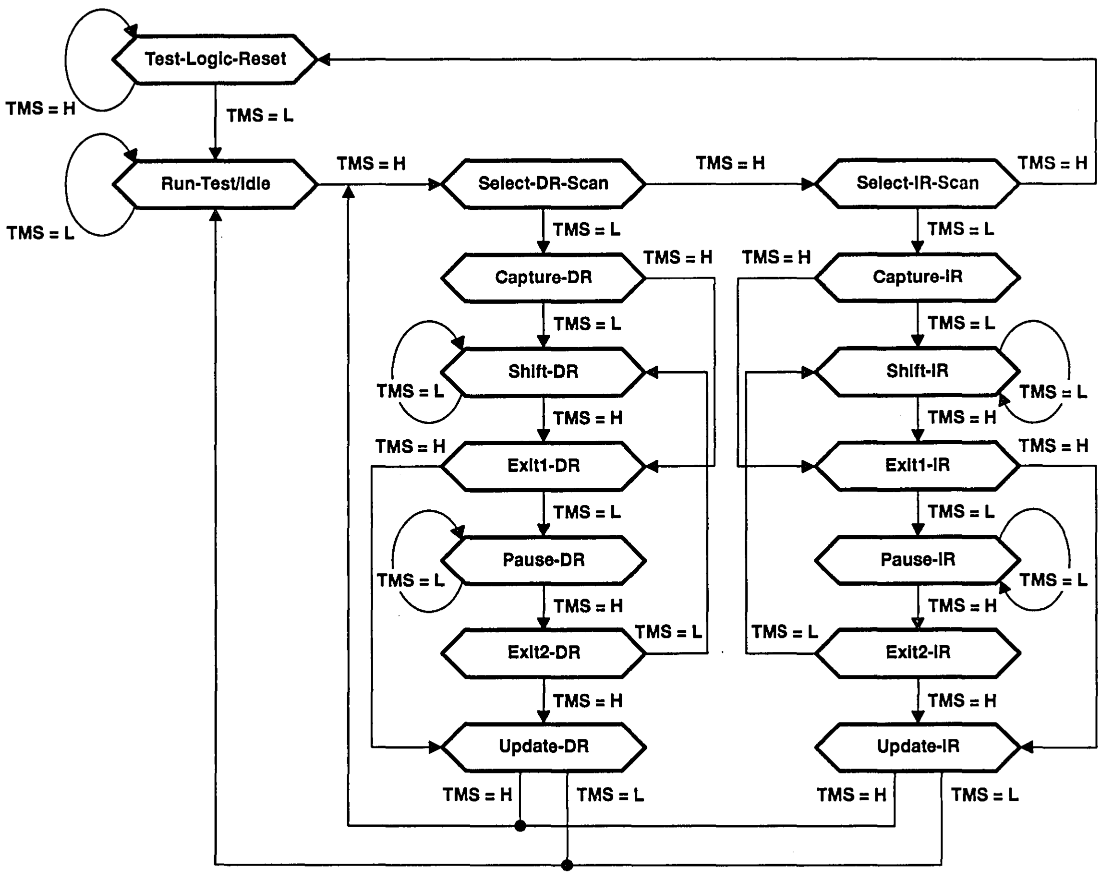



**Figure 2. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 2 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABTH18652A and 'ABTH182652A, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–46 in the boundary-scan register are reset to logic 0 while bits 45–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

### Shift-DR (continued)

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'ABTH18652A and 'ABTH182652A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABTH18652A and 'ABTH182652A. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected to verify that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 3.

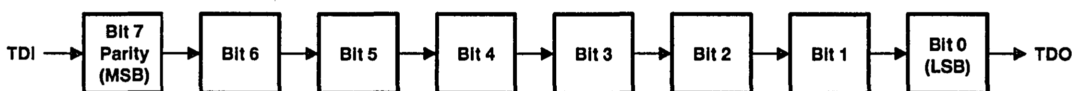



**Figure 3. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–46 are reset to logic 0, while BSCs 45–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | 2OEAB | 35 | 2A9-I/O | 17 | 2B9-I/O |
| 46 | 1OEAB | 34 | 2A8-I/O | 16 | 2B8-I/O |
| 45 | 2$\overline{\text{OEBA}}$ | 33 | 2A7-I/O | 15 | 2B7-I/O |
| 44 | 1$\overline{\text{OEBA}}$ | 32 | 2A6-I/O | 14 | 2B6-I/O |
| 43 | 2CLKAB | 31 | 2A5-I/O | 13 | 2B5-I/O |
| 42 | 1CLKAB | 30 | 2A4-I/O | 12 | 2B4-I/O |
| 41 | 2CLKBA | 29 | 2A3-I/O | 11 | 2B3-I/O |
| 40 | 1CLKBA | 28 | 2A2-I/O | 10 | 2B2-I/O |
| 39 | 2SAB | 27 | 2A1-I/O | 9 | 2B1-I/O |
| 38 | 1SAB | 26 | 1A9-I/O | 8 | 1B9-I/O |
| 37 | 2SBA | 25 | 1A8-I/O | 7 | 1B8-I/O |
| 36 | 1SBA | 24 | 1A7-I/O | 6 | 1B7-I/O |
| — | — | 23 | 1A6-I/O | 5 | 1B6-I/O |
| — | — | 22 | 1A5-I/O | 4 | 1B5-I/O |
| — | — | 21 | 1A4-I/O | 3 | 1B4-I/O |
| — | — | 20 | 1A3-I/O | 2 | 1B3-I/O |
| — | — | 19 | 1A2-I/O | 1 | 1B2-I/O |
| — | — | 18 | 1A1-I/O | 0 | 1B1-I/O |

### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run test (RUNT) instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 4.

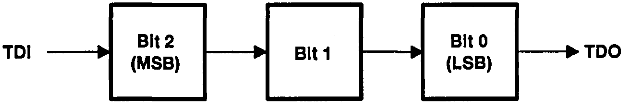



**Figure 4. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 5.

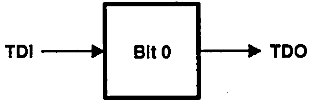



**Figure 5. Bypass Register Order of Scan**

### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'ABTH18652A, the binary value 00000000000000101010000000101111 (0002A02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74ABTH18652A.

For the 'ABTH182652A, the binary value 00000000000000101110000000101111 (0002E02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74ABTH182652A.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary-run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABTH18652A or 'ABTH182652A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–44 of the BSR). When a given output enable is active (logic 0 for $\overline{\text{OEBA}}$, logic 1 for OEAB), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a RUNT operation to specify which test operation is to be executed.

## boundary-control register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 47–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 47–44 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when both bytes of the device are operating in one direction of data flow (that is, 1OEAB = 1$\overline{\text{OEBA}}$ and 2OEAB = 2$\overline{\text{OEBA}}$) and in the same direction of data flow (that is, 1OEAB = 2OEAB and 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

**pseudo-random pattern generation (PRPG)**

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 6 and 7 illustrate the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

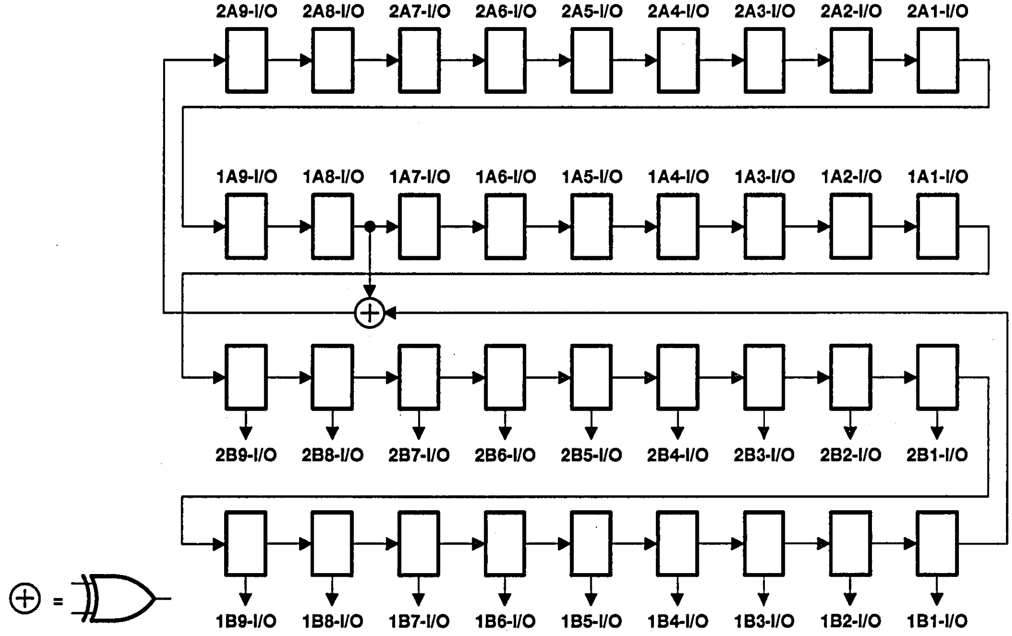



**Figure 6. 36-Bit PRPG Configuration (1OEAB = 2OEAB = 1, $\overline{1OEBA}$ = $\overline{2OEBA}$ = 1)**

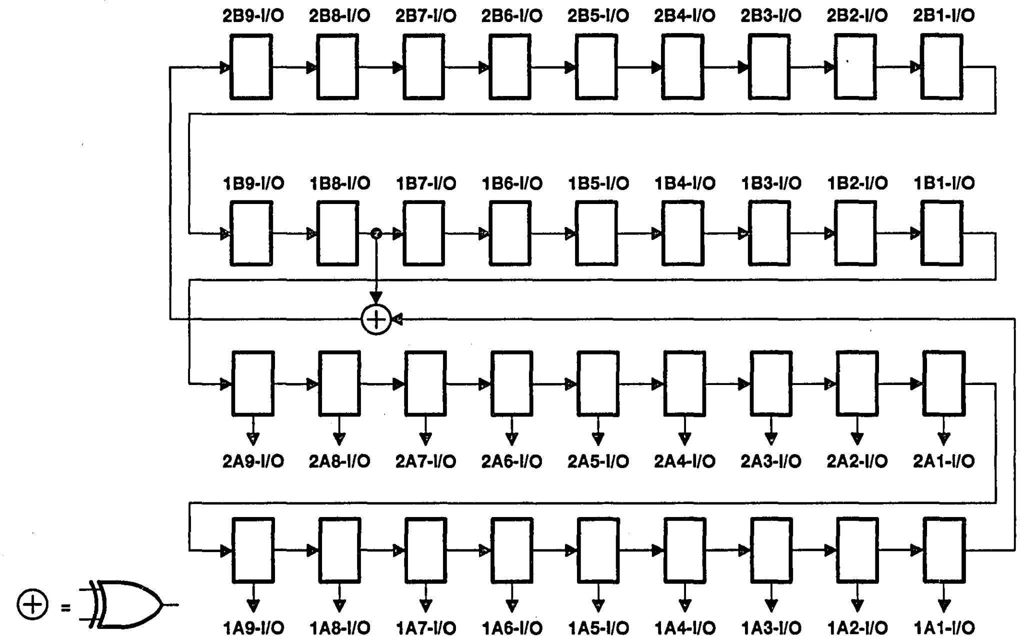



**Figure 7. 36-Bit PRPG Configuration (1OEAB = 2OEAB = 0, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 0)**

### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 8 and 9 illustrate the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

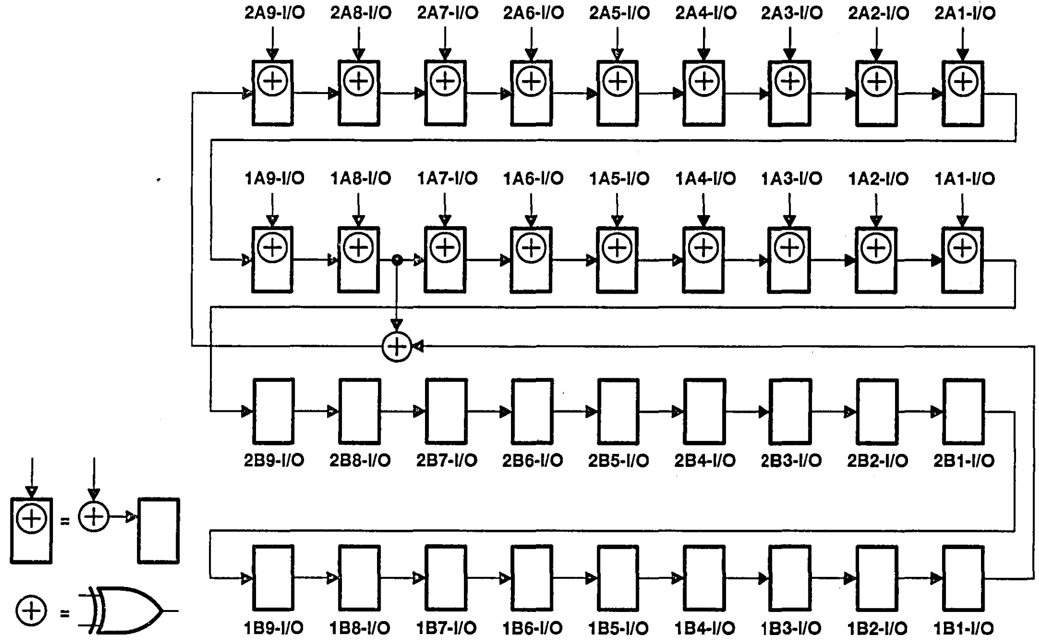



**Figure 8. 36-Bit PSA Configuration (1OEAB = 2OEAB = 1, $\overline{1OEBA}$ = $\overline{2OEBA}$ = 1)**

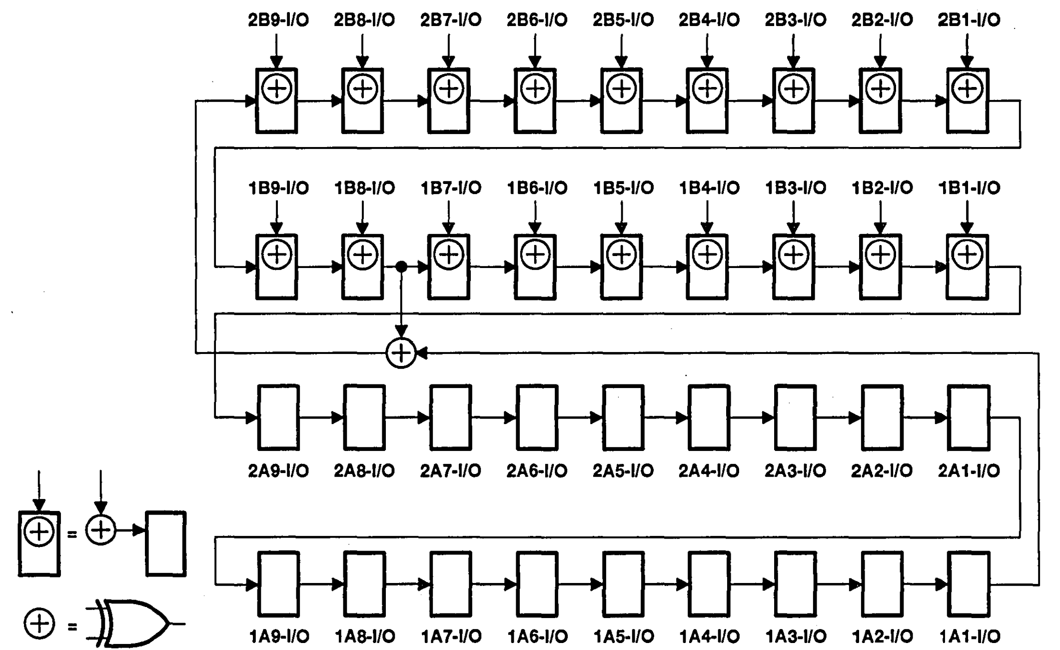



**Figure 9. 36-Bit PSA Configuration (1OEAB = 2OEAB = 0, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 0)**

## simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 10 and 11 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

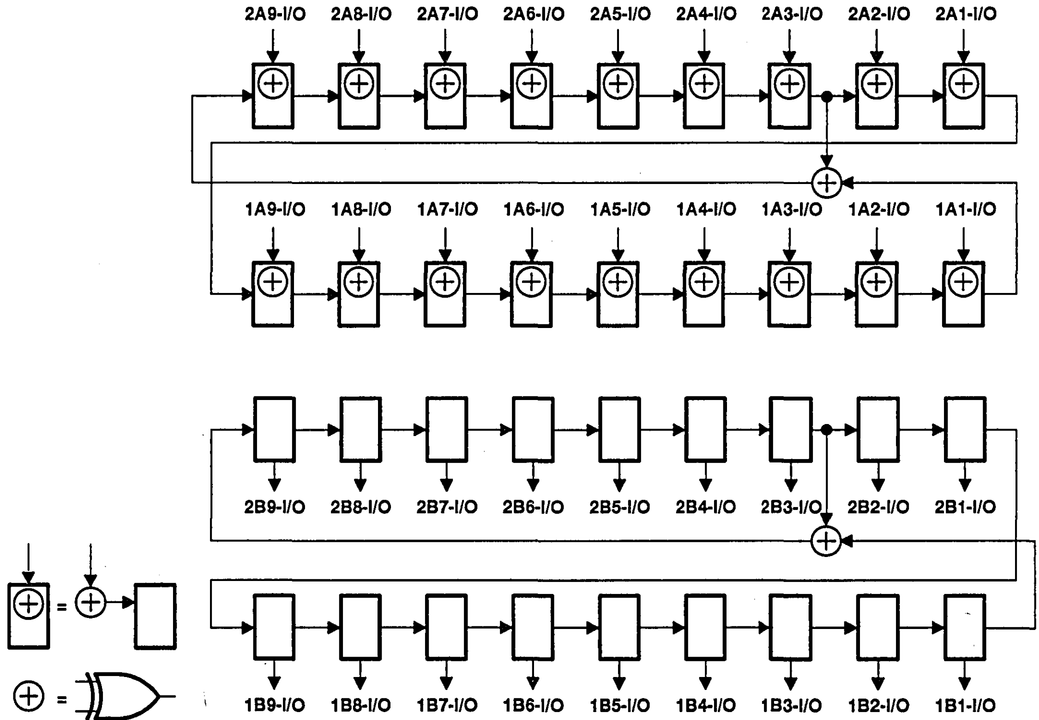



**Figure 10. 18-Bit PSA/PRPG Configuration (1OEAB = 2OEAB = 1, $\overline{1OEBA}$ = $\overline{2OEBA}$ = 1)**

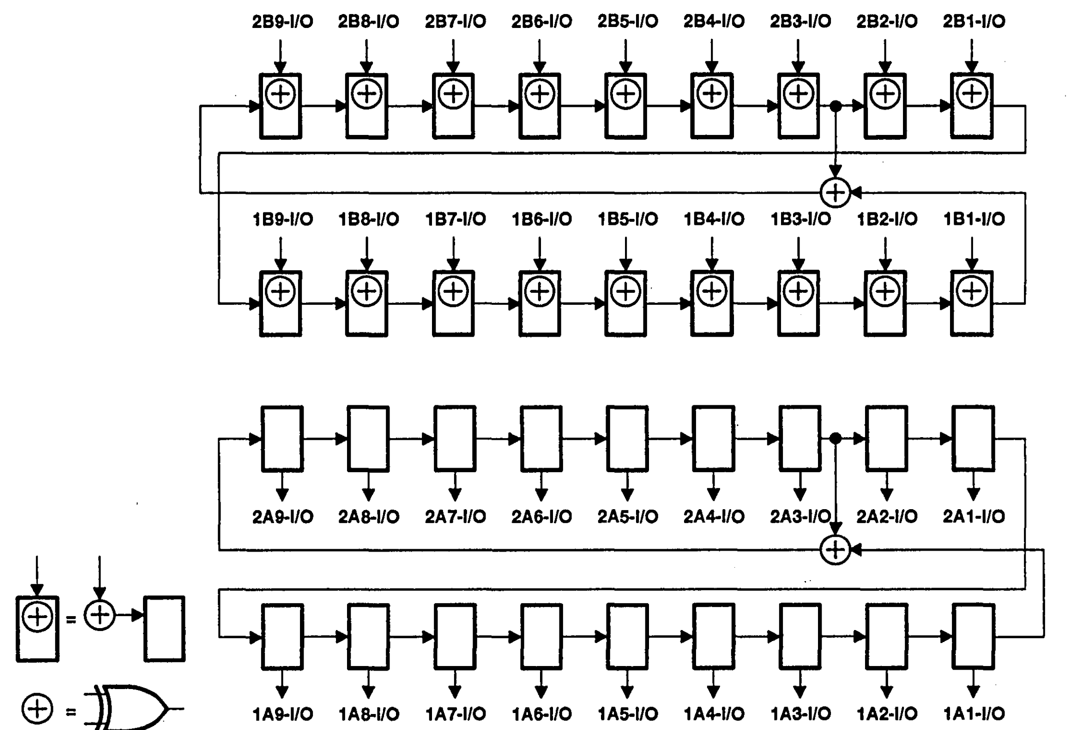



**Figure 11. 18-Bit PSA/PRPG Configuration (1OEAB = 2OEAB = 0, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 12 and 13 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

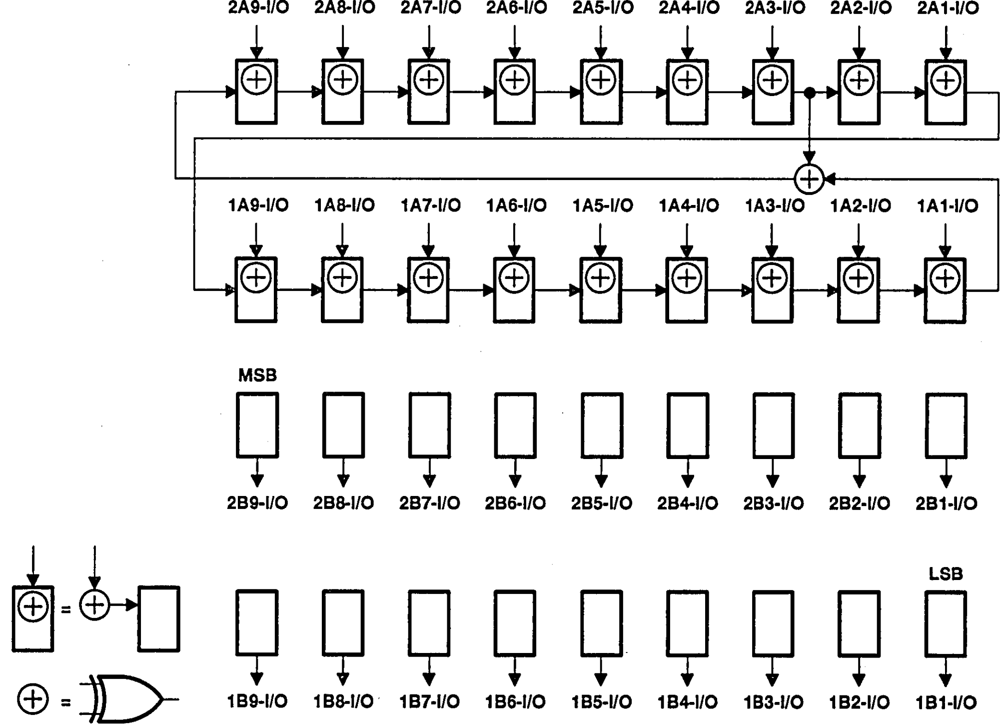



**Figure 12. 18-Bit PSA/COUNT Configuration (1OEAB = 2OEAB = 1, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 1)**

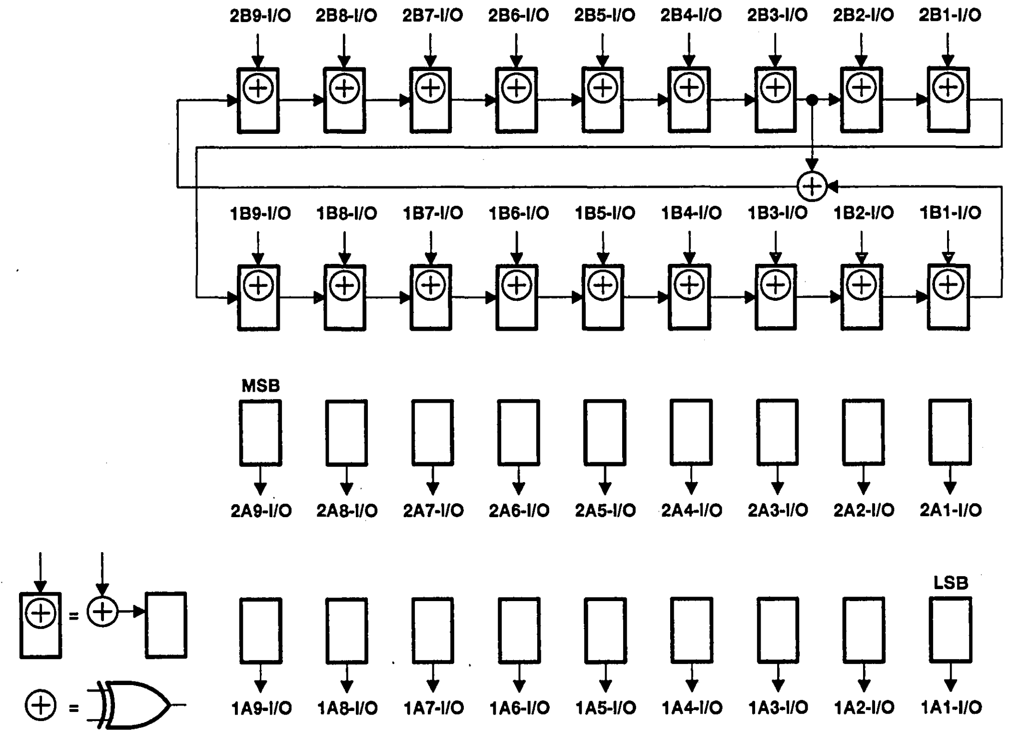



**Figure 13. 18-Bit PSA/COUNT Configuration (1OEAB = 2OEAB = 0, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 0)**

## timing description

All test operations of the 'ABTH18652A and 'ABTH182652A are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 2) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 14. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | The selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

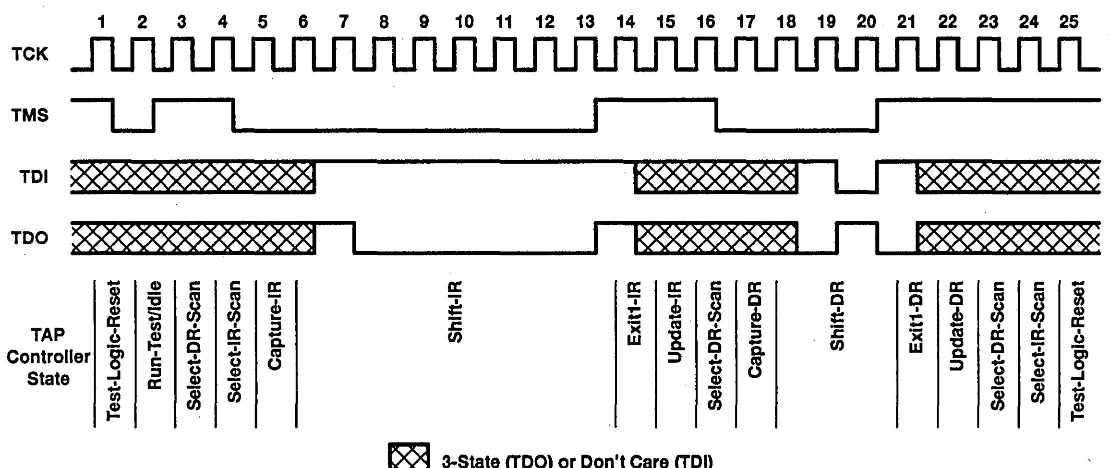



**Figure 14. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Parameter | | Value |
|---|---|---|
| Supply voltage range, $V_{CC}$ | | –0.5 V to 7 V |
| Input voltage range, $V_I$: | except I/O ports (see Note 1) | –0.5 V to 7 V |
| | I/O ports (see Note 1) | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ | | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$: | SN54ABTH18652A | 96 mA |
| | SN54ABTH182652A (A port or TDO) | 96 mA |
| | SN54ABTH182652A (B port) | 30 mA |
| | SN74ABTH18652A | 128 mA |
| | SN74ABTH182652A (A port or TDO) | 128 mA |
| | SN74ABTH182652A (B port) | 30 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | | –18 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | | –50 mA |
| Maximum package power dissipation at $T_A$ = 55°C (in still air) (see Note 2): | PM package | 1 W |
| Storage temperature range, $T_{stg}$ | | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | −24 | | −32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | −55 | 125 | −40 | 85 | °C |

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, $I_I$ = –18 mA | | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, $I_{OH}$ = – 3 mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, $I_{OH}$ = – 3 mA | | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V, $I_{OH}$ = – 24 mA | | 2 | | | 2 | | | | |
| | | $V_{CC}$ = 4.5 V, $I_{OH}$ = – 32 mA | | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| $I_I$ | CLK, S, TCK | $V_{CC}$ = 0 to 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±20 | | ±20 | | ±20 | |
| $I_{IH}$ | OEAB | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ | | 40 | | 150 | 40 | 150 | 40 | 150 | µA |
| | $\overline{OEBA}$, TDI, TMS | | | | | 10 | | 10 | | 10 | |
| $I_{IL}$ | OEAB | $V_{CC}$ = 5.5 V, $V_I$ = GND | | | | –10 | | –10 | | –10 | µA |
| | $\overline{OEBA}$, TDI, TMS | | | –40 | | –150 | –40 | –150 | –40 | –150 | |
| $I_{I(hold)}$‡ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 75 | 220 | 500 | | | 75 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | –180 | –500 | | | –75 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 2.7 V, OE = 0.8 V, $\overline{OE}$ = 2 V | | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 0.5 V, OE = 0.8 V, $\overline{OE}$ = 2 V | | | | –10 | | –10 | | –10 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 2.7 V or 0.5 V, OE = 2 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, OE = 2 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, $V_I$ or $V_O$ ≤ 4.5 V | | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, $V_O$ = 5.5 V | | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, $V_O$ = 2.5 V | | –50 | –110 | –200 | –50 | –200 | –50 | –200 | mA |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | | 1.8 | 2.2 | | 2.2 | | 2.2 | mA |
| | Outputs low | | | | 20 | 24 | | 24 | | 24 | |
| | Outputs disabled | | | | 1.1 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |

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* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS | $T_A$ = 25°C | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | 5 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | 8 | | | | | | pF |

† All typical values are at $V_{CC}$ = 5 V.

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## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 15)

| | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | 3 | | 3 | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | 3 | | 3 | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | 0.5 | | 0.5 | | ns |

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## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 15)

| | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 8 | | 8 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, OEAB, $\overline{OEBA}$, or S before TCK↑ | 6 | | 6 | | ns |
| | | TDI before TCK↑ | 4.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3 | | 3 | | |
| $t_h$ | Hold time | A, B, CLK, OEAB, $\overline{OEBA}$, or S after TCK↑ | 1.5 | | 1.5 | | ns |
| | | TDI after TCK↑ | 1 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | µs |

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## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 150 | | 100 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | 1.5 | 2.6 | 4.7 | 1.5 | 5.2 | 1.5 | 5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.2 | 5 | 1.5 | 5.6 | 1.5 | 5.4 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 1.5 | 3.1 | 5.2 | 1.5 | 6.2 | 1.5 | 5.9 | ns |
| $t_{PHL}$ | | | 1.5 | 3.7 | 5.5 | 1.5 | 6.5 | 1.5 | 6.1 | |
| $t_{PLH}$ | SAB or SBA | B or A | 1.5 | 3.8 | 5.6 | 1.5 | 6.8 | 1.5 | 6.6 | ns |
| $t_{PHL}$ | | | 1.5 | 3.8 | 6 | 1.5 | 7.2 | 1.5 | 6.8 | |
| $t_{PZH}$ | OEAB or $\overline{OEBA}$ | B or A | 1.5 | 3.8 | 5.7 | 1.5 | 7 | 1.5 | 6.6 | ns |
| $t_{PZL}$ | | | 1.5 | 3.9 | 5.8 | 1.5 | 7 | 1.5 | 6.6 | |
| $t_{PHZ}$ | OEAB or $\overline{OEBA}$ | B or A | 2 | 5.3 | 8.2 | 2 | 9.8 | 2 | 9.3 | ns |
| $t_{PLZ}$ | | | 2 | 4 | 6.3 | 2 | 8 | 2 | 7.2 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 6 | 11 | 2.5 | 14.5 | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | 2.5 | 6.3 | 10.8 | 2.5 | 14 | 2.5 | 12.4 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.5 | 5.1 | 2 | 7 | 2 | 5.6 | ns |
| $t_{PHL}$ | | | 2 | 3.6 | 5.1 | 2 | 7 | 2 | 5.6 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 7.2 | 11.5 | 4 | 14.5 | 4 | 13.4 | ns |
| $t_{PZL}$ | | | 4 | 7.2 | 11.8 | 4 | 15 | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.6 | 5.7 | 2 | 7.5 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2 | 3.8 | 6.2 | 2 | 8 | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 7.5 | 13 | 4 | 18 | 4 | 15 | ns |
| $t_{PLZ}$ | | | 3 | 6.5 | 13.3 | 3 | 17.5 | 3 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5 | 6.8 | 3 | 8 | 3 | 7.2 | ns |
| $t_{PLZ}$ | | | 2.5 | 3.9 | 5.5 | 2.5 | 8 | 2.5 | 6.3 | |

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## recommended operating conditions

| | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| | | B port | | 12 | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

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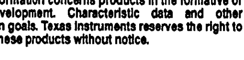
## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | A port, TDO | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = – 3 mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 24 mA | 2 | | | 2 | | | | |
| | | | $I_{OH}$ = – 32 mA | 2* | | | | | 2 | | |
| | B port | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 1 mA | 3.35 | | | 3.3 | | 3.35 | | |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = – 1 mA | 3.85 | | | 3.8 | | 3.85 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 3 mA | 3.1 | | | 3 | | 3.1 | | |
| | | | $I_{OH}$ = – 12 mA | 2.6* | | | | | 2.6 | | |
| $V_{OL}$ | A port, TDO | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | | 0.55* | | | | 0.55 | |
| | B port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 8 mA | | | 0.8 | | 0.8 | | 0.65 | |
| | | | $I_{OL}$ = 12 mA | | | 0.8* | | | | 0.8 | |
| $I_I$ | CLK, S, TCK | $V_{CC}$ = 0 to 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±20 | | ±20 | | ±20 | |
| $I_{IH}$ | OEAB | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ | | 40 | | 150 | 40 | 150 | 40 | 150 | µA |
| | $\overline{OEBA}$, TDI, TMS | | | | | 10 | | 10 | | 10 | |
| $I_{IL}$ | OEAB | $V_{CC}$ = 5.5 V, $V_I$ = GND | | | | –10 | | –10 | | –10 | µA |
| | $\overline{OEBA}$, TDI, TMS | | | –40 | | –150 | –40 | –150 | –40 | –150 | |
| $I_{I(hold)}$‡ | A or B ports | $V_{CC}$ = 4.5 V | $V_I$ = 0.8 V | 75 | 220 | 500 | | | 75 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | –180 | –500 | | | –75 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 2.7 V, OE = 0.8 V, $\overline{OE}$ = 2 V | | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 2.1 V to 5.5 V, $V_O$ = 0.5 V, OE = 0.8 V, $\overline{OE}$ = 2 V | | | | –10 | | –10 | | –10 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 2.7 V or 0.5 V, OE = 2 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, OE = 2 V, $\overline{OE}$ = 0.8 V | | | | ±50 | | | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \le$ 4.5 V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, $V_O$ = 5.5 V | | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | A port, TDO | $V_{CC}$ = 5.5 V, $V_O$ = 2.5 V | | –50 | –110 | –200 | –50 | –200 | –50 | –200 | mA |
| | B port | $V_{CC}$ = 5.5 V, $V_O$ = 2.5 V | | –25 | –55 | –100 | –25 | –100 | –25 | –100 | |

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | A or B ports | | 1.8 | 2.2 | | 2.2 | | 2.2 | mA |
| | Outputs low | | | | 22 | 27 | | 27 | | 27 | |
| | Outputs disabled | | | | 1.1 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$‡ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 5 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | | | | pF |

† All typical values are at $V_{CC}$ = 5 V.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 15)

| | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | 3 | | 3 | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | 3 | | 3 | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | 0.5 | | 0.5 | | ns |

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 15)

| | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 8 | | 8 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, OEAB, $\overline{OEBA}$, or S before TCK↑ | 6 | | 6 | | ns |
| | | TDI before TCK↑ | 4.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3 | | 3 | | |
| $t_h$ | Hold time | A, B, CLK, OEAB, $\overline{OEBA}$, or S after TCK↑ | 1.5 | | 1.5 | | ns |
| | | TDI after TCK↑ | 1 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | µs |

PRODUCT PREVIEW

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## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 150 | | 100 | | 100 | | MHz |
| $t_{PLH}$ | A | B | 1.5 | 3.5 | 5.1 | 1.5 | 5.8 | 1.5 | 5.3 | ns |
| $t_{PHL}$ | | | 1.5 | 4.1 | 5.8 | 1.5 | 6.4 | 1.5 | 6.1 | |
| $t_{PLH}$ | B | A | 1.5 | 3.1 | 4.7 | 1.5 | 5.2 | 1.5 | 5 | ns |
| $t_{PHL}$ | | | 1.5 | 3.3 | 5 | 1.5 | 5.6 | 1.5 | 5.4 | |
| $t_{PLH}$ | CLKAB | B | 1.5 | 4.3 | 6.2 | 1.5 | 7 | 1.5 | 6.5 | ns |
| $t_{PHL}$ | | | 1.5 | 4.9 | 7 | 1.5 | 8.1 | 1.5 | 7.4 | |
| $t_{PLH}$ | CLKBA | A | 1.5 | 3.6 | 5.2 | 1.5 | 6.2 | 1.5 | 5.9 | ns |
| $t_{PHL}$ | | | 1.5 | 3.8 | 5.5 | 1.5 | 6.5 | 1.5 | 6.1 | |
| $t_{PLH}$ | SAB | B | 1.5 | 4.4 | 6.9 | 1.5 | 7.6 | 1.5 | 7.2 | ns |
| $t_{PHL}$ | | | 1.5 | 4.8 | 7.4 | 1.5 | 8.3 | 1.5 | 7.8 | |
| $t_{PLH}$ | SBA | A | 1.5 | 3.8 | 5.6 | 1.5 | 6.8 | 1.5 | 6.6 | ns |
| $t_{PHL}$ | | | 1.5 | 3.9 | 6 | 1.5 | 7.2 | 1.5 | 6.8 | |
| $t_{PZH}$ | OEAB or $\overline{OEBA}$ | B or A | 1.5 | 4.6 | 6.4 | 1.5 | 7.8 | 1.5 | 7.4 | ns |
| $t_{PZL}$ | | | 1.5 | 4.5 | 6.2 | 1.5 | 7.4 | 1.5 | 7 | |
| $t_{PHZ}$ | OEAB or $\overline{OEBA}$ | B or A | 2 | 5.3 | 8.2 | 2 | 9.8 | 2 | 9.3 | ns |
| $t_{PLZ}$ | | | 2 | 4 | 6.3 | 2 | 8 | 2 | 7.2 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 6.8 | 11 | 2.5 | 14.5 | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | 2.5 | 7.4 | 10.8 | 2.5 | 14 | 2.5 | 12.4 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 3.5 | 5.1 | 2 | 7 | 2 | 5.6 | ns |
| $t_{PHL}$ | | | 2 | 3.6 | 5.1 | 2 | 7 | 2 | 5.6 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 8.4 | 11.5 | 4 | 14.5 | 4 | 13.4 | ns |
| $t_{PZL}$ | | | 4 | 8.4 | 11.8 | 4 | 15 | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | 2 | 3.6 | 5.7 | 2 | 7.5 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2 | 3.8 | 6.2 | 2 | 8 | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 7.5 | 13 | 4 | 18 | 4 | 15 | ns |
| $t_{PLZ}$ | | | 3 | 6.5 | 13.3 | 3 | 17.5 | 3 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 5 | 6.8 | 3 | 8 | 3 | 7.2 | ns |
| $t_{PLZ}$ | | | 2.5 | 3.9 | 5.5 | 2.5 | 8 | 2.5 | 6.3 | |

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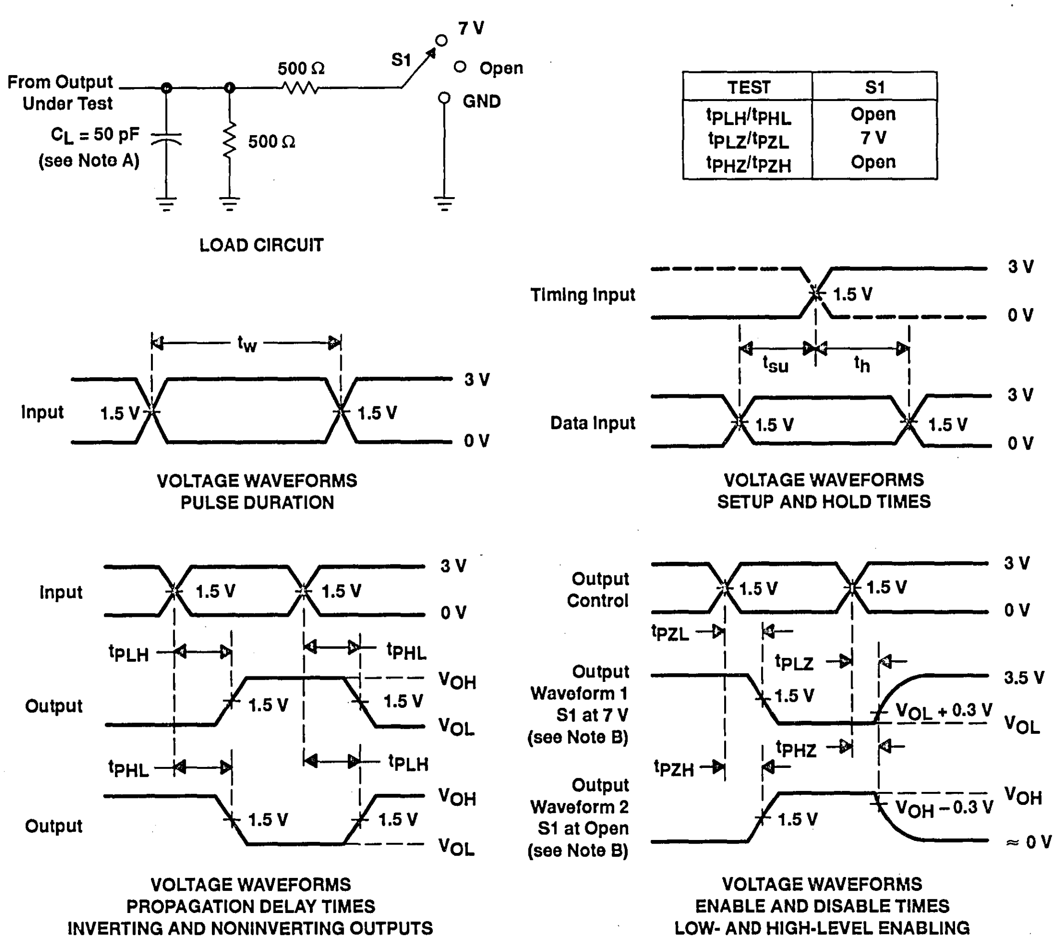
## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 15. Load Circuit and Voltage Waveforms**

General Information 1

SN54/74BCT Octals 2

SN54/74ABT Octals 3

SN54/74ABT Widebus™ With Dual-Sided Terminals 4

SN54/74ABT Widebus™ With Quad-Sided Terminals 5

SN54/74LVT Widebus™ With Dual-Sided Terminals 6

SN54/74LVT Widebus™ With Quad-Sided Terminals 7

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- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)
- Support Unregulated Battery Operation Down to 2.7 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- B-Port Outputs of 'LVTH182245 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages

SN54LVTH18245, SN54LVTH182245 . . . WD PACKAGE
SN74LVTH18245, SN74LVTH182245 . . . DGG OR DL PACKAGE
(TOP VIEW)

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| 1DIR | 1 | 56 | 1$\overline{OE}$ |
| 1B1 | 2 | 55 | 1A1 |
| 1B2 | 3 | 54 | 1A2 |
| GND | 4 | 53 | GND |
| 1B3 | 5 | 52 | 1A3 |
| 1B4 | 6 | 51 | 1A4 |
| $V_{CC}$ | 7 | 50 | $V_{CC}$ |
| 1B5 | 8 | 49 | 1A5 |
| 1B6 | 9 | 48 | 1A6 |
| 1B7 | 10 | 47 | 1A7 |
| GND | 11 | 46 | GND |
| 1B8 | 12 | 45 | 1A8 |
| 1B9 | 13 | 44 | 1A9 |
| 2B1 | 14 | 43 | 2A1 |
| 2B2 | 15 | 42 | 2A2 |
| 2B3 | 16 | 41 | 2A3 |
| 2B4 | 17 | 40 | 2A4 |
| GND | 18 | 39 | GND |
| 2B5 | 19 | 38 | 2A5 |
| 2B6 | 20 | 37 | 2A6 |
| 2B7 | 21 | 36 | 2A7 |
| $V_{CC}$ | 22 | 35 | $V_{CC}$ |
| 2B8 | 23 | 34 | 2A8 |
| 2B9 | 24 | 33 | 2A9 |
| GND | 25 | 32 | GND |
| 2DIR | 26 | 31 | 2$\overline{OE}$ |
| TDO | 27 | 30 | TDI |
| TMS | 28 | 29 | TCK |

PRODUCT PREVIEW

## description

The 'LVTH18245 and 'LVTH182245 scan test devices with 18-bit bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit noninverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

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## description (continued)

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at DIR. The $\overline{OE}$ can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVTH182245, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN74LVTH18245 and SN54LVTH182245 are available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVTH18245 and SN54LVTH182245 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH18245 and SN74LVTH182245 are characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(normal mode, each 9-bit section)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

PRODUCT PREVIEW

## functional block diagram

Boundary-Scan Register
1DIR 1
VCC
1OE 56
1A1 55
2 1B1
One of Nine Channels
2DIR 26
VCC
2OE 31
2A1 43
14 2B1
One of Nine Channels
Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
VCC
TDI 30
VCC
TMS 28
TCK 29
TAP Controller
27 TDO

PRODUCT PREVIEW

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1DIR, 2DIR | Normal-function direction controls. See function table for normal-mode logic. |
| GND | Ground |
| $1\overline{OE}$, $2\overline{OE}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

PRODUCT PREVIEW

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and four test-data registers: a 44-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

**Figure 1. TAP-Controller State Diagram**

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## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'LVTH18245 and 'LVTH182245, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 43–40 in the boundary-scan register are reset to logic 0, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.



### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

**Shift-DR (continued)**

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data register-scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'LVTH18245 and 'LVTH182245, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

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### register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

### instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'LVTH18245 and 'LVTH182245. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

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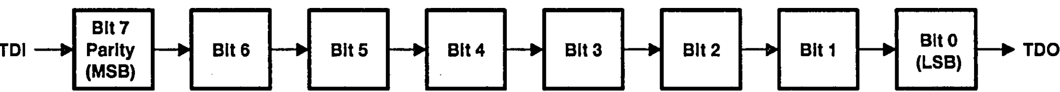


**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 44 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, one BSC for each normal-function I/O pin (one single cell for both input data and output data), and one BSC for each of the internally decoded output-enable signals (1OEA, 2OEA, 1OEB, 2OEB). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle, as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 43–40 are reset to logic 0, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values for other BSCs should be considered indeterminate.

When external data is to be captured, the BSCs for signals 1OEA, 2OEA, 1OEB, and 2OEB capture logic values determined by the following positive-logic equations:

$1OEA = \overline{1OE} \bullet \overline{1DIR}$, $2OEA = \overline{2OE} \bullet \overline{2DIR}$, $1OEB = \overline{1OE} \bullet DIR$, and $2OEB = \overline{2OE} \bullet DIR$

When data is to be applied externally, these BSCs control the drive state (active or high impedance) of their respective outputs.

The BSR order of scan is from TDI through bits 43–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|---|---|---|---|
| 43 | 2OEB | 35 | 2A9-I/O | 26 | 1A9-I/O | 17 | 2B9-I/O | 8 | 1B9-I/O |
| 42 | 1OEB | 34 | 2A8-I/O | 25 | 1A8-I/O | 16 | 2B8-I/O | 7 | 1B8-I/O |
| 41 | 2OEA | 33 | 2A7-I/O | 24 | 1A7-I/O | 15 | 2B7-I/O | 6 | 1B7-I/O |
| 40 | 1OEA | 32 | 2A6-I/O | 23 | 1A6-I/O | 14 | 2B6-I/O | 5 | 1B6-I/O |
| 39 | 2DIR | 31 | 2A5-I/O | 22 | 1A5-I/O | 13 | 2B5-I/O | 4 | 1B5-I/O |
| 38 | 1DIR | 30 | 2A4-I/O | 21 | 1A4-I/O | 12 | 2B4-I/O | 3 | 1B4-I/O |
| 37 | $2\overline{OE}$ | 29 | 2A3-I/O | 20 | 1A3-I/O | 11 | 2B3-I/O | 2 | 1B3-I/O |
| 36 | $1\overline{OE}$ | 28 | 2A2-I/O | 19 | 1A2-I/O | 10 | 2B2-I/O | 1 | 1B2-I/O |
| — | — | 27 | 2A1-I/O | 18 | 1A1-I/O | 9 | 2B1-I/O | 0 | 1B1-I/O |

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### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

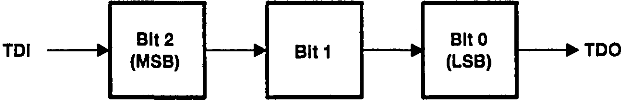


**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

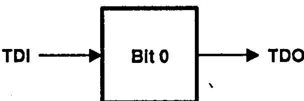


**Figure 4. Bypass Register Order of Scan**

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### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'LVTH18245, the binary value 00000000000000011011000000101111 (0001B02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74LVTH18245.

For the 'LVTH182245, the binary value 00000000000000100000000000101111 (0002002F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74LVTH182245.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

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## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'LVT18245 or 'LVT182245.

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### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device I/O pins is passed through the I/O BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 43–40 of the BSR). When a given output enable is active (logic 1), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

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## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 43–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 43–40 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when both bytes of the device are operating in one direction of data flow (that is, 1OEA ≠ 1OEB and 2OEA ≠ 2OEB) and in the same direction of data flow (that is, 1OEA = 2OEA and 1OEB = 2OEB). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

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### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 illustrate the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

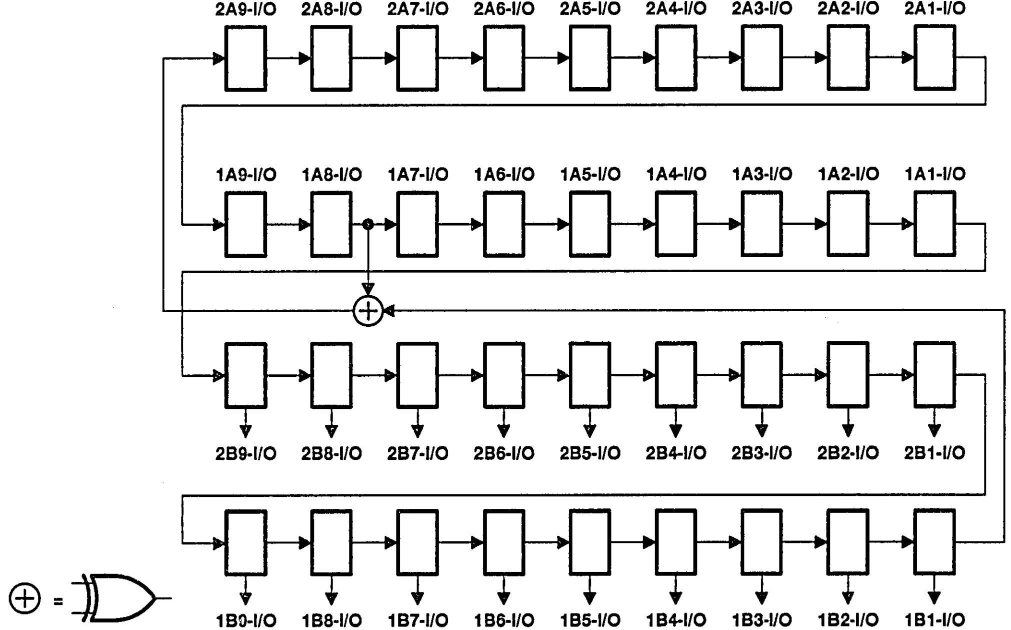


**Figure 5. 36-Bit PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

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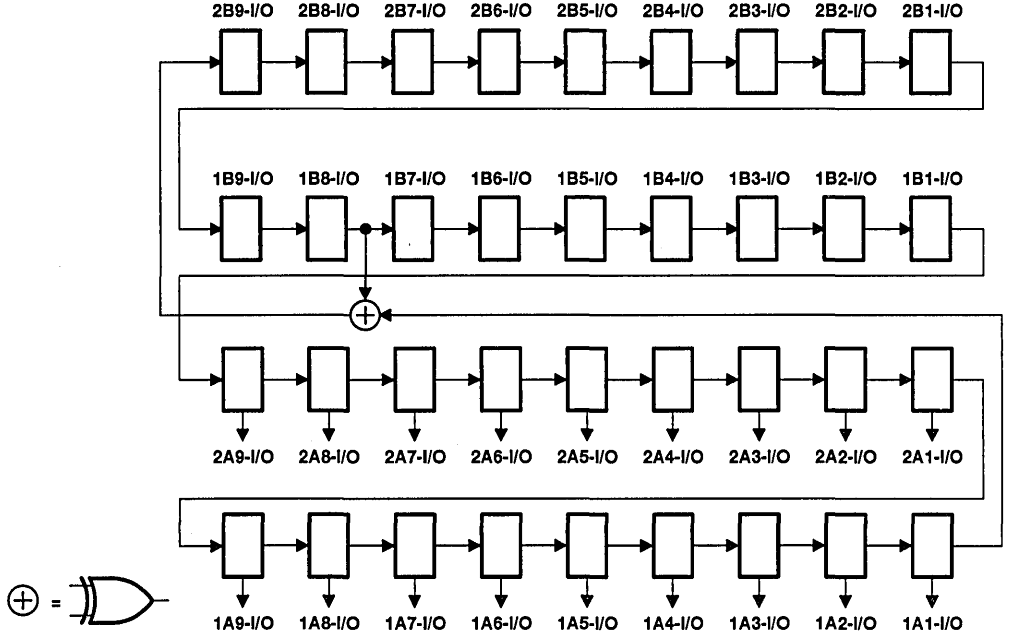


**Figure 6. 36-Bit PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

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### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 illustrate the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

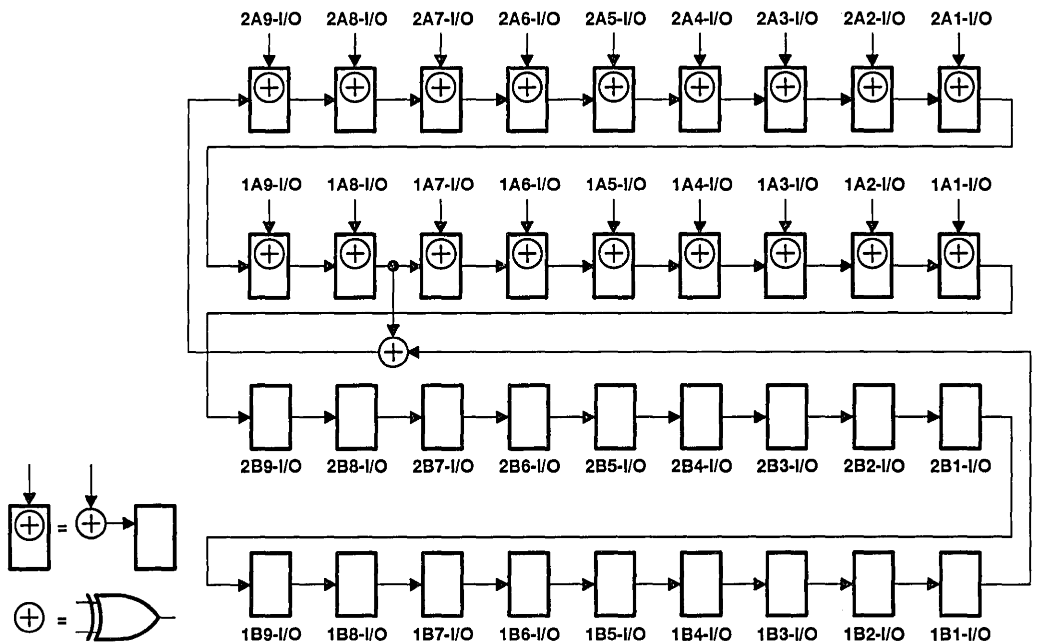


Figure 7. 36-Bit PSA Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)

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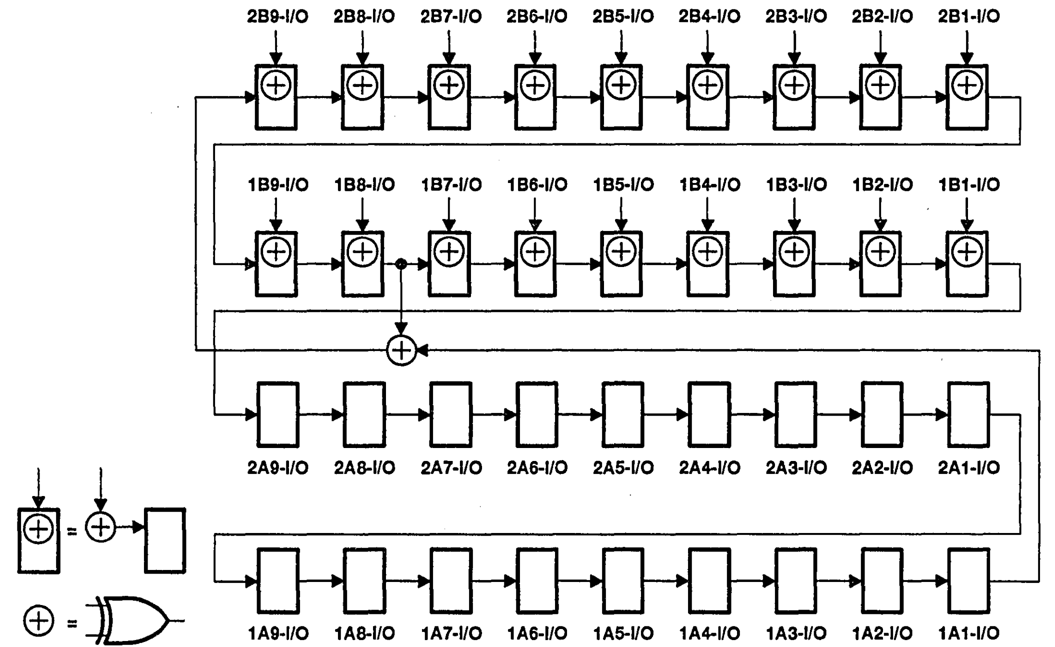


**Figure 8. 36-Bit PSA Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

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**simultaneous PSA and PRPG (PSA/PRPG)**

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

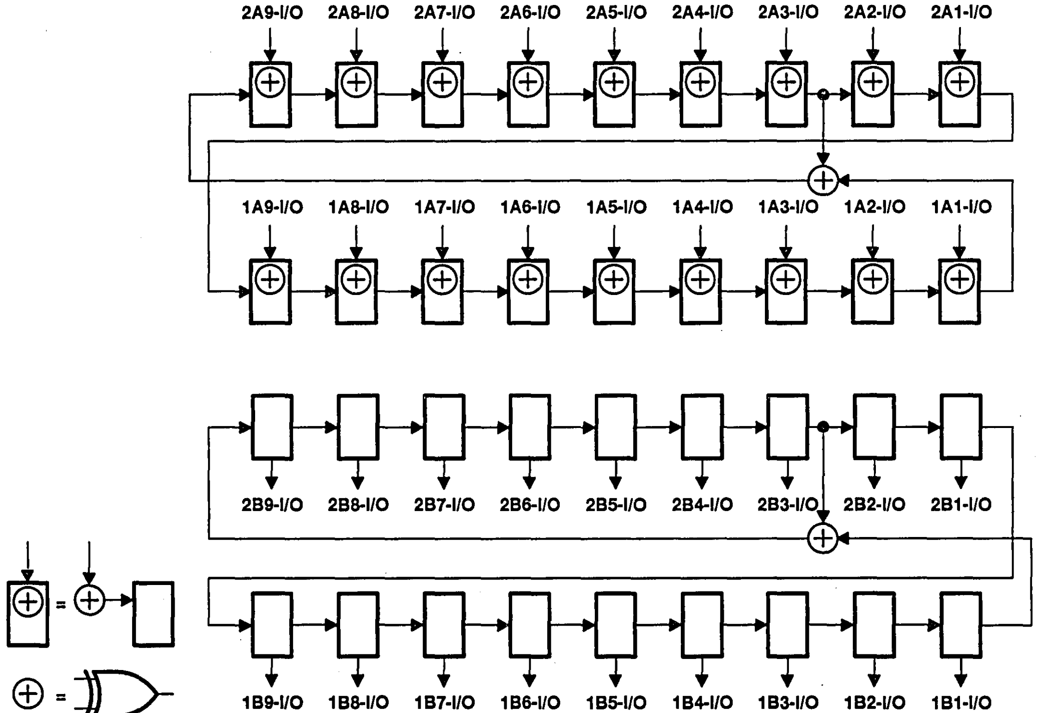


**Figure 9. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

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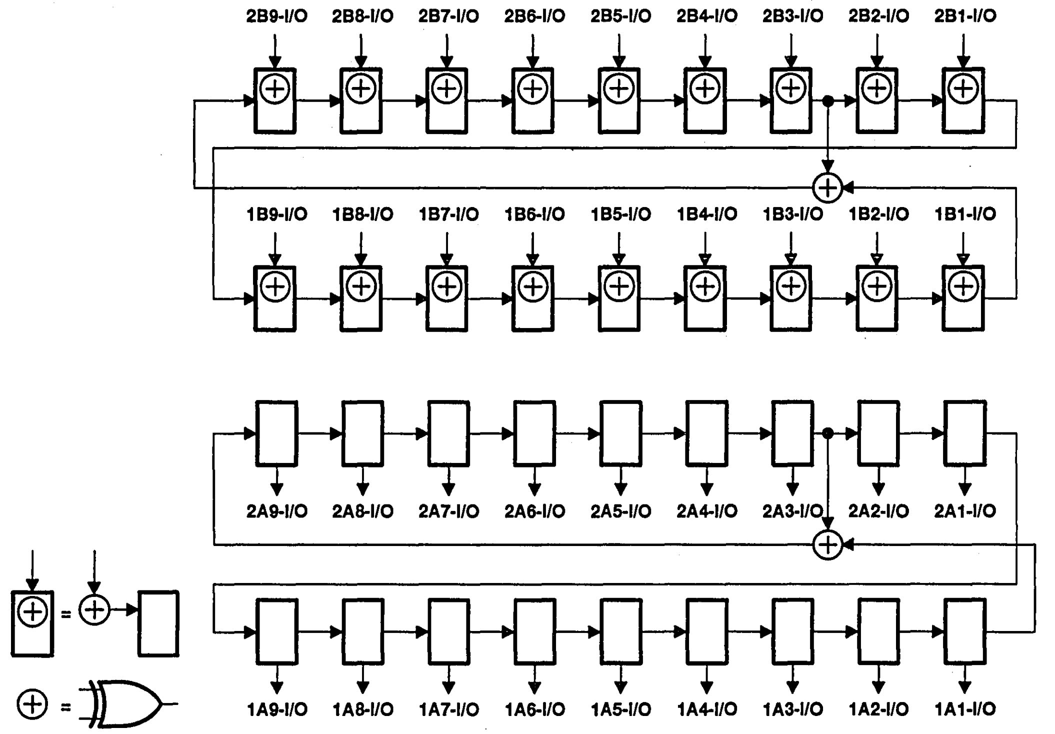


Figure 10. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

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### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

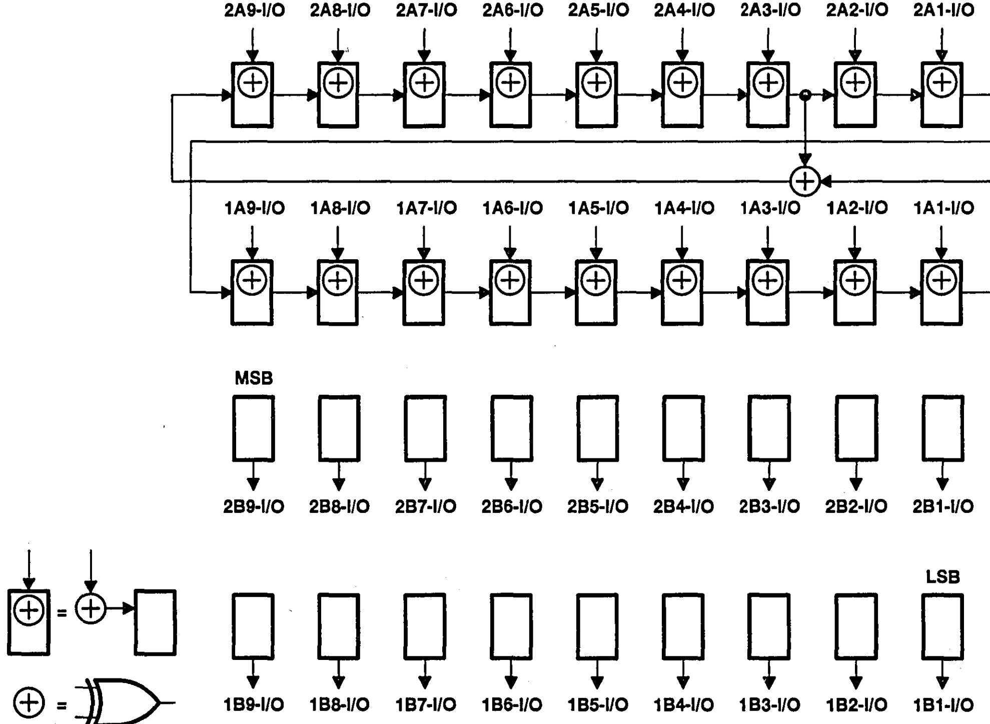


**Figure 11. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

PRODUCT PREVIEW

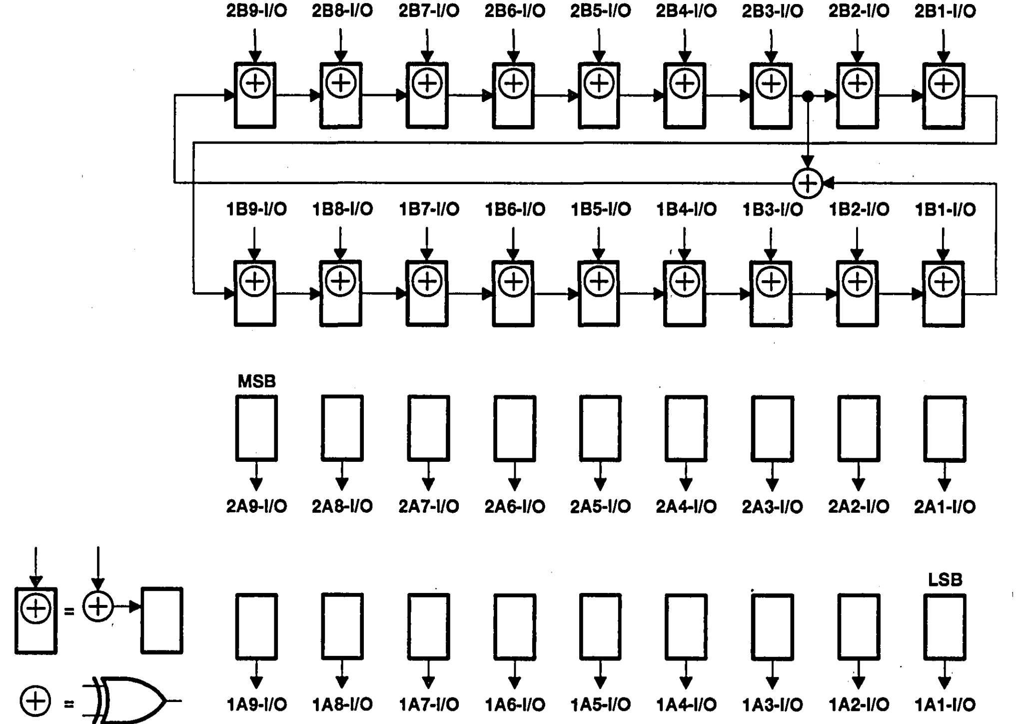


**Figure 12. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**

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## timing description

All test operations of the 'LVTH18245 and 'LVTH182245 are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

PRODUCT PREVIEW

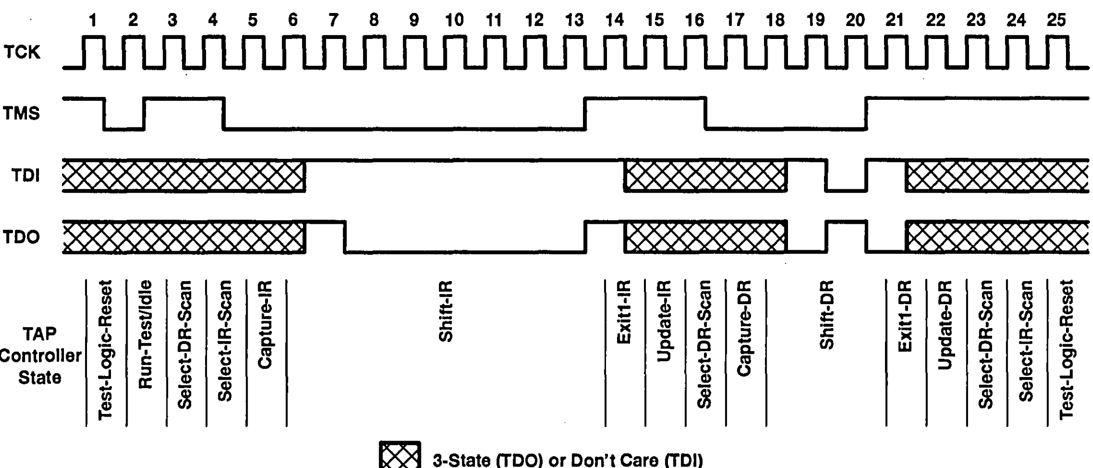



**Figure 13. Timing Example**

PRODUCT PREVIEW

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 4.6 V |
| Input voltage range, $V_I$ (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) | –0.5 V to 7 V |
| Current into any output in the low state, $I_O$: SN54LVTH18245 | 96 mA |
| SN54LVTH182245 (A port or TDO) | 96 mA |
| SN54LVTH182245 (B port) | 30 mA |
| SN74LVTH18245 | 128 mA |
| SN74LVTH182245 (A port or TDO) | 128 mA |
| SN74LVTH182245 (B port) | 30 mA |
| Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH18245 | 48 mA |
| SN54LVTH182245 (A port or TDO) | 48 mA |
| SN54LVTH182245 (B port) | 30 mA |
| SN74LVTH18245 | 64 mA |
| SN74LVTH182245 (A port or TDO) | 64 mA |
| SN74LVTH182245 (B port) | 30 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | –50 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | –50 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): DGG package | 1 W |
| DL package | 1.4 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the ABT *Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54LVTH18245 | | SN74LVTH18245 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 32 | mA |
| $I_{OL}$† | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | TEST CONDITIONS | | | SN54LVTH18245 | | | SN74LVTH18245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | | 2.4 | | | 2.4 | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | | 2.4 | | | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | | 2 | | | | | | |
| | | $I_{OH}$ = –32 mA | | | | | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | | 0.2 | | | 0.2 | V |
| | | $I_{OL}$ = 24 mA | | | | 0.5 | | | 0.5 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 32 mA | | | | 0.5 | | | 0.5 | |
| | | $I_{OL}$ = 48 mA | | | | 0.55 | | | | |
| | | $I_{OL}$ = 64 mA | | | | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | DIR, TCK | | | ±1 | | | ±1 | µA |
| | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | | 10 | | | 10 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | $\overline{OE}$, TDI, TMS | | | 50 | | | 50 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | –25 | | –100 | –25 | | –100 | |
| | | $V_I$ = 5.5 V | A or B ports§ | | | 20 | | | 20 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | | | –5 | | | –5 | |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | A or B ports | 75 | | | 75 | | | µA |
| | | $V_I$ = 2 V | | –75 | | | –75 | | | |
| $I_{OZH}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | TDO | | | 1 | | | 1 | µA |
| $I_{OZL}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | TDO | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs high | | | 2 | | | 2 | mA |
| | | | Outputs low | | | 30 | | | 30 | |
| | | | Outputs disabled | | | 2 | | | 2 | |
| $\Delta I_{CC}$# | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | $V_I$ = 3 V or 0 | | | | 4 | | | 4 | | pF |
| $C_{io}$ | $V_O$ = 3 V or 0 | | | | 11 | | | 11 | | pF |
| $C_o$ | $V_O$ = 3 V or 0 | | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)**

| | | | SN54LVTH18245 | | | | SN74LVTH18245 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, DIR, or $\overline{OE}$ before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, DIR, or $\overline{OE}$ after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18245 | | | | SN74LVTH18245 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 5.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.5 | | | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | | | | | 2 | 9.5 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 9.5 | | | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | | | | | 2.5 | 10.5 | | | ns |
| $t_{PLZ}$ | | | | | | | 2.5 | 9.5 | | | |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18245 | | | | SN74LVTH18245 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK↓ | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 15 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 15 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 3 | 18 | | | ns |
| $t_{PZL}$ | | | | | | | 3 | 18 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 3 | 19 | | | ns |
| $t_{PLZ}$ | | | | | | | 3 | 19 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 8 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 8 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## recommended operating conditions

| | | | SN54LVTH182245 | | SN74LVTH182245 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | A port or TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port or TDO | | 24 | | 32 | mA |
| | | B port | | 12 | | 12 | |
| $I_{OL}$† | Low-level output current | A port or TDO | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | TEST CONDITIONS | | | SN54LVTH182245 | | | SN74LVTH182245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | A port, TDO | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | | 2.4 | | | 2.4 | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | | 2.4 | | | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | | 2 | | | | | | |
| | | $I_{OH}$ = –32 mA | | | | | 2 | | | |
| | | $I_{OH}$ = –12 mA | B port | 2 | | | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | A port, TDO | | | 0.2 | | | 0.2 | V |
| | | $I_{OL}$ = 24 mA | | | | 0.5 | | | 0.5 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 32 mA | | | | 0.5 | | | 0.5 | |
| | | $I_{OL}$ = 48 mA | | | | 0.55 | | | | |
| | | $I_{OL}$ = 64 mA | | | | | | | 0.55 | |
| | | $I_{OL}$ = 64 mA | B port | | | 0.8 | | | 0.8 | |
| $I_I$ | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | DIR, TCK | | | ±1 | | | ±1 | µA |
| | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | | 10 | | | 10 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | $\overline{OE}$, TDI, TMS | | | 50 | | | 50 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | –25 | | –100 | –25 | | –100 | |
| | | $V_I$ = 5.5 V | A or B ports§ | | | 20 | | | 20 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | | | –5 | | | –5 | |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | A or B ports | 75 | | | 75 | | | µA |
| | | $V_I$ = 2 V | | –75 | | | –75 | | | |
| $I_{OZH}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | TDO | | | 1 | | | 1 | µA |
| $I_{OZL}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | TDO | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs high | | | 2 | | | 2 | mA |
| | | | Outputs low | | | 35 | | | 35 | |
| | | | Outputs disabled | | | 2 | | | 2 | |
| $\Delta I_{CC}$# | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | $V_I$ = 3 V or 0 | | | | 4 | | | 4 | | pF |
| $C_{io}$ | $V_O$ = 3 V or 0 | | | | 11 | | | 11 | | pF |
| $C_o$ | $V_O$ = 3 V or 0 | | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| | | | SN54LVTH182245 | | | | SN74LVTH182245 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, DIR, or $\overline{OE}$ before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, DIR, or $\overline{OE}$ after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)**

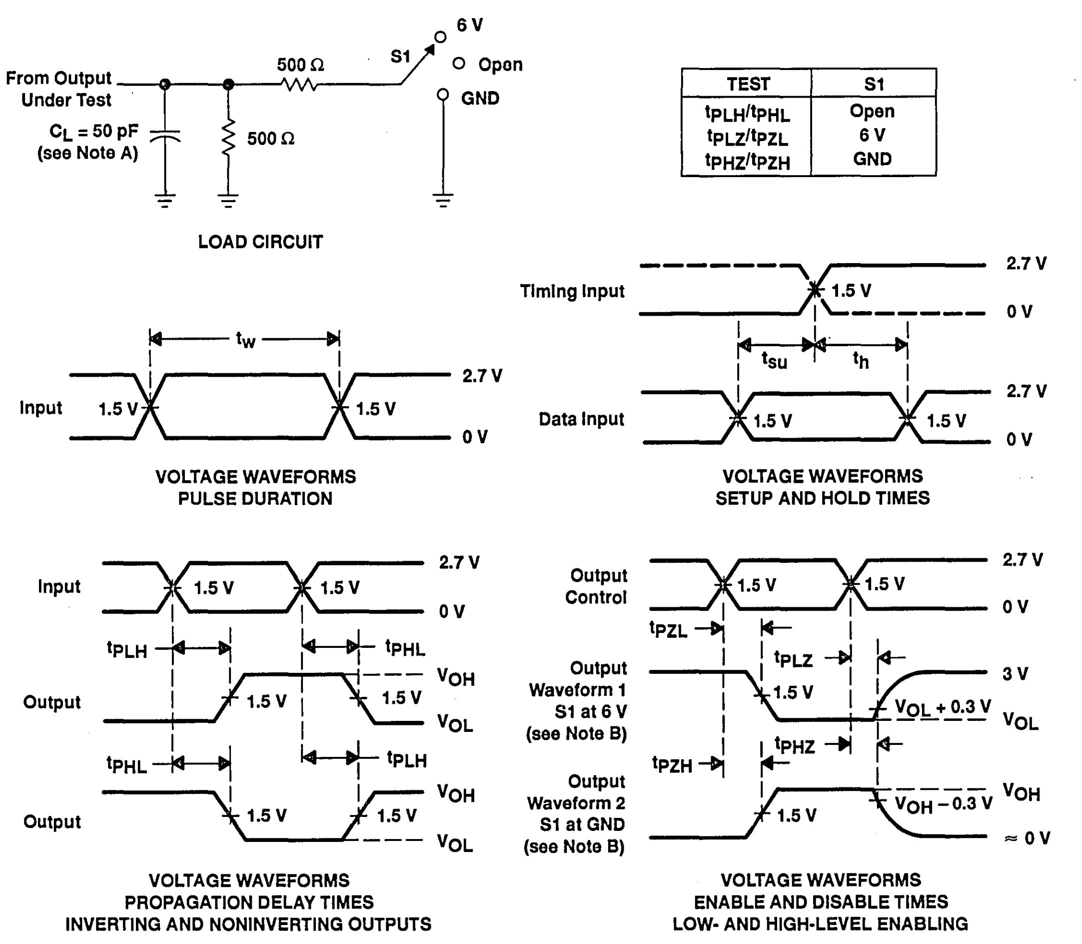
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182245 | | | | SN74LVTH182245 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 6.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.5 | | | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | | | | | 2 | 10 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 10 | | | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | | | | | 2.5 | 11.5 | | | ns |
| $t_{PLZ}$ | | | | | | | 2.5 | 10.5 | | | |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182245 | | | | SN74LVTH182245 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK↓ | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 15 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 15 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 3 | 18 | | | ns |
| $t_{PZL}$ | | | | | | | 3 | 18 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 3 | 19 | | | ns |
| $t_{PLZ}$ | | | | | | | 3 | 19 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 8 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 8 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)**
- **Support Unregulated Battery Operation Down to 2.7 V**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors**
- **B-Port Outputs of 'LVTH182512 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ**
  - **Parallel-Signature Analysis at Inputs**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**
- **Packaged in 64-Pin Plastic Thin Shrink Small Outline (DGG) and 64-Pin Ceramic Dual Flat (HKC) Packages Using 0.5-mm Center-to-Center Spacings**

**SN54LVTH18512, SN54LVTH182512 . . . HKC PACKAGE**
**SN74LVTH18512, SN74LVTH182512 . . . DGG PACKAGE**
**(TOP VIEW)**

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| 1CLKBA | 1 | 64 | 1CLKAB |
| 1LEBA | 2 | 63 | 1LEAB |
| 1$\overline{OEBA}$ | 3 | 62 | 1$\overline{OEAB}$ |
| 1B1 | 4 | 61 | 1A1 |
| 1B2 | 5 | 60 | 1A2 |
| GND | 6 | 59 | GND |
| 1B3 | 7 | 58 | 1A3 |
| 1B4 | 8 | 57 | 1A4 |
| $V_{CC}$ | 9 | 56 | $V_{CC}$ |
| 1B5 | 10 | 55 | 1A5 |
| 1B6 | 11 | 54 | 1A6 |
| GND | 12 | 53 | GND |
| 1B7 | 13 | 52 | 1A7 |
| 1B8 | 14 | 51 | 1A8 |
| 1B9 | 15 | 50 | 1A9 |
| 2B1 | 16 | 49 | 2A1 |
| 2B2 | 17 | 48 | 2A2 |
| 2B3 | 18 | 47 | 2A3 |
| 2B4 | 19 | 46 | 2A4 |
| GND | 20 | 45 | GND |
| 2B5 | 21 | 44 | 2A5 |
| 2B6 | 22 | 43 | 2A6 |
| 2B7 | 23 | 42 | 2A7 |
| $V_{CC}$ | 24 | 41 | $V_{CC}$ |
| 2B8 | 25 | 40 | 2A8 |
| 2B9 | 26 | 39 | 2A9 |
| GND | 27 | 38 | GND |
| 2$\overline{OEBA}$ | 28 | 37 | 2$\overline{OEAB}$ |
| 2LEBA | 29 | 36 | 2LEAB |
| 2CLKBA | 30 | 35 | 2CLKAB |
| TDO | 31 | 34 | TDI |
| TMS | 32 | 33 | TCK |

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## description

The 'LVTH18512 and 'LVTH182512 scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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## description (continued)

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVTH182512, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN74LVTH18512 and SN74LVTH182512 are available in TI's thin shrink small-outline package, which provides twice the I/O pin count and functionality of the standard small-outline packages in the same printed-circuit-board area.

The SN54LVTH18512 and SN54LVTH182512 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH18512 and SN74LVTH182512 are characterized for operation from –40°C to 85°C.



**FUNCTION TABLE†**
**(normal mode, each register)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OEAB}$ | LEAB | CLKAB | A | B |
| L | L | L | X | $B_0$‡ |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | H | X | L | L |
| L | H | X | H | H |
| H | X | X | X | Z |

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established

## functional block diagram

Boundary-Scan Register

1LEAB 63
1CLKAB 64
$V_{CC}$
1$\overline{OEAB}$ 62
1LEBA 2
1CLKBA 1
$V_{CC}$
1$\overline{OEBA}$ 3
C1 1D
1A1 61
4 1B1
One of Nine Channels

2LEAB 36
2CLKAB 35
$V_{CC}$
2$\overline{OEAB}$ 37
2LEBA 29
2CLKBA 30
$V_{CC}$
2$\overline{OEBA}$ 28
C1 1D
2A1 49
16 2B1
One of Nine Channels

Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller

$V_{CC}$
TDI 34
$V_{CC}$
TMS 32
TCK 33
31 TDO

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## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| GND | Ground |
| 1LEAB, 1LEBA, 2LEAB, 2LEBA | Normal-function latch enables. See function table for normal-mode logic. |
| $1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

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## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test-data registers: a 48-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device identification register.

**Figure 1. TAP-Controller State Diagram**

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## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'LVTH18512 and 'LVTH182512, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–44 in the boundary-scan register are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked the outputs would be at the high-impedance state). Reset-value of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register captures a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

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### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'LVTH18512 and 'LVTH182512, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to the active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

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## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'LVTH18512 and 'LVTH182512. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

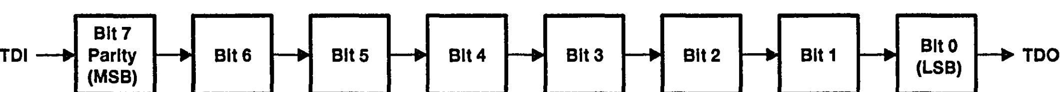


Figure 2. Instruction Register Order of Scan

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## data register description

### boundary-scan register

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs are set to benign values (i.e., if test mode were invoked, the outputs would be at the high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | 2$\overline{OEAB}$ | 35 | 2A9-I/O | 17 | 2B9-I/O |
| 46 | 1$\overline{OEAB}$ | 34 | 2A8-I/O | 16 | 2B8-I/O |
| 45 | 2$\overline{OEBA}$ | 33 | 2A7-I/O | 15 | 2B7-I/O |
| 44 | 1$\overline{OEBA}$ | 32 | 2A6-I/O | 14 | 2B6-I/O |
| 43 | 2CLKAB | 31 | 2A5-I/O | 13 | 2B5-I/O |
| 42 | 1CLKAB | 30 | 2A4-I/O | 12 | 2B4-I/O |
| 41 | 2CLKBA | 29 | 2A3-I/O | 11 | 2B3-I/O |
| 40 | 1CLKBA | 28 | 2A2-I/O | 10 | 2B2-I/O |
| 39 | 2LEAB | 27 | 2A1-I/O | 9 | 2B1-I/O |
| 38 | 1LEAB | 26 | 1A9-I/O | 8 | 1B9-I/O |
| 37 | 2LEBA | 25 | 1A8-I/O | 7 | 1B8-I/O |
| 36 | 1LEBA | 24 | 1A7-I/O | 6 | 1B7-I/O |
| — | — | 23 | 1A6-I/O | 5 | 1B6-I/O |
| — | — | 22 | 1A5-I/O | 4 | 1B5-I/O |
| — | — | 21 | 1A4-I/O | 3 | 1B4-I/O |
| — | — | 20 | 1A3-I/O | 2 | 1B3-I/O |
| — | — | 19 | 1A2-I/O | 1 | 1B2-I/O |
| — | — | 18 | 1A1-I/O | 0 | 1B1-I/O |

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### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run test (RUNT) instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

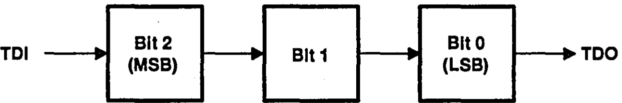


**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

**Figure 4. Bypass Register Order of Scan**

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### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'LVTH18512, the binary value 00000000000000111011000000101111 (0003B02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74LVTH18512.

For the 'LVTH182512, the binary value 00000000000000111100000000101111 (0003C02F, hex) is captured (during Capture-DR state) in the device-identification register to identify this device as Texas Instruments SN54/74LVTH182512.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

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### instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary-run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'LVTH18512 or 'LVTH182512.

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### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–44 of the BSR). When a given output enable is active (logic 0), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

### control boundary to high impedance

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

### control boundary to 1/0

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

### boundary-run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

### boundary read

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

### boundary self test

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

### boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

### boundary-control-register scan

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

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### boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 47–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 47–44 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when both bytes of the device are operating in one direction of data flow (i.e., 1$\overline{\text{OEAB}}$ ≠ 1$\overline{\text{OEBA}}$ and 2$\overline{\text{OEAB}}$ ≠ 2$\overline{\text{OEBA}}$) and in the same direction of data flow (i.e., 1$\overline{\text{OEAB}}$ = 2$\overline{\text{OEAB}}$ and 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$). Otherwise, the bypass instruction is operated.

### sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

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### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 show the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

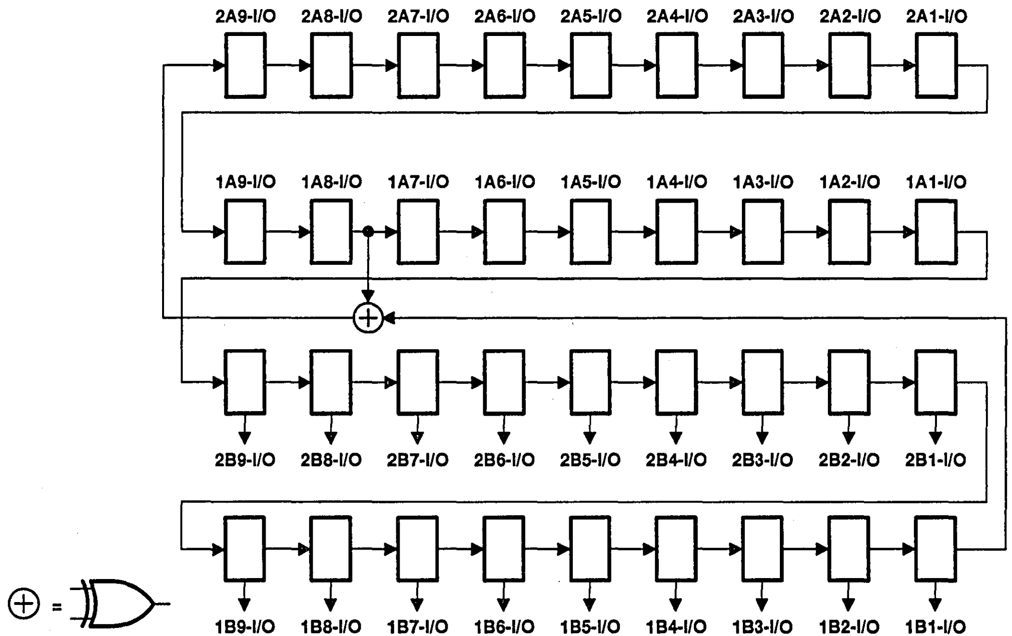


**Figure 5. 36-Bit PRPG Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 0, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 1)**

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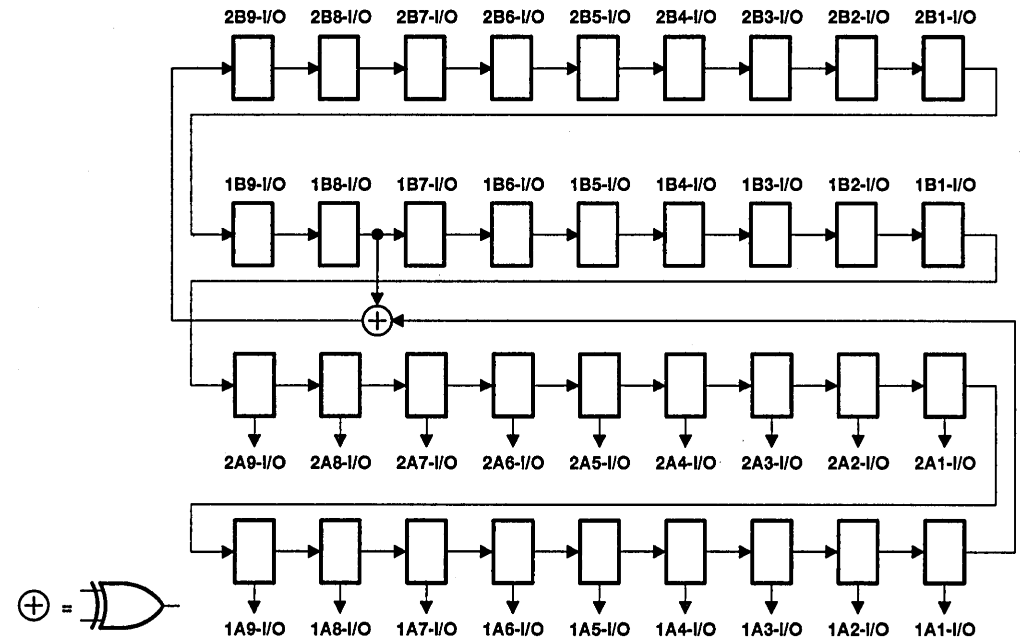


**Figure 6. 36-Bit PRPG Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)**

### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 show the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

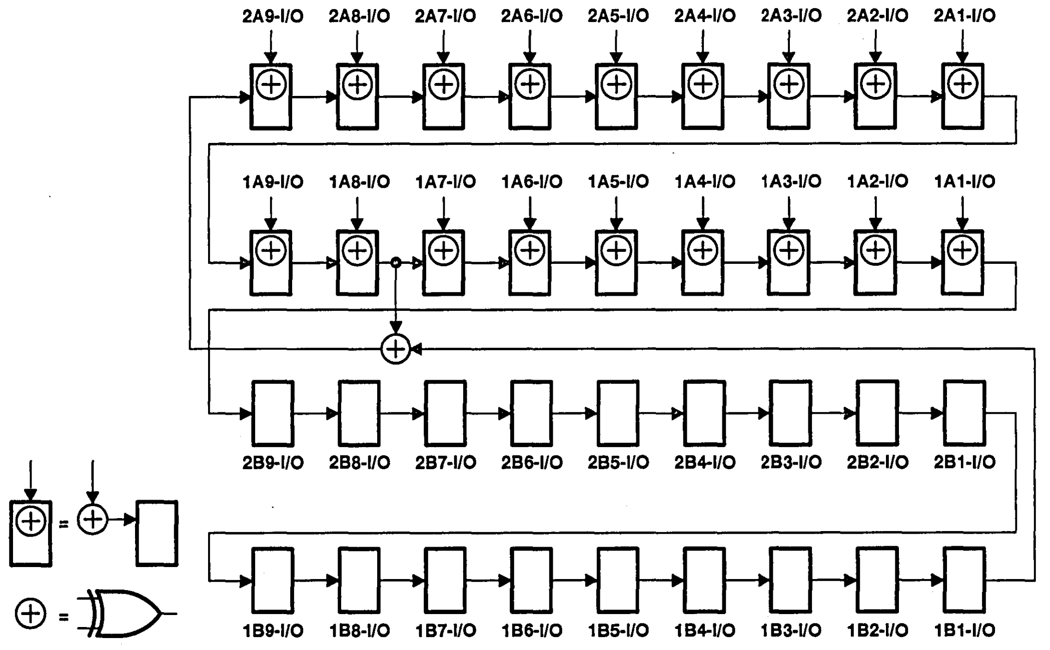


**Figure 7. 36-Bit PSA Configuration ($\overline{1OEAB}$ = $\overline{2OEAB}$ = 0, $\overline{1OEBA}$ = $\overline{2OEBA}$ = 1)**

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2B9-I/O 2B8-I/O 2B7-I/O 2B6-I/O 2B5-I/O 2B4-I/O 2B3-I/O 2B2-I/O 2B1-I/O

1B9-I/O 1B8-I/O 1B7-I/O 1B6-I/O 1B5-I/O 1B4-I/O 1B3-I/O 1B2-I/O 1B1-I/O

2A9-I/O 2A8-I/O 2A7-I/O 2A6-I/O 2A5-I/O 2A4-I/O 2A3-I/O 2A2-I/O 2A1-I/O

1A9-I/O 1A8-I/O 1A7-I/O 1A6-I/O 1A5-I/O 1A4-I/O 1A3-I/O 1A2-I/O 1A1-I/O

Figure 8. 36-Bit PSA Configuration ($1\overline{OEAB}$ = $2\overline{OEAB}$ = 1, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 0)

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**simultaneous PSA and PRPG (PSA/PRPG)**

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 show the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

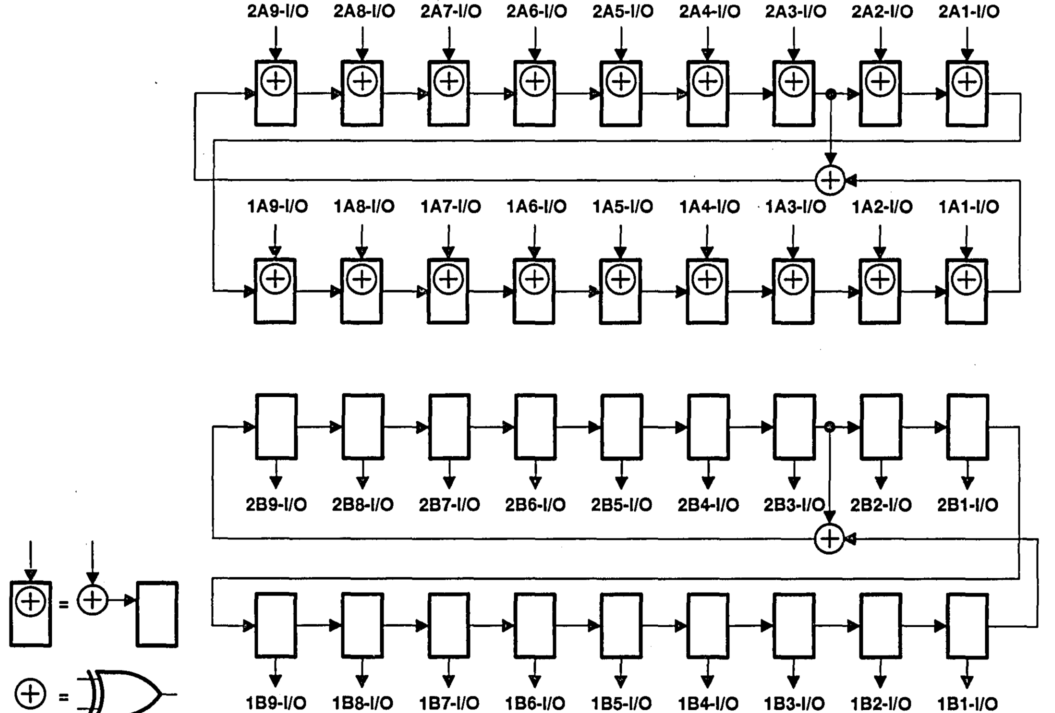


**Figure 9. 18-Bit PSA/PRPG Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 0, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 1)**

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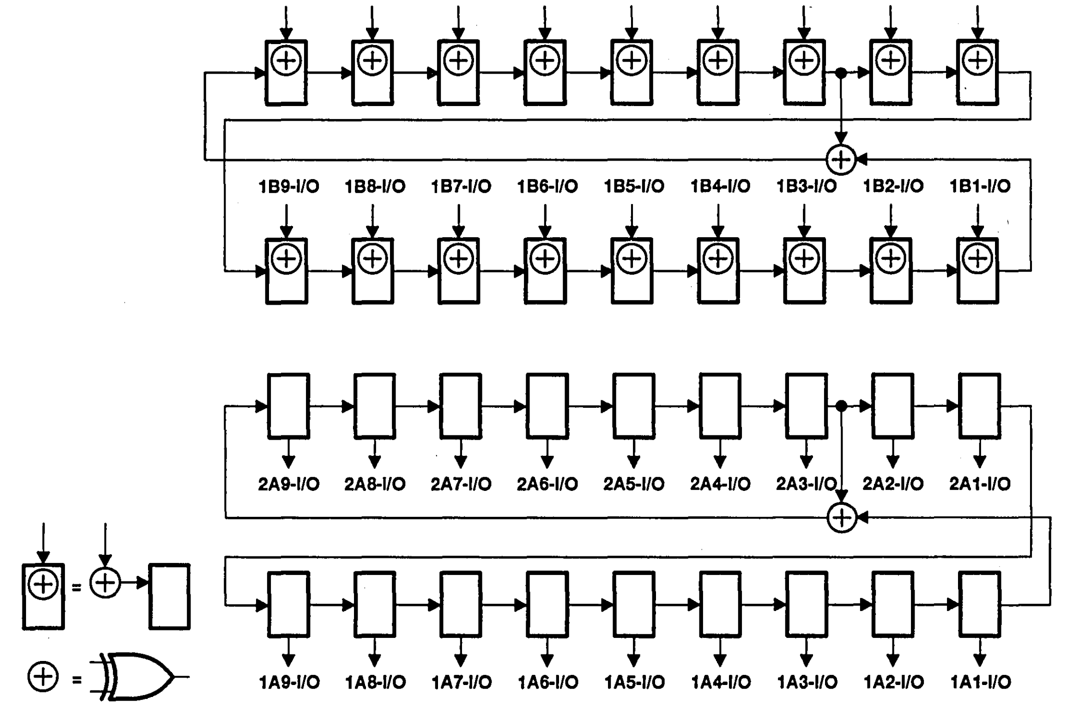


Figure 10. 18-Bit PSA/PRPG Configuration (1$\overline{\text{OEAB}}$ = 2$\overline{\text{OEAB}}$ = 1, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 0)

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### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 show the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

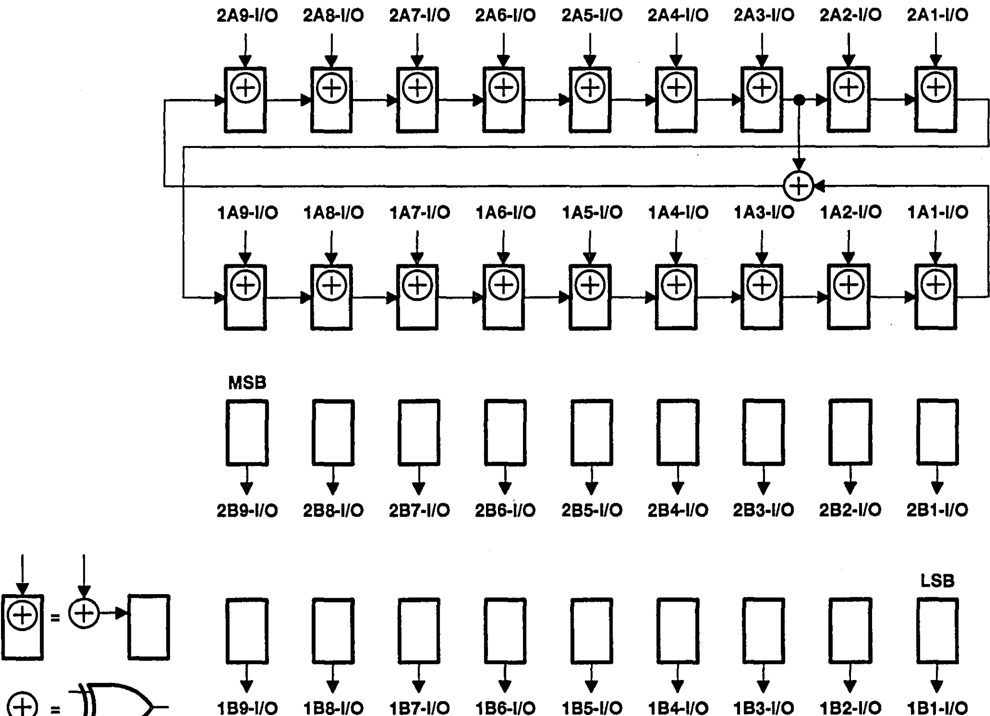


**Figure 11. 18-Bit PSA/COUNT Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 0, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 1)**

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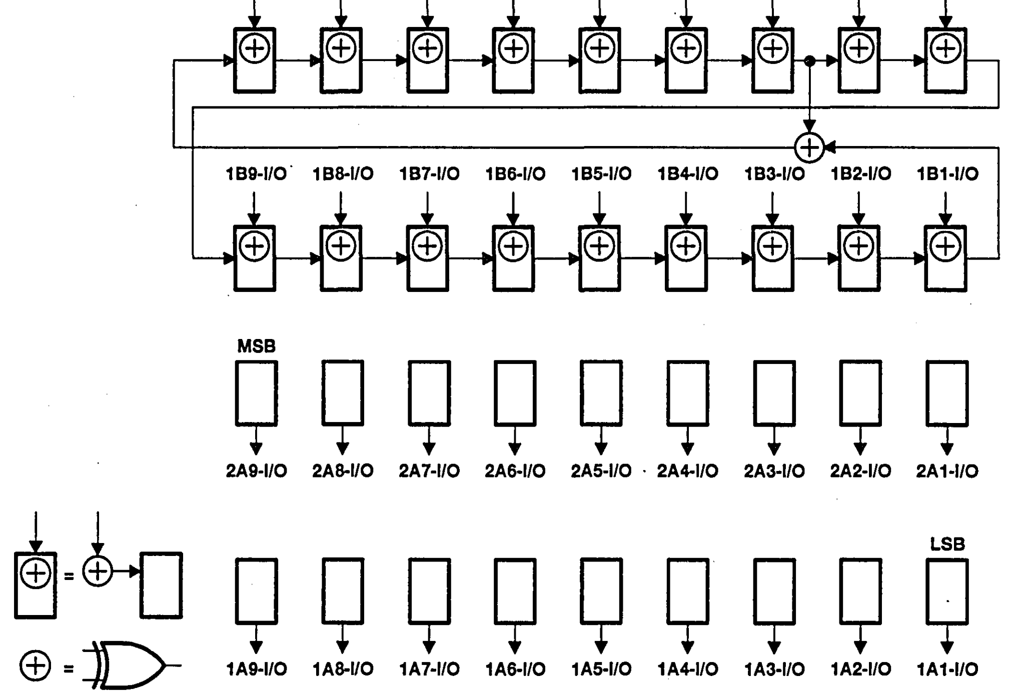


Figure 12. 18-Bit PSA/COUNT Configuration ($1\overline{OEAB}$ = $2\overline{OEAB}$ = 1, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 0)

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## timing description

All test operations of the 'LVTH18512 and 'LVTH182512 are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, as necessary, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | The selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

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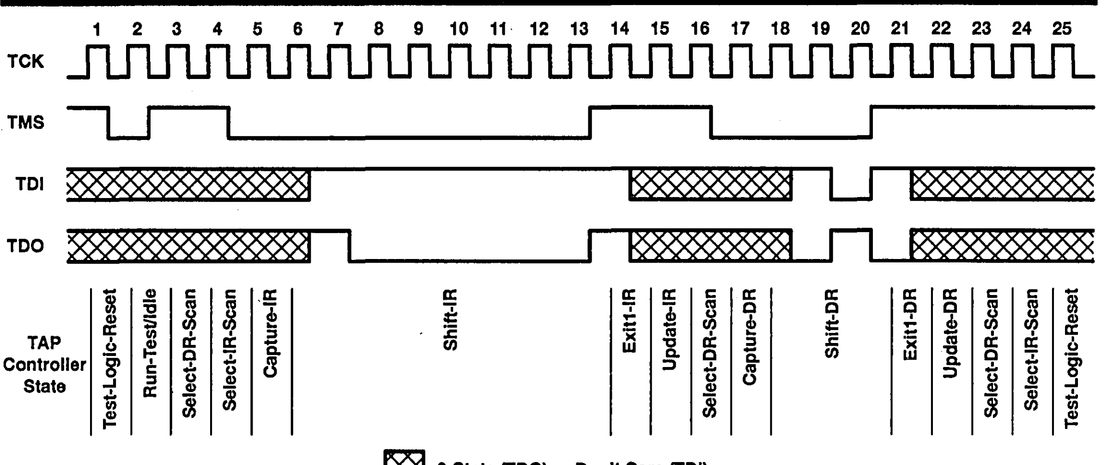


**Figure 13. Timing Example**



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Parameter | Device | Value |
|---|---|---|
| Supply voltage range, $V_{CC}$ | | –0.5 V to 4.6 V |
| Input voltage range, $V_I$ (see Note 1) | | –0.5 V to 7 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) | | –0.5 V to 7 V |
| Current into any output in the low state, $I_O$: | SN54LVTH18512 | 96 mA |
| | SN54LVTH182512 (A port or TDO) | 96 mA |
| | SN54LVTH182512 (B port) | 30 mA |
| | SN74LVTH18512 | 128 mA |
| | SN74LVTH182512 (A port or TDO) | 128 mA |
| | SN74LVTH182512 (B port) | 30 mA |
| Current into any output in the high state, $I_O$ (see Note 2): | SN54LVTH18512 | 48 mA |
| | SN54LVTH182512 (A port or TDO) | 48 mA |
| | SN54LVTH182512 (B port) | 30 mA |
| | SN74LVTH18512 | 64 mA |
| | SN74LVTH182512 (A port or TDO) | 64 mA |
| | SN74LVTH182512 (B port) | 30 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | | –50 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | | –50 mA |
| Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 3): | DGG package | 1 W |
| Storage temperature range, $T_{stg}$ | | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current only flows when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54LVTH18512 | | SN74LVTH18512 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 32 | mA |
| $I_{OL}$† | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH18512 | | | SN74LVTH18512 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| $I_I$ | CLK, LE, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 5 | | | 5 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | 500 | 75 | 150 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | | –500 | –75 | –150 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | | | 1 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | | | | 3 | mA |
| | | | Outputs low | | | | | | 30 | |
| | | | Outputs disabled | | | | | | 3 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.5 | | | 0.5 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 10 | | | 10 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)

| | | | | SN54LVTH18512 | | | | SN74LVTH18512 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | | | | 0 | 100 | | | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | | | 4.4 | | | | ns |
| | | LEAB or LEBA high | | | | | | 3 | | | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | | | 2.8 | | | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | | | | | 1.5 | | | | |
| | | | CLK low | | | | | 1.6 | | | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | | | | 1.4 | | | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | | | | | 3.1 | | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| | | | SN54LVTH18512 | | | | SN74LVTH18512 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, CLK, LE, or $\overline{OE}$ before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, CLK, LE, or $\overline{OE}$ after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | μs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

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### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18512 | | | | SN74LVTH18512 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | | | | | 100 | | | | MHz |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 4.9 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 4.9 | | | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | | | | | 1.5 | 5.8 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.8 | | | |
| $t_{PLH}$ | LEAB or LEBA | B or A | | | | | 1.5 | 7.4 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.7 | | | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 1.5 | 7.1 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 7.1 | | | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 2.5 | 7.8 | | | ns |
| $t_{PLZ}$ | | | | | | | 2.5 | 7.8 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18512 | | | | SN74LVTH18512 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 14 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 14 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.5 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 4 | 17 | | | ns |
| $t_{PZL}$ | | | | | | | 4 | 17 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 5.5 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 4 | 18 | | | ns |
| $t_{PLZ}$ | | | | | | | 4 | 17 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 7 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## recommended operating conditions

| | | | SN54LVTH182512 | | SN74LVTH182512 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 24 | | 32 | mA |
| | | B port | | 12 | | 12 | |
| $I_{OL}$† | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH182512 | | | SN74LVTH182512 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | A, B, TDO | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | A port, TDO | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| | B port | $V_{CC}$ = 3 V, | $I_{OH}$ = –12 mA | 2 | | | 2 | | | |
| $V_{OL}$ | A, B, TDO | $V_{CC}$ = 2.7 V, | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | A port, TDO | $V_{CC}$ = 2.7 V, | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| | B port | $V_{CC}$ = 3 V, | $I_{OL}$ = 12 mA | | | 0.8 | | | 0.8 | |
| $I_I$ | CLK, LE, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 5 | | | 5 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | 500 | 75 | 150 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | | –500 | –75 | –150 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | | | 1 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | | | | 3 | mA |
| | | | Outputs low | | | | | | 30 | |
| | | | Outputs disabled | | | | | | 3 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.5 | | | 0.5 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 10 | | | 10 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

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### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)

| | | | | SN54LVTH182512 | | | | SN74LVTH182512 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | | | | 0 | 100 | | | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | | | 4.4 | | | | ns |
| | | LEAB or LEBA high | | | | | | 3 | | | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | | | 2.8 | | | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | | | | | 1.5 | | | | |
| | | | CLK low | | | | | 1.6 | | | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | | | | 1.4 | | | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | | | | | 3.1 | | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| | | | SN54LVTH182512 | | | | SN74LVTH182512 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, CLK, LE, or $\overline{OE}$ before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, CLK, LE, or $\overline{OE}$ after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182512 | | | | SN74LVTH182512 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | | | | | 100 | | | | MHz |
| $t_{PLH}$ | A | B | | | | | 1.5 | 5.7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.7 | | | |
| $t_{PLH}$ | B | A | | | | | 1.5 | 4.9 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 4.9 | | | |
| $t_{PLH}$ | CLKAB | B | | | | | 1.5 | 6.7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.7 | | | |
| $t_{PLH}$ | CLKBA | A | | | | | 1.5 | 5.8 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.8 | | | |
| $t_{PLH}$ | LEAB | B | | | | | 1.5 | 8.2 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.2 | | | |
| $t_{PLH}$ | LEBA | A | | | | | 1.5 | 7.4 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.7 | | | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 1.5 | 7.9 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 7.9 | | | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 2.5 | 8.4 | | | ns |
| $t_{PLZ}$ | | | | | | | 2.5 | 8.4 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182512 | | | | SN74LVTH182512 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 14 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 14 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.5 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 4 | 17 | | | ns |
| $t_{PZL}$ | | | | | | | 4 | 17 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 5.5 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 4 | 18 | | | ns |
| $t_{PLZ}$ | | | | | | | 4 | 17 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 7 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## PARAMETER MEASUREMENT INFORMATION

From Output Under Test

$C_L$ = 50 pF (see Note A)

500 Ω

500 Ω

S1: 6 V / Open / GND

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)
- Support Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- B-Port Outputs of 'LVTH182514 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Shrink Small-Outline (DGG) and 64-Pin Ceramic Dual Flat (HKC) Packages Using 0.5-mm Center-to-Center Spacings

SN54LVTH18514, SN54LVTH182514 . . . HKC PACKAGE
SN74LVTH18514, SN74LVTH182514 . . . DGG PACKAGE
(TOP VIEW)

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| CLKENBA | 1 | 64 | CLKBA |
| $\overline{OEBA}$ | 2 | 63 | LEBA |
| B1 | 3 | 62 | A1 |
| B2 | 4 | 61 | A2 |
| B3 | 5 | 60 | A3 |
| GND | 6 | 59 | GND |
| B4 | 7 | 58 | A4 |
| B5 | 8 | 57 | A5 |
| $V_{CC}$ | 9 | 56 | $V_{CC}$ |
| B6 | 10 | 55 | A6 |
| B7 | 11 | 54 | A7 |
| GND | 12 | 53 | GND |
| B8 | 13 | 52 | A8 |
| B9 | 14 | 51 | A9 |
| B10 | 15 | 50 | A10 |
| B11 | 16 | 49 | A11 |
| B12 | 17 | 48 | A12 |
| B13 | 18 | 47 | A13 |
| B14 | 19 | 46 | A14 |
| GND | 20 | 45 | GND |
| B15 | 21 | 44 | A15 |
| B16 | 22 | 43 | A16 |
| B17 | 23 | 42 | A17 |
| $V_{CC}$ | 24 | 41 | $V_{CC}$ |
| B18 | 25 | 40 | A18 |
| B19 | 26 | 39 | A19 |
| GND | 27 | 38 | GND |
| B20 | 28 | 37 | A20 |
| $\overline{OEAB}$ | 29 | 36 | LEAB |
| CLKENAB | 30 | 35 | CLKAB |
| TDO | 31 | 34 | TDI |
| TMS | 32 | 33 | TCK |

PRODUCT PREVIEW

## description

The 'LVTH18514 and 'LVTH182514 scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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## description (continued)

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self-test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while $\overline{CLKENAB}$ is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and $\overline{CLKENAB}$ is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow, but uses the $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions, such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVTH182514, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN74LVTH18514 and SN74LVTH182514 are available in TI's thin shrink small-outline (DGG) package, which provides twice the I/O pin count and functionality in the same printed-circuit-board area.

The SN54LVTH18514 and SN54LVTH182514 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH18514 and SN74LVTH182514 are characterized for operation from –40°C to 85°C.

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**FUNCTION TABLE†**
**(normal mode, each register)**

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{OEAB}$ | LEAB | $\overline{CLKENAB}$ | CLKAB | A | B |
| L | L | L | L | X | $B_0$‡ |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | H | X | X | $B_0$‡ |
| L | H | X | X | L | L |
| L | H | X | X | H | H |
| H | X | X | X | X | Z |

† A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established

## functional block diagram

Boundary-Scan Register
CLKENAB 30
LEAB 36
CLKAB 35
VCC
OEAB 29
CLKENBA 1
LEBA 63
CLKBA 64
VCC
OEBA 2
A1 62
C1 1D
3 B1
1 of 20 Channels
Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller
VCC
TDI 34
VCC
TMS 32
TCK 33
31 TDO

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## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A1–A20 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| B1–B20 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| CLKAB, CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| $\overline{CLKENAB}$, $\overline{CLKENBA}$ | Normal-function clock enables. See function table for normal-mode logic. |
| GND | Ground |
| LEAB, LEBA | Normal-function latch enables. See function table for normal-mode logic. |
| $\overline{OEAB}$, $\overline{OEBA}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

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## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are passed along this serial-test bus. The TAP controller monitors two signals from the test bus: TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationships of the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test data registers: a 48-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.



Figure 1. TAP-Controller State Diagram

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## state diagram description

The TAP controller is a synchronous finite-state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states, based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register at a time can be accessed.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'LVTH18514 and 'LVTH182514, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–46 in the boundary-scan register are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

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**Shift-DR (continued)**

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle, in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, such updates occur on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'LVTH18514 and 'LVTH182514, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to the active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

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### register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

### instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'LVTH18514 and 'LVTH182514. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The instruction register order of scan is shown in Figure 2.

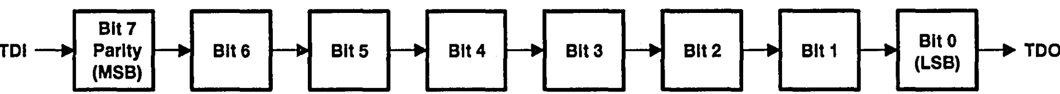


**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used to store test data that is to be applied externally to the device output pins, and/or to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–46 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | $\overline{OEAB}$ | 39 | A20-I/O | 19 | B20-I/O |
| 46 | $\overline{OEBA}$ | 38 | A19-I/O | 18 | B19-I/O |
| 45 | CLKAB | 37 | A18-I/O | 17 | B18-I/O |
| 44 | CLKBA | 36 | A17-I/O | 16 | B17-I/O |
| 43 | $\overline{CLKENAB}$ | 35 | A16-I/O | 15 | B16-I/O |
| 42 | $\overline{CLKENBA}$ | 34 | A15-I/O | 14 | B15-I/O |
| 41 | LEAB | 33 | A14-I/O | 13 | B14-I/O |
| 40 | LEBA | 32 | A13-I/O | 12 | B13-I/O |
| — | — | 31 | A12-I/O | 11 | B12-I/O |
| — | — | 30 | A11-I/O | 10 | B11-I/O |
| — | — | 29 | A10-I/O | 9 | B10-I/O |
| — | — | 28 | A9-I/O | 8 | B9-I/O |
| — | — | 27 | A8-I/O | 7 | B8-I/O |
| — | — | 26 | A7-I/O | 6 | B7-I/O |
| — | — | 25 | A6-I/O | 5 | B6-I/O |
| — | — | 24 | A5-I/O | 4 | B5-I/O |
| — | — | 23 | A4-I/O | 3 | B4-I/O |
| — | — | 22 | A3-I/O | 2 | B3-I/O |
| — | — | 21 | A2-I/O | 1 | B2-I/O |
| — | — | 20 | A1-I/O | 0 | B1-I/O |

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### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run (RUNT) instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The boundary-control register order of scan is shown in Figure 3.

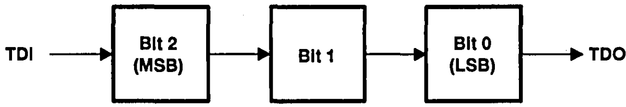


**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

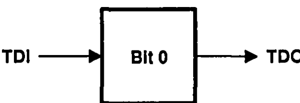


**Figure 4. Bypass Register Order of Scan**

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### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'LVTH18514, the binary value 00000000000000111101000000101111 (0003D02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74LVTH18514.

For the 'LVTH182514, the binary value 00000000000000111110000000101111 (0003E02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74LVTH182514.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE† |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

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## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary-run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control-register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control-register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'LVTH18514 or 'LVTH182514.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output-enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–46 of the BSR). When a given output enable is active (logic 0), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift register and shadow latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

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## boundary-control register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE<br>BIT 2 → BIT 0<br>MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/40-bit mode (PRPG) |
| X10 | Parallel-signature analysis/40-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/20-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/20-bit mode (PSA/COUNT) |

While the control input BSCs (bits 47–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 47–46 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when the device is operating in one direction of data flow (that is, $\overline{OEAB} \neq \overline{OEBA}$). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

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**pseudo-random pattern generation (PRPG)**

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 illustrate the 40-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

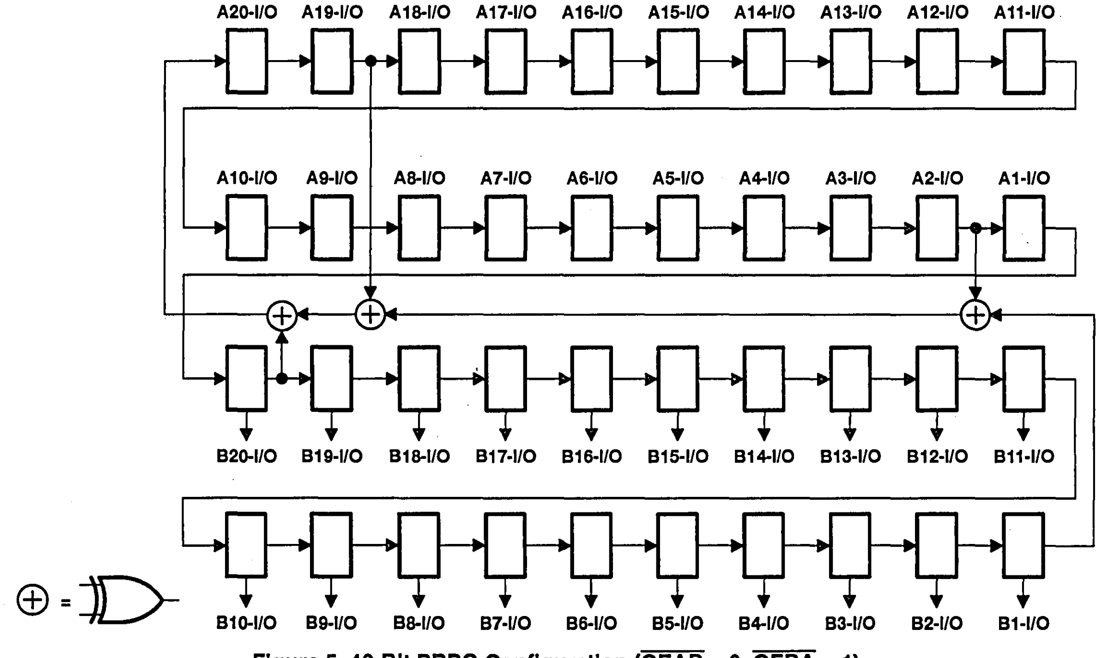


**Figure 5. 40-Bit PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

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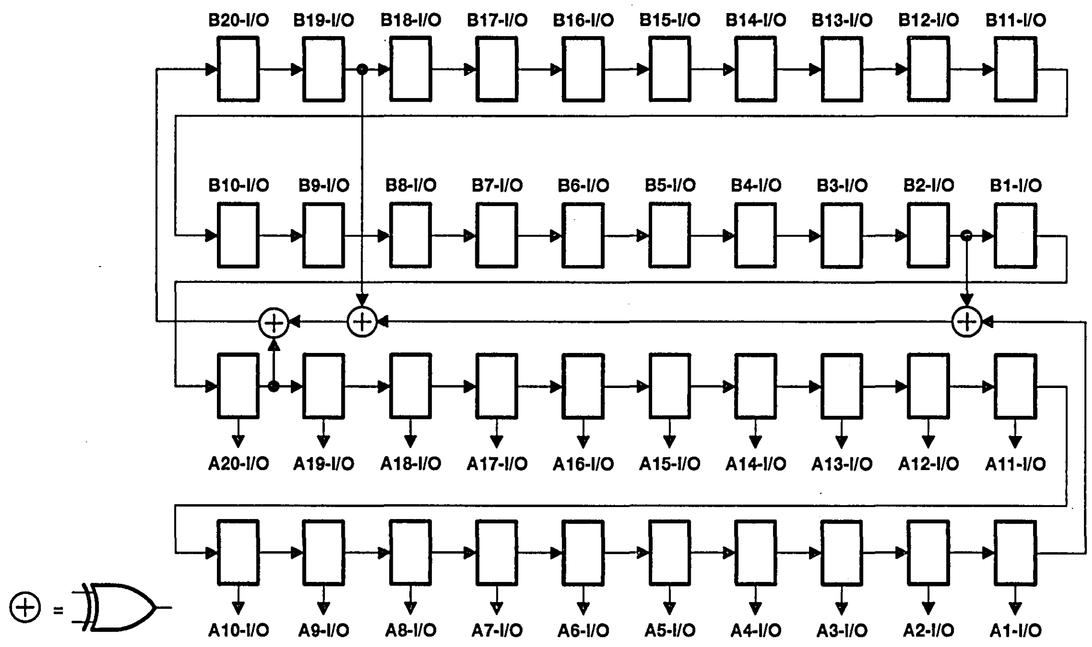


Figure 6. 40-Bit PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

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### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 40-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 illustrate the 40-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

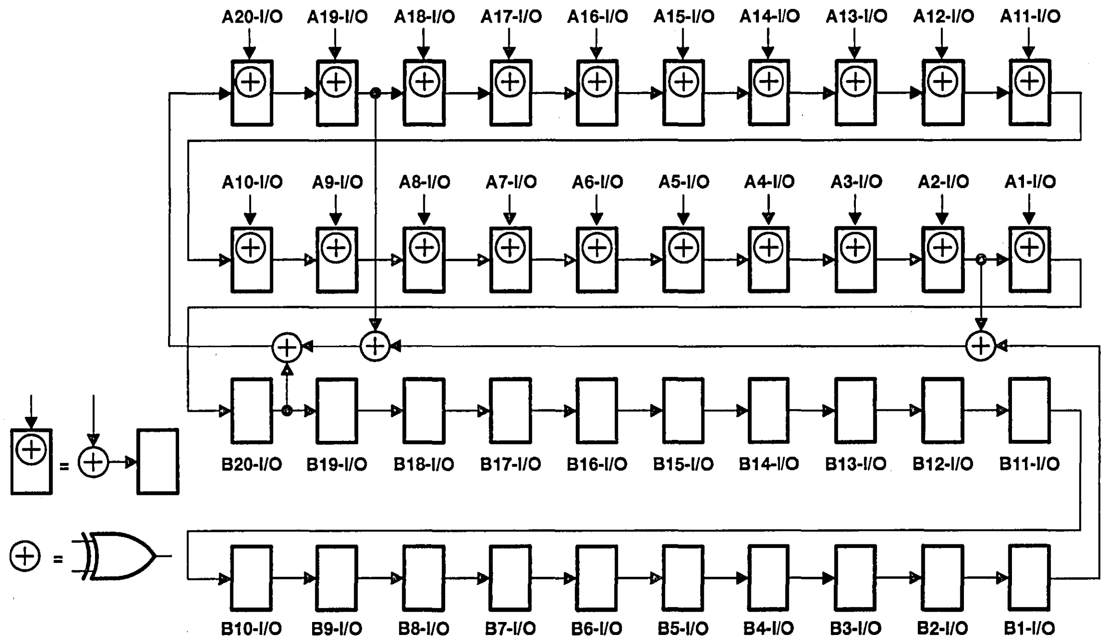



Figure 7. 40-Bit PSA Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

PRODUCT PREVIEW

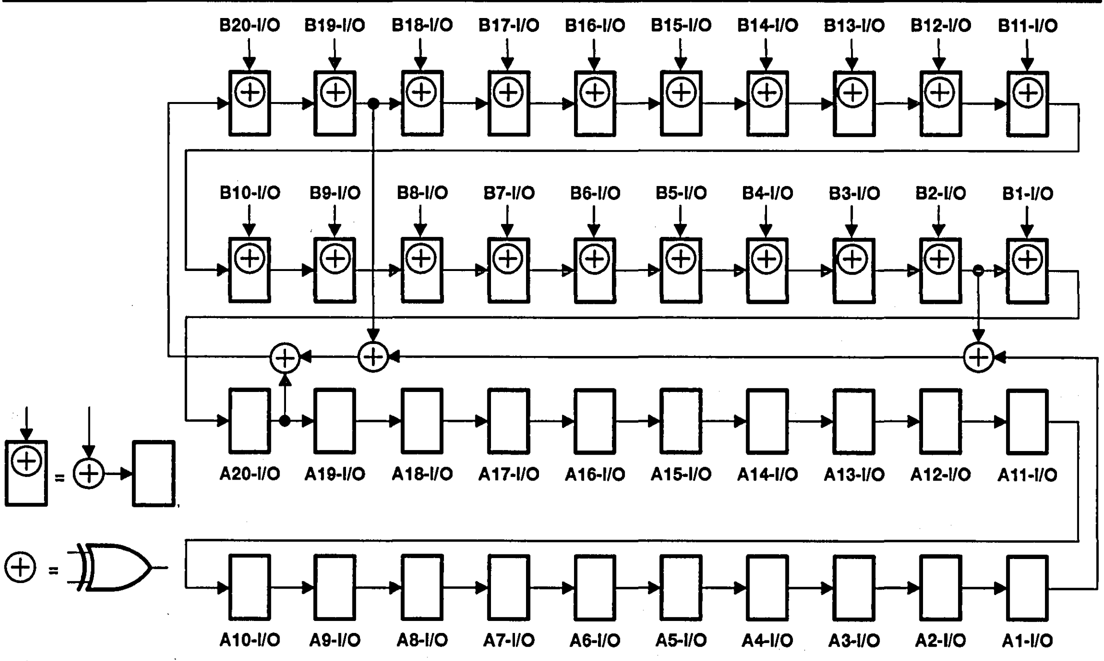



**Figure 8. 40-Bit PSA Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

PRODUCT PREVIEW

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into a 20-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, a 20-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 illustrate the 20-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

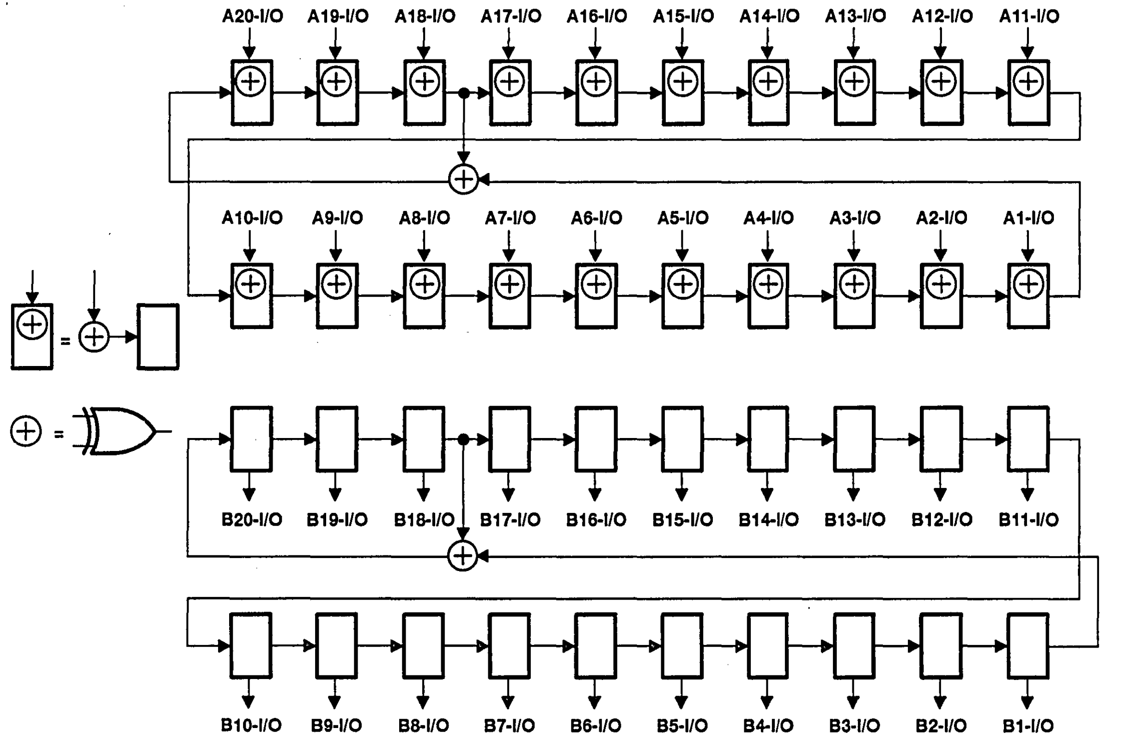



**Figure 9. 20-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

PRODUCT PREVIEW

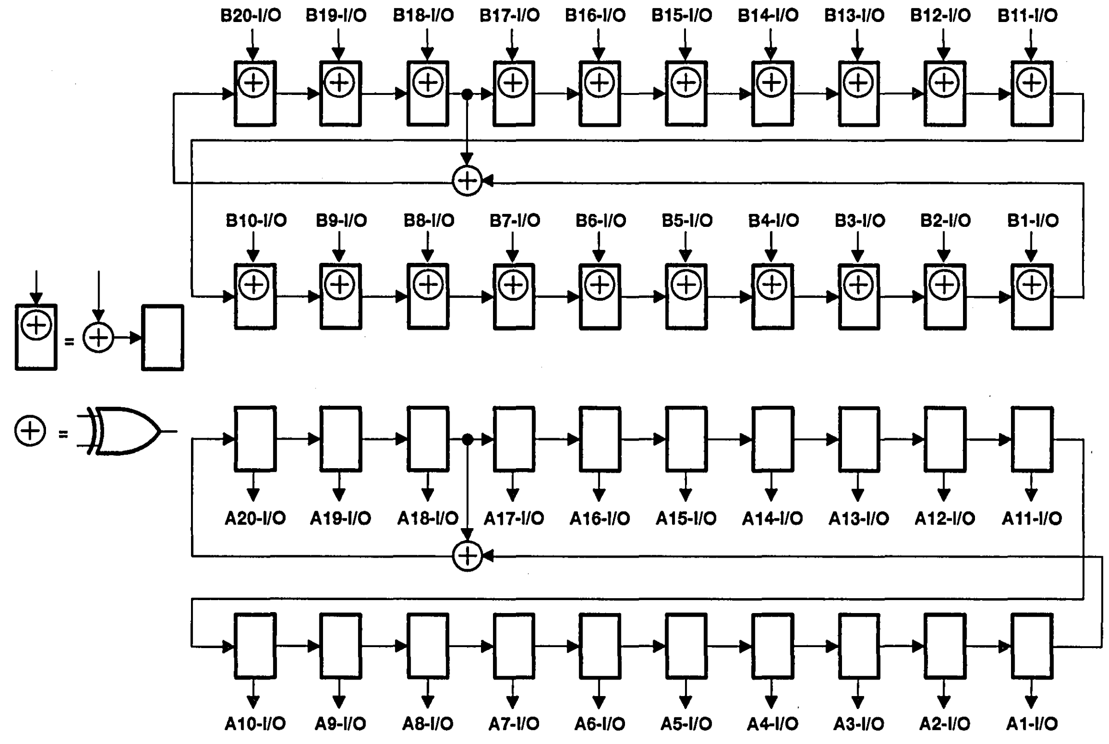



Figure 10. 20-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

PRODUCT PREVIEW

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into a 20-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, a 20-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 illustrate the 20-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

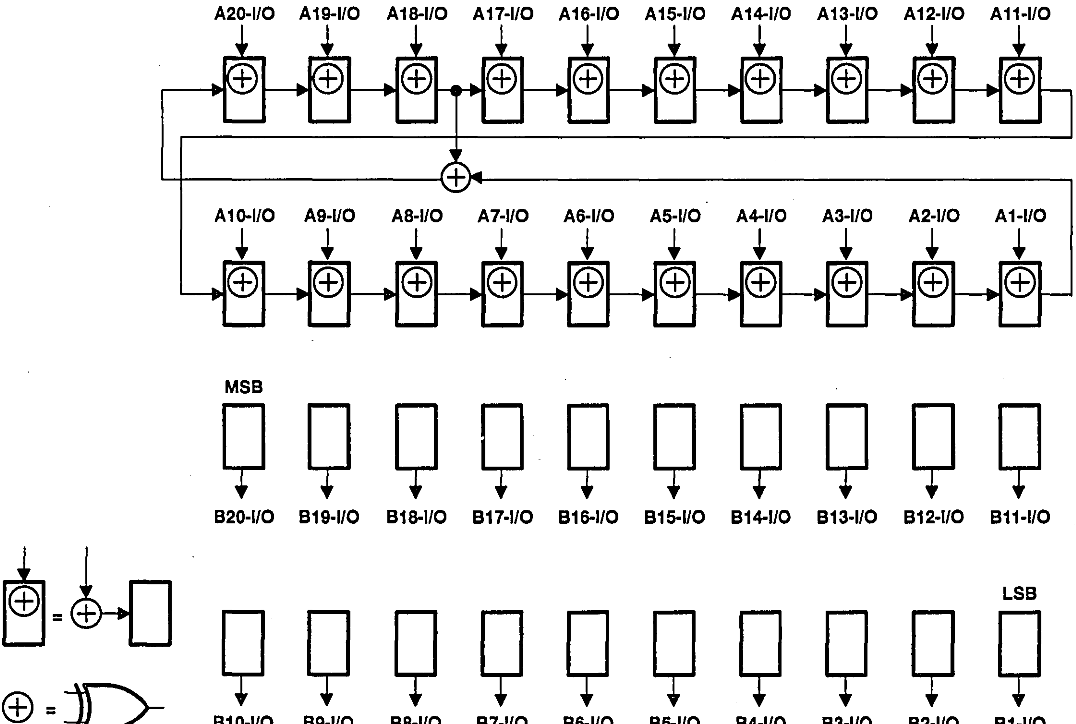



**Figure 11. 20-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

PRODUCT PREVIEW

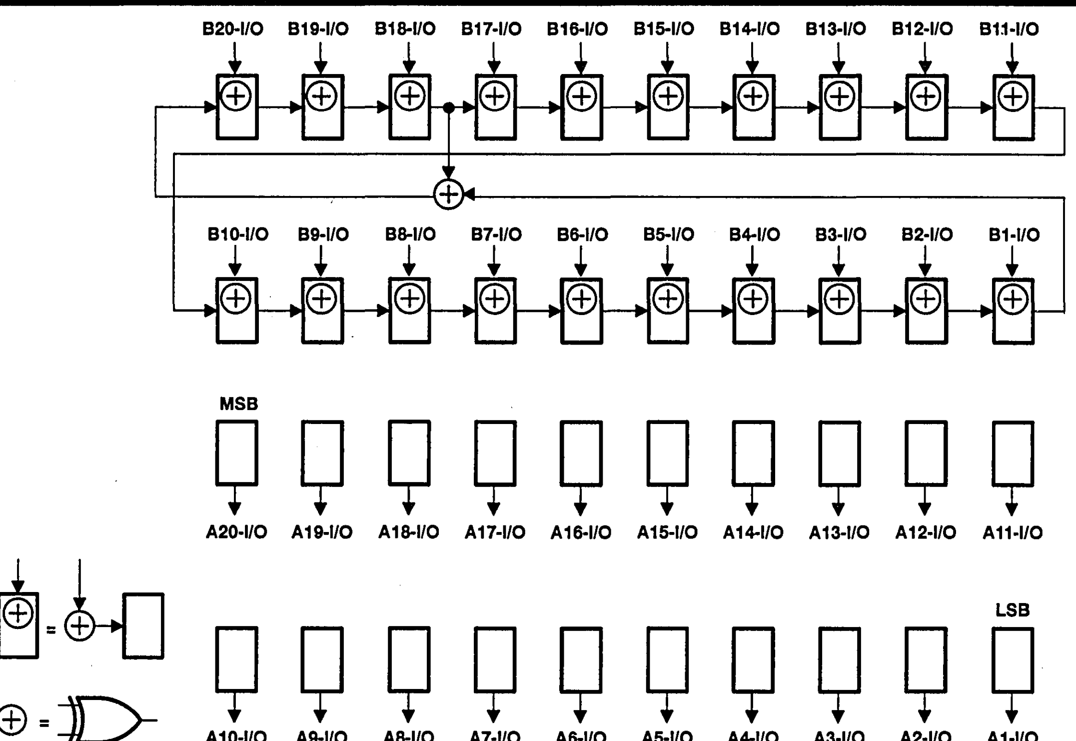



Figure 12. 20-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

PRODUCT PREVIEW

## timing description

All test operations of the 'LVTH18514 and 'LVTH182514 are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, as necessary, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 describes the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed. |

PRODUCT PREVIEW

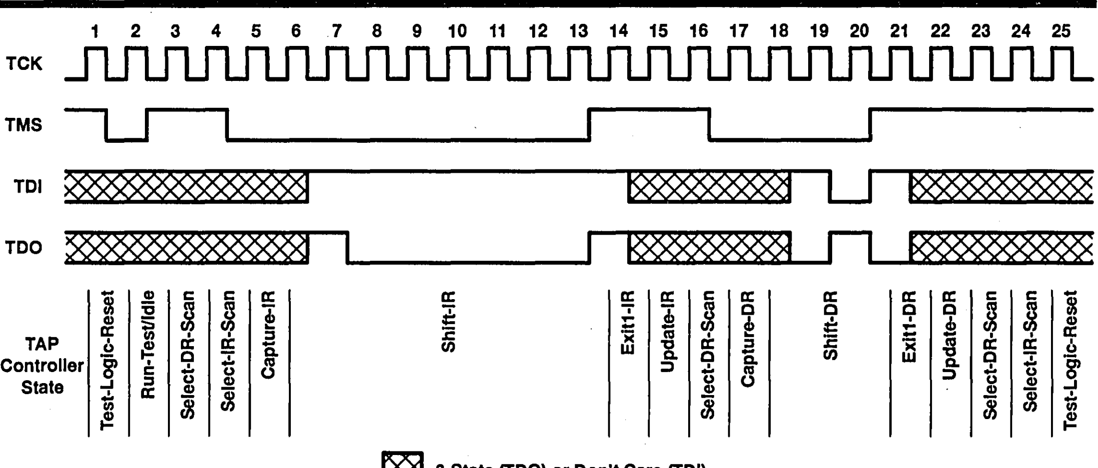



**Figure 13. Timing Example**

PRODUCT PREVIEW

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ........ –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) ........ –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) ........ –0.5 V to 7 V
Current into any output in the low state, $I_O$: SN54LVTH18514 ........ 96 mA
SN54LVTH182514 (A port or TDO) ........ 96 mA
SN54LVTH182514 (B port) ........ 30 mA
SN74LVTH18514 ........ 128 mA
SN74LVTH182514 (A port or TDO) ........ 128 mA
SN74LVTH182514 (B port) ........ 30 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH18514 ........ 48 mA
SN54LVTH182514 (A port or TDO) ........ 48 mA
SN54LVTH182514 (B port) ........ 30 mA
SN74LVTH18514 ........ 64 mA
SN74LVTH182514 (A port or TDO) ........ 64 mA
SN74LVTH182514 (B port) ........ 30 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) ........ –50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) ........ –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): DGG package ........ 1 W
Storage temperature range ........ –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current only flows when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54LVTH18514 | | SN74LVTH18514 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 32 | mA |
| $I_{OL}$† | Low-level output current | | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | TEST CONDITIONS | | | SN54LVTH18514 | | | SN74LVTH18514 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 2.7 V, | $I_I$ = −18 mA | | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = −100 µA | | $V_{CC}$−0.2 | | | $V_{CC}$−0.2 | | | V |
| | $V_{CC}$ = 2.7 V, | $I_{OH}$ = −3 mA | | 2.4 | | | 2.4 | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = −8 mA | | 2.4 | | | 2.4 | | | |
| | | $I_{OH}$ = −24 mA | | 2 | | | | | | |
| | | $I_{OH}$ = −32 mA | | | | | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | | 0.2 | | | 0.2 | V |
| | | $I_{OL}$ = 24 mA | | | | 0.5 | | | 0.5 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 32 mA | | | | 0.5 | | | 0.5 | |
| | | $I_{OL}$ = 48 mA | | | | 0.55 | | | | |
| | | $I_{OL}$ = 64 mA | | | | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | CLK, $\overline{CLKEN}$, LE, TCK | | | ±1 | | | ±1 | µA |
| | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | | 10 | | | 10 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | $\overline{OE}$, TDI, TMS | | | 5 | | | 5 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | −25 | | −100 | −25 | | −100 | |
| | | $V_I$ = 5.5 V | A or B ports§ | | | 20 | | | 20 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | | | −5 | | | −5 | |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | A or B ports | 75 | | 500 | 75 | 150 | 500 | µA |
| | | $V_I$ = 2 V | | −75 | | −500 | −75 | −150 | −500 | |
| $I_{OZH}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | TDO | | | 1 | | | 1 | µA |
| $I_{OZL}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | TDO | | | −1 | | | −1 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | $V_{CC}$ = 3.6 V, $V_I$ = $V_{CC}$ or GND | $I_O$ = 0, | Outputs high | | | | | | 3 | mA |
| | | | Outputs low | | | | | | 30 | |
| | | | Outputs disabled | | | | | | 3 | |
| $\Delta I_{CC}$# | $V_{CC}$ = 3 V to 3.6 V, Other inputs at $V_{CC}$ or GND | One input at $V_{CC}$ – 0.6 V, | | | | 0.5 | | | 0.5 | mA |
| $C_i$ | $V_I$ = 3 V or 0 | | | | 4 | | | 4 | | pF |
| $C_{io}$ | $V_O$ = 3 V or 0 | | | | 10 | | | 10 | | pF |
| $C_o$ | $V_O$ = 3 V or 0 | | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)

| | | | SN54LVTH18514 | | | | SN74LVTH18514 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | | | 0 | 100 | | | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | | 4.4 | | | | ns |
| | | LEAB or LEBA high | | | | | 3 | | | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | | 2.4 | | | | ns |
| | | A before LEAB↓ or B before LEBA↓, CLK high | | | | | 1.5 | | | | |
| | | A before LEAB↓ or B before LEBA↓, CLK low | | | | | 1.6 | | | | |
| | | $\overline{CLKEN}$ before CLK↑ | | | | | 2.8 | | | | |
| $t_h$ | Hold time | A after CLKAB↑ | | | | | 1 | | | | ns |
| | | B after CLKBA↑ | | | | | 1.4 | | | | |
| | | A after LEAB↓ or B after LEBA↓ | | | | | 3.1 | | | | |
| | | $\overline{CLKEN}$ after CLK↑ | | | | | 0.7 | | | | |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| | | | SN54LVTH18514 | | | | SN74LVTH18514 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)

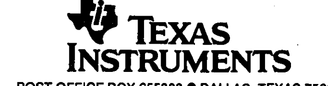
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18514 | | | | SN74LVTH18514 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | | | | | 100 | | | | MHz |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 5.1 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.1 | | | |
| $t_{PLH}$ | CLKAB | B | | | | | 1.5 | 5.8 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.8 | | | |
| $t_{PLH}$ | CLKBA | A | | | | | 1.5 | 6.4 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.4 | | | |
| $t_{PLH}$ | LEAB or LEBA | B or A | | | | | 2 | 8.1 | | | ns |
| $t_{PHL}$ | | | | | | | 2 | 6.7 | | | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 2 | 9.1 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 9.6 | | | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 2.5 | 10.4 | | | ns |
| $t_{PLZ}$ | | | | | | | 2.5 | 9.1 | | | |

PRODUCT PREVIEW

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18514 | | | | SN74LVTH1854 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 14 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 14 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.5 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 4 | 17 | | | ns |
| $t_{PZL}$ | | | | | | | 4 | 17 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 5.5 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 4 | 18 | | | ns |
| $t_{PLZ}$ | | | | | | | 4 | 17 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 7 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.



## recommended operating conditions

| | | | SN54LVTH182514 | | SN74LVTH182514 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 24 | | 32 | mA |
| | | B port | | 12 | | 12 | |
| $I_{OL}$† | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | TEST CONDITIONS | | | SN54LVTH182514 | | | SN74LVTH182514 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | A, B, TDO | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | A port, TDO | 2.4 | | | 2.4 | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | | 2.4 | | | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | | 2 | | | | | | |
| | | $I_{OH}$ = –32 mA | | | | | 2 | | | |
| | | $I_{OH}$ = –12 mA | B port | 2 | | | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | A, B, TDO | | | 0.2 | | | 0.2 | V |
| | | $I_{OL}$ = 24 mA | A port, TDO | | | 0.5 | | | 0.5 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 32 mA | | | | 0.5 | | | 0.5 | |
| | | $I_{OL}$ = 48 mA | | | | 0.55 | | | | |
| | | $I_{OL}$ = 64 mA | | | | | | | 0.55 | |
| | | $I_{OL}$ = 12 mA | B port | | | 0.8 | | | 0.8 | |
| $I_I$ | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | CLK, $\overline{CLKEN}$, LE, TCK | | | ±1 | | | ±1 | µA |
| | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | | 10 | | | 10 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | $\overline{OE}$, TDI, TMS | | | 5 | | | 5 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | –25 | | –100 | –25 | | –100 | |
| | | $V_I$ = 5.5 V | A or B ports§ | | | 20 | | | 20 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | | | –5 | | | –5 | |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | A or B ports | 75 | | 500 | 75 | 150 | 500 | µA |
| | | $V_I$ = 2 V | | –75 | | –500 | –75 | –150 | –500 | |
| $I_{OZH}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | TDO | | | 1 | | | 1 | µA |
| $I_{OZL}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | TDO | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs high | | | | | | 3 | mA |
| | | | Outputs low | | | | | | 30 | |
| | | | Outputs disabled | | | | | | 3 | |
| $\Delta I_{CC}$# | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | | 0.5 | | | 0.5 | mA |
| $C_i$ | $V_I$ = 3 V or 0 | | | | 4 | | | 4 | | pF |
| $C_{io}$ | $V_O$ = 3 V or 0 | | | | 10 | | | 10 | | pF |
| $C_o$ | $V_O$ = 3 V or 0 | | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
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## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)

| | | | SN54LVTH182514 | | | | SN74LVTH182514 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | | | 0 | 100 | | | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | | 4.4 | | | | ns |
| | | LEAB or LEBA high | | | | | 3 | | | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | | 2.8 | | | | ns |
| | | A before LEAB↓ or B before LEBA↓, CLK high | | | | | 1.5 | | | | |
| | | A before LEAB↓ or B before LEBA↓, CLK low | | | | | 1.6 | | | | |
| | | $\overline{CLKEN}$ before CLK↑ | | | | | 2.8 | | | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | | | 1.4 | | | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | | | | 3.1 | | | | |
| | | $\overline{CLKEN}$ after CLK↑ | | | | | 0.7 | | | | |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| | | | SN54LVTH182514 | | | | SN74LVTH182514 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182514 | | | | SN74LVTH182514 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | | | | | 100 | | | | MHz |
| $t_{PLH}$ | A | B | | | | | 1.5 | 5.9 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.9 | | | |
| $t_{PLH}$ | B | A | | | | | 1.5 | 5.1 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.1 | | | |
| $t_{PLH}$ | CLKAB | B | | | | | 1.5 | 6.7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.7 | | | |
| $t_{PLH}$ | CLKBA | A | | | | | 1.5 | 6.4 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.4 | | | |
| $t_{PLH}$ | LEAB | B | | | | | 2 | 8.2 | | | ns |
| $t_{PHL}$ | | | | | | | 2 | 6.7 | | | |
| $t_{PLH}$ | LEBA | A | | | | | 2 | 8.1 | | | ns |
| $t_{PHL}$ | | | | | | | 2 | 6.7 | | | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 2 | 9.5 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 9.7 | | | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 2.5 | 11.1 | | | ns |
| $t_{PLZ}$ | | | | | | | 2.5 | 9.8 | | | |

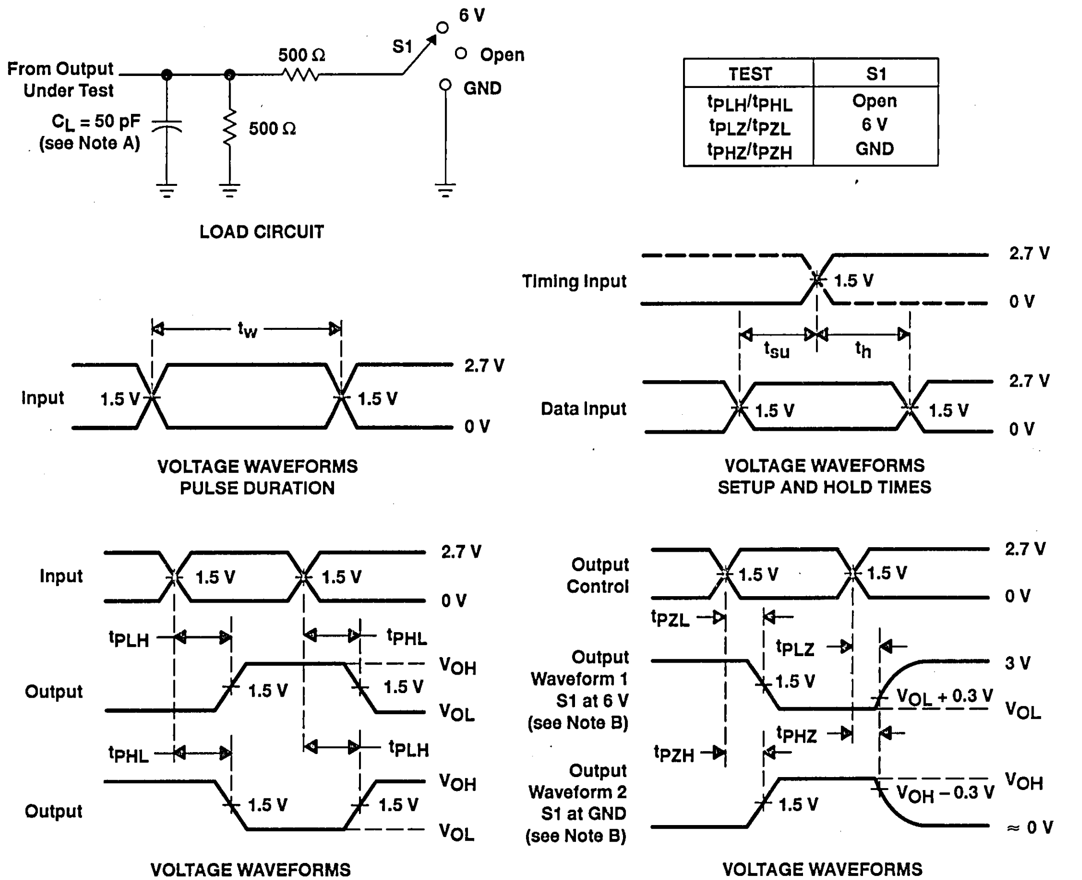
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182514 | | | | SN74LVTH182514 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 14 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 14 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.5 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 4 | 17 | | | ns |
| $t_{PZL}$ | | | | | | | 4 | 17 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 5.5 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 4 | 18 | | | ns |
| $t_{PLZ}$ | | | | | | | 4 | 17 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 7 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)
- Support Unregulated Battery Operation Down to 2.7 V
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- B-Port Outputs of 'LVTH182516 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Shrink Small-Outline (DGG), 64-Pin Ceramic Dual Flat (HKC), and 68-Pin Ceramic Quad Flat (HV) Packages

SN54LVTH18516, SN54LVTH182516 . . . HKC PACKAGE
SN74LVTH18516, SN74LVTH182516 . . . DGG PACKAGE
(TOP VIEW)

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| $\overline{CLKENBA}$ | 1 | 64 | CLKBA |
| $\overline{OEBA}$ | 2 | 63 | LEBA |
| NC | 3 | 62 | SBA |
| B1 | 4 | 61 | A1 |
| B2 | 5 | 60 | A2 |
| GND | 6 | 59 | GND |
| B3 | 7 | 58 | A3 |
| B4 | 8 | 57 | A4 |
| $V_{CC}$ | 9 | 56 | $V_{CC}$ |
| B5 | 10 | 55 | A5 |
| B6 | 11 | 54 | A6 |
| GND | 12 | 53 | GND |
| B7 | 13 | 52 | A7 |
| B8 | 14 | 51 | A8 |
| B9 | 15 | 50 | A9 |
| B10 | 16 | 49 | A10 |
| B11 | 17 | 48 | A11 |
| B12 | 18 | 47 | A12 |
| B13 | 19 | 46 | A13 |
| GND | 20 | 45 | GND |
| B14 | 21 | 44 | A14 |
| B15 | 22 | 43 | A15 |
| B16 | 23 | 42 | A16 |
| $V_{CC}$ | 24 | 41 | $V_{CC}$ |
| B17 | 25 | 40 | A17 |
| B18 | 26 | 39 | A18 |
| GND | 27 | 38 | GND |
| NC | 28 | 37 | SAB |
| $\overline{OEAB}$ | 29 | 36 | LEAB |
| $\overline{CLKENAB}$ | 30 | 35 | CLKAB |
| TDO | 31 | 34 | TDI |
| TMS | 32 | 33 | TCK |

NC – No internal connection

PRODUCT PREVIEW

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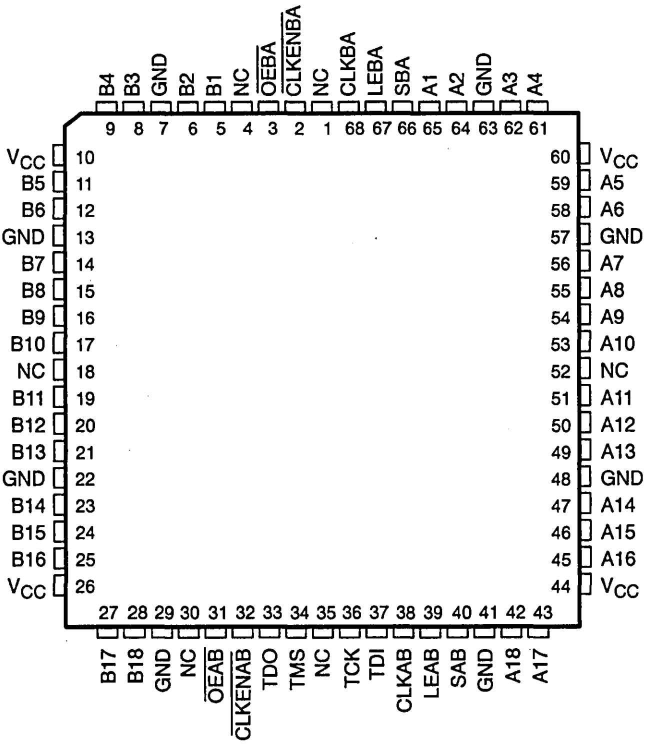


NC – No internal connection

PRODUCT PREVIEW

## description

The 'LVTH18516 and 'LVTH182516 scan test devices with 18-bit bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clock modes and that also allow for multiplexed transmission of data directly from the input bus or from the internal registers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

## description (continued)

Data flow in each direction is controlled by latch-enable (LEAB and LEBA), clock-enable (CLKENAB and CLKENBA), clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and OEBA) inputs. For A-to-B data flow, the device registers operate in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKENAB is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and CLKENAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (real-time data mode). When SAB is high, stored A-data is selected for presentation to the B bus (stored data mode). When OEAB is low, the B outputs are active. When OEAB is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the LEBA, CLKENBA, CLKBA, SBA, and OEBA inputs. Figure 1 illustrates the four fundamental bus-management functions that are performed with the 'LVTH18516 and 'LVTH182516.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVTH182516, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN74LVTH18516 and SN74LVTH182516 are available in TI's thin shrink small-outline (DGG) package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVTH18516 and SN54LVTH182516 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH18516 and SN74LVTH182516 are characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

**FUNCTION TABLE†**
**(normal mode, each register)**

| INPUTS | | | | | | OUTPUT | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|
| OEAB | SAB | LEAB | CLKENAB | CLKAB | A | B | |
| H | X | X | X | X | X | Z | Isolation |
| L | L | X | X | X | L | L | Real-time A data to B bus |
| L | L | X | X | X | H | H | Real-time A data to B bus |
| L | H | X | X | X | X | $Q_{A0}$‡ | Stored A data to B bus |
| X | X | H | X | X | X | Unspecified§ | Store A data ($A \rightarrow Q_A$) |
| X | X | L | L | ↑ | X | Unspecified§ | Store A data ($A \rightarrow Q_A$) |
| X | X | L | L | L | X | Unspecified§ | Hold A data ($Q_{A0} \rightarrow Q_A$) |
| X | X | L | H | X | X | Unspecified§ | Hold A data ($Q_{A0} \rightarrow Q_A$) |

† A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, SBA, LEBA, CLKENBA, and CLKBA.
‡ Output level of internal register before the indicated steady-state input conditions are established.
§ The data output functions are enabled or disabled by various signals at the OE and S inputs. Data input functions are always enabled.

PRODUCT PREVIEW

BUS A BUS B

| $\overline{OEAB}$ | $\overline{OEBA}$ | SBA |
|---|---|---|
| H | L | L |

REAL-TIME TRANSFER
BUS B TO BUS A

BUS A BUS B

| $\overline{OEAB}$ | $\overline{OEBA}$ | SAB |
|---|---|---|
| L | H | L |

REAL-TIME TRANSFER
BUS A TO BUS B

BUS A BUS B

| $\overline{OEAB}$ | $\overline{OEBA}$ | LEAB | LEBA | $\overline{CLKENAB}$ | $\overline{CLKENBA}$ | CLKAB | CLKBA |
|---|---|---|---|---|---|---|---|
| X | H | H | X | X | X | X | X |
| H | X | X | H | X | X | X | X |
| H | H | H | H | X | X | X | X |
| X | H | L | X | L | X | ↑ | X |
| H | X | X | L | X | L | X | ↑ |
| H | H | L | L | L | L | ↑ | ↑ |

STORAGE FROM
A, B, OR A AND B

BUS A BUS B

| $\overline{OEAB}$ | $\overline{OEBA}$ | SAB | SBA |
|---|---|---|---|
| H | L | X | H |
| L | H | H | X |
| L | L | H | H |

TRANSFER STORED DATA
TO A AND/OR B

**Figure 1. Bus-Management Functions**

## functional block diagram

Boundary-Scan Register

CLKENAB 30
LEAB 36
CLKAB 35
SAB 37
VCC
OEAB 29
CLKENBA 1
LEBA 63
CLKBA 64
SBA 62
VCC
OEBA 2

C1 1D
C1 1D
C1 1D
C1 1D

A1 61
4 B1

1 of 18 Channels

Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller

VCC
TDI 34
VCC
TMS 32
TCK 33
31 TDO

Pin numbers shown are for the DGG and HKC packages.

PRODUCT PREVIEW

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A1–A18 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| B1–B18 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| CLKAB, CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| $\overline{\text{CLKENAB}}$, $\overline{\text{CLKENBA}}$ | Normal-function clock enables. See function table for normal-mode logic. |
| GND | Ground |
| LEAB, LEBA | Normal-function latch enables. See function table for normal-mode logic. |
| $\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$ | Normal-function active-low output enables. See function table for normal-mode logic. An internal pullup at each terminal will force the terminal to a high level if left unconnected. |
| SAB, SBA | Normal-function select controls. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

PRODUCT PREVIEW

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 2 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test-data registers: a 46-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

Test-Logic-Reset
TMS = H
TMS = L
Run-Test/Idle
TMS = L
TMS = H
Select-DR-Scan
TMS = H
Select-IR-Scan
TMS = H
TMS = L
Capture-DR
TMS = H
TMS = H
Capture-IR
TMS = L
TMS = L
Shift-DR
TMS = L
Shift-IR
TMS = L
TMS = H
TMS = H
TMS = H
Exit1-DR
Exit1-IR
TMS = H
TMS = L
TMS = L
Pause-DR
TMS = L
Pause-IR
TMS = L
TMS = H
TMS = H
TMS = L
TMS = L
Exit2-DR
Exit2-IR
TMS = H
TMS = H
Update-DR
Update-IR
TMS = H
TMS = L
TMS = H
TMS = L

**Figure 2. TAP-Controller State Diagram**

PRODUCT PREVIEW

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 2 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'LVTH18516 and 'LVTH182516, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 45–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., such that if test mode were invoked the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

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### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

**Shift-DR (continued)**

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'LVTH18516 and 'LVTH182516, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to the active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

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## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'LVTH18516 and 'LVTH182516. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 3.

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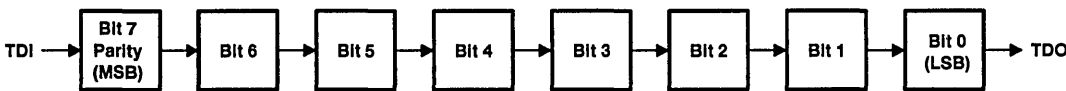


**Figure 3. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 46 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle, as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 45–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 45–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 45 | $\overline{\text{OEAB}}$ | 35 | A18-I/O | 17 | B18-I/O |
| 44 | $\overline{\text{OEBA}}$ | 34 | A17-I/O | 16 | B17-I/O |
| 43 | LEAB | 33 | A16-I/O | 15 | B16-I/O |
| 42 | LEBA | 32 | A15-I/O | 14 | B15-I/O |
| 41 | $\overline{\text{CLKENAB}}$ | 31 | A14-I/O | 13 | B14-I/O |
| 40 | $\overline{\text{CLKENBA}}$ | 30 | A13-I/O | 12 | B13-I/O |
| 39 | CLKAB | 29 | A12-I/O | 11 | B12-I/O |
| 38 | CLKBA | 28 | A11-I/O | 10 | B11-I/O |
| 37 | SAB | 27 | A10-I/O | 9 | B10-I/O |
| 36 | SBA | 26 | A9-I/O | 8 | B9-I/O |
| — | — | 25 | A8-I/O | 7 | B8-I/O |
| — | — | 24 | A7-I/O | 6 | B7-I/O |
| — | — | 23 | A6-I/O | 5 | B6-I/O |
| — | — | 22 | A5-I/O | 4 | B5-I/O |
| — | — | 21 | A4-I/O | 3 | B4-I/O |
| — | — | 20 | A3-I/O | 2 | B3-I/O |
| — | — | 19 | A2-I/O | 1 | B2-I/O |
| — | — | 18 | A1-I/O | 0 | B1-I/O |

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### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 4.

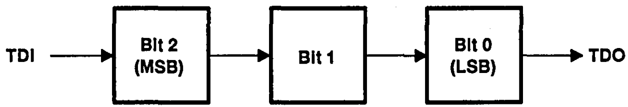


**Figure 4. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 5.

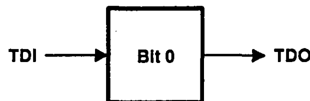


**Figure 5. Bypass Register Order of Scan**

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### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'LVTH18516, the binary value 00000000000000111111000000101111 (0003F02F, hex) is captured (during Capture-DR state) in the device-identification register to identify this device as Texas Instruments SN54/74LVTH18516.

For the 'LVTH182516, the binary value 00000000000001000000000000101111 (0004002F, hex) is captured (during Capture-DR state) in the device-identification register to identify this device as Texas Instruments SN54/74LVTH182516.

The device-identification register order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the device-identification register bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

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## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'LVTH18516 or 'LVTH182516.

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### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 45–44 of the BSR). When a given output enable is active (logic 0), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The device identification register is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

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## boundary-control register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 45–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 45–44 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when the device is operating in one direction of data flow (that is, $\overline{OEAB} \neq \overline{OEBA}$). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

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**pseudo-random pattern generation (PRPG)**

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 6 and 7 illustrate the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR prior to performing this operation. A seed value of all zeroes will not produce additional patterns.

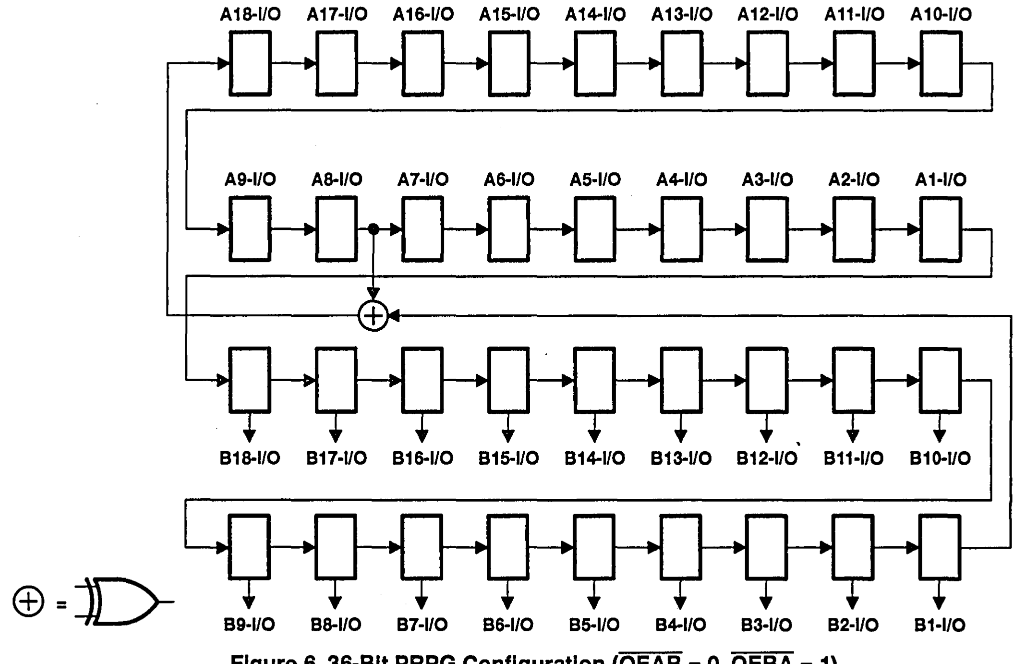


**Figure 6. 36-Bit PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

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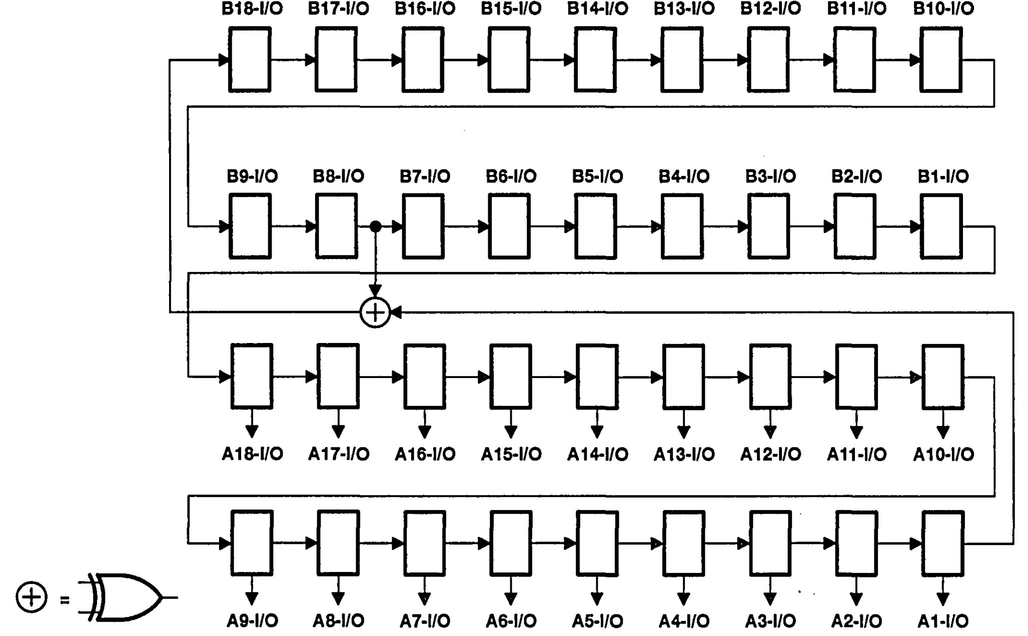


**Figure 7. 36-Bit PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

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### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 8 and 9 illustrate the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

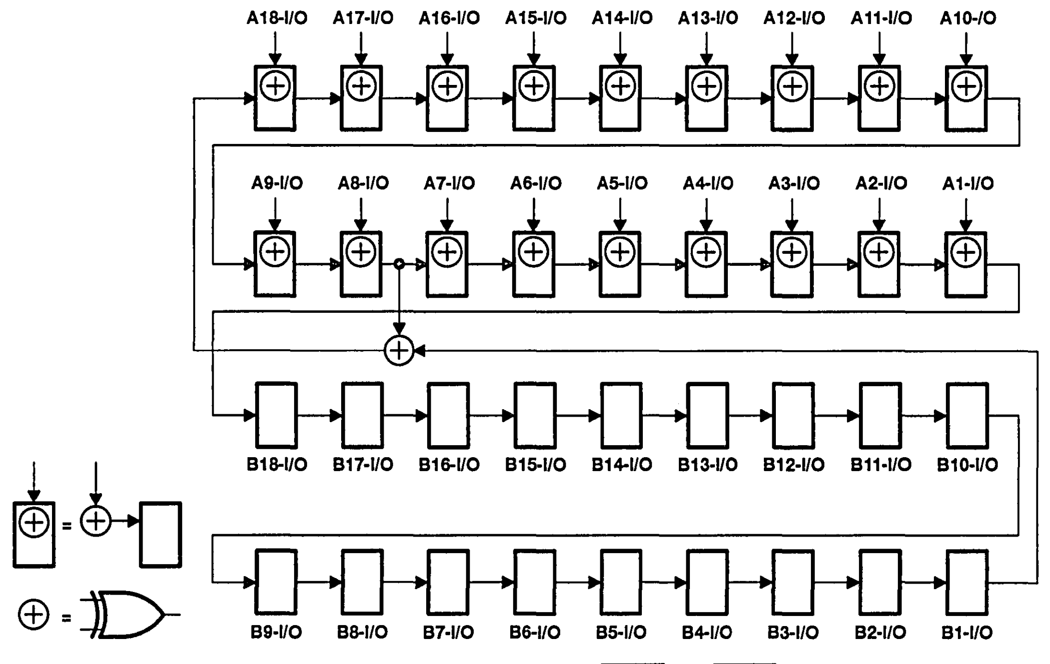


**Figure 8. 36-Bit PSA Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

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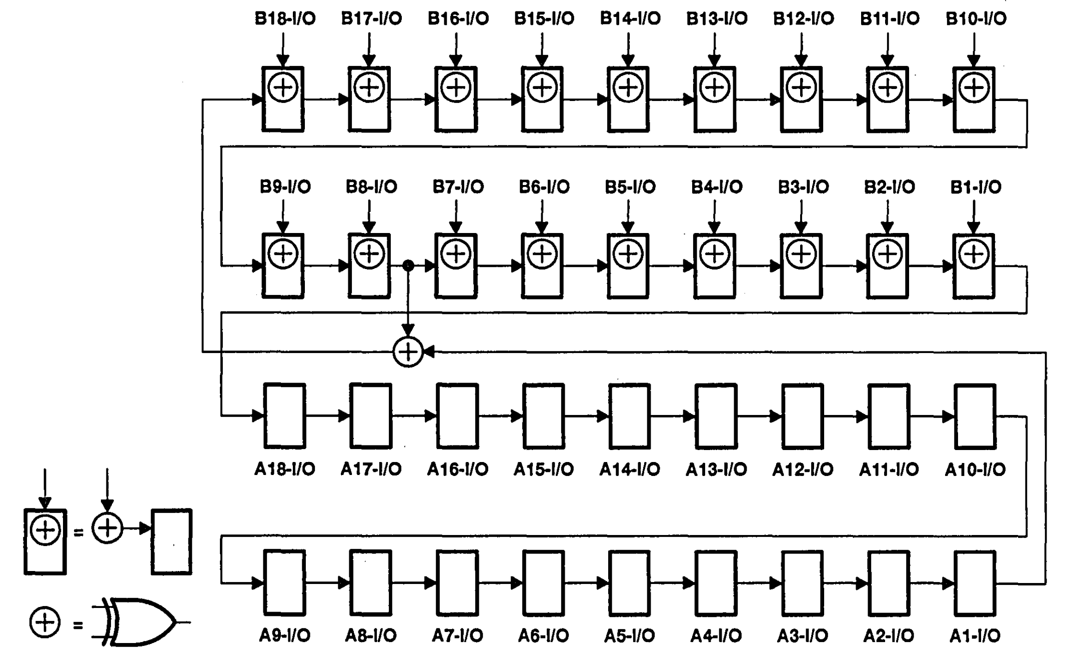


**Figure 9. 36-Bit PSA Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

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**simultaneous PSA and PRPG (PSA/PRPG)**

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 10 and 11 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

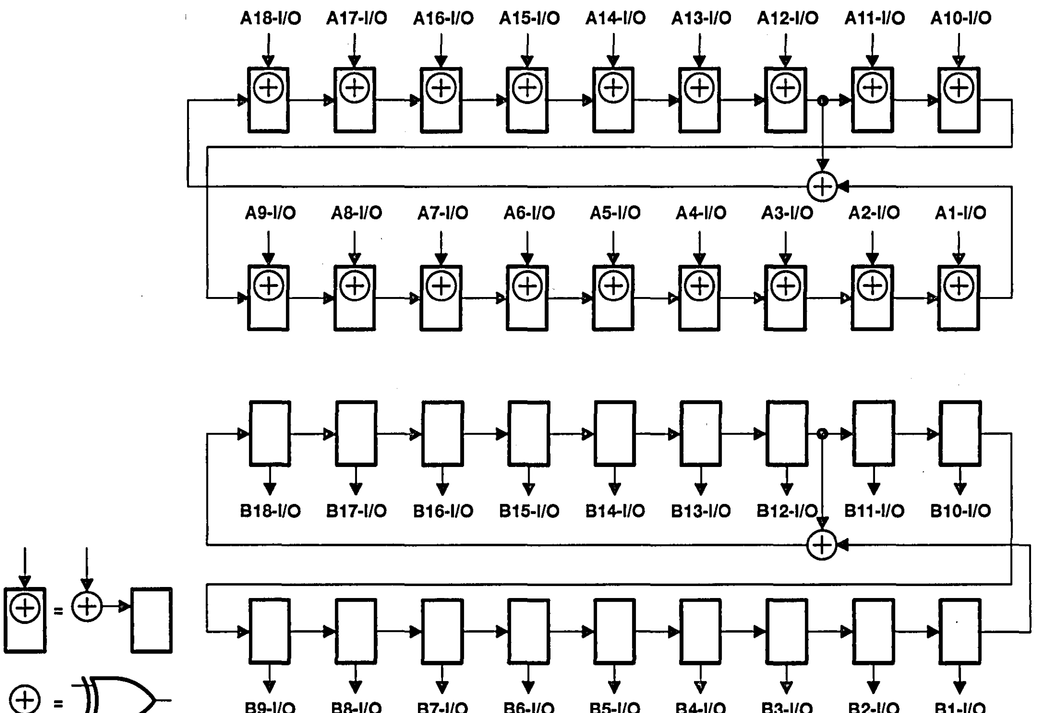


**Figure 10. 18-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

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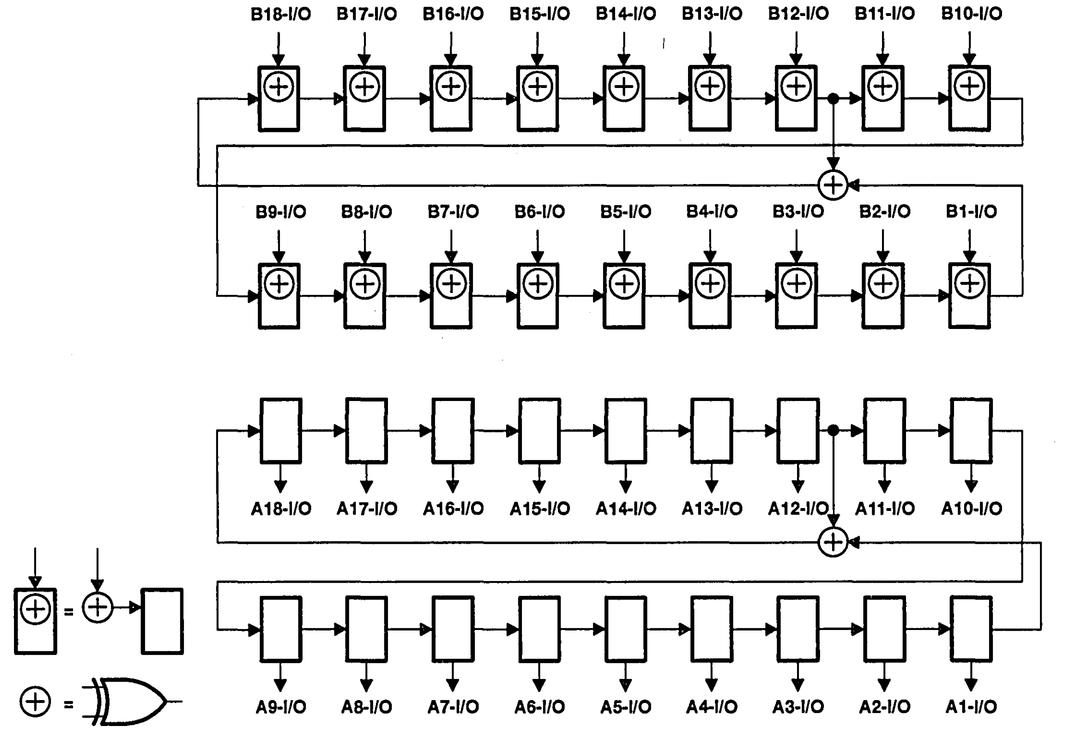


Figure 11. 18-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

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**simultaneous PSA and binary count up (PSA/COUNT)**

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 12 and 13 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

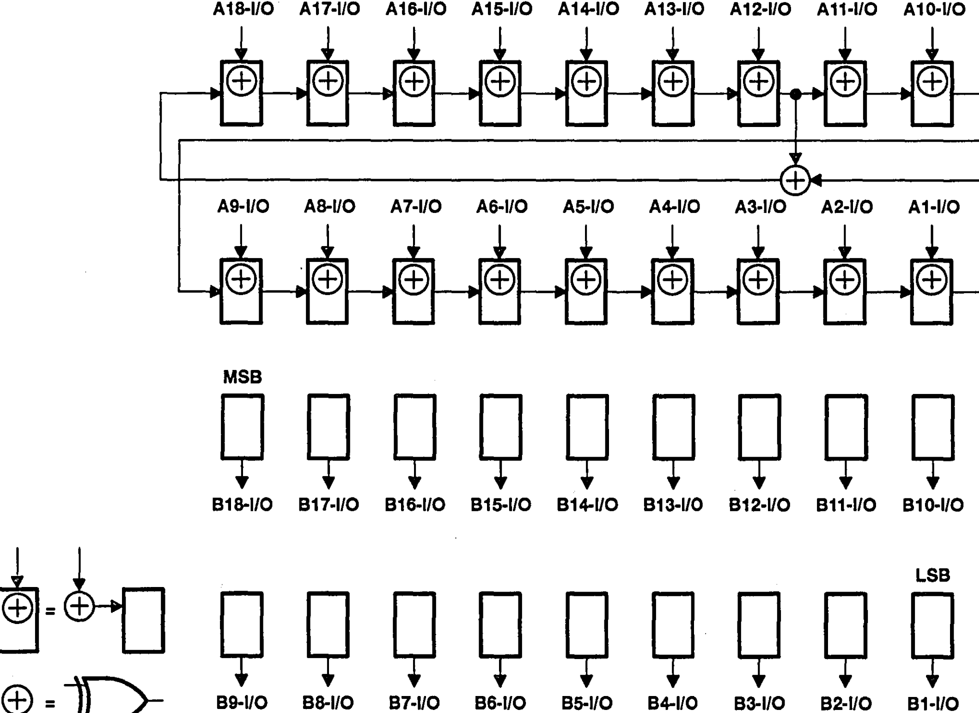


**Figure 12. 18-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

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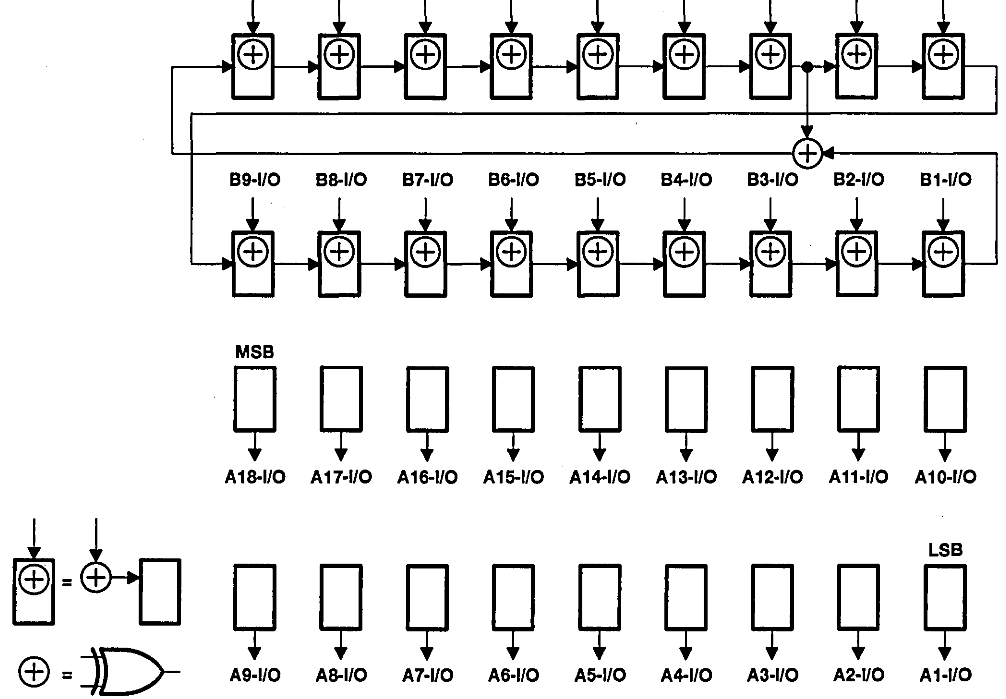


Figure 13. 18-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

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## timing description

All test operations of the 'LVTH18516 and 'LVTH182516 are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 2) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 14. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

PRODUCT PREVIEW

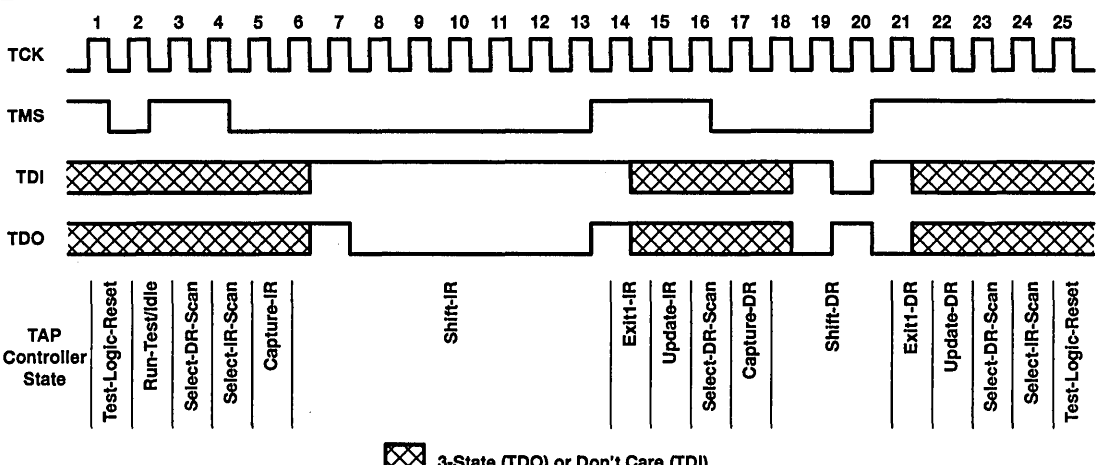


Figure 14. Timing Example

PRODUCT PREVIEW

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .......... –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .......... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) .... –0.5 V to 7 V
Current into any output in the low state, $I_O$: SN54LVTH18516 .......... 96 mA
SN54LVTH182516 (A port or TDO) .......... 96 mA
SN54LVTH182516 (B port) .......... 30 mA
SN74LVTH18516 .......... 128 mA
SN74LVTH182516 (A port or TDO) .......... 128 mA
SN74LVTH182516 (B port) .......... 30 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH18516 .......... 48 mA
SN54LVTH182516 (A port or TDO) ...... 48 mA
SN54LVTH182516 (B port) .......... 30 mA
SN74LVTH18516 .......... 64 mA
SN74LVTH182516 (A port or TDO) ...... 64 mA
SN74LVTH182516 (B port) .......... 30 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) .......... –50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) .......... –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): DGG package .......... 1 W
Storage temperature range, $T_{stg}$ .......... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book,* literature number SCBD002.

## recommended operating conditions

| | | | SN54LVTH18516 | | SN74LVTH18516 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 32 | mA |
| $I_{OL}$† | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | TEST CONDITIONS | | | SN54LVTH18516 | | | SN74LVTH18516 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 2.7 V, | $I_I$ = −18 mA | | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = −100 µA | | $V_{CC}$−0.2 | | | $V_{CC}$−0.2 | | | V |
| | $V_{CC}$ = 2.7 V, | $I_{OH}$ = −3 mA | | 2.4 | | | 2.4 | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = −8 mA | | 2.4 | | | 2.4 | | | |
| | | $I_{OH}$ = −24 mA | | 2 | | | | | | |
| | | $I_{OH}$ = −32 mA | | | | | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | | 0.2 | | | 0.2 | V |
| | | $I_{OL}$ = 24 mA | | | | 0.5 | | | 0.5 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 32 mA | | | | 0.5 | | | 0.5 | |
| | | $I_{OL}$ = 48 mA | | | | 0.55 | | | | |
| | | $I_{OL}$ = 64 mA | | | | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | CLK, $\overline{CLKEN}$, LE, S, TCK | | | ±1 | | | ±1 | µA |
| | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | | 10 | | | 10 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | $\overline{OE}$, TDI, TMS | | | 50 | | | 50 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | −25 | | −100 | −25 | | −100 | |
| | | $V_I$ = 5.5 V | A or B ports§ | | | 20 | | | 20 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | | | −5 | | | −5 | |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | A or B ports | 75 | | | 75 | | | µA |
| | | $V_I$ = 2 V | | −75 | | | −75 | | | |
| $I_{OZH}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | TDO | | | 1 | | | 1 | µA |
| $I_{OZL}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | TDO | | | −1 | | | −1 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 3 V or 0.5 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 3 V or 0.5 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs high | | | | | | 3 | mA |
| | | | Outputs low | | | | | | 30 | |
| | | | Outputs disabled | | | | | | 3 | |
| $\Delta I_{CC}$# | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | $V_I$ = 3 V or 0 | | | | 4 | | | 4 | | pF |
| $C_{io}$ | $V_O$ = 3 V or 0 | | | | 10 | | | 10 | | pF |
| $C_o$ | $V_O$ = 3 V or 0 | | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)

| | | | SN54LVTH18516 | | | | SN74LVTH18516 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | | | 0 | 100 | | | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | | 5 | | | | ns |
| | | LEAB or LEBA high or low | | | | | 4 | | | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | | 4 | | | | ns |
| | | A before LEAB↓ or B before LEBA↓, CLK high | | | | | 2 | | | | |
| | | A before LEAB↓ or B before LEBA↓, CLK low | | | | | 2 | | | | |
| | | $\overline{CLKEN}$ before CLK↑ | | | | | 3 | | | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | | | 2 | | | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | | | | 4 | | | | |
| | | CLKEN after CLK↑ | | | | | 1 | | | | |

### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)

| | | | SN54LVTH18516 | | | | SN74LVTH18516 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, CLK, $\overline{CLKEN}$, LE, $\overline{OE}$ or S before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, CLK, $\overline{CLKEN}$, LE, $\overline{OE}$ or S TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18516 | | | | SN74LVTH18516 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | | | | | 100 | | | | MHz |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 6 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6 | | | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PLH}$ | LEAB or LEBA | B or A | | | | | 2 | 9 | | | ns |
| $t_{PHL}$ | | | | | | | 2 | 9 | | | |
| $t_{PLH}$ | SAB or SBA | B or A | | | | | 2 | 9 | | | ns |
| $t_{PHL}$ | | | | | | | 2 | 9 | | | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 2 | 10 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 10 | | | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 2 | 11 | | | ns |
| $t_{PLZ}$ | | | | | | | 2 | 11 | | | |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18516 | | | | SN74LVTH18516 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 14 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 14 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.5 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 4 | 17 | | | ns |
| $t_{PZL}$ | | | | | | | 4 | 17 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 5.5 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 4 | 18 | | | ns |
| $t_{PLZ}$ | | | | | | | 4 | 17 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 7 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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## recommended operating conditions

| | | | SN54LVTH182516 | | SN74LVTH182516 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 24 | | 32 | mA |
| | | B port | | 12 | | 12 | |
| $I_{OL}$† | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | TEST CONDITIONS | | | SN54LVTH182516 | | | SN74LVTH182516 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 2.7 V, | $I_I$ = −18 mA | | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = −100 µA | A port, TDO | $V_{CC}$−0.2 | | | $V_{CC}$−0.2 | | | V |
| | $V_{CC}$ = 2.7 V, | $I_{OH}$ = −3 mA | A port, TDO | 2.4 | | | 2.4 | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = −8 mA | A port, TDO | 2.4 | | | 2.4 | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = −24 mA | A port, TDO | 2 | | | | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = −32 mA | A port, TDO | | | | 2 | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = −12 mA | B port | 2 | | | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | A port, TDO | | | 0.2 | | | 0.2 | V |
| | $V_{CC}$ = 2.7 V | $I_{OL}$ = 24 mA | A port, TDO | | | 0.5 | | | 0.5 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | A port, TDO | | | 0.4 | | | 0.4 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 32 mA | A port, TDO | | | 0.5 | | | 0.5 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 48 mA | A port, TDO | | | 0.55 | | | | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 64 mA | A port, TDO | | | | | | 0.55 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 12 mA | B port | | | 0.8 | | | 0.8 | |
| $I_I$ | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | CLK, $\overline{CLKEN}$, LE, S, TCK | | | ±1 | | | ±1 | µA |
| | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | CLK, $\overline{CLKEN}$, LE, S, TCK | | | 10 | | | 10 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | $\overline{OE}$, TDI, TMS | | | 50 | | | 50 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ | $\overline{OE}$, TDI, TMS | | | 1 | | | 1 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 0 | $\overline{OE}$, TDI, TMS | −25 | | −100 | −25 | | −100 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | A or B ports§ | | | 20 | | | 20 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ | A or B ports§ | | | 1 | | | 1 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 0 | A or B ports§ | | | −5 | | | −5 | |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | A or B ports | 75 | | | 75 | | | µA |
| | $V_{CC}$ = 3 V | $V_I$ = 2 V | A or B ports | −75 | | | −75 | | | |
| $I_{OZH}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | TDO | | | 1 | | | 1 | µA |
| $I_{OZL}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | TDO | | | −1 | | | −1 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 3 V or 0.5 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 3 V or 0.5 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs high | | | | | | 3 | mA |
| | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs low | | | | | | 30 | |
| | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs disabled | | | | | | 3 | |
| $\Delta I_{CC}$# | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ − 0.6 V, Other inputs at $V_{CC}$ or GND | | | | | 0.2 | | | 0.2 | mA |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | TEST CONDITIONS | SN54LVTH182516 | | | SN74LVTH182516 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $C_i$ | $V_I$ = 3 V or 0 | | 4 | | | 4 | | pF |
| $C_{io}$ | $V_O$ = 3 V or 0 | | 10 | | | 10 | | pF |
| $C_o$ | $V_O$ = 3 V or 0 | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)

| | | | | SN54LVTH182516 | | | | SN74LVTH182516 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | | | | 0 | 100 | | | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | | | 5 | | | | ns |
| | | LEAB or LEBA high | | | | | | 4 | | | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | | | 4 | | | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | | | | | 2 | | | | |
| | | | CLK low | | | | | 2 | | | | |
| | | CLKEN before CLK↑ | | | | | | 3 | | | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | | | | 2 | | | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | | | | | 4 | | | | |
| | | $\overline{CLKEN}$ after CLK↑ | | | | | | 1 | | | | |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)

| | | | SN54LVTH182516 | | | | SN74LVTH182516 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, CLK, $\overline{CLKEN}$, LE, $\overline{OE}$ or S before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, CLK, $\overline{CLKEN}$, $\overline{OE}$ or S after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182516 | | | | SN74LVTH182516 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | | | | | 100 | | | | MHz |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | | | | | 1.5 | 7.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7.5 | | | |
| $t_{PLH}$ | LEAB or LEBA | A or B | | | | | 2 | 9 | | | ns |
| $t_{PHL}$ | | | | | | | 2 | 9 | | | |
| $t_{PLH}$ | SAB or SBA | B or A | | | | | 2 | 10 | | | ns |
| $t_{PHL}$ | | | | | | | 2 | 10 | | | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 2 | 11 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 11 | | | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | | | | | 2 | 11 | | | ns |
| $t_{PLZ}$ | | | | | | | 2 | 11 | | | |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182516 | | | | SN74LVTH182516 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 14 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 14 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.5 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 4 | 17 | | | ns |
| $t_{PZL}$ | | | | | | | 4 | 17 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1 | 5.5 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 5.5 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 4 | 18 | | | ns |
| $t_{PLZ}$ | | | | | | | 4 | 17 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 7 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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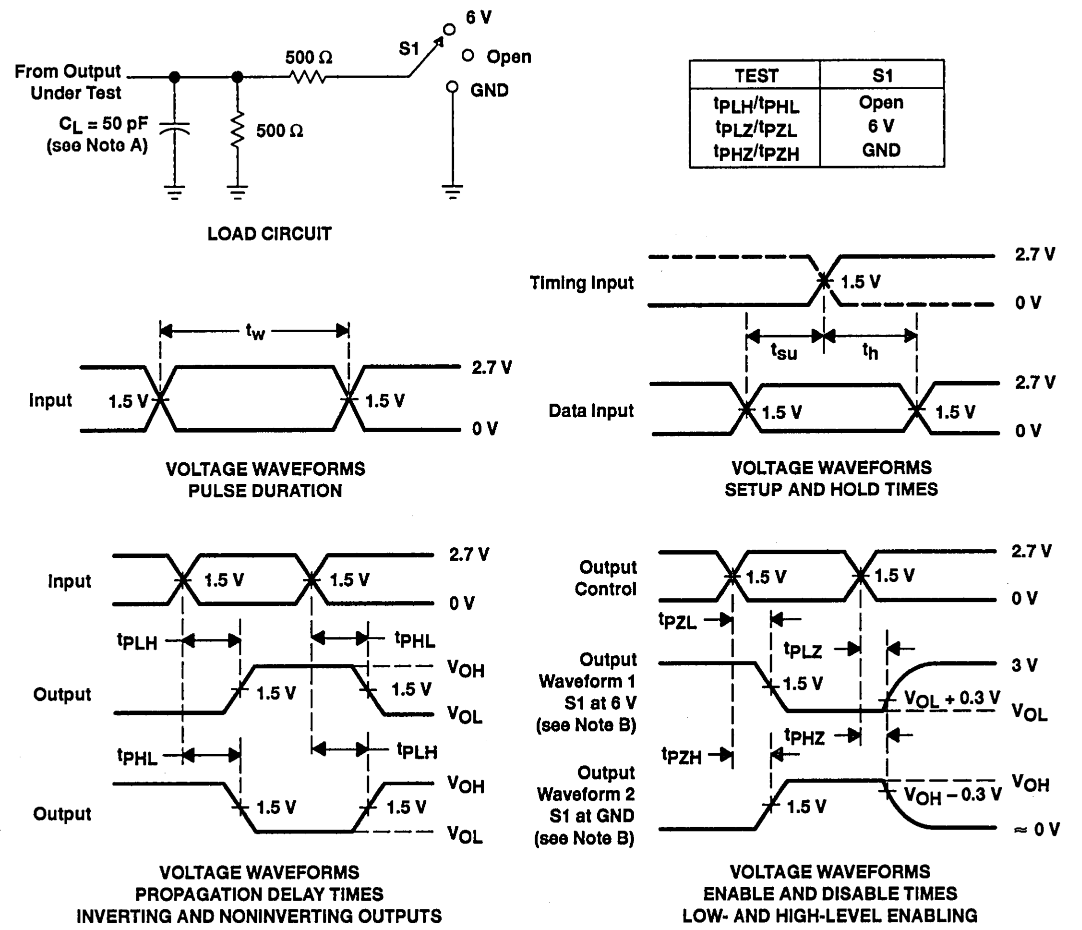
## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 15. Load Circuit and Voltage Waveforms**

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- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)
- Support Unregulated Battery Operation Down to 2.7 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- B-Port Outputs of 'LVTH182640 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages

SN54LVTH18640, SN54LVTH182640 . . . WD PACKAGE
SN74LVTH18640, SN74LVTH182640 . . . DGG OR DL PACKAGE
(TOP VIEW)

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| 1DIR | 1 | 56 | $1\overline{OE}$ |
| 1B1 | 2 | 55 | 1A1 |
| 1B2 | 3 | 54 | 1A2 |
| GND | 4 | 53 | GND |
| 1B3 | 5 | 52 | 1A3 |
| 1B4 | 6 | 51 | 1A4 |
| $V_{CC}$ | 7 | 50 | $V_{CC}$ |
| 1B5 | 8 | 49 | 1A5 |
| 1B6 | 9 | 48 | 1A6 |
| 1B7 | 10 | 47 | 1A7 |
| GND | 11 | 46 | GND |
| 1B8 | 12 | 45 | 1A8 |
| 1B9 | 13 | 44 | 1A9 |
| 2B1 | 14 | 43 | 2A1 |
| 2B2 | 15 | 42 | 2A2 |
| 2B3 | 16 | 41 | 2A3 |
| 2B4 | 17 | 40 | 2A4 |
| GND | 18 | 39 | GND |
| 2B5 | 19 | 38 | 2A5 |
| 2B6 | 20 | 37 | 2A6 |
| 2B7 | 21 | 36 | 2A7 |
| $V_{CC}$ | 22 | 35 | $V_{CC}$ |
| 2B8 | 23 | 34 | 2A8 |
| 2B9 | 24 | 33 | 2A9 |
| GND | 25 | 32 | GND |
| 2DIR | 26 | 31 | $2\overline{OE}$ |
| TDO | 27 | 30 | TDI |
| TMS | 28 | 29 | TCK |

PRODUCT PREVIEW

## description

The 'LVTH18640 and 'LVTH182640 scan test devices with 18-bit inverting bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit inverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

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## description (continued)

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at DIR. The output-enable ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVTH182640, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN74LVTH18640 and SN74LVTH182640 are available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVTH18640 and SN54LVTH182640 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH18640 and SN74LVTH182640 are characterized for operation from –40°C to 85°C.

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**FUNCTION TABLE**
**(normal mode, each 9-bit section)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | $\overline{B}$ data to A bus |
| L | H | $\overline{A}$ data to B bus |
| H | X | Isolation |

## functional block diagram

Boundary-Scan Register
1DIR 1
VCC
1OE 56
1A1 55
2 1B1
One of Nine Channels
2DIR 26
VCC
2OE 31
2A1 43
14 2B1
One of Nine Channels
Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller
VCC
TDI 30
VCC
TMS 28
TCK 29
27 TDO

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## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1DIR, 2DIR | Normal-function direction controls. See function table for normal-mode logic. |
| GND | Ground |
| $1\overline{OE}$, $2\overline{OE}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

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## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test-data registers: a 44-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

**Figure 1. TAP-Controller State Diagram**

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## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'LVTH18640 and 'LVTH182640, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 43–40 in the boundary-scan register are reset to logic 0, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

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### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'LVTH18640 and 'LVTH182640, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

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## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'LVTH18640 and 'LVTH182640. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

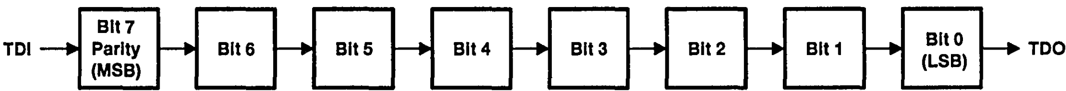


**Figure 2. Instruction Register Order of Scan**

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## data register description

### boundary-scan register

The boundary-scan register (BSR) is 44 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, one BSC for each normal-function I/O pin (one single cell for both input data and output data), and one BSC for each of the internally decoded output-enable signals (1OEA, 2OEA, 1OEB, 2OEB). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 43–40 are reset to logic 0, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

When external data is to be captured, the BSCs for signals 1OEA, 2OEA, 1OEB, and 2OEB capture logic values determined by the following positive-logic equations:

$1OEA = \overline{\overline{1OE}} \bullet \overline{1DIR}$ and $2OEA = \overline{\overline{2OE}} \bullet \overline{2DIR}$, $1OEB = \overline{\overline{1OE}} \bullet DIR$ and $2OEB = \overline{\overline{2OE}} \bullet DIR$.

When data is to be applied externally, these BSCs control the drive state (active or high impedance) of their respective outputs.

The BSR order of scan is from TDI through bits 43–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|---|---|---|---|
| 43 | 2OEB | 35 | 2A9-I/O | 26 | 1A9-I/O | 17 | 2B9-I/O | 8 | 1B9-I/O |
| 42 | 1OEB | 34 | 2A8-I/O | 25 | 1A8-I/O | 16 | 2B8-I/O | 7 | 1B8-I/O |
| 41 | 2OEA | 33 | 2A7-I/O | 24 | 1A7-I/O | 15 | 2B7-I/O | 6 | 1B7-I/O |
| 40 | 1OEA | 32 | 2A6-I/O | 23 | 1A6-I/O | 14 | 2B6-I/O | 5 | 1B6-I/O |
| 39 | 2DIR | 31 | 2A5-I/O | 22 | 1A5-I/O | 13 | 2B5-I/O | 4 | 1B5-I/O |
| 38 | 1DIR | 30 | 2A4-I/O | 21 | 1A4-I/O | 12 | 2B4-I/O | 3 | 1B4-I/O |
| 37 | $\overline{2OE}$ | 29 | 2A3-I/O | 20 | 1A3-I/O | 11 | 2B3-I/O | 2 | 1B3-I/O |
| 36 | $\overline{1OE}$ | 28 | 2A2-I/O | 19 | 1A2-I/O | 10 | 2B2-I/O | 1 | 1B2-I/O |
| — | — | 27 | 2A1-I/O | 18 | 1A1-I/O | 9 | 2B1-I/O | 0 | 1B1-I/O |

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### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

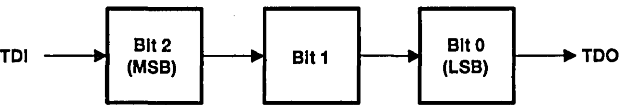


**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation.During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

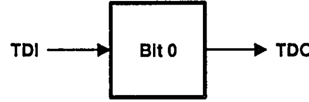


**Figure 4. Bypass Register Order of Scan**

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### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'LVTH18640, the binary value 00000000000000110000000000101111 (0003002F, hex) is captured (during Capture-DR state) in the device-identification register to identify this device as Texas Instruments SN54/74LVTH18640.

For the 'LVTH182640, the binary value 00000000000000110001000000101111 (0003102F, hex) is captured (during Capture-DR state) in the device-identification register to identify this device as Texas Instruments SN54/74LVTH182640.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

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## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'LVTH18640 and 'LVTH182640.

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### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device I/O pins is passed through the I/O BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 43–40 of the BSR). When a given output enable is active (logic 1), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

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## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 43–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 43–40 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when both bytes of the device are operating in one direction of data flow (that is, 1OEA ≠ 1OEB and 2OEA ≠ 2OEB) and in the same direction of data flow (that is, 1OEA = 2OEA and 1OEB = 2OEB). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

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**pseudo-random pattern generation (PRPG)**

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 show the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

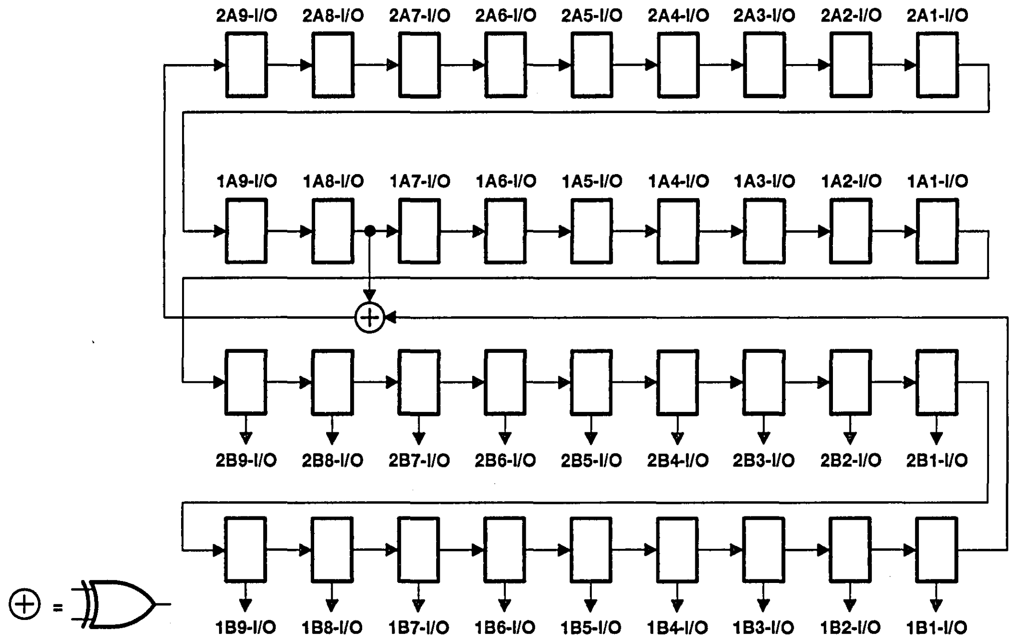


Figure 5. 36-Bit PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)

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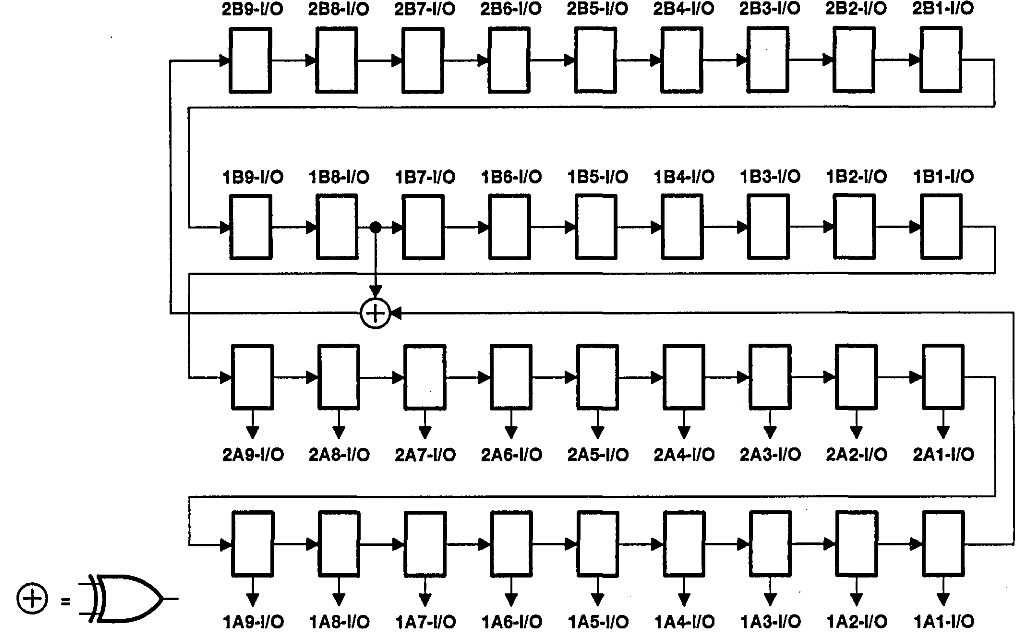


Figure 6. 36-Bit PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

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### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 show the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

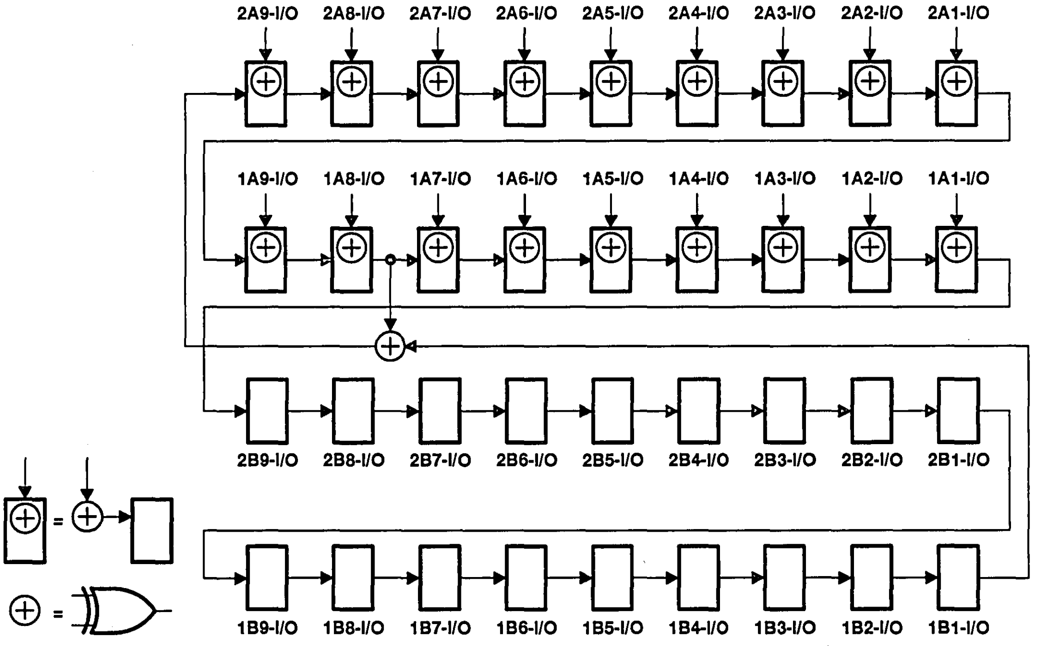


Figure 7. 36-Bit PSA Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)

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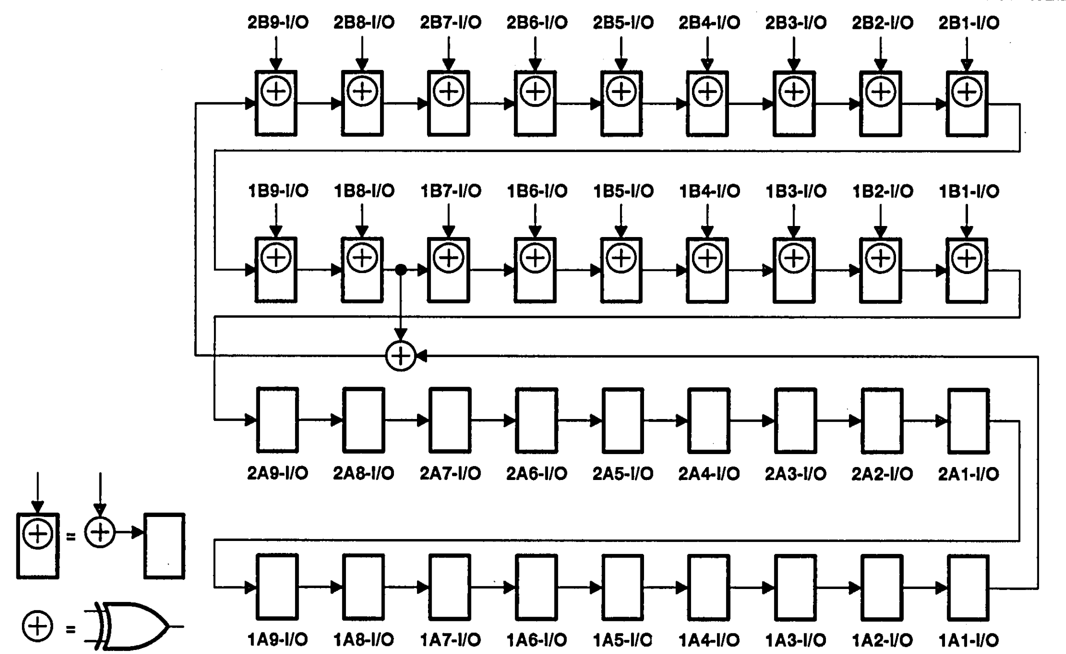


Figure 8. 36-Bit PSA Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

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### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 show the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

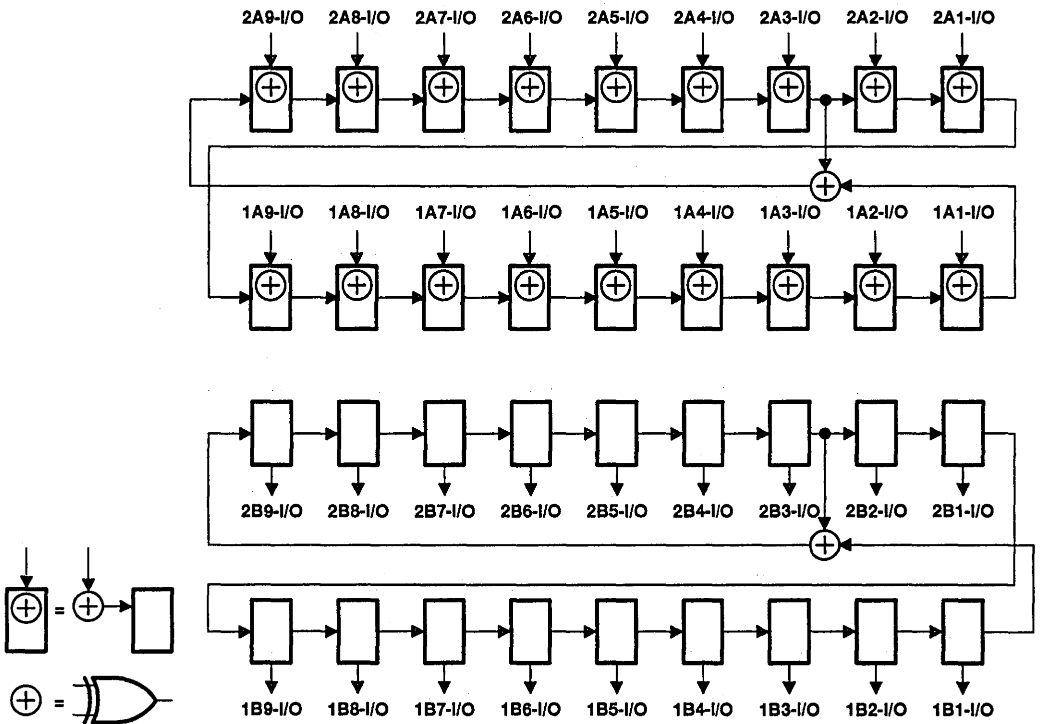


**Figure 9. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

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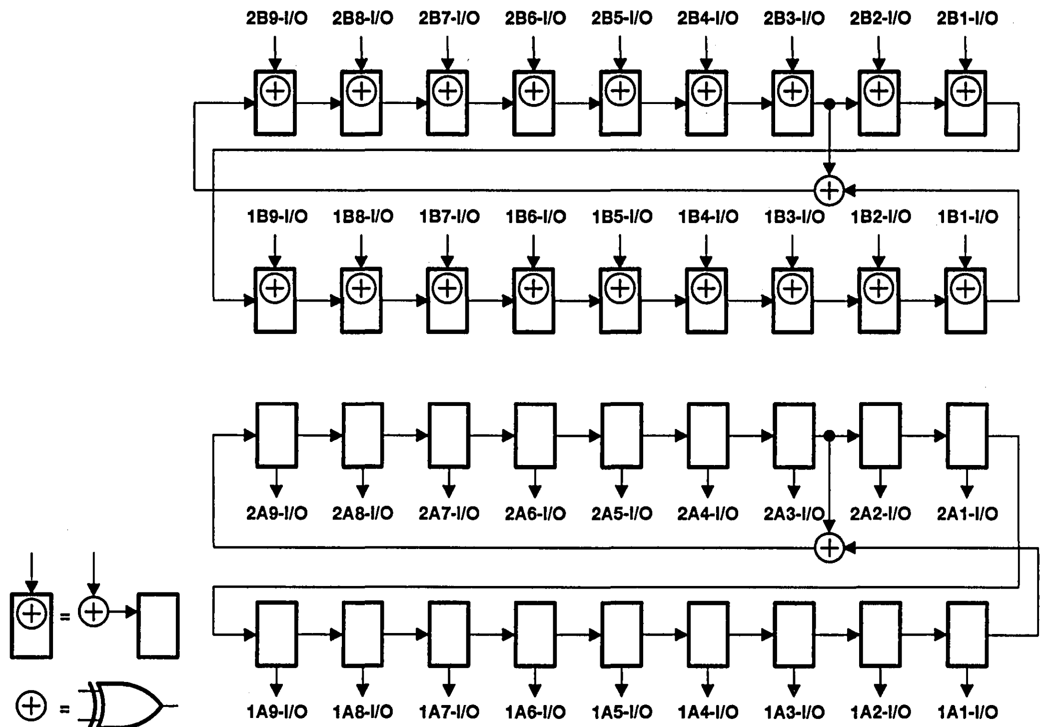


Figure 10. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

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### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 show the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

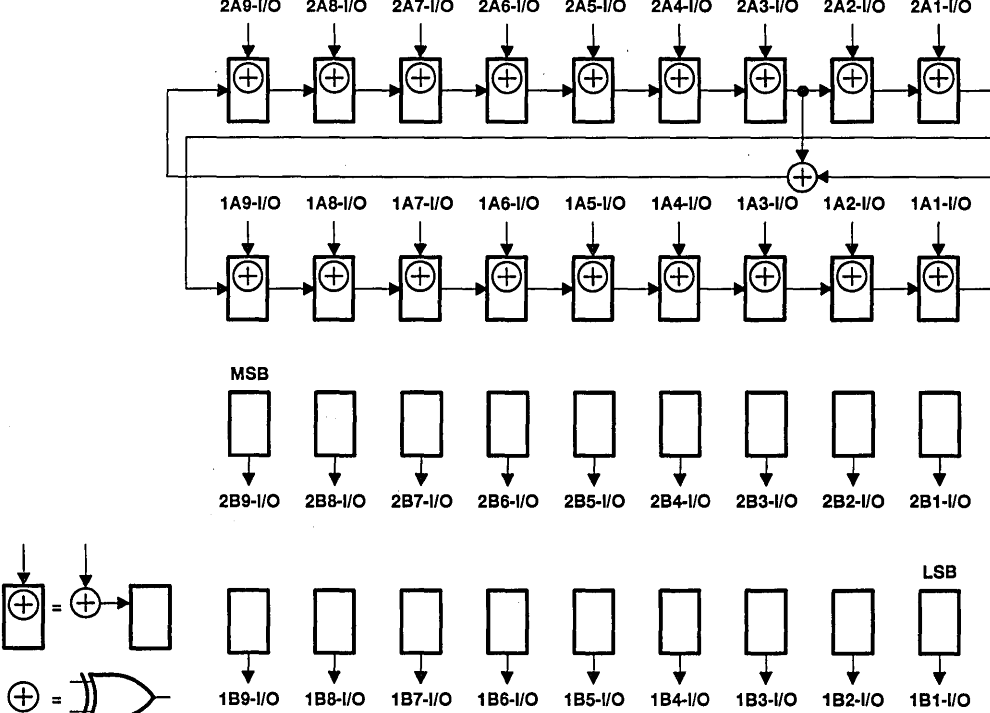


**Figure 11. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

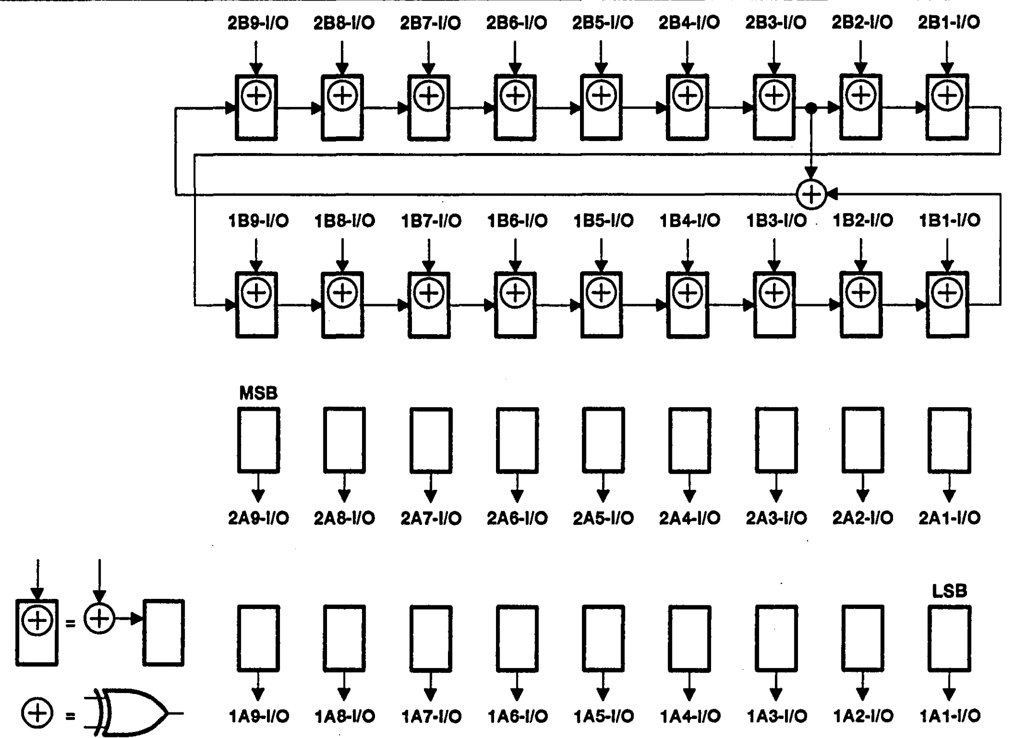


Figure 12. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

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## timing description

All test operations of the 'LVTH18640 and 'LVTH182640 are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

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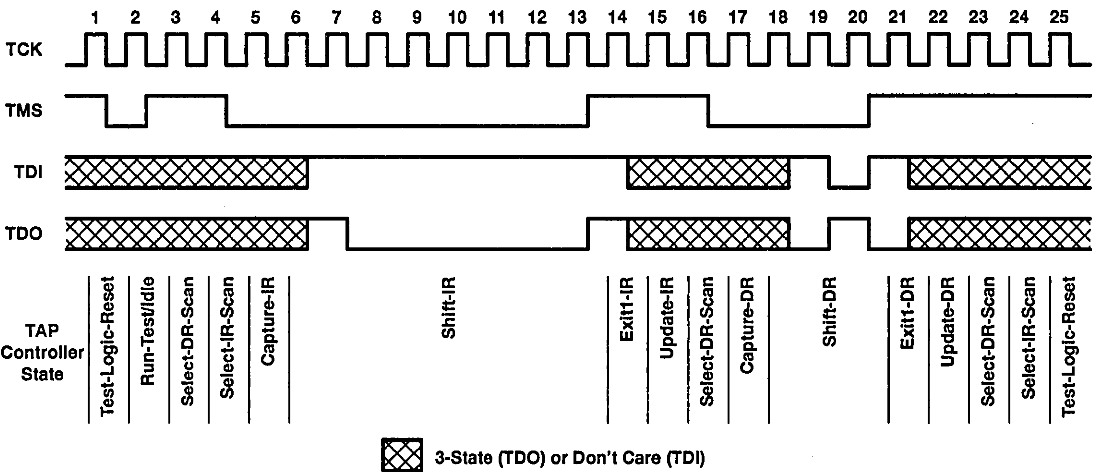


**Figure 13. Timing Example**

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ........ –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) ........ –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) .... –0.5 V to 7 V
Current into any output in the low state, $I_O$: SN54LVTH18640 ........ 96 mA
SN54LVTH182640 (A port or TDO) ........ 96 mA
SN54LVTH182640 (B port) ........ 30 mA
SN74LVTH18640 ........ 128 mA
SN74LVTH182640 (A port or TDO) ........ 128 mA
SN74LVTH182640 (B port) ........ 30 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH18640 ........ 48 mA
SN54LVTH182640 (A port or TDO) ...... 48 mA
SN54LVTH182640 (B port) ........ 30 mA
SN74LVTH18640 ........ 64 mA
SN74LVTH182640 (A port or TDO) ...... 64 mA
SN74LVTH182640 (B port) ........ 30 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) ........ –50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) ........ –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): DGG package ........ 1 W
DL package ........ 1.4 W
Storage temperature range, $T_{stg}$ ........ –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the ABT *Advanced BiCMOS Technology Data Book,* literature number SCBD002.

## recommended operating conditions

| | | | SN54LVTH18640 | | SN74LVTH18640 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 32 | mA |
| $I_{OL}$† | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH18640 | | | SN74LVTH18640 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| $I_I$ | DIR, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 50 | | | 50 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | 500 | 75 | 150 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | | –500 | –75 | –170 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | | | 1 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 2 | | | 2 | mA |
| | | | Outputs low | | | 30 | | | 30 | |
| | | | Outputs disabled | | | 2 | | | 2 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 11 | | | 11 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| | | | SN54LVTH18640 | | | | SN74LVTH18640 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, DIR, or $\overline{OE}$ before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, DIR, or $\overline{OE}$ after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18640 | | | | SN74LVTH18640 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 5.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 5.5 | | | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | | | | | 2 | 9.5 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 9.5 | | | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | | | | | 2.5 | 10.5 | | | ns |
| $t_{PLZ}$ | | | | | | | 2.5 | 9.5 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18640 | | | | SN74LVTH18640 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK↓ | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 15 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 15 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 3 | 18 | | | ns |
| $t_{PZL}$ | | | | | | | 3 | 18 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 3 | 19 | | | ns |
| $t_{PLZ}$ | | | | | | | 3 | 19 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 8 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 8 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## recommended operating conditions

| | | | SN54LVTH182640 | | SN74LVTH182640 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | A port or TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port or TDO | | 24 | | 32 | mA |
| | | B port | | 12 | | 12 | |
| $I_{OL}$† | Low-level output current | A port or TDO | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH182640 | | | SN74LVTH182640 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | A port, TDO | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| | B port | $V_{CC}$ = 3 V, | $I_{OH}$ = –12 mA | 2 | | | 2 | | | |
| $V_{OL}$ | A port, TDO | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| | B port | $V_{CC}$ = 3 V, | $I_{OL}$ = 12 mA | | | 0.8 | | | 0.8 | |
| $I_I$ | DIR, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 50 | | | 50 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | 500 | 75 | 150 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | | –500 | –75 | –170 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | | | 1 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 2 | | | 2 | mA |
| | | | Outputs low | | | 35 | | | 35 | |
| | | | Outputs disabled | | | 2 | | | 2 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 11 | | | 11 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)

| | | | SN54LVTH182640 | | | | SN74LVTH182640 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, DIR, or $\overline{OE}$ before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, DIR, or $\overline{OE}$ after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182640 | | | | SN74LVTH182640 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 6.5 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6.5 | | | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | | | | | 2 | 10 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 10 | | | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | | | | | 2.5 | 11.5 | | | ns |
| $t_{PLZ}$ | | | | | | | 2.5 | 10.5 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

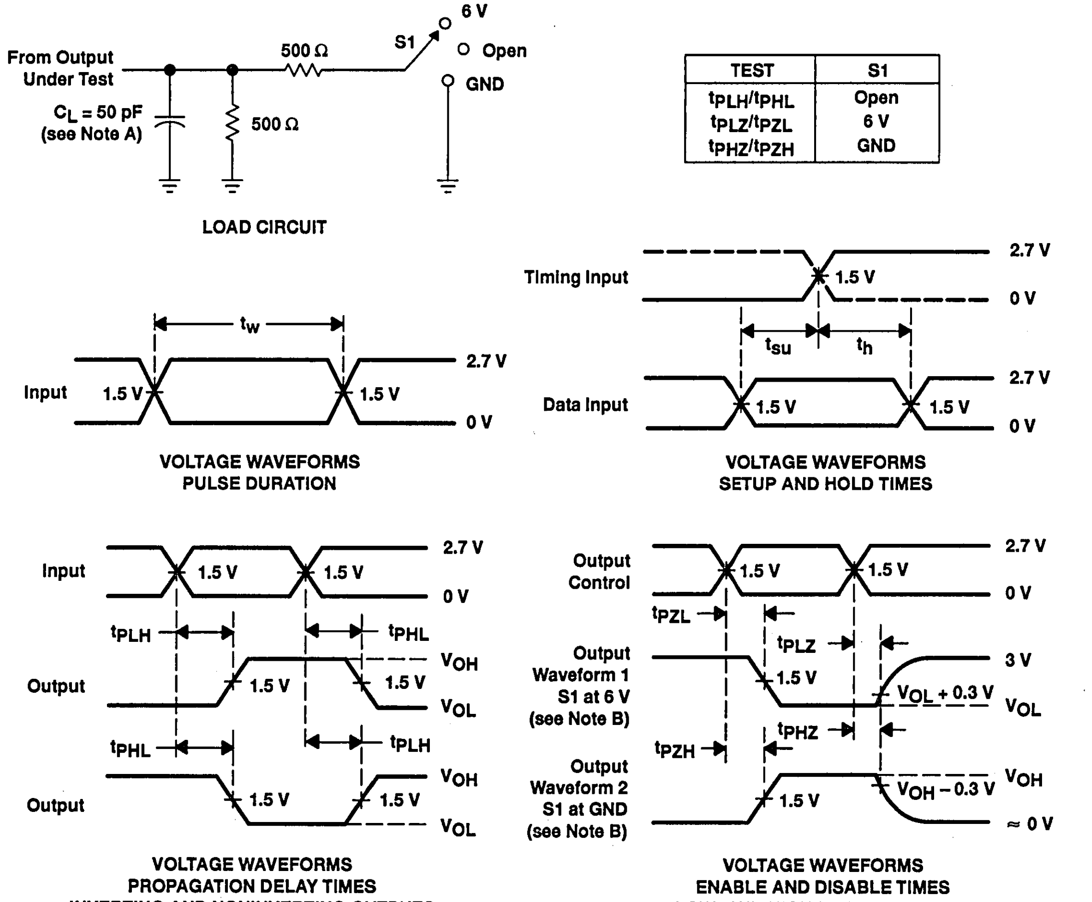
**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 14)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182640 | | | | SN74LVTH182640 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK↓ | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 15 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 15 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 3 | 18 | | | ns |
| $t_{PZL}$ | | | | | | | 3 | 18 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 3 | 19 | | | ns |
| $t_{PLZ}$ | | | | | | | 3 | 19 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 8 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 8 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

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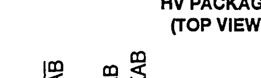
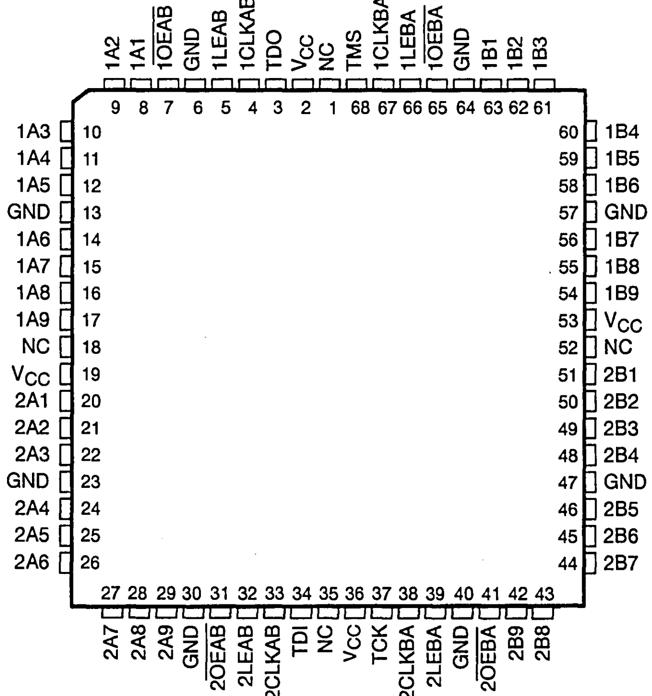
- Member of the Texas Instruments *SCOPE*™ Family of Testability Products
- Member of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

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## description

The SN54LVT18502 scan test device with 18-bit universal bus transceivers is a member of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, this device is designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, this device is an 18-bit universal bus transceiver that combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. It can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow, but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT18502 is characterized for operation over the full military temperature range of –55°C to 125°C.

**FUNCTION TABLE†**
**(normal mode, each register)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OEAB}$ | LEAB | CLKAB | A | B |
| L | L | L | X | $B_0$‡ |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | H | X | L | L |
| L | H | X | H | H |
| H | X | X | X | Z |

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established

## functional block diagram

Boundary-Scan Register
1LEAB 5
1CLKAB 4
VCC
1OEAB 7
1LEBA 66
1CLKBA 67
VCC
1OEBA 65
1A1 8
C1 1D
63 1B1
One of Nine Channels
2LEAB 32
2CLKAB 33
VCC
2OEAB 31
2LEBA 39
2CLKBA 38
VCC
2OEBA 41
2A1 20
51 2B1
One of Nine Channels
Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller
VCC
TDI 34
VCC
TMS 68
TCK 37
3 TDO

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| GND | Ground |
| 1LEAB, 1LEBA, 2LEAB, 2LEBA | Normal-function latch enables. See function table for normal-mode logic. |
| $1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. The device contains an 8-bit instruction register and four test-data registers: a 48-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device identification register.



**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite state machine that provides test-control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. TMS has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the SN54LVT18502, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–44 in the boundary-scan register are reset to logic 1, ensuring that these cells that control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked the outputs would be at the high-impedance state). Reset value of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the SN54LVT18502, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to the active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the SN54LVT18502. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

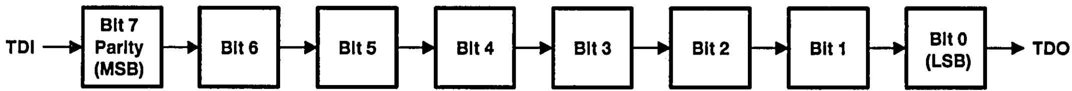


**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle, as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at the high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | $2\overline{\text{OEAB}}$ | 35 | 2A9-I/O | 17 | 2B9-I/O |
| 46 | $1\overline{\text{OEAB}}$ | 34 | 2A8-I/O | 16 | 2B8-I/O |
| 45 | $2\overline{\text{OEBA}}$ | 33 | 2A7-I/O | 15 | 2B7-I/O |
| 44 | $1\overline{\text{OEBA}}$ | 32 | 2A6-I/O | 14 | 2B6-I/O |
| 43 | 2CLKAB | 31 | 2A5-I/O | 13 | 2B5-I/O |
| 42 | 1CLKAB | 30 | 2A4-I/O | 12 | 2B4-I/O |
| 41 | 2CLKBA | 29 | 2A3-I/O | 11 | 2B3-I/O |
| 40 | 1CLKBA | 28 | 2A2-I/O | 10 | 2B2-I/O |
| 39 | 2LEAB | 27 | 2A1-I/O | 9 | 2B1-I/O |
| 38 | 1LEAB | 26 | 1A9-I/O | 8 | 1B9-I/O |
| 37 | 2LEBA | 25 | 1A8-I/O | 7 | 1B8-I/O |
| 36 | 1LEBA | 24 | 1A7-I/O | 6 | 1B7-I/O |
| — | — | 23 | 1A6-I/O | 5 | 1B6-I/O |
| — | — | 22 | 1A5-I/O | 4 | 1B5-I/O |
| — | — | 21 | 1A4-I/O | 3 | 1B4-I/O |
| — | — | 20 | 1A3-I/O | 2 | 1B3-I/O |
| — | — | 19 | 1A2-I/O | 1 | 1B2-I/O |
| — | — | 18 | 1A1-I/O | 0 | 1B1-I/O |

### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run test (RUNT) instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

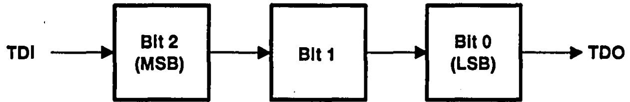


**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

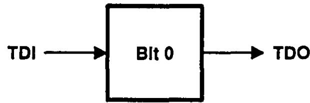


**Figure 4. Bypass Register Order of Scan**

### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the SN54LVT18502, the binary value 00010000000000011100000000101111 (1001C02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54LVT18502.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary-run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the SN54LVT18502

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–44 of the BSR). When a given output enable is active (logic 0), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0, as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 47–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 47–44 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when both bytes of the device are operating in one direction of data flow (i.e., 1$\overline{\text{OEAB}}$ ≠ 1$\overline{\text{OEBA}}$ and 2$\overline{\text{OEAB}}$ ≠ 2$\overline{\text{OEBA}}$) and in the same direction of data flow (i.e., 1$\overline{\text{OEAB}}$ = 2$\overline{\text{OEAB}}$ and 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

**pseudo-random pattern generation (PRPG)**

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 show the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

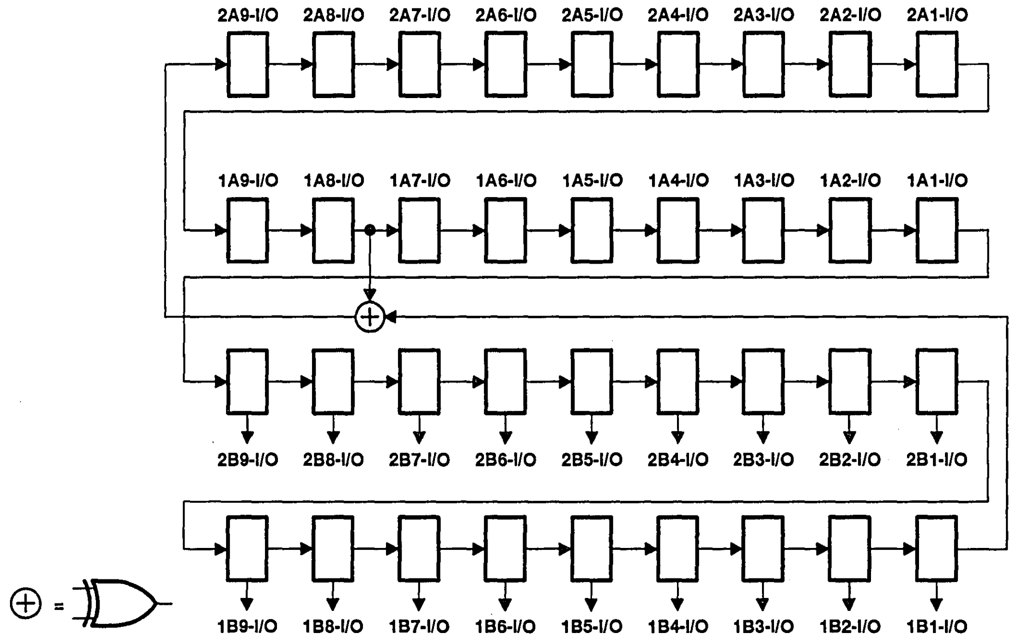


**Figure 5. 36-Bit PRPG Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 0, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 1)**

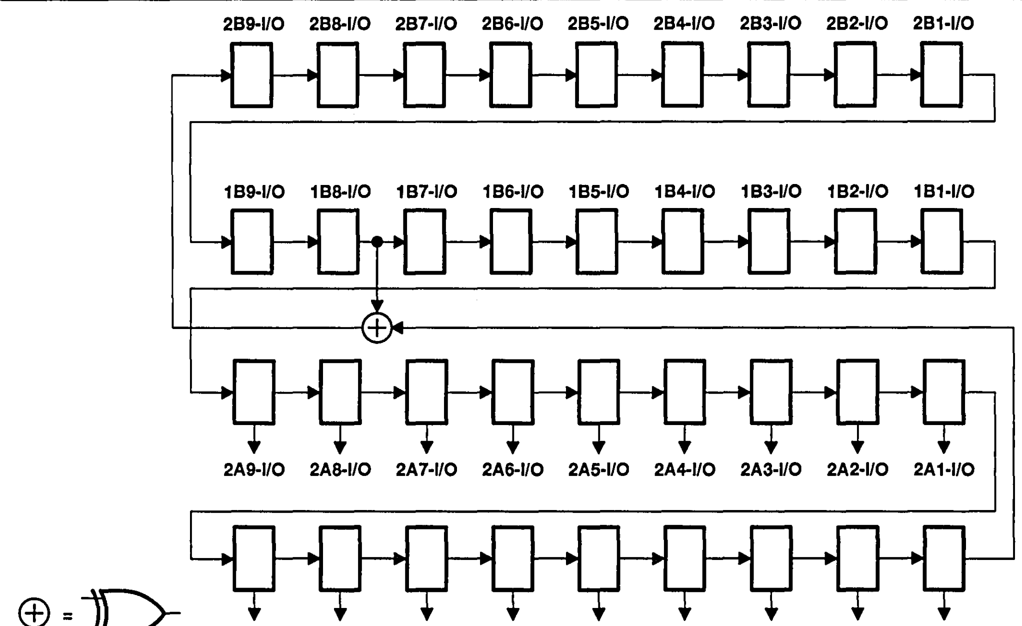


**Figure 6. 36-Bit PRPG Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)**

**parallel-signature analysis (PSA)**

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 show the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

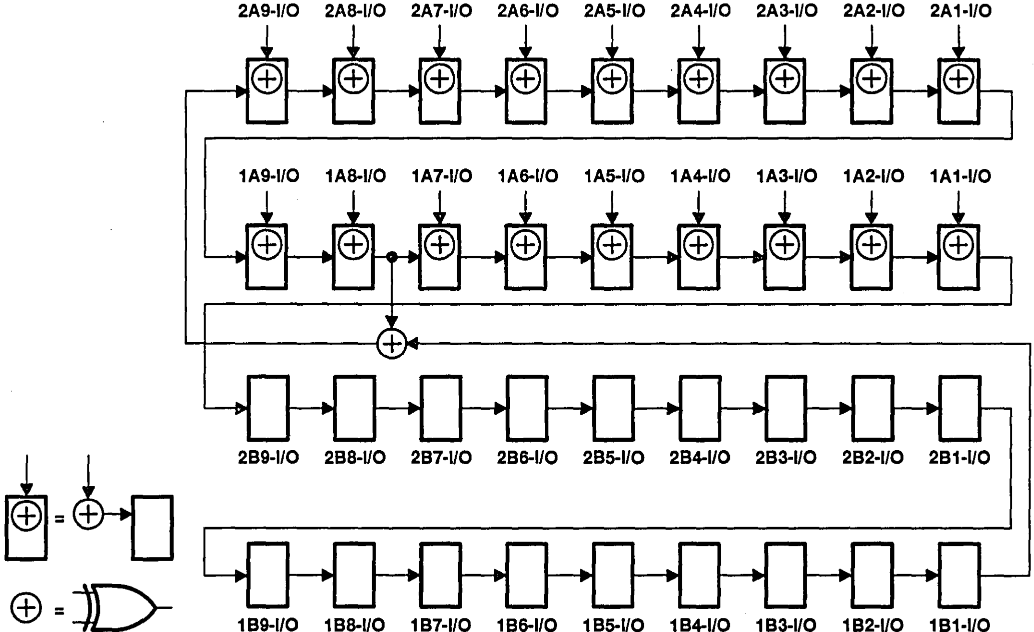


**Figure 7. 36-Bit PSA Configuration ($1\overline{OEAB}$ = $2\overline{OEAB}$ = 0, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 1)**

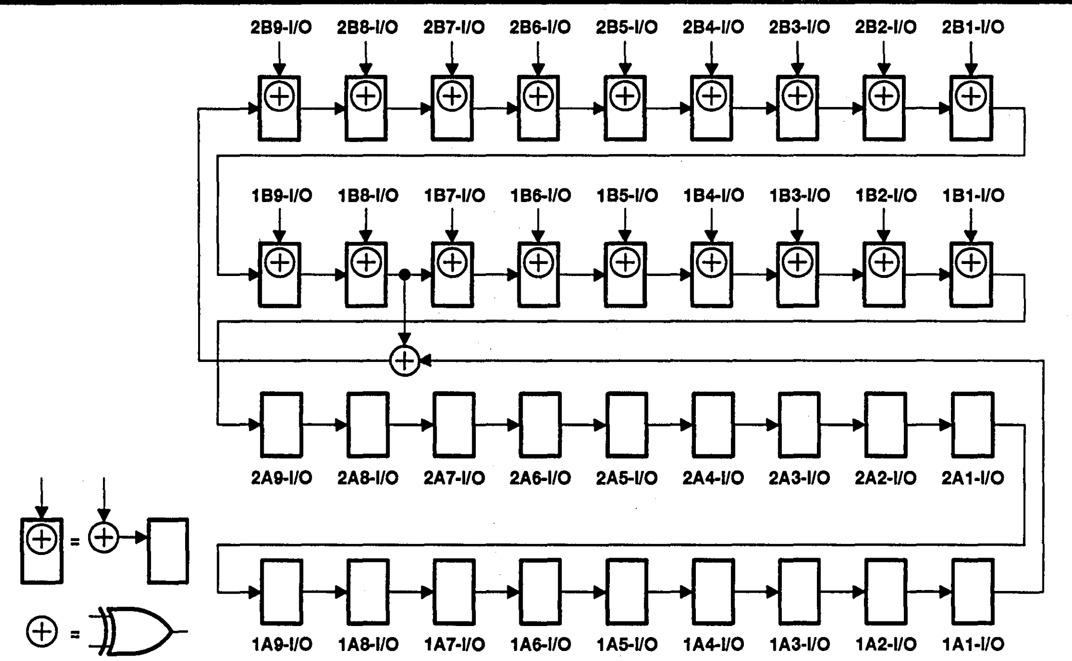


**Figure 8. 36-Bit PSA Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 show the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

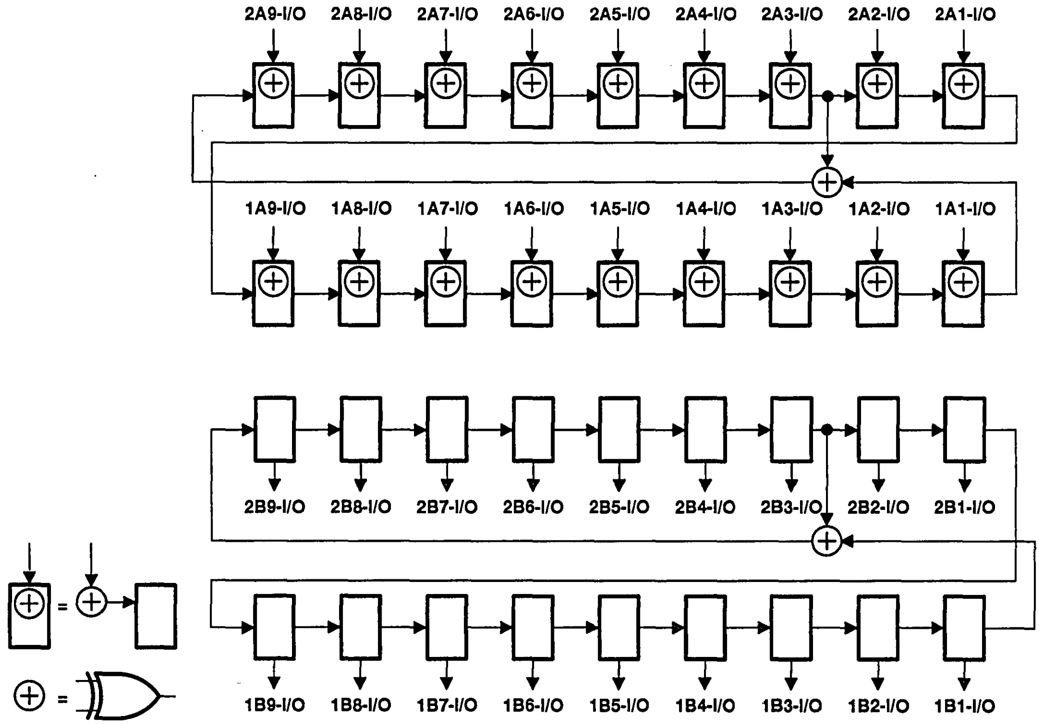


Figure 9. 18-Bit PSA/PRPG Configuration ($1\overline{OEAB} = 2\overline{OEAB} = 0$, $1\overline{OEBA} = 2\overline{OEBA} = 1$)

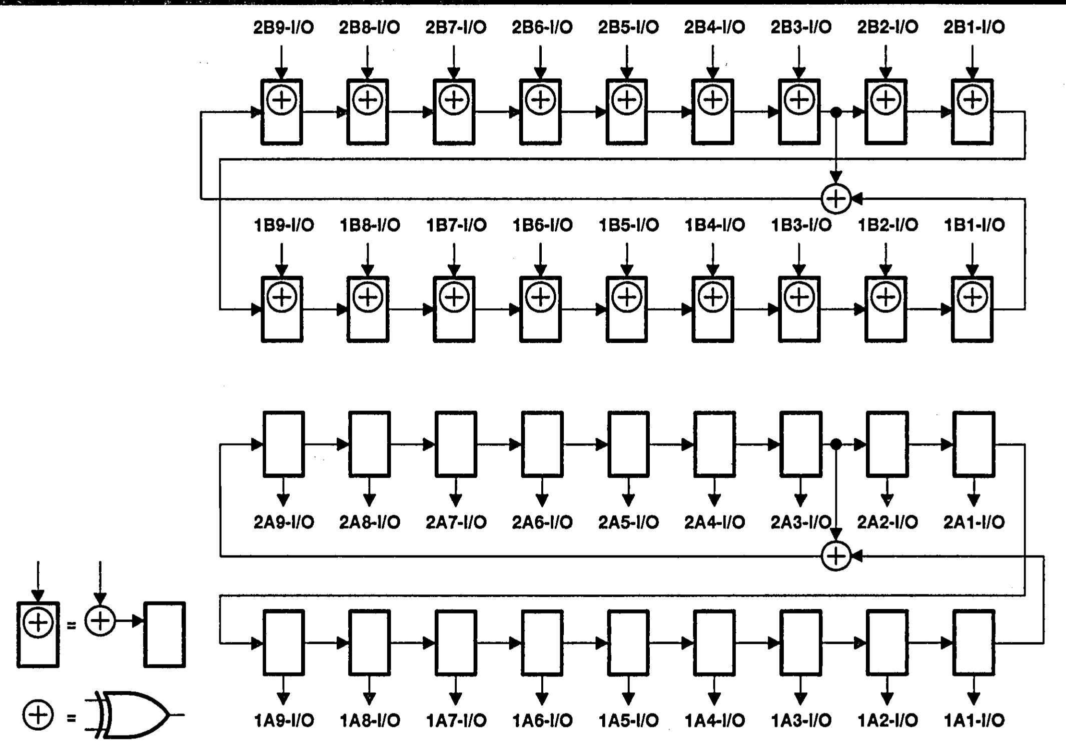


**Figure 10. 18-Bit PSA/PRPG Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 show the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

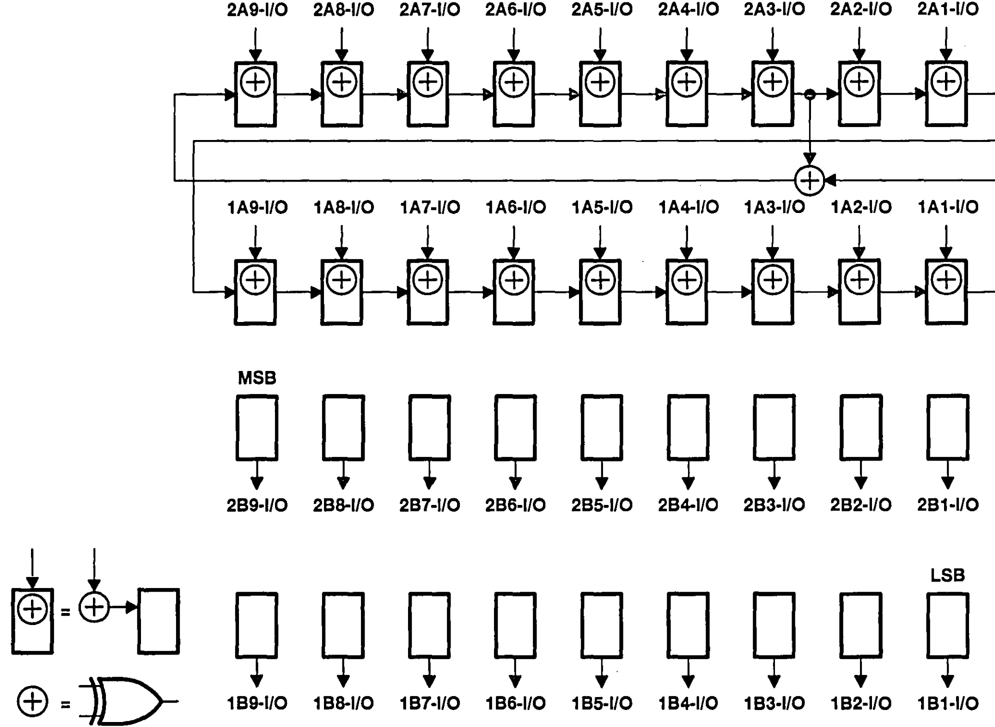


**Figure 11. 18-Bit PSA/COUNT Configuration ($1\overline{OEAB} = 2\overline{OEAB} = 0$, $1\overline{OEBA} = 2\overline{OEBA} = 1$)**

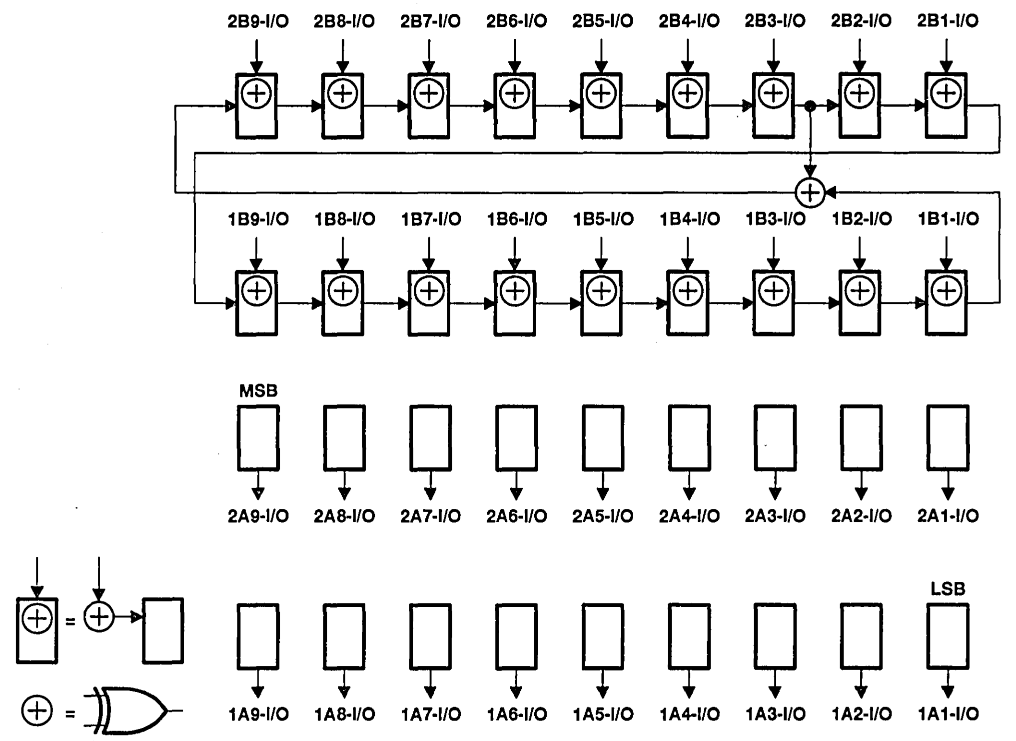


**Figure 12. 18-Bit PSA/COUNT Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)**

## timing description

All test operations of the SN54LVT18502 and are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | The selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

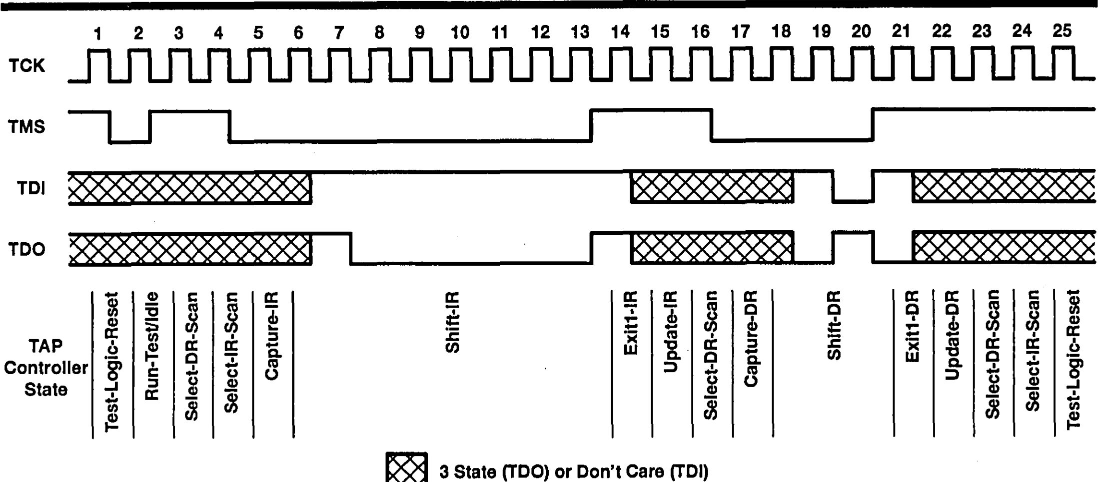


Figure 13. Timing Example

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .......... –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .......... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) .... –0.5 V to 7 V
Current into any output in the low state, $I_O$ .......... 96 mA
Current into any output in the high state, $I_O$ (see Note 2) .......... 48 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) .......... –50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) .......... –50 mA
Storage temperature range, $T_{stg}$ .......... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current only flows when the output is in the high state and $V_O > V_{CC}$.

## recommended operating conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| $I_{OL}$‡ | Low-level output current | | | 48 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | °C |

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | |
| $I_I$ | CLK, LE, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 50 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | 500 | µA |
| | | | $V_I$ = 2 V | –75 | | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 50 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –50 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.7 | 3 | mA |
| | | | Outputs low | | 21 | 30 | |
| | | | Outputs disabled | | 0.7 | 3 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 11 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 14)

| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | 0 | 90 | 0 | 80 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | 6.5 | | 6.7 | | ns |
| | | LEAB or LEBA high | | 2.4 | | 2.4 | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | 3.6 | | 4 | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | 1.2 | | 0.6 | | |
| | | | CLK low | 1.4 | | 1.5 | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | 1.2 | | 0.8 | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | 4.9 | | 5.4 | | |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 14)

| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 40 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 12 | | 14 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, LE, or $\overline{OE}$ before TCK↑ | 8 | | 9 | | ns |
| | | TDI before TCK↑ | 3.5 | | 4.5 | | |
| | | TMS before TCK↑ | 3 | | 4 | | |
| $t_h$ | Hold time | A, B, CLK, LE, or $\overline{OE}$ after TCK↑ | 1.7 | | 1.1 | | ns |
| | | TDI after TCK↑ | 1.5 | | 0.8 | | |
| | | TMS after TCK↑ | 1.5 | | 0.6 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50* | | 50* | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1* | | 1* | | µs |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 3.3 V ± 0.3 V MIN | $V_{CC}$ = 3.3 V ± 0.3 V MAX | $V_{CC}$ = 2.7 V MIN | $V_{CC}$ = 2.7 V MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | CLKAB or CLKBA | | 90 | | 80 | | MHz |
| $t_{PLH}$ | A or B | B or A | 1.5 | 6.8 | | 8.4 | ns |
| $t_{PHL}$ | | | 1.5 | 6.8 | | 8.4 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 2 | 9 | | 10 | ns |
| $t_{PHL}$ | | | 2 | 8.5 | | 9.4 | |
| $t_{PLH}$ | LEAB or LEBA | B or A | 2.5 | 10.8 | | 12.5 | ns |
| $t_{PHL}$ | | | 2.5 | 8.6 | | 9.4 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2 | 10.5 | | 11.5 | ns |
| $t_{PZL}$ | | | 2 | 11 | | 12 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 3 | 10.8 | | 11.5 | ns |
| $t_{PLZ}$ | | | 2.5 | 9.9 | | 10.6 | |

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 3.3 V ± 0.3 V MIN | $V_{CC}$ = 3.3 V ± 0.3 V MAX | $V_{CC}$ = 2.7 V MIN | $V_{CC}$ = 2.7 V MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | TCK | | 50 | | 40 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 3 | 18 | | 20 | ns |
| $t_{PHL}$ | | | 3 | 18 | | 20 | |
| $t_{PLH}$ | TCK↓ | TDO | 2 | 6.6 | | 9 | ns |
| $t_{PHL}$ | | | 2.5 | 8 | | 9 | |
| $t_{PZH}$ | TCK↓ | A or B | 5 | 20 | | 23 | ns |
| $t_{PZL}$ | | | 5 | 20 | | 23 | |
| $t_{PZH}$ | TCK↓ | TDO | 1.5 | 6.7 | | 8 | ns |
| $t_{PZL}$ | | | 2 | 7 | | 8.5 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 22 | | 24 | ns |
| $t_{PLZ}$ | | | 4 | 21 | | 23 | |
| $t_{PHZ}$ | TCK↓ | TDO | 2.5 | 8.5 | | 10 | ns |
| $t_{PLZ}$ | | | 2 | 8 | | 9.5 | |

## PARAMETER MEASUREMENT INFORMATION

From Output Under Test
$C_L$ = 50 pF (see Note A)
500 Ω
500 Ω
S1
6 V
Open
GND

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

LOAD CIRCUIT

Timing Input, 1.5 V, 2.7 V, 0 V, $t_{su}$, $t_h$, Data Input, 1.5 V, 1.5 V, 2.7 V, 0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

$t_w$, Input, 1.5 V, 1.5 V, 2.7 V, 0 V

VOLTAGE WAVEFORMS
PULSE DURATION

Input, 1.5 V, 1.5 V, 2.7 V, 0 V, $t_{PLH}$, $t_{PHL}$, Output, 1.5 V, 1.5 V, $V_{OH}$, $V_{OL}$, $t_{PHL}$, $t_{PLH}$, Output, 1.5 V, 1.5 V, $V_{OH}$, $V_{OL}$

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

Output Control, 1.5 V, 1.5 V, 2.7 V, 0 V, $t_{PZL}$, $t_{PLZ}$, Output Waveform 1 S1 at 6 V (see Note B), 1.5 V, 3 V, $V_{OL}$ + 0.3 V, $V_{OL}$, $t_{PZH}$, $t_{PHZ}$, Output Waveform 2 S1 at GND (see Note B), 1.5 V, $V_{OH}$ – 0.3 V, $V_{OH}$, ≈ 0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)
- Support Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- B-Port Outputs of 'LVTH182502A Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

## description

The 'LVTH18502A and 'LVTH182502A scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow, but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

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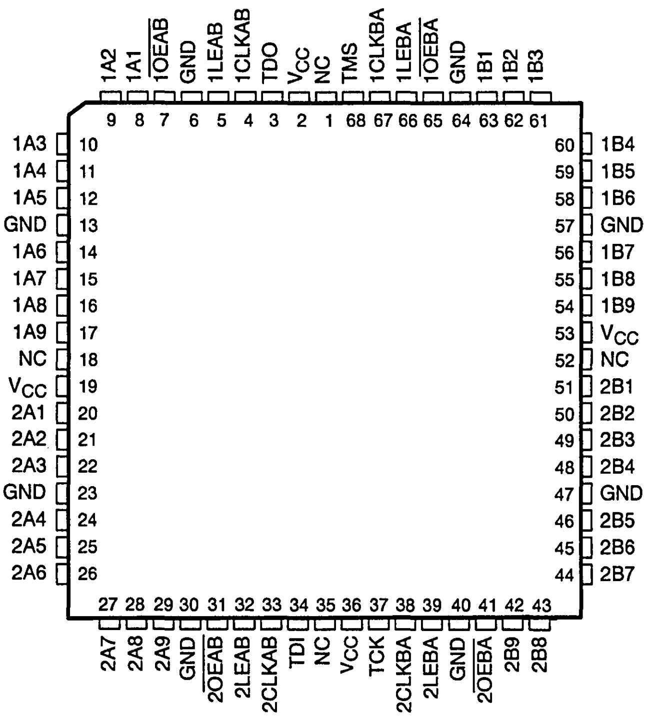
## description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

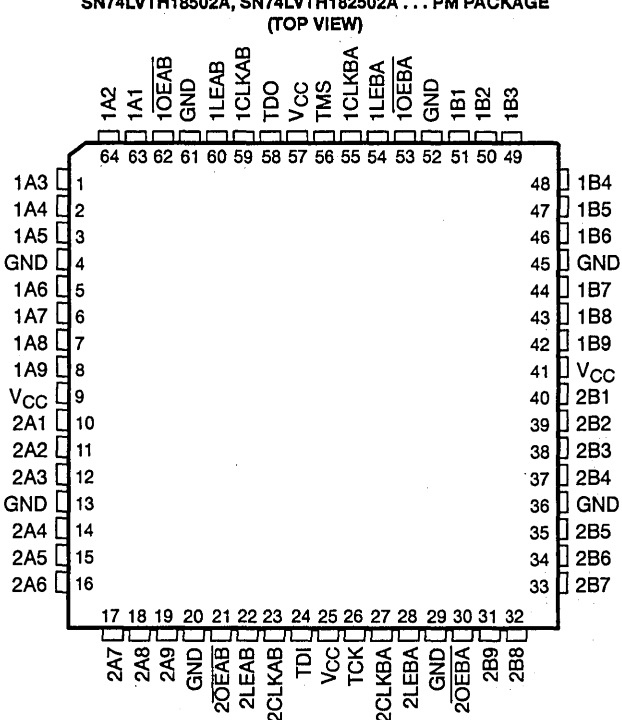
The B-port outputs of 'LVTH182502A, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54LVTH18502A and SN54LVTH182502A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH18502A and SN74LVTH182502A are characterized for operation from –40°C to 85°C.




NC – No internal connection

SN74LVTH18502A, SN74LVTH182502A . . . PM PACKAGE
(TOP VIEW)




**FUNCTION TABLE†**
**(normal mode, each register)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{\text{OEAB}}$ | LEAB | CLKAB | A | B |
| L | L | L | X | $B_0$‡ |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | H | X | L | L |
| L | H | X | H | H |
| H | X | X | X | Z |

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions are established

## functional block diagram

Boundary-Scan Register

1LEAB 60
1CLKAB 59
VCC
1OEAB 62
1LEBA 54
1CLKBA 55
VCC
1OEBA 53
1A1 63
C1 1D
51 1B1
One of Nine Channels

2LEAB 22
2CLKAB 23
VCC
2OEAB 21
2LEBA 28
2CLKBA 27
VCC
2OEBA 30
2A1 10
C1 1D
40 2B1
One of Nine Channels

Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller

VCC
TDI 24
VCC
TMS 56
TCK 26
58 TDO

Pin numbers shown are for the PM package.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| GND | Ground |
| 1LEAB, 1LEBA, 2LEAB, 2LEBA | Normal-function latch enables. See function table for normal-mode logic. |
| $1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test-data registers: a 48-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device identification register.

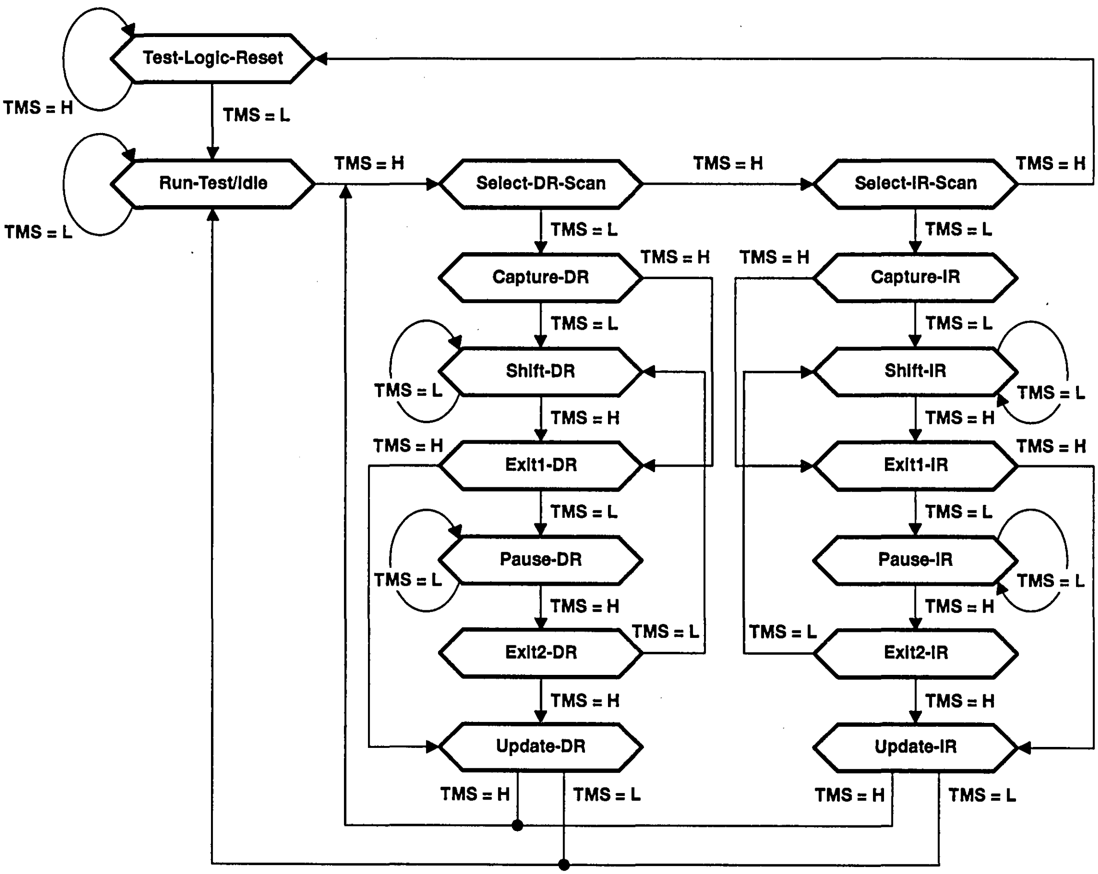



Figure 1. TAP-Controller State Diagram

## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'LVTH18502A and 'LVTH182502A, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–44 in the boundary-scan register are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked the outputs would be at the high-impedance state). Reset-value of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

**Shift-DR**

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'LVTH18502A and 'LVTH182502A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to the active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'LVTH18502A and 'LVTH182502A. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

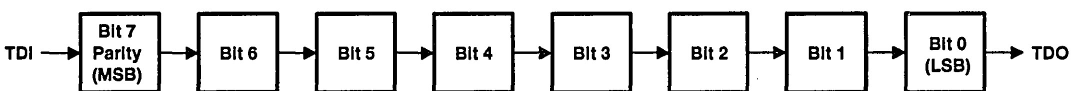



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs are set to benign values (i.e., if test mode were invoked, the outputs would be at the high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | 2$\overline{OEAB}$ | 35 | 2A9-I/O | 17 | 2B9-I/O |
| 46 | 1$\overline{OEAB}$ | 34 | 2A8-I/O | 16 | 2B8-I/O |
| 45 | 2$\overline{OEBA}$ | 33 | 2A7-I/O | 15 | 2B7-I/O |
| 44 | 1$\overline{OEBA}$ | 32 | 2A6-I/O | 14 | 2B6-I/O |
| 43 | 2CLKAB | 31 | 2A5-I/O | 13 | 2B5-I/O |
| 42 | 1CLKAB | 30 | 2A4-I/O | 12 | 2B4-I/O |
| 41 | 2CLKBA | 29 | 2A3-I/O | 11 | 2B3-I/O |
| 40 | 1CLKBA | 28 | 2A2-I/O | 10 | 2B2-I/O |
| 39 | 2LEAB | 27 | 2A1-I/O | 9 | 2B1-I/O |
| 38 | 1LEAB | 26 | 1A9-I/O | 8 | 1B9-I/O |
| 37 | 2LEBA | 25 | 1A8-I/O | 7 | 1B8-I/O |
| 36 | 1LEBA | 24 | 1A7-I/O | 6 | 1B7-I/O |
| — | — | 23 | 1A6-I/O | 5 | 1B6-I/O |
| — | — | 22 | 1A5-I/O | 4 | 1B5-I/O |
| — | — | 21 | 1A4-I/O | 3 | 1B4-I/O |
| — | — | 20 | 1A3-I/O | 2 | 1B3-I/O |
| — | — | 19 | 1A2-I/O | 1 | 1B2-I/O |
| — | — | 18 | 1A1-I/O | 0 | 1B1-I/O |

### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run test (RUNT) instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 3.

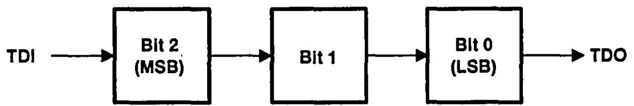



**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

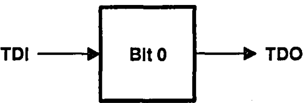



**Figure 4. Bypass Register Order of Scan**

### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'LVTH18502A, the binary value 00110000000000011100000000101111 (3001C02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74LVTH18502A.

For the 'LVTH182502A, the binary value 00110000000000100001000000101111 (3002102F, hex) is captured (during Capture-DR state) in the device-identification register to identify this device as Texas Instruments SN54/74LVTH182502A.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary-run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'LVTH18502A or 'LVTH182502A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–44 of the BSR). When a given output enable is active (logic 0), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

### control boundary to high impedance

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

### control boundary to 1/0

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

### boundary-run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

### boundary read

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

### boundary self test

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

### boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

### boundary-control-register scan

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0, as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 47–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 47–44 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when both bytes of the device are operating in one direction of data flow (i.e., $1\overline{OEAB} \neq 1\overline{OEBA}$ and $2\overline{OEAB} \neq 2\overline{OEBA}$) and in the same direction of data flow (i.e., $1\overline{OEAB} = 2\overline{OEAB}$ and $1\overline{OEBA} = 2\overline{OEBA}$). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 show the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

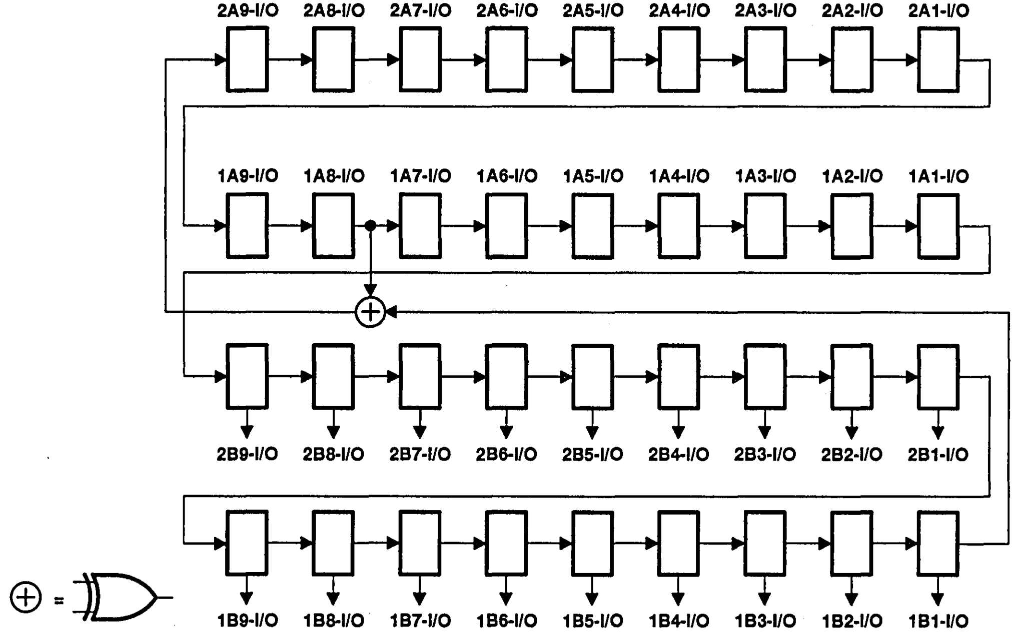



**Figure 5. 36-Bit PRPG Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 0, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 1)**

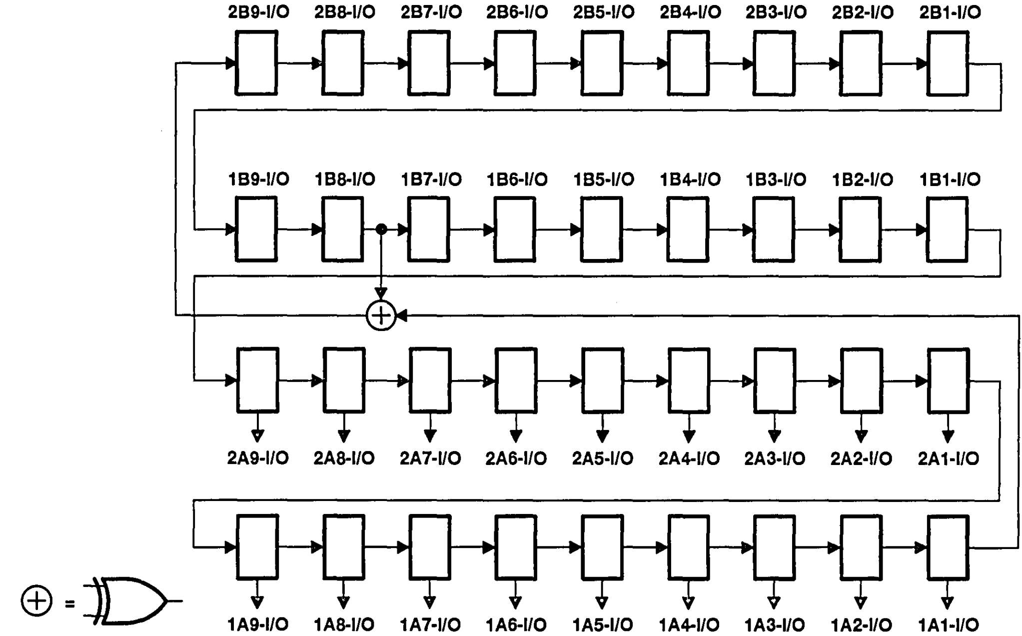



**Figure 6. 36-Bit PRPG Configuration ($1\overline{OEAB}$ = $2\overline{OEAB}$ = 1, $1\overline{CEBA}$ = $2\overline{OEBA}$ = 0)**

**parallel-signature analysis (PSA)**

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 show the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

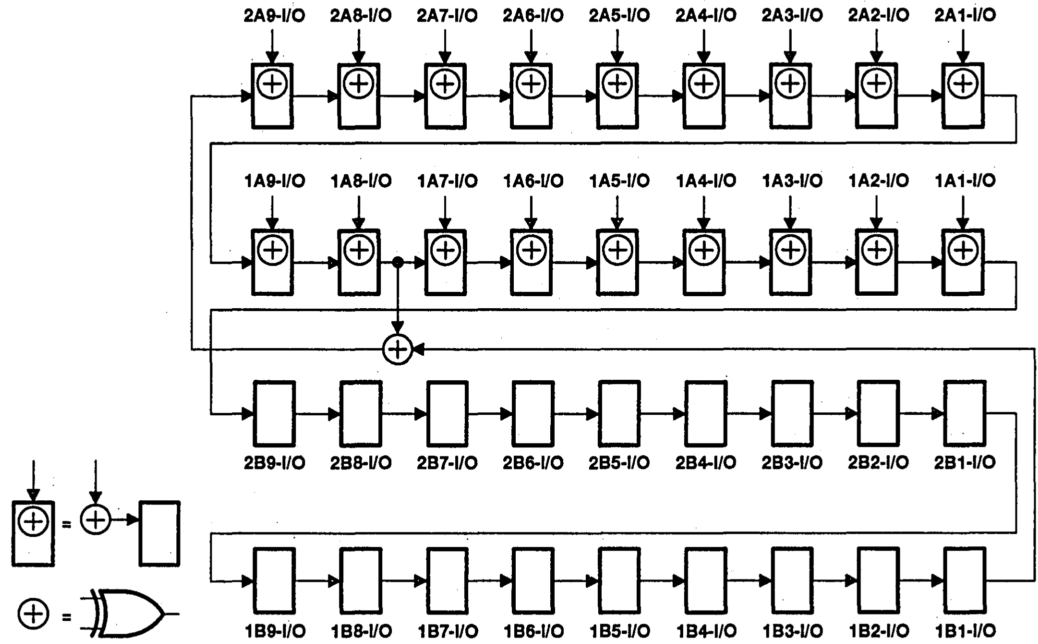



**Figure 7. 36-Bit PSA Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 0, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 1)**

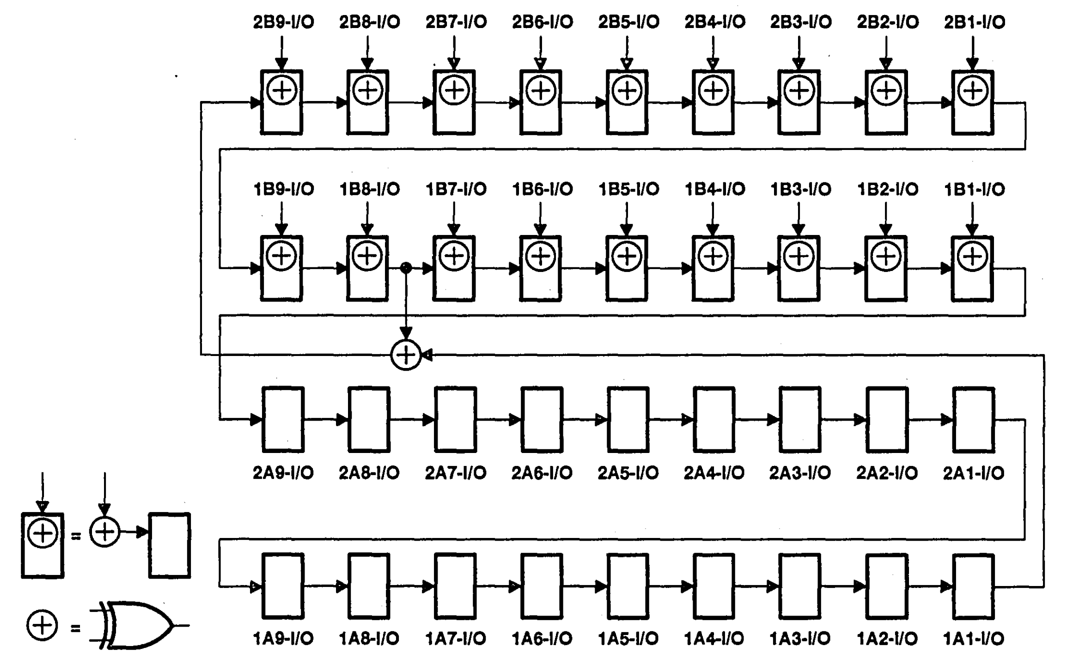



Figure 8. 36-Bit PSA Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 show the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

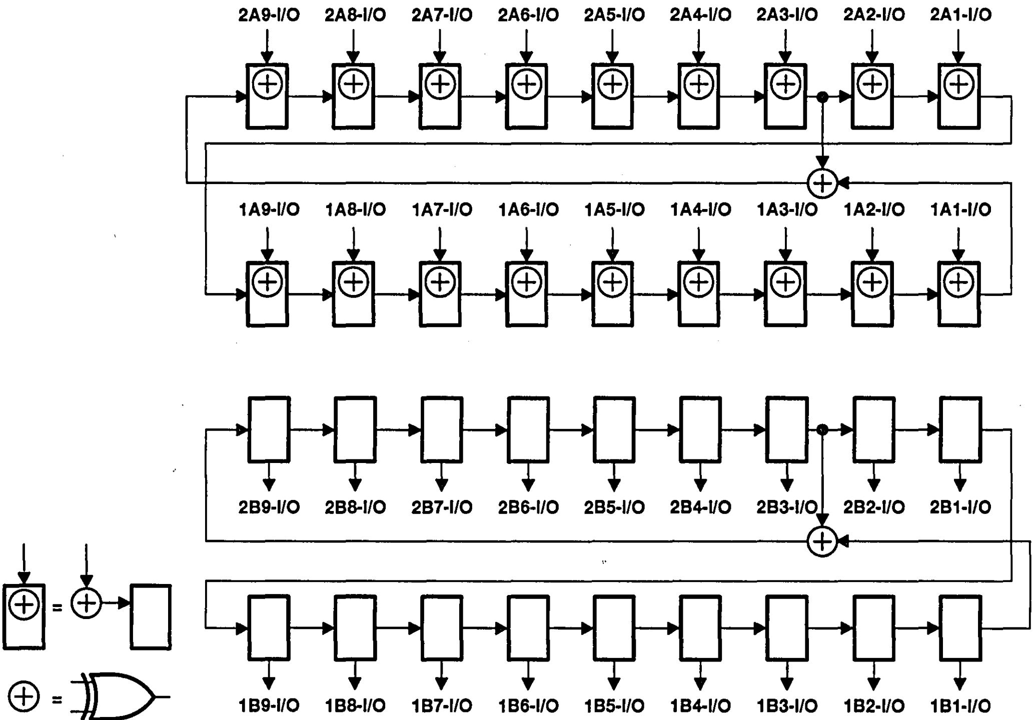



**Figure 9. 18-Bit PSA/PRPG Configuration ($1\overline{OEAB} = 2\overline{OEAB} = 0$, $1\overline{OEBA} = 2\overline{OEBA} = 1$)**

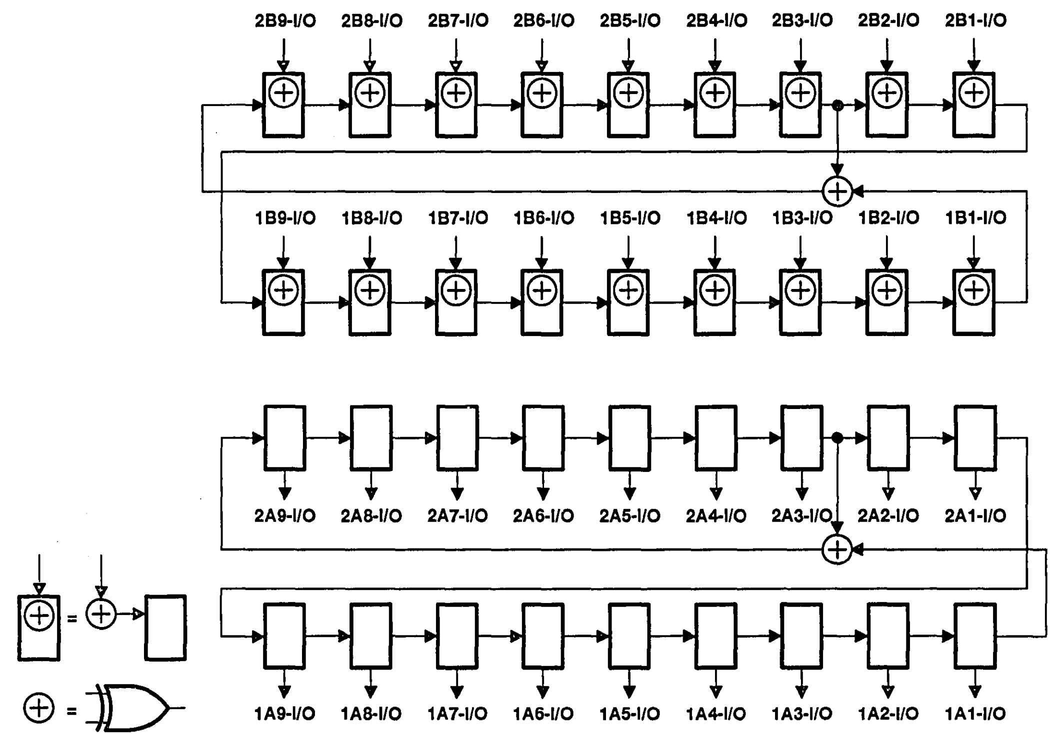



Figure 10. 18-Bit PSA/PRPG Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 show the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

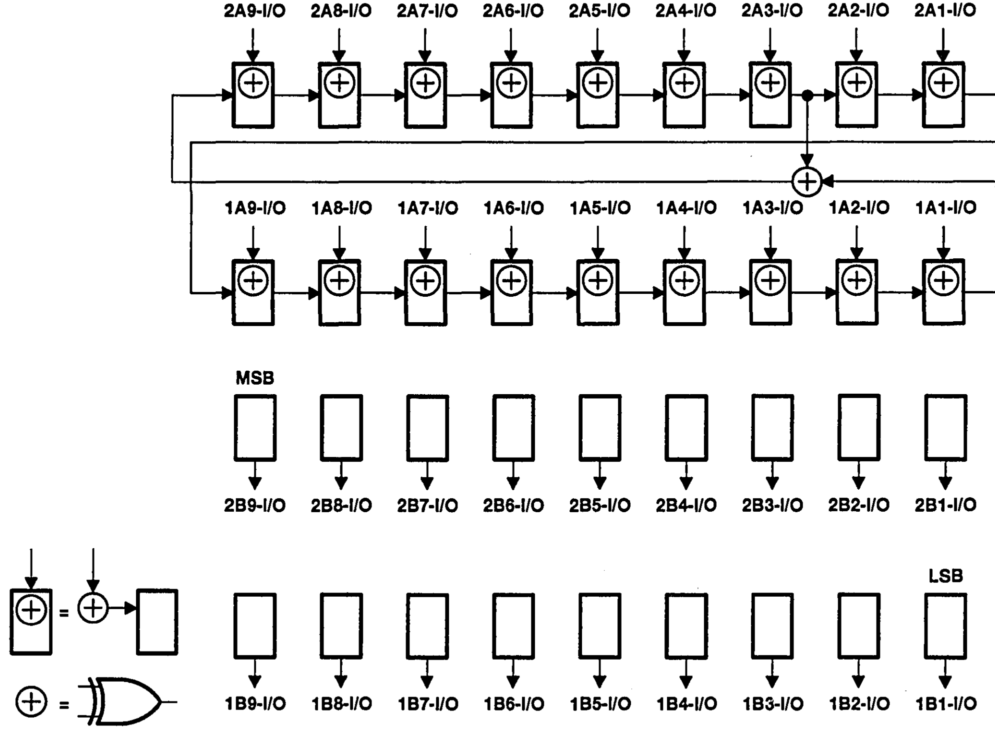



**Figure 11. 18-Bit PSA/COUNT Configuration ($1\overline{OEAB} = 2\overline{OEAB} = 0$, $1\overline{OEBA} = 2\overline{OEBA} = 1$)**

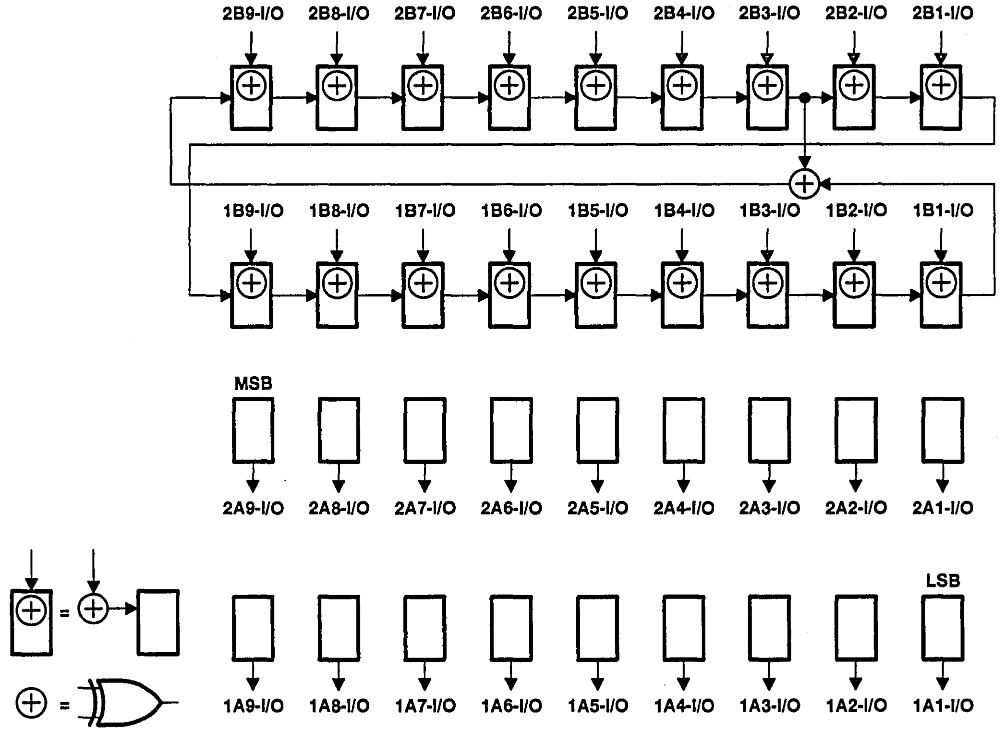



**Figure 12. 18-Bit PSA/COUNT Configuration (1$\overline{OEAB}$ = 2$\overline{OEAB}$ = 1, 1$\overline{OEBA}$ = 2$\overline{OEBA}$ = 0)**

## timing description

All test operations of the 'LVTH18502A and 'LVTH182502A are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, as necessary, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | The selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

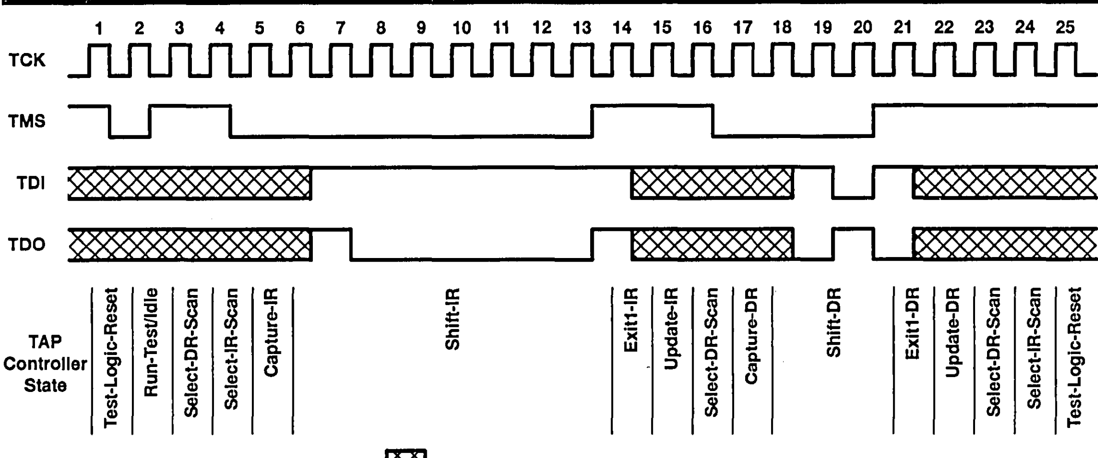



**Figure 13. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .......... –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .......... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) .......... –0.5 V to 7 V
Current into any output in the low state, $I_O$: SN54LVTH18502A .......... 96 mA
SN54LVTH182502A (A port or TDO) .......... 96 mA
SN54LVTH182502A (B port) .......... 30 mA
SN74LVTH18502A .......... 128 mA
SN74LVTH182502A (A port or TDO) .......... 128 mA
SN74LVTH182502A (B port) .......... 30 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH18502A .......... 48 mA
SN54LVTH182502A (A port or TDO) .......... 48 mA
SN54LVTH182502A (B port) .......... 30 mA
SN74LVTH18502A .......... 64 mA
SN74LVTH182502A (A port or TDO) .......... 64 mA
SN74LVTH182502A (B port) .......... 30 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) .......... –50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) .......... –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): PM package .......... 1 W
Storage temperature range, $T_{stg}$ .......... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current only flows when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54LVTH18502A | | SN74LVTH18502A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 32 | mA |
| $I_{OL}$† | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH18502A | | | SN74LVTH18502A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| $I_I$ | CLK, LE, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 5 | | | 5 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | 500 | 75 | 150 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | | –500 | –75 | –150 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | | | 1 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.6 | 2 | | 0.6 | 2 | mA |
| | | | Outputs low | | 18 | 24 | | 18 | 24 | |
| | | | Outputs disabled | | 0.6 | 2 | | 0.6 | 2 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.5 | | | 0.5 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 10 | | | 10 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

PRODUCT PREVIEW

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### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 14)

| | | | | SN54LVTH18502A | | | | SN74LVTH18502A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | 0 | 100 | 0 | 80 | 0 | 100 | 0 | 80 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | 4.4 | | 5.6 | | 4.4 | | 5.6 | | ns |
| | | LEAB or LEBA high | | 3 | | 3 | | 3 | | 3 | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | 2.8 | | 3 | | 2.8 | | 3 | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | 1.5 | | 0.7 | | 1.5 | | 0.7 | | |
| | | | CLK low | 1.6 | | 1.6 | | 1.6 | | 1.6 | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | 1.4 | | 1.1 | | 1.4 | | 1.1 | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | 3.1 | | 3.5 | | 3.1 | | 3.5 | | |

PRODUCT PREVIEW

### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 14)

| | | | SN54LVTH18502A | | | | SN74LVTH18502A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 40 | 0 | 50 | 0 | 40 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 9.5 | | 10.5 | | 9.5 | | 10.5 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, LE, or $\overline{OE}$ before TCK↑ | 6.5 | | 7 | | 6.5 | | 7 | | ns |
| | | TDI before TCK↑ | 2.5 | | 3.5 | | 2.5 | | 3.5 | | |
| | | TMS before TCK↑ | 2.5 | | 3.5 | | 2.5 | | 3.5 | | |
| $t_h$ | Hold time | A, B, CLK, LE, or $\overline{OE}$ after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | ns |
| | | TDI after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | 1 | | 1 | | μs |

PRODUCT PREVIEW

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## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18502A | | | | SN74LVTH18502A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | | 80 | | 100 | | 80 | | MHz |
| $t_{PLH}$ | A or B | B or A | 1.5 | 5.1 | | 5.8 | 1.5 | 4.9 | | 5.6 | ns |
| $t_{PHL}$ | | | 1.5 | 5.1 | | 5.8 | 1.5 | 4.9 | | 5.6 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 1.5 | 6.3 | | 7.2 | 1.5 | 5.8 | | 6.8 | ns |
| $t_{PHL}$ | | | 1.5 | 6.3 | | 7.2 | 1.5 | 5.8 | | 6.8 | |
| $t_{PLH}$ | LEAB or LEBA | B or A | 1.5 | 7.8 | | 9.2 | 1.5 | 7.4 | | 8.4 | ns |
| $t_{PHL}$ | | | 1.5 | 6 | | 6.6 | 1.5 | 5.7 | | 6.4 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 1.5 | 7.6 | | 8.5 | 1.5 | 7.1 | | 8.3 | ns |
| $t_{PZL}$ | | | 1.5 | 7.6 | | 8.5 | 1.5 | 7.1 | | 8.3 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2.5 | 8.3 | | 8.8 | 2.5 | 7.8 | | 8.4 | ns |
| $t_{PLZ}$ | | | 2.5 | 8.3 | | 8.8 | 2.5 | 7.8 | | 8.4 | |

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18502A | | | | SN74LVTH18502A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | | 40 | | 50 | | 40 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 15 | | 18 | 2.5 | 14 | | 17 | ns |
| $t_{PHL}$ | | | 2.5 | 15 | | 18 | 2.5 | 14 | | 17 | |
| $t_{PLH}$ | TCK↓ | TDO | 1 | 6 | | 7 | 1 | 5.5 | | 6.5 | ns |
| $t_{PHL}$ | | | 1.5 | 7 | | 8 | 1.5 | 6.5 | | 7.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 18 | | 21 | 4 | 17 | | 20 | ns |
| $t_{PZL}$ | | | 4 | 18 | | 21 | 4 | 17 | | 20 | |
| $t_{PZH}$ | TCK↓ | TDO | 1 | 6 | | 7 | 1 | 5.5 | | 6.5 | ns |
| $t_{PZL}$ | | | 1.5 | 6 | | 7 | 1.5 | 5.5 | | 6.5 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 19 | | 21 | 4 | 18 | | 20 | ns |
| $t_{PLZ}$ | | | 4 | 18 | | 19.5 | 4 | 17 | | 18.5 | |
| $t_{PHZ}$ | TCK↓ | TDO | 1.5 | 7.5 | | 9 | 1.5 | 7 | | 8.5 | ns |
| $t_{PLZ}$ | | | 1.5 | 7.5 | | 8.5 | 1.5 | 7 | | 8 | |

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## recommended operating conditions

| | | | SN54LVTH182502A | | SN74LVTH182502A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 24 | | 32 | mA |
| | | B port | | 12 | | 12 | |
| $I_{OL}$† | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH182502A | | | SN74LVTH182502A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | A, B, TDO | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | A port, TDO | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| | B port | $V_{CC}$ = 3 V, | $I_{OH}$ = –12 mA | 2 | | | 2 | | | |
| $V_{OL}$ | A, B, TDO | $V_{CC}$ = 2.7 V, | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | A port, TDO | $V_{CC}$ = 2.7 V, | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| | B port | $V_{CC}$ = 3 V, | $I_{OL}$ = 12 mA | | | 0.8 | | | 0.8 | |
| $I_I$ | CLK, LE, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 5 | | | 5 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | 500 | 75 | 150 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | | –500 | –75 | –150 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | | | 1 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.6 | 2 | | 0.6 | 2 | mA |
| | | | Outputs low | | 18 | 24 | | 18 | 24 | |
| | | | Outputs disabled | | 0.6 | 2 | | 0.6 | 2 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.5 | | | 0.5 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 10 | | | 10 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

PRODUCT PREVIEW

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## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 14)

| | | | | SN54LVTH182502A | | | | SN74LVTH182502A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | 0 | 100 | 0 | 80 | 0 | 100 | 0 | 80 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | 4.4 | | 5.6 | | 4.4 | | 5.6 | | ns |
| | | LEAB or LEBA high | | 3 | | 3 | | 3 | | 3 | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | 2.8 | | 3 | | 2.8 | | 3 | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | 1.5 | | 0.7 | | 1.5 | | 0.7 | | |
| | | | CLK low | 1.6 | | 1.6 | | 1.6 | | 1.6 | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | 1.4 | | 1.1 | | 1.4 | | 1.1 | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | 3.1 | | 3.5 | | 3.1 | | 3.5 | | |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 14)

| | | | SN54LVTH182502A | | | | SN74LVTH182502A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 40 | 0 | 50 | 0 | 40 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 9.5 | | 10.5 | | 9.5 | | 10.5 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, LE, or $\overline{OE}$ before TCK↑ | 6.5 | | 7 | | 6.5 | | 7 | | ns |
| | | TDI before TCK↑ | 2.5 | | 3.5 | | 2.5 | | 3.5 | | |
| | | TMS before TCK↑ | 2.5 | | 3.5 | | 2.5 | | 3.5 | | |
| $t_h$ | Hold time | A, B, CLK, LE, or $\overline{OE}$ after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | ns |
| | | TDI after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | 1 | | 1 | | µs |

PRODUCT PREVIEW

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## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182502A | | | | SN74LVTH182502A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | | 80 | | 100 | | 80 | | MHz |
| $t_{PLH}$ | A | B | 1.5 | 6 | | 6.7 | 1.5 | 5.7 | | 6.4 | ns |
| $t_{PHL}$ | | | 1.5 | 6 | | 6.7 | 1.5 | 5.7 | | 6.4 | |
| $t_{PLH}$ | B | A | 1.5 | 5.1 | | 5.8 | 1.5 | 4.9 | | 5.6 | ns |
| $t_{PHL}$ | | | 1.5 | 5.1 | | 5.8 | 1.5 | 4.9 | | 5.6 | |
| $t_{PLH}$ | CLKAB | B | 1.5 | 7.1 | | 8.1 | 1.5 | 6.7 | | 7.7 | ns |
| $t_{PHL}$ | | | 1.5 | 7.1 | | 8.1 | 1.5 | 6.7 | | 7.7 | |
| $t_{PLH}$ | CLKBA | A | 1.5 | 6.3 | | 7.2 | 1.5 | 5.8 | | 6.8 | ns |
| $t_{PHL}$ | | | 1.5 | 6.3 | | 7.2 | 1.5 | 5.8 | | 6.8 | |
| $t_{PLH}$ | LEAB | B | 1.5 | 8.7 | | 9.7 | 1.5 | 8.2 | | 9.2 | ns |
| $t_{PHL}$ | | | 1.5 | 6.5 | | 6.9 | 1.5 | 6.2 | | 6.7 | |
| $t_{PLH}$ | LEBA | A | 1.5 | 7.8 | | 9.2 | 1.5 | 7.4 | | 8.4 | ns |
| $t_{PHL}$ | | | 1.5 | 6 | | 6.6 | 1.5 | 5.7 | | 6.4 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 1.5 | 8.4 | | 9.6 | 1.5 | 7.9 | | 8.7 | ns |
| $t_{PZL}$ | | | 1.5 | 8.4 | | 9.6 | 1.5 | 7.9 | | 8.7 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2.5 | 9.1 | | 9.3 | 2.5 | 8.4 | | 8.9 | ns |
| $t_{PLZ}$ | | | 2.5 | 9.1 | | 9.3 | 2.5 | 8.4 | | 8.9 | |

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182502A | | | | SN74LVTH182502A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | | 40 | | 50 | | 40 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 15 | | 18 | 2.5 | 14 | | 17 | ns |
| $t_{PHL}$ | | | 2.5 | 15 | | 18 | 2.5 | 14 | | 17 | |
| $t_{PLH}$ | TCK↓ | TDO | 1 | 6 | | 7 | 1 | 5.5 | | 6.5 | ns |
| $t_{PHL}$ | | | 1.5 | 7 | | 8 | 1.5 | 6.5 | | 7.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 18 | | 21 | 4 | 17 | | 20 | ns |
| $t_{PZL}$ | | | 4 | 18 | | 21 | 4 | 17 | | 20 | |
| $t_{PZH}$ | TCK↓ | TDO | 1 | 6 | | 7 | 1 | 5.5 | | 6.5 | ns |
| $t_{PZL}$ | | | 1.5 | 6 | | 7 | 1.5 | 5.5 | | 6.5 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 19 | | 21 | 4 | 18 | | 20 | ns |
| $t_{PLZ}$ | | | 4 | 18 | | 19.5 | 4 | 17 | | 18.5 | |
| $t_{PHZ}$ | TCK↓ | TDO | 1.5 | 7.5 | | 9 | 1.5 | 7 | | 8.5 | ns |
| $t_{PLZ}$ | | | 1.5 | 7.5 | | 8.5 | 1.5 | 7 | | 8 | |

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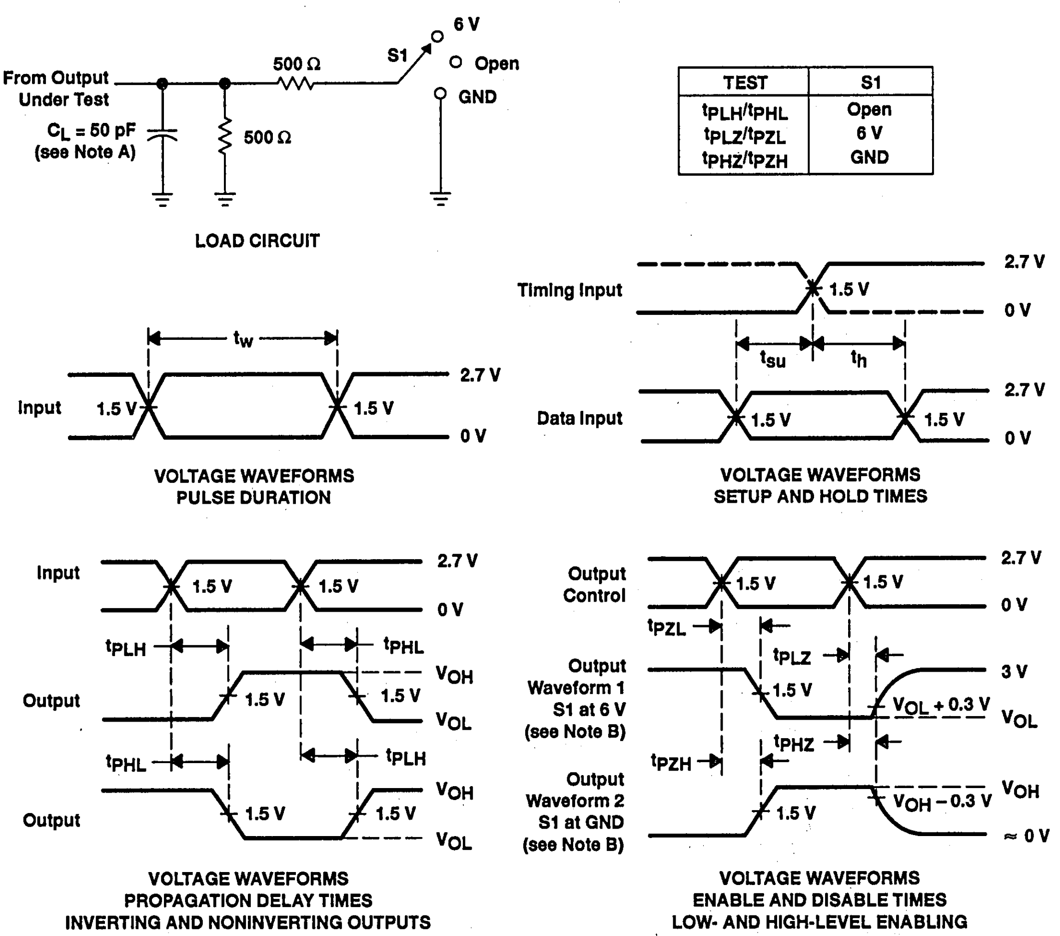
## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)
- Support Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- B-Port Outputs of 'LVTH182504A Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

## description

The 'LVTH18504A and 'LVTH182504A scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self-test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while $\overline{CLKENAB}$ is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and $\overline{CLKENAB}$ is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow, but uses the $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

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## description (continued)

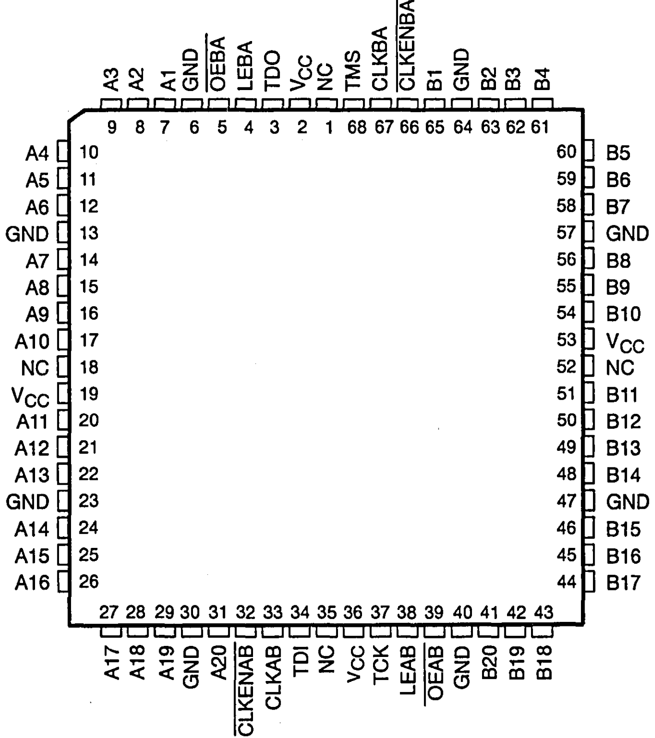
Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions, such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVTH182504A, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

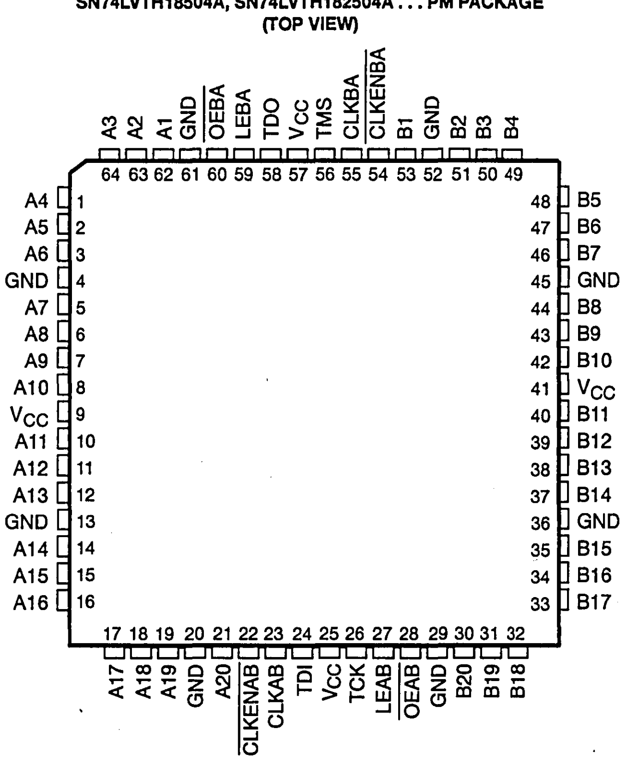
The SN54LVTH18504A and SN54LVTH182504A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH18504A and SN74LVTH182504A are characterized for operation from –40°C to 85°C.

SN54LVTH18504A, SN54LVTH182504A . . . HV PACKAGE
(TOP VIEW)




NC – No internal connection

SN74LVTH18504A, SN74LVTH182504A . . . PM PACKAGE
(TOP VIEW)




FUNCTION TABLE†
(normal mode, each register)

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| OEAB | LEAB | CLKENAB | CLKAB | A | B |
| L | L | L | L | X | $B_0$‡ |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | H | X | X | $B_0$‡ |
| L | H | X | X | L | L |
| L | H | X | X | H | H |
| H | X | X | X | X | Z |

† A-to-B data flow is shown. B-to-A data flow is similar, but uses OEBA, LEBA, CLKENBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established

## functional block diagram

Boundary-Scan Register

CLKENAB 22
LEAB 27
CLKAB 23
VCC
OEAB 28
CLKENBA 54
LEBA 59
CLKBA 55
VCC
OEBA 60

C1 1D
C1 1D
C1 1D
C1 1D

A1 62
53 B1

1 of 20 Channels

Bypass Register
Boundary-Control Register
Identification Register
Instruction Register
TAP Controller

VCC
TDI 24
VCC
TMS 56
TCK 26
58 TDO

Pin numbers shown are for the PM package.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A1–A20 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| B1–B20 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| CLKAB, CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| $\overline{\text{CLKENAB}}$, $\overline{\text{CLKENBA}}$ | Normal-function clock enables. See function table for normal-mode logic. |
| GND | Ground |
| LEAB, LEBA | Normal-function latch enables. See function table for normal-mode logic. |
| $\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are passed along this serial-test bus. The TAP controller monitors two signals from the test bus: TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationships of the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test data registers: a 48-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

Test-Logic-Reset
TMS = H
TMS = L
Run-Test/Idle
TMS = H
TMS = L
Select-DR-Scan
Select-IR-Scan
Capture-DR
Capture-IR
Shift-DR
Shift-IR
Exit1-DR
Exit1-IR
Pause-DR
Pause-IR
Exit2-DR
Exit2-IR
Update-DR
Update-IR

**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite-state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states, based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register at a time can be accessed.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'LVTH18504A and 'LVTH182504A, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–46 in the boundary-scan register are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

**Shift-DR**

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle, in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, such updates occur on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'LVTH18504A and 'LVTH182504A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to the active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'LVTH18504A and 'LVTH182504A. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The instruction register order of scan is shown in Figure 2.

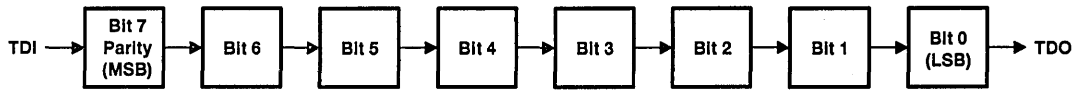



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary-scan register

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used to store test data that is to be applied externally to the device output pins, and/or to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–46 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | $\overline{\text{OEAB}}$ | 39 | A20-I/O | 19 | B20-I/O |
| 46 | $\overline{\text{OEBA}}$ | 38 | A19-I/O | 18 | B19-I/O |
| 45 | CLKAB | 37 | A18-I/O | 17 | B18-I/O |
| 44 | CLKBA | 36 | A17-I/O | 16 | B17-I/O |
| 43 | $\overline{\text{CLKENAB}}$ | 35 | A16-I/O | 15 | B16-I/O |
| 42 | $\overline{\text{CLKENBA}}$ | 34 | A15-I/O | 14 | B15-I/O |
| 41 | LEAB | 33 | A14-I/O | 13 | B14-I/O |
| 40 | LEBA | 32 | A13-I/O | 12 | B13-I/O |
| — | — | 31 | A12-I/O | 11 | B12-I/O |
| — | — | 30 | A11-I/O | 10 | B11-I/O |
| — | — | 29 | A10-I/O | 9 | B10-I/O |
| — | — | 28 | A9-I/O | 8 | B9-I/O |
| — | — | 27 | A8-I/O | 7 | B8-I/O |
| — | — | 26 | A7-I/O | 6 | B7-I/O |
| — | — | 25 | A6-I/O | 5 | B6-I/O |
| — | — | 24 | A5-I/O | 4 | B5-I/O |
| — | — | 23 | A4-I/O | 3 | B4-I/O |
| — | — | 22 | A3-I/O | 2 | B3-I/O |
| — | — | 21 | A2-I/O | 1 | B2-I/O |
| — | — | 20 | A1-I/O | 0 | B1-I/O |

### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the boundary-run (RUNT) instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The boundary-control register order of scan is shown in Figure 3.

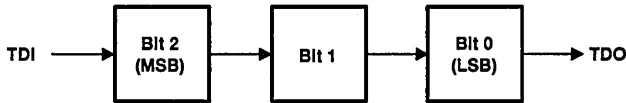



**Figure 3. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 4.

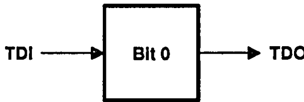



**Figure 4. Bypass Register Order of Scan**

### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'LVTH18504A, the binary value 00100000000000011101000000101111 (2001D02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74LVTH18504A.

For the 'LVTH182504A, the binary value 00010000000000100010000000101111 (1002202F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74LVTH182504A.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE† |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary-run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control-register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control-register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'LVTH18504A or 'LVTH182504A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output-enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–46 of the BSR). When a given output enable is active (logic 0), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift register and shadow latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE<br>BIT 2 → BIT 0<br>MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/40-bit mode (PRPG) |
| X10 | Parallel-signature analysis/40-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/20-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/20-bit mode (PSA/COUNT) |

While the control input BSCs (bits 47–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 47–46 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when the device is operating in one direction of data flow (that is, $\overline{OEAB} \neq \overline{OEBA}$). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 5 and 6 show the 40-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

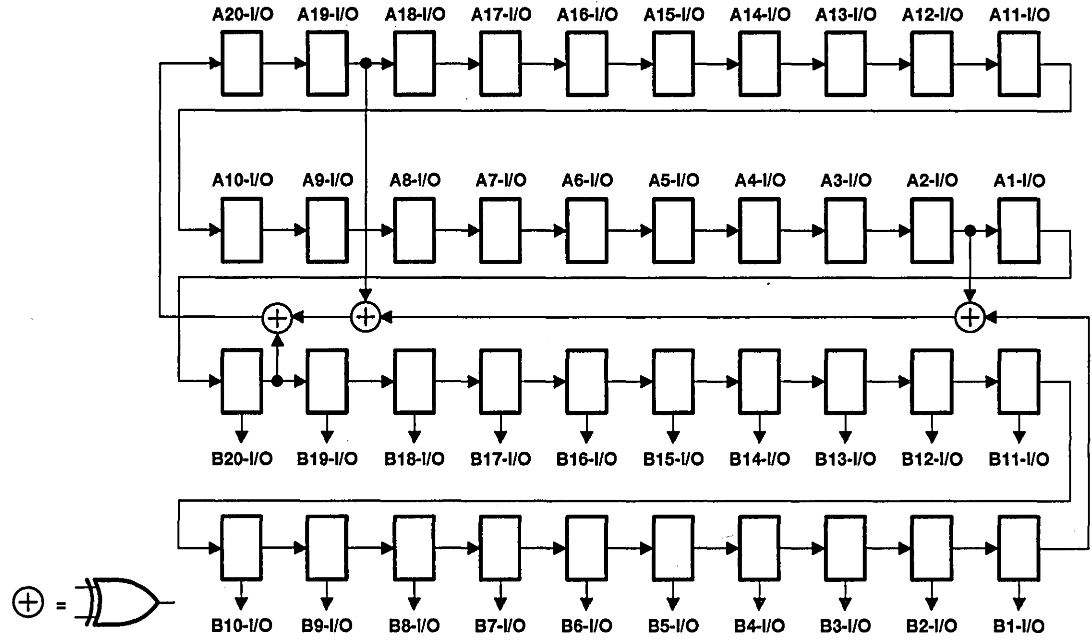



Figure 5. 40-Bit PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

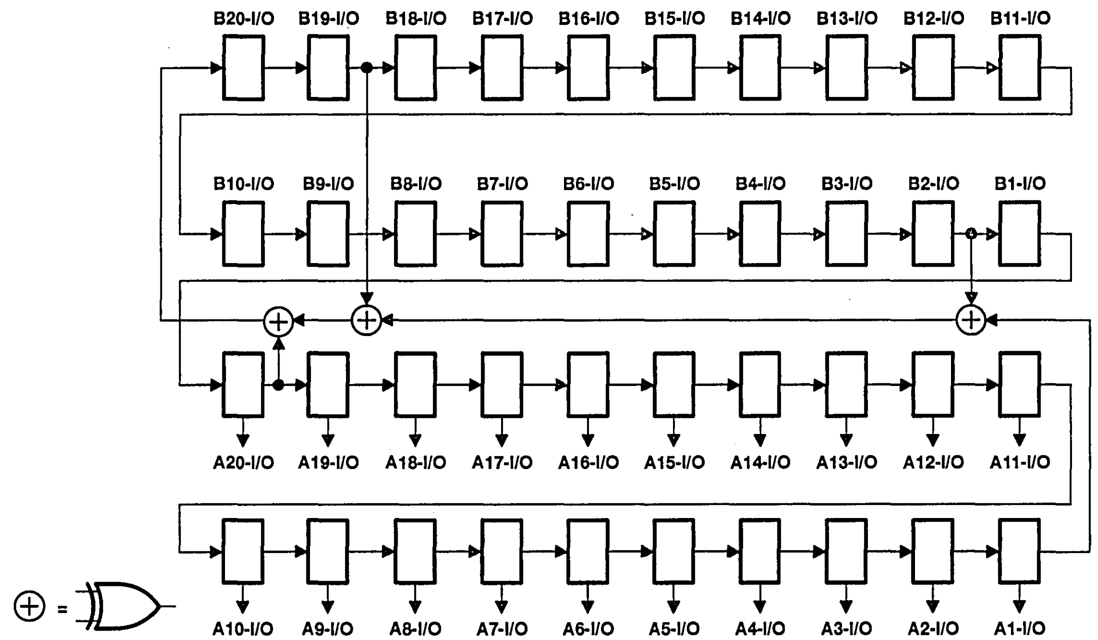



Figure 6. 40-Bit PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 40-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 7 and 8 show the 40-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

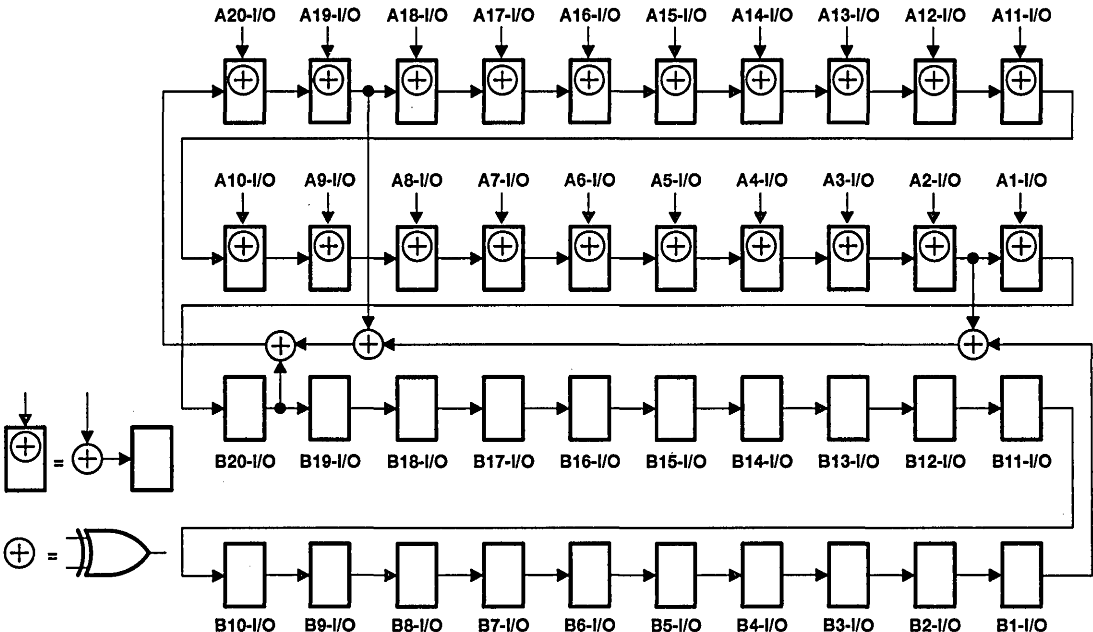



Figure 7. 40-Bit PSA Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

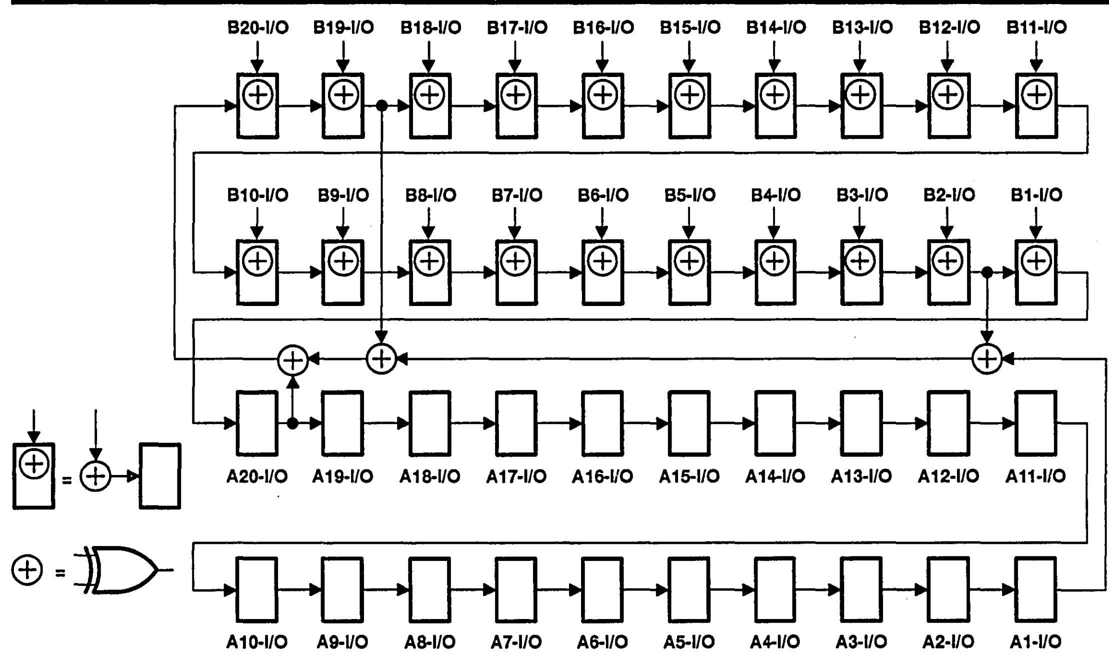



**Figure 8. 40-Bit PSA Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into a 20-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, a 20-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 9 and 10 show the 20-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

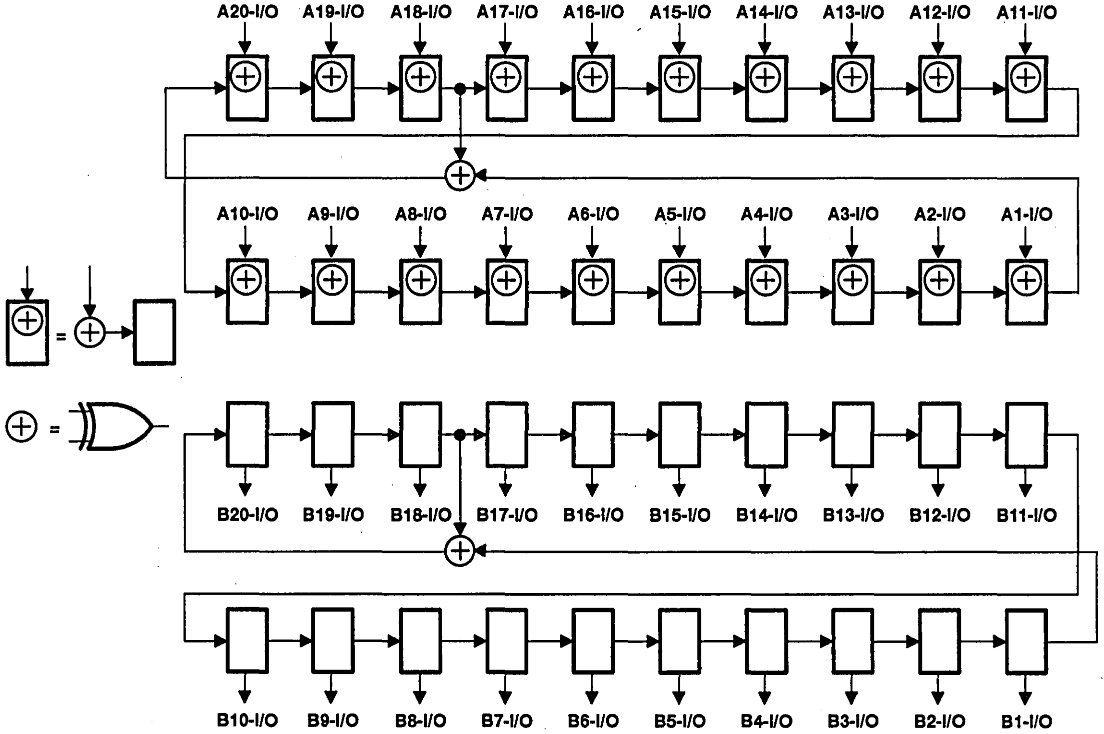



**Figure 9. 20-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

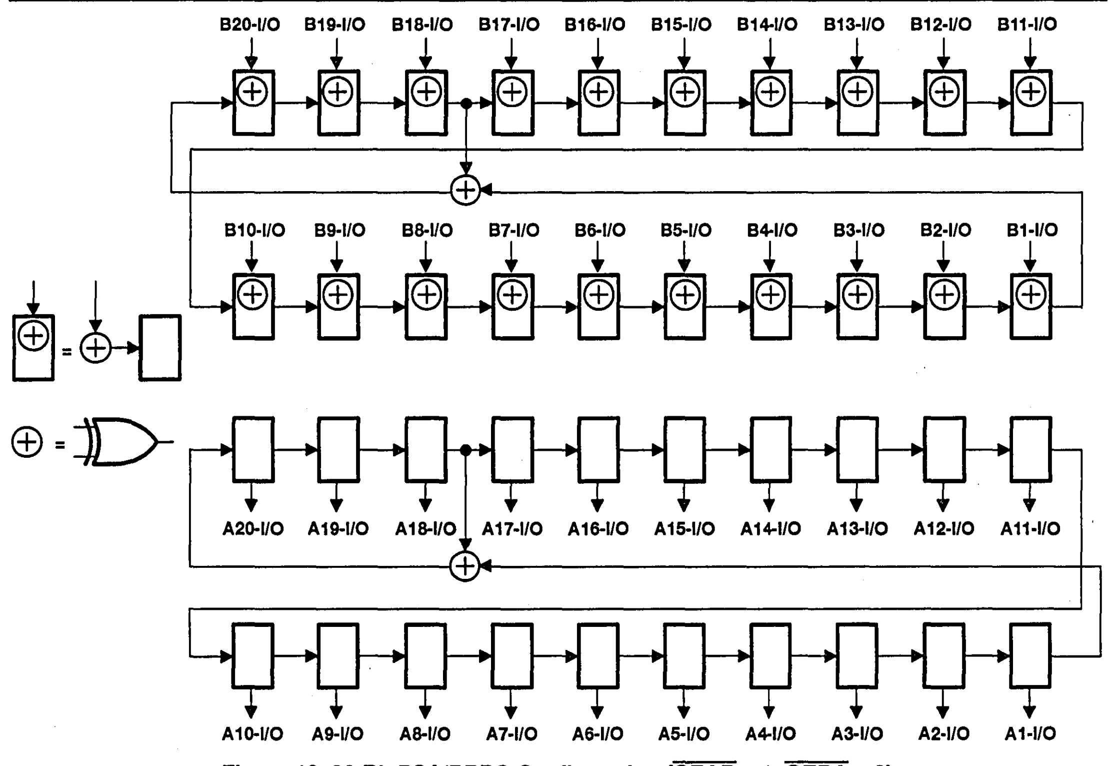



**Figure 10. 20-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into a 20-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, a 20-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 11 and 12 show the 20-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

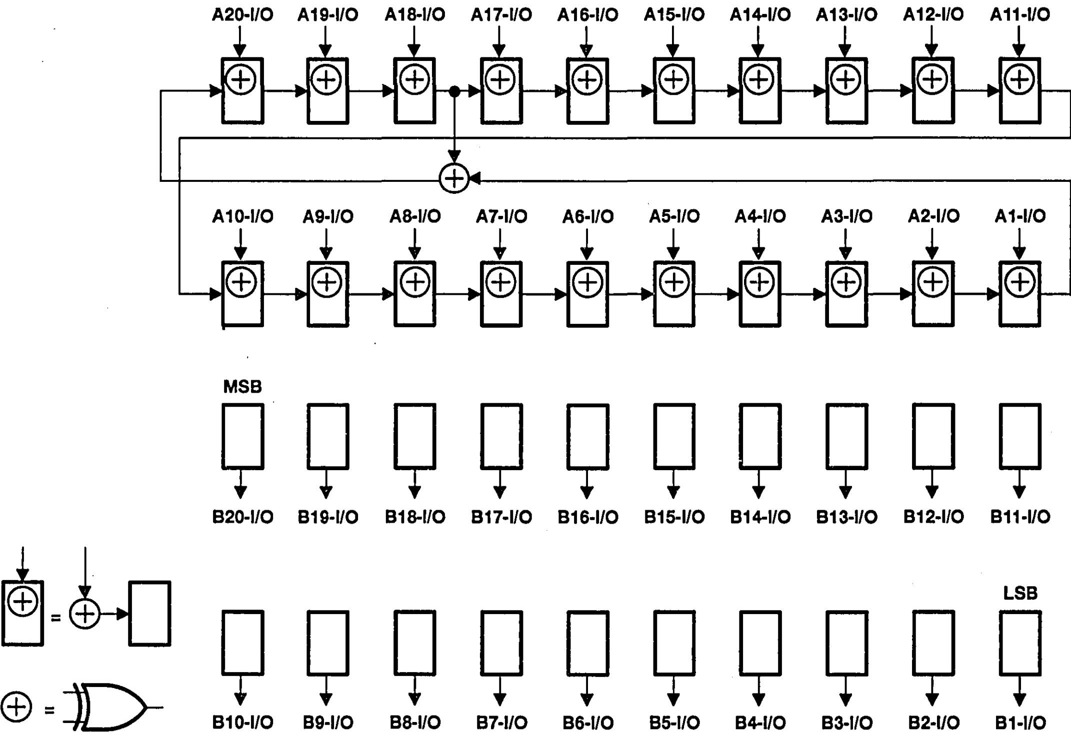



**Figure 11. 20-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)**

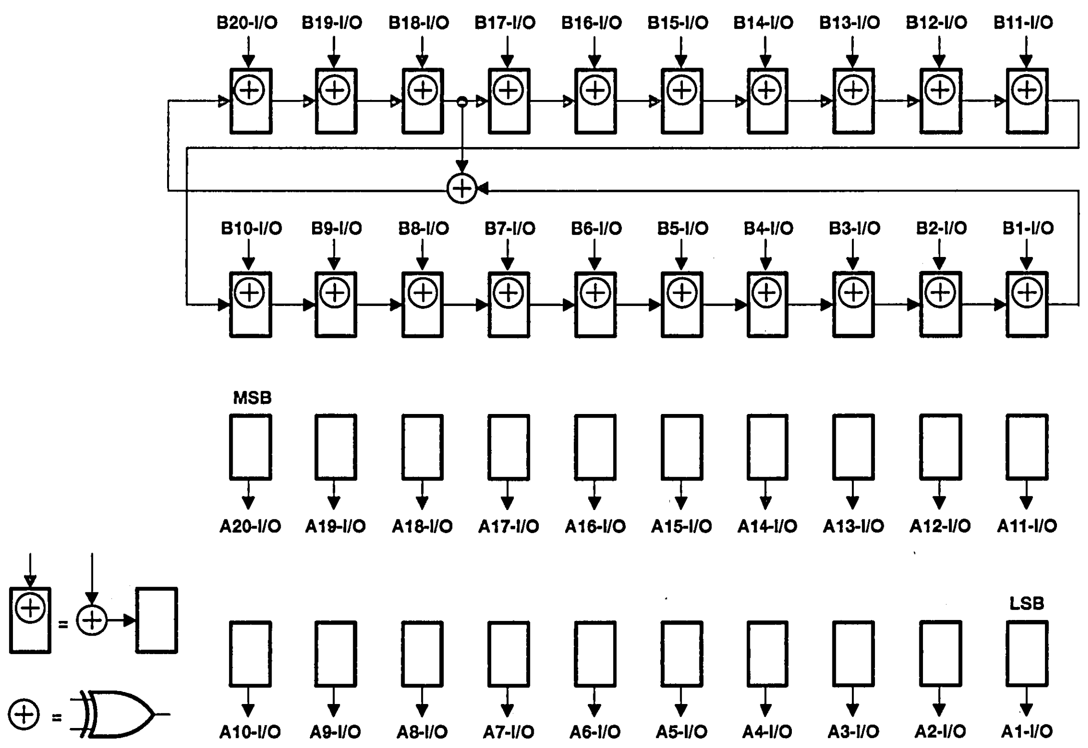



**Figure 12. 20-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)**

## timing description

All test operations of the 'LVTH18504A and 'LVTH182504A are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 13. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 details the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed. |

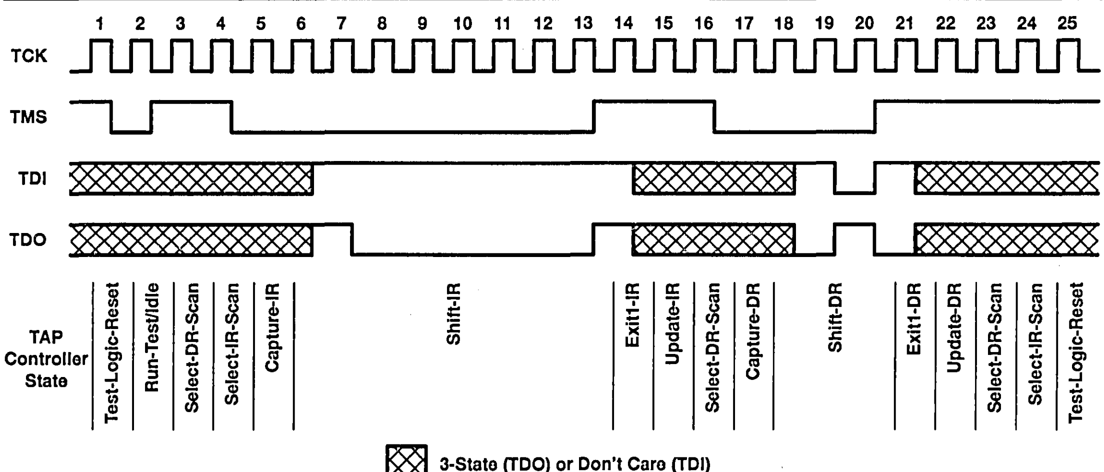



**Figure 13. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Parameter | | Value |
|---|---|---|
| Supply voltage range, $V_{CC}$ | | –0.5 V to 4.6 V |
| Input voltage range, $V_I$ (see Note 1) | | –0.5 V to 7 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) | | –0.5 V to 7 V |
| Current into any output in the low state, $I_O$: | SN54LVTH18504A | 96 mA |
| | SN54LVTH182504A (A port or TDO) | 96 mA |
| | SN54LVTH182504A (B port) | 30 mA |
| | SN74LVTH18504A | 128 mA |
| | SN74LVTH182504A (A port or TDO) | 128 mA |
| | SN74LVTH182504A (B port) | 30 mA |
| Current into any output in the high state, $I_O$ (see Note 2): | SN54LVTH18504A | 48 mA |
| | SN54LVTH182504A (A port or TDO) | 48 mA |
| | SN54LVTH182504A (B port) | 30 mA |
| | SN74LVTH18504A | 64 mA |
| | SN74LVTH182504A (A port or TDO) | 64 mA |
| | SN74LVTH182504A (B port) | 30 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | | –50 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | | –50 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): PM package | | 1 W |
| Storage temperature range, $T_{stg}$ | | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current only flows when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54LVTH18504A | | SN74LVTH18504A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 32 | mA |
| $I_{OL}$† | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH18504A | | | SN74LVTH18504A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| $I_I$ | CLK, $\overline{CLKEN}$, LE, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 5 | | | 5 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | 500 | 75 | 150 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | | –500 | –75 | –150 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | | | 1 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.6 | 2 | | 0.6 | 2 | mA |
| | | | Outputs low | | 19.5 | 27 | | 19.5 | 27 | |
| | | | Outputs disabled | | 0.6 | 2 | | 0.6 | 2 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.5 | | | 0.5 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 10 | | | 10 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 14)

| | | | | SN54LVTH18504A | | | | SN74LVTH18504A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | 0 | 100 | 0 | 80 | 0 | 100 | 0 | 80 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | 4.4 | | 5.6 | | 4.4 | | 5.6 | | ns |
| | | LEAB or LEBA high | | 3 | | 3 | | 3 | | 3 | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | 2.4 | | 2.8 | | 2.4 | | 2.8 | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | 1.5 | | 0.7 | | 1.5 | | 0.7 | | |
| | | | CLK low | 1.6 | | 1.6 | | 1.6 | | 1.6 | | |
| | | $\overline{CLKEN}$ before CLK↑ | | 2.8 | | 3.4 | | 2.8 | | 3.4 | | |
| $t_h$ | Hold time | A after CLKAB↑ | | 1 | | 0.8 | | 1 | | 0.8 | | ns |
| | | B after CLKBA↑ | | 1.4 | | 1.1 | | 1.4 | | 1.1 | | |
| | | A after LEAB↓ or B after LEBA↓ | | 3.1 | | 3.5 | | 3.1 | | 3.5 | | |
| | | $\overline{CLKEN}$ after CLK↑ | | 0.7 | | 0.2 | | 0.7 | | 0.2 | | |

PRODUCT PREVIEW

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 14)

| | | | SN54LVTH18504A | | | | SN74LVTH18504A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 40 | 0 | 50 | 0 | 40 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 9.5 | | 10.5 | | 9.5 | | 10.5 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ before TCK↑ | 6.5 | | 7 | | 6.5 | | 7 | | ns |
| | | TDI before TCK↑ | 2.5 | | 3.5 | | 2.5 | | 3.5 | | |
| | | TMS before TCK↑ | 2.5 | | 3.5 | | 2.5 | | 3.5 | | |
| $t_h$ | Hold time | A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | ns |
| | | TDI after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | 1 | | 1 | | µs |

PRODUCT PREVIEW

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## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18504A | | | | SN74LVTH18504A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | | 80 | | 100 | | 80 | | MHz |
| $t_{PLH}$ | A or B | B or A | 1.5 | 5.4 | | 5.8 | 1.5 | 5.1 | | 5.6 | ns |
| $t_{PHL}$ | | | 1.5 | 5.4 | | 5.8 | 1.5 | 5.1 | | 5.6 | |
| $t_{PLH}$ | CLKAB | B | 1.5 | 6.9 | | 7.8 | 1.5 | 5.8 | | 6.8 | ns |
| $t_{PHL}$ | | | 1.5 | 6.9 | | 7.8 | 1.5 | 5.8 | | 6.8 | |
| $t_{PLH}$ | CLKBA | A | 1.5 | 6.9 | | 7.8 | 1.5 | 6.4 | | 7.4 | ns |
| $t_{PHL}$ | | | 1.5 | 6.9 | | 7.8 | 1.5 | 6.4 | | 7.4 | |
| $t_{PLH}$ | LEAB or LEBA | B or A | 2 | 8.7 | | 9.5 | 2 | 8.1 | | 8.8 | ns |
| $t_{PHL}$ | | | 2 | 7.1 | | 7.4 | 2 | 6.7 | | 7.1 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2 | 9.5 | | 10.5 | 2 | 9.1 | | 10 | ns |
| $t_{PZL}$ | | | 2 | 10 | | 10.8 | 2 | 9.6 | | 10.4 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2.5 | 12 | | 12.7 | 2.5 | 10.4 | | 11.2 | ns |
| $t_{PLZ}$ | | | 2.5 | 9.6 | | 9.9 | 2.5 | 9.1 | | 9.5 | |

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18504A | | | | SN74LVTH18504A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | | 40 | | 50 | | 40 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 15 | | 18 | 2.5 | 14 | | 17 | ns |
| $t_{PHL}$ | | | 2.5 | 15 | | 18 | 2.5 | 14 | | 17 | |
| $t_{PLH}$ | TCK↓ | TDO | 1 | 6 | | 7 | 1 | 5.5 | | 6.5 | ns |
| $t_{PHL}$ | | | 1.5 | 7 | | 8 | 1.5 | 6.5 | | 7.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 18 | | 21 | 4 | 17 | | 20 | ns |
| $t_{PZL}$ | | | 4 | 18 | | 21 | 4 | 17 | | 20 | |
| $t_{PZH}$ | TCK↓ | TDO | 1 | 6 | | 7 | 1 | 5.5 | | 6.5 | ns |
| $t_{PZL}$ | | | 1.5 | 6 | | 7 | 1.5 | 5.5 | | 6.5 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 19 | | 21 | 4 | 18 | | 20 | ns |
| $t_{PLZ}$ | | | 4 | 18 | | 19.5 | 4 | 17 | | 18.5 | |
| $t_{PHZ}$ | TCK↓ | TDO | 1.5 | 7.5 | | 9 | 1.5 | 7 | | 8.5 | ns |
| $t_{PLZ}$ | | | 1.5 | 7.5 | | 8.5 | 1.5 | 7 | | 8 | |

PRODUCT PREVIEW

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## recommended operating conditions

| | | | SN54LVTH182504A MIN | SN54LVTH182504A MAX | SN74LVTH182504A MIN | SN74LVTH182504A MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 24 | | 32 | mA |
| | | B port | | 12 | | 12 | |
| $I_{OL}$† | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH182504A | | | SN74LVTH182504A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | A, B, TDO | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | A port, TDO | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| | B port | $V_{CC}$ = 3 V, | $I_{OH}$ = –12 mA | 2 | | | 2 | | | |
| $V_{OL}$ | A, B, TDO | $V_{CC}$ = 2.7 V, | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | A port, TDO | $V_{CC}$ = 2.7 V, | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| | B port | $V_{CC}$ = 3 V, | $I_{OL}$ = 12 mA | | | 0.8 | | | 0.8 | |
| $I_I$ | CLK, $\overline{CLKEN}$, LE, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 5 | | | 5 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | 500 | 75 | 150 | 500 | µA |
| | | | $V_I$ = 2 V | –75 | | –500 | –75 | –150 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | | | 1 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.6 | 2 | | 0.6 | 2 | mA |
| | | | Outputs low | | 19.5 | 27 | | 19.5 | 27 | |
| | | | Outputs disabled | | 0.6 | 2 | | 0.6 | 2 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.5 | | | 0.5 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 10 | | | 10 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | | 8 | | pF |

PRODUCT PREVIEW

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

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## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 14)

| | | | | SN54LVTH182504A | | | | SN74LVTH182504A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | 0 | 100 | 0 | 80 | 0 | 100 | 0 | 80 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | 4.4 | | 5.6 | | 4.4 | | 5.6 | | ns |
| | | LEAB or LEBA high | | 3 | | 3 | | 3 | | 3 | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | 2.8 | | 3 | | 2.8 | | 3 | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | 1.5 | | 0.7 | | 1.5 | | 0.7 | | |
| | | | CLK low | 1.6 | | 1.6 | | 1.6 | | 1.6 | | |
| | | $\overline{CLKEN}$ before CLK↑ | | 2.8 | | 3.4 | | 2.8 | | 3.4 | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | 1.4 | | 1.1 | | 1.4 | | 1.1 | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | 3.1 | | 3.5 | | 3.1 | | 3.5 | | |
| | | $\overline{CLKEN}$ after CLK↑ | | 0.7 | | 0.2 | | 0.7 | | 0.2 | | |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 14)

| | | | SN54LVTH182504A | | | | SN74LVTH182504A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 40 | 0 | 50 | 0 | 40 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 9.5 | | 10.5 | | 9.5 | | 10.5 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ before TCK↑ | 6.5 | | 7 | | 6.5 | | 7 | | ns |
| | | TDI before TCK↑ | 2.5 | | 3.5 | | 2.5 | | 3.5 | | |
| | | TMS before TCK↑ | 2.5 | | 3.5 | | 2.5 | | 3.5 | | |
| $t_h$ | Hold time | A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | ns |
| | | TDI after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1 | | 1.5 | | 1 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | 1 | | 1 | | µs |

PRODUCT PREVIEW

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## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182504A $V_{CC}$ = 3.3 V ± 0.3 V MIN | SN54LVTH182504A $V_{CC}$ = 3.3 V ± 0.3 V MAX | SN54LVTH182504A $V_{CC}$ = 2.7 V MIN | SN54LVTH182504A $V_{CC}$ = 2.7 V MAX | SN74LVTH182504A $V_{CC}$ = 3.3 V ± 0.3 V MIN | SN74LVTH182504A $V_{CC}$ = 3.3 V ± 0.3 V MAX | SN74LVTH182504A $V_{CC}$ = 2.7 V MIN | SN74LVTH182504A $V_{CC}$ = 2.7 V MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | CLKAB or CLKBA | | 100 | | 80 | | 100 | | 80 | | MHz |
| $t_{PLH}$ | A | B | 1.5 | 6.4 | | 6.9 | 1.5 | 5.9 | | 6.6 | ns |
| $t_{PHL}$ | | | 1.5 | 6.4 | | 6.9 | 1.5 | 5.9 | | 6.6 | |
| $t_{PLH}$ | B | A | 1.5 | 5.4 | | 5.8 | 1.5 | 5.1 | | 5.6 | ns |
| $t_{PHL}$ | | | 1.5 | 5.4 | | 5.8 | 1.5 | 5.1 | | 5.6 | |
| $t_{PLH}$ | CLKAB | B | 1.5 | 6.9 | | 7.8 | 1.5 | 6.7 | | 7.7 | ns |
| $t_{PHL}$ | | | 1.5 | 6.9 | | 7.8 | 1.5 | 6.7 | | 7.7 | |
| $t_{PLH}$ | CLKBA | A | 1.5 | 6.9 | | 7.8 | 1.5 | 6.4 | | 7.4 | ns |
| $t_{PHL}$ | | | 1.5 | 6.9 | | 7.8 | 1.5 | 6.4 | | 7.4 | |
| $t_{PLH}$ | LEAB | B | 2 | 8.7 | | 9.5 | 2 | 8.2 | | 9.2 | ns |
| $t_{PHL}$ | | | 2 | 7.1 | | 7.4 | 2 | 6.7 | | 7.1 | |
| $t_{PLH}$ | LEBA | A | 2 | 8.7 | | 9.5 | 2 | 8.1 | | 8.8 | ns |
| $t_{PHL}$ | | | 2 | 7.1 | | 7.4 | 2 | 6.7 | | 7.1 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2 | 9.9 | | 11.1 | 2 | 9.5 | | 10.6 | ns |
| $t_{PZL}$ | | | 2 | 10.2 | | 11 | 2 | 9.7 | | 10.5 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2.5 | 12 | | 12.7 | 2.5 | 11.1 | | 11.8 | ns |
| $t_{PLZ}$ | | | 2.5 | 11 | | 11.2 | 2.5 | 9.8 | | 10 | |

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 14)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182504A $V_{CC}$ = 3.3 V ± 0.3 V MIN | SN54LVTH182504A $V_{CC}$ = 3.3 V ± 0.3 V MAX | SN54LVTH182504A $V_{CC}$ = 2.7 V MIN | SN54LVTH182504A $V_{CC}$ = 2.7 V MAX | SN74LVTH182504A $V_{CC}$ = 3.3 V ± 0.3 V MIN | SN74LVTH182504A $V_{CC}$ = 3.3 V ± 0.3 V MAX | SN74LVTH182504A $V_{CC}$ = 2.7 V MIN | SN74LVTH182504A $V_{CC}$ = 2.7 V MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | TCK | | 50 | | 40 | | 50 | | 40 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 15 | | 18 | 2.5 | 14 | | 17 | ns |
| $t_{PHL}$ | | | 2.5 | 15 | | 18 | 2.5 | 14 | | 17 | |
| $t_{PLH}$ | TCK↓ | TDO | 1 | 6 | | 7 | 1 | 5.5 | | 6.5 | ns |
| $t_{PHL}$ | | | 1.5 | 7 | | 8 | 1.5 | 6.5 | | 7.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 18 | | 21 | 4 | 17 | | 20 | ns |
| $t_{PZL}$ | | | 4 | 18 | | 21 | 4 | 17 | | 20 | |
| $t_{PZH}$ | TCK↓ | TDO | 1 | 6 | | 7 | 1 | 5.5 | | 6.5 | ns |
| $t_{PZL}$ | | | 1.5 | 6 | | 7 | 1.5 | 5.5 | | 6.5 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 19 | | 21 | 4 | 18 | | 20 | ns |
| $t_{PLZ}$ | | | 4 | 18 | | 19.5 | 4 | 17 | | 18.5 | |
| $t_{PHZ}$ | TCK↓ | TDO | 1.5 | 7.5 | | 9 | 1.5 | 7 | | 8.5 | ns |
| $t_{PLZ}$ | | | 1.5 | 7.5 | | 8.5 | 1.5 | 7 | | 8 | |

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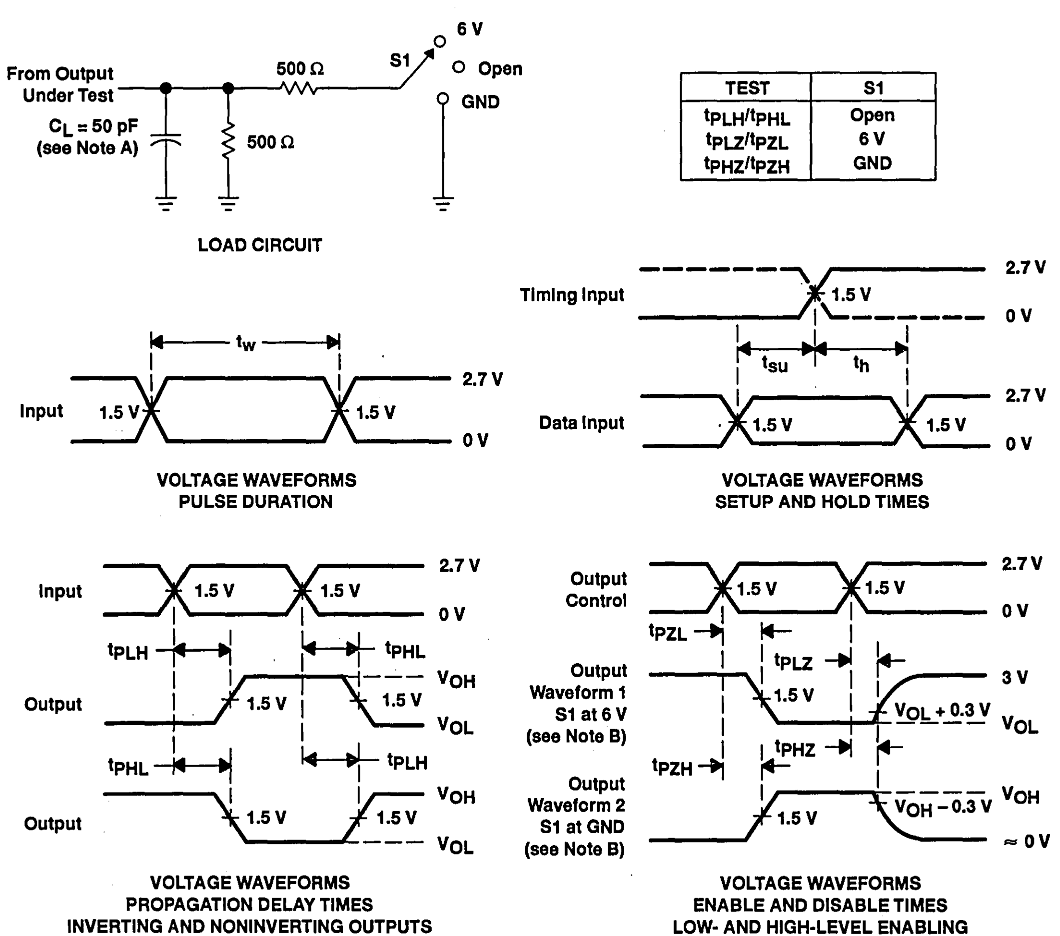
## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 14. Load Circuit and Voltage Waveforms**

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors**
- **B-Port Outputs of 'LVTH182646A Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ**
  - **Parallel-Signature Analysis at Inputs**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**
- **Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings**

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## description

The 'LVTH18646A and 'LVTH182646A scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Transceiver function is controlled by output-enable ($\overline{OE}$) and direction (DIR) inputs. When $\overline{OE}$ is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When $\overline{OE}$ is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 shows the four fundamental bus-management functions that can be performed with the 'LVTH18646A and 'LVTH182646A.

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## description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

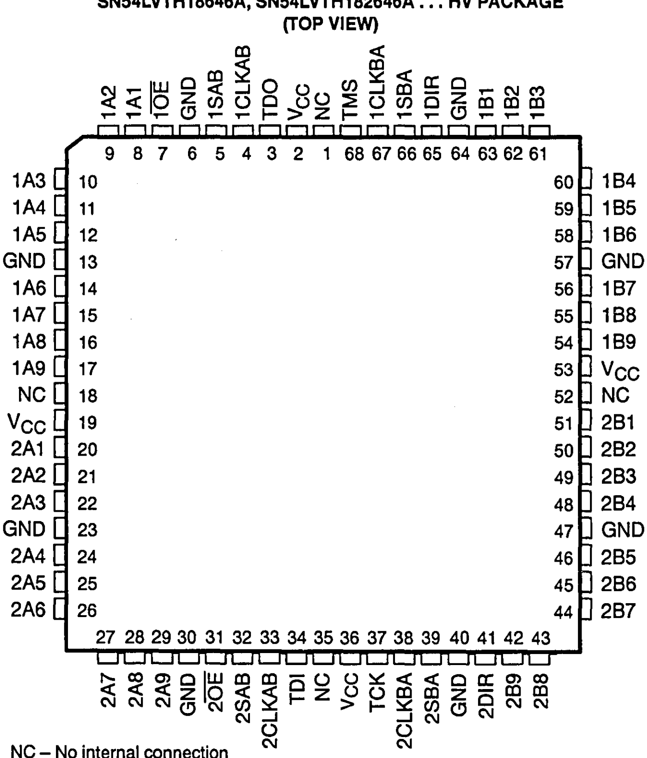
Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVTH182646A, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54LVT18646 and SN54LVTH182646A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVTH18646A and SN74LVTH182646A are characterized for operation from −40°C to 85°C.

SN54LVTH18646A, SN54LVTH182646A . . . HV PACKAGE
(TOP VIEW)




NC – No internal connection

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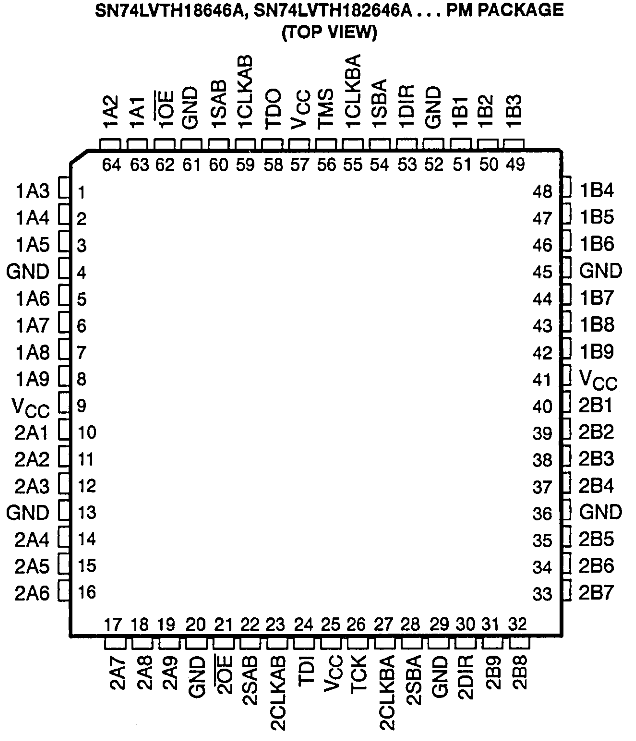
**SN74LVTH18646A, SN74LVTH182646A . . . PM PACKAGE**
**(TOP VIEW)**




**FUNCTION TABLE**
**(normal mode, each 9-bit section)**

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA | A1–A9 | B1–B9 | |
| X | X | ↑ | X | X | X | Input | Unspecified† | Store A, B unspecified† |
| X | X | X | ↑ | X | X | Unspecified† | Input | Store B, A unspecified† |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| H | X | L | L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | X | X | H | Output | Input disabled | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | X | X | H | X | Input disabled | Output | Stored A data to B bus |

† The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data-input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

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BUS A BUS B

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER BUS B TO BUS A**

BUS A BUS B

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | H | X | X | L | X |

**REAL-TIME TRANSFER BUS A TO BUS B**

BUS A BUS B

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| H | X | ↑ | ↑ | X | X |

**STORAGE FROM A, B, OR A AND B**

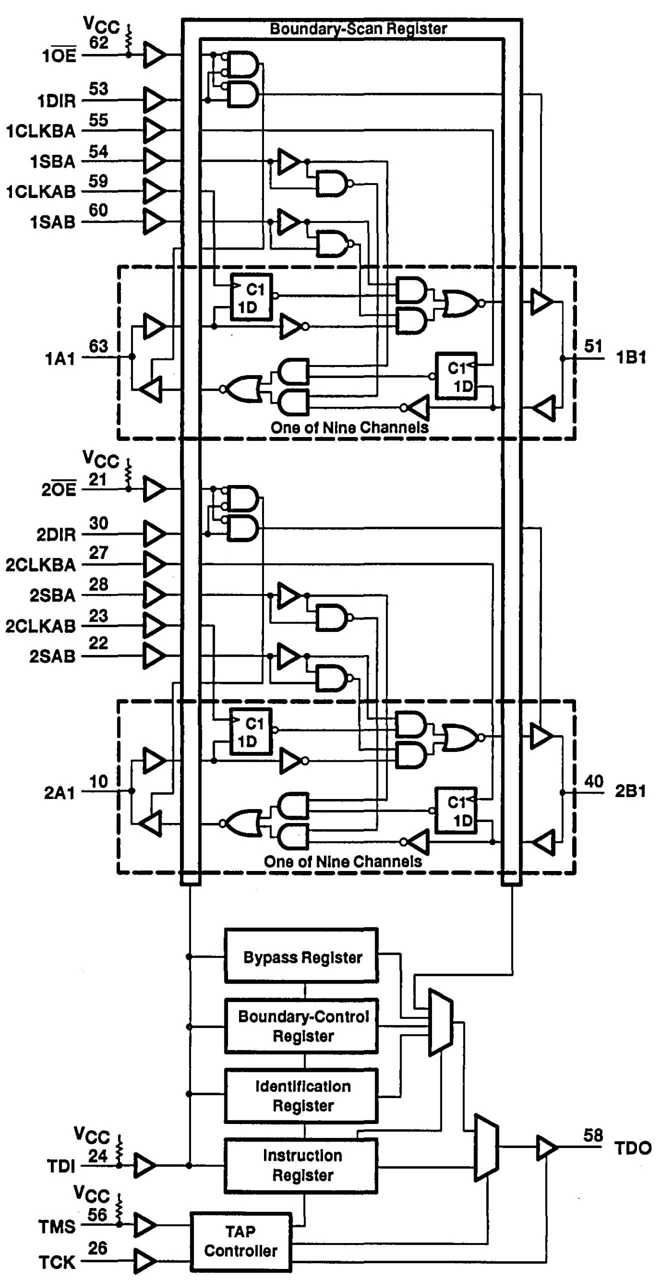
BUS A BUS B

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | H |
| L | H | X | X | H | X |

**TRANSFER STORED DATA TO A AND/OR B**

**Figure 1. Bus-Management Functions**

## functional block diagram




Pin numbers shown are for the PM package.

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## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| 1DIR, 2DIR | Normal-function direction controls. See function table for normal-mode logic. |
| GND | Ground |
| $1\overline{OE}$, $2\overline{OE}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal will force the terminal to a high level if left unconnected. |
| 1SAB, 1SBA, 2SAB, 2SBA | Normal-function select controls. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

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## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 2 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and four test-data registers: a 52-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.

Test-Logic-Reset
TMS = H
TMS = L
Run-Test/Idle
TMS = L
TMS = H
Select-DR-Scan
TMS = H
Select-IR-Scan
TMS = H
TMS = L
Capture-DR
TMS = H
TMS = H
TMS = L
Capture-IR
TMS = L
Shift-DR
TMS = L
TMS = L
Shift-IR
TMS = L
TMS = H
TMS = H
TMS = H
Exit1-DR
Exit1-IR
TMS = H
TMS = L
TMS = L
Pause-DR
TMS = L
Pause-IR
TMS = L
TMS = H
TMS = H
TMS = L
Exit2-DR
TMS = L
Exit2-IR
TMS = H
TMS = H
Update-DR
Update-IR
TMS = H
TMS = L
TMS = H
TMS = L

**Figure 2. TAP-Controller State Diagram**

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## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 2 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'LVTH18646A and 'LVTH182646A, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 51–48 in the boundary-scan register are reset to logic 0, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

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### Shift-DR (continued)

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'LVTH18646A and 'LVTH182646A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to the active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction-register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'LVTH18646A and 'LVTH182646A. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 3.

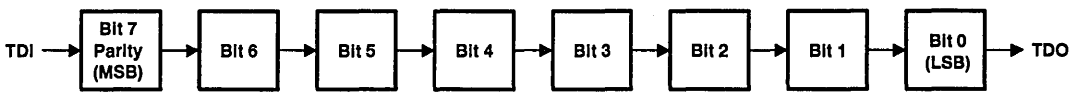


**Figure 3. Instruction Register Order of Scan**

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## data register description

### boundary-scan register

The boundary-scan register (BSR) is 52 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, one BSC for each normal-function I/O pin (one single cell for both input data and output data), and one BSC for each of the internally decoded output-enable signals (1OEA, 2OEA, 1OEB, 2OEB). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle, as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 51–48 are reset to logic 0, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

When external data is to be captured, the BSCs for signals 1OEA, 2OEA, 1OEB, and 2OEB capture logic values determined by the following positive-logic equations:

1OEA = $\overline{1OE}$ • $\overline{1DIR}$, 2OEA = $\overline{2OE}$ • $\overline{2DIR}$, 1OEB = $\overline{1OE}$ • DIR, and 2OEB = $\overline{2OE}$ • DIR

When data is to be applied externally, these BSCs control the drive state (active or high impedance) of their respective outputs.

The BSR order of scan is from TDI through bits 51–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 51 | 2OEB | 35 | 2A9-I/O | 17 | 2B9-I/O |
| 50 | 1OEB | 34 | 2A8-I/O | 16 | 2B8-I/O |
| 49 | 2OEA | 33 | 2A7-I/O | 15 | 2B7-I/O |
| 48 | 1OEA | 32 | 2A6-I/O | 14 | 2B6-I/O |
| 47 | 2DIR | 31 | 2A5-I/O | 13 | 2B5-I/O |
| 46 | 1DIR | 30 | 2A4-I/O | 12 | 2B4-I/O |
| 45 | $\overline{2OE}$ | 29 | 2A3-I/O | 11 | 2B3-I/O |
| 44 | $\overline{1OE}$ | 28 | 2A2-I/O | 10 | 2B2-I/O |
| 43 | 2CLKAB | 27 | 2A1-I/O | 9 | 2B1-I/O |
| 42 | 1CLKAB | 26 | 1A9-I/O | 8 | 1B9-I/O |
| 41 | 2CLKBA | 25 | 1A8-I/O | 7 | 1B8-I/O |
| 40 | 1CLKBA | 24 | 1A7-I/O | 6 | 1B7-I/O |
| 39 | 2SAB | 23 | 1A6-I/O | 5 | 1B6-I/O |
| 38 | 1SAB | 22 | 1A5-I/O | 4 | 1B5-I/O |
| 37 | 2SBA | 21 | 1A4-I/O | 3 | 1B4-I/O |
| 36 | 1SBA | 20 | 1A3-I/O | 2 | 1B3-I/O |
| — | — | 19 | 1A2-I/O | 1 | 1B2-I/O |
| — | — | 18 | 1A1-I/O | 0 | 1B1-I/O |

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### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The boundary-control register order of scan is shown in Figure 4.

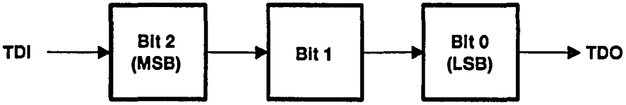


**Figure 4. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 5.

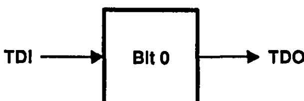


**Figure 5. Bypass Register Order of Scan**

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### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'LVTH18646A, the binary value 00100000000000011110000000101111 (2001E02F, hex) is captured (during Capture-DR state) in the device-identification register to identify this device as Texas Instruments SN54/74LVTH18646A.

For the 'LVTH182646A, the binary value 00100000000000100011000000101111 (2002302F, hex) is captured (during Capture-DR state) in the device-identification register to identify this device as Texas Instruments SN54/74LVTH182646A.

The device-identification register order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the device identification register bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

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## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'LVT18646 or 'LVT182646.

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### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 51 – 48 of the BSR). When a given output enable is active (logic 1), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The device identification register is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

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## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 51–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 51–48 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when both bytes of the device are operating in one direction of data flow (that is, 1OEA ≠ 1OEB and 2OEA ≠ 2OEB) and in the same direction of data flow (that is, 1OEA = 2OEA and 1OEB = 2OEB). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 6 and 7 illustrate the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

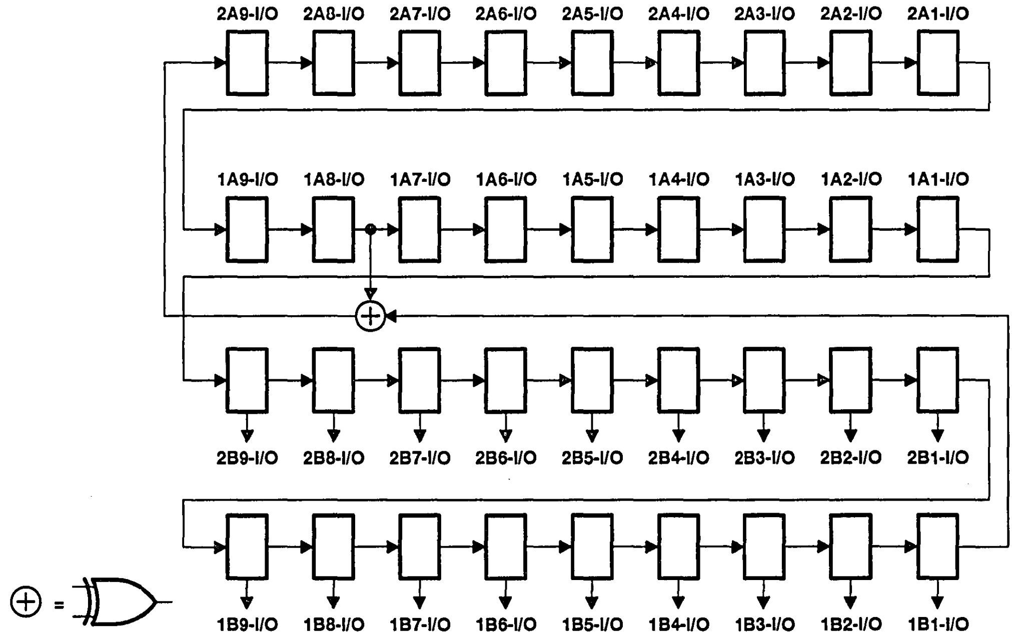


**Figure 6. 36-Bit PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

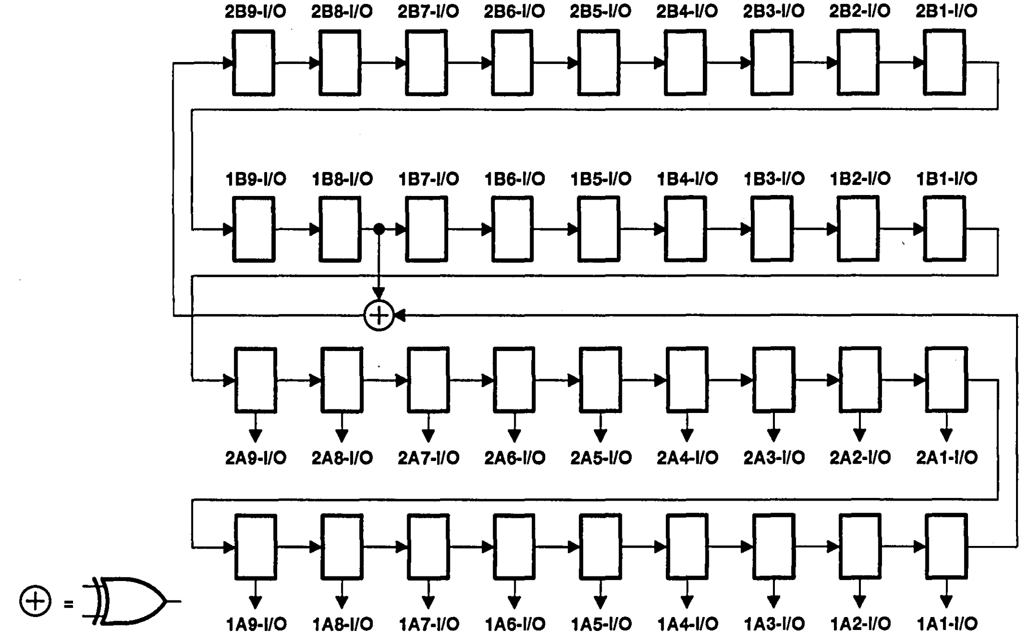


Figure 7. 36-Bit PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

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### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 8 and 9 illustrate the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

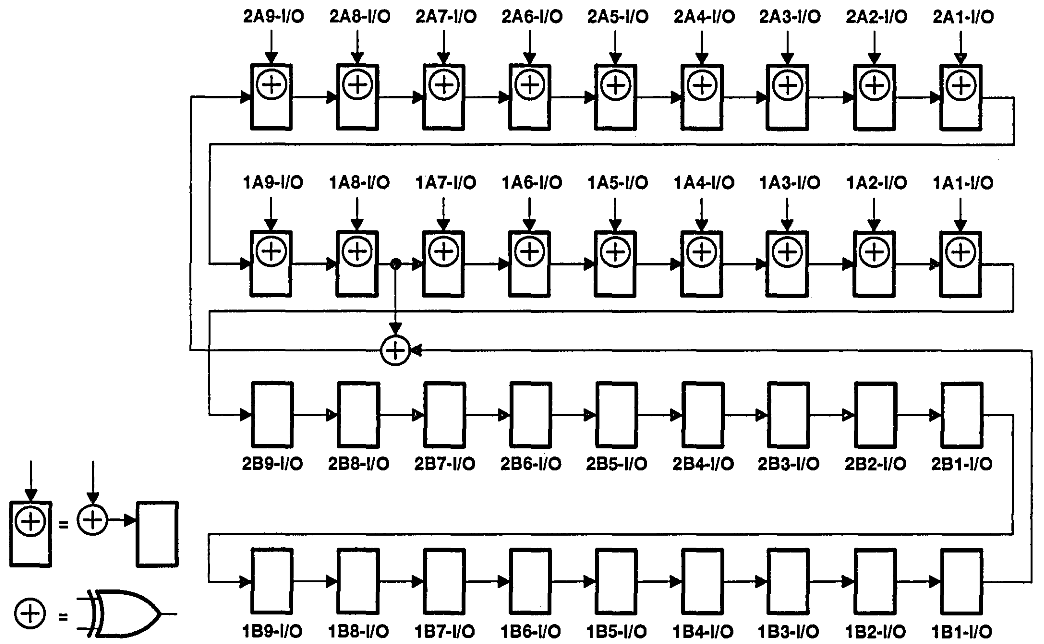


Figure 8. 36-Bit PSA Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)

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2B9-I/O 2B8-I/O 2B7-I/O 2B6-I/O 2B5-I/O 2B4-I/O 2B3-I/O 2B2-I/O 2B1-I/O

1B9-I/O 1B8-I/O 1B7-I/O 1B6-I/O 1B5-I/O 1B4-I/O 1B3-I/O 1B2-I/O 1B1-I/O

2A9-I/O 2A8-I/O 2A7-I/O 2A6-I/O 2A5-I/O 2A4-I/O 2A3-I/O 2A2-I/O 2A1-I/O

1A9-I/O 1A8-I/O 1A7-I/O 1A6-I/O 1A5-I/O 1A4-I/O 1A3-I/O 1A2-I/O 1A1-I/O

Figure 9. 36-Bit PSA Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

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### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 10 and 11 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

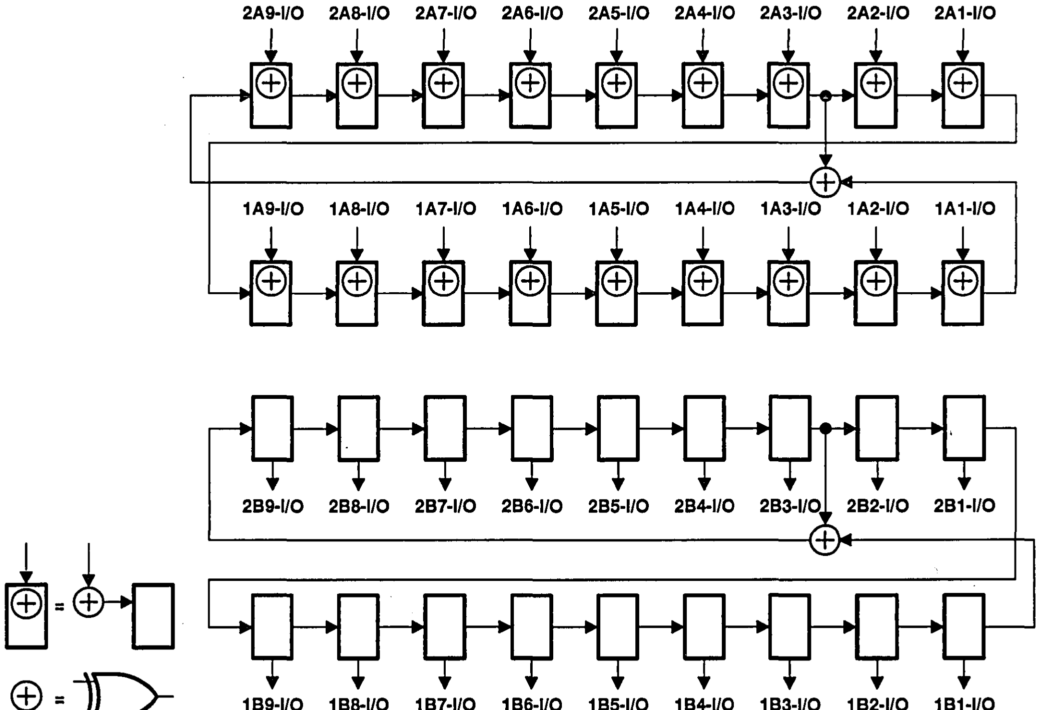


**Figure 10. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

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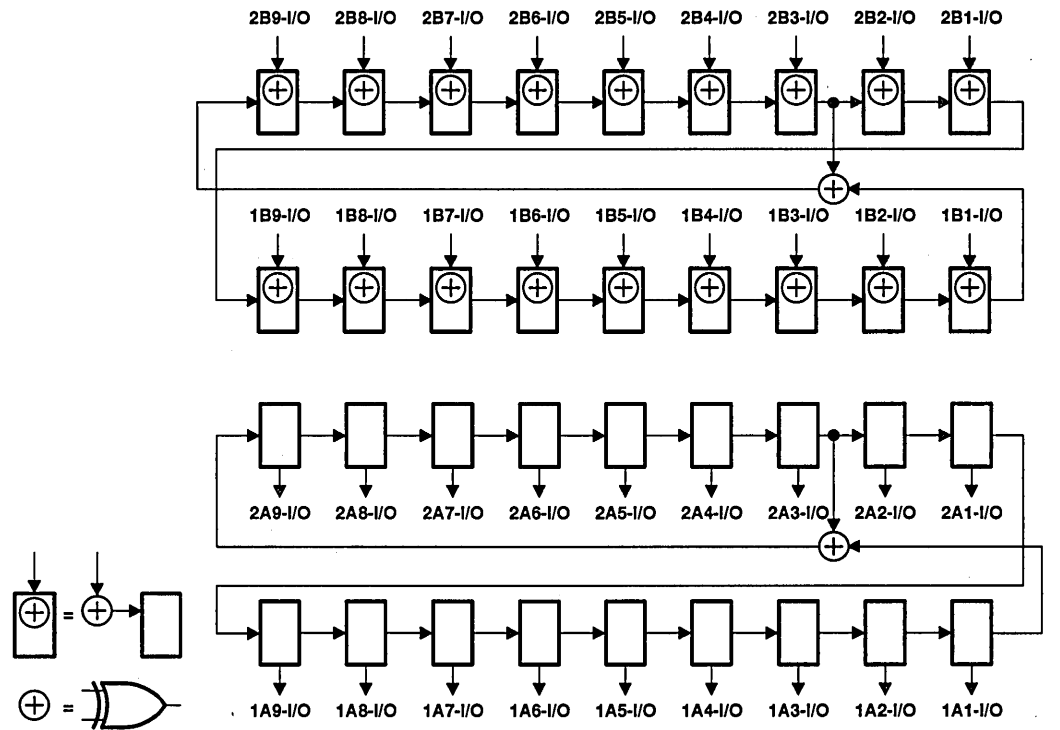


Figure 11. 18-Bit PSA/PRPG Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)

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### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 12 and 13 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

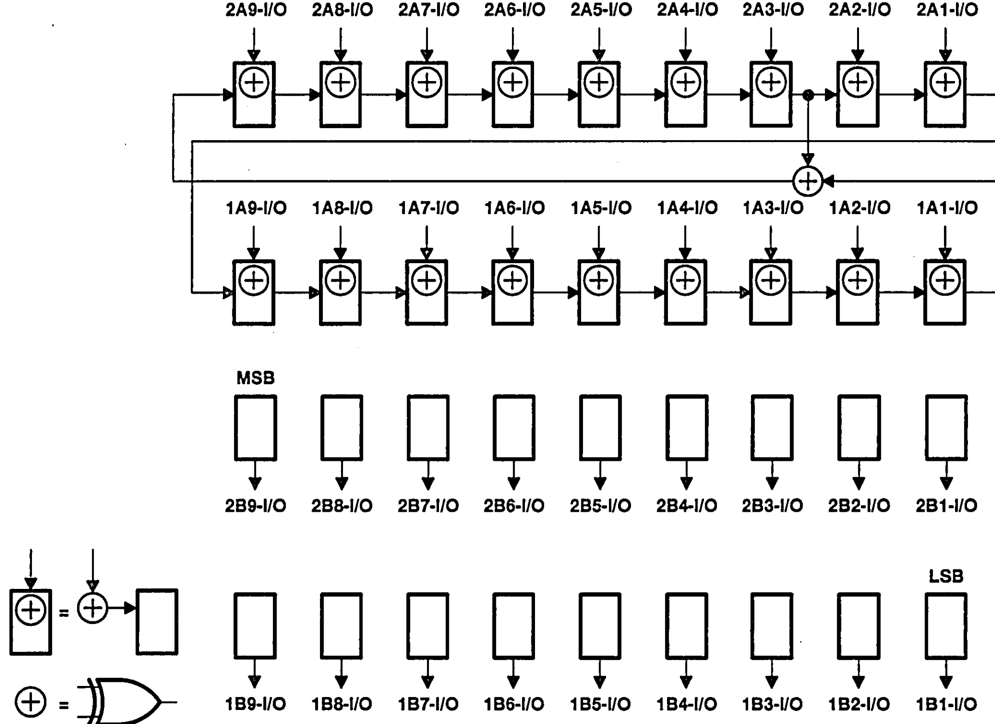


**Figure 12. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 0, 1OEB = 2OEB = 1)**

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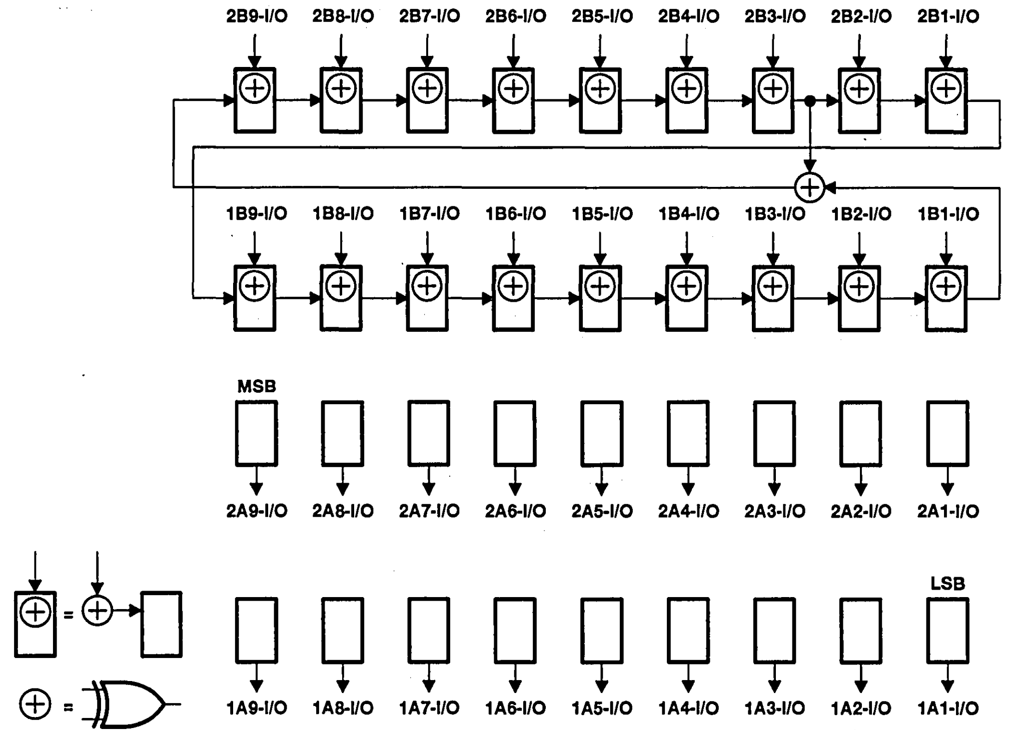


**Figure 13. 18-Bit PSA/COUNT Configuration (1OEA = 2OEA = 1, 1OEB = 2OEB = 0)**





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## timing description

All test operations of the 'LVTH18646A and 'LVTH182646A are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 2) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 14. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

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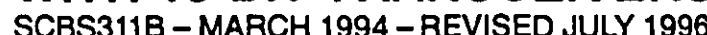


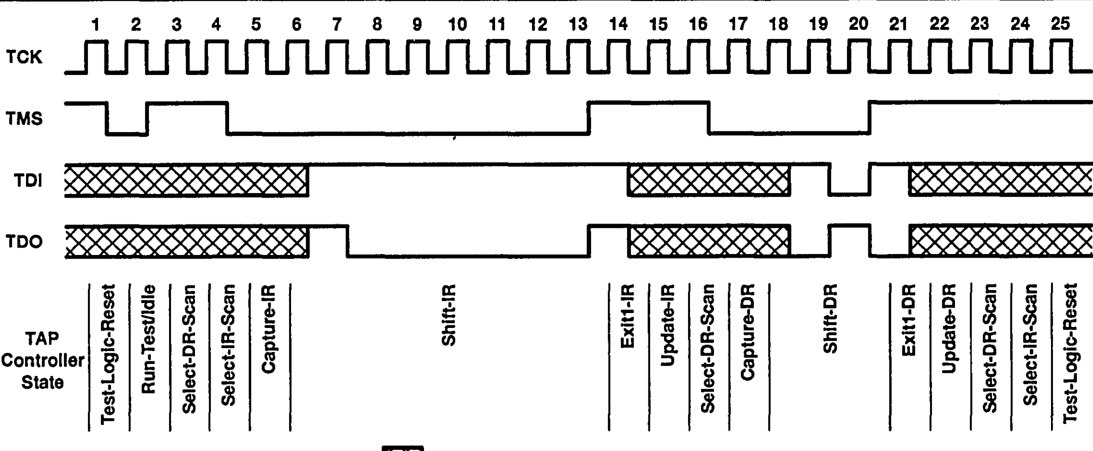



**Figure 14. Timing Example**

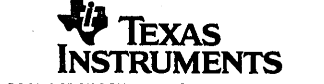


## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 4.6 V |
| Input voltage range, $V_I$ (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) | –0.5 V to 7 V |
| Current into any output in the low state, $I_O$: SN54LVTH18646A | 96 mA |
| SN54LVTH182646A (A port or TDO) | 96 mA |
| SN54LVTH182646A (B port) | 30 mA |
| SN74LVTH18646A | 128 mA |
| SN74LVTH182646A (A port or TDO) | 128 mA |
| SN74LVTH182646A (B port) | 30 mA |
| Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH18646A | 48 mA |
| SN54LVTH182646A (A port or TDO) | 48 mA |
| SN54LVTH182646A (B port) | 30 mA |
| SN74LVTH18646A | 64 mA |
| SN74LVTH182646A (A port or TDO) | 64 mA |
| SN74LVTH182646A (B port) | 30 mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | –50 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | –50 mA |
| Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): PM package | 1 W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the ABT *Advanced BiCMOS Technology Data Book*, literature number SCBD002.



## recommended operating conditions

| | | | SN54LVTH18646A | | SN74LVTH18646A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | −24 | | −32 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 32 | mA |
| $I_{OL}$† | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH18646A | | | SN74LVTH18646A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| $I_I$ | CLK, DIR, S, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 50 | | | 50 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | | 75 | | | µA |
| | | | $V_I$ = 2 V | –75 | | | –75 | | | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | | | 1 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 2 | | | 2 | mA |
| | | | Outputs low | | | 30 | | | 30 | |
| | | | Outputs disabled | | | 2 | | | 2 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 11 | | | 11 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)**

| | | | SN54LVTH18646A | | | | SN74LVTH18646A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | | | 0 | 100 | | | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | | 5 | | | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | | 4 | | | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | | | 1 | | | | ns |

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)**

| | | | SN54LVTH18646A | | | | SN74LVTH18646A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, CLK, DIR, $\overline{OE}$ or S before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, CLK, DIR, $\overline{OE}$ or S after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18646A | | | | SN74LVTH18646A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | | | | | 100 | | | | MHz |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 6 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6 | | | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PLH}$ | SAB or SBA | B or A | | | | | 1.5 | 8 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 8 | | | |
| $t_{PZH}$ | DIR | B or A | | | | | 2 | 12 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 12 | | | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | | | | | 2 | 12 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 12 | | | |
| $t_{PHZ}$ | DIR | B or A | | | | | 3 | 12 | | | ns |
| $t_{PLZ}$ | | | | | | | 3 | 12 | | | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | | | | | 2 | 11 | | | ns |
| $t_{PLZ}$ | | | | | | | 2 | 11 | | | |

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18646A | | | | SN74LVTH18646A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 15 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 15 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 3 | 18 | | | ns |
| $t_{PZL}$ | | | | | | | 3 | 18 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 3 | 19 | | | ns |
| $t_{PLZ}$ | | | | | | | 3 | 19 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 8 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 8 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## recommended operating conditions

| | | | SN54LVTH182646A | | SN74LVTH182646A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 24 | | 32 | mA |
| | | B port | | 12 | | 12 | |
| $I_{OL}$† | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)**

| PARAMETER | | TEST CONDITIONS | | SN54LVTH182646A | | | SN74LVTH182646A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| | | | $I_{OH}$ = –12 mA | 2 | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| | | | $I_{OL}$ = 12 mA | | | 0.8 | | | 0.8 | |
| $I_I$ | CLK, DIR, S, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 50 | | | 50 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | –25 | | –100 | |
| | A or B ports§ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | | 75 | | | µA |
| | | | $V_I$ = 2 V | –75 | | | –75 | | | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | | | 1 | µA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 2 | | | 2 | mA |
| | | | Outputs low | | | 35 | | | 35 | |
| | | | Outputs disabled | | | 2 | | | 2 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 11 | | | 11 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state ouput leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)

| | | | SN54LVTH182646A | | | | SN74LVTH182646A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | | | 0 | 100 | | | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | | 5 | | | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | | 4 | | | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | | | 1 | | | | ns |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)

| | | | SN54LVTH182646A | | | | SN74LVTH182646A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, CLK, DIR, $\overline{OE}$ or S before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, CLK, DIR, $\overline{OE}$ or S after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182646A | | | | SN74LVTH182646A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | | | | | 100 | | | | MHz |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | | | | | 1.5 | 8 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 8 | | | |
| $t_{PLH}$ | SAB or SBA | B or A | | | | | 1.5 | 9 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 9 | | | |
| $t_{PZH}$ | DIR | B or A | | | | | 2 | 13 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 13 | | | |
| $t_{PZH}$ | $\overline{OE}$ | B or A | | | | | 2 | 13 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 13 | | | |
| $t_{PHZ}$ | DIR | B or A | | | | | 3 | 13 | | | ns |
| $t_{PLZ}$ | | | | | | | 3 | 13 | | | |
| $t_{PHZ}$ | $\overline{OE}$ | B or A | | | | | 2 | 12 | | | ns |
| $t_{PLZ}$ | | | | | | | 2 | 12 | | | |

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182646A | | | | SN74LVTH182646A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 15 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 15 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 3 | 18 | | | ns |
| $t_{PZL}$ | | | | | | | 3 | 18 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 3 | 19 | | | ns |
| $t_{PLZ}$ | | | | | | | 3 | 19 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 8 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 8 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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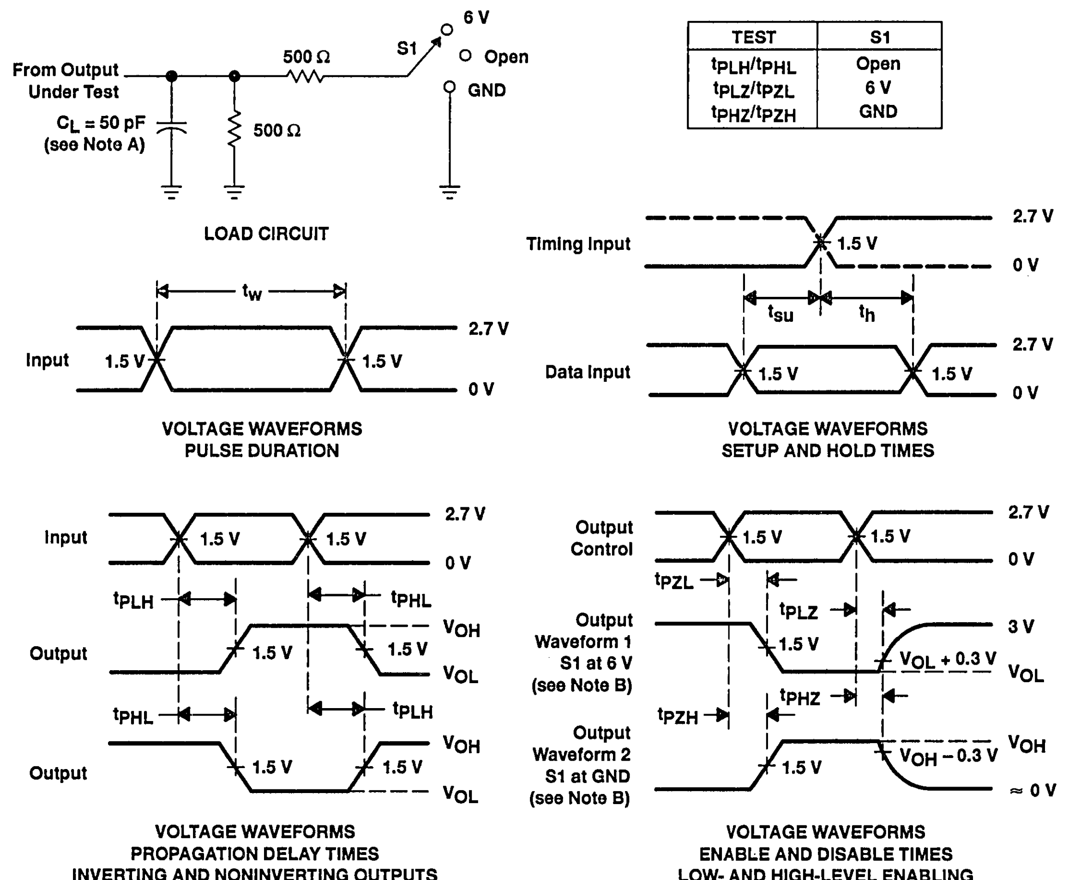
## PARAMETER MEASUREMENT INFORMATION

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 15. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)
- Support Unregulated Battery Operation Down to 2.7 V
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- B-Port Outputs of 'LVTH182652A Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

PRODUCT PREVIEW

## description

The 'LVTH18652A and 'LVTH182652A scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and $\overline{OEBA}$) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state.

Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and $\overline{OEBA}$ inputs. Since the $\overline{OEBA}$ input is active-low, the A outputs are active when $\overline{OEBA}$ is low and are in the high-impedance state when $\overline{OEBA}$ is high. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH18652A and 'LVTH182652A.

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## description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

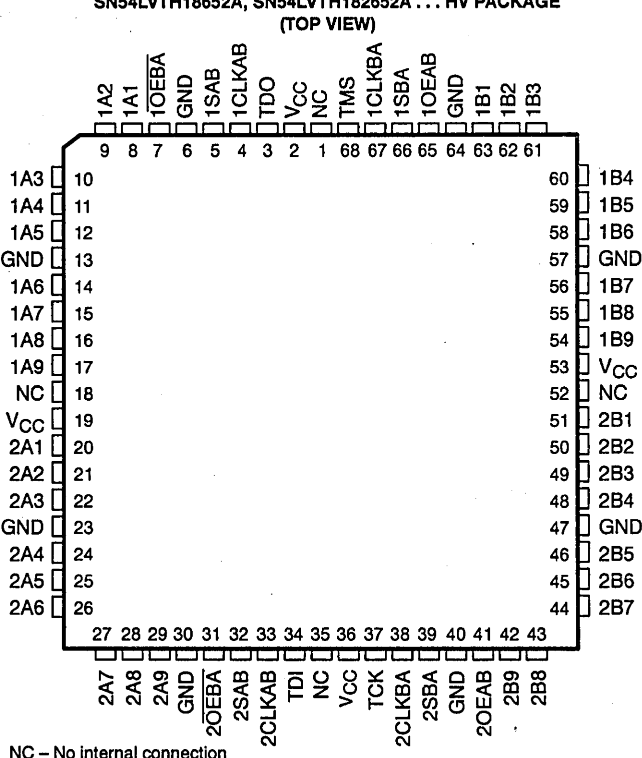
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVTH182652A, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54LVTH18652A and SN54LVTH182652A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH18652A and SN74LVTH182652A are characterized for operation from –40°C to 85°C.

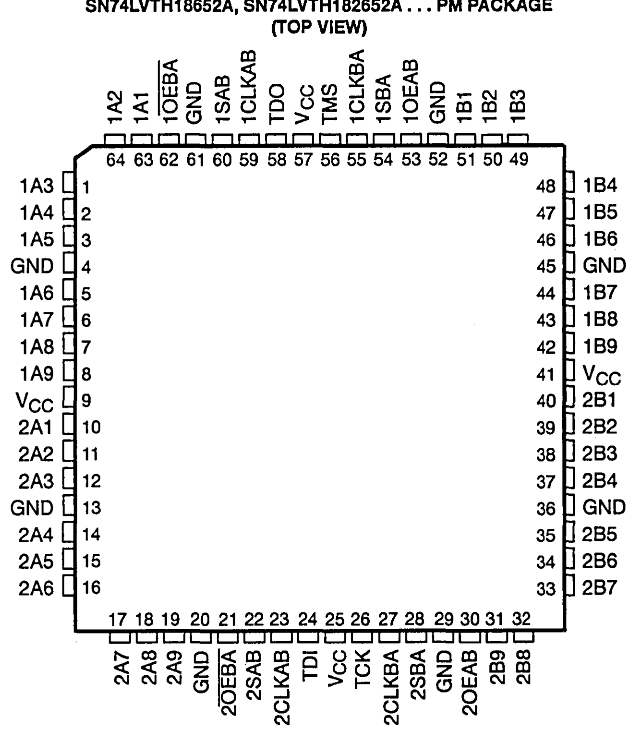
PRODUCT PREVIEW

SN54LVTH18652A, SN54LVTH182652A . . . HV PACKAGE
(TOP VIEW)




NC – No internal connection

**SN74LVTH18652A, SN74LVTH182652A . . . PM PACKAGE**
**(TOP VIEW)**




**FUNCTION TABLE**
**(normal mode, each 9-bit section)**

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA | A1–A9 | B1–B9 | |
| L | H | L | L | X | X | Input disabled | Input disabled | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | L | X | X | Input | Unspecified† | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | L | ↑ | X | X | Unspecified† | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | X | X | H | Output | Input | Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | X | X | H | X | Input | Output | Stored A data to B bus |
| H | L | X | X | H | H | Output | Output | Stored A data to B bus and stored B data to A bus |

† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or $\overline{OEBA}$. Data-input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered to load both registers.

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BUS A BUS B

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**

BUS A BUS B

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**

BUS A BUS B

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**

BUS A BUS B

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | L | X | X | H | H |

**TRANSFER STORED DATA**
**TO A AND/OR B**

**Figure 1. Bus-Management Functions**

## functional block diagram

Pin numbers shown are for the PM package.

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## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| GND | Ground |
| 1OEAB, 2OEAB | Normal-function active-high output enables. See function table for normal-mode logic. An internal pulldown at each terminal will force the terminal to a low level if left unconnected. |
| $1\overline{OEBA}$, $2\overline{OEBA}$ | Normal-function active-low output enables. See function table for normal-mode logic. An internal pullup at each terminal will force the terminal to a high level if left unconnected. |
| 1SAB, 1SBA, 2SAB, 2SBA | Normal-function select controls. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

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## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 2 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and four test-data registers: a 48-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.



**Figure 2. TAP-Controller State Diagram**

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## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram shown in Figure 2 is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers can also be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'LVTH18652A and 'LVTH182652A, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–46 in the boundary-scan register are reset to logic 0 while bits 45–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., such that if test mode were invoked the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

**Shift-DR (continued)**

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the 'LVTH18652A and 'LVTH182652A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to the active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

### register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

### instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'LVTH18652A and 'LVTH182652A. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 3.

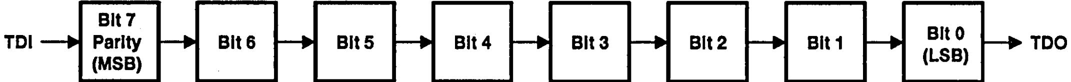


**Figure 3. Instruction Register Order of Scan**

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## data register description

### boundary-scan register

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle, as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–46 are reset to logic 0 while BSCs 45–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary-Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | 2OEAB | 35 | 2A9-I/O | 17 | 2B9-I/O |
| 46 | 1OEAB | 34 | 2A8-I/O | 16 | 2B8-I/O |
| 45 | 2$\overline{\text{OEBA}}$ | 33 | 2A7-I/O | 15 | 2B7-I/O |
| 44 | 1$\overline{\text{OEBA}}$ | 32 | 2A6-I/O | 14 | 2B6-I/O |
| 43 | 2CLKAB | 31 | 2A5-I/O | 13 | 2B5-I/O |
| 42 | 1CLKAB | 30 | 2A4-I/O | 12 | 2B4-I/O |
| 41 | 2CLKBA | 29 | 2A3-I/O | 11 | 2B3-I/O |
| 40 | 1CLKBA | 28 | 2A2-I/O | 10 | 2B2-I/O |
| 39 | 2SAB | 27 | 2A1-I/O | 9 | 2B1-I/O |
| 38 | 1SAB | 26 | 1A9-I/O | 8 | 1B9-I/O |
| 37 | 2SBA | 25 | 1A8-I/O | 7 | 1B8-I/O |
| 36 | 1SBA | 24 | 1A7-I/O | 6 | 1B7-I/O |
| — | — | 23 | 1A6-I/O | 5 | 1B6-I/O |
| — | — | 22 | 1A5-I/O | 4 | 1B5-I/O |
| — | — | 21 | 1A4-I/O | 3 | 1B4-I/O |
| — | — | 20 | 1A3-I/O | 2 | 1B3-I/O |
| — | — | 19 | 1A2-I/O | 1 | 1B2-I/O |
| — | — | 18 | 1A1-I/O | 0 | 1B1-I/O |

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### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is shown in Figure 4.

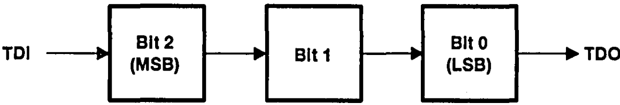


**Figure 4. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 5.

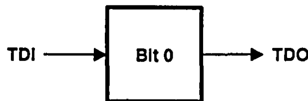


**Figure 5. Bypass Register Order of Scan**

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### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'LVTH18652A, the binary value 00100000000000011111000000101111 (2001F02F, hex) is captured (during Capture-DR state) in the device-identification register to identify this device as Texas Instruments SN54/74LVTH18652A.

For the 'LVTH182652A, the binary value 00100000000000100100000000101111 (2002402F, hex) is captured (during Capture-DR state) in the device-identification register to identify this device as Texas Instruments SN54/74LVTH182652A.

The device-identification register order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the device-identification register bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

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## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS‡ | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'LVT18652 or 'LVT182652.

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### boundary scan

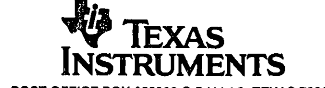
This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–44 of the BSR). When a given output enable is active (logic 0 for $\overline{OEBA}$, logic 1 for OEAB), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The device identification register is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.



**bypass scan**

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

**boundary-run test**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

**boundary read**

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

**boundary self test**

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

**boundary toggle outputs**

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

**boundary-control-register scan**

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

PRODUCT PREVIEW

## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

**Table 4. Boundary-Control Register Opcodes**

| BINARY CODE<br>BIT 2 → BIT 0<br>MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 47–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 47–44 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when both bytes of the device are operating in one direction of data flow (that is, 1OEAB = 1$\overline{\text{OEBA}}$ and 2OEAB = 2$\overline{\text{OEBA}}$) and in the same direction of data flow (that is, 1OEAB = 2OEAB and 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

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### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 6 and 7 illustrate the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR prior to performing this operation. A seed value of all zeroes will not produce additional patterns.

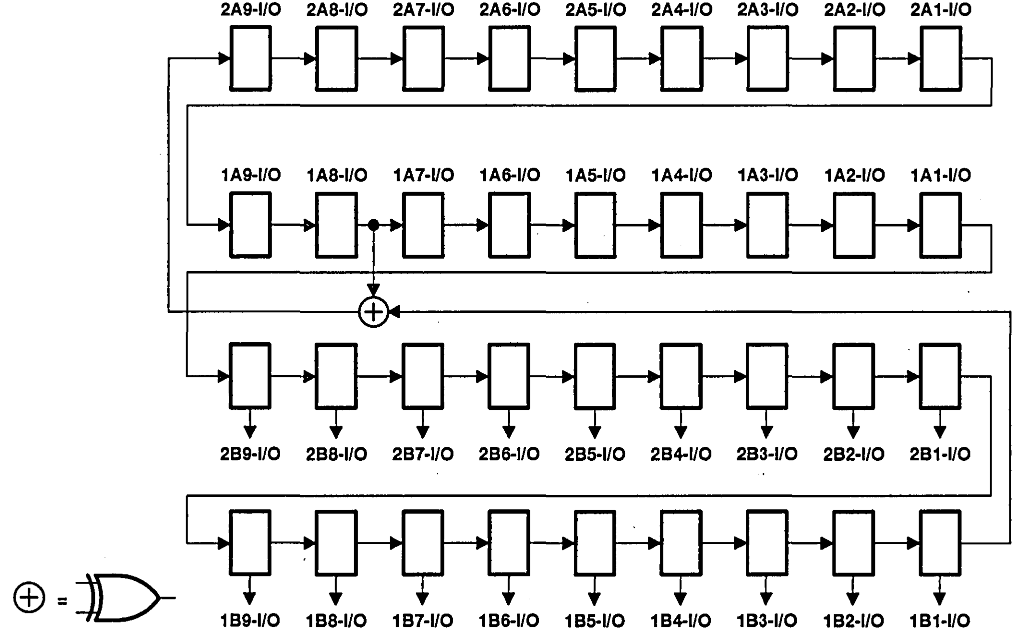


**Figure 6. 36-Bit PRPG Configuration (1OEAB = 2OEAB = 1, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 1)**

PRODUCT PREVIEW

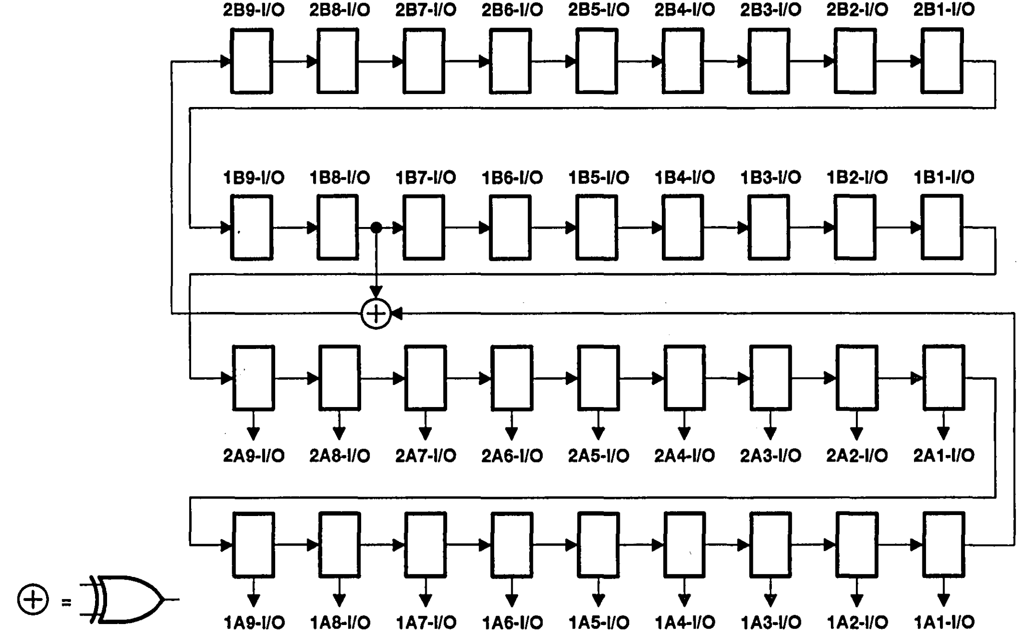


**Figure 7. 36-Bit PRPG Configuration (1OEAB = 2OEAB = 0, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 0)**

**parallel-signature analysis (PSA)**

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 8 and 9 illustrate the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

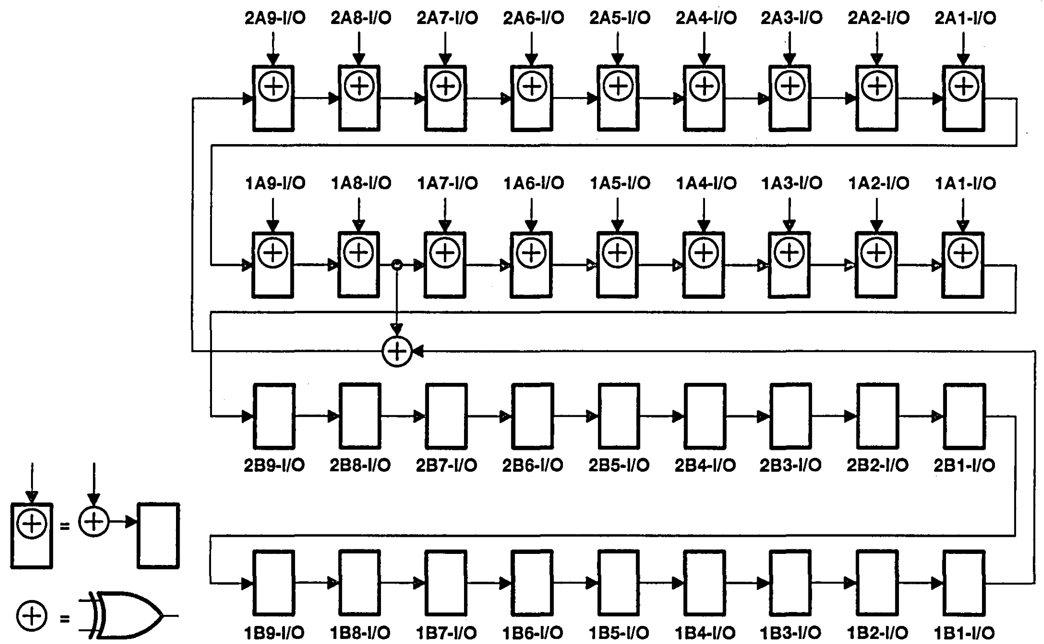


**Figure 8. 36-Bit PSA Configuration (1OEAB = 2OEAB = 1, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 1)**

PRODUCT PREVIEW

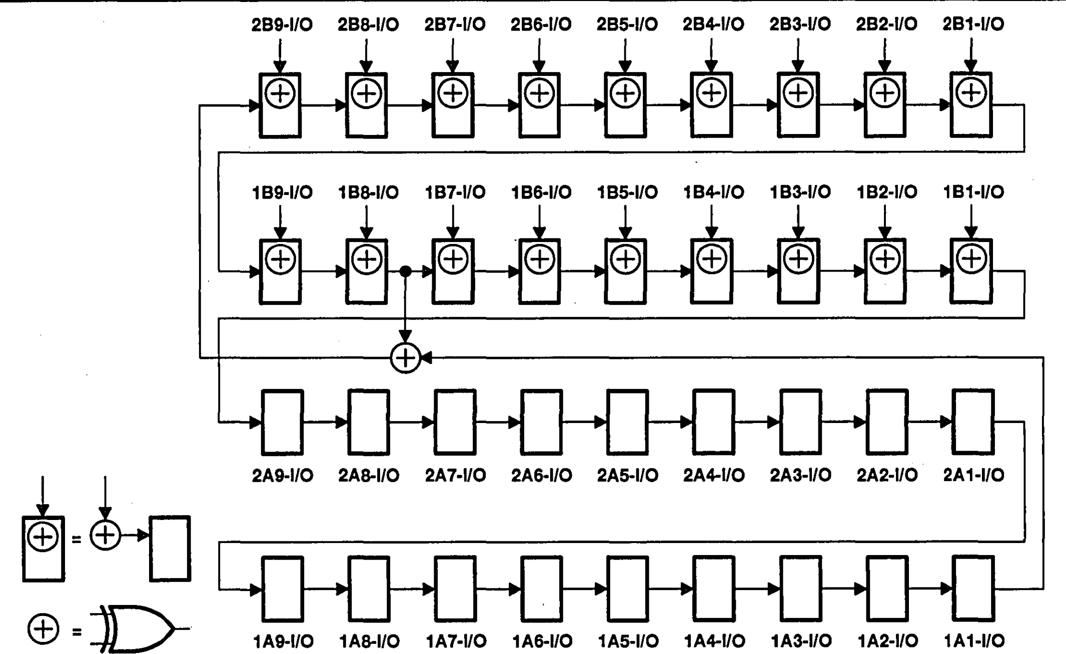


Figure 9. 36-Bit PSA Configuration (1OEAB = 2OEAB = 0, $1\overline{OEBA}$ = $2\overline{OEBA}$ = 0)

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### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 10 and 11 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes will not produce additional patterns.

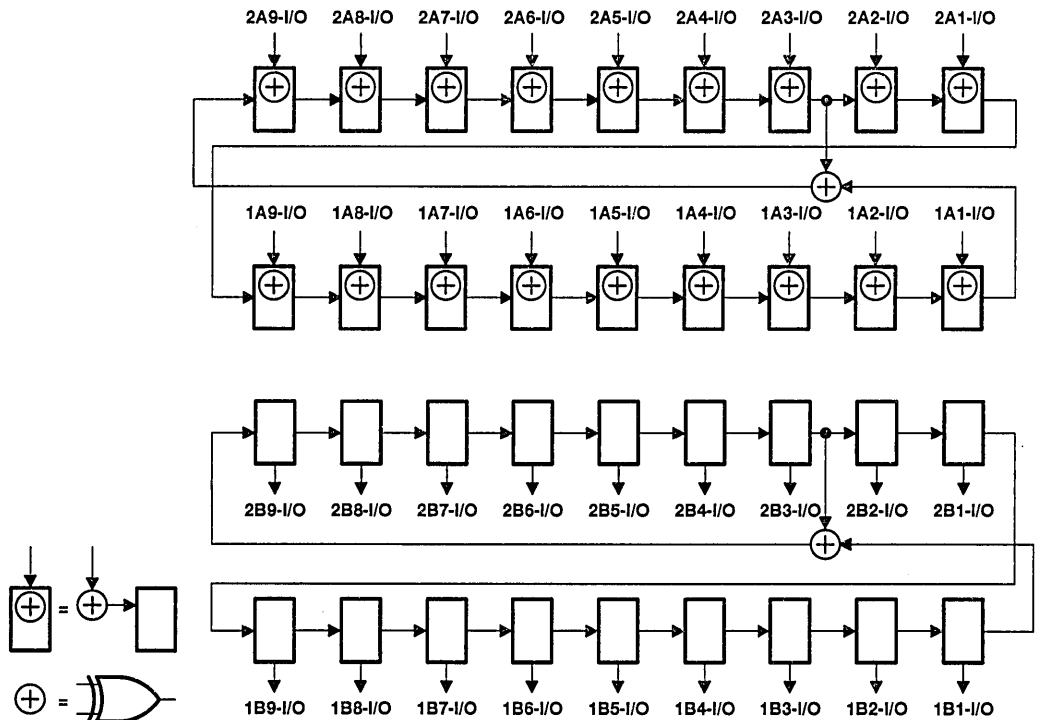


**Figure 10. 18-Bit PSA/PRPG Configuration (1OEAB = 2OEAB = 1, $\overline{1OEBA}$ = $\overline{2OEBA}$ = 1)**

PRODUCT PREVIEW

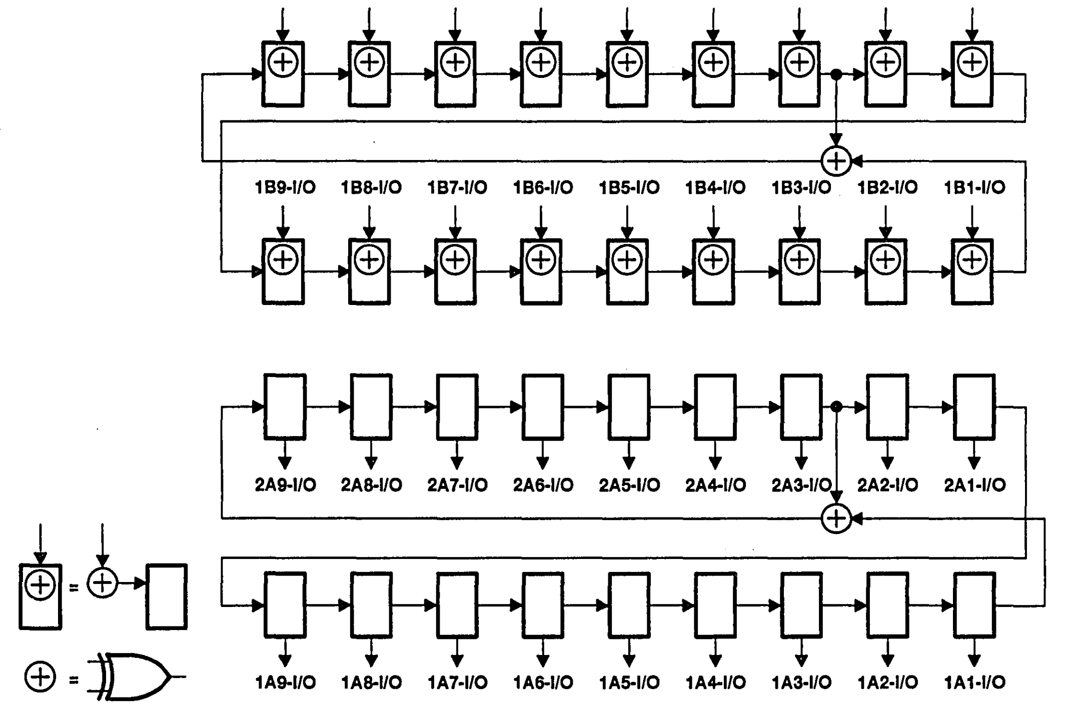


Figure 11. 18-Bit PSA/PRPG Configuration (1OEAB = 2OEAB = 0, $1\overline{OEBA} = 2\overline{OEBA} = 0$)

PRODUCT PREVIEW

**simultaneous PSA and binary count up (PSA/COUNT)**

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 12 and 13 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

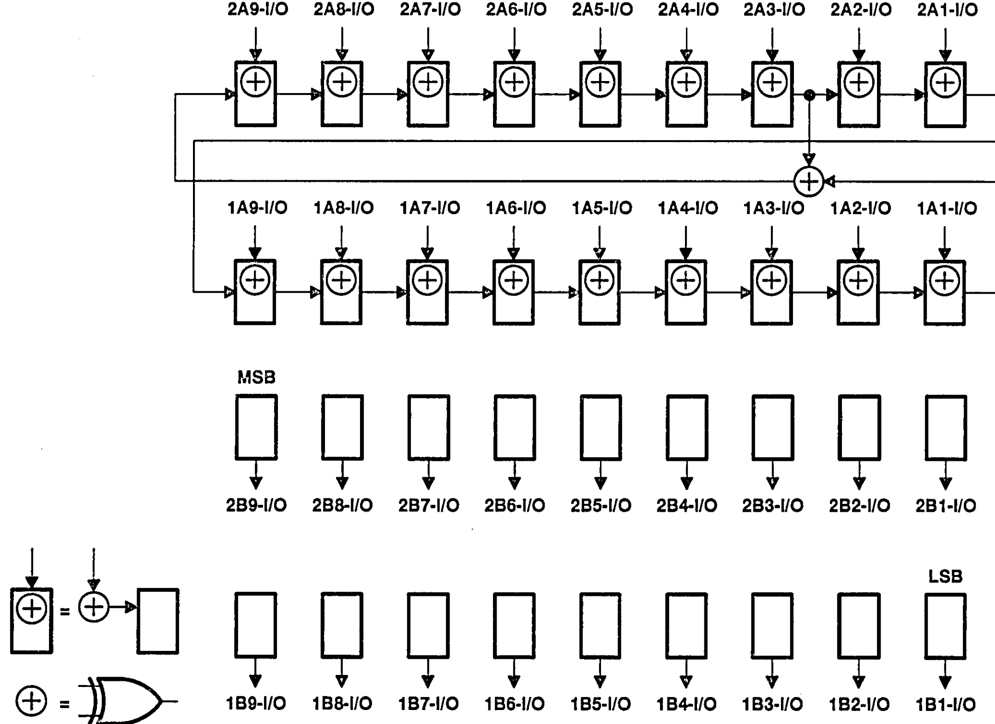


**Figure 12. 18-Bit PSA/COUNT Configuration (1OEAB = 2OEAB = 1, $\overline{1OEBA}$ = $\overline{2OEBA}$ = 1)**

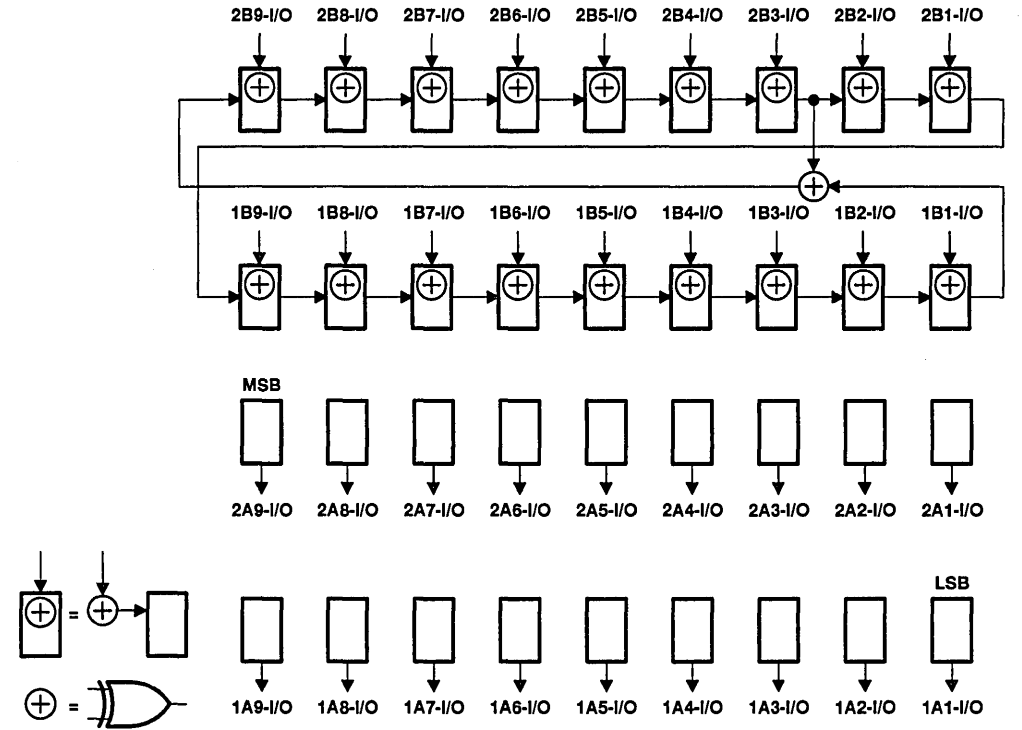


Figure 13. 18-Bit PSA/COUNT Configuration (1OEAB = 2OEAB = 0, $1\overline{OEBA} = 2\overline{OEBA} = 0$)

PRODUCT PREVIEW

## timing description

All test operations of the 'LVTH18652A and 'LVTH182652A are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 2) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 14. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

PRODUCT PREVIEW

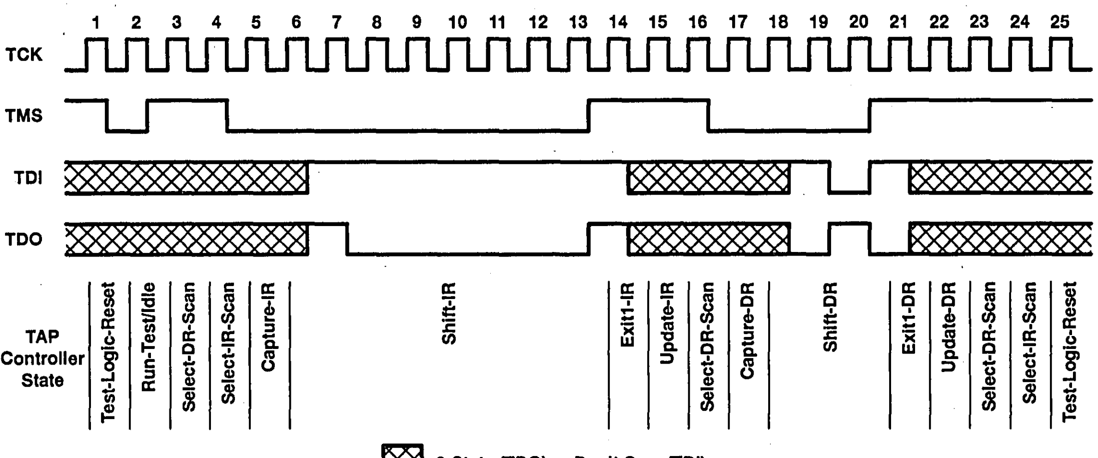


Figure 14. Timing Example



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .......... –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .......... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) .... –0.5 V to 7 V
Current into any output in the low state, $I_O$: SN54LVTH18652A .......... 96 mA
SN54LVTH182652A (A port or TDO) .......... 96 mA
SN54LVTH182652A (B port) .......... 30 mA
SN74LVTH18652A .......... 128 mA
SN74LVTH182652A (A port or TDO) .......... 128 mA
SN74LVTH182652A (B port) .......... 30 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH18652A .......... 48 mA
SN54LVTH182652A (A port or TDO) .... 48 mA
SN54LVTH182652A (B port) .......... 30 mA
SN74LVTH18652A .......... 64 mA
SN74LVTH182652A (A port or TDO) .... 64 mA
SN74LVTH182652A (B port) .......... 30 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) .......... –50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) .......... –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): PM package .......... 1 W
Storage temperature range, $T_{stg}$ .......... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the ABT *Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54LVTH18652A | | SN74LVTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | 32 | mA |
| $I_{OL}$† | Low-level output current | | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | TEST CONDITIONS | | | SN54LVTH18652A | | | SN74LVTH18652A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | | 2.4 | | | 2.4 | | | |
| | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | | 2.4 | | | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | | 2 | | | | | | |
| | | $I_{OH}$ = –32 mA | | | | | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | | 0.2 | | | 0.2 | V |
| | | $I_{OL}$ = 24 mA | | | | 0.5 | | | 0.5 | |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 32 mA | | | | 0.5 | | | 0.5 | |
| | | $I_{OL}$ = 48 mA | | | | 0.55 | | | | |
| | | $I_{OL}$ = 64 mA | | | | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | CLK, S, TCK | | | ±1 | | | ±1 | µA |
| | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | | 10 | | | 10 | |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | $\overline{OEBA}$, TDI, TMS | | | 50 | | | 50 | |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | –25 | | –100 | –25 | | –100 | |
| | | $V_I$ = 5.5 V | OEAB | 35 | | 150 | 35 | | 150 | µA |
| | | $V_I$ = $V_{CC}$ | | 25 | | 100 | 25 | | 100 | |
| | | $V_I$ = 0 | | | | –5 | | | –5 | |
| | | $V_I$ = 5.5 V | A or B ports§ | | | 20 | | | 20 | µA |
| | | $V_I$ = $V_{CC}$ | | | | 1 | | | 1 | |
| | | $V_I$ = 0 | | | | –5 | | | –5 | |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | A or B ports | 75 | | | 75 | | | µA |
| | | $V_I$ = 2 V | | –75 | | | –75 | | | |
| $I_{OZH}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | TDO | | | 1 | | | 1 | µA |
| $I_{OZL}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | TDO | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs high | | | 2 | | | 2 | mA |
| | | | Outputs low | | | 30 | | | 30 | |
| | | | Outputs disabled | | | 2 | | | 2 | |
| $\Delta I_{CC}$# | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | $V_I$ = 3 V or 0 | | | | 4 | | | 4 | | pF |
| $C_{io}$ | $V_O$ = 3 V or 0 | | | | 11 | | | 11 | | pF |
| $C_o$ | $V_O$ = 3 V or 0 | | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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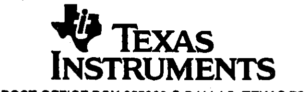



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## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)

| | | | SN54LVTH18652A | | | | SN74LVTH18652A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | | | 0 | 100 | | | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | | 5 | | | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | | 4 | | | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | | | 1 | | | | ns |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)

| | | | SN54LVTH18652A | | | | SN74LVTH18652A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, CLK, OEAB, $\overline{OEBA}$ or S before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, CLK, OEAB, $\overline{OEBA}$ or S after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18652A | | | | SN74LVTH18652A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | | | | | 100 | | | | MHz |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 6 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 6 | | | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PLH}$ | SAB or SBA | B or A | | | | | 1.5 | 8 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 8 | | | |
| $t_{PZH}$ | OEAB or $\overline{OEBA}$ | B or A | | | | | 2 | 10 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 10 | | | |
| $t_{PHZ}$ | OEAB or $\overline{OEBA}$ | B or A | | | | | 1.5 | 11 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 11 | | | |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH18652A | | | | SN74LVTH18652A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 15 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 15 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 3 | 18 | | | ns |
| $t_{PZL}$ | | | | | | | 3 | 18 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 3 | 19 | | | ns |
| $t_{PLZ}$ | | | | | | | 3 | 19 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 8 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 8 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## recommended operating conditions

| | | | SN54LVTH182652A | | SN74LVTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | A port, TDO | | –24 | | –32 | mA |
| | | B port | | –12 | | –12 | |
| $I_{OL}$ | Low-level output current | A port, TDO | | 24 | | 32 | mA |
| | | B port | | 12 | | 12 | |
| $I_{OL}$† | Low-level output current | A port, TDO | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)**

| PARAMETER | TEST CONDITIONS | | | SN54LVTH182652A MIN | SN54LVTH182652A TYP† | SN54LVTH182652A MAX | SN74LVTH182652A MIN | SN74LVTH182652A TYP† | SN74LVTH182652A MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | A port, TDO | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | A port, TDO | 2.4 | | | 2.4 | | | V |
| | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | A port, TDO | 2.4 | | | 2.4 | | | V |
| | $V_{CC}$ = 3 V | $I_{OH}$ = –24 mA | A port, TDO | 2 | | | | | | V |
| | $V_{CC}$ = 3 V | $I_{OH}$ = –32 mA | A port, TDO | | | | 2 | | | V |
| | $V_{CC}$ = 3 V | $I_{OH}$ = –12 mA | B port | 2 | | | 2 | | | V |
| $V_{OL}$ | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | A port, TDO | | | 0.2 | | | 0.2 | V |
| | $V_{CC}$ = 2.7 V | $I_{OL}$ = 24 mA | A port, TDO | | | 0.5 | | | 0.5 | V |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | A port, TDO | | | 0.4 | | | 0.4 | V |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 32 mA | A port, TDO | | | 0.5 | | | 0.5 | V |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 48 mA | A port, TDO | | | 0.55 | | | | V |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 64 mA | A port, TDO | | | | | | 0.55 | V |
| | $V_{CC}$ = 3 V | $I_{OL}$ = 12 mA | B port | | | 0.8 | | | 0.8 | V |
| $I_I$ | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | CLK, S, TCK | | | ±1 | | | ±1 | µA |
| | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | CLK, S, TCK | | | 10 | | | 10 | µA |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | $\overline{OEBA}$, TDI, TMS | | | 50 | | | 50 | µA |
| | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ | $\overline{OEBA}$, TDI, TMS | | | 1 | | | 1 | µA |
| | $V_{CC}$ = 3.6 V | $V_I$ = 0 | $\overline{OEBA}$, TDI, TMS | –25 | | –100 | –25 | | –100 | µA |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | OEAB | 35 | | 150 | 35 | | 150 | µA |
| | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ | OEAB | 25 | | 100 | 25 | | 100 | µA |
| | $V_{CC}$ = 3.6 V | $V_I$ = 0 | OEAB | | | –5 | | | –5 | µA |
| | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | A or B ports§ | | | 20 | | | 20 | µA |
| | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ | A or B ports§ | | | 1 | | | 1 | µA |
| | $V_{CC}$ = 3.6 V | $V_I$ = 0 | A or B ports§ | | | –5 | | | –5 | µA |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | | ±100 | µA |
| $I_{I(hold)}$¶ | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | A or B ports | 75 | | | 75 | | | µA |
| | $V_{CC}$ = 3 V | $V_I$ = 2 V | A or B ports | –75 | | | –75 | | | µA |
| $I_{OZH}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | TDO | | | 1 | | | 1 | µA |
| $I_{OZL}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | TDO | | | –1 | | | –1 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | TDO | | | ±50 | | | ±50 | µA |
| $I_{CC}$ | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs high | | | 2 | | | 2 | mA |
| | | | Outputs low | | | 35 | | | 35 | mA |
| | | | Outputs disabled | | | 2 | | | 2 | mA |
| $\Delta I_{CC}$# | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | | 0.2 | | | 0.2 | mA |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at $V_{CC}$ or GND
¶ The parameter $I_{I(hold)}$ includes the off-state output current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER | TEST CONDITIONS | SN54LVTH182652A | | | SN74LVTH182652A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $C_i$ | $V_I$ = 3 V or 0 | | 4 | | | 4 | | pF |
| $C_{io}$ | $V_O$ = 3 V or 0 | | 11 | | | 11 | | pF |
| $C_o$ | $V_O$ = 3 V or 0 | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)

| | | | SN54LVTH182652A | | | | SN74LVTH182652A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | | | 0 | 100 | | | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | | 5 | | | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | | 4 | | | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | | | 1 | | | | ns |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)

| | | | SN54LVTH182652A | | | | SN74LVTH182652A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | | | | 0 | 50 | | | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | | 9.5 | | | | ns |
| $t_{su}$ | Setup time | A, B, CLK, OEAB, $\overline{OEBA}$ or S before TCK↑ | | | | | 6.5 | | | | ns |
| | | TDI before TCK↑ | | | | | 2.5 | | | | |
| | | TMS before TCK↑ | | | | | 2.5 | | | | |
| $t_h$ | Hold time | A, B, CLK, OEAB, $\overline{OEBA}$ or S after TCK↑ | | | | | 1.5 | | | | ns |
| | | TDI after TCK↑ | | | | | 1.5 | | | | |
| | | TMS after TCK↑ | | | | | 1.5 | | | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | | 50 | | | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | | 1 | | | | µs |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Note 4 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182652A | | | | SN74LVTH182652A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | | | | | 100 | | | | MHz |
| $t_{PLH}$ | A or B | B or A | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | | | | | 1.5 | 8 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 8 | | | |
| $t_{PLH}$ | SAB or SBA | B or A | | | | | 1.5 | 9 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 9 | | | |
| $t_{PZH}$ | OEAB or $\overline{OEBA}$ | B or A | | | | | 2 | 11 | | | ns |
| $t_{PZL}$ | | | | | | | 2 | 11 | | | |
| $t_{PHZ}$ | OEAB or $\overline{OEBA}$ | B or A | | | | | 1.5 | 12 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 12 | | | |

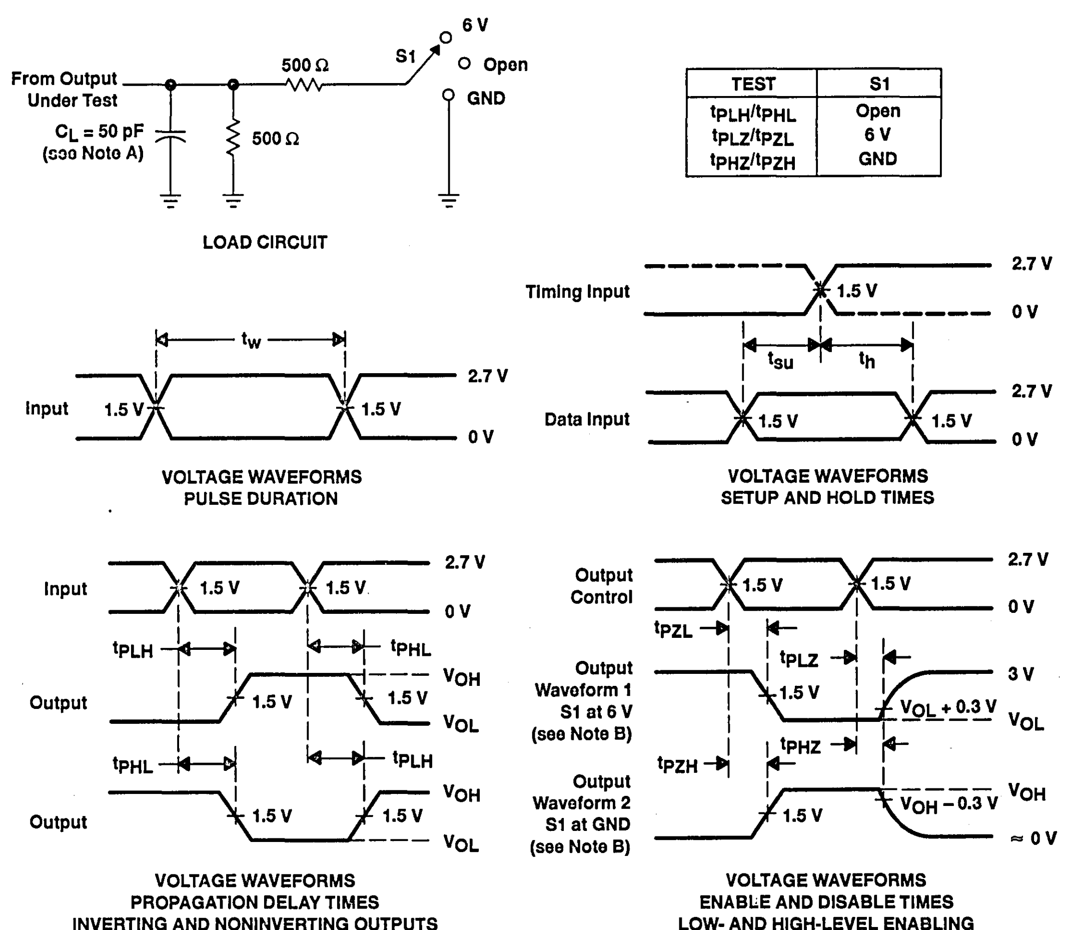
PRODUCT PREVIEW

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Note 4 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH182652A | | | | SN74LVTH182652A | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | | | | | 50 | | | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | 2.5 | 15 | | | ns |
| $t_{PHL}$ | | | | | | | 2.5 | 15 | | | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PHL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | 3 | 18 | | | ns |
| $t_{PZL}$ | | | | | | | 3 | 18 | | | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | 1.5 | 7 | | | ns |
| $t_{PZL}$ | | | | | | | 1.5 | 7 | | | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | 3 | 19 | | | ns |
| $t_{PLZ}$ | | | | | | | 3 | 19 | | | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | 1.5 | 8 | | | ns |
| $t_{PLZ}$ | | | | | | | 1.5 | 8 | | | |

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

## PARAMETER MEASUREMENT INFORMATION




PRODUCT PREVIEW

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 15. Load Circuit and Voltage Waveforms**

General Information 1

SN54/74BCT Octals 2

SN54/74ABT Octals 3

SN54/74ABT Widebus™ With Dual-Sided Terminals 4

SN54/74ABT Widebus™ With Quad-Sided Terminals 5

SN54/74LVT Widebus™ With Dual-Sided Terminals 6

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Technical Information A

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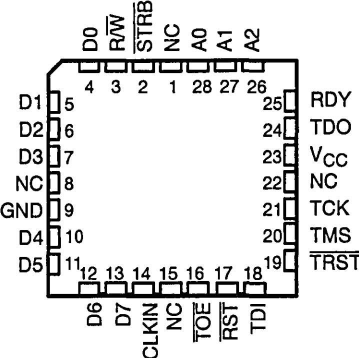
- Members of Texas Instruments Broad Family of Testability Products Supporting IEEE Std 1149.1-1990 (JTAG) Test Access Port (TAP) and Boundary-Scan Architecture
- Provide Built-In Access to IEEE Std 1149.1 Scan-Accessible Test/Maintenance Facilities at Board and System Levels
- While Powered at 3.3 V, the TAP Interface Is Fully 5-V Tolerant for Mastering Both 5-V and/or 3.3-V IEEE Std 1149.1 Targets
- Simple Interface to Low-Cost 3.3-V Microprocessors/Microcontrollers Via 8-Bit Asynchronous Read/Write Data Bus
- Easy Programming Via Scan-Level Command Set and Smart TAP Control
- Transparently Generate Protocols to Support Multidrop TAP Configurations Using TI's Addressable Scan Port
- Flexible TCK Generator Provides Programmable Division, Gated-TCK, and Free-Running-TCK Modes
- Discrete TAP Control Mode Supports Arbitrary TMS/TDI Sequences for Non-Compliant Targets
- Programmable 32-Bit Test Cycle Counter Allows Virtually Unlimited Scan/Test Length
- Accommodate Target Retiming (Pipeline) Delays of Up to 15 TCK Cycles
- Test Output Enable ($\overline{TOE}$) Allows for External Control of TAP Signals
- High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$) at TAP Support Backplane Interface and/or High Fanout
- Package Options Include Plastic Small-Outline Packages (DW), Ceramic Chip Carriers (FK), and Ceramic 300-mil DIPs (JT)

SN54LVT8980 . . . JT PACKAGE
SN74LVT8980 . . . DW PACKAGE
(TOP VIEW)

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| $\overline{STRB}$ | 1 | 24 | A0 |
| R/$\overline{W}$ | 2 | 23 | A1 |
| D0 | 3 | 22 | A2 |
| D1 | 4 | 21 | RDY |
| D2 | 5 | 20 | TDO |
| D3 | 6 | 19 | $V_{CC}$ |
| GND | 7 | 18 | TCK |
| D4 | 8 | 17 | TMS |
| D5 | 9 | 16 | $\overline{TRST}$ |
| D6 | 10 | 15 | TDI |
| D7 | 11 | 14 | $\overline{RST}$ |
| CLKIN | 12 | 13 | $\overline{TOE}$ |

SN54LVT8980 . . . FK PACKAGE
(TOP VIEW)




NC – No internal connection

## description

The 'LVT8980 embedded test-bus controllers (eTBC) are members of Texas Instruments broad family of testability integrated circuits. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit assemblies. Unlike most other devices of this family, the eTBC is not a boundary-scannable device; rather, its function is to master an IEEE Std 1149.1 (JTAG) test access port (TAP) under the command of an embedded host microprocessor/microcontroller. Thus, the eTBC enables the practical and effective use of the IEEE Std 1149.1 test-access infrastructure to support embedded/built-in test, emulation, and configuration/maintenance facilities at board and system levels.

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## description (continued)

The eTBC masters all TAP signals required to support one 4- or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset ($\overline{TRST}$). All such signals can be connected directly to the associated target IEEE Std 1149.1 devices without need for additional logic or buffering. However, as well as being directly connected, the TMS, TDI, and TDO signals can be connected to distant target IEEE Std 1149.1 devices via a pipeline, with a retiming delay of up to 15 TCK cycles; the eTBC automatically handles all associated serial-data justification.

Conceptually, the eTBC operates as a simple 8-bit memory- or I/O- mapped peripheral to a microprocessor/microcontroller (host). High-level commands and parallel data are passed to/from the eTBC via its generic host interface, which includes an 8-bit data bus (D7–D0) and a 3-bit address bus (A2–A0). Read/write select (R/$\overline{W}$) and strobe ($\overline{STRB}$) signals are implemented so that the critical host-interface timing is independent of the CLKIN period. An asynchronous ready (RDY) indicator is provided to hold off, or insert wait states into, a host read/write cycle when the eTBC cannot respond immediately to the requested read/write operation.

High-level commands are issued by the host to cause the eTBC to generate the TMS sequences necessary to move the test bus from any stable TAP-controller state to any other such stable state, to scan instruction or data through test registers in target devices, and/or to execute instructions in the Run-Test/Idle TAP state. A 32-bit counter can be programmed to allow a predetermined number of scan or execute cycles.

During scan operations, serial data that appears at the TDI input is transferred into a serial-to-4 × 8-bit-parallel first-in/first-out (FIFO) read buffer, which can then be read by the host to obtain the return serial-data stream up to eight bits at a time. Serial data that is to be transmitted from the TDO output is written by the host, up to eight bits at a time, to a 4 × 8-bit-parallel-to-serial FIFO write buffer.

In addition to such simple state-movement, scan, and run-test operations, the eTBC supports several additional commands that provide for input-only scans, output-only scans, recirculate scans (in which TDI is mirrored back to TDO), and a scan mode that generates the protocols used to support multidrop TAP configurations using TI's addressable scan port. Two loopback modes also are supported that allow the microprocessor/microcontroller host to monitor the TDO or TMS data streams output by the eTBC.

The eTBC's flexible clocking architecture allows the user to choose between free-running (in which the TCK always follows CLKIN) and gated modes (in which the TCK output is held static except during state-move, run-test, or scan cycles) as well as to divide down TCK from CLKIN. A discrete mode is also available in which the TAP is driven strictly by read/write cycles under full control of the microprocessor/microcontroller host. These features ensure that virtually any IEEE Std 1149.1 target device or device chain – even where such may not fully comply to IEEE Std 1149.1 – can be serviced by the eTBC.

While most operations of the eTBC are synchronous to CLKIN, a test-output enable ($\overline{TOE}$) is provided for output control of the TAP outputs, and a reset ($\overline{RST}$) input is provided for hardware reset of the eTBC. The former can be used to disable the eTBC so that an external controller can master the associated IEEE Std 1149.1 test bus.

The SN54LVT8980 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT8980 is characterized for operation from –40°C to 85°C.

## functional block diagram

$V_{CC}$
RST
RDY
$V_{CC}$
$V_{CC}$
STRB
TDI
TDI Buffer
R/W
Host Interface
Command/ Control
TDO Buffer
TDO
A2–A0
TAP-State Generator
TMS
D7–D0
TCK
Discrete Control
CLKIN
TCK Generator
TRST
$V_{CC}$
TOE

Pin numbers shown are for the DW and JT packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A2–A0 | Address inputs. A2–A0 form the 3-bit address bus that interfaces the eTBC to its microprocessor/microcontroller host. These inputs directly index the eTBC register to be accessed (read from or written to). |
| CLKIN | Clock input. CLKIN is the system clock input for the eTBC. Most operations of the eTBC are synchronous to CLKIN. Internally, the CLKIN signal is divided by a programmable divisor to generate TCK. |
| D7–D0 | Data inputs/outputs. D7–D0 form the 8-bit bidirectional data bus that interfaces the eTBC to its microprocessor/microcontroller host. Data in the eTBC registers is accessed (read or written) using this data bus. D7 is considered the most-significant bit, while D0 is considered the least-significant bit. |
| GND | Ground |
| RDY | Ready output. RDY is used to indicate to the microprocessor/microcontroller host whether or not the eTBC is ready to service the access (read or write) operation that is currently being requested. If RDY remains high following the initiation of an access cycle ($\overline{STRB}$ negative edge) then the eTBC is ready. Otherwise, if RDY goes low following the initiation of an access cycle ($\overline{STRB}$ negative edge) then the eTBC is not ready. In cases where the eTBC is not ready, subsequent processing in the eTBC may clear the not-ready state, which allows RDY to return high before the end of the access cycle. In any event, the RDY output returns high upon the termination of any access cycle ($\overline{STRB}$ positive edge). |
| $\overline{RST}$ | Reset input. $\overline{RST}$ is used to initiate asynchronous reset of the eTBC. Assertion (low) of $\overline{RST}$ places the eTBC in a reset state from which it does not exit until $\overline{RST}$ is released (high). While $\overline{RST}$ is low, the eTBC ignores host writes, the RDY, TDO, TMS, and $\overline{TRST}$ outputs are high, while TCK outputs CLKIN/16. An internal pullup forces $\overline{RST}$ to a high level if it has no external connection. |
| R/$\overline{W}$ | Read/write select. R/$\overline{W}$ is used by the microprocessor/microcontroller host to instruct the eTBC as to whether it is to perform read access (R/$\overline{W}$ high) or write access (R/$\overline{W}$ low). While R/$\overline{W}$ is high and $\overline{STRB}$ is low, the D7-D0 outputs are enabled to drive low and/or high logic levels onto the host data bus. Otherwise, while R/$\overline{W}$ is low, the D7–D0 outputs are disabled to a high-impedance state so that the host data bus can drive to the eTBC. |
| $\overline{STRB}$ | Read/write strobe. $\overline{STRB}$ is used by the microprocessor/microcontroller host to instruct the eTBC to initiate ($\overline{STRB}$ negative edge) or terminate/conclude ($\overline{STRB}$ positive edge) an access (read or write) operation. An internal pullup forces $\overline{STRB}$ to a high level if it has no external connection. |
| TCK | Test clock. TCK transmits the TCK signal required by the eTBC's IEEE Std 1149.1 target(s). All operations of the TAP are synchronous to TCK. Generally, the TCK signal is generated internally by the eTBC by division of CLKIN by a programmable divisor. Alternatively, when the eTBC is in its discrete-control mode, a rising edge of TCK is generated on a read to the discrete-control register, while a falling edge is generated on a write to the discrete-control register. |
| TDI | Test data input. TDI receives the TDI signal output by the eTBC's IEEE Std 1149.1 target(s). It is the serial input for shifting test data from the target(s); it is sampled on the rising edge of TCK and is expected to be transferred from the target(s) on the falling edge of TCK. An internal pullup forces TDI to a high level if it has no external connection. |
| TDO | Test data output. TDO transmits the TDO signal required by the eTBC's IEEE Std 1149.1 target(s). It is the serial output for shifting test data to the target(s); it is transferred on the falling edge of TCK and is to be sampled in the target on the rising edge of TCK. |
| TMS | Test mode select. TMS transmits the TMS signal required by the eTBC's IEEE Std 1149.1 target(s). It is the one control signal that directs the next TAP-controller state of the target(s). It is transferred from the eTBC on the falling edge of TCK and is to be sampled in the target(s) on the rising edge of TCK. |
| $\overline{TOE}$ | Test-output enable. $\overline{TOE}$ is the active-low output enable for the eTBC TAP outputs (TCK, TDO, TMS, $\overline{TRST}$). When $\overline{TOE}$ is inactive (high) the TAP outputs are disabled to a high-impedance state. Otherwise, when $\overline{TOE}$ is active (low), the TAP outputs are enabled to drive low and/or high logic levels according to other eTBC functions. An internal pullup forces $\overline{TOE}$ to a high level if it has no external connection. |
| $\overline{TRST}$ | Test reset. $\overline{TRST}$ transmits the $\overline{TRST}$ signal that may be required by some of the eTBC's IEEE Std 1149.1 target(s). A low signal at $\overline{TRST}$ is intended to initiate asynchronous test reset of the connected target(s). Such a low signal at $\overline{TRST}$ is generated only when the microprocessor/microcontroller host writes an appropriate value into the eTBC command register or, while the eTBC is in discrete-control mode, into the discrete-control register. |
| $V_{CC}$ | Supply voltage |

## application information

In application, the eTBC is used to master a single IEEE Std 1149.1 test access port (TAP) under the control of a microprocessor/microcontroller host. A typical implementation is shown in Figure 1.

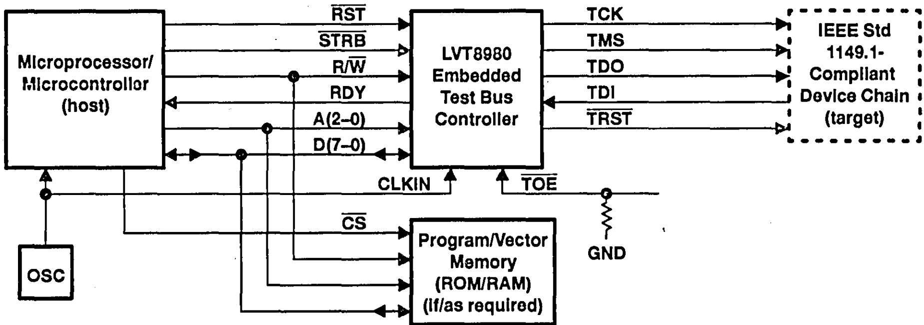


**Figure 1. eTBC Application**

All signals required to master IEEE Std 1149.1-compliant devices – TCK, TMS, TDO, TDI – are sourced/received by the eTBC. The eTBC can also source the optional TRST signal. Additionally, the eTBC implements high-drive output buffers, allowing it to interface directly to on- or off-board targets without need for buffering or other additional logic.

The eTBC's generic host interface allows it to act as a simple 8-bit memory- or I/O-mapped peripheral. As shown in Figure 1, for many choices of host microprocessor/microcontroller, this interface can be accomplished without additional logic. While the eTBC requires a clock input (CLKIN), in many cases it can be driven from the same source that provides a clock signal to the host.

Thus, in combination with the host microprocessor/microcontroller, the eTBC can be used to implement a two-chip embedded test-control function supporting board- and system-level built-in test based on structured IEEE Std 1149.1 test access. In some cases, for additional program and/or test vector storage, an external ROM/RAM may be required.

By use of the eTBC in such an embedded test control function, the host microprocessor/microcontroller is freed from the burden of generating the TAP-state sequences, serializing the outgoing bit stream, and de-serializing the incoming bit stream. All such tasks are implemented in the eTBC, allowing the host to operate at full 8-bit parallel efficiency, host software to operate at the level of discrete scan operations versus the level of TAP manipulation, and test throughput to be maximized. The eTBC's full suite of data-scan and instruction-scan commands ensure that the host software operates efficiently.

Host efficiency and flexibility is also maximized through the eTBC's fully visible status and implementation of the ready output (RDY). RDY goes inactive during a read or write access if the host-requested access cannot be performed immediately. Thus, it can be used to insert hold or wait states back to the host. When the condition blocking the access clears, the requested access completes. Additionally, all conditions that can cause such a blocking condition are continuously updated in the eTBC status and command registers. Thus, the host software can poll the eTBC status rather than implement RDY in hardware.

The eTBC also provides several capabilities that support special target application requirements. The eTBC's test-output enable allows its master function to be disabled so that another device (an external tester, for example) can control the target test access port. Where required, due to target non-compliance or sensitivity to state sequencing, discrete-control mode provides the host software with arbitrary control of TMS and TDO sequences. Also, where targets may be sensitive to leaving Shift-DR state during scan operation, gated-TCK mode allows the TCK output to be stopped, rather than cycling the target TAP state to Pause-DR state, when service to TDI buffer or TDO buffer is required.

## application information (continued)

Where target devices are extremely distant (due to cabling, etc.), pipelining may be implemented at intervals along the incoming or outgoing paths to retime (deskew) the TDI, TDO, and TMS signals. An example is shown in Figure 2. In such applications, the eTBC can automatically adjust the incoming test-data bit stream to account for cycle delays introduced by the pipeline.

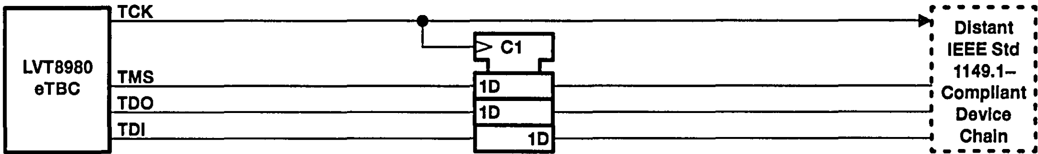


**Figure 2. Retimed Interface to Target**

Also, in gated-TCK mode, special scan commands provide transparent support for addressable shadow protocols. Thus, in conjunction with its high-drive outputs, the eTBC can fully support multidrop backplane TAP configurations implemented with TI's addressable scan ports (ASP). Figure 3 shows a multidrop TAP configuration in a passive-backplane application implemented with a centralized (one eTBC per chassis/rack) test-control architecture while Figure 4 shows a passive-backplane application implemented with a distributed (eTBC per module) test-control architecture. Figure 5 shows a multidrop TAP configuration in an active-backplane (motherboard) application.

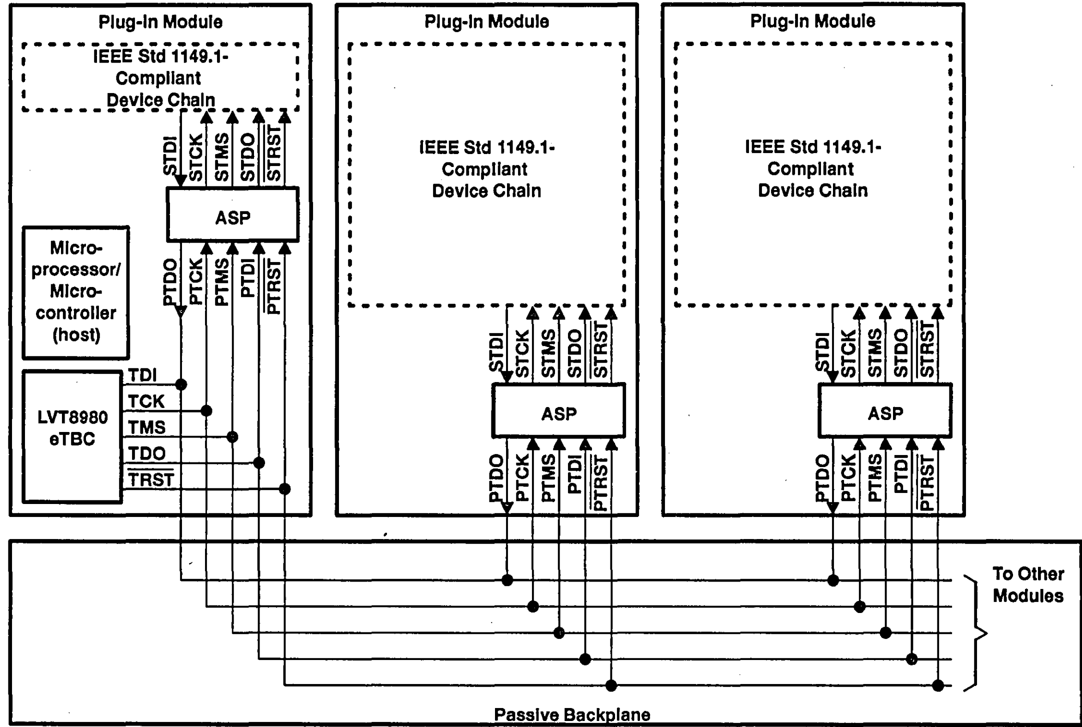


**Figure 3. Passive-Backplane Application with Centralized (eTBC per chassis) Test-Control Architecture**

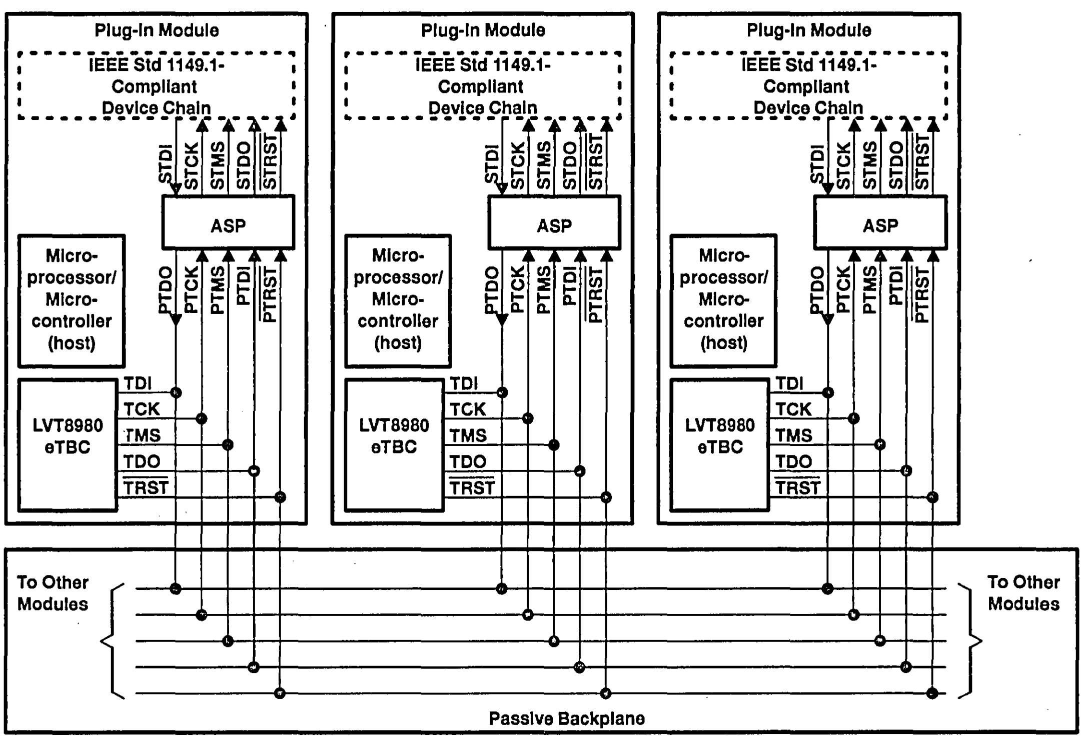


Figure 4. Passive-Backplane Application with Distributed Test-Control (eTBC per card) Architecture

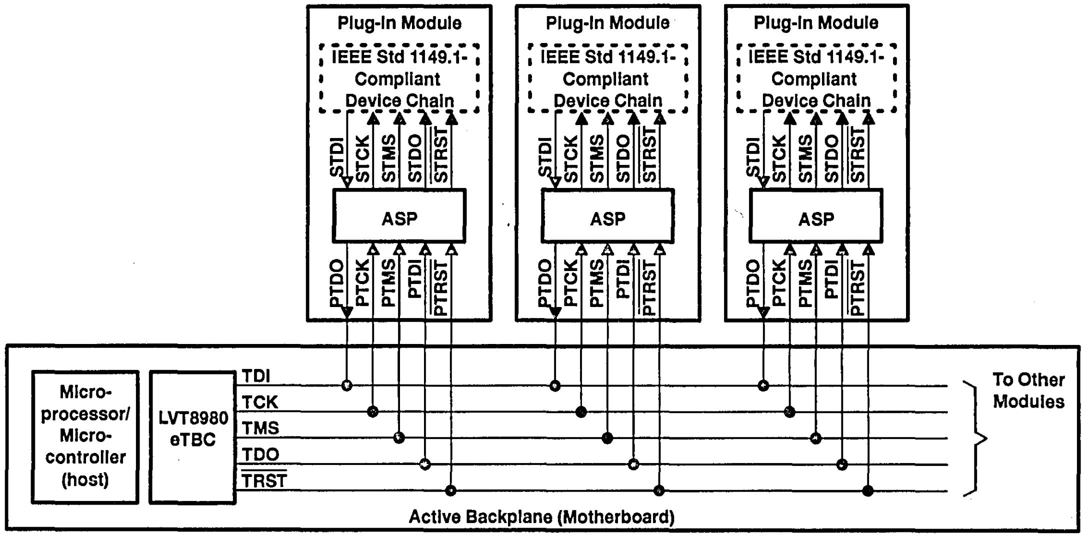


Figure 5. Active-Backplane (Motherboard) Application

### architecture

Conceptually, the eTBC can be viewed as an IEEE Std 1149.1 coprocessor/accelerator that operates in conjunction with (and under the control of) a host microprocessor/microcontroller. The eTBC implements this function using an 8-bit generic host interface and a scan-test-based command/control architecture. As shown in the functional block diagram, beyond these fundamental elements and another central block supporting discrete-control mode, the eTBC functions are accomplished in four additional blocks – one for each of the required TAP signals – a TCK generator, a TAP-state (TMS) generator, a TDO buffer, and a TDI buffer.

### host interface

The eTBC host interface is implemented generically on an 8-bit read/write data bus (D7–D0). Three address pins (A2–A0) directly index the eTBC's eight read/write registers: configurationA, configurationB, status, command, TDO-buffer, TDI-buffer, counter, and discrete-control. The register address map is given in Table 1.

### host access timing

Host access timing is asynchronous to the clock input (CLKIN) and is fully controlled by the read/write strobe ($\overline{STRB}$). The read/write select (R/$\overline{W}$) serves to control the direction of data flow on the bidirectional data bus. Figure 6 shows the read access timing while Figure 7 shows the write access timing. As shown, for either read or write access, R/$\overline{W}$ and address signals should be held while $\overline{STRB}$ is low.

For read access (R/$\overline{W}$ high) the eTBC data bus outputs are made active, on the falling edge of $\overline{STRB}$, to drive the data contained in the selected eTBC register. Otherwise, when $\overline{STRB}$ is high, the eTBC data outputs are at high impedance. Therefore, in many applications, the R/$\overline{W}$ signal can be shared in common with other host peripherals (ROM or RAM, for example) while the $\overline{STRB}$ signal is generated separately (by discrete chip-select signals available from the host or a decode logic) for each required peripheral.

For write access (R/$\overline{W}$ low), the eTBC data outputs remain at high impedance independent of $\overline{STRB}$. The address of the register to be written is latched from the address pins on the falling edge of $\overline{STRB}$ while the data to be written is latched from the data bus on the rising edge of $\overline{STRB}$.

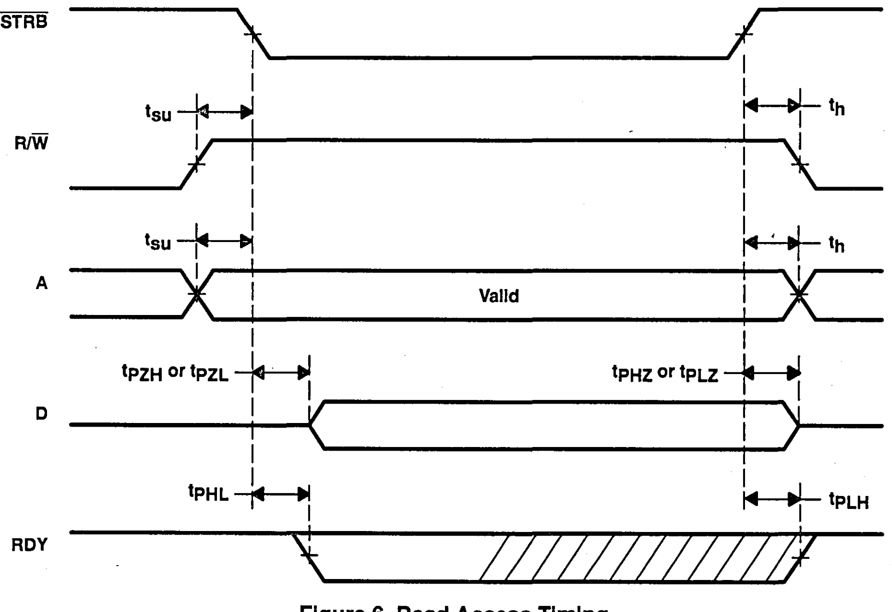


Figure 6. Read Access Timing

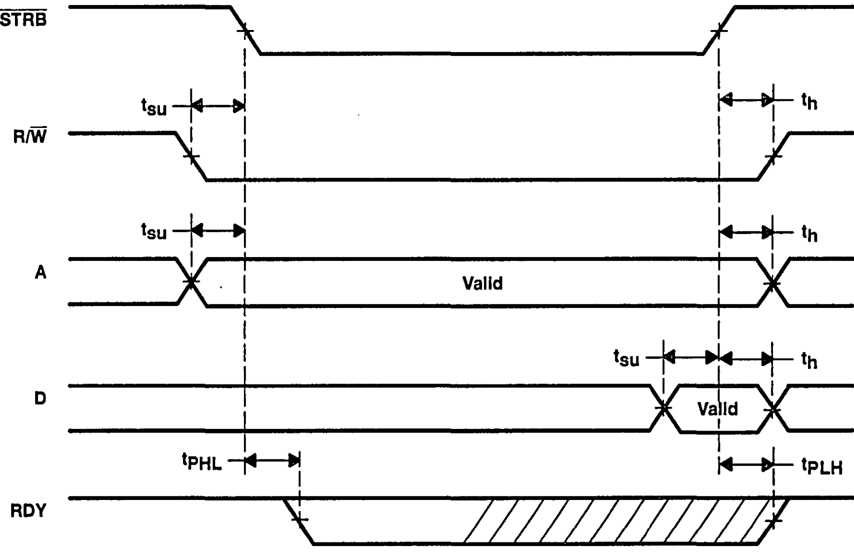


**Figure 7. Write Access Timing**

### ready output

The ready output (RDY) from the host interface can be used, where the selected microprocessor/microcontroller supports it, to insert wait or hold states back to the host. If a host-requested access cannot be performed immediately, RDY will go inactive (low) during that given access. When the condition blocking the access clears, RDY will go active (high) and the eTBC will grant the requested access. Alternatively, where such hardware-generated hold or wait states are not supported in the selected microprocessor/microcontroller host, the eTBC status and/or command registers can be polled to determine its readiness to grant a given read or write access.

Conditions that will cause a host access to be blocked (and RDY to become inactive) are limited to the following:

- While the TDI buffer is empty, as indicated in status register (bit 7, TDIS), a requested read to TDI-buffer register will generate RDY inactive; this condition will clear, RDY will go active, and the requested access will complete, when the TDI buffer is no longer empty.
- While the TDO buffer is full or is being reset upon initiation of a scan command, as indicated in status register (bit 6, TDOS), a requested write to TDO-buffer register will generate RDY inactive; this condition will clear, RDY will go active, and the requested access will complete, when the TDO buffer is no longer full or the TDO-buffer reset completes, as applicable.
- While a command is in progress, as indicated by a non-zero value in the opcode field (bits 3–0, OPCOD) of the command register, a requested write to command, configurationA, configurationB, or counter registers will generate RDY inactive. This condition will clear, RDY will go active, and the requested access will complete, when the previously specified command finishes. The sole exception is the writing of a logic 1 into the software reset (bit 7, SWRST) bit of the command register, which is never blocked.
- While a full-duplex scan command is in-progress, and the number of retiming-delay bits is other than zero, the number of writes to TDO-buffer register may not exceed, by more than 5, the number of reads to TDI-buffer register. A write to TDO-buffer register that does exceed this limit will be blocked, and will generate RDY inactive, indefinitely; the TDI-buffer register must be read before another write to TDO-buffer register.

## register descriptions

A summary of the eTBC registers, their address mappings, bit assignments, reset values, and host accessibility (read/write or read-only) is provided in Table 1. All registers are fully readable by the host. All registers are fully writeable by the host with the sole exception of the status register. Also, with the exception of TDO-buffer and command registers, writes to any register while a command is in progress will be held off (RDY inactive) or ignored. Bits designated as reserved should be written to logic 0; read-only bits designated as reserved will always read logic 0.

**Table 1. Register Summary**

| ADDRESS A2–A0 | REGISTER | REGISTER DETAIL (BIT ASSIGNMENTS) | | | | | | | | RESET VALUE | HOST ACCESS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) | | |
| 000 | ConfigurationA | Reserved | | NTOE | LPBK | | MODE | | | 0x00 | R/W |
| 001 | ConfigurationB | CDIV | | | Reserved | RDLY | | | | 0x80 | R/W |
| 010 | Status | TDIS | TDOS | CTRS | Reserved | TAPST | | | | 0x00 | R |
| 011 | Command | SWRST | NTRST | ENDST | | OPCOD | | | | 0x00 | R/W |
| 100 | TDO-buffer | | | | | | | | | 0x00 | R/W |
| 101 | TDI-buffer | | | | | | | | | 0x00 | R/W |
| 110 | Counter | | | | | | | | | 0x00 | R/W |
| 111 | Discrete-control | Reserved | | | | DNTR | DTMS | DTDO | DTDI | 0x00 | R/W |

## configuration registers

All eTBC test commands operate under the influence of the configurationA and configurationB registers. The decodes of the various bit groups assigned to these registers are given in Table 2 and Table 3, respectively. These registers are fully readable at all times and are fully writeable except when an eTBC command is in progress. Bit group values designated as reserved should not be written.

**Table 2. ConfigurationA Register Decode**

| CONFIGURATIONA BIT GROUP | CONFIGURATIONA BIT NO(S). | VALUE | RESULT |
|---|---|---|---|
| NTOE | 5 | 0 | TAP outputs (TCK, TDO, TMS, $\overline{TRST}$) are enabled. |
| | | 1 | TAP outputs (TCK, TDO, TMS, $\overline{TRST}$) are disabled (high impedance). |
| LPBK | 4–3 | 00 | No loopback – TDI pin inputs to TDI buffer. |
| | | 01 | TMS loopback – TAP-state generator inputs to TDI buffer. TMS and TDO pins are fixed high. |
| | | 10 | TDO loopback – TDO buffer inputs to TDI buffer. TMS and TDO pins are fixed high. |
| | | 11 | Reserved |
| MODE | 2–0 | 000 | Automatic/free-running-TCK mode – all TAP outputs are generated autonomously in the eTBC according to the active command. The TCK output runs continuously; while operating a scan command, if the TDI buffer becomes full and/or the TDO buffer becomes empty, the TAP state will be cycled to Pause-DR or Pause-IR, as appropriate, until the host performs the required buffer service. |
| | | 001 | Automatic/gated-TCK mode – all TAP outputs are generated autonomously in the eTBC according to the active command. The TCK output is run only when required to move TAP state or to progress run-test or scan operations, otherwise, it is gated off (low); while operating a scan command, if the TDI buffer becomes full and/or the TDO buffer becomes empty, the TAP state will remain in Shift-IR or Shift-DR, as appropriate, but the TCK output will be gated off until the host performs the required buffer service. |
| | | 010 | Discrete-control mode – all TAP outputs are determined by contents of the discrete-control register under control of host software. |
| | | 011–111 | Reserved |

**Table 3. ConfigurationB Register Decode**

| CONFIGURATIONB | | VALUE | RESULT |
|---|---|---|---|
| BIT GROUP | BIT NO(S). | | |
| CDIV | 7–5 | 000–111 | TCK = (CLKIN)/($2^{CDIV}$); reset value TCK = (CLKIN)/($2^4$) = CLKIN/16 |
| RDLY | 3–0 | 0000–1111 | Number of retiming delays to accommodate = RDLY; while operating a scan command, TDI sampling will be delayed by a number of TCK cycles, equal to RDLY, following the generation of Shift-DR or Shift-IR state, as appropriate. |

The negated test-output-enable (NTOE) bit is provided to allow the host to disable the TAP outputs via software in a manner analogous to the hardware $\overline{TOE}$. The loopback (LPBK) bit group allows the selection of the source of data to be input to the TDI buffer – from the TDI pin for normal eTBC operations or, for eTBC verification purpose, from TAP-state (TMS) generator or TDO buffer. The test mode (MODE) bit group provides for a choice of automatic/free-running-TCK, automatic/gated-TCK, or discrete-control modes.

The clock-divisor (CDIV) bit group allows software control of the TCK output frequency based on a division of the CLKIN input. Divisors from $2^0$ (1) to $2^7$ (128) are provided. The clock divisor defaults to $2^4$ (16) on eTBC reset (power-up, hardware-initiated, or software-initiated). The retiming-delay (RDLY) bit group provides for the automatic accommodation of retiming (pipeline) delays, which can be used to deskew the TAP signals to target scan chains that are electrically distant (due to cabling delays, etc).

### status register

The status of the eTBC is fully reported and continuously updated in the status register. The decode of the various bit groups assigned to the status register is given in Table 4.

**Table 4. Status Register Decode**

| STATUS | | VALUE | RESULT |
|---|---|---|---|
| BIT GROUP | BIT NO(S). | | |
| TDIS | 7 | 0 | The TDI buffer is empty – no TDI data is available for host read. |
| | | 1 | The TDI buffer is not empty – at least one byte of TDI data is available for host read. |
| TDOS | 6 | 0 | The TDO buffer is not full – at least one byte in TDO buffer is available for host write. |
| | | 1 | The TDO buffer is full – no bytes in TDO buffer are available for host write. |
| CTRS | 5 | 0 | The counter is not loaded with a complete 32-bit value – command operation cannot begin until counter load completes. |
| | | 1 | The counter is loaded with a complete 32-bit value – command operation can begin. |
| TAPST | 3–0 | 0000 | The current target TAP state (as sent by eTBC) is Test-Logic-Reset. |
| | | 0001 | The current target TAP state (as sent by eTBC) is Select-DR-Scan. |
| | | 0010 | The current target TAP state (as sent by eTBC) is Capture-DR. |
| | | 0011 | The current target TAP state (as sent by eTBC) is Shift-DR. |
| | | 0100 | The current target TAP state (as sent by eTBC) is Exit1-DR. |
| | | 0101 | The current target TAP state (as sent by eTBC) is Pause-DR. |
| | | 0110 | The current target TAP state (as sent by eTBC) is Exit2-DR. |
| | | 0111 | The current target TAP state (as sent by eTBC) is Update-DR. |
| | | 1000 | The current target TAP state (as sent by eTBC) is Run-Test/Idle. |
| | | 1001 | The current target TAP state (as sent by eTBC) is Select-IR-Scan. |
| | | 1010 | The current target TAP state (as sent by eTBC) is Capture-IR. |
| | | 1011 | The current target TAP state (as sent by eTBC) is Shift-IR |
| | | 1100 | The current target TAP state (as sent by eTBC) is Exit1-IR. |
| | | 1101 | The current target TAP state (as sent by eTBC) is Pause-IR. |
| | | 1110 | The current target TAP state (as sent by eTBC) is Exit2-IR. |
| | | 1111 | The current target TAP state (as sent by eTBC) is Update-IR. |

The TDI-buffer-status (TDIS) bit reports the readiness of the TDI buffer to respond to a host read. The TDO-buffer-status (TDOS) bit reports the readiness of the TDO buffer to respond to a host write. The counter-status (CTRS) bit reports the readiness of the counter to support a command which uses the counter. The current-TAP-state (TAPST) bit group continuously reports the target TAP state as monitored by the eTBC.

### command register

The command register is used to perform software reset of the eTBC, to discretely control the state of the TRST output when not in discrete-control mode, and to initiate test operations in the target(s).The decode of the various bits assigned to the command register is given in Table 5.

Any read to the command register while a command is in progress will return the value written to the command register upon initiation of the command. Once a command finishes, the operation-code (OPCOD) bit group in the command register will be reset to null. In this way, the status of a requested command can be monitored/polled by the host.

With the exception of the software-reset (SWRST) bit, which can be written at any time, writes to the command register while a command is in progress will cause RDY inactive and will be ignored if the write cycle is terminated before the previously requested command finishes.

**Table 5. Command Register Decode**

| COMMAND | | VALUE | RESULT | TEST OPERATION COMMENTS | | | |
|---|---|---|---|---|---|---|---|
| BIT GROUP | BIT NO(S). | | | WORKING TAP STATE | USES COUNTER | USES TDI BUFFER | USES TDO BUFFER |
| SWRST | 7 | 0 | Normal operation | | | | |
| | | 1 | Full reset | | | | |
| NTRST | 6 | 0 | If not in discrete-control mode, output low to $\overline{\text{TRST}}$ pin. | | | | |
| | | 1 | If not in discrete-control mode, output high to $\overline{\text{TRST}}$ pin. | | | | |
| ENDST | 5–4 | 00 | Finish command in TAP state Test-Logic-Reset. | | | | |
| | | 01 | Finish command in TAP state Run-Test/Idle. | | | | |
| | | 10 | Finish command in TAP state Pause-DR. | | | | |
| | | 11 | Finish command in TAP state Pause-IR. | | | | |
| OPCOD | 3–0 | 0000 | Null | | | | |
| | | 0001 | Reserved | | | | |
| | | 0010 | Execute run test. | Run-Test/Idle | Yes | No | No |
| | | 0011 | Execute input-only ASP scan. | N/A | Yes | Yes | No |
| | | 0100 | Execute ASP scan. | N/A | Yes | Yes | Yes |
| | | 0101 | Execute output-only ASP scan. | N/A | Yes | No | Yes |
| | | 0110 | Execute state move. | N/A | No | No | No |
| | | 0111 | Execute state jump. | N/A | No | No | No |
| | | 1000 | Execute instruction-register scan. | Shift-IR | Yes | Yes | Yes |
| | | 1001 | Execute data-register scan. | Shift-DR | Yes | Yes | Yes |
| | | 1010 | Execute input-only instruction-register scan. | Shift-IR | Yes | Yes | No |
| | | 1011 | Execute input-only data-register scan. | Shift-DR | Yes | Yes | No |
| | | 1100 | Execute output-only instruction-register scan. | Shift-IR | Yes | No | Yes |
| | | 1101 | Execute output-only data-register scan. | Shift-DR | Yes | No | Yes |
| | | 1110 | Execute recirculate instruction-register scan. | Shift-IR | Yes | Yes | No |
| | | 1111 | Execute recirculate data-register scan. | Shift-DR | Yes | Yes | No |

The software-reset (SWRST) bit is provided to allow software initiation of full eTBC reset. This bit of the command register can be written at any time regardless of configuration or command in progress. The negated-test-reset (NTRST) bit allows direct software control of the state of $\overline{\text{TRST}}$ output in modes other than discrete-control.

The end-TAP-state (ENDST) bit group determines the TAP state in which the target scan chain will be left when the requested command finishes. The operation-code (OPCOD) bit group determines the test operation to be executed in the target.

### counter register

The counter register, while only 8-bits wide like any other eTBC register, provides read/write access to the full 32-bit eTBC counter. Writes or reads to the counter register should be accomplished by holding the eTBC address pins throughout four complete host access cycles, otherwise the counter will be considered unloaded and the four-cycle access must be restarted. The counter access (both read and write) is in least-significant-byte-first order. Any writes to the counter register while a command is in progress will be ignored. The 32-bit value loaded in the counter at initiation of a command is used to determine the number of TCK cycles or scan bits for which the command will be operated.

### TDO-buffer register

The TDO-buffer register, while only 8-bits wide like any other eTBC register, provides write access to the full 4 × 8 (32-bit) FIFO that comprises the TDO buffer. The TDO-buffer register can be written as long as the TDO buffer does not become full. When the TDO buffer becomes full, further writes to the TDO-buffer register cause RDY inactive (and consequent hold or wait states to be sent back to the host, if supported) and cause the write to be ignored if the write cycle is terminated before the TDO-buffer-full status is cleared.

### TDI-buffer register

The TDI-buffer register, while only 8-bits wide like any other eTBC register, provides read access to the full 4 × 8 (32-bit) FIFO that comprises the TDI buffer. The TDI-buffer register can be read as long as the TDI buffer does not become empty. When the TDI buffer becomes empty, further reads to the TDI-buffer register cause RDY inactive (and consequent hold or wait states to be sent back to the host, if supported) and cause the read data to be invalid if the read cycle is terminated before the TDI-buffer-empty status is cleared.

### discrete-control register

The discrete-control register is used to program the state of the TAP outputs (TCK, TDO, TMS, $\overline{\text{TRST}}$) and to poll the state of the TAP input (TDI) when the eTBC is in its discrete-control mode. The contents of the discrete-control register determine values output to the TDO, TMS, and TRST according to the decode in Table 6. The TCK output is generated on each read and write to the discrete-control register; writes generate TCK falling edge, while reads generate TCK rising edge. In modes other than the discrete-control mode, this register is fully writeable and readable, but writes and reads have no effect on eTBC or target operation.

**Table 6. Discrete-Control Register Decode**

| DISCRETE-CONTROL | | VALUE | RESULT |
|---|---|---|---|
| BIT GROUP | BIT NO(S). | | |
| DNTR | 3 | 0 | If in discrete-control mode, output low to $\overline{\text{TRST}}$ pin, otherwise nothing. |
| | | 1 | If in discrete-control mode, output high to $\overline{\text{TRST}}$ pin, otherwise nothing. |
| DTMS | 2 | 0 | If in discrete-control mode, output low to TMS pin, otherwise nothing. |
| | | 1 | If in discrete-control mode, output high to TMS pin, otherwise nothing. |
| DTDI | 1 | 0 | The TDI data received is a logic 0. |
| | | 1 | The TDI data received is a logic 1. |
| DTDO | 0 | 0 | If in discrete-control mode, output low to TDO pin, otherwise nothing. |
| | | 1 | If in discrete-control mode, output high to TDO pin, otherwise nothing. |

### command/control

The eTBC's command-based architecture is structured around a set of comprehensive IEEE Std 1149.1 (JTAG) test objectives, which include TAP state movement, scan operations, and run test (operation of test logic in Run-Test/Idle state). The set of test operations, as decoded from the command register (bits 3–0, OPCOD) is given in Table 5. Commands are initiated by writing the eTBC command register; upon command initiation, the test-control logic is initialized and the TDO and TDI buffers are cleared. Command completion is indicated when the operation code (OPCOD) field of the command register returns to the value of the null command.

The eTBC command operation is modified by the configurationA, and configurationB registers, which should be written prior to writing of the command register as the values in these registers cannot be modified while a command is in progress. Also, commands are only operated in automatic test modes as specified in the configurationA register (bits 2–0, MODE) – while in discrete-control mode, commands are ignored.

All eTBC commands operate similarly to accomplish IEEE Std 1149.1 test objectives. First, the eTBC generates a TMS sequence to move the target scan chain from its current TAP state to a working state that depends on the test objective. Second, the command is operated (test run, bits scanned) in the working state for a number of TCK cycles (or scan bits) determined by the value of the counter upon command initiation. Third, the eTBC generates a TMS sequence to move the target scan chain from the working state to the end state specified in the command register (bits 5–4, ENDST). For some commands, one or more of these steps are omitted.

#### TAP-state-movement commands

Two eTBC commands are provided to accomplish TAP state movement. The state-move command operates to generate a TMS sequence to move the target scan chain directly from its current TAP state to the end state specified in the command register. The state-jump command operates to move the eTBC's stored value of the target TAP state without generating any changes to the TMS output. The state-jump command can therefore be used to switch between targets that share the same test bus, such as those in a multidrop backplane configuration implemented with TI addressable scan ports, but that may be left in different TAP states.

#### run-test command

The run-test command is provided to allow the test logic of the target scan chain to execute autonomously in the Run-Test/Idle TAP state. Such test logic is commonly used to implement chip- or board-level built-in self test. The run-test command operates by generating TMS sequences to move the target scan chain from its current TAP state to the Run-Test/Idle TAP state where it will remain for a number of TCK cycles determined by the value of the counter upon command initiation. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

#### scan commands

Eleven eTBC commands are provided to perform scan operations to target scan chains. These can be classified by the destination of scan data in the target – addressable scan port (ASP), IEEE Std 1149.1 instruction register, or IEEE Std 1149.1 data register – and by the nature/direction of the data transfer – full-duplex (default), input-only, output-only, or recirculate. The only combination of these two factors that is not implemented is recirculate ASP scan.

#### addressable scan port (ASP) scan commands

The ASP scan commands operate to scan data to and/or from an addressable scan port target. Since ASP devices require that TMS remain fixed throughout their select and acknowledge protocols, the eTBC does not generate TMS sequences or change its stored value of the target's TAP state. Also, for the same reason, ASP scan commands that target ASP devices should be operated in gated-TCK mode. The ASP scan commands do allow data written to the TDO buffer to be driven serially onto the TDO pin and bits received serially at the TDI pin to be stored into the TDI buffer for reading by the host. However, the ASP scan commands do not perform any bit-pair encoding of ASP select protocols or decoding of ASP acknowledge protocols. Such encoding/decoding must be performed in the host. The number of data bits to be transferred in and/or out is determined by the value of the counter upon command initiation.

### instruction-register scan commands

The instruction-register scan commands operate to scan bits to and/or from the concatenation of instruction registers in a target scan chain. The eTBC generates a TMS sequence to move the target scan chain from its current TAP state to the Shift-IR TAP state. Data written to the TDO buffer can be driven serially onto the TDO pin and bits received serially at the TDI pin can be stored into the TDI buffer for reading by the host. The number of data bits to be transferred in and/or out is determined by the value of the counter upon command initiation. If during the operation of an instruction register scan command, the TDO buffer becomes empty, or the TDI buffer becomes full, the TAP state will be sequenced to Pause-IR (if in free-running-TCK mode) or the TCK output will be gated off (if in gated-TCK mode) until the required buffer service is performed. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

### data-register scan commands

The data-register scan commands operate to scan bits to and/or from the concatenation of data registers in a target scan chain. The eTBC generates a TMS sequence to move the target scan chain from its current TAP state to the Shift-DR TAP state. Data written to the TDO buffer may be driven serially onto the TDO pin and bits received serially at the TDI pin may be stored into the TDI buffer for reading by the host. The number of data bits to be transferred in and/or out is determined by the value of the counter upon command initiation. If during the operation of a data-register scan command, the TDO buffer becomes empty, or the TDI buffer becomes full, the TAP state will be sequenced to Pause-DR (if in free-running-TCK mode) or the TCK output will be gated off (if in gated-TCK mode) until the required buffer service is performed. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

### other scan-command variations

As noted before, the nature/direction of the data transfer for any scan command can vary along with the destination of scan data in the target, as follows:

- For scan commands of the full-duplex (default) class, both TDO buffer and TDI buffer are used to scan data to and from the target scan chain, respectively.
- For scan commands of the input-only class, only the TDI buffer is used to scan data from the target scan chain; outgoing TDO data is fixed at a high level throughout the scan operation.
- For scan commands of the output-only class, only the TDO buffer is used to scan data to the target scan chain; incoming TDI data is simply ignored.
- For scan commands of the recirculate class, only the TDI buffer is used to scan data from the target scan chain; outgoing TDO data is generated by recirculating the incoming TDI data back into the target scan chain.

### counter

As described above, the value loaded in the eTBC's 32-bit counter at initiation of a command is used to specify the number of TCK cycles or scan bits to remain in the command's working state. As each TCK cycle or scan bit is processed for a run-test or scan command, respectively, the counter value is decremented. When the counter value reaches zero, the command leaves its working state to finish in the end state specified in the command register.

Before a command that uses the counter can be initiated, a full 32-bit value should be loaded by four consecutive writes to the counter register. As well, the full 32-bit current value of the counter can be observed by four consecutive reads to the counter register. The counter status (unloaded/loaded) is maintained and observable in the status register (bit 5, CTRS).

Upon eTBC reset (power-up, hardware-initiated, or software-initiated), the counter is cleared and assumes its unloaded state.

## TCK generator

The TCK generator sources the test clock (TCK) signal required by the IEEE Std 1149.1 target(s) and the eTBC-internal test-control logic. The fundamental TCK frequency is produced by division of CLKIN. The divisor to be used is programmable within a range of 1 to 128 in the configurationB register (bits 7–5, CDIV). The TCK output to the target(s) can be operated in free-running or gated modes. The free-running mode toggles TCK continuously, based on CLKIN, while the gated mode operates the TCK only when required to move the target TAP state or to perform a run-test or scan operation.

While the eTBC is in discrete-control mode, the TCK generator is not used; instead, the state of TCK is toggled on each alternating read and write to the discrete-control register. A falling edge of TCK is produced by write, while a rising edge of TCK is produced by read.

Upon eTBC reset (power-up, hardware-initiated, or software-initiated), the TCK generator assumes its free-running mode with a clock divisor of 16 (TCK = CLKIN/16).

## TAP-state generator

The TAP-state generator sources the TMS signal, which sequences the TAP controllers of connected IEEE Std 1149.1-compliant target devices. The TAP controller specified by IEEE Std 1149.1 is a synchronous finite-state machine that provides test control signals throughout each target device; its state diagram is shown in Figure 8. This diagram and the TAP-controller states are discussed subsequently.

The TAP-state generator operates under the control of an executing command to generate the TMS sequences required to move connected target devices from one stable state to another, to capture and scan test data into/out of target devices, and to operate built-in test modes of target devices in the Run-Test/Idle state.

The TAP state currently being generated is always maintained by the TAP-state generator and is constantly available in the eTBC status register (bits 3–0, TAPST) for host read. Based on the TAP state that is current upon command initiation, the TAP-state generator will source a defined sequence of TMS values to reach the TAP state in which the command is progressed (e.g., Shift-IR, Shift-DR, Run-Test/Idle), and ultimately to reach the specified end TAP state. These sequences are detailed in Tables 7–12.

While the eTBC is in free-running-TCK mode, if a currently operating scan command empties or fills a required test data buffer, then the TAP-state generator will source the TMS sequences required to move the connected target devices to their Pause-IR or Pause-DR states. In such case, the TAP-state generator will maintain target devices in their Pause-IR or Pause-DR states until the required test data buffer is serviced appropriately. On the other hand, if such a buffer condition occurs while the eTBC is in gated-TCK mode, the TAP-state generator maintains the target devices in their Shift-IR or Shift-DR states while the TCK is gated off.

While the eTBC is in discrete-control mode, the TAP-state generator is not used; instead, the state of the TMS pin is determined by the contents of the discrete-control register. Thus, TMS sequences that cannot be generated automatically can still be applied through the eTBC to targets that require such (e.g., near-compliant devices).

The TAP-state generator also is not used during the operation of the special addressable shadow protocol (ASP) scan commands. Since, by definition, ASPs operate only while the TAP is idling (maintaining one of the TAP states Test-Logic-Reset, Run-Test/Idle, Pause-IR, or Pause-DR), the TMS pin must be maintained at the value it held upon initiation of the ASP scan command.

For eTBC verification/debugging, in addition to continuous update of the current target TAP state in the eTBC status register, the output of the TAP-state (TMS) generator can be selected for loopback into the TDI buffer. When this TMS-loopback mode is selected, although a host-requested command will execute in the eTBC, the target will not be affected as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power-up, hardware-initiated, or software-initiated), the TAP-state generator assumes the Test-Logic-Reset TAP state.

**Table 7. TMS Sequencing from TAP State Test-Logic-Reset**

| FROM TEST-LOGIC-RESET (TMS = H) TO | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TEST-LOGIC-RESET | | RUN-TEST-IDLE | | SHIFT-DR | | PAUSE-DR | | SHIFT-IR | | PAUSE-IR | |
| NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE |
| H | T-L-R | L | R-T/I | L | R-T/I | L | R-T/I | L | R-T/I | L | R-T/I |
| | | | | H | S-DR-S | H | S-DR-S | H | S-DR-S | H | S-DR-S |
| | | | | L | Capture-DR | L | Capture-DR | H | S-IR-S | H | S-IR-S |
| | | | | L | Shift-DR | H | Exit1-DR | L | Capture-IR | L | Capture-IR |
| | | | | | | L | Pause-DR | L | Shift-IR | H | Exit1-IR |
| | | | | | | | | | | L | Pause-IR |

**Table 8. TMS Sequencing from TAP State Run-Test/Idle**

| FROM RUN-TEST/IDLE (TMS = L) TO | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TEST-LOGIC-RESET | | RUN-TEST-IDLE | | SHIFT-DR | | PAUSE-DR | | SHIFT-IR | | PAUSE-IR | |
| NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE |
| H | S-DR-S | L | R-T/I | H | S-DR-S | H | S-DR-S | H | S-DR-S | H | S-DR-S |
| H | S-IR-S | | | L | Capture-DR | L | Capture-DR | H | S-IR-S | H | S-IR-S |
| H | T-L-R | | | L | Shift-DR | H | Exit1-DR | L | Capture-IR | L | Capture-IR |
| | | | | | | L | Pause-DR | L | Shift-IR | H | Exit1-IR |
| | | | | | | | | | | L | Pause-IR |

**Table 9. TMS Sequencing from TAP State Pause-DR**

| FROM PAUSE-DR (TMS = L) TO | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TEST-LOGIC-RESET | | RUN-TEST-IDLE | | SHIFT-DR | | PAUSE-DR | | SHIFT-IR | | PAUSE-IR | |
| NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE |
| H | Exit2-DR | H | Exit2-DR | H | Exit2-DR | H | Exit2-DR | H | Exit2-DR | H | Exit2-DR |
| H | Update-DR | H | Update-DR | L | Shift-DR | H | Update-DR | H | Update-DR | H | Update-DR |
| H | S-DR-S | L | R-T/I | | | H | S-DR-S | H | S-DR-S | H | S-DR-S |
| H | S-IR-S | | | | | L | Capture-DR | H | S-IR-S | H | S-IR-S |
| H | T-L-R | | | | | H | Exit1-DR | L | Capture-IR | L | Capture-IR |
| | | | | | | L | Pause-DR | L | Shift-IR | H | Exit1-IR |
| | | | | | | | | | | L | Pause-IR |

### Table 10. TMS Sequencing from TAP State Pause-IR

| FROM PAUSE-IR (TMS = L) TO | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TEST-LOGIC-RESET | | RUN-TEST-IDLE | | SHIFT-DR | | PAUSE-DR | | SHIFT-IR | | PAUSE-IR | |
| NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE |
| H | Exit2-IR | H | Exit2-IR | H | Exit2-IR | H | Exit2-IR | H | Exit2-IR | H | Exit2-IR |
| H | Update-IR | H | Update-IR | H | Update-IR | H | Update-IR | L | Shift-IR | H | Update-IR |
| H | S-DR-S | L | R-T/I | H | S-DR-S | H | S-DR-S | | | H | S-DR-S |
| H | S-IR-S | | | L | Capture-DR | L | Capture-DR | | | H | S-IR-S |
| H | T-L-R | | | L | Shift-DR | H | Exit1-DR | | | L | Capture-IR |
| | | | | | | L | Pause-DR | | | H | Exit1-IR |
| | | | | | | | | | | L | Pause-IR |

### Table 11. TMS Sequencing from TAP State Shift-DR

| FROM SHIFT-DR (TMS = L) TO | | | | | | | |
|---|---|---|---|---|---|---|---|
| TEST-LOGIC-RESET | | RUN-TEST-IDLE | | PAUSE-DR | | PAUSE-IR | |
| NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE |
| H | Exit1-DR | H | Exit1-DR | H | Exit1-DR | H | Exit1-DR |
| H | Update-DR | H | Update-DR | L | Pause-DR | H | Update-DR |
| H | S-DR-S | L | R-T/I | | | H | S-DR-S |
| H | S-IR-S | | | | | H | S-IR-S |
| H | T-L-R | | | | | L | Capture-IR |
| | | | | | | H | Exit1-IR |
| | | | | | | L | Pause-IR |

### Table 12. TMS Sequencing from TAP State Shift-IR

| FROM SHIFT-IR (TMS = L) TO | | | | | | | |
|---|---|---|---|---|---|---|---|
| TEST-LOGIC-RESET | | RUN-TEST-IDLE | | PAUSE-DR | | PAUSE-IR | |
| NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE | NEXT TMS | NEXT TAP STATE |
| H | Exit1-IR | H | Exit1-IR | H | Exit1-IR | H | Exit1-IR |
| H | Update-IR | H | Update-IR | H | Update-IR | L | Pause-IR |
| H | S-DR-S | L | R-T/I | H | S-DR-S | | |
| H | S-IR-S | | | L | Capture-DR | | |
| H | T-L-R | | | H | Exit1-DR | | |
| | | | | L | Pause-DR | | |

### state diagram description

The state diagram shown in Figure 8 is in accordance with IEEE Standard 1149.1–1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at any given time.

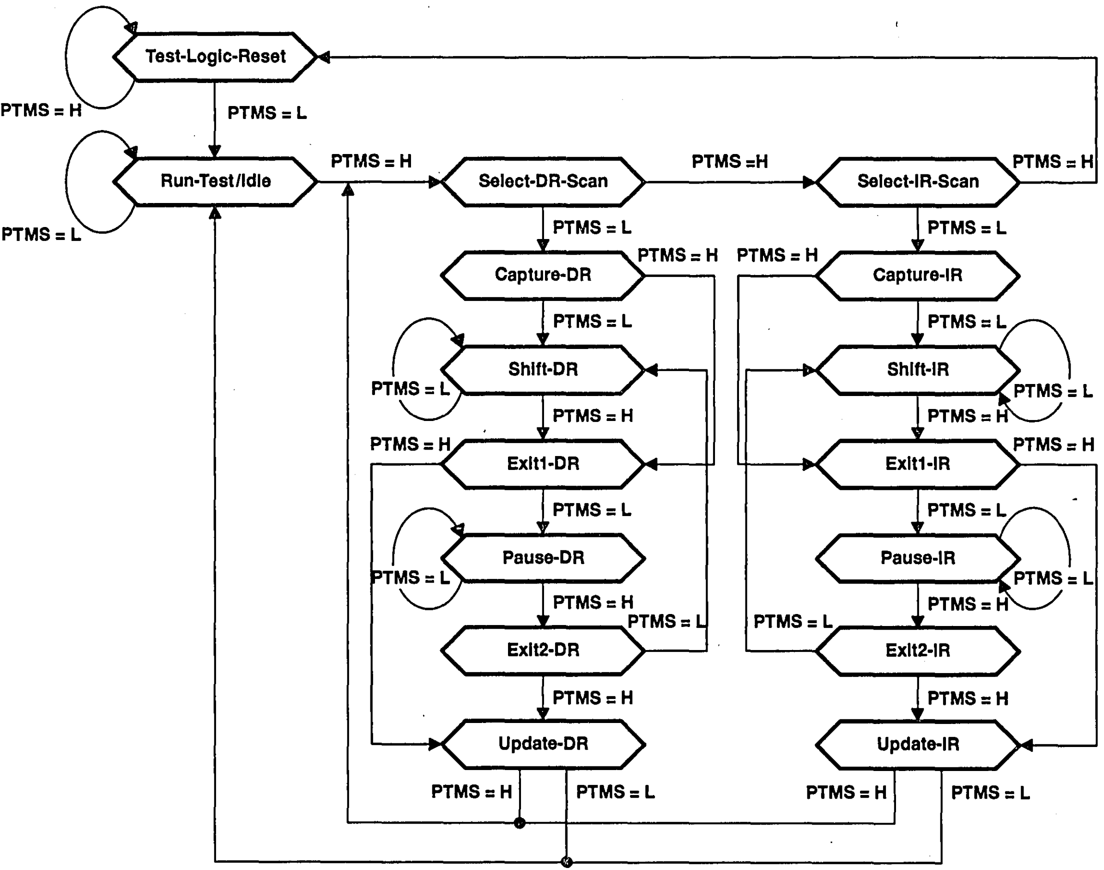


Figure 8. TAP-Controller State Diagram


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### Test-Logic-Reset

The eTBC TAP-state generator powers up in the Test-Logic-Reset state. Alternatively, the eTBC can be forced to this state asynchronously by assertion of its $\overline{RST}$ input or synchronously by writing the eTBC command register (bit 7-SWRST).

For a target device in the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

### Run-Test/Idle

For a target device, Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

### Select-DR-Scan, Select-IR-Scan

For a target device, no specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

For a target device in the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the Capture-DR state is exited.

### Shift-DR

For a target device, upon entry to the Shift-DR state, the selected data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the selected data register. While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle.

### Exit1-DR, Exit2-DR

For a target device, the Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

For target devices, no specific function is performed in the stable Pause-DR state. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

For a target device, if the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK following entry to the Update-DR state.

### Capture-IR

For a target device in the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the Capture-IR state is exited.

### Shift-IR

For a target device, upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the instruction register. While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle.

### Exit1-IR, Exit2-IR

For target devices, the Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

For target devices, no specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

For target devices, the current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## TDO buffer

The TDO buffer is the 4 × 8-bit-parallel-to-serial FIFO that accepts scan data from the host in 8-bit-parallel format and serializes it onto the TDO pin during scan operations. Scan data is expected to be transferred from the host in least-significant-byte-first order to meet IEEE Std 1149.1 requirements for least-significant-bit-first scan order. Any partial byte to be written should be justified to D0. The TDO buffer is cleared upon command initiation, so no scan data should be written to the TDO buffer before writing a scan command to the command register.

The TDO-buffer status (not full/full) is maintained in the status register (bit 6, TDOS). When the TDO-buffer status is full, writes to the TDO buffer will be held off by RDY inactive and if the write cycle is aborted prior to RDY active, the write data will be ignored.

For the convenience and efficiency of operating scans to the target for which outgoing data is not required, the eTBC supports special classes of input-only and recirculate scan commands which do not require nor operate the TDO buffer and so the host need not perform any write access to it. While the input-only scan commands are operating, the TDO pin outputs a fixed high level. While the recirculate scan commands are operating, the TDO pin recirculates to the target the data that is received at TDI.

While the eTBC is in discrete-control mode, the TDO buffer is not used; instead, the state of the TDO pin is determined by the contents of the discrete-control register. Thus, TMS/TDO sequences that cannot be automatically generated can still be applied through the eTBC to targets that require such (e.g., near-compliant devices).

For eTBC verification/debugging, the TDO-buffer output can be selected for loopback into the TDI buffer. When this TDO-loopback mode is selected, although a host-requested command will execute in the eTBC, the target will not be affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power-up, hardware-initiated, or software-initiated), the TDO buffer is cleared and assumes its not-full state.

### TDI buffer

The TDI buffer is the serial-to-4 × 8-bit-parallel FIFO that serially receives data at the TDI pin and makes it available in 8-bit-parallel format for reading by the host. Scan data is expected to be transferred from the IEEE Std 1149.1 targets in least-significant-bit-first order and is made available for host read in least-significant-byte-first order. The last data available for host read during a scan command may be a partial byte, in which case it will be justified to D0.

The TDI-buffer status (empty/not empty) is maintained in the status register (bit 7, TDIS). When the TDI-buffer status is empty, reads to the TDI buffer will be held off by RDY inactive and, if the read cycle is aborted prior to RDY active, the read data will be invalid.

The TDI buffer is able to automatically accommodate retiming (pipeline) delays to the target. While operating a scan command, TDI sampling will be delayed by a number of TCK cycles, equal to a value given in the configurationB register (bits 3–0, RDLY), following the generation of Shift-DR or Shift-IR state, as appropriate.

For the convenience and efficiency of operating scans to the target for which incoming data is not required, the eTBC supports a special class of output-only scan commands that neither require nor operate the TDI buffer. While the output-only scan commands are operating, the data received at TDI is ignored and the host need not perform any read access to the TDI buffer.

While the eTBC is in discrete-control mode, the TDI buffer is not used; instead, the state of the TDO pin is observed in the discrete-control register. Thus, TMS/TDO sequences that cannot be automatically generated can still be applied through the eTBC to targets that require such (e.g., near-compliant devices).

For eTBC verification/debugging, the input to the TDI buffer can be selected for loopback from either TDO buffer or TAP-state (TMS) generator. When either of these loopback modes is selected, although a host-requested command will execute in the eTBC, the target will not be affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power-up, hardware-initiated, or software-initiated), the TDI buffer is cleared and assumes its empty state.

### discrete control

The discrete-control block provides the multiplexing and control logic required to support the eTBC's discrete-control mode in addition to its automatic modes. While the eTBC is in discrete-control mode, the TAP signals are fully controllable/accessible to the host via reads/writes to the discrete-control register. No commands can be initiated/operated while the eTBC is in discrete-control mode.

Upon eTBC reset (power-up, hardware-initiated, or software-initiated), the discrete-control mode is inactive.

### reset

The eTBC provides three mechanisms for comprehensive and equivalent reset – power-up reset, hardware-initiated reset ($\overline{RST}$), and software-initiated reset (SWRST, bit 7 of command register) to the following effect:

- All eTBC registers are reset to default values as given in Table 1.
- The command/control logic is fully reset.
- The counter is cleared/unloaded. The TDO buffer and TDI buffer are cleared/emptied.
- The TAP-state generator is reset to the Test-Logic-Reset TAP state.
- TDO, TMS, and TRST output high levels; TCK outputs CLKIN/16.

As a consequence, the IEEE Std 1149.1 targets can be expected to be driven synchronously to the Test-Logic-Reset state no later than the fifth rising edge of TCK (72 CLKIN cycles).

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .......... –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .......... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state,
$V_O$ (see Note 1): D, RDY .......... –0.5 V to $V_{CC}$ + 0.5 V
TCK, TDO, TMS, $\overline{TRST}$ .......... –0.5 V to 7 V
Current into any output in the low state, $I_O$: SN54LVT8980 (D, RDY) .......... 12 mA
SN54LVT8980 (TCK, TDO, TMS, $\overline{TRST}$) .......... 96 mA
SN74LVT8980 (D, RDY) .......... 12 mA
SN74LVT8980 (TCK, TDO, TMS, $\overline{TRST}$) .......... 128 mA
Current into any output in the high state,
$I_O$ (see Note 2): SN54LVT8980 (D, RDY) .......... 16 mA
SN54LVT8980 (TCK, TDO, TMS, $\overline{TRST}$) .......... 48 mA
SN74LVT8980 (D, RDY) .......... 16 mA
SN74LVT8980 (TCK, TDO, TMS, $\overline{TRST}$) .......... 64 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) .......... –50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) .......... –50 mA
Output clamp current, $I_{OK}$ ($V_O > V_{CC}$): D, RDY .......... 50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): DW package .......... 1.7 W
Storage temperature range, $T_{stg}$ .......... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions (see Note 4)

| | | | SN54LVT8980 | | SN74LVT8980 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | D, RDY | | –8 | | –8 | mA |
| | | TCK, TDO, TMS, $\overline{TRST}$ | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | D, RDY | | 6 | | 6 | mA |
| | | TCK, TDO, TMS, $\overline{TRST}$ | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 200 | | 200 | | µs/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

PRODUCT PREVIEW

NOTE 4: Unused control inputs (A, CLKIN, R/$\overline{W}$) must be held high or low to prevent them from floating.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVT8980 MIN | SN54LVT8980 TYP† | SN54LVT8980 MAX | SN74LVT8980 MIN | SN74LVT8980 TYP† | SN74LVT8980 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | D, RDY | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = – 4 mA | 2.3 | | | 2.3 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = – 4 mA | 2.6 | | | 2.6 | | | |
| | | | $I_{OH}$ = – 8 mA | 2.4 | | | 2.4 | | | |
| | TCK, TDO, TMS, $\overline{TRST}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = – 8 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = – 24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| $V_{OL}$ | D, RDY | $V_{CC}$ = MIN to MAX‡, | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 4 mA | | | 0.55 | | | 0.55 | |
| | | | $I_{OL}$ = 6 mA | | | 0.8 | | | 0.8 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 4 mA | | | 0.55 | | | 0.55 | |
| | | | $I_{OL}$ = 6 mA | | | 0.8 | | | 0.8 | |
| | TCK, TDO, TMS, $\overline{TRST}$ | $V_{CC}$ = MIN to MAX‡, | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | |
| | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| $I_I$ | A, CLKIN, $\overline{RST}$, R/$\overline{W}$, $\overline{STRB}$, TDI, $\overline{TOE}$ | $V_{CC}$ = 0 or MAX‡, | $V_I$ = 5.5 V | | | 10 | | | 10 | µA |
| | A, CLKIN, R/$\overline{W}$ | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | |
| | RST, STRB, TDI, $\overline{TOE}$ | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | –40 | | –100 | – 40 | | –100 | |
| $I_{off}$ | TCK, TDO, TMS, $\overline{TRST}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | ±100 | | | ±100 | µA |
| $I_{OZH}$ | D, TCK, TDO, TMS, $\overline{TRST}$ | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 5 | | | 5 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –5 | | | –5 | |
| $I_{OZPU}$§ | TCK, TDO, TMS, $\overline{TRST}$ | $V_{CC}$ = 0 to 1.5 V, $V_O$ = 0.5 V to 3 V, $\overline{TOE}$ = 0 | | | | ±100 | | | ±100 | µA |
| $I_{OZPD}$§ | | $V_{CC}$ = 1.5 V to 0, $V_O$ = 0.5 V to 3 V, $\overline{TOE}$ = 0 | | | | ±100 | | | ±100 | |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 3.6 V, $V_I$ = $V_{CC}$ or GND | $I_O$ = 0, | | | 0.5 | | | 0.5 | mA |
| | Outputs low | | | | | 7 | | | 7 | |
| | Outputs disabled | | | | | 0.5 | | | 0.5 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 3 V to 3.6 V, Other inputs at $V_{CC}$ or GND | One input at $V_{CC}$ – 0.6 V, | | | 0.2 | | | 0.2 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 5 | | | 5 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 7 | | | 7 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This parameter is characterized but not tested.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

PRODUCT PREVIEW

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## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 9 and Figure 10)

| | | | SN54LVT8980 | | | | SN74LVT8980 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency, CLKIN | TCK=CLKIN (CDIV=0) | 0 | 20 | 0 | 16 | 0 | 20 | 0 | 16 | MHz |
| | | TCK=CLKIN/2 (CDIV=1) | 0 | 40 | 0 | 32 | 0 | 40 | 0 | 32 | |
| | | TCK≤CLKIN/4 (CDIV≥2) | 0 | 70 | 0 | 64 | 0 | 70 | 0 | 64 | |
| $t_w$ | Pulse duration, CLKIN high or low | TCK=CLKIN (CDIV=0) | 25 | | 31 | | 25 | | 31 | | ns |
| | | TCK=CLKIN/2 (CDIV=1) | 12.5 | | 15.6 | | 12.5 | | 15.6 | | |
| | | TCK≤CLKIN/4 (CDIV≥2) | 7.1 | | 7.8 | | 7.1 | | 7.8 | | |
| $t_w$ | Pulse duration, $\overline{RST}$ low | | 10 | | 10 | | 10 | | 10 | | ns |
| $t_w$ | Pulse duration, $\overline{STRB}$ low | | 8 | | 8 | | 8 | | 8 | | ns |
| $t_{su}$ | Setup time, A before $\overline{STRB}$↓ | Read or write (R/$\overline{W}$ high or low) | 10 | | 10 | | 10 | | 10 | | ns |
| $t_{su}$ | Setup time, D before $\overline{STRB}$↑ | Write (R/$\overline{W}$ low) | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, R/$\overline{W}$ before $\overline{STRB}$↓ | | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, TDI before CLKIN↑ | | 5 | | 5 | | 5 | | 5 | | ns |
| $t_h$ | Hold time, A after $\overline{STRB}$↑ | Read or write (R/$\overline{W}$ high or low) | 5 | | 5 | | 5 | | 5 | | ns |
| $t_h$ | Hold time, D after $\overline{STRB}$↑ | Write (R/$\overline{W}$ low) | 15 | | 15 | | 15 | | 15 | | ns |
| $t_h$ | Hold time, R/$\overline{W}$ after $\overline{STRB}$↑ | | 6 | | 6 | | 6 | | 6 | | ns |
| $t_h$ | Hold time, TDI after CLKIN↑ | | 10 | | 10 | | 10 | | 10 | | ns |

PRODUCT PREVIEW

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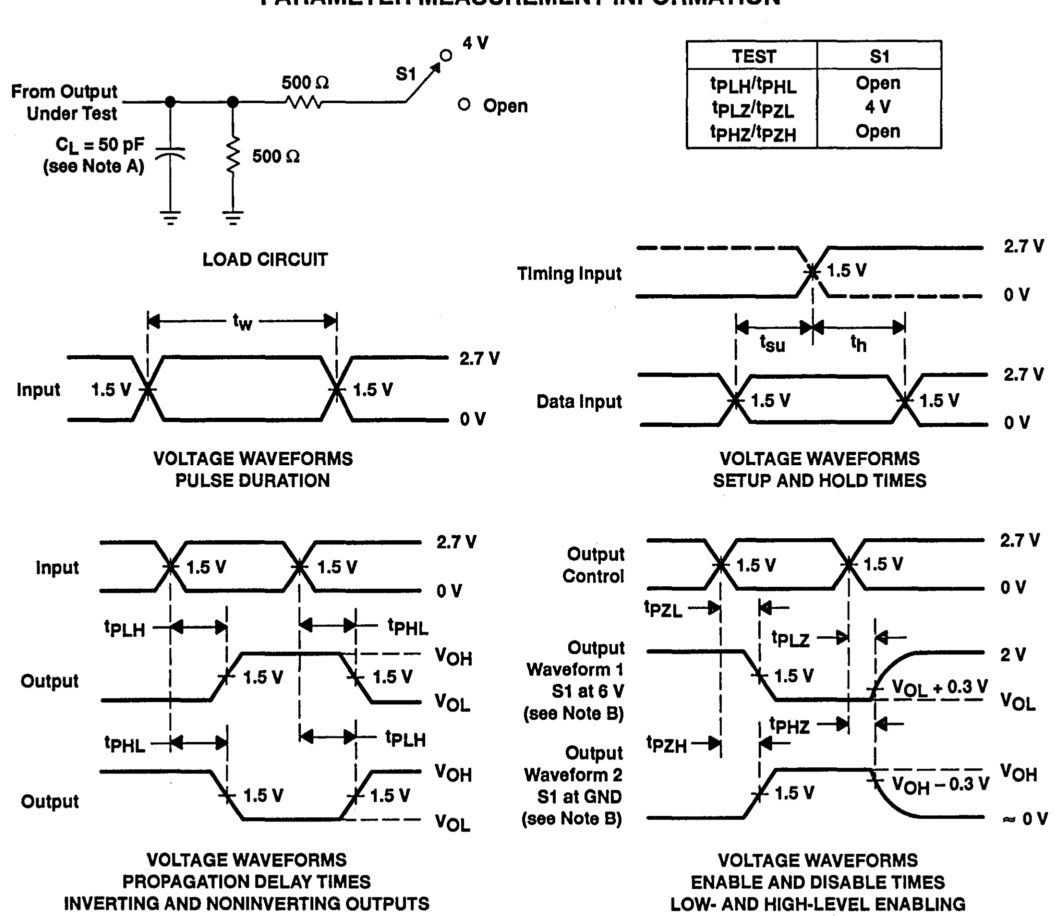
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 9 and Figure 10)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVT8980 | | | SN74LVT8980 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$= 2.7 V | $V_{CC}$ = 3.3 V ± 0.3 V | | | $V_{CC}$= 2.7 V | |
| | | | MIN | MAX | MAX | MIN | TYP† | MAX | MAX | |
| $t_{PLH}$ | CLKIN | TCK | 6 | 20 | 25 | 8 | 10 | 17 | 20 | ns |
| $t_{PHL}$ | | | 6 | 20 | 25 | 8 | 10 | 17 | 20 | |
| $t_{PLH}$ | CLKIN | TDO, TMS | 12 | 35 | 40 | 14 | 18 | 30 | 35 | ns |
| $t_{PHL}$ | | | 12 | 35 | 40 | 14 | 18 | 30 | 35 | |
| $t_{PLH}$ | RST↓ | D | 3 | 35 | 40 | 4 | 17 | 30 | 35 | ns |
| $t_{PHL}$ | | | 3 | 35 | 40 | 4 | 17 | 30 | 35 | |
| $t_{PLH}$ | RST↓ | RDY | 3 | 35 | 40 | 4 | 17 | 30 | 35 | ns |
| $t_{PHL}$ | | | 3 | 35 | 40 | 4 | 17 | 30 | 35 | |
| $t_{PHL}$ | $\overline{\text{RST}}$↓ | TCK | 5 | 30 | 35 | 6 | 15 | 25 | 30 | ns |
| $t_{PLH}$ | $\overline{\text{RST}}$↓ | TDO, TMS, $\overline{\text{TRST}}$ | 5 | 30 | 35 | 6 | 15 | 25 | 30 | ns |
| $t_{PLH}$ | $\overline{\text{STRB}}$↑ | RDY | 3 | 22 | 28 | 5 | 10 | 18 | 22 | ns |
| $t_{PHL}$ | $\overline{\text{STRB}}$↓ | RDY | 3 | 22 | 28 | 5 | 10 | 18 | 22 | |
| $t_{PLH}$ | STRB↑ | TCK, TDO, TMS, TRST discrete mode | 8 | 28 | 35 | 10 | 14 | 22 | 28 | ns |
| $t_{PHL}$ | | | 8 | 28 | 35 | 10 | 14 | 22 | 28 | |
| $t_{PLH}$ | STRB↑ | TCK, TDO, TMS, TRST other modes | 6 | 40 | 45 | 8 | 20 | 35 | 40 | ns |
| $t_{PHL}$ | | | 6 | 40 | 45 | 8 | 20 | 35 | 40 | |
| $t_{PZH}$ | $\overline{\text{STRB}}$↓ | D | 3 | 20 | 25 | 4 | 8 | 15 | 18 | ns |
| $t_{PZL}$ | | | 3 | 20 | 25 | 4 | 8 | 15 | 18 | |
| $t_{PZH}$ | $\overline{\text{STRB}}$↑ | TCK, TDO, TMS, TRST | 5 | 30 | 35 | 7 | 15 | 25 | 30 | ns |
| $t_{PZL}$ | | | 5 | 30 | 35 | 7 | 15 | 25 | 30 | |
| $t_{PZH}$ | $\overline{\text{TOE}}$↓ | TCK, TDO, TMS, TRST | 2 | 15 | 18 | 2 | 6 | 12 | 15 | ns |
| $t_{PZL}$ | | | 2 | 15 | 18 | 2 | 6 | 12 | 15 | |
| $t_{PHZ}$ | $\overline{\text{STRB}}$↑ | D | 3 | 20 | 25 | 4 | 8 | 15 | 18 | ns |
| $t_{PLZ}$ | | | 3 | 20 | 25 | 4 | 8 | 15 | 18 | |
| $t_{PHZ}$ | $\overline{\text{STRB}}$↑ | TCK, TDO, TMS, TRST | 5 | 30 | 35 | 7 | 15 | 25 | 30 | ns |
| $t_{PLZ}$ | | | 5 | 30 | 35 | 7 | 15 | 25 | 30 | |
| $t_{PHZ}$ | $\overline{\text{TOE}}$↑ | TCK, TDO, TMS, TRST | 2 | 15 | 18 | 2 | 6 | 12 | 15 | ns |
| $t_{PLZ}$ | | | 2 | 15 | 18 | 2 | 6 | 12 | 15 | |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

## PARAMETER MEASUREMENT INFORMATION

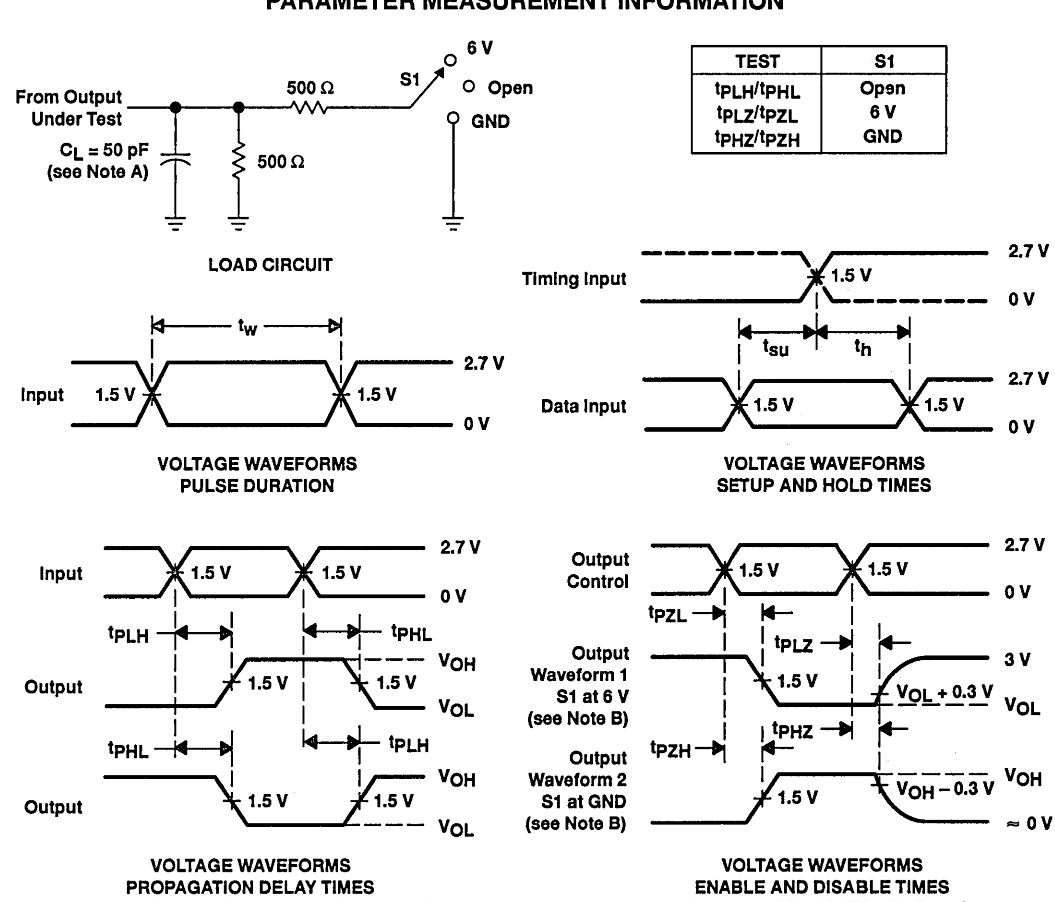



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 4 V |
| $t_{PHZ}/t_{PZH}$ | Open |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 9. Load Circuit and Voltage Waveforms (D and RDY Outputs)**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

**Figure 10. Load Circuit and Voltage Waveforms (TCK, TDO, TMS, $\overline{\text{TRST}}$ Outputs)**

- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Control Operation of Up to Six Parallel Target Scan Paths**
- **Accommodate Pipeline Delay to Target of Up to 31 Clock Cycles**
- **Scan Data Up to $2^{32}$ Clock Cycles**
- **Execute Instructions for Up to $2^{32}$ Clock Cycles**
- **Each Device Includes Four Bidirectional Event Pins for Additional Test Capability**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-µm Process**
- **Packaged in 44-Pin Plastic Leaded Chip Carrier (FN), 68-Pin Ceramic Pin Grid Array (GB), and 68-Pin Ceramic Quad Flat Packages (HV)**

## description

The 'ACT8990 test-bus controllers (TBC) are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of components supports IEEE Standard 1149.1-1990 (JTAG) boundary scan to facilitate testing of complex circuit-board assemblies. The 'ACT8990 differ from other SCOPE™ integrated circuits. Their function is to control the JTAG serial-test bus rather than being target boundary-scannable devices.

The required signals of the JTAG serial-test bus – test clock (TCK), test mode select (TMS), test data input (TDI), and test data output (TDO) can be connected from the TBC to a target device without additional logic. This is done as a chain of IEEE Standard 1149.1-1990 boundary-scannable components that share the same serial-test bus. The TBC generates TMS and TDI signals for its target(s), receives TDO signals from its target(s), and buffers its test clock input (TCKI) to a test clock output (TCKO) for distribution to its target(s). The TMS, TDI, and TDO signals can be connected to a target directly or via a pipeline, with a retiming delay of up to 31 bits. Since the TBC can be configured to generate up to six separate TMS signals [TMS (5–0)], it can be used to control up to six target scan paths that are connected in parallel (i.e., sharing common TCK, TDI, and TDO signals).

While most operations of the TBC are synchronous to TCKI, a test-off ($\overline{\text{TOFF}}$) input is provided for output control of the target interface, and a test-reset ($\overline{\text{TRST}}$) input is provided for hardware/software reset of the TBC. In addition, four event [EVENT (3–0)] I/Os are provided for asynchronous communication to target device(s). Each event has its own event generation/detection logic, and detected events can be counted by two 16-bit counters.

The TBC operates under the control of a host microprocessor/microcontroller via the 5-bit address bus [ADRS (4–0)] and the 16-bit read/write data bus [DATA (15–0)]. Read ($\overline{\text{RD}}$) and write ($\overline{\text{WR}}$) strobes are implemented such that the critical host-interface timing is independent of the TCKI period. Any one of 24 registers can be addressed for read and/or write operations. In addition to control and status registers, the TBC contains two command registers, a read buffer, and a write buffer. Status of the TBC is transmitted to the host via ready ($\overline{\text{RDY}}$) and interrupt ($\overline{\text{INT}}$) outputs.

Major commands can be issued by the host to cause the TBC to generate the TMS sequences necessary to move the target(s) from any stable test-access-port (TAP) controller state to any other stable TAP state, to execute instructions in the Run-Test/Idle TAP state, or to scan instruction or test data through the target(s). A 32-bit counter can be preset to allow a predetermined number of execution or scan operations.

Serial data that appears at the selected TDI input (TDI1 or TDI0) is transferred into the read buffer, which can be read by the host to obtain up to 16 bits of the serial-data stream. Serial data that is transmitted from the TDO output is written by the host to the write buffer.

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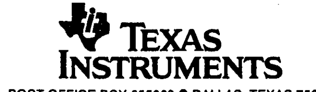
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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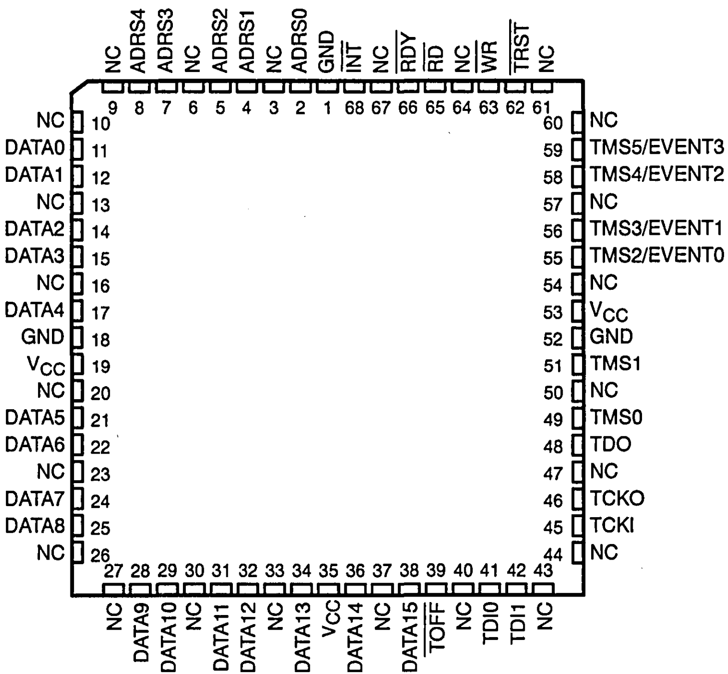
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

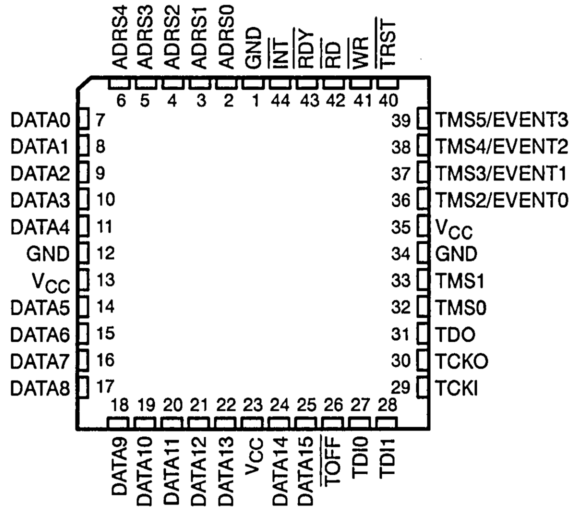
The SN54ACT8990 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT8990 is characterized for operation from 0°C to 70°C.

**SN54ACT8990 . . . HV PACKAGE
(TOP VIEW)**




NC – No internal connection

**SN74ACT8990 . . . FN PACKAGE**
**(TOP VIEW)**




**SN54ACT8990 . . . GB PACKAGE**
**(TOP VIEW)**

1 2 3 4 5 6 7 8 9 10 11

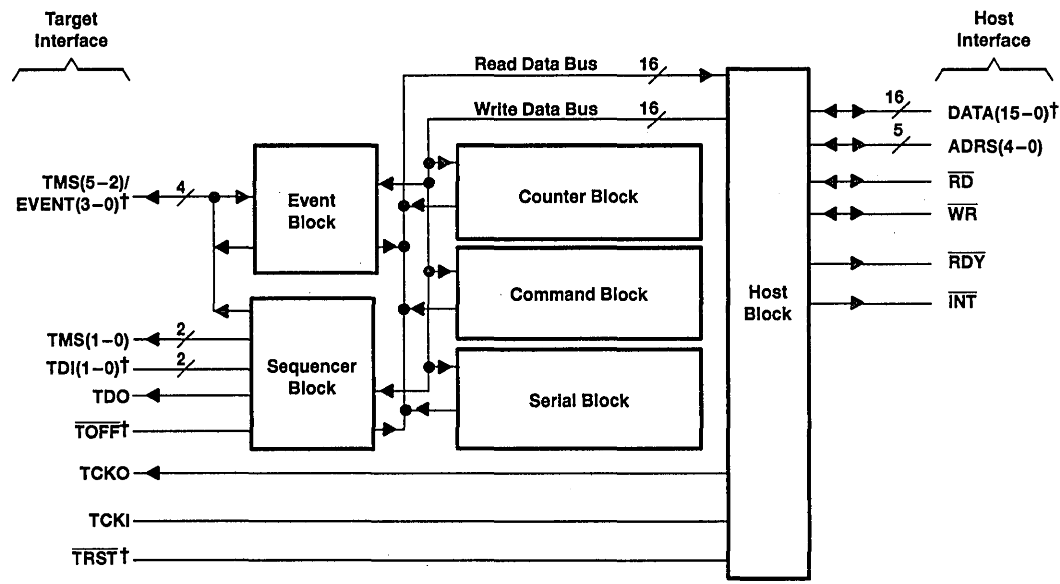
A
B
C
D
E
F
G
H
J
K
L

**Table 1. Terminal Assignments**

| TERMINAL | | TERMINAL | | TERMINAL | | TERMINAL | |
|---|---|---|---|---|---|---|---|
| NO. | NAME | NO. | NAME | NO. | NAME | NO. | NAME |
| A2 | NC | B10 | NC | F11 | NC | K6 | NC |
| A3 | ADRS4 | B11 | NC | G1 | DATA5 | K7 | $V_{CC}$ |
| A4 | NC | C1 | DATA2 | G2 | NC | K8 | DATA15 |
| A5 | ADRS1 | C2 | DATA1 | G10 | NC | K9 | TDI0 |
| A6 | ADRS0 | C3 | NC | G11 | TMS1 | K10 | NC |
| A7 | NC | C10 | TMS4/EVENT2 | H1 | NC | K11 | TCKI |
| A8 | $\overline{INT}$ | C11 | TMS5/EVENT3 | H2 | DATA6 | L2 | DATA9 |
| A9 | $\overline{RD}$ | D1 | DATA4 | H10 | TDO | L3 | NC |
| A10 | $\overline{TRST}$ | D2 | DATA3 | H11 | TMS0 | L4 | DATA12 |
| B1 | DATA0 | D10 | TMS3/EVENT1 | J1 | DATA8 | L5 | DATA13 |
| B2 | NC | D11 | NC | J2 | DATA7 | L6 | NC |
| B3 | ADRS3 | E1 | NC | J10 | TCKO | L7 | DATA14 |
| B4 | ADRS2 | E2 | GND | J11 | NC | L8 | $\overline{TOFF}$ |
| B5 | NC | E10 | $V_{CC}$ | K1 | NC | L9 | TDI1 |
| B6 | NC | E11 | TMS2/EVENT0 | K2 | NC | L10 | NC |
| B7 | GND | F1 | $V_{CC}$ | K3 | DATA10 | | |
| B8 | $\overline{RDY}$ | F2 | NC | K4 | DATA11 | | |
| B9 | $\overline{WR}$ | F10 | GND | K5 | NC | | |

NC – No internal connection

## functional block diagram




† Inputs have internal pullup resistors.

## Terminal Functions

| TERMINAL NAME | I/O | DESCRIPTION |
|---|---|---|
| ADRS4–ADRS0 | I | Address inputs. ADRS4–ADRS0 form the 5-bit address bus that interfaces the TBC to its host. These inputs specify the TBC register to be read from or written to. |
| DATA15–DATA0 | I/O | Data inputs and outputs. DATA15–DATA0 form the 16-bit bidirectional data bus that interfaces the TBC to its host. Data is read from or written to the TBC register using this data bus. |
| GND | | Ground |
| $\overline{\text{INT}}$ | O | Interrupt. $\overline{\text{INT}}$ transmits an interrupt signal to the host. When the TBC requires service from the host, $\overline{\text{INT}}$ is asserted (low). $\overline{\text{INT}}$ will remain asserted (low) until the host has completed the required service. |
| NC | | No connection |
| $\overline{\text{RD}}$ | I | Read strobe. $\overline{\text{RD}}$ is the active low output enable for the data bus. $\overline{\text{RD}}$ is used as the strobe for reading data from the selected TBC register. |
| $\overline{\text{RDY}}$ | O | Ready. $\overline{\text{RDY}}$ transmits a status signal to the host. When the TBC is ready to accept a read or write operation from the host, $\overline{\text{RDY}}$ is asserted (low). $\overline{\text{RDY}}$ is not asserted (high) when the TBC is in recovery from a read, write, command, or reset operation. |
| TCKI | I | Test clock input. TCKI is the clock input for the TBC. Most operations of the TBC are synchronous to TCKI. When enabled, all target interface outputs change on the falling edge of TCKI. Sampling of target interface inputs are configured to occur on either the rising edge or falling edge of TCKI. |
| TCKO | O | Test clock output. TCKO distributes TCK to the target(s). The TCKO is configured to be disabled, constant zero, constant one, or to follow TCKI. When TCKO follows TCKI, it is delayed to match the delay of generating the TDO and TMS signals. |
| TDI1–TDI0 | I | Test data inputs. The TDI1–TDI0 serial inputs are used for shifting test data from the target(s). The TDI inputs can be directly connected to the TDO pin(s) of the target(s). |
| TDO | O | Test data output. TDO is used for shifting test data into the target(s). TDO can be directly connected to the TDI terminal(s) of the target(s). |
| TMS1–TMS0 | O | Test mode select outputs. These parallel outputs transmit TMS signals to the target(s), which direct them through their TAP controller states. TMS1–TMS0 can be directly connected to the TMS terminals of the target(s). |
| TMS5–TMS2/ EVENT3–EVENT0 | I/O | Test mode select outputs or event inputs/outputs. These I/Os can be configured for use as either TMS outputs or event inputs/outputs. As TMS outputs, they function similarly to TMS1–TMS0 above. As event I/Os, they can be used to receive/transmit interrupt signals to/from the target(s). |
| $\overline{\text{TOFF}}$ | I | Test-off input. $\overline{\text{TOFF}}$ is the active low output disable for all outputs and I/Os of the target interface (TCKO, TDO, TMS, TMS/EVENT). |
| $\overline{\text{TRST}}$ | I | Test-reset input. $\overline{\text{TRST}}$ is used to initiate hardware and software reset operations of the TBC. Hardware reset begins when $\overline{\text{TRST}}$ is asserted (low). Software reset begins when $\overline{\text{TRST}}$ is released (high) and proceeds synchronously to TCKI to completion in a predetermined number of cycles. |
| $\overline{\text{WR}}$ | I | Write input. $\overline{\text{WR}}$ is the strobe for writing data to a TBC data register. Signals present at the data and address buses are captured on the rising edge of $\overline{\text{WR}}$. |
| $V_{CC}$ | | Supply voltage |

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .......... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .......... –0.5 V to $V_{CC}$
Output voltage range, $V_O$ (see Note 1) .......... –0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) .......... ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) .......... ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) .......... ±25 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): FN package .......... 1.5W
Storage temperature range, $T_{stg}$ .......... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | SN54ACT8990 | | SN74ACT8990 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $T_A$ | Operating free-air temperature | –55 | 125 | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ACT8990 | | SN74ACT8990 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –20 μA | 4.4 | | | 4.4 | | 4.4 | | V |
| | | | $I_{OH}$ = –8 mA | 3.7 | | | 3.7 | | 3.7 | | |
| | | $V_{CC}$ = 5.5 V | $I_{OH}$ = –20 μA | 5.4 | | | 5.4 | | 5.4 | | |
| | | | $I_{OH}$ = –8 mA | 4.7 | | | 4.7 | | 4.7 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V to 5.5 V | $I_{OL}$ = 20 μA | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | $I_{OL}$ = 8 mA | | | 0.5 | | 0.5 | | 0.5 | |
| $I_I$ | ADRS, $\overline{RD}$, $\overline{WR}$, TCKI | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | ±1 | | ±1 | μA |
| | TDI, $\overline{TOFF}$, $\overline{TRST}$ | $V_{CC}$ = 5.5 V | $V_I$ = $V_{CC}$ | | | ±1 | | ±1 | | ±1 | |
| | | | $V_I$ = GND | –35 | –70 | –250 | –35 | –250 | –35 | –250 | |
| $I_{OZ}$‡ | $\overline{INT}$, $\overline{RDY}$, TCKO, TDO, TMS | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or GND | | | ±10 | | ±10 | | ±10 | μA |
| | DATA, TMS/EVENT | $V_{CC}$ = 5.5 V | $V_O$ = $V_{CC}$ | | | ±10 | | ±10 | | ±10 | |
| | | | $V_O$ = GND | –35 | –70 | –250 | –35 | –250 | –35 | –250 | |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, $I_O$ = 0, | $V_I$ = $V_{CC}$ or GND | | | 450* | | 450 | | 450 | μA |
| | | $V_{CC}$ = 5.5 V, $f_{clock}$ = 30 MHz | $C_L$ = 50 pF | | 100 | | | | | | mA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | | | 5* | | | | | | pF |
| $C_{io}$ | | $V_I$ = $V_{CC}$ or GND | | | 9* | | | | | | pF |
| $C_o$ | | $V_I$ = $V_{CC}$ or GND | | | 8* | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† Typical values are at $V_{CC}$ = 5 V.
‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)**

| | | | SN54ACT8990 | | SN74ACT8990 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 30 | 0 | 30 | MHz |
| $t_w$ | Pulse duration | $\overline{RD}$ low† | | | 5.5 | | ns |
| | | $\overline{WR}$ low | 5.5 | | 5.5 | | ns |
| | | EVENT high or low | 8 | | 8 | | |
| | | TCKI high or low | 10.5 | | 10.5 | | |
| | | $\overline{TRST}$ low | 6 | | 6 | | |
| $t_{su}$ | Setup time | ADRS† before $\overline{RD}$↑ | | | 6.5 | | ns |
| | | ADRS before $\overline{WR}$↑ | 6.5 | | 6.5 | | ns |
| | | DATA before $\overline{WR}$↑ | 6 | | 6 | | |
| | | EVENT before TCKI↑ | 6 | | 5.5 | | |
| | | EVENT before TCKI↓ | 5 | | 5 | | |
| | | TDI before TCKI↑ | 2 | | 2 | | |
| | | TDI before TCKI↓ | 2 | | 2 | | |
| $t_h$ | Hold time | ADRS† after $\overline{RD}$↑ | | | 5 | | ns |
| | | ADRS after $\overline{WR}$↑ | 5.5 | | 5 | | ns |
| | | DATA after $\overline{WR}$↑ | 5.5 | | 5.5 | | |
| | | EVENT after TCKI↑ | 5.5 | | 5 | | |
| | | EVENT after TCKI↓ | 5 | | 5 | | |
| | | TDI after TCKI↑ | 4 | | 2.5 | | |
| | | TDI after TCKI↓ | 4 | | 2.5 | | |

† Applies only in the case where ADRS (4-0) = 10110 (read buffer).

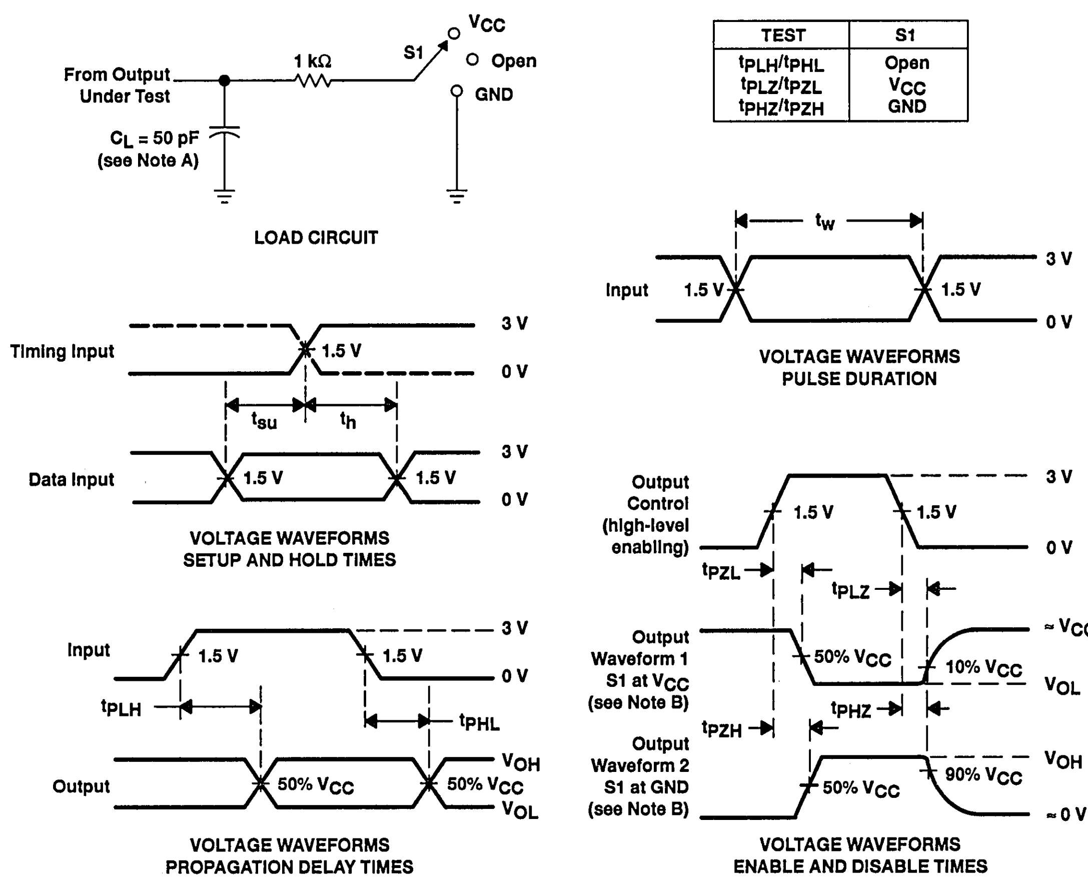
## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ACT8990 | | SN74ACT8990 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 30 | | 30 | | MHz |
| $t_{PLH}$ | ADRS | DATA | 8 | 43 | 19.5 | 39.3 | ns |
| $t_{PHL}$ | | | 8 | 43 | 19.5 | 39.3 | |
| $t_{PLH}$ | $\overline{RD}$↑ | $\overline{RDY}$ | 5.3 | 17 | 5.3 | 13.8 | ns |
| | $\overline{WR}$↑ | | 2.5 | 16 | 2.5 | 13 | |
| $t_{PLH}$ | TCKI↑ | $\overline{INT}$ | 3.7 | 16 | 3.7 | 12.9 | ns |
| $t_{PHL}$ | | | 5.5 | 15 | 5.5 | 13.1 | |
| $t_{PHL}$ | TCKI↑ | $\overline{RDY}$ | 4.4 | 15 | 4.4 | 13.4 | ns |
| $t_{PLH}$ | TCKI↑ | TCKO | 3.3 | 17 | 3.3 | 14.1 | ns |
| $t_{PLH}$ | TCKI↓ | TCKO | 2.3 | 19 | 2.3 | 15.9 | ns |
| $t_{PHL}$ | | | 3.6 | 17 | 3.6 | 15.6 | |
| $t_{PLH}$ | TCKI↓ | TDO | 2.9 | 19 | 2.9 | 17.5 | ns |
| $t_{PHL}$ | | | 5.2 | 20 | 5.2 | 17.9 | |
| $t_{PLH}$ | TCKI↓ | TMS | 3.1 | 19 | 3.1 | 17.5 | ns |
| $t_{PHL}$ | | | 5.1 | 19 | 5.1 | 18.2 | |
| $t_{PLH}$ | TCKI↓ | TMS/EVENT | 1.5 | 19 | 1.5 | 17.5 | ns |
| $t_{PHL}$ | | | 3.5 | 20 | 3.5 | 18.9 | |
| $t_{PZH}$ | $\overline{RD}$↓ | DATA | 3.8 | 21 | 3.8 | 17.6 | ns |
| $t_{PZL}$ | | | 6.8 | 28 | 6.8 | 22.6 | |
| $t_{PZH}$ | TCKI↑ | $\overline{INT}$ | 4.9 | 19 | 4.9 | 15.3 | ns |
| | | $\overline{RDY}$ | 3.6 | 19 | 3.6 | 15.3 | |
| $t_{PZH}$ | TCKI↓ | TCKO | 4.1 | 23 | 4.1 | 19.2 | ns |
| $t_{PZL}$ | | | 4.8 | 20 | 4.8 | 17.4 | |
| $t_{PZH}$ | TCKI↓ | TDO | 4.3 | 22 | 4.3 | 19.5 | ns |
| $t_{PZL}$ | | | 5 | 20 | 5 | 17.7 | |
| $t_{PZH}$ | TCKI↓ | TMS | 4.6 | 23 | 4.6 | 19.9 | ns |
| $t_{PZL}$ | | | 5.1 | 20 | 5.1 | 18.5 | |
| $t_{PZH}$ | TCKI↓ | TMS/EVENT | 2 | 21 | 2 | 18.8 | ns |
| $t_{PZL}$ | | | 3.2 | 20 | 3.2 | 18.7 | |
| $t_{PZH}$ | $\overline{TOFF}$↑ | TCKO | 4.6 | 16 | 4.6 | 12.2 | ns |
| $t_{PZL}$ | | | 3.1 | 14 | 3.1 | 10.3 | |
| $t_{PZH}$ | $\overline{TOFF}$↑ | TDO | 4.4 | 15 | 4.4 | 12.2 | ns |
| $t_{PZL}$ | | | 3.5 | 14 | 3.5 | 10.8 | |
| $t_{PZH}$ | $\overline{TOFF}$↑ | TMS | 3.1 | 16.2 | 3.1 | 14.7 | ns |
| $t_{PZL}$ | | | 1.9 | 16.7 | 1.9 | 13.6 | |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (continued) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ACT8990 | | SN74ACT8990 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PZH}$ | $\overline{TOFF}$↑ | TMS/EVENT | 2.3 | 15.3 | 2.3 | 13.8 | ns |
| $t_{PZL}$ | | | 2.7 | 16.4 | 2.7 | 13.9 | |
| $t_{PHZ}$ | $\overline{RD}$↑ | DATA | 3.8 | 18.4 | 3.8 | 15.4 | ns |
| $t_{PLZ}$ | | | 4.1 | 17.1 | 4.1 | 14.8 | |
| $t_{PHZ}$ | TCKI↓ | TCKO | 6.7 | 20.4 | 6.7 | 19.8 | ns |
| $t_{PLZ}$ | | | 4.8 | 21.1 | 4.8 | 20.4 | |
| $t_{PHZ}$ | TCKI↓ | TDO | 5.1 | 21.7 | 5.1 | 21.3 | ns |
| $t_{PLZ}$ | | | 5 | 20.7 | 5 | 20.3 | |
| $t_{PHZ}$ | TCKI↓ | TMS | 6.9 | 22.4 | 6.9 | 21.9 | ns |
| $t_{PLZ}$ | | | 4.6 | 20.6 | 4.6 | 20.1 | |
| $t_{PHZ}$ | TCKI↓ | TMS/EVENT | 4.7 | 22.5 | 4.7 | 22.1 | ns |
| $t_{PLZ}$ | | | 2.8 | 20.5 | 2.8 | 20.1 | |
| $t_{PHZ}$ | $\overline{TOFF}$↓ | TCKO | 5 | 15.6 | 5 | 15.4 | ns |
| $t_{PLZ}$ | | | 4.4 | 15.5 | 4.4 | 15.3 | |
| $t_{PHZ}$ | $\overline{TOFF}$↓ | TDO | 5.6 | 16.6 | 5.6 | 16.5 | ns |
| $t_{PLZ}$ | | | 4.6 | 15.4 | 4.6 | 15.4 | |
| $t_{PHZ}$ | $\overline{TOFF}$↓ | TMS | 4.8 | 19.1 | 4.8 | 17.1 | ns |
| $t_{PLZ}$ | | | 4.4 | 17 | 4.4 | 15.8 | |
| $t_{PHZ}$ | $\overline{TOFF}$↓ | TMS/EVENT | 4.5 | 18.8 | 4.5 | 17.3 | ns |
| $t_{PLZ}$ | | | 2.4 | 17.1 | 2.4 | 16.2 | |
| $t_{PHZ}$ | $\overline{TRST}$↓ | DATA | 5.7 | 23 | 5.7 | 20.8 | ns |
| $t_{PLZ}$ | | | 4.2 | 20.3 | 4.2 | 20 | |
| $t_{PHZ}$ | $\overline{TRST}$↓ | $\overline{INT}$ | 6 | 19.6 | 8 | 19.5 | ns |
| $t_{PLZ}$ | | | 6.1 | 18 | 6.1 | 17.8 | |
| $t_{PHZ}$ | $\overline{TRST}$↓ | $\overline{RDY}$ | 6.5 | 18.8 | 6.5 | 18.7 | ns |
| $t_{PLZ}$ | | | 4.8 | 17.8 | 4.8 | 17.8 | |
| $t_{PHZ}$ | $\overline{TRST}$↓ | TMS/EVENT | 6 | 21.1 | 6 | 21.1 | ns |
| $t_{PLZ}$ | | | 4.2 | 20 | 4.2 | 19.9 | |

## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

NOTES: A. $C_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

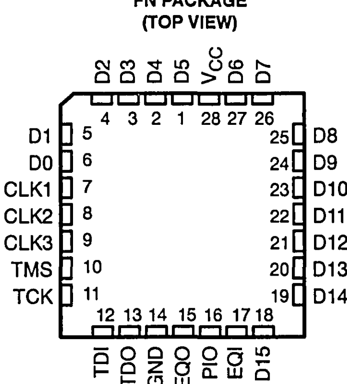
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.

D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

- Member of the Texas Instruments *SCOPE*™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Contains a 1024-Word by 16-Bit Random-Access Memory (RAM) to Store the States of a Digital Bus
- Test Operations Are Synchronous to the Test Clock or System Clock(s)
- Contains Texas Instruments Event Qualification Module for Real-Time System Test
- Eight Protocols for On-Line Signal Monitoring and Test Operations
- Inputs Are TTL-Voltage Compatible
- Performs Parallel-Signature Analysis (PSA) of Data Inputs With User-Definable Feedback
- Data Inputs Are Maskable During PSA Operations
- Cascaded PSA Mode Allows Compression of Parallel Data Paths Greater Than 16 Bits in Width
- Direct Memory Access (DMA) Speeds Memory and Register File Read/Write Operations
- Power-Down Mode When RAM Is Idling Reduces Power Dissipation
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Packaged in 28-Pin Plastic Chip Carriers

FN PACKAGE
(TOP VIEW)




## description

The SN74ACT8994 digital bus monitor (DBM) is a member of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of components supports IEEE Standard 1149.1-1990 (JTAG) boundary scan to facilitate testing of complex circuit-board assemblies. The DBM is a boundary-scannable device designed to monitor and/or store the values of a digital bus up to 16 bits in width. It resides in parallel with the bus being monitored.

Data at the D-input pins can be stored in a scannable random-access memory (RAM). Up to 1024 words of 16 bits can be stored. A parallel-signature analysis (PSA) can be performed on the data or on the contents of memory. The PSA operations use a linear-feedback shift-register technique to compress data into a signature. The user can configure the device to mask any combination of data inputs and control the feedback used during PSA operations.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

The DBM receives instructions via the IEEE Standard 1149.1-1990 test access port (TAP) interface. The TAP interface consists of test clock (TCK), test mode select (TMS), test data input (TDI), and test data output (TDO) pins.

The DBM can be operated in the off-line mode or the on-line mode. In the off-line mode, the device performs test operations independent of system conditions. Off-line test operations include parallel-signature analysis (PSA) on the contents of RAM and external test.

In the on-line mode, the DBM can be configured to perform test operations that are initiated based on system conditions and that operate synchronously to a logical combination of one or more system clocks. The device allows sample, storage, and/or PSA operations to be performed according to one of eight protocols. Compare patterns, which can be stored in the event-qualification module (EQM), allow the user to define specific values of the 16-bit bus for which the test operations are to be performed.

The 1024-word by 16-bit RAM and the EQM register files can be serially accessed using IEEE-Standard-1149.1-1990-compatible read and write instructions. However, direct memory access (DMA) instructions also are provided to speed transfer of large amounts of data to and from the RAM and EQM.

The polynomial input/output (PIO) is a bidirectional pin used to cascade more than one DBM to provide signature analysis on a bus larger than 16 bits.

The SN74ACT8994 is characterized for operation from 0°C to 70°C.

## functional block diagram

Boundary-Scan Register

EQI 17
CLK1 7
CLK2 8
CLK3 9
D0 6
D1 5
D2 4
D3 3
D4 2
D5 1
D6 27
D7 26
D8 25
D9 24
D10 23
D11 22
D12 21
D13 20
D14 19
D15 18
$V_{CC}$
TDI 12
$V_{CC}$
TMS 10
TCK 11

PCI
Test-Cell Register
16
RAM
EQM
Control/
Bypass/
Header Registers
TAP Controller/
Instruction Register
TDO
MUX

15 EQO
16 PIO
13 TDO

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| CLK1, CLK2, CLK3 | 7, 8, 9 | I | Clock 1, 2, and 3. CLK1 – CLK3 provide various types of system clock and control signals to the DBM for the purpose of synchronizing test operations to the system under test. |
| D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15 | 6, 5, 4, 3, 2, 1, 27, 26, 25 24, 23, 22, 21, 20, 19, 18 | I | Data bus inputs. D15–D0 form the 16-bit digital bus that is monitored by the DBM. Data that appears at this bus can be compressed into a 16-bit signature and/or stored in the 1024-word RAM. Each data bit can be individually masked during test operations. |
| EQI | 17 | I | Event-qualification input. EQI is used to receive an external (global) event signal from user-defined event-qualification logic. EQI can be configured to initiate test operations in the on-line mode. |
| EQO | 15 | O | Event-qualification output. EQO is used to transmit any of several internally generated status signals. EQO can be configured to transmit internal (local) event signals to external (global) event-qualification logic. |
| GND | 14 | | Ground |
| PIO | 16 | I/O | Polynominal input/output. PIO is used to cascade more than one DBM to provide signature analysis on a bus larger than 16 bits. Its configuration as an input or output for a particular DBM device depends on the significance (most, middle, or least) of that DBM in the scan path. |
| TCK | 11 | I | Test clock. One of four pins required by IEEE Standard 1149.1-1990. Scan operations of the DBM are synchronous to TCK. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK. |
| TDI | 12 | I | Test data input. One of four pins required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | 13 | O | Test data output. One of four pins required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | 10 | I | Test mode select. One of four pins required by IEEE standard 1149.1-1990. TMS directs the DBM through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | 28 | | Supply voltage |

## detailed description

The general architecture of the DBM is shown in the functional block diagram. The DBM contains eight data registers and an instruction register that are accessed serially through the TAP. The TAP controller is a finite-state machine that issues control and enable signals throughout the device, based on its current state. The instruction register (IR) provides additional control signals that are specific to the current instruction. Test data is transmitted serially from TDI through the scan path to TDO. The IR or one of the eight data registers is always selected in the scan path by the TAP control signals issued to the TDO multiplexer.

The 1024-word RAM can be used to store data from the bus being monitored during test operations. The RAM is accessed via the TAP interface when the RAM register (RAMR) is selected in the scan path.

The event-qualification module (EQM) contains two data registers that contain configuration, compare, and mask data associated with on-line test operations. The EQM also contains the state machines for the eight protocols that include various start/stop, start/pause/resume, and do-while algorithms. These protocols operate synchronously to the clock signal generated by the programmable clock interface (PCI). The PCI generates a clock signal from one of 32 different logical combinations of CLK1, CLK2, CLK3, and TCK. The user configures the PCI through the control register (CTLR).

## detailed description (continued)

The test-cell register (TCR) is a data register that performs PSA operations on the data bus or on the contents of RAM. During PSA operations, the TCR is a linear-feedback shift register. The CTLR configures the data masking and controls the feedback for PSA operations. The boundary-scan register (BSR), header register (HR), and bypass register (BR) are data registers that can be serially accessed through the TAP interface.

### instruction register

The 8-bit instruction register (IR) contains the DBM current instruction, which controls all operations of the device. When the IR is placed in the scan path, the IR status word is loaded into the IR and shifted out on TDO when the new instruction is shifted in.

The IR status word contains four status bits. The $\overline{\text{IRERR}}$ status bit is asserted when an opcode that does not exhibit even parity is loaded into the IR. The OVF status bit is asserted when the RAM address counter is incremented past its maximum value of 3FFh (register value given in hexadecimal format, indicated by the letter h following the value). The RUN and EOT status bits pertain to on-line testing and are asserted when a protocol is active (RUN) or the end of the protocol is reached (EOT).

### boundary-scan register

The boundary-scan register (BSR) is a 24-bit register that includes one boundary-scan cell (BSC) for each of the non-JTAG input and output pins of the device, two BSCs for PIO (one for input data and one for output data), and one BSC for the PIO direction signal. The BSR is used to capture the data appearing at the device periphery and to apply test data to the device outputs.

### bypass register

The bypass register (BR) is a 1-bit register required by IEEE Standard 1149.1-1990. It provides an abbreviated scan path through the DBM when the current test operations do not require it to access one of the other data registers.

### control register

The 45-bit control register (CTLR) issues configuration, control, and enable signals to the device. Data shifted into the CTLR configures the data mask and feedback for PSA operations. It also configures the programmable clock interface and selects the test operations to be performed (see test operations).

### event-qualification register 1

Event-qualification register 1 (EQR1) is a 32-bit register that configures the DBM for on-line testing (event-qualified testing). Data shifted into EQR1 selects and controls one of eight event-qualification protocols and configures the event and status signals. The event signal triggers test operations according to the protocol being executed. The status signal is output via EQO. EQR1 also contains the loop counter, which controls the number of times an event-qualification protocol is executed.

### event-qualification register 2

Event-qualification register 2 (EQR2) is used to load the event counter, expected data, and mask data (16-word-deep register files) for event-qualified tests. Depending on the current instruction, it is either 48 or 56 bits in length and can be thought of as three 16-bit data segments and two 4-bit address segments. One 4-bit address segment addresses the event counter, while the other 4-bit address segment addresses the expected data and mask data.

The register files can be accessed using IEEE-Standard-1149.1-1990-compatible instructions or DMA instructions. When using IEEE-Standard-1149.1-1990-compatible instructions, EQR2 is configured as a 56-bit register. The data appearing in the 16-bit data segments is loaded into or out of the addresses specified by the register's two 4-bit address segments.

**event-qualification register 2 (continued)**

During execution of the DMA instructions, EQR2 is configured as a 48-bit register containing only the three 16-bit data segments. Using DMA instructions allows a continuous stream of data to be loaded or unloaded from the register files. After each 48th bit of the data stream has been shifted to or from the register files, the register file addresses are automatically incremented and the first data bit of the next address is shifted.

**header register**

The header register (HR) is an 8-bit register that initiates DMA write operations on the RAM and on the EQR2 register files. When a DMA write instruction is active, the data being shifted from TDI to TDO is compared against the current value of the HR and the DMA write operation begins after a match is found. When the value of the HR is set to 00h, DMA write operations can only be initiated by the TAP and are not initiated by the TDI-to-TDO data flow.

**random-access memory register**

The random-access memory register (RAMR) is used to access the 1024-word RAM. Depending on the current instruction, it is either 16 bits or 26 bits in length and can be thought of as a 16-bit data segment and a 10-bit address segment.

The RAMR can be accessed using IEEE-Standard-1149.1-1990-compatible instructions or DMA instructions. When using the IEEE-Standard-1149.1-1990-compatible instructions, RAMR is configured as a 26-bit register. The data appearing in the 16-bit data segment is loaded into or out of the address specified by the register's 10-bit address.

During execution of the DMA instructions, RAMR is configured as a 16-bit register containing only the 16-bit data segment. Using DMA instructions allows a continuous stream of data to be loaded or unloaded from the register. After each 16th bit of the data stream has been shifted to or from the register, the address is automatically incremented and the first data bit of the next address is shifted.

**test-cell register**

The test-cell register (TCR) is a 16-bit register. It can perform PSA operations on the data inputs or on the contents of RAM. The resulting signature can be scanned out and compared against an expected value. The TCR is also used during test operations to capture the current value of the data bus.

## test operations

The primary function of the DBM is to perform test operations while monitoring a digital bus. The test operations can be initiated by system conditions (on-line mode) or independent of system conditions (off-line mode). The description of each of the system test operations follows.

**sample**

The data at the D inputs is captured in the test-cell register and can be shifted out via TDO for inspection.

**parallel-signature analysis**

A parallel-signature analysis (PSA) is performed on the data appearing at the D inputs. The test-cell register is configured as a linear-feedback shift register that compresses the data into a signature. The user can configure the device to mask data bits from PSA operations and control the feedback of the linear-feedback shift register. When an input is masked, it is ignored and has no effect on the generated signature.

**trace**

The data at the D inputs is stored in the RAM. The RAM address is automatically incremented after each write cycle. The device can be configured to clear the RAM address to 000h at the beginning of test execution. It also can be configured to allow write cycles to continue after the maximum address 3FFh is reached (thus clearing the address to 000h and overwriting data).

### trace/PSA

The trace and PSA operations are executed simultaneously. All the configuration options for the trace and PSA operations are available for trace/PSA.

In the off-line mode, system test operations are performed via the TAP controller. This is done independent of system conditions.

In the on-line mode, the device is configured to perform system test operations that are dependent on system conditions (event-qualified testing) and synchronous to the system clock(s). Eight different event-qualification protocols offer a wide range of test schemes that control when system test operations take place.

An event can be configured as a match between expected data from the register files and data at the D inputs (local event-qualified testing). Mask data bits from the register files allow any combination of bits to be ignored when the compare takes place. The EQI pin can also be configured as an event to trigger system test operations (global event-qualified testing). The device can be configured to output one of several different status signals via EQO. These are used for global event-qualified testing.

The DBM has instructions that enable the user to perform a self-test on the RAM. This is done by filling the RAM with known values and performing a PSA on its contents. Instructions are included to expedite the loading of the RAM with known values, as well as to perform PSA on the contents of the RAM.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .......... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .......... –0.5 V to $V_{CC}$
Output voltage range, $V_O$ (see Note 1) .......... –0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) .......... ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) .......... ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) .......... ±25 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2) .......... 1.1 W
Storage temperature range, $T_{stg}$ .......... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | EQO | | –4 | mA |
| | | PIO, TDO | | –16 | |
| $I_{OL}$ | Low-level output current | EQO | | 4 | mA |
| | | PIO, TDO | | 16 | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | EQO | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | | | | | V |
| | | | $I_{OH}$ = –4 mA | | 3.7 | | | |
| | | $V_{CC}$ = 5.5 V | $I_{OH}$ = –3 mA | | | | | |
| | | | $I_{OH}$ = –4 mA | | 4.7 | | | |
| | PIO, TDO | $V_{CC}$ = 4.5 V | $I_{OH}$ = –11 mA | | | | | |
| | | | $I_{OH}$ = –16 mA | | 3.7 | | | |
| | | $V_{CC}$ = 5.5 V | $I_{OH}$ = –11 mA | | | | | |
| | | | $I_{OH}$ = –16 mA | | 4.7 | | | |
| $V_{OL}$ | EQO | $V_{CC}$ = 4.5 V to 5.5 V | $I_{OL}$ = 3 mA | | | | | V |
| | | | $I_{OL}$ = 4 mA | | | | 0.5 | |
| | PIO, TDO | $V_{CC}$ = 4.5 V to 5.5 V | $I_{OL}$ = 11 mA | | | | | |
| | | | $I_{OL}$ = 16 mA | | | | 0.5 | |
| $I_I$ | CLK, D, EQI, TCK | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | | ±1 | μA |
| | TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | | | | ±1 | |
| | TDI, TMS | $V_{CC}$ = 5.5 V, | $V_I$ = GND | | –0.1 | | –20 | |
| $I_{OZ}$‡ | PIO, TDO | $V_{CC}$ = 5.5 V, | $V_O$ = $V_{CC}$ or GND | | | | ±5 | μA |
| $I_{CC}$ | RAM disabled | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | | | 200 | μA |
| | RAM enabled | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | | | 200 | mA |
| $\Delta I_{CC}$ | | $V_{CC}$ = 5.5 V, Other inputs at $V_{CC}$ or GND | One input at 3.4 V, | | | | 1 | mA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | | | | 4* | | pF |
| $C_{io}$ | | $V_O$ = $V_{CC}$ or GND | | | | 7* | | pF |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | | | | 6* | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† Typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O pins, the parameter $I_{OZ}$ includes the input-leakage current.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{clock}$ | Clock frequency | Any CLK (except during PSARAM instruction)§ | 0 | 50 | MHz |
| | | TCK (except during PSARAM instruction)§ | 0 | 50 | |
| | | Any CLK or TCK (during PSARAM instruction)§ | 0 | 17 | |
| $t_w$ | Pulse duration | Any CLK or TCK high or low | 7 | | ns |
| $t_{su}$ | Setup time | TDI before TCK↑ | 2 | | ns |
| | | TMS before TCK↑ | 4 | | |
| | | Any D before any CLK or TCK | 5 | | |
| | | EQI before any CLK or TCK | 4 | | |
| | | PIO before any CLK or TCK | 1 | | |
| $t_h$ | Hold time | TDI after TCK↑ | 5 | | ns |
| | | TMS after TCK↑ | 3 | | |
| | | Any D after any CLK or TCK | 3 | | |
| | | EQI after any CLK or TCK | 2 | | |
| | | PIO after any CLK or TCK | 5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 100 | | ns |

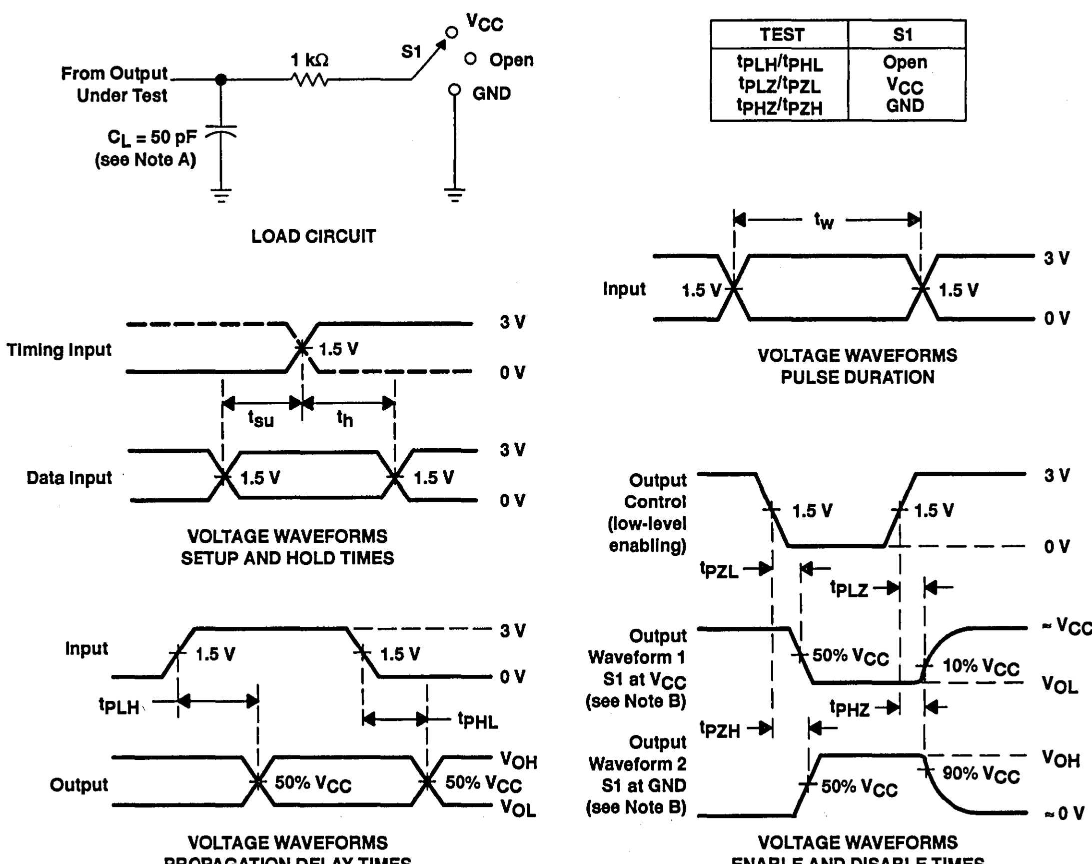
§ The PSARAM instruction performs a parallel-signature analysis on the contents of RAM. This instruction is provided to allow self-test of the RAM.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{max}$ | Any CLK (except during PSARAM instruction)† | | 50 | | MHz |
| | TCK (except during PSARAM instruction)† | | 50 | | |
| | Any CLK or TCK (during PSARAM instruction)† | | 17 | | |
| $t_{PLH}$ | Any CLK | EQO | 7 | 18 | ns |
| $t_{PHL}$ | | | 7 | 17 | |
| $t_{PLH}$ | Any CLK | PIO | 9 | 22 | ns |
| $t_{PHL}$ | | | 9 | 22 | |
| $t_{PLH}$ | Any CLK | TDO | 9 | 20 | ns |
| $t_{PHL}$ | | | 8 | 19 | |
| $t_{PLH}$ | Any D | EQO | 5 | 17 | ns |
| $t_{PHL}$ | | | 4 | 15 | |
| $t_{PLH}$ | TCK↓ | EQO | 5 | 16 | ns |
| $t_{PHL}$ | | | 5 | 15 | |
| $t_{PLH}$ | TCK↓ | PIO | 8 | 19 | ns |
| $t_{PHL}$ | | | 8 | 19 | |
| $t_{PLH}$ | TCK↓ | TDO | 3 | 12 | ns |
| $t_{PHL}$ | | | 3 | 11 | |
| $t_{PZH}$ | TCK↓ | PIO | 5 | 18 | ns |
| $t_{PZL}$ | | | 5 | 18 | |
| $t_{PZH}$ | TCK↓ | TDO | 3 | 11 | ns |
| $t_{PZL}$ | | | 2 | 10 | |
| $t_{PHZ}$ | TCK↓ | PIO | 6 | 16 | ns |
| $t_{PLZ}$ | | | 5 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | 9 | 16 | ns |
| $t_{PLZ}$ | | | 8 | 15 | |

† The PSARAM instruction performs a parallel-signature analysis on the contents of RAM. This instruction is provided to allow self test of the RAM.

## PARAMETER MEASUREMENT INFORMATION




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

NOTES: A. $C_L$ includes probe and jig capacitance.

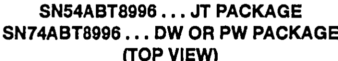
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

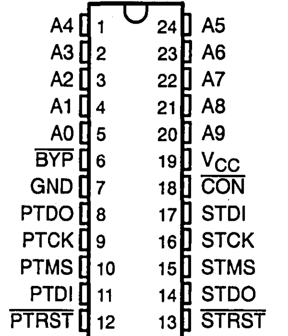
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.

D. The outputs are measured one at a time with one transition per measurement.

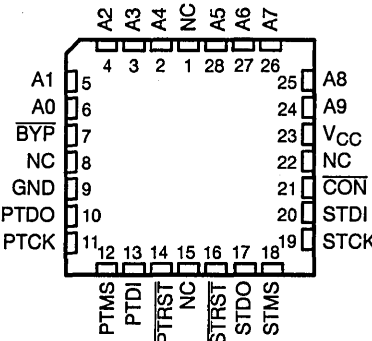
**Figure 1. Load Circuit and Voltage Waveforms**

- **Members of Texas Instruments Broad Family of Testability Products Supporting IEEE Std 1149.1-1990 (JTAG) Test Access Port (TAP) and Boundary-Scan Architecture**
- **Extend Scan Access From Board Level to Higher Levels of System Integration**
- **Promote Reuse of Lower-Level (Chip/Board) Tests in System Environment**
- **Switch-Based Architecture Allows Direct Connect of Primary TAP to Secondary TAP**
- **Primary TAP Is Multidrop for Minimal Use of Backplane Wiring Channels**
- **Simple Addressing (Shadow) Protocol Is Received/Acknowledged on Primary TAP**
- **Shadow Protocols Can Occur in Any of Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR TAP States to Provide for Board-to-Board Test and Built-In Self Test**
- **10-Bit Address Space Provides for up to 1021 User-Specified Board Addresses**
- **Bypass (BYP) Pin Forces Primary-to-Secondary Connection Without Use of Shadow Protocols**
- **Connect (CON) Pin Provides Indication of Primary-to-Secondary Connection**
- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$) Support Backplane Interface at Primary and High Fanout at Secondary**
- **Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (JT)**




**SN54ABT8996 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'ABT8996 10-bit addressable scan ports (ASP) are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit assemblies. Unlike most SCOPE™ devices, the ASP is not a boundary-scannable device, rather, it applies TI's addressable-shadow-port technology to the IEEE Standard 1149.1-1990 (JTAG) test access port (TAP) to extend scan access beyond the board level.

Conceptually, the ASP is a simple switch that can be used to directly connect a set of multidrop primary TAP signals to a set of secondary TAP signals – for example, to interface backplane TAP signals to a board-level TAP. The ASP provides all signal buffering that might be required at these two interfaces. When primary and secondary TAPs are connected, only a moderate propagation delay is introduced – no storage/retiming elements are inserted. This minimizes the need for reformatting board-level test vectors for in-system use.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## description (continued)

Most operations of the ASP are synchronous to the primary test clock (PTCK) input. This PTCK signal is always buffered directly onto the secondary test clock (STCK) output.

Upon power up of the device, the ASP assumes a condition in which the primary TAP is disconnected from the secondary TAP (unless the bypass signal is used, as below). This reset condition also can be entered by the assertion of the primary test reset ($\overline{PTRST}$) input or by use of shadow protocol. The $\overline{PTRST}$ signal is always buffered directly onto the secondary test reset ($\overline{STRST}$) output, ensuring that the ASP and its associated secondary TAP can be reset simultaneously.

When connected, the primary test data input (PTDI) and primary test mode select (PTMS) input are buffered onto the secondary test data output (STDO) and secondary test mode select (STMS) output, respectively, while the secondary test data input (STDI) is buffered onto the primary test data output (PTDO). When disconnected, STDO is at high impedance, while PTDO is at high impedance, except during acknowledgement of a shadow protocol. Upon disconnect of the secondary TAP, STMS holds its last low or high level, allowing the secondary TAP to be held in its last stable state. Upon reset of the ASP, STMS is high, allowing the secondary TAP to be synchronously reset to the Test-Logic-Reset state.

In system, primary-to-secondary connection is based on shadow protocols that are received and acknowledged on PTDI and PTDO, respectively. These protocols can occur in any of the stable TAP states other than Shift-DR or Shift-IR (i.e., Test-Logic-Reset, Run-Test/Idle, Pause-DR or Pause-IR). The essential nature of the protocols is to receive/transmit an address via a serial bit-pair signaling scheme. When an address is received serially at PTDI that matches that at the parallel address inputs (A9–A0), the ASP serially retransmits its address at PTDO as an acknowledgement and then assumes the connected (ON) status, as above. If the received address does not match that at the address inputs, the ASP immediately assumes the disconnected (OFF) status without acknowledgement.

The ASP also supports three dedicated addresses that can be received globally (that is, to which all ASPs respond) during shadow protocols. Receipt of the dedicated disconnect address (DSA) causes the ASP to disconnect in the same fashion as a non-matching address. Reservation of this address for global use ensures that at least one address is available to disconnect all receiving ASPs. The DSA is especially useful when the secondary TAPs of multiple ASPs are to be left in different stable states. Receipt of the reset address (RSA) causes the ASP to assume the reset condition, as above. Receipt of the test-synchronization address (TSA) causes the ASP to assume a connect status (MULTICAST) in which PTDO is at high impedance but the connections from PTMS to STMS and PTDI to STDO are maintained to allow simultaneous operation of the secondary TAPs of multiple ASPs. This is useful for multicast TAP-state movement, simultaneous test operation (such as in Run-Test/Idle state), and scanning of common test data into multiple like scan chains. The TSA is valid only when received in the Pause-DR or Pause-IR TAP states.

Alternatively, primary-to-secondary connection can be selected by assertion of a low level at the bypass ($\overline{BYP}$) input. This operation is asynchronous to PTCK and is independent of $\overline{PTRST}$ and/or power-up reset. This bypassing feature is especially useful in the board-test environment, since it allows the board-level automated test equipment (ATE) to treat the ASP as a simple transceiver. When the $\overline{BYP}$ input is high, the ASP is free to respond to shadow protocols. Otherwise, when $\overline{BYP}$ is low, shadow protocols are ignored.

Whether the connected status is achieved by use of shadow protocol or by use of $\overline{BYP}$, this status is indicated by a low level at the connect ($\overline{CON}$) output. Likewise, when the secondary TAP is disconnected from the primary TAP, the $\overline{CON}$ output is high.

The SN54ABT8996 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8996 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | SHADOW-PROTOCOL RESULT† | OUTPUTS | | | | | | PRIMARY-TO-SECONDARY CONNECT STATUS |
|---|---|---|---|---|---|---|---|---|---|
| BYP | PTRST | | STRST | STCK | STMS | STDO | PTDO | CON | |
| L | L | — | L | PTCK | H‡ | PTDI | STDI | L | BYP/TRST‡ |
| L | H | — | H | PTCK | PTMS | PTDI | STDI | L | BYP |
| H | L | — | L | PTCK | H | Z | Z | H | TRST |
| H | H | RESET | H | PTCK | H | Z | Z | H | RESET |
| H | H | MATCH | H | PTCK | PTMS | PTDI | STDI | L | ON |
| H | H | NO MATCH | H | PTCK | $STMS_0$§ | Z | Z | H | OFF |
| H | H | HARD ERROR¶ | H | PTCK | $STMS_0$§ | Z | Z | H | OFF |
| H | H | DISCONNECT | H | PTCK | $STMS_0$§ | Z | Z | H | OFF |
| H | H | TEST SYNCHRONIZATION | H | PTCK | PTMS | PTDI | Z | L | MULTICAST |

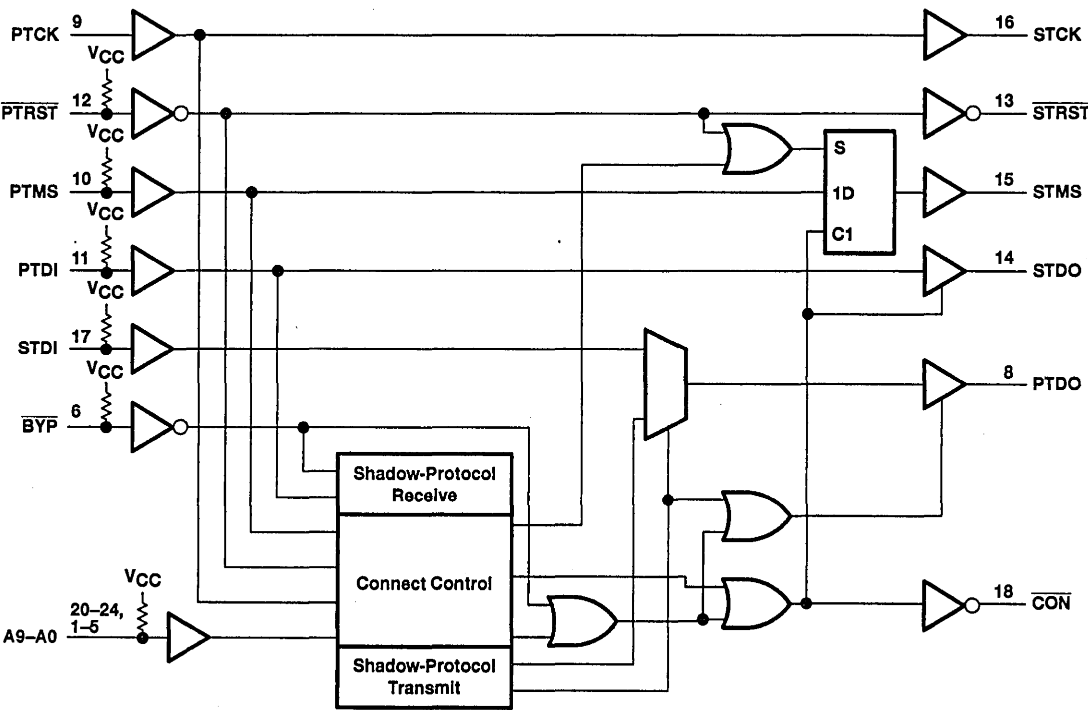
† Shadow protocols are received serially via PTCK and PTDI and acknowledged serially via PTCK and PTDO under certain conditions in which PTMS is static low or static high (see shadow protocol). The result shown here follows any required acknowledgement.

‡ In normal operation of IEEE Std 1149.1-compliant architectures, it is recommended that TMS be high prior to release of TRST. The BYP/TRST connect status ensures that this condition is met at STMS regardless of the applied PTMS. Also, it is recommended that STMS be kept high for a minimum duration of 5 PTCK cycles following assertion of PTRST, either by maintaining PTRST low or by setting PTMS high. This ensures that ICs both with and without TRST inputs are moved to their Test-Logic-Reset TAP states. It is expected that in normal application, this condition will only occur when BYP is fixed at the low state. In such case, upon release of PTRST, the ASP immediately resumes the BYP connect status.

§ STMS level before indicated steady-state conditions were established

¶ The shadow protocol is well defined. Some variations in the protocol are tolerated (see protocol errors). Those that are not tolerated are considered hard errors and cause disconnect as indicated.

## functional block diagram




Pin numbers shown are for the DW, JT, and PW packages.

## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| A9–A0 | Address inputs. The ASP compares addresses received via shadow protocol against the value at A9–A0 to determine address match. The bit order is from most significant to least significant. An internal pullup at each A9–A0 terminal forces the terminal to a high level if it has no external connection. |
| $\overline{\text{BYP}}$ | Bypass input. A low input at $\overline{\text{BYP}}$ forces the ASP into BYP or BYP/TRST status, depending on $\overline{\text{PTRST}}$ being high or low, respectively. While $\overline{\text{BYP}}$ is low, shadow protocols are ignored. Otherwise, while $\overline{\text{BYP}}$ is high, the ASP is free to respond to shadow protocols. An internal pullup forces $\overline{\text{BYP}}$ to a high level if it has no external connection. |
| $\overline{\text{CON}}$ | Connect indicator (output). The ASP indicates secondary-scan-port activity (resulting from BYP, BYP/TRST, MULTICAST, or ON status) by forcing $\overline{\text{CON}}$ to be low. Inactivity (resulting from OFF, RESET, or TRST status) is indicated when $\overline{\text{CON}}$ is high. |
| GND | Ground |
| PTCK | Primary test clock. PTCK receives the TCK signal required by IEEE Standard 1149.1-1990. The ASP always buffers PTCK to STCK. Shadow protocols are received/acknowledged synchronously to PTCK and connect-status changes invoked by shadow protocol are made synchronously to PTCK. |
| PTDI | Primary test data input. PTDI receives the TDI signal required by IEEE Standard 1149.1-1990. During appropriate TAP states, the ASP monitors PTDI for shadow protocols. During shadow protocols, data at PTDI is captured on the rising edge of PTCK. When a valid shadow protocol is received in this fashion, the ASP compares the received address against the A9–A0 inputs. If the ASP detects a match, it outputs an acknowledgement and then connects its primary TAP terminals to its secondary TAP terminals. Under BYP, BYP/TRST, MULTICAST or ON status, the ASP buffers the PTDI signal to STDO. An internal pullup forces PTDI to a high level if it has no external connection. |
| PTDO | Primary test data output. PTDO transmits the TDO signal required by IEEE Standard 1149.1-1990. During shadow protocols, the ASP transmits any required acknowledgement via the PTDO. The acknowledgement data output at PTDO changes on the falling edge of PTCK. Under BYP, BYP/TRST, or ON status, the ASP buffers the PTDO signal from STDI. Under OFF, MULTICAST, RESET, or TRST status, PTDO is at high impedance. |
| PTMS | Primary test mode select. PTMS receives the TMS signal required by IEEE Standard 1149.1-1990. The ASP monitors the PTMS to determine the TAP-controller state. During stable TAP states other than Shift-DR or Shift-IR (i.e., Test-Logic-Reset, Run-Test-Idle, Pause-DR, Pause-IR) the ASP can respond to shadow protocols. Under BYP, MULTICAST, or ON status, the ASP buffers the PTMS signal to STMS. An internal pullup forces PTMS to a high level if it has no external connection. |
| $\overline{\text{PTRST}}$ | Primary test reset. $\overline{\text{PTRST}}$ receives the $\overline{\text{TRST}}$ signal allowed by IEEE Standard 1149.1-1990. The ASP always buffers $\overline{\text{PTRST}}$ to $\overline{\text{STRST}}$. A low input at $\overline{\text{PTRST}}$ forces the ASP to assume TRST or BYP/TRST status, depending on $\overline{\text{BYP}}$ being high or low, respectively. Such operation also asynchronously resets the internal ASP state to its power-up condition. Otherwise, while $\overline{\text{PTRST}}$ is high, the ASP is free to respond to shadow protocols. An internal pullup forces $\overline{\text{PTRST}}$ to a high level if it has no external connection. |
| STCK | Secondary test clock. STCK retransmits the TCK signal required by IEEE Standard 1149.1-1990. The ASP always buffers STCK from PTCK. |
| STDI | Secondary test data input. STDI receives the TDI signal required by IEEE Standard 1149.1-1990. Under BYP, BYP/TRST, or ON status, the ASP buffers STDI to PTDO. An internal pullup forces STDI to a high level if it has no external connection. |
| STDO | Secondary test data output. STDO transmits the TDO signal required by IEEE Standard 1149.1-1990. Under BYP, BYP/TRST, MULTICAST, or ON status, the ASP buffers STDO from PTDI. Under OFF, RESET, or TRST status, STDO is at high impedance. |
| STMS | Secondary test mode select. STMS retransmits the TMS signal required by IEEE Standard 1149.1-1990. Under BYP, MULTICAST, or ON status, the ASP buffers STMS from PTMS. When disconnected (as a result of OFF status), STMS maintains its last valid state until the ASP assumes BYP/TRST, RESET, or TRST status (upon which it is forced high) or the ASP again assumes BYP, MULTICAST, or ON status. |
| $\overline{\text{STRST}}$ | Secondary test reset. $\overline{\text{STRST}}$ retransmits the $\overline{\text{TRST}}$ signal allowed by IEEE Standard 1149.1-1990. The ASP always buffers $\overline{\text{STRST}}$ from $\overline{\text{PTRST}}$. |
| $V_{CC}$ | Supply voltage |

## application information

In application, the ASP is used at each of several (serially-chained) groups of IEEE Std 1149.1-compliant devices. The ASP for each such group is assigned an address (via inputs A9–A0) that is unique from that assigned to ASPs for the remaining groups. Each ASP is wired at its primary TAP to common (multidrop) TAP signals (sourced from a central IEEE Std 1149.1 bus master) and fans out its secondary TAP signals to the specific group of IEEE Std 1149.1-compliant devices with which it is associated. An example is shown in Figure 1.

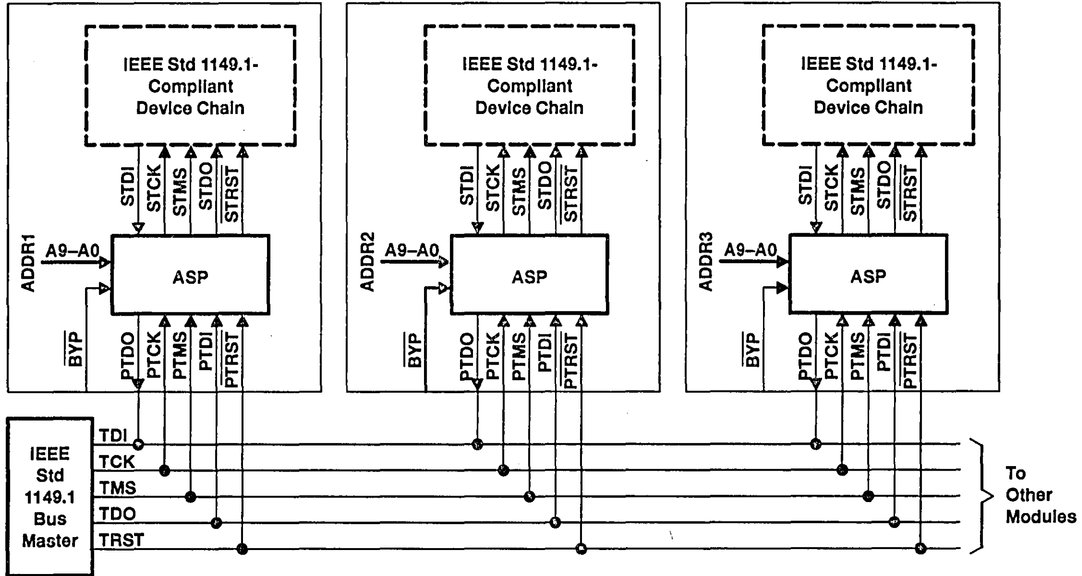



**Figure 1. ASP Application**

This application allows the ASP to be wired to a 4- or 5-wire multidrop test access bus, such as might be found on a backplane. Each ASP would then be located on a module, for example a printed-circuit board (PCB), which contains a serial chain of IEEE Std 1149.1-compliant devices and which would plug into the module-to-module bus (e.g., backplane). In the complete system, the ASP shadow protocols would allow the selection of the scan chain on a single module. The selected scan chain could then be controlled, via the multidrop TAP, as if it were the only scan chain in the system. Normal IR and DR scans can then be performed to accomplish the module test objectives.

Once scan operations to a given module are complete, another module can be selected in the same fashion, at which time the ASP-based connection to the first module is dissolved. This procedure can be continued progressively for each module to be tested. Finally, one of two global addresses can be issued to either leave all modules unselected (disconnect address, DSA) or to deselect and reset scan chains for all modules (reset address, RSA).

Additionally, in Pause-DR and Pause-IR TAP states, a third global address (test-synchronization address, TSA) can be invoked to allow simultaneous TAP-state changes and multicast scan-in operations to selected modules. This is especially useful in the former case, for allowing selected modules to be moved simultaneously to the Run-Test-Idle TAP state for module-level or module-to-module built-in self-test (BIST) functions, which operate synchronously to TCK in that TAP state, and in the latter case, for scanning common test setup/data into multiple like modules.

## architecture

Conceptually, the ASP can be viewed as a bank of switches that can connect or isolate a module-level TAP to/from a higher-level (e.g., module-to-module) TAP. This is shown in Figure 2. The state of the switches (open versus closed) is based on shadow protocols, which are received on PTDI and are synchronous to PTCK.

The simple architecture of the ASP allows the system designer to overcome the limitations of IEEE Std 1149.1 *ring* and *star* configurations. Ring configurations (in which each module's TDO is chained to the next module's TDI) are of limited use in backplane environments, since removal of a module breaks the scan chain and prevents test of the remainder of the system. Star configurations (in which all module TDOs and TDIs are connected in parallel) are suited to the backplane environment, but, since each module must receive its own TMS, are costly in terms of backplane routing channels. By comparison, use of the ASP allows all five IEEE Std 1149.1 signals to be routed in multidrop fashion.

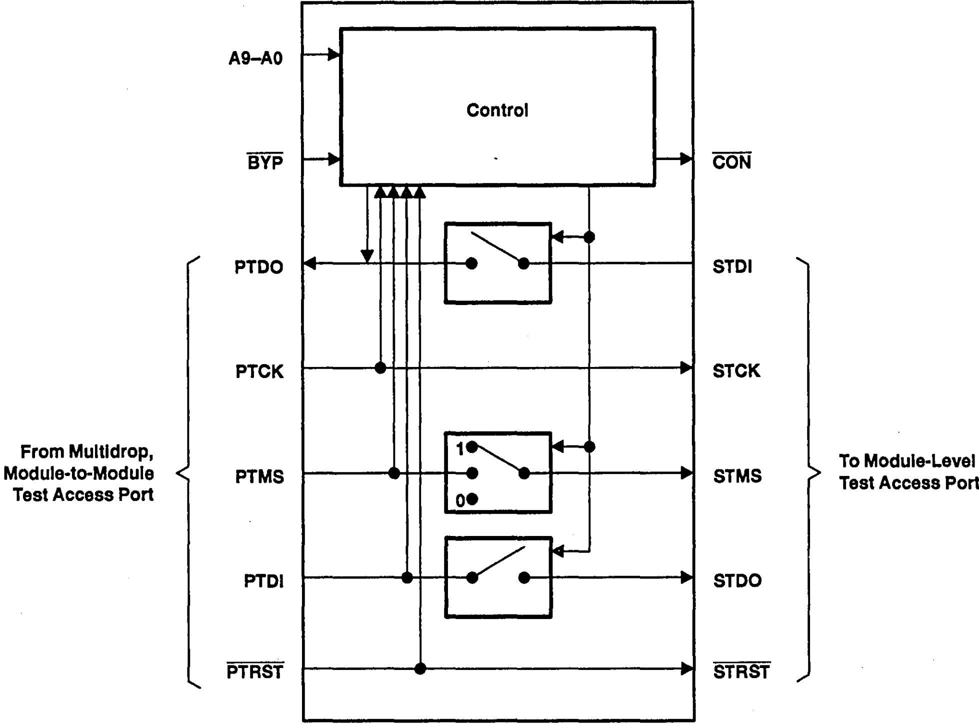



**Figure 2. ASP Conceptual Model**

As shown in the functional block diagram, the ASP comprises three major logic blocks. Blocks for shadow-protocol receive and shadow-protocol transmit are responsible for receipt of select protocol and transmission of acknowledge protocol, respectively. The connect-control block is responsible for TAP-state monitor and address matching.

Some additional logic is illustrated outside of these major blocks. This additional logic is responsible for controlling the activity of the ASP outputs based on the shadow-protocol result and/or protocol bypass [as selected by an active (low) $\overline{\text{BYP}}$ input].

## shadow protocol

Addressing of an ASP in system is accomplished by shadow protocols, which are received at PTDI synchronously to PTCK. Shadow protocols can occur only in the following stable TAP states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR. Shadow protocols never occur in Shift-DR or Shift-IR states in order to prevent contention on the signal bus to which PTDO is wired. Additionally, the ASP PTMS must be held at a constant low or high level throughout a shadow protocol. If TAP-state changes occur in the midst of a shadow protocol, the shadow protocol is aborted and the select-protocol state machine returns to its initial state.

The shadow protocol is based on a serial bit-pair signaling scheme in which two bit-pair combinations (data one, data zero) are used to represent address data and the other two bit-pair combinations (select, idle) are used for framing – that is, to indicate where address data begins and ends.

These bit pairs are received serially at PTDI (or transmitted serially at PTDO) synchronously to PTCK as follows:

- The idle bit pair (I) is represented as two consecutive high signals.
- The select bit pair (S) is represented as two consecutive low signals.
- The data-one bit pair (D) is represented as a low signal followed by a high signal.
- The data-zero bit pair (D) is represented as a high signal followed by a low signal.

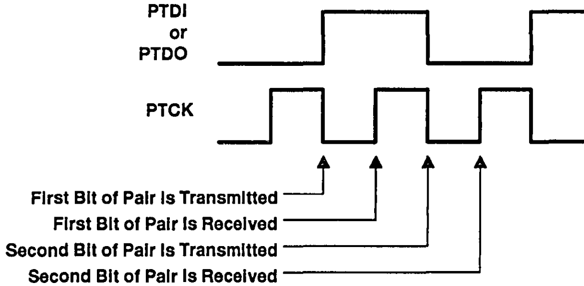



**Figure 3. Bit-Pair Timing (Data Zero Shown)**

A complete shadow protocol is composed of the receipt of a select protocol followed, if applicable, by the transmission of an acknowledge protocol (which is issued from PTDO only if the received address matches that at the A9–A0 inputs). Both of these subprotocols are composed of ten data bit pairs framed at the beginning by idle and select bit pairs and at the end by select and idle bit pairs. This is represented in an abbreviated fashion as follows: ISDDDDDDDDDDSI. Figure 4 shows a complete shadow protocol (the symbol T is used to represent a high-impedance condition on the associated signal line – since the high-impedance state at PTDI is logically high due to pullup, it maps onto the idle bit pair).

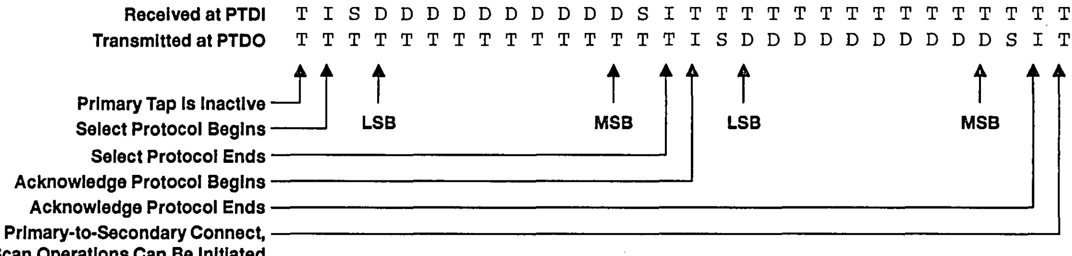



**Figure 4. Complete Shadow Protocol**

### select protocol

The select protocol is the ASP's means of receiving (at PTDI) address information from an IEEE Std 1149.1 bus master. It follows the ISDDDDDDDDDDSI sequence described previously. A 10-bit address value is decoded from the received data-one and/or data-zero bit pairs. These bit pairs are interpreted in least-significant-bit-first order (that is, the first data bit pair received is considered to correspond to A0).

### acknowledge protocol

Following the receipt of a complete select-protocol sequence, the protocol result provisionally is set to NO MATCH and the connect status set to OFF. The received address is then compared to that at the ASP address inputs (A9–A0). If these address values match, the ASP immediately (with no delay) responds with an acknowledge protocol transmitted from PTDO. This protocol follows the ISDDDDDDDDDDSI sequence described previously. The transmitted address represents the address of the selected ASP which, by definition, is the same address the ASP received in the select protocol. The 10-bit address value is encoded into data-one and/or data-zero bit pairs. The bit pairs are to be interpreted in least-significant-bit-first order (that is, the first data bit pair transmitted is to be considered to correspond to A0). If the received address does not match that at the A9–A0 inputs, no acknowledge protocol is transmitted and the shadow protocol is considered complete.

### protocol errors

Protocol errors occur when bit pairs are received out of sequence. Some of these sequencing errors can be tolerated and are termed *soft* errors. No specific action occurs as the result of a soft error. Other errors represent cases where the addressing information could be incorrectly received and are termed *hard* errors. Hard errors are characterized by sequences in which at least one bit of address data has been properly transmitted followed by a sequencing error. When a hard error occurs, any connection to an ASP is dissolved.

Table 1 lists the bit-pair sequences that result in soft errors and hard errors. A hard error also results when the primary TAP state changes during select protocol following the proper transmission of at least one bit of address data. Figures 16 and 17 show shadow-protocol timing in case of protocol hard error while Figure 18 shows shadow-protocol timing in case of protocol soft error.

**Table 1. Shadow-Protocol Errors†**

| SOFT ERRORS | HARD ERRORS |
|---|---|
| I(D)I<br>I(D)(S)I<br>I(D)(S)(D)I<br>I(S)I<br>IS(S)(D)I<br>IS(S)(D)(S)I | IS(D)I<br>IS(D)S(D)I<br>IS(D)S(S)I |

† A bit-pair token in parentheses represents one or more instances.

### long address

Receipt of an address longer than ten bits is considered a hard error and the ASP assumes OFF status. The sole exceptions are when all data ones are received or all data zeros are received. In these special cases, the global addresses represented by these bit sequences are observed and appropriate action taken. That is, in the case that only data ones (ten or more) are received, the shadow-protocol result is TEST SYNCHRONIZATION (if the primary TAP state is Pause-DR or Pause-IR), and in the case that only data zeros (ten or more) are received, the shadow-protocol result is RESET (see test-synchronization address and reset address).

### short address

In all cases, receipt of an address shorter than ten bits is considered a hard error and the ASP assumes OFF status.

## connect control

The connect-control block monitors the primary TAP state to enable receipt/acknowledge of shadow protocols in appropriate states (namely, the stable, non-Shift TAP states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR). Upon receipt of a valid shadow protocol, this block performs the address matching required to compute the shadow-protocol result.

## TAP-state monitor

The TAP-state monitor is a synchronous finite-state machine that monitors the primary TAP state. The state diagram is shown in Figure 5 and mirrors that specified by IEEE Standard 1149.1-1990. The TAP-state monitor proceeds through its states based on the level of PTMS at the rising edge of PTCK. Each state is described both in terms of its significance for ASP devices and for connected IEEE Std 1149.1-compliant devices (called targets). However, the monitor state (primary TAP) can be different from that of disconnected scan chains (secondary TAP).

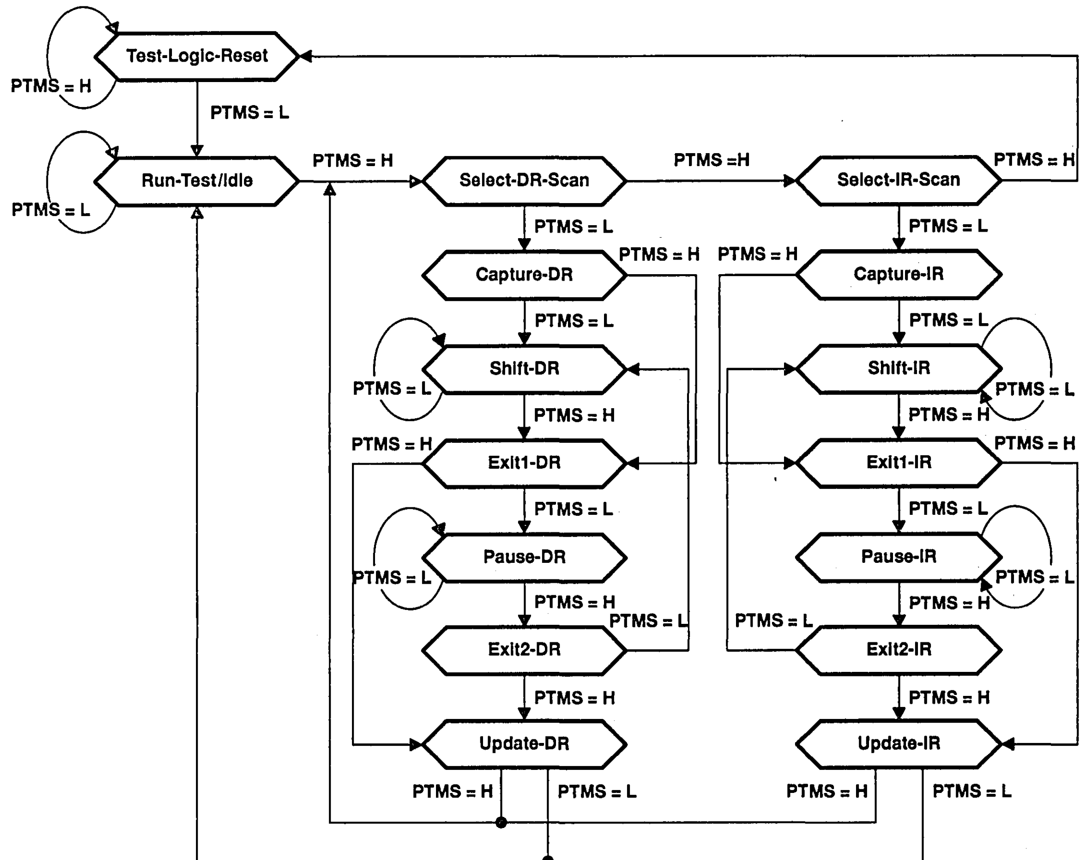



**Figure 5. TAP-Monitor State Diagram**

**Test-Logic-Reset**

The ASP TAP-state monitor powers up in the Test-Logic-Reset state. Alternatively, the ASP can be forced asynchronously to this state by assertion of its $\overline{\text{PTRST}}$ input. In the stable Test-Logic-Reset state, the ASP is enabled to receive and respond to shadow protocols. The ASP does not recognize the TSA in this state.

For a target device in the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

**Run-Test/Idle**

In the stable Run-Test/Idle state, the ASP is enabled to receive and respond to shadow protocols. The ASP does not recognize the TSA in this state.

For a target device, Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

**Select-DR-Scan, Select-IR-Scan**

The ASP is not enabled to receive and respond to shadow protocols in the Select-DR-Scan and Select-IR-Scan states.

For a target device, no specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

**Capture-DR**

The ASP is not enabled to receive and respond to shadow protocols in the Capture-DR state.

For a target device in the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the Capture-DR state is exited.

**Shift-DR**

The ASP is not enabled to receive and respond to shadow protocols in the Shift-DR state.

For a target device, upon entry to the Shift-DR state, the selected data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the selected data register. While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle.

**Exit1-DR, Exit2-DR**

The ASP is not enabled to receive and respond to shadow protocols in the Exit1-DR and Exit2-DR states.

For a target device, the Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

In the stable Pause-DR state, the ASP is enabled to receive and respond to shadow protocols. Additionally, the TSA can be recognized in this state.

For target devices, no specific function is performed in the stable Pause-DR state. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

The ASP is not enabled to receive and respond to shadow protocols in the Update-DR state.

For a target device, if the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK following entry to the Update-DR state.

### Capture-IR

The ASP is not enabled to receive and respond to shadow protocols in the Capture-IR state.

For a target device in the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the Capture-IR state is exited.

### Shift-IR

The ASP is not enabled to receive and respond to shadow protocols in the Shift-IR state.

For a target device, upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the instruction register. While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle.

### Exit1-IR, Exit2-IR

The ASP is not enabled to receive and respond to shadow protocols in the Exit1-IR and Exit2-IR states.

For target devices, the Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

In the stable Pause-IR state, the ASP is enabled to receive and respond to shadow protocols. Additionally, the TSA can be recognized in this state.

For target devices, no specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The ASP is not enabled to receive and respond to shadow protocols in the Update-IR state.

For target devices, the current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

### address matching

Connect status of the ASP is computed by a match of the address received in the last valid shadow protocol against that at the address inputs (A9–A0) as well as against the three dedicated addresses that are internal to the ASP (DSA, RSA, and TSA). The address map is shown in Table 2.

**Table 2. Address Map**

| ADDRESS NAME | BINARY CODE | HEX CODE | SHADOW-PROTOCOL RESULT | RESULTANT PRIMARY-TO-SECONDARY CONNECT STATUS |
|---|---|---|---|---|
| Reset Address (RSA) | 0000000000 | 000 | RESET | RESET |
| Matching Address | A9–A0 | A9–A0 | MATCH | ON |
| Disconnect Address (DSA) | 1111111110 | 3FE | DISCONNECT | OFF |
| Test Synchronization Address (TSA) | 1111111111 | 3FF | TEST SYNCHRONIZATION | MULTICAST |
| All Other Addresses | All others | All others | NO MATCH | OFF |

If the shadow-protocol address matches the address inputs (A9–A0), then the ASP responds by transmitting an acknowledge protocol. Following the complete transmission of the acknowledge protocol, the ASP assumes ON status (in which PTDI, PTDO, and PTMS are connected to STDO, STDI, and STMS, respectively). The ON status allows the scan chain associated with the ASP's secondary TAP to be controlled from the multidrop primary TAP as if it were directly wired as such. Figures 6 and 7 show the shadow-protocol timing for MATCH result when the prior ASP connect status is ON and OFF, respectively.

If the shadow-protocol address does not match the address inputs (A9–A0), then (unless the address is one of the three dedicated global addresses described below) the ASP responds immediately by assuming the OFF status (in which PTDO and STDO are high impedance and STMS is held at its last level). This has the effect of deselecting the scan chain associated with the ASP secondary TAP, but leaves the TAP state of the scan chain unchanged. No acknowledge protocol is sent. Figures 8 and 9 show the shadow-protocol timing for NO MATCH result when the prior ASP connect status is ON and OFF, respectively.

### disconnect address

The disconnect address (DSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the DSA, it immediately responds by assuming the OFF status (in which PTDO and STDO are high impedance and STMS is held at its last level). This has the effect of deselecting the scan chain associated with the ASP secondary TAP, but leaves the TAP state of the scan chain unchanged. No acknowledge protocol is sent. Figures 10 and 11 show the shadow-protocol timing for DISCONNECT result when the prior ASP connect status is ON and OFF, respectively.

The same result occurs when a non-matching address is received. No specific action to disconnect an ASP is required, as a given ASP is disconnected by the address that connects another. The dedicated DSA ensures that at least one address is available for the purpose of disconnecting all receiving ASPs. It is especially useful when the currently selected scan chain is in a different TAP state than that to be selected. In such a case, the DSA is used to leave the former scan chain in the proper state, after which the primary TAP state is moved to that needed to select the latter scan chain.

### reset address

The reset address (RSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the RSA, it immediately responds by assuming the RESET status (in which PTDO and STDO are high impedance and STMS is forced to the high level). This has the effect of deselecting and resetting (to Test-Logic-Reset state) the scan chain associated with the ASP secondary TAP. No acknowledge protocol is sent. Figures 12 and 13 show the shadow-protocol timing for RESET result when the prior ASP connect status is ON and OFF, respectively.

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### test synchronization address

The test synchronization address (TSA) is one of the three internally dedicated addresses that are recognized globally. When an ASP receives the TSA while its secondary TAP state is Pause-DR or Pause-IR, it immediately responds by assuming the MULTICAST status (in which PTDI and PTMS are connected to STDO and STMS respectively, while PTDO is high impedance). No acknowledge protocol is sent. The TSA is valid only when the TAP state of both primary and secondary is Pause-DR or Pause-IR. If the TSA is received when the TAP state of either primary or secondary is Test-Logic-Reset or Run-Test-Idle, the shadow-protocol result is considered to be DISCONNECT. Figures 14 and 15 show the shadow-protocol timing for TEST SYNCHRONIZATION result when the prior ASP connect status is ON and OFF, respectively.

The TSA allows simultaneous operation of the scan chains of all selected ASPs, either for global TAP-state movement or for scan input of common serial test data via PTDI. This is especially useful in the former case, to simultaneously move such scan chains into the Run-Test/Idle state in which module-level or module-to-module BIST operations can operate synchronous to TCK in that TAP state, and in the later case, to scan common test setup/data into multiple like modules.

### protocol bypass

Protocol bypass is selected by a low $\overline{BYP}$ input. This protocol-bypass mode forces the ASP into BYP status (primary TAP signals are connected to secondary TAP signals) regardless of previous shadow-protocol results. The $\overline{CON}$ output is made active (low). Receipt of shadow protocols is disabled.

When $\overline{BYP}$ is taken low, the primary TAP serial data signals (PTDI, PTDO) are immediately (asynchronously to PTCK) connected to their respective secondary TAP signals (STDO, STDI). The primary TAP mode-select signal (PTMS) is also connected to its respective secondary TAP signal (STMS) unless $\overline{PTRST}$ is low, in which case STMS remains high until $\overline{PTRST}$ is released. Also, the shadow-protocol-receive block is reset to its power-up state and is held in this state such that select protocols appearing at the primary TAP are ignored.

When the $\overline{BYP}$ input is released (taken high), the ASP immediately (asynchronously to PTCK) resumes the connect status selected by the last valid shadow protocol. The shadow-protocol-receive block is again enabled to respond to select protocols.

Figures 19 and 20 show protocol-bypass timing when the ASP connect status before $\overline{BYP}$ active is ON and OFF, respectively.

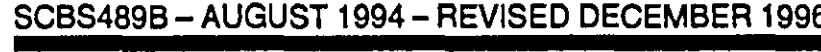
### asynchronous reset

While the $\overline{PTRST}$ input is always buffered directly to the $\overline{STRST}$ output, it also serves as an asynchronous reset for the ASP. Given that $\overline{BYP}$ is high, when $\overline{PTRST}$ goes low, the ASP immediately assumes TRST status in which $\overline{CON}$ is high and PTDO and STDO are at high impedance. Otherwise, if $\overline{BYP}$ is low, the ASP assumes BYP/TRST status. In either case, STMS is set high so that connected IEEE Std 1149.1-compliant devices can be synchronously driven to their Test-Logic-Reset states. While $\overline{PTRST}$ is low, receipt of shadow protocols is disabled.

Figures 21 and 22 show asynchronous reset timing when the ASP connect status before $\overline{PTRST}$ active is ON and OFF, respectively. Figure 23 shows asynchronous reset timing when $\overline{BYP}$ is low.

### connect indicator

The $\overline{CON}$ output indicates secondary-scan-port activity (STDO, STMS active) regardless of whether such activity is achieved via protocol bypass or shadow protocol. If the $\overline{BYP}$ input is low, the $\overline{CON}$ output is low. Otherwise, if the $\overline{BYP}$ input is high, the $\overline{CON}$ output is low if the result of the last valid shadow protocol is MATCH or TEST SYNCHRONIZATION. In all other cases, and while acknowledge protocol is in progress, the $\overline{CON}$ output is high.



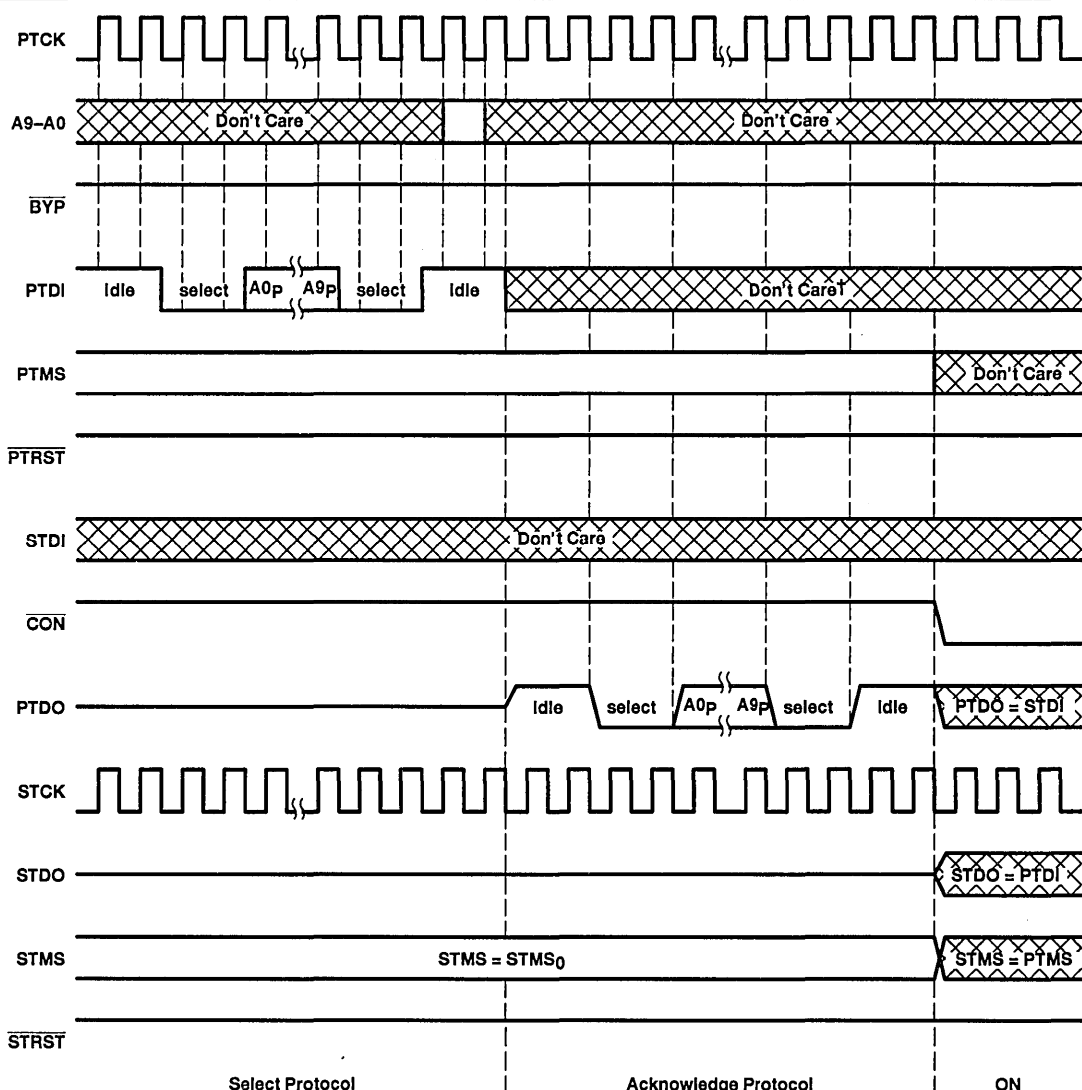
## shadow-protocol timing

PTCK
A9–A0 Don't Care Don't Care
$\overline{\text{BYP}}$
PTDI Idle select A0p A9p select Idle Don't Care†
PTMS Don't Care
$\overline{\text{PTRST}}$
STDI Don't Care
$\overline{\text{CON}}$
PTDO PTDO = STDI Idle select A0p A9p select Idle PTDO = STDI
STCK
STDO A0p A9p STDO = PTDI
STMS STMS = PTMS STMS = $STMS_0$ STMS = PTMS
$\overline{\text{STRST}}$

Select Protocol | Acknowledge Protocol | ON

† The instantaneous value of PTDI during protocol acknowledge is "don't care" as long as the cumulative effect does not represent a protocol hard-error or another valid select protocol.

**Figure 6. Shadow-Protocol Timing, Protocol Result = MATCH, Prior Connect Status = ON**




† The instantaneous value of PTDI during protocol acknowledge is "don't care" as long as the cumulative effect does not represent a protocol hard-error or another valid select protocol.

**Figure 7. Shadow-Protocol Timing, Protocol Result = MATCH, Prior Connect Status = OFF**

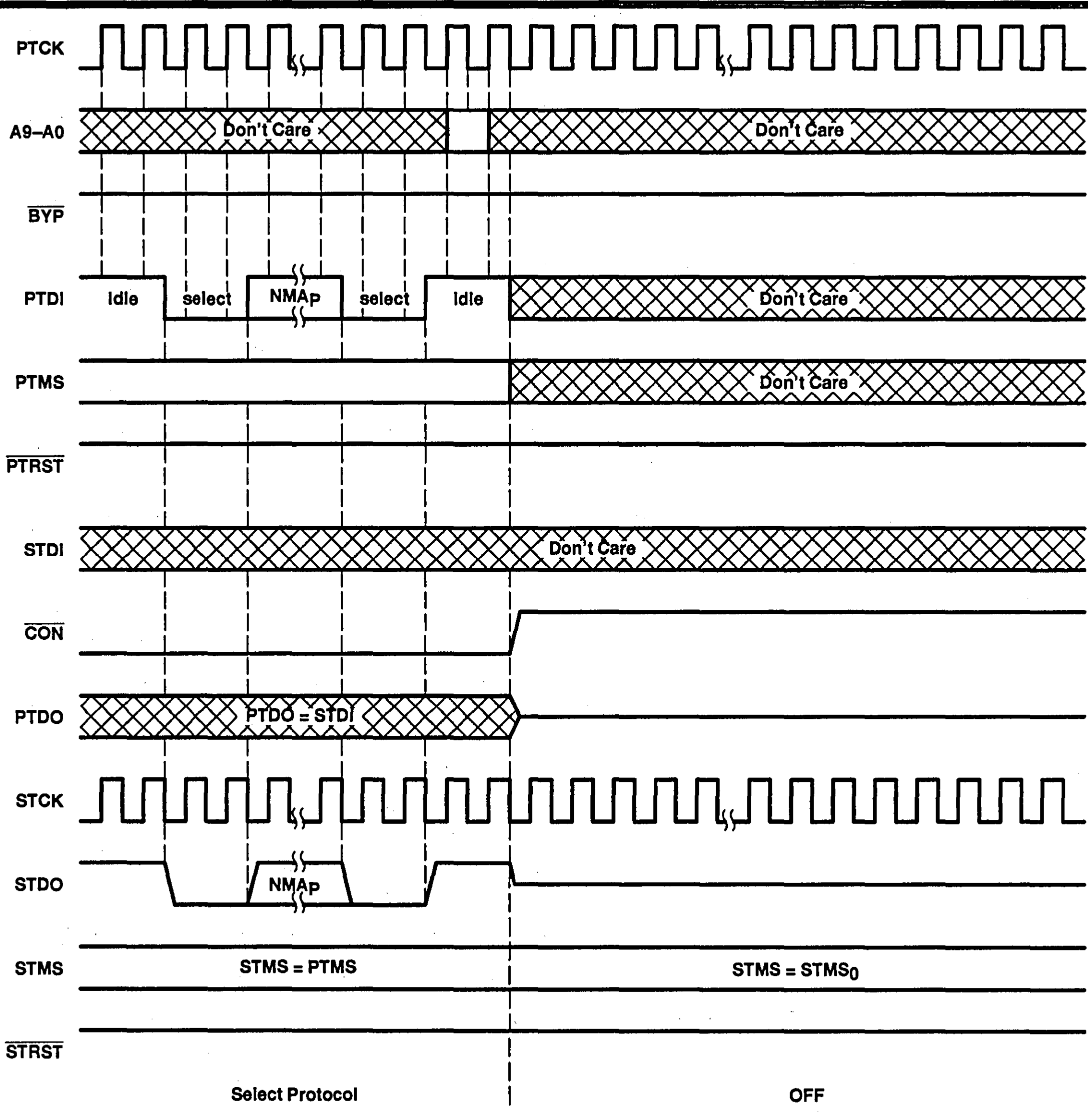



**Figure 8. Shadow-Protocol Timing, Protocol Result = NO MATCH, Prior Connect Status = ON**

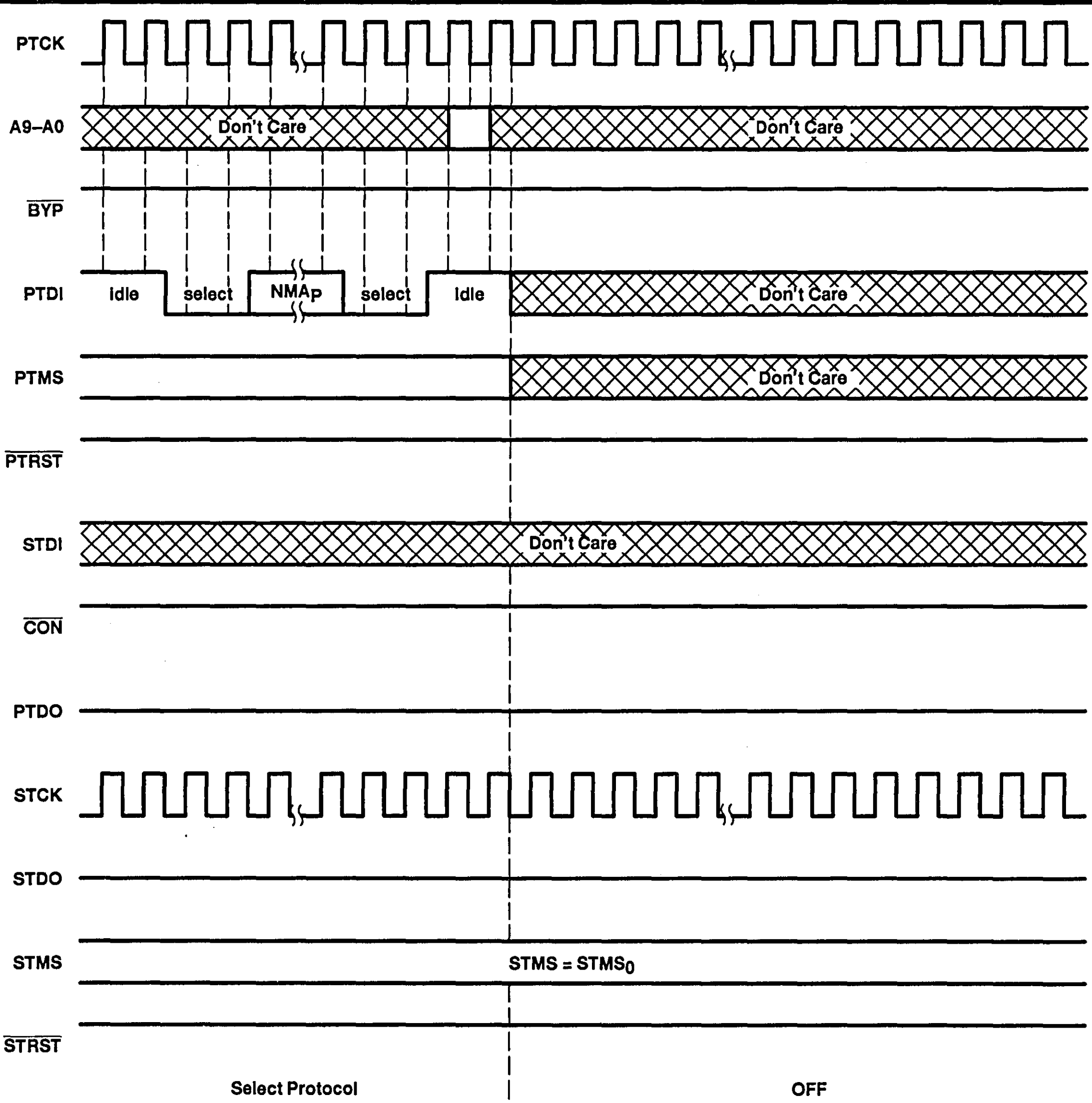



Figure 9. Shadow-Protocol Timing, Protocol Result = NO MATCH, Prior Connect Status = OFF

Figure 10. Shadow-Protocol Timing, Protocol Result = DISCONNECT, Prior Connect Status = ON

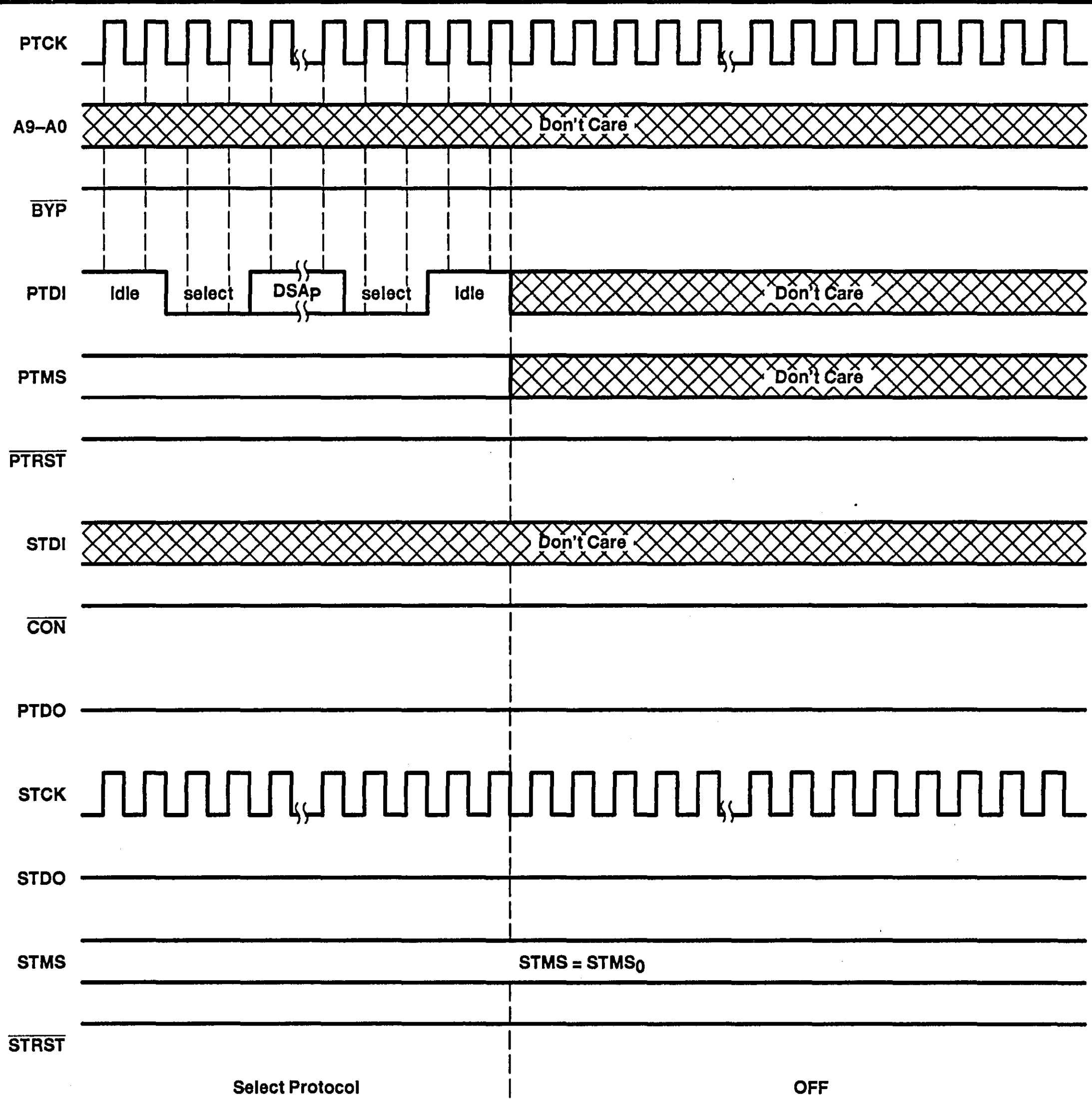



Figure 11. Shadow-Protocol Timing, Protocol Result = DISCONNECT, Prior Connect Status = OFF

**Figure 12. Shadow-Protocol Timing, Protocol Result = RESET, Prior Connect Status = ON**

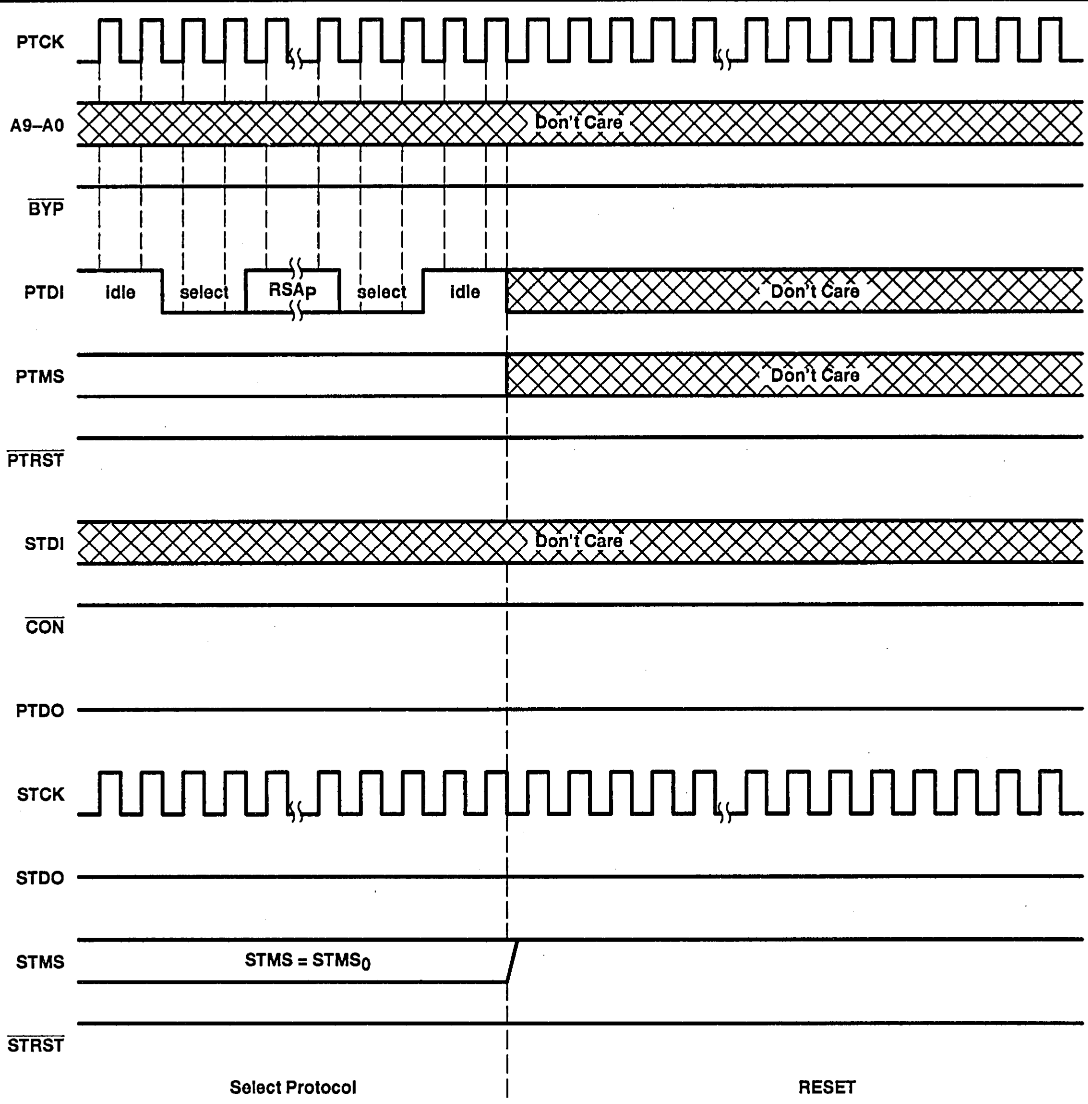



Figure 13. Shadow-Protocol Timing, Protocol Result = RESET, Prior Connect Status = OFF

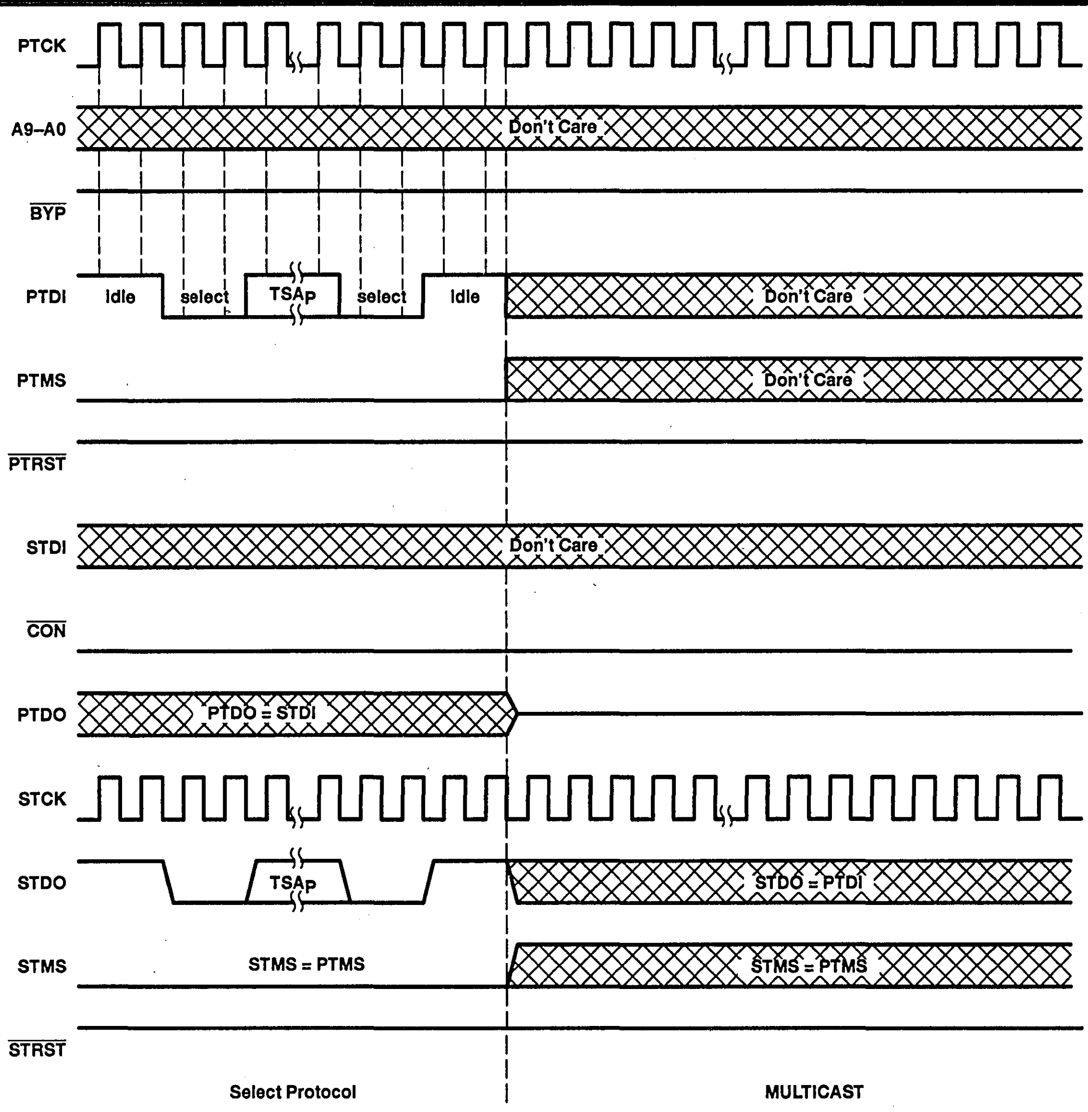



Figure 14. Shadow-Protocol Timing,
Protocol Result = TEST SYNCHRONIZATION, Prior Connect Status = ON

PTCK
A9–A0 Don't Care
BYP
PTDI idle select TSAp select idle Don't Care
PTMS Don't Care
PTRST
STDI Don't Care
CON
PTDO
STCK
STDO STDO = PTDI
STMS STMS = STMS0 STMS = PTMS
STRST
Select Protocol MULTICAST

**Figure 15. Shadow-Protocol Timing,**
**Protocol Result = TEST SYNCHRONIZATION, Prior Connect Status = OFF**

PTCK
A9–A0 Don't Care
$\overline{BYP}$
PTDI Idle select D0p Dnp select Idle Don't Care
PTMS Don't Care
$\overline{PTRST}$
STDI Don't Care
$\overline{CON}$
PTDO PTDO = STDI
STCK
STDO D0p Dnp
STMS STMS = PTMS STMS = $STMS_0$
$\overline{STRST}$

Select Protocol (aborted) OFF

NOTE: The position of PTMS shown in this figure is only one of many that would produce protocol result HARD ERROR.

**Figure 16. Shadow-Protocol Timing, Protocol Result = HARD ERROR (PTMS change during select protocol), Prior Connect Status = ON**

PTCK

A9–A0 Don't Care Don't Care

$\overline{BYP}$

PTDI Idle select A0p A9p select Idle Don't Care

PTMS Don't Care

$\overline{PTRST}$

STDI Don't Care

$\overline{CON}$

PTDO PTDO = STDI Idle

STCK

STDO A0p A9p

STMS STMS = PTMS STMS = $STMS_0$

$\overline{STRST}$

Select Protocol | Acknowledge Protocol (aborted) | OFF

NOTE: The position of PTMS shown in this figure is only one of many that would produce protocol result HARD ERROR.

**Figure 17. Shadow-Protocol Timing,
Protocol Result = HARD ERROR (PTMS change during acknowledge protocol),
Prior Connect Status = ON**

NOTE: The sequence of PTDI bits shown in this figure is only one of many that would produce protocol result SOFT ERROR.

**Figure 18. Shadow-Protocol Timing,
Protocol Result = SOFT ERROR, Prior Connect Status = ON**

## protocol-bypass timing



Figure 19. Protocol-Bypass Timing, Prior Connect Status = ON

PTCK
A9–A0 Don't Care
$\overline{BYP}$
PTDI Don't Care
PTMS Don't Care
$\overline{PTRST}$
STDI Don't Care
$\overline{CON}$
PTDO PTDO = STDI
STCK
STDO STDO = PTDI
STMS STMS = $STMS_0$ STMS = PTMS STMS = $STMS_0$
$\overline{STRST}$
OFF BYP OFF

**Figure 20. Protocol-Bypass Timing, Prior Connect Status = OFF**

### asynchronous reset timing

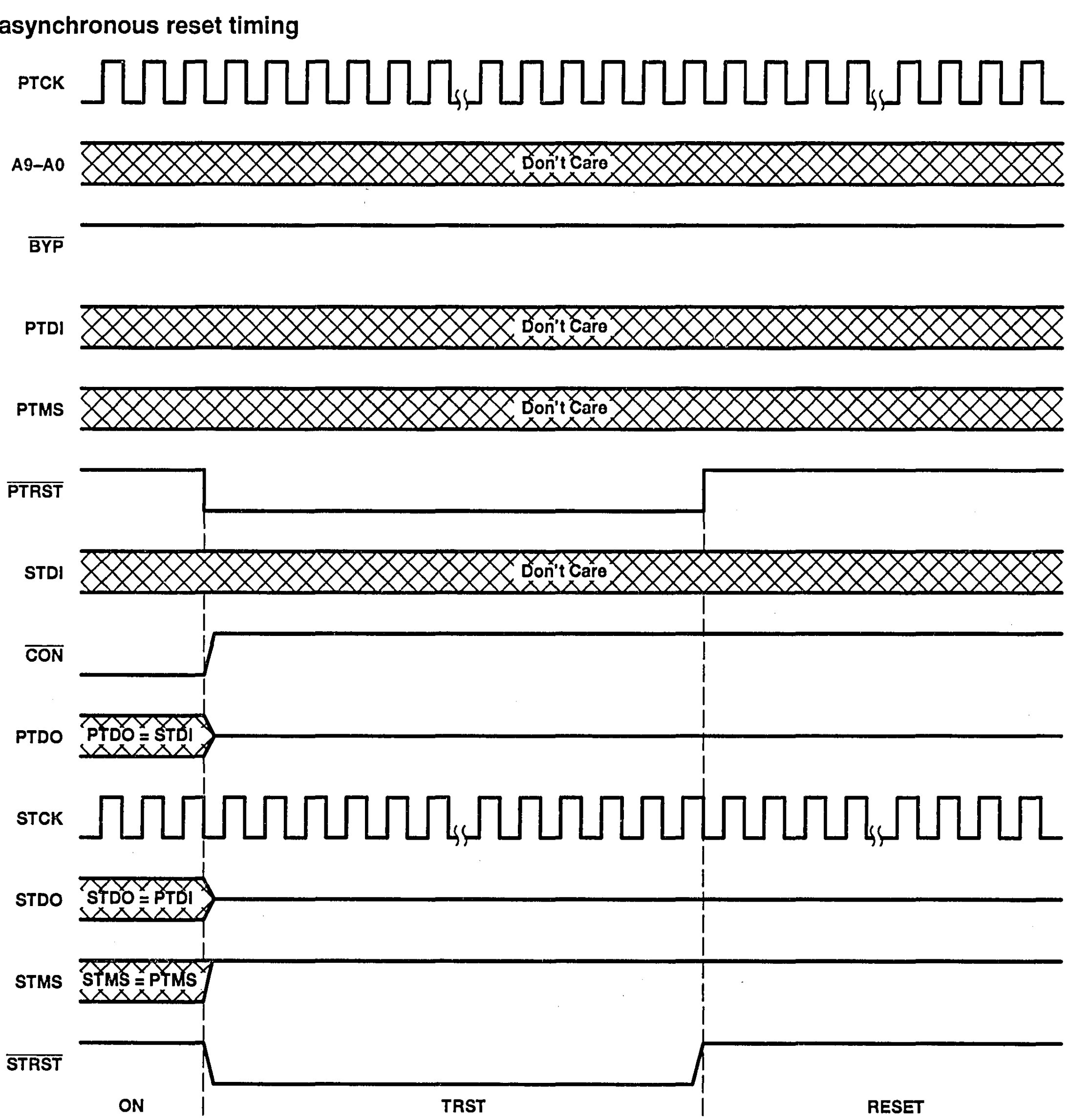



Figure 21. Asynchronous Reset Timing, Prior Connect Status = ON

PTCK
A9–A0 Don't Care
BYP
PTDI Don't Care
PTMS Don't Care
PTRST
STDI Don't Care
CON
PTDO
STCK
STDO
STMS STMS = $STMS_0$
STRST
OFF TRST RESET

Figure 22. Asynchronous Reset Timing, Prior Connect Status = OFF

PTCK
A9–A0 Don't Care
$\overline{BYP}$
PTDI Don't Care
PTMS Don't Care
$\overline{PTRST}$
STDI Don't Care
$\overline{CON}$
PTDO PTDO = STDI
STCK
STDO STDO = PTDI
STMS STMS = PTMS STMS = PTMS
$\overline{STRST}$

BYP | BYP/TRST | BYP

**Figure 23. Asynchronous Reset Timing, $\overline{BYP}$ = L**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ . . . . . . . . . . –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT8996 . . . . . . . . . . 96 mA
SN74ABT8996 . . . . . . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) . . . . . . . . . . –18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) . . . . . . . . . . –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air)(see Note 2): DW package . . . . . . . . . . 1.7 W
PW package . . . . . . . . . . 0.7 W
Storage temperature range, $T_{stg}$ . . . . . . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | SN54ABT8996 | | SN74ABT8996 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | $T_A$ = 25°C MIN | $T_A$ = 25°C TYP† | $T_A$ = 25°C MAX | SN54ABT8996 MIN | SN54ABT8996 MAX | SN74ABT8996 MIN | SN74ABT8996 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | | 3 | | | 3 | | 3 | | |
| | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | | 2 | | | 2 | | | | |
| | | $I_{OH}$ = –32 mA | | 2* | | | | | 2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | | 0.55 | | 0.55 | | | V |
| | | $I_{OL}$ = 64 mA | | | | 0.55* | | | | 0.55 | |
| $I_I$ | $V_{CC}$ = 0 to 5.5 V, $V_I$ = $V_{CC}$ or GND | | PTCK | | | ±1 | | | | ±1 | µA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ | PTDI, PTMS, $\overline{PTRST}$ | | | 10 | | 10 | | 10 | µA |
| | | | A9–A0, $\overline{BYP}$, STDI | | | 10 | | 10 | | 10 | |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = GND | PTDI, PTMS, $\overline{PTRST}$ | –18 | | –50 | –18 | –50 | –18 | –50 | µA |
| | | | A9–A0, $\overline{BYP}$, STDI | –60 | | –150 | –60 | –150 | –60 | –150 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | PTDO, STDO | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | PTDO, STDO | | | –10 | | –10 | | –10 | µA |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | | –50 | –110 | –200 | –50 | –200 | –50 | –200 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | OFF, STCK = H, STMS = H | | | 0.8 | 1.5 | | 1.5 | | 1.5 | mA |
| | | ON, PTDO = L, STCK = L, STDO = L, STMS = L | | | 13 | 18 | | 18 | | 18 | |
| | | ON, PTDO = H, STCK = H, STDO = H, STMS = H | | | 3.2 | 5 | | 5 | | 5 | |
| | | TRST, STCK = L | | | 6 | 8 | | 8 | | 8 | |
| $\Delta I_{CC}$§ | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = 2.5 V or 0.5 V | | | | 5 | | | | | | pF |
| $C_o$ | $V_O$ = 2.5 V or 0.5 V | | | | 8 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)**

| | | | SN54ABT8996 | | SN74ABT8996 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | PTCK | 0 | 40 | 0 | 40 | MHz |
| $t_w$ | Pulse duration | $\overline{BYP}$ low† | 4.9 | | 4.9 | | ns |
| | | PTCK high | 12 | | 12 | | |
| | | PTCK low | 6.5 | | 6.5 | | |
| | | $\overline{PTRST}$ low | 2.6 | | 2.6 | | |
| $t_{su}$ | Setup time | A9–A0 before PTCK↓‡ | 6.6 | | 6.6 | | ns |
| | | PTDI before PTCK↑ | 4.9 | | 4.9 | | |
| | | PTMS before $\overline{BYP}$↑† | 0.8 | | 0.6 | | |
| | | PTMS before PTCK↑ | 9 | | 9 | | |
| $t_h$ | Hold time | A9–A0 after PTCK↓‡ | 0.3 | | 0.3 | | ns |
| | | PTDI after PTCK↑ | 0.7 | | 0.7 | | |
| | | PTMS after $\overline{BYP}$↑† | 2.4 | | 2.4 | | |
| | | PTMS after PTCK↑ | 1.3 | | 1.3 | | |

† In normal application of the ASP, such timing requirements with respect to $\overline{BYP}$ are met implicitly and, therefore, need not be considered.
‡ These requirements apply only in the case where the address inputs are changed during a shadow protocol. For normal application of the ASP, it is recommended that the address inputs remain static throughout any shadow protocols. In such cases, the timing of address inputs relative to PTCK need not be considered.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT8996 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –55°C to 125°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | PTCK | | 40 | | | 40 | | MHz |
| $t_{PLH}$ | $\overline{BYP}$↑ | $\overline{CON}$ | 1 | 3 | 4.2 | 1 | 5.3 | ns |
| $t_{PHL}$ | $\overline{BYP}$↓ | | 1 | 3.8 | 5.2 | 1 | 6.3 | |
| $t_{PLH}$ | $\overline{BYP}$↓ | STMS | 2.5 | 7.8 | 10 | 2.5 | 12.9 | ns |
| $t_{PHL}$ | | | 2.5 | 5.2 | 7 | 2.5 | 8.9 | |
| $t_{PLH}$ | PTCK | STCK | 1 | 2.2 | 3.1 | 1 | 3.7 | ns |
| $t_{PHL}$ | | | 1 | 2.8 | 3.9 | 1 | 4.6 | |
| $t_{PLH}$ | PTCK↓ | $\overline{CON}$ | 3.5 | 6.9 | 8.9 | 3.5 | 11.2 | ns |
| $t_{PHL}$ | | | 3.5 | 7 | 9.3 | 3.5 | 11.6 | |
| $t_{PLH}$ | PTCK↓ (shadow-protocol acknowledge) | PTDO | 3 | 7.6 | 9.9 | 3 | 12.6 | ns |
| $t_{PHL}$ | | | 3 | 6.2 | 9.4 | 3 | 10.9 | |
| $t_{PLH}$† | PTCK↓ (connect) | STMS | 5.5 | 12.1 | 15.4 | 5.5 | 19.9 | ns |
| $t_{PHL}$† | | | 5.5 | 9.7 | 12.5 | 5.5 | 15.8 | |
| $t_{PLH}$ | PTDI | STDO | 1 | 3.1 | 4.4 | 1 | 5.4 | ns |
| $t_{PHL}$ | | | 1 | 3.3 | 4.5 | 1 | 5.6 | |
| $t_{PLH}$ | PTMS | STMS | 1 | 3.2 | 4.4 | 1 | 5.5 | ns |
| $t_{PHL}$ | | | 1 | 3.4 | 4.7 | 1 | 5.7 | |
| $t_{PLH}$ | $\overline{PTRST}$ | $\overline{STRST}$ | 1 | 3.2 | 4.8 | 1 | 5.8 | ns |
| $t_{PHL}$ | | | 1 | 3.3 | 4.7 | 1 | 5.7 | |
| $t_{PLH}$ | $\overline{PTRST}$↓ | $\overline{CON}$ | 3.5 | 7.4 | 9.5 | 3.5 | 12.1 | ns |
| | | STMS | 2.5 | 5.6 | 7.7 | 2.5 | 9.6 | |
| $t_{PLH}$ | STDI | PTDO | 1 | 2.8 | 4 | 1 | 4.9 | ns |
| $t_{PHL}$ | | | 1 | 3.3 | 4.6 | 1 | 5.7 | |

† The transitions at STMS are only possible when a shadow-protocol select is issued while STMS is held (in the OFF status) at a level that differs from that at PTMS. Such operation is not recommended since state synchronization of the primary TAP to secondary TAP cannot be ensured.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued) (see Figure 24)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT8996 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –55°C to 125°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PZH}$† | $\overline{BYP}$↓ | PTDO | 1.5 | 4 | 5.5 | 1.5 | 6.9 | ns |
| $t_{PZL}$ | | | 1.5 | 4.5 | 6.1 | 1.5 | 7.5 | |
| $t_{PZH}$‡ | $\overline{BYP}$↓ | STDO | 1.5 | 3.7 | 5.2 | 1.5 | 6.2 | ns |
| $t_{PZL}$ | | | 1.5 | 4.2 | 5.8 | 1.5 | 6.9 | |
| $t_{PZH}$† | PTCK↓ | PTDO | 4 | 7.2 | 9.5 | 4 | 12.1 | ns |
| $t_{PZH}$‡ | PTCK↓ | STDO | 4 | 7.6 | 10 | 4 | 12.5 | ns |
| $t_{PZL}$ | | | 4 | 8.1 | 10.7 | 4 | 12.8 | |
| $t_{PHZ}$† | $\overline{BYP}$↑ | PTDO | 1.5 | 3.6 | 4.8 | 1.5 | 5.5 | ns |
| $t_{PLZ}$ | | | 1.3 | 3.6 | 4.9 | 1.3 | 5.8 | |
| $t_{PHZ}$‡ | $\overline{BYP}$↑ | STDO | 1.5 | 3.6 | 4.8 | 1.5 | 5.5 | ns |
| $t_{PLZ}$ | | | 1.5 | 3 | 4.2 | 1.5 | 4.8 | |
| $t_{PHZ}$† | PTCK↓ | PTDO | 3 | 6.2 | 8.2 | 3 | 11 | ns |
| $t_{PLZ}$ | | | 1 | 6.9 | 9.5 | 1 | 13.1 | |
| $t_{PHZ}$‡ | PTCK↓ | STDO | 3.5 | 7.3 | 9.2 | 3.5 | 12 | ns |
| $t_{PLZ}$§ | | | 1 | 7.1 | 8.7 | 1 | 10.4 | |
| $t_{PHZ}$† | $\overline{PTRST}$↓ | PTDO | 3.5 | 6.6 | 9.2 | 3.5 | 11 | ns |
| $t_{PLZ}$ | | | 1 | 7.4 | 10.2 | 1 | 13.4 | |
| $t_{PHZ}$‡ | $\overline{PTRST}$↓ | STDO | 4.5 | 9.4 | 12 | 4.5 | 13.6 | ns |
| $t_{PLZ}$ | | | 3 | 7.3 | 9 | 3 | 10.5 | |

† In most applications, the node to which PTDO is connected has a pullup resistor. In such cases, this parameter is not significant.
‡ In most applications, the node to which STDO is connected has a pullup resistor. In such cases, this parameter is not significant.
§ This parameter applies only in case of protocol hard error.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT8996 $V_{CC}$ = 5 V, $T_A$ = 25°C MIN | TYP | MAX | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | PTCK | | 40 | | | 40 | | MHz |
| $t_{PLH}$ | $\overline{BYP}$↑ | $\overline{CON}$ | 1 | 3 | 4.2 | 1 | 4.8 | ns |
| $t_{PHL}$ | $\overline{BYP}$↓ | | 1 | 3.8 | 5.2 | 1 | 6 | |
| $t_{PLH}$ | $\overline{BYP}$↓ | STMS | 2.5 | 7.8 | 10 | 2.5 | 12.2 | ns |
| $t_{PHL}$ | | | 2.5 | 5.2 | 7 | 2.5 | 8.4 | |
| $t_{PLH}$ | PTCK | STCK | 1 | 2.2 | 3.1 | 1 | 3.4 | ns |
| $t_{PHL}$ | | | 1 | 2.8 | 3.9 | 1 | 4.5 | |
| $t_{PLH}$ | PTCK↓ | $\overline{CON}$ | 3.5 | 6.9 | 8.9 | 3.5 | 10.6 | ns |
| $t_{PHL}$ | | | 3.5 | 7 | 9.3 | 3.5 | 10.8 | |
| $t_{PLH}$ | PTCK↓ (shadow-protocol acknowledge) | PTDO | 3 | 7.6 | 9.9 | 3 | 11.8 | ns |
| $t_{PHL}$ | | | 3 | 6.2 | 9.4 | 3 | 10.2 | |
| $t_{PLH}$† | PTCK↓ (connect) | STMS | 5.5 | 12.1 | 15.4 | 5.5 | 18.6 | ns |
| $t_{PHL}$† | | | 5.5 | 9.7 | 12.5 | 5.5 | 14.9 | |
| $t_{PLH}$ | PTDI | STDO | 1 | 3.1 | 4.4 | 1 | 5 | ns |
| $t_{PHL}$ | | | 1 | 3.3 | 4.5 | 1 | 5.3 | |
| $t_{PLH}$ | PTMS | STMS | 1 | 3.2 | 4.4 | 1 | 5.1 | ns |
| $t_{PHL}$ | | | 1 | 3.4 | 4.7 | 1 | 5.5 | |
| $t_{PLH}$ | $\overline{PTRST}$ | $\overline{STRST}$ | 1 | 3.2 | 4.8 | 1 | 5.7 | ns |
| $t_{PHL}$ | | | 1 | 3.3 | 4.7 | 1 | 5.7 | |
| $t_{PLH}$ | $\overline{PTRST}$↓ | $\overline{CON}$ | 3.5 | 7.4 | 9.5 | 3.5 | 11.4 | ns |
| | | STMS | 2.5 | 5.6 | 7.7 | 2.5 | 9.2 | |
| $t_{PLH}$ | STDI | PTDO | 1 | 2.8 | 4 | 1 | 4.5 | ns |
| $t_{PHL}$ | | | 1 | 3.3 | 4.6 | 1 | 5.4 | |

† The transitions at STMS are possible only when a shadow-protocol select is issued while STMS is held (in the OFF status) at a level that differs from that at PTMS. Such operation is not recommended since state synchronization of the primary TAP to secondary TAP cannot be ensured.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued) (see Figure 24)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT8996 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –40°C to 85°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PZH}$† | $\overline{BYP}$↓ | PTDO | 1.5 | 4 | 5.5 | 1.5 | 6.6 | ns |
| $t_{PZL}$ | | | 1.5 | 4.5 | 6.1 | 1.5 | 7.2 | |
| $t_{PZH}$‡ | $\overline{BYP}$↓ | STDO | 1.5 | 3.7 | 5.2 | 1.5 | 6 | ns |
| $t_{PZL}$ | | | 1.5 | 4.2 | 5.8 | 1.5 | 6.7 | |
| $t_{PZH}$† | PTCK↓ | PTDO | 4 | 7.2 | 9.5 | 4 | 11.3 | ns |
| $t_{PZH}$‡ | PTCK↓ | STDO | 4 | 7.6 | 10 | 4 | 11.7 | ns |
| $t_{PZL}$ | | | 4 | 8.1 | 10.7 | 4 | 12.2 | |
| $t_{PHZ}$† | $\overline{BYP}$↑ | PTDO | 1.5 | 3.6 | 4.8 | 1.5 | 5.3 | ns |
| $t_{PLZ}$ | | | 1.5 | 3.6 | 4.9 | 1.5 | 5.3 | |
| $t_{PHZ}$‡ | $\overline{BYP}$↑ | STDO | 1.5 | 3.6 | 4.8 | 1.5 | 5.4 | ns |
| $t_{PLZ}$ | | | 1.5 | 3 | 4.2 | 1.5 | 4.4 | |
| $t_{PHZ}$† | PTCK↓ | PTDO | 3 | 6.2 | 8 | 3 | 10.3 | ns |
| $t_{PLZ}$ | | | 3 | 6.9 | 9.5 | 3 | 11.2 | |
| $t_{PHZ}$‡ | PTCK↓ | STDO | 3.5 | 7.3 | 9 | 3.5 | 10.9 | ns |
| $t_{PLZ}$§ | | | 3.5 | 7.1 | 8.7 | 3.5 | 10.4 | |
| $t_{PHZ}$† | $\overline{PTRST}$↓ | PTDO | 3.5 | 6.6 | 8.5 | 3.5 | 10.4 | ns |
| $t_{PLZ}$ | | | 3.5 | 7.4 | 10.2 | 3.5 | 11.7 | |
| $t_{PHZ}$‡ | $\overline{PTRST}$↓ | STDO | 4.5 | 9.4 | 11.5 | 4.5 | 13.2 | ns |
| $t_{PLZ}$ | | | 4.5 | 7.3 | 9 | 4.5 | 10.5 | |

† In most applications, the node to which PTDO is connected has a pullup resistor. In such cases, this parameter is not significant.
‡ In most applications, the node to which STDO is connected has a pullup resistor. In such cases, this parameter is not significant.
§ This parameter applies only in case of protocol hard error.

## PARAMETER MEASUREMENT INFORMATION

From Output Under Test

$C_L$ = 50 pF (see Note A)

500 Ω

500 Ω

S1

7 V

Open

GND

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

Input 1.5 V 1.5 V 3 V 0 V $t_w$

VOLTAGE WAVEFORMS
PULSE DURATION

Timing Input 1.5 V 3 V 0 V $t_{su}$ $t_h$

Data Input 1.5 V 1.5 V 3 V 0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

Input 1.5 V 1.5 V 3 V 0 V

$t_{PLH}$ $t_{PHL}$

Output 1.5 V 1.5 V $V_{OH}$ $V_{OL}$

$t_{PHL}$ $t_{PLH}$

Output 1.5 V 1.5 V $V_{OH}$ $V_{OL}$

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

Output Control 1.5 V 1.5 V 3 V 0 V

$t_{PZL}$ $t_{PLZ}$

Output Waveform 1 S1 at 7 V (see Note B) 1.5 V $V_{OL}$ + 0.3 V 3.5 V $V_{OL}$

$t_{PZH}$ $t_{PHZ}$

Output Waveform 2 S1 at Open (see Note B) 1.5 V $V_{OH}$ – 0.3 V $V_{OH}$ ≈ 0 V

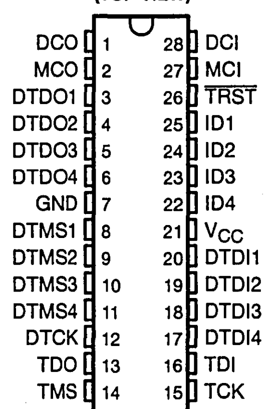
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. $C_L$ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

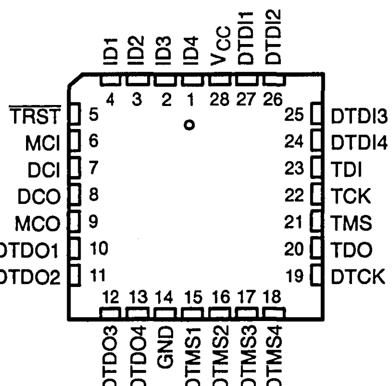
**Figure 24. Load Circuit and Voltage Waveforms**

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Serial Test Bus
- Allow Partitioning of System Scan Paths
- Can Be Cascaded Horizontally or Vertically
- Select Up to Four Secondary Scan Paths to Be Included in a Primary Scan Path
- Include 8-Bit Programmable Binary Counter to Count or Initiate Interrupt Signals
- Include 4-Bit Identification Bus for Scan-Path Identification
- Inputs Are TTL Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

SN54ACT8997 . . . JT PACKAGE
SN74ACT8997 . . . DW OR NT PACKAGE
(TOP VIEW)




SN54ACT8997 . . . FK PACKAGE
(TOP VIEW)




## description

The 'ACT8997 are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of components facilitates testing of complex circuit-board assemblies.

The 'ACT8997 enhance the scan capability of TI's SCOPE™ family by allowing augmentation of a system's primary scan path with secondary scan paths (SSPs), which can be individually selected by the 'ACT8997 for inclusion in the primary scan path. These devices also provide buffering of test signals to reduce the need for external logic.

By loading the proper values into the instruction register and data registers, the user can select up to four SSPs to be included in a primary scan path. Any combination of the SSPs can be selected at a time. Any of the device's six data registers or the instruction register can be placed in the device's scan path, i.e., placed between test data input (TDI) and test data output (TDO) for subsequent shift and scan operations.

All operations of the device except counting are synchronous to the test clock pin (TCK). The 8-bit programmable up/down counter can be used to count transitions on the device condition input (DCI) pin and output interrupt signals via the device condition output (DCO) pin. The device can be configured to count on either the rising or falling edge of DCI.

The test access port (TAP) controller is a finite-state machine compatible with IEEE Standard 1149.1.

The SN54ACT8997 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT8997 is characterized for operation from 0°C to 70°C.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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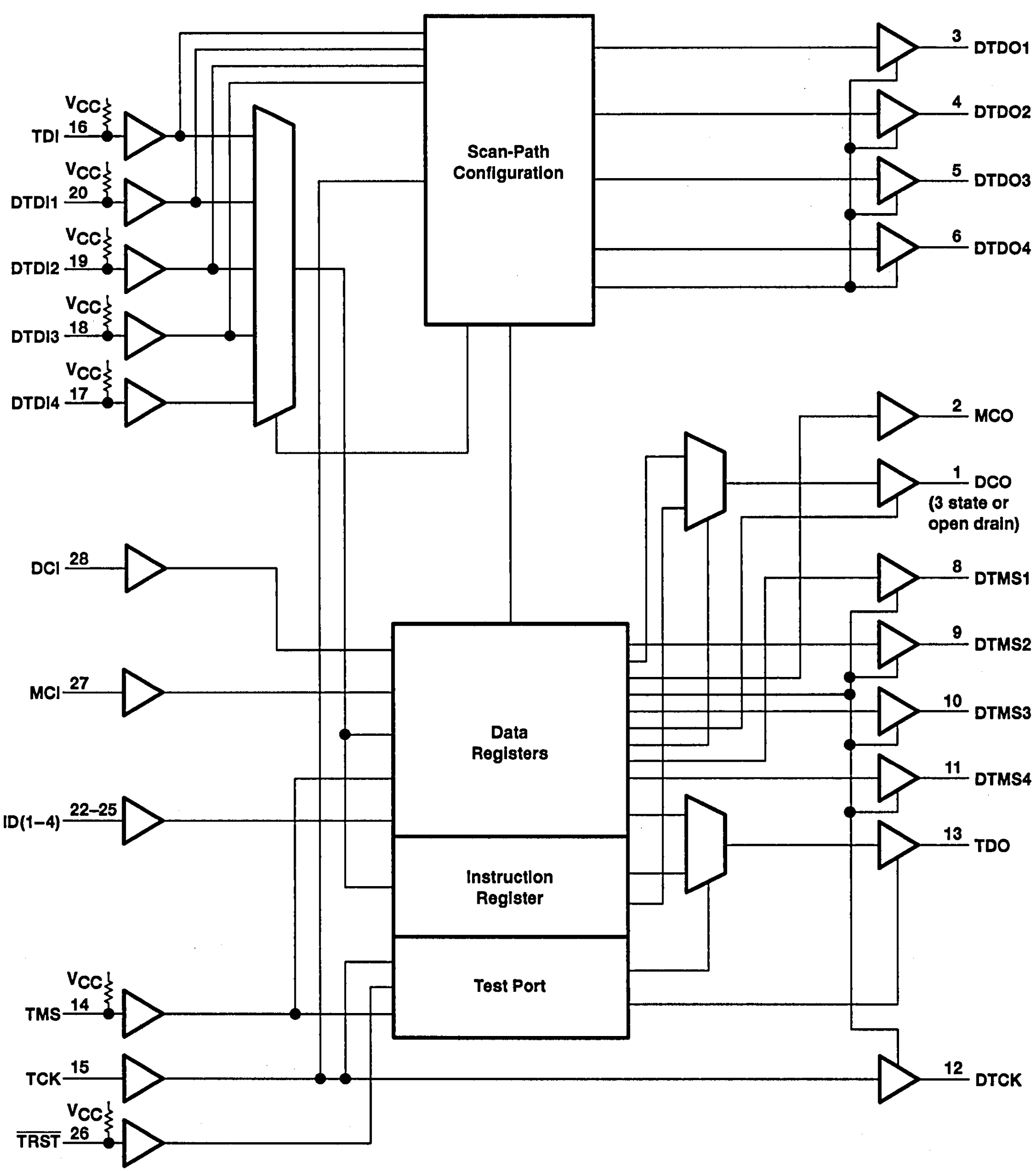
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

### functional block diagram




Pin numbers shown are for the DW, JT, and NT packages.



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## functional block description

The 'ACT8997 is intended to link secondary scan paths for inclusion in a primary scan path. Any combination of the four secondary scan paths can be linked, or the device can be bypassed entirely.

The least-significant bit (LSB) of any value scanned into any register of the device is the first bit shifted in (nearest to TDO). The most-significant bit (MSB) is the last bit shifted in (nearest to TDI).

The 'ACT8997 is divided into functional blocks as detailed below.

### test port

The test port decodes the signals on TCK, TMS, and $\overline{TRST}$ to control the operation of the circuit. The test port includes a TAP controller that issues the proper control instructions to the data registers according to the IEEE Standard 1149.1 protocol. The TAP controller state diagram is shown in Figure 1.

### instruction register

The instruction register (IR) is an 8-bit-wide serial-shift register that issues commands to the device. Data is input to the instruction register via TDI (or one of the DTDI pins) and shifted out via TDO. All device operations are initiated by loading the proper instruction or sequence of instructions into the IR.

### data registers

Six parallel data registers are included in the 'ACT8997: bypass, control, counter, boundary-scan, ID-bus, and select. The ID bus register is a part of the boundary-scan register. Each data register is serially loaded via TDI or DTDI and outputs data via TDO. Table 1 summarizes the registers in the 'ACT8997.

### scan-path-configuration circuit

This circuit decodes bits in the select and control registers to determine which, if any, of the secondary scan paths are to be included in the primary scan path.

**Table 1. Register Summary**

| REGISTER NAME | LENGTH (BITS) | FUNCTION |
|---|---|---|
| Instruction | 8 | Issue command information to the device |
| Control | 10 | Configuration and enable control |
| Counter | 8 | Count events on DCI, output interrupts via DCO |
| Select | 8 | Select one or more secondary scan paths |
| Boundary Scan | 10 | Capture and force test data at device periphery |
| ID Bus | 4 | Provide subsystem identification code |
| Bypass | 1 | Remove the 'ACT8997 from the scan path |

## Terminal Functions

| TERMINAL NAME | I/O | DESCRIPTION |
|---|---|---|
| DCI | I | Device condition input. DCI receives interrupt and protocol signals from the secondary scan path(s). When the counter register is instructed to count up or down, DCI is configured as the counter clock. |
| DCO | O | Device condition output. DCO is configured by the control register to output protocol and interrupt signals and can be configured by the control register to output an error signal if the instruction register is loaded with an invalid value. DCO is further configured by the control register as:<br>Active high or active low (reset condition = active low)<br>Open drain or 3 state (reset condition = open drain) |
| DTCK | O | Device test clock. DTCK outputs the buffered test clock TCK to the secondary scan path(s). |
| DTDI1<br>DTDI2<br>DTDI3<br>DTDI4 | I | Device test data input 1–4. DTDI1–DTDI4 receive the serial test data output(s) of the selected secondary scan path(s). An internal pullup forces DTDI1–DTDI4 to a high logic level if it is left unconnected. |
| DTDO1<br>DTDO2<br>DTDO3<br>DTDO4 | O | Device test data output 1–4. These outputs send serial test data to the TDI input(s) of the secondary scan path(s). |
| DTMS1<br>DTMS2<br>DTMS3<br>DTMS4 | O | Device test mode select 1–4. Any combination of these four outputs can be selected to follow TMS to direct the secondary scan path(s) through the TAP controller states in Figure 1. The unselected DTMS outputs can be set independently to a high or low logic level. The TMS circuit monitors input from the select register to determine the configuration of the DTMS outputs. |
| GND | | Ground |
| ID1<br>ID2<br>ID3<br>ID4 | I | Identification 1–4. This 4-bit data bus can be hardwired to provide identification of the subsystem under test. The value present on the bus can be scanned out through the boundary scan or ID bus registers. |
| MCI | I | Master condition input. MCI receives interrupt and protocol signals from a primary bus controller (PBC). The level on MCI is buffered and output on MCO. |
| MCO | O | Master condition output. MCO transmits interrupt and protocol signals to the secondary scan path(s). |
| TCK | I | Test clock. One of four terminals required by IEEE Standard 1149.1. All operations of the 'ACT8997 except for the count function are synchronous to TCK. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK. |
| TDI | I | Test data input. One of four terminals required by IEEE Standard 1149.1. TDI is the serial input for shifting information into the instruction register or selected data register. TDI is typically driven by the TDO of the PBC. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | O | Test data output. One of four terminals required by IEEE Standard 1149.1. TDO is the serial output for shifting information out of the instruction register or selected data register. TDO is typically connected to the TDI of the next scannable device in the primary scan path. |
| TMS | I | Test mode select. One of four terminals required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the 'ACT8997 through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $\overline{TRST}$ | I | Test reset. This active-low input implements the optional reset terminal of IEEE Standard 1149.1. When asserted, $\overline{TRST}$ causes the 'ACT8997 to go to the Test-Logic-Reset state and configure the instruction register and data registers to their power-up values. An internal pullup forces $\overline{TRST}$ to a high level if left unconnected. |
| $V_{CC}$ | | Supply voltage |

## state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. No more than one register can be manipulated at a time.

**Figure 1. TAP-Controller State Diagram**

### Test-Logic-Reset

In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if the test mode select (TMS) input is high. The TMS pin has an internal pullup that forces it to a high level if it is left unconnected or if a board defect causes it to be open circuited. The device powers up in the Test-Logic-Reset state.

### Run-Test/Idle

The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle. The 8-bit programmable up/down counter can be operated in this state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states; the TAP exits either of them on the next TCK cycle.

### Capture-DR

The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK, causing the TAP state to change.

### Shift-DR

In this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). On the falling edge of TCK in Shift-DR, TDO goes from the high-impedance state to the active state. TDO enables to the value present in the least-significant bit of the selected data register.

### Exit1-DR, Exit2-DR

These are temporary states that end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit-DR. TDO changes from the active state to the high-impedance state on the falling edge of TCK in Exit1-DR.

### Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state suspends and resumes shift operations without loss of data.

### Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated only during this state.

### Capture-IR

The instruction register is preloaded with the IR status word (see Table 4) and placed in the scan path.

### Shift-IR

In this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state, and will enable to a high level.

**Exit1-IR, Exit2-IR**

These are temporary states that end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR. TDO changes from the active state to the high-impedance state on the falling edge of TCK in Exit1-IR.

**Pause-IR**

The TAP can remain in this state indefinitely. The Pause-IR state suspends and resumes shift operations without loss of data.

**Update-IR**

In this state, the latches shadowing the instruction register are updated with the new instruction.

## instruction-register description

The instruction register (IR) is an 8-bit serial register that outputs control signals to the device. Table 2 lists the instructions implemented in the 'ACT8997 and the data register selected by each instruction. The MSB of the IR is an even-parity bit. If the value scanned into the IR during Shift-IR does not contain even parity, an error signal ($\overline{\text{IRERR}}$) is generated internally as shown in Table 3. The 'ACT8997 can be configured to output $\overline{\text{IRERR}}$ via DCO if the TAP enters the Pause-IR state.

During the Capture-IR state, the IR status word is loaded.The IR status word contains information about the most recently loaded value of the instruction register and the logic level present at the DCI input. The IR status word is encoded as shown in Table 4. Figure 2 shows the order of scan for the IR.

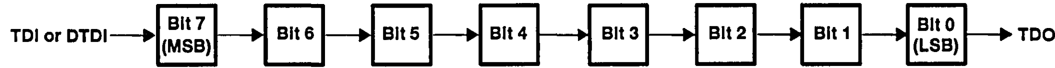



**Figure 2. Instruction-Register Bits and Order of Scan**

### Table 2. Instruction-Register Opcodes

| BINARY CODE BIT 7 → BIT 0 MSB → LSB | HEX VALUE | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|---|
| 00000000 | 00 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | 81 | BYPASS† | Bypass scan | Bypass | Normal |
| 10000010 | 82 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | 03 | INTEST | Boundary scan | Boundary scan | Test |
| 10000100 | 84 | BYPASS† | Bypass scan | Bypass | Normal |
| 00000101 | 05 | BYPASS† | Bypass scan | Bypass | Normal |
| 00000110 | 06 | BYPASS† | Bypass scan | Bypass | Normal |
| 10000111 | 87 | BYPASS† | Bypass scan | Bypass | Normal |
| 10001000 | 88 | COUNT | Count | Bypass | Normal |
| 00001001 | 09 | COUNT | Count | Bypass | Normal |
| 00001010 | 0A | BYPASS† | Bypass scan | Bypass | Normal |
| 10001011 | 8B | BYPASS† | Bypass scan | Bypass | Normal |
| 00001100 | 0C | BYPASS† | Bypass scan | Bypass | Normal |
| 10001101 | 8D | BYPASS | Bypass scan | Bypass | Normal |
| 10001110 | 8E | SCANCN | Control register scan | Control | Normal |
| 00001111 | 0F | SCANCN | Control register scan | Control | Normal |
| 11111010 | FA | SCANCNT | Counter scan | Counter | Normal |
| 01111011 | 7B | READCNT | Counter read | Counter | Normal |
| 11111100 | FC | SCANIDB | ID bus register scan | ID bus | Normal |
| 01111101 | 7D | READIDB | ID bus register read | ID bus | Normal |
| 01111110 | 7E | SCANSEL | Select register scan | Select | Normal |
| All others | | BYPASS | Bypass scan | Bypass | Normal |

† A SCOPE opcode exists but is not supported by the 'ACT8997.

### Table 3. $\overline{\text{IRERR}}$ Function Table

| NO. OF INSTRUCTION REGISTER BITS = 1 | $\overline{\text{IRERR}}$ |
|---|---|
| 0, 2, 4, 6, 8 | 1 |
| 1, 3, 5, 7 | 0 |

### Table 4. Instruction-Register Status Word

| IR BIT | VALUE† |
|---|---|
| 7 | $\overline{\text{IRERR}}$ (see Table 3) |
| 6 | 0 |
| 5 | 0 |
| 4 | 0 |
| 3 | DCI (1 = active, 0 = inactive) |
| 2 | 0 |
| 1 | 0 |
| 0 | 1 |

† This value is loaded in the instruction register during the Capture-IR TAP state.

## instruction-register opcode description

The operation of the 'ACT8997 is dependent on the instruction loaded into the IR. Each instruction selects one of the data registers to be placed between TDI or DTDI and TDO during the Shift-DR TAP state. All the required instructions of IEEE Standard 1149.1 are implemented in the 'ACT8997.

### boundary scan

This instruction implements the required EXTEST and optional INTEST operations of IEEE Standard 1149.1. The boundary-scan register (which includes the ID-bus register) is placed in the scan path. Data appearing at input pins included in the boundary-scan register is captured. Data previously loaded into the output pins included in the boundary-scan register is forced through the outputs.

### bypass scan

This instruction implements the required BYPASS operation of IEEE Standard 1149.1. The bypass register is placed in the scan path and preloads with a logic 0 during Capture-DR.

### sample boundary

This instruction implements the required SAMPLE/PRELOAD operation of IEEE Standard 1149.1. The boundary-scan register is placed in the scan path, and data appearing at the inputs and outputs included in the boundary-scan register is sampled on the rising edge of TCK in Capture-DR.

### count

The counter register begins counting on each DCI transition. The count begins from the value present in the register before the count instruction was loaded. The counter can be configured by the control register to count up or down on either the low-to-high or high-to-low transition of DCI. Counting occurs only while in the Run-Test/Idle TAP state.

### control-register scan

The control register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

### counter-register scan

The counter register is placed in the scan path. During Capture-DR, the current value of the counter is loaded in the counter register. At Update-DR, the newly shifted value is preloaded to the counter.

### counter-register read

The counter register is placed in the scan path. During Capture-DR, the prior preload value of the counter is loaded into the counter register. At Update-DR, the newly shifted value is preloaded to the counter.

### ID-bus-register scan

The ID-bus register (a subset of the boundary-scan register) is placed in the scan path for a subsequent shift operation. The data appearing on the ID bus is loaded into the ID-bus register on the rising edge of TCK in Capture-DR.

### ID-bus-register read

The ID-bus register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

### select-register scan

The select register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

## control register description

The control register (CTLR) is a 10-bit serial register that controls the enable and select functions of the 'ACT8997. A reset operation forces all bits to a low logic level. The contents of the CTLR are latched and decoded during the Update-DR TAP state. The specific function of each bit is listed in Table 5. The enable and select functions of the CTLR bits are mapped as follows:

**Table 5. Control-Register Bit Mapping**

| BIT | VALUE | FUNCTION |
|---|---|---|
| 9 | 0 | Configure counter to count up |
| | 1 | Configure counter to count down |
| 8 | 0 | Do not stop counting when the count reaches 00000000 |
| | 1 | Stop counting when the count reaches 00000000 (count down only) |
| 7 | 0 | Configure DCO as an active-low output |
| | 1 | Configure DCO as an active-high output |
| 6, 5 | 00 | DCO = Inactive (level depends on CTLR bit 7) |
| | 01 | DCO = $\overline{\text{IRERR}}$ |
| | 10 | DCO = $\overline{\text{CE}}$, an internal logic 0 generated when the count is 00000000 (count down) or 11111111 (count up) |
| | 11 | DCO = DCI |
| 4 | 0 | Do not mask $\overline{\text{IRERR}}$ from DCO |
| | 1 | Mask $\overline{\text{IRERR}}$ from DCO |
| 3 | 0 | Configure DCO as an open-drain output |
| | 1 | Configure DCO as a 3-state output |
| 2 | 0 | Disable DCO |
| | 1 | Enable DCO |
| 1 | 0 | Configure DCI as an active-low input |
| | 1 | Configure DCI as an active-high input |
| 0 | 0 | Enable DTCK, DTDO(1–4), and DTMS(1–4) [outputs DTDO(1–4) depend on select register (see Table 7)] |
| | 1 | Disable DTCK, DTDO(1–4), and DTMS(1–4) |

### Bit 9–$\overline{\text{Up}}$/Down

This bit sets the count mode of the counter register (reset condition = count up).

### Bit 8 – Latch on Zero

The counter register can be configured to stop counting when its value is 00000000 and ignore subsequent transitions on the counter clock, DCI. The latch-on-zero option is valid only in the count-down mode (reset condition = do not latch on zero). The value of this bit has no effect on the operation of the counter if CTLR bit 9 = 0.

### Bit 7 – DCO Polarity Select

DCO can be configured as an active-low or active-high output (reset condition = active low).

### Bit 6/Bit 5 – DCO Source Select 1/DCO Source Select 0

DCO can be used to output the $\overline{\text{IRERR}}$ signal generated by the 'ACT8997 (see Table 3). Bits 6 and 5 can be set to output $\overline{\text{IRERR}}$ via DCO on the falling edge of TCK in the Pause-IR state. DCO can also be configured to become active when the value of the counter is 00000000, to follow DCI, or be set to a static high or low level (reset condition = static high level).

**Bit 4 – Parity Mask**

The signal $\overline{\text{IRERR}}$ can be masked from appearing on DCO even if bits 6 and 5 are set such that it is output in the Pause-IR state (reset condition = do not mask $\overline{\text{IRERR}}$).

**Bit – DCO Drive Select**

DCO can be configured as either an open-drain or 3-state output (reset condition = open drain). The open-drain configuration allows multiple DCO outputs to be used in a wired-OR or wired-AND application. The 3-state configuration allows the DCO output to be connected to a bus.

**Bit 2 – DCO Enable**

When configured as a 3-state output, DCO can be placed in the high-impedance state (reset condition = disabled). If configured as an open-drain output and disabled, DCO outputs a high level.

**Bit 1 – DCI Polarity Select**

DCI can be configured as an active-low or active-high input (reset condition = active low).

**Bit 0 – Device Test Pins Output Enable (active low)**

DTCK, DTDO1–4, and DTMS1–4 pins can be placed in the high-impedance state (disabled) with this bit (reset condition = not disabled). If DTDO1–4 pins are not disabled using this control bit, then their drive state is dependent on the value of the select register (see Table 7).

Several CTLR bits affect the functionality of the DCO output. The DCO function table is given in Table 6. Figure 3 illustrates the order of scan for the CTLR.

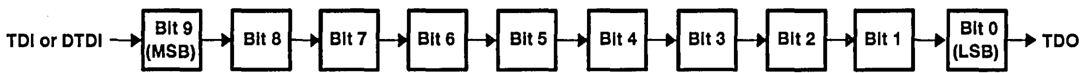



**Figure 3. Control-Register Bits and Order of Scan**

**Table 6. DCO Function Table**

| DCI | INTERNAL SIGNALS† | | CONTROL-REGISTER BITS‡ | | | | | | | DCO |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{IRERR}$ | $\overline{CE}$ | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | |
| X | X | X | X | X | X | X | 0 | 0 | X | H |
| X | X | X | X | X | X | X | 1 | 0 | X | Z |
| X | X | X | 0 | 0 | 0 | X | X | 1 | X | H |
| X | X | X | 1 | 0 | 0 | X | X | 1 | X | L |
| X | X | X | 0 | 0 | 1 | 1 | X | 1 | X | H |
| X | X | X | 1 | 0 | 1 | 1 | X | 1 | X | L |
| X | 0 | X | 0 | 0 | 1 | 0 | X | 1 | X | L in Pause-IR§, H otherwise |
| X | 1 | X | 0 | 0 | 1 | 0 | X | 1 | X | H |
| X | 0 | X | 1 | 0 | 1 | 0 | X | 1 | X | H in Pause-IR§, L otherwise |
| X | 1 | X | 1 | 0 | 1 | 0 | X | 1 | X | L |
| X | X | 0 | 0 | 1 | 0 | X | X | 1 | X | L |
| X | X | 0 | 1 | 1 | 0 | X | X | 1 | X | H |
| X | X | 1 | 0 | 1 | 0 | X | X | 1 | X | H |
| X | X | 1 | 1 | 1 | 0 | X | X | 1 | X | L |
| L | X | X | 1 | 1 | 1 | X | X | 1 | 0 | H |
| L | X | X | 1 | 1 | 1 | X | X | 1 | 1 | L |
| L | X | X | 0 | 1 | 1 | X | X | 1 | 0 | L |
| L | X | X | 0 | 1 | 1 | X | X | 1 | 1 | H |
| H | X | X | 1 | 1 | 1 | X | X | 1 | 0 | L |
| H | X | X | 1 | 1 | 1 | X | X | 1 | 1 | H |
| H | X | X | 0 | 1 | 1 | X | X | 1 | 0 | H |
| H | X | X | 0 | 1 | 1 | X | X | 1 | 1 | L |

† These signals are generated as described elsewhere in this data sheet.
‡ The control register must contain these values after the TAP has passed through its most recent Update-DR state.
§ DCO becomes active on the falling edge of TCK as the TAP enters the Pause-IR state and becomes inactive on the falling edge of TCK as the TAP enters Exit2-IR.

## select register description

The select register (SR) is an 8-bit serial register that determines which, if any, of the secondary scan paths (SSPs) will be included in the primary scan path. A reset operation forces all bits to a logic 0. The register is divided into four 2-bit sections, each of which controls one SSP. Figure 4 shows the mapping of the bits to the SSPs and the order of scan. For each SSP, the higher-order bit is the MSB and the lower-order bit is the LSB (e.g., bit 3 is the MSB of SSP2 and bit 2 is the LSB of SSP2).

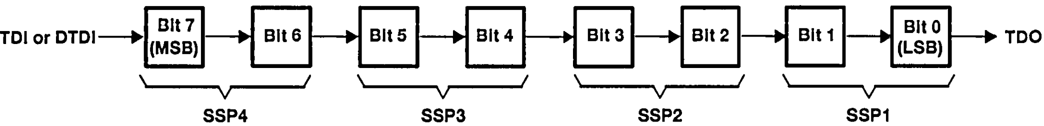



**Figure 4. Select Register Bits and Order of Scan**

When a new 8-bit value is loaded into the SR, the configuration of one or more DTMS pins may change. If the new value of the SR configures a DTMS pin to a static (high or low) level, it assumes that level on the falling edge of TCK in the Update-DR TAP state. This condition is independent of any previous SR configurations. If the new value of the SR forces a DTMS pin to follow TMS (i.e., select the secondary scan path) and one or more DTMS pins are currently in the TMS-follow mode, the transfer of DTMS lines occurs on the falling edge of TCK in the Update-DR TAP state. If, however, the new configuration forces a DTMS pin to follow TMS while no other DTMS pin is selected, the DTMS pin is forced low and does not begin following TMS until the falling edge of TCK in the Run-Test/Idle TAP state; therefore, when an SSP is initially selected, the TAP state should travel from Update-DR to Run-Test/Idle, not from Update-DR to Select-DR-Scan.

Although any combination of SSPs can be selected, the order of scan for each combination is fixed (see data flow description for details). The SR bit decoding is shown in Table 7.

**Table 7. Select Register-Bit Decoding**

| MSB | LSB | DTMS SOURCE | DTDO STATUS |
|---|---|---|---|
| 0 | 0 | H | Z |
| 0 | 1 | L | Z |
| 1 | X | TMS | Active† |

† The DTDO1–4 outputs are active only in the Shift-IR and Shift-DR TAP states.

## boundary-scan register/ID-bus register description

The boundary-scan register (BSR) is a 10-bit serial register that can be used to capture data appearing at selected device inputs, force data through device outputs, and apply data to the device's internal logic. The BSR is made up of boundary-scan cells (BSCs). Table 8 lists the device signal for each of the 10 BSCs that comprise the BSR. A reset operation does not affect the contents of the BSR.

**Table 8. Boundary-Scan Register Bit Mapping**

| BIT | TERMINAL NAME | SIGNAL DESCRIPTION |
|---|---|---|
| 9 | MCI | Master condition in |
| 8 | MCO | Master condition out |
| 7 | DCI | Device condition in |
| 6 | $\overline{DCOTS}$† | Enable control for DCO in 3-state configuration (active low) |
| 5 | $\overline{DCOOD}$† | Enable control for DCO in open-drain configuration (active low) |
| 4 | DCO | Device condition out |
| 3 | ID4 | Identification bus bit 4 |
| 2 | ID3 | Identification bus bit 3 |
| 1 | ID2 | Identification bus bit 2 |
| 0 | ID1 | Identification bus bit 1 |

† This internal signal cannot be observed from the I/O terminals of the device.

The four BSCs connected to the ID(1–4) terminals form a subset of the BSR called the ID-bus register (IDBR). The IDBR can be scanned without accessing the remaining BSCs of the BSR. Figure 5 shows the order of scan for the BSR and IDBR.

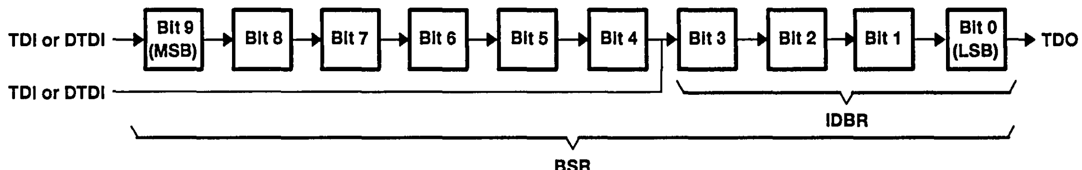



**Figure 5. Boundary-Scan Register Bits and Order of Scan**

## bypass register description

The bypass register (BR) is a 1-bit serial register. The BR provides a means of effectively removing the 'ACT8997 from the primary scan path when it is not needed for the current test operation. Any selected secondary scan paths remain active in the primary scan path as described in the data flow description. At power up, the BR is placed in the scan path. During Capture-DR, the BR is preloaded with a low logic level. Figure 6 shows the order of scan for the bypass register.

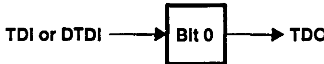



**Figure 6. Bypass-Register Bit and Order of Scan**

## counter register description

The counter register (CNTR) is an 8-bit serial register and an associated 8-bit parallel-load up/down counter. A reset operation forces all bits of the shift register to a logic 0 but does not affect the counter. The counter can be preloaded with an initial value before counting begins, and the current value of the counter scanned out via the shift register. The CNTR can be used to count events occurring on the secondary scan path(s) using the DCI pin as a counter clock and can output interrupt signals via DCO when the count has reached its end value.

An internal signal, $\overline{CE}$, is generated as a logic 0 when the count reaches its end value (i.e., 00000000 for count down, 11111111 for count up). For any other count value, $\overline{CE}$ is a logic 1. Many of the features of the CNTR are configured by a bit in the CTLR including:

Count direction up or down (control register bit 9; reset condition = count up).

Stop counting upon counting down to 00000000 (control register bit 8; reset condition = do not latch on zero).

Output $\overline{CE}$ signals at DCO (control register bits 5 and 6; reset condition = do not output $\overline{CE}$ at DCO).

Edge of DCI on which to trigger (control register bit 1; reset condition = positive edge).

Figure 7 shows the order of scan for the CNTR.

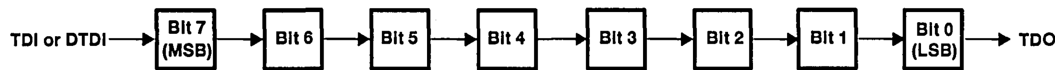
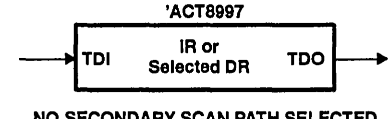


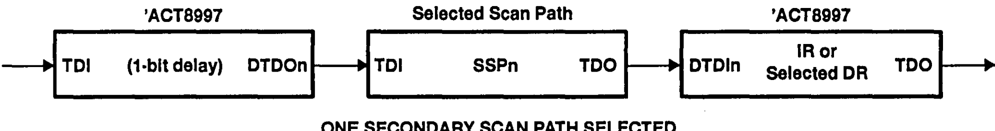

**Figure 7. Counter-Register Bits and Order of Scan**

## data flow description

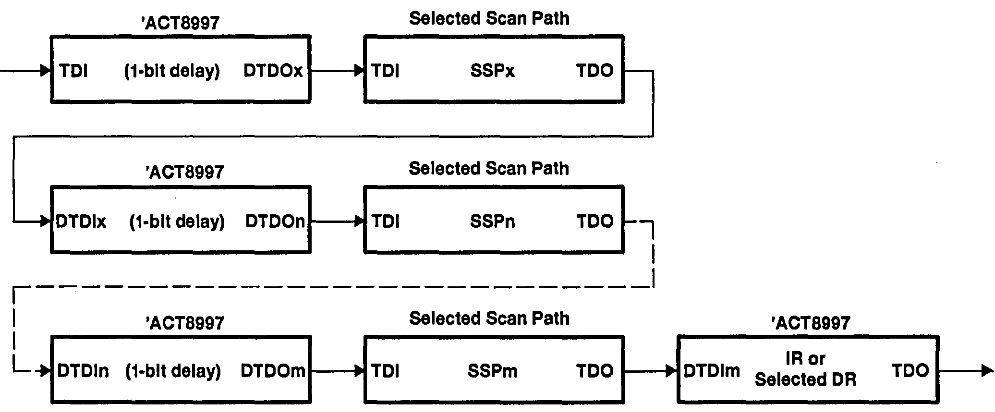
The direction of serial-data flow in the 'ACT8997 is dependent on the current instruction and value of the SR. Figure 8 shows the data flow when one or more SSPs have been selected. When more than one SSP has been selected, the order of scan is determined by which SSPs have been selected as shown in Table 9. The 'ACT8997 add one bit of delay from TDI or DTDI to DTDO.




NO SECONDARY SCAN PATH SELECTED




ONE SECONDARY SCAN PATH SELECTED




MULTIPLE SECONDARY SCAN PATHS SELECTED

**Figure 8. Data Flow in the 'ACT8997**

**Table 9. Scan-Path Configurations**

| SR BIT | | | | SSP CONFIGURATION | | | | SCAN-PATH CONFIGURATION†‡ |
|---|---|---|---|---|---|---|---|---|
| 7 | 5 | 3 | 1 | SSP4 | SSP3 | SSP2 | SSP1 | |
| 0 | 0 | 0 | 0 | Inactive | Inactive | Inactive | Inactive | TDI–SPL–TDO |
| 0 | 0 | 0 | 1 | Inactive | Inactive | Inactive | Active | TDI–(1)–SSP1–SPL–TDO |
| 0 | 0 | 1 | 0 | Inactive | Inactive | Active | Inactive | TDI–(1)–SSP2–SPL–TDO |
| 0 | 0 | 1 | 1 | Inactive | Inactive | Active | Active | TDI–(1)–SSP1–(1)–SSP2–SPL–TDO |
| 0 | 1 | 0 | 0 | Inactive | Active | Inactive | Inactive | TDI–(1)–SSP3–SPL–TDO |
| 0 | 1 | 0 | 1 | Inactive | Active | Inactive | Active | TDI–(1)–SSP1–(1)–SSP3–SPL–TDO |
| 0 | 1 | 1 | 0 | Inactive | Active | Active | Inactive | TDI–(1)–SSP2–(1)–SSP3–SPL–TDO |
| 0 | 1 | 1 | 1 | Inactive | Active | Active | Active | TDI–(1)–SSP1–(1)–SSP2–(1)–SSP3–SPL–TDO |
| 1 | 0 | 0 | 0 | Active | Inactive | Inactive | Inactive | TDI–(1)–SSP4–SPL–TDO |
| 1 | 0 | 0 | 1 | Active | Inactive | Inactive | Active | TDI–(1)–SSP1–(1)–SSP4–SPL–TDO |
| 1 | 0 | 1 | 0 | Active | Inactive | Active | Inactive | TDI–(1)–SSP2–(1)–SSP4–SPL–TDO |
| 1 | 0 | 1 | 1 | Active | Inactive | Active | Active | TDI–(1)–SSP1–(1)–SSP2–(1)–SSP4–SPL–TDO |
| 1 | 1 | 0 | 0 | Active | Active | Inactive | Inactive | TDI–(1)–SSP3–(1)–SSP4–SPL–TDO |
| 1 | 1 | 0 | 1 | Active | Active | Inactive | Active | TDI–(1)–SSP1–(1)–SSP3–(1)–SSP4–SPL–TDO |
| 1 | 1 | 1 | 0 | Active | Active | Active | Inactive | TDI–(1)–SSP2–(1)–SSP3–(1)–SSP4–SPL–TDO |
| 1 | 1 | 1 | 1 | Active | Active | Active | Active | TDI–(1)–SSP1–(1)–SSP2–(1)–SSP3–(1)–SSP4–SPL–TDO |

† The scan-path configuration is the order of scan, beginning with the TDI of the 'ACT8997 and ending with the TDO of the 'ACT8997.
‡ A (1) indicates one bit of delay through the 'ACT8997. SPL indicates the selected scan register within the 'ACT8997.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, $V_{CC}$ .......... –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .......... –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) .......... –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) .......... ±20 mA
Output clamp current, $I_{OK}$ ($V_I < 0$ or $V_I > V_{CC}$) .......... ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) .......... ±25 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DW package .......... 1.7 W
NT package .......... 1.3 W
Storage temperature range, $T_{stg}$ .......... –65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

## recommended operating conditions

| | | | SN54ACT8997 | | SN74ACT8997 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | TDO, DTDO(1–4), MCO | | –7 | | –10 | mA |
| | | DTMS(1–4), DCO (3 state), DTCK | | –11 | | –16 | |
| $I_{OL}$ | Low-level output current | TDO, DTDO(1–4), MCO | | 7 | | 10 | mA |
| | | DCO (open drain or 3 state) | | 11 | | 16 | |
| | | DTMS(1–4) | | 16 | | 24 | |
| | | DTCK | | 32 | | 48 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ACT8997 | | SN74ACT8997 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | TYP† | MAX | |
| $V_{OH}$ | TDO, DTDO(1–4), MCO | $V_{CC}$ = 4.5 V | $I_{OH}$ = –7 mA | 3.6 | | | | | V |
| | | | $I_{OH}$ = –10 mA | | | 3.7 | | | |
| | DTMS(1–4), DCO (3 state), DTCK | $V_{CC}$ = 4.5 V | $I_{OH}$ = –11 mA | 3.6 | | | | | |
| | | | $I_{OH}$ = –16 mA | | | 3.7 | | | |
| $V_{OL}$ | TDO, DTDO(1–4), MCO | $V_{CC}$ = 4.5 V | $I_{OL}$ = 7 mA | | 0.5 | | | | V |
| | | | $I_{OL}$ = 10 mA | | | | | 0.5 | |
| | DCO (open drain or 3 state) | $V_{CC}$ = 4.5 V | $I_{OL}$ = 11 mA | | 0.5 | | | | |
| | | | $I_{OL}$ = 16 mA | | | | | 0.5 | |
| | DTMS(1–4) | $V_{CC}$ = 4.5 V | $I_{OL}$ = 16 mA | | 0.5 | | | | |
| | | | $I_{OL}$ = 24 mA | | | | | 0.5 | |
| | DTCK | $V_{CC}$ = 4.5 V | $I_{OL}$ = 32 mA | | 0.5 | | | | |
| | | | $I_{OL}$ = 48 mA | | | | | 0.5 | |
| $I_{OZ}$‡ | DTDO(1–4), DTMS(1–4), DCO, DTCK | $V_{CC}$ = 5.5 V, $V_O$ = $V_{CC}$ or GND | | | ±10 | | | ±5 | μA |
| $I_{OH}$ | DCO (open drain) | $V_{CC}$ = 5.5 V, $V_O$ = $V_{CC}$ | | | 20 | | | 10 | μA |
| $I_I$ | MCI, DCI, TCK, ID(1–4) | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | μA |
| | TDI, DTDI(1–4), TMS, $\overline{TRST}$ | $V_{CC}$ = 5.5 V | $V_I$ = $V_{CC}$ | | ±1 | | | ±1 | |
| | | | $V_I$ = GND | –0.1 | –20 | –0.1 | | –20 | |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | | | 100 | | | 100 | μA |
| $\Delta I_{CC}$§ | | $V_{CC}$ = 5.5 V, One input at $V_I$ = 3.4 V, Other inputs at $V_{CC}$ or GND | | | 1 | | | 1 | mA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | | | | | 6 | | pF |
| $C_o$ | DCO | $V_O$ = $V_{CC}$ or GND | | | | | 15 | | pF |
| $C_o$ | All other outputs | $V_O$ = $V_{CC}$ or GND | | | | | 10 | | pF |

† Typical values are at $V_{CC}$ = 5 V.
‡ For I/O pins, the parameter $I_{OZ}$ includes the input-leakage current. For the DCO pin, the parameter $I_{OZ}$ includes the open-drain output-leakage current.
§ This is the increase in supply current for each input being driven at TTL levels rather than $V_{CC}$ or GND.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | | | SN54ACT8997 | | SN74ACT8997 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 20 | 0 | 20 | MHz |
| | | DCI (count mode) | 0 | 20 | 0 | 20 | |
| $t_w$ | Pulse duration | TCK high or low | 12 | | 12 | | ns |
| | | DCI high or low (count mode) | 7 | | 7 | | |
| | | $\overline{TRST}$ low | 7 | | 7 | | |
| $t_{su}$ | Setup time | TMS before TCK↑ | 8 | | 8 | | ns |
| | | TDI before TCK↑ | 9 | | 9 | | |
| | | Any DTDI before TCK↑ | 7 | | 7 | | |
| | | MCI before TCK↑ | 3 | | 3 | | |
| | | DCI before TCK↑ | 3 | | 2 | | |
| | | Any ID before TCK↑ | 2 | | 2 | | |
| $t_h$ | Hold time | TMS after TCK↑ | 2 | | 2 | | ns |
| | | TDI after TCK↑ | 2 | | 2 | | |
| | | Any DTDI after TCK↑ | 2 | | 2 | | |
| | | MCI after TCK↑ | 4 | | 4 | | |
| | | DCI after TCK↑ | 4 | | 4 | | |
| | | Any ID after TCK↑ | 4 | | 4 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 100* | | 100 | | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.



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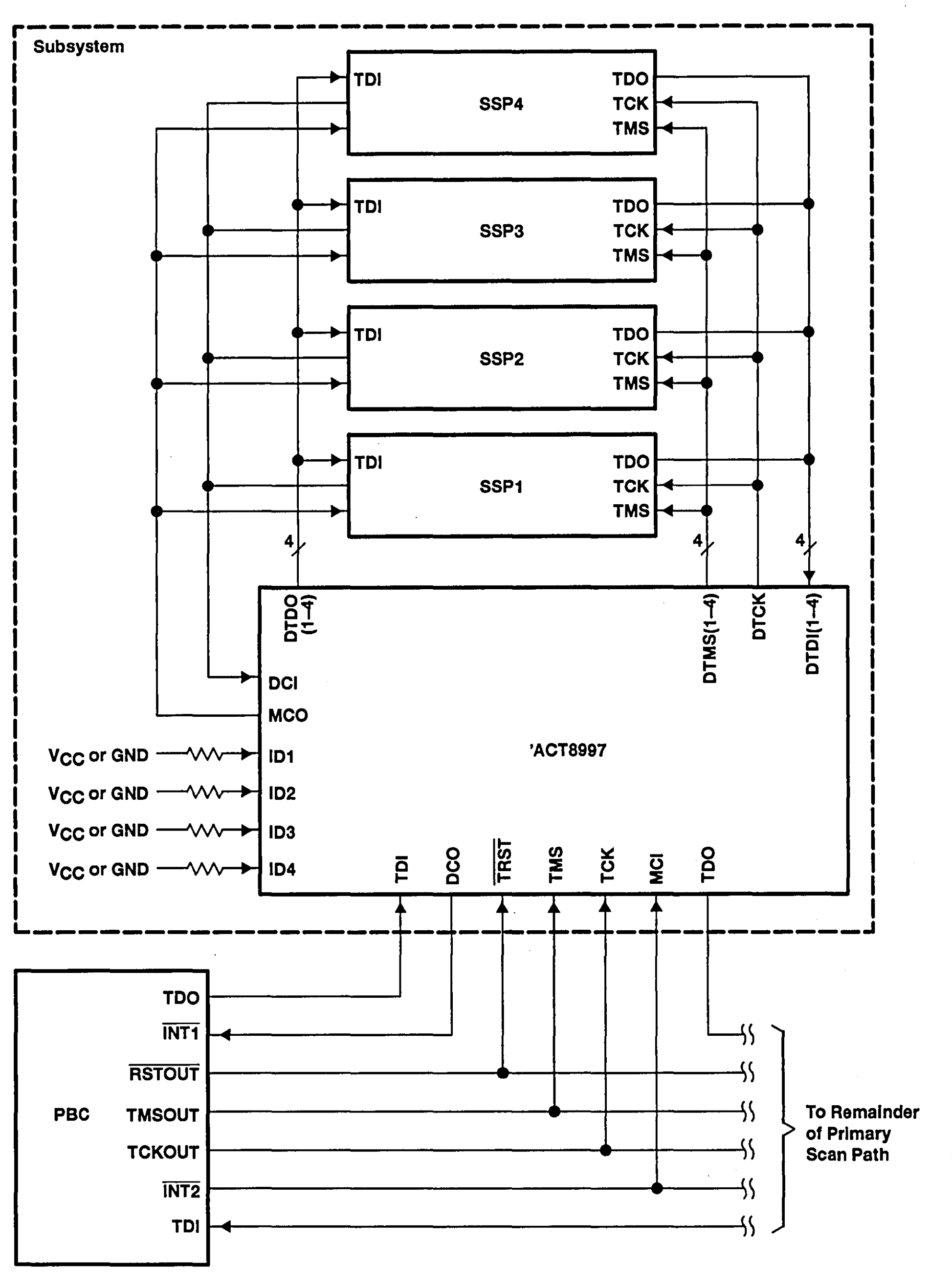
## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 9)

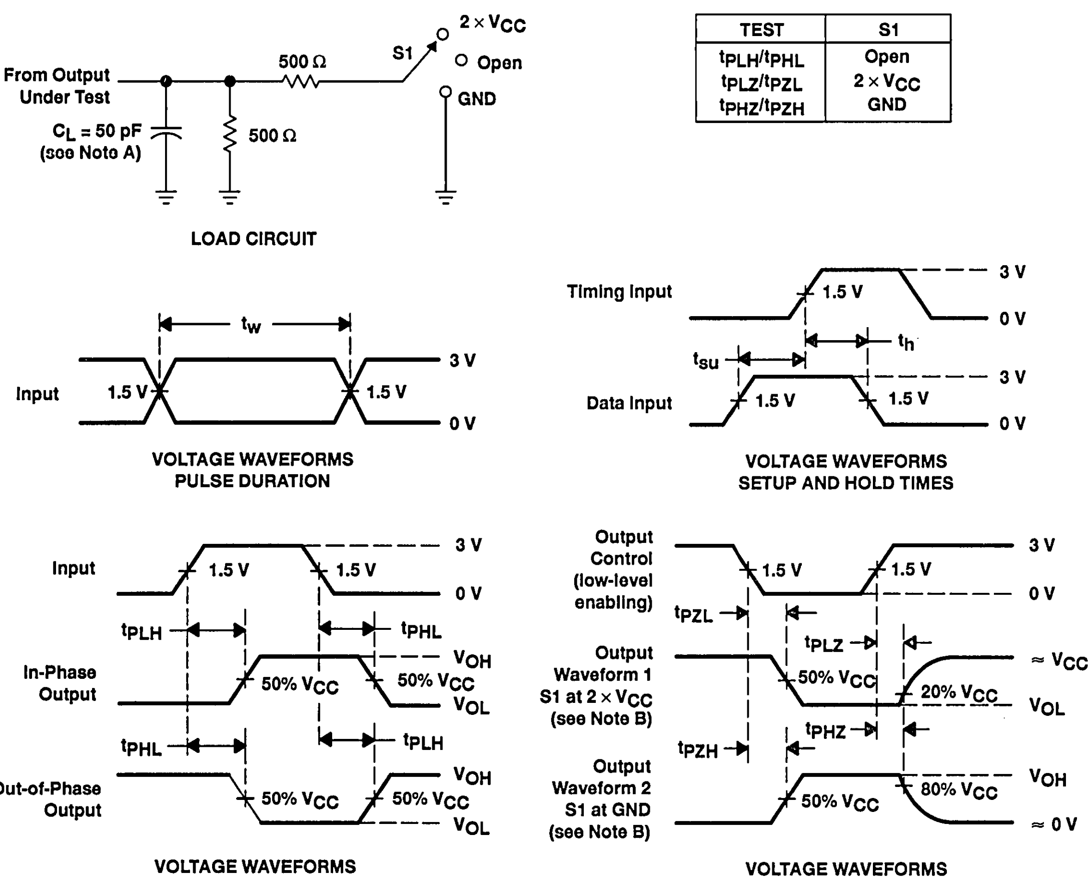
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ACT8997 | | SN74ACT8997 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 20 | | 20 | | MHz |
| | DCI (count mode) | | 20 | | 20 | | |
| $t_{PLH}$ | TCK | DTCK | 2 | 14 | 3 | 12 | ns |
| $t_{PHL}$ | | | 2 | 16 | 3 | 14 | |
| $t_{PLH}$ | TCK↓ | TDO | 7 | 28 | 9 | 25 | ns |
| $t_{PHL}$ | | | 7 | 26 | 9 | 24 | |
| $t_{PLH}$ | TCK↓ | Any DTDO | 7 | 27 | 9 | 25 | ns |
| $t_{PHL}$ | | | 7 | 26 | 9 | 24 | |
| $t_{PLH}$ | TCK↓ | Any DTMS | 9 | 31 | 11 | 29 | ns |
| $t_{PHL}$ | | | 9 | 31 | 12 | 29 | |
| $t_{PLH}$ | TCK↓ | DCO (open drain) | 9 | 33 | 12 | 31 | ns |
| | | DCO (3 state) | 9 | 32 | 12 | 30 | |
| $t_{PHL}$ | TCK↓ | DCO (open drain) | 9 | 34 | 12 | 32 | |
| | | DCO (3 state) | 9 | 31 | 12 | 29 | |
| $t_{PLH}$ | TMS | Any DTMS | 4 | 21 | 6 | 19 | ns |
| $t_{PHL}$ | | | 5 | 23 | 7 | 21 | |
| $t_{PLH}$ | MCI | MCO | 5 | 23 | 7 | 20 | ns |
| $t_{PHL}$ | | | 5 | 22 | 7 | 20 | |
| $t_{PLH}$ | DCI | DCO (open drain) | 9 | 30 | 11 | 27 | ns |
| | | DCO (3 state) | 6 | 29 | 10 | 26 | |
| $t_{PHL}$ | DCI | DCO (open drain) | 7 | 29 | 10 | 25 | |
| | | DCO (3 state) | 6 | 26 | 9 | 23 | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 17 | 5 | 15 | ns |
| $t_{PLZ}$ | | | 3 | 16 | 4 | 14 | |
| $t_{PHZ}$ | TCK↓ | Any DTDO | 5 | 19 | 5 | 17 | ns |
| $t_{PLZ}$ | | | 5 | 20 | 7 | 18 | |
| $t_{PHZ}$ | TCK↓ | Any DTMS | 6 | 23 | 7 | 21 | ns |
| $t_{PLZ}$ | | | 6 | 28 | 9 | 26 | |
| $t_{PHZ}$ | TCK↓ | DCO | 6 | 23 | 9 | 21 | ns |
| $t_{PLZ}$ | | | 6 | 24 | 9 | 22 | |
| $t_{PZH}$ | TCK↓ | TDO | 8 | 30 | 10 | 27 | ns |
| $t_{PZL}$ | | | 8 | 31 | 10 | 28 | |
| $t_{PZH}$ | TCK↓ | Any DTDO | 9 | 31 | 11 | 28 | ns |
| $t_{PZL}$ | | | 9 | 33 | 11 | 30 | |
| $t_{PZH}$ | TCK↓ | Any DTMS | 8 | 31 | 11 | 29 | ns |
| $t_{PZL}$ | | | 10 | 35 | 13 | 33 | |
| $t_{PZH}$ | TCK↓ | DCO | 9 | 37 | 14 | 35 | ns |
| $t_{PZL}$ | | | 8 | 35 | 13 | 32 | |

## APPLICATION INFORMATION



## PARAMETER MEASUREMENT INFORMATION

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

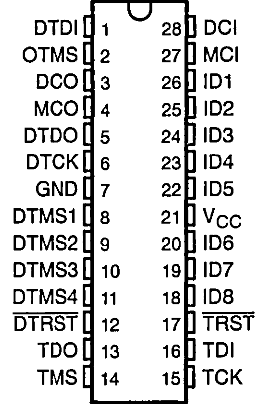



NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns. For testing pulse duration: $t_r$ = 1 to 3 ns, $t_f$ = 1 to 3 ns. Pulse polarity may be either high-to-low-to-high or a low-to-high-to-low.
D. The outputs are measured one at a time with one transition per measurement.

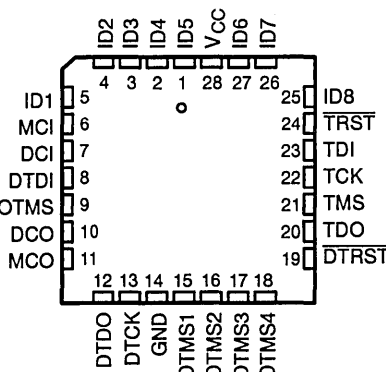
**Figure 9. Load Circuit and Voltage Waveforms**

- Members of theTexas Instruments *SCOPE*™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus
- Allow Partitioning of System Scan Paths
- Can Be Cascaded Horizontally or Vertically
- Select One of Four Secondary Scan Paths to Be Included in a Primary Scan Path
- Provide Communication Between Primary and Remote Test Bus Controllers
- Include 8-Bit Programmable Binary Counter to Count or Initiate Interrupt Signals
- Include 8-Bit Identification Bus for Scan Path Identification
- Inputs Are TTL Compatible
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

SN54ACT8999 . . . JT PACKAGE
SN74ACT8999 . . . DW OR NT PACKAGE
(TOP VIEW)




SN54ACT8999 . . . FK PACKAGE
(TOP VIEW)




## description

The 'ACT8999 are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of components facilitates testing of complex circuit-board assemblies.

The 'ACT8999 enhance the scan capability of TI's SCOPE™ family by allowing augmentation of a system's primary scan path with secondary scan paths (SSPs), which can be individually selected by the 'ACT8999 for inclusion in the primary scan path. The device also provides buffering of test signals to reduce the need for external logic.

By loading the proper values into the instruction register and data registers, the user can select one of four secondary scan paths. This has the effect of shortening the scan path to allow maximum test throughput when an individual subsystem (board or box) is to be tested. Any of the device's six data registers or the instruction register can be placed in the device's scan path, i.e., placed between test data input (TDI) and test data output (TDO) for subsequent shift and scan operations.

All operations of the device except counting are synchronous to the test clock (TCK). The 8-bit programmable up/down counter can be used to count transitions on the device condition input (DCI) and output interrupt signals via the device condition output (DCO). The device can be configured to count on either the rising or falling edge of DCI.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## description (continued)

If a system's test architecture contains more than one test bus controller, the 8-bit bidirectional bus can be used to interface a higher-level primary bus controller (PBC) with one or more lower-level remote bus controllers (RBCs). A protocol allows the PBC to pass control of the 'ACT8999 to an RBC, freeing the PBC for other tasks. The 8-bit bus also can be hardwired to provide one of 256 codes for subsystem identification. The test access port (TAP) controller is a finite-state machine compatible with IEEE Standard 1149.1.

The SN54ACT8999 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT8999 is characterized for operation from 0°C to 70°C.

## functional block diagram

$V_{CC}$
OTMS 2
$V_{CC}$
DTDI 1
$V_{CC}$
TDI 16
DCI 28
MCI 27
ID1–ID8
$V_{CC}$
TMS 14
TCK 15
$V_{CC}$
$\overline{TRST}$ 17
Remote Test Port
Test Mode Select Circuit
Data Registers
Instruction Register
Primary Test Port
8 DTMS1
9 DTMS2
10 DTMS3
11 DTMS4
5 DTDO
3 DCO (3 state or open drain)
4 MCO
13 TDO
6 DTCK
12 $\overline{DTRST}$

Pin numbers shown are for the DW, JT, and NT packages.

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## functional block description

The 'ACT8999 implements two separate functions in one package. The primary function of the device is to include a selected secondary scan path in the system's primary scan path to enable a PBC to perform controlling and observing test functions on the selected path. This is accomplished by driving the TMS terminal(s) of a secondary scan path with one of the DTMS pins of the device. This approach allows a system to have built-in testability at all levels without requiring that the primary-system scan path always include all subsystem scan paths. As a result, test throughput is improved and the amount of test data that must be interpreted is reduced. The device includes error-detection circuitry that prevents the user from inadvertently activating more than one secondary scan path at a time.

Another function of the device is provided by the 8-bit identification bus. This bus can be hardwired with pullup and pulldown resistors to supply an identification code to the test controller(s) to verify that test operations are being performed on the proper portion of the system. The bus can also transfer data and instructions to another device, such as a local or remote bus controller, and pass control of the scan-path select function to that device. This frees the primary controller to activate another secondary scan path elsewhere in the system or perform higher-level test control functions. When the RBC is ready to return control of the device, interrupt signals alert the primary controller.

The least-significant bit (LSB) of any value scanned into any register of the device is the first bit shifted in (nearest to TDO). The most-significant bit (MSB) is the last bit shifted in (nearest to TDI). The 'ACT8999 is divided into functional blocks as detailed below.

### test ports

The test ports decode the signals on TCK, TMS, OTMS, and $\overline{TRST}$ to control the operation of the circuit. Each test port includes a TAP controller that issues the proper control instructions to the data registers according to the IEEE Standard 1149.1 protocol. The TAP controller state diagram is shown in Figure 1. Two test ports are included on the 'ACT8999, allowing different test controllers to command different sections of the device.

### TMS circuit

The TMS circuit decodes bits in the select and control registers to determine which one, if any, of the DTMS pins (which provide mode-select signals to the secondary scan path(s)) follow the TMS pin or OTMS pin. The unselected DTMS pins are set by the circuit to a static high or low level.

### instruction register

The instruction register (IR) is an 8-bit-wide serial-shift register that issues commands to the device. Data is input to the instruction register via TDI or DTDI and shifted out via TDO. All device operations are initiated by loading the proper instruction or sequence of instructions into the IR.

### data registers

Six parallel data registers are included in the 'ACT8999: bypass, control, counter, boundary-scan, ID-bus, and select. The ID bus register is a part of the boundary-scan register. Each data register is serially loaded via TDI or DTDI and outputs data via TDO. Table 1 summarizes the registers in the 'ACT8999.

**Table 1. Register Summary**

| REGISTER NAME | LENGTH (BITS) | FUNCTION |
|---|---|---|
| Instruction | 8 | Issue command information to the device |
| Remote Instruction | 8 | Issue command information to the select register |
| Control | 13 | Configuration and enable control |
| Counter | 8 | Count events on DCI, output interrupts via DCO |
| Select | 8 | Select one of four DTMS pins to follow TMS or OTMS |
| Boundary Scan | 15 | Capture and force test data at device periphery |
| ID Bus | 8 | Pass test commands and data between a PBC and RBC(s) |
| Bypass | 1 | Remove the 'ACT8999 from the scan path |

## Terminal Functions

| TERMINAL NAME | I/O | DESCRIPTION |
|---|---|---|
| DCI | I | Device condition input. DCI receives interrupt and protocol signals from an RBC and/or the secondary scan path(s). When the counter register is instructed to count up or down, DCI is configured as the counter clock. |
| DCO | O | Device condition output. DCO is configured by the control register to output protocol and interrupt signals to a PBC. It also can be configured by the control register to output an error signal if the instruction register or select register are loaded with invalid values. DCO is further configured by the control register as:<br>Active high or active low (reset condition = active low)<br>Open drain or 3-state (reset condition = open drain) |
| DTCK | O | Device test clock. DTCK outputs the buffered test clock TCK to the secondary scan path(s). |
| DTDI | I | Device test data input. DTDI receives the serial test data output of the selected secondary scan path. An internal pullup forces DTDI to a high logic level if it is left unconnected. |
| DTDO | O | Device test data output. DTDO outputs serial test data to the TDI input(s) of the secondary scan path(s). |
| DTMS1<br>DTMS2<br>DTMS3<br>DTMS4 | O | Device test mode select 1–4. Either one or none of these four outputs can be selected to follow TMS or OTMS to include a secondary scan path in the primary scan path. The unselected DTMS outputs can be independently set to a static high or low logic level. The TMS circuit monitors input from the select register to determine the configuration of the DTMS outputs. |
| $\overline{\text{DTRST}}$ | O | Device test reset. This active-low output transmits a reset signal to the secondary scan path(s). $\overline{\text{DTRST}}$ can be asserted by a bit in the control register or by setting $\overline{\text{TRST}}$ low. |
| GND | | Ground |
| ID1<br>ID2<br>ID3<br>ID4<br>ID5<br>ID6<br>ID7<br>ID8 | I/O | Identification 1–8. This 8-bit data bus can be used to communicate with an RBC and pass data and control instructions. By wiring pullup and pulldown resistors to these terminals, one of 255 unique identification codes can be assigned to the device to allow a test controller to determine the identity of the subsystem under test. |
| MCI | I | Master condition input. MCI receives interrupt and protocol singals from a PBC. |
| MCO | O | Master condition output. MCO transmits interrupt and protocol signals to an RBC and/or the secondary scan path(s). MCO also outputs an active-low error signal during the Pause-DR TAP state if an RBC loads an invalid value in the select register. |
| OTMS | I | Optional test mode select. OTMS can be used instead of TMS to control the select register. This is useful when a remote bus controller is available to control the secondary scan path(s). An internal pullup forces OTMS to a high level if left unconnected. |
| TCK | I | Test clock. One of four terminals required by IEEE Standard 1149.1. All operations of the 'ACT8999 except for the count function are synchronous to TCK. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK. |
| TDI | I | Test data input. One of four terminals required by IEEE Standard 1149.1. TDI is the serial input for shifting information into the instruction register or selected data register. TDI is typically driven by the TDO output of the primary bus controller. An internal pullup forces TDI to a high level if it is left unconnected. |
| TDO | O | Test data output. One of four terminals required by IEEE Standard 1149.1. TDO is the serial output for shifting information out of the instruction register or selected data register. TDO is typically connected to the TDI input of the next scannable device in the primary scan path. |
| TMS | I | Test mode select. One of four terminals required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the 'ACT8999 through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $\overline{\text{TRST}}$ | I | Test reset. This active-low input inplements the optional reset terminal of IEEE Standard 1149.1. When asserted, $\overline{\text{TRST}}$ causes the 'ACT8999 to go to the Test-Logic-Reset state and configure the instruction register and data registers to their power-up values. $\overline{\text{TRST}}$ is also output without inversion via $\overline{\text{DTRST}}$. An internal pullup forces $\overline{\text{TRST}}$ to a high level if left unconnected. |
| $V_{CC}$ | | Supply voltage |

## state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. No more than one register can be manipulated at a time.

Test-Logic-Reset
TMS = H
TMS = L
TMS = H
Run-Test/Idle
TMS = L
TMS = H
Select-DR-Scan
TMS = H
Select-IR-Scan
TMS = L
TMS = L
Capture-DR
TMS = H
TMS = H
Capture-IR
TMS = L
TMS = L
Shift-DR
TMS = L
Shift-IR
TMS = L
TMS = H
TMS = H
TMS = H
Exit1-DR
Exit1-IR
TMS = H
TMS = L
TMS = L
Pause-DR
TMS = L
Pause-IR
TMS = L
TMS = H
TMS = L
TMS = L
TMS = H
Exit2-DR
Exit2-IR
TMS = H
TMS = H
Update-DR
Update-IR
TMS = H
TMS = L
TMS = H
TMS = L

**Figure 1. TAP-Controller State Diagram**

### Test-Logic-Reset

In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if the test mode select (TMS) input is high. The TMS pin has an internal pullup that forces it to a high level if it is left unconnected or if a board defect causes it to be open circuited. The device powers up in the Test-Logic-Reset state.

### Run-Test/Idle

The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle. The 8-bit programmable up/down counter can be operated in this state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states; the TAP exits either of them on the next TCK cycle.

### Capture-DR

The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK, causing the TAP state to change.

### Shift-DR

In this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). On the falling edge of TCK in Shift-DR, TDO goes from the high-impedance state to the active state. TDO enables to the value present in the least-significant bit of the selected data register.

### Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR. TDO changes from the active state to the high-impedance state on the falling edge of TCK in Exit1-DR.

### Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state suspends and resumes shift operations without loss of data.

### Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated only during this state.

### Capture-IR

The instruction register is preloaded with the IR status word (see Table 4) and placed in the scan path.

### Shift-IR

In this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state, and will enable to a high level.

**Exit1-IR, Exit2-IR**

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR. TDO changes from the active state to the high-impedance state on the falling edge of TCK in Exit1-IR.

**Pause-IR**

The TAP can remain in this state indefinitely. The Pause-IR state suspends and resumes shift operations without loss of data.

**Update-IR**

In this state, the latches shadowing the instruction register are updated with the new instruction.

## instruction register description

The instruction register (IR) is an 8-bit serial register that outputs control signals to the device. Table 2 lists the instructions implemented in the 'ACT8999 and the data register selected by each instruction. The MSB of the IR is an even-parity bit. If the value scanned into the IR during Shift-IR does not contain even parity, an error signal ($\overline{\text{IRERR}}$) is generated internally as shown in Table 3. The 'ACT8999 can be configured to output $\overline{\text{IRERR}}$ via DCO if the TAP enters the Pause-IR state.

During the Capture-IR state, the IR status word is loaded. The IR status word contains information about the most recently loaded values of the instruction and select registers and the logic level present at the DCI input. The IR status word is encoded as shown in Table 4. Figure 2 shows the order of scan for the IR.

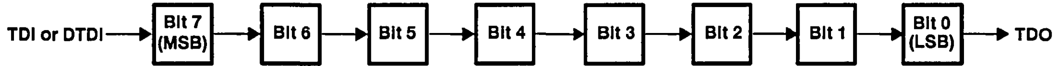



**Figure 2. Instruction-Register Bits and Order of Scan**

### Table 2. Instruction-Register Opcodes

| BINARY CODE BIT 7 → BIT 0 MSB → LSB | HEX VALUE | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|---|
| 00000000 | 00 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | 81 | BYPASS | Bypass scan | Bypass | Normal |
| 10000010 | 82 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | 03 | INTEST | Boundary scan | Boundary scan | Test |
| 10000100 | 84 | BYPASS† | Bypass scan | Bypass | Normal |
| 00000101 | 05 | BYPASS† | Bypass scan | Bypass | Normal |
| 00000110 | 06 | BYPASS† | Bypass scan | Bypass | Normal |
| 10000111 | 87 | BYPASS† | Bypass scan | Bypass | Normal |
| 10001000 | 88 | COUNT | Count | Bypass | Normal |
| 00001001 | 09 | COUNT | Count | Bypass | Normal |
| 00001010 | 0A | BYPASS† | Bypass scan | Bypass | Normal |
| 10001011 | 8B | BYPASS† | Bypass scan | Bypass | Normal |
| 00001100 | 0C | BYPASS† | Bypass scan | Bypass | Normal |
| 10001101 | 8D | BYPASS | Bypass scan | Bypass | Normal |
| 10001110 | 8E | SCANCN | Control register scan | Control | Normal |
| 00001111 | 0F | SCANCN | Control register scan | Control | Normal |
| 11111010 | FA | SCANCNT | Counter scan | Counter | Normal |
| 01111011 | 7B | READCNT | Counter read | Counter | Normal |
| 11111100 | FC | SCANIDB | ID bus register scan | ID bus | Normal |
| 01111101 | 7D | READIDB | ID bus register read | ID bus | Normal |
| 01111110 | 7E | SCANSEL | Select register scan | Select | Normal |
| All others | | BYPASS | Bypass scan | Bypass | Normal |

† A SCOPE opcode exists but is not supported by the 'ACT8999.

### Table 3. $\overline{\text{IRERR}}$ Function Table

| NO. OF INSTRUCTION REGISTER BITS = 1 | $\overline{\text{IRERR}}$ |
|---|---|
| 0, 2, 4, 6, 8 | 1 |
| 1, 3, 5, 7 | 0 |

### Table 4. Instruction-Register Status Word

| IR BIT | VALUE‡ |
|---|---|
| 7 | $\overline{\text{IRERR}}$ (see Table 3) |
| 6 | 0 |
| 5 | 0 |
| 4 | 0 |
| 3 | Level present at DCI input (1 = H, 0 = L) |
| 2 | $\overline{\text{SRERR}}$ (see Table 8) |
| 1 | 0 |
| 0 | 1 |

‡ This value is loaded in the instruction register during the Capture-IR TAP state.

## instruction-register opcode description

The operation of the 'ACT8999 is dependent on the instruction loaded into the instruction register. Each instruction selects one of the data registers to be placed between TDI or DTDI and TDO during the Shift-DR TAP state. All the required instructions of IEEE Standard 1149.1 are implemented in the 'ACT8999.

### boundary scan

This instruction implements the required EXTEST and optional INTEST operations of IEEE Standard 1149.1. The boundary-scan register (which includes the ID-bus register) is placed in the scan path. Data appearing at input pins included in the boundary-scan register is captured. Data previously loaded into the output pins included in the boundary-scan register is forced through the outputs.

### bypass scan

This instruction implements the required BYPASS operation of IEEE Standard 1149.1. The bypass register is placed in the scan path and preloads with a logic 0 during Capture-DR.

### sample boundary

This instruction implements the required SAMPLE/PRELOAD operation of IEEE Standard 1149.1. The boundary-scan register is placed in the scan path, and data appearing at the inputs and outputs included in the boundary-scan register is sampled on the rising edge of TCK in Capture-DR.

### count

The counter register begins counting on each DCI transition. The count begins from the value present in the register before the count instruction was loaded. The counter can be configured by the control register to count up or down on either the low-to-high or high-to-low transition of DCI. Counting occurs only while in the Run-Test/Idle TAP state.

### control-register scan

The control register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

### counter-register scan

The counter register is placed in the scan path. During Capture-DR, the current value of the counter is loaded in the counter register. At Update-DR, the newly shifted value is preloaded to the counter.

### counter-register read

The counter register is placed in the scan path. During Capture-DR, the prior preload value of the counter is loaded into the counter register. At Update-DR, the newly shifted value is preloaded to the counter.

### ID-bus-register scan

The ID-bus register (a subset of the boundary-scan register) is placed in the scan path for a subsequent shift operation. The data appearing on the ID bus is loaded into the ID-bus register on the rising edge of TCK in Capture-DR.

### ID-bus register read

The ID-bus register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

### select-register scan

The select register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

## control-register description

The control register (CTLR) is a 13-bit serial register that controls the enable and select functions of the 'ACT8999. A reset operation forces all bits to a logic 0. The contents of the control register are latched and decoded during the Update-DR TAP state. The specific function of each bit is listed in Table 5. The enable and select functions of the control register bits are mapped as follows:

**Table 5. Control-Register Bit Mapping**

| BIT | VALUE | FUNCTION |
|---|---|---|
| 12 | 0 | Configure counter to count up |
| | 1 | Configure counter to count down |
| 11 | 0 | Do not stop counting when the count reaches 00000000 |
| | 1 | Stop counting when the count reaches 00000000 (count down only) |
| 10 | 0 | Configure DCO as an active-low output |
| | 1 | Configure DCO as an active-high output |
| 9, 8 | 00 | DCO = Inactive (level depends on CTLR bit 10) |
| | 01 | DCO = ($\overline{IRERR}$ • $\overline{SRERR}$) |
| | 10 | DCO = $\overline{CE}$, an internal logic 0 generated when the count is 00000000 (count down) or 11111111 (count up) |
| | 11 | DCO = DCI |
| 7 | 0 | Do not mask $\overline{IRERR}$ and $\overline{SRERR}$ from DCO |
| | 1 | Mask $\overline{IRERR}$ and $\overline{SRERR}$ from DCO |
| 6 | 0 | Configure DCO as an open-drain output |
| | 1 | Configure DCO as a 3-state output |
| 5 | 0 | Disable DCO |
| | 1 | Enable DCO |
| 4 | 0 | Configure DCI as an active-low input |
| | 1 | Configure DCI as an active-high input |
| 3 | 0 | Enable DTCK, DTDO, and DTMS(1–4) |
| | 1 | Disable DTCK, DTDO, and DTMS(1–4) |
| 2 | 0 | Disable ID(1–8) |
| | 1 | Enable ID(1–8) |
| 1 | 0 | Disable RBC |
| | 1 | Enable RBC |
| 0 | 0 | $\overline{DTRST}$ = $\overline{TRST}$ |
| | 1 | $\overline{DTRST}$ = L |

### Bit 12 – $\overline{Up}$/Down

This bit sets the count mode of the counter register (reset condition = count up).

### Bit 11 – Latch on Zero

The counter register can be configured to stop counting when its value is 00000000 and ignore subsequent transitions on the counter clock, DCI. The latch-on-zero option is valid only in the count-down mode (reset condition = do not latch on zero). The value of this bit has no effect on the operation of the counter if CTLR bit 12 = 0.

### Bit 10 – DCO Polarity Select

DCO can be configured as an active-low or active-high output (reset condition = active low).

**Bit 9/Bit 8 – DCO Source Select 1/DCO Source Select 0**

DCO can be used to output two error signals generated by the 'ACT8999: $\overline{\text{IRERR}}$ (see Table 3) and $\overline{\text{SRERR}}$ (see Table 8). Bits 9 and 8 can be set to output $\overline{\text{IRERR}}$ via DCO on the falling edge of TCK in the Pause-IR state and $\overline{\text{SRERR}}$ via DCO on the falling edge of TCK in the Pause-DR state. DCO also can be configured to become active when the value of the counter is 00000000, to follow DCI, or be set to a static high or low level (reset condition = static high level).

**Bit 7 – Parity Mask**

The internal error signals can be masked from appearing on DCO even if bits 9 and 8 are set such that $\overline{\text{IRERR}}$ and $\overline{\text{SRERR}}$ are output in the Pause-IR and Pause-DR states (reset condition = do not mask $\overline{\text{IRERR}}$ or $\overline{\text{SRERR}}$).

**Bit 6 – DCO Drive Select**

DCO can be configured as either an open-drain or 3-state output (reset condition = open drain). The open-drain configuration allows multiple DCO outputs to be used in a wired-OR or wired-AND application. The 3-state configuration allows the DCO output to be connected to a bus.

**Bit 5 – DCO Enable**

When configured as a 3-state output, DCO can be placed in the high-impedance state (reset condition = disabled). If configured as an open-drain output and disabled, DCO outputs a high level.

**Bit 4 – DCI Polarity Select**

DCI can be configured as an active-low or active-high input (reset condition = active low).

**Bit 3 – Device Test Pins Output Enable (active low)**

DTCK, DTDO, and DTMS(1–4) pins can be placed in the high-impedance state (disabled) with this bit (reset condition = enabled).

**Bit 2 – ID Bus Enable**

The ID bus (ID1–8) is a bidirectional bus. The output buffers are enabled and disabled with this bit (reset condition = output buffers disabled).

**Bit 1 – Remote-Bus-Controller (RBC) Enable**

An RBC can issue protocol and data instructions to the select register if the 'ACT8999 is configured to allow it (reset condition = RBC disabled). When an RBC is enabled, the TAP in the select register operates according to the OTMS signal.

**Bit 0 – Device Test Reset**

$\overline{\text{DTRST}}$ can be configured to output a reset signal independently of the level on $\overline{\text{TRST}}$ (reset condition = no reset signal issued).

Several control-register bits affect the functionality of the DCO output. The DCO function table is given in Table 6. Figure 3 shows the order of scan for the control register.

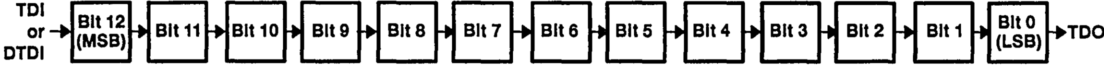



**Figure 3. Control-Register Bits and Order of Scan**

**Table 6. DCO Function Table**

| DCI | INTERNAL SIGNALS† | | | CONTROL REGISTER BITS‡ | | | | | | | DCO |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{IRERR}$ | $\overline{SRERR}$ | $\overline{CE}$ | BIT 10 | BIT 9 | BIT 8 | BIT 7 | BIT 6 | BIT 5 | BIT 4 | |
| X | X | X | X | X | X | X | X | 0 | 0 | X | H |
| X | X | X | X | X | X | X | X | 1 | 0 | X | Z |
| X | X | X | X | 0 | 0 | 0 | X | X | 1 | X | H |
| X | X | X | X | 1 | 0 | 0 | X | X | 1 | X | L |
| X | X | X | X | 0 | 0 | 1 | 1 | X | 1 | X | H |
| X | X | X | X | 1 | 0 | 1 | 1 | X | 1 | X | L |
| X | 0 | X | X | 0 | 0 | 1 | 0 | X | 1 | X | L in Pause-IR§, H otherwise |
| X | X | 0 | X | 0 | 0 | 1 | 0 | X | 1 | X | L in Pause-DR§, H otherwise |
| X | 1 | 1 | X | 0 | 0 | 1 | 0 | X | 1 | X | H |
| X | 0 | X | X | 1 | 0 | 1 | 0 | X | 1 | X | H in Pause-IR§, L otherwise |
| X | X | 0 | X | 1 | 0 | 1 | 0 | X | 1 | X | H in Pause-DR§, L otherwise |
| X | 1 | 1 | X | 1 | 0 | 1 | 0 | X | 1 | X | L |
| X | X | X | 0 | 0 | 1 | 0 | X | X | 1 | X | L |
| X | X | X | 0 | 1 | 1 | 0 | X | X | 1 | X | H |
| X | X | X | 1 | 0 | 1 | 0 | X | X | 1 | X | H |
| X | X | X | 1 | 1 | 1 | 0 | X | X | 1 | X | L |
| L | X | X | X | 1 | 1 | 1 | X | X | 1 | 0 | H |
| L | X | X | X | 1 | 1 | 1 | X | X | 1 | 1 | L |
| L | X | X | X | 0 | 1 | 1 | X | X | 1 | 0 | L |
| L | X | X | X | 0 | 1 | 1 | X | X | 1 | 1 | H |
| H | X | X | X | 1 | 1 | 1 | X | X | 1 | 0 | L |
| H | X | X | X | 1 | 1 | 1 | X | X | 1 | 1 | H |
| H | X | X | X | 0 | 1 | 1 | X | X | 1 | 0 | H |
| H | X | X | X | 0 | 1 | 1 | X | X | 1 | 1 | L |

† These signals are generated as described elsewhere in this data sheet.
‡ The control register must contain these values after the TAP has passed through its most recent Update-DR state.
§ DCO becomes active on the falling edge of TCK as the TAP enters the appropriate pause state (Pause-IR or Pause-DR) and becomes inactive on the falling edge of TCK as the TAP enters the appropriate exit2 state (Exit2-IR or Exit2-DR).

## select register description

The select register (SR) is an 8-bit serial register that determines which one, if any, of the DTMS lines follows the TMS or OTMS input. A reset operation forces all bits to a logic 0. The register is divided into four 2-bit sections, each of which controls one DTMS output. Figure 4 shows the mapping of the bits to the DTMS outputs and the order of scan. For each DTMS pin, the higher-order bit is the MSB and the lower-order bit is the LSB (e.g., bit 3 is the MSB of DTMS2 and bit 2 is the LSB of DTMS2).

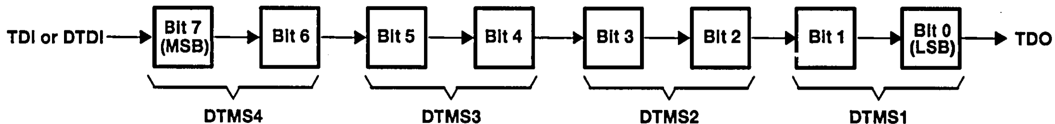



**Figure 4. Select Register Bits and Order of Scan**

### select register description (continued)

Only one of the four DTMS outputs can be selected to drive a secondary scan path with TMS or OTMS. If the SR is loaded with an invalid value, an error signal ($\overline{SRERR}$) is generated internally as shown in Table 8. If the TAP enters the Pause-DR state, $\overline{SRERR}$ may be output via DCO (see Table 8). If the TAP enters the Update-DR state while an invalid value is in the SR, all four DTMS outputs are set to a high level.

When a new 8-bit value is loaded into the SR, the configuration of one or more DTMS pins may change. If the new value of the SR configures a DTMS pin to a static (high or low) level, it assumes that level on the falling edge of TCK in the Update-DR TAP state. This condition is independent of any previous SR configurations. If the new value of the SR forces a DTMS pin to follow TMS (i.e., select a single secondary scan path) and a DTMS pin is currently in the TMS/OTMS-follow mode, the transfer of the DTMS line occurs on the falling edge of TCK in the Update-DR TAP state. However, if the new configuration forces a DTMS pin to follow TMS/OTMS while no other DTMS pin is selected, the DTMS pin does begin following TMS/OTMS until the falling edge of TCK in the Run-Test/Idle TAP state; therefore, when an SSP is initially selected, the TAP state should travel from Update-DR to Run-Test/Idle, not from Update-DR to Select-DR-Scan. Additionally, when deselecting from any DTMS output the TAP state must proceed back through Capture-DR to fully disconnect from SSP operations.

The SR can also be accessed from an RBC. A test port in the register contains a TAP that can be enabled by the control register to monitor the values of TCK and OTMS to perform scan operations on the SR. The SR bit decoding is shown in Table 7.

**Table 7. Select-Register Bit Decoding**

| MSB | LSB | DTMS SOURCE |
|---|---|---|
| 0 | 0 | H |
| 0 | 1 | L |
| 1 | 0 | OTMS |
| 1 | 1 | TMS |

**Table 8. $\overline{SRERR}$ Function Table**

| SELECT REGISTER BITS | | | | | | | | $\overline{SRERR}$ |
|---|---|---|---|---|---|---|---|---|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| 0 | X | 0 | X | 0 | X | 0 | X | 1 |
| 1 | X | 0 | X | 0 | X | 0 | X | 1 |
| 0 | X | 1 | X | 0 | X | 0 | X | 1 |
| 0 | X | 0 | X | 1 | X | 0 | X | 1 |
| 0 | X | 0 | X | 0 | X | 1 | X | 1 |
| 1 | X | 1 | X | X | X | X | X | 0 |
| 1 | X | X | X | 1 | X | X | X | 0 |
| 1 | X | X | X | X | X | 1 | X | 0 |
| X | X | 1 | X | 1 | X | X | X | 0 |
| X | X | 1 | X | X | X | 1 | X | 0 |
| X | X | X | X | 1 | X | 1 | X | 0 |

## boundary-scan register/ID-bus register description

The boundary-scan register (BSR) is a 15-bit serial register that can be used to capture data appearing at selected device inputs, force data through device outputs, and apply data to the device's internal logic. The BSR is made up of boundary-scan cells (BSCs). Table 9 lists the device signal for each of the 15 BSCs that comprise the BSR. A reset operation does not affect the contents of the BSR.

**Table 9. Boundary-Scan Register Bit Mapping**

| BIT | TERMINAL NAME | SIGNAL DESCRIPTION |
|---|---|---|
| 14 | MCI | Master condition in |
| 13 | MCO | Master condition out |
| 12 | DCI | Device condition in |
| 11 | $\overline{\text{DCOTS}}$† | Enable control for DCO in 3-state configuration (active low) |
| 10 | $\overline{\text{DCOOD}}$† | Enable control for DCO in open-drain configuration (active low) |
| 9 | DCO | Device condition out |
| 8 | $\overline{\text{IDBOE}}$† | Enable control for ID bus (active low) |
| 7 | ID8 | Identification bus bit 8 |
| 6 | ID7 | Identification bus bit 7 |
| 5 | ID6 | Identification bus bit 6 |
| 4 | ID5 | Identification bus bit 5 |
| 3 | ID4 | Identification bus bit 4 |
| 2 | ID3 | Identification bus bit 3 |
| 1 | ID2 | Identification bus bit 2 |
| 0 | ID1 | Identification bus bit 1 |

† This internal signal cannot be observed from the I/O pins of the device.

The eight BSCs connected to the ID(1–8) pins form a subset of the BSR called the ID-bus register (IDBR). The IDBR can be scanned without accessing the remaining BSCs of the BSR. The IDBR is used when the ID bus is enabled to allow communication between a PBC and one or more RBCs. Figure 5 shows the order of scan for the BSR and IDBR.

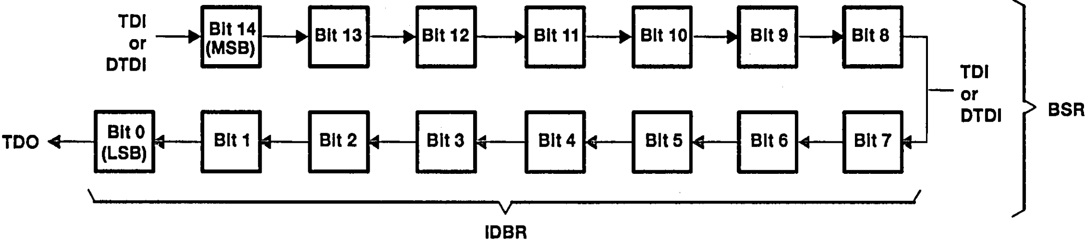



**Figure 5. Boundary-Scan Register Bits and Order of Scan**

## bypass register description

The bypass register (BR) is a 1-bit serial register. The function of the BR is to provide a means of effectively removing the 'ACT8999 from the primary scan path when it is not needed for the current test operation or other function of the PBC. A selected secondary scan path remains active in the primary scan path as described in the data flow description. At power up, the BR is placed in the scan path. Figure 6 shows the order of scan for the bypass register.

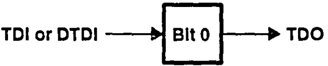



**Figure 6. Bypass-Register Bit and Order of Scan**

## counter register description

The counter register (CNTR) is an 8-bit serial register and an associated 8-bit parallel-load up/down counter. A reset operation forces all bits of the shift register to logic 0 but does not affect the counter. The counter can be preloaded with an initial value before counting begins, and the current value of the counter can be scanned out via the shift register. The CNTR can be used to count events occurring on the secondary scan path(s) using DCI as a counter clock and can output interrupt signals via DCO when the count has reached its end value.

An internal signal, $\overline{CE}$, is generated as a logic 0 when the count reaches its end value (i.e., 00000000 for count down, 11111111 for count up). For any other count value, $\overline{CE}$ is a logic 1. Many of the features of the CNTR are configured by a bit in the CTLR, including:

- Count direction up or down (control register bit 12; reset condition count up)
- Stop counting upon counting down to 00000000 (control register bit 11; reset condition = do not latch on zero)
- Output $\overline{CE}$ signals at DCO (control register bits 8 and 9; reset condition = do not output $\overline{CE}$ at DCO)
- Edge of DCI on which to trigger (control register bit 4, reset condition = positive edge)

Figure 7 shows the order of scan for the CNTR.

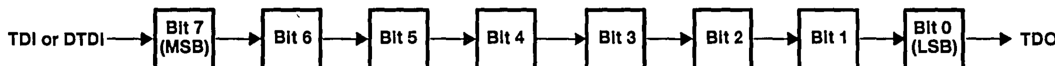



**Figure 7. Counter-Register Bits and Order of Scan**

### enabling a remote bus controller

Bit 1 in the control register allows a remote bus controller to control parts of the 'ACT8999. When an RBC is enabled, the remote test port (RTP) in the select register is activated. The RTP operates according to the same state diagram as the primary test port but only has access to the select register. Operation of the RTP is synchronous to TCK. OTMS is the RTP mode-select pin.

The RTP contains an 8-bit instruction register. Data is shifted in via DTDI and shifted out via DTDO. As shown in Table 10, only one instruction selects something other than the bypass register to be included in the scan path. When SCANSEL is executed, the select register is placed between DTDI and DTDO. The function of the select register and the decoding of the select register bits by the TMS circuit is identical, regardless of which test port accesses the register.

**Table 10. Remote-Test-Port Instruction-Register Opcodes**

| BINARY CODE BIT 7 → BIT 0 MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER |
|---|---|---|---|
| 01111110 | SCANSEL | Select-register scan | Select |
| All other | BYPASS | Bypass scan | Bypass |

An internal error signal ($\overline{RSRERR}$) is generated if an RBC loads an invalid value in the select register, and the MCO output goes low if the $\overline{RSRERR}$ is active and the remote TAP enters the Pause-DR state. The function table for $\overline{RSRERR}$ is shown in Table 11.

**Table 11. $\overline{RSRERR}$ Function Table**

| SELECT REGISTER BITS | | | | | | | | $\overline{RSRERR}$ | MCO† |
|---|---|---|---|---|---|---|---|---|---|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | | |
| 0 | X | 0 | X | 0 | X | 0 | X | 1 | MCI |
| 1 | X | 0 | X | 0 | X | 0 | X | 1 | MCI |
| 0 | X | 1 | X | 0 | X | 0 | X | 1 | MCI |
| 0 | X | 0 | X | 1 | X | 0 | X | 1 | MCI |
| 0 | X | 0 | X | 0 | X | 1 | X | 1 | MCI |
| 1 | X | 1 | X | X | X | X | X | 0 | L |
| 1 | X | X | X | 1 | X | X | X | 0 | L |
| 1 | X | X | X | X | X | 1 | X | 0 | L |
| X | X | 1 | X | 1 | X | X | X | 0 | L |
| X | X | 1 | X | X | X | 1 | X | 0 | L |
| X | X | X | X | 1 | X | 1 | X | 0 | L |

† This table is valid only when the remote TAP is in the Pause-DR state. Under any other condition, MCO = MCI.

The RTP does not have access to the control register, so it cannot disable itself. The PBC must reset bit 1 in the control register to return control of the select register to the primary test port.

## data flow description

The direction of serial data flow in the 'ACT8999 is dependent on the current instruction. Figure 8 shows the data flow for the different operating modes of the device. When a secondary scan path is selected, the 'ACT8999 adds one bit of delay from TDI to DTDO.

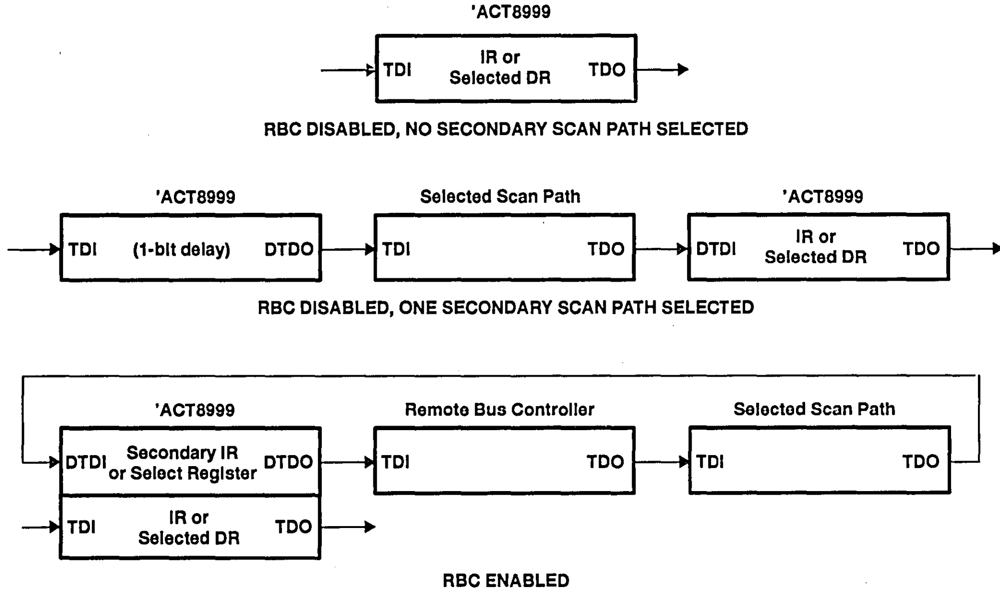



**Figure 8. Data Flow in the 'ACT8999**

## bus-communication protocol

The 8-bit identification bus [ID(1–8)] allows data transfer between a PBC and an RBC. Control register bit 2 configures the 'ACT8999 to transmit or receive command and test data via the IDBR. The DCI, DCO, MCI, and MCO pins are used to signal the PBC and RBC(s) that a data transfer is required. The 'ACT8999 can accommodate either local or global handshake protocol, depending on the number of DCO inputs that the PBC can accommodate.

Figure 9 shows a protocol for local communication between the PBC and an RBC. In this mode, communication is initiated by the PBC by driving the MCI input of the 'ACT8999 to a low level. MCI is buffered and output on MCO, which notifies the RBC that control of a scan path is to be relinquished. Prior to activating the MCI signal, the PBC scans the value 00000000 into the IDBR and enables the output buffers of ID(1–8). When the RBC recognizes that MCO has gone low, it samples the ID bus and looks for the 00000000 value to verify that the PBC is going to issue further commands. Upon verifying the value on the ID bus, the RBC drives DCI low, which is buffered and output via DCO. (In this example, DCI is configured as noninverting and DCO is configured as active low). When the PBC sees that DCO is active, it takes MCI high, forcing MCO high. When the RBC sees that MCO is high, it takes DCO high (inactive) completing one handshake cycle. A similar operation can ensue when the RBC initiates communication with the PBC as shown in Figure 9. Commands and test data can be exchanged between two bus controllers via the ID bus.

Figure 10 shows one way of using the ID bus to interface a PBC to multiple RBCs. The timing is similar to the local communication example in Figure 9, except that the PBC waits for all RBCs to acknowledge transmissions before switching MCI.

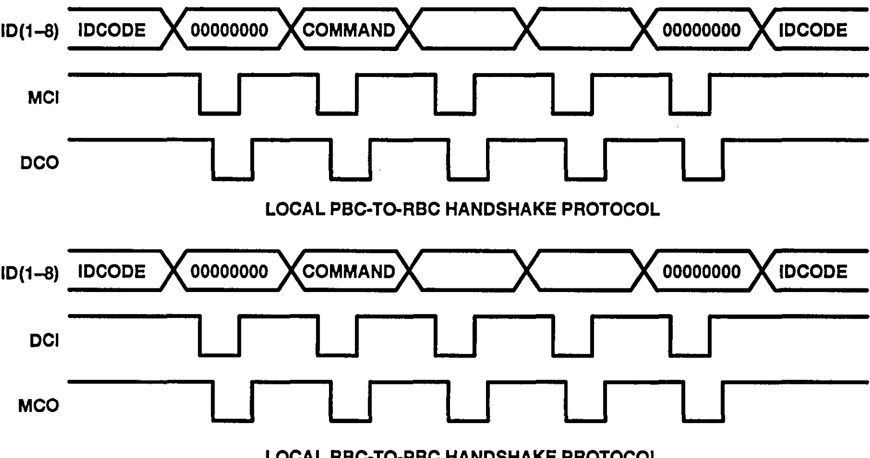



**Figure 9. Local Bus-Communication Protocol**

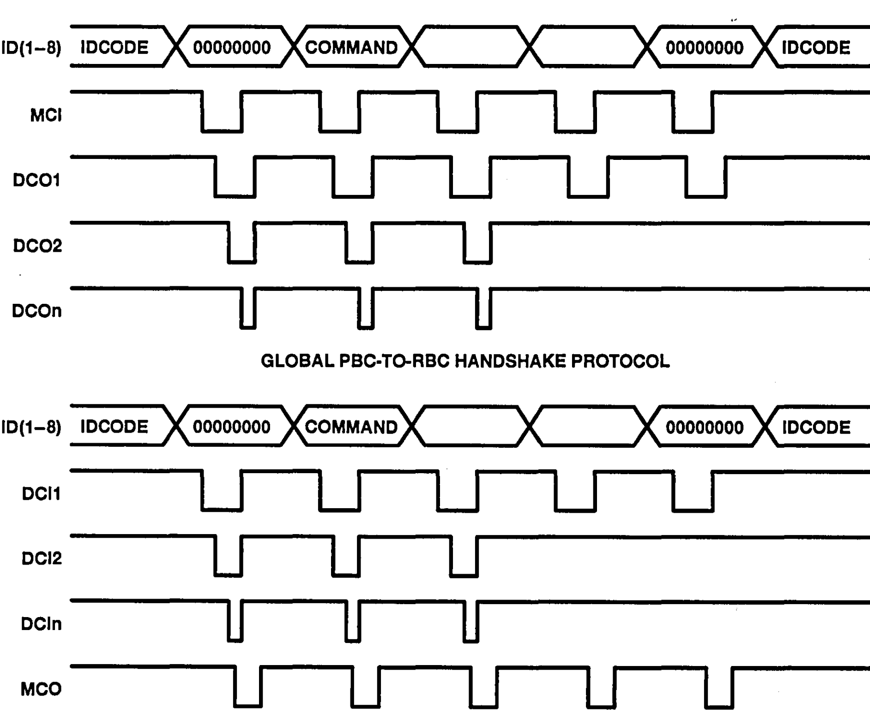



**Figure 10. Global Bus-Communication Protocol**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ........ –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ........ –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) ........ –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) ........ ±20 mA
Output clamp current, $I_{OK}$ ($V_I < 0$ or $V_I > V_{CC}$) ........ ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) ........ ±25 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DW package ........ 1.7 W
NT package ........ 1.3 W
Storage temperature range, $T_{stg}$ ........ –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage rating may be exceeded if the input and output clamp-current rating are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book,* literature number SCBD002.

## recommended operating conditions

| | | | SN54ACT8999 | | SN74ACT8999 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | ID(1–8) | | –1.5 | | –2 | mA |
| | | TDO, DTDO, MCO | | –7 | | –10 | |
| | | DTMS(1–4), DCO (3 state), $\overline{DTRST}$, DTCK | | –11 | | –16 | |
| $I_{OL}$ | Low-level output current | ID(1–8) | | 1.5 | | 2 | mA |
| | | TDO, DTDO, MCO | | 7 | | 10 | |
| | | DTMS(1–4), DCO (3 state or open drain) | | 11 | | 16 | |
| | | $\overline{DTRST}$ | | 16 | | 24 | |
| | | DTCK | | 32 | | 48 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | 0 | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | SN54ACT8999 | | SN74ACT8999 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | TYP† | MAX | |
| $V_{OH}$ | ID(1–8) | $I_{OH}$ = –1.5 mA | 4.5 V | 3.6 | | | | | V |
| | | $I_{OH}$ = –2 mA | 4.5 V | | | 3.7 | | | |
| | TDO, DTDO, MCO | $I_{OH}$ = –7 mA | 4.5 V | 3.6 | | | | | |
| | | $I_{OH}$ = –10 mA | 4.5 V | | | 3.7 | | | |
| | DTMS(1–4), DCO (3 state), $\overline{DTRST}$, DTCK | $I_{OH}$ = –11 mA | 4.5 V | 3.6 | | | | | |
| | | $I_{OH}$ = –16 mA | 4.5 V | | | 3.7 | | | |
| $V_{OL}$ | ID(1–8) | $I_{OL}$ = 1.5 mA | 4.5 V | | 0.5 | | | | V |
| | | $I_{OL}$ = 2 mA | 4.5 V | | | | | 0.5 | |
| | TDO, DTDO, MCO | $I_{OL}$ = 7 mA | 4.5 V | | 0.5 | | | | |
| | | $I_{OL}$ = 10 mA | 4.5 V | | | | | 0.5 | |
| | DTMS(1–4), DCO (3 state or open drain) | $I_{OL}$ = 11 mA | 4.5 V | | 0.5 | | | | |
| | | $I_{OL}$ = 16 mA | 4.5 V | | | | | 0.5 | |
| | $\overline{DTRST}$ | $I_{OL}$ = 16 mA | 4.5 V | | 0.5 | | | | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | | | | 0.5 | |
| | DTCK | $I_{OL}$ = 32 mA | 4.5 V | | 0.5 | | | | |
| | | $I_{OL}$ = 48 mA | 4.5 V | | | | | 0.5 | |
| $I_{OZ}$‡ | ID(1–8), DTDO, DTMS(1–4), DCO, DTCK | $V_O = V_{CC}$ or GND | 5.5 V | | ±10 | | | ±5 | μA |
| $I_{OH}$ | DCO (open drain) | $V_O = V_{CC}$ | 5.5 V | | 20 | | | 10 | μA |
| $I_I$ | MCI, DCI, TCK | $V_I = V_{CC}$ or GND | 5.5 V | | ±1 | | | ±1 | μA |
| | TDI, DTDI, TMS, OTMS, $\overline{TRST}$ | $V_I = V_{CC}$ | 5.5 V | | ±1 | | | ±1 | |
| | | $V_I$ = GND | 5.5 V | –0.1 | –20 | –0.1 | –0.1 | –20 | |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O = 0$ | 5.5 V | | 100 | | | 100 | μA |
| $\Delta I_{CC}$§ | | One input at $V_I$ = 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | 1 | | | 1 | mA |
| $C_i$ | | $V_I = V_{CC}$ or GND | | | | | 6 | | pF |
| $C_{io}$ | | $V_O = V_{CC}$ or GND | | | | | 15 | | pF |
| $C_o$ | MCI, DCI, TCK | $V_O = V_{CC}$ or GND | | | | | 15 | | pF |
| $C_o$ | DCO | $V_O = V_{CC}$ or GND | | | | | 10 | | pF |

† Typical values are at $V_{CC}$ = 5 V.
‡ For I/O, the parameter $I_{OZ}$ includes the input-leakage current. For DCO, the parameter $I_{OZ}$ includes the open-drain output-leakage current.
§ This is the increase in supply current for each input being driven at TTL levels rather than $V_{CC}$ or GND.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 11 and 12)

| | | | SN54ACT8999 | | SN74ACT8999 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 20 | 0 | 20 | MHz |
| | | DCI (count mode) | 0 | 20 | 0 | 20 | |
| $t_w$ | Pulse duration | TCK high or low | 16 | | 16 | | ns |
| | | DCI high or low (count mode) | 9 | | 9 | | |
| | | $\overline{TRST}$ low | 10 | | 10 | | |
| $t_{su}$ | Setup time | TMS before TCK↑ | 9 | | 9 | | ns |
| | | OTMS before TCK↑ | 12 | | 12 | | |
| | | TDI before TCK↑ | 11 | | 11 | | |
| | | DTDI before TCK↑ | 5 | | 5 | | |
| | | MCI before TCK↑ | 5 | | 5 | | |
| | | DCI before TCK↑ | 9 | | 9 | | |
| | | Any ID before TCK↑ | 3 | | 3 | | |
| $t_h$ | Hold time | TMS after TCK↑ | 2 | | 2 | | ns |
| | | OTMS after TCK↑ | 2 | | 2 | | |
| | | TDI after TCK↑ | 4 | | 4 | | |
| | | DTDI after TCK↑ | 4 | | 4 | | |
| | | MCI after TCK↑ | 5 | | 5 | | |
| | | DCI after TCK↑ | 5 | | 5 | | |
| | | Any ID after TCK↑ | 5 | | 5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 100* | | 100 | | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

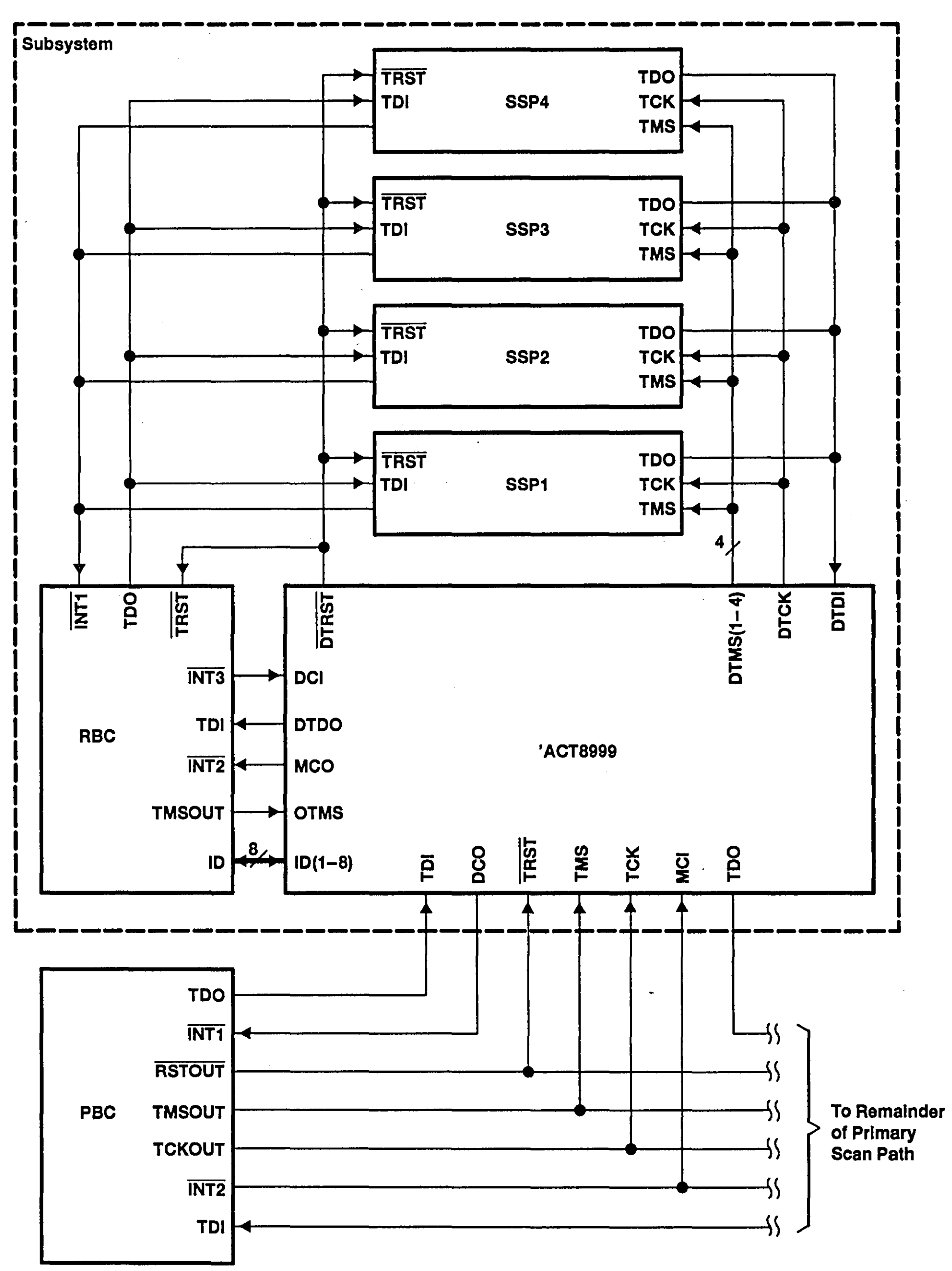
## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 11 and 12)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ACT8999 | | SN74ACT8999 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 20 | | 20 | | MHz |
| | DCI (count mode) | | 20 | | 20 | | |
| $t_{PLH}$ | TCK | DTCK | 3 | 16 | 3 | 14 | ns |
| $t_{PHL}$ | | | 3 | 19 | 3 | 17 | |
| $t_{PLH}$ | TCK↓ | TDO | 7 | 30 | 7 | 28 | ns |
| $t_{PHL}$ | | | 7 | 29 | 8 | 27 | |
| $t_{PLH}$ | TCK↓ | DTDO | 7 | 31 | 7 | 29 | ns |
| $t_{PHL}$ | | | 7 | 29 | 8 | 27 | |
| $t_{PLH}$ | TCK↓ | Any DTMS | 11 | 40 | 11 | 38 | ns |
| $t_{PHL}$ | | | 11 | 37 | 11 | 35 | |
| $t_{PLH}$ | TCK↓ | $\overline{DTRST}$ | 9 | 35 | 10 | 33 | ns |
| $t_{PHL}$ | | | 9 | 35 | 10 | 33 | |
| $t_{PLH}$ | TCK↓ | Any ID | 20 | 64 | 22 | 61 | ns |
| $t_{PHL}$ | | | 22 | 65 | 24 | 62 | |
| $t_{PLH}$ | TCK↓ | MCO | 9 | 34 | 9 | 32 | ns |
| $t_{PHL}$ | | | 9 | 31 | 9 | 29 | |
| $t_{PLH}$ | TCK↓ | DCO (open drain) | 14 | 45 | 18 | 42 | ns |
| | | DCO (3 state) | 10 | 40 | 11 | 38 | |
| $t_{PHL}$ | | DCO (open drain) | 10 | 39 | 11 | 37 | |
| | | DCO (3 state) | 10 | 37 | 11 | 35 | |
| $t_{PLH}$ | TMS | Any DTMS | 5 | 22 | 6 | 20 | ns |
| $t_{PHL}$ | | | 4 | 23 | 5 | 21 | |
| $t_{PLH}$ | OTMS | Any DTMS | 5 | 22 | 6 | 20 | ns |
| $t_{PHL}$ | | | 4 | 23 | 5 | 21 | |
| $t_{PLH}$ | MCI | MCO | 7 | 26 | 8 | 24 | ns |
| $t_{PHL}$ | | | 6 | 25 | 7 | 23 | |
| $t_{PLH}$ | DCI | DCO (open drain) | 8 | 32 | 9 | 30 | ns |
| | | DCO (3 state) | 8 | 30 | 10 | 28 | |
| $t_{PHL}$ | | DCO (open drain) | 8 | 34 | 9 | 32 | |
| | | DCO (3 state) | 8 | 30 | 9 | 28 | |
| $t_{PLH}$ | $\overline{TRST}$ | $\overline{DTRST}$ | 4 | 20 | 5 | 18 | ns |
| $t_{PHL}$ | | | 5 | 25 | 6 | 23 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 11 and 12) (continued)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ACT8999 | | SN74ACT8999 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PHZ}$ | TCK↓ | TDO | 3 | 17 | 4 | 15 | ns |
| $t_{PLZ}$ | | | 3 | 18 | 5 | 16 | |
| $t_{PHZ}$ | TCK↓ | DTDO | 3 | 18 | 3 | 16 | ns |
| $t_{PLZ}$ | | | 7 | 26 | 7 | 24 | |
| $t_{PHZ}$ | TCK↓ | Any DTMS | 7 | 26 | 8 | 24 | ns |
| $t_{PLZ}$ | | | 7 | 28 | 7 | 26 | |
| $t_{PHZ}$ | TCK↓ | DCO | 9 | 28 | 12 | 26 | ns |
| $t_{PLZ}$ | | | 7 | 31 | 7 | 29 | |
| $t_{PHZ}$ | TCK↓ | Any ID | 12 | 38 | 14 | 36 | ns |
| $t_{PLZ}$ | | | 9 | 34 | 10 | 32 | |
| $t_{PHZ}$ | DCI | Any ID | 8 | 27 | 9 | 25 | ns |
| $t_{PLZ}$ | | | 10 | 33 | 15 | 31 | |
| $t_{PZH}$ | TCK↓ | TDO | 9 | 35 | 9 | 33 | ns |
| $t_{PZL}$ | | | 9 | 36 | 11 | 34 | |
| $t_{PZH}$ | TCK↓ | DTDO | 10 | 39 | 11 | 37 | ns |
| $t_{PZL}$ | | | 10 | 40 | 12 | 38 | |
| $t_{PZH}$ | TCK↓ | Any DTMS | 8 | 34 | 9 | 32 | ns |
| $t_{PZL}$ | | | 8 | 34 | 9 | 32 | |
| $t_{PZH}$ | TCK↓ | DCO | 12 | 46 | 14 | 43 | ns |
| $t_{PZL}$ | | | 10 | 38 | 11 | 36 | |
| $t_{PZH}$ | TCK↓ | Any ID | 20 | 73 | 22 | 70 | ns |
| $t_{PZL}$ | | | 22 | 58 | 24 | 65 | |
| $t_{PZH}$ | MCI | Any ID | 18 | 65 | 20 | 62 | ns |
| $t_{PZL}$ | | | 20 | 62 | 20 | 59 | |

## APPLICATION INFORMATION





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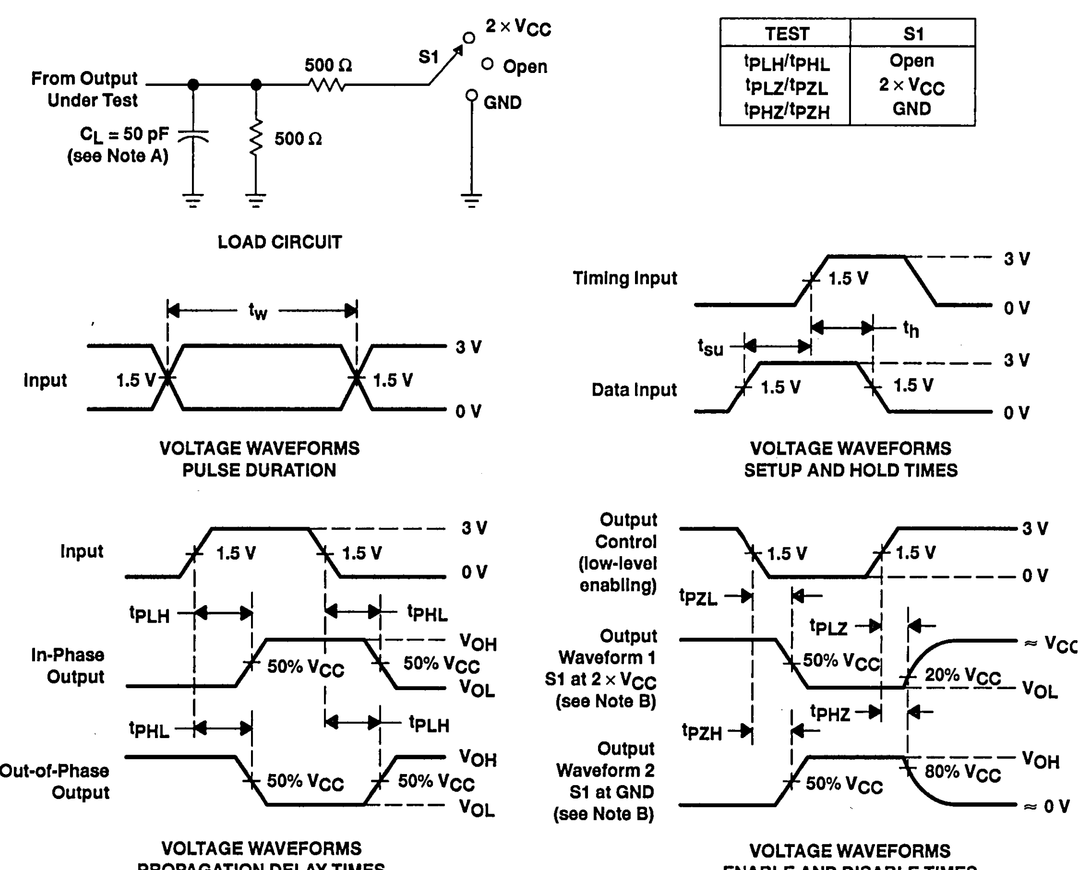
## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns. For testing pulse duration: $t_r$ = 1 to 3 ns, $t_f$ = 1 to 3 ns. Pulse polarity may be either high-to-low-to-high or a low-to-high-to-low.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 11. Load Circuit and Voltage Waveforms (For All Pins Except ID-Bus Pins)**

## PARAMETER MEASUREMENT INFORMATION

From Output Under Test — 1 kΩ — S1 ($V_{CC}$ / Open / GND); $C_L$ = 50 pF (see Note A)

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns. For testing pulse duration: $t_r$ = 1 to 3 ns, $t_f$ = 1 to 3 ns. Pulse polarity may be either high-to-low-to-high or a low-to-high-to-low.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 12. Load Circuit and Voltage Waveforms (ID-Bus Pins)**

General Information 1

SN54/74BCT Octals 2

SN54/74ABT Octals 3

SN54/74ABT Widebus™ With Dual-Sided Terminals 4

SN54/74ABT Widebus™ With Quad-Sided Terminals 5

SN54/74LVT Widebus™ With Dual-Sided Terminals 6

SN54/74LVT Widebus™ With Quad-Sided Terminals 7

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Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.

**EXAMPLE: SN 74BCT8240A DW R**

**Prefix**

SN = Standard prefix
SNJ = MIL-PRF-38535 (QML) qualified

**Unique Circuit Description**

MUST CONTAIN NINE TO THIRTEEN CHARACTERS

Examples: 74ACT8990
74LVTH18504A
74ABTH182502A

**Package**

MUST CONTAIN ONE TO THREE LETTERS

| | | |
|---|---|---|
| DW | = | plastic small-outline package |
| DL | = | plastic shrink small-outline package |
| DGG, PW | = | plastic thin shrink small-outline package |
| FK | = | leadless ceramic chip carrier |
| FN | = | plastic J-leaded chip carrier |
| GA-GB | = | ceramic pin grid array |
| HKC | = | ceramic dual flat package |
| HV | = | ceramic quad flat package |
| JT | = | ceramic dual-in-line package |
| NT | = | plastic dual-in-line package |
| PM | = | plastic thin quad flat package |
| WD | = | ceramic dual flat package |

(from pin-connection diagram on individual data sheet)

**Tape and Reel Packaging**

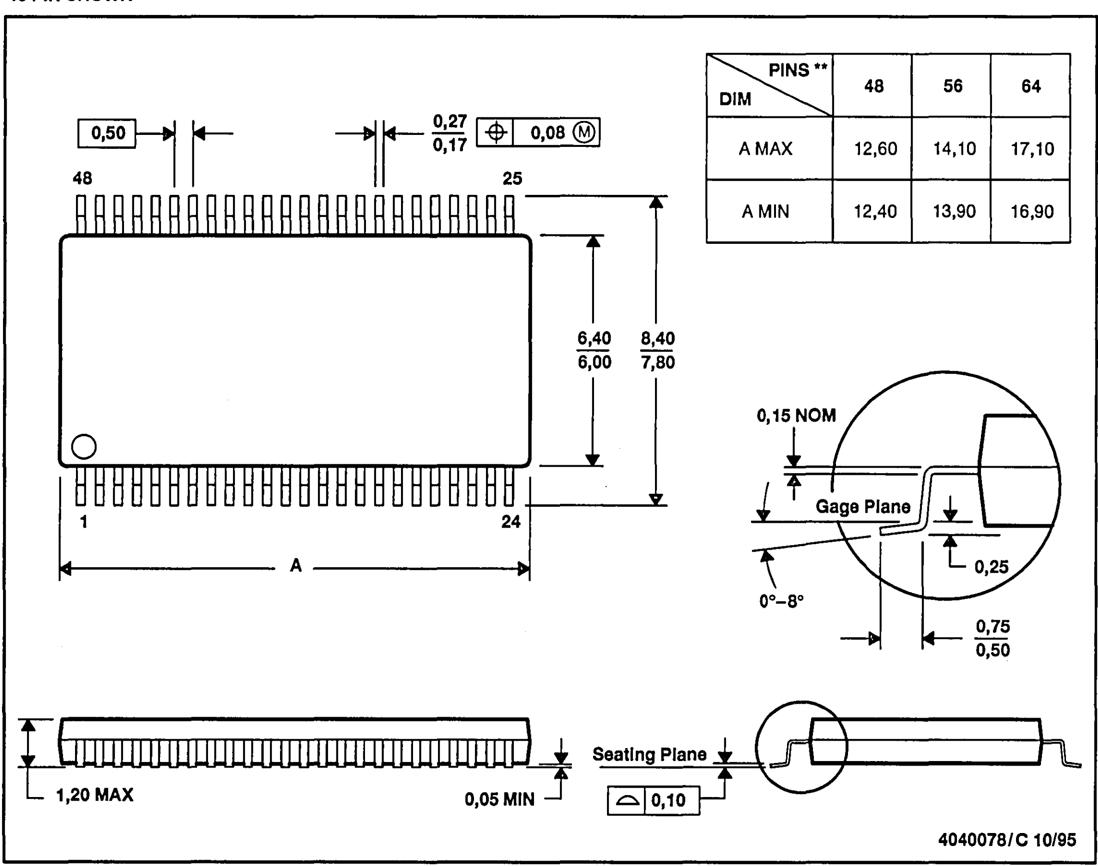
Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for PW packages)
R = Standard tape and reel (required for DGG; optional for DL and DW packages)

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PIN SHOWN**




| PINS ** / DIM | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-153

**DL (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN

| DIM \ PINS ** | 28 | 48 | 56 |
|---|---|---|---|
| A MAX | 0.380 (9,65) | 0.630 (16,00) | 0.730 (18,54) |
| A MIN | 0.370 (9,40) | 0.620 (15,75) | 0.720 (18,29) |



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).



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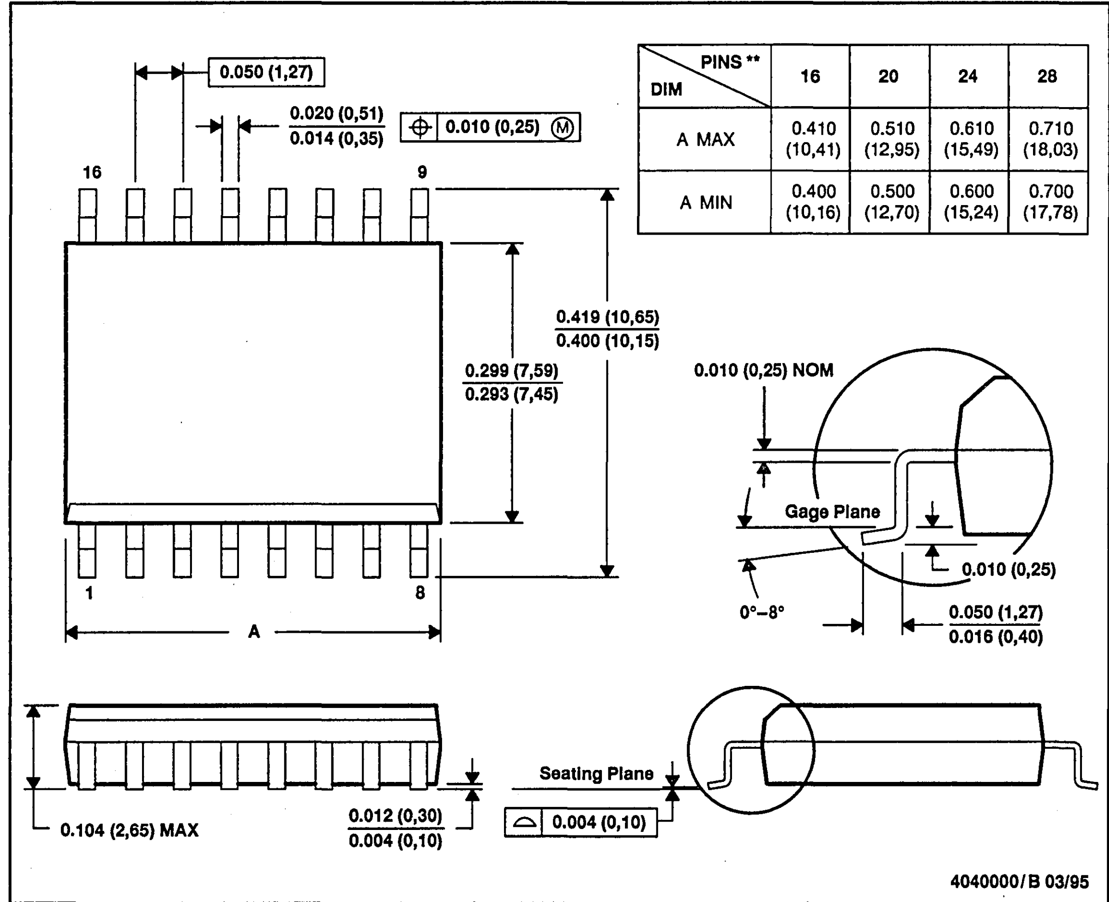
**DW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**16 PIN SHOWN**




| DIM \ PINS ** | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MAX | 0.410 (10,41) | 0.510 (12,95) | 0.610 (15,49) | 0.710 (18,03) |
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.600 (15,24) | 0.700 (17,78) |

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013

**FK (S-CQCC-N**)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.739 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

18 17 16 15 14 13 12
19 20 21 22 23 24 25
11 10 9 8 7 6 5
26 27 28 1 2 3 4
B SQ
A SQ

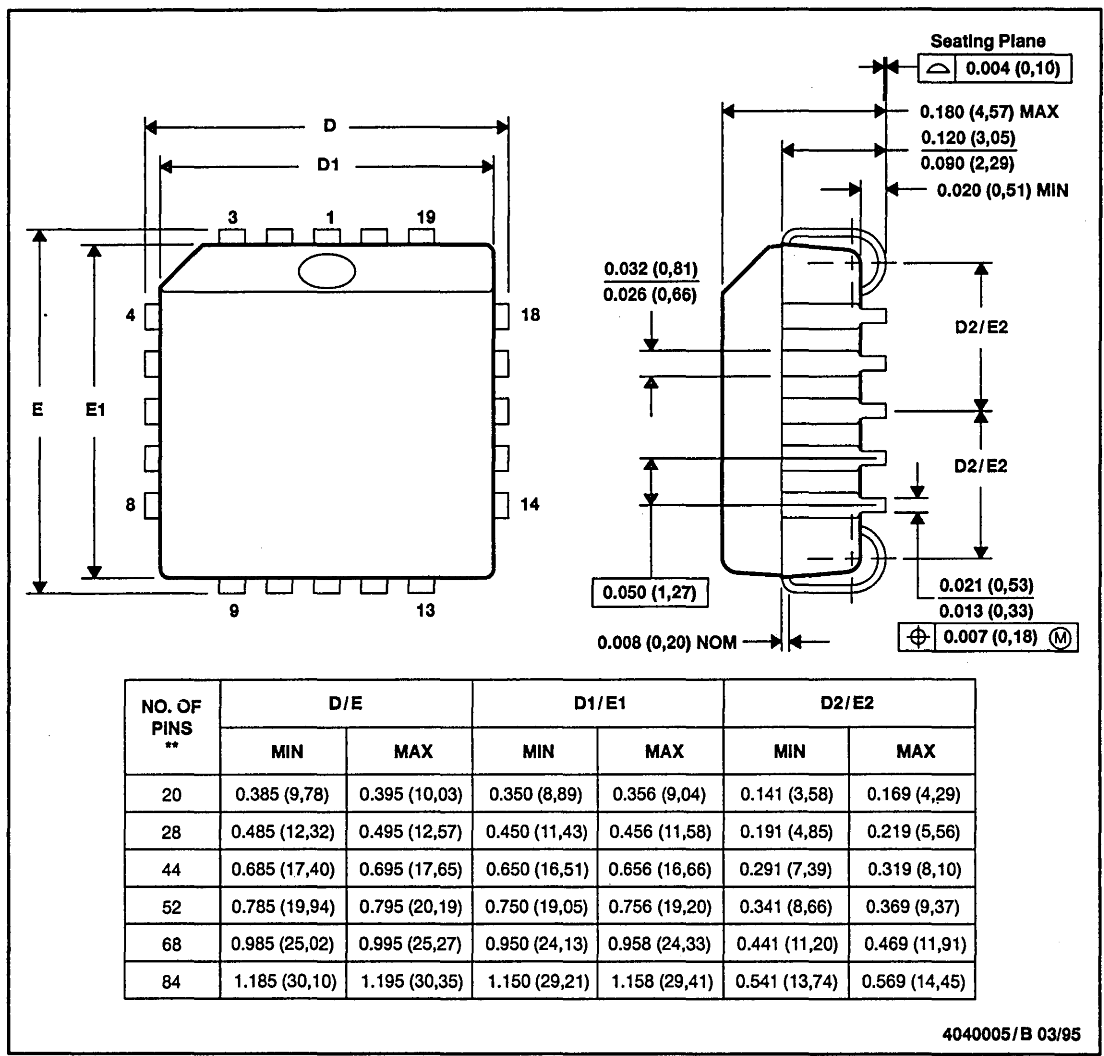
0.020 (0,51) / 0.010 (0,25)
0.020 (0,51) / 0.010 (0,25)
0.080 (2,03) / 0.064 (1,63)
0.055 (1,40) / 0.045 (1,14)
0.045 (1,14) / 0.035 (0,89)
0.028 (0,71) / 0.022 (0,54)
0.045 (1,14) / 0.035 (0,89)
0.050 (1,27)

4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

**FN (S-PQCC-J**)** **PLASTIC J-LEADED CHIP CARRIER**

**20 PIN SHOWN**

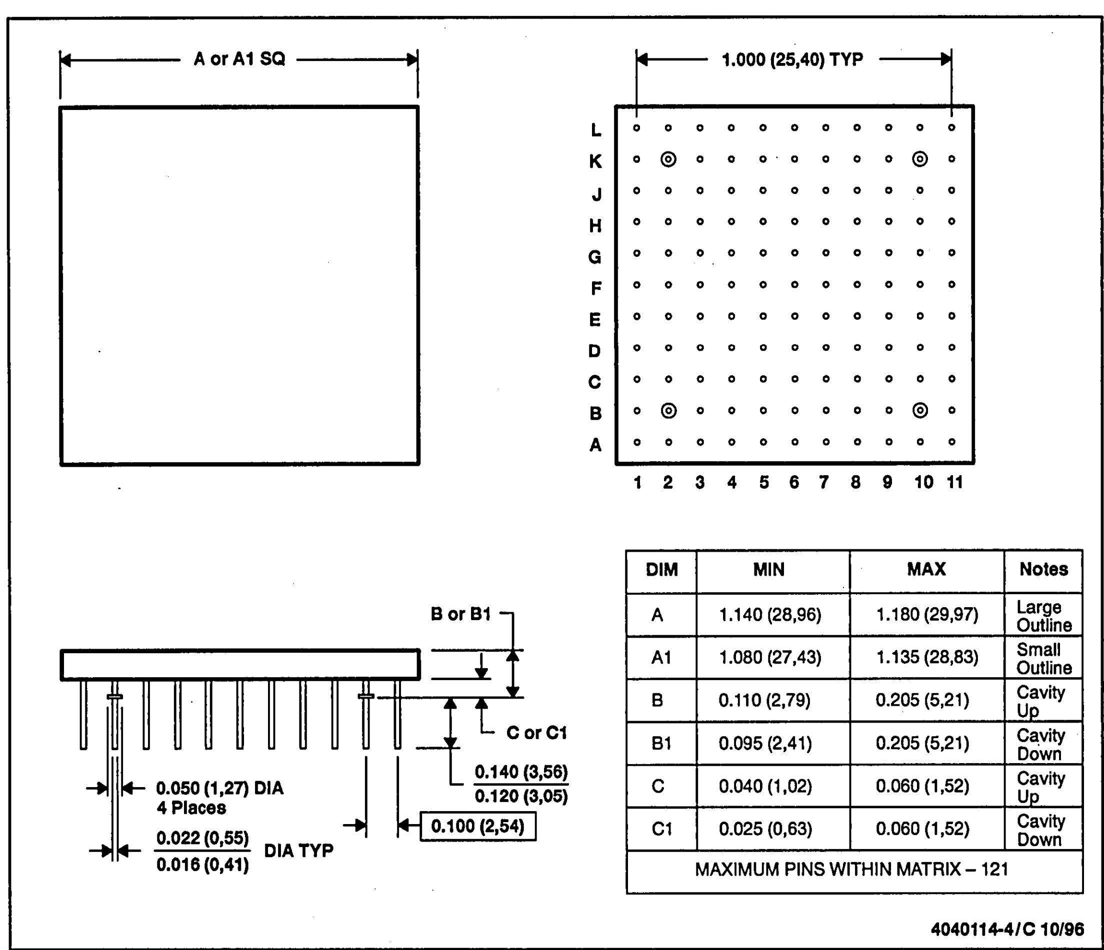



| NO. OF PINS ** | D / E | | D1 / E1 | | D2 / E2 | |
|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX |
| 20 | 0.385 (9,78) | 0.395 (10,03) | 0.350 (8,89) | 0.356 (9,04) | 0.141 (3,58) | 0.169 (4,29) |
| 28 | 0.485 (12,32) | 0.495 (12,57) | 0.450 (11,43) | 0.456 (11,58) | 0.191 (4,85) | 0.219 (5,56) |
| 44 | 0.685 (17,40) | 0.695 (17,65) | 0.650 (16,51) | 0.656 (16,66) | 0.291 (7,39) | 0.319 (8,10) |
| 52 | 0.785 (19,94) | 0.795 (20,19) | 0.750 (19,05) | 0.756 (19,20) | 0.341 (8,66) | 0.369 (9,37) |
| 68 | 0.985 (25,02) | 0.995 (25,27) | 0.950 (24,13) | 0.958 (24,33) | 0.441 (11,20) | 0.469 (11,91) |
| 84 | 1.185 (30,10) | 1.195 (30,35) | 1.150 (29,21) | 1.158 (29,41) | 0.541 (13,74) | 0.569 (14,45) |

4040005 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

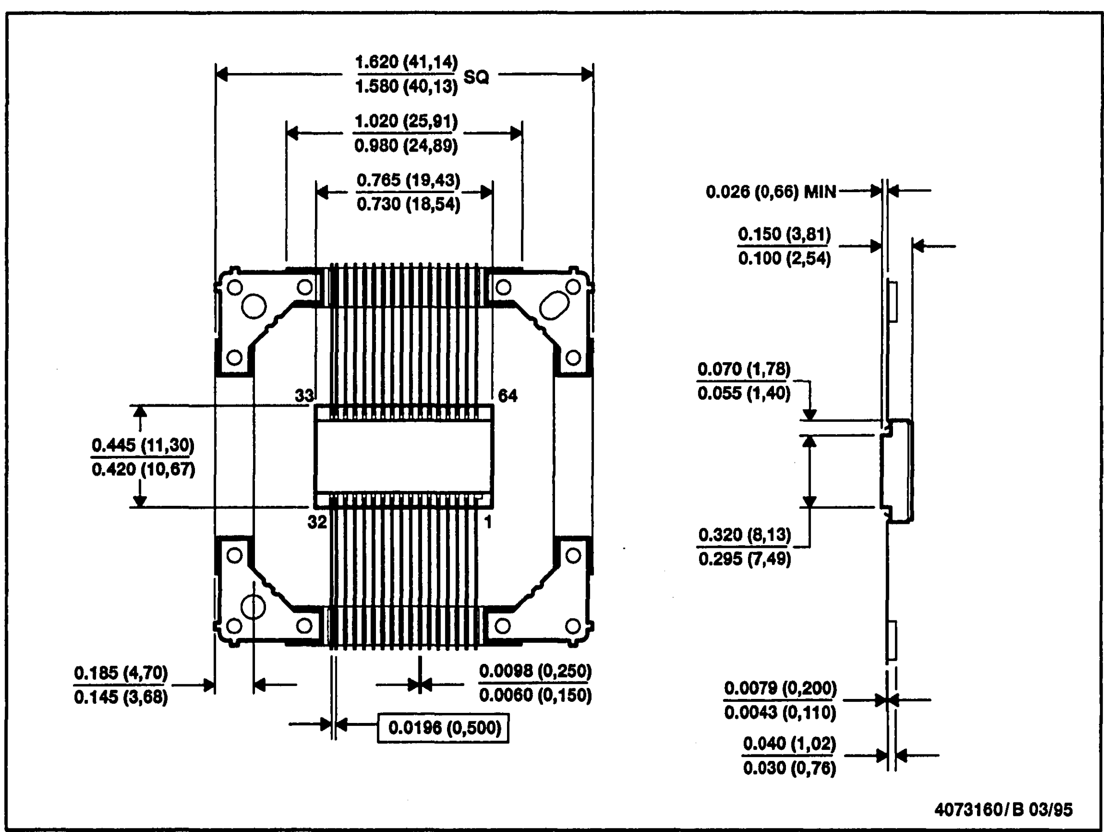
**GA-GB (S-CPGA-P11 X 11)** **CERAMIC PIN GRID ARRAY PACKAGE**




| DIM | MIN | MAX | Notes |
|---|---|---|---|
| A | 1.140 (28,96) | 1.180 (29,97) | Large Outline |
| A1 | 1.080 (27,43) | 1.135 (28,83) | Small Outline |
| B | 0.110 (2,79) | 0.205 (5,21) | Cavity Up |
| B1 | 0.095 (2,41) | 0.205 (5,21) | Cavity Down |
| C | 0.040 (1,02) | 0.060 (1,52) | Cavity Up |
| C1 | 0.025 (0,63) | 0.060 (1,52) | Cavity Down |
| MAXIMUM PINS WITHIN MATRIX – 121 | | | |

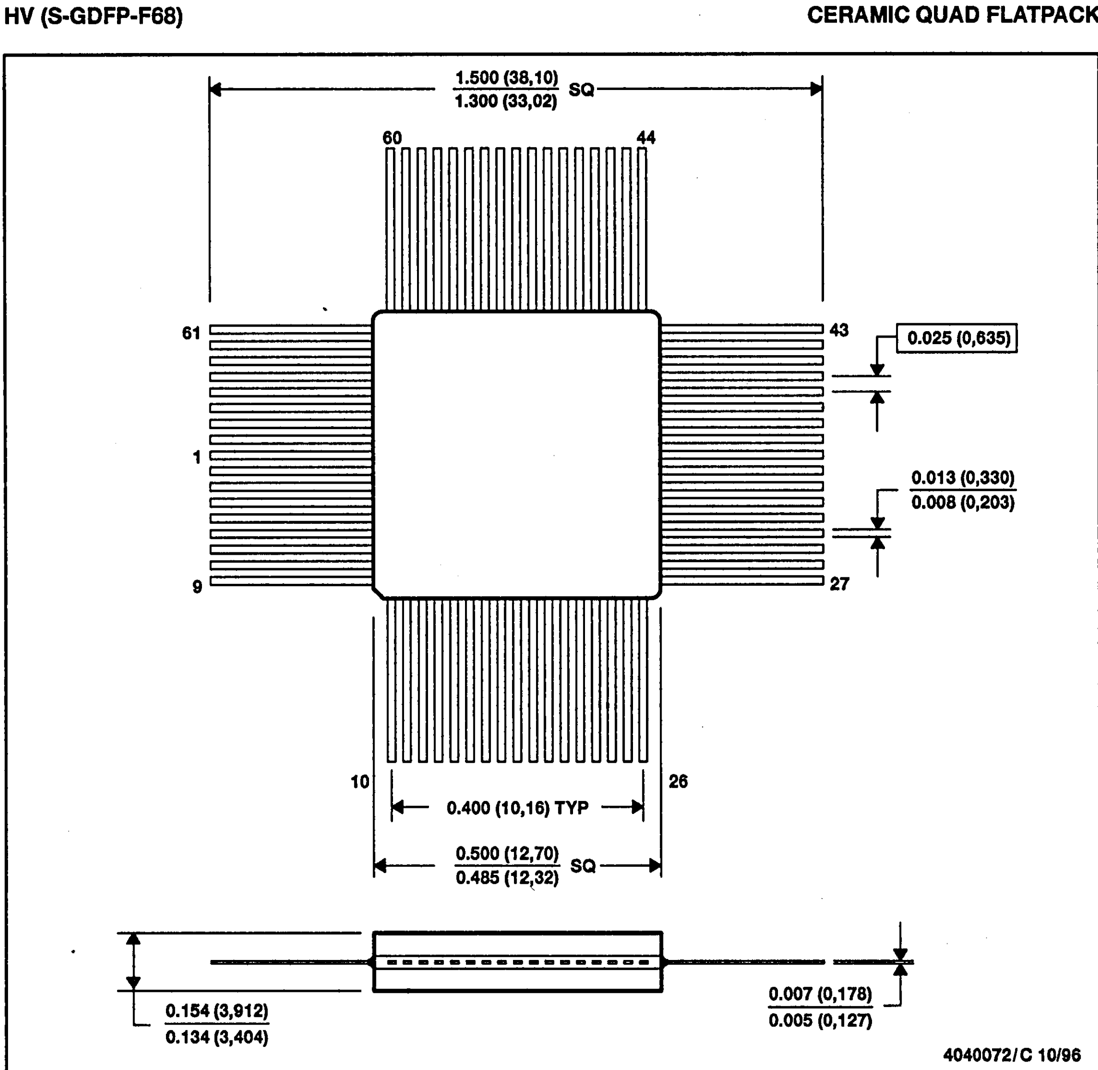
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Index mark may appear on top or bottom depending on package vendor.
- D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
- E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
- F. The pins can be gold plated or solder dipped.
- G. Falls within MIL-STD-1835 CMGA3-PN and CMGA15-PN and JEDEC MO-067AC and MO-066AC, respectively

**HKC (R-CDFP-F64)** **CERAMIC DUAL FLATPACK WITH TIE BAR**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. All leads not shown for clarity purposes.

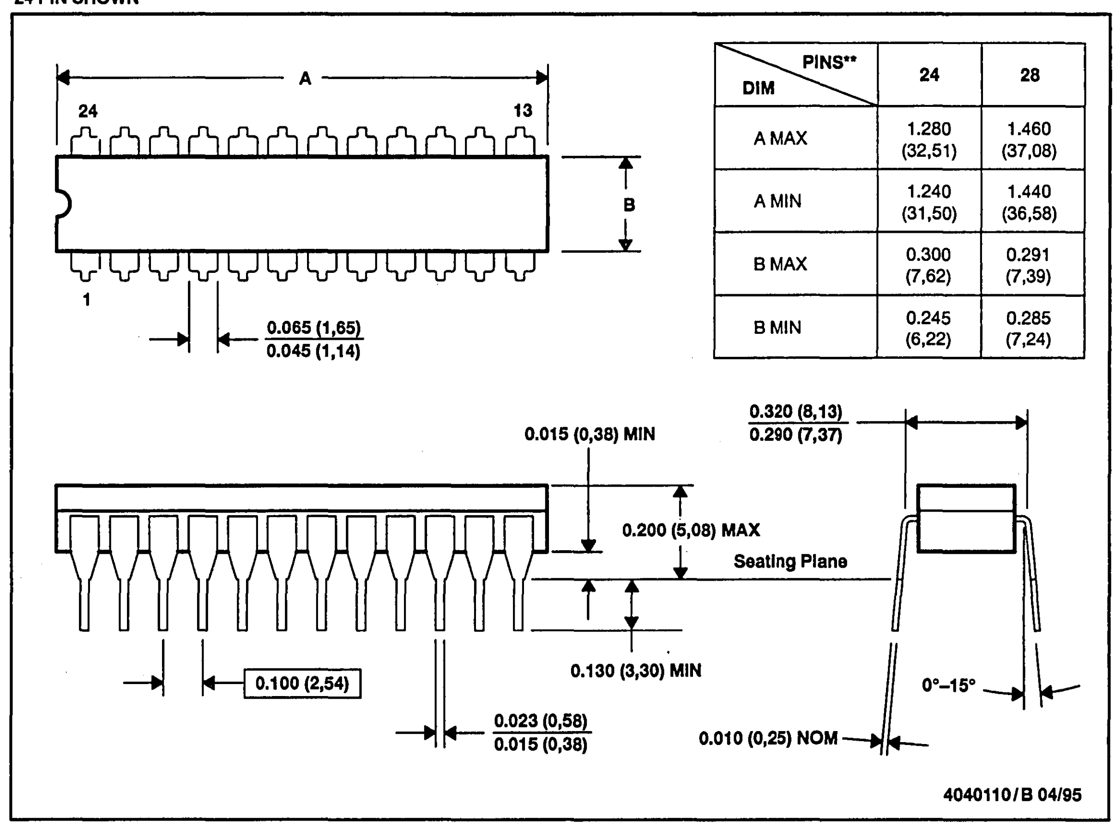
**HV (S-GDFP-F68)** **CERAMIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

**JT (R-GDIP-T**)** **CERAMIC DUAL-IN-LINE PACKAGE**

**24 PIN SHOWN**

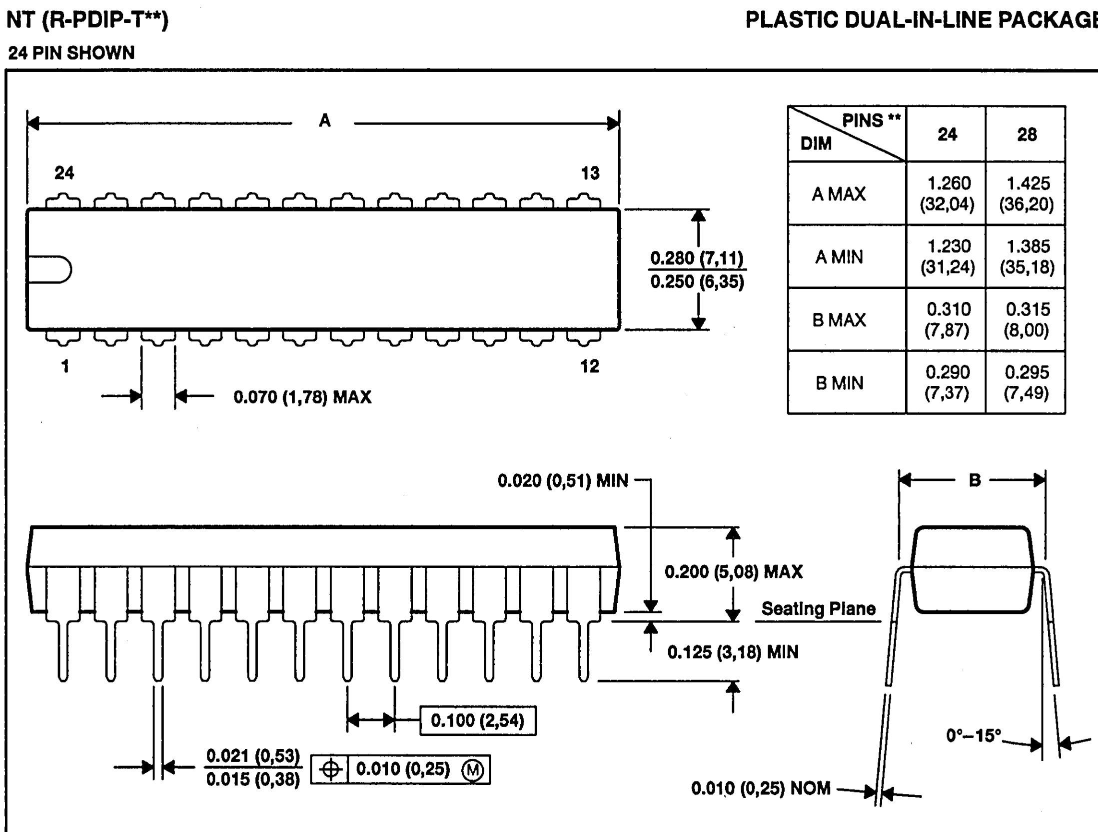



| PINS** / DIM | 24 | 28 |
|---|---|---|
| A MAX | 1.280 (32,51) | 1.460 (37,08) |
| A MIN | 1.240 (31,50) | 1.440 (36,58) |
| B MAX | 0.300 (7,62) | 0.291 (7,39) |
| B MIN | 0.245 (6,22) | 0.285 (7,24) |

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP-T24 and GDIP-T28 and JEDEC MO-058AA and MO-058AB

**NT (R-PDIP-T**)** **PLASTIC DUAL-IN-LINE PACKAGE**

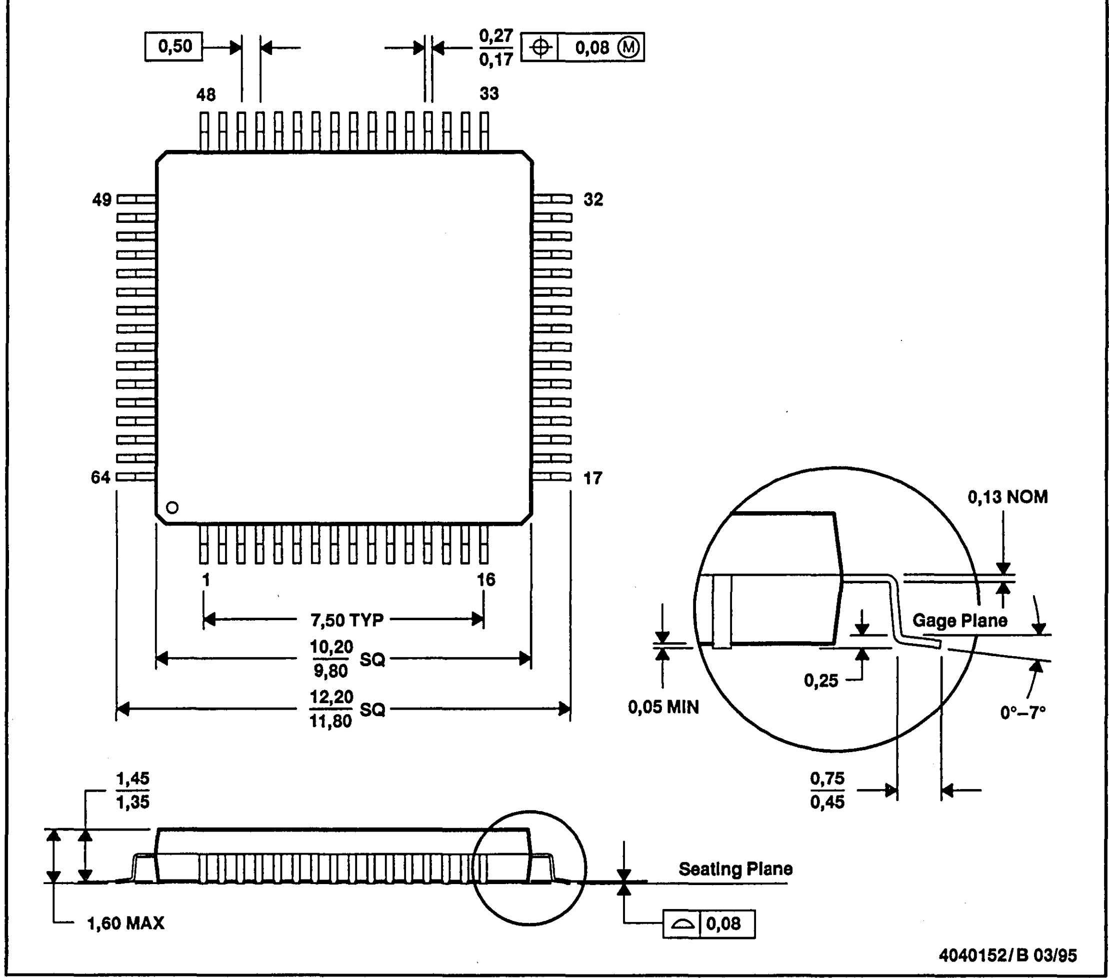
**24 PIN SHOWN**




| DIM \ PINS ** | 24 | 28 |
|---|---|---|
| A MAX | 1.260 (32,04) | 1.425 (36,20) |
| A MIN | 1.230 (31,24) | 1.385 (35,18) |
| B MAX | 0.310 (7,87) | 0.315 (8,00) |
| B MIN | 0.290 (7,37) | 0.295 (7,49) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

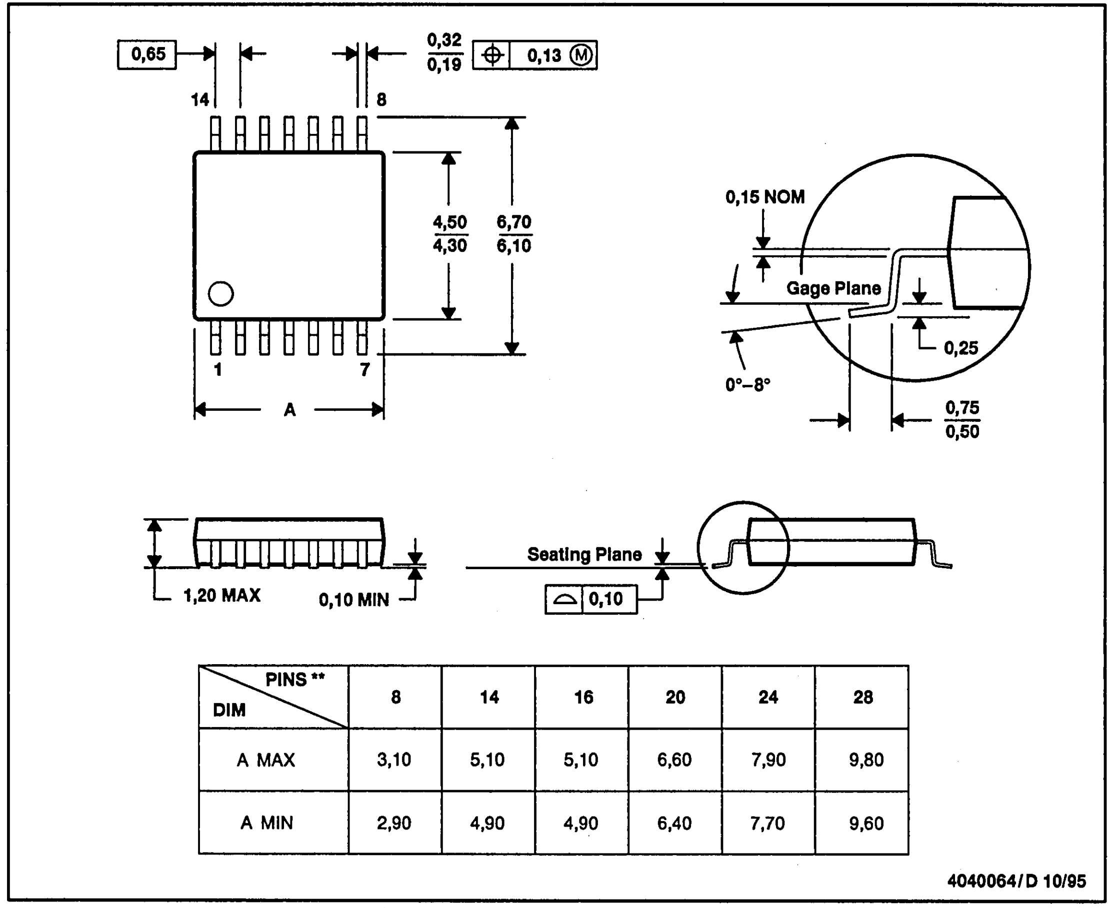
**PM (S-PQFP-G64)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

## PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

**14 PIN SHOWN**

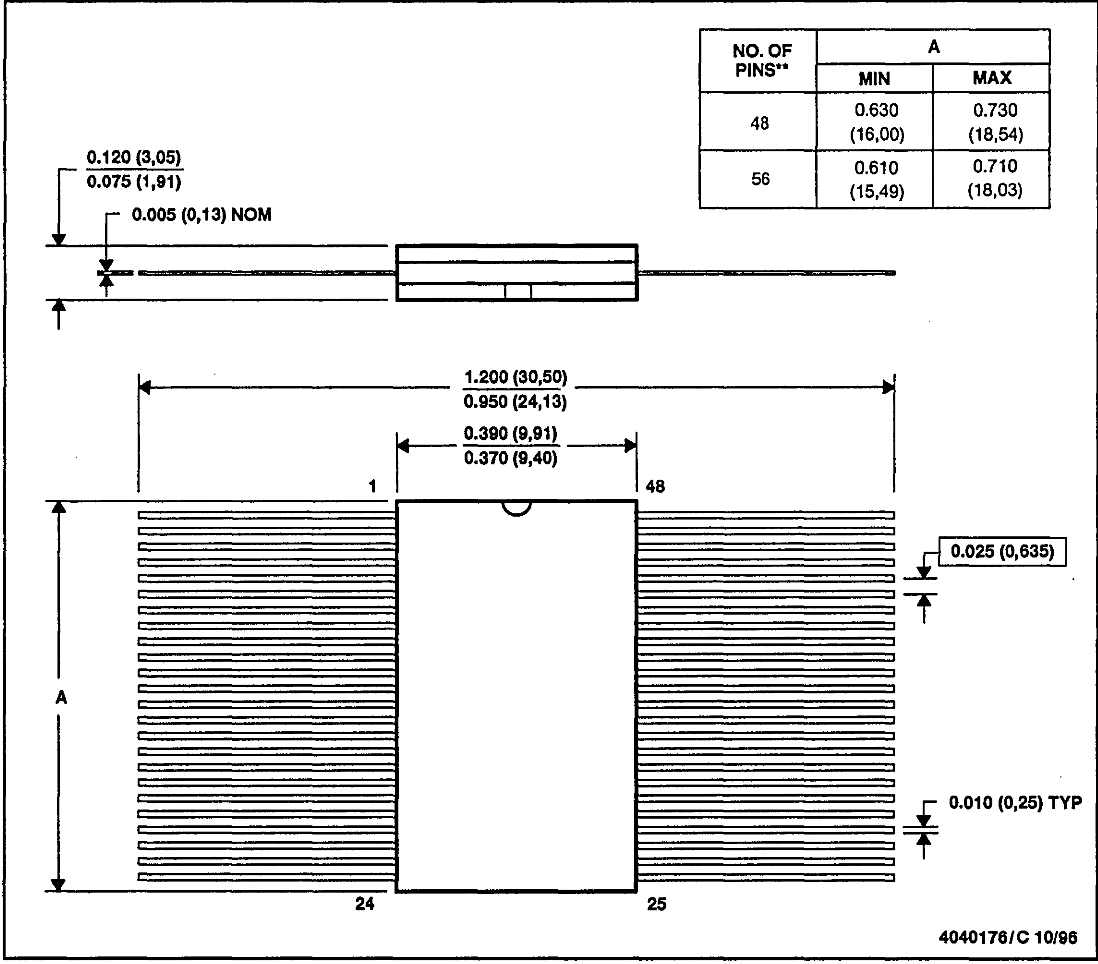



| PINS ** / DIM | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

**WD (R-GDFP-F**)** **CERAMIC DUAL FLATPACK**

48 PIN SHOWN




| NO. OF PINS** | A | |
|---|---|---|
| | MIN | MAX |
| 48 | 0.630 (16,00) | 0.730 (18,54) |
| 56 | 0.610 (15,49) | 0.710 (18,03) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for pin identification only.
E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

General Information 1

SN54/74BCT Octals 2

SN54/74ABT Octals 3

SN54/74ABT Widebus™ With Dual-Sided Terminals 4

SN54/74ABT Widebus™ With Quad-Sided Terminals 5

SN54/74LVT Widebus™ With Dual-Sided Terminals 6

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Technical Information

# JTAG/IEEE 1149.1 Design Considerations

*Johnny Young*
*Semiconductor Group*

SCTA029

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## Introduction

The JTAG/IEEE 1149.1 test standard is becoming widely accepted as a way to overcome the problems created by surface-mount packages, double-sided boards, and multichip modules (see Figure 1), all of which result in a loss of physical access to signals on the board. By providing a means to test printed-circuit boards and modules that might otherwise be untestable, the time and cost required to develop a product and bring it to market can be reduced significantly. (see Appendix A for a brief overview of the 1149.1 standard.)

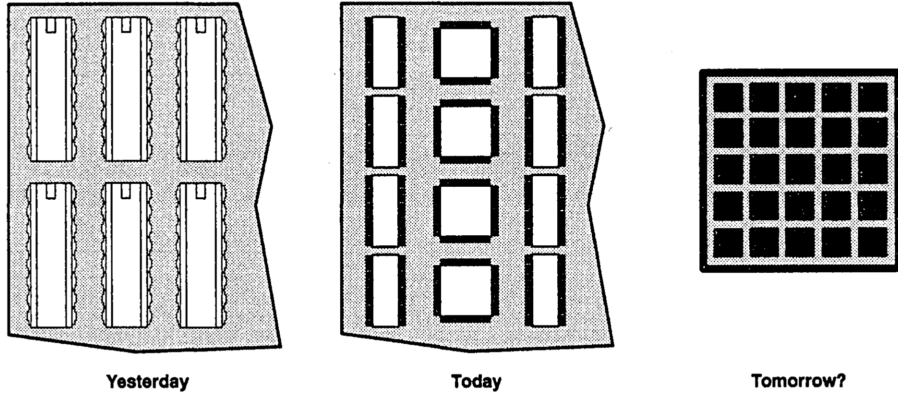



**Figure 1. Physical-Access Problem in PCB Designs**

The conversion to boundary scan has been readily accepted by many who realize that traditional test methods are not effective in dealing with the issues of decreasing physical access. Their products are such that faults not detected in the factory can be costly to isolate and repair if they surface after they are in the field. These customers see boundary scan as the only solution and have realized cost as well as time-to-market savings, in addition to providing a more reliable product to their customers.

There are others who view boundary scan more skeptically and are uncertain of the ultimate benefits. To help illustrate the potential savings of boundary scan, Table 1 provides a comparative test cost model for an application from the professional product division of Philips Electronics, which involved including boundary scan in their ASICs. Though it doesn't specifically address boundary-scan logic, the benefits to test program generation, testers, fixture costs, etc. apply.

The reader may use this table as a guide to determine the comparative cost savings for his application. In place of the implementation costs for ASICs, you can substitute additional material costs associated with boundary-scan bus interface devices over their nonscan counterparts. In addition to costs savings, there are the benefits of decreased time to market, improved product quality, reduced customer downtime, etc.

**Table 1. Comparative Test-Cost Model**

| | BOUNDARY SCAN | NON BOUNDARY SCAN |
|---|---|---|
| **Implementation cost**<br>(BSR) 200k boards/year,<br>12 ASICs per PCB,<br>1% of $25 ASIC | **$600k** | **None** |
| **Test program generation**<br>30 PCB types/year @ $50/hour | 50 hours/type = **$75k** | 300 hours/type = **$450k** |
| **Diagnostics**<br>70% yield of 200k PCBs = 60k PCBs<br>to be repaired @ $25/hour | 2 min. per repair = 2k hours = **$50k** | 10 min. per repair = 10k hours =<br>**$250k** |
| **Number of testers**<br>200k PCBs/year, test time 3 min./PCB = 10k hrs;<br>3 shifts/tester yields 5k hrs/year/tester | plus diagnostic time and retest<br>= 15k hours = 3 testers | plus diagnostic time and retest<br>= 23k hours = 5 testers |
| **Tester costs**<br>Investment = cost of ownership 33%/year | $75k<br>**$75k** | $500k<br>**$830k** |
| **Fixture costs**<br>30 fixtures | @ $5k = **$150k** | @ $15k = **$450k** |
| **Labor cost**<br>@ $25/hour | 15k hours<br>**$375k** | 23k hours<br>**$575k** |
| **Yearly total** | **$1325k** | **$2555k** |

(from: *Boundary-Scan Test, A Practical Approach* by Harry Bleeker, Peter van den Eijnden, and Frans de Jong, 1993)

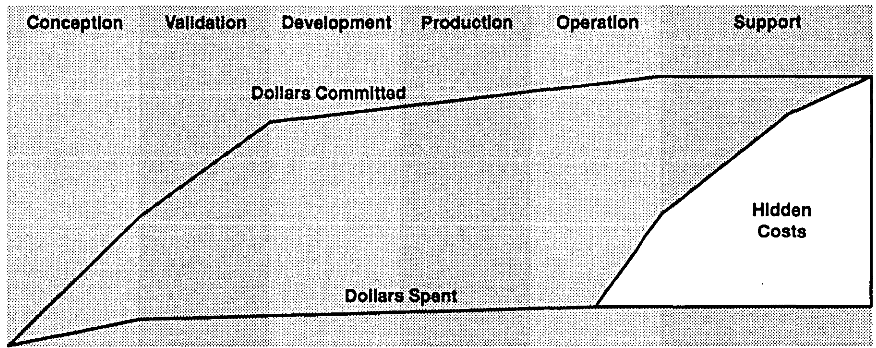
Implementing boundary scan into a design requires a different mindset due to the different hardware, software, and test equipment needs versus traditional test methods, Designers are often uncertain as to exactly how they should begin, what issues must be considered, and what pitfalls await. The purpose of this report is to touch on some of the issues designers should consider when designing with off-the-shelf boundary-scan logic components.

## Is JTAG Right for You?

As noted in the introduction, one of the first decisions you will face is whether using boundary scan is of benefit to you. The designer is faced with many issues that must be addressed when implementing boundary scan into a design, versus a design with standard components. A key concern is the fact that boundary-scan devices generally are priced slightly higher than their non-JTAG counterparts. However, as shown in Table 1, there are many situations where the additional material cost of implementing boundary scan is offset by a reduction in life-cycle costs.

Figure 2 provides two views of product life-cycle costs. The lower curve represents actual dollars spent. The upper curve illustrates that development decisions commit funds that other process steps must spend. By the time engineering "releases" a product to manufacturing, 85% of the project's total costs are committed. These costs are driven by decisions made during the design phase and can only be reduced if they are considered early in the design phase.

Both of the above examples illustrate that the goal of boundary scan is to reduce the product's life-cycle cost, even though board or system material costs may increase. The life-cycle cost reduction is achieved by enabling faults to be easily identified and isolated, reducing test development and execution time. Further cost reduction is achieved by reducing or eliminating the need for expensive test fixtures and equipment.




(from "Controlling Life-Cycle Costs Through Concurrent Engineering", Addendum to the ATE and Instrumentation Proceedings, Miller Freeman Expositions, 1992)

**Figure 2. Life-Cycle Costs of Typical Product**

The use of boundary scan can also have a positive impact on time to market, resulting in a maximization of profit potential. These benefits are discussed in greater detail throughout this document.

To make an accurate assessment of the benefits of boundary scan, representatives of all of the disciplines involved in the product's development must discuss their respective problem areas. Only then can a solution be reached that truly addresses the total product life-cycle cost. Several factors can be analyzed to determine the impact of boundary scan on your application:

### Boundary Scan Can Reduce PCB Debug Time

By providing access to device I/O without probes, boundary scan allows you to quickly identify and isolate defects to the device and, often, the pin level. Boards that previously may have taken weeks to debug can now be tested in a matter of days or even hours. Additionally, faults that may not have been detected during board test can now be found, preventing faults from surfacing during final test when the costs of finding and repairing the failure are magnified.

### Boundary-Scan Components Help Reduce Test Program Development Time

Because tests can be performed independent of device functionality, costly in-circuit test models do not have to be developed. Instead, the user can obtain boundary-scan description language files (BSDL) from the silicon vendor. These files describe how boundary scan has been implemented within the part so tools can understand how to communicate with it. Another key feature of boundary scan is that tests performed at the device level can be rerun at the PCB and system level, reducing or eliminating the need to develop new tests or generate new test vectors. (See Appendix B for examples of how other customers have benefited from the use of boundary scan.)

### Boundary Scan Can Reduce the Need for Costly Fixtures

Boundary-scan testing of a PCB only requires the user to access the 4-wire JTAG bus. Thus, a PCB or system can be tested in its normal configuration without the need to develop fixtures for each PCB or subsystem.

### Boundary Scan Can Reduce or Eliminate the Need for Test Points

By providing "virtual nails" to each boundary-scannable I/O, the designer no longer needs test points for standard in-circuit testers. Removing these test points reduces board manufacturing cost by reducing the number of board layers required.

### Boundary Scan Can Reduce the Number of Pins Needed for In-Circuit Testers

Even if all parts on a PCB do not have boundary scan, all of the benefits discussed here still apply. You may still need to use in-circuit testers to access nonscan nodes. However, by reducing the number of test points needed, you also reduce the number of pins required for the in-circuit tester, which determines the type and cost of the tester needed. The cost of automatic test equipment of this type has risen to as much as $1.5M in the past several years. Reducing the complexity of the tester may mean being able to utilize a tester that is priced significantly less.

### Boundary Scan Can Help to Perform Functional Testing

While boundary scan was invented to test for manufacturing defects, users are finding it valuable in doing a variety of functional tests. ASICs and microprocessors can make use of boundary scan to access internal registers and enable testing of the device itself. Clusters of nonscannable logic may be tested by using a boundary-scan device at the cluster input to drive a predetermined pattern. Additional boundary-scan devices at the output can capture the cluster output data and compare it to expected results. In the same manner, other devices such as memories can also be tested.

These are just some of the areas where boundary scan can be of use to you. In some cases you may want to consult with your test or manufacturing engineer to understand the problems they face since, in many cases, designers are unaware of the difficulties their designs pose to others later in the product life cycle.

The degree to which the use of JTAG components impacts your life-cycle development costs will depend on the specifics of your design. While it is not necessary to have a 100% boundary-scan board, the more controllability and observability you can gain by adding boundary-scan devices in key areas, the more benefits you will realize.

## Boundary-Scan Training

Whether you are a hardware design engineer, ASIC designer, test engineer, or program manager, there are several options available for learning more about design for test (DFT) and specifically boundary scan. Texas Instruments (TI) has developed several testability training tools to aid you in finding out more about how boundary scan works and how it can benefit you. Some of these are listed below. For more information on available literature and training, please contact your local TI sales representative or authorized distributor.

### TI Boundary-Scan Training

#### *Scan Educator (SATB002A)*

An educational software program, Scan Educator introduces the fundamentals of the IEEE 1149.1 boundary-scan standard, including architecture, protocol, and required instruction sets.

Self-paced and menu-driven, it contains both information and animated boundary-scan test simulations. Hands-on, practice exercises guide you through boundary-scan test of our SCOPE™ octals at the TAP and at the register level. You are also shown how to use IEEE 1149.1 with single or multiple devices for in-circuit observability and controllability and for interconnect testing.

#### *Testability Primer (SSYA002C)*

This pocket-sized book provides an introduction and indispensable reference to JTAG/IEEE 1149.1 testability. It includes discussion of cost benefits/trade-offs associated with design for test, a technical overview of IEEE Std 1149.1 and supporting data formats (BSDL, HSDL, SVF), and a set of application briefs. Summary information on TI silicon testability solutions and support and learning products is also included.

#### *Testability Videotape*

This two-part videotape provides a background of the growing need for testability and its economic impact. It also describes the work of JTAG and the provisions of the IEEE 1149.1 standard. Part two of the videotape examines the standard in detail. It explains the function of each component of the standard and shows how they work together to provide an accurate, dependable test procedure.

#### *Testability CD-ROM*

TI has assembled the key components of testability on a searchable CD-ROM that includes the IEEE Std 1149.1-1990 and IEEE Std 1149.1a-1993 merged into a single updated document, the TI Test Bus Evaluation Report, application notes on IEEE 1149.1, and device data sheets.

In addition to educational opportunities from TI, other vendors supplying boundary-scan products are usually able to provide training.

For more personal training, TI is also able to hold on-site meetings and seminars tailored to address the needs of your application. Please contact your local TI sales representative or authorized distributor.

## Determining Where to Place Boundary-Scan Devices

Once you have become familiar with boundary scan, you will want to integrate it in your design. TI has a broad spectrum of boundary-scan devices available today:

- ASICs
- Fixed and floating-point digital signal processors
- Bus-interface ICs
- Scan-Support ICs

To identify which devices are needed and where they should be placed, there are several questions you should ask:

### *What Signals Do You Need to Control and Observe?*

The boundary-scan standard allows you to take control of an I/O to either sample data at the pin or stimulate the pin with known data. By replacing standard components with JTAG-compliant devices, you can gain access to individual pins for a variety of tests.

### *Would You Like to Use Boundary Scan to Test Nonscan Logic Clusters?*

By having the ability to control and observe device I/O, you can use scannable devices to test devices without JTAG capability. One JTAG device can be loaded with a predetermined pattern that can be driven onto the cluster inputs while additional JTAG devices can capture the output information to be compared against the expected result.

### *Do You Need Embedded Test Capability?*

In support of applications requiring a JTAG controller to be "embedded" within the design, TI has developed devices that can translate parallel commands from a processor into the required JTAG protocol to drive the JTAG bus. For embedded applications, TI has developed a software driver for this bus controller that can be compiled with user code to execute pass/fail tests stored in memory.

### *Will You Be Implementing Built-In-Self-Test Capability In Your Design?*

If you would like to have your board/system execute some form of self test, TI has devices that can help. Within each TI bus interface device lies the ability to execute instructions that command the device to automatically generate output patterns. This capability can reduce or eliminate the need to develop test patterns, as well as significantly reduce the time involved to execute some tests.

### *What Performance Requirements (Speed, Power, Drive) Are Needed?*

The constraints of your design will determine the technology you require in a bus-interface device. TI's JTAG family contains over 20 devices and crosses a variety of technologies, giving you the ability to pick the device that best suits your needs. Table 2 below provides an example of the performance differences between TI's BCT and ABT technologies versus competing technology.

**Table 2. Performance Comparison, JTAG Transceiver Functions**

| SPECIFICATION | BCT (TI) | ABT 18-BIT (TI) | FACTQ (NSC) |
|---|---|---|---|
| tp A/B to B/A | 10 ns | 5.4 ns | 8.8 ns |
| Maximum TCK rate | 20 MHz | 50 MHz | 25 MHz |
| Number of bits | 8 | 18 | 18 |

Based on comparison of TI BCT8245 and ABT18245 vs. NSC SCAN18245.

### *Will You Require Devices That Operate From 3-V Power?*

With more systems moving toward 3-V power, TI has developed 3-V versions of our more popular JTAG Widebus™ devices. These devices are designated as LVTH18xxx. Universal bus transceiver (UBT™) functions are also available now.

### *Will You Need to Drive JTAG Signals Across a Backplane?*

As boundary scan gains acceptance at the board level, the need to perform system-level tests with boundary scan is creating an interesting problem for test engineers. While several approaches have been proposed to date, none addresses the problem better than TI's ABT8996 addressable scan port. This device provides a simple approach to solving a very complex problem without the overhead associated with competing solutions.

### *What Function Type, Bit Width, or Packaging Limitations Do You Have?*

There are many more boundary-scan functions available on the market today than there were even one year ago. Designers are able to select a device based on the functionality, performance, and board area limitations of their design. Boundary-scan buffers, drivers, transceivers, latches, and flip-flops are available in a variety of technologies. TI is the leading supplier of JTAG logic, with over 30 device types available now.

### *What Type of Test Equipment Do You Expect to Use?*

To make the conversion to a test philosophy based on boundary scan, you should define your design, manufacturing, test, and field support flow before beginning hardware design. The details of this test plan will determine the types of tests to be performed, the devices to be used and their placement, and, therefore, the equipment that will be required. There are several vendors supplying CAE and ATE tools to the market today in support of boundary scan.

### *Will You Need to Use Bare Die for Use in Multichip Modules?*

Multichip modules epitomize the problem of no physical access. Boundary scan can be very beneficial by providing you access to internal signals of the MCM. TI supports this effort by supplying bare die for all of its standard components. Additionally, special devices such as the ACT8994 digital bus monitor can give you logic-analyzer capability within the MCM via the JTAG bus.

### *What Type of Field-Service Requirements Will You Need?*

With boundary scan, you now have the ability to access your circuitry via the 4-wire JTAG port without having to totally disassemble the unit. This provides many options to support field maintenance. Will you want the system to execute system self-test and simply notify the end user as to the source of the fault? Or will the system execute self test and then remotely dial back to the factory with the fault? Will a technician go out to the customer site and connect to the JTAG port with boundary-scan diagnostics on a PC to identify the fault? Each of these options and others are available to you because of boundary scan. The option you choose will depend on the ramifications of system downtime to you and your customer and should assist you in determining your use of boundary-scan devices.

The answers to these questions will determine which products you will need, where they should be placed, and what tools and equipment you will require. Additionally, as you begin to understand the types of boundary-scan components that are needed, you will make decisions as to which vendor is best able to support your testability needs. The TI SCOPE family of testability products is the most comprehensive in the industry and is backed by many years of working with customers and other vendors to solve complex testability problems.

## Available Literature on TI's JTAG Boundary-Scan Logic Products

The items below contain information on TI's bus-interface and scan-support products that are compatible with the JTAG standard. To obtain a copy of any of these items, please contact your local TI sales representative or authorized distributor.

- Boundary-Scan Logic IEEE Std 1149.1 (JTAG) Data Book 1996 (SCTD002A)
- Testability Primer (SSYA002C)
- Testability CD-ROM
- World Wide Web – URL – http://www.ti.com/sc/docs/jtag/jtaghome.htm

## Appendix A – Basics of Boundary Scan

Boundary scan involves placing test points (boundary-scan cells) within each digital I/O of a device. The boundary-scan cell enables the I/O to observe normal data flow through the pin, or the cell can be used to control the state of a pin by providing source data via the serial input (SI). Figure 3 provides a view of the typical boundary-scan cell.

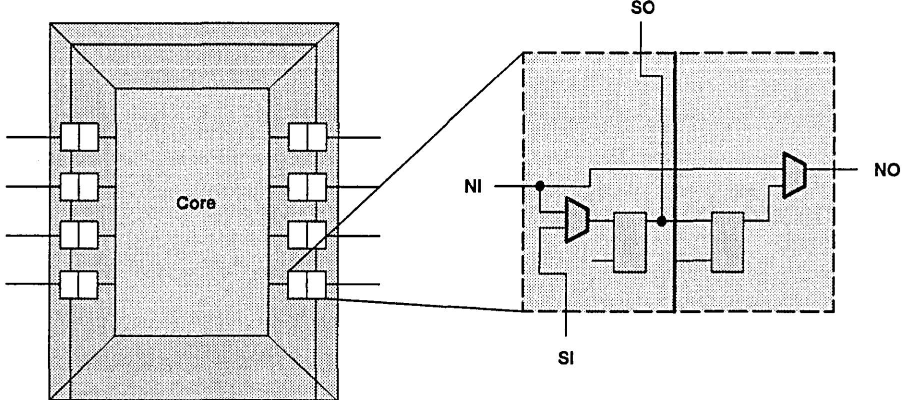



**Figure 3. Boundary-Scan Cell**

Each boundary-scannable device will contain a minimum of four additional pins:

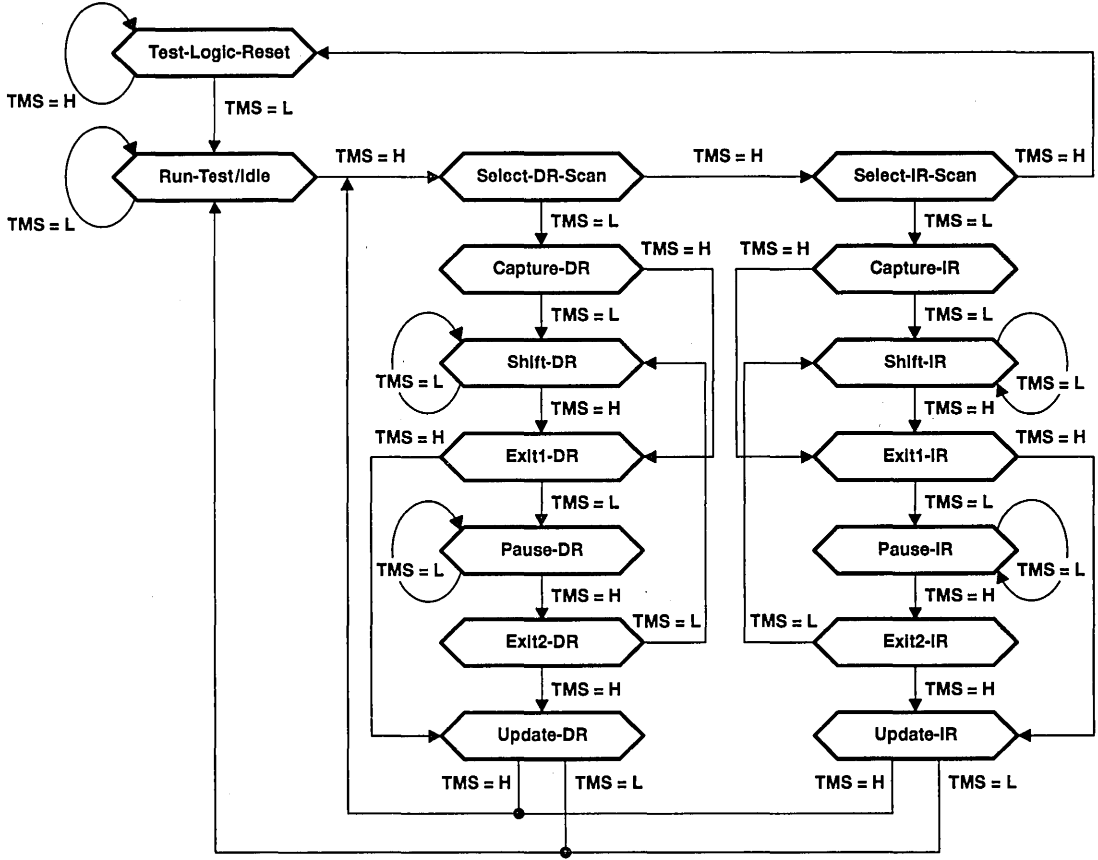
TDI – test data input
TDO – test data output
TMS – test mode select
TCK – test clock

The TDI and TDO pins serve as the path by which serial data enters and exits the device. The TMS and TCK pins control the state of the device, placing it in either test mode or normal mode. In some cases, an optional fifth pin, test reset (TRST) may be included to reset the test logic and return the device to normal mode. Figure 4 shows these four pins as implemented in one of TI's SCOPE octals.

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| $\overline{1OE}$ | 1 | 24 | $\overline{2OE}$ |
| 1Y1 | 2 | 23 | 1A1 |
| 1Y2 | 3 | 22 | 1A2 |
| 1Y3 | 4 | 21 | 1A3 |
| 1Y4 | 5 | 20 | 1A4 |
| GND | 6 | 19 | 2A1 |
| 2Y1 | 7 | 18 | $V_{CC}$ |
| 2Y2 | 8 | 17 | 2A2 |
| 2Y3 | 9 | 16 | 2A3 |
| 2Y4 | 10 | 15 | 2A4 |
| TDO | 11 | 14 | TDI |
| TMS | 12 | 13 | TCK |

**Figure 4. Pinout of TI's SN74BCT8244**

The TMS and TCK signals serve as inputs to control the transition of the device between normal and test modes. These inputs drive a state machine known as the test access port (TAP). The TAP controls serial scanning of instruction or data information through the device and is common to all JTAG/IEEE–1149.1-compliant devices. The TAP state is sequenced based on the state of TMS on the rising edge of TCK, as shown in Figure 5.




16-State TAP provides four major operations: RESET, RUN-TEST, SCAN-DR, and SCAN-IR.
Scans consist of three primary steps: CAPTURE, SHIFT, and UPDATE.

**Figure 5. TAP-Controller State Diagram**

Boundary-scan devices communicate via the serial path from TDO to TDI. This connection is shown in Figure 6. To test the interconnect between two JTAG devices, the user could (for example) serially shift all ones into device 1 and execute an instruction that would drive the data onto the parallel outputs. Device 2 could then be commanded to capture the incoming data at its parallel inputs, transferring the information to the corresponding boundary-scan cells for each input and then serially shift the data to an off-board tester to be compared to the expected results. Any discrepancies in the data can be traced back to the pins where the data mismatch occurs.

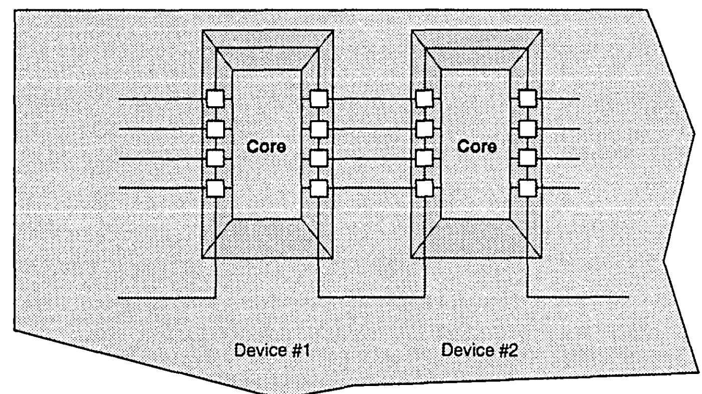



**Figure 6. Scan Path Connecting Two Boundary-Scan Devices**

For more detailed information on boundary scan, please use the boundary-scan training materials cited in this report.

## Appendix B – Boundary-Scan Success Stories

- "We've (AT&T) reduced the number of test points on some boards from 40 down to four and shortened test - debug time on some products from six weeks to two days."[1]
- Hewlett Packard printers reduced the time from the drawing board to production from four and one-half years to two years.[2]
- Test program development time on Intel '386 vs. Intel '486 with JTAG:[3]

| Intel '386 | Intel '486 |
|---|---|
| 7 weeks | 10 hours (2 hours if vendor supplied BSDL) |

- Controller design company using two programmable logic devices with boundary scan were able to use low-cost tester with ATPG ($25K) instead of standard ATE system ($750K) that would have been used without boundary scan.[4]

[1] Computer Design, January 1994, "Testing Dilemmas and Corporate Alliances Fuel Boundary Scan's Acceptance"

[2] Test and Measurement World, October 1992, "Concurrent Engineering is Common Sense"

[3] Computer Design, November 1992, "Design and Test Engineers Alter Rules to Facilitate Test"

[4] EDN, December 3. 1992. "No 'Accounting' for Boundary Scan Test"

# A Look at Boundary Scan From a Designer's Perspective

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SCTA028

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## Abstract

*Much attention has been focused in the past on the benefits of boundary scan to the manufacturing test process and the test engineer. While ultimately the decision to use boundary scan in a given project should be based on positive impact to product life-cycle cost, the benefits that accrue to the designer are often overlooked. This paper describes such benefits to designers at all levels of product design: chip, board, system. It also provides insight into special considerations for the designer who implements or uses boundary scan.*

## Background

Beginning in 1985, several European and North American companies banded together to form the Joint Test Action Group (JTAG). Their stated task was to solve the problem of printed-circuit board (PCB) manufacturing test, which was growing more difficult as integrated circuits (ICs) became smaller and more complex (Figures 1 and 2).[1,2] Their solution was eventually standardized as the IEEE Std 1149.1-1990 Test Access Port and Boundary-Scan Architecture. This standard provides for inclusion of required test resources into ICs themselves.[3]

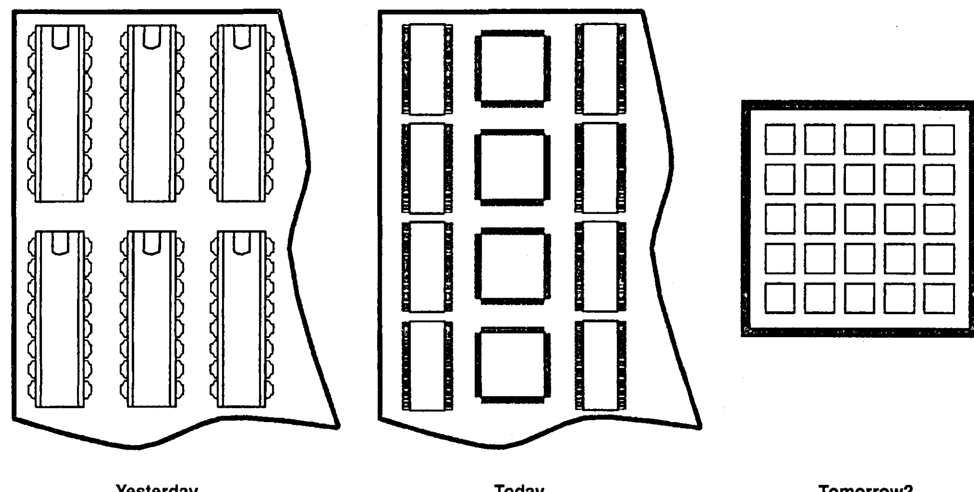



**Figure 1. The Incredible Shrinking Board Results in Loss of Test Access**

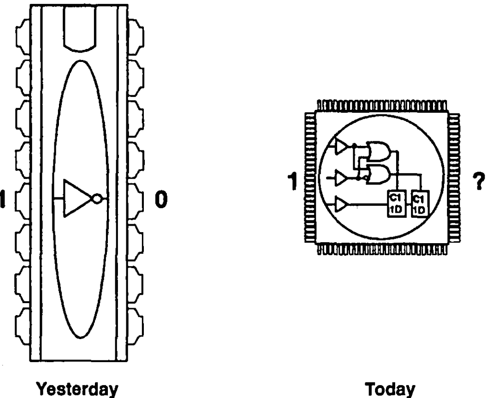



**Figure 2. Increasing Integration at Chip Level Complicates Controllability**

Manufacturing test of PCBs is essentially an effort to find defects (such as net-to-net shorts and solder opens) in the assembly of ICs and other components onto a board. This effort is obviously made more difficult by ICs that are both smaller and more complex. The ability of functional ("edge-connector") test to isolate PCB assembly defects to an adequate level is quickly thwarted by increased board functional density (Figure 3). Since only the primary input/output are used for the test, the difficulty of test generation and the requisite test length grow dramatically as the board complexity increases.[1,2,4]

In-circuit ("bed-of-nails") test, which was an earlier attempt to improve fault isolation in complex boards, is likewise thwarted by increased IC functional density and, further, by physical constraints (Figure 3). Since in-circuit test is based on the physical probing of (preferably all) nets internal to a PCB, smaller pin-to-pin spacing requires improvements in probe technology that are becoming increasingly more difficult and costly. In many cases, such as multichip modules (MCMs), ball-grid arrays (BGAs) and buried signal traces, physical access to internal nodes is not possible at all. Increased functional complexity of ICs causes problems because, in order to place IC outputs in known states for continuity test, the function of the device must be manipulated by often long and complex pattern sequences at IC inputs. A similar argument holds for continuity test at IC inputs.[1,2,4]

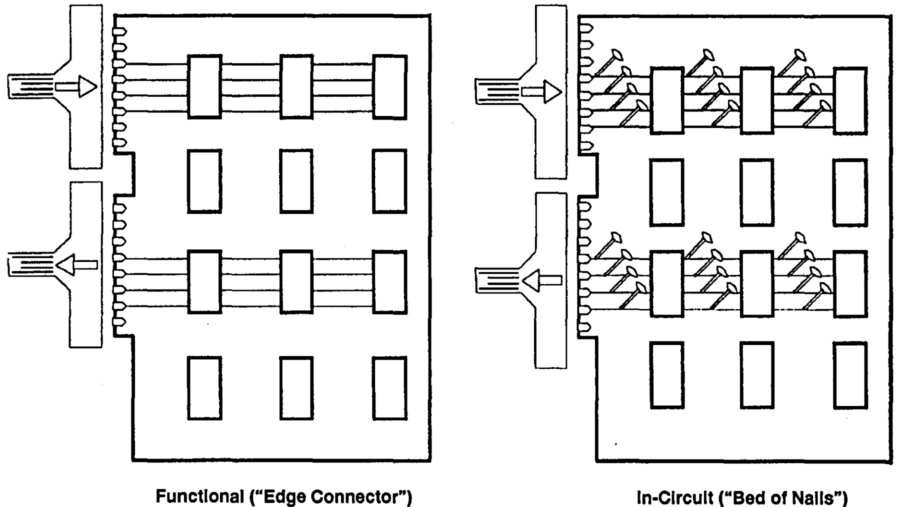



**Figure 3. Traditional Methods of Board Test**

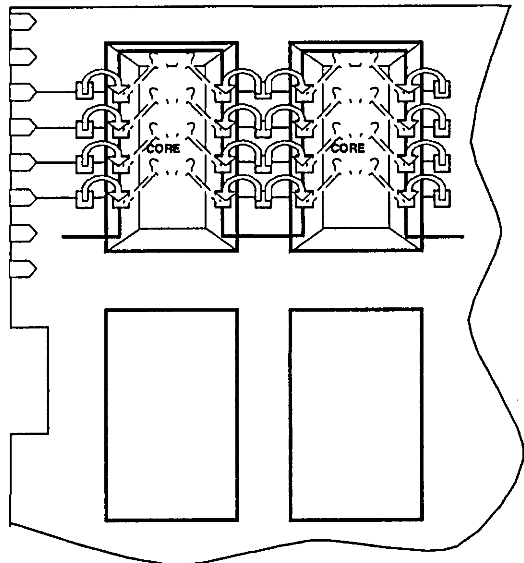



**Figure 4. The Boundary-Scan Idea**

The boundary-scan idea builds on the concepts of in-circuit test. However, physical probes ("nails"), which are placed mid-net, are replaced by boundary-scan cells (BSCs). These "virtual" probes are placed on-chip at IC inputs and outputs (the boundary of the IC), and are therefore placed at the net ends (Figure 4). This results in two major improvements: (1) physical access is no longer required at boundary-scan nets, and (2) continuity test is no longer subject to IC complexity. The net effect is that the goal of manufacturing test, to isolate defects in assembly process to a pin or net, can be accomplished by highly automated test-pattern generation (ATPG).[2]

Finally, in order to provide a means to arbitrarily control and observe these BSCs with minimal pin overhead, the BSCs are designed such that they can be serially concatenated to form a shift register between two IC pins, Test Data Input (TDI) and Test Data Output (TDO). The additional control structures required to select between normal and test operational modes have also been designed to minimize pin overhead and to maximize flexibility to handle test modes in addition to that used for PCB manufacturing test (Figure 5). This Test Access Port (TAP) is based on a state machine (TAP Controller) that operates synchronously to a Test Clock (TCK, to which all operations of the test logic are synchronous) and under the control of a single Test Mode Select (TMS). The TAP Controller explicitly provides for a single instruction register that controls the test modes and for any number of test data registers (including the boundary-scan register) that can be selected by specific instructions.[2]

Standardization of the TAP and TAP Controller, as well as the boundary-scan architecture, has been key to the broad acceptance of the technology across IC, tester, and computer-automated engineering (CAE) tool vendors. Thereby, this structured design-for-test (DFT) technique may be used widely across all types of board designs by all sorts of board manufacturers, even those where catalog ICs and off-the-shelf testers and tools must be used. Additionally, the flexibility of the TAP and TAP Controller allows them to be used for access to other test features built into chip, board, or system, such as on-chip scan test or built-in self-test (BIST).[2]

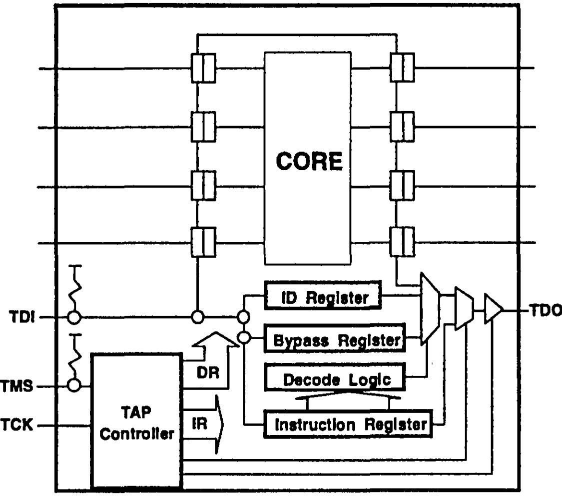



**Figure 5. The Boundary-Scan Control Architecture**

## Use of the Standard by the Board Designer

Since the standard has been designed primarily with board-level (test) concerns in mind, we can expect many benefits for board designers. Although many designers might deny it, they do perform at least one critical "test" operation: design verification/debug. And, just as board manufacturing test benefits from increased observability and controllability, so does board design "test" (that is, verification and debug). Boundary scan, along with other DFT techniques applied at chip or board level, can greatly aid these design test functions.

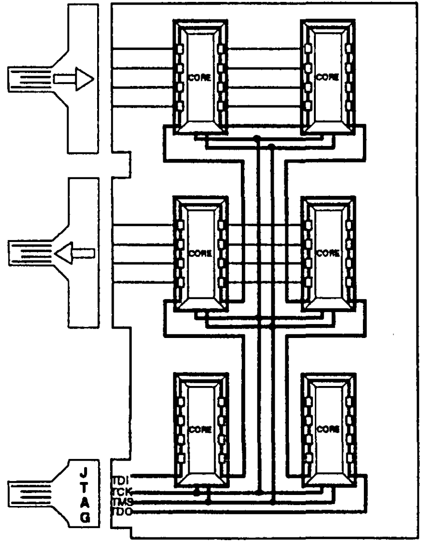



**Figure 6. Board-Level Boundary-Scan Path**

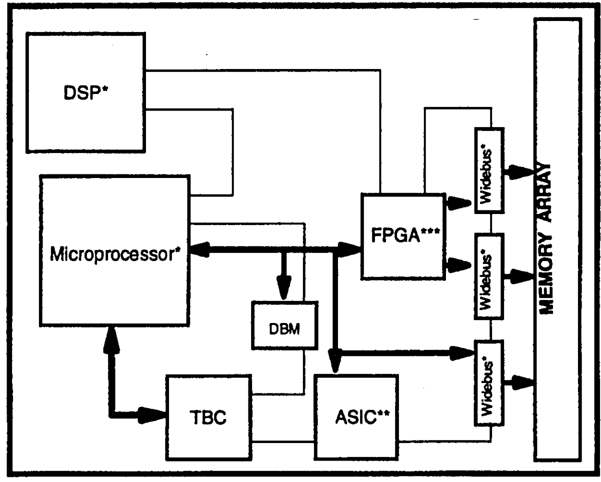
As in the case of manufacturing test, these benefits are derived in two fashions. Where boundary-scan access is provided, observability and/or controllability of a net may be obtained without concern for the function of the driving and/or receiving ICs. Also, no physical access to the board under test is required (Figure 6). One result is that inexpensive test equipment can be used, since tester channels are needed only for the TAP and other primary I/O ("edge connector") signals. Another, perhaps more important result, is that design test can proceed even in cases where physical access to board internal nodes is difficult or impossible (due to board physical characteristics or operating environment[5]).

In the design CAE environment, the designer could have virtually any desired level of observability and controllability to board-internal and (in case of ASICs, FPGAs, or PLDs) chip-internal nodes. With the appropriate boundary-scan and chip-internal scan facilities, the designer can enjoy this same level of access to such nodes in the prototype. Further, a structural ("assembly") test of the prototype can be generated that can be applied from this inexpensive test equipment and without need for expensive test fixturing. Such a test can be automatically generated, given the board netlist and descriptions (in the boundary-scan description language, BSDL) of the boundary-scannable devices. This simple test is available even when manufacturing test program, equipment, and fixtures are not (as is most often the case for prototypes, since they are difficult to provide for an unproved design). Such a test can save many frustrating hours (a testimonial indicates a reduction from 6 weeks to only 2 days[6]) which would normally be required to separate assembly problems from design problems. This is especially important if new and unproved assembly processes have been developed for the board.[5,7,8,9,15]

In some cases, the provision of boundary scan and DFT can permit some prototype testing to begin even in the absence of "key" components. For example, if a processor board were designed with proper planning, associated memory could be tested by emulating the processor, or vice versa.[10]

In addition, the actual design time and manufacturing cost of PCBs may be reduced by elimination of test points.[7,11] If enough test points can be eliminated (one example cites a reduction from 40 down to 4[6]), then possibly some PCB layers can be eliminated as well, which might greatly decrease PCB cost. In some cases, such elimination of test points may be critical to the very miniaturization goal that drives the choice of extremely dense packaging options such as BGAs.[6]

The board designer can obtain these benefits by specifying the use of boundary scan in proprietary ASICs and by placing boundary-scannable catalog (including user-programmable) components wherever possible. The task of finding such components is becoming less difficult daily as the number of such products grows. As of this writing, it has been reported that boundary scan is supported by 22 ASIC vendors, 24 vendors of over 120 standard components and 12 vendors of user-programmable logic (Figure 7).[12]




* catalog: 120 components, 24 vendors
**ASIC: 22 vendors
***user/field-programmable: 12 vendors

**Figure 7. IEEE 1149.1 In Action**

Included in such offerings are boundary-scannable bus interface devices. These reasonably inexpensive components can replace their nonscan counterparts to gain all the above benefits. It may be useful in some cases to insert such devices even where they are not required for normal system function (for example, in parallel to a bus that is not boundary-scannable for performance reasons) in order to improve test access.[13] Often such components may bound simple clusters of nonscannable logic that can be tested using the "virtual nails" of these devices for simple "virtual" in-circuit testing (Figure 8). Additionally, some vendors offer built-in parallel-output pattern generators and parallel-input signature registers that allow the board designer to implement board-level BIST capabilities that provide high fault coverage with very little test pattern generation.[7,14]

In designing the board-level scan chain, a single, simple scan chain is recommended.[4,15] Simple buffering of the TCK and TMS signals should be used, and care should be exercised in the routing, termination, and timing of these signals.[4,10,14] In the prototype, all TAP signals should be checked for signal integrity at their destinations.[10] Failure to maintain signal integrity at these signals may cause improper movement of the TAP controller and premature or unintended entry of device(s) into test modes, such as EXTEST. In such modes, the outputs of the device(s), which would be controlled from the boundary-scan register, might come into contention with those of other scannable or nonscannable devices. In general, the board designer must beware of conditions in which scannable and nonscannable drivers might be in conflict.[4]

Another key to obtaining such benefits will be access to enabling CAE tools. As of this writing, it has been reported that 14 CAE vendors supply tools that support boundary-scan test.[12] These tools fall roughly into three classes: boundary-scan insertion, access analysis, and boundary-scan ATPG. The topic of boundary-scan insertion, since it is a chip design activity, will be discussed later.

Access analysis tools examine board designs prior to layout for nets to which physical test access is not required. Such tools will identify nets in at least three categories: pure boundary-scan (all connected devices have boundary scan), mixed boundary-scan (some, but not all connected devices have boundary scan), and nonboundary-scan (no connected devices have boundary scan).[16] These nets will then be prioritized (in the stated order) for test-point elimination. Such information is then passed to a layout tool (or designer) for elimination of the test points, as required for optimal board layout and fabrication cost.[17]

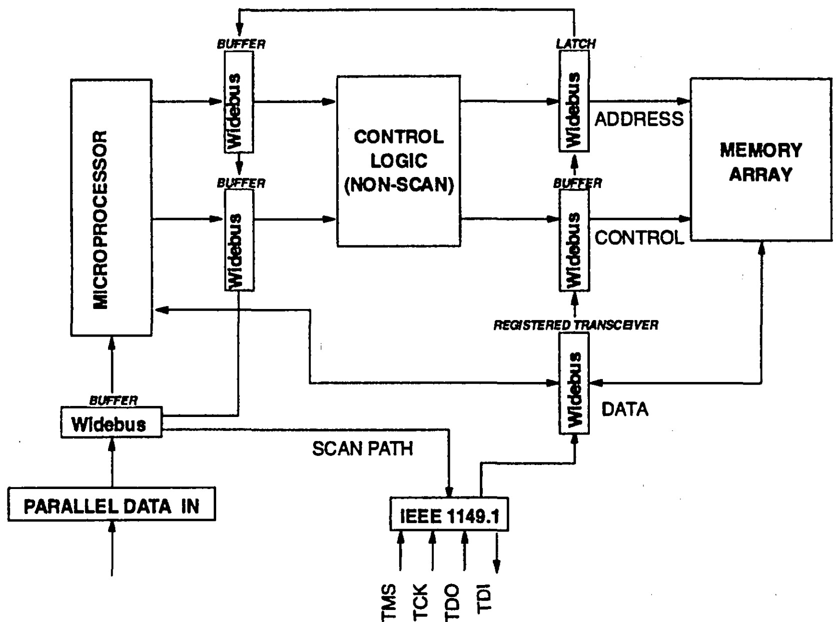



Figure 8. Logic Cluster Test

Boundary-scan ATPG tools automatically generate prototype or manufacturing tests to be applied to the board under test using the board-level TAP. Some of these tools can consider physical access (via in-circuit "bed-of-nails") as well. The best-in-class tools of this type will generate tests for TAP and BSDL validation, and board-level scan-path integrity. These tests, in combination, verify the infrastructure for applying remaining tests. The best-in-class tools generate the following additional types of test for board structural test: boundary in-circuit, virtual interconnect and interactions, and virtual cluster/component test. Boundary in-circuit test uses physical access, but utilizes boundary-scan for simple access to on-chip inputs and outputs for reduced test generation time and complexity. Virtual interconnect and virtual cluster/component tests allow for removal of some or all physical access for test of interconnect and of nonscannable logic clusters, respectively. Such tests will include diagnostics of board assembly faults to the pin. Some tools support multiple board-level scan chains, while others support only a single chain.[6,12,16,17,18]

Some means of boundary-scan test application is required. In some cases, this may be in-circuit or board-functional test equipment that is already owned, perhaps with some modifications to handle deep serial patterns. In other cases, it may be an inexpensive test adapter for PC or workstation. Such "testers" must, at a minimum, exercise the board-level TAP(s) under control of a simple vector file. In either case, to get the most out of boundary scan in design debug, an interactive scan-based diagnostic capability is desired.[10]

The best scan-based diagnostic tools will use a scan-path management database that permits interactive view and control of only those portions of the board (pin, register, bus, or user-defined signal group) that are of interest (Figure 9). Such tools completely hide the complexity of the TAP protocol and boundary-scan chain from the user and allow efficient design debug in the fashion of parallel stimulus generators and logic analyzers to which the design engineer is accustomed. In fact, the best such tools include logic-analyzer-like waveform and state table displays.[19]

Such tools should also support multiple test vector generation methods: interactive, CAE parallel (with automated serialization), and boundary-scan ATPG (based on a standard interchange format such as the Serial Vector Format, SVF). They should also describe the boundary-scan hierarchy using industry standard formats such as BSDL, the Hierarchical Scan Description Language (HSDL), and EDIF (Electronic Design Interchange Format) netlist. And, they must be sensitive to board-level constraints so that physical damage to the board, which might result from improper control of boundary-scan drivers, does not occur.[19]

Finally, they must support scan test and test reuse across all product phases. This means they must allow access to chip-internal scan and BIST, as well as board-level BIST capabilities. They must provide a flow of test information from chip to board to system. Ideally, they will provide a flow to embedded system test, enabling system built-in test based on reuse of scan-based test.[10,19]

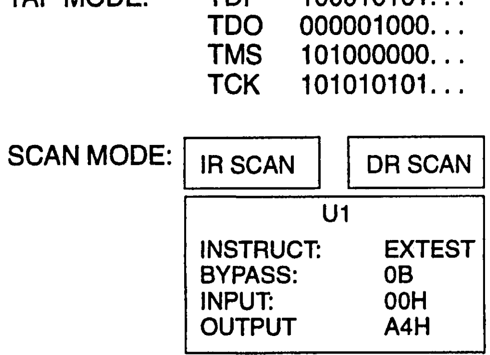



**Figure 9. Scan-Path Management**

## Use of the Standard at Chip Level

At chip level, the standard provides most benefit in its provision for a standard test access method (the TAP) which allows access to chip-internal test facilities in addition to the required boundary-scan test facilities. Such chip-internal test facilities include internal scan path, BIST, and built-in emulation and debug.[5,7,8,10,17,20]

Chip-internal scan path involves the substitution of normal storage elements (latches and flip-flops) with scannable counterparts that can be serially interconnected for test purposes. In a full-scan approach, all such storage elements are replaced, and the circuit is thereby partitioned into blocks of combinational logic between parallel inputs and outputs of a simple shift register. Robust combinational ATPG algorithms can then be used for rigorous structural test of the chip logic. Partial scan implies the replacement of only selected storage elements. It is used in cases where chip area and performance cannot be traded-off for improved fault coverage. However, since not all storage elements are scanned, some sequential ATPG must be used. The failing of such ATPG to provide adequate fault coverage is the primary reason for adopting chip-internal scan in the first place.[21]

BIST uses on-chip stimulus generators and response monitors to eliminate the need for any test generation. Most commonly it uses pseudo-random pattern generation and signature analysis (cyclic redundancy checking) implemented in linear-feedback shift-registers (LFSRs). In such cases, care must be taken that the circuit to be tested is not resistant to pseudo-random techniques. Where the circuit is not suitable for pseudo-random techniques, deterministic BIST methods are possible.[22]

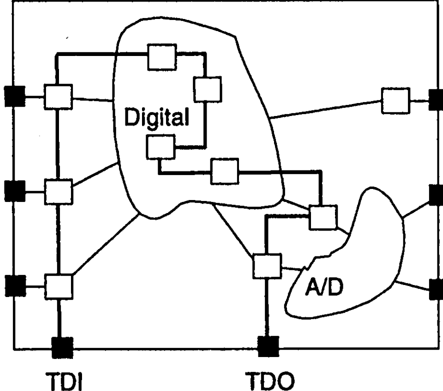



**Figure 10. Boundary Scan Plus Internal Scan In Mixed-Signal Circuit**

Such features are often most powerful when used in combination. For instance, if boundary-scan and chip-internal scan path are both implemented so that they may be used simultaneously in a given IC, then static test application requirements can be reduced to only the four TAP signals, since the boundary-scan register can control/observe the primary inputs/outputs to the core logic (Figure 10).[22] If internal scan path is combined with BIST, the BIST may be used for quick pass/fail testing while the internal scan is used for chip debug and failure diagnosis. Additionally, if a standard RUNBIST capability is provided, the end user may perform quick function testing while the IC is in-system.[23]

Finally, boundary scan alone can reduce test access requirements to the TAP only. The same static functional vectors that would be applied by an expensive IC tester with many parallel channels can be applied through boundary scan (if INTEST capability is provided). Setup of ICs for parametric test can also be facilitated by boundary scan. And boundary scan can be used in hostile environments where physical access is difficult or impossible.[5] For mixed-signal ICs, inclusion of boundary scan can provide a very useful partitioning of analog and digital functions, allowing each to be tested independently (Figure 10).[24]

To benefit from these capabilities, they must be designed into the chip. Several types of CAE tools can aid this process. Most such tools provide for some level of automation of internal (full or partial) scan, BIST, and boundary scan. The abstraction level at which these tools operate ranges from register-transfer level down to gate level, and the point of use ranges from pre-synthesis to post-synthesis (or schematic capture). In the area of internal scan insertion, the best tools will provide full scan insertion and partial scan insertion driven from chip area, performance, and test coverage constraints. They will also provide the combinational and/or sequential ATPG needed to capitalize on the scan path.[6,12,21]

Boundary-scan insertion tools are similarly varied. Capabilities to look for besides automated insertion of TAP and boundary-register are BSDL output, test pattern generation for standard-conformance checking and BSDL validation. Some tools use BSDL (or graphical entry) as an input, rather than an output, to the boundary-scan insertion process.[18]

The need for validation of BSDL and TAP integrity cannot be overstated since the entire test infrastructure is based upon proper operation of these components.[4,17] Special attention should be given to TAP pin placement and to considerations for proper clocking of internal scan path relative to boundary-scan path.[4,25]

## Use of the Standard at System Level

Finally, the standard can bring benefits to design at system level also. Such benefits are primarily derived from the ability for TAP-accessed tests to be reused at higher levels of product integration, from chip to board to system.[1,7] These capabilities may be used for system hardware debug and hardware/software integration while chips and boards are in their normal system configuration and operating environment. Since no physical access is required, use of "extender" cards, complex connectors, and large environmental control systems is not needed.[5,7,8]

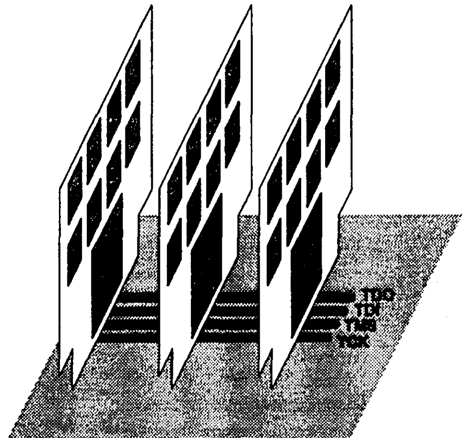


**Figure 11. Multidrop System TAP**

Additionally, boundary scan and other TAP-accessed test facilities may be useful in meeting system design requirements for built-in test, field service test, and remote diagnostics. Clearly, in most such cases it is desirable to limit the expense and complexity of test equipment required. Boundary scan can facilitate this by limiting test access and control requirements to an inexpensive diagnostics port (the TAP).[7,20]

Boundary-scannable bus interface devices can be useful in these applications, as well, by partitioning the system along field-replaceable unit (PCB) boundaries. Also, if the backplane interface of PCBs is scannable, then backplane connectivity and integrity testing can be performed. By using the previously mentioned pattern generation and signature analysis techniques, it is even possible to perform gross performance testing on the backplane.[14]

One problem in the area of system implementation of TAP access is referred to as the multidrop problem (Figure 11). Since TDI and TDO are serial terminals, they must be daisy-chained in simple chains. This "ring" configuration presents a problem in backplane-oriented systems, since some boards may be removed, disabling the scan chain. An alternative, proposed by the standard, is the "star" configuration which allows TDI and TDO pins on PCBs to be bussed.[3] However, since multiple TMS signals are required to prevent simultaneous scanning (and thereby contention on TDO bus) of PCBs, many backplane routing channels are required. Several alternative multidrop schemes, based on serial addressing techniques, have been proposed to alleviate this problem. The best of these techniques will enable multidrop routing of backplane signals, with minimal need for test reformatting and minimal impact on test application time.[1,4,6,7,20,26]

## Conclusion

We have discussed many benefits that are available to designers through use of the Test Access Port and Boundary-Scan Architecture. These benefits are primarily in the area of design verification and debug and are enabled by improved controllability and observability into circuits, and freedom from physical access constraints provided by boundary scan. While some effort is certainly required to derive such benefits, a suite of CAE tools that reduces such effort has been presented. Designers at all levels of product integration (chip, board, system) are encouraged to evaluate boundary scan for benefits that they and their companies may derive from its use.

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# Boundary Scan Speeds Static Memory Tests

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*Semiconductor Group*

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# BOUNDARY SCAN SPEEDS STATIC MEMORY TESTS

## THE BOUNDARY-SCAN STANDARD CAN SUPPLY ACCESS NEEDED TO CONTROL BUILT-IN SELF-TEST FUNCTIONS.

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The steady increase in memory densities used in microprocessor-based systems has stretched functional test times, as large memories require time-consuming tests for adequate fault coverage. Moreover, using high-density ASICs with embedded memory limits physical test access. Wide buses and high bus fan out further complicate testing by limiting component fault isolation. Fortunately, the IEEE-1149.1 boundary-scan standard offers a solution to the problem of testing static memory.

The boundary-scan standard was initially conceived to test board interconnections without the need for physical probing. The standard requires the inclusion of boundary-scan functions on ICs, and its success is evidenced by willingness of silicon vendors to add that capability to their new products. Boundary-scan devices available now include general microprocessors, digital-signal processors, field-programmable gate arrays, ASIC libraries (standard cell and gate arrays), and bus-interface components.

Designers of microprocessor-based applications typically buffer the processor's address and data buses to solve electrical loading or isolation problems. If the bus-interface parts are IEEE-1149.1 compatible, then boundary-scan functions can be used to test the memory.

One technique uses boundary-scan instructions to scan in the address value and the data value, set a memory strobe active to perform the memory access, and set the memory strobe inactive to complete the cycle. Because these multiple-scan steps must be done for each memory address, this technique is very scan-intensive and therefore very time consuming. For extremely large memory arrays, the process could require millions of IEEE-1149.1 scan operations and take hundreds of minutes to perform.

A better solution, which can speed up test execution time by a factor of hundreds, employs IEEE-1149.1-controlled built-in self-test (BIST) with off-the-shelf components or ASIC macros. With either method, the fault detection and isolation provided by a given memory test will depend on the stimulus patterns used. To compare the two techniques, a 256-by-8-bit memory array and associated bus-interface and control logic was constructed *(Fig. 1)*. This configuration allows for explicit read/write operations using the IEEE-1149.1 Extest and Sample instructions. The IEEE-1149.1 components, which have a BIST capability controlled by boundary-scan methods, can also perform the memory read/write operations.

Two tests were run on the memory. The first explicitly scanned in the RAM array address, data, and strobe signal; the second executed IEEE-1149.1-controlled BIST, which generated the address, data, and strobe signals automatically at the test clock (TCK) rate of 6.25 MHz. The boundary-scan technique solved the problem of direct physical access, but was time consuming *(Table 1)*. The second test, however, clearly showed the advantage of IEEE-

**TABLE 1: BOUNDARY SCAN VERSUS CONTROLLED BIST**

| Mode | 256 accesses | 1,000,000 accesses |
|---|---|---|
| IEEE 1149.1 (Extest & Sample) | | |
| Time to apply | 4.8 sec. | 332.00 min. |
| Scans | 512 | 2,000,000 |
| Patterns | 512 | 2,000,000 |
| IEEE 1149.1 (with BIST capability) | | |
| Time to apply | 0.011 sec. | 0.75 min. |
| Scans | 7 | 28,000 |
| Patterns | 512 | 2,000,000 |

1149.1-controlled BIST. That is, by using IEEE-1149.1-controlled BIST circuitry embedded within the functional logic surrounding large memory arrays, designers can closely emulate the actual functional characteristics and timing speeds of the memory being accessed.

This article describes how to implement this solution using Texas Instruments Scope bus-interface components. These are off-the-shelf devices that offer the IEEE-1149.1-controlled BIST functionality needed to test static memory. The Scope devices also supply the electrical signal conditioning and buffering a design engineer would typically design around a microprocessor.

## Generating Patterns

First, a few comments regarding deterministic and algorithmic patterns. Using algorithmically generated patterns for memory-array tests is an accepted engineering practice commonly used in software-based built-in test (BIT) code. Deterministic patterns that can't be generated with a BIST algorithmic circuit would require more memory to store the patterns than the memory array that's being tested.

Various memory-testing algorithms are available. Each technique specializes in detecting and isolating particular memory faults. Once the engineer analyzes the memory fault classes and testing approaches applicable to a given design, the appropriate BIST structures can be integrated into the processor, ASIC, or bus-interface components.

The size of the memory array is important in determining the desired width of the BIST structure bounding the address and data buses. An octal bus-interface component can generate only 256 unique patterns from its BIST circuit. So, if two 8-bit octals are used on a 16-bit bus, the BIST must be executed 256 times to cover a 64-kbit memory space.

The Scope 8-bit octal bus interface components provide flexible, generic types of BIST structures that support several memory-testing algorithms. The 8-bit biCMOS technology (BCT) devices have BIST structures for pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), concurrent PSA/PRPG, and Toggle/Sample. The 8-bit advanced biCMOS technology (ABT) versions have the same capabilities as the BCT parts, and add a Count-up (256 patterns) function at the outputs. The 18- and 20-bit Widebus Scope bus interface components generate 256-kbit and 1-Mbit unique patterns, respectively, in one BIST execution. These parts also have advanced BIST capabilities, including the Count-up function of the ABT devices.

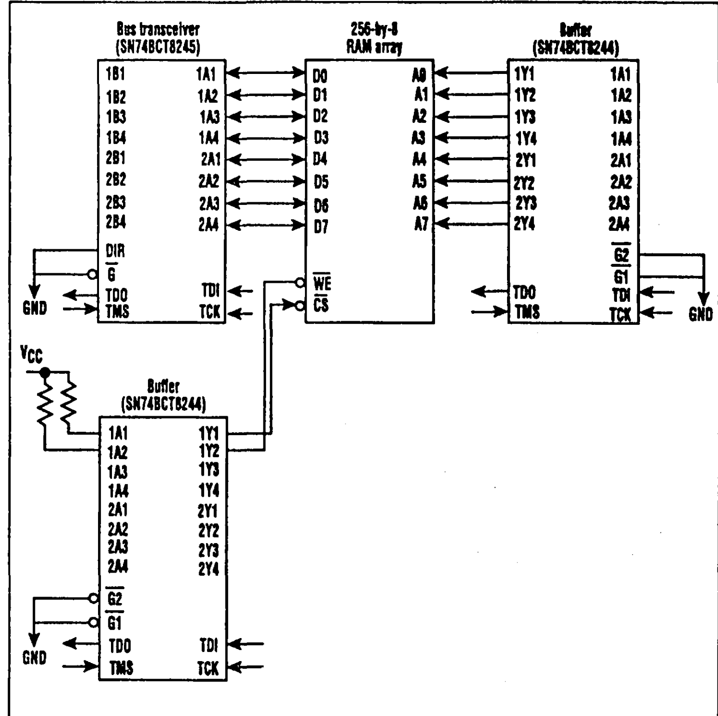
The example circuit uses the BCT octal bus interface components, so a review of their BIST functions is appropriate at this point. Specifically, the following descriptions of PRPG, PSA, combined PSA/PRPG, and Toggle/Sample patterns apply to the BCT8240, BCT8244, BCT8245, BCT8373, and BCT8374.

For PRPG, the patterns are generated at the functional outputs. The user should select an initial seed value and scan it into the boundary-scan register before performing the scanning sequence required to place the device into PRPG *(Table 2)*. After the Instruction Register (IR) scan of step 5 is completed and the test access port (TAP) has entered the Run-Test/Idle state, the device outputs begin generating pseudo-random patterns.

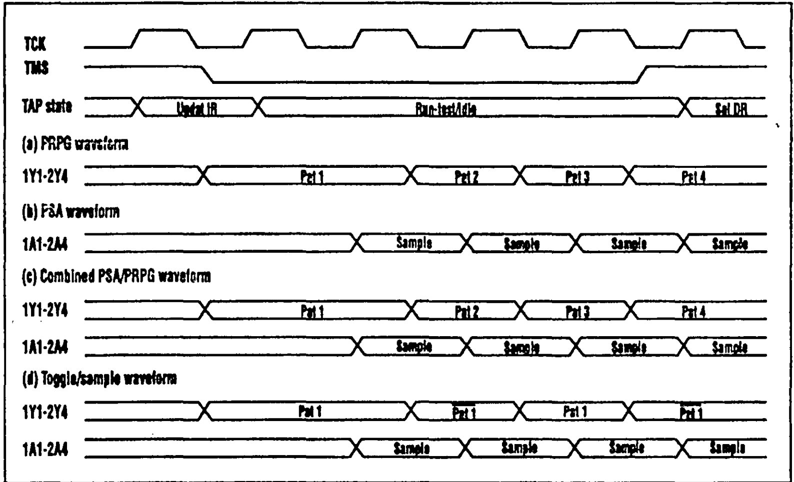
The timing relationship of these patterns to TCK and test mode select

**TABLE 2: SCAN SEQUENCE FOR PRPG**

| Step | Type | Data scanned into device | Register accessed |
|---|---|---|---|
| 1 | IR scan | READBN opcode | Instruction |
| 2 | DR scan | Initial seed (16 bits) | Boundary register |
| 3 | IR scan | SCANCN opcode | Instruction |
| 4 | DR scan | b'01' (PRPG) | Boundary control |
| 5 | IR scan | Runt opcode | Instruction |
| 6 | IR scan | Bypass opcode | Instruction |




**1. A SIMPLE CIRCUIT CONSISTING** of a memory array and associated bus-interface and control logic was constructed in order to evaluate two memory test methods.




**2. THIS timing diagram shows the relationship between the IEEE-1149.1 signals—TCK, TMS, and TAP state—and the different types of test data signals that can be used to test the memory.**

(TMS) is given in Figure 2a. The Scope octal's outputs change value after the falling edge of TCK while the TAP is in Run-Test/Idle and the current instruction register is loaded with the instruction Runt.

All Scope octals use an internal 16-bit linear feedback shift register (LFSR) for PRPG. The devices must receive a total of 65,535 TCKs in order to generate every sequence combination of 8-bit (octal) output values. The sequence of these values is pseudo-random, based on the initial seed value written into the boundary-scan register. The seed can be any value between x0001 and xFFFF. A seed of x0000 causes the LFSR to remain at x0000. After 65,535 TCKs, the output pattern sequence begins to repeat.

The 16-bit PRPG function can be used to generate input patterns for the data bus when performing memory write operations. This function would not normally be used for generating address patterns because it would take more than 256 TCKs to ensure that all 256 memory locations were accessed.

## USING PSA

When the PSA function is used, data appearing on the eight functional data inputs is compressed into a 16-bit signature. As with PRPG, an initial seed value must be scanned into the boundary-scan register before the scanning sequence required to place the device into PSA is performed *(Table 3)*. The compression occurs after the IR scan of step 5 is completed and the TAP enters the Run-Test/Idle state.

The timing relationship of the data sampling to TCK is shown in Figure 2b. The A-inputs of the Scope octal devices are sampled on the rising edge of TCK, while the TAP is in Run-Test/Idle and the current instruction register is loaded with the instruction Runt.

The PSA function uses the 16-bit LFSR to generate the 16-bit signature, based on the initial seed value loaded in the boundary-scan register. The 16-bit seed can be any value between x0000 and xFFFF. The seed value chosen will affect the validity of the signature and the detection of faulty patterns. Therefore, the engineer should carefully study the nature of the LFSR's signature analysis in order to understand aliasing conditions. Aliasing occurs when multiple input-pattern combinations produce the same final signature. If that happens, certain memory data faults could be masked and thus go undetected.

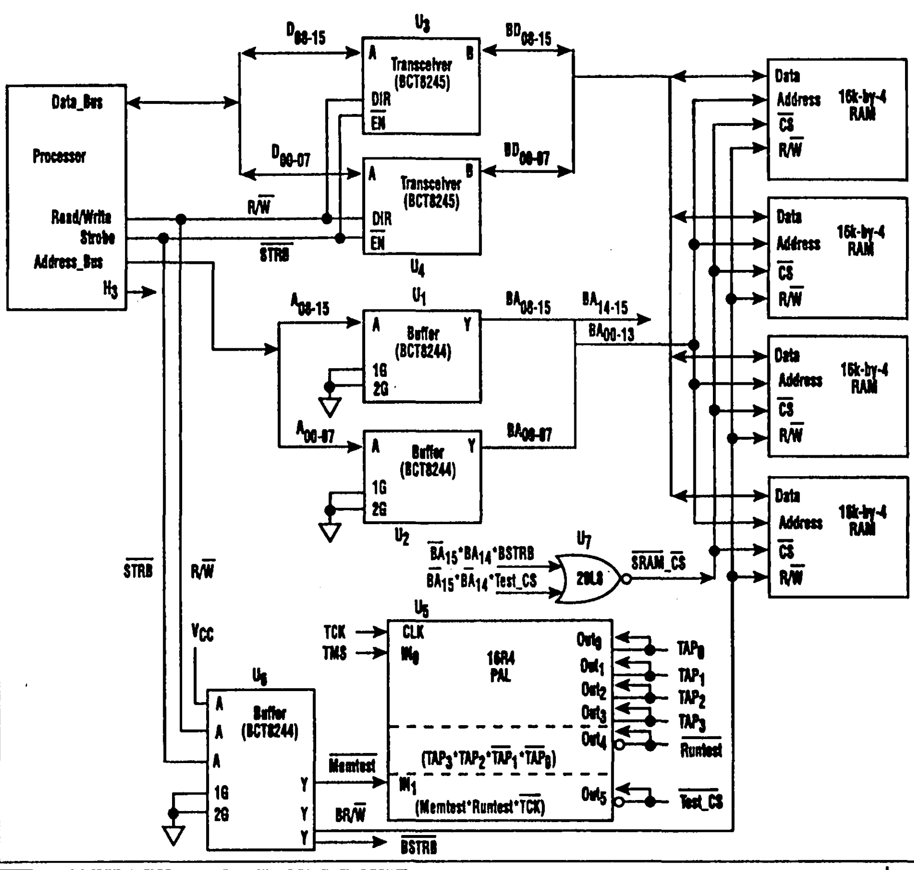
The PSA mode would typically be used when verifying the validity of known data previously written to a block of memory. Using the 16-bit PSA function of a Scope octal device reduces the chance of aliasing.

As noted, the Scope octals can also combine PRPG and PSA operations. In this mode, the devices simultaneously generate pseudo-random patterns on the outputs while compressing a signature on the inputs. The IEEE-1149.1 scan operations needed to set up a device for combined PSA/PRPG operation are similar to those for the PSA mode *(Table 3, again)*. One difference is that the 16-bit seed value is split into two 8-bit seeds, one for PRPG and the other for PSA (step 2). In addition, the boundary-control register should be loaded with a b'11' value (step 4). After the IR scan of step 5 is completed and the TAP enters the Run-Test/Idle state, the octal's outputs begin generating PRPG patterns and the inputs are compressed. The timing relationship of these operations to TCK is shown in Figure 2c.

Because the two 8-bit seeds split the 16-bit LFSR, only 255 TCKs are required to generate every PRPG output value, and the device generates only an 8-bit PSA signature. After 255 TCKs, the output PRPG sequence repeats itself. Because of the nature of an LFSR, the eight outputs will never be all zeros. Because only 8 bits of the LFSR are used for PSA, the possibility for aliasing increases. Consequently, the 8-bit PRPG func-

**TABLE 3: SCAN SEQUENCE FOR PSA**

| Step | Type | Data scanned into device | Register accessed |
|---|---|---|---|
| 1 | IR scan | READBN opcode | Instruction |
| 2 | DR scan | Initial seed (16 bits) | Boundary Register |
| 3 | IR scan | SCANCN opcode | Instruction |
| 4 | DR scan | b'10' (PSA) | Boundary Control |
| 5 | IR scan | Runt opcode | Instruction |
| 6 | IR scan | READBN opcode | Instruction |
| 7 | DR scan | Resulting signature | Boundary Register |




**3. IN THE EXAMPLE TEST CIRCUIT,** several bus-interface devices partition the address and data buses to facilitate boundary scan around the microprocessor.

tion could be used to produce memory addresses, since 255 address values can be generated within 255 TCKs. But the 8-bit PSA function would not be recommended for sampling memory data because of the greater possibility of aliasing.

In the Toggle/Sample mode, the octal device generates a toggle pattern at the functional outputs while the inputs are sampled. Once again, the scan operations used to set up the octal for Toggle/Sample mode are similar to those for PSA setup. Two 8-bit seeds are entered (step 2). The first is the initial value of the toggle pattern at the outputs, and the second isn't used. To configure the octal for this BIST function, the boundary control register should be loaded with a b'00' value (step 4). As in the other modes, the octal's outputs begin to toggle after the IR scan of step 5 is completed and the TAP enters the Run-Test/Idle state.

The timing relationship of these patterns to TCK is shown in Figure 2d. The outputs of the Scope octal change value after the falling edge of TCK, and the TAP is in Run-Test/Idle and the current instruction register is loaded with the instruction Runt. The toggling output function could also be used for generating memory data input patterns, such as 55/AA, FF/00, and so on.

An example circuit consists of a generic microprocessor, a static RAM array, two PALs, and several Scope octal ICs *(Fig. 3)*. The microprocessor has a 16-bit address bus and a 16-bit data bus, as well as read/write (R/W) and address strobe ($\overline{STRB}$) control signals. The Scope octal devices partition the address and data buses to facilitate boundary scan around the microprocessor. Specifically, $U_1$ and $U_2$ (BCT8244 types) buffer the microprocessor's address bus, and $U_3$ and $U_4$ (BCT8245 types) are transceivers on the microprocessor's data bus. $U_6$ (a BCT8244) buffers the processor's R/W signal and other control signals.

**TABLE 4: MEMORY MAP AND ADDRESS DECODER**

| Address range $BA_{00}$-$BA_{15}$ | Memory selected |
|---|---|
| 0000-3FFF | Not defined |
| 4000-7FFF | RAM array (to be tested) |
| 8000-FFFF | Not defined |
| !SRAMCS = ((!BA15 & BA14 & BSTRB) # (!BA15 & BA14 & TSTCS)) | |

For simplicity, the example circuit doesn't detail the data-transfer acknowledgement logic. The signal $H_3$ is the microprocessor's functional clock, from which all functional read/writes are timed *(Fig. 4)*.

The circuit's memory map and address decoder equation, including the buffered upper address lines, $BA_{14}$, and $BA_{15}$, are defined in Table 4. To select the memory resource to be tested by the BIST function, $BA_{14}$ and $BA_{15}$ must be controlled properly to generate the necessary chip select. The 20L8 PAL, $U_7$, generates a chip select to the RAM array, $\overline{SRAM_CS}$.

The logic equation generating $\overline{SRAM_CS}$ has two product terms

# BOUNDARY-SCAN MEMORY TESTS

(P-Terms). The first generates the "functional operation" chip select; the second supports IEEE-1149.1 BIST testing. When $BA_{15}$ is a logic 0 and $BA_{14}$ is a logic 1 and $\overline{STRB}$ is a logic 0, the output $\overline{SRAM_CS}$ is a logic 0. This enables the RAM array (via the chip-select pin).

The second term is logically ORed with the first and supports the BIST operation. $U_1$ (the octal that buffers the upper address bus) must be loaded with the Extest instruction and must drive the upper address lines, $BA_{00-15}$. The output $\overline{SRAM_CS}$ is a logic 0 when $BA_{15}$ is a logic 0, $BA_{14}$ is a logic 1, and $\overline{Test_CS}$ is a logic 0. The lower address lines, $BA_{00-07}$, are driven by $U_2$'s PRPG BIST circuit.

The 16R4 PAL, $U_5$, generates the $\overline{Test_CS}$ signal at the appropriate time to allow the IEEE-1149.1 BIST functions to time properly with the RAM circuitry. This device holds three logic components.

The first logic component has two inputs—TCK and TMS. The TMS signal is sampled on every rising edge of TCK, just as in other IEEE-1149.1 devices. By sampling TMS, the PAL logic can monitor the TAP state of the IEEE-1149.1 scan bus. The TAP has 16 possible states, encoded into four outputs defined as $TAP_0$-$TAP_3$ *(Table 5)*.

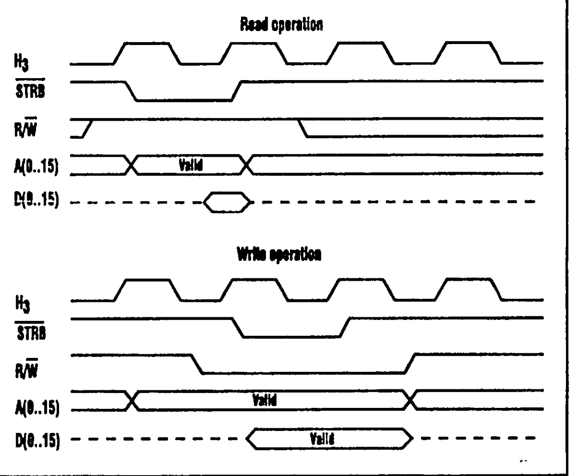
The PAL's second logic component generates the output signal $\overline{Runtest}$. This signal is asserted (logic 0) whenever the TAP is in the Run-Test/Idle state. This signal, which indicates when the TAP is in Run-Test/Idle state, is important. When the TAP is in this state and the octal is loaded with the Runt instruction, the BIST circuitry generates pseudo-random patterns or compresses a PSA signature.

The third logic component actually generates the $\overline{Test_CS}$ signal. While the octals are performing the BIST in the Run-Test/Idle state, this PAL needs to know when the Runt instruction is loaded into the octals. A scannable signal, $\overline{Memtest}$, is used to accomplish this. $U_6$, a BCT8244 octal buffer, drives this signal.

The equation for $\overline{Test_CS}$ is:

$\overline{Test_CS}$ = (Memtest * Runtest * $\overline{TCK}$)

Software performing the IEEE-1149.1 scan operations must set the $\overline{Memtest}$ signal low at the same time that the Runt instruction is loaded into the octals performing PRPG and PSA.




**4. THE READ/WRITE WAVEFORMS** for the example circuit show the relationship between the microprocessor's functional clock, $H_3$, and the appropriate signals.

**TABLE 5: DEVICE U5 TAP STATE DEFINITION**

| Output | | | | |
|---|---|---|---|---|
| $TAP_3$ | $TAP_2$ | $TAP_1$ | $TAP_0$ | TAP State |
| 1 | 1 | 1 | 1 | Strap |
| 1 | 1 | 0 | 0 | Run-Test/Idle |
| 0 | 1 | 1 | 1 | Select_DR |
| 0 | 1 | 0 | 0 | Select_IR |
| 0 | 1 | 1 | 0 | Capture_DR |
| 0 | 0 | 1 | 0 | Shift_DR |
| 0 | 0 | 0 | 1 | $Exit_1$_DR |
| 0 | 0 | 1 | 1 | Pause_DR |
| 0 | 0 | 0 | 0 | $Exit_2$_DR |
| 0 | 1 | 0 | 1 | Update_DR |
| 1 | 1 | 1 | 0 | Capture_IR |
| 1 | 0 | 1 | 0 | Shift_IR |
| 1 | 0 | 0 | 1 | $Exit_1$_IR |
| 1 | 0 | 1 | 1 | Pause_IR |
| 1 | 0 | 0 | 0 | $Exit_2$_IR |
| 1 | 1 | 0 | 1 | Update_IR |

!RUNTEST = ($TAP_3$ * $TAP_2$ * !$TAP_1$ * !$TAP_0$)

The designer must be able to shut off the microprocessor or hold it in a reset state while the test is executing. Thus, the processor should be controllable via an IEEE-1149.1 scannable register. Table 6 defines the scan operations required to perform BIST memory writes to RAM addresses 4001-40FF, using pseudo-code to generate both the address and data patterns. Device $U_2$ generates pseudo-random addresses on signals $BA_{00-07}$, and devices $U_3$ and $U_4$ generate pseudo-random data on signals $BD_{00-15}$ *(Table 6)*.

The following steps execute the BIST memory write operation:

*Step 1* loads all Scope octals with a READBN instruction, which allows access to the octal boundary-scan register (BSR) while the octals remain in their functional mode.

*Step 2* involves a Data Register scan that initializes the BSRs of each octal device. $U_1$ ($BA_{08-15}$) is set up with the desired RAM memory address and $U_2$ ($BA_{00-07}$) is loaded with a PRPG seed value. Both $U_3$ ($BD_{08-15}$) and $U_4$ ($BD_{00-07}$) are loaded with a PRPG seed value. $U_5$ is set up with the Memtest signal asserted (logic 0), and the read/write-signal (BR/$\overline{W}$) logic level selecting a write (logic 0) operation.

*Step 3* is an Instruction Register scan that loads the octals $U_2$, $U_3$, and $U_4$ with the SCANCN instruction. This instruction allows access to the boundary control register (BCR). $U_1$

## TABLE 6: PSEUDO-CODE FOR MEMORY WRITE OPERATIONS

| Sequence and type | $BA_{08}$-$BA_{15}$ $U_1$ | $BA_{00}$-$BA_{07}$ $U_2$ | $BD_{08}$-$BD_{15}$ $U_3$ | $BD_{00}$-$BD_{07}$ $U_4$ | $\overline{Memtest}$ and BR/$\overline{W}$ $U_5$ |
|---|---|---|---|---|---|
| **Shut off the embedded microprocessor | | | | | |
| 1. IR | READBN | READBN | READBN | READBN | READBN |
| 2. DR | $BA_{15}=0$ $BA_{14}=1$ $BA_{08-13}=000000$ | LFSR seed | LFSR seed (set direction A → B) | LFSR seed | BR/$\overline{W}$=0 $\overline{Memtest}$=0 |
| 3. IR | Bypass | SCANCN | SCANCN | SCANCN | Bypass |
| 4. DR | Bypass 0 | PSA/PRPG 11 | PSA/PRPG 11 | PSA/PRPG 11 | Bypass 0 |
| 5. IR | Extest | Runt | Runt | Runt | Extest |
| **Hold in 1149.1 Run-Test/Idle state for 255 Test Clocks (TCKs) | | | | | |
| 6. IR | READBN | READBN | READBN | READBN | READBN |
| 7. DR | $BA_{15}=0$ $BA_{14}=1$ $BA_{08-13}=000001$ | LFSR seed | LFSR seed (set direction A → B) | LFSR seed | BR/$\overline{W}$=0 $\overline{Memtest}$=0 |

and $U_5$ are loaded with the Bypass instruction.

*Step 4* is a Data Register scan that loads the $U_2$, $U_3$, and $U_4$ BCRs with the PSA/PRPG code (11).

*Step 5* is an Instruction Register scan that loads $U_2$, $U_3$, and $U_4$ with the Runt instruction and loads $U_1$ and $U_5$ with the Extest instruction. Extest allows the previously loaded values for BA, BR/$\overline{W}$, and $\overline{Memtest}$ to be asserted when the TAP enters the Update-IR state. When the TAP enters the Runtest/Idle state, $U_2$, $U_3$, and $U_4$ begin generating PRPG patterns *(Fig. 5)*.

*Step 6* is an Instruction Register scan that puts the octals into their functional mode. It also deasserts $U_5$'s Memtest signal (logic 1), preventing Test_CS from being generated when the Runtest/Idle state is reentered.

*Step 7* is a Data Register scan that sets up the memory write operation for the next block of memory.

Similarly, the scan operations needed for memory read operations read from RAM addresses 4001-40FF. $U_2$ generates pseudo-random addresses on address bus signals $BA_{00-07}$, and devices $U_3$ and $U_4$ compress a signature from data bus signals $BD_{00-15}$ *(Table 7)*.

The following steps are required in order to execute the memory read operation:

*Step 1* loads the octals with the READBN instruction, which allows access to the octal BSR while the octals remain in their functional mode.

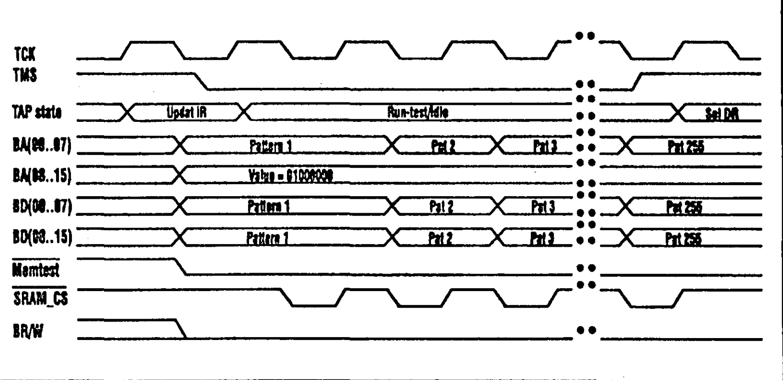
*Step 2* is a Data Register scan that initializes the Scope octals' BSRs. $U_1$ ($BA_{08-15}$) is set up with the desired RAM memory address and $U_2$ ($BA_{00-07}$) is loaded with a PRPG seed value. Both $U_3$ ($BD_{08-15}$) and $U_4$ ($BD_{00-07}$) are loaded with a PSA seed value. $U_5$ is set up with the Memtest signal asserted (logic 0), and the read/write signal BR/W logic level selects read (logic 1).

*Step 3* is an Instruction Register scan that loads octals $U_2$, $U_3$, and $U_4$ with the SCANCN instruction, permitting access to the boundary control register. $U_1$ and $U_5$ are loaded with the Bypass instruction.

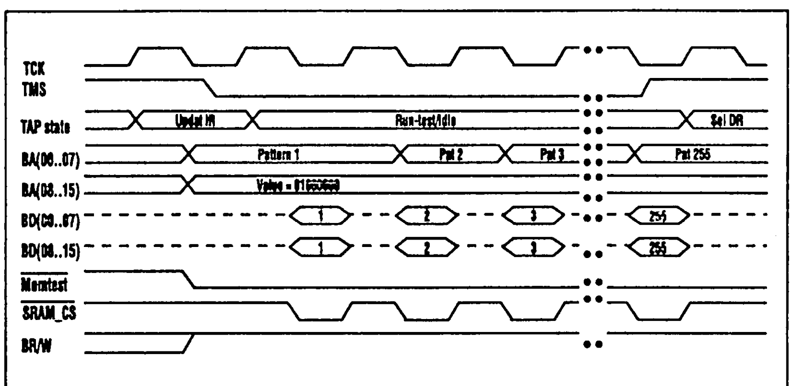
*Step 4* is a Data Register scan that loads the $U_2$, $U_3$, and $U_4$ boundary control register with the PSA/PRPG code (11) and PSA code (10).

*Step 5* is an Instruction Register scan that loads $U_2$, $U_3$, and $U_4$ with the Runt instruction and loads $U_1$ and $U_5$ with the Extest instruction. The Extest instruction allows the previously loaded values for $BA_{08-15}$, BR/$\overline{W}$, and $\overline{Memtest}$ to be asserted when the TAP enters the Update-IR state. When the TAP enters the Runtest/Idle state, $U_2$ begins generating PRPG patterns and $U_3$ and $U_4$ begin compressing a signature.

*Step 6* is an Instruction Register scan that puts the octals into functional mode. It also deasserts octal device $U_5$'s Memtest signal (logic 1),




**5. THE BIST-GENERATED** PRPG patterns for memory write operations are created after $U_2$, $U_3$, and $U_4$ are loaded with the Runt instruction, and the TAP enters the Run-test/Idle state.




**6. THE BIST-GENERATED** waveforms for memory read operations are created after the Data Register scan that reads the signature from octals $U_3$ and U.

preventing Test_CS from being generated when the Runtest/Idle state is reentered.

*Step 7* is a Data Register scan that reads the signature from octals $U_3$ and $U_4$. In adition, it sets up the memory read operation for the next block of memory.

The BIST-generated waveforms for the memory read operation are shown in Figure 6.

The designer can repeat these procedures to access other locations in the RAM array by changing the value of $U_1$'s boundary-scan register output signals, $BA_{08\text{-}13}$. Because $U_1$ operates in the Extest mode, software has to increment and scan out each of these addresses.

During Read cycles, the data bus, $BD_{00\text{-}15}$, becomes valid during the assertion of SRAM_CS (after the RAM access time). The bus is sampled by devices $U_3$ and $U_4$ on the rising edge of TCK, which is when SRAM_CS is being deasserted. The address bus changes value after the falling edge of TCK (after the propagation time, TCK-to-Q valid). The calculation of the minimum TCK period must consider the address setup time, RAM access time, and the octal data setup and hold times.

## Other Considerations

The 8-bit Scope octals offer two practical patterns for generating BIST addresses to a block of memory: 8-bit PRPG and Binary Count-up (for ABT parts only). The devices also supply four ways of writing data to a block of memory: 8-bit PRPG, 16-bit PRPG, Toggle, and Binary Count-up. The parts allow for reading BIST data from a block of memory by using 16-bit PSA data compression.

The use of 8-bit PRPG for address generation has a minor weakness in that it does not include address 00. Designers can ignore this shortcoming or do a separate boundary-scan procedure for address 00 in each memory block tested. The Binary Count-up algorithm accesses every address in the memory block.

One type of fault not fully covered by PRPG, or by one pass of any data pattern, is a single stuck bit in a memory cell. To guarantee detection of this fault, the test must write and read back a data pattern and its complement on two successive BIST executions. Only the Toggle algorithm can do this. The other data patterns require many more BIST operations.

Regardless of the address and data patterns used, all BIST memory blocks are read back using 16-bit PSA data compression. If the data patterns created a unique signature for each data byte within all the memory blocks, the tests should detect the general area and/or type of error. For example, if an error occurs in the same byte of every block, a data line probably has a short or an open. If all the bytes in a memory

**TABLE 7: PSEUDO-CODE FOR MEMORY READ OPERATIONS**

| Sequence and type | $BA_{08}$-$BA_{15}$ $U_1$ | $BA_{00}$-$BA_{07}$ $U_2$ | $BD_{08}$-$BD_{15}$ $U_3$ | $BD_{00}$-$BD_{07}$ $U_4$ | $\overline{\text{Memtest}}$ and BR/W $U_5$ |
|---|---|---|---|---|---|
| **Shut off the embedded microprocessor | | | | | |
| 1. IR | READBN | READBN | READBN | READBN | READBN |
| 2. DR | $BA_{15}=0$<br>$BA_{14}=1$<br>$BA_{08\text{-}13}=000000$ | LFSR seed | LFSR seed (set direction B → A) | LFSR seed | BR/W = 1<br>$\overline{\text{Memtest}}=0$ |
| 3. IR | Bypass | SCANCN | SCANCN | SCANCN | Bypass |
| 4. DR | Bypass<br>0 | PSA/PRPG<br>11 | PSA<br>10 | PSA<br>10 | Bypass<br>0 |
| 5. IR | Extest | Runt | Runt | Runt | Extest |
| **Hold in 1149.1 Run-Test/Idle state for 255 Test Clocks (TCKs) | | | | | |
| 6. IR | READBN | READBN | READBN | READBN | READBN |
| 7. DR | $BA_{15}=0$<br>$BA_{14}=1$<br>$BA_{08\text{-}13}=000001$ | | Read signature (and load next LFSR seed) | Read signature | BR/W = 1<br>$\overline{\text{Memtest}}=0$ |

## BOUNDARY-SCAN MEMORY TESTS

block are in error, an address line may have a problem. If only one byte in a block has a error, a memory cell may be bad, especially if complementary data does not cause an error.

Once the general area or type of error is known, the designer can write a simple program using TI's Asset boundary-scan development tools that will read and write to any selected address. Using various addresses and data patterns, this program can help determine the exact location of the problem.

For larger memory arrays, the Widebus interface parts can be used. These parts allow a larger block of data (up to 65,536 addresses) to be tested in one BIST execution. Also, one device can generate or read two data bytes. Although this capability increases test speed, it reduces resolution in locating a particular fault.

The techniques discussed in this article are for testing of static devices (RAM, ROM, EPROM, etc.). However, with some minor changes depending on the type of device being tested, similar methods can be used to test dynamic RAMs. The main consideration is the refresh cycle time required by the DRAM. One alternative is to make the BIST for each memory block short enough that a burst refresh before and after each BIST can keep the memory refreshed. Another technique is to design the address generator part of the BIST circuit so that it is tied to all the DRAM row-address lines. Then the DRAM will be refreshed automatically while the BIST is running.

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# *Design-for-Test Analysis of a Buffered SDRAM DIMM*

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## Abstract

*This paper presents a design-for-test (DFT) analysis of a buffered synchronous dynamic random-access memory (SDRAM) dual in-line memory module (DIMM). The analysis is restricted to board-level manufacturing faults. The test problem is described, alternate test methods are suggested, and a comparative study is presented contrasting a DFT approach – including boundary-scan test – versus a non-DFT approach.*



*Keywords: boundary scan, design-for-test, DFT, DIMM, DRAM, IEEE Std 1149.1, in-circuit, JTAG, memory, module, SDRAM, test.*


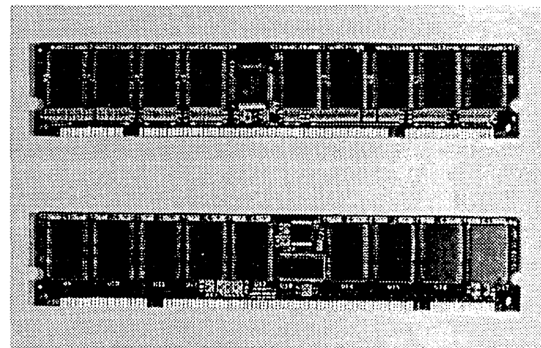

**Figure 1. Subject Module (1/2X)**

## 1. Introduction

The high quality of electronic systems being demanded by business and private consumers today is driving the growing importance that manufacturers are placing on testing as a whole. Ever-increasing miniaturization and complexity of very-large-scale integration (VLSI) integrated circuits (ICs) and systems are, in turn, leading to escalating difficulties faced by board/module manufacturers in using conventional test methods for their testing needs. The advent of new assembly technologies like fine-pitch surface-mount technology (SMT), multichip modules (MCMs), tape-automated bonding (TAB), and chip-on-board (COB) have complicated matters further.

Due to such advances, not only has it become difficult to gain physical access to probe printed-wiring-board (PWB) traces, but it has also become impractical to continue with conventional test development. With increased IC and module complexity, the high costs involved with developing test programs are recurring, as standard test programs that could be reused several times in the past, now need to be generated with a specific application in mind, due to the application-specific nature of ICs. Therefore, to maintain quality of products and increase competitive advantage while remaining economically viable, new and evolving system-level test methodologies aimed at improving overall testability must be adopted. This paper will demonstrate the applicability of such methods to a buffered SDRAM DIMM.

## 2. Module Construction

The analysis to be presented in this paper is based on a 200-pin, 2-bank x 2M x 72, buffered SDRAM DIMM designed at Texas Instruments (TI) according to JEDEC Standard 21-C. Figure 1 shows the subject module at half-size magnification. As shown, the module is a double-sided assembly that uses a high degree of miniaturization for both components and assembly.

The fundamental elements of the buffered SDRAM DIMM are a laminate substrate with dual-in-line edge contacts, a high-speed buffered register IC, a phase-locked-loop (PLL) clock distribution IC, several SDRAM ICs, as well as several capacitor and resistor components. Table 1 provides a summary of the module construction. As can be ascertained from this summary, all components, including passives as well as ICs, are of the fine-pitch surface-mount type.

**Table 1. Summary of Module Construction**

| PWB | | | | | | | |
|---|---|---|---|---|---|---|---|
| Finished size: 1.15 in. x 6.05 in. x 0.05 in; finished cost: $10 | | | | | | | |
| Substrate: glass-base epoxy resin, flame retardant (FR4) – 6 layers; edge: 200 pin, gold plate | | | | | | | |
| Wiring: copper/entek plus, size 4 mil, pitch 10 mil; vias: size 12 mil, pitch 50 mil | | | | | | | |
| ICs | DESCRIPTION | NO. | PART NO. | COST $ | | PACKAGE | LEAD PITCH |
| | | | | UNIT | EXT'ED | | |
| SDRAM | 2M × 8 | 18 | TMS626802 | 30.00 | 540.00 | 44-pin TSOP | 0.80 mm |
| Buffered register | 20 bit | 1 | ALVCH162721 | 5.00 | 5.00 | 56-pin TSSOP | 0.50 mm |
| Clock driver | 1-to-12 PLL | 1 | CDC2586 | 6.00 | 6.00 | 52-pin TQFP | 0.65 mm |
| PD buffer | 8 bit | 1 | LVC244 | 1.00 | 1.00 | 20-pin TSSOP | 0.65 mm |
| PASSIVES | | NO. | | COST $ | | PACKAGE | PITCH |
| | | | | UNIT | EXT'ED | | |
| Shunt/tie-off resistors (0, 10) | | 8, 72 | | 0.01 | 0.80 | 0603 | 50 mil |
| Bypass capacitors (0.001, 0.1) | | 24, 24 | | 0.03 | 1.44 | 0603 | 50 mil |

In the dual-bank architecture of the subject module, nine SDRAM ICs are placed on each side of the PWB. The clock driver and related passives are placed on one side of the board, while the register and buffer, along with associated passives, are placed on the other side of the board.

As noted in the construction summary, the PWB was constructed in six layers. The two outer layers were used for the data I/O and address/control buses. One inner layer was used for the clock signal routing, while another was used for routing register outputs to receiving SDRAMs on the back side. Finally, the remaining two layers were used for power (Vcc) and ground planes.

## 3. Module Function

The function of the subject SDRAM DIMM is shown in the block diagram of Figure 2. All address (12) and control (8) lines to the SDRAM devices are buffered and retimed through the 20-bit register. Data in/out signals are driven directly to/from the card edge via 10-ohm series damping resistors. External damping resistors are avoided on the address, clocks, and controls through the use of ICs that integrate such resistors. The single clock driver supplies buffered, phase-controlled clock signals to the register, as well as all SDRAM devices. The octal buffer sources the buffered presence-detect outputs, which provide configuration information about the DIMM. The output enable for this buffer is controlled by the presence-detect enable (PDE) signal.

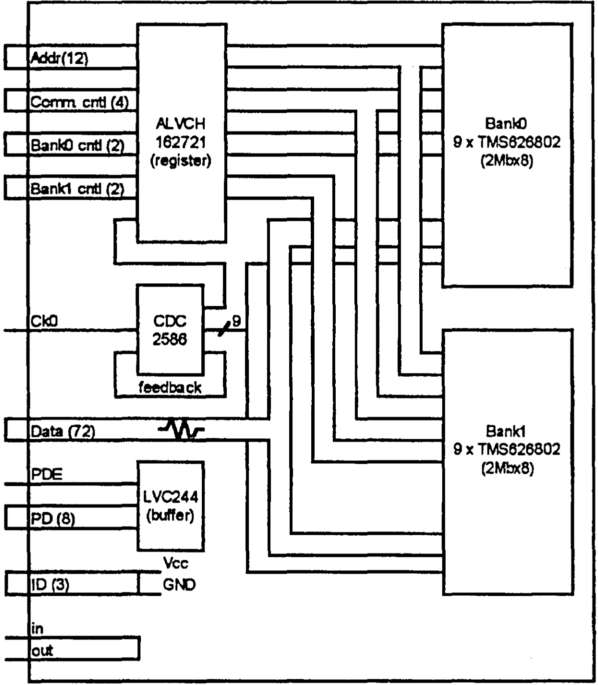


Figure 2. Module Block Diagram

## 4. Taxonomy of Defects

The causes for defects in a module can broadly be classified into process defects and random point defects. Process defects can result from high or abnormal variation in processing, such as in solder paste thickness, wiper pitch, etc., while point defects may result from particulate or other contamination.

Some defects that occur during the assembly process are commonly caused by manufacturing errors, such as the use of wrong components or missing components. Defects introduced during module assembly can also result from manufacturing processes, such as incorrect or insufficient paste, incorrect component placement, cold solder, solder splashes, contamination, or process damage. These may also be caused by use of defective or faulty components in the form of broken or improper leads, mislabeled parts or wrong values, or cracked components.

Regardless of their root cause, such defects can result in improper operation/function of the assembly. Therefore, testing is necessary to verify proper module function, to identify defects in faulty assemblies for rework and repair, as well as to eliminate sources of defects in the process.

A specific manifestation of a defect in an assembly is referred to as an assembly fault. These can be broadly grouped into gross and marginal classes. Marginal assembly faults are parametric in nature and deal with electrical characteristics of circuits like threshold, bias, and leakage currents and voltages. Delay faults can be classified as such. Gross assembly faults can be divided into interconnect faults, which include shorts and opens, and placement faults, which are caused by wrong component orientation or wrong part in socket.

**Table 2. Node/Solder-Joint Matrix With Card-Edge and In-Circuit Test Fault Classification**

| SIGNAL NODES | NO. | ASSOCIATED SOLDER JOINTS | NO. | DESCRIPTION | CLASSIFICATION OF SOLDER JOINT FAULTS | | | | | ICT ACCESSIBILITY |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | CARD-EDGE (NO DFT) | | | | ICT | |
| | | | | | ss/ L | ss/ H | so/ L† | so/ H† | so‡ | |
| Edge → Reg(addr) | 12 | Reg-I(addr) | 12 | Module Address Inputs | fA | fA | fA | fA | iB | a |
| Edge → Reg(cas) | 1 | Reg-I(cas) | 1 | Module Column-Address Strobe Input | fX | fX | fX | fX | iB | a |
| Edge → Reg(cke) | 2 | Reg-I(cke) | 2 | Module Clock Enable Inputs 1 per bank | fX' | fQ | fX' | fQ | iB | a |
| Edge → Reg(dqm) | 1 | Reg-I(dqm) | 1 | Module Data/ Output Mask Enable Input | fR | fX | fR | fX | iB | a |
| Edge → Reg(ras) | 1 | Reg-I(ras) | 1 | Module Row-Address Strobe Input | fX | fX | fX | fX | iB | a |
| Edge → Reg(s) | 2 | Reg-I(s) | 2 | Module Chip Select Inputs 1 per bank | fX' | fX' | fX' | fX' | iB | a |
| Edge → Reg(w) | 1 | Reg-I(w) | 1 | Module Write Enable Input | fX | fX | fX | fX | iB | a |
| Edge → CDC(clk) | 1 | CDC-I(clkin) | 1 | Module System Clock Input | fX | fX | fX | fX | iC | a |
| Edge → Buf(pde) | 1 | Buf-I(pde) | 2 | Module Presence Detect Enable Input | fS | fS | fS | fS | iS | a |
| Edge → Shunt(id) | 3 | Shunt-head(id) Shunt-tail(id) | 3 | Module Identification Output | fT | fT | fT | fT | iT | a x |
| Edge ↔ Shunt(in/out) | 2 | Shunt-head(in/out) Shunt-tail(in/out) | 1 | Module Physical Presence Detect Input/Output | fU | fU | fU | fU | iT | a |
| Edge ↔ SDRAM(dq): | 72 | Resistor-head | 72 | Module Data Input/Data Output | fV | fV | fV | fV | IV | a |
| Edge ↔ Resistor | 72 | Resistor-tail | 72 | All SDRAM I/Os are driven through 10-ohm resistors | fV | fV | fV | fV | iV | d |
| Resistor ↔ SDRAM(dq) | 72 | SDRAM-I/O(dq) | 144 | to/from card edge | fV | fV | fV | fV | iV | |
| Edge | 8 | Buf-O(pd) | 4 | Module Logical Presence | fW | fW | fW | fW | iB | a |
| | | | | Detect Outputs | fW' | fW' | fW' | fW' | | |
| Reg → SDRAM(addr) | 12 | Reg-O(addr) | 12 | SDRAM Address | fA | fA | fA | fA | iB | b |
| | | SDRAM-I(addr) | 216 | | | | fA' | fA' | iA' | |
| Reg → SDRAM(cas) | 1 | Reg-O(cas) | 1 | SDRAM Column-Address Strobe | fX | fX | fX | fX | iB | b |
| | | SDRAM-I(cas) | 18 | | | | fX''' | fX''' | iX''' | |
| Reg → SDRAM(cke) | 2 | Reg-O(cke) | 2 | SDRAM Clock Enable 1 per bank | fX' | fQ | fX' | fQ | iB | b |
| | | SDRAM-I(cke) | 18 | | | | fX''' | fQ' | iX''' | |
| Reg → SDRAM(dqm) | 1 | Reg-O(dqm) | 1 | SDRAM Data/Output Mask Enable | fR | fX | fR | fX | iB | b |
| | | SDRAM-I(dqm) | 18 | | | | fR' | fX''' | iX''' | |
| Reg → SDRAM(ras) | 1 | Reg-O(ras) | 1 | SDRAM Row-Address Strobe | fX | fX | fX | fX | iB | b |
| | | SDRAM-I(ras) | 18 | | | | fX''' | fX''' | iX''' | |
| Reg → SDRAM(s) | 2 | Reg-O(s) | 2 | SDRAM Chip Select 1 per bank | fX' | fX' | fX' | fX' | iB | b |
| | | SDRAM-I(s) | 18 | | | | fX''' | fX''' | iX''' | |
| Reg → SDRAM(w) | 1 | Reg-O(w) | 1 | SDRAM Write Enable | fX | fX | fX | fX | iB | b |
| | | SDRAM-I(w) | 18 | | | | fX''' | fX''' | iX''' | |

n/c = not considered; n/f = no fault

† noise injected onto open inputs may cause intermittent/unexpected results

‡ assuming 100% node coverage

**Table 2. Node/Solder-Joint Matrix With Card-Edge and In-Circuit Test Fault Classification (Continued)**

| SIGNAL NODES | NO. | ASSOCIATED SOLDER JOINTS | NO. | DESCRIPTION | CLASSIFICATION OF SOLDER JOINT FAULTS: CARD-EDGE (NO DFT) ss/ L | ss/ H | so/ L† | so/ H† | ICT so‡ | ICT ACCESSIBILITY |
|---|---|---|---|---|---|---|---|---|---|---|
| CDC → SDRAM(clk) | 9 | CDC-O(clk) | 9 | SDRAM System Clock | fX" | fX" | fX" | fX" | iC' | b/c |
| | | SDRAM-I(clk) | 18 | | | | fX"' | fX"' | iX"' | |
| CDC → Reg(clk) | 1 | CDC-O(clk) | 1 | Register System Clock | fX | fX | fX | fX | iC' | b |
| | | Reg-I(clk) | | | | | | | iD | |
| CDC → CDC(fb) | 1 | CDC-O(fb) | 1 | CDC External Feedback | fX | fX | fX | fX | iC' | b |
| | | CDC-I(fb) | | | | | | | iC | |
| Buf ← Shunt(pd-I) | 4 | Buf-I(pd) | 4 | Buffer Input (Presence Detect) Tie-offs | fW | fW | fW | fW | iB' | d |
| | | Shunt-head(pd) | | | | | | | iT | |
| | | Shunt-tail(pd) | | | | | | | iT | x |
| | | **OTHER SOLDER JOINTS** | | | | | | | | |
| | | Reg-I(clken) | 1 | Reg Clock Enable (to be low) | n/f | fX | n/f | fX | iD | x |
| | | Reg-I(NC) | 1 | Reg No-Connect (to be low) | n/f | n/f | n/f | n/f | n/f | x |
| | | Reg-I(oe) | 1 | Reg Output Enable (to be low) | n/f | fX | n/f | fX | iS | x |
| | | CDC-I(clr) | 1 | CDC Clear (to be low) | n/f | n/f | n/f† | n/f† | n/f† | x |
| | | CDC-I(NC) | 1 | CDC No-Connect (to be low) | n/f | n/f | n/f | n/f | n/f | x |
| | | CDC-I(oe) | 1 | CDC Output Enable (to be low) | n/f | fX | n/f | fX | iS | x |
| | | CDC-I(sel) | 2 | CDC Select (to be low) | n/f | fY | n/f | fY | iY | x |
| | | CDC-I(test) | 1 | CDC Test (to be low) | n/f | fZ | n/f | fZ | iZ | x |
| | | SDRAM-I(NC) | 90 | SDRAM No-Connect (to be low) | n/f | n/f | n/f | n/f | n/f | x |
| | | Buf-I(pd) | 4 | Buf Input (Presence Detect – to be low) | n/f | fW' | n/f | fW' | iB | x |
| | | Reg-Power | 12 | Register Vcc/GND | n/c | n/c | n/c | n/c | n/c | x |
| | | CDC-Power | 32 | CDC Vcc/GND | n/c | n/c | n/c | n/c | n/c | x |
| | | SDRAM-Power | 216 | SDRAM Vcc/GND | n/c | n/c | n/c | n/c | n/c | x |
| | | Buf-Power | 2 | Buffer Vcc/GND | n/c | n/c | n/c | n/c | n/c | x |
| | | Cap-head | 48 | Bypass Capacitors | n/c | n/c | n/c | n/c | n/c | x |
| | | Cap-tail | | | | | | | | |
| **TOTAL SIGNAL NODES** | 214 | **TOTAL SOLDER JOINTS** | 1175 | | | | | | | |

n/c = not considered; n/f = no fault
† noise injected onto open inputs may cause intermittent/unexpected results
‡ assuming 100% node coverage

Because of its construction, the module typically is subject to such manufacturing defects and consequent assembly faults. As the majority of defects in fine-pitch surface-mount assemblies, especially those associated with process rather than human error, directly affect solder joints, the analysis presented in this paper addresses that issue. Columns 1 to 5 of Table 2 enumerate the signal nodes, their associated solder joints, and other solder joints (those associated with Vcc/GND nodes) in the module.

## 5. Fault Models

For faults to be modeled or simulated – for coverage and diagnostic analysis among other purposes – they must be represented mathematically by abstraction through a logical model. Such logical models are called fault models. They constitute a basic set of assumptions that represent such faults. By such abstraction, the problem of modeling physical faults is reduced to a logical level that can represent the effects of physical faults on the behavior of the system. The process of fault analysis is also simplified by converting faults across several technologies into logical fault models that are independent of process.

A fault model used pervasively in many sorts of test and DFT analysis is the single-stuck-at model, in which a single defective node is presumed to behave as if it were constantly held to a static low or high level. For our analysis, this model will be extended to comprehend faults resulting from defects in solder joints.

Each solder joint can be faulty, either due to an open condition or a short condition. Thus, the single-stuck-at model is modified to cover both cases, resulting in the fault model detailed in Table 3.

**Table 3. Defined Solder-Joint Fault Model**

| NOTATION | FAULT NAME | DESCRIPTION |
|---|---|---|
| ss/L | Solder-short/low | Entire associated node stuck low |
| ss/H | Solder-short/high | Entire associated node stuck high |
| so/L | Solder-open/low | Pin is stuck low, independent of associated node |
| so/H | Solder-open/high | Pin is stuck high, independent of associated node |

## 6. Test Methodologies

Two categories of test are typically considered for manufacturing use:

1. Dynamic functional tests: tests defined in association with a functional and/or performance fault model. These test for faults, such as delay faults, that are associated with the performance of the system and are intended to demonstrate the suitability of the finished module to its intended function.
2. Static structural tests: tests defined in association with a structural fault model. These methods test for gross interconnectivity issues. In-circuit test (ICT) is an example of a static structural test method. The solder-open/short faults of Table 3 would be susceptible to such methods.

While the need for dynamic functional test is taken as a given, such analysis is beyond the scope of this paper. Such testing may in fact be required to detect certain classes of solder-open faults, such as those associated with bypass capacitors. However, the capability of such testing to diagnose or even detect structural defects is generally suspect. Therefore, the remaining analysis will focus exclusively on structural test goals.

## 7. Card-Edge Test (Module Without DFT)

As the subject module was designed solely for the purpose of demonstrating electrical performance characteristics of a buffered SDRAM DIMM, it was designed without any consideration for testability. Without such DFT, observability and controllability are limited to the primary (card edge) input/outputs (I/Os) of the module. This implies that for faults to be detected, such faults must be sensitized from the card-edge inputs and propagated through the entire module to the card-edge outputs. Diagnosis (isolation and location) of faults poses even greater difficulties, as many faults will produce the same syndrome at the primary I/Os.

The various fault syndromes resulting from modeled faults at each class of module solder joint are classified in columns 6–9 of Table 2 and defined in Table 4. The latter table also details the number of patterns and/or read/write cycles to be applied, along with a brief description of algorithms and consequent diagnostic resolution.

As shown in this analysis, many solder-joint faults produce common syndromes resulting in poor diagnostic resolution for structural faults when only card-edge access is provided.

**Table 4. Card-Edge Test Fault Classification**

| FAULT CLASS | DESCRIPTION | NUMBER PATTERNS FOR DETECTION/ISOLATION; (ALGORITHM) | DIAGNOSTIC RESOLUTION | |
|---|---|---|---|---|
| | | | NO. COMPONENTS | NO. SOLDER JOINTS |
| fA | All-chip addressing fault | 2 *((N+1)w + (N+1)r) = 26w + 26r; (write to all-0 addr and to all addr with only 1 logic-1 bit – read same; repeat for all-1 addr and all addr with only 1 logic-0 bit) | 19 | 20 |
| fA' | Single-chip addressing fault | " | 1 | 1 |
| fQ | Bank access-hold fault | 1wb + 1rb; (CKE low during read burst for access hold) | 10 | 11 |
| fQ' | Single-chip access-hold fault | " | 1 | 1 |
| fR | All-chip access-mask fault | 1wb + 1rb; (DQM high during read/write burst for data mask) | 19 | 20 |
| fR' | Single-chip access-mask fault | " | 1 | 1 |
| fS | Presence detect enable/disable fault | 2; (PDE low/high) | 1 | 1 |
| fT | Identification output fault | 1; (static output) | 1 | 2 |
| fU | IN/OUT fault | 4; (IN low/high, OUT low/high) | 1 | 2 |
| fV | Dual-chip data fault | 2 * 2*72(1w + 1r) = 288w + 288r; (walking-1 each bank, walking-0 each bank) | 3 | 4 |
| fV' | Single-chip data fault | " | 1 | 1 |
| fW | Presence detect output fault(1) | 1; (static output) | 2 | 4 |
| fW' | Presence detect output fault(2) | 1; (static output) | 1 | 1 |
| fX | All-chip gross access fault | 1w + 1r; (any valid write /read access with any addr/data) | 20 | 69 |
| fX' | Bank gross access fault | " | 10 | 22 |
| fX" | Dual-chip gross access fault | " | 2 | 3 |
| fX"' | Single-chip gross access fault | " | 1 | 7 |
| fY | Clock multiply fault | 2*(1wb + 1rb); (1 wb/rb to bank0, 1 wb/rb to bank1) | 1 | 1 |
| fZ | Clock PLL-bypass fault | 1w + 1r; (at freq. which will not result in phase-lock) | 1 | 1 |

## 8. Module DFT

Design-for-test techniques are generally based on providing greater access to the module under test for the purpose of improving the degree to which the module function can be observed and controlled. Another way of looking at DFT is that it seeks to partition the larger module function into smaller functions that are easier to test. Several techniques for this are in common use today. The two that are considered in this paper are in-circuit test (ICT) and boundary scan.

## 9. In-Circuit Test

ICT is based on providing physical access to probe as many module nodes as possible and on *ad-hoc* circuit techniques that allow internal nodes to be safely controlled (as well as observed) by an external tester. The resulting test fixture is commonly called a “bed of nails” (or in the case of double-sided assembly such as the subject module, a “clam shell”) and the required tester consists of a large number of high-drive parallel test channels.

Generally, on fine-pitch SMT assemblies such as the subject module, provision for ICT requires placement of “test points” on which ICT probes may land. In some cases, the vias that are anyway present to route signals from outer layers to other layers may provide such test points. In other cases, vias must be added to bring signals to be accessed up from inner layer to outer layer.

Such placement of test points requires use of module "real estate" that may not be available. Generally, the finest available ICT probes (50-mil pitch) require test pads of 25 mils minimum width.

While modifications to the module layout have not been specifically implemented, the module layout has been analyzed for placement of physical test points. The results by node are presented in column 11 of Table 2 according to the accessibility classes defined in Table 5.

**Table 5. In-Circuit Test Accessibility Classification**

| ACCESSIBILITY CLASS | DESCRIPTION |
|---|---|
| a | Accessible from module edge |
| b | Test points easily provided |
| c | Test points provided with difficulty |
| d | Test points difficult/impossible to provide |
| x | Accessible from module edge (Vcc/GND) |

With test points provided at all internal nodes, the module is quite controllable at the IC level. Since all ICs on the module provide means for placing their outputs at high impedance, the tester can safely disable any ICs that are not under test. The only provision that would be required for this is to add pull-down resistors at register and clock driver output-enable pins versus the direct tie to GND that is specified for the original module.

Based on the presumed insertion of test points at all internal nodes except those in accessibility class d (quantity 31), full coverage and diagnostic of solder shorts are provided. The nodes excluded are indirectly accessible via shunt or resistor, and so their exclusion may somewhat reduce fault diagnostic, but not coverage. In case of solder opens, the consequent fault syndromes resulting at each class of module solder joint are classified in column 10 of Table 2 and are defined in Table 6. The latter table also indicates the consequent diagnostic resolution.

**Table 6. In-Circuit Test Fault Classification**

| FAULT CLASS | DESCRIPTION | DIAGNOSTIC RESOLUTION | |
|---|---|---|---|
| | | NO. COMPONENTS | NO. SOLDER JOINTS |
| iA' | Single-Chip Addressing Fault | 1 | 1 |
| iB | Buffer Data Fault | 1 | 2 |
| iB' | Buffer Data Fault (no access) | 2 | 3 |
| iC | Gross Clock Output Fault | 1 | 2 |
| iC' | Single Clock Output Fault | 1 | 1 |
| iD | Register Clock Fault | 1 | 2 |
| iS | Output Enable Fault | 1 | 1 |
| iT | Shunt/Resistor Fault | 1 | 2 |
| iV | Memory Data Fault | 2 | 3 |
| iX''' | Single-Chip Gross Access Fault | 1 | 7 |
| iY | Clock Multiply Fault | 1 | 1 |
| iZ | Clock PLL-Bypass Fault | 1 | 1 |

As shown, the diagnostic resolution is remarkably improved (versus card-edge test), such that all single solder-stuck faults are generally diagnosable to the component and often to the pin level. Such a diagnostic provides the information necessary to improve process and repair failed boards for subsequent shipment.

## 10. Boundary-Scan Test

Like ICT, boundary-scan test (BST), as standardized in IEEE Std 1149.1 (JTAG), is based on providing test access to as many module internal nodes as possible. Unlike ICT, boundary scan provides access by integrating digital test cells behind the pins of compliant ICs. Access to such boundary-scan cells for control and observation of the module is provided by a 4-wire test access port (TAP) at each compliant IC. Thus, the complex and expensive fixturing and automated test equipment (ATE) required for ICT is avoided.

### 10.1 Boundary Scan at Register and Clock Driver

Of the 31 internal nodes that are presumed to be ICT accessible, 21 are associated with the register (ALVCH162721) while 10 are associated with the clock driver (CDC2586). Therefore, if the register and clock driver were replaced with suitably equivalent ICs with boundary scan, all ICT-covered nodes would be boundary-scan accessible, and thus, ICT could be eliminated without any consequent loss of fault coverage or diagnostic.

Such equivalents or near equivalents to the ALVCH162721 are, or will be, available soon (such as LVTH182504A and/or ALVCH182504, at an estimated additional cost of $5). Unfortunately, the authors are unaware of any clock drivers available or planned with boundary scan. If these were available (at an estimated additional cost of $3), then boundary scan would displace ICT, while requiring off-edge physical access only to the four TAP signals and using much less expensive ATE – all at an additional component cost that is barely 1% of the total cost of module materials.

### 10.2 Boundary Scan at Register Only

Even with boundary scan available only in the register, controllability and observability of the SDRAM ICs is provided, with the exception of the clock signals. Observability of one output of the clock driver is also provided. Therefore, if access to the TEST input of the CDC2586 were provided, the low-cost boundary-scan tester could source the module CLKIN signal so that it would be coordinated with boundary-scan operations to perform read/write cycles to the SDRAM array. By doing so, all interconnects to the SDRAMs can be tested with the same fault coverage and diagnostic capability provided by ICT. Access to only five off-edge signals is required (four TAP signals, plus the CDC2586 TEST input).

### 10.3 Boundary Scan at SDRAM ICs

Boundary scan in the SDRAMs would greatly impact the overall controllability/observability of the module such that diagnostic resolution would be improved over that provided by ICT. For example, where faults of class iX" (single-chip gross access fault) occur in ICT, the boundary-scan facility on the SDRAM would be able to distinguish which of seven pins on the device were open.

At this time, the authors are unaware of any available or planned offerings of SDRAMs with boundary scan. However, due to the large ratio of die size to I/O pins of such ICs, it is estimated that the silicon overhead for providing boundary-scan should be less than 5%. It is hoped that memory IC vendors will realize the benefit of scan-test techniques, not only for board/manufacturing test, but also to access built-in test capabilities of such ICs.

### 10.4 Boundary Scan at Buffer

As it has a very simple function on the module (drive static outputs), the octal buffer is the last device to warrant consideration for boundary scan. Still, the additional cost (estimated at $2) required to procure equivalent buffers with boundary scan would be minimal.

### 10.5 Boundary Scan: Beyond Manufacturing Test

A real advantage that boundary scan holds over any other manufacturing test or DFT approach is that it is built into the ICs and, thus, the module, and so is available for use when ATE is not. For example, it can be used for module test during burn-in or under other conditions where the module is not accessible by ATE. Additionally, if appropriate system-level access to boundary scan is provided, it can be used for in-system test, diagnostics, configuration, programming, emulation, etc.

## 11. Comparative Study

Several metrics have been used to grade the different structural test methodologies outlined. A tabulation of the performance of the various test methodologies versus these metrics is given in Table 7.

**Table 7. Comparison of Test Methodologies**

| METRIC | CARD-EDGE | ICT | BST |
|---|---|---|---|
| Fault coverage | 95%+ | 95%+ | 95%+ |
| Fault diagnostic | 4 sol. joints | 2 sol. joints | 2 sol. joints |
| Vector development | 100 per-hr | 30 per-hr | 15 per-hr |
| Test pattern size | 1 Mb | 100 kb | 20 kb |
| Test time | 0.1 s | 0.1 s | 0.1 s |
| Tester cost | $200k | $400k | $40k |

Fault coverage is the estimated percentage of faults that will be detected. Since the subject module is fairly simple structurally, it is expected that all test methods will obtain a high level of coverage.

Fault-diagnostic capability is expressed as a weighted average of resolution in terms of solder joints. Excellent results from ICT and BST are typical, while the result for card-edge test belies the simple function of this module.

Vector development effort is measured in terms of the estimated number of person-hours required to complete the test set. Boundary-scan test development is highly automated, while ICT is somewhat less so. On the other hand, card-edge test development tends to be manual.

Test-pattern size is expressed in bits. With full BST, the vector set is on the order of $\log_2$ (number of module nodes). ICT vector sets will be somewhat longer, while card-edge vector sets can be very lengthy, in order to obtain desired fault coverage and diagnostic resolution.

Test time is a factor of the number of vectors and the vector application time. BST uses a low vector bit rate, but due to the small number of vectors, performs quite adequately. ICT and card-edge testers can use much higher vector bit rates.

Tester cost is estimated and is a function of performance (vector bit rate), number of test channels, etc. The small number of channels required for BST and modest performance requirements result in very inexpensive test systems.

## 12. Conclusion

Considering the metrics and discussion provided in the prior section, boundary-scan test is clearly a winning manufacturing test strategy, even for a module of modest functional complexity. Add to this the ability to reuse boundary scan during burn-in, and more importantly in fielded systems, and a small investment in additional component cost for boundary scan will reap dividends many times over throughout the product's life cycle.

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# A Proposed Method of Accessing 1149.1 in a Backplane Environment

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# A Proposed Method of Accessing 1149.1 in a Backplane Environment

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**Abstract**

This paper presents a novel circuit and protocol that can be used in system backplanes to provide a connection method between backplane and board level IEEE 1149.1 serial buses. While the basic objective of this approach is to provide a simple 1149.1 backplane to board connection method, it can be expanded to include other features, some of which are similar to those being developed in the IEEE P1149.5 and P1394 backplane serial bus standards.

## 1.0 Introduction

The concept of a simple, cost-effective serial bus protocol providing linkage between 1149.1 board and backplane environments has been developed. This serial bus protocol operates on the backplane, using the signal wires defined in 1149.1, to address and select one of the boards in a backplane. Once selected, the board can be communicated to using the standard 1149.1 bus protocol. In general, the technique described in this paper can be applied to any type of bus. However, in this paper it is described as a feature added to the IEEE/ANSI 1149.1 standard serial bus designed for boundary scan testing of ICs at the board level [1]. The author assumes the reader has a basic understanding of the 1149.1 standard.

The approach described in this paper is based on a unique protocol. This protocol can be embedded in existing serial bus protocols and invoked, during times when the buses are in an idle or non-operational state, to address and select a slave device for access by a serial bus master. After the protocol has been used to connect a serial bus slave up to a serial bus master, it relinquishes control of the bus, and allows the bus to revert back to its normal mode of operation. One of the advantages of this approach is that it does not require modifying the protocol of the serial bus it is used with. Therefore, upgrading a preferred or existing serial bus to include the connection method provided by the protocol can be less costly and time consuming than a complete redesign approach.

The term "serial bus slave" used in this paper represents any logic module capable of being interfaced to and controlled by a serial bus master. While this papers describes serial bus slaves as being boards in a backplane, they could also be: sub-circuits in an IC, ICs on a multi-chip module, ICs on a board, backplanes in a subsystem, or subsystems in a system. The term "serial bus master" used in this paper represents any logic module capable of interfacing to and controlling a serial bus slave. While this paper will illustrate the serial bus master as existing on the backplane wiring, it actually exists either in a backplane board or as an external tester connected to the backplane.

## 2.0 Background

As the use of 1149.1 continues to grow, more interest is being focused on how to access 1149.1 board designs in a backplane environment. Several methods of accessing 1149.1 boards in a backplane environment have been proposed. The following is a brief description of each of these methods.

### 2.1 Using 1149.1 at the Backplane Level

The 1149.1 standard describes a 4-wire serial bus that can be used to transmit serial data between a serial bus master and slave device. The 1149.1 bus consists of a test mode select (TMS) signal, a test clock (TCK) signal, a test data output (TDO) signal, and a test data input (TDI) signal. The TMS and TCK signals are output from the master and input to the slave. The TDO output from the master is input to the TDI input of the slave, and the TDO output from the slave is input to the TDI input of the master. During serial access, the master outputs control on TMS and clock on TCK to allow serial data to be transferred between the master and slave, via the TDO and TDI bus connections.

While 1149.1 was developed to serially access ICs on a board, it can be used at the backplane level to serially access boards. 1149.1 has two serial access configurations, referred to as "ring" and "star", that can be used at the backplane level. The following describes both configurations and identifies problems with each when used at the backplane level.

#### 2.1.1 1149.1 Backplane Ring Configuration

In a backplane 1149.1 ring configuration, all boards directly receive the TCK and TMS control outputs from a primary serial bus master (PSBM) and are daisy chained between the PSBM's TDO output and TDI input. During scan operation, the PSBM outputs control on TMS and TCK to scan data through all boards in the backplane, via its TDO and TDI bus connections. The problem associated with the ring configuration, is that the scan operation only works if all the boards are included in the backplane and are operable to scan data from their TDI input to TDO output. If one of the boards is removed or has a fault, the PSBM will be unable to

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scan data through the backplane. Since the ring configuration does not allow access to remaining boards when one is removed or disabled, it does not fully meet the needs of a backplane serial bus.

### 2.1.2 1149.1 Backplane Star Configuration

In a backplane 1149.1 star configuration, all boards directly receive the TCK and TDI signals from the PSBM and output a TDO signal to the PSBM. Also each board receives a unique TMS signal from the PSBM. In the star configuration only one board is enabled at a time to be serially accessed by the PSBM. When a board is enabled, the TMS signal associated with that board will be active while all other TMS signals are inactive. The problem with the star configuration is that each board requires its own TMS signal. In a backplane with 50 boards, the PSBM would have to have 50 individually controllable TMS signals, and the backplane would have to have traces for each of the 50 TMS signals. Due to these requirements, star configurations are typically not considered for backplane applications.

### 2.2 Interfacing 1149.1 to other IEEE Buses

Two IEEE serial bus standards, P1149.5 and P1394, are in development for use in system backplanes. Since these standards are being specifically designed for backplane applications, they overcome the problems stated using 1149.1 as a backplane bus. However, the protocols of these anticipated standards are different from the 1149.1 protocol and therefore methods must be defined to translate between them and 1149.1. The following sections describe each backplane bus and identify problems with each when used to interface into 1149.1 board environments.

### 2.2.1 Interfacing P1149.5 to 1149.1

The P1149.5 standard working group is defining a module test and maintenance bus that can be used in system backplane environments [2,3]. P1149.5 is a single master/multiple slave bus defined by a 5-wire interface. Two of the wires are used for transferring serial data between the bus master and slave devices, one wire is used as a clock, one wire is used to control the operation of the bus, and one wire is used as a pause request from a slave to the master. The P1149.5 bus master initiates a data transfer operation by transmitting a data packet to all slave devices. The data packet consists of an address and command section. The slave device with a matching address is enabled to respond to the command section of the data packet as described in the P1149.5 standard proposal.

While the P1149.5 is a good data transfer type backplane bus for high-end commercial and military systems, its capabilities may exceed the requirements of some middle and low-end commercial systems that don't require or support its command set. Interfacing P1149.5 into an 1149.1 environment can be done but the system hardware and software designers must have an understanding of both bus types. One of the problems, therefore, in using P1149.5 to only interface into an 1149.1 environment, is that it adds an unnecessary complication to an otherwise simple serial access approach. Another problem is that the bandwidth of the 1149.1 serial data transfer may be adversely affected by the P1149.5 to 1149.1 protocol conversion process.

### 2.2.2 Interfacing P1394 to 1149.1

The P1394 standard working group is defining a 2-wire high-speed serial bus that can be used in either a cable or system backplane environment [4]. The P1394 standard, unlike P1149.5, is not a single master/multiple slave type bus. In P1394, all devices (nodes) connected to the bus are considered to be of equal mastership. Control of the bus is achieved by one node winning an arbitration contest with the other nodes in the network. Once a node wins control of the bus, it can transfer data to or from any other node in the network. The fact that P1394 can operate on a 2-wire interface makes this bus attractive in newer 32-bit backplane standards where only two wires are reserved for serial communication [5,6,7,8]. However, there are problems in using P1394 as a backplane test bus to access 1149.1 board environments.

The first problem is that P1394 is significantly more complex in operation than 1149.1, thus devices designed to translate between P1394 and 1149.1 may be costly. The second problem is that P1394 is not a full time test bus, but rather it is a general purpose serial communication bus. Its primary purpose in a backplane environment is to act as a backup interface in the event the parallel interface between boards becomes disabled. While 1149.1 test access can be achieved via P1394, it will be available only during time slices when the bus is not handling functional operations. Thus on-line 1149.1 test access will be limited and must be coordinated with other transactions occurring on the P1394 bus.

### 2.3 Extending 1149.1 for Backplane Usage

Another method of achieving a backplane to board level interface is to extend the protocol defined in the 1149.1 standard. Such an approach has been described in a paper presented at the 1991 International Test Conference by D. Bhavsar [9]. While the approach described in the paper has the same basic goal in mind as the one presented in this paper, they are fundamentally different in the method used to achieve the goal.

The Bhavsar paper describes a method of extending the protocol of 1149.1 to where it can be used to access an interface circuit residing between the backplane and board level 1149.1 buses. The interface circuit responds to 1149.1 protocol transmitted over the backplane bus to load an

address. If the address matches the address of the interface circuit, the interface circuit is connected to the backplane. After the interface circuit is connected to the backplane, additional 1149.1 protocol is input to the interface circuit to connect the backplane and board level 1149.1 buses. Following this connection procedure, the board level 1149.1 bus can be controlled by the backplane 1149.1 bus. While Bhavsar's approach is an interesting one, it has one problem that limits its effectiveness as a general purpose 1149.1 backplane to board interfacing method.

The problem is that the approach does not allow for selecting one board, then selecting another board without first resetting the backplane and board level 1149.1 buses, by transitioning them into their test logic reset (TLRST) state. Entering the TLRST state causes test conditions setup in the ICs of a previously selected board to be lost due to the test reset action of the 1149.1 bus on the test access ports (TAPs) of the ICs.

For example, if the interconnects between two boards are to be tested, it is necessary to select and setup one of the boards to output a test pattern, then select the other board to receive the test pattern. With the described approach, the only way to select the second board, after the first board has been selected and setup, is to place the backplane serial bus in its TLRST state. The action of placing the backplane 1149.1 bus in it TLRST state clears out the test pattern setup in the first selected board, so the second selected board cannot receive the intended test pattern.

In another example, it may be desirable to select and initiate self-tests in a selected group of backplane boards. However, since the approach requires resetting the 1149.1 bus each time a new board is selected, it is impossible to self-test more than one board at a time, because resetting the bus aborts any previously initiated self-test.

### 3.0 A New Backplane Access Approach

The backplane access approach described in this paper provides a method of using the 1149.1 bus at the backplane level without incurring the problems previously described. Using this approach, it is envisioned that one homogeneous serial bus may be used throughout a system design, rather than translating between multiple serial bus types. Employing a common serial bus in system designs can simplify software and hardware engineering efforts, since only an understanding of one bus type is required.

A circuit, called an addressable shadow port (ASP), and a protocol, called a shadow protocol, have been defined to provide a simple method of directly connecting 1149.1 backplane and board buses together. When the 1149.1 backplane bus is in either its run test/idle (RT/IDLE) or TLRST state, the ASP can be enabled, via the shadow protocol, to connect a target board's 1149.1 bus up to the backplane 1149.1 bus. After the shadow protocol has been used to connect the target board and backplane buses together, it is disabled and becomes transparent to the operation of the 1149.1 bus protocol.

A board example using the ASP is shown in Figure 1. The board consists of multiple ICs and an ASP. The ICs operate, when connected to the 1149.1 backplane bus, via the ASP, as described in the 1149.1 standard. The ASP has a primary port for connection to the backplane 1149.1 bus, a secondary port for connection to the board 1149.1 bus, and an address input. The primary port signals are labeled; PTDI, PTDO, PTCK, and PTMS. The secondary port signals are labeled; STDI, STDO, STCK, and STMS. The address input to the ASP is a binary value used to identify the board on which the ASP mounted.

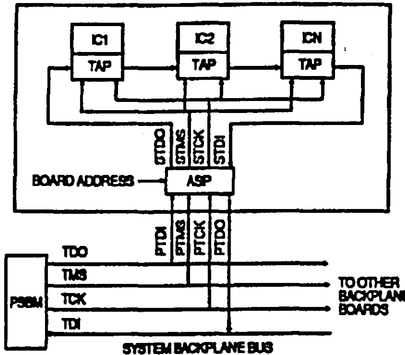



FIGURE 1 Board Using ASP Circuit

In Figure 2, multiple boards, similar the one in Figure 1, are shown interfaced to a PSBM via ASPs. When one of the boards needs to be accessed, the PSBM transmits a selection shadow protocol, called a select protocol, to address and enable the ASP of the selected board. The PSBM transmits the select protocol while the backplane 1149.1 bus is in either the RT/IDLE or TLRST state. The select protocol contains an address that is used to match against the address input to the ASP. All ASPs receive the select protocol, but only the one with the matching address is selected.

In response to the select protocol, the selected ASP transmits an acknowledgement shadow protocol, called an acknowledge protocol, to the PSBM to verify reception of the select protocol. The acknowledge protocol contains the address of the selected ASP to allow the PSBM to verify the correct ASP was selected. After transmitting the acknowledge protocol, the selected ASP makes a connection between its primary and secondary ports.

In response to the acknowledge protocol, the PSBM communicates to the selected board using the 1149.1 bus protocol. If the PSBM does not receive an acknowledge protocol, it assumes the board has been removed or is disabled and will not attempt to communicate to it using the 1149.1 protocol.

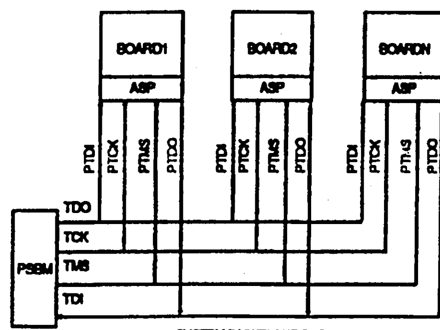



FIGURE 2 Backplane ASP Connections

After the PSBM completes its 1149.1 access of the currently selected board, it can output a new select protocol to select another board's ASP. In response to the new select protocol, the newly selected ASP transmits an acknowledge protocol back to the PSBM, then connects its primary and secondary ports. Also in response to the new select protocol, the previously selected ASP breaks the connection between its primary and secondary ports. The disconnecting ASP remains in the state the backplane 1149.1 bus was in when the disconnect occurs, i.e. the 1149.1 RT/IDLE or TLRST state. The ability to disconnect and leave a board level 1149.1 bus in the RT/IDLE state is very important since it allows leaving a board in a test mode while other boards are being selected and accessed.

A key objective in developing this backplane access approach was designing the select and acknowledge protocols so that they could be transmitted, via the 4-wire 1149.1 bus, without infringing upon the 1149.1 bus protocol. This objective was met by specifying that the select and acknowledge protocols could not use the 1149.1 TMS signal, and that the protocols could only be transmitted while the 1149.1 bus is idle in its RT/IDLE state or reset in its TLRST state.

In the RT/IDLE and TLRST states, TDO and TDI are disabled and pulled high (via pull-ups on TDI), TCK free runs, and TMS is held at either a logic zero or one state. While the 1149.1 bus is in one of these two states, the PSBM can output the select protocol from the PSBM's TDO output to the PTDI inputs of the ASPs, and receive the acknowledge protocol from the selected ASP's PTDO output on the PSBM's TDI input. Since the 1149.1 bus is inactive, the transmission of the select and acknowledge protocols is transparent to the 1149.1 bus, and does not infringe upon its protocol.

### 3.1 Design of Select/Acknowledge Protocols

To transmit the select and acknowledge protocols without using the TMS control signal, a bit-pair signaling method was designed to allow control and data to be transmitted together on a single wiring channel. During select protocols, the bit-pair signaling method allows the PSBM to transmit control and data from its TDO output to the ASP's PTDI input. During acknowledge protocols, the bit-pair signaling method allows the selected ASP to transmit control and data from its PTDO output to the PSBM's TDI input. Both protocols include control to indicate: an idle condition, a start data transfer condition, and a stop data transfer condition. In addition, both protocols include a method of transmitting data during the interval between the start and stop data transfer conditions.

The bit-pair signals are output from the transmitting device (PSBM or ASP) on the falling edge of the TCK and input to the receiving device (PSBM or ASP) on the rising edge of the TCK. Since this timing is consistent with 1149.1 timing, upgrading a PSBM to support this approach is simply a matter of forcing the TMS output to hold its present state ("0" for RT/IDLE and "1" for TLRST) while using normal 1149.1 scan operations to transmit and receive the select and acknowledge protocols. The simplicity of this approach makes it an attractive addition to the 1149.1 test bus. The bit-pair signals used in the select and acknowledge protocols are defined in the following list.

<u>Idle Bit-Pair</u> – *an encoded control signal (I) identified by the transfer of two successive logic one bits from a transmitter to a receiver.*

<u>Select Bit-Pair</u> – *an encoded control signal (S) identified by the transfer of two successive logic zero bits from a transmitter to a receiver.*

<u>Logic 1 Bit-Pair</u> – *an encoded logic one signal (D) identified by the transfer of a logic zero bit followed by a logic one bit from a transmitter to a receiver.*

<u>Logic 0 Bit-Pair</u> – *an encoded logic zero signal (D) identified by the transfer of a logic one bit followed by a logic zero bit from a transmitter to a receiver.*

### 3.2 Framing of Select/Acknowledge Protocols

A diagram of the select and acknowledge protocols being transmitted while the 1149.1 bus is in its RT/IDLE state is shown in Figure 3. The T signals shown in the protocol sequence indicate when the TDO to PTDI and PTDO to TDI wiring channels are tristate and pulled high. The first sequence framed between the first and second I signals is the select protocol output from the PSBM to the ASP (TDO to PTDI). The second sequence framed between the first and second I signals is the acknowledge protocol output from the selected ASP to the PSBM

(PTDO to TDI). The select protocol always precedes the acknowledge protocol as shown in the diagram.

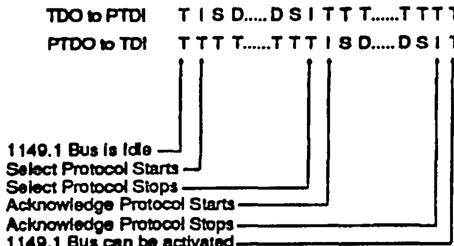



FIGURE 3 Select and Acknowledge Protocols

The I signal at the beginning of each protocol is designed to be indistinguishable from the preceding T signals. This avoids unintentional entry into a select or acknowledge protocol when the 1149.1 bus enters the RT/IDLE state after a scan operation. However, the I signal at the end of each protocol is designed to be distinguishable from the preceding S and D signals so that it can be used to terminate the protocol. Inside each protocol, first and second S signals are used to frame the address which is defined by a series of D signals. The logic zero and one D signals are distinguishable so that the binary address can be recovered.

### 3.3 ASP Circuit Description

A circuit example of the ASP is shown in Figure 4. The ASP consists of a receiver circuit (RCR), a transmitter circuit (XMT), a slave control circuit, multiplexers (MX1 and MX2), a power up reset circuit (PRST), and a reset address (RSTA). The primary port signals (PTDI, PTMS, PTCK, PTDO) connect to the backplane level 1149.1 bus. The secondary port signals (STDO, STMS, STCK, STDI) connect to the board level 1149.1 bus. The address input bus receives the board address.

#### 3.3.1 ASP Receiver Circuit

The receiver circuit consists of a controller and a serial input/parallel output (SIPO) register. The PTDI signal from the PSBM is input to the receiver's SIPO register to supply the serial address during select protocols, and input to the receiver's controller to regulate the receiver during select protocols. The parallel address output from the SIPO is input to the slave control circuit via the address input (AI) bus. The status output from the receiver is input to the slave controller circuit to indicate when a select protocol has started, when the address is ready to read, and when the select protocol has completed. The control bus input to the receiver from the slave control circuit enables the receiver to respond to a select protocol input. The receiver is only enabled when the backplane 1149.1 bus is in the RT/IDLE or TLRST state.

The receiver's controller determines when a first "I-S-D" signal sequence occurs on PTDI, indicating the start of a select protocol and address input. In response to this input sequence, the controller enables the SIPO to receive the serial address input on PTDI. The controller determines when a first "D-S-I" signal sequence occurs on PTDI, indicating the end of the address input and select protocol. In response to this input sequence, the controller signals the slave control circuit, via the status bus, to read the address, then terminates the select protocol input operation.

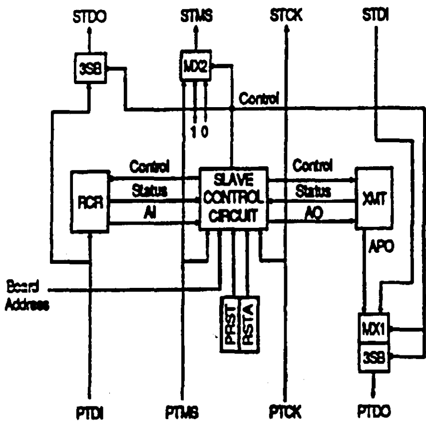



FIGURE 4 ASP Circuit Example

#### 3.3.2 ASP Transmitter Circuit

The transmitter circuit consists of a controller and a parallel input/serial output (PISO) register. The transmitter's PISO register receives parallel data from the slave control circuit via the address output (AO) bus, and outputs the address serially to the PTDO output via the acknowledge protocol output (APO) signal and MX1. The transmitter's controller receives control input from the slave control circuit via the control bus, and outputs status to the slave control circuit via the status bus. The control input regulates the parallel to serial conversion process that takes place during the acknowledge protocol. The control input only enables the transmitter to output an acknowledge protocol when the backplane 1149.1 bus is in the RT/IDLE or TLRST state. The status output informs the slave control circuit of the transmitters status, i.e. whether the acknowledge protocol is in progress or complete.

At the beginning of an acknowledge protocol, the slave control circuit enables MX1 and the 3-state buffer (3SB) to pass the APO signal from the transmitter to the PTDO output. The slave control

circuit then inputs the board address to the transmitter via the AO bus. In response to the address input, the transmitter outputs an I and S signal on PTDO to start the acknowledge protocol, then transmits the address on PTDO. After the address is shifted out, the transmitter circuit outputs an S and I signal sequence to stop the acknowledge protocol.

### 3.3.3 ASP Slave Control Circuit

The slave control circuit regulates the operation of the transmitter, receiver, and multiplexers during select and acknowledge protocols. The slave control circuit is clocked by the PTCK input from the primary port. The PTMS input from the primary port indicates to the slave control circuit when the 1149.1 bus is busy, idle or reset. While the backplane bus is idle (RT/IDLE) or reset (TLRST), the slave control circuit enables the transmitter and receiver circuits. The status buses from the receiver and transmitter circuits are used to input status to the slave control circuit. The AI bus from the receiver inputs the address received during select protocols. The AO bus from the slave control circuit outputs the board address to the transmitter during acknowledge protocols. The address input from the reset address (RSTA) allows resetting the ASP in response to a reset address input during a select protocol. The input from the power up reset circuit (PRST) allows resetting the ASP at power up.

During select protocols, the slave control circuit receives parallel address input from the receiver via the AI bus. The slave control circuit compares the received address against the board address. If the addresses match, the ASP responds by outputting an acknowledge protocol.

During the acknowledge protocol, the slave control circuit outputs control to the transmitter to load the board address and initiate the acknowledge protocol. After the acknowledge protocol has been transmitted, the slave control circuit outputs control to connect the primary and secondary ports.

## 3.4 Resetting the ASP

When power is first applied to the ASP, the slave control circuit is reset by input from the power-up reset circuit (PRST). When reset, the transmitter and receiver circuits are initialized and the primary and secondary ports are disconnected by disabling the STDO and PTDO outputs and setting the STMS output high. The STCK output always outputs the PTCK input. If desired, a reset input could be used to reset the ASP as well.

The ASP can also be reset by inputting a select protocol with an address that matches the reset address (RSTA) inside the ASP. If the address input matches the reset address, the ASP is reset to the same state as described in the power-up reset. The reset address is the same for all ASPs so that a global reset of all ASPs can be achieved by the transmission of a single select protocol containing the reset address. The reset address is unique from the board addresses. A preferred value for the reset address is zero, since board addressing will usually start with an address of one. An acknowledge protocol is not transmitted after a reset address has been received, to avoid contention on the PTDO outputs of multiple ASPs.

## 3.5 Disconnecting a Selected ASP

When 1149.1 access to another board is required, a new select protocol is issued from the PSBM. When the previously selected ASP receives the new select protocol its primary and secondary ports are disconnected. If the new select protocol was issued while the backplane 1149.1 bus was in its RT/IDLE state (PTMS=0), MX2 of the disconnecting ASP outputs a logic zero on STMS, to force the board level 1149.1 bus to remain in the RT/IDLE state. If the new select protocol was issued while the backplane 1149.1 bus was in its TLRST state (PTMS=1), MX2 of the disconnecting ASP outputs a logic one on STMS, to force the board level 1149.1 bus to remain in the TLRST state. Once again, the ability to maintain the RT/IDLE state on a disconnected board is very important because it allows tests to be setup and executed on more than one board at a time.

## 3.6 Advantages in Using ASPs

When comparing the described 1149.1 star configuration against the ASP configuration of Figure 2, it is clear that the ASP approach eliminates the need for additional TMS signals required by the star configuration. Thus the ASP provides a method of overcoming the problem stated for the 1149.1 star configuration.

Also, when comparing the use of different backplane buses to interface into 1149.1 board environments vs using the ASP, it is clear that the ASP does not require use of sophisticated, and bandwidth reducing translation circuitry. Thus the ASP provides a method of overcoming the problems related with using different backplane buses to access 1149.1 board environments.

Further, since the select and acknowledge protocols can be transmitted while the 1149.1 bus is in either the RT/IDLE or TLRST states, the board being disconnected can be left in either an idle or reset state. Thus the ASP provides a method of overcoming the forced-reset-on-disconnect problem associated with the approach described by Bhavsar.

## 4.0 Commandable ASPs

In small backplanes, a single centralized PSBM may be all that is necessary to serially access boards for test and maintenance operations. However, as the number and complexity of boards in a backplane

grows, the serial access task increases to where a single centralized PSBM cannot handle the task in a timely manner. Anticipating the need for distributed test control, the ASP can be expanded to include a connection method and command set to enable board resident remote SBMs (RSBM) to autonomously test boards.

The addition of a command set, enables the ASP to perform other features in addition to its basic backplane to board connection function. Some of the commandable features include; (1) a method of connecting RSBMs to the board level 1149.1 bus, (2) a method of commanding RSBMs to independently test boards, (3) a method of non-intrusively monitoring the status of a remote test operation, and (4) a method of transferring data between a board resident memory and PSBM. The ASP's data transfer method achieves the same goal as the data transfer methods used in the P1149.5 and P1394 standard proposals. These commandable features further improve the ASPs ability to serve, in combination with 1149.1, as a system backplane test bus.

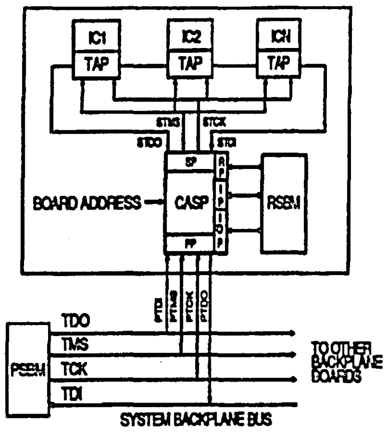



FIGURE 5 CASP Circuit Application

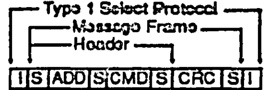
In Figure 5, a board is shown consisting of functional ICs (1-n), a commandable ASP (CASP), and a RSBM. The RSBM consists of a processor for executing local test programs, a memory for storage of test programs and data, an interrupt port, and an 1149.1 master interface port. The RSBM's processor and memory can either be dedicated for test or shared with the system logic on the board. The CASP consists of an 1149.1 primary port (PP) for interfacing to the backplane PSBM, an 1149.1 secondary port (SP) for interfacing to the functional ICs, an 1149.1 remote port (RP) for interfacing to the RSBM's master interface port, an interrupt port (IP) for interfacing to the RSBM's interrupt port, and an I/O port (IOP) for interfacing to the RSBM's memory. If required, additional I/O ports may be added to the CASP to provide parallel interfaces to other memories or I/O devices.

## 4.1 Expanded Select Protocol

To allow commands to be input to the CASP, the select protocol is expanded to allow for command transfer. In the ASP, a select protocol was defined by the transfer of a first I signal to start the select protocol, followed by the transfer of an address frame (of D signals) bounded by first and second S signals, followed by a second I signal to stop the select protocol. The select protocol of the CASP follows this format but expands the definition of the address frame into what is referred to as a message frame.

The select protocol message frame consists of a header containing an address (ADD) and command (CMD) field, and a cyclic redundancy check (CRC) field. The address field selects the CASP, the command field commands the CASP, and the CRC field is used for error detection. All fields within the message frame are separated by an S signal. The message frame may include optional fields between the header and the CRC field, as required by the command being sent. While the framing method allows fields to be transferred in either a fixed or variable D signal length, a fixed length field is preferred because it simplifies memory packing/unpacking operations, and improves error detection using simple signal counting techniques.

In Figure 6, examples of the two types of CASP select protocols are shown. Type 1 has a message frame containing the header's ADD and CMD fields, and the CRC field. Type 2 has a message frame containing the header's ADD and CMD fields, optional fields (OF) 1-N, and the CRC field.



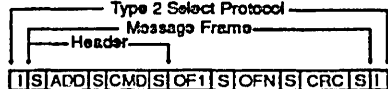




FIGURE 6 Expanded Select Protocols

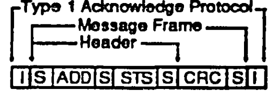
In response to receiving either select protocol type (1 or 2) from the PSBM, the CASP checks its address against the received address field. If the addresses do not match, the CASP ignores the remainder of the select protocol and does not send an acknowledge protocol. If the addresses match, the CASP checks the command field against a set of

known commands to see what operation is to be performed. In response to an unknown command, the CASP ignores the remainder of the select protocol, sets a command error bit in its status register, then sends an appropriate acknowledge protocol type (1 or 2) to the PSBM, to indicate the command error. In response to a known command, the CASP receives the remainder of the select protocol, then matches the received CRC field against a CRC it calculates on the data received in the select protocol. If the CRCs do not match, the CASP ignores the command, sets a CRC error bit in its status register, then sends an appropriate acknowledge protocol type to the PSBM, to indicate the CRC error. If the CRCs match, the CASP sends an appropriate acknowledge protocol type to the PSBM, to indicate that an error-free select protocol was received.

### 4.2 Expanded Acknowledge Protocol

To allow the PSBM to verify that the command input to the CASP was received correctly, the acknowledge protocol is expanded to allow for status transfer. In the ASP, the acknowledge protocol was defined by the transfer of a first I signal to start the acknowledge protocol, followed by the transfer of an address frame bounded by first and second S signals, followed by a second I signal to stop the acknowledge protocol. The acknowledge protocol of the CASP follows this format but expands the definition of the address frame into a message frame.

The acknowledge protocol message frame consists of a header containing an address (ADD) and status (STS) field, and a CRC field. The address field identifies the CASP, the status field informs the PSBM of the CASP status, and the CRC field is used for error detection. All fields within the message frame are separated by an S signal. The message frame within the acknowledge protocol may include optional data fields between the header and the CRC field, if required by the command sent in the previous select protocol.



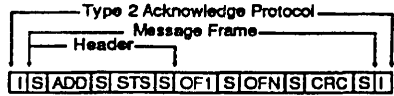




FIGURE 7 Expanded Acknowledge Protocols

In Figure 7, examples of the two types of CASP acknowledge protocols are shown. Type 1 has a message frame containing the header's ADD and STS fields, and the CRC field. Type 2 has a message frame containing the header's ADD and STS fields, optional fields (OF) 1-N, and the CRC field.

In response to receiving either acknowledge protocol type (1 or 2) from the CASP, the PSBM checks that the correct address field was received, then checks the status field for errors. After checking the address and status fields, the PSBM receives the remainder of the acknowledge protocol. At the end of the acknowledge protocol, the PSBM matches the received CRC field against a CRC it calculates on the received data. If the correct address field was received, the status field indicates no errors, and the CRCs match, the PSBM is assured that the CASP has properly received and executed the command sent in the previous select protocol. If a failure occurred in the address or status field test, the PSBM knows that the CASP did not properly receive the previous command select protocol. If the address and status fields test passed, but a CRC error occurred, the PSBM knows that an error in the optional data fields following the header fields occurred. In response to an acknowledge protocol error, the PSBM can resend the command via another select protocol.

### 4.3 Pausing During a Protocol Transfer

During the transmission of a Type 2 select or acknowledge protocol it may be necessary to pause the transfer of fields within the message frame, due to memory limitations of the PSBM and/or CASP. For example, if a large number of optional fields is being sent, the transmitting or receiving device may not have sufficient memory to allow all the message frame fields to be transferred at one time. It is necessary, therefore, to provide a method of pausing the transfer of message frame fields so that the memories of the transmitter and receiver can be periodically downloaded from or uploaded to a larger memory, such as a disk drive.

A pausing capability can be easily realized by having the transmitting device (PSBM or CASP) output additional S signals following the S signal that separates the fields. Using this approach, pausing can occur between any two field frames. The length of the pause is determined by the number of additional S signals output from the transmitter. The transferring of fields within the message frame is resumed when the transmitting device outputs a D signal to start the next field.

### 4.4 CASP Command Set

The following commands form the basic CASP command set. Some of the commands support connecting the CASP's secondary port up to either the primary or remote port, while other commands support data transfer operations between a PSBM and a board resident memory, via the CASP's I/O port. Other commands can be added as required.

### 4.4.1 Connect PSBM Command

When the PSBM needs to access the board ICs, it sends a connect PSBM command to the CASP via a type 1 select protocol. In response to the connect PSBM command, the CASP sets the "PSBM connected" status bit, sends a reply to the PSBM using a type 1 acknowledge protocol, then connects its primary and secondary ports.

After receiving the acknowledge protocol from the CASP and verifying the "PSBM connected" status bit is set, the PSBM can access the board ICs using the 1149.1 bus protocol. After the connect PSBM command has been input to the CASP, other commands that do not effect the connection between the primary and secondary ports, such as the read and write commands, can be input to and executed by the CASP.

### 4.4.2 Disconnect PSBM Command

When the PSBM completes its access of the board ICs, it sends a disconnect PSBM command to the CASP via a type 1 select protocol. In response to the disconnect PSBM command, the CASP resets the "PSBM connected" status bit, sends a reply to the PSBM using a type 1 acknowledge protocol, then disconnects its primary and secondary ports. After receiving the acknowledge protocol from the CASP, the PSBM verifies the "PSBM disconnected" status bit has been reset.

### 4.4.3 Connect RSBM Command

When the PSBM requires the RSBM to access the board ICs, it sends a connect RSBM command to the CASP via a type 1 select protocol. In response to the connect RSBM command, the CASP sets the "RSBM connected" status bit, sends a reply to the PSBM using a type 1 acknowledge protocol, then connects its remote and secondary ports. After receiving the acknowledge protocol from the CASP, the PSBM verifies the "RSBM connected" status bit is set.

After the connect RSBM command has been input to the CASP, other commands that do not effect the connection between the remote and secondary ports, such as the read and write commands, can be input to and executed by the CASP. For example, the PSBM can send a command to the RSBM, via the CASP's I/O port, to initiate the remote access operation using a write command. Further, the PSBM can monitor the status of the remote access operation, via the CASP's I/O port, using a read command.

### 4.4.4 Disconnect RSBM Command

When the PSBM determines that the remote access of the board ICs is complete, it sends a disconnect RSBM command to the CASP via a type 1 select protocol. In response to the disconnect RSBM command, the CASP resets the "RSBM connected" status bit, sends a reply to the PSBM using a type 1 acknowledge protocol, then disconnects its remote and secondary ports. After receiving the acknowledge protocol from the CASP, the PSBM verifies the "RSBM Connected" status bit has been reset.

### 4.4.5 Write Command

When data is to be transferred from the PSBM to a memory via the CASP's I/O port, the CASP receives a write command from the PSBM via a type 2 select protocol. The write command select protocol message frame contains: a header with the CASP address and write command, a starting address field where the first data field will be written, a count field indicating the number of data fields to be written, one or more data fields, and a CRC field.

At the beginning of the write command select protocol, the CASP checks its address against the received address field and the write command against known commands. In response to the write command, the CASP outputs the received starting address field on the I/O port and stores the write count field. Next, the CASP writes the first received data field to the addressed memory location and decrements the count field. If the count field is not zero after the first write operation, the ASP increments the starting memory address, writes the next received data field, and decrements the count field again. These steps are repeated until the count field decrements to zero.

When the count field decrements to zero, the CASP realizes that the last data field has been received and written to memory and the next field received is the CRC. The CASP compares the received CRC with a CRC it has calculated on the received data to check for errors, then sends an appropriate reply to the PSBM using a type 1 acknowledge protocol. After receiving the acknowledge protocol from the CASP, the PSBM verifies that the write command was successful by checking the address and status fields within the header and the CRC field for errors.

While multiple data fields will usually be transferred during the write command to upload a test program or data, a single data field can be transmitted by simply setting the count field to one. An example of a single data write command is when the PSBM sends a command to the RSBM instructing it to execute a remote test operation, such as "initiate self-test #1".

### 4.4.6 Read Command

When data is to be transferred from a memory to the PSBM via the CASP I/O port, the CASP receives a read command from the PSBM via a type 2 select protocol. The read command select protocol message frame contains: a header with the CASP address and read command, a starting address field where the first data field will be read, a count field

indicating the number of data fields to be read, and a CRC field.

At the beginning of the read command select protocol, the CASP checks its address against the received address field and the read command against known commands. In response to the read command, the CASP stores the received starting address and read count fields, then matches the received CRC against the calculated CRC.

After the read command select protocol completes, the CASP outputs the starting memory address from the I/O port, reads the first data field from memory, decrements the read count field, and starts a type 2 acknowledge protocol to transfer the data read from the memory to the PSBM. If the read count field is not zero after the first read operation, the CASP increments the memory address, and repeats the memory read and acknowledge protocol transfer sequence. When the read count field decrements to zero, the CASP realizes that the last data field has been read from memory. After sending the last data field to the PSBM, the CASP sends the calculated CRC field then terminates the acknowledge protocol.

In response to the read command acknowledge protocol, the PSBM checks the header's address and status fields, receives and stores a predetermined number of data fields, then matches the received CRC field against a calculated CRC. If no errors are found, the PSBM is assured that the read command has been executed and the data received is correct.

While multiple data fields will usually be transferred during the read command acknowledge protocol, to download test or system data, a single data field can be transmitted by simply setting the count field to one. An example of a single data read command is when the PSBM needs only to read the status of the RSBM.

### 4.4.7 Read Status Command

To allow the PSBM to read the CASP's internal status register, the PSBM sends a read status command to the CASP via a type 1 select protocol. The read status command select protocol message frame contains a header with the CASP address and read status command, and a CRC field. After checking the read status command select protocol's address, command, and CRC fields, the CASP sends a type 1 acknowledge protocol to the PSBM to transfer its status register field to the PSBM. In response to the read status command acknowledge protocol, the PSBM can check the settings of the CASP's status register bits.

The read status command, like the read and write commands, can be executed without effecting any of the connection type commands. The read status command allows the PSBM to monitor the internal status of CASP, as well as external status inputs, such as the RSBM's interrupt input. The following list defines the required status bits in the CASP's status register.

*Command Error* – *A status register bit indicating an unknown command was received.*

*CRC Error* – *A status register bit indicating a mismatch between the received and calculated CRC.*

*Interrupt Request* – *A status register bit indicating the occurrence of an external interrupt request.*

*Primary Port Connected* – *A status register bit indicating a connection between the primary and secondary ports.*

*Remote Port Connected* – *A status register indicating a connection between the remote and secondary ports.*

*Secondary Port Idle* – *A status register bit indicating that the secondary port is idle (STMS=0).*

*Secondary Port Reset* – *A status register bit indicating that the secondary port is reset (STMS=1).*

### 4.5 Global Commanding

To support a method of executing global commands, CASPs can include a global command address (GCA), similar to the reset address (RSTA) in Figure 4. During a global command select protocol, all CASPs respond to the GCA to execute the command that follows. To avoid bus contention on PTDO, CASPs do not output acknowledge protocols in response to global command select protocols.

## 5.0 Adapting the CASP for 2-wire Backplanes

As mentioned in the "Interfacing P1394 to 1149.1" section, newer 32-bit IEEE backplane standards only allocate two wires for a backplane level serial bus. If this trend continues, only a 2-wire serial bus, such as P1394, can be used in future backplanes, since both 1149.1 and P1149.5 require more than two bus wires. While P1394 is a good high speed 2-wire communications bus, its complex protocols and circuitry may be too sophisticated and/or costly for the simpler access applications involved in serial testing. To provide an alternate 2-wire serial bus for newer backplane standards, the primary port of the CASP can be easily adapted to communicate the select and acknowledge protocols using only two wires.

In Figure 8, the CASP's primary port is shown interfaced to a 2-wire PSBM via a serial input/output (SIO) wire and a clock (CLK) wire. The SIO wire combines the unidirectional TDO and TDI backplane wiring channels into a single bidirectional wiring channel. The SIO wire is capable of transferring the select and acknowledge protocols between the PSBM and CASP in response to the CLK output from the PSBM. The select and acknowledge protocols can both be transmitted on a single wire since they are transmitted at different times, as shown in Figure 3. When the CASP is

used in a 2-wire backplane, the connect and disconnect PSBM commands are no longer valid, since an 1149.1 connection is not possible in two wires. However, all the other CASP commands can be used, as previously described, to enable remote test access and data transfer operations.

Using this approach, a cost-effective 2-wire serial bus can optionally be used in newer backplane standards, in place of P1394, to provide a simple access method for test and data transfer operations. An important advantage of this approach is that it allows a common backplane test methodology to be developed and practiced, independent of the physical interfaces used in various system backplanes. For example, a backplane test access program, designed using a common CASP command set, could be used in either a 4 or 2-wire serial backplane environment. The combination of a common set of backplane test commands and a flexible serial interface, provides the building blocks from which a standard backplane test access language could be developed.

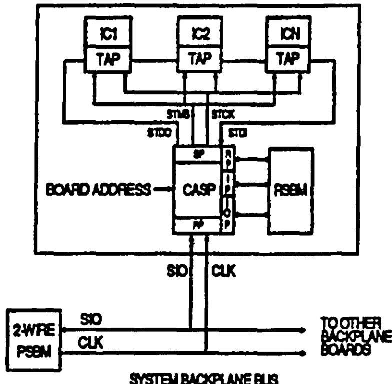



FIGURE 8 2-Wire CASP Backplane Interface

In future updates to the current 32-bit backplane buses, and in definitions of future 64-bit buses, it may be beneficial for test representatives to participate in backplane working groups to help specify backplane test bus requirements. Since a need will probably exist for both a 2-wire communications bus (like P1394) and a 2-wire test bus (like the one proposed here), an ideal scenario would be for backplane standards to specify two pairs of backplane wires so that both serial bus types could be supported. In this way, both serial buses could operate full-time in a backplane environment to optimally perform the task each was designed for. Also, since separate interfaces for the higher performance communications bus and lower performance test bus could be designed more efficiently, a lower cost of implementation would probably be achieved. Further, if separate serial buses existed at the backplane level for test and communication, the software for each bus could be designed more efficiently and executed in parallel.

## 6.0 Summary and Conclusion

This paper has described a new approach of accessing 1149.1 based boards in a backplane environment. The approach can be used as a simple backplane to board connection method or expanded to include commandable features considered useful in a backplane environment.

The ASP provides a simple backplane to board connection circuit to effectuate expanded use of the 1149.1 test bus. The select and acknowledge protocols can be transmitted between a PSBM and ASP using normal 1149.1 scan operations, assuming the PSBM can hold its TMS signal at a 1 or 0 during scan. Therefore, existing 1149.1 bus masters and software can easily be adapted to use this approach. The ASP circuit is simple and can be assembled in small footprint packages (20 pins), resulting in a low cost, low area overhead, backplane-to-board level 1149.1 test interface.

The commandable ASP (CASP) provides a way of expanding the basic ASP and protocols to suit the needs of more demanding applications, while maintaining protocol compatibility with the 1149.1 standard. The ability of the CASP to support board resident RSBMs, provides a structured method of designing systems capable of distributed test control. The ability of the CASP to support data transfer, provides a method of emulating the data transfer features being developed in the IEEE P1149.5 and P1394 serial bus standards. The ability of the CASP to operate in a 2-wire backplane environment, allows it to serve as an alternate serial bus to P1394 when only simple test access is required in a system.

The advantages offered by this new approach are: (1) direct compatibility with 1149.1, (2) improved serial data transfer bandwidth, (3) simple, cost effective implementation, (4) easily expandable to include other features useful in backplane applications, and (5) capable of being used in either a 4 or 2-wire serial bus backplane environment.

## References


1 *IEEE Std 1149.1-1990, Standard Test Access Port and Boundary Scan Architecture*
2 *IEEE P1149.5, Standard Module Test and Maintenance Bus Protocol*
3 *J. Andrews, "IEEE's 1149.5 Bus Facilitates JTAG", ATE & Instrumentation Conference, January 1991.*
4 *IEEE P1394, High Speed Serial Bus*
5 *IEEE/ANSI 896, Futurebus+*
6 *IEEE/ANSI 960, FASTBUS*
7 *IEEE/ANSI 1014, VMEbus*
8 *IEEE/ANSI 1295, Multibus II*
9 *D. Bhavsar, "An Architecture for Extending the IEEE Standard 1149.1 Test Access Port to System Backplanes", International Test Conference, October 1991.*

# *Hierarchically Accessing 1149.1 Applications in a System Environment*

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# Hierarchically Accessing 1149.1 Applications in a System Environment

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## Abstract

This paper presents a novel connection method that enables an 1149.1 test bus controller to hierarchically access and test 1149.1 circuits, independent of where the circuits exists within in an electronic system. The advantage of this approach is that it enables the 1149.1 test bus to be used hierarchically as a system level test bus, instead of only as a board level test bus.

## Background

In the electronics industry, significant improvements have been made in the area of board level testing, largely due to the development of a standard test access port and boundary scan architecture for ICs, referred to as IEEE Std 1149.1-1990 [1]. The 1149.1 standard defines a test access port and associated test circuitry that can be included in ICs to simplify testing at the board level.

One of the most important features of the 1149.1 standard is a four wire test bus that enables commands and data to be serially communicated to ICs on a board for testing purposes. The presence of this standard board level test bus interface has inspired the test community to focus on a common approach to board level testing problems.

The challenge now facing the electronics test industry is how to gain access to 1149.1 testability features after the board has been embedded within a system. Most system companies who invest in 1149.1 at the board level, do so under the assumption that the board testability resources can be reused to simplify their system testing problems. However, currently there are no proposed methods of accessing 1149.1 in a system environment. There are proposals for accessing 1149.1 boards in a backplane environment, but these proposals are focused on single level access operations and do not anticipate the hierarchical access needs found within system architectures. [2,3,4,5,7,8]

If test access solutions progress the way they currently are, the industry will eventually have a unique test access standard for each different environment level within a system. For example, the industry may eventually have different standards for: accessing multi-chip modules on a board, accessing boards in a backplane, accessing backplanes in a subsystem, and accessing subsystems in a system. If system test access evolves in this fashion, the end result may well turn out to be an overly complicated, inefficient network of non-compatible test buses interfaced together using protocol translating devices.

## Introduction

This paper presents an approach which anticipates the hierarchical test access needs of system architectures. Using this approach, hierarchical connections can be made in a system architecture to enable 1149.1 applications to be accessed directly via the standard 1149.1 test bus. The primary benefit of this approach is that it eliminates the need to use other environment-specific test buses to gain access to embedded 1149.1 applications within systems.

A paper presented at ITC in 1992 described how an 1149.1 test bus controller (TBC) could select and access 1149.1 applications in a single level environment, such as boards in a backplane, using a protocol referred to as a shadow protocol and a connection device referred to as an addressable shadow port (ASP) [6]. The approach described in this paper is based on an extended shadow protocol and a connection device referred to as a hierarchically addressable shadow port (HASP). The extended shadow protocol and HASP allow the connection features described in the 1992 paper to be used hierarchically in a system architecture, instead

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of being limited to single level connection applications.

Throughout the remainder of this paper the words "environment" and "application" are used. The word "environment" is used to indicate a physical level within a system architecture where one or more ASPs or HASPs reside. The "root environment" is the lowest level environment, and is where the 1149.1 TBC resides. The word "application" is used to indicate an 1149.1 circuit within an environment that can be accessed by a TBC after a hierarchical connection has been made. In this paper, the hierarchical access examples are described as coming from a lower level environment to a higher level environment.

## Shadow Protocols

The 1149.1 test bus has four signal wires, test clock (TCK), test mode select (TMS), test data output (TDO), and test data input (TDI). 1149.1 protocol transmitted on the TMS signal controls applications on the test bus to scan data, enter an idle state, or enter a reset state. When TMS places the test bus in an idle state (i.e. 1149.1 RT/IDLE, PAUSE-IR or PAUSE-DR states) or a reset state (i.e. 1149.1 TLRST state), all 1149.1 applications are disabled from responding to data transmitted on TDI and TDO. While the 1149.1 test bus is idle or reset, the shadow protocol can be transmitted over the TDI and TDO wires to make a connection between a TBC and a target application within a system, via an ASP or via an ASP connected to one or more HASP circuits.

The shadow protocol comprises two protocols, a select protocol and an acknowledge protocol. At the beginning of a shadow protocol, a select protocol is transmitted from the TBC to an ASP either directly or through one or more HASPs residing between the TBC and ASP to make a connection. After the select protocol has been transmitted, an acknowledge protocol is transmitted to the TBC from the selected ASP either directly or through one or more HASPs residing between the ASP and TBC to confirm the connection. The shadow protocol is transmitted on the TDI and TDO bus wires using a bit-pair signaling method. The TMS signal is not involved with the shadow protocol, therefore the TMS signal can be used to hold 1149.1 applications in a desired 1149.1 steady state while the shadow protocol is transmitted to make a connection.

The bit-pair signaling method used in the shadow protocol allows control and data to be transmitted together on a single wiring channel. The control signals are used to start and stop the select and acknowledge protocols and to frame data signals that form addresses within the select and acknowledge protocols. The bit-pair signals used in the select and acknowledge protocols are defined in the following list.

*Idle Signal (I)* – *a control signal identified by the transfer of two successive logic one bits from a transmitter to a receiver.*

*Select Signal (S)* – *a control signal identified by the transfer of two successive logic zero bits from a transmitter to a receiver.*

*Data 1 Signal (D)* – *a logic one signal identified by the transfer of a logic zero bit followed by a logic one bit from a transmitter to a receiver.*

*Data 0 Signal (D)* – *a logic zero signal identified by the transfer of a logic one bit followed by a logic zero bit from a transmitter to a receiver.*

The bit-pair signals are output from the transmitting device's (TBC's, ASP's, or HASP's) TDO on the falling edge of TCK and are input to the receiving device's (TBC's, ASP's, or HASP's) TDI on the rising edge of TCK. Since this data transfer is consistent with the way 1149.1 serial data is transferred, upgrading a TBC to support this approach is simply a matter of controlling TMS to idle or reset 1149.1 applications, while using otherwise normal 1149.1 scan operations to transmit and receive the select and acknowledge protocols.

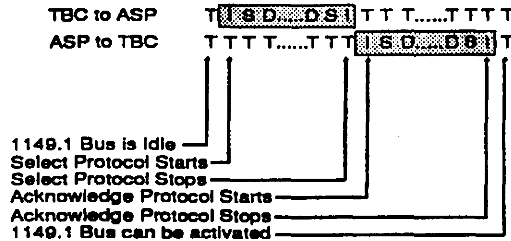



FIGURE 1 Select and Acknowledge Protocols

### Select and Acknowledge Protocols

In Figure 1, a diagram is shown of a single level select and acknowledge protocol being transmitted while the 1149.1 test bus is idle to make a connection between a TBC and

ASP application. The tristate signals (T) before and after the protocol sequences indicate that the 1149.1 test bus is idle and that the TDO outputs from the TBC and ASP are disabled and pulled high. The "ISD..DSI" sequence transmitted from the TBC to the ASP is the select protocol. The "ISD..DSI" sequence transmitted from the ASP to the TBC is the acknowledge protocol. After the ASP transmits the acknowledge protocol it connects the TBC up to the application.

The I signal at the beginning of each protocol is designed to be indistinguishable from the preceding T signals. This avoids unintentional entry into a select or acknowledge protocol when the 1149.1 bus enters an idle or reset state. However, the I signal at the end of each protocol is designed to be distinguishable from the preceding S and D signals so that it can be used to terminate the protocol. Inside each protocol, first and second S signals are used to frame the address which is defined by a series of logic 1 and logic 0 D signals.

In this single level access shadow protocol, only one address frame (SD..DS) is transmitted between the first and second I signals of the select and acknowledge protocol. However, in a multi-level shadow protocol, two or more address frames (SD..DS) are transmitted between the first and second I signals of the select and acknowledge protocol to make a hierarchical connection.

**Hierarchical Access Examples**

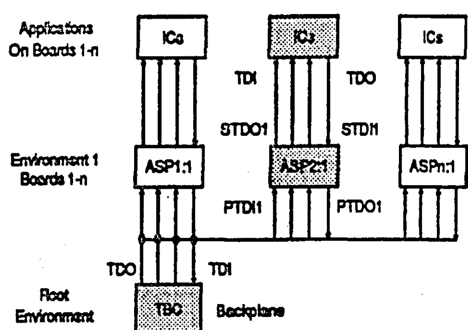
The following examples illustrate how a TBC can use ASP and HASP circuits to hierarchically access 1149.1 applications in systems having from one to "m" environment levels. In the examples, analogies are made between the way this approach hierarchically links to an 1149.1 application through multiple system environments, and the way an operating system hierarchically links to a file through multiple software directories. In the analogies, "Sys"=system, "Sub"=subsystem, "Bpn"=backplane, "Brd"=board, "App" = application, "Env"=environment, and "Dir"=directory.

Single Level System Test Access

In the single level environment of Figure 2, a Backplane resident TBC is connected to Board ASPs (1-n) via a four wire 1149.1 test bus. Each ASP is further connected to ICs on a board (application) via a four wire 1149.1 test bus. The naming convention given to the ASPs in Figure 1 is "ASPn:m", where "n" indicates the ASP's address and "m" indicates the environment level the ASP resides on. The ASPs are connected to the TBC via their primary port signals (PTDI, PTMS, PTCK, PTDO) and to the application via their secondary port signals (STDI, STMS, STCK, STDO). While all four 1149.1 signal wires are shown in Figure 2, only the ASP PTDI, STDI, PTDO, and STDO, and application and TBC TDI and TDO signals are named. The environment level number of the ASP is included in the primary and secondary port signal names, i.e. PTDI1, PTDO1, STDO1, and STDO1. The above mentioned naming conventions are followed throughout the remainder of this paper.

Hierarchical Analogies

Root Dir\1stDir1-n\File
Root Env\1stEnv1-n\App
Bpn\Brd1-n\ICs




TDO to PTDI1 T I S(A2)S I T——T
PTDO1 to TDI T——T I S(A2)S I T

FIGURE 2 Single Level System Test Access

Before an application on one of the Boards (1-n) can be serially accessed by the TBC, a connection must be made between the TBC and application. To make a connection between the application of ASP2:1 and the TBC, the TBC outputs a single level select protocol from its TDO output to the PTDI1 input of all ASPs on Environment 1. In this example, the address sent in the select protocol is address 2 (A2). In response to receiving the select protocol with an address of 2, ASP2:1 outputs an acknowledge protocol containing its

address (A2) from its PTDO1 output to the TBC's TDI input, then connects the application to the TBC (as shown in darkened boxes). The TBC verifies the connection by inspecting the address returned in the acknowledge protocol, then accesses the application using the 1149.1 protocol. This single level connection example is identical to the one described in the 1992 paper, since only a single level connection is made, i.e. board and backplane.

Two Level System Test Access

In the two level environment of Figure 3, a Subsystem resident TBC is connected to Backplane HASPs (1-n) in Environment 1. Each Backplane HASP (1-n) is further connected to Board ASPs (1-n) in Environment 2. Each Board ASP (1-n) is further connected to an Application. While connections are only shown between HASP1:1 and its ASP/Application group, each HASP is similarly connected to an ASP/Application group.

Hierarchical Analogies

Root Dir\1stDir1-n\2ndDir1-n\File
Root Env\1stEvn1-n\2ndEvn1-n\App
Sub\Bpn1-n\Brd1-n\ICs

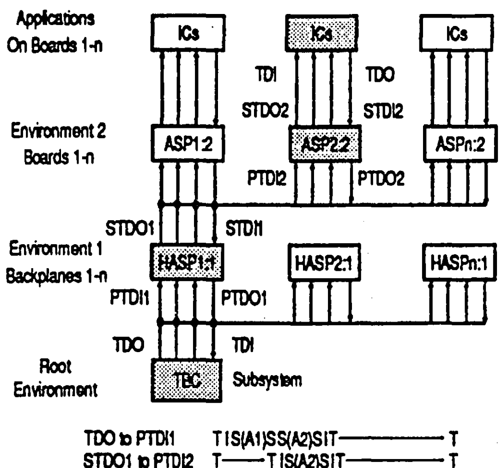



FIGURE 3 Two Level System Test Access

Before an application on one of the Boards (1-n) can be serially accessed by the TBC, a hierarchical connection must be made between the TBC and application. To make a connection between the application of ASP2:2 and the TBC, the TBC outputs a two level select protocol from its TDO output to the PTDI1 input of all HASPs on Environment 1. The two level hierarchical select protocol differs from the single level select protocol of Figure 1 in that two address frames are transmitted between the first and second I signals. The first address frame (A1) selects HASP1:1 and the second address frame (A2) selects ASP2:2.

After HASP1:1 has received its address frame (SA1S), it looks to see what signal follows the address frame. If an I signal were to follow the first address frame, HASP1:1 would recognize the protocol as a single level type and would start its acknowledge protocol. However, since an S signal follows the first address frame, HASP1:1 recognizes that the select protocol is hierarchical and that a new address frame is being transmitted. After HASP1:1 recognizes that the select protocol is hierarchical, it does not respond to any of the additional address frames it receives, thus it cannot be deselected by subsequent address frames transmitted within the current hierarchical select protocol. Also when HASP1:1 recognizes that the select protocol is hierarchical, it sets an internal flag which modifies the way it operates during the hierarchical acknowledge protocol.

In response to the start of the second address frame (SA2S) from the TBC, HASP1:1 enables its STDO1 output, sends an I signal, then relays the second address frame to ASPs of Environment 2. There is a one bit-pair signal latency between the end of the first address frame from the TBC (SA1S) and the start of the relayed second address frame from HASP1:1 (SA2S). This latency is caused by the decision step HASP1:1 performs to determine what signal (S or I) follows the first address frame (SA1S).

When the TBC completes the transmission of the hierarchical select protocol, it outputs T signals (or logic 1's) on its TDO output and monitors its TDI input for the start of an acknowledge protocol from the PTDO1 output of HASP1:1. Likewise, when HASP1:1 completes relaying the hierarchical select protocol it outputs T signals on its STDO1 output and monitors its STDI1 input for the start of an acknowledge protocol from the PTDO2 output of ASP2:2.

After ASP2:2 has received its address frame (SA2S) from HASP1:1, it starts an

acknowledge protocol output to HASP1:1. After transmitting a first I signal to initiate the acknowledge protocol, ASP2:2 outputs its address frame sequence (SA2S) from its PTDO2 output to the STDI1 input of HASP1:1. In response to the first S signal of the address frame input from ASP2:2, HASP1:1 enables its PTDO1 output and starts relaying the acknowledge protocol from ASP2:2 to the TBC's TDI input by outputting a first I signal. After ASP2:2 has transmitted its address frame to the STDI1 input of HASP1:1, it terminates its acknowledge protocol by outputting a second I signal, then makes a connection between its application and the secondary port of HASP1:1.

In response to the second I signal input from ASP2:2, HASP1:1 continues the acknowledge protocol sequence by inserting and outputting its own address frame (SA1S) to the TDI input of the TBC. After HASP1:1 has transmitted its address frame to the TBC, it terminates the hierarchical acknowledge protocol by outputting a second I signal, then makes a connection between ASP1:1 and the TBC. After the TBC receives the second I signal it determines that the hierarchical acknowledge protocol is complete and examines the addresses received to confirm the correct hierarchical connection was made. If the connection is correct, the TBC accesses the application using the 1149.1 protocol.

## Three Level System Test Access

In the three level environment of Figure 4, a System resident TBC is connected to Subsystem HASPs (1-n). Each Subsystem HASP (1-n) is further connected to Backplane HASPs (1-n). Each Backplane HASP (1-n) is further connected to Board ASPs (1-n). Each Board ASP (1-n) is further connected to an Application.

The steps for the TBC to hierarchically connect and access the application of ASPn:3 is similar to the two level access example of Figure 3 and comprises; (1) outputting a three level hierarchical select protocol to select HASP1:1, HASP2:2, and ASPn:3, (2) receiving and confirming a three level hierarchical acknowledge protocol from ASPn:3, HASP2:2, and HASP1:1, and (3) accessing the application via the connections made between HASP1:1, HASP2:2, and ASPn:3 using the 1149.1 protocol.

Hierarchical Analogies

Root Dir\1stDir1-n\2ndDir1-n\3rdDir1-n\File
Root Env\1stEvn1-n\2ndEvn1-n\3rdEnv1-n\App
Sys\Sub1-n\Bpn1-n\Brd1-n\ICs

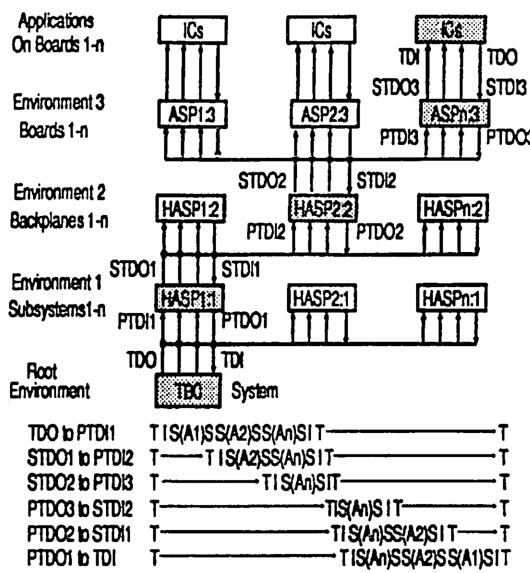



FIGURE 4 Three Level System Test Access

## Mth-Level System Test Access

While the previous examples have shown how shadow protocols and ASP/HASP circuits are used to access applications existing on 1, 2, and 3 level system environments, the approach can be used to access any environment level (m) within a system.

For example, the hierarchical select and acknowledge protocols of Figure 5 illustrate connecting an application in environment level "m" to a TBC in the root environment (RE) via intermediate environment levels E1, E2, E3...Em-2, and Em-1. Each address frame in the hierarchical select and acknowledge protocols is indicated by the sequence "Sn:mS", where "n" is the address and "m" is the environment level the address is sent to or received from. The ability of the this approach to hierarchically connect a TBC to an application on any environment level within any type of system, provides an extremely simple, yet powerful method of accessing and testing 1149.1 applications.

Hierarchical Select Protocol to Environment "m"

RE to E1 T I Sn:1 S Sn:2 S Sn:3 S....Sn:m-2 S Sn:m-1 S Sn:m S I T______T
E1 to E2 T______T I Sn:2 S Sn:3 S....Sn:m-2 S Sn:m-1 S Sn:m S I T____T
E2 to E3 T____________T I Sn:3 S....Sn:m-2 S Sn:m-1 S Sn:m S I T__T
Em-3 to Em-2 T ______________________T I Sn:m-2 S Sn:m-1 S Sn:m S I T__T
Em-2 to Em-1 T ________________________________T I Sn:m-1 S Sn:m S I T T
Em-1 to Em T __________________________________________T I Sn:m S I T

Hierarchical Acknowledge Protocol from Environment "m"

Em to Em-1 T I Sn:m S I T __________________________________________ T
Em-1 to Em-2 T T I Sn:m S Sn:m-1 S I T ________________________________ T
Em-2 to Em-3 T__T I Sn:m S Sn:m-1 S Sn:m-2 S I T ______________________ T
E3 to E2 T___T I Sn:m S Sn:m-1 S Sn:m-2 S Sn:m-3_Sn:3 S I T____________ T
E2 to E1 T______T I Sn:m S Sn:m-1 S Sn:m-2 S Sn:m-3_Sn:3 S Sn:2 S I T______ T
E1 to RE T______T I Sn:m S Sn:m-1 S Sn:m-2 S Sn:m-3_Sn:3 S Sn:2 S Sn:1 S I T

FIGURE 5 Mth-Level System Test Access

## Acknowledge Protocol Address Ordering

The ordering of the address frames in the hierarchical acknowledge protocol is key to making the scheme work in various hierarchical arrangements. By having the selected ASP of the highest accessed environment level initiate the hierarchical acknowledge protocol, HASPs in lower environment levels only have to monitor their STDI inputs to determine when the hierarchical acknowledge protocol has been started.

Since the higher level acknowledge protocols are framed by first and second I signals, it is a simple process for a lower level HASP to determine when a higher level acknowledge protocol transmission is complete so that it can insert its own address frame in the hierarchical acknowledge protocol being relayed to the TBC. By its design, the operation of the hierarchical acknowledge protocol is simple and structured, and independent of the number of environment levels it traverses.

## Hierarchical Connection Example

In Figure 6, a System TBC is connected to Subsystem HASP1 of Environment 1, HASP1/E1. HASP1/E1 is connected to Backplane HASP1 of Environment 2, HASP1/E2. HASP1/E2 is connected to Board ASP1 of Environment 3, ASP1/E3. ASP1/E3 is connected to the Application on Board 1 (ICs).

The TBC has a transmitter (XMT) to output the select protocol, a receiver (RCR) to receive the acknowledge protocol, and a controller (CTL) to regulate the operation of the transmitter and receiver, and the TMS output signal. When the controller is not using the transmitter and receiver to communicate select and acknowledge protocols, the controller can use them to communicate the 1149.1 protocol by activation of the TMS output signal.

System Subsystem Environment 1 Backplane Environment 2 Board Environment 3 Board 1

XMT TDO PTDI1 RCR STDO1 PTDI2 RCR STDO2 PTDI3 RCR STDO3 TDI
TCK PTCK1 STCK1 PTCK2 STCK2 PTCK3 STCK3 TCK
CTL TMS PTMS1 CTL STMS1 PTMS2 CTL STMS2 PTMS3 CTL STMS3 TMS ICs
RCR TDI PTDO1 XMT STDI1 PTDO2 XMT STDI2 PTDO3 XMT STDI3 TDO

TBC HASP1/E1 HASP1/E2 ASP1/E3 Application

FIGURE 6 Hierarchical Connection Example

The ASPs and HASPs have a receiver (RCR) to receive the select protocol, a transmitter (XMT) to output the acknowledge protocol, and a controller (CTL) to regulate the operation of the transmitter and receiver, and the PTMS to STMS signal connection. If the receiver and transmitter are not being used to communicate select and acknowledge protocols, and if the ASP/HASP is selected, serial data and TMS control may be transferred from PTDI to STDO, from STDI to PTDO, and from PTMS to STMS during 1149.1 scan operations.

When scan access of the ICs of Board 1 is required, the TBC outputs a hierarchical select protocol to the receiver of HASP1/E1. In response, HASP1/E1's receiver strips off its address frame and relays the remaining portion of the select protocol to the receiver of HASP1/E2. In response, HASP1/E2's receiver strips off its address frame and relays the remaining portion of the select protocol to the receiver of ASP1/E3.

After the hierarchical select protocol completes, the transmitter of ASP1/E3 outputs an acknowledge protocol to the transmitter of HASP1/E2. In response, HASP1/E2's

transmitter relays the acknowledge protocol to the transmitter of HASP1/E1, inserting its own address frame before terminating the acknowledge protocol. In response, HASP1/E1's transmitter relays the acknowledge protocol to the receiver of the TBC, inserting its own address frame before terminating the acknowledge protocol.

After each HASP and ASP completes its acknowledge protocol, it connects its primary and secondary ports together. After receiving and verifying the hierarchical acknowledge protocol, the TBC's control circuit enables the transmitter, receiver, and TMS output to access the ICs of Board 1, via the connections made through HASP1/E1, HASP1/E2, and ASP1/E3, using the 1149.1 protocol.

Synchronizing 1149.1 Data Transfers

In Figure 7, an important difference is shown between the methods used by the HASPs and ASP of Figure 6 to connect their primary and secondary bus signals. In the ASP, a simple electronic switch is used to connect the primary and secondary port signals, since only a single level connection is made. However, since any number of levels may be connected using hierarchically arranged HASPs, it is important to provide a method of synchronizing the data transfer between HASP primary and secondary ports using clocked storage elements such as the D-flip flops (DFF) of Figure 7.

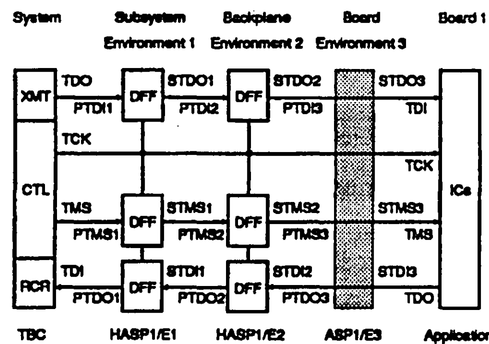



FIGURE 7 HASP Port Synchronization

If the primary and secondary bus signal connections of the HASP were made by simple electronic switches, as in the ASP, the accumulation of delays through the switches of hierarchically connected HASPs would limit the 1149.1 data transfer rate through the connection. However, with the primary and secondary HASP connections synchronized through DFFs as shown in Figure 7, delays do not accumulate as more HASPs are included in a hierarchical connection. Thus, no limitation is placed on the 1149.1 data transfer rate as more environment levels are connected between the TBC and application.

**Accessing and Testing Applications**

In Figure 8, a TBC is shown connected to the primary ports (PP) of ASPs 1-(n-2) via an 1149.1 test bus. Each ASP's secondary port (SP) is connected to an appropriately numbered 1149.1 application via an 1149.1 test bus. The TBC and applications illustrate the 1149.1 steady states in which shadow protocols can be transmitted to make or break connections between the TBC and applications. The darkened boxes of Figure 8, indicate reserved addresses "0", "n-1" and "n", which are not used as application addresses.

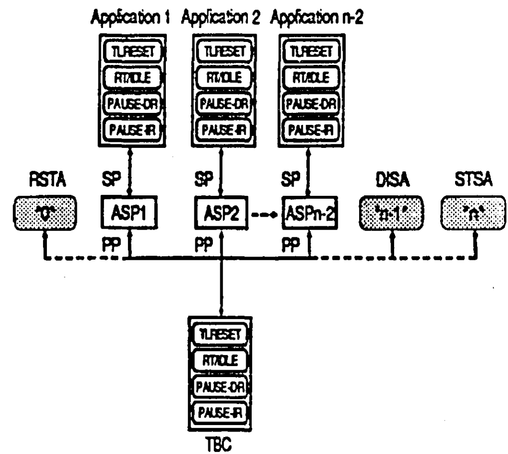



FIGURE 8 Single Level Test Access Example

The "0" address is a reset address (RSTA) recognizable by all ASPs and HASPs. ASPs and HASPs receiving the RSTA address disconnect their ports and force their applications into the TLRST state by setting their STMS output to a logic one. The "n-1" address is a disconnect address (DISA) recognizable by all ASPs and HASPs. ASPs and HASPs receiving the DISA address

disconnect their ports and remain in the 1149.1 steady state they were in when the disconnect occurs. The "n" address is a self test synchronization address (STSA) recognizable by all ASPs and HASPs. ASPs and HASPs receiving the STSA address while in the 1149.1 PAUSE-IR/DR states connect PTMS to STMS and disconnect PTDI and STDO, and STDI and PTDO.

Executing Single Application Self Tests

If Application 1 needs to be tested using a BIST based test instruction, like the 1149.1 RunBist instruction [1], and is currently in the TLRST state, the TBC moves itself to the TLRST state to synchronize states with Application 1, then executes a shadow protocol to connect to Application 1. After a connection is made between the TBC and Application 1, the TBC transitions itself and Application 1 from TLRST to the RT/IDLE state to prepare for testing.

After entering the RT/IDLE state, the TBC executes an 1149.1 instruction scan operation to load the test instruction, then returns to the RT/IDLE state. In the RT/IDLE state the test instruction starts and executes until it terminates either on its own (like RunBist) or in response to the TBC transitioning from the RT/IDLE state. While the test executes, the TBC is free to synchronize, connect, and start tests in other applications if desired. At the end of the test, the TBC synchronizes and connects to Application 1 (if it has disconnected) and accesses the test results using 1149.1 scan operations.

Executing Parallel Application Self Tests

If all applications of Figure 8 need to be tested in parallel using a BIST based test instruction, and all are currently in the TLRST state, the TBC moves itself to the TLRST state and executes the following sequence.

The TBC transmits a shadow protocol to connect Application 1 to the TBC. After the connection is made, the TBC transitions itself and Application 1 from TLRST to the RT/IDLE state. After entering the RT/IDLE state, the TBC executes an instruction scan operation to load the test instruction into Application 1 then terminates the instruction scan operation in the PAUSE-IR state. The TBC then transmits a shadow protocol containing the DISA address to disconnect Application 1 in the PAUSE-IR state. The TBC then transitions itself from PAUSE-IR to the TLRST state to synchronize 1149.1 states with the next application to be connected. These steps are repeated on Applications 2 through n-3.

After Application n-3 has been setup as previously described, the TBC transmits a shadow protocol to connect Application n-2 to the TBC. After the connection is made, the TBC transitions itself and Application n-2 from TLRST to the RT/IDLE state. After entering the RT/IDLE state, the TBC executes an instruction scan operation to load the test instruction into Application n-2 then terminates the instruction scan operation in the PAUSE-IR state. While in PAUSE-IR, the TBC transmits a shadow protocol containing the STSA address. All ASPs currently in the PAUSE-IR state respond to the STSA address to connect their PTMS and STMS signals together, enabling the TBC's TMS output to be input to each ASP application. After making this global TMS connection, the TBC transitions itself and all applications from PAUSE-IR to RT/IDLE to start the parallel test operation.

The parallel test operation continues until all tests have terminated either on their own or in response to the TBC transitioning from the RT/IDLE state. At the end of the parallel test operation, the TBC executes shadow protocols to connect to each application, one at a time, to access the test results using 1149.1 scan operations. If one or more of the ASPs in Figure 8 had not been positioned in the PAUSE-IR state when the STSA address was issued, they would have ignored the STSA address and remained in their present state. Thus, selective execution of parallel test operations is provided.

Executing Application Interconnection Tests

Testing the functional interconnection between applications is easy if each application includes 1149.1 boundary scan on its functional I/O. The test is setup by the TBC synchronizing states with and connecting to each application, one at a time. After the TBC is connected to an application it performs an 1149.1 instruction scan operation to load the 1149.1 Sample/Preload instruction. After loading the Sample/Preload instruction, the TBC performs a data scan operation to load a safe initial boundary I/O test pattern. Next,

the TBC performs an instruction scan operation to load the 1149.1 Extest instruction, terminating the instruction scan operation in the PAUSE-IR state. While in the PAUSE-IR state, the TBC executes a shadow protocol containing the DISA address to disconnect from the application so that other applications can be connected and setup as described. Since the application is disconnected in PAUSE-IR, the Extest instruction has not been updated to take effect.

After all applications have been setup as described, the TBC positions itself in the PAUSE-IR state, then transmits a shadow protocol containing the STSA address. In response to the STSA address, all applications are connected to the TBC's TMS output, via their ASPs. The TBC then transitions itself and all applications from PAUSE-IR to RT/IDLE to cause all applications to simultaneously update their Extest instructions and enter test mode. Since each application was loaded with a safe initial boundary I/O test pattern, no I/O conflicts occur between applications when the Extest mode is entered.

Following this setup procedure, interconnection testing is accomplished by the TBC selectively connecting to each application, one at a time and while in the RT/IDLE state, to set boundary outputs and read boundary inputs using 1149.1 data scan operations.

While this example used the Extest instruction to scan test the interconnections between applications, at-speed interconnection tests based on BIST (i.e. pseudorandom pattern generation/data compaction) could be used as well. If BIST interconnection testing is performed the applications are setup and enabled for testing as described in the "Executing Parallel Application Self Test" section.

## Hierarchical Access and Testing

In the example of Figure 8, the TBC was shown directly connected to the ASP of each application. In actual systems however, the TBC may not always be directly connectible to the ASP of each application due to the placement of the applications in the system hierarchy. Therefore HASPs may reside between the TBC and ASPs to provide a hierarchical connection between the TBC and applications, as shown in Figure 9.

The access and testing procedures previously described in regard to the single level connection arrangement shown in Figure 8 still apply to the three level connection arrangement shown in Figure 9. The only difference in Figure 9 is that a three level connection is traversed to access and test the applications.

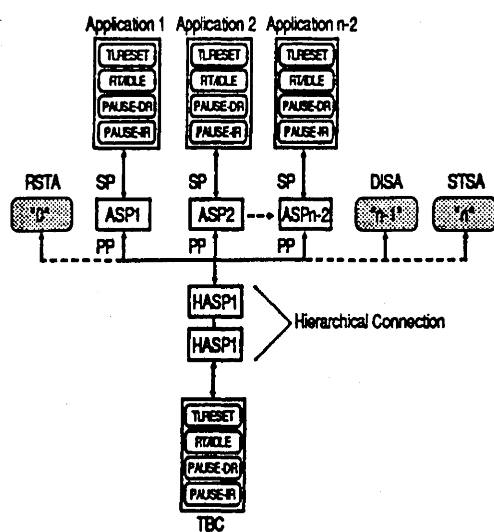



FIGURE 9 Three Level Test Access Example

## Hierarchically Sending RSTA Addresses

After hierarchically accessing and testing applications within a system, numerous applications may be left in various 1149.1 steady states and test modes. To insure the stability of the system in its mission mode, all applications need to be placed in the TLRST state following test.

One way of placing system applications in the TLRST state is for the TBC to individually connect and set each application into the TLRST state. However, a faster way of placing system applications in TLRST is for the TBC to globally transmit a hierarchical select protocol consisting of multiple RSTA address frames. Alternately, the TBC can locally place applications existing at and above a selected environment level in TLRST by sending actual address frames in a hierarchical select protocol prior to sending the RSTA frames. The actual address frames direct the reset action to only the applications at and above the selected environment level.

Hierarchical Select Protocol for Global Resetting

| | |
|---|---|
| RE to E1 | T I Sr1SSr2SSr3S.........Srm-2SSrm-1SSrmS I T.........T |
| E1 to E2 | T.........T I Sr2SSr3S.........Srm-2SSrm-1SSrmS I T.........T |
| E2 to E3 | T..................T I Sr3S.........Srm-2SSrm-1SSrmS I T......T |
| Em-3 to Em-2 | T ..............................T I Srm-2SSrm-1SSrmS I T...T |
| Em-2 to Em-1 | T ....................................T I Srm-1SSrmS I T..T |
| Em-1 to Em | T .............................................T I SrmS I T T |

Hierarchical Select Protocol for Local Resetting of Environment "m"

| | |
|---|---|
| RE to E1 | T I Sn1SSn2SSn3S.........Snm-2SSnm-1SSrmS I T.........T |
| E1 to E2 | T.........T I Sn2SSn3S.........Snm-2SSnm-1SSrmS I T.........T |
| E2 to E3 | T..................T I Sn3S.........Snm-2SSnm-1SSrmS I T......T |
| Em-3 to Em-2 | T ..............................T I Snm-2SSnm-1SSrmS I T...T |
| Em-2 to Em-1 | T ....................................T I Snm-1SSrmS I T..T |
| Em-1 to Em | T .............................................T I SrmS I T T |

FIGURE 11 Hierarchically Resetting Applications

Examples of global and local resetting in a system containing "m" environment levels are shown in Figure 11. The "r" in the address frames 1 through m indicate the RSTA address. The "n" in the address frames 1 through m indicate an actual address. All HASPs in each intermediate environment level (1 through m-1) between the root environment (RE) and environment "m" wait to respond to the RSTA address until after the hierarchical select protocol terminates, so that all relayed RSTA address frames can be transmitted to the highest environment level (m). HASPs and ASPs receiving a RSTA address do not execute an acknowledge protocol. However, HASPs that receive an actual address do respond with an acknowledge protocol.

Hierarchically Sending DISA/STSA Addresses

While Figure 11 illustrates RSTA address frames "r" being globally and locally transmitted to connections and applications, DISA and STSA address frames can be globally or locally transmitted as well. DISA address frames are transmitted in place of the "r" addresses in the hierarchical select protocols to disconnect connections and applications. STSA frames are transmitted in place of the "r" addresses in the hierarchical select protocols to synchronize selected connections and application groups to the TBC's TMS output. As with the RSTA address frame, HASPs and ASPs receiving DISA or STSA address frames do not execute an acknowledge protocol.

## Conclusion

This paper has described a hierarchical test access problem the industry will eventually face in system architectures, and a proposed solution to this problem. The solution is based on a connection circuit and protocol that can operate in any hierarchical arrangement to provide access to and test control of 1149.1 applications in a system environment. This access method provides a simple way to effectuate expanded use of the 1149.1 test bus in systems. The advantages of this approach are: (1) connection protocol is supportable by most 1149.1 TBCs/ATEs, (2) connection protocol rides on top of existing 1149.1 bus wiring, (3) does not require protocol translation in the connection path, (4) does not impact 1149.1 test bus bandwidth, (5) supports parallel 1149.1 test operations, (6) supports any type of hierarchical connection arrangement, and (7) simple, cost-effective implementation.

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# An IEEE 1149.1 Based Logic/Signature Analyzer in a Chip

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# AN IEEE 1149.1 BASED LOGIC/SIGNATURE ANALYZER IN A CHIP

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## ABSTRACT

This paper describes an IEEE 1149.1 based test IC that emulates the functions of logic and signature analysis test instruments. These ICs can be used at the board or multi-chip module level to provide an embedded method of monitoring circuits at-speed. This paper assumes the reader has a basic understanding of the IEEE 1149.1 standard[1,2].

## INTRODUCTION

Test instruments, such as logic analyzers, have traditionally been used to test the at-speed interaction of functioning ICs on board designs. These test instruments gain access to the circuit under test by physically contacting the circuit using a probing mechanism. The use of these test instruments to test functioning circuitry can reveal timing sensitive and/or intermittent failures that would otherwise not be detectable in a nonfunctional test environment. The ability of these test instruments to synchronize up with and observe the at-speed operation of electronic circuits, have made them an invaluable asset in a wide range of testing applications.

With the increasing use of high-speed, state-of-the-art integrated circuits in combination with the miniaturized substrates on which they are assembled, the physical access between an external test instrument and a circuit under test is being severely reduced and in some cases completely eliminated. New test approaches such as the IEEE 1149.1 boundary scan standard provide a method to regain electrical access to miniaturized circuits and substrates through the use of an IC resident test port and boundary scan architecture. The 1149.1 standard provides an excellent method of testing the structural integrity of the wiring interconnects between ICs on a common substrate[3,4]. In addition, 1149.1 can be used to test individual ICs while they are in a nonfunctional mode.

However, the 1149.1 standard cannot be used effectively for at-speed functional testing of ICs or circuits. The standard does provide a test instruction, referred to as Sample/Preload, that allows the boundary scan register to take a snapshot sample of the data entering and leaving a functioning IC. While a specific application of the Sample/Preload instruction has been described[5], its general use suffers due to problems not addressed in the standard[6].

One problem with the Sample/Preload instruction is that there is no prescribed method of synchronizing the sample operation with the operation of the host IC. Sampling data asynchronously is a hit and miss proposition that serves no useful purpose. Another problem is that there is no prescribed method of qualifying when to execute the sample operation in a functioning system. Sampling data synchronously but at random does little to support testing. The solutions to these potentially challenging problems is left up to the user of 1149.1.

A new approach, therefore, is required to provide a method of functionally testing the at-speed operation of miniaturized electronic circuits. The approach described in this paper overcomes the loss of functional test access to state-of-the-art circuitry through the use of an IC designed specifically for embedded at-speed testing applications. This test IC is a member of TIs SCOPE™ family of testability components[7,8], and is referred to as a Digital Bus Monitor (DBM). The DBM can be implemented in board or multi-chip module designs and coupled to critical functional IC bus signals to provide a method of non-intrusively monitoring the functional operation of the circuit.

When the DBM is enabled via serial input from the 1149.1 test bus, it synchronizes up with the functional circuitry to perform data trace and/or data compaction on the at-speed data flow between the functional ICs of the circuit. Following the test, the trace data and/or signature collected can be accessed via the 1149.1 test bus for processing.

The advantage offered by the DBM is that it enables the use of traditional at-speed test approaches without having to physically probe the electronic circuit being tested. Also, since the DBMs are embedded in the product and accessible via the 1149.1 test bus, the tests they provide are reusable throughout the life cycle of the product. For example the DBMs can be used for at-speed testing of the product at the assembly site, then later reused during other phases of the products life cycle such as; hardware/software integration and debug, at-speed system testing, environmental chamber testing, and field testing and diagnostics.

## DBM ARCHITECTURE

The DBM is a 28 pin device designed in compliance with the rules set forth in the IEEE 1149.1 boundary scan standard. The DBM supports all required 1149.1 boundary scan test instructions as well as a rich set of special test instructions supporting its data trace and signature analysis test operations. The data trace and signature analysis operations can operate from control input from the 1149.1 test bus or from control generated internal to the DBM.

The DBM IC architecture of Figure 1 has input pins for receiving 16 data inputs (D0-15), 3 clock inputs (CK1,CK2,CK3), an event qualification input (EQI), an output pin for outputting an event qualification output (EQO), and a bidirectional pin for inputting or outputting a polynomial input/output signal (PIO). In addition, the DBM is coupled to the 1149.1 test bus via the test data input (TDI), test data output (TDO), test

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mode select (TMS), and test clock (TCK) pins, to provide a standard serial interface for input and output.

The DBM consists of a 1Kx16-bit trace memory for test data storage, a 16-bit parallel signature analysis (PSAR) register for test data compaction, a 16-bit comparator for pattern detection, an event qualification module (EQM) for at-speed test control, a programmable clock interface (PCI) for clock conditioning, a boundary scan register for interconnect testing, and a 1149.1 circuit block consisting of a control register for instruction amplification, a bypass register for abbreviating the scan path through the DBM, an instruction register for instruction storage, and the 1149.1 test access port (TAP).

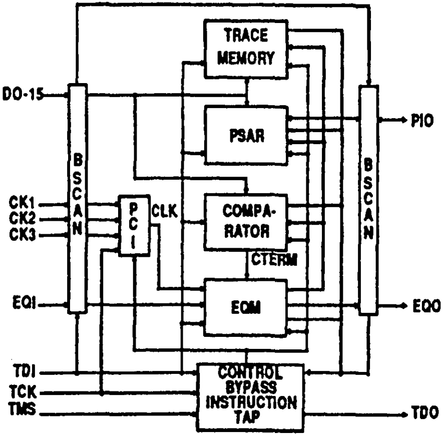


FIGURE 1 DBM Architecture

### 1149.1 Circuitry

The TAP along with the instruction, bypass, and boundary scan registers are test circuits required in the 1149.1 standard. The TAP receives the 1149.1 TMS and TCK bus control signals and provides the interface through which an external test bus controller can input control to shift data through the IC from the TDI input to the TDO output, or effectuate an 1149.1 controlled test operation. The instruction register provides storage for test instructions shifted into the IC. The bypass register provides a single bit scan path through the IC when 1149.1 testing is not being performed. The boundary scan register consists of a series of cells associated with each IC input and output pin. When placed in their test mode, the boundary cells can be accessed via the TAP to output test data from the IC's outputs and receive test data into the IC's inputs, in accordance to the IEEE 1149.1 Extest instruction.

### Trace Memory

The trace memory receives the 16-bit data bus, serial input from the TDI pin, control input from the TAP and EQM, and outputs serial data to the TDO pin. The trace memory is a 16-bit by 1024 location static RAM. When disabled the trace memory powers down and requires minimum power to maintain its contents. When enabled the trace memory can be used to store the 16-bit data input to the DBM in response to control input from either the TAP or EQM. The DBM can receive and store 16-bit data words at up to 40Mhz.

The trace memory of Figure 2 consists of a 1Kx16-bit static RAM, a 16-bit data input/output register (DIOR), a 10-bit address register (AREG), and read/write control circuitry. The read/write control circuitry receives control input from the TAP and EQM, and outputs control to the DIOR, AREG, and RAM. The selection of which control input is used, TAP or EQM, is determined by the instruction in the 1149.1 instruction register.

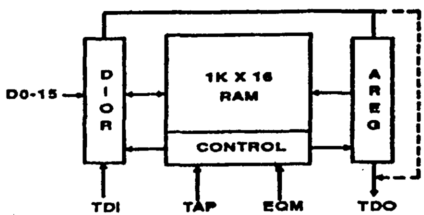


FIGURE 2 Trace Memory

When trace operations are controlled from the 1149.1 TAP, data input on the data bus is clock into the DIOR register then transferred into the addressed RAM location during each TCK while the TAP is in its RT/IDLE state. After each data pattern is written to RAM, the AREG is incremented to address the next RAM location.

When trace operations are controlled from the EQM, data input on the data bus is clocked into the DIOR register during each CLK output from the PCI. However, the data is only transferred into the RAM when the EQM is qualified, via input from either the internal CTERM or external EQI signal, to execute one of its eight selectable test protocols. After a data pattern is transferred into the RAM, the AREG is incremented to address the next RAM location.

### Trace Memory Read/Write Modes

The RAM has two modes of serial read/write access, 1149.1 scan access mode and direct memory access mode (DMA). The RAM access mode is selected via an instruction loaded into the instruction register. In the 1149.1 scan access mode, the TAP inputs or outputs RAM data via the DIOR and AREG registers by cycling through multiple data register scan operations. During each scan operation the AREG addresses a RAM location to be written to or read from via the DIOR. Each RAM read or write cycle requires one 1149.1 data register scan operation.

In the DMA mode, the DIOR is configured as either a serial input/parallel output register for DMA write operations or a parallel input/serial output register for DMA read operations, and the AREG is configured as a counter. During DMA write operations, a DMA controller embedded in the TAP, outputs control to cause serial data to be shifted into the DIOR from the TDI input. After the DIOR has received a predetermined number of bits, the DMA controller inputs control to cause the RAM

to accept the parallel data from the DIOR, the AREG to increment, and the DIOR to continue inputting serial data. These steps of serially inputting data to the DIOR, writing the data into the RAM, and incrementing the AREG are repeated until the RAM is full.

During DMA read operations, the DMA controller inputs control to cause the DIOR to parallel load data from the RAM. After the data is loaded, the DMA controller inputs control to cause the AREG to increment, and the DIOR to shift data out via the TDO output. When the last bit is shifted out, the DMA controller repeats the steps of parallel loading RAM data into the DIOR, incrementing the AREG, and shifting data out of the DIOR until the RAM data is read.

The reason for developing the DMA mode for RAM access is that it significantly reduces read/write access time to embedded memories over using the 1149.1 scan approach, especially in a system environment where multiple devices precede and follow the target device. The time savings is brought about by the fact that the DMA mode allows a single, but extended 1149.1 data register scan cycle to stream serial data continuously into or out of a device's embedded memory without interruption.

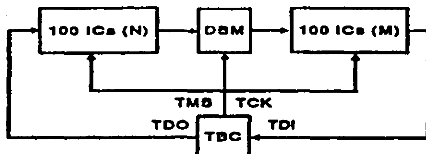


FIGURE 3 Trace Memory Access Example

To illustrate the time savings using the DMA mode to access the DBM's memory over using the 1149.1 data register scan mode, calculations are made on the example system scan path environment illustrated in Figure 3. The scan path consists of a test bus controller (TBC), a DBM, 100 1149.1 compliant ICs (N) between the TDO output from the TBC and the TDI input to the DBM, and 100 1149.1 compliant ICs (M) between the TDO output from the DBM and TDI input to the TBC.

In both the 1149.1 (1) and DMA (2) RAM access mode calculations, assume a 5Mhz TCK and that the ICs preceding and following the DBM are in their Bypass mode. Since the scan path is symmetrical the read and write access times are identical for both DMA and 1149.1 access modes, so only a read access calculation will be performed on each. A comparison of the calculated RAM access times, shows the DMA access time (3.3ms) to be 93% less than the 1149.1 access time (47ms).

(1) <u>1149.1 Access Time</u> $= [(L_{sp} x S_{st} + D_{st}) x T_{ck}] x M_{pd} = 47$ ms

Where: $L_{sp}$ = Length of scan path = (N+DBM+M) = (100+26+100)
$S_{st}$ = TAP Shift state
$D_{st}$ = TAP Dead states (4)
$T_{ck}$ = TCK period (200ns)
$M_{pd}$ = Memory pattern depth (1024)

(2) <u>DMA Access Time</u> $= (L_{dior} x M_{pd} x S_{st} + D_{st} + L_{m}) x T_{ck} = 3.3$ ms

Where: $L_{dior}$ = Length of DIOR register (16)
$L_{m}$ = Length of M scan path (100)
$S_{st}$ = TAP Shift state
$D_{st}$ = TAP Dead states (4)
$T_{ck}$ = TCK period (200ns)
$M_{pd}$ = Memory pattern depth (1024)

## Trace Memory Self-Test

The trace memory was designed with a self-testing capability that enables quick verification of the DBM's RAM in both an IC production and field test environment. The self-test is executed in two steps. The first step loads the RAM contents with test patterns, and the second step compacts the contents of the RAM into a signature.

The first step, RAM initialization, can be accomplished using one of two methods. One method uses RAM upload instructions designed to allow the data scanned into the DIOR to be automatically uploaded into the RAM for 1024 TCKs while the TAP is in its RT/IDLE state. Two RAM upload instructions are provided to allow data to be uploaded into the RAM in either a fixed or toggled format. This automatic RAM upload method is also used to initialize the RAM prior to performing a data trace operation. The other method of initializing the RAM uses the DMA input method. While the DMA input mode takes longer to load the RAM than the RAM upload instructions, it allows deterministic test patterns to be input to the RAM for more thorough testing.

The second step, RAM compaction, is accomplished using a RAM data compaction instruction. The data compaction instruction enables the RAM contents to be read and compacted into a 16-bit signature for 1024 TCKs while the TAP is in it's RT/IDLE state. During this instruction, the DIOR operates as a multiple input signature register (MISR) and the AREG operates as a self incrementing RAM address counter.

If desired, deterministic testing of the RAM can be achieved efficiently using the DMA input and DMA output instructions to stream data into and out of the RAM. The RAMs data retention can be tested by disabling the RAM to its low power mode after it has be initialized, then enabling the RAM and testing its contents using either the data compaction or DMA output instruction.

## PSA Register

The PSAR receives the 16-bit data bus, serial input from the TDI pin, control input from the TAP and EQM, and outputs serial data to the TDO pin. Also the PSAR is coupled to a bidirectional pin serving as a polynomial input or output (PIO) to allow cascading the PSARs of multiple DBMs. The PSAR is used to sample or compact data input to the DBM via the data bus in response to control input from either the TAP or EQM. The selection of which control input is used, TAP or EQM, is determined by the instruction in the 1149.1 instruction register. The PSAR can receive and compact data words at up to 40 Mhz.

The PSAR in Figure 4 consists of a 16-bit MISR and data bit masking circuitry. The polynomial tap connections in

the MISR are programmable via input from the control register in the 1149.1 circuit block of Figure 1, to enable use of any polynomial feedback equation during data compaction operations[9]. Also the bit masking circuitry receives masking control input from the control register to selectively mask one or more of the data bus input signals from being compacted into the MISR. This bit masking feature allows the MISR to operate as a parallel, serial, or selectable input signature analyzer. Also the bit masking provides a method of diagnosing why a parallel signature fails, by repeating the test on individual or selected groups of non-masked inputs[9].

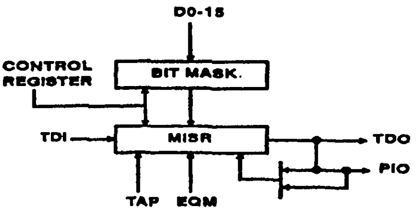


FIGURE 4 PSA Register

When PSAR operations are controlled from the 1149.1 TAP, data input on the data bus is compacted into the MISR during each TCK while the TAP is in its RT/IDLE state. When PSAR operations are controlled from the EQM, data input on the data bus is compacted into the MISR when the EQM is qualified, via input from either the internal CTERM or external EQI signal, to execute one of its eight selectable test protocols. After either data compaction operation is complete, the signature can be shifted out of the MISR by loading in an PSAR read instruction and performing a data register scan operation to shift out the contents of the MISR.

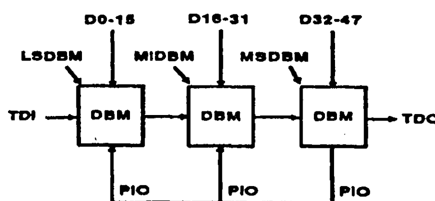


FIGURE 5 Cascading DBMs

The PSARs of multiple DBMs can be cascaded in 16 bit increments to form wider parallel signature analysis registers. For example, Figure 5 illustrates three DBMs cascaded to form a 48-bit PSAR. During cascaded PSAR operation, the least significant DBM's (LSDBM) TDI input is disabled, the TDO output is enabled to output the quotient from the MISR, and the PIO pin is configured as a polynomial input to the MISR. The middle DBM's (MIDBM) TDI input is enabled to receive the TDO output from the LSDBM, the TDO output is enable to output the quotient from the MISR, and the PIO pin is configured as a polynomial input to the MISR. The most significant DBM's (MSDBM) TDI is enabled to receive the TDO output from the MIDBM, the TDO output is disabled, and the PIO pin is configured as a quotient output from the MISR.

Since the MISR in each DBM is designed using an internal type polynomial feedback circuit, any number of MIDBMs can be placed between a LSDBM and MSDBM without incurring the delays associated with external type polynomial feedback circuits.

## Comparator

The comparator receives the 16-bit data bus, serial input from the TDI pin, control input from the TAP and EQM, and outputs a compare term (CTERM) to the EQM and serial data to the TDO pin. The comparator is used during EQM controlled data trace and compaction test operations to detect patterns input to the DBM via the data bus and output a CTERM signal to the EQM in response to a detection.

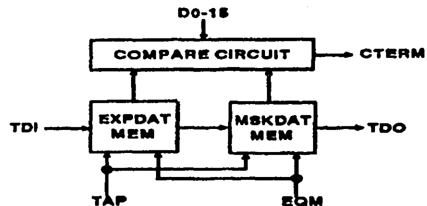


FIGURE 6 Comparator

The comparator in Figure 6 consists of a 16-bit compare circuit, and two 16x16 memories used to store expected data and mask data patterns. The memories are accessible for data input/output using either 1149.1 data register scan or DMA access modes described in the trace memory. The memories provide storage of 16 levels of 16-bit expected and mask data, enabling the comparator to perform up to 16 levels of pattern detection. The mask data memory provides selective bit masking on each of the 16 pattern detection operations. Masked bits become don't cares and are not used in the compare operation.

## Programmable Clock Interface

The PCI receives clock inputs from the CK1, CK2, CK3, and TCK pins, control input from the control register, and outputs a conditioned clock signal to the EQM. The PCI is programmable via input from the control register to couple one of the clock inputs or its complement to the PCI CLK output, or combine the clock inputs using Boolean AND and OR functions and couple the combined clock signal or its complement to the PCI CLK output. The purpose of the PCI is to minimize clock gating and selection logic external to the DBM. For example, the PCI clock inputs can programmed to accept Motorola or Intel type read/write bus control without any external interfacing logic.

## Event Qualification Module

The EQM is a test control macro that has been developed by Texas Instruments to provide a standard method of enabling an IC's test circuitry during normal operation of the IC[6]. The EQM receives control input from the TAP, clock input from the PCI, external event input from the EQI pin, internal event input from the CTERM signal, serial data input from the TDI pin, and outputs event signals to the EQO pin and serial data to the TDO pin.

The EQM of Figure 7 consists of a test controller, an event multiplexer, and a scan path consisting of command (CMD), loop counter (LPCNT), and event counter (EVCNT) sections. The test controller operates synchronous to the CLK output from the PCI to execute one of eight predefined test protocols. The protocol to be executed is input to the test controller via the CMD register. The LPCNT register serves as a programmable 16-bit counter enabling a protocol to be looped up to $2^{16}$ times. Each protocol is executed in response to event inputs from the event multiplexer. The event multiplexer can be set via the CMD register to select the event input to come from either the internal CTERM signal from the comparator or from an external signal input via the EQI pin.

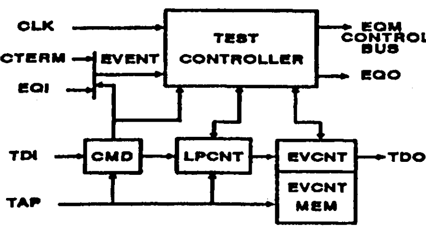


FIGURE 7 Event Qualification Module

The EVCNT register serves as a programmable 16-bit counter enabling a protocol to be started or stopped on the Nth occurrence of predetermined events. Also the EVCNT register can be used within a protocol to enable testing for a programmed number of CLK cycles, from N = 1 to $2^{16}$. To allow for multiple Nth events and multiple clocked test operations within a test protocol, a 16x16 EVCNT memory is coupled to the EVCNT register. The EVCNT memory can be accessed for input and output using either 1149.1 scan operations or DMA operations as described in the trace memory section. When an existing count has expired in the EVCNT register, the test controller uploads a new count pattern into the EVCNT register. Each protocol can use up to 16 different count patterns during the execution of a test operation.

During EQM controlled data trace and/or data compaction operations, the EQM outputs control to the trace memory and PSAR via the EQM control bus. Also the test controller outputs test status or internal event signals off chip via the EQO pin. In the status output mode, test status signals can be output from the EQO pin to indicate, among other things, (1) test-in-progress or (2) end-of-test. These status outputs can be monitored by external controllers or testers to determine the state of the test being performed. Alternately, these test status signals can be inspected via 1149.1 instruction register scan operations.

In the event output mode, the CTERM signal from the comparator can be output from the EQO pin to indicate the occurrence of an internal event. The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation. The action of outputting an internally detected event on the EQO pin of one IC to be received by the EQI input of another IC enables EQMs to cross trigger one another. This cross triggering scheme can be expanded to where multiple ICs can participate via an external voting circuit to generate a global cross triggering mechanism between EQO outputs and EQI inputs.

## EQM Test Protocols

The eight EQM test protocols are summarized in the following protocol test action code statements. In each protocol, "M" references a count value from 1 to $2^{16}$ in the 16-bit LPCNT, "N" references 1 of 16 stored count values (1 to $2^{16}$) that can be loaded into the 16-bit EVCNT, "test" refers to a data trace and/or data compaction operation, "event" refers to a signal input to the EQM from either the CTERM output of the comparator or the EQI input pin, and "clock" refers to the CLK output from the PCI circuit.

**Protocol 1:** For M times do;
On $N^{th}$ event do test
End of test

**Protocol 2:** For M times do;
During $N^{th}$ event do test
End of test

**Protocol 3:** For M times do;
On $N^{th}$ event start test
On $N^{th}$ event stop test
End Of Test

**Protocol 4:** For M times do;
On $N^{th}$ event start test
On $N^{th}$ event stop test
after N clocks
End of test

**Protocol 5:** For M times do;
On $N^{th}$ event, test for
N clocks
End of test

**Protocol 6:** For M times do;
On $N^{th}$ event,
Pause N clocks
Then test for N clocks
End of test

**Protocol 7:** On $N^{th}$ event, test for N clocks
Then for M-1 times do;
Pause for N clocks
Test for N clocks
End of test

**Protocol 8:** On $N^{th}$ event, For M times do;
Pause for N clocks
Test for N clocks
End of test

## DBM TEST APPLICATIONS

As described previously, the DBM can operate in two test modes, an off-line test mode controlled by the TAP, and an on-line test mode controlled by the EQM. In the off-line test mode the circuitry to be monitored needs to be placed in a nonfunctional mode and preferably under 1149.1 control. In the on-line test mode the circuitry to be monitored may remain in its normal functional mode while being tested by the DBM.

In Figure 8, a typical circuit is shown consisting of a processor, RAM, ROM, I/O port, buffering/transceiving

circuits, and two DBMs. This circuit could be realized on either a printed circuit board or multi-chip module substrate, and may be one of many such circuits in an electronic system. During functional operation, the processor outputs address and control to enable data transfers between it and one of the other devices in the circuit. DBMs are coupled to the processors address, data, and control buses.

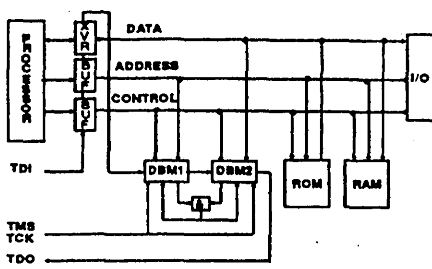


FIGURE 8 DBM Application Example

While non-testing buffers/transceivers could have been used in this circuit, 1149.1 compliant ones are implemented to provide embedded control and observability of the processors 16-bit data, 16-bit address, and control buses. The 8-bit buffers and transceivers used, like the DBMs, are members of TIs SCOPE family of testability components and are referred to as SCOPE octals[7].

In addition to their buffering and transceiving functions, the octals include circuitry supporting both 1149.1 boundary scan and built-out-self-test features. The term built-out-self-test (BOST) is probably one the reader may not be familiar with and is coined here to differentiate from the common terminology of built-in-self-test (BIST). BIST is a pseudorandom based test structure designed primarily to test circuits inside an IC, whereas BOST is a pseudorandom based test structure designed primarily to test circuits outside an IC.

While in their functional mode, the octals allow the data, address, and control bus signals to pass through unobstructed. However, when placed in their test mode, the octals can execute all required 1149.1 scan based test operations as well as additional pseudorandom based BOST features[8,10,11]. One of the BOST features included in the octals that is pertinent to the DBM's off-line test mode description is the ability to generate and output pseudorandom test patterns in response to control input from the 1149.1 test bus.

## DBM Off-Line Test Examples

The primary objective of an off-line test of the circuit in Figure 8 is to verify the structural integrity of the interconnections between the ICs. Most manufacturing failures are those related to shorts and opens in either the wiring interconnects between ICs or the solder connection between ICs and their associated substrate footprints. A secondary objective of the off-line test is to verify the basic functionality of each component in the circuit.

### 1 – Off-Line Shorts Testing

To achieve the shorts test part of the primary objective, the octals as well as the DBMs are scanned into their 1149.1 external test (Extest) mode. In the Extest mode the devices are operable to output test patterns from their outputs and receive test patterns into their inputs under control input from a test bus controller on the 1149.1 test bus. During the shorts test, the octals are scanned to output a sequence of test patterns, such as walking ones, on the data, address, and control buses. Concurrently, the DBMs are scanned to receive the test patterns from the octals and output them to the test bus controller for inspection.

Alternately, a shorts test on the data and address buses could be accomplished by enabling the octals to generate and output pseudorandom patterns while the DBMs receive and store the patterns into their trace memory and/or compact the patterns into their PSAR. After the test is complete, the test bus controller accesses the stored test pattern response and/or signature from the DBMs for processing. This shorts test may provide a reduced test time over the scan based shorts test, since the test patterns are generated by the octals, not scanned into the octals.

### 2 – Off-Line Opens Testing

To achieve the opens test part of the primary objective, the octals are scanned into their 1149.1 Extest mode and operated under control input from the test bus controller to emulate processor read and write operations to the RAM, ROM, and I/O port. Good connectivity between the octals and the RAM and I/O port is verified by successful read and write operations. Good connectivity between the octals and the ROM is verified by successful read operations.

### 3 – Off-Line Component Testing

To achieve the secondary objective of the off-line test, the functionality of the RAM, ROM, and I/O port must be verified. The I/O port can be easily verified by scanning the octals into their Extest mode and inputting and outputting a sequence of data to the I/O port via multiple 1149.1 scan cycles.

The RAM can be tested by first loading it with test patterns, then reading back the test patterns to verify they were input and output correctly. While there are ways to automate the loading of the RAM using the BOST features of the octals, the loading here is performed by scanning the octals into their Extest mode, then scanning them multiple times to provide the address, data and control required to load the RAM.

After the RAM is loaded, the octals are scanned to setup the RAM read part of the test. During RAM reads, the output of the data octals are disabled, the control octal is set to Extest mode and outputs control for read operations, the higher order byte addressing octal is set to Extest mode and addresses a 256 location address range within the RAMs memory space, and the lower order byte addressing octal is set to output pseudorandom patterns within the specified 256 location RAM memory space during the TAP RT/IDLE state. Also DBM2 is scanned to enable its trace memory to operate during the TAP RT/IDLE state. During the RT/IDLE state, the low order address octal outputs

addresses on the falling edge of the TCK and DBM2 stores RAM output data on the rising edge of the TCK.

After 254 TCKs the test bus controller moves the octals and DBM2 out of the RT/IDLE state, scans the higher order address octal to point to the next 256 location address range within the RAM memory space, then moves the devices back into the RT/IDLE state for 254 more TCKs. The 255th TCK of each address sequence is produced upon moving out of the RT/IDLE state. This process is repeated four times to fill the trace memory of DBM2.

After the trace memory fills, the test bus controller inputs a DMA output instruction into the DBM and streams out the contents of the trace memory. The test bus controller must read the first (>00) memory location of each 256 location address range using the Extest mode to complete the test. This additional step is required since pseudorandom generators cannot produce an all zero output. This entire process is repeated until all the RAM data has been read.

Testing of the ROM is simpler than the RAM since no preloading of test data is required. During ROM testing the octals and DBM2 are setup and operated as described in the RAM read test description. The only difference is that the ROM will be located in a different memory map space than the RAM.

If a faster ROM or RAM read access is desired, the data read from either could be compacted into a 16-bit signature using DBM2's PSAR. After the data is compacted, the signature is accessed by the test bus controller and compared to an expected value. The reduction in test time is brought about by the ability of the PSAR to compact the entire contents of the ROM or RAM before outputting the signature to the test bus controller.

Additional SCOPE buffering/transceiving devices are being developed. These devices will be in 8, 16, and 18-bit configurations, and will provide both pseudorandom and binary counting output modes. The binary count output mode will eliminate the missing read operations to "all zero" address locations associated with the pseudorandom output mode. Also, if 16-bit devices were used in this example, the RAM/ROM read operations would be much more efficient since they would not have to be interrupted every 256 locations to scan in the next higher 256 location address range.

## DBM On-Line Test Examples

The objective of an on-line test of the circuit in Figure 8 is to verify that the circuit as well as the controlling software functions properly at its rated speed. If the circuit passes an off-line structural and component test, there is a good chance it will operate at-speed. However, subtle problems associated with the interaction of the ICs in response to software control cannot be adequately tested in an off-line test environment.

To provide an embedded on-line testing method, the DBMs can be controlled via their internal EQMs to monitor the circuits functional operation. During on-line testing the octals remain in their functional mode and do not participate in the test. The 16-bit data bus input of DBM1 is connected to the processors address bus to allow triggering on and tracing of address patterns. The 16-bit data bus input of DBM2 is connected to the processors data bus to allow triggering on and tracing of data patterns. The CK 1, 2 and 3 inputs of both DBMs are connected to the processors control bus to allow test operations to be enabled and synchronized with read, write, or read/write bus transactions. The TAP pins of the DBMs are connected to the 1149.1 test bus to allow an external test bus controller to input test instructions, monitor test status, and receive test results.

To expand the DBMs event qualification capability, the EQO outputs from both DBMs are input to an And gate, and the EQI inputs to both DBMs receive the output from the And gate. This is a standard configuration for ICs equipped with EQMs and allows the qualification of a test operation to be determined by events detected in DBM1, DBM2 or both DBM 1 and 2.

Since the DBMs have eight protocols from which a monitoring operation may be controlled, the first step is to determine the type of test to be performed, then select a protocol best suited for the test. For example, if the test is to trace data bus transactions occurring between two particular addresses, protocol 3 would suffice. Alternately, if the test is to sample a single data pattern in response to the occurrence of a particular data and/or address pattern, then protocol 1 one may be used. Moreover, if the test is to compact data appearing on the data bus for a predetermined number of bus cycles in response to the occurrence of a particular data and/or address pattern, then protocol 5 may be used. The range of defined protocols provides the user with a very flexible triggering environment through which a test operation may be effectuated.

After choosing the appropriate test protocol, the control and data required by the protocol is input to the DBMs via the 1149.1 test bus. Following this protocol setup procedure, an instruction is input to the DBMs, via the 1149.1 test bus, to initiate the on-line test operation. Once the DBMs receive the on-line test instruction, their operation is autonomous from the 1149.1 test bus. During test, the test bus controller can monitor the state of the DBMs by accessing test status information via 1149.1 instruction register scan operations.

When the test bus controller receives an end-of-test status output from the DBMs, it performs an instruction register scan operation to input an instruction to access the test results. If a data trace operation was performed, an instruction enabling a read of the trace memory is input. If a data compaction operation was performed, an instruction enabling a read of the signature is input. After the test bus controller receives the test result data, the data may be processed as required.

In some applications, the test result data may need only to indicate a pass or fail condition using the signature analysis test mode. In other applications, the test data result may be used to help diagnose hardware/software integration problems using the data trace mode. To facilitate human interpretation of the test result data, the test bus controller may output trace data to a video monitor for display in a standard logic analyzer waveform format.

To simplify the use of the DBM's on-line test features, software support is being developed in TIs ASSET™ diagnostic system[12,13]. The software support will

include a windowing environment through which on-line test operations can be easily setup and executed, and the results displayed in a waveform format. From a users perspective the interface to DBMs will be similar to that used by traditional logic analyzer testing instruments.

The following example applications provide insight into some of the types of on-line test operations the DBM can perform on the example circuit of Figure 8.

### 1 – On-Line Testing During An Event

As part of the normal operation of the circuit, the software program controlling the action of the processor periodically addresses the I/O port to enable multiple transfers of data into and out of the circuit. The DBMs can non-intrusively trace and/or compact the circuits data I/O transfers by using DBM1 to provide the triggering function and DBM2 to provide the data trace and/or compaction function. In this example a trace operation is selected.

To setup any EQM controlled test operation, three basic decisions need to be made, (1) protocol selection, (2) protocol control input selection, and (3) number of times (M) to repeat the protocol. Since the I/O port uses only one address in the processors memory map space, Protocol 2 best fits the protocol selection for this test application (decision 1). Since the PCI circuit of the DBMs can be programmed to respond to read, write, or read/write control input from the processor, the data to be traced can be defined as input only, output only, or both input and output. To test both directions of data transfer through the I/O port, the PCI is selected to enable tracing of both input and output data (decision 2). Assuming each I/O operation transfers 100 data words and it is desired to fill the trace memory, but not overflow it, the trace operation is set to repeat 10 times (M=10), to allow 1000 I/O transfers to be traced (decision 3).

With these setup decisions made, the 1149.1 test bus controller inputs the required data and control to the DBMs to execute the I/O trace test. After starting the test, the test bus controller monitors the test status via instruction scan operations. During the test DBM1 continuously monitors the address bus for the I/O port address. When DBM1 detects the address, it outputs an EQO signal to the And gate, which in turn inputs the signal to the EQI input of DBM2. While the EQI input signal is present, DBM2 stores the I/O data transfers into its trace memory. When DBM1 detects a different address, it stops outputting the EQO signal which terminates the first I/O trace operation of DBM2.

The second through tenth repetitions of the I/O trace operation are performed exactly as the first. At the end of the tenth I/O trace operation, the end-of-test status bit is set in DBM2. When the test bus controller detects the end-of-test status, it accesses the trace data stored in DBM2 using either the 1149.1 scan or DMA output modes and either processes the data directly or displays it in a desired format for human interpretation.

### 2 – On-Line Testing Between Two Events

During program execution the processor reads and writes data and instruction words to the RAM. If desired, the DBMs can be used to trace and/or compact selectable R/W transfers between processor and RAM memory. In this example the transfers are traced. The RAM R/W trace operation differs from the I/O trace operation in that RAM is accessed via a plurality of sequential addresses within the processors memory map. Since the RAM has a different addressing scheme than the I/O port, a different protocol is required for the trace operation.

During RAM R/W tracing the DBMs need to window the trace operation between a first address that starts the RAM R/W trace operation and a second address that stops the RAM R/W trace operation. Protocols 3 and 4 support test operations bounded by starting and stopping events or in this case addresses. Protocol 4 enables additional trace operations to continue for a specified number of bus cycles after the stop event, whereas Protocol 3 stops the trace operation in response to the stop event.

Since only the data within the window is to be traced, Protocol 3 is selected for the R/W trace operation. Also, during the RAM R/W trace operation, the address associated with each data word is traced, to simplify interpretation of the data by the user. Since Protocol 3 enables the trace operation in DBM 1 and 2 to be repeated a specified number of times (M) with up to 8 pairs of different start and stop addresses (events), it is possible to perform multiple RAM R/W traces within the protocol.

For the RAM R/W trace operation both DBMs are setup to; (1) perform Protocol 3 operations, (2) trace both address and data for both read and write transfers, and (3) repeat traces for 5 times. With these setup decisions made, the 1149.1 test bus controller inputs the required data and control to the DBMs to execute the RAM R/W trace test. After starting the test, the test bus controller monitors the test status via instruction scan operations.

During the test DBM1 continuously monitors the address bus for the first trace start address. When DBM1 detects the address, it outputs an EQO signal to the EQI input of DBM2. In response to the first trace start address, DBM1 starts tracing addresses and monitoring for the first trace stop address, and DBM2 starts tracing data. When DBM1 detects the first trace stop address it signals DBM2 via the EQO to EQI signal path. In response to the first trace stop address, both DBMs stop their trace operations and DBM1 starts monitoring the address bus for the second trace start address.

The second through fifth trace operations are performed exactly as the first. At the end of the fifth trace operation, the end-of-test status bit is set in DBMs 1 and 2. When the test bus controller detects the end-of-test status, it accesses the trace data stored in DBMs 1 and 2 using either the 1149.1 scan or DMA output modes and either processes the data directly or displays it in a desired format for human interpretation. Since both address and data were traced, the display can associate each data word transfer with a particular address.

### 3 – On-Line Testing In Response To An Event

In some monitoring applications it may be desired to trace and/or compact data words transferred between the processor and I/O, RAM, and ROM in response to a single predetermined address and/or data pattern. To enable this type of test operation, Protocols 1, 5, 6, and 7

should be considered. Protocol 1 enables a single data trace and/or compaction operation in response to an event. Protocol 5 enables data trace and/or compaction for a specified number of bus cycles in response to an event. Protocol 6 enables the steps of (1) pausing for a specified number of bus cycles and (2) performing a data trace and/or compaction operation for a specified number of bus cycles. Protocol 7 enables the steps of (1) performing a data trace and/or compaction operation for a specified number of bus cycles and (2) pausing for a specified number of bus cycles. Each protocol can be repeated M times.

One application of this type of test protocol would be to use Protocol 1 to take a single snapshot sample of the data bus in response to a particular address pattern. In this application DBM1 would detect a predetermined address and output an event signal to DBM2. In response to the event input, DBM2 would execute a Protocol 1 operation to sample and store the pattern on the data bus. After the test, the test bus controller accesses the sampled pattern from DBM2 for displaying. While the other protocols of this type offer expanded test control features, many hardware and software debug tasks can be resolved by viewing a single pattern in response to a particular circuit state or condition.

Another application of this type of test protocol would be to use Protocol 5 in combination with a self test program residing in the ROM to compact the contents of the ROM into a signature. The self test program would be designed to cause the processor to sequentially read the contents of the ROM from the ROM's starting address to ending address. Prior to invoking the self test, DBM1 would be setup to detect the occurrence of a read operation to the ROM's starting address and to output an event signal to DBM2. Also, DBM2 would be setup to perform a data compaction operation on each ROM read cycle in response to an event input signal from DBM1 using Protocol 5. The N variable in Protocol 5 would be set to equal the address range of the ROM. This testing scenario assumes the processor can upload the self-test code from ROM prior to starting the ROM read operations so that the self-test code executes internal to the processor, not external to the processor. After the self test completes, the data compacted in DBM2 can be accessed by the test bus controller to compare the ROM signature against a known good signature.

Still another application of this type of test protocol would be to use Protocol 6 to respond to an event and perform a data trace and/or compaction operation after a predetermined delay. For example, if the software program transfers into an area of code that is to be tested, and it is not desired to start the test when the transfer first occurs, a delay can be setup in Protocol 6 to suspend testing for a selected number of bus cycles (N). After the delay, the data can be traced and/or compacted for a selected number of bus cycles (N). With the ability of Protocol 6 to repeat the steps of pausing and testing M times, the data trace and/or compaction operation can be accurately mapped into only those areas of code to be tested, skipping over areas of code not to be tested.

Protocol 7 is the inverse of Protocol 6 in that it allows testing to begin immediately in response to an event, then paused for a specified number of bus cycles before once again testing for a number of bus cycles. The inverse test scenario of that described for Protocol 6 can be envisioned for testing using Protocol 7.

**4 – On-Line Failure Monitoring**

While the previous examples have been associated with test operations setup and executed by a test bus controller for the purpose of testing the at-speed operation of the circuit, the DBMs can be used in a different way to achieve still another embedded monitoring capability. To set this scenario up assume that the data inputs from the I/O port indicates some external condition that the circuit is monitoring. Normally the inputs can be monitored and processed without problems. However, if an unexpected input is received that the program is unable to process, it transfers into an area of code designed to recover from such failures and to output status via the I/O port that it has encountered the failure. When attempting to diagnose the problem it would be beneficial to have a history of the circuits operation before and after the occurrence of the failure condition that caused the problem.

To provide a means of monitoring for failure conditions and for creating a history of the circuits operation before and after the failure, the DBMs can be setup using Protocol 4 to continuously trace the data and address buses while the circuit is operating. Protocol 4 is a windowing type protocol that allows the trace operation to be started in response to a first predetermined event, and stopped N clocks after the occurrence of a second predetermined event. When using Protocol 4 as control for failure monitoring, the trace functions of both DBMs are started in response to some arbitrary address/data pattern that occurs normally during the operation of the circuit. However, the second address/data pattern that initiates the termination of the trace operation is specified to be the particular address/data pattern that transfers code execution into the failure recovery and status output routine.

With the DBMs setup in this mode, they continuously input and store address and data patterns into their 1Kx16 trace memory during each bus cycle. During this test scenario, the trace memory is enabled to overflow or wraparound as it fills with data. If no failure is encountered, Protocol 4 never terminates. However, if a failure occurs the DBMs will stop storing address and data patterns into the trace memory after a specified number of bus cycles (N). The specified number of bus cycles to continue tracing after detection of a failure is defined by the user and allows partitioning the trace memory of DBMs 1 and 2 into two sections, one for pre-failure circuit history and the other for post-failure circuit history.

For example, if Protocol 4 is set to terminate the trace operation 512 bus cycles after detecting a failure, half the DBMs trace memory (512 locations) will contain information about the circuits operation before the failure and half will contain information about the circuits operation after the failure. By increasing the number of bus cycles to execute following the failure, the trace memory will contain more post-failure information. Likewise, by decreasing the number of bus cycles to execute following the failure, the trace memory will contain more pre-failure information.

A test bus controller monitoring the DBMs status via instruction register scans can determine if the Protocol 4 operation terminates. If a termination is found, the test bus controller can access the address and data patterns

stored in trace memories of DBM1 and DBM2 and provide this circuit history information to aid in diagnosing the cause of the failure.

### On-Line Testing of System Sub-Circuits

In the examples described, the DBM's on-line test modes have been shown to provide an improved method of testing the at-speed operation of the circuit in Figure 8. If the test scenario is expanded to encompass a complete system comprising multiple sub-circuits similar to the one in Figure 8, the benefit of the DBM's on-line testing features becomes even more significant.

While it is important to verify the functional operation of each sub-circuit in a system, it is even more important to verify the complete functional operation of the entire system. If DBMs were included in each sub-circuit of a system, their testing capabilities could be used to functionally test each sub-circuit, then harnessed together to provide a method of concurrently testing the functional operation of the entire system.

Such a capability would be equivalent to having logic analyzers embedded and coupled to all critical signals and buses in each buried sub-circuit within a system. System level on-line monitoring could be achieved by setting up the DBMs in each sub-circuit to perform an at-speed test operation in response to a predetermined or expected system level transaction.

For example, if the system sub-circuits are similar to the one in Figure 8, and they communicate together at the system level via their I/O port, the DBMs of each sub-circuit could be setup to monitor the I/O port for an expected input or output transaction. In response to the expected transaction, the DBMs of each sub-circuit could simultaneously execute a data trace on the local operation of each sub-circuit. After this system level test is completed, a test bus controller could access the traced data from each sub-circuit and process the data to determine how each sub-circuit responded during the predetermined system level transaction.

The power of such a test approach comes from the fact that the functional operation of a plurality of sub-circuits can be monitored concurrently and non-intrusively during normal system operation. Thus the functional interaction between multiple embedded sub-circuits in a system can be tested to verify that each sub-circuit as well as the entire system operates properly.

## SUMMARY

While the off-line and on-line test features described in this paper require adding DBMs to boards/multi-chip module substrates, the benefit gained may, in some applications, offset the additional package/die penalty incurred. Without including the DBMs in the example circuit, the type of test operations described would have to be performed using external test instruments and probing mechanisms. If the circuit is embedded within a system, access for probing may be a difficult and time consuming proposition, if possible at all.

The decision whether to use DBMs in a product is influenced by many factors such as; product type, manufacturing costs, test requirements, and life cycle costs. In any case, the DBM offers a test option currently not available to the industry, and provides a novel method of testing state-of-the-art technologies that are resistant to traditional test approaches.

## CONCLUSION

This paper has described the architecture and operation of an 1149.1 based digital bus monitor (DBM) IC. The ability of the DBM to monitor the at-speed signal transfers between ICs in real time provides a method of monitoring the functional operation of circuits assembled on board and multi-chip module substrates. Such tests can be used to reveal timing sensitive and/or intermittent failures that would otherwise not be detectable without the use of external testers and mechanical probing fixtures. This test approach may, in some cases, reduce the cost to manufacture and support a product by reducing the need for test equipment in both factory and field environments.

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# *Partitioning Designs With 1149.1 Scan Capabilities*

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SCTA031

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# Partitioning Designs with 1149.1 Scan Capabilities

by Steve Altaffer

## Introduction

### Typical 1149.1 Scan Architecture Descriptions

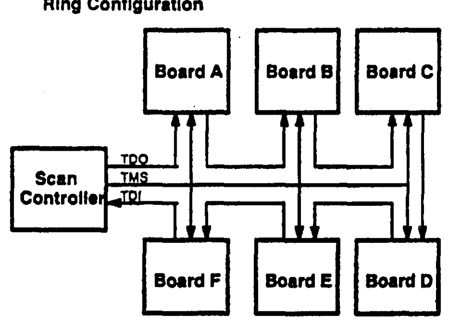
Star vs. Scan path system scan designs addressed in IEEE 1149.1 use either a single scan path, employing a common mode line and daisy-chained data (scan path), or separate mode lines to individually controlled independent rings and common TDI/TDO signals (star). Figure 1 depicts each configuration. Each can have advantages over the other depending on applications and design requirements.

The reduced path lengths of a star configuration simplify the scan controller design since each scan path is shorter than if the entire system were connected on a single scan path. Although the same amount of data may be necessary to control the entire system, the overhead of tracking unused elements in the scan path for a particular test is reduced. The star configuration is usually recommended for systems that require individualized control over independent functions or shorter scan-path lengths to simplify the scan controller design. The star configuration also has an inherent fault tolerance as an advantage. Because each of the rings in a star configuration is isolated from the system, a fault within the scan path itself does not corrupt the entire system scan path as would be the case in a scan-path configuration. A multi-board system employing a scan-path configuration has the ability to control all of the elements in a scan path regardless of the board on which they are located. A system that is backplane bus intensive or has functions spread across board boundaries would most likely employ a scan-path configuration to simplify board boundary and functional testing.

## Scan-Path Linker (SPL) and Scan-Path Selector (SPS) Overview

### Theory of Operation

The scan ring family of devices (SPS and SPL) provide the ability to create a hybrid star-scan-path architecture in a system while maintaining the advantages of both. The devices can be used to bypass an entire scan path on a board or select up to four independent rings (SPL) on the board. A single scan path can be selected and scanned or a combination of rings can be linked together in series, depending on the scan ring support device being used. Figure 2 depicts the SPS as it would be connected in a system.



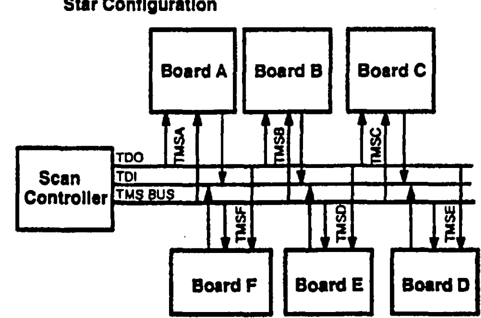




**Figure 1. Ring and Star Configurations**

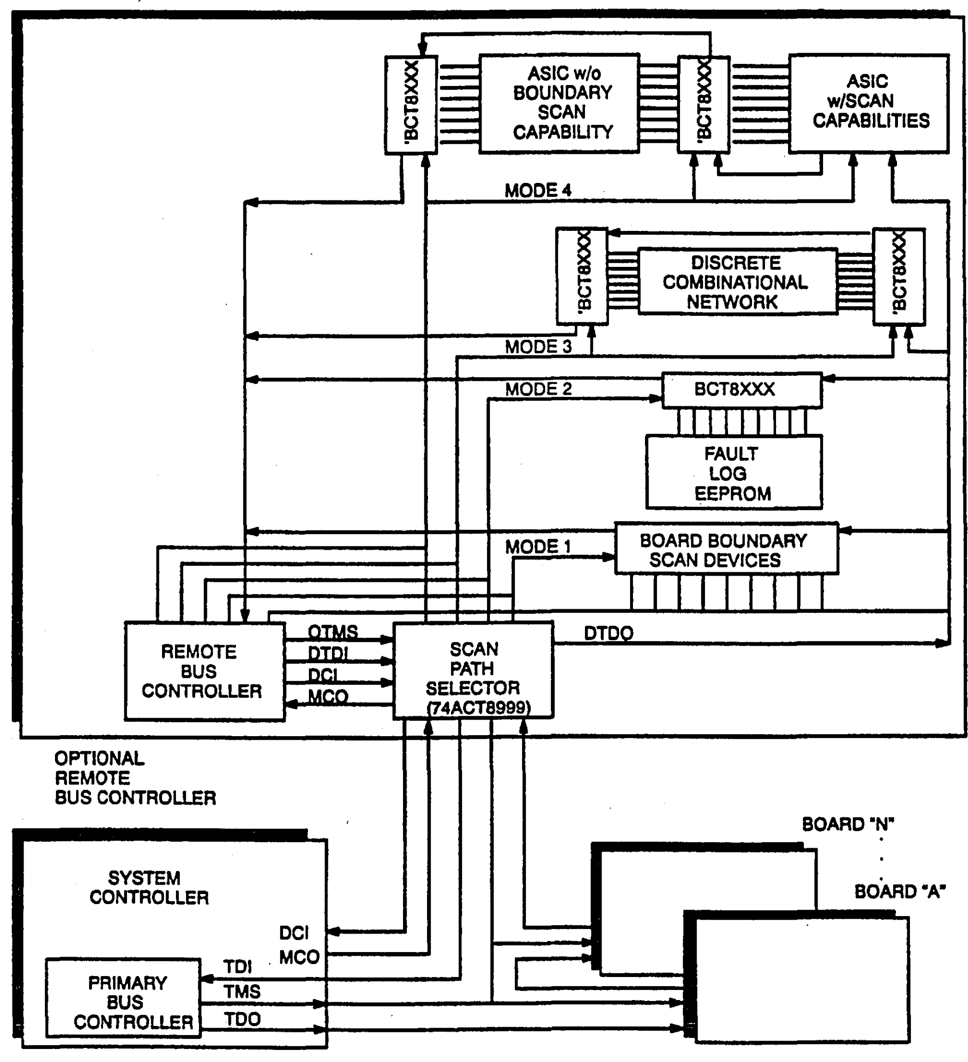



**Figure 2. SPS System Scan Design**

Note that each board is in a scan-path configuration while internal to the board, a star configuration is created by the SPS. A feature of the scan ring support devices is the ID bus that uniquely identifies a board to a system controller. The ID bus in the SPS (SN74ACT8999) also serves as a bidirectional data bus (BiD), capable of communicating with a remote bus controller or other on-board controller through the scan interface.

The 'ACT8999 also has a remote controller input that can be used to share the board's scan buses between the Primary Bus Controller (PBC) and a Remote Bus Controller (RBC) on the board. The remote input can select any of the four scan rings on a board while maintaining the primary path through the device to the rest of the system. In order to properly handshake with the board for remote-control handoff, ID bus operation,

or status/interrupt capabilities, a four-wire status bus is included in the devices. Those wires are labeled Master Condition Input (MCI), Master Condition Output (MCO), Device Condition Input (DCI) and Device Condition Output (DCO). The DCI pin also serves as the clock input to an 8-bit internal programmable counter. Properties such as the polarity of the clock, up/down counting, and latch-on-zero in the countdown mode are all programmable. The DCO pin can serve as the terminal count (MAX/MIN) output to allow cascading or interrupting the scan controller.

## Select Register Operation

The SELECT data register is an 8-bit control register that determines the output of each of the DEVICE TEST MODE SELECT (DTMS) signals (2 bits per output). The select decoding for a single DTMS is shown in Table 1.

**Table 1. Select Register Decoding**

| Select Bit MSB | LSB | DTMS Output |
|---|---|---|
| 0 | 0 | High (STRAP) |
| 0 | 1 | Low (IDLE) |
| 1 | 0 | OTMS * |
| 1 | 1 | TMS |

* For devices without OTMS input, TMS is transferred to DTMS.

It is the same for each of the other DTMS outputs. For the case of a scan-path device not having an OTMS (remote) input, the device will route the primary TMS to the selected DTMS output. When an output or outputs are selected to convey TMS, the scan-path device waits until the primary TMS enters the IDLE state before multiplexing the TMS and TDI to the secondary scan path. This ensures proper state synchronization between the primary and board scan path(s) with respect to the TAP controllers on each. Any other means to "open" a secondary scan path would result in scan-path corruption and asynchroneity of data and control, and therefore is not allowed within the scan-path device hardware. This must be clearly understood by the software or firmware controlling the scan-path device so that the hardware is configured as the software believes it is. Referring to Figure 3, when a secondary scan path is opened, the TMS is driven directly to the output with internal delays only. Due to the routing of the data path directly from TDI to DTDO, it is necessary to sample the data on the rising edge of TCK and output to the secondary scan paths on the falling edge of TCK to comply with IEEE 1149.1 specifications. This creates an extra bit of data in the path whenever an external scan path is selected, but it is necessary to ensure data synchronization to the rings at high TCK frequencies. This sync bit will be present in all data and instruction scans and must be recognized by the scan bus controller whenever a secondary scan path is opened. The data from the scan path is then fed to the "normal" input of the scan-path device data or instruction registers and output to the primary scan path. For the SPL (SN74ACT8997), much the same data path is created.

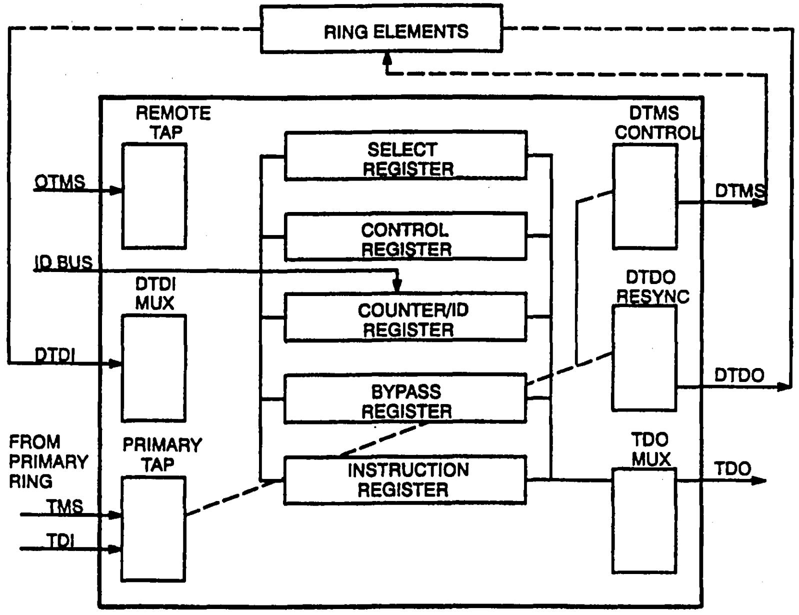



**Figure 3. Scan-Path Selector (SPS) Scan-Path Ring with Ring Selected**

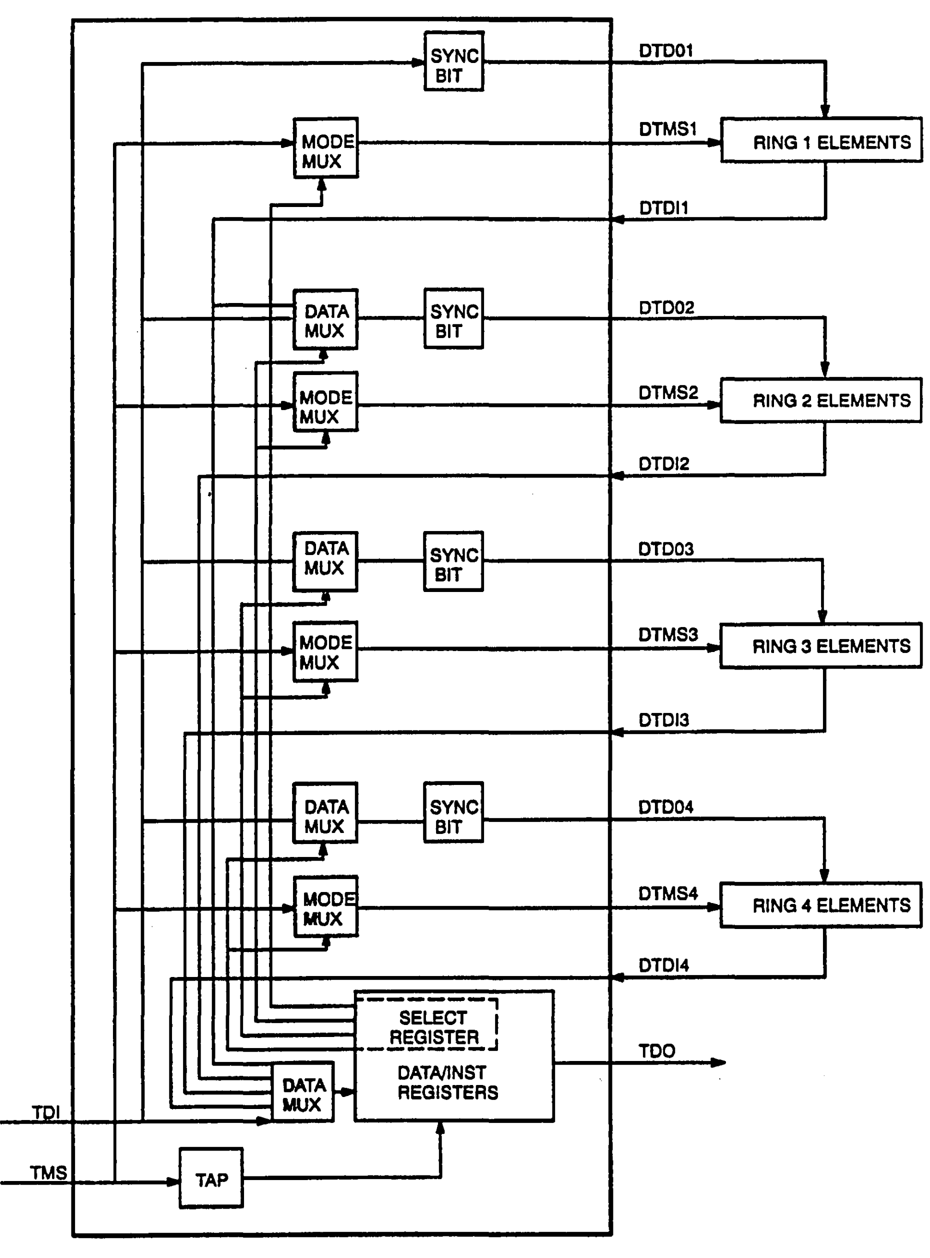
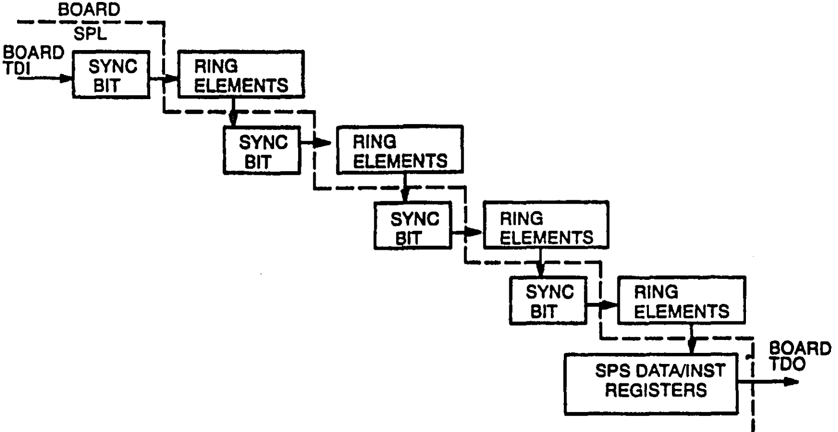
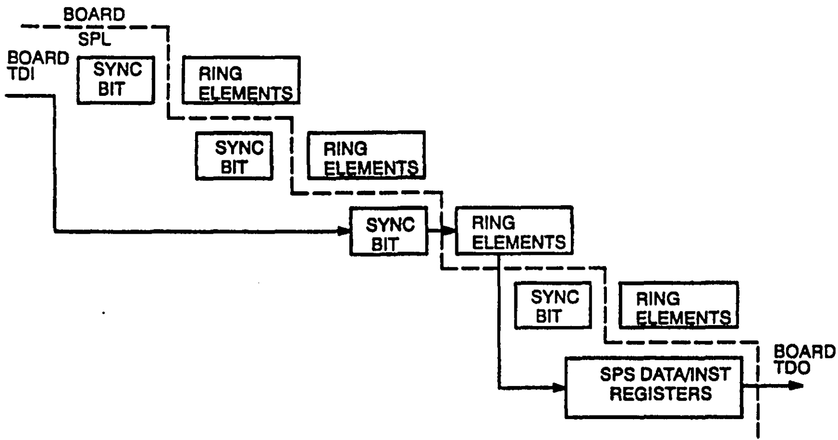



**Figure 4. Scan-Path Linker (SN74ACT8997)**




Scan-Path Linker (74ACT8997) with All Secondary Scan Paths Selected




Scan-Path Linker (74ACT8997) with One Secondary Scan Path Selected

**Figure 5. Scan-Path Linker Data Path**

Referring to Figure 4, the Scan-Path Linker again introduces an extra bit into the data path of each secondary scan path when opened. Figure 5 depicts the actual scan order when one or four secondary scan paths are opened in Scan-Path Linker.

Each of the sync bits are bypassed when a scan path is not selected and only the scan path or rings that are selected will introduce an extra bit into the path.

## Remote Bus Controller Interfaces

When a Remote Bus Controller (RBC) is present with the Scan-Path Selector, certain interfaces to and from the SPS device need to be modified to ensure proper operation. The RBC inputs its TMS output to the OPTIONAL TMS (OTMS) pin of the SPS. When the SELECT register is loaded to output OTMS to the DTMS outputs, the CONTROL register must

also be loaded with the RBC Enable bit (RBCE) set TRUE to allow the RBC TMS direct control of the SELECT register. In this mode the Remote Test Access Port (RTAP) controls the shifting of data through the DTDI to the DTDO to the rings. When the RTAP is in control a dedicated instruction and bypass register become activated to emulate a true 1149.1 interface as seen by the RBC, as depicted in Figure 6.

The only valid instructions are 'scan the select register' or 'scan the bypass bit' during this mode of operation. The Primary Bus Controller (PBC) still has the ability to scan the other registers in the SPS that enables it to disable the RBC by setting the RBCE bit to FALSE should it become necessary. When connecting an RBC to the SPS the normal interfacing must be altered as shown in Figure 7.

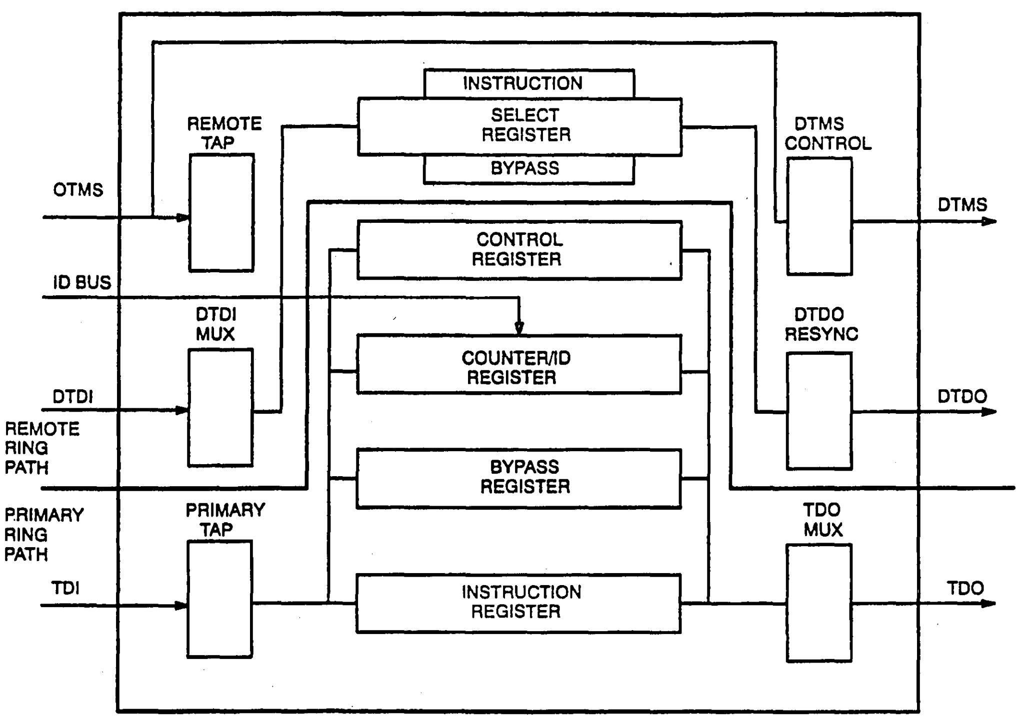



**Figure 6. Scan-Path Selector (SN74ACT8999) with Optional (Remote) TMS Selected**

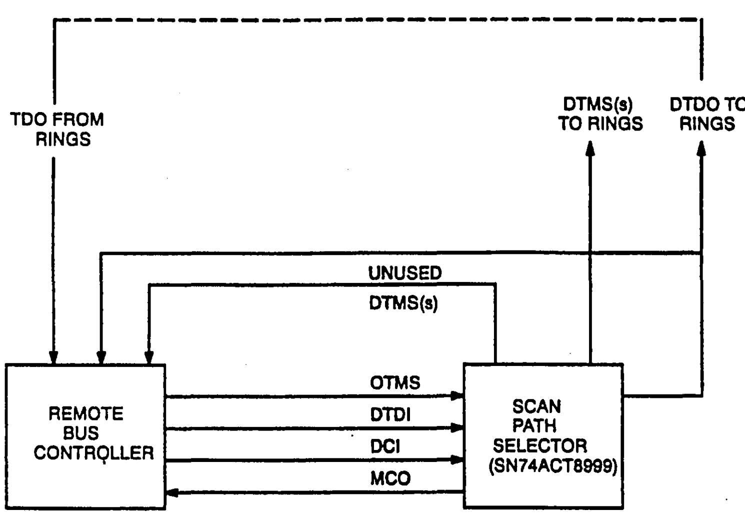



**Figure 7. Remote Bus Controller Interface to Scan-Path Selector**

The TDO signals of each of the rings must pass through the RBC in order for the RBC to receive data when active. In the same way each of the rings is resynchronized within the SPS, the RBC must clock the TDO data in and pass it out to the DTDI input of the scan-path device when inactive. For this reason, all of the DTMS signals must be fed to the RBC in order to determine when data is being shifted through a scan path so that the internal resync bit can be properly clocked or held. When activated, the RBC must also have the ability to bypass all of the rings, hence the requirement to feed the DTDO of the scan-path device directly to the RBC. Finally, to ensure proper handoff of control of the board rings, it is recommended that the RBC receive MCO from the SPS, to signal a grant from the PBC, and send DCI to the SPS, to indicate to the PBC that the RBC is currently using the board rings. This is also the handshake mechanism between the PBC and RBC for BiD bus transfers.

## Partitioning 1149.1 Designs Using the Scan-Path Support Devices

### System Level Partitioning and Considerations

#### *Design Requirements*

The ability to create a hybrid star/scan-path architecture using a scan-path device has many advantages over a single scan-path design. Scan designs can be partitioned in such a way as to completely isolate functions for testing while leaving others undisturbed. In scan-path architecture this is also possible. However, the devices not related to a particular test still must be placed in the BYPASS SCAN mode through an instruction scan, and the bypass bit in the data path must be recognized by software. In a design that requires time slice testing, that is, taking a function off-line to run a test and returning it back within a fixed amount of time, lends itself quite well to the scan-path device architecture. The controller can open a secondary scan path, test a function, and replace it to normal operation while not disturbing or scanning other functions in the system. In order to properly implement such a scheme, a careful design requirement must be developed in advance to account for any possible unexpected operations when exercising a function. For instance, an ASIC self test may inadvertently toggle its device outputs that in turn ripple to another function not under test. The inputs of the ASIC under test must be isolated so that the circuits feeding it do not effect the self-test. Avoiding inadvertent operation is probably the most common consideration but there are many others when implementing a time slice test scheme. Only through proper system definition and specification can all of the pitfalls be avoided. Another advantage of using a scan-path device is the ability to have a remote bus controller resident on the board to relieve the test burden of the primary bus controller. This creates a distributed test structure in which the PBC can command tests to be run autonomously on multiple boards and report status back. The relief realized at the system level is, of course, not

without cost. The development of board controller software will still be necessary as well as the handshaking and reporting structure between master and remote. This structure has a payoff throughout a product life cycle by exploiting tests during board and system integration, board production and depot testing as well as common module insertion. It can also reduce system test times by having all tests within a system running tests concurrently and reporting status instead of a single primary system executing tests in series.

### *Partitioning of Scan Paths*

The proper partitioning of rings is the single most important factor in successfully reaping the benefits of scan-path device insertion into a scan design. Normally a board is functionally partitioned within a system by design. Within a board, functions also need to be partitioned for scan testing by placing test-related scan elements adjacent in the scan path. When using a scan-path device this is a requirement to enable efficient use of the device. If a test requires scanning of devices on separate rings of a scan-path device on a board, the controller must scan the devices to stimulate a test, scan the scan-path device SELECT register to place the stimulus secondary scan path in IDLE in order to hold the data, and open the response scan path, and then scan the results from the response scan path. This procedure becomes even more complex should the stimulus and response elements be mixed on separate rings. Should the test involve a dynamic stimulus and response, that is not static patterns, repeatability may not be possible. This fact arises due to the need to leave either the stimulus or response elements in IDLE (which implies running) while the other is being initialized. The time between scanning the first scan-path elements and the second could be variable or cause unknown data to be generated or sampled. Careful timing analyses can be performed to eliminate the problem but such an architecture is not recommended. Instead, the linkable scan-path device, SPL, should be used if scan elements for tests MUST reside on different rings for multiple uses, i.e., an element in RING1 is used for stimulus in a test with RING2, and response with elements on RING3. In most cases this is avoidable or optimization is possible to minimize the number of "inter-scan path" tests through proper partitioning.

### *How Much Scan*

Another consideration for system-level designs is how much partitioning should be performed. Each scan-path device has four rings that can be used in a design, but not all of them have to be used. If the design does not lend itself to creating four separate rings, two or three can be used. This can create an open scan-path condition when an unused scan path is inadvertently selected. Great care must be taken during software development and design to avoid this possibility from occurring through constraint checking. If SPL is used, the DTDO and DTDI of unused rings can and should be tied together to at least create a path for data. Software must still detect the lack of any device(s) on the scan path that was opened, based upon instruction scan error checking or through examination of the scan-path device's SELECT register. This problem compounds itself when multiple scan-path devices exist within a system that have unused DTMS signals. Under such conditions the scan controller software will have to find the SELECT register contents of each scan-path device in the scan path to detect the error, determine the true state of the scan path, and correct the problem. The controller software becomes an issue in determining whether to use the scan-path device in a design. The obvious solution is to use all of the scan rings available on the scan-path device. Switching between multiple secondary scan paths for a test again becomes a problem and the SPL is recommended. If a remote controller is being used, all of the DTMS signals and the DTDO must be fed to it and can be used to detect the error condition, maintain the data-path integrity, and signal the PBC through the DCI-> DCO status signals of the condition.

## Board Boundary Testing

When implementing scan-path devices into designs that contain board boundary scan elements to test backplanes or motherboards, two options exist for placing the boundary elements as depicted in Figure 8.

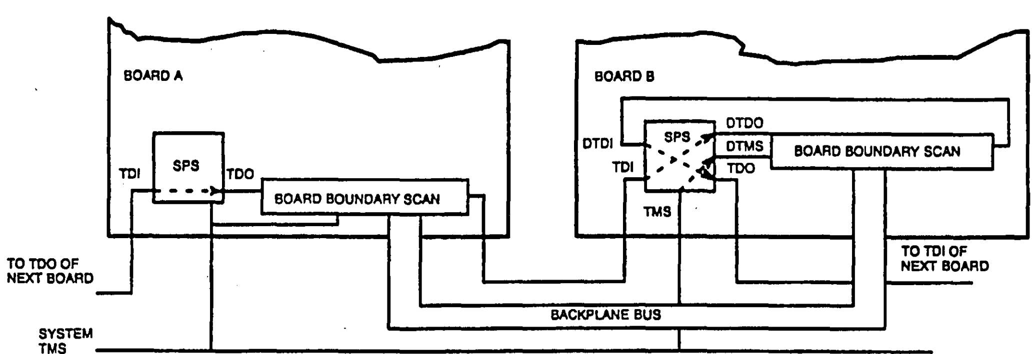



**Figure 8. Board Boundary Element Scan-Path Options**

Board A has the boundary elements placed on the primary scan path of the system. This would allow for two scenarios. First, if an RBC was also present on the board, the PBC could perform board boundary tests while the RBC performed board tests. Secondly, this implementation also allows selecting a scan path on the board and scanning the boundary elements to perform multiple tests concurrently. The disadvantage of this scheme is that the board is no longer isolated from the system by a single interface and some of the fault tolerance of the scan-path device architecture is lost. Board B places the boundary elements on a scan path of the scan-path device. This option retains all of the advantages of the scan-path device fault tolerance with the trade-off being the inability to run RBC concurrent tests if one is present in the design. In both cases board-to-board testing is still possible using the system scan-path architecture and the ability to open a scan path on each board.

## Partitioning a Board Design – An Example Memory Board Description

The example given is a simple memory board. It consists of a bus interface controller that could be an ASIC or discrete circuitry. The bus controller decodes address and control activity on the backplane and creates the necessary address and control signals required locally for memory and I/O cycles. The board also includes further decoding to create specific device selects for the memory and I/O arrays and any further control signal generation not performed within the bus controller. Finally, the board contains a memory array and I/O register array. The memory array could contain both static- and PROM-type devices.

## Partitioning for Test

The buffers for the board are chosen from the 'BCT8XXX family of 1149.1-compatible octal devices ('BCT8244,8245,8373,8374). Referring to Figure 9, the placement of these devices partition the board into its three functions; bus controller, decode circuitry, and the memory and I/O space.

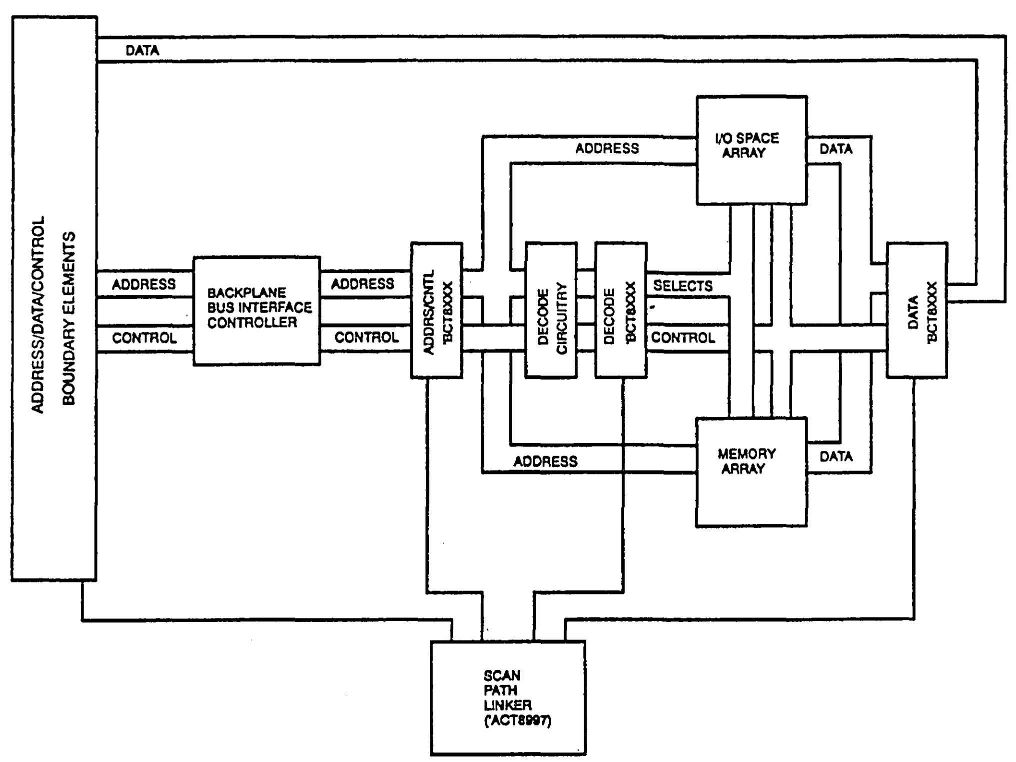



**Figure 9. Memory Board Partition Example Using Scan-Path Linker**

In addition, the backplane has been isolated by inserting the 1149.1-compatible octals for testing the interface to and from other boards using the test controller. These elements are on a scan path by themselves so that they can be scanned to perform the aforementioned tests without scanning the rest of the board. Next, 1149.1-compatible octals are placed between the bus controller and decode circuitry and between the decode circuitry and memory-I/O space arrays, each on its own scan path. Since tests of each of the functions relies on two of the scan-path device rings, the SPL is chosen. Thus, to test the memory array the control selects the address/control buffers and data buffers to be opened and links through the SPL; the boundary elements and address/control to test the bus interface controller; and so on. The address/control and decode octals could have been placed on the same scan path, but this would only serve to complicate the tests.

## Remote Bus Controller Implementation

When Remote Bus Controller (RBC) is added and the rings slightly altered to best accommodate it, the SPS with an RBC input does not allow linking of the rings. Referring to Figure 10, in order to reduce the amount of switching between the rings, the address/control and data octals are placed on the same scan path. This allows the RBC (and the PBC) to test the memory array most efficiently, since it would most likely be the longest test to be performed on the board. The boundary and decode circuitry are also placed on the same secondary scan path so that they can be tested quicker. Detection of a fault in the functions is possible, but isolation to the failing function still requires switching between secondary scan paths.

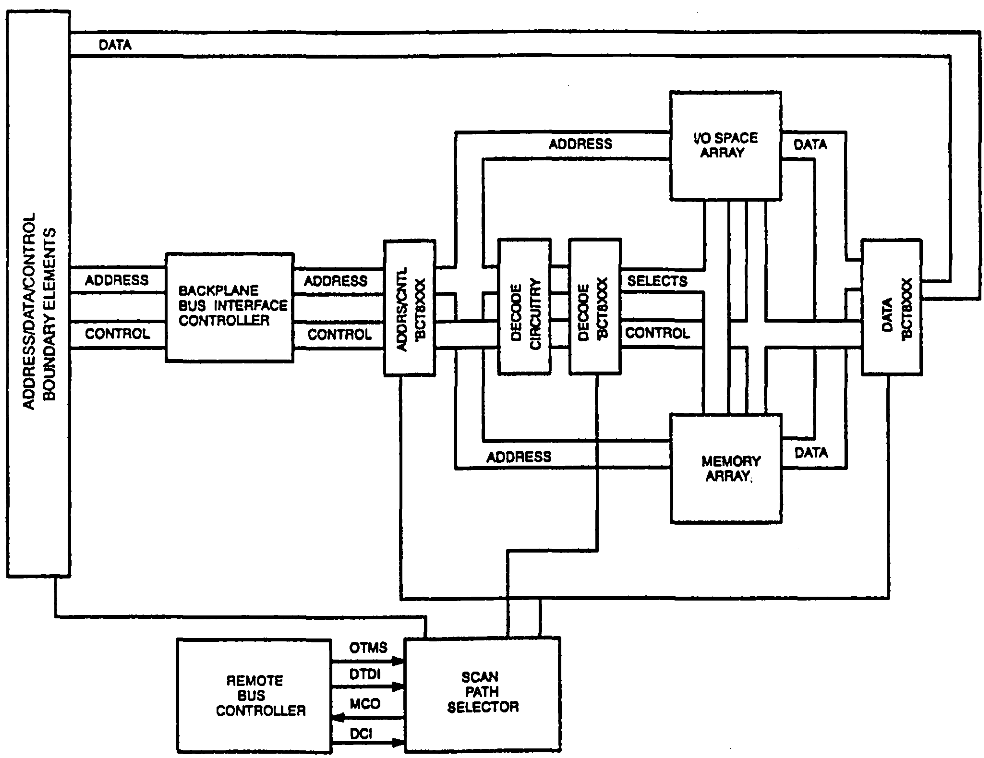



**Figure 10. Memory Board Partition Example Using Scan-Path Selector**

## NOTES

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