TEXAS INSTRUMENTS

Power Management Products

Data Book

Volume 2

2000

Analog and Mixed Signal

Data Book Volume 2

Power Management Products

2000

Power Management Products Data Book

Volume 2

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INTRODUCTION

The Texas Instruments 1999 Power Management Products Data Book Set showcases TI's broad portfolio of analog components for power supply designs. Featured in this set are most of the components previously found in the 1996 Power Supply Circuits Data Book, the new and exciting power management products introduced since then, and other components useful for power supply designs.

The set consists of three product area specific volumes:

- Power Management Products, Volume 1:
  - Linear voltage regulators
  - Shunt regulators
  - Voltage references
  - Precision virtual grounds
- Power Management Products, Volume 2:
  - Processor power supply controllers (DSP and CPU)
  - Switching power supply controllers and DC/DC charge pump converters
  - MOSFET drivers
  - Supervisory circuits
- Power Management Products, Volume 3:
  - Power distribution switches
  - LED drivers
  - Voltage Rail splitters
  - Special Functions

More than a collection of data sheets, this data book set is a tool for locating the best power management components for a successful design effort. It is structured to help you quickly find the devices best suited to your application. The set contains:

- An alphanumeric index at the beginning of each book to make finding known part numbers simple.
- Product selection guides with a condensed view of parametric information organized to help you choose the devices that most closely fit your needs.
- Key specifications and features presented for easy comparison.
- A section on mechanical specifications for all packages used with Texas Instruments power management devices.

While this data book offers design and specification data only for power management products, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or from the TI web site at:

http://www.ti.com/sc

We believe you will find the 1999 Power Management Data Book set to be a valuable addition to your collection of technical literature.

General Information (Vol. 2)

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS76912	1.224	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77012	1.224	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS76515	1.5	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76615	1.5	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76715	1.5	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76815	1.5	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76915	1.5	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77015	1.5	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS77515	1.5	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–373
TPS77615	1.5	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–373
TPS77715	1.5	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–391
TPS77815	1.5	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–391
TPS76316	1.6	150	0.36	0.6	0.085	4	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76318	1.8	150	0.3	0.5	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS73HD318	1.8	750	0.353		0.55	2	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2–185
TPS76518	1.8	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76618	1.8	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76718	1.8	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS767D318	1.8	1000	0.35	0.825	0.085	2	10	Yes	Yes	Dual, Fixed, LDO, Positive Output	2–311
TPS76818	1.8	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76918	1.8	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77018	1.8	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS77518	1.8	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–373
TPS77718	1.8	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–391
TPS77618	1.8	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–373
TPS77818	1.8	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–391
TPS76325	2.5	150	0.36	0.6	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS71025	2.5	500	0.33	0.5	0.29	2	10	Yes	No	Fixed, LDO, Positive Output	2–59
TPS7225	2.5	250			0.18	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS7325	2.5	500	0.27	0.6	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–145
TPS73HD325	2.5	750	0.353		0.55	2	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2–185
TPS76425	2.5	150	0.36	0.6	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–247
TPS76525	2.5	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261

FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS (continued)

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS76625	2.5	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76725	2.5	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS767D325	2.5	1000	0.35	0.825	0.085	2	10	Yes	Yes	Dual, Fixed, LDO, Positive Output	2–311
TPS76825	2.5	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76925	2.5	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77025	2.5	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS77525	2.5	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–373
TPS77625	2.5	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–373
TPS77725	2.5	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–391
TPS77825	2.5	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–391
TPS76327	2.7	150	0.36	0.6	0.085	3.75	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76427	2.7	150	0.36	0.6	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–247
TPS76527	2.7	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76627	2.7	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76727	2.7	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76827	2.7	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76927	2.7	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77027	2.7	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS76928	2.784	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77028	2.784	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS7228	2.8	250			0.18	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS76328	2.8	150	0.35	0.55	0.085	3.75	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76428	2.8	150	0.36	0.6	0.085	3.8	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–247
TPS76528	2.8	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76628	2.8	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76728	2.8	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76828	2.8	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS7230	3	250	0.39	0.9	0.18	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS7330	3	500	0.052	0.075	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–145
TPS76030	3	50	0.12	0.18	0.85	3	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–211
TPS76130	3	100	0.17	0.28	2.6	3.6	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–221
TPS76330	3	150	0.35	0.55	0.085	3.75	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76430	3	150	0.36	0.6	0.085	3.8	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–247

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FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS (continued)

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS76530	3	150	0.16	0.28	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76630	3	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76730	3	1000	0.45	0.675	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76830	3	1000	0.45	0.675	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS77030	3	50	0.048	0.1	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS76930	3.09	100	0.115	0.23	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS76032	3.2	50	0.12	0.18	0.85	3.1	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–211
TPS76132	3.2	100	0.17	0.28	2.6	3	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–221
TPS7133QPWP	3.3	500	0.047	0.06	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–3
TPS7133	3.3	500	0.047	0.06	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–29
TPS71H33	3.3	500	0.047	0.06	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–75
TPS7233	3.3	250	0.14	0.18	0.155	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS7333	3.3	500	0.044	0.06	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–145
TPS76033	3.3	50	0.12	0.18	0.85	3	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–211
TPS76133	3.3	100	0.17	0.28	2.6	3	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–221
TPS76333	3.3	150	0.3	0.5	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76433	3.3	150	0.3	0.5	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–247
TPS76533	3.3	150	0.14	0.24	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76633	3.3	250	0.23	0.4	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76733	3.3	1000	0.35	0.575	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76833	3.3	1000	0.35	0.575	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76933	3.3	100	0.098	0.2	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77033	3.3	50	0.048	0.1	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS77533	3.3	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–373
TPS77633	3.3	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–373
TPS77733	3.3	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–391
TPS77833	3.3	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–391
TLV2217–33	3.3	500	0.4	0.5	19	1	12	No	No	LDO	2–461
TPS76038	3.8	50	0.12	0.18	0.85	2.6	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–211
TPS76138	3.8	100	0.17	0.28	2.6	3	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–221
TPS76338	3.8	150	0.36	0.6	0.085	3.5	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS7148	4.85	500	0.03	0.037	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–29
TPS71H48	4.85	500	0.03	0.047	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–75

FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS (continued)

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS7248	4.85	250	0.09	0.1	0.155	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS7348	4.85	500	0.028	0.037	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–145
TPS7150	5	500	0.027	0.033	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–29
TPS71H50	5	500	0.027	0.033	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–75
TPS7250	5	250	0.76	0.85	0.155	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS7350	5	500	0.027	0.035	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–145
TPS76050	5	50	0.12	0.18	0.85	2	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–211
TPS76150	5	100	0.17	0.28	2.6	2.8	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–221
TPS76350	5	150	0.18	0.3	0.085	4	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76550	5	150	0.085	0.15	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76650	5	250	0.14	0.25	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76750	5	1000	0.23	0.38	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76850	5	1000	0.23	0.38	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76950	5	100	0.071	0.17	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77050	5	50	0.035	0.085	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TL750L05	5	150	0.2	0.6	10	4	26	No	No	Fixed, LDO, Positive Output	2–421
TL750M05	5	750	0.5	0.6	60	2	26	No	No	Fixed, LDO, Positive Output	2–429
TL751L05	5	150	0.2	0.6	10	4	26	Yes	No	Fixed, LDO, Positive Output	2–421
TL751M05	5	750	0.5	0.6	60	2	26	Yes	No	Fixed, LDO, Positive Output	2–429
TL750L08	8	150	0.2	0.7	10	4	26	No	No	Fixed, LDO, Positive Output	2–421
TL750M08	8	750	0.5	0.7	60	2	26	No	No	Fixed, LDO, Positive Output	2–429
TL751L08	8	150	0.2	0.7	10	4	26	Yes	No	Fixed, LDO, Positive Output	2–421
TL751M08	8	750	0.5	0.7	60	2	26	Yes	No	Fixed, LDO, Positive Output	2–429
TL750L10	10	150	0.2	0.8	10	4	26	No	No	Fixed, LDO, Positive Output	2–421
TL750M10	10	750	0.5	0.8	60	2	26	No	No	Fixed, LDO, Positive Output	2–429
TL751L10	10	150	0.2	0.8	10	4	26	Yes	No	Fixed, LDO, Positive Output	2–421
TL751M10	10	750	0.5	0.8	60	2	26	Yes	No	Fixed, LDO, Positive Output	2–429
TL750L12	12	150	0.2	0.9	10	4	26	No	No	Fixed, LDO, Positive Output	2–421
TL750M12	12	750	0.5	0.9	60	2	26	No	No	Fixed, LDO, Positive Output	2–429
TL751L12	12	150	0.2	0.9	10	4	26	Yes	No	Fixed, LDO, Positive Output	2–421
TL751M12	12	750	0.5	0.9	60	2	26	Yes	No	Fixed, LDO, Positive Output	2–429

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ADJUSTABLE OUTPUT-VOLTAGE REGULATORS

Device	V_O Adjustable (nom) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS76501	1.2 – 5.5	150	0.16	0.33	0.038	3	13.5	Yes	No	Adjustable, LDO, Positive Output	2–261
TPS76601	1.2 – 5.5	250	0.23	0.54	0.038	3	13.5	Yes	No	Adjustable, LDO, Positive Output	2–277
TPS76701	1.5 – 5.5	1000	0.5	0.825	0.085	2	10	Yes	Yes	Adjustable, LDO, Positive Output	2–293
TPS767D301	1.2–5.5	1000	0.35	0.825	0.085	2	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2–311
TPS76801	1.5 – 5.5	1000	0.5	0.825	0.085	2	10	Yes	No	Adjustable, LDO, Positive Output	2–329
TPS76901	1.2 – 5.5	100	0.071	0.245	0.017	3	13.5	Yes	No	Adjustable, LDO, Positive Output, SOT–23	2–345
TPS77001	1.2 – 5.5	50	0.035	0.125	0.017	3	13.5	Yes	No	Adjustable, LDO, Positive Output, SOT–23	2–359
TPS77501	1.2 – 5.5	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Adjustable, LDO, Positive Output	2–373
TPS77601	1.2 – 5.5	500	0.169	0.287	0.085	2	13.5	Yes	No	Adjustable, LDO, Positive Output	2–373
TPS77701	1.2 – 5.5	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Adjustable, LDO, Positive Output	2–391
TPS77801	1.2 – 5.5	750	0.26	0.427	0.085	2	13.5	Yes	No	Adjustable, LDO, Positive Output	2–391
TPS76301	1.5 – 6.5	150	0.6	0.6	0.085	3	10	Yes	No	Adjustable, LDO, Positive Output, SOT–23	2–231
TPS7101	1.2 – 9.75	500	0.052	0.085	0.285	3	10	Yes	No	Adjustable, LDO	2–29
TPS71H01	1.2 – 9.75	500	0.052	0.085	0.285	3	10	Yes	No	Adjustable, LDO	2–75
TPS7201	1.2 – 9.75	250	0.16	0.27	0.155	3	10	Yes	No	Adjustable, LDO	2–113
TPS7301	1.2 – 9.75	500	0.052	0.085	0.34	3	10	Yes	Yes	Adjustable, LDO	2–145
TPS73HD301	1.2 – 9.75	750	0.353	0.6	1.1	3	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2–185
TL317	1.2 – 32	100	2.5	3	1.5	4	35	No	No	Adjustable	2–415
µA723	2 – 37	150		3	2.3	1	40	No	No	Adjustable	2–467
TL783	1.25 – 125	700	10	15	15	6	125	No	No	Adjustable	2–449
LM237	–1.2 – –37	1500			2.2			No	No	3-Terminal Adjustable Regulator	2–409
LM337	–1.2 – –37	1500			2.2			No	NO	3-Terminal Adjustable Regulator	2–409

FIXED POSITIVE-OUTPUT VOLTAGE VOLTAGE REGULATORS

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
µA78L02A	2	100	1.7	3	3.6	5	20	No	No	Fixed, Positive Output	2–493
TL–SCSI285	2.85	500		0.7	26	1	5.5	No		Fixed Reg. for SCSI Active Termination	2–527
TL2217–285	2.85	500		1	26	1.5	5.5	No		Fixed Reg. for SCSI Active Termination	2–533
µA7805	5	1500	2	3	4.2	4	25	No	No	Fixed, Positive Output	2–479
µA78L05	5	100	2	3	3.8	10	20	No	No	Fixed, Positive Output	2–493
µA78L05A	5	100	1.7	3	3.8	5	20	No	No	Fixed, Positive Output	2–493
µA78M05	5	500	2	3	4.5	4	25	No	No	Fixed, Positive Output	2–505
TL780–05	5	1500	2	3	5	1	25	No	No	Fixed, Positive Output	2–441
µA7806	6	1500	2	3	4.3	4	25	No	No	Fixed, Positive Output	2–479
µA78L06	6	100	1.7	3	3.9	10	20	No	No	Fixed, Positive Output	2–493
µA78L06A	6	100	1.7	3	3.9	5	20	No	No	Fixed, Positive Output	2–493
µA78M06	6	500	2	3	4.5	4	25	No	No	Fixed, Positive Output	2–505
µA7808	8	1500	2.5	3	4.3	4	25	No	No	Fixed, Positive Output	2–479
µA7885	8	1500	2	3	4.3	4	25	No	No	Fixed, Positive Output	2–479
µA78L08	8	100	1.7	3	4	10	23	No	No	Fixed, Positive Output	2–493
µA78L08A	8	100	1.7	3	4	5	23	No	No	Fixed, Positive Output	2–493
µA78M08	8	500	2.5	3	4.6	4	25	No	No	Fixed, Positive Output	2–505
µA78L09	9	100	1.7	3	4.1	10	24	No	No	Fixed, Positive Output	2–493
µA78L09A	9	100	1.7	3	4.1	5	24	No	No	Fixed, Positive Output	2–493
µA78M09	9	500	2.5	3	4.6	4	26	No	No	Fixed, Positive Output	2–505
µA7810	10	1500	2.5	3	4.3	4	28	No	No	Fixed, Positive Output	2–479
µA78L10	10	100	1.7	3	4.2	10	25	No	No	Fixed, Positive Output	2–493
µA78L10A	10	100	1.7	3	4.2	5	25	No	No	Fixed, Positive Output	2–493
µA78M10	10	500	2.5	3	4.6	4	28	No	No	Fixed, Positive Output	2–505
TL780–12	12	1500	2.5	3	5.5	1	30	No	No	Fixed, Positive Output	2–441
µA7812	12	1500	2.5	3	4.3	4	30	No	No	Fixed, Positive Output	2–479
µA78L12	12	100	1.7	3	4.3	10	27	No	No	Fixed, Positive Output	2–493
µA78L12A	12	100	1.7	3	4.3	5	27	No	No	Fixed, Positive Output	2–493
µA78M12	12	500	2.5	3	4.8	4	30	No	No	Fixed, Positive Output	2–505
TL780–15	15	1500	2.5	3	5.5	1	30	No	No	Fixed, Positive Output	2–441
µA7815	15	1500	2.5	3	4.4	4	30	No	No	Fixed, Positive Output	2–479
µA78L15	15	100	1.7	3	4.6	10	30	No	No	Fixed, Positive Output	2–493
µA78L15A	15	100	1.7	3	4.6	5	30	No	No	Fixed, Positive Output	2–493

TEXAS INSTRUMENTS
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FIXED POSITIVE-OUTPUT VOLTAGE VOLTAGE REGULATORS (continued)

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
µA78M15	15	500	2.5	3	4.8	4	30	No	No	Fixed, Positive Output	2–505
µA7818	18	1500	3	3	4.5	4	33	No	No	Fixed, Positive Output	2–479
µA78M20	20	500	3	3	4.9	4	35	No	No	Fixed, Positive Output	2–505
µA7824	24	1500	3	3	4.6	4	38	No	No	Fixed, Positive Output	2–479
µA78M24	24	500	3	3	5	4	38	No	No	Fixed, Positive Output	2–505

FIXED NEGATIVE-OUTPUT VOLTAGE VOLTAGE REGULATORS

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
µA79M05	–5	500	2	3	1	4	–25	No	No	Fixed, Negative Output	2–517
µA79M06	–6	500	2	3	1	4	–25	No	No	Fixed, Negative Output	2–517
µA79M08	–8	500	2.5	3	1	4	–25	No	No	Fixed, Negative Output	2–517
µA79M12	–12	500	2.5	3	1.5	4	–30	No	No	Fixed, Negative Output	2–517
µA79M15	–15	500	2.5	3	1.5	4	–30	No	No	Fixed, Negative Output	2–517
µA79M20	–20	500	3	3	1.5	4	–35	No	No	Fixed, Negative Output	2–517
µA79M24	–24	500	3	3	1.5	4	–38	No	No	Fixed, Negative Output	2–517

SHUNT REGULATORS

Device	V_{ref} (V)	I_Z (min) (μA)	I_Z (max) (mA)	V_O (min) (V)	V_O (max) (V)	Tolerance (%)	V_I (max) (V)	Temp Coeff (typ) (ppm/°C)	Description	Page No.
TLV431A	1.24	100	15	Vref	6	1	6	46	Adjustable Shunt	3–45
TL1431	2.5	1000	100	Vref	36	0.4	36	30	Adjustable Shunt	3–27
TL431	2.5	1000	100	Vref	36	2	36	30	Adjustable Shunt	3–9
TL431A	2.5	1000	100	Vref	36	1	36	30	Adjustable Shunt	3–9
TLV431	2.5	1000	100	Vref	36	2	36	30	Adjustable Shunt	3–45
TL430	2.75	2000	100	Vref	30	9	30	120	Adjustable Shunt	3–3

PRECISION VIRTUAL GROUNDS

Device	I_O (typ) (mA)	Output Regulation (typ) (μA)	V_O (min) (V)	V_O (max) (V)	V_I (max) (V)	Temp Coeff (typ) (ppm/°C)	Description	Page No.
TLE2425	20	–45 – 15	2.48	2.52	40	20	Precision Virtual Ground	4–3

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PROCESSOR POWER SUPPLY CONTROLLERS

Device	Droop Comp	OCP	Output Drive Current (A)	Outputs	OVP	Power Good	Soft Start	UVLO	V_{IN} (V)	V_O (typ) (V)	V_{ref} (tol) (±%)	Description	Page No.
TPS5102	No	Yes	1.5	2	No	No	Yes	Yes	4.5 – 25	1.2 – Vcc	1.5	Notebook	7–3
TPS5103	No	Yes	1.5	1	No	No	Yes	Yes	4.5 – 25	1.2 – Vcc	1.5	Multipurpose	7–33
TPS5210	Yes	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	pgm 1.3 to 3.5	1	Pentium class	7–123
TPS5211	Yes	Yes	2.4	1	Yes	Yes	Yes	Yes	5, 12	pgm 1.3 to 3.5	1.5	Pentium class	7–69
TPS5602	No	Yes	1	2	No	No	Yes	Yes	4.5 – 25	1.2 – V_{CC}	2	DSP	7–149
TPS56100	No	Yes	2	1	Yes	Yes	Yes	Yes	5	0.9 – V_{CC}	1.5	DSP	7–171
TPS5615	No	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	1.5	1	DSP	7–99
TPS5618	No	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	1.8	1	DSP	7–99
TPS5625	No	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	2.8	1	DSP	7–99
TPS5633	No	Yes	2.4	1	Yes	Yes	Yes	Yes	5, 12	3.3	1	DSP	7–99

SWITCHING POWER SUPPLY CONTROLLERS

Device	SHDN	Pulse -by- Pulse I_{sense}	V_{IN} Range (VDC)	Output Type	Output Current (mA)	Freq (max) (kHz)	Operating/ Standby Current (mA)	Reference Voltage (V)	V_{ref} Tol (%)	Duty Cycle (max) (%)	UVLO	Description	Page No.
SG2524	Yes	No	8–40	Single Switch	100	500	NA/8	5	4	90	No	Voltage-Mode PWM	8–97
SG3524	Yes	No	8–40	Single Switch	100	500	NA/8	5	8	90	No	Voltage-Mode PWM	8–97
TL494	No	No	7–40	Single Switch	200	300	7.5/6	5	5	90	No	Voltage-Mode PWM	8–111
TL497A	Yes	No	4.5–12	Single Switch	500	50	11/6	1.2	5		No	Fixed On-Time Voltage-Mode	8–121
TL499A	No	No	1.1–35	Single Switch	500	40	1.8/NA	1.26	5		No	Fixed On-Time Voltage-Mode	8–129
TL594	No	No	7–40	Single Switch	200	300	12.4/9	5	1	90	Yes	Voltage-Mode PWM	8–137
TL598	No	No	7–40	Totem Pole	–250	300	15/NA	5	1	90	Yes	Voltage-Mode PWM	8–149
UC2842	No	Yes	30	Totem Pole	–200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8–159
UC2843	No	Yes	30	Totem Pole	–200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8–159
UC2844	No	Yes	30	Totem Pole	–200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8–159
UC2845	No	Yes	30	Totem Pole	–200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8–159
UC3842	No	Yes	30	Totem Pole	–200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8–159
UC3843	No	Yes	30	Totem Pole	–200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8–159
UC3844	No	Yes	30	Totem Pole	–200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8–159
UC3845	No	Yes	30	Totem Pole	–200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8–159
TL5001	No	No	3.6–40	Single Switch	20	400	1.1/1	1	5	100	Yes	Voltage-Mode PWM	8–79
TL5001A	No	No	3.6–40	Single Switch	20	400	1.1/1	1	3	100	Yes	Voltage-Mode PWM	8–79
LT1054	No	No	3.6–15	Totem Pole	±100	2000	3.5/3.1	1.25	2.5	100	Yes	Dual Channel-Mode PWM	8–171

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DC/DC CHARGE PUMP CONVERTERS

Device	SHDN	VO (typ) (V)	Tolerance (%)	V_{IN} Range (VDC)	Output Current (mA)	Freq (max) (kHz)	Quiescent Current (μA)	Shut-down Current (μA)	UVLO	Description	Page No.
TPS60100	Yes	3.3	±4	1.8–3.6	200	300	50	0.05	Yes	Charge Pump DC/DC Converter, 3.3-V	8–3
TPS60101	Yes	3.3	±4	1.8–3.6	100	300	50	0.05	Yes	Charge Pump DC/DC Converter, 3.3-V	8–23
TPS60110	Yes	5	±4	2.7–5.4	300	300	60	0.05	Yes	Charge Pump DC/DC Converter, 5-V	8–43
TPS60111	Yes	5	±4	2.7–5.4	150	300	60	0.05	Yes	Charge Pump DC/DC Converter, 5-V	8–61

MOSFET DRIVERS

Device	I_{CC} (μA)	Internal Regulator	Output Current (max) (A)	Rise/Fall Time (max) (ns)	Supply Voltage(s) (V)	Description	Page No.
TPS2811	5	Yes (8 – 40 V)	2	20	4–14	Dual Channel	9–3
TPS2812	5	Yes (8 – 40 V)	2	20	4–14	Dual Channel	9–3
TPS2813	5	Yes (8 – 40 V)	2	20	4–14	Dual Channel	9–3
TPS2814	5	No	2	20	4–14	Dual Channel	9–3
TPS2815	5	No	2	20	4–14	Dual Channel	9–3
TPS2816	150	Yes (8 – 40 V)	2	25	4–14	Active Pullup, Internal Regulator, Single Channel	9–31
TPS2817	150	Yes (8 – 40 V)	2	25	4–14	Active Pullup, Internal Regulator, Single Channel	9–31
TPS2818	25	Yes (8 – 40 V)	2	25	4–14	Single Channel	9–31
TPS2819	25	Yes (8 – 40 V)	2	25	4–14	Single Channel	9–31
TPS2828	25	No	2	25	4–14	Single Channel	9–31
TPS2829	25	No	2	25	4–14	Single Channel	9–31
TPS2830	1	No	2	50 / 85	4.5–15	Fast Synchronous-Buck With Deadtime Control	9–49
TPS2831	1	No	2	50 / 85	4.5–15	Fast Synchronous-Buck With Deadtime Control	9–49
TPS2832	1	No	2	50 / 85	4.5–15	Fast Synchronous-Buck With Deadtime Control	9–61
TPS2833	1	No	2	50 / 85	4.5–15	Fast Synchronous-Buck With Deadtime Control	9–61

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SUPERVISORY CIRCUITS

Device	V_{CC} (nom) (V)	V_t (V)	Tolerance (%)	I_{CC} (max) (mA)	V_{IN} (min) (V)	Over Voltage Sense	Comp Outputs	Number of SVS	WDI	Description	Page No.
TPS3123J12	1.2	1.08	2	0.03	0.75	No	No	1	Yes	Fixed Delay, Micropower	10–21
TPS3124J12	1.2	1.08	2	0.03	0.75	No	Yes	1	Yes	Fixed Delay, Micropower	10–21
TPS3125J12	1.2	1.08	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10–21
TPS3123G15	1.5	1.4	2	0.03	0.75	No	No	1	Yes	Fixed Delay, Micropower	10–21
TPS3124G15	1.5	1.4	2	0.03	0.75	No	Yes	1	Yes	Fixed Delay, Micropower	10–21
TPS3125G15	1.5	1.4	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10–21
TPS3123J18	1.8	1.62	2	0.03	0.75	No	No	1	Yes	Fixed Delay, Micropower	10–21
TPS3124J18	1.8	1.62	2	0.03	0.75	No	Yes	1	Yes	Fixed Delay, Micropower	10–21
TPS3125J18	1.8	1.62	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10–21
TPS3305–18	1.8	1.68	2	0.04	2.7	No	Yes	2	Yes	Fixed Delay, Micropower	10–33
TPS3307–18	1.8	1.68	2	0.04	2	No	Yes	3	No	Fixed Delay, Micropower	10–43
TLC7725	2.5	2.25	3	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10–9
TPS3707–25	2.5	2.25	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10–53
TPS3801J25	2.5	2.25	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–63
TPS3305–25	2.5	2.25	2	0.04	2.7	No	Yes	2	Yes	Fixed Delay, Micropower	10–33
TPS3809J25	2.5	2.25	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–3
TPS3820–25	2.5	2.25	1.8	0.025		No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3823–25	2.5	2.25	1.8	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3824–25	2.5	2.25	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3825–25	2.5	2.25	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3828–25	2.5	2.25	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3307–25	2.5	2.25	2	0.04	2	No	Yes	3	No	Fixed Delay, Micropower	10–43
TLC7703	3	2.63	2.7	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10–9
TPS3125L30	3	2.64	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10–21
TPS3705–30	3	2.63	2	0.05	2	No	No	1	Yes	Fixed Delay, Micropower	10–53
TPS3707–30	3	2.63	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10–53
TPS3801L30	3	2.64	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–63
TPS3809L30	3	2.64	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–3
TPS3820–30	3	2.63	1.5	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3823–30	3	2.63	1.5	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3824–30	3	2.63	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71

SUPERVISORY CIRCUITS (continued)

Device	V_{CC} (nom) (V)	V_t (V)	Tolerance (%)	I_{CC} (max) (mA)	V_{IN} (min) (V)	Over Voltage Sense	Comp Outputs	Number of SVS	WDI	Description	Page No.
TPS3825–30	3	2.63	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3828–30	3	2.63	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TLC7733	3.3	2.93	2.4	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10–9
TPS3705–33	3.3	2.93	2	0.05	2	No	No	1	Yes	Fixed Delay, Micropower	10–53
TPS3707–33	3.3	2.93	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10–53
TPS3801K33	3.3	2.93	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–63
TPS3809K33	3.3	2.93	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–3
TPS3820–33	3.3	2.93	1.7	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3823–33	3.3	2.93	1.7	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3824–33	3.3	2.93	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3825–33	3.3	2.93	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3828–33	3.3	2.93	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TL7705A	5	4.55	2	3	3.6	No	Yes	1	No	Programmable Delay	10–91
TL7705B	5	4.55	2	3	1	No	Yes	1	No	Programmable Delay	10–113
TL7757	5	4.55	3	2.5	1	No	No	1	No	No Delay	10–123
TL7759	5	4.55	3	2	1	No	Yes	1	No	No Delay	10–133
TLC7705	5	4.55	1.5	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10–9
TL7770–5	5	4.55	1	5	1	Yes	Yes	2	No	Programmable Delay	10–139
TPS3705–50	5	4.55	2	0.05	2	No	No	1	Yes	Fixed Delay, Micropower	10–53
TPS3707–50	5	4.55	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10–53
TPS3801I50	5	4.55	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–63
TPS3305–33	5	4.55	2	0.04	2.7	No	Yes	2	Yes	Fixed Delay, Micropower	10–33
TPS3809I50	5	4.55	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–3
TPS3820–50	5	4.55	1.3	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3823–50	5	4.55	1.3	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3824–50	5	4.55	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3825–50	5	4.55	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3828–50	5	4.55	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3307–33	5	4.55	2	0.04	2	No	Yes	3	No	Fixed Delay, Micropower	10–43
TL7709A	9	7.6	2	3	3.6	No	Yes	1	No	Programmable Delay	10–91

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SUPERVISORY CIRCUITS (continued)

Device	V_{CC} (nom) (V)	V_t (V)	Tolerance (%)	I_{CC} (max) (mA)	V_{IN} (min) (V)	Over Voltage Sense	Comp Outputs	Number of SVS	WDI	Description	Page No.
TL7712A	12	10.8	2	3	3.6	No	Yes	1	No	Programmable Delay	10–91
TL7770–12	12	10.9	1	5	1	Yes	Yes	2	No	Programmable Delay	10–139
TL7715A	15	13.5	2	3	3.6	No	Yes	1	No	Programmable Delay	10–91
TPS5510			3	1	4	Yes	Yes	3	No	Fixed Delay	10–79
TPS5511			3	1	4	Yes	Yes	3	No	Fixed Delay	10–85
TL7700	adj			0.016		No	Yes	1	No	Micropower, Programmable Delay	10–101
TL7702A	pgm	pgm	2	3	3.6	No	Yes	1	No	Programmable Delay	10–91
TL7702B	pgm	pgm	2	3	1	No	Yes	1	No	Programmable Delay	10–113
TLC7701	adj	1.1	5.4	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10–9

GENERAL PURPOSE DISTRIBUTION SWITCHES

Device	Number of FETs	$r_{DS(on)}$ (typ) (mΩ)	I_O (max) (A)	Current Limit (typ) (A)	V_{IN} Range (typ) (V)	Over Current Reporting	Over Temp Protection	Enable	Description	Page No.
TPS2010	1	75	0.2	0.4	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–25
TPS2010A	1	30	0.2	0.3	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–53
TPS2011	1	75	0.6	1.2	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–25
TPS2011A	1	30	0.6	0.9	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–53
TPS2012	1	75	1	2	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–25
TPS2012A	1	30	1	1.5	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–53
TPS2013	1	75	1.5	2.6	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–25
TPS2013A	1	30	1.5	2.2	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–53

V_{AUX} SWITCHES

Device	Number of Inputs	IN1 $r_{DS(on)}$ (typ) (mΩ)	IN2 $r_{DS(on)}$ (typ) (Ω)	IN1 Output Current (mA)	IN2 Output Current (mA)	IN1 Supply Current (typ) (uA)	IN2 Supply Current (typ) (uA)	IN1, IN2 Input Voltage Range (V)	Enable	Page No.
TPS2100	2	250	1.3	500	10	10	0.75	2.7 – 4.0	Neg	13–311
TPS2101	2	250	1.3	500	10	10	0.75	2.7 – 4.0	Pos	13–311

PCMCIA/CARDBUS DISTRIBUTION SWITCHES

Device	12-V Supply Required	3V/5V $r_{DS(on)}$ (typ) (mΩ)	Control Inputs	Current and Temperature Protection	VPP_Good and OC Reporting	Description	Page No.
TPS2205	No	110/140	8 Line Parallel	Yes	N/Y	Dual Channel	13–325
TPS2206	No	110/140	3 Line Serial w/Reset	Yes	N/Y	Dual Channel	13–349
TPS2211	No	50	4 Line Parallel	Yes	N/Y	Single Channel	13–375
TPS2212	No	160	4 Line Parallel	Yes	N/Y	Single Channel	13–395
TPS2214	No	60	3 Line Serial, w/independent VCC/VPP	Yes	N/Y	Dual Channel	13–413
TPS2216	No	60	3 Line Serial, w/independent VCC/VPP	Yes	N/Y	Dual Channel	13–437

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USB SWITCHES

Device	Number of FETs	$r_{DS(on)}$ (typ) (mΩ)	I_O (max) (A)	Current Limit (typ) (A)	V_{IN} Range (typ) (V)	Over Current Reporting	Over Temp Reporting	Enable	Description	Page No.
TPS2014	1	95	0.6	1.2	4.0 – 5.5	Yes	No	Neg	Current–Limited, UL Listed, USB	13–73
TPS2015	1	95	1	2	4.0 – 5.5	Yes	No	Neg	Current–Limited, USB	13–73
TPS2020	1		0.2	0.3	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, USB	13–93
TPS2021	1		0.6	0.9	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, USB	13–93
TPS2022	1		1	1.5	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, USB	13–93
TPS2023	1		1.5	2.2	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, USB	13–93
TPS2024	1		2	3	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, USB	13–93
TPS2030	1	30	0.2	0.3	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, USB	13–115
TPS2031	1	30	0.6	0.9	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, USB	13–115
TPS2032	1	30	1	1.5	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, USB	13–115
TPS2033	1	30	1.5	2.2	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, USB	13–115
TPS2034	1	30	2	3	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, USB	13–115
TPS2041	1	80	0.5	0.9	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, Nemko Recognized	13–137
TPS2042	2	80	0.5	0.9	2.7 – 5.5	Each	Yes	Neg	Current–Limited, Nemko Recognized	13–157
TPS2043	3	80	0.5	0.9	2.7 – 5.5	Each	Yes	Neg	Current–Limited, Nemko Recognized	13–179
TPS2044	4	80	0.5	0.9	2.7 – 5.5	Each	Yes	Neg	Current–Limited, Nemko Recognized	13–203
TPS2045	1	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, Nemko Recognized	13–227
TPS2046	2	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, Nemko Recognized	13–247
TPS2047	3	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, Nemko Recognized	13–267
TPS2048	4	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, Nemko Recognized	13–289
TPS2051	1	80	0.5	0.9	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, Nemko Recognized	13–137
TPS2052	2	80	0.5	0.9	2.7 – 5.5	Each	Yes	Pos	Current–Limited, Nemko Recognized	13–157
TPS2053	3	80	0.5	0.9	2.7 – 5.5	Each	Yes	Pos	Current–Limited, Nemko Recognized	13–179
TPS2054	4	80	0.5	0.9	2.7 – 5.5	Each	Yes	Pos	Current–Limited, Nemko Recognized	13–203
TPS2055	1	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, Nemko Recognized	13–227
TPS2056	2	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, Nemko Recognized	13–247
TPS2057	3	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, Nemko Recognized	13–267
TPS2058	4	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, Nemko Recognized	13–289

PMOS DISTRIBUTION SWITCHES

Device	Number of FETs	$r_{DS(on)}$ (typ) (mΩ)	V_{DS} (max) (V)	I_{DD} (max) (A)	ESD Circuitry	Description	Page No.
TPS1100	1	180	15	1.6	Yes	High–Side PMOS	13–3
TPS1101	1	90	15	2.3	Yes	High–Side PMOS	13–13
TPS1120	2	180	15	1.17	Yes	High–Side PMOS	13–23

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LED DRIVERS

Device	V_{ref} (V)	I_Z (min) (μA)	I_Z (max) (mA)	V_O (min) (V)	V_O (max) (V)	Tolerance (%)	V_I (max) (V)	Temp Coeff (typ) (ppm/°C)	Description	Page No.
TLC5904	2.5	1000	100	Vref	36	0.4	36	30	LED Driver	14–3

VOLTAGE RAIL SPLITTERS

Device	I_{CC} (μA)	V_{CC} (V)	I_O (mA)	V_O (min) (V)	V_O (max) (V)	Temp Coeff (typ) (ppm/°C)	Description	Page No.
TLE2426	280	4 – 40	20	1.98	20.2	25	Rail Splitter Precision Virtual Ground	15–3

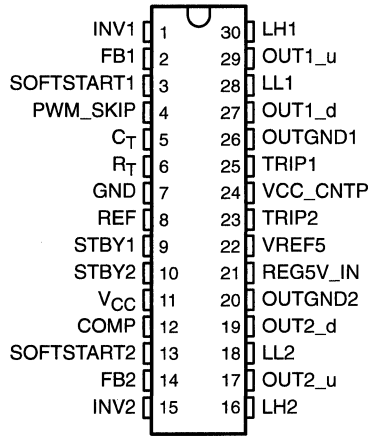
SPECIAL FUNCTIONS

Device	V_{ref} (V)	I_Z (min) (μA)	I_Z (max) (μA)	V_O (min) (V)	Input Clamp Current (mA)	Settling Time (μs)	Description	Page No.
TL7726	4.5		60		25	30	Hex Clamping Circuit	16–3
TL2218–285		–20.5		2.5			Excalibur Current-Mode SCSI Terminator	16–7

7 Processor PS Controllers

- **Dual, Step-Down for Notebook System Power**
- **4.5 V to 25 V Input Voltage Range**
- **Adjustable Output Voltage**
- **95% Efficiency Achievable**
- **PWM/Skip Mode Control Maintains High Efficiency Under Light Load Conditions**
- **Fixed-Frequency Operation**
- **Resistorless Current Protection**
- **Fixed High-Side Driver Voltage**
- **Low Quiescent Current (0.6 mA, <1 μA for Standby)**
- **Small 30-Pin TSSOP**
- **EVM Available (TPS5102EVM-135)**

DBT PACKAGE
(TOP VIEW)

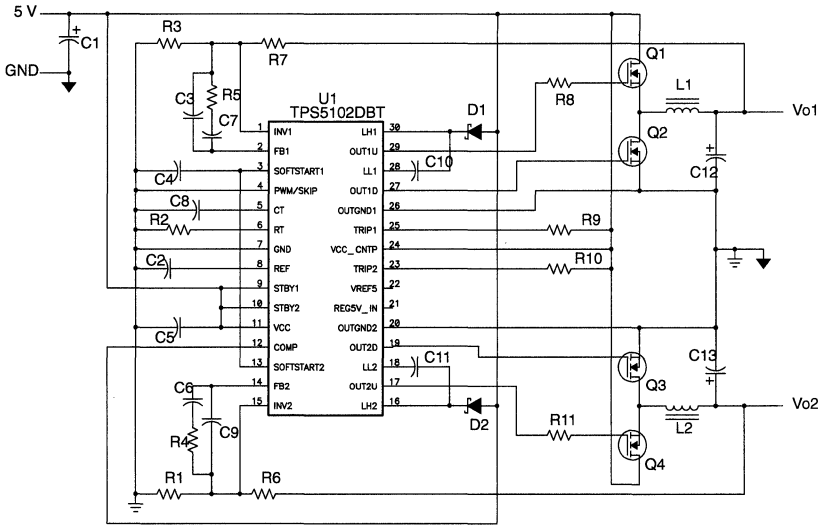


description

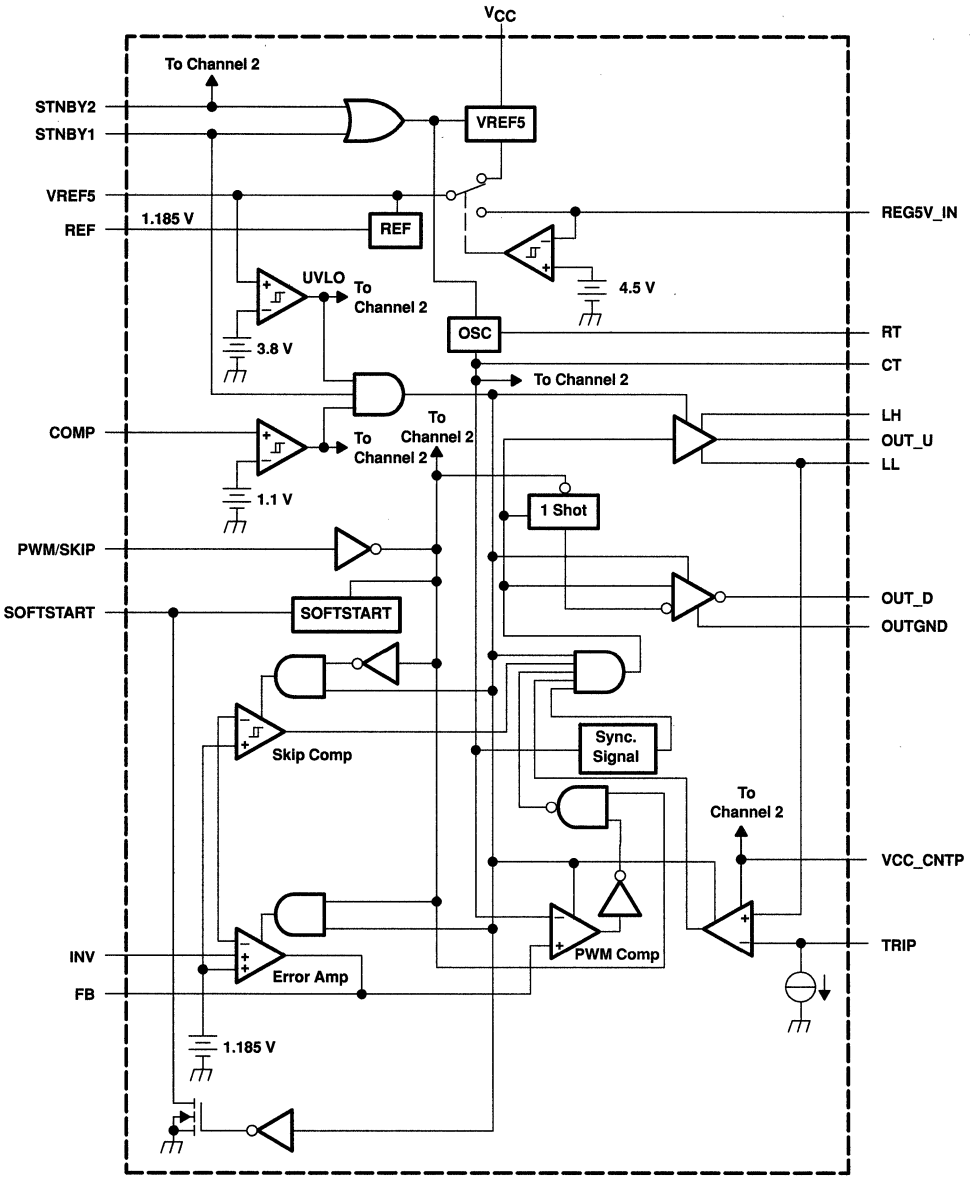
The TPS5102 is a dual, high efficiency controller designed for notebook system power requirements. Under light load conditions, high efficiency is maintained as the controller switches from the PWM mode to the lower frequency Skip mode.

These two operating modes, along with the synchronous-rectifier drivers, dead-time, and very low quiescent current, allow power to be conserved and the battery life extended, under all load conditions.

The resistor-less current protection and fixed high-side driver voltage simplify the system design and reduce the external parts count. The wide input voltage range and adjustable output voltages allow flexibility for using the TPS5102 in notebook power supply applications.



functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE	EVM
	TSSOP(DBT)	
–40°C to 85°C	TPS5102IDBT	TPS5102EVM-135
	TPS5102IDBTR	

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
COMP	12	I/O	Voltage monitor comparator input
C_T	5	I/O	External capacitor connection for switching frequency adjustment
FB1	2	O	CH1 error amp output
FB2	14	O	CH2 error amp output
GND	7		Control GND
INV1	1	I	CH1 inverting input
INV2	15	I	CH2 inverting input
LH1	30	I/O	CH1 boost capacitor connection
LH2	16	I/O	CH2 boost capacitor connection
LL1	28	I/O	CH1 boost circuit connection
LL2	18	I/O	CH2 boost circuit connection
OUT1_d	27	I/O	CH1 low-side gate-drive output
OUT2_d	19	O	CH2 low-side gate-drive output
OUT1_u	29	O	CH1 high-side drive output
OUT2_u	17	O	CH2 high-side drive output
OUTGND1	26		Output GND 1
OUTGND2	20		Output GND 2
PWM_SKIP	4	I	PWM/SKIP mode select L:PWM mode H:SKIP mode
REF	8	O	1.185-V reference voltage output
REG5V_IN	21	I	External 5-V input
R_T	6	I/O	External resistor connection for switching frequency adjustment
SOFTSTART1	3	I/O	External capacitor connection for CH1soft start timing.
SOFTSTART2	13	I/O	External capacitor connection for CH2 soft start timing.
STBY1	9	I	CH1 stand-by control
STBY2	10	I	CH2 stand-by control
TRIP2	23	I	External resistor connection for CH2 over current protection.
TRIP1	25	I	External resistor connection for CH1 over current protection.
V_{CC}	11		Supply voltage input
$V_{ref}5$	22	O	5-V internal regulator output
VCC_CNTP	24	I	Supply voltage sense input

detailed description

Vref (1.185 V)

The reference voltage is used to set the output voltage and the overvoltage protection (COMP).

Vref5 (5 V)

The internal linear voltage regulator is used for the high-side driver bootstrap voltage. Since the input voltage range is from 4.5 V to 25 V, this feature offers a fixed voltage for the bootstrap voltage greatly simplifying the drive design. It is also used for powering the low side driver. The tolerance is 6%.

5-V Switch

If the internal 5 V switch senses a 5-V input from REG5V_IN pin, the internal 5-V linear regulator will be disconnected from the MOSFET drivers. The external 5 V will be used for both the low-side driver and the high side bootstrap, thus increasing the efficiency.

PWM/SKIP

This pin is used to change between PWM and Skip mode. If the pin is lower than 0.5-V, the IC is in regular PWM mode; if a minimum 2-V is applied to this pin, the IC works in Skip mode. In light load condition (<0.2 A), the skip mode gives a short pulse to the low-side FET instead of a full pulse. By this control, switching frequency is lowered, reducing switching loss; also the output capacitor energy discharging through the output inductor and the low-side FET is prevented. Therefore, the IC can achieve high efficiency at light load conditions (< 0.2 A).

err-amp

Each channel has its own error amplifier to regulate the output voltage of the synchronous-buck converter. It is used in the PWM mode for the high output current condition (>0.2A). Voltage mode control is applied.

skip comparator

In Skip mode, each channel has its own hysteretic comparator to regulate the output voltage of the synchronous-buck converter. The hysteresis is set internally and typically at 8.5 mV. The delay from the comparator input to the driver output is typically 1.2 µs.

low-side driver

The low-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The maximum drive voltage is 5 V from Vref5. The current rating of the driver is typically 1 A, source and sink.

high-side driver

The high side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 1 A, source and sink. When configured as a floating driver, the bias voltage to the driver is developed from Vref5, limiting the maximum drive voltage between OUT_u and LL to 5 V. The maximum voltage that can be applied between LHx and OUTGND is 30 V.

deadtime control

Deadtime prevents shoot–through current from flowing through the main power FETs during switching transitions by actively controlling the turn-on time of the MOSFETs drivers. The typical deadtime from low-side-driver-off to high-side-driver-on is 70 ns, and 85 ns from high-side-driver-off to low-side-driver-on.

detailed description (continued)

current protection

Current protection is achieved by sensing the high-side power MOSFET drain-to-source voltage drop during on-time at VCC_CNTP and LL. An external resistor between Vin and TRIP pin in serial with the internal current source adjusts the current limit. When the voltage drop during the on-time is high enough, the current comparator triggers the current protection and the circuit is reset. The reset repeats until the over-current condition is removed.

COMP

COMP is an internal comparator used for any voltage protection such as the output under-voltage protection for notebook power applications. If the core voltage is lower than the setpoint, the comparator turns off both channels to prevent the notebook from damage.

SOFT1, SOFT2

Separate softstart terminals make it possible to set the start-up time of each output for any possibility.

STBY1, STBY2

Both channels can be switched into standby mode separately by grounding the STBY pin. The standby current is as low as 1 μA.

ULVO

When the input voltage goes up to about 4 V, the IC is turned on, ready to function. When the input voltage is lower than the turn-on value, the IC is turned off. The typical hysteresis is 40 mV.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, Vcc (see Note 1) ..... -0.3 V to 27 V
Input voltage, INV ..... -0.3 V to 7 V
SOFTSTART ..... -0.3 V to 7 V
COMP ..... -0.3 V to 6 V
REG5_IN ..... -0.3 V to 6 V
STBY ..... -0.3 V to 15 V
Driver current ..... 3 A
TRIP ..... -0.3 V to 27 V
C_T ..... -0.3 V to 7 V
R_T ..... -0.3 V to 7 V
LL ..... -0.3 V to 27 V
LH ..... -0.3 V to 32 V
OUT_u ..... -0.3 V to 32 V
OUT_d ..... -0.3 V to 7 V
PWM/SKIP ..... -0.3 V to 7 V
VCC_Sense ..... -0.3 V to 27V
Power dissipation (T_A = 25°C) ..... 874 mW
Operating temperature (T_A) ..... -40°C to 85°C
Operating temperature (T_J) ..... -40°C to 125°C
Storage temperature (T_{STG}) ..... -55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. This rating is specified at duty ≤ 10% on output rise and fall each pulse. Each pulse width (rise and fall) for the peak current should not exceed 2 µs.
3. See Dissipation Rating Table for free-air temperature range above 25°C.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
DBT	874 mW	6.993 mW/°C	454 mW

recommended operating conditions

PARAMETERS			MIN	NOM	MAX	UNIT
Supply voltage, Vcc			4.5		25	V
Input voltage, V_I		INV1/2 C_T R_T, PWM/SKIP, SOFTSTART			6	V
		5 V_IN	-0.1		5.5	
		STBY1, STBY2			12	
		TRIP1/2 VCC_SENSE	-0.1		25	
Oscillator frequency	C_T			100		pF
	R_T			82		kΩ
	f_{osc}	PWM		200		KHz
Operation temperature range, T_A			-40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 7 V (unless otherwise noted)

reference voltage

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vref	Reference voltage	T_A = 25°C, I_{vref} = 50 µA	1.167	1.185	1.203	V
		I_{vref} = 50 µA	1.155		1.215	
Regin	Line regulation	Vcc = 4.5, 25V, I = 50 µA		0.2	12	mV
Regl	Load regulation	I = 0.1 µA to 1 mA		0.5	10	mV

quiescent current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Icc	Operating current without switching	Both STBY > 2.5 V, No switching, Vin = 4.5 – 25 V		0.6	1.5	mA
Iccs	Stand-by current	Both STBY < 0.5 V, Vin = 4.5 – 25 V		1	1000	nA

oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
fosc	Frequency	PWM operation			500	kHz
R_T	Timing resistor		56			kΩ
fdv	fosc change	Vcc = 4.5 V to 25 V		0.1%		
fdt		T_A = -40°C to 85°C		2%		
V_{oscH}	H-level output voltage	DC, includes internal comparator error	1	1.1	1.2	V
		Fosc = 200 kHz, Includes internal comparator error		1.17		
V_{oscL}	L-level output voltage	Includes internal comparator error	0.4	0.5	0.6	V
		Fosc = 200 kHz, Includes internal comparator error		0.43		

error amp

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vio	Input offset voltage	T_A = 25°C		±2	±10	mV
Av	Open-loop voltage gain		50			dB
GB	Unity-gain bandwidth			0.8		MHz
Isnk	Output sink current	Vo = 0.4 V	30	45		µA
Isrc	Output source current	Vo = 1 V		300		µA

skip comparator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vhys†	Hysteresis window		6	9.5	13	mV
Vhoff	Offset voltage			2		mV
Ihbias	Bias current			10		pA
T_{LHT}	Propagation delay‡ from INV to OUTxU	TTL input signal		0.7		µs
T_{LH}		10 mV overdrive on hysteresis band signal		1.2		µs

† Vhys is assured by design.
‡ The total delay in the table includes the driver delay.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 7 V (unless otherwise noted) (continued)

driver deadtime

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{DRVLH}	Low side to high side			70		nS
T_{DRVHL}	High side to low side			85		nS

standby

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	H-level input voltage	STBY1, STBY2	2.5			V
V_{IL}	L-level input voltage				0.5	
T_{turnon}	Propagation delay	STBY to driver output		1.5		µs
$T_{turnoff}$	Propagation delay			1.8		

5V regulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	I = 10 mA	4.7		5.3	V
Regin	Line regulation	Vcc = 5.5 V, 25 V, I = 10 mA			20	mV
Regl	Load regulation	I = 1 V, 10 mA, Vcc = 5.5 V			40	mV
Ios	Short-circuit output current	Vref = 0 V		80		mA

5-V internal switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TLH}	Threshold voltage		4.2		4.8	V
V_{THL}			4.1		4.7	V
V_{hys}	Hysteresis		30		150	mV

UVLO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TLH}	Threshold voltage		3.7		4.2	V
V_{THL}			3.6		4.1	V
V_{hys}	Hysteresis		10	40	150	mV

current limit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal current source		PWM mode	10	15	20	µA
		Skip mode	3	5	7	
Input offset voltage				2.5		mV

driver output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT_u sink current	Vo = 3 V	0.5	1.2		A
OUT_d sink current		0.5	1.2		
OUT_u source current	Vo = 3 V	–1	–1.7		A
OUT_d source current		–1	–1.5		

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 7 V (unless otherwise noted) (continued)

softstart

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CTRL}	Soft-start current		1.8	2.5	3	µA
	Maximum discharge current			0.92		mA
V_{TLH}	Threshold voltage (skip mode)		3.4	3.9	4.7	V
V_{THL}			1.8	2.6	3.4	

output voltage protection (COMP)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Threshold voltage		0.9	1.1	1.3	V
	Progagation delay†, 50% duty cycle, No capacitor on COMP or OUT_u pin, Frequency = 200 kHz	Turnon		900		ns
		Turnoff (with channel on)		400		ns

† The delay time in the table includes the driver delay.

PWM/SKIP

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Threshold	High to low			0.5	V
		Low to high	2			
	Delay	High to low		550		ns
		Low to high		400		

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT (BOTH CHANNELS ON)
vs
INPUT VOLTAGE

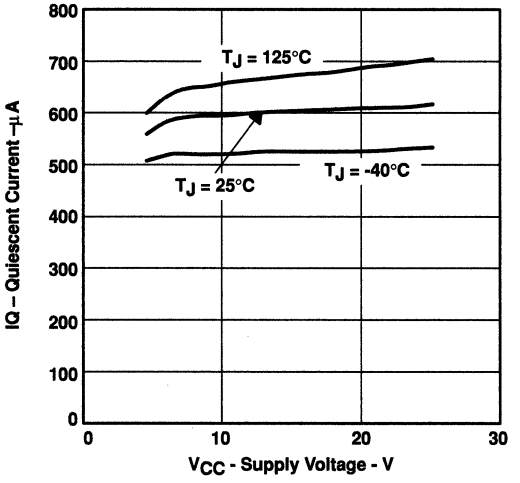


Figure 1

QUIESCENT CURRENT (BOTH CHANNELS STANDBY)
vs
INPUT VOLTAGE

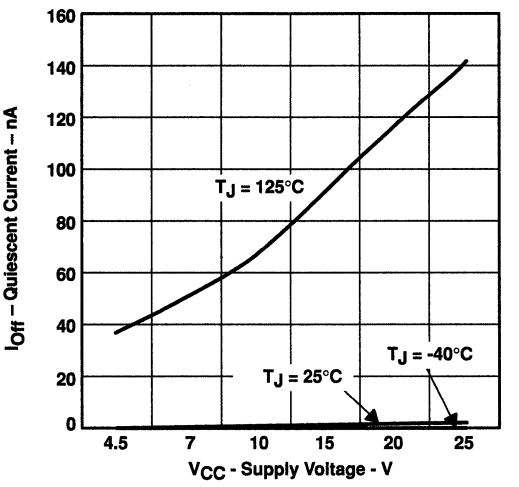


Figure 2

DRIVE CURRENT (SOURCE)
vs
DRIVE VOLTAGE

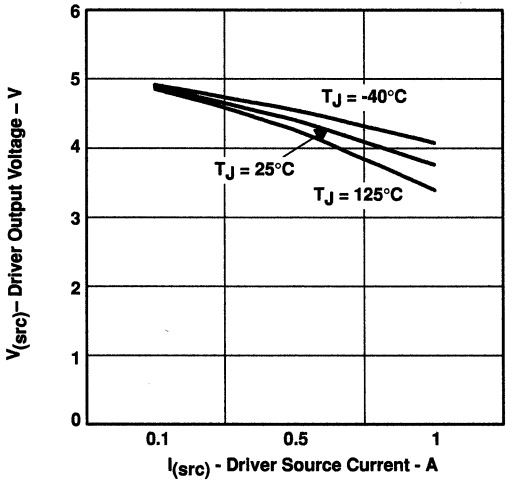


Figure 3

DRIVE CURRENT (SINK)
vs
DRIVE VOLTAGE

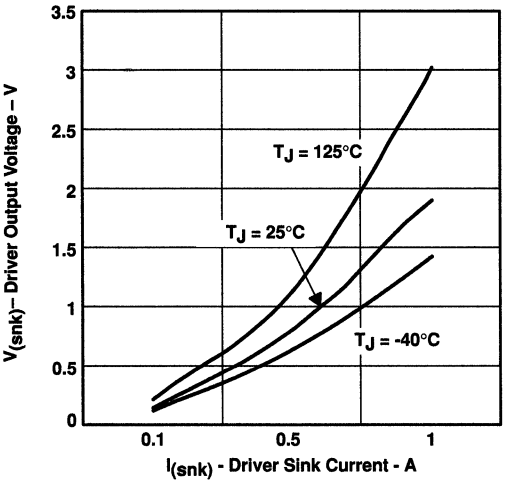


Figure 4

TYPICAL CHARACTERISTICS

CURRENT PROTECTION SOURCE CURRENT
(SKIP MODE)
vs
INPUT VOLTAGE

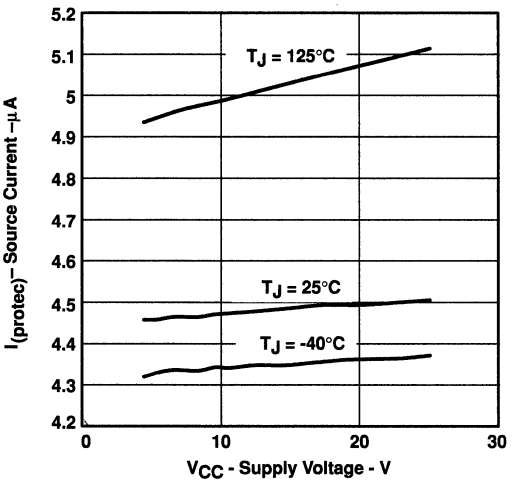


Figure 5

CURRENT PROTECTION SOURCE CURRENT
(PWM MODE)
vs
INPUT VOLTAGE

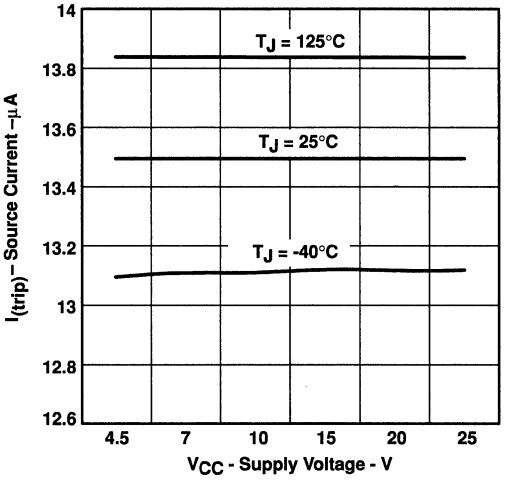


Figure 6

PWM/SKIP THRESHOLD VOLTAGE
vs
INPUT VOLTAGE

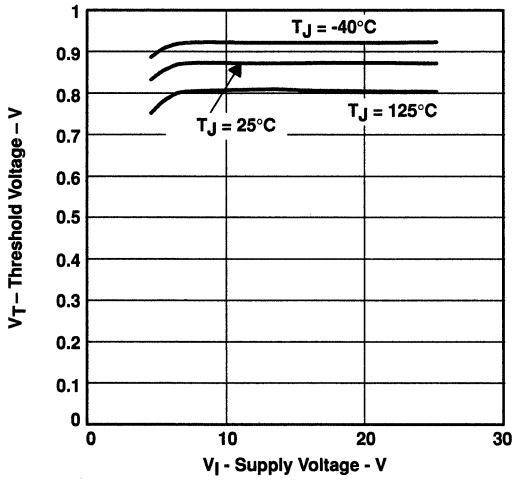


Figure 7

V_{ref5} VOLTAGE
vs
CURRENT

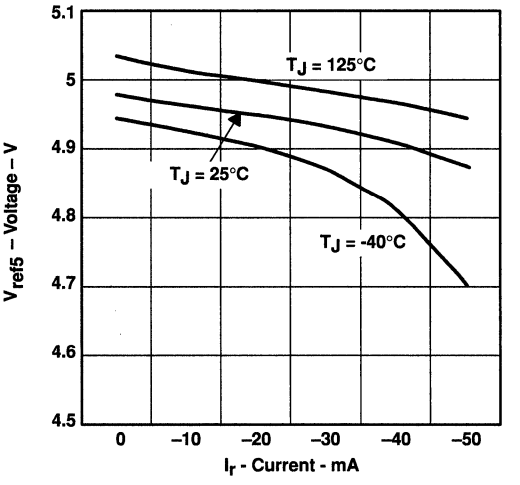


Figure 8

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT VOLTAGE
vs
SWITCHING FREQUENCY

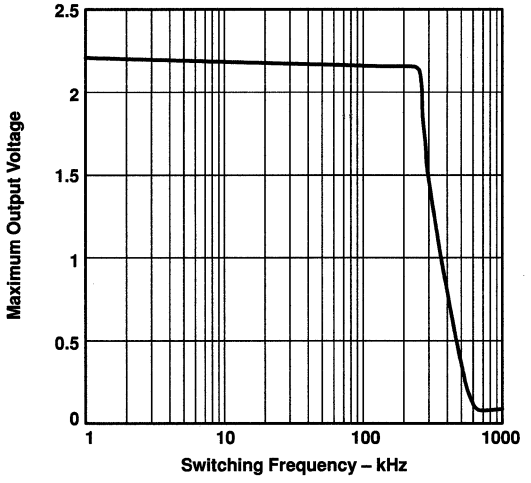


Figure 9

SOFT START CHARGE CURRENT
vs
JUNCTION TEMPERATURE

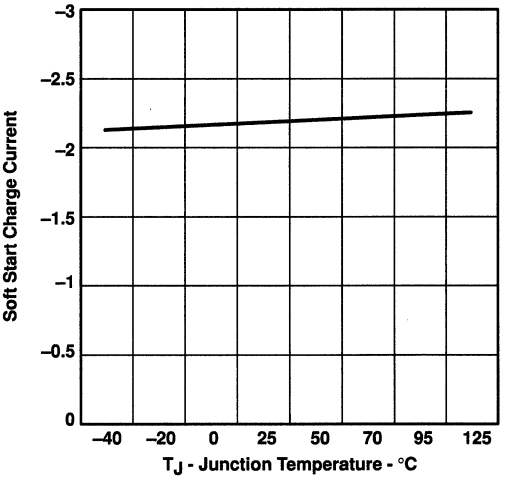


Figure 10

SWITCHING FREQUENCY
vs
TIMING RESISTOR

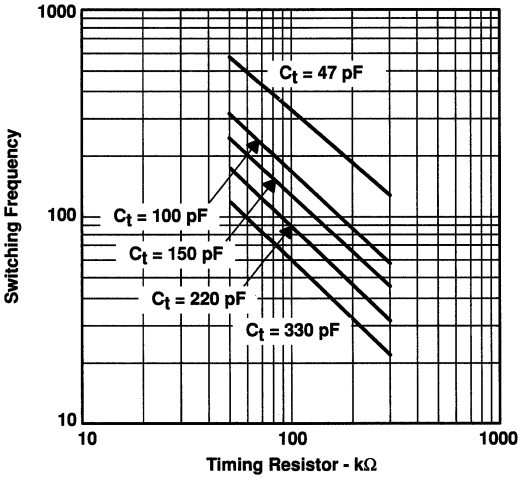
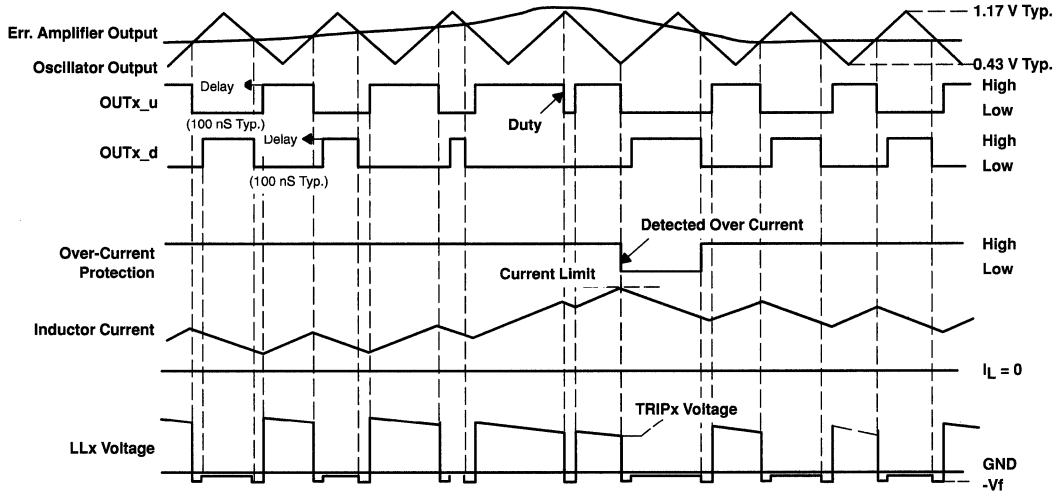


Figure 11

TYPICAL CHARACTERISTICS

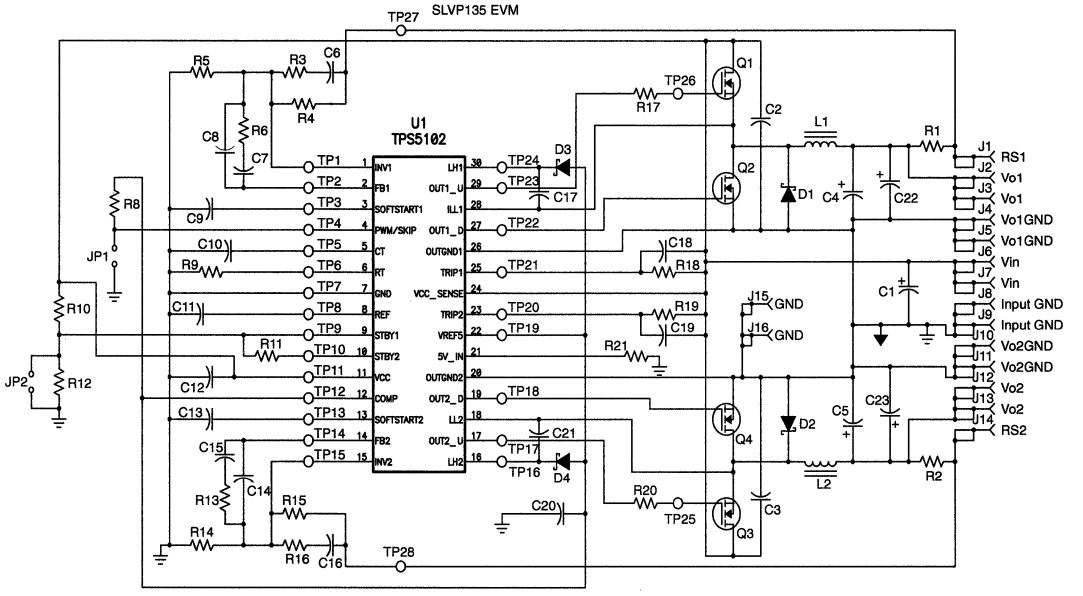
timing diagram



APPLICATION INFORMATION

The design shown in this application report is a reference design for notebook applications. An evaluation module (EVM), TPS5102EVM-135 (SLVP135), is available for customer testing and evaluation. The intent is to allow a customer to fully evaluate the given design using the plug-in EVM supply shown here. For subsequent customer board revisions, the EVM design can be copied onto the users' PCB to shorten design cycle.

The following key design procedures will aid in the design of the notebook power supply using the TPS5102:



Vin	Iin	Vo1	Io1	Vo2	Io2
6 V to 15 V	6 A	3.3 V	4 A	5 V	4 A
16 V to 25 V		3.3 V	2.5 A	5 V	2.5 A

output voltage setpoint calculation

The output voltage is set by the reference voltage and the voltage divider. In the TPS5102, the reference voltage is 1.185-V, and the divider is composed of two resistors in the EVM design that are R4 and R5, or R14 and R15. The equation for the setpoint is:

$$R2 = \frac{R1 \times Vr}{Vo - Vr}$$

Where R1 is the top resistor (kΩ) (R4 or R15); R2 is the bottom resistor (kΩ) (R5 or R14); Vo is the required output voltage (V); Vr is the reference voltage (1.185 V in TPS5102).

Example: R1 = 1 kΩ; Vr = 1.185 V; Vo = 3.3 V, then R2 = 560 Ω.

Some of the most popular output voltage setpoints are calculated in the table below:

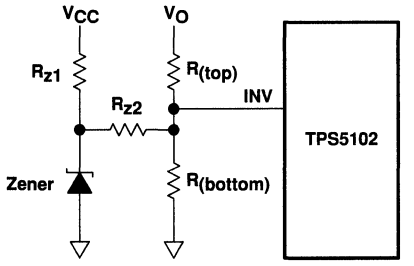
V_O	1.3 V	1.5 V	1.8 V	2.5 V	3.3 V	5 V
R1 (top) (kΩ)	1 V	1 V	1 V	1 V	1 V	1 V
R2 (bottom) (kΩ)	10 V	3.7 V	1.9 V	0.9 V	0.56 V	0.31 V

APPLICATION INFORMATION

output voltage setpoint calculation (continued)

If a higher precision resistor is used, the voltage setup can be more accurate.

In some applications, the output voltage is required to be lower than the reference voltage. With a few extra components, the lower voltage can be easily achieved. The drawing below shows the method.



In the schematic, the Rz1, the Rz2, and the zener are the extra components. Rz1 is used to give the zener enough current to build up the zener voltage. The zener voltage is added to INV through Rz2. Therefore, the voltage on the INV is still equal to the IC internal voltage (1.185 V) even if the output voltage is regulated at a lower setpoint. The equation for setting up the output voltage is shown below:

$$Rz\,2 = \frac{(Vz - Vr)}{\frac{(Vr - Vo)}{Rtop} + \frac{Vr}{Rbtm}}$$

When Rz2 is the adjusting resistor for low output voltage; Vz is the zener voltage; Vr is the internal reference voltage; Rtop is the resistor of the voltage sensing network; Rbtm is the bottom resistor of the sensing network;V_O is the required output voltage setpoint.

Example: Assuming the required output voltage setpoint is V_O = 0.8 V, V_Z = 5 V; Rtop = 1 kΩ; Rbottom = 1 kΩ, Then the Rz2 = 2.43 kΩ.

output inductor ripple current

The output inductor current ripple can affect not only the efficiency, but also the output voltage ripple. The equation is exhibited below:

$$Iripple = \frac{Vin - Vout - Iout \times (Rdson + R_L)}{Lout} \times D \times Ts$$

Where *Iripple* is the peak-to-peak ripple current (A) through the inductor; *Vin* is the input voltage (V); *Vout* is the output voltage (V); *Iout* is the output current; *Rdson* is the on-time resistance of MOSFET (Ω); *D* is the duty cycle; and *Ts* is the switching cycle (S). From the equation, it can be seen that the current ripple can be adjusted by changing the output inductor value.

Example: Vin = 5 V; Vout = 1.8 V; Iout = 5 A; Rdson = 10 mΩ; RL = 5 mΩ; D = 0.36; Ts = 10 µS; Lout = 6 µH

Then, the ripple Iripple = 2 A.

APPLICATION INFORMATION

output capacitor RMS current

Assuming the inductor ripple current totally goes through the output capacitor to ground, the RMS current in the output capacitor can be calculated as:

$$Iorms = \frac{\Delta I}{\sqrt{12}}$$

Where *Io(rms)* is the maximum RMS current in the output capacitor (A); ΔI is the peak-to-peak inductor ripple current (A).

Example: ΔI = 2 A, so Io(rms) = 0.58 A

input capacitor RMS current

Assuming the input ripple current totally goes into the input capacitor to the power ground, the RMS current in the input capacitor can be calculated as:

$$Iirms = \sqrt{Io^2 \times D \times (1-D) + \frac{1}{12} D \times Iripple^2}$$

Where *Ii(rms)* is the input RMS current in the input capacitor (A); *Io* is the output current (A); Iripple is the peak-to-peak output inductor ripple current; *D* is the duty cycle. From the equation, it can be seen that the highest input RMS current usually occurs at the lowest input voltage, so it is the worst case design for input capacitor ripple current.

Example: Io = 5 A; D = 0.36; Iripple = 2 A,

Then, Ii(rms) = 2.42 A

soft-start

The soft-start timing can be adjusted by selecting the soft-start capacitor value. The equation is

$$C_{soft} = 2 \times T_{soft}$$

Where C_{soft} is the soft-start capacitance (μF) (C9 or C13 in EVM design); T_{soft} is the start-up time (S).

Example: Tsoft = 5 mS, so Csoft = 0.01 μF.

APPLICATION INFORMATION

current protection

The current limit in TPS5102 on each channel is set using an internal current source and an external resistor (R18 or R19). The sensed high side MOSFET drain-to-source voltage drop is compared to the set point, if the voltage drop exceeds the limit, the internal oscillator is activated, and it continuously reset the current limit until the over-current condition is removed. The equation below should be used for calculating the external resistor value for current protection setpoint:

$$Rcl = \frac{Rds(on) \times (Itrip + Iind(p\text{-}p)/2)}{0.000015}$$

In skip mode,

$$Rcl = \frac{Rds(on) \times (Itrip + Iind(p\text{-}p)/2)}{0.000005}$$

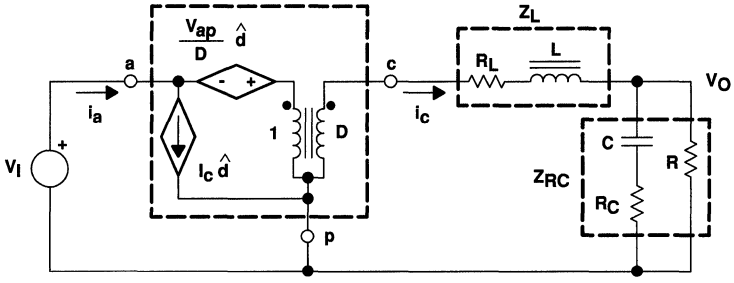
Where Rcl is the external current limit resistor (R10 or R11); Rds(on) is the high side MOSFET (Q1 or Q3) on-time resistance. Itrip is the required current limit; Iind(p-p) is the peak-to-peak output inductor current.

Example for voltage mode: Rds(on) = 10 mΩ, Itrip = 5 A, Iind = 2 A, so Rcl = 4 kΩ.

loop-gain compensation

Voltage mode control is used in this controller for the output voltage regulation. To achieve fast, stabilized control, two parts are discussed in this section: the power stage small signal modeling and the compensation circuit design.

For the buck converter, the small signal modeling circuit is shown below:



From this equivalent circuit, several control transfer functions can be derived: input-to-output, output impedance, and control-to-output. Typically the control-to-output transfer function is used for the feedback control design.

Assuming Rc and RL are much smaller than R, the simplified small signal control-to-output transfer function is:

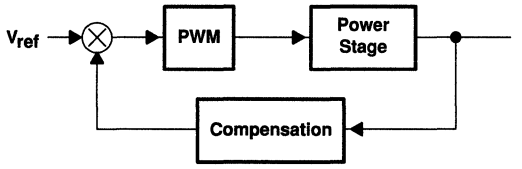
$$Vod = \frac{\hat{Vo}}{\hat{d}} = \frac{(1 + sCRc)}{1 + s\left[C \times \left(Rc + R_L\right) + \frac{L}{R}\right] + s^2LC}$$

Where C is the output capacitance; Rc is the equivalent serial resistance (ESR) in the output capacitor; L is the output inductor; RL is the equivalent serial resistance (DCR) in the output inductor; R is the load resistance.

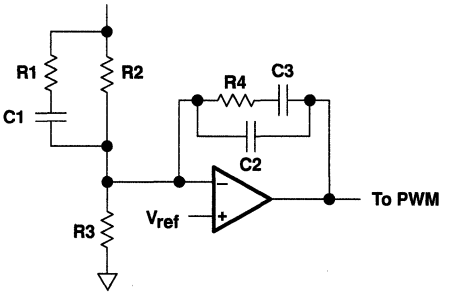
APPLICATION INFORMATION

loop-gain compensation (continued)

To achieve fast transient response and the better output voltage regulation, a compensation circuit is added to improve the feedback control. The whole system is shown:



The typical compensation circuit used as an option in the EVM design is a part of the output feedback circuit. The circuitry is displayed below:



This circuit is composed of one integrator, two poles, and two zeros:

Assuming R1 << R2 and C2 << C3, the equation is:

$$Comp = \frac{(1 + sC3R4) \times (1 + sC2R2)}{sC3R2(1 + sC2R4)\ (1 + sC1R1)}$$

Therefore,

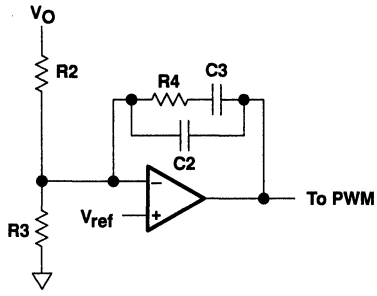
$$Pole1 = \frac{1}{2\pi C1R1} \qquad Zero1 = \frac{1}{2\pi C2R2}$$

$$Pole2 = \frac{1}{2\pi C2R4} \qquad Zero2 = \frac{1}{2\pi C3R4} \qquad Integrator = \frac{1}{2\pi C3R2}$$

A simplified version used in the EVM design is exhibited below:

APPLICATION INFORMATION

loop-gain compensation (continued)



Assuming C2 << C3, the equation is:

$$Comp = \frac{(1 + sC3R4)}{sC3R2(1 + sC2R4)}$$

There is one pole, one zero and one integrator:

$$Zero = \frac{1}{2\pi C3R4} \qquad Integrator = \frac{1}{2\pi fC3R2} \qquad Pole = \frac{1}{2\pi C2R4}$$

The loop-gain concept is used to design a stable and fast feedback control. The loop-gain equation is derived by the control-to-output transfer function times the compensation:

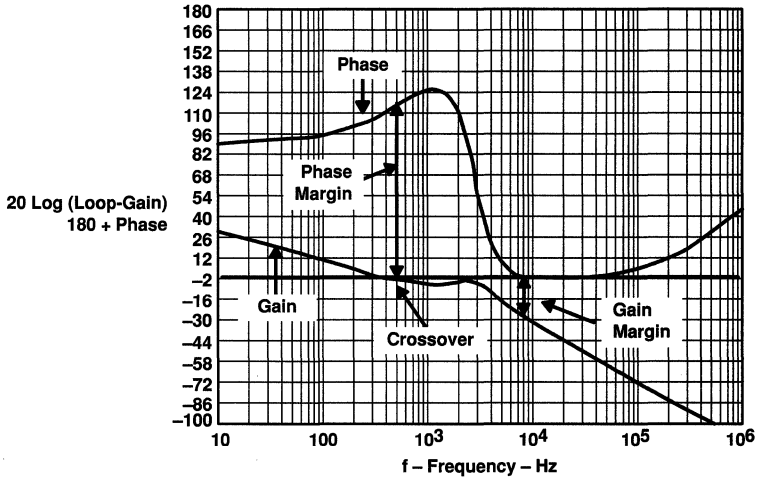
$$Loop\text{–}gain = Vod \times Comp$$

The amplitude and the phase of this equation can be drawn with software such as MathCad. In turn, the stability can be easily designed by adjusting the compensation parameters. The sample bode plot is shown below to explain the phase margin, gain margin, and the crossover frequency.

The gain is drawn as 20 log (loop-gain), and the phase is in degrees. To explain them clearer, 180 degrees is added to the phase, so that the gain and phase share the same zero.

The crossover frequency is the point at which the gain curve touches zero. The higher this frequency, the faster the transient response, since the transient recovery time is 1/(crossover frequency). The phase is the phase margin. The phase margin should be at least 60 degrees to cover all changes such as temperature. The gain margin is the gap between the gain curve and the zero when the phase curve touches zero. This margin should be at least 20 dB to guarantee stability over all conditions.

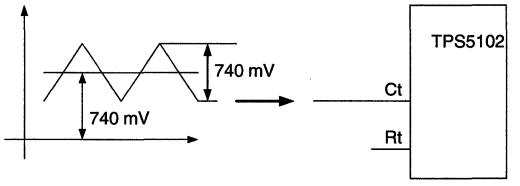
APPLICATION INFORMATION



synchronization

Some applications require switching clock synchronization. There are two methods that can be used for synchronization: the triangle wave synchronization and the square wave synchronization.

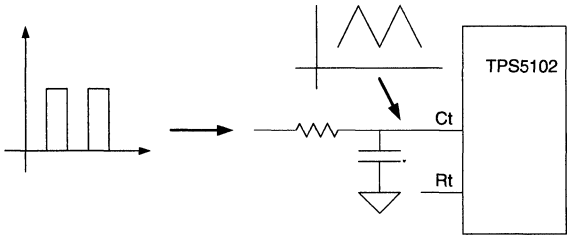
The triangle wave synchronization is displayed below:



It can be seen that both Rt and Ct are removed from the circuit. Therefore, two components are saved. This method is good for the synchronization between two controllers. If the controller needs to be synchronized with a digital circuit such as DSP, the square-type clock signal is usually used. The configuration exhibited below is for this type of application:

APPLICATION INFORMATION

synchronization (continued)



An external resistor is added into the circuit, but Rt is still removed. Ct is kept to be a part of RC circuit generating triangle waveform for the controller. Assuming the peak value of the square is known, the resistor and the capacitor can be adjusted to achieve the correct peak-to-peak value and the offset value.

layout guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, parallel the low-level components. Below are several specific points to consider *before* the layout of a TPS5102 design begins.

- All sensitive analog components should be referenced to ANAGND. These include components connected to Vref5, Vref, INV, LH, and COMP.
- Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.
- Connections from the drivers to the gate of the power FETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
- The bypass capacitor for V_{CC} should be placed close to the TPS5102.
- When configuring the high-side driver as a floating driver, the connection from LL to the power FETs should be as short and as wide as possible.
- When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from LH to LL) should be placed close to the TPS5102.
- When configuring the high-side driver as a ground-referenced driver, LL should be connected to DRVGND.
- The bulk storage capacitors across V_{In} should be placed close to the power FETS. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
- High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
- LH and LL should be connected very close to the drain and source, respectively, of the high-side FET. LH and LL should be routed very close to each other to minimize differential-mode noise coupling to these traces.
- The output voltage sensing trace should be isolated by either ground trace or Vcc trace.

APPLICATION INFORMATION

PWM AND SKIP MODE EFFICIENCY COMPARISON

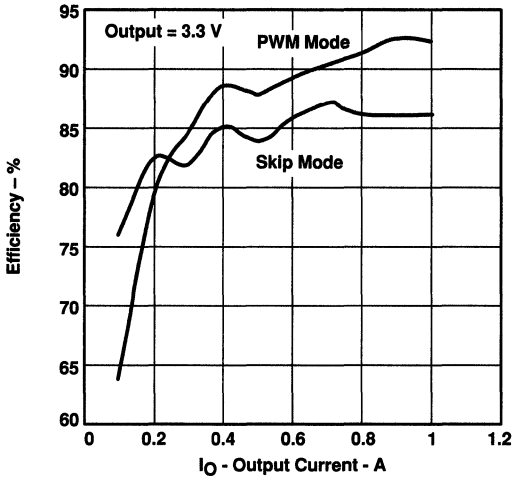


Figure 12

PWM AND SKIP MODE EFFICIENCY COMPARISON

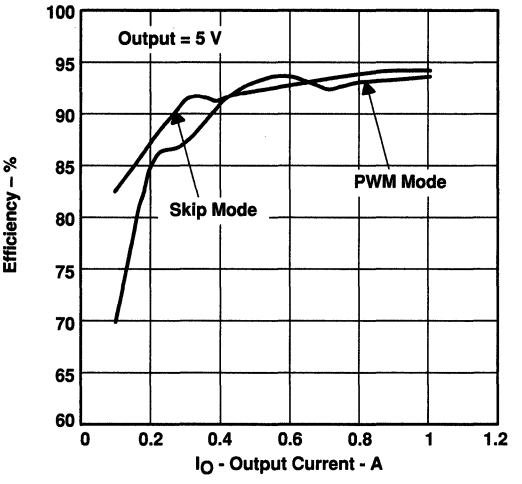


Figure 13

EFFICIENCY vs OUTPUT CURRENT

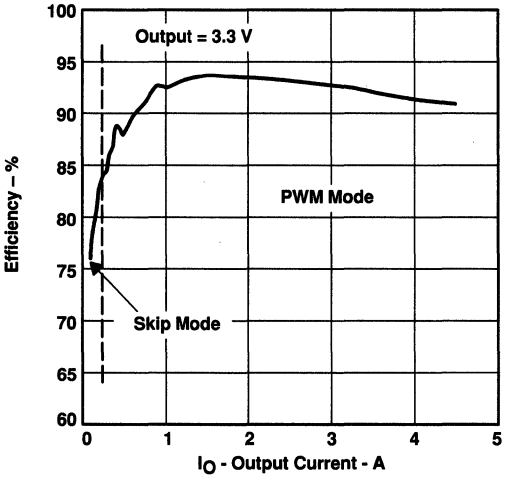


Figure 14

EFFICIENCY vs OUTPUT CURRENT

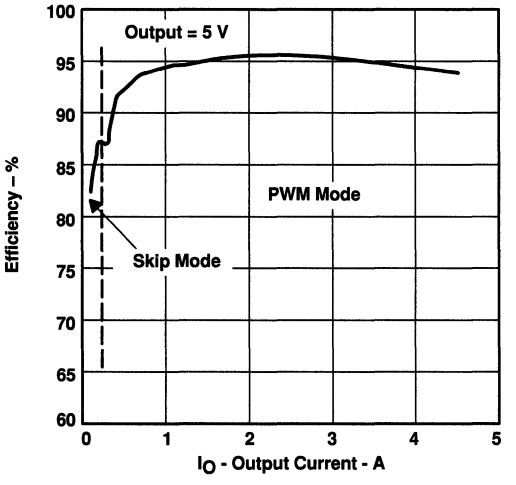


Figure 15

APPLICATION INFORMATION

EFFICIENCY
vs
OUTPUT CURRENT

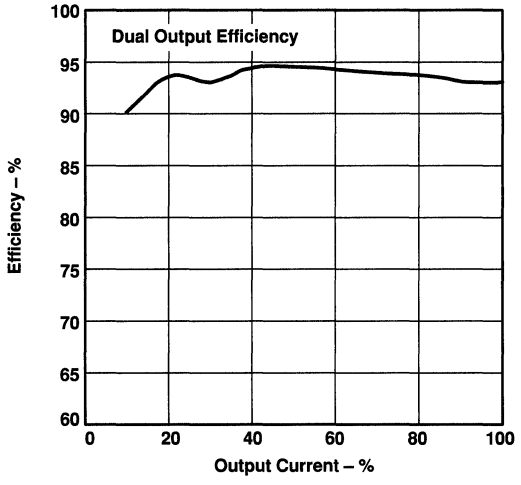


Figure 16

OUTPUT LOAD REGULATION

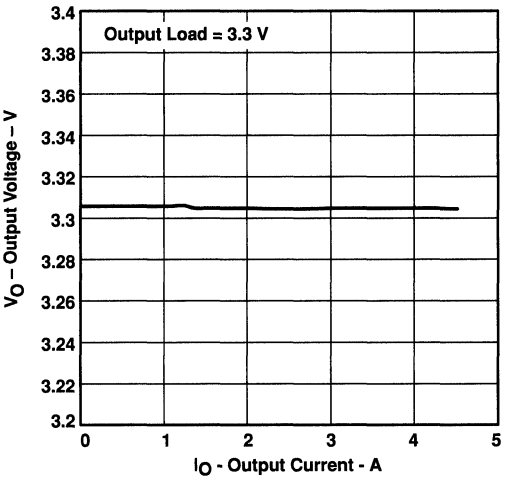


Figure 17

OUTPUT LOAD REGULATION

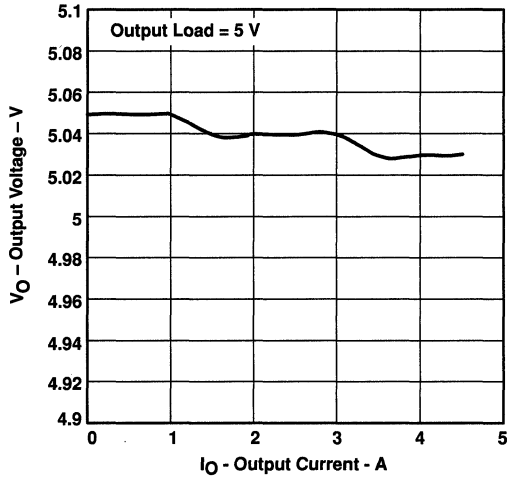


Figure 18

OUTPUT LINE REGULATION

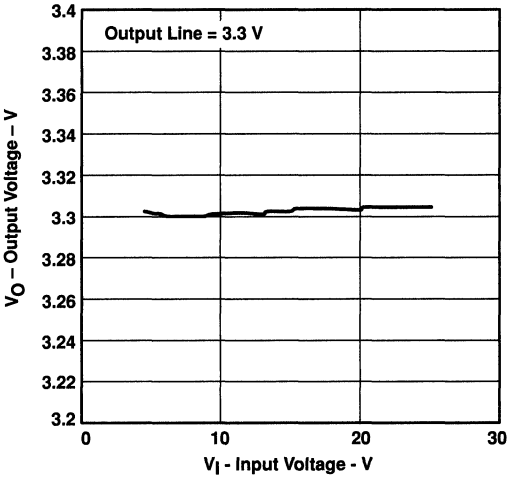


Figure 19

APPLICATION INFORMATION

OUTPUT LINE REGULATION

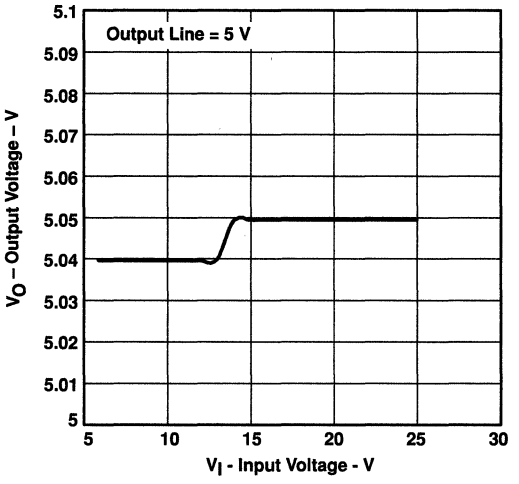


Figure 20

DIODE VERSION EFFICIENCY

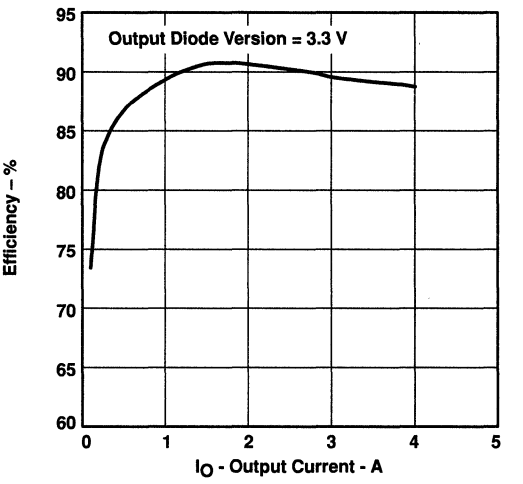


Figure 21

3.3–V OUTPUT VOLTAGE RIPPLE

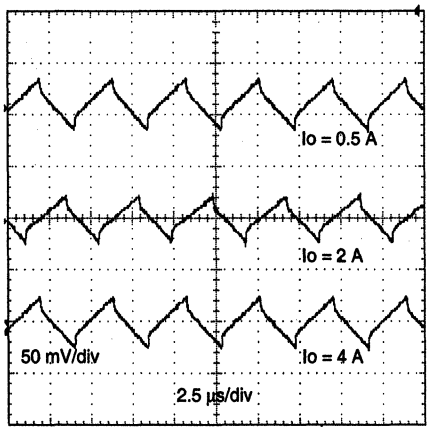


Figure 22

5–V OUTPUT VOLTAGE RIPPLE

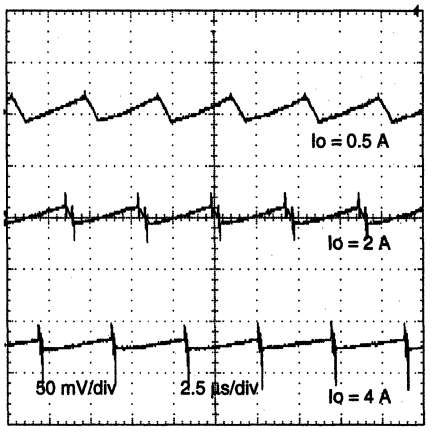


Figure 23

APPLICATION INFORMATION

Table 1. Bill of Materials

REF.	PN	DESCRIPTION	MANUFACTURER	SIZE
C1	RV-35V221MH10-R	Capacitor, electrolytic, 220 µF, 35 V	ELNA	10x10mm
C1†opt	10TPB220M	Capacitor, POSCAP, 220 µF, 10 V	Sanyo	7.3x4.3mm
C2	GMK325F106ZH	Capacitor, ceramic, 10 µF, 35 V	Taiyo Yuden	1210
C3	GMK325F106ZH	Capacitor, ceramic, 10 µF, 35 V	Taiyo Yuden	1210
C4	4TPB470M	Capacitor, POSCAP, 470 µF, 4 V	Sanyo	7.3x4.3mm
C5	10TPB220M	Capacitor, POSCAP, 220 µF, 10 V	Sanyo	7.3x4.3mm
C5†opt	6TPB330M	Capacitor, POSCAP, 330 µF, 6.3 V	Sanyo	7.3x4.3mm
C6†	Standard	Open, capacitor, ceramic, 0.22 µF, 16 V		805
C7	Standard	Capacitor, ceramic, 0,01 µF, 16 V		805
C8	Standard	Capacitor, ceramic, 220 pF, 16 V		805
C9	Standard	Capacitor, ceramic, 0.01 µF, 16 V		805
C10	Standard	Capacitor, ceramic, 100 pF, 16 V		805
C11	Standard	Capacitor, ceramic, 1 µF, 16 V	muRata	805
C12	GMK316F225ZG	Capacitor, ceramic, 2.2 µF, 35 V	Taiyo Yuden	1206
C13	Standard	Capacitor, ceramic, 0.01 µF, 16 V		805
C14	Standard	Capacitor, ceramic, 220 pF, 16 V		805
C15	Standard	Capacitor, ceramic, 0.1 µF, 16 V		805
C16†	Standard	Open, capacitor, ceramic, 0.1 µF, 16 V		805
C17	GMK316F225ZG	Capacitor, ceramic, 2.2 µF, 35 V	Taiyo Yuden	1206
C18	Standard	Open		805
C19	Standard	Open		805
C20	GMK325F106ZH	Capacitor, ceramic, 10 µF, 35 V	Taiyo Yuden	1210
C21	GMK316F225ZG	Capacitor, ceramic, 2.2 µF, 35 V	Taiyo Yuden	1206
C22†				7.3x4.3mm
C23†				7.3x4.3mm
D1	MBRS340T3	Diode, Schottky, 40 V, 3 A	Motorola	SMC
D2	MBRS340T3	Diode, Schottky, 40 V, 3 A	Motorola	SMC
D3	SD103-AWDICT-ND	Diode, Schottky, 40 V, 200 mA	Digikey	3.5x1.5mm
D4	SD103-AWDICT-ND	Diode, Schottky, 40 V, 200 mA	Digikey	3.5x1.5mm
L1	DO3316P-682	Inductor, 6.8 µH, 4.4 A	Coilcraft	0.5x0.37in
L2	DO3316P-682	Inductor, 6.8 µH, 4.4 A	Coilcraft	0.5x0.37in
J1-J16	CA26DA-D36W-OFC	Edge connector, surface mount, 0.040" board, 0.090" standoff	NAS Interplex	0.040in
JP1	S1132-2-ND	Header, straight, 2-pin, 0.1 ctrs, 0.3" pins	Sullins	DigiKey # 1132-2-ND
JP1 shunt	S1132-14-ND	Shunt, jumper, 0.1"	Sullins	DigiKey # 929950-00-ND
JP2	S1132-14-ND	Header, straight, 2-pin, 0.1 ctrs, 0.3" pins	Sullins	DigiKey # 1132-2-ND
R1	Standard	Resistor, 5.1 Ω, 5%		805
R2	Standard	Resistor, 5.1 Ω, 5%		805
R3†	Standard	Open		805
R4	Standard	Resistor, 1.21 kΩ, 1%		805
R5	Standard	Resistor, 680 Ω, 1%		805
R6	Standard	Resistor, 5.1 kΩ, 5%		805
R8	Standard	Resistor, 1 kΩ, 5%		805

† Option table

APPLICATION INFORMATION

Table 1. Bill of Materials (continued)

REF.	PN	DESCRIPTION	MANUFACTURER	SIZE
R9	Standard	Resistor, 82 kΩ, 5%		805
R10	Standard	Resistor, 1 kΩ, 5%		805
R11	Standard	Resistor, 0 Ω, 5%		805
R12	Standard	Resistor, 1 kΩ, 5%		805
R13	Standard	Reistor, 1 kΩ, 5%		805
R14	Standard	Resistor, 310 kΩ, 1%		805
R15	Standard	Resistor, 1 kΩ, 1%		805
R16†	Standard	Open resistor, 5.1 Ω, 5%		805
R17	Standard	Resister, 15 Ω, 5%		805
R18	Standard	Resistor, 7.5 kΩ, 5%		805
R19	Standard	Resistor, 7.5 kΩ, 5%		805
R20	Standard	Resistor, 15 Ω, 5%		805
R21	Standard	Open		805
Q1	Si4410DY	Transistor, MOSFET, n-ch, 30 V, 10 A, 13 mΩ,	Siliconix	SO-8
Q2	Si4410DY	Transistor, MOSFET, n-ch, 30 V, 10 A, 13 mΩ,	Siliconix	SO-8
Q3	Si4410DY	Transistor, MOSFET, n-ch, 30 V, 10 A, 13 mΩ,	Siliconix	SO-8
Q4	Si4410DY	Transistor, MOSFET, n-ch, 30 V, 10 A, 13 mΩ,	Siliconix	SO-8
U1	TPS5102	IC, Dual Controller	TI	TSSOP

† Option table

This EVM is designed to cover as many applications as possible. For some more specific applications, the circuit can be simpler. The table below gives some recommendations.

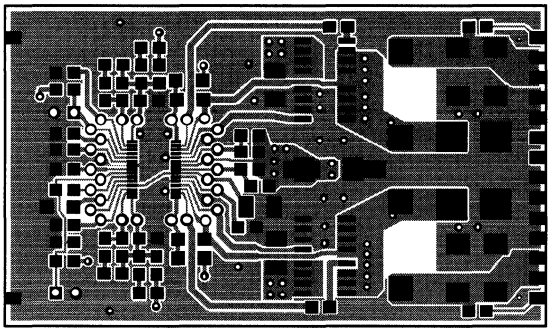
Table 2. EVM Application Recommendations

5V INPUT VOLTAGE	<3–A OUTPUT CURRENT	DIODE VERSION
Change C1 to low profile capacitor Sanyo 10TPB220M (220 µF, 10 V) Or 6TPB330M (330 µF, 6.3 V)	Change Q1/Q2 and Q3/Q4 to dual pack MOSFET, IRF7311 to reduce the cost.	Remove Q2 and Q4 to reduce the cost.
Remove R12		

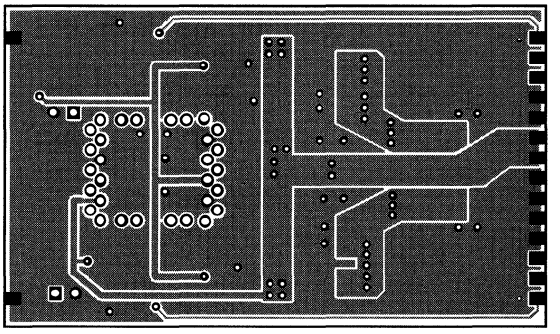
Table 3. Vendor and Source Information

MATERIAL	SOURCE	PART NUMBER	DISTRIBUTORS
MOSFETS (Q1–Q4)	In EVM Design	Si4410DY (SILICONIX)	Local Distributor
	Second Source	IRF7811 (International Rectifier)	
INPUT CAPACITORS (C1)	In EVM Design	RV–35V221MH10–R (ELNA)	Bell Microproducts 972–783–4191
	Second Source	35CV330AX/GX (Sanyo)	870–633–5030
		UUR1V221MNR1GS (Nichicon)	Future Electronics (Local Office)
MAIN DIODES (D1 – D2)	In EVM Design	MBRS340T3 (Motorola)	Local Distributors
	Second Source	U3FWJ44N (Toshiba)	Local Distributors
INDUCTORS (L1 – L2)	In EVM Design	DO3316P–682 (Coilcraft)	972–248–3575
	Second Source	CTDO3316P–682 (Inductor Warehouse)	800–533–8295
CERAMIC CAPACITORS (C2, C3) (C12, C17, C21)	IN EVM Design	GMK325F106ZH GMK316F225ZG (Taiyo Yuden)	SMEC 512–331–1877
	Taiyo Yuden, Representative		e–mail: mike@millsales.com

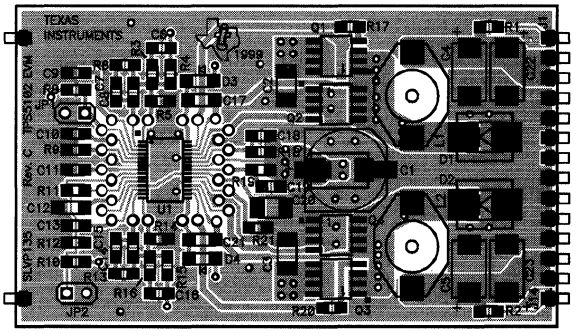
APPLICATION INFORMATION



Top Layer

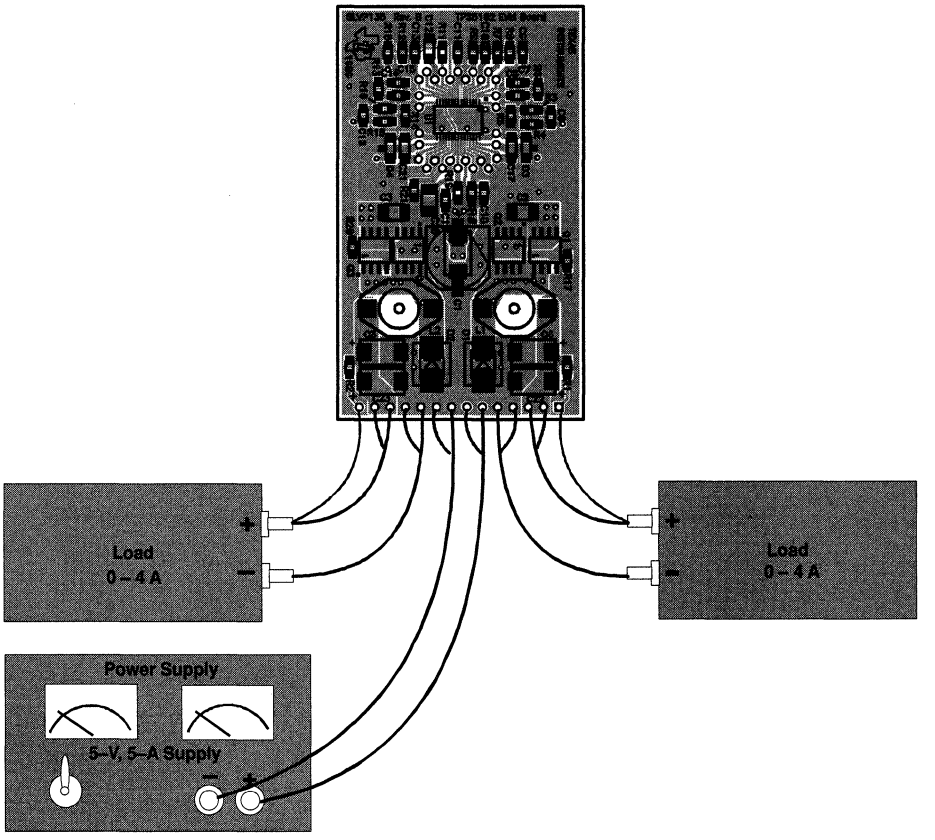


Bottom Layer (Top View)



Top Assembly

APPLICATION INFORMATION



NOTE: All wire pairs should be twisted.

Test Setup

APPLICATION INFORMATION

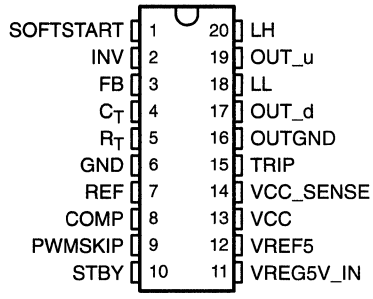
High current applications are described in table . The values are recommendations based on actual test circuits. Many variations are possible based on the requirements of the user. Performance of teh circuit is dependent upon the layout rather than the on specific components, if the device parameters are not exceeded. The power stage, having the highest current levels and greatest dv/dt rates, should be given the most attention, as both the supply and load can be severly affected by the power levels and edge rates.

Table 4. High Current Applications

REFERENCE DESIGNATIONS	FUNCTION	8-A OUTPUT	12-A OUTPUT	16-A OUTPUT
C1	Input Bulk Capacitor	2x ELNA RV-35V221MH10-R 220 µF, 35 V	3x ELNA RV-35V221MH10-R 220 µF, 35 V	4x ELNA RV-35V221MH10-R 220 µF, 35 V
C2 (C3)	Input Bypass Capacitor	2x Taiyo Yuden GMK325F106ZH 10 µF, 35 V	3x Taiyo Yuden GMK325F106ZH 10 µF, 35 V	4x Taiyo Yuden GMK325F106ZH 10 µF, 35 V
L1 (L2)	Output Filter Indicator	Coiltronics UP3B-2R2 2.2 µH, 9.2 A	Coiltronics UP4B-1R5 1.5 µH, 13.4 A	MicorMetals T68-8/90 Core w/7T, #16 1.0 µH, 25 A
C4 (C22)	Output Filter Capacitor	2x Sanyo 4TPB470M 470 µF, 4 V	3x Sanyo 4TPB470M 470 µF, 4 V	4x Sanyo 4TPB470M 470 µF, 4 V
C5 (C23)	Output Filter Capacitor	2x Sanyo 6TPB330M 330 µF, 6.3 V	3x Sanyo 6TPB330M 330 µF, 6.3 V	4x Sanyo 6TPB330M 330 µF, 6.3 V
Q1 (Q3)	Power Switch	2x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	3x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	4x Siliconix Si4410DY 30 V, 10 A, 13 mΩ
Q2 (Q4)	Power Switch	2x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	3x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	4x Siliconix Si4410DY 30 V, 10 A, 13 mΩ
R17 (R20)	Gate Drive Resistor	7 Ω	5 Ω	4 Ω
R18 (R19)	Current Limit Resistor	10 kΩ	15 kΩ	20 kΩ
Switching Frequency		200 kHz	150 kHz	100 kHz

- Step-Down DC-DC Converter
- Three Operation-Mode
  - Heavy Load:
    - Fixed Frequency PWM
    - Hysteretic (User Selctable)
  - Light Load:
    - Skip Mode
- 4.5 V to 25 V Input Voltage Range
- Adjustable Output Voltage Down to 1.2 V
- 95% Efficiency
- Stand-By Control
- Over Current Protection
- UVLO for Internal 5 V Regulation
- Low Standby Current . . . 0.5 mA Typical
- T_A = –40°C to 85°C

DB PACKAGE
(TOP VIEW)



description

The TPS5103 is a synchronous buck dc/dc controller, designed for notebook PC system power. The controller has three user-selectable operation modes available; hysteretic mode, fixed frequency PWM control, or SKIP control.

In high current applications, where fast transient response is advantageous for reducing bulk capacitance, the hysteretic mode is selected by connecting the Rt pin to Vref5. Selecting the PWM/SKIP modes for less demanding transient applications is ideal for conserving notebook battery life under light load conditions. The device includes high-side and low-side MOSFET drivers capable of driving low Rds (on) N–channel MOSFETs.

The user-selectable overcurrent protection (OCP) threshold is set by an external TRIP pin resister in order to protect the system. The TPS5103 is configured so that a current sense resistor is not required, improving the operating efficiency.

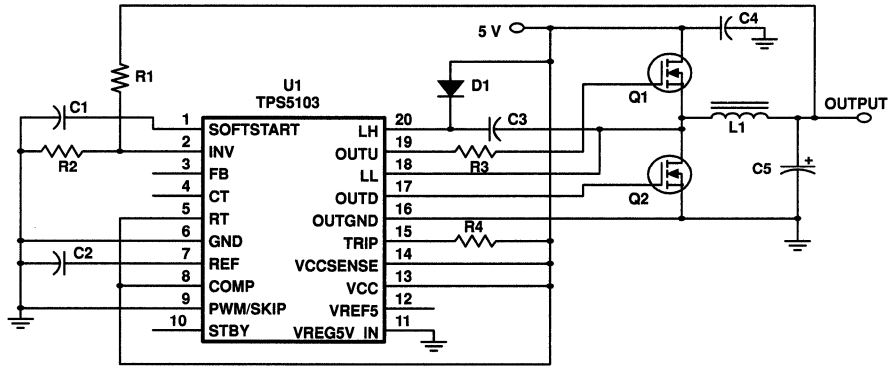
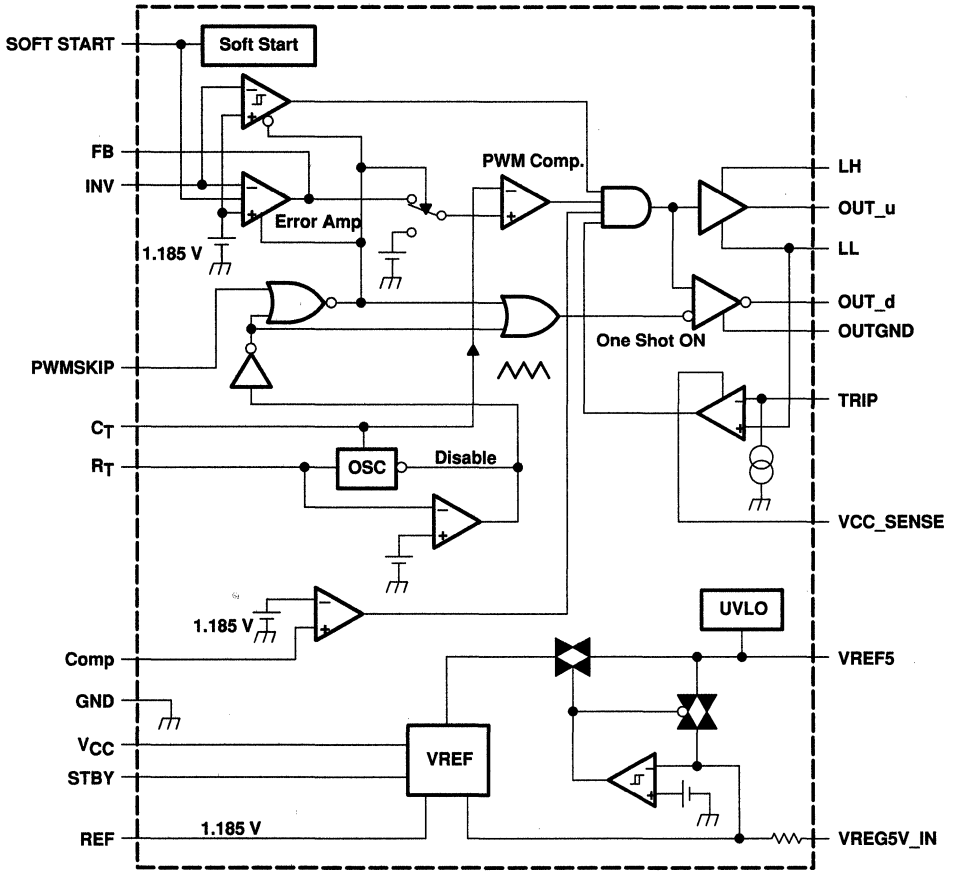


Figure 1. Typical Design

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE	
	SSOP(DB)	EVM
–40 °C to 85 °C	TPS5103IDB	TPS5103EVM–136
	TPS5103IDBR	

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
COMP	8	I	Comparator input for voltage monitor
C_T	4	I/O	External capacitor from C_T to GND for adjusting the triangle oscillator and decreasing the current limiting voltage
FB	3	O	Feedback output of error amp
GND	6		Control GND
INV	2	I	Inverting input of both error amp and hysteretic comparator
LH	20	I/O	Bootstrap. Connect 1 µF low-ESR capacitor from LH to LL.
LL	18	I/O	Bootstrap low. High side gate driving return and output current protection. Connect to the junction of the high side and low side FETs for floating drive configuration.
OUT_d	17	I/O	Gate-drive output for low-side power switching FETs
OUTGND	16		Ground for FET drivers
OUT_u	19	O	Gate-drive output for high-side power switching FETs
PWMSKIP	9	I	PWM/SKIP mode select L:PWM mode H:SKIP mode
REF	7	O	1.185-V reference voltage output
R_T	5	I/O	External resistor connection for adjusting the triangle oscillator.
SOFTSTART	1	I	External capacitor from SOFTSTART to GND for soft start control
STBY	10	I	Standby control
TRIP	15	I	External resistor connection for output current control
V_{CC}	13	I	Supply voltage input
VCC_SENSE	14	I	Supply voltage sense for current protection
VREF5	12	O	5-V-internal regulator output
VREG5V_IN	11	I	External 5-V input (input voltage range = 4.5 V to 25 V)

detailed description

REF

The reference voltage is used for the output voltage setting and the voltage protection(COMP). The tolerance is 1.5% typically.

VREF5

An internal linear voltage regulator is used for the high-side driver bootstrap voltage. Since the input voltage range is from 4.5 V to 25 V, this voltage offers a fixed voltage for the bootstrap voltage so that the design for the bootstrap is much easier. The tolerance is 6%.

hysteretic comparator

The hysteretic comparator is used to regulate the output voltage of the synchronous-buck converter. The hysteresis is set internally and is typically 9.7 mV. The total delay time from the comparator input to the driver output is typically 400 ns for going both high and low.

error amplifier

The error amplifier is used to sense the output voltage of the synchronous buck converter. The negative input of the error amplifier is connected to the Vref voltage(1.185 V) with a resistive divider network. The output of the error amplifier is brought out to the FB terminal to be used for loop gain compensation.

low-side driver

The low-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The maximum drive voltage is 5 V from VREF5. The current rating of driver is typically 1.2 A at sink current, –1.5 A at source current.

high-side driver

The high-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 1.2 A at sink current, –1.7 A at source current. When configured as a floating driver, the bias voltage to the driver is developed from the VREF5, limiting the maximum drive voltage between OUT_u and LL to 5 V. The maximum voltage that can be applied between LH and OUTGND is 30 V.

driver deadtime control

The deadtime control prevents shoot-through current from flowing through the main power FETs. During switching transitions the deadtime control actively controls the turnon time of the MOSFET drivers. The typical deadtime from the low-side-driver-off to the high-side-driver-on is 90 ns, and 110 ns from high-side-driver-off to low-side-driver-on.

COMP

COMP is designed for use with a regulation output monitor. COMP also functions as an internal comparator used for any voltage protection such as the input under voltage protection. If the input voltage is lower than the setpoint, the comparator turns off and prevents external parts from damage. The investing terminal of the comparator is internally connected to REF(1.185 V).

current protection

Current protection is achieved by sensing the high-side power MOSFET drain-to-source voltage drop during on-time through VCC_SENSE and LL terminals. An external resistor between Vin and TRIP terminal with the internal current source connected to the current comparator negative input adjusts the current limit. The typical internal current source value is 15 μA in PWM mode, 5 μA in SKIP mode. When the voltage on the positive terminal is lower than the negative terminal, the current comparator turns on the trigger, and then activates the oscillator. This oscillator repeatedly reset the trigger until the over current condition is removed. The capacitor on the C_T terminal can be open or added to adjust the reset frequency.

detailed description (continued)

softstart

SOFTSTART sets the sequencing of the output for any possibility. The capacitor value for a start-up time can be calculated by the following equation: C = 2xT (uF) where C is the external capacitor value, T is the required start-up time in (ms).

standby

This controller can be switched into standby mode by grounding the STBY terminal. When it is in standby mode, the quiescent current is less than 1.0 uA.

UVLO

The under-voltage-lock-out (ULVO) threshold is approximately 3.8 V. The typical hysteresis is 55 mV.

5-V Switch

5-V Switch if the internal 5-V switch senses a 5-V input from REG5V terminal, the internal 5-V linear regulator will be disconnected from the MOSFET drivers. The external 5 V will be used for both the low-side driver and the high-side bootstrap, thus increasing the efficiency.

PWM/SKIP switch

The PWM/SKIP switch selects the output operating mode. This controller has three operational modes, PWM, SKIP, and Hysteretic. The PWM and SKIP mode control should be used for slower transient applications.

oscillator

The oscillator gives a triangle wave by connecting an external resistor to the R_T terminal and an external capacitor to the C_T terminal. The voltage amplitude is 0.43 V ~ 1.17 V. This wave is connected to the non-inverting input of the PWM comparator.

Comparison Table Between PWM Mode and Hysteretic Mode

MODE	PWM	HYSTERETIC
Frequency	Fixed	Not Fixed
Transient Response	Normal	Very fast
Feed back compensation	Need	Needless

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... –0.3 V to 27 V
Input voltage, V_I, INV, C_T, R_T, PWM/SKIP, SOFTSTART, COMP ..... –0.3 V to 7 V
Input voltage, VREG5V_IN ..... –0.3 V to 6 V
Input voltage, STBY ..... –0.3 V to 15 V
Input voltage, TRIP, VCC_SENSE ..... –0.3 V to 27 V
Output current, I_O ..... 3 A
Low level output voltage, V_{OL} ..... –0.3 V to 27 V
High level output voltage, V_{OH} ..... –0.3 V to 32 V
Reference voltage, V_{ref} ..... –0.3 V to 3 V
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating virtual junction temperature range, T_J ..... –125°C
Storage temperature range, T_{stg} ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. See Dissipation Rating Table for free-air temperature range above 25°C.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DB	801 mW	6.408mW/°C	416 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		25	V
V_I	Input voltage	INV, CT, RT, COMP, PWM_SKIP, SOFTSTART			6	V
		VREG5V_IN			5.5	
		STBY			12	
		TRIP, V_{CC}_SENCE			25	
R_T‡	Oscillator frequency	Timing register		82		kΩ
C_T‡		Timing capacitor		100		pF
f		Frequency		200		kHz
T_A	Operating temperature range		–40		85	°C

‡ Not a JEDEC symbol.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 7 V (unless otherwise noted)

reference voltage

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference voltage	T_A = 25°C,	I_{vref} = 50 µA	1.167	1.185	1.203	V
		I_{vref} = 50 µA‡		1.155		1.215	
Regin	Line regulation†	V_{CC} = 4.5 V to 25 V,	I = 50 µA		0.2	12	mV
Regl	Load regulation†	I = 1 µA to 1 mA			0.5	10	mV

† Not a JEDEC symbol.

oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Frequency	PWM mode			500	kHz
R_T	Timing resistor		47			kΩ
fdv	Frequency change†	V_{CC} = 4.5 V to 25 V		0.1%		
fdt		T_A = −40°C to 85°C		2%		
V_{HL}‡	High-level output voltage	DC includes internal comparator error	1	1.1	1.2	V
		f = 200 kHz, includes internal comparator error		1.17		
V_{LL}‡	Low-level output voltage	DC includes internal comparator error	0.4	0.5	0.6	V
		f = 200 kHz, includes internal comparator error		0.43		

† Not a JEDEC symbol.
‡ The output voltages of oscillator (f = 200 kHz) are ensured by design.

error amp

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V	Input offset voltage	T_A = 25°C		2	10	mV
Av	Open-loop voltage gain†		50			dB
GB	Unity-gain bandwidth†			0.8		MHz
I_O	Output sink current	VO = 0.4 V	30	45		µA
I_S	Output source current	VO = 1 V		300		µA

† Not a JEDEC symbol.

hysteresis comparator§

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hsy}	Hysteresis window	Hysteretic mode	6	9.7	13	mV
Vp-V_S	Offset voltage			2		mV
I	Bias current			10		pA
t_{PHL}	Propagation delay from INV to OUT_U	TTL input signal		230		ns
t_{PLH}		10 mV overdrive on hysteresis band signal		400		ns

§ The numbers in the table include the driver delay. All numbers are ensured by design.

control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IHA}	High-level input voltage	STBY	2.5			V
		PWM_SKIP	2			
V_{ILA}	Low-level input voltage	STBY			0.5	V
		PWM_SKIP			0.5	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 7 V (unless otherwise noted) (continued)

5-V regulator

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	I = 10 mA		4.7		5.3	V
Regin	Line regulation†	V_{CC} = 5.5 V to 25 V,	I = 10 mA			20	mV
Regl	Load regulation†	I = 1 mA to 10 mA,	V_{CC} = 5.5 V			40	mV
I_{OS}	Short-circuit output current	V_{ref} = 0 V			70		mA

† Not a JEDEC symbol.

5-V switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(high)}$	Threshold voltage†		4.2		4.9	V
$V_{IT(low)}$			4.1		4.8	
V_{hsy}	Hysteresis)		50	150	250	mV

† Not a JEDEC symbol.

UVLO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(high)}$	Threshold voltage†		3.6		4.2	V
$V_{IT(low)}$			3.5		4.1	
V_{hys}	Hysteresis		10		150	mV

† Not a JEDEC symbol.

output

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_O	OUT_u sink curent	V_O = 3 V		0.5	1.2		A
I_S	OUT_u source current	V_O = 2 V		–1	–1.7		A
I_O	OUT_d sink current	V_O = 3 V		0.5	1.2		A
I_S	OUT_d source current	V_O = 2 V		–1	–1.5		A
I	TRIP terminal current	PWM mode,	VTRIP = 7 V	10	15	20	µA
		SKIP mode,	VTRIP = 7 V	3	5	7	
t_r	Rise time	High side driver is GND referenced.					ns
		Input: INV = 0 – 3V					
		t_r/t_f = 10 ns,	Frequency = 200 kHz				
		C_L = 2200 pF			28		
		C_L = 3300 pF			39		
t_f	Fall time	High side driver is GND referenced.					ns
		Input: INV = 0 – 3 V					
		t_r/t_f = 10 ns,	Frequency = 200 kHz				
		C_L = 2200 pF			30		
		C_L = 3300 pF			38		

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 7 V (unless otherwise noted) (continued)

softstart

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(CTRL)}$	Softstart current		1.9	2.5	3	µA
$V_{IT(high)}$	Threshold voltage (SKIP mode)†			3.9		V
$V_{IT(low)}$				2.6		

† Not a JEDEC symbol.

output voltage monitor

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		1.08	1.18	1.28	V

driver deadtime section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{DRVLH}	Low-side to high-side			90		ns
T_{DRVHL}	High-side to low-side			110		ns

whole device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current			0.5	1.2	mA
I	Shutdown current	STBY = 0 V		0.01	10	µA

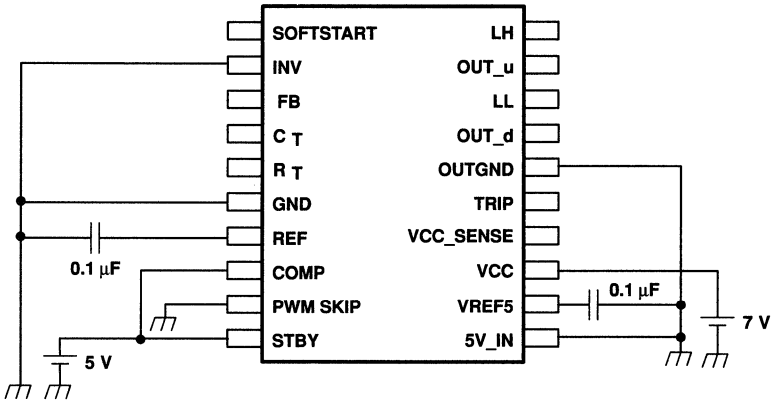


Figure 2. Test Circuit

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE

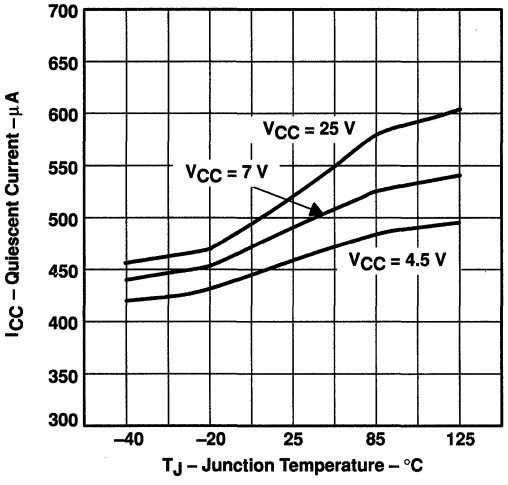


Figure 3

QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE

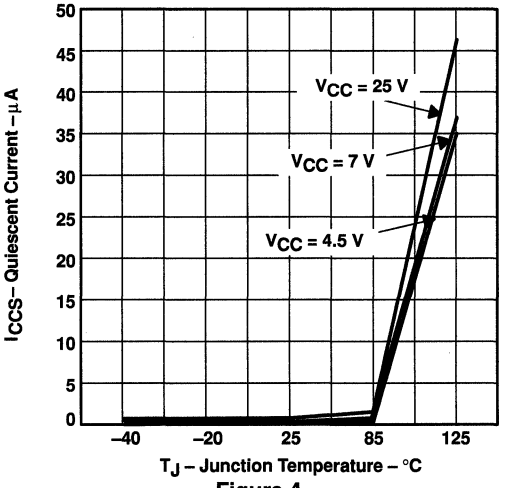


Figure 4

DRIVE OUTPUT VOLTAGE
vs
DRIVE CURRENT

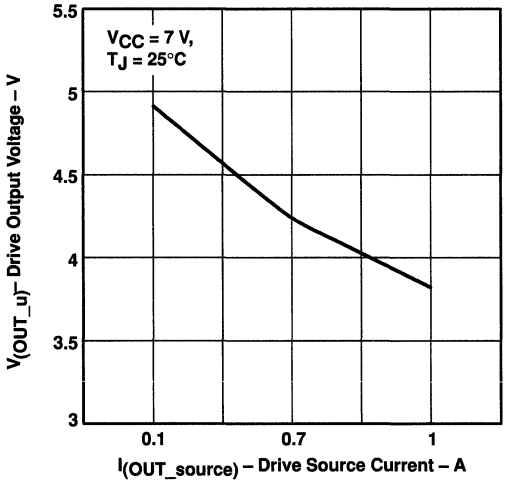


Figure 5

DRIVE OUTPUT VOLTAGE
vs
DRIVE CURRENT

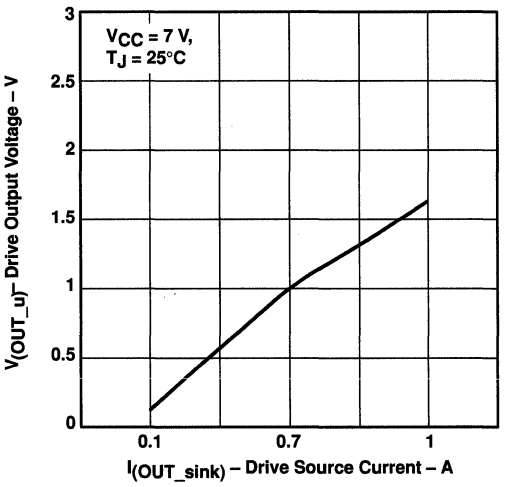


Figure 6

TYPICAL CHARACTERISTICS

DRIVE OUTPUT VOLTAGE
vs
DRIVE CURRENT

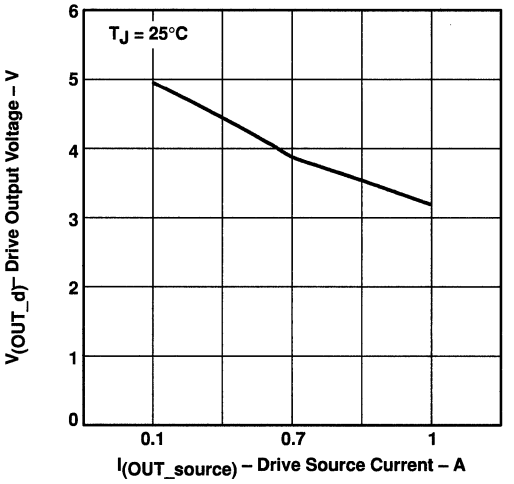


Figure 7

DRIVE OUTPUT VOLTAGE
vs
DRIVE CURRENT

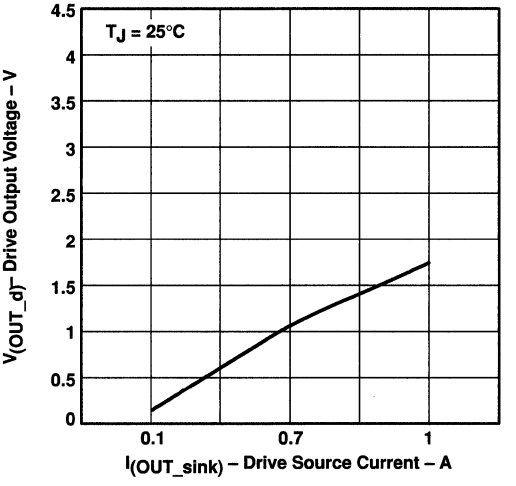


Figure 8

OSCILLATOR OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

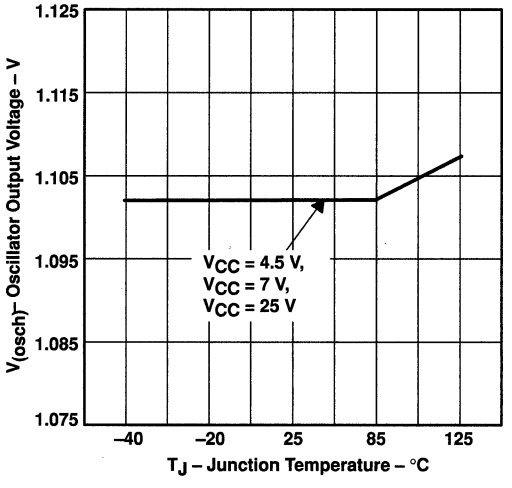


Figure 9

OSCILLATOR OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

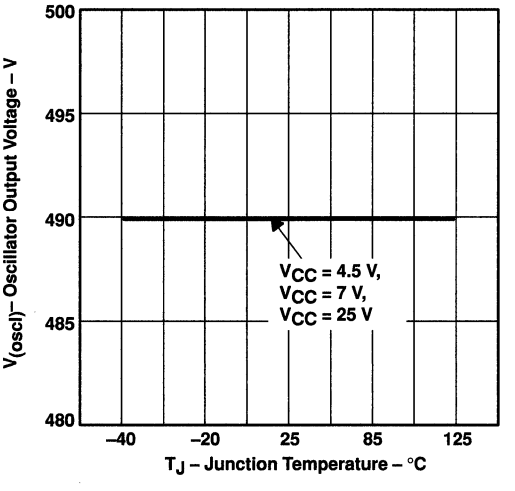


Figure 10

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER INPUT OFFSET VOLTAGE
vs
JUNCTION TEMPERATURE

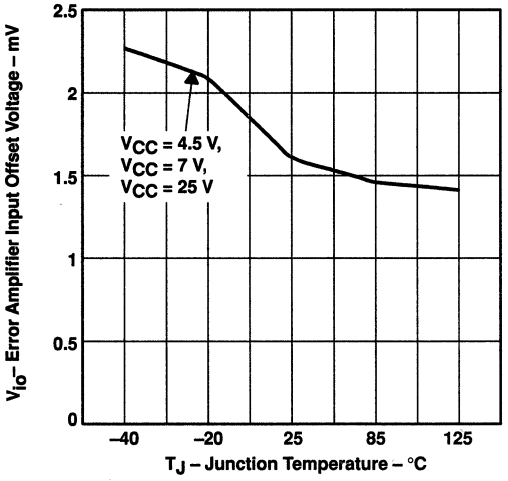


Figure 11

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

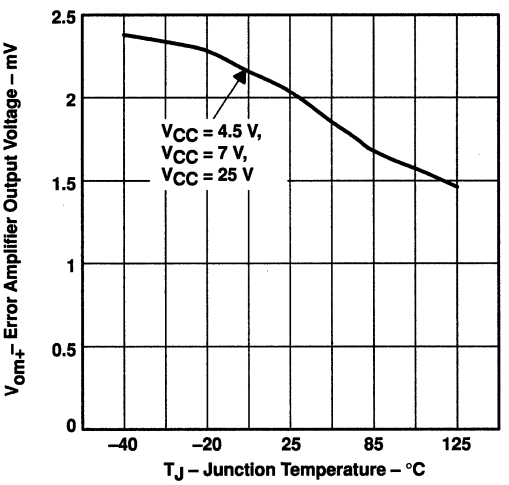


Figure 12

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

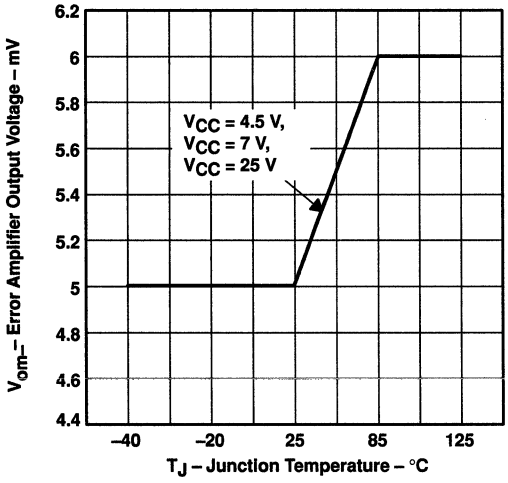


Figure 13

HYSTERESIS COMPARATOR HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

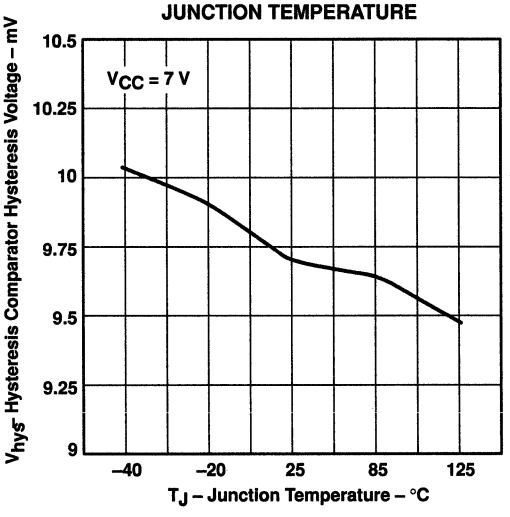


Figure 14

TYPICAL CHARACTERISTICS

STANDBY SWITCH THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

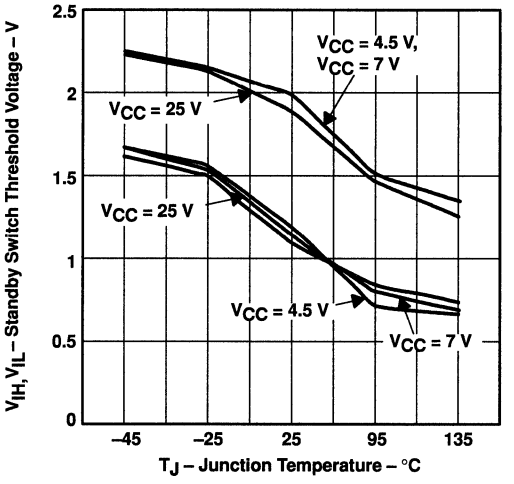


Figure 15

VREF5 OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

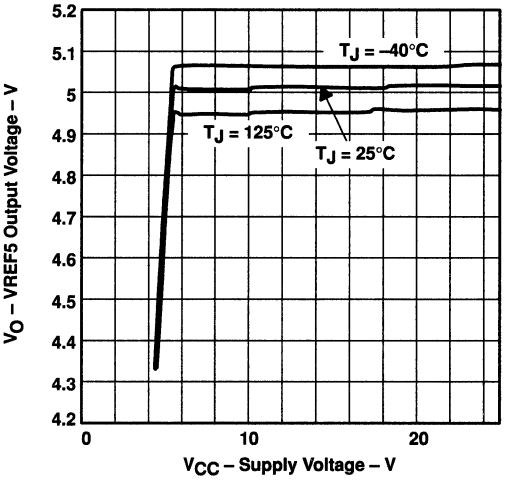


Figure 16

VREF5 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

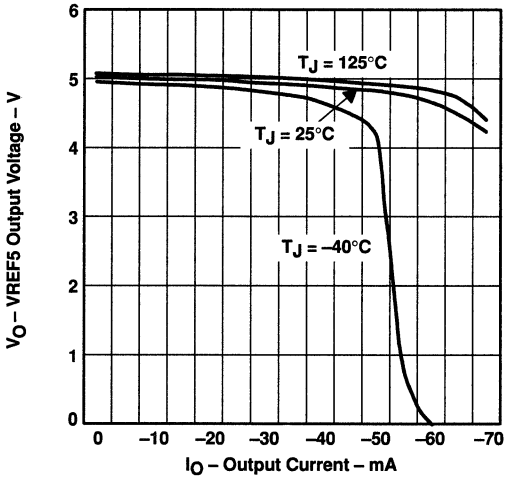


Figure 17

VREF5 SHORT CURRENT
vs
JUNCTION TEMPERATURE

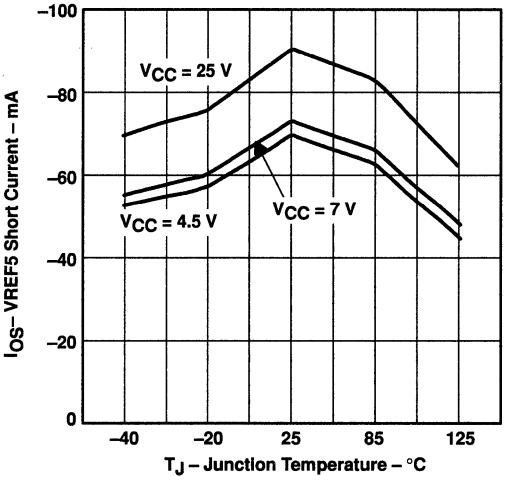


Figure 18

TYPICAL CHARACTERISTICS

UVLO THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

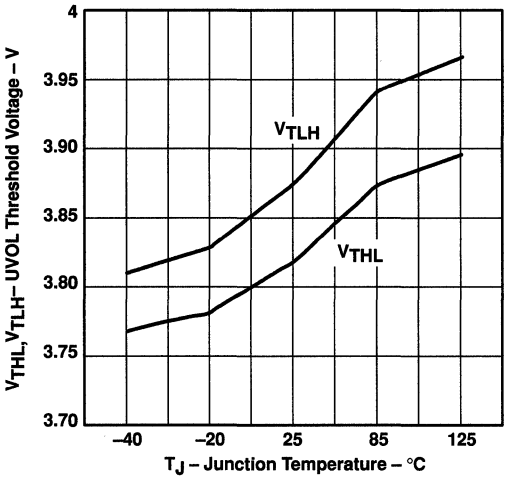


Figure 19

UVLO HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

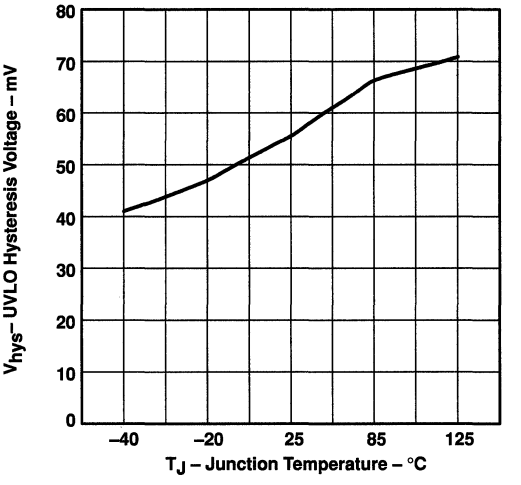


Figure 20

5 VSW THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

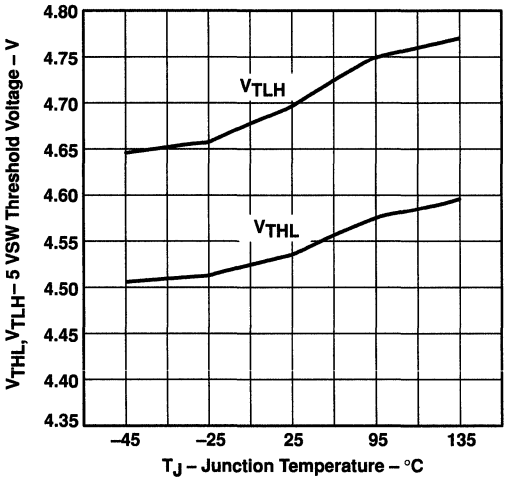


Figure 21

5 VSW HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

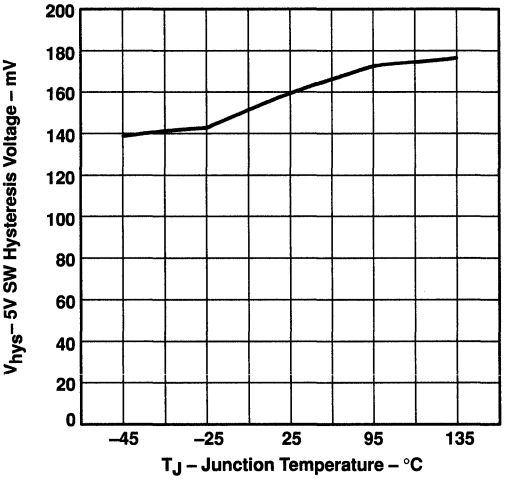


Figure 22

TYPICAL CHARACTERISTICS

SOFTSTART CURRENT
vs
JUNCTION TEMPERATURE

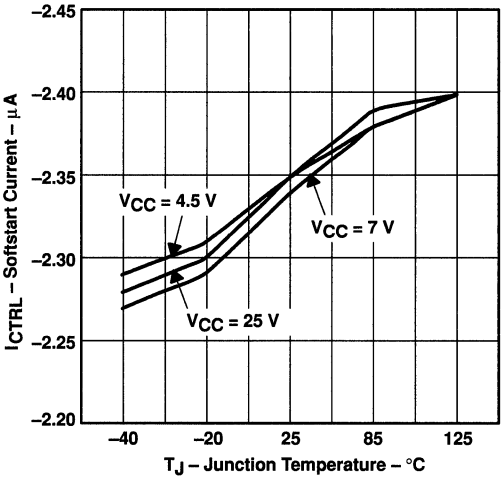


Figure 23

SOFTSTART THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

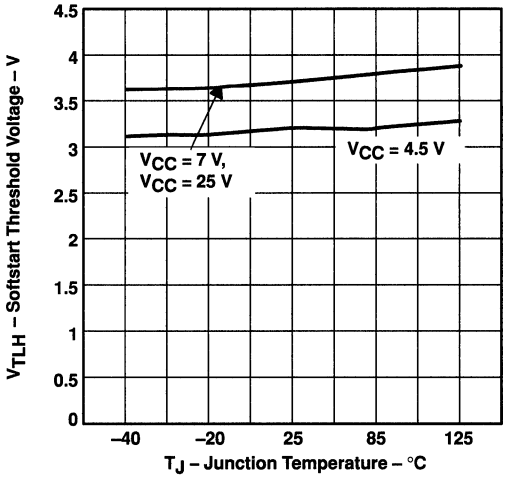


Figure 24

SOFTSTART THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

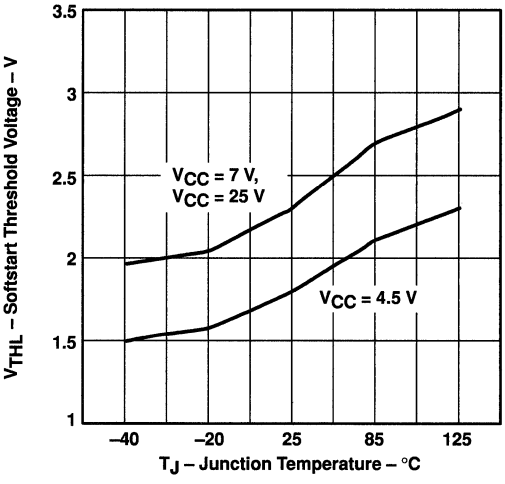


Figure 25

OUTPUT VOLTAGE MONITOR COMPARATOR
THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

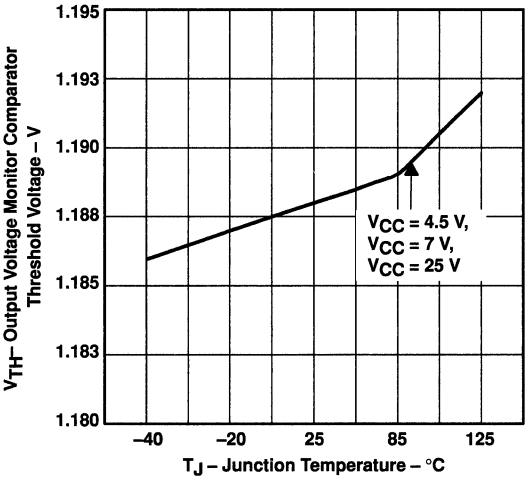


Figure 26

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY
vs
JUNCTION TEMPERATURE

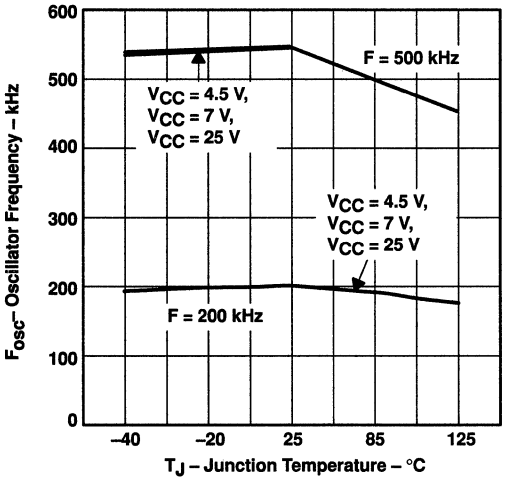


Figure 27

OSCILLATOR OUTPUT VOLTAGE
vs
FREQUENCY

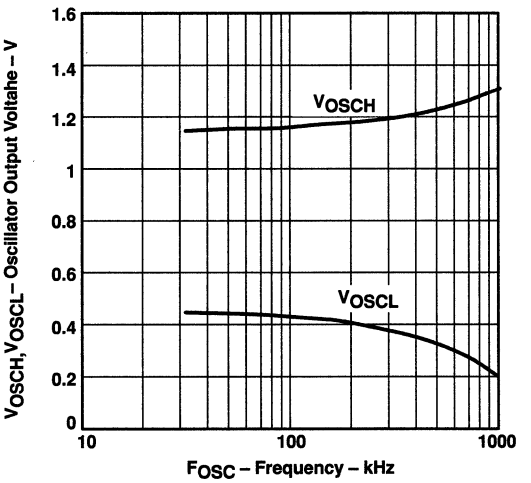


Figure 28

ERROR AMPLIFIER GAIN AND PHASE SHIFT

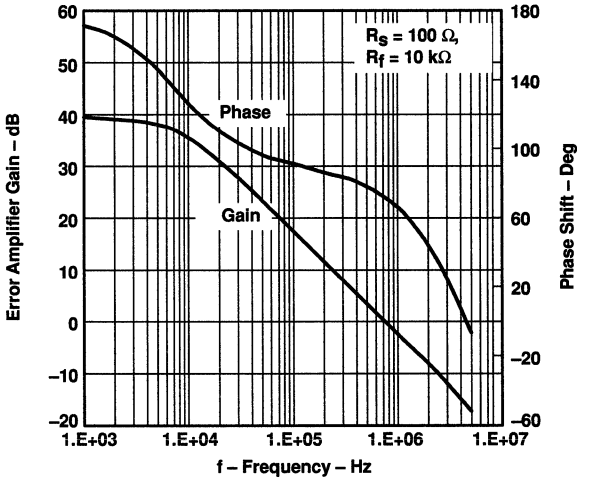


Figure 29

TYPICAL CHARACTERISTICS

MAXIMUM DUTY CYCLE
vs
JUNCTION TEMPERATURE

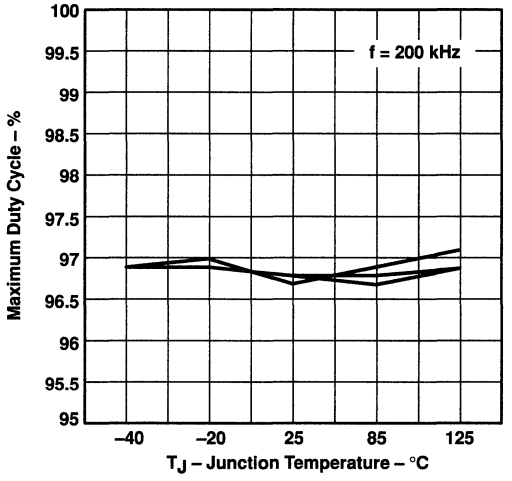


Figure 30

SOFTSTART CAPACITANCE
vs
SOFTSTART TIME

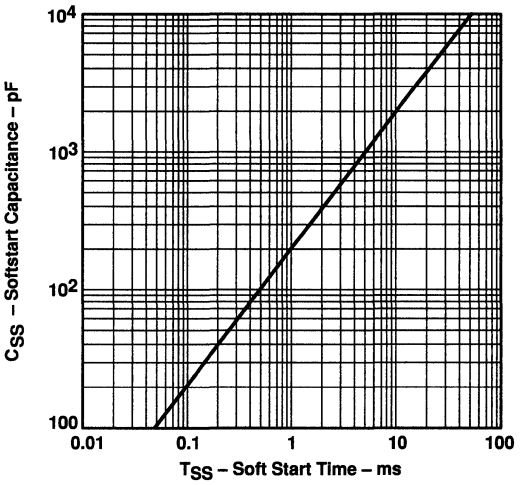


Figure 31

DRIVER DEAD TIME
vs
JUNCTION TEMPERATURE

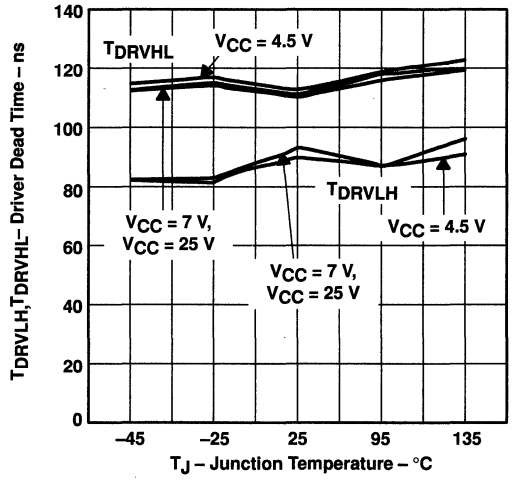


Figure 32

CURRENT PROTECTION SOURCE CURRENT
vs
INPUT VOLTAGE PWM MODE

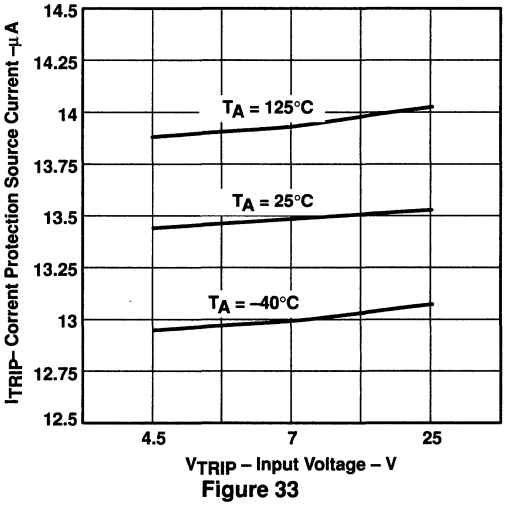


Figure 33

TYPICAL CHARACTERISTICS

CURRENT PROTECTION SOURCE CURRENT
vs
INPUT VOLTAGE SKIP MODE

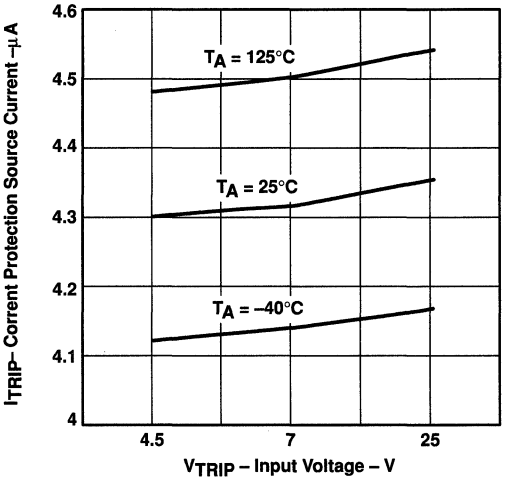


Figure 34

OSCILLATOR FREQUENCY
vs
RESISTOR

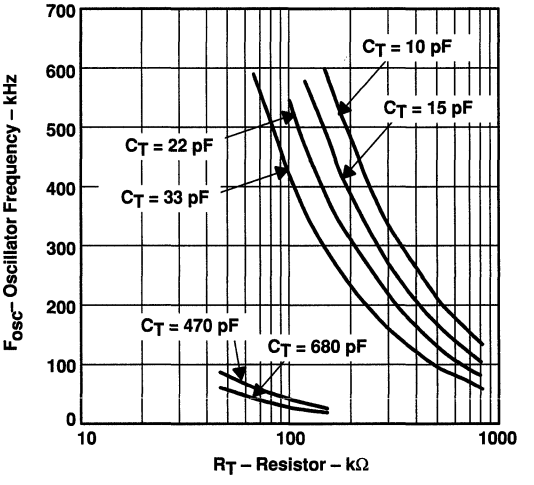
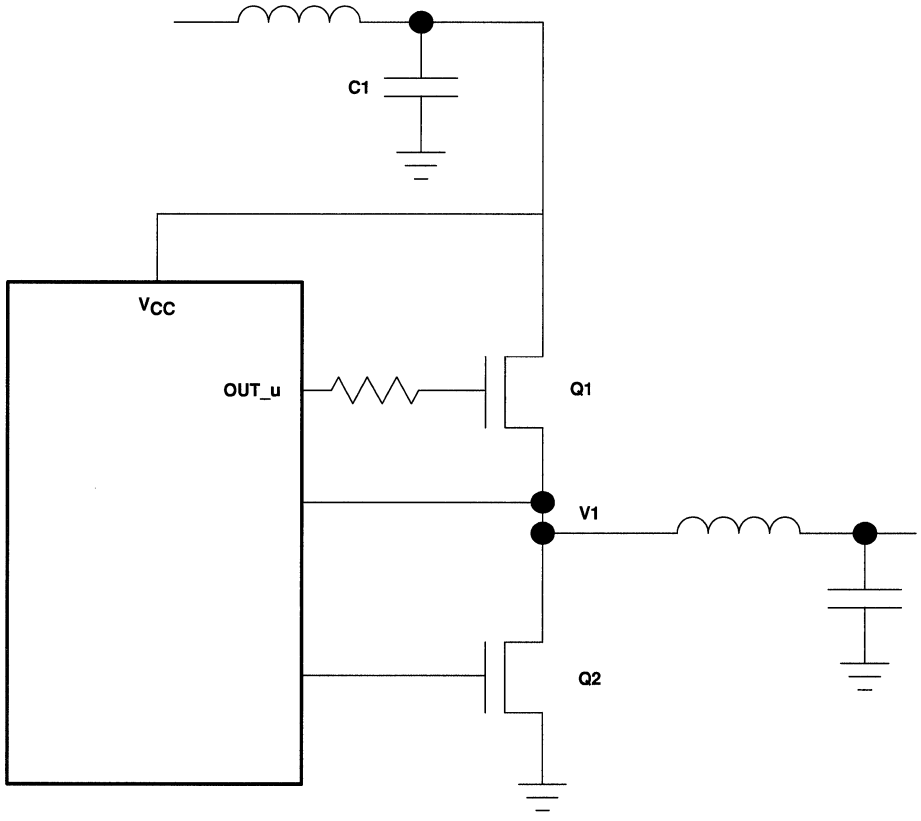


Figure 35

APPLICATION INFORMATION

overshoot of output rectangle wave

The drivers in the TPS5103 controller are fast and can produce high transients on V_{CC} or the junction of Q1 and Q2(shown below). Care must be taken to insure that these transients do not exceed the absolute maximum rating for the device or associated external component. A low-ESR capacitor connected directly from Q1 drain to Q2 source can greatly reduce transient pulses on V_{CC}. Also, Q1 turn-on-speed can be reduced by adding a resistor (5 – 15 Ω) in series with OUT_u. Poor layout of the switching node (V1 in figure) can result in the requirement for additional snubber circuitry require from V1 to ground.



APPLICATION INFORMATION

application for general power

The design shown in this data sheet is a reference design for a general power supply application. An evaluation module (EVM), TPS5103EVM-136 (SLVP136), is available for customer testing and evaluation. The intent is to allow a customer to fully evaluate the given design using the plug-in EVM supply shown here. For subsequent customer board revisions, the EVM design can be copied onto the users PCB to shorten design cycle time, component count, and board cost.

To help the customers to design the power supply using TPS5103, some key design procedures are shown below.

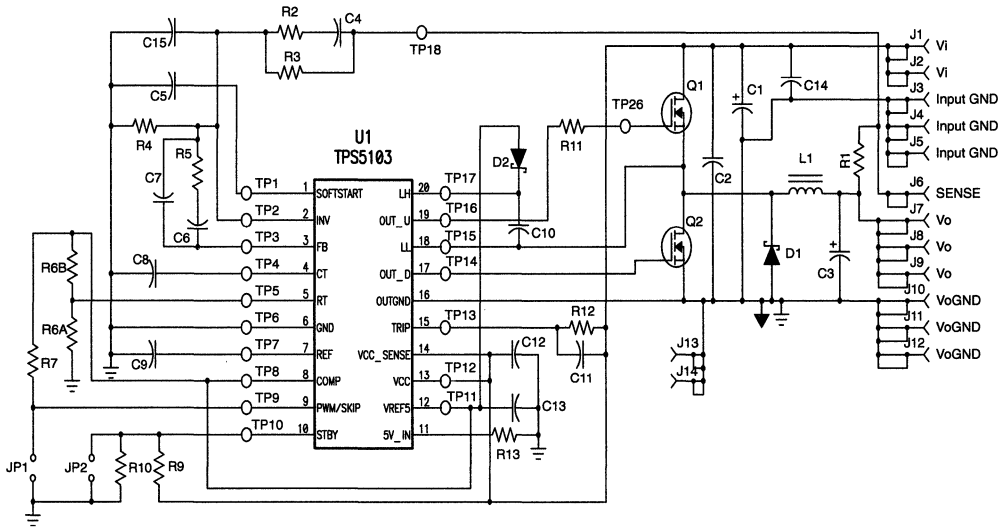


Figure 36. EVM Schematic

APPLICATION INFORMATION

output voltage setpoint calculation

The output voltage is set by the reference voltage and the voltage divider. In TPS5102, the reference voltage is 1.185 V, and the divider is composed of two resistors in the EVM design that are R4 and R5, or R14 and R15. The equation for the setpoint is:

$$R2 = \frac{R1 \times Vr}{Vo - Vr}$$

Where R1 is the top resistor (kΩ) like R4 or R15; R2 is the bottom resistor (kΩ) such as R5 or R14; Vo is the required output voltage (V); Vr is the reference voltage (1.185 V in TPS5103).

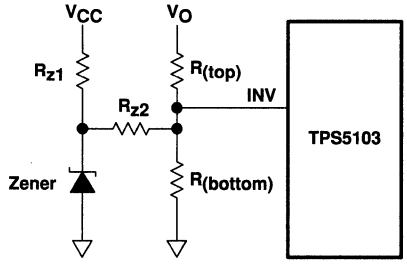
Example: R1 = 1 kΩ; Vr = 1.185 V; Vo = 1.8 V, then R2 = 1.9 kΩ.

For your convenience, some of the most popular output voltage setpoints are calculated in the table below:

Vo	1.3 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
R1 (top) (kΩ)	1	1	1	1	1	1
R2 (bottom) (kΩ)	10	3.7	1.9	0.9	0.56	0.31

If higher precision resistor is used, the output voltage setpoint can be more accurate.

In some applications, the output voltage is required to be lower than the reference voltage. With few extra components, the lower voltage can be easily achieved. The drawing below shows the method.



In the schematic, the Rz1, Rz1, and the zener are the extra components. Rz1 is used to give zener enough current to build up the zener voltage. The zener voltage is added to INV through Rz2. Therefore, the voltage on INV is still equal to the IC internal voltage (1.185 V) even if the output voltage is regulated at lower setpoint. The equation for setting up the output voltage is shown below:

$$Rz2 = \frac{(Vz-Vr)}{\frac{(Vr-Vo)}{Rtop} + \frac{Vr}{Rbtm}}$$

Where Rz2 is the adjusting resistor for low output voltage; Vz is the zener voltage; Vr is the internal reference voltage; Rtop is the top resistor of voltage sensing network; Rbtm is the bottom resistor of the sensing network; Vo is the required output voltage setpoint.

Example: Assuming the required output voltage setpoint is Vo = 0.8 V, Vz = 5 V; Rtop = 1 kΩ; Rbottom = 1 kΩ, then the Rz2 = 2.43 kΩ.

APPLICATION INFORMATION

switching frequency

With hysteretic control, the switching frequency is a function of the input voltage, the output voltage, the hysteresis window, the delay of the hysteresis comparator and the driver, the output inductance, the resistance in the output inductor, the output capacitance, the ESR and ESL in the output capacitor, the output current, and the turnon resistance of high side and low side MOSFET. It is a very complex equation if everything is included. To make it more useful to the designers, a simplified equation only considers the most influential factors. The tolerance of this equation is about 30%:

$$fs = \frac{V_{out} \times (V_{in} - V_{out}) \times (ESR - (10 \times 10^{-7} + Td)/C_{out})}{V_{in} \times (V_{in} \times ESR \times (10 \times 10^{-7} + Td) + 0.0097 \times L_{out} - ESL \times V_{in})}$$

Where *fs* is the switching frequency (Hz); *Vout* is the output voltage (V); *Vin* is the input voltage (V); *Cout* is the output capacitance; *ESR* is the equivalent series resistance in the output capacitor (Ω); *ESL* is the equivalent series inductance in the output capacitor (H); *Lout* is the output inductance (H); *Td* is output feedback RC filter time constant (S).

In the EVM module design, for the 1.8 V output, for example: Vin = 5 V, Vout = 1.8 V, Cout = 680 µF; ESR = 40 mΩ; ESL = 3 nH; Lout = 6 µH; Td = 0.5 µs.

Then, the frequency *fs = 122 kHz.*

output inductor ripple current

The output inductor current ripple can affect not only the efficiency and the inductor saturation, but also the output voltage capacitor selection. The equation is exhibited as below:

$$Iripple = \frac{Vin - Vout - Iout \times (Rdson + RL)}{Lout} \times D \times Ts$$

Where *Iripple* is the peak-to-peak ripple current (A) through inductor; *Vin* is the input voltage (V); *Vout* is the output voltage (V); *Iout* is the output current; *Rdson* is the on-time resistance of MOSFET (Ω); *D* is the duty cycle; and *Ts* is the switching cycle (S). From the equation, it can be seen that the current ripple can be adjusted by changing the output inductor value.

Example: Vin = 5 V; Vout = 1.8 V; Iout = 5 A; Rdson = 10 mΩ; RL = 5 mΩ; D = 0.36; Ts = 10 µS; Lout = 6 µH

Then, the ripple Iripple = 2 A.

output capacitor RMS current

Assuming the inductor ripple current totally goes through the output capacitor to the ground, the RMS current in the output capacitor can be calculated as:

$$I_o(rms) = \frac{\Delta I}{\sqrt{12}}$$

Where *I(orms)* is the maximum RMS current in the output capacitor (A); *ΔI* is the peak-to-peak inductor ripple current (A).

Example: ΔI = 2 A, so Io(rms) = 0.58 A

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input capacitor RMS current

Assuming the input ripple current totally goes into the input capacitor to the power ground, the RMS current in the input capacitor can be calculated as:

$$I_i(rms) = \sqrt{I_o^2 \times D \times (1 - D) + \frac{1}{12} \times D \times Iripple^2}$$

Where *Ii(rms)* is the input RMS current in the input capacitor (A); *Io* is the output current (A); *D* is the duty cycle. From the equation, it can be seen that the highest input RMS current usually occurs at the lowest input voltage, so it is the worst case design for input capacitor ripple current.

Example: Io = 5 A; D = 0.36

Then, Ii(rms)= 3.36 A

softstart

The softstart timing can be adjusted by selecting the soft-start capacitor value. The equation is

$$C_{soft} = 2 \times T_{soft}$$

Where C_{soft} is the softstart capacitance (μF); T_{soft} is the start-up time on softstart terminal (S).

Example: Tsoft = 5 mS, so Csoft = 0.01 μF.

current protection

The current protection in TPS5103 is set using an internal current source and an external resistor to set up the current limit. The sensed high side MOSFET drain-to-source voltage drop is compared to the set point, if the voltage drop exceeds the limit, the internal oscillator is activated, and it continuously resets the current limit until the over-current condition is removed. The equation below should be used for calculating the external resistor value for current protection:

PWM or HYS mode $$Rcl = \frac{Rds(on) \times (Itrip + Iind(p\text{-}p)/2)}{0.000015}$$

SKIP mode $$Rcl = \frac{Rds(on) \times (Itrip + Iind(p\text{-}p)/2)}{0.000005}$$

Where Rcl is the external current limit resistor (R10,R11); Rds(on) is the high side MOSFET on-time resistance. Itrip is the required current limit; Iind(p-p) is the peak-to-peak output inductor current.

Example: PWM mode or HYS mode

Rds(on) = 10 mΩ, Itrip =5 A, Iind = 2 A, so Rcl = 4 kΩ

Example: SKIP mode

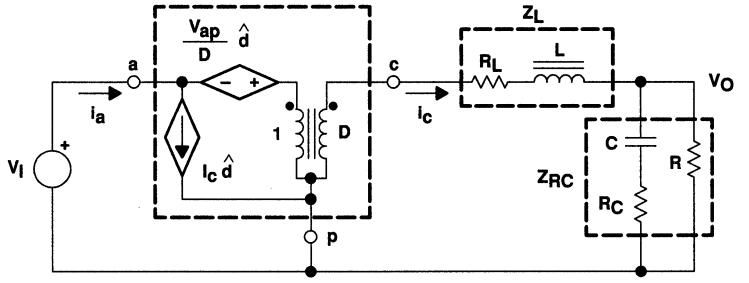
Rds(on) = 10 mΩ, Itrip = 2 A, Iind = 1 A, so Rcl = 5 kΩ

APPLICATION INFORMATION

loop gain compensation

Voltage mode control is used in this controller for the output voltage regulation. To achieve fast, stabilized control, two parts are discussed in this section: the power stage small signal modeling and the compensation circuit design.

For the buck converter, the small signal modeling circuit is shown below:



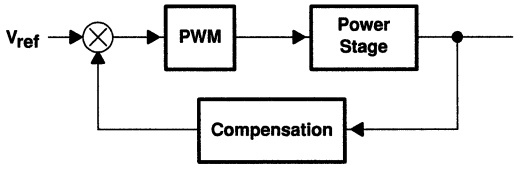
From this equivalent circuit, several control transfer functions can be derived: input-to-output, output impedance, and control-to-output. Typically the control-to-output transfer function is used for the feedback control design.

Assuming Rc and RL are much smaller than R, the simplified small signal control-to-output transfer function is:

$$\frac{\hat{V}od}{\hat{d}} = \frac{(1 + sCRc)}{1 + s\left[C \times \left(Rc + R_L\right) + \frac{L}{R}\right] + s^2LC}$$

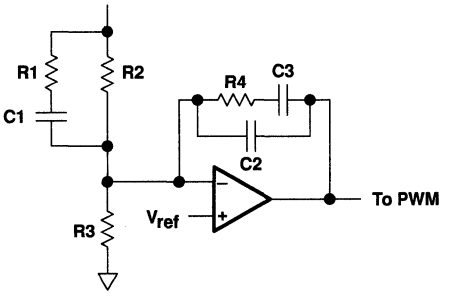
Where C is the output capacitance; Rc is the equivalent serial resistance (ESR) in the output capacitor; L is the output inductor; RL is the equivalent serial resistance (ESR) in the output inductor; R is the load resistance.

To achieve the fast transient response and the better output voltage regulation, a compensation circuit is added to improve the feedback control. The whole system is shown below:



APPLICATION INFORMATION

The typical compensation circuit used as an option in the EVM design is a part of the output feedback circuit. The circuitry is displayed below.



This circuit is composed of one integrator, two poles, and two zeros:

Assuming R1 << R2 and C2 << C3, the equation is:

$$\text{Comp} = \frac{(1 + sC3R4) \times (1 + sC2R2)}{sC3R2(1 + sC2R4)(1 + sC1R1)}$$

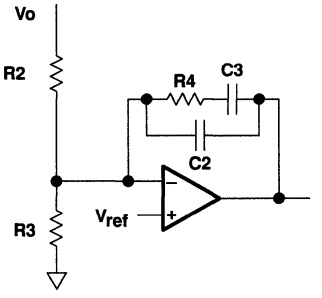
Therefore,

$$\text{Pole1} = \frac{1}{2\pi C1R1} \qquad \text{Pole2} = \frac{1}{2\pi C2R4}$$

$$\text{Zero2} = \frac{1}{2\pi C3R4} \qquad \text{Zero1} = \frac{1}{2\pi C2R2}$$

$$\text{Integrator} = \frac{1}{2\pi f C3R2}$$

A simplified version used in the EVM design is exhibited below.



Assuming C2 << C3, the equation is:

$$\text{Comp} = \frac{(1 + sC3R4)}{sC3R2(1 + sC2R4)}$$

APPLICATION INFORMATION

there is one pole, one zero and one integrator:

$$\text{Zero} = \frac{1}{2\pi C3R4} \qquad \text{Pole} = \frac{1}{2\pi C2R4} \qquad \text{Integrator} = \frac{1}{2\pi f C3R2}$$

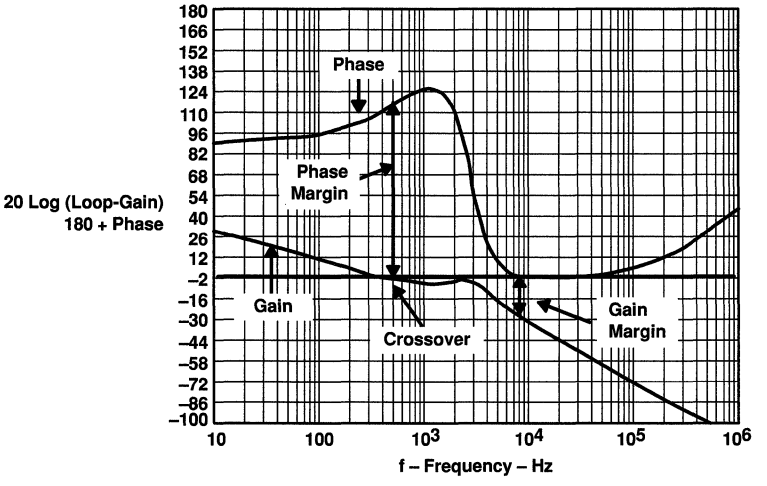
The loop-gain concept is used to design a stable and fast feedback control. The loop-gain equation is derived by that the control-to-output transfer function times the compensation:

$$\text{Loop} - \text{gain} = \text{Vod X Comp}$$

By using a bode plot, the amplitude and the phase of this equation can be drawn with software such as MathCad. In turn, the stability can be easily designed by adjusting the compensation perimeters. The sample bode plot is shown below to explain the phase margin, gain margin and the crossover frequency.

The gain is drawn as 20 log (loop-gain), and the phase is in degrees. To explain them clearer, 180 degrees is added to the phase, so that the gain and phase share the same zero.

Where the gain curve touches the zero is the crossover frequency. The higher this frequency is, the faster the transient response is, since the transient recovery time is 1/(crossover frequency). The phase to the zero is the phase margin at the crossover frequency. The phase margin should be at least 60 degrees to cover all the condition changes such as temperature. The gain margin is the gap between gain curve and the zero when the phase curve touches the zero. This margin should be at least 20 dB to guarantee the stability over all conditions.

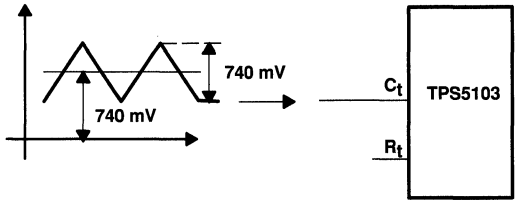


APPLICATION INFORMATION

synchronization

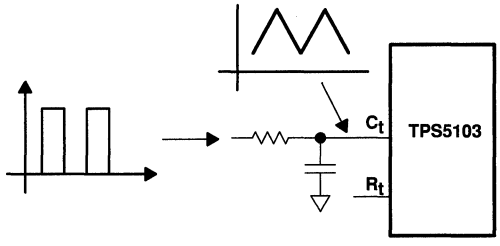
Some applications require switching clock synchronization. Two methods are used for synchronization:

- Triangle wave synchronization



- Square wave synchronization

It can be seen that R_T and C_T are removed from the circuit. Therefore, two components are saved. This method is good for the synchronization between two controllers. If the controller needs to be synchronized with digital circuit such as DSP, usually the square-type clock signal is used. The configuration exhibited below is for this type of application:



An external resistor is added into the circuit, but R_T is still removed. C_T is kept to be a part of RC circuit generating triangle waveform for the controller. Assuming the peak value of the square is known, the resistor and the capacitor can be adjusted to achieve the correct peak–to–peak value and the offset value.

layout guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, place the low-level components. Below are several specific points to consider before layout of a TPS5103 design begins.

- All sensitive analog components should be referenced to ANAGND. These include components connected to Vref5, Vref, INV, LH, and COMP .
- Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.

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- Connections from the drivers to the gate of the power FETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
- The bypass capacitor for V_{CC} should be placed close to the TPS5103.
- When configuring the high-side driver as a floating driver, the connection from LL to the power FETs should be as short and as wide as possible.
- When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from LH to LL) should be placed close to the TPS5103.
- When configuring the high-side driver as a ground-referenced driver, LL should be connected to DRVGND.
- The bulk storage capacitors across V_{IN} should be placed close to the power FETS. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
- High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
- LH and LL should be connected very close to the drain and source, respectively, of the high-side FET. LH and LL should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed close to where V_{CC} connects to V_{in}, to reduce high-frequency noise coupling on V_{CC}.
- The output voltage sensing trace should be isolated by either ground trace or V_{CC} trace.

test results

The tests are conducted at T_A = 25°C, the point voltage is 5 V.

APPLICATION INFORMATION

EFFICIENCY
vs
OUTPUT CURRENT

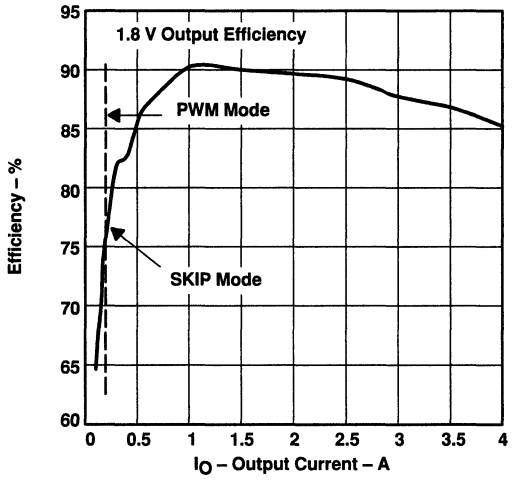


Figure 37

EFFICIENCY
vs
OUTPUT CURRENT

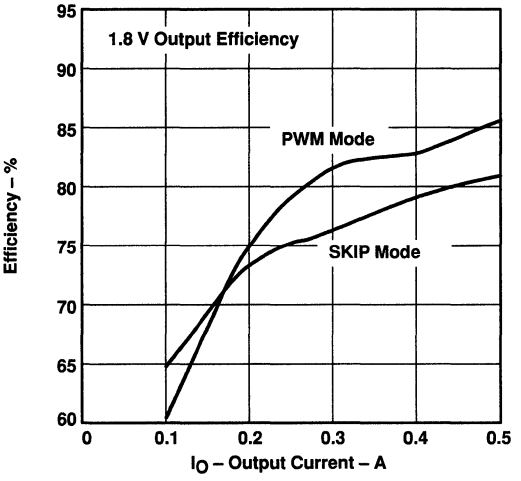


Figure 38

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

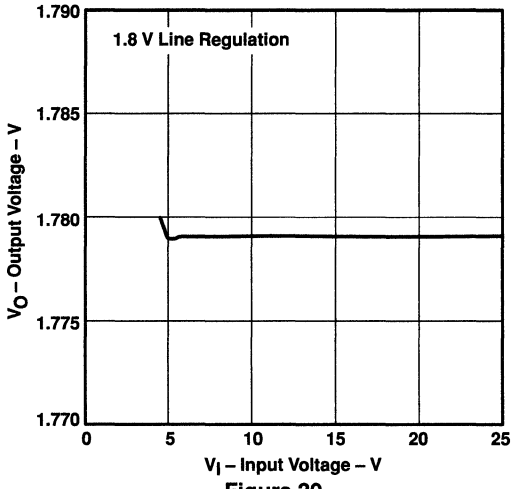


Figure 39

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

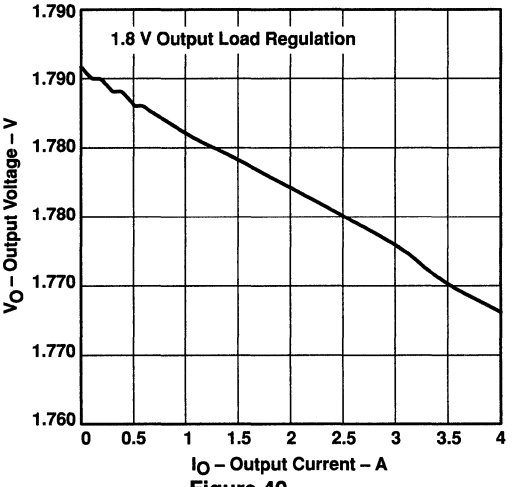


Figure 40

EFFICIENCY
vs
OUTPUT CURRENT

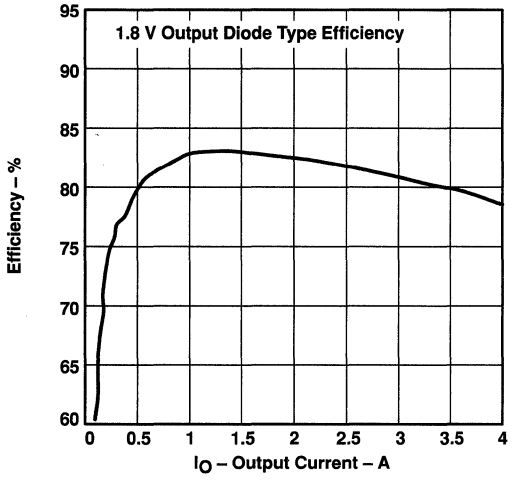


Figure 41

OUTPUT/VOLTAGE

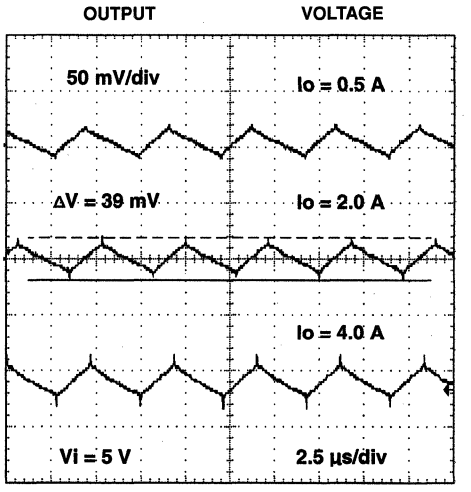


Figure 42

TRANSIENT RESPONSE (OVERSHOOT)

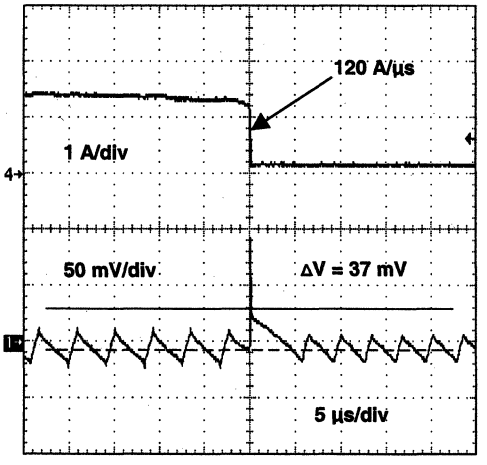


Figure 43

TRANSIENT RESPONSE (UNDERSHOOT)

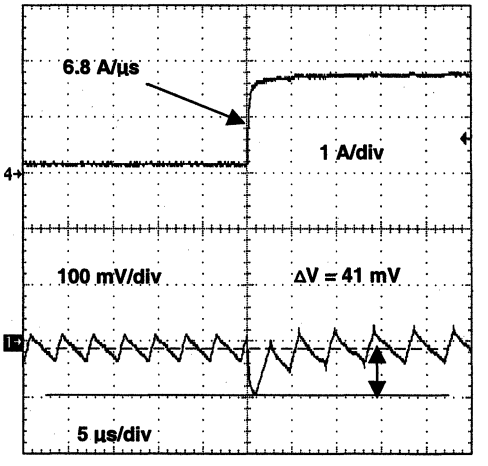


Figure 44

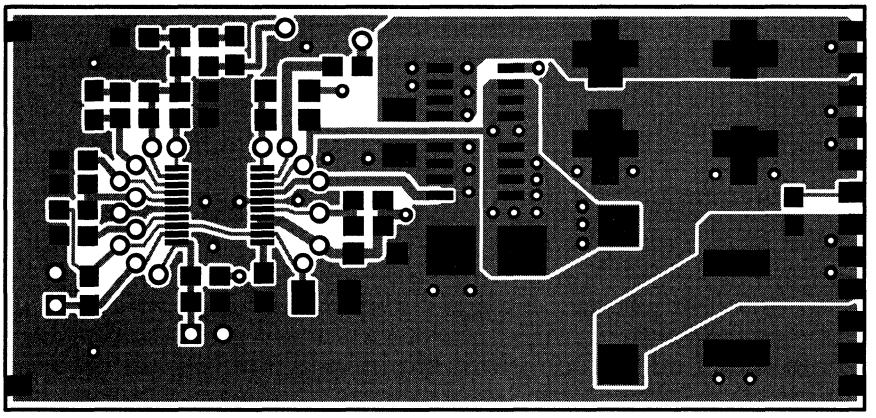
APPLICATION INFORMATION

Table 1. Bill of Materials (see Note 3)

REF	PN	DESCRIPTION	MFG	SIZE
C1opt	10TPB220M	Capacitor, POSCAP, 220 µF, 10 V	Sanyo	7.3x4.3mm
C1	RV-35V221MH10-R	Capacitor, electrolytic, 220 µF, 35 V	ELNA	10x10mm
C2	GMK325F106ZH	Capacitor, ceramic, 10 µF, 35 V	Taiyo Yuden	1210
C3	4TPB470M	Capacitor, POSCAP, 470 µF, 4 V	Sanyo	7.3x4.3mm
C4†	std	Open, capacitor, Ceramic, 2.2 µF, 16 V		805
C5	std	Capacitor, ceramic, 1 µF, 16 V		805
C6	std	Capacitor, ceramic, 0.01 µF, 16 V		805
C7	std	Capacitor, ceramic, 220 pF, 16 V		805
C8	std	Capacitor, ceramic, 100 pF, 16 V		805
C9	std	Capacitor, ceramic, 1 µF, 16 V		805
C10	GMK316F225ZG	Capacitor, ceramic, 2.2 µF, 35 V	Taiyo Yuden	1206
C11†	std	Open		805
C12	GMK316F225ZG	Capacitor, Ceramic, 2.2 µF, 35 V	Taiyo Yuden	1206
C13	GMK325F106ZH	Capacitor, Ceramic, 10 µF, 35 V	Taiyo Yuden	1210
C14		Open		
C14†opt		Open		10x10mm
C15†	std	Open, capacitor, ceramic, 1000 pF, 16 V		805
D1	MBRS340T3	Diode, Schottky, 40 V, 3 A	Motorola	SMC
D1opt	MBRS130LT3	Diode, Schottky, 30 V, 1 A	Motorola	SMB
D2	SD103-AWDICT-ND	Diode, Schottky, 40 V, 200 mA, 400 mW	Digikey	3.5x1.5mm
L1	DO3316P-682	Inductor, 6.8 uH, 4.4 A	Coilcraft	0.5x0.37 in
J1–J14	CA26DA-D36W-0FC	Edge connector, surface-mount, 0.040" board, 0.090" standoff	NAS Interplex	0.040"
JP1	S1132-2-ND	Header, straight, 2–pin, 0.1 ctrs, 0.3" pins	Sullins	DigiKey # S1132-2-ND
JP1 Shunt	929950-00-ND	Shunt, jumper, 0.1"	3M	DigiKey #929950-00-ND
JP2	S1132-2-ND	Header, straight, 2–pin, 0.1 ctrs, 0.3" pins	Sullins	DigiKey #S1132-2-ND
R1	std	Resistor, 5.1 kΩ, 5 %		805
R2†	std	Open, resistor, 1 kΩ, 5%		805
R3	std	Resistor, 910 Ω, 1%		805
R4	std	Resistor, 1.74 kΩ, 1%		805
R5	std	Resistor, 5.1 kΩ, 5%		805
R6A	std	Resistor, 82 kΩ, 5%		805
R6B†	std	Open, 0 Ω, 5%		805
R7	std	Resistor, 1 kΩ, 5%		805
R9	std	Resistor, 1 kΩ, 5%		805
R10	std	Resistor, 1 kΩ, 5%		805
R11	std	Resistor, 10 Ω, 5%		805
R12	std	Resistor, 51 kΩ, 5%		805
R13†	std	Open		805
Q1	Si4410DY	Transistor, MOSFET, n-ch, 30-V, 10-A, 13–mΩ	Siliconix	SO–8
Q2	Si4410DY	Transistor, MOSFET, n-ch, 30-V, 10-A, 13-mΩ	Siliconix	SO–8
U1	TPS5103	IC, controller	TI	SSOP–20

† Components for optional mode test only.
NOTE 3: This operation mode is PWM mode only.

APPLICATION INFORMATION



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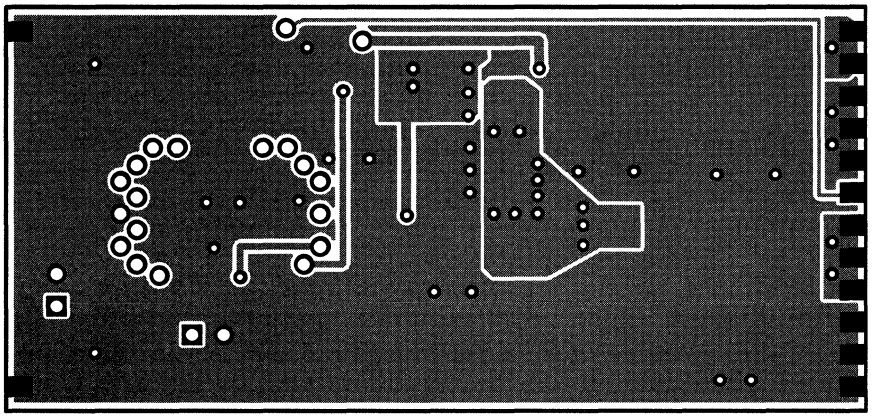
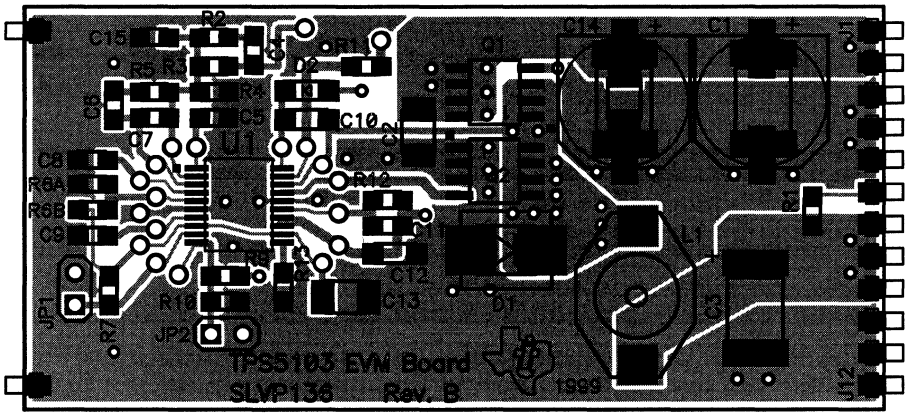
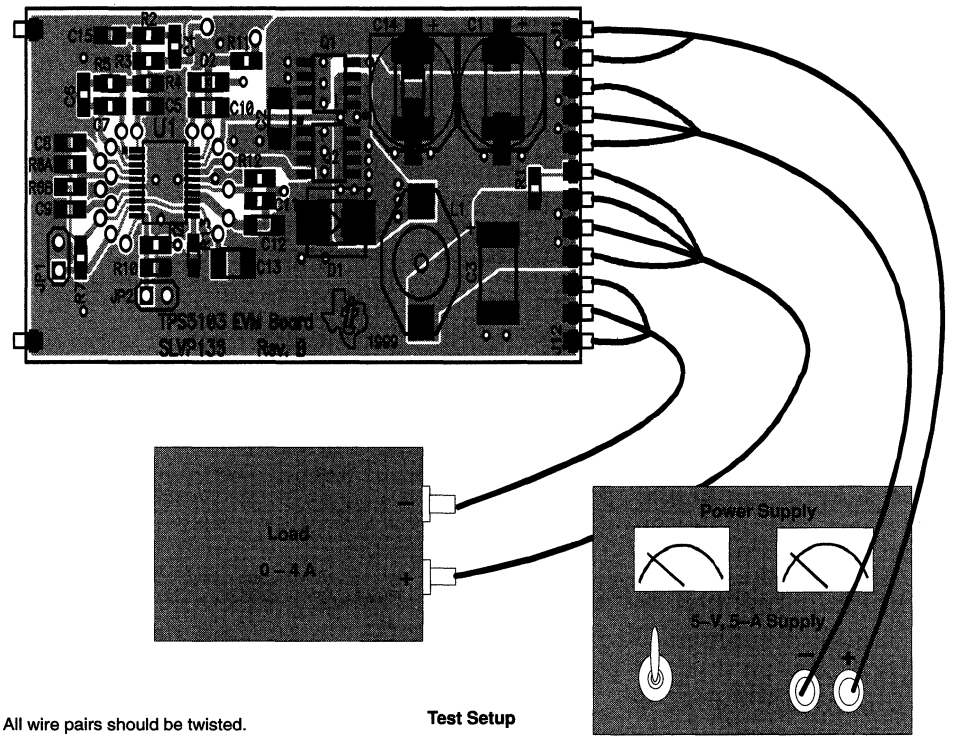


Bottom Layer (Top View)

APPLICATION INFORMATION



Top Assembly



NOTE: All wire pairs should be twisted.

Test Setup

APPLICATION INFORMATION

Table 2. Test Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range		5		25	V
Output voltage range	Vi = 5 – 25 V Io = 0 – 4 A	1.7	1.8	1.9	V
Output current range	Vi = 5 – 10 V	0		4	A
Output current limit	Vi = 5 V	4.3			A
Output ripple	Vi =5 V, Io = 4 A			50	mVp–p
Operating frequency	Io = 4 A	150		250	KHz
Efficiency	Vi = 5 V, Vo = 1.8 V, Io = 4 A		90		%

Table 3. EVM Operating Specifications

SKIP MODE	HYS MODE
Remove JP1 shunt	Remove R5, C6 and C7
	Remove R6A
	Add R6B
	Add C15
	If it needs the loop-compensation, add R2 and C4

This EVM is designed to cover as many applications as possible. For some more specific applications, the circuit can be simpler. The table below gives some recommendations.

Table 4. EVM Application Recommendations

5-V INPUT VOLTAGE	<3-A OUTPUT CURRENT	DIODE VERSION
Change C1 to low profile capacitor Sanyo 10TPB220M (220 µF, 10 V) Or 6TPB330M (330 µF, 6.3 V)	Change Q1 and Q2 to dual pack MOSFET, IRF7311 to reduce the cost.	Remove Q2 to reduce the cost.
Remove R10		

Table 5. Vendor and Source Information

MATERIAL	SOURCE	PART NUMBER	DISTRIBUTORS
MOSFETS (Q1–Q2)	In EVM design	Si4410	Local distributor
	Second source	IRF7811 (International Rectifier)	
INPUT CAPACITORS (C1)	In EVM design	RV–35V221MH10–R (ELNA)	Bell Microproducts 972–783–4191
	Second source	35CV330AX/GX (Sanyo)	870–633–5030
		UUR1V221MNR1GS (Nichicon)	Future Electronics (Local Office)
MAIN DIODES (D1)	In EVM design	MBRS340T3 (Motorola)	Local distributors
	Second source	U3FWJ44N (Toshiba)	Local distributors
INDUCTORS (L1)	In EVM design	DO3316P–682 (Coilcraft)	972–458–2645
	Second source	CTDO3316P–682 (Inductor Warehouse)	800–533–8295
CERAMIC CAPACITORS (C2, C14) (C12, C10)	IN EVM design	GMK325F106ZH GMK316F225ZG (Taiyo Yuden)	SMEC 512–331–1877
	Taiyo Yuden representative		e–mail: mike@millsales.com

APPLICATION INFORMATION

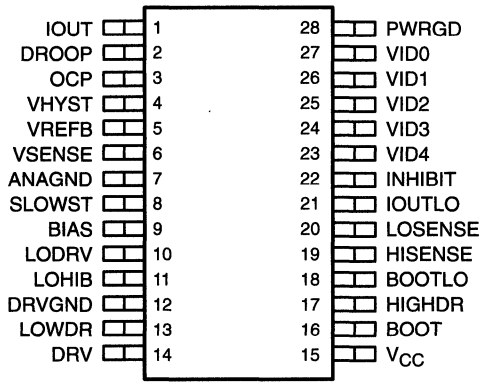
High current applications are described in Table 6. The values are recommendations based on actual test circuits. Many variations are possible based on the requirements of the user. Performance of the circuit is dependent upon the layout rather than on the specific components, if the device parameters are not exceeded. The power stage, having the highest current levels and greatest dv/dt rates, should be given the most attention, as both the supply and load can be severely affected by the power levels and edge rates.

Table 6. High Current Applications

REFERENCE DESIGNATIONS	FUNCTION	8-A OUTPUT	12-A OUTPUT	16-A OUTPUT
C1	Input bulk capacitor	2x ELNA RV-35V221MH10-R 220 µF, 35 V	3x ELNA RV-35V221MH10-R 220 µF, 35 V	4x ELNA RV-35V221MH10-R 220 µF, 35 V
C2	Input bypass capacitor	2x Taiyo Yuden GMK325F106ZH 10 µF, 35 V	3x Taiyo Yuden GMK325F106ZH 10 µF, 35 V	4x Taiyo Yuden GMK325F106ZH 10 µF, 35 V
L1	Output filter indicator	Coiltronics UP3B-2R2 2.2 µH, 9.2 A	Coiltronics UP4B-1R5 1.5 µH, 13.4 A	MicorMetals T68-8/90 Core w/7T, #16 1.0 µH, 25 A
C3	Output filter capacitor	2x Sanyo 4TPB470M 470 µF, 4 V	3x Sanyo 4TPB470M 470 µF, 4 V	4x Sanyo 4TPB470M 470 µF, 4 V
Q1	Power switch	2x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	3x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	4x Siliconix Si4410DY 30 V, 10 A, 13 mΩ
Q2	Power switch	2x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	3x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	4x Siliconix Si4410DY 30 V, 10 A, 13 mΩ
R11	Gate drive resistor	7 Ω	5 Ω	4 Ω
R12	Current limit resistor	10 kΩ	15 kΩ	20 kΩ
Switching frequency		200 kHz	150 kHz	100 kHz

- **700 KHz Operation**
- **1.25 MHz Operation With External Driver**
- **1.5% Reference Over Full Operating Temperature Range**
- **Synchronous Rectifier Driver for Greater Than 90% Efficiency**
- **Programmable Reference Voltage Range of 1.3 V to 3.5 V**
- **User–Selectable Hysteretic Type Control**
- **Droop Compensation for Improved Load Transient Regulation**
- **Adjustable Overcurrent Protection**
- **Programmable Softstart**
- **Overvoltage Protection**
- **Active Deadtime Control**
- **Power Good Output**
- **Internal Bootstrap Schottky Diode**
- **Low Supply Current . . . 3-mA Typ**
- **Reduced System Component Count and Size**

PWP PACKAGE
(TOP VIEW)



description

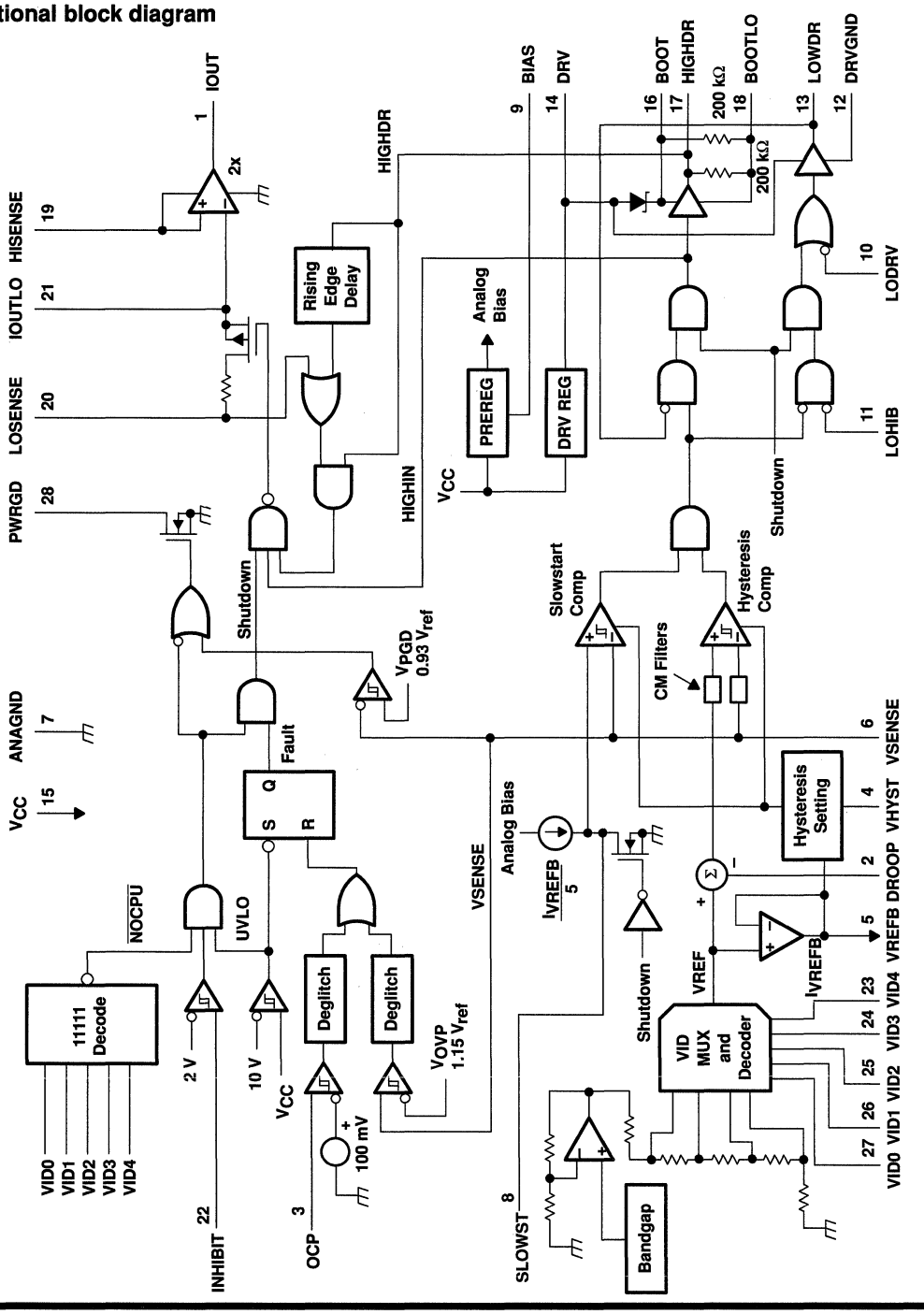
The TPS5211 is a hysteretic regulator controller which provides an accurate, programmable supply voltage to microprocessors. An internal 5-bit DAC is used to program the reference voltage to within a range of 1.3 V to 3.5 V. The output voltage can be set to equal the reference voltage or some multiple of the reference voltage. A hysteretic controller with user-selectable hysteresis and programmable droop compensation is used to dramatically reduce overshoot and undershoot caused by load transients. Propagation delay from the comparator inputs to the output drivers is less than 250 ns. Overcurrent shutdown and crossover protection for the output drivers combine to eliminate destructive faults in the output FETs. The softstart current source is proportional to the reference voltage, thereby eliminating variation of the softstart timing when changes are made to the output voltage. PWRGD monitors the output voltage and pulls the open-collector output low when the output drops 7% below the nominal output voltage. An overvoltage circuit disables the output drivers if the output voltage rises 15% above the nominal value. The inhibit pin can be used to control power sequencing. Inhibit and undervoltage lockout assures the 12-V supply voltage and system supply voltage (5 V or 3.3 V) is within proper operating limits before the controller starts. Single-supply (12 V) operation is easily accomplished using a low-current divider for the required 5-V signals. The output driver circuits include 2-A drivers with internal 8-V gate-voltage regulators. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. The TPS5211 is available in a 28-pin TSSOP PowerPAD™ package. It operates over a junction temperature range of 0°C to 125°C.

AVAILABLE OPTIONS

T_J	PACKAGE
	TSSOP (PWP)
0°C to 125°C	TPS5211PWPR

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANAGND	7		Analog ground
BIAS	9	O	Analog BIAS pin. A 1-μF ceramic capacitor should be connected from BIAS to ANAGND.
BOOT	16	I	Bootstrap. Connect a 1-μF low-ESR capacitor from BOOT to BOOTLO.
BOOTLO	18	O	Bootstrap low. Connect BOOTLO to the junction of the high-side and low-side FETs for floating drive configuration. Connect BOOTLO to PGND for ground reference drive configuration.
DROOP	2	I	Droop voltage. Voltage input used to set the amount of output-voltage set-point droop as a function of load current. The amount of droop compensation is set with a resistor divider between IOUT and ANAGND.
DRV	14	O	Drive regulator for the FET drivers. A 1-μF ceramic capacitor should be connected from DRV to DRVGND.
DRVGND	12		Drive ground. Ground for FET drivers. Connect to FET PWRGND.
HIGHDR	17	O	High drive. Output drive to high-side power switching FETs
HISENSE	19	I	High current sense. For current sensing across high-side FETs, connect to the drain of the high-side FETs; for optional resistor sensing scheme, connect to power supply side of current-sense resistor placed in series with high-side FET drain.
INHIBIT	22	I	Disables the drive signals to the MOSFET drivers. Can also serve as UVLO for system logic supply (either 3.3 V or 5 V).
IOUT	1	O	Current out. Output voltage on this pin is proportional to the load current as measured across the Rds(on) of the high-side FETs. The voltage on this pin equals $2 \times Rds(on) \times IOUT$. In applications requiring very accurate current sensing, a sense resistor should be connected between the input supply and the drain of the high-side FETs.
IOUTLO	21	O	Current sense low output. This is the voltage on the LOSENSE pin when the high-side FETs are on. A ceramic capacitor should be connected from IOUTLO to HISENSE to hold the sensed voltage while the high-side FETs are off. Capacitance range should be between 0.033 μF and 0.1 μF.
LODRV	10	I	Low drive enable. Normally tied to 5 V. To activate the low-side FETs as a crowbar, pull LODRV low.
LOHIB	11	I	Low side inhibit. Connect to the junction of the high and low side FETs to control the anti-cross-conduction and eliminate shoot-through current. Disabled when configured in crowbar mode.
LOSENSE	20	I	Low current sense. For current sensing across high-side FETs, connect to the source of the high-side FETs; for optional resistor sensing scheme, connect to high-side FET drain side of current-sense resistor placed in series with high-side FET drain.
LOWDR	13	O	Low drive. Output drive to synchronous rectifier FETs
OCP	3	I	Over current protection. Current limit trip point is set with a resistor divider between IOUT and ANAGND.
PWRGD	28	O	Power good. Power good signal goes high when output voltage is within 7% of voltage set by VID pins. Open-drain output.
SLOWST	8	O	Slowstart (soft start). A capacitor from SLOWST to ANAGND sets the slowstart time. Slowstart current = $I_{VREFB}/5$
V_{CC}	15		12-V supply. A 1-μF ceramic capacitor should be connected from V_{CC} to DRVGND.
VHYST	4	I	HYSTERESIS set pin. The hysteresis is set with a resistor divider from V_{REFB} to ANAGND. The hysteresis window = $2 \times (V_{REFB} - V_{HYST})$
VID0	27	I	Voltage identification input 0
VID1	26	I	Voltage identification input 1
VID2	25	I	Voltage identification input 2
VID3	24	I	Voltage identification input 3
VID4	23	I	Voltage Identification input 4. Digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in Table 1. Internally pulled up to 5 V with a resistor divider biased from V_{CC}.
VREFB	5	O	Buffered reference voltage from VID network
VSENSE	6	I	Voltage sense input. To be connected to converter output voltage bus to sense and control output voltage. It is recommended an RC low pass filter be connected at this pin to filter noise.

detailed description

V_{REF}

The reference/voltage identification (VID) section consists of a temperature-compensated bandgap reference and a 5-bit voltage selection network. The 5 VID terminals are inputs to the VID selection network and are TTL-compatible inputs internally pulled up to 5 V by a resistor divider connected to V_{CC}. The VID codes conform to the Intel *VRM 8.3 DC-DC Converter Specification* for voltage settings between 1.8 V and 3.5 V, and they are decremented by 50 mV, down to 1.3 V, for the lower VID settings. Voltages higher than V_{REF} can be implemented using an external divider. Refer to Table 1 for the VID code settings. The output voltage of the VID network, V_{REF}, is within ±1.5% of the nominal setting over the VID range of 1.3 V to 2.5 V, including a junction temperature range of 5°C to +125°C, and a V_{CC} supply voltage range of 11.4 V to 12.6 V. The output of the reference/VID network is indirectly brought out through a buffer to the V_{REFB} pin. The voltage on this pin will be within 5mV of V_{REF}. It is not recommended to drive loads with V_{REFB}, other than setting the hysteresis of the hysteretic comparator, because the current drawn from V_{REFB} sets the charging current for the slowstart capacitor. Refer to the slowstart section for additional information.

hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by 2 external resistors and is centered on V_{REF}. The 2 external resistors form a resistor divider from V_{REFB} to ANAGND, with the output voltage connecting to the VHYST pin. The hysteresis of the comparator will be equal to twice the voltage *difference* between the VREFB and VHYST pins. The propagation delay from the comparator inputs to the driver outputs is 250 ns (maximum). The maximum hysteresis setting is 60 mV.

low-side driver

The low-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The bias to the low-side driver is internally connected to the DRV regulator.

high-side driver

The high-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from the DRV regulator. The internal bootstrap diode, connected between the DRV and BOOT pins, is a Schottky for improved drive efficiency. The maximum voltage that can be applied between BOOT and DRVGND is 30 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting BOOT to either DRV or V_{CC}. The rms current through the drivers output should not exceed 110 mA. Refer to the application information section to determine how to calculate an operating frequency to meet this requirement.

deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate-drive voltage to the low-side FETs is below 2 V; the low-side driver is not allowed to turn on until the voltage at the junction of the high-side and low-side FETs (Vphase) is below 2 V.

detailed description (continued)

current sensing

Current sensing is achieved by sampling and holding the voltage across the high-side power FETs while the high-side FETs are on. The sampling network consists of an internal 60-Ω switch and an external ceramic hold capacitor. Recommended value of the hold capacitor is between 0.033 µF and 0.1 µF. Internal logic controls the turnon and turnoff of the sample/hold switch such that the switch does not turn on until the Vphase voltage transitions high, and the switch turns off when the input to the high-side driver goes low. The sampling will occur only when the high-side FETs are conducting current. The voltage on the IOUT pin equals 2 times the sensed

high-side voltage. In applications where a higher accuracy in current sensing is required, a sense resistor can be placed in series with the high-side FETs, and the voltage across the sense resistor can be sampled by the current sensing circuit.

droop compensation

The droop compensation network reduces the load transient overshoot/undershoot on V_O, relative to V_{REF}. V_O is programmed to a voltage greater than V_{REF} by an external resistor divider from V_O to VSENSE to reduce the undershoot on V_O during a low-to-high load transient. The overshoot during a high-to-low load transient is reduced by subtracting the voltage on DROOP from V_{REF}. The voltage on IOUT is divided with an external resistor divider, and connected to DROOP.

inhibit

INHIBIT is a TTL-compatible digital input used to enable the controller. When INHIBIT is low, the output drivers are low and the slowstart capacitor is discharged. When INHIBIT goes high, the short across the slowstart capacitor is released and normal converter operation begins. When the system-logic supply is connected to INHIBIT, it also controls power sequencing by locking out controller operation until the system-logic supply exceeds the input threshold voltage of the inhibit circuit. The 12-V supply and the system logic supply (either 5 V or 3.3 V) must be above UVLO thresholds before the controller is allowed to start up. The start threshold is 2.1 V and the hysteresis is 100 mV for the INHIBIT comparator.

V_{CC} undervoltage lockout (UVLO)

The undervoltage lockout circuit disables the controller while the V_{CC} supply is below the 10-V start threshold during power up. When the controller is disabled, the output drivers will be low and the slowstart capacitor is discharged. When V_{CC} exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 2-V hysteresis in the undervoltage lockout circuit for noise immunity.

slowstart

The slowstart circuit controls the rate at which V_O powers up. A capacitor is connected between SLOWST and ANAGND and is charged by an internal current source. The current source is proportional to the reference voltage, so that the charging rate of C_{SLOWST} is proportional to the reference voltage. By making the charging current proportional to V_{REF}, the power-up time for V_O will be independent of V_{REF}. Thus, C_{SLOWST} can remain the same value for all VID settings. The slowstart charging current is determined by the following equation:

$$I_{slowstart} = I(VREFB) / 5 \quad \text{(amps)}$$

Where I(VREFB) is the current flowing out of VREFB.

It is recommended that no additional loads be connected to VREFB, other than the resistor divider for setting the hysteresis voltage. The maximum current that can be sourced by the VREFB circuit is 500 μA. The equation for setting the slowstart time is:

$$t_{SLOWST} = 5 \times C_{SLOWST} \times R_{VREFB} \quad \text{(seconds)}$$

Where R_{VREFB} is the total external resistance from V_{REFB} to ANAGND.

detailed description (continued)

power good

The power-good circuit monitors for an undervoltage condition on V_O. If V_O is 7% below V_{REF}, then the PWRGD pin is pulled low. PWRGD is an open-drain output.

overvoltage protection

The overvoltage protection (OVP) circuit monitors V_O for an overvoltage condition. If V_O is 15% above V_{REF}, then a fault latch is set and both output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value. A 3-µs deglitch timer is included for noise immunity. Refer to the LODRV section for information on how to protect the microprocessor against overvoltages due to a shorted fault across the high-side power FET.

overcurrent protection

The overcurrent protection (OCP) circuit monitors the current through the high-side FET. The overcurrent threshold is adjustable with an external resistor divider between IOUT and ANAGND, with the divider voltage connected to the OCP pin. If the voltage on OCP exceeds 100 mV, then a fault latch is set and the output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value. A 3-µs deglitch timer is included for noise immunity. The OCP circuit is also designed to protect the high-side power FET against a short-to-ground fault on the terminal common to both power FETs.

drive regulator

The drive regulator provides drive voltage to the output drivers. The minimum drive voltage is 7 V. The minimum short circuit current is 100 mA. Connect a 1-µF ceramic capacitor from DRV to DRVGND.

LODRV

The LODRV circuit is designed to protect the microprocessor against overvoltages that can occur if the high-side power FETs become shorted. External components to sense an overvoltage condition are required to use this feature. When an overvoltage fault occurs, the low-side FETs are used as a crowbar. LODRV is pulled low and the low-side FET will be turned on, overriding all control signals inside the TPS5211 controller. The crowbar action will short the input supply to ground through the faulted high-side FETs and the low-side FETs. A fuse in series with V_{in} should be added to disconnect the short-circuit.

Table 1. Voltage Identification Codes

VID TERMINALS (0 = GND, 1 = floating or pull-up to 5 V)					V_{REF}
VID4	VID3	VID2	VID1	VID0	(Vdc)
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90

Table 1. Voltage Identification Codes (Continued)

VID TERMINALS (0 = GND, 1 = floating or pull-up to 5 V)					V_{REF}
VID4	VID3	VID2	VID1	VID0	(Vdc)
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	No CPU
1	1	1	1	0	2.10
1	1	1	0	1	2.20
1	1	1	0	0	2.30
1	1	0	1	1	2.40
1	1	0	1	0	2.50
1	1	0	0	1	2.60
1	1	0	0	0	2.70
1	0	1	1	1	2.80
1	0	1	1	0	2.90
1	0	1	0	1	3.00
1	0	1	0	0	3.10
1	0	0	1	1	3.20
1	0	0	1	0	3.30
1	0	0	0	1	3.40
1	0	0	0	0	3.50

absolute maximum ratings over operating virtual junction temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note1) ..... –0.3 V to 14 V
Input voltage range: BOOT to DRVGND (High-side Driver ON) ..... –0.3 V to 30 V
BOOT to HIGHDRV ..... –0.3 V to 15 V
BOOT to BOOTLO ..... –0.3 V to 15 V
INHIBIT, VIDx, LODRV ..... –0.3 V to 7.3 V
PWRGD, OCP, DROOP ..... –0.3 V to 7 V
LOHIB, LOSENSE, IOUTLO, HISENSE ..... –0.3 V to 14 V
VSENSE ..... –0.3 V to 5 V
Voltage difference between ANAGND and DRVGND ..... ±0.5 V
Output current, V_{REFB} ..... 0.5 mA
Short circuit duration, DRV ..... Continuous
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... 0°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to ANAGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	1150 mW	11.5 mW/°C	630 mW	460 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	11.4	13	V
Input voltage, BOOT to DRVGND	0	28	V
Input voltage, BOOT to BOOTLO	0	13	V
Input voltage, INHIBIT, VIDx, LODRV, PWRGD, OCP, DROOP	0	6	V
Input voltage, LOHIB, LOSENSE, IOUTLO, HISENSE	0	13	V
Input voltage, VSENSE	0	4.5	V
Voltage difference between ANAGND and DRVGND	0	±0.2	V
Output current, V_{REFB}†	0	0.4	mA

† Not recommended to load V_{REFB} other than to set hystersis since I_{VREFB} sets slowstart time.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted)

reference/voltage identification

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Cumulative reference accuracy (see Note 2)	V_{CC} = 11.4 to 12.6 V, 1.3 V ≤ V_{REF} ≤ 3.5 V	–0.015		0.015	V/V
VIDx	High-level input voltage		2.25			V
VIDx	Low-level input voltage				1	V
V_{REFB}	Output voltage	I_{VREFB} = 50 µA	V_{REF}–5mV	V_{REF}	V_{REF}+5mV	V
	Output regulation	10 µA ≤ I_O ≤ 500 µA		2		mV
VIDx	Input resistance	VIDx = 0 V	36	73	95	kΩ
	Input pull-up voltage divider		4.8	4.9	5	V

NOTES: 2. Cumulative reference accuracy is the combined accuracy of the reference voltage and the input offset voltage of the hysteretic comparator. Cumulative accuracy equals the average of the high-level and low-level thresholds of the hysteretic comparator.
3. This parameter is ensured by design and is not production tested.

power good

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Undervoltage trip threshold		90	93	95	%V_{REF}
V_{OL}	Low-level output voltage	I_O = 5 mA		0.5	0.75	V
I_{OH}	High-level input current	V_{PWRGD} = 6 V		1		µA
V_{hys}	Hysteresis voltage		1.3	2.9	4.5	%V_{REF}

slowstart

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge current	V_{SLOWST} = 0.5 V, V_{VREFB} = 1.3 V, I_{VREFB} = 65 µA	10.4	13	15.6	µA
Discharge current	V_{SLOWST} = 1 V		3		mA
Comparator input offset voltage				10	mV
Comparator input bias current	See Note 3		10	100	nA
Comparator hysteresis		–7.5		7.5	mV

NOTE 3: This parameter is ensured by design and is not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

hysteretic comparator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	V_{DROOP} = 0 V (see Note 3)	–2.5		2.5	mV
Input bias current	See Note 3			500	nA
Hysteresis accuracy	$V_{REFB} - V_{HYST}$ = 15 mV (Hysteresis window = 30 mV)	–3.5		3.5	mV
Maximum hysteresis setting	$V_{REFB} - V_{HYST}$ = 30 mV		60		mV

NOTE 3: This parameter is ensured by design and is not production tested.

high-side VDS sensing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain				2		V/V
Initial accuracy		$V_{HISENSE}$ = 12 V, $V_{LOSENSE}$ = 11.9 V, Differential input to V_{ds} sensing amp = 100 mV	194		206	mV
IOUTLO	Sink current	5 V ≤ V_{IOUTLO} ≤ 13 V			250	nA
IOUT	Source current	V_{IOUT} = 0.5 V, $V_{HISENSE}$ = 12 V, V_{IOUTLO} = 11.5 V	500			µA
IOUT	Sink current	V_{IOUT} = 0.05 V, $V_{HISENSE}$ = 12 V, V_{IOUTLO} = 12 V	50			µA
Output voltage swing		$V_{HISENSE}$ = 11 V, R_{IOUT} = 10 kΩ	0		2	V
		$V_{HISENSE}$ = 4.5 V, R_{IOUT} = 10 kΩ	0		1.5	V
		$V_{HISENSE}$ = 3 V, R_{IOUT} = 10 kΩ	0		0.75	V
LOSENSE	High-level input voltage	$V_{HISENSE}$ = 4.5 V (see Note 3)	2.85			V
	Low-level input voltage				2.4	V
Sample/hold resistance		11.4 V ≤ $V_{HISENSE}$ ≤ 12.6 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V	50	60	80	Ω
		4.5 V ≤ $V_{HISENSE}$ ≤ 5.5 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V	62	85	123	
		3 V ≤ $V_{HISENSE}$ ≤ 3.6 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V	67	95	144	
CMRR		$V_{HISENSE}$ = 12.6 V to 3 V, $V_{HISENSE} - V_{OUTLO}$ = 100 mV	69	75		dB

NOTE 3. This parameter is ensured by design and is not production tested.

inhibit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		1.9	2.1	2.35	V
Hysteresis		0.08	0.1	0.12	V
Stop threshold		1.85			V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

overvoltage protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overvoltage trip threshold		112	115	120	$\%V_{REF}$
Hysteresis	See Note 3		10		mV

NOTE 3: This parameter is ensured by design and is not production tested.

overcurrent protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OCP trip threshold		90	100	110	mV
Input bias current				100	nA

deadtime

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOHIB	High-level input voltage		2.4			V
	Low-level input voltage				1.4	
LOWDR	High-level input voltage	See Note 3	3			V
	Low-level input voltage	See Note 3			1.7	

NOTE 3: This parameter is ensured by design and is not production tested.

LODRV

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LODRV	High-level input voltage		1.85			V
	Low-level input voltage				0.95	

droop compensation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial accuracy	V_{DROOP} = 50 mV	46		54	mV

drive regulator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	11.4 V ≤ V_{CC} ≤ 12.6 V, I_{DRV} = 120 mA	7		9	V
Output regulation	1 mA ≤ I_{DRV} ≤ 50 mA		100		mV
Short-circuit current		120			mA

bias regulator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	11.4 V ≤ V_{CC} ≤ 12.6 V, See Note 4	6			V

NOTE 4: The bias regulator is designed to provide a quiet bias supply for the TPS5211 controller. External loads should not be driven by the bias regulator.

input undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		9.25	10	10.75	V
Hysteresis		1.9	2	2.2	V
Stop threshold		7.5			V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

output drivers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output current (see Note 5)	High-side sink	Duty cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 6.5 V,	2			A
	High-side source	V_{HIGHDR} = 1.5 V (source) or 6 V (sink), See Note 3	2			
	Low-side sink	Duty Cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, V_{DRV} = 6.5 V,	2			
	Low-side source	V_{LOWDR} = 1.5 V (source) or 5 V (sink), See Note 3	2			
Output resistance (see Note 5)	High-side sink	T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 6.5 V,			3	Ω
	High-side source	V_{HIGHDR} = 6 V (source) or 0.5 V (sink)			45	
	Low-side sink	T_J = 125°C, V_{DRV} = 6.5 V,			5.7	
	Low-side source	V_{LOWDR} = 6 V (source) or 0.5 V (sink)			45	

NOTES: 3. This parameter is ensured by design and is not production tested.
5. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{ds(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		11.4	12	13	V
V_{CC}	Quiescent current	$V_{INHIBIT}$ = 5 V, V_{CC} > 10.75 V at startup, VID code ≠ 11111, V_{BOOTLO} = 0 V		3	10	mA
		$V_{INHIBIT}$ = 5 V, V_{CC} > 10.75 V at startup, C_{HIGHDR} = 50 pF, f_{SWX} = 200 kHz, VID code ≠ 11111, V_{BOOTLO} = 0 V, C_{LOWDR} = 50 pF, See Note 3		5		
	High-side driver quiescent current	$V_{INHIBIT}$ = 0 V or VID code = 11111 or V_{CC} < 9.25 V at startup, V_{BOOT} = 13 V, V_{BOOTLO} = 0 V			80	µA
		$V_{INHIBIT}$ = 5 V, V_{BOOT} = 13 V, C_{HIGHDR} = 50 pF, VID code ≠ 11111, V_{CC} > 10.75 V at startup, V_{BOOTLO} = 0 V, f_{SWX} = 200 kHz (see Note 3)		2		mA

NOTE 3: This parameter is ensured by design and is not production tested.

switching characteristics over recommended operating virtual-junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay	VSENSE to HIGHDR or LOWDR (excluding dead-time)	1.3 V ≤ V_{VREF} ≤ 3.5 V, 10 mV overdrive (see Note 3)		150	250	ns
		1.3 V ≤ V_{VREF} ≤ 3.5 V, 20 mV overdrive			200	
		1.3 V ≤ V_{VREF} ≤ 3.5 V, 30 mV overdrive			190	
		1.3 V ≤ V_{VREF} ≤ 3.5 V, 40 mV overdrive			180	
	OCP comparator	See Note 3		1		µs
	OVP comparator			1		
	PWRGD comparator			1		
	SLOWST comparator	Overdrive = 10 mV (see Note 3)		560	900	ns
Rise time	HIGHDR output	C_L = 50 pF, V_{BOOTLO} = 0 V			8	ns
		C_L = 3 nF			35	
	LOWDR output	C_L = 50 pF			8	
		C_L = 3 nF			40	
Fall time	HIGHDR output	C_L = 50 pF, V_{BOOTLO} = 0 V			TBD	ns
		C_L = 3 nF			35	
	LOWDR output	C_L = 50 pF			TBD	
		C_L = 3 nF			40	
Deglitch time (Includes comparator propagation delay)	OCP	See Note 3	2		5	µs
	OVP		2		5	
Response time	High-side VDS sensing	$V_{HISENSE}$ = 12 V, V_{IOUTLO} pulsed from 12 V to 11.9 V, 100 ns rise/fall times (see Note 3)			2	µs
		$V_{HISENSE}$ = 4.5 V, V_{IOUTLO} pulsed from 4.5 V to 4.4 V, 100 ns rise/fall times (see Note 3)			3	
		$V_{HISENSE}$ = 3 V, V_{IOUTLO} pulsed from 3 V to 2.9 V, 100 ns rise/fall times (see Note 3)			3	
Short-circuit protection rising-edge delay	SCP	LOSENSE = 0 V (see Note 3)	300		500	ns
Turnon/turnoff delay	V_{DS} sensing sample/hold switch	3 V ≤ $V_{HISENSE}$ ≤ 11 V, $V_{LOSENSE}$ = $V_{HISENSE}$ (see Note 3)	30		100	ns
Crossover delay time	LOWDR to HIGHDRV, and LOHIB to LOWDR	See Note 3	30		100	ns
Prefilter pole frequency	Hysteretic comparator	See Note 3		5		MHz
Propagation delay	LODRV	See Note 3			400	ns

NOTE 3: This parameter is ensured by design and is not production tested.

TYPICAL CHARACTERISTICS

SLOWSTART TIME
vs
SLOWSTART CAPACITANCE

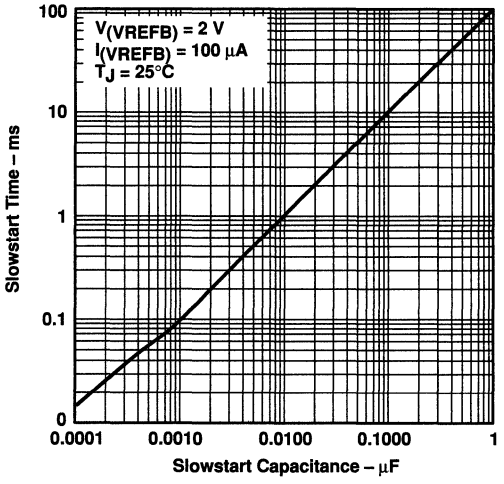


Figure 1

SLOWSTART TIME
vs
SUPPLY CURRENT (VREFB)

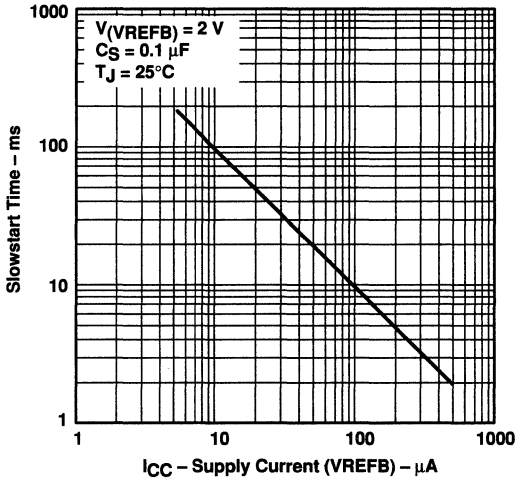


Figure 2

DRIVER
OUTPUT RISE TIME
vs
LOAD CAPACITANCE

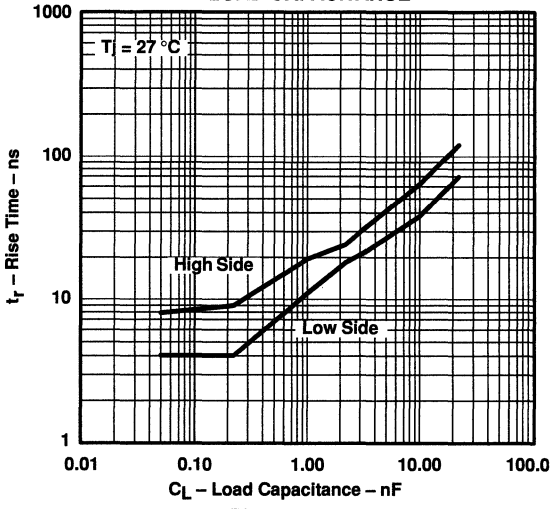


Figure 3

DRIVER
OUTPUT FALL TIME
vs
LOAD CAPACITANCE

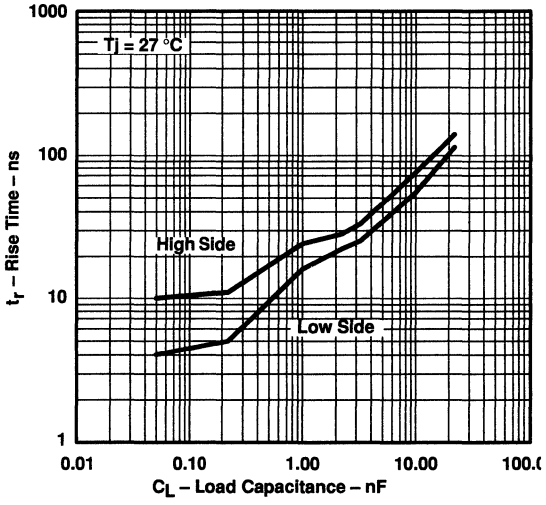


Figure 4

TYPICAL CHARACTERISTICS

OVP THRESHOLD
vs
JUNCTION TEMPERATURE

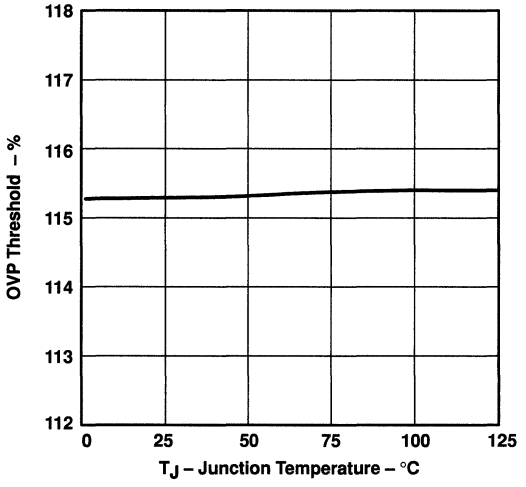


Figure 5

OCP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

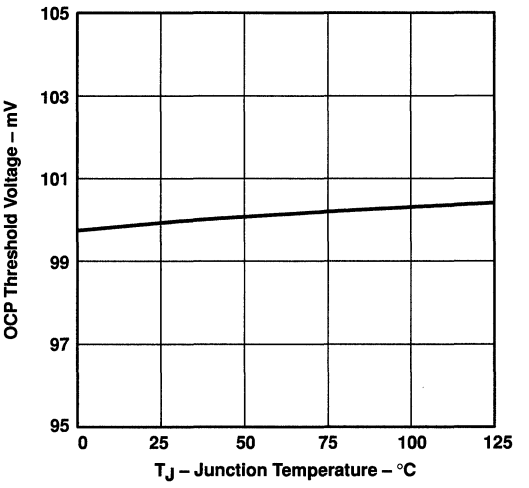


Figure 6

INHIBIT START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

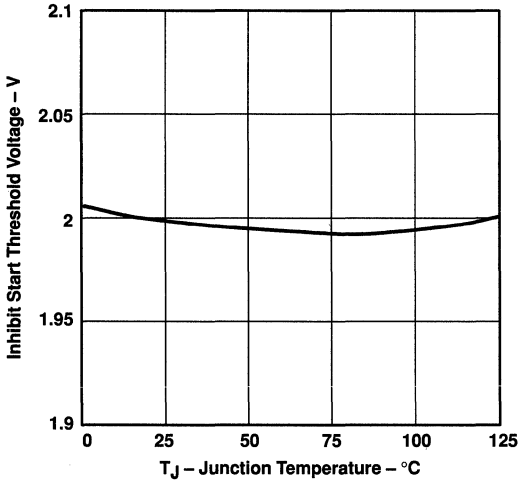


Figure 7

INHIBIT HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

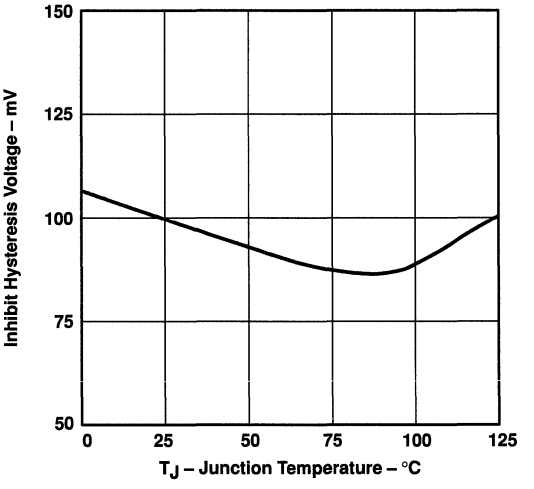


Figure 8

TYPICAL CHARACTERISTICS

UVLO START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

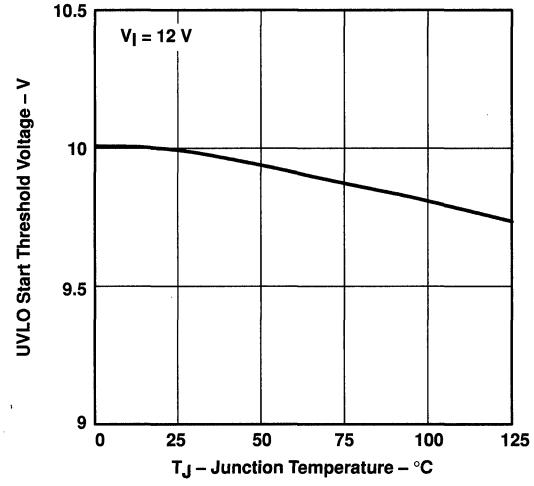


Figure 9

UVLO HYSTERESIS
vs
JUNCTION TEMPERATURE

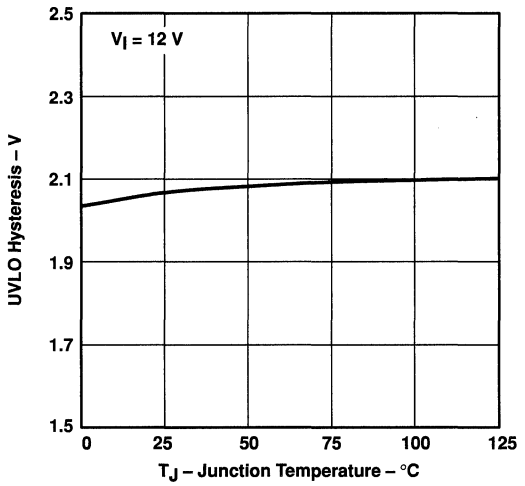


Figure 10

QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE

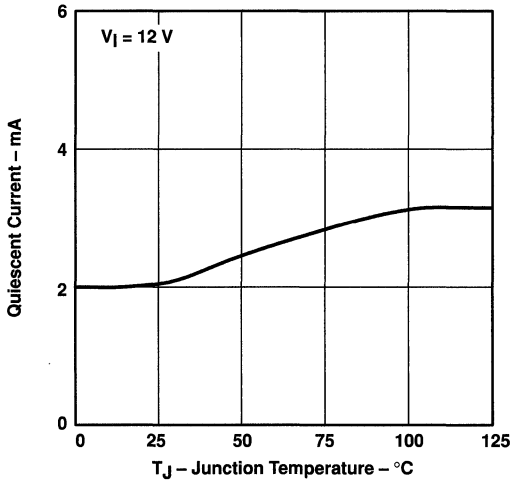


Figure 11

POWERGOOD THRESHOLD
vs
JUNCTION TEMPERATURE

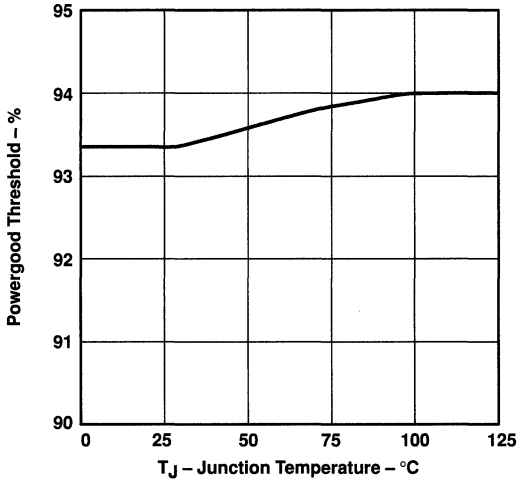


Figure 12

TYPICAL CHARACTERISTICS

SLOWSTART CHARGE CURRENT
vs
JUNCTION TEMPERATURE

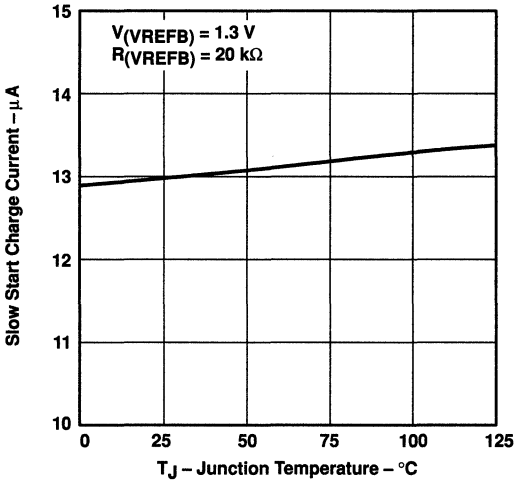


Figure 13

DRIVER
REGULATOR VOLTAGE
vs
JUNCTION TEMPERATURE

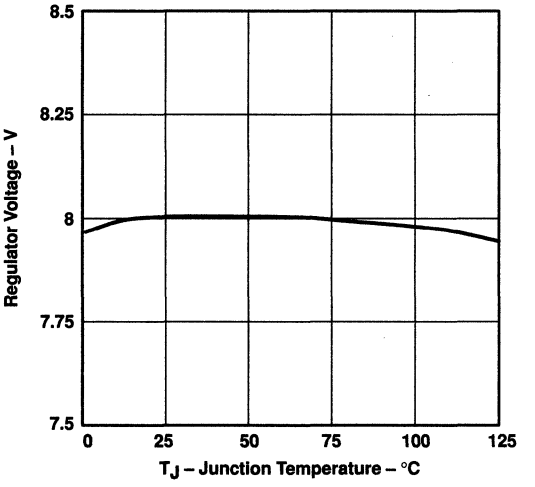


Figure 14

DRIVER
HIGH-SIDE OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

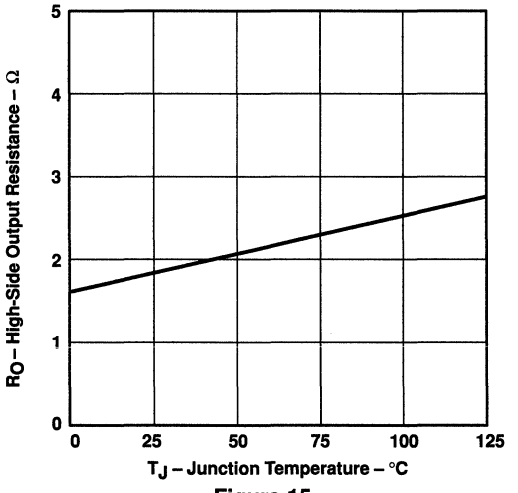


Figure 15

DRIVER
LOW-SIDE OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

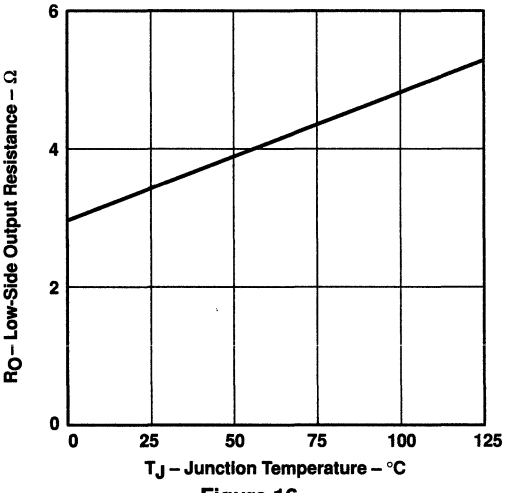


Figure 16

TYPICAL CHARACTERISTICS

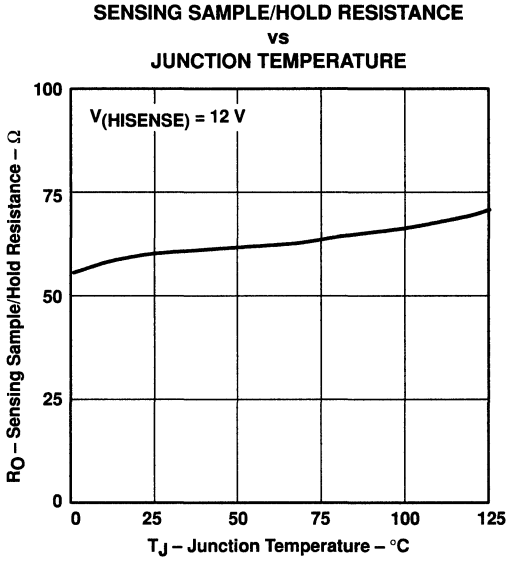
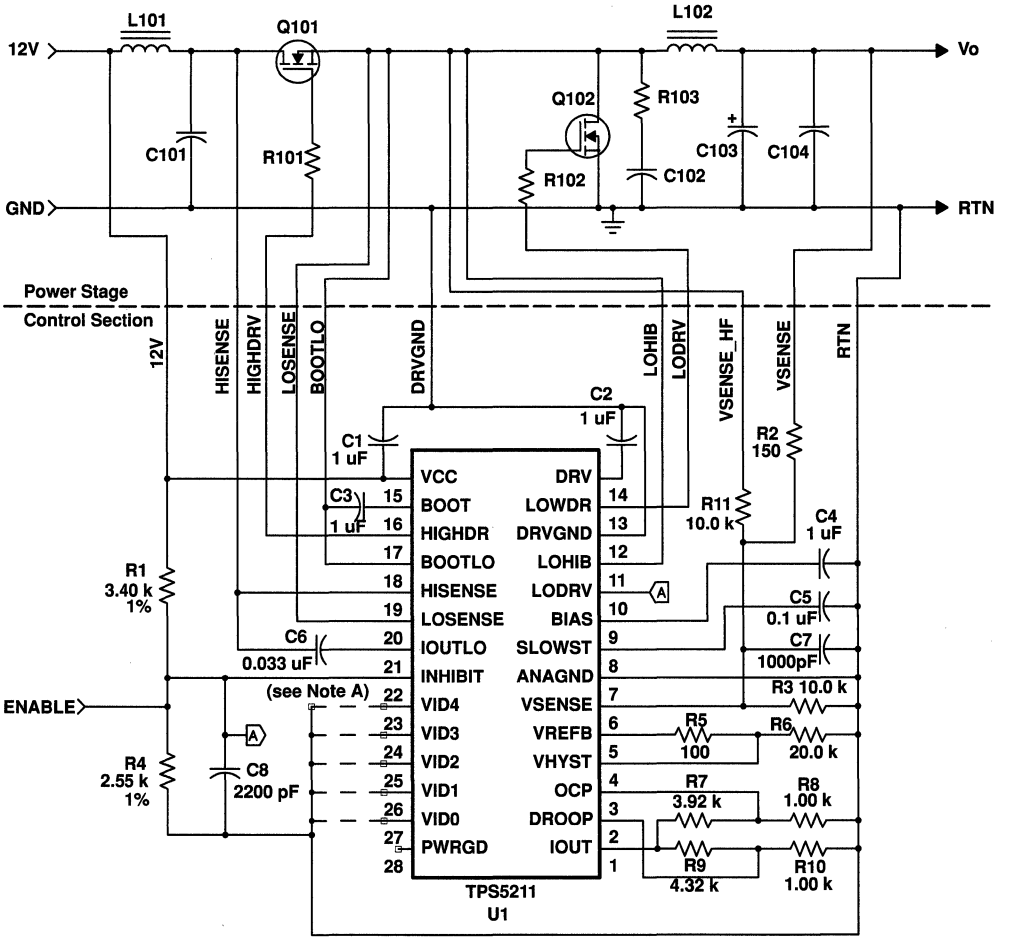


Figure 17

APPLICATION INFORMATION

The following figure is a typical application schematic. The circuit can be divided into the power-stage section and the control-circuit section. The power stage must be tailored to the input/output requirements of the application. The control circuit is basically the same for all applications with some minor tweaking of specific values. Table 2 shows the values of the power stage components for various output-current options.



NOTE A. VID0 – VID4 User – selected to set output voltage.

Figure 18. Standard Application Schematic

APPLICATION INFORMATION

Table 2. Power Stage Components

Reference Designation	Function	12-V–Input Power Stage Components			
		4–A Out	8–A Out	12–A Out	20–A Out
C101	Input capacitor	muRata, GRM235Y106Z016A, 2 x 10–uF, 16–V, Y5V	muRata, GRM235Y106Z016A, 4 x 10–uF, 16–V, Y5V	muRata, GRM235Y106Z016A, 6 x 10–uF, 16–V, Y5V	muRata, GRM235Y106Z016A, 10 x 10–uF, 16–V, Y5V
C102	Snubber capacitor	muRata, GRM39X7R102K050A, 1000–pF, 50–V, X7R	muRata, GRM39X7R102K050A, 1000–pF, 50–V, X7R	muRata, GRM39X7R102K050A, 2 x 1000–pF, 50–V, X7R	muRata, GRM39X7R102K050A, 3 x 1000–pF, 50–V, X7R
C103	Output bulk capacitor	Sanyo, 4TPC150M, 150–uF, 4–V, 20%	Sanyo, 4TPC150M, 2 x 150–uF, 4–V, 20%	Sanyo, 4TPC150M, 3 x 150–uF, 4–V, 20%	Sanyo, 4TPC150M, 4 x 150–uF, 4–V, 20%
C104	Output hi–freq bypass capacitor	muRata, GRM235Y106Z016A, 2 x 10–uF, 16–V, Y5V	muRata, GRM235Y106Z016A, 4 x 10–uF, 16–V, Y5V	muRata, GRM235Y106Z016A, 6 x 10–uF, 16–V, Y5V	muRata, GRM235Y106Z016A, 8 x 10–uF, 16–V, Y5V
L101	Input filter inductor	CoilCraft, DO1607C–152, 1.5–uH, 2.1–A	CoilCraft, DO1813HC–122, 1.2–uH, 4.4–A	CoilCraft, DO1813HC–122, 1.2–uH, 4.4–A	CoilCraft, DO3316P–152HC, 1.5–uH, 9.0–A
L102	Output filter inductor	CoilCraft, DO1813HCP–561, 0.56–uH, 6–A	CoilCraft, DO3316P–681HC, 0.68–uH, 12–A	Vishay–Dale, IHLP–5050CE–XX, 0.82–uH, 16–A, New product	Vishay–Dale, IHLP–5050CE–XX, 0.5–uH, 25–A, New product
R101	High–side gate resistor	10.0–Ohm, 1/16–W, 5%	10.0–Ohm, 1/16–W, 5%	2 x 10.0–Ohm, 1/16–W, 5%	2 x 10.0–Ohm, 1/16–W, 5%
R102	Lo–side gate resistor	3.3–Ohm, 1/16–W, 5%	3.3–Ohm, 1/16–W, 5%	2 x 3.3–Ohm, 1/16–W, 5%	3 x 3.3–Ohm, 1/16–W, 5%
R103	Snubber resistor	2.7–Ohm, 1/10–W, 5%	2.7–Ohm, 1/10–W, 5%	2 x 2.7–Ohm, 1/10–W, 5%	3 x 2.7–Ohm, 1/10–W, 5%
Q101	Power switch	IR, IRF7811, NMOS, 11–mOhm	IR, IRF7811, NMOS, 11–mOhm	IR, 2 x IRF7811, NMOS, 11–mOhm	IR, 2 x IRF7811, NMOS, 11–mOhm
Q102	Synchronous switch	IR, IRF7811, NMOS, 11–mOhm	IR, IRF7811, NMOS, 11–mOhm	IR, 2 x IRF7811, NMOS, 11–mOhm	IR, 2 x IRF7811, NMOS, 11–mOhm
Nominal frequency†	700 KHz				
Hysteresis window	20 mV				

† Nominal frequency measured with Vo set to 2 V.

The values listed above are recommendations based on actual test circuits. Many variations of the above are possible based upon the desires and/or requirements of the user. Performance of the circuit is equally, if not more, dependent upon the layout than on the specific components, as long as the device parameters are not exceeded. Fast-response, low-noise circuits require critical attention to the layout details. Even though the operating frequencies of typical power supplies are relatively low compared to today's microprocessor circuits, the power levels and edge rates can cause severe problems both in the supply and the load. The power stage, having the highest current levels and greatest dv/dt rates, should be given the greatest attention.

APPLICATION INFORMATION

frequency calculation

The simplified equation shown below can be used for a preliminary frequency calculation:

$$f_s \cong \frac{V_{REF} \times (V_I - V_{REF})}{V_I \times R11 \times C7 \times \text{Hysteresis Window}} \times 0.85 \quad (1)$$

High frequency operations require special attention not to exceed maxium current through the controller (120mA), and the maximum total power dissipation.

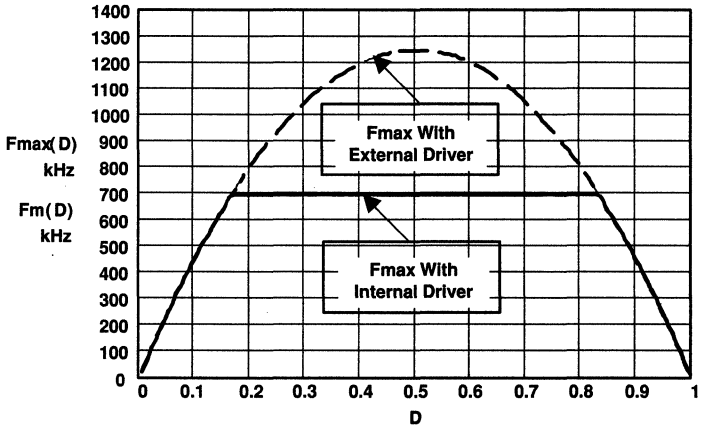


Figure 19

Another restriction relates to the maximum rms current through the output of the highside driver, (110mA.) The maximum allowable operating frequency can be defined by the following equation:

$$Fmax = \frac{(110mA)^2 \times 60ohm)}{Qg \times (V_I + Vdrv)} \quad (2)$$

Where Qg = Total gate charge of the upper FETs in the hysteretic converter (in nanocoulombs)
Vdrv = 8 V and is the drive regulator voltage of the TPS5211 controller
V_I = Input voltage
Fmax = Maximum switching frequency in kHz

Figure 19 and equation (2) should be used to determine the maximum operating frequency of a converter. The operating frequency should not exceed the lower of the two values determined by Figure 19 and equation (2).

APPLICATION INFORMATION

Control Section

Below are the equations needed to select the various components within the control section.

output voltage selection

The most important function of the power supply is to regulate the output voltage to a specific value. Values between 1.3 V and 3.5 V can be easily set by shorting the correct VID inputs to ground. Values above the maximum reference voltage (3.5 V) can be set by setting the reference voltage to any convenient voltage within its range and selecting values for R2 and R3 to give the correct output. Select R3:

R3 << than $V_{REF}/I_{BIAS(VSENSE)}$; a recommended value is 10 kΩ

Then, calculate R2 using:

$$V_O = V_{REF}\left(1 + \frac{R2}{R3}\right) \qquad \text{or} \qquad R2 = \frac{R3 \times \left(V_O - V_{REF}\right)}{V_{REF}}$$

These equations are accurate if R2<<R11. If this condition is not fullfilled, the following equation must be used:

$$V_O = V_{REF}\left(1 + \frac{R2 \text{ x } R11}{R3 \text{ x } (R2 + R11)}\right)$$

Another soultion is to use 0.1-μF DC decoupling capacitor in series with R11. In such a case, R11 does not influence the output voltage value.

R2 and R3 can also be used to make small adjusts to the output voltage within the reference-voltage range and/or to adjust for load-current active droop compensation. If there is no need to adjust the output voltage, R3 can be eliminated. R2, R3 (if used), and C7 are used as a noise filter; calculate using:

$$C7 = \frac{150 \text{ ns}}{(R2 \parallel R3)}$$

slowstart timing

Slowstart reduces the startup stresses on the power-stage components and reduces the input current surge. Slowstart timing is a function of the reference-voltage current (determined by R6) and is independent of the reference voltage. The first step in setting slowstart timing will be to determine R6:

R6 should be between 7 kΩ and 300 kΩ, a recommended value is 20 kΩ.

Set the slowstart timing using the formula:

$$C5 = \frac{t_{SS}}{(5 \times R_{VREFB})} \cong \frac{t_{SS}}{(5 \times R6)}$$

Where C5 = Slowstart capacitance in μF
t_{SS} = Slowstart timing in μs
R_{VREFB} = Resistance from VREFB to GND in ohms (≈ R6)

APPLICATION INFORMATION

hysteresis voltage

A hysteretic controller regulates by self-oscillation, thus requiring a small ripple voltage on the VSENSE pin which the input comparator uses for sensing. Once selected, the TPS5211 hysteresis is proportional to the reference voltage; programming Vref to a new value automatically adjusts the hysteresis to be the same percentage of Vref. Since the output current from VREFB should be less than 500 µA, the total divider resistance (R5 + R6) should be greater than 7 KΩ. The hysteresis voltage should be no greater than 60 mV so R6 will dominate the divider.

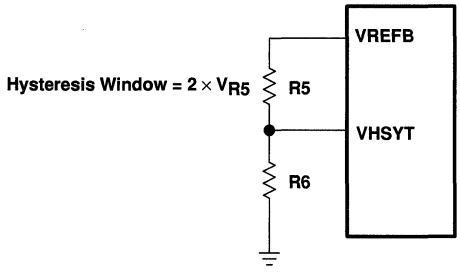


Figure 20. Hysteresis Divider Circuit

The upper divider resistor, R5, is calculated using:

$$R5 = \frac{\textit{Hysteresis Window}}{(2 \times \textit{VREFB} - \textit{Hysteresis Window})} \times R6 \cong \frac{V_{HYST}\,(\%)}{(2 \times 100)} \times R6$$

Where Hysteresis Window = The desired peak-to-peak hysteresis voltage
VREFB = Selected reference voltage
V_{HYST} (%) = [(Hysteresis Window)/VREFB] * 100 < $V_{O(Ripple)(P-P)}$ (%)

current limit

Current limit can be implemented using the on-resistance of the upper FETs as the sensing elements. Select R8:

$$R8 << \frac{V_{OCP}}{I_{Bias(OCP)}} \leq \frac{0.1V}{(100 \times 100\,nA)} \leq 10\ \text{k}\Omega$$ (A recommended value is 1 kΩ)

The IOUT signal is used to drive the current limit and droop-circuit dividers. The voltage at IOUT at the output current trip point will be:

$$V_{IOUT(Trip)} = \frac{(2 \times R_{DS(ON)} \times TF)}{NumFETs} \times I_{O(Trip)}$$

Where NumFETS = Number of upper FETS in parallel
TF = $R_{DS(ON)}$ temperature correction factor
$I_{O(Trip)}$ = Desired output current trip level (A)

APPLICATION INFORMATION

Calculate R7 using:

$$R7 = \left(\frac{V_{IOUT(Trip)}}{0.1\ V} - 1\right) \times R8$$

Note that since $R_{DS(ON)}$ of MOSFETs can vary from lot to lot and with temperature, tight current-limit control (less than 1.5 x I_O) using this method is not practical. If tight control is required, an external current-sense resistor in series with the drain of the upper FET can be used with HISENSE and LOSENSE connected across the resistor.

droop compensation

Active voltage droop positioning is used to reduce the output voltage range during load transients by increasing the output voltage setpoint toward the upper tolerance limit during light loads and decreasing the voltage setpoint toward the lower tolerance limit during heavy loads. This allows the output voltage to swing a greater amount and still remain within the tolerance window. The maximum droop voltage is set with R9 and R10. Select R10:

$$R10 << \frac{V_{DROOP(Min)}}{I_{Bias(DROOP,Max)}} \leq \frac{0.01V}{(100 \times 100\ nA)} \leq 1\ k\Omega$$

(Again, a value of 1 kΩ is recommended)

The voltage at IOUT during normal operation (0 to 100% load) will vary from 0 V up to:

$$V_{IOUT(Max)} = \frac{(2 \times R_{DS(ON)} \times TF)}{NumFETs} \times I_{O(Max)}$$

Where $I_{O(Max)}$ = Maximum output load current (A).

droop compensation (continued)

Then, calculate R9:

$$R9 = \left(\frac{V_{IOUT(Max)}}{V_{DROOP}} - 1\right) \times R10$$

Where V_{DROOP} = Desired droop voltage

At full load, the output voltage will be:

$$V_O = V_{REF} \times \left(1 + \frac{R2}{R3}\right) - V_{DROOP}$$

APPLICATION INFORMATION

using the TPS5211 when both 12 V and 5 V are available

When both 12 V and 5 V are available, several components can be removed from the basic schematic shown in Figure 18. R1, R4, and C9 are no longer required if 5 V is brought in directly to INHIBIT and LODRV. However, if undervoltage lockout for the 5-V input is desired, R1 and R4 can be used to set the startup setpoint. The INHIBIT pin trip level is 2.1 V. Select R4:

$$R4 << \frac{V_{INH}}{I_{INH(Max)}} \leq \frac{2.1V}{(100 \times 100\,nA)} \leq 210\,k\Omega$$

Then, set the 5-V UVLO trip level with R1:

$$R1 = \frac{(5\,V_{Trip} - 2V)}{2V} \times R4$$

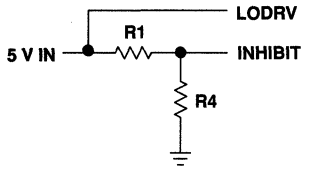
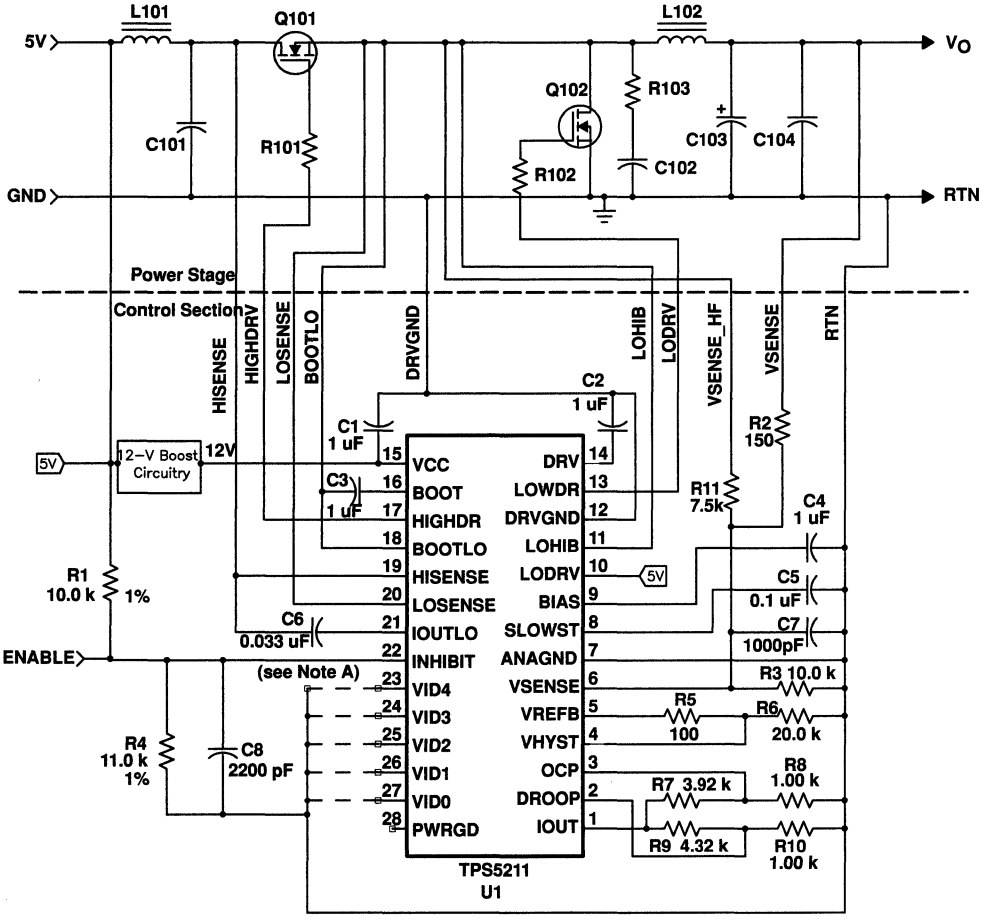


Figure 21. 5-V Input With UVLO

APPLICATION INFORMATION

using the TPS5211 when only 5 V is available

The TPS5211 controller requires 12 V for internal control of the device. If an external source for 12 V is not available, a small onboard source must be included in the design. A simple boost circuitry is described in TIs application report AN452 *Providing a DSP Power Solution from +5 V or +3.3 V only Systems.* Total 12-V current depends on switching frequency and power FETs gate charge characteristics. For reliable operation, this current should not exceed 120 mA. The power stage is not voltage dependent, but component values must be selected for 5-V inputs. The frequency of operation is dependent upon the power stage input voltage. A typical 5-V only application circuit is shown in Figure 22.



NOTE A. VID0 – VID4 User – selected to set output voltage.

Figure 22. Typical 5-V-Only Application Circuit

APPLICATION INFORMATION

controller operation

Operation of the TPS5211 controller differs from a regular hysteretic controller. The additional ramp signal through the input of the hysteretic comparator is formed by R11 and C7. The two signals are summed through the inputs of the comparator. The two signals are the ramp signal from R11 - C7 circuitry and the signal from the output converter. By proper selection of R11 and C7, one can get the amplitude of an additional ramp signal which is greater than the output ripple of the converter. As a result, the switching frequency is greater while the output ripple becomes lower. The additional ramp signal and output ripple waveforms are shown in Figure 23. The switching frequency now depends on R11 and C7 values and does not depend on the output filter characteristics including ESR, ESL, and C of the output capacitor (see frequency calculation section).

The dc feedback signal from the output of the converter through resistor R2 controls the dc level of the output voltage. Because the switching frequency of TPS5211 is high and it does not depend on output capacitor characteristics, low cost cermic or film capacitors can be used in a dc to dc converter while having the same load current transient response characteristics.

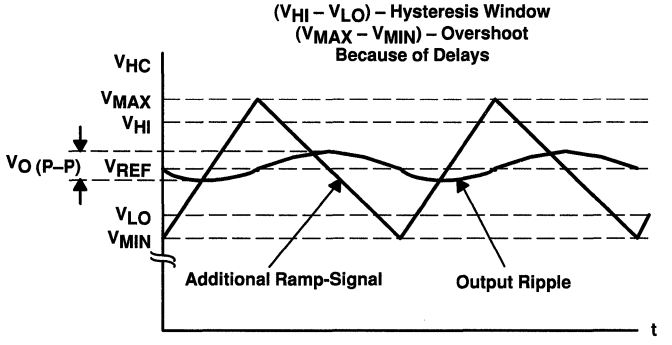


Figure 23. The Additional Ramp-Signal and Output Voltage Ripple Waveforms

APPLICATION INFORMATION

application examples

Below are waveforms and test results measured on the EVM for a 12-V input and a 2-V, 20-A output application. The output voltage ripple and power switches midpoints are shown in Figure 24. The converter operates at 450 kHz. The peak to peak output ripple is 9.6 mV, while the hysteresis window is set at 20 mV. Therefore, the output ripple for converter with TPS5211 is much lower than the hysteresis window.

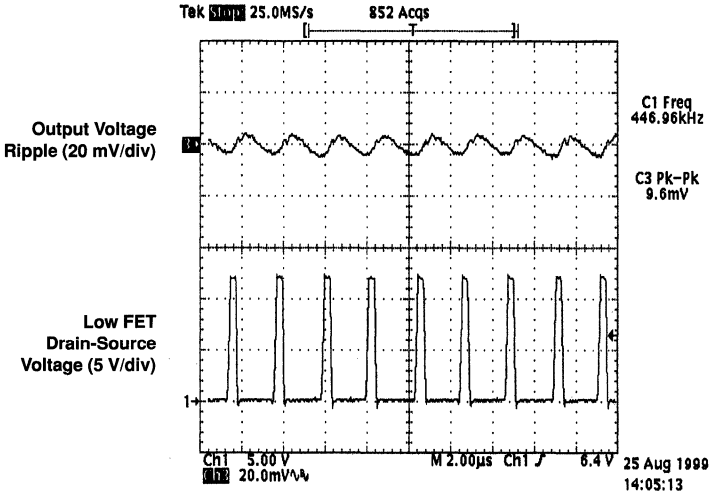


Figure 24. The Output Voltage Ripple ans Low FET Drain-Source Voltage Waveforms

APPLICATION INFORMATION

The load current transient response waveforms are shown in Figure 25 to illustrate the excellent load current transient response characteristics of TPS5211.

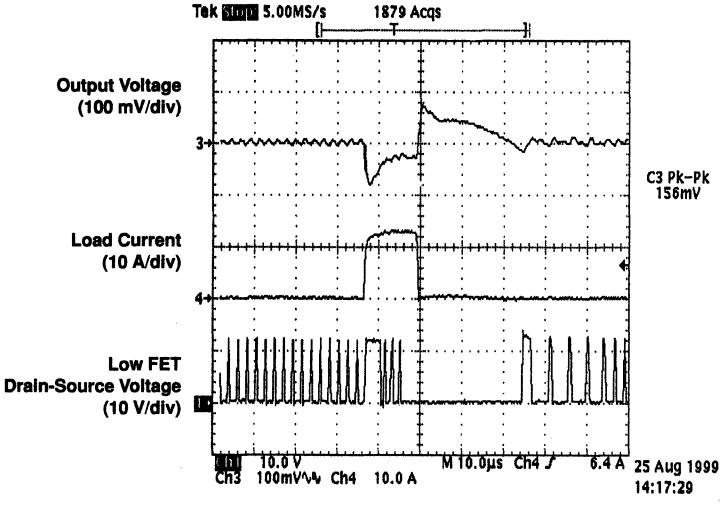


Figure 25

The output voltage transient response of the converter with TPS5211 controller. The load current has 14 A step with slew rate of 30 A/µS.

APPLICATION INFORMATION

Comparison of TPS5210 and TPS5211 controller applications

The TPS5210 and TPS5211 hysteretic controllers have excellent load current transient response characteristics, which is one of the most important advantages of hysteretic mode. There are specific application areas where one of the hysteretic controllers is preferable over the other. The table below gives a comparative view on application areas for the TPS5210 and TPS5211 controllers

comparison of TPS5210 and TPS5211 applications		
Controller	TPS5210	TPS5211
Switching frequency, kHz	100 – 400	400 – 700
Frequency variation	Depends on outout filter characteristics	Independent of output filter and easy to evaluate
Output current, A	up to 40	up to 18 – 20 (can be increased in multi-phase configuration)
Efficiency, % (depends on frequency, output current, Vin, Vout, components, etc.)	85 – 95	75 – 85
Input and output filter	Requires bulk electrolytic capacitors especially if Iout > 12A and larger inductor	Surface-mount ceramic and POSCAP type capacitors and 40% – 65% smaller inductors.
Component Cost	20% – 40% lower for TPS5211	
System cost including reliability, power losses, cooling, etc.	Can be estimated only during design for a given specific application.	
Layout and design	Special attention to the noise sensitive places such as the hysteresis comparator and the sample hold circuitry.	Special attention not to exceed frequency and Icc limits. The high frequency dc – dc converter design rules should be used.
Compatibility with the whole system	For high current applications, it is difficult to meet high density minimum size requirements.	A dc – dc converter can be placed close to the microprocessor or DSP to decrease the number of decoupling capacitors.

APPLICATION INFORMATION

layout guidelines

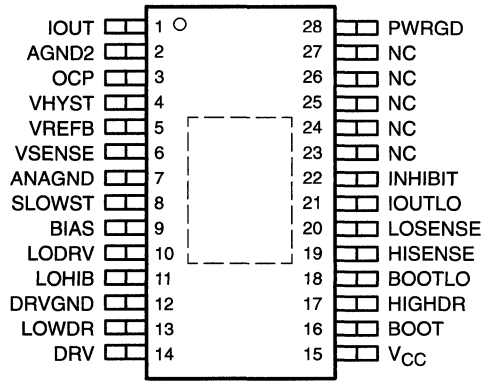
Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB design. The general design should proceed from the switching node to the output, then back to the driver section, and, finally, to placing the low-level components. Below are several specific points to consider *before* layout of a TPS5211 design begins.

1. All sensitive analog components should be referenced to ANAGND. These include components connected to SLOWST, DROOP, IOUT, OCP, VSENSE, VREFB, VHYST, BIAS, and LOHIB.
2. Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.
3. Connections from the drivers to the gate of the power FETs, should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
4. The bypass capacitor for the DRV regulator should be placed close to the TPS5210 and be connected to DRVGND.
5. The bypass capacitor for V_{CC} should be placed close to the TPS5210 and be connected to DRVGND.
6. When configuring the high-side driver as a floating driver, the connection from BOOTLO to the power FETs should be as short and as wide as possible. The other pins that also connect to the power FETs, LOHIB and LOSENSE, should have a separate connection to the FETS since BOOTLO will have large peak currents flowing through it.
7. When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from BOOT to BOOTLO) should be placed close to the TPS5210.
8. When configuring the high-side driver as a ground-referenced driver, BOOTLO should be connected to DRVGND.
9. The bulk storage capacitors across V_I should be placed close to the power FETS. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
10. High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
11. HISENSE and LOSENSE should be connected very close to the drain and source, respectively, of the high-side FET. HISENSE and LOSENSE should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed close to where HISENSE connects to Vin, to reduce high-frequency noise coupling on HISENSE.

SLVS177A – SEPTEMBER 1998 – REVISED NOVEMBER 1998

- ±1% Reference Over Full Operating Temperature Range
- Synchronous Rectifier Driver for >90% Efficiency
- Fixed Output Voltage Options of 1.5 V, 1.8 V, 2.5 V, and 3.3 V
- User-Selectable Hysteretic-Type Control
- Low Supply Current . . . 3 mA Typ
- 11.4-V to 13-V Input Voltage Range, V_{CC}
- Power Good Output
- Programmable Soft-Start
- Overvoltage/Overcurrent Protection
- Active Deadtime Control

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

description

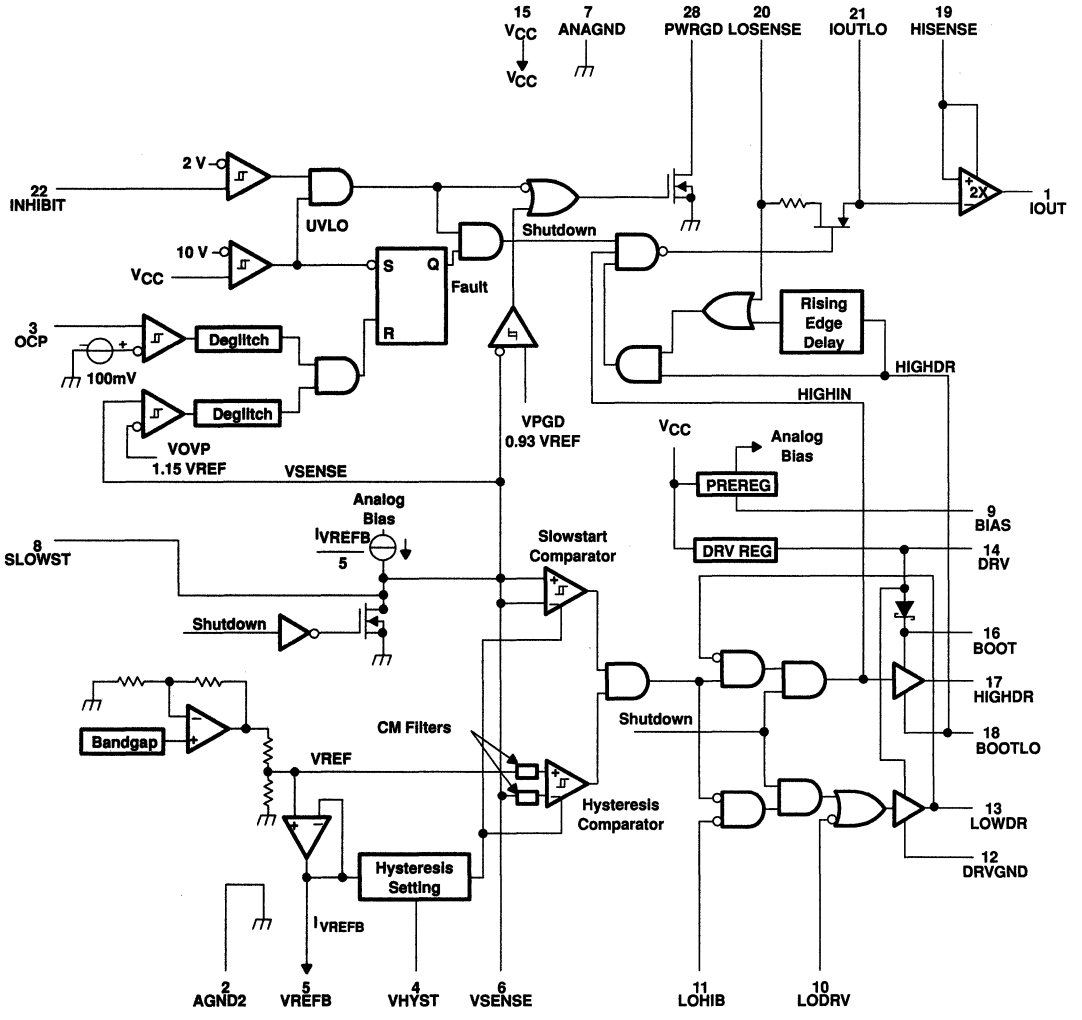
The TPS5615 family of synchronous-buck regulator controllers provides an accurate supply voltage to DSPs. The output voltage is internally set by a resistive divider with an accuracy of 1% over the full operating temperature range. A hysteretic controller with user-selectable hysteresis is used to dramatically reduce overshoot and undershoot caused by load transients. Propagation delay from the comparator inputs to the output drivers is less than 250 ns. Overcurrent shutdown and crossover protection for the output drivers combine to eliminate destructive faults in the output FETs. PWRGD monitors the output voltage and pulls the open-collector output low when the output drops below 93% of the nominal output voltage. An overvoltage circuit disables the output drivers if the output voltage rises 15% above the nominal value. The inhibit pin can be used to control power sequencing. Inhibit and undervoltage lockout assures that the 12-V supply voltage and system supply voltage (5 V or 3.3 V) are within proper operating limits before the controller starts. The output driver circuits include 2-A drivers with internal 8-V gate-voltage regulators that can easily provide sufficient power for today's high-powered DSPs. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. The TPS5615 family is available in a 28-pin TSSOP PowerPad™ package. It operates over a junction temperature range of 0°C to 125°C.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE	PACKAGE
		TSSOP† (PWP)
0°C to 125°C	1.5 V	TPS5615PWP
	1.8 V	TPS5618PWP
	2.5 V	TPS5625PWP
	3.3 V	TPS5633PWP

† The PWP package is availble taped and reeled. Add R suffix to device type (e.g., TPS5615PWPR).

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND2	2		Analog ground (must be connected).
ANAGND	7		Analog ground
BIAS	9		Analog bias pin. A 1-μF capacitor should be connected from BIAS to ANAGND.
BOOT	16		Bootstrap. A 1-μF capacitor should be connected from BOOT to BOOTLO.
BOOTLO	18		Bootstrap low. Connect to the junction of the high-side and low-side FETs for floating drive configuration. Connect to PGND for ground-reference drive configuration.
DRV	14		Drive regulator for the FET drivers. A 1-μF capacitor should be connected from DRV to DRVGND.
DRVGND	12		Drive ground. Ground for FET drivers. Connect to FET PWRGND.
HIGHDR	17		High drive. Output drive to high-side power switching FETs.
HISENSE	19		High current sense. For current sensing across high-side FETs, connect to the drain of the high-side FETs; for optional current sensing scheme, connect to power supply side of current-sense resistor placed in series with high-side FET drain.
INHIBIT	22		Disables the drive signals to the MOSFET drivers. Also serves as UVLO for system logic supply (3.3 V or 5 V). An external pull-up resistor should be connected to system-logic supply.
IOUT	1		Current out. Output voltage on this terminal is proportional to the load current as measured across the $R_{ds(on)}$ of the high side FET. The voltage on this terminal equals $2 \times R_{DS(ON)} \times$ IOUT. In applications where very accurate current-sensing is required, a sense resistor should be connected between the input supply and the drain of the high-side FETs.
IOUTLO	21		Current sense low output. This is the voltage on the LOSENSE terminal when the high-side FETs are on. A ceramic capacitor (between 0.033 μF and 0.1 μF) should be connected from IOUTLO to HISENSE to hold the sensed voltage.
LODRV	10		Low drive enable. Normally tied to 5 V. To configure the low-side FET as a crowbar, pull LODRV low.
LOHIB	11		Low side inhibit. Connect to the junction of the high- and low-side FETs to control the anti-cross-conduction and eliminate shoot-through current. Disabled when configured in crowbar mode.
LOSENSE	20		Low current sense. For current sensing across high-side FETs, connect to the source of the high-side FETs; for optional current sensing scheme, connect to high-side FET drain side of current-sense resistor placed in series with high-side FET drain.
LOWDR	13		Low drive. Output drive to synchronous rectifier FETs.
NC	23–27		No connect
OCP	3		Over current protection. Current limit trip point is set with a resistor divider between IOUT and ANAGND.
PWRGD	28		Power good. PWRGD signal goes high when output voltage is within 7% of voltage setpoint. Open-drain output.
SLOWST	8		Slow Start (soft start). A capacitor form SLOWST to ANAGND sets the slowstart time. Slowstart current = $I_{VREFB}/5$
VHYST	4		Hysteresis set input. The hysteresis is set with a resistor divider from VREFB to ANAGND. Hysteresis = 2 × (VREFB – VHYST)
V_{CC}	15		12-V supply. A 1-μF capacitor should be connected from V_{CC} to DRVGND.
VREFB	5		Buffered reference voltage
VSENSE	6		Voltage sense Input. To be connected from converter output voltage bus to sense and control output voltage. It is recommended that a RC low-pass filter be connected at this pin to filter noise.

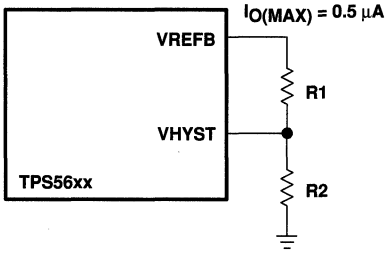
detailed description

Vref

The reference voltage section consists of a temperature-compensated bandgap reference and a resistive divider that sets the output voltage option. The output voltage, VREF, is within 1% of the nominal setting over the full junction temperature range of 0°C to 125°C, and a V_{CC} supply voltage range of 11.4 V to 12.6 V. The output of the reference network is indirectly brought out through a buffer to the VREFB pin. The voltage on this pin will be within 2% of VREF. It is not recommended to drive loads with VREFB, other than setting the hysteresis of the hysteretic comparator, because the current drawn from VREFB sets the charging current for the slowstart capacitor. Refer to the *slowstart* section for additional information.

hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by 2 external resistors and is centered on VREF. The 2 external resistors form a resistor divider from VREFB to ANAGND, with the output voltage connecting to the VHYST pin. The hysteresis of the propagation delay from the comparator inputs to the driver outputs is 250 ns (maximum). The maximum hysteresis setting is 60 mV.



$$R1 = \frac{R2 \times V_H}{2 \times VREFB - V_H}$$

Where

V_H = desired hysteresis voltage

$= 2 \times (VREFB - V_H)$

Figure 1. Setting the Hysteresis Voltage

low-side driver

The low-side driver is designed to drive low-$R_{ds(on)}$ n-channel MOSFETs. The current rating of the driver is 2 A, source or sink. The bias to the low-side driver is internally connected to the DRV regulator.

high-side driver

The high-side driver is designed to drive low-$R_{ds(on)}$ n-channel MOSFETs. The current rating of the driver is 2 A, source or sink. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from the DRV regulator. The internal bootstrap diode, connected between the DRV and BOOT pins, is a Schottky for improved drive efficiency. The maximum voltage that can be applied between BOOT and DRVGND is 30 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting BOOT to either DRV or V_{CC}.

deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate-drive voltage to the low-side FET is below 2 V; the low-side driver is not allowed to turn on until the voltage at the junction of the 2 FETs (Vphase) is below 2 V.

detailed description (continued)

current sensing

Current sensing is achieved by sampling and holding the voltage across the high-side power FET while the high-side FET is on. The sampling network consists of an internal 60-Ω switch and an external ceramic hold capacitor. Recommended value of the hold capacitor is between 0.033 µF and 0.1 µF. The actual value should give a time constant (60 Ω × C_H) greater than the FET on time. Internal logic controls the turn-on and turn-off of the sample/hold switch such that the switch does not turn on until the Vphase voltage transitions high, and the switch turns off when the input to the high-side driver goes low. Thus sampling will occur only when the high side FET is conducting current. The voltage on the IOUT pin equals 2 times the sensed high-side voltage. In applications where a higher accuracy in current-sensing is required, a sense resistor can be placed in series with the high-side FET and the voltage across the sense resistor can be sampled by the current sensing circuit. See Figures 2 and 3.

overcurrent protection

The overcurrent protection (OCP) circuit monitors the current through the high-side FET. The overcurrent threshold is adjustable with an external resistor divider between IOUT and ANAGND, with the divider voltage connected to OCP. If the voltage on OCP (V_S) exceeds 100 mV, then a fault latch is set and the output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value. A 3-µs deglitch timer is included for noise immunity. The OCP circuit is also designed to protect the high-side power FET against a short-to-ground fault on the terminal common to both power FETs (Vphase).

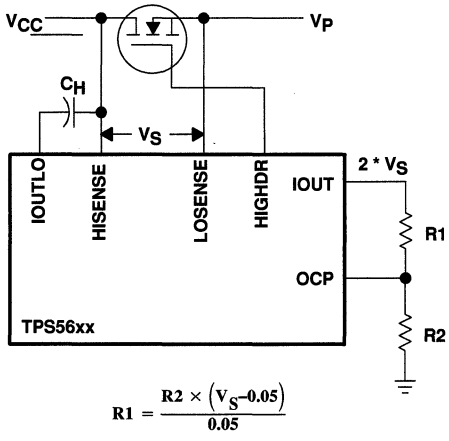


Figure 2. OCP Using FET ON-Resistance

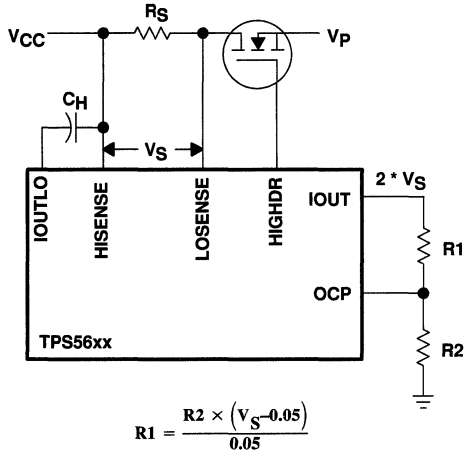
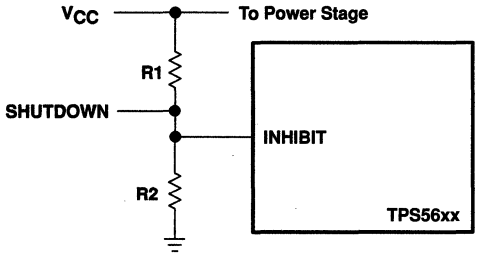


Figure 3. Precision OCP Using External Resistor

inhibit

INHIBIT is a TTL-compatible digital input used to enable the controller. When INHIBIT is low, the output drivers are low and the slowstart capacitor is discharged. When INHIBIT goes high, the short across the slowstart capacitor is released and normal converter operation begins. When the system-logic supply is connected to INHIBIT, it also controls power sequencing by locking out controller operation until the system-logic supply exceeds the input threshold voltage of the inhibit circuit. Thus the 12-V supply and the system-logic supply (either 5 V or 3.3 V) must be above UVLO thresholds before the controller is allowed to start up. The INHIBIT comparator start threshold is 2.1 V and the hysteresis is 100 mV.

detailed description (continued)



$$R2 = \frac{2.1 \times R1}{V_{TRIP} - 2.1}$$

Where

V_{TRIP}=desired V_{SUPPLY} trip voltage

Figure 4. Input Undervoltage Lockout Circuit Using INHIBIT

V_{CC} undervoltage lockout (UVLO)

The undervoltage lockout circuit disables the controller while the V_{CC} supply is below the 10-V start threshold during power-up. While the controller is disabled, the output drivers will be low and the slowstart capacitor will be shorted. When V_{CC} exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 2-V hysteresis in the undervoltage lockout circuit for noise immunity.

slowstart

The slowstart circuit controls the rate at which V_O powers up. A capacitor is connected between SLOWSST and ANAGND and is charged by an internal current source. The slowstart charging current is determined by the following equation:

$$I_{SLOWSTART} = \frac{I(VREFB)}{5}$$

where I(VREFB) is the current flowing out of VREFB. It is recommended that no additional loads be connected to VREFB, other than the resistor divider for setting the hysteresis voltage. The maximum current that can be sourced by the VREFB circuit is 500 µA. The slowstart time is set by:

$$t_{SLOWSTART} = 5 \times C_{SLOWST} \times R_{VREFB}$$

where R_{VREFB} is the total external resistance from VREFB to ANAGND.

power good

The power good circuit monitors for an undervoltage condition on V_O. If V_O is 7% below V_{REF}, then PWRGD is pulled low. PWRGD is an open-drain output.

overvoltage protection

The overvoltage protection (OVP) circuit monitors V_O for an overvoltage condition. If V_O is 15% above V_{REF}, then a fault latch is set and both output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value. A 3-µs deglitch timer is included for noise immunity. Refer to the LODRV section for information on how to protect the load against overvoltages due to a shorted fault across the high-side power FET.

detailed description (continued)

drive regulator

The drive regulator provides drive voltage to the output drivers. The minimum drive voltage is 7 V. The minimum short circuit current is 100 mA. Connect a 1-µF ceramic capacitor from DRV to DRVGND.

LODRV

The LODRV circuit is designed to protect the load against overvoltages that occur if the high-side FETs become shorted. External components to sense an overvoltage condition are required to use this feature. When an overvoltage fault occurs, LODRV is pulled low and the low-side FET will be turned on, overriding all control signals inside the TPS56xx controller. The crowbar action will short the system-logic supply to ground through the faulted high-side FETs and the low-side FETs. A fuse, in series with V_{IN}, should be added to disconnect the short circuit.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –0.3 to 14 V
Input voltage range: BOOT to DRVGND (high-side driver ON) ..... –0.3 to 30 V
BOOT to HIGHDRV ..... –0.3 to 15 V
BOOT to BOOTLO ..... –0.3 to 15 V
INHIBIT, LODRV ..... –0.3 to 7.3 V
PWRGD, OCP ..... –0.3 to 7 V
LOHIB, LOSENSE, IOUTLO, HISENSE ..... –0.3 to 14 V
VSENSE ..... –0.3 to 5 V
Voltage difference between ANAGND and DRVGND ..... ±0.5 V
Output current, VREFB ..... 0.5 mA
Short circuit duration, DRV ..... Continuous
Continuous total power dissipation ..... See Dissipation Rating Table
Operating junction temperature range, T_J ..... 0°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to ANAGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	1150 mW	11.5 mW/°C	630 mW	460 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		11.4	13	V
Input voltage	BOOT to DRVGND	0	28	V
	BOOT to BOOTLO	0	13	
	INHIBIT, LODRV, PWRGD, OCP	0	6	
	LOHIB, LOSENSE, IOUTLO, HISENSE	0	13	
	VSENSE	0	4.5	
Voltage difference between ANAGND and DRVGND		0	±0.2	V
Output current, VREFB†		0	0.4	mA

† Not recommended to load VREFB other than to set hysteresis since I_{VREFB} sets slowstart time.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted)

reference

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREF	Reference voltage	TPS5615	V_{CC} = 11.4 V to 12.6 V	1.485		1.515	V
		TPS5618		1.782		1.818	
		TPS5625		2.475		2.525	
		TPS5633		3.267		3.333	
VREFB	Output voltage		I_{REFB} = 50 µA	VREF–2%	VREF	VREF+2%	V
VREFB	Output regulation		10 µA ≤ I_O ≤ 500 µA		2		mV

power good

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Undervoltage trip threshold		90	93	95	%VREF
Low-level output voltage, PWRGD	I_O = 5 mA		0.5	0.75	V
High-level input current, PWRGD	V_{PWRGD} = 6 V		1		µA
Hysteresis			10		mV

overvoltage protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overvoltage trip threshold		112	115	120	%VREF
Hysteresis	See Note 2		10		mV

NOTE 2: Ensured by design, not tested.

slowstart

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge current	V_{SLOWST} = 0.5 V, I_{VREFB} = 65 µA	10.4	13	15.6	µA
Discharge current	V_{SOFTST} = 1 V		3		mA
Comparator input offset voltage				10	mV
Comparator input bias current	See Note 2		10	100	nA
Hysteresis		–7.5		7.5	mV

NOTE 2: Ensured by design, not tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

inhibit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Startup threshold		1.9	2.1	2.35	V
Hysteresis		0.08	0.1	0.12	V
Stop threshold		1.85			V

input undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Startup threshold		9.25	10	10.75	V
Hysteresis		1.9	2	2.2	V
Stop threshold		7.5			V

hysteretic comparator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage		–2.5		2.5	mV
Input bias current	See Note 2			500	nA
Hysteresis accuracy	$V_{REFB} - V_{HYST}$ = 15 mV, (hysteresis window = 30 mV)	–3.5		3.5	mV
Maximum hysteresis setting	$V_{REFB} - V_{HYST}$ = 30 mV		60		mV

NOTE 2: Ensured by design, not tested.

overcurrent protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OCP trip threshold		90	100	110	mV
Input bias current				100	nA

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

high-side VDS sensing

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain				2		V/V
Initial accuracy	$V_{HISENSE}$ = 12 V, $V_{LOSENSE}$ = 11.9 V Differential input to Vds sensing amp = 100 mV		194		206	mV
IOUTLO sink current	5 V ≤ V_{IOUTLO} ≤ 13 V				250	nA
IOUT source current	V_{IOUT} = 0.5 V, $V_{HISENSE}$ = 12 V, V_{IOUTLO} = 11.5 V		500			µA
IOUT sink current	V_{IOUT} = 0.05 V, $V_{HISENSE}$ = 12 V, V_{IOUTLO} = 12 V		50			µA
Output voltage swing	$V_{HISENSE}$ = 11 V	R_{IOUT} = 10 kΩ	0		2	V
	$V_{HISENSE}$ = 4.5 V		0		1.5	
	$V_{HISENSE}$ = 3 V		0		0.75	
LOSENSE high-level input voltage	$V_{HISENSE}$ = 4.5 V,	See Note 2	2.85			V
LOSENSE low-level input voltage	$V_{HISENSE}$ = 4.5 V,	See Note 2			2.4	V

Sample/hold resistance	11.4 V ≤ $V_{HISENSE}$ ≤ 12.6 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V	50	60	80	Ω
	4.5 V ≤ $V_{HISENSE}$ ≤ 5.5 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V	62	85	123	
	3 V ≤ $V_{HISENSE}$ ≤ 3.6 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V	67	95	144	
CMRR	$V_{HISENSE}$ = 12.6 V to 3 V, $V_{HISENSE} - V_{OUTLO}$ = 100 mV	69	75		dB

NOTE 2: Ensured by design, not tested.

deadtime

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOHIB	High-level input voltage	See Note 2	2.4			V
LODR		See Note 2	3			
LOHIB	Low-level input voltage	See Note 2			1.4	V
LODR		See Note 2			1.7	

NOTE 2: Ensured by design, not tested.

LODRV

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LODRV	High-level input voltage		1.85			V
	Low-level input voltage				0.95	V

drive regulator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	11.4 V ≤ VCC ≤ 12.6 V, I_{DRV} = 50 mA	7		9	V
Output regulation	1 mA ≤ I_{DRV} ≤ 500 mA		100		mV
Short-circuit current		100			mA

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

bias regulator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	11.4 V ≤ VCC ≤ 12.6 V, See Note 3	6			V

NOTE 3: The bias regulator is designed to provide a quiet bias supply for the TPS56xx controller. External loads should not be driven by the bias regulator.

output drivers

PARAMETER (see Note 4)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output current	High-side sink	Duty cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 1.5 V (SRC) or 5 V (sink), See Note 2	2			A
	High-side source		2			
	Low-side sink	Duty cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, V_{DRV} = 6.5 V, V_{LOWDR} = 1.5 V (SRC) or 5 V (sink), See Note 2	2			
	Low-side source		2			

Output resistance	High-side sink	T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 1.5 V (SRC) or 5 V (sink)	3	Ω
	High-side source		45	
	Low-side sink	T_J = 125°C, V_{DRV} = 6.5 V, V_{LOWDR} = 1.5 V (SRC) or 5 V (sink)	5.7	
	Low-side source		45	

NOTES: 2. Ensured by design, not tested.

4. The pull up/down circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} supply voltage range		11.4	12	13	V
V_{CC} quiescent current	$V_{INHIBIT}$ = 5 V, V_{BOOTLO} = 0 V, V_{CC} > 10.75 V at startup, See Note 2		3	10	mA
	$V_{INHIBIT}$ = 5 V, V_{BOOTLO} = 0 V, C_{LOWDR} = 50 pF, V_{CC} > 10.75 V at startup, C_{HIGHDR} = 50 pF, f_{swx} = 200 kHz		5		
High-side drive regulator quiescent current	$V_{INHIBIT}$ = 0 V or V_{CC} < 9.25 V at startup, V_{BOOT} = 13 V, V_{BOOTLO} = 0 V			10	µA
	$V_{INHIBIT}$ = 5 V, V_{BOOT} = 13 V, C_{HIGHDR} = 50 pF, V_{CC} > 10.75 V at startup, V_{BOOTLO} = 0 V, f_{swx} = 200 kHz		2		mA

NOTE 2: Ensured by design, not tested.

switching characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay	VSENSE to HIGHDR or LOWDR (excluding deadtime)	Overdrive = 10 mV (see Note 2)		150	250	ns
	OCP comparator	See Note 2		1		µs
	OVP comparator	See Note 2		1		
	PWRGD comparator	See Note 2		1		
	SLOWST comparator	Overdrive = 10 mV (see Note 2)		560	900	ns
Rise time	HIGHDR output	C_L = 9 nF, V_{BOOT} = 6.5 V, V_{BOOTLO} = 0 V, T_J = 125°C			60	ns
	LOWDR output	C_L = 9 nF, V_{DRV} = 6.5 V, T_J = 125°C			60	
Fall time	HIGHDR output	C_L = 9 nF, V_{BOOT} = 6.5 V, V_{BOOTLO} = 0 V, T_J = 125°C			60	ns
	LOWDR output	C_L = 9 nF, V_{DRV} = 6.5 V, T_J = 125°C			60	
Deglitch time (includes comparator propagation delay)	OCP	See Note 2	2		5	µs
	OVP	See Note 2	2		5	
Response time	High-side VDS sensing	$V_{HISENSE}$ = 12 V, V_{IOUTLO} pulsed from 12 V to 11.9 V, 100 ns rise/fall times, See Note 2			2	µs
		$V_{HISENSE}$ = 4.5 V, V_{IOUTLO} pulsed from 4.5 V to 4.4 V, 100 ns rise/fall times, See Note 2			3	
		$V_{HISENSE}$ = 3 V, V_{IOUTLO} pulsed from 3 V to 2.9 V, 100 ns rise/fall times, See Note 2			3	
Short-circuit protection rising-edge delay	SCP	LOSENSE = 0 V, (see Note 2)	300		500	ns
Turn-on/turn-off delay	V_{DS} sensing sample/hold switch	3 V ≤ $V_{HISENSE}$ ≤ 11 V, $V_{LOSENSE}$ = $V_{HISENSE}$ (see Note 2)	30		100	ns
Crossover delay time	LOWDR to HIGHDRV, and LOHIB to LOWDR	See Note 2	30		100	ns
Prefilter pole frequency	Hysteretic comparator	See Note 2		5		MHz
Propagation delay	LODRV	See Note 2			400	ns

NOTE 2: Ensured by design, not tested.

TYPICAL CHARACTERISTICS

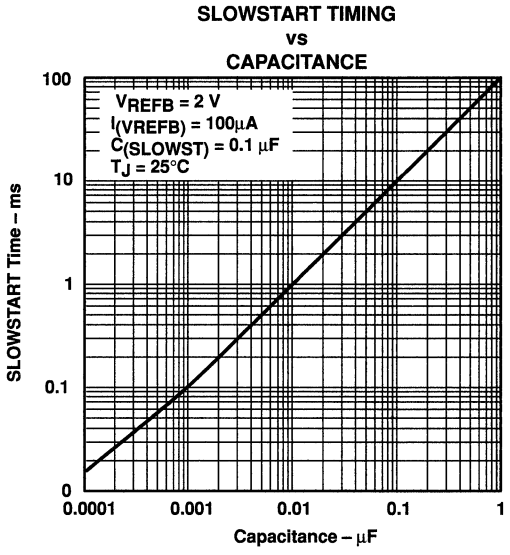


Figure 5

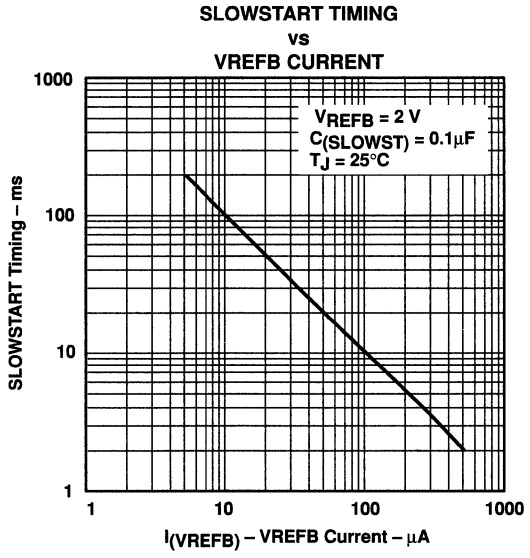


Figure 6

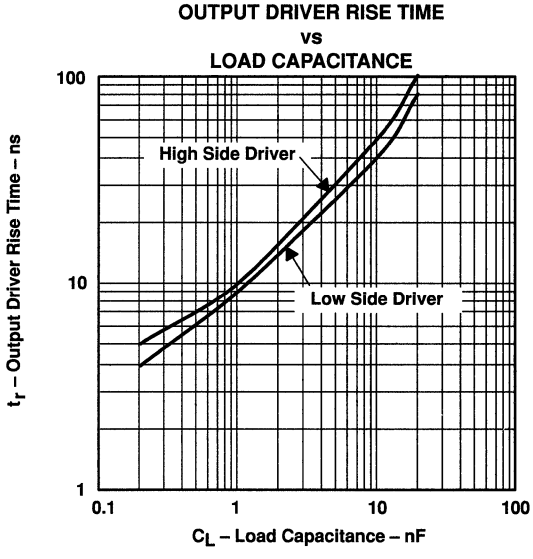


Figure 7

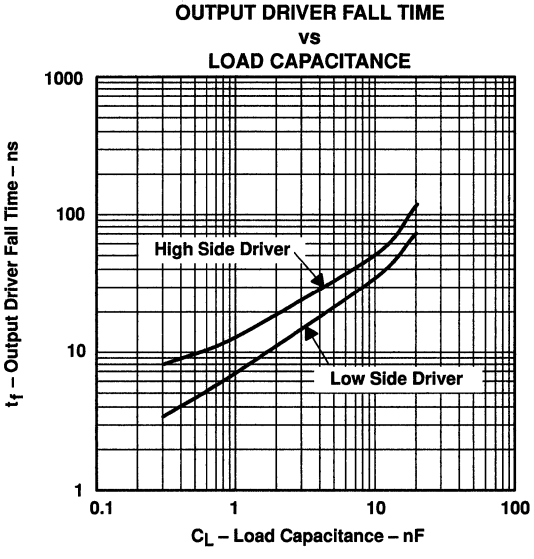


Figure 8

TYPICAL CHARACTERISTICS

OVP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

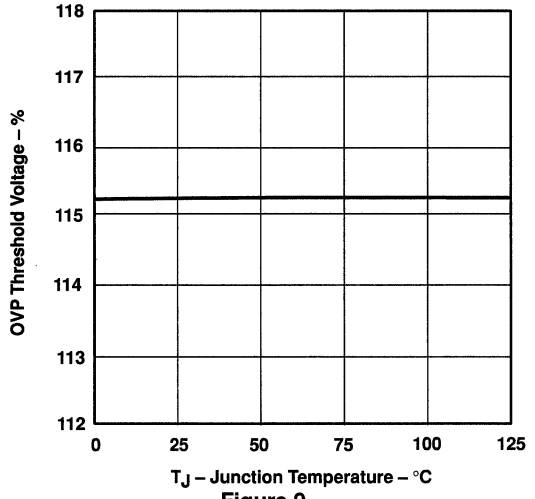


Figure 9

OCP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

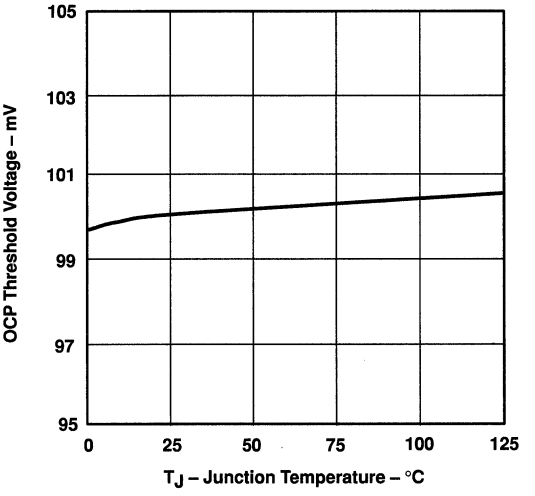


Figure 10

INHIBIT START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

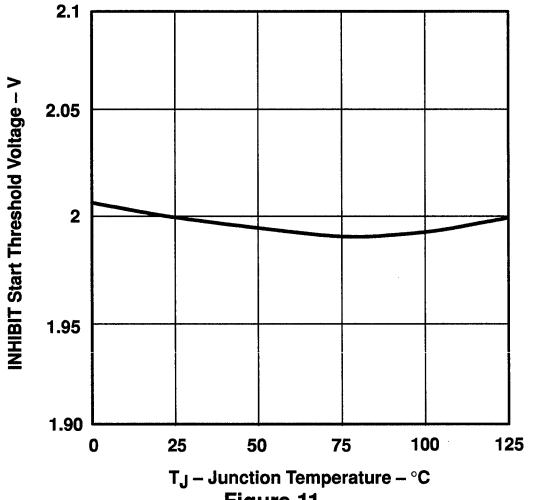


Figure 11

INHIBIT HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

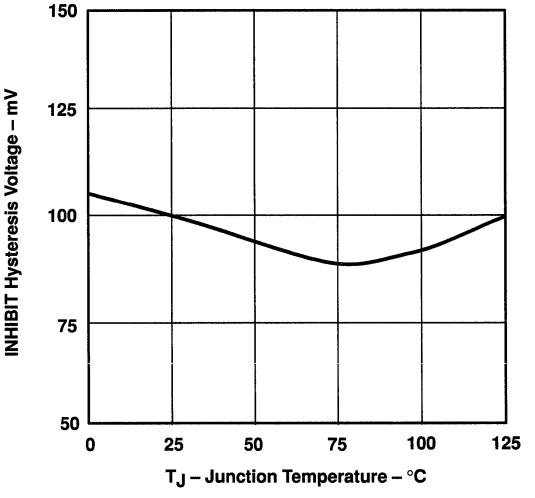


Figure 12

TYPICAL CHARACTERISTICS

UVLO START THRESHOLD VOLTAGE V_{CC}
vs
JUNCTION TEMPERATURE

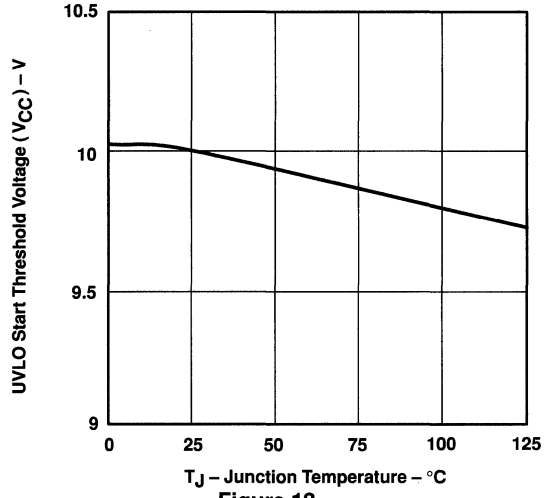


Figure 13

UVLO HYSTERESIS VOLTAGE (V_{CC})
vs
JUNCTION TEMPERATURE

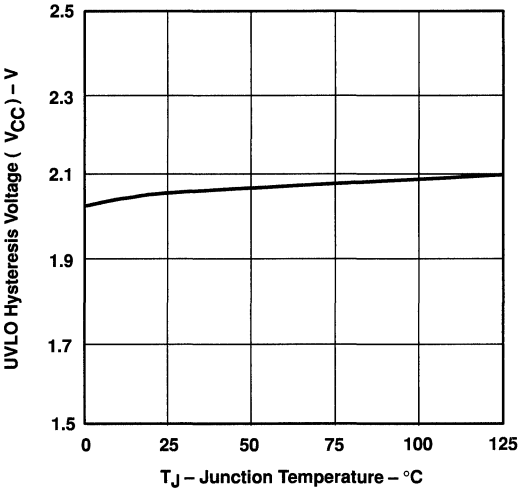


Figure 14

QUIESCENT CURRENT V_{CC}
vs
JUNCTION TEMPERATURE

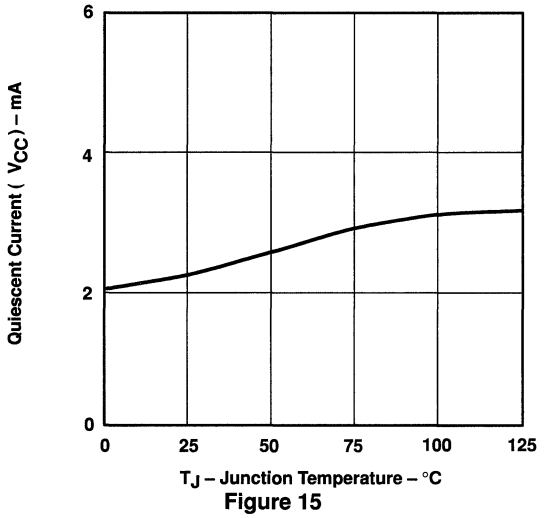


Figure 15

PWRGD THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

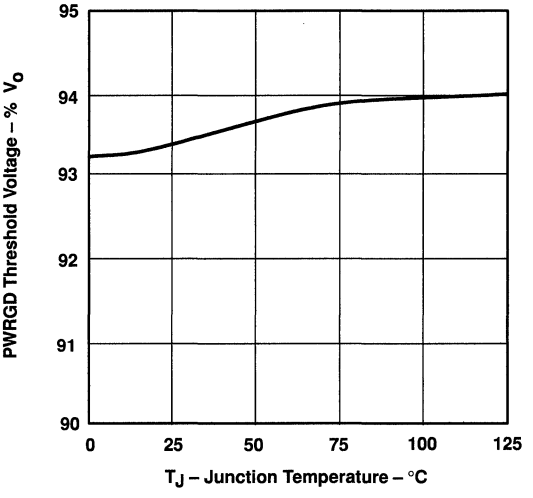


Figure 16

TYPICAL CHARACTERISTICS

SLOWSTART CHARGE CURRENT
vs
JUNCTION TEMPERATURE

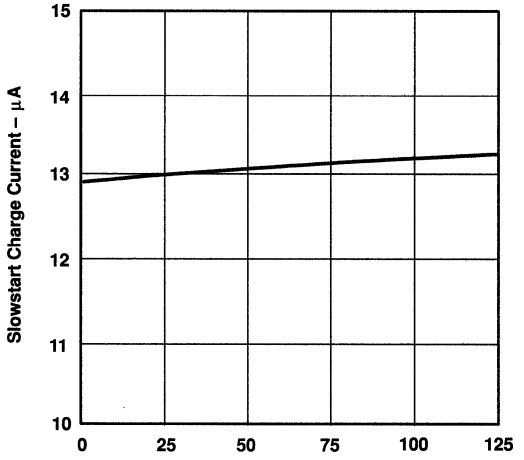


Figure 17

VDS SAMPLE/HOLD RESISTANCE
vs
JUNCTION TEMPERATURE

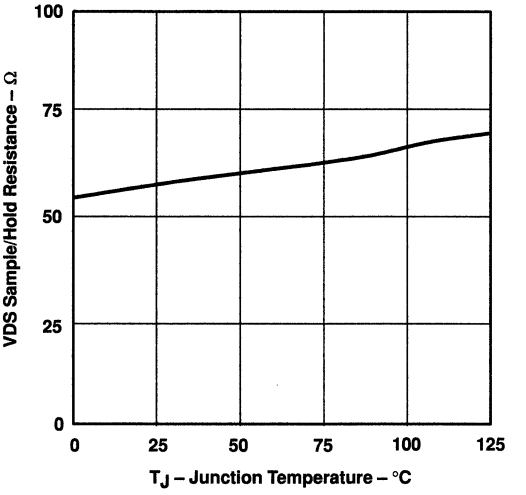


Figure 18

DRIVE REGULATOR OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

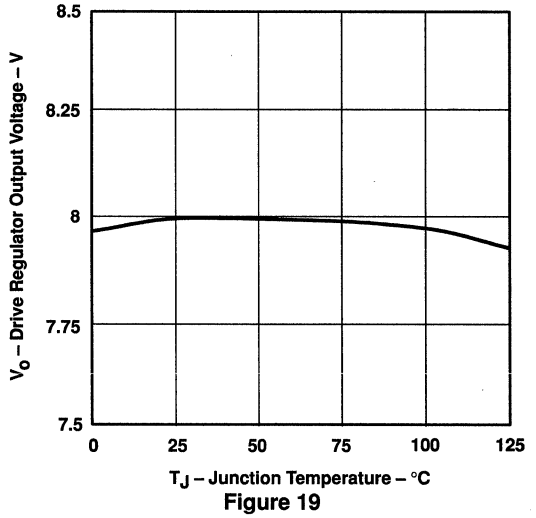


Figure 19

DRIVE REGULATOR LOAD REGULATION
vs
JUNCTION TEMPERATURE

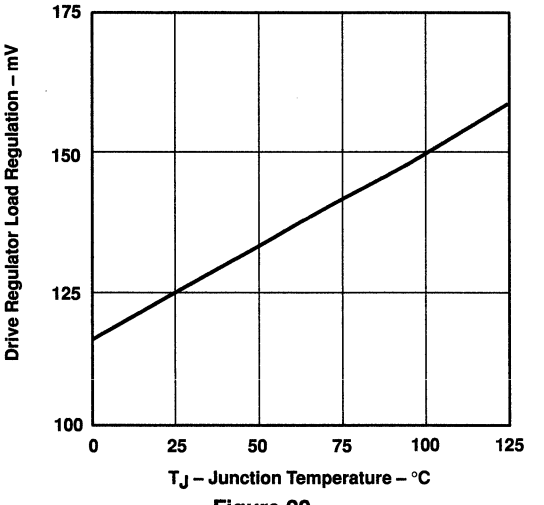


Figure 20

TYPICAL CHARACTERISTICS

DRIVE REGULATOR LINE REGULATION
vs
JUNCTION TEMPERATURE

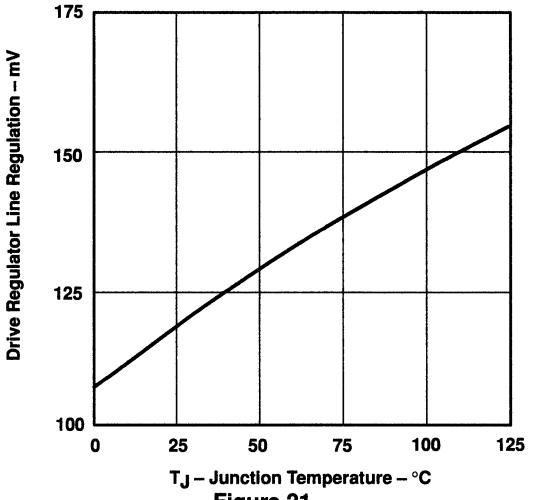


Figure 21

HIGH–SIDE DRIVER OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

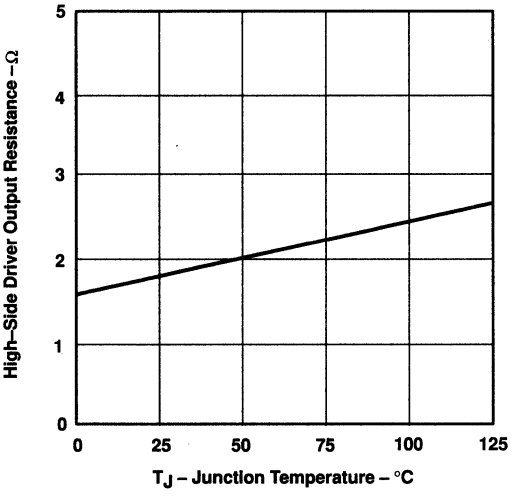


Figure 22

LOW–SIDE DRIVER OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

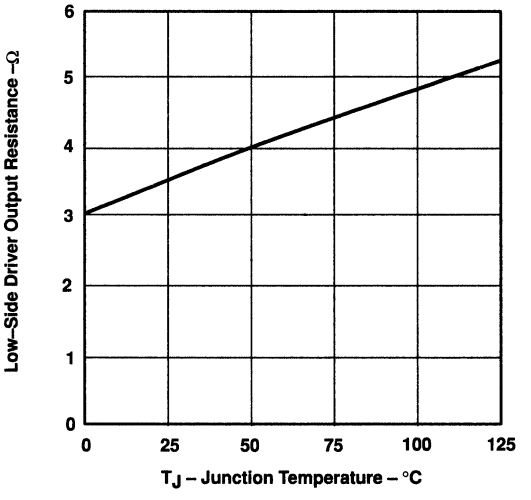


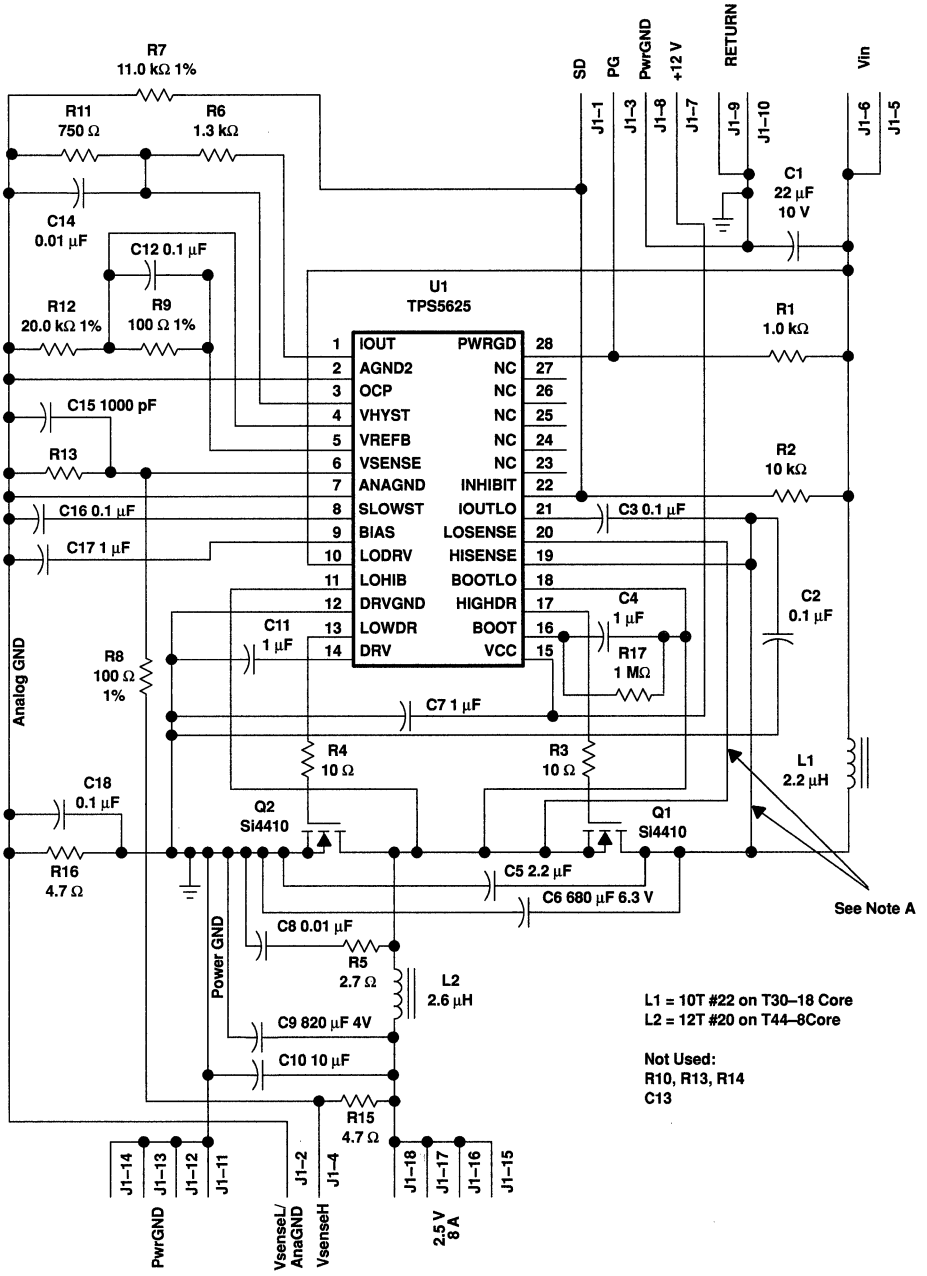
Figure 23

APPLICATION INFORMATION

Synchronous rectifier buck regulator circuits are used where high efficiency and low dropout voltages are required. The TPS56xx controller is useful in applications with very high transient loads and wide dc load ranges, such as multiple-DSP applications.

The circuit below will meet a wide variety of applications with maximum continuous-rated output currents of up to 8 A. Design tradeoffs, such as cost, size, or efficiency may need to be addressed for specific applications. Care should be taken in the proper layout (see last section of this data sheet for specific layout guidelines), especially in the higher-current configurations, to ensure that noise and ripple are kept to a minimum. Basic layout considerations are discussed in the *1996 Power Supply Circuits Databook* (Literature no. SLVD002). Design guidelines and equations are discussed in *Synchronous Buck Converter Design Using TPS56xx Controllers in SLVP10x EVMs User's Guide* (Literature no. SLVU007).

APPLICATION INFORMATION



NOTE A. Theses two traces should be physically close to each other for good noise immunity.

Figure 24. Typical Design Schematic

Table 1. Test Results for 2.5-V, 8-A Converter

TEST	CONDITIONS	QTY	UNITS
Output voltage	V_{IN} = 5.25 V, I_O = 8 A	2.50	V
Load regulation	V_{IN} = 5.25 V, I_O = 0.8 to 8 A	0.4	%
Line regulation	I_O =6 A, V_{CC} = 4.5 V to 6 V	0.2	%
Ripple	V_{IN} = 5.25 V, I_O = 8 A	50	mVpp
Efficiency	V_{IN} = 5.25 V, I_O = 8 A	89	%

Table 2. 2.5-V, 8-A Converter Bill of Materials

REF DES	QTY	PART NUMBER	DESCRIPTION	MFG
C1	1	10SS22M	Capacitor, Os-Con, 22 µF, 10 V, 20%	Sanyo
C2	4	GRM39X7R104K016A	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R	muRata
C3		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R	muRata
C4	4	GRM42-6Y5V105Z016A	Capacitor, Ceramic, 1 µF, 16 V, +80%–20%	muRata
C5	1	GRM42-6Y5V225Z016A	Capacitor, Os-Con, 2.2 µF, 16 V, Y5U	muRata
C6	1	6SP680M	Capacitor, Os-Con, 680 µF, 6.3 V, 20%	Sanyo
C7		GRM42-6Y5V105Z016A	Capacitor, Ceramic, 1 µF, 16 V, +80%–20%	muRata
C8	2	GRM39X7R103K025A	Capacitor, Ceramic, 0.01 µF, 25 V, 10%, X7R	muRata
C9	1	4SP820M	Capacitor, Os-Con, 820 µF, 4 V, 20%	Sanyo
C10	1	GRM235Y5V106Z016A	Capacitor, Ceramic, 10 µF, 16 V, Y5V	muRata
C11		GRM42-6Y5V105Z016A	Capacitor, Ceramic, 1 µF, 16 V, +80%–20%	muRata
C12		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R	muRata
C14		GRM39X7R103K025A	Capacitor, Ceramic, 0.01 µF, 25 V, 10%, X7R	muRata
C15	1	GRM39X7R102K050A	Capacitor, Ceramic, 1000 pF, 50 V, 10%, X7R	muRata
C16		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R	muRata
C17		GRM42-6Y5V105Z016A	Capacitor, Ceramic, 1 µF, 16 V, +80%–20%	muRata
C18		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R	muRata
J1	1	S1122-18-ND	Header, RA, 18-pin, 0.23 Posts × 0.20 Tails	Sullins
L1	1		Inductor, Filter, 2.2 µH, 8.5 A (10T #22 on T30-18 Core)	
L2	1		Inductor, Filter, 2.6 µH, 8.5 A (12T #20 on T44-8 Core)	
Q1	2	Si4410DY	FET, N-ch, 30-V, 10-A, 13-mΩ	Siliconix
Q2		Si4410DY	FET, N-ch, 30-V, 10-A, 13-mΩ	Siliconix
R1	3	Std	Resistor, Chip, 1.0 kΩ, 1/16W, 5%	
R2	1	Std	Resistor, Chip, 10 kΩ, 1/16W, 5%	
R3	2	Std	Resistor, Chip, 10 Ω, 1/10W, 5%	
R4		Std	Resistor, Chip, 10 Ω, 1/10W, 5%	
R5	1	Std	Resistor, Chip, 2.7 Ω, 1/4W, 5%	
R6		Std	Resistor, Chip, 1.3 kΩ, 1/16W, 5%	
R7	1	Std	Resistor, Chip, 11.0 kΩ, 1/16W, 1%	
R8	2	Std	Resistor, Chip, 100 Ω, 1/16W, 1%	
R9		Std	Resistor, Chip, 100 Ω, 1/16W, 1%	
R11		Std	Resistor, Chip, 750 Ω, 1/16W, 5%	
R12	1	Std	Resistor, Chip, 20.0 kΩ, 1/16W, 1%	
R15	2	Std	Resistor, Chip, 4.7 Ω, 1/16W, 5%	
R16		Std	Resistor, Chip, 4.7 Ω, 1/16W, 5%	
R17	1	Std	Resistor, Chip, 1 MΩ, 1/16W, 5%	
U1	1	TPS5625PWP	IC, PWM Ripple Controller, Fixed 2.5 V	TI

APPLICATION INFORMATION

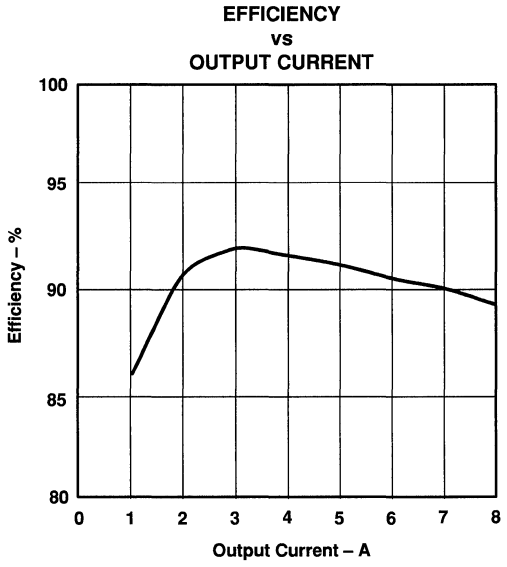


Figure 25

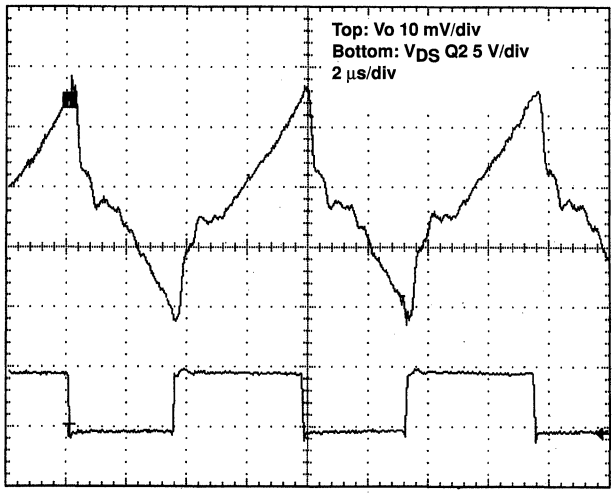


Figure 26. Output Voltage Ripple at 8 A

APPLICATION INFORMATION

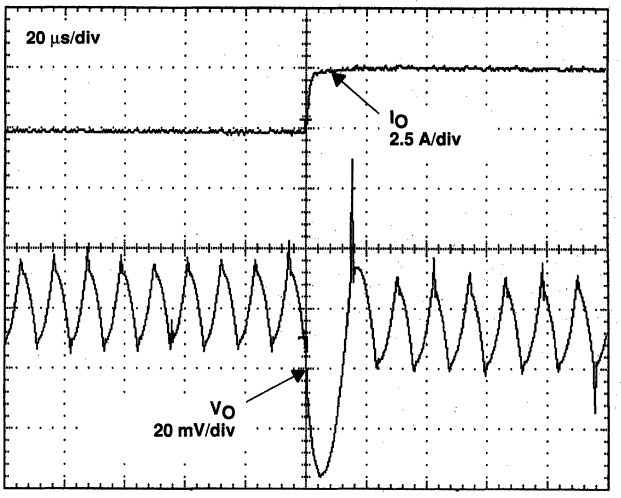


Figure 27. Rising Load Transient Response

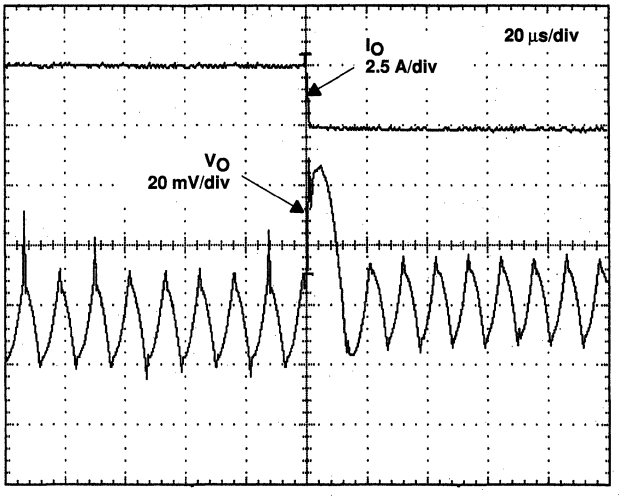


Figure 28. Falling Load Transient Response

APPLICATION INFORMATION

layout guidelines

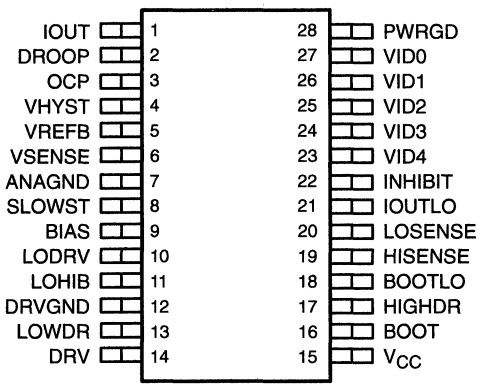
Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB design. The general design should proceed from the switching node to the output, then back to the driver section and, finally, place the low-level components. Below are several specific points to consider before layout of a TPS56xx design begins.

1. All sensitive analog components should be referenced to ANAGND. These include components connected to SLOWST, IOUT, OCP, VSENSE, VREFB, VHYST, BIAS, and LOHIB.
2. Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors, on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.
3. Connections from the drivers to the gate of the power FETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
4. The bypass capacitor for the DRV regulator should be placed close to the TPS56xx and be connected to DRVGND.
5. The bypass capacitor for V_{CC} should be placed close to the TPS56xx and be connected to DRVGND.
6. When configuring the high-side driver as a floating driver, the connection from BOOTLO to the power FETs should be as short and as wide as possible. The other pins that also connect to the power FETs, LOHIB and LOSENSE, should have a separate connection to the FETs, since BOOTLO will have large peak currents flowing through it.
7. When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from BOOT to BOOTLO) should be placed close to the TPS56xx.
8. When configuring the high-side driver as a ground referenced driver, BOOTLO should be connected to DRVGND.
9. The bulk storage capacitors across V_I should be placed close to the power FETs. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and close to the source of the low-side FET.
10. High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
11. HISENSE and LOSENSE should be connected very close to the drain and source, respectively, of the high-side FET. HISENSE and LOSENSE should be routed very close to each other to minimize differential-mode noise coupling to these traces.

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

- ±1% Reference Over Full Operating Temperature Range
- Synchronous Rectifier Driver for Greater Than 90% Efficiency
- Programmable Reference Voltage Range of 1.3 V to 3.5 V
- User–Selectable Hysteretic Type Control
- Droop Compensation for Improved Load Transient Regulation
- Adjustable Overcurrent Protection
- Programmable Softstart
- Overvoltage Protection
- Active Deadtime Control
- Power Good Output
- Internal Bootstrap Schottky Diode
- Low Supply Current . . . 3-mA Typ

DW OR PWP PACKAGE
(TOP VIEW)



description

The TPS5210 is a synchronous-buck regulator controller which provides an accurate, programmable supply voltage to microprocessors. An internal 5-bit DAC is used to program the reference voltage to within a range of 1.3 V to 3.5 V. The output voltage can be set to be equal to the reference voltage or to some multiple of the reference voltage. A hysteretic controller with user-selectable hysteresis and programmable droop compensation is used to dramatically reduce overshoot and undershoot caused by load transients. Propagation delay from the comparator inputs to the output drivers is less than 250 ns. Overcurrent shutdown and crossover protection for the output drivers combine to eliminate destructive faults in the output FETs. The softstart current source is proportional to the reference voltage, thereby eliminating variation of the softstart timing when changes are made to the output voltage. PWRGD monitors the output voltage and pulls the open-collector output low when the output drops 7% below the nominal output voltage. An overvoltage circuit disables the output drivers if the output voltage rises 15% above the nominal value. The inhibit pin can be used to control power sequencing. Inhibit and undervoltage lockout assures the 12-V supply voltage and system supply voltage (5 V or 3.3 V) are within proper operating limits before the controller starts. Single-supply (12 V) operation is easily accomplished using a low-current divider for the required 5-V signals. The output driver circuits include 2-A drivers with internal 8-V gate-voltage regulators. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. The TPS5210 is available in a 28-pin SOIC package and a 28-pin TSSOP PowerPAD™ package. It operates over a junction temperature range of 0°C to 125°C.

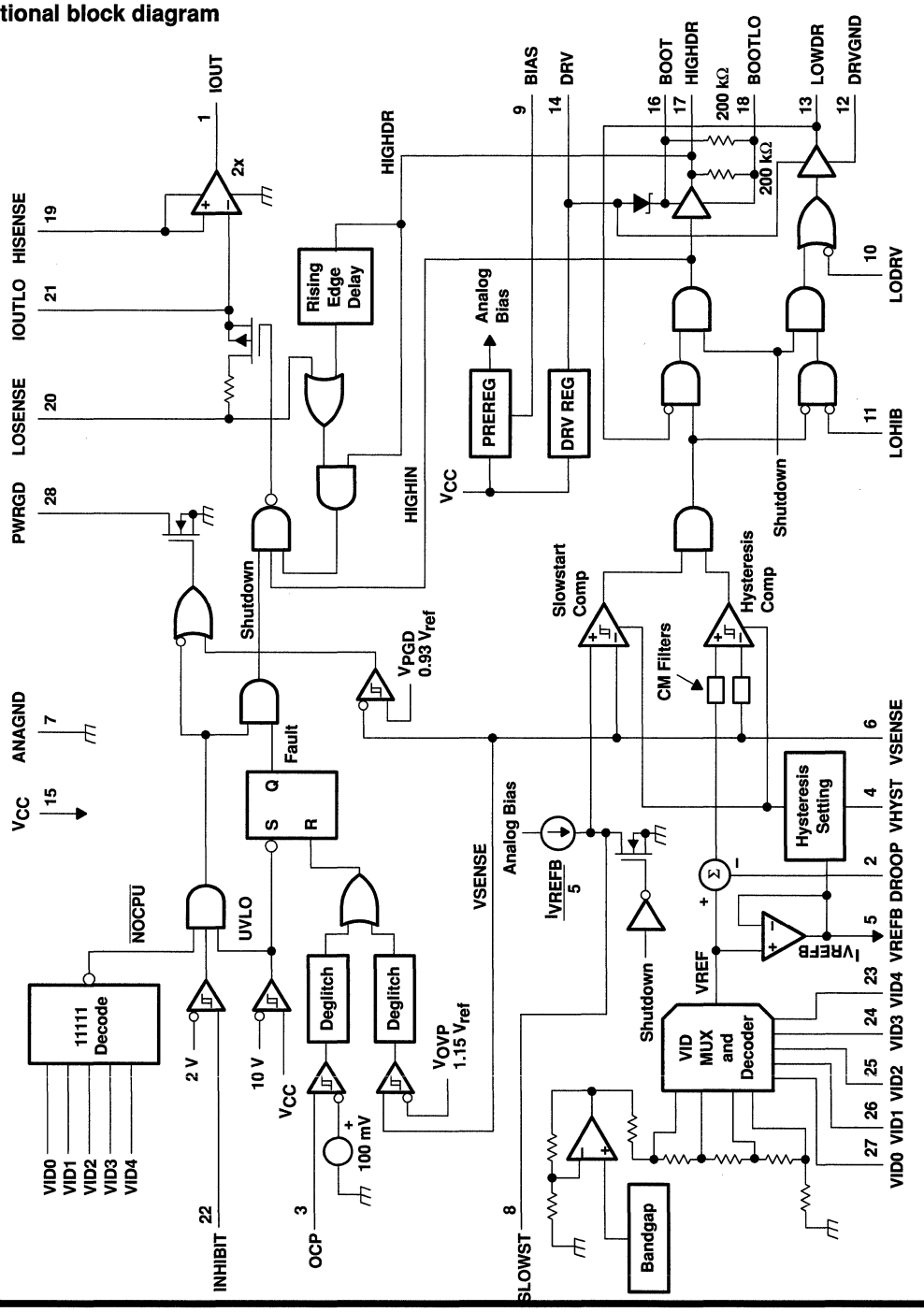
AVAILABLE OPTIONS

T_J	PACKAGES	
	SOIC (DW)	TSSOP (PWP)
0°C to 125°C	TPS5210DW	TPS5210PWPR

The DW package is available taped and reeled. Add R suffix to device type (e.g., TPS5210DWR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANAGND	7		Analog ground
BIAS	9	O	Analog BIAS pin. A 1-µF ceramic capacitor should be connected from BIAS to ANAGND.
BOOT	16	I	Bootstrap. Connect a 1-µF low-ESR capacitor from BOOT to BOOTLO.
BOOTLO	18	O	Bootstrap low. Connect BOOTLO to the junction of the high-side and low-side FETs for floating drive configuration. Connect BOOTLO to PGND for ground reference drive configuration.
DROOP	2	I	Droop voltage. Voltage input used to set the amount of output-voltage set-point droop as a function of load current. The amount of droop compensation is set with a resistor divider between IOUT and ANAGND.
DRV	14	O	Drive regulator for the FET drivers. A 1-µF ceramic capacitor should be connected from DRV to DRVGND.
DRVGND	12		Drive ground. Ground for FET drivers. Connect to FET PWRGND.
HIGHDR	17	O	High drive. Output drive to high-side power switching FETs
HISENSE	19	I	High current sense. For current sensing across high-side FETs, connect to the drain of the high-side FETs; for optional resistor sensing scheme, connect to power supply side of current-sense resistor placed in series with high-side FET drain.
INHIBIT	22	I	Disables the drive signals to the MOSFET drivers. Can also serve as UVLO for system logic supply (either 3.3 V or 5 V).
IOUT	1	O	Current out. Output voltage on this pin is proportional to the load current as measured across the Rds(on) of the high-side FETs. The voltage on this pin equals 2×Rds(on)×IOUT. In applications where very accurate current sensing is required, a sense resistor should be connected between the input supply and the drain of the high-side FETs.
IOUTLO	21	O	Current sense low output. This is the voltage on the LOSENSE pin when the high-side FETs are on. A ceramic capacitor should be connected from IOUTLO to HISENSE to hold the sensed voltage while the high-side FETs are off. Capacitance range should be between 0.033 µF and 0.1 µF.
LODRV	10	I	Low drive enable. Normally tied to 5 V. To activate the low-side FETs as a crowbar, pull LODRV low.
LOHIB	11	I	Low side inhibit. Connect to the junction of the high and low side FETs to control the anti-cross-conduction and eliminate shoot-through current. Disabled when configured in crowbar mode.
LOSENSE	20	I	Low current sense. For current sensing across high-side FETs, connect to the source of the high-side FETs; for optional resistor sensing scheme, connect to high-side FET drain side of current-sense resistor placed in series with high-side FET drain.
LOWDR	13	O	Low drive. Output drive to synchronous rectifier FETs
OCP	3	I	Over current protection. Current limit trip point is set with a resistor divider between IOUT and ANAGND.
PWRGD	28	O	Power good. Power Good signal goes high when output voltage is within 7% of voltage set by VID pins. Open-drain output.
SLOWST	8	O	Slow Start (soft start). A capacitor from SLOWST to ANAGND sets the slowstart time. Slowstart current = $I_{VREFB}/5$
V_{CC}	15		12-V supply. A 1-µF ceramic capacitor should be connected from V_{CC} to DRVGND.
VHYST	4	I	HYSTERESIS set pin. The hysteresis is set with a resistor divider from V_{REFB} to ANAGND. The hysteresis window = $2 \times (V_{REFB} - V_{HYST})$
VID0	27	I	Voltage Identification input 0
VID1	26	I	Voltage Identification input 1
VID2	25	I	Voltage Identification input 2
VID3	24	I	Voltage Identification input 3
VID4	23	I	Voltage Identification input 4. Digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in Table 1. Internally pulled up to 5 V with a resistor divider biased from V_{CC}.
VREFB	5	O	Buffered reference voltage from VID network
VSENSE	6	I	Voltage sense Input. To be connected to converter output voltage bus to sense and control output voltage. It is recommended an RC low pass filter be connected at this pin to filter noise.

detailed description

V_{REF}

The reference/voltage identification (VID) section consists of a temperature-compensated bandgap reference and a 5-bit voltage selection network. The 5 VID terminals are inputs to the VID selection network and are TTL-compatible inputs internally pulled up to 5 V by a resistor divider connected to V_{CC}. The VID codes conform to the Intel *VRM 8.3 DC-DC Converter Specification* for voltage settings between 1.8 V and 3.5 V, and they are decremented by 50 mV, down to 1.3 V, for the lower VID settings. Voltages higher than V_{REF} can be implemented using an external divider. Refer to Table 1 for the VID code settings. The output voltage of the VID network, V_{REF}, is within ±1% of the nominal setting over the VID range of 1.3 V to 2.5 V, including a junction temperature range of 5°C to +125°C, and a V_{CC} supply voltage range of 11.4 V to 12.6 V. The output of the reference/VID network is indirectly brought out through a buffer to the V_{REFB} pin. The voltage on this pin will be within 2% of V_{REF}. It is not recommended to drive loads with V_{REFB}, other than setting the hysteresis of the hysteretic comparator, because the current drawn from V_{REFB} sets the charging current for the slowstart capacitor. Refer to the slowstart section for additional information.

hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by 2 external resistors and is centered on V_{REF}. The 2 external resistors form a resistor divider from V_{REFB} to ANAGND, with the output voltage connecting to the V_{HYST} pin. The hysteresis of the comparator will be equal to twice the voltage *difference* between the V_{REFB} and V_{HYST} pins. The propagation delay from the comparator inputs to the driver outputs is 250 ns (maximum). The maximum hysteresis setting is 60 mV.

low-side driver

The low-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The bias to the low-side driver is internally connected to the DRV regulator.

high-side driver

The high-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from the DRV regulator. The internal bootstrap diode, connected between the DRV and BOOT pins, is a Schottky for improved drive efficiency. The maximum voltage that can be applied between BOOT and DRVGND is 30 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting BOOT to either DRV or V_{CC}.

deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate-drive voltage to the low-side FETs is below 2 V; the low-side driver is not allowed to turn on until the voltage at the junction of the high-side and low-side FETs (Vphase) is below 2 V.

current sensing

Current sensing is achieved by sampling and holding the voltage across the high-side power FETs while the high-side FETs are on. The sampling network consists of an internal 60-Ω switch and an external ceramic hold capacitor. Recommended value of the hold capacitor is between 0.033 µF and 0.1 µF. Internal logic controls the turn-on and turn-off of the sample/hold switch such that the switch does not turn on until the Vphase voltage transitions high, and the switch turns off when the input to the high-side driver goes low. The sampling will occur only when the high-side FETs are conducting current. The voltage on the IOUT pin equals 2 times the sensed high-side voltage. In applications where a higher accuracy in current sensing is required, a sense resistor can be placed in series with the high-side FETs, and the voltage across the sense resistor can be sampled by the current sensing circuit.

detailed description (continued)

droop compensation

The droop compensation network reduces the load transient overshoot/undershoot on V_O, relative to V_{REF}. V_O is programmed to a voltage greater than V_{REF} by an external resistor divider from V_O to VSENSE to reduce the undershoot on V_O during a low-to-high load transient. The overshoot during a high-to-low load transient is reduced by subtracting the voltage on DROOP from V_{REF}. The voltage on IOUT is divided with an external resistor divider, and connected to DROOP.

inhibit

INHIBIT is a TTL-compatible digital input used to enable the controller. When INHIBIT is low, the output drivers are low and the slowstart capacitor is discharged. When INHIBIT goes high, the short across the slowstart capacitor is released and normal converter operation begins. When the system-logic supply is connected to INHIBIT, it also controls power sequencing by locking out controller operation until the system-logic supply exceeds the input threshold voltage of the inhibit circuit. The 12-V supply and the system logic supply (either 5 V or 3.3 V) must be above UVLO thresholds before the controller is allowed to start up. The start threshold is 2.1 V and the hysteresis is 100 mV for the INHIBIT comparator.

V_{CC} undervoltage lockout (UVLO)

The undervoltage lockout circuit disables the controller while the V_{CC} supply is below the 10-V start threshold during power up. When the controller is disabled, the output drivers will be low and the slowstart capacitor is discharged. When V_{CC} exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 2-V hysteresis in the undervoltage lockout circuit for noise immunity.

slowstart

The slowstart circuit controls the rate at which V_O powers up. A capacitor is connected between SLOWST and ANAGND and is charged by an internal current source. The current source is proportional to the reference voltage, so that the charging rate of C_{slowst} is proportional to the reference voltage. By making the charging current proportional to V_{REF}, the power-up time for V_O will be independent of V_{REF}. Thus, C_{SLOWST} can remain the same value for all VID settings. The slowstart charging current is determined by the following equation:

$$I_{slowstart} = I(V_{REFB}) / 5 \quad \text{(amps)}$$

Where $I(V_{REFB})$ is the current flowing out of V_{REFB}.

It is recommended that no additional loads be connected to V_{REFB}, other than the resistor divider for setting the hysteresis voltage. The maximum current that can be sourced by the V_{REFB} circuit is 500 μA. The equation for setting the slowstart time is:

$$t_{SLOWST} = 5 \times C_{SLOWST} \times R_{VREFB} \quad \text{(seconds)}$$

Where R_{VREFB} is the total external resistance from V_{REFB} to ANAGND.

power good

The power-good circuit monitors for an undervoltage condition on V_O. If V_O is 7% below V_{REF}, then the PWRGD pin is pulled low. PWRGD is an open-drain output.

overvoltage protection

The overvoltage protection (OVP) circuit monitors V_O for an overvoltage condition. If V_O is 15% above V_{REF}, then a fault latch is set and both output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value. A 3-μs deglitch timer is included for noise immunity. Refer to the LODRV section for information on how to protect the microprocessor against overvoltages due to a shorted fault across the high-side power FET.

detailed description (continued)

overcurrent protection

The overcurrent protection (OCP) circuit monitors the current through the high-side FET. The overcurrent threshold is adjustable with an external resistor divider between IOUT and ANAGND, with the divider voltage connected to the OCP pin. If the voltage on OCP exceeds 100 mV, then a fault latch is set and the output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value. A 3-µs deglitch timer is included for noise immunity. The OCP circuit is also designed to protect the high-side power FET against a short-to-ground fault on the terminal common to both power FETs.

drive regulator

The drive regulator provides drive voltage to the output drivers. The minimum drive voltage is 7 V. The minimum short circuit current is 100 mA. Connect a 1-µF ceramic capacitor from DRV to DRVGND.

LODRV

The LODRV circuit is designed to protect the microprocessor against overvoltages that can occur if the high-side power FETs become shorted. External components to sense an overvoltage condition are required to use this feature. When an overvoltage fault occurs, the low-side FETs are used as a crowbar. LODRV is pulled low and the low-side FET will be turned on, overriding all control signals inside the TPS5210 controller. The crowbar action will short the input supply to ground through the faulted high-side FETs and the low-side FETs. A fuse in series with V_{in} should be added to disconnect the short-circuit.

Table 1. Voltage Identification Codes

VID TERMINALS (0 = GND, 1 = floating or pull-up to 5 V)					V_{REF}
VID4	VID3	VID2	VID1	VID0	(Vdc)
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	No CPU
1	1	1	1	0	2.10
1	1	1	0	1	2.20
1	1	1	0	0	2.30
1	1	0	1	1	2.40
1	1	0	1	0	2.50
1	1	0	0	1	2.60

Table 1. Voltage Identification Codes (Continued)

VID TERMINALS (0 = GND, 1 = floating or pull-up to 5 V)					V_{REF}
VID4	VID3	VID2	VID1	VID0	(Vdc)
1	1	0	0	0	2.70
1	0	1	1	1	2.80
1	0	1	1	0	2.90
1	0	1	0	1	3.00
1	0	1	0	0	3.10
1	0	0	1	1	3.20
1	0	0	1	0	3.30
1	0	0	0	1	3.40
1	0	0	0	0	3.50

absolute maximum ratings over operating virtual junction temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note1) ..... –0.3 V to 14 V
Input voltage range: BOOT to DRVGND (High-side Driver ON) ..... –0.3 V to 30 V
BOOT to HIGHDRV ..... –0.3 V to 15 V
BOOT to BOOTLO ..... –0.3 V to 15 V
INHIBIT, VIDx, LODRV ..... –0.3 V to 7.3 V
PWRGD, OCP, DROOP ..... –0.3 V to 7 V
LOHIB, LOSENSE, IOUTLO, HISENSE ..... –0.3 V to 14 V
VSENSE ..... –0.3 V to 5 V
Voltage difference between ANAGND and DRVGND ..... ±0.5 V
Output current, V_{REFB} ..... 0.5 mA
Short circuit duration, DRV ..... Continuous
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... 0°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to ANAGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1200 mW	12 mW/°C	660 mW	480 mW
PWP	1150 mW	11.5 mW/°C	630 mW	460 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	11.4	13	V
Input voltage, BOOT to DRVGND	0	28	V
Input voltage, BOOT to BOOTLO	0	13	V
Input voltage, INHIBIT, VIDx, LODRV, PWRGD, OCP, DROOP	0	6	V
Input voltage, LOHIB, LOSENSE, IOUTLO, HISENSE	0	13	V
Input voltage, VSENSE	0	4.5	V
Voltage difference between ANAGND and DRVGND	0	±0.2	V
Output current, V_{REFB}†	0	0.4	mA

† Not recommended to load V_{REFB} other than to set hystersis since I_{VREFB} sets slowstart time.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted)

reference/voltage identification

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage accuracy, (Includes offset of droop compensation network)	V_{CC} = 11.4 to 12.6 V, 1.3 V ≤ V_{REF} ≤ 2.5 V	–0.01		0.01	V/V
		V_{CC} = 11.4 to 12.6 V, V_{REF} = 2.6 V	–0.0104		0.0104	V/V
		V_{CC} = 11.4 to 12.6 V, V_{REF} = 2.7 V	–0.0108		0.0108	V/V
		V_{CC} = 11.4 to 12.6 V, V_{REF} = 2.8 V	–0.0112		0.0112	V/V
		V_{CC} = 11.4 to 12.6 V, V_{REF} = 2.9 V	–0.0116		0.0116	V/V
		V_{CC} = 11.4 to 12.6 V, V_{REF} = 3 V	–0.0120		0.0120	V/V
		V_{CC} = 11.4 to 12.6 V, V_{REF} = 3.1 V	–0.0124		0.0124	V/V
		V_{CC} = 11.4 to 12.6 V, V_{REF} = 3.2 V	–0.0128		0.0128	V/V
		V_{CC} = 11.4 to 12.6 V, V_{REF} = 3.3 V	–0.0132		0.0132	V/V
		V_{CC} = 11.4 to 12.6 V, V_{REF} = 3.4 V	–0.0136		0.0136	V/V
		V_{CC} = 11.4 to 12.6 V, V_{REF} = 3.5 V	–0.0140		0.0140	V/V
	Cumulative reference accuracy (see Note 2)	V_{REF} = 1.3 V, Hysteresis window = 30 mV	–0.011		0.011	V/V
		V_{REF} =1.3 V, Hysteresis, T_J = 60°C window = 30 mV (see Note 3)	–0.008		0.008	
		V_{REF} = 1.9 Vv, Hysteresis, T_J = 60°C window = 30 mV (see Note 3)	–0.0090		0.0090	
		V_{REF} = 3.5 V, Hysteresis, T_J = 60°C window = 30 mV (see Note 3)	–0.0115		0.0115	
VIDx	High-level input voltage		2.25			V
VIDx	Low-level input voltage				1	V
V_{REFB}	Output voltage	I_{VREFB} = 50 µA	V_{REF}–2%	V_{REF}	V_{REF}+2%	V
	Output regulation	10 µA ≤ I_O ≤ 500 µA		2		mV
VIDx	Input resistance	VIDx = 0 V	36	73	95	kΩ
	Input pull-up voltage divider		4.8	4.9	5	V

NOTES: 2. Cumulative reference accuracy is the combined accuracy of the reference voltage and the input offset voltage of the hysteretic comparator. Cumulative accuracy equals the average of the high-level and low-level thresholds of the hysteretic comparator.
3. This parameter is ensured by design and is not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

power good

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Undervoltage trip threshold		90	93	95	%V_{REF}
V_{OL}	Low-level output voltage	I_O = 5 mA		0.5	0.75	V
I_{OH}	High-level input current	V_{PWRGD} = 6 V		1		µA
V_{hys}	Hysteresis voltage		1.3	2.9	4.5	%V_{REF}

slowstart

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge current	V_{SLOWST} = 0.5 V, V_{VREFB} = 1.3 V, I_{VREFB} = 65 µA	10.4	13	15.6	µA
Discharge current	V_{SLOWST} = 1 V		3		mA
Comparator input offset voltage				10	mV
Comparator input bias current	See Note 3		10	100	nA
Comparator hysteresis		–7.5		7.5	mV

NOTE 3: This parameter is ensured by design and is not production tested.

hysteretic comparator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	V_{DROOP} = 0 V (see Note 3)	–2.5		2.5	mV
Input bias current	See Note 3			500	nA
Hysteresis accuracy	$V_{REFB} – V_{HYST}$ = 15 mV (Hysteresis window = 30 mV)	–3.5		3.5	mV
Maximum hysteresis setting	$V_{REFB} – V_{HYST}$ = 30 mV		60		mV

NOTE 3: This parameter is ensured by design and is not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

high-side VDS sensing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain			2		V/V
	Initial accuracy	$V_{HISENSE}$ = 12 V, $V_{LOSENSE}$ = 11.9 V, Differential input to V_{ds} sensing amp = 100 mV	194		206	mV
IOUTLO	Sink current	5 V ≤ V_{IOUTLO} ≤ 13 V			250	nA
IOUT	Source current	V_{IOUT} = 0.5 V, $V_{HISENSE}$ = 12 V, V_{IOUTLO} = 11.5 V	500			µA
IOUT	Sink current	V_{IOUT} = 0.05 V, $V_{HISENSE}$ = 12 V, V_{IOUTLO} = 12 V	50			µA
	Output voltage swing	$V_{HISENSE}$ = 11 V, R_{IOUT} = 10 kΩ	0		2	V
		$V_{HISENSE}$ = 4.5 V, R_{IOUT} = 10 kΩ	0		1.5	V
		$V_{HISENSE}$ = 3 V, R_{IOUT} = 10 kΩ	0		0.75	V
LOSENSE	High-level input voltage	$V_{HISENSE}$ = 4.5 V (see Note 3)	2.85			V
	Low-level input voltage				2.4	V
	Sample/hold resistance	11.4 V ≤ $V_{HISENSE}$ ≤ 12.6 V, LOSENSE connected to HISENSE, $V_{HISENSE}$ – V_{IOUTLO} = 0.15 V	50	60	80	Ω
		4.5 V ≤ $V_{HISENSE}$ ≤ 5.5 V, LOSENSE connected to HISENSE, $V_{HISENSE}$ – V_{IOUTLO} = 0.15 V	62	85	123	Ω
		3 V ≤ $V_{HISENSE}$ ≤ 3.6 V, LOSENSE connected to HISENSE, $V_{HISENSE}$ – V_{IOUTLO} = 0.15 V	67	95	144	Ω
CMRR		$V_{HISENSE}$ = 12.6 V to 3 V, $V_{HISENSE}$ – V_{OUTLO} = 100 mV	69	75		dB

NOTE 3. This parameter is ensured by design and is not production tested.

inhibit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		1.9	2.1	2.35	V
Hysteresis		0.08	0.1	0.12	V
Stop threshold		1.85			V

overvoltage protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overvoltage trip threshold		112	115	120	%V_{REF}
Hysteresis	See Note 3		10		mV

NOTE 3: This parameter is ensured by design and is not production tested.

overcurrent protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OCP trip threshold		90	100	110	mV
Input bias current				100	nA

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

deadtime

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOHIB	High-level input voltage		2.4			V
	Low-level input voltage				1.4	
LOWDR	High-level input voltage	See Note 3	3			V
	Low-level input voltage	See Note 3			1.7	

NOTE 3: This parameter is ensured by design and is not production tested.

LODRV

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LODRV	High-level input voltage		1.85			V
	Low-level input voltage				0.95	

droop compensation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial accuracy	V_{DROOP} = 50 mV	46		54	mV

drive regulator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	11.4 V ≤ V_{CC} ≤ 12.6 V, I_{DRV} = 50 mA	7		9	V
Output regulation	1 mA ≤ I_{DRV} ≤ 50 mA		100		mV
Short-circuit current		100			mA

bias regulator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	11.4 V ≤ V_{CC} ≤ 12.6 V, See Note 4	6			V

NOTE 4: The bias regulator is designed to provide a quiet bias supply for the TPS5210 controller. External loads should not be driven by the bias regulator.

input undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		9.25	10	10.75	V
Hysteresis		1.9	2	2.2	V
Stop threshold		7.5			V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

output drivers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output current (see Note 5)	High-side sink	Duty cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 6.5 V,	2			A
	High-side source	V_{HIGHDR} = 1.5 V (source) or 6 V (sink), See Note 3	2			
	Low-side sink	Duty Cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, V_{DRV} = 6.5 V,	2			
	Low-side source	V_{LOWDR} = 1.5 V (source) or 5 V (sink), See Note 3	2			
Output resistance (see Note 5)	High-side sink	T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 6 V (source) or 0.5 V (sink)			3	Ω
	High-side source				45	
	Low-side sink	T_J = 125°C, V_{DRV} = 6.5 V, V_{LOWDR} = 6 V (source) or 0.5 V (sink)			5.7	
	Low-side source				45	

NOTES: 3. This parameter is ensured by design and is not production tested.
5. The pull-up/pull-down circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{ds(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		11.4	12	13	V
V_{CC}	Quiescent current	$V_{INHIBIT}$ = 5 V, VID code ≠ 11111, V_{CC} > 10.75 V at startup, V_{BOOTLO} = 0 V		3	10	mA
		$V_{INHIBIT}$ = 5 V, VID code ≠ 11111, V_{CC} > 10.75 V at startup, V_{BOOTLO} = 0 V, C_{HIGHDR} = 50 pF, C_{LOWDR} = 50 pF, f_{SWX} = 200 kHz, See Note 3		5		
	High-side driver quiescent current	$V_{INHIBIT}$ = 0 V or VID code = 11111 or V_{CC} < 9.25 V at startup, V_{BOOT} = 13 V, V_{BOOTLO} = 0 V			80	µA
		$V_{INHIBIT}$ = 5 V, VID code ≠ 11111, V_{CC} > 10.75 V at startup, V_{BOOT} = 13 V, V_{BOOTLO} = 0 V, C_{HIGHDR} = 50 pF, f_{SWX} = 200 kHz (see Note 3)		2		mA

NOTE 3: This parameter is ensured by design and is not production tested.

switching characteristics over recommended operating virtual-junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay	VSENSE to HIGHDR or LOWDR (excluding dead-time)	1.3 V ≤ V_{VREF} ≤ 3.5 V, 10 mV overdrive (see Note 3)		150	250	ns
	OCP comparator	See Note 3		1		µs
	OVP comparator			1		
	PWRGD comparator			1		
	SLOWST comparator	Overdrive = 10 mV (see Note 3)		560	900	ns
Rise time	HIGHDR output	C_L = 9 nF, V_{BOOTLO} = 0 V, V_{BOOT} = 6.5 V, T_J = 125°C			60	ns
	LOWDR output	C_L = 9 nF, T_J = 125°C, V_{DRV} = 6.5 V			60	
Fall time	HIGHDR output	C_L = 9 nF, V_{BOOTLO} = 0 V, V_{BOOT} = 6.5 V, T_J = 125°C			60	ns
	LOWDR output	C_L = 9 nF, T_J = 125°C, V_{DRV} = 6.5 V			60	
Deglitch time (Includes comparator propagation delay)	OCP	See Note 3	2		5	µs
	OVP		2		5	
Response time	High-side VDS sensing	$V_{HISENSE}$ = 12 V, V_{IOUTLO} pulsed from 12 V to 11.9 V, 100 ns rise/fall times (see Note 3)			2	µs
		$V_{HISENSE}$ = 4.5 V, V_{IOUTLO} pulsed from 4.5 V to 4.4 V, 100 ns rise/fall times (see Note 3)			3	
		$V_{HISENSE}$ = 3 V, V_{IOUTLO} pulsed from 3 V to 2.9 V, 100 ns rise/fall times (see Note 3)			3	
Short-circuit protection rising-edge delay	SCP	LOSENSE = 0 V (see Note 3)	300		500	ns
Turn-on/turn-off delay	V_{DS} sensing sample/hold switch	3 V ≤ $V_{HISENSE}$ ≤ 11 V, $V_{LOSENSE}$ = $V_{HISENSE}$ (see Note 3)	30		100	ns
Crossover delay time	LOWDR to HIGHDRV, and LOHIB to LOWDR	See Note 3	30		100	ns
Prefilter pole frequency	Hysteretic comparator	See Note 3		5		MHz
Propagation delay	LODRV	See Note 3			400	ns

NOTE 3: This parameter is ensured by design and is not production tested.

TYPICAL CHARACTERISTICS

SLOWSTART TIME
vs
SLOWSTART CAPACITANCE

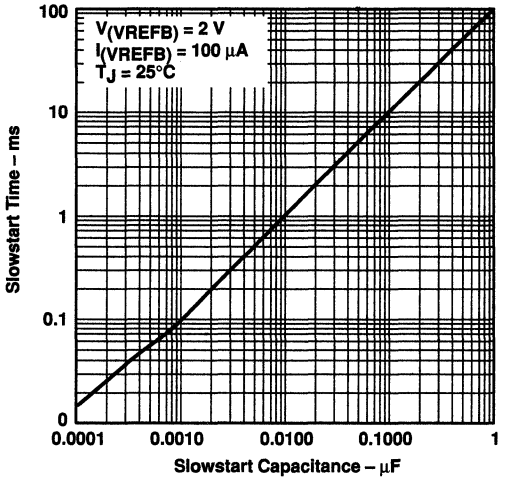


Figure 1

SLOWSTART TIME
vs
SUPPLY CURRENT (VREFB)

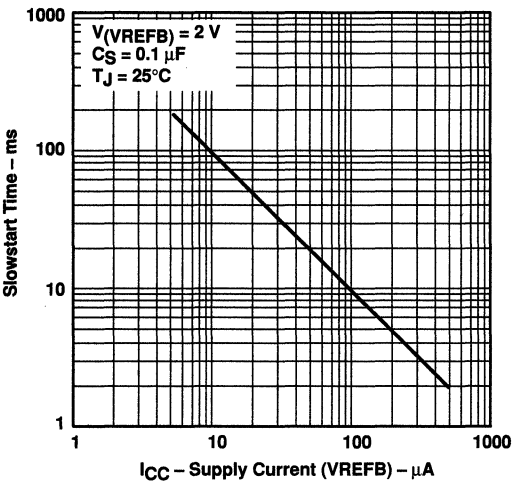


Figure 2

DRIVER
OUTPUT RISE TIME
vs
LOAD CAPACITANCE

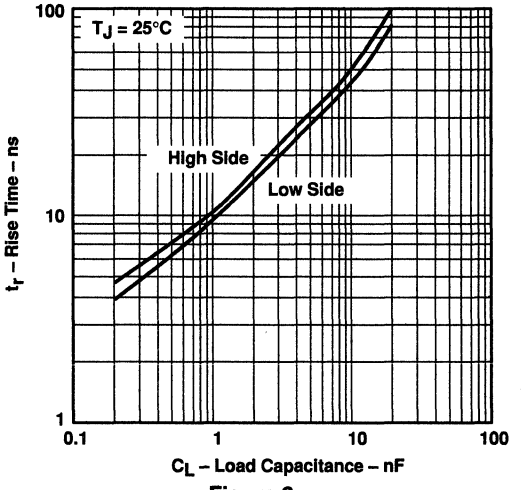


Figure 3

DRIVER
OUTPUT FALL TIME
vs
LOAD CAPACITANCE

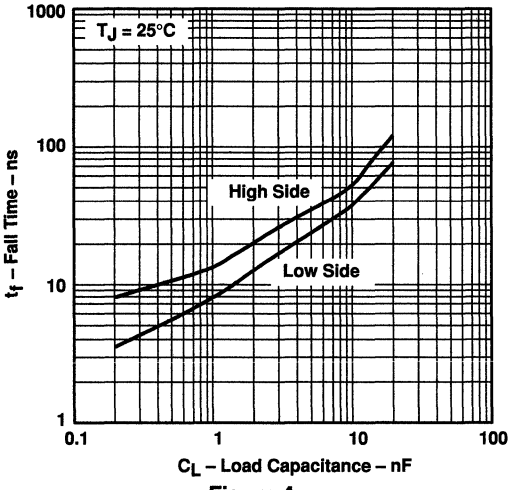


Figure 4

TYPICAL CHARACTERISTICS

OVP THRESHOLD
vs
JUNCTION TEMPERATURE

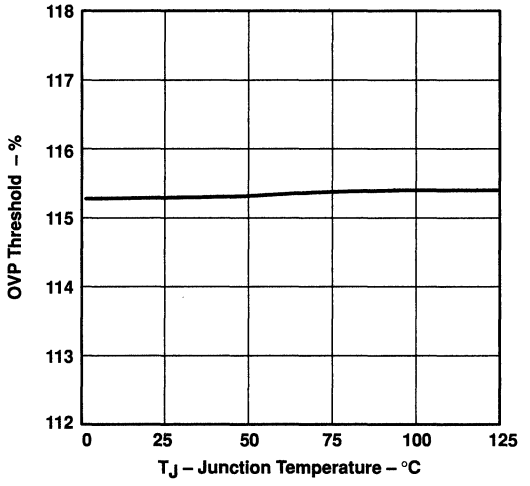


Figure 5

OCP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

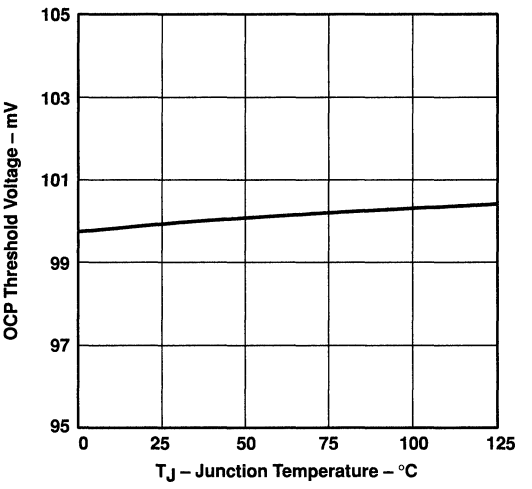


Figure 6

INHIBIT START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

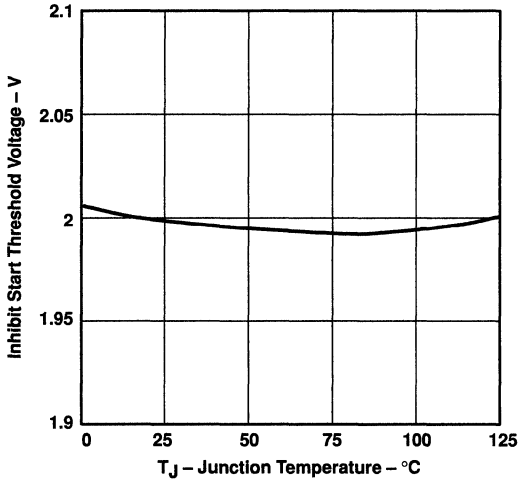


Figure 7

INHIBIT HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

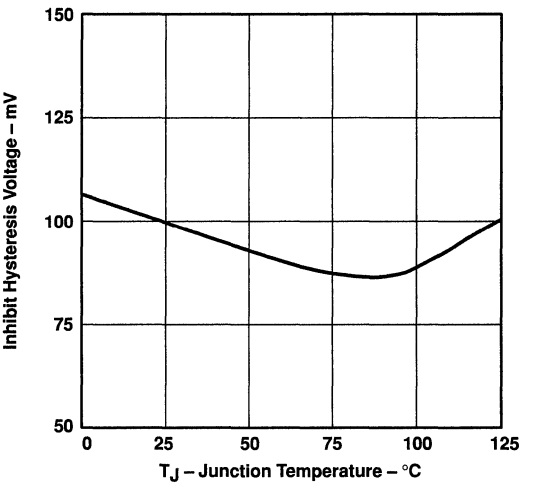


Figure 8

TYPICAL CHARACTERISTICS

UVLO START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

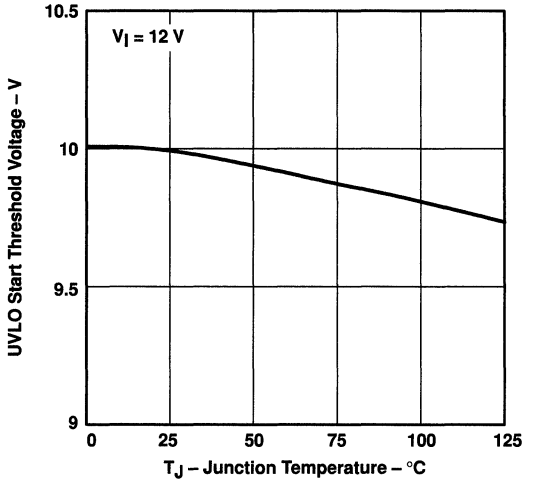


Figure 9

UVLO HYSTERESIS
vs
JUNCTION TEMPERATURE

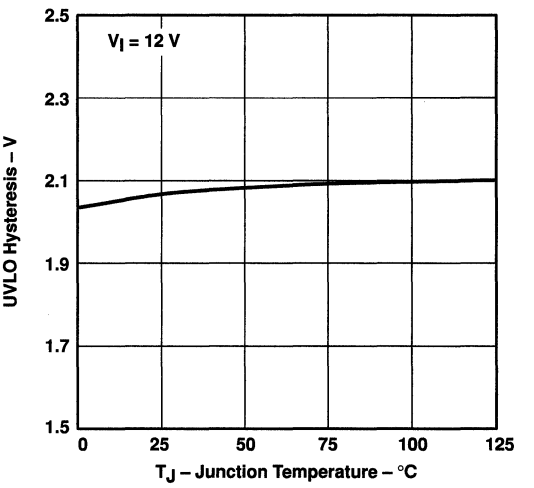


Figure 10

QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE

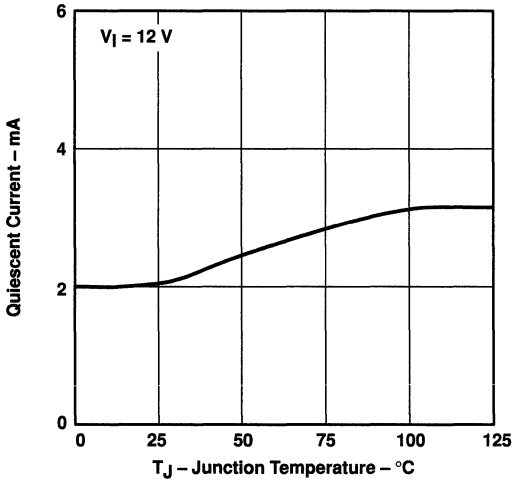


Figure 11

POWERGOOD THRESHOLD
vs
JUNCTION TEMPERATURE

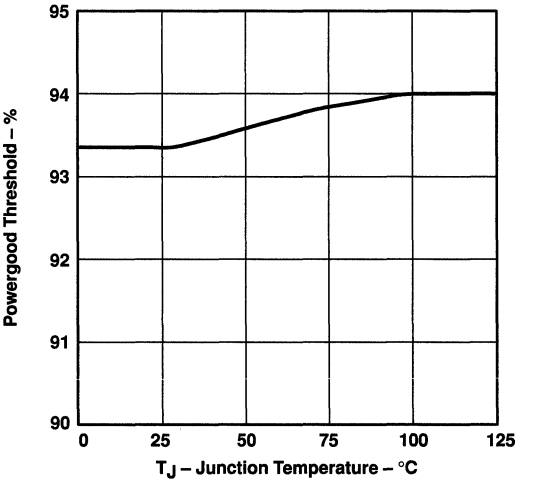


Figure 12

TYPICAL CHARACTERISTICS

SLOW START CHARGE CURRENT
vs
JUNCTION TEMPERATURE

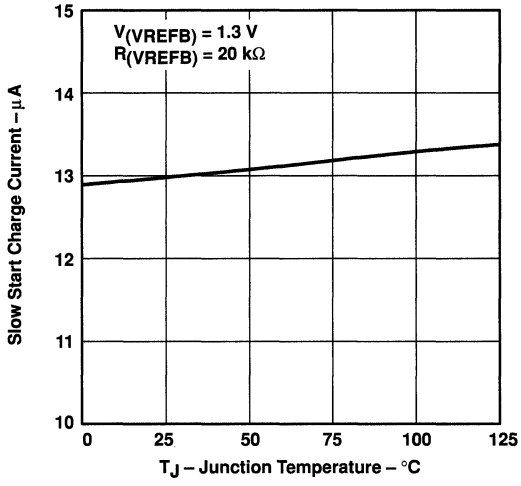


Figure 13

DRIVER
REGULATOR VOLTAGE
vs
JUNCTION TEMPERATURE

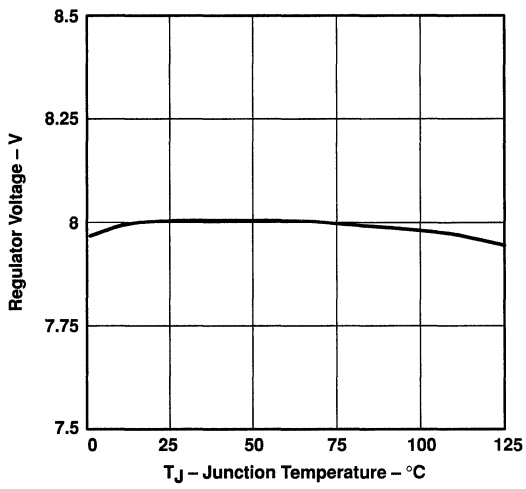


Figure 14

DRIVER
HIGH-SIDE OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

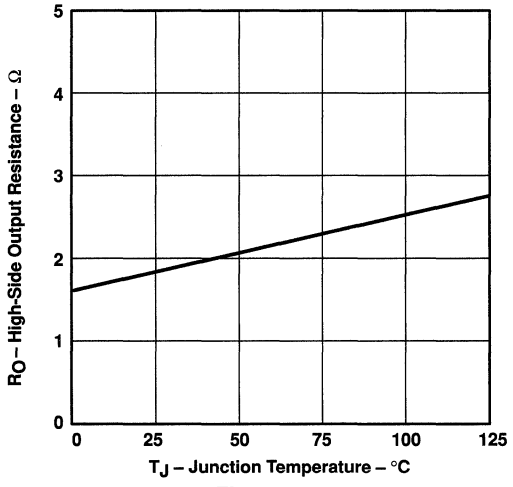


Figure 15

DRIVER
LOW-SIDE OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

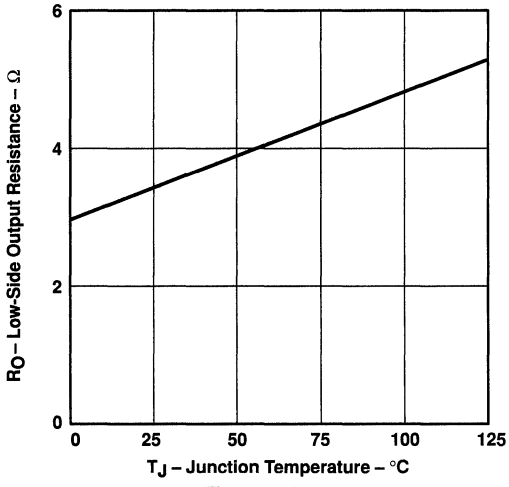


Figure 16

TYPICAL CHARACTERISTICS

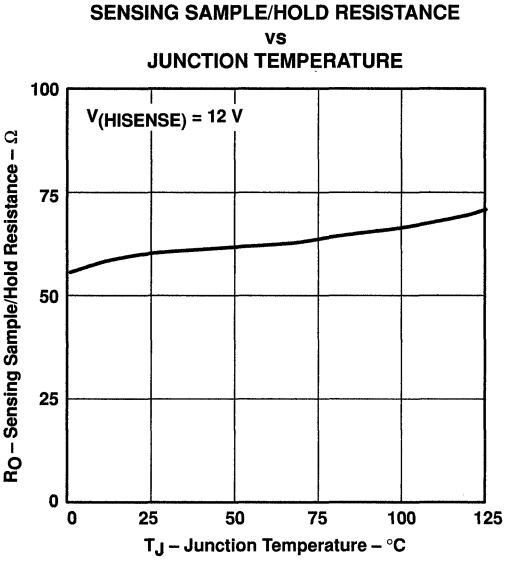


Figure 17

APPLICATION INFORMATION

The following figure is a typical application schematic. The circuit can be divided into the power-stage section and the control-circuit section. The power stage must be tailored to the input/output requirements of the application. The control circuit is basically the same for all applications with some minor tweaking of specific values. Table 2 shows the values of the power stage components for various output-current options.

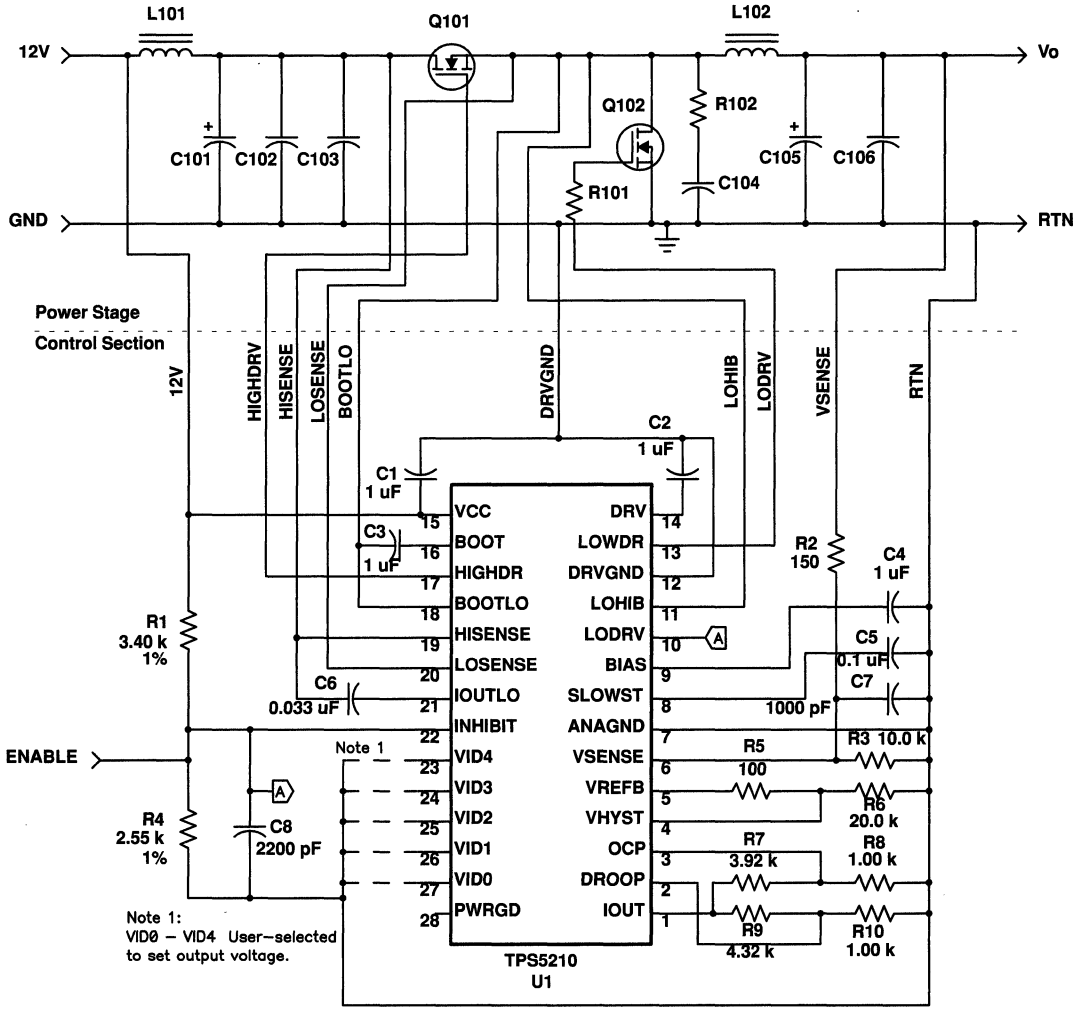


Figure 18. Standard Application Schematic

APPLICATION INFORMATION

Table 2. Power Stage Components

Ref Des	Function	12-V–Input Power Stage Components				
		4–A Out	8–A Out	12–A Out	20–A Out	40–A Out
C101	Input Bulk Capacitor	Sanyo, 16SV100M, 100–uF, 16–V, 20%	Sanyo, 16SA470M, 2 x 470–uF, 16–V, 20%	Sanyo, 16SA470M, 2 x 470–uF, 16–V, 20%	Sanyo, 16SA470M, 3 x 470–uF, 16–V, 20%	Sanyo, 16SA470M, 4 x 470–uF, 16–V, 20%
C102	Input Mid–Freq Capacitor	muRata, GRM42–6Y5V105Z025A 1.0–uF, 25–V, +80%–20%, Y5V	muRata, GRM42–6Y5V225Z016A 2.2–uF, 16–V, +80%–20%, Y5V	muRata, GRM42–6Y5V225Z016A 2.2–uF, 16–V, +80%–20%, Y5V	muRata, GRM42–6Y5V105Z025A 3 x 1.0–uF, 25–V, +80%–20%, Y5V	muRata, GRM42–6Y5V105Z025A 4 x 1.0–uF, 25–V, +80%–20%, Y5V
C103	Input Hi–Freq Bypass Capacitor	muRata, GRM39X7R104K016A 0.1–uF, 16–V, X7R	muRata, GRM39X7R104K016A, 0.1–uF, 16–V, X7R	muRata, GRM39X7R104K016A, 2 x 0.1–uF, 16–V, X7R	muRata, GRM39X7R104K016A, 3 x 0.1–uF, 16–V, X7R	muRata, GRM39X7R104K016A, 4 x 0.1–uF, 16–V, X7R
C104	Snubber Capacitor	muRata, GRM39X7R102K050A, 1000–pF, 50–V, X7R	muRata, GRM39X7R102K050A, 1000–pF, 50–V, X7R	muRata, GRM39X7R102K050A, 2 x 1000–pF, 50–V, X7R	muRata, GRM39X7R102K050A, 3 x 1000–pF, 50–V, X7R	muRata, GRM39X7R102K050A, 4 x 1000–pF, 50–V, X7R
C105	Output Bulk Capacitor	Sanyo, 6TPB150M, 3 x 150–uF, 6.3–V, 20%	Sanyo, 4SP820M, 820–uF, 4–V, 20%	Sanyo, 4SP820M, 2 x 820–uF, 4–V, 20%	Sanyo, 4SP820M, 3 x 820–uF, 4–V, 20%	Sanyo, 4SP820M, 4 x 820–uF, 4–V, 20%
C106	Output Hi–Freq Bypass Capacitor	muRata, GRM39X7R104K016A, 0.1–uF, 16–V, X7R	muRata, GRM39X7R104K016A, 0.1–uF, 16–V, X7R	muRata, GRM39X7R104K016A, 2 x 0.1–uF, 16–V, X7R	muRata, GRM39X7R104K016A, 3 x 0.1–uF, 16–V, X7R	muRata, GRM39X7R104K016A, 4 x 0.1–uF, 16–V, X7R
L101	Input Filter Inductor	CoilCraft, DO1608C–332, 3.3–uH, 2.0–A	Coiltronics, UP2B–2R2, 2.2–uH, 7.2–A	Coiltronics, UP2B–2R2, 2.2–uH, 7.2–A	Coiltronics, UP3B–1R0, 1–uH, 12.5–A	Coiltronics, UP3B–1R0, 1–uH, 12.5–A
L102	Output Filter Inductor	CoilCraft, DO3316P–332, 3.3–uH, 6.1–A	Coiltronics, UP3B–2R2, 2.2–uH, 9.2–A	Coiltronics, UP4B–1R5, 1.5–uH, 13.4–A	MicroMetals, T68–8/90 Core w/7T #16, 1.0–uH, 25–A	Pulse Engineering, P1605, 1.0–uH, 50–A
R101	Lo–Side Gate Resistor	3.3–Ohm, 1/16–W, 5%	3.3–Ohm, 1/16–W, 5%	2 x 3.3–Ohm, 1/16–W, 5%	3 x 3.3–Ohm, 1/16–W, 5%	4 x 3.3–Ohm, 1/16–W, 5%
R102	Snubber Resistor	2.7–Ohm, 1/10–W, 5%	2.7–Ohm, 1/10–W, 5%	2 x 2.7–Ohm, 1/10–W, 5%	3 x 2.7–Ohm, 1/10–W, 5%	4 x 2.7–Ohm, 1/10–W, 5%
Q101	Power Switch	Siliconix, Si4410, NMOS, 13–mOhm	Siliconix, Si4410, NMOS, 13–mOhm	Siliconix, 2 x Si4410, NMOS, 13–mOhm	Siliconix, 2 x Si4410, NMOS, 13–mOhm	IR, 2 x IRF7811, NMOS, 11–mOhm
Q102	Synchron-ous Switch	Siliconix, Si4410, NMOS, 13–mOhm	Siliconix, Si4410, NMOS, 13–mOhm	Siliconix, 2 x Si4410, NMOS, 13–mOhm	Siliconix, 3 x Si4410, NMOS, 13–mOhm	IR, 4 x IRF7811, NMOS, 11–mOhm
Nominal Frequency†		220 KHz	330 KHz	240 KHz	140 KHz	168 KHz
Hysteresis Window		20 mV	20 mV	20 mV	20 mV	10 mV

† Nominal frequency measured with Vo set to 2 V.

The values listed above are recommendations based on actual test circuits. Many variations of the above are possible based upon the desires and/or requirements of the user. Performance of the circuit is equally, if not more, dependent upon the layout than on the specific components, as long as the device parameters are not exceeded. Fast-response, low-noise circuits require critical attention to the layout details. Even though the operating frequencies of typical power supplies are relatively low compared to today's microprocessor circuits, the power levels and edge rates can cause severe problems both in the supply and the load. The power stage, having the highest current levels and greatest dv/dt rates, should be given the greatest attention.

APPLICATION INFORMATION

frequency calculation

A detailed derivation of frequency calculation is shown in the application report, "*Designing Fast Response Synchronous Buck Regulators Using the TPS5210*", TI Literature number SLVA044. When less accurate results are acceptable, the simplified equation shown below can be used:

$$f_s \cong \frac{\left(V_O \times \left[V_I - V_O\right] \times ESR\right)}{\left(V_I \times L \times \text{Hysteresis Window}\right)}$$

Control Section

Below are the equations needed to select the various components within the control section. Details and the derivations of the equations used in this section are available in the application report "*Designing Fast Response Synchronous Buck Regulators Using the TPS5210*", TI Literature number SLVA044.

output voltage selection

Of course the most important function of the power supply is to regulate the output voltage to a specific value. Values between 1.3 V and 3.5 V can be easily set by shorting the correct VID inputs to ground. Values above the maximum reference voltage (3.5 V) can be set by setting the reference voltage to any convenient voltage within its range and selecting values for R2 and R3 to give the correct output. Select R3:

R3 << than $V_{REF}/I_{BIAS(VSENSE)}$; a recommended value is 10 kΩ

Then, calculate R2 using:

$$V_O = V_{REF}\left(1 + \frac{R2}{R3}\right) \qquad \text{or} \qquad R2 = \frac{R3 \times \left(V_O - V_{REF}\right)}{V_{REF}}$$

R2 and R3 can also be used to make small adjusts to the output voltage within the reference-voltage range and/or to adjust for load-current active droop compensation. If there is no need to adjust the output voltage, R3 can be eliminated. R2, R3 (if used), and C7 are used as a noise filter; calculate using:

$$C7 = \frac{150\ ns}{(R2 \parallel R3)}$$

slowstart timing

Slowstart reduces the startup stresses on the power-stage components and reduces the input current surge. Slowstart timing is a function of the reference-voltage current (determined by R6) and is independent of the reference voltage. The first step in setting slowstart timing will be to determine R6:

R6 should be between 7 kΩ and 300 kΩ, a recommended value is 20 kΩ.

Set the slowstart timing using the formula:

$$C5 = \frac{t_{SS}}{\left(5 \times R_{VREFB}\right)} \cong \frac{t_{SS}}{(5 \times R6)}$$

Where C5 = Slowstart capacitance in μF
t_{SS} = Slowstart timing in μs
R_{VREFB} = Resistance from VREFB to GND in ohms (≈ R6)

APPLICATION INFORMATION

hysteresis voltage

A hysteretic controller regulates by self-oscillation, thus requiring a small ripple voltage on the output which the input comparator uses for sensing. Once selected, the TPS5210 hysteresis is proportional to the reference voltage; programming Vref to a new value automatically adjusts the hysteresis to be the same percentage of Vref. The actual output ripple voltage is the combination of the hysteresis voltage, overshoot caused by internal delays, and the output capacitor characteristics. Figure 20 shows the hysteresis window voltage (V_{HI} to V_{LO}) and the output voltage ripple (V_{MAX} to V_{MIN}). Since the output current from VREFB should be less than 500 µA, the total divider resistance (R5 + R6) should be greater than 7 KΩ. The hysteresis voltage should be no greater than 60 mV so R6 will dominate the divider.

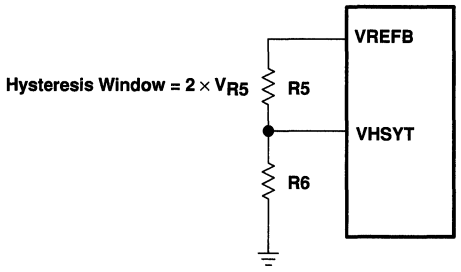


Figure 19. Hysteresis Divider Circuit

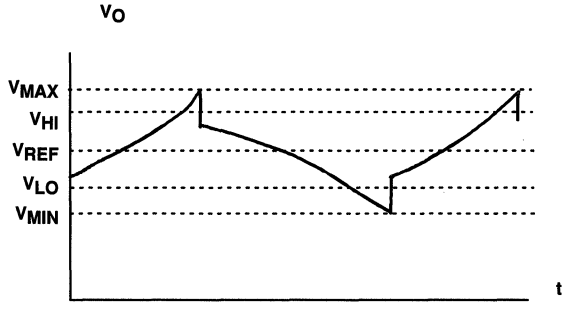


Figure 20. Output Ripple

The upper divider resistor, R5, is calculated using:

$$R5 = \frac{\textit{Hysteresis Window}}{(2 \times \textit{VREFB} - \textit{Hysteresis Window})} \times R6 \cong \frac{V_{HYST}\,(\%)}{(2 \times 100)} \times R6$$

Where Hysteresis Window = the desired peak-to-peak hysteresis voltage.
VREFB = selected reference voltage.
V_{HYST} (%) = [(Hysteresis Window)/VREFB] * 100 < $V_{O(Ripple)(P-P)}$ (%)

APPLICATION INFORMATION

current limit

Current limit can be implemented using the on-resistance of the upper FETs as the sensing elements. Select R8:

$$R8 << \frac{V_{OCP}}{I_{Bias(OCP)}} \leq \frac{0.1V}{(100 \times 100\,nA)} \leq 10\ k\Omega$$ (A recommended value is 1 kΩ)

The IOUT signal is used to drive the current limit and droop-circuit dividers. The voltage at IOUT at the output current trip point will be:

$$V_{IOUT(Trip)} = \frac{(2 \times R_{DS(ON)} \times TF)}{NumFETs} \times I_{O(Trip)}$$

Where NumFETS = Number of upper FETS in Parallel.
TF = $R_{DS(ON)}$ temperature correction factor.
$I_{O(Trip)}$ = Desired output current trip level (A).

Calculate R7 using:

$$R7 = \left(\frac{V_{IOUT(Trip)}}{0.1\ V} - 1 \right) \times R8$$

Note that since $R_{DS(ON)}$ of MOSFETs can vary from lot to lot and with temperature, tight current-limit control (less than 1.5 x I_O) using this method is not practical. If tight control is required, an external current-sense resistor in series with the drain of the upper FET can be used with HISENSE and LOSENSE connected across the resistor.

droop compensation

Droop compensation is used to reduce the output voltage range during load transients by increasing the output voltage setpoint toward the upper tolerance limit during light loads and decreasing the voltage setpoint toward the lower tolerance limit during heavy loads. This allows the output voltage to swing a greater amount and still remain within the tolerance window. The maximum droop voltage is set with R9 and R10. Select R10:

$$R10 << \frac{V_{DROOP(Min)}}{I_{Bias(DROOP,Max)}} \leq \frac{0.01V}{(100 \times 100\,nA)} \leq 1\ k\Omega$$ (Again, a value of 1 kΩ is recommended)

The voltage at IOUT during normal operation (0 to 100% load) will vary from 0 V up to:

$$V_{IOUT(Max)} = \frac{(2 \times R_{DS(ON)} \times TF)}{NumFETs} \times I_{O(Max)}$$

Where $I_{O(Max)}$ = Maximum output load current (A).

APPLICATION INFORMATION

droop compensation (continued)

Then, calculate R9:

$$R9 = \left(\frac{V_{IOUT(Max)}}{V_{DROOP}} - 1\right) \times R10$$

Where V_{DROOP} = Desired droop voltage

At full load, the output voltage will be:

$$V_O = V_{REF} \times \left(1 + \frac{R2}{R3}\right) - V_{DROOP}$$

using the TPS5210 when both 12 V and 5 V are available

When both 12 V and 5 V are available, several components can be removed from the basic schematic shown above. R1, R4, and C9 are no longer required if 5 V is brought in directly to INHIBIT and LODRV. However, if undervoltage lockout for the 5-V input is desired, R1 and R4 can be used to set the startup setpoint. The INHIBIT pin trip level is 2.1 V. Select R4:

$$R4 << \frac{V_{INH}}{I_{INH(Max)}} \leq \frac{2.1V}{(100 \times 100\,nA)} \leq 210\,k\Omega$$

Then, set the 5-V UVLO trip level with R1:

$$R1 = \frac{(5V_{Trip} - 2V)}{2V} \times R4$$

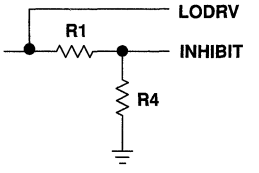


Figure 21. 5-V Input with UVLO

using the TPS5210 when only 5 V is available

The TPS5210 controller requires 12 V for internal control of the device. If an external source for 12 V is not available, a small on-board source must be included in the design. Total 12-V current is very small, typically about 20 mA, so even a small charge pump can be used to generate the supply voltage. The power stage is not voltage dependent, but component values must be selected for 5-V inputs and the frequency of operation is dependent upon the power stage input voltage.

APPLICATION INFORMATION

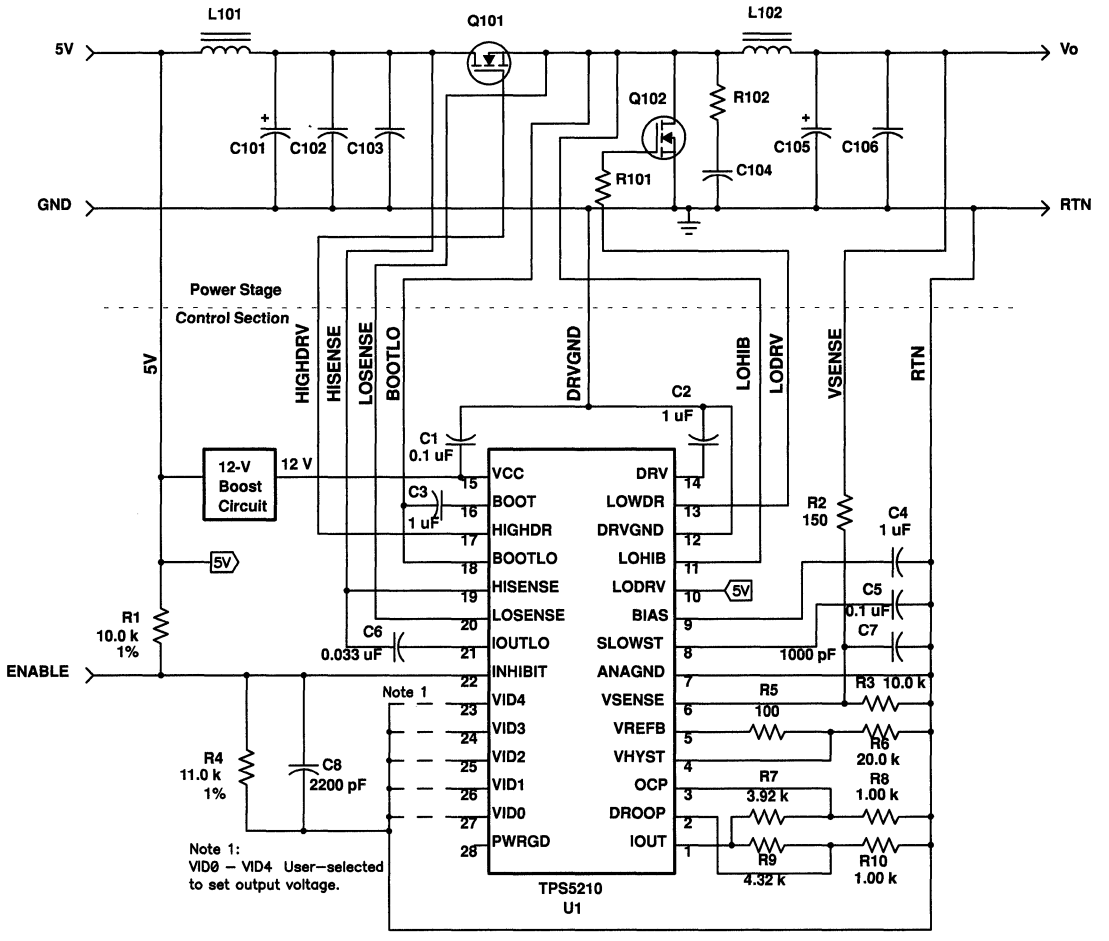


Figure 22. Typical 5-V-Only Application Circuit

application examples

Various application and layout examples using the TPS5210 are available from Texas Instruments. This information can be downloaded from *http://www.ti.com/sc/docs/products/msp/pwrsply/default.htm* or received from your TI representative.

APPLICATION INFORMATION

layout guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB design. The general design should proceed from the switching node to the output, then back to the driver section, and, finally, place the low-level components. Below are several specific points to consider *before* layout of a TPS5210 design begins.

1. All sensitive analog components should be referenced to ANAGND. These include components connected to SLOWST, DROOP, IOUT, OCP, VSENSE, VREFB, VHYST, BIAS, and LOHIB.
2. Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.
3. Connections from the drivers to the gate of the power FETs, should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
4. The bypass capacitor for the DRV regulator should be placed close to the TPS5210 and be connected to DRVGND.
5. The bypass capacitor for V_{CC} should be placed close to the TPS5210 and be connected to DRVGND.
6. When configuring the high-side driver as a floating driver, the connection from BOOTLO to the power FETs should be as short and as wide as possible. The other pins that also connect to the power FETs, LOHIB and LOSENSE, should have a separate connection to the FETS since BOOTLO will have large peak currents flowing through it.
7. When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from BOOT to BOOTLO) should be placed close to the TPS5210.
8. When configuring the high-side driver as a ground-referenced driver, BOOTLO should be connected to DRVGND.
9. The bulk storage capacitors across V_I should be placed close to the power FETS. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
10. High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
11. HISENSE and LOSENSE should be connected very close to the drain and source, respectively, of the high-side FET. HISENSE and LOSENSE should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed close to where HISENSE connects to Vin, to reduce high-frequency noise coupling on HISENSE.

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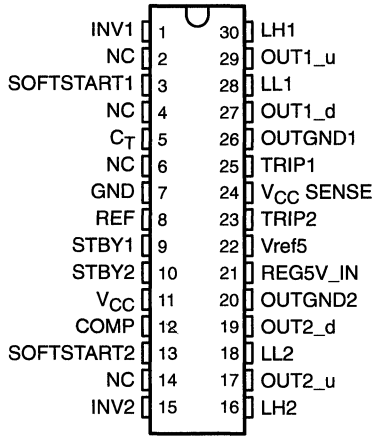
- **Independent Dual Channels**
- **Hysteretic Control for Fast Transient Response**
- **4.5-V to 25-V Input Voltage Range**
- **Adjustable Output Voltage Down to 1.2 V**
- **Synchronous Rectifier Enables Efficiencies of >95%**
- **Minimized External Component Count**
- **Separate Standby Control and Over Current Protection**
- **Low Supply Current . . . 0.8 mA Typ**
- **30-Pin TSSOP**
- **Low Standby Current (1-μA maximum)**
- **EVM Available (TPS5602EVM-121)**

DBT PACKAGE
(TOP VIEW)

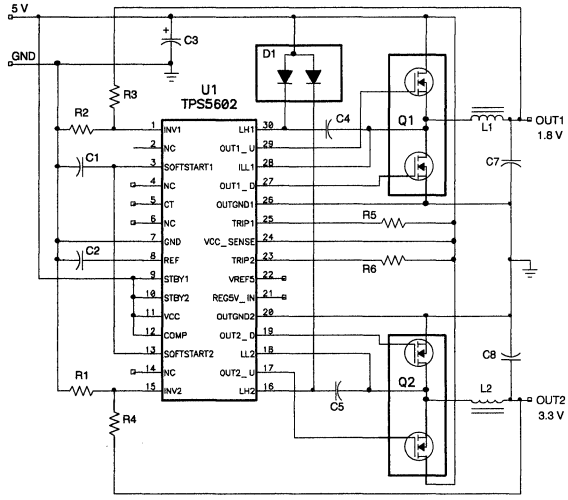


NC – No internal connection

description

The TPS5602 is a dual-channel synchronous buck switch-mode power supply controller featuring very fast feedback control and minimized component count. By using the hysteretic control method, it is ideal for high-transient current applications, such as 'C6000 and multiple 'C54x DSPs. The TPS5602 is designed specifically for DSP applications that require high efficiency. Since both channels are independent, the up and down power sequencing can be easily achieved by properly setting the standby pins. The wide input voltage and adjustable output voltage make the TPS5602 suitable for many applications.

typical design

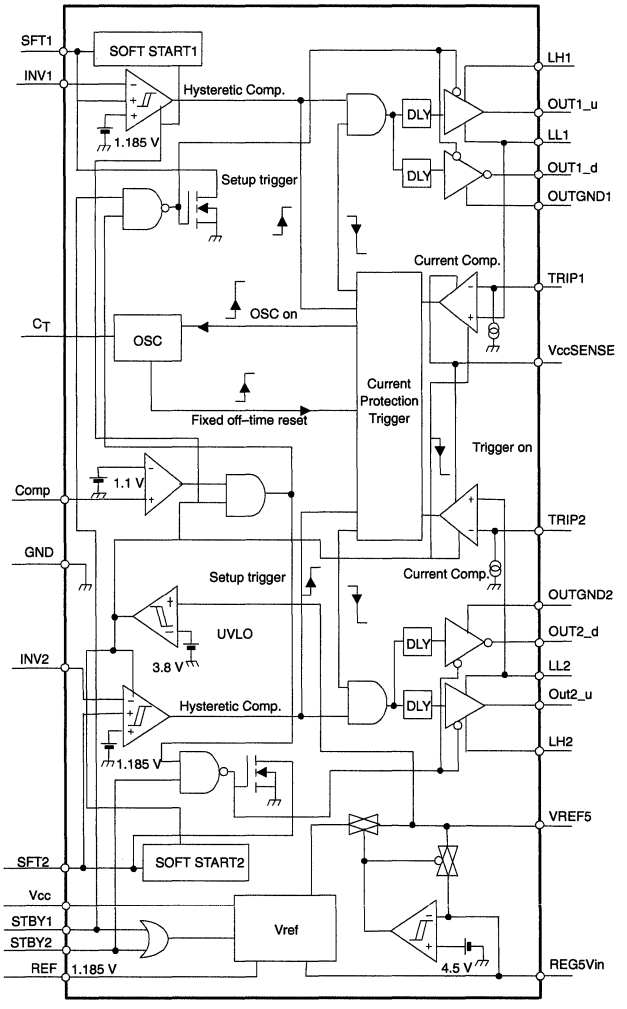


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGE	
	TSSOP (DBT)	EVM
–40°C to 85°C	TPS5602IDBT	TPS5602EVM-121
	TPS5602IDBTR	

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
COMP	12	I/O	Voltage monitor comparator input
C_T	5	I/O	The oscillator frequency external capacitor connection
GND	7		Control GND
INV1	1	I	CH1 hysteretic comparator inverting input
INV2	15	I	CH2 hysteretic comparator inverting input
LH1	30	I/O	CH2 high-side gate drive boost capacitor input
LH2	16	I/O	CH1 high-side gate drive boost capacitor input
LL1	28	I/O	CH1 high-side drive and current protection
LL2	18	I/O	CH2 high-side drive and current protection
NC	2, 4, 6, 14		
OUT1_d	27	I/O	CH1 low-side gate drive output
OUT2_d	19	O	CH2 low-side gate drive output
OUT1_u	29	O	CH1 high-side switch output
OUT2_u	17	O	CH2 high-side switch output
OUTGND1	26		Output GND 1
OUTGND2	20		Output GND 2
REF	8	O	1.185-V reference voltage output
REG5V_IN	21	I	External 5-V input
SOFTSTART1	3	I/O	CH1 soft start control external capacitor connection
SOFTSTART2	13	I/O	CH2 soft start control external capacitor connection
STBY1	9	I	CH1 standby control
STBY2	10	I	CH2 standby control
TRIP1	25	I	CH1 output current control input
TRIP2	23	I	CH2 output current control input
V_{CC}	11	I	Supply voltage input
Vref5	22	O	5-V internal regulator output
V_{CC}SENSE	24	I	Supply voltage sense input

detailed description

vref (1.185 V)

The reference voltage is used for the output voltage setting and the voltage protection (COMP).

vref (5 V)

An internal linear voltage regulator offers a fixed 5-V voltage as the bootstrap voltage so that the design for the bootstrap is much easier. The tolerance is 6%. The extra current capability can also be used to power external circuitry.

5-V switch

If the internal 5-V switch senses a 5-V input from REG5V pin, the internal 5-V linear regulator will be disconnected from the MOSFET drivers. The external 5-V will be used for the low-side driver and the high-side bootstrap, thus increasing the efficiency.

detailed description (continued)

hysteretic comparator

Each channel has a hysteretic comparator to regulate the output voltage of the synchronous-buck converter. The hysteresis is set internally and is typically 8.5 mV. The total delay from the comparator input to the driver output is typically 500 ns from low to high and 350 ns from high to low.

low-side driver

The low-side driver is designed to driver low-Rds(on) n-channel MOSFETs. The maximum drive voltage is 5 V from Vref5. The current rating of the driver is typically 1 A, source and sink.

high-side driver

The high side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 1 A, source and sink. When configured as a floating driver, the bias voltage to the driver is developed from the Vref5, limiting the maximum drive voltage between OUTxU and LLx to 5 V. The maximum voltage that can be applied between LHx and OUTGNDx is 30 V.

deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turnon time of the MOSFETs drivers. The typical deadtime from low-side-driver-off to high-side-driver-on is 75 ns and 164 ns from high-side-driver-off to low-side-driver-on.

current protection

The current protection is achieved by sensing the high-side power MOSFET drain-to-source voltage drop during on-time through V_{CC}Sense and LLx pins. An external resistor between Vin and TRIPx pin with the internal current source connected to the current comparator negative input adjusts the current limit. The typical internal current source current is 15 µA. When the voltage on the positive pin is lower than the negative pin, the current comparator turns on the trigger, and then activates the oscillator. This oscillator repeatedly resets the trigger until the overcurrent condition is removed. The equation for the external resistor selection is:

$$Rclmt = \frac{Rds(on) \times (Itrip + Iind(p\text{-}p)/2)}{0.000015}$$

Where Rds(on) is the MOSFET turnon resistance; Itrip is the required trip current; Iind(p-p) is the peak-to-peak inductor ripple current. Itrip must be greater than 0.5×Iind(p-p). The tolerance is ±30%.

COMP

COMP is an internal comparator used for any voltage protection such as the output under-voltage protection for DSP power applications. If the core voltage is lower than the setpoint, the comparator turns off both channels to prevent the DSP from damage.

SOFT1, SOFT2

Separate soft-start terminals make it possible to set the sequencing of each output for any possibility. The capacitor value for a start-up time can be calculated by the following equation:

$$C = 2 \times T \quad (\mu F)$$

Where C is the external capacitor value, T is the required start-up time in (ms).

STBY1, STBY2

Both channels can be switched into standby mode separately by grounding the STBY pin. The standby current is less than 1 µA. The STBY pins can be used for sequencing.

UVLO

When the input voltage rises to about 3.8 V, the IC is turned on, ready to function. When the input voltage falls below the turnon value, the IC is turned off. The typical hysteresis is 149 mV.

absolute maximum ratings over operating free-air temperature (see Note 1) (unless otherwise noted)†

Supply voltage, V_{CC} ..... –0.3 V to 27 V
Input voltage, V_I, INV ..... –0.3 V to 7 V
Softstart ..... –0.3 V to 7 V
COMP ..... –0.3 V to 6 V
REG5V_IN ..... –0.3 V to 6 V
STBY ..... –0.3 V to 15 V
TRIP ..... –0.3 V to 15 V
Maximum Driver current ..... 3 A
Output voltage, LLx ..... –0.3 V to 27 V
Output voltage, OUTx_u ..... –0.3 V to 32 V
Output voltage, OUTx_d ..... –0.3 V to 7 V
Power dissipation (T_A = 25°C) ..... See Dissipation Table
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating virtual junction temperature range, T_J ..... 125°C
Storage temperature range, T_{stg} ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER DISSIPATION	$T_A \geq$ 25°C DERATING FACTOR	T_A = 85°C POWER DISSIPATION
DBT	874 mW	6.993 mW/°C	454 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		25	V
Input voltage, V_I	INV1/2			6	V
	COMP			6	
	SOFTSTART1/2			6	
	REG5V_IN			5.5	
	STBY1/STBY2			12	
	TRIP1/2 V_{CC_SENCE}			25	
Operation junction temperature range, T_A		–40		85	°C

electrical characteristics over recommended T_A = –40°C to 85°C temperature range, V_{CC} = 7 V (unless otherwise noted)

reference voltage

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference voltage	T_A = 25°C,	I_{vref} = 50 µA	1.167	1.185	1.203	V
		V_I = 4.5 V to 25 V,	I = 1 µA to 1 mA	1.155		1.215	
$V_{I(Regin)}$	Line regulation	V_{CC} = 5.5 V to 25 V,	I = 50 µA		0.2	12	mV
$V_{I(Regl)}$	Load regulation	I = 1 µA to 1 mA,			0.5	10	mV

quiescent current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Operating current without switching	Both STBY >2.5 V, No switching V_I = 4.5 V to 25 V		0.8	1.5	mA
$I_{(CCS)}$	Stand-by current	Both STBY <0.5 V, V_I = 4.5 V to 25 V		1	1000	nA

hysteretic comparator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}†	Hysteresis window		5.5	8.5	11.5	mV
$V_{H(off)}$	Offset voltage			2		mV
$I_{H(bias)}$	Bias current			10		pA
$t_{(HLT)}$, $t_{(LHT)}$	Propagation delay from INV to OUTxU‡	TTL input signal		230		ns
$t_{(LH)}$		10 mV overdrive on hysteretic band signal		500	650	
$t_{(HI)}$				350	500	

† V_{hys} is assured by design.
‡ The delay time in the table includes the driver.

driver deadtime

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(DRVLH)}$	Low side to high side			90		ns
$t_{(DRVHL)}$	High side to low side			160		

standby

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_H	High-level input voltage	STBY1, STBY2	2.5			V
I_L	Low-level input voltage				0.5	V
Tturn-on	Propagation delay	Staby to driver output		7.2		µs
Tturn-off				4.8		

5 V regulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	I = 10 mA	4.7		5.3	V
$V_{I(Regin)}$	Load regulation	V_{CC} = 5.5 V to 25 V, I = 10 mA			20	mV
$V_{I(Regl)}$		I = 1 mA to 10 mA, V_{CC} = 5.5 V			40	
I_{OS}	Short-circuit output current	Vref = 0 V		80		mA

electrical characteristics over recommended free-air temperature range, V_{CC} = 7 V (unless otherwise noted) (continued)

5-V internal switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TLH}	Threshold voltage		4.2		4.9	V
V_{THL}			4.1		4.7	
Rson	On-time resistance			2.5	8	Ω
V_{hys}	Hysteresis		50		250	mV

current limit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal current source		10	15	20	μA
	Input offset voltage			2.5		mV

UVLO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TLH)}$	Threshold voltage		3.6		4.2	V
$V_{(THL)}$			3.5		4.1	
	Hysteresis		50		250	mV

driver output

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUT_u sink current	V_O = 3 V		0.5	1.2		A
OUT_u source current	V_O = 2 V		–1	–1.7		
OUT_d sink current	V_O = 3 V		0.5	1.2		A
OUT_d source current	V_O = 2 V		–1	–1.7		
Rise time	High side driver is GND referenced, Input: INV = 0 V – 3 V, t_r/t_f = 10 ns, Frequency = 200 kHz,	C_L = 2200 pF		25.6		ns
		C_L = 3300 pF		30.8		
Fall time	High side driver is GND referenced, Input: INV = 0 V – 3 V, t_r/t_f = 10 ns, Frequency = 200 kHz,	C_L = 2200 pF		23.2		ns
		C_L = 3300 pF		25.2		

Softstart

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(CTRL)}$	Softstart current		1.8	2.5	3	μA
	Maximum discharge current			0.92		mA

COMP†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Threshold voltage		1	1.1	1.25	V
Turn on	Propagation delay 50% duty cycle, No capacitor on COMP or OUT_u pin,	Frequency = 200 kHz		452		ns
Turn off				384		

† The delay time in the table includes the drivers.

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency without Ct			202.4		kHz
Frequency with Ct	Ct = 100 pF		67.5		kHz

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT (BOTH CHANNELS ON)
vs
SUPPLY VOLTAGE

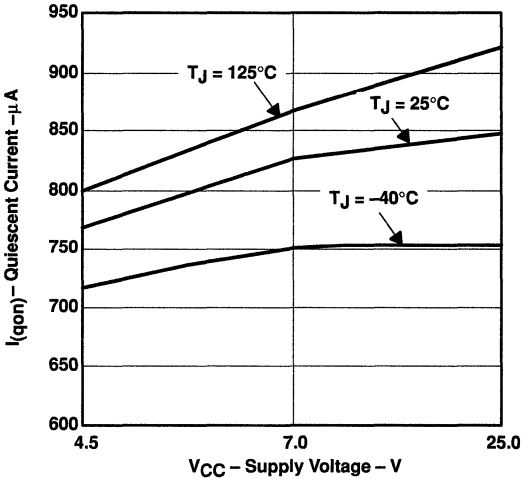


Figure 1

QUIESCENT CURRENT (BOTH CHANNEL STANDBY)
vs
SUPPLY VOLTAGE

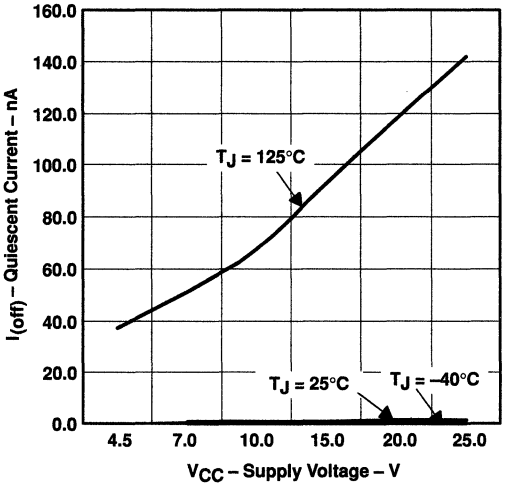


Figure 2

DRIVE OUTPUT VOLTAGE
vs
DRIVE CURRENT (SOURCE)

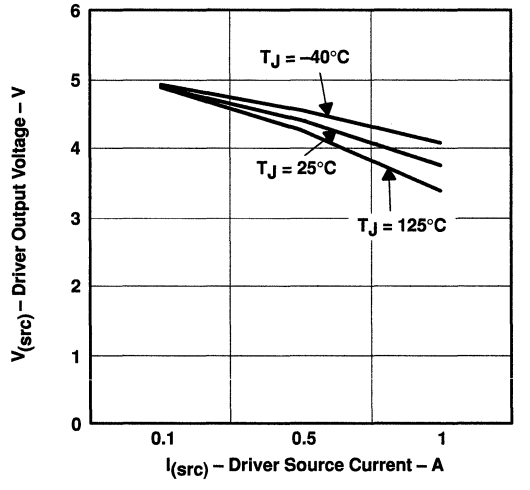


Figure 3

DRIVE VOLTAGE
vs
DRIVE CURRENT (SINK)

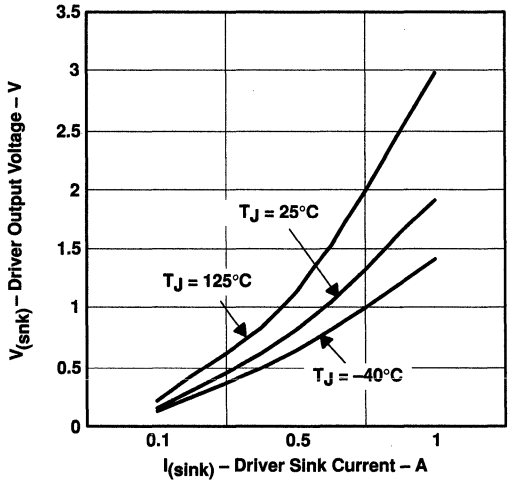


Figure 4

TYPICAL CHARACTERISTICS

SOFTSTART CAPACITANCE
vs
SOFTSTART TIMING

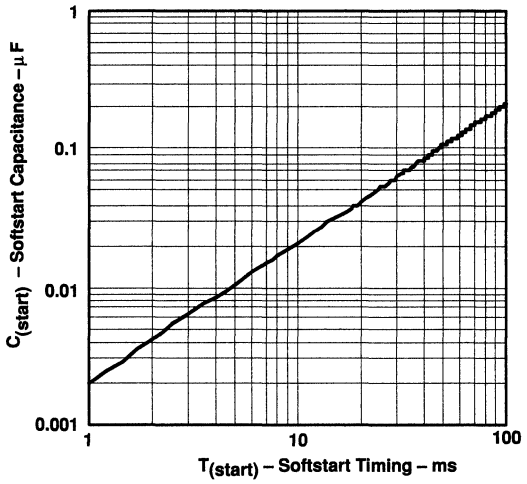


Figure 5

CURRENT-PROTECTION SOURCE CURRENT
vs
SUPPLY VOLTAGE

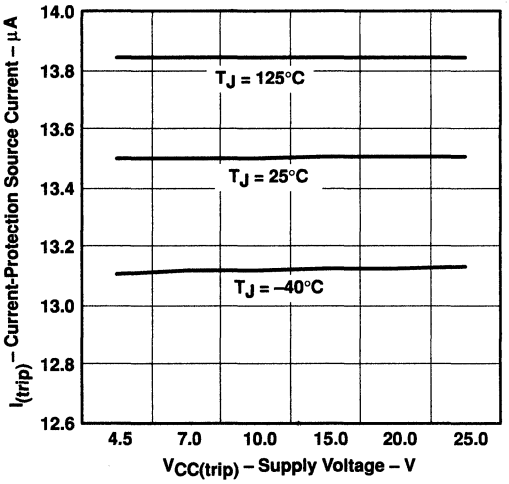


Figure 6

STANDBY THRESHOLD VOLTAGE (H–L)
vs
JUNCTION TEMPERATURE

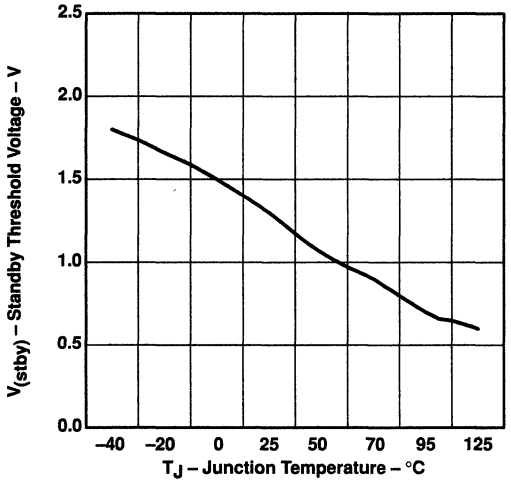


Figure 7

UVLO HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

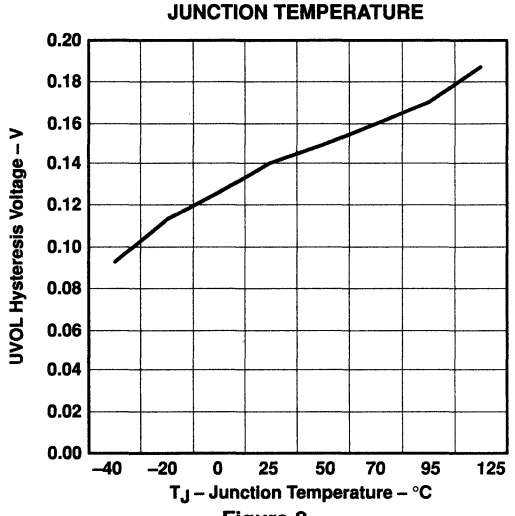


Figure 8

TYPICAL CHARACTERISTICS

UVLO THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

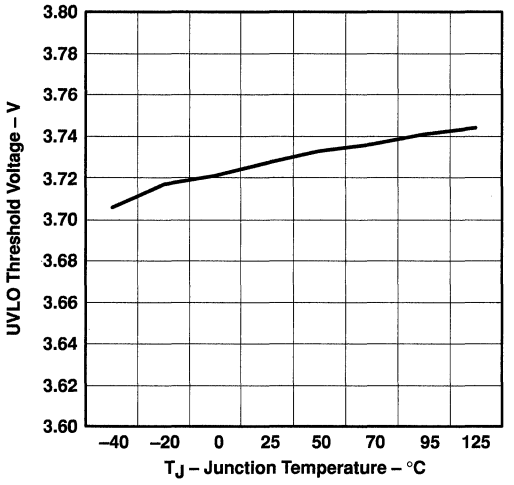


Figure 9

STANDBY THRESHOLD (L–H)
vs
JUNCTION TEMPERATURE

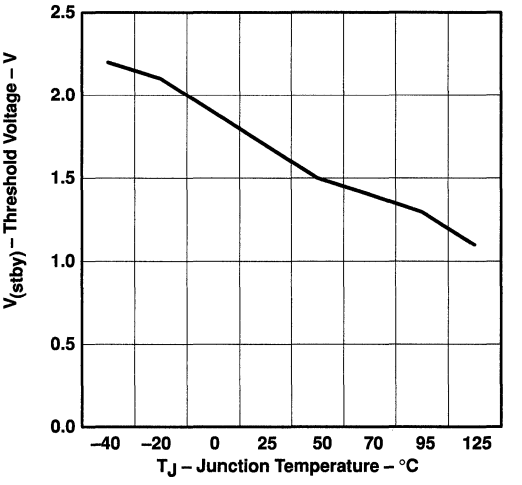


Figure 10

SOFT START CHARGE CURRENT
vs
JUNCTION TEMPERATURE

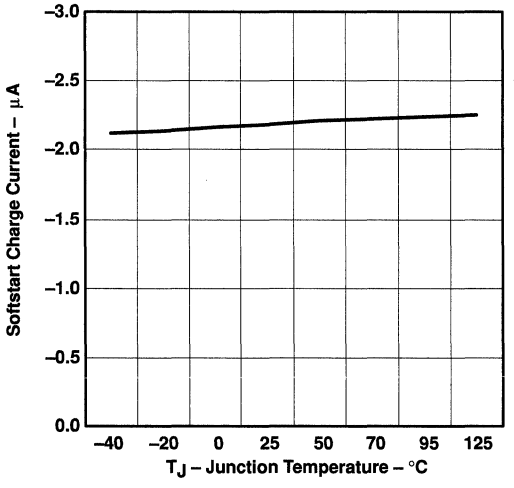


Figure 11

VREF5 VOLTAGE
vs
VREF5 CURRENT

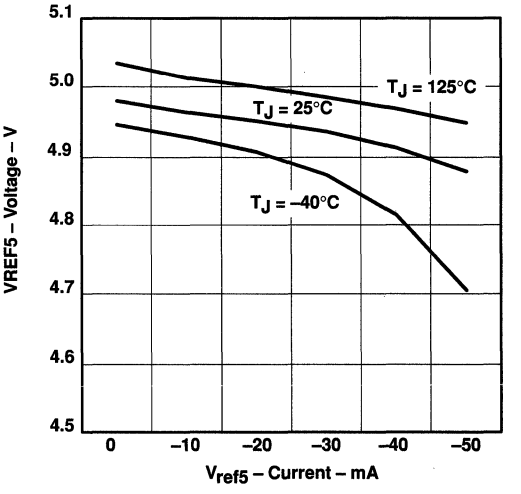


Figure 12

APPLICATION INFORMATION

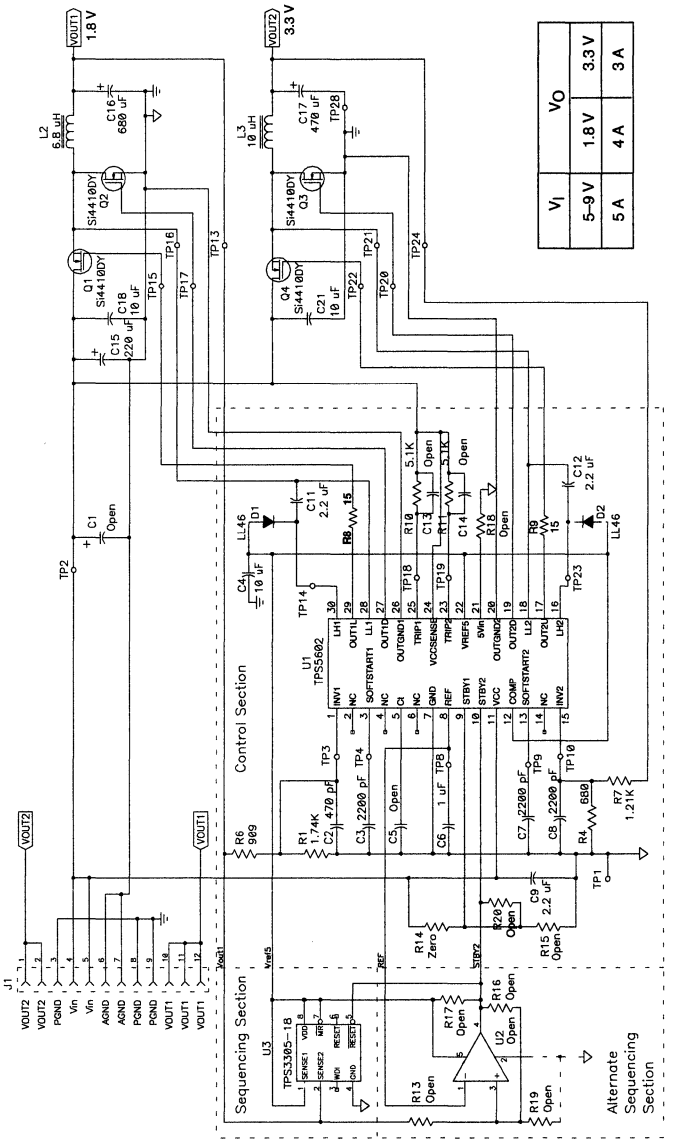


Figure 13. EVM Schematic Diagram

APPLICATION INFORMATION

application for DSP power

The design shown in this data sheet is a reference design for a DSP application. An evaluation module (EVM), TPS5602EVM-121 (SLVP121), is available for customer testing and evaluation. The intent is to allow a customer to fully evaluate the given design using the plug-in EVM supply shown here. The input voltage for this EVM is from 4.5 V to 9 V. The outputs are 1.8 V at 4 A and 3.3 V at 3 A. By changing few components this EVM can be used for different operating specifications such as high-input voltage.

This application provides the following power supply sequence: the core power goes up before the I/O supply, and if the core power is brought down by abnormal condition, the I/O power will be brought down with it.

To help the customers to design the power supply using the TPS5602, key design procedures are shown below:

switching frequency

With hysteretic control, the switching frequency is a function of the input voltage, the output voltage, the hysteresis window, the delay of the hysteresis comparator and the driver, the output inductance, the resistance in the output inductor, the output capacitance, the ESR and ESL in the output capacitor, the output current, and the turn on resistance of high side and low side MOSFET. It is a very complex equation if everything is included. To make it more useful to the designers, a simplified equation only considers the most influential factors. The tolerance of this equation is about 30%:

$$fs = \frac{Vout \times (Vin - Vout) \times \left(ESR - \left(10 \times 10^{-7} + Td\right)/Cout\right)}{Vin \times \left(Vin \times ESR \times \left(10 \times 10^{-7} + Td\right) + 0.007 \times Lout - ESL \times Vin\right)}$$

Where fs is the switching frequency (Hz); *Vout* is the output voltage (V); *Vin* is the input voltage (V); *Cout* is the output capacitance; *ESR* is the equivalent series resistance in the output capacitor (Ω); *ESL* is the equivalent series inductance in the output capacitor (H); *Lout* is the output inductance (H); and *Td* is the output feedback filter time constant (S).

Example: Vin = 5 V, Vout = 1.8 V, Cout = 680 µF: ESR = 40 mΩ; ESL = 3 nH; Lout = 6 µH; Td = 0.5 µs

Then, the frequency *fs = 122 kHz*.

output inductor ripple current

The output inductor current ripple can affect not only the efficiency and the inductor saturation, but also the output capacitor selection. The equation is exhibited below:

$$Iripple = \frac{Vin - Vout - Iout \times \left(Rdson + R_L\right)}{Lout} \times D \times Ts$$

Where *Iripple* is the peak-to-peak ripple current through the inductor (A); Vin is the input voltage (V); Vout is the output voltage (V); Iout is the output current; Rdson is the on-time resistance of MOSFET (Ω); D is the duty cycle; and Ts is the switching cycle (S). From the equation, it can be seen that the current ripple can be adjusted by changing the output inductor value.

Example: Vin = 5 V, Vout = 1.8 V, Iout = 5 A: Rdson = 10 mΩ; RL = 5 mΩ; D = 0.36; Ts = 10 mS; Lout = 6 µH

Then, the ripple current Iripple = 2 A.

APPLICATION INFORMATION

application for DSP power (continued)

output capacitor RMS current

Assuming the inductor ripple current totally goes through the output capacitor to ground, the RMS current in the output capacitor can be calculated as:

$$Io(rms) = \frac{\Delta I}{\sqrt{12}}$$

Where *Io(rms)* is the maximum RMS current in the output capacitor (A); ΔI is the peak–to–peak inductor ripple current (A).

Example: $\Delta I = 2\ A$, so $Io(rms) = 0.58\ A$

input capacitor RMS current

Assuming the input ripple current totally goes into the input capacitor to the power ground, the RMS current in the input capacitor can be calculated as:

$$Ii(rms) = Io \times \left(D \times \sqrt{(1 - D)} + (1 - D) \times \sqrt{D}\right)$$

Where *Ii(rms)* is the input RMS current in the input capacitor (A); *Io* is the output current (A); D is the duty cycle. From the equation, it can be seen that the highest input RMS current usually occurs at lowest input voltage.

Example: $Io = 5\ A;\ D = 0.36$
Then, Ii(rms) = 3.36 A

softstart

The softstart timing can be adjusted by selecting the softstart capacitor value. The equation is

$$C_{soft} = 2 \times T_{soft}$$

Where C_{soft} is the softstart capacitance (μF); T_{soft} is the start-up time pin (S).

Example: $Tsoft = 5\ ms$, so $Csoft = 0.01\ \mu F$.

current protection

The current protection in TPS5602 is set using an internal current source and an external resistor to set up the current limit. The sensed high side MOSFET drain-to-source voltage drop is compared to the set point; if the voltage drop exceeds the limit, the internal oscillator is activated, and continuously resets the current limit until the over-current condition is removed. The equation below should be used for calculating the external resistor value for current protection:

$$Rclmt = \frac{Rds(on) \times (Itrip + Iind(p\text{-}p)/2)}{0.000015}$$

Where Rclmt is the external current limit resistor (R10, R11); Rds(on) is the high side MOSFET on resistance; Itrip is the required current limit; Iind(p-p) is the peak-to-peak output inductor current.

Example: Rds(on) = $10\ m\Omega$, $Itrip = 5\ A$, $Lind = 2\ A$, so $Rclmt = 4\ k\Omega$.

APPLICATION INFORMATION

application for DSP power (continued)

sequencing and under voltage protection

The EVM design uses the standby pins to implement power sequencing. There are two ways to achieve the protection: one uses a voltage supervisory circuit such as the TI TPS3305-18, the other uses a low cost comparator, such as the TI TLV1391. The standby pin for the second channel is pulled low by either the supervisory circuit or the external protection comparator until the first channel output voltage is above the start-up threshold voltage. With the protection hysteresis, during the power down, if the core voltage is lower than, for example, 1.3 V, the 3.3 output will be pulled down together. During the normal operation, if the core voltage is lost, the I/O voltage will be pulled down at the same time. This protection circuit prevents the DSPs from any damage caused by the malfunctioning power supply. The equation displayed below uses the comparator for the protection setpoint:

Assuming R16 is much larger than R17, and R19 is 10 kΩ, and the R13 value is adjusted for the turnon setpoint:

$$R13 = \frac{(Von - 1.2) \times (R16 \parallel R19)}{1.2}$$

Where *Von* is the required turn on setpoint. For the turn-off setpoint, R16 is adjusted,

$$R16 = \frac{R13 \times R19 \times (1.2 - Vin)}{R19 \times (Voff - 1.2) - 1.2 \times R13}$$

By solving these equations together, or using a spreadsheet to iterate, the setpoints can be easily derived. The two equations are used for the verification:

$$Von = \frac{1.2 \times (R13 + (R16 \parallel R19)}{(R16 \parallel R19)} \quad \text{and} \quad Voff = R13 \times \left(\frac{1.2 - Vin}{R16} + \frac{1.2}{R19} + \frac{1.2}{R13}\right)$$

Where *Von* and *Voff* are the turnon and turnoff setpoints respectively

Example can be found by using the numbers in the bill of materials.

layout considerations

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, placing the low-level components. Below are several specific points to consider *before* layout of a TPS5602 design begins.

- All sensitive analog components should be referenced to ANAGND. These include components connected to Vref5, Vref, INV, LH, and COMP.
- Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.
- Connections from the drivers to the gate of the power FETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
- The bypass capacitor for V_{CC} should be placed close to the TPS5602.

APPLICATION INFORMATION

layout considerations (continued)

- When configuring the high-side driver as a floating driver, the connection from LL to the power FETs should be as short and as wide as possible.
- When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from LH to LL) should be placed close to the TPS5602.
- When configuring the high-side driver as a ground-referenced driver, LL should be connected to DRVGND.
- The bulk storage capacitors across V_{IN} should be placed close to the power FETs. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
- High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
- LH and LL should be connected very close to the drain and source, respectively, of the high-side FET. LH and LL should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed close to where HISENSE connects to V_{IN}, to reduce high-frequency noise coupling on HISENSE.
- The output voltage sensing trace should be isolated from the switching node and/or inductor pulses by the use of a ground trace or plane.

test results

The tests are conducted at T_A = 25°C, the input voltage is 5 V (if not specifically noted).

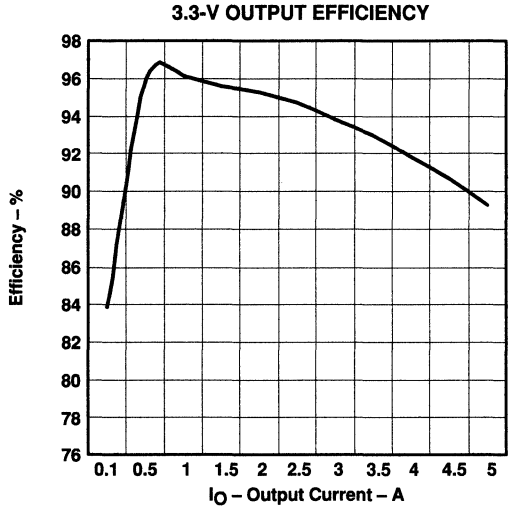


Figure 14

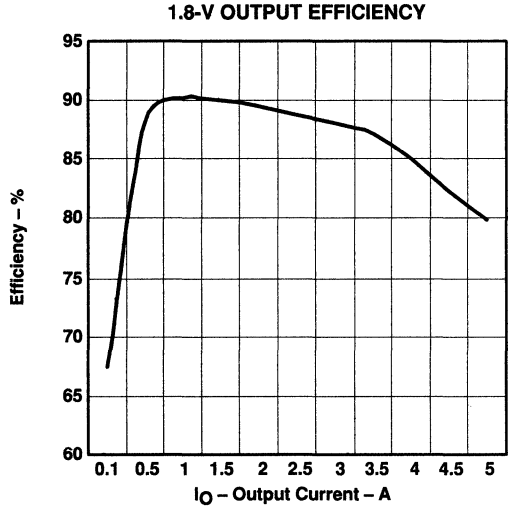


Figure 15

APPLICATION INFORMATION

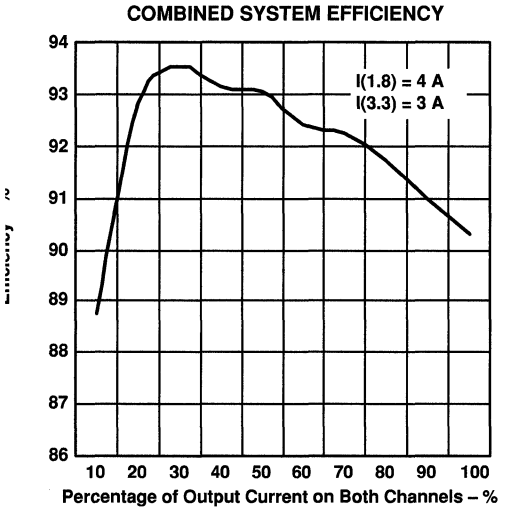


Figure 16

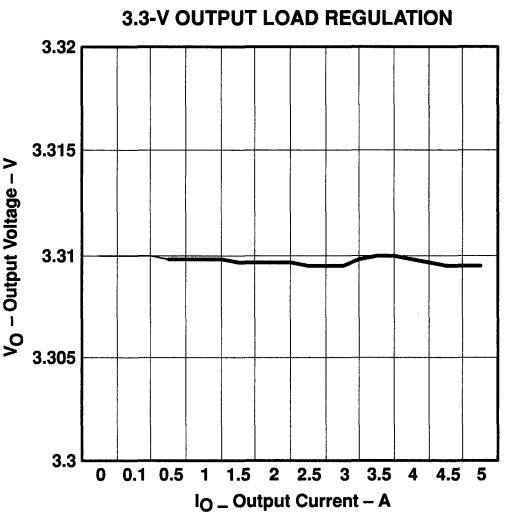


Figure 17

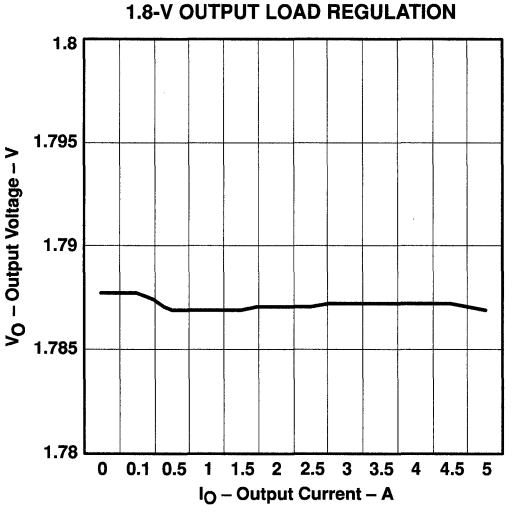


Figure 18

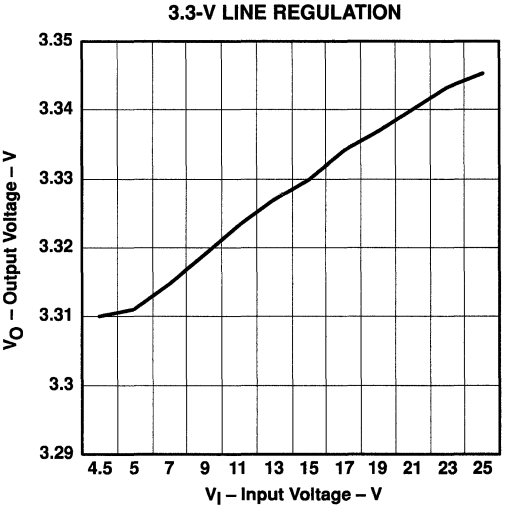


Figure 19

APPLICATION INFORMATION

1.8-V OUTPUT LINE REGULATION

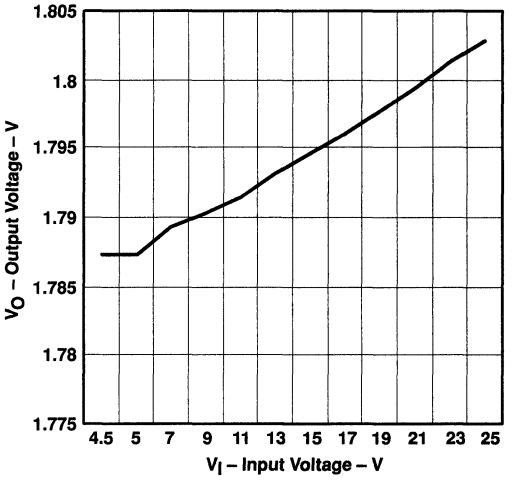


Figure 20

OUTPUT VOLTAGE RIPPLE

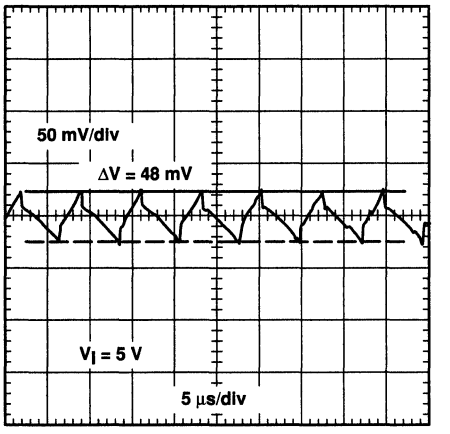


Figure 21

POWER-UP SEQUENCING

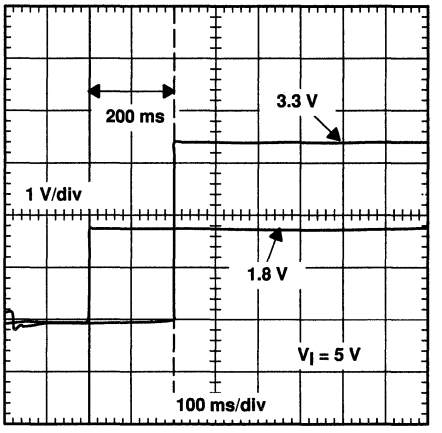


Figure 22

POWER-DOWN SEQUENCING

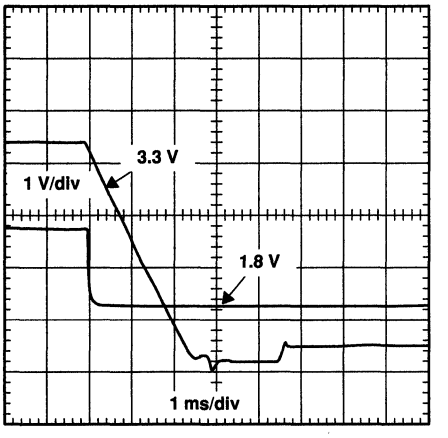


Figure 23

APPLICATION INFORMATION

TRANSIENT RESPONSE (OVERSHOOT)

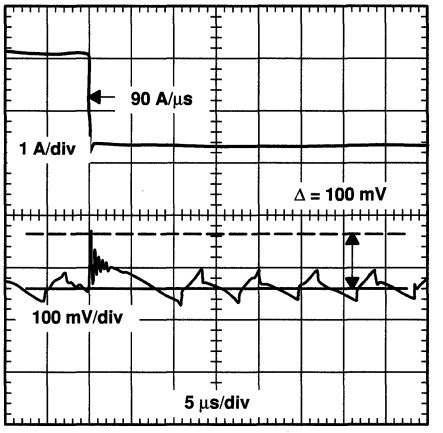


Figure 24

TRANSIENT RESPONSE (UNDERSHOOT)

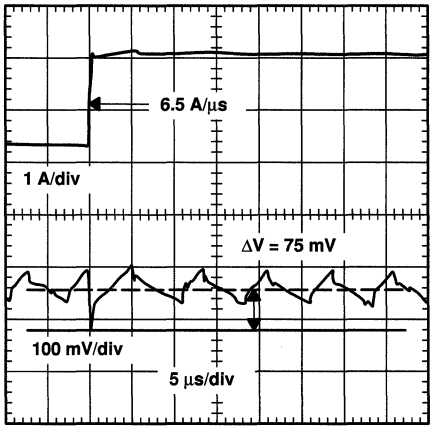


Figure 25

APPLICATION INFORMATION

Table 1. SLVP121 Bill of Materials

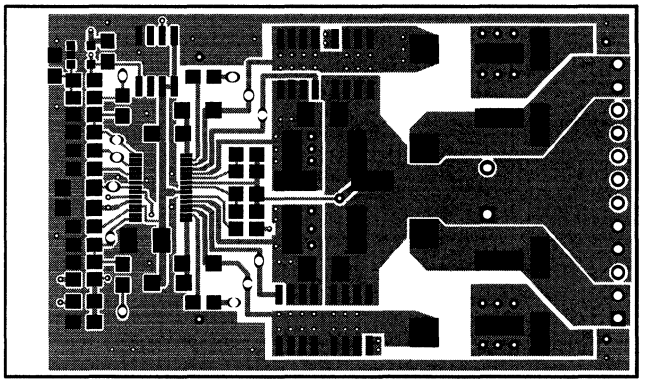
REF.	PART NUMBER	MFR.	DESCRIPTION	SIZE
C1†			Open	
C2	Std		Capacitor, ceramic, 470 pF,16 V, X7R, 20%	805
C3	Std		Capacitor, ceramic, 2200 pF,16 V, X7R, 20%	805
C4	GRM235Y5V106Z016A	muRata	Capacitor, ceramic, 10 µF, 16 V, Y5V	1210
C5†			Open	805
C6	Std		Capacitor, ceramic, 1 µF, 16 V, X7R, 20%	1206
C7	Std		Capacitor, ceramic, 2200 pF, 16 V, X7R, 20%	805
C8	Std		Capacitor, ceramic, 2200 pF, 16 V, X7R, 20%	805
C9	GRK316F225ZG	Taiyo Yuden	Capacitor, ceramic, 2.2 µF, 35 V, X7R, 20%	1206
C11	GRK316F225ZG	Taiyo Yuden	Capacitor, ceramic, 2.2 µF, 35 V, X7R, 20%	1206
C12	GRK316F225ZG	Taiyo Yuden	Capacitor, ceramic, 2.2 µF, 35 V, X7R, 20%	1206
C13†	Std		Open	805
C14†	Std		Open	805
C15	10TPB220M	SANYO	Capacitor, electrolytic, 220 µF, 10 V, 20%	10×10 mm
C16	2R5TPB680M	SANYO	Capacitor, POSCAP, 680 µF, 2.5 V, 20%	7.3×4.3 mm
C17	4TPB470M	SANYO	Capacitor, POSCAP, 470 µF, 4 V, 20%	7.3×4.3 mm
C18	GMK325F106ZH	Taiyo Yuden	Capacitor, ceramic, 10 µF, 35 V	1210
C21	GMK325F106ZH	Taiyo Yuden	Capacitor, ceramic, 10 µF, 35 V	1210
D1	SD103-AWDICT-ND	Digikey	Diode, Schottky, 40 mA, 200 mA, 400 mW	3.5×1.5 mm
D2	SD103-AWDICT-ND	Digikey	Diode, Schottky, 40 mA, 200 mA, 400 mW	3.5×1.5 mm
J1	S1132-12-ND	Sullins	Header, right angle, 12-pin, 0.1 ctrs, 0.3" pins	Digikey, S1132–12–ND
L2	DO3316P-682	Coilcraft	Inductor, 6.8 µH, 4.4 A	0.5x0.37 in
L3	DO3316P-103	Coilcraft	Inductor 10 µH, 3.9 A	0.5x0.37 in
Q1–Q4	Si441DY Rev. A	Siliconix	MOSFET, N-Ch, 30 V, 10-A, 0.013 Ω	SO–8
R1	Std		Resistor, SMD, MF, 1.74 kΩ, 1/8W, 1%	805
R4	Std		Resistor, SMD, MF, 680 Ω, 1/8W, 1%	805
R6	Std		Resistor, SMD, MF, 910 Ω, 1/8W, 1%	805
R7	Std		Resistor, SMD, MF, 1.21 kΩ, 1/8W, 1%	805
R8	Std		Resistor, SMD, MF, 15 Ω, 1/8W, 5%	805
R9	Std		Resistor, SMD, MF, 15 Ω, 1/8W, 5%	805
R10	Std		Resistor, SMD, MF, 5.1 kΩ, 1/8W, 5%	805
R11	Std		Resistor, SMD, MF, 5.1 kΩ, 1/8W, 5%	805
R13†	Std		Open, resistor, SMD, MF, 3.3 kΩ, 1/8W, 5%	805
R14	Std		Open, resistor, SMD, MF, kΩ, 1/8W, 5%	805
R15†	Std		Open, resistor, SMD, MF, 1 kΩ, 1/8W, 5%	805
R16†	Std		Open, resistor, SMD, MF, 200 kΩ, 1/8W, 5%	805
R17†	Std		Open, resistor, SMD, MF, 10 kΩ, 1/8W, 5%	805
R18†	Std		Open, resistor, SMD, MF, 1 kΩ, 1/8W, 5%	805
R19†	Std		Open, resistor, SMD, MF, 10 kΩ, 1/8W, 5%	805
R20†	Std		Open, resistor, SMD, MF, 0 kΩ	805
U1	TPS5602DBT	TI	Dual channel controller	TSSOP 30-pin
U2†	TLV1391	TI	Open, single Comparator	SOT-23
U3	TPS3305-18D	TI	Supervisor	D

NOTE: This table is for 5–9 V input voltage and 3.3 V/1.8 V only.
† Any components with † are for optional test purpose only.

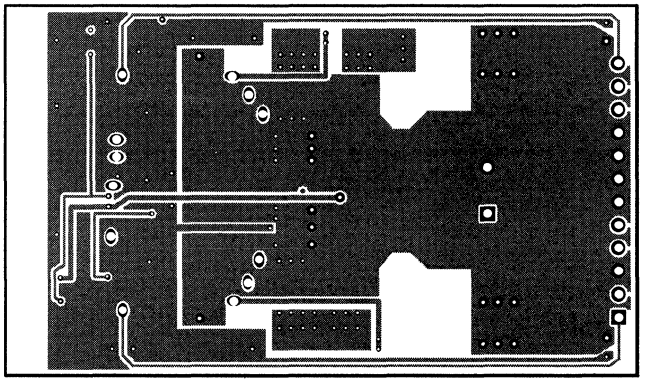
APPLICATION INFORMATION

To change the EVM operating specifications, several suggestions are shown in the following table.

HIGH INPUT VOLTAGE (TO 25 V)	2.5 V OUTPUT VOLTAGE	LOW-COST POWER SEQUENCING	COMPONENT SECOND SOURCE	
	Change R1 to 1 kΩ	Remove U3	Q1–4	IR7811 for higher efficiency
Add R15 (1 kΩ)	Change Rt to 1.2 kΩ	Add U2		
Change C15 to ELNA RV-35V221MH10-R (35 V, 220 µF)	Change U3 to TPS3305-25D	Add R13, R16, R17, R19		

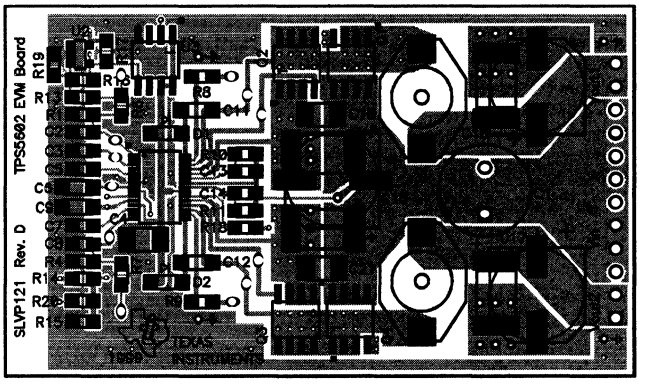


TOP SIDE



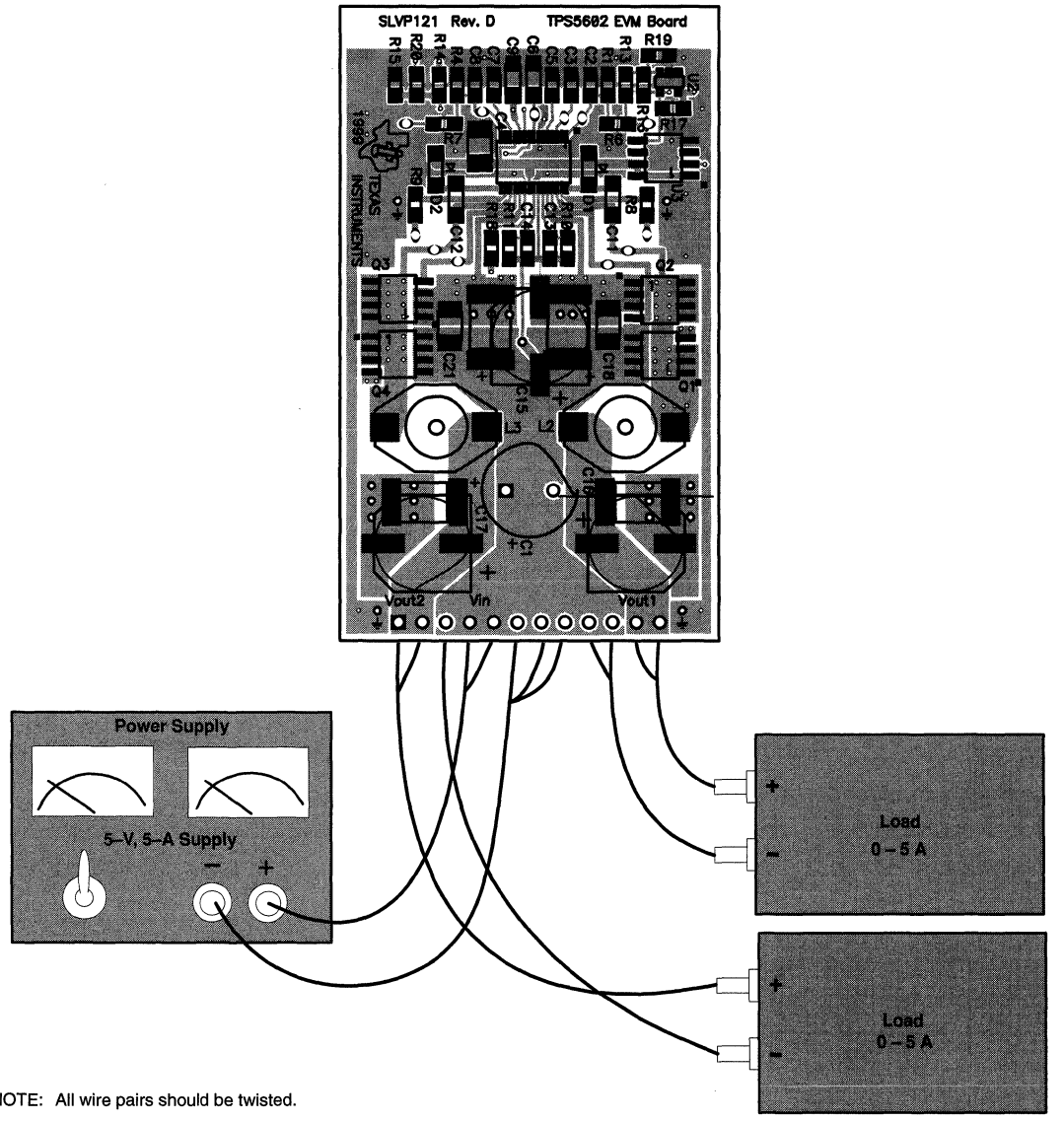
BOTTOM SIDE

APPLICATION INFORMATION



BOARD ASSEMBLY

APPLICATION INFORMATION

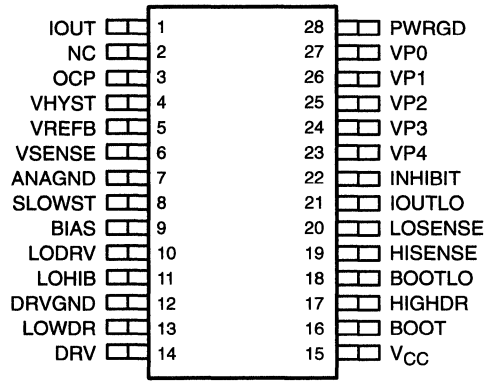


NOTE: All wire pairs should be twisted.

Figure 26. Test Setup

- **Single-Channel, 5-V Controller**
- **Synchronous-Rectifier Drivers for Greater Than 90% Efficiency**
- **Useable for All Common DSP Supply Voltages – Popular Output Voltage Options Set With Program Pins**
- **EVM Available**
- **Ideal for Applications With Current Ranges From 3 A to 30 A.**
- **Hysteretic Control Technique Enables Fast Transient Response — Ideal for 'C6000 or Multiple 'C5000 Applications**
- **Low Supply Current**
  - **3 mA in Operation**
  - **90 μA in Standby**
- **Power Good Output**
- **28-Pin TSSOP PowerPAD™ Package**

PWP PACKAGE
(TOP VIEW)

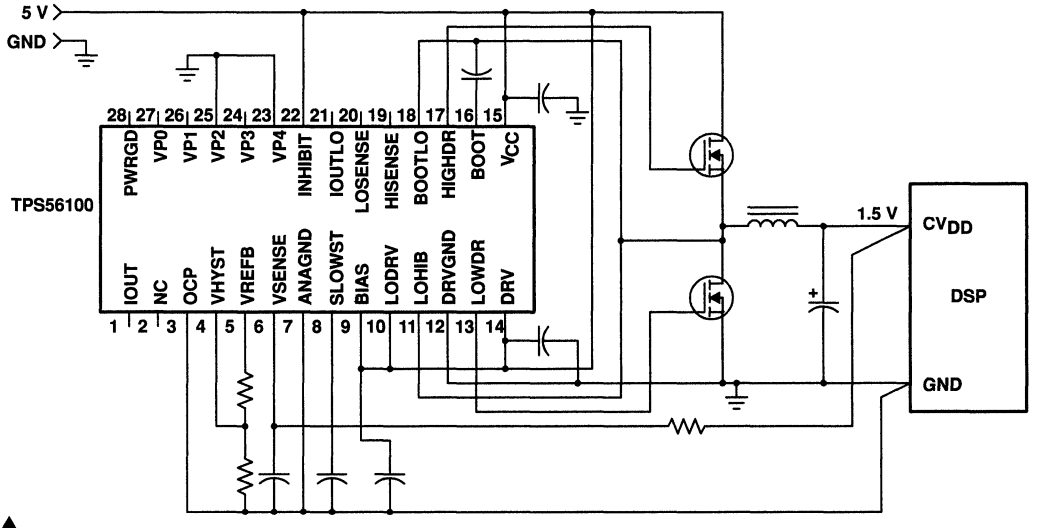


NC – Not Connected

description

The TPS56100 is a high-efficiency synchronous-buck regulator controller which provides an accurate programmable supply voltage to low-voltage digital signal processors, such as the 'C6x and 'C54x DSPs. An internal 5-bit DAC is used to program the reference voltage from 1.3 V to 2.6 V. Higher output voltages can be implemented using an external input resistive divider. The TPS56100 uses a fast hysteretic control method that provides a quick transient response. The propagation delay from the comparator input to the output driver is

application example



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PowerPAD is a trademark of Texas Instruments Incorporated.

description (continued)

less than 300 ns, even at maximum output current. Overcurrent shutdown and crossover protection combine to eliminate destructive faults in the output MOSFETs, thereby protecting the processor during operation. The slowstart current source is proportional to the reference voltage, thereby eliminating variation of the slowstart timing when changes are made to the output voltage. When the output drops to less than 93% of the nominal output voltage, PWRGD will pull the open-drain output low. The overvoltage circuit will disable the output drivers if the output voltage rises more than 15% above the nominal output voltage. The TPS56100 also includes an inhibit input to control power sequencing and undervoltage lockout thereby insuring the 5-V supply is within limits before the controller starts. The 2-A MOSFET drivers can power multiple MOSFETs in parallel to drive single or multiple DSPs and load currents up to 30 A. The high-side driver can be configured as a ground-referenced driver or as a floating bootstrap driver with the included internal bootstrap Schottky diode.

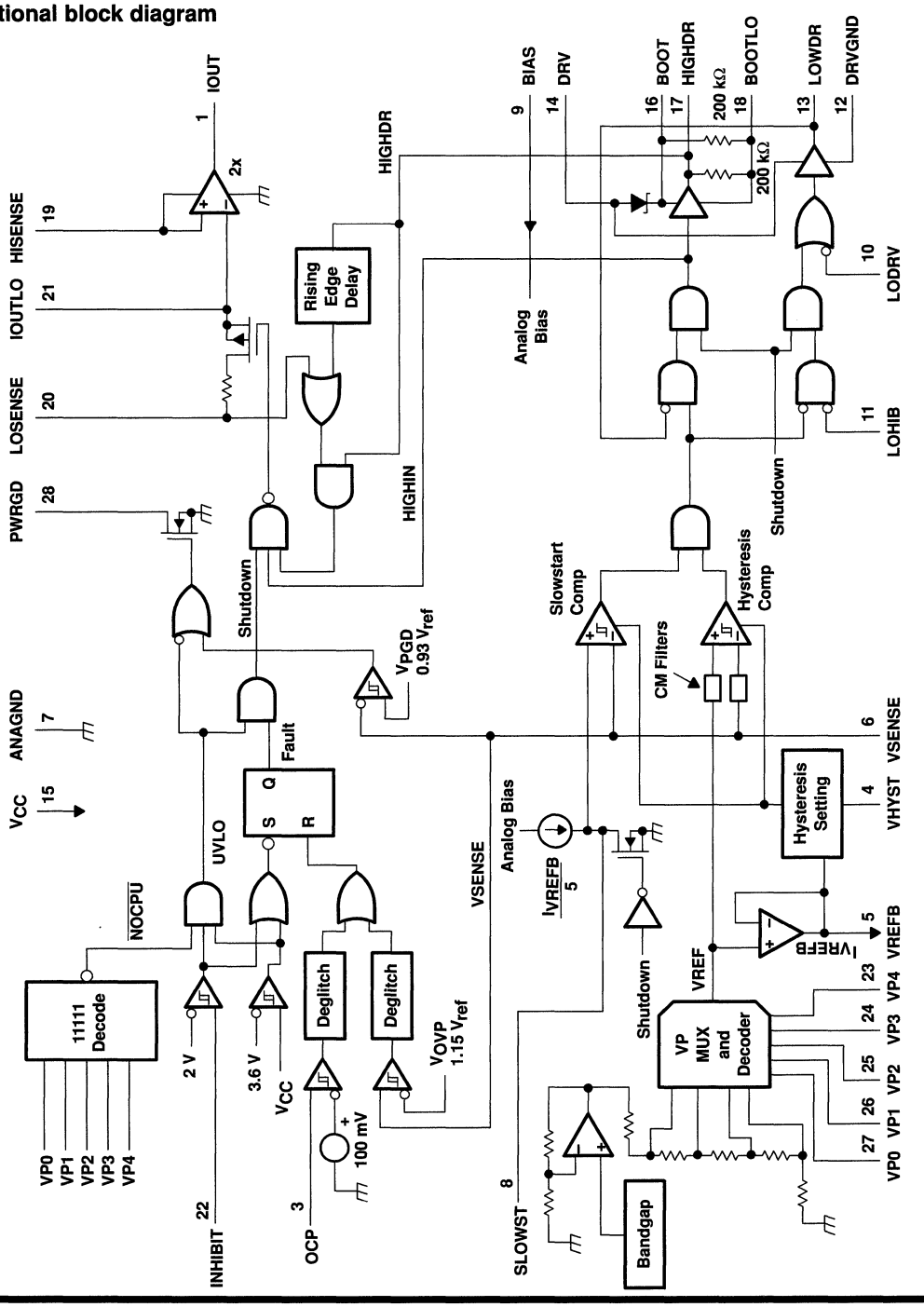
The TPS56100 is available in a 28-pin TSSOP PowerPAD package, which increases thermal efficiency and eliminates bulky heat sinks.

AVAILABLE OPTIONS

T_J	PACKAGES	EVM
	TSSOP† (PWP)	
0°C to 125°C	TPS561000PWP	TPS56100EVM–128

† The PWP package is also available taped and reel. To order, add an R to the end of the part number (e.g., TPS561000PWPR).

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANAGND	7	I	Analog ground
BIAS	9	I	Analog BIAS pin. This terminal must be connected to 5-V supply voltage. A 1-µF ceramic capacitor should be connected from BIAS to ANAGND.
BOOT	16	I	Bootstrap. Connect a 1-µF low-ESR capacitor from BOOT to BOOTLO.
BOOTLO	18	I	Bootstrap low. Connect BOOTLO to the junction of the high-side and low-side FETs for floating drive configuration. Connect BOOTLO to PGND for ground reference drive configuration.
DRV	14	I	Drive bias for the FET drivers. This terminal must be connected to 5-V supply voltage. A 1-µF ceramic capacitor should be connected from DRV to DRVGND.
DRVGND	12	I	Drive ground. Ground for FET drivers. Connect to FET PWRGND.
HIGHDR	17	O	High drive. Output drive to high-side power switching FETs
HISENSE	19	I	High current sense. For current sensing across high-side FETs, connect to the drain of the high-side FETs; for optional resistor sensing scheme, connect to power supply side of current-sense resistor placed in series with high-side FET drain.
INHIBIT	22	I	Disables the drive signals to the MOSFET drivers.
IOUT	1	O	Current out. Output voltage on this pin is proportional to the load current as measured across the Rds(on) of the high-side FETs. The voltage on this pin equals $2 \times R_{DS(on)} \times I_{OUT}$. In applications where very accurate current sensing is required, a sense resistor should be connected between the input supply and the drain of the high-side FETs.
IOUTLO	21	O	Current sense low output. This is the voltage on the LOSENSE pin when the high-side FETs are on. A ceramic capacitor should be connected from IOUTLO to HISENSE to hold the sensed voltage while the high-side FETs are off. Capacitance range should be between 0.033 µF and 0.1 µF.
LODRV	10	I	Low drive enable. Normally tied to 5 V. To activate the low-side FETs as a crowbar, pull LODRV low.
LOHIB	11	I	Low side inhibit. Connect to the junction of the high and low side FETs to control the anti-cross-conduction and eliminate shoot-through current. Disabled when configured in crowbar mode.
LOSENSE	20	I	Low current sense. For current sensing across high-side FETs, connect to the source of the high-side FETs; for optional resistor sensing scheme, connect to high-side FET drain side of current-sense resistor placed in series with high-side FET drain.
LOWDR	13	O	Low drive. Output drive to synchronous rectifier FETs
NC	2		Not connected
OCP	3	I	Over current protection. Current limit trip point is set with a resistor divider between IOUT and ANAGND.
PWRGD	28	O	Power good. Power Good signal goes high when output voltage is within 7% of voltage set by VID pins. Open-drain output.
SLOWST	8	O	Slow Start (soft start). A capacitor from SLOWST to ANAGND sets the slowstart time. Slowstart current = $I_{VREFB}/5$
V_{CC}	15	I	5-V supply. A 1-µF ceramic capacitor should be connected from V_{CC} to DRVGND.
VHYST	4	I	HYSTERESIS set pin. The hysteresis is set with a resistor divider from V_{REFB} to ANAGND. The hysteresis window = $2 \times (V_{REFB} - V_{HYST})$
VP0	27	I	Voltage programming input 0
VP1	26	I	Voltage programming input 1
VP2	25	I	Voltage programming input 2
VP3	24	I	Voltage programming input 3
VP4	23	I	Voltage programming input 4. Digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in Table 1. Internally pulled up to 5 V.
VREFB	5	O	Buffered reference voltage from VP network
VSENSE	6	I	Voltage sense Input. To be connected to converter output voltage bus to sense and control output voltage. It is recommended that an RC low pass filter be connected at this pin to filter noise.

detailed description

V_{REF}

The reference/voltage programming (VP) section consists of a temperature-compensated bandgap reference and a 5-bit voltage selection network. The 5 VP terminals are inputs to the VP selection network and are TTL-compatible inputs internally pulled up to 5 V. The VP codes conform to the Intel *VRM 8.3 DC-DC Converter Specification* for voltage settings between 1.8 V and 2.6 V, and they are decremented by 50 mV, down to 1.3 V, for the lower VP settings. Voltages higher than V_{REF} can be implemented using an external resistive divider. Refer to Table 1 for the VP code settings. The output voltage of the VP network, V_{REF}, is within ±1.5% of the nominal setting over the VP range of 1.3 V to 2.6 V, including a junction temperature range of 0°C to +125°C. The output of the reference/VP network is indirectly brought out through a buffer to the V_{REFB} pin. The voltage on this pin will be within 2% of V_{REF}. It is not recommended to drive loads with V_{REFB}, other than setting the hysteresis of the hysteretic comparator, because the current drawn from V_{REFB} sets the charging current for the slowstart capacitor. Refer to the slowstart section for additional information.

hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by 2 external resistors and is centered about V_{REF}. The 2 external resistors form a resistor divider from V_{REFB} to ANAGND, with the output voltage connecting to the V_{HYST} pin. The hysteresis of the comparator will be equal to twice the voltage *difference* between the V_{REFB} and V_{HYST} pins. The propagation delay from the comparator inputs to the driver outputs is 300 ns (maximum). The maximum hysteresis setting is 60 mV.

low-side driver

The low-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The bias to the low-side driver is derived from DRV.

high-side driver

The high-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from DRV. The internal bootstrap diode connected between the DRV and BOOT pins is a Schottky for improved drive efficiency. The maximum voltage that can be applied between BOOT and DRVGND is 30 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting BOOT to a voltage supply.

deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate-drive voltage to the low-side FETs is below 2 V; the low-side driver is not allowed to turn on until the voltage at the junction of the high-side and low-side FETs (Vphase) is below 2 V.

current sensing

Current sensing is achieved by sampling and holding the voltage across the high-side power FETs while the high-side FETs are on. The sampling network consists of an internal 85-Ω switch and an external ceramic hold capacitor. Recommended value of the hold capacitor is between 0.033 µF and 0.1 µF. Internal logic controls the turnon and turnoff of the sample/hold switch such that the switch does not turn on until the Vphase voltage transitions high, and the switch turns off when the input to the high-side driver goes low. The sampling will occur only when the high-side FETs are conducting current. The voltage on the IOUT pin equals 2 times the sensed high-side voltage. In applications where a higher accuracy in current sensing is required, a sense resistor can be placed in series with the high-side FETs, and the voltage across the sense resistor can be sampled by the current sensing circuit.

detailed description (continued)

inhibit

INHIBIT is a TTL-compatible digital input used to enable the controller. When INHIBIT is low, the output drivers are low and the slowstart capacitor is discharged. When INHIBIT goes high, the short across the slowstart capacitor is released and normal converter operation begins. The 5-V supply must be above UVLO thresholds before the controller is allowed to start up. The inhibit start threshold is 2.1 V and the hysteresis is 100 mV for the INHIBIT comparator.

V_{CC} undervoltage lockout (UVLO)

The undervoltage lockout circuit disables the controller while the V_{CC} supply is below the 4-V start threshold during power up. When the controller is disabled, the output drivers will be low and the slowstart capacitor is discharged. When V_{CC} exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 0.5-V hysteresis in the undervoltage lockout circuit for noise immunity.

slowstart

The slowstart circuit controls the rate at which V_O powers up. A capacitor is connected between SLOWST and ANAGND and is charged by an internal current source. The current source is proportional to the reference voltage, so that the charging rate of C_{SLOWST} is proportional to the reference voltage. By making the charging current proportional to V_{REF}, the power-up time for V_O will be independent of V_{REF}. Thus, C_{SLOWST} can remain the same value for all VP settings. The slowstart charging current is determined by the following equation:

$$I_{slowstart} = I(V_{REFB}) / 5 \quad \text{(amps)}$$

Where $I(V_{REFB})$ is the current flowing out of V_{REFB}.

It is recommended that no additional loads be connected to V_{REFB}, other than the resistor divider for setting the hysteresis voltage. The maximum current that can be sourced by the V_{REFB} circuit is 500 μA. The equation for setting the slowstart time is:

$$t_{SLOWST} = 5 \times C_{SLOWST} \times R_{VREFB} \quad \text{(seconds)}$$

Where R_{VREFB} is the total external resistance from V_{REFB} to ANAGND.

power good

The power-good circuit monitors for an undervoltage condition on V_O. If V_O is 7% below V_{REF}, then the PWRGD pin is pulled low. PWRGD is an open-drain output.

overvoltage protection

The overvoltage protection (OVP) circuit monitors V_O for an overvoltage condition. If V_O is 15% above V_{REF}, then a fault latch is set and both output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value or INHIBIT is low. A 3-μs deglitch timer is included for noise immunity. Refer to the LODRV section for information on how to protect the microprocessor against overvoltages due to a shorted high-side power FET.

detailed description (continued)

overcurrent protection

The overcurrent protection (OCP) circuit monitors the current through the high-side FET. The overcurrent threshold is adjustable with an external resistor divider between IOUT and ANAGND, with the divider voltage connected to the OCP pin. If the voltage on OCP exceeds 100 mV, then a fault latch is set and the output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value and back up above

3.6 V or INHIBIT is similarly brought below its stop threshold and back above its start threshold. A 3-µs deglitch timer is included for noise immunity. The OCP circuit is also designed to protect the high-side power FET against a short-to-ground fault on the terminal common to both power FETs.

LODRV

The LODRV circuit is designed to protect the microprocessor against overvoltages that can occur if the high-side power FETs become shorted. External components sensing an overvoltage condition are required to use this feature. When an overvoltage fault occurs, the low-side FETs are used as a crowbar. LODRV is pulled low and the low-side FET will be turned on, overriding all control signals inside the TPS5210 controller. The crowbar action will short the input supply to ground through the faulted high-side FETs and the low-side FETs. A fuse in series with V_{in} should be added to disconnect the short circuit.

Table 1. Voltage Programming Codes

VP TERMINALS (0 = GND, 1 = floating or pull-up to 5 V)					V_{REF}
VP4	VP3	VP2	VP1	VP0	(Vdc)
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	No CPU
1	1	1	1	0	2.10
1	1	1	0	1	2.20
1	1	1	0	0	2.30
1	1	0	1	1	2.40
1	1	0	1	0	2.50
1	1	0	0	1	2.60

Table 1. Voltage Programming Codes (Continued)

VP TERMINALS (0 = GND, 1 = floating or pull-up to 5 V)					V_{REF}
VP4	VP3	VP2	VP1	VP0	(Vdc)
1	1	0	0	0	2.60
1	0	1	1	1	2.60
1	0	1	1	0	2.60
1	0	1	0	1	2.60
1	0	1	0	0	2.60
1	0	0	1	1	2.60
1	0	0	1	0	2.60
1	0	0	0	1	2.60
1	0	0	0	0	2.60

absolute maximum ratings over operating virtual junction temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note1), BIAS, DRV ..... –0.3 V to 7 V
Input voltage range: BOOT to DRVGND (High-side Driver ON) ..... –0.3 V to 30 V
BOOT to HIGHDRV ..... –0.3 V to 15 V
BOOT to BOOTLO ..... –0.3 V to 15 V
INHIBIT, VPx, LODRV ..... –0.3 V to 7.3 V
PWRGD, OCP ..... –0.3 V to 7 V
LOHIB, LOSENSE, IOUTLO, HISENSE ..... –0.3 V to 7 V
VSENSE ..... –0.3 V to 5 V
Voltage difference between ANAGND and DRVGND ..... ±0.5 V
Output current, V_{REFB} ..... 0.5 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... 0°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to ANAGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	1150 mW	11.5 mW/°C	630 mW	460 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.5	6	V
Input voltage, BOOT to DRVGND	0	28	V
Input voltage, BOOT to BOOTLO	0	13	V
Input voltage, INHIBIT, VPx, LODRV, PWRGD, OCP	0	6	V
Input voltage, LOHIB, LOSENSE, IOUTLO, HISENSE, BIAS, DRV	0	6	V
Input voltage, VSENSE	0	4.5	V
Voltage difference between ANAGND and DRVGND	0	±0.2	V
Output current, V_{REFB}†	0	0.4	mA

† Not recommended to load V_{REFB} other than to set hystersis since I_{VREFB} sets slowstart time.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 5 V (unless otherwise noted)

reference/voltage programming

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Cumulative voltage reference accuracy	V_{CC} = 4.5 to 5.5 V, 1.3 V ≤ V_{REF} ≤ 2.6 V, See Note 2	–1.5%		1.5%	
VPx	High-level input voltage		2.25			V
VPx	Low-level input voltage				1	V
V_{REFB}	Output voltage	I_{VREFB} = 50 µA	V_{REF}–10 mV	V_{REF}	V_{REF}+10 mV	V
	Output regulation	10 µA ≤ I_O ≤ 500 µA		2		mV
VPx	Input pullup resistance			190		kΩ

NOTES: 2. Cumulative reference accuracy is the combined accuracy of the reference voltage and the input offset voltage of the hysteretic comparator. Cumulative accuracy equals the average of the high-level and low-level thresholds of the hysteretic comparator.
3. This parameter is ensured by design and is not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 5 V (unless otherwise noted) (continued)

power good

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Undervoltage trip threshold		90	93	95	%V_{REF}
V_{OL}	Low-level output voltage	I_O = 2.5 mA		0.4	0.75	V
I_{OH}	High-level input current	V_{PWRGD} = 5 V		1		µA
V_{hys}	Hysteresis voltage			3		%V_{REF}

slowstart

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge current	V_{SLOWST} = 0.5 V, V_{VREFB} = 1.3 V, I_{VREFB} = 65 µA	10.4	13	15.6	µA
Discharge current	V_{SLOWST} = 1 V	3			mA
Comparator input offset voltage		–18		18	mV
Comparator input bias current	See Note 3		10	100	nA
Comparator hysteresis		–8.5		8.5	mV

NOTE 3: This parameter is ensured by design and is not production tested.

hysteretic comparator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	See Note 3	–4		4	mV
Input bias current	See Note 3			500	nA
Hysteresis accuracy	$V_{REFB} - V_{HYST}$ = 15 mV (Hysteresis window = 30 mV)	–5		5	mV
Maximum hysteresis setting	$V_{REFB} - V_{HYST}$ = 30 mV		60		mV

NOTE 3: This parameter is ensured by design and is not production tested.

thermal shutdown

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Over temperature trip point	See Note 3		160		°C
Hysteresis	See Note 3		10		°C

NOTE 3: This parameter is ensured by design and is not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 5 V (unless otherwise noted) (continued)

high-side VDS sensing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain			2		V/V
	Initial accuracy	$V_{HISENSE}$ = 5 V, $V_{LOSENSE}$ = 4.5 V	194		206	mV
IOUTLO	Sink current	V_{IOUTLO} = 5 V			250	nA
IOUT	Source current	V_{IOUT} = 0.5 V, $V_{HISENSE}$ = 5 V, V_{IOUTLO} = 4.5 V	500			µA
IOUT	Sink current	V_{IOUT} = 0.05 V, $V_{HISENSE}$ = 5 V, V_{IOUTLO} = 5 V	50			µA
	Output voltage swing	$V_{HISENSE}$ = 4.5 V, R_{IOUT} = 10 kΩ	0		1	V
		$V_{HISENSE}$ = 3 V, R_{IOUT} = 10 kΩ	0		0.75	V
LOSENSE	High-level input voltage	$V_{HISENSE}$ = 4.5 V (see Note 3)	2.85			V
	Low-level input voltage				2.4	V
	Sample/hold resistance	4.5 V ≤ $V_{HISENSE}$ ≤ 5.5 V, LOSENSE connected to HISENSE, $V_{HISENSE}$ – V_{IOUTLO} = 0.15 V	62	85	123	Ω
		3 V ≤ $V_{HISENSE}$ ≤ 3.6 V, LOSENSE connected to HISENSE, $V_{HISENSE}$ – V_{IOUTLO} = 0.15 V	67	95	144	Ω
CMRR		$V_{HISENSE}$ = 5.5 V to 3 V, $V_{HISENSE}$ – V_{OUTLO} = 100 mV	62	65		dB

NOTE 3. This parameter is ensured by design and is not production tested.

inhibit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		1.85	2.1	2.35	V
Hysteresis		0.08	0.1	0.14	V
Stop threshold		1.76			V

overvoltage protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overvoltage trip threshold		112	115	120	%V_{REF}
Hysteresis	See Note 3		10		mV

NOTE 3: This parameter is ensured by design and is not production tested.

overcurrent protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OCP trip threshold		80	100	125	mV
Input bias current				100	nA

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 5 V (unless otherwise noted) (continued)

deadtime

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOHIB	High-level input voltage		2.4			V
	Low-level input voltage				1.33	
LOWDR	High-level input voltage	See Note 3	2.38			V
	Low-level input voltage	See Note 3			1.23	

NOTE 3: This parameter is ensured by design and is not production tested.

LODRV

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LODRV	High-level input voltage		1.70			V
	Low-level input voltage				0.95	

input undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		3.8	4.08	4.46	V
Hysteresis		0.4	0.5	0.6	V
Stop threshold		3.3			V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 5 V (unless otherwise noted) (continued)

output drivers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output current (see Note 4)	High-side sink	Duty cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 4.5 V,	0.7			A
	High-side source	V_{HIGHDR} = 0.5 V (source) or 4 V (sink), See Note 3	1.2			
	Low-side sink	Duty Cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, V_{DRV} = 4.5 V,	1.3			
	Low-side source	V_{LOWDR} = 0.5 V (source) or 4 V (sink), See Note 3	1.4			
Output resistance (see Note 4)	High-side sink	T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 4 V (source) or 0.5 V (sink)			5	Ω
	High-side source				75	
	Low-side sink	T_J = 125°C, V_{DRV} = 4.5 V, V_{LOWDR} = 4 V (source) or 0.5 V (sink)			9	
	Low-side source				75	

NOTES: 3. This parameter is ensured by design and is not production tested.
4. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{ds(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		4.5	5	5.5	V
V_{CC}	Quiescent current	$V_{INHIBIT}$ = 5 V, V_{CC} > 4.46 V at startup, VP code ≠ 11111, V_{BOOTLO} = 0 V		3	10	mA
		$V_{INHIBIT}$ = 5 V, V_{CC} > 4.46 V at startup, C_{HIGHDR} = 50 pF, f_{SWX} = 200 kHz, VP code ≠ 11111, V_{BOOTLO} = 0 V, C_{LOWDR} = 50 pF, See Note 3		5		
	High-side driver quiescent current	$V_{INHIBIT}$ = 0 V or VP code = 11111 or V_{CC} < 3.8 V at startup, V_{BOOT} = 13 V, V_{BOOTLO} = 0 V			90	µA
		$V_{INHIBIT}$ = 5 V, V_{BOOT} = 13 V, C_{HIGHDR} = 50 pF, VP code ≠ 11111, V_{CC} > 4.46 V at startup, V_{BOOTLO} = 0 V, f_{SWX} = 200 kHz (see Note 3)		2		mA

NOTE 3: This parameter is ensured by design and is not production tested.

switching characteristics over recommended operating virtual-junction temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay	VSENSE to HIGHDR or LOWDR (excluding dead-time)	1.3 V ≤ V_{VREF} ≤ 2.6 V, 10 mV overdrive (see Note 3)		230	300	ns
	OCP comparator	See Note 3		1		µs
	OVP comparator			1		
	PWRGD comparator			1		
	SLOWST comparator	Overdrive = 10 mV (see Note 3)		700	1000	ns
Rise and fall time	HIGHDR output	C_L = 6 nF, V_{BOOT} = 4.5 V, V_{BOOTLO} = 0 V, T_J = 125°C			120	ns
	LOWDR output	C_L = 6 nF, V_{DRV} = 4.5 V, T_J = 125°C			80	
Deglitch time (Includes comparator propagation delay)	OCP	See Note 3	2		5	µs
	OVP		1.8		5	
Response time	High-side VDS sensing	$V_{HISENSE}$ = 4.5 V, V_{IOUTLO} pulsed from 4.5 V to 4.4 V, 100 ns rise/fall times (see Note 3)			3	µs
		$V_{HISENSE}$ = 3 V, V_{IOUTLO} pulsed from 3 V to 2.9 V, 100 ns rise/fall times (see Note 3)			3	
Short-circuit protection rising-edge delay	SCP	LOSENSE = 0 V (see Note 3)	300		500	ns
Turnon/turnoff delay	V_{DS} sensing sample/hold switch	3 V ≤ $V_{HISENSE}$ ≤ 5.5 V, $V_{LOSENSE}$ = $V_{HISENSE}$ (see Note 3)	30		100	ns
Crossover delay time	LOWDR to HIGHDRV, and LOHIB to LOWDR	See Note 3	50		200	ns
Prefilter pole frequency	Hysteretic comparator	See Note 3		5		MHz
Propagation delay	LODRV	See Note 3			400	ns

NOTE 3: This parameter is ensured by design and is not production tested.

TYPICAL CHARACTERISTICS

SLOWSTART TIME
vs
SLOWSTART CAPACITANCE

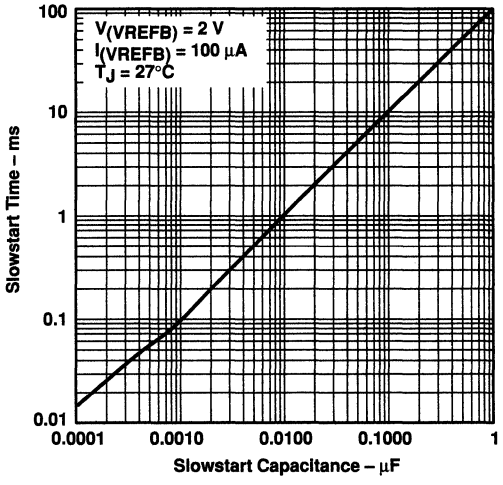


Figure 1

SLOWSTART TIME
vs
SUPPLY CURRENT (VREFB)

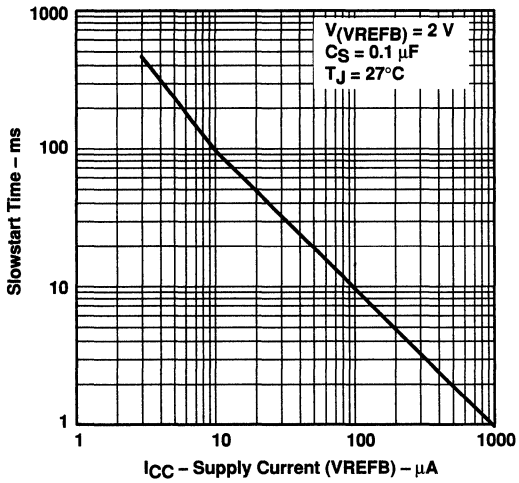


Figure 2

DRIVER
RISE TIME
vs
LOAD CAPACITANCE

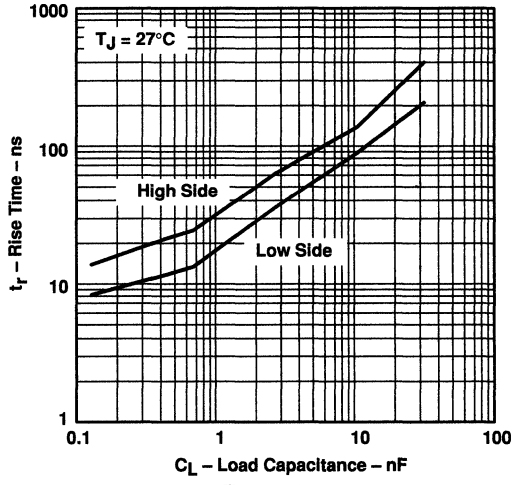


Figure 3

DRIVER
FALL TIME
vs
LOAD CAPACITANCE

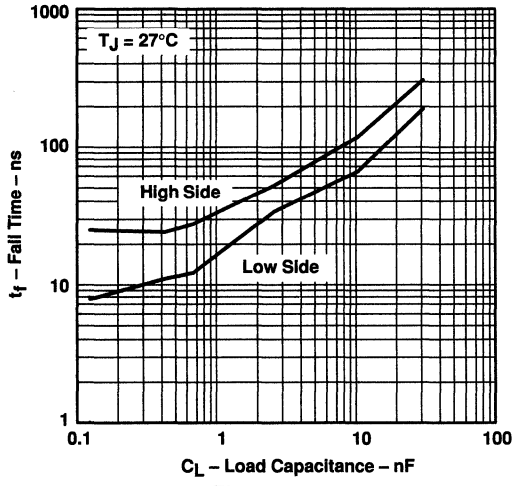


Figure 4

TYPICAL CHARACTERISTICS

OVP THRESHOLD
vs
JUNCTION TEMPERATURE

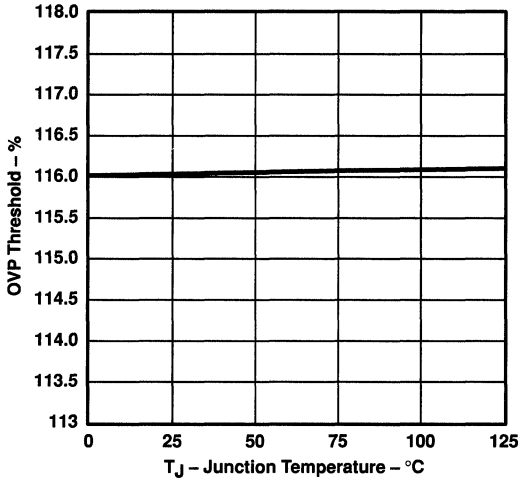


Figure 5

OCP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

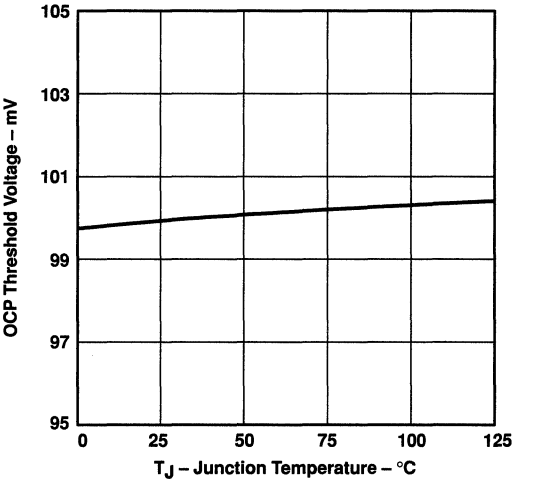


Figure 6

INHIBIT START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

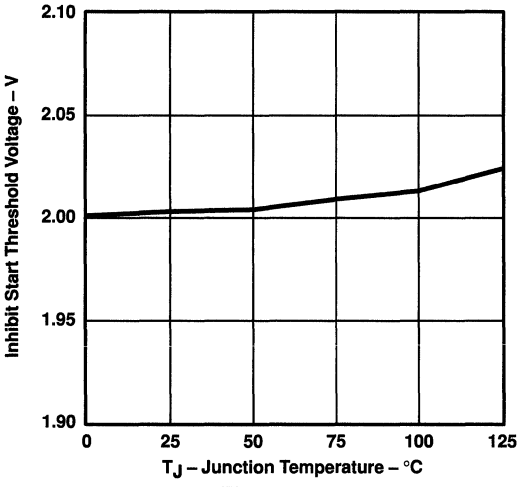


Figure 7

INHIBIT HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

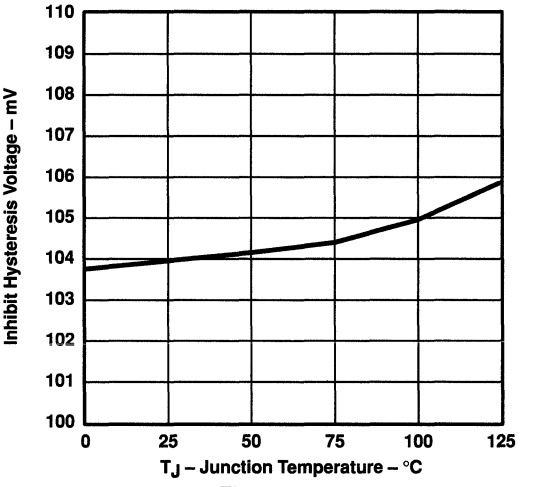


Figure 8

TYPICAL CHARACTERISTICS

UVLO START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

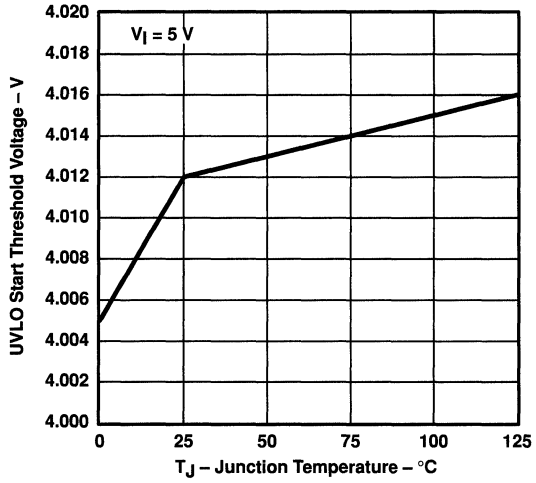


Figure 9

UVLO HYSTERESIS
vs
JUNCTION TEMPERATURE

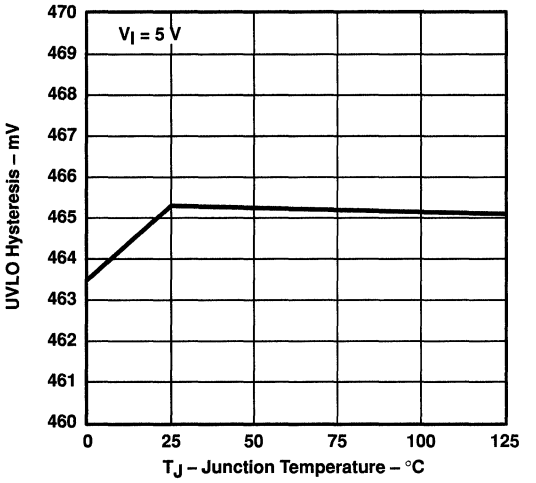


Figure 10

QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE

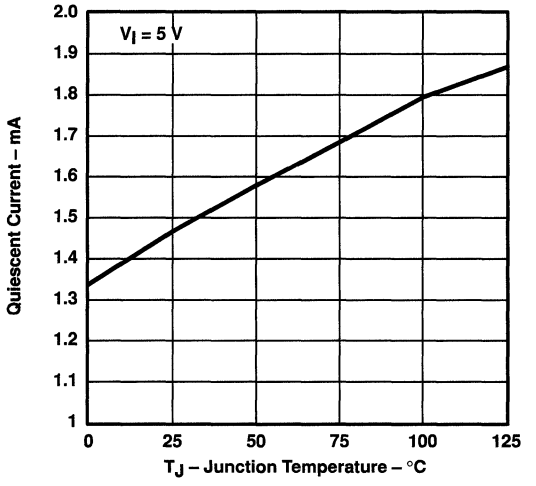


Figure 11

POWERGOOD THRESHOLD
vs
JUNCTION TEMPERATURE

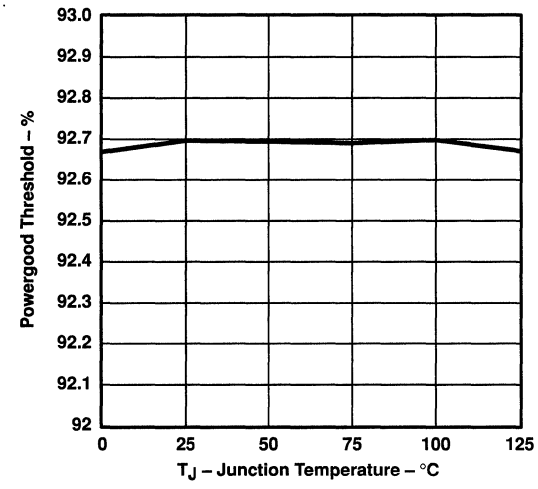


Figure 12

TYPICAL CHARACTERISTICS

SLOW START CHARGE CURRENT
vs
JUNCTION TEMPERATURE

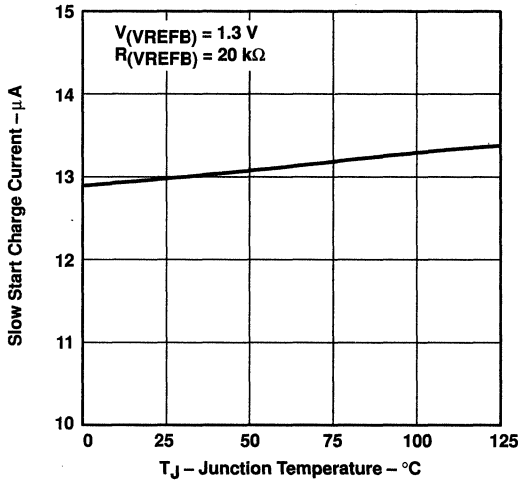


Figure 13

DRIVER
HIGH-SIDE OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

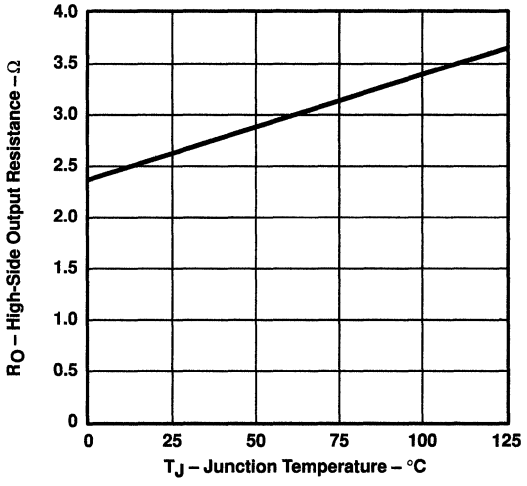


Figure 14

DRIVER
LOW-SIDE OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

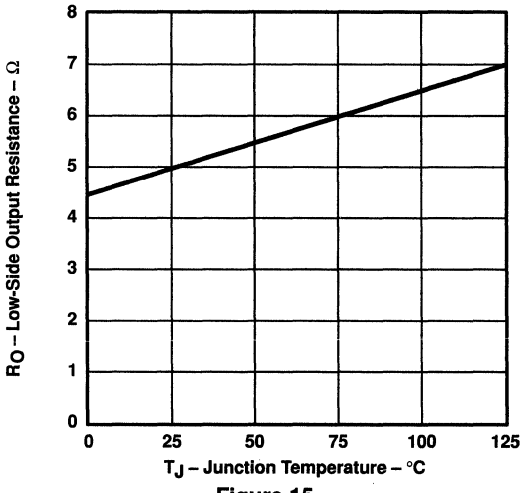


Figure 15

SENSING SAMPLE/HOLD RESISTANCE
vs
JUNCTION TEMPERATURE

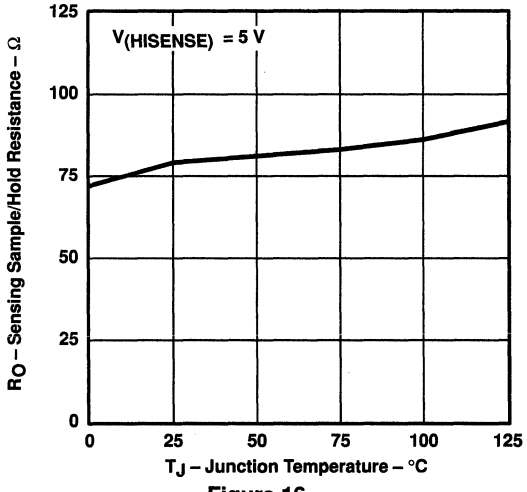


Figure 16

APPLICATION INFORMATION

The hysteretic-type controller method used in the TPS56100 controller gives very fast transient response for today's high-speed DSP applications. Traditional PWM-type controllers use an oscillator to control the timing of the control signals used to adjust the output voltage. During a transient load event, the PWM-type controller must wait until the next oscillator cycle to begin the output voltage adjustment process. This delay causes output droop (or overshoot) and longer recovery times. Hysteretic-type controllers, such as the TPS56100, are self-oscillating and require no cycle-time to begin the recovery process. Hysteretic controllers have extremely high gain and are sensitive to noise. The TPS56100 has internal low-pass noise filters to eliminate much of this problem, however an external RC low-pass filter between the output and VSENSE input is recommended.

The TPS56100 controller includes all of the functions necessary for a dependable high-efficiency power converter. High-current synchronous MOSFET drivers are used for fast, low-loss switching allowing for efficiencies greater than 90%. An internal bootstrap circuit provides the high-side drive voltage necessary for the upper n-channel MOSFET. Overcurrent protection protects the power supply in case of load faults. Overvoltage protection protects the load in case of high-side switch failure. Programmable hysteresis allows users to tailor the output ripple and operating frequency to suit their needs. Slowstart provides a controlled rampup time for the output voltage eliminating output overshoot. Inhibit is provided for sequencing of the converter in multiple-voltage circuits. Power good provides an indication that the output voltage is within operating limits. The design of each of these functions is discussed in detail in the following. Refer to Figure 19 for location of components discussed in the following.

APPLICATION INFORMATION

frequency calculation

A detailed derivation of frequency calculation is shown in the application report, *Designing Fast Response Synchronous Buck Regulators Using the TPS5210*, TI Literature number SLVA044. When less accurate results are acceptable, the simplified equation shown below can be used:

$$f_S \cong \frac{\left(V_O \times \left[V_I - V_O\right] \times ESR\right)}{\left(V_I \times L \times \text{Hysteresis Window}\right)}$$

control section

Below are the equations needed to select the various components within the control section. Component reference numbers refer to the example application given at the end of this section. Details and the derivations of the equations used in this section are available in the application report *Designing Fast Response Synchronous Buck Regulators Using the TPS5210*, TI Literature number SLVA044.

output voltage selection

Of course the most important function of the power supply is to regulate the output voltage to a specific value. Values between 1.3 V and 2.6 V can be easily set by shorting the correct VP inputs to ground. Values above the maximum reference voltage (2.6 V) can be set by changing the reference voltage to any convenient voltage within its range and selecting values for R2 and R3 to give the correct output. Select R3:

R3 << than $V_{REF}/I_{BIAS(VSENSE)}$; a recommended value is 10 kΩ

Then, calculate R2 using:

$$V_O = V_{REF}\left(1 + \frac{R2}{R3}\right) \quad \text{or} \quad R2 = \frac{R3 \times \left(V_O - V_{REF}\right)}{V_{REF}}$$

R2 and R3 can also be used to make small adjusts to the output voltage within the reference-voltage range. If there is no need to adjust the output voltage, R3 can be eliminated. R2, R3 (if used), and C7 are used as a noise filter; calculate using:

$$C7 = \frac{150\ ns}{(R2 \parallel R3)}$$

Recommended values for 3.3 V: V_{REF} = 1.65 V, R3 = 1.00 kΩ, R2 = 1.00 kΩ, and C7 = 100 pF.

slowstart timing

Slowstart reduces the start-up stresses on the power-stage components and reduces the input current surge. Slowstart timing is a function of the reference-voltage current (determined by R5) and is independent of the reference voltage. The first step in setting slowstart timing will be to determine R5:

R5 should be between 7 kΩ and 300 kΩ, a recommended value is 20 kΩ.

APPLICATION INFORMATION

slowstart timing (continued)

Set the slowstart timing using the formula:

$$C5 = \frac{t_{SS}}{\left(5 \times R_{VREFB}\right)} \cong \frac{t_{SS}}{(5 \times R5)}$$

Where

C5 = Slowstart capacitance in μF
t_{SS} = Slowstart timing in μs
R_{VREFB} = Resistance from VREFB to GND in ohms (≈ R5)

hysteresis voltage

A hysteretic controller regulates by self-oscillation, thus requiring a small ripple voltage on the output which the input comparator uses for sensing. Once selected, the TPS56100 hysteresis is proportional to the reference voltage; programming Vref to a new value automatically adjusts the hysteresis to be the same percentage of Vref. The actual output ripple voltage is the combination of the hysteresis voltage, overshoot caused by internal delays, and the output capacitor characteristics. Figure 19 shows the hysteresis window voltage (V_{HI} to V_{LO}) and the output voltage ripple (V_{MAX} to V_{MIN}). Since the output current from VREFB should be less than 500 μA, the total divider resistance (R4 + R5) should be greater than 7 kΩ. The hysteresis voltage should be no greater than 60 mV so R5 will dominate the divider.

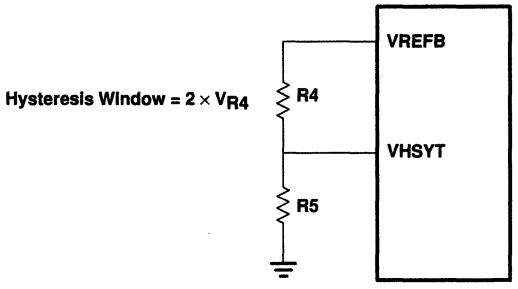


Figure 17. Hysteresis Divider Circuit

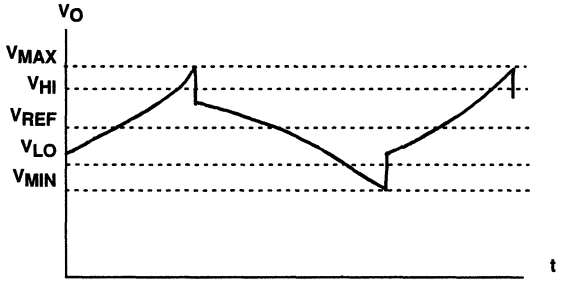


Figure 18. Output Ripple

APPLICATION INFORMATION

hysteresis voltage (continued)

The upper divider resistor, R4, is calculated using:

$$R4 = \frac{\text{Hysteresis Window}}{2 \times (\text{VREFB} - \text{Hysteresis Window})} \times R5 \cong \frac{V_{HYST}(\%)}{(2 \times 100)} \times R5$$

Where

Hysteresis Window = the desired peak-to-peak hysteresis voltage.
VREFB = selected reference voltage.
V_{HYST} (%) = [(Hysteresis Window)/VREFB] * 100 < $V_{O(Ripple)(P-P)}$ (%)

current limit

Current limit can be implemented using the on-resistance of the upper FETs as the sensing element. Select R7:

$$R7 \ll \frac{V_{OCP}}{I_{Bias(OCP)}} \leq \frac{0.1\ V}{(100 \times 100\ nA)} \leq 10\ k\Omega \quad \text{(A recommended value is 1 k}\Omega\text{)}$$

The IOUT signal is used to drive the current limit divider. The voltage at IOUT at the output current trip point will be:

$$V_{IOUT(Trip)} = \frac{\left(2 \times R_{DS(ON)} \times TF\right)}{\text{NumFETs}} \times I_{O(Trip)}$$

Where

NumFETS = Number of upper FETS in Parallel.
TF = $R_{DS(ON)}$ temperature correction factor.
$I_{O(Trip)}$ = Desired output current trip level (A).

Calculate R6 using:

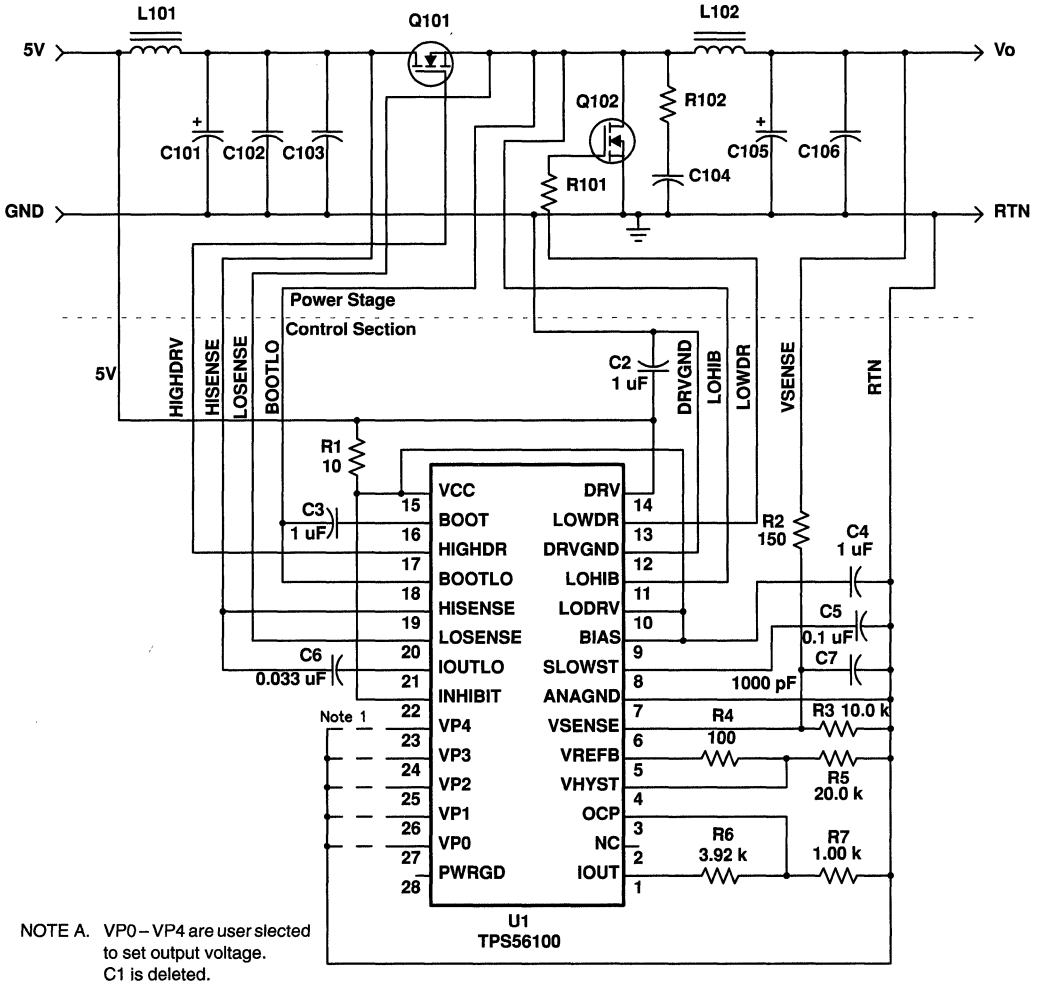
$$R6 = \left(\frac{V_{IOUT(Trip)}}{0.1\ V} - 1\right) \times R7$$

Note that since $R_{DS(ON)}$ of MOSFETs can vary from lot to lot and with temperature, tight current-limit control (less than 1.5 x I_O) using this method is not practical. If tight control is required, an external current-sense resistor in series with the drain of the upper FET can be used with HISENSE and LOSENSE connected across the resistor.

APPLICATION INFORMATION

application example

Below is a typical application schematic. The circuit can be divided into the power-stage section and the control-circuit section. The power stage must be tailored to the input/output requirements of the application. The control circuit is basically the same for all applications with some minor tweaking of specific values.



NOTE A. VP0 – VP4 are user slected to set output voltage. C1 is deleted.

Figure 19. Typical Application Schematic

APPLICATION INFORMATION

application example (continued)

Table 2. Power Stage Components

Ref Des	Function	4–A Out	8–A Out	12–A Out	20–A Out
C101	Input Bulk Capacitor	Sanyo, 10TPB220M, 220–µF, 10–V, 20%	Sanyo, 10SA220M, 2 x 220–µF, 10–V, 20%	Sanyo, 10SP470M, 2 x 470–µF, 10–V, 20%	Sanyo, 10SP470M, 3 x 470–µF, 10–V, 20%
C102	Input Mid–Freq Capacitor	muRata, GRM42–6Y5V105Z025A, 1.0–µF, 25–V, +80%–20%, Y5V	muRata, GRM42–6Y5V225Z016A, 2.2–µF, 16–V, +80%–20%, Y5V	muRata, GRM42–6Y5V225Z016A, 2.2–µF, 16–V, +80%–20%, Y5V	muRata, GRM42–6Y5V105Z025A, 3 x 1.0–µF, 25–V, +80%–20%, Y5V
C103	Input Hi–Freq Bypass Capacitor	muRata, GRM39X7R104K016A, 0.1–µF, 16–V, X7R	muRata, GRM39X7R104K016A, 0.1–µF, 16–V, X7R	muRata, GRM39X7R104K016A, 2 x 0.1–µF, 16–V, X7R	muRata, GRM39X7R104K016A, 3 x 0.1–µF, 16–V, X7R
C104	Snubber Capacitor	muRata, GRM39X7R102K050A, 1000–pF, 50–V, X7R	muRata, GRM39X7R102K050A, 1000–pF, 50–V, X7R	muRata, GRM39X7R102K050A, 2 x 1000 pF, 50–V, X7R	muRata, GRM39X7R102K050A, 3 x 1000–pF, 50–V, X7R
C105	Output Bulk Capacitor	Sanyo, 4TPC150, 2 x 150–µF, 4–V, 20%	Sanyo, 4SP820M, 820–µF, 4–V, 20%	Sanyo, 4SP820M, 2 x 820–µF, 4–V, 20%	Sanyo, 4SP820M, 3 x 820–µF, 4–V, 20%
C106	Output Hi–Freq Bypass Capacitor	muRata, GRM39X7R104K016A, 0.1–µF, 16–V, X7R	muRata, GRM39X7R104K016A, 0.1–µF, 16–V, X7R	muRata, GRM39X7R104K016A, 2 x 0.1–µF, 16–V, X7R	muRata, GRM39X7R104K016A, 3 x 0.1–µF, 16–V, X7R
L101	Input Filter Inductor	CoilCraft, DO1608C–332, 3.3–µH, 2.0–A	Coiltronics, UP2B–2R2, 2.2–µH, 7.2–A	Coiltronics, UP2B–2R2, 2.2–µH, 7.2–A	Coiltronics, UP3B–1R0, 1–µH, 12.5–A
L102	Output Filter Inductor	CoilCraft, DO3316P–332, 3.3–µH, 6.1–A	Coiltronics, UP3B–2R2, 2.2–µH, 9.2–A	Coiltronics, UP4B–1R5, 1.5–µH, 13.4–A	MicroMetals, T68–8/90 Core w/7T #16, 1.0–µH, 25–A
R101	Lo–Side Gate Resistor	3.3–Ω, 1/16–W, 5%	3.3–Ω, 1/16–W, 5%	2 x 3.3–Ω, 1/16–W, 5%	3 x 3.3–Ω, 1/16–W, 5%
R102	Snubber Resistor	2.7–Ω, 1/10–W, 5%	2.7–Ω, 1/10–W, 5%	2 x 2.7–Ω, 1/10–W, 5%	3 x 2.7–Ω, 1/10–W, 5%
Q101	Power Switch	IR, IRF7811, NMOS, 11–mΩ	IR, IRF7811, NMOS, 11–mΩ	IR, 2 x IRF7811, NMOS, 11–mΩ	IR, 2 x IRF7811, NMOS, 11–mΩ
Q102	Synchronous Switch	IR, IRF7811, NMOS, 11–mΩ	IR, IRF7811, NMOS, 11–mΩ	IR, 2 x IRF7811, NMOS, 11–mΩ	IR, 3 x IRF7811, NMOS, 11–mΩ
Nominal Frequency†		280 kHz	250 kHz	170 kHz	170 kHz
Hysteresis Window		15 mV	15 mV	15 mV	15 mV

† Nominal frequency measured with Vo set to 1.5 V.

The values listed above are recommendations based on actual test circuits. Many variations of the above are possible based upon the desires and/or requirements of the user. Performance of the circuit is equally, if not more, dependent upon the layout than on the specific components, as long as the device parameters are not exceeded. Fast-response, low-noise circuits require critical attention to the layout details. Even though the operating frequencies of typical power supplies are relatively low compared to today's microprocessor circuits, the power levels and edge rates can cause severe problems both in the supply and the load. The power stage, having the highest current levels and greatest dv/dt rates, should be given the greatest attention.

APPLICATION INFORMATION

layout guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, place the low-level components. Below are several specific points to consider *before* layout of a TPS56100 design begins.

1. All sensitive analog components should be referenced to ANAGND. These include components connected to SLOWST, IOUT, OCP, VSENSE, VREFB, VHYST, BIAS, and LOHIB.
2. Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.
3. Connections from the drivers to the gate of the power FETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
4. The bypass capacitor for the DRV input should be placed close to the TPS56100 and be connected to DRVGND.
5. The bypass capacitor for V_{CC} should be placed close to the TPS56100 and be connected to AGND.
6. When configuring the high-side driver as a floating driver, the connection from BOOTLO to the power FETs should be as short and as wide as possible. The other pins that also connect to the power FETs, LOHIB and LOSENSE, should have a separate connection to the FETS since BOOTLO will have large peak currents flowing through it.
7. When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from BOOT to BOOTLO) should be placed close to the TPS56100.
8. When configuring the high-side driver as a ground-referenced driver, BOOTLO should be connected to DRVGND.
9. The bulk storage capacitors across V_I should be placed close to the power FETS. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
10. High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
11. HISENSE and LOSENSE should be connected very close to the drain and source, respectively, of the high-side FET. HISENSE and LOSENSE should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed close to where HISENSE connects to Vin, to reduce high-frequency noise coupling on HISENSE.

8 Switching PS and DC/DC Converters

features

- Up to 200-mA Output Current
- Less Than 5-mV_{pp} Output Voltage Ripple
- No Inductors Required/Low EMI
- Regulated 3.3-V ±4% Output
- Only Four External Components Required
- Up to 90% Efficiency
- 1.8-V to 3.6-V Input Voltage Range
- 50-μA Quiescent Supply Current
- 0.05-μA Shutdown Current
- Load Isolated in Shutdown
- Space-Saving Thermally-Enhanced TSSOP PowerPAD™ Package
- Evaluation Module Available (TPS60100EVM–131)

description

The TPS60100 step-up, regulated charge pump generates a 3.3-V ±4% output voltage from a 1.8-V to 3.6-V input voltage (two alkaline, NiCd, or NiMH batteries). Output current is 200 mA from a 2-V input. Only four external capacitors are needed to build a complete low-noise dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple as current is continuously transferred to the output. From a 2-V input, the TPS60100 can start into full load with loads as low as 16 Ω.

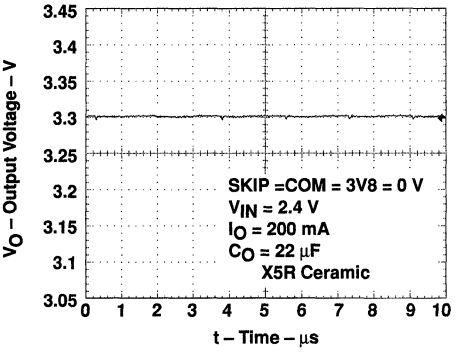
The TPS60100 features either constant frequency mode to minimize noise and output voltage ripple or the power-saving pulse-skip mode to extend battery life at light loads. The TPS60100 switching frequency is 300 kHz. The logic shutdown function reduces the supply current to 1-μA (max) and disconnects the load from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during start-up. This dc/dc converter requires no inductors and has low EMI. It is available in the small 20-pin TSSOP PowerPAD™ package (PWP).

applications

Replaces DC/DC Converters With Inductors in

- Battery-Powered Applications
- Two Battery Cells to 3.3-V Conversion
- Portable Instruments
- Battery-Powered Microprocessor and DSP Systems
- Miniature Equipment
- Backup-Battery Boost Converters
- PDAs
- Laptops
- Handheld Instrumentation
- Medical Instruments
- Cordless Phones

output voltage ripple



typical operating circuit

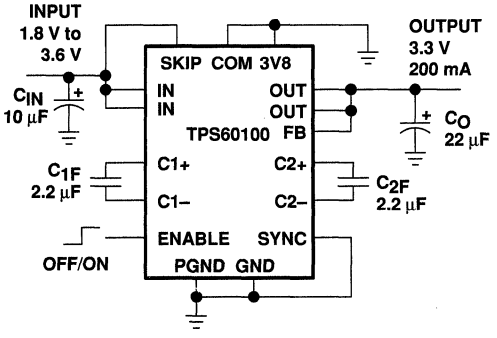
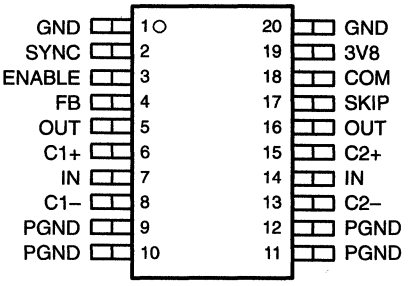


Figure 1

PowerPAD is a trademark of Texas Instruments Incorporated.

PWP PACKAGE
(TOP VIEW)



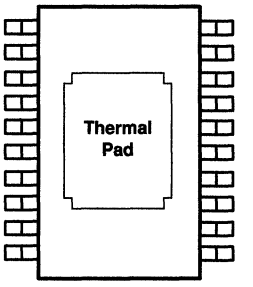


Figure 2. Bottom View of PWP Package, Showing the Thermal Pad

AVAILABLE OPTIONS

PACKAGE
TSSOP† (PWP)
TPS60100PWP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TPS60100PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3V8	19	I	Mode selection. When 3V8 is logic low the charge pump operates in the regulated 3.3-V mode. When 3V8 is connected to IN the regulator operates in preregulated 3.8-V mode.
C1+	6		Positive terminal of the charge-pump capacitor C_{1F}
C1–	8		Negative terminal of the charge-pump capacitor C_{1F}
C2+	15		Positive terminal of the charge-pump capacitor C_{2F}
C2–	13		Negative terminal of the charge-pump capacitor C_{2F}
COM	18	I	Mode selection. When COM is logic low the charge pump operates in push-pull mode to minimize output ripple. When COM is connected to IN the regulator operates in single-ended mode requiring only one flying capacitor.
ENABLE	3	I	ENABLE Input. The device turns off, the output disconnects from the input, and the supply current decreases to 0.05 µA when ENABLE is a logic low. Connect ENABLE to IN for normal operation.
FB	4	I	FEEDBACK input. Connect FB to OUT as close to the load as possible to achieve best regulation. Resistive divider is on chip to match internal reference voltage of 1.22 V.
GND	1, 20		GROUND. Analog ground for internal reference and control circuitry. Connect to PGND through a short trace.
IN	7, 14	I	Supply Input. Connect to an input supply in the 1.8-V to 3.6-V range. Bypass IN to GND with a (C_O/2) µF capacitor. Connect both INs through a short trace.
OUT	5, 16	O	Regulated power output. Connect both OUTs through a short trace and bypass OUT to GND with the output filter capacitor C_O. V_O = 3.3 V when 3V8 = low and V_O = 3.8 V when 3V8 = high.
PGND	9–12		PGND power ground. Charge-pump current flows through this pin. Connect all PGNDs together.
SKIP	17	I	Mode selection. When SKIP is logic low, the charge pump operates in constant-frequency mode. Output ripple and noise are minimized in this mode. When SKIP is connect to IN, the device operates in pulse skip mode. Quiescent current is lowest in this mode.
SYNC	2	I	Selection for external clock signal. Connect to GND to use the internally generated clock signal. Connect to IN for external synchronization. In this case, the clock signal needs to be fed through 3V8 and the device operates in the regulated 3.3-V mode.

absolute maximum ratings (unless otherwise noted)†‡

Input voltage range, V_I (IN, OUT, ENABLE, SKIP, COM, 3V8, FB, SYNC) ..... –0.3 V to 5.5 V
Differential input voltage, V_{ID} (C1+, C2+ to GND) ..... –0.3 V to (V_{OUT} + 0.3 V)
Differential input voltage, V_{ID} (C1–, C2– to GND) ..... –0.3 V to (V_{IN} + 0.3 V)
Continuous total power dissipation ..... See Dissipation Rating Tables
Continuous output current ..... 300 mA
Storage temperature range, T_{stg} ..... –55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10s ..... 260°C
Maximum junction temperature, T_J ..... 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ V_{ENABLE}, V_{SKIP}, V_{COM}, V_{3V8} and V_{SYNC} can exceed V_{IN} up to the maximum rated voltage without increasing the leakage current drawn by these mode select inputs.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	700 mW	5.6 mW/°C	448 mW	364 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)

PACKAGE	$T_C \le 62.5°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING
PWP	25 W	285.7 mW/°C	22.9 W	18.5 W

DISSIPATION DERATING CURVE§ vs FREE-AIR TEMPERATURE

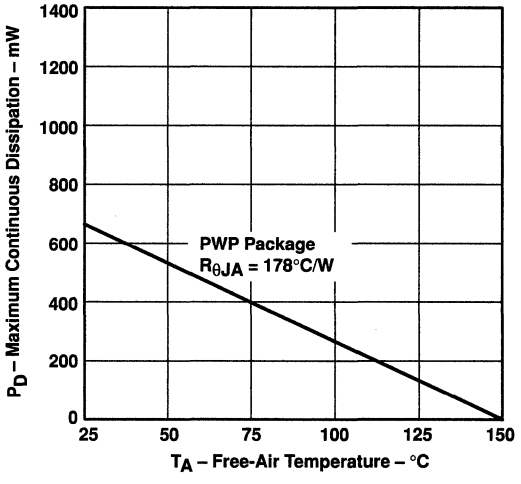


Figure 3

MAXIMUM CONTINUOUS DISSIPATION§ vs CASE TEMPERATURE

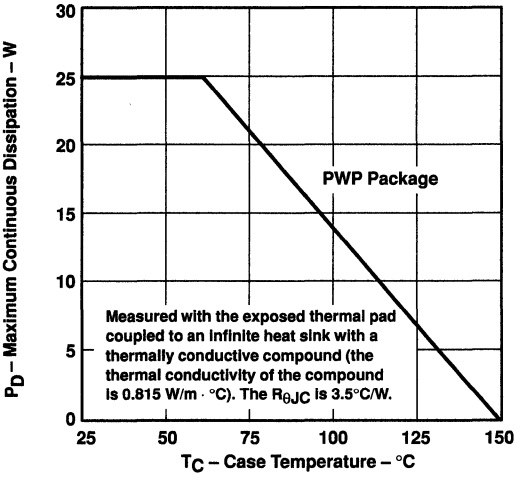


Figure 4

§ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. It is recommended not to exceed a junction temperature of 125°C.

electrical characteristics at C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF†, C_O = 22 µF, T_C = –40°C to 85°C, V_{IN} = 2 V, V_{FB} = V_O, V_{ENABLE} = V_{IN}, V_{SKIP} = V_{IN} or 0 V and V_{COM} = V_{3V8} = V_{SYNC} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.8		3.6	V
$V_{IN(UV)}$	Input undervoltage lockout threshold				1.6	1.8	V
$I_{O(MAX)}$	Maximum output current			200			mA
V_O	Output voltage	1.8 V < V_{IN} < 2 V, $V_{O(Start-Up)}$ = 3.3 V,	0 < I_O < 100 mA, T_C = 25°C	3.17	3.3	3.43	V
		2 V < V_{IN} < 3.3 V,	0 < I_O < 200 mA	3.17	3.3	3.43	
		3.3 V < V_{IN} < 3.6 V,	0 < I_O < 200 mA	3.17	3.3	3.47	
$V_{O(RIP)}$	Output voltage ripple	I_O = 200 mA,	V_{SKIP} = 0 V		5‡		mV_{PP}
$I_{O(LEAK)}$	Output leakage current	V_{IN} = 2.4 V,	V_{ENABLE} = 0 V			1	µA
I_Q	Quiescent current (no-load input current)	V_{SKIP} = V_{IN} = 2.4 V			50	90	µA
		V_{SKIP} = 0 V,	V_{IN} = 2.4 V		1.5		mA
$I_{DD(SDN)}$	Shutdown supply current	V_{IN} = 2.4 V,	V_{ENABLE} = 0 V		0.05	1	µA
$f_{OSC(int)}$	Internal switching frequency	V_{IN} = 2.4 V		200	300	400	kHz
$f_{OSC(ext)}$	External clock frequency	V_{SYNC} = V_{IN},	V_{IN} = 1.8V to 3.6 V	400	600	800	kHz
	External clock duty cycle	V_{SYNC} = V_{IN},	V_{IN} = 1.8V to 3.6 V	20%		80%	
	Efficiency	I_O = 100 mA			80%		
V_{INL}	Input voltage low, ENABLE, SKIP, COM, 3V8, SYNC	V_{IN} = 1.8 V				0.3 × V_{IN}	V
V_{INH}	Input voltage high, ENABLE, SKIP, COM, 3V8, SYNC	V_{IN} = 3.6 V		0.7 × V_{IN}			V
$I_{I(LEAK)}$	Input leakage current, ENABLE, SKIP, COM, 3V8, SYNC	V_{ENABLE} = V_{SKIP} = V_{COM} = V_{3V8} = V_{SYNC} = V_{GND} or V_{IN}			0.01	0.1	µA
	Output load regulation	V_O = 3.3 V, T_C = 25°C	1 mA < I_O < 200 mA		0.004		%/mA
	Output line regulation	2 V < V_{IN} < 3.3 V, I_O = 100 mA,	V_O = 3.3 V, T_C = 25°C		0.6		%/V
	Short circuit current	V_{IN} = 2.4 V T_C = 25°C	V_O = 0 V,		125		mA

† Use only ceramic capacitors with X5R or X7R dielectric as flying capacitors.
‡ Achieved with C_O = 22 µF X5R dielectric ceramic capacitor

electrical characteristics for preregulated 3.8-V Mode ($V_{(3V8)}$ = V_{IN}), C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF†, C_O = 22 µF, T_C = –40°C to 85°C, V_{IN} = 2.4 V, V_{FB} = V_O, V_{ENABLE} = V_{IN}, V_{SKIP} = V_{IN} or 0 V and V_{COM} = V_{SYNC} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2.2		3.6	V
$I_{O(MAX)}$	Maximum output current		200			mA
V_O	Output voltage	2.2 V < V_{IN} < 3.6 V, 0 < I_O < 200 mA	3.6	3.8	4	V
$I_{O(LEAK)}$	Output leakage current	V_{ENABLE} = 0 V			1	µA
I_Q	Quiescent current (no-load input current)	V_{SKIP} = V_{IN}		60		µA
		V_{SKIP} = 0 V		2		mA
$I_{DD(SDN)}$	Shutdown supply current	V_{ENABLE} = 0 V		0.05	1	µA
f_{OSC}	Internal switching frequency		200	300	400	kHz
	Short circuit current	V_O = 0 V, T_C = 25°C		125		mA

† Use only ceramic capacitors with X5R or X7R dielectric as flying capacitors.

TYPICAL CHARACTERISTICS†

EFFICIENCY
vs
OUTPUT CURRENT (V_O = 3.3 V)

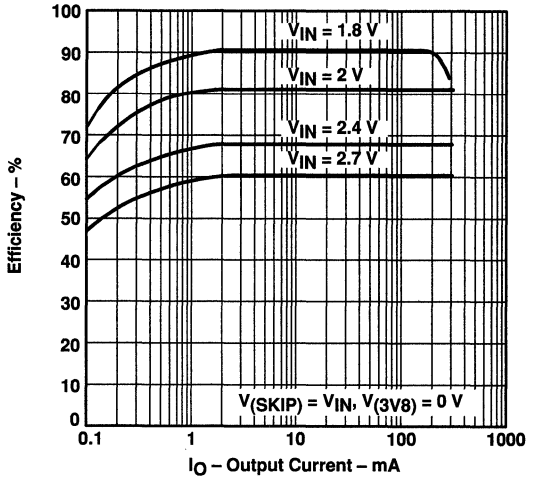


Figure 5

EFFICIENCY
vs
OUTPUT CURRENT (V_O = 3.3 V)

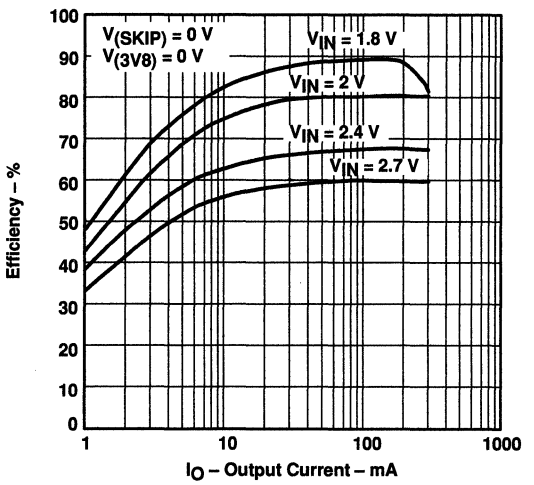


Figure 6

EFFICIENCY
vs
OUTPUT CURRENT (V_O = 3.8 V)

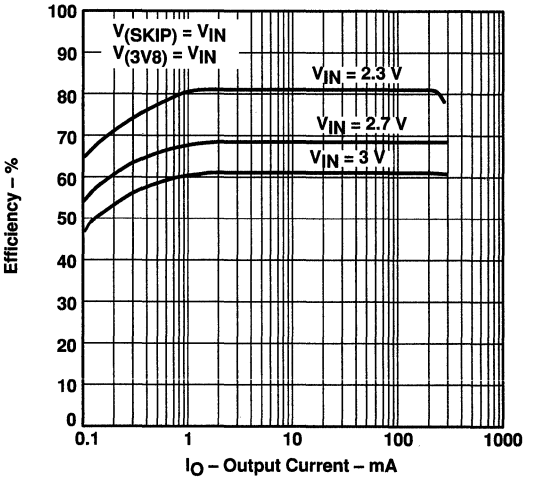


Figure 7

EFFICIENCY
vs
OUTPUT CURRENT (V_O = 3.8 V)

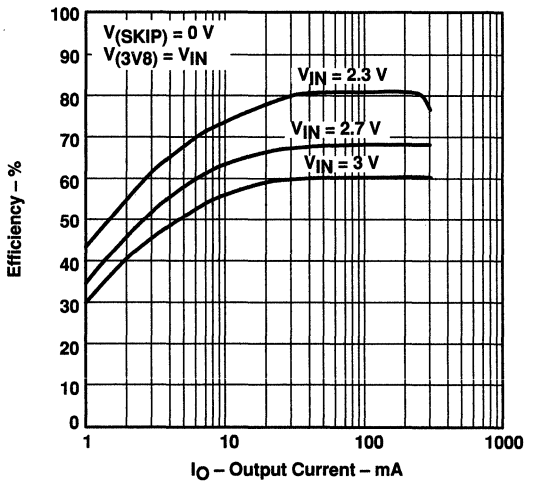


Figure 8

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 22 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

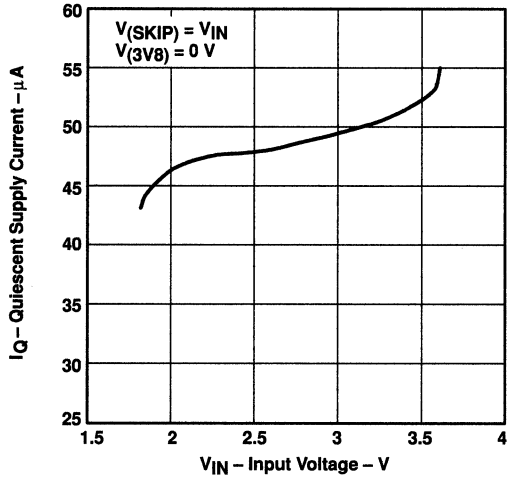


Figure 9

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

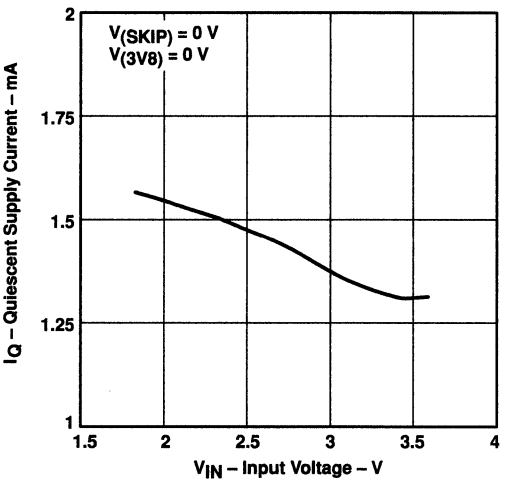


Figure 10

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

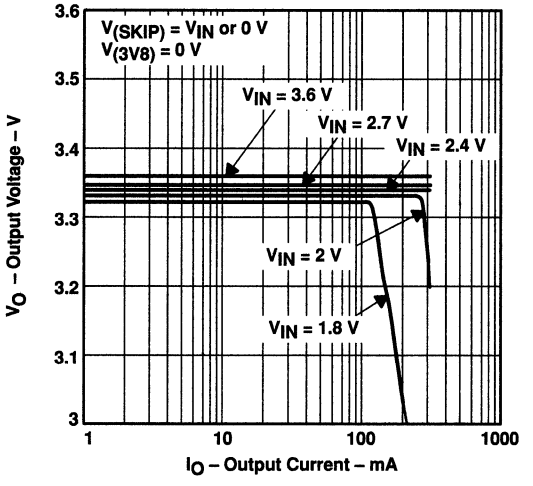


Figure 11

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

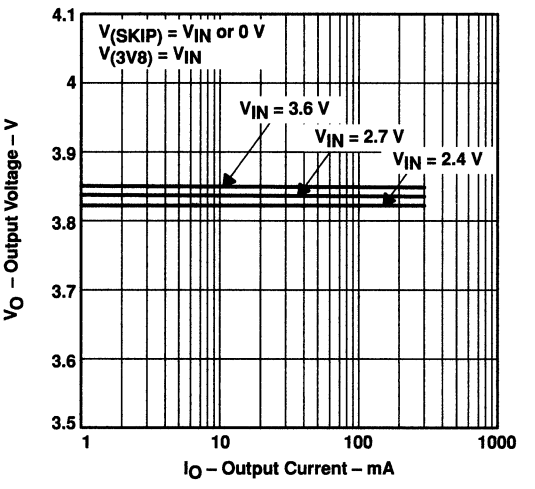


Figure 12

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 22 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs INPUT VOLTAGE

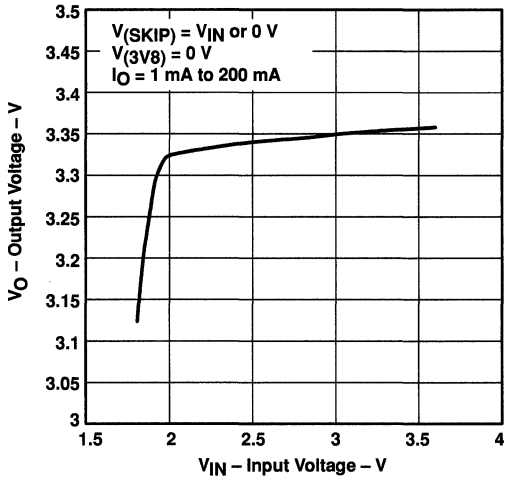


Figure 13

OUTPUT VOLTAGE vs INPUT VOLTAGE

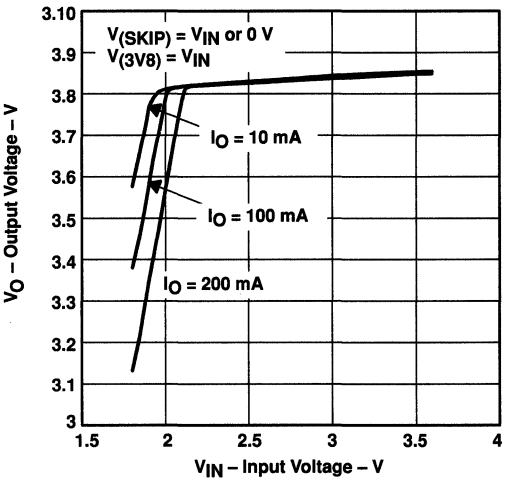


Figure 14

OUTPUT VOLTAGE vs TIME

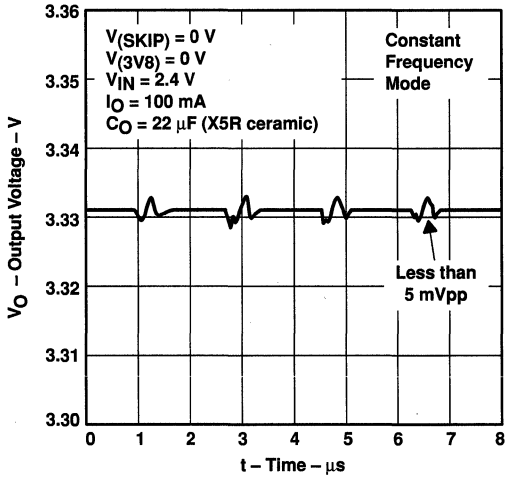


Figure 15

OUTPUT VOLTAGE vs TIME

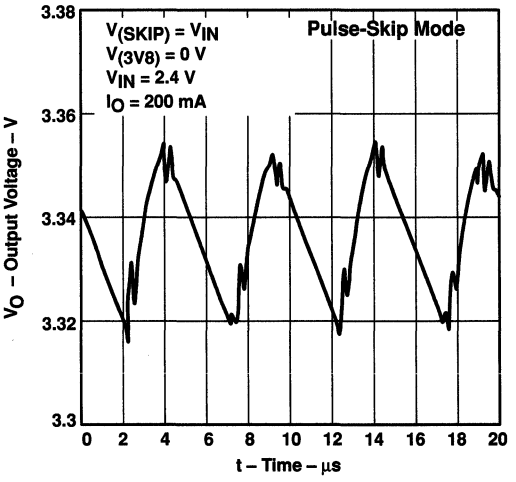


Figure 16

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 22 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

LOAD TRANSIENT RESPONSE

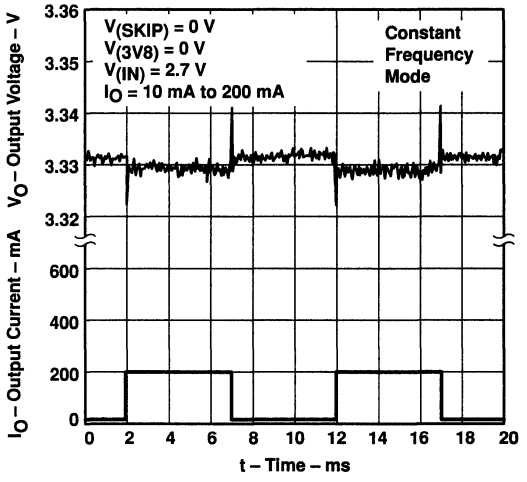


Figure 17

LOAD TRANSIENT RESPONSE

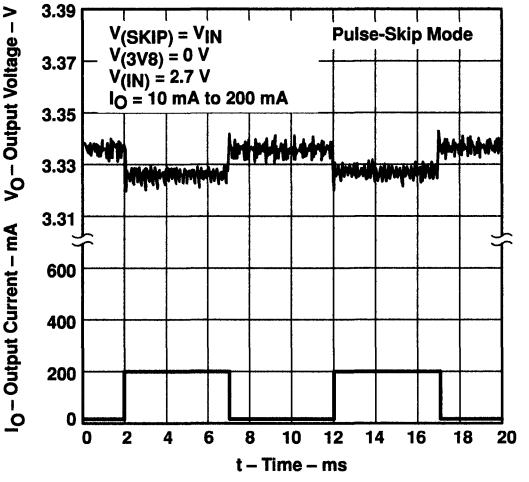


Figure 18

LINE TRANSIENT RESPONSE

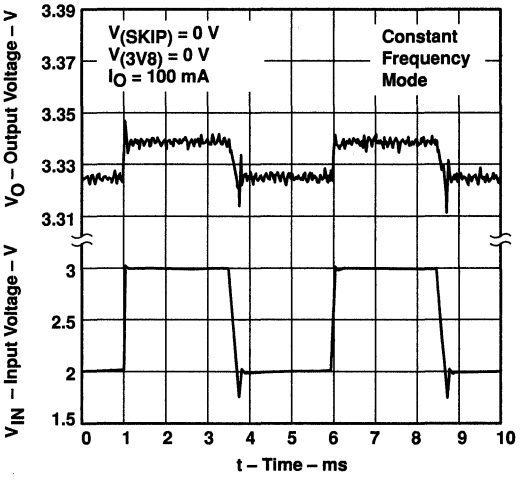


Figure 19

LINE TRANSIENT RESPONSE

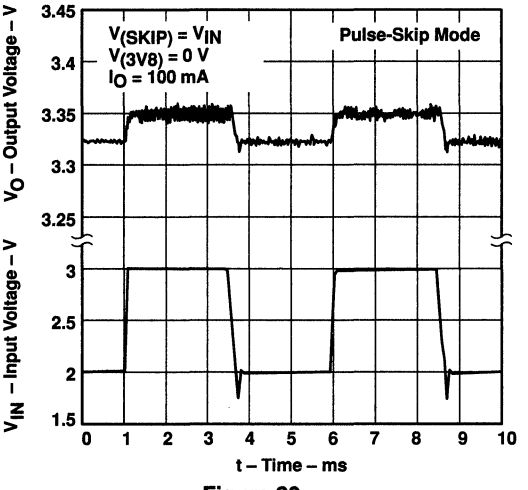


Figure 20

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 22 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

FREQUENCY SPECTRUM
CONSTANT FREQUENCY MODE‡

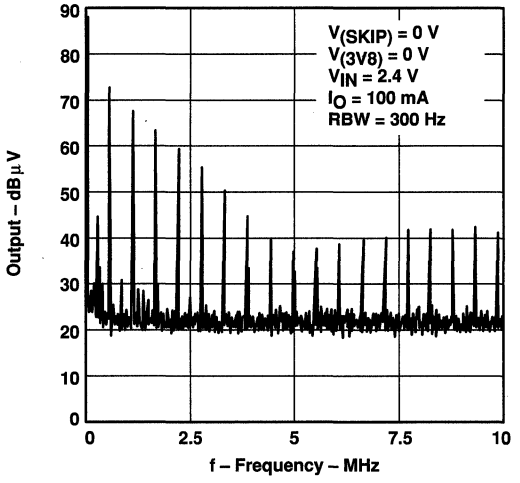


Figure 21

FREQUENCY SPECTRUM
PULSE-SKIP MODE‡

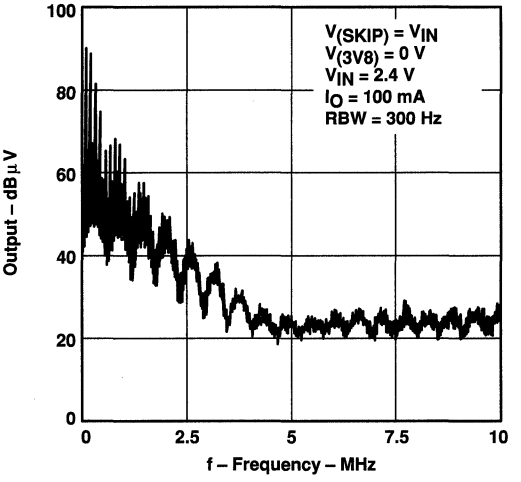


Figure 22

FREQUENCY SPECTRUM
CONSTANT FREQUENCY MODE‡

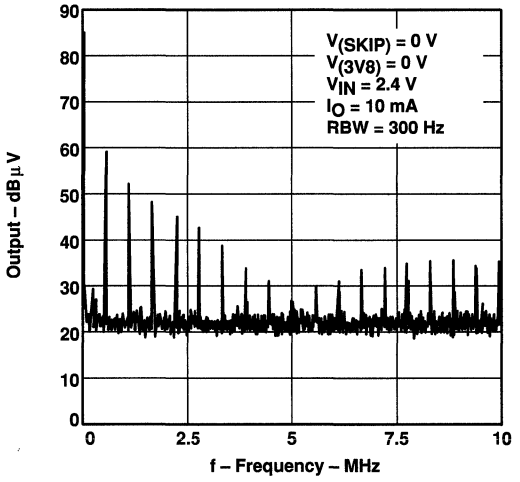


Figure 23

FREQUENCY SPECTRUM
PULSE-SKIP MODE‡

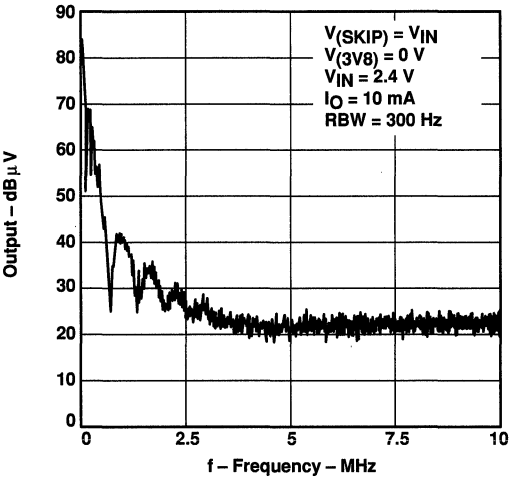


Figure 24

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 μF, C_{1F} = C_{2F} = 2.2 μF, C_O = 22 μF, unless otherwise noted
‡Test circuit: TPS60100EVM–131

TYPICAL CHARACTERISTICS†

EFFICIENCY
vs
INPUT VOLTAGE

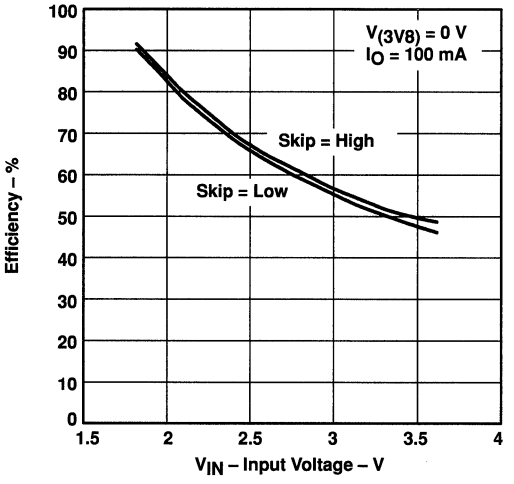


Figure 25

EFFICIENCY
vs
INPUT VOLTAGE

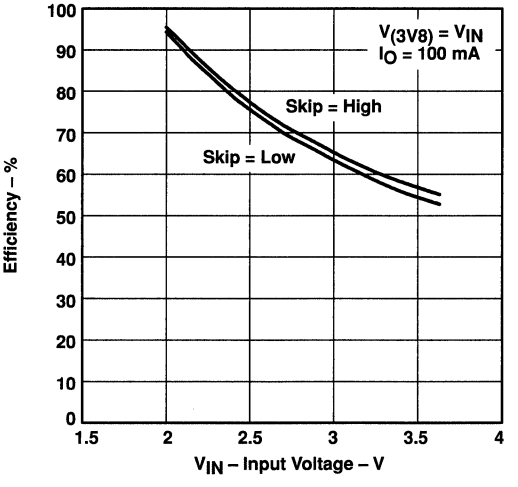


Figure 26

START-UP TIMING

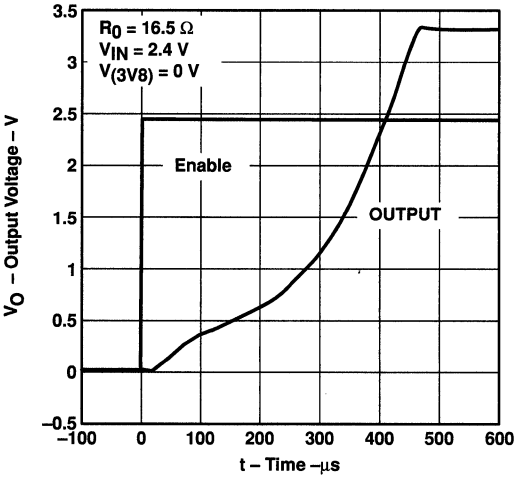


Figure 27

START-UP TIMING

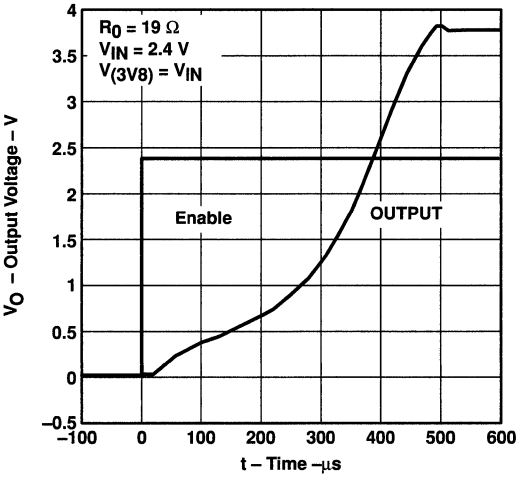


Figure 28

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 22 µF, unless otherwise noted

detailed description

operating principle

The TPS60100 charge pump provides a regulated 3.3-V output from a 1.8-V to 3.6-V input. It delivers a maximum load current of 200 mA. Designed specifically for space critical battery powered applications, the complete charge pump circuit requires only four external capacitors. The circuit can be optimized for highest efficiency at light loads or lowest output noise. The TPS60100 consists of an oscillator, a 1.22-V bandgap reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (Figure 29)

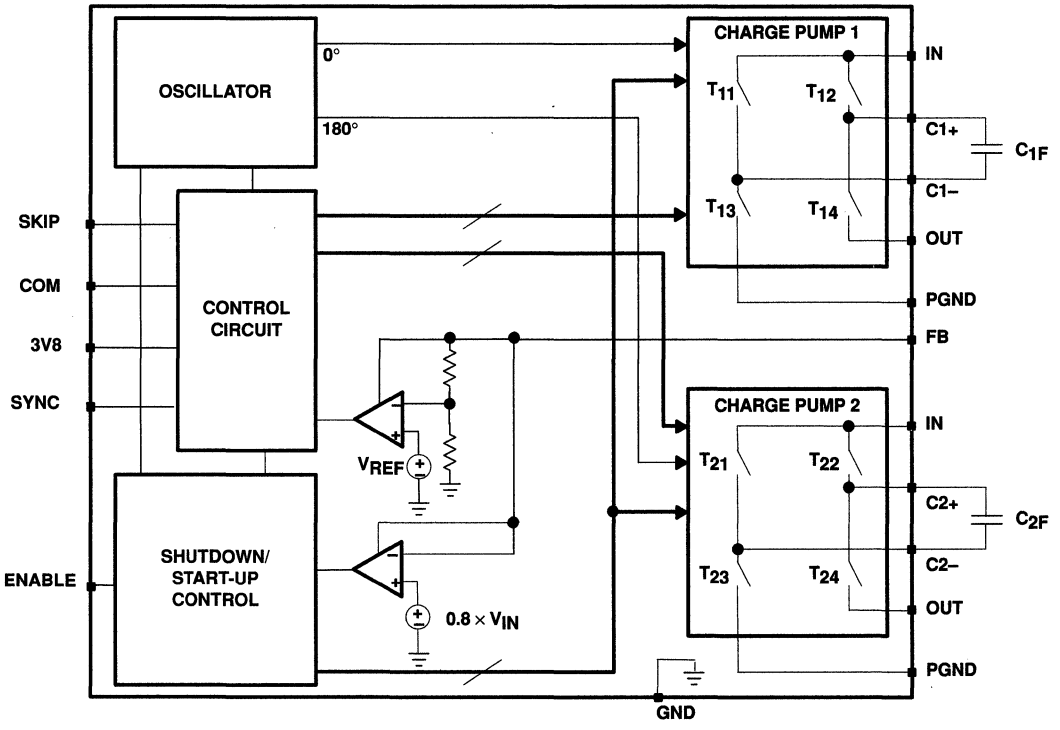


Figure 29. Functional Block Diagram TPS60100

The oscillator runs at a 50% duty cycle. The device consists of two single-ended charge pumps which operate with 180° phase shift. Each single ended charge pump transfers charge into its transfer capacitor (C_{XF}) in one half of the period. During the other half of the period (transfer phase), C_{XF} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name doubler). In order to provide a regulated fixed output voltage of 3.3 V, the TPS60100 uses either pulse-skip mode or constant-frequency mode. Pulse-skip mode and constant-frequency mode are externally selected via the SKIP input pin.

detailed description (continued)

start-up procedure

During start-up, i.e. when ENABLE is set from logic low to logic high, the switches T12 and T14 (charge pump 1), and the switches T22 and T24 (charge pump 2) are conducting to charge up the output capacitor until the output voltage V_O reaches $0.8 \times V_{IN}$. When the start-up comparator detects this limit, the IC begins to operate in the mode selected with SKIP, COM and 3V8. This start-up charging of the output capacitor guarantees a short start-up time and eliminates the need for a Schottky diode between IN and OUT.

pulse-skip mode

In pulse-skip mode (SKIP = high), the error amplifier disables switching of the power stages when it detects an output higher than 3.3 V. The oscillator halts. The IC then skips switching cycles until the output voltage drops below 3.3 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except bandgap reference and error amplifier when the output is higher than 3.3 V. When switching is disabled from the error amplifier, the load is also isolated from the input. SKIP is a logic input and should not remain floating. The typical operating circuit of the TPS60100 in pulse skip mode is shown in Figure 1.

constant-frequency mode

When SKIP is low, the charge pump runs continuously at the frequency f_{OSC}. The control circuit, fed from the error amplifier, controls the charge on C_{1F} and C_{2F} by driving the gates of the FETs T_{12}/T_{13} and T_{22}/T_{23}, respectively. When the output voltage falls, the gate drive increases, resulting in a larger voltage across C_{1F} and C_{2F}. This regulation scheme minimizes output ripple. Since the device switches continuously, the output noise contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads than pulse-skip mode.

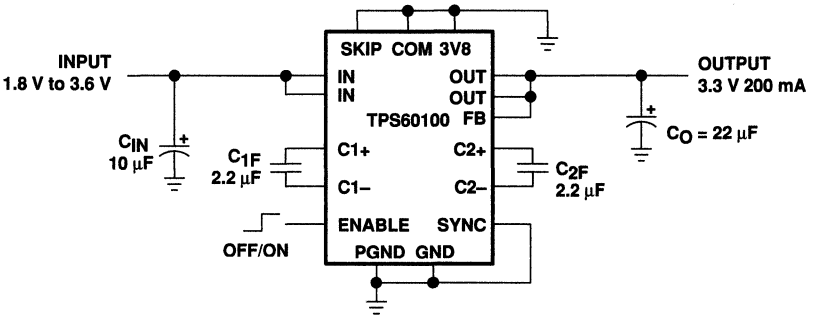


Figure 30. Typical Operating Circuit TPS60100 in Constant Frequency Mode

Table 1. Tradeoffs Between Operating Modes

FEATURE	PULSE-SKIP MODE (SKIP = High)	CONSTANT-FREQUENCY MODE (SKIP = Low)
Best light-load efficiency	X	
Smallest external component size for a given output ripple		X
Output ripple amplitude	Small amplitude	Very small amplitude
Output ripple frequency	Variable	Constant
Load regulation	Very good	Good

NOTE: Even in pulse-skip mode the output ripple amplitude is small if the push-pull operating mode is selected via COM.

detailed description (continued)

push-pull operating mode

In push-pull operating mode (COM = low), the two single-ended charge pumps operate with 180° phase shift. The oscillator signal has a 50% duty cycle. Each single-ended charge pump transfers charge into its transfer capacitor (C_{xF}) in one-half of the period. During the other half of the period (transfer phase), C_{xF} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple. COM is a logic input and should not remain floating. The typical operating circuit of the TPS60100 in push-pull mode is shown in Figure 1 and Figure 30.

single-ended operating mode

When COM is high, the device runs in single-ended operating mode. The two single-ended charge pumps operate in parallel without phase shift. They transfer charge into the transfer capacitor (C_F) in one half of the period. During the other half of the period (transfer phase), C_F is placed in series with the input to transfer its charge to C_O. In single-ended operating mode only one transfer capacitor ($C_F = C_{1F} + C_{2F}$) is required, resulting in less board space.

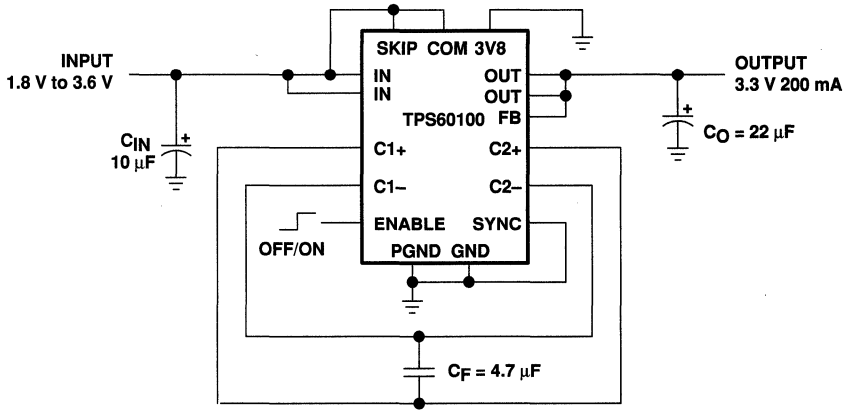


Figure 31. Typical Operating Circuit TPS60100 in Single-Ended Operating Mode

Table 2. Tradeoffs Between Operating Modes

FEATURE	PUSH-PULL MODE (COM = Low)	SINGLE-ENDED MODE (COM = High)
Output ripple amplitude	Small amplitude	Large amplitude
Smallest board space		X

regulated 3.3 V operating mode

In regulated 3.3 V operating mode (3V8 = low) the device provides a regulated 3.3-V output from a1.8-V to 3.6-V input. 3V8 is a logic input and should not remain floating. The typical operating circuit of the TPS60100 in (3.3 V) regulated mode is shown in Figure 1 and Figure 30.

pre-regulated 3.8 V operating mode

When 3V8 is high, the device provides a preregulated 3.8-V output from a 2.2-V to 3.6-V input. This mode should be used if a tighter output voltage tolerance is a major concern. In this case the charge pump generates the input voltage for a low-dropout regulator.

detailed description (continued)

shutdown

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05-μA (1-μA max) of supply current in this mode. Leakage current drawn from the output is as low as 1 μA max. The device exits shutdown once ENABLE is set high level. The typical no-load shutdown exit time is 10 μs. When the device is in shutdown, the load is isolated from the input and the output is high impedance.

external clock signal

If the device shall operate at a user defined frequency, an external clock signal can be used. Therefore, SYNC needs to be connected to IN and the external oscillator signal can drive 3V8. The maximum external frequency is limited to 800 kHz. The switching frequency of the converter is half of the external oscillator frequency. It is recommended to operate the charge pump in constant-frequency mode if an external clock signal is used so that the output noise contains only well-defined frequency components.

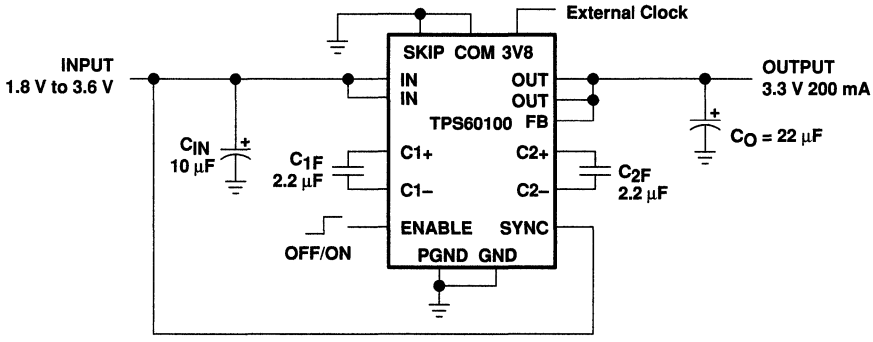


Figure 32. Typical Operating Circuit TPS60100 With External Synchronization

undervoltage lockout

The TPS60100 has an undervoltage lockout feature that deactivates the device and places it in shutdown mode when the input voltage falls below 1.6 V.

APPLICATION INFORMATION

capacitor selection

The TPS60100 requires only four external capacitors as shown in the basic application circuit. Their values are closely linked to the output current capacity, output noise requirements, and mode of operation. Generally, the transfer capacitors (C_{xF}) will be the smallest.

The input capacitor improves system efficiency by reducing the input impedance and stabilizes the input current. C_{IN} is recommended to be about two to four times as large as C_{xF}.

The output capacitor (C_O) can be selected from 5-times to 50-times larger than C_{xF}, depending on the mode of operation and ripple tolerance†. Tables 3 and 4 show capacitor values recommended for low quiescent-current operation (pulse-skip mode) and for low output voltage ripple operation (constant-frequency mode). A recommendation is given for smallest size.

Table 3. Recommended Capacitor Values for Low Quiescent-Current Operation† (pulse-skip mode)

V_{IN} [V]	I_O [mA]	C_{IN} [µF]		C_{xF} [µF]	C_O [µF]		OUTPUT VOLTAGE RIPPLE V_{PP} [mV]
		TANTALUM	CERAMIC		TANTALUM	CERAMIC	
2.4	150	10		2.2	22		90
2.4	150		10 (X5R)	2.2		22 (X5R)	45
2.4	200	10		2.2	22		55
2.4	200		10 (X5R)	2.2		22 (X5R)	30

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

Table 4. Recommended Capacitor Values for Low Output Voltage Ripple Operation† (constant-frequency mode)

V_{IN} [V]	I_O [mA]	C_{IN} [µF]		C_{xF} [µF]	C_O [µF]		OUTPUT VOLTAGE RIPPLE V_{PP} [mV]
		TANTALUM	CERAMIC		TANTALUM	CERAMIC	
2.4	150	10		2.2	22		13
2.4	150		10 (X5R)	2.2		22 (X5R)	4
2.4	200	10		2.2	22		15
2.4	200		10 (X5R)	2.2		22 (X5R)	5

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

† In constant-frequency mode always select $C_O \geq 22$ µF

APPLICATION INFORMATION

For the TPS60100, the smallest board space size can be achieved using Sprague's 595D-series tantalum capacitors for input and output. However, with the trend towards high capacitance ceramic capacitors in smaller size packages, these type of capacitors might become competitive in size soon.

Table 5. Recommended Capacitors

MANUFACTURER	PART NUMBER	CAPACITANCE	TYPE
Taiyo Yuden	LMK212BJ105KG–T	1 µF	Ceramic
	LMK212BJ225MG–T	2.2 µF	Ceramic
	JMK316BJ106ML–T	10 µF	Ceramic
	LMK432BJ226MM–T	22 µF	Ceramic
AVX	0805ZC105KAT2A	1 µF	Ceramic
	1206ZC225KAT2A	2.2 µF	Ceramic
	TPSC106025R0500	10 µF	Tantalum
	TPSC226016R0375	22 µF	Tantalum
Sprague	595D106X0010A2T	10 µF	Tantalum
	595D226X06R3A2T	22 µF	Tantalum
	595D226X06R3B2T	22 µF	Tantalum
	595D226X0020C2T	22 µF	Tantalum
Kemet	T494C106M010AS	10 µF	Tantalum
	T494C226M010AS	22 µF	Tantalum

Table 6 lists the manufacturers of recommended capacitors. In most applications surface-mount tantalum capacitors will be the right choice. However, ceramic capacitors will provide the lowest output voltage ripple due to their typically lower ESR.

Table 6. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET
Taiyo Yuden	X7R/X5R ceramic	www.t–yuden.com
AVX	X7R/X5R ceramic TPS–series tantalum	www.avxcorp.com
Sprague	595D–series tantalum 593D–series tantalum	www.vishay.com
Kemet	T494–series tantalum	www.kemet.com

power dissipation

The power dissipated in the TPS60100 depends on output current and is approximated by:

$$P_{DISS} = I_O \times (2\ V_{IN} - V_O) \text{ for } I_Q << I_O$$

P_{DISS} must be less than that allowed by the package rating. See the ratings for 20-PowerPAD™ package power-dissipation limits and deratings.

APPLICATION INFORMATION

layout

All capacitors should be soldered in close proximity to the IC. A PCB layout proposal for a two-layer board is given in Figure 33. Care has been taken to connect both single-ended charge pumps symmetrically to the load to achive optimized output voltage ripple performance. The proposed layout also provides improved thermal performance as the exposed leadframe is soldered to the PCB. The bottom layer of the PCB is a ground plain only. All ground areas on the PCB should be connected. Connect ground areas on top layer to the bottom layer via through hole connections.

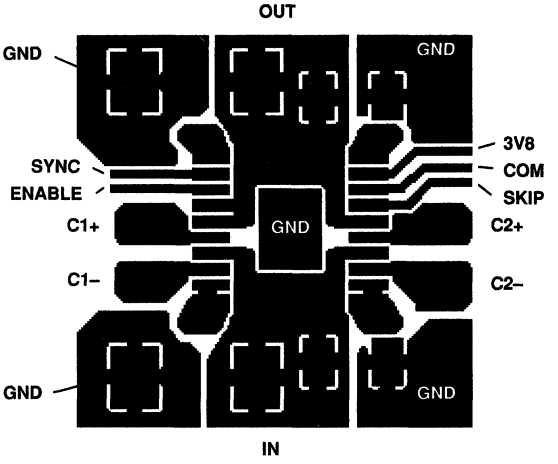


Figure 33. Recommended PCB Layout for TPS60100 (top view)

An evaluation module for the TPS60100 is available and can be ordered under literature code SLVP131 or under product code TPS60100EVM–131.

APPLICATION INFORMATION

applications proposals

paralleling of two TPS60100 to deliver 400 mA

The TPS60100 can be paralleled to yield higher load currents. The circuit of Figure 34 can deliver 400 mA at an output voltage of 3.3 V. It uses two TPS60100 devices in parallel. The devices can share the output capacitors, but each one requires its own transfer capacitors and input capacitor. For best performance, the paralleled devices should operate in the same mode (pulse-skip or constant frequency).

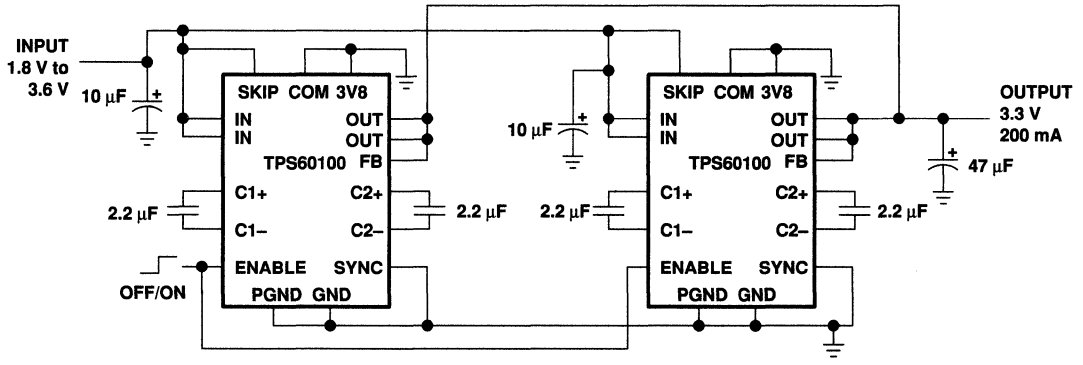


Figure 34. Paralleling of Two TPS60100

TPS60100 with LC output filter for ultra low ripple

For applications where extremely low output ripple is required, a small LC filter is recommended. This is shown in Figure 35. The addition of a small inductor and filter capacitor will reduce the output ripple well below what could be achieved with capacitors alone. The corner frequency of 500 kHz was chosen above the 300 kHz switching frequency to avoid loop stability issues in case the feedback is taken from the output of the LC filter. Leaving the feedback (FB) connection point before the LC filter, the filter capacitance value can be increased to achieve even higher ripple attenuation without affecting stability margin.

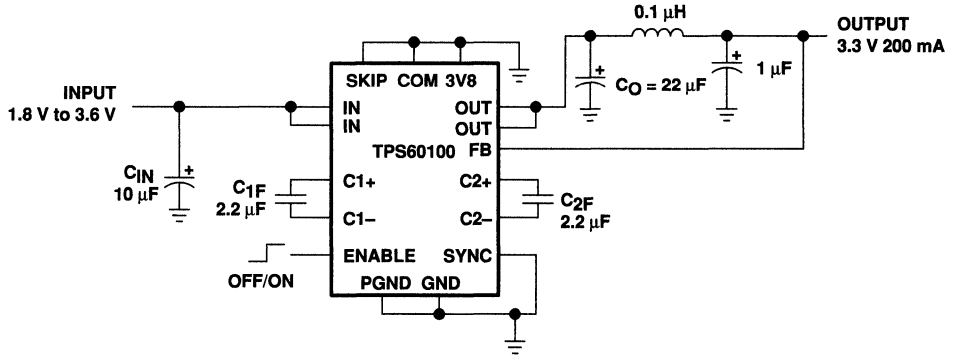


Figure 35. TPS60100 With LC Filter for Ultra Low Output Ripple Applications

APPLICATION INFORMATION

related information

application reports

For more application information see:

- *PowerPAD™ Application Report* (Literature Number: SLMA002)
- *TPS6010x/TPS6011x Charge Pump Application Report* (Literature Number: SLVA070)

device family products

Other devices in this family are:

PART NUMBER	LITERATURE NUMBER	DESCRIPTION
TPS60101	SLVS214	Regulated 3.3-V, 100-mA Low-Noise Charge Pump DC/DC Converter
TPS60110	SLVS215	Regulated 5-V, 300-mA Low-Noise Charge Pump DC/DC Converter
TPS60111	SLVS216	Regulated 5-V, 150-mA Low-Noise Charge Pump DC/DC Converter

features

- Up to 100-mA Output Current
- Less Than 5-mV$_{pp}$ Output Voltage Ripple
- No Inductors Required/Low EMI
- Regulated 3.3-V ±4% Output
- Only Four External Components Required
- Up to 90% Efficiency
- 1.8-V to 3.6-V Input Voltage Range
- 50-µA Quiescent Supply Current
- 0.05-µA Shutdown Current
- Load Isolated in Shutdown
- Space-Saving Thermally-Enhanced TSSOP PowerPAD™ Package
- Evaluation Module Available (TPS60100EVM–131)

description

The TPS60101 step-up, regulated charge pump generates a 3.3-V ±4% output voltage from a 1.8-V to 3.6-V input voltage (two alkaline, NiCd, or NiMH batteries). Output current is 100 mA from a 2-V input. Only four external capacitors are needed to build a complete low-noise dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple as current is continuously transferred to the output. From a 2-V input, the TPS60101 can start into full load with loads as low as 33 Ω.

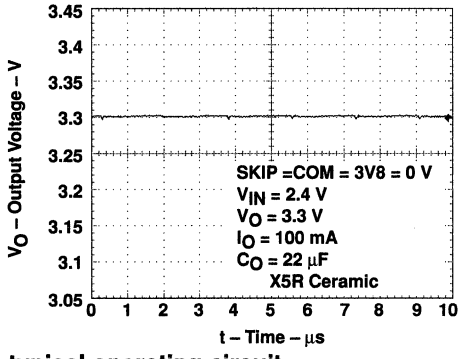
The TPS60101 features either constant frequency mode to minimize noise and output voltage ripple or the power-saving pulse-skip mode to extend battery life at light loads. The TPS60101 switching frequency is 300 kHz. The logic shutdown function reduces the supply current to 1-µA (max) and disconnects the load from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during start-up. This DC/DC converter requires no inductors and has low EMI. It is available in the small 20-pin TSSOP PowerPAD™ package (PWP).

applications

Replaces DC/DC Converters With Inductors in

- Battery-Powered Applications
- Two Battery Cells to 3.3-V Conversion
- Portable Instruments
- Battery-Powered Microprocessor and DSP Systems
- Miniature Equipment
- Backup-Battery Boost Converters
- PDAs
- Laptops
- Handheld Instrumentation
- Medical Instruments
- Cordless Phones

output voltage ripple



typical operating circuit

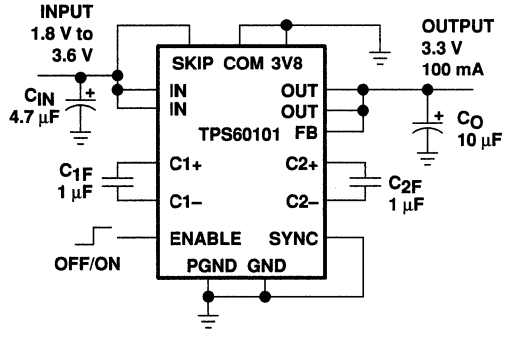
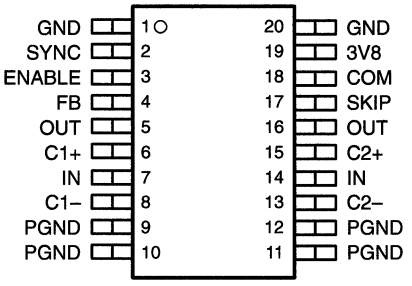


Figure 1

PowerPAD is a trademark of Texas Instruments Incorporated.

PWP PACKAGE
(TOP VIEW)



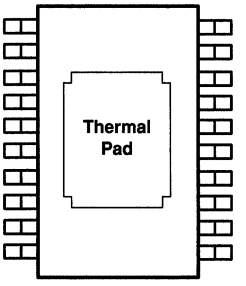


Figure 2. Bottom View of PWP Package, Showing the Thermal Pad

AVAILABLE OPTIONS

PACKAGE
TSSOP† (PWP)
TPS60101PWP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TPS60101PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3V8	19	I	Mode selection. When 3V8 is logic low the charge pump operates in the regulated 3.3-V mode. When 3V8 is connected to IN the regulator operates in preregulated 3.8-V mode.
C1+	6		Positive terminal of the charge-pump capacitor C_{1F}
C1–	8		Negative terminal of the charge-pump capacitor C_{1F}
C2+	15		Positive terminal of the charge-pump capacitor C_{2F}
C2–	13		Negative terminal of the charge-pump capacitor C_{2F}
COM	18	I	Mode selection. When COM is logic low the charge pump operates in push-pull mode to minimize output ripple. When COM is connected to IN the regulator operates in single-ended mode requiring only one flying capacitor.
ENABLE	3	I	ENABLE Input. The device turns off, the output disconnects from the input, and the supply current decreases to 0.05 µA when ENABLE is a logic low. Connect ENABLE to IN for normal operation.
FB	4	I	FEEDBACK input. Connect FB to OUT as close to the load as possible to achieve best regulation. Resistive divider is on chip to match internal reference voltage of 1.22 V.
GND	1, 20		GROUND. Analog ground for internal reference and control circuitry. Connect to PGND through a short trace.
IN	7, 14	I	Supply Input. Connect to an input supply in the 1.8-V to 3.6-V range. Bypass IN to GND with a (C_O/2) µF capacitor. Connect both INs through a short trace.
OUT	5, 16	O	Regulated power output. Connect both OUTs through a short trace and bypass OUT to GND with the output filter capacitor C_O. V_O = 3.3 V when 3V8 = low and V_O = 3.8 V when 3V8 = high.
PGND	9–12		PGND power ground. Charge-pump current flows through this pin. Connect all PGNDs together.
SKIP	17	I	Mode selection. When SKIP is logic low, the charge pump operates in constant-frequency mode. Output ripple and noise are minimized in this mode. When SKIP is connect to IN, the device operates in pulse skip mode. Quiescent current is lowest in this mode.
SYNC	2	I	Selection for external clock signal. Connect to GND to use the internally generated clock signal. Connect to IN for external synchronization. In this case, the clock signal needs to be fed through 3V8 and the device operates in the regulated 3.3-V mode.

absolute maximum ratings (unless otherwise noted)†‡

Input voltage range, V_I (IN, OUT, ENABLE, SKIP, COM, 3V8, FB, SYNC) ..... –0.3 V to 5.5 V
Differential input voltage, V_{ID} (C1+, C2+ to GND) ..... –0.3 V to (V_{OUT} + 0.3 V)
Differential input voltage, V_{ID} (C1–, C2– to GND) ..... –0.3 V to (V_{IN} + 0.3 V)
Continuous total power dissipation ..... See Dissipation Rating Tables
Continuous output current ..... 150 mA
Storage temperature range, T_{stg} ..... –55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10s ..... 260°C
Maximum junction temperature, T_J ..... 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ V_{ENABLE}, V_{SKIP}, V_{COM}, V_{3V8} and V_{SYNC} can exceed V_{IN} up to the maximum rated voltage without increasing the leakage current drawn by these mode select inputs.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	700 mW	5.6 mW/°C	448 mW	364 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)

PACKAGE	$T_C \le 62.5°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING
PWP	25 W	285.7 mW/°C	22.9 W	18.5 W

DISSIPATION DERATING CURVE§ vs FREE-AIR TEMPERATURE

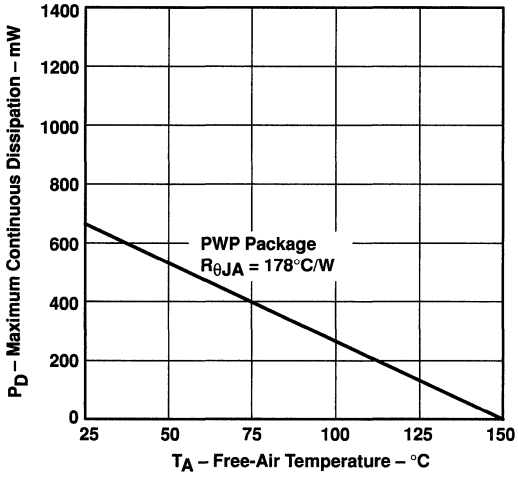


Figure 3

MAXIMUM CONTINUOUS DISSIPATION§ vs CASE TEMPERATURE

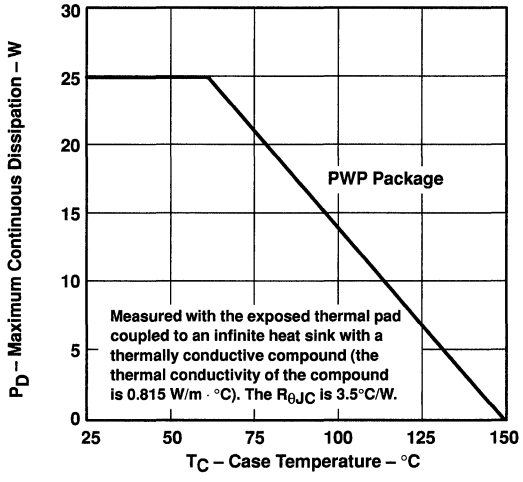


Figure 4

§ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. It is recommended not to exceed a junction temperature of 125°C.

electrical characteristics at C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF†, C_O = 22 µF, T_C = –40°C to 85°C, V_{IN} = 2 V, V_{FB} = V_O, V_{ENABLE} = V_{IN}, V_{SKIP} = V_{IN} or 0 V and V_{COM} = V_{3V8} = V_{SYNC} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.8		3.6	V
$V_{IN(UV)}$	Input undervoltage lockout threshold				1.6	1.8	V
$I_{O(MAX)}$	Maximum output current			100			mA
V_O	Output voltage	1.8 V < V_{IN} < 2 V, $V_{O(Start-Up)}$ = 3.3 V,	0 < I_O < 50 mA, T_C = 25°C	3.17	3.3	3.43	V
		2 V < V_{IN} < 3.3 V,	0 < I_O < 100 mA	3.17	3.3	3.43	
		3.3 V < V_{IN} < 3.6 V,	0 < I_O < 100 mA	3.17	3.3	3.47	
$V_{O(RIP)}$	Output voltage ripple	I_O = 100 mA,	V_{SKIP} = 0 V		5‡		mV_{PP}
$I_{O(LEAK)}$	Output leakage current	V_{IN} = 2.4 V,	V_{ENABLE} = 0 V			1	µA
I_Q	Quiescent current (no-load input current)	V_{SKIP} = V_{IN} = 2.4 V			50	90	µA
		V_{SKIP} = 0 V,	V_{IN} = 2.4 V		1.5		mA
$I_{DD(SDN)}$	Shutdown supply current	V_{IN} = 2.4 V,	V_{ENABLE} = 0 V		0.05	1	µA
$f_{OSC(int)}$	Internal switching frequency	V_{IN} = 2.4 V		200	300	400	kHz
$f_{OSC(ext)}$	External clock frequency	V_{SYNC} = V_{IN},	V_{IN} = 1.8V to 3.6 V	400	600	800	kHz
	External clock duty cycle	V_{SYNC} = V_{IN},	V_{IN} = 1.8V to 3.6 V	20%		80%	
	Efficiency	I_O = 50 mA			80%		
V_{INL}	Input voltage low, ENABLE, SKIP, COM, 3V8, SYNC	V_{IN} = 1.8 V				0.3 × V_{IN}	V
V_{INH}	Input voltage high, ENABLE, SKIP, COM, 3V8, SYNC	V_{IN} = 3.6 V		0.7 × V_{IN}			V
$I_{I(LEAK)}$	Input leakage current, ENABLE, SKIP, COM, 3V8, SYNC	V_{ENABLE} = V_{SKIP} = V_{COM} = V_{3V8} = V_{SYNC} = V_{GND} or V_{IN}			0.01	0.1	µA
	Output load regulation	V_O = 3.3 V, T_C = 25°C	1 mA < I_O < 100 mA		0.004		%/mA
	Output line regulation	2 V < V_{IN} < 3.3 V, I_O = 50 mA,	V_O = 3.3 V, T_C = 25°C		0.6		%/V
	Short circuit current	V_{IN} = 2.4 V T_C = 25°C	V_O = 0 V,		125		mA

† Use only ceramic capacitors with X5R or X7R dielectric as flying capacitors.
‡ Achieved with C_O = 22 µF X5R dielectric ceramic capacitor

electrical characteristics for preregulated 3.8-V Mode ($V_{(3V8)}$ = V_{IN}), at C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF†, C_O = 22 µF, T_C = –40°C to 85°C, V_{IN} = 2.4 V, V_{FB} = V_O, V_{ENABLE} = V_{IN}, V_{SKIP} = V_{IN} or 0 V and V_{COM} = V_{SYNC} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2.2		3.6	V
$I_{O(MAX)}$	Maximum output current		100			mA
V_O	Output voltage	2.2 V < V_{IN} < 3.6 V, 0 < I_O < 100 mA	3.6	3.8	4	V
$I_{O(LEAK)}$	Output leakage current	V_{ENABLE} = 0 V			1	µA
I_Q	Quiescent current (no-load input current)	V_{SKIP} = V_{IN}		60		µA
		V_{SKIP} = 0 V		2		mA
$I_{DD(SDN)}$	Shutdown supply current	V_{ENABLE} = 0 V		0.05	1	µA
f_{OSC}	Internal switching frequency		200	300	400	kHz
	Short circuit current	V_O = 0 V, T_C = 25°C		125		mA

† Use only ceramic capacitors with X5R or X7R dielectric as flying capacitors.

TYPICAL CHARACTERISTICS†

EFFICIENCY
vs
OUTPUT CURRENT (V_O = 3.3 V)

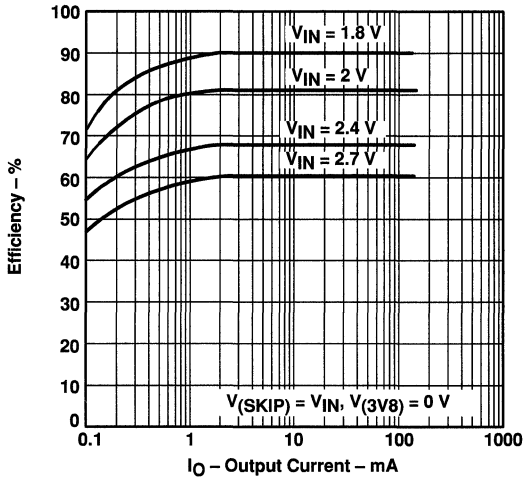


Figure 5

EFFICIENCY
vs
OUTPUT CURRENT (V_O = 3.3 V)

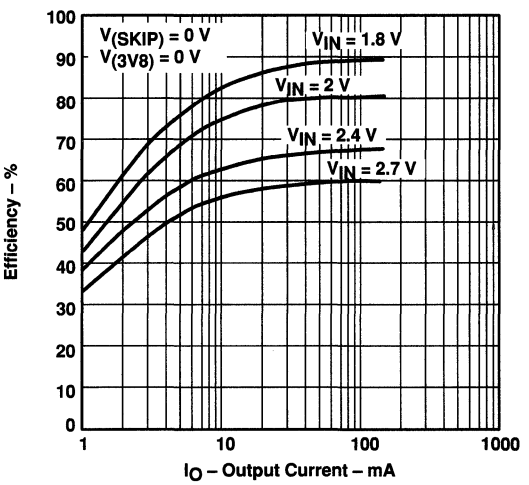


Figure 6

EFFICIENCY
vs
OUTPUT CURRENT (V_O = 3.8 V)

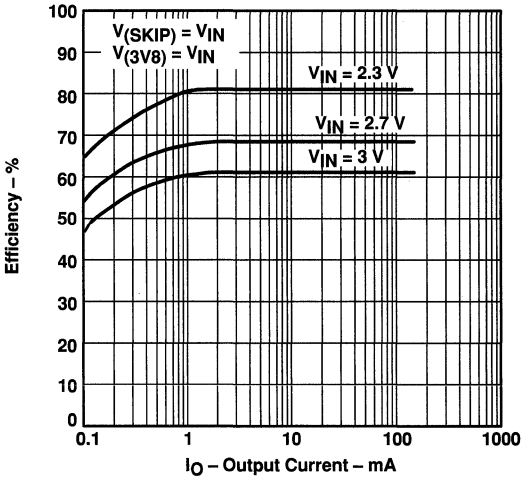


Figure 7

EFFICIENCY
vs
OUTPUT CURRENT (V_O = 3.8 V)

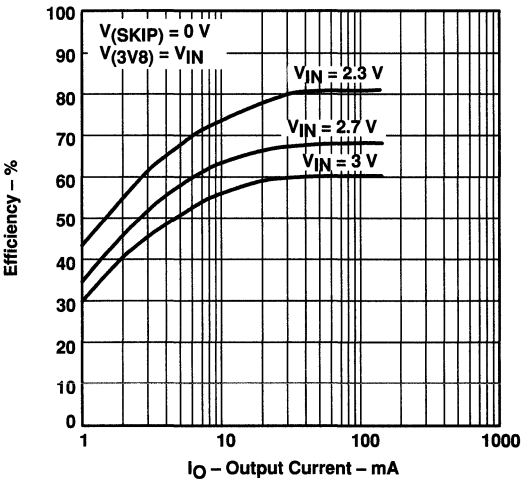


Figure 8

† T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 22 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

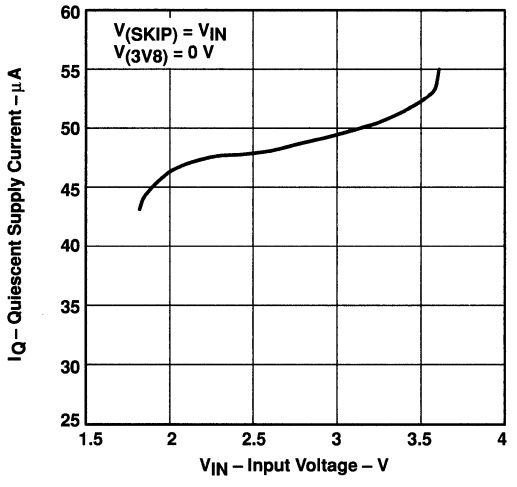


Figure 9

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

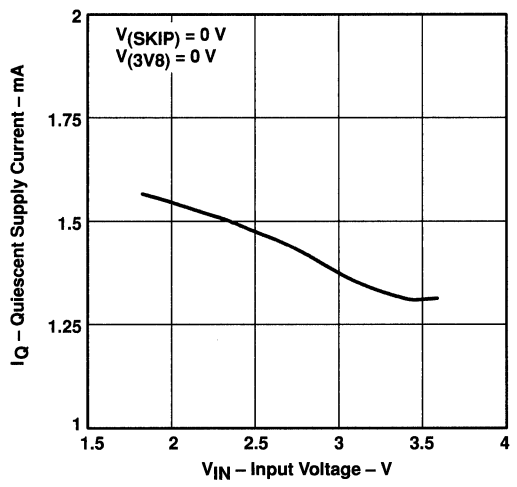


Figure 10

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

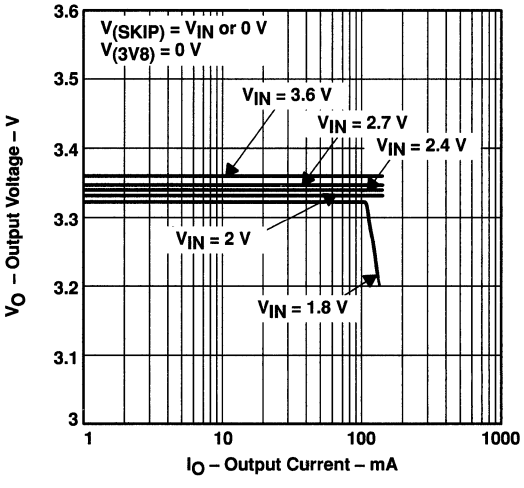


Figure 11

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

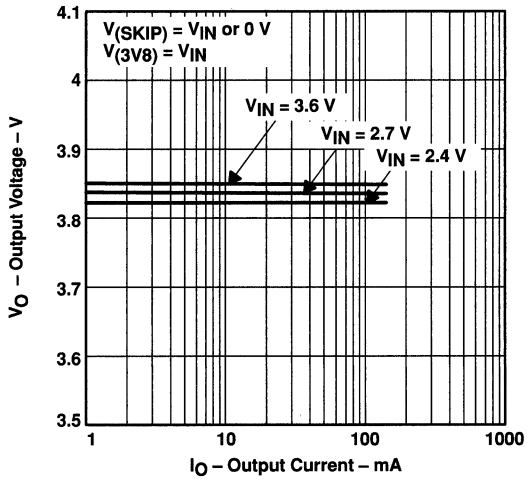


Figure 12

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 22 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

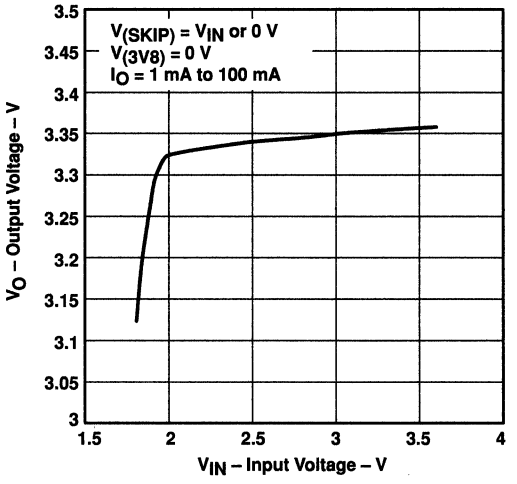


Figure 13

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

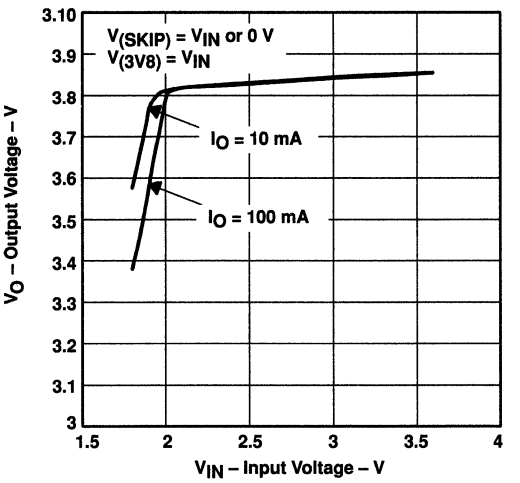


Figure 14

OUTPUT VOLTAGE
vs
TIME

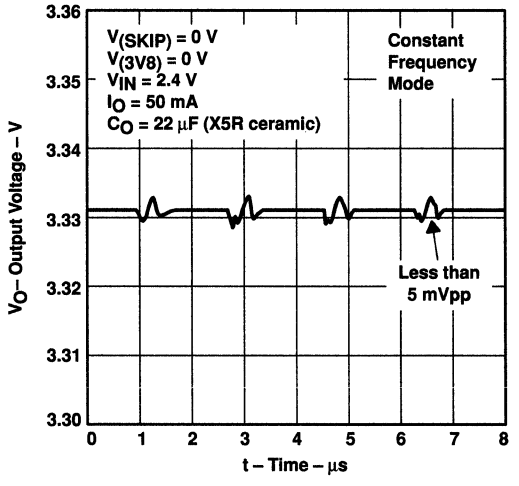


Figure 15

OUTPUT VOLTAGE
vs
TIME

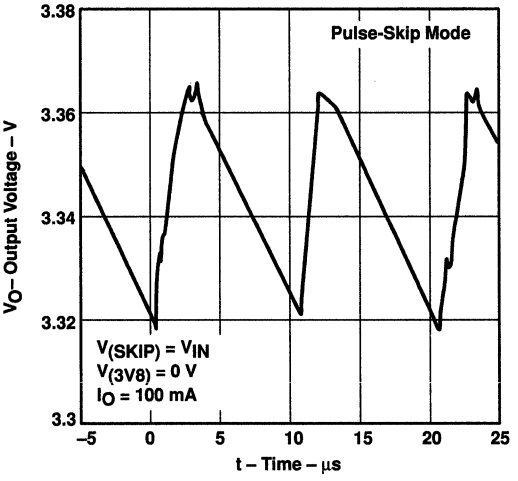


Figure 16

† T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 22 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

LOAD TRANSIENT RESPONSE

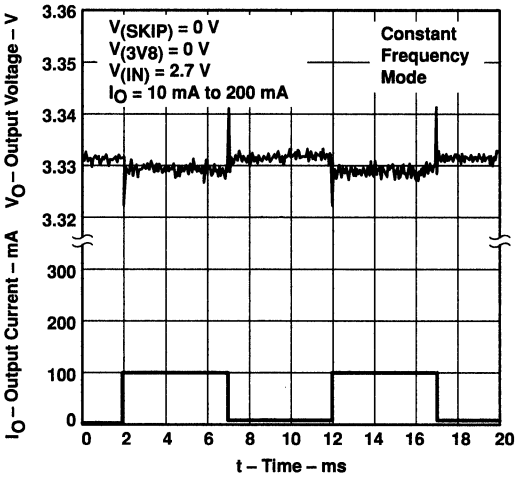


Figure 17

LOAD TRANSIENT RESPONSE

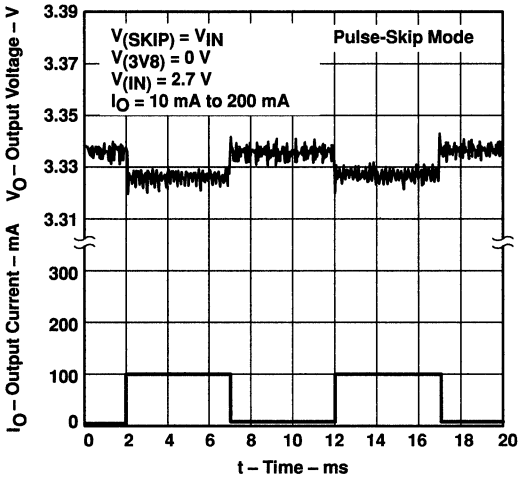


Figure 18

LINE TRANSIENT RESPONSE

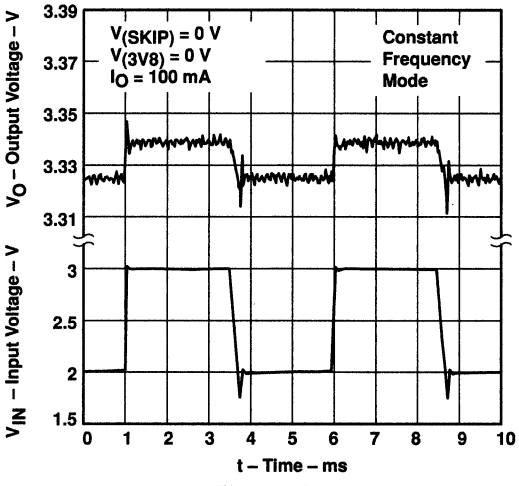


Figure 19

LINE TRANSIENT RESPONSE

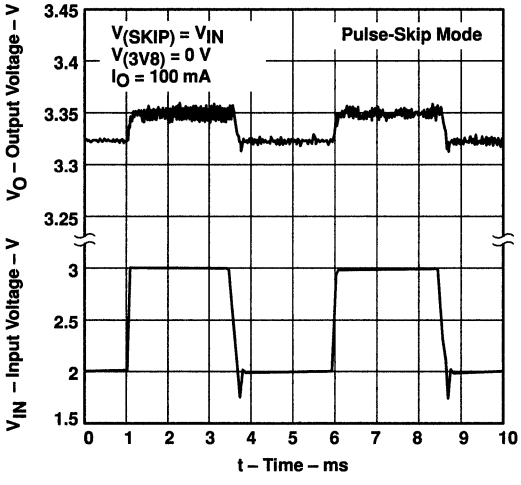


Figure 20

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 22 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

FREQUENCY SPECTRUM
CONSTANT FREQUENCY MODE‡

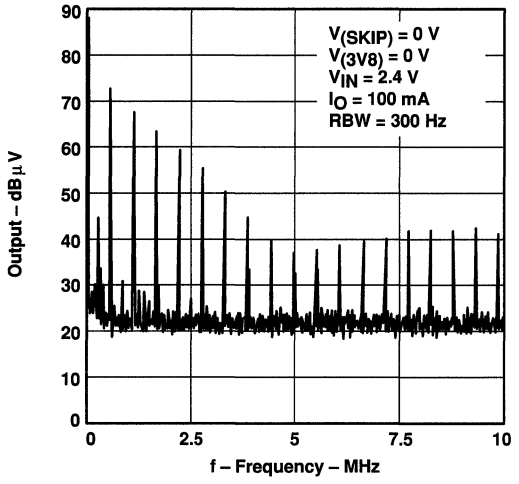


Figure 21

FREQUENCY SPECTRUM
PULSE-SKIP MODE‡

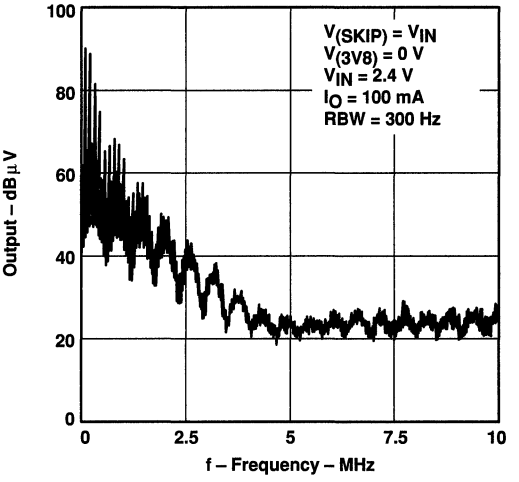


Figure 22

FREQUENCY SPECTRUM
CONSTANT FREQUENCY MODE‡

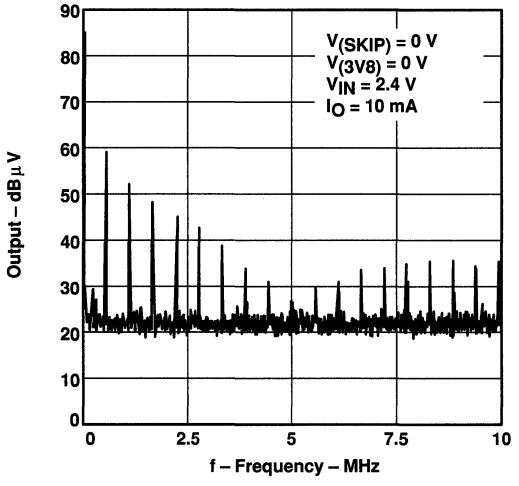


Figure 23

FREQUENCY SPECTRUM
PULSE-SKIP MODE‡

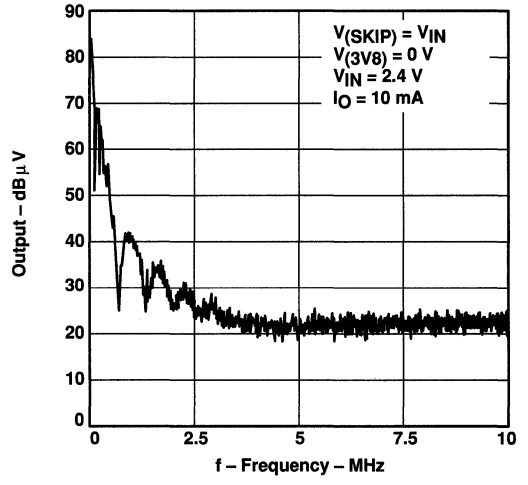


Figure 24

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 μF, C_{1F} = C_{2F} = 2.2 μF, C_O = 22 μF, unless otherwise noted
‡Test circuit: TPS60100EVM–131 with TPS60101

TYPICAL CHARACTERISTICS†

EFFICIENCY
vs
INPUT VOLTAGE

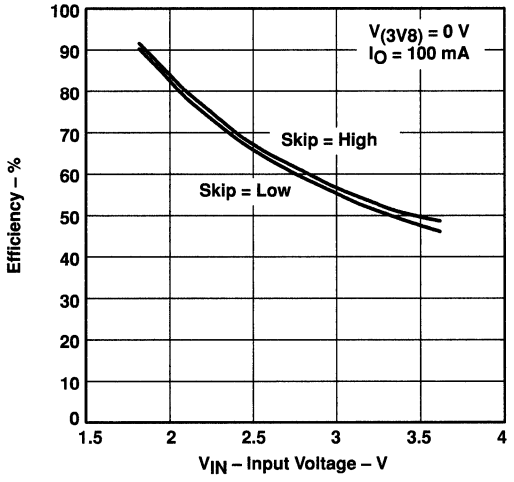


Figure 25

EFFICIENCY
vs
INPUT VOLTAGE

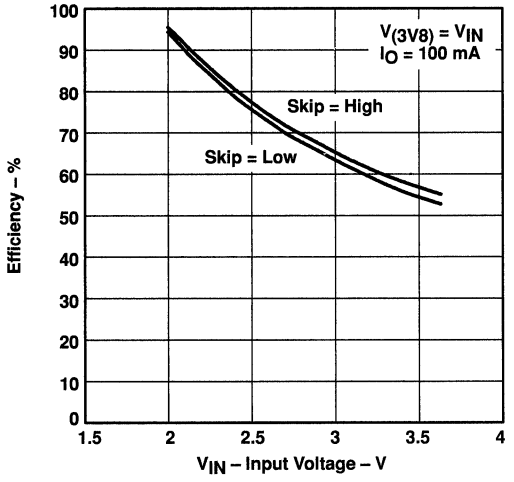


Figure 26

START-UP TIMING

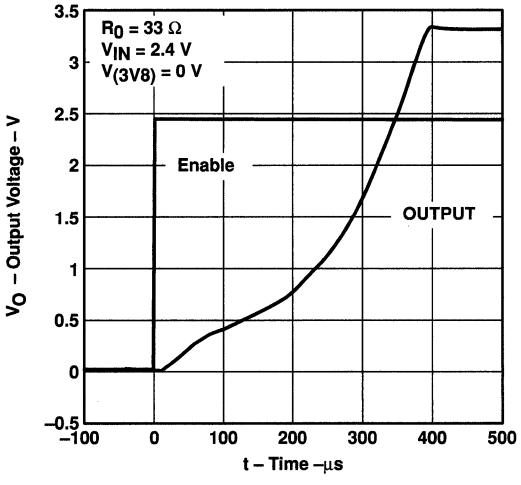


Figure 27

START-UP TIMING

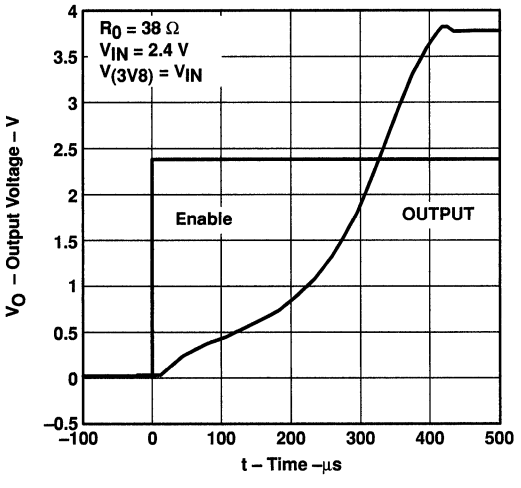


Figure 28

† T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 10 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 22 µF, unless otherwise noted

detailed description

operating principle

The TPS60101 charge pump provides a regulated 3.3-V output from a 1.8-V to 3.6-V input. It delivers a maximum load current of 100 mA. Designed specifically for space critical battery powered applications, the complete charge pump circuit requires only four external capacitors. The circuit can be optimized for highest efficiency at light loads or lowest output noise. The TPS60101 consists of an oscillator, a 1.22-V bandgap reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (Figure 29)

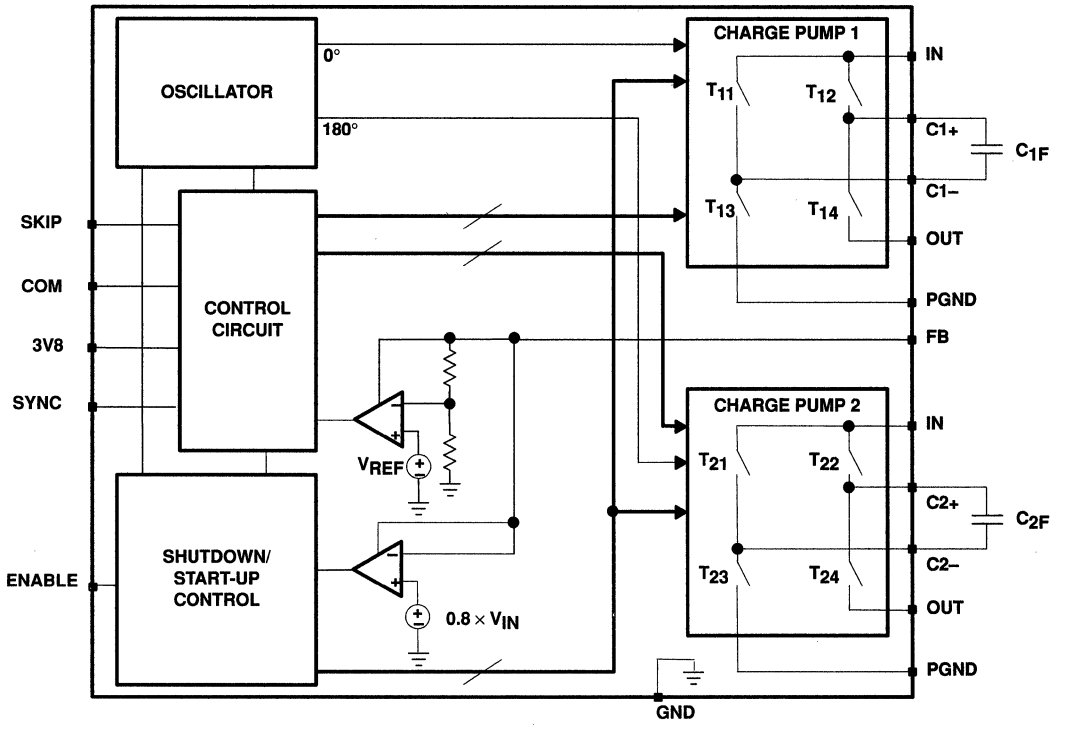


Figure 29. Functional Block Diagram TPS60101

The oscillator runs at a 50% duty cycle. The device consists of two single-ended charge pumps which operate with 180° phase shift. Each single ended charge pump transfers charge into its transfer capacitor (C_{xF}) in one half of the period. During the other half of the period (transfer phase), C_{xF} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name doubler). In order to provide a regulated fixed output voltage of 3.3 V, the TPS60101 uses either pulse-skip mode or constant-frequency mode. Pulse-skip mode and constant-frequency mode are externally selected via the SKIP input pin.

detailed description (continued)

start-up procedure

During start-up, i.e. when ENABLE is set from logic low to logic high, the switches T12 and T14 (charge pump 1), and the switches T22 and T24 (charge pump 2) are conducting to charge up the output capacitor until the output voltage V_O reaches $0.8 \times V_{IN}$. When the start-up comparator detects this limit, the IC begins to operate in the mode selected with SKIP, COM and 3V8. This start-up charging of the output capacitor guarantees a short start-up time and eliminates the need for a Schottky diode between IN and OUT.

pulse-skip mode

In pulse-skip mode (SKIP = high), the error amplifier disables switching of the power stages when it detects an output higher than 3.3 V. The oscillator halts. The IC then skips switching cycles until the output voltage drops below 3.3 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except bandgap reference and error amplifier when the output is higher than 3.3 V. When switching is disabled from the error amplifier, the load is also isolated from the input. SKIP is a logic input and should not remain floating. The typical operating circuit of the TPS60101 in pulse skip mode is shown in Figure 1.

constant-frequency mode

When SKIP is low, the charge pump runs continuously at the frequency f_{OSC}. The control circuit, fed from the error amplifier, controls the charge on C_{1F} and C_{2F} by driving the gates of the FETs T_{12}/T_{13} and T_{22}/T_{23}, respectively. When the output voltage falls, the gate drive increases, resulting in a larger voltage across C_{1F} and C_{2F}. This regulation scheme minimizes output ripple. Since the device switches continuously, the output noise contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads than pulse-skip mode.

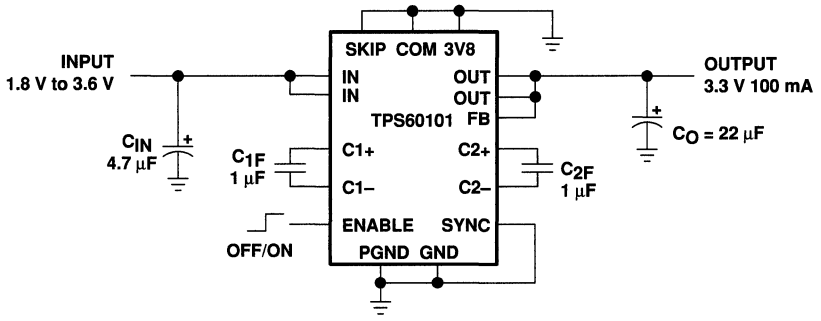


Figure 30. Typical Operating Circuit TPS60101 in Constant Frequency Mode

Table 1. Tradeoffs Between Operating Modes

FEATURE	PULSE-SKIP MODE (SKIP = High)	CONSTANT-FREQUENCY MODE (SKIP = Low)
Best light-load efficiency	X	
Smallest external component size for a given output ripple		X
Output ripple amplitude	Small amplitude	Very small amplitude
Output ripple frequency	Variable	Constant
Load regulation	Very good	Good

NOTE: Even in pulse-skip mode the output ripple amplitude is small if the push-pull operating mode is selected via COM.

detailed description (continued)

push-pull operating mode

In push-pull operating mode (COM = low), the two single-ended charge pumps operate with 180° phase shift. The oscillator signal has a 50% duty cycle. Each single-ended charge pump transfers charge into its transfer capacitor (C_{xF}) in one-half of the period. During the other half of the period (transfer phase), C_{xF} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple. COM is a logic input and should not remain floating. The typical operating circuit of the TPS60101 in push-pull mode is shown in Figure 1 and Figure 30.

single-ended operating mode

When COM is high, the device runs in single-ended operating mode. The two single-ended charge pumps operate in parallel without phase shift. They transfer charge into the transfer capacitor (C_F) in one half of the period. During the other half of the period (transfer phase), C_F is placed in series with the input to transfer its charge to C_O. In single-ended operating mode only one transfer capacitor ($C_F = C_{1F} + C_{2F}$) is required, resulting in less board space.

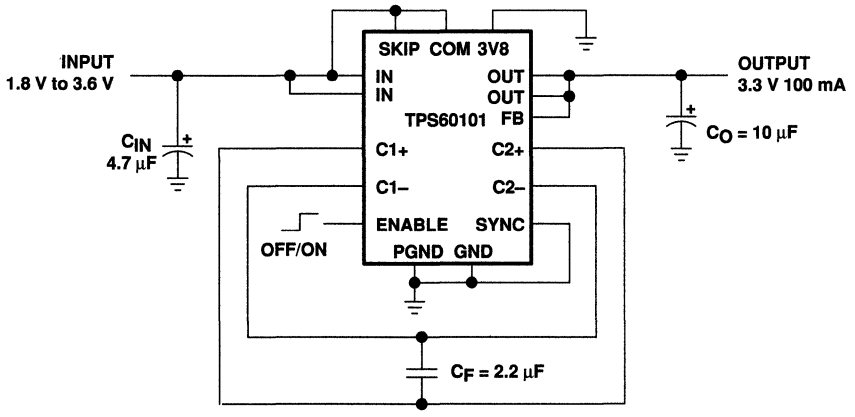


Figure 31. Typical Operating Circuit TPS60101 in Single-Ended Operating Mode

Table 2. Tradeoffs Between Operating Modes

FEATURE	PUSH-PULL MODE (COM = Low)	SINGLE-ENDED MODE (COM = High)
Output ripple amplitude	Small amplitude	Large amplitude
Smallest board space		X

regulated 3.3 V operating mode

In regulated 3.3-V operating mode (3V8 = low) the device provides a regulated 3.3-V output from a1.8-V to 3.6-V input. 3V8 is a logic input and should not remain floating. The typical operating circuit of the TPS60101 in (3.3 V) regulated mode is shown in Figure 1 and Figure 30.

pre-regulated 3.8 V operating mode

When 3V8 is high, the device provides a preregulated 3.8-V output from a 2.2-V to 3.6-V input. This mode should be used if a tighter output voltage tolerance is a major concern. In this case the charge pump generates the input voltage for a low-dropout regulator.

detailed description (continued)

shutdown

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05-μA (1-μA max) of supply current in this mode. Leakage current drawn from the output is as low as 1 μA max. The device exits shutdown once ENABLE is set high level. The typical no-load shutdown exit time is 10 μs. When the device is in shutdown, the load is isolated from the input and the output is high impedance.

external clock signal

If the device operates at a user defined frequency, an external clock signal can be used. Therefore, SYNC needs to be connected to IN and the external oscillator signal can drive 3V8. The maximum external frequency is limited to 800 kHz. The switching frequency of the converter is half of the external oscillator frequency. It is recommended to operate the charge pump in constant-frequency mode if an external clock signal is used so that the output noise contains only well-defined frequency components.

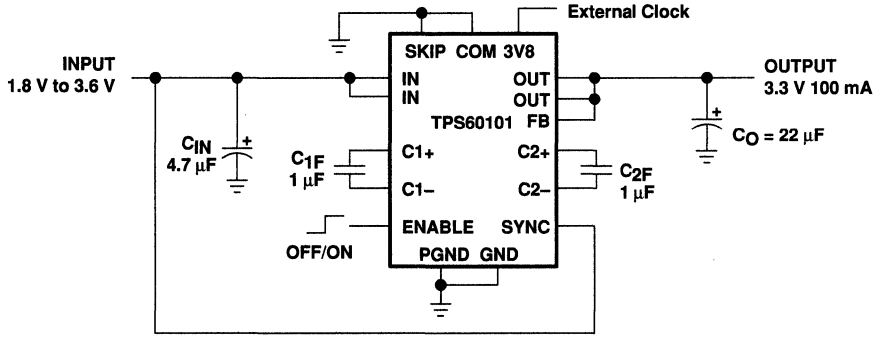


Figure 32. Typical Operating Circuit TPS60101 With External Synchronization

undervoltage lockout

The TPS60101 has an undervoltage lockout feature that deactivates the device and places it in shutdown mode when the input voltage falls below 1.6 V.

APPLICATION INFORMATION

capacitor selection

The TPS60101 requires only four external capacitors as shown in the basic application circuit. Their values are closely linked to the output current capacity, output noise requirements, and mode of operation. Generally, the transfer capacitors (C_{xF}) will be the smallest.

The input capacitor improves system efficiency by reducing the input impedance and stabilizes the input current. C_{IN} is recommended to be about two to four times as large as C_{xF}.

The output capacitor (C_O) can be selected from 5-times to 50-times larger than C_{xF}, depending on the mode of operation and ripple tolerance†. Tables 3 and 4 show capacitor values recommended for low quiescent-current operation (pulse-skip mode) and for low output voltage ripple operation (constant-frequency mode). A recommendation is given for smallest size.

Table 3. Recommended Capacitor Values for Low Quiescent-Current Operation† (pulse-skip mode)

V_{IN} [V]	I_O [mA]	C_{IN} [µF]		C_{xF} [µF]	C_O [µF]		OUTPUT VOLTAGE RIPPLE V_{pp} [mV]
		TANTALUM	CERAMIC		TANTALUM	CERAMIC	
2.4	50	4.7		1	10		135
2.4	50		4.7 (X7R)	1		10 (X5R)	125
2.4	100	4.7		1	10		70
2.4	100		4.7 (X7R)	1		10 (X5R)	65

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

Table 4. Recommended Capacitor Values for Low Output Voltage Ripple Operation† (constant-frequency mode)

V_{IN} [V]	I_O [mA]	C_{IN} [µF]		C_{xF} [µF]	C_O [µF]		OUTPUT VOLTAGE RIPPLE V_{pp} [mV]
		TANTALUM	CERAMIC		TANTALUM	CERAMIC	
2.4	50	4.7		1	22		5
2.4	50		4.7 (X7R)	1		22 (X5R)	3
2.4	100	4.7		1	22		10
2.4	100		4.7 (X7R)	1		22 (X5R)	5

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

† In constant-frequency mode always select $C_O \geq 22$ µF

APPLICATION INFORMATION

For the TPS60101, the smallest board space size can be achieved using Sprague's 595D-series tantalum capacitors for input and output. However, with the trend towards high capacitance ceramic capacitors in smaller size packages, these type of capacitors might become competitive in size soon.

Table 5. Recommended Capacitors

MANUFACTURER	PART NUMBER	CAPACITANCE	TYPE
Taiyo Yuden	LMK212BJ105KG–T	1 µF	Ceramic
	LMK212BJ225MG–T	2.2 µF	Ceramic
	LMK316BJ475KL–T	4.7 µF	Ceramic
	JMK316BJ106ML–T	10 µF	Ceramic
	LMK432BJ226MM–T	22 µF	Ceramic
AVX	0805ZC105KAT2A	1 µF	Ceramic
	1206ZC225KAT2A	2.2 µF	Ceramic
	TPSC475035R0600	4.7 µF	Tantalum
	TPSC106025R0500	10 µF	Tantalum
	TPSC226016R0375	22 µF	Tantalum
Sprague	595D475X0016A2T	4.7 µF	Tantalum
	595D106X0010A2T	10 µF	Tantalum
	595D226X06R3A2T	22 µF	Tantalum
	595D226X06R3B2T	22 µF	Tantalum
	595D226X0020C2T	22 µF	Tantalum
Kemet	T494B475M010AS	4.7 µF	Tantalum
	T494C106M010AS	10 µF	Tantalum
	T494C226M010AS	22 µF	Tantalum

Table 6 lists the manufacturers of recommended capacitors. In most applications surface-mount tantalum capacitors will be the right choice. However, ceramic capacitors will provide the lowest output voltage ripple due to their typically lower ESR.

Table 6. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET
Taiyo Yuden	X7R/X5R ceramic	www.t–yuden.com
AVX	X7R/X5R ceramic TPS–series tantalum	www.avxcorp.com
Sprague	595D–series tantalum 593D–series tantalum	www.vishay.com
Kemet	T494–series tantalum	www.kemet.com

power dissipation

The power dissipated in the TPS60101 depends on output current and is approximated by:

$$P_{DISS} = I_O \times (2\ V_{IN} - V_O) \text{ for } I_Q << I_O$$

P_{DISS} must be less than that allowed by the package rating. See the ratings for 20-PowerPAD™ package power-dissipation limits and deratings.

APPLICATION INFORMATION

layout

All capacitors should be soldered in close proximity to the IC. A PCB layout proposal for a two-layer board is given in Figure 33. Care has been taken to connect both single-ended charge pumps symmetrically to the load to achive optimized output voltage ripple performance. The proposed layout also provides improved thermal performance as the exposed leadframe is soldered to the PCB. The bottom layer of the PCB is a ground plain only. All ground areas on the PCB should be connected. Connect ground areas on top layer to the bottom layer via through hole connections.

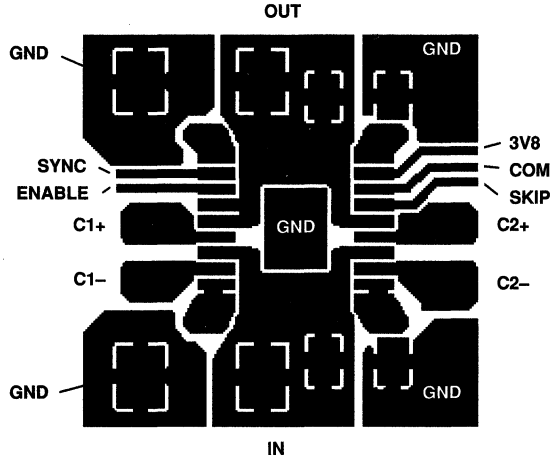


Figure 33. Recommended PCB Layout for TPS60101 (top view)

The evaluation module designed for the TPS60100 can, with slight modifications, be used for evaluation of the TPS60101. The EVM can be ordered under literature code SLVP131 or under product code TPS60100EVM–131.

APPLICATION INFORMATION

applications proposals

TPS60101 with LC output filter for ultra low ripple

For applications where extremely low output ripple is required, a small LC filter is recommended. This is shown in Figure 34. The addition of a small inductor and filter capacitor will reduce the output ripple well below what could be achieved with capacitors alone. The corner frequency of 500 kHz was chosen above the 300 kHz switching frequency to avoid loop stability issues in case the feedback is taken from the output of the LC filter. Leaving the feedback (FB) connection point before the LC filter, the filter capacitance value can be increased to achieve even higher ripple attenuation without affecting stability margin.

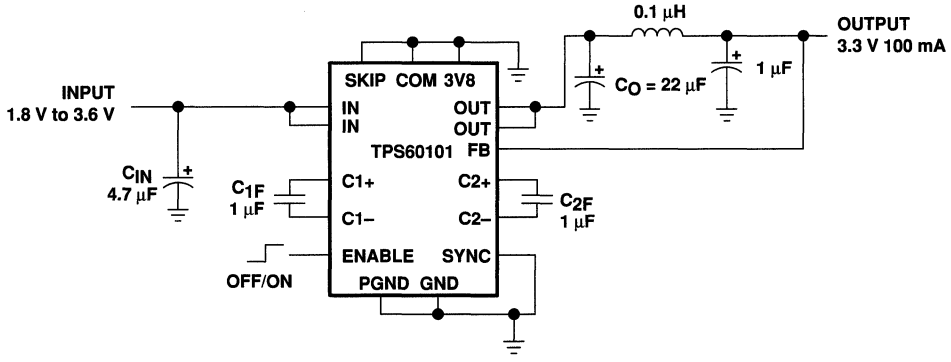


Figure 34. TPS60101 With LC Filter for Ultra Low Output Ripple Applications

related information

application reports

For more application information see:

- *PowerPAD™ Application Report* (Literature Number: SLMA002)
- *TPS6010x/TPS6011x Charge Pump Application Report* (Literature Number: SLVA070)

device family products

Other devices in this family are:

PART NUMBER	LITERATURE NUMBER	DESCRIPTION
TPS60100	SLVS213	Regulated 3.3-V, 200-mA Low-Noise Charge Pump DC/DC Converter
TPS60110	SLVS215	Regulated 5-V, 300-mA Low-Noise Charge Pump DC/DC Converter
TPS60111	SLVS216	Regulated 5-V, 150-mA Low-Noise Charge Pump DC/DC Converter

features

- Up to 300-mA Output Current
- Less Than 10-mV$_{pp}$ Output Voltage Ripple
- No Inductors Required/Low EMI
- Regulated 5-V ±4% Output
- Only Four External Components Required
- Up to 90% Efficiency
- 2.7-V to 5.4-V Input Voltage Range
- 60-μA Quiescent Supply Current
- 0.05-μA Shutdown Current
- Load Isolated in Shutdown
- Space-Saving Thermally-Enhanced TSSOP PowerPAD™ Package
- Evaluation Module Available (TPS60110EVM–132)

description

The TPS60110 step-up, regulated charge pump generates a 5-V ±4% output voltage from a 2.7-V to 5.4-V input voltage (three alkaline, NiCd, or NiMH batteries; or, one lithium or lithium ion battery). Output current is 300 mA from a 3-V input. Only four external capacitors are needed to build a complete low-noise dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple as current is continuously transferred to the output. From a 3-V input, the TPS60110 can start into full load with loads as low as 16 Ω.

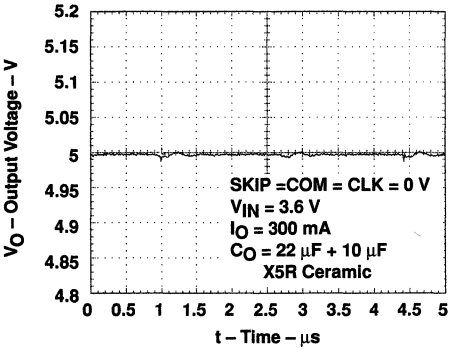
The TPS60110 features either constant frequency mode to minimize noise and output voltage ripple or the power-saving pulse-skip mode to extend battery life at light loads. The TPS60110 switching frequency is 300 kHz. The logic shutdown function reduces the supply current to 1-μA (max) and disconnects the load from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during start-up. This dc/dc converter requires no inductors and has low EMI. It is available in the small 20-pin TSSOP PowerPAD™ package (PWP).

applications

Replaces DC/DC Converters With Inductors in

- Battery-Powered Applications
- Li-Ion Battery to 5-V Conversion
- Portable Instruments
- Battery-Powered Microprocessor Systems
- Miniature Equipment
- Backup-Battery Boost Converters
- PDAs
- Laptops
- Handheld Instrumentation
- Medical Instruments

output voltage ripple



typical operating circuit

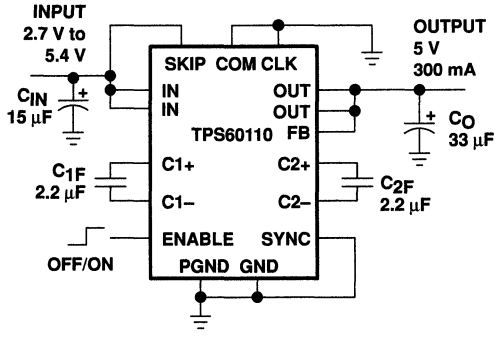
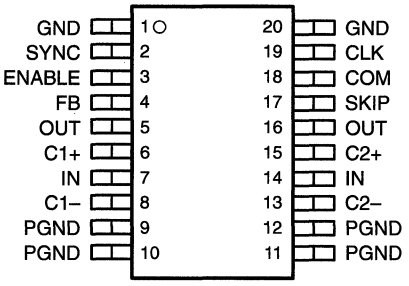


Figure 1

PowerPAD is a trademark of Texas Instruments Incorporated.

PWP PACKAGE
(TOP VIEW)



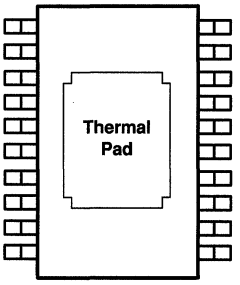


Figure 2. Bottom View of PWP Package, Showing the Thermal Pad

AVAILABLE OPTIONS

PACKAGE
TSSOP† (PWP)
TPS60110PWP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TPS60110PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	19	I	Input for external clock signal. If the internal clock is used, connect this terminal to GND.
C1+	6		Positive terminal of the charge-pump capacitor C_{1F}
C1–	8		Negative terminal of the charge-pump capacitor C_{1F}
C2+	15		Positive terminal of the charge-pump capacitor C_{2F}
C2–	13		Negative terminal of the charge-pump capacitor C_{2F}
COM	18	I	Mode selection. When COM is logic low the charge pump operates in push-pull mode to minimize output ripple. When COM is connected to IN the regulator operates in single-ended mode requiring only one flying capacitor.
ENABLE	3	I	ENABLE Input. The device turns off, the output disconnects from the input, and the supply current decreases to 0.05 µA when ENABLE is a logic low. Connect ENABLE to IN for normal operation.
FB	4	I	FEEDBACK input. Connect FB to OUT as close to the load as possible to achieve best regulation. Resistive divider is on-chip to match internal reference voltage of 1.22 V.
GND	1, 20		GROUND. Analog ground for internal reference and control circuitry. Connect to PGND through a short trace.
IN	7, 14	I	Supply Input. Connect to an input supply in the 2.7-V to 5.4-V range. Bypass IN to GND with a (C_O/2) µF capacitor. Connect both INs through a short trace.
OUT	5, 16	O	Regulated 5-V power output. Connect both OUTs through a short trace and bypass OUT to GND with the output filter capacitor C_O.
PGND	9–12		PGND power ground. Charge-pump current flows through this pin. Connect all PGNDs together.
SKIP	17	I	Mode selection. When SKIP is logic low, the charge pump operates in constant-frequency mode. Output ripple and noise are minimized in this mode. When SKIP is connect to IN, the device operates in pulse skip mode. Quiescent current is lowest in this mode.
SYNC	2	I	Selection for external clock signal. Connect to GND to use the internally generated clock signal. Connect to IN for external synchronization. In this case, the clock signal needs to be fed through CLK.

absolute maximum ratings (unless otherwise noted)†‡

Input voltage range, V_I (IN, OUT, ENABLE, SKIP, COM, CLK, FB, SYNC) ..... –0.3 V to 5.5 V
Differential input voltage, V_{ID} (C1+, C2+ to GND) ..... –0.3 V to (V_O + 0.3 V)
Differential input voltage, V_{ID} (C1–, C2– to GND) ..... –0.3 V to (V_{IN} + 0.3 V)
Continuous total power dissipation ..... See Dissipation Rating Tables
Continuous output current ..... 400 mA
Storage temperature range, T_{stg} ..... –55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10s ..... 260°C
Maximum junction temperature, T_J ..... 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ V_{ENABLE}, V_{SKIP}, V_{COM}, V_{CLK} and V_{SYNC} can exceed V_{IN} up to the maximum rated voltage without increasing the leakage current drawn by these mode select inputs.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	700 mW	5.6 mW/°C	448 mW	364 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)

PACKAGE	$T_C \le 62.5°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING
PWP	25 W	285.7 mW/°C	22.9 W	18.5 W

DISSIPATION DERATING CURVE§ vs FREE-AIR TEMPERATURE

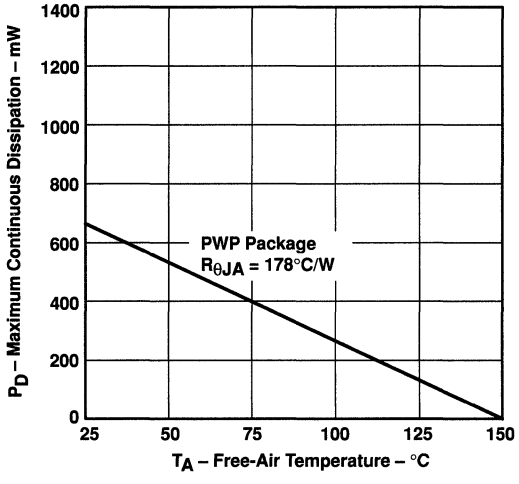


Figure 3

MAXIMUM CONTINUOUS DISSIPATION§ vs CASE TEMPERATURE

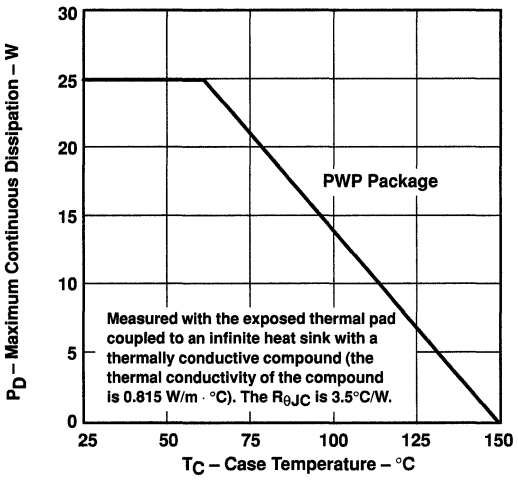


Figure 4

§ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. It is recommended not to exceed a junction temperature of 125°C.

electrical characteristics at C_{IN} = 15 µF, C_{1F} = C_{2F} = 2.2 µF†, C_O = 33 µF, T_C = –40°C to 85°C, V_{IN} = 3 V, V_{FB} = V_O, V_{ENABLE} = V_{IN}, V_{SKIP} = V_{IN} or 0 V and V_{COM} = V_{CLK} = V_{SYNC} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			2.7		5.4	V
$I_{O(MAX)}$	Maximum output current			300			mA
V_O	Output voltage	2.7 V < V_{IN} < 3 V, $V_{O(Start-Up)}$ = 5 V,	0 < I_O < 150 mA, T_C = 25°C	4.8	5	5.2	V
		3 V < V_{IN} < 5 V,	0 < I_O < 300 mA	4.8	5	5.2	
		5 V < V_{IN} < 5.4 V,	0 < I_O < 300 mA	4.8	5	5.25	
$V_{O(RIP)}$	Output voltage ripple	I_O = 300 mA,	V_{SKIP} = 0 V		10‡		mVPP
$I_{O(LEAK)}$	Output leakage current	V_{IN} = 3.6 V,	V_{ENABLE} = 0 V			1	µA
I_Q	Quiescent current (no-load input current)	V_{SKIP} = V_{IN} = 3.6 V			60	90	µA
		V_{SKIP} = 0 V,	V_{IN} = 3.6 V		2.8		mA
$I_{DD(SDN)}$	Shutdown supply current	V_{IN} = 3.6 V,	V_{ENABLE} = 0 V		0.05	1	µA
$f_{OSC(int)}$	Internal switching frequency	V_{IN} = 3.6 V		200	300	400	kHz
$f_{OSC(ext)}$	External clock frequency	V_{SYNC} = V_{IN},	V_{IN} = 2.7 V to 5.4 V	400	600	800	kHz
	External clock duty cycle	V_{SYNC} = V_{IN},	V_{IN}= 2.7V to 5.4 V	20%		80%	
	Efficiency	I_O = 150 mA			80%		
V_{INL}	Input voltage low, ENABLE, SKIP, COM, CLK, SYNC	V_{IN} = 2.7 V				0.3 × V_{IN}	V
V_{INH}	Input voltage high, ENABLE, SKIP, COM, CLK, SYNC	V_{IN} = 5.4 V		0.7 × V_{IN}			V
$I_{I(LEAK)}$	Input leakage current, ENABLE, SKIP, COM, CLK, SYNC	V_{ENABLE} = V_{SKIP} = V_{COM} = V_{CLK} = V_{SYNC} = V_{GND} or V_{IN}			0.01	0.1	µA
	Output load regulation	V_O = 5 V, T_C = 25°C	1 mA < I_O < 300 mA		0.002		%/mA
	Output line regulation	3 V < V_{IN} < 5 V, I_O = 150 mA,	V_O = 5 V, T_C = 25°C		0.6		%/V
	Short circuit current	V_{IN} = 3.6 V T_C = 25°C	V_O = 0 V,		150		mA

† Use only ceramic capacitors with X5R or X7R dielectric as flying capacitors.
‡ Achieved with C_O = 22 µF + 10 µF X5R dielectric ceramic capacitor

TYPICAL CHARACTERISTICS†

EFFICIENCY
vs
OUTPUT CURRENT

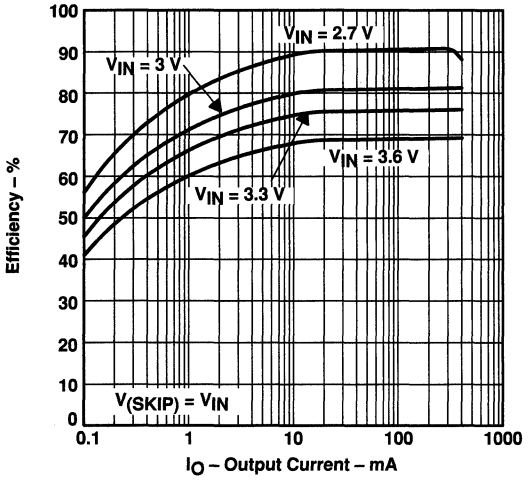


Figure 5

EFFICIENCY
vs
OUTPUT CURRENT

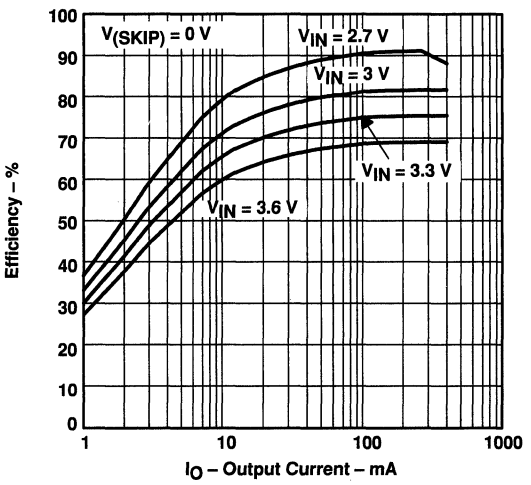


Figure 6

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

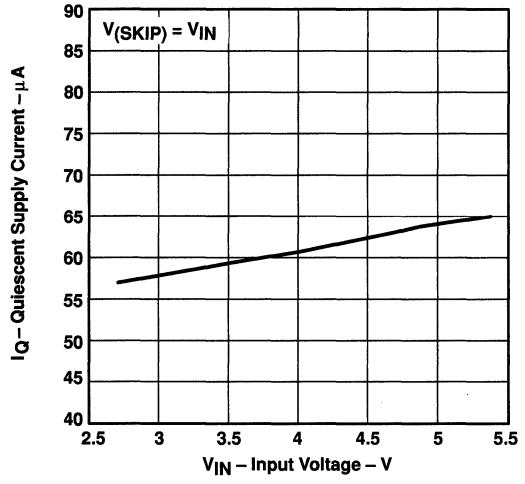


Figure 7

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

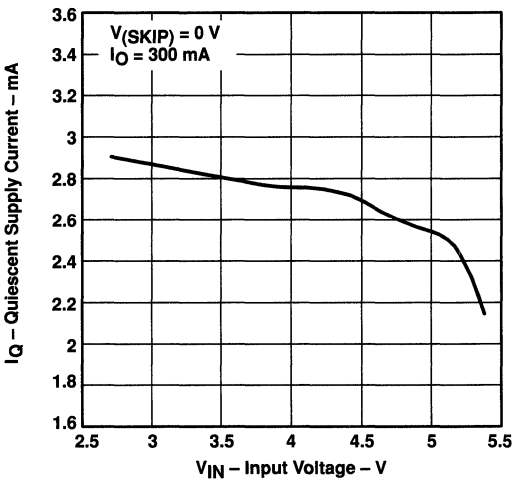


Figure 8

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 33 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

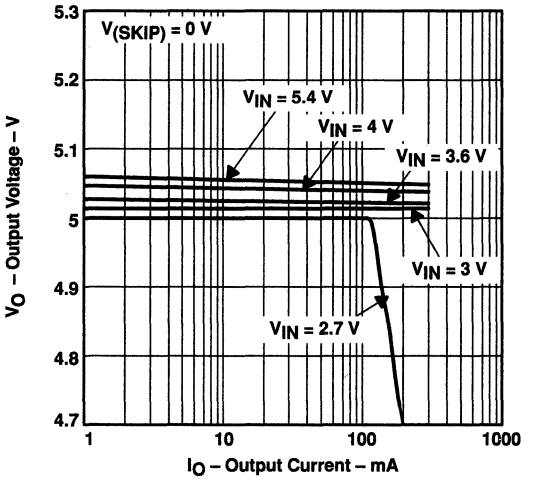


Figure 9

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

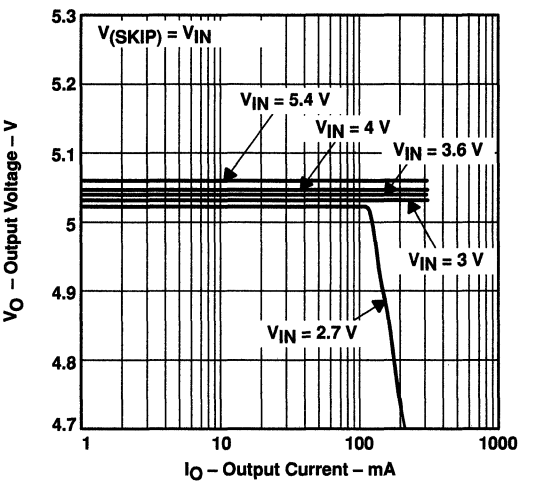


Figure 10

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

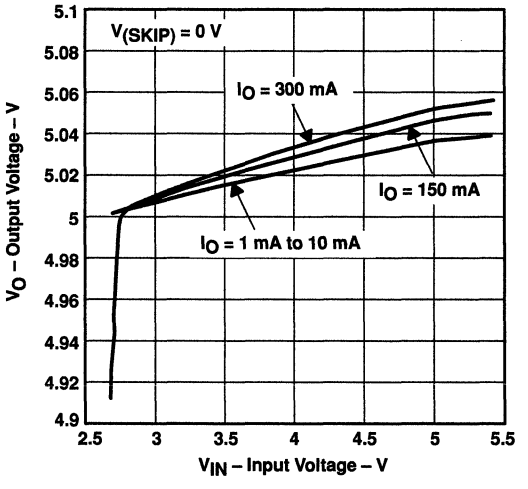


Figure 11

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

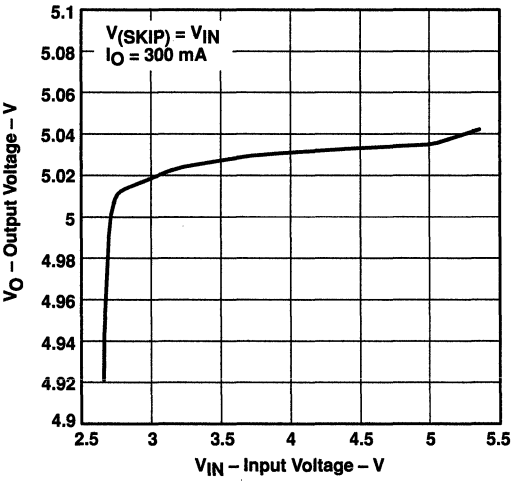


Figure 12

† T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 33 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
TIME

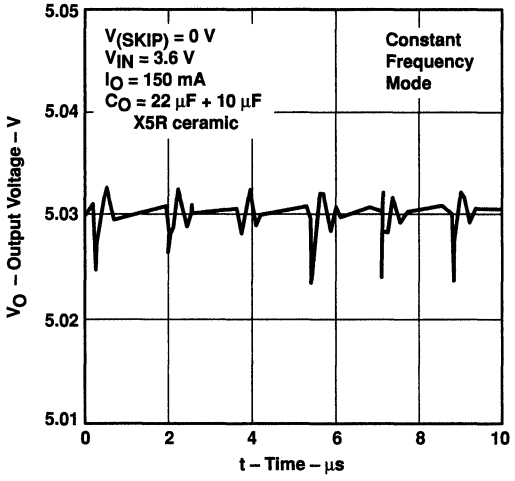


Figure 13

OUTPUT VOLTAGE
vs
TIME

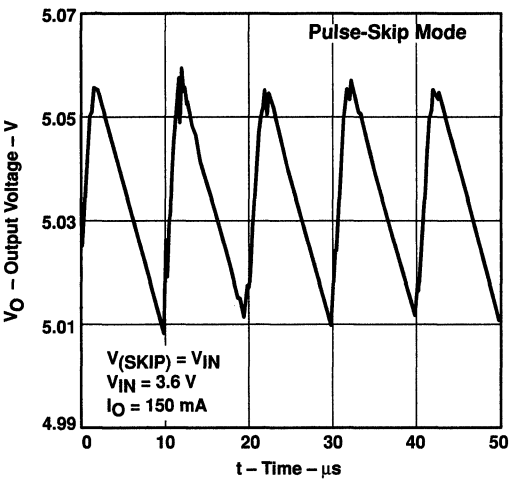


Figure 14

LOAD TRANSIENT RESPONSE

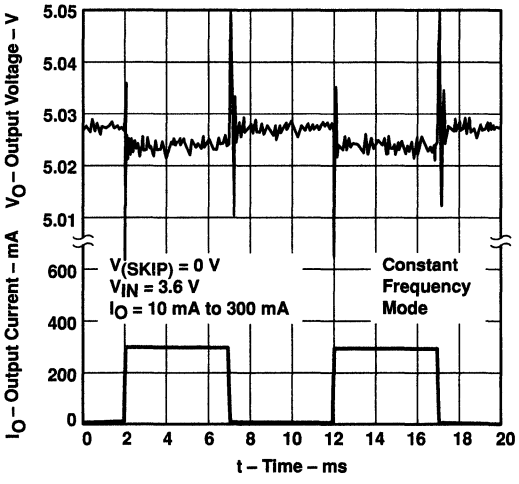


Figure 15

LOAD TRANSIENT RESPONSE

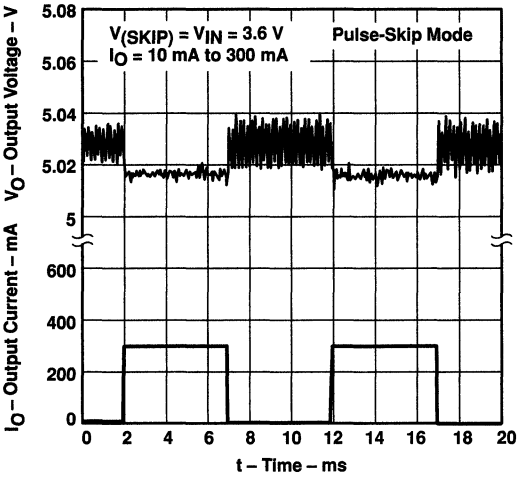


Figure 16

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 µF, C_{1F} = C_{2F} = 2.2 µF, C_O = 33 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

LINE TRANSIENT RESPONSE

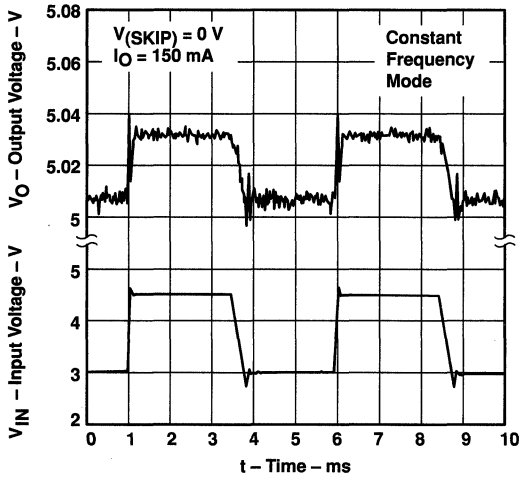


Figure 17

LINE TRANSIENT RESPONSE

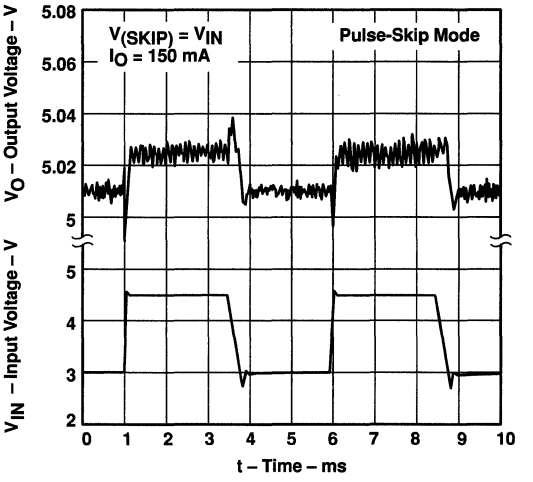


Figure 18

FREQUENCY SPECTRUM CONSTANT FREQUENCY MODE‡

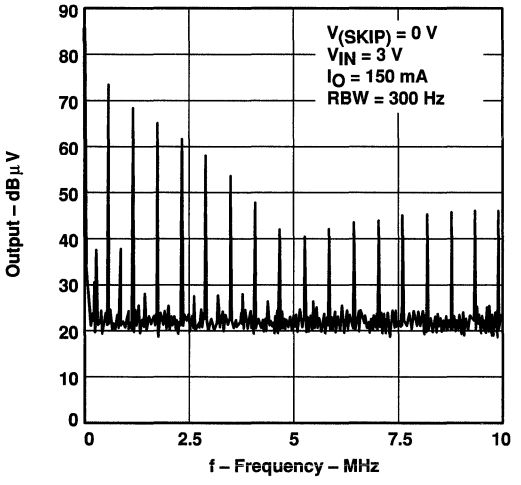


Figure 19

FREQUENCY SPECTRUM PULSE-SKIP MODE‡

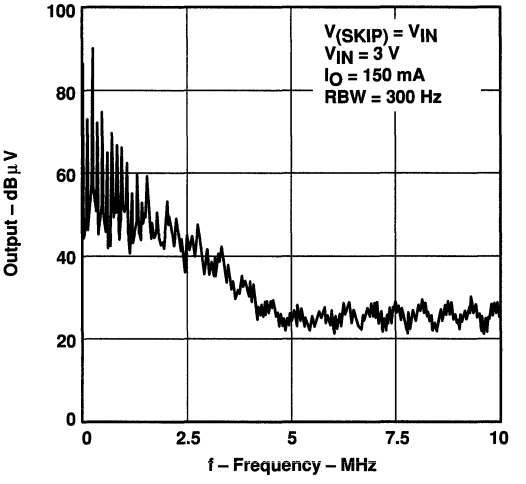


Figure 20

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 μF, C_{1F} = C_{2F} = 2.2 μF, C_O = 33 μF, unless otherwise noted
‡Test circuit: TPS60110EVM–132

TYPICAL CHARACTERISTICS†

FREQUENCY SPECTRUM
CONSTANT FREQUENCY MODE‡

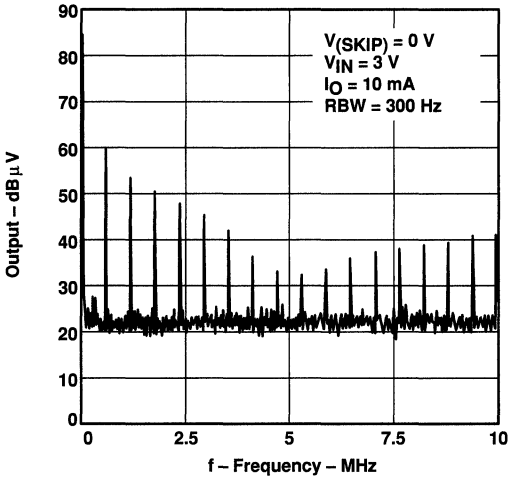


Figure 21

FREQUENCY SPECTRUM
PULSE-SKIP MODE‡

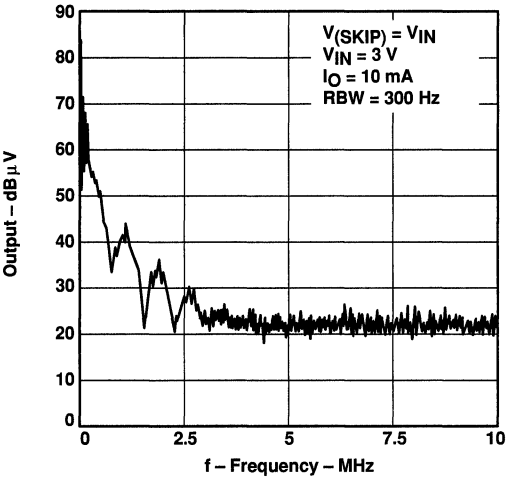


Figure 22

EFFICIENCY
vs
INPUT VOLTAGE

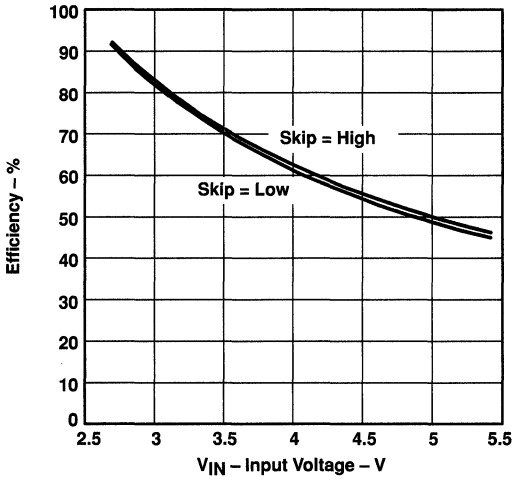


Figure 23

START-UP TIMING

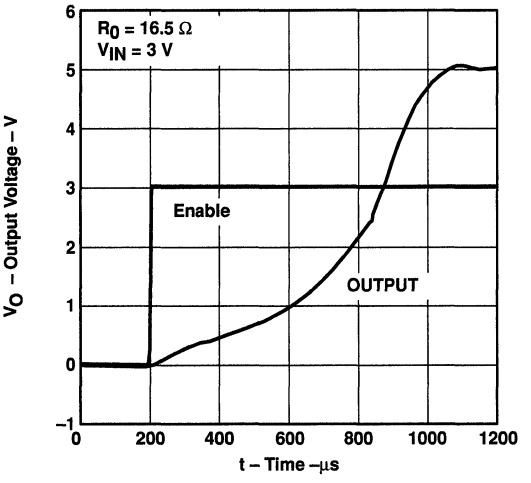


Figure 24

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 μF, C_{1F} = C_{2F} = 2.2 μF, C_O = 33 μF, unless otherwise noted
‡Test circuit: TPS60110EVM–132

detailed description

operating principle

The TPS60110 charge pump provides a regulated 5-V output from a 2.7-V to 5.4-V input. It delivers a maximum load current of 300 mA. Designed specifically for space critical battery powered applications, the complete charge pump circuit requires only four external capacitors. The circuit can be optimized for highest efficiency at light loads or lowest output noise. The TPS60110 consists of an oscillator, a 1.22-V bandgap reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (Figure 25)

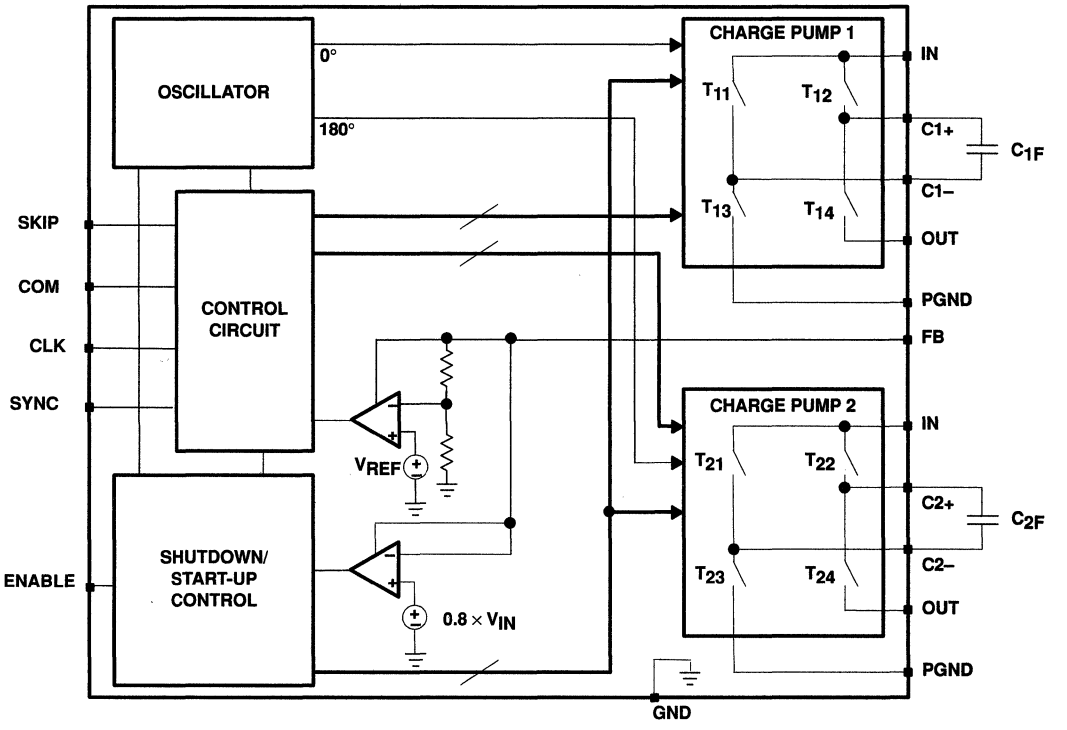


Figure 25. Functional Block Diagram TPS60110

The oscillator runs at a 50% duty cycle. The device consists of two single-ended charge pumps which operate with 180° phase shift. Each single ended charge pump transfers charge into its transfer capacitor (C_{xF}) in one half of the period. During the other half of the period (transfer phase), C_{xF} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name doubler). In order to provide a regulated fixed output voltage of 5 V, the TPS60110 uses either pulse-skip mode or constant-frequency mode. Pulse-skip mode and constant-frequency mode are externally selected via the SKIP input pin.

detailed description (continued)

start-up procedure

During start-up, i.e. when ENABLE is set from logic low to logic high, the switches T12 and T14 (charge pump 1), and the switches T22 and T24 (charge pump 2) are conducting to charge up the output capacitor until the output voltage V_O reaches $0.8 \times V_{IN}$. When the start-up comparator detects this limit, the IC begins to operate in the mode selected with SKIP and COM. This start-up charging of the output capacitor guarantees a short start-up time and eliminates the need for a Schottky diode between IN and OUT.

pulse-skip mode

In pulse-skip mode (SKIP = high), the error amplifier disables switching of the power stages when it detects an output higher than 5 V. The oscillator halts. The IC then skips switching cycles until the output voltage drops below 5 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except bandgap reference and error amplifier when the output is higher than 5 V. When switching is disabled from the error amplifier, the load is also isolated from the input. SKIP is a logic input and should not remain floating. The typical operating circuit of the TPS60110 in pulse skip mode is shown in Figure 1.

constant-frequency mode

When SKIP is low, the charge pump runs continuously at the frequency f_{OSC}. The control circuit, fed from the error amplifier, controls the charge on C_{1F} and C_{2F} by driving the gates of the FETs T_{12}/T_{13} and T_{22}/T_{23}, respectively. When the output voltage falls, the gate drive increases, resulting in a larger voltage across C_{1F} and C_{2F}. This regulation scheme minimizes output ripple. Since the device switches continuously, the output noise contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads than pulse-skip mode.

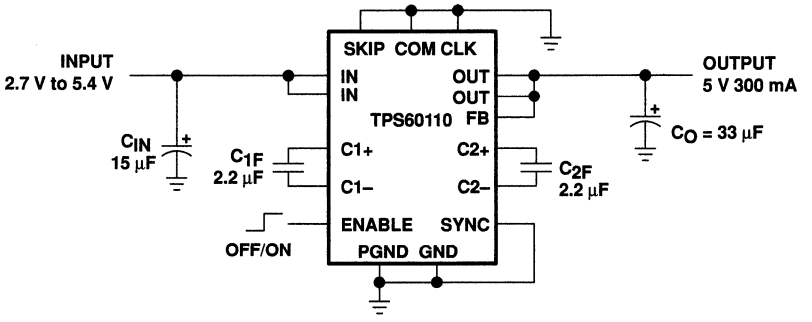


Figure 26. Typical Operating Circuit TPS60110 in Constant Frequency Mode

Table 1. Tradeoffs Between Operating Modes

FEATURE	PULSE-SKIP MODE (SKIP = High)	CONSTANT-FREQUENCY MODE (SKIP = Low)
Best light-load efficiency	X	
Smallest external component size for a given output ripple		X
Output ripple amplitude	Small amplitude	Very small amplitude
Output ripple frequency	Variable	Constant
Load regulation	Very good	Good

NOTE: Even in pulse-skip mode the output ripple amplitude is small if the push-pull operating mode is selected via COM.

detailed description (continued)

push-pull operating mode

In push-pull operating mode (COM = low), the two single-ended charge pumps operate with 180° phase shift. The oscillator signal has a 50% duty cycle. Each single-ended charge pump transfers charge into its transfer capacitor (C_{xF}) in one-half of the period. During the other half of the period (transfer phase), C_{xF} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple. COM is a logic input and should not remain floating. The typical operating circuit of the TPS60110 in push-pull mode is shown in Figure 1 and Figure 26.

single-ended operating mode

When COM is high, the device runs in single-ended operating mode. The two single-ended charge pumps operate in parallel without phase shift. They transfer charge into the transfer capacitor (C_F) in one half of the period. During the other half of the period (transfer phase), C_F is placed in series with the input to transfer its charge to C_O. In single-ended operating mode only one transfer capacitor ($C_F = C_{1F} + C_{2F}$) is required, resulting in less board space.

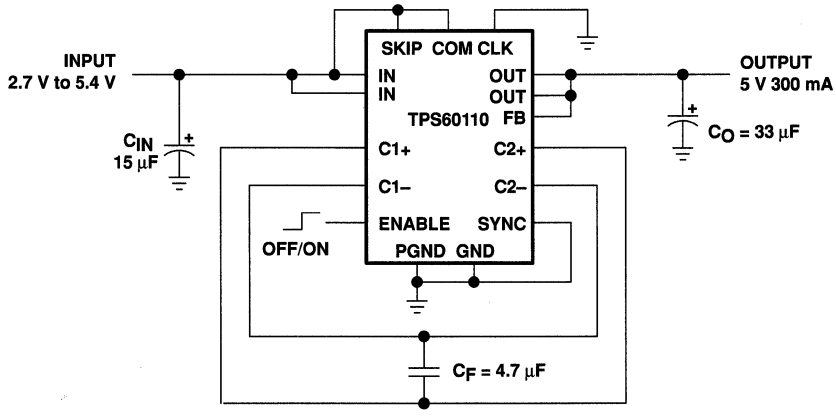


Figure 27. Typical Operating Circuit TPS60110 in Single-Ended Operating Mode

Table 2. Tradeoffs Between Operating Modes

FEATURE	PUSH-PULL MODE (COM = Low)	SINGLE-ENDED MODE (COM = High)
Output ripple amplitude	Small amplitude	Large amplitude
Smallest board space		X

detailed description (continued)

shutdown

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05-µA (1-µA max) of supply current in this mode. Leakage current drawn from the output is as low as 1 µA max. The device exits shutdown once ENABLE is set high level. The typical no-load shutdown exit time is 20 µs. When the device is in shutdown, the load is isolated from the input and the output is high impedance.

external clock signal

If the device operates at a user defined frequency, an external clock signal can be used. Therefore, SYNC needs to be connected to IN and the external oscillator signal can drive CLK. The maximum external frequency is limited to 800 kHz. The switching frequency of the converter is half of the external oscillator frequency. It is recommended to operate the charge pump in constant-frequency mode if an external clock signal is used so that the output noise contains only well-defined frequency components.

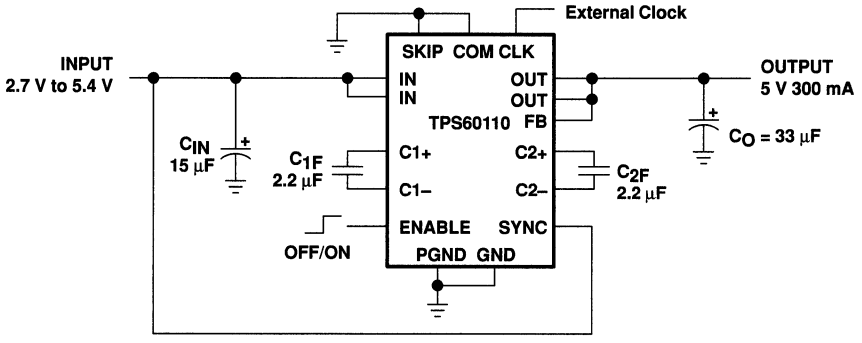


Figure 28. Typical Operating Circuit TPS60110 With External Synchronization

APPLICATION INFORMATION

capacitor selection

The TPS60110 requires only four external capacitors as shown in the basic application circuit. Their values are closely linked to the output current capacity, output noise requirements, and mode of operation. Generally, the transfer capacitors (C_{xF}) will be the smallest.

The input capacitor improves system efficiency by reducing the input impedance and stabilizes the input current. C_{IN} is recommended to be about two to four times as large as C_{xF}.

The output capacitor (C_O) can be selected from 8-times to 50-times larger than C_{xF}, depending on the mode of operation and ripple tolerance†. Tables 3 and 4 show capacitor values recommended for low quiescent-current operation (pulse-skip mode) and for low output voltage ripple operation (constant-frequency mode). A recommendation is given for smallest size.

Table 3. Recommended Capacitor Values for Low Quiescent-Current Operation† (pulse-skip mode)

V_{IN} [V]	I_O [mA]	C_{IN} [µF]		C_{xF} [µF]	C_O [µF]		OUTPUT VOLTAGE RIPPLE V_{PP} [mV]
		TANTALUM	CERAMIC		TANTALUM	CERAMIC	
3.6	225	15		2.2	33		145
3.6	225		4.7 + 10, (X5R)	2.2		22 + 10, (X5R)	55
3.6	300	15		2.2	33		135
3.6	300		4.7 + 10, (X5R)	2.2		22 + 10, (X5R)	75

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

Table 4. Recommended Capacitor Values for Low Output Voltage Ripple Operation† (constant-frequency mode)

V_{IN} [V]	I_O [mA]	C_{IN} [µF]		C_{xF} [µF]	C_O [µF]		OUTPUT VOLTAGE RIPPLE V_{PP} [mV]
		TANTALUM	CERAMIC		TANTALUM	CERAMIC	
3.6	225	15		2.2	33		17
3.6	225		4.7 + 10, (X5R)	2.2		22 + 10, (X5R)	6
3.6	300	15		2.2	33		22
3.6	300		4.7 + 10, (X5R)	2.2		22 + 10, (X5R)	8

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

† In constant-frequency mode always select $C_O \geq 33$ µF

APPLICATION INFORMATION

For the TPS60110, the smallest board space size can be achieved using Sprague's 595D-series tantalum capacitors for input and output. However, with the trend towards high capacitance ceramic capacitors in smaller size packages, these type of capacitors might soon become competitive in size.

Table 5. Recommended Capacitors

MANUFACTURER	PART NUMBER	CAPACITANCE	TYPE
Taiyo Yuden	LMK212BJ105KG–T	1 µF	Ceramic
	LMK212BJ225MG–T	2.2 µF	Ceramic
	LMK316BJ475KL–T	4.7 µF	Ceramic
	JMK316BJ106ML–T	10 µF	Ceramic
	LMK432BJ226MM–T	22 µF	Ceramic
AVX	0805ZC105KAT2A	1 µF	Ceramic
	1206ZC225KAT2A	2.2 µF	Ceramic
	TPSC156K020R0450	15 µF	Tantalum
	TPSC336K010R0375	33 µF	Tantalum
Sprague	595D156X06R3A2T	15 µF	Tantalum
	595D156X0016B2T	15 µF	Tantalum
	595D336X06R3A2T	33 µF	Tantalum
	595D336X0016B2T	33 µF	Tantalum
	595D336X0016C2T	33 µF	Tantalum
Kemet	T494C156K010AS	15 µF	Tantalum
	T494C336K010AS	33 µF	Tantalum

Table 6 lists the manufacturers of recommended capacitors. In most applications surface-mount tantalum capacitors will be the right choice. However, ceramic capacitors will provide the lowest output voltage ripple due to their typically lower ESR.

Table 6. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET
Taiyo Yuden	X7R/X5R ceramic	www.t–yuden.com
AVX	X7R/X5R ceramic TPS–series tantalum	www.avxcorp.com
Sprague	595D–series tantalum 593D–series tantalum	www.vishay.com
Kemet	T494–series tantalum	www.kemet.com

power dissipation

The power dissipated in the TPS60110 depends on output current and is approximated by:

$$P_{DISS} = I_O \times (2\ V_{IN} - V_O) \text{ for } I_Q << I_O$$

P_{DISS} must be less than that allowed by the package rating. See the ratings for 20-PowerPAD™ package power-dissipation limits and deratings.

APPLICATION INFORMATION

layout

All capacitors should be soldered in close proximity to the IC. A PCB layout proposal for a two-layer board is given in Figure 29. Care has been taken to connect both single-ended charge pumps symmetrically to the load to achive optimized output voltage ripple performance. The proposed layout also provides improved thermal performance as the exposed leadframe is soldered to the PCB. The bottom layer of the PCB is a ground plain only. All ground areas on the PCB should be connected. Connect ground areas on top layer to the bottom layer via through hole connections.

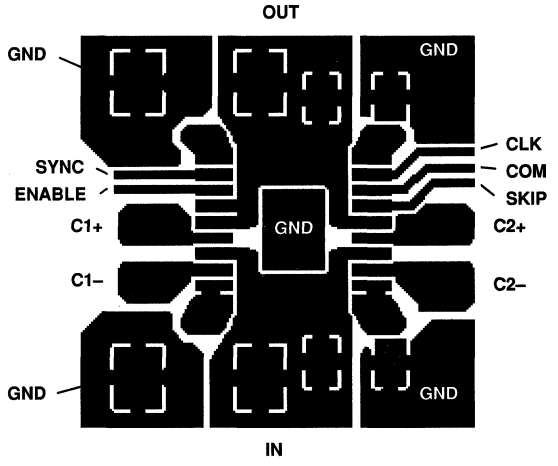


Figure 29. Recommended PCB Layout for TPS60110 (top view)

An evaluation module for the TPS60110 is available and can be ordered under literature code SLVP132 or under product code TPS60110EVM–132.

APPLICATION INFORMATION

applications proposals

paralleling of two TPS60110 to deliver 600 mA

The TPS60110 can be paralleled to yield higher load currents. The circuit of Figure 30 can deliver 600 mA at an output voltage of 5 V. It uses two TPS60110 devices in parallel. The devices can share the output capacitors, but each one requires its own transfer capacitors and input capacitor. For best performance, the paralleled devices should operate in the same mode (pulse-skip or constant frequency).

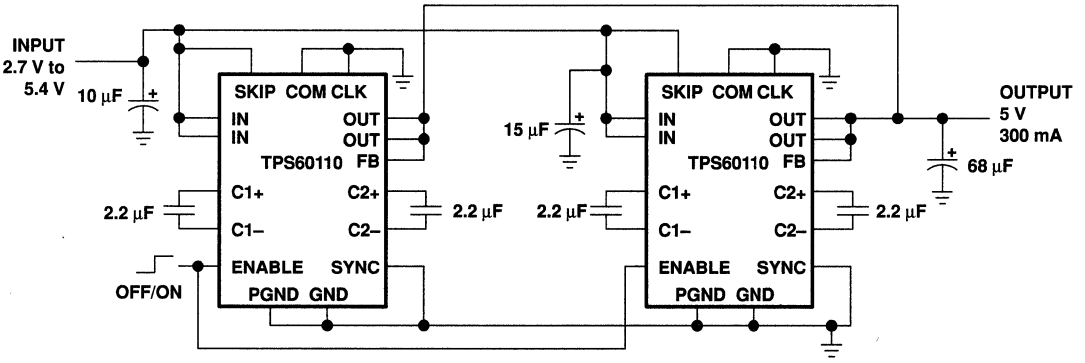


Figure 30. Paralleling of Two TPS60110

TPS60110 with LC output filter for ultra low ripple

For applications where extremely low output ripple is required, a small LC filter is recommended. This is shown in Figure 31. The addition of a small inductor and filter capacitor will reduce the output ripple well below what could be achieved with capacitors alone. The corner frequency of 500 kHz was chosen above the 300 kHz switching frequency to avoid loop stability issues in case the feedback is taken from the output of the LC filter. Leaving the feedback (FB) connection point before the LC filter, the filter capacitance value can be increased to achieve even higher ripple attenuation without affecting stability margin.

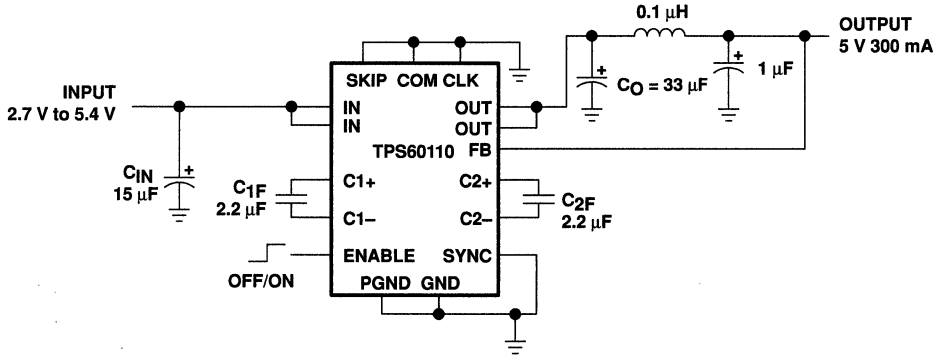


Figure 31. TPS60110 With LC Filter for Ultra Low Output Ripple Applications

APPLICATION INFORMATION

related information

application reports

For more application information see:

- *PowerPAD™ Application Report* (Literature Number: SLMA002)
- *TPS6010x/TPS6011x Charge Pump Application Report* (Literature Number: SLVA070)

device family products

Other devices in this family are:

PART NUMBER	LITERATURE NUMBER	DESCRIPTION
TPS60100	SLVS213	Regulated 3.3-V, 200-mA Low-Noise Charge Pump DC/DC Converter
TPS60101	SLVS214	Regulated 3.3-V, 100-mA Low-Noise Charge Pump DC/DC Converter
TPS60111	SLVS216	Regulated 5-V, 150-mA Low-Noise Charge Pump DC/DC Converter

features

- Up to 150-mA Output Current
- Less Than 10-mV$_{pp}$ Output Voltage Ripple
- No Inductors Required/Low EMI
- Regulated 5-V ±4% Output
- Only Four External Components Required
- Up to 90% Efficiency
- 2.7-V to 5.4-V Input Voltage Range
- 60-μA Quiescent Supply Current
- 0.05-μA Shutdown Current
- Load Isolated in Shutdown
- Space-Saving Thermally-Enhanced TSSOP PowerPAD™ Package
- Evaluation Module Available (TPS60110EVM–132)

description

The TPS60111 step-up, regulated charge pump generates a 5-V ±4% output voltage from a 2.7-V to 5.4-V input voltage (three alkaline, NiCd, or NiMH batteries; or, one lithium or lithium ion battery). Output current is 150 mA from a 3-V input. Only four external capacitors are needed to build a complete low-noise dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple as current is continuously transferred to the output. From a 3-V input, the TPS60111 can start into full load with loads as low as 33 Ω.

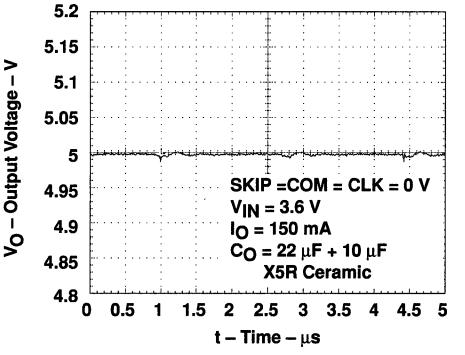
The TPS60111 features either constant frequency mode to minimize noise and output voltage ripple or the power-saving pulse-skip mode to extend battery life at light loads. The TPS60111 switching frequency is 300 kHz. The logic shutdown function reduces the supply current to 1-μA (max) and disconnects the load from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during start-up. This dc/dc converter requires no inductors and has low EMI. It is available in the small 20-pin TSSOP PowerPAD™ package (PWP).

applications

Replaces DC/DC Converters With Inductors in

- Battery-Powered Applications
- Li-Ion Battery to 5-V Conversion
- Portable Instruments
- Battery-Powered Microprocessor Systems
- Miniature Equipment
- Backup-Battery Boost Converters
- PDAs
- Laptops
- Handheld Instrumentation
- Medical Instruments

output voltage ripple



typical operating circuit

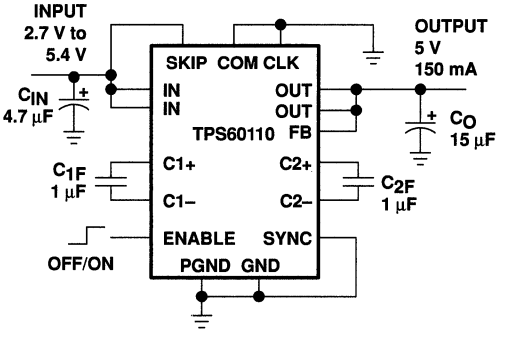
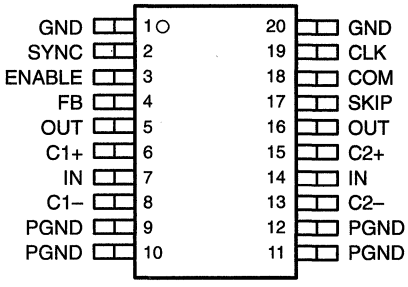


Figure 1

PowerPAD is a trademark of Texas Instruments Incorporated.

PWP PACKAGE
(TOP VIEW)



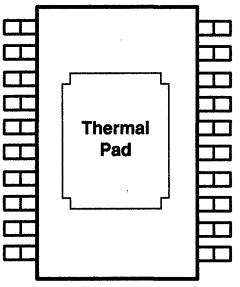


Figure 2. Bottom View of PWP Package, Showing the Thermal Pad

AVAILABLE OPTIONS

PACKAGE
TSSOP† (PWP)
TPS60111PWP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TPS60111PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	19	I	Input for external clock signal. If the internal clock is used, connect this terminal to GND.
C1+	6		Positive terminal of the charge-pump capacitor C_{1F}
C1–	8		Negative terminal of the charge-pump capacitor C_{1F}
C2+	15		Positive terminal of the charge-pump capacitor C_{2F}
C2–	13		Negative terminal of the charge-pump capacitor C_{2F}
COM	18	I	Mode selection. When COM is logic low the charge pump operates in push-pull mode to minimize output ripple. When COM is connected to IN the regulator operates in single-ended mode requiring only one flying capacitor.
ENABLE	3	I	ENABLE Input. The device turns off, the output disconnects from the input, and the supply current decreases to 0.05 µA when ENABLE is a logic low. Connect ENABLE to IN for normal operation.
FB	4	I	FEEDBACK input. Connect FB to OUT as close to the load as possible to achieve best regulation. Resistive divider is on-chip to match internal reference voltage of 1.22 V.
GND	1, 20		GROUND. Analog ground for internal reference and control circuitry. Connect to PGND through a short trace.
IN	7, 14	I	Supply Input. Connect to an input supply in the 2.7-V to 5.4-V range. Bypass IN to GND with a (C_O/2) µF capacitor. Connect both INs through a short trace.
OUT	5, 16	O	Regulated 5-V power output. Connect both OUTs through a short trace and bypass OUT to GND with the output filter capacitor C_O.
PGND	9–12		PGND power ground. Charge-pump current flows through this pin. Connect all PGNDs together.
SKIP	17	I	Mode selection. When SKIP is logic low the charge pump operates in constant-frequency mode. Thus output ripple and noise are minimized. When SKIP is connected to IN, the regulator operates in low-quiescent-current pulse-skip mode.
SYNC	2	I	Selection for external clock signal. Connect to GND to use the internally generated clock signal. Connect to IN for external synchronization. In this case, the clock signal needs to be fed through CLK.

absolute maximum ratings (unless otherwise noted)†‡

Input voltage range, V_I (IN, OUT, ENABLE, SKIP, COM, CLK, FB, SYNC) ..... –0.3 V to 5.5 V
Differential input voltage, V_{ID} (C1+, C2+ to GND) ..... –0.3 V to (V_O + 0.3 V)
Differential input voltage, V_{ID} (C1–, C2– to GND) ..... –0.3 V to (V_{IN} + 0.3 V)
Continuous total power dissipation ..... See Dissipation Rating Tables
Continuous output current ..... 200 mA
Storage temperature range, T_{stg} ..... –55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10s ..... 260°C
Maximum junction temperature, T_J ..... 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ V_{ENABLE}, V_{SKIP}, V_{COM}, V_{CLK} and V_{SYNC} can exceed V_{IN} up to the maximum rated voltage without increasing the leakage current drawn by these mode select inputs.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	700 mW	5.6 mW/°C	448 mW	364 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)

PACKAGE	$T_C \le 62.5°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING
PWP	25 W	285.7 mW/°C	22.9 W	18.5 W

DISSIPATION DERATING CURVE§ vs FREE-AIR TEMPERATURE

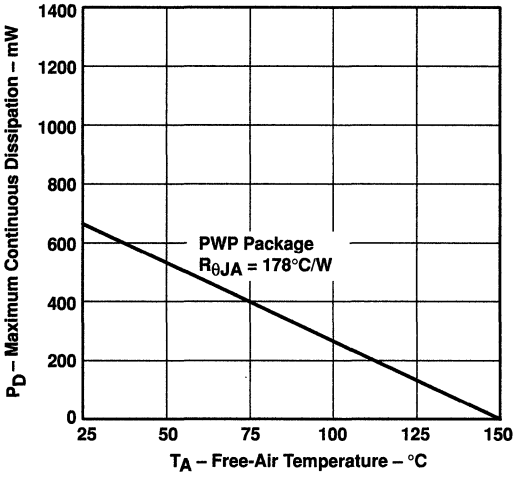


Figure 3

MAXIMUM CONTINUOUS DISSIPATION§ vs CASE TEMPERATURE

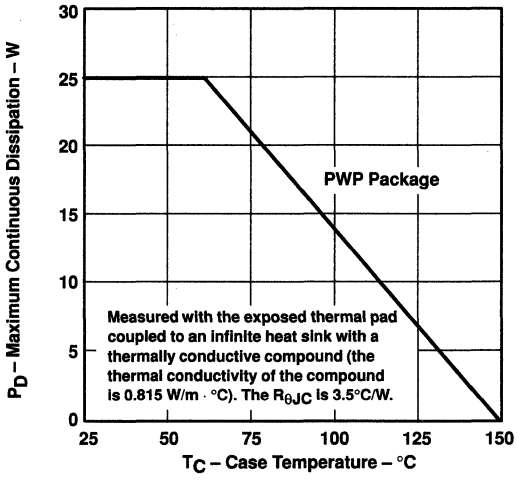


Figure 4

§ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. It is recommended not to exceed a junction temperature of 125°C.

electrical characteristics at C_{IN} = 15 µF, C_{1F} = C_{2F} = 2.2 µF†, C_O = 33 µF, T_C = –40°C to 85°C, V_{IN} = 3 V, V_{FB} = V_O, V_{ENABLE} = V_{IN}, V_{SKIP} = V_{IN} or 0 V and V_{COM} = V_{CLK} = V_{SYNC} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			2.7		5.4	V
$I_{O(MAX)}$	Maximum output current			150			mA
V_O	Output voltage	2.7 V < V_{IN} < 3 V, $V_{O(Start-Up)}$ = 5 V,	0 < I_O < 75 mA, T_C = 25°C	4.8	5	5.2	V
		3 V < V_{IN} < 5 V,	0 < I_O < 150 mA	4.8	5	5.2	
		5 V < V_{IN} < 5.4 V,	0 < I_O < 150 mA	4.8	5	5.25	
$V_{O(RIP)}$	Output voltage ripple	I_O = 150 mA,	V_{SKIP} = 0 V		10‡		mV_{PP}
$I_{O(LEAK)}$	Output leakage current	V_{IN} = 3.6 V,	V_{ENABLE} = 0 V			1	µA
I_Q	Quiescent current (no-load input current)	V_{SKIP} = V_{IN} = 3.6 V			60	90	µA
		V_{SKIP} = 0 V,	V_{IN} = 3.6 V		2.8		mA
$I_{DD(SDN)}$	Shutdown supply current	V_{IN} = 3.6 V,	V_{ENABLE} = 0 V		0.05	1	µA
$f_{OSC(int)}$	Internal switching frequency	V_{IN} = 3.6 V		200	300	400	kHz
$f_{OSC(ext)}$	External clock frequency	V_{SYNC} = V_{IN},	V_{IN} = 2.7 V to 5.4 V	400	600	800	kHz
	External clock duty cycle	V_{SYNC} = V_{IN},	V_{IN}= 2.7V to 5.4 V	20%		80%	
	Efficiency	I_O = 75 mA			80%		
V_{INL}	Input voltage low, ENABLE, SKIP, COM, CLK, SYNC	V_{IN} = 2.7 V				0.3 × V_{IN}	V
V_{INH}	Input voltage high, ENABLE, SKIP, COM, CLK, SYNC	V_{IN} = 5.4 V		0.7 × V_{IN}			V
$I_{I(LEAK)}$	Input leakage current, ENABLE, SKIP, COM, CLK, SYNC	V_{ENABLE} = V_{SKIP} = V_{COM} = V_{CLK} = V_{SYNC} = V_{GND} or V_{IN}			0.01	0.1	µA
	Output load regulation	V_O = 5 V, T_C = 25°C	1 mA < I_O < 150 mA		0.002		%/mA
	Output line regulation	3 V < V_{IN} < 5 V, I_O = 75 mA,	V_O = 5 V, T_C = 25°C		0.6		%/V
	Short circuit current	V_{IN} = 3.6 V T_C = 25°C	V_O = 0 V,		150		mA

† Use only ceramic capacitors with X5R or X7R dielectric as flying capacitors.
‡ Achieved with C_O = 22 µF + 10 µF X5R dielectric ceramic capacitor

TYPICAL CHARACTERISTICS†

EFFICIENCY
vs
OUTPUT CURRENT

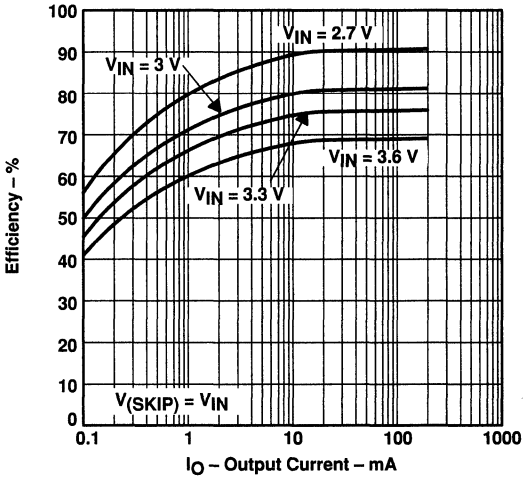


Figure 5

EFFICIENCY
vs
OUTPUT CURRENT

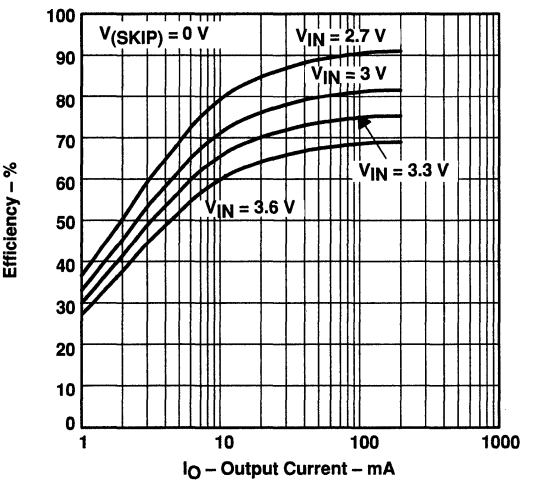


Figure 6

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

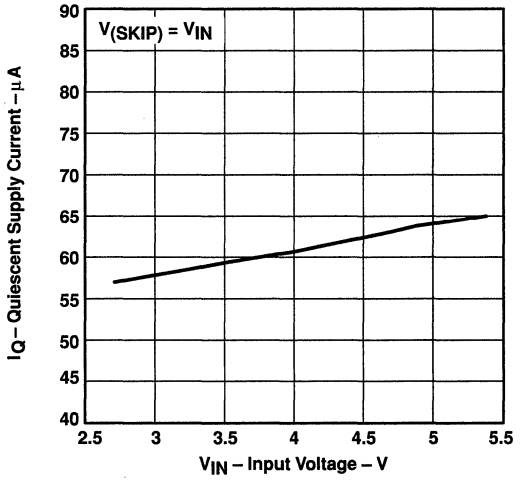


Figure 7

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

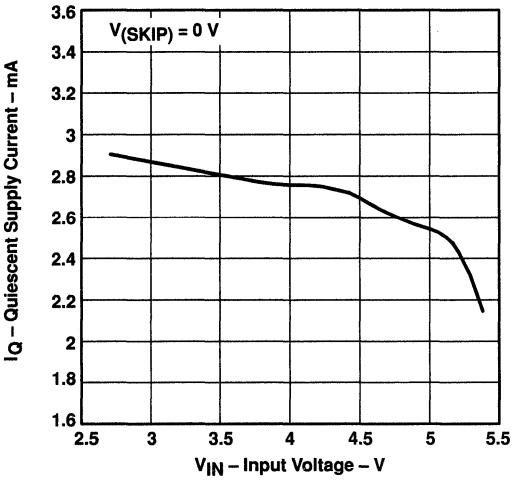


Figure 8

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 µF, C_{1F} and C_{2F} = 2.2 µF (X7R ceramic), C_O = 33 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

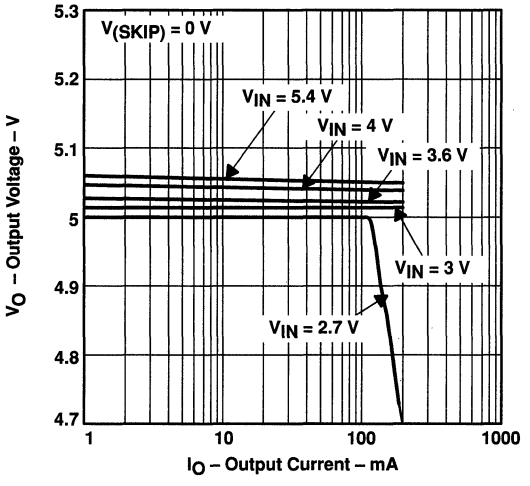


Figure 9

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

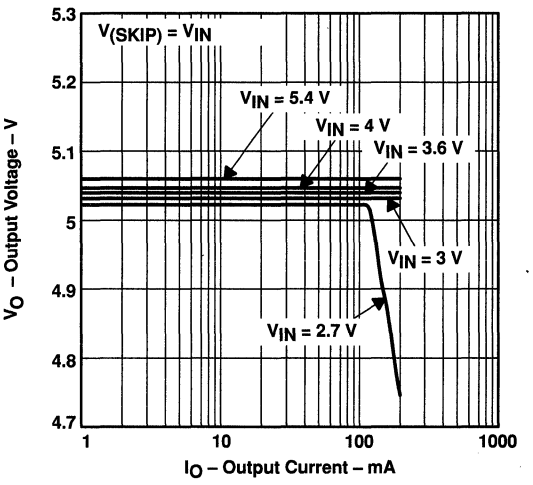


Figure 10

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

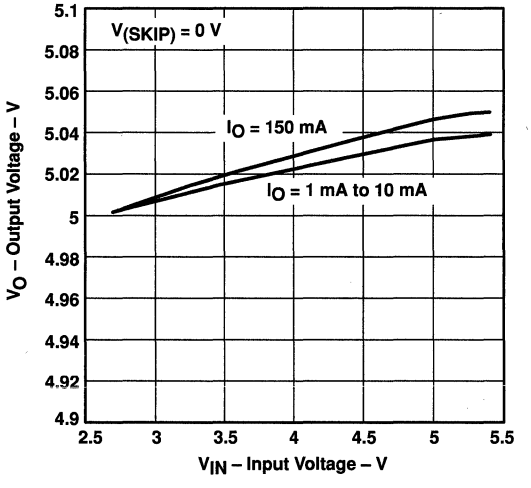


Figure 11

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

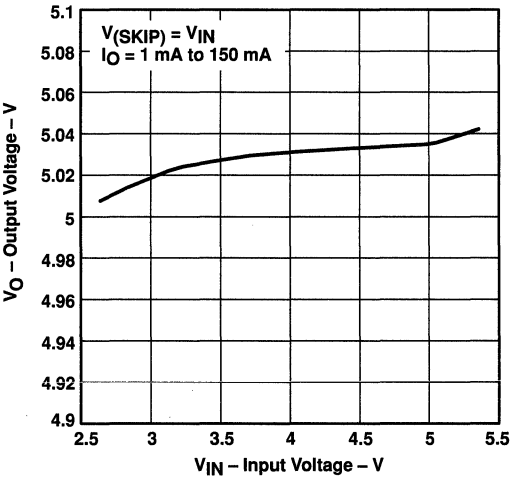


Figure 12

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 µF, C_{1F} and C_{2F} = 2.2 µF (X7R ceramic), C_O = 33 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
TIME

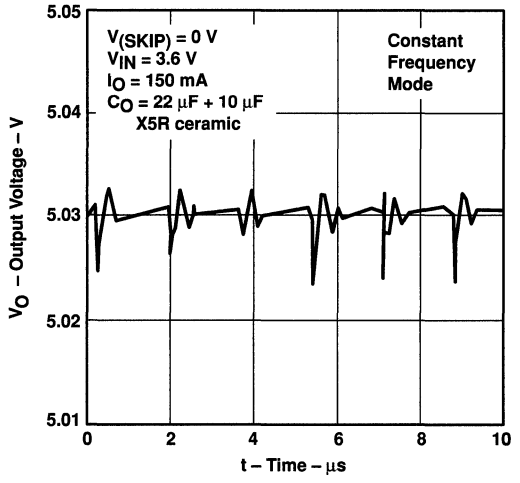


Figure 13

OUTPUT VOLTAGE
vs
TIME

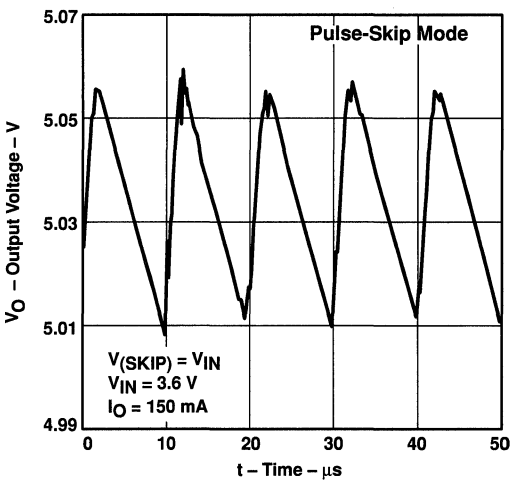


Figure 14

LOAD TRANSIENT RESPONSE

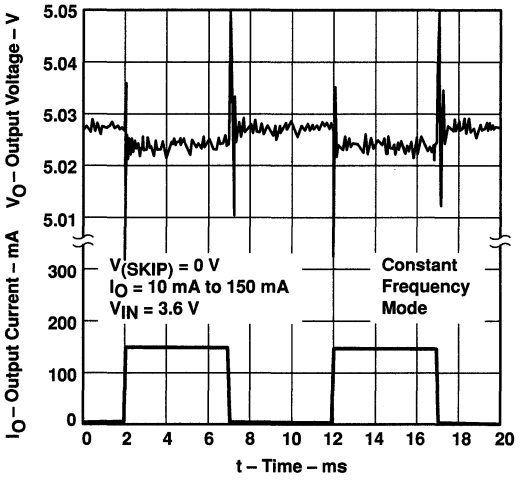


Figure 15

LOAD TRANSIENT RESPONSE

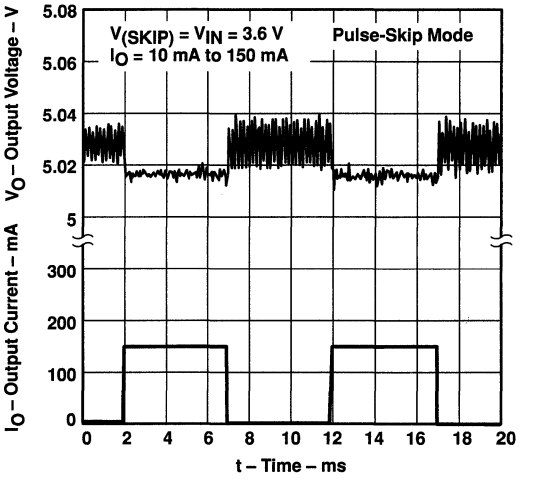


Figure 16

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 µF, C_{1F} and C_{2F} = 2.2 µF (X7R ceramic), C_O = 33 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

LINE TRANSIENT RESPONSE

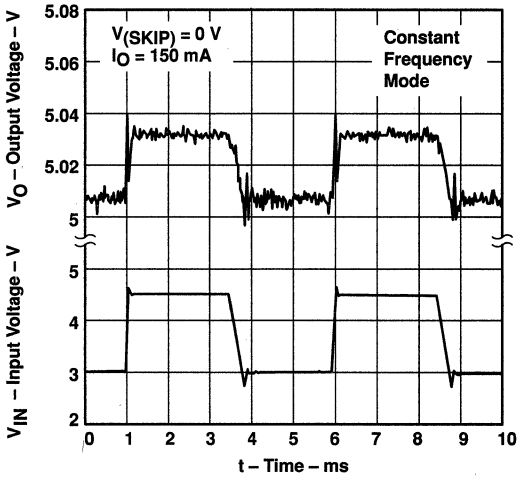


Figure 17

LINE TRANSIENT RESPONSE

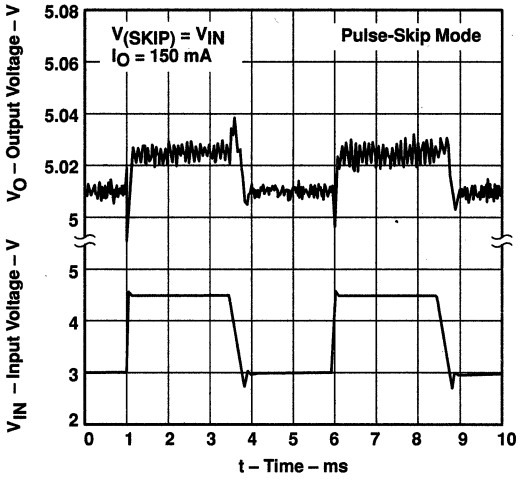


Figure 18

FREQUENCY SPECTRUM
CONSTANT FREQUENCY MODE‡

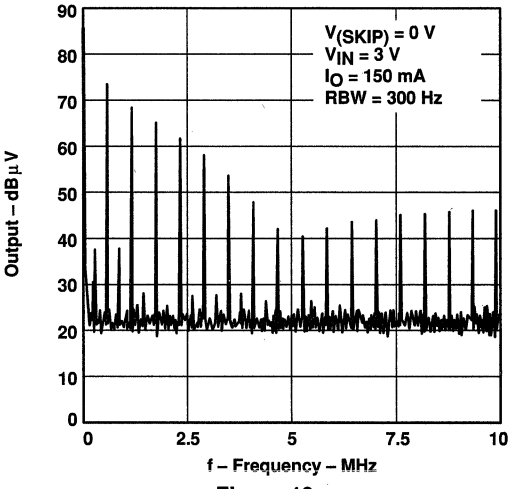


Figure 19

FREQUENCY SPECTRUM
PULSE-SKIP MODE‡

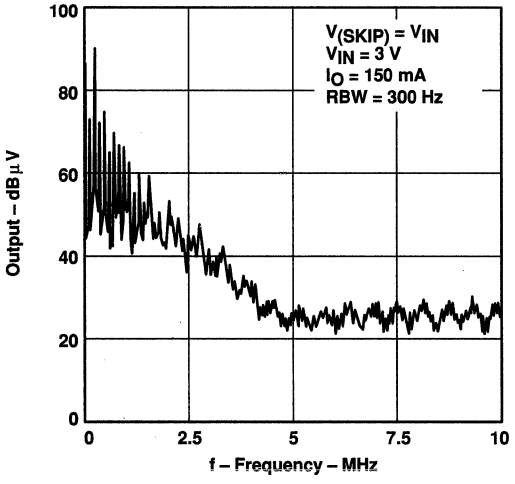


Figure 20

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 μF, C_{1F} and C_{2F} = 2.2 μF (X7R ceramic), C_O = 33 μF, unless otherwise noted
‡Test circuit: TPS60110EVM–132 with TPS60111

TYPICAL CHARACTERISTICS†

FREQUENCY SPECTRUM
CONSTANT FREQUENCY MODE‡

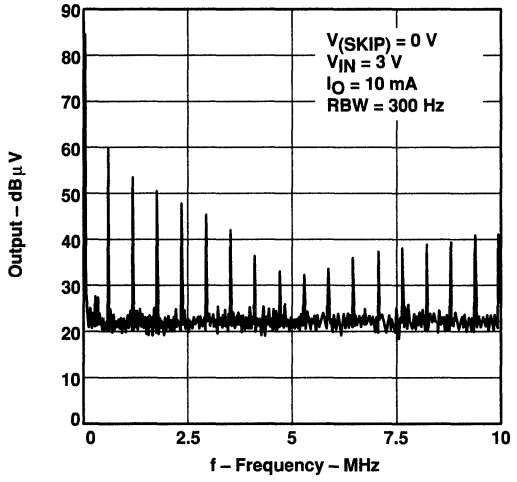


Figure 21

FREQUENCY SPECTRUM
PULSE-SKIP MODE‡

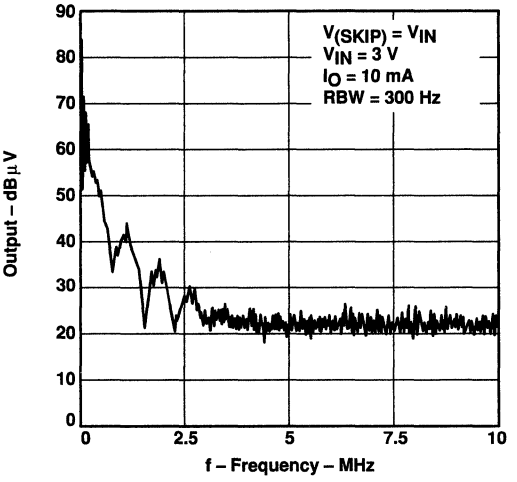


Figure 22

EFFICIENCY
vs
INPUT VOLTAGE

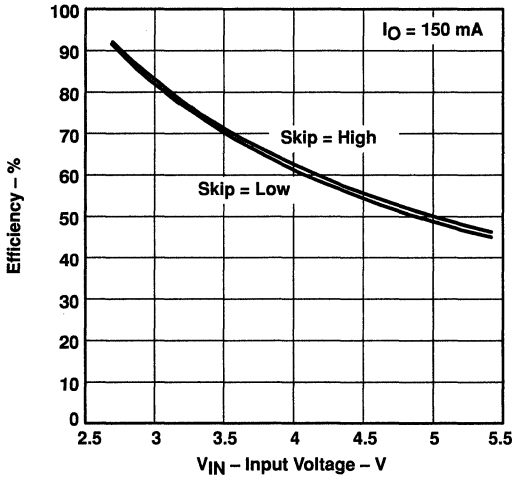


Figure 23

START-UP TIMING

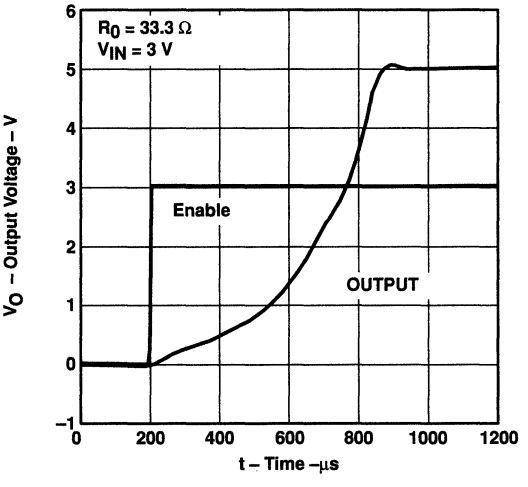


Figure 24

†T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 μF, C_{1F} and C_{2F} = 2.2 μF (X7R ceramic), C_O = 33 μF, unless otherwise noted
‡Test circuit: TPS60110EVM–132 with TPS60111

detailed description

operating principle

The TPS60111 charge pump provides a regulated 5-V output from a 2.7-V to 5.4-V input. It delivers a maximum load current of 150 mA. Designed specifically for space critical battery powered applications, the complete charge pump circuit requires only four external capacitors. The circuit can be optimized for highest efficiency at light loads or lowest output noise. The TPS60111 consists of an oscillator, a 1.22-V bandgap reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (Figure 25).

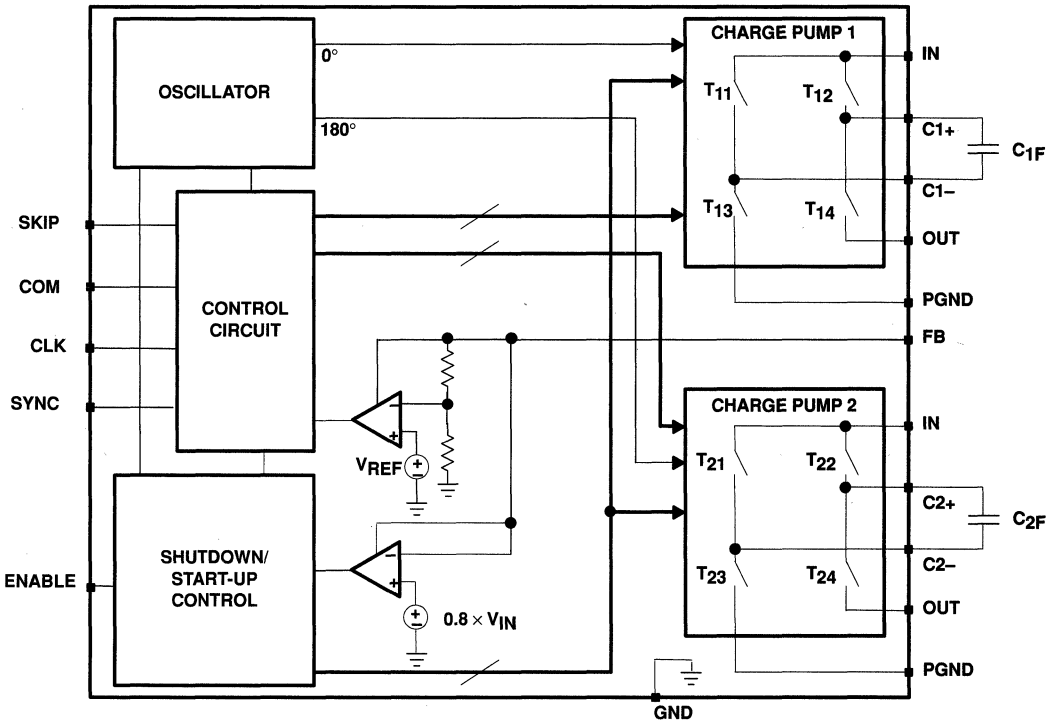


Figure 25. Functional Block Diagram TPS60111

The oscillator runs at a 50% duty cycle. The device consists of two single-ended charge pumps which operate with 180° phase shift. Each single ended charge pump transfers charge into its transfer capacitor (C_{xF}) in one half of the period. During the other half of the period (transfer phase), C_{xF} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name doubler). In order to provide a regulated fixed output voltage of 5 V, the TPS60111 uses either pulse-skip mode or constant-frequency mode. Pulse-skip mode and constant-frequency mode are externally selected via the SKIP input pin.

detailed description (continued)

start-up procedure

During start-up, i.e. when ENABLE is set from logic low to logic high, the switches T12 and T14 (charge pump 1), and the switches T22 and T24 (charge pump 2) are conducting to charge up the output capacitor until the output voltage V_O reaches $0.8 \times V_{IN}$. When the start-up comparator detects this limit, the IC begins to operate in the mode selected with SKIP and COM. This start-up charging of the output capacitor guarantees a short start-up time and eliminates the need for a Schottky diode between IN and OUT.

pulse-skip mode

In pulse-skip mode (SKIP = high), the error amplifier disables switching of the power stages when it detects an output higher than 5 V. The oscillator halts. The IC then skips switching cycles until the output voltage drops below 5 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except bandgap reference and error amplifier when the output is higher than 5 V. When switching is disabled from the error amplifier, the load is also isolated from the input. SKIP is a logic input and should not remain floating. The typical operating circuit of the TPS60111 in pulse skip mode is shown in Figure 1.

constant-frequency mode

When SKIP is low, the charge pump runs continuously at the frequency f_{OSC}. The control circuit, fed from the error amplifier, controls the charge on C_{1F} and C_{2F} by driving the gates of the FETs T_{12}/T_{13} and T_{22}/T_{23}, respectively. When the output voltage falls, the gate drive increases, resulting in a larger voltage across C_{1F} and C_{2F}. This regulation scheme minimizes output ripple. Since the device switches continuously, the output noise contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads than pulse-skip mode.

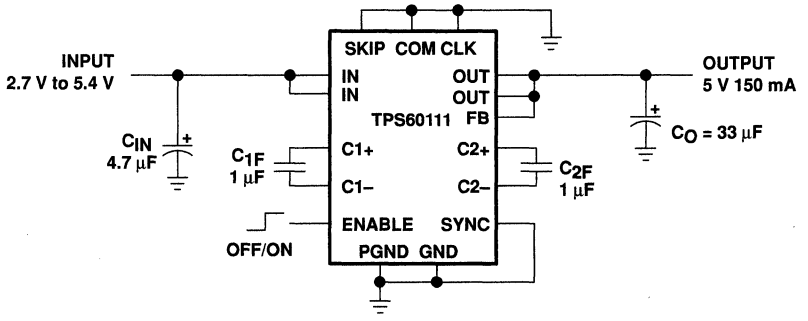


Figure 26. Typical Operating Circuit TPS60111 in Constant Frequency Mode

Table 1. Tradeoffs Between Operating Modes

FEATURE	PULSE-SKIP MODE (SKIP = High)	CONSTANT-FREQUENCY MODE (SKIP = Low)
Best light-load efficiency	X	
Smallest external component size for a given output ripple		X
Output ripple amplitude	Small amplitude	Very small amplitude
Output ripple frequency	Variable	Constant
Load regulation	Very good	Good

NOTE: Even in pulse-skip mode the output ripple amplitude is small if the push-pull operating mode is selected via COM.

detailed description (continued)

push-pull operating mode

In push-pull operating mode (COM = low), the two single-ended charge pumps operate with 180° phase shift. The oscillator signal has a 50% duty cycle. Each single-ended charge pump transfers charge into its transfer capacitor (C_{xF}) in one-half of the period. During the other half of the period (transfer phase), C_{xF} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple. COM is a logic input and should not remain floating. The typical operating circuit of the TPS60111 in push-pull mode is shown in Figure 1 and Figure 26.

single-ended operating mode

When COM is high, the device runs in single-ended operating mode. The two single-ended charge pumps operate in parallel without phase shift. They transfer charge into the transfer capacitor (C_F) in one half of the period. During the other half of the period (transfer phase), C_F is placed in series with the input to transfer its charge to C_O. In single-ended operating mode only one transfer capacitor ($C_F = C_{1F} + C_{2F}$) is required, resulting in less board space.

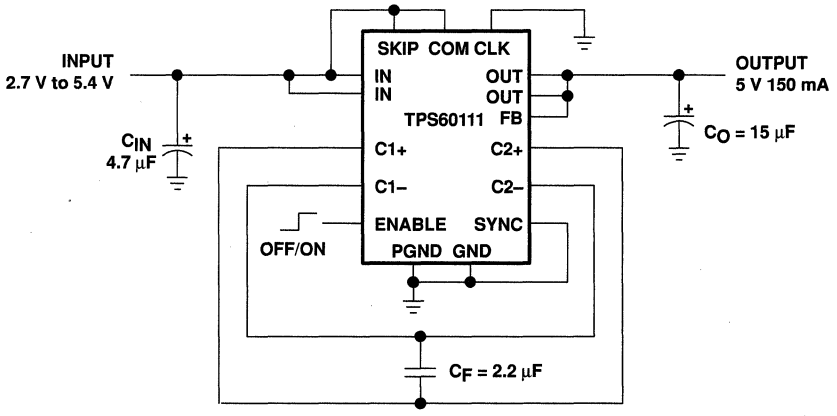


Figure 27. Typical Operating Circuit TPS60111 in Single-Ended Operating Mode

Table 2. Tradeoffs Between Operating Modes

FEATURE	PUSH-PULL MODE (COM = Low)	SINGLE-ENDED MODE (COM = High)
Output ripple amplitude	Small amplitude	Large amplitude
Smallest board space		X

detailed description (continued)

shutdown

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05-µA (1-µA max) of supply current in this mode. Leakage current drawn from the output is as low as 1 µA max. The device exits shutdown once ENABLE is set high level. The typical no-load shutdown exit time is 20 µs. When the device is in shutdown, the load is isolated from the input and the output is high impedance.

external clock signal

If the device operates at a user-defined frequency, an external clock signal can be used. Therefore, SYNC needs to be connected to IN and the external oscillator signal can drive CLK. The maximum external frequency is limited to 800 kHz. The switching frequency of the converter is half of the external oscillator frequency. It is recommended to operate the charge pump in constant-frequency mode if an external clock signal is used so that the output noise contains only well-defined frequency components.

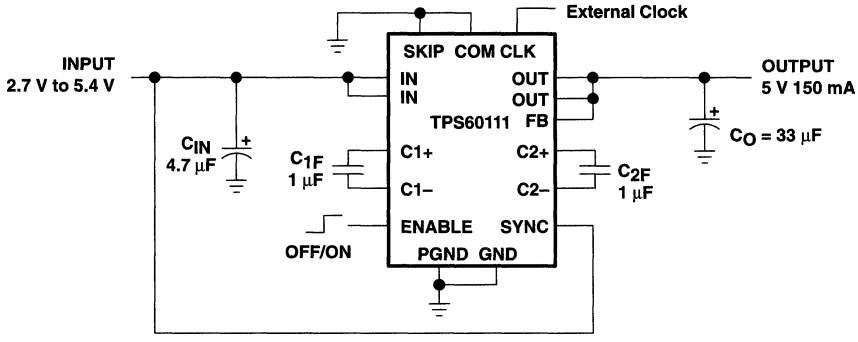


Figure 28. Typical Operating Circuit TPS60111 With External Synchronization

APPLICATION INFORMATION

capacitor selection

The TPS60111 requires only four external capacitors as shown in the basic application circuit. Their values are closely linked to the output current capacity, output noise requirements, and mode of operation. Generally, the transfer capacitors (C_{xF}) will be the smallest.

The input capacitor improves system efficiency by reducing the input impedance and stabilizes the input current. C_{IN} is recommended to be about two to four times as large as C_{xF}.

The output capacitor (C_O) can be selected from 8-times to 50-times larger than C_{xF}, depending on the mode of operation and ripple tolerance†. Tables 3 and 4 show capacitor values recommended for low quiescent-current operation (pulse-skip mode) and for low output voltage ripple operation (constant-frequency mode). A recommendation is given for smallest size.

Table 3. Recommended Capacitor Values for Low Quiescent-Current Operation† (pulse-skip mode)

V_{IN} [V]	I_O [mA]	C_{IN} [µF]		C_{xF} [µF]	C_O [µF]		OUTPUT VOLTAGE RIPPLE V_{pp} [mV]
		TANTALUM	CERAMIC		TANTALUM	CERAMIC	
3.6	75	4.7		1	15		150
3.6	75		4.7 (X7R)	1		10 (X5R)	105
3.6	150	4.7		1	15		150
3.6	150		4.7 (X7R)	1		10 (X5R)	105

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

Table 4. Recommended Capacitor Values for Low Output Voltage Ripple Operation† (constant-frequency mode)

V_{IN} [V]	I_O [mA]	C_{IN} [µF]		C_{xF} [µF]	C_O [µF]		OUTPUT VOLTAGE RIPPLE V_{pp} [mV]
		TANTALUM	CERAMIC		TANTALUM	CERAMIC	
3.6	75	4.7		1	33		10
3.6	75		4.7 (X7R)	1		22 + 10, (X5R)	6
3.6	150	4.7		1	33		17
3.6	150		4.7 (X7R)	1		22 + 10, (X5R)	10

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

† In constant-frequency mode always select $C_O \geq 33$ µF

APPLICATION INFORMATION

For the TPS60111, the smallest board space size can be achieved using Sprague's 595D-series tantalum capacitors for input and output. However, with the trend towards high capacitance ceramic capacitors in smaller size packages, these type of capacitors might soon become competitive in size.

Table 5. Recommended Capacitors

MANUFACTURER	PART NUMBER	CAPACITANCE	TYPE
Taiyo Yuden	LMK212BJ105KG–T	1 µF	Ceramic
	LMK212BJ225MG–T	2.2 µF	Ceramic
	LMK316BJ475KL–T	4.7 µF	Ceramic
	JMK316BJ106ML–T	10 µF	Ceramic
	LMK432BJ226MM–T	22 µF	Ceramic
AVX	0805ZC105KAT2A	1 µF	Ceramic
	1206ZC225KAT2A	2.2 µF	Ceramic
	TPSC475K035R0600	4.7 µF	Tantalum
	TPSC156K020R0450	15 µF	Tantalum
	TPSC336K010R0375	33 µF	Tantalum
Sprague	595D475X0016A2T	4.7 µF	Tantalum
	595D156X06R3A2T	15 µF	Tantalum
	595D156X0016B2T	15 µF	Tantalum
	595D336X06R3A2T	33 µF	Tantalum
	595D336X0016B2T	33 µF	Tantalum
	595D336X0016C2T	33 µF	Tantalum
Kemet	T494B475M010AS	4.7 µF	Tantalum
	T494C156K010AS	15 µF	Tantalum
	T494C336K010AS	33 µF	Tantalum

Table 6 lists the manufacturers of recommended capacitors. In most applications surface-mount tantalum capacitors will be the right choice. However, ceramic capacitors will provide the lowest output voltage ripple due to their typically lower ESR.

Table 6. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET
Taiyo Yuden	X7R/X5R ceramic	www.t–yuden.com
AVX	X7R/X5R ceramic TPS–series tantalum	www.avxcorp.com
Sprague	595D–series tantalum 593D–series tantalum	www.vishay.com
Kemet	T494–series tantalum	www.kemet.com

power dissipation

The power dissipated in the TPS60111 depends on output current and is approximated by:

$$P_{DISS} = I_O \times (2\ V_{IN} - V_O) \text{ for } I_Q << I_O$$

P_{DISS} must be less than that allowed by the package rating. See the ratings for 20-PowerPAD™ package power-dissipation limits and deratings.

APPLICATION INFORMATION

layout

All capacitors should be soldered in close proximity to the IC. A PCB layout proposal for a two-layer board is given in Figure 29. Care has been taken to connect both single-ended charge pumps symmetrically to the load to achive optimized output voltage ripple performance. The proposed layout also provides improved thermal performance as the exposed leadframe is soldered to the PCB. The bottom layer of the PCB is a ground plain only. All ground areas on the PCB should be connected. Connect ground areas on top layer to the bottom layer via through hole connections.

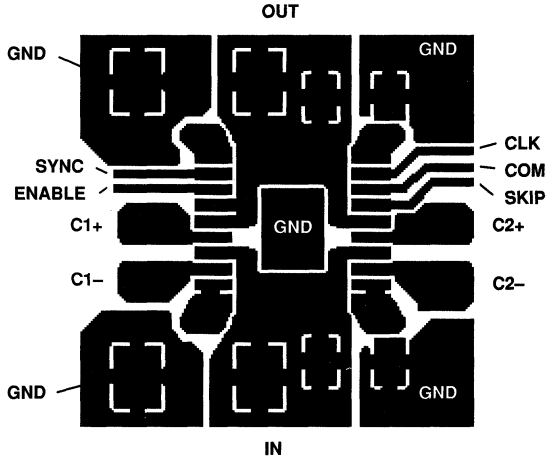


Figure 29. Recommended PCB Layout for TPS60111 (top view)

The evaluation module designed for the TPS60110 can, with slight modifications, be used for evaluation of the TPS60111. The EVM can be ordered under literature code SLVP132 or under product code TPS60110EVM–132.

APPLICATION INFORMATION

applications proposals

TPS60111 with LC output filter for ultra low ripple

For applications where extremely low output ripple is required, a small LC filter is recommended. This is shown in Figure 30. The addition of a small inductor and filter capacitor will reduce the output ripple well below what could be achieved with capacitors alone. The corner frequency of 500 kHz was chosen above the 300 kHz switching frequency to avoid loop stability issues in case the feedback is taken from the output of the LC filter. Leaving the feedback (FB) connection point before the LC filter, the filter capacitance value can be increased to achieve even higher ripple attenuation without affecting stability margin.

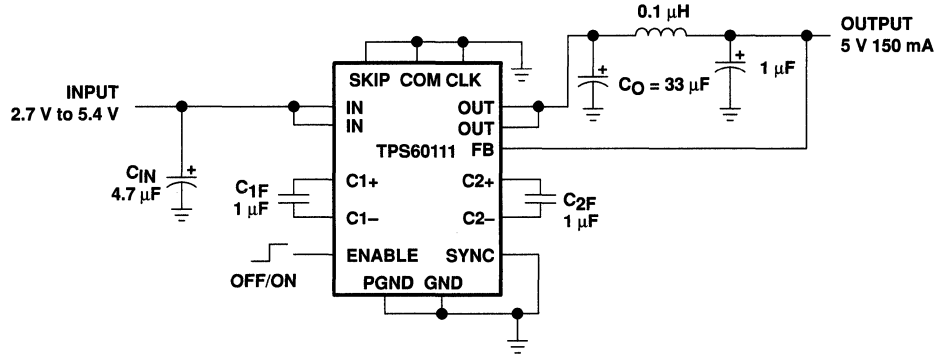


Figure 30. TPS60111 With LC Filter for Ultra Low Output Ripple Applications

related information

application reports

For more application information see:

- *PowerPAD™ Application Report* (Literature Number: SLMA002)
- *TPS6010x/TPS6011x Charge Pump Application Report* (Literature Number: SLVA070)

device family products

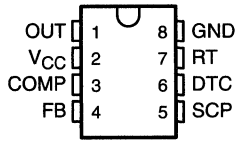
Other devices in this family are:

PART NUMBER	LITERATURE NUMBER	DESCRIPTION
TPS60100	SLVS213	Regulated 3.3-V, 200-mA Low-Noise Charge Pump DC/DC Converter
TPS60101	SLVS214	Regulated 3.3-V, 100-mA Low-Noise Charge Pump DC/DC Converter
TPS60110	SLVS215	Regulated 5-V, 300-mA Low-Noise Charge Pump DC/DC Converter

SLVS084D – APRIL 1994 – REVISED JUNE 1998

- **Complete PWM Power Control**
- **3.6-V to 40-V Operation**
- **Internal Undervoltage-Lockout Circuit**
- **Internal Short-Circuit Protection**
- **Oscillator Frequency . . . 20 kHz to 500 kHz**
- **Variable Dead Time Provides Control Over Total Range**
- **±3% Tolerance on Reference Voltage (TL5001A)**

D OR P PACKAGE
(TOP VIEW)



description

The TL5001 and TL5001A incorporates on a single monolithic chip all the functions required for a pulse-width-modulation (PWM) control circuit. Designed primarily for power-supply control, the TL5001/A contains an error amplifier, a regulator, an oscillator, a PWM comparator with a dead-time-control input, undervoltage lockout (UVLO), short-circuit protection (SCP), and an open-collector output transistor. The TL5001A has a reference voltage tolerance of ±3% compared to ±5% for the TL5001.

The error-amplifier common-mode voltage ranges from 0 V to 1.5 V. The noninverting input of the error amplifier is connected to a 1-V reference. Dead-time control (DTC) can be set to provide 0% to 100% dead time by connecting an external resistor between DTC and GND. The oscillator frequency is set by terminating RT with an external resistor to GND. During low V_{CC} conditions, the UVLO circuit turns the output off until V_{CC} recovers to its normal operating range.

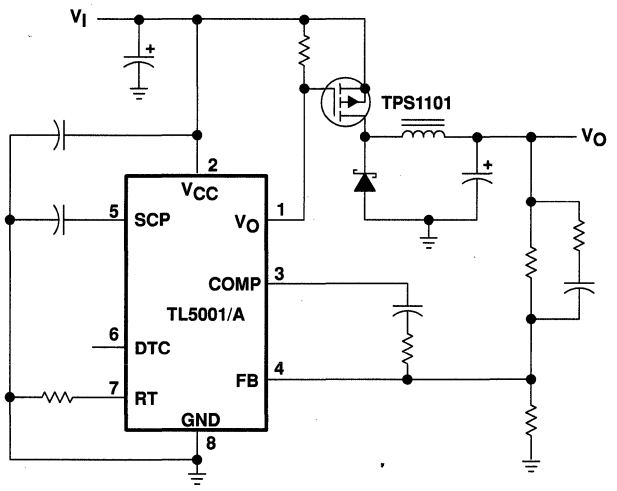
The TL5001C and TL5001AC are characterized for operation from –20°C to 85°C. The TL5001I and TL5001AI are characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

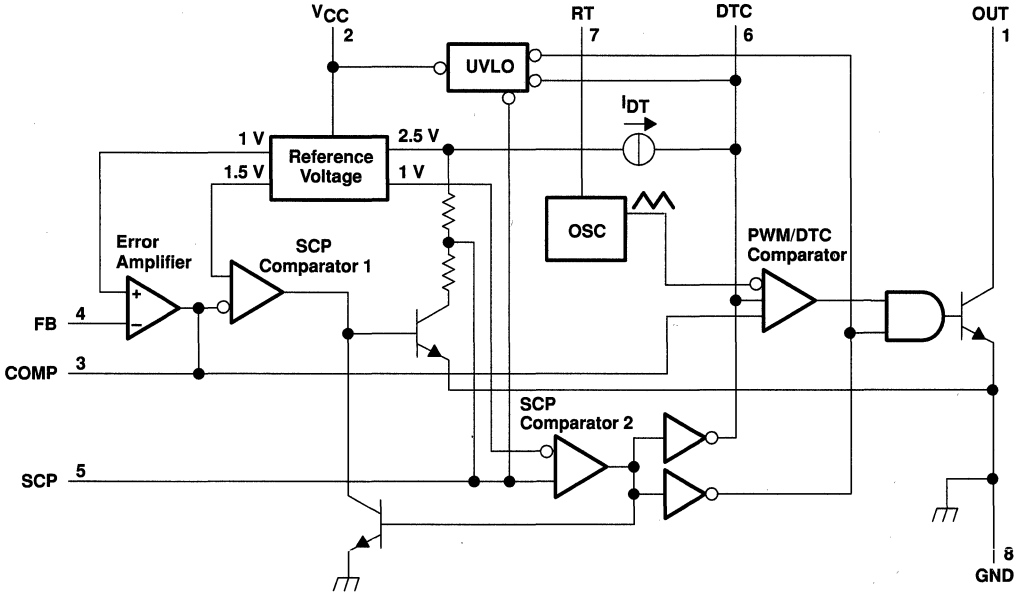
T_A	PACKAGED DEVICES		
	SMALL OUTLINE (D)	PLASTIC DIP (P)	CHIP FORM (Y)
–20°C to 85°C	TL5001CD	TL5001CP	TL5001Y
	TL5001ACD	TL5001ACP	—
–40°C to 85°C	TL5001ID	TL5001IP	—
	TL5001AID	TL5001AIP	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL5001CDR). Chip forms are tested at T_A = 25°C.

schematic for typical application



functional block diagram

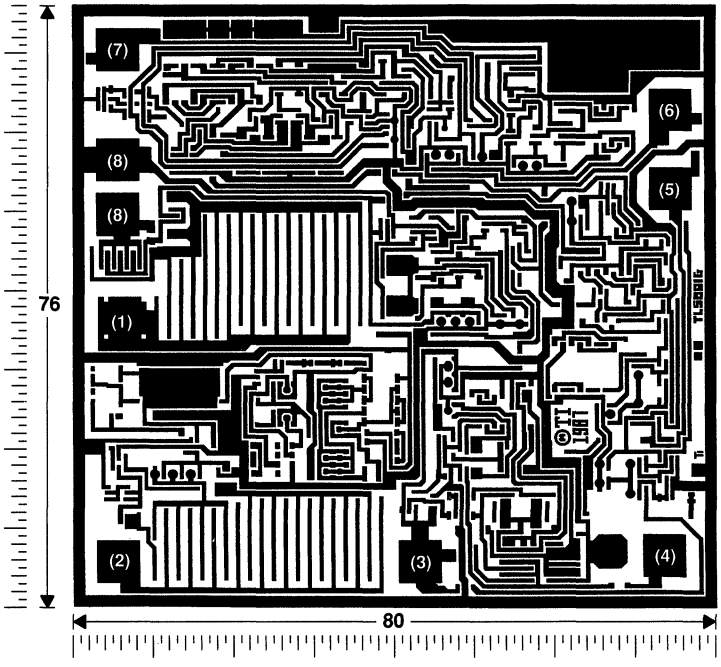


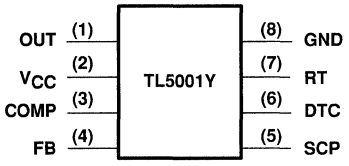
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TL5001Y chip information

This chip, when properly assembled, displays characteristics similar to the TL5001C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
11 MILS TYPICAL

BONDING PADS:
7X7 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

detailed description

voltage reference

A 2.5-V regulator operating from V_{CC} is used to power the internal circuitry of the TL5001 and TL5001A and as a reference for the error amplifier and SCP circuits. A resistive divider provides a 1-V reference for the error amplifier noninverting input. The TL5001 1-V reference remains within 5% of nominal over the operating temperature range. In the TL5001A, the 1-V reference remains within 3% of nominal.

error amplifier

The error amplifier compares a sample of the dc-to-dc converter output voltage to the 1-V reference and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

$$V_O = (1 + R1/R2)\ (1\ V)$$

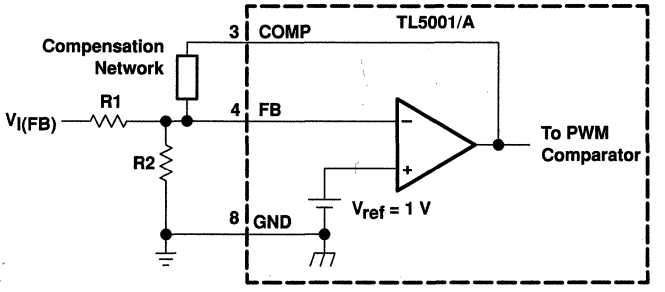


Figure 1. Error-Amplifier Gain Setting

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45 μA, the total dc load resistance should be 100 kΩ or more.

oscillator/PWM

The oscillator frequency (f_{osc}) can be set between 20 kHz and 500 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15 kΩ to 250 kΩ. The oscillator frequency can be determined by using the graph shown in Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

dead-time control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100%, which is critical for boost and flyback converters. A current source generates a reference current (I_{DT}) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a dead-time reference voltage (V_{DT}), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0% when V_{DT} is 0.7 V or less and 100% when V_{DT} is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250 Ω), choosing R_{DT} for a specific maximum duty cycle, D, is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 (V_{osc}max and V_{osc}min are the maximum and minimum oscillator levels):

dead-time control (DTC) (continued)

$$R_{DT} = \left(R_t + 1250\right)\left[D(V_{osc}max - V_{osc}min) + V_{osc}min\right]$$

where

R_{DT} and R_t are in ohms, D in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor (C_{DT}) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT}R_{DT}\left(1-e^{\left(-t/R_{DT}C_{DT}\right)}\right)$$

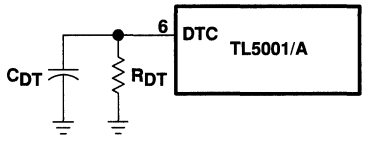


Figure 2. Soft-Start Circuit

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant, $R_{DT}C_{DT}$, should be $t_0/3$ to $t_0/5$. The TL5001/A remains off until $V_{DT} \approx 0.7$ V, the minimum ramp value. C_{DT} is discharged every time UVLO or SCP becomes active.

undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low (approximately 3 V) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

short-circuit protection (SCP)

The TL5001/A includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5 V. If the short is removed and the error-amplifier output drops below 1.5 V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns off the TL5001/A output transistor.

short-circuit protection (SCP) (continued)

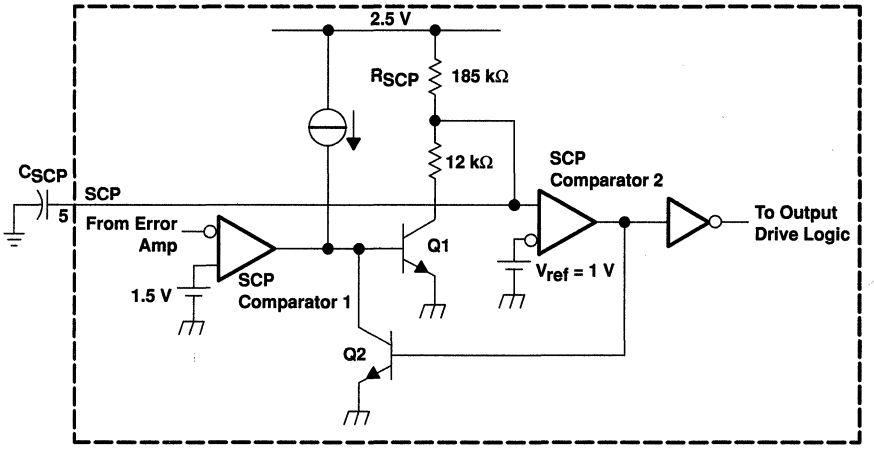


Figure 3. SCP Circuit

The timer operates by charging an external capacitor (C_{SCP}), connected between the SCP terminal and ground, towards 2.5 V through a 185-kΩ resistor (R_{SCP}). The circuit begins charging from an initial voltage of approximately 185 mV and times out when the capacitor voltage reaches 1 V. The output of SCP comparator 2 then goes high, turns on Q2, and latches the timer circuit. The expression for setting the SCP time period is derived from the following equation:

$$V_{SCP} = (2.5 - 0.185)\left(1 - e^{-t/\tau}\right) + 0.185$$

where

$$\tau = R_{SCP}C_{SCP}$$

The end of the time-out period, t_{SCP}, occurs when V_{SCP} = 1 V. Solving for C_{SCP} yields:

$$C_{SCP} = 12.46 \times t_{SCP}$$

where

t is in seconds, C in μF.

t_{SCP} must be much longer (generally 10 to 15 times) than the converter start-up period or the converter will not start.

output transistor

The output of the TL5001/A is an open-collector transistor with a maximum collector current rating of 21 mA and a voltage rating of 51 V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 41 V
Amplifier input voltage, $V_{I(FB)}$ ..... 20 V
Output voltage, V_O, OUT ..... 51 V
Output current, I_O, OUT ..... 21 mA
Output peak current, $I_{O(peak)}$, OUT ..... 100 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating ambient temperature range, T_A: TL5001C, TL5001AC ..... −20°C to 85°C
TL5001I, TL5001AI ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.6	40	V
Amplifier input voltage, $V_{I(FB)}$		0	1.5	V
Output voltage, V_O, OUT			50	V
Output current, I_O, OUT			20	mA
COMP source current			45	μA
COMP dc load resistance		100		kΩ
Oscillator timing resistor, R_t		15	250	kΩ
Oscillator frequency, f_{osc}		20	500	kHz
Operating ambient temperature, T_A	TL5001C, TL5001AC	−20	85	°C
	TL5001I, TL5001AI	−40	85	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted)

reference

PARAMETER	TEST CONDITIONS	TL5001			TL5001A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output voltage	COMP connected to FB	0.95	1	1.05	0.97	1	1.03	V
Input regulation	V_{CC} = 3.6 V to 40 V		2	12.5		2	12.5	mV
Output voltage change with temperature	T_A = −20°C to 25°C (C suffix)	−10	−1	10	−10	−1	10	mV/V
	T_A = −40°C to 25°C (I suffix)	−10	−1	10	−10	−1	10	
	T_A = 25°C to 85°C	−10	−2	10	−10	−2	10	

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

undervoltage lockout

PARAMETER	TEST CONDITIONS	TL5001			TL5001A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Upper threshold voltage	T_A = 25°C		3			3		V
Lower threshold voltage	T_A = 25°C		2.8			2.8		V
Hysteresis	T_A = 25°C	100	200		100	200		mV
Reset threshold voltage	T_A = 25°C	2.1	2.55		2.1	2.55		V

† All typical values are at T_A = 25°C.

short-circuit protection

PARAMETER	TEST CONDITIONS	TL5001			TL5001A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
SCP threshold voltage	T_A = 25°C	0.95	1.00	1.05	0.97	1.00	1.03	V
SCP voltage, latched	No pullup	140	185	230	140	185	230	mV
SCP voltage, UVLO standby	No pullup		60	120		60	120	mV
Input source current	T_A = 25°C	–10	–15	–20	–10	–15	–20	µA
SCP comparator 1 threshold voltage			1.5			1.5		V

† All typical values are at T_A = 25°C.

oscillator

PARAMETER	TEST CONDITIONS	TL5001			TL5001A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Frequency	R_t = 100 kΩ		100			100		kHz
Standard deviation of frequency			15			15		kHz
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1			1		kHz
Frequency change with temperature	T_A = –40°C to 25°C	–4	–0.4	4	–4	–0.4	4	kHz
	T_A = –20°C to 25°C	–4	–0.4	4	–4	–0.4	4	kHz
	T_A = 25°C to 85°C	–4	–0.2	4	–4	–0.2	4	kHz
Voltage at RT			1			1		V

† All typical values are at T_A = 25°C.

dead-time control

PARAMETER		TEST CONDITIONS	TL5001			TL5001A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Output (source) current	TL5001C	$V_{(DT)}$ = 1.5 V	0.9 × I_{RT}‡		1.1 × I_{RT}	0.9 × I_{RT}‡		1.1 × I_{RT}	µA
	TL5001I	$V_{(DT)}$ = 1.5 V	0.9 × I_{RT}‡		1.2 × I_{RT}	0.9 × I_{RT}‡		1.2 × I_{RT}	
Input threshold voltage		Duty cycle = 0%	0.5	0.7		0.5	0.7		V
		Duty cycle = 100%		1.3	1.5		1.3	1.5	

† All typical values are at T_A = 25°C.
‡ Output source current at RT

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

error amplifier

PARAMETER		TEST CONDITIONS	TL5001			TL5001A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Input voltage		V_{CC} = 3.6 V to 40 V	0		1.5	0		1.5	V
Input bias current				−160	−500		−160	−500	nA
Output voltage swing	Positive		1.5	2.3		1.5	2.3		V
	Negative			0.3	0.4		0.3	0.4	V
Open-loop voltage amplification				80			80		dB
Unity-gain bandwidth				1.5			1.5		MHz
Output (sink) current		$V_{I(FB)}$ = 1.2 V, COMP = 1 V	100	600		100	600		µA
Output (source) current		$V_{I(FB)}$ = 0.8 V, COMP = 1 V	−45	−70		−45	−70		µA

† All typical values are at T_A = 25°C.

output

PARAMETER	TEST CONDITIONS	TL5001			TL5001A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output saturation voltage	I_O = 10 mA		1.5	2		1.5	2	V
Off-state current	V_O = 50 V, V_{CC} = 0			10			10	µA
	V_O = 50 V			10			10	
Short-circuit output current	V_O = 6 V		40			40		mA

† All typical values are at T_A = 25°C.

total device

PARAMETER		TEST CONDITIONS	TL5001			TL5001A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Standby supply current	Off state			1	1.5		1	1.5	mA
Average supply current		R_t = 100 kΩ		1.4	2.1		1.4	2.1	mA

† All typical values are at T_A = 25°C.

electrical characteristics, V_{CC} = 6 V, f_{osc} = 100 kHz, T_A = 25°C (unless otherwise noted)

reference

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Output voltage	COMP connected to FB		1		V
Input regulation	V_{CC} = 3.6 V to 40 V		2		mV
Output voltage change with temperature			–2		mV/V

undervoltage lockout

PARAMETER	TL5001Y			UNIT
	MIN	TYP	MAX	
Upper threshold voltage		3		V
Lower threshold voltage		2.8		V
Hysteresis		200		mV
Reset threshold voltage		2.55		V

short-circuit protection

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
SCP threshold voltage			1		V
SCP voltage, latched	No pullup		185		mV
SCP voltage, UVLO standby	No pullup		60		mV
Input source current			–15		μA
SCP comparator 1 threshold voltage			1.5		V

oscillator

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Frequency	R_t = 100 kΩ		100		kHz
Standard deviation of frequency			15		kHz
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1		kHz
Frequency change with temperature			–0.4		kHz
			–0.2		
Voltage at RT			1		V

dead-time control

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Input threshold voltage	Duty cycle = 0%		0.7		V
	Duty cycle = 100%		1.3		

electrical characteristics, V_{CC} = 6 V, f_{osc} = 100 kHz, T_A = 25°C (unless otherwise noted) (continued)

error amplifier

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Input bias current			–160		nA

Output voltage swing	Positive		2.3	V
	Negative		0.3	V
Open-loop voltage amplification			80	dB
Unity-gain bandwidth			1.5	MHz
Output (sink) current		$V_{I(FB)}$ = 1.2 V, COMP = 1 V	600	μA
Output (source) current		$V_{I(FB)}$ = 0.8 V, COMP = 1 V	−70	μA

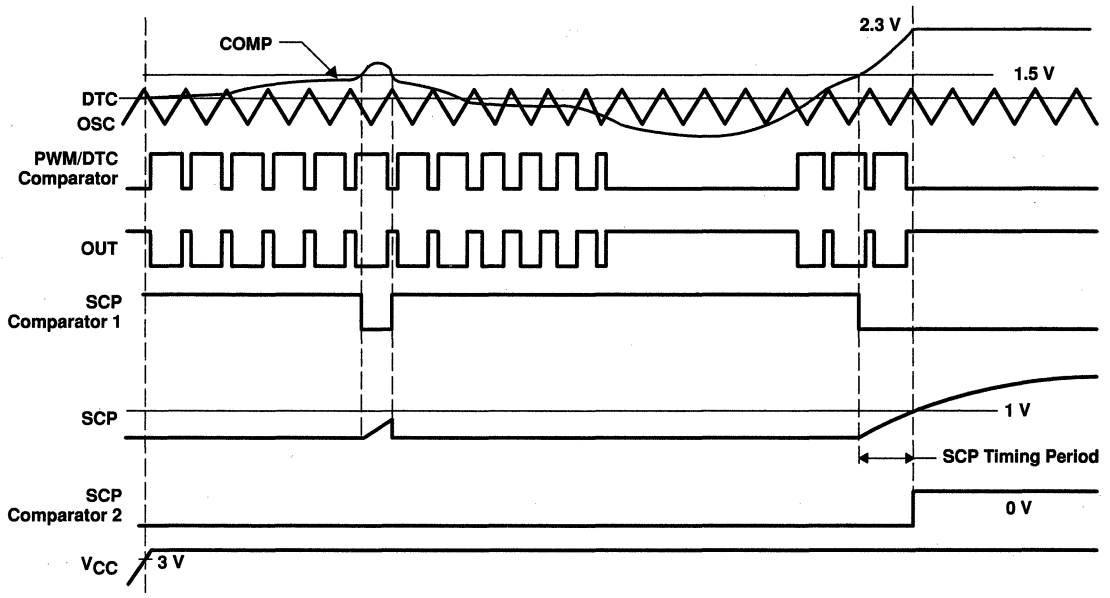
output

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Output saturation voltage	I_O = 10 mA		1.5		V
Short-circuit output current	V_O = 6 V		40		mA

total device

PARAMETER		TEST CONDITIONS	TL5001Y			UNIT
			MIN	TYP	MAX	
Standby supply current	Off state			1		mA
Average supply current		R_t = 100 kΩ		1.4		mA

PARAMETER MEASUREMENT INFORMATION



NOTE A. The waveforms show timing characteristics for an intermittent short circuit and a longer short circuit that is sufficient to activate SCP.

Figure 4. PWM Timing Diagram

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY
vs
TIMING RESISTANCE

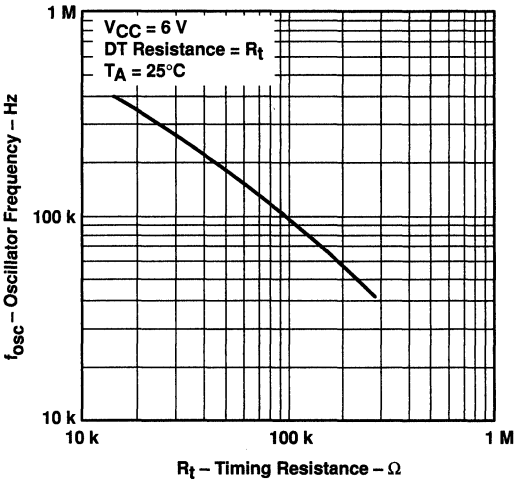


Figure 5

OSCILLATION FREQUENCY
vs
AMBIENT TEMPERATURE

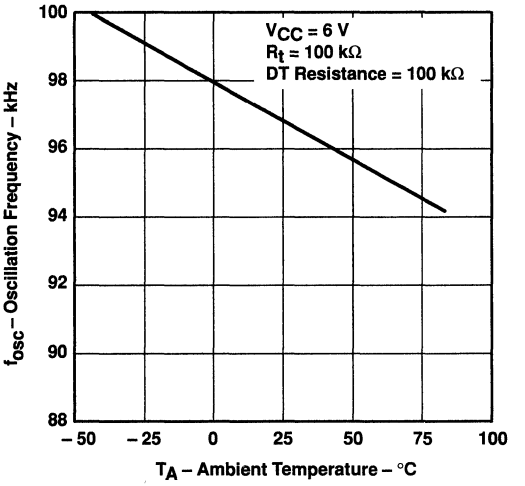


Figure 6

REFERENCE OUTPUT VOLTAGE
vs
POWER-SUPPLY VOLTAGE

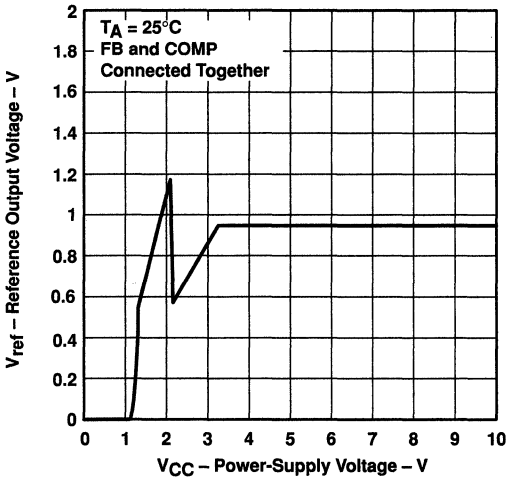


Figure 7

REFERENCE OUTPUT VOLTAGE FLUCTUATION
vs
AMBIENT TEMPERATURE

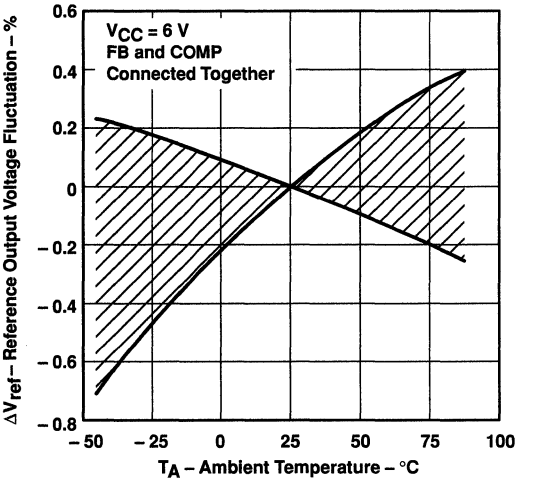


Figure 8

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
POWER-SUPPLY VOLTAGE

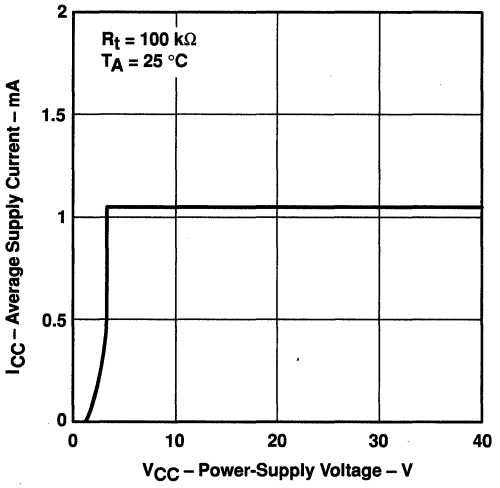


Figure 9

AVERAGE SUPPLY CURRENT
vs
AMBIENT TEMPERATURE

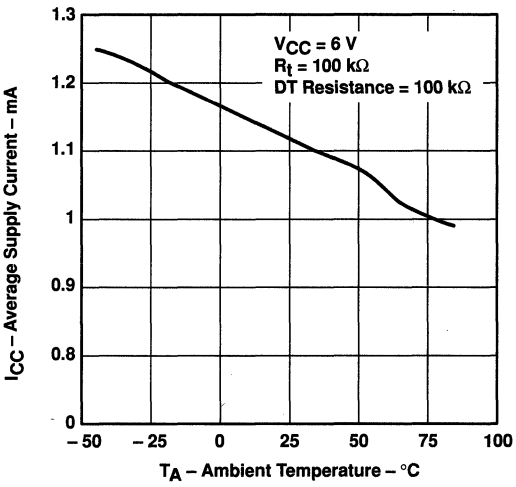


Figure 10

PWM TRIANGLE WAVE AMPLITUDE VOLTAGE
vs
OSCILLATOR FREQUENCY

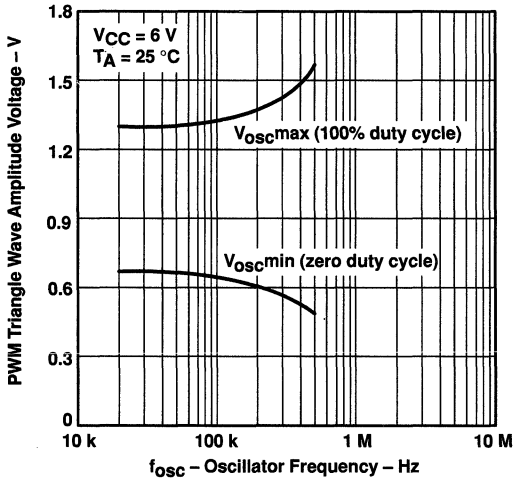


Figure 11

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
OUTPUT (SINK) CURRENT

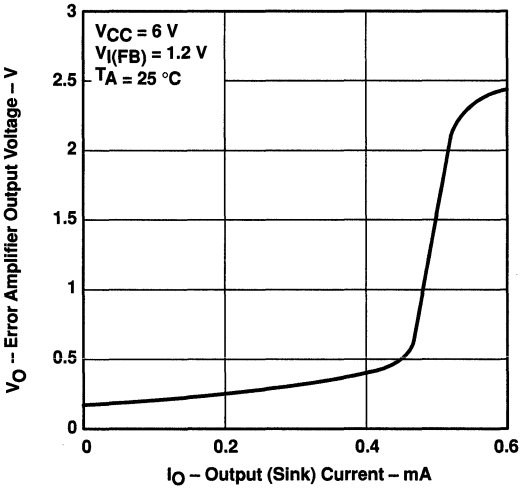


Figure 12

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
OUTPUT (SOURCE) CURRENT

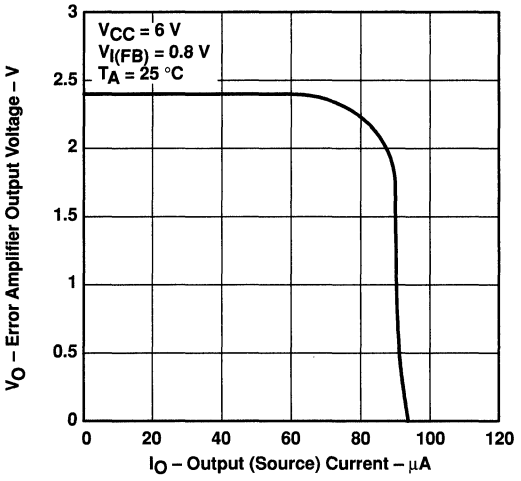


Figure 13

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
AMBIENT TEMPERATURE

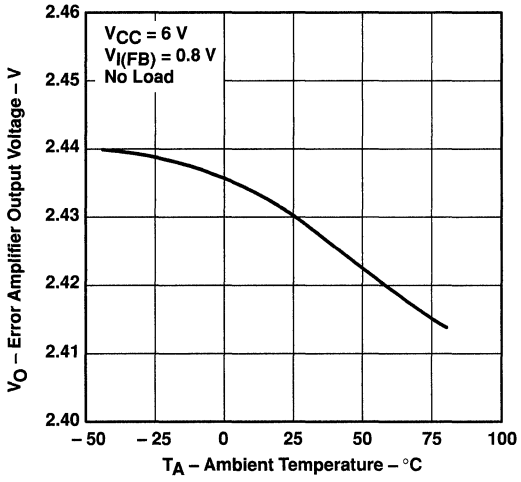


Figure 14

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
AMBIENT TEMPERATURE

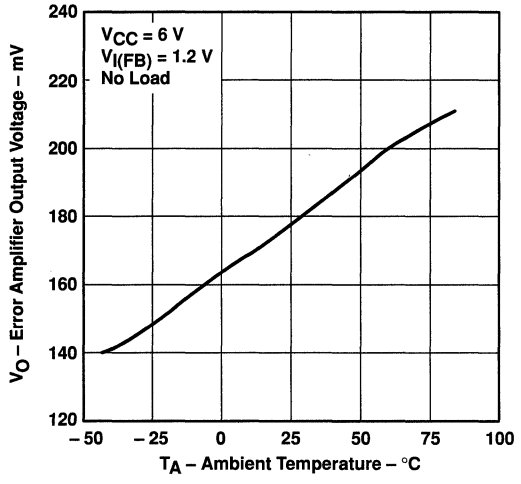


Figure 15

ERROR AMPLIFIER CLOSED-LOOP GAIN AND
PHASE SHIFT
vs
OSCILLATOR FREQUENCY

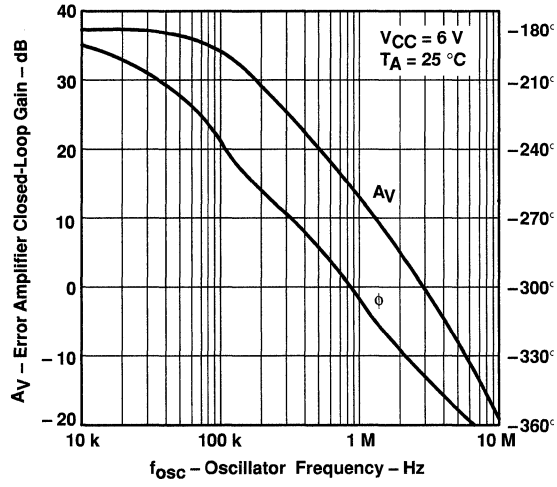


Figure 16

TYPICAL CHARACTERISTICS

OUTPUT DUTY CYCLE
vs
DTC VOLTAGE

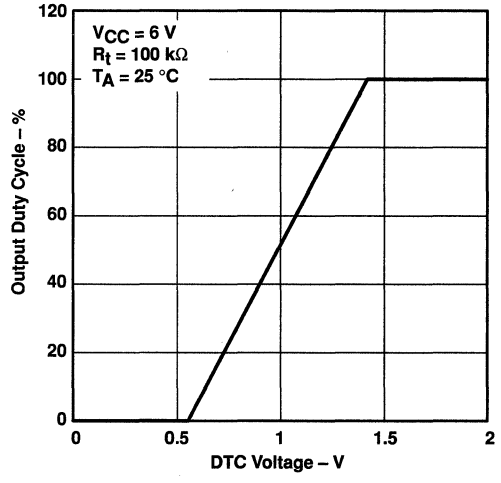


Figure 17

SCP TIME-OUT PERIOD
vs
SCP CAPACITANCE

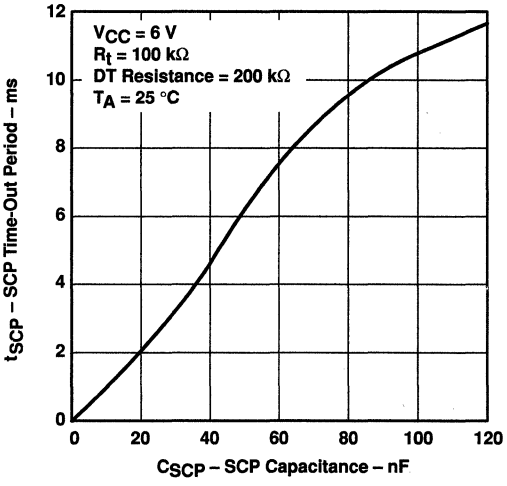


Figure 18

DTC OUTPUT CURRENT
vs
RT OUTPUT CURRENT

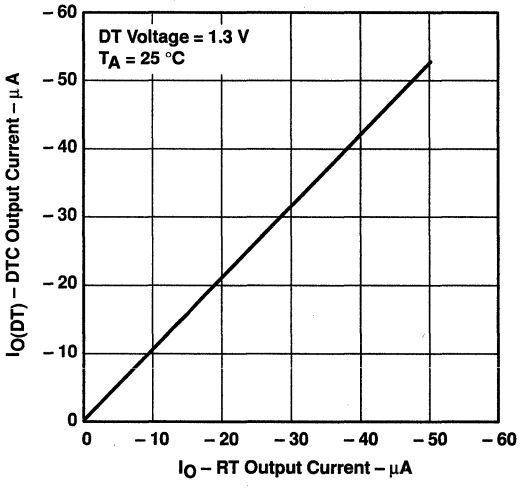


Figure 19

OUTPUT SATURATION VOLTAGE
vs
OUTPUT (SINK) CURRENT

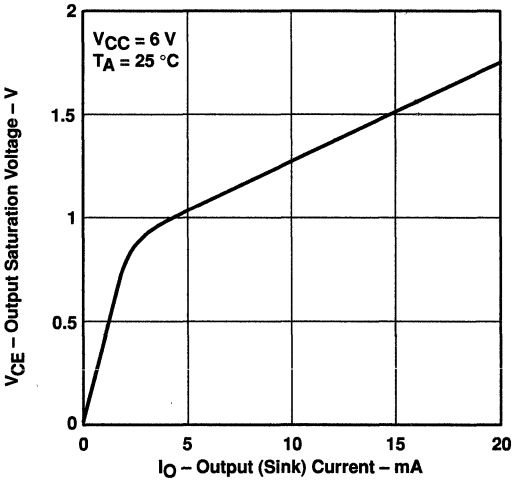
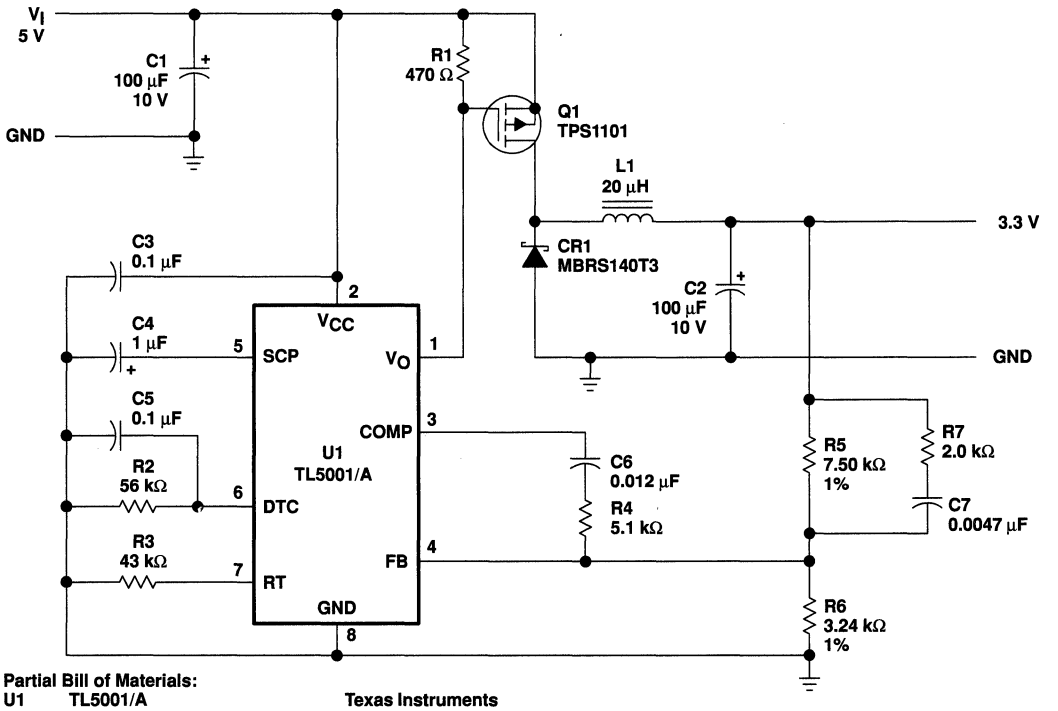


Figure 20

APPLICATION INFORMATION



Partial Bill of Materials:

U1	TL5001/A	Texas Instruments
Q1	TPS1101	Texas Instruments
LI	CTX20-1 or 23 turns of #28 wire on Micrometals No. T50-26B core	Coiltronics
C1	TPSD107M010R0100	AVX
C2	TPSD107M010R0100	AVX
CR1	MBRS140T3	Motorola

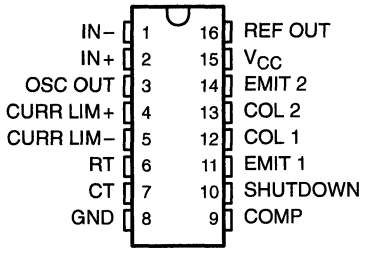
NOTES: A. Frequency = 200 kHz
B. Duty cycle = 90% max
C. Soft-start time constant (TC) = 5.6 ms
D. SCP TC = 70 msA

Figure 21. Step-Down Converter

SLVS077B – APRIL 1977 – REVISED JULY 1999

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for Single-Ended or Push-Pull Applications**
- **Low Standby Current . . . 8 mA Typ**
- **Interchangeable With Silicon General SG2524 and SG3524**

D OR N PACKAGE
(TOP VIEW)



description

The SG2524 and SG3524 incorporate all the functions required in the construction of a regulating power supply, inverter, or switching regulator on a single chip. They also can be used as the control element for high-power-output applications. The SG2524 and SG3524 were designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers, and polarity converter applications employing fixed-frequency, pulse-width-modulation (PWM) techniques. The complementary output allows either single-ended or push-pull application. Each device includes an on-chip regulator, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted pass transistors, a high-gain comparator, and current-limiting and shut-down circuitry.

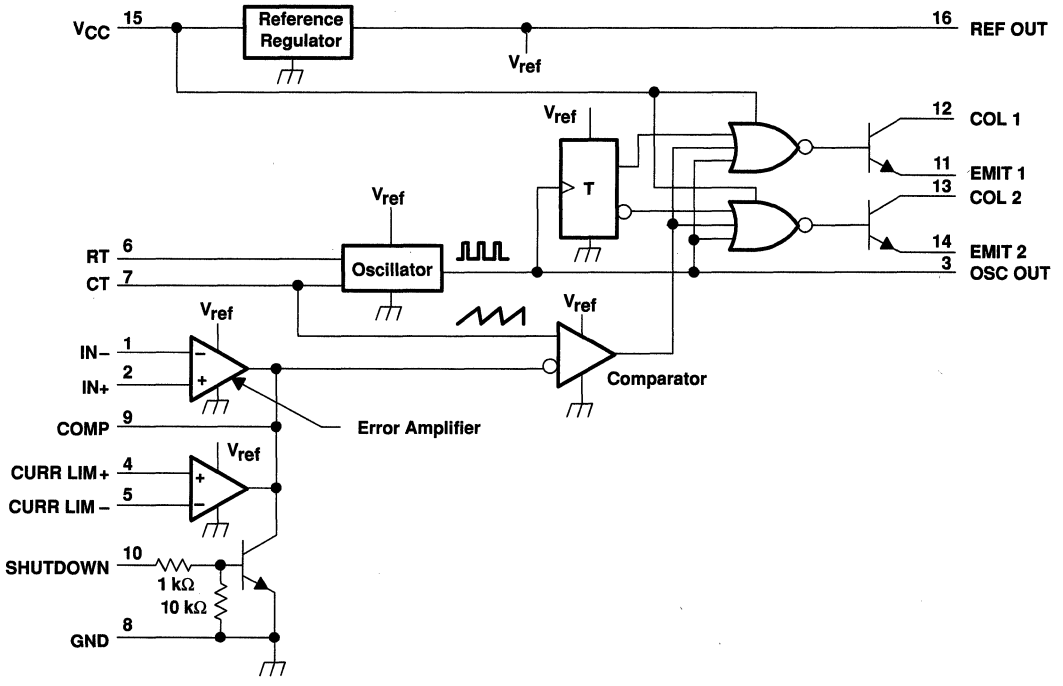
The SG2524 is characterized for operation from –25°C to 85°C, and the SG3524 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	INPUT REGULATION MAX (MV)	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	
0°C to 70°C	30	SG3524D	SG3524N	SG3524Y
–25°C to 85°C	20	SG2524D	SG2524N	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., SG3524DR). Chip forms are tested at 25°C.

functional block diagram



NOTE A. Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Notes 1 and 2)	40 V
Collector output current, I_{CC}	100 mA
Reference output current, $I_{O(ref)}$	50 mA
Current through CT terminal	−5 mA
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D package	112°C/W
N package	88°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The reference regulator may be bypassed for operation from a fixed 5-V supply by connecting the V_{CC} and reference output pin both to the supply voltage. In this configuration, the maximum supply voltage is 6 V.
3. Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operation at the absolute maximum T_J of 150°C can impact reliability.
4. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages which use a trace length of zero.

recommended operating conditions

	SG2524		SG3524		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	8	40	8	40	V
Reference output current	0	50	0	50	mA
Current through CT terminal	−0.03	−2	−0.03	−2	mA
Timing resistor, R_T	1.8	100	1.8	100	kΩ
Timing capacitor, C_T	0.001	0.1	0.001	0.1	μF
Operating free-air temperature	−25	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	SG2524			SG3524			SG3524Y			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage		4.8	5	5.2	4.6	5	5.4		5		V
Input regulation	V_{CC} = 8 V to 40 V		10	20		10	30		10		mV
Ripple rejection	f = 120 Hz		66			66			66		dB
Output regulation	I_O = 0 mA to 20 mA		20	50		20	50		20		mV
Output voltage change with temperature	T_A = MIN to MAX		0.3%	1%		0.3%	1%				
Short-circuit output current§	V_{ref} = 0		100			100			100		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C
§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

oscillator section

PARAMETER		TEST CONDITIONS†	SG2524, SG3524			SG3524Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{osc}	Oscillator frequency	C_T = 0.001 µF, R_T = 2 kΩ		450			450		kHz
	Standard deviation of frequency§	All values of voltage, temperature, resistance, and capacitance constant		5%			5%		
Δf_{osc}	Frequency change with voltage	V_{CC} = 8 V to 40 V, T_A = 25°C			1%			1%	
	Frequency change with temperature	T_A = MIN to MAX			2%				
	Output amplitude at OSC OUT	T_A = 25°C		3.5			3.5		V
t_w	Output pulse duration (width) at OSC OUT	C_T = 0.01 µF, T_A = 25°C		0.5			0.5		µs

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C
§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

error amplifier section

PARAMETER		TEST CONDITIONS†	SG2524			SG3524			SG3524Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{IC} = 2.5 V		0.5	5		2	10		2		mV
I_{IB}	Input bias current	V_{IC} = 2.5 V		2	10		2	10		2		µA
	Open-loop voltage amplification		72	80		60	80			80		dB
V_{ICR}	Common-mode input voltage range	T_A = 25°C	1.8 to 3.4			1.8 to 3.4						V
CMMR	Common-mode rejection ratio			70			70			70		dB
B_1	Unity-gain bandwidth			3			3			3		MHz
	Output swing	T_A = 25°C	0.5		3.8	0.5		3.8	0.5		3.8	V

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS†	SG2534, SG3524			SG3524Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{(BR)CE}$	Collector-emitter breakdown voltage		40						V
	Collector off-state current	V_{CE} = 40 V		0.01	50		0.01		μA
V_{sat}	Collector-emitter saturation voltage	I_C = 50 mA		1	2		1		V
V_O	Emitter output voltage	V_C = 20 V, I_E = −250 μA	17	18			18		V
t_r	Turn-off voltage rise time	R_C = 2 kΩ		0.2			0.2		μs
t_f	Turn-on voltage fall time	R_C = 2 kΩ		0.1			0.1		μs

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C.

comparator section

PARAMETER		TEST CONDITIONS†	SG2534, SG3524			SG3524Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
	Maximum duty cycle, each output		45%						
V_{IT}	Input threshold voltage at COMP	Zero duty cycle		1			1		V
		Maximum duty cycle		3.5			3.5		
I_{IB}	Input bias current			−1			−1		μA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at T_A = 25°C.

current limiting section

PARAMETER		TEST CONDITIONS	SG2524			SG3524			SG3524Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_I	Input voltage range (either input)		−1 to 1			−1 to 1						V
$V_{(SENSE)}$	Sense voltage at T_A = 25°C	$V_{(IN+)} - V_{(IN-)} \geq 50$ mV, $V_{(COMP)}$ = 2 V	175	200	225	175	200	225	175	200	225	mV
	Temperature coefficient of sense voltage			0.2			0.2			0.2		mV/°C

‡ All typical values, except for temperature coefficients, are at T_A = 25°C.

total device

PARAMETER		TEST CONDITIONS	SG2524, SG3524			SG3524Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
I_{st}	Standby current	V_{CC} = 40 V, IN−, CURR LIM+, C_T, GND, COMP, EMIT 1, EMIT 2 grounded, IN+ at 2 V, All other inputs and outputs open		8	10		8		mA

‡ All typical values, except for temperature coefficients, are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

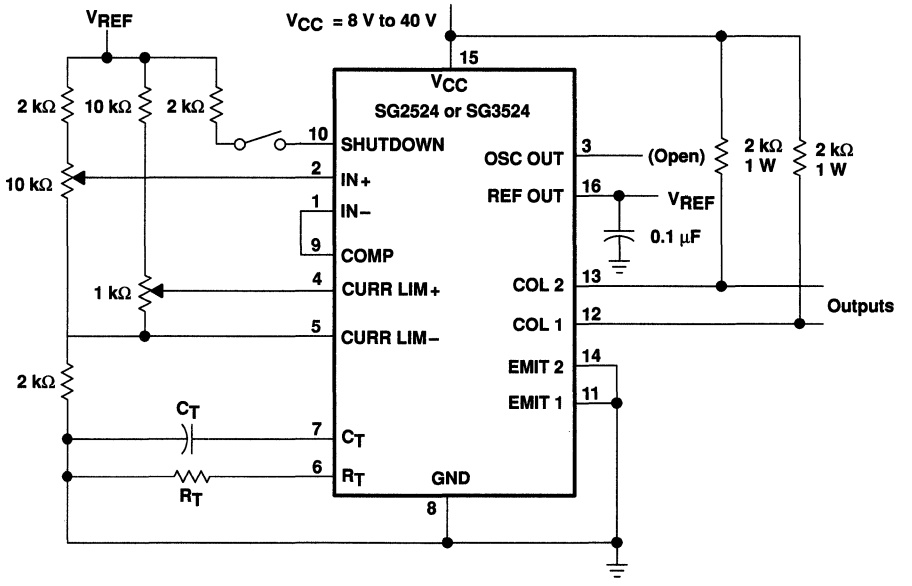


Figure 1. General Test Circuit

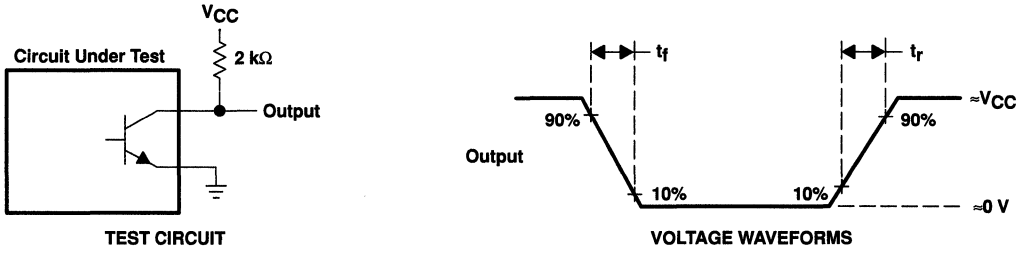


Figure 2. Switching Times

TYPICAL CHARACTERISTICS

OPEN-LOOP VOLTAGE AMPLIFICATION
OF ERROR AMPLIFIER
vs
FREQUENCY

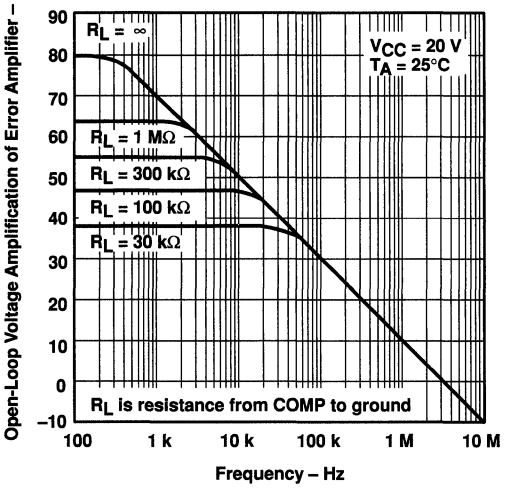


Figure 3

OSCILLATOR FREQUENCY
vs
TIMING RESISTANCE

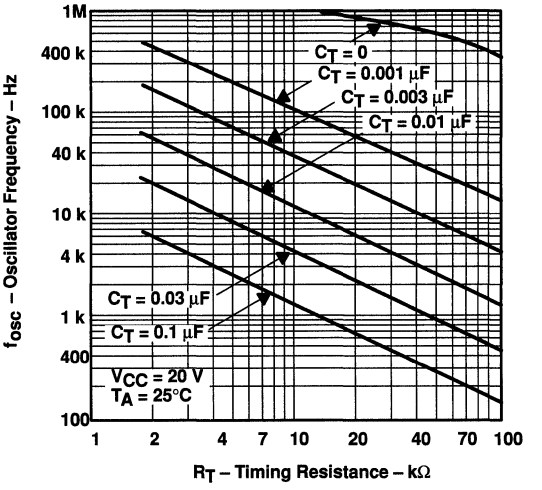


Figure 4

OUTPUT DEAD TIME
vs
TIMING CAPACITANCE

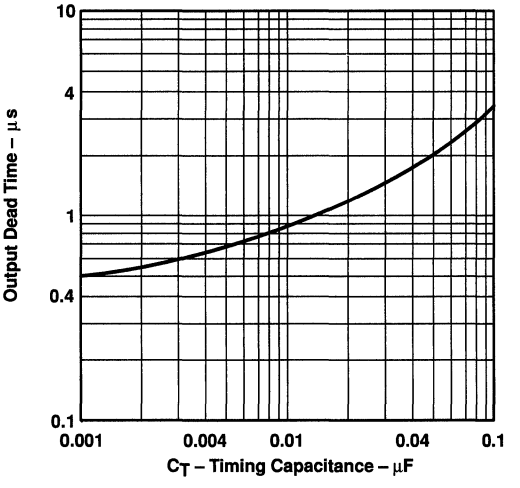


Figure 5

PRINCIPLES OF OPERATION†

The SG2524 is a fixed-frequency pulse-width-modulation voltage-regulator control circuit. The regulator operates at a fixed frequency that is programmed by one timing resistor, R_T, and one timing capacitor, C_T. R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse duration (width) by the error amplifier. The SG2524 contains an onboard 5-V regulator that serves as a reference, as well as supplying the SG2524 internal regulator control circuitry. The internal reference voltage is divided externally by a resistor ladder network to provide a reference within the common-mode range of the error amplifier as shown in Figure 6, or an external reference can be used. The output is sensed by a second resistor divider network and the error signal is amplified. This voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q1 or Q2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to ensure both outputs are never on simultaneously during the transition times. The duration of the blanking pulse is controlled by the value of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current-limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point also is available externally and can be employed to control the gain of, to compensate the error amplifier, or to provide additional control to the regulator.

APPLICATION INFORMATION†

oscillator

The oscillator controls the frequency of the SG2524 and is programmed by R_T and C_T as shown in Figure 4.

$$f \approx \frac{1.30}{R_T C_T}$$

where: R_T is in kΩ
C_T is in μF
f is in kHz

Practical values of C_T fall between 0.001 and 0.1 μF. Practical values of R_T fall between 1.8 and 100 kΩ. This results in a frequency range typically from 130 Hz to 722 kHz.

blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse duration is controlled by the value of C_T as shown in Figure 5. If small values of C_T are required, the oscillator output pulse duration can still be maintained by applying a shunt capacitance from OSC OUT to ground.

synchronous operation

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kΩ. In this configuration, $R_T C_T$ must be selected for a clock period slightly greater than that of the external clock.

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

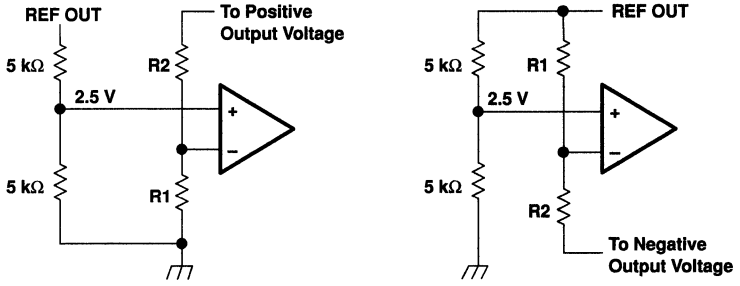
APPLICATION INFORMATION†

synchronous operation (continued)

If two or more SG2524 regulators are operated synchronously, all oscillator output terminals must be tied together. The oscillator programmed for the minimum clock period is the master from which all the other SG2524s operate. In this application, the $C_T R_T$ values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, C_T (master) = 2 C_T (slave) to ensure that the master output pulse, which occurs first, has a longer pulse duration and subsequently resets the slave regulators.

voltage reference

The 5-V internal reference can be employed by use of an external resistor divider network to establish a reference common-mode voltage range (1.8 V to 3.4 V) within the error amplifiers as shown in Figure 6, or an external reference can be applied directly to the error amplifier. For operation from a fixed 5-V supply, the internal reference can be bypassed by applying the input voltage to both the V_{CC} and V_{REF} terminals. In this configuration, however, the input voltage is limited to a maximum of 6 V.



$$V_O = 2.5\,V \frac{R1 + R2}{R1} \qquad V_O = 2.5\,V \left(1 - \frac{R2}{R1}\right)$$

Figure 6. Error-Amplifier Bias Circuits

error amplifier

The error amplifier is a differential-input transconductance amplifier. The output is available for dc gain control or ac phase compensation. The compensation node (COMP) is a high-impedance node (R_L = 5 MΩ). The gain of the amplifier is $A_V = (0.002\ \Omega^{-1})R_L$ and can easily be reduced from a nominal 10,000 by an external shunt resistance from COMP to ground. Refer to Figure 3 for data.

compensation

COMP, as discussed above, is made available for compensation. Since most output filters introduce one or more additional poles at frequencies below 200 Hz, which is the pole of the uncompensated amplifier, introduction of a zero to cancel one of the output filter poles is desirable. This can best be accomplished with a series RC circuit from COMP to ground in the range of 50 kΩ and 0.001 µF. Other frequencies can be canceled by use of the formula $f \approx 1/RC$.

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

shut-down circuitry

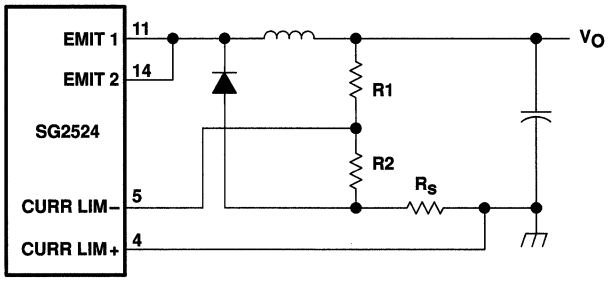
COMP can also be employed to introduce external control of the SG2524. Any circuit that can sink 200 μA can pull the compensation terminal to ground and thus disable the SG2524.

In addition to constant-current limiting, CURR LIM+ and CURR LIM– may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse should transformer saturation occur. CURR LIM– may also be grounded to convert CURR LIM+ into an additional shut-down terminal.

current limiting

A current-limiting sense amplifier is provided in the SG2524. The current-limiting sense amplifier exhibits a threshold of 200 mV ±25 mV and must be applied in the ground line since the voltage range of the inputs is limited to 1 V to –1 V. Caution should be taken to ensure the –1 V limit is not exceeded by either input, otherwise damage to the device may result.

Foldback current limiting can be provided with the network shown in Figure 7. The current-limit schematic is shown in Figure 8.



$$I_{O(max)} = \frac{1}{R_S}\left(200\ mV + \frac{V_O\ R2}{R1 + R2}\right)$$

$$I_{OS} = \frac{200\ mV}{R_S}$$

Figure 7. Foldback Current Limiting for Shorted Output Conditions

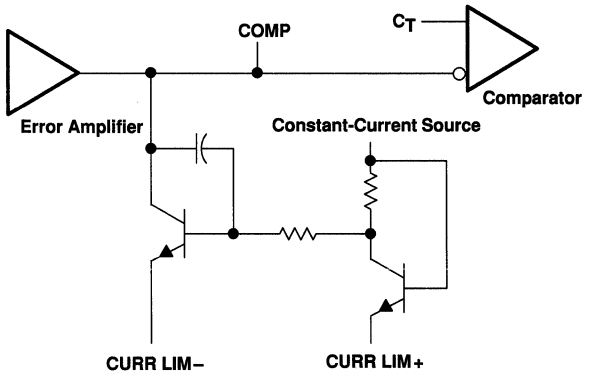


Figure 8. Current-Limit Schematic

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

output circuitry

The SG2524 contains two identical npn transistors, the collectors and emitters of which are uncommitted. Each transistor has antisaturation circuitry that limits the current through that transistor to a maximum of 100 mA for fast response.

general

There are a wide variety of output configurations possible when considering the application of the SG2524 as a voltage regulator control circuit. They can be segregated into three basic categories:

1. Capacitor-diode-coupled voltage multipliers
2. Inductor-capacitor-implemented single-ended circuits
3. Transformer-coupled circuits

Examples of these categories are shown in Figures 9, 10 and 11 respectively. Detailed diagrams of specific applications are shown in Figures 12 through 15.

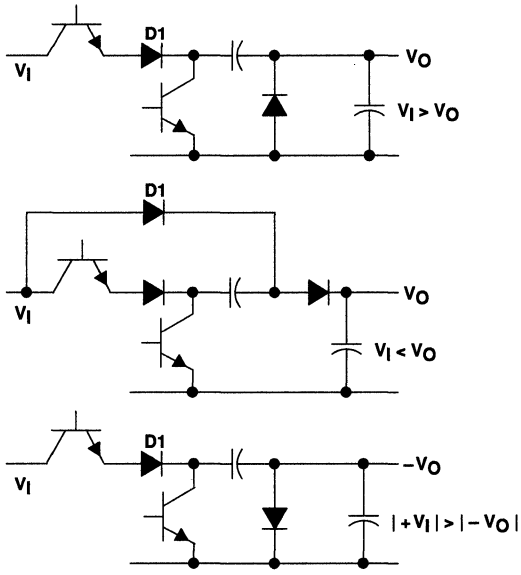


Figure 9. Capacitor-Diode-Coupled Voltage-Multiplier Output Stages

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

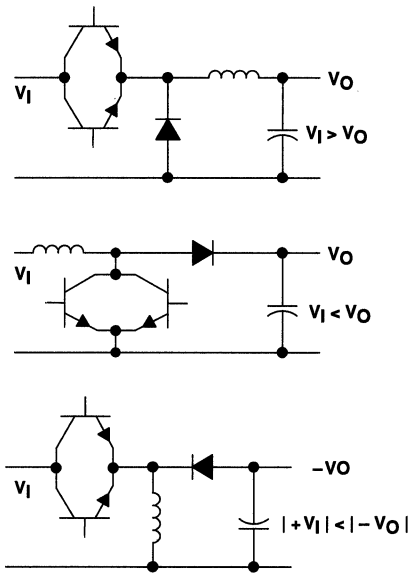


Figure 10. Single-Ended Inducor Circuit

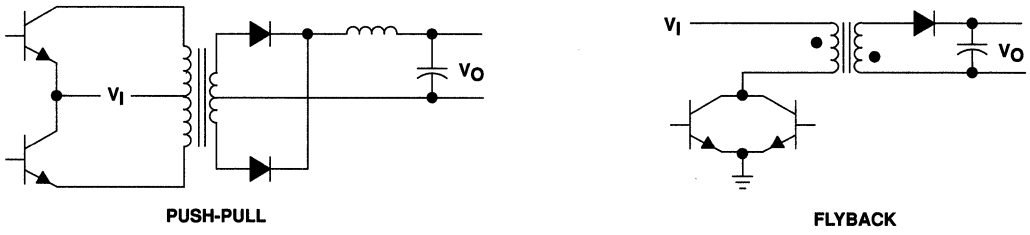


Figure 11. Transformer-Coupled Outputs

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

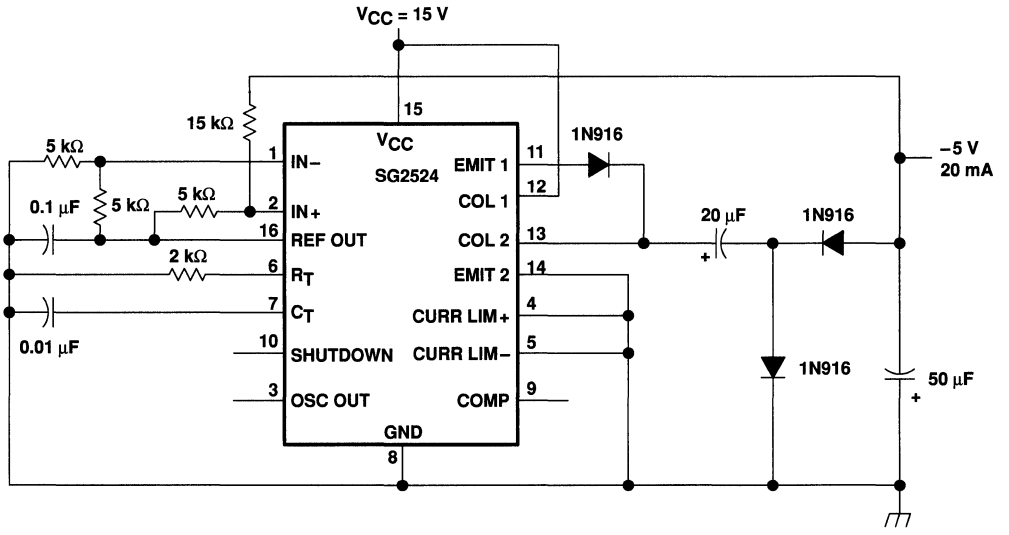


Figure 11. Capacitor-Diode Output Circuit

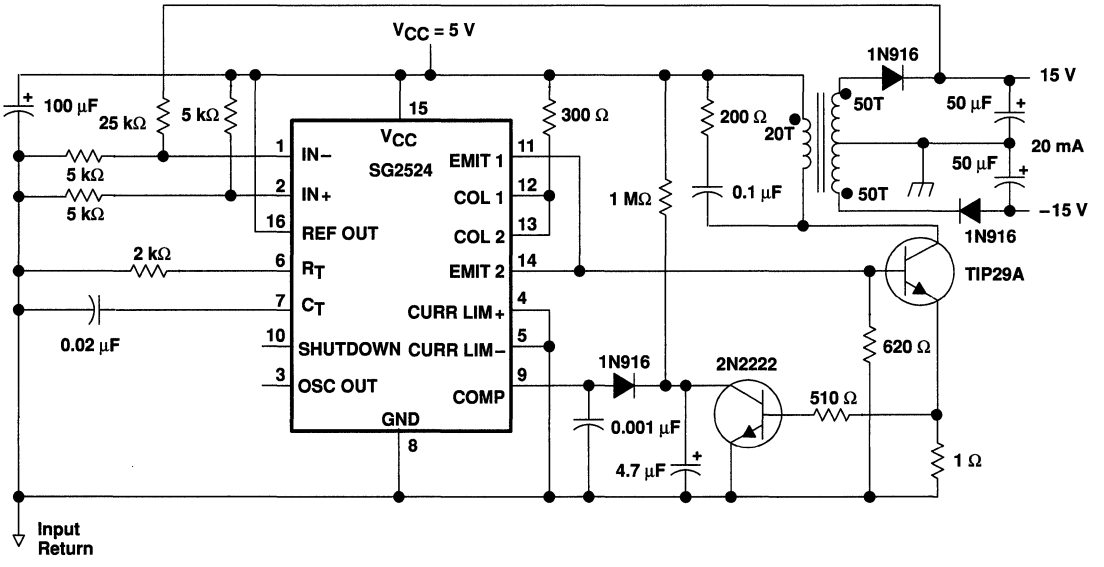


Figure 12. Flyback Converter Circuit

†Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

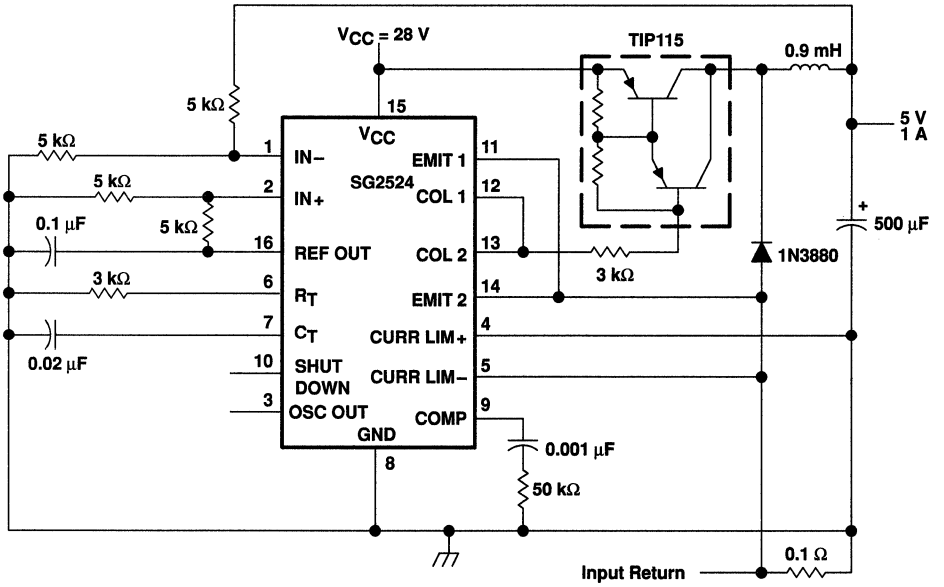


Figure 13. Single-Ended LC Circuit

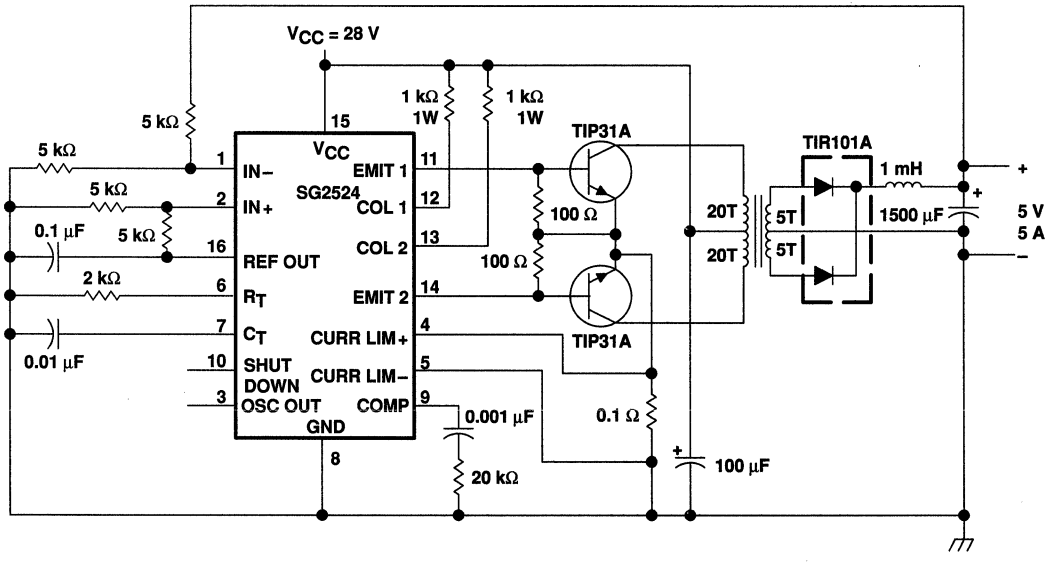


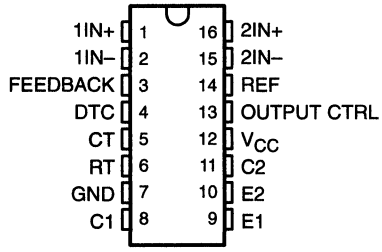
Figure 14. Push-Pull Transformer-Coupled Circuit

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

SLVS074B – JANUARY 1983 – REVISED JULY 1999

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance**
- **Circuit Architecture Allows Easy Synchronization**

D, N, NS, OR PW PACKAGE
(TOP VIEW)



description

The TL494 incorporates all the functions required in the construction of a pulse-width-modulation (PWM) control circuit on a single chip. Designed primarily for power-supply control, this device offers the flexibility to tailor the power-supply control circuitry to a specific application.

The TL494 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from –0.3 V to V_{CC} – 2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can drive the common circuits in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 provides for push-pull or single-ended output operation, which can be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL494C is characterized for operation from 0°C to 70°C. The TL494I is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

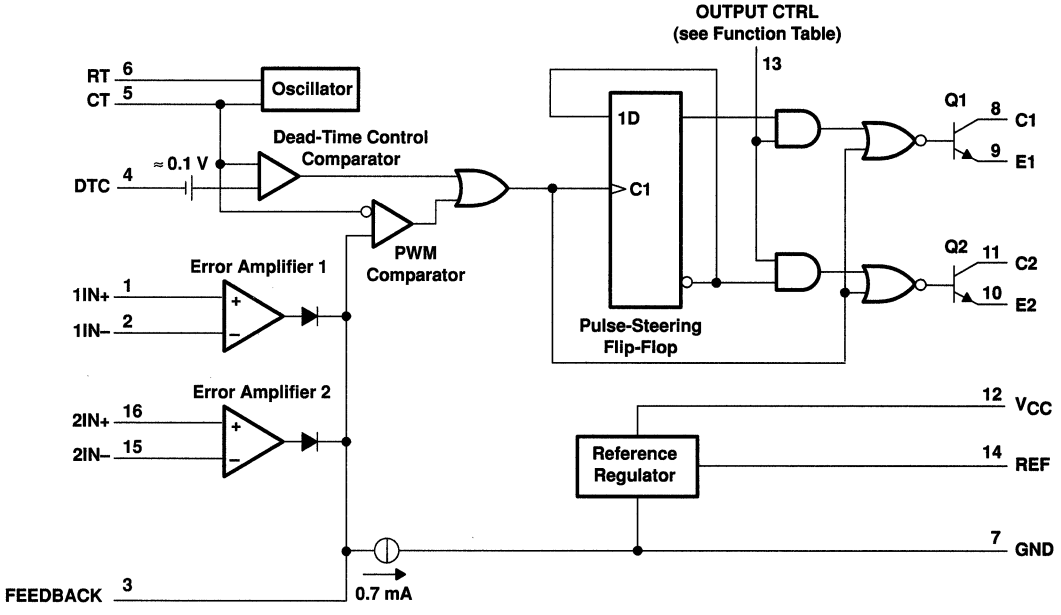
INPUT TO OUTPUT CTRL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
V_I = V_{ref}	Normal push-pull operation

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES				CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (N)	SMALL OUTLINE (NS)	SHRINK SMALL OUTLINE (PW)	
0°C to 70°C	TL494CD	TL494CN	TL494CNS	TL494CPW	TL494Y
–40°C to 85°C	TL494ID	TL494IN	—	—	—

The D, NS, and PW packages are available taped and reeled. Add the suffix R to device type (e.g., TL494CDR). Chip forms are tested at 25°C.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		TL494	UNIT
Supply voltage, V_{CC} (see Note 1)		41	V
Amplifier input voltage, V_I		V_{CC}+0.3	V
Collector output voltage, V_O		41	V
Collector output current, I_O		250	mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3)	D package	73	°C
	N package	88	
	NS package	64	
	PW package	108	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or PW package	260	°C
Storage temperature range, T_{stg}		–65 to 150	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		TL494		UNIT
		MIN	MAX	
Supply voltage, V_{CC}		7	40	V
Amplifier input voltage, V_I		–0.3	V_{CC}–2	V
Collector output voltage, V_O			40	V
Collector output current (each transistor)			200	mA
Current into feedback terminal			0.3	mA
Oscillator frequency, f_{osc}		1	300	kHz
Timing capacitor, C_T		0.47	10000	nF
Timing resistor, R_T		1.8	500	kΩ
Operating free-air temperature, T_A	TL494C	0	70	°C
	TL494I	–40	85	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	TL494C, TL494I			UNIT
		MIN	TYP‡	MAX	
Output voltage (REF)	I_O = 1 mA	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V		2	25	mV
Output regulation	I_O = 1 mA to 10 mA		1	15	mV
Output voltage change with temperature	ΔT_A = MIN to MAX		2	10	mV/V
Short-circuit output current§	REF = 0 V		25		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for parameter changes with temperature, are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.

oscillator section, C_T = 0.01 μF, R_T = 12 kΩ (see Figure 1)

PARAMETER	TEST CONDITIONS†	TL494, TL494I			UNIT
		MIN	TYP‡	MAX	
Frequency			10		kHz
Standard deviation of frequency¶	All values of V_{CC}, CT, RT, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1		Hz/kHz
Frequency change with temperature#	ΔT_A = MIN to MAX			10	Hz/kHz

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for parameter changes with temperature, are at T_A = 25°C.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

Temperature coefficient of timing capacitor and timing resistor are not taken into account.

error-amplifier section (see Figure 2)

PARAMETER	TEST CONDITIONS		TL494, TL494I			UNIT
			MIN	TYP‡	MAX	
Input offset voltage	V_O (FEEDBACK) = 2.5 V			2	10	mV
Input offset current	V_O (FEEDBACK) = 2.5 V			25	250	nA
Input bias current	V_O (FEEDBACK) = 2.5 V			0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V		–0.3 to V_{CC}–2			V
Open-loop voltage amplification	ΔV_O = 3 V, R_L = 2 kΩ,	V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V,	R_L = 2 kΩ		800		kHz
Common-mode rejection ratio	ΔV_O = 40 V, T_A = 25°C		65	80		dB
Output sink current (FEEDBACK)	V_{ID} = –15 mV to –5 V,	V (FEEDBACK) = 0.7 V	0.3	0.7		mA
Output source current (FEEDBACK)	V_{ID} = 15 mV to 5 V,	V (FEEDBACK) = 3.5 V	–2			mA

‡ All typical values, except for parameter changes with temperature, are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz, T_A = 25°C (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	TL494Y			UNIT
		MIN	TYP†	MAX	
Output voltage (REF)	I_O = 1 mA		5		V
Input regulation	V_{CC} = 7 V to 40 V		2		mV
Output regulation	I_O = 1 mA to 10 mA		1		mV
Short-circuit output current‡	REF = 0 V		25		mA

† All typical values, except for parameter changes with temperature, are at T_A = 25°C.
‡ Duration of the short circuit should not exceed one second.

oscillator section, C_T = 0.01 μF, R_T = 12 kΩ (see Figure 1)

PARAMETER	TEST CONDITIONS†	TL494Y			UNIT
		MIN	TYP†	MAX	
Frequency			10		kHz
Standard deviation of frequency§	All values of V_{CC}, CT, RT, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V		1		Hz/kHz

† All typical values, except for parameter changes with temperature, are at T_A = 25°C.
§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

error-amplifier section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL494Y			UNIT
		MIN	TYP†	MAX	
Input offset voltage	V_O (FEEDBACK) = 2.5 V		2		mV
Input offset current	V_O (FEEDBACK) = 2.5 V		25		nA
Input bias current	V_O (FEEDBACK) = 2.5 V		0.2		μA
Open-loop voltage amplification	ΔV_O = 3 V, R_L = 2 kΩ, V_O = 0.5 V to 3.5 V		95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		800		kHz
Common-mode rejection ratio	ΔV_O = 40 V		80		dB
Output sink current (FEEDBACK)	V_{ID} = –15 mV to –5 V, V (FEEDBACK) = 0.7 V		0.7		mA

† All typical values, except for parameter changes with temperature, are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS		TL494, TL494Y			UNIT
				MIN	TYP†	MAX	
Collector off-state current		V_{CE} = 40 V,	V_{CC} = 40 V		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40 V,	V_E = 0			–100	μA
Collector-emitter saturation voltage	Common emitter	V_E = 0,	I_C = 200 mA		1.1	1.3	V
	Emitter follower	$V_{O(C1 \text{ or } C2)}$ = 15 V,	I_E = –200 mA		1.5	2.5	
Output control input current		V_I = V_{ref}				3.5	mA

† All typical values except for temperature coefficient are at T_A = 25°C.

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS	TL494, TL494Y			UNIT
		MIN	TYP†	MAX	
Input bias current (DEAD-TIME CTRL)	V_I = 0 to 5.25 V		–2	–10	μA
Maximum duty cycle, each output	V_I (DEAD-TIME CTRL) = 0, C_T = 0.1 μF, R_T = 12 kΩ		45%		
Input threshold voltage (DEAD-TIME CTRL)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

† All typical values except for temperature coefficient are at T_A = 25°C.

PWM comparator section (see Figure 1)

PARAMETER	TEST CONDITIONS	TL494, TL494Y			UNIT
		MIN	TYP†	MAX	
Input threshold voltage (FEEDBACK)	Zero duty cycle		4	4.5	V
Input sink current (FEEDBACK)	V (FEEDBACK) = 0.7 V	0.3	0.7		mA

† All typical values except for temperature coefficient are at T_A = 25°C.

total device

PARAMETER	TEST CONDITIONS		TL494, TL494Y			UNIT
			MIN	TYP†	MAX	
Standby supply current	RT = V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		6	10	mA
		V_{CC} = 40 V		9	15	
Average supply current	V_I (DEAD-TIME CTRL) = 2 V,	See Figure 1		7.5		mA

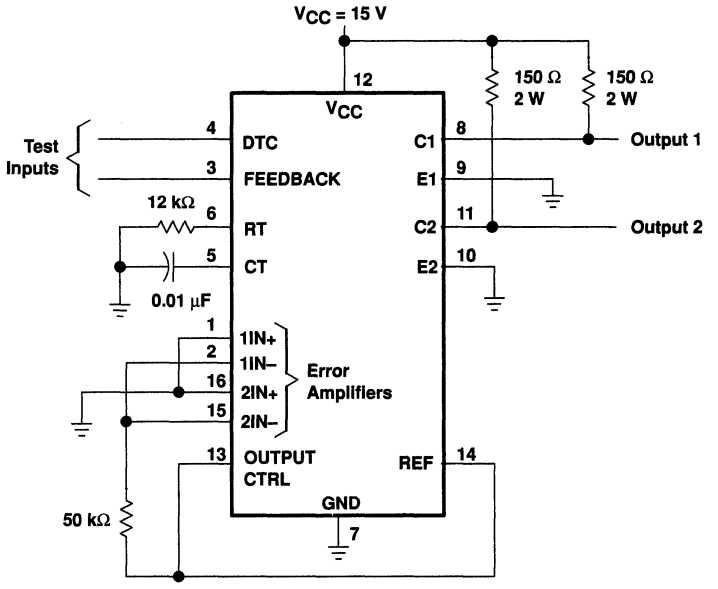
† All typical values except for temperature coefficient are at T_A = 25°C.

switching characteristics, T_A = 25°C

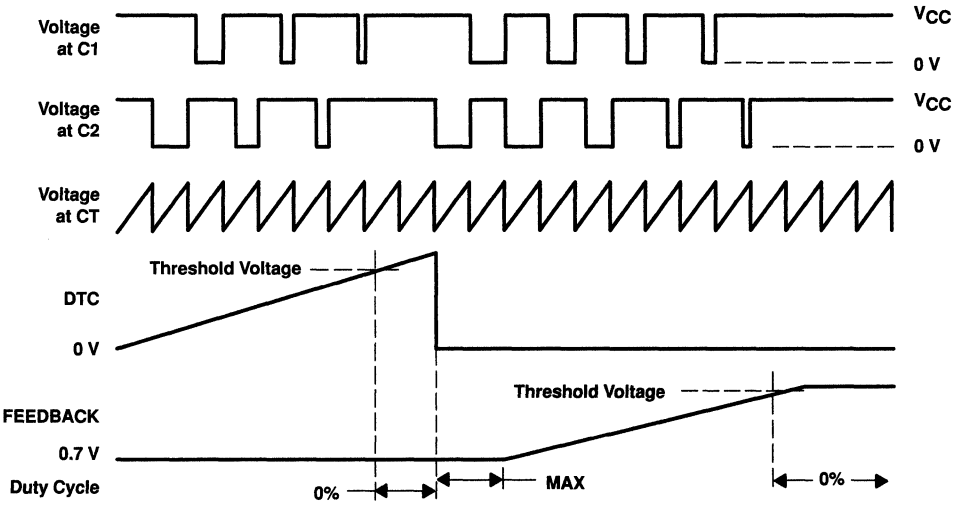
PARAMETER	TEST CONDITIONS		TL494, TL494Y			UNIT
			MIN	TYP†	MAX	
Rise time	Common-emitter configuration,	See Figure 3		100	200	ns
Fall time				25	100	ns
Rise time	Emitter-follower configuration,	See Figure 4		100	200	ns
Fall time				40	100	ns

† All typical values except for temperature coefficient are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 1. Operational Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

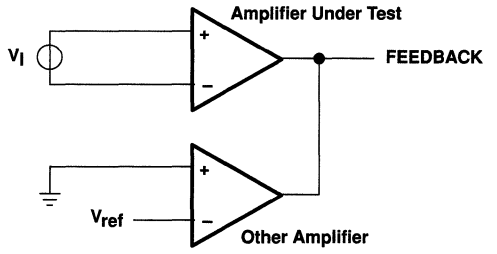
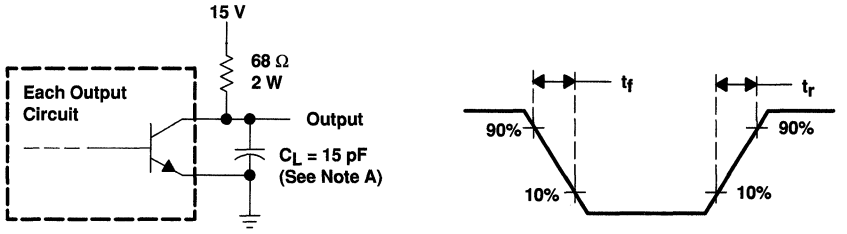
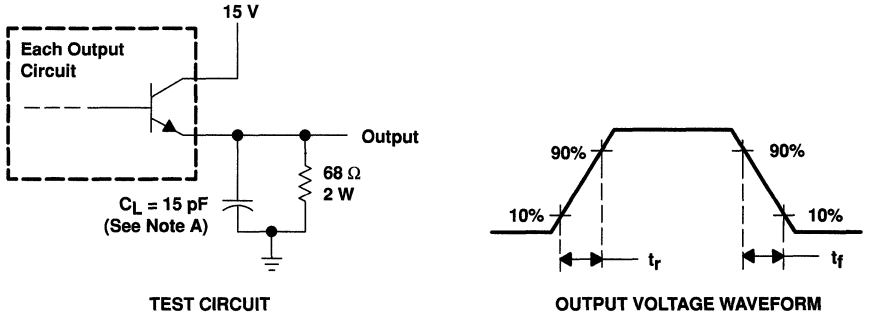


Figure 2. Amplifier Characteristics



NOTE A. C_L includes probe and jig capacitance.

Figure 3. Common-Emitter Configuration

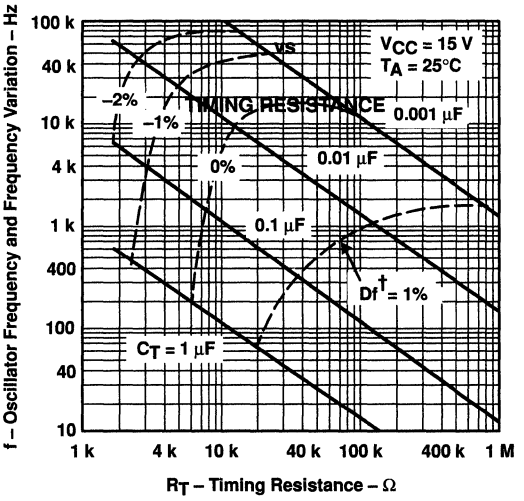


NOTE A. C_L includes probe and jig capacitance.

Figure 4. Emitter-Follower Configuration

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION†



† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

Figure 5

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

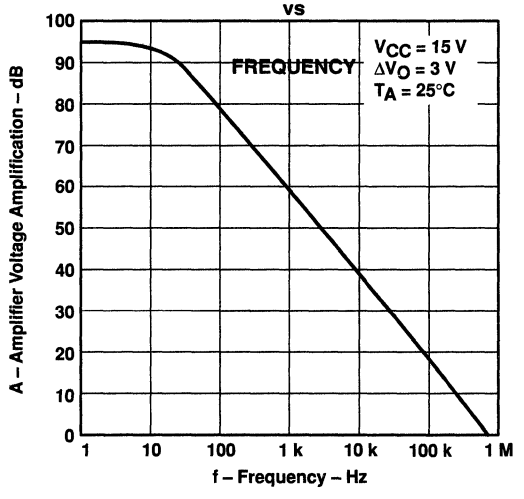
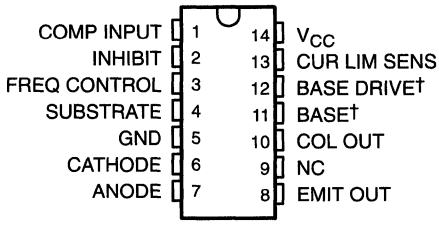


Figure 6

SLVS009D – JUNE 1976 – REVISED JULY 1999

- **High Efficiency . . . 60% or Greater**
- **Output Current . . . 500 mA**
- **Input Current Limit Protection**
- **TTL-Compatible Inhibit**
- **Adjustable Output Voltage**
- **Input Regulation . . . 0.2% Typ**
- **Output Regulation . . . 0.4% Typ**
- **Soft Start-Up Capability**

D, N, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection
† BASE (11) and BASE DRIVE (12) are used for device testing only. They normally are not used in circuit applications of the device.

description

The TL497A incorporates all the active functions required in the construction of switching voltage regulators. It can also be used as the control element to drive external components for high-power-output applications. The TL497A was designed for ease of use in step-up, step-down, or voltage-inversion applications requiring high efficiency.

The TL497A is a fixed-on-time variable-frequency switching-voltage-regulator control circuit. The switch-on time is programmed by a single external capacitor connected between FREQ CONTROL and GND. This capacitor, C_T, is charged by an internal constant-current generator to a predetermined threshold. The charging current and the threshold vary proportionally with V_{CC}. Thus, the switch-on time remains constant over the specified range of input voltage (4.5 V to 12 V). Typical on times for various values of C_T are as follows:

TIMING CAPACITOR, C_T (pF)	200	250	350	400	500	750	1000	1500	2000
ON TIME (μs)	19	22	26	32	44	56	80	120	180

The output voltage is controlled by an external resistor ladder network (R1 and R2 in Figures 1, 2, and 3) that provides a feedback voltage to the comparator input. This feedback voltage is compared to the reference voltage of 1.2 V (relative to SUBSTRATE) by the high-gain comparator. When the output voltage decays below the value required to maintain 1.2 V at the comparator input, the comparator enables the oscillator circuit, which charges and discharges C_T as described above. The internal pass transistor is driven on during the charging of C_T. The internal transistor can be used directly for switching currents up to 500 mA. Its collector and emitter are uncommitted, and it is current driven to allow operation from the positive supply voltage or ground. An internal Schottky diode matched to the current characteristics of the internal transistor also is available for blocking or commutating purposes. The TL497A also has on-chip current-limit circuitry that senses the peak currents in the switching regulator and protects the inductor against saturation and the pass transistor against overstress. The current limit is adjustable and is programmed by a single sense resistor, R_{CL}, connected between V_{CC} and CUR LIM SENS. The current-limit circuitry is activated when 0.7 V is developed across R_{CL}. External gating is provided by the INHIBIT input. When the INHIBIT input is high, the output is turned off.

Simplicity of design is a primary feature of the TL497A. With only six external components (three resistors, two capacitors, and one inductor), the TL497A operates in numerous voltage-conversion applications (step-up, step-down, invert) with as much as 85% of the source power delivered to the load. The TL497A replaces the TL497 in all applications.

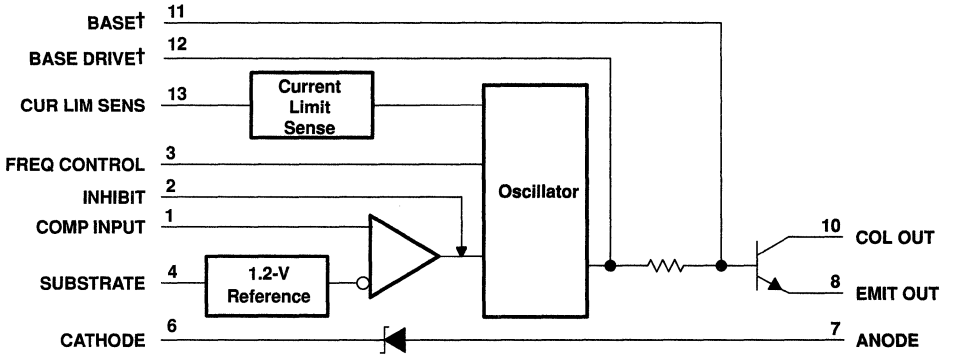
The TL497AC is characterized for operation from 0°C to 70°C. The TL497AI is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL-OUTLINE (D)	PLASTIC DIP (N)	SHRINK SMALL-OUTLINE (PW)	
0°C to 70°C	TL497ACD	TL497ACN	TL497ACPW	TL497AY
–40°C to 85°C	TL497AID	TL497AIN	—	—

The D and PW packages are only taped and reeled. Add the suffix R to the device type (e.g., TL497ACPWR). Chip forms are tested at 25°C.

functional block diagram



† BASE and BASE DRIVE are used for device testing only. They normally are not used in circuit applications of the device.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 15 V
Output voltage, V_O ..... 35 V
Input voltage, V_I(COMP INPUT) ..... 5 V
Input voltage, V_I(INHIBIT) ..... 5 V
Diode reverse voltage ..... 35 V
Power switch current ..... 750 mA
Diode forward current ..... 750 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package ..... 86°C/W
N package ..... 101°C/W
PW package ..... 113°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except diode voltages are with respect to network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{CC}			4.5	12	V
High-level input voltage, V_{IH}	INHIBIT pin		2.5		V
Low-level input voltage, V_{IL}	INHIBIT pin			0.8	V
Output voltage	Step-up configuration (see Figure 1)		$V_I + 2$	30	V
	Step-down configuration (see Figure 2)		V_{ref}	$V_I - 1$	
	Inverting regulator (see Figure 3)		$-V_{ref}$	–25	
Power switch current				500	mA
Diode forward current				500	mA
Operating free-air temperature range, T_A		TL497AC	0	70	°C
		TL497AI	–40	85	

electrical characteristics over recommended operating conditions, V_{CC} = 6 V (unless otherwise noted)

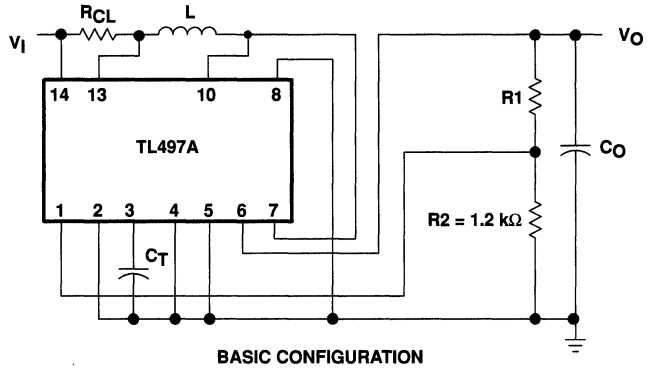
PARAMETER	TEST CONDITIONS		T_A†	TL497AC			TL497AI			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
High-level input current, INHIBIT	$V_{I(I)}$ = 5 V		Full range		0.8	1.5		0.8	1.5	mA
Low-level input current, INHIBIT	$V_{I(I)}$ = 0 V		Full range		5	10		5	20	µA
Comparator reference voltage	V_I = 4.5 V to 6 V		Full range	1.08	1.2	1.32	1.14	1.2	1.26	V
Comparator input bias current	V_I = 6 V		Full range		40	100		40	100	µA
Switch on-state voltage	V_I = 4.5 V	I_O = 100 mA	25°C		0.13	0.2		0.13	0.2	V
		I_O = 500 mA	Full range			0.85			1	
Switch off-state current	V_I = 4.5 V, V_O = 30 V		25°C		10	50		10	50	µA
			Full range			200			500	
Sense voltage, CUR LIM SENS	V_I = 6 V		25°C	0.45		1	0.45		1	V
Diode forward voltage	I_O = 10 mA		Full range		0.75	0.85		0.75	0.95	V
	I_O = 100 mA		Full range		0.9	1		0.9	1.1	
	I_O = 500 mA		Full range		1.33	1.55		1.33	1.75	
Diode reverse voltage	I_O = 500 µA		Full range				30			V
	I_O = 200 µA		Full range	30						
On-state supply current			25°C		11	14		11	14	mA
			Full range			15			16	
Off-state supply current			25°C		6	9		6	9	mA
			Full range			10			11	

† Full range is 0°C to 70°C for the TL497AC and –40°C to 85°C for the TL497AI.
‡ All typical values are at T_A = 25°C.

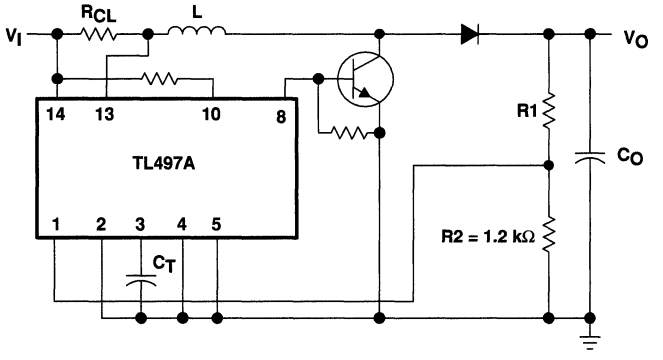
electrical characteristics over recommended operating conditions, V_{CC} = 6 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL497AY			UNIT
		MIN	TYP	MAX	
High-level input current, INHIBIT	$V_{I(I)}$ = 5 V		0.8		mA
Low-level input current, INHIBIT	$V_{I(I)}$ = 0 V		5		µA
Comparator reference voltage	V_I = 4.5 V to 6 V		1.2		V
Comparator input bias current	V_I = 6 V		40		µA
Switch on-state voltage	V_I = 4.5 V, I_O = 100 mA		0.13		V
Switch off-state current	V_I = 4.5 V, V_O = 30 V		10		µA
Diode forward voltage	I_O = 10 mA		0.75		V
	I_O = 100 mA		0.9		
	I_O = 500 mA		1.33		
On-state supply current			11		mA
Off-state supply current			6		mA

APPLICATION INFORMATION



BASIC CONFIGURATION
(Peak Switching Current = $I_{(PK)}$ < 500 mA)



EXTENDED POWER CONFIGURATION
(using external transistor)

DESIGN EQUATIONS

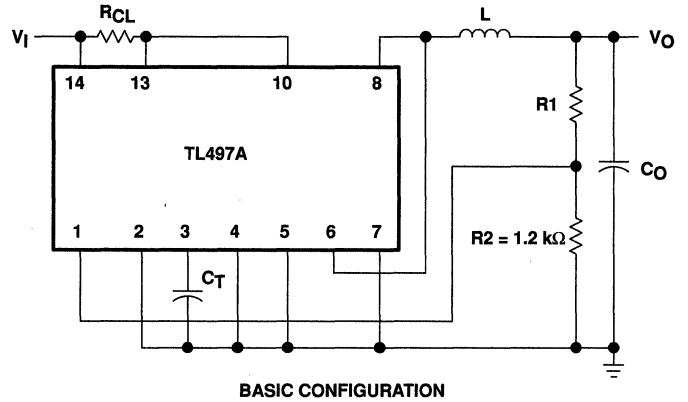
- $I_{(PK)} = 2\ I_O max \left[\frac{V_O}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{(PK)}} t_{on}\ (\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

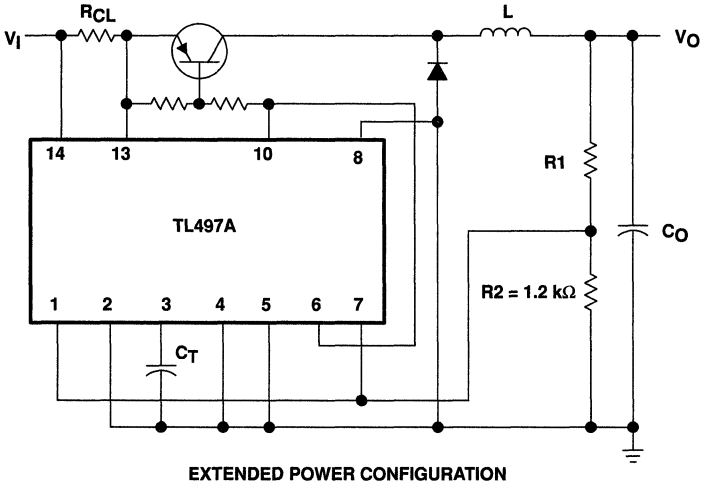
- $C_T (pF) \approx 12\ t_{on}\ (\mu s)$
- $R1 = (V_O - 1.2\ V)\ k\Omega$
- $R_{CL} = \frac{0.5\ V}{I_{(PK)}}$
- $C_O\ (\mu F) \approx t_{on}(\mu s) \frac{\left[\frac{V_I}{V_O} I_{(PK)} + I_O\right]}{V_{ripple\ (PK)}}$

Figure 1. Positive Regulator, Step-Up Configurations

APPLICATION INFORMATION



BASIC CONFIGURATION
(Peak Switching Current = $I_{(PK)}$ < 500 mA)



EXTENDED POWER CONFIGURATION
(using external transistor)

DESIGN EQUATIONS

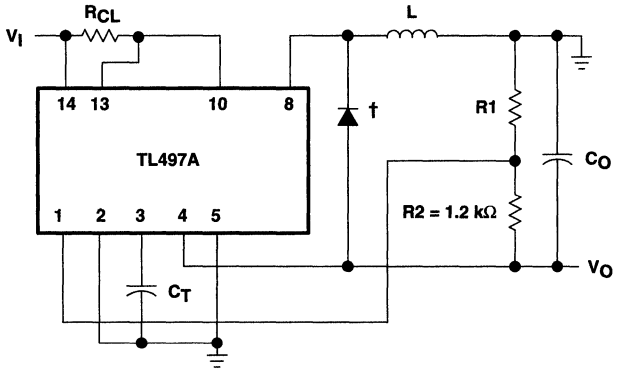
- $I_{(PK)} = 2\ I_O\ max$
- $L\ (\mu H) = \dfrac{V_I - V_O}{I_{(PK)}} t_{on}(\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (10 to 150 μs)

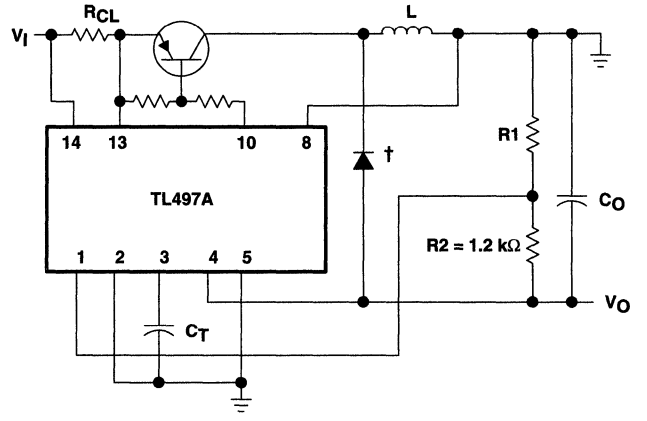
- $C_T(pF) \approx 12\ t_{on}(\mu s)$
- $R1 = (V_O - 1.2\ V)\ k\Omega$
- $R_{CL} = \dfrac{0.5\ V}{I_{(PK)}}$
- $C_O\ (\mu F) \approx t_{on}(\mu s) \dfrac{\left[\dfrac{V_I - V_O}{V_O} I_{(PK)} + I_O\right]}{V_{ripple\ (PK)}}$

Figure 2. Positive Regulator, Step-Down Configurations

APPLICATION INFORMATION



BASIC CONFIGURATION
(Peak Switching Current = $I_{(PK)}$ < 500 mA)



EXTENDED POWER CONFIGURATION
(using external transistor)

DESIGN EQUATIONS

- $I_{(PK)} = 2\, I_O \max\left[1 + \frac{|V_O|}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{(PK)}} t_{on}(\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (10 to 150 μs)

- $C_T(pF) \approx 12\ t_{on}(\mu s)$
- $R1 = \left(|V_O| - 1.2\ V\right)\ k\Omega$

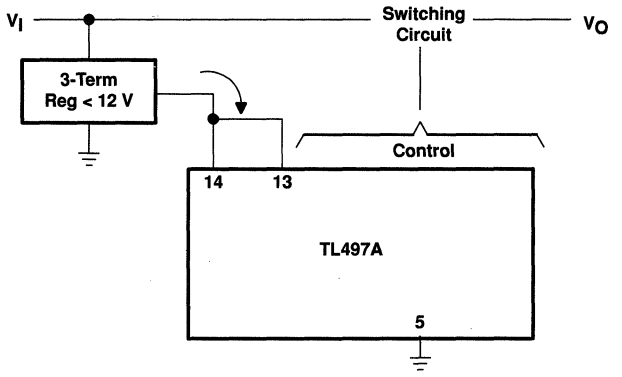
$$R_{CL} = \frac{0.5\ V}{I_{(PK)}}$$

- $C_O\ (\mu F) \approx t_{on}(\mu s) \frac{\left[\frac{V_I}{|V_O|} I_{(PK)} + I_O\right]}{V_{ripple\ (PK)}}$

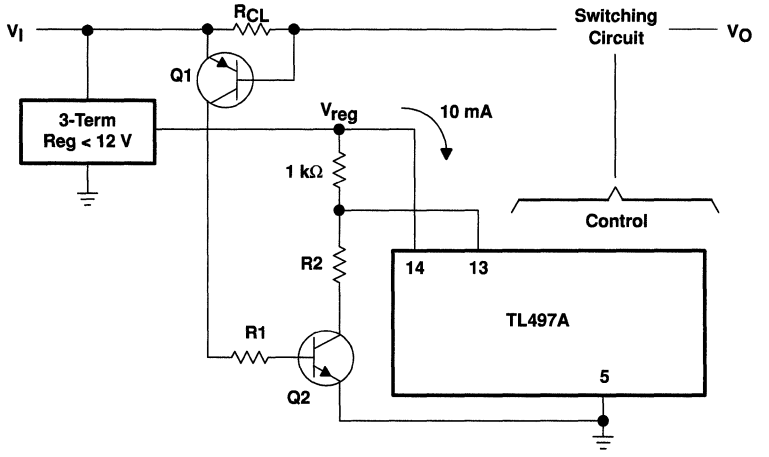
† Use external catch diode, e.g., 1N4001, when building an inverting supply with the TL497A.

Figure 3. Inverting Applications

APPLICATION INFORMATION



EXTENDED INPUT CONFIGURATION WITHOUT CURRENT LIMIT



CURRENT LIMIT FOR EXTENDED INPUT CONFIGURATION

DESIGN EQUATIONS

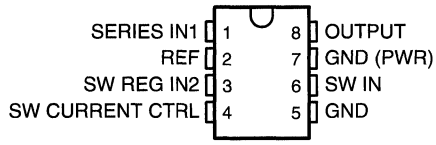
- $R_{CL} = \frac{V_{BE(Q1)}}{I_{limit\ (PK)}}$
- $R1 + \frac{V_I}{I_{B(Q2)}}$
- $R2 = \left(V_{reg} - 1\right) 10\ k\Omega$

Figure 4. Extended Input Voltage Range (V_I > 12 V)

SLVS029D – JANUARY 1984 – REVISED JULY 1999

- **Internal Series-Pass and Step-Up Switching Regulator**
- **Output Adjustable From 2.9 V to 30 V**
- **1-V to 10-V Input for Switching Regulator**
- **4.5-V to 32-V Input for Series Regulator**
- **Externally Controlled Switching Current**
- **No External Rectifier Required**

P PACKAGE
(TOP VIEW)



description

The TL499A is an integrated circuit designed to provide a wide range of adjustable regulated supply voltages. The regulated output voltage can be varied from 2.9 V to 30 V by adjusting two external resistors. When the TL499A is ac-coupled to line power through a step-down transformer, it operates as a series dc voltage regulator to maintain the regulated output voltage. With the addition of a battery from 1.1 V to 10 V, an inductor, a filter capacitor, and two resistors, the TL499A operates as a step-up switching regulator during an ac-line failure.

The adjustable regulated output voltage makes the TL499A useful for a wide range of applications. Providing backup power during an ac-line failure makes the TL499A extremely useful in microprocessor memory applications.

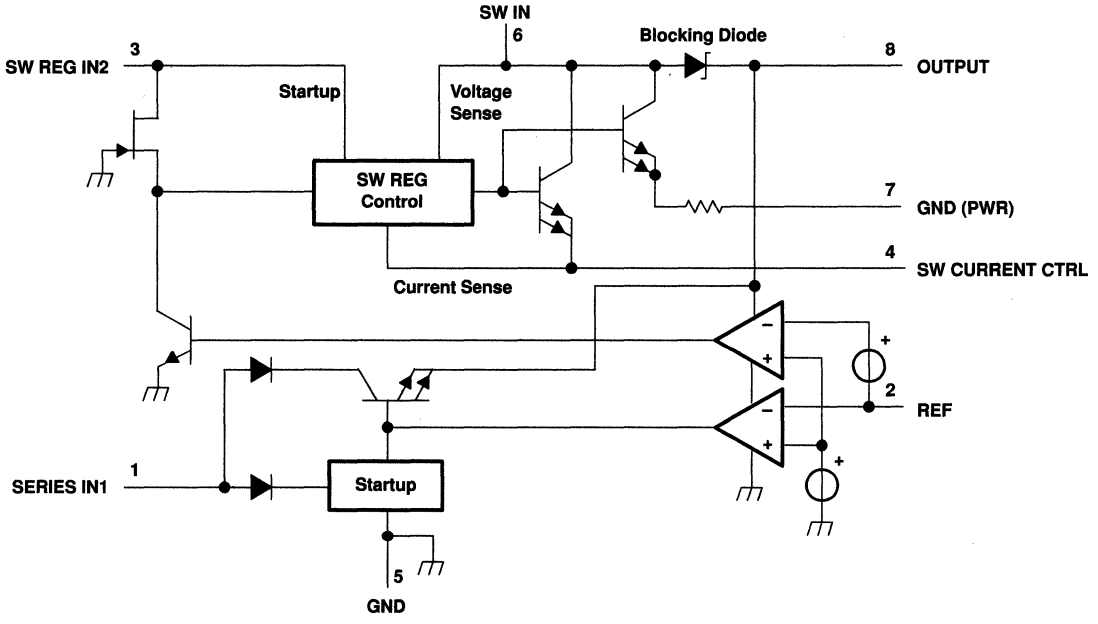
The TL499AC is designed for operation from –20°C to 85°C.

AVAILABLE OPTIONS

T_A	PLASTIC DIP (P)	CHIP FORM (Y)
–20°C to 85°C	TL499ACP	TL499AY

Chip forms are tested at 25°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Output voltage, V_O (see Note 1) ..... 35 V
Input voltage, series regulator, V_I1 ..... 35 V
Input voltage, switching regulator, V_I2 ..... 10 V
Blocking-diode reverse voltage ..... 35 V
Blocking-diode forward current ..... 1 A
Power switch current (SW IN) ..... 1 A
Package thermal impedance, θ_{JA} (see Notes 2 and 3): ..... 127°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Output voltage, V_O	2.9		30	V
Input voltage, V_I1 (SERIES IN1)	4.5		32	V
Input voltage, V_I2 (SW REG IN2)	1.1		10	V
Output-to-input differential voltage, switching regulator, $V_O - V_I2$ (see Note 4)	1.2		28.9	V
Continuous output current, I_O			100	mA
Power switch current (at SW IN)			500	mA
Current-limiting resistor, R_{CL}	150		1000	Ω
Filter capacitor	100		470	µF
Pass capacitor		0.1		µF
Inductor, L (dcr ≤ 0.1 Ω)	50		150	µH
Operating free-air temperature, T_A	–20		85	°C

NOTE 4: When operating temperature range is $T_A \leq 70°C$, minimum $V_O - V_I2$ is ≥ 1.2 V. When operating temperature range is $T_A \leq 85°C$, minimum $V_O - V_I2$ is ≥ 1.9 V.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TL499AC			UNIT
			MIN	TYP	MAX	
Voltage deviation (see Note 5)				20	30	mV/V
Dropout voltage	Switching regulator	T_A = –20°C to 70°C			1.2	V
					1.9	
	Series regulator	V_I1 = 15 V, I_O = 50 mA			1.8	
Reference voltage (internal)		V_I2 = 5 V, V_O = 3 V, I_O = 1 mA	1.2	1.26	1.32	V
Reference voltage change with temperature				5	10	mV/°C
Output regulation (of reference voltage)		I_O = 1 mA to 50 mA		10	30	mV
Output current (see Figure 1)	Switching regulator	V_I2 = 1.1 V, V_O = 12 V, R_{CL} = 150 Ω, T_A = 25°C	10			mA
		V_I2 = 1.5 V, V_O = 15 V, R_{CL} = 150 Ω, T_A = 25°C	15			
		V_I2 = 6 V, V_O = 30 V, R_{CL} = 150 Ω, T_A = 25°C	65			
	Series regulator				100	
Standby current	Switching regulator	V_I2 = 3 V, V_O = 9 V, T_A = 25°C		15	80	µA
	Series regulator	V_I1 = 15 V, V_O = 9 V, R_E2 = 4.7 kΩ		0.8	1.2	mA

NOTE 5: Voltage deviation is the output voltage differences that occurs in a change from series regulation to switching regulation:
Voltage deviation = V_O(series regulation) – V_O(switching regulation)

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TL499AY			UNIT
			MIN	TYP	MAX	
Voltage deviation (see Note 5)				20	30	mV/V
Dropout voltage	Switching regulator	T_A = –20°C to 70°C			1.2	V
		T_A = –20°C to 85°C			1.9	
	Series regulator	V_I1 = 15 V, I_O = 50 mA			1.8	
Reference voltage (internal)		V_I2 = 5 V, V_O = 3 V, I_O = 1 mA	1.2	1.26	1.32	V
Reference voltage change with temperature				5	10	mV/V
Output regulation (of reference voltage)		I_O = 1 mA to 50 mA		10	30	mV/V
Output current (see Figure 1)	Switching regulator	V_I2 = 1.1 V, V_O = 12 V, R_{CL} = 150 Ω	10			mA
		V_I2 = 1.5 V, V_O = 15 V, R_{CL} = 150 Ω	15			
		V_I2 = 6 V, V_O = 30 V, R_{CL} = 150 Ω	65			
	Series regulator				100	
Standby current	Switching regulator	V_I2 = 3 V, V_O = 9 V		15	80	µA
	Series regulator	V_I1 = 15 V, V_O = 9 V, R_E2 = 4.7 kΩ		0.8	1.2	mA

NOTE 5: Voltage deviation is the output voltage differences that occurs in a change from series regulation to switching regulation:
Voltage deviation = V_O(series regulation) – V_O(switching regulation)

APPLICATION INFORMATION

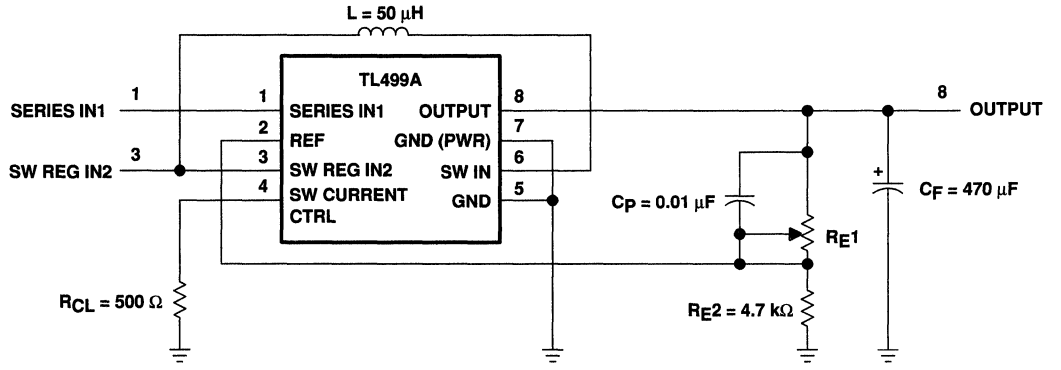


Figure 1. TL499A Basic Configuration

Table 1. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 150 Ω

OUTPUT VOLTAGE (V)	SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30										65	90
25									50	80	100
20						20	25	30	80	100	100
15				15	20	30	45	55	100	100	100
12	10	15	20	25	30	40	55	70	100	100	100
10	15	20	25	30	35	45	65	80	100	100	
9	20	25	25	35	40	50	70	90	100	100	
6	30	35	40	45	55	75	95	100			
5	35	40	45	55	70	85	100	100	Circuit of Figure 1 except:		
4.5	35	45	50	60	75	95	100	100†	R_{CL} = 150 Ω		
3	55	65†	75†	95†	100†				C_F = 330 µF		
2.9	60†	70†	75†	100†	100†				C_P = 0.1 µF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

APPLICATION INFORMATION

Table 2. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 200 Ω

OUTPUT VOLTAGE (V)	SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30										50	100
25									50	70	100
20						15	25	30	70	90	100
15				10	15	25	35	45	90	100	100
12	10	10	15	20	25	35	45	60	100	100	100
10	15	20	20	25	30	40	55	70	100	100	
9	20	20	25	30	35	45	60	80	100		
6	25	30	35	45	50	65	90	100			
5	30	35	40	55	60	75	100	100	Circuit of Figure 1 except:		
4.5	35	40	45	55	65	85	100	100†	R_{CL} = 200 Ω		
3	50	55†	65†	80†	90†				C_F = 330 µF		
2.9	50†	60†	65†	85†	100†				C_P = 0.1 µF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

Table 3. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 300 Ω

OUTPUT VOLTAGE (V)	SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30										40	70
25									40	55	100
20						10	15	20	55	70	100
15				10	10	20	30	35	75	95	100
12	10	10	10	15	20	25	35	45	95	100	100
10	15	15	15	20	25	30	45	55	100	100	
9	15	15	20	25	30	35	50	60	100	100	
6	25	25	30	35	45	55	70	90			
5	30	30	35	45	50	65	85	100	Circuit of Figure 1 except:		
4.5	30	35	40	45	55	70	95	100†	R_{CL} = 300 Ω		
3	45	50†	55†	70†	90†				C_F = 330 µF		
2.9	45†	50†	60†	75†	95†				C_P = 0.1 µF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

APPLICATION INFORMATION

Table 4. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 510 Ω

OUTPUT VOLTAGE (V)	SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30										30	50
25									25	40	75
20									40	55	90
15							15	20	55	70	100
12					10	15	25	35	65	80	100
10				10	20	25	30	40	70	85	
9	10	10	10	15	20	25	35	45	75	100	
6	15	20	20	25	30	35	50	60			
5	20	20	25	30	35	45	55	70	Circuit of Figure 1 except:		
4.5	20	25	30	35	40	50	65	90†	R_{CL} = 510 Ω		
3	35	35†	40†	50†	75†				C_F = 330 µF		
2.9	35†	35†	40†	55†	80†				C_P = 0.1 µF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

Table 5. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 1 kΩ

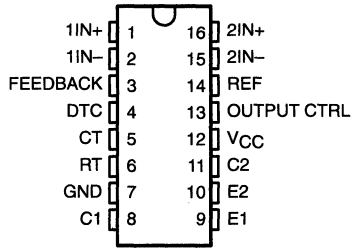
OUTPUT VOLTAGE (V)	SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30											35
25										35	50
20										35	60
15								10	30	45	65
12								20	40	45	85
10							15	25	40	55	
9				10	10	15	25	30	45	60	
6	10	10	10	15	20	20	30	35			
5	10	10	15	20	20	25	35	40	Circuit of Figure 1 except:		
4.5	15	15	15	20	25	30	40	45†	R_{CL} = 1 kΩ		
3	20	25†	25†	30†	35†				C_F = 330 µF		
2.9	20†	25†	25†	30†	45†				C_P = 0.1 µF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

SLVS052C – APRIL 1988 – REVISED JULY 1999

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply Trimmed to 1%**
- **Circuit Architecture Allows Easy Synchronization**
- **Undervoltage Lockout for Low V_{CC} Conditions**

D OR N PACKAGE
(TOP VIEW)



description

The TL594 incorporates all the functions required in the construction of a pulse-width-modulation control circuit on a single chip. Designed primarily for power-supply control, these devices offer the systems engineer the flexibility to tailor the power-supply control circuitry to a specific application.

The TL594 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V regulator with a precision of 1%, an undervoltage lockout control circuit, and output control circuitry.

The error amplifiers exhibit a common-mode voltage range from –0.3 V to V_{CC} –2 V. The DTC comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can be used to drive the common circuitry in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Each device provides for push-pull or single-ended output operation, with selection by means of the output-control function. The architecture of these devices prohibits the possibility of either output being pulsed twice during push-pull operation. The undervoltage lockout control circuit locks the outputs off until the internal circuitry is operational.

The TL594C is characterized for operation from 0°C to 70°C. The TL594I is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

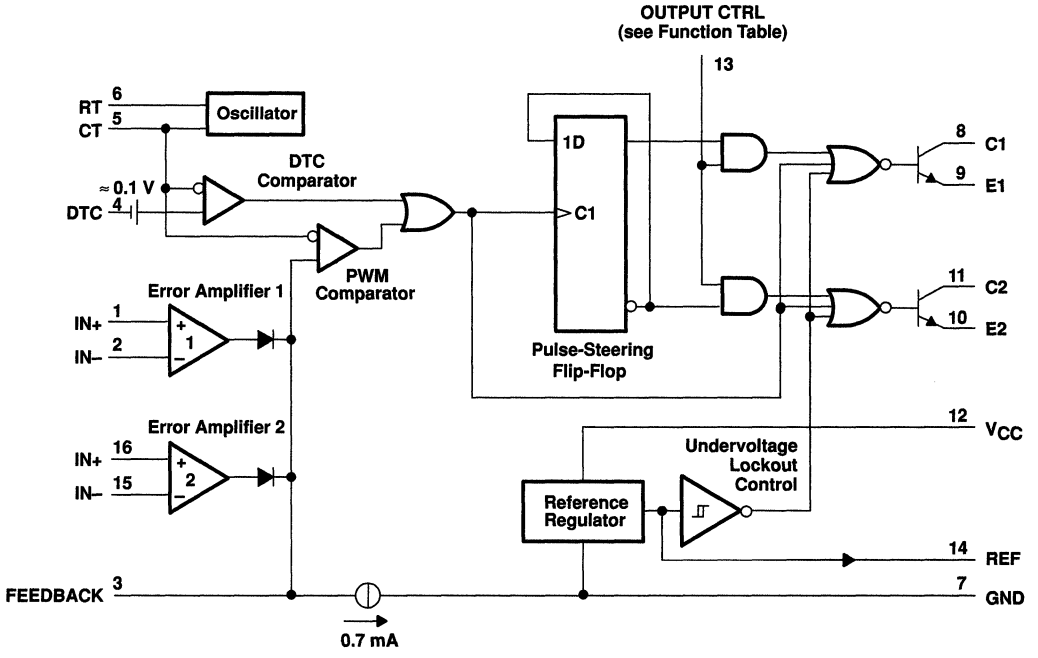
INPUT OUTPUT CTRL	OUTPUT FUNCTION
V_I = –0	Single-ended or parallel output
$V_I = V_{ref}$	Normal push-pull operation

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (N)	
0°C to 70°C	TL594CD	TL594CN	TL594Y
–40°C to 85°C	TL594ID	TL594IN	

The D package is available taped and reeled. Add "R" suffix to device type (e.g., TL594CDR). Chip forms are tested at 25°C.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		TL594X	UNIT
Supply voltage, V_{CC} (see Note 1)		41	V
Amplifier input voltage		V_{CC}+0.3	V
Collector output voltage		41	V
Collector output current		250	mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3)	D package	73	°C
	N package	88	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
Storage temperature range, T_{stg}		–65 to 150	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		7	40	V
Amplifier input voltage, V_I		–0.3	V_{CC}–2	V
Collector output voltage, V_O			40	V
Collector output current (each transistor)			200	mA
Current into feedback terminal			0.3	mA
Timing capacitor, C_T		0.47	10000	nF
Timing resistor, R_T		1.8	500	kΩ
Oscillator frequency, f_{osc}		1	300	kHz
Operating free-air temperature, T_A	TL594C	0	70	°C
	TL594I	–40	85	°C

electrical characteristics over recommended operating conditions, V_{CC} = 15 V, (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†		TL594C, TL594I			UNIT
			MIN	TYP‡	MAX	
Output voltage (REF)	I_O = 1 mA,	T_A = 25°C	4.95	5	5.05	V
Input regulation	V_{CC} = 7 V to 40 V,	T_A = 25°C		2	25	mV
Output regulation	I_O = 1 to 10 mA,	T_A = 25°C		14	35	mV
Output-voltage change with temperature	ΔT_A = MIN to MAX			2	10	mV/V
Short-circuit output current§	V_{ref} = 0		10	35	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.

amplifier section (see Figure 1)

PARAMETER	TEST CONDITIONS			TL594C, TL594I			UNIT
				MIN	TYP‡	MAX	
Input offset voltage, error amplifier	FEEDBACK = 2.5 V				2	10	mV
Input offset current	FEEDBACK = 2.5 V				25	250	nA
Input bias current	FEEDBACK = 2.5 V				0.2	1	μA
Common-mode input voltage range, error amplifier	V_{CC} = 7 V to 40 V			0.3 to V_{CC}–2			V
Open-loop voltage amplification, error amplifier	ΔV_O = 3 V,	R_L = 2 kΩ,	V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V,	R_L = 2 kΩ			800		kHz
Common-mode rejection ratio, error amplifier	V_{CC} = 40 V,	T_A = 25°C		65	80		dB
Output sink current, FEEDBACK	V_{ID} = –15 mV to –5 V,	FEEDBACK = 0.5 V		0.3	0.7		mA
Output source current, FEEDBACK	V_{ID} = 15 mV to 5 V,	FEEDBACK = 3.5 V		–2			mA

‡ All typical values except for parameter changes with temperature are at T_A = 25°C.

oscillator section, C_T = 0.01 μF, R_T = 12 kΩ (see Figure 2)

PARAMETER	TEST CONDITIONS†	TL594C, TL594I			UNIT
		MIN	TYP‡	MAX	
Frequency			10		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1		Hz/kHz
Frequency change with temperature#	ΔT_A = MIN to MAX			50	Hz/kHz

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{X})^2}{N - 1}}$$

Temperature coefficient of timing capacitor and timing resistor not taken into account.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, (unless otherwise noted)

dead-time control section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594C, TL594I			UNIT
		MIN	TYP†	MAX	
Input bias current	V_I = 0 to 5.25 V		–2	–10	μA
Maximum duty cycle, each output	DTC = 0 V	0.45			
Input threshold voltage	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

† All typical values except for parameter changes with temperature are at T_A = 25°C.

output section

PARAMETER		TEST CONDITIONS		TL594C, TL594I			UNIT
				MIN	TYP†	MAX	
Collector off-state current		V_C = 40 V, V_E = 0 V,	V_{CC} = 40 V		2	100	μA
		DTC and OUTPUT CTRL = 0 V, V_C = 15 V, V_E = 0 V,	V_{CC} = 1 to 3 V		4	200	
Emitter off-state current		V_{CC} = V_C = 40 V,	V_E = 0			–100	μA
Collector-emitter saturation voltage	Common emitter	V_E = 0,	I_C = 200 mA		1.1	1.3	V
	Emitter follower	V_C = 15 V,	I_E = –200 mA		1.5	2.5	
Output control input current		V_I = V_{ref}				3.5	mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.

pwm comparator section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594C, TL594I			UNIT
		MIN	TYP†	MAX	
Input threshold voltage, FEEDBACK	Zero duty cycle		4	4.5	V
Input sink current, FEEDBACK	FEEDBACK = 0.5 V	0.3	0.7		mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.

undervoltage lockout section (see Figure 2)

PARAMETER	TEST CONDITIONS‡	TL594C, TL594I		UNIT
		MIN	MAX	
Threshold voltage	T_A = 25°C		6	V
	ΔT_A = MIN to MAX	3.5	6.9	
Hysteresis§		100		mV

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.

PARAMETER	TEST CONDITIONS		TL594C, TL594I			UNIT
			MIN	TYP†	MAX	
Standby supply current	RT at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		9	15	mA
		V_{CC} = 40 V		11	18	
Average supply current	DTC = 2 V,	See Figure 2		12.4		mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, (unless otherwise noted) (continued)

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TL594C, TL594I			UNIT
		MIN	TYP†	MAX	
Output-voltage rise time	Common-emitter configuration (see Figure 3		100	200	ns
Output-voltage fall time			30	100	ns
Output-voltage rise time	Emitter-follower configuration (see Figure 4)		200	400	ns
Output-voltage fall time			45	100	ns

† All typical values except for parameter changes with temperature are at T_A = 25°C.

electrical characteristics over recommended operating conditions, V_{CC} = 15 V, T_A = 25°C (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Output voltage (REF)	I_O = 1 mA		5		V
Input regulation	V_{CC} = 7 V to 40 V		2		mV
Output regulation	I_O = 1 to 10 mA		14		mV
Short-circuit output current‡	V_{ref} = 0		35		mA

‡ Duration of the short circuit should not exceed one second.

oscillator section, C_T = 0.01 µF, R_T = 12 kΩ (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Frequency			10		kHz
Standard deviation of frequency§	All values of V_{CC}, C_T, R_T, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V		1		Hz/kHz

§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

amplifier section (see Figure 1)

PARAMETER	TEST CONDITIONS			TL594Y			UNIT
				MIN	TYP	MAX	
Input offset voltage, error amplifier	FEEDBACK = 2.5 V				2		mV
Input offset current	FEEDBACK = 2.5 V				25		nA
Input bias current	FEEDBACK = 2.5 V				0.2		µA
Open-loop voltage amplification, error amplifier	ΔV_O = 3 V,	R_L = 2 kΩ,	V_O = 0.5 V to 3.5 V		95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V,	R_L = 2 kΩ			800		kHz
Common-mode rejection ratio, error amplifier	V_{CC} = 40 V,	T_A = 25°C			80		dB
Output sink current, FEEDBACK	V_{ID} = –15 mV to –5 V,	FEEDBACK = 0.5 V			0.7		mA

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, T_A = 25°C (unless otherwise noted)

dead-time control section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Input bias current	V_I = 0 to 5.25 V		–2		µA
Input threshold voltage	Zero duty cycle		3		V

output section

PARAMETER		TEST CONDITIONS	TL594Y			UNIT
			MIN	TYP†	MAX	
Collector off-state current		V_C = 40 V, V_E = 0 V, V_{CC} = 40 V		2		µA
		DTC and OUTPUT CTRL = 0 V, V_C = 15 V, V_E = 0 V, V_{CC} = 1 to 3 V		4		
Emitter off-state current		V_{CC} = V_C = 40 V, V_E = 0				µA
Collector-emitter saturation voltage	Common emitter	V_E = 0, I_C = 200 mA		1.1		V
	Emitter follower	V_C = 15 V, I_E = –200 mA		1.5		

pwm comparator section (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Input threshold voltage, FEEDBACK	Zero duty cycle		4		V
Input sink current, FEEDBACK	FEEDBACK = 0.5 V		0.7		mA

total device (see Figure 2)

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Standby supply current	All other inputs and outputs open, R_T at V_{ref}		9		mA
Average supply current	DTC = 2 V, See Figure 2		12.4		mA

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TL594Y			UNIT
		MIN	TYP	MAX	
Output-voltage rise time	Common-emitter configuration (see Figure 3)		100		ns
Output-voltage fall time			30		ns
Output-voltage rise time	Emitter-follower configuration (see Figure 4)		200		ns
Output-voltage fall time			45		ns

PARAMETER MEASUREMENT INFORMATION

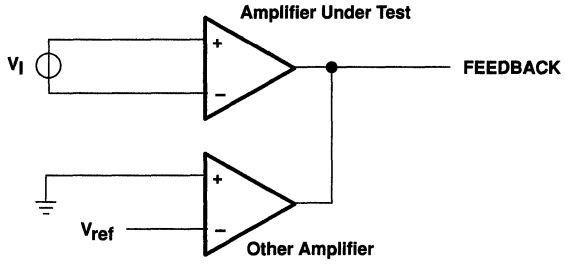
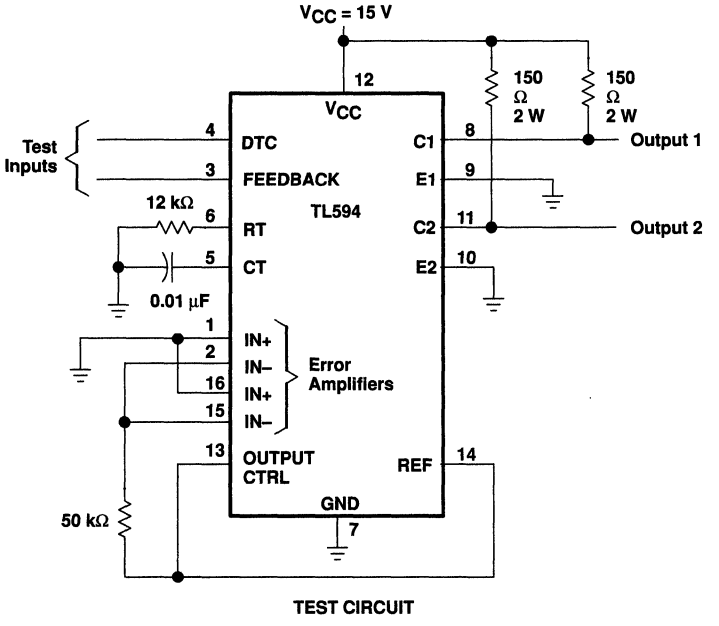
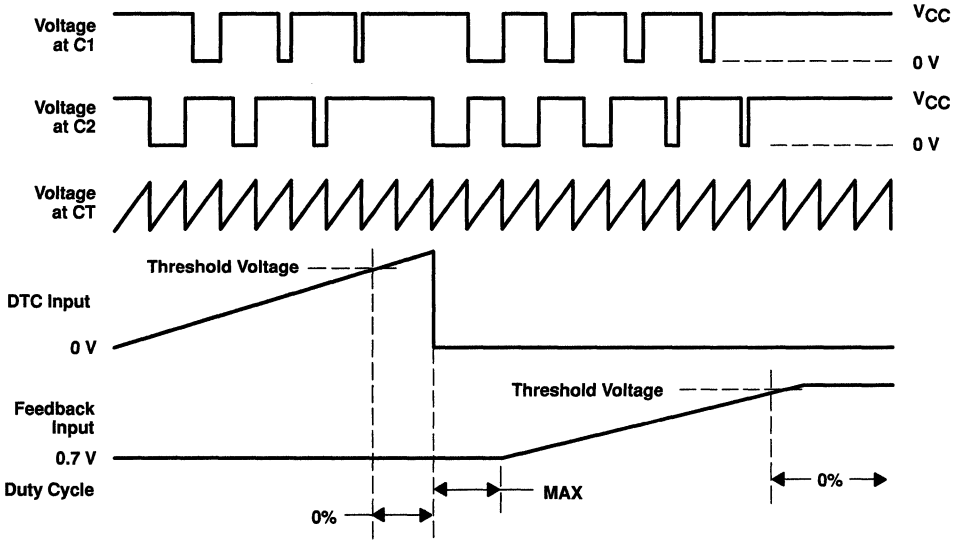


Figure 1. Amplifier-Characteristics Test Circuit

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 2. Operational Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

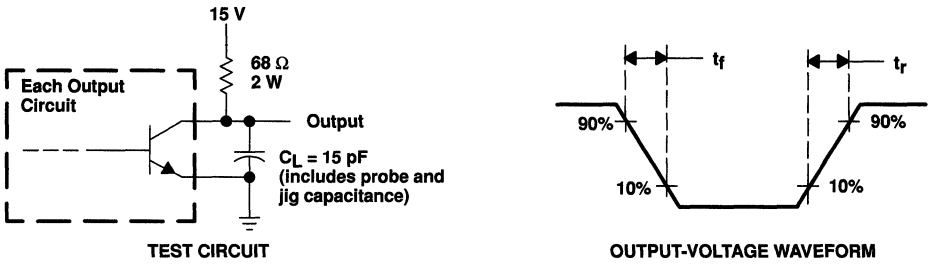


Figure 3. Common-Emitter Configuration

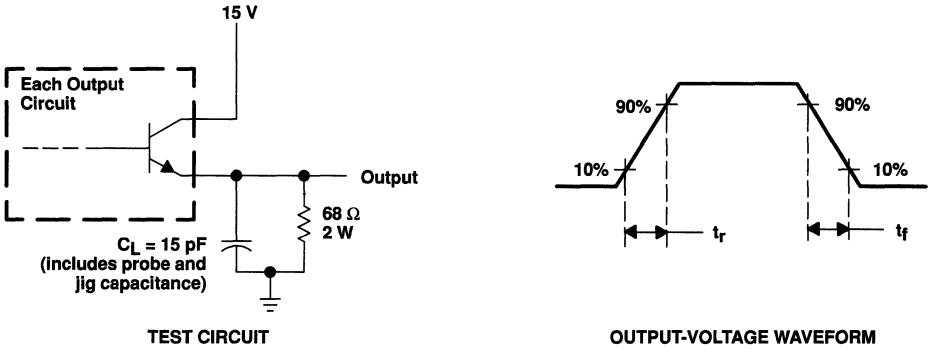
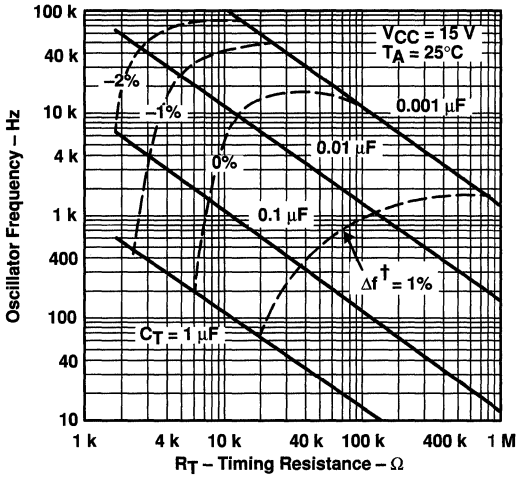


Figure 4. Emitter-Follower Configuration

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION† VS TIMING RESISTANCE



† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

Figure 5

AMPLIFIER VOLTAGE AMPLIFICATION VS FREQUENCY

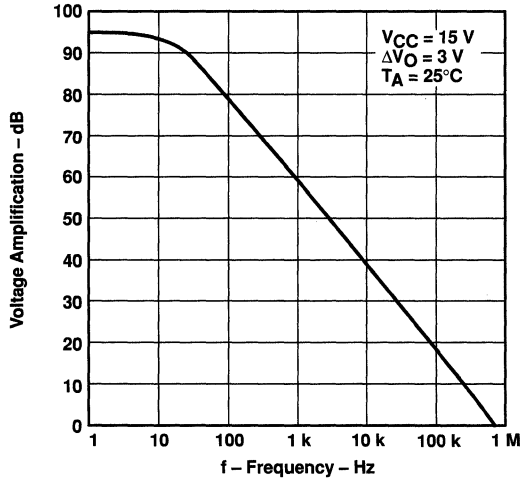
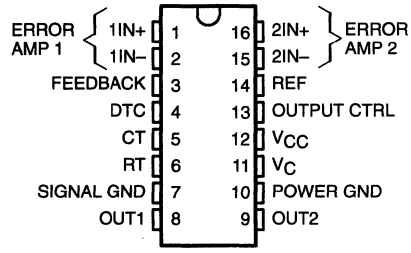


Figure 6

SLVS053C – FEBRUARY 1988 – REVISED JULY 1999

- **Complete PWM Power Control Function**
- **Totem-Pole Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Parallel or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead-Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply, Trimmed to 1% Tolerance**
- **On-Board Output Current-Limiting Protection**
- **Undervoltage Lockout for Low V_{CC} Conditions**
- **Separate Power and Signal Grounds**
- **TL598Q Has Extended Temperature Range . . . –40°C to 125°C**

D OR N PACKAGE
(TOP VIEW)



description

The TL598 incorporates all the functions required in the construction of pulse-width-modulated (PWM) controlled systems on a single chip. Designed primarily for power-supply control, the TL598 provides the systems engineer with the flexibility to tailor the power-supply control circuits to a specific application.

The TL598 contains two error amplifiers, an internal oscillator (externally adjustable), a dead-time control (DTC) comparator, a pulse-steering flip-flop, a 5-V precision reference, undervoltage lockout control, and output control circuits. Two totem-pole outputs provide exceptional rise- and fall-time performance for power FET control. The outputs share a common source supply and common power ground terminals, which allow system designers to eliminate errors caused by high current-induced voltage drops and common-mode noise.

The error amplifier has a common-mode voltage range from 0 V to V_{CC} –2 V. The DTC comparator has a fixed offset that prevents overlap of the outputs during push-pull operation. A synchronous multiple supply operation can be achieved by connecting RT to the reference output and providing a sawtooth input to CT.

The TL598 device provides an output control function to select either push-pull or parallel operation. Circuit architecture prevents either output from being pulsed twice during push-pull operation. The output frequency for push-pull applications is one-half the oscillator frequency $\left(f_o = \frac{1}{2\ RT\ CT}\right)$. For single-ended applications: $f_o = \frac{1}{RT\ CT}$.

The TL598C is characterized for operation from 0°C to 70°C. The TL598Q is characterized for operation from –40°C to 125°C.

FUNCTION TABLE

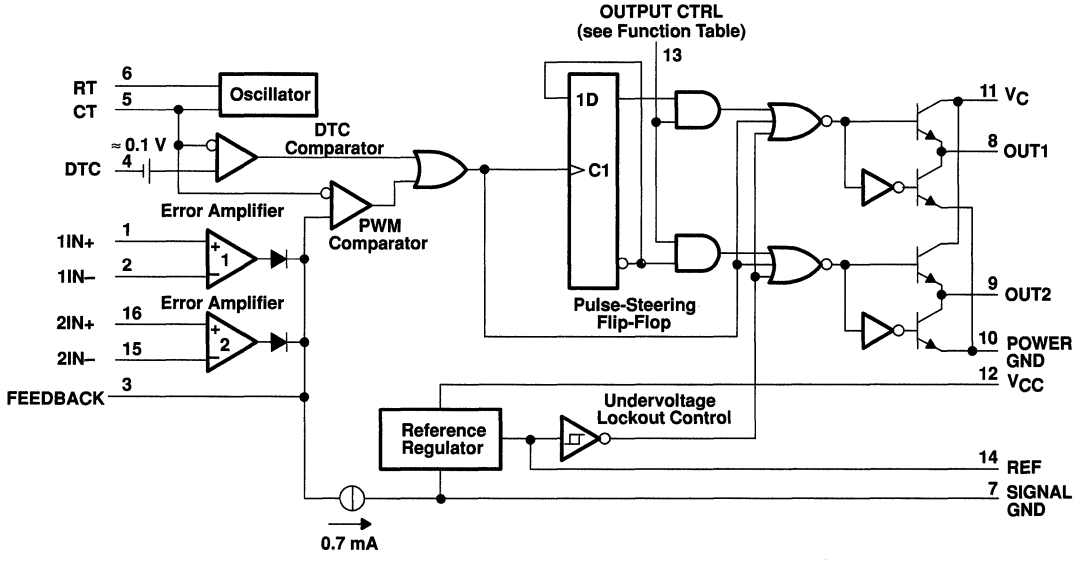
INPUT/OUTPUT CTRL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
V_I = REF	Normal push-pull operation

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (N)	
0°C to 70°C	TL598CD	TL598CN	TL598Y
–40°C to 125°C	TL598QD	–	

Chip forms are tested at 25°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 41 V
Amplifier input voltage, V_I . . . . . V_{CC} + 0.3 V
Collector voltage . . . . . 41 V
Output current (each output), sink or source, I_O . . . . . 250 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . . 73°C/W
N package . . . . . 88°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the signal ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		7	40	V
Amplifier input voltage, V_I		0	V_{CC}–2	V
Collector voltage			40	V
Output current (each output), sink or source, I_O			200	mA
Current into feedback terminal, I_{IL}			0.3	mA
Timing capacitor, C_T		0.00047	10	μF
Timing resistor, R_T		1.8	500	kΩ
Oscillator frequency, f_{osc}		1	300	kHz
Operating free-air temperature, T_A	TL598C	0	70	°C
	TL598Q	–40	125	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

reference section (see Note 4)

PARAMETER	TEST CONDITIONS†		TL598C			TL598Q			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage (REF)	I_O = 1 mA	T_A = 25°C	4.95	5	5.05	4.95	5	5.05	V
		T_A = full range	4.9		5.1	4.9		5.1	
Input regulation	V_{CC} = 7 V to 40 V	T_A = 25°C		2	25		2	22	mV
Output regulation	I_O = 1 mA to 10 mA	T_A = 25°C		1	15		1	15	mV
		T_A = full range			50			80	
Output voltage change with temperature	ΔT_A = MIN to MAX			2	10		2	10	mV/V
Short-circuit output current§	REF = 0 V		–10	–48		–10	–48		mA

† Full range is 0°C to 70°C for the TL598C, and –40°C to 125°C for the TL598Q.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.
NOTE 4: Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

oscillator section, C_T = 0.001 µF, R_T = 12 kΩ (see Figure 1) (see Note 4)

PARAMETER	TEST CONDITIONS†	TL598C, TL598Q			UNIT
		MIN	TYP‡	MAX	
Frequency			100		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1	10	Hz/kHz
Frequency change with temperature#	ΔT_A = full range		70	120	Hz/kHz
	ΔT_A = full range, C_T = 0.01 µF		50	80	

† Full range is 0°C to 70°C for the TL598C, and –40°C to 125°C for the TL598Q.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{X})^2}{N-1}}$$

Effects of temperature on external R_T and C_T are not taken into account.
NOTE 4. Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

error amplifier section (see Note 4)

PARAMETER	TEST CONDITIONS	TL598C, TL598Q			UNIT
		MIN	TYP‡	MAX	
Input offset voltage	FEEDBACK = 2.5 V		2	10	mV
Input offset current	FEEDBACK = 2.5 V		25	250	nA
Input bias current	FEEDBACK = 2.5 V		0.2	1	µA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	0 to V_{CC}–2			V
Open-loop voltage amplification	ΔV_O (FEEDBACK) = 3 V, V_O (FEEDBACK) = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth			800		kHz
Common-mode rejection ratio	V_{CC} = 40 V, ΔV_{IC} = 6.5 V, T_A = 25°C	65	80		dB
Output sink current (FEEDBACK)	FEEDBACK = 0.5 V	0.3	0.7		mA
Output source current (FEEDBACK)	FEEDBACK = 3.5 V	–2			mA
Phase margin at unity gain	FEEDBACK = 0.5 V to 3.5 V, R_L = 2 kΩ		65°		
Supply-voltage rejection ratio	FEEDBACK = 2.5 V, ΔV_{CC} = 33 V, R_L = 2 kΩ		100		dB

‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
NOTE 4. Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

undervoltage lockout section (see Note 4)

PARAMETER	TEST CONDITIONS†	TL598C		TL598Q		UNIT
		MIN	MAX	MIN	MAX	
Threshold voltage	T_A = 25°C	4	6	4	6	V
	ΔT_A = full range	3.5	6.9	3	6.9	
Hysteresis‡	T_A = 25°C	100		100		mV
	T_A = full range	50		30		

† Full range is 0°C to 70°C for the TL598C, and –40°C to 125°C for the TL598Q.
‡ Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.
NOTE 4. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

output section (see Note 4)

PARAMETER	TEST CONDITIONS		TL598C, TL598Q		UNIT
			MIN	MAX	
High-level output voltage	V_{CC} = 15 V, V_C = 15 V	I_O = –200 mA	12		V
		I_O = –20 mA	13		
Low-level output voltage	V_{CC} = 15 V, V_C = 15 V	I_O = 200 mA		2	V
		I_O = 20 mA		0.4	
Output-control input current	V_I = V_{ref}			3.5	mA
	V_I = 0.4 V			100	µA

NOTE 4. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

dead-time control section (see Figure 1) (see Note 4)

PARAMETER	TEST CONDITIONS	TL598C			TL598Q			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
Input bias current (DTC)	V_I = 0 to 5.25 V		–2	–10		–2	–25	µA
Maximum duty cycle, each output	DTC = 0 V	0.45			0.45			
Input threshold voltage (DTC)	Zero duty cycle		3	3.3		3	3.2	V
	Maximum duty cycle	0			0			

§ All typical values except for parameter changes with temperature are at T_A = 25°C.
NOTE 4. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

pwm comparator section (see Note 4)

PARAMETER	TEST CONDITIONS	TL598C, TL598Q			UNIT
		MIN	TYP§	MAX	
Input threshold voltage (FEEDBACK)	DTC = 0 V		3.75	4.5	V
Input sink current (FEEDBACK)	$V_{(FEEDBACK)}$ = 0.5 V	0.3	0.7		mA

§ All typical values except for parameter changes with temperature are at T_A = 25°C.
NOTE Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

total device (see Figure 1) (see Note 4)

PARAMETER	TEST CONDITIONS		TL598C, TL598Q			UNIT
			MIN	TYP§	MAX	
Standby supply current	RT = V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		15	21	mA
		V_{CC} = 40 V		20	26	
Average supply current	DTC = 2 V			15		mA

§ All typical values except for parameter changes with temperature are at T_A = 25°C.
NOTE 4. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

switching characteristics, T_A = 25°C (see Note 4)

PARAMETER	TEST CONDITIONS	TL598C, TL598Q			UNIT
		MIN	TYP	MAX	
Output-voltage rise time	CL = 1500 pF, VC = 15 V, VCC = 15 V, See Figure 2		60	150	ns
Output-voltage fall time			35	75	

NOTE 4. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, V_{CC} = 15 V, T_A = 25°C

reference section (see Note 4)

PARAMETER	TEST CONDITIONS	TL598Y			UNIT
		MIN	TYP†	MAX	
Output voltage (REF)	I_O = 1 mA		5		V
Input regulation	V_{CC} = 7 V to 40 V		2		mV
Output regulation	I_O = 1 mA to 10 mA		1		mV
Output-voltage change with temperature			2		mV/V
Short-circuit output current‡	REF = 0 V		–48		mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.
‡ Duration of the short circuit should not exceed one second.
NOTE 4. Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

oscillator section, C_T = 0.001 µF, R_T = 12 kΩ (see Figure 1) (see Note 4)

PARAMETER	TEST CONDITIONS	TL598Y			UNIT
		MIN	TYP	MAX	
Frequency			100		kHz
Standard deviation of frequency§	All values of V_{CC}, C_T, R_T, T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V,		1		Hz/kHz

§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{X})^2}{N-1}}$$

NOTE 4. Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

error amplifier section (see Note 4)

PARAMETER	TEST CONDITIONS	TL598Y			UNIT
		MIN	TYP	MAX	
Input offset voltage	Feedback = 2.5 V		2		mV
Input offset current	Feedback = 2.5 V		25		nA
Input bias current	Feedback = 2.5 V		0.2		µA
Open-loop voltage amplification	ΔV_O (FEEDBACK) = 3 V, V_O (FEEDBACK) = 0.5 V to 3.5 V		95		dB
Unity-gain bandwidth			800		kHz
Common-mode rejection ratio	V_{CC} = 40 V, ΔV_{IC} = 6.5 V,		80		dB
Output sink current (FEEDBACK)	FEEDBACK = 0.5 V		0.7		mA
Phase margin at unity gain	FEEDBACK = 0.5 V to 3.5 V, R_L = 2 kΩ		65°		
Supply-voltage rejection ratio	FEEDBACK = 2.5 V, ΔV_{CC} = 33 V, R_L = 2 kΩ		100		dB

NOTE 4. Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

electrical characteristics, V_{CC} = 15 V, T_A = 25°C

dead-time control section (see Figure 1) (see Note 4)

PARAMETER	TEST CONDITIONS	TL598Y			UNIT
		MIN	TYP	MAX	
Input bias current (DTC)	V_I = 0 to 5.25 V		–2		µA
Input threshold voltage (DTC)	Zero duty cycle		3		V

NOTE 4. Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

pwm comparator section (see Note 4)

PARAMETER	TEST CONDITIONS	TL598Y			UNIT
		MIN	TYP	MAX	
Input threshold voltage (FEEDBACK)	DTC = 0 V		3.75		V
Input sink current (FEEDBACK)	FEEDBACK = 0.5 V		0.7		mA

NOTE 4. Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

total device (see Figure 1) (see Note 4)

PARAMETER	TEST CONDITIONS		TL598Y			UNIT
			MIN	TYP	MAX	
Standby supply current	RT = V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		15		mA
		V_{CC} = 40 V		20		
Average supply current	DTC = 2 V			15		mA

NOTE 4. Pulse-testing techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

PARAMETER MEASUREMENT INFORMATION

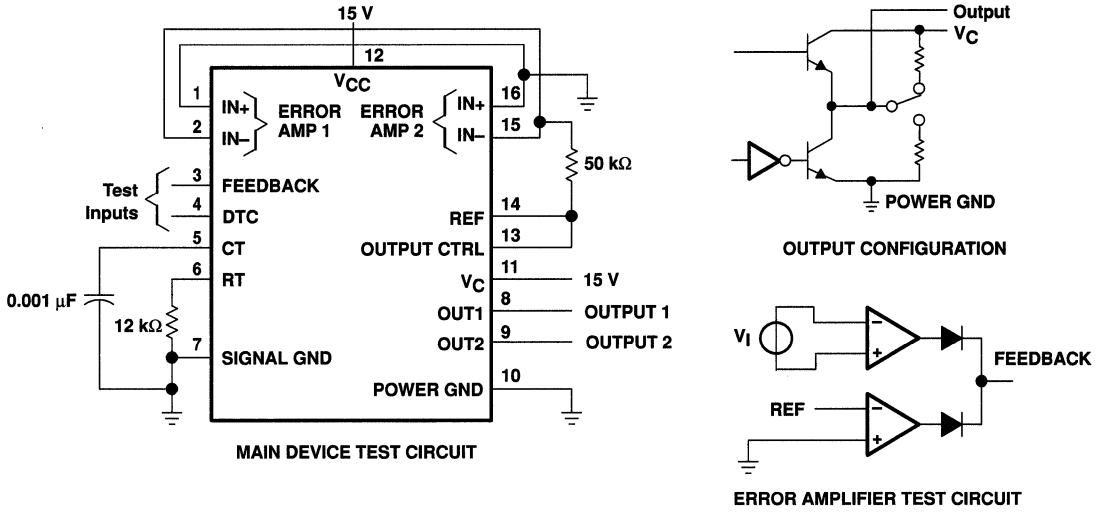


Figure 1. Test Circuits

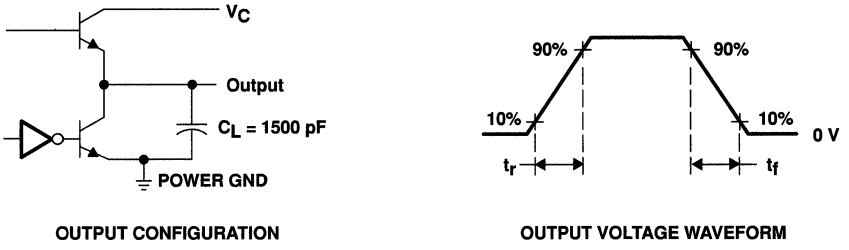
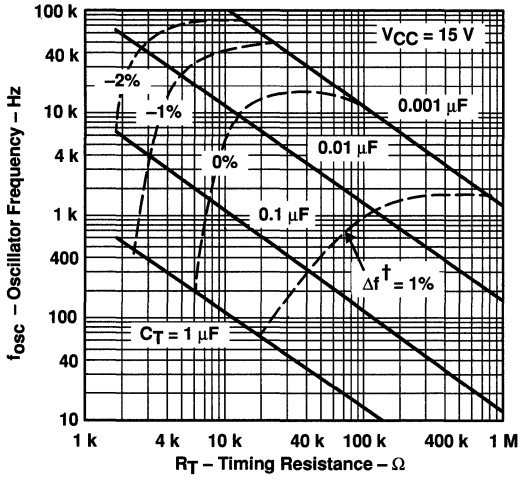


Figure 2. Switching Output Configuration and Voltage Waveform

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION† vs TIMING RESISTANCE



† Frequency variation (Δf) is the change in predicted oscillator frequency that occurs over the full temperature range.

Figure 3

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

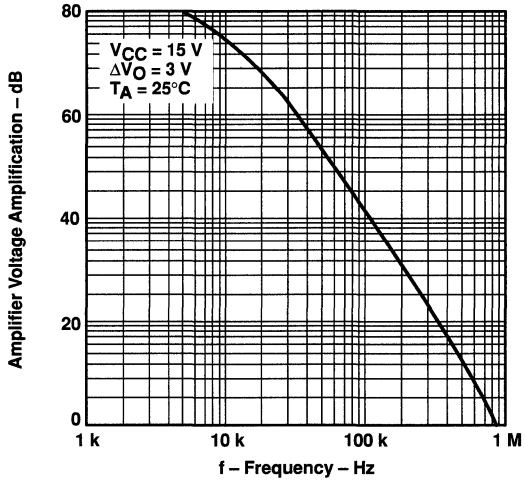
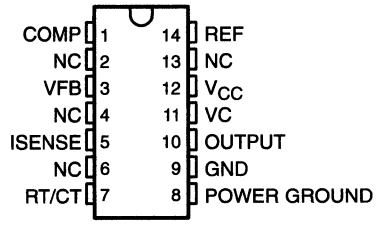


Figure 4

SLVS038D – JANUARY 1989 – REVISED JULY 1999

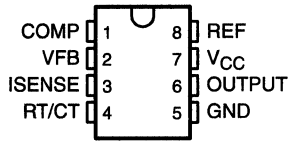
- **Optimized for Off-Line and dc-to-dc Converters**
- **Low Start-Up Current (<1 mA)**
- **Automatic Feed-Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load-Response Characteristics**
- **Undervoltage Lockout With Hysteresis**
- **Double-Pulse Suppression**
- **High-Current Totem-Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500-kHz Operation**
- **Error Amplifier With Low Output Resistance**
- **Designed to Be Interchangeable With Unitrode UC2842 and UC3842 Series**

D PACKAGE
(TOP VIEW)



NC – No internal connection

D-8 OR P PACKAGE
(TOP VIEW)



description

The UC284x and UC384x series of control integrated circuits provide the features that are necessary to implement off-line or dc-to-dc fixed-frequency current-mode control schemes with a minimum number of external components. Some of the internally implemented circuits are an undervoltage lockout (UVLO), featuring a start-up current of less than 1 mA, and a precision reference trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator (which also provides current-limit control), and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

Major differences between members of these series are the UVLO thresholds and maximum duty-cycle ranges. Typical UVLO thresholds of 16 V (on) and 10 V (off) on the UCx842 and UCx844 devices make them ideally suited to off-line applications. The corresponding typical thresholds for the UCx843 and UCx845 devices are 8.4 V (on) and 7.6 V (off). The UCx842 and UCx843 devices can operate to duty cycles approaching 100%. A duty-cycle range of 0 to 50% is obtained by the UCx844 and UCx845 by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle.

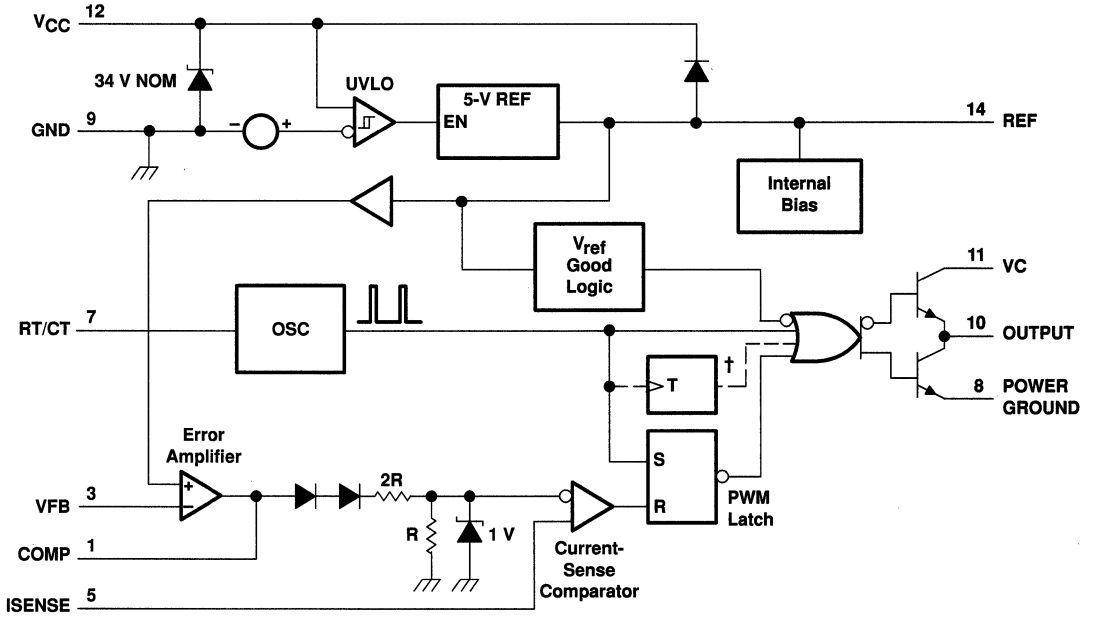
The UC284x-series devices are characterized for operation from –40°C to 85°C. The UC384x-series devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL-OUTLINE (D)	SMALL-OUTLINE (D-8)	PLASTIC DIP (P)	
0°C to 70°C	UC3842D UC3843D UC3844D UC3845D	UC3842D-8 UC3843D-8 UC3844D-8 UC3845D-8	UC3842P UC3843P UC3844P UC3845P	UC3842Y UC3843Y UC3844Y UC3845Y
–40°C to 85°C	UC2842D UC2843D UC2844D UC2845D	UC2842D-8 UC2843D-8 UC2844D-8 UC2845D-8	UC2842P UC2843P UC2844P UC2845P	– – – –

The D and D-8 packages are available taped and reeled. Add the suffix R to the device type (i.e., UC3842DR or UC3842DR-8). Chip forms are tested at 25°C.

functional block diagram



† The toggle flip-flop is present only in UC2844, UC2845, UC3844, and UC3845.
Pin numbers shown are for the D Package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1) (I_{CC} < 30 mA) ..... Self limiting
Analog input voltage range, V_I (VFB and ISENSE) ..... –0.3 V to 6.3 V
Output voltage, V_O (OUTPUT) ..... 35 V
Input voltage, V_I, (VC, D package only) ..... 35 V
Supply current, I_{CC} ..... 30 mA
Output current, I_O ..... ±1 A
Error amplifier output sink current ..... 10 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package ..... 86°C/W
N package ..... 127°C/W
Output energy (capacitive load) ..... 5 µJ
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the device GND terminal.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} and VC‡				30	V
Input voltage, V_I, RT/CT		0		5.5	V
Input voltage, V_I, VFB and ISENSE		0		5.5	V
Output voltage, V_O, OUTPUT		0		30	V
Output voltage, V_O, POWER GROUND†		–0.1		1	V
Supply current, externally limited, I_{CC}				25	mA
Average output current, I_O				200	mA
Reference output current, $I_{O(ref)}$				–20	mA
Timing capacitance, C_T					nF
Oscillator frequency, f_{osc}			100	500	kHz
Operating free-air temperature, T_A	UC284x	–40		85	°C
	UC384x	0		70	

‡ These recommended voltages for V_C and POWER GROUND apply only to the D package.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (see Note 4), R_T = 10 kΩ, C_T = 3.3 nF (unless otherwise specified)

reference section

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output voltage	I_O = 1 mA, T_J = 25°C	4.95	5	5.05	4.9	5	5.1	V
Line regulation	V_{CC} = 12 V to 25 V		6	20		6	20	mV
Load regulation	I_O = 1 mA to 20 mA		6	25		6	25	mV
Temperature coefficient of output voltage			0.2	0.4		0.2	0.4	mV/°C
Output voltage with worst-case variation	V_{CC} = 12 V to 25 V, I_O = 1 mA to 20 mA	4.9		5.1	4.82		5.18	V
Output noise voltage	f = 10 Hz to 10 kHz, T_J = 25°C		50			50		μV
Output-voltage long-term drift	After 1000 h at T_A = 25°C		5	25		5	25	mV
Short-circuit output current		–30	–100	–180	–30	–100	–180	mA

† All typical values are at T_J = 25°C.
NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

oscillator section

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Oscillator frequency (see Note 5)	T_J = 25°C	47	52	57	47	52	57	kHz
Frequency change with supply voltage	V_{CC} = 12 V to 25 V		2	10		2	10	Hz/kHz
Frequency change with temperature			50			50		Hz/kHz
Peak-to-peak amplitude at RT/CT			1.7			1.7		V

† All typical values are at T_J = 25°C.
NOTES: 4. Adjust V_{CC} above the start threshold before setting it to 15 V.
5. Output frequency equals oscillator frequency for the UCx842 and UCx843. Output frequency is one-half oscillator frequency for the UCx844 and UCx845.

error-amplifier section

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Feedback input voltage	COMP at 2.5 V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input bias current			–0.3	–1		–0.3	–2	μA
Open-loop voltage amplification	V_O = 2 V to 4 V	65	90		65	90		dB
Gain-bandwidth product		0.7	1		0.7	1		MHz
Supply-voltage rejection ratio	V_{CC} = 12 V to 25 V	60	70		60	70		dB
Output sink current	VFB at 2.7 V, COMP at 1.1 V	2	6		2	6		mA
Output source current	VFB at 2.3 V, COMP at 5 V	–0.5	–0.8		–0.5	–0.8		mA
High-level output voltage	VFB at 2.3 V, R_L = 15 kΩ to GND	5	6		5	6		V
Low-level output voltage	VFB at 2.7 V, R_L = 15 kΩ to GND		0.7	1.1		0.7	1.1	V

† All typical values are at T_J = 25°C.
NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (see Note 4), R_T = 10 kΩ, C_T = 3.3 nF (unless otherwise specified) (continued)

current-sense section

PARAMETER	TEST CONDITIONS		UC284x			UC384x			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Voltage amplification	See Notes 6 and 7		2.85	3	3.13	2.85	3	3.15	V/V
Current-sense comparator threshold	COMP at 5 V,	See Note 6	0.9	1	1.1	0.9	1	1.1	V
Supply-voltage rejection ratio	V_{CC} = 12 V to 25 V,	See Note 6		70			70		dB
Input bias current				–2	–10		–2	–10	μA
Delay time to output				150	300		150	300	ns

† All typical values are at T_J = 25°C.

NOTES: 4. Adjust V_{CC} above the start threshold before setting it to 15 V.
6. These parameters are measured at the trip point of the latch, with VFB at 0 V.
7. Voltage amplification is measured between ISENSE and COMP, with the input changing from 0 V to 0.8 V.

output section

PARAMETER	TEST CONDITIONS		UC284x			UC384x			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
High-level output voltage	I_{OH} = –20 mA		13	13.5		13	13.5		V
	I_{OH} = –200 mA		12	13.5		12	13.5		
Low-level output voltage	I_{OL} = 20 mA			0.1	0.4		0.1	0.4	V
	I_{OL} = 200 mA			1.5	2.2		1.5	2.2	
Rise time	C_L = 1 nF,	T_J = 25°C		50	150		50	150	ns
Fall time	C_L = 1 nF,	T_J = 25°C		50	150		50	150	ns

† All typical values are at T_J = 25°C.

NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

undervoltage-lockout section

PARAMETER		UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Start threshold voltage	UCx842, UCx844	15	16	17	14.5	16	17.5	V
	UCx843, UCx845	7.8	8.4	9	7.8	8.4	9	
Minimum operating voltage after startup	UCx842, UCx844	9	10	11	8.5	10	11.5	V
	UCx843, UCx845	7	7.6	8.2	7	7.6	8.2	

† All typical values are at T_J = 25°C.

NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

pulse-width-modulator section

PARAMETER		UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum duty cycle	UCx842, UCx843	95%	97%	100%	95%	97%	100%	
	UCx844, UCx845	46%	48%	50%	46%	48%	50%	
Minimum duty cycle				0			0	

† All typical values are at T_J = 25°C.

NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (see Note 4), R_T = 10 kΩ, C_T = 3.3 nF (unless otherwise specified) (continued)

supply voltage

PARAMETER	TEST CONDITIONS	UC284x			UC384x			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Start-up current			0.5	1		0.5	1	mA
Operating supply current	VFB and ISENSE at 0 V		11	17		11	17	mA
Limiting voltage	I_{CC} = 25 mA		34			34		V

† All typical values are at T_J = 25°C.

NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

electrical characteristics, V_{CC} = 15 V (see Note 4), R_T = 10 kΩ, C_T = 3.3 nF, T_J = 25°C (unless otherwise specified)

reference section

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
Output voltage	I_O = 1 mA		5		V
Line regulation	V_{CC} = 12 V to 25 V		6		mV
Load regulation	I_O = 1 mA to 20 mA		6		mV
Temperature coefficient of output voltage			0.2		mV/°C
Output noise voltage	f = 10 Hz to 10 kHz		50		μV
Output-voltage long-term drift	After 1000 h at T_A = 25°C		5		mV
Short-circuit output current			–100		mA

NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

oscillator section

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
Oscillator frequency (see Note 5)			52		kHz
Frequency change with supply voltage	V_{CC} = 12 V to 25 V		2		Hz/kHz
Frequency change with temperature			5		Hz/kHz
Peak-to-peak amplitude at RT/CT			1.7		V

NOTES: 4. Adjust V_{CC} above the start threshold before setting it to 15 V.

5. Output frequency equals oscillator frequency for the UCx842 and UCx843. Output frequency is one-half oscillator frequency for the UCx844 and UCx845.

electrical characteristics, V_{CC} = 15 V (see Note 4), R_T = 10 kΩ, C_T = 3.3 nF, T_J = 25°C (unless otherwise specified) (continued)

error-amplifier section

PARAMETER	TEST CONDITIONS		UC384xY			UNIT
			MIN	TYP	MAX	
Feedback input voltage	COMP at 2.5 V			2.50		V
Input bias current				–0.3		μA
Open-loop voltage amplification	V_O = 2 V to 4 V			90		dB
Gain-bandwidth product				1		MHz
Supply-voltage rejection ratio	V_{CC} = 12 V to 25 V			70		dB
Output sink current	VFB at 2.7 V,	COMP at 1.1 V		6		mA
Output source current	VFB at 2.3 V,	COMP at 5 V		–0.8		mA
High-level output voltage	VFB at 2.3 V,	R_L = 15 kΩ to GND		6		V
Low-level output voltage	VFB at 2.7 V,	R_L = 15 kΩ to GND		0.7		V

NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

current-sense section

PARAMETER	TEST CONDITIONS		UC384xY			UNIT
			MIN	TYP	MAX	
Voltage amplification	See Notes 6 and 7			3		V/V
Current-sense comparator threshold	COMP at 5 V,	See Note 6		1		V
Supply-voltage rejection ratio	V_{CC} = 12 V to 25 V,	See Note 6		70		dB
Input bias current				–2		μA
Delay time to output				150		ns

NOTES: 4. Adjust V_{CC} above the start threshold before setting it to 15 V.
6. These parameters are measured at the trip point of the latch, with VFB at 0 V.
7. Voltage amplification is measured between ISENSE and COMP, with the input changing from 0 V to 0.8 V.

output section

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
High-level output voltage	I_{OH} = –20 mA		13.5		V
	I_{OH} = –200 mA		13.5		
Low-level output voltage	I_{OL} = 20 mA		0.1		V
	I_{OL} = 200 mA		1.5		
Rise time	C_L = 1 nF		50		ns
Fall time	C_L = 1 nF		50		ns

NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

undervoltage-lockout section

PARAMETER		UC384xY			UNIT
		MIN	TYP	MAX	
Start threshold voltage	UC3842Y, UC3844Y		16		V
	UC3843Y, UC3845Y		8.4		
Minimum operating voltage after startup	UC3842Y, UC3844Y		10		V
	UC3843Y, UC3845Y		7.6		

NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

electrical characteristics, V_{CC} = 15 V (see Note 4), R_T = 10 kΩ, C_T = 3.3 nF, T_J = 25°C (unless otherwise specified) (continued)

pulse-width-modulator section

PARAMETER		UC384xY			UNIT
		MIN	TYP	MAX	
Maximum duty cycle	UC3842Y, UC3843Y		97%		
	UC3844Y, UC3845Y		48%		

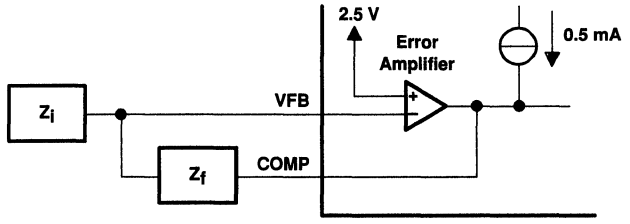
NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

supply voltage

PARAMETER	TEST CONDITIONS	UC384xY			UNIT
		MIN	TYP	MAX	
Start-up current			0.5	1	mA
Operating supply current	VFB and ISENSE at 0 V		11	17	mA
Limiting voltage	I_{CC} = 25 mA		34		V

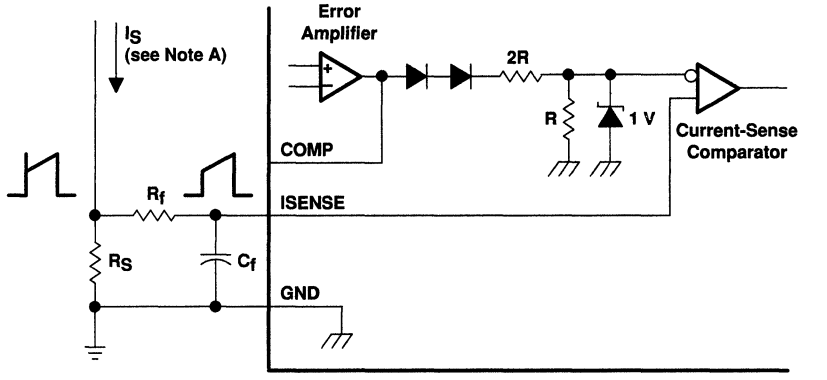
NOTE Adjust V_{CC} above the start threshold before setting it to 15 V.

APPLICATION INFORMATION



NOTE A. Error amplifier can source or sink up to 0.5 mA.

Figure 1. Error-Amplifier Configuration

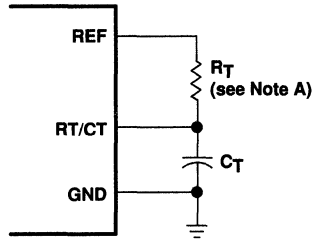


NOTE A. Peak current (I_S) is determined by the formula:

$$I_{S(max)} = \frac{1\ V}{R_S}$$

A small RC filter formed by resistor R_f and capacitor C_f may be required to suppress switch transients.

Figure 2. Current-Sense Circuit



NOTE A. For $R_T > 5\ k\Omega$: $f \approx \frac{1.72}{R_T C_T}$

Figure 3. Oscillator Section

APPLICATION INFORMATION

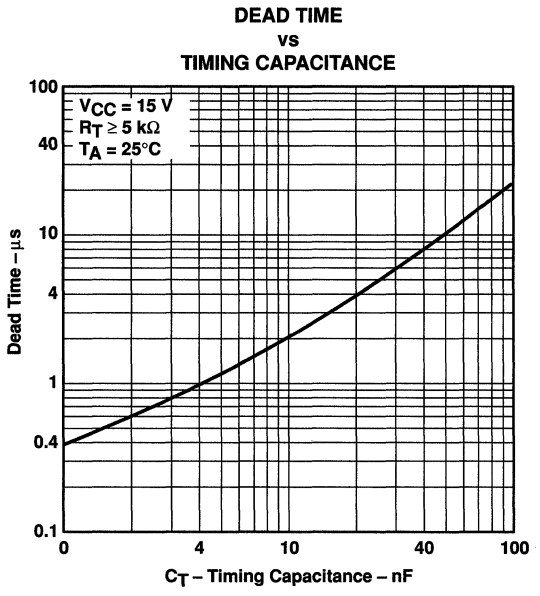


Figure 4

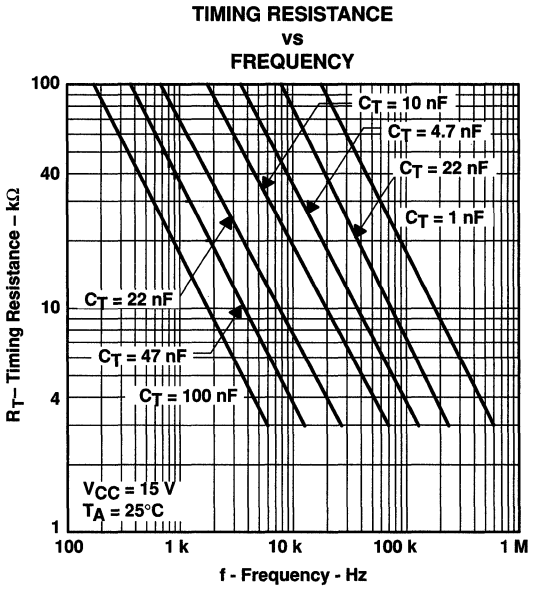


Figure 5

open-loop laboratory test fixture

In the open-loop laboratory test fixture shown in Figure 6, high peak currents associated with loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the GND terminal in a single-point ground. The transistor and 5-kΩ potentiometer sample the oscillator waveform and apply an adjustable ramp to the ISENSE terminal.

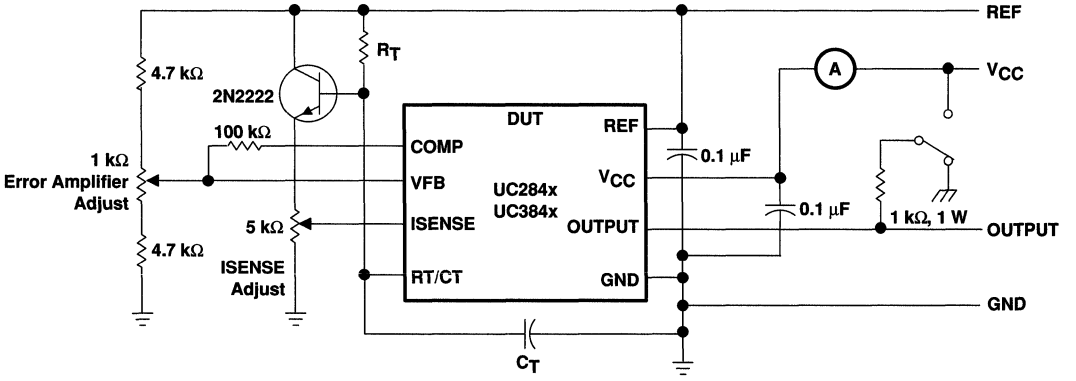


Figure 6. Open-Loop Laboratory Test Fixture

APPLICATION INFORMATION

shutdown technique

The PWM controller (see Figure 7) can be shut down by two methods: either raise the voltage at ISENSE above 1 V or pull the COMP terminal below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or ISENSE terminal is removed. In one example, an externally latched shutdown can be accomplished by adding an SCR that resets by cycling V_{CC} below the lower UVLO threshold. At this point, the reference turns off, allowing the SCR to reset.

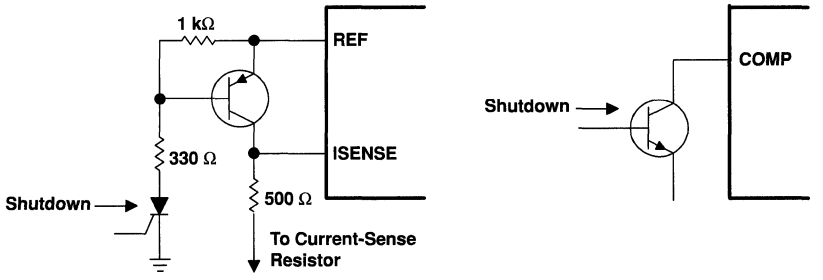


Figure 7. Shutdown Techniques

A fraction of the oscillator ramp can be resistively summed with the current-sense signal to provide slope compensation for converters requiring duty cycles over 50% (see Figure 8). Note that capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

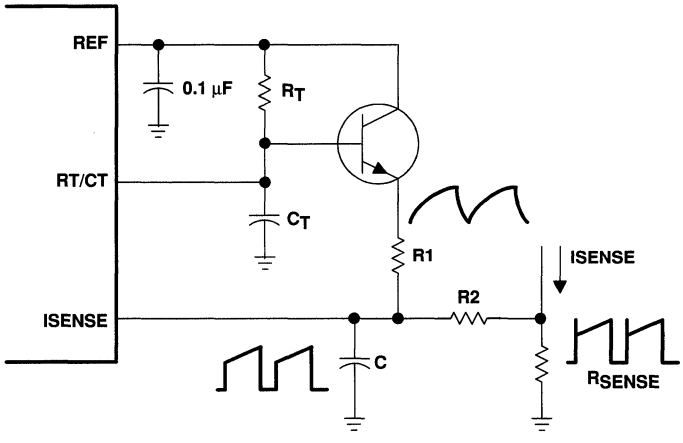
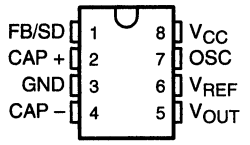


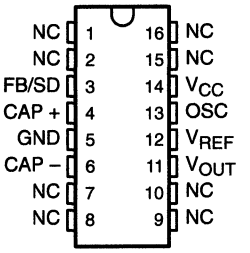
Figure 8. Slope Compensation

- **Output Current . . . 100 mA**
- **Low Loss . . . 1.1 V at 100 mA**
- **Operating Range . . . 3.5 V to 15 V**
- **Reference and Error Amplifier for Regulation**
- **External Shutdown**
- **External Oscillator Synchronization**
- **Devices Can Be Paralleled**
- **Pin-to-Pin Compatible With the LTC1044/7660**

P PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The LT1054 is a bipolar, switched-capacitor voltage converter with regulator. It provides higher output current and significantly lower voltage losses than previously available converters. An adaptive-switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage drop at 100-mA output current is typically 1.1 V. This holds true over the full supply-voltage range of 3.5 V to 15 V. Quiescent current is typically 2.5 mA.

The LT1054 also provides regulation, a feature not previously available in switched-capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output is regulated against changes in both input voltage and output current. The LT1054 also can be shut down by grounding the feedback terminal. Supply current in shutdown is typically 100 μA.

The internal oscillator of the LT1054 runs at a nominal frequency of 25 kHz. The oscillator terminal can be used to adjust the switching frequency or to externally synchronize the LT1054.

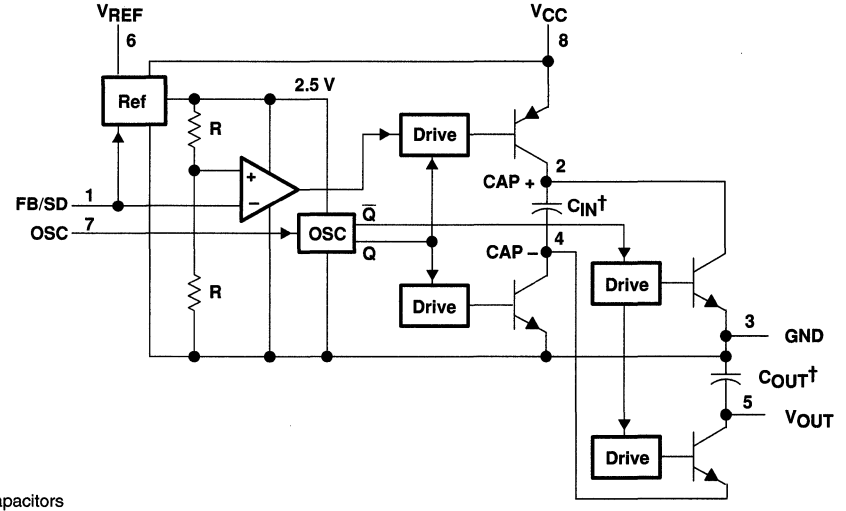
The LT1054C is characterized for operation over a free-air temperature range of 0°C to 70°C. The LT1054I is characterized for operation over a free-air temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (DW)	PLASTIC DIP (P)	
0°C to 70°C	LT1054CDW	LT1054CP	LT1054Y
–40°C to 85°C	LT1054IDW	LT1054IP	—

The DW package is available taped and reeled. Add the suffix R to the device type, (i.e., LT1054CDWR). Chip forms are tested at 25°C.

functional block diagram



† External capacitors
Pin numbers shown are for the P package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted‡

Supply voltage, V_{CC} (see Note 1)	16 V
Input voltage range, V_I (FB/SD terminal)	0 V to V_{CC}
Input voltage range, V_I (OSC terminal)	0 V to V_{ref}
Junction temperature (see Note 2) T_J: LT1054C	125°C
LT1054I	135°C
Package thermal impedance, θ_{JA} (see Notes 3 and 4): DW package	57°C/W
P package	127°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–55°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The absolute maximum supply voltage rating of 16 V is for unregulated circuits. For regulation mode circuits with $V_{OUT} \leq 15$ V, this rating may be increased to 20 V.
2. The devices are functional up to the absolute maximum junction temperature.
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
4. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	15	V
Operating free-air temperature range, T_A	LT1054C	0	70	°C
	LT1054I	–40	85	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	LT1054C LT1054I			UNIT
					MIN	TYP‡	MAX	
V_O	Regulated output voltage	V_{CC} = 7 V, T_J = 25°C, R_L = 500 Ω, See Note 5		25°C	–4.7	–5	–5.2	V
	Input regulation	V_{CC} = 7 V to 12 V, R_L = 500 Ω, See Note 5		Full range		5	25	mV
	Output regulation	V_{CC} = 7 V, See Note 5	R_L = 100 Ω to 500 Ω,	Full range		10	50	mV
	Voltage loss, $V_{CC} - \lvert V_O \rvert$ (see Note 6)	$C_I = C_O$ = 100 µF tantalum	I_O = 10 mA	Full range		0.35	0.55	V
			I_O = 100 mA	Full range		1.1	1.6	
	Output resistance	ΔI_O = 10 mA to 100 mA, See Note 7		Full range		10	15	Ω
	Oscillator frequency	V_{CC} = 3.5 V to 15 V		Full range	15	25	35	kHz
V_{ref}	Reference voltage	$I_{(REF)}$ = 60 µA		25°C	2.35	2.5	2.65	V
				Full range	2.25		2.75	
	Maximum switch current			25°C		300		mA
I_{CC}	Supply current	I_O = 0	V_{CC} = 3.5 V	Full range		2.5	4	mA
			V_{CC} = 15 V	Full range		3	5	
	Supply current in shutdown	$V_{(FB/SD)}$ = 0 V		Full range		100	200	µA

† Full range is 0°C to 70°C for the LT1054C and –40°C to 85°C for the LT1054I.
‡ All typical values are at T_A = 25°C.

NOTES: 5. All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, external capacitor C_{IN} = 10 µF (tantalum), external capacitor C_{OUT} = 100 µF (tantalum) and C1 = 0.002 µF (see Figure 15).

6. For voltage-loss tests, the device is connected as a voltage inverter, with terminals 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations. C_{IN} and C_{OUT} are external capacitors.

7. Output resistance is defined as the slope of the curve (ΔV_O versus ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve is higher at currents less than 10 mA due to the characteristics of the switch transistors.

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			LT1054Y MIN	LT1054Y TYP	LT1054Y MAX	UNIT
V_O	Regulated output voltage	V_{CC} = 7 V T_J = 25°C, R_L = 500 Ω, See Note 5				–5		V
	Input regulation	V_{CC} = 7 V to 12 V, R_L = 500 Ω, See Note 5				5		mV
	Output regulation	V_{CC} = 7 V, R_L = 100 Ω to 500 Ω, See Note 5				10		mV
	Voltage loss, $V_{CC} - \lvert V_O \rvert$ (see Note 6)	$C_I = C_O$ = 100 µF tantalum		I_O = 10 mA		0.35		V
				I_O = 100 mA		1.1		
	Output resistance	ΔI_O = 10 mA to 100 mA, See Note 7				10		Ω
	Oscillator frequency	V_{CC} = 3.5 V to 15 V				25		kHz
V_{ref}	Reference voltage	$I_{(REF)}$ = 60 µA				2.5		V
	Maximum switch current					300		mA
I_{CC}	Supply current	I_O = 0	V_{CC} = 3.5 V			2.5		mA
			V_{CC} = 15 V			3		
	Supply current in shutdown	$V_{(FB/SD)}$ = 0 V				100		µA

NOTES: 5. All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, external capacitor C_{IN} = 10 µF (tantalum), external capacitor C_{OUT} = 100 µF (tantalum) and C1 = 0.002 µF (see Figure 15).

6. For voltage-loss tests, the device is connected as a voltage inverter, with terminals 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations. C_{IN} and C_{OUT} are external capacitors.

7. Output resistance is defined as the slope of the curve (ΔV_O versus ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve is higher at currents less than 10 mA due to the characteristics of the switch transistors.

TYPICAL CHARACTERISTICS

Table of Graphs

Table of Figures

TYPICAL CHARACTERISTICS†

SHUTDOWN THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

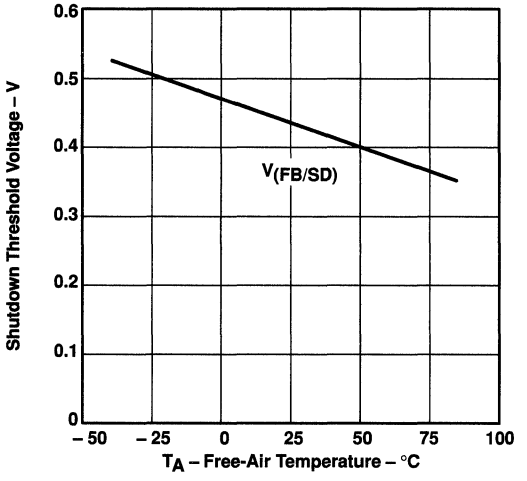


Figure 1

SUPPLY CURRENT
vs
INPUT VOLTAGE

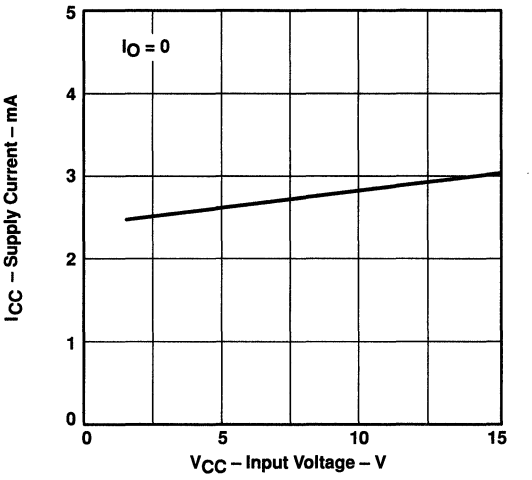


Figure 2

OSCILLATOR FREQUENCY
vs
FREE-AIR TEMPERATURE

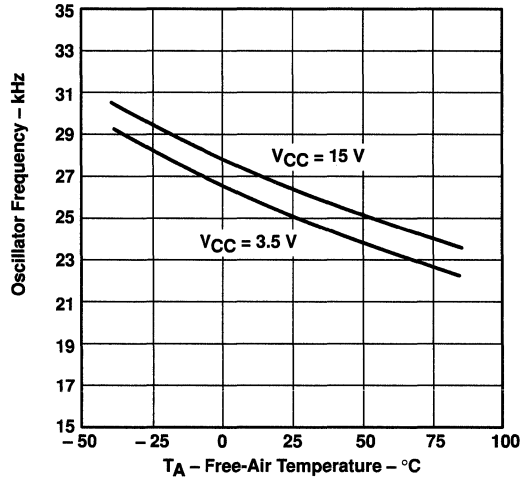


Figure 3

SUPPLY CURRENT IN SHUTDOWN
vs
INPUT VOLTAGE

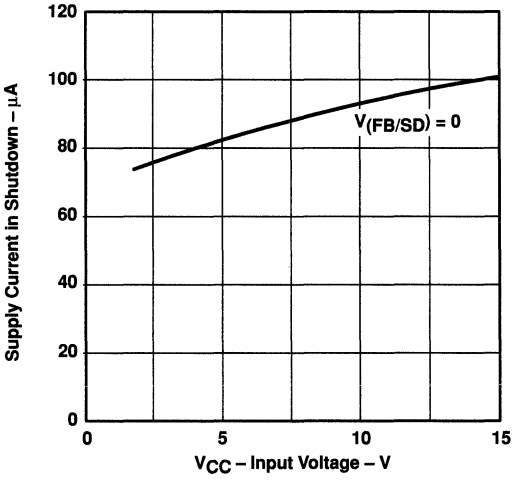


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
OUTPUT CURRENT

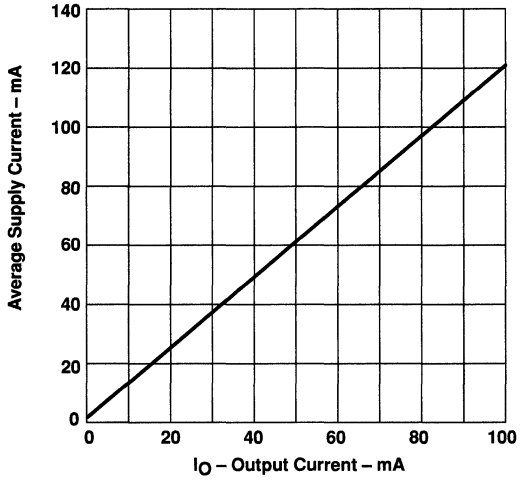


Figure 5

OUTPUT VOLTAGE LOSS
vs
INPUT CAPACITANCE

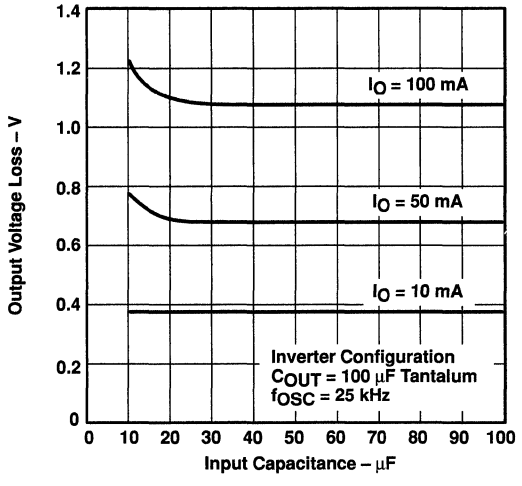


Figure 6

OUTPUT VOLTAGE LOSS
vs
OSCILLATOR FREQUENCY

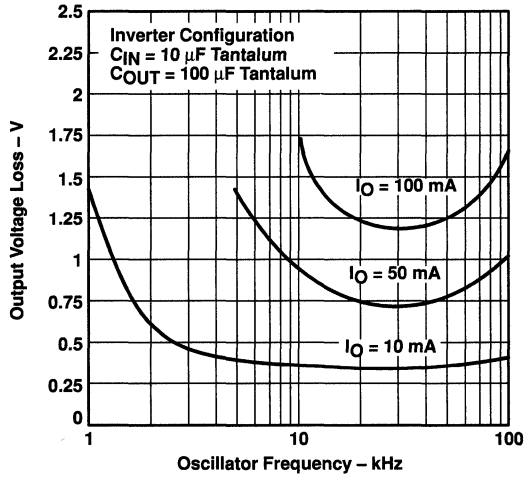


Figure 7

OUTPUT VOLTAGE LOSS
vs
OSCILLATOR FREQUENCY

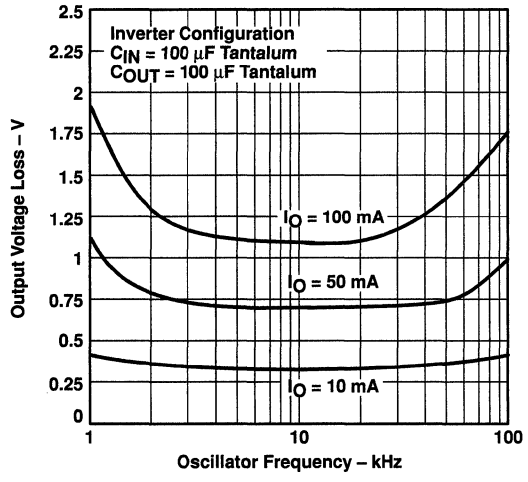


Figure 8

TYPICAL CHARACTERISTICS†

REGULATED OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

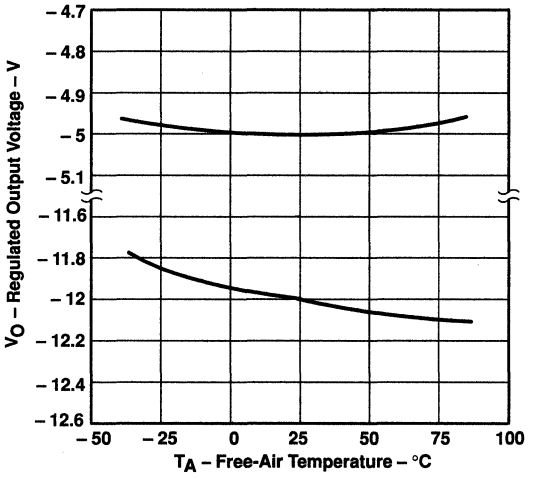


Figure 9

REFERENCE VOLTAGE CHANGE
vs
FREE-AIR TEMPERATURE

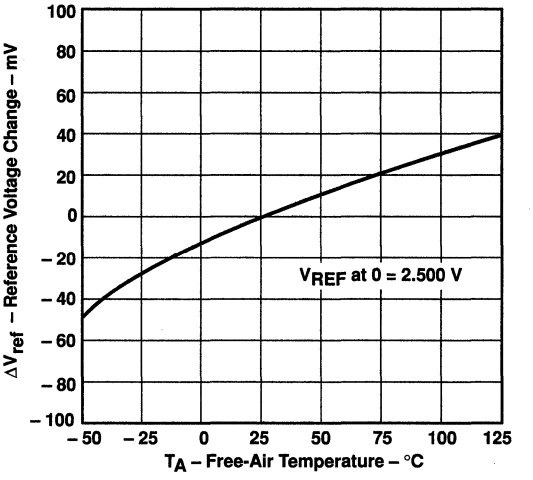


Figure 10

VOLTAGE LOSS
vs
OUTPUT CURRENT

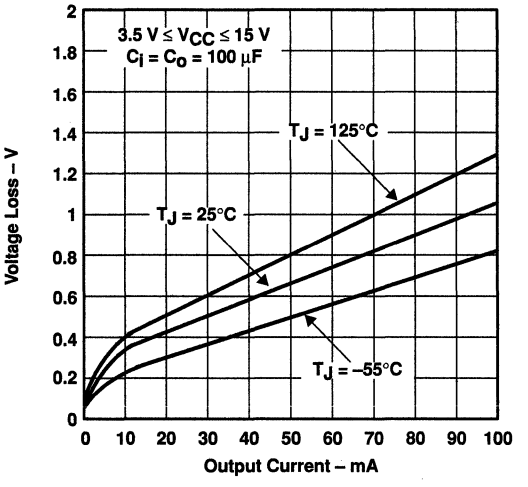


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PRINCIPLES OF OPERATION

A review of a basic switched-capacitor building block is helpful in understanding the operation of the LT1054. When the switch shown in Figure 12 is in the left position, capacitor C1 charges to the voltage at V1. The total charge on C1 is q1 = C1V1. When the switch is moved to the right, C1 is discharged to the voltage at V2. After this discharge time, the charge on C1 is q2 = C1V2. The charge has been transferred from the source V1 to the output V2. The amount of charge transferred is shown in equation 1.

$$\Delta q = q1 - q2 = C1(V1 - V2) \quad (1)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is as shown in equation 2.

$$I = f \times \Delta q = f \times C1(1-V2) \quad (2)$$

To obtain an equivalent resistance for a switched-capacitor network, this equation can be rewritten in terms of voltage and impedance equivalence as shown in equation 3.

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}} \quad (3)$$

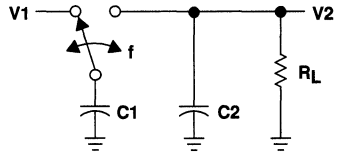


Figure 12. Switched-Capacitor Building Block

PRINCIPLES OF OPERATION

A new variable, R_{EQUIV}, is defined as $R_{EQUIV} = 1 \div fC1$. The equivalent circuit for the switched-capacitor network is shown in Figure 13. The LT1054 has the same switching action as the basic switched-capacitor building block. Even though this simplification does not include finite switch-on resistance and output-voltage ripple, it provides an insight into how the device operates.

These simplified circuits explain voltage loss as a function of oscillator frequency (see Figure 7). As oscillator frequency is decreased, the output impedance is eventually dominated by the 1/fC1 term and voltage losses rise.

Voltage losses also rise as oscillator frequency increases. This is caused by internal switching losses that occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency, this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to run in the frequency band where voltage losses are at a minimum.

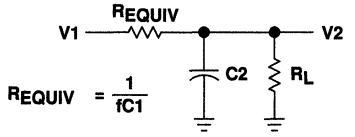


Figure 13. Switched-Capacitor Equivalent Circuit

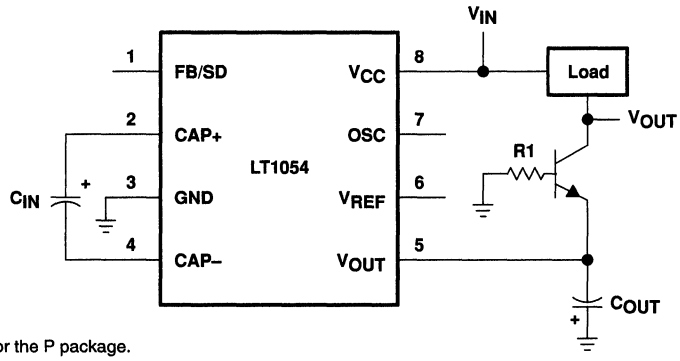
terminal functions (see functional block diagram)

Supply voltage V_{CC} alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current is approximately 2.2 times the output current. During the time that C_{IN} is delivering a charge to C_{OUT}, the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor supplies part of the peak input current drawn by the LT1054, and averages out the current drawn from the supply. A minimum input supply bypass capacitor of 2 µF, preferably tantalum or some other low equivalent-series-resistance (ESR) type, is recommended. A larger capacitor is desirable in some cases. An example of this would be when the actual input supply is connected to the LT1054 through long leads or when the pulse currents drawn by the LT1054 might affect other circuits through supply coupling.

In addition to being the output terminal, V_{OUT} is tied to the substrate of the device. Special care must be taken in LT1054 circuits to avoid making V_{OUT} positive with respect to any of the other terminals. For circuits with the output load connected from V_{CC} to V_{OUT} or from some external positive supply voltage to V_{OUT}, an external transistor must be added (see Figure 14). This transistor prevents V_{OUT} from being pulled above GND during start up. Any small general-purpose transistor such as a 2N2222 or a 2N2219 device can be used. Resistor R1 should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions.

$$R1 \leq \frac{(|V_{OUT}|)\,\beta}{I_{OUT}} \qquad (4)$$

APPLICATION INFORMATION



Pin numbers shown are for the P package.

Figure 14. Circuit With Load Connected from V_{CC} to V_{OUT}

The voltage reference (V_{ref}) output provides a 2.5-V reference point for use in LT1054-based regulator circuits. The temperature coefficient (TC) of the reference voltage has been adjusted so that the TC of the regulated output voltage is near zero. As seen in the typical performance curves, this requires the reference output to have a positive TC. This non-zero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback terminal. The overall result of these drift terms is a regulated output that has a slight positive TC at output voltages below 5 V and a slight negative TC at output voltages above 5 V. For regulator feedback networks, reference output current should be limited to approximately 60 μA. V_{ref} draws approximately 100 μA when shorted to ground and does not affect the internal reference/regulator. This terminal also can be used as a pullup for LT1054 circuits that require synchronization.

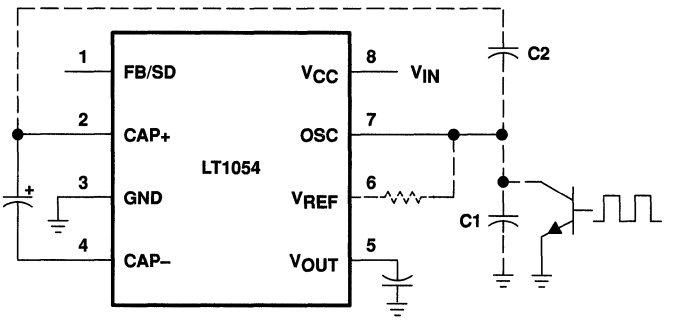
CAP+ is the positive side of input capacitor C_{IN} and is alternately driven between V_{CC} and ground. When driven to V_{CC}, CAP+ sources current from V_{CC}. When driven to ground, CAP+ sinks current to ground. CAP– is the negative side of the input capacitor and is driven alternately between ground and V_{OUT}. When driven to ground, CAP– sinks current to ground. When driven to V_{OUT}, CAP– sources current from C_{OUT}. In all cases, current flow in the switches is unidirectional, as should be expected when using bipolar switches.

The OSC can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally, OSC is connected to the oscillator timing capacitor ($C_t \approx 150$ pF), which is alternately charged and discharged by current sources of ±7 μA, so that the duty cycle is approximately 50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be increased by adding an external capacitor (C2 in Figure 15) in the range of 5 pF – 20 pF from CAP+ to OSC. This capacitor couples a charge into C_t at the switch transitions. This shortens the charge and discharge time and raises the oscillator frequency. Synchronization can be accomplished by adding an external pullup resistor from OSC to V_{ref}. A 20-kΩ pullup resistor is recommended. An open-collector gate or an NPN transistor can then be used to drive OSC at the external clock frequency as shown in Figure 15.

The frequency can be lowered by adding an external capacitor (C_1 in Figure 15) from OSC to ground. This increases the charge and discharge times, which lowers the oscillator frequency.

APPLICATION INFORMATION



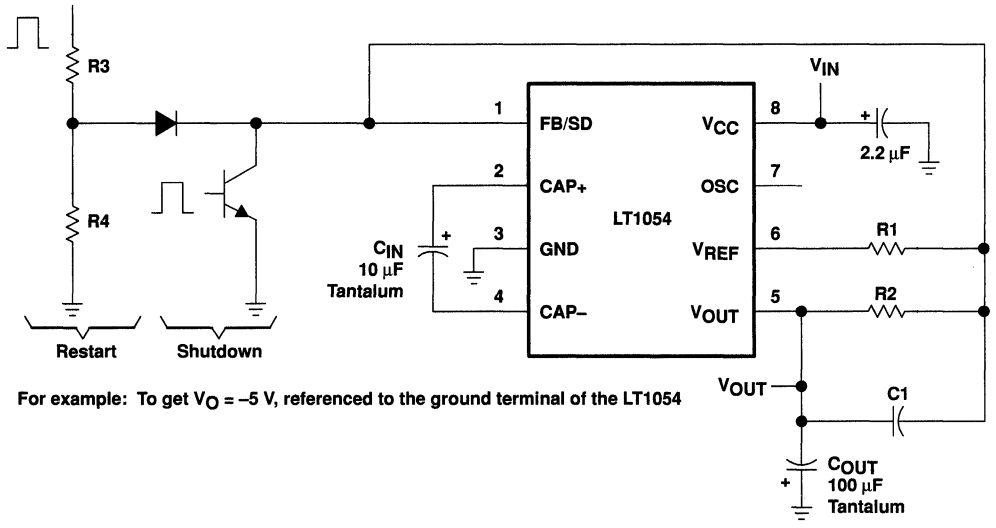
Pin numbers shown are for the P package.

Figure 15. External Clock System

The feedback/shutdown (FB/SD) terminal has two functions. Pulling FB/SD below the shutdown threshold (≈ 0.45 V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100 μA. Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation, the device will restart when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pulldown to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where the LT1054 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to FB/SD of the LT1054. Using the circuit shown in Figure 16, the restart signal can be either a pulse (t_p > 100 μs) or a logic high. Diode coupling the restart signal into FB/SD allows the output voltage to rise and regulate without overshoot. The resistor divider R3/R4 shown in Figure 16 should be chosen to provide a signal level at FB/SD of 0.7 V – 1.1 V.

FB/SD is also the inverting input of the LT1054 error amplifier and, as such, can be used to obtain a regulated output voltage.

APPLICATION INFORMATION



For example: To get V_O = –5 V, referenced to the ground terminal of the LT1054

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = 20\text{ k}\Omega\left(\frac{|-5\text{ V}|}{\frac{2.5\text{ V}}{2} - 40\text{ mV}} + 1\right) = 102.6\text{ k}\Omega^{\dagger}$$

Where: $R1 = 20\text{ k}\Omega$
$V_{REF} = 2.5\text{ V}$ Nominal

† Choose the closest 1% value.
Pin numbers shown are for the P package.

Figure 16. Basic Regulation Configuration

regulation

The error amplifier of the LT1054 drives the pnp switch to control the voltage across the input capacitor (C_{IN}), which determines the output voltage. When the reference and error amplifier of the LT1054 are used, an external resistive divider is all that is needed to set the regulated output voltage. Figure 16 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be 20 kΩ or greater because the reference current is limited to ±100 µA. R2 should be in the range of 100 kΩ to 300 kΩ. Frequency compensation is accomplished by adjusting the ratio of C_{IN} to C_{OUT}.

For best results, this ratio should be approximately 1 to 10. Capacitor C1, required for good load regulation, should be 0.002 µF for all output voltages.

The functional block diagram shows that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referenced to the ground terminal of the LT1054, must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves. Other configurations, such as the negative doubler, can provide higher voltages at reduced output currents.

APPLICATION INFORMATION

capacitor selection

While the exact values of C_{IN} and C_{OUT} are non-critical, good-quality low-ESR capacitors, such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN}, the effect of the ESR of the capacitor is multiplied by four, since switch currents are approximately two times higher than output current. Losses occur on both the charge and discharge cycle, which means that a capacitor with 1 Ω of ESR for C_{IN} has the same effect as increasing the output impedance of the LT1054 by 4 Ω. This represents a significant increase in the voltage losses. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current. The ESR of the capacitor causes a step function to occur in the output ripple at the switch transitions. This step function degrades the output regulation for changes in output load current and should be avoided. A technique used to gain both low ESR and reasonable cost is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor.

output ripple

The peak-to-peak output ripple is determined by the output capacitor and the output current values. Peak-to-peak output ripple is approximated as shown:

$$\Delta V = \frac{I_{OUT}}{2\ fC_{OUT}} \tag{5}$$

where:

ΔV = p-p ripple
f_{OSC} = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$$(2I_{OUT})\ (\text{ESR of } C_{OUT}) \tag{6}$$

power dissipation

The power dissipation of any LT1054 circuit must be limited so that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation is calculated from two components, the power loss due to voltage drops in the switches, and the power loss due to drive current losses. The total power dissipated by the LT1054 is calculated as shown.

$$P \approx (V_{CC} - |V_{OUT}|)\ I_{OUT} + (V_{CC})\ (I_{OUT})\ (0.2) \tag{7}$$

where both V_{CC} and V_{OUT} are referenced to ground. The power dissipation is equivalent to that of a linear regulator. Limited power-handling capability of the LT1054 packages causes limited output-current requirements or steps can be taken to dissipate power external to the LT1054 for large input or output differentials. This is accomplished by placing a resistor in series with C_{IN} as shown in Figure 17. A portion of the input voltage is dropped across this resistor without affecting the output regulation. Since switch current is approximately 2.2 times the output current and the resistor causes a voltage drop when C_{IN} is both charging and discharging, the resistor chosen is as shown:

$$R_X = V_X/(4.4\ I_{OUT})$$

where:

$$V_X \approx V_{CC} - [(\text{LT1054 voltage loss})\ (1.3) + |V_{OUT}|] \tag{8}$$

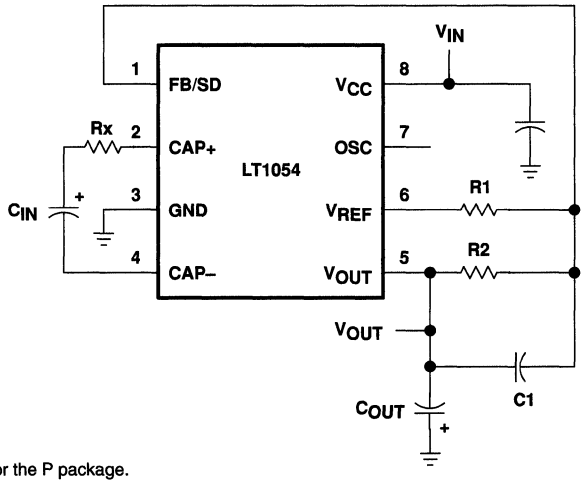
and I_{OUT} = maximum required output current. The factor of 1.3 allows some operating margin for the LT1054.

APPLICATION INFORMATION

When using a 12-V to –5-V converter at 100-mA output current, calculate the power dissipation without an external resistor.

$$P = (12\ V - |-5\ V|)\ (100\ mA) + (12\ V)\ (100\ mA)\ (0.2)$$

$$P = 700\ mW + 240\ mW = 940\ mW \quad (9)$$



Pin numbers shown are for the P package.

Figure 17. Power-Dissipation-Limiting Resistor in Series with C_{IN}

At $R_{\theta JA}$ of 130°C/W for a commercial plastic device, a junction temperature rise of 122°C is seen. The device exceeds the maximum junction temperature at an ambient temperature of 25°C. To calculate the power dissipation with an external resistor (R_X), determine how much voltage can be dropped across R_X. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100 mA output current is 1.6 V.

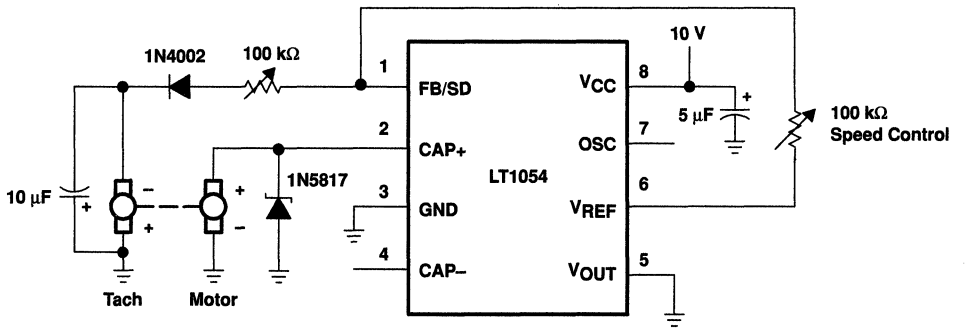
$$V_x = 12\ V - [(1.6\ V)\ (1.3) + |-5\ V|] = 4.9\ V$$

and

$$R_x = 4.9\ V/(4.4)\ (100\ mA) = 11\ \Omega \quad (10)$$

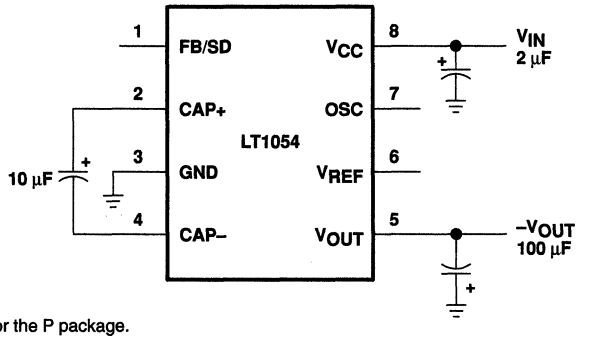
APPLICATION INFORMATION

The resistor reduces the power dissipated by the LT1054 by (4.9 V) (100 mA) = 490 mW. The total power dissipated by the LT1054 is equal to (940 mW – 490 mW) = 450 mW. The junction temperature rise is 58°C. Although commercial devices are functional up to a junction temperature of 125°C, the specifications are tested to a junction temperature of 100°C. In this example, this means limiting the ambient temperature to 42°C. To allow higher ambient temperatures, the thermal resistance numbers for the LT1054 packages represent worst-case numbers with no heat sinking and still air. Small clip-on heat sinks can be used to lower the thermal resistance of the LT1054 package. Airflow in some systems helps to lower the thermal resistance. Wide PC board traces from the LT1054 leads help to remove heat from the device. This is especially true for plastic packages.



NOTE: Motor-Tach Canon CKT26-T5-3SAE
Pin numbers shown are for the P package.

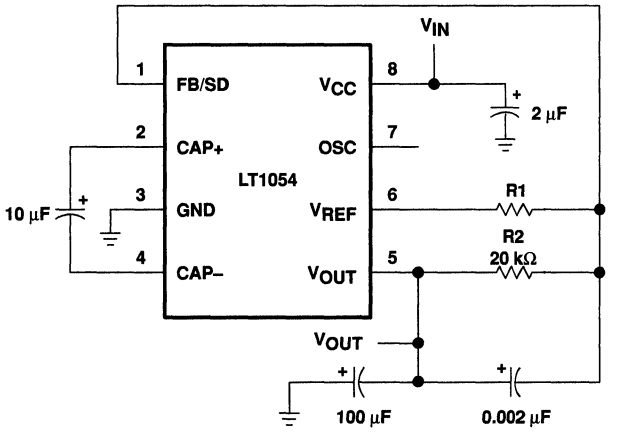
Figure 18. Motor Speed Servo



Pin numbers shown are for the P package.

Figure 19. Basic Voltage Inverter

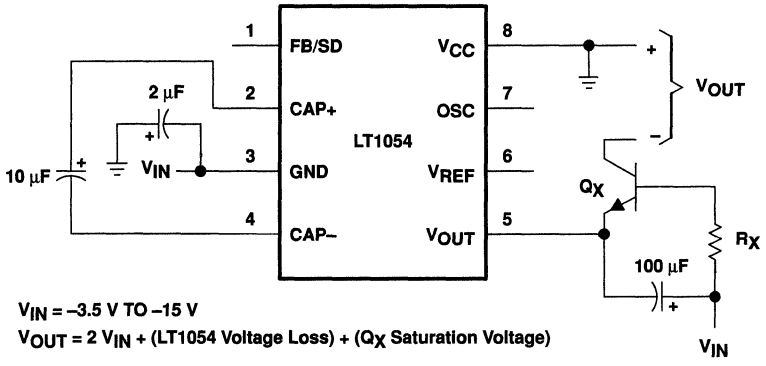
APPLICATION INFORMATION



$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = 20\ k\Omega\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

Pin numbers shown are for the P package.

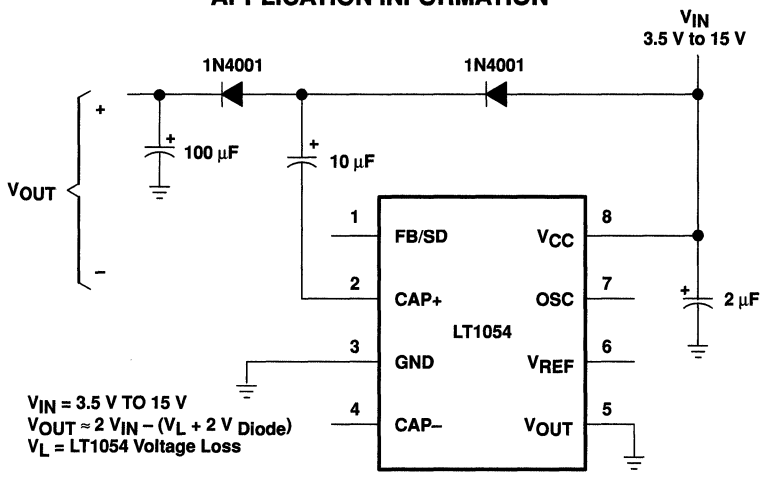
Figure 20. Basic Voltage Inverter/Regulator



Pin numbers shown are for the P package.

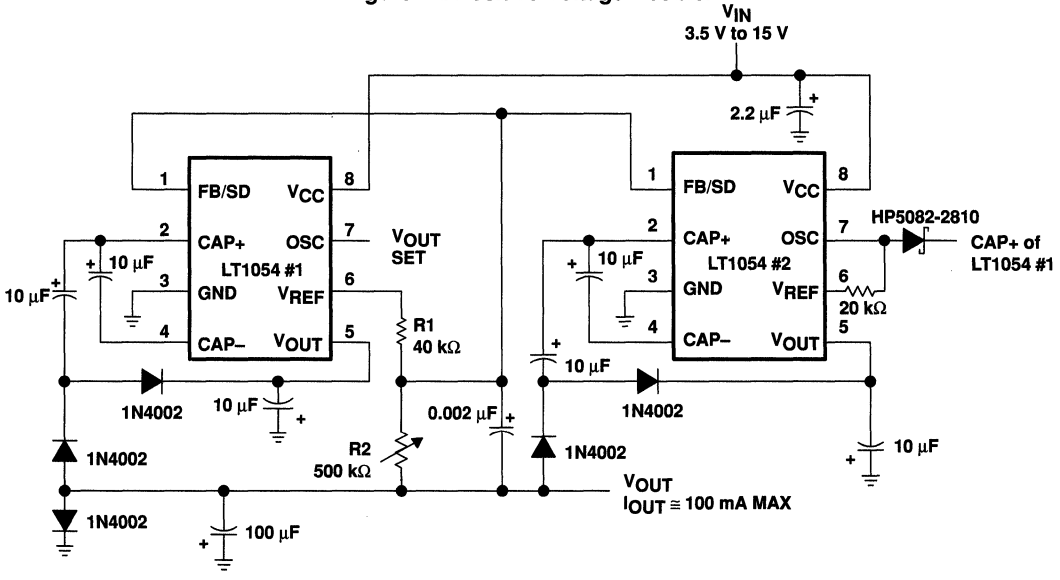
Figure 21. Negative-Voltage Doubler

APPLICATION INFORMATION



Pin numbers shown are for the P package.

Figure 22. Positive-Voltage Doubler



V_{IN} = 3.5 V to 15 V

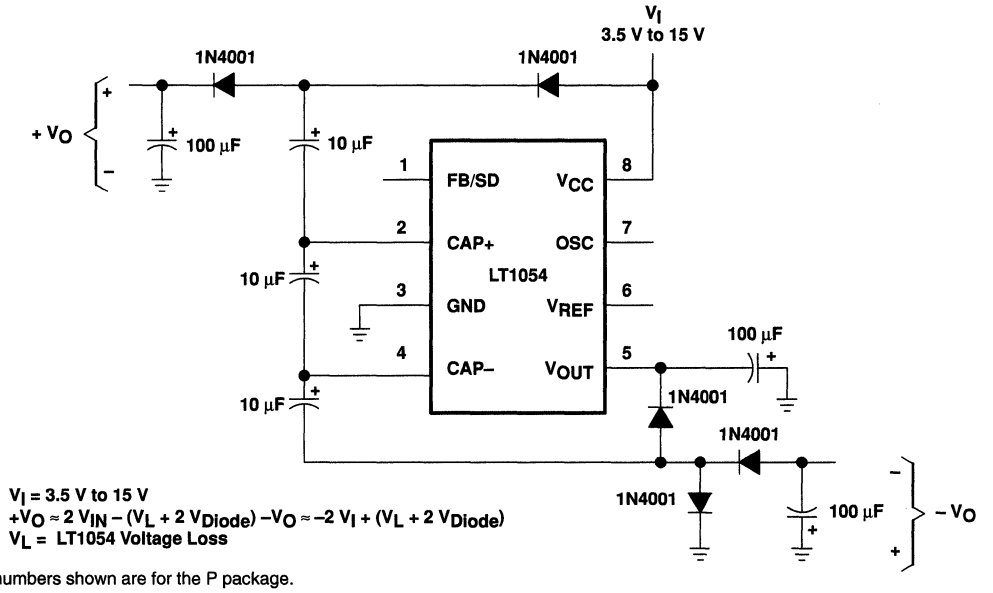
V_{OUT} MAX ≈ –2 V_{IN} + [LT1054 Voltage Loss +2 (V_{Diode})]

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

Pin numbers shown are for the P package.

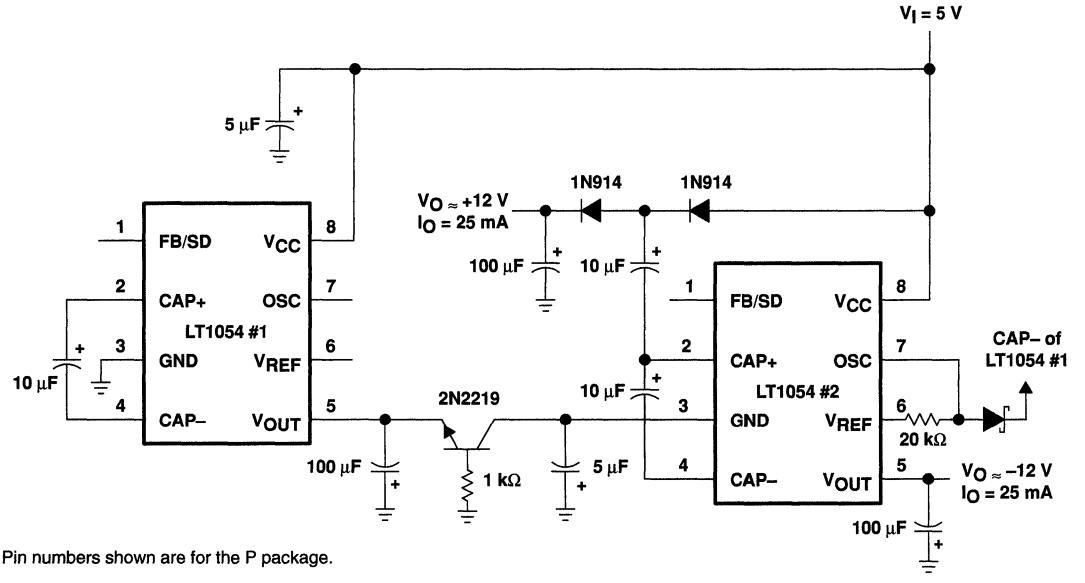
Figure 23. 100-mA Regulating Negative Doubler

APPLICATION INFORMATION



Pin numbers shown are for the P package.

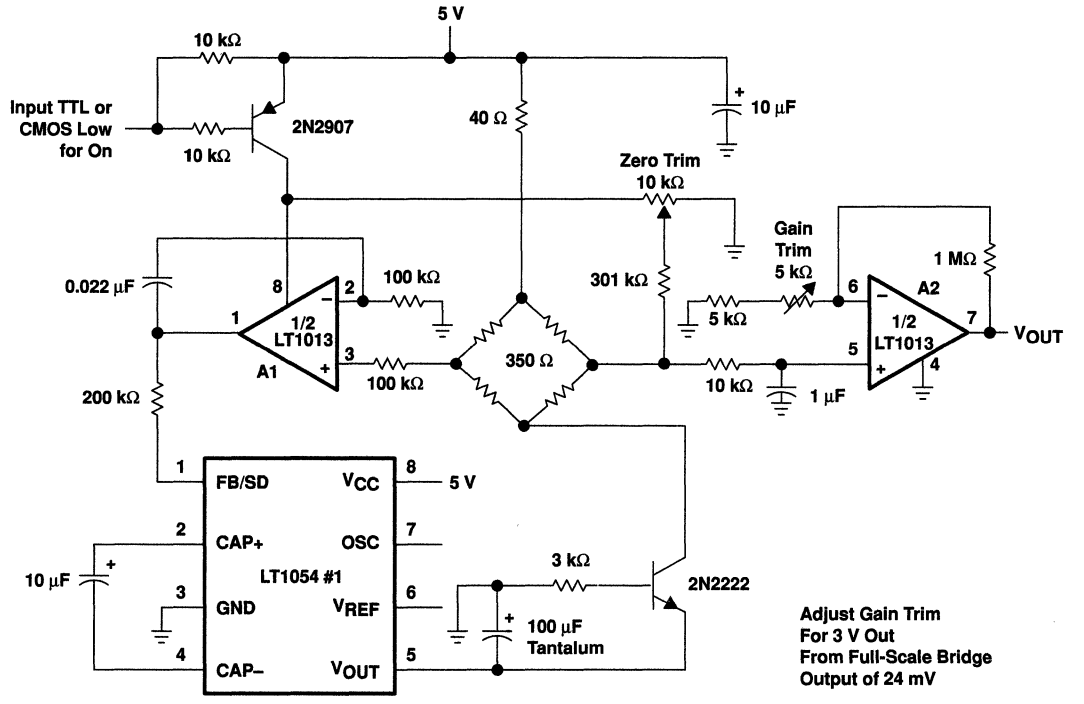
Figure 24. Dual-Output Voltage Doubler



Pin numbers shown are for the P package.

Figure 25. 5-V to ±12-V Converter

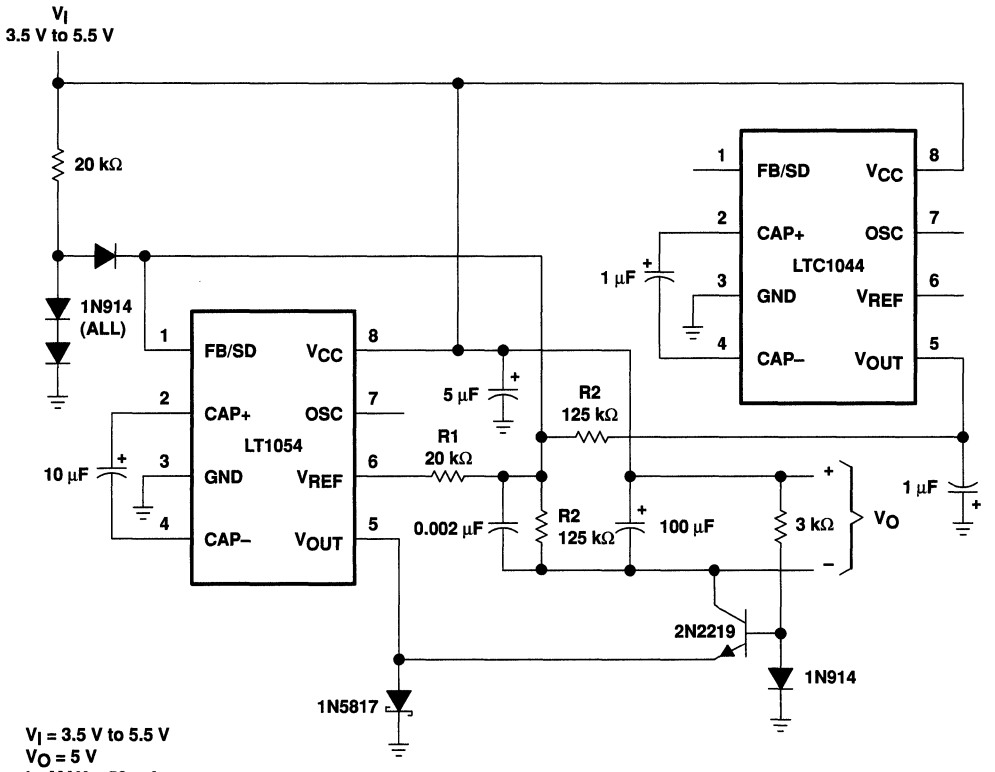
APPLICATION INFORMATION



Pin numbers shown are for the P package.

Figure 26. Strain-Gage Bridge Signal Conditioner

APPLICATION INFORMATION



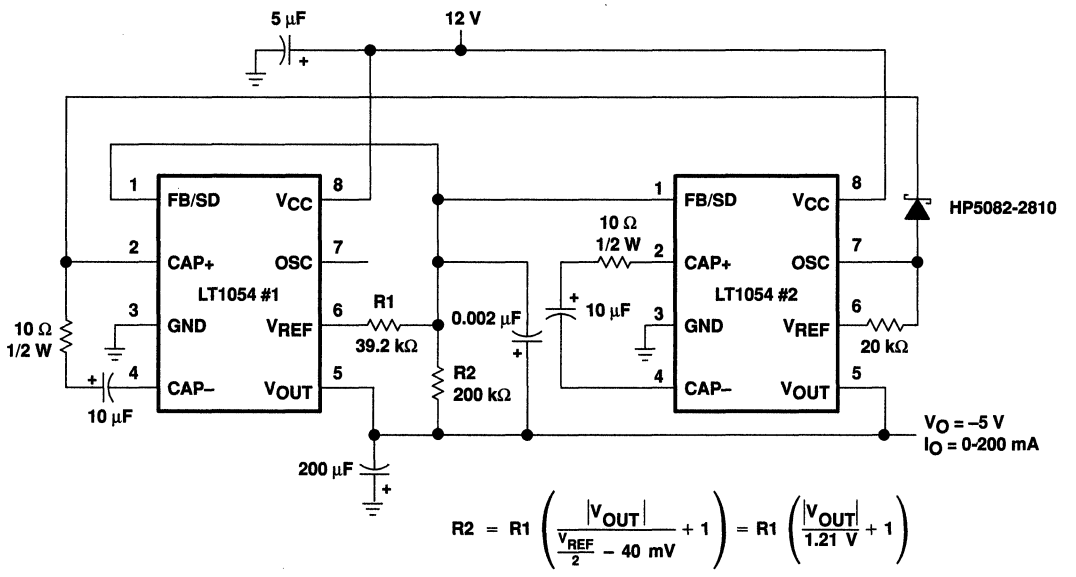
V_I = 3.5 V to 5.5 V
V_O = 5 V
I_O MAX = 50 mA

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

Pin numbers shown are for the P package.

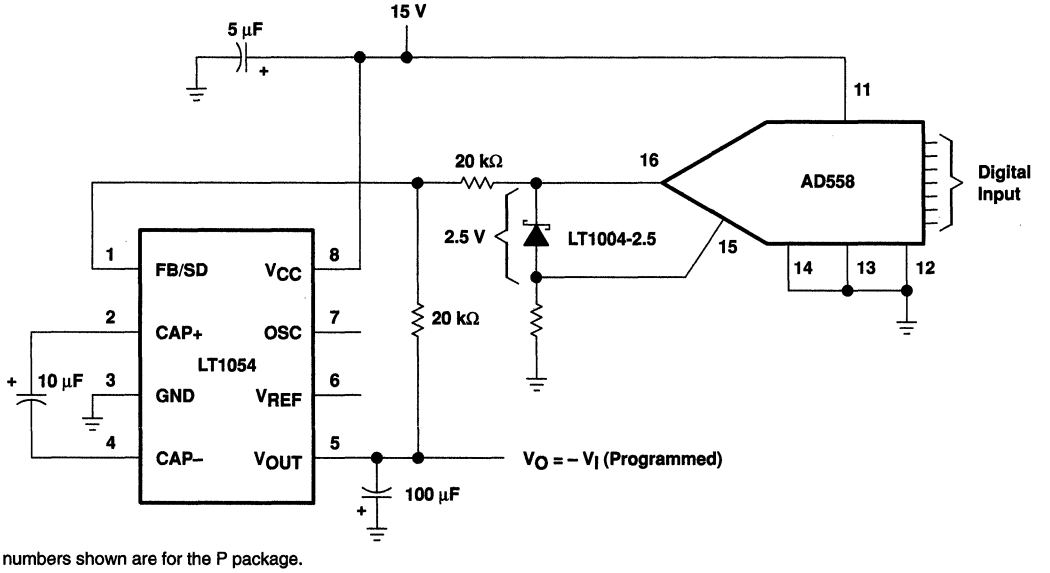
Figure 27. 3.5-V to 5-V Regulator

APPLICATION INFORMATION



Pin numbers shown are for the P package.

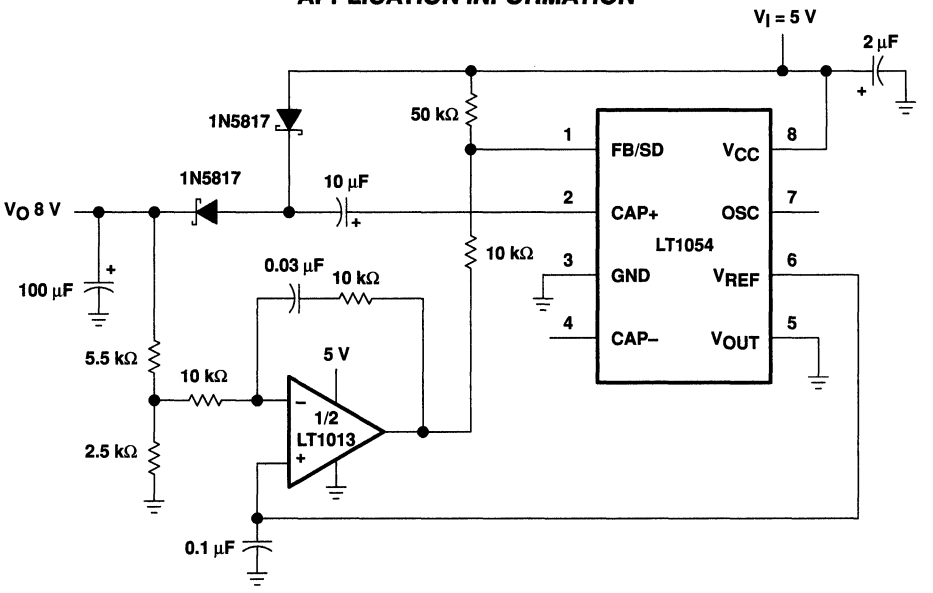
Figure 28. Regulating 200-mA + 12-V to –5-V Converter



Pin numbers shown are for the P package.

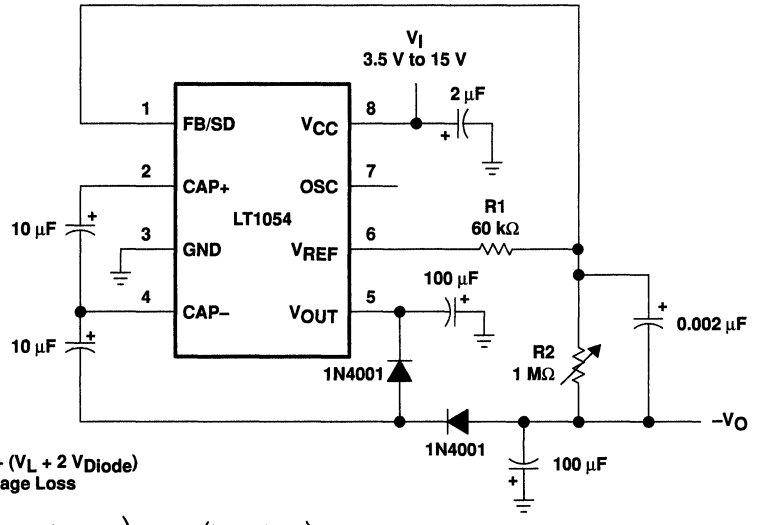
Figure 29. Digitally Programmable Negative Supply

APPLICATION INFORMATION



Pin numbers shown are for the P package.

Figure 30. Positive Doubler With Regulation (5-V to 8-V Converter)



V_I = 3.5 V to 15 V
V_O MAX ≈ 2 V_{IN} + (V_L + 2 V_{Diode})
V_L = LT1054 Voltage Loss

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

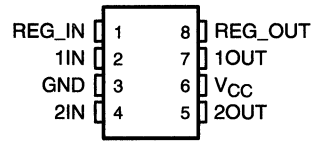
Pin numbers shown are for the P package.

Figure 31. Negative Doubler With Regulator

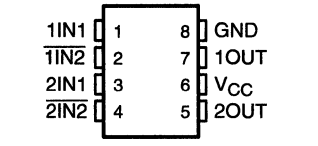
SLVS132D – NOVEMBER 1995 – REVISED NOVEMBER 1997

- **Industry-Standard Driver Replacement**
- **25-ns Max Rise/Fall Times and 40-ns Max Propagation Delay – 1-nF Load, V_{CC} = 14 V**
- **2-A Peak Output Current, V_{CC} = 14 V**
- **5-μA Supply Current — Input High or Low**
- **4-V to 14-V Supply-Voltage Range; Internal Regulator Extends Range to 40 V (TPS2811, TPS2812, TPS2813)**
- **–40°C to 125°C Ambient-Temperature Operating Range**

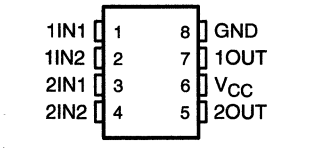
TPS2811, TPS2812, TPS2813 . . . D, P, AND PW PACKAGES
(TOP VIEW)



TPS2814 . . . D, P, AND PW PACKAGES
(TOP VIEW)



TPS2815 . . . D, P, AND PW PACKAGES
(TOP VIEW)



description

The TPS28xx series of dual high-speed MOSFET drivers are capable of delivering peak currents of 2 A into highly capacitive loads. This performance is achieved with a design that inherently minimizes shoot-through current and consumes an order of magnitude less supply current than competitive products.

The TPS2811, TPS2812, and TPS2813 drivers include a regulator to allow operation with supply inputs between 14 V and 40 V. The regulator output can power other circuitry, provided power dissipation does not exceed package limitations. When the regulator is not required, REG_IN and REG_OUT can be left disconnected or both can be connected to V_{CC} or GND.

The TPS2814 and the TPS2815 have 2-input gates that give the user greater flexibility in controlling the MOSFET. The TPS2814 has AND input gates with one inverting input. The TPS2815 has dual-input NAND gates.

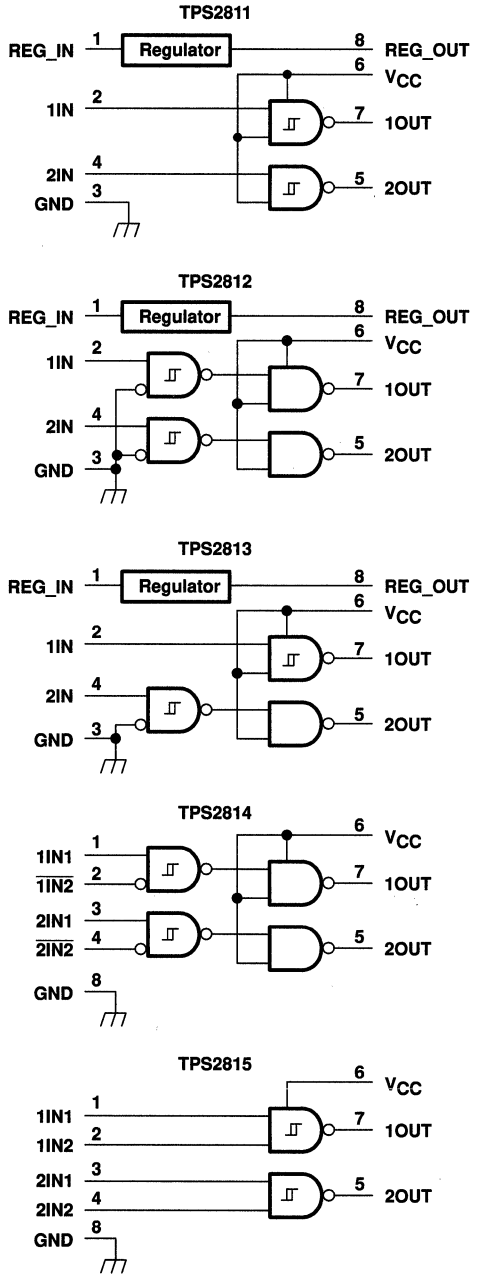
TPS28xx series drivers, available in 8-pin PDIP, SOIC, and TSSOP packages and as unmounted ICs, operate over a ambient temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

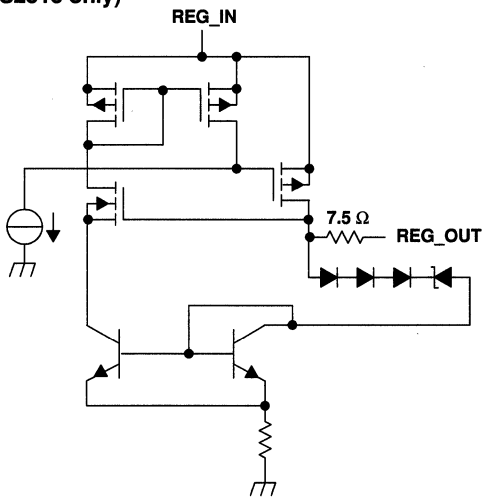
T_A	INTERNAL REGULATOR	LOGIC FUNCTION	PACKAGED DEVICES			CHIP FORM (Y)
			SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 125°C	Yes	Dual inverting drivers	TPS2811D	TPS2811P	TPS2811PWLE	TPS2811Y
		Dual noninverting drivers	TPS2812D	TPS2812P	TPS2812PWLE	TPS2812Y
		One inverting and one noninverting driver	TPS2813D	TPS2813P	TPS2813PWLE	TPS2813Y
	No	Dual 2-input AND drivers, one inverting input on each driver	TPS2814D	TPS2814P	TPS2814PWLE	TPS2814Y
		Dual 2-input NAND drivers	TPS2815D	TPS2815P	TPS2815PWLE	TPS2815Y

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS2811DR). The PW package is only available left-end taped and reeled and is indicated by the LE suffix on the device type (e.g., TPS2811PWLE).

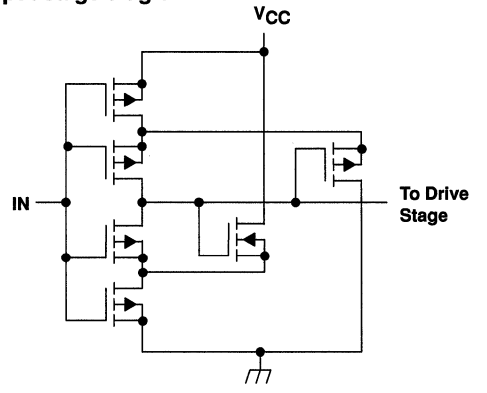
functional block diagram



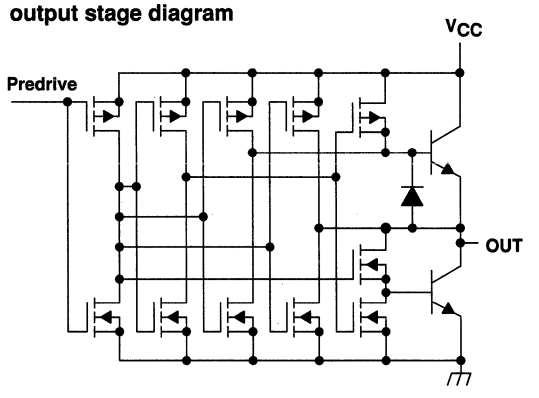
regulator diagram (TPS2811, TPS2812, TPS2813 only)



input stage diagram



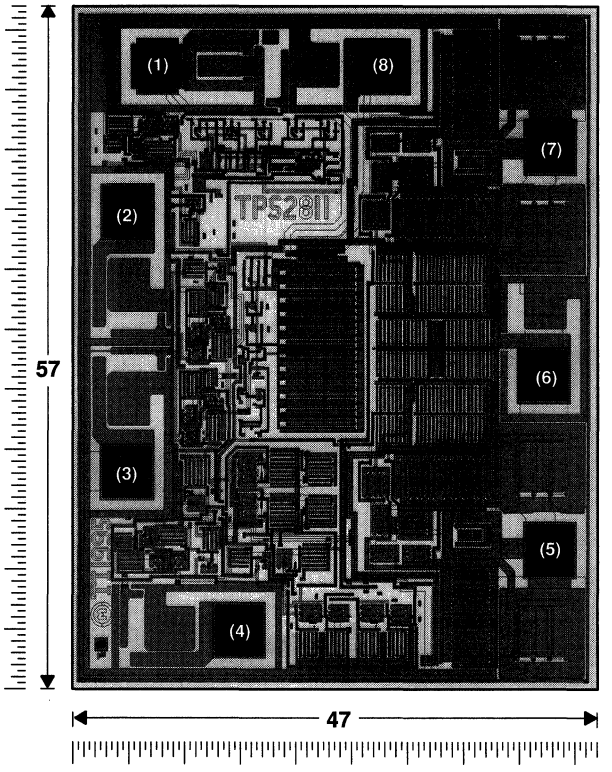
output stage diagram

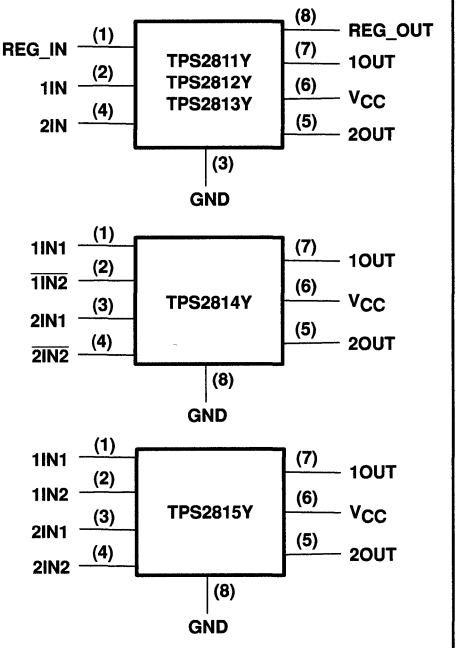


TPS28xxY chip information

This chip, when properly assembled, displays characteristics similar to those of the TPS28xx. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max OPERATING TEMPERATURE = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TPS2811, TPS2812, TPS2813

TERMINAL NAME	TERMINAL NUMBERS			DESCRIPTION
	TPS2811 Dual Inverting Drivers	TPS2812 Dual Noninverting Drivers	TPS2813 Complimentary Drivers	
REG_IN	1	1	1	Regulator input
1IN	2	2	2	Input 1
GND	3	3	3	Ground
2IN	4	4	4	Input 2
2OUT	5 = $\overline{2IN}$	5 = 2IN	5 = 2IN	Output 2
V_{CC}	6	6	6	Supply voltage
1OUT	7 = $\overline{1IN}$	7 = 1IN	7 = $\overline{1IN}$	Output 1
REG_OUT	8	8	8	Regulator output

TPS2814, TPS2815

TERMINAL NAME	TERMINAL NUMBERS		DESCRIPTION
	TPS2814 Dual AND Drivers with Single Inverting Input	TPS2815 Dual NAND Drivers	
1IN1	1	1	Noninverting input 1 of driver 1
$\overline{1IN2}$	2	-	Inverting input 2 of driver 1
1IN2	-	2	Noninverting input 2 of driver 1
2IN1	3	3	Noninverting input 1 of driver 2
$\overline{2IN2}$	4	-	Inverting input 2 of driver 2
2IN2	-	4	Noninverting input 2 of driver 2
2OUT	5 = 2IN1 • $\overline{2IN2}$	5 = $\overline{2IN1}$ • $\overline{2IN2}$	Output 2
V_{CC}	6	6	Supply voltage
1OUT	7 = 1IN1 • $\overline{1IN2}$	7 = $\overline{1IN1}$ • $\overline{1IN2}$	Output 1
GND	8	8	Ground

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
P	1090 mW	8.74 mW/°C	697 mW	566 mW
D	730 mW	5.84 mW/°C	467 mW	380 mW
PW	520 mW	4.17 mW/°C	332 mW	270 mW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Regulator input voltage range, REG_IN ..... −0.3 V to 42 V
Supply voltage, V_{CC} ..... −0.3 V to 15 V
Input voltage range, 1IN, 2IN, 1IN1, 1IN2, $\overline{1IN2}$, 2IN1, 2IN2, $\overline{2IN2}$ ..... −0.3 V to V_{CC}
Continuous regulator output current, REG_OUT ..... 25 mA
Continuous output current, 1OUT, 2OUT ..... ±100 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating ambient temperature range, T_A ..... −40°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to device GND pin.

recommended operating conditions

	MIN	MAX	UNIT
Regulator input voltage range	8	40	V
Supply voltage, V_{CC}	4	14	V
Input voltage, 1IN1, 1IN2, $\overline{1IN2}$, 2IN1, 2IN2, $\overline{2IN2}$, 1IN, 2IN	−0.3	V_{CC}	V
Continuous regulator output current, REG_OUT	0	20	mA
Ambient temperature operating range	−40	125	°C

TPS28xx electrical characteristics over recommended operating ambient temperature range, V_{CC} = 10 V, REG_IN open for TPS2811/12/13, C_L = 1 nF (unless otherwise noted)

inputs

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Positive-going input threshold voltage	V_{CC} = 5 V		3.3	4	V
	V_{CC} = 10 V		5.8	9	V
	V_{CC} = 14 V		8.3	13	V
Negative-going input threshold voltage	V_{CC} = 5 V	1	1.6		V
	V_{CC} = 10 V	1	4.2		V
	V_{CC} = 14 V	1	6.2		V
Input hysteresis	V_{CC} = 5 V		1.6		V
Input current	Inputs = 0 V or V_{CC}	−1	0.2	1	µA
Input capacitance			5	10	pF

† Typicals are for T_A = 25°C unless otherwise noted.

outputs

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
High-level output voltage	I_O = −1 mA	9.75	9.9		V
	I_O = −100 mA	8	9.1		
Low-level output voltage	I_O = 1 mA		0.18	0.25	V
	I_O = 100 mA		1	2	
Peak output current	V_{CC} = 10 V		2		A

† Typicals are for T_A = 25°C unless otherwise noted.

regulator (TPS2811/2812/2813 only)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage	14 ≤ REG_IN ≤ 40 V, 0 ≤ I_O ≤ 20 mA	10	11.5	13	V
Output voltage in dropout	I_O = 10 mA, REG_IN = 10 V	9	9.6		V

† Typicals are for T_A = 25°C unless otherwise noted.

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply current into V_{CC}	Inputs high or low		0.2	5	µA
Supply current into REG_IN	REG_IN = 20 V, REG_OUT open		40	100	µA

† Typicals are for T_A = 25°C unless otherwise noted.

TPS28xxY electrical characteristics at T_A = 25°C, V_{CC} = 10 V, REG_IN open for TPS2811/12/13, C_L = 1 nF (unless otherwise noted)

inputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-going input threshold voltage	V_{CC} = 5 V		3.3		V
	V_{CC} = 10 V		5.8		V
	V_{CC} = 14 V		8.2		V
Negative-going input threshold voltage	V_{CC} = 5 V		1.6		V
	V_{CC} = 10 V		3.3		V
	V_{CC} = 14 V		4.2		V
Input hysteresis	V_{CC} = 5 V		1.2		V
Input current	Inputs = 0 V or V_{CC}		0.2		µA
Input capacitance			5		pF

outputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage	I_O = –1 mA		9.9		V
	I_O = –100 mA		9.1		
Low-level output voltage	I_O = 1 mA		0.18		V
	I_O = 100 mA		1		
Peak output current	V_{CC} = 10.5 V		2		A

regulator (TPS2811, 2812, 2813)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	14 ≤ REG_IN ≤ 40 V, 0 ≤ I_O ≤ 20 mA		11.5		V
Output voltage in dropout	I_O = 10 mA, REG_IN = 10 V		9.6		V

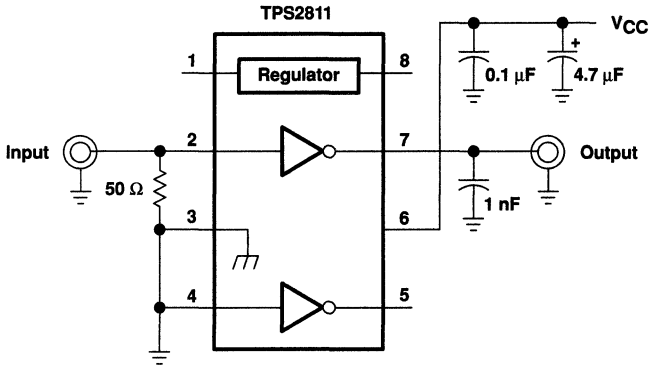
power supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current into V_{CC}	Inputs high or low		0.2		µA
Supply current into REG_IN	REG_IN = 20 V, REG_OUT open		40		µA

switching characteristics for all devices over recommended operating ambient temperature range, REG_IN open for TPS2811/12/13, C_L = 1 nF (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_{CC} = 14 V		14	25	ns
		V_{CC} = 10 V		15	30	
		V_{CC} = 5 V		20	35	
t_f	Fall time	V_{CC} = 14 V		15	25	ns
		V_{CC} = 10 V		15	30	
		V_{CC} = 5 V		18	35	
t_{PHL}	Prop delay time high-to-low-level output	V_{CC} = 14 V		25	40	ns
		V_{CC} = 10 V		25	45	
		V_{CC} = 5 V		34	50	
t_{PLH}	Prop delay time low-to-high-level output	V_{CC} = 14 V		24	40	ns
		V_{CC} = 10 V		26	45	
		V_{CC} = 5 V		36	50	

PARAMETER MEASUREMENT INFORMATION



NOTE A. Input rise and fall times should be ≤10 ns for accurate measurement of ac parameters.

Figure 1. Test Circuit For Measurement of Switching Characteristics

PARAMETER MEASUREMENT INFORMATION

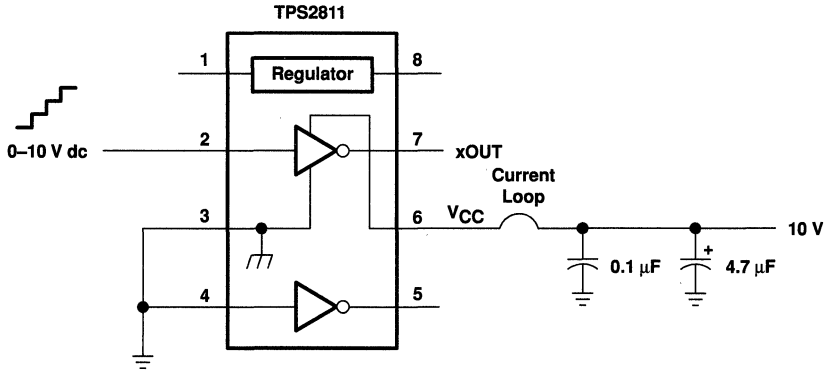


Figure 2. Shoot-through Current Test Setup

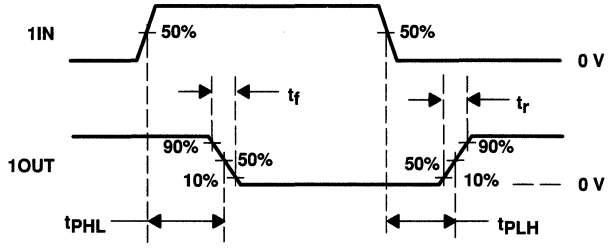


Figure 3. Typical Timing Diagram (TPS2811)

TYPICAL CHARACTERISTICS

Tables of Characteristics Graphs and Application Information

typical characteristics

PARAMETER	vs PARAMETER 2	FIGURE	PAGE
Rise time	Supply voltage	4	10
Fall time	Supply voltage	5	10
Propagation delay time	Supply voltage	6, 7	10
Supply current	Supply voltage	8	11
	Load capacitance	9	11
	Ambient temperature	10	11
Input threshold voltage	Supply voltage	11	11
Regulator output voltage	Regulator input voltage	12, 13	12
Regulator quiescent current	Regulator input voltage	14	12
Peak source current	Supply voltage	15	12
Peak sink current	Supply voltage	16	13
Shoot-through current	Input voltage, high-to-low	17	13
	Input voltage, low-to-high	18	13

TYPICAL CHARACTERISTICS

Tables of Characteristics Graphs and Application Information (Continued)

general applications

PARAMETER	vs PARAMETER 2		FIGURE	PAGE
Switching test circuits and application information			19, 20	15
Voltage of 1OUT vs 2OUT	Time	Low-to-high	21, 23, 25	16, 17
		High-to-low	22, 24, 26	16, 17

circuit for measuring paralleled switching characteristics

PARAMETER	vs PARAMETER 2		FIGURE	PAGE
Switching test circuits and application information			27	17
Input voltage vs output voltage	Time	Low-to-high	28, 30	18
		High-to-low	29, 31	18

Hex-1 to Hex-4 application information

PARAMETER	vs PARAMETER 2		FIGURE	PAGE
Driving test circuit and application information			32	19
Drain-source voltage vs drain current	Time	Hex-1 size	33	20
		Hex-2 size	36	20
		Hex-3 size	39	21
		Hex-4 size	41	22
		Hex-4 size parallel drive	45	23
Drain-source voltage vs gate-source voltage at turn-on	Time	Hex-1 size	34	20
		Hex-2 size	37	21
		Hex-3 size	40	21
		Hex-4 size	43	22
		Hex-4 size parallel drive	46	23
Drain-source voltage vs gate-source voltage at turn-off	Time	Hex-1 size	35	20
		Hex-2 size	38	21
		Hex-3 size	42	22
		Hex-4 size	44	22
		Hex-4 size parallel drive	47	23

synchronous buck regulator application

PARAMETER	vs PARAMETER 2		FIGURE	PAGE
3.3-V 3-A Synchronous-Rectified Buck Regulator Circuit			48	24
Q1 drain voltage vs gate voltage at turn-on	Time		49	26
Q1 drain voltage vs gate voltage at turn-off			50	26
Q1 drain voltage vs Q2 gate-source voltage			51, 52, 53	26, 27
Output ripple voltage vs inductor current		3 A	54	27
		5 A	55	27

TYPICAL CHARACTERISTICS

RISE TIME
vs
SUPPLY VOLTAGE

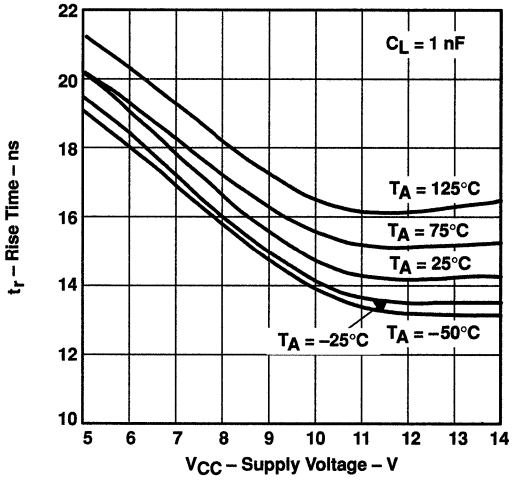


Figure 4

FALL TIME
vs
SUPPLY VOLTAGE

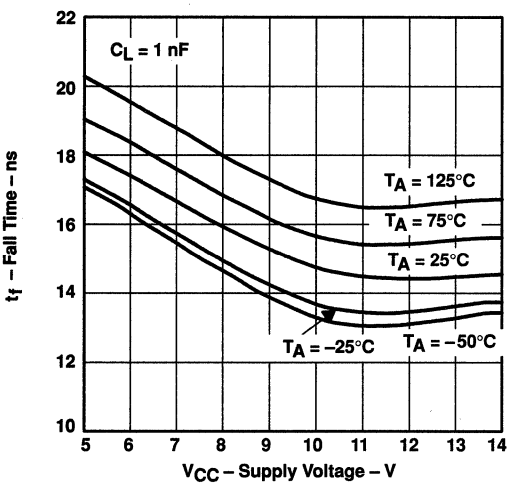


Figure 5

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

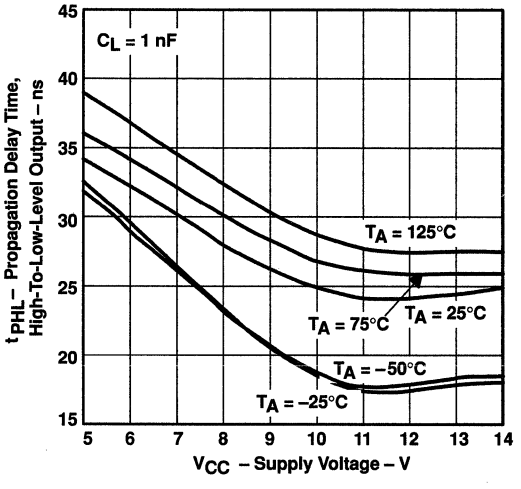


Figure 6

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

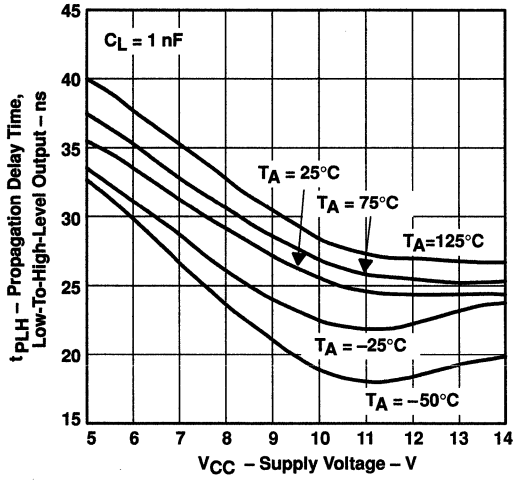


Figure 7

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

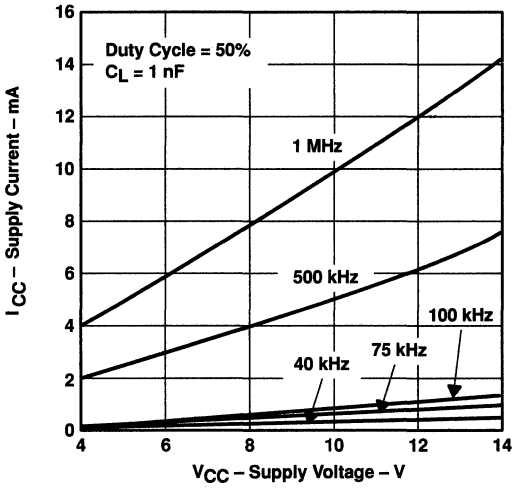


Figure 8

SUPPLY CURRENT
vs
LOAD CAPACITANCE

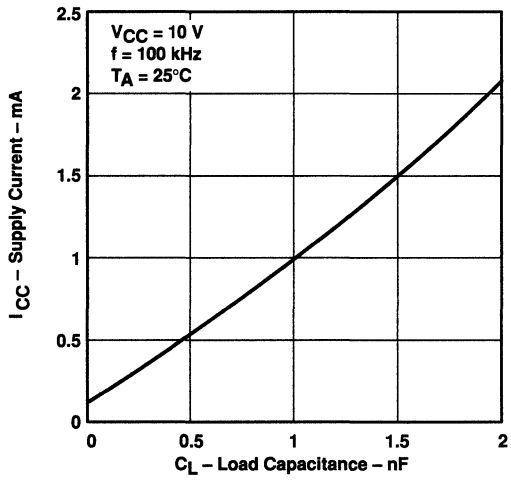


Figure 9

SUPPLY CURRENT
vs
AMBIENT TEMPERATURE

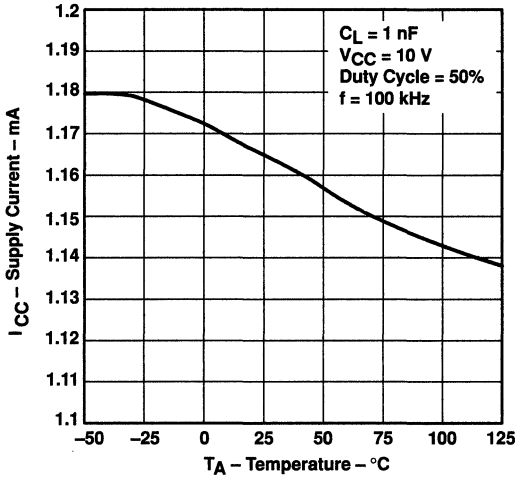


Figure 10

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

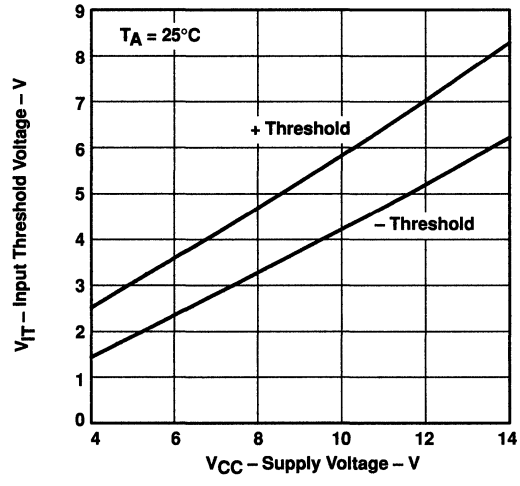


Figure 11

TYPICAL CHARACTERISTICS

REGULATOR OUTPUT VOLTAGE
vs
REGULATOR INPUT VOLTAGE

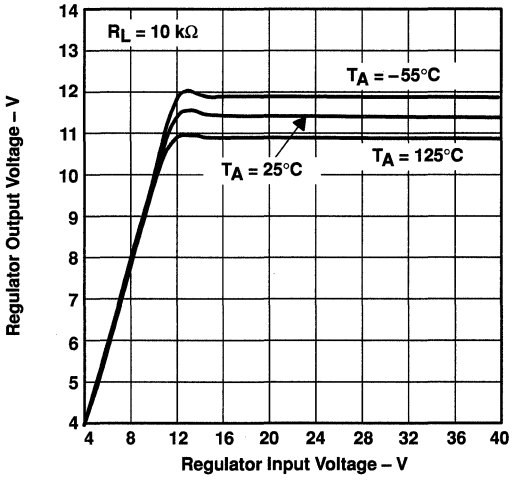


Figure 12

REGULATOR OUTPUT VOLTAGE
vs
REGULATOR INPUT VOLTAGE

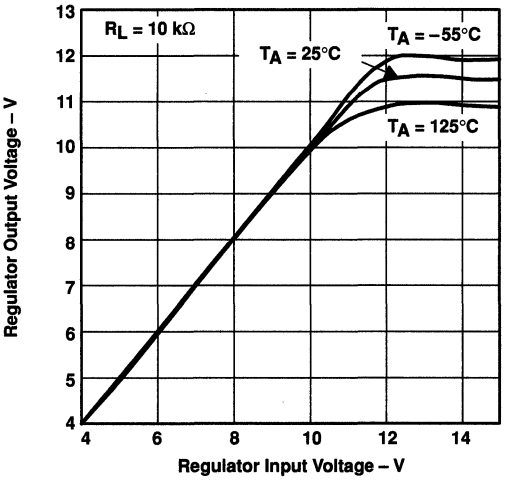


Figure 13

REGULATOR QUIESCENT CURRENT
vs
REGULATOR INPUT VOLTAGE

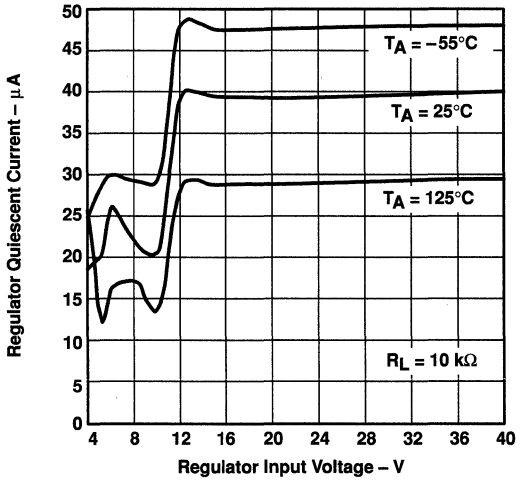


Figure 14

PEAK SOURCE CURRENT
vs
SUPPLY VOLTAGE

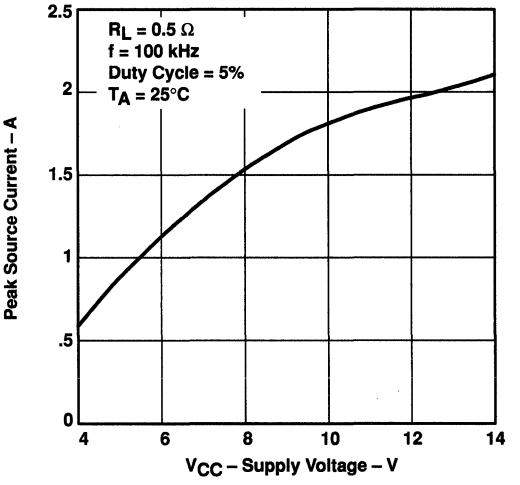


Figure 15

TYPICAL CHARACTERISTICS

PEAK SINK CURRENT
vs
SUPPLY VOLTAGE

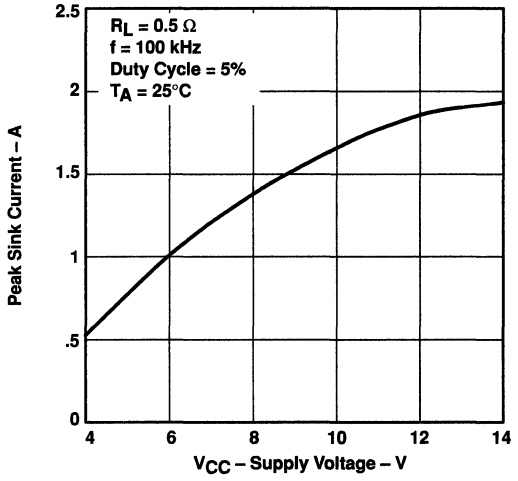


Figure 16

SHOOT-THROUGH CURRENT
vs
INPUT VOLTAGE, HIGH-TO-LOW

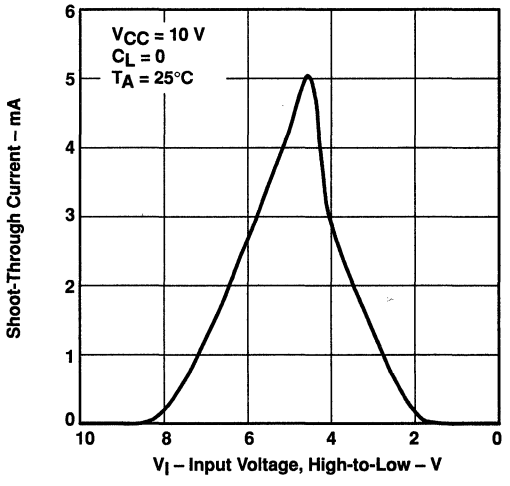


Figure 17

SHOOT-THROUGH CURRENT
vs
INPUT VOLTAGE, LOW-TO-HIGH

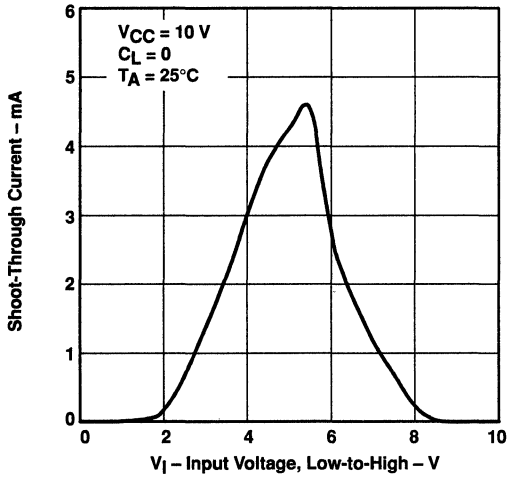


Figure 18

APPLICATION INFORMATION

The TPS2811, TPS2812 and TPS2813 circuits each contain one regulator and two MOSFET drivers. The regulator can be used to limit V_{CC} to between 10 V and 13 V for a range of input voltages from 14 V to 40 V, while providing up to 20 mA of dc drive. The TPS2814 and TPS2815 both contain two drivers, each of which has two inputs. The TPS2811 has inverting drivers, the TPS2812 has noninverting drivers, and the TPS2813 has one inverting and one noninverting driver. The TPS2814 is a dual 2-input AND driver with one inverting input on each driver, and the TPS2815 is a dual 2-input NAND driver. These MOSFET drivers are capable of supplying up to 2.1 A or sinking up to 1.9 A (see Figures 15 and 16) of instantaneous current to n-channel or p-channel MOSFETs. The TPS2811 family of MOSFET drivers have very fast switching times combined with very short propagation delays. These features enhance the operation of today's high-frequency circuits.

The CMOS input circuit has a positive threshold of approximately 2/3 of V_{CC}, with a negative threshold of 1/3 of V_{CC}, and a very high input impedance in the range of 10^9 Ω. Noise immunity is also very high because of the Schmidt trigger switching. In addition, the design is such that the normal shoot-through current in CMOS (when the input is biased halfway between V_{CC} and ground) is limited to less than 6 mA. The limited shoot-through is evident in the graphs in Figures 17 and 18. The input stage shown in the functional block diagram better illustrates the way the front end works. The circuitry of the device is such that regardless of the rise and/or fall time of the input signal, the output signal will always have a fast transition speed; this basically isolates the waveforms at the input from the output. Therefore, the specified switching times are not affected by the slopes of the input waveforms.

The basic driver portion of the circuits operate over a supply voltage range of 4 V to 14 V with a maximum bias current of 5 μA. Each driver consists of a CMOS input and a buffered output with a 2-A instantaneous drive capability. They have propagation delays of less than 30 ns and rise and fall times of less than 20 ns each. Placing a 0.1-μF ceramic capacitor between V_{CC} and ground is recommended; this will supply the instantaneous current needed by the fast switching and high current surges of the driver when it is driving a MOSFET.

The output circuit is also shown in the functional block diagram. This driver uses a unique combination of a bipolar transistor in parallel with a MOSFET for the ability to swing from V_{CC} to ground while providing 2 A of instantaneous driver current. This unique parallel combination of bipolar and MOSFET output transistors provides the drive required at V_{CC} and ground to guarantee turn-off of even low-threshold MOSFETs. Typical bipolar-only output devices don't easily approach V_{CC} or ground.

The regulator, included in the TPS2811, TPS2812 and TPS2813, has an input voltage range of 14 V to 40 V. It produces an output voltage of 10 V to 13 V and is capable of supplying from 0 to 20 mA of output current. In grounded source applications, this extends the overall circuit operation to 40 V by clamping the driver supply voltage (V_{CC}) to a safe level for both the driver and the MOSFET gate. The bias current for full operation is a maximum of 150 μA. A 0.1-μF capacitor connected between the regulator output and ground is required to ensure stability. For transient response, an additional 4.7-μF electrolytic capacitor on the output and a 0.1-μF ceramic capacitor on the input will optimize the performance of this circuit. When the regulator is not in use, it can be left open at both the input and the output, or the input can be shorted to the output and tied to either the V_{CC} or the ground pin of the chip.

APPLICATION INFORMATION

matching and paralleling connections

Figures 21 and 22 show the delays for the rise and fall time of each channel. As can be seen on a 5-ns scale, there is very little difference between the two channels at no load. Figures 23 and 24 show the difference between the two channels for a 1-nF load on each output. There is a slight delay on the rising edge, but little or no delay on the falling edge. As an example of extreme overload, Figures 25 and 26 show the difference between the two channels, or two drivers in the package, each driving a 10-nF load. As would be expected, the rise and fall times are significantly slowed down. Figures 28 and 29 show the effect of paralleling the two channels and driving a 1-nF load. A noticeable improvement is evident in the rise and fall times of the output waveforms. Finally, Figures 30 and 31 show the two drivers being paralleled to drive the 10-nF load and as could be expected the waveforms are improved. In summary, the paralleling of the two drivers in a package enhances the capability of the drivers to handle a larger load. Because of manufacturing tolerances, it is not recommended to parallel drivers that are not in the same package.

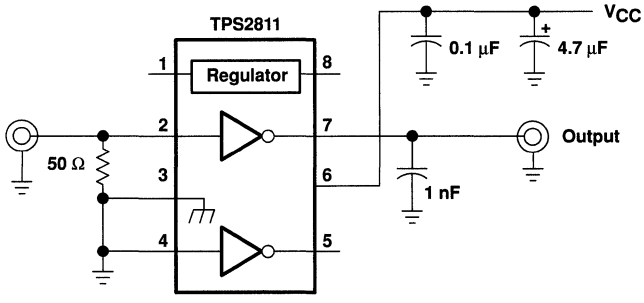
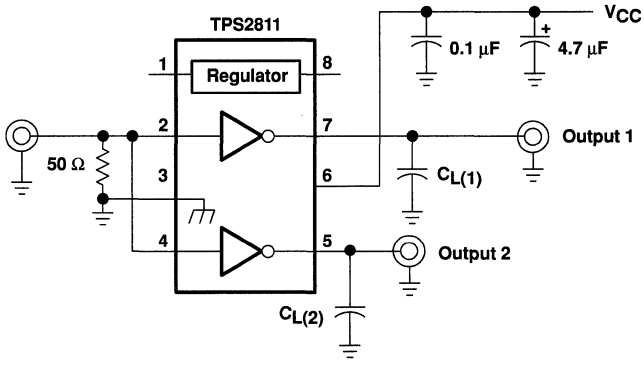


Figure 19. Test Circuit for Measuring Switching Characteristics



NOTE A: Input rise and fall times should be ≤10 ns for accurate measurement of ac parameters.

Figure 20. Test Circuit for Measuring Switching Characteristics with the Inputs Connected in Parallel

APPLICATION INFORMATION

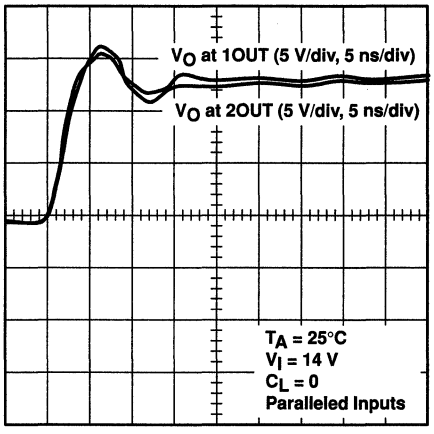


Figure 21. Voltage of 1OUT vs Voltage at 2OUT, Low-to-High Output Delay

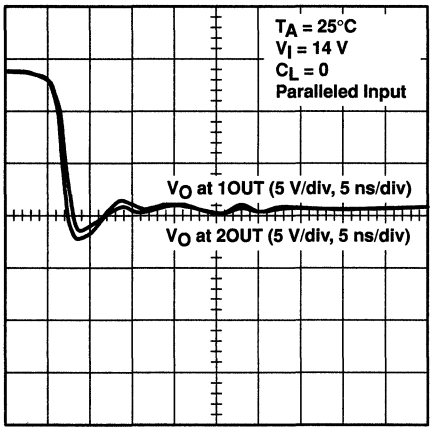


Figure 22. Voltage at 1OUT vs Voltage at 2OUT, High-to-Low Output Delay

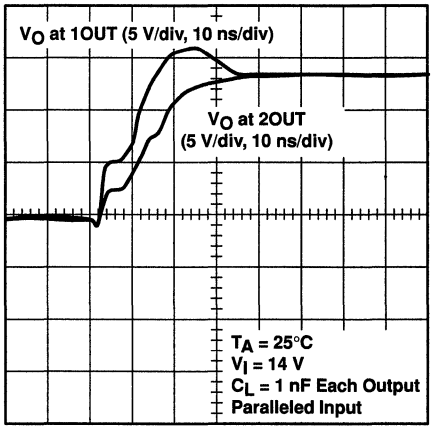


Figure 23. Voltage at 1OUT vs Voltage at 2OUT, Low-to-High Output Delay

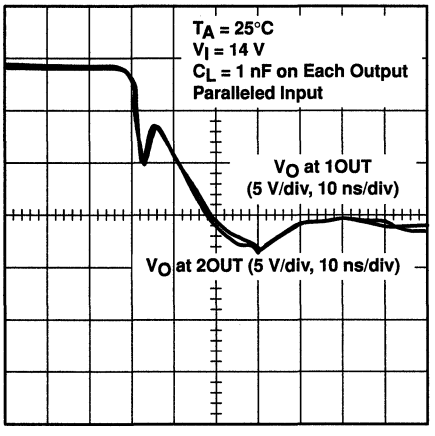


Figure 24. Voltage at 1OUT vs Voltage at 2OUT, High-to-Low Output Delay

APPLICATION INFORMATION

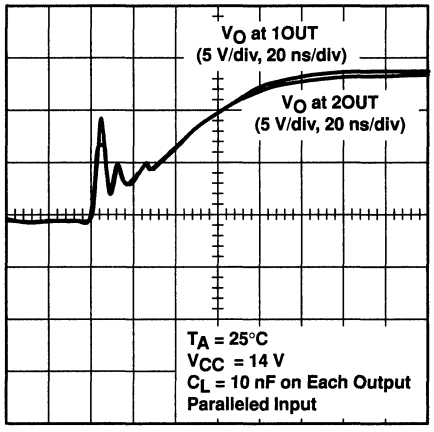


Figure 25. Voltage at 1OUT vs Voltage at 2OUT, Low-to-High Output Delay

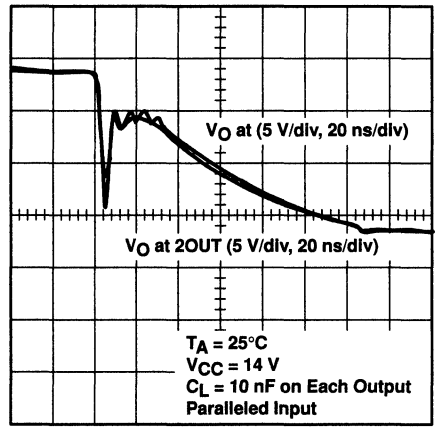
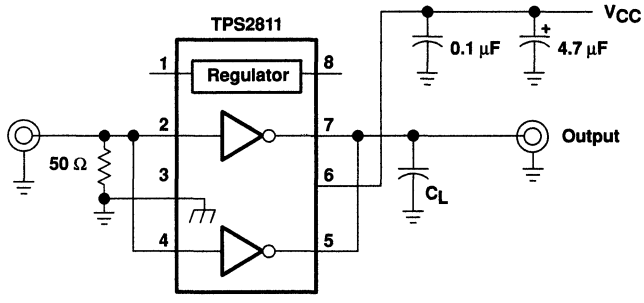


Figure 26. Voltage at 1OUT vs Voltage at 2OUT, High-to-Low Output Delay



NOTE A: Input rise and fall times should be ≤10 ns for accurate measurement of ac parameters.

Figure 27. Test Circuit for Measuring Paralleled Switching Characteristics

APPLICATION INFORMATION

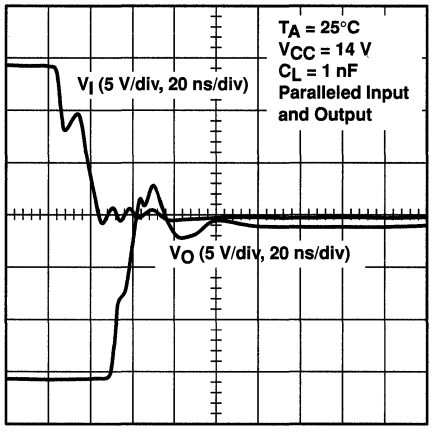


Figure 28. Input Voltage vs Output Voltage, Low-to-High Propagation Delay of Paralleled Drivers

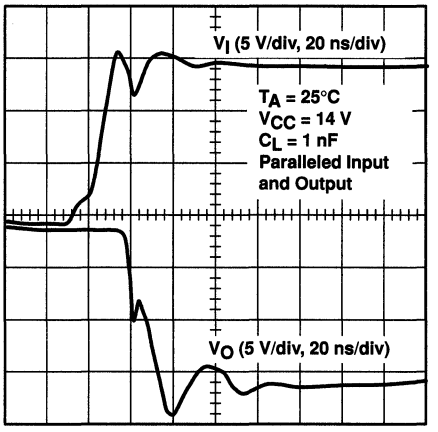


Figure 29. Input Voltage vs Output Voltage, High-to-Low Propagation Delay of Paralleled Drivers

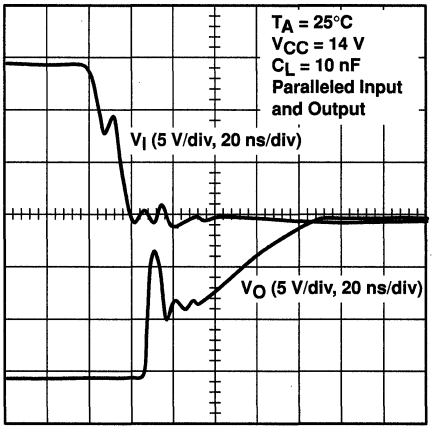


Figure 30. Input Voltage vs Output Voltage, Low-to-High Propagation Delay of Paralleled Drivers

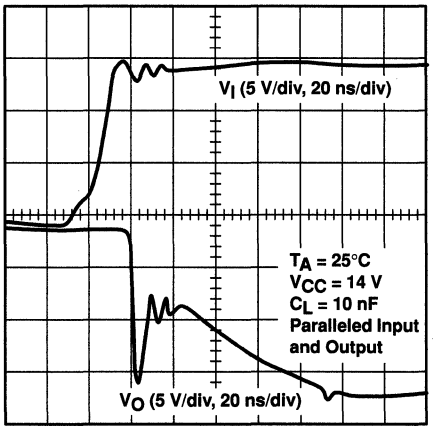


Figure 31. Input Voltage vs Output Voltage, High-to-Low Propagation Delay of Paralleled Drivers

APPLICATION INFORMATION

Figures 33 through 47 illustrate the performance of the TPS2811 driving MOSFETs with clamped inductive loads, similar to what is encountered in discontinuous-mode flyback converters. The MOSFETs that were tested range in size from Hex-1 to Hex-4, although the TPS28xx family is only recommended for Hex-3 or below.

The test circuit is shown in Figure 32. The layout rules observed in building the test circuit also apply to real applications. Decoupling capacitor C1 is a 0.1-µF ceramic device, connected between V_{CC} and GND of the TPS2811, with short lead lengths. The connection between the driver output and the MOSFET gate, and between GND and the MOSFET source, are as short as possible to minimize inductance. Ideally, GND of the driver is connected directly to the MOSFET source. The tests were conducted with the pulse generator frequency set very low to eliminate the need for heat sinking, and the duty cycle was set to turn off the MOSFET when the drain current reached 50% of its rated value. The input voltage was adjusted to clamp the drain voltage at 80% of its rating.

As shown, the driver is capable of driving each of the Hex-1 through Hex-3 MOSFETs to switch in 20 ns or less. Even the Hex-4 is turned on in less than 20 ns. Figures 45, 46 and 47 show that paralleling the two drivers in a package enhances the gate waveforms and improves the switching speed of the MOSFET. Generally, one driver is capable of driving up to a Hex-4 size. The TPS2811 family is even capable of driving large MOSFETs that have a low gate charge.

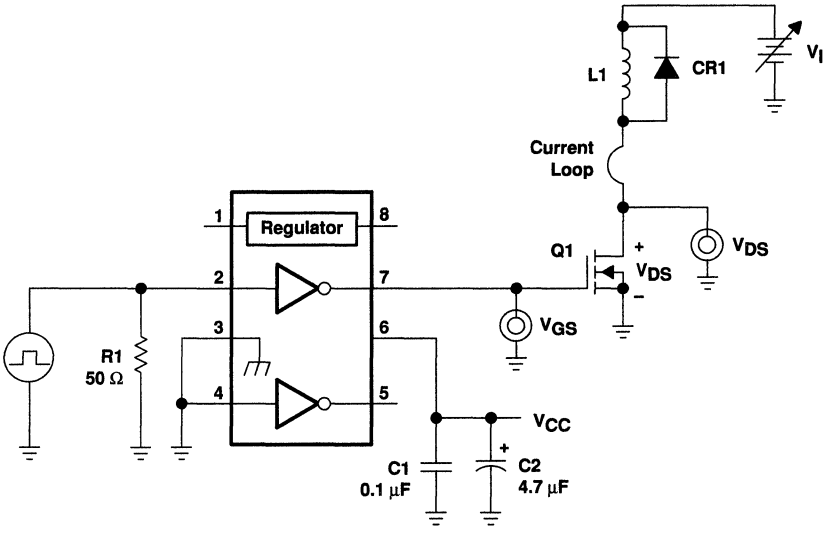


Figure 32. TPS2811 Driving Hex-1 through Hex-4 Devices

APPLICATION INFORMATION

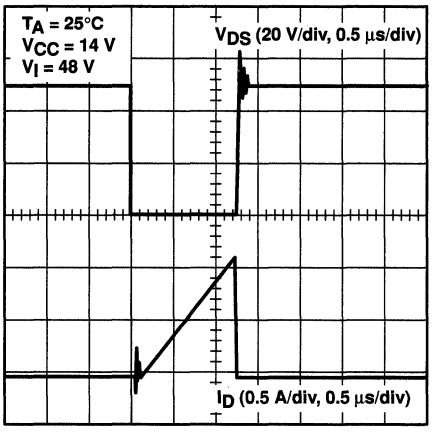


Figure 33. Drain-Source Voltage vs Drain Current, TPS2811 Driving an IRFD014 (Hex-1 Size)

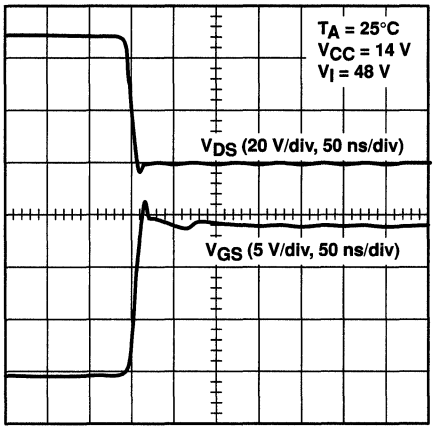


Figure 34. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, TPS2811 Driving an IRFD014 (Hex-1 Size)

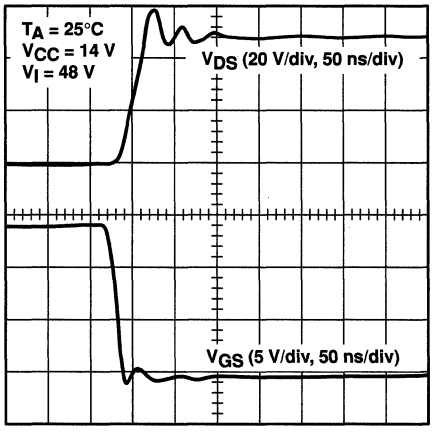


Figure 35. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, TPS2811 Driving an IRFD014 (Hex-1 Size)

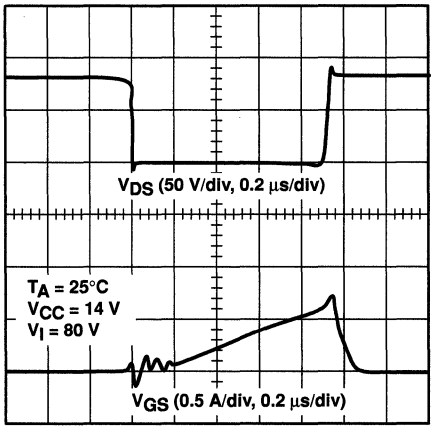


Figure 36. Drain-Source Voltage vs Drain Current, TPS2811 Driving an IRFD120 (Hex-2 Size)

APPLICATION INFORMATION

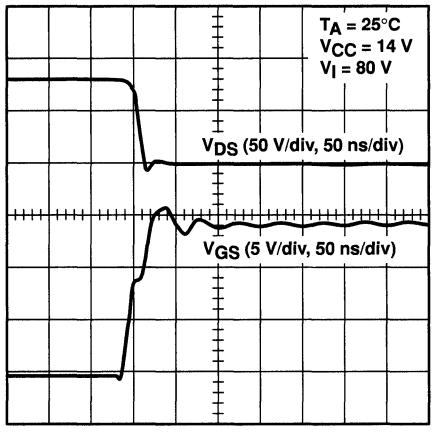


Figure 37. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, TPS2811 Driving an IRFD120 (Hex-2 Size)

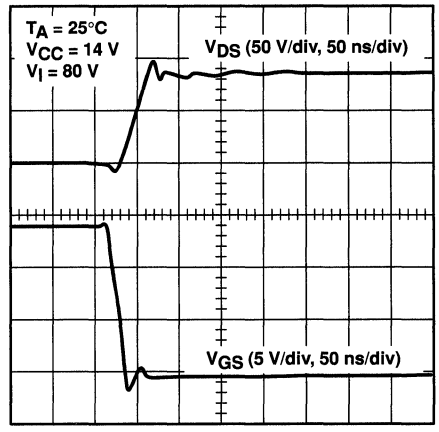


Figure 38. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, TPS2811 Driving an IRFD120 (Hex-2 Size)

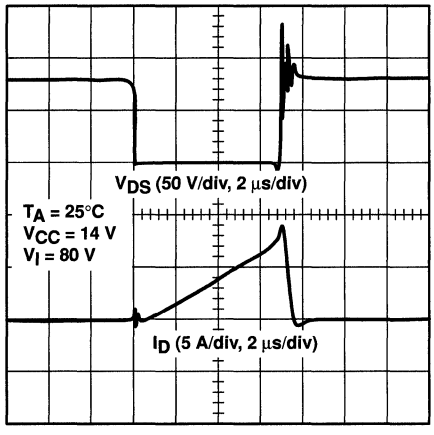


Figure 39. Drain-Source Voltage vs Drain Current, TPS2811 Driving an IRF530 (Hex-3 Size)

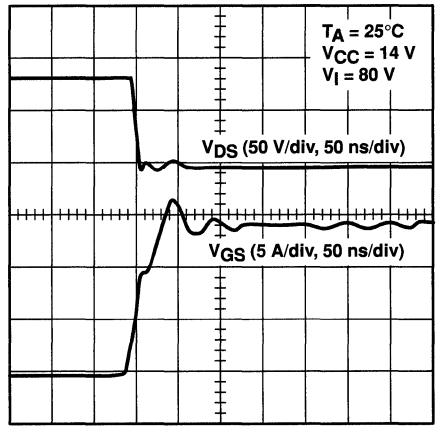


Figure 40. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, TPS2811 Driving an IRF530 (Hex-3 Size)

APPLICATION INFORMATION

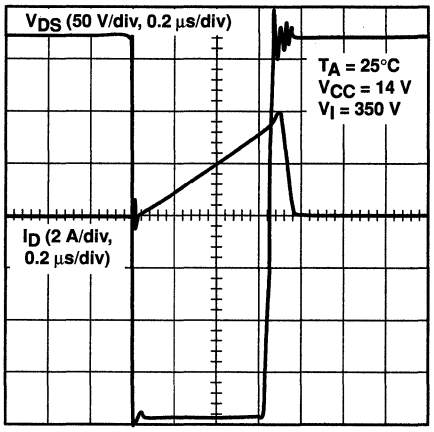


Figure 41. Drain-Source Voltage vs Drain Current, One Driver, TPS2811 Driving an IRF840 (Hex-4 Size)

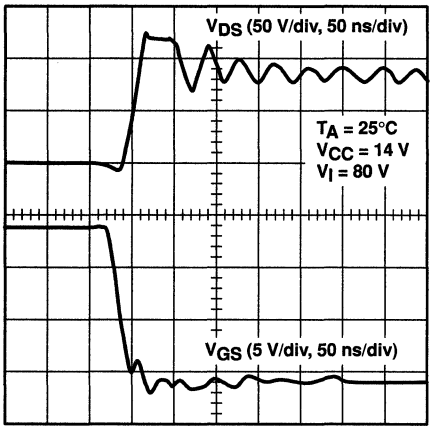


Figure 42. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, TPS2811 Driving an IRF530 (Hex-3 Size)

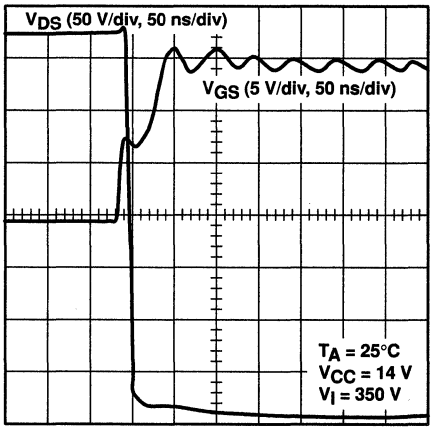


Figure 43. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, One Driver, TPS2811 Driving an IRF840 (Hex-4 Size)

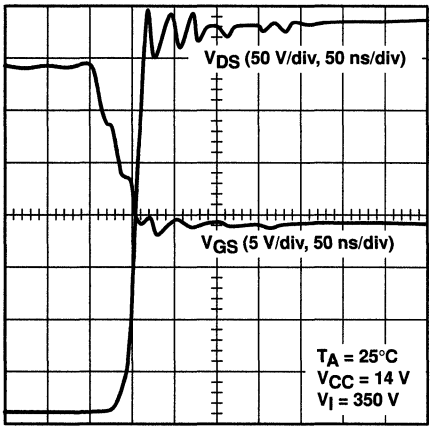


Figure 44. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, One Driver, TPS2811 Driving an IRF840 (Hex-4 Size)

APPLICATION INFORMATION

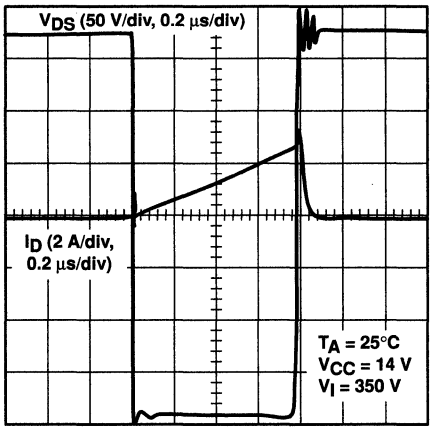


Figure 45. Drain-Source Voltage vs Drain Current, Parallel Drivers, TPS2811 Driving an IRF840 (Hex-4 Size)

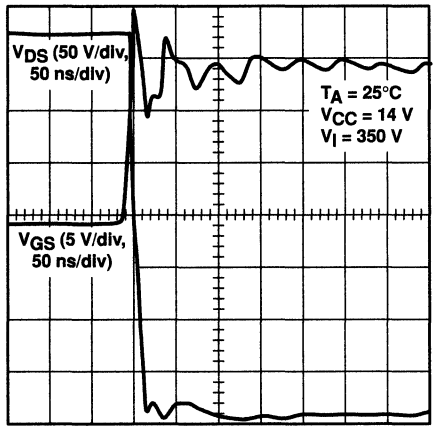


Figure 46. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, Parallel Drivers, TPS2811 Driving an IRF840 (Hex-4 Size)

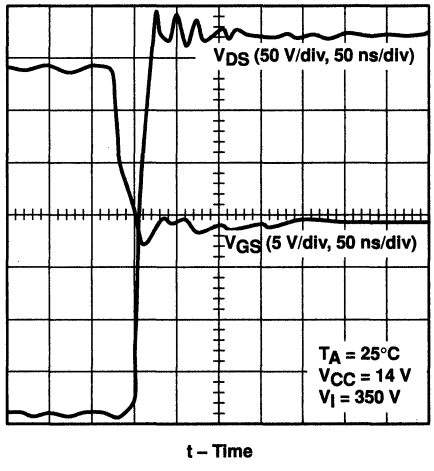


Figure 47. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, Parallel Drivers, TPS2811 Driving an IRF840 (Hex-4 Size)

APPLICATION INFORMATION

synchronous buck regulator

Figure 48 is the schematic for a 100-kHz synchronous-rectified buck converter implemented with a TL5001 pulse-width-modulation (PWM) controller and a TPS2812 driver. The bill of materials is provided in Table 1. The converter operates over an input range from 5.5 V to 12 V and has a 3.3-V output capable of supplying 3 A continuously and 5 A during load surges. The converter achieves an efficiency of 90.6% at 3 A and 87.6% at 5 A. Figures 49 and 50 show the power switch switching performance. The output ripple voltage waveforms are documented in Figures 54 and 55.

The TPS2812 drives both the power switch, Q2, and the synchronous rectifier, Q1. Large shoot-through currents, caused by power switch and synchronous rectifier remaining on simultaneously during the transitions, are prevented by small delays built into the drive signals, using CR2, CR3, R11, R12, and the input capacitance of the TPS2812. These delays allow the power switch to turn off before the synchronous rectifier turns on and vice versa. Figure 51 shows the delay between the drain of Q2 and the gate of Q1; expanded views are provided in Figures 52 and 53.

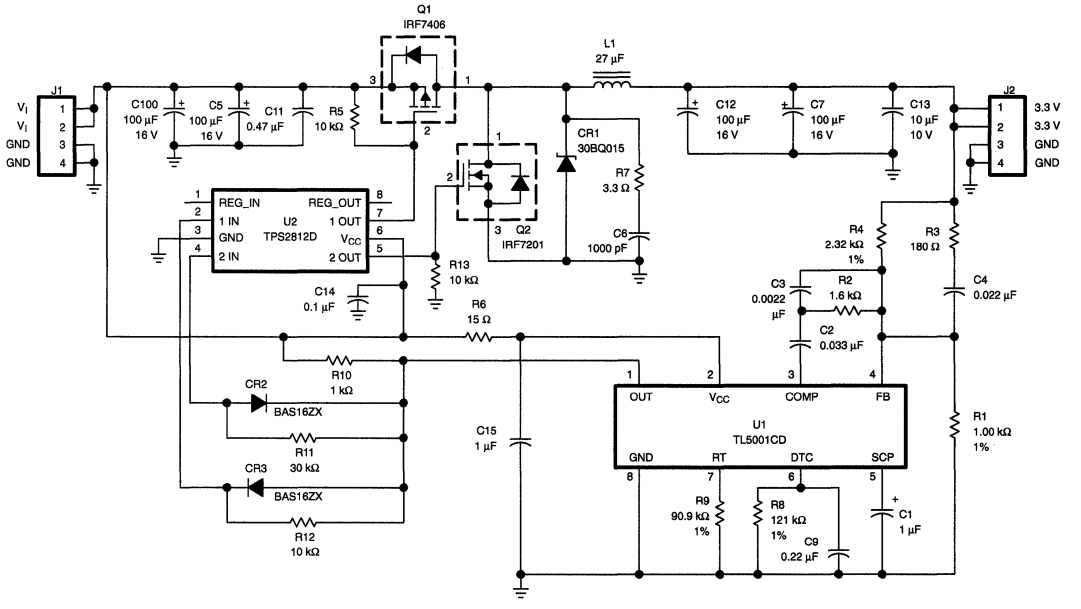


Figure 48. 3.3-V 3-A Synchronous-Rectified Buck Regulator Circuit

APPLICATION INFORMATION

**Table 1. Bill of Materials,
3.3-V, 3-A Synchronous-Rectified Buck Converter**

REFERENCE	DESCRIPTION	VENDOR	
U1	TL5001CD, PWM	Texas Instruments,	972-644-5580
U2	TPS2812D, N.I. MOSFET Driver	Texas Instruments,	972-644-5580
CR1	3 A, 15 V, Schottky, 30BQ015	International Rectifier,	310-322-3331
CR2,CR3	Signal Diode, BAS16ZX	Zetex,	516-543-7100
C1	1 μF, 16 V, Tantalum		
C2	0.033 μF, 50 V		
C3	0.0022 μF, 50 V		
C4	0.022 μF, 50 V		
C5,C7,C10,C12	100 μF, 16 V, Tantalum, TPSE107M016R0100	AVX,	800-448-9411
C6	1000 pF, 50 V		
C9	0.22 μF, 50 V		
C11	0.47 μF, 50 V, Z5U		
C13	10 μF, 10 V, Ceramic, CC1210CY5V106Z	TDK,	708-803-6100
C14	0.1 μF, 50 V		
C15	1.0 μF, 50 V		
J1,J2	4-Pin Header		
L1	27 μH, 3 A/5 A, SML5040	Nova Magnetics, Inc.,	972-272-8287
Q1	IRF7406, P-FET	International Rectifier,	310-322-3331
Q2	IRF7201, N-FET	International Rectifier,	310-322-3331
R1	1.00 kΩ, 1%		
R2	1.6 kΩ		
R3	180 Ω		
R4	2.32 kΩ, 1 %		
R5,R12,R13	10 kΩ		
R6	15 Ω		
R7	3.3 Ω		
R8	121 kΩ, 1%		
R9	90.9 kΩ, 1%		
R10	1 kΩ		
R11	30 kΩ		

NOTES: 2. Unless otherwise specified, capacitors are X7R ceramics.
3. Unless otherwise specified, resistors are 5%, 1/10 W.

APPLICATION INFORMATION

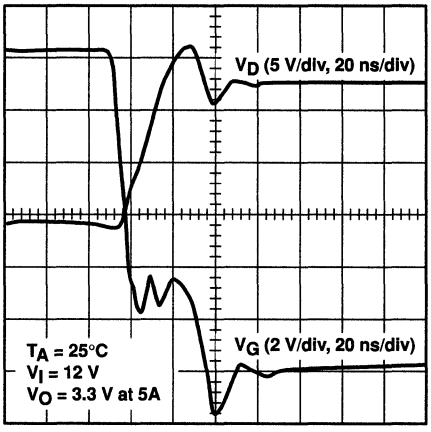


Figure 49. Q1 Drain Voltage vs Gate Voltage, at Switch Turn-on

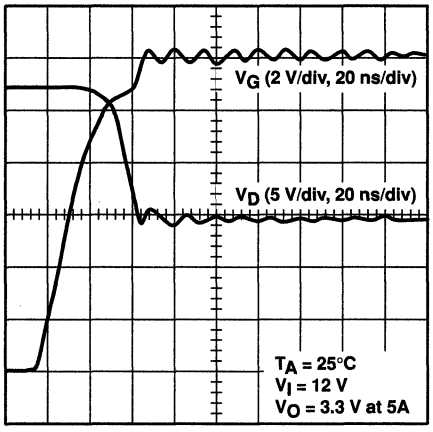


Figure 50. Q1 Drain Voltage vs Gate Voltage, at Switch Turn-off

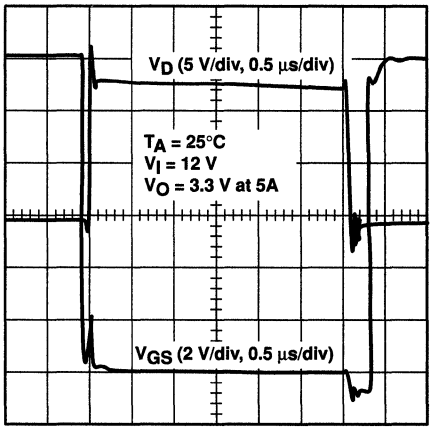


Figure 51. Q1 Drain Voltage vs Q2 Gate-Source Voltage

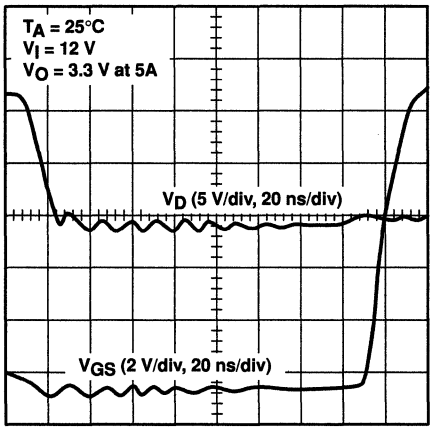


Figure 52. Q1 Drain Voltage vs Q2 Gate-Source Voltage

APPLICATION INFORMATION

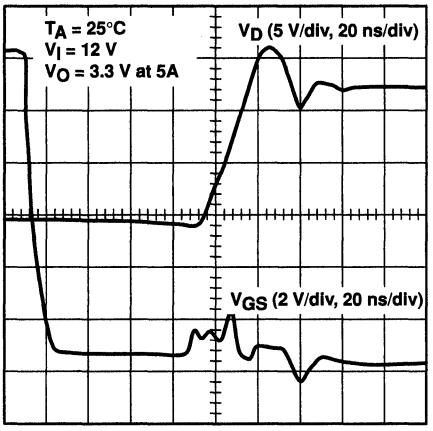


Figure 53. Q1 Drain Voltage vs Q2 Gate-Source Voltage

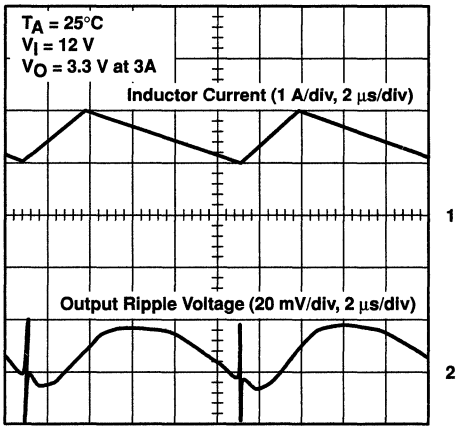


Figure 54. Output Ripple Voltage vs Inductor Current, at 3 A

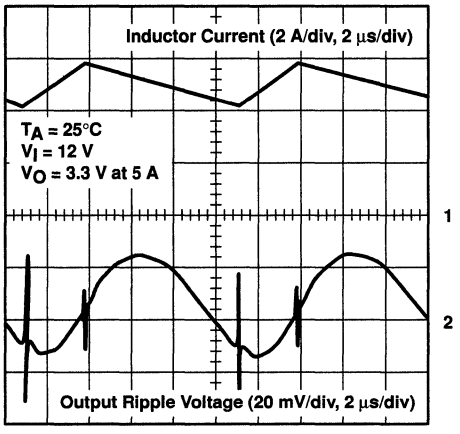
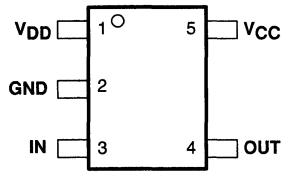


Figure 55. Output Ripple Voltage vs Inductor Current, at 5 A

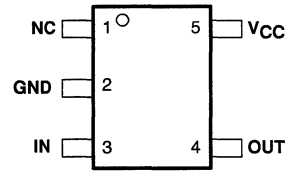
SLVS160A – FEBRUARY 1997 – REVISED NOVEMBER 1997

- **Low-Cost Single-Channel High-Speed MOSFET Driver**
- **I_{CC} . . . 15-μA Max (TPS2828, TPS2829)**
- **25-ns Max Rise/Fall Times and 40-ns Max Propagation Delay . . . 1-nF Load**
- **2-A Peak Output Current**
- **4-V to 14-V Driver Supply Voltage Range; Internal Regulator Extends Range to 40 V (TPS2816, TPS2817, TPS2818, TPS2819)**
- **5-pin SOT-23 Package**
- **–40°C to 125°C Ambient-Temperature Operating Range**
- **Highly Resistant to Latch-ups**

TPS2816, TPS2817
TPS2818, TPS2819
DBV PACKAGE
(TOP VIEW)



TPS2828, TPS2829
DBV PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS28xx single-channel high-speed MOSFET drivers are capable of delivering peak currents of up to 2 A into highly capacitive loads. High switching speeds (t_r and t_f = 14 ns typ) are obtained with the use of BiCMOS outputs. Typical threshold switching voltages are 2/3 and 1/3 of V_{CC}. The design inherently minimizes shoot-through current.

A regulator is provided on TPS2816 through TPS2819 devices to allow operation with supply inputs between 14 V and 40 V. The regulator output can be used to power other circuits, provided power dissipation does not exceed package limitations. If the regulator is not required, V_{DD} (the regulator input) should be connected to V_{CC}. The TPS2816 and TPS2817 input circuits include an active pullup circuit to eliminate the need for an external resistor when using open-collector PWM controllers. The TPS2818 and TPS2819 are identical to the TPS2816 and TPS2817, except that the active pullup circuit is omitted. The TPS2828 and TPS2829 are identical to the TPS2818 and TPS2819, except that the internal voltage regulator is omitted, allowing quiescent current to drop to less than 15 μA when the inputs are high or low.

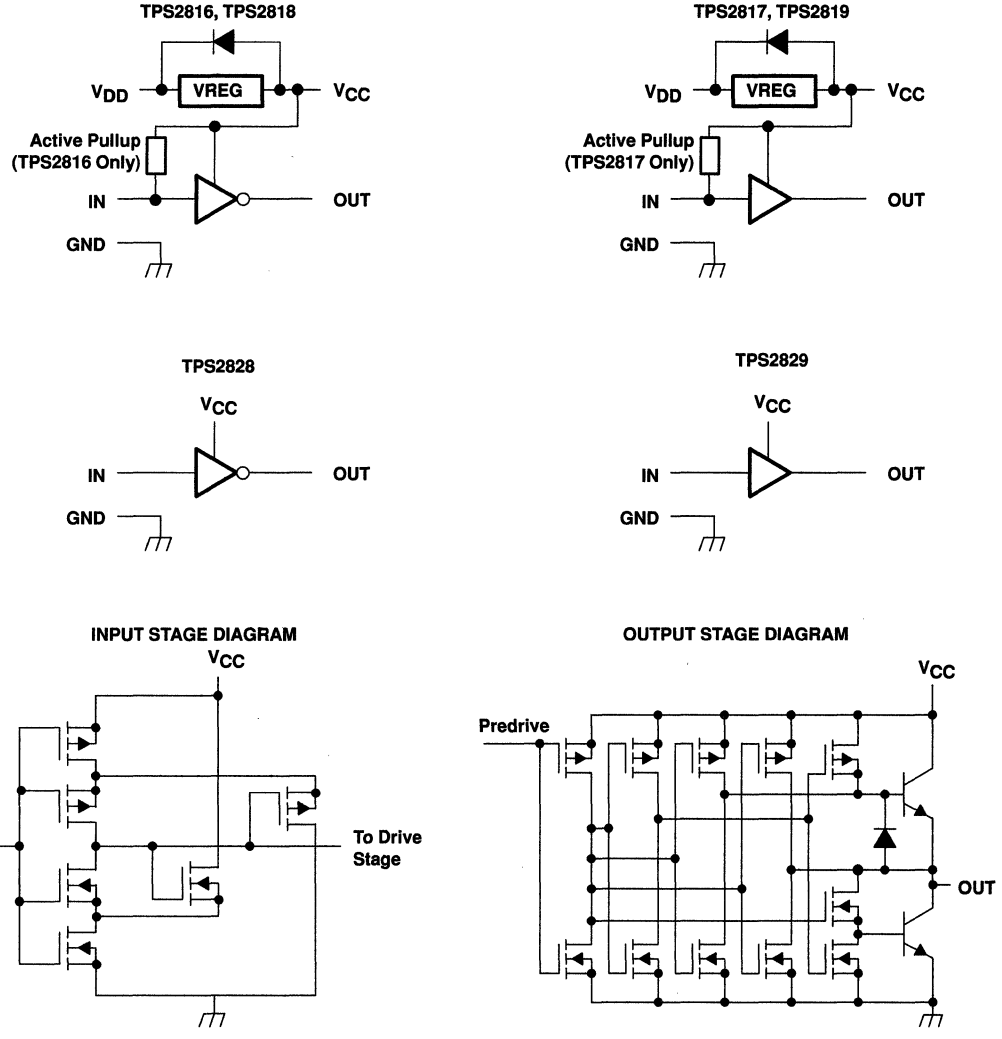
The TPS28xx series devices are available in 5-pin SOT-23 (DBV) packages and operate over an ambient temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_A	FUNCTION	PACKAGED DEVICES	CHIP FORM (Y)
		SOT-23–5 (DBV)	
–40°C to 125°C	Inverting driver with active pullup input	TPS2816DBV	TPS2816Y
	Noninverting driver with active pullup input	TPS2817DBV	TPS2817Y
	Inverting driver	TPS2818DBV	TPS2818Y
	Noninverting driver	TPS2819DBV	TPS2819Y
	Inverting driver, no regulator	TPS2828DBV	TPS2828Y
	Noninverting driver, no regulator	TPS2829DBV	TPS2829Y

The DBV package is available taped and reeled only.

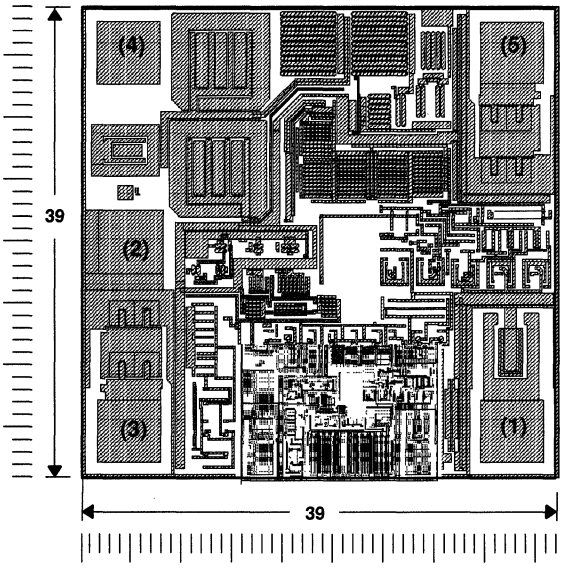
functional block diagram

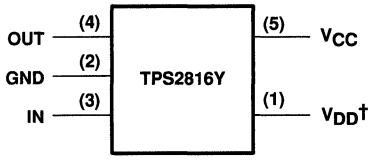


TPS28xxY chip information

This chip, when properly assembled, displays characteristics similar to those of the TPS28xx. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





†TPS2816 through TPS2819 only

CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TPS2816, TPS2818, TPS2828 (inverting driver)

TERMINAL		DESCRIPTION
NAME	NO.	
V_{DD}	1	Regulator supply voltage input. (Not connected on TPS2828)
GND	2	Ground
IN	3	Driver input.
OUT	4	Driver output, OUT = $\overline{IN}$
V_{CC}	5	Driver supply voltage/regulator output voltage

TPS2817, TPS2819, TPS2829 (noninverting driver)

TERMINAL		DESCRIPTION
NAME	NO.	
V_{DD}	1	Regulator supply voltage input. (Not connected on TPS2829)
GND	2	Ground
IN	3	Driver input.
OUT	4	Driver output, OUT= IN
V_{CC}	5	Driver supply voltage/regulator output voltage

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 80°C$ POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

These dissipation ratings are based upon EIA specification JESD51-3, "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages," in tests conducted in a zero-airflow, wind tunnel environment.

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Regulator supply voltage range, V_{DD} ..... –0.3 V to 42 V
Supply voltage range, V_{CC} ..... –0.3 V to 15 V
Input voltage range, IN ..... –0.3 V to 15 V
Continuous regulator output current, V_{CC} ..... 25 mA
Continuous output current, OUT ..... ±100 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating ambient temperature range, T_A ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to device GND terminal.

recommended operating conditions

	MIN	MAX	UNIT
Regulator input voltage range, V_{DD}, TPS2816 through TPS2819	8	40	V
Supply voltage, V_{CC}	4	14	V
Input voltage, IN	–0.3	V_{CC}	V
Continuous regulator output current, I_{CC}	0	20	mA
Operating ambient temperature range, T_A	–40	125	°C

TPS28xx electrical characteristics over recommended operating ambient temperature range, V_{CC} = 10 V, V_{DD} tied to V_{CC}, C_L = 1 nF (unless otherwise specified)

Inputs

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Positive-going input threshold voltage	V_{CC} = 5 V		3.3	4	V
	V_{CC} = 10 V		6.6	7	
	V_{CC} = 14 V		9.3	10	
Negative-going input threshold voltage	V_{CC} = 5 V	1	1.7		V
	V_{CC} = 10 V	2	3.3		
	V_{CC} = 14 V	2.5	4.6		
Input voltage hysteresis			1.3		V
Input current, TPS2818/19/28/29	Input = 0 V or V_{CC}		0.2		µA
Input current, TPS2816/17	Input = 0 V		650		µA
	Input = V_{CC}		15		
Input capacitance			5	10	pF

† Typicals are for T_A = 25°C unless otherwise noted.

outputs

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
High-level output voltage	I_O = –1 mA	9.75	9.9		V
	I_O = –100 mA	8	9.1		
Low-level output voltage	I_O = 1 mA		0.18	0.25	V
	I_O = 100 mA		1	2	

† Typicals are for T_A = 25°C unless otherwise noted.

regulator, TPS2816 through TPS2819

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage	14 ≤ V_{DD} ≤ 40 V, 0 ≤ I_O ≤ 20 mA	10	11.5	13	V
Output voltage in dropout	I_O = 10 mA, V_{DD} = 10 V	8		10	V

† Typicals are for T_A = 25°C unless otherwise noted.

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply current into V_{CC}	TPS2816, TPS2817	IN = high = 10 V		150	250	µA
		IN = low = 0 V		650	1000	
	TPS2818, TPS2819	IN = high or low, High = 10 V, Low = 0 V		25	50	
	TPS2828, TPS2829			0.1	15	
Supply current into V_{DD}	TPS2816, TPS2817	V_{DD} = 20 V, IN = high = 10 V or low = 0 V		650	1000	µA
	TPS2818, TPS2819	V_{DD} = 20 V, IN = high = 10 V or low = 0 V		50	150	

† Typicals are for T_A = 25°C unless otherwise noted.

TPS28xxY electrical characteristics at T_A = 25°C, V_{CC} = 10 V, V_{DD} tied to V_{CC}, C_L = 1 nF (unless otherwise specified)

Inputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-going input threshold voltage	V_{CC} = 5 V		3.3		V
	V_{CC} = 10 V		6.6		
	V_{CC} = 14 V		9.3		
Negative-going input threshold voltage	V_{CC} = 5 V		1.7		V
	V_{CC} = 10 V		3.3		
	V_{CC} = 14 V		4.6		
Input voltage hysteresis			1.3		V
Input current, TPS2818/19/28/29	Input = 0 V or V_{CC}		0.2		µA
Input current, TPS2816/17	Input = 0 V		650		µA
	Input = V_{CC}		15		
Input resistance			1000		MΩ
Input capacitance			5		pF

outputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage	I_O = –1 mA		9.9		V
	I_O = –100 mA		9.1		
Low-level output voltage	I_O = 1 mA		0.18		V
	I_O = 100 mA		1		

regulator, TPS2816 through TPS2819

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	14 ≤ V_{DD} ≤ 40 V, 0 ≤ I_O ≤ 20 mA		11.5		V
Output voltage in dropout	I_O = 10 mA, V_{DD} = 10 V		9		V

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current into V_{CC}	TPS2816, TPS2817	IN = high = 10 V		150		µA
		IN = low = 0 V		650		
	TPS2818, TPS2819	IN = high or low, High = 10 V, Low = 0 V		25		
	TPS2828, TPS2829			0.1		
Supply current into V_{DD}	TPS2816, TPS2817	V_{DD} = 20 V, IN = high = 10 V or low = 0 V		650		µA
	TPS2818, TPS2819	V_{DD} = 20 V, IN = high = 10 V or low = 0 V		50		

switching characteristics for all devices over recommended operating ambient temperature range, V_{CC} = 10 V, V_{DD} tied to V_{CC}, C_L = 1 nF (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_{CC} = 14 V			25	ns
		V_{CC} = 10 V		14	30	
		V_{CC} = 5 V			35	
t_f	Fall time	V_{CC} = 14 V			25	ns
		V_{CC} = 10 V		14	30	
		V_{CC} = 5 V			35	
t_{PHL}	Propagation delay time, high-to-low-level output	V_{CC} = 14 V			40	ns
		V_{CC} = 10 V		24	45	
		V_{CC} = 5 V			50	
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC} = 14 V			40	ns
		V_{CC} = 10 V		24	45	
		V_{CC} = 5 V			50	

PARAMETER MEASUREMENT INFORMATION

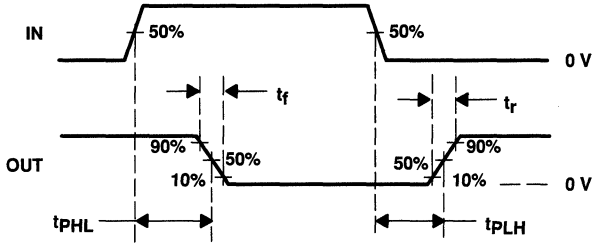


Figure 1. Typical Timing Diagram (TPS2816)

PARAMETER MEASUREMENT INFORMATION

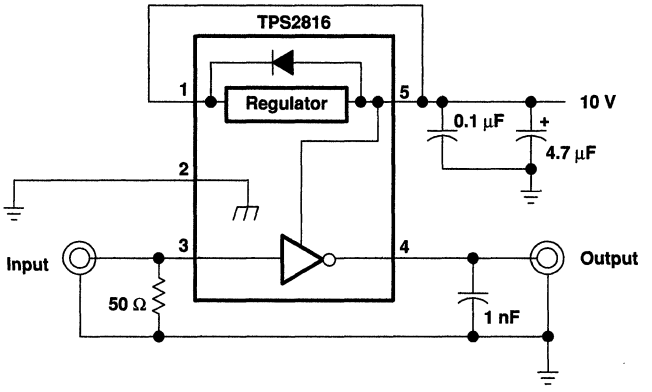


Figure 2. Switching Time Test Setup

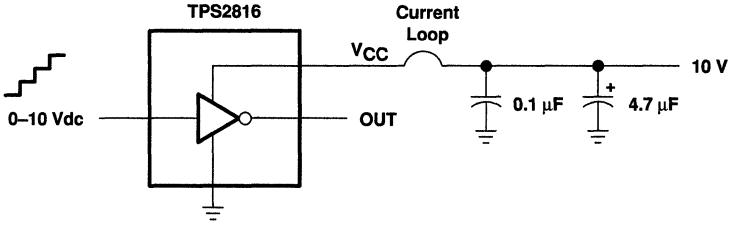


Figure 3. Shoot-Through Current Test Setup

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Rise time	vs Supply voltage	4
Fall time	vs Supply voltage	5
Propagation time (L>H)	vs Supply voltage	6
Propagation Time (H>L)	vs Supply voltage	7
Rise time	vs Ambient temperature	8
Fall time	vs Ambient temperature	9
Propagation time (L>H)	vs Supply voltage	10
Propagation time (H>L)	vs Ambient temperature	11
Supply current (V_{CC})	vs Supply voltage	12
Supply current (V_{CC})	vs Load capacitance	13
Supply current (V_{CC})	vs Ambient temperature	14
Input threshold voltage	vs Supply voltage	15
Regulator output voltage	vs Regulator supply voltage	16
Regulator quiescent current	vs Regulator supply voltage	17
Shoot-through current	vs Input voltage (L>H)	18
Shoot-through current	vs Input voltage (H>L)	19

TYPICAL CHARACTERISTICS

RISE TIME
vs
SUPPLY VOLTAGE

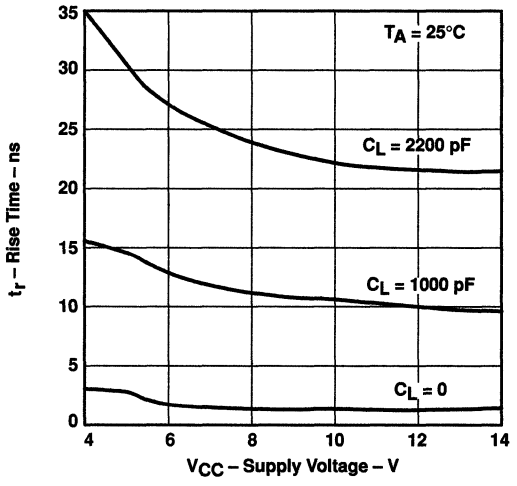


Figure 4

FALL TIME
vs
SUPPLY VOLTAGE

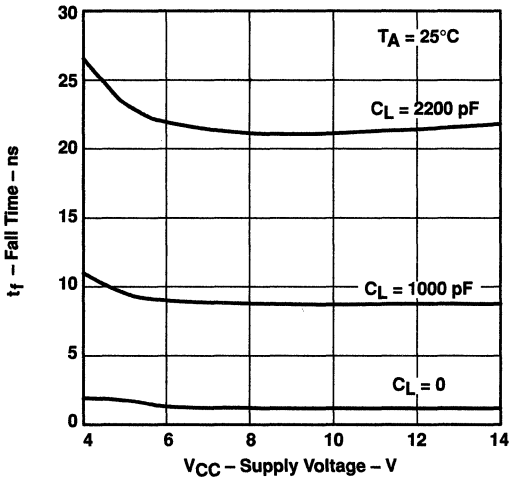


Figure 5

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

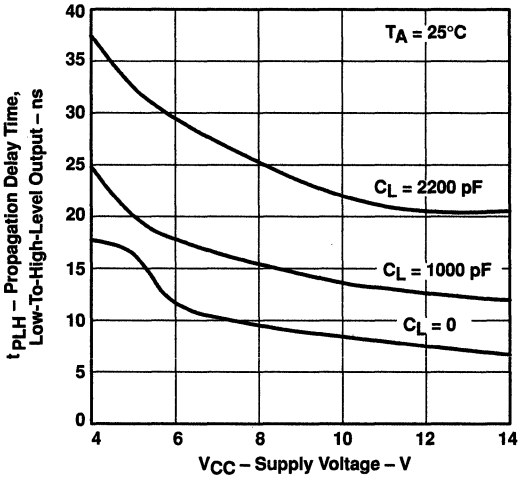


Figure 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

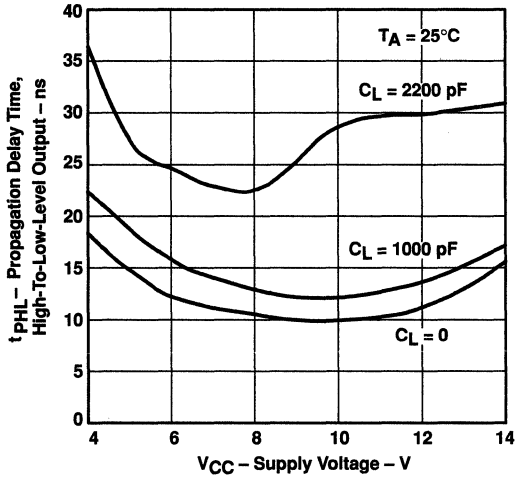


Figure 7

TYPICAL CHARACTERISTICS

RISE TIME
vs
AMBIENT TEMPERATURE

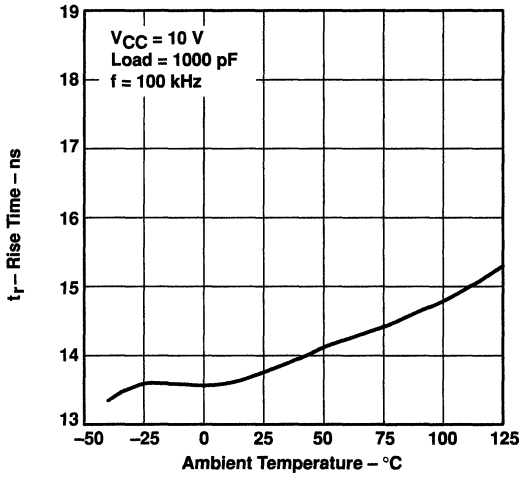


Figure 8

FALL TIME
vs
AMBIENT TEMPERATURE

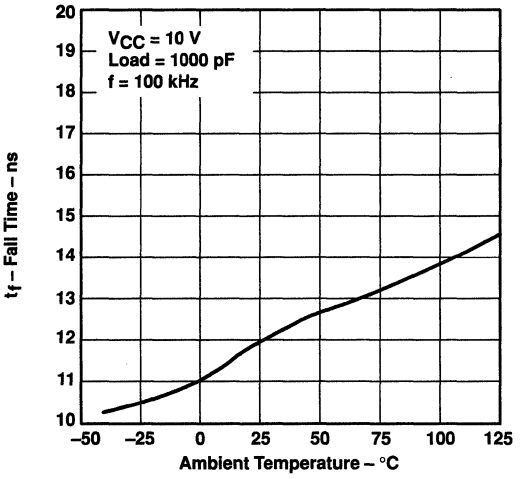


Figure 9

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

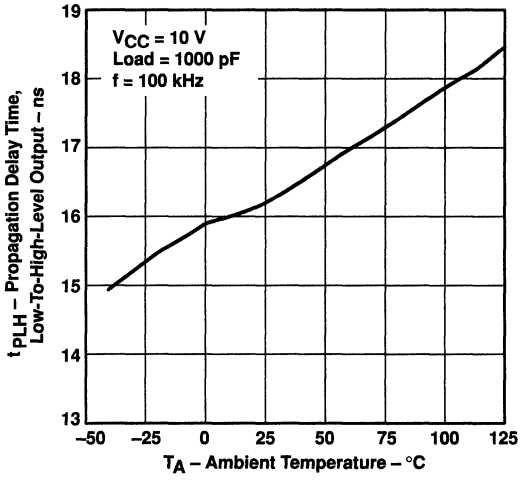


Figure 10

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
AMBIENT TEMPERATURE

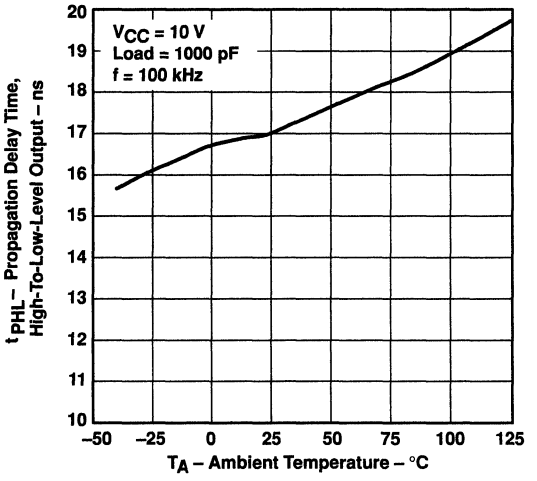


Figure 11

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

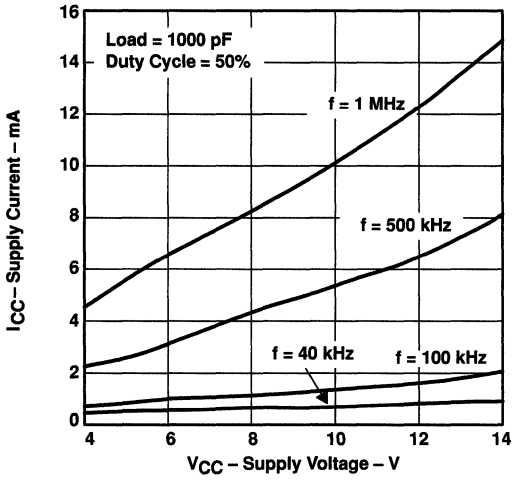


Figure 12

SUPPLY CURRENT
vs
LOAD CAPACITANCE

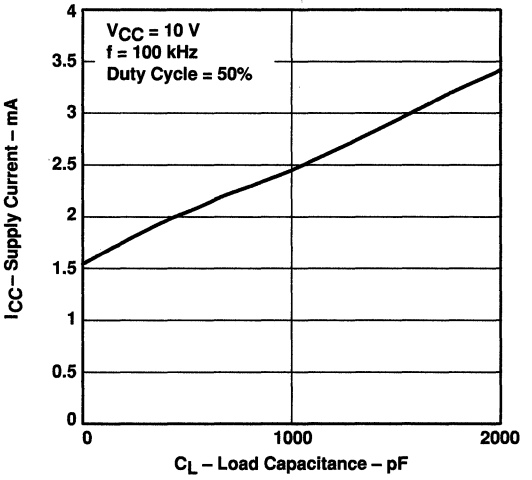


Figure 13

SUPPLY CURRENT
vs
AMBIENT TEMPERATURE

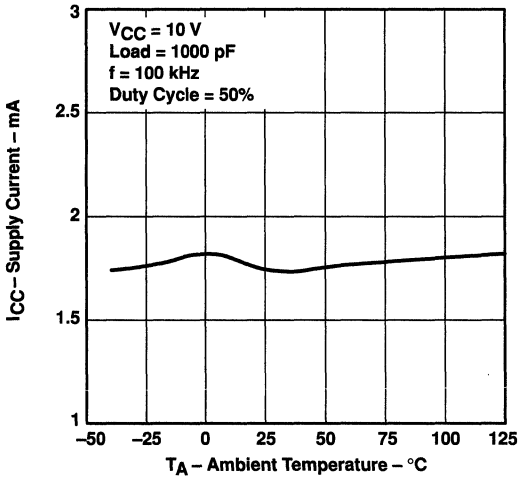


Figure 14

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

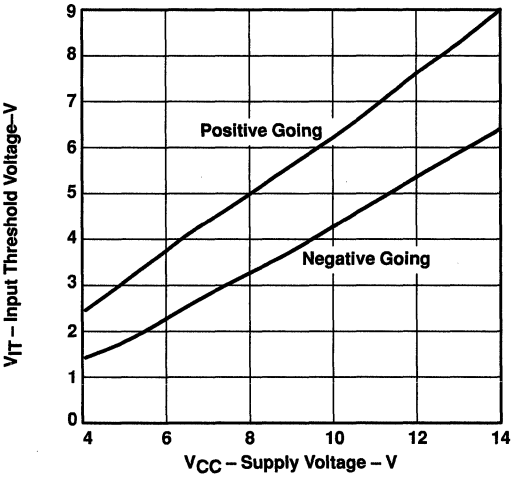


Figure 15

TYPICAL CHARACTERISTICS

REGULATOR OUTPUT VOLTAGE
vs
REGULATOR SUPPLY VOLTAGE

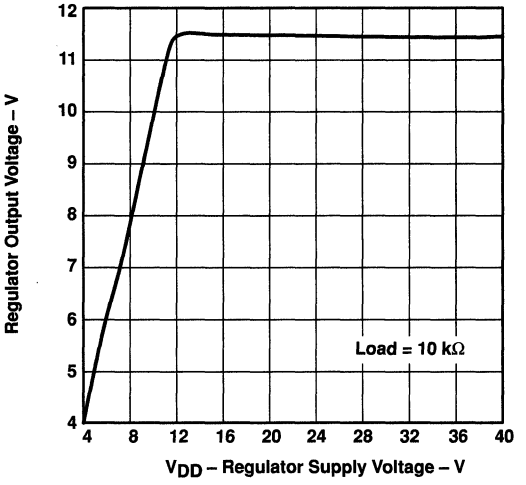


Figure 16

REGULATOR QUIESCENT CURRENT
vs
REGULATOR SUPPLY VOLTAGE

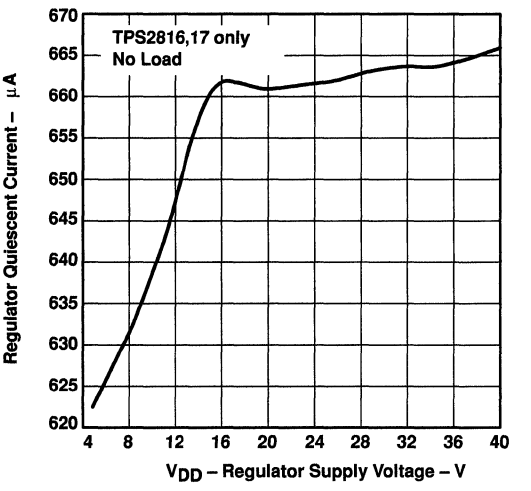


Figure 17

SHOOT-THROUGH CURRENT
vs
INPUT VOLTAGE LOW-TO-HIGH

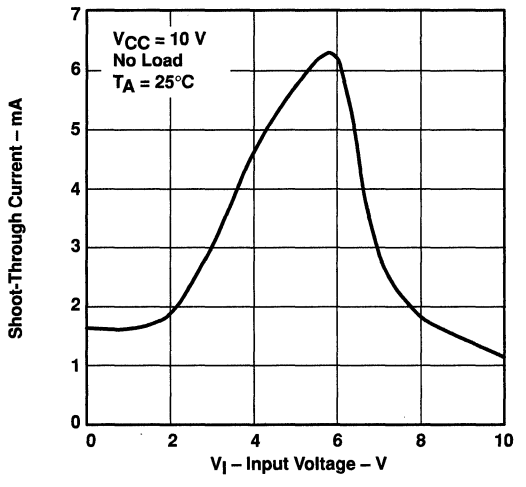


Figure 18

SHOOT-THROUGH CURRENT
vs
INPUT VOLTAGE HIGH-TO-LOW

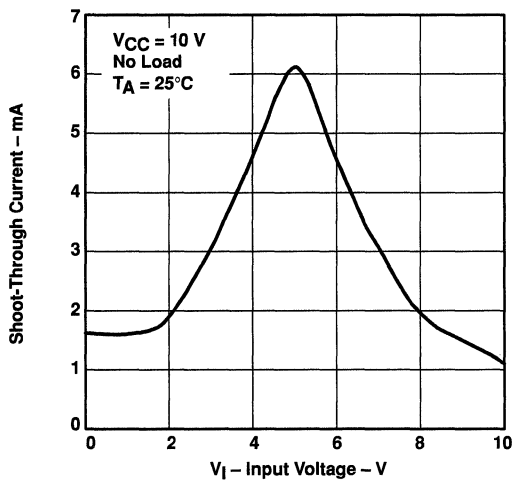


Figure 19

APPLICATION INFORMATION

MOSFETs are voltage-driven devices that require very little steady-state drive current. However, the large input capacitance (200 pF to 3000 pF or greater) of these devices requires large current surges to reduce the turn-on and turn-off times. The TPS2816 series of high-speed drivers can supply up to 2 A to a MOSFET, greatly reducing the switching times. The fast rise times and fall times and short propagation delays allow for operation in today's high-frequency switching converters.

In addition, MOSFETs have a limited gate-bias voltage range, usually less than 20 V. The TPS2816 series of drivers extends this operating range by incorporating an on-board series regulator with an input range up to 40 V. This regulator can be used to power the drivers, the PWM chip, and other circuitry, providing the power dissipation rating is not exceeded.

When using these devices, care should be exercised in the proper placement of the driver, the switching MOSFET, and the bypass capacitor. Because of the large input capacitance of the MOSFET, the driver should be placed close to the gate to eliminate the possibility of oscillations caused by trace inductance ringing with the gate capacitance of the MOSFET. When the driver output path is longer than approximately 2 inches, a resistor in the range of 10 Ω should be placed in series with the gate drive as close as possible to the MOSFET. A ceramic bypass capacitor is also recommended to provide a source for the high-speed current transients that the MOSFET requires. This capacitor should be placed between V_{CC} and GND of the driver (see Figures 20 and 21).

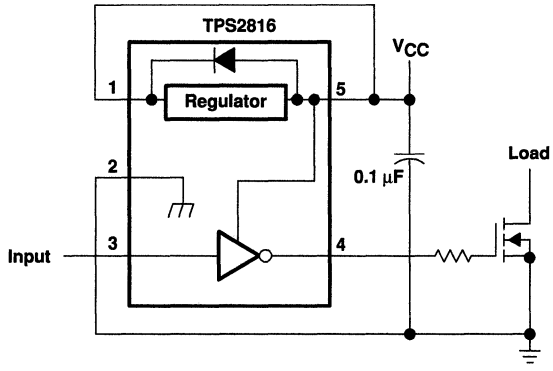


Figure 20. V_{CC} < 14 V

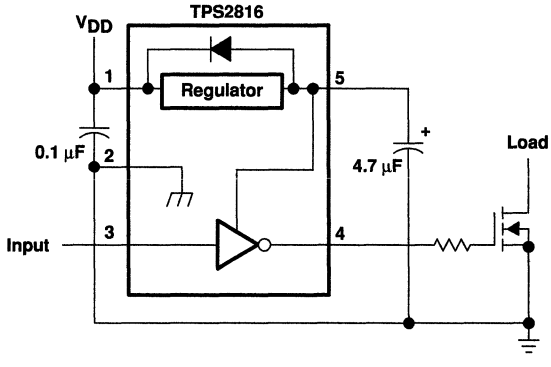


Figure 21. V_{CC} > 14 V

APPLICATION INFORMATION

The on-board series regulator supplies approximately 20 mA of current at 11.5 V, some of which can be used for external circuitry, providing the power dissipation rating for the driver is not exceeded. When using the on-board series regulator, an electrolytic output capacitor of 4.7 μF or larger is recommended. Although not required, a 0.1-μF ceramic capacitor on the input of the regulator can help suppress transient currents (see Figure 22). When not used, the regulator should be connected to V_{CC}. Grounding V_{DD} will result in destruction of the regulator.

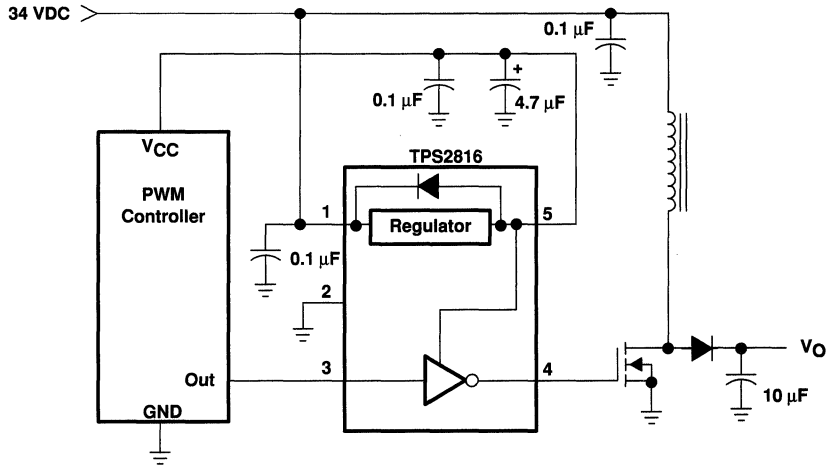


Figure 22. Boost Application

The TPS2816 and TPS2818 drivers include active pullup circuits on the inputs to eliminate the need for external pullup resistors when using controllers with open-collector outputs (such as the TL5001). The TPS2817 and TPS2819 drivers have standard CMOS inputs providing a total device operating current of less than 50 μA. All devices switch at standard CMOS logic levels of approximately 2/3 V_{CC} with positive-going input levels, and approximately 1/3 V_{CC} with negative-going input levels. Being CMOS drivers, these devices will draw relatively large amounts of current (Approximately 5 mA) when the inputs are in the range of one-half of the supply voltage. In normal operation, the driver input is in this range for a very short time. Care should be taken to avoid use of very low slew-rate inputs, used under normal operating conditions. Although not destructive to the device, slew rates slower than 0.1 V/μs are not recommended.

The BiCMOS output stage provides high instantaneous drive current to rapidly toggle the power switch, and very low drop to each rail to ensure proper operation at voltage extremes.

Low-voltage circuits (less than 14 V) that require very low quiescent currents can use the TPS2828 and TPS2829 drivers. These drivers use typically 0.2 μA of quiescent current (with inputs high or low). They do not have the internal regulator or the active pullup circuit, but all other specifications are the same as for the rest of the family

2.5-V/3.3-V, 3-A application

Figure 23 illustrates the use of the TPS2817 with a TL5001 PWM controller and a TPS1110 in a simple step-down converter application. The converter operates at 275 kHz and delivers either 2.5 V or 3.3 V (determined by the value of R6) at 3 A (5 A peak) from a 5-V supply. The bill of materials is provided in Table 1.

APPLICATION INFORMATION

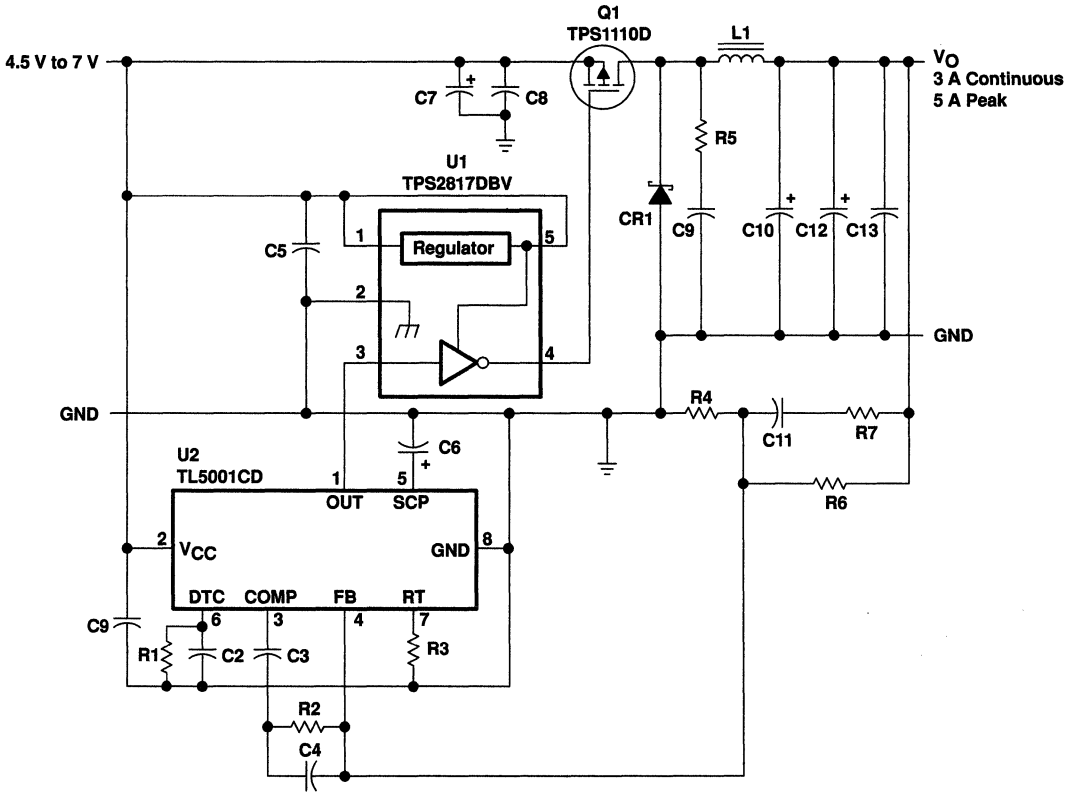


Figure 23. Step-Down Application

APPLICATION INFORMATION

Table 1. Bill of Materials

REF DES	PART NO.	DESCRIPTION	MFR
U1	TPS2817DBV	IC, MOSFET driver, single noninverting	TI
U2	TL5001CD	IC, PWM controller	TI
Q1	TPS1110D	MOSFET, p-channel, 6 A, 7 V, 75 mΩ	TI
C1, C2, C5, C8		Capacitor, ceramic, 0.1 µF, 50 V, X7R, 1206	
C3		Capacitor, ceramic, 0.033 µF, 50 V, X7R, 1206	
C4		Capacitor, ceramic, 2200 pF, 50 V, X7R, 0805	
C6	ECS-T1CY105R	Capacitor, tantalum, 1.0 µF, 16 V, A case	Panasonic
C7	10SC47M	Capacitor, OS-Con, 47 µF, 10 V	Sanyo
C9		Capacitor, ceramic, 1000 pF, 50 V, X7R, 0805	
C10, C12	10SA220M	Capacitor, OS-Con, 220 µF, 10 V	Sanyo
C11		Capacitor, ceramic, 0.022 µF, 50 V, X7R, 0805	
C13		Capacitor, ceramic, 47 µF, 50 V, X7R	
CR1	50WQ03F	Diode, Shottky, D-pak, 5 A 30 V	IR
L1	SML3723	Inductor, 27 µH, +/– 20%, 3 A	Nova Magnetics
R1		Resistor, CF, 47 kΩ, 1/10 W, 5%, 0805	
R2		Resistor, CF, 1.5 kΩ, 1/10 W, 5%, 0805	
R3		Resistor, MF, 30.1 kΩ, 1/10 W, 1%, 0805	
R4		Resistor, MF, 1.00 kΩ, 1/10 W, 1%, 0805	
R5		Resistor, CF, 47 Ω, 1/10 W, 5%, 0805	
R6 (3.3-V)		Resistor, MF, 2.32 kΩ, 1/10 W, 1%, 0805	
R6 (2.5-V)		Resistor, MF, 1.50 kΩ, 1/10 W, 1%, 0805	
R7		Resistor, CF, 100 Ω, 1/10 W, 5%, 0805	

As shown in Figures 24 and 25, the TPS2817 turns on the TPS1110 power switch in less than 20 ns and off in 25 ns.

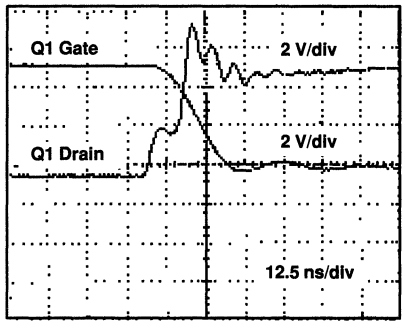


Figure 24. Q1 Turn-On Waveform

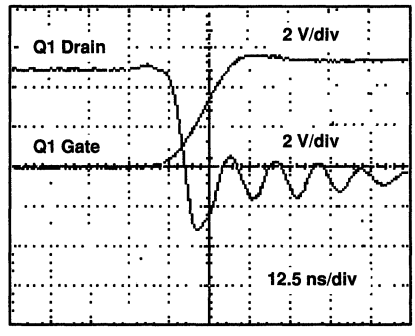


Figure 25. Q1 Turn-Off Waveform

APPLICATION INFORMATION

The efficiency for various output currents, with a 5.25-V input, is shown in Figure 26. For a 3.3-V output, the efficiency is greater than 90% for loads up to 2 A – exceptional for a simple, inexpensive design.

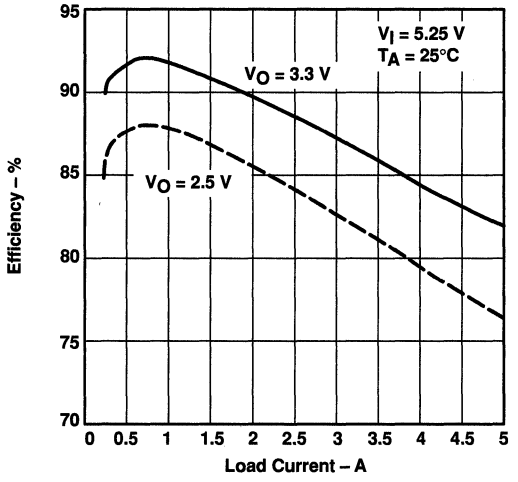
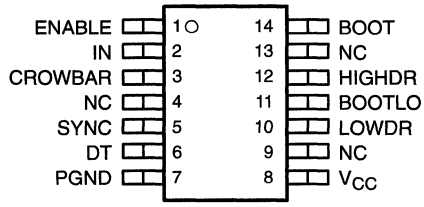


Figure 26. Converter Efficiency

- **Floating Bootstrap or Ground-Reference High-Side Driver**
- **Active Deadtime Control**
- **50-ns Max Rise/Fall Times and 100-ns Max Propagation Delay — 3-nF Load**
- **Ideal for High-Current Single or Mutiphase Applications**
- **2.4-A Typ Peak Output Current**
- **4.5-V to 15-V Supply Voltage Range**
- **Internal Schottky Bootstrap Diode**
- **SYNC Control for Synchronous or Nonsynchronous Operation**
- **CROWBAR for OVP, Protects Against Faulted High-Side Power FETs**
- **Low Supply Current . . . 3-mA Typ**
- **–40°C to 125°C Junction-Temperature Operating Range**

D OR PWP PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS2830 and TPS2831 are MOSFET drivers for synchronous-buck power stages. These devices are ideal for designing a high-performance power supply using a switching controller that does not include suitable MOSFET drivers on the chip. The drivers are designed to deliver 2.4-A peak currents into large capacitive loads. Higher currents can be controlled by using multiple drivers in a multiphase configuration. The high-side driver can be configured as a ground-reference driver or as a floating bootstrap driver. An adaptive dead-time control circuit eliminates shoot-through currents through the main power FETs during switching transitions, and provides high efficiency for the buck regulator. The TPS2830/31 drivers have additional control functions: ENABLE, SYNC, and CROWBAR. Both drivers are off when ENABLE is low. The driver is configured as a nonsynchronous-buck driver when SYNC is low. The CROWBAR function turns on the low-side power FET, overriding the IN signal, for over-voltage protection against faulted high-side power FETs.

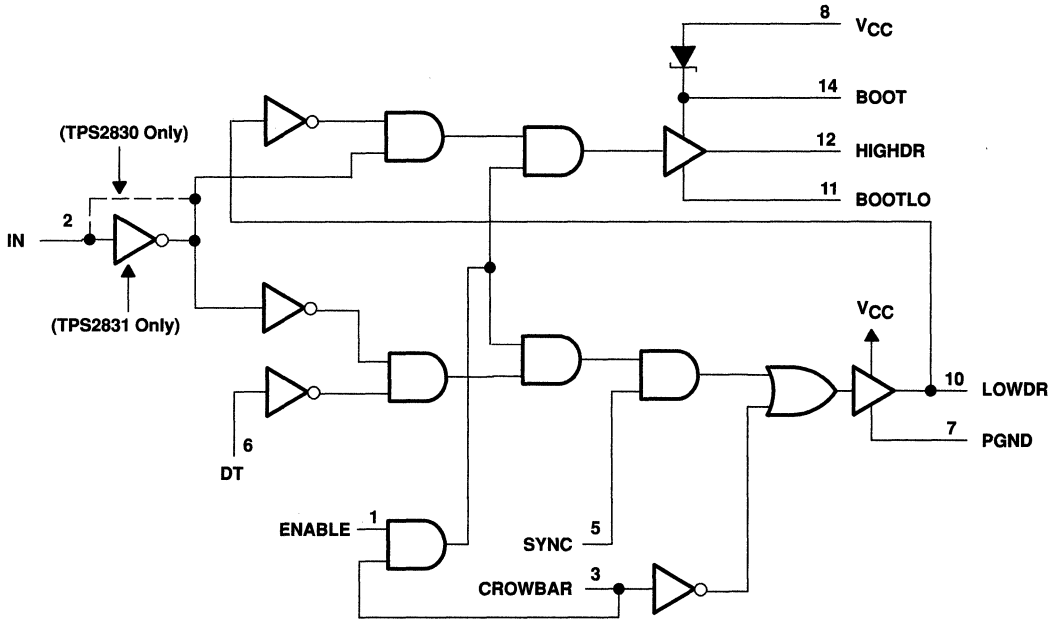
The TPS2830 has a noninverting input. The TPS2831 has an inverting input. The TPS2830/31 drivers are available in 14-terminal SOIC and TSSOP packages and operate over a junction temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES	
	SOIC (D)	TSSOP (PWP)
–40°C to 125°C	TPS2830D TPS2831D	TPS2830PWP TPS2831PWP

The D and PWP packages are available taped and reeled. Add R suffix to device type (e.g., TPS2830DR)

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOT	14	I	Bootstrap terminal. A ceramic capacitor is connected between BOOT and BOOTLO terminals to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 µF and 1 µF. A 1-MΩ resistor should be connected across the bootstrap capacitor to provide a discharge path when the driver has been powered down.
BOOTLO	11	O	This terminal connects to the junction of the high-side and low-side MOSFETs.
CROWBAR	3	I	CROWBAR can to be driven by an external OVP circuit to protect against a short across the high-side MOSFET. If CROWBAR is driven low, the low-side driver will be turned on and the high-side driver will be turned off, independent of the status of all other control terminals.
DT	6	I	Deadtime control terminal. Connect DT to the junction of the high-side and low-side MOSFETs.
ENABLE	1	I	If ENABLE is low, both drivers are off.
HIGHDR	12	O	Output drive for the high-side power MOSFET
IN	2	I	Input signal to the MOSFET drivers (noninverting input for the TPS2830; inverting input for the TPS2831).
LOWDR	10	O	Output drive for the low-side power MOSFET
NC	4, 9, 13		
PGND	7		Power ground. Connect to the FET power ground
SYNC	5	I	Synchronous Rectifier Enable terminal. If SYNC is low, the low-side driver is always off; If SYNC is high, the low-side driver provides gate drive to the low-side MOSFET.
V_{CC}	8	I	Input supply. Recommended that a 1-µF capacitor be connected from V_{CC} to PGND.

detailed description

low-side driver

The low-side driver is designed to drive low Rds(on) N-channel MOSFETs. The current rating of the driver is 2 A, source and sink.

high-side driver

The high-side driver is designed to drive low Rds(on) N-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured as a GND-reference driver or as a floating bootstrap driver. The internal bootstrap diode is a Schottky, for improved drive efficiency. The maximum voltage that can be applied from BOOT to ground is 30 V.

deadtime (DT) control†

Deadtime control prevents shoot through current from flowing through the main power FETs during switching transitions by controlling the turn-on times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs (Vdrn) is low; the DT terminal connects to the junction of the power FETs.

ENABLE†

The ENABLE terminal enables the drivers. When enable is low, the output drivers are low.

IN†

The IN terminal is the input control signal for the drivers. The TPS2830 has a noninverting input; the TPS2831 has an inverting input.

SYNC†

The SYNC terminal controls whether the drivers operate in synchronous or nonsynchronous mode. In synchronous mode, the low-side FET is operated as a synchronous rectifier. In nonsynchronous mode, the low-side FET is always off.

CROWBAR†

The CROWBAR terminal overrides the normal operation of the driver. When the CROWBAR terminal is low, the low-side FET turns on to act as a clamp, protecting the output voltage of the dc/dc converter against over voltages due to a short across the high-side FET. V_{IN} should be fused to protect the low-side FET.

†High-level input voltages on ENABLE, SYNC, CROWBAR, IN, and DT must be greater than or equal to V_{CC}.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –0.3 V to 16 V
Input voltage range: BOOT to PGND (high-side driver ON) ..... –0.3 V to 30 V
BOOTLO to PGND ..... –0.3 V to 16 V
BOOT to BOOTLO ..... –0.3 V to 16 V
ENABLE, SYNC, and CROWBAR (see Note 2) ..... –0.3 V to 16 V
IN (see Note 2) ..... –0.3 V to 16 V
DT (see Note 2) ..... –0.3 V to 30 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise specified, all voltages are with respect to PGND.
2. High-level input voltages on the ENABLE, SYNC, CROWBAR, IN, and DT terminals must be greater than or equal to V_{CC}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	760 mW	7.6 mW/°C	420 mW	305 mW
PWP	2400 mW	25 mW/°C	1275 mW	900 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		15	V
Input voltage	BOOT to PGND	4.5		28	V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range			4.5		15	V
V_{CC}	Quiescent current	V_{ENABLE} = LOW,	V_{CC} =15 V			100	µA
		V_{ENABLE} = HIGH,	V_{CC} =15 V		0.1		mA
		V_{ENABLE} = HIGH, f_{SWX} = 200 kHz, C_{HIGHDR} = 50 pF, See Note 3	V_{CC} =12 V, BOOTLO grounded, C_{LOWDR} = 50 pF,		3		

NOTE 3: Ensured by design, not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted) (continued)

output drivers

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output-current	High-side sink (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 4 V	0.7	1.1		A
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 5 V	1.1	1.5		
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} = 10.5 V	2	2.4		
	High-side source (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 0.5V	1.2	1.4		A
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 1.5 V	1.3	1.6		
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} = 1.5 V	2.3	2.7		
	Low-side sink (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	V_{CC} = 4.5 V, V_{LOWDR} = 4 V	1.3	1.8		A
			V_{CC} = 6.5 V, V_{LOWDR} = 5 V	2	2.5		
			V_{CC} = 12 V, V_{LOWDR} = 10.5 V	3	3.5		
	Low-side source (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	V_{CC} = 4.5 V, V_{LOWDR} = 0.5V	1.4	1.7		A
			V_{CC} = 6.5 V, V_{LOWDR} = 1.5 V	2	2.4		
			V_{CC} = 12 V, V_{LOWDR} = 1.5 V	2.5	3		
Output resistance	High-side sink (see Note 4)		$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 0.5 V			5	Ω
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 0.5 V			5	
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} = 0.5 V			5	
	High-side source (see Note 4)		$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 4 V			45	Ω
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 6 V			45	
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} =11.5 V			45	
	Low-side sink (see Note 4)		V_{DRV} = 4.5 V, V_{LOWDR} = 0.5 V			9	Ω
			V_{DRV} = 6.5 V V_{LOWDR} = 0.5 V			7.5	
			V_{DRV} = 12 V, V_{LOWDR} = 0.5 V			6	
	Low-side source (see Note 4)		V_{DRV} = 4.5 V, V_{LOWDR} = 4 V			45	Ω
			V_{DRV} = 6.5 V, V_{LOWDR} = 6 V			45	
			V_{DRV} = 12 V, V_{LOWDR} = 11.5 V			45	

NOTES: 3. Ensured by design, not production tested.
4. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the Rds(on) of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

deatime control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOWDR	High-level input voltage	Over the V_{CC} range (see Note 3)	2			V
	Low-level input voltage				1	V
DT	High-level input voltage	Over the V_{CC} range	2			V
	Low-level input voltage				1	V

NOTE 3: Ensured by design, not production tested.

digital control terminals

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	Over the V_{CC} range	2			V
Low-level input voltage				1	V

switching characteristics over recommended operating virtual junction temperature range, ENABLE = High, C_L = 3.3 nF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Rise time	HIGHDR output (see Note 3)	V_{BOOT} = 4.5 V,	V_{BOOTLO} = 0 V			60	ns
		V_{BOOT} = 6.5 V,	V_{BOOTLO} = 0 V			50	
		V_{BOOT} = 12 V,	V_{BOOTLO} = 0 V			50	
	LOWDR output (see Note 3)	V_{CC} = 4.5 V				40	ns
		V_{CC} = 6.5 V				30	
		V_{CC} = 12 V				30	
Fall time	HIGHDR output (see Note 3)	V_{BOOT} = 4.5 V,	V_{BOOTLO} = 0 V			60	ns
		V_{BOOT} = 6.5 V,	V_{BOOTLO} = 0 V			50	
		V_{BOOT} = 12 V,	V_{BOOTLO} = 0 V			50	
	LOWDR output (see Note 3)	V_{CC} = 4.5 V				40	ns
		V_{CC} = 6.5 V				30	
		V_{CC} = 12 V				30	
Propagation delay time	HIGHDR going low (excluding deadtime) (see Note 3)	V_{BOOT} = 4.5 V,	V_{BOOTLO} = 0 V			130	ns
		V_{BOOT} = 6.5 V,	V_{BOOTLO} = 0 V			100	
		V_{BOOT} = 12 V,	V_{BOOTLO} = 0 V			75	
	LOWDR going high (excluding deadtime) (see Note 3)	V_{BOOT} = 4.5 V,	V_{BOOTLO} = 0 V			80	ns
		V_{BOOT} = 6.5 V,	V_{BOOTLO} = 0 V			70	
		V_{BOOT} = 12 V,	V_{BOOTLO} = 0 V			60	
Propagation delay time	LOWDR going low (excluding deadtime) (see Note 3)	V_{CC} = 4.5 V				80	ns
		V_{CC} = 6.5 V				70	
		V_{CC} = 12 V				60	
Driver nonoverlap time	DT to LOWDR and LOWDR to HIGHDR (see Note 3)	V_{CC} = 4.5 V		40		170	ns
		V_{CC} = 6.5 V		25		135	
		V_{CC} = 12 V		15		85	

NOTE 3: Ensured by design, not production tested.

TYPICAL CHARACTERISTICS

RISE TIME
vs
SUPPLY VOLTAGE

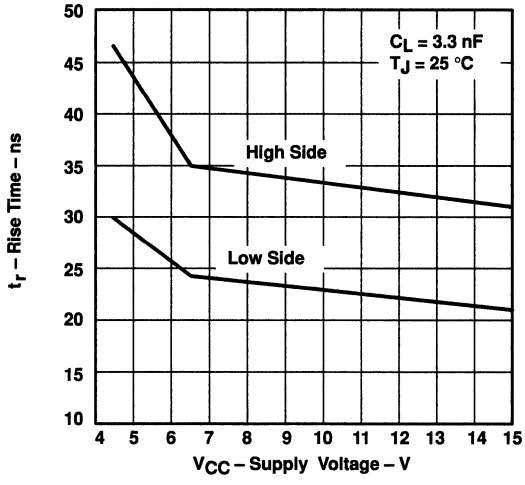


Figure 1

FALL TIME
vs
SUPPLY VOLTAGE

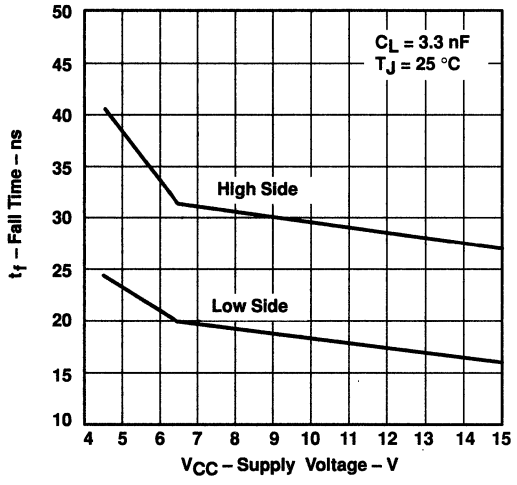


Figure 2

RISE TIME
vs
JUNCTION TEMPERATURE

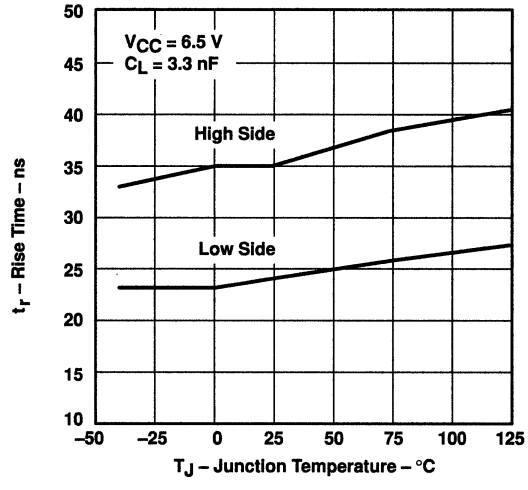


Figure 3

FALL TIME
vs
JUNCTION TEMPERATURE

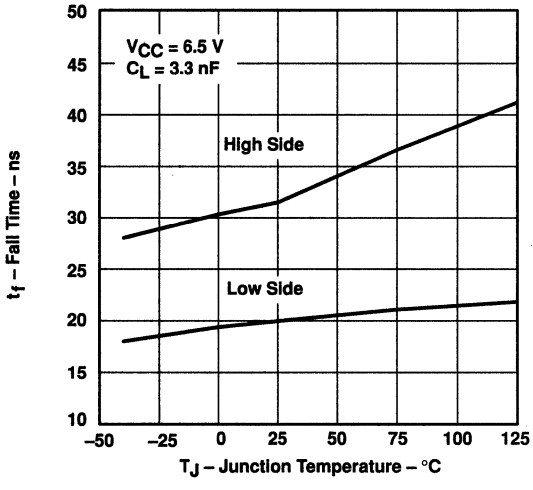


Figure 4

TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE, LOW TO HIGH LEVEL

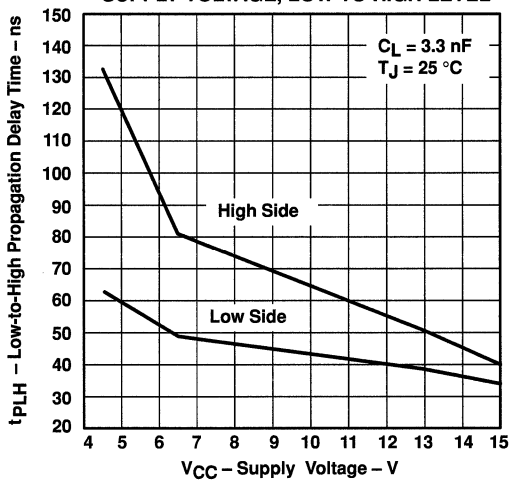


Figure 5

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE, HIGH TO LOW LEVEL

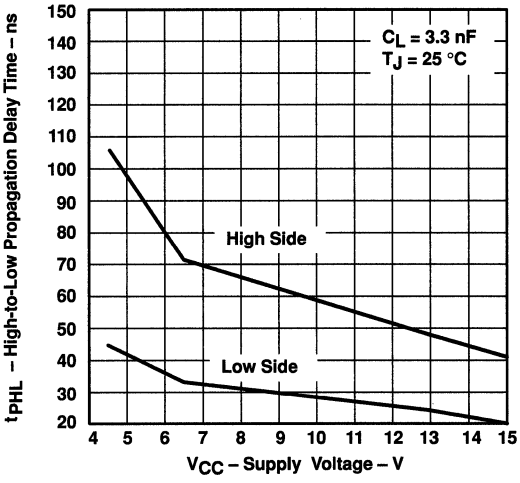


Figure 6

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
JUNCTION TEMPERATURE

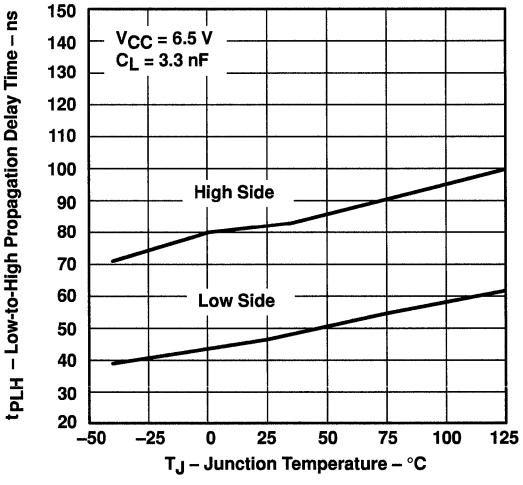


Figure 7

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
JUNCTION TEMPERATURE

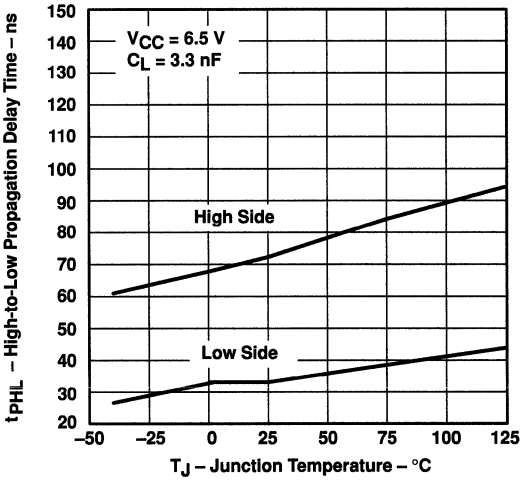


Figure 8

TYPICAL CHARACTERISTICS

RISE TIME
vs
LOAD CAPACITANCE

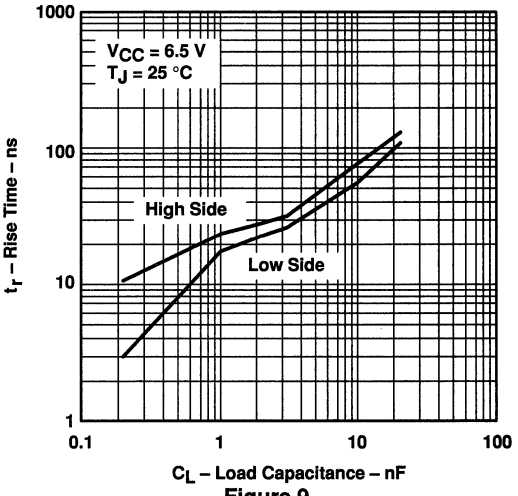


Figure 9

FALL TIME
vs
LOAD CAPACITANCE

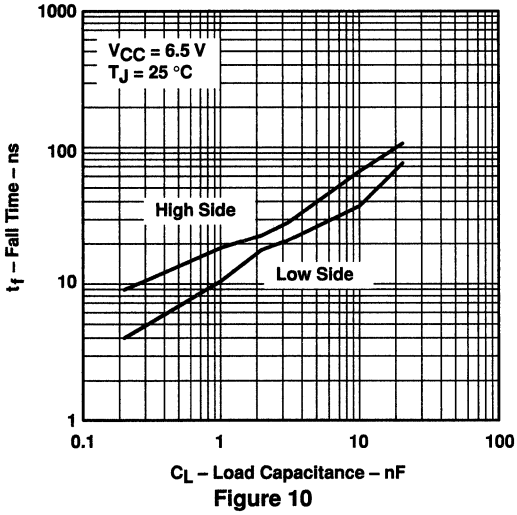


Figure 10

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

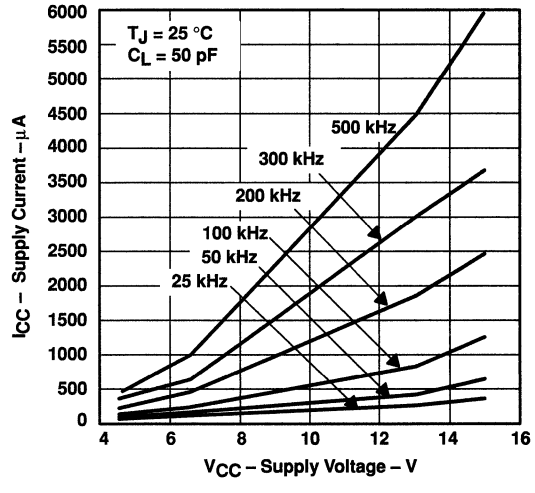


Figure 11

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

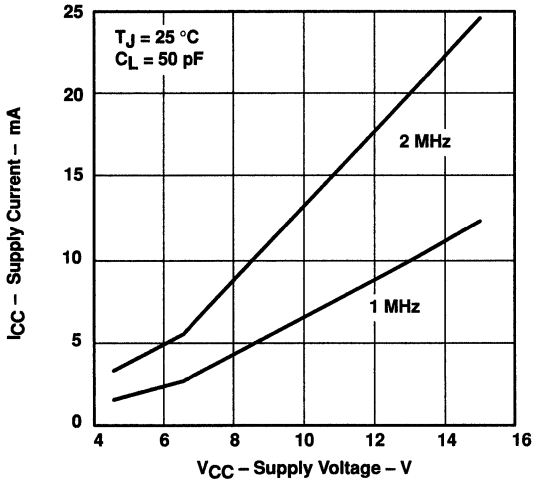


Figure 12

TYPICAL CHARACTERISTICS

PEAK SOURCE CURRENT
vs
DRIVE VOLTAGE

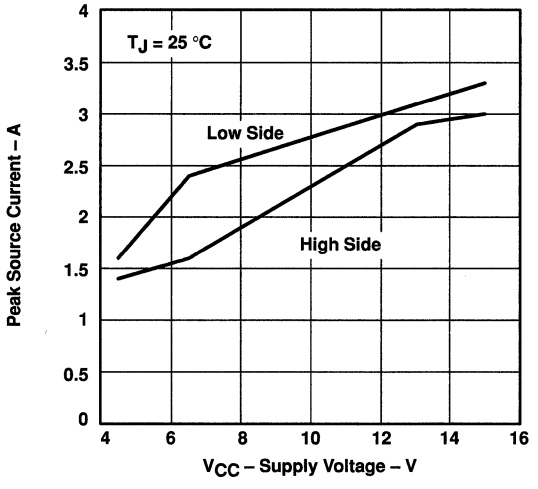


Figure 13

PEAK SINK CURRENT
vs
DRIVE VOLTAGE

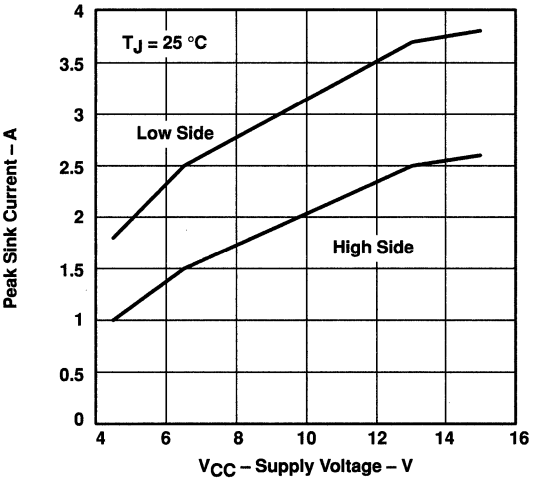


Figure 14

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

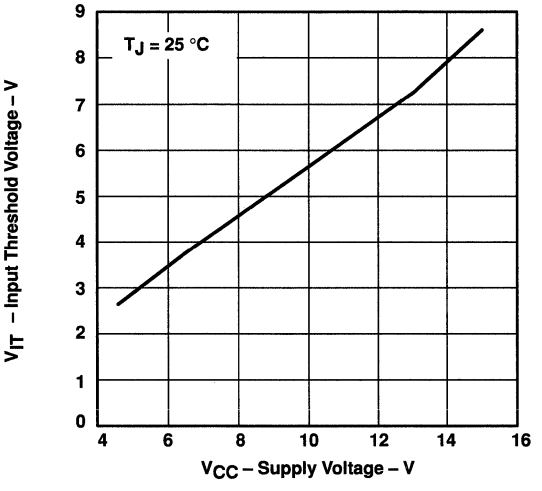


Figure 15

APPLICATION INFORMATION

Figure 15 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001A pulse-width-modulation (PWM) controller and a TPS2831 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3-V output. The circuit can supply 3 A continuous load. The converter achieves an efficiency of 94% for V_{IN} = 5 V, I_{load}=1 A, and 93% for V_{in} = 5 V, I_{load} = 3 A.

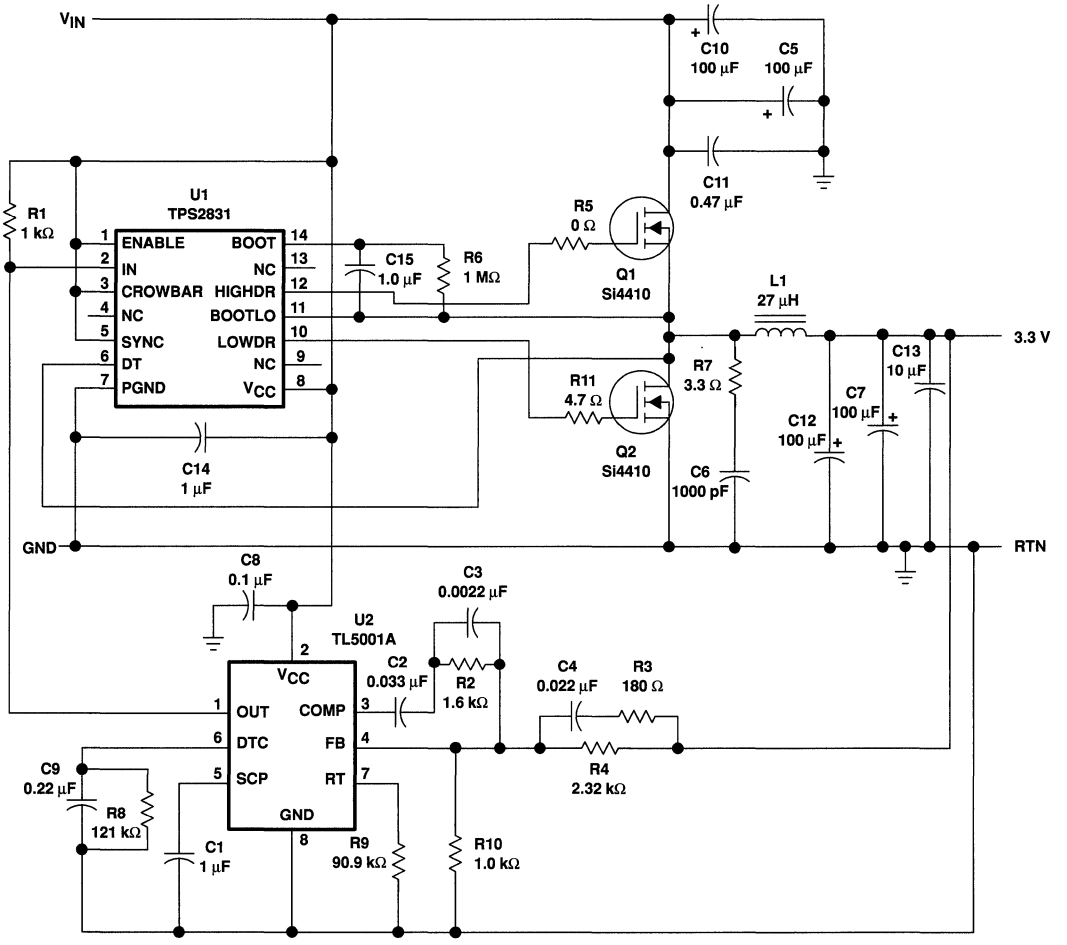


Figure 16. 3.3-V 3-A Synchronous-Buck Converter Circuit

APPLICATION INFORMATION

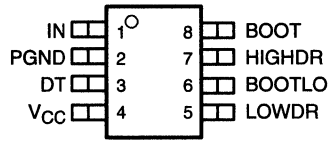
Great care should be taken when laying out the pc board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across V_{CC} and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A) This node is very sensitive to noise pick up and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have any other EMI problems and the power supply will be relatively free of noise.

- **Floating Bootstrap or Ground-Reference High-Side Driver**
- **Active Deadtime Control**
- **50-ns Max Rise/Fall Times and 100-ns Max Propagation Delay — 3-nF Load**
- **Ideal for High-Current Single or Mutiphase Applications**
- **2.4-A Typ Peak Output Current**
- **4.5-V to 15-V Supply Voltage Range**
- **Internal Schottky Bootstrap Diode**
- **Low Supply Current . . . 3–mA Typ**
- **–40°C to 125°C Junction-Temperature Operating Range**

D PACKAGE
(TOP VIEW)



description

The TPS2832 and TPS2833 are MOSFET drivers for synchronous-buck power stages. These devices are ideal for designing a high-performance power supply using a switching controller that does not include suitable MOSFET drivers on the chip. The drivers are designed to deliver 2.4-A peak currents into large capacitive loads. Higher currents can be controlled by using multiple drivers in a multiphase configuration. The high-side driver can be configured as a ground-reference driver or as a floating bootstrap driver. An adaptive dead-time control circuit eliminates shoot-through currents through the main power FETs during switching transitions and provides high efficiency for the buck regulator.

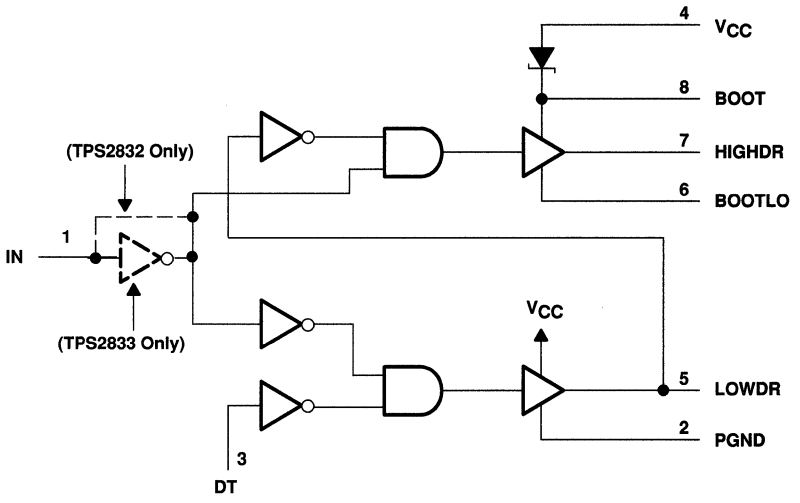
The TPS2832 has a noninverting input. The TPS2833 has an inverting input. The TPS2832/33 drivers, available in 8-terminal SOIC packages, operate over a junction temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES
	SOIC (D)
–40°C to 125°C	TPS2832D TPS2833D

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS2830DR)

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOT	8	I	Bootstrap terminal. A ceramic capacitor is connected between BOOT and BOOTLO terminals to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 µF and 1 µF. A 1-MΩ resistor should be connected across the bootstrap capacitor to provide a discharge path when the driver has been powered down.
BOOTLO	6	O	This terminal connects to the junction of the high-side and low-side MOSFETs.
DT	3	I	Deadtime control terminal. Connect DT to the junction of the high-side and low-side MOSFETs
HIGHDR	7	O	Output drive for the high-side power MOSFET
IN	1	I	Input signal to the MOSFET drivers (noninverting input for the TPS2832; inverting input for the TPS2833).
LOWDR	5	O	Output drive for the low-side power MOSFET
PGND	2		Power ground. Connect to the FET power ground.
V_{CC}	4	I	Input supply. Recommended that a 1 µF capacitor be connected from V_{CC} to PGND.

detailed description

low-side driver

The low-side driver is designed to drive low Rds(on) N-channel MOSFETs. The current rating of the driver is 2 A, source and sink.

high-side driver

The high-side driver is designed to drive low Rds(on) N-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured as a ground-reference driver or a floating bootstrap driver. The internal bootstrap diode, is a Schottky for improved drive efficiency. The maximum voltage that can be applied between the BOOT terminal and ground is 30 V.

deadtime (DT) control†

Deadtime control prevents shoot through current from flowing through the main power FETs during switching transitions by controlling the turn-on times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs (Vdrn) is low; the DT terminal connects to the junction of the power FETs.

IN†

The IN terminal is a digital terminal that is the input control signal for the drivers. The TPS2832 has a noninverting input; the TPS2833 has an inverting input.

†High-level input voltages on IN and DT must be greater than or equal to V_{CC}.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –0.3 V to 16 V
Input voltage range: BOOT to PGND (high-side driver ON) ..... –0.3 V to 30 V
BOOTLO to PGND ..... –0.3 V to 16 V
BOOT to BOOTLO ..... –0.3 V to 16 V
IN (see Note 2) ..... –0.3 V to 16 V
DT (see Note 2) ..... –0.3 V to 30 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise specified, all voltages are with respect to PGND.
2. High-level input voltages on the IN and DT terminals must be greater than or equal to V_{CC}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	580 mW	5.8 mW/°C	320 mW	232 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		15	V
Input voltage	BOOT to PGND	4.5		28	V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, C_L = 3.3 nF (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range			4.5		15	V
V_{CC}	Quiescent current	V_{CC} =15 V				100	µA
		V_{CC} =12 V, f_{SWX} = 200 kHz, C_{HIGHDR} = 50 pF,	BOOTLO grounded, C_{LOWDR} = 50 pF, See Note 3		3		mA

NOTE 3: Ensured by design, not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, C_L = 3.3 nF (unless otherwise noted) (continued)

output drivers

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output-current	High-side sink (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 4 V	0.7	1.1		A
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 5 V	1.1	1.5		
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} = 10.5 V	2	2.4		
	High-side source (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 0.5V	1.2	1.4		A
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 1.5 V	1.3	1.6		
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} = 1.5 V	2.3	2.7		
	Low-side sink (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	V_{CC} = 4.5 V, V_{LOWDR} = 4 V	1.3	1.8		A
			V_{CC} = 6.5 V, V_{LOWDR} = 5 V	2	2.5		
			V_{CC} = 12 V, V_{LOWDR} = 10.5 V	3	3.5		
	Low-side source (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	V_{CC} = 4.5 V, V_{LOWDR} = 0.5V	1.4	1.7		A
			V_{CC} = 6.5 V, V_{LOWDR} = 1.5 V	2	2.4		
			V_{CC} = 12 V, V_{LOWDR} = 1.5 V	2.5	3		
Output resistance	High-side sink (see Note 4)		$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 0.5 V			5	Ω
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 0.5 V			5	
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} = 0.5 V			5	
	High-side source (see Note 4)		$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 4 V			45	Ω
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 6 V			45	
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} =11.5 V			45	
	Low-side sink (see Note 4)		V_{DRV} = 4.5 V, V_{LOWDR} = 0.5 V			9	Ω
			V_{DRV} = 6.5 V V_{LOWDR} = 0.5 V			7.5	
			V_{DRV} = 12 V, V_{LOWDR} = 0.5 V			6	
	Low-side source (see Note 4)		V_{DRV} = 4.5 V, V_{LOWDR} = 4 V			45	Ω
			V_{DRV} = 6.5 V, V_{LOWDR} = 6 V			45	
			V_{DRV} = 12 V, V_{LOWDR} = 11.5 V			45	

NOTES: 3. Ensured by design, not production tested.
4. The pull-up/pull-down circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the Rds(on) of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

deadtime

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOWDR	High-level input voltage	Over the V_{CC} range (see Note 3)	2			V
	Low-level input voltage				1	V
DT	High-level input voltage	Over the V_{CC} range	2			V
	Low-level input voltage				1	V

NOTE 3: Ensured by design, not production tested.

digital control terminals

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	Over the V_{CC} range	2			V
Low-level input voltage				1	V

switching characteristics over recommended operating virtual junction temperature range, C_L = 3.3 nF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Rise time	HIGHDR output (see Note 3)	V_{BOOT} = 4.5 V,	V_{BOOTLO} = 0 V			60	ns
		V_{BOOT} = 6.5 V,	V_{BOOTLO} = 0 V			50	
		V_{BOOT} = 12 V,	V_{BOOTLO} = 0 V			50	
	LOWDR output (see Note 3)	V_{CC} = 4.5 V				40	ns
		V_{CC} = 6.5 V				30	
		V_{CC} = 12 V				30	
Fall time	HIGHDR output (see Note 3)	V_{BOOT} = 4.5 V,	V_{BOOTLO} = 0 V			60	ns
		V_{BOOT} = 6.5 V,	V_{BOOTLO} = 0 V			50	
		V_{BOOT} = 12 V,	V_{BOOTLO} = 0 V			50	
	LOWDR output (see Note 3)	V_{CC} = 4.5 V				40	ns
		V_{CC} = 6.5 V				30	
		V_{CC} = 12 V				30	
Propagation delay time	HIGHDR going low (excluding deadtime) (see Note 3)	V_{BOOT} = 4.5 V,	V_{BOOTLO} = 0 V			130	ns
		V_{BOOT} = 6.5 V,	V_{BOOTLO} = 0 V			100	
		V_{BOOT} = 12 V,	V_{BOOTLO} = 0 V			75	
	LOWDR going high (excluding deadtime) (see Note 3)	V_{BOOT} = 4.5 V,	V_{BOOTLO} = 0 V			80	ns
		V_{BOOT} = 6.5 V,	V_{BOOTLO} = 0 V			70	
		V_{BOOT} = 12 V,	V_{BOOTLO} = 0 V			60	
Propagation delay time	LOWDR going low (excluding deadtime) (see Note 3)	V_{CC} = 4.5 V				80	ns
		V_{CC} = 6.5 V				70	
		V_{CC} = 12 V				60	
Driver nonoverlap time	DT to LOWDR and LOWDR to HIGHDR (see Note 3)	V_{CC} = 4.5 V		40		170	ns
		V_{CC} = 6.5 V		25		135	
		V_{CC} = 12 V		15		85	

NOTE 3: Ensured by design, not production tested.

TYPICAL CHARACTERISTICS

RISE TIME
vs
SUPPLY VOLTAGE

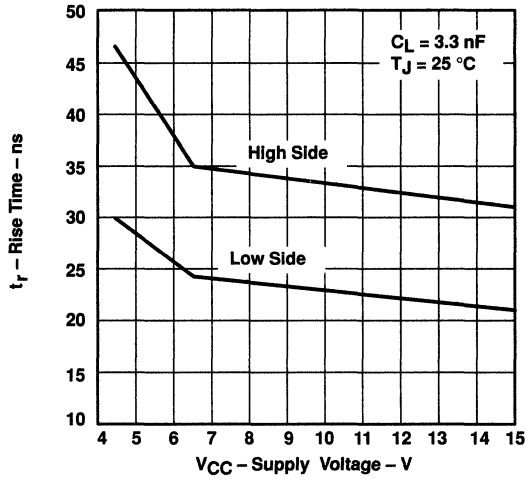


Figure 1

FALL TIME
vs
SUPPLY VOLTAGE

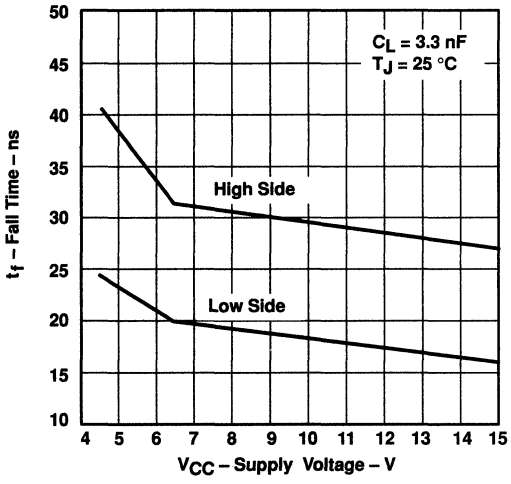


Figure 2

RISE TIME
vs
JUNCTION TEMPERATURE

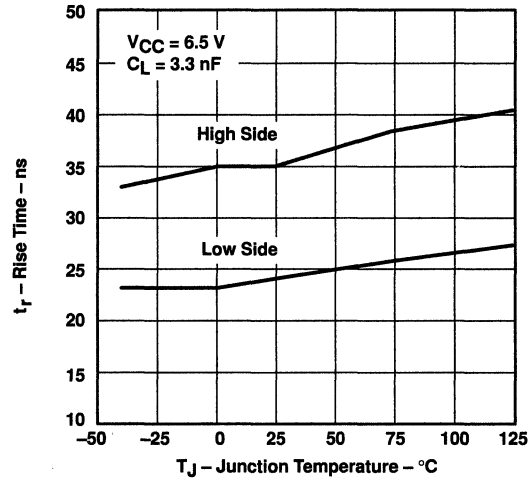


Figure 3

FALL TIME
vs
JUNCTION TEMPERATURE

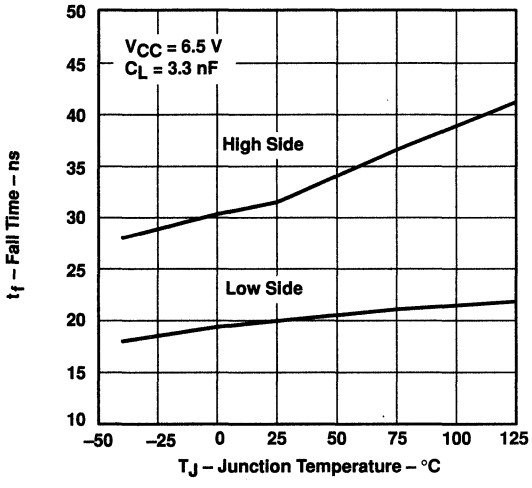


Figure 4

TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE, LOW TO HIGH LEVEL

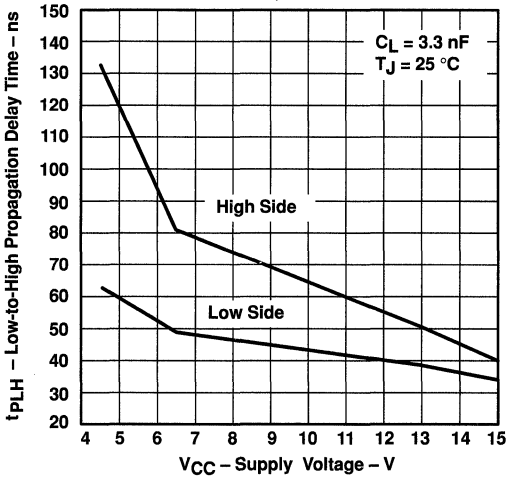


Figure 5

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE, HIGH TO LOW LEVEL

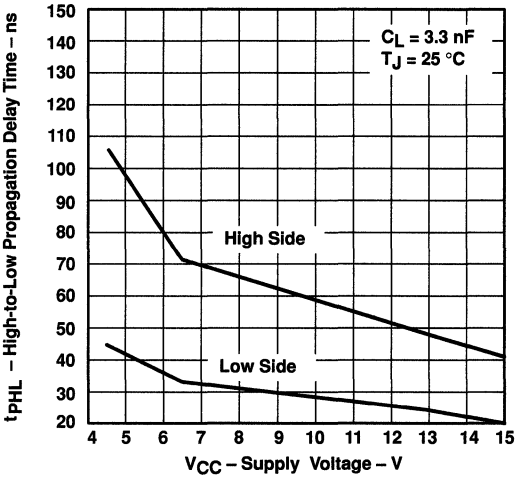


Figure 6

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
JUNCTION TEMPERATURE

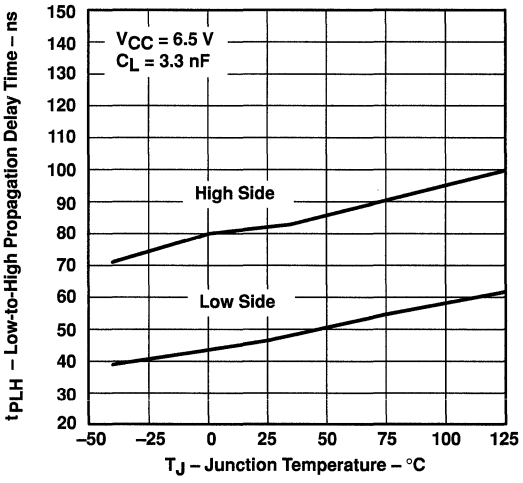


Figure 7

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
JUNCTION TEMPERATURE

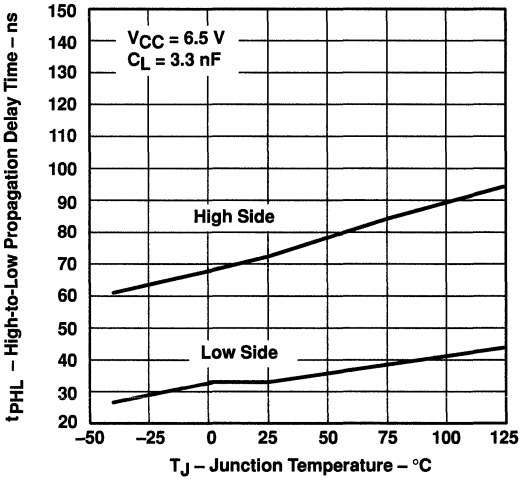


Figure 8

TYPICAL CHARACTERISTICS

RISE TIME
vs
LOAD CAPACITANCE

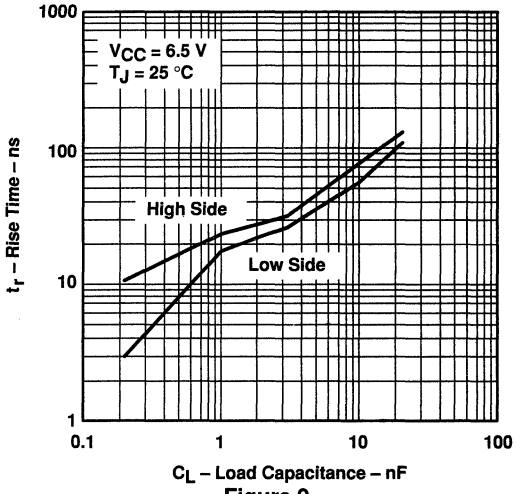


Figure 9

FALL TIME
vs
LOAD CAPACITANCE

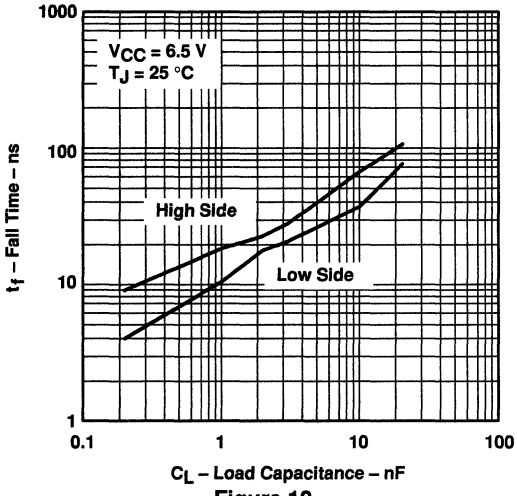


Figure 10

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

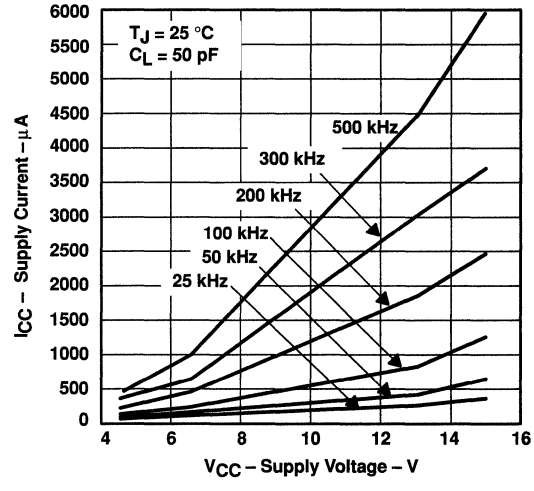


Figure 11

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

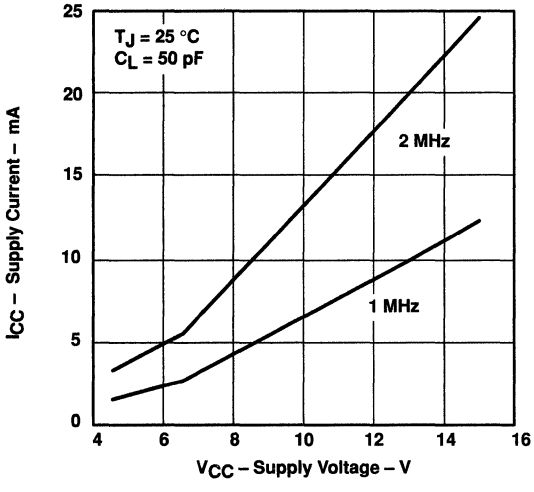


Figure 12

TYPICAL CHARACTERISTICS

PEAK SOURCE CURRENT
vs
DRIVE VOLTAGE

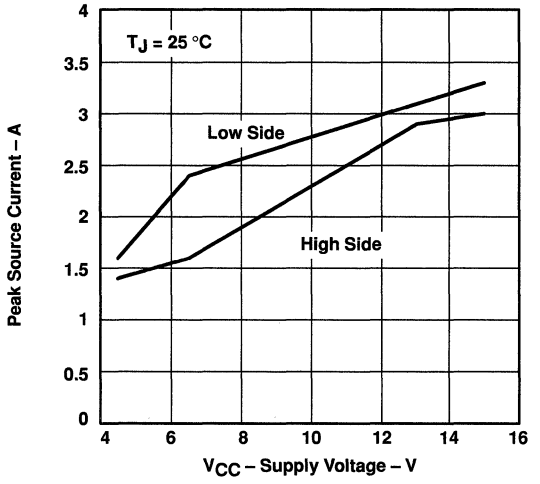


Figure 13

PEAK SINK CURRENT
vs
DRIVE VOLTAGE

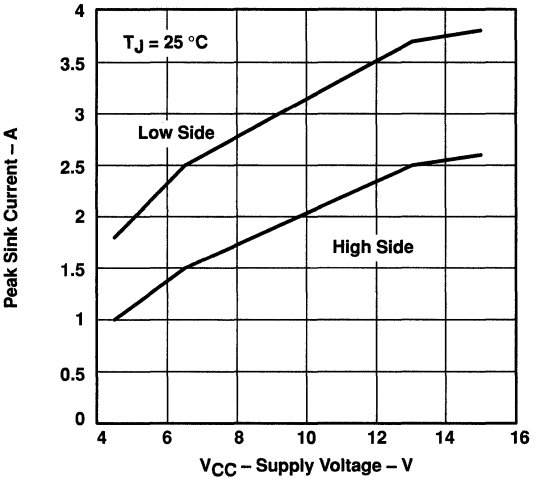


Figure 14

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

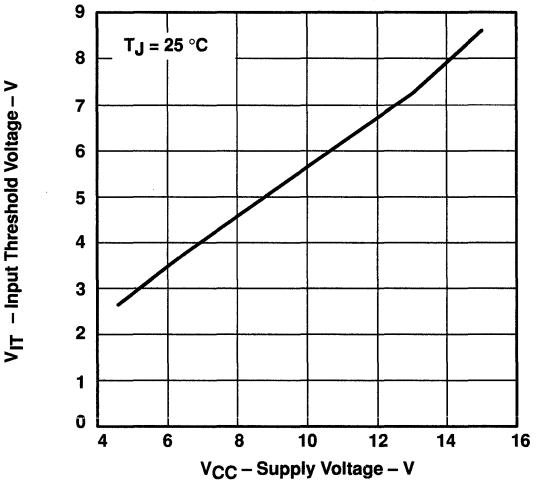


Figure 15

APPLICATION INFORMATION

Figure 15 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001A pulse-width-modulation (PWM) controller and a TPS2833 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3 V output. The circuit can supply 3 A continuous load and the transient load is 5 A. The converter achieves an efficiency of 94% for V_{IN} = 5 V, I_{load}=1 A, and 93% for V_{in} = 5 V, I_{load} = 3 A.

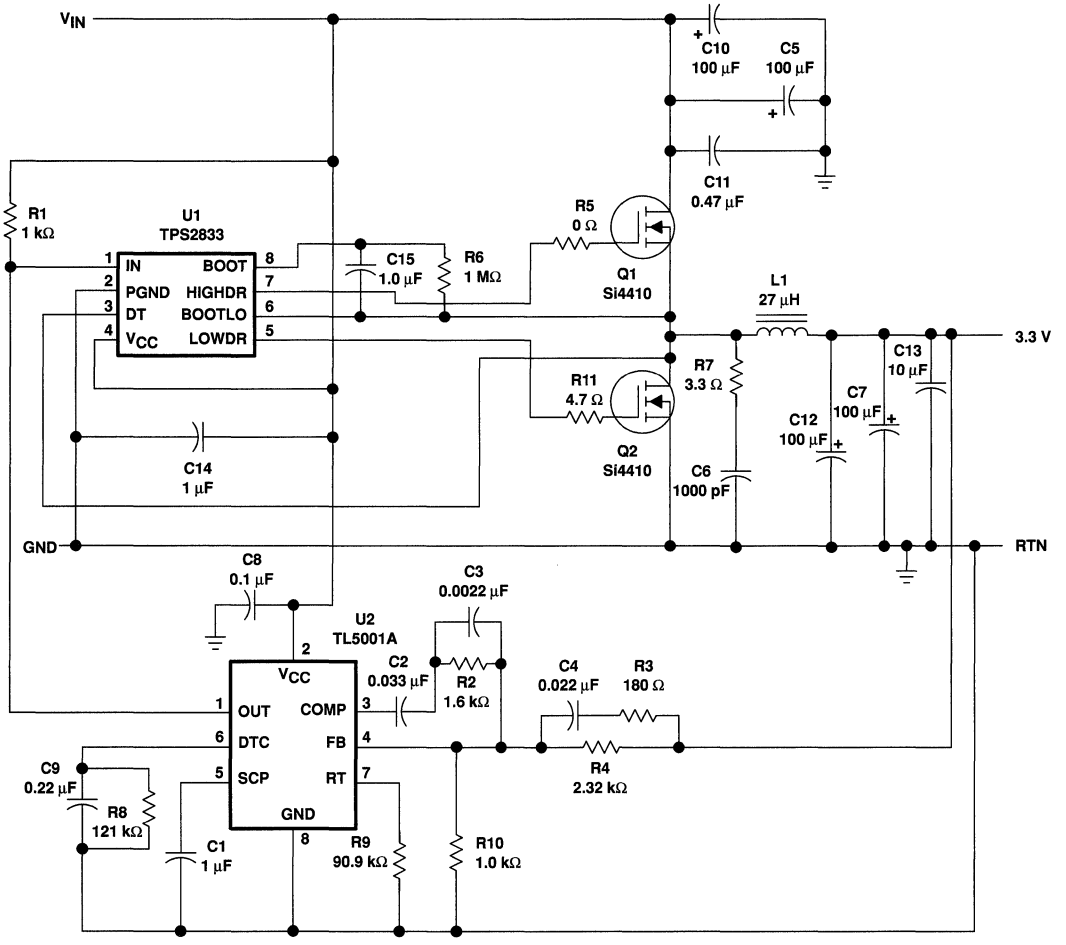


Figure 16. 3.3 V 3 A Synchronous-Buck Converter Circuit

APPLICATION INFORMATION

Great care should be taken when laying out the pc board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

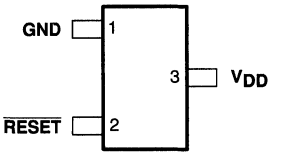
Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across V_{CC} and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A) This node is very sensitive to noise pick up and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have any other EMI problems and the power supply will be relatively free of noise.

SLVS228 – AUGUST 1999

- **3-Pin SOT-23 Package**
- **Supply Current of 9 μA (Typical)**
- **Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, 5 V**
- **Power-On Reset Generator With Fixed Delay Time of 200 ms**
- **Pin-For-Pin Compatible With MAX 809**
- **Temperature Range . . . –40°C to 85°C**

TPS3809 . . . DBV PACKAGE
(TOP VIEW)



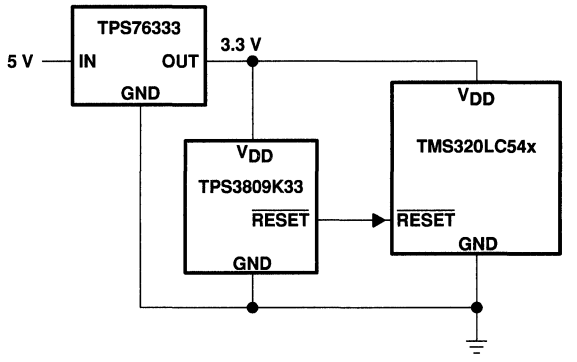
description

The TPS3809 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage V_{IT}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d(typ)}$ = 200 ms, starts after V_{DD} has risen above the threshold voltage V_{IT}. When the supply voltage drops below the threshold voltage V_{IT}, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed sense-threshold voltage V_{IT} set by an internal voltage divider.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23. The TPS3809 devices are characterized for operation over a temperature range of –40°C to 85°C.

typical applications



- **Applications Using DSPs, Microcontrollers, or Microprocessors**
- **Wireless Communication Systems**
- **Portable/Battery-Powered Equipment**
- **Programmable Controls**
- **Intelligent Instruments**
- **Industrial Equipment**
- **Notebook/Desktop Computers**
- **Automotive Systems**

AVAILABLE OPTIONS

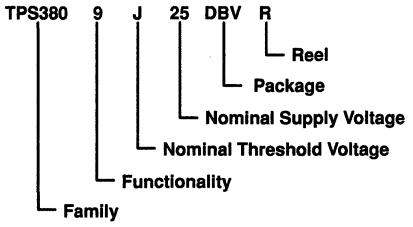
T_A	DEVICE NAME		THRESHOLD VOLTAGE	MARKING
–40°C to 85°C	TPS3809J25DBVR†	TPS3809J25DBVT‡	2.25 V	PCZI
	TPS3809L30DBVR†	TPS3809L30DBVT‡	2.64 V	PDAI
	TPS3809K33DBVR†	TPS3809K33DBVT‡	2.93 V	PDBI
	TPS3809I50DBVR†	TPS3809I50DBVT‡	4.55 V	PDCI

† The DBVR passive indicates tape and reel of 3000 parts.
‡ The DBVT passive indicates tape and reel of 250 parts.

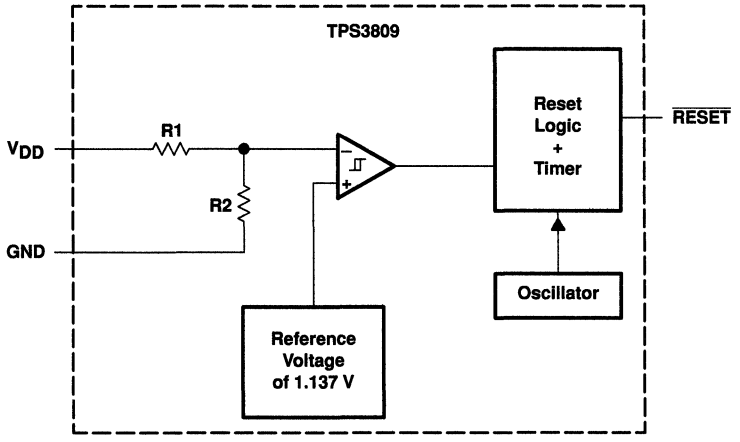
FUNCTION/TRUTH TABLE, TPS3809

$V_{DD}>V_{IT}$	$\overline{RESET}$
0	L
1	H

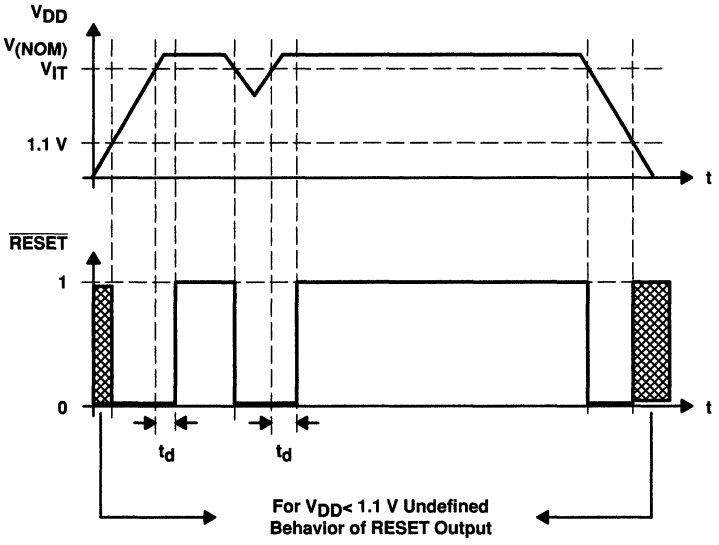
ORDERING INFORMATION



functional block diagram



timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1) ..... 7 V
All other pins (see Note 1) ..... –0.3 V to 7 V
Maximum low output current, I_{OL} ..... 5 mA
Maximum high output current, I_{OH} ..... –5 mA
Input clamp current, I_{IK} (V_I<0 or V_I>V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O<0 or V_O>V_{DD}) ..... ±20 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... –40°C to 85°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Soldering temperature ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t=1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	T_A <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 2.5 V to 6 V,	I_{OH} = –500 µA	V_{DD} –0.2			V
			V_{DD} = 3.3 V,	I_{OH} = –2 mA	V_{DD} –0.4			
			V_{DD} = 6 V,	I_{OH} = –4 mA	V_{DD} –0.4			
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V,	I_{OL} = 500 µA			0.2	V
			V_{DD} = 3.3 V,	I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V,	I_{OL} = 4 mA			0.4	
	Power-up reset voltage (see Note 2)		V_{DD} ≥ 1.1 V,	I_{OL} = 50 µA			0.2	V
V_{IT-}	Negative-going input threshold voltage (see Note 3)	TPS3809J25	T_A – 40°C to 85°C		2.20	2.25	2.30	V
		TPS3809L30			2.58	2.64	2.70	
		TPS3809K33			2.87	2.93	2.99	
		TPS3809I50			4.45	4.55	4.65	
V_{hys}	Hysteresis	TPS3809J25				30		mV
		TPS3809L30				35		
		TPS3809K33				40		
		TPS3809I50				60		
I_{DD}	Supply current		V_{DD} = 2 V, Output unconnected			9	12	µA
			V_{DD} = 6 V, Output unconnected			20	25	
C_i	Input capacitance		V_I = 0 V to V_{DD}			5		pF

NOTES: 2. The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥ 15 µs/V.
3. To ensure best stability of the threshold voltage, a bypass capacitor (0.1 µF ceramic) should be placed near the supply terminals.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	at V_{DD}	V_{DD} = V_{IT-} + 0.2 V, V_{DD} = V_{IT-} – 0.2 V	3			µs

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		V_{DD} ≥ V_{IT-} + 0.2 V, See timing diagram	120	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay	V_{IL} = V_{IT-} –0.2 V, V_{IH} = V_{IT-} +0.2 V		1		µs

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

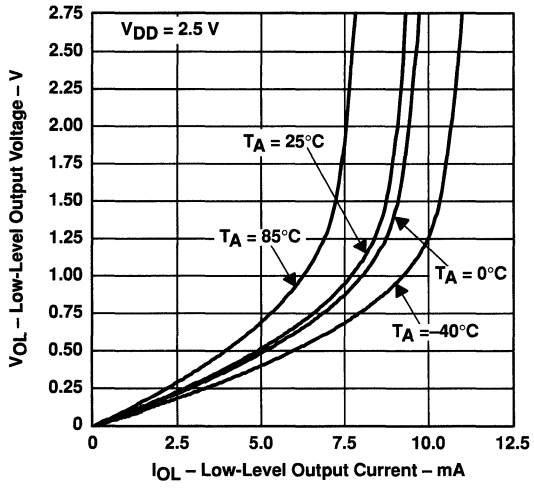


Figure 1

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

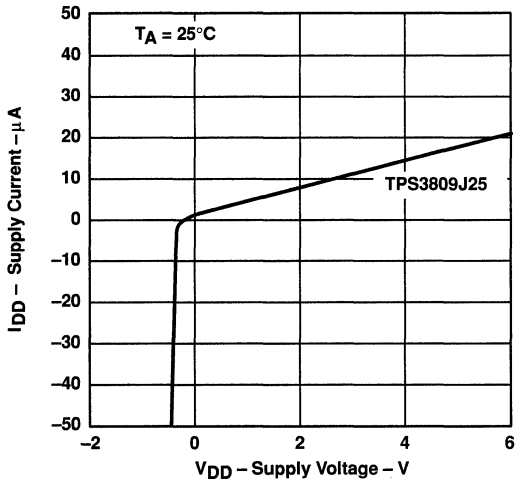


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

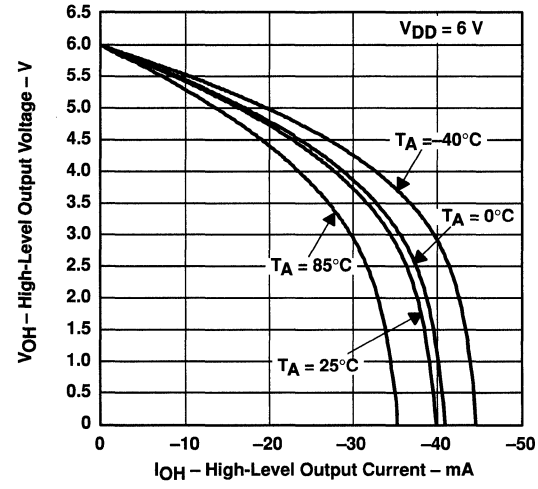


Figure 3

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

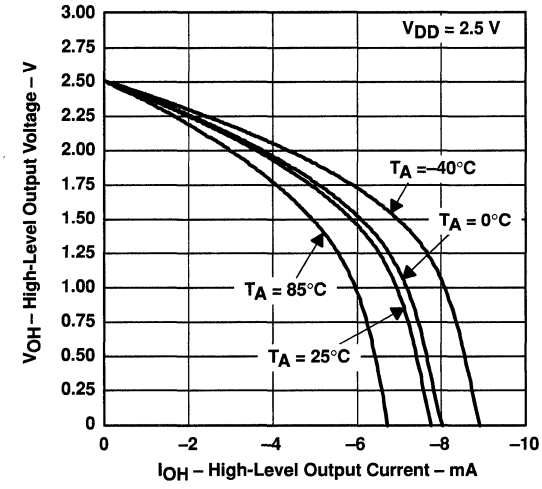


Figure 4

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE AT V_{DD}

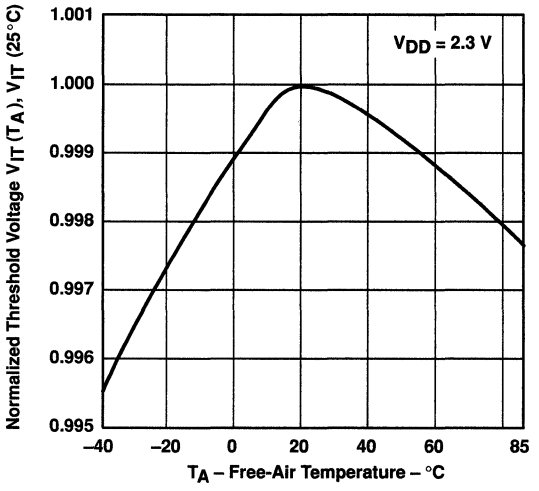


Figure 5

MINIMUM PULSE DURATION AT V_{DD}
vs
V_{DD} THRESHOLD OVERDRIVE VOLTAGE

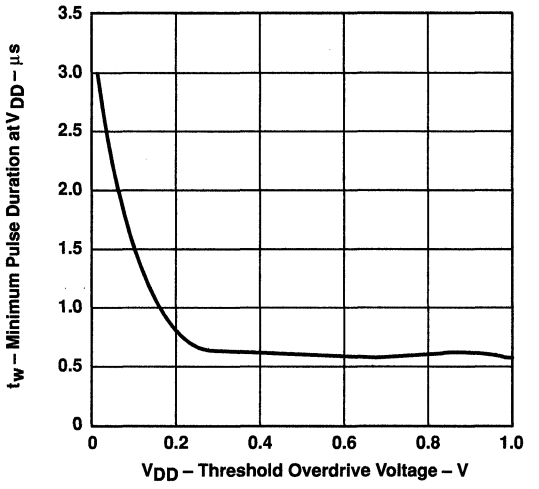
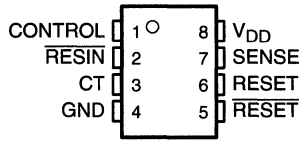


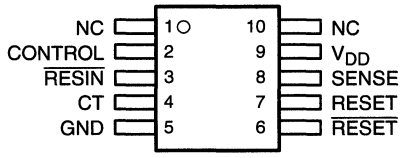
Figure 6

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **Programmable Delay Time by External Capacitor**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{DD} \geq 1$ V**
- **Power-Down Control Support for Static RAM With Battery Backup**
- **Maximum Supply Current of 16 μA**
- **Power Saving Totem-Pole Outputs**
- **Temperature Range . . . –40°C to 125°C**

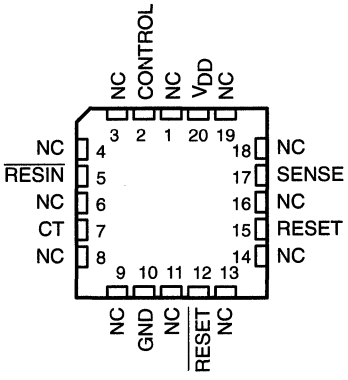
D, JG, P OR PW PACKAGE
(TOP VIEW)



U PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum V_{DD} ($\geq$ 2 V) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(SENSE)}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_d, is determined by an external capacitor:

$$t_d = 2.1 \times 10^4 \times C_T$$

Where

C_T is in farads

t_d is in seconds

Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed SENSE threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time, t_d, has expired.

description (continued)

In addition to the power-on-reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ($\overline{CS}$) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ($\overline{CSH1}$) of the microprocessor (see Figure 10), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

The TLC77xxI is characterized for operation over a temperature range of –40°C to 85°C; the TLC77xxQ is characterized for operation over a temperature range of –40°C to 125°C; and the TLC77xxM is characterized for operation over the full Military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	THRESHOLD VOLTAGE (V)	PACKAGED DEVICES					
		SMALL OUTLINE (D)†	CHIP CARRIER (FK)	CERAMIC DIP (JG)	CERAMIC DUAL FLATPACK (U)	PLASTIC DIP (P)	THIN SHRINK SMALL OUTLINE (PW)‡
–40°C to 85°C	1.1	TLC7701ID	—	—	—	TLC7701IP	TLC7701IPW
	2.25	TLC7725ID	—	—	—	TLC7725IP	TLC7725IPW
	2.63	TLC7703ID	—	—	—	TLC7703IP	TLC7703IPW
	2.93	TLC7733ID	—	—	—	TLC7733IP	TLC7733IPW
	4.55	TLC7705ID	—	—	—	TLC7705IP	TLC7705IPW
–40°C to 125°C	1.1	TLC7701QD	—	—	—	TLC7701QP	TLC7701QPW
	2.25	TLC7725QD	—	—	—	TLC7725QP	TLC7725QPW
	2.63	TLC7703QD	—	—	—	TLC7703QP	TLC7703QPW
	2.93	TLC7733QD	—	—	—	TLC7733QP	TLC7733QPW
	4.55	TLC7705QD	—	—	—	TLC7705QP	TLC7705QPW
–55°C to 125°C	2.93	—	TLC7733MFK	TLC7733MJG	—	—	—
	4.55	—	TLC7705MFK	TLC7705MJG	TLC7705MU	—	—

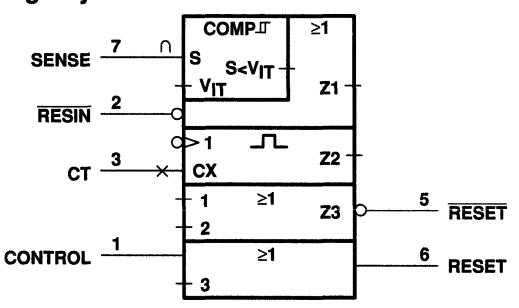
† The D package is available taped and reeled. Add the suffix R to the device type when ordering (e.g., TLC7705QDR).
‡ The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TLC7705QPWLE).

FUNCTION TABLE

CONTROL	$\overline{RESIN}$	$V_{I(SENSE)} > V_{IT+}$	RESET	$\overline{RESET}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L§	H§
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H§

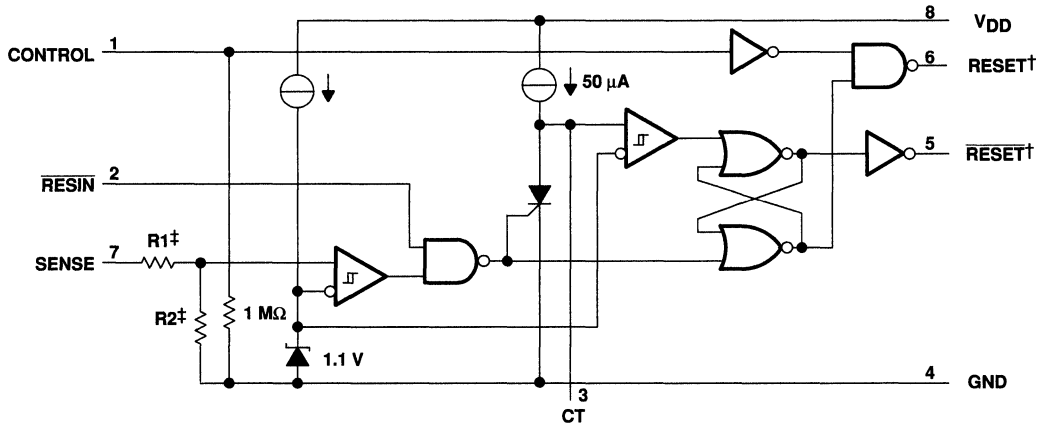
§ RESET and $\overline{RESET}$ states shown are valid for $t > t_d$.

logic symbol¶



¶ This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617-12.

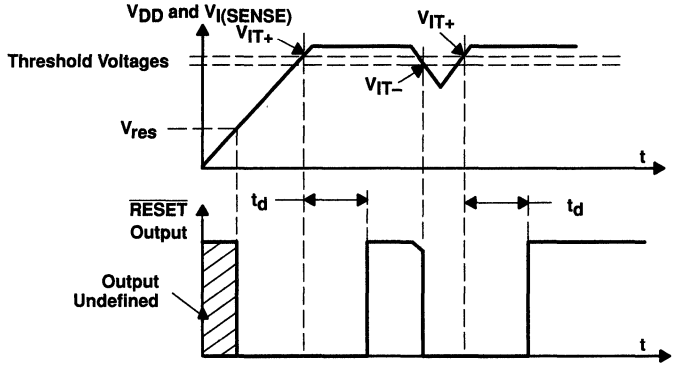
functional block diagram



† Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.
‡ Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	∞
TLC7725	600 kΩ	600 kΩ
TLC7703	698 kΩ	502 kΩ
TLC7733	750 kΩ	450 kΩ
TLC7705	910 kΩ	290 kΩ

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 7 V
Input voltage range, CONTROL, $\overline{RESIN}$, SENSE (see Note 1) ..... −0.3 V to 7 V
Maximum low output current, I_{OL} ..... 10 mA
Maximum high output current, I_{OH} ..... −10 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) ..... ±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±10 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TL77xxI ..... −40°C to 85°C
TL77xxQ ..... −40°C to 125°C
TL77xxM ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
P	1000 mW	8.0 mW/°C	520 mW	200 mW
PW	525 mW	4.2 mW/°C	273 mW	105 mW
U	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions at specified temperature range

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	6	V
Input voltage, V_I		0	V_{DD}	V
High-level input voltage at $\overline{RESIN}$ and CONTROL‡, V_{IH}		0.7×V_{DD}		V
Low-level input voltage at $\overline{RESIN}$ and CONTROL‡, V_{IL}			0.2×V_{DD}	V
High-level output current, I_{OH}	$V_{DD} \ge 2.7$ V		−2	mA
Low-level output current, I_{OL}	$V_{DD} \ge 2.7$ V		2	mA
Input transition rise and fall rate at $\overline{RESIN}$ and CONTROL, $\Delta t/\Delta V$			100	ns/V
Operating free-air temperature range, T_A	TLC77xxI	−40	85	°C
	TLC77xxQ	−40	125	
Operating free-air temperature range, T_A	TLC77xxM	−55	125	°C

‡ To ensure a low supply current, V_{IL} should be kept < 0.3 V and $V_{IH} > V_{DD} - 0.3$ V.

electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TLC77xx			UNIT
					MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = –20 µA		V_{DD} = 2 V	1.8			V
				V_{DD} = 2.7 V	2.5			
				V_{DD} = 4.5 V	4.3			
		I_{OH} = –2 mA		V_{DD} = 4.5 V	3.7			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA		V_{DD} = 2 V			0.2	V
				V_{DD} = 2.7 V			0.2	
				V_{DD} = 4.5 V			0.2	
		I_{OL} = 2 mA		V_{DD} = 4.5 V			0.5	
V_{IT-}	Negative-going input threshold voltage, SENSE (see Note 3)		TLC7701	V_{DD} = 2 V to 6 V	1.04	1.1	1.16	V
			TLC7725		2.18	2.25	2.32	
			TLC7703		2.56	2.63	2.70	
			TLC7733		2.86	2.93	3	
			TLC7705		4.47	4.55	4.63	
V_{hys}	Hysteresis voltage, SENSE		TLC7701	V_{DD} = 2 V to 6 V		30		mV
			TLC7725	V_{DD} = 2 V to 6 V		70		mV
			TLC7703,					
			TLC7733,					
			TLC7705					
V_{res}	Power-up reset voltage‡			I_{OL} = 20 µA			1	V
I_I	Input current	$\overline{RESIN}$		V_I = 0 V to V_{DD}			2	µA
		CONTROL		V_I = V_{DD}		7	15	
		SENSE		V_I = 5 V		5	10	
		SENSE, TLC7701 only		V_I = 5 V			2	
I_{DD}	Supply current			$\overline{RESIN}$ = V_{DD}, SENSE = V_{DD} ≥ V_{IT}max + 0.2 V, CONTROL = 0 V, Outputs open		9	16	µA
$I_{DD(d)}$	Supply current during t_d			V_{DD} = 5 V, V_{CT} = 0, $\overline{RESIN}$ = V_{DD}, SENSE = V_{DD}, CONTROL = 0 V, Outputs open		120	150	µA
C_I	Input capacitance, SENSE			V_I = 0 V to V_{DD}		50		pF

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which $\overline{RESET}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD} ≥ 15 µs/V.

NOTES: 2. All characteristics are measured with C_T = 0.1 µF.

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be connected near the supply terminals.

electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER				TEST CONDITIONS		TLC77xxM			UNIT
						MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = –20 µA		V_{DD} = 2 V,	T_A = 25°C	1.8			V
					T_A = –55°C to 125°C	1.7			
				V_{DD} = 2.7 V	T_A = 25°C	2.5			
					T_A = –55°C to 125°C	2.3			
				V_{DD} = 4.5 V	T_A = 25°C	4.3			
					T_A = –55°C to 125°C	4.2			
		I_{OH} = –2 mA		V_{DD} = 4.5 V	T_A = 25°C	3.7			
					T_A = –55°C to 125°C	3.6			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA		V_{DD} = 2 V	T_A = 25°C			0.2	V
					T_A = –55°C to 125°C			0.2	
				V_{DD} = 2.7 V	T_A = 25°C			0.2	
					T_A = –55°C to 125°C			0.2	
				V_{DD} = 4.5 V	T_A = 25°C			0.2	
					T_A = –55°C to 125°C			0.2	
		I_{OL} = 2 mA		V_{DD} = 4.5 V	T_A = 25°C			0.5	
					T_A = –55°C to 125°C			0.5	
V_{IT-}	Negative-going input threshold voltage, SENSE (see Note 3)		TLC7733	V_{DD} = 2 V to 6 V		2.86	2.93	3.1	V
			TLC7705			4.3	4.5	4.8	
V_{hys}	Hysteresis voltage, SENSE			V_{DD} = 2 V to 6 V	V_{DD} = 2 V to 6 V		70		mV
V_{res}	Power-up reset voltage‡			I_{OL} = 20 µA				1	V
I_I	Input current	$\overline{RESIN}$		V_I = 0 V to V_{DD}				2	µA
		CONTROL		V_I = V_{DD}			7	15	
		SENSE		V_I = 5 V			5	10	
		SENSE, TLC7701 only		V_I = 5 V				2	
I_{DD}	Supply current			$\overline{RESIN}$ = V_{DD}, SENSE = V_{DD} ≥ V_{IT}max + 0.2 V, CONTROL = 0 V, Outputs open			9	16	µA
$I_{DD(d)}$	Supply current during t_d		TLC7733	V_{CT} = 0, $\overline{RESIN}$ = V_{DD}, CONTROL = 0 V, SENSE = V_{DD}, Outputs open	V_{DD} = 3.3 V			250	µA
			TLC7705		V_{DD} = 5 V		120	150	
C_I	Input capacitance, SENSE			V_I = 0 V to V_{DD}			50		pF

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which $\overline{RESET}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD} ≥ 15 µs/V.

NOTES: 2. All characteristics are measured with C_T = 0.1 µF.

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminals.

switching characteristics at V_{DD} = 5 V, R_L = 2 kΩ, C_L = 50 pF, T_A = 25°C

PARAMETER		MEASURED FROM (INPUT)	MEASURED TO (OUTPUT)	TEST CONDITIONS	TLC77xx MIN	TLC77xx TYP	TLC77xx MAX	UNIT
t_d	Delay time	$V_{I(SENSE)} \geq V_{IT+}$	RESET and $\overline{\text{RESET}}$	$\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CONTROL = 0.2 × V_{DD}, C_T = 100 nF, See timing diagram	1.1	2.1	4.2	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min – 0.2 V, $\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CONTROL = 0.2 × V_{DD}, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						5	
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				5	
t_{PHL}	Propagation delay time, high-to-low-level output						20	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × V_{DD}, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.2 × V_{DD}, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						40	ns
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				45	ns
t_{PHL}	Propagation delay time, high-to-low-level output						20	µs
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × V_{DD}, SENSE = V_{IT+}max + 0.2 V, $\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CT = NC†			38	ns
t_{PHL}	Propagation delay time, high-to-low-level output						38	ns
	Low-level minimum pulse duration to switch RESET and $\overline{\text{RESET}}$	SENSE		$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min – 0.2 V,	3			µs
		$\overline{\text{RESIN}}$		V_{IL} = 0.2 × V_{DD}, V_{IH} = 0.7 × V_{DD}	1			
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%		8		ns/V
t_f	Fall time			90% to 10%		4		

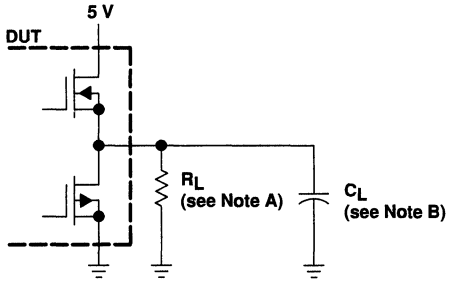
† NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

switching characteristics at V_{DD} = 5 V, R_L = 2 kΩ, C_L = 50 pF

PARAMETER		MEASURED FROM (INPUT)	MEASURED TO (OUTPUT)	TEST CONDITIONS	T_A	TLC77xxM MIN	TLC77xxM TYP	TLC77xxM MAX	UNIT
t_d	Delay time	$V_{I(SENSE)} \geq V_{IT+}$	RESET and $\overline{RESET}$	$\overline{RESIN}$ = 2.7 V, CONTROL = 0.4 V, C_T = 100 nF, See timing diagram	25°C	1.1	2.1	4.2	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{RESET}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min – 0.2 V, $\overline{RESIN}$ = 2.7 V, CONTROL = 0.4 V, CT = NC†	25°C			20	µs
					Full range			24	
			RESET		25°C			5	µs
					Full range			7	
t_{PHL}	Propagation delay time, high-to-low-level output	SENSE	$\overline{RESET}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min – 0.2 V, $\overline{RESIN}$ = 2.7 V, CONTROL = 0.4 V, CT = NC†	25°C			5	µs
					Full range			7	
			RESET		25°C			20	µs
					Full range			24	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{RESIN}$	$\overline{RESET}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.4 V, CT = NC†	25°C			20	µs
					Full range			24	
			RESET		25°C			45	ns
					Full range			65	
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{RESIN}$	$\overline{RESET}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.4 V, CT = NC†	25°C			40	ns
					Full range			60	
			RESET		25°C			20	µs
					Full range			24	
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, $\overline{RESIN}$ = 2.7 V, CT = NC†	25°C			38	ns
					Full range			58	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C			38	ns
					Full range			58	
	Low-level minimum pulse duration	SENSE		$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min – 0.2 V,	Full range	3			µs
		$\overline{RESIN}$		V_{IL} = 0.4 V, V_{IH} = 2.7 V		1			
t_r	Rise time		RESET and $\overline{RESET}$	10% to 90%	Full range		8		ns/V
t_f	Fall time			90% to 10%			4		

† NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. For switching characteristics, R_L = 2 kΩ.
B. C_L = 50 pF includes jig and probe capacitance.

Figure 1. RESET AND $\overline{\text{RESET}}$ Output Configurations

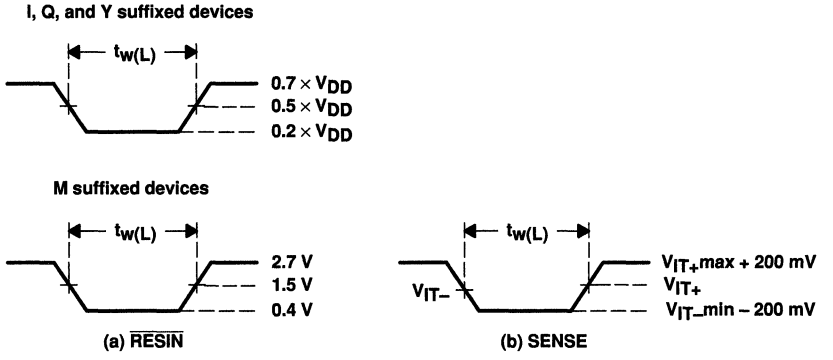


Figure 2. Input Pulse Definition Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE
vs
TEMPERATURE

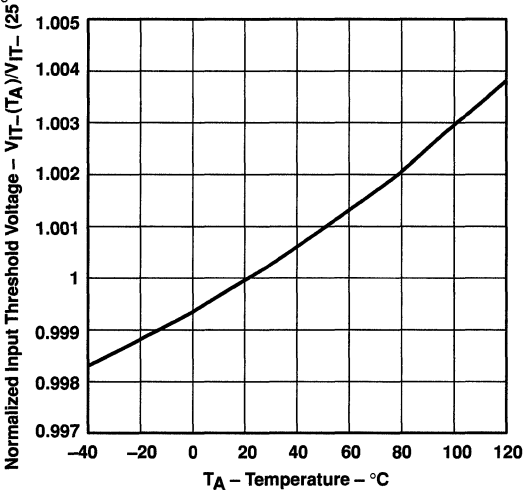


Figure 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

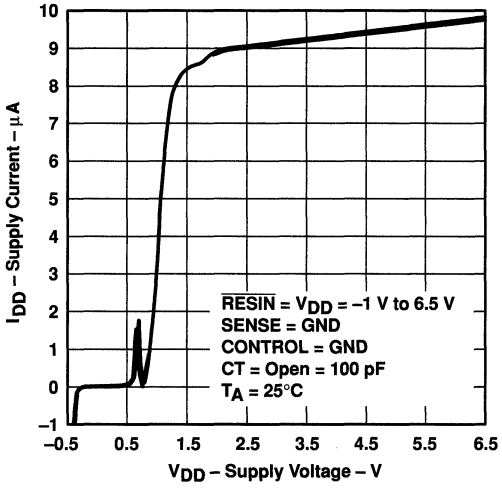


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

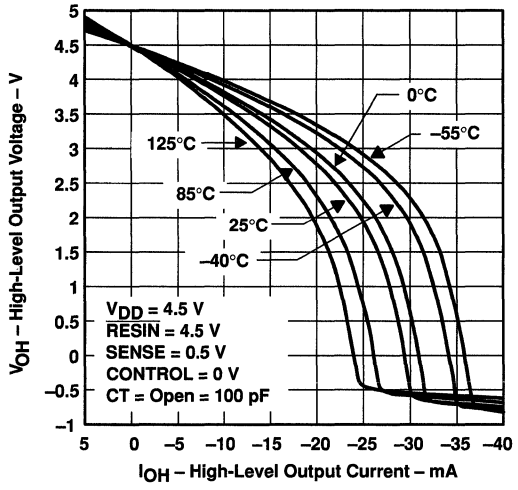


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

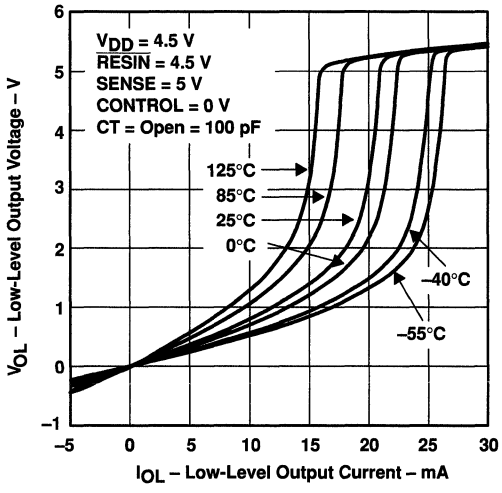


Figure 6

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE AT SENSE

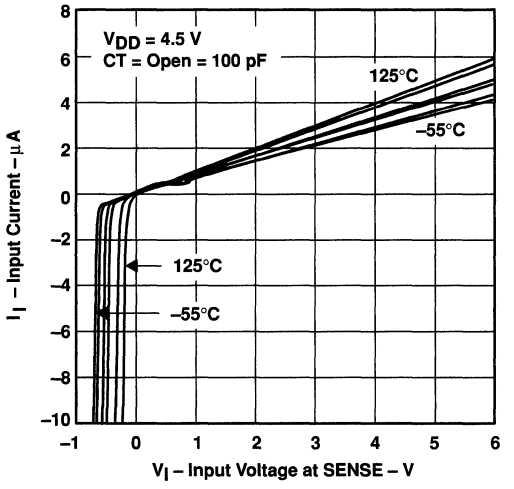


Figure 7

MINIMUM PULSE DURATION AT SENSE
vs
SENSE THRESHOLD OVERDRIVE

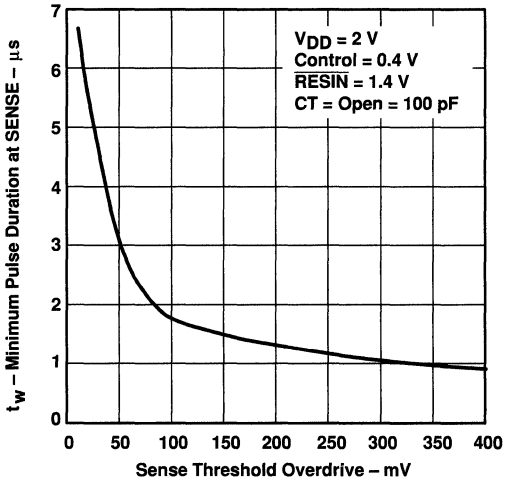


Figure 8

APPLICATION INFORMATION

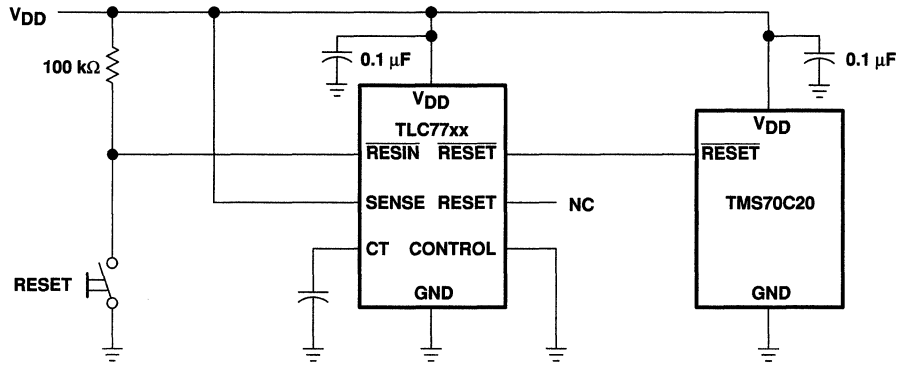


Figure 9. Reset Controller in a Microcomputer System

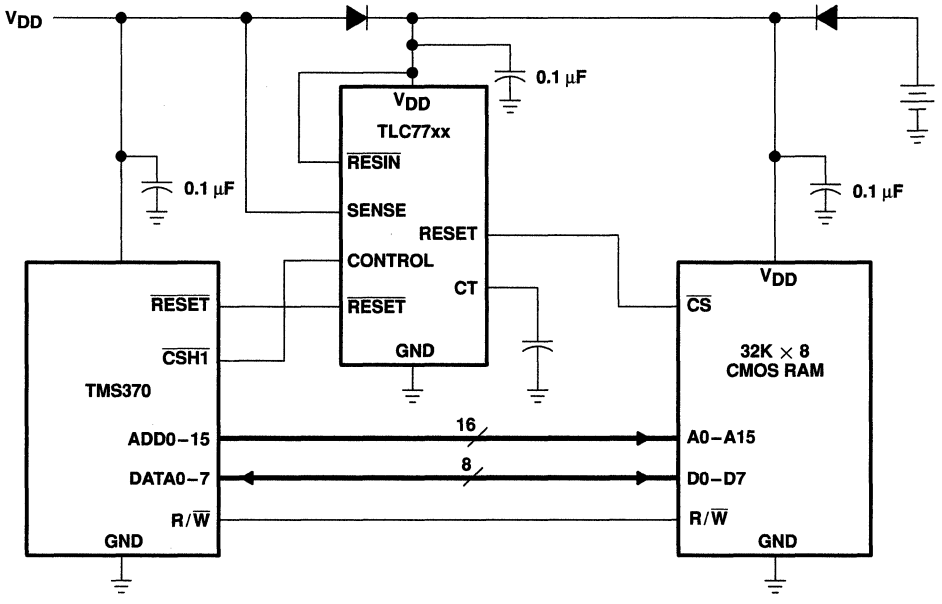


Figure 10. Data Retention During Power Down Using Static CMOS RAMs

features

- Minimum Supply Voltage of 0.75 V
- Supply Voltage Supervision Range:
  - 1.2 V, 1.5 V, 1.8 V (TPS3123, TPS3124, TPS3125)
  - 3 V (TPS3125 Devices only)
- Power-On Reset Generator With Fixed Delay Time of 180 ms
- Manual Reset Input (TPS3123 and TPS3125)
- Watchdog Timer Retriggers the $\overline{\text{RESET}}$ Output at $V_{DD} \geq V_{IT}$
- Supply Current of 14 μA (Typ)
- SOT23–5 Package
- Temperature Range . . . –40°C to 85°C

typical applications

- Applications Using Low Voltage DSPs, Microcontrollers or Microprocessors
- Wireless Communication Systems
- Portable/Battery-Powered Equipment
- Programmable Controls
- Intelligent Instruments
- Industrial Equipment
- Notebook/Desktop Computers
- Automotive Systems

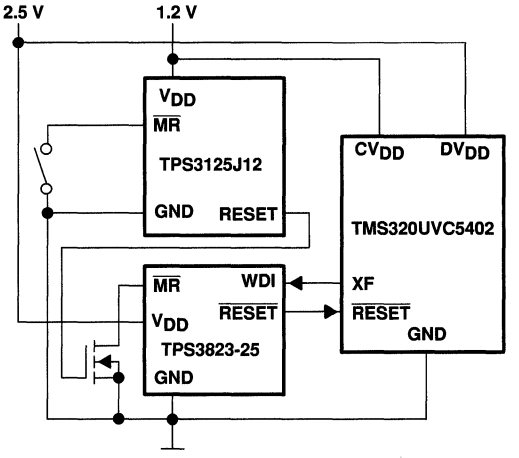
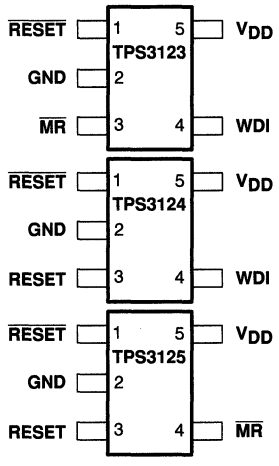


Figure 1. Typical Dual-Voltage DSP Application

DBV PACKAGE
(TOP VIEW)



description

The TPS3123, TPS3124, TPS3125 family of ultra-low voltage processor supervisory circuits provides circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD}) becomes higher than 0.75 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage V_{IT}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_{dtyp} = 180 ms starts after V_{DD} has risen above the threshold voltage V_{IT}.

description (continued)

When the supply voltage drops below the threshold voltage V_{IT}, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage V_{IT} set by an internal voltage divider.

The TPS3123-xx and TPS3125-xx devices incorporate a manual reset input, $\overline{MR}$. A low level at $\overline{MR}$ causes $\overline{RESET}$ to become active. The TPS3124-xx devices do not have the input $\overline{MR}$, but include a high-level output RESET same as the TPS3125-xx devices. In addition the TPS3123-xx and TPS3124-xx have a watchdog timer that need to be triggered periodically by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval t_{tout} = 0.8 s, $\overline{RESET}$ output becomes active for the time period t_d. This event also reinitializes the watchdog timer.

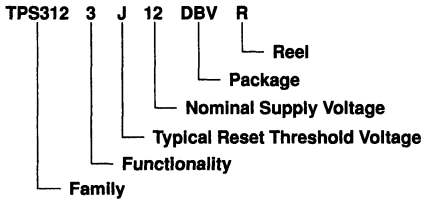
The circuits are available in a 5-pin SOT23-5 package. The TPS3123, TPS3124, TPS3125 devices are characterized for operation over a temperature range of –40°C to 85°C.

PACKAGE INFORMATION STANDARD VERSIONS

T_A	DEVICE NAME		THRESHOLD VOLTAGE	MARKING
–40°C to 85°C	TPS3123J12DBVR†	TPS3123J12DBVT‡	1.08 V	PBNI
	TPS3123G15DBVR†	TPS3123G15DBVT‡	1.40 V	PBOI
	TPS3123J18DBVR†	TPS3123J18DBVT‡	1.62 V	PBPI
	TPS3124J12DBVR†	TPS3124J12DBVT‡	1.08 V	PBQI
	TPS3124G15DBVR†	TPS3124G15DBVT‡	1.40 V	PBRI
	TPS3124J18DBVR†	TPS3124J18DBVT‡	1.62 V	PBSI
	TPS3125J12DBVR†	TPS3125J12DBVT‡	1.08 V	PBTI
	TPS3125G15DBVR†	TPS3125G15DBVT‡	1.40 V	PBUI
	TPS3125J18DBVR†	TPS3125J18DBVT‡	1.62 V	PBVI
	TPS3125L30DBVR†	TPS3125L30DBVT‡	2.64 V	PBXI

† The DBVR passive indicates tape and reel of 3000 parts.
‡ The DBVT passive indicates tape and reel of 250 parts.

ordering information application specific versions



DEVICE NAME	NOMINAL SUPPLY VOLTAGE, V_{NOM}
TPS312xx12DBV	1.2 V
TPS312xx15DBV	1.5 V
TPS312xx18DBV	1.8 V
TPS312xx30DBV	3.0 V

DEVICE NAME	TYPICAL RESET THRESHOLD VOLTAGE–V_{IT-}
TPS312xAxxDBV	V_{NOM}–1%
TPS312xBxxDBV	V_{NOM}–2%
TPS312xCxxDBV	V_{NOM}–3%
TPS312xDxxDBV	V_{NOM}–4%
TPS312xExxDBV	V_{NOM}–5%
TPS312xFxxDBV	V_{NOM}–6%
TPS312xGxxDBV	V_{NOM}–7%
TPS312xHxxDBV	V_{NOM}–8%
TPS312xIxxDBV	V_{NOM}–9%
TPS312xJxxDBV	V_{NOM}–10%
TPS312xKxxDBV	V_{NOM}–11%
TPS312xLxxDBV	V_{NOM}–12%
TPS312xMxxDBV	V_{NOM}–13%
TPS312xNxxDBV	V_{NOM}–14%
TPS312xOxxDBV	V_{NOM}–15%

NOTE: Ten standard versions will be available at product introduction.
For the application specific versions contact the local TI sales office for availability and lead time.

Function Tables

TPS3123

$\overline{MR}$	VDD > V_{IT}	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

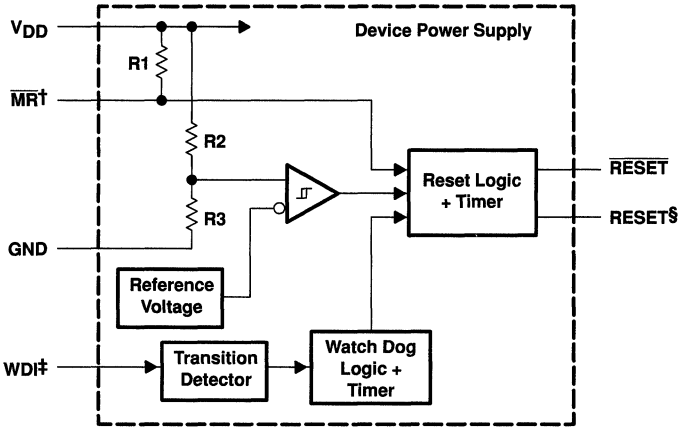
TPS3124

VDD > V_{IT}	$\overline{RESET}$	RESET
0	L	H
1	H	L

TPS3125

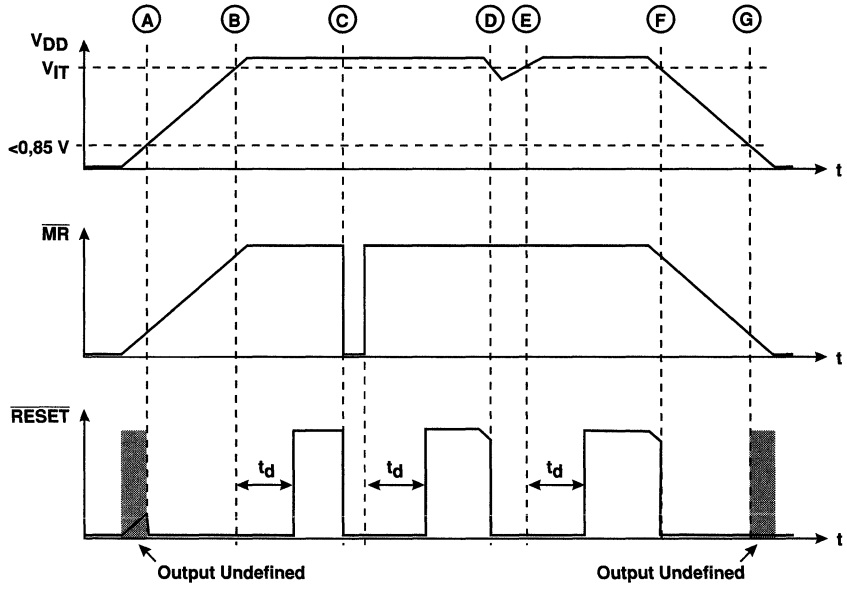
$\overline{MR}$	VDD > V_{IT}	$\overline{RESET}$	RESET
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

functional block diagram

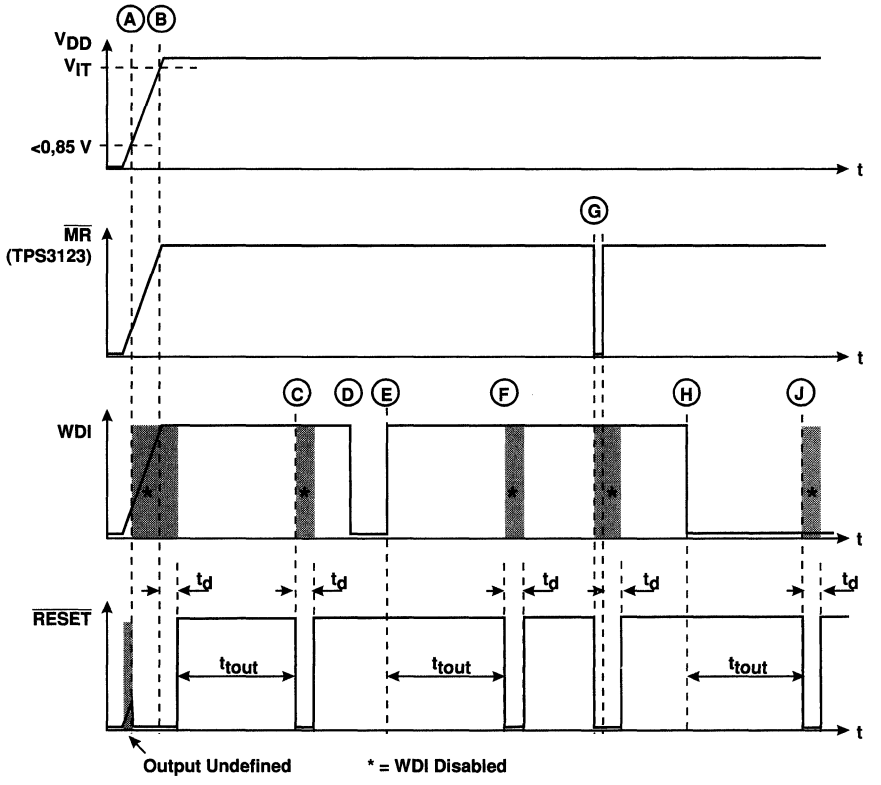


† TPS3123 and TPS3125 Only
‡ TPS3123 and TPS3124 Only
§ TPS3124 and TPS3125 Only

timing diagram TPS3123 and TPS3125



timing diagram TPS3123 and TPS3124



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 3.6 V
All other pins (see Note 1) ..... −0.3 V to 3.6 V
Maximum low output current, I_{OL} ..... 5 mA
Maximum high output current, I_{OH} ..... −5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) ..... ±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±10 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Soldering temperature ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions at specified temperature range

		MIN	MAX	UNIT
Supply voltage, V_{DD}	T_A = 0°C to 85°C	0.75	3.3	V
	T_A = −40°C to 85°C	0.85	3.3	
Input voltage, V_I		0	V_{DD}+0.3	V
High-level input voltage, V_{IH}		0.7×V_{DD}		V
Low-level input voltage, V_{IL}			0.3×V_{DD}	V
Input transition rise and fall rate at WDI, $\Delta t/\Delta V$			1	µs/V
Operating free-air temperature range, T_A		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	$\overline{MR}$ pullup resistor (internal)					27		kΩ
I_{IH}	High-level input current	WDI	WDI = V_{DD} = 3.3 V		–1		1	µA
		$\overline{MR}$	$\overline{MR}$ = 0.7×V_{DD},	V_{DD} = 3.3 V	–20		–55	
I_{IL}	Low-level input current	WDI	WDI = 0 V,	V_{DD} = 3.3 V	–1		1	µA
		$\overline{MR}$	$\overline{MR}$ = 0 V,	V_{DD} = 3.3 V	–80		–170	
V_{OH}	High-level output voltage	$\overline{RESET}$	V_{DD} = 1.5 V,	I_{OH} = –1 mA	0.8×V_{DD}			V
			V_{DD} = 3.3 V,	I_{OH} = –4.5 mA				
		RESET	V_{DD} = 0.75 V,	I_{OH} = –8 µA				
			V_{DD} = 1.5 V,	I_{OH} = –1 mA				
V_{OL}	Low-level output voltage	$\overline{RESET}$	V_{DD} = 0.75 V,	I_{OL} = 15 µA			0.2×V_{DD}	V
			V_{DD} = 1.5 V,	I_{OL} = 1.4 mA				
		RESET	V_{DD} = 1.5 V,	I_{OL} = 1.4 mA				
			V_{DD} = 3.3 V,	I_{OL} = 3 mA			0.4	
V_{IT-}	Negative-going input threshold voltage (see Note 2)	TPS312xJ12	T_A = –40°C to 85°C		1.04	1.08	1.12	V
		TPS312xG15			1.35	1.40	1.45	
		TPS312xJ18			1.56	1.62	1.68	
		TPS312xL30			2.57	2.64	2.71	
V_{hys}	Hysteresis at V_{DD} input		1 V < V_{IT-} < 1.4 V			15		mV
			1.4 V < V_{IT-} <2 V			20		
			2 V < V_{IT-} < 3 V			30		
I_{DD}	Supply current	TPS3123-xx TPS3124-xx	WDI = V_{DD}, $\overline{MR}$ unconnected	V_{DD} = 0.75 V		14		µA
				V_{DD} = 3.3 V		22	30	
		TPS3125-xx (see Note 3)	$\overline{MR}$ unconnected	V_{DD} = 0.75 V		14		
				V_{DD} = 3.3 V		18	25	
C_i	Input capacitance at $\overline{MR}$, WDI		V_I = 0 V to 3.3 V			5		pF

NOTES: 2. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminal.
3. The supply current during delay time t_d is typical 5 µA higher.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	At V_{DD}	$V_{IH} = V_{IT-} + 0.2$ V, $V_{IL} = V_{IT-} - 0{,}2$ V	6			µs
		At $\overline{MR}$	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	1			
		At WDI		0.1			

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{tout}	Watchdog time out		$V_{DD} \geq V_{IT-} + 0.2$ V, See timing diagram	0.8	1.4	2.1	s
t_d	Delay time		$V_{DD} > V_{IT-} + 0.2$ V, See timing diagram	100	180	260	ms
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay (TPS3123/25 only)	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.2 \times V_{DD}$, $V_{IH} = 0.8 \times V_{DD}$			0.1	µs
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{MR}$ to RESET delay (TPS3125 only)				0.1	
t_{PHL}	Propagation delay time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay	$V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V			10	µs
t_{PLH}	Propagation delay time, low-to-high-level output	V_{DD} to RESET delay (TPS3124/25 only)				10	

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

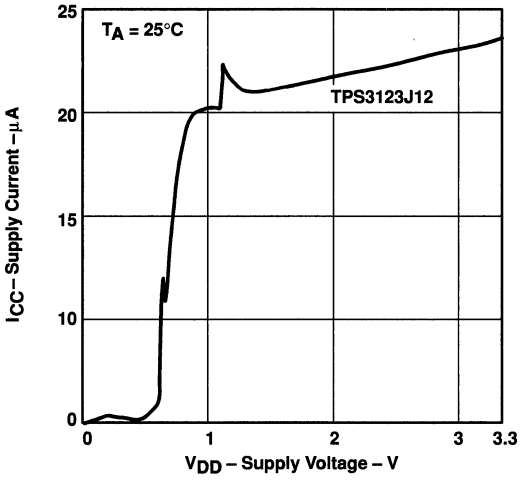


Figure 2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

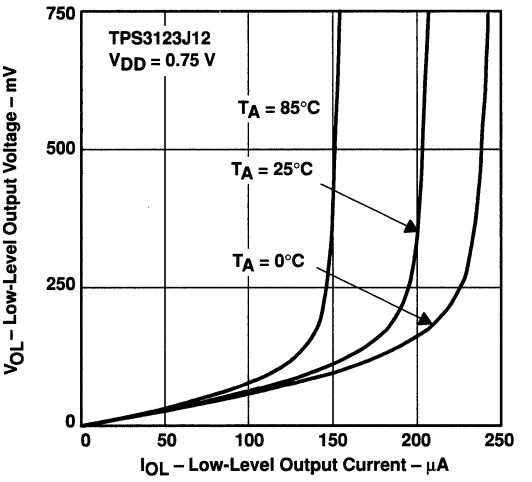


Figure 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

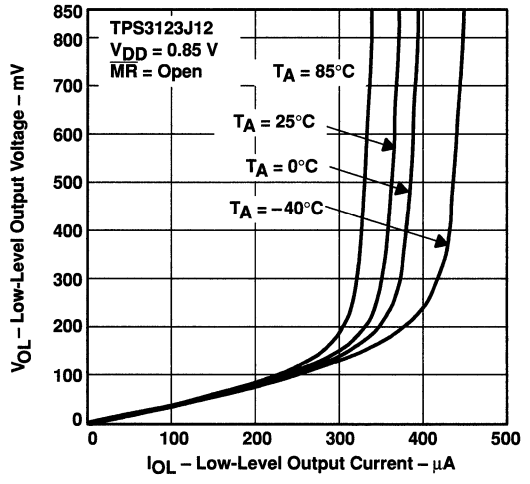


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

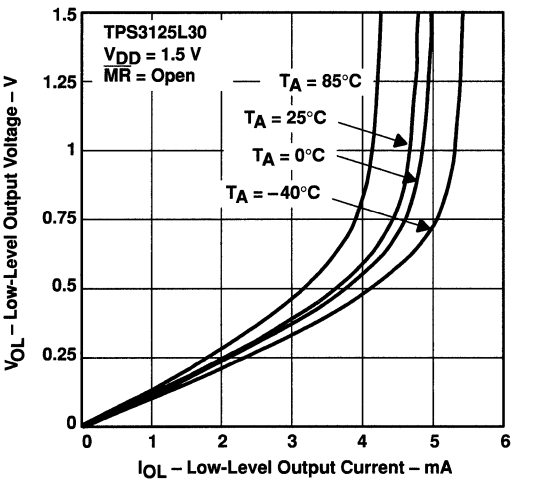


Figure 5

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

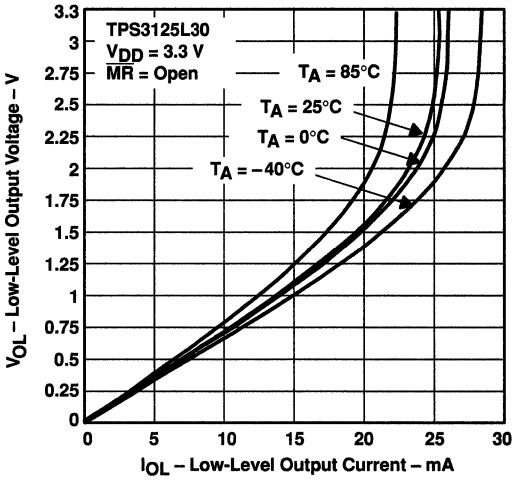


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

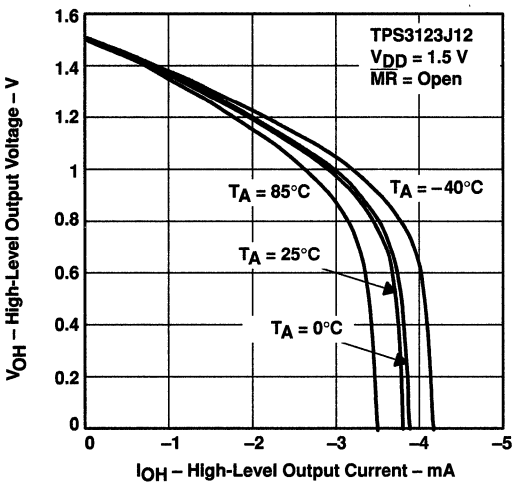


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

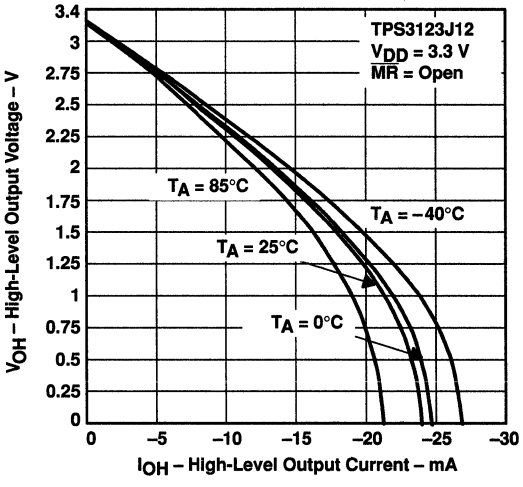


Figure 8

NORMALIZED INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

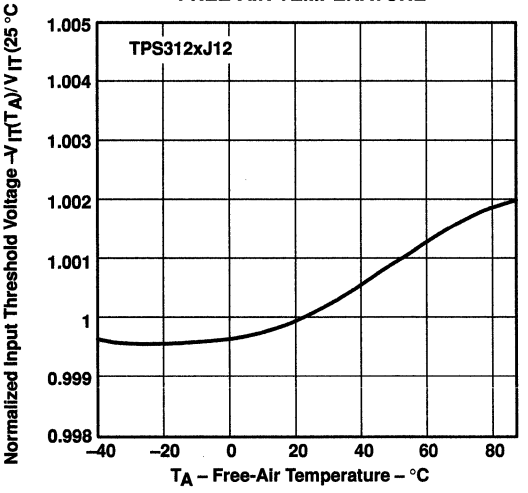


Figure 9

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

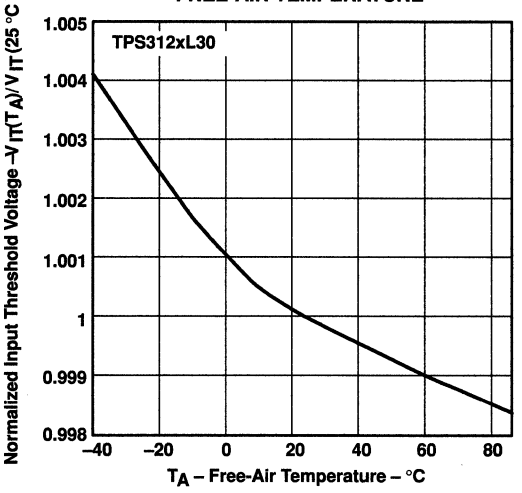


Figure 10

MINIMUM PULSE DURATION
vs
THRESHOLD OVERDRIVE

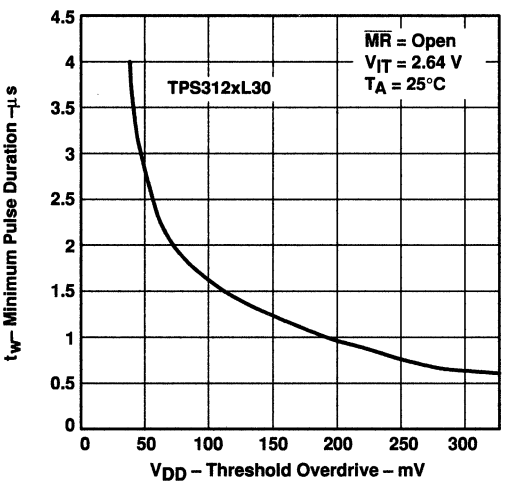


Figure 11

MINIMUM PULSE DURATION
vs
THRESHOLD OVERDRIVE

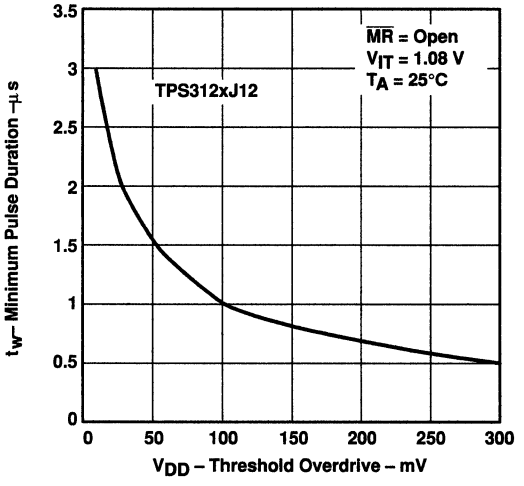
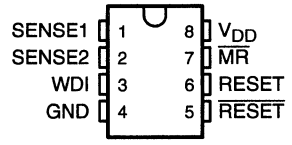


Figure 12

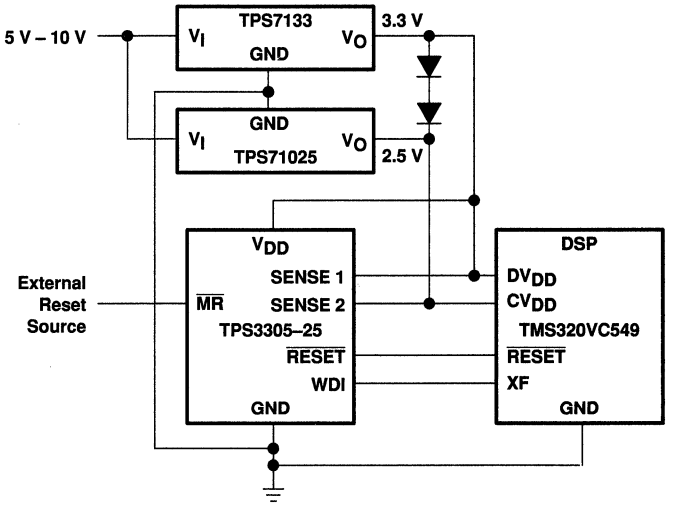
- **Dual Supervisory Circuits for DSP and Processor-Based Systems**
- **Power-On Reset Generator with Fixed Delay Time of 200 ms, no External Capacitor Needed**
- **Watchdog Timer Retriggers the $\overline{\text{RESET}}$ Output at SENSEn ≥ V_{IT+}**
- **Temperature-Compensated Voltage Reference**
- **Maximum Supply Current of 40 μA**
- **Supply Voltage Range . . . 2.7 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output from V_{DD} ≥ 1.1 V**
- **MSOP-8 and SO-8 Packages**
- **Temperature Range . . . – 40°C to 85°C**

D OR DGN PACKAGE
(TOP VIEW)



typical applications

Figure 1 lists some of the typical applications for the TPS3305 family, and a schematic diagram for a DSP-based system application. This application uses TI part numbers TPS3305–25, TPS7133, TPS71025, and TMS320VC549.



- **Applications using DSPs, Microcontrollers or Microprocessors**
- **Industrial Equipment**
- **Programmable Controls**
- **Automotive Systems**
- **Portable/Battery Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communication Systems**
- **Notebook/Desktop Computers**

Figure 1. Applications Using the TPS3305 Family

description

The TPS3305 family is a series of micropower supply voltage supervisors designed for circuit initialization, primarily in DSP and processor-based systems, which require two supply voltages.

The product spectrum of the TPS3305 is designed for monitoring two independent supply voltages of 3.3 V/1.8 V, 3.3 V/2.5 V or 3.3 V /5 V.

description (continued)

The various supply voltage supervisors are designed to monitor the nominal supply voltage, as shown in the following supply voltage monitoring table.

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE		THRESHOLD VOLTAGE (TYP)	
	SENSE1	SENSE2	SENSE1	SENSE2
TPS3305-18	3.3 V	1.8 V	2.93 V	1.68 V
TPS3305-25	3.3 V	2.5 V	2.93 V	2.25 V
TPS3305-33	5 V	3.3 V	4.55 V	2.93 V

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors the SENSEn inputs and keeps $\overline{\text{RESET}}$ active as long as SENSEn remains below the threshold voltage V_{IT+}.

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d\,typ}$ = 200 ms, starts after SENSE1 and SENSE2 inputs have risen above the threshold voltage V_{IT+}. When the voltage at SENSE1 or SENSE2 input drops below the threshold voltage V_{IT-}, the $\overline{\text{RESET}}$ output becomes active (low) again.

The TPS3305-xx devices integrate a watchdog timer that is periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $t_{t(out)}$ = 1.6 s, $\overline{\text{RESET}}$ becomes active for the time period t_d . This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3305-xx family of devices incorporates a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. In addition to the active-low $\overline{\text{RESET}}$ output, the TPS3305-xx family includes an active-high RESET output.

The TPS3305-xx devices are available in either 8-pin MSOP or standard 8-pin SO packages.

The TPS3305-xx family is characterized for operation over a temperature range of – 40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
	SMALL OUTLINE (D)	PowerPAD™ μ-SMALL OUTLINE (DGN)		
–40°C to 85°C	TPS3305-18D	TPS3305-18DGN	TIAAM	TPS3305-18Y
	TPS3305-25D	TPS3305-25DGN	TIAAN	TPS3305-25Y
	TPS3305-33D	TPS3305-33DGN	TIAAO	TPS3305-33Y

description (continued)

FUNCTION/TRUTH TABLES

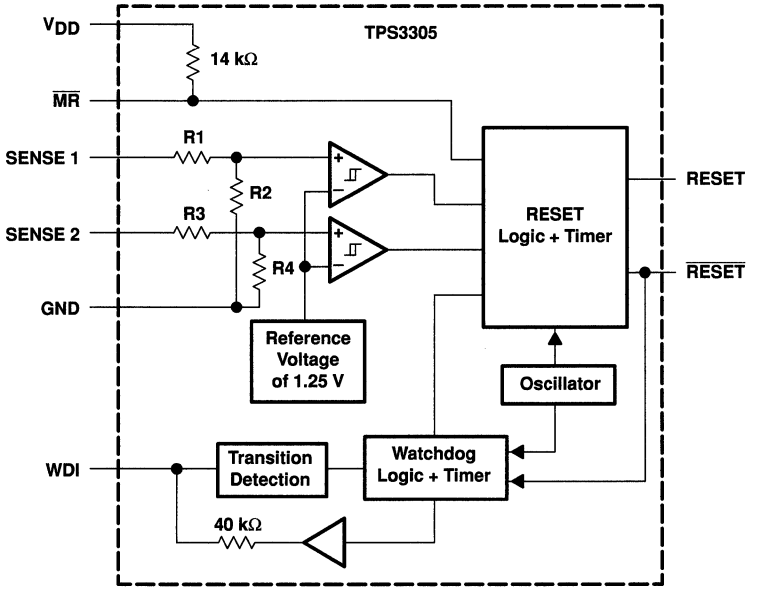
$\overline{\text{MR}}$	SENSE1>V_{IT1}	SENSE2>V_{IT2}	$\overline{\text{RESET}}$	RESET
L	X†	X†	L	H
H	0	0	L	H
H	0	0	L	H
H	0	1	L	H
H	0	1	L	H
H	1	0	L	H

PowerPAD is a trademark of Texas Instruments Incorporated.

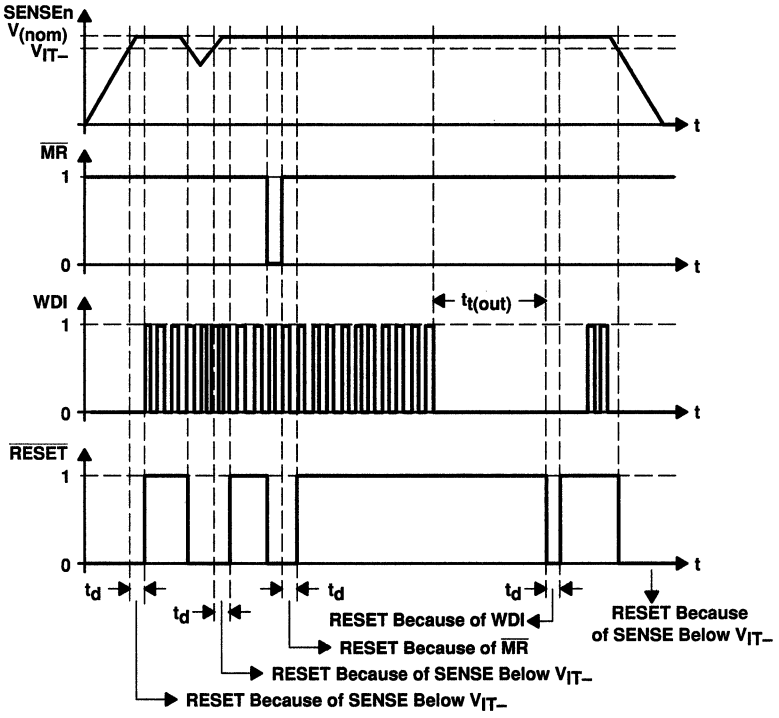
H	1	0	L	H
H	1	1	L	H
H	1	1	H	L

† X = Don't care

functional block diagram

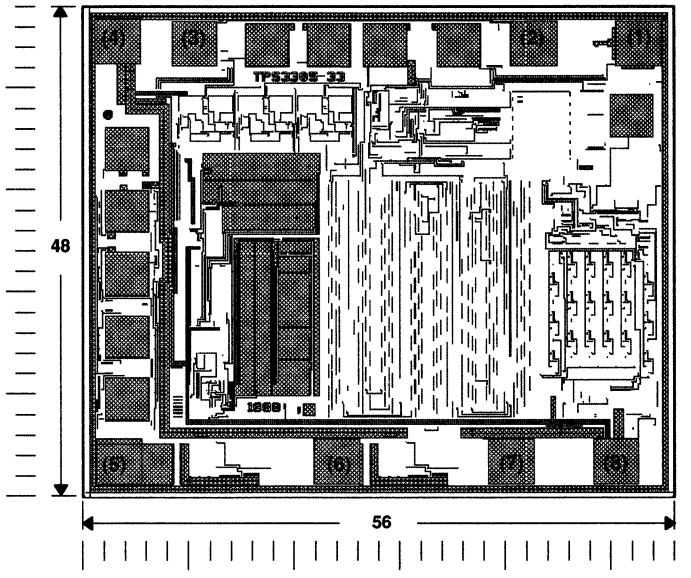


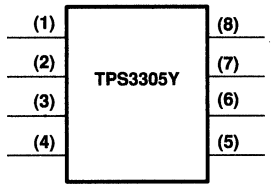
timing diagram



TPS3305Y chip information

These chips, when properly assembled, display characteristics similar to those of the TPS3305. Thermal compression or ultrasonic bonding may take place on the doped aluminium bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.





CHIP THICKNESS: 10 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{MR}$	7	I	Manual reset
$\overline{RESET}$	5	O	Active-low reset output
RESET	6	O	Active-high reset output
SENSE1	1	I	Sense voltage input 1
SENSE2	2	I	Sense voltage input 2
WDI	3	I	Watchdog timer input
V_{DD}	8		Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1) ..... 7 V
All other pins (see Note 1) ..... – 0.3 V to 7 V
Maximum low output current, I_{OL} ..... 5 mA
Maximum high output current, I_{OH} ..... – 5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±20 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... –40°C to 85°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Soldering temperature ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000 h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN	2.14 mW	17.1 mW/°C	1.37 mW	1.11 mW
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.7	6	V
Input voltage at $\overline{MR}$ and WDI, V_I	0	V_{DD}+0.3	V
Input voltage at SENSE1 and SENSE2, V_I	0	(V_{DD}+0.3)V_{IT}/1.25V	V
High-level input voltage at $\overline{MR}$ and WDI, V_{IH}	0.7xV_{DD}		V
Low-level input voltage at $\overline{MR}$ and WDI, V_{IL}		0.3xV_{DD}	V
Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$		50	ns/V
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 2.7 V to 6 V, I_{OH} = –20 µA	V_{DD}– 0.2V			V
			V_{DD} = 3.3 V, I_{OH} = –2 mA	V_{DD}– 0.4V			
			V_{DD} = 6 V, I_{OH} = –3 mA	V_{DD}– 0.4V			
V_{OL}	Low-level output voltage		V_{DD} = 2.7 V to 6 V, I_{OL} = 20 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 3 mA			0.4	
	Power-up reset voltage (see Note 2)		V_{DD} ≥ 1.1 V, I_{OL} = 20 µA			0.4	V
V_{IT-}	Negative-going input threshold voltage (see Note 3)	VSENSE1, VSENSE2	V_{DD} = 2.7 V to 6 V, T_A = 0°C to 85°C	1.64	1.68	1.72	V
				2.20	2.25	2.30	
				2.86	2.93	3	
				4.46	4.55	4.64	
		VSENSE1, VSENSE2	V_{DD} = 2.7 V to 6 V, T_A =–40°C to 85°C	1.64	1.68	1.73	V
				2.20	2.25	2.32	
				2.86	2.93	3.02	
				4.46	4.55	4.67	
V_{hys}	Hysteresis at VSENSEn input		V_{IT-} = 1.68 V		15		mV
			V_{IT-} = 2.25 V		20		
			V_{IT-} = 2.93 V		30		
			V_{IT-} = 4.55 V		40		
$I_{H(AV)}$	Average high-level input current	WDI	WDI = V_{DD} = 6 V Time average (dc = 88%)		100	150	µA
$I_{L(AV)}$	Average low-level input current		WDI = 0 V, V_{DD} = 6 V, Time average (dc = 12%)		–15	–20	
I_H	High-level input current	WDI	WDI = V_{DD} = 6 V,		120	170	µA
		$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V		–130	–180	
		SENSE1	VSENSE1 = V_{DD} = 6 V		5	8	
		SENSE2	VSENSE2 = V_{DD} = 6 V		6	9	
I_L	Low-level input current	WDI	WDI = 0 V, V_{DD}, = 6 V		–120	–170	µA
		$\overline{MR}$	$\overline{MR}$ = 0V, V_{DD} = 6 V		–430	–600	
		SENSEn	VSENSE1,2 = 0 V	–1		1	
I_{DD}	Supply current					40	µA
C_i	Input capacitance		V_I = 0 V to V_{DD}		10		pF

NOTES: 2. The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥ 15 µs/V.
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 µF) should be placed close to the supply terminals.

timing requirements at V_{DD} = 2.7 V to 6 V, R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	SENSEn	$V_{SENSEnL} = V_{IT-} - 0.2$ V, $V_{SENSEnH} = V_{IT+} + 0.2$ V	6			µs
		$\overline{MR}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns
		WDI		100			ns

switching characteristics at V_{DD} = 2.7 V to 6 V, R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time out		$V_{I(SENSEn)} \geq V_{IT+} + 0.2$ V, $\overline{MR} \geq 0.7 \times V_{DD}$, See timing diagram	1.1	1.6	2.3	s
t_d	Delay time		$V_{I(SENSEn)} \geq V_{IT+} + 0.2$ V, $\overline{MR} \geq 0.7 \times V_{DD}$, See timing diagram	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	$\overline{MR}$ to $\overline{RESET}$, $\overline{MR}$ to RESET	$V_{I(SENSEn)} \geq V_{IT+} + 0.2$ V, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
t_{PLH}	Propagation (delay) time, low-to-high level output	$\overline{MR}$ to $\overline{RESET}$, $\overline{MR}$ to RESET					
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to $\overline{RESET}$, SENSEn to RESET	$V_{IH} = V_{IT+} + 0.2$ V, $V_{IL} = V_{IT-} - 0.2$ V, $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	µs
t_{PLH}	Propagation (delay) time, low-to-high level output	SENSEn to $\overline{RESET}$, SENSEn to RESET					

TYPICAL CHARACTERISTICS

NORMALIZED SENSE THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE AT V_{DD}

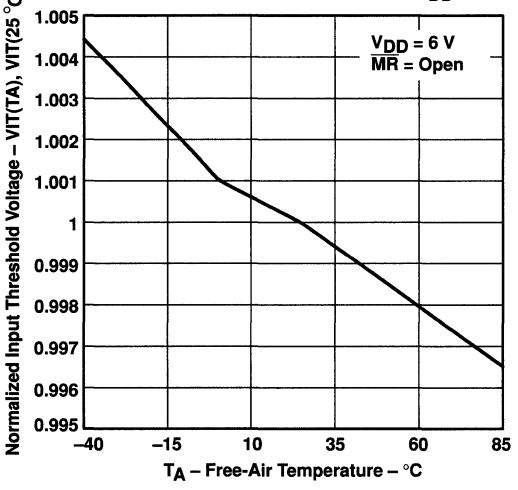


Figure 2

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

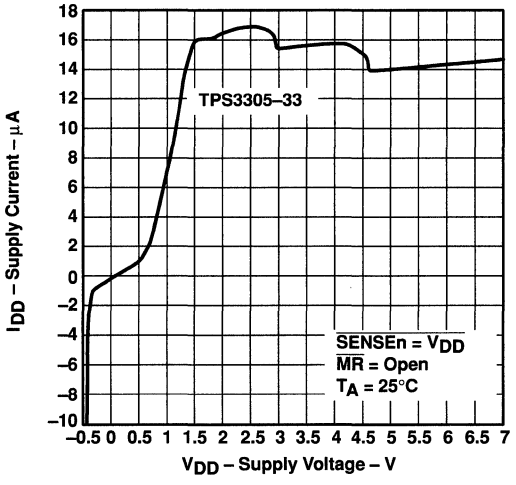


Figure 3

INPUT CURRENT
vs
INPUT VOLTAGE AT $\overline{MR}$

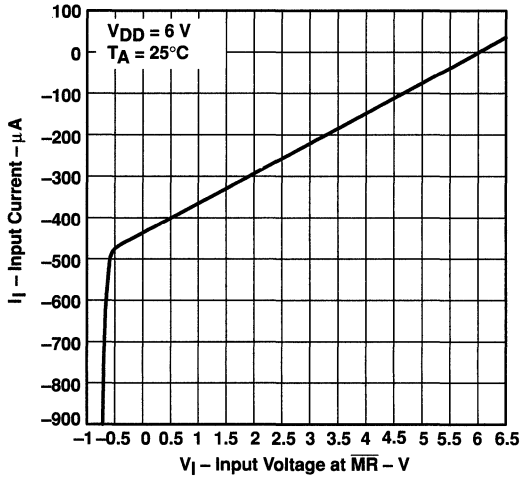


Figure 4

MINIMUM PULSE DURATION AT SENSE
vs
THRESHOLD OVERDRIVE

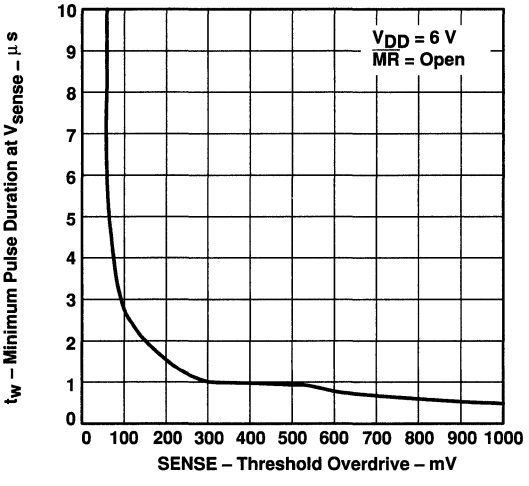


Figure 5

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

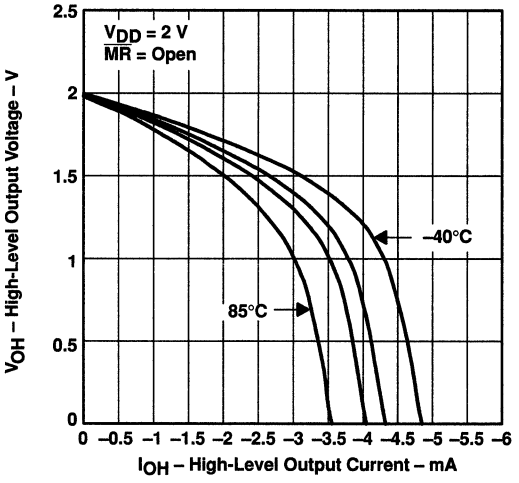


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

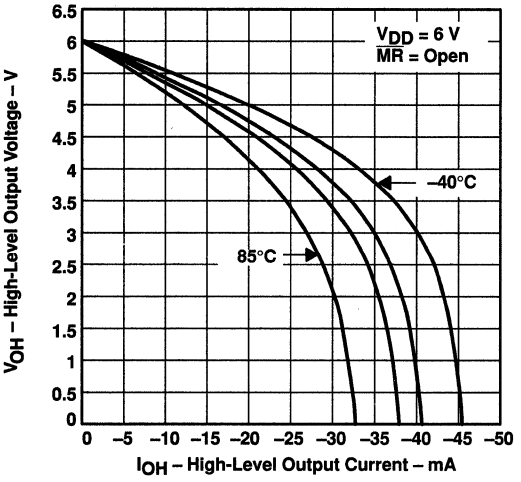


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

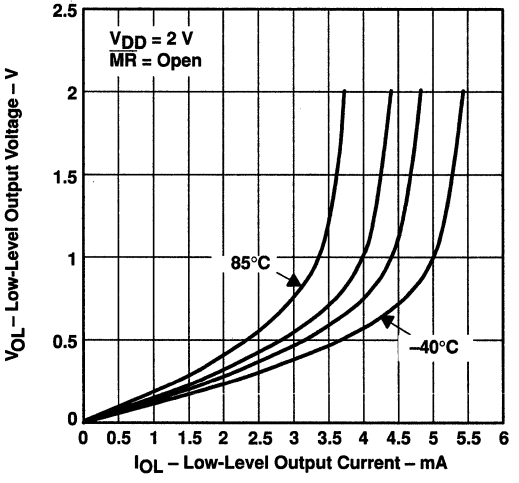


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

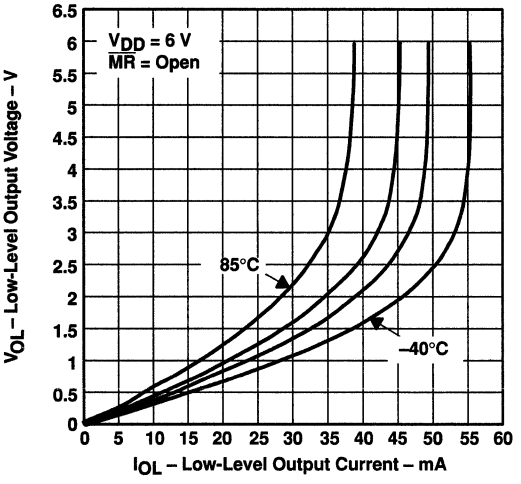
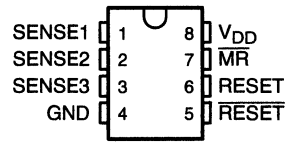


Figure 9

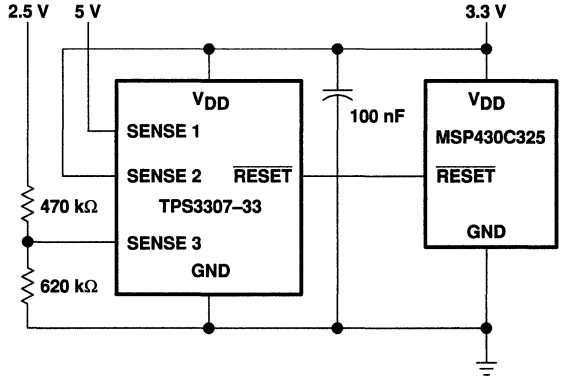
- **Triple Supervisory Circuits for DSP and Processor-Based Systems**
- **Power-On Reset Generator with Fixed Delay Time of 200 ms, No External Capacitor Needed**
- **Temperature-Compensated Voltage Reference**
- **Maximum Supply Current of 40 μA**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{DD} \geq 1.1$ V**
- **MSOP-8 and SO-8 Packages**
- **Temperature Range . . . – 40°C to 85°C**

D OR DGN PACKAGE
(TOP VIEW)



typical applications

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses TI part numbers TPS3307–33 and MSP430C325.



- **Applications using DSPs, Microcontrollers or Microprocessors**
- **Industrial Equipment**
- **Programmable Controls**
- **Automotive Systems**
- **Portable/Battery Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communication Systems**
- **Notebook/Desktop Computers**

Figure 1. Applications Using the TPS3307 Family

description

The TPS3307 family is a series of micropower supply voltage supervisors designed for circuit initialization primarily in DSP and processor-based systems, which require more than one supply voltage.

The product spectrum of the TPS3307-xx is designed for monitoring three independent supply voltages: 3.3 V/1.8 V/adj, 3.3 V/2.5 V/adj or 3.3 V/5 V/adj. The adjustable SENSE input allows the monitoring of any supply voltage >1.25 V.

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following supply voltage monitoring table.

description (continued)

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE			THRESHOLD VOLTAGE (TYP)		
	SENSE1	SENSE2	SENSE3	SENSE1	SENSE2	SENSE3
TPS3307-18	3.3 V	1.8 V	User defined	2.93 V	1.68 V	1.25 V†
TPS3307-25	3.3 V	2.5 V	User defined	2.93 V	2.25 V	1.25 V†
TPS3307-33	5 V	3.3 V	User defined	4.55 V	2.93 V	1.25 V†

† The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors the SENSEn inputs and keeps $\overline{\text{RESET}}$ active as long as SENSEn remain below the threshold voltage V_{IT+}.

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d\,typ}$ = 200 ms, starts after all SENSEn inputs have risen above the threshold voltage V_{IT+}. When the voltage at any SENSE input drops below the threshold voltage V_{IT-}, the $\overline{\text{RESET}}$ output becomes active (low) again.

The TPS3307-xx family of devices incorporates a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. In addition to the active-low $\overline{\text{RESET}}$ output, the TPS3307-xx family includes an active-high RESET output.

The devices are available in either 8-pin MSOP or standard 8-pin SO packages.

The TPS3307-xx devices are characterized for operation over a temperature range of – 40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
	SMALL OUTLINE (D)	PowerPAD™ μ-SMALL OUTLINE (DGN)		
–40°C to 85°C	TPS3307-18D	TPS3307-18DGN	TIAAP	TPS3307-18Y
	TPS3307-25D	TPS3307-25DGN	TIAAQ	TPS3307-25Y
	TPS3307-33D	TPS3307-33DGN	TIAAR	TPS3307-33Y

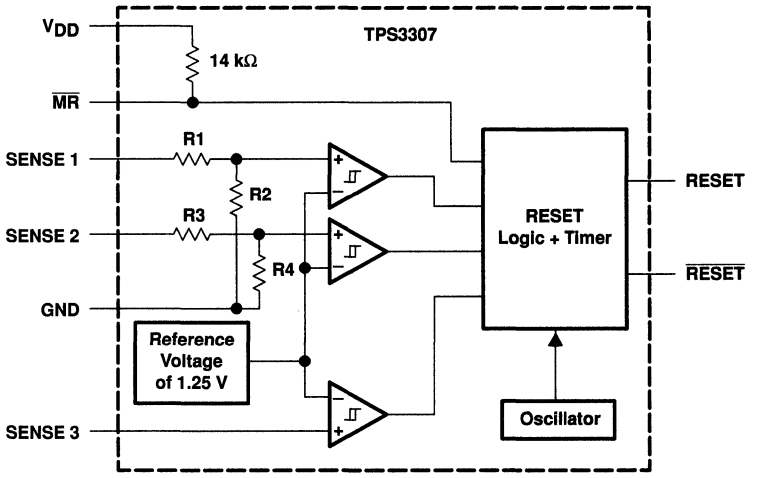
FUNCTION/TRUTH TABLES

$\overline{\text{MR}}$	SENSE1>V_{IT1}	SENSE2>V_{IT2}	SENSE3>V_{IT3}	$\overline{\text{RESET}}$	RESET
L	X†	X†	X	L	H
H	0	0	0	L	H
H	0	0	1	L	H
H	0	1	0	L	H
H	0	1	1	L	H
H	1	0	0	L	H
H	1	0	1	L	H
H	1	1	0	L	H
H	1	1	1	H	L

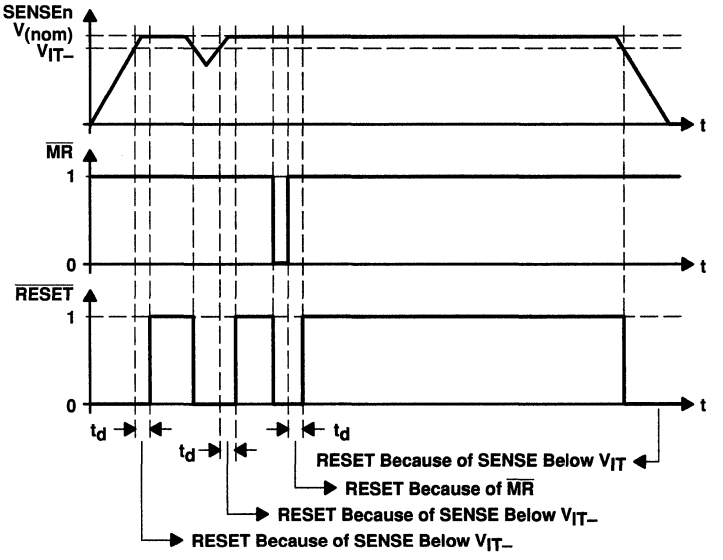
† X = Don't care

PowerPAD is a trademark of Texas Instruments Incorporated.

functional block diagram

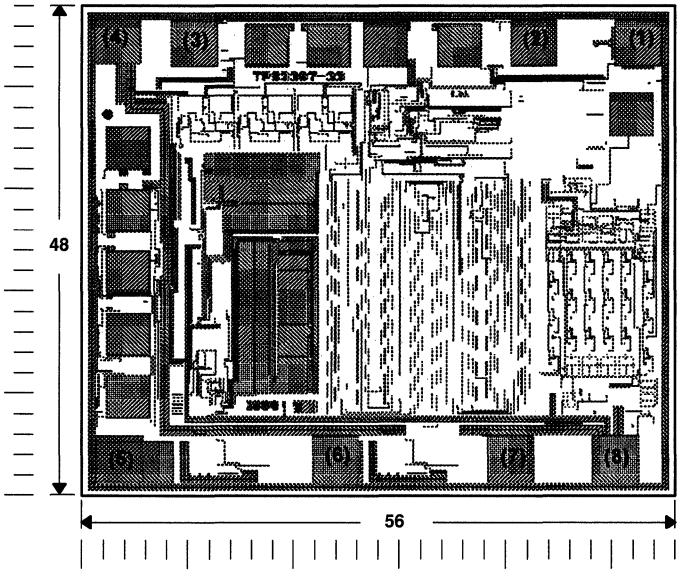


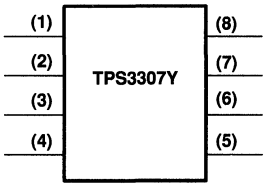
timing diagram



TPS3307Y chip information

These chips, when properly assembled, display characteristics similar to those of the TPS3307. Thermal compression or ultrasonic bonding may take place on the doped aluminium bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.





CHIP THICKNESS: 10 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{MR}$	7	I	Manual reset
$\overline{RESET}$	5	O	Active-low reset output
RESET	6	O	Active-high reset output
SENSE1	1	I	Sense voltage input 1
SENSE2	2	I	Sense voltage input 2
SENSE3	3	I	Sense voltage input 3
V_{DD}	8		Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1) ..... 7 V
All other pins (see Note 1) ..... –0.3 V to 7 V
Maximum low output current, I_{OL} ..... 5 mA
Maximum high output current, I_{OH} ..... –5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±20 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... –40°C to 85°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Soldering temperature ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000 h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN	2.14 mW	17.1 mW/°C	1.37 mW	1.11 mW
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage at $\overline{MR}$ and SENSE3, V_I	0	$V_{DD}+0.3$	V
Input voltage at SENSE1 and SENSE2, V_I	0	$(V_{DD}+0.3)V_{IT}/1.25V$	V
High-level input voltage at $\overline{MR}$, V_{IH}	$0.7xV_{DD}$		V
Low-level input voltage at $\overline{MR}$, V_{IL}		$0.3xV_{DD}$	V
Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$		50	ns/V
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 2 V to 6 V, I_{OH} = –20 µA	V_{DD}– 0.2V			V
			V_{DD} = 3.3 V, I_{OH} = –2 mA	V_{DD}– 0.4V			
			V_{DD} = 6 V, I_{OH} = –3 mA	V_{DD}– 0.4V			
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V, I_{OL} = 20 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 3 mA			0.4	
	Power-up reset voltage (see Note 2)		V_{DD} ≥ 1.1 V, I_{OL} = 20 µA			0.4	V
V_{IT-}	Negative-going input threshold voltage (see Note 3)	VSENSE3	V_{DD} = 2 V to 6 V, T_A = 0°C to 85°C	1.22	1.25	1.28	V
		VSENSE1, VSENSE2		1.64	1.68	1.72	
				2.20	2.25	2.30	
				2.86	2.93	3	
				4.46	4.55	4.64	
		VSENSE3	V_{DD} = 2 V to 6 V, T_A = –40°C to 85°C	1.22	1.25	1.29	V
		VSENSE1, VSENSE2		1.64	1.68	1.73	V
				2.20	2.25	2.32	
				2.86	2.93	3.02	
				4.46	4.55	4.67	
V_{hys}	Hysteresis at VSENSEn input		V_{IT-} = 1.25 V		10		mV
			V_{IT-} = 1.68 V		15		
			V_{IT-} = 2.25 V		20		
			V_{IT-} = 2.93 V		30		
			V_{IT-} = 4.55 V		40		
I_H	High-level input current	$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V		–130	–180	µA
		SENSE1	VSENSE1 = V_{DD} = 6 V		5	8	
		SENSE2	VSENSE2 = V_{DD} = 6 V		6	9	
		SENSE3	VSENSE3 = V_{DD}	–1		1	
I_L	Low-level input current	$\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 6 V		–430	–600	µA
		SENSEn	VSENSE1,2,3 = 0 V	–1		1	
I_{DD}	Supply current					40	µA
C_i	Input capacitance		V_I = 0 V to V_{DD}		10		pF

NOTES: 2. The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥ 15 µs/V
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 µF) should be placed close to the supply terminals.

timing requirements at V_{DD} = 2 V to 6 V, R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	SENSEn	$V_{SENSEnL} = V_{IT-} - 0.2$ V, $V_{SENSEnH} = V_{IT+} + 0.2$ V	6			µs
		$\overline{MR}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns

switching characteristics at V_{DD} = 2 V to 6 V, R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{I(SENSEn)} \geq V_{IT+} + 0.2$ V, $\overline{MR} \geq 0.7 \times V_{DD}$, See timing diagram	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	$\overline{MR}$ to $\overline{RESET}$	$V_{I(SENSEn)} \geq V_{IT+} + 0.2$ V, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
		$\overline{MR}$ to RESET					
t_{PLH}	Propagation (delay) time, low-to-high level output	$\overline{MR}$ to $\overline{RESET}$					
		$\overline{MR}$ to RESET					
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to $\overline{RESET}$	$V_{IH} = V_{IT+} + 0.2$ V, $V_{IL} = V_{IT-} - 0.2$ V, $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	µs
		SENSEn to RESET					
t_{PLH}	Propagation (delay) time, low-to-high level output	SENSEn to $\overline{RESET}$					
		SENSEn to RESET					

TYPICAL CHARACTERISTICS

NORMALIZED SENSE THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE AT V_{DD}

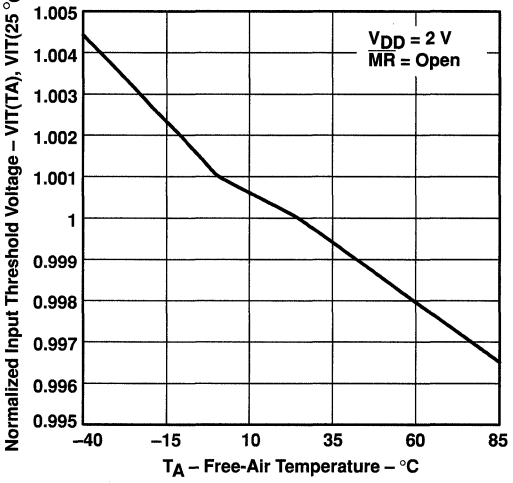


Figure 2

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

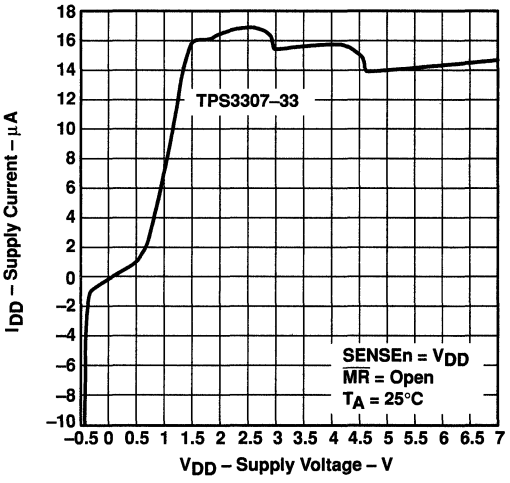


Figure 3

INPUT CURRENT
vs
INPUT VOLTAGE AT $\overline{MR}$

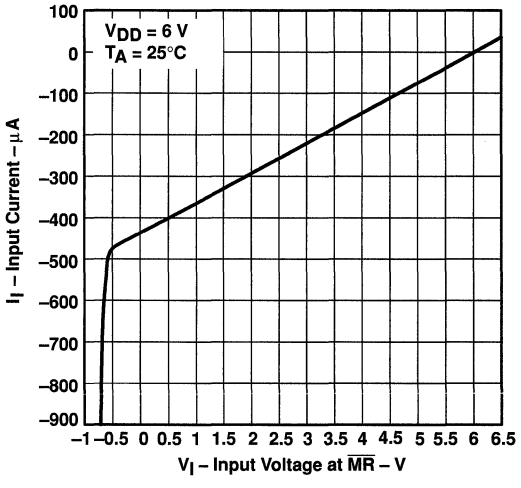


Figure 4

MINIMUM PULSE DURATION AT SENSE
vs
THRESHOLD OVERDRIVE

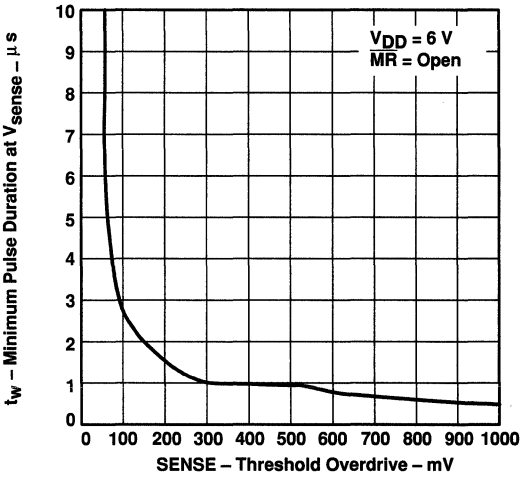


Figure 5

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

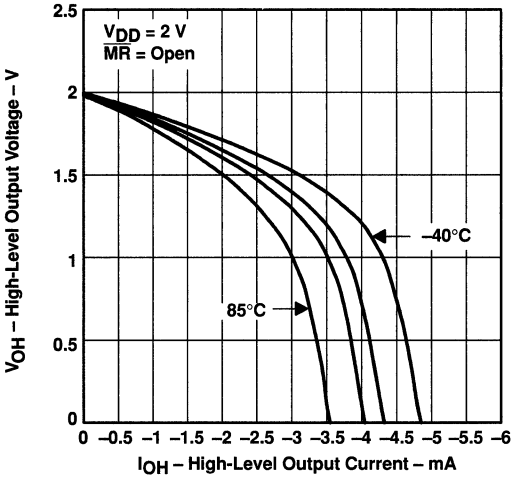


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

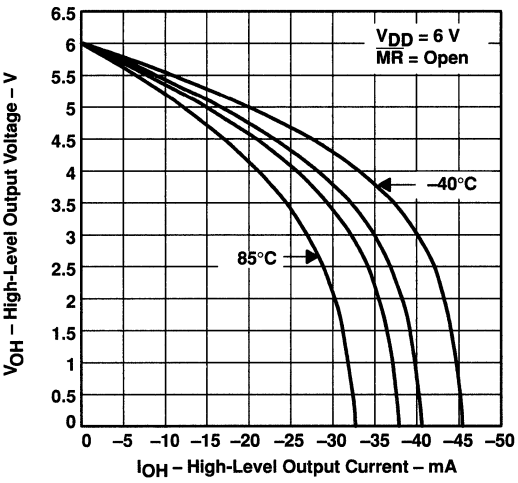


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

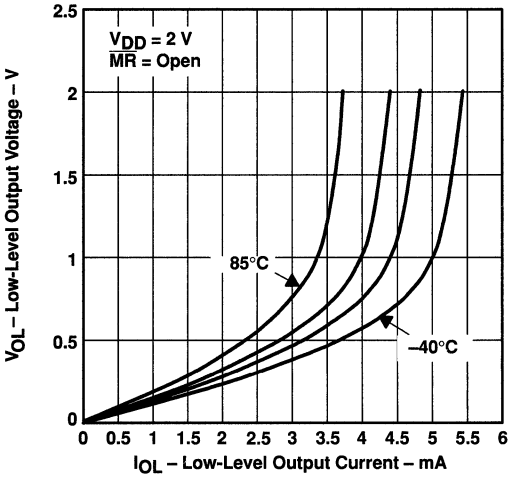


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

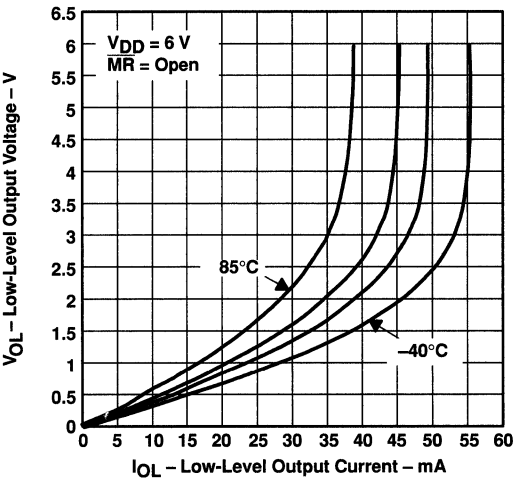


Figure 9

features

- Power-On Reset Generator with Fixed Delay Time of 200 ms, no External Capacitor Needed
- Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, and 5 V
- Pin-For-Pin Compatible with the MAX705 through MAX708 Series
- Integrated Watchdog Timer (TPS3705 only)
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Maximum Supply Current of 50 μA
- MSOP-8 and SO-8 Packages
- Temperature Range . . . –40°C to 85°C

typical applications

- Designs Using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable/Battery Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook/Desktop Computers

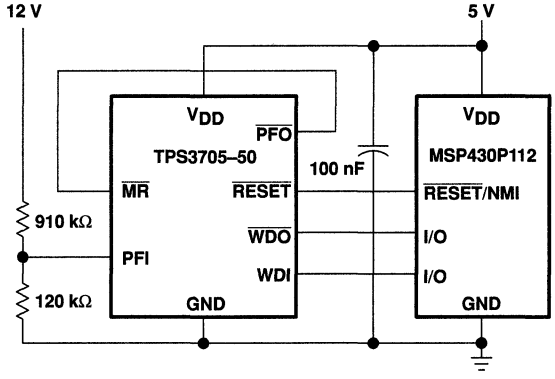
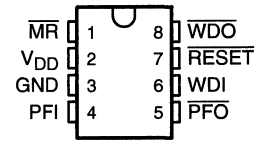
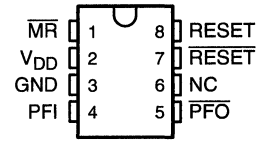


Figure 1. Typical MSP430 Application

TPS3705 . . . D PACKAGE
(TOP VIEW)

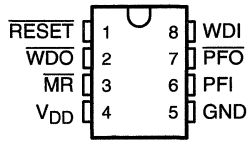


TPS3707 . . . D PACKAGE
(TOP VIEW)

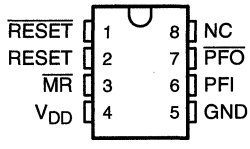


NC – No internal connection

TPS3705 . . . DGN PACKAGE
(TOP VIEW)



TPS3707 . . . DGN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS3705, TPS3707 family of microprocessor supply-voltage supervisors provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage V_{IT+}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d\,typ}$ = 200 ms, starts after V_{DD} has risen above the threshold voltage V_{IT+}. When the supply voltage drops below the threshold voltage V_{IT-}, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage V_{IT-} set by an internal voltage divider.

The TPS3705-xx and TPS3707-xx devices incorporate a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active.

The TPS370x-xx families integrate a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

The TPS3705-xx devices have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $t_{t(out)}$ = 1.6 s, $\overline{\text{WDO}}$ becomes active. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3707-xx devices do not have the Watchdog function, but include a high-level output RESET.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in either 8-pin MSOP or standard SOIC packages. The TPS3705, TPS3707 devices are characterized for operation over a temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	THRESHOLD VOLTAGE	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
		SMALL OUTLINE (D)	POWER–PAD™ μ-SMALL OUTLINE (DGN)		
–40°C to 85°C	2.63 V	TPS3705–30D	TPS3705–30DGN	TIAAT	TPS3705-30Y
	2.93 V	TPS3705–33D	TPS3705–33DGN	TIAAU	TPS3705–33Y
	4.55 V	TPS3705–50D	TPS3705–50DGN	TIAAV	TPS3705–50Y
	2.25 V	TPS3707–25D	TPS3707–25DGN	TIAAW	TPS3707–25Y
	2.63 V	TPS3707–30D	TPS3707–30DGN	TIAAX	TPS3707–30Y
	2.93 V	TPS3707–33D	TPS3707–33DGN	TIAAY	TPS3707–33Y
	4.55 V	TPS3707–50D	TPS3707–50DGN	TIAAZ	TPS3707–50Y

Function Tables

TRUTH TABLE, TPS3705

$\overline{MR}$	$V_{DD}>V_{IT}$	$\overline{RESET}$	TYPICAL DELAY
H→L	1	H→L	30 ns
L→H	1	L→H	200 ms
H	1→0	H→L	3 µs
H	0→1	L→H	200 ms

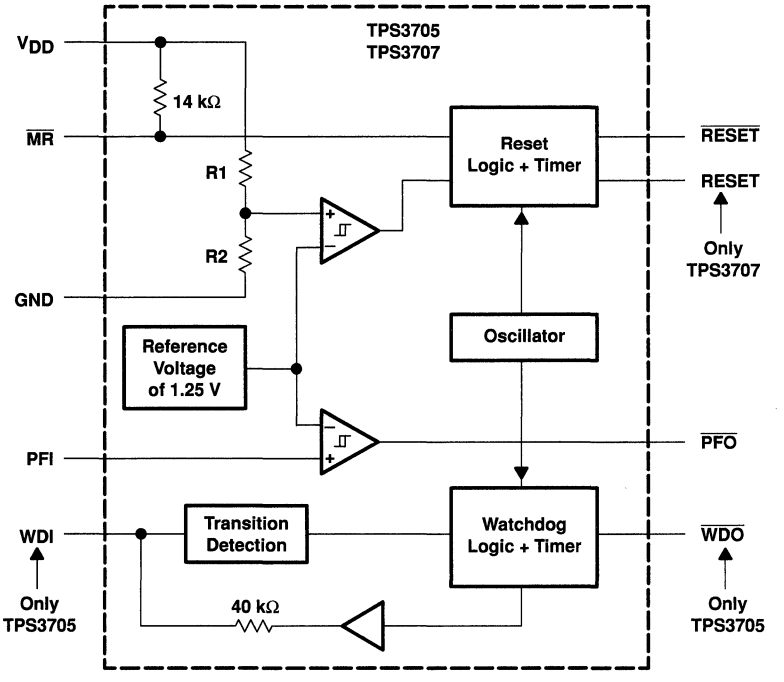
TRUTH TABLE, TPS3707

$\overline{MR}$	$V_{DD}>V_{IT}$	$\overline{RESET}$	RESET	TYPICAL DELAY
H→L	1	H→L	L→H	30 ns
L→H	1	L→H	H→L	200 ms
H	1→0	H→L	L→H	3 µs
H	0→1	L→H	H→L	200 ms

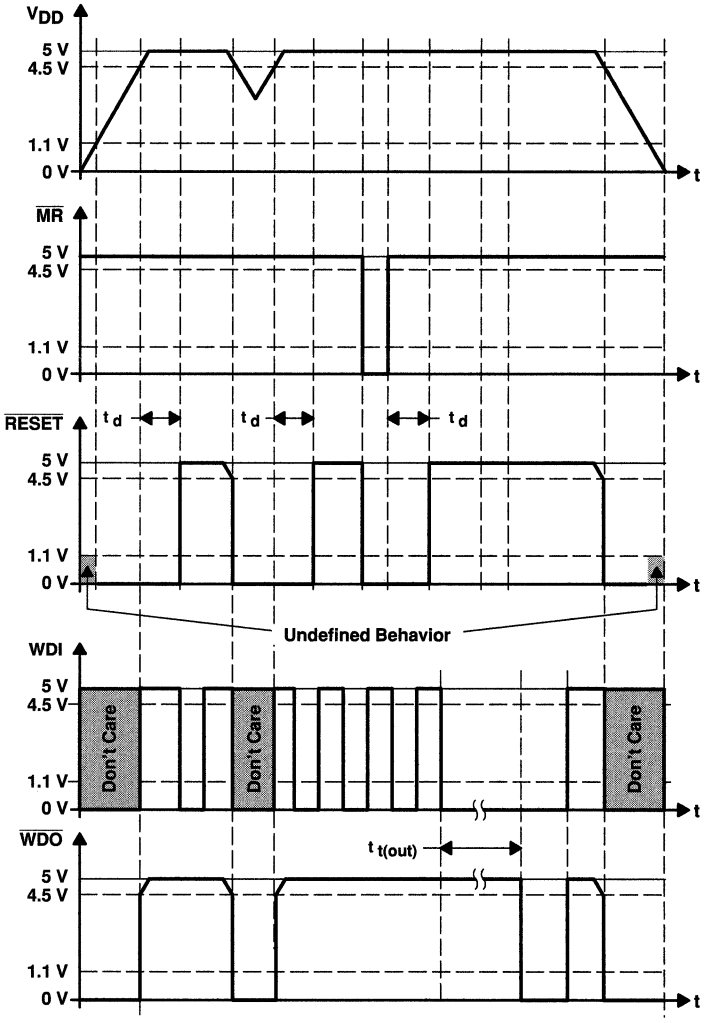
TRUTH TABLE, TPS370x

$PFI>V_{IT}$	$\overline{PFO}$	TYPICAL DELAY
0→1	L→H	0.5 µs
1→0	H→L	0.5 µs

functional block diagram



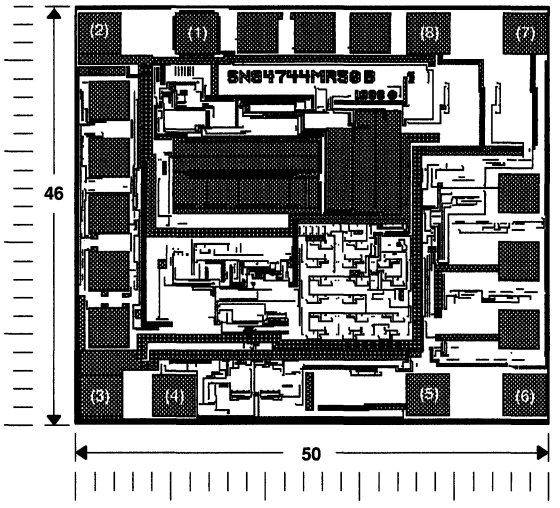
timing diagrams

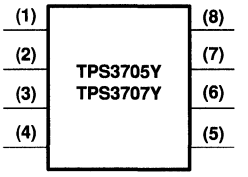


TPS370xY chip information

These chips, when properly assembled, display characteristics similar to those of the TPS370x. Thermal compression or ultrasonic bonding may be caused on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

Terminal Functions

TERMINAL NAME		NO.	I/O	DESCRIPTION
$\overline{MR}$		1	I	Manual reset
VDD		2		Supply voltage
GND		3		Ground
PFI		4	I	Power-fail comparator input
$\overline{PFO}$		5	O	Power-fail comparator output
WDI	TPS3705	6	I	Watchdog timer input
NC	TPS3707			No internal connection
$\overline{RESET}$		7	O	Active-low reset output
$\overline{WDO}$	TPS3705	8	O	Watchdog timer output
RESET	TPS3707		O	Active-high reset output

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1) . . . . . 7 V
All other pins (see Note 1) . . . . . –0.3 V to 7 V
Maximum low output current, I_{OL} . . . . . 5 mA
Maximum high output current, I_{OH} . . . . . –5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . . ±20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Soldering temperature . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	T_A <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGN	2.14 W	17.1 mW/°C	1.37 W	1.11 W
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage, V_I	0	V_{DD}+0.3	V
High-level input voltage, V_{IH}	0.7×V_{DD}		V
Low-level input voltage, V_{IL}		0.3×V_{DD}	V
Input transition rise and fall rate at $\overline{MR}$ or WDI, $\Delta t/\Delta V$		100	ns/V
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		TPS370x-xx	V_{DD} = 1.1 V, I_{OH} = –4 µA	0.8			V
			TPS3707-25	$V_{DD} = V_{IT+} + 0.2$ V, I_{OH} = –500 µA	0.7×V_{DD}			
			TPS370x-30					
			TPS370x-33					
			TPS370x-50	$V_{DD} = V_{IT+} + 0.2$ V, I_{OH} = –800 µA	V_{DD} –1.5 V			
			TPS370x-xx	V_{DD} = 6 V, I_{OH} = –800 µA				
V_{OL}	Low-level output voltage		TPS3707-25	$V_{DD} = V_{IT+}$+0.2 V, I_{OL} = 1 mA			0.3	V
			TPS370x-30					
			TPS370x-33					
			TPS370x-50	$V_{DD} = V_{IT+}$+0.2 V, I_{OL} = 2.5 mA			0.4	V
			TPS370x-xx	V_{DD} = 6 V, I_{OL} = 3 mA				
	Power-up reset voltage (see Note 2)			$V_{DD} \geq$ 1.1 V, I_{OL} = 50 µA			0.3	V
V_{IT-}	Negative-going input threshold voltage (see Note 3)		TPS3707-25	T_A = 0°C to 85°C	2.20	2.25	2.30	V
			TPS370x-30		2.57	2.63	2.68	
			TPS370x-33		2.87	2.93	2.98	
			TPS370x-50		4.45	4.55	4.63	
			TPS3707-25	T_A = –40°C to 85°C	2.20	2.25	2.32	V
			TPS370x-30		2.57	2.63	2.70	
			TPS370x-33		2.87	2.93	3.0	
			TPS370x-50		4.45	4.55	4.65	
		PFI	TPS370x-xx	$V_{DD} \geq$ 2 V, T_A = –40°C to 85°C	1.20	1.25	1.30	V
V_{hys}	Hysteresis	V_{DD}	TPS3707-25			40		mV
			TPS370x-30			50		
			TPS370x-33			50		
			TPS370x-50			70		
		PFI	TPS370x-xx			10		
$I_{IH(AV)}$	Average high-level input current	WDI		WDI = V_{DD} = 6 V, Time average (dc = 88%)		100	150	µA
$I_{IL(AV)}$	Average low-level input current			WDI = 0 V, V_{DD} = 6 V, Time average (dc = 12%)		–15	–20	µA
I_{IH}	High-level input current	WDI		WDI = V_{DD} = 6 V		120	170	µA
		$\overline{MR}$		$\overline{MR}$ = 0.7×V_{DD}, V_{DD} = 6 V		–130	–180	
I_{IL}	Low-level input current	WDI		WDI = 0 V, V_{DD} = 6 V		–120	–170	µA
		$\overline{MR}$		$\overline{MR}$ = 0 V, V_{DD} = 6 V		–430	–600	
I_I	Input current	PFI		V_{DD} = 6 V, 0 V ≤ $V_I \leq V_{DD}$	–1	0	1	µA
I_{DD}	Supply current		TPS3707-xx	V_{DD} = 2 V to 6 V, $\overline{MR}$ = V_{DD}, $\overline{MR}$, WDI and outputs unconnected		20	50	µA
			TPS3705-xx	V_{DD} = 2 V to 6 V, $\overline{MR}$= V_{DD}, $\overline{MR}$, WDI and outputs unconnected		30	50	µA
C_i	Input capacitance			V_I = 0 V to V_{DD}		5		pF

NOTES: 2. The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_{r,VDD} \geq 15$ µs/V
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	at V_{DD}	$V_{DD} = V_{IT+} + 0.2$ V, $V_{DD} = V_{IT-} - 0.2$ V	6			µs
		at $\overline{MR}$	$V_{DD} \geq V_{IT+} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100			ns
		at WDI	$V_{DD} \geq V_{IT+} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100			ns

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time out		$V_{DD} \geq V_{IT+} + 0.2$ V, See timing diagram	1.1	1.6	2.3	s
t_d	Delay time		$V_{DD} > V_{IT+} + 0.2$ V, See timing diagram	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay	$V_{DD} \geq V_{IT+} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$		50	250	ns
t_{PLH}	Propagation (delay) time, low-to-high-level output	$\overline{MR}$ to RESET delay (TPS3707–xx only)			50	250	ns
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay			3	5	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output	V_{DD} to RESET delay (TPS3707-xx only)			3	5	µs
t_{PHL}	Propagation (delay) time, high-to-low-level output	PFI to $\overline{PFO}$ delay	V_{DD} = 2 V to 6 V		0.5	1	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output				0.5	1	µs

TYPICAL CHARACTERISTICS

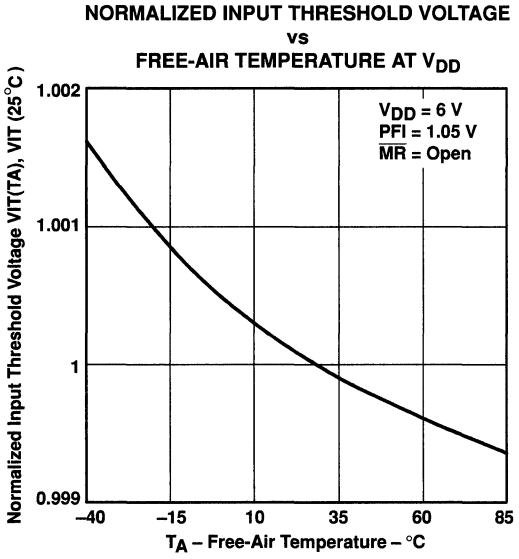


Figure 2

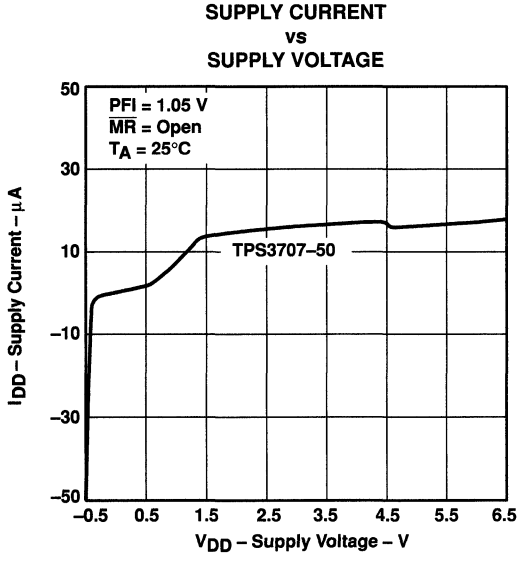


Figure 3

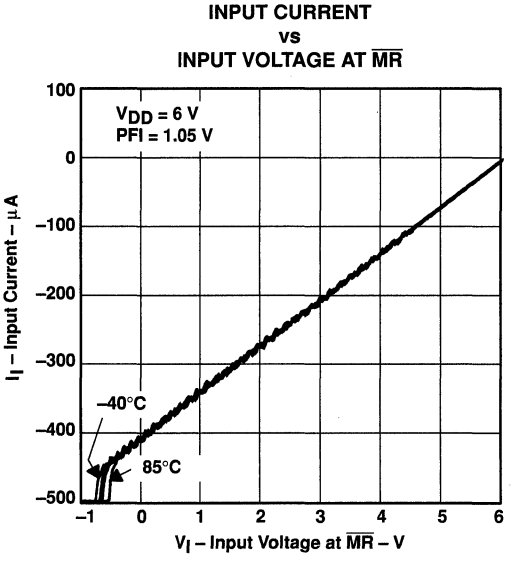


Figure 4

TYPICAL CHARACTERISTICS

MINIMUM PULSE DURATION AT V_{DD}
vs
V_{DD} THRESHOLD OVERDRIVE

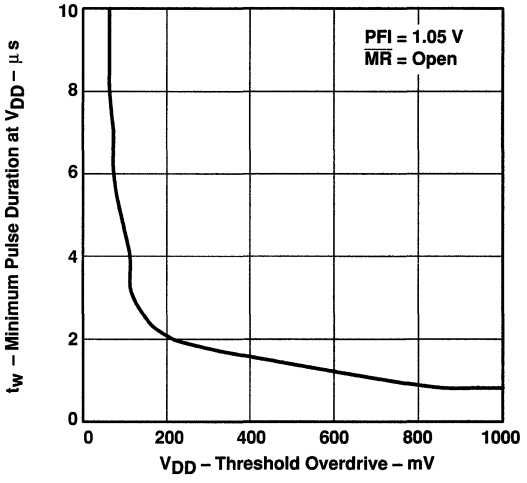


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

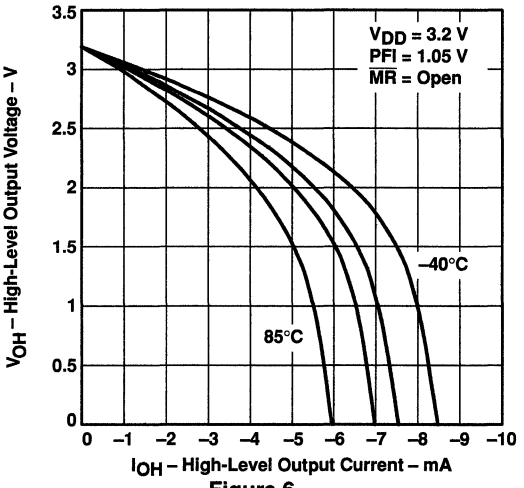


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

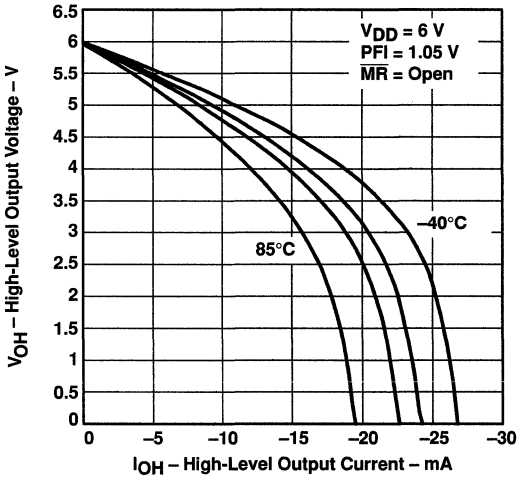


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

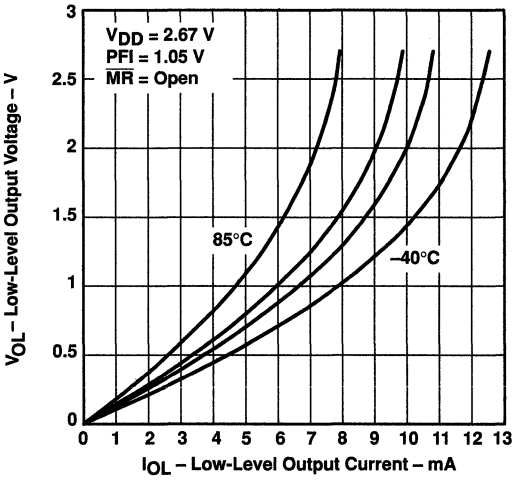
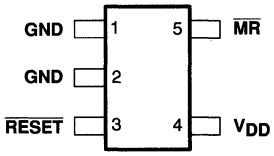


Figure 8

SLVS219 – AUGUST 1999

- **5-Pin SC-70 (SOT-323) Package**
- **Supply Current of 9 μA (Typ)**
- **Power-On Reset Generator With Fixed Delay Time of 200 ms**
- **Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, 5 V**
- **Manual Reset Input**
- **Temperature Range . . . –40°C to 85°C**

TPS3801 . . . DCK PACKAGE
(TOP VIEW)



description

The TPS3801 family of supervisory circuits provide circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

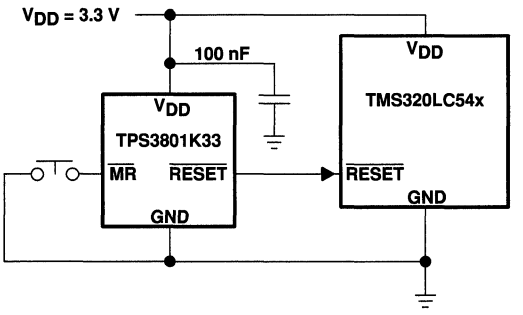
During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage V_{IT}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d(typ)}$ = 200 ms, starts after V_{DD} has risen above the threshold voltage V_{IT}. When the supply voltage drops below the threshold voltage V_{IT}, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed sense-threshold voltage V_{IT} set by an internal voltage divider.

The TPS3801 devices incorporate a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 5-pin SC-70 (SOT-323) package which is only about half the size of a 5-pin SOT-23 package.

The TPS3801 devices are characterized for operation over a temperature range of –40°C to 85°C.

typical applications



- **Applications Using DSPs, Microcontrollers, or Microprocessors**
- **Wireless Communication Systems**
- **Portable/Battery-Powered Equipment**
- **Programmable Controls**
- **Intelligent Instruments**
- **Industrial Equipment**
- **Notebook/Desktop Computers**
- **Automotive Systems**

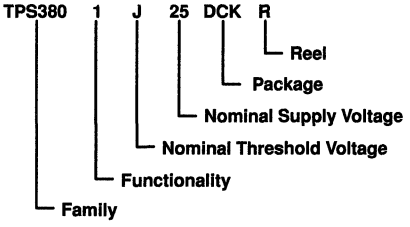
AVAILABLE OPTIONS

T_A	DEVICE NAME	THRESHOLD VOLTAGE	MARKING
–40°C to 85°C	TPS3801J25DCK	2.25 V	NJA
	TPS3801L30DCK	2.64 V	NPA
	TPS3801K33DCK	2.93 V	NWA
	TPS3801I50DCK	4.55 V	NSA

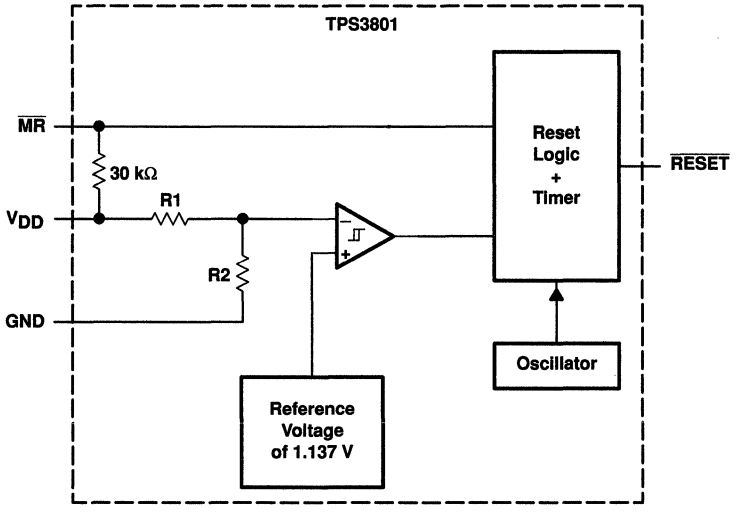
FUNCTION/TRUTH TABLE, TPS3801

$\overline{MR}$	$V_{DD}>V_{IT}$	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

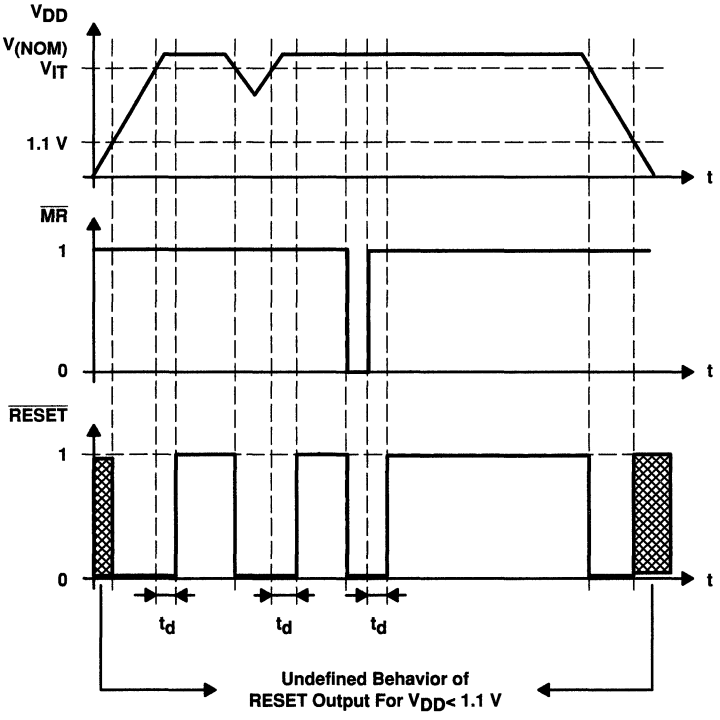
ORDERING INFORMATION



functional block diagram



timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1) . . . . . 7 V
All other pins (see Note 1) . . . . . –0.3 V to 7 V
Maximum low output current, I_{OL} . . . . . 5 mA
Maximum high output current, I_{OH} . . . . . –5 mA
Input clamp current, I_{IK} (V_I<0 or V_I>V_{DD}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O<0 or V_O>V_{DD}) . . . . . ±20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Soldering temperature . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t=1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	T_A <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DCK	321 mW	2.6 mW/°C	206 mW	167 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage, V_I	0	V_{DD}+0.3	V
High-level input voltage, V_{IH}	0.7×V_{DD}		V
Low-level input voltage, V_{IL}		0.3×V_{DD}	V
Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$		100	ns/V
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 2.5 V to 6 V I_{OH} = –500 µA	V_{DD} –0.2			V
			V_{DD} = 3.3 V I_{OH} = –2 mA	V_{DD} –0.4			
			V_{DD} = 6 V I_{OH} = –4 mA	V_{DD} –0.4			
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V, I_{OL} = 500 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 4 mA			0.4	
	Power-up reset voltage (see Note 2)		V_{DD} ≥ 1.1 V, I_{OL} = 50 µA			0.2	V
V_{IT-}	Negative-going input threshold voltage (see Note 3)	TPS3801J25	T_A – 40°C to +85°C	2.20	2.25	2.30	V
		TPS3801L30		2.58	2.64	2.70	
		TPS3801K33		2.87	2.93	2.99	
		TPS3801I50		4.45	4.55	4.65	
V_{hys}	Hysteresis	TPS3801J25			30		mV
		TPS3801L30			35		
		TPS3801K33			40		
		TPS3801I50			60		
I_{IH}	High-level input current	$\overline{MR}$	$\overline{MR}$ = 0.7×V_{DD}, V_{DD} = 6 V	–40	–60	–100	µA
I_{IL}	Low-level input current		$\overline{MR}$ = 0 V, V_{DD} = 6 V	–130	–200	–340	
I_{DD}	Supply current		V_{DD} = 2 V, $\overline{MR}$ and output unconnected		9	12	µA
			V_{DD} = 6 V, $\overline{MR}$ and output unconnected		20	25	
C_i	Input capacitance		V_I = 0 V to V_{DD}		5		pF

NOTES: 2. The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥ 15 µs/V.
3. To ensure best stability of the threshold voltage, a bypass capacitor (0.1 µF ceramic) should be placed near the supply terminals.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	at V_{DD}	V_{DD} = V_{IT-} + 0.2 V, V_{DD} = V_{IT-} –0.2 V	3			µs
		at $\overline{MR}$	V_{DD} ≥ V_{IT-} + 0.2V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	100			ns

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		V_{DD} ≥ V_{IT-} + 0.2 V, $\overline{MR}$ ≥ 0.7 × V_{DD} See timing diagram	120	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay	V_{DD} ≥ V_{IT-} + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}		15		ns
		V_{DD} to $\overline{RESET}$ delay	V_{IL} = V_{IT-} – 0.2 V, V_{IH} = V_{IT-} + 0.2 V		1		µs

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

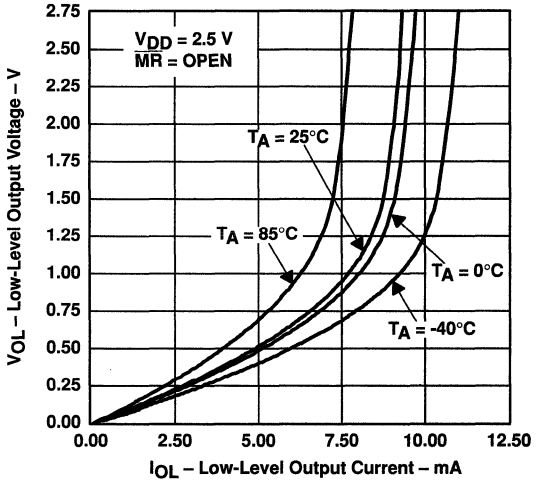


Figure 1

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

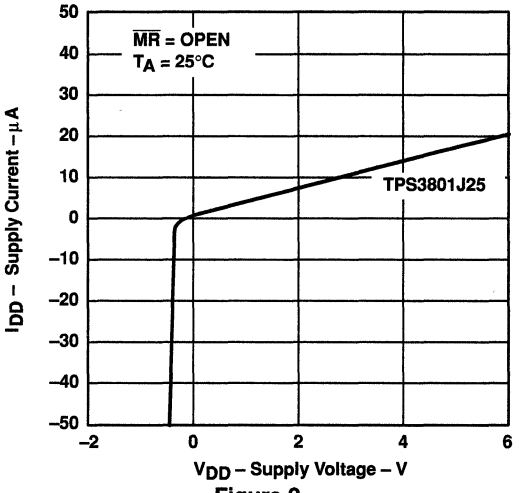


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

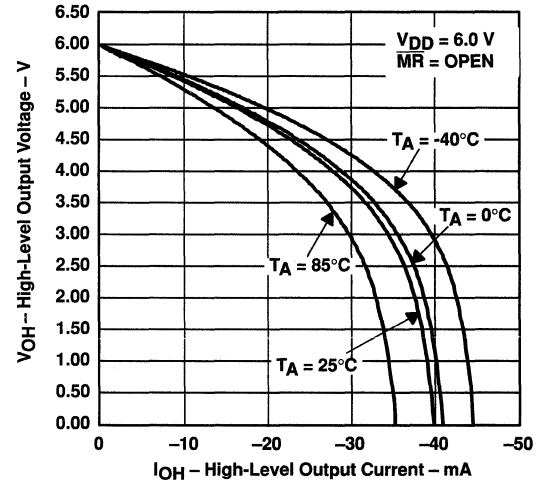


Figure 3

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

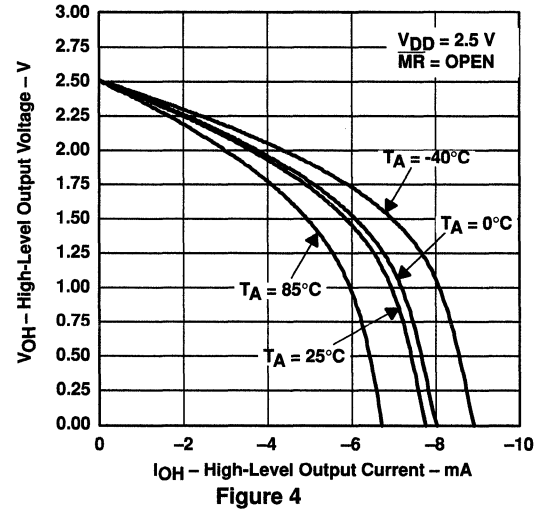


Figure 4

TYPICAL CHARACTERISTICS

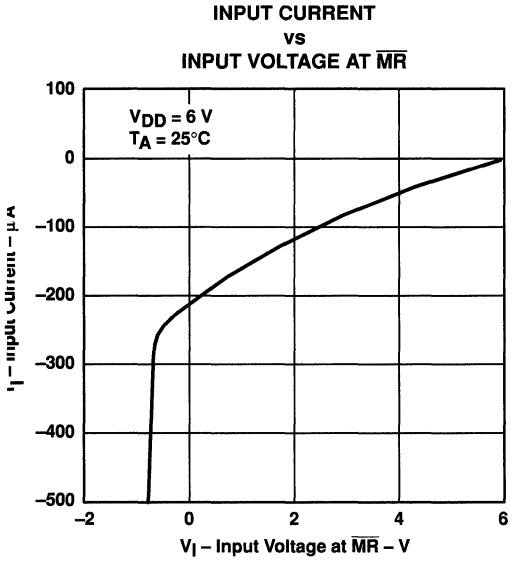


Figure 5

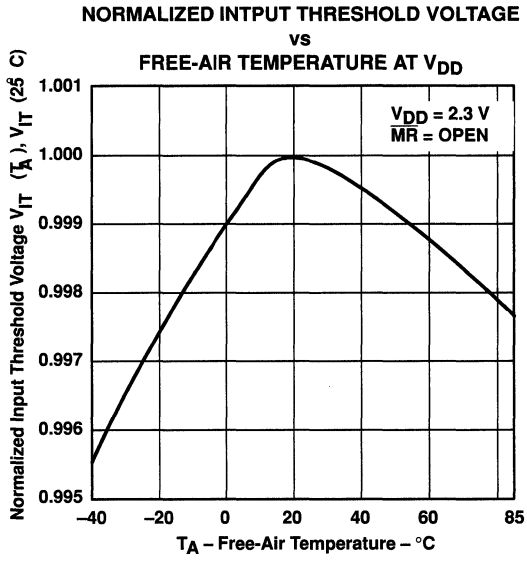


Figure 6

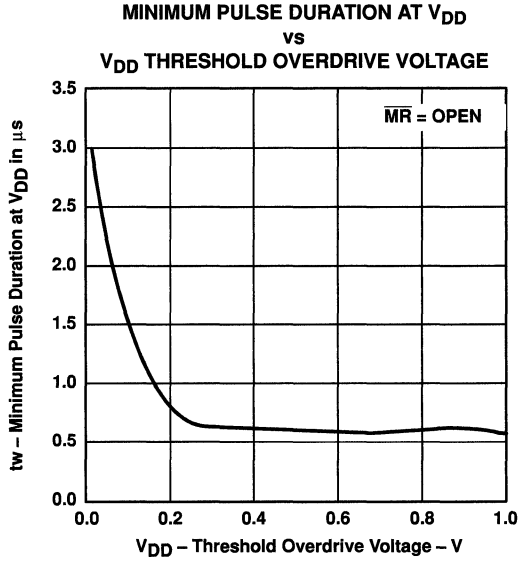
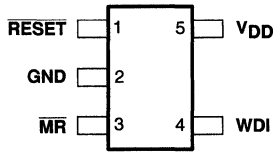


Figure 7

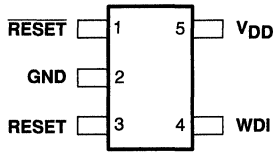
SLVS165B – APRIL 1998 – REVISED MAY 1999

- **Power-On Reset Generator With Fixed Delay Time of 200 ms (TPS3823/4/5/8) or 25 ms (TPS3820)**
- **Manual Reset Input (TPS3820/3/5/8)**
- **Push/Pull Reset (TPS3820/3/4/5), Reset (TPS3824), or Open-Drain Outputs (TPS3828)**
- **Supply Voltage Supervision Range 2.5 V, 3 V, 3.3 V, 5 V**
- **Watchdog Timer (TPS3820/3/4/8)**
- **Supply Current of 15 μA (Typ)**
- **SOT23-5 Package**
- **Temperature Range . . . –40°C to 85°C**

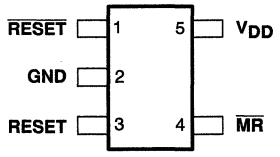
TPS3820†, TPS3823, TPS3828†
DBV PACKAGE
(TOP VIEW)



TPS3824 . . . DBV PACKAGE
(TOP VIEW)



TPS3825† . . . DBV PACKAGE
(TOP VIEW)



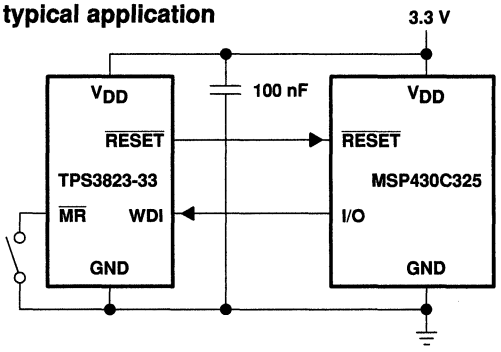
† This device is in the Product Preview stage of development. Contact the local TI sales office for availability

description

The TPS382x family of supervisors provides circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage V_{IT-}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_d, starts after V_{DD} has risen above the threshold voltage V_{IT-}. When the supply voltage drops below the threshold voltage V_{IT-}, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage V_{IT-} set by an internal voltage divider.

typical application



- **Applications Using DSPs, Microcontrollers, or Microprocessors**
- **Industrial Equipment**
- **Programmable Controls**
- **Automotive Systems**
- **Portable/Battery-Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communications Systems**
- **Notebook/Desktop Computers**

description (continued)

The TPS3820/3/5/8 devices incorporate a manual reset input, $\overline{MR}$. A low level at $\overline{MR}$ causes $\overline{RESET}$ to become active. The TPS3824/5 devices include a high-level output RESET. TPS3820/3/4/8 have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{tout}, $\overline{RESET}$ becomes active for the time period t_d. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 5-pin SOT23-5 package. The TPS382x devices are characterized for operation over a temperature range of -40°C to 85°C.

PACKAGE INFORMATION

DEVICE NAME	THRESHOLD VOLTAGE	MARKING
TPS3820-25DBVR†	2.25 V	
TPS3820-30DBVR†	2.63 V	
TPS3820-33DBVR†	2.93 V	PDEI
TPS3820-50DBVR†	4.55 V	PDDI
TPS3823-25DBVR	2.25 V	PAPI
TPS3823-30DBVR	2.63 V	PAQI
TPS3823-33DBVR	2.93 V	PARI
TPS3823-50DBVR	4.55 V	PASI
TPS3824-25DBVR	2.25 V	PATI
TPS3824-30DBVR	2.63 V	PAUI
TPS3824-33DBVR	2.93 V	PAVI
TPS3824-50DBVR	4.55 V	PAWI
TPS3825-25DBVR†	2.25 V	
TPS3825-30DBVR†	2.63 V	
TPS3825-33DBVR†	2.93 V	PDGI
TPS3825-50DBVR†	4.55 V	PDFI
TPS3828-25DBVR†	2.25 V	
TPS3828-30DBVR†	2.63 V	
TPS3828-33DBVR†	2.93 V	PDII
TPS3828-50DBVR†	4.55 V	PDHI

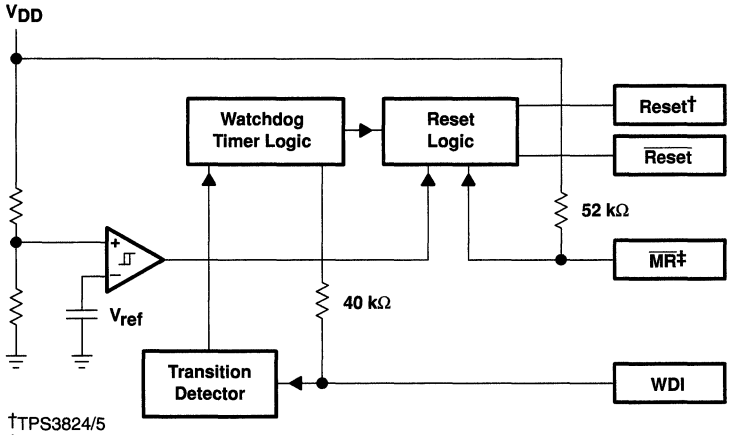
† This device is in the Product Preview stage of development. Contact the local TI sales office for availability

FUNCTION/TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{MR}$‡	$V_{DD}>V_{IT}$	$\overline{RESET}$	RESET†
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

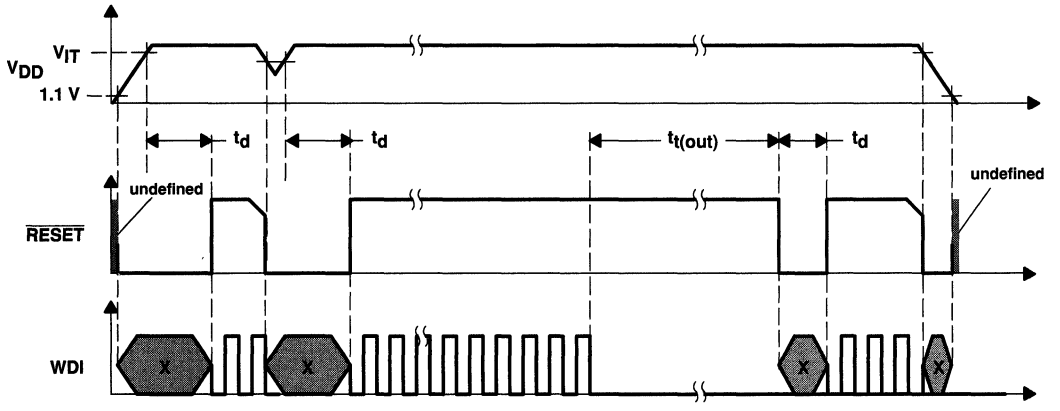
† TPS3824/5
‡ TPS3820/3/5/8

functional block diagram



†TPS3824/5
‡TPS3820/3/5/8

timing diagram



X = Don't care

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 6 V
Input voltage, $\overline{MR}$, WDI (see Note 1) ..... –0.3 V to (V_{DD} + 0.3 V)
Maximum low output current, I_{OL} ..... 5 mA
Maximum high output current, I_{OH} ..... –5 mA
Input clamp current range, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±10 mA
Output clamp current range, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±10 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... –40°C to 85°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Soldering temperature ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	350 mW	3.5 mW/°C	192 mW	140 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.1	5.5	V
Input voltage, V_I	0	V_{DD} + 0.3	V
High-level input voltage at $\overline{MR}$ and WDI, V_{IH}	0.7 × V_{DD}		V
Low-level input voltage, V_{IL}		0.3 × V_{DD}	V
Input transition rise and fall rate at $\overline{MR}$ or WDI, $\Delta t/\Delta V$		100	ns/V
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$	TPS382x-25	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OH} = -20$ µA	$0.8 \times V_{DD}$			V
			TPS382x-30, TPS382x-33	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OH} = -30$ µA				
			TPS382x-50	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OH} = -120$ µA	$V_{DD} - 1.5$ V			
		RESET	TPS3824-25, TPS3825-25	$V_{DD} \geq 1.8$ V, $I_{OH} = -100$ µA	$0.8 \times V_{DD}$			V
			TPS3824-30, TPS3825-30	$V_{DD} \geq 1.8$ V, $I_{OH} = -150$ µA				
			TPS3824-33, TPS3825-33					
			TPS3824-50, TPS3825-50					
V_{OL}	Low-level output voltage	RESET	TPS3824-25, TPS3825-25	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OL} = 1$ mA			0.4	V
			TPS3824-30, TPS3825-30	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OL} = 1.2$ mA				
			TPS3824-33, TPS3825-33					
			TPS3824-50, TPS3825-50	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OL} = 3$ mA				
		$\overline{RESET}$	TPS382x-25	$V_{DD} = V_{IT-} - 0.2$ V, $I_{OL} = 1$ mA			0.4	V
			TPS382x-30	$V_{DD} = V_{IT-} - 0.2$ V, $I_{OL} = 1.2$ mA				
			TPS382x-33					
			TPS382x-50	$V_{DD} = V_{IT-} - 0.2$ V, $I_{OL} = 3$ mA				
	Power-up reset voltage (see Note 2)			$V_{DD} \geq 1.1$ V, $I_{OL} = 20$ µA			0.4	V
V_{IT-}	Negative-going input threshold voltage (see Note 3)		TPS382x-25	$T_A = 0°C - 85°C$	2.21	2.25	2.30	V
			TPS382x-30		2.59	2.63	2.69	
			TPS382x-33		2.88	2.93	3	
			TPS382x-50		4.49	4.55	4.64	
			TPS382x-25	$T_A = -40°C - 85°C$	2.20	2.25	2.30	V
			TPS382x-30		2.57	2.63	2.69	
			TPS382x-33		2.86	2.93	3	
			TPS382x-50		4.46	4.55	4.64	
V_{hys}	Hysteresis at V_{DD} input		TPS382x-25, TPS382x-30, TPS382x-33			30		mV
			TPS382x-50			50		

NOTES: 2. The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, $V_{DD} \geq 15$ µs/V
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminals.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IH(AV)}$	Average high-level input current		WDI	WDI = V_{DD}, time average (dc = 88%)		120		µA
$I_{IL(AV)}$	Average low-level input current		WDI	WDI = 0.3 V, V_{DD} = 5.5 V time average (dc = 12%)		–15		µA
I_{IH}	High-level input current		WDI	WDI = V_{DD}		140	190	µA
			$\overline{MR}$	$\overline{MR}$ = V_{DD} × 0.7, V_{DD} = 5.5 V		–40	–60	µA
I_{IL}	Low-level input current		WDI	WDI = 0.3 V, V_{DD} = 5.5 V		140	190	µA
			$\overline{MR}$	$\overline{MR}$ = 0.3 V, V_{DD} = 5.5 V		–110	–160	µA
I_{OS}	Output short-circuit current (see Note 4)	$\overline{RESET}$	TPS382x-25	V_{DD} = V_{IT}, max + 0.2 V, V_O = 0 V			–400	µA
			TPS382x-30				–400	µA
			TPS382x-33				–400	µA
			TPS382x-50				–800	µA
I_{DD}	Supply current			WDI and $\overline{MR}$ unconnected, Outputs unconnected		15	25	µA
	Internal pullup resistor at $\overline{MR}$					52		kΩ
C_i	Input capacitance at $\overline{MR}$, WDI			V_I = 0 V to 5.5 V		5		pF

NOTE 4: The $\overline{RESET}$ short-circuit current is the maximum pullup current when $\overline{RESET}$ is driven low by a µP bidirectional reset pin.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_w	Pulse width	at V_{DD}	V_{DD} = V_{IT-} + 0.2 V, V_{DD} = V_{IT-} - 0.2 V	6		µs
		at $\overline{MR}$	V_{DD} ≥ V_{IT-} + 0.2 V, V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}	1		µs
		at WDI	V_{DD} ≥ V_{IT-} + 0.2 V, V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}	100		ns

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{tout}	Watchdog time out	TPS3820	V_{DD} ≥ V_{IT-} + 0.2 V, See Timing Diagram	112	200	310	ms
		TPS3823/4/8		0.9	1.6	2.5	s
t_d	Delay time	TPS3820	V_{DD}≥V_{IT-} +0.2 V, See timing diagram	15	25	37	ms
		TPS3823/4/5/8		120	200	300	ms
t_{pHL}	Propagation (delay) time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay (TPS3820/3/5/8)	V_{DD}≥V_{IT-} +0.2 V, V_{IL}=0.3 x V_{DD}, V_{IH}=0.7 x V_{DD}			0.1	µs
		V_{DD} to $\overline{RESET}$ delay	V_{IL} = V_{IT-} - 0.2 V, V_{IH} = V_{IT-} + 0.2 V			25	µs
		V_{DD} to RESET delay (TPS3824/5)				25	µs

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE AT V_{DD}

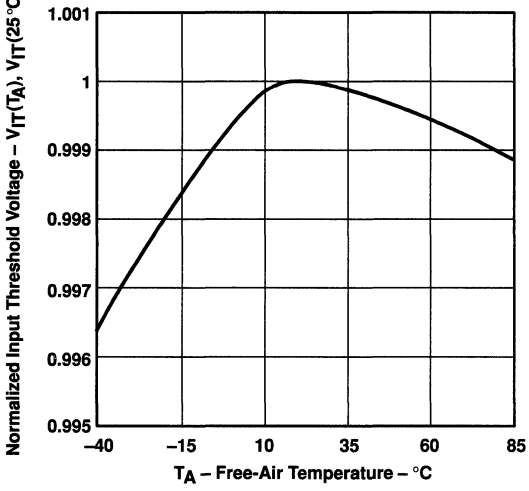


Figure 1

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

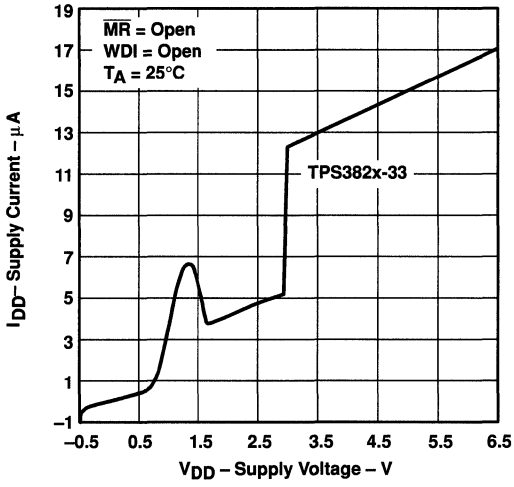


Figure 2

INPUT CURRENT
vs
INPUT VOLTAGE AT $\overline{MR}$

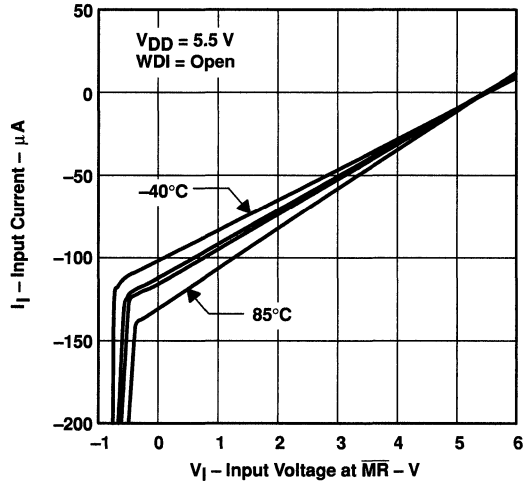


Figure 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

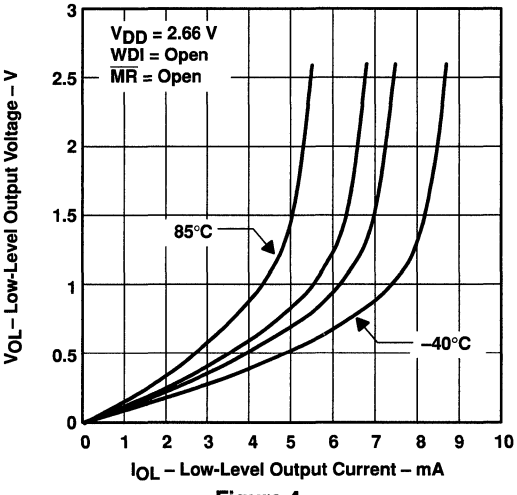


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

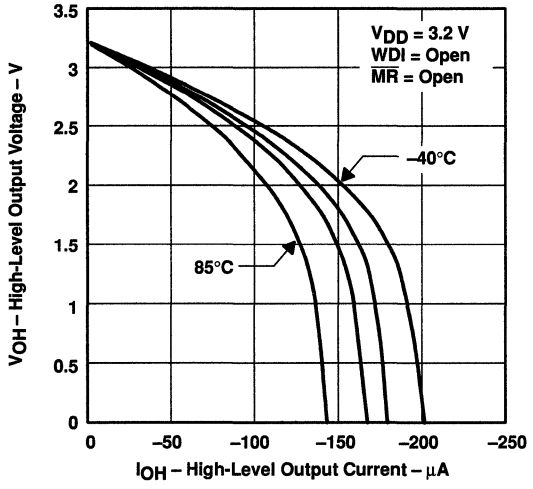


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

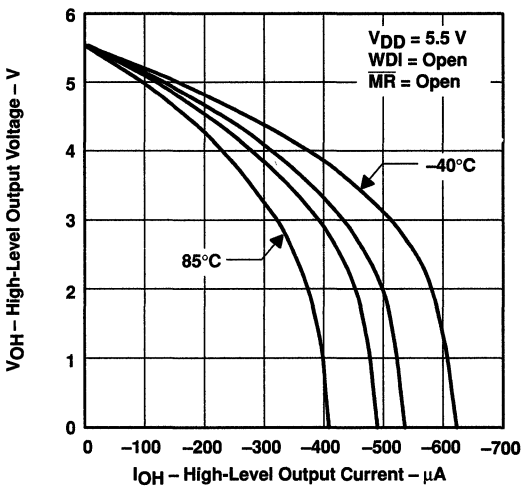


Figure 6

MINIMUM PULSE DURATION AT V_{DD}
vs
V_{DD} THRESHOLD OVERDRIVE

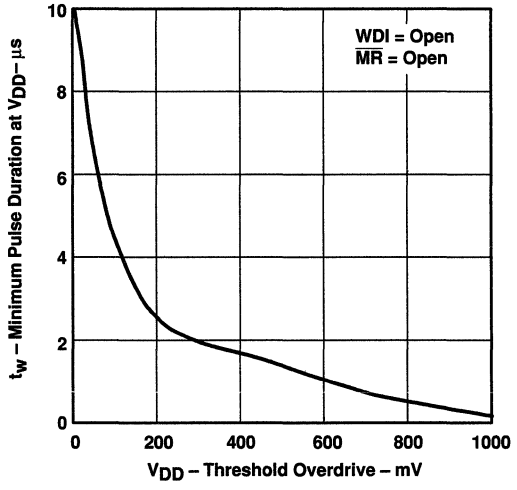
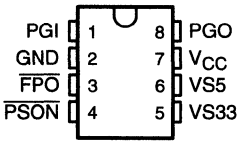


Figure 7

- **Over Voltage Protection and Lock Out for 5 V, 3.3 V, and 12 V**
- **Under Voltage Protection and Lock Out for 5 V and 3.3 V**
- **Fault Protection Output with Open Drain Output Stage**
- **Open Drain Power Good Output Signal for Power Good Input, 5 V and 3.3 V**
- **300 ms Power Good Delay**
- **75 ms Delay for 5-V and 3.3-V Short-Circuit Turn On Protection**
- **38 ms $\overline{\text{PSON}}$ Control Debounce**
- **73 μs Width Noise Deglitches**
- **Wide Power Supply Voltage Range from 4 V to 15 V**

D OR P PACKAGE
(TOP VIEW)



description

The TPS5510 is designed to minimize external components of personal computer switching power supply systems. It provides protection circuits, power good indicator, fault protection output ($\overline{\text{FPO}}$), and a $\overline{\text{PSON}}$ control.

OVP (Over Voltage Protection) monitors 5 V, 3.3 V, and 12 V (12 V OV detects via V_{CC} terminal). UVP (Under Voltage Protection) monitors 5 V and 3.3 V. When an OV or UV condition is detected, the PGO (power good output) is asserted low and $\overline{\text{FPO}}$ is latched high. $\overline{\text{PSON}}$ from low to high resets the protection latch. UVP function will be enabled 75 ms after $\overline{\text{PSON}}$ is set low and debounced.

Power good feature monitors PGI, 5 V and 3.3 V and issues a power good signal when they are ready.

The TPS5510 is characterised for operation from T_J = –40°C to 125°C junction temperature.

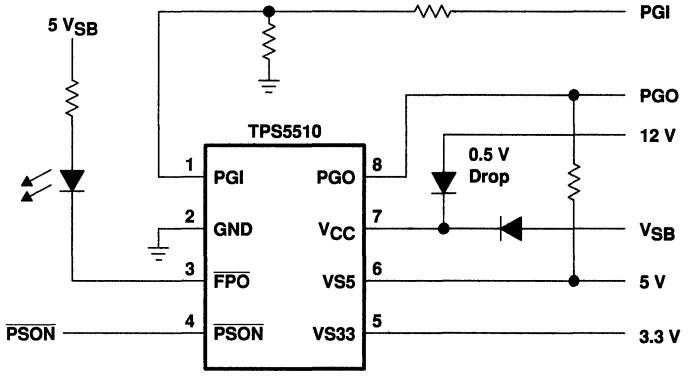
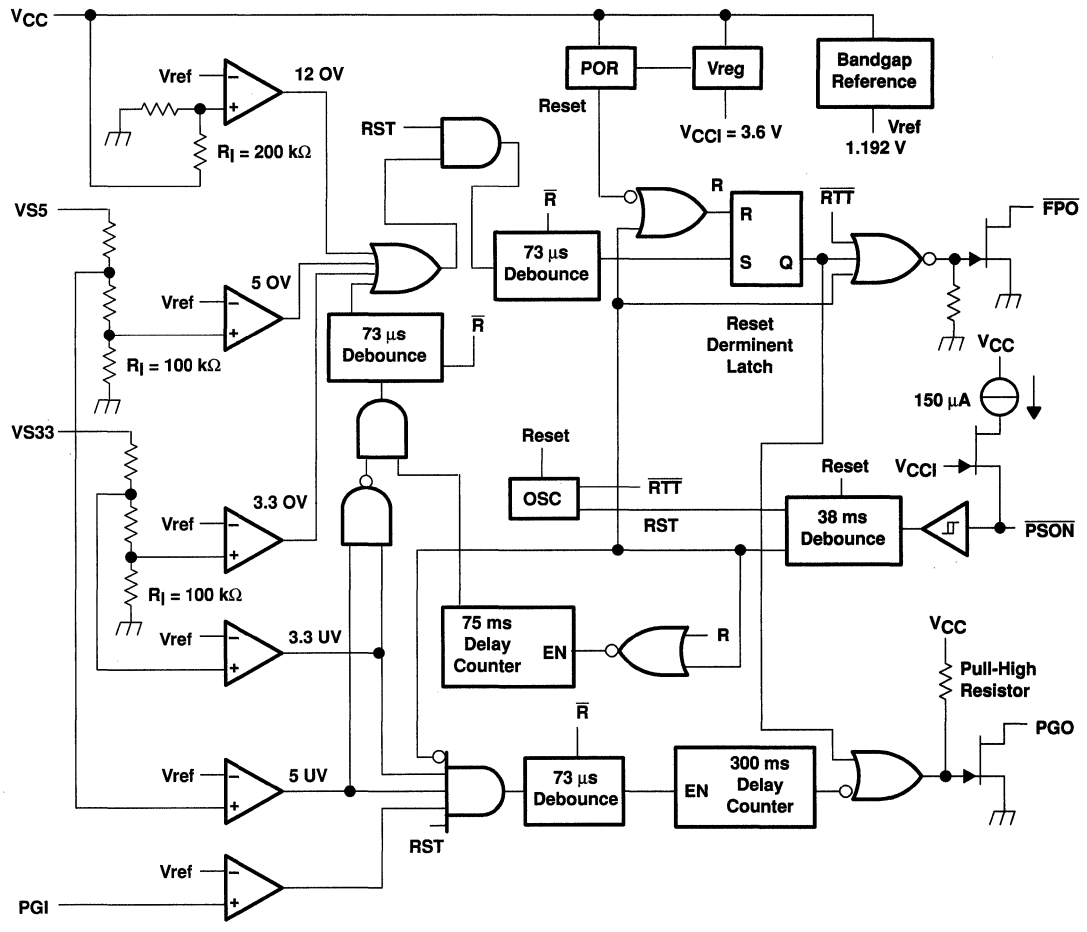


Figure 1. TPS5510 Typical Application

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
VS33	5	I	3.3 V over/under voltage protection input pin
VS5	6	I	5 V over/under voltage protection input pin
GND	2		Ground
$\overline{FPO}$	3	O	Inverted fault protection output, open drain output stage
PGI	1	I	Power good input signal pin
PGO	8	O	Power good output signal pin, open drain output stage
$\overline{PSON}$	4	I	ON/OFF control input pin
V_{CC}	7	I	Supply voltage/12 V over voltage protection input pin

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
P	1092 mW	8.74 mW/°C	218 mW
D	730 mW	5.84 mW/°C	146 mW

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC}, (see Note1) ..... 16 V
Output voltage, V_O ($\overline{FPO}$) ..... 16 V
Output voltage, V_O (PGO) ..... 8 V
Supply current, I_{CC} ..... 1 mA
Continuous total power dissipation ..... see Dissipation Rating Table
Operating junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the device GND terminal.

recommended operating conditions

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}			4		15	V
Input voltage, V_I	$\overline{PSON}$, VS5, VS33, PGI				7	V
Output voltage, V_O	$\overline{FPO}$				15	V
	PGO				7	V
Operating junction temperature, T_J			–40		125	°C
Output sink current, $I_{O(sink)}$	$\overline{FPO}$				30	mA
	PGO				10	mA
Supply voltage rising time, t_r		See Note 2	1			ms

NOTE 2: V_{CC} rising and falling slew rate must be less then 14 V/ms.

electrical characteristics, V_{CC} = 5 V, T_J = full range. (unless otherwise specified)

over voltage protection

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Over-voltage threshold	VS33		3.9	4.1	4.3	V
		VS5		5.7	6.1	6.5	
		V_{CC}		13.3	13.8	14.3	
I_{LKG}	Leakage current ($\overline{FPO}$)		$V(\overline{FPO})$ = 5 V			5	µA
V_{OL}	Low level output voltage ($\overline{FPO}$)		I_{sink} = 10 mA			0.3	V
			I_{sink} = 30 mA			0.7	

PGI and PGO

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input threshold voltage (PGI)			1.141	1.192	1.242	V
	Under-voltage threshold	VS33		2.71	2.83	2.95	V
		VS5		4.1	4.3	4.47	
	Short circuit protection delay time	3.3 V, 5 V		49	75	114	ms
I_{LKG}	Leakage current (PGO)		PGO = 5 V			5	µA
V_{OL}	Low level output voltage (PGO)		Sink current = 10 mA			0.4	V

$\overline{PSON}$ control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input pull-up current	$\overline{PSON}$ = 0 V		150		µA
	High-level input voltage		2.4			V
	Low-level input voltage				1.2	V

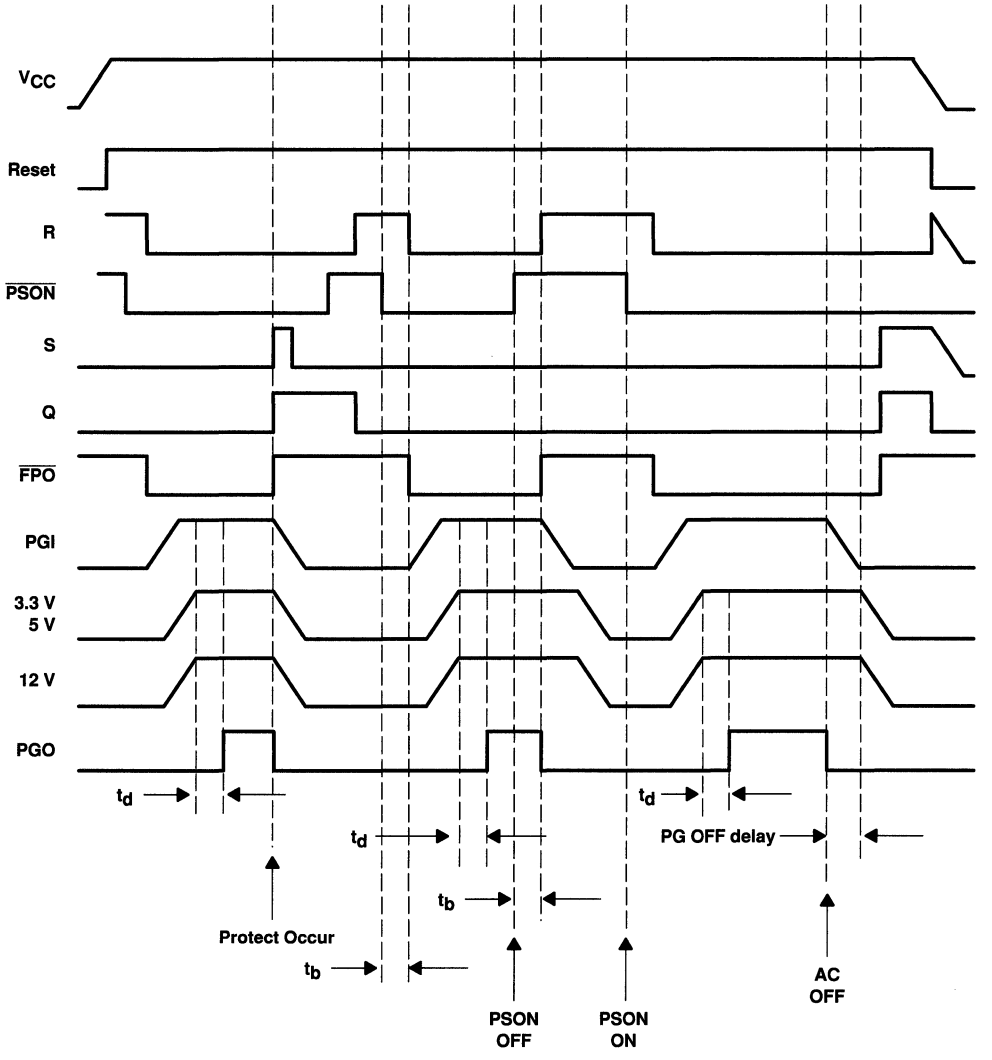
total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	$\overline{PSON}$ = 5 V			1	mA

switching characteristics, V_{CC} = 5 V, T_J = full range

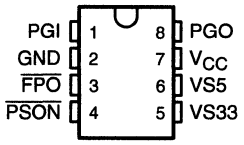
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time (PGI to PGO)		200	300	450	ms
t_b	De-bounce time ($\overline{PSON}$)		24	38	57	ms
	Noise deglitch time		47	73	110	µs

timing chart



- **Over Voltage Protection and Lock Out for 5 V, 3.3 V, and 12 V**
- **Fault Protection Output with Open Drain Output Stage**
- **Open Drain Power Good Output Signal for Power Good Input, 5 V and 3.3 V**
- **300 ms Power Good Delay**
- **2.3 ms $\overline{\text{PSON}}$ Control to $\overline{\text{FPO}}$ Turn-Off Delay**
- **38 ms $\overline{\text{PSON}}$ Control Debounce**
- **73 μs Width Noise Deglitches**
- **Wide Power Supply Voltage Range from 4 V to 15 V**

D OR P PACKAGE
(TOP VIEW)



description

The TPS5511 is designed to minimize the external components of personal-computer switching power supply systems. It provides protection circuits, power good indicator, fault protection output ($\overline{\text{FPO}}$), and $\overline{\text{PSON}}$ control.

OVP (over voltage protection) monitors 5 V, 3.3 V, and 12 V (12 V OV detects via V_{CC} terminal). When an OV condition is detected, the PGO (power good output) is asserted low and $\overline{\text{FPO}}$ is latched high. $\overline{\text{PSON}}$ from low to high resets the protection latch. There is a 2.3-ms turn-off delay from $\overline{\text{PSON}}$ to $\overline{\text{FPO}}$. There is no delay during turn on.

Power good feature monitors PGI, 5 V and 3.3 V under voltages and issues a power good signal when they are ready.

The TPS5511 is characterized for operation from T_J = –40°C to 125°C junction temperature.

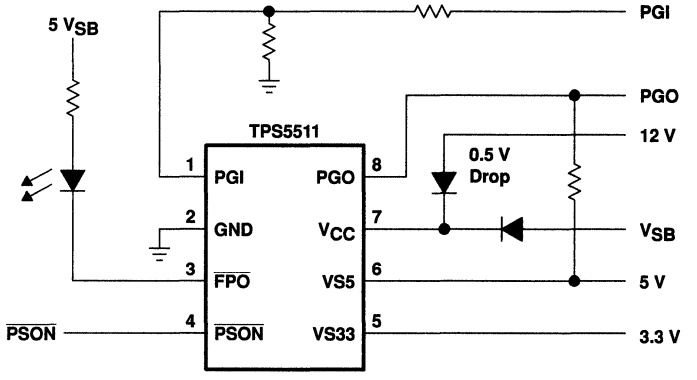
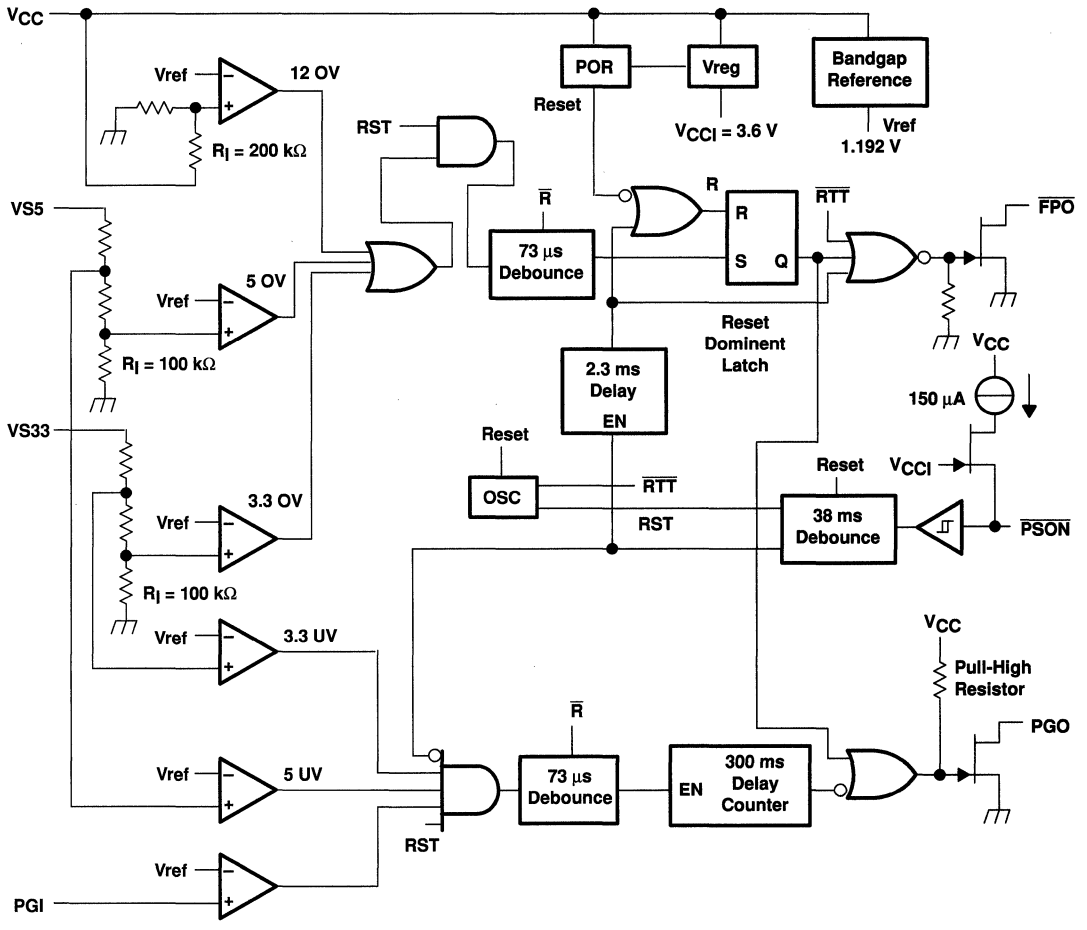


Figure 1. TPS5511 Typical Application

functional block diagram



Terminal Functions

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VS5	6	I	5 V over/under voltage protection input pin
GND	2		Ground
$\overline{FPO}$	3	O	Inverted fault protection output, open drain output stage
PGI	1	I	Power good input signal pin
PGO	8	O	Power good output signal pin, open drain output stage
$\overline{PSON}$	4	I	ON/OFF control input pin
V_{CC}	7	I	Supply voltage/12 V over voltage protection input pin

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
P	1092 mW	8.74 mW/°C	218 mW
D	730 mW	5.84 mW/°C	146 mW

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC}, (see Note1) ..... 16 V
Output voltage, V_O ($\overline{FPO}$) ..... 16 V
Output voltage, V_O (PGO) ..... 8 V
Supply current, I_{CC} ..... 1 mA
Continuous total power dissipation ..... see Dissipation Rating Table
Operating junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the device GND terminal.

recommended operating conditions

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}			4		15	V
Input voltage, V_I	$\overline{PSON}$, VS5, VS33, PGI				7	V
Output voltage, V_O	$\overline{FPO}$				15	V
	PGO				7	V
Operating junction temperature, T_J			–40		125	°C
Output sink current, $I_{O(sink)}$	$\overline{FPO}$				30	mA
	PGO				10	mA
Supply voltage rising time, t_r		See Note 2	1			ms

NOTE 2: V_{CC} rising and falling slew rate must be less then 14 V/ms.

electrical characteristics, V_{CC} = 5 V, T_J = full range. (unless otherwise specified)

over voltage protection

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Over-voltage threshold	VS33		3.9	4.1	4.3	V
		VS5		5.7	6.1	6.5	
		V_{CC}		13.3	13.8	14.3	
I_{LKG}	Leakage current ($\overline{FPO}$)		$V(\overline{FPO})$ = 5 V			5	µA
V_{OL}	Low level output voltage ($\overline{FPO}$)		I_{sink} = 10 mA			0.3	V
			I_{sink} = 30 mA			0.7	

PGI and PGO

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input threshold voltage (PGI)			1.141	1.192	1.242	V
	Under-voltage threshold	VS33		2.71	2.83	2.95	V
		VS5		4.1	4.3	4.47	
I_{LKG}	Leakage current (PGO)		PGO = 5 V			5	µA
V_{OL}	Low level output voltage (PGO)		Sink current = 10 mA			0.4	V

$\overline{PSON}$ control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input pull-up current	$\overline{PSON}$ = 0 V		150		µA
	High-level input voltage		2.4			V
	Low-level input voltage				1.2	V

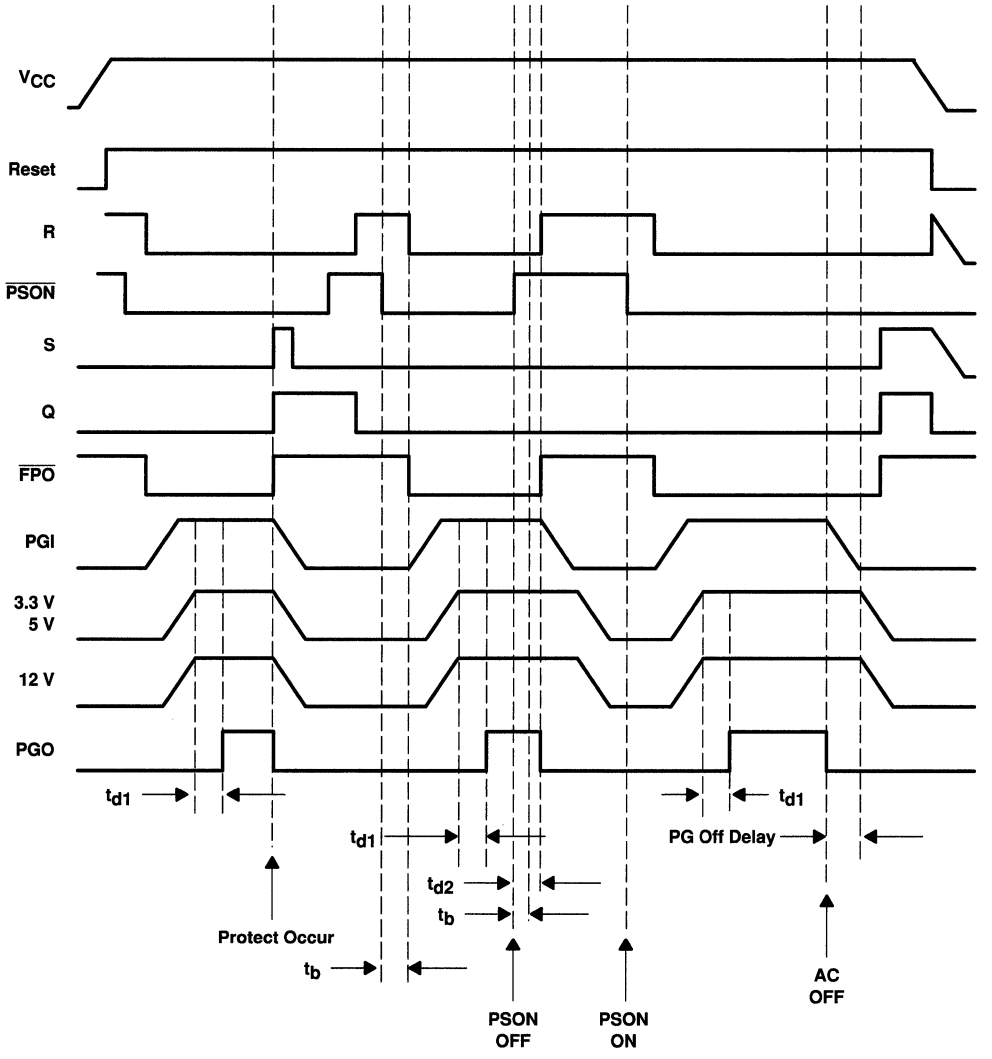
total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	$\overline{PSON}$ = 5 V			1	mA

switching characteristics, V_{CC} = 5 V, T_J = full range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d1}	Delay time (PGI to PGO)		200	300	450	ms
t_b	De-bounce time ($\overline{PSON}$)		24	38	57	ms
	Noise deglitch time		47	73	110	µs
t_{d2}	$\overline{PSON}$ to $\overline{FPO}$ delay time		t_b + 1.1	t_b + 2.3	t_b + 4	ms

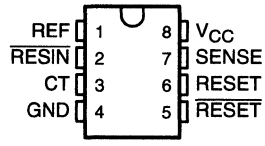
timing chart



SLVS028E – APRIL 1983 – REVISED JULY 1999

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Wide Supply-Voltage Range**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

D OR P PACKAGE
(TOP VIEW)



description

The TL77xxA family of integrated-circuit supply-voltage supervisors is specifically designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 3.6 V. At this point (assuming that SENSE is above V_{IT+}), the delay timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d = 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

During power down (assuming that SENSE is below V_{IT-}), the outputs remain active until the V_{CC} falls below a maximum of 2 V. After this, the outputs are undefined.

An external capacitor (typically 0.1 μF for the TL77xxAC and TL77xxAI) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL77xxAC series is characterized for operation from 0°C to 70°C. The TL77xxAI series is characterized for operation from –40°C to 85°C.

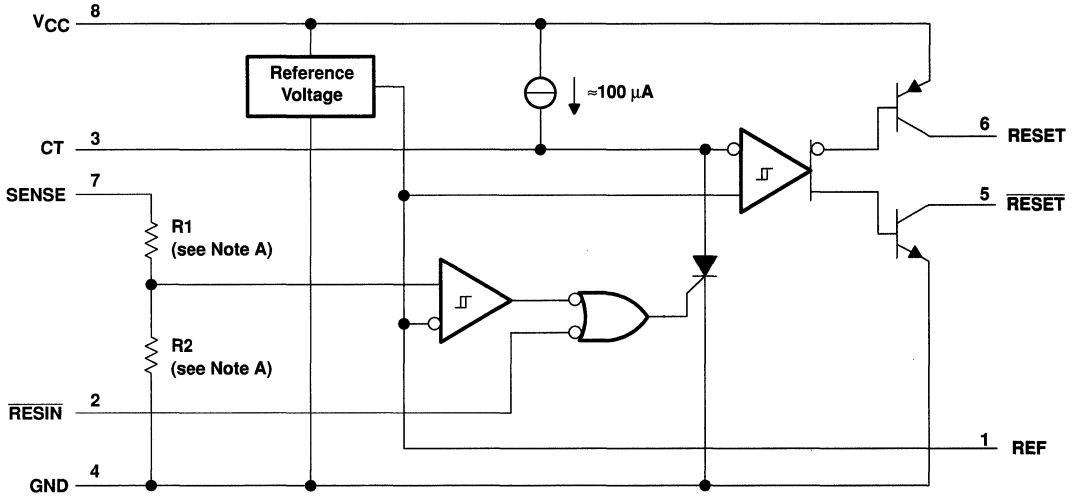
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	TL7702ACD TL7705ACD TL7709ACD TL7712ACD TL7715ACD	TL7702ACP TL7705ACP TL7709ACP TL7712ACP TL7715ACP	TL7702ACY TL7705ACY TL7709ACY TL7712ACY TL7715ACY
–40°C to 85°C	TL7702AID TL7705AID TL7709AID TL7712AID TL7715AID	TL7702AIP TL7705AIP TL7709AIP TL7712AIP TL7715AIP	— — — — —

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL7702ACDR). Chip forms are tested at 25°C.

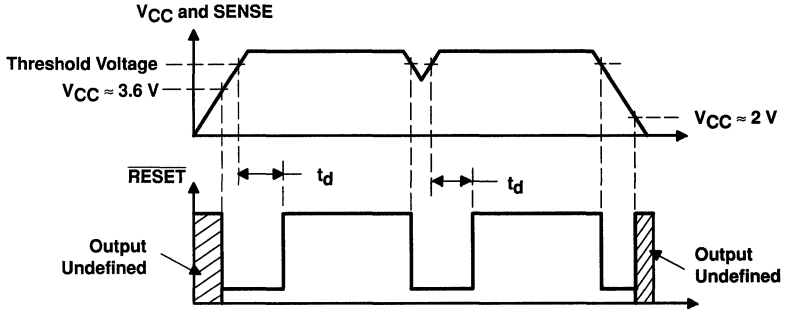
functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



NOTES: A. TL7702A: R1 = 0 Ω, R2 = open
TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ
B. Resistor values shown are nominal.

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 20 V
Input voltage range, V_I, $\overline{RESIN}$ ..... –0.3 V to 20 V
Input voltage range, V_I, SENSE: TL7702A (see Note 2) ..... –0.3 V to 6 V
TL7705A ..... –0.3 V to 20 V
TL7709A ..... –0.3 V to 20 V
TL7712A, TL7715A ..... –0.3 V to 20 V
High-level output current, I_{OH}, RESET ..... –30 mA
Low-level output current, I_{OL}, $\overline{RESET}$ ..... 30 mA
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D package ..... 97°C/W
P package ..... 127°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} – 1 V or 6 V, whichever is less.
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
4. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
High-level input voltage at $\overline{RESIN}$, V_{IH}		2		V
Low-level input voltage at $\overline{RESIN}$, V_{IL}			0.6	V
Input voltage, SENSE, V_I	TL7702A	0	See Note 2	V
	TL7705A	0	10	
	TL7709A	0	15	
	TL7712A	0	20	
	TL7715A	0	20	
High-level output current, RESET, I_{OH}			–16	mA
Low-level output current, $\overline{RESET}$, I_{OL}			16	mA
Timing capacitor, C_T			10	µF
Operating free-air temperature range, T_A	TL77xxAC	0	70	°C
	TL77xxAI	–40	85	

NOTE 2: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} – 1 V or 6 V, whichever is less.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL77xxAC TL77xxAI			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA	V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage		T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702A	T_A = 25°C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11	
		TL7715A		13.2	13.5	13.8	
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702A	T_A = 25°C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 2.4 V to V_{CC}			20	µA
			V_I = 0.4 V			–100	
		SENSE TL7702A	$V_{ref} < V_I < V_{CC} - 1.5$ V		0.5	2	
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 18 V			50	µA
I_{OL}	Low-level output current, RESET		V_O = 0			–50	µA
I_{CC}	Supply current		All inputs and outputs open		1.8	3	mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡		TL77xxAC TL77xxAI			UNIT
					MIN	TYP	MAX	
	Output pulse duration		C_T = 0.1 µF		0.65	1.2	2.6	µs
	Input pulse duration at $\overline{\text{RESIN}}$				0.4			µs
$t_{w(S)}$	Pulse duration at SENSE input to switch outputs		$V_{IH} = V_{IT-}$ +200 mV,	$V_{IL} = V_{IT-}$ –200 mV	2			µs
t_{pd}	Propagation delay time, $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$		V_{CC} = 5 V				1	µs
t_r	Rise time	RESET	V_{CC} = 5 V,	See Note 5			0.2	µs
		$\overline{\text{RESET}}$					3.5	
t_f	Fall time	RESET	V_{CC} = 5 V,	See Note 5			3.5	µs
		$\overline{\text{RESET}}$					0.2	

‡ All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.
NOTE 5: The rise and fall times are measured with a 4.7-kΩ load resistor at RESET and $\overline{\text{RESET}}$.

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL77xxAY			UNIT
				MIN	TYP	MAX	
V_{ref}	Reference voltage				2.53		V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702A			2.53		V
		TL7705A			4.55		
		TL7709A			7.6		
		TL7712A			10.8		
		TL7715A			13.5		
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702A			10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current, SENSE	TL7702A	$V_{ref} < V_I < V_{CC} - 1.5$ V		0.5		µA
I_{CC}	Supply current		All inputs and outputs open		1.8		mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	TL77xxAY			UNIT
			MIN	TYP	MAX	
t_d	Output pulse time delay	C_T = 0.1 µF		1.2		µs

‡ All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.

PARAMETER MEASUREMENT INFORMATION

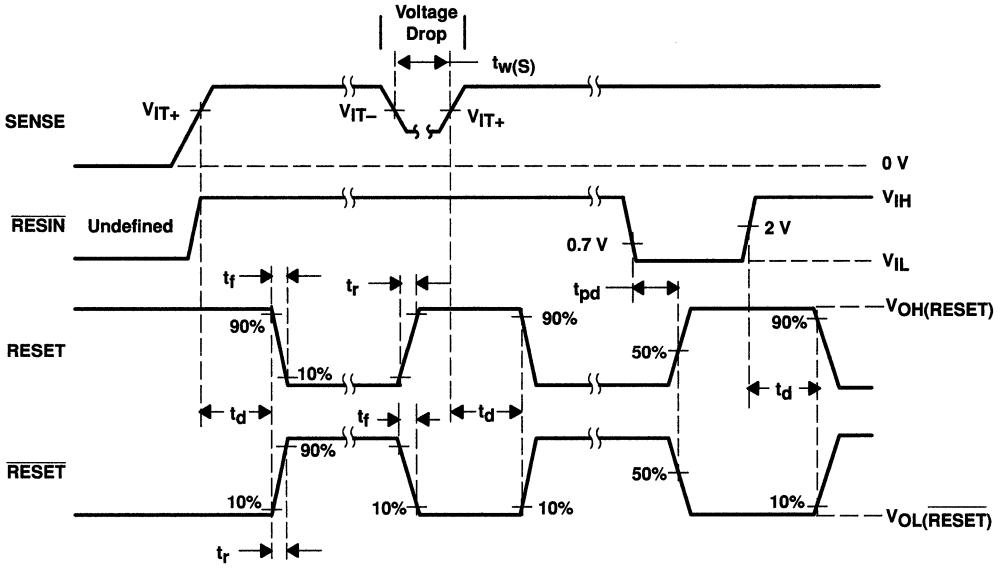


Figure 1. Voltage Waveforms

TYPICAL CHARACTERISTICS†

ASSERTION TIME vs LOAD RESISTANCE

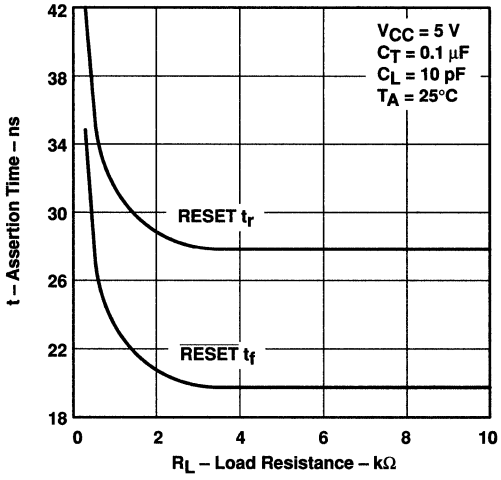


Figure 2

DEASSERTION TIME vs LOAD RESISTANCE

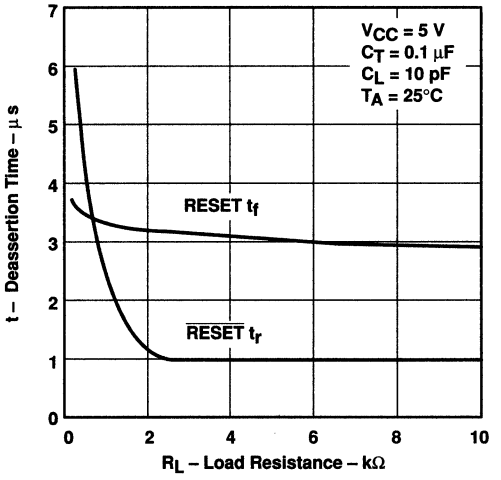


Figure 3

ASSERTION TIME vs LOAD CAPACITANCE

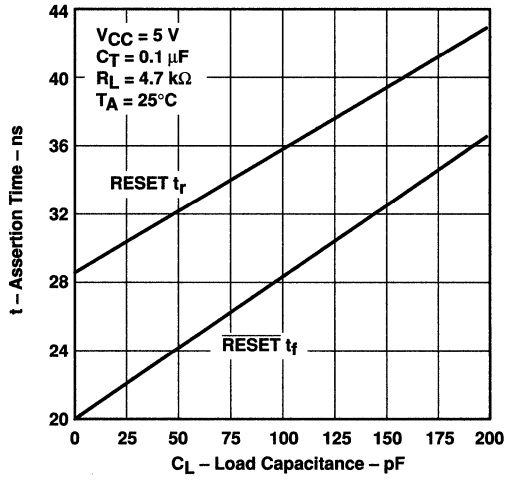


Figure 4

DEASSERTION TIME vs LOAD CAPACITANCE

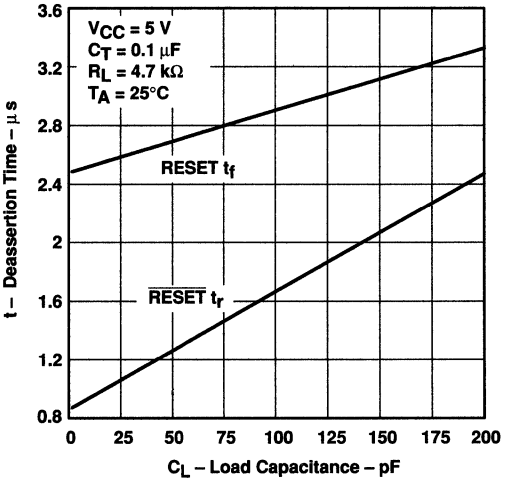


Figure 5

† For proper operation, both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

APPLICATION INFORMATION

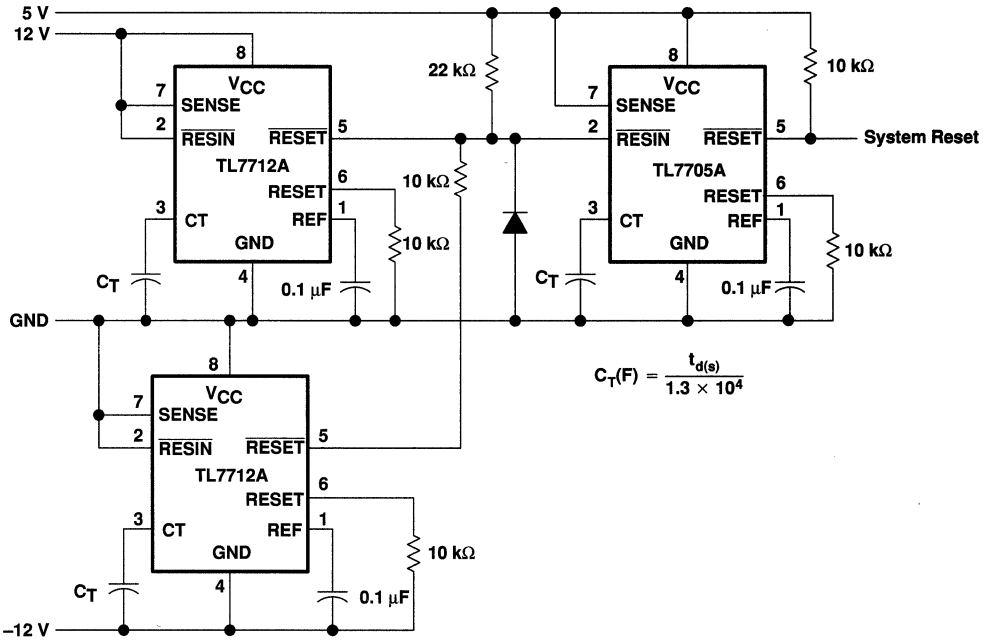


Figure 6. Multiple Power-Supply System Reset Generation

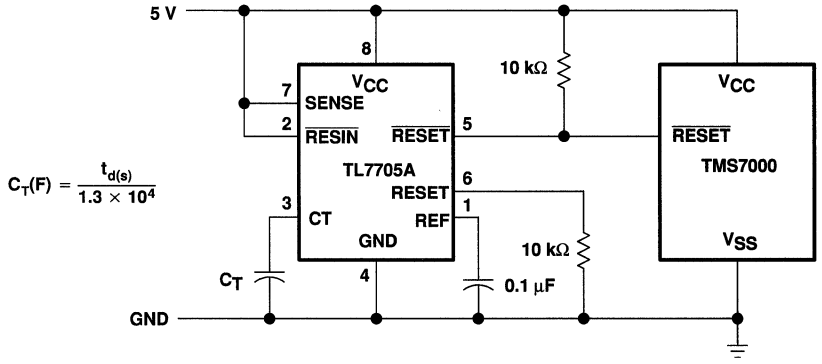


Figure 7. Reset Controller for TMS7000 System

TEXAS INSTRUMENTS
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APPLICATION INFORMATION

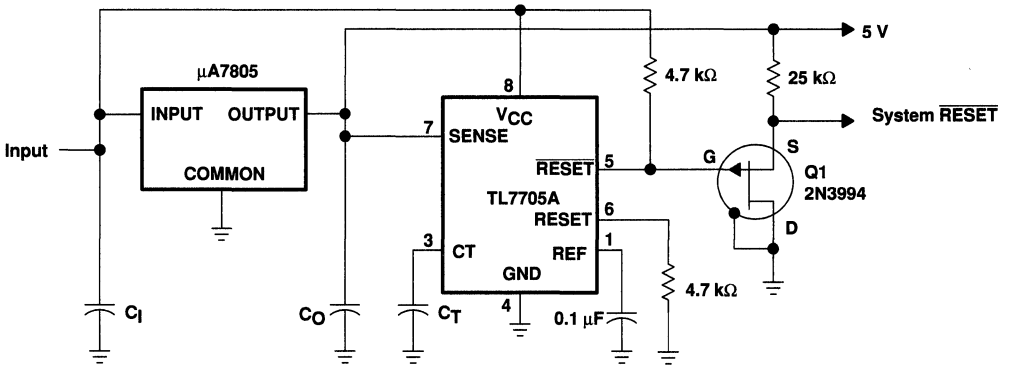


Figure 8. Eliminating Undefined States Using a P-Channel JFET

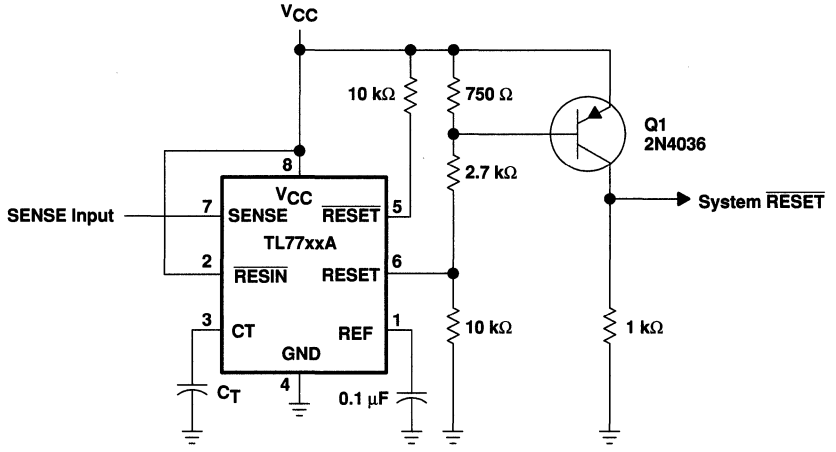
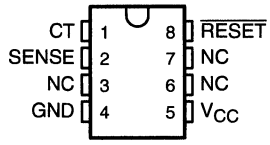


Figure 9. Eliminating Undefined States Using a pnp Transistor

SLVS220 – JULY 1999

- **Adjustable Sense Voltage With Two External Resistors**
- **Adjustable Hysteresis of Sense Voltage**
- **Wide Operating Supply-Voltage Range . . . 1.8 V to 40 V**
- **Wide Operating-Temperature Range . . . –40°C to 85°C**
- **Low Power Consumption (I_{CC} = 0.6 mA TYP, V_{CC} = 40 V)**
- **Minimum External Components**
- **Package Options Include Plastic Small-Outline (PS) Package and Standard (P) DIP**

P OR PS PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL7700 is a bipolar integrated circuit designed for use as a reset controller in microcomputer and microprocessor systems. The SENSE voltage can be set to any value greater than 0.5 V using two external resistors. The hysteresis value of the sense voltage also can be set by the same resistors. The device includes a precision voltage reference, fast comparator, timing generator, and output driver, so it can generate a power-on reset signal in a digital system.

The TL7700 has an internal 1.5-V temperature-compensated voltage reference from which all function blocks are supplied. Circuit function is very stable with supply voltage in the 1.8-V to 40-V range. Minimum supply current allows use with ac line operation, portable battery operation, and automotive applications.

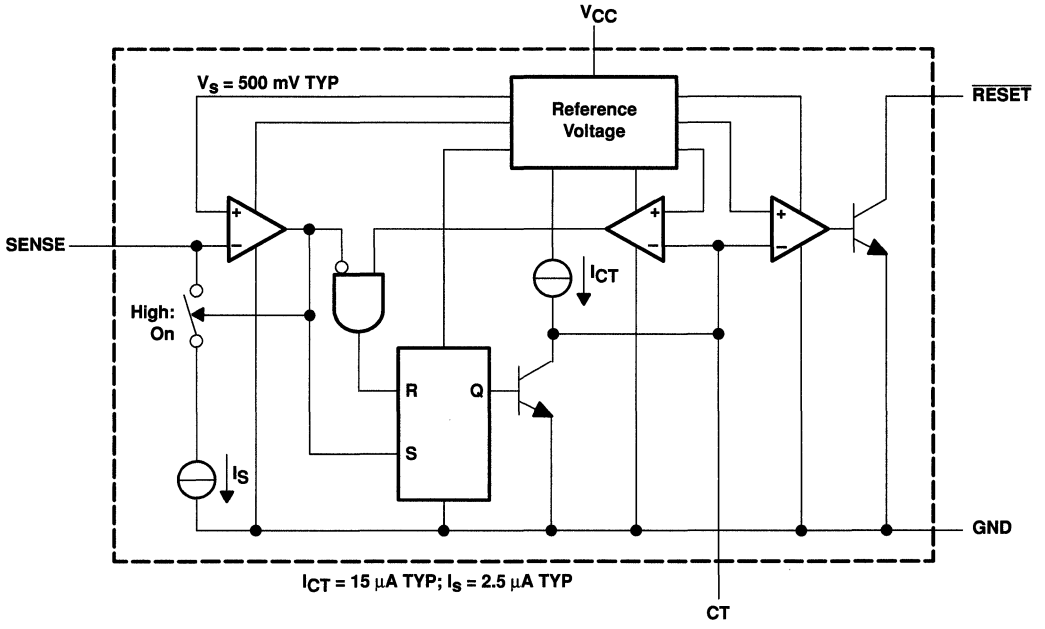
The TL7700C is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC DUAL-IN-LINE (P)	SMALL OUTLINE (PS)
–40°C to 85°C	TL7700CP	TL7700CPS

PS package is available taped and reeled. Add R suffix to device type for ordering, e.g., TL7700CPSR.

functional block diagram



Terminal Functions

TERMINAL NO.	NAME	DESCRIPTION
1	CT	Timing capacitor connection. This terminal sets the $\overline{\text{RESET}}$ output pulse width (t_{po}). It is connected internally to a 15-µA constant-current source. There is a limit on the switching speed of internal elements; even if CT is set to 0, response speeds remain at approximately 5 to 10 µs. If CT is open, the device can be used as an adjustable-threshold noninverting comparator. If CT is low, the internal output-stage comparator is active and the $\overline{\text{RESET}}$ output transistor is on. An external voltage must not be applied to this terminal due to the internal structure of the device. Therefore, drive the device using an open-collector transistor, FET, or 3-state buffer (in the low-level or high-impedance state).
2	SENSE	Voltage-sense. This terminal has a threshold level of 500 mV. The sense voltage and hysteresis can be set at the same time when the two voltage-dividing resistors are connected. The reference voltage is temperature compensated to inhibit temperature drift in the threshold voltage within the operating temperature range.
3, 6, 7	NC	No internal connection
4	GND	Ground. Keep this terminal as low impedance to reduce circuit noise.
5	V_{CC}	Power supply. This terminal is used in an operating-voltage range of 1.8 V to 40 V.
8	$\overline{\text{RESET}}$	Reset output. This terminal can be connected directly to a system that resets in the active-low state. A pullup resistor usually is required because the output is a npn open-collector transistor. An additional transistor should be connected when the active-high reset or higher output current is required.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 41 V
Sense input voltage range, V_S ..... –0.3 V to 41 V
Output voltage, V_{OH} (off state) ..... 41 V
Output current, I_{OL} (on state) ..... 5 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): P package ..... 85°C/W
PS package ..... 95°C/W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	1.8		40	V
Low-level output current, I_{OL}			3	mA
Operating free-air temperature, T_A	–40		85	°C

electrical characteristics, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_S	SENSE input voltage			495	500	505	mV
		T_A = –40°C to 85°C		490		510	
I_S	SENSE input current	V_S = 0.4 V		2	2.5	3	µA
			T_A = –40°C to 85°C	1.5		3.5	
I_{CC}	Supply current	V_{CC} = 40 V, V_S = 0.6 V, No load			0.6	1	mA
V_{OL}	Low-level output voltage	I_{OL} = 1.5 mA				0.4	V
		I_{OL} = 3 mA				0.8	
I_{OH}	High-level output current	V_{OH} = 40 V, V_S = 0.6 V, T_A = –40°C to 85°C				1	µA
I_{CT}	Timing capacitor charge current	V_S = 0.6 V		11	15	19	µA

switching characteristics, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pi}	SENSE pulse duration	C_T = 0.01 µF	2			µs
t_{po}	Output pulse duration	C_T = 0.01 µF	0.5	1	1.5	ms
t_r	Output rise time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF			15	µs
t_f	Output fall time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF			0.5	µs
t_{pd}	Propagation delay time, SENSE to output	C_T = 0.01 µF			10	µs

PARAMETER MEASUREMENT INFORMATION

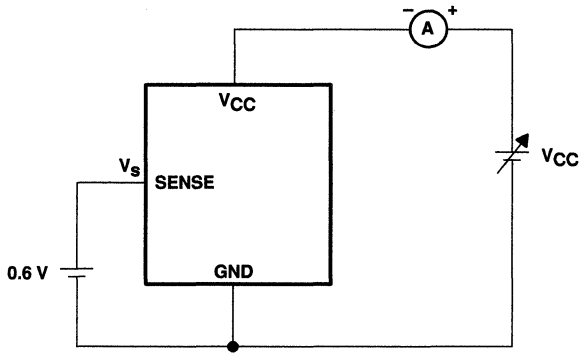


Figure 1. V_{CC} vs I_{CC} Measurement Circuit

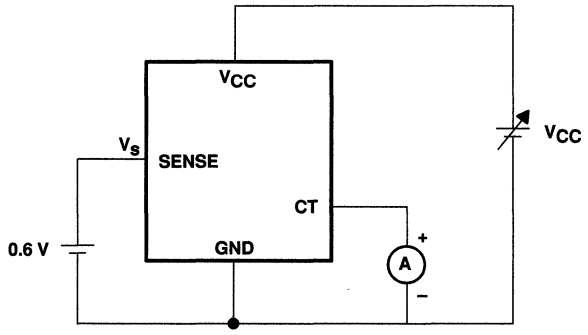


Figure 2. V_{CC} vs I_{CT}

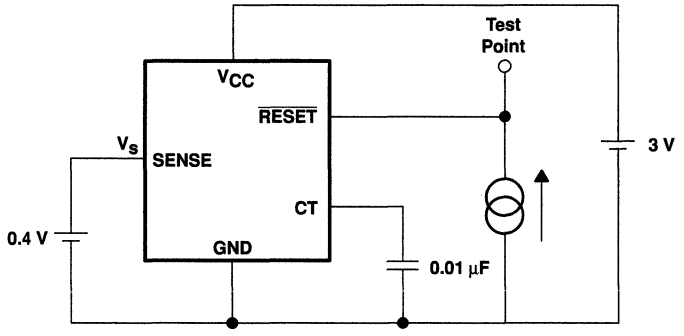


Figure 3. I_{OL} vs V_{OL}

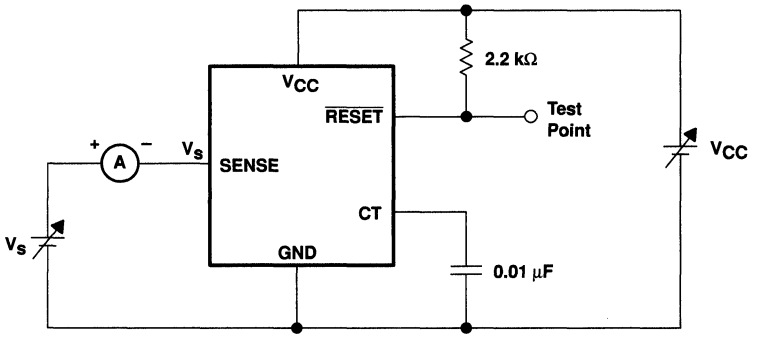


Figure 4. V_S, I_S Characteristics

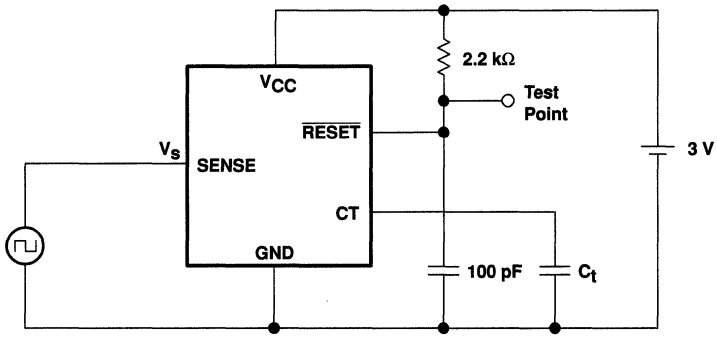


Figure 5. Switching Characteristics

TYPICAL CHARACTERISTICS

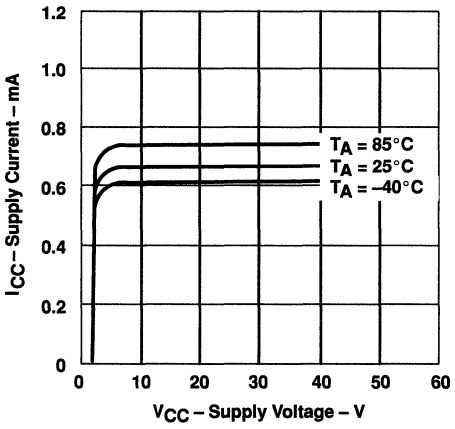


Figure 6. Supply Current vs Supply Voltage

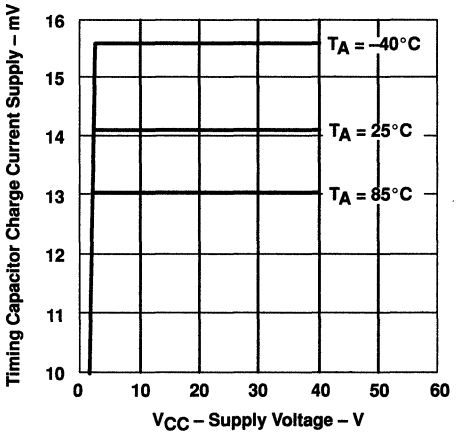


Figure 7. Timing Capacitor Charge Current vs Supply Voltage

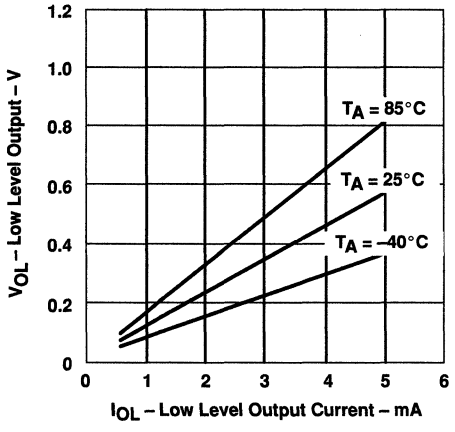


Figure 8. I_{OL} vs V_{OL} Characteristics

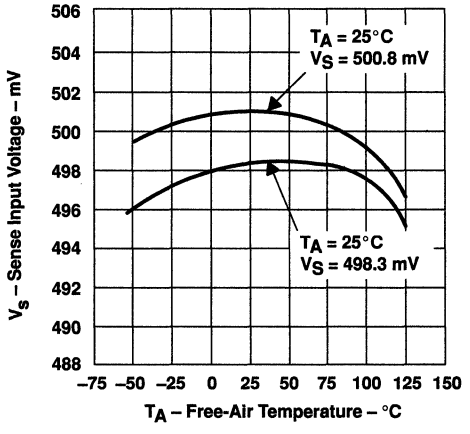


Figure 9. Timing Capacitor Charge Current vs Supply Voltage

TYPICAL CHARACTERISTICS

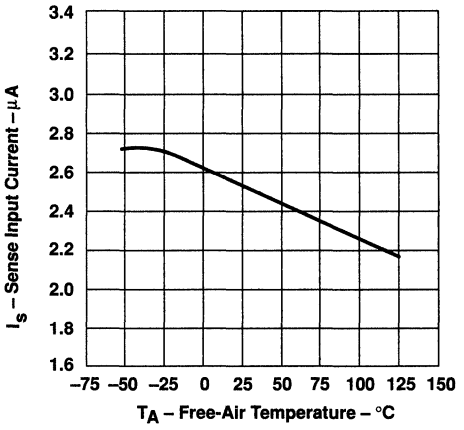


Figure 10. Sense Input Current vs Temperature

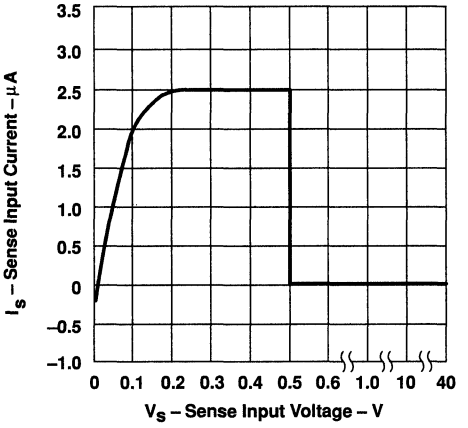


Figure 11. V_S vs I_S Characteristics

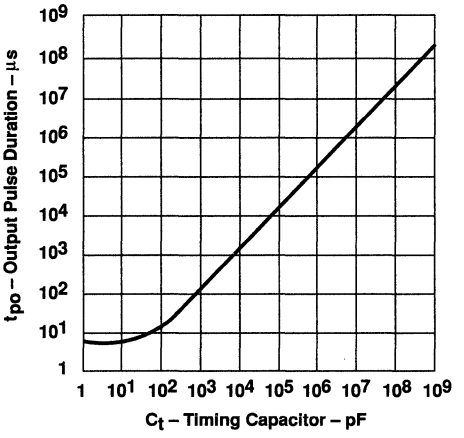


Figure 12. Timing Capacitor vs Output Pulse Duration

TYPICAL CHARACTERISTICS

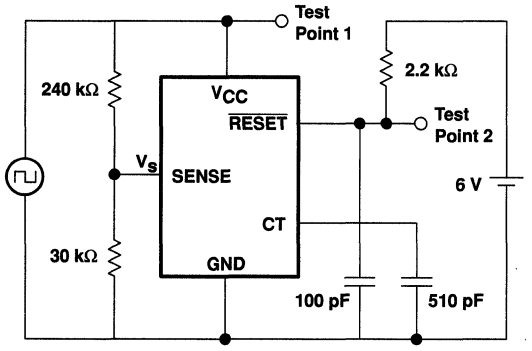


Figure 13. V_{CC} vs Output Test Circuit 1

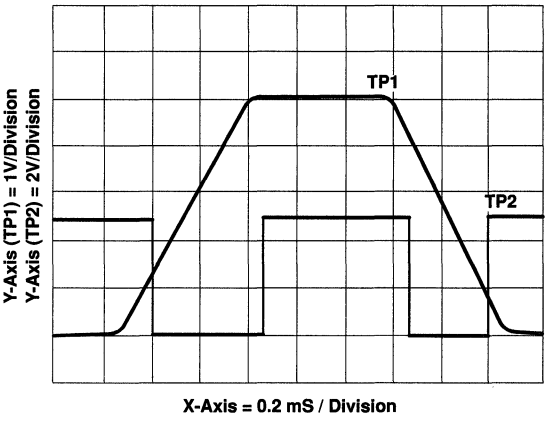


Figure 14. V_{CC} vs Output Waveform 1

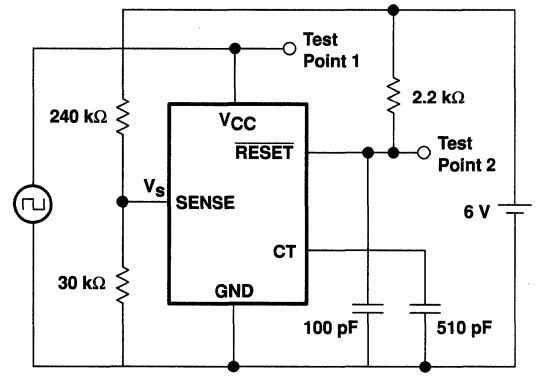


Figure 15. V_{CC} vs Output Test Circuit 2

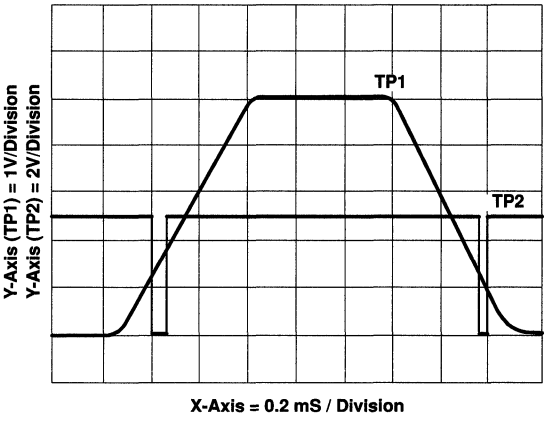


Figure 16. V_{CC} vs Output Waveform 2

TYPICAL CHARACTERISTICS

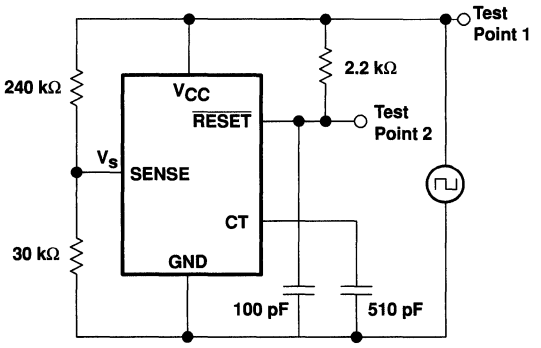


Figure 17. V_{CC} vc Output Test Circuit 3

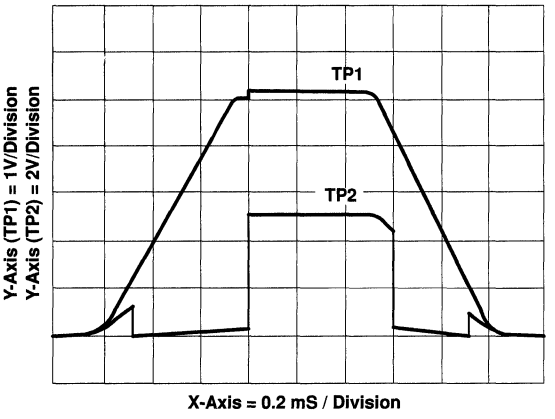


Figure 18. V_{CC} vs Output Waveform 3

detailed description

sense voltage setting

The sense voltage, V_S, of the TL7700 is typically 500 mV. By applying two external resistors, the circuit designer can obtain any sense voltage over 500 mV. In Figure 19, the sensing voltage, V's, is calculated as follows:

$$V's = V_S \times (R1 + R2)/R2$$

Where:

V_S = 500 mV, typically at T_A = 25°C

At room temperature, V_S has a variation of 500 mV ±5 mV. In the basic circuit shown in Figure 19, variations of [±5 × (R1 + R2)/R2] mV are superimposed on V_S.

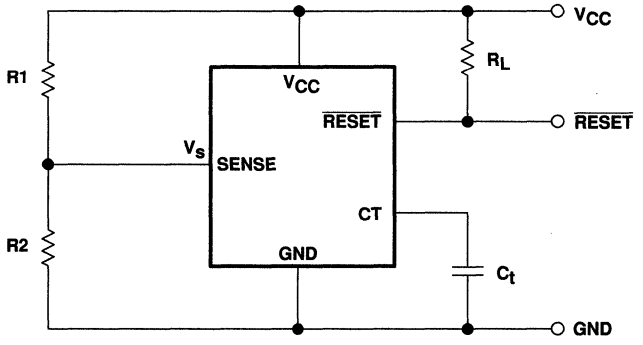


Figure 19.

sense voltage hysteresis setting

If the sense voltage, V_S, does not have hysteresis in it and the voltage on the sensing line contains ripples, the resetting of TL7700 will be unstable. Hysteresis is added to the sense voltage to prevent such problems. As shown in Figure 20, the hysteresis, V_{hys}, is added, and the value is determined as follows:

$$V_{hys} = I_S \times R1$$

Where:

$I_S = 2.5\ \mu A$, typically at $T_A = 25°C$

At room temperature, I_S has variations of $2.5 \pm 0.5\ \mu A$, so in the circuit shown in Figure 19, V_{hys} has variations of $(\pm 0.5 \times R1)\ \mu V$. In circuit design, it is necessary to consider the voltage-dividing resistor tolerance and temperature coefficient in addition to variations in V_S and V_{hys}.

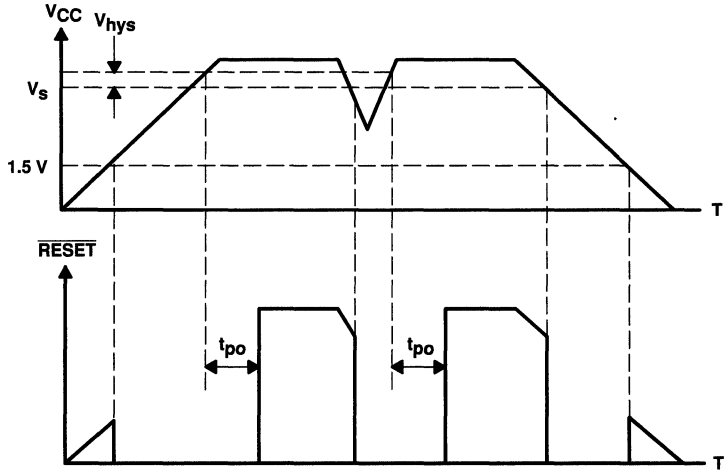


Figure 20. V_{CC}-RESET Timing Chart

output pulse duration setting

Constant-current charging starts on the timing capacitor when the sensing-line voltage reaches the TL7700's sense voltage. When the capacitor voltage exceeds the threshold level of the output drive comparator, $\overline{\text{RESET}}$ changes from a low to a high level. The output pulse duration is the time between the point when the sense-pin voltage exceeds the threshold level and the point when the $\overline{\text{RESET}}$ output changes from a low level to a high level. When the TL7700 is used for system power-on reset, the output pulse duration, t_{po}, must be set longer than the power rise time. The value of t_{po} is:

$$t_{po} = C_t \times 10^5 \text{ seconds}$$

Where:

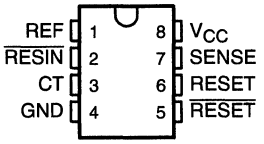
C_t is the timing capacitor in farads

There is a limit on the device response speed; even if $C_t = 0$, t_{po} will not be 0, but approximately 5 to 10 µs. Therefore, when the TL7700 is used as a comparator with hysteresis, without connecting C_t, switching speeds (t_r/t_f, t_{po}/t_{pd}, etc.) must be considered.

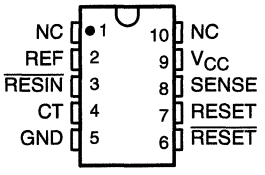
SLVS037H – SEPTEMBER 1989 – REVISED JULY 1999

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **$\overline{\text{RESET}}$ Output Defined From $V_{CC} \geq 1$ V**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

TL77xxBC . . . D OR P PACKAGE
TL7705BM . . . JG PACKAGE
TL7705BQ . . . D PACKAGE
(TOP VIEW)

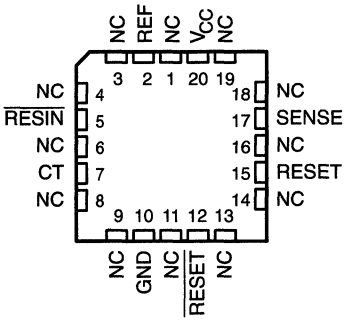


TL7705BM . . . U PACKAGE
(TOP VIEW)



NC – No internal connection

TL7705BM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL7702B and TL7705B are integrated-circuit supply-voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

An external capacitor (typically 0.1 μF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL7702BC and TL7705BC are characterized for operation from 0°C to 70°C. The TL7702BI and TL7705BI are characterized for operation from –40°C to 85°C. The TL7705BQ is characterized for operation from –40°C to 125°C. The TL7705BM is characterized for operation from –55°C to 125°C.

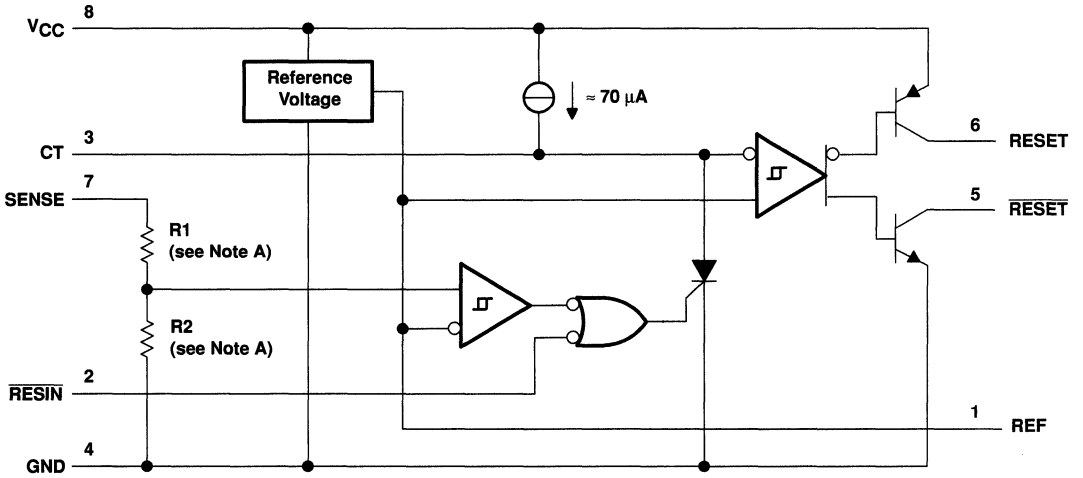
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES					CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CERAMIC FLATPACK (U)	
0°C to 70°C	TL7702BCD	—	—	TL7702BCP	—	TL7702BY, TL7705BY
	TL7705BCD	—	—	TL7705BCP	—	
–40°C to 85°C	TL7702BID	—	—	TL7702BIP	—	
	TL7705BID	—	—	TL7705BIP	—	
–40°C to 125°C	TL7705BQD	—	—	—	—	
–55°C to 125°C	—	TL7702BMFK	TL7702BMJG	—	TL7702BMU	
	—	TL7705BMFK	TL7705BMJG	—	TL7705BMU	

The D package is available taped and reeled. Add the suffix R to device type (e.g., TL7702BCDR). Chip forms are tested at 25°C.

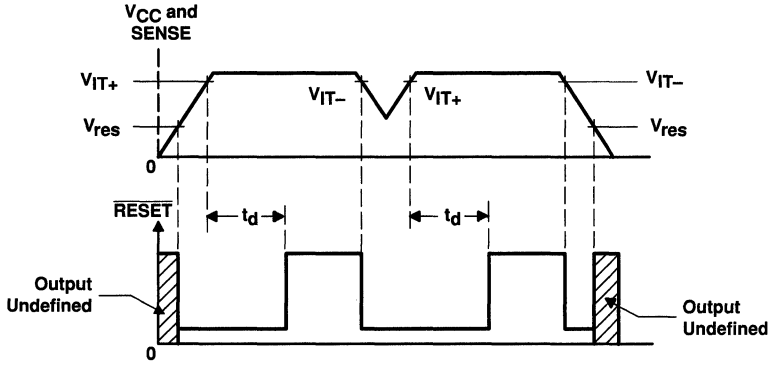
functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



Pin numbers shown are for the D, JG, and P packages.
NOTE A: TL7702B: R1 = 0 Ω, R2 = open
TL7705B: R1 = 23 kΩ, R2 = 10 kΩ, nominal

typical timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 20 V
Input voltage range, V_I: $\overline{RESIN}$ ..... –0.3 V to 20 V
SENSE ..... –0.3 V to 20 V
High-level output current, I_{OH} ($\overline{RESET}$) ..... –30 mA
Low-level output current, I_{OL} ($\overline{RESET}$) ..... 30 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package ..... 97°C/W
P package ..... 127°C/W
Case temperature for 60 seconds, T_C: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or U packages ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P packages ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.6	18	V
High-level input voltage, V_{IH}	$\overline{RESIN}$	2	18	V
Low-level input voltage, V_{IL}	$\overline{RESIN}$	0	0.8	V
Input voltage, V_I	SENSE	0	18	V
High-level output current, I_{OH}	RESET		–16	mA
Low-level output current, I_{OL}	$\overline{RESET}$		16	mA
Operating free-air temperature range, T_A	TL770xBC	0	70	°C
	TL770xBI	–40	85	
	TL7705BQ	–40	125	
	TL7705BM	–55	125	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS†		TL77xxBC TL77xxBI TL7705BQ			UNIT
						MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET			I_{OH} = –16 mA		V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{RESET}$			I_{OL} = 16 mA				0.4	V
V_{ref}	Reference voltage			I_{ref} = 500 µA,	T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage at SENSE input		TL7702B	T_A = 25°C		2.505	2.53	2.555	V
			TL7705B			4.5	4.55	4.6	
			TL7702B	T_A = full range‡		2.48	2.53	2.58	
			TL7705B			4.45	4.55	4.65	
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)		TL7702B	V_{CC} = 3.6 V to 18 V,	T_A = 25°C		10		mV
			TL7705B				30		
V_{res}§	Power-up reset voltage			I_{OL} at $\overline{RESET}$ = 2 mA,	T_A = 25°C			1	V
I_I	Input current	$\overline{RESIN}$		V_I = 0.4 V to V_{CC}				–10	µA
		SENSE	TL7702B	V_I = V_{ref} to 18 V			–0.1	–2	
I_{OH}	High-level output current, $\overline{RESET}$			V_O = 18 V,	See Figure 1			50	µA
I_{OL}	Low-level output current, RESET			V_O = 0 V,	See Figure 1			–50	µA
I_{CC}	Supply current			V_{SENSE} = 15 V,	$\overline{RESIN}$ ≥ 2 V		1.8	3	mA
				V_{CC} = 18 V,	T_A = full range‡			3.5	mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.
‡ Full range is 0°C to 70°C for the C-suffix devices, –40°C to 85°C for the I-suffix devices, and –40°C to 125°C for the Q-suffix device.
§ This is the lowest voltage at which $\overline{RESET}$ becomes active.

switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL77xxBC TL77xxBI TL7705BQ			UNIT
					MIN	TYP	MAX	
t_{PLH}	Propagation delay time from low- to high-level output	$\overline{RESIN}$	RESET	See Figures 1, 2, and 3		270	500	ns
t_{PHL}	Propagation delay time from high- to low-level output	$\overline{RESIN}$	$\overline{RESET}$			270	500	ns
t_w	Effective pulse duration	$\overline{RESIN}$		See Figure 2		150		ns
		SENSE				100		
t_r	Rise time		RESET	See Figures 1 and 3			75	ns
t_f	Fall time					150	200	
t_r	Rise time		$\overline{RESET}$			75	150	ns
t_f	Fall time						50	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS†		TL7705BM			UNIT
						MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, RESET			I_{OH} = –16 mA		V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{RESET}$			I_{OL} = 16 mA				0.4	V
V_{ref}	Reference voltage			I_{ref} = 500 µA,	T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage at SENSE input		TL7702B	T_A = 25°C		2.505	2.53	2.555	V
			TL7705B			4.5	4.55	4.6	
			TL7702B	T_A = –55°C to 125°C		2.48	2.53	2.58	
			TL7705B			4.45	4.55	4.65	
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)		TL7702B	V_{CC} = 3.6 V to 18 V,	T_A = 25°C		10		mV
			TL7705B				30		
V_{res}‡	Power-up reset voltage			I_{OL} at $\overline{RESET}$ = 2 mA,	T_A = 25°C			1	V
I_I	Input current	$\overline{RESIN}$		V_I = 0.4 V to V_{CC}				–10	µA
		SENSE	TL7702B	V_I = V_{ref} to V_{CC} – 1.5 V			–0.1	–2	
I_{OH}	High-level output current, $\overline{RESET}$			V_O = 18 V				50	µA
I_{OL}	Low-level output current, RESET			V_O = 0				–50	µA
I_{CC}	Supply current			V_{SENSE} = 15 V,	$\overline{RESIN}$ ≥ 2 V		1.8	3	mA
				V_{CC} = 18 V,	T_A = –55°C to 125°C			4	

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.
‡ This is the lowest value at which $\overline{RESET}$ becomes active.

switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7705BM			UNIT
					MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time from low- to high-level output	$\overline{RESIN}$	RESET	See Figures 1, 2, and 3		270	500*	ns
t_{PHL}	Propagation delay time from high- to low-level output	$\overline{RESIN}$	$\overline{RESET}$			270	500*	ns
t_w	Effective pulse duration	$\overline{RESIN}$		See Figure 2		150		ns
		SENSE				100		
t_r	Rise time		RESET	See Figures 1 and 3			75*	ns
t_f	Fall time					150	200*	
t_r	Rise time		$\overline{RESET}$			75	150*	ns
t_f	Fall time						50*	

* On products compliant to MIL-PRF-38535, these parameters are not production tested.

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

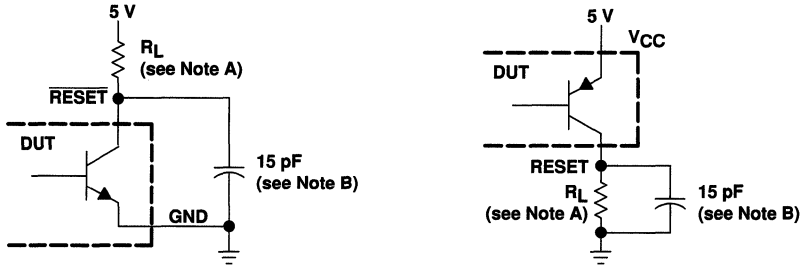
PARAMETER				TEST CONDITIONS†		TL7702BY TL7705BY			UNIT
						MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET			I_{OH} = –16 mA		V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$			I_{OL} = 16 mA				0.4	V
V_{ref}	Reference voltage			I_{ref} = 500 µA		2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage at SENSE input		TL7702BY			2.505	2.53	2.555	V
			TL7705BY			4.5	4.55	4.6	
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)		TL7702BY	V_{CC} = 3.6 V to 18 V			10		mV
			TL7705BY				30		
V_{res}‡	Power-up reset voltage			I_{OL} at $\overline{\text{RESET}}$ = 2 mA				1	V
I_I	Input current	$\overline{\text{RESIN}}$		V_I = 0.4 V to V_{CC}				–10	µA
		SENSE	TL7702BY	V_I = V_{ref} to 18 V			–0.1	–2	
I_{OH}	High-level output current, $\overline{\text{RESET}}$			V_O = 18 V,	See Figure 1			50	µA
I_{OL}	Low-level output current, RESET			V_O = 0 V,	See Figure 1			–50	µA
I_{CC}	Supply current			V_{SENSE} = 15 V,	$\overline{\text{RESIN}} \geq$ 2 V		1.8	3	mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7702BY TL7705BY			UNIT
					MIN	TYP	MAX	
t_{PLH}	Propagation delay time from low- to high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1, 2, and 3		270	500	ns
t_{PHL}	Propagation delay time from high- to low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$			270	500	ns
t_w	Effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2		150		ns
		SENSE				100		
t_r	Rise time		RESET	See Figures 1 and 3			75	ns
t_f	Fall time					150	200	
t_r	Rise time		$\overline{\text{RESET}}$			75	150	ns
t_f	Fall time						50	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. For I_{OL} and I_{OH}, R_L = 10 kΩ. For all switching characteristics, R_L = 511 Ω.
B. This figure includes jig and probe capacitance.

Figure 1. RESET and $\overline{\text{RESET}}$ Output Configurations

Figure 2. Input Pulse Definition

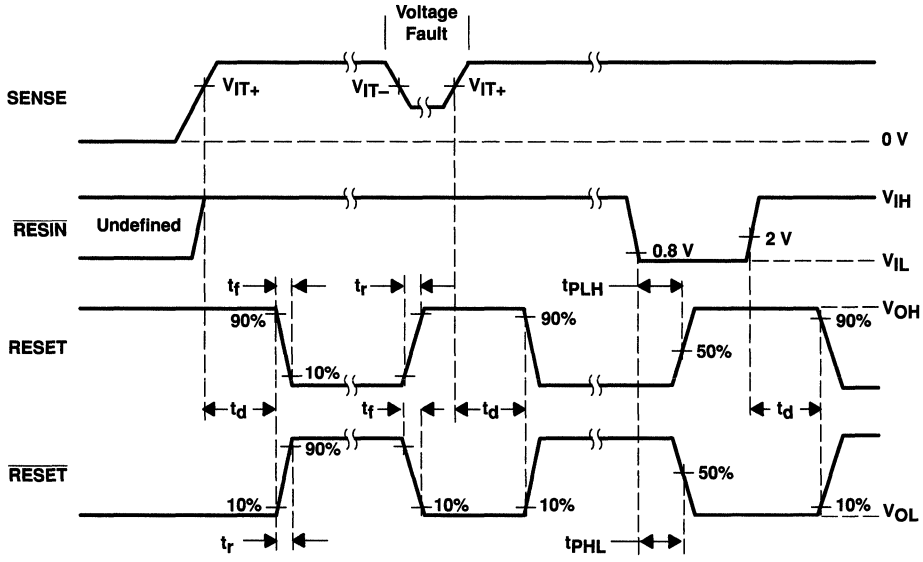


Figure 3. Voltage Waveforms

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS†

ASSERTION TIME vs LOAD RESISTANCE

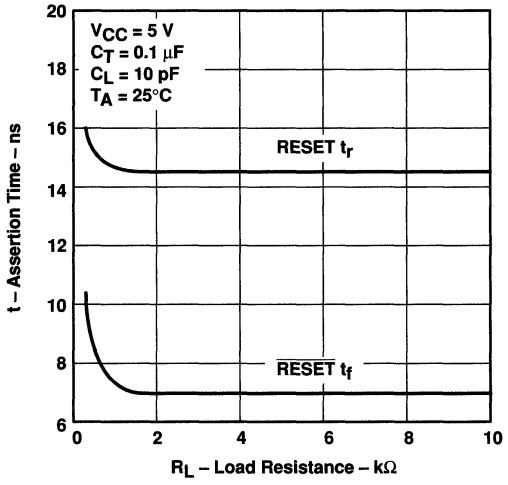


Figure 4

DEASSERTION TIME vs LOAD RESISTANCE

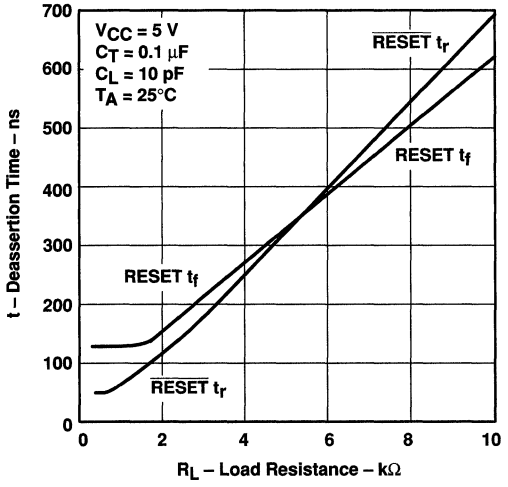


Figure 5

ASSERTION TIME vs LOAD CAPACITANCE

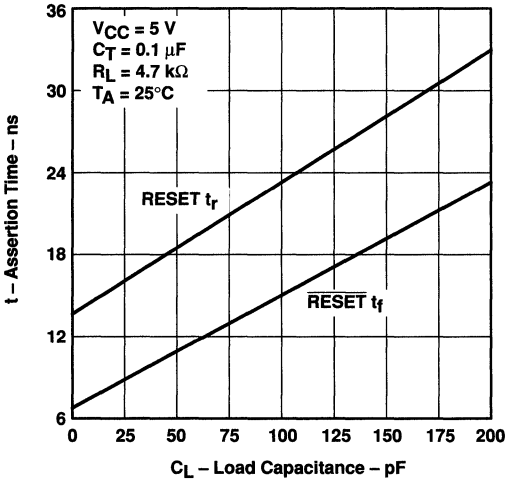


Figure 6

DEASSERTION TIME vs LOAD CAPACITANCE

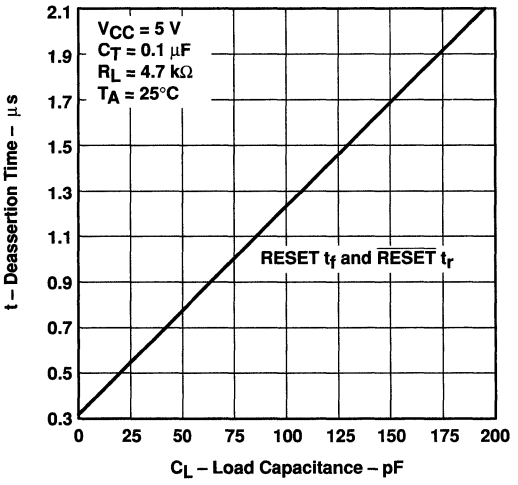


Figure 7

† For proper operation, both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

APPLICATION INFORMATION

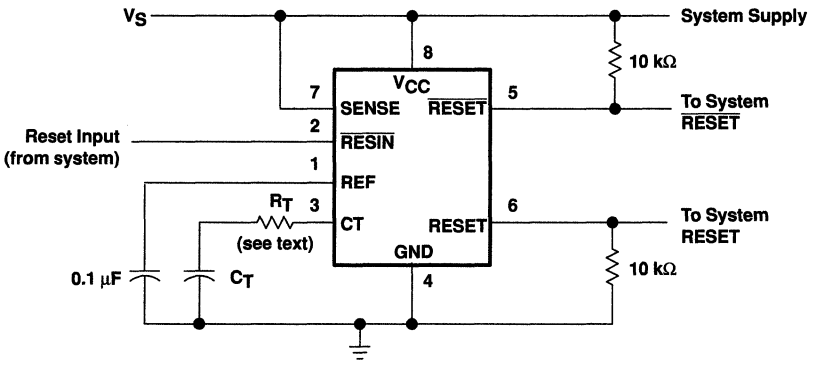


Figure 8. System Reset Controller With Undervoltage Sensing

When the TL770xB SENSE terminal is used to monitor V_{CC}, a current-limiting resistor in series with C_T is recommended. During normal operation, the timing capacitor is charged by the onboard current source to approximately V_{CC} or an internal voltage clamp (≈7.1-V zener), whichever is less. When the circuit is then subjected to an undervoltage condition during which V_{CC} is rapidly slewed down, the voltage on CT exceeds that on V_{CC}. This forward biases a secondary path internally, which falsely activates the outputs. A fault is indicated when V_{CC} drops below $V_{(CT)}$, not when V_{SENSE} falls below V_{T-}.

Texas Instruments performs a 100% electrical screen to verify that the outputs do not switch with 1 mA forced into the CT terminal. Adding the external resistor, R_T, prevents false triggering. Its value is calculated as follows:

$$\frac{V_{(CT)} - V_{T-}}{R_T}$$

Where:

$V_{(CT)}$ = V_{CC} or 7.1 V, whichever is less
V_{T-} = 4.55 V (nom)
R_T = value of series resistor required

For V_{CC} = 5 V:

$$\frac{5 - 4.55}{R_T} < 1 \text{ mA}$$

Therefore,

$$R_T > 450\ \Omega$$

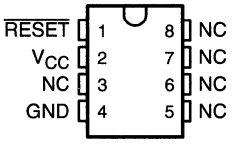
Using a 20% tolerance resistor, R_T should be greater than 560 Ω.

Adding this series resistor changes the duration of the reset pulse by no more than 10%. R_T extends the discharge of C_T, but also skews the $V_{(CT)}$ threshold. These effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent upon the duration of the supply-voltage fault condition.

Both outputs of the TL770xB should be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset.

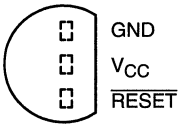
- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Low Standby Current . . . 20 μA**
- **Reset Output Defined When V_{CC} Exceeds 1 V**
- **Complementary Reset Output**
- **True and Complementary Reset Outputs**
- **Precision Threshold Voltage 4.55 V ±120 mV**
- **High Output Sink Capability . . . 20 mA**
- **Comparator Hysteresis Prevents Erratic Resets**

D PACKAGE
(TOP VIEW)

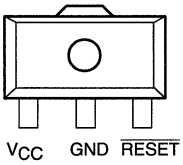


NC–No internal connection

LP PACKAGE
(TOP VIEW)



PK PACKAGE
(TOP VIEW)



GND is in electrical contact with the tab.

description

The TL7757 is a supply-voltage supervisor designed for use in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power up, when the supply voltage, V_{CC}, attains a value approaching 1 V, the $\overline{RESET}$ output becomes active (low) to prevent undefined operation. If the supply voltage drops below threshold voltage level (V_{IT-}), the $\overline{RESET}$ output goes to the active (low) level until the supply undervoltage fault condition is eliminated.

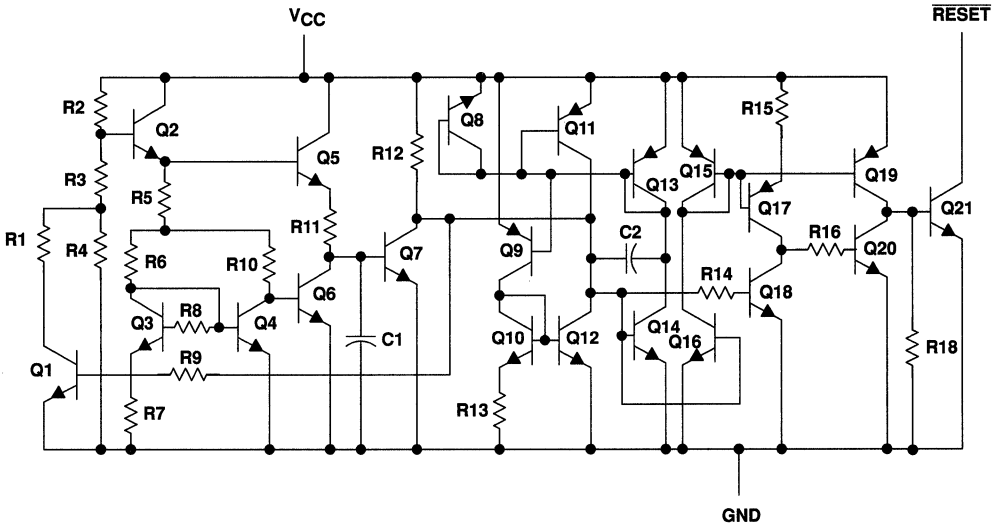
The TL7757C is characterized for operation from 0°C to 70°C. The TL7757I is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL OUTLINE (D)	TO-226AA (LP)	SOT-89 (PK)	
0°C to 70°C	TL7757CD	TL7757CLP	TL7757CPK	TL7757Y
–40°C to 85°C	TL7757ID	TL7757ILP	TL7757IPK	

D and LP packages are available taped and reeled. Add the suffix R to device type (e.g., TL7757CDR). Chip forms are tested at 25°C.

equivalent schematic



ACTUAL DEVICE COMPONENT COUNT	
Transistors	27
Resistors	20
Capacitors	2

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –0.3 V to 20 V
Offstate output voltage range (see Note 1) ..... –0.3 V to 20 V
Output current, I_O ..... 30 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package ..... 97°C/W
LP package ..... 156°C/W
PK package ..... 52°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network terminal ground.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		1	7	V
High-level output voltage, V_{OH}			15	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	TL7757C	0	70	°C
	TL7757I	–40	85	

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A	TL7757C			UNIT
				MIN	TYP	MAX	
V_{IT-}	Negative-going input threshold voltage at V_{CC}		25°C	4.43	4.55	4.67	V
			0°C to 70°C	4.4		4.7	
V_{hys}†	Hysteresis at V_{CC}		25°C	40	50	60	mV
			0°C to 70°C	30		70	
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V	25°C		0.4	0.8	V
			0°C to 70°C			0.8	
I_{OH}	High-level output current	V_{CC} = 7 V, V_{OH} = 15 V, See Figure 1	25°C			1	μA
			0°C to 70°C			1	
V_{res}‡	Power-up reset voltage	R_L = 2.2 kΩ, V_{CC} slew rate ≤ 5 V/μs	25°C		0.8	1	V
			0°C to 70°C			1.2	
I_{CC}	Supply current	V_{CC} = 4.3 V	25°C		1400	2000	μA
			0°C to 70°C			2000	
		V_{CC} = 5.5 V	0°C to 70°C			40	

† This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A	TL7757C			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC} slew rate ≤ 5 V/μs, See Figures 2 and 3	25°C		3.4	5	μs
			0°C to 70°C			5	
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3	25°C		2	5	μs
			0°C to 70°C			5	
t_r	Rise time	V_{CC} slew rate ≤ 5 V/μs, See Figures 2 and 3	25°C		0.4	1	μs
			0°C to 70°C			1	
t_f	Fall time	See Figures 2 and 3	25°C		0.05	1	μs
			0°C to 70°C			1	
$t_{w(min)}$	Minimum pulse duration at V_{CC} for output response		25°C			5	μs
			0°C to 70°C			5	

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A	TL7757I			UNIT
				MIN	TYP	MAX	
V_{IT-}	Negative-going input threshold voltage at V_{CC}		25°C	4.43	4.55	4.67	V
			–40°C to 85°C	4.4		4.7	
V_{hys}†	Hysteresis at V_{CC}		25°C	40	50	60	mV
			–40°C to 85°C	30		70	
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V	25°C		0.4	0.8	V
			–40°C to 85°C			0.8	
I_{OH}	High-level output current	V_{CC} = 7 V, V_{OH} = 15 V, See Figure 1	25°C			1	µA
			–40°C to 85°C			1	
V_{res}‡	Power-up reset voltage	R_L = 2.2 kΩ, V_{CC} slew rate ≤ 5 V/µs	25°C		0.8	1	V
			–40°C to 85°C			1.2	
I_{CC}	Supply current	V_{CC} = 4.3 V	25°C		1400	2000	µA
			–40°C to 85°C			2100	
		V_{CC} = 5.5 V	–40°C to 85°C			40	

† This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A	TL7757I			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC} slew rate ≤ 5 V/µs, See Figures 2 and 3	25°C		3.4	5	µs
			–40°C to 85°C			5	
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3	25°C		2	5	µs
			–40°C to 85°C			5	
t_r	Rise time	V_{CC} slew rate ≤ 5 V/µs, See Figures 2 and 3	25°C		0.4	1	µs
			–40°C to 85°C			1	
t_f	Fall time	See Figures 2 and 3	25°C		0.05	1	µs
			–40°C to 85°C			1	
$t_{w(min)}$	Minimum pulse duration at V_{CC} for output response		25°C			5	µs
			–40°C to 85°C			5	

electrical characteristics at T_A = 25°C

PARAMETER		TEST CONDITIONS	TL7757Y			UNIT
			MIN	TYP	MAX	
V_{IT-}	Negative-going input threshold voltage at V_{CC}			4.55		V
V_{hys}†	Hysteresis at V_{CC}			50		mV
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V		0.4		V
I_{OH}	High-level output current	V_{CC} = 7 V, V_{OH} = 15 V, See Figure 1				µA
V_{res}‡	Power-up reset voltage	R_L = 2.2 kΩ, V_{CC} slew rate ≤ 5 V/µs		0.8		V
I_{CC}	Supply current	V_{CC} = 4.3 V		1400		µA
		V_{CC} = 5.5 V				

† This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics at T_A = 25°C

PARAMETER		TEST CONDITIONS	TL7757Y			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC} slew rate ≤ 5 V/µs, See Figures 2 and 3		3.4		µs
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3		2		µs
t_r	Rise time	V_{CC} slew rate ≤ 5 V/µs, See Figures 2 and 3		0.4		µs
t_f	Fall time	See Figures 2 and 3		0.05		µs

PARAMETER MEASUREMENT INFORMATION

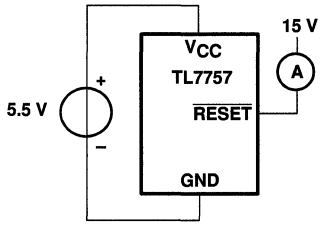
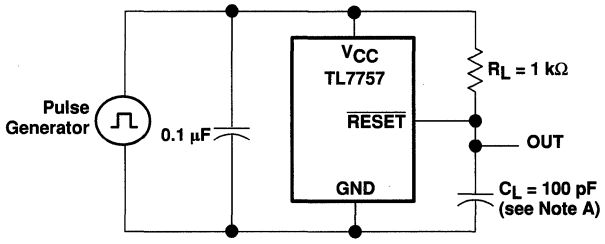
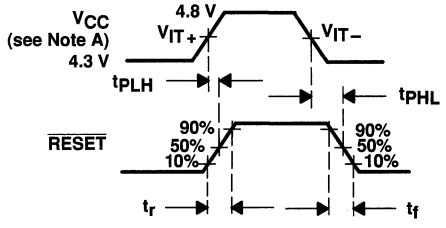


Figure 1. Test Circuit for Output Leakage Current



NOTE A: Includes jig and probe capacitance.

Figure 2. Test Circuit for $\overline{\text{RESET}}$ Output Switching Characteristics



NOTE A: V_{CC} slew rate ≤ 5 μs

Figure 3. Switching Diagram

TYPICAL CHARACTERISTICS†

Table of Graphs

		FIGURE
V_{CC}	Supply voltage vs $\overline{RESET}$ output voltage	4
I_{CC}	Supply current vs Supply voltage	5
I_{CC}	Supply current vs Free-air temperature	6
V_{OL}	Low-level output voltage vs Low-level output current	7
V_{OL}	Low-level output voltage vs Free-air temperature	8
I_{OL}	Output current vs Supply voltage	9
V_{IT-}	Input threshold voltage (negative-going V_{CC}) vs Free-air temperature	10
V_{res}	Power-up reset voltage vs Free-air temperature	11
V_{res}	Power-up reset voltage and supply voltage vs Time	12
	Propagation delay time	13

SUPPLY VOLTAGE vs $\overline{RESET}$ OUTPUT VOLTAGE

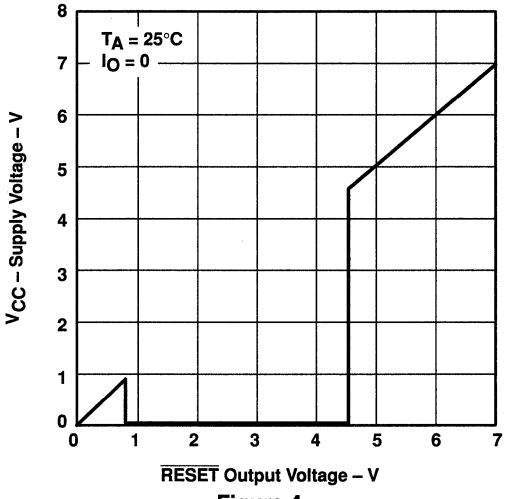


Figure 4

SUPPLY CURRENT vs SUPPLY VOLTAGE

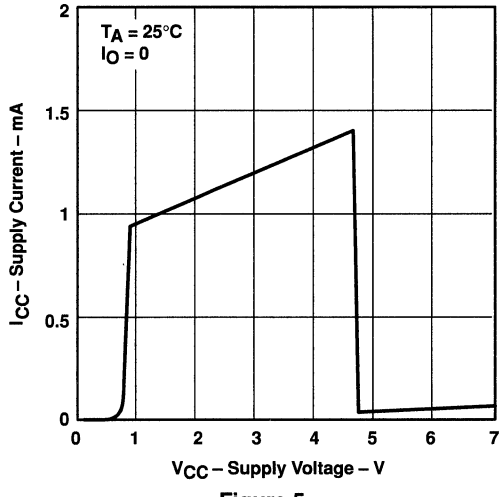


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

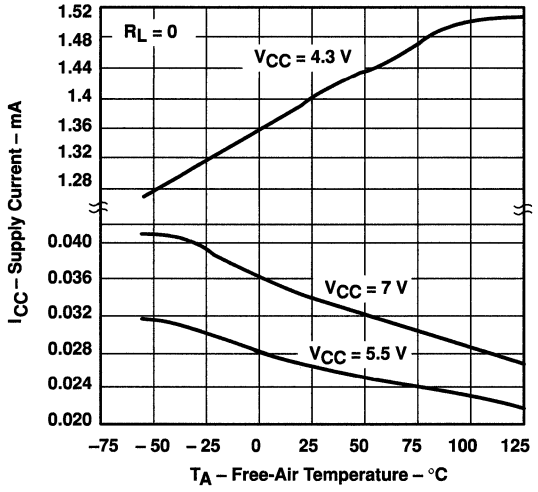


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

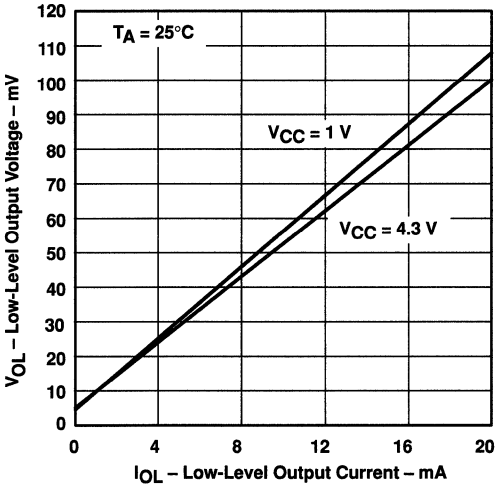


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

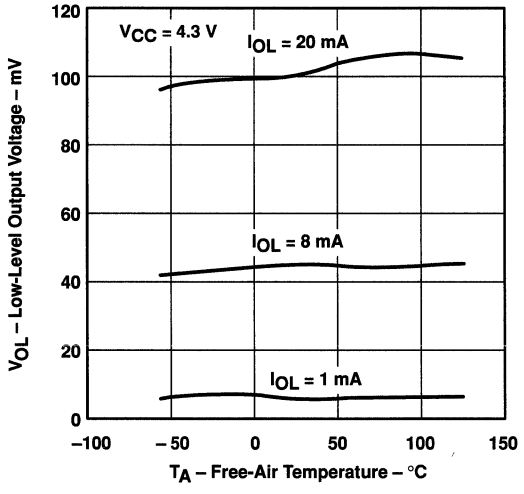


Figure 8

OUTPUT CURRENT
vs
SUPPLY VOLTAGE

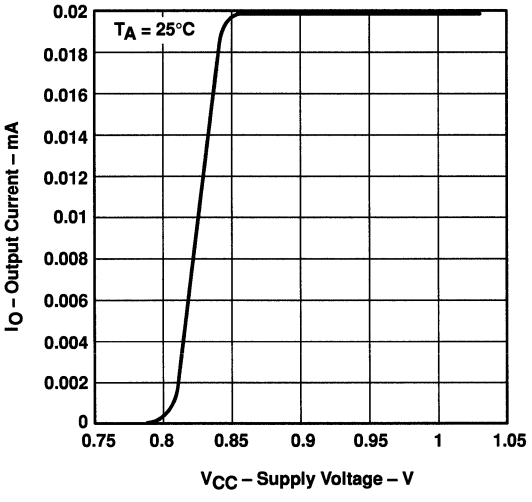


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT THRESHOLD VOLTAGE
(NEGATIVE-GOING V_{CC})
vs
FREE-AIR TEMPERATURE

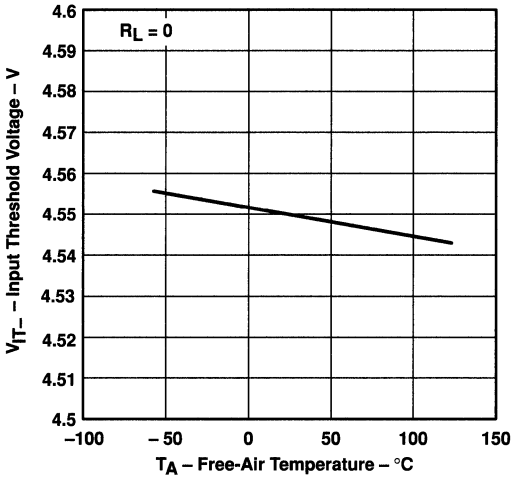


Figure 10

POWER-UP RESET VOLTAGE
vs
FREE-AIR TEMPERATURE

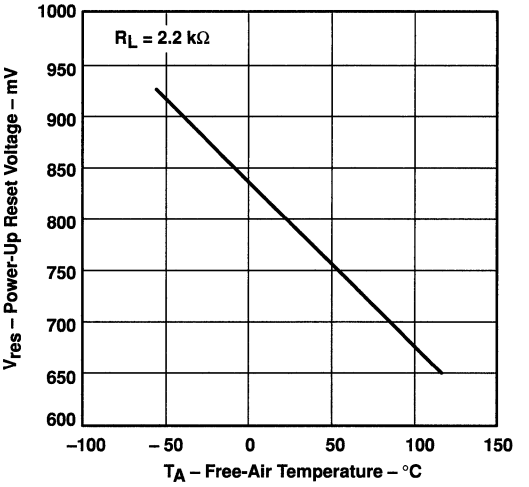


Figure 11

POWER-UP RESET VOLTAGE
AND SUPPLY VOLTAGE
vs
TIME

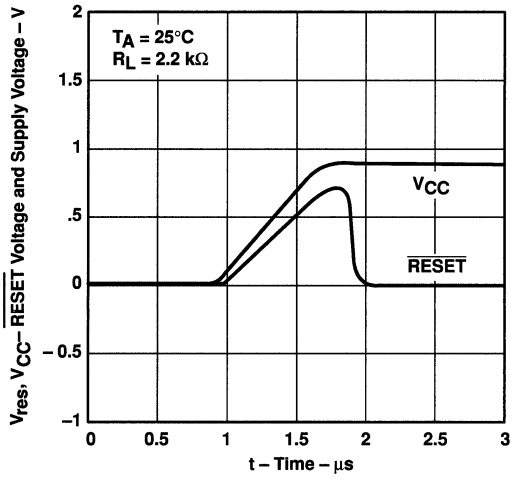


Figure 12

PROPAGATION DELAY TIME

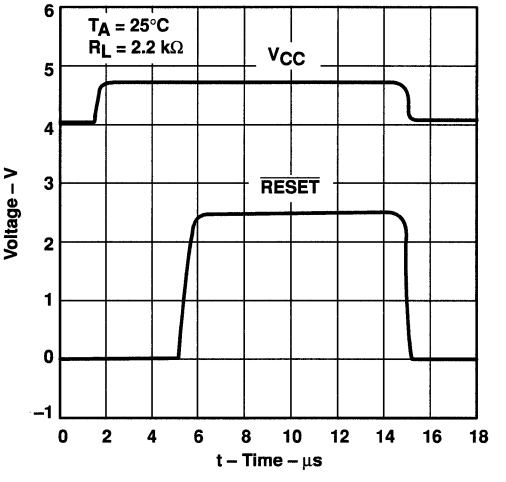
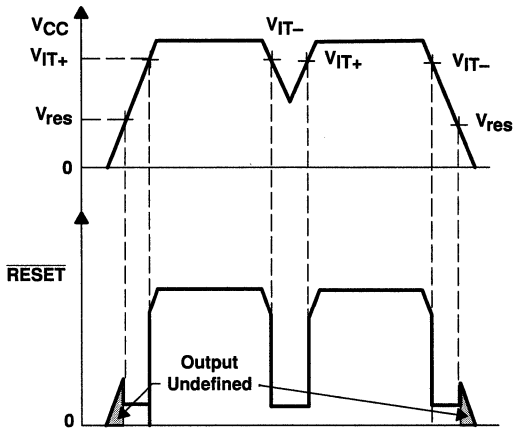


Figure 13

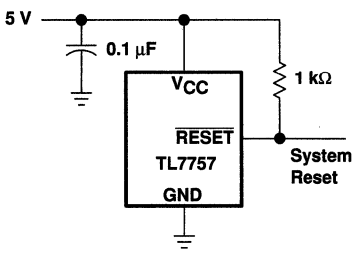
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

TYPICAL TIMING DIAGRAM



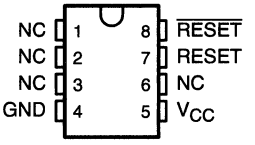
TYPICAL APPLICATION DIAGRAM



SLVS042D – JANUARY 1991 – REVISED JULY 1999

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Input Threshold Voltage . . . 4.55 V ±120 mV**
- **Low Standby Current . . . 20 μA**
- **Reset Outputs Defined When V_{CC} Exceeds 1 V**
- **True and Complementary Reset Outputs**
- **Wide Supply-Voltage Range . . . 1 V to 7 V**

D, P, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL7759 is a supply-voltage supervisor designed for use as a reset controller in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power up, when the supply voltage, V_{CC}, attains a value approaching 1 V, the RESET and $\overline{\text{RESET}}$ outputs become active (high and low, respectively) to prevent undefined operation. If the supply voltage drops below the input threshold voltage level (V_{IT-}), the reset outputs go to the reset active state until the supply voltage has returned to its nominal value (see timing diagram).

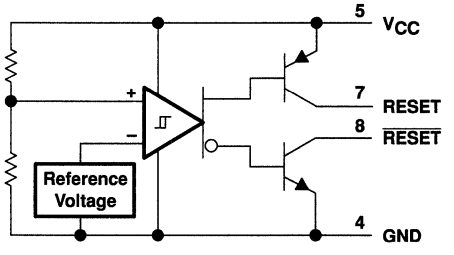
The TL7759C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	SHRINK SMALL OUTLINE (PW)	
0°C to 70°C	TL7759CD	TL7759CP	TL7759CPW	TL7759Y

The D and PW packages are available taped and reeled. Add the suffix R to the device type (e.g., TL7759CDR). Chip forms are tested at 25°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 20 V
Off-state output voltage range: $\overline{\text{RESET}}$ voltage ..... –0.3 V to 20 V
RESET voltage ..... –0.3 V to 20 V
Low-level output current, I_{OL} ($\overline{\text{RESET}}$) ..... 30 mA
High-level output current, I_{OH} (RESET) ..... –10 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package ..... 97°C/W
P package ..... 127°C/W
PW package ..... 149°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		1	7	V
Output voltage, V_O (see Note 4)	Transistor off $\overline{\text{RESET}}$ voltage		15	V
	Transistor off RESET voltage	0		
Low-level output current, I_{OL}	$\overline{\text{RESET}}$		24	mA
High-level output current, I_{OH}	RESET		–8	mA
Operating free-air temperature, T_A	TL7759C	0	70	°C

NOTE 4: RESET output must not be pulled down below GND potential.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL7759C MIN	TL7759C TYP‡	TL7759C MAX	UNIT
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	V_{CC} = 4.3 V	I_{OL} = 24 mA		0.4	0.8	V
V_{OH}	High-level output voltage	RESET	V_{CC} = 4.3 V	I_{OH} = –8 mA	V_{CC}–1			V
V_{IT-}	Input threshold voltage (negative-going V_{CC})		T_A = 25°C		4.43	4.55	4.67	V
			T_A = 0°C to 70°C		4.4		4.7	
V_{res}§	Power-up reset voltage		R_L = 2.2 kΩ	T_A = 25°C		0.8	1	V
				T_A = 0°C to 70°C			1.2	
V_{hys}¶	Hysteresis at V_{CC} input		T_A = 25°C		40	50	60	mV
			T_A = 0°C to 70°C		30		70	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_{CC} = 7 V, See Figure 1	V_{OH} = 15 V			1	µA
I_{OL}	Low-level output current	RESET		V_{OL} = 0 V			–1	µA
I_{CC}	Supply current		No load	V_{CC} = 4.3 V		1400	2000	µA
				V_{CC} = 5.5 V			40	

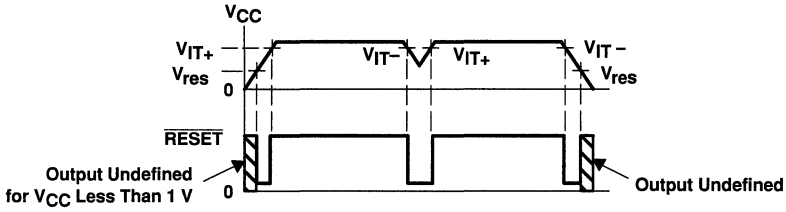
‡ Typical values are at T_A = 25°C.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active, V_{CC} slew rate ≤ 5 V/µs.
¶ This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL7759Y			UNIT
					MIN	TYP	MAX	
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	V_{CC} = 4.3 V,	I_{OL} = 24 mA		0.4		V
V_{IT-}	Input threshold voltage (negative-going V_{CC})					4.55		V
V_{res}†	Power-up reset voltage		R_L = 2.2 kΩ			0.8		V
V_{hys}‡	Hysteresis at V_{CC} input					50		mV
I_{CC}	Supply current		V_{CC} = 4.3 V,	No load		1400		µA

† This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active, V_{CC} slew rate ≤ 5 V/µs.
‡ This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.

timing diagram



switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7759C		UNIT
					MIN	MAX	
t_{PLH}	Propagation delay time, low-to high-level output	V_{CC}	RESET	See Figures 2 and 3§		5	µs
t_{PHL}	Propagation delay time, high-to low-level output	V_{CC}	$\overline{\text{RESET}}$	See Figures 2 and 4		5	µs
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 2 and 4§		1	µs
t_f	Fall time		$\overline{\text{RESET}}$	See Figures 2 and 4		1	µs
$t_{w(min)}$	Minimum pulse duration	V_{CC}	$\overline{\text{RESET}}$	See Figures 2 and 4	5		µs

§ V_{CC} slew rate ≤ 5 V/µs

PARAMETER MEASUREMENT INFORMATION

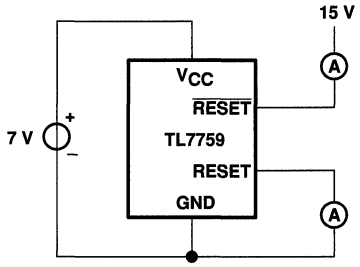
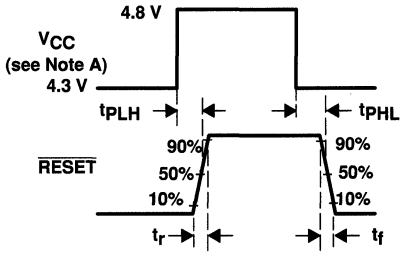
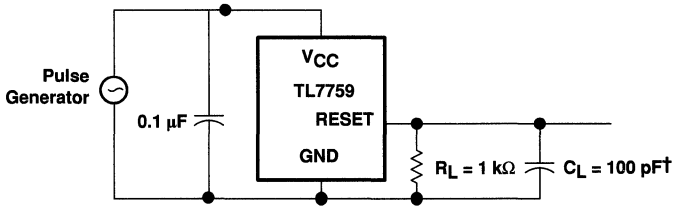


Figure 1. Test Circuit for Output Leakage Current



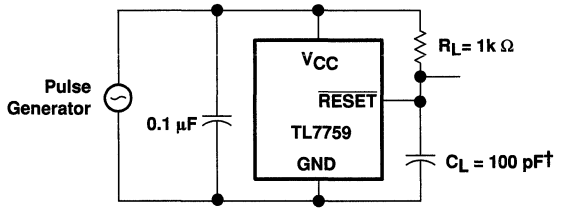
NOTE A. V_{CC} slew rate ≤ 5 V/μs.

Figure 2. Switching Diagram



† C_L Includes jig and probe capacitance.

Figure 3. Test Circuit for RESET Output Switching Characteristics



† C_L Includes jig and probe capacitance.

Figure 4. Test Circuit for $\overline{\text{RESET}}$ Output Switching Characteristics

APPLICATION INFORMATION

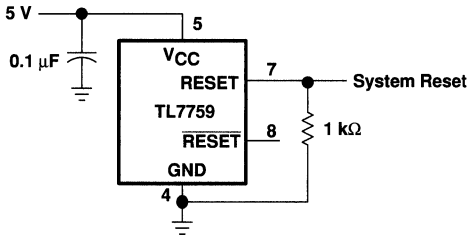
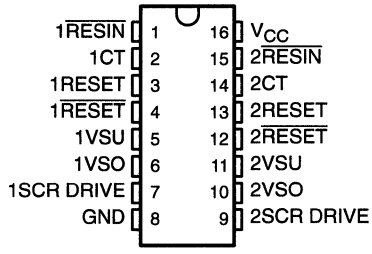


Figure 5. Power-Supply System Reset Generation

SLVS019F – OCTOBER 1987 – REVISED JULY 1999

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **$\overline{\text{RESET}}$ Defined When V_{CC} Exceeds 1 V**
- **Wide Supply-Voltage Range . . . 3.5 V to 18 V**
- **Precision Overvoltage and Undervoltage Sensing**
- **250-mA Peak Output Current for Driving SCR Gates**
- **2-mA Active-Low SCR Gate Drive for False-Trigger Protection**
- **Temperature-Compensated Voltage Reference**
- **True and Complementary Reset Outputs**
- **Externally Adjustable Output Pulse Duration**

DW OR N PACKAGE
(TOP VIEW)



description

The TL7770 is an integrated-circuit system supervisor designed for use as a reset controller in microcomputer and microprocessor power-supply systems. This device contains two independent supply-voltage supervisors that monitor the supplies for overvoltage and undervoltage conditions at the VSO and VSU terminals, respectively. When V_{CC} attains the minimum voltage of 1 V during power up, the $\overline{\text{RESET}}$ output becomes active (low). As V_{CC} approaches 3.5 V, the time-delay function activates, latching RESET and $\overline{\text{RESET}}$ active (high and low, respectively) for a time delay (t_d) after system voltages have achieved normal levels. Above V_{CC} = 3.5 V, taking $\overline{\text{RESIN}}$ low activates the time-delay function during normal system-voltage levels. To ensure that the microcomputer system has reset, the outputs remain active until the voltage at VSU exceeds the threshold value, V_{IT+}, for a time delay, which is determined by an external timing capacitor such that:

$$t_d \approx 20 \times 10^3 \times \text{capacitance}$$

where t_d is in seconds and capacitance is in farads.

The overvoltage-detection circuit is programmable for a wide range of designs. During an overvoltage condition, an internal silicon-controlled rectifier (SCR) is triggered, providing 250-mA peak instantaneous current and 25-mA continuous current to the SCR gate drive terminal, which can drive an external high-current SCR gate or an overvoltage-warning circuit.

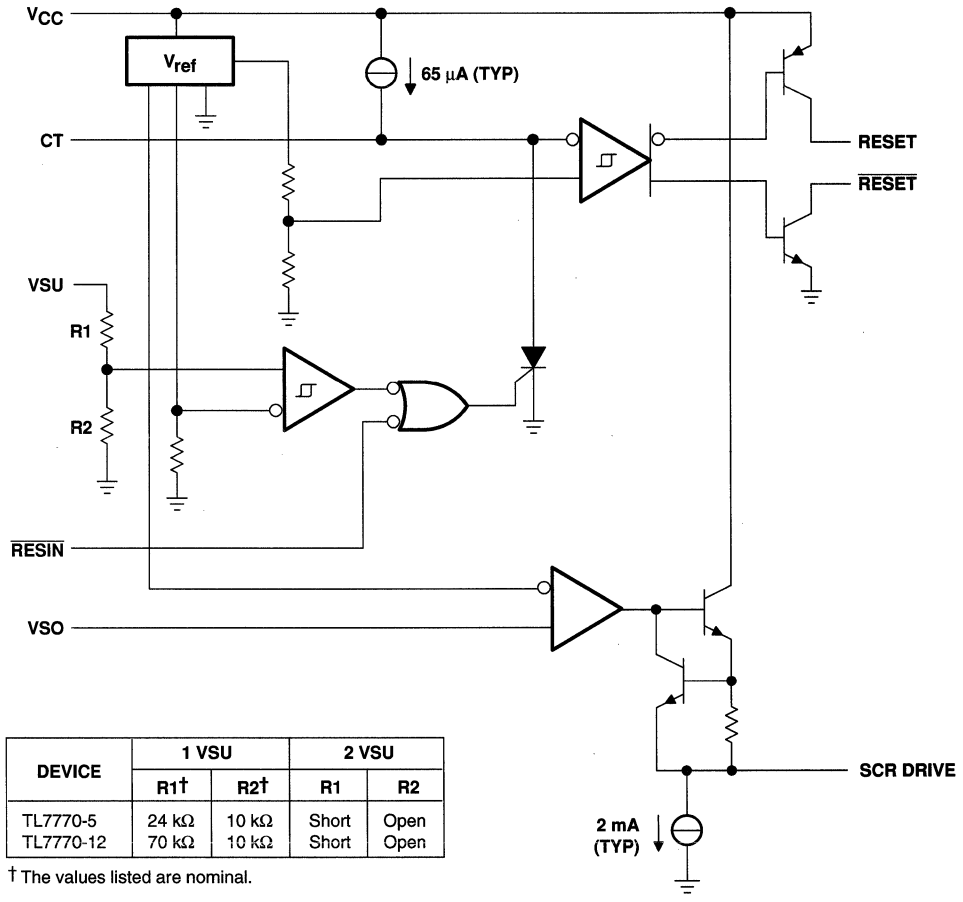
The TL7770C series is characterized for operation from 0°C to 70°C. The TL7770I series is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (DW)	PLASTIC DIP (N)	
0°C to 70°C	TL7770-5CDW TL7770-12CDW	TL7770-5CN TL7770-12CN	TL7770-5Y TL7770-12Y
–40°C to 85°C	TL7770-5IDW	TL7770-5IN	—

DW package is available taped and reeled. Add the suffix R to the device type (e.g., TL7770-5CDWR). Chip forms are tested at 25°C.

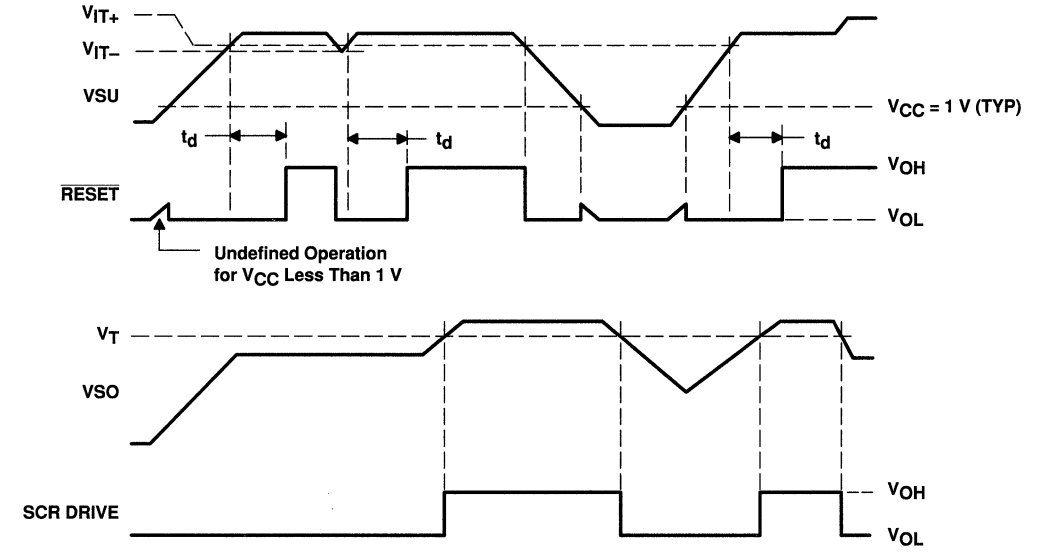
functional block diagram (each channel)



DEVICE	1 VSU		2 VSU	
	R1†	R2†	R1	R2
TL7770-5	24 kΩ	10 kΩ	Short	Open
TL7770-12	70 kΩ	10 kΩ	Short	Open

† The values listed are nominal.

timing requirements



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 20 V
Input voltage range, V_I: 1VSU, 2VSU, 1VSO, and 2VSO (see Note 1) ..... –0.3 V to 18 V
Low-level output current (1$\overline{\text{RESET}}$ and 2$\overline{\text{RESET}}$), I_{OL} ..... 20 mA
High-level output current (1RESET and 2RESET), I_{OH} ..... –20 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DW package ..... 57°C/W
N package ..... 88°C/W
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: DW or N package ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
Input voltage range, V_I (see Note 4)	1VSU, 2VSU, 2VSO, 1VSO	0	18	V
Output voltage, V_O (1CT, 2CT)			5	V
High-level input voltage range, V_{IH} (1$\overline{\text{RESIN}}$, 2$\overline{\text{RESIN}}$)		2	18	V
Low-level input voltage range, V_{IL} (1$\overline{\text{RESIN}}$, 2$\overline{\text{RESIN}}$)		0	0.8	V
Output sink current, I_O (1CT, 2CT)			50	μA
High-level output current, I_{OH} (1RESET, 2RESET)			–16	mA
Low-level output current, I_{OL} (1$\overline{\text{RESET}}$, 2$\overline{\text{RESET}}$)			16	mA
Continuous output current, I_O (1SCR DRIVE, 2SCR DRIVE)			25	mA
Timing capacitor, C_T			10	μF
Operating free-air temperature, T_A	TL7770C series	0	70	°C
	TL7770I series	–40	85	°C

NOTE 4: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating conditions (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS†	TL7770-5C TL7770-12C TL7770-5I			UNIT
				MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	RESET	I_{OH} = –15 mA	V_{CC}–1.5			V
		SCR DRIVE	I_{OH} = –20 mA	V_{CC}–1.5			
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	I_{OL} = 15 mA			0.4	V
V_{IT-}	Undervoltage input threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	T_A = MIN to MAX	4.46		4.64	V
		TL7770-12 (12-V sense, 1VSU)		10.68		11.12	
		TL7770-5, TL7770-12 (programmable sense, 2VSU)		1.47		1.53	
V_{hys}	Hysteresis at VSU ($V_{IT+} - V_{IT-}$)	TL7770-5 (5-V sense, 1VSU)	T_A = MIN to MAX		15		mV
		TL7770-12 (12-V sense, 1VSU)			36		
		TL7770-5, TL7770-12 (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5, TL7770-12 (VSO)	T_A = MIN to MAX	2.48		2.68	V
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 5.5 V or 0.4 V			–10	µA
		VSO	V_I = 2.4 V		0.5	2	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_O = 18 V			50	µA
I_{OL}	Low-level output current	RESET	V_O = 0			–50	µA
I_{OH}	Peak output current	SCR DRIVE	Duration = 1 ms	250			mA

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

total device

PARAMETER		TEST CONDITIONS†		TL7770-5C TL7770-12C TL7770-5I			UNIT
				MIN	TYP‡	MAX	
V_{res}§	Power-up reset voltage	V_{CC} = VSU			0.8	1	V
I_{CC}	Supply current	1VSU = 18 V, 2VSU = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	T_A = 25°C			5	mA
			T_A = MIN to MAX			6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

electrical characteristics over recommended operating conditions (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS	TL7770-5Y TL7770-12Y			UNIT
				MIN	TYP†	MAX	
V_{IT-}	Undervoltage input threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	T_A = MIN to MAX	4.46		4.64	V
		TL7770-12 (12-V sense, 1VSU)		10.68		11.12	
		TL7770-5, TL7770-12 (programmable sense, 2VSU)		1.47		1.53	
V_{hys}	Hysteresis at VSU ($V_{IT+} - V_{IT-}$)	TL7770-5 (5-V sense, 1VSU)	T_A = MIN to MAX		15		mV
		TL7770-12 (12-V sense, 1VSU)			36		
		TL7770-5, TL7770-12 (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5, TL7770-12 (VSO)	T_A = MIN to MAX	2.48		2.68	V
I_I	Input current	VSO	V_I = 2.4 V		0.5		µA

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

total device

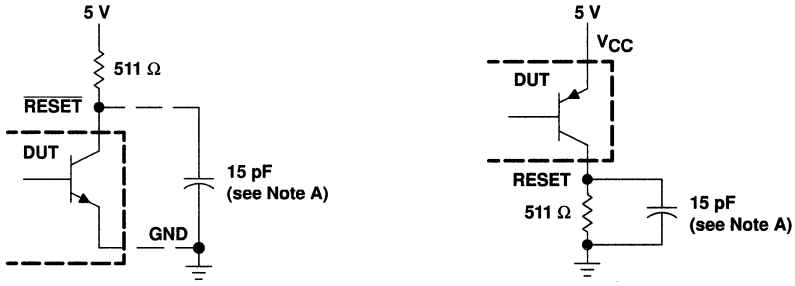
PARAMETER		TEST CONDITIONS		TL7770-5Y TL7770-12Y			UNIT
				MIN	TYP†	MAX	
V_{res}‡	Power-up reset voltage	V_{CC} = VSU,	V_{OL} = 0.4 V, I_{OL} = 1 mA		0.8		V
I_{CC}	Supply current	1VSU = 18 V, 2VSU = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	T_A = 25°C			5	mA

† Typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	See Figures 1 and 3		270	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$			270	500	ns
t_r	Rise time		RESET				75	ns
t_f	Fall time					150		
t_r	Rise time		$\overline{\text{RESET}}$			75		ns
t_f	Fall time						50	
$t_{w(min)}$	Minimum effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2a		150		ns
		VSU		See Figure 2b		100		

PARAMETER MEASUREMENT INFORMATION

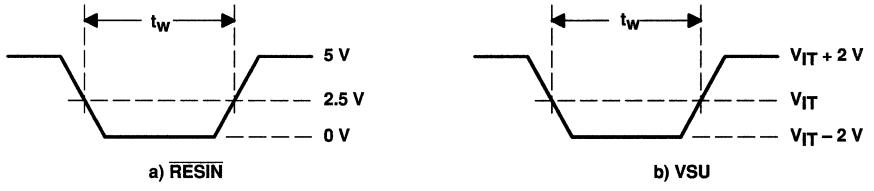


RESET OUTPUT CONFIGURATION

RESET OUTPUT CONFIGURATION

NOTE A. This includes jig and probe capacitance.

Figure 1. RESET and RESET Output Configurations



a) RESIN

b) VSU

WAVEFORMS

Figure 2. Input Pulse Definition

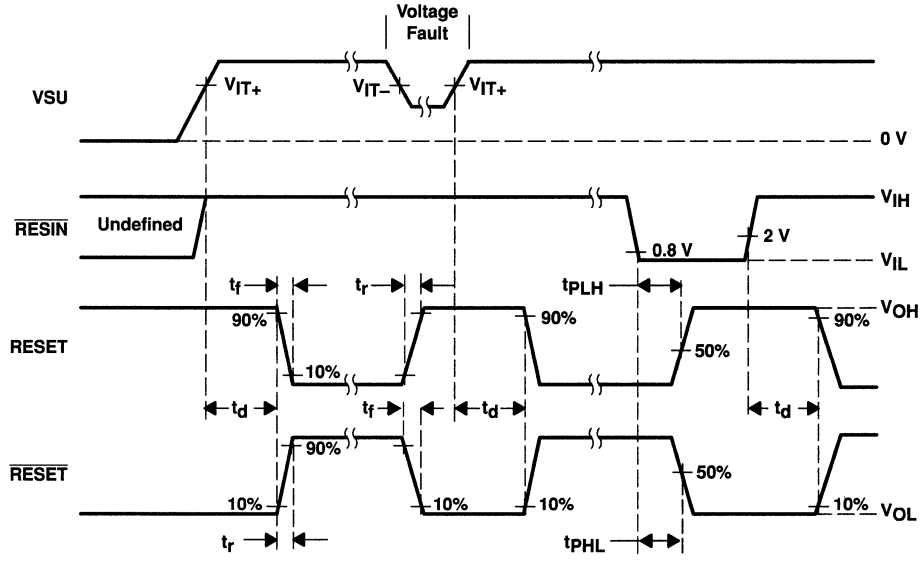
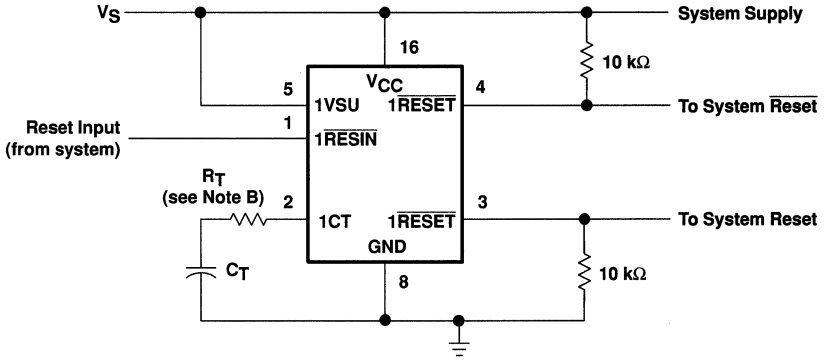


Figure 3. Voltage Waveforms

APPLICATION INFORMATION



NOTE B. When V_{CC} and 1VSU are connected to the same point, it is recommended that series resistance (R_T) be added between the time-delay programming capacitor (C_T) and the voltage-supervisor device terminal (1CT). The suggested R_T value is given by:

$$R_T > \frac{V_I - V_{IT-}}{1 \times 10^{-3}}, \text{ where } V_I = (\text{the lesser of 7.1 V or } V_S)$$

When this series resistor is used, the t_d calculation is as follows:

$$t_d = \frac{1.3 - [((6.5E - 5) \times 10^{-5}) \times R_T]}{6.5 \times 10^{-5}} \times C_T$$

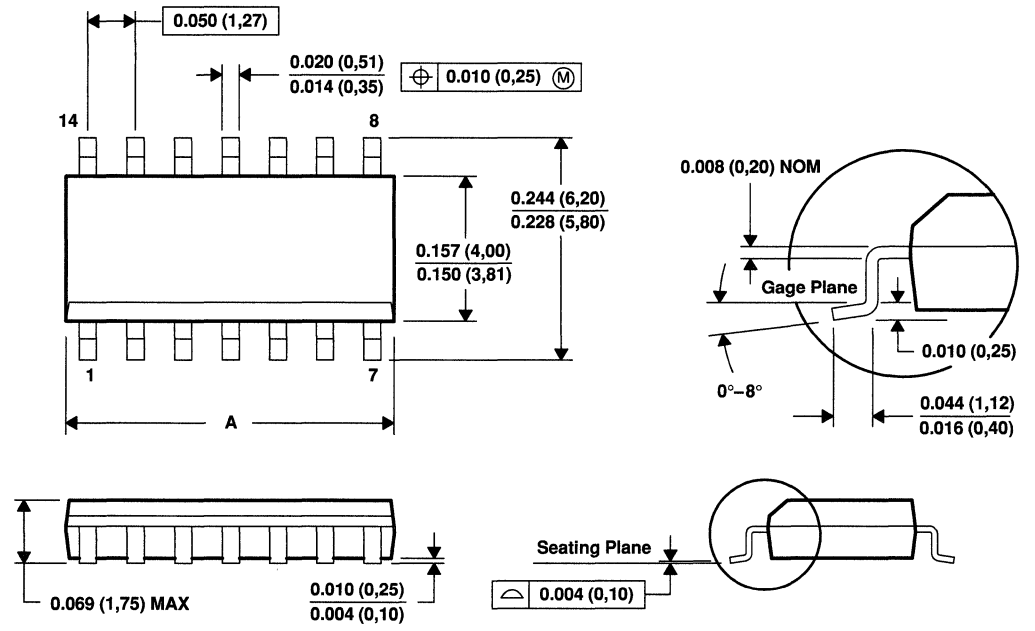
Figure 4. System Reset Controller With Undervoltage Sensing

Mechanical Data

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

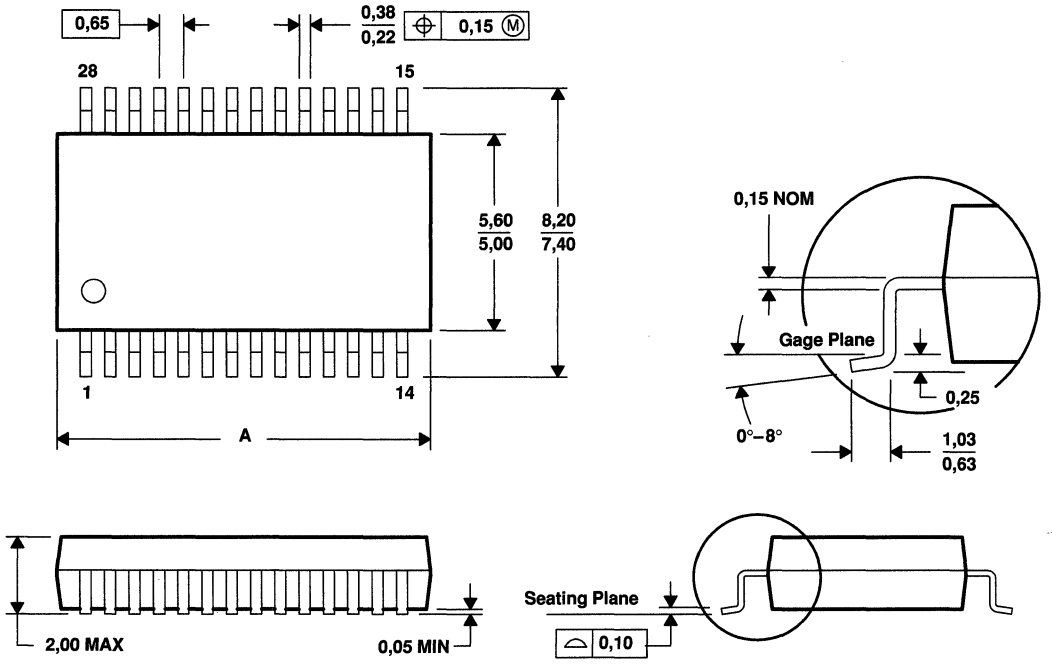
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

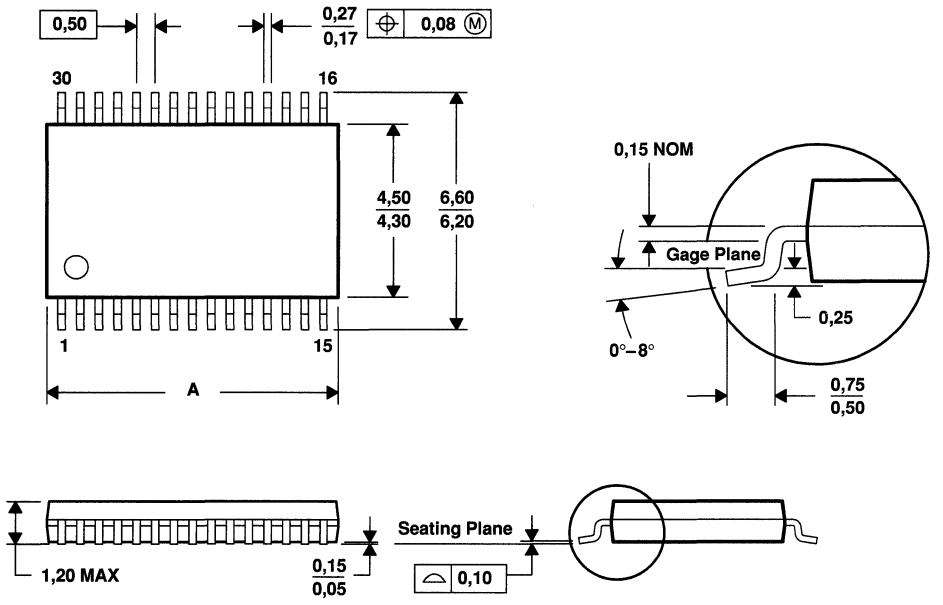
4040065 / C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

MECHANICAL INFORMATION

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



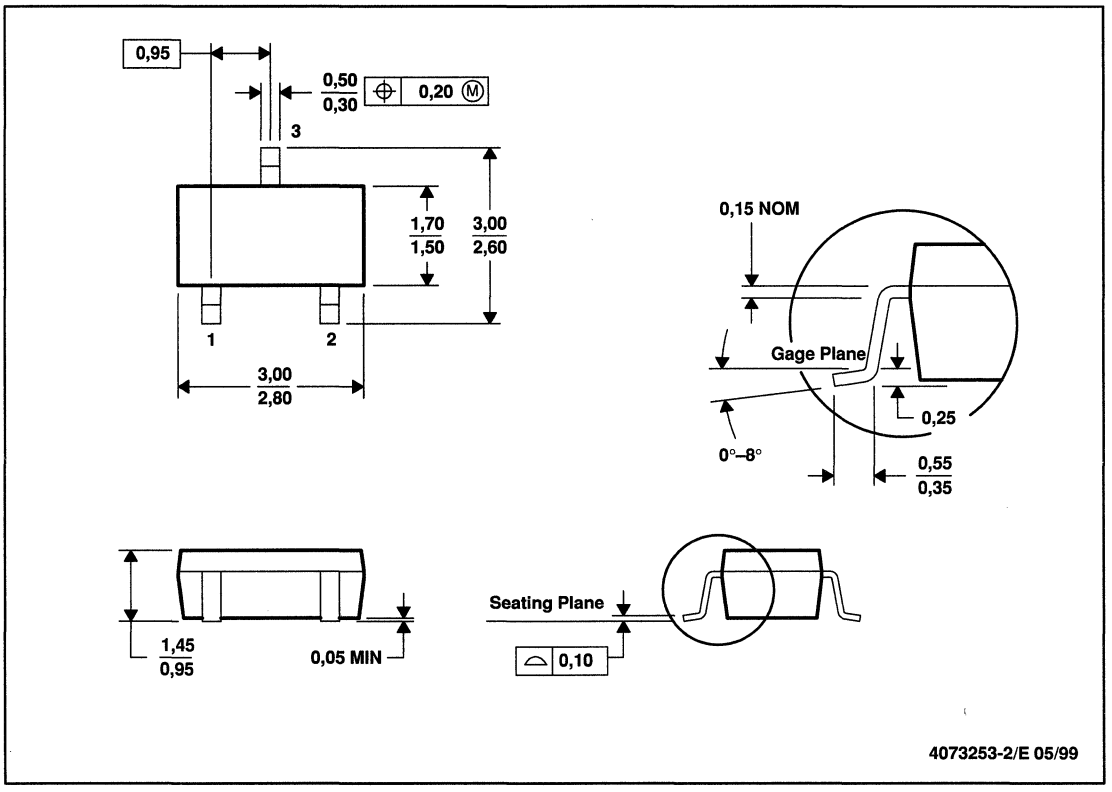
DIM \ PINS **	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,10	12,60
A MIN	7,70	7,70	9,60	10,90	12,40

4073252/D 09/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

MECHANICAL INFORMATION

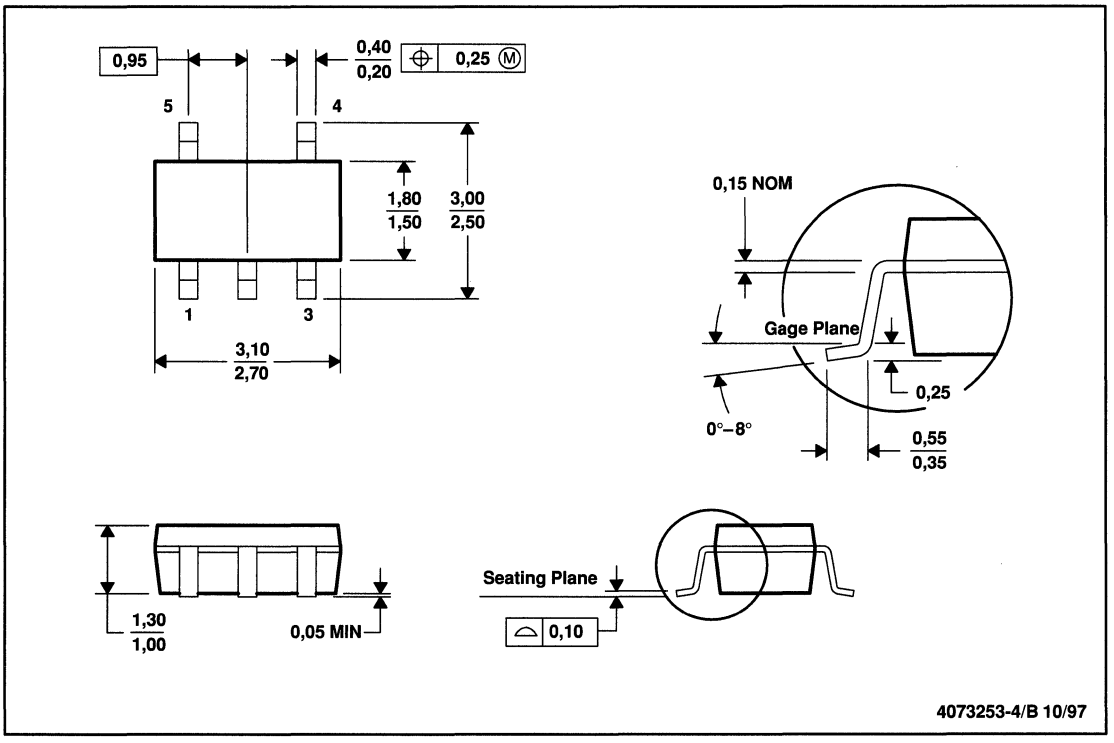
DBV (R-PDSO-G3) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL INFORMATION

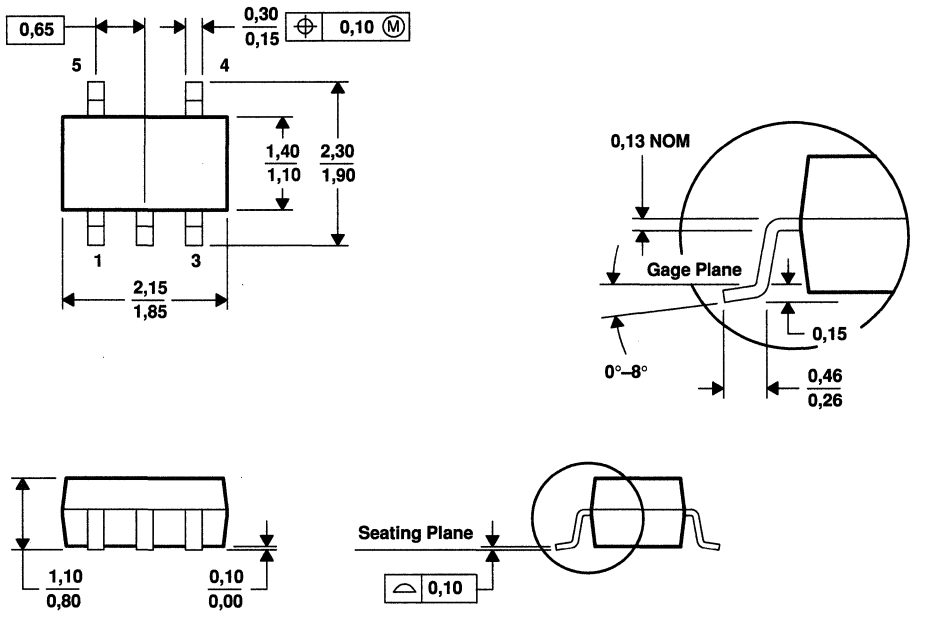
DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

MECHANICAL INFORMATION

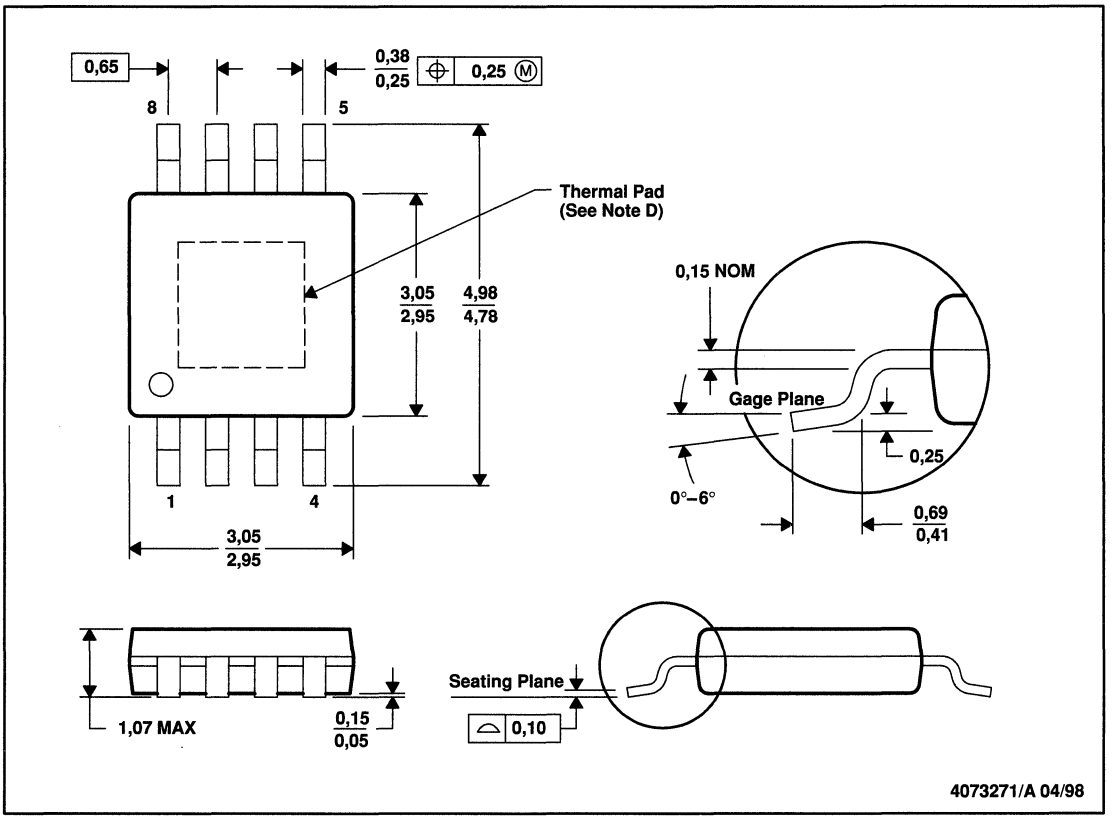
DCK (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-203

MECHANICAL INFORMATION

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



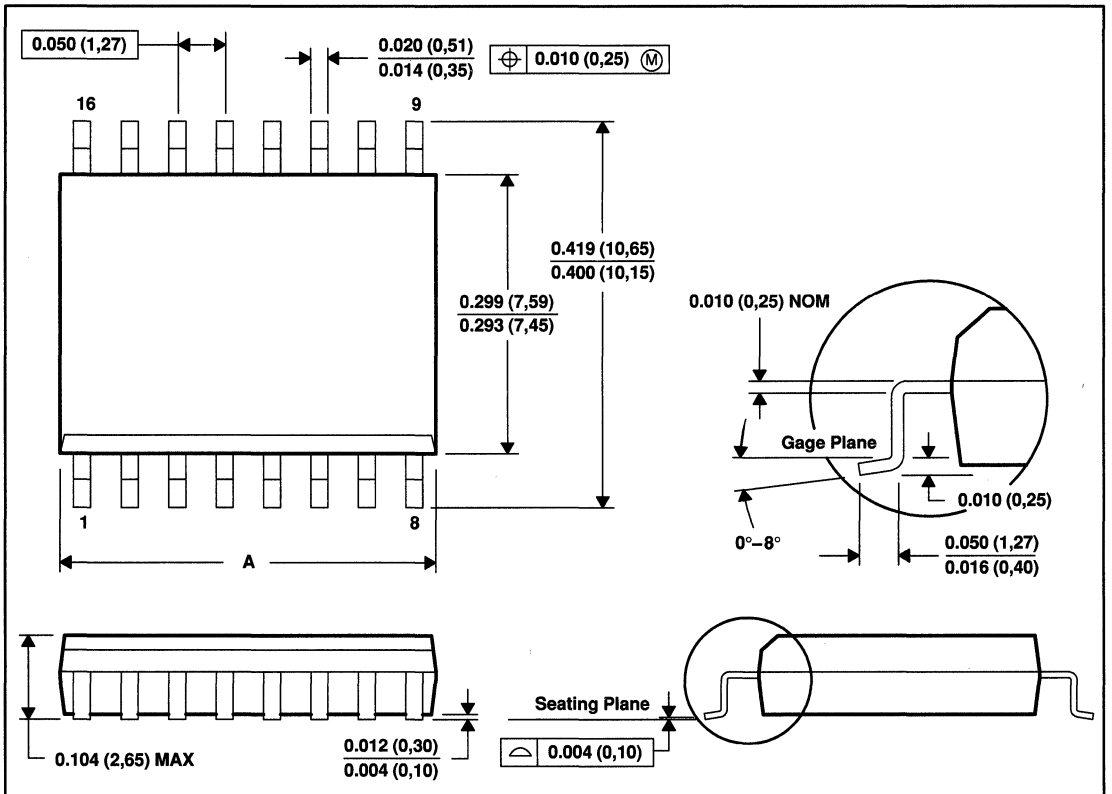
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments Incorporated.

MECHANICAL INFORMATION

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

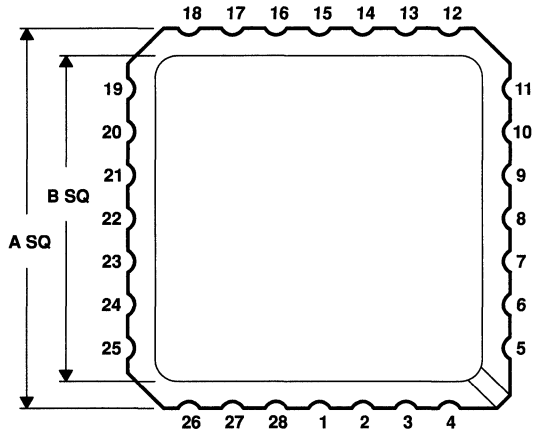
4040000/C 07/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

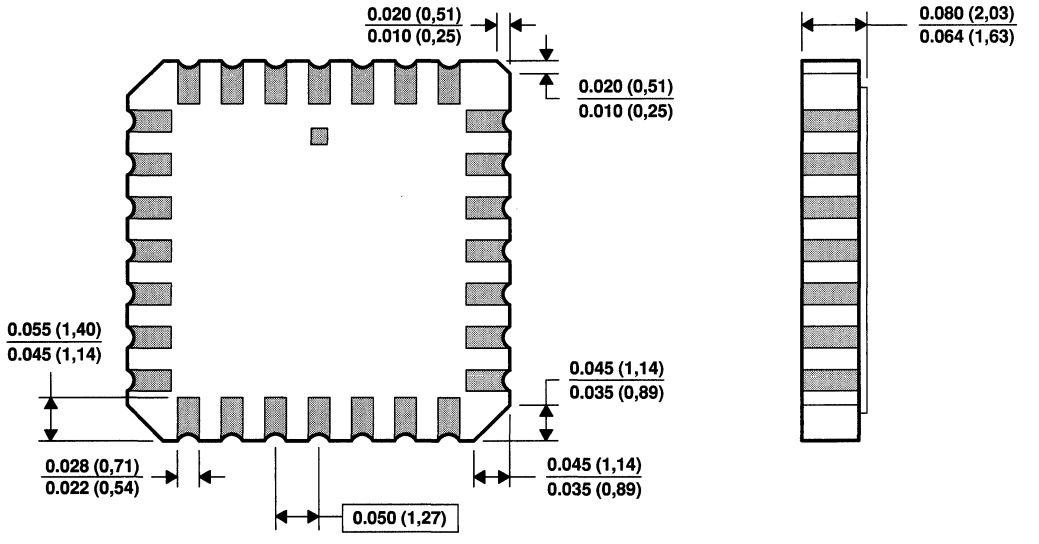
MECHANICAL INFORMATION

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINALS SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

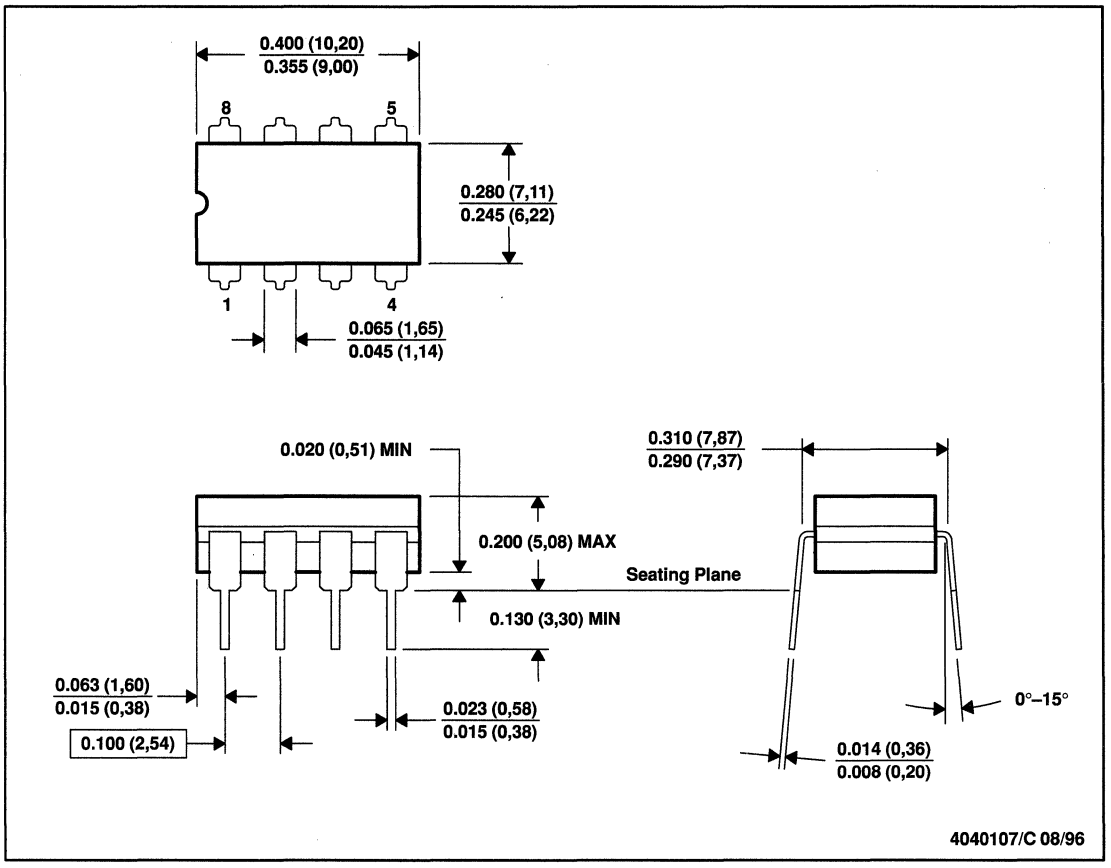


4040140/C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold-plated.
E. Falls within JEDEC MS-004

MECHANICAL INFORMATION

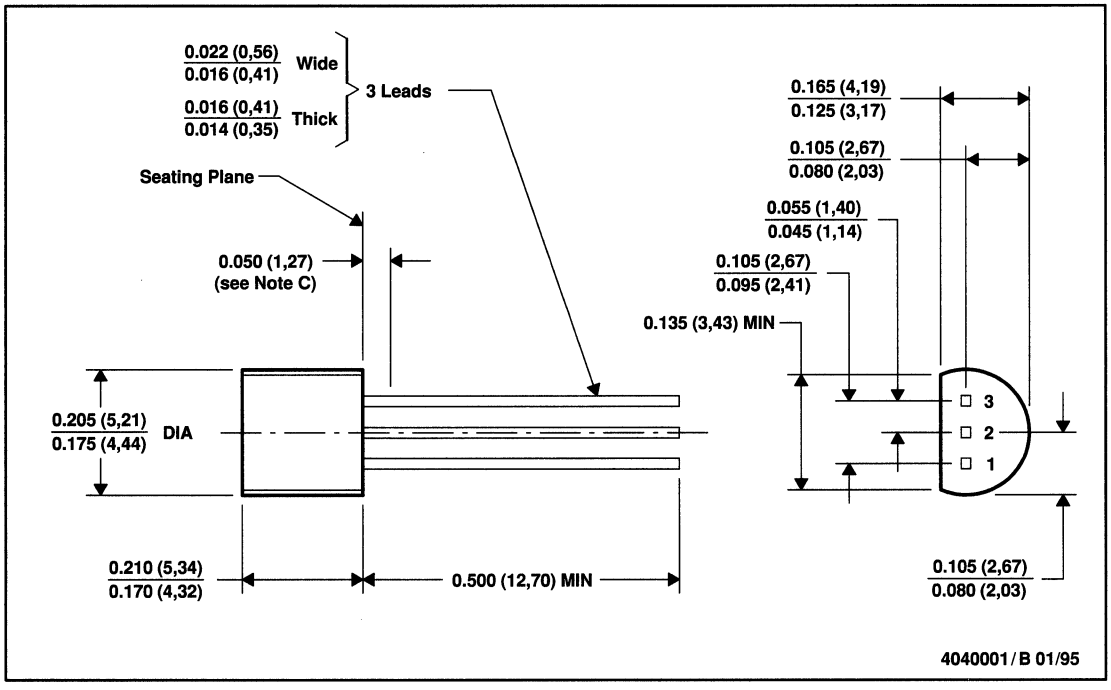
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL INFORMATION

LP (O-PBCY-W3) **PLASTIC CYLINDRICAL PACKAGE**



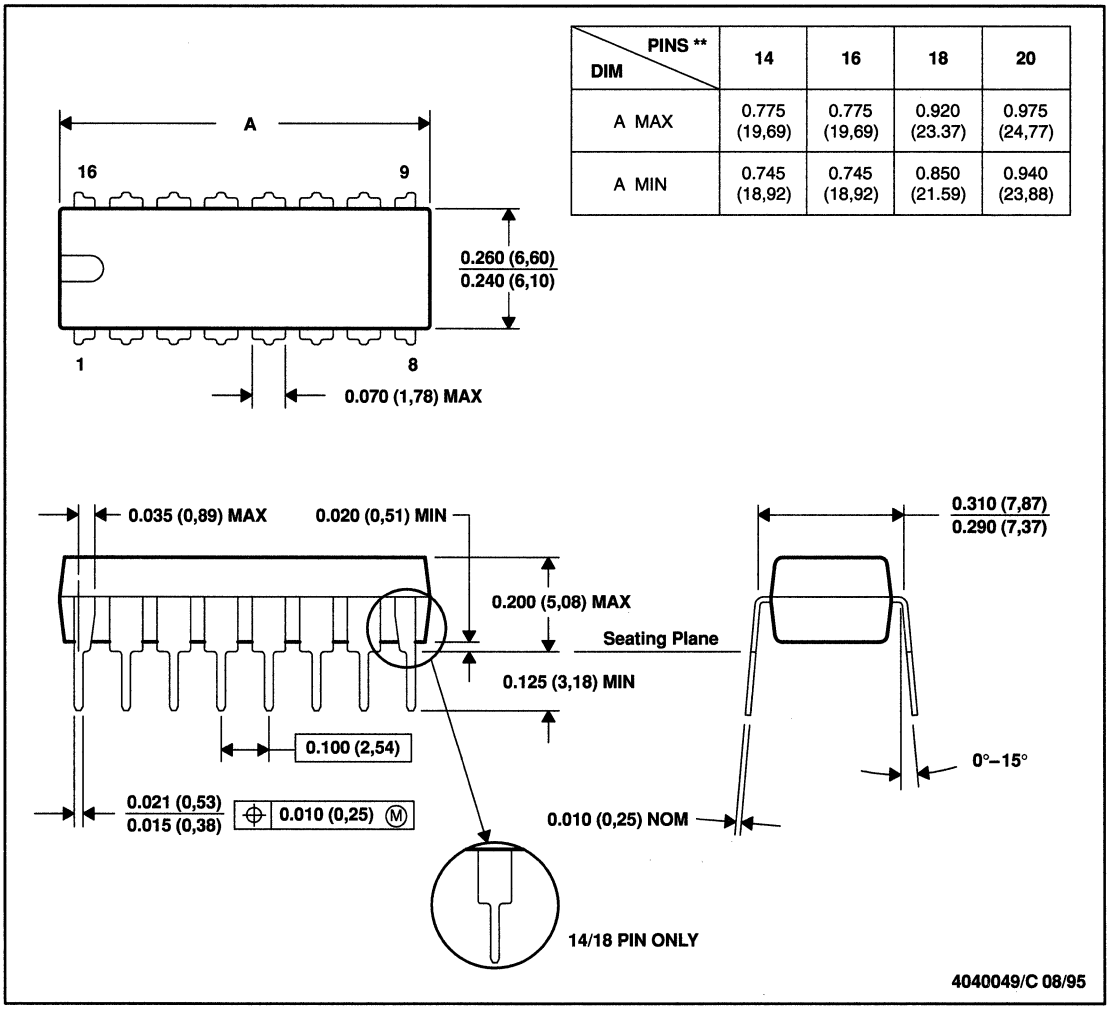
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. Falls within JEDEC TO-226AA (TO-226AA replaces TO-92)

MECHANICAL INFORMATION

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)

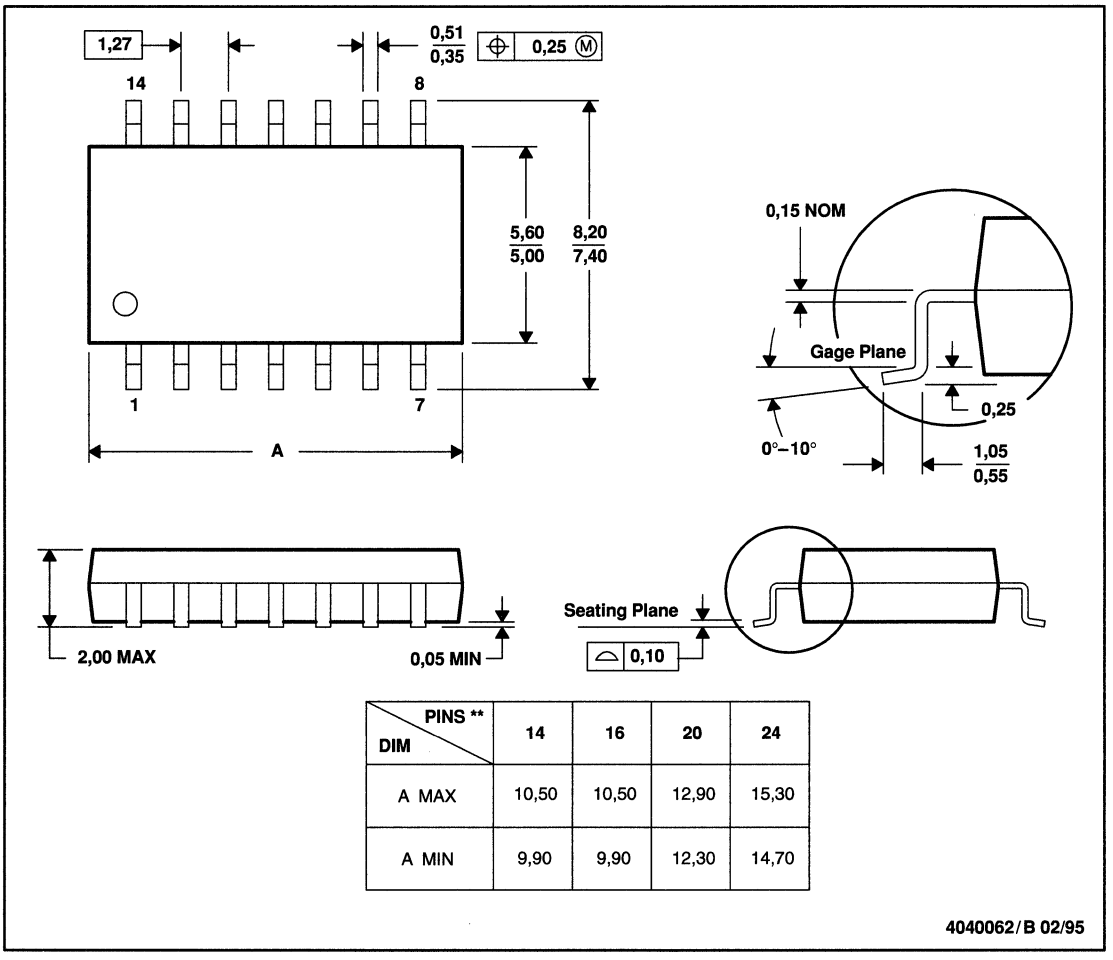


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

MECHANICAL INFORMATION

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



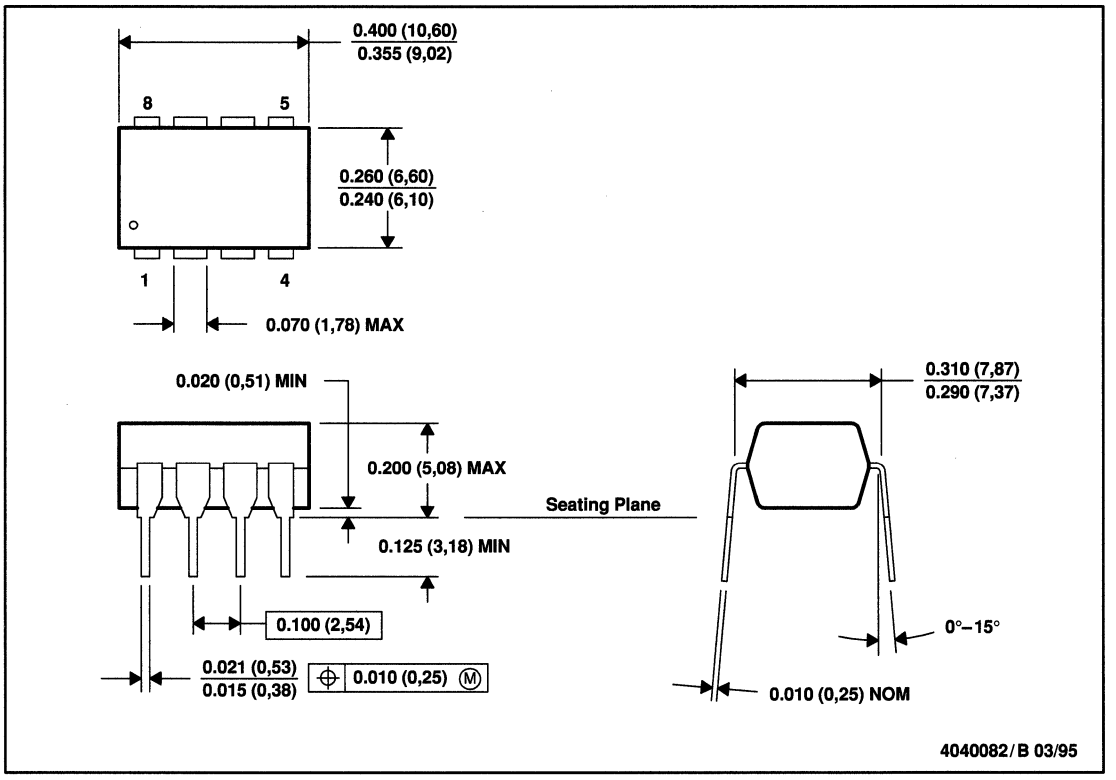
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/B 02/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL INFORMATION

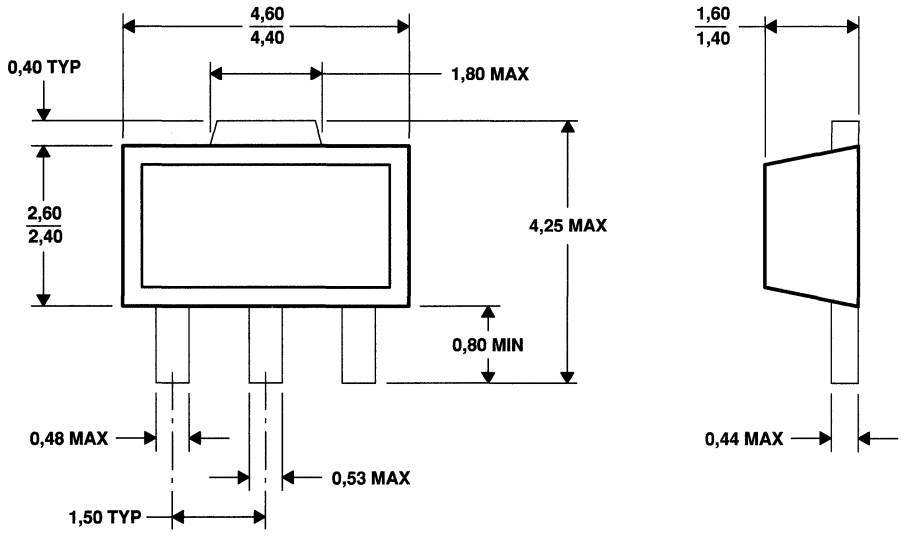
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL INFORMATION

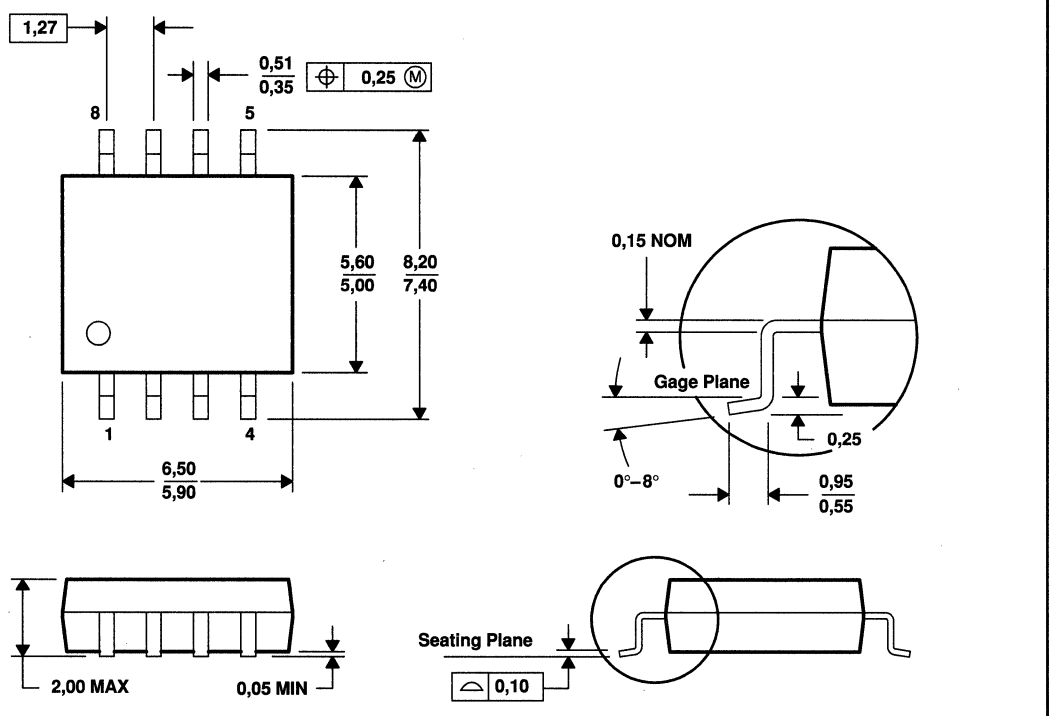
PK (R-PSSO-F3) **PLASTIC SINGLE-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.

MECHANICAL INFORMATION

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**

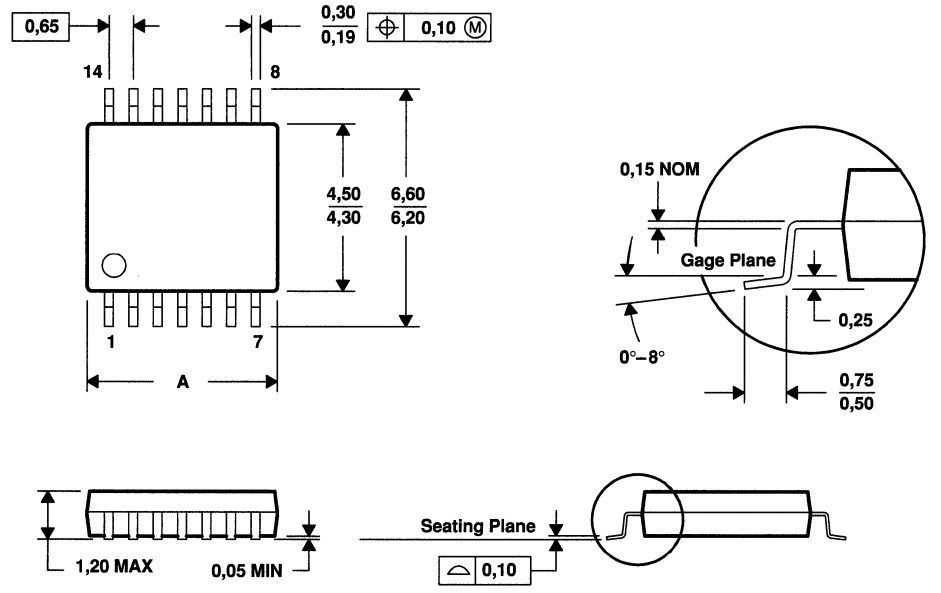


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

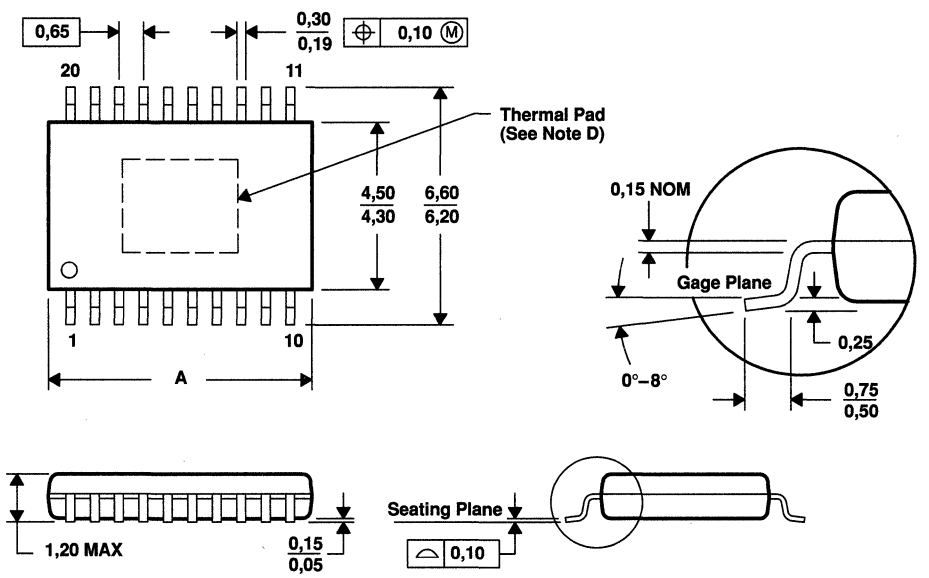
4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL INFORMATION

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

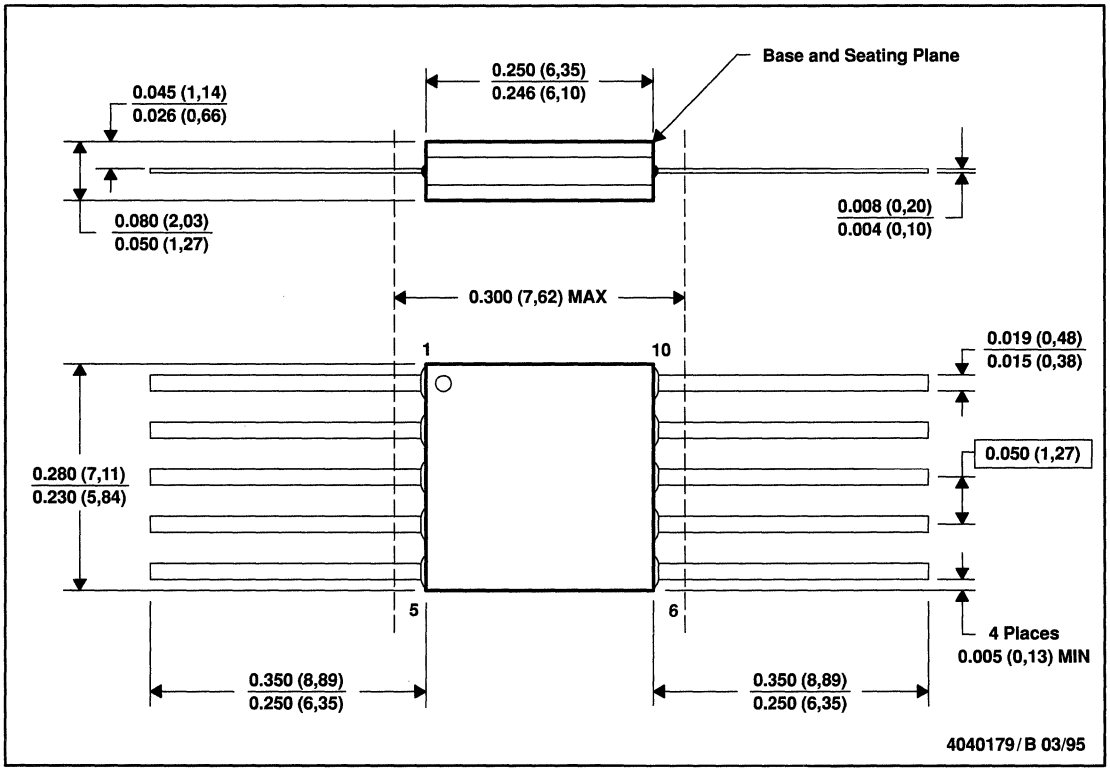
4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments Incorporated.

MECHANICAL INFORMATION

U (S-GDFP-F10) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

NOTES

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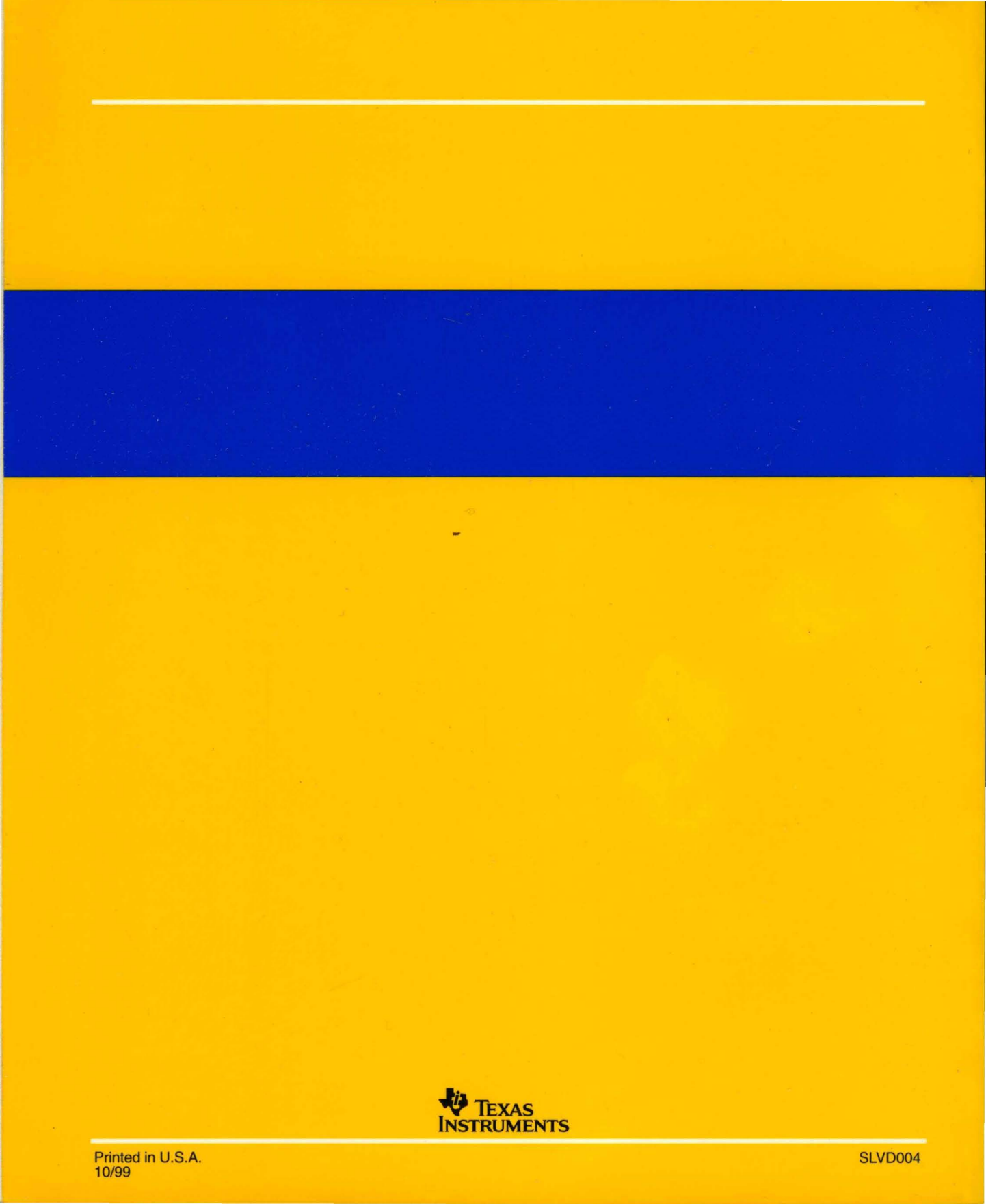
TEXAS INSTRUMENTS

A101299



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