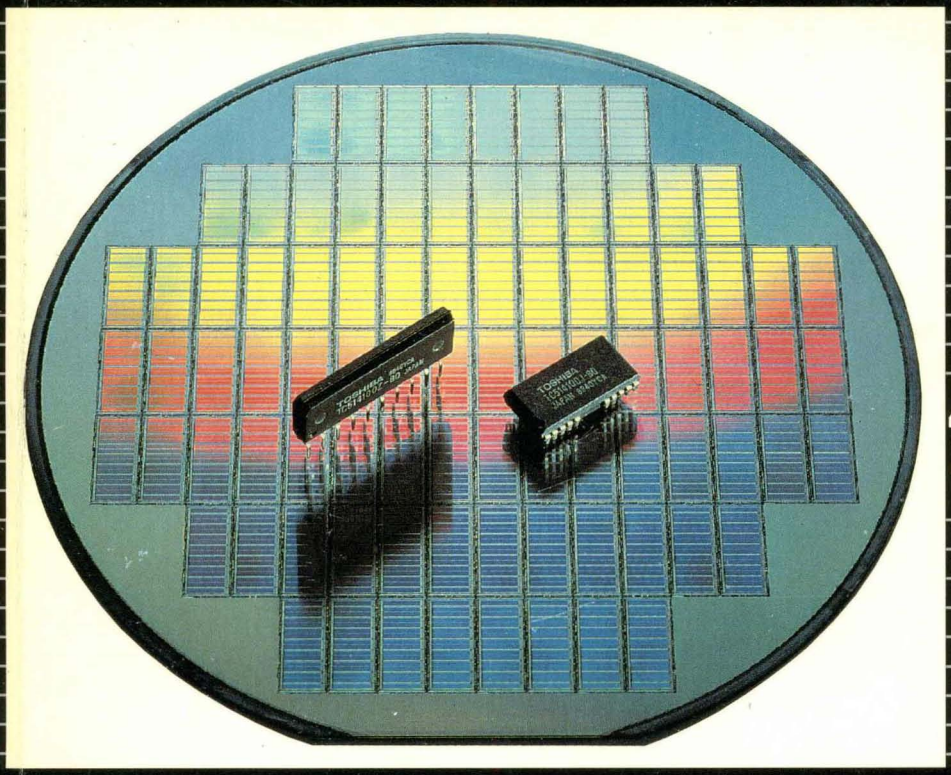
TOSHIBA



4M DRAM 1991

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

TOSHIBA 4M DRAM 1991 TAEC

TOSHIBA

4M DRAM
1991

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NOTE: FOR 60ns AND 70ns ACCESS TIME VERSIONS, PLEASE CONTACT YOUR LOCAL REGIONAL SALES OFFICE. REGIONAL SALES OFFICE LOCATIONS ARE LISTED ON THE BACK COVER.

DRAM PRODUCT GUIDE

1. CMOS 4M DYNAMIC RAM

CAPACITY	PART NUMBER	ORGANIZATION OPERATING MODE	$\overline{RAS}$ ACCESS TIME MAX (NS)	$\overline{CAS}$ ACCESS TIME MAX (NS)	POWER DISSIPATION max (mW) ACTIVE	POWER DISSIPATION max (mW) STANDBY	PIN COUNT	PACKAGE P	PACKAGE J	PACKAGE SJ	PACKAGE Z	PACKAGE WIDTH (P, J, SJ, FT) OR HEIGHT (Z) (inch)
4M	TC514100J/Z-80	4MX1, FAST PAGE MODE	80	20	550	5.5	18(P) 26/20 (J) 26/20 (SJ) 20 (Z)	■		■	■	0.300 (P) 0.350 (J) 0.300 (SJ) 0.400 (Z)
	TC514100J/Z-10		100	25	468			■		■	■	
	TC514100JL/ZL-80		80	20	550	2.2		■		■	■	
	TC514100JL/ZL-10		100	25	468			■		■	■	
	TC514100AP/AJ/ASJ/AZ-60		60	20	660	5.5		■	■	■	■	
	TC514100APL/AJL/ASJL/AZL-60					1.1		■	■	■	■	
	TC514100AP/AJ/ASJ/AZ-70		70		550	5.5		■	■	■	■	
	TC514100APL/AJL/ASJL/AZL-70					1.1		■	■	■	■	
	TC514100AP/AJ/ASJ/AZ-80		80		468	5.5		■	■	■	■	
	TC514100APL/AJL/ASJL/AZL-80					1.1		■	■	■	■	
	TC514100AP/AJ/ASJ/AZ-10		100	25	413	5.5		■	■	■	■	
	TC514100APL/AJL/ASJL/AZL-10					1.1		■	■	■	■	
	TC514101J/Z-80	4MX1, NIBBLE MODE	80	20	578	5.5		■		■	■	
	TC514101J/Z-10		100	25	495			■		■	■	
	TC514101AP/AJ/ASJ/AZ-60		60	20	660			■	■	■	■	
	TC514101AP/AJ/ASJ/AZ-70		70		550			■	■	■	■	
	TC514101AP/AJ/ASJ/AZ-80		80		468			■	■	■	■	
	TC514101AP/AJ/ASJ/AZ-10		100	25	413			■	■	■	■	
	TC514102J/Z-80	4MX1, STATIC COLUMN MODE	80	20	550			■		■	■	
	TC514102J/Z-10		100	25	468			■		■	■	
	TC514102AP/AJ/ASJ/AZ-60		60	20	660			■	■	■	■	
	TC514102AP/AJ/ASJ/AZ-70		70		550			■	■	■	■	
	TC514102AP/AJ/ASJ/AZ-80		80		468			■	■	■	■	
	TC514102AP/AJ/ASJ/AZ-10		100	25	413			■	■	■	■	

CAPACITY	PART NUMBER	ORGANIZATION OPERATING MODE	$\overline{RAS}$ ACCESS TIME MAX (NS)	$\overline{CAS}$ ACCESS TIME MAX (NS)	POWER DISSIPATION max (mW) ACTIVE	POWER DISSIPATION max (mW) STANDBY	PIN COUNT	PACKAGE P J SJ Z	PACKAGE WIDTH (P, J, SJ, FT) OR HEIGHT (Z) (inch)
4M	TC514400J/Z-80	1MX4, FAST PAGE MODE	80	20	578	5.5	20 (P) 26/20 (J) 26/20 (SJ) 20 (Z)	■ ■	0.300 (P) 0.350 (J) 0.300 (SJ) 0.400 (Z)
	TC514400J/Z-10		100	25	495			■ ■	
	TC514400JL/ZL-80		80	20	578	2.2		■ ■	
	TC514400JL/ZL-10		100	25	495			■ ■	
	TC14400AP/AJ/ASJ/AZ-60		60	20	660	5.5		■ ■ ■ ■	
	TC514400APL/AJL/ASJL/AZL-60					1.1		■ ■ ■ ■	
	TC514400AP/AJ/ASJ/AZ-70		70		550	5.5		■ ■ ■ ■	
	TC514400APL/AJL/ASJL/AZL-70					1.1		■ ■ ■ ■	
	TC514400AP/AJ/ASJ/AZ-80		80		468	5.5		■ ■ ■ ■	
	TC514400APL/AJL/ASJL/AZL-80					1.1		■ ■ ■ ■	
	TC514400AP/AJ/ASJ/AZ-10		100	25	413	5.5		■ ■ ■ ■	
	TC514400APL/AJL/ASJL/AZL-10					1.1		■ ■ ■ ■	
	TC514402J/Z-80	4MX1, STATIC COLUMN MODE	80	20	578	5.5		■ ■	
	TC514402J/Z-10		100	25	495			■ ■	
	TC514402AP/AJ/ASJ/AZ-60		60	20	660			■ ■ ■ ■	
	TC514402AP/AJ/ASJ/AZ-70		70		550			■ ■ ■ ■	
	TC514402AP/AJ/ASJ/AZ-80		80		468			■ ■ ■ ■	
	TC514402AP/AJ/ASJ/AZ-10		100	25	413			■ ■ ■ ■	
	TC514410J/Z-80	4MX1, WRITE PER BIT MODE	80	20	578			■ ■	
	TC514410J/Z-10		100	25	495			■ ■	
	TC514410AP/AJ/ASJ/AZ-60		60	20	660			■ ■ ■ ■	
	TC514410AP/AJ/ASJ/AZ-70		70		550			■ ■ ■ ■	
	TC514410AP/AJ/ASJ/AZ-80		80		468			■ ■ ■ ■	
	TC514410AP/AJ/ASJ/AZ-10		100	25	413			■ ■ ■ ■	

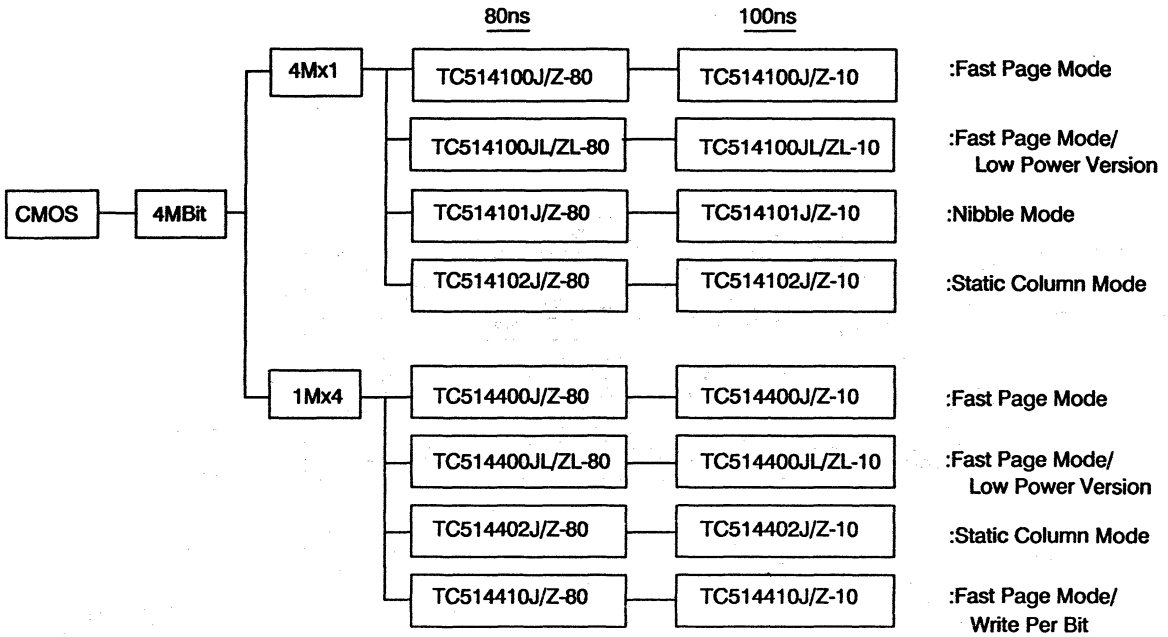
P = PLASTIC DIP, J = PLASTIC SOJ, SJ = PLASTIC SKINNY SOJ, Z = PLASTIC ZIP

MODULES

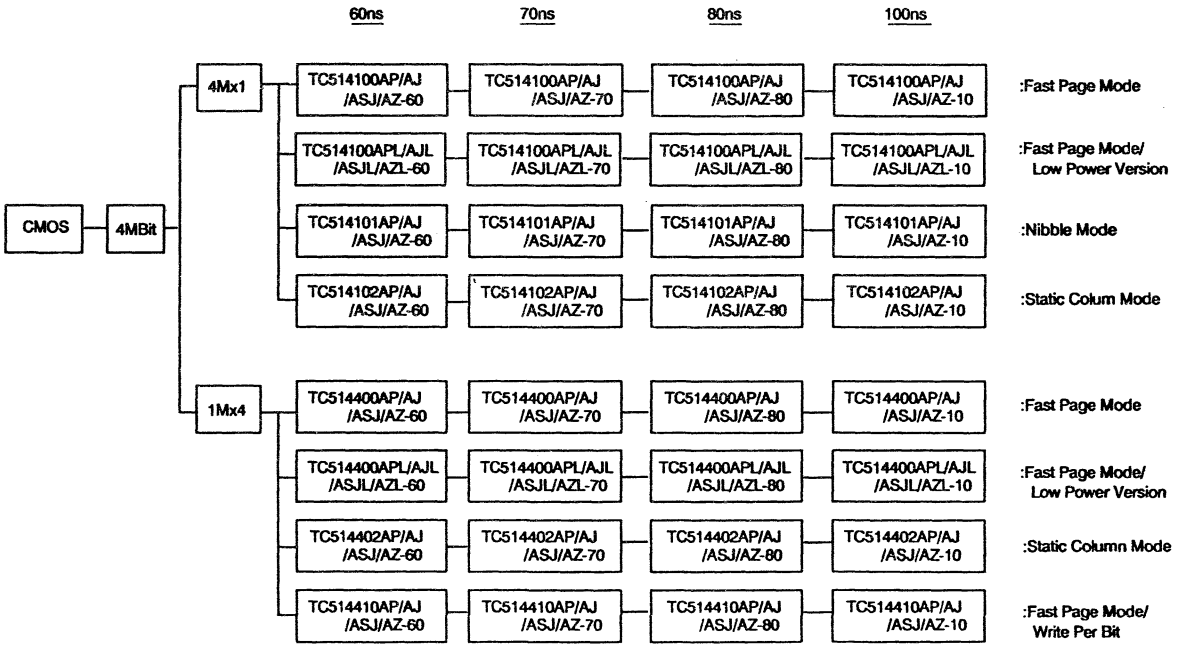
CAPACITY	PART NUMBER	ORGANIZATION	RAS ACCESS TIME MAX (ns)	CAS ACCESS TIME MAX (ns)	POWER DISSIPATION MAX (mW)		PIN COUNT	PACKAGE			MODULE HEIGHT (in)
					ACTIVE	STANDBY		S	SG	L	
32M BIT	THM84000S/L-80	4Mx8	80	20	4400	44	30	■		■	0.95 (S)
	THM84000S/L-10		100	25	3740			■		■	1.035 (L)
	THM321000S/SG-80	1Mx32	80	20	4620	44	72	■	■		1.0
	THM321000S/SG-10		100	25	3960			■	■		
	THM321020S/SG-80		80	20	4620			■	■		
	THM321020S/SG-10		100	25	3960			■	■		
36M BIT	THM94000S/L-80	4Mx9	80	20	4950	49.5	30	■		■	0.95 (S)
	THM94000S/L-10		100	25	4212			■		■	1.035 (L)
	THM361020S/SG-80	1Mx36	80	20	6160	66	72	■	■		1.0
	THM361020S/SG-10		100	25	5280			■	■		
40M BIT	THM401020SG-80	1Mx40	80	20	5775	55	72		■		1.0
	THM401020SG-10		100	25	4950				■		
64M BIT	THM322020S/SG-80	2Mx32	80	20	4708	88	72	■	■		1.0
	THM322020S/SG-10		100	25	4048			■	■		
72M BIT	THM362020S/SG-80	2Mx36	80	20	6292	132	72	■	■		1.169
	THM362020S/SG-10		100	25	5412			■	■		
80M BIT	THM402020SG-80	2Mx40	80	20	5885	110	72		■		1.0
	THM402020SG-10		100	25	5060				■		

NOTE:
S = SOLDER (TIN/LEAD) PLATED CONTACTS, SOCKET TYPE MODULE
SG = GOLD PLATED CONTACTS, SOCKET TYPE MODULE
L = SOLDER PLATED LEADS, THROUGH-HOLE TYPE MODULE

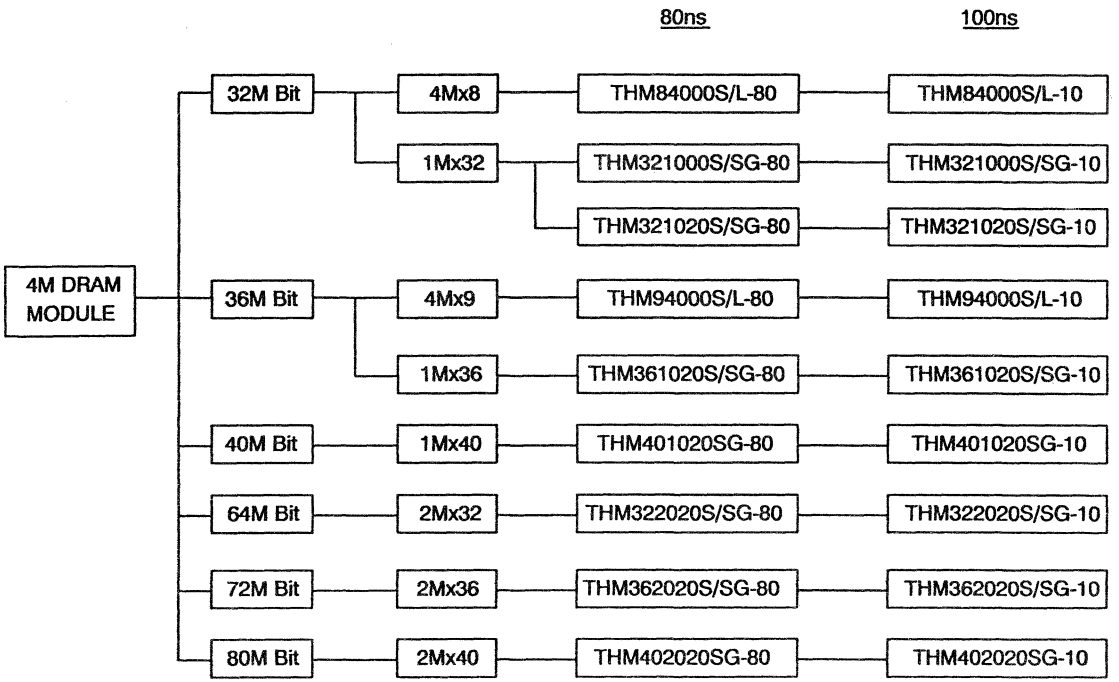
TOSHIBA 1ST GENERATION 4M DYNAMIC RAM



TOSHIBA 2ND GENERATION 4M DYNAMIC RAM



TOSHIBA 1ST GENERATION 4M DRAM MODULES



DRAM CROSS REFERENCE

1. 4M X 1 DYNAMIC RAM

FUNCTION	FAST PAGE	NIBBLE	STATIC COLUMN
TOSHIBA	**TC514100AP/AJ/ASJ/AZ**	**TC514101AP/AJ/ASJ/AZ**	**TC514102AP/AJ/ASJ/AZ**
HITACHI	HM514100AJ/AS/AZ	HM514100AJ/AS/AZ	HM514102AJ/AS/AZ
NEC	MPD424100	MPD424101	MPD424102
MITSUBISHI	M5M44100J/L	M5M44101J/L	M5M44102J/Z
OKI	MSM514100RS/JS/ZS	MSM514101RS/JS/ZS	MSM514102RS/JS/ZS
FUJITSU	MB814100		
PANASONIC	MN41C4000SJ/L		MN41C4000SJ/L
SAMSUNG	KM41C4000	KM41C4001	KM41C4002
MICRON	MT4C1004		
TI	TMS44100		
MOSAIC	MDM14000		
MOTOROLA	MCM514100		
SIEMENS	HYB514100		
VITELIC	V53C400		

2. 1M X 4 DYNAMIC RAM

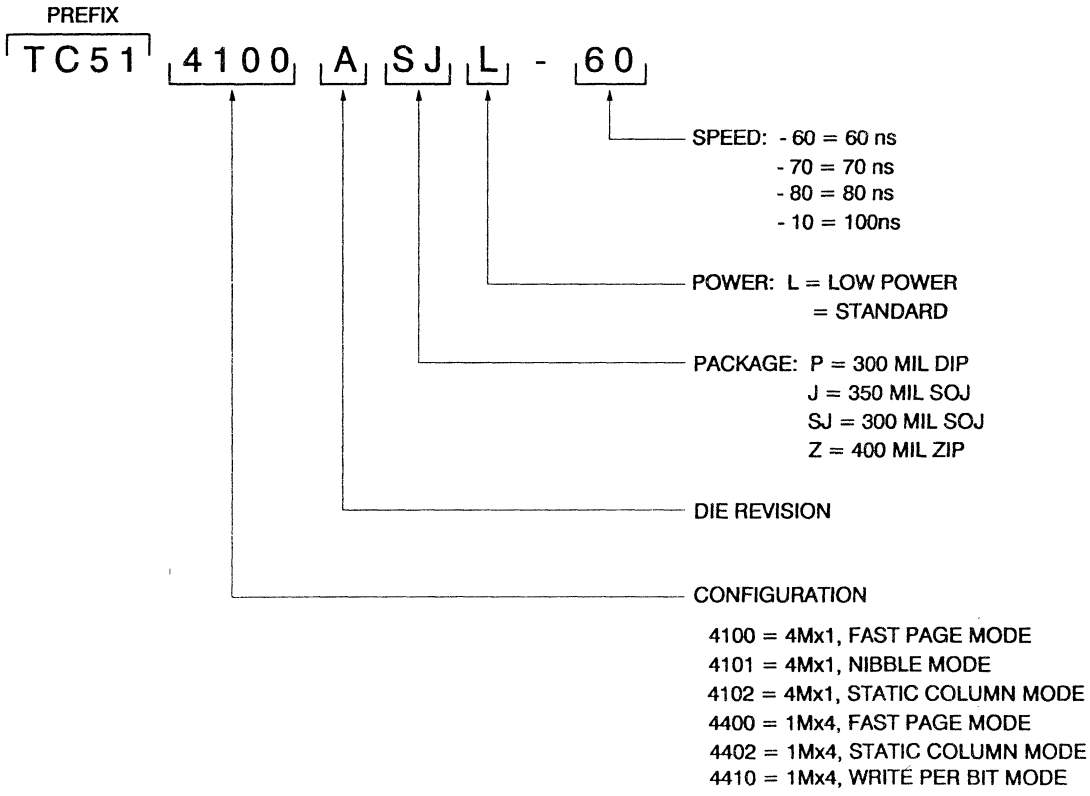
FUNCTION	FAST PAGE	STATIC COLUMN	FAST PAGE WRITE PER BIT
TOSHIBA	**TC514400AP/AJ/ASJ/AZ**	**TC514402AP/AJ/ASJ/AZ**	**TC514410AP/AJ/ASJ/AZ**
HITACHI	HM514400AJ/AS/AZ	HM514402AJ/AS/AZ	HM514410AJ/AS/AZ
NEC	MPD424400	MPD424402	MPD424410
MITSUBISHI	M5M44400J/L	M5M44402J/L	M5M44410J/L
OKI	MSM514400RS/JS/ZS	MSM514402RS/JS/ZS	
FUJITSU	MB814400		
PANASONIC	MN41C41000SJ/L		MN41C41002SJ/L
SAMSUNG	KM44C1000		
MICRON	MT4C4001		
TI	TMS44400		
MOSAIC	MDM41000		
MOTOROLA	MCM514400		
SIEMENS	HYB514400		
VITELIC	V53C404		

3. DRAM MODULE

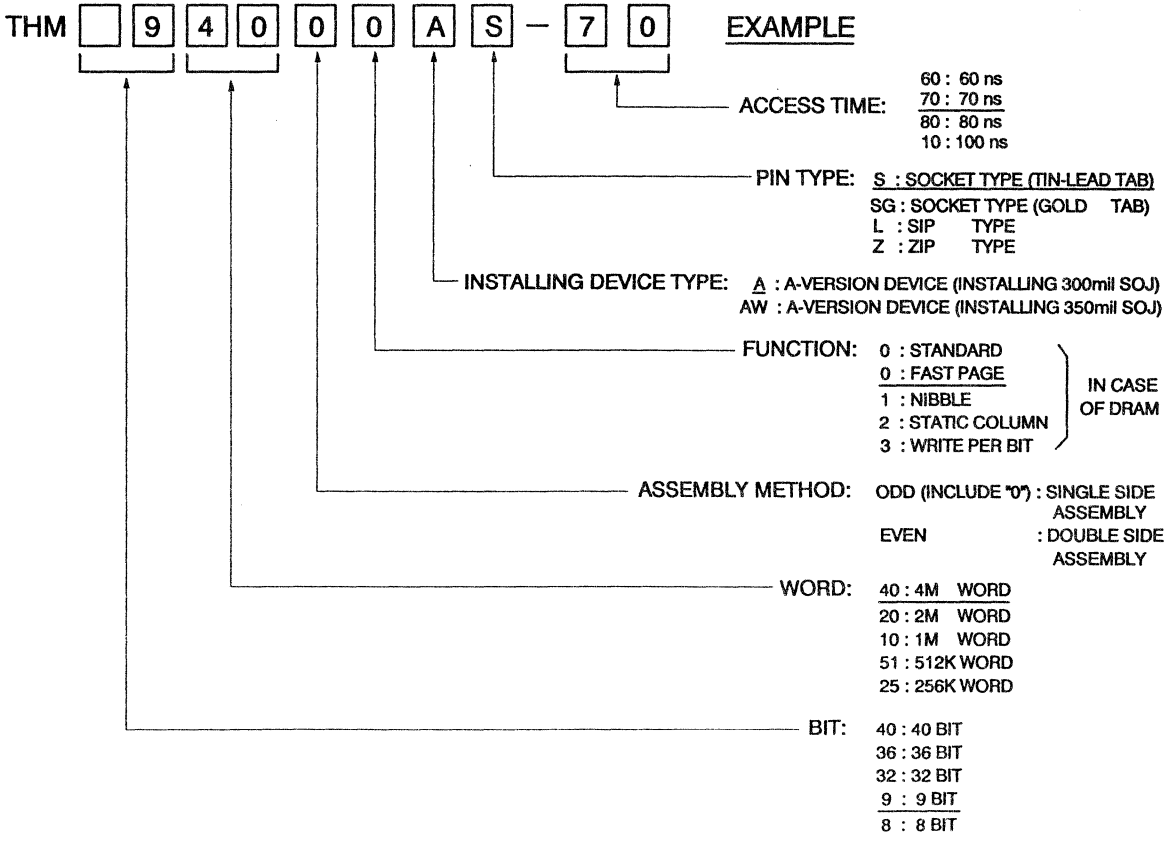
ORGANIZATION	4Mx8	1Mx32	4Mx9	1Mx36	1Mx40	2Mx32	2Mx36	2Mx40
TOSHIBA	THM84000	THM321000	THM94000	THM361020	THM401020	THM322020	THM362020	THM402020
HITACHI	HB56A48	HB56D132	HB56A49	HB56D136		HB56D232	HB56D236	
MITSUBISHI	MH4M08		MH4M09	MH1M36				
OKI	MSC2341		MSC2340	MSC2350				

PART NUMBER GUIDE

4M DRAM PART NUMBER GUIDE



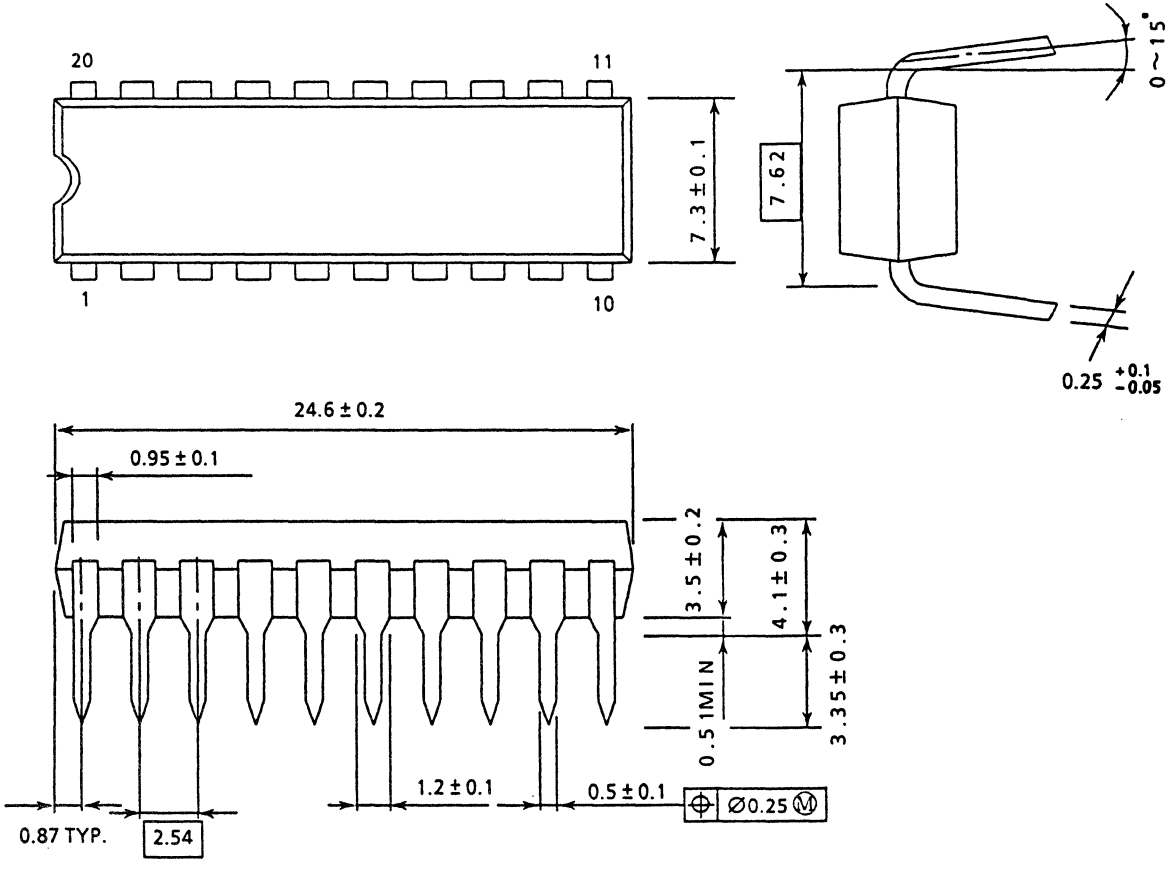
4M DRAM MODULES PART NUMBER GUIDE



COMPONENT MECHANICAL DIMENSIONS

300 MIL WIDTH DIP OUTLINE DRAWING

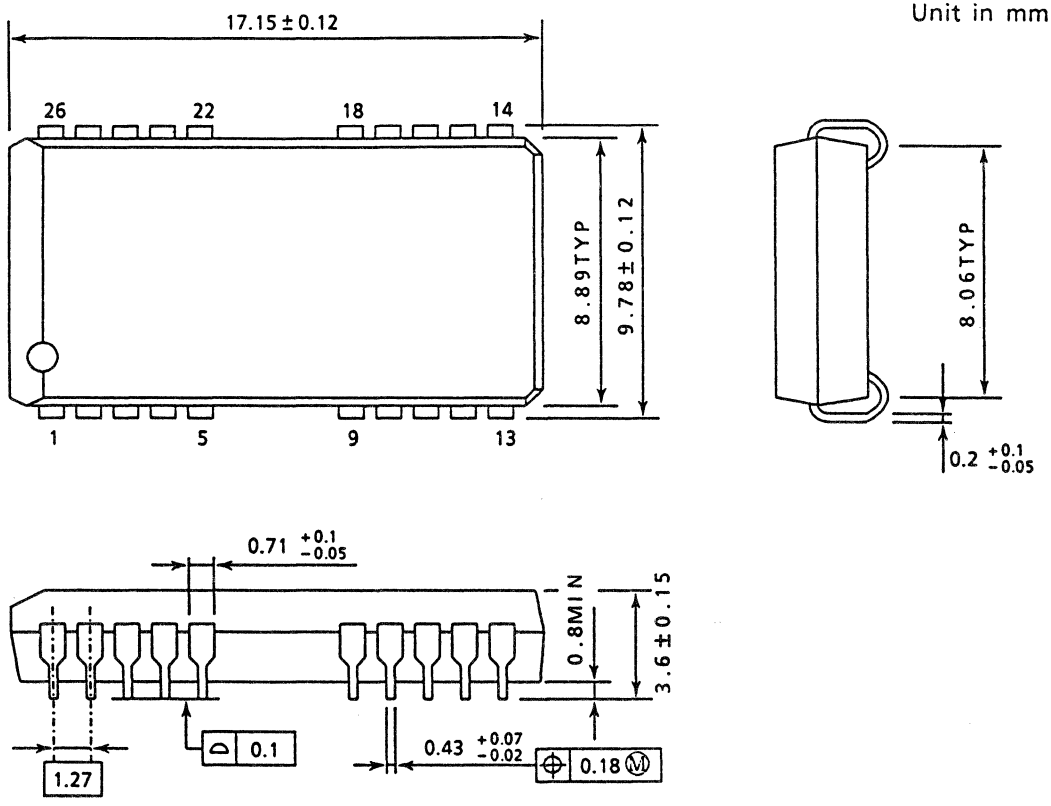
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

350 MIL WIDTH SOJ PACKAGE OUTLINE DRAWING

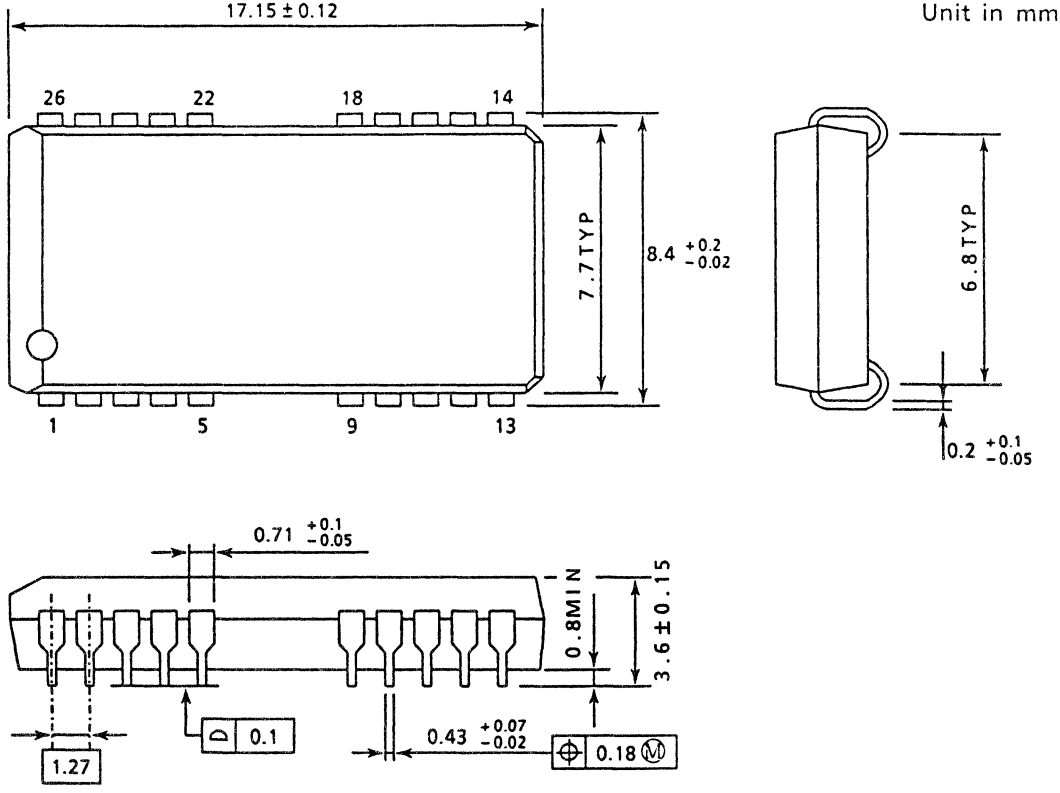
Unit in mm



Note: **Package width and length do not include mold protrusion,** allowable mold protrusion is 0.15mm.

300 MIL WIDTH SOJ PACKAGE OUTLINE DRAWING

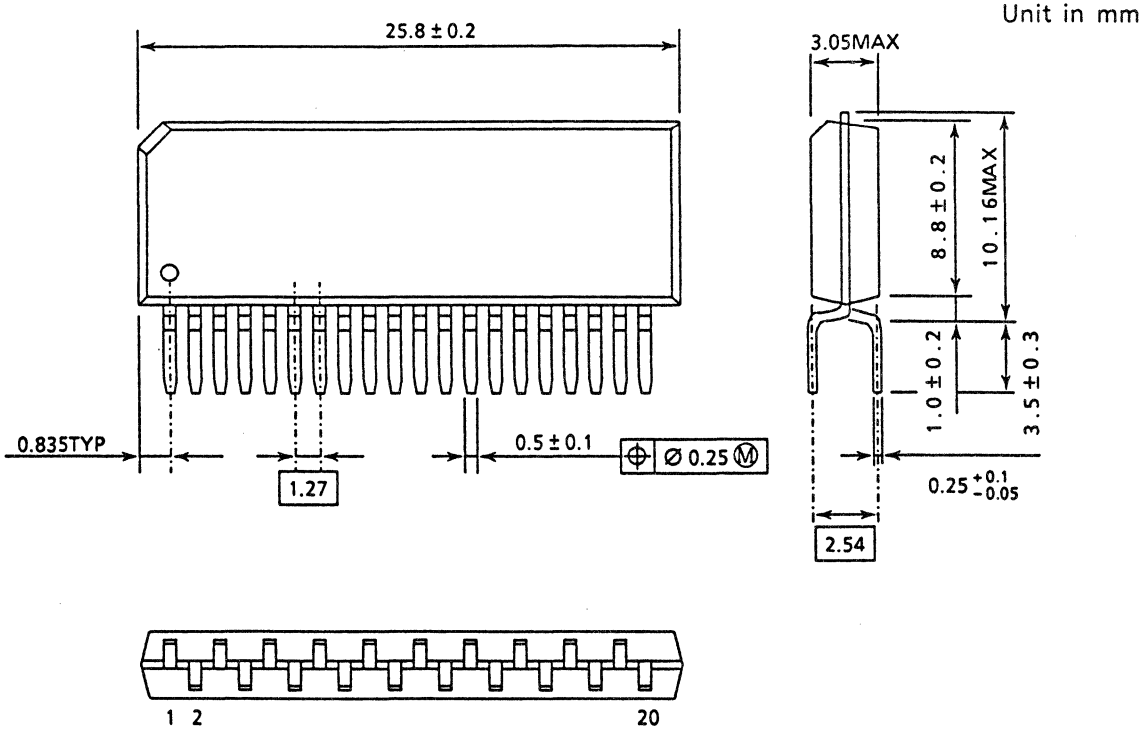
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

400 MIL HEIGHT ZIP OUTLINE DRAWING

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

DYNAMIC RAM

4,194,304 WORD × 1 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514100J/Z is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514100J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514100J/Z to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

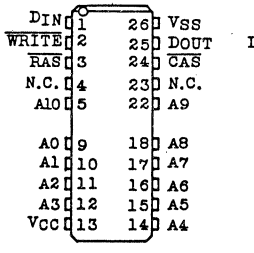
- 4,194,304 word by 1 bit organization
- Fast access time and cycle time

		TC514100J/Z-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

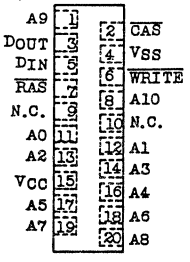
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  550mW Operating (TC514100J/Z-80)
  468mW Operating (TC514100J/Z-10)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and output TTL compatible
- 1024 refresh cycles/16ms
- Package Plastic SOJ: TC514100J
  Plastic ZIP: TC514100Z

PIN CONNECTION (TOP VIEW)

Plastic SOJ



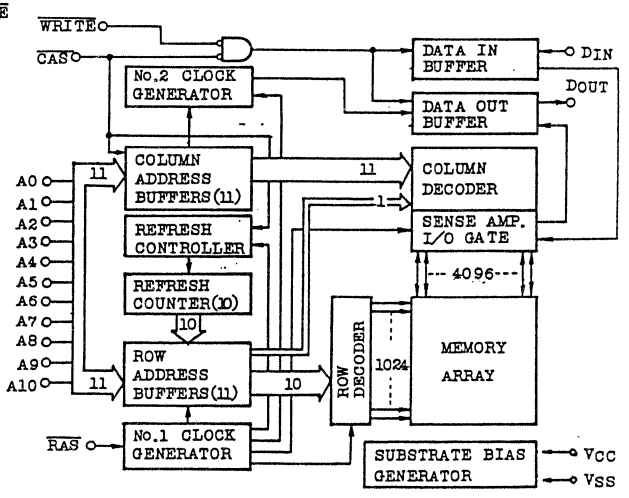
Plastic ZIP



PIN NAMES

A0 ∿ A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	-1∿7	V	1
Output Voltage	V_{OUT}	-1∿7	V	1
Power Supply Voltage	V_{CC}	-1∿7	V	1
Operating Temperature	T_{OPR}	0∿70	°C	1
Storage Temperature	T_{STG}	-55∿150	°C	1
Soldering Temperature・Time	T_{SOLDER}	260・10	°C・sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0∿70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514100J/Z-80	-	100	mA	3,4,5
		TC514100J/Z-10	-	85		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514100J/Z-80	-	100	mA	3,5
		TC514100J/Z-10	-	85		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC514100J/Z-80	-	60	mA	3,4,5
		TC514100J/Z-10	-	50		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514100J/Z-80	-	100	mA	3
		TC514100J/Z-10	-	85		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≦V_{IN}≦6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V≦V_{OUT}≦5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ~ 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514100J/Z-80		TC514100J/Z-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	175	-	210	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	60	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	75	-	90	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	40	-	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	55	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	-	55	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	20	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

SYMBOL	PARAMETER	TC514100J/Z -80		TC514100J/Z -10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	20	-	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	25	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80	-	100	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	40	-	50	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time (Fast Page Mode)	45	-	55	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{WTS}	Write Command Set-Up Time(Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514100J/Z -80		TC514100J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	155	-	185	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	105	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	30	ns	9,14
t_{AA}	Access Time from Column Address	-	45	-	55	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	60	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	105	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	50	-	60	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume $t_T=5ns$.

8. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.

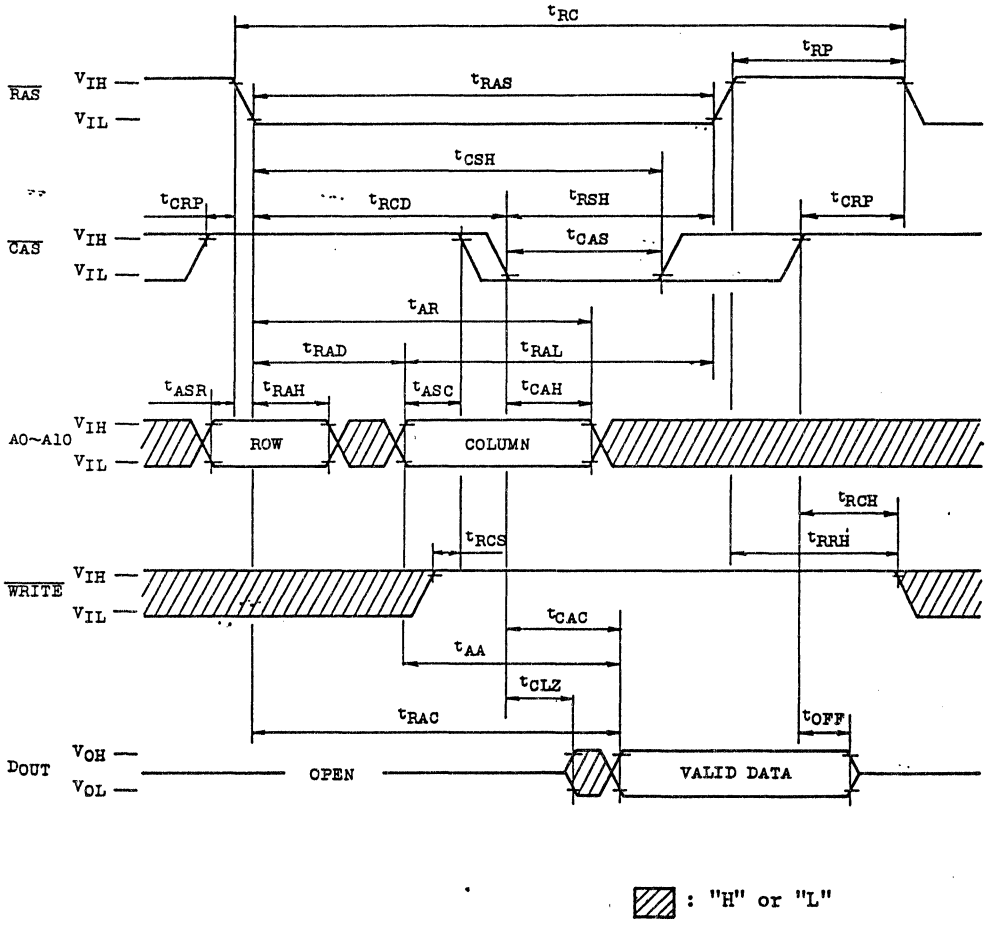
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet at electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWD} \geq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

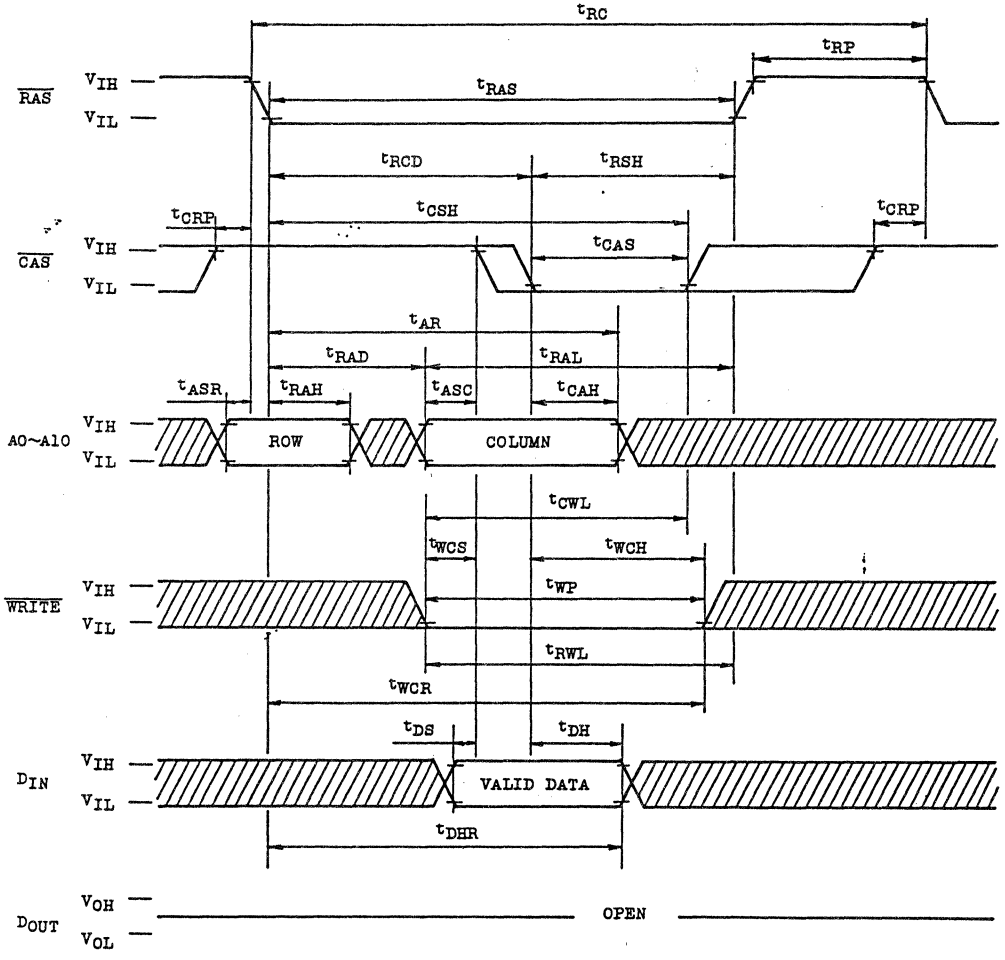
TIMING WAVEFORMS

READ CYCLE



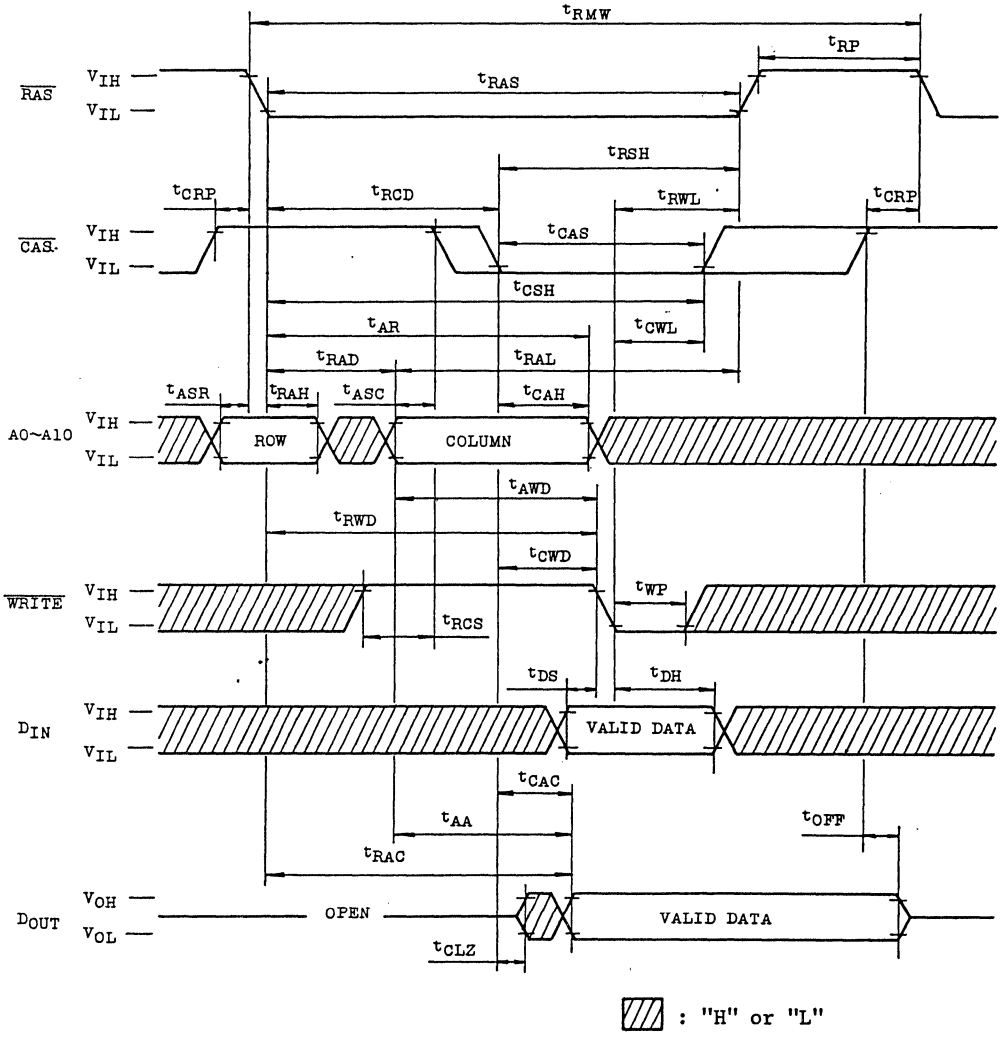
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)

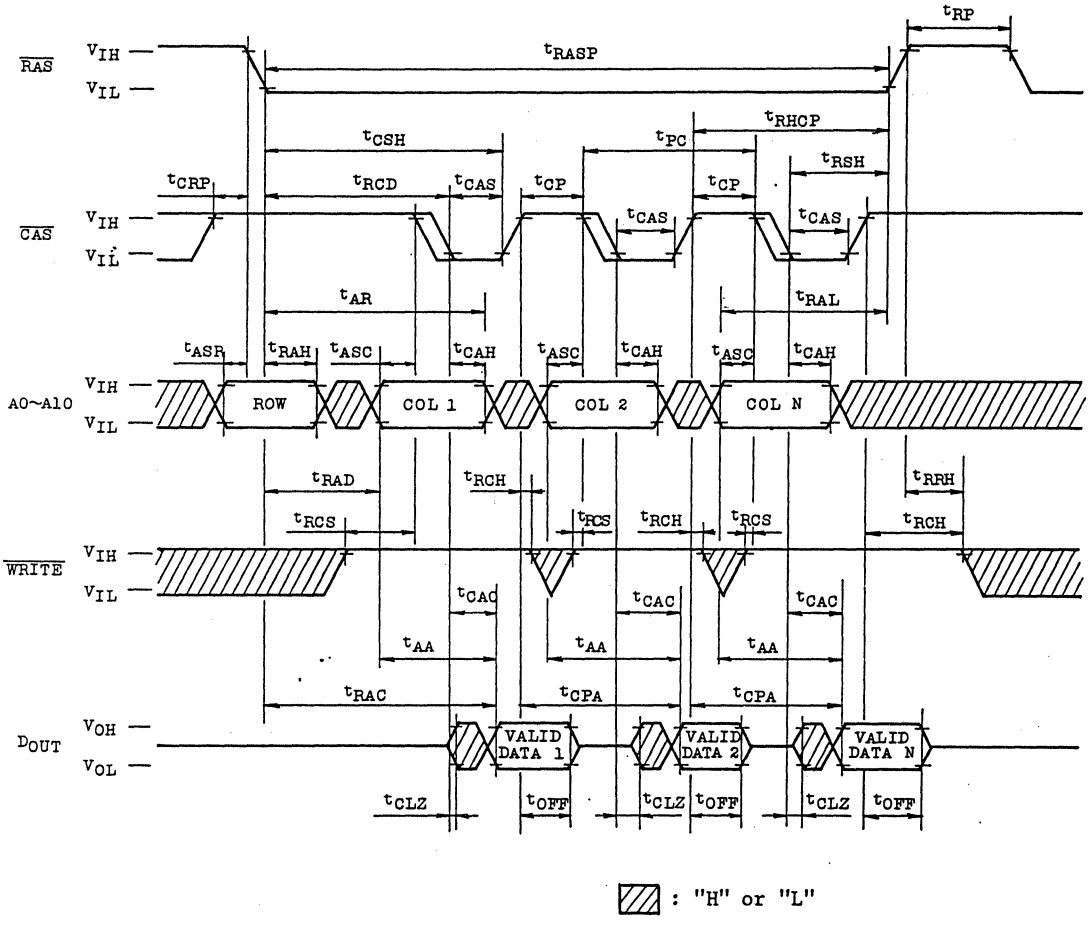


▨ : "H" or "L"

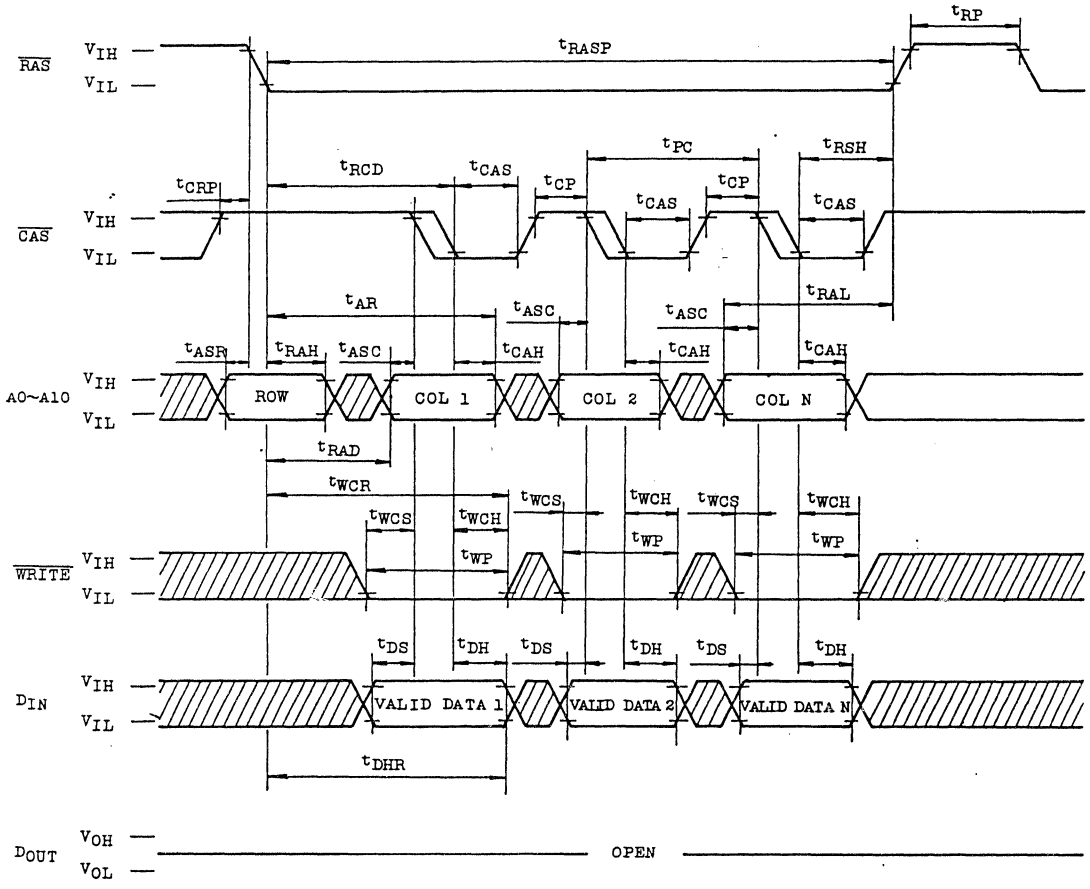
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

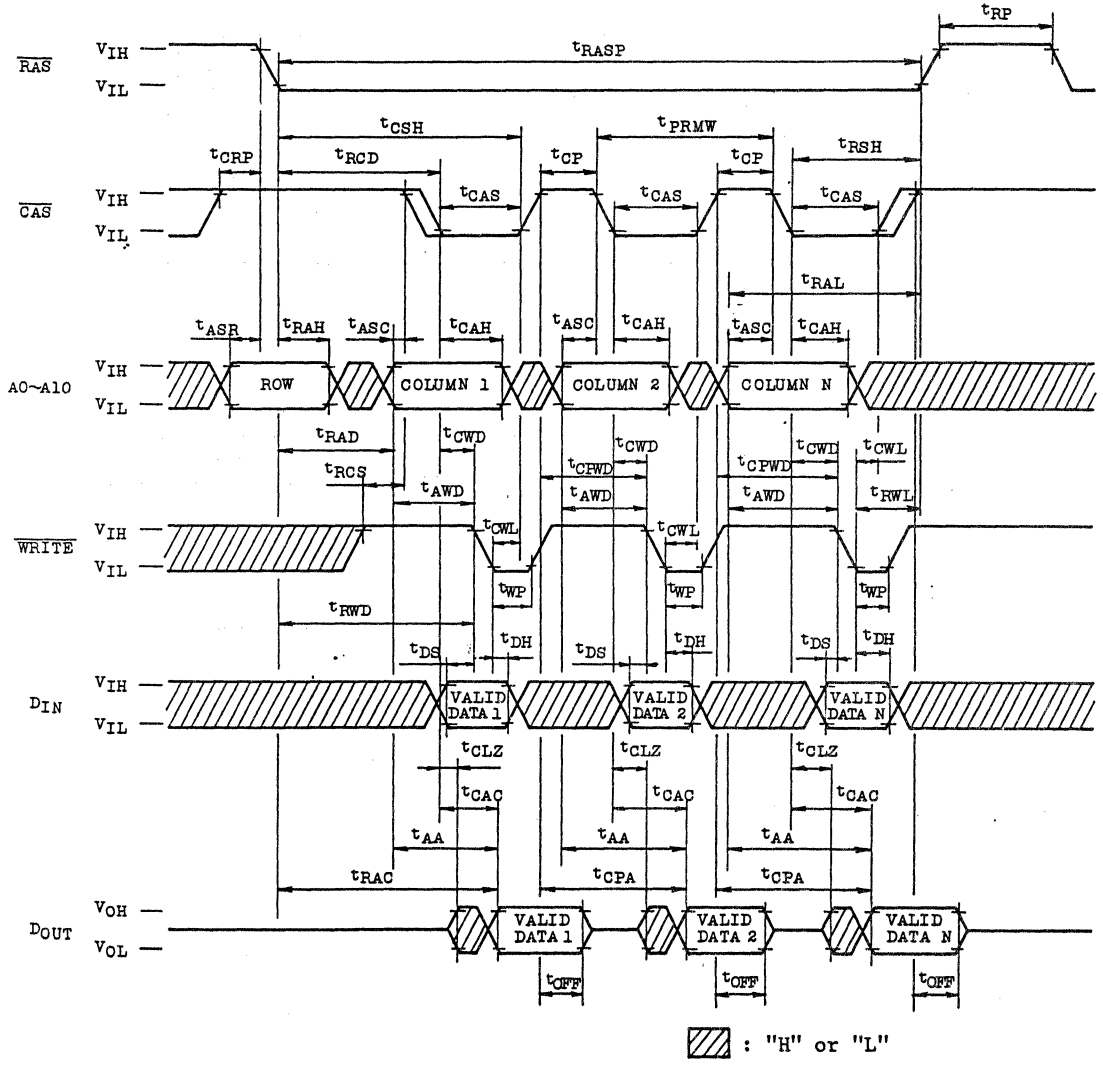


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

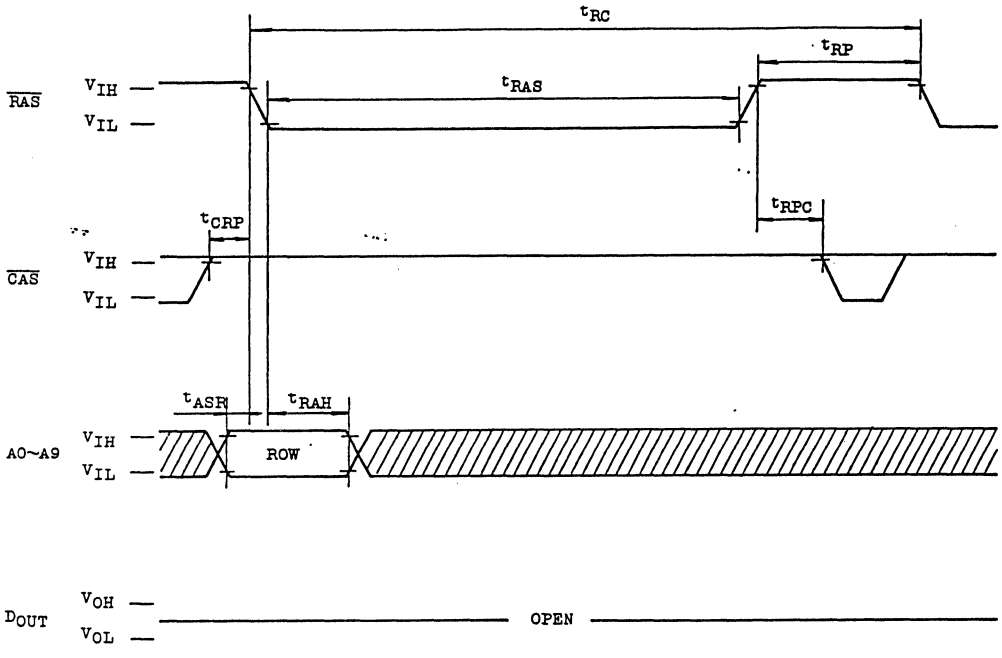


▨: "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



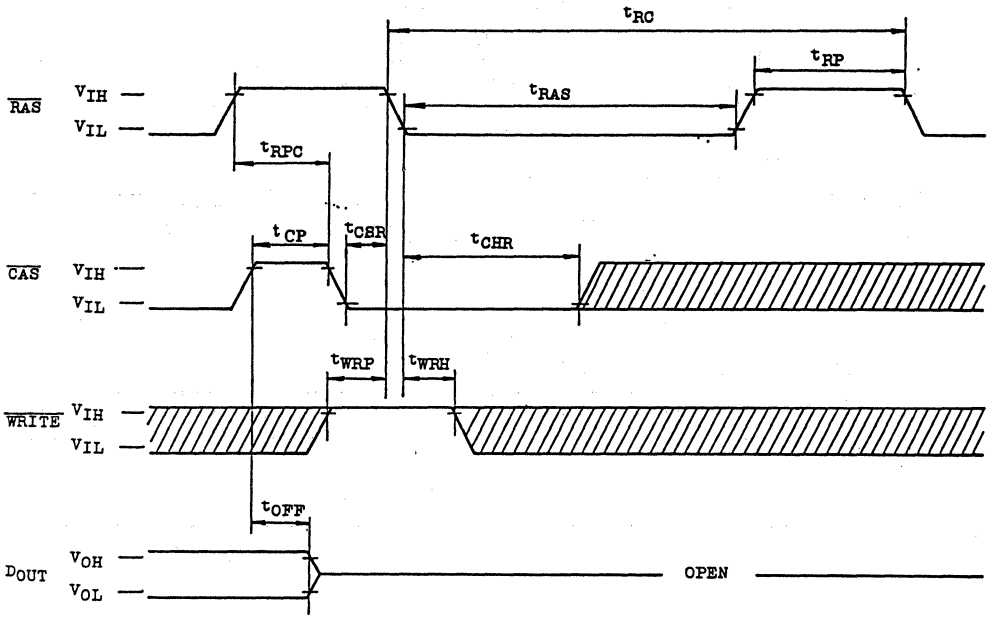
$\overline{RAS}$ ONLY REFRESH CYCLE



▨ : "H" or "L"

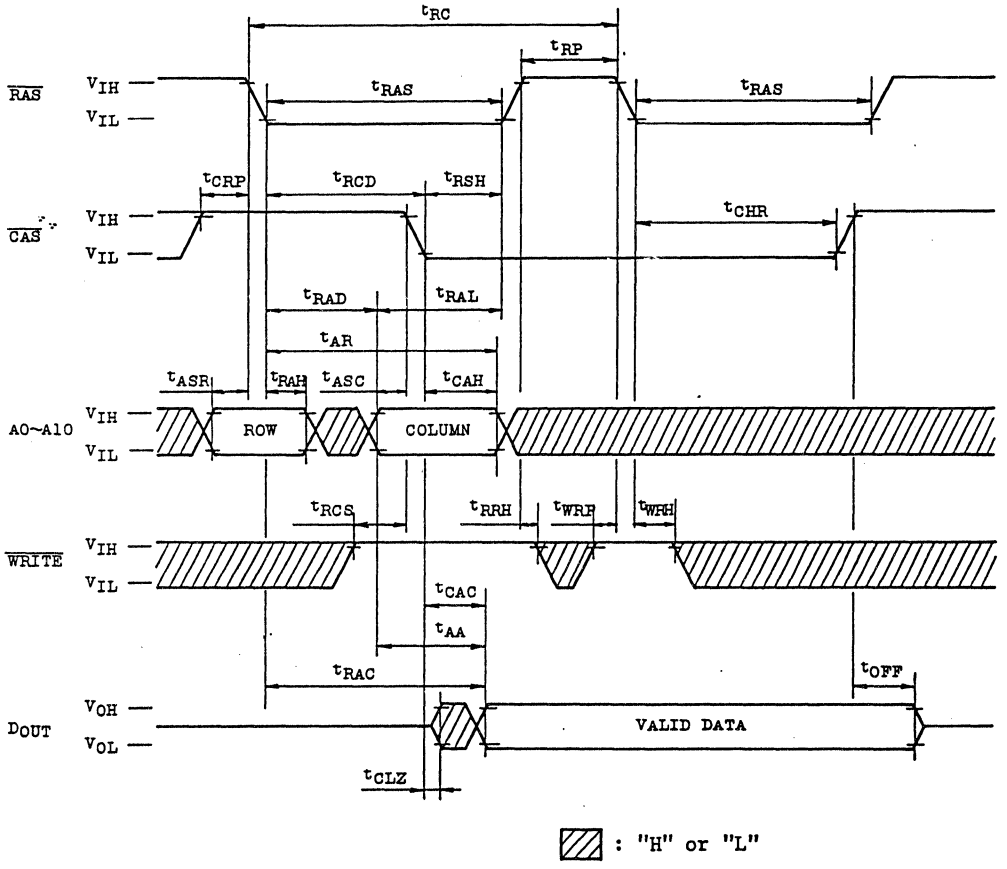
NOTE: $\overline{WRITE}$="H" or "L", A10="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

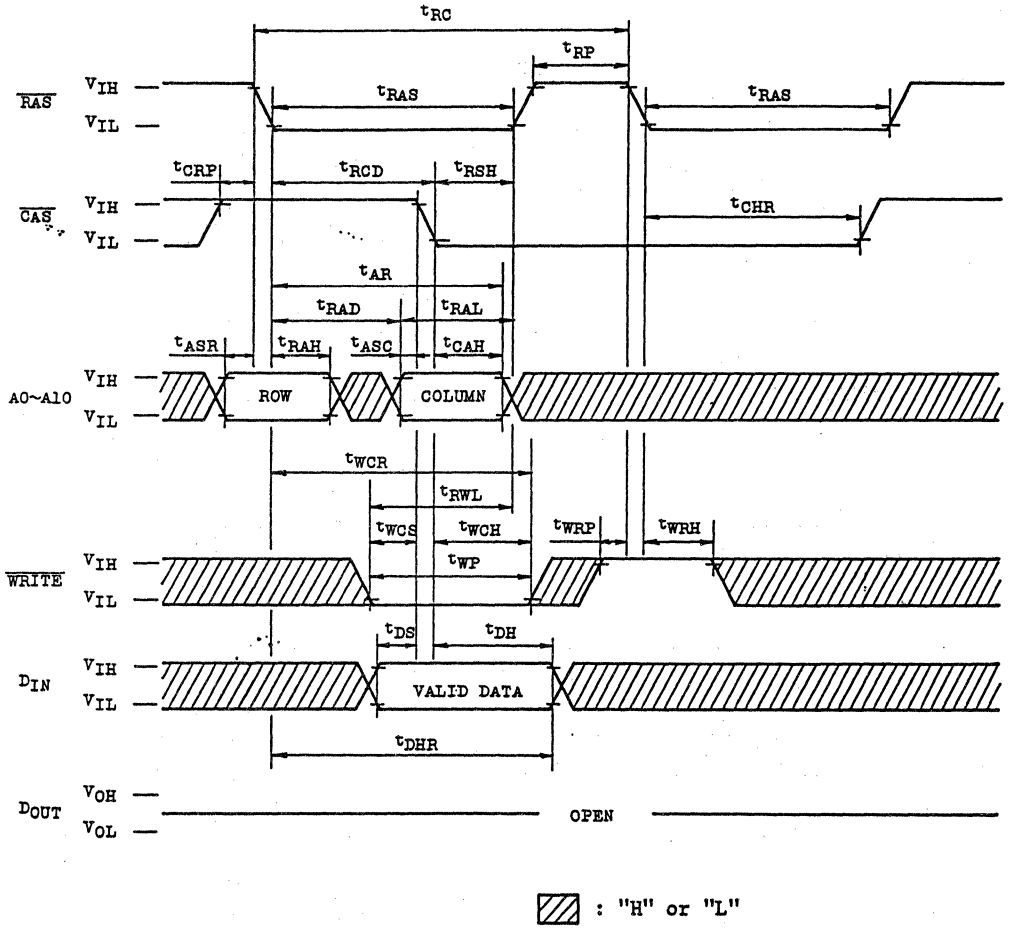


NOTE: A0 ~ A10="H" or "L" ▨ : "H" or "L"

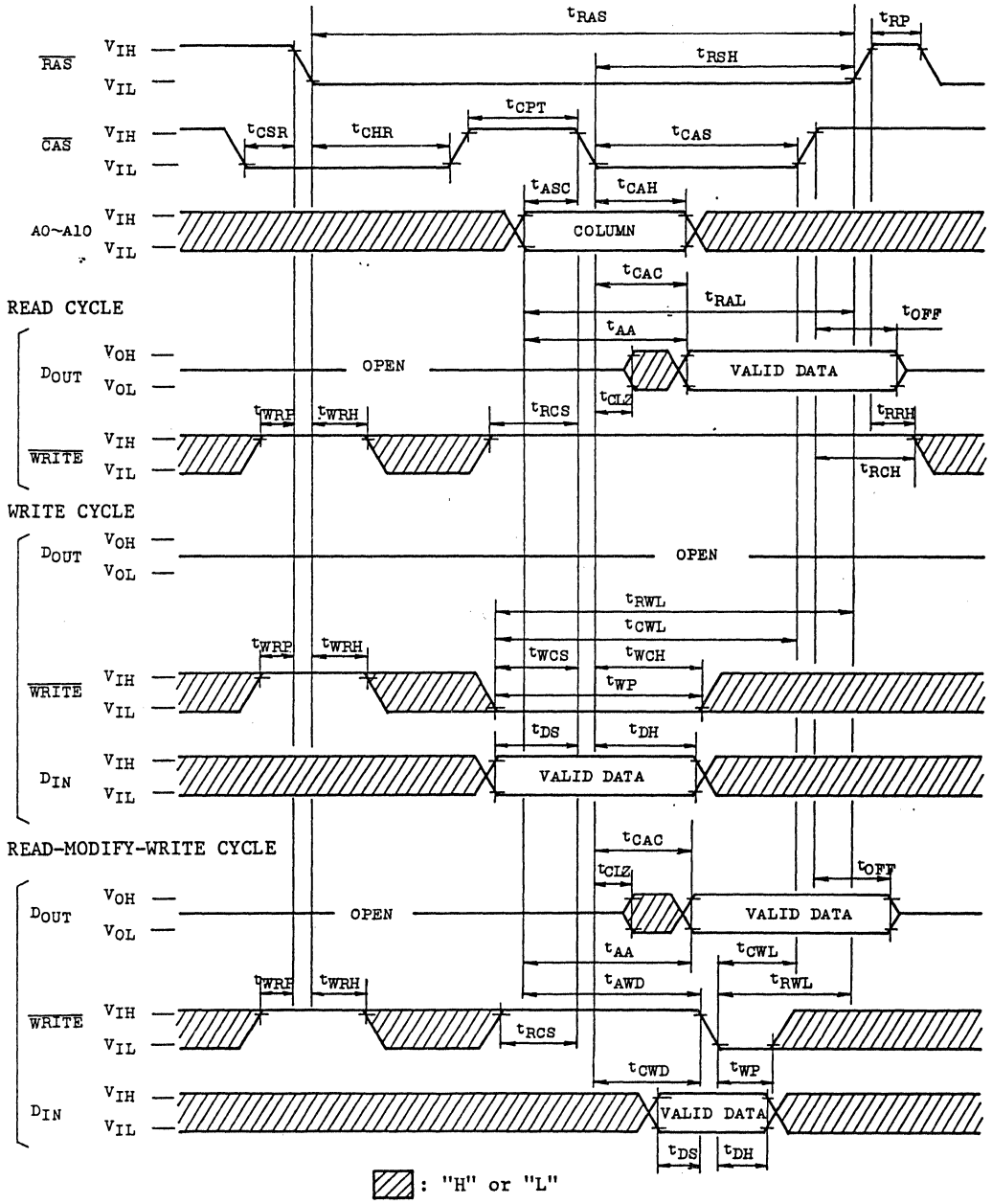
HIDDEN REFRESH CYCLE (READ)



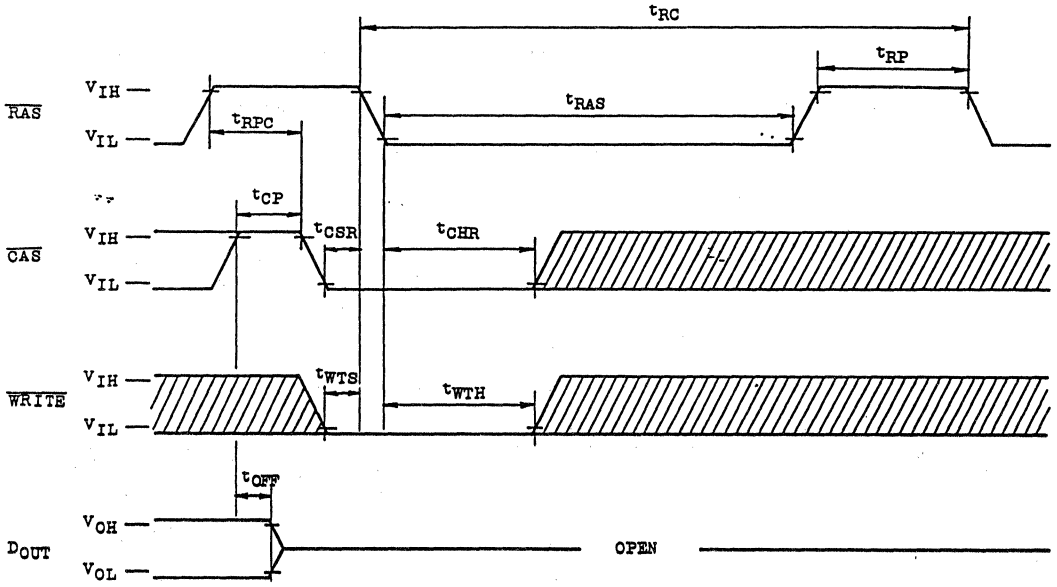
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



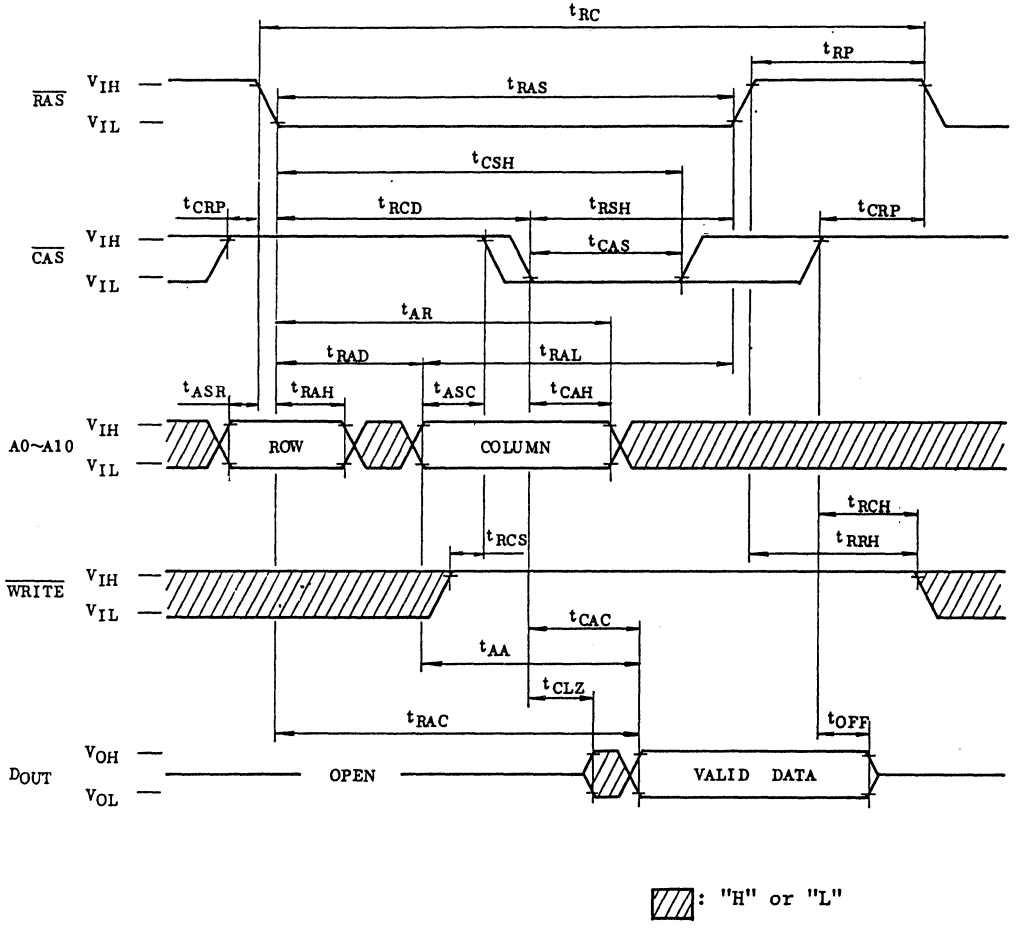
WRITE, CAS BEFORE RAS REFRESH CYCLE



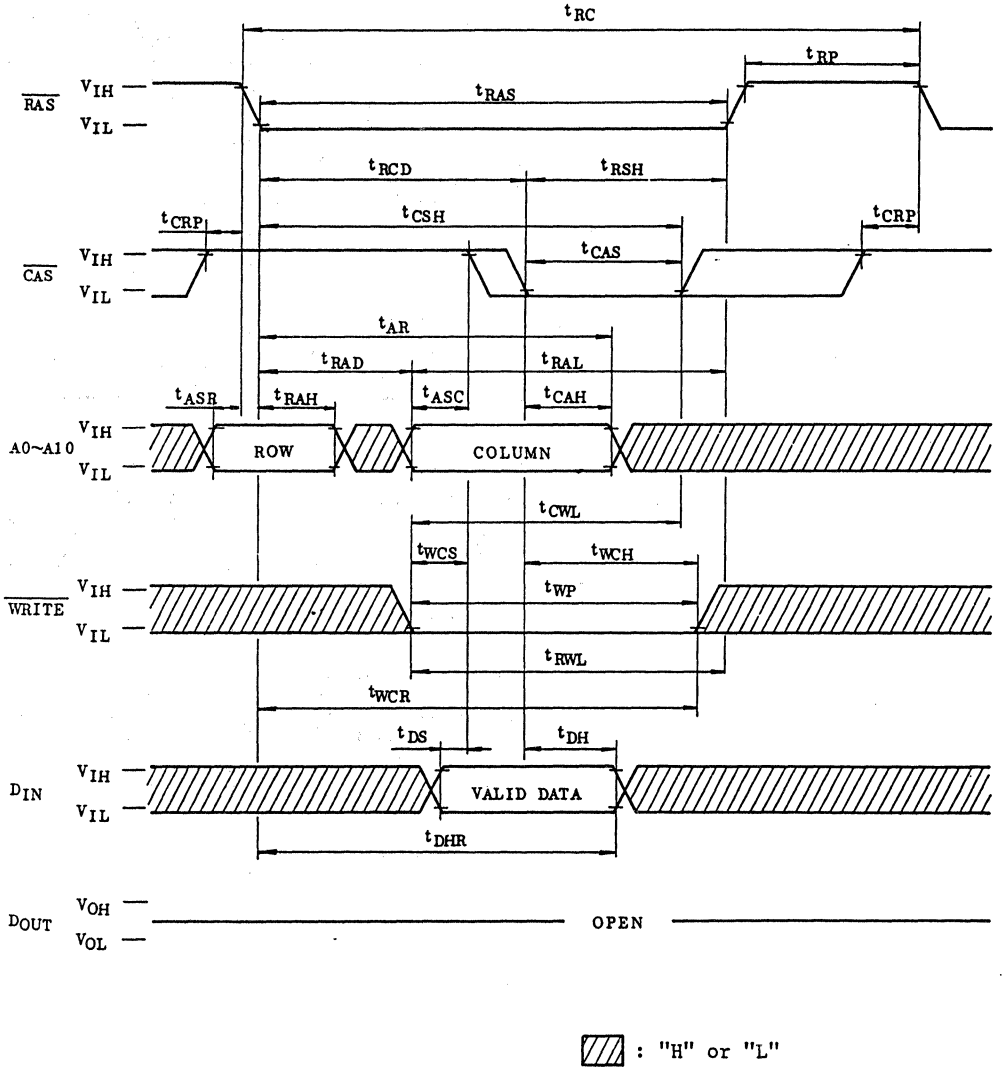
NOTE: D_{IN}, A0 ~ A10: "H" or "L"

▨: "H" or "L"

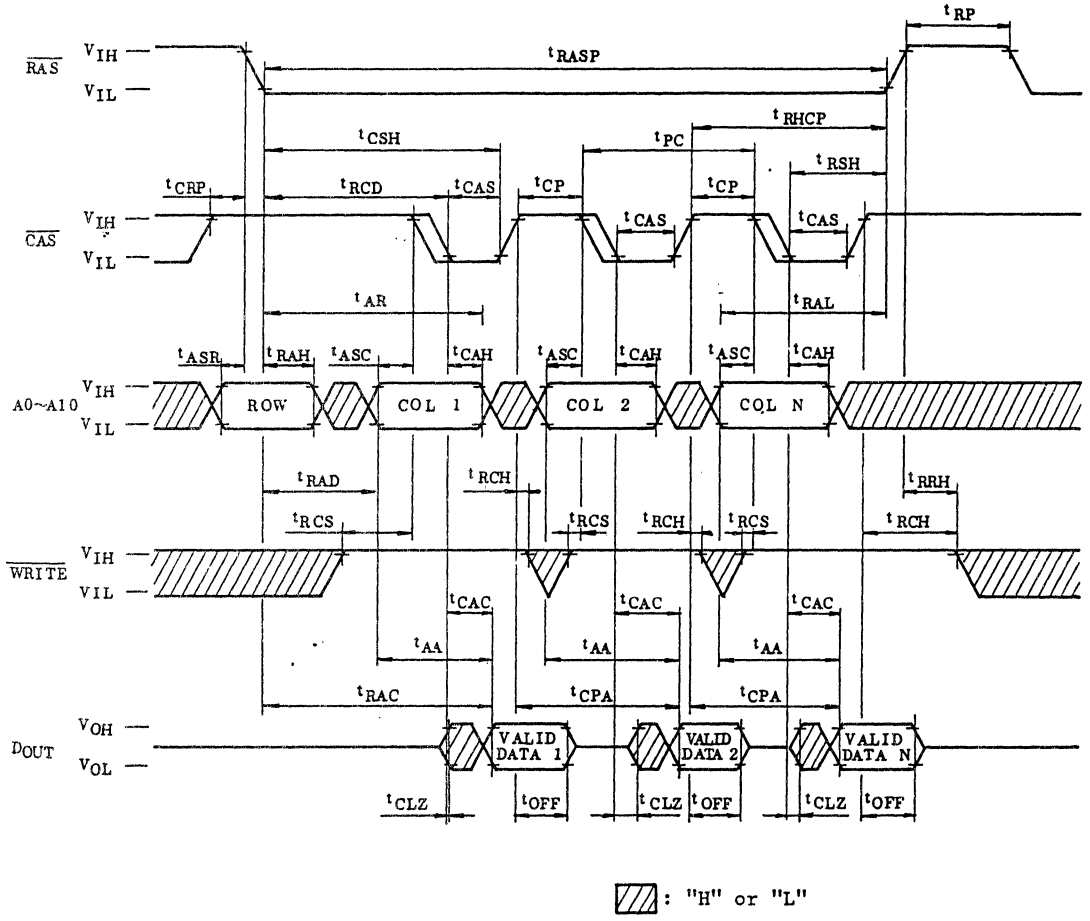
READ CYCLE IN THE TEST MODE



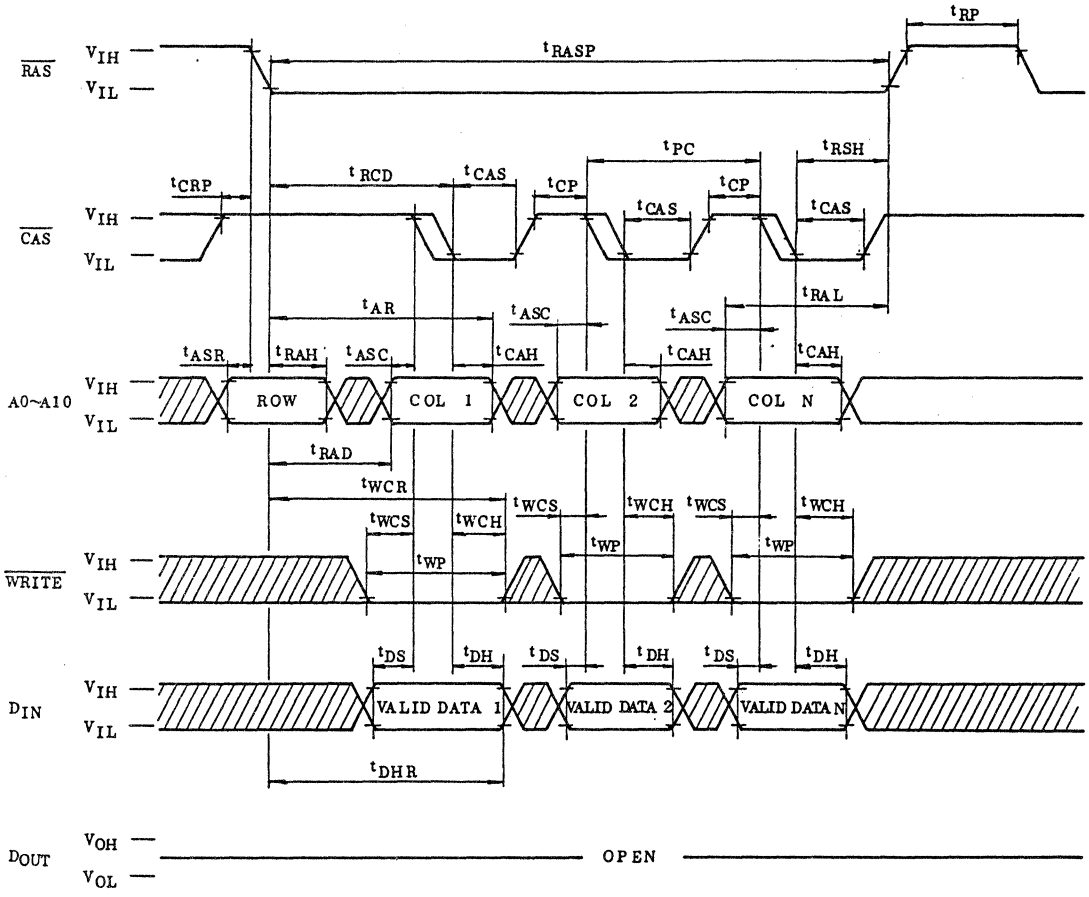
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



FAST PAGE MODE READ CYCLE IN THE TEST MODE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



TEST MODE

The TC514100J/Z is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 secotrs in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig. 1 shows the block diagram of TC514100J/Z. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycel" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern)..

BLOCK DIAGRAM IN THE TEST MODE

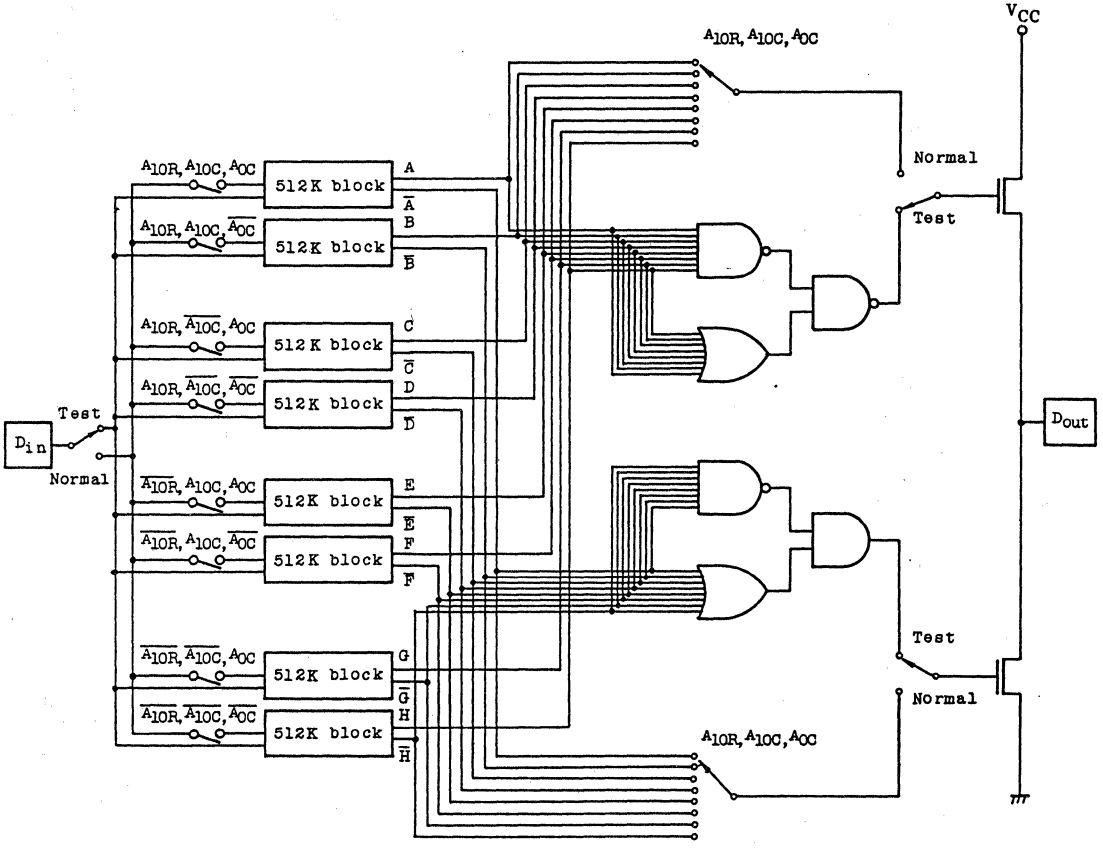


Fig. 1

4,194,304 WORD x 1 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514100JL/ZL is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514100JL/ZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514100JL/ZL to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

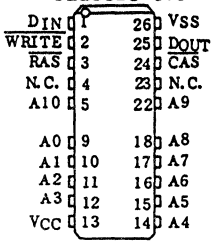
- 4,194,304 word by 1 bit organization
- Fast access time and cycle time

		TC514100JL/ZL-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

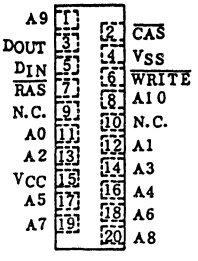
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  550mW Operating (TC514100JL/ZL-80)
  468mW Operating (TC514100JL/ZL-10)
  2.2mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package Plastic SOJ: TC514100JL
  Plastic ZIP: TC514100ZL

PIN CONNECTION (TOP VIEW)

Plastic SOJ



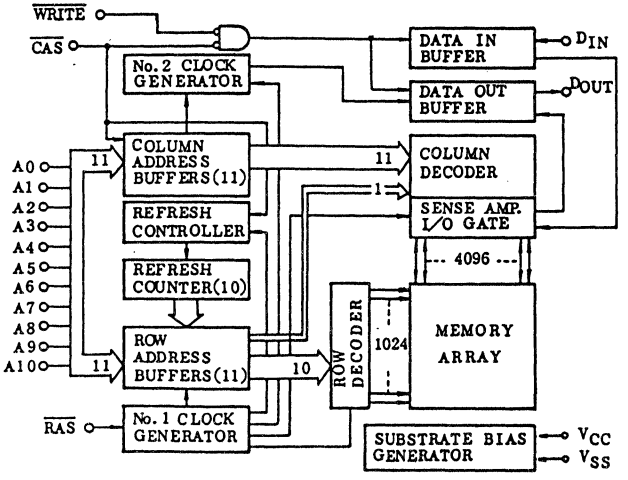
Plastic ZIP



PIN NAMES

A0 ∿ A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($Ta=0 \sim 70°C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $Ta=0 \sim 70°C$)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC}=t_{RC}$ MIN.)	TC514100JL/ZL-80	-	100	mA	3,4,5
		TC514100JL/ZL-10	-	85		
I_{CC2}	Standby Current Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		-	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$: $t_{RC}=t_{RC}$ MIN.)	TC514100JL/ZL-80	-	100	mA	3,5
		TC514100JL/ZL-10	-	85		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}=V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC}=t_{PC}$ MIN.)	TC514100JL/ZL-80	-	60	mA	3,4,5
		TC514100JL/ZL-10	-	50		
I_{CC5}	Standby Current Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$)		-	400	µA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	TC514100JL/ZL-80	-	100	mA	3
		TC514100JL/ZL-10	-	85		
I_{CC7}	Battery Back Up Current Average Power Supply Current, Battery Back Up Mode ($\overline{CAS}=\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{WRITE}=V_{CC}-0.2V$ A0 ∿ 10=$V_{CC}-0.2V$ or 0.2V, $D_{IN}=V_{CC}-0.2V$, 0.2V or OPEN: $t_{RC}=125\mu s$, $t_{RAS}=t_{RAS}$ MIN. ∿ 1µs)		-	500	µA	3,6
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		-10	10	µA	
V_{OH}	Output Level Output "H" Level Voltage ($I_{OUT}=-5mA$)		2.4	-	V	
V_{OL}	Output Level Output "L" Level Voltage ($I_{OUT}=4.2mA$)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ~ 70°C) (Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514100JL/ZL-80		TC514100JL/ZL-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	175	-	210	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	60	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	75	-	90	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	ns	10.15.16
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	10,16
t_{AA}	Access Time from Column Address	-	40	-	50	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	55	ns	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t_{T}	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	-	55	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	12
t_{WCH}	Write Command Hold Time	15	-	20	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514100JL/ ZL-80		TC514100JL/ ZL-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	13
t_{DH}	Data Hold Time	15	-	20	-	ns	13
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	128	-	128	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	25	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80	-	100	-	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	40	-	50	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time (Fast Page Mode)	45	-	55	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{WTS}	Write Command Set-Up Time(Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN TEST MODE

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514100JL/ZL-80		TC514100JL/ZL-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	155	-	185	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	105	ns	10,15,16
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	30	ns	10,15
t_{AA}	Access Time from Column Address	-	45	-	55	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	60	ns	10
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	105	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	50	-	60	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Column address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

6. t_{RAS}(max.)=1μs is only applied to refresh of battery-back up. t_{RAS}(max.)=10μs is applied to functional operating.

7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

8. AC measurements assume t_T=5ns.

9. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

13. These parameters are referenced to CAS leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.

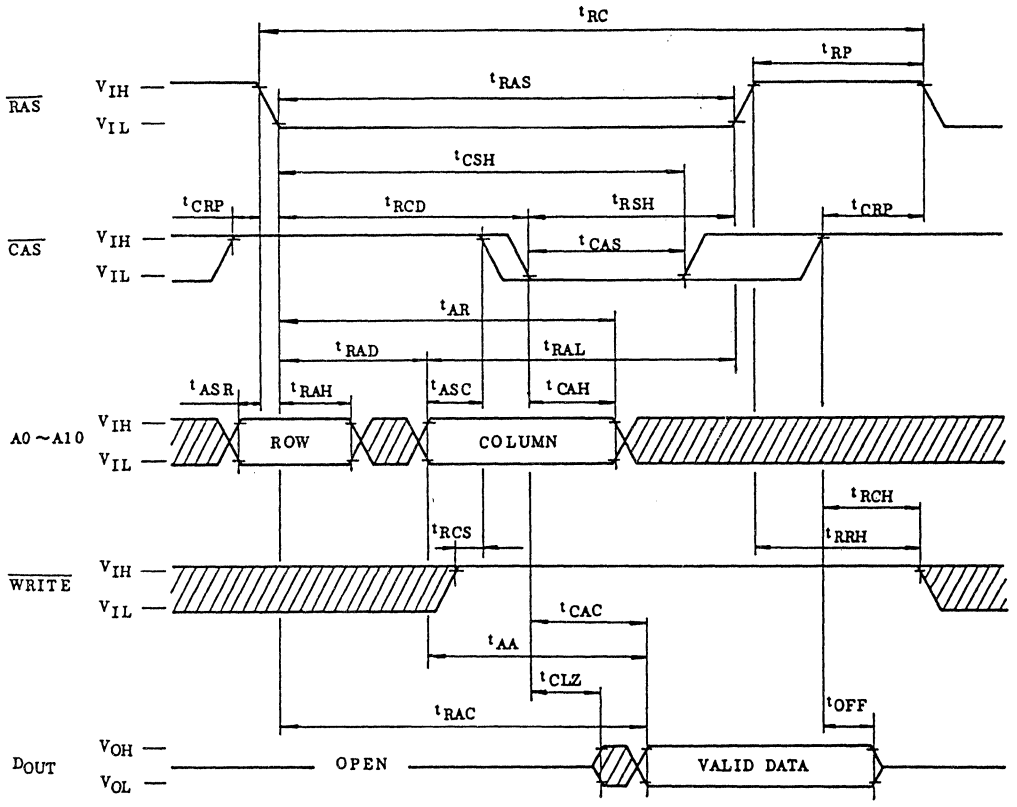
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPWD} \geq t_{CPWD}$(min.) (Fast Page Mode), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

15. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

16. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

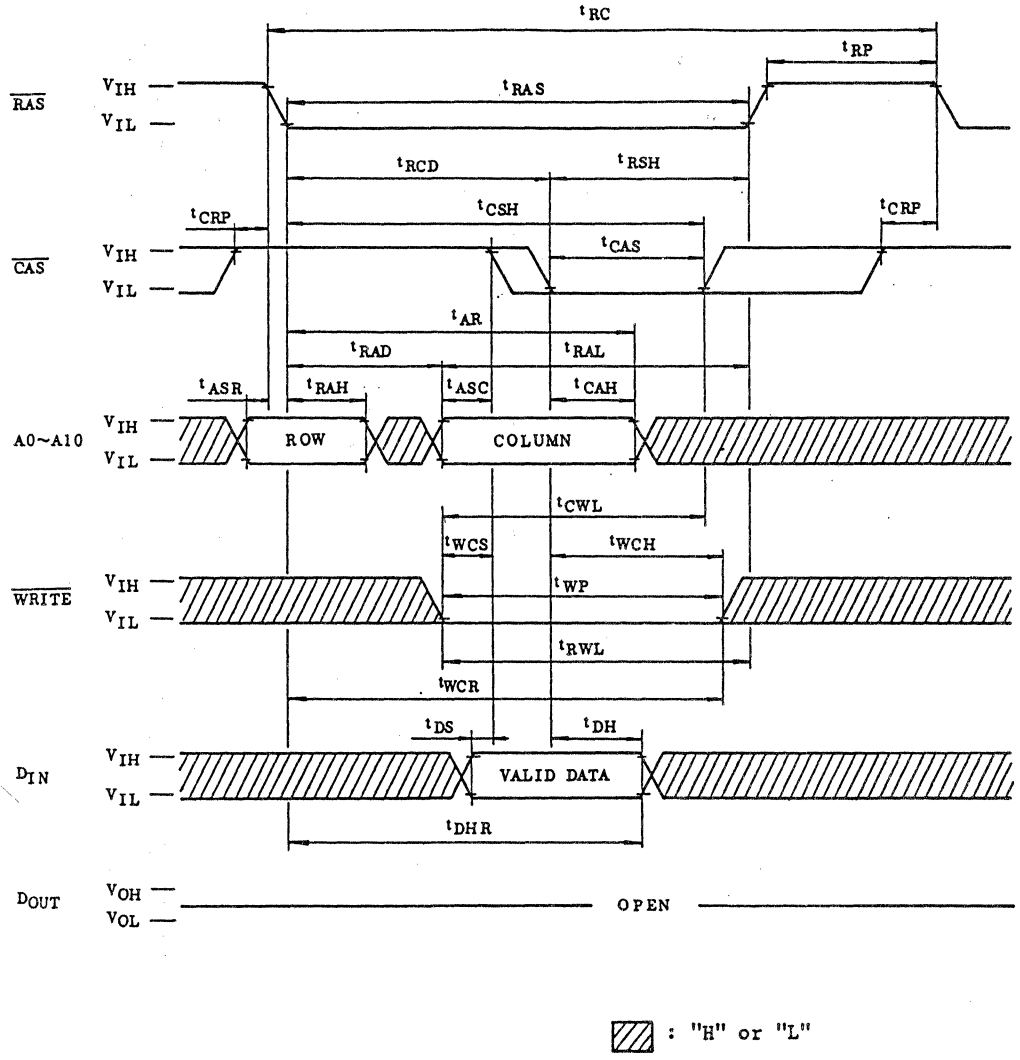
TIMING WAVEFORMS

READ CYCLE



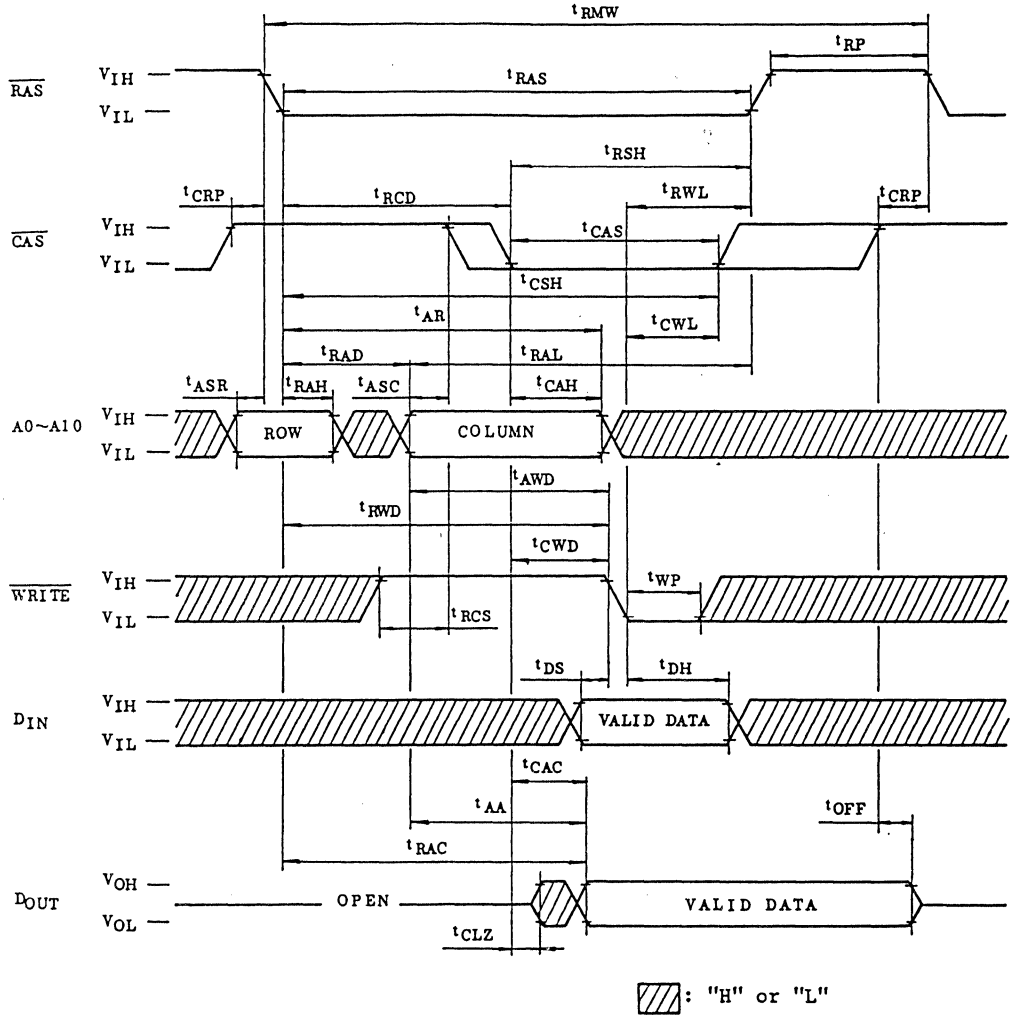
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)

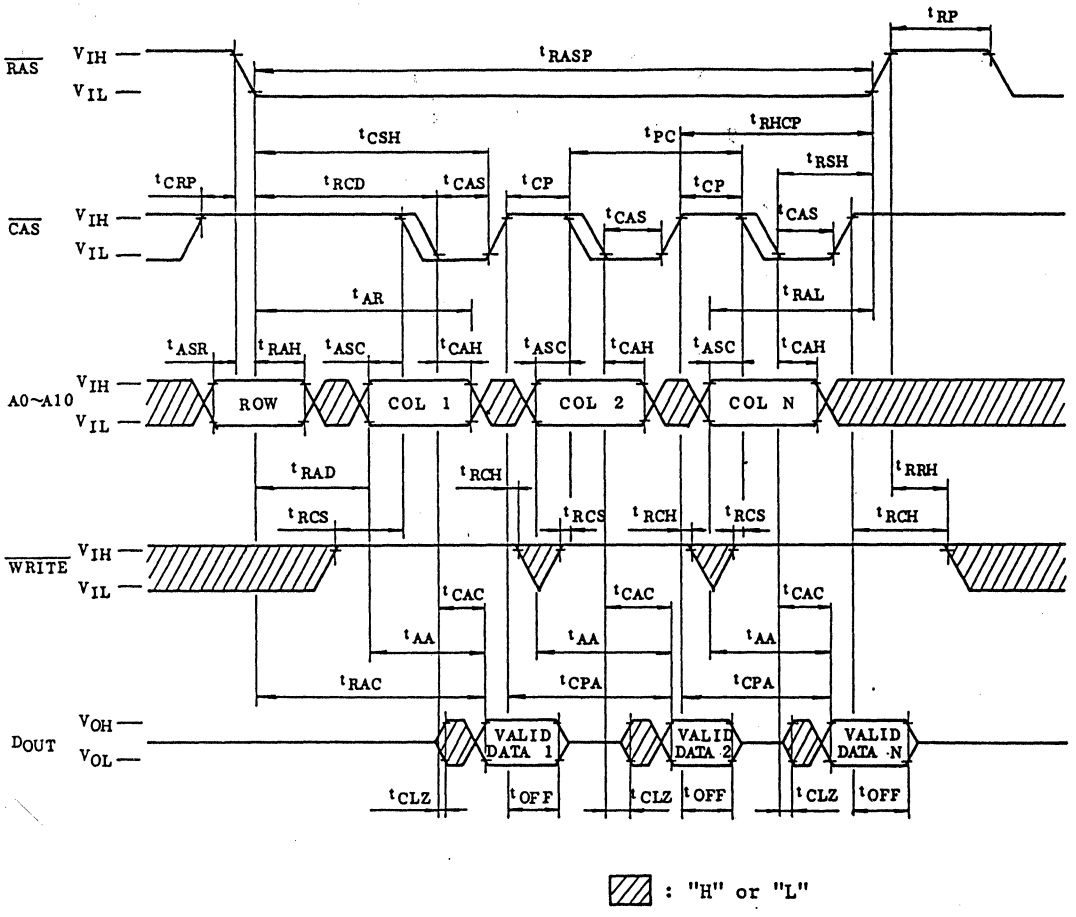


▨ : "H" or "L"

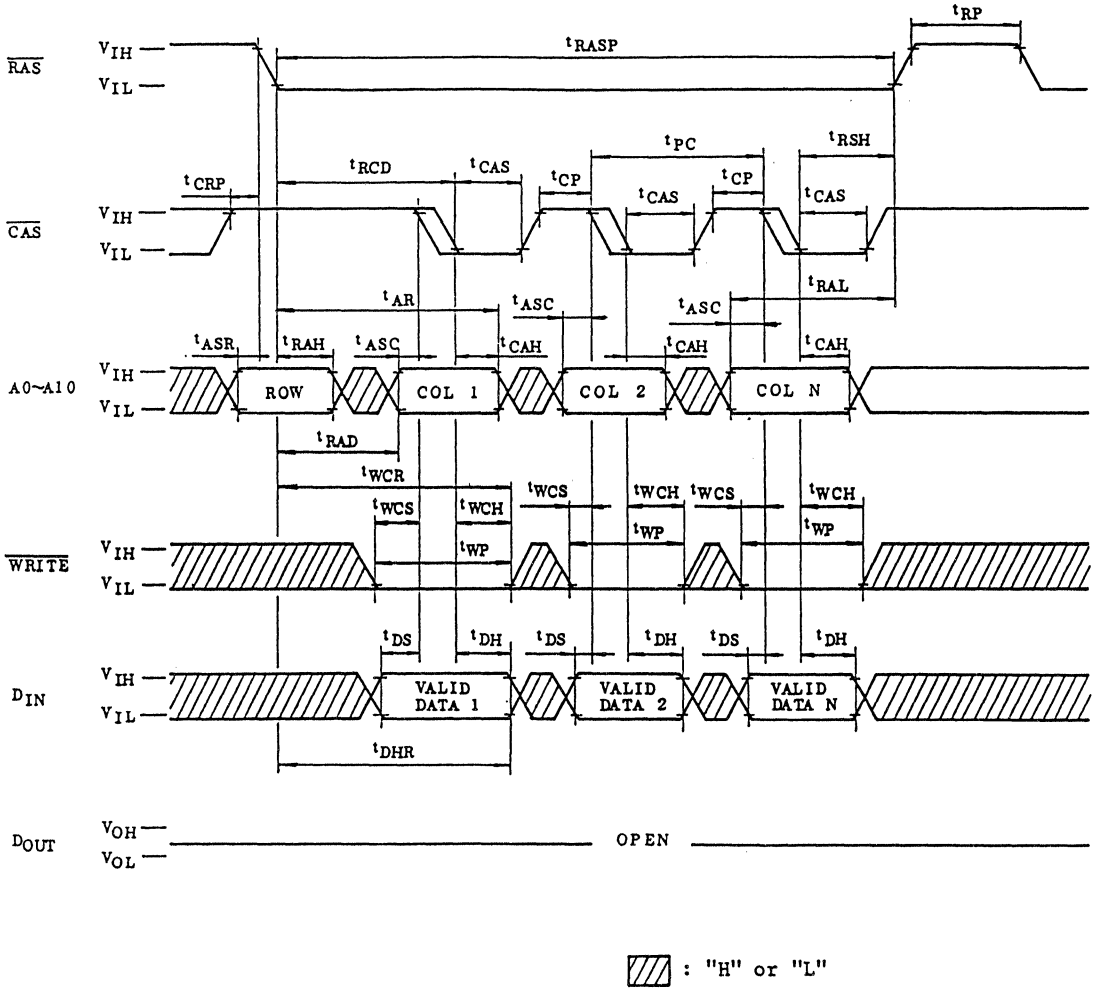
READ-MODIFY-WRITE CYCLE



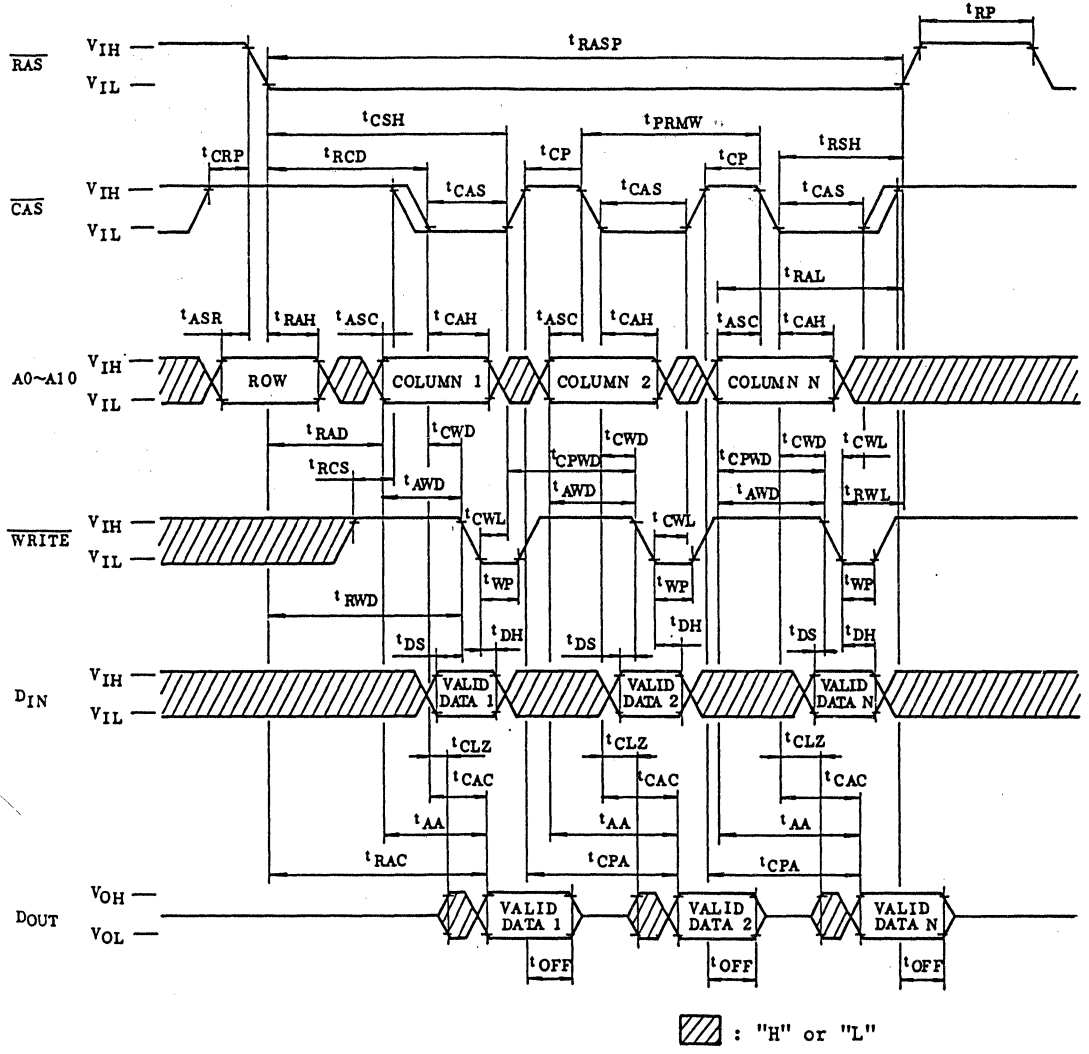
FAST PAGE MODE READ CYCLE



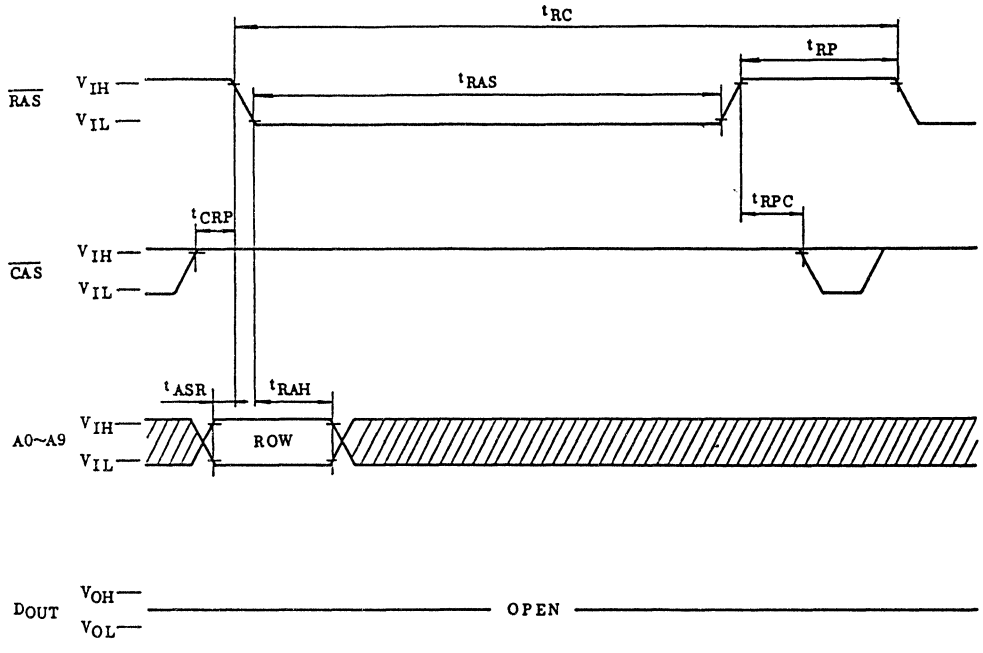
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



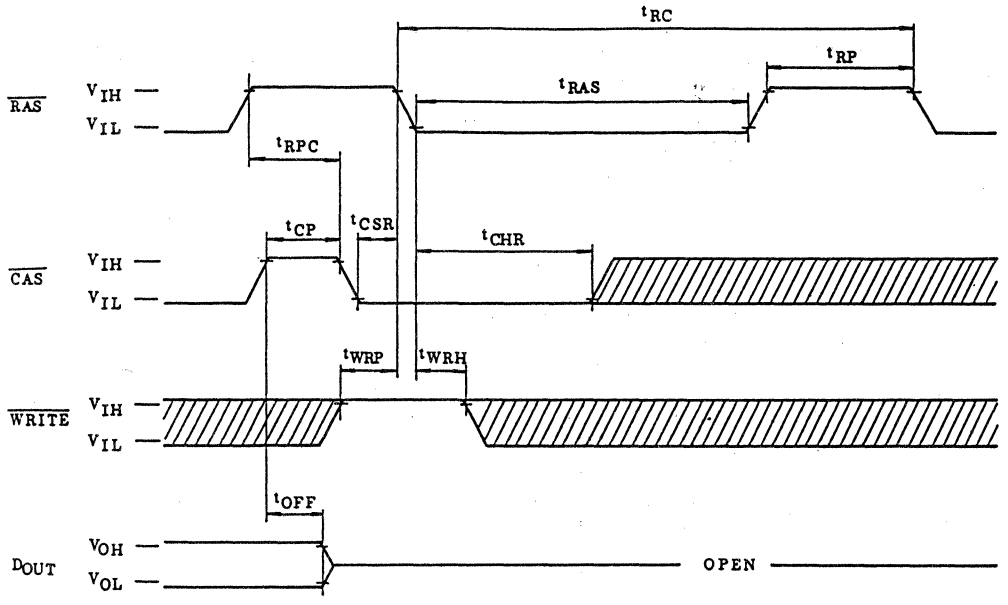
$\overline{RAS}$ ONLY REFRESH CYCLE



▨ : "H" or "L"

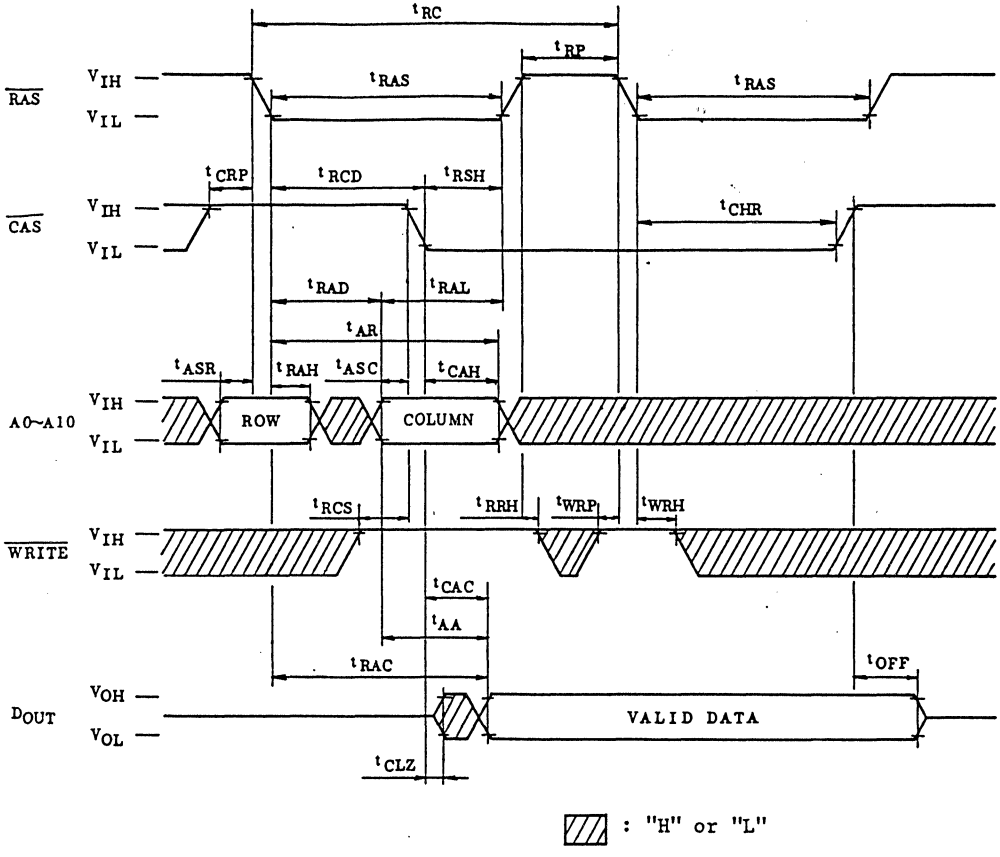
NOTE: $\overline{WRITE}$="H" or "L", A10="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

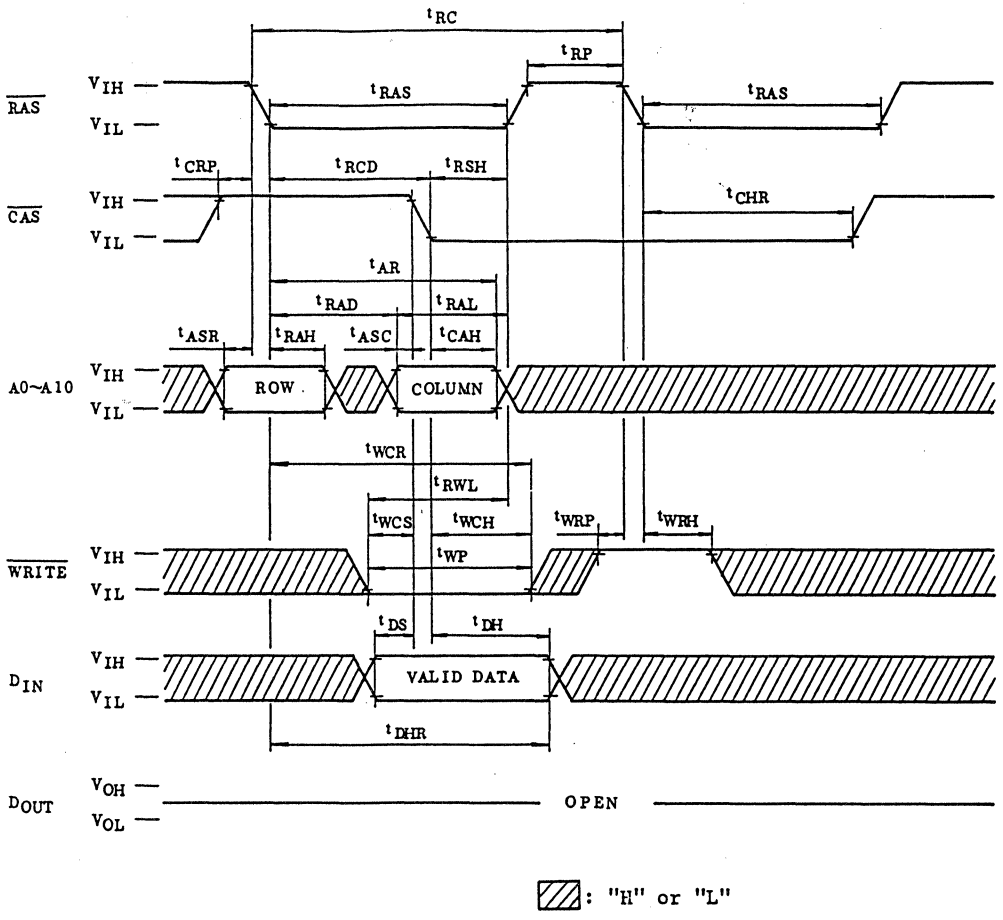


NOTE: A0 ∿ A10="H" or "L" ▨ : "H" or "L"

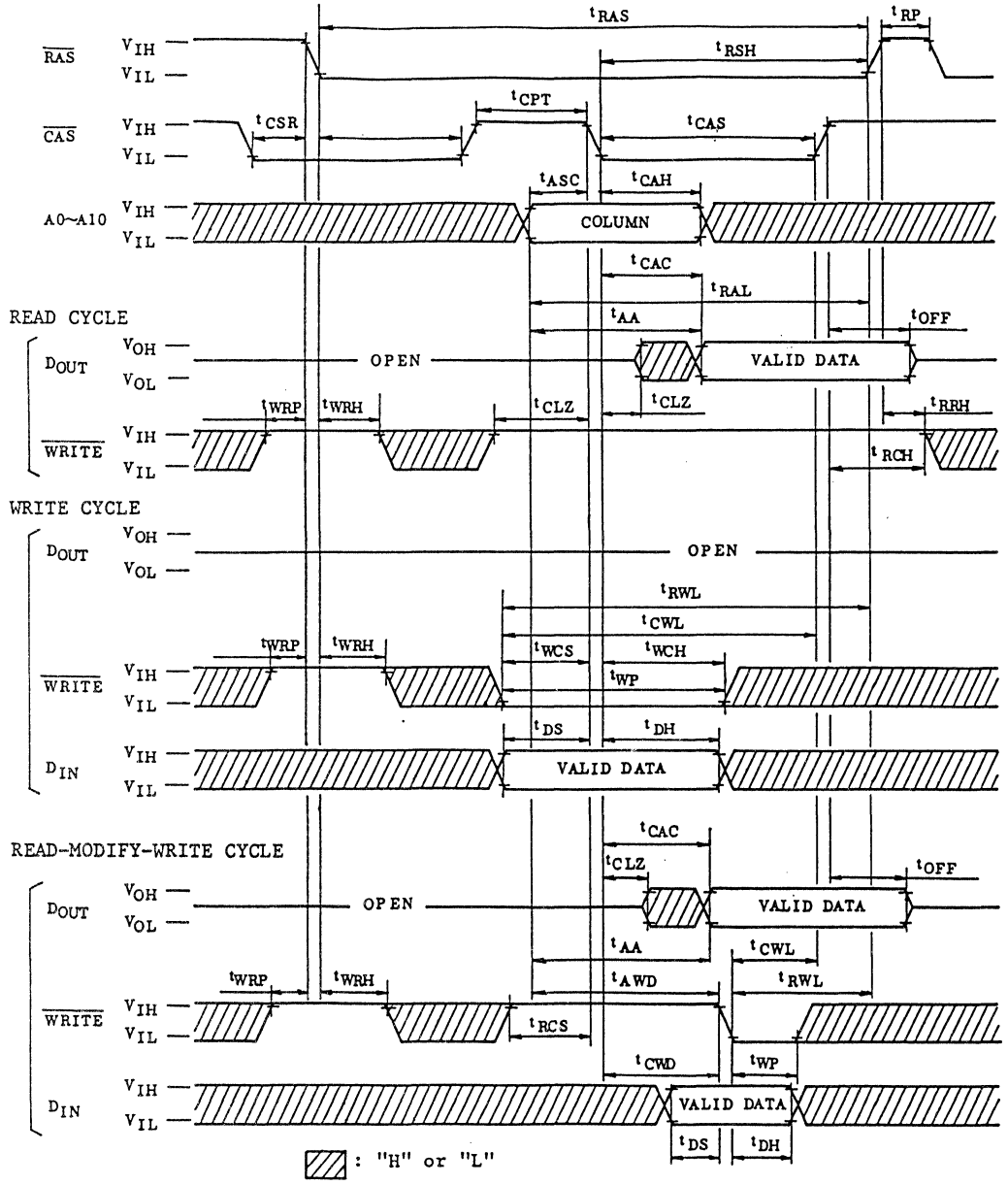
HIDDEN REFRESH CYCLE (READ)



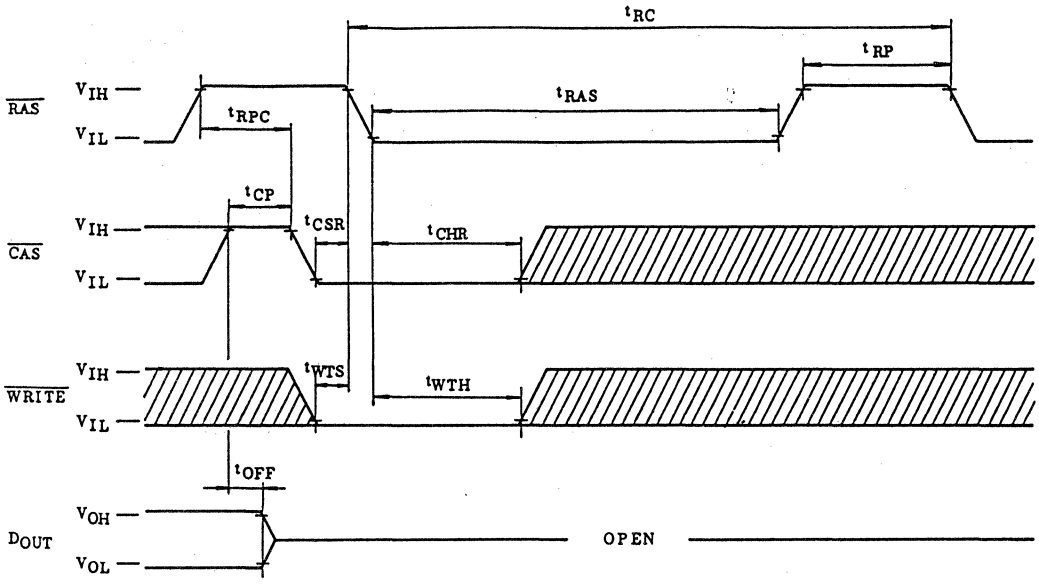
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

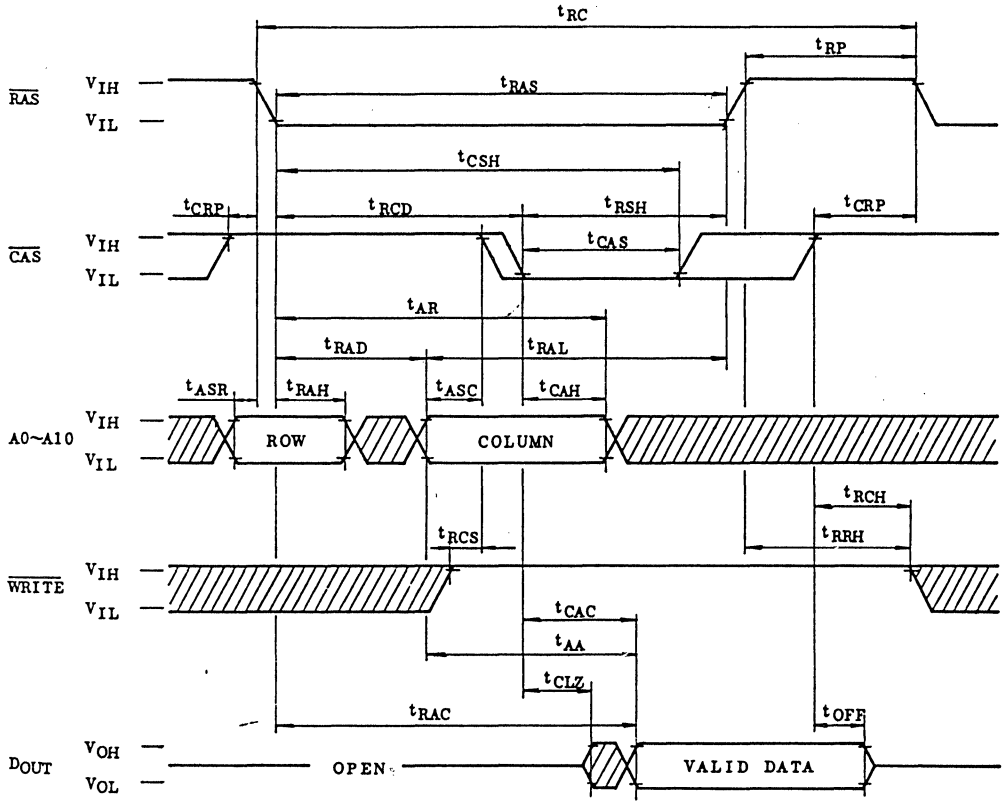


WRITE, CAS BEFORE RAS REFRESH CYCLE



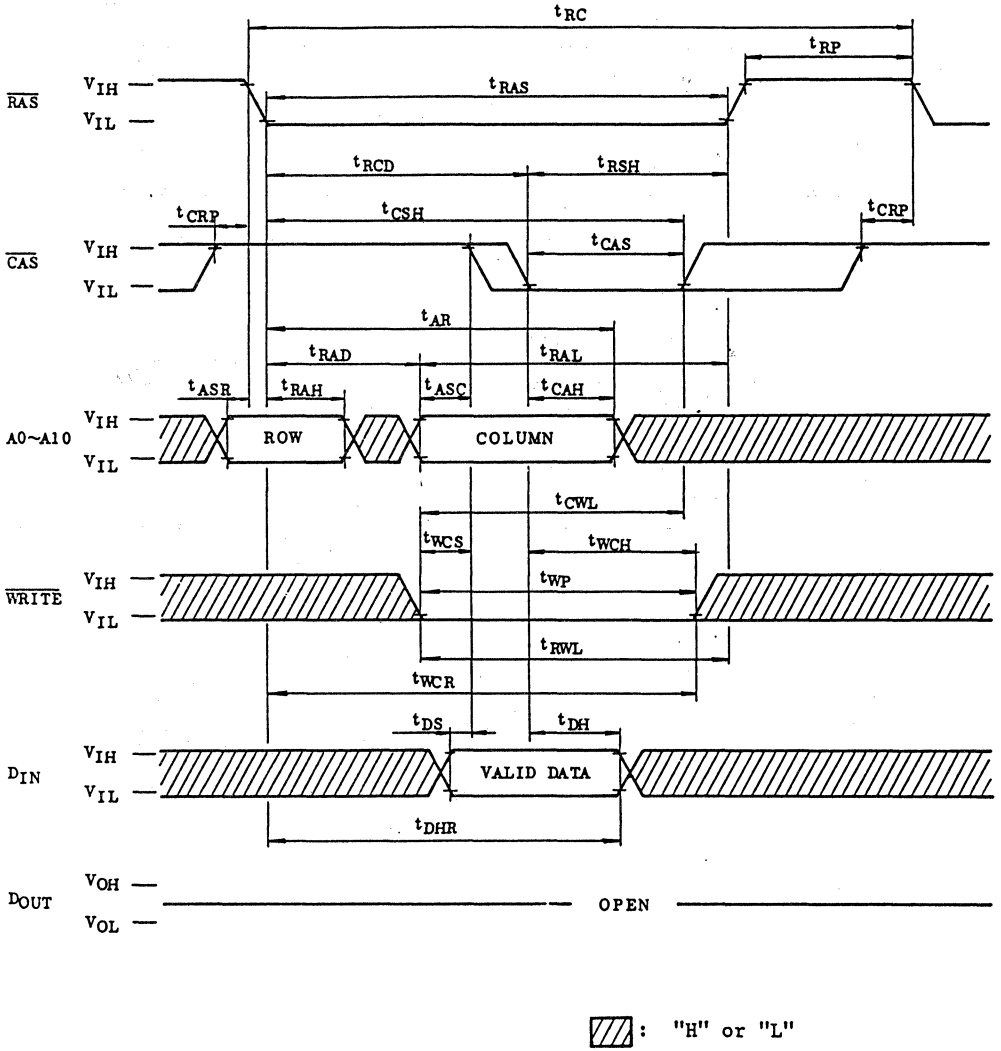
NOTE: D_{IN}, A0 ∿ A10: "H" or "L" ▨ : "H" or "L"

READ CYCLE IN THE TEST MODE



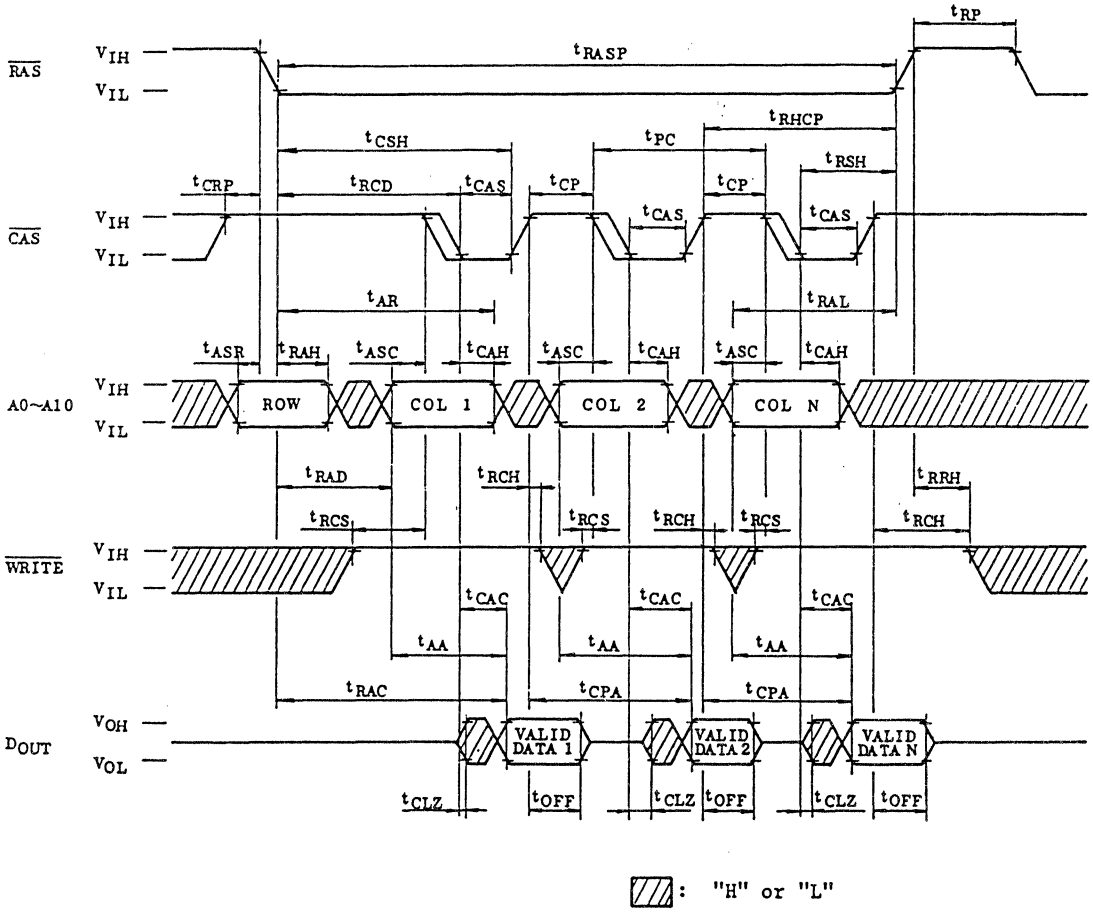
▨: "H" or "L"

WRITE CYCLE (EARLY WRITE) IN THE TEST MODE

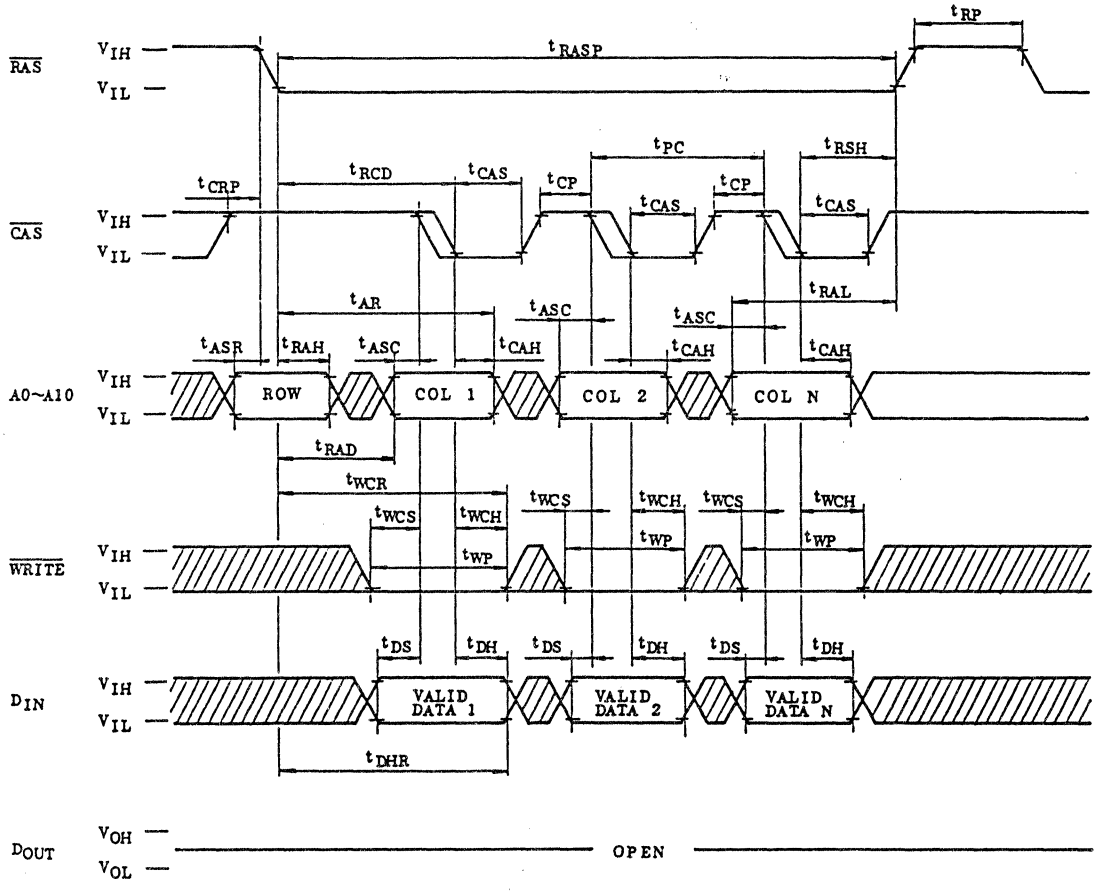


▨: "H" or "L"

FAST PAGE MODE READ CYCLE IN THE TEST MODE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN TEH TEST MODE



TEST MODE

The TC514100J/Z is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig. 1 shows the block diagram of TC514100J/Z. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

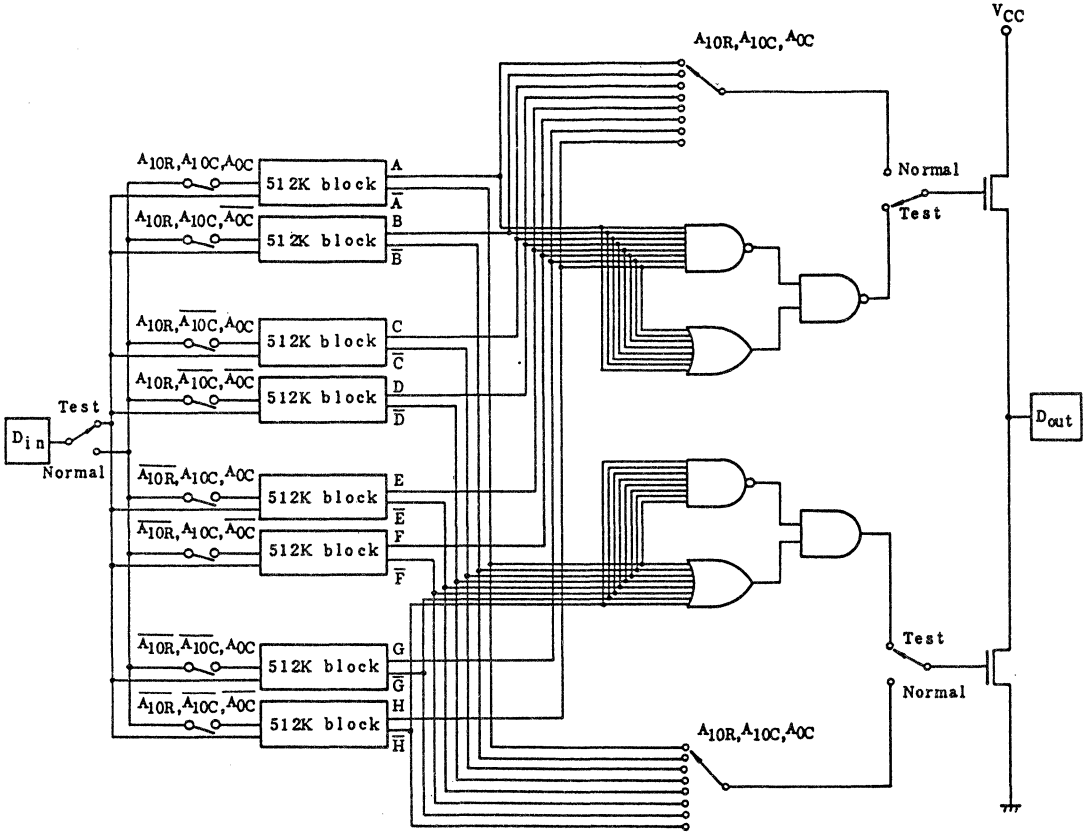


Fig. 1

4,194,304 WORD × 1 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514100AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514100AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514100AP/AJ/ASJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 1bit organization
- Fast access time and cycle time

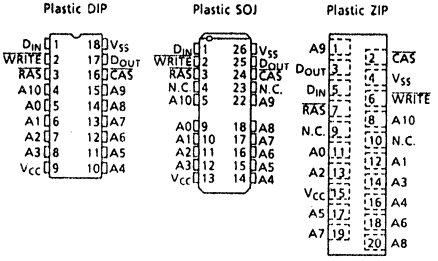
	TC514100AP/AJ/ASJ/AZ-60
t_{RAC} $\overline{RAS}$ Access Time	60ns
t_{AA} Column Address Access Time	30ns
t_{CAC} $\overline{CAS}$ Access Time	20ns
t_{RC} Cycle Time	110ns
t_{PC} Fast Page Mode Cycle Time	45ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  660mW MAX. Operating
  (TC514100AP/AJ/ASJ/AZ-60)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC514100AP : DIP18-P-300E
  TC514100AJ : SOJ26-P-350
  TC514100ASJ : SOJ26-P-300A
  TC514100AZ : ZIP20-P-400A

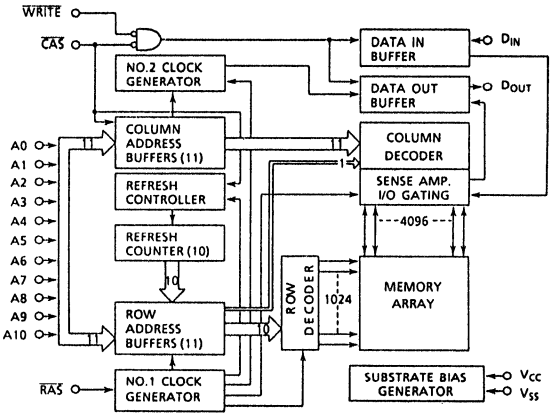
PIN NAMES

A0~A10	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	N.C.	No Connection
$\overline{CAS}$	Column Address Strobe		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514100AP/AJ/ ASJ/AZ-60	–	120	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC514100AP/AJ/ ASJ/AZ-60	–	120	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	TC514100AP/AJ/ ASJ/AZ-60	–	60	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514100AP/AJ/ ASJ/AZ-60	–	120	mA	3, 5
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514100AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	135	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	70	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	20	ns	9,14
t_{AA}	Access Time from Column Address	–	30	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to RAS	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	ns	

ELECTRICAL CHARACTGERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514100AP/AJ/ASJ/AZ-60		UNITS	NOTES
		MIN.	MAX.		
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	12
t_{DH}	Data Hold Time	15	–	ns	12
t_{REF}	Refresh Period	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	40	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	–		
t_{WTH}	Write Command Hold Time (Test Mode In)	10	–		
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–		
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–		

ELECTRICAL CHARACTGERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514100AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	115	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	65	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	45	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

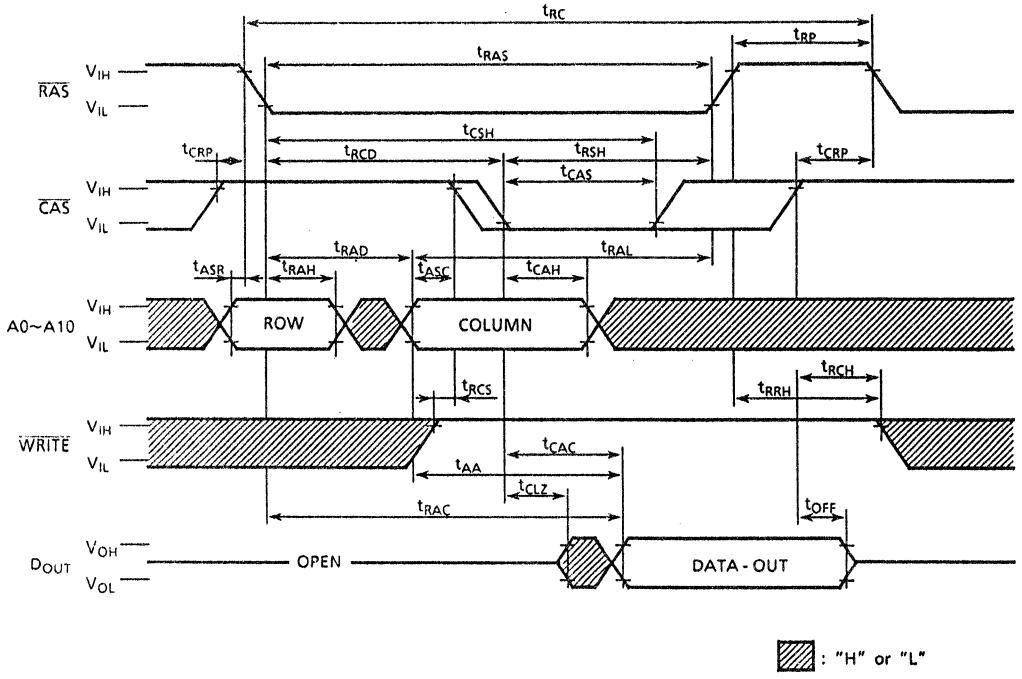
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

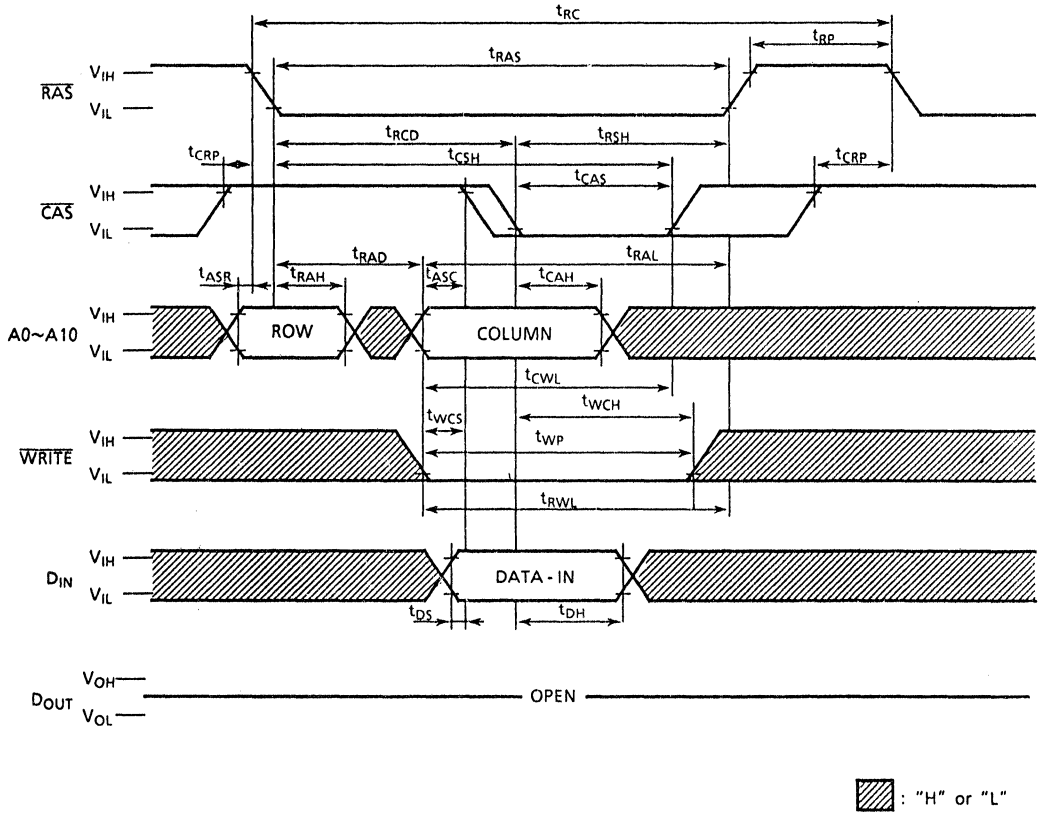
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

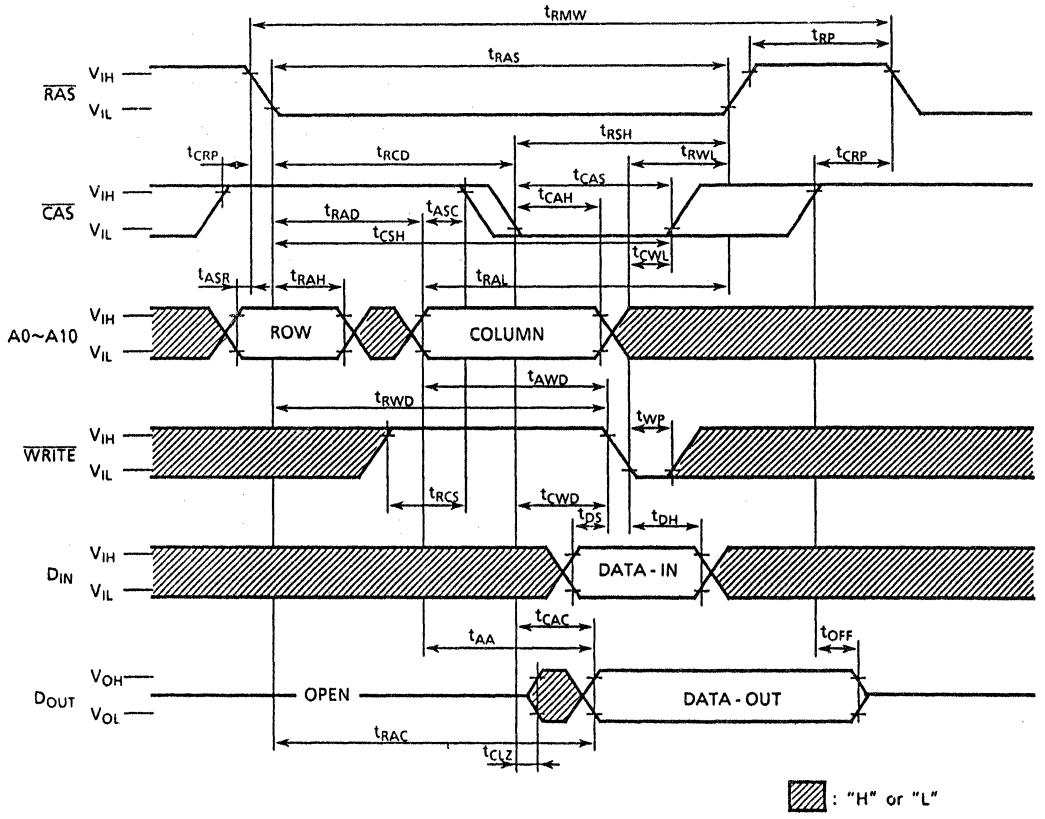
READ CYCLE



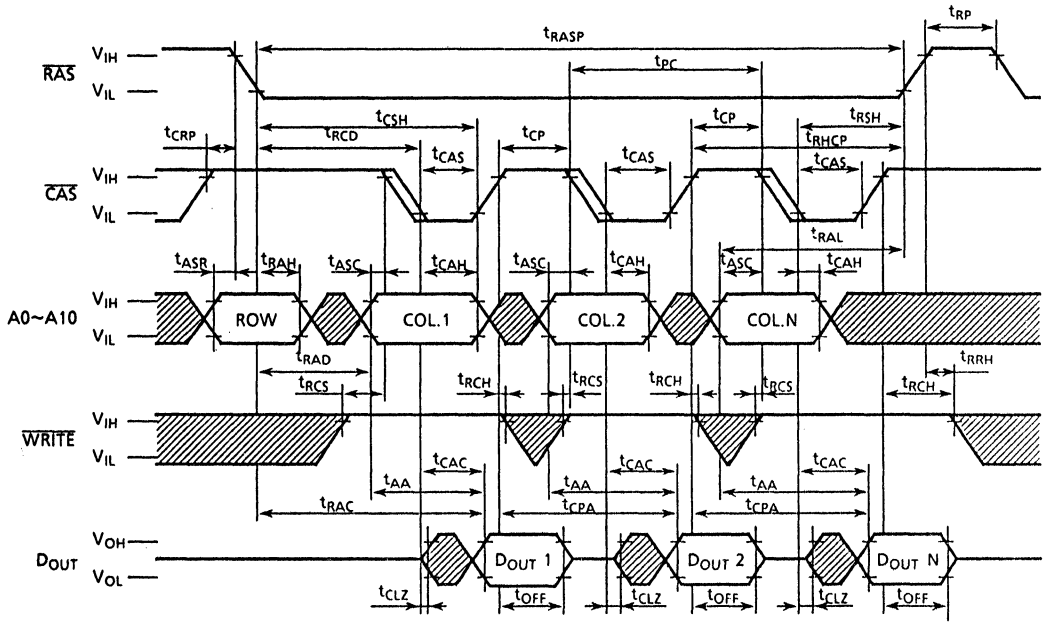
WRITE CYCLE (EARLY WRITE)



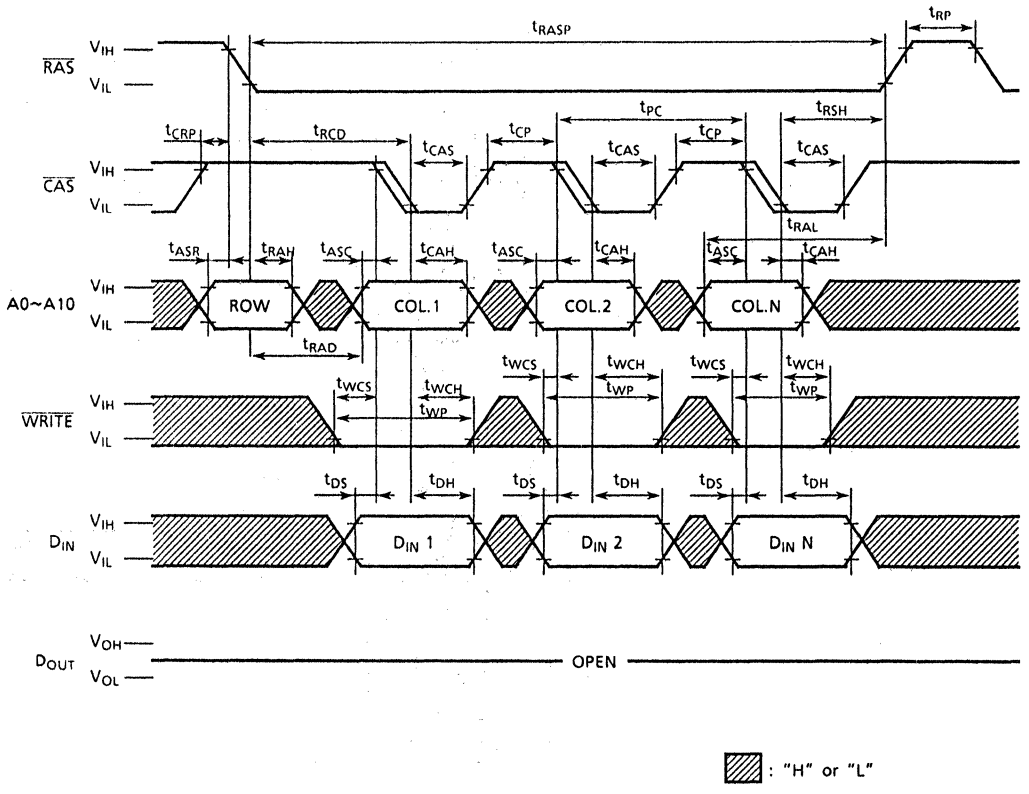
READ-MODIFY-WRITE CYCLE



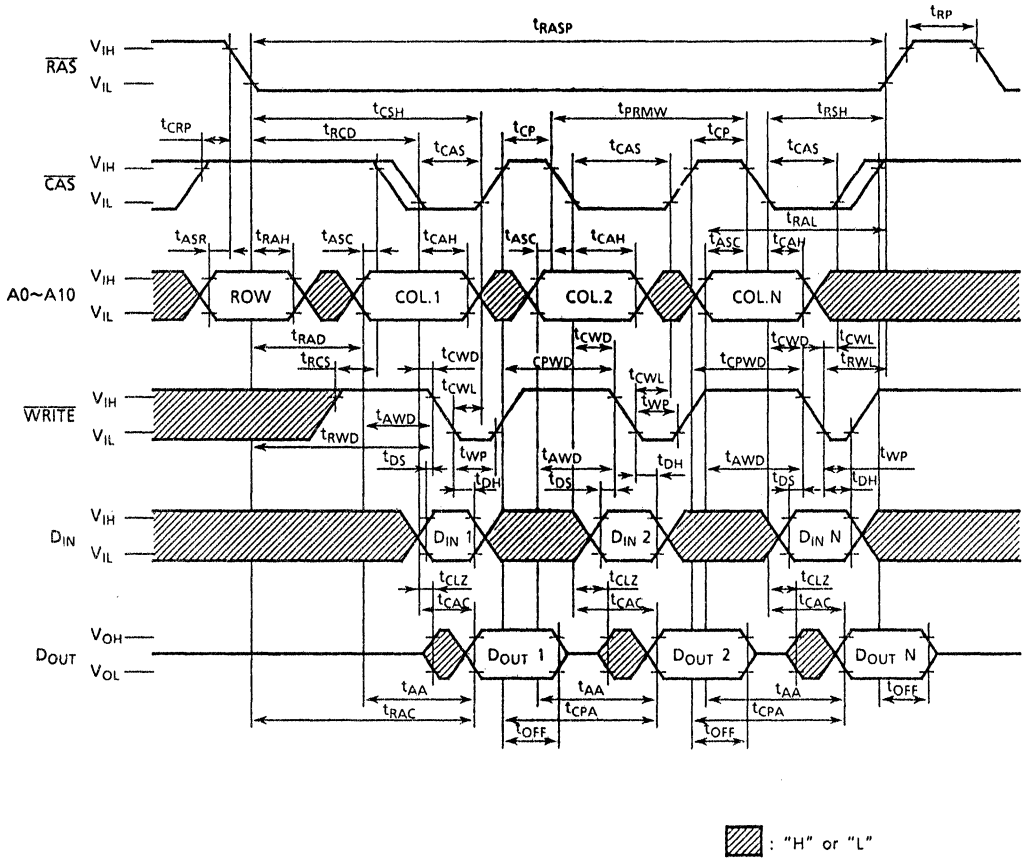
FAST PAGE MODE READ CYCLE



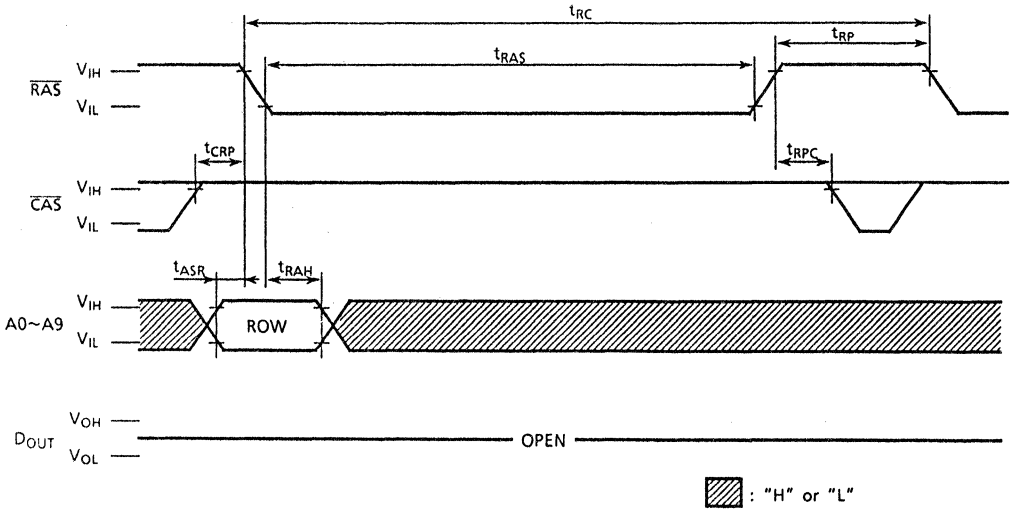
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

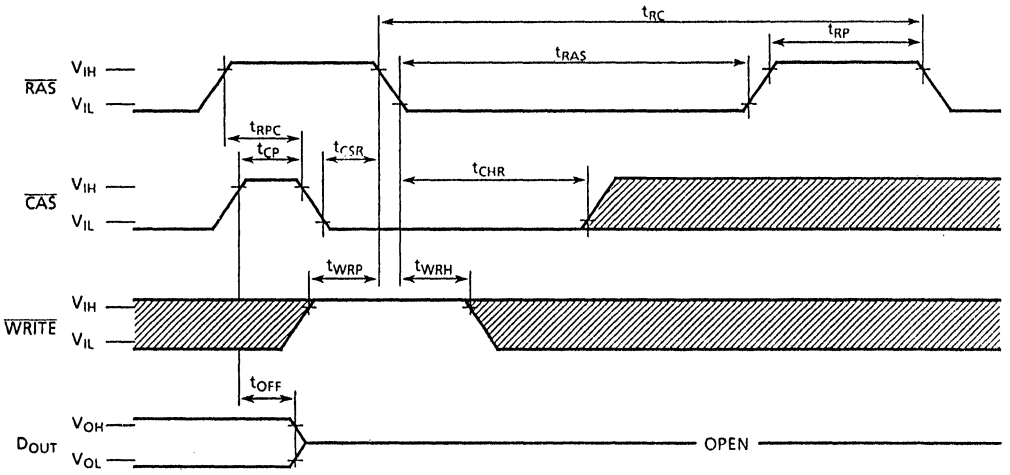


$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, A10 = "H" or "L"

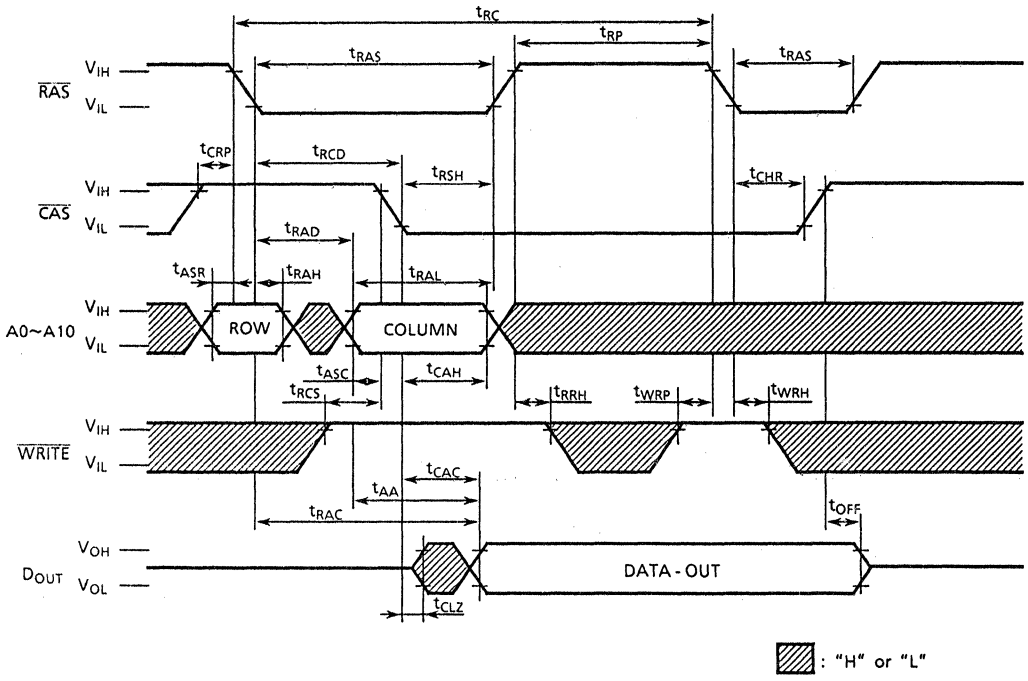
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



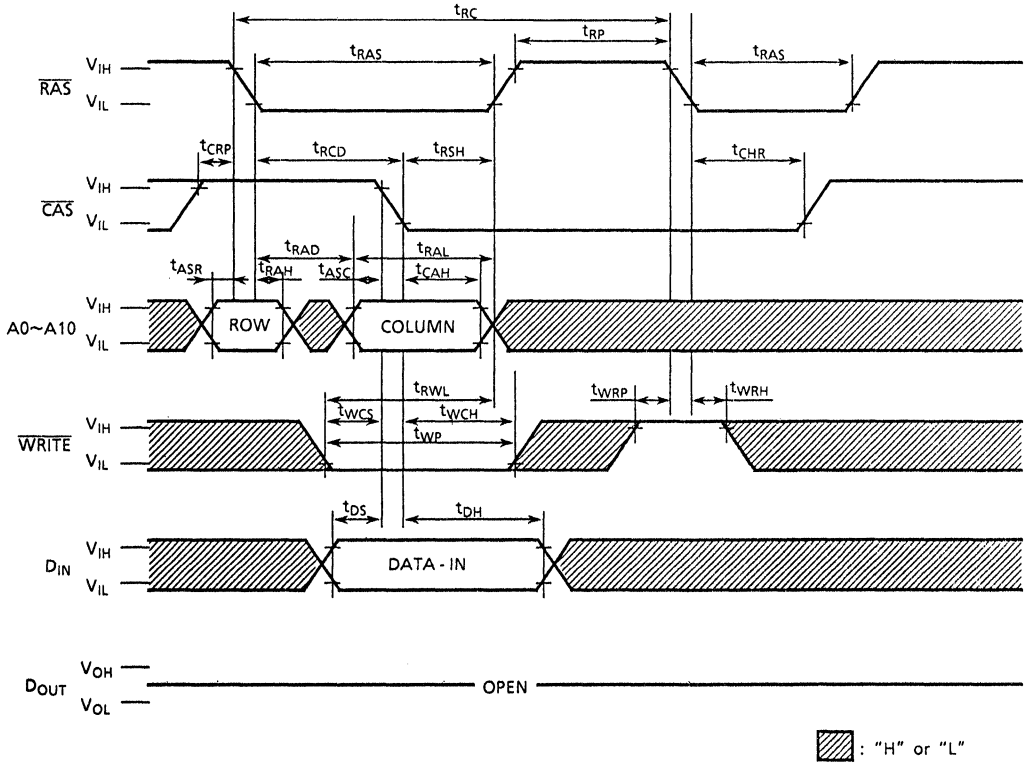
Note : A0~A10 = "H" or "L"

: "H" or "L"

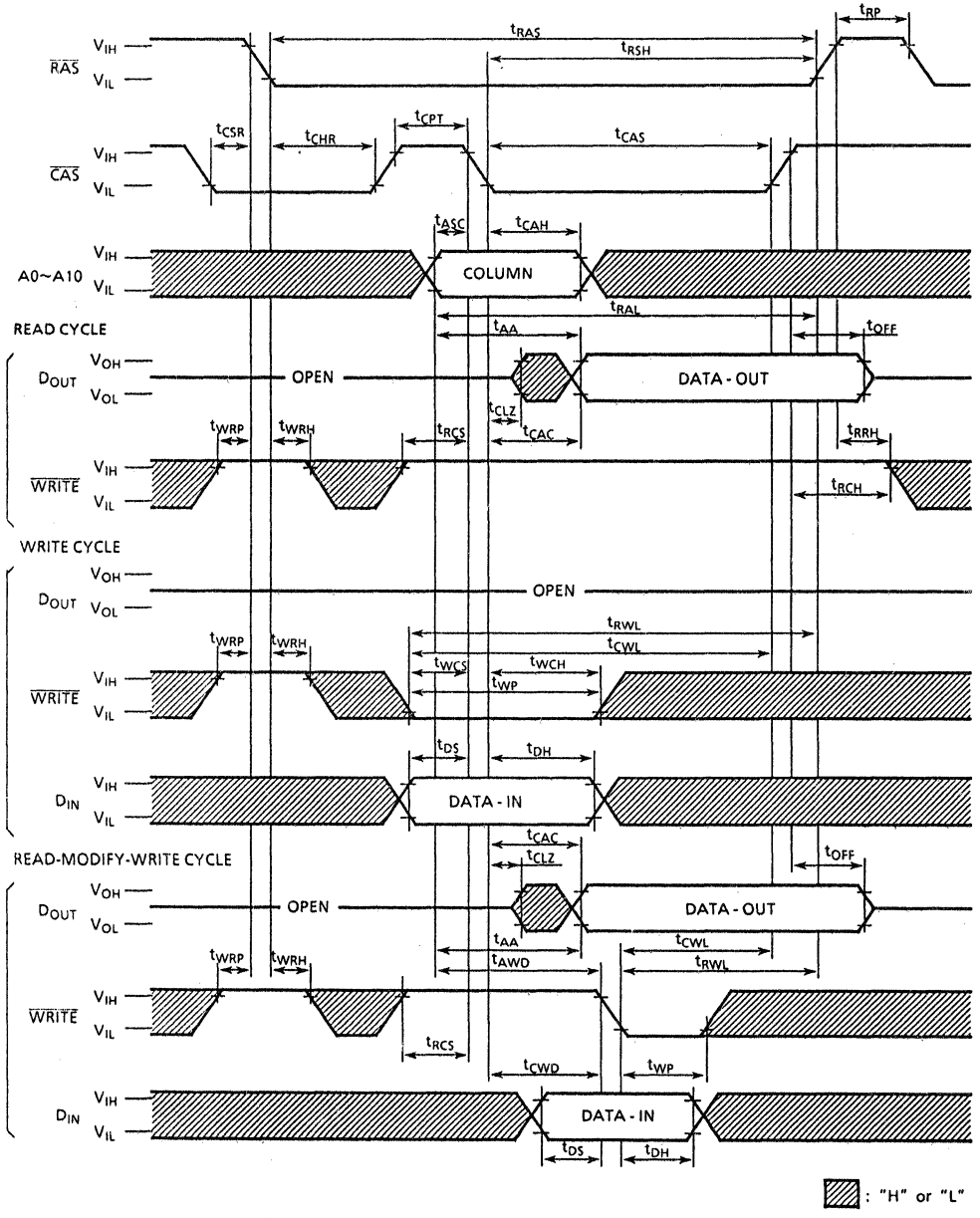
HIDDEN REFRESH CYCLE (READ)



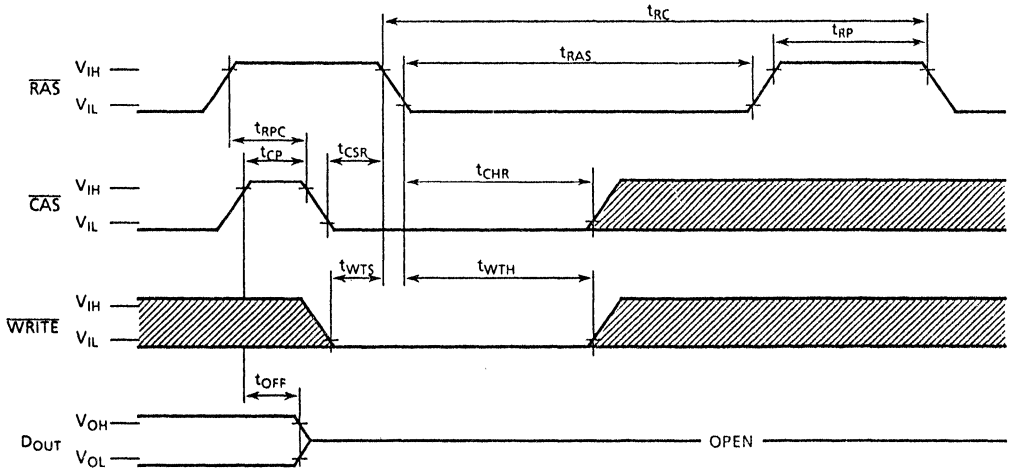
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, CAS BEFORE RAS REFRESH CYCLE



Note : D_{IN}, A0~A10 = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC514100AP/AJ/ASJ/AZ is the RAM organized 4,194,304 words by 1 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig.1 shows the block diagram of TC514100AP/AJ/ASJ/AZ. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

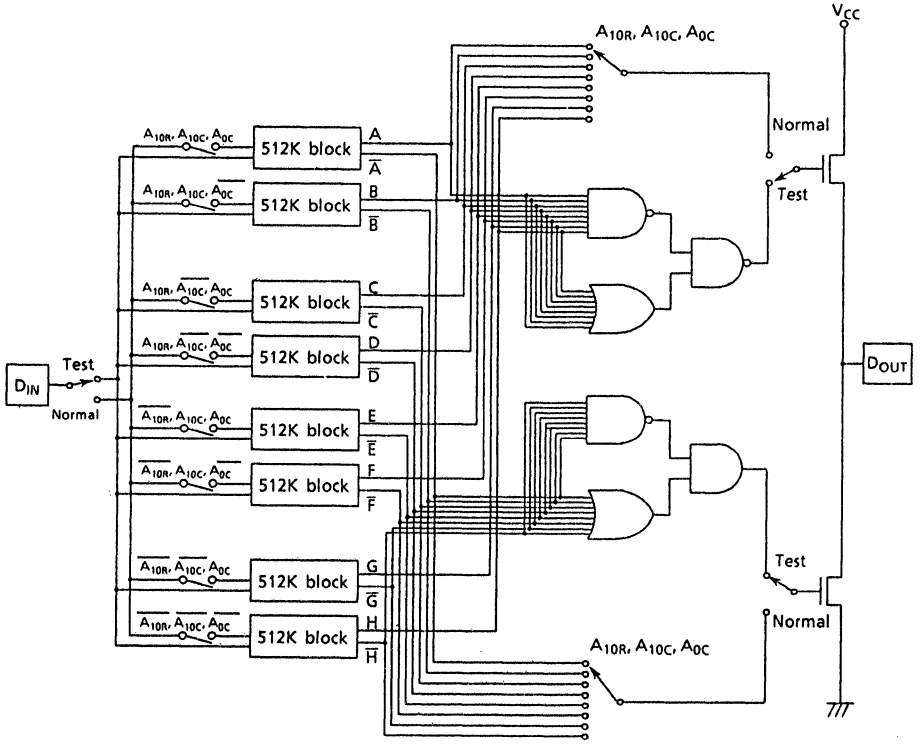


Fig. 1

NOTES

4,194,304 WORD × 1 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514100APL/AJL/ASJL/AZL is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514100APL/AJL/ASJL/AZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514100APL/AJL/ASJL/AZL to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 1bit organization
- Fast access time and cycle time

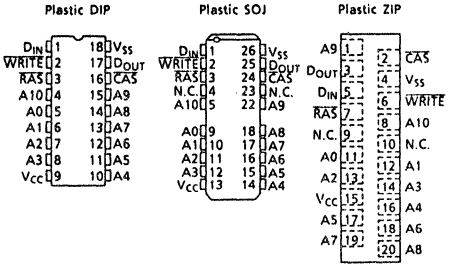
	TC514100APL/AJL/ASJL/AZL-60
t_{RAC} $\overline{RAS}$ Access Time	60ns
t_{AA} Column Address Access Time	30ns
t_{CAC} $\overline{CAS}$ Access Time	20ns
t_{RC} Cycle Time	110ns
t_{PC} Fast Page Mode Cycle Time	45ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  660mW MAX. Operating
  (TC514100APL/AJL/ASJL/AZL-60)
  1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514100APL : DIP18-P-300E
  TC514100AJL : SOJ26-P-350
  TC514100ASJL: SOJ26-P-300A
  TC514400AZL : ZIP20-P-400A

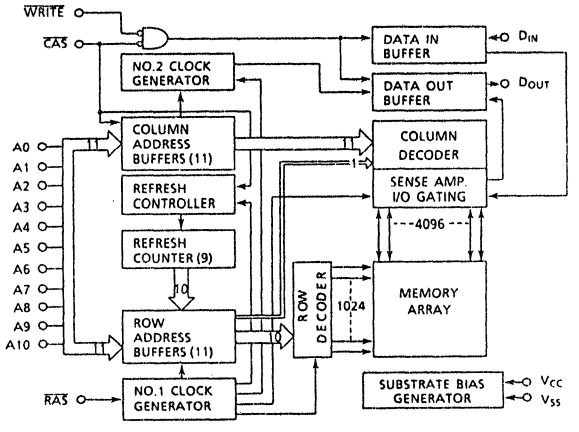
PIN NAMES

A0~A10	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	N.C.	No Connection
$\overline{CAS}$	Column Address Strobe		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514100APL/AJL/ASJL/AZL-60	–	120	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514100APL/AJL/ASJL/AZL-60	–	120	mA	3,5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514100APL/AJL/ASJL/AZL-60	–	60	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514100APL/AJL/ASJL/AZL-60	–	120	mA	3,5
I_{CC7}	Battery Back Up Current Average power Supply Current, Battery Back Up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V A0~10 = V_{CC} – 0.2V or 0.2V, D_{IN} = V_{CC} – 0.2V, 0.2V or OPEN: t_{RC} = 125µs, t_{RAS} = 300ns ~ 1µs)		–	400	µA	3,6
I_{CC7}	Battery Back Up Current Average power Supply Current, Battery Back Up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V A0~10 = V_{CC} – 0.2V or 0.2V, D_{IN} = V_{CC} – 0.2V, 0.2V or OPEN: t_{RC} = 125µs, t_{RAS} = t_{RAS} MIN. ~300ns)		–	300	µA	3,6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514100APL/AJL/ASJL/AZL-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	135	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	70	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	10, 15 16
t_{CAC}	Access Time from $\overline{CAS}$	–	20	ns	10, 15
t_{AA}	Access Time from Column Address	–	30	ns	10, 16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	ns	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	12
t_{WCH}	Write Command Hold Time	10	–	ns	

ELECTRICAL CHARACTGERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514100APL/AJL/ASJL/AZL-60		UNITS	NOTES
		MIN.	MAX.		
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	13
t_{DH}	Data Hold Time	15	–	ns	13
t_{REF}	Refresh Perio	–	128	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	–	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	40	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	–	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	ns	

ELECTRICAL CHARACTGERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514100APL/AJL/ASJL/AZL-60		UNITS	NOTES
		MIN.	MAX.		
t_{RC}	Random Read Write Cycle Time	115	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	65	ns	10, 15 16
t_{CAC}	Access Time from $\overline{CAS}$	–	25	ns	10, 15
t_{AA}	Access Time from Column Address	–	35	ns	10, 16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	ns	10
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	–	ns	
t_{RHCP}	$\overline{CAS}$ Prechrge to $\overline{RAS}$ Hold Time	45	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

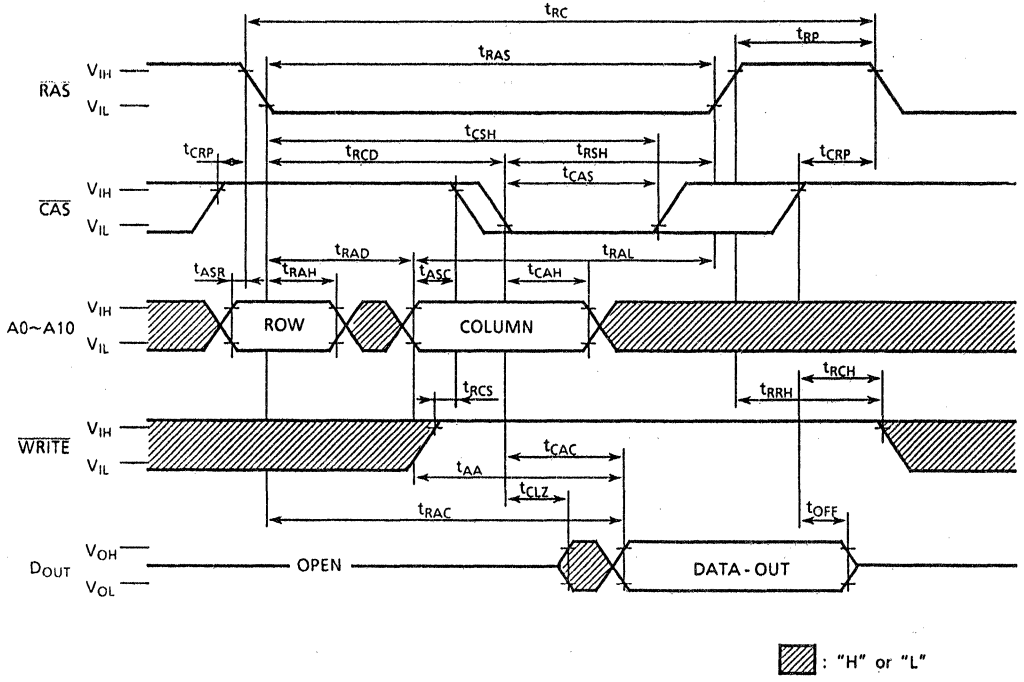
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

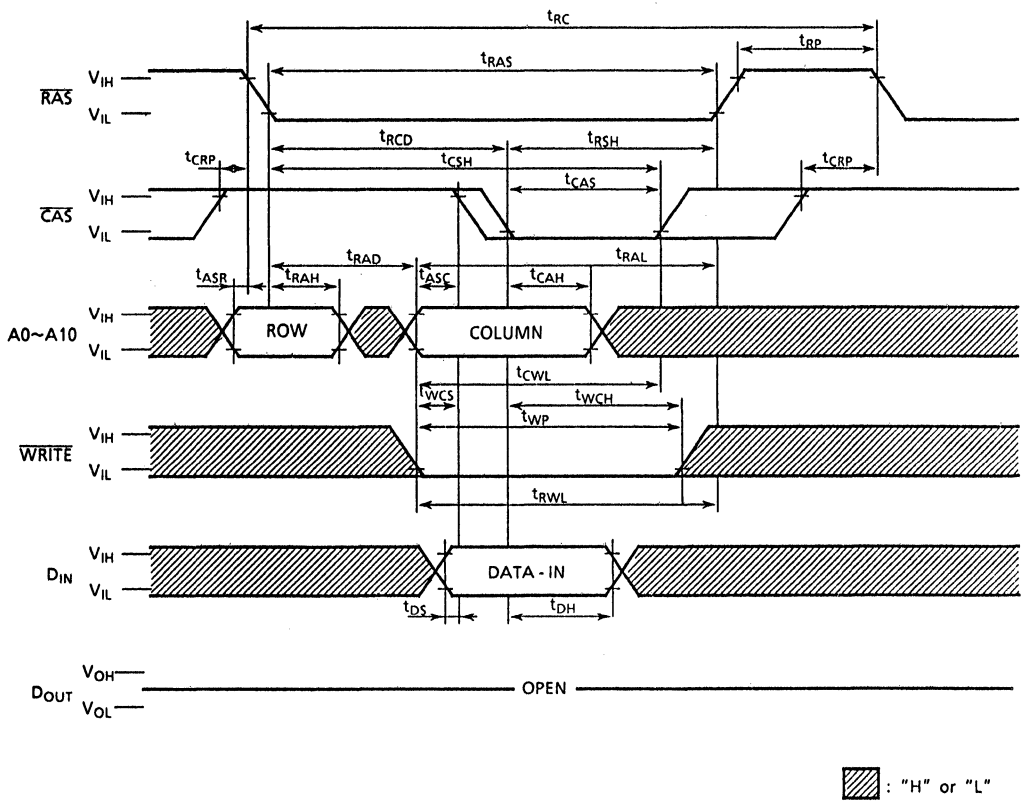
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. t_{RAS} (max.) = 1μs is only applied to refresh of battery-back up. t_{RAS} (max.) = 10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume t_T = 5ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

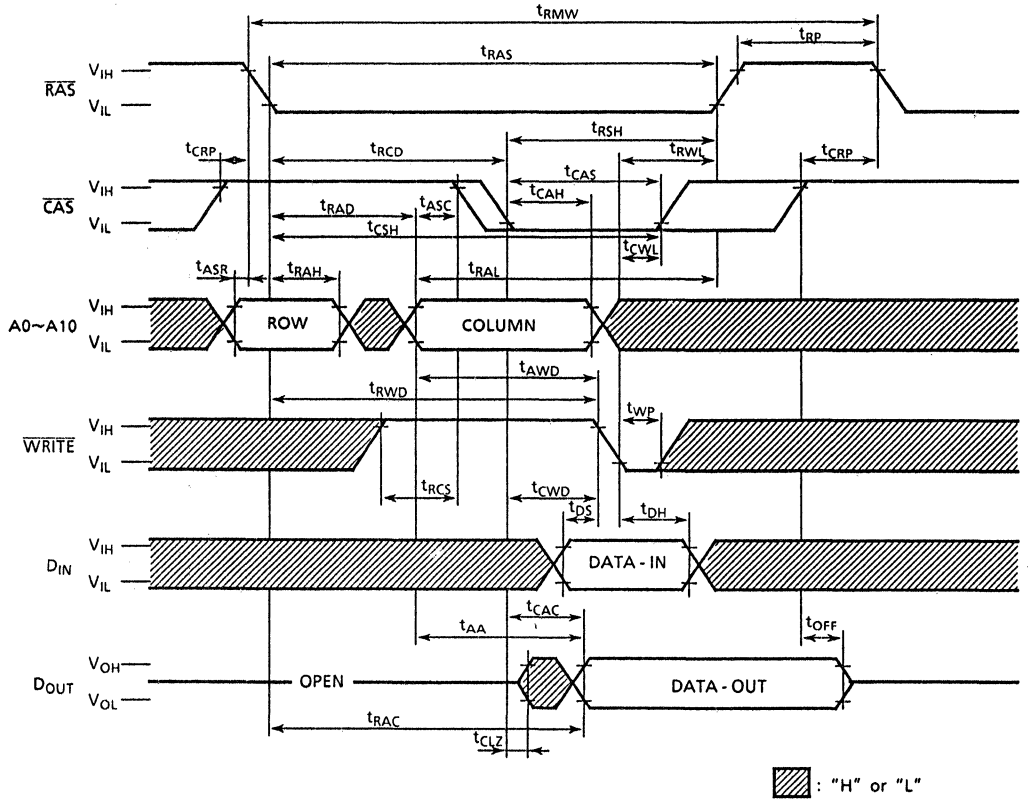
READ CYCLE



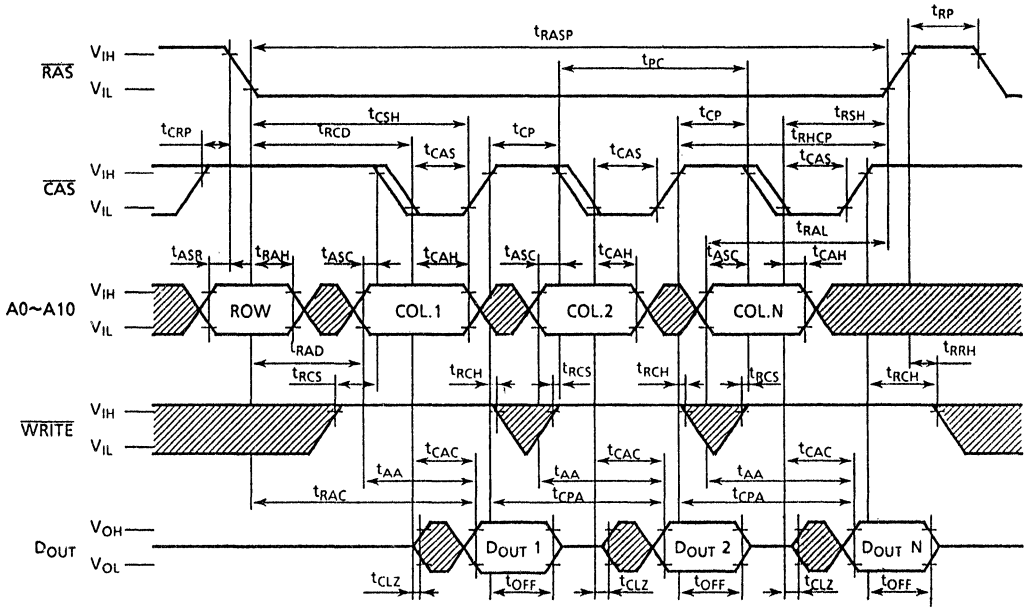
WRITE CYCLE (EARLY WRITE)



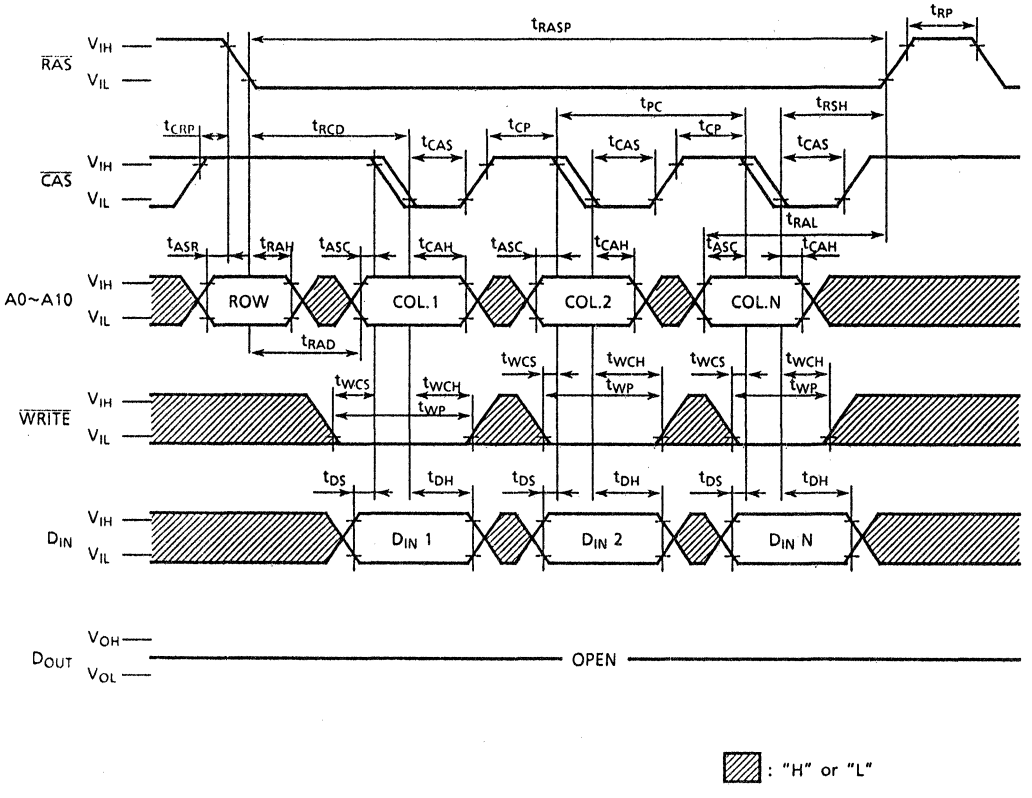
READ-MODIFY-WRITE CYCLE



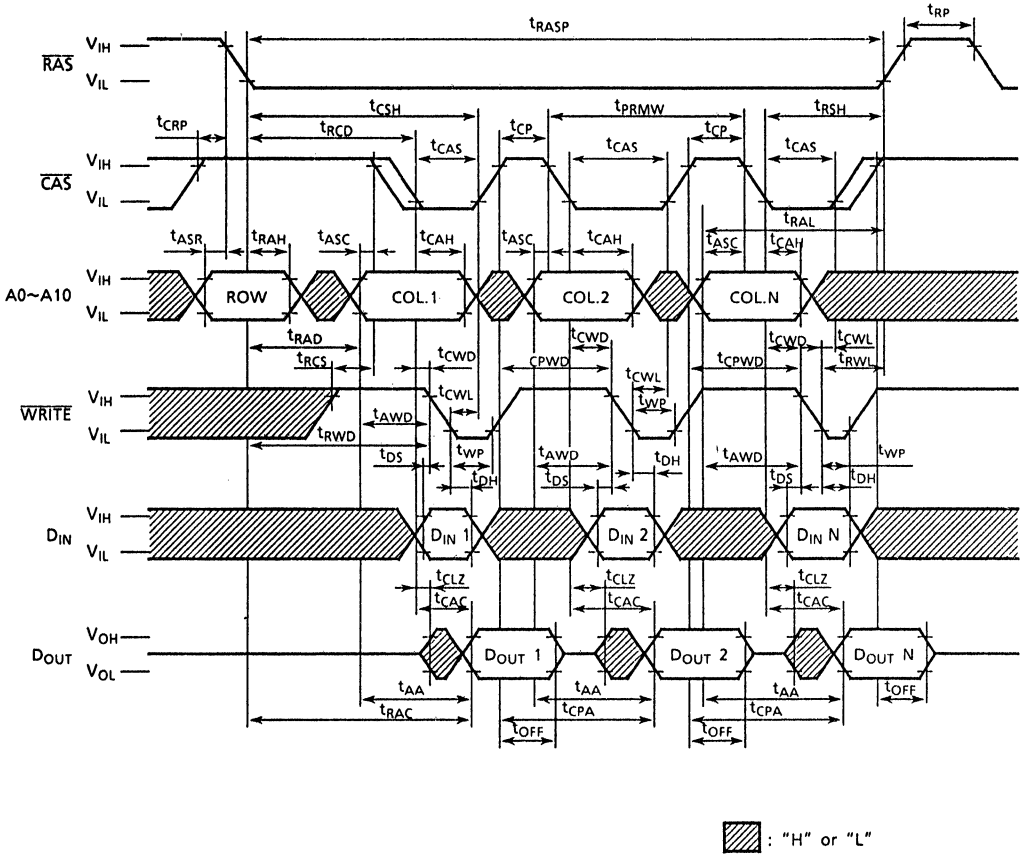
FAST PAGE MODE READ CYCLE



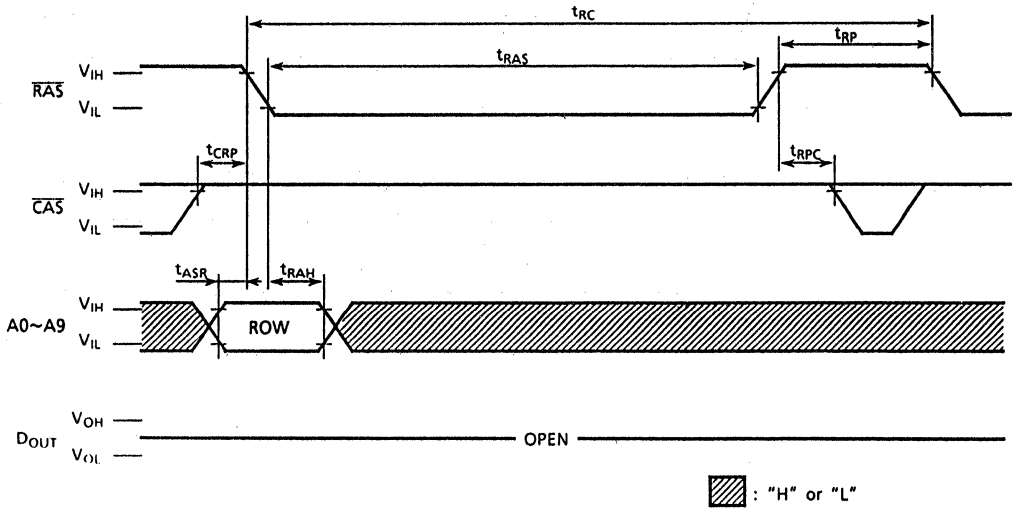
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

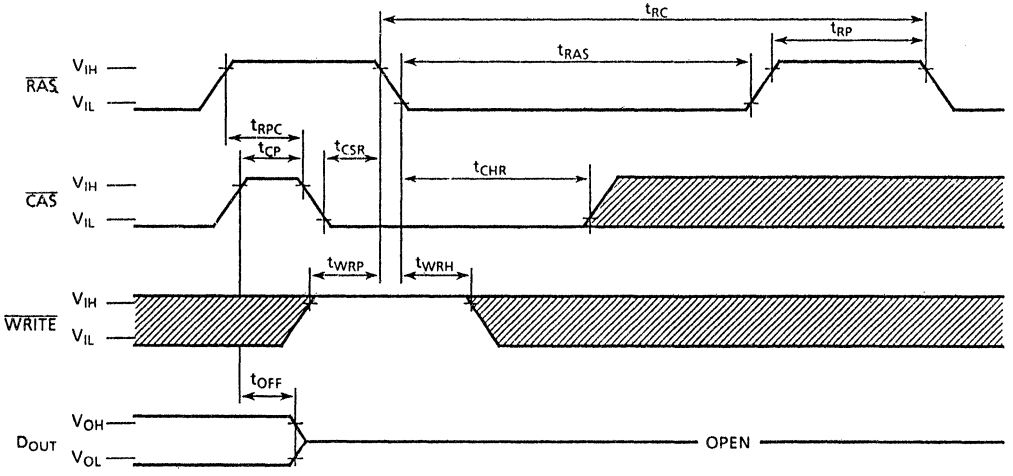


$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



Note: $\overline{\text{WRITE}}$, A10 = "H" or "L"

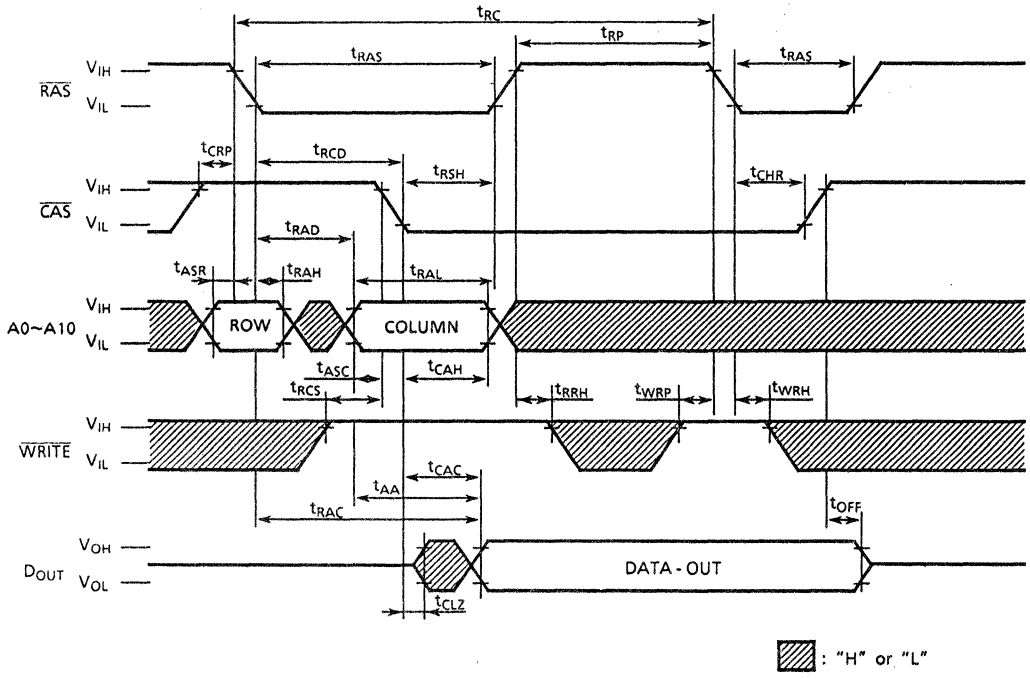
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



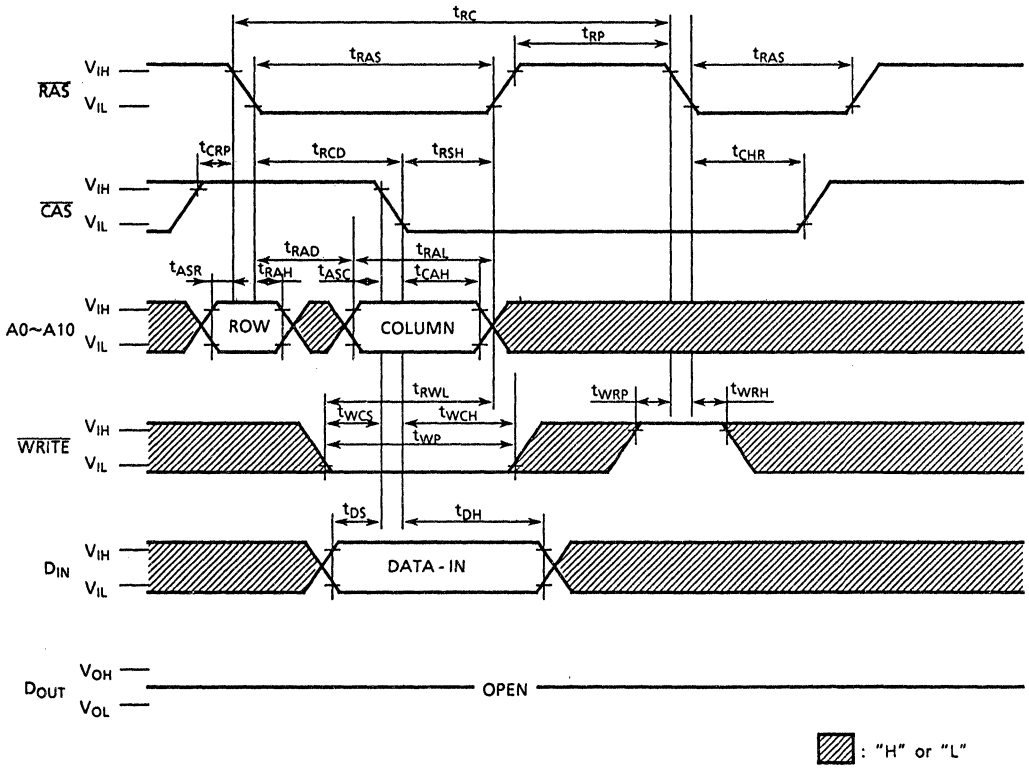
Note: A0~A10 = "H" or "L"

: "H" or "L"

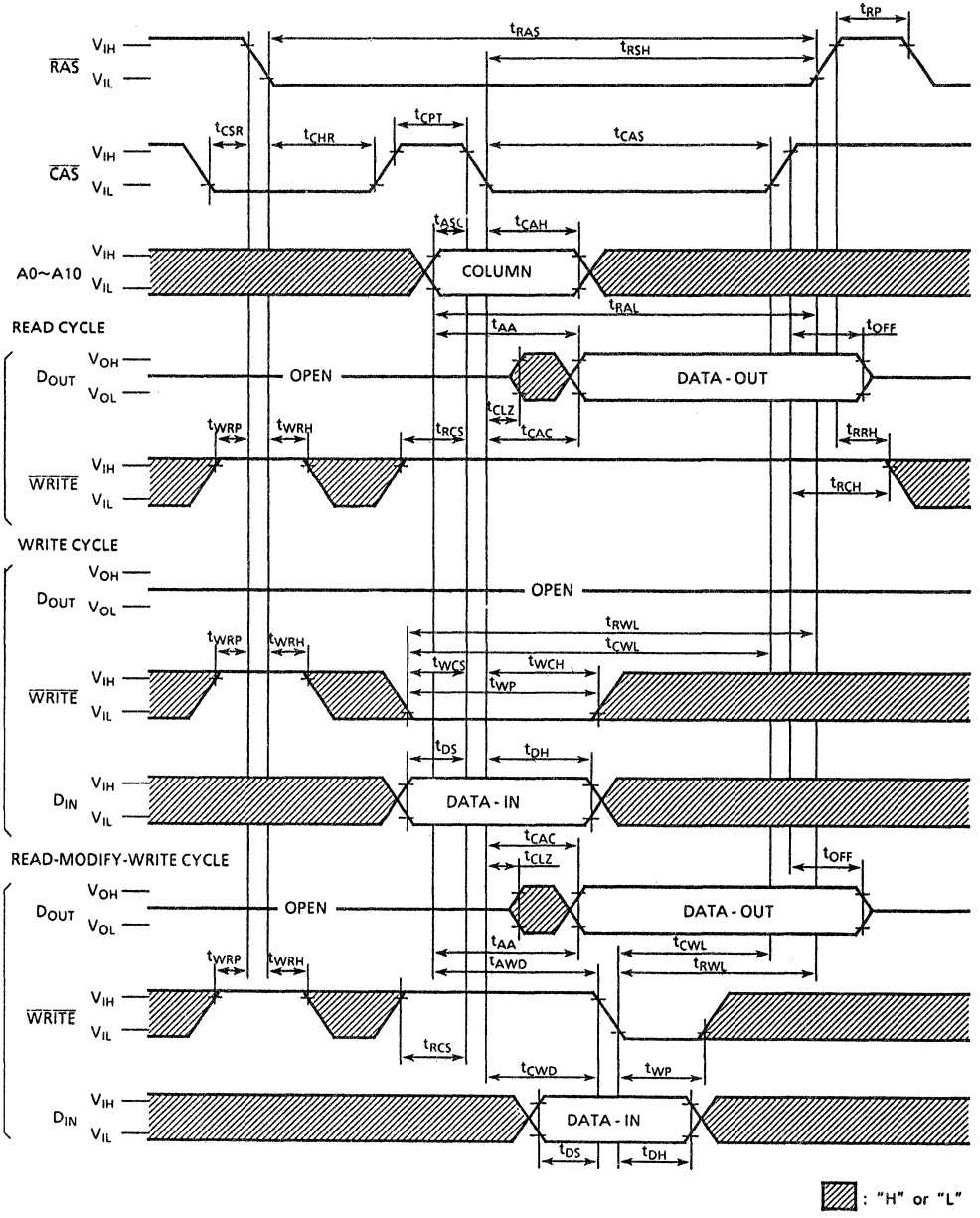
HIDDEN REFRESH CYCLE (READ)



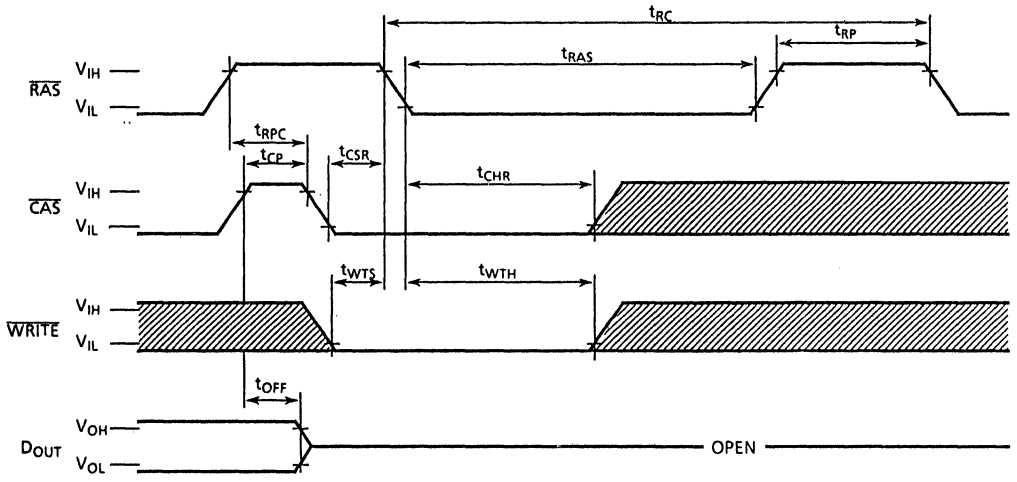
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, CAS BEFORE RAS REFRESH CYCLE



Note: D_{IN}, A0~A10 = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC514100APL/AJL/ASJL/AZL is the RAM organized 4,194,304 words by 1 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, and A_{0C} are not used. If, upon reading, all bits equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig.1 shows the block diagram of TC514100APL/AJL/ASJL/AZL. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

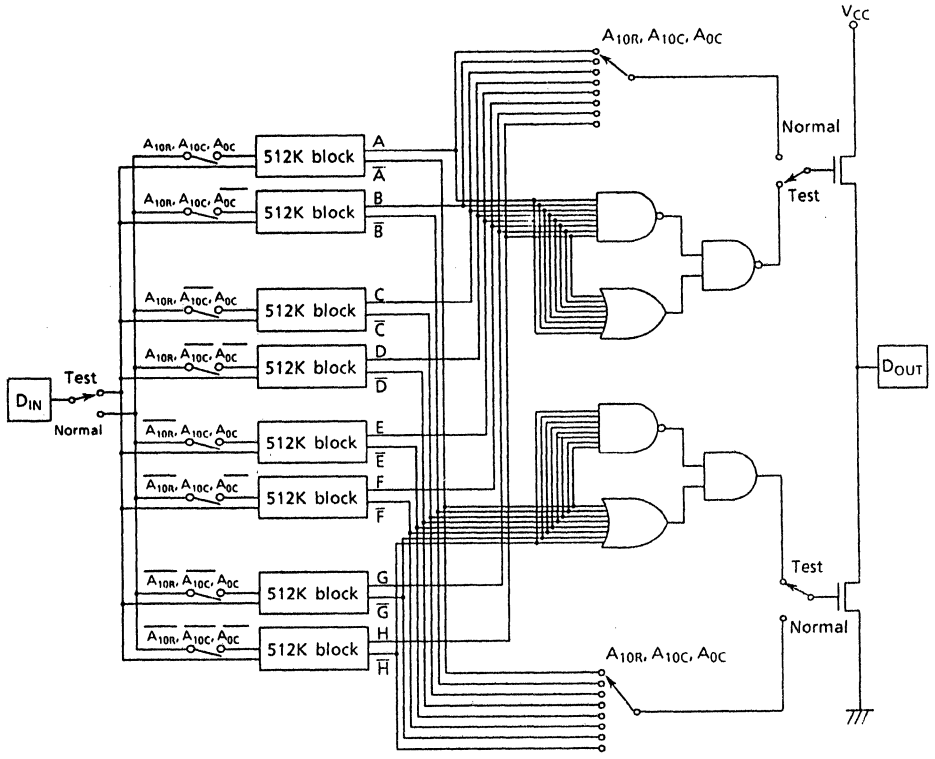


Fig. 1

NOTES

4,194,304 WORD × 1 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514100AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514100AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514100AP/AJ/ASJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 1bit organization
- Fast access time and cycle time

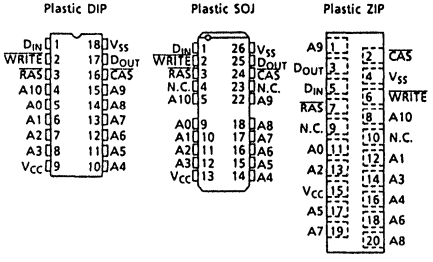
	TC514100AP/AJ/ASJ/AZ - 70/80/10		
t_{RAC} $\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA} Column Address Access Time	35ns	40ns	50ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC} Cycle Time	130ns	150ns	180ns
t_{PC} Fast Page Mode Cycle Time	45ns	50ns	60ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 550mW MAX. Operating (TC514100AP/AJ/ASJ/AZ-70)
  - 468mW MAX. Operating (TC514100AP/AJ/ASJ/AZ-80)
  - 413mW MAX. Operating (TC514100AP/AJ/ASJ/AZ-10)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC514100AP : DIP18-P-300E
  TC514100AJ : SOJ26-P-350
  TC514100ASJ : SOJ26-P-300A
  TC514100AZ : ZIP20-P-400A

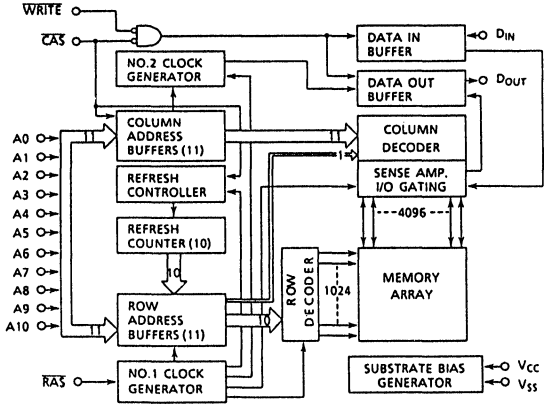
PIN NAMES

A0~A10	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	N.C.	No Connection
$\overline{CAS}$	Column Address Strobe		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514100AP/AJ/ASJ/AZ-70	–	100	mA	3, 4 5
		TC514100AP/AJ/ASJ/AZ-80	–	85		
		TC514100AP/AJ/ASJ/AZ-10	–	75		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514100AP/AJ/ASJ/AZ-70	–	100	mA	3,5
		TC514100AP/AJ/ASJ/AZ-80	–	85		
		TC514100AP/AJ/ASJ/AZ-10	–	75		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514100AP/AJ/ASJ/AZ-70	–	60	mA	3, 4 5
		TC514100AP/AJ/ASJ/AZ-80	–	50		
		TC514100AP/AJ/ASJ/AZ-10	–	45		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514100AP/AJ/ASJ/AZ-70	–	100	mA	3,5
		TC514100AP/AJ/ASJ/AZ-80	–	85		
		TC514100AP/AJ/ASJ/AZ-10	–	75		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514100AP/AJ/ASJ/AZ-70		TC514100AP/AJ/ASJ/AZ-80		TC514100AP/AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	–	175	–	210	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	70	–	75	–	90	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	9, 14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	9, 14
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	200,000	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	

ELECTRICAL CHARACTGERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514100AP/ AJ/ASJ/AZ-70		TC514100AP/ AJ/ASJ/AZ-80		TC514100AP/ AJ/ASJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	12
t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	20	–	25	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	70	–	80	–	100	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	–	40	–	50	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	40	–	45	–	55	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	–	10	–	10	–	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	–	10	–	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTGERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514100AP/ AJ/ASJ/AZ-70		TC514100AP/ AJ/ASJ/AZ-80		TC514100AP/ AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read Write Cycle Time	135	–	155	–	185	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	160	–	180	–	215	–		
t_{PC}	Fast Page Mode Cycle Time	50	–	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	75	–	80	–	95	–	ns	13
t_{RAC}	Access Time from $\overline{RAS}$	–	75	–	85	–	105	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	9, 14
t_{AA}	Access Time from Column Address	–	40	–	45	–	55	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	50	–	60	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	75	200,000	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	75	–	85	–	105	–	ns	
t_{RHCP}	$\overline{CAS}$ Prechrge to $\overline{RAS}$ Hold Time	45	–	50	–	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	45	–	55	–	ns	
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	25	–	25	–	30	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	75	–	85	–	105	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	40	–	45	–	55	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	45	–	50	–	60	–	ns	13

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

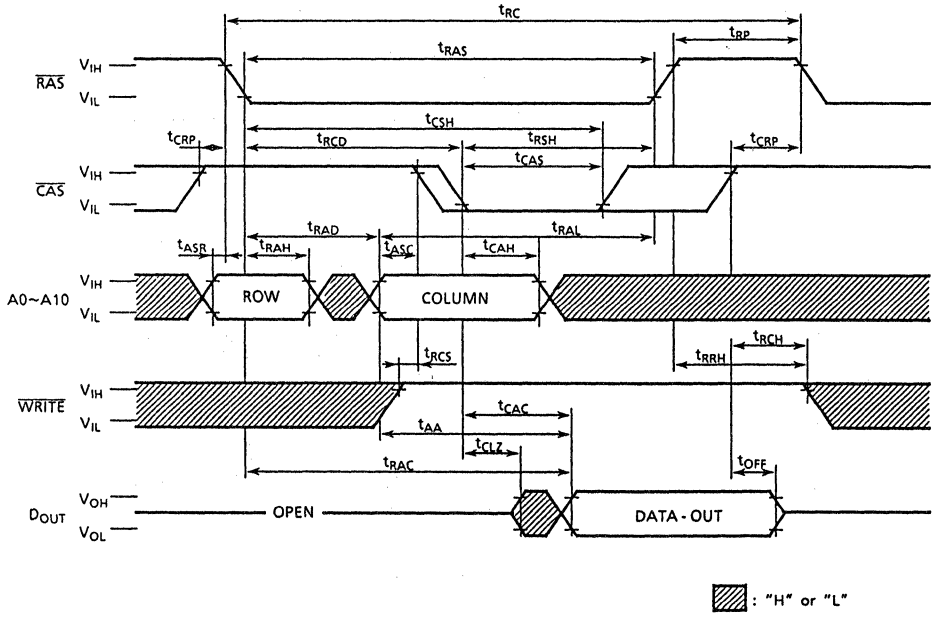
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

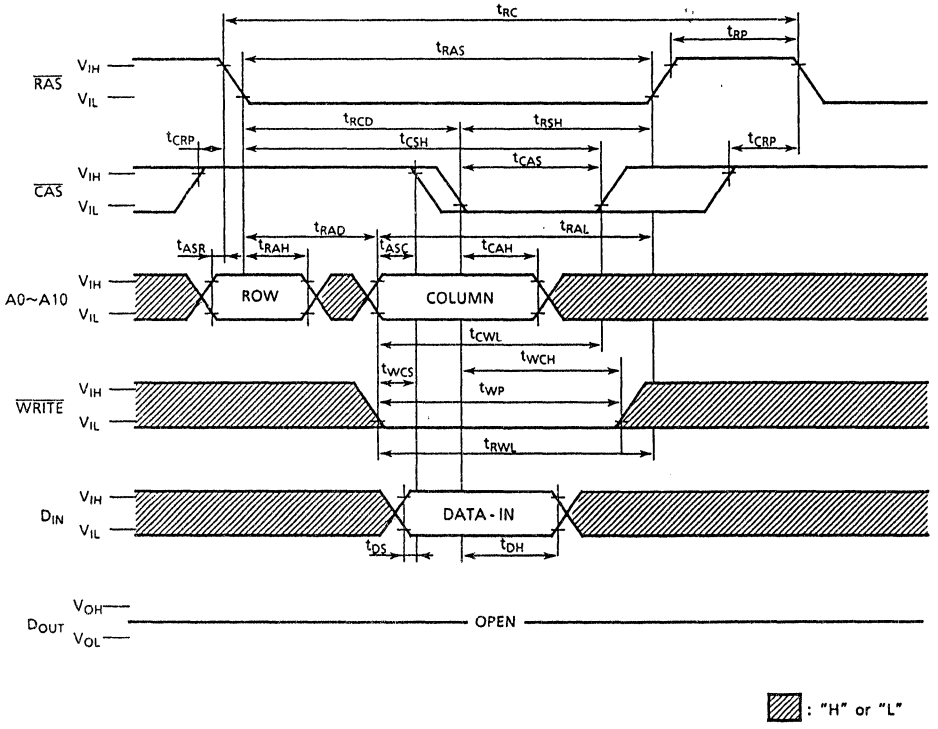
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

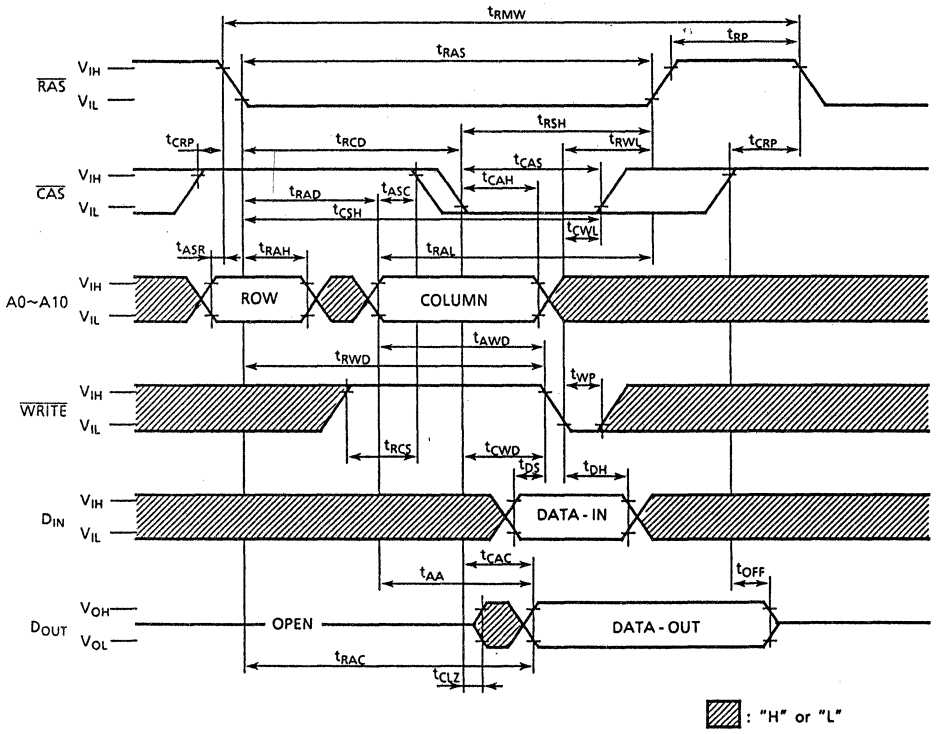
READ CYCLE



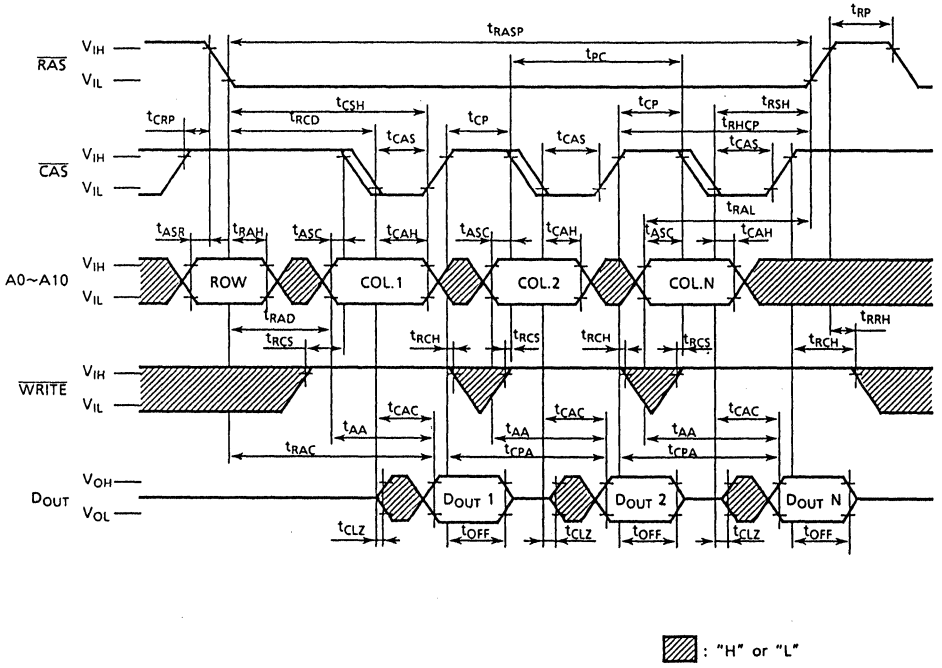
WRITE CYCLE (EARLY WRITE)



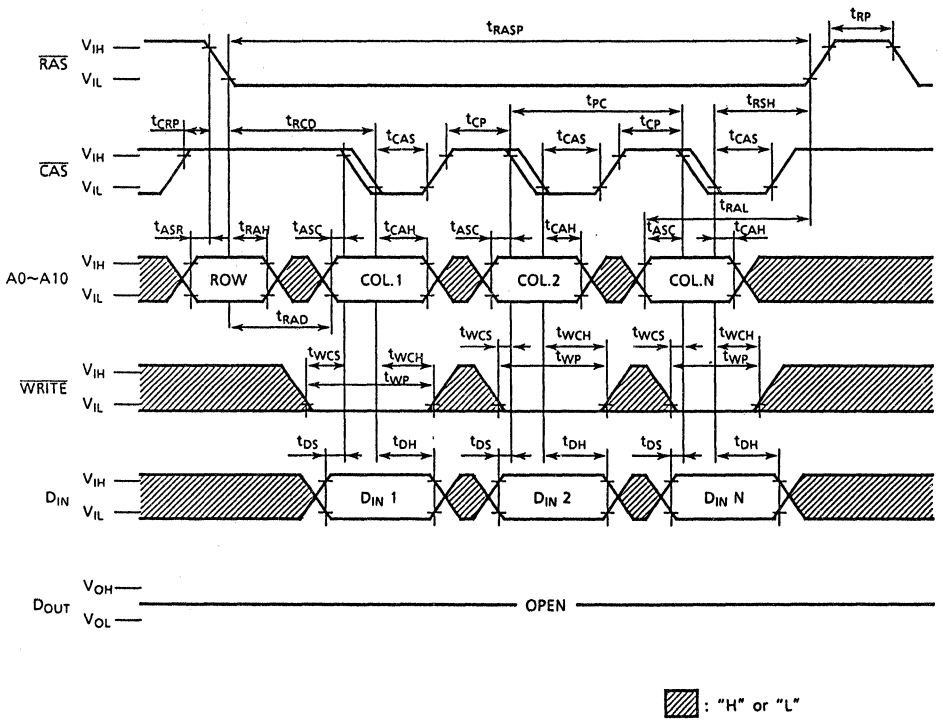
READ-MODIFY-WRITE CYCLE



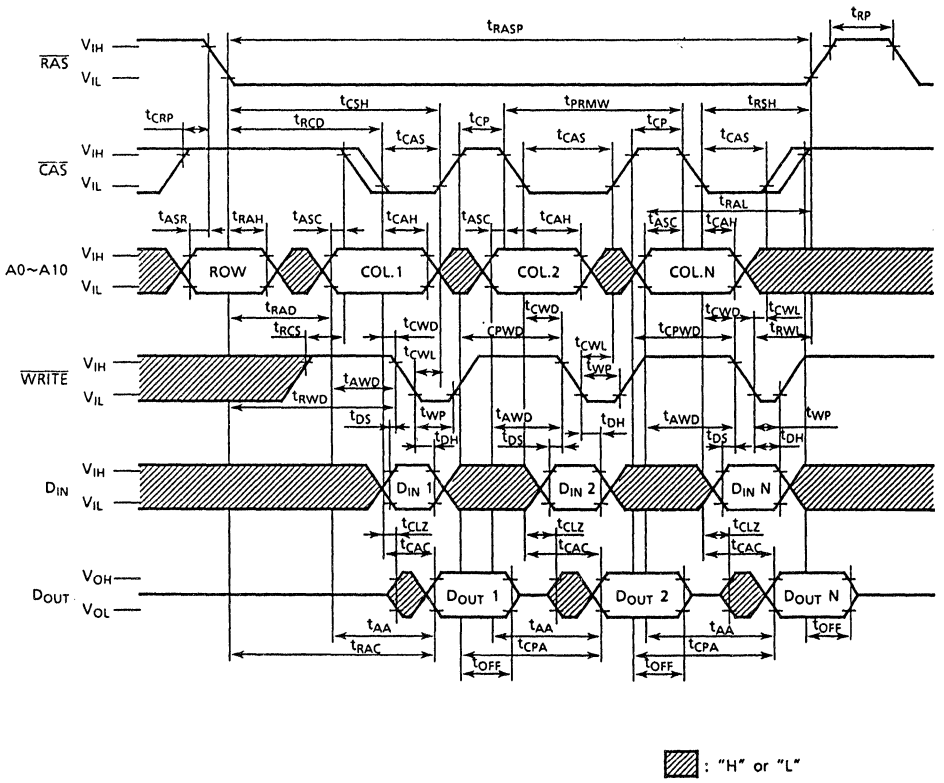
FAST PAGE MODE READ CYCLE



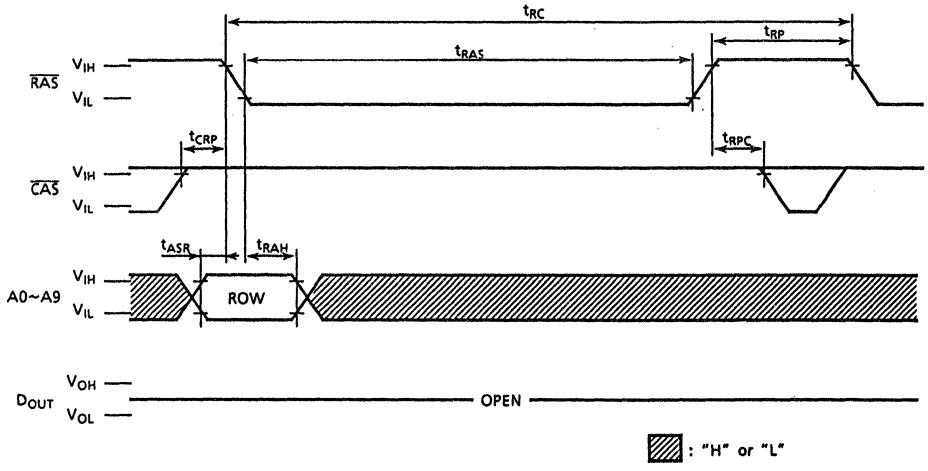
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

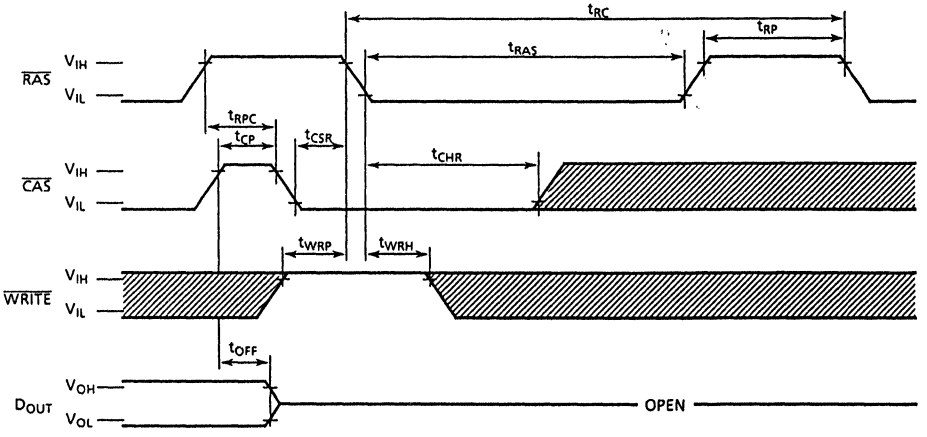


$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, A10 = "H" or "L"

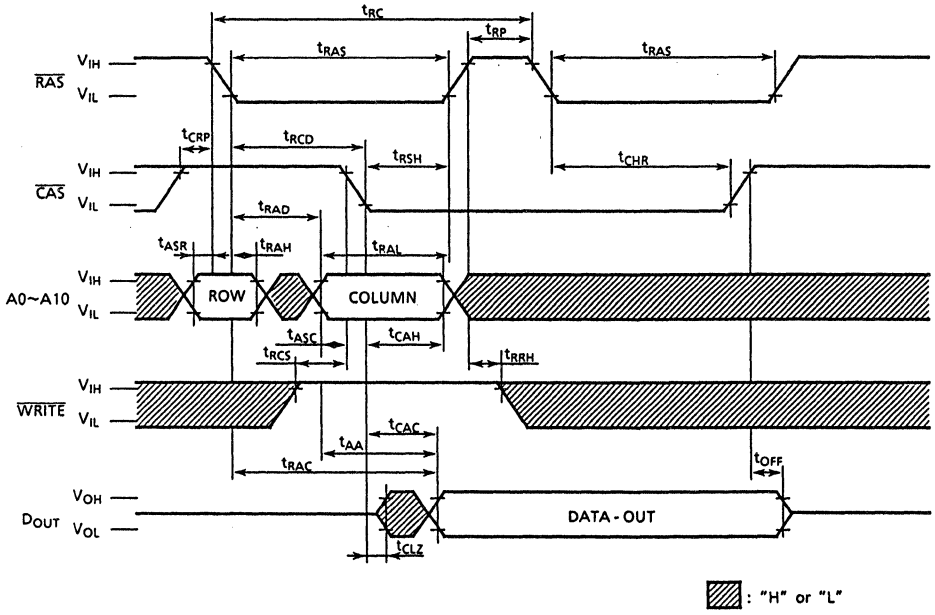
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



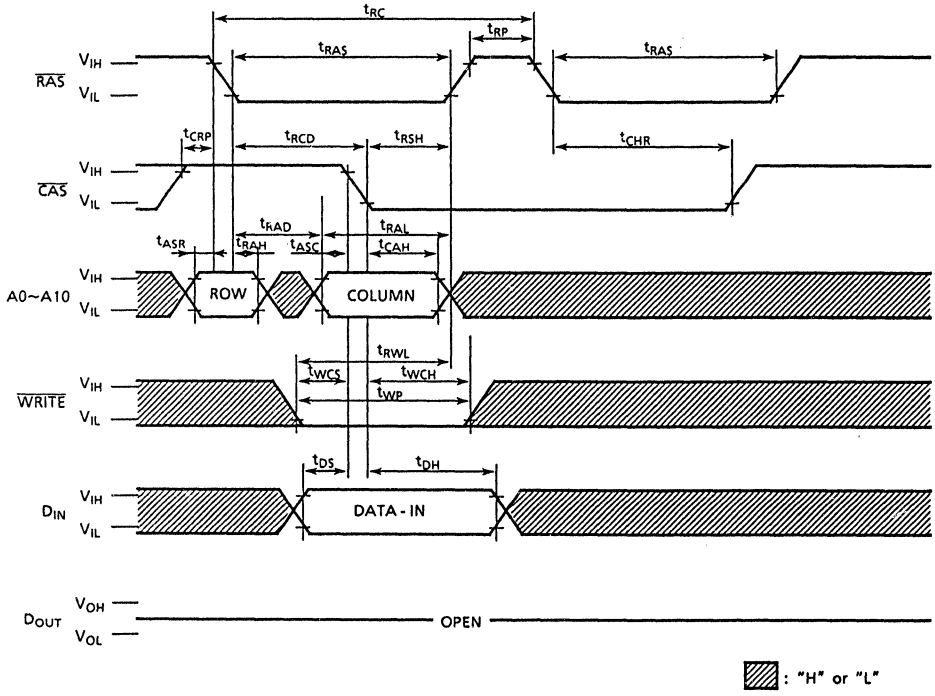
Note: A0~A10 = "H" or "L"

▨ : "H" or "L"

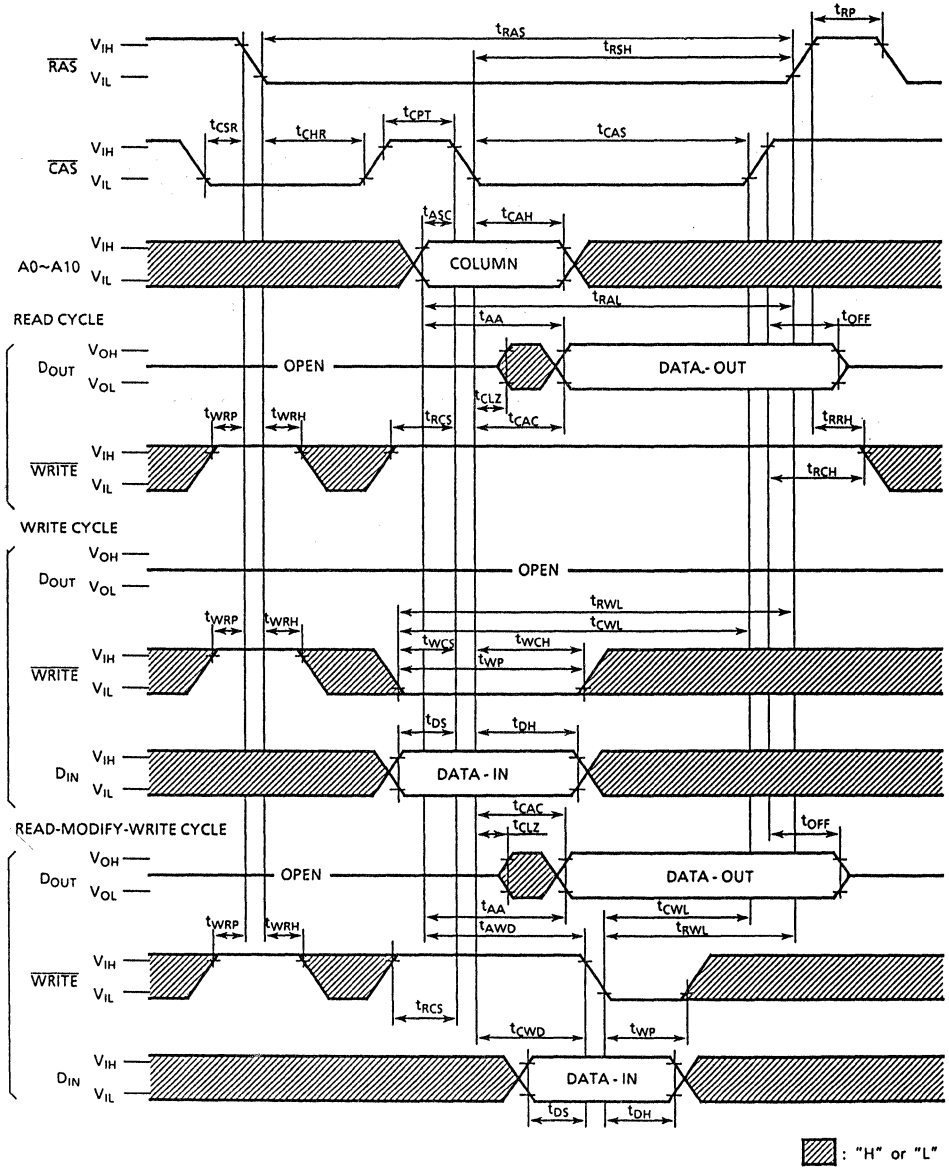
HIDDEN REFRESH CYCLE (READ)



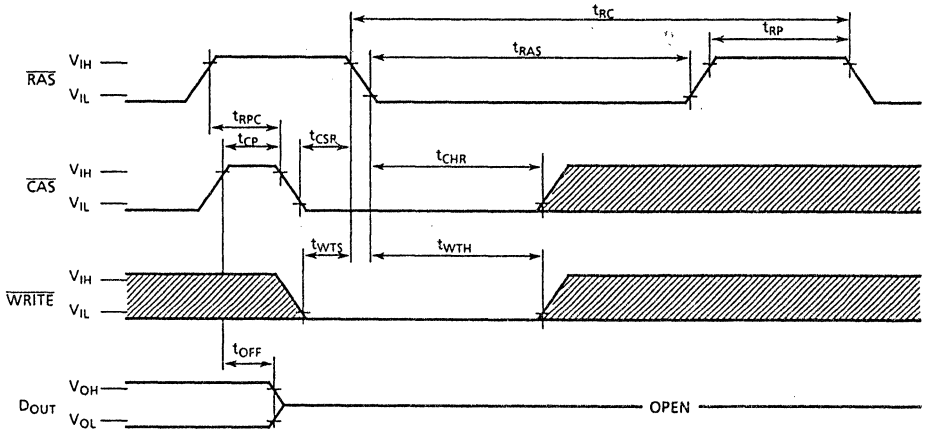
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, CAS BEFORE RAS REFRESH CYCLE



Note : D_{IN}, A0~A10 = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC514100AP/AJ/ASJ/AZ is the RAM organized 4,194,304 words by 1 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig.1 shows the block diagram of TC514100AP/AJ/ASJ/AZ. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

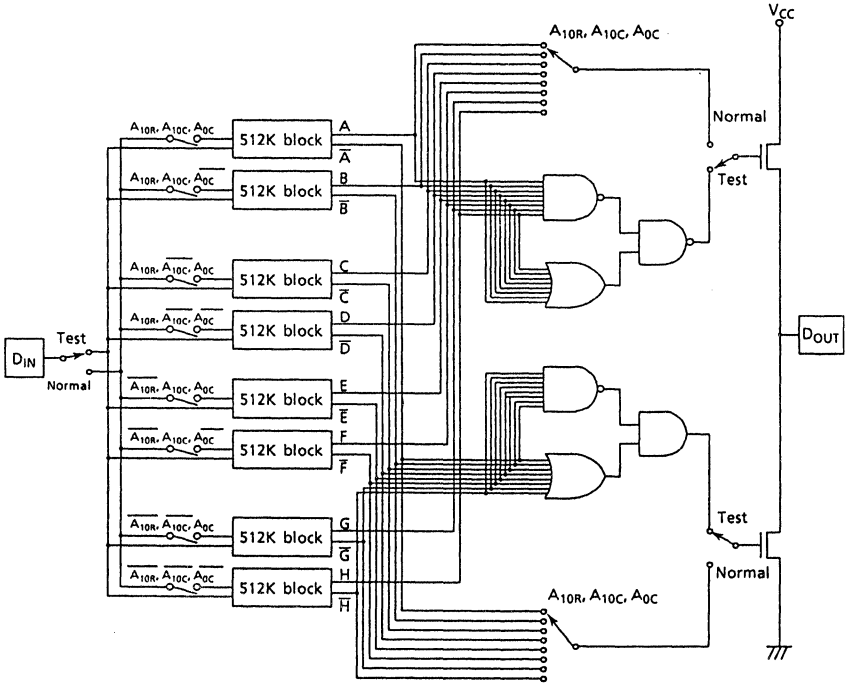


Fig. 1

NOTES

4,194,304 WORD × 1 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514100APL/AJL/ASJL/AZL is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514100APL/AJL/ASJL/AZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514100APL/AJL/ASJL/AZL to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 1bit organization
- Fast access time and cycle time

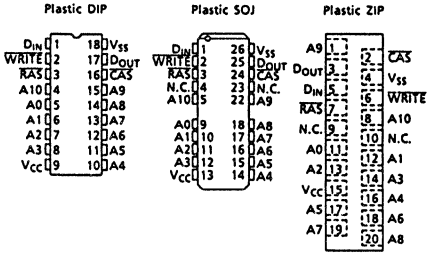
	TC514100APL/AJL/ASJL/AZL-70/80/10		
t_{RAC} $\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA} Column Address Access Time	35ns	40ns	50ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC} Cycle Time	130ns	150ns	180ns
t_{PC} Fast Page Mode Cycle Time	45ns	50ns	60ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 550mW MAX. Operating (TC514100APL/AJL/ASJL/AZL-70)
  - 468mW MAX. Operating (TC514100APL/AJL/ASJL/AZL-80)
  - 413mW MAX. Operating (TC514100APL/AJL/ASJL/AZL-10)
  - 1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514100APL : DIP18-P-300E
  TC514100AJL : SOJ26-P-350
  TC514100ASJL: SOJ26-P-300A
  TC514400AZL : ZIP20-P-400A

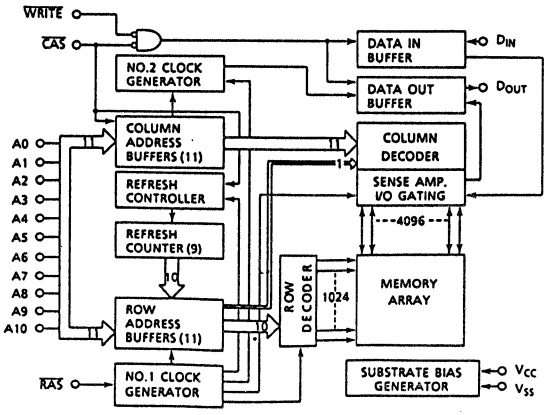
PIN NAMES

A0~A10	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	N.C.	No Connection
$\overline{CAS}$	Column Address Strobe		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature·Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514100APL/AJL/ASJL/AZL-70	–	100	mA	3, 4
		TC514100APL/AJL/ASJL/AZL-80	–	85		5
		TC514100APL/AJL/ASJL/AZL-10	–	75		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514100APL/AJL/ASJL/AZL-70	–	100	mA	3,5
		TC514100APL/AJL/ASJL/AZL-80	–	85		
		TC514100APL/AJL/ASJL/AZL-10	–	75		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514100APL/AJL/ASJL/AZL-70	–	70	mA	3, 4
		TC514100APL/AJL/ASJL/AZL-80	–	60		5
		TC514100APL/AJL/ASJL/AZL-10	–	55		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514100APL/AJL/ASJL/AZL-70	–	100	mA	3,5
		TC514100APL/AJL/ASJL/AZL-80	–	85		
		TC514100APL/AJL/ASJL/AZL-10	–	75		
I_{CC7}	Battery Back Up Current Average power Supply Current, Battery Back Up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V A0~10 = V_{CC} – 0.2V or 0.2V, D_{IN} = V_{CC} – 0.2V, 0.2V or OPEN: t_{RC} = 125µs, t_{RAS} = 300ns ~ 1µs)		–	400	µA	3,6
I_{CC7}	Battery Back Up Current Average power Supply Current, Battery Back Up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V A0~10 = V_{CC} – 0.2V or 0.2V, D_{IN} = V_{CC} – 0.2V, 0.2V or OPEN: t_{RC} = 125µs, t_{RAS} = t_{RAS} MIN. ~300ns)		–	300	µA	3,6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514100APL/ AJL/ASJL/AZL-70		TC514100APL/ AJL/ASJL/AZL-80		TC514100APL/ AJL/ASJL/AZL-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	–	175	–	210	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	70	–	75	–	90	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	10, 15 16
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	10, 15
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	10, 16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	–	55	ns	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	200,000	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	12
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	

ELECTRICAL CHARACTGERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514100APL/ AJL/ASJL/AZL-70		TC514100APL/ AJL/ASJL/AZL-80		TC514100APL/ AJL/ASJL/AZL-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	13
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	13
t_{REF}	Refresh Period	–	128	–	128	–	128	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	20	–	25	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	70	–	80	–	100	–	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	–	40	–	50	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	40	–	45	–	55	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	–	10	–	10	–	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	–	10	–	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTGERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514100APL/ AJL/ASJL/AZL-70		TC514100APL/ AJL/ASJL/AZL-80		TC514100APL/ AJL/ASJL/AZL-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read Write Cycle Time	135	–	155	–	185	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	–	180	–	215	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	75	–	80	–	95	–	ns	14
t_{RAC}	Access Time from $\overline{RAS}$	–	75	–	85	–	105	ns	10, 15 16
t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	10, 15
t_{AA}	Access Time from Column Address	–	40	–	45	–	55	ns	10, 16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	50	–	60	ns	10
t_{RAS}	$\overline{RAS}$ Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	75	200,000	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	75	–	85	–	105	–	ns	
t_{RHCP}	$\overline{CAS}$ Prechrge to $\overline{RAS}$ Hold Time	40	–	50	–	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	45	–	55	–	ns	
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	25	–	25	–	30	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	75	–	85	–	105	–	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	40	–	45	–	55	–	ns	14
t_{CPWD}	$\overline{CAS}$ Prechrge to $\overline{WRITE}$ Delay Time	45	–	50	–	60	–	ns	14

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

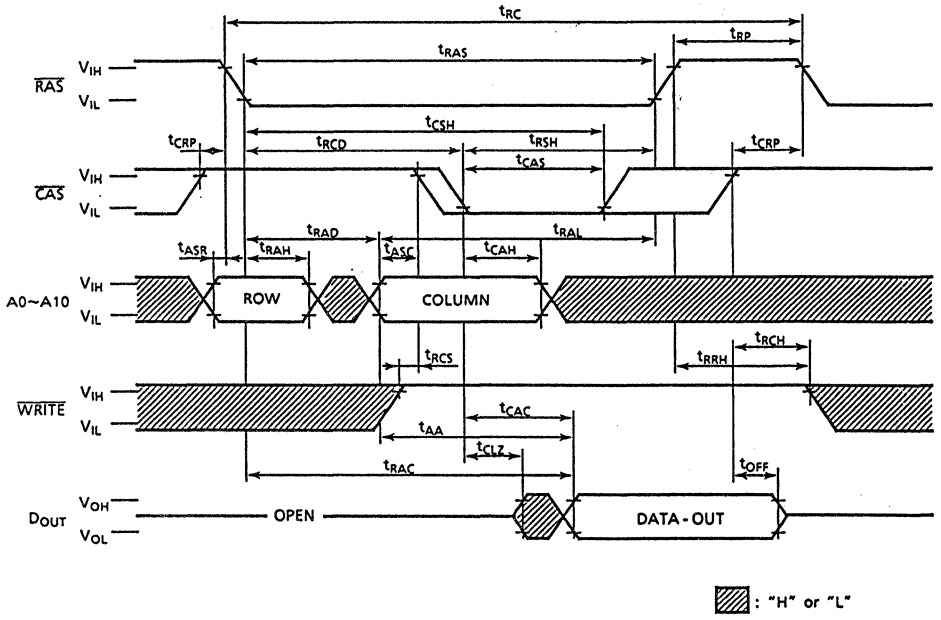
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

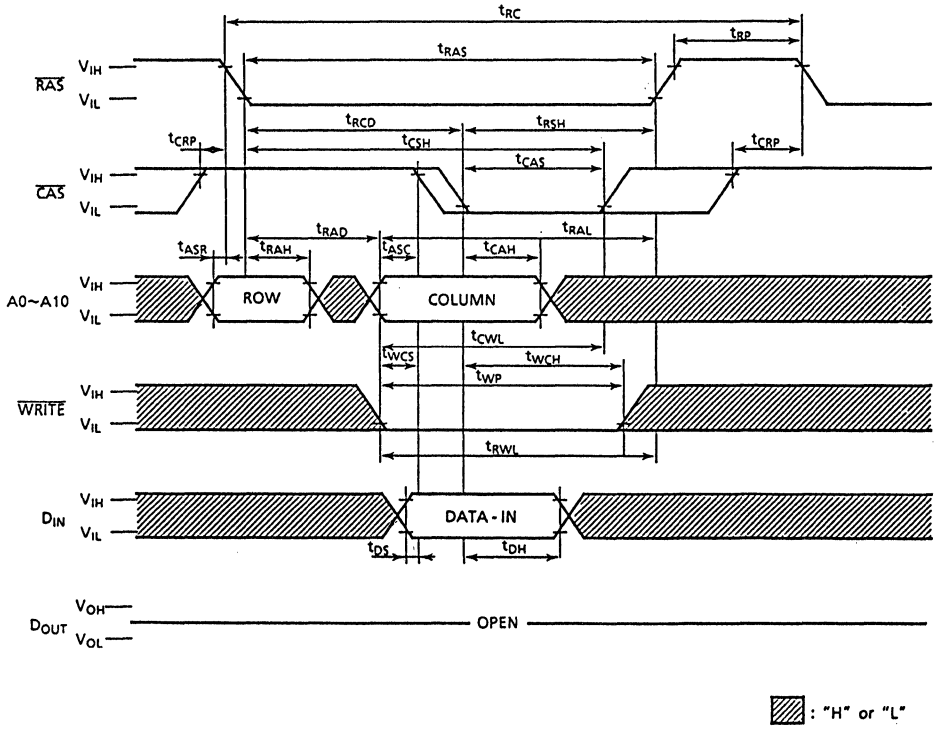
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. t_{RAS} (max.)=1μs is only applied to refresh of battery-back up. t_{RAS} (max.)=10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume t_T=5ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

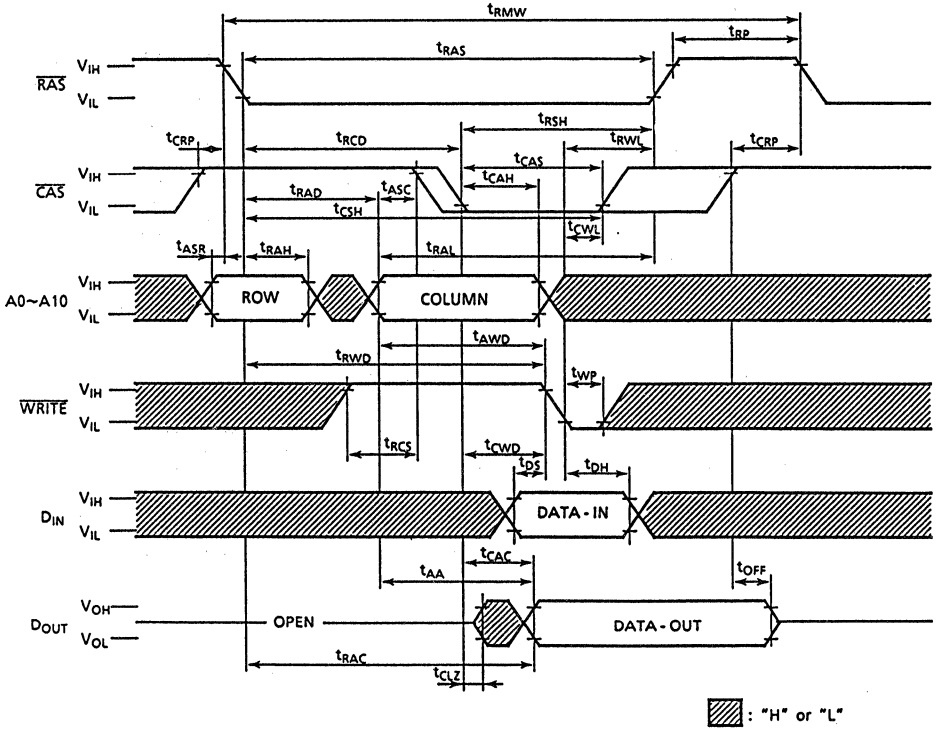
READ CYCLE



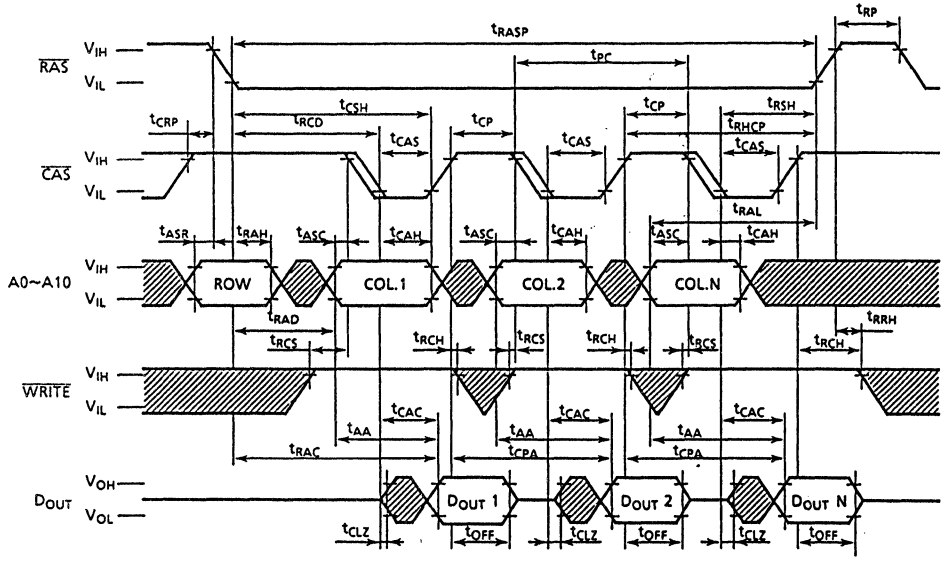
WRITE CYCLE (EARLY WRITE)



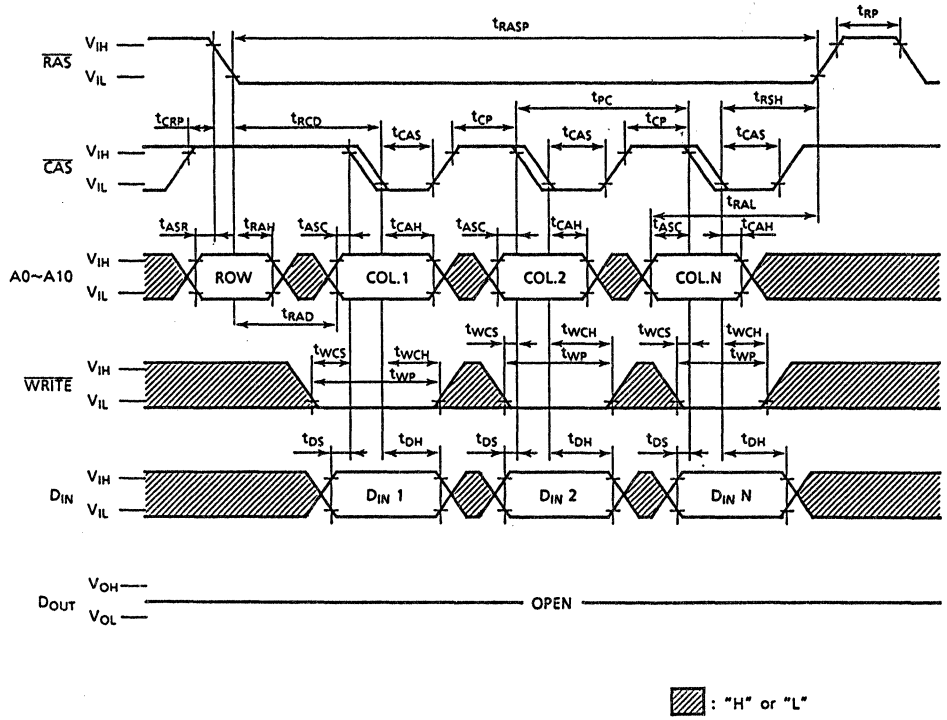
READ-MODIFY-WRITE CYCLE



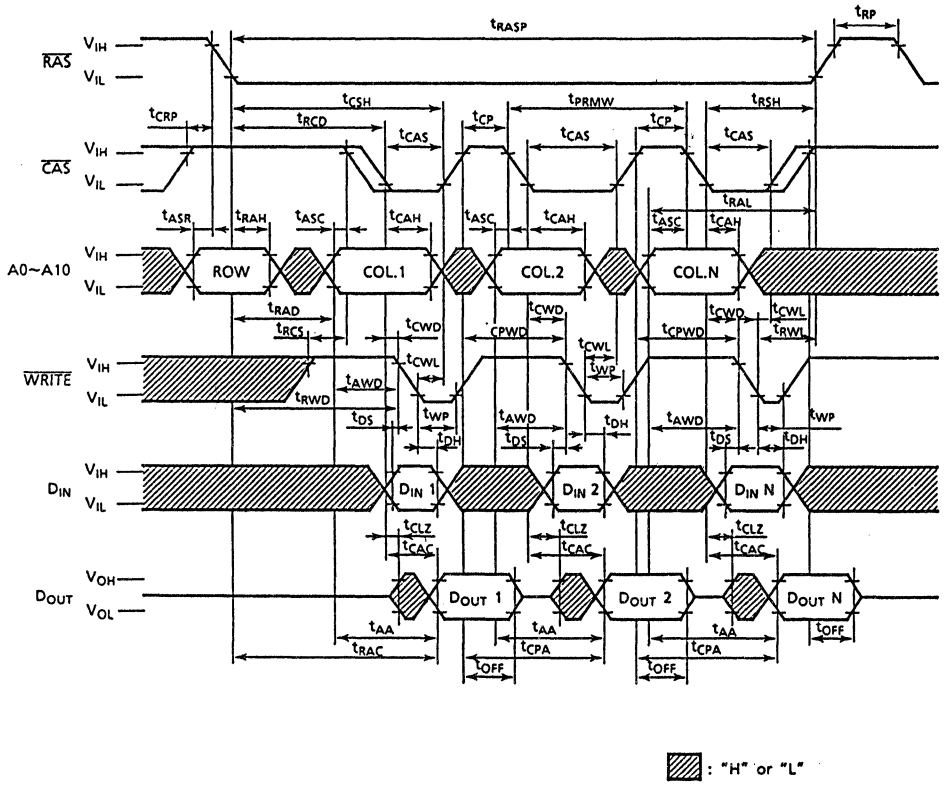
FAST PAGE MODE READ CYCLE



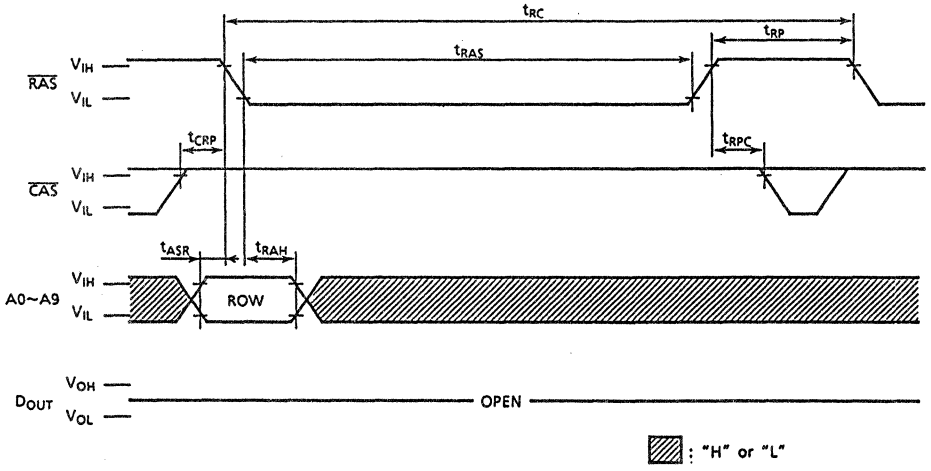
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

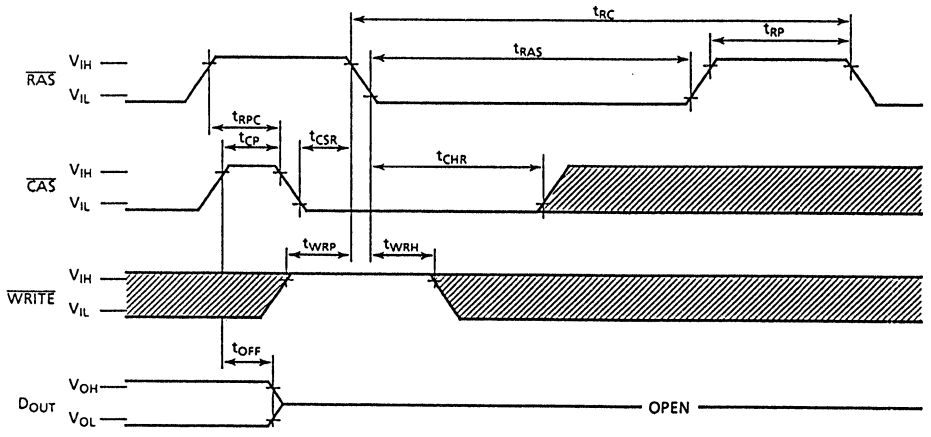


$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, A10 = "H" or "L"

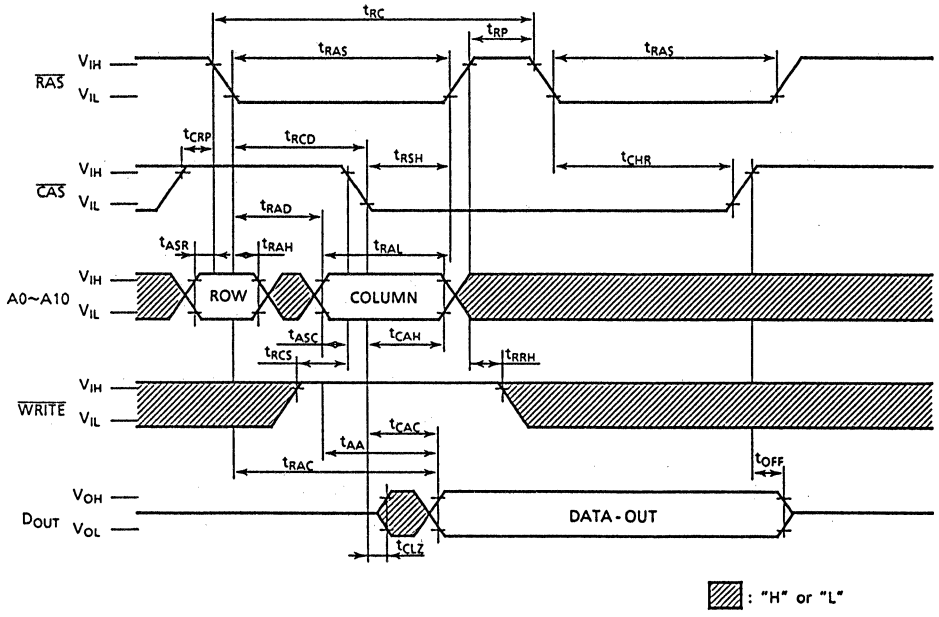
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



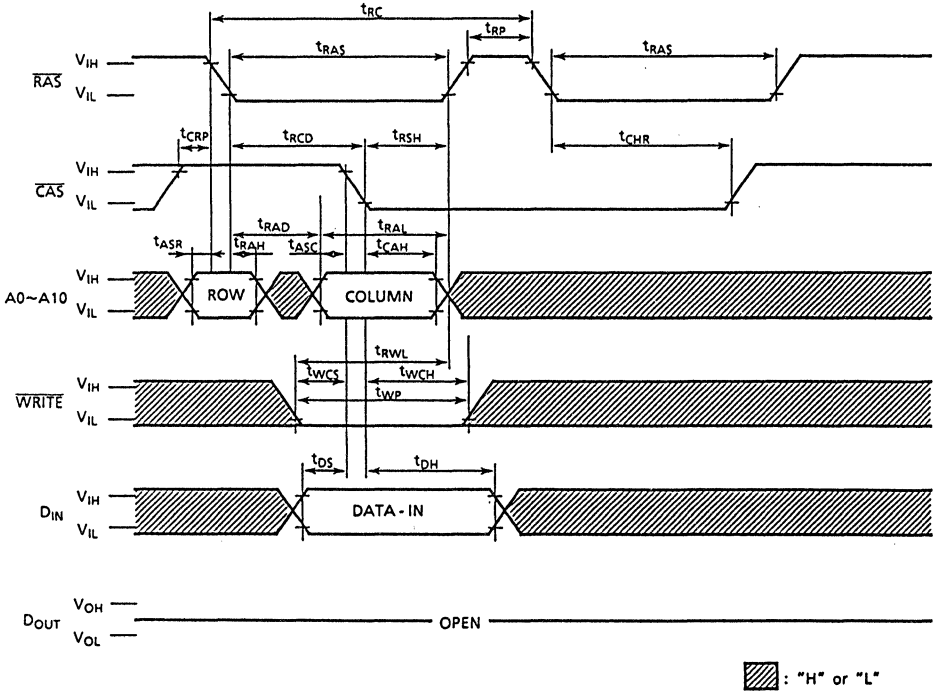
Note: A0~A10 = "H" or "L"

▨ : "H" or "L"

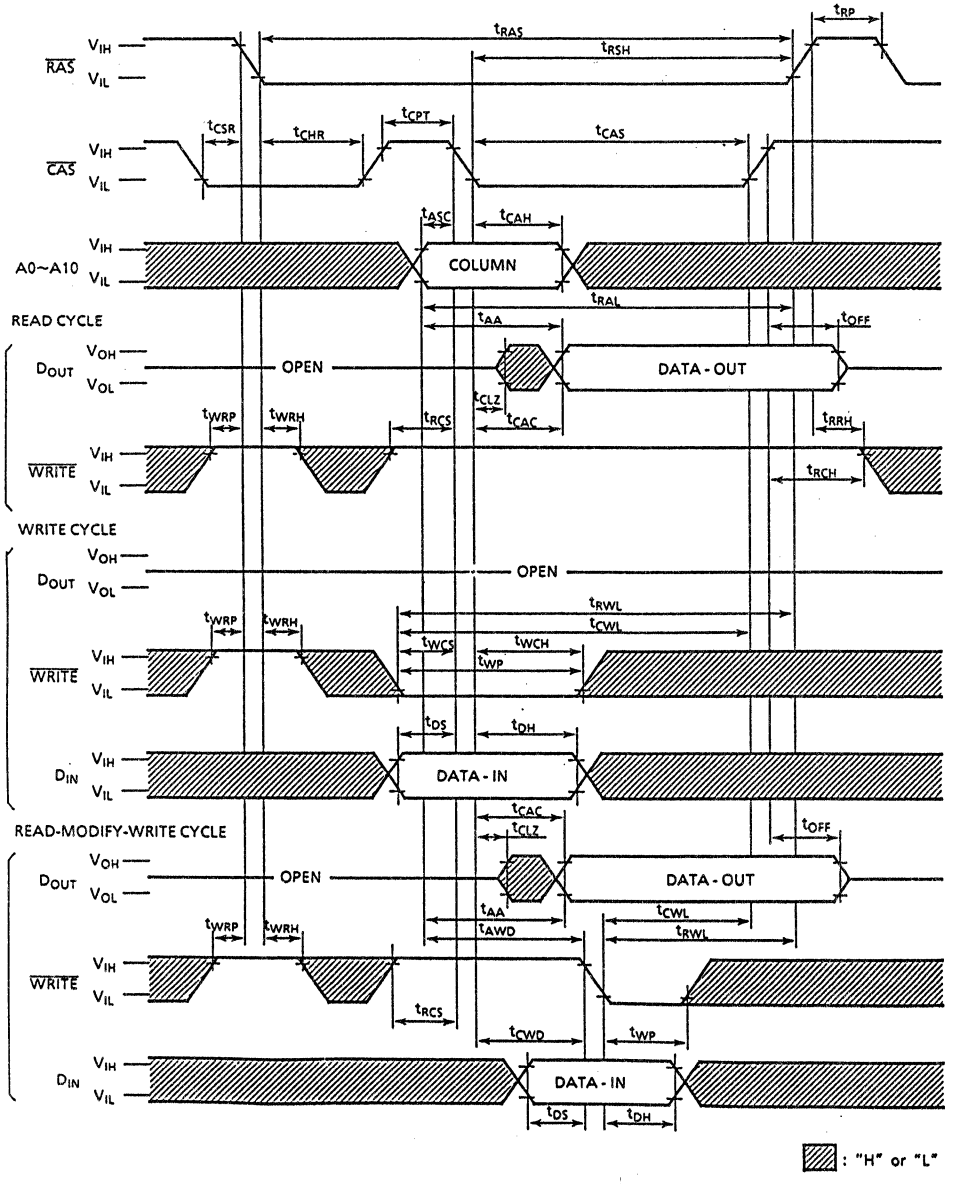
HIDDEN REFRESH CYCLE (READ)



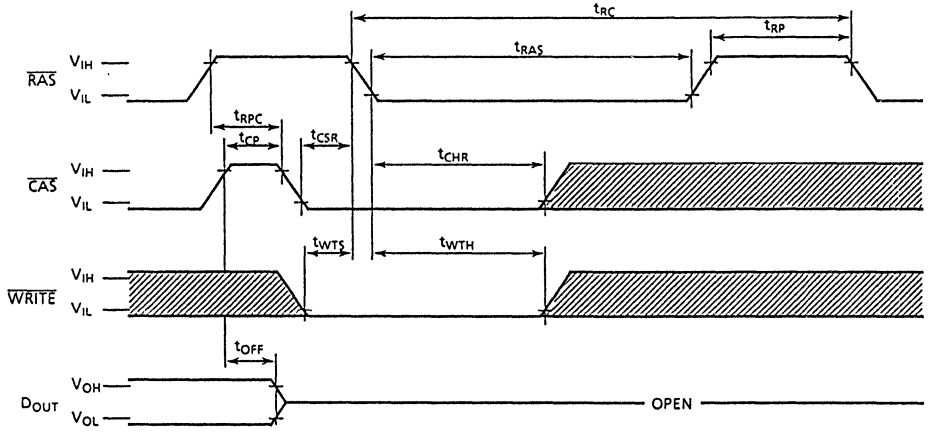
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, CAS BEFORE RAS REFRESH CYCLE



Note: D_{IN}, A0~A10 = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC514100APL/AJL/ASJL/AZL is the RAM organized 4,194,304 words by 1 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, and A_{0C} are not used. If, upon reading, all bits equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig.1 shows the block diagram of TC514100APL/AJL/ASJL/AZL. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

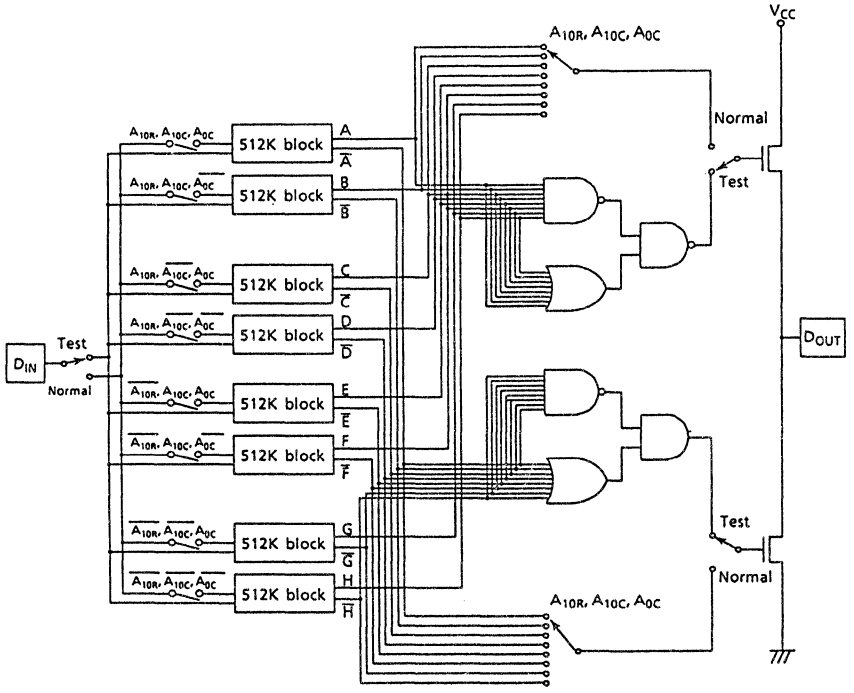


Fig. 1

NOTES

4,194,304 WORD x 1 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514101J/Z is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514101J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514101J/Z to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

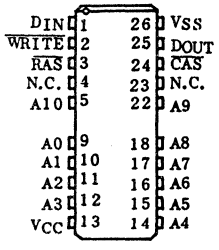
- 4,194,304 word by 1 bit organization
- Fast access time and cycle time

		TC514101J/Z-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{NC}	Nibble Mode Cycle Time	40ns	45ns

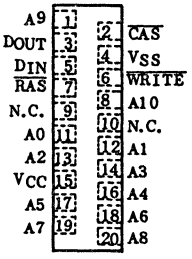
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low power
  578mW Operating (TC514101J/Z-80)
  495mW Operating (TC514101J/Z-10)
  5.5mW MAX. Standby
- Output unlatched at cylce end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Nibble Mode and Test Mode capability
- All inputs and output TTL compatible
- 1024 refresh cycles/16ms
- Package Plastic SOJ: TC514101J
  Plastic ZIP: TC514101Z

PIN CONNECTION (TOP VIEW)

Plastic SOJ



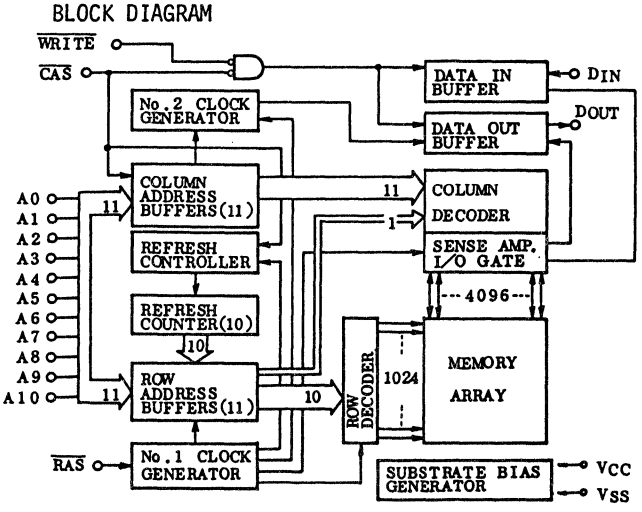
Plastic ZIP



PIN NAMES

A0 ∿ A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514101J/Z-80	-	105	mA	3,4,5
		TC514101J/Z-10	-	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514101J/Z-80	-	105	mA	3,5
		TC514101J/Z-10	-	90		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{NC}=t_{NC} MIN.)	TC514101J/Z-80	-	60	mA	3,4,5
		TC514101J/Z-10	-	50		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514101J/Z-80	-	105	mA	3
		TC514101J/Z-10	-	90		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514101J/Z -80		TC514101J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	175	-	210	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	45	-	ns	
t_{NRMW}	Nibble Mode Read-Modify-Write Cycle Time	65	-	75	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	40	-	50	ns	9,15
t_{NCAC}	Nibble Mode Access Time	-	20	-	25	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514101J/Z -80		TC514101J/Z -10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	20	-	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	25	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80	-	100	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	40	-	50	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	-	25	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	25	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC}=5V±10%, Ta=0∿70°C) (Note 6, 7, 8)

SYMBOL	PARAMETER	TC514101J/Z -80		TC514101J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	155	-	185	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	105	ns	9.14.15
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	30	ns	9,14
t_{AA}	Access Time from Column Address	-	45	-	55	ns	9,15
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	105	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	105	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A10, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.

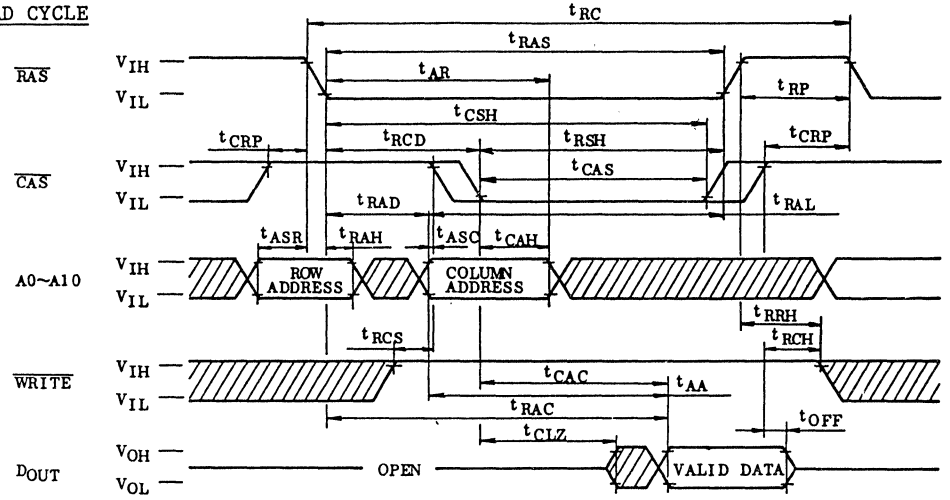
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

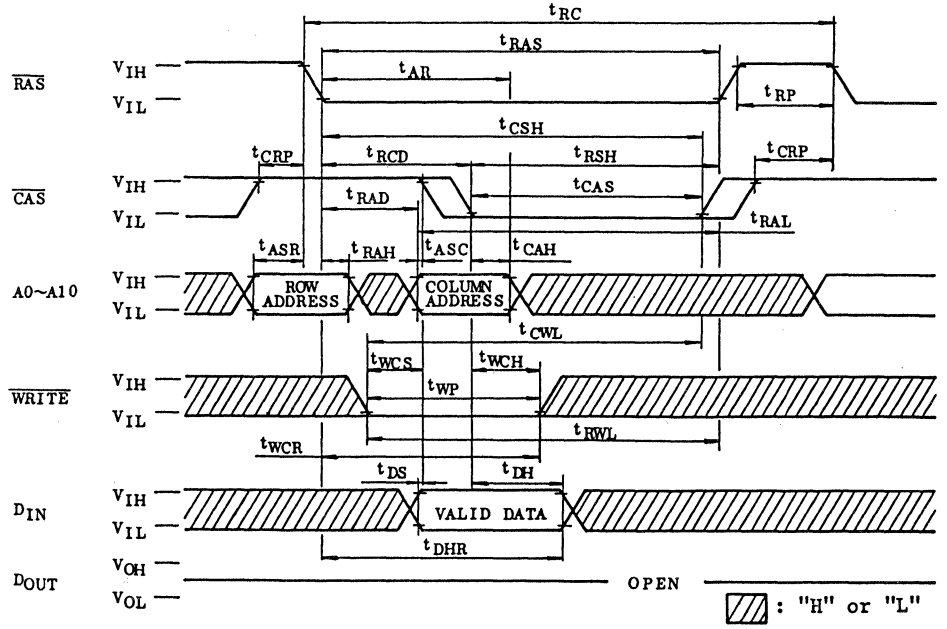
15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

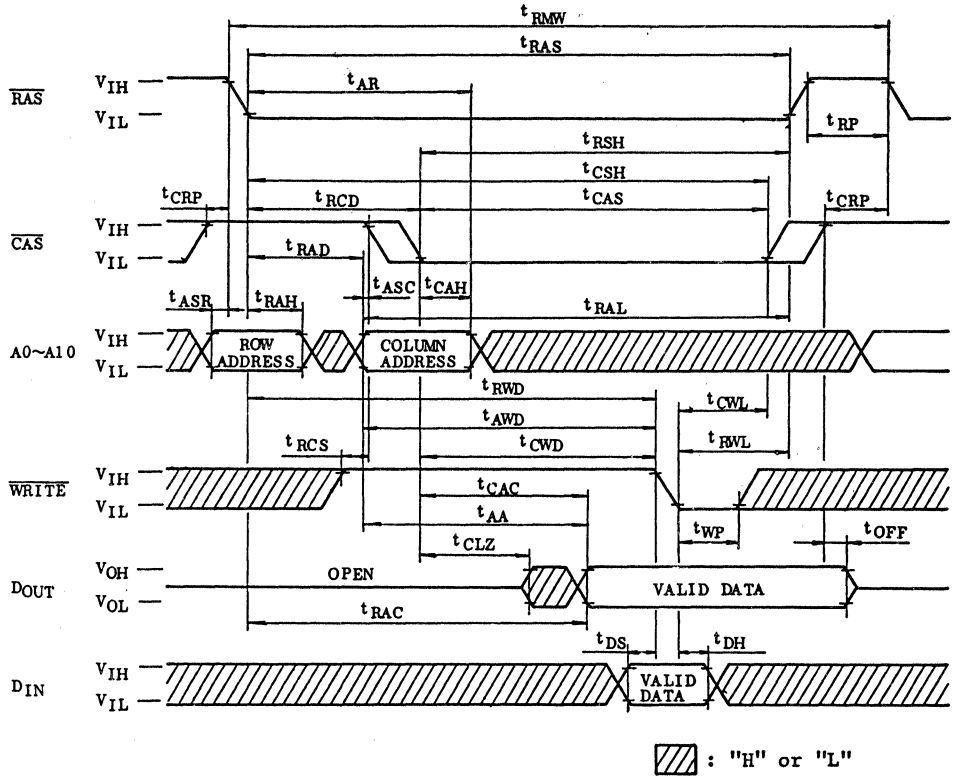
READ CYCLE



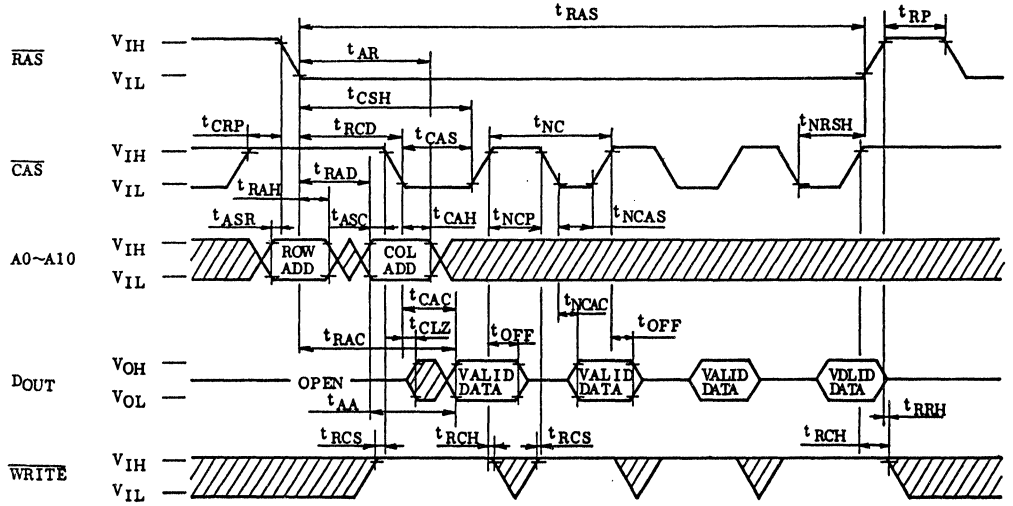
WRITE CYCLE (EARLY WRITE)



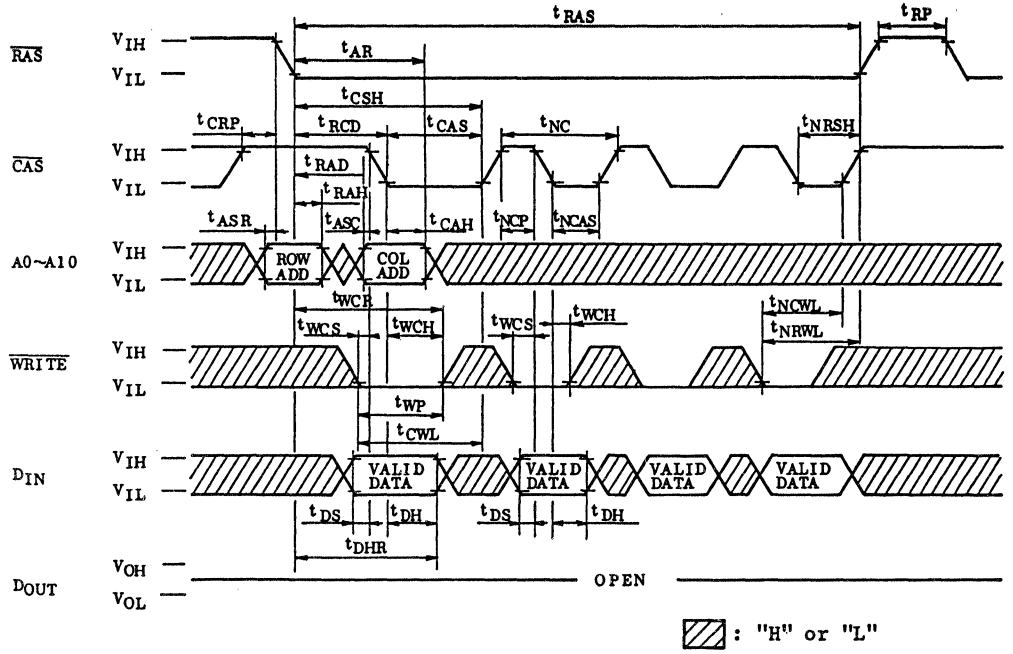
READ-MODIFY-WRITE CYCLE



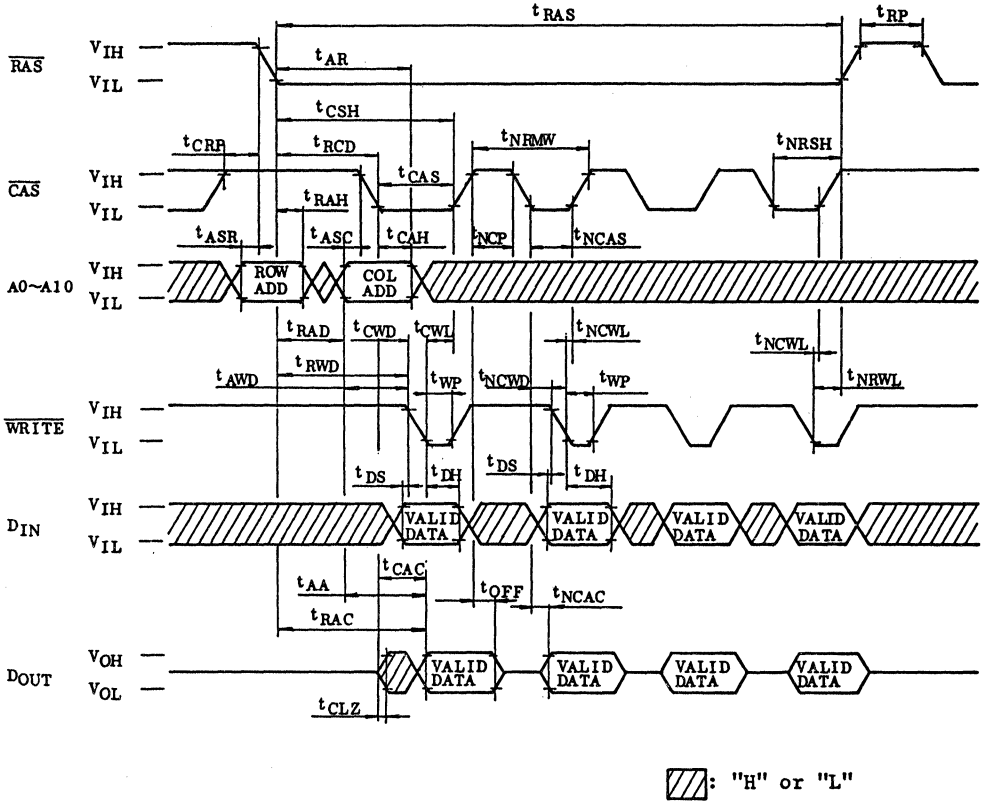
NIBBLE MODE READ CYCLE



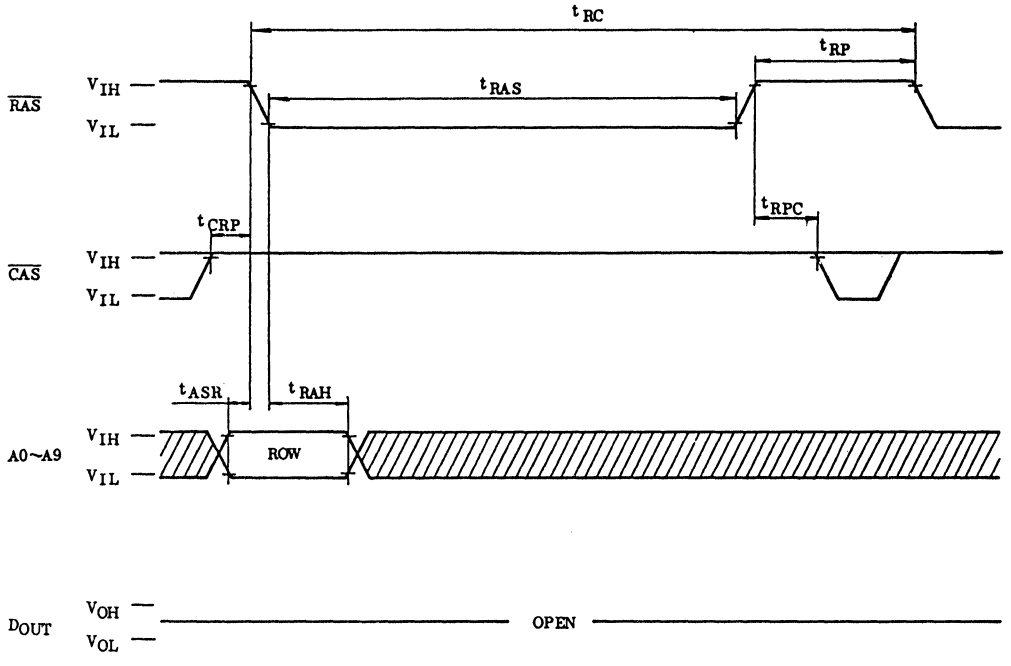
NIBBLE MODE WRITE CYCLE (EARLY WRITE)



NIBBLE MODE READ-MODIFY-WRITE CYCLE



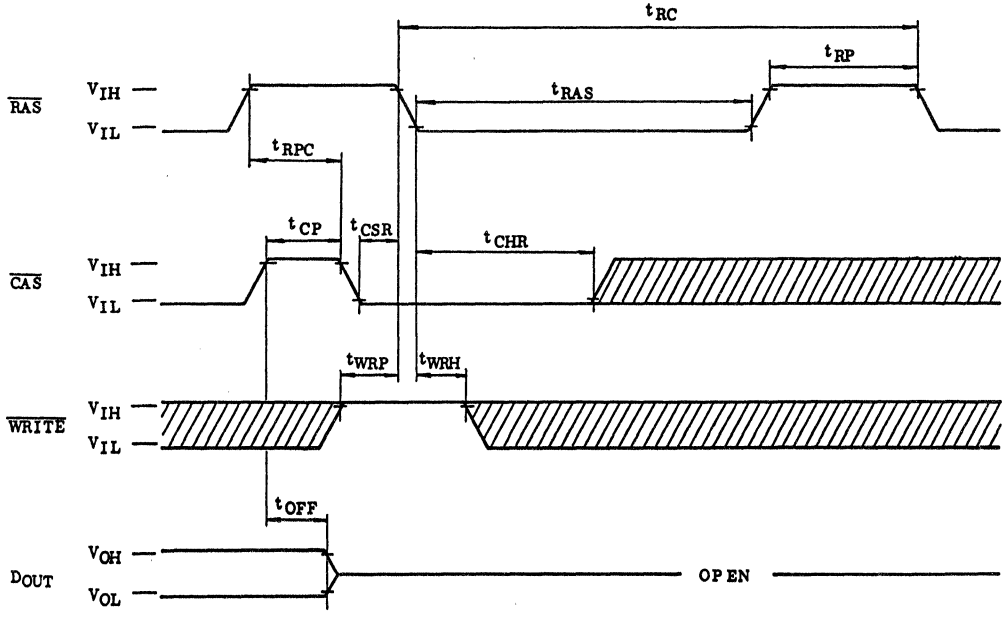
$\overline{RAS}$ ONLY REFRESH CYCLE



▨: "H" or "L"

NOTE: $\overline{WRITE}$="H" or "L" , A10="H" or "L"

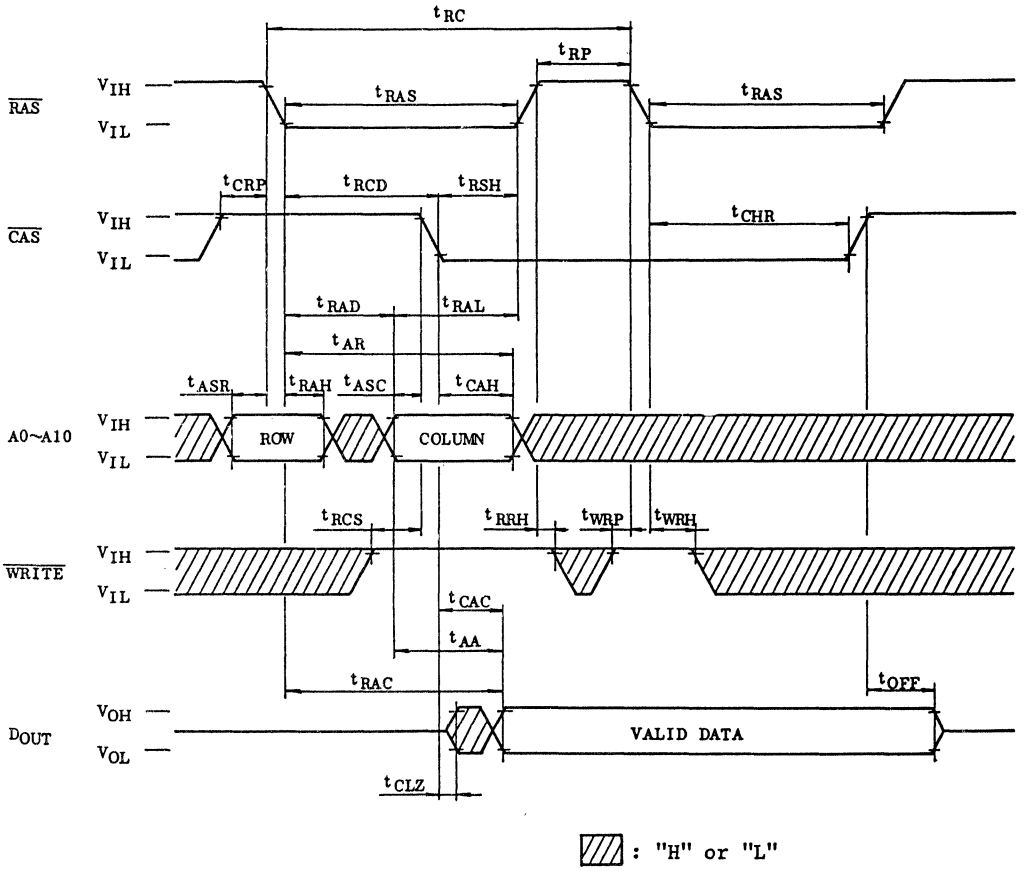
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



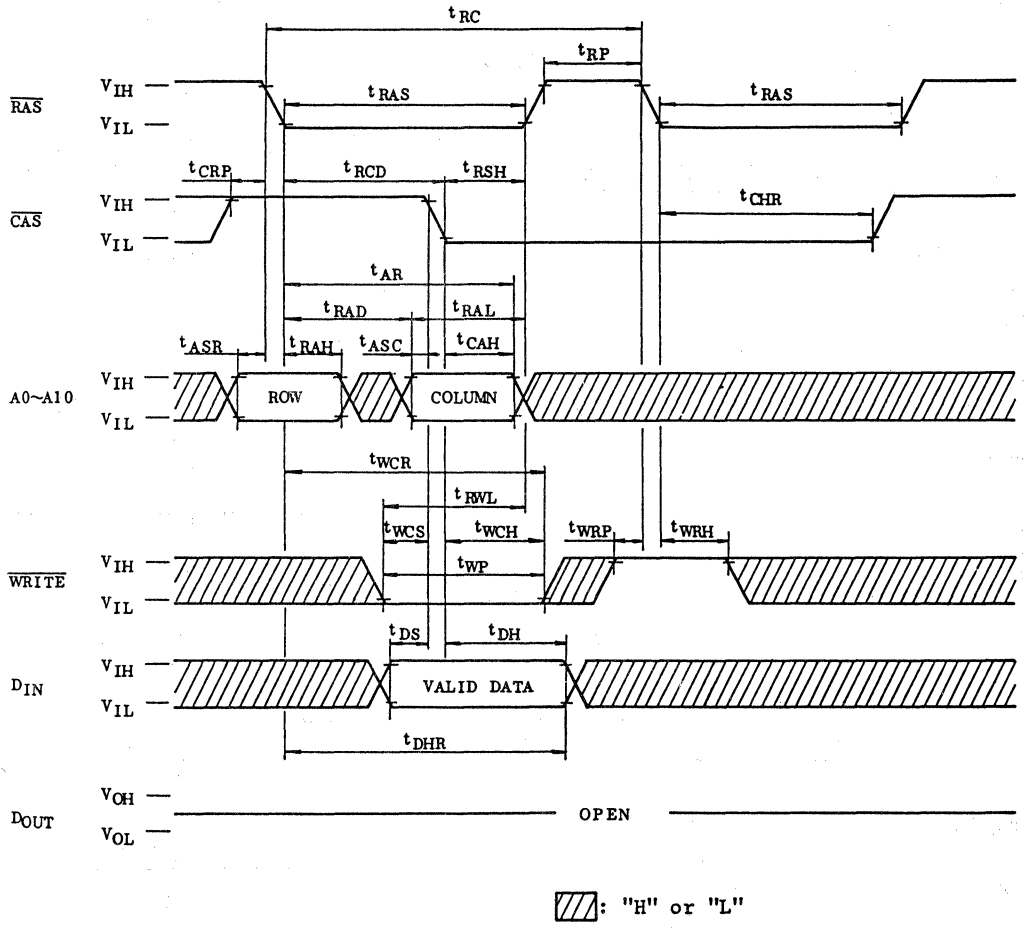
NOTE: A0 ~ A10="H" or "L"

▨: "H" or "L"

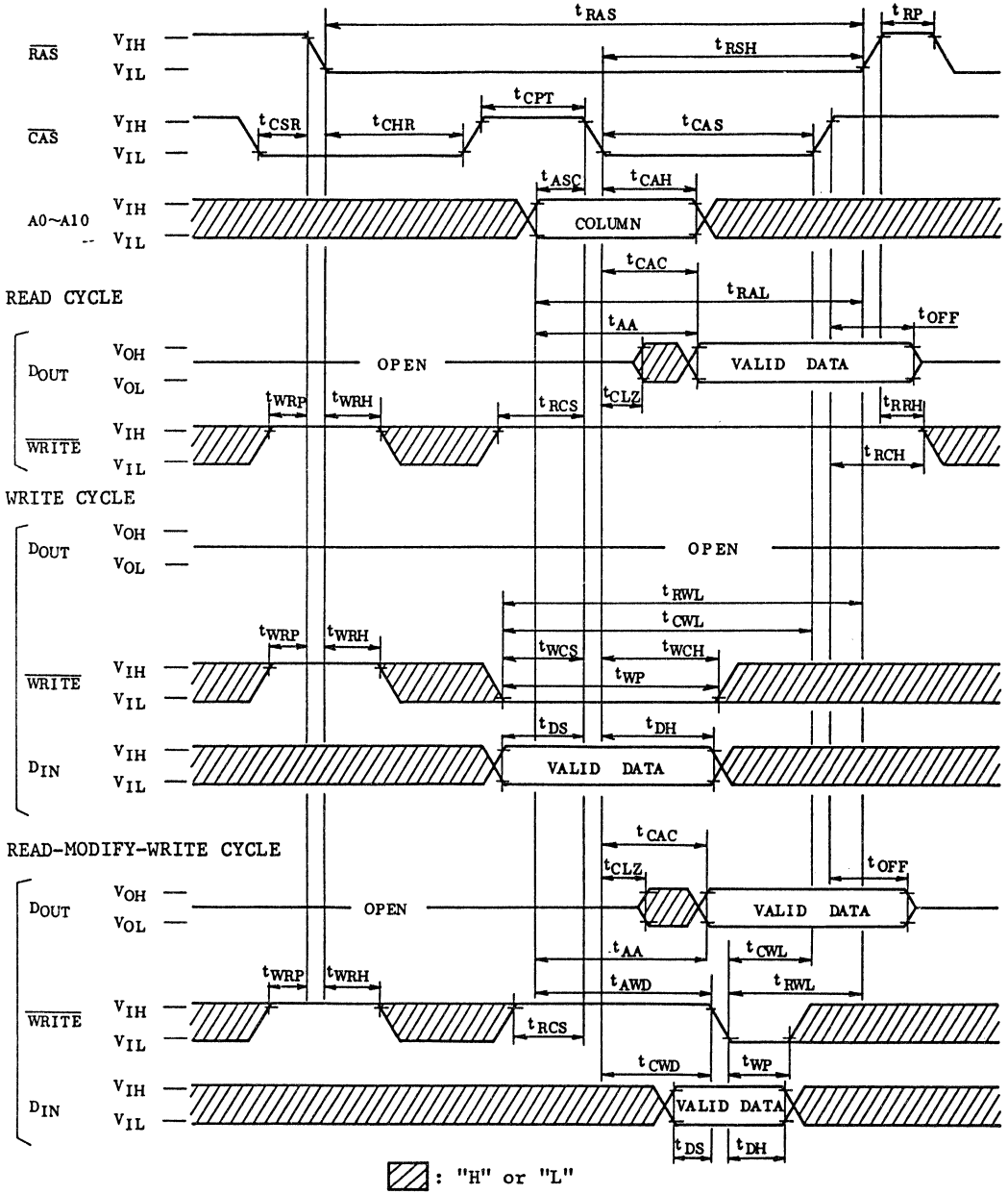
HIDDEN REFRESH CYCLE (READ)



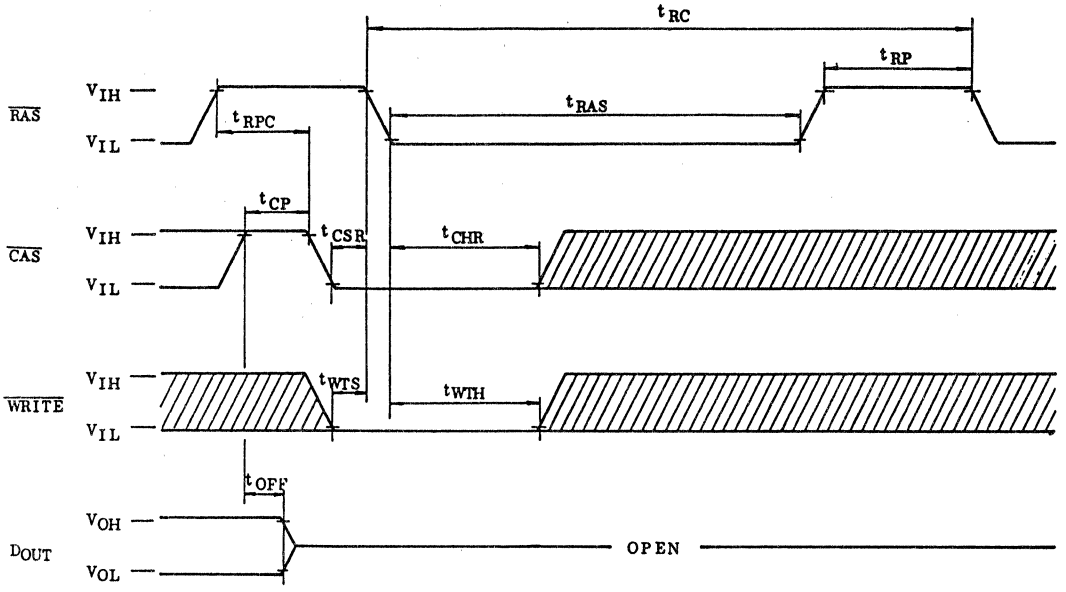
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

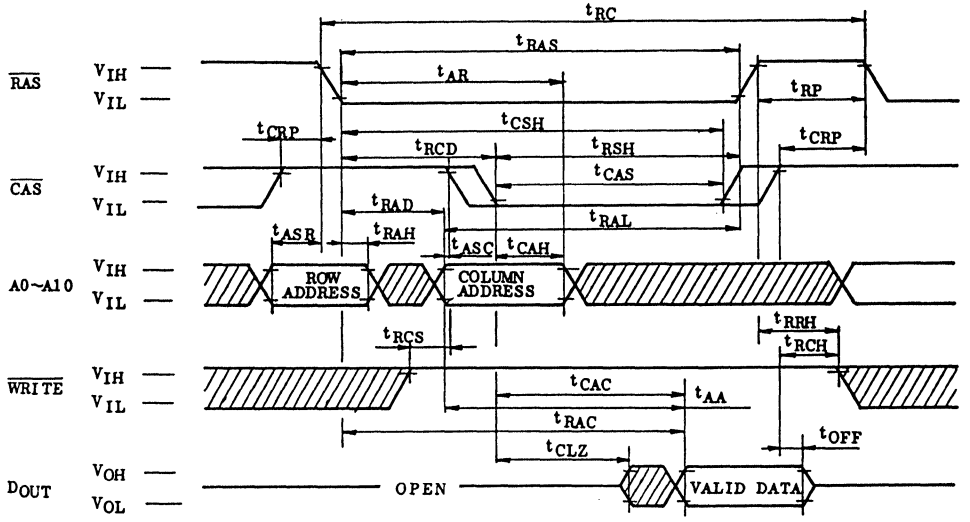


WRITE, CAS BEFORE RAS REFRESH CYCLE

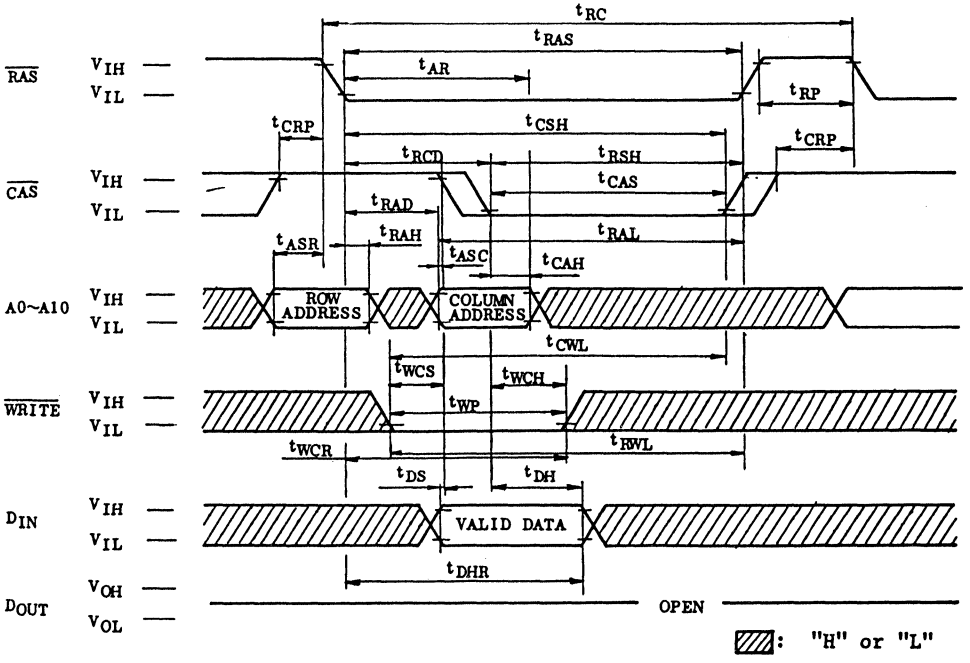


NOTE: D_{IN}, A0 ∿ A10: "H" or "L" ▨ : "H" or "L"

READ CYCLE IN THE TEST MODE



WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



APPLICATION INFORMATION

ADDRESSING

The 22 address bits required to decode 1 of the 4,194,304 cell locations within the TC514101J/Z are multiplexed onto the 11 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 11 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 11 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

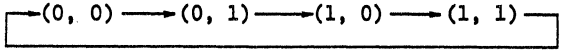
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the ouptut within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC514101J/Z is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate. Row and column address need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A10 determines the starting point of the circular 4 bits nibble. Row A10 and column A10 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A10 row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

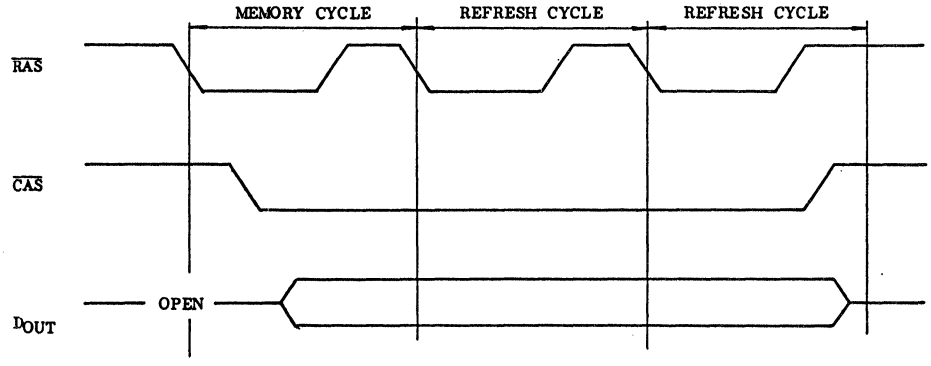
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 1024 row address (A0 ∿ A9) within each 16 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514101J/Z offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC514101J/Z is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refersh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TC514101J/Z can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE).
Repeat this operation 1024 times.

③ Check "1" out of 1024 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST.
Repeat this operation 1024 times.

⑤ Check "0" out of 1024 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

TEST MODE

The TC514101J/Z is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig. 1 shows the block diagram of TC514101J/Z. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN TEST MODE

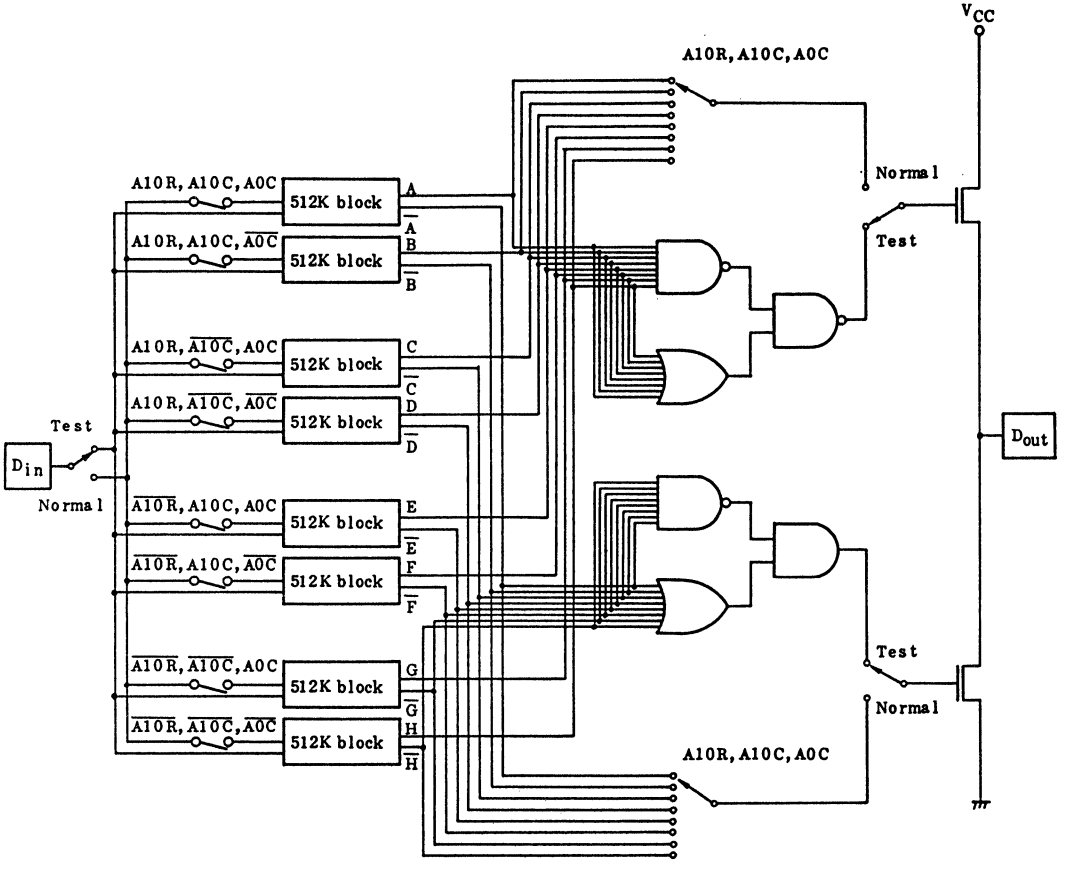


Fig. 1

NOTES

4,194,304 WORD × 1 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514101AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514101AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514101AP/AJ/ASJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ(300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The special feature of TC514101AP/AJ/ASJ/AZ is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

FEATURES

- 4,194,304 word by 1bit organization
- Fast access time and cycle time

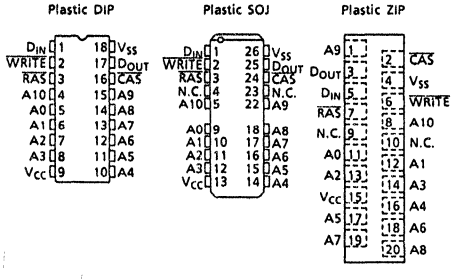
		TC514101AP/AJ/ASJ/AZ-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{NCAC}	Nibble Mode Access Time	20ns
t_{NC}	Nibble Mode Cycle Time	40ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  660mW MAX. Operating
  (TC514101AP/AJ/ASJ/AZ-60)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Nibble Mode and Test Mode capability
- All inputs and output TTL compatible
- 1024 refresh cycles/16ms
- Package TC514101AP : DIP18-P-300E
  TC514101AJ : SOJ26-P-350
  TC514101ASJ : SOJ26-P-300A
  TC514101AZ : ZIP20-P-400A

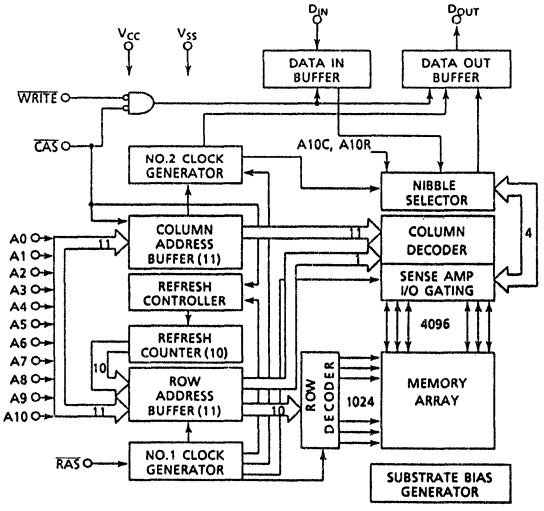
PIN NAMES

A0~A10	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	N.C.	No Connection
$\overline{RAS}$	Row Address Strobe		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514101AP/AJ/ASJ/AZ-60	–	120	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC514101AP/AJ/ASJ/AZ-60	–	120	mA	3,5
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Cycling: $t_{NC} = t_{NC}$ MIN.)	TC514101AP/AJ/ASJ/AZ-60	–	50	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514101AP/AJ/ASJ/AZ-60	–	120	mA	3, 5
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514101AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	135	–	ns	
t_{NC}	Nibble Mode Cycle Time	40	–	ns	
t_{NRMW}	Nibble Mode Read--Modify Write Cycle Time	65	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	20	ns	9,14
t_{AA}	Access Time from Column Address	–	30	ns	9,15
t_{NCAC}	Nibble Mode Access Time	–	20	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	ns	
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514101AP/AJ/ASJ/AZ-60		UNITS	NOTES
		MIN.	MAX.		
t_{DH}	Data-In Hold Time	15	–	ns	12
t_{REF}	Refresh Period	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	15	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	30	–	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	–	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	–	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	–	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	–	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATION CONDITIONS IN THE TEST MODE (Vcc = 5V ± 10%, Ta = 0~70°C) (Note6, 7, 8)

SYMBOL	PARAMETER	TC514101AP/AJ/ASJ/AZ-60		UNITS	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	115	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	65	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	ns	9,15
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

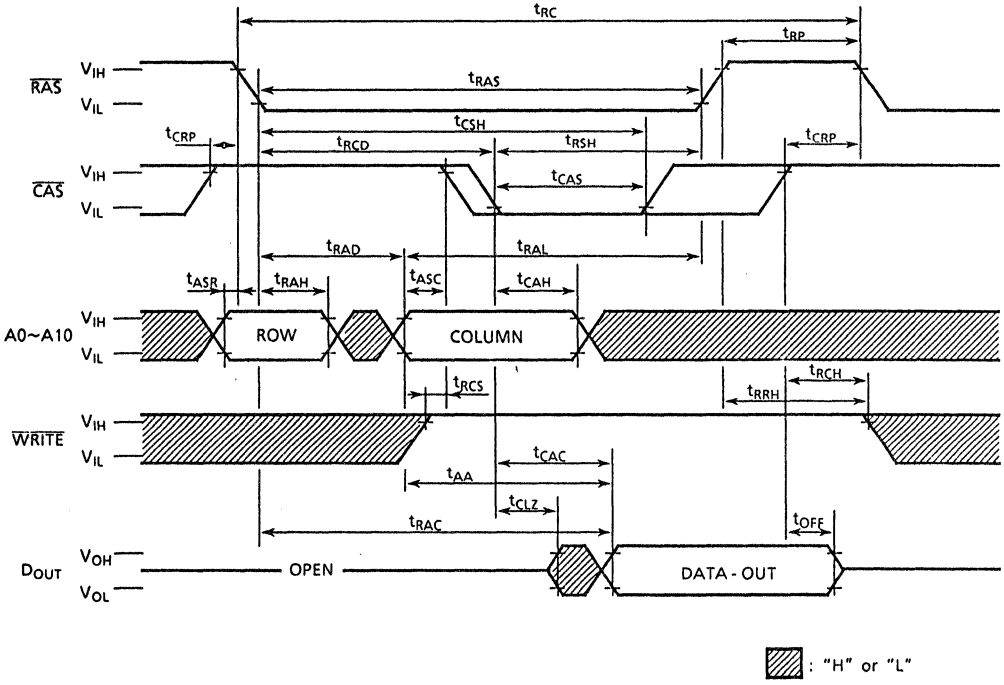
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

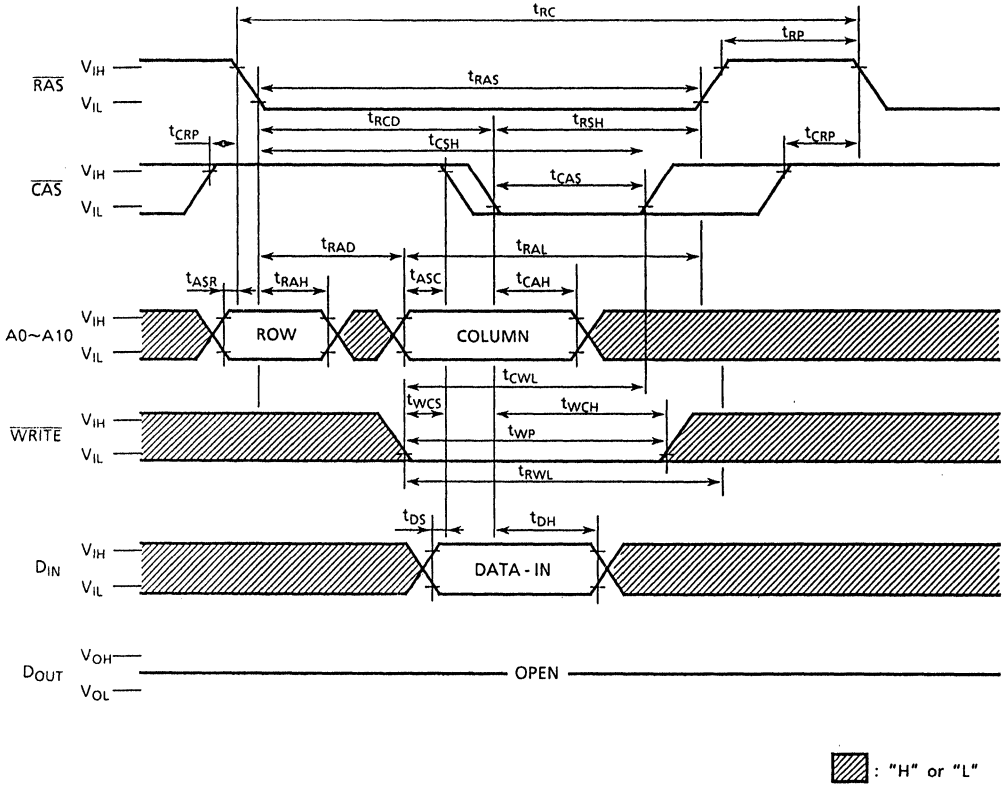
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T=5$ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.) the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

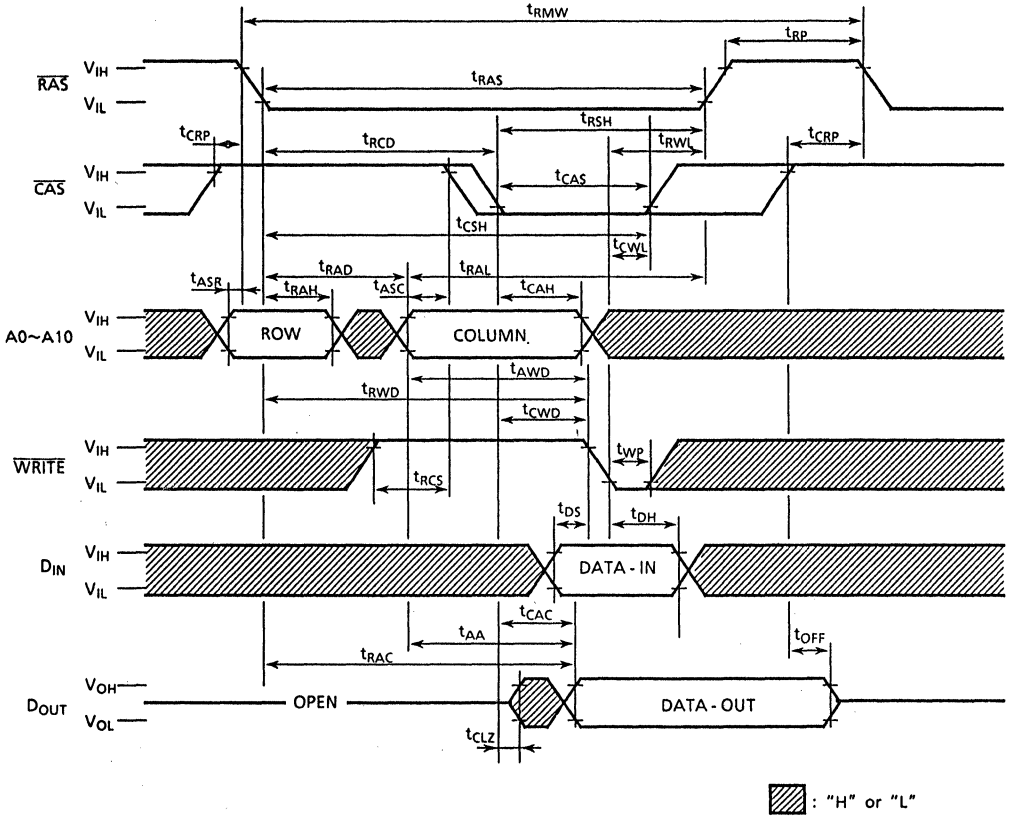
READ CYCLE



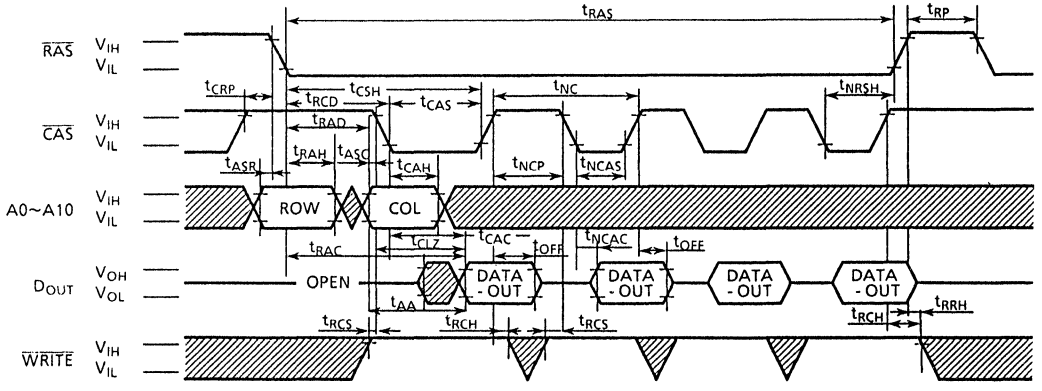
WRITE CYCLE (EARLY WRITE)



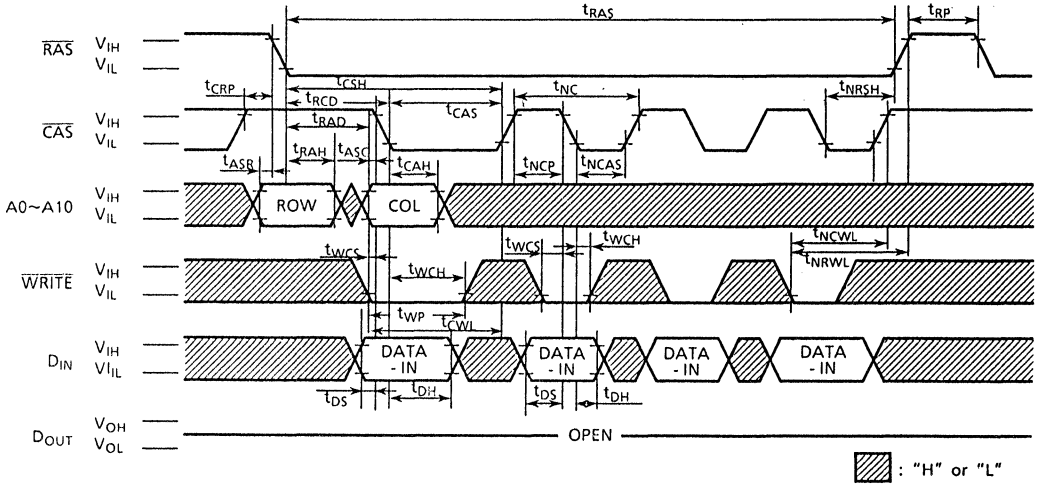
READ-MODIFY-WRITE CYCLE



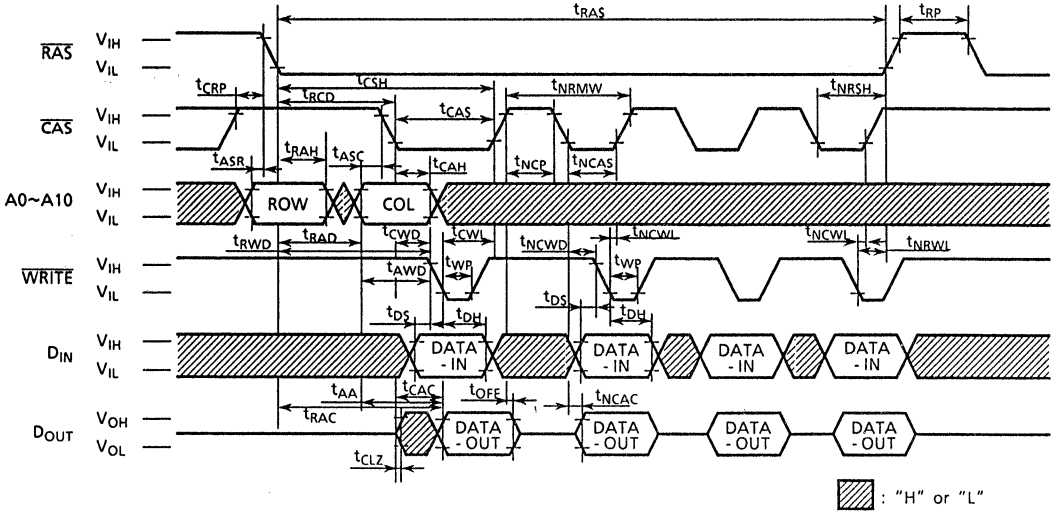
NIBBLE MODE READ CYCLE



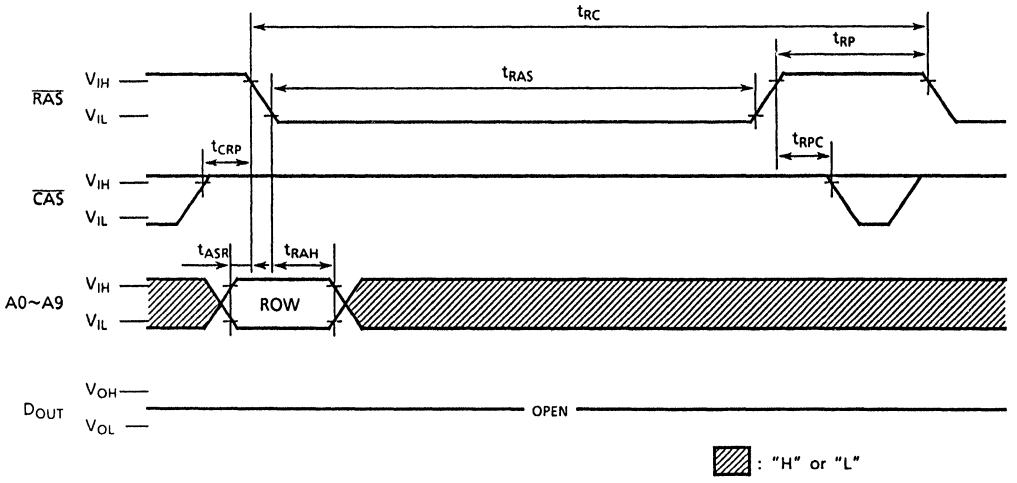
NIBBLE MODE WRITE CYCLE(EARLY WRITE)



NIBBLE MODE READ - MODIFY - WRITE

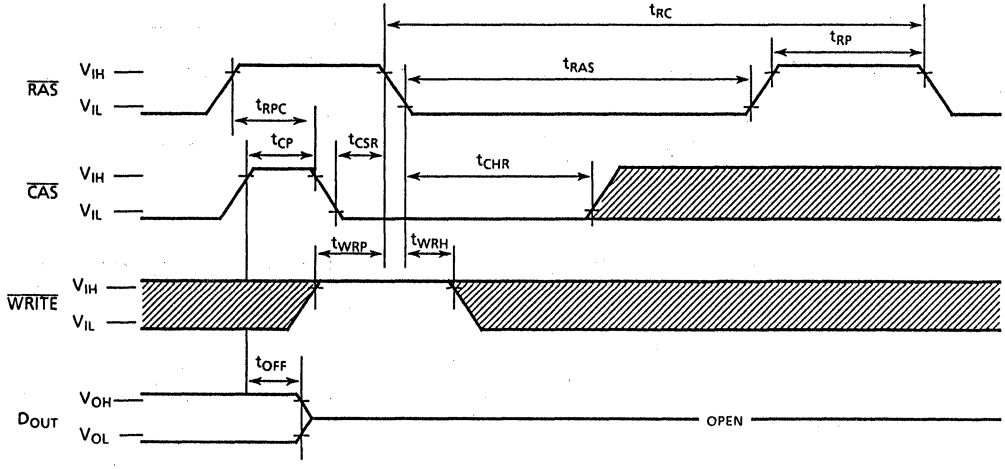


$\overline{RAS}$ ONLY REFRESH CYCLE



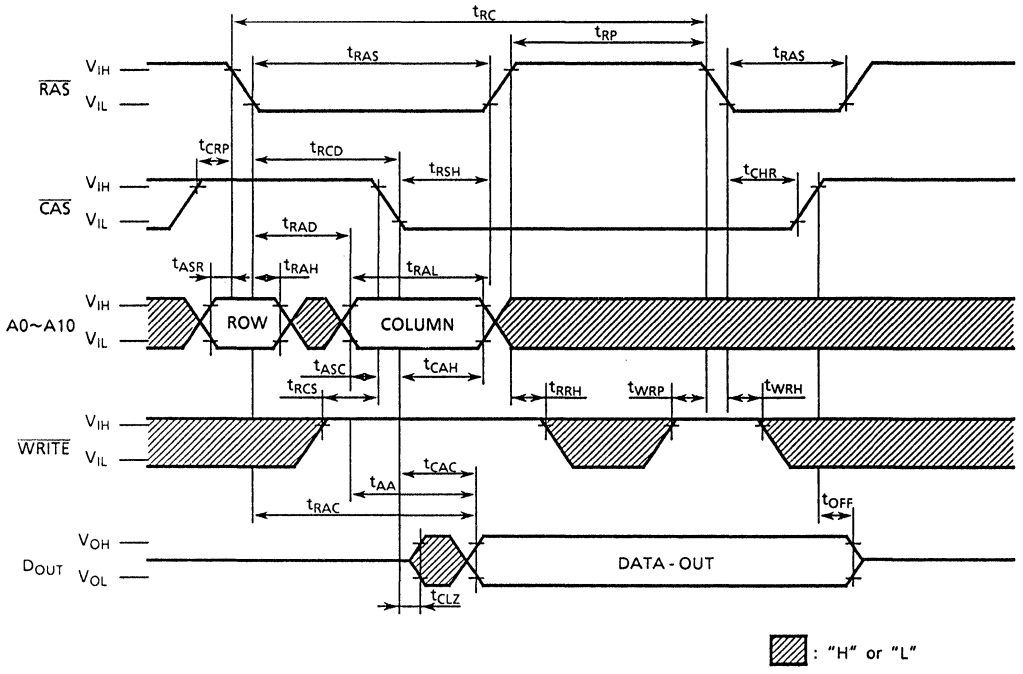
Note: $\overline{WRITE}$ = "H" or "L" A10 = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

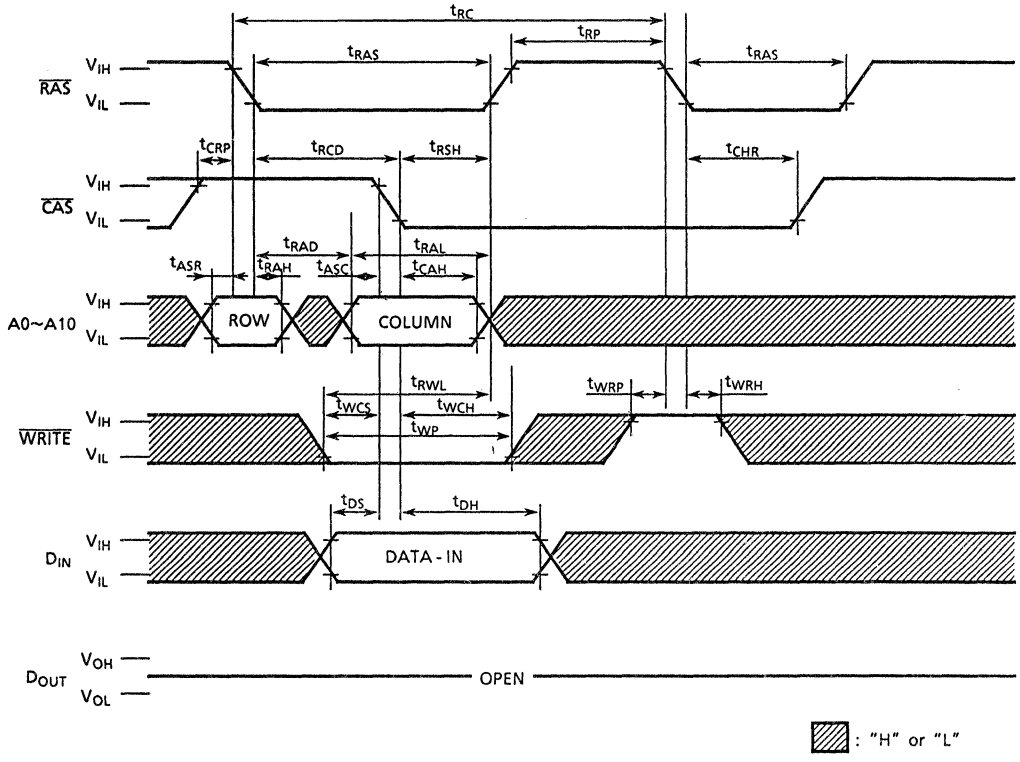


Note: A0~A10="H" or "L" ▨ : "H" or "L"

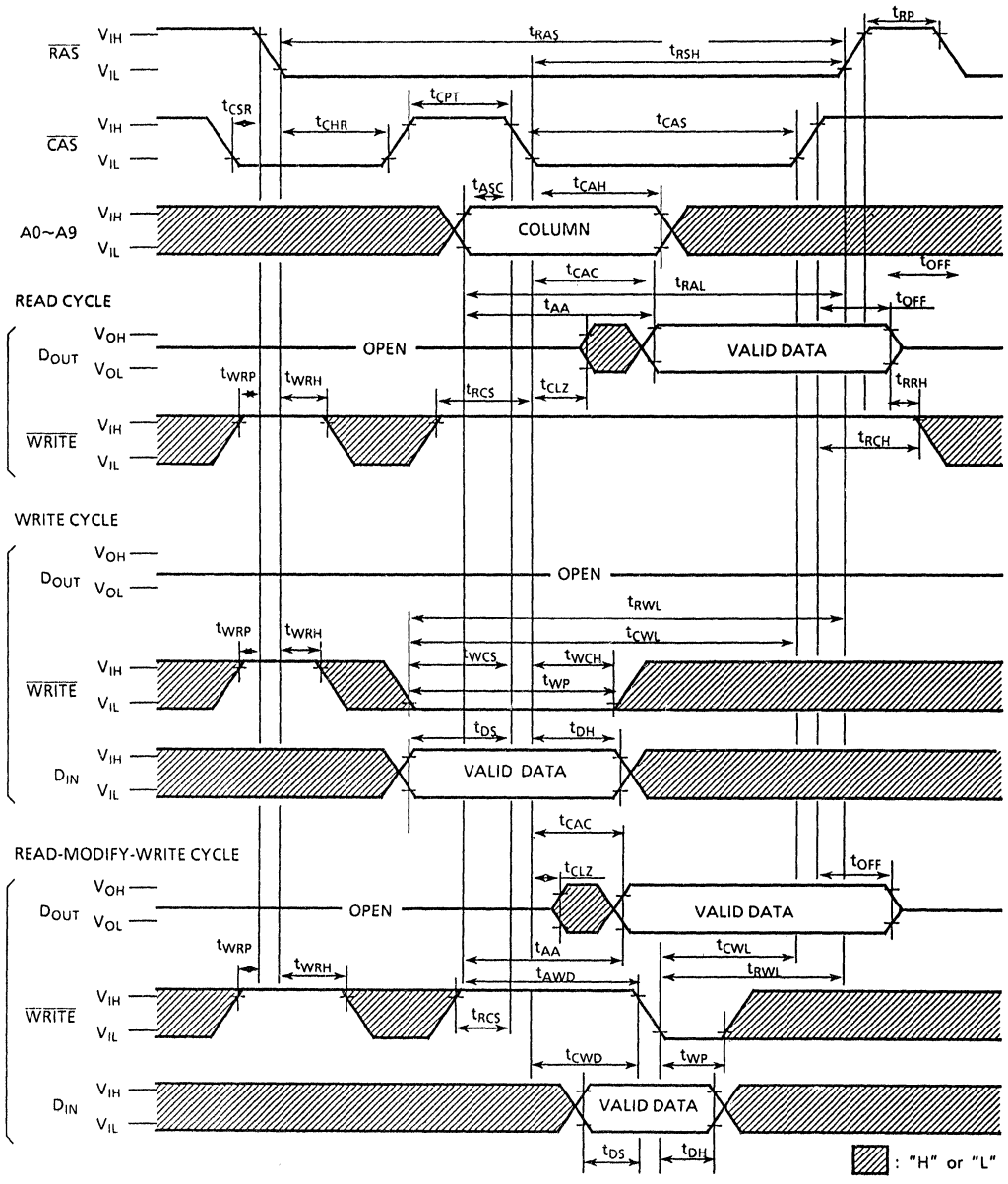
HIDDEN REFRESH CYCLE (READ)



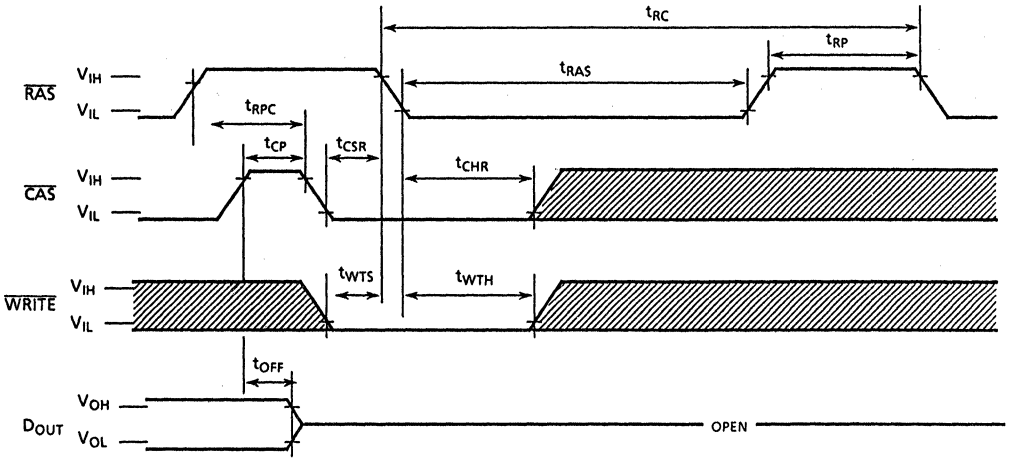
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, CAS BEFORE RAS REFRESH CYCLE



Note: D_{IN}, A0~A10="H" or "L" ▨ : "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 22 address bits required to decode 1 of the 4,194,304 cell locations within the TC514101AP/AJ/ASJ/AZ are multiplexed onto the 11 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 11 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 11 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ While $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the DIN is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle"the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-modify-write and nibble mode write cycles while the "early write"cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

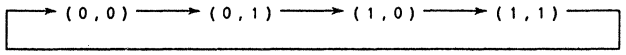
Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC514101AP/AJ/ASJ/AZ is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A10 determines the starting point of the circular 4 bits nibble. Row A10 and column A10 provide the two binary bits needed to select one of four bits.
From then on, successive bits come out in a binary fashion; 00→01→10→11 with A10 row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any conbinations of reads and writes or late writes will be allowed. In addition, the circular wraparound will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

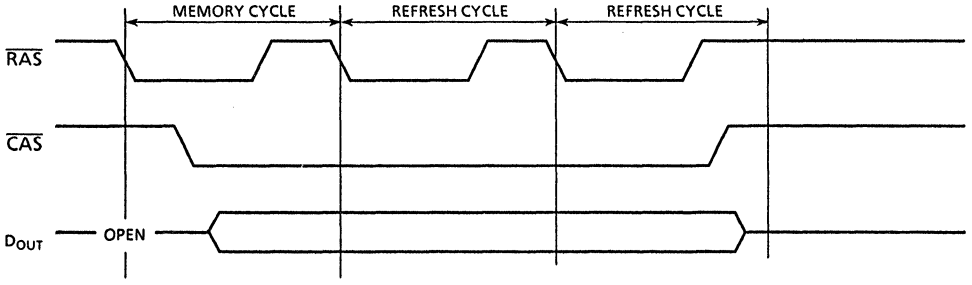
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 1024 row address (A0~A9) within each 16 millisecond time interval.
Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514101AP/AJ/ASJ/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC514101AP/AJ/ASJ/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data avilability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514101AP/AJ/ASJ/AZ can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE) . Repeat this operation 1024 times.

③ Check "1" out of 1024 bits at normal read mode, which was written at ② .

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 1024 times.

⑤ Check "0" out of 1024 bits at normal read mode, which was written at ④ .

⑥ Perform the above ① to ⑤ to the complement data.

TEST MODE

The TC514101AP/AJ/ASJ/AZ is the RAM organized 4,194,304words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or" 0"s), the data output pin indicates a "1". If any of the bits differed, the data outputpin would indcate shows the block diagram of TC514101AP/ASJ/AZ. In"Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or" $\overline{\text{RAS}}$ Only Refresh Cycle"puts it back into "Normal Mode".In the Test Mode, "$\overline{\text{WRITE}}$. $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" functiom reduces test times(1/8 in case of N test pattern)

BLOCK DIAGRAM IN THE TEST MODE

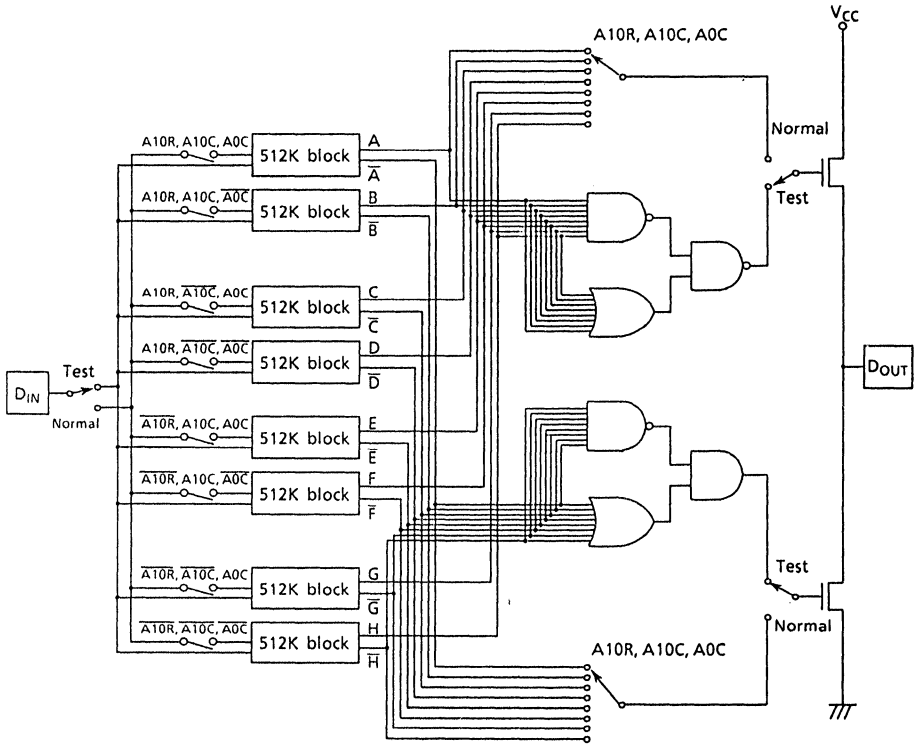


Fig. 1

NOTES

4,194,304 WORD × 1 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514101AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514101AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514101AP/AJ/ASJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The special feature of TC511001AP/AJ/ASJ/AZ is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

FEATURES

- 4,194,304 word by 1bit organization
- Fast access time and cycle time

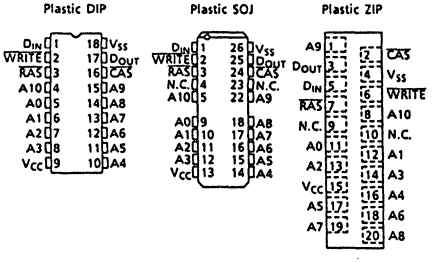
		TC514101AP/AJ/ASJ/AZ-70/80/10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{NCAC}	Nibble Mode Access Time	20ns	20ns	25ns
t_{NC}	Nibble Mode Cycle Time	40ns	40ns	45ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 550mW MAX. Operating (TC514101AP/AJ/ASJ/AZ-70)
  - 468mW MAX. Operating (TC514101AP/AJ/ASJ/AZ-80)
  - 413mW MAX. Operating (TC514101AP/AJ/ASJ/AZ-10)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC514101AP : DIP18-P-300E
  TC514101AJ : SOJ26-P-350
  TC514101ASJ : SOJ26-P-300A
  TC514101AZ : ZIP20-P-400A

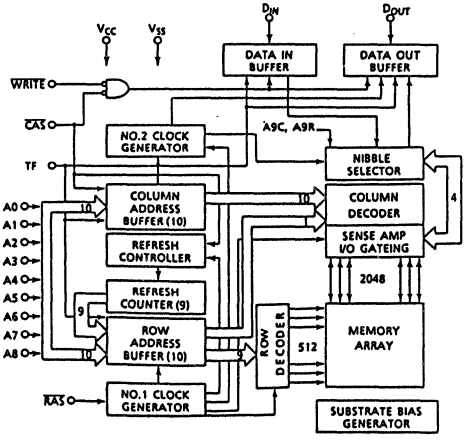
PIN NAMES

A0~A10	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	N.C.	No Connection
$\overline{RAS}$	Row Address Strobe		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514101AP/AJ/ASJ/AZ-70	–	100	mA	3, 4 5
		TC514101AP/AJ/ASJ/AZ-80	–	85		
		TC514101AP/AJ/ASJ/AZ-10	–	75		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514101AP/AJ/ASJ/AZ-70	–	100	mA	3,5
		TC514101AP/AJ/ASJ/AZ-80	–	85		
		TC514101AP/AJ/ASJ/AZ-10	–	75		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Cycling: t_{NC} = t_{NC} MIN.)	TC514101AP/AJ/ASJ/AZ-70	–	70	mA	3, 4 5
		TC514101AP/AJ/ASJ/AZ-80	–	86		
		TC514101AP/AJ/ASJ/AZ-10	–	55		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514101AP/AJ/ASJ/AZ-70	–	100	mA	3,5
		TC514101AP/AJ/ASJ/AZ-80	–	85		
		TC514101AP/AJ/ASJ/AZ-10	–	75		
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514101AP/AJ/ASJ /AZ-70		TC514101AP/AJ/ASJ /AZ-80		TC514101AP/AJ/ASJ /AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	–	175	–	210	–	ns	
t_{NC}	Nibble Mode Cycle Time	40	–	40	–	45	–	ns	
t_{NRMW}	Nibble Mode Read--Modify Write Cycle Time	65	–	65	–	70	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	9,15
t_{NCAC}	Nibble Mode Access Time	–	20	–	20	–	25	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514101AP/ AJ/ASJ/AZ-70		TC514101AP/ AJ/ASJ/AZ-80		TC514101AP/ AJ/ASJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{DH}	Data-In Hold Time	15	–	15	–	20	–	ns	12
t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	20	–	25	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	70	–	80	–	100	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	–	40	–	50	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	40	–	40	–	50	–	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	–	20	–	25	–	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	20	–	25	–	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	–	10	–	10	–	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	–	10	–	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATION CONDITIONS IN THE TEST MODE (Vcc = 5V ± 10%, Ta = 0~70°C) (Note6, 7, 8)

SYMBOL	PARAMETER	TC514101AP/ AJ/ASJ/AZ-70		TC514101AP/ AJ/ASJ/AZ-80		TC514101AP/ AJ/ASJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	155	–	185	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	160	–	180	–	215	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	75	–	85	–	105	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	9,14
t_{AA}	Access Time from Column Address	–	40	–	45	–	55	ns	9,15
t_{RAS}	$\overline{RAS}$ Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	75	–	85	–	105	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	45	–	55	–	ns	
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay Time	25	–	25	–	30	–	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	75	–	85	–	105	–	ns	
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	40	–	45	–	55	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

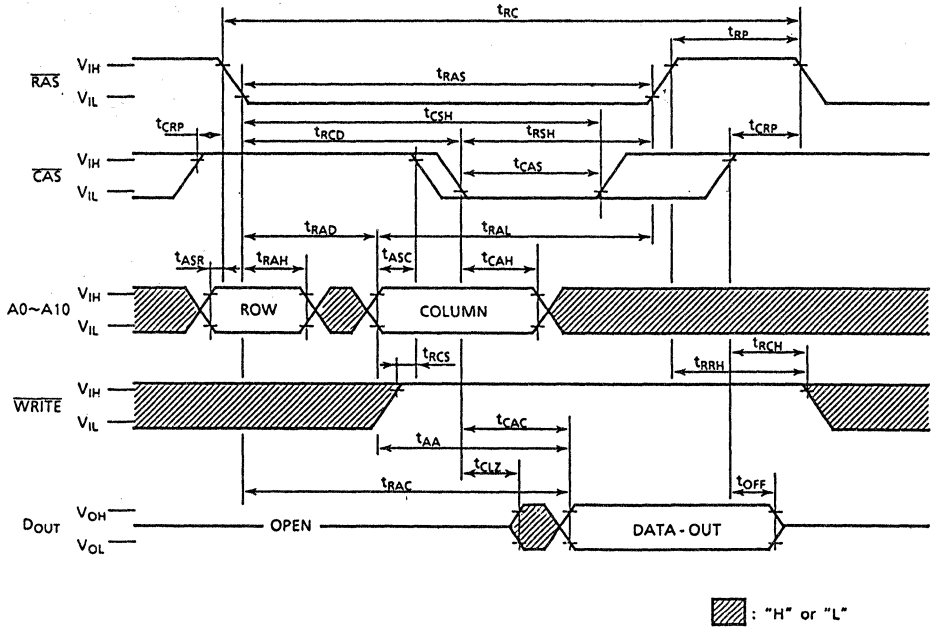
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

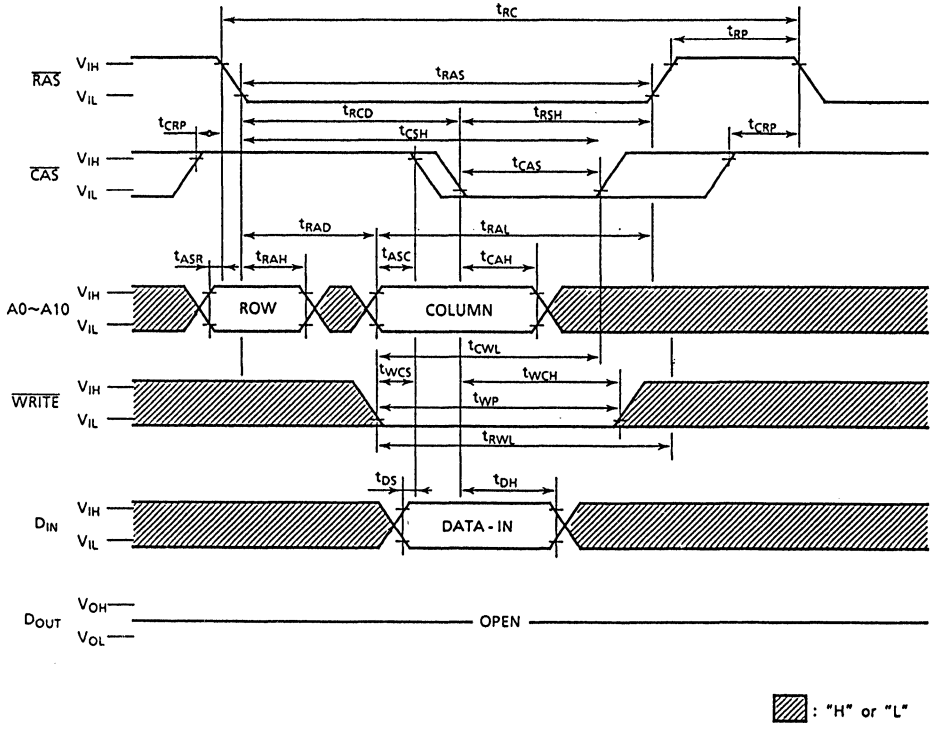
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

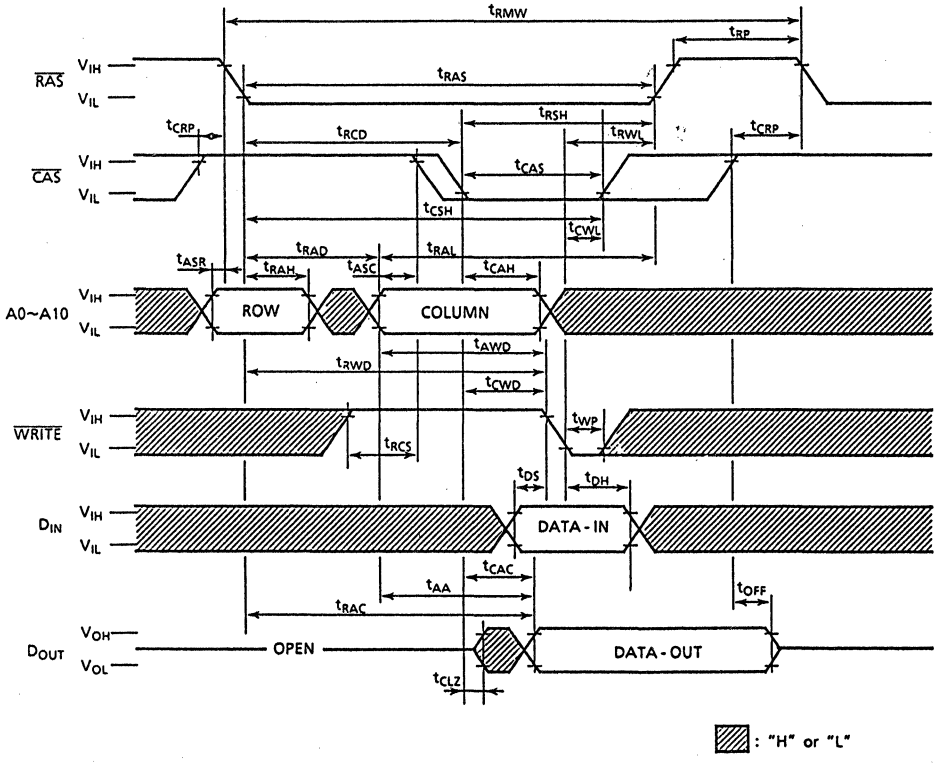
READ CYCLE



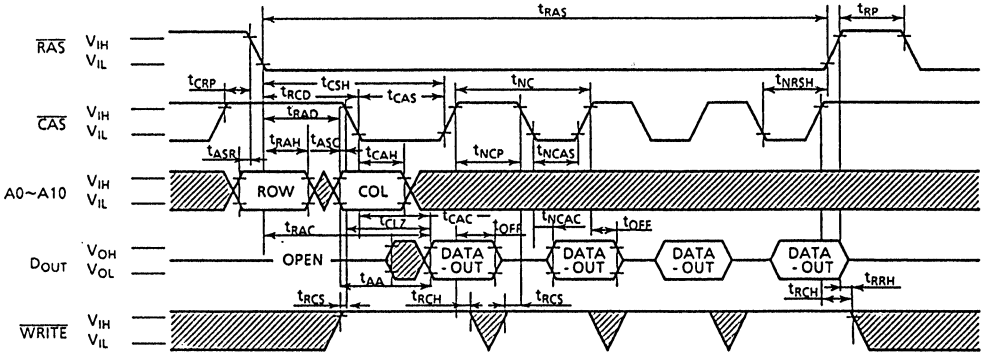
WRITE CYCLE (EARLY WRITE)



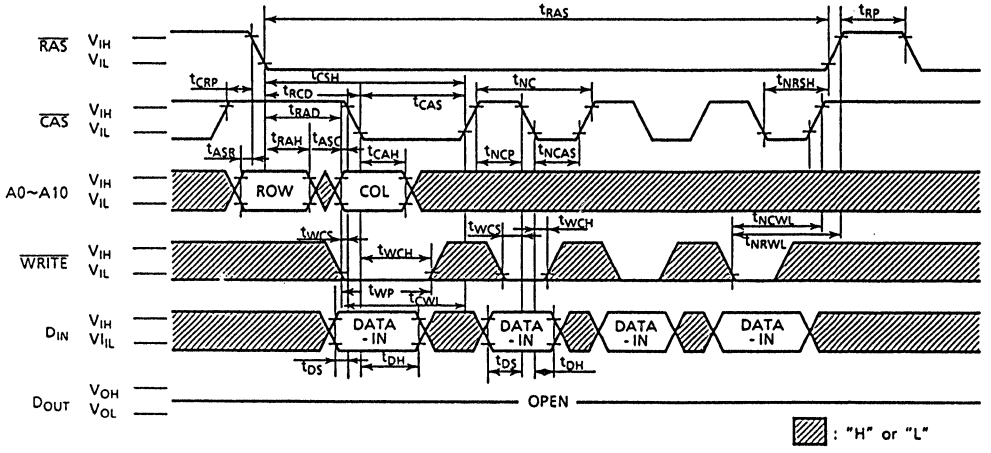
READ-MODIFY-WRITE CYCLE



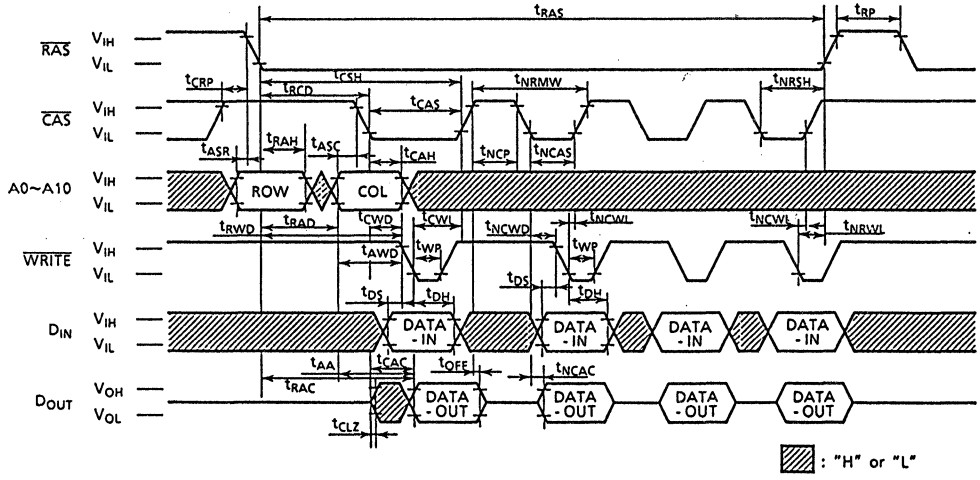
NIBBLE MODE READ CYCLE



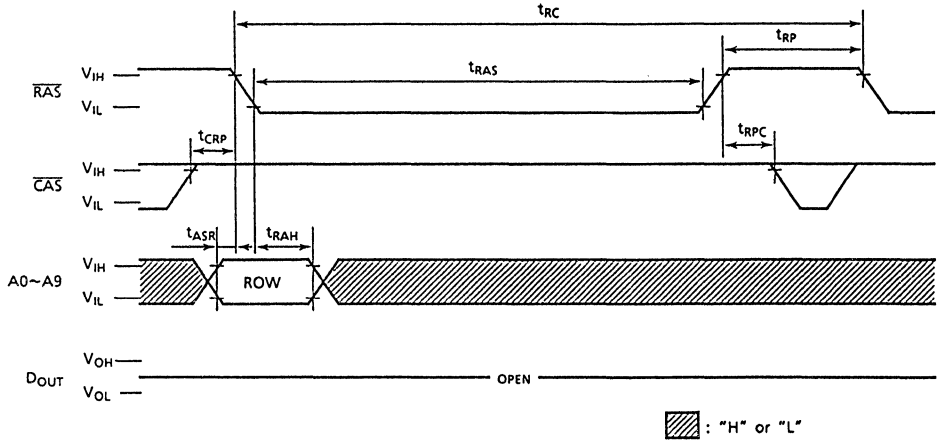
NIBBLE MODE WRITE CYCLE(EARLY WRITE)



NIBBLE MODE READ - MODIFY - WRITE

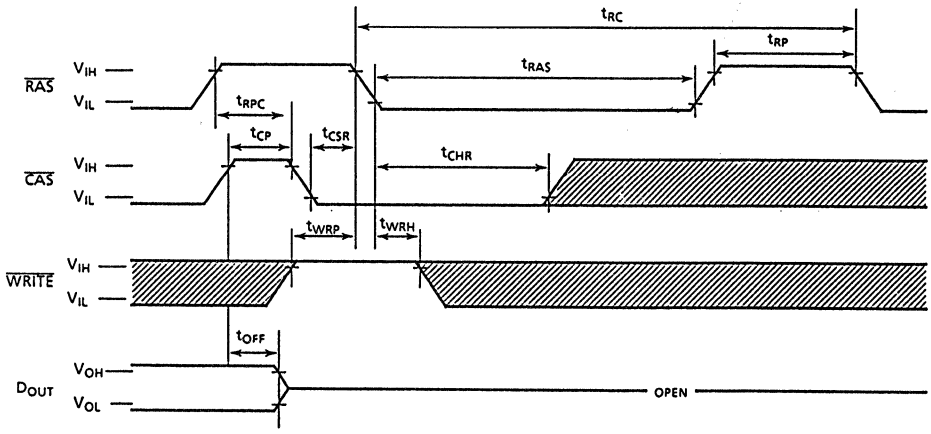


$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



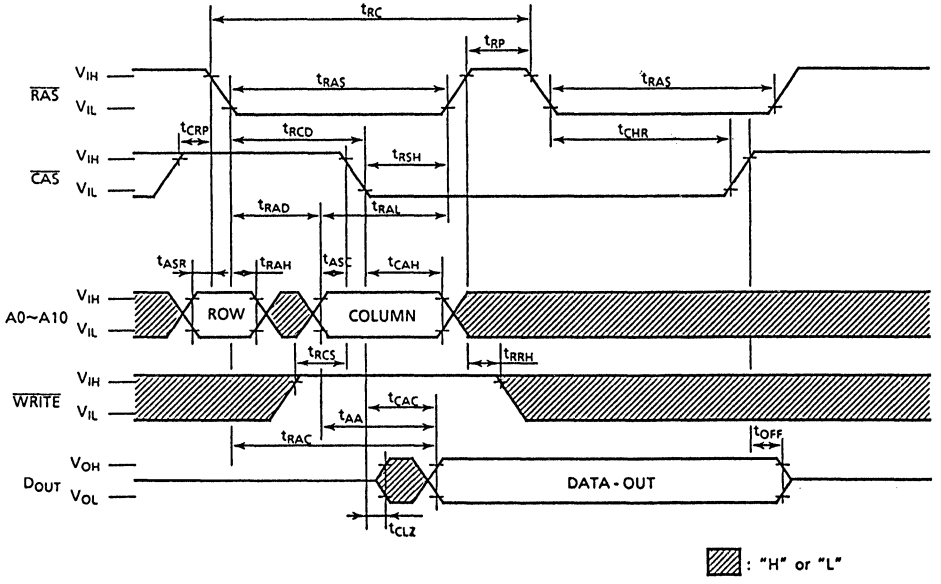
Note: $\overline{\text{WRITE}}$ = "H" or "L" A10 = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

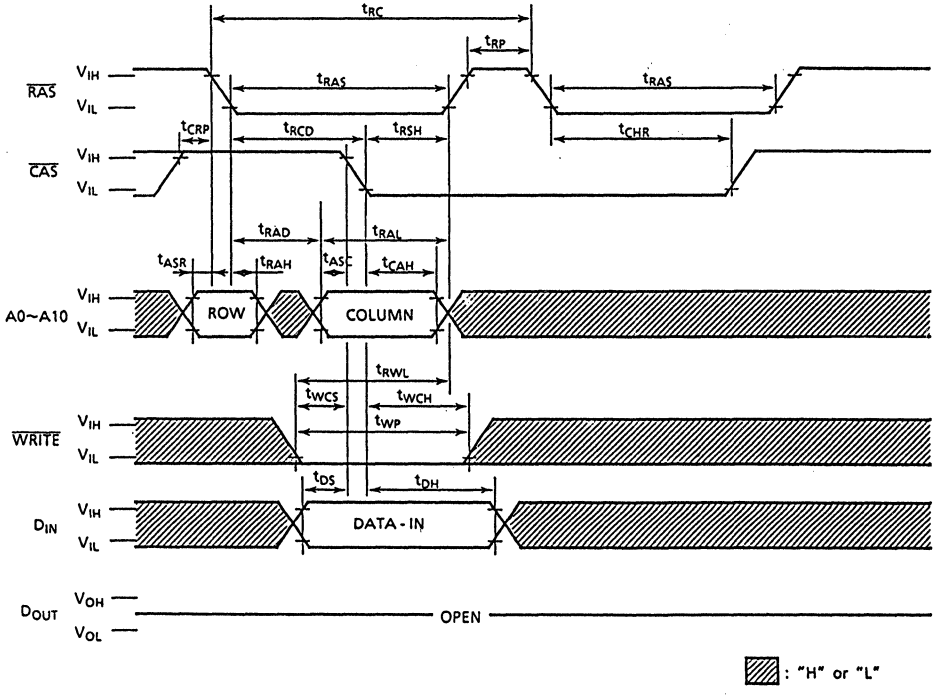


Note: A0~A10="H" or "L" ▨ : "H" or "L"

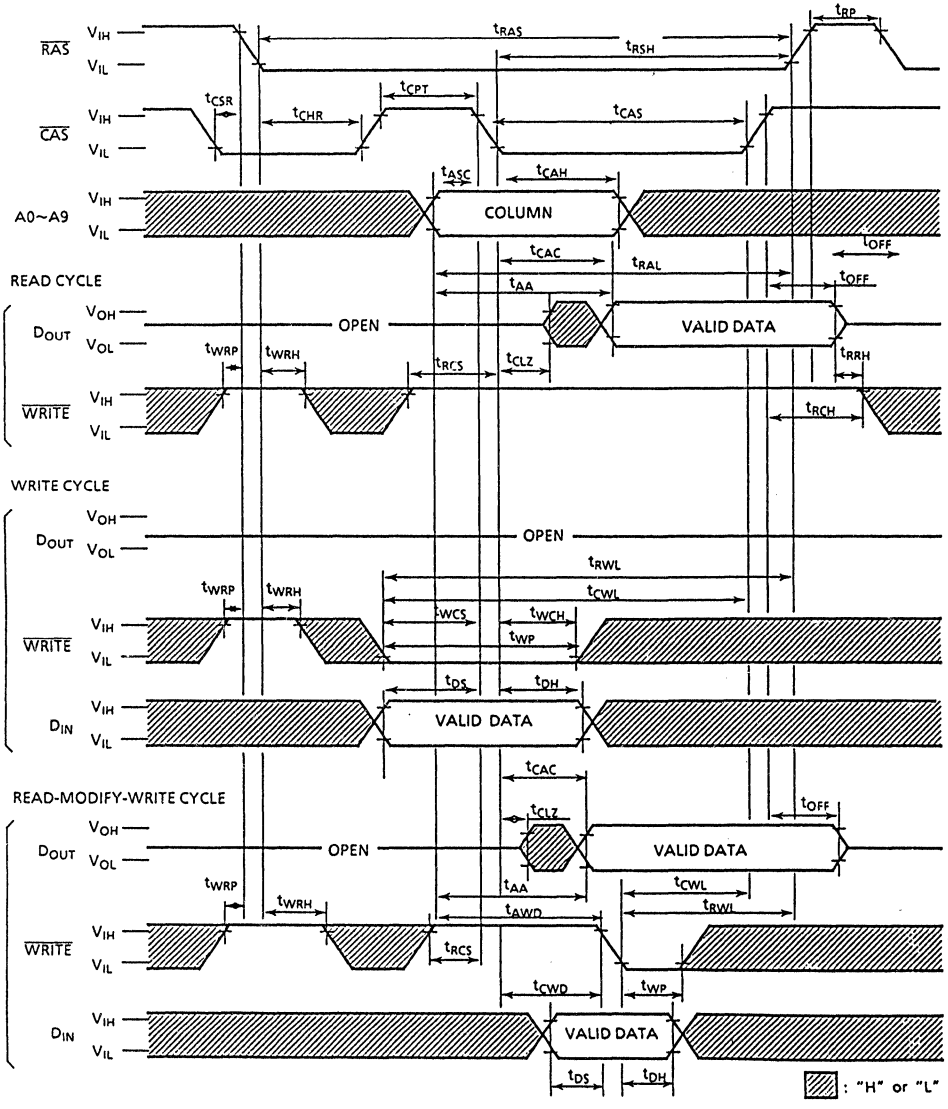
HIDDEN REFRESH CYCLE (READ)



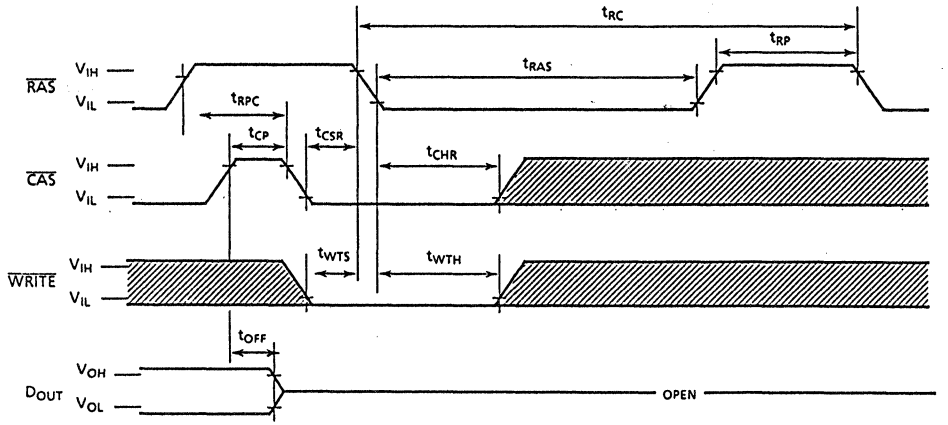
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, A0~A10=“H” or “L” ▨ : “H” or “L”

APPLICATION INFORMATION

ADDRESSING

The 22 address bits required to decode 1 of the 4,194,304 cell locations within the TC514101AP/AJ/ASJ/AZ are multiplexed onto the 11 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 11 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 11 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ While $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the DIN is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle"the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-modify-write and nibble mode write cycles while the "early write"cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

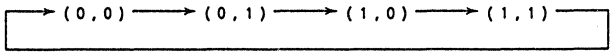
Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC514101AP/AJ/ASJ/AZ is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A10 determines the starting point of the circular 4 bits nibble. Row A10 and column A10 provide the two binary bits needed to select one of four bits.
From then on, successive bits come out in a binary fashion; 00→01→10→11 with A10 row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any conbinations of reads and writes or late writes will be allowed. In addition, the circular wraparound will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

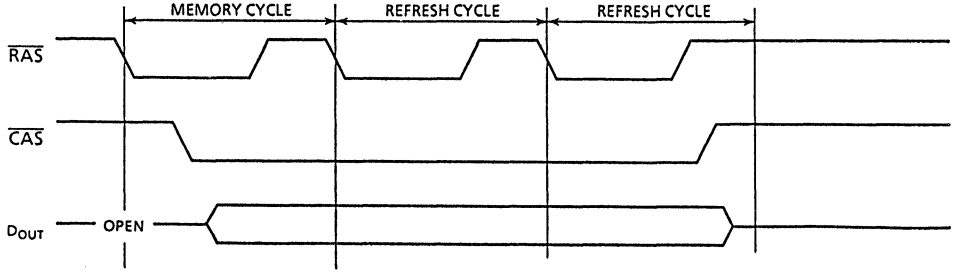
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 1024 row address (A0~A9) within each 16 millisecond time interval.
Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514101AP/AJ/ASJ/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC514101AP/AJ/ASJ/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data avilability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514101AP/AJ/ASJ/AZ can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE) . Repeat this operation 1024 times.

③ Check "1" out of 1024 bits at normal read mode, which was written at ② .

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 1024 times.

⑤ Check "0" out of 1024 bits at normal read mode, which was written at ④ .

⑥ Perform the above ① to ⑤ to the complement data.

TEST MODE

The TC514101AP/AJ/ASJ/AZ is the RAM organized 4,194,304words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or" 0"s), the data output pin indicates a "1". If any of the bits differed, the data outputpin would indcate shows the block diagram of TC514101AP/ASJ/AZ. In"Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or" $\overline{\text{RAS}}$ Only Refresh Cycle"puts it back into "Normal Mode".In the Test Mode, "$\overline{\text{WRITE}}$. $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" functiom reduces test times(1/8 in case of N test pattern)

BLOCK DIAGRAM IN THE TEST MODE

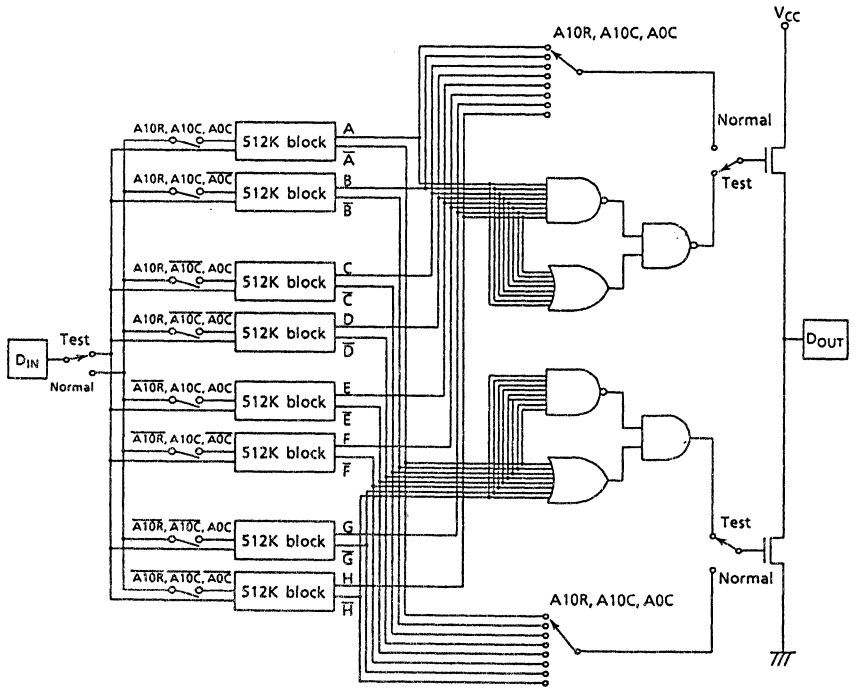


Fig. 1

NOTES

4,194,304 WORD x 1 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514102J/Z is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514102J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514102J/Z to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

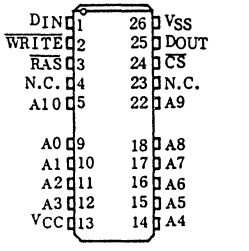
- 4,194,304 word by 1 bit organization
- Fast access time and cycle time

		TC514102J/Z-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{SC}	Static Column Mode Cycle Time	45ns	55ns

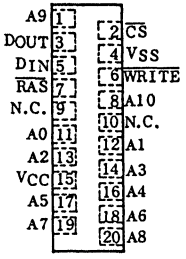
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low power
  550mW Operating (TC514102J/Z-80)
  468mW Operating (TC514102J/Z-10)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and output TTL compatible
- 1024 refresh cycles/16ms
- Package Plastic SOJ: TC514102J
  Plastic ZIP: TC514102Z

PIN CONNECTION (TOP VIEW)

Plastic SOJ



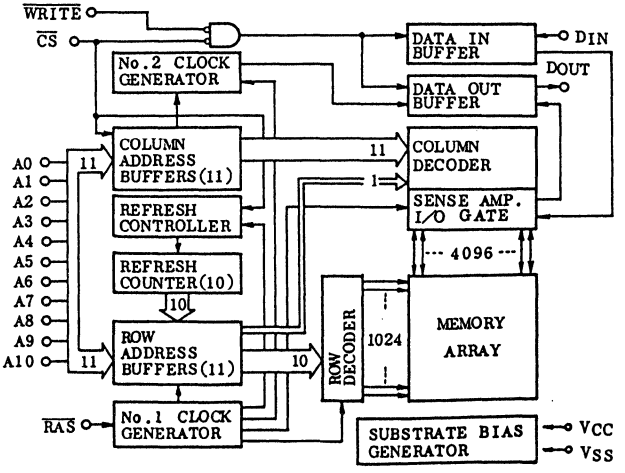
Plastic ZIP



PIN NAMES

A0 ∿ A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CS}$	Chip Select Input
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	-1 ~ 7	V	1
Output Voltage	V_{OUT}	-1 ~ 7	V	1
Power Supply Voltage	V_{CC}	-1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	-55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C·sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514102J/Z-80	-	100	mA	3,4,5
		TC514102J/Z-10	-	85		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514102J/Z-80	-	100	mA	3,5
		TC514102J/Z-10	-	85		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	TC514102J/Z-80	-	75	mA	3,4,5
		TC514102J/Z-10	-	65		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514102J/Z-80	-	100	mA	3
		TC514102J/Z-10	-	85		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{I(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514102J/Z -80		TC514102J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	175	-	210	-	ns	
t_{SC}	Static Column Mode Cycle Time	45	-	55	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	80	-	100	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	40	-	50	ns	9,15
t_{ALW}	Access Time from Last Write	-	75	-	95	ns	9,16
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	25	-	30	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CS}$ Hold Time	80	-	100	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	200,000	25	200,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	10	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	90	-	115	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514102J/Z -80		TC514102J/Z -10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{WI}	Write Command Inactive Time	10	-	10	-	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	-	10	-	ns	17
t_{LWAD}	Last Write to Column Address Delay Time	20	35	25	45	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	75	-	95	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	20	-	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time	20	-	25	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80	-	100	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	40	-	50	-	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514102J/Z -80		TC514102J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	155	-	185	-	ns	
t_{SC}	Static Column Mode Cycle Time	50	-	60	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	105	ns	9,14,15
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	30	ns	9,14
t_{AA}	Access Time from Column Address	-	45	-	55	ns	9,15
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	105	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CS}$ Hold Time	85	-	105	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	200,000	30	200,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

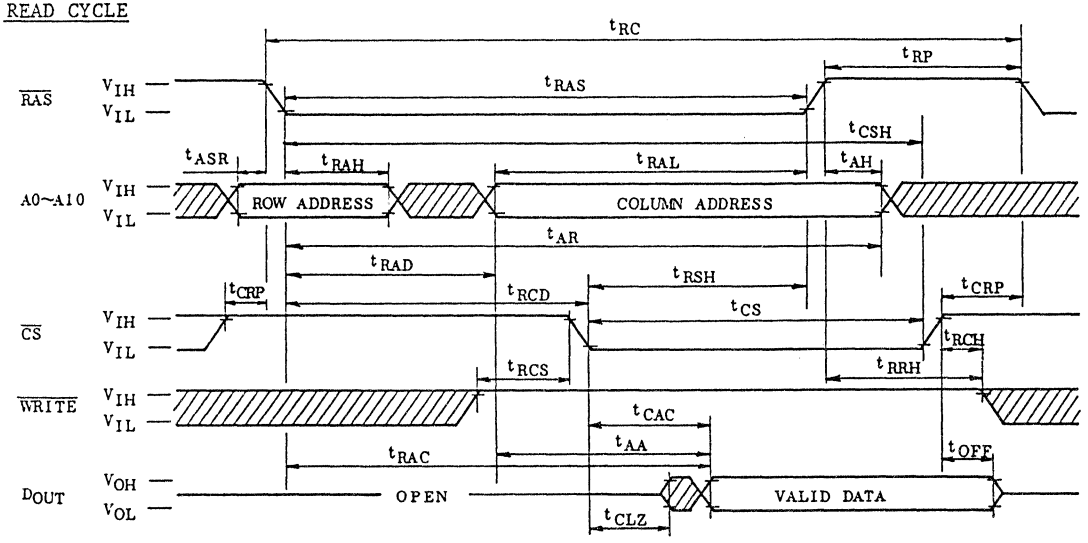
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

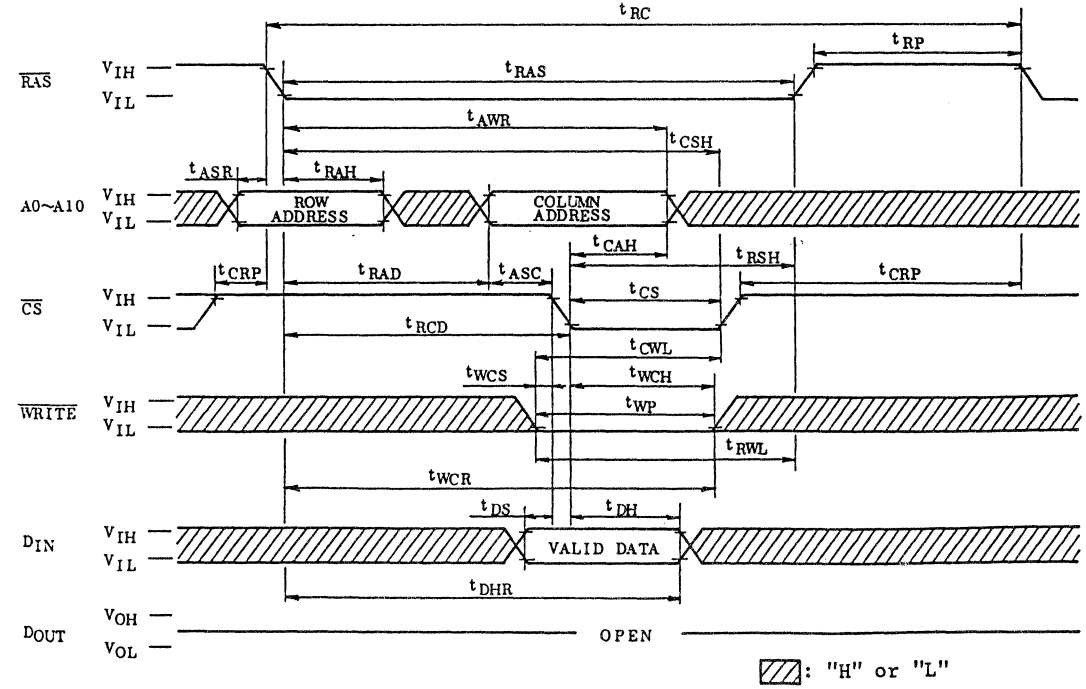
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$.
6. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved.
   In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
17. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

TIMING WAVEFORMS

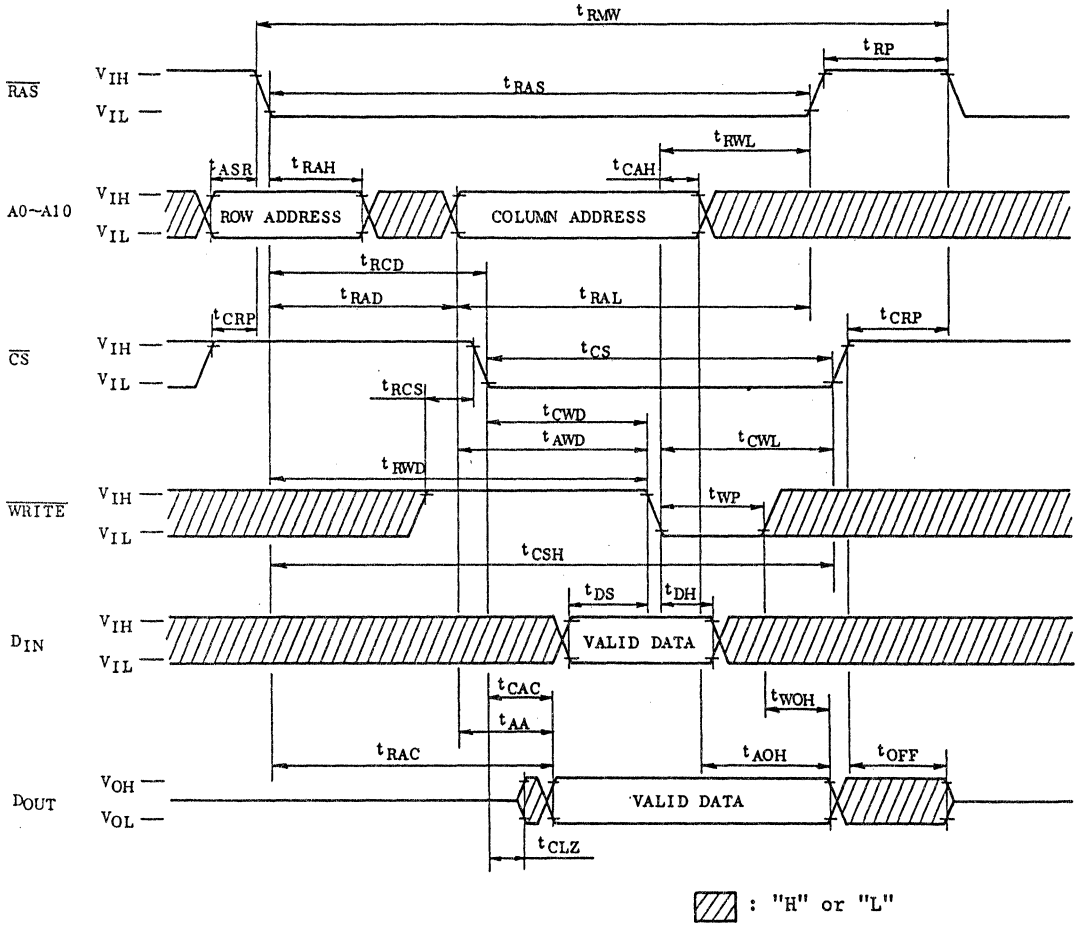
READ CYCLE



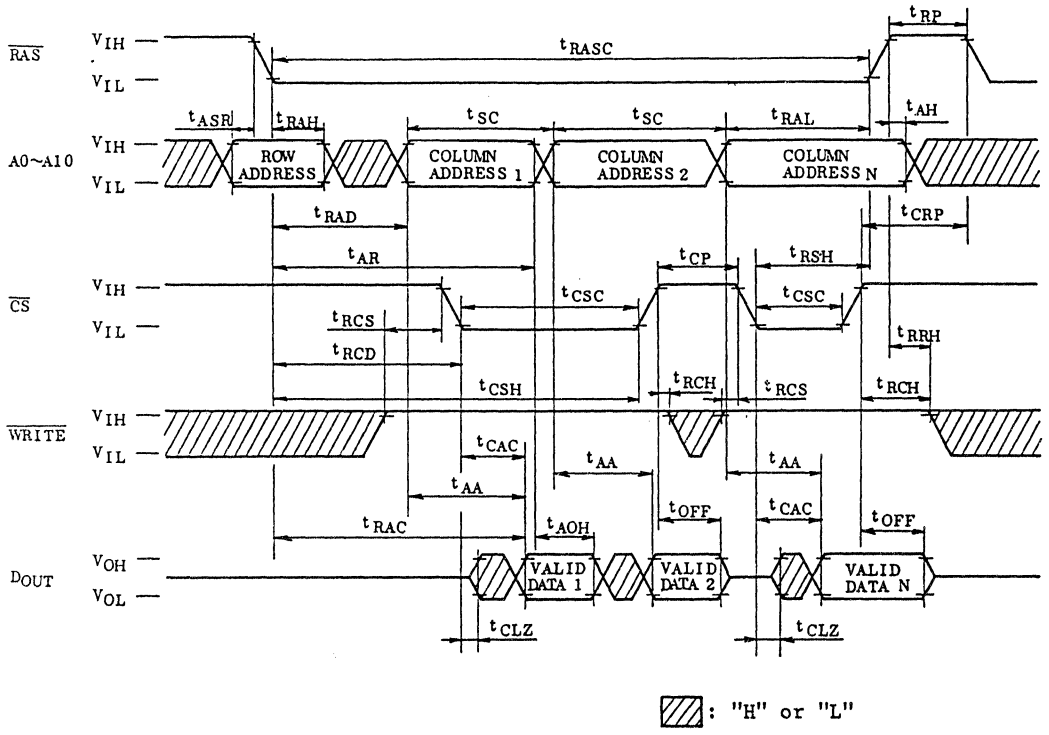
WRITE CYLCE (EARLY WRITE)



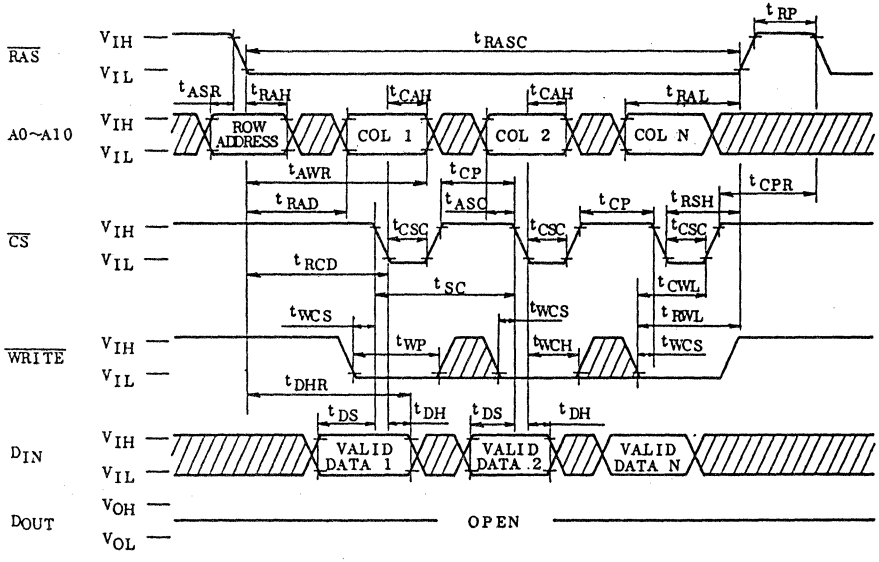
READ-MODIFY-WRITE CYCLE



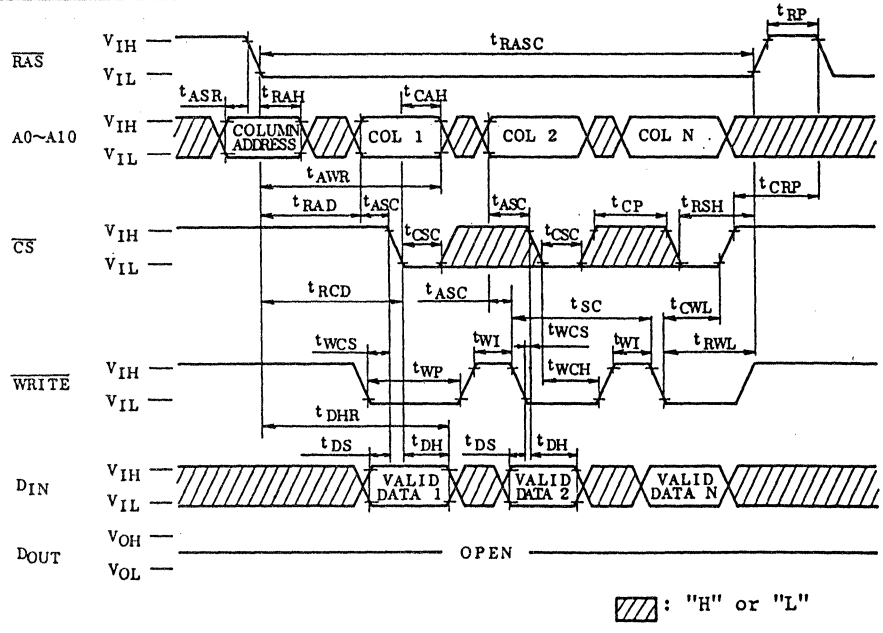
STATIC COLUMN MODE READ CYCLE



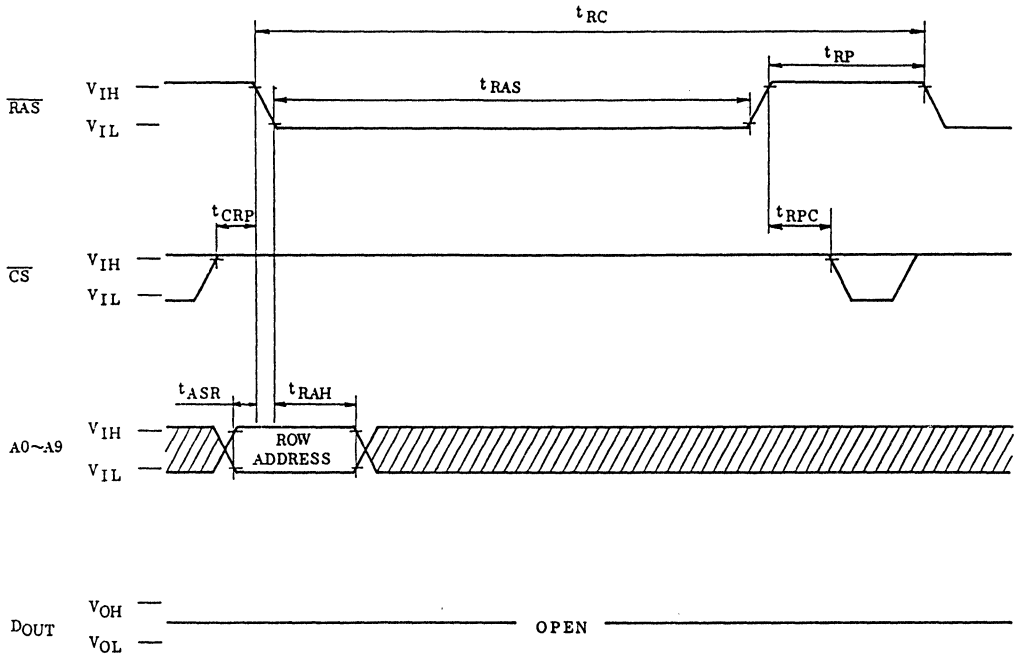
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



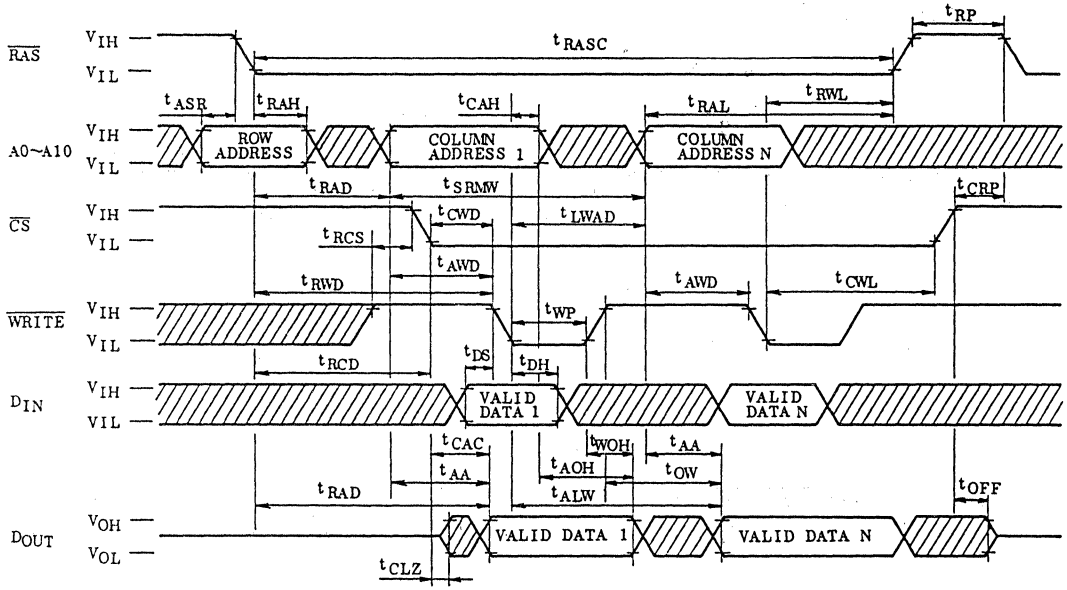
$\overline{RAS}$ ONLY REFRESH CYCLE



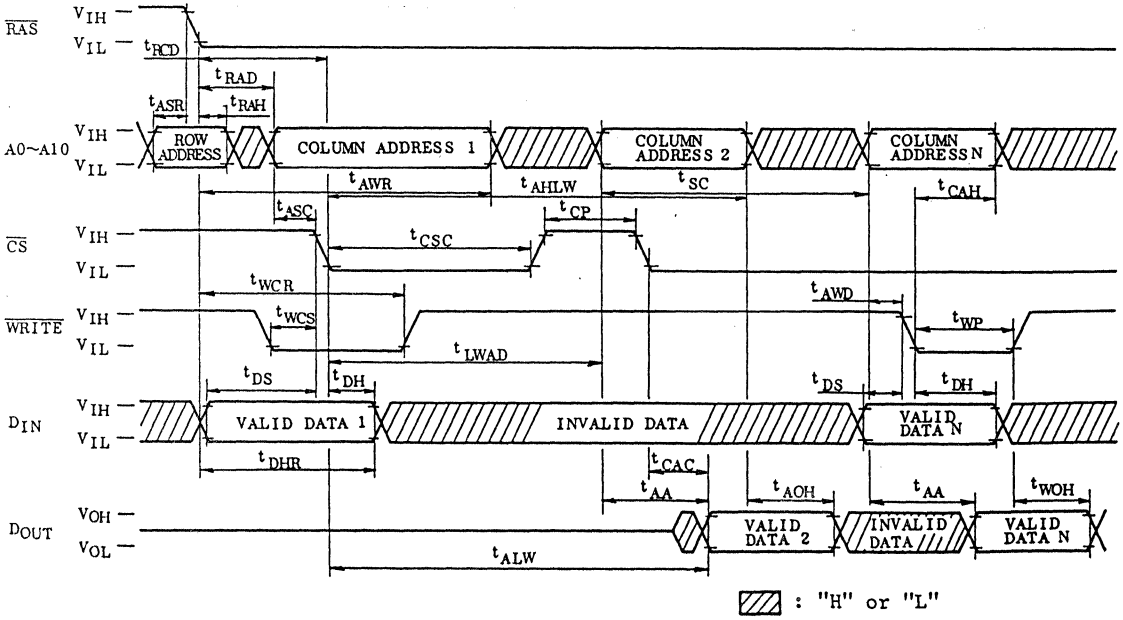
▨: "H" or "L"

NOTE: $\overline{WRITE}$="H" or "L", A10="H" or "L"

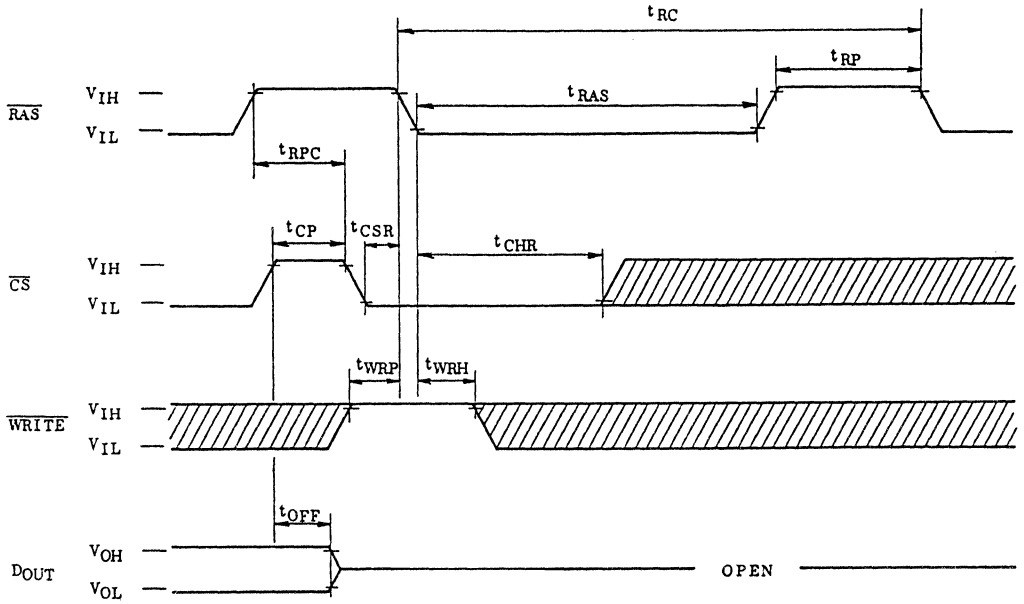
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE



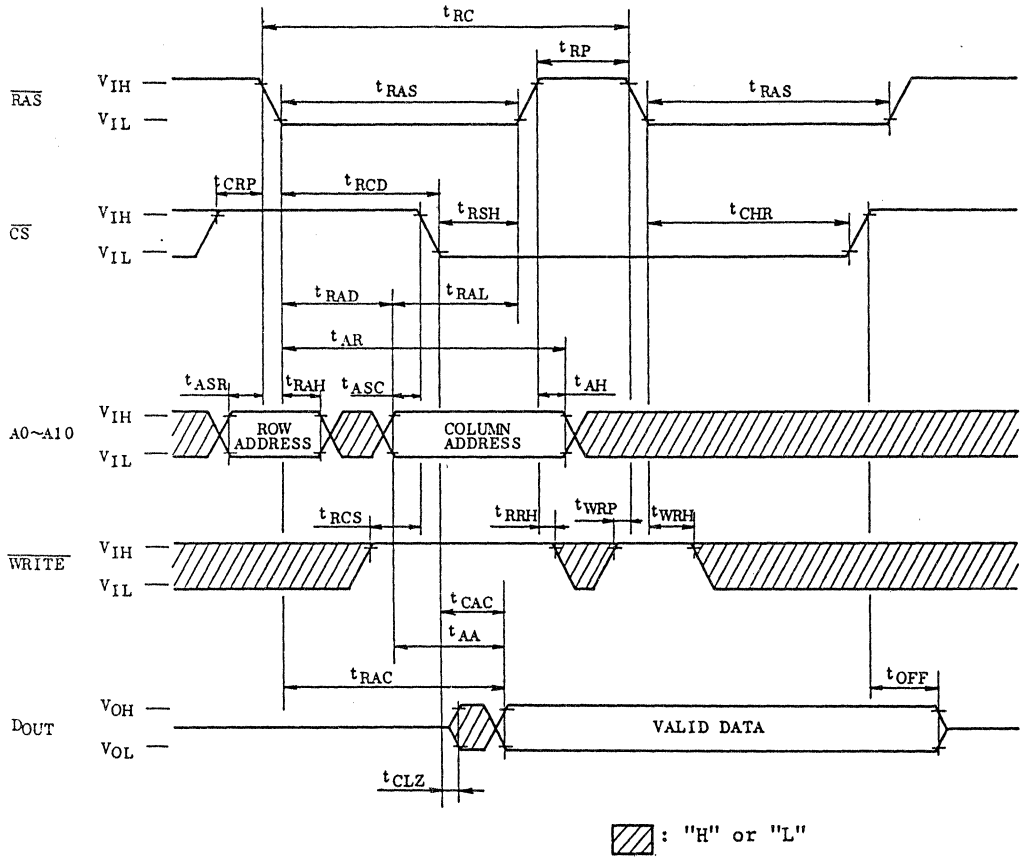
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



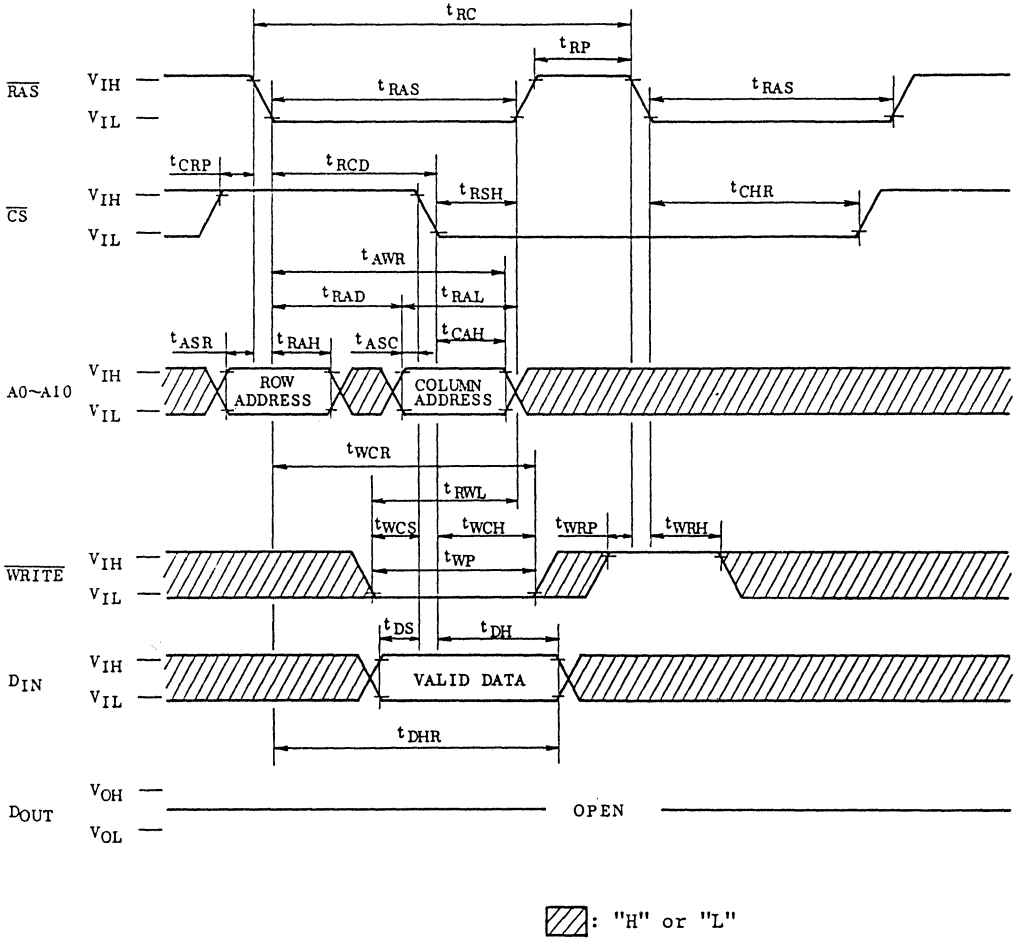
NOTE: A0 ∿ A10="H" or "L"

▨ : "H" or "L"

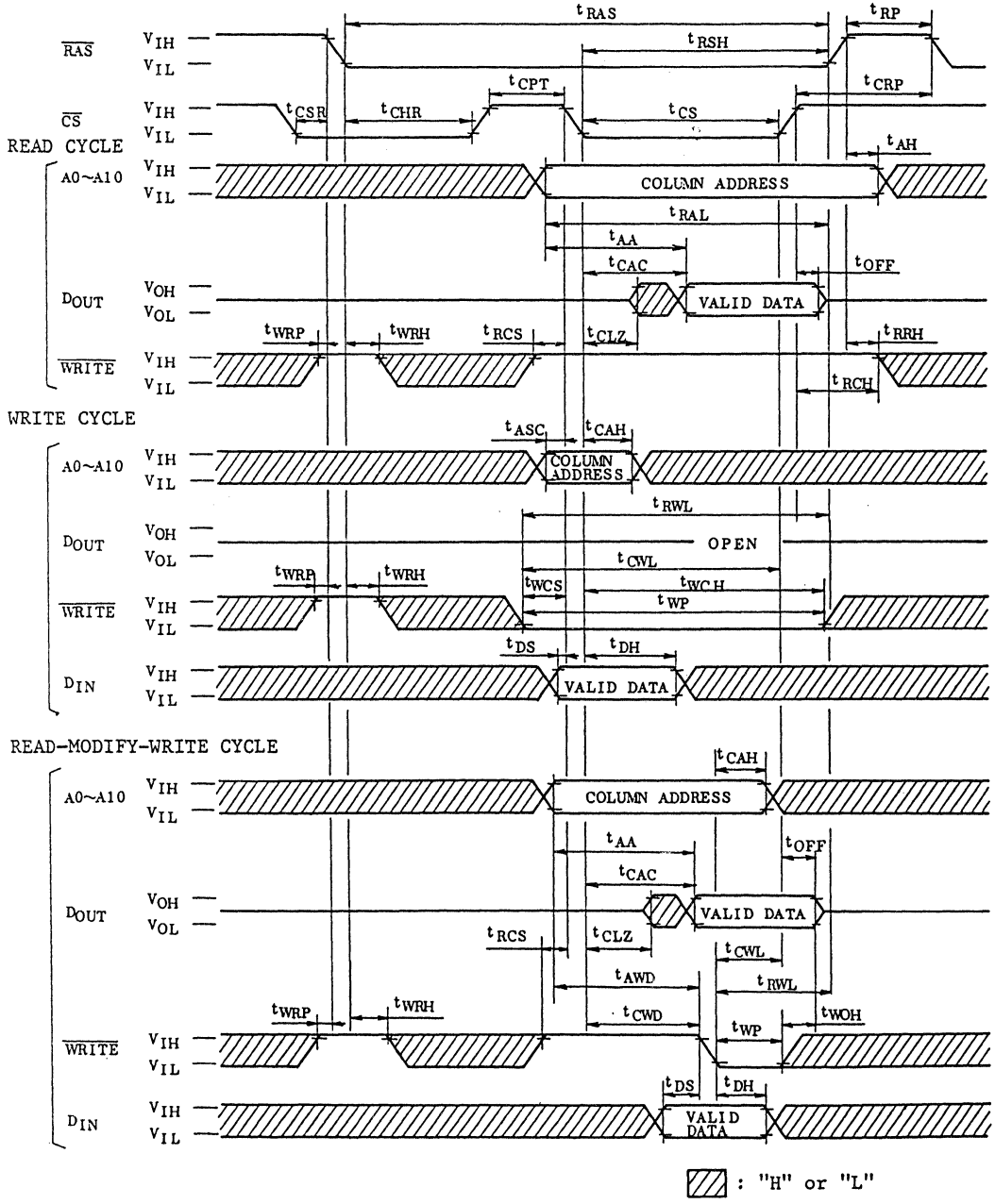
HIDDEN REFRESH CYCLE (READ)



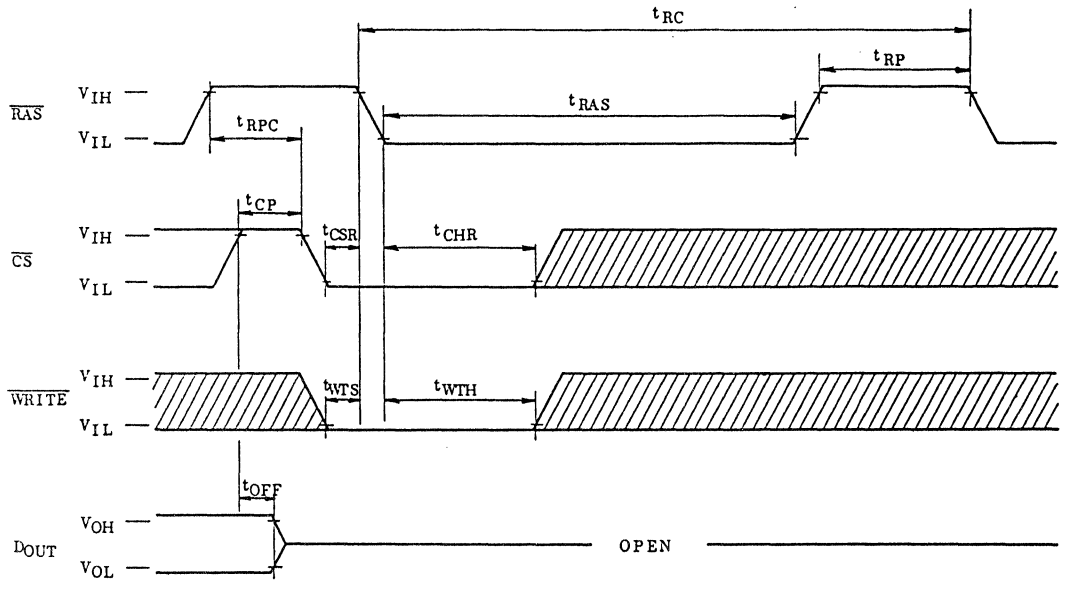
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



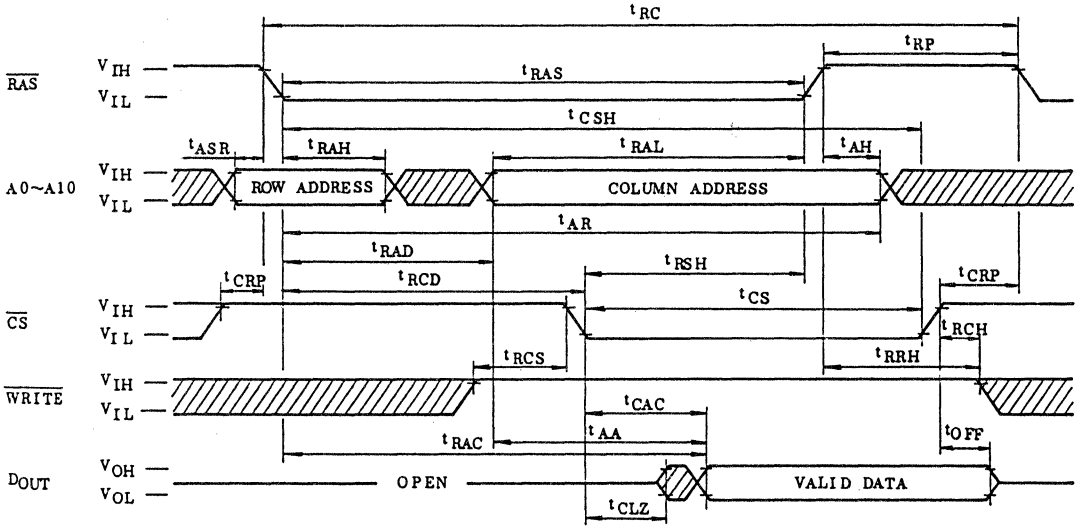
WRITE, $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



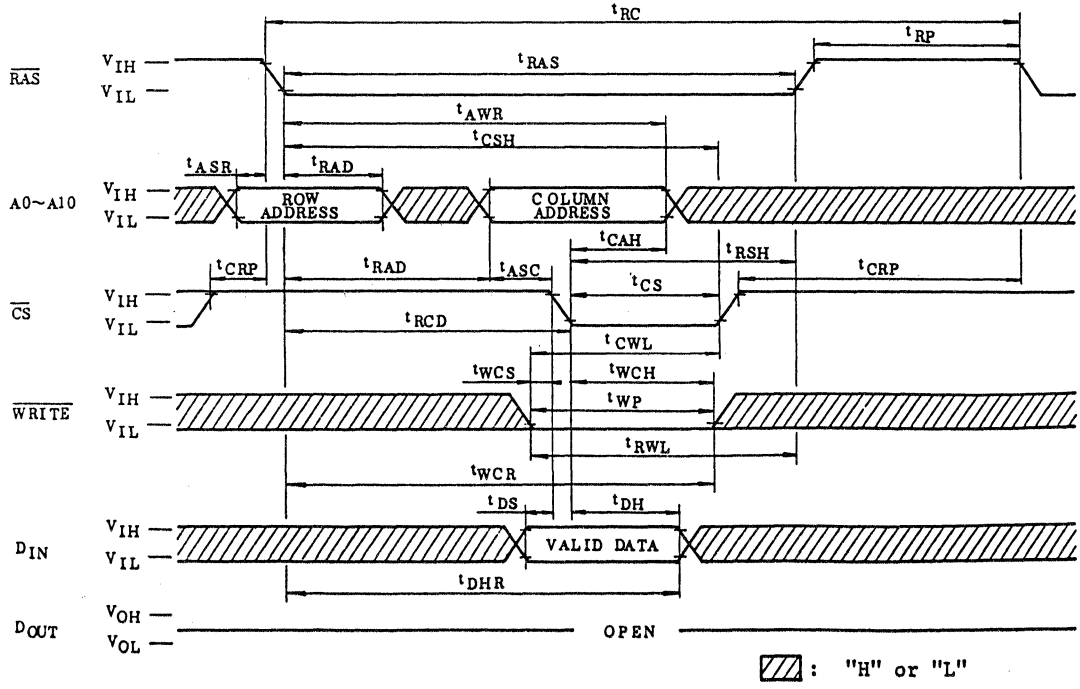
NOTE: D_{IN}, A0 ∿ A10: "H" or "L"

▨ : "H" or "L"

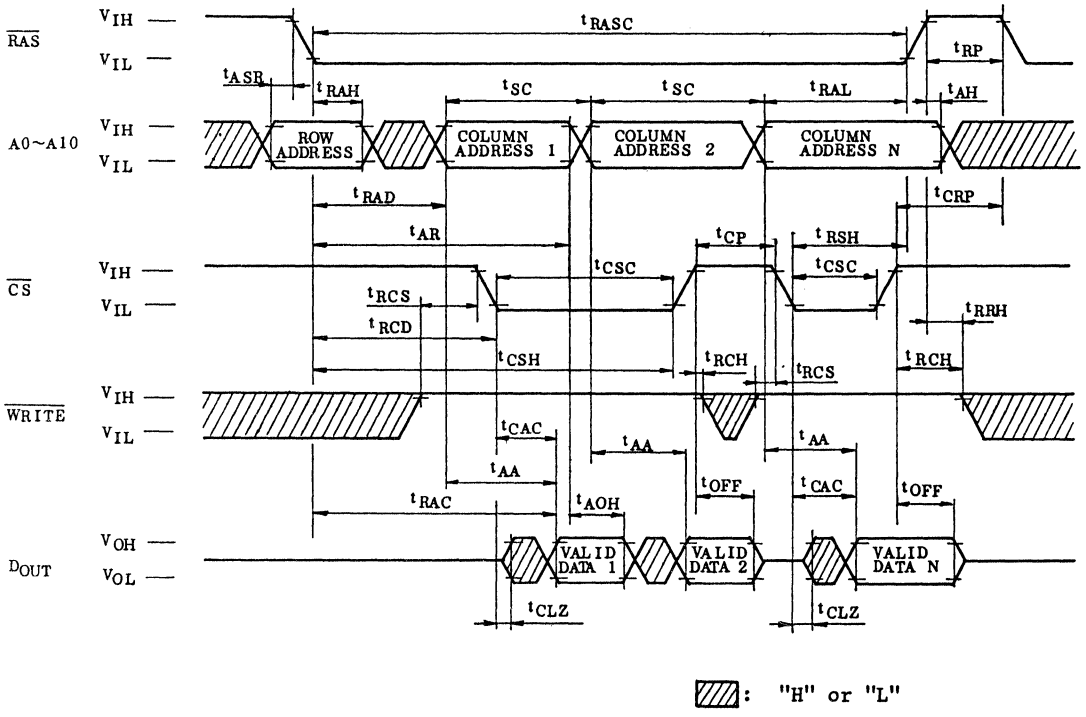
READ CYCLE IN THE TEST MODE



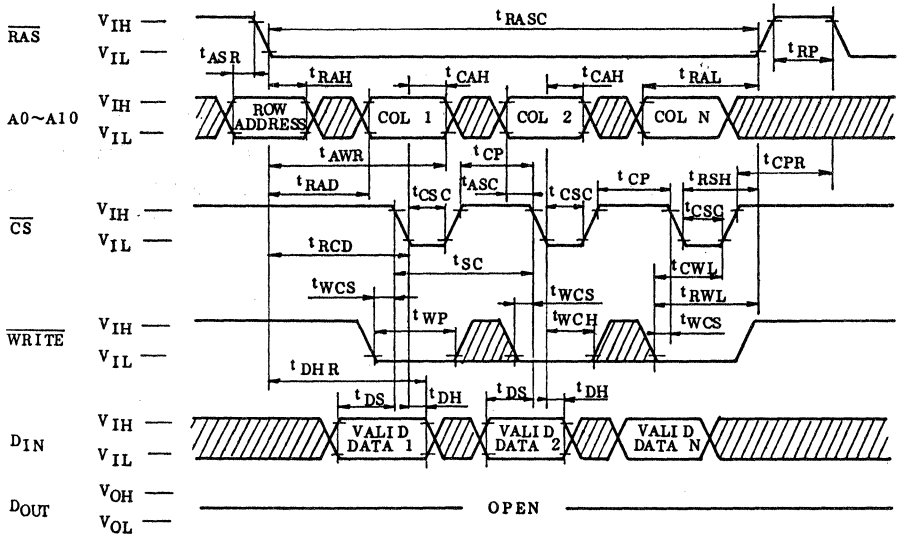
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



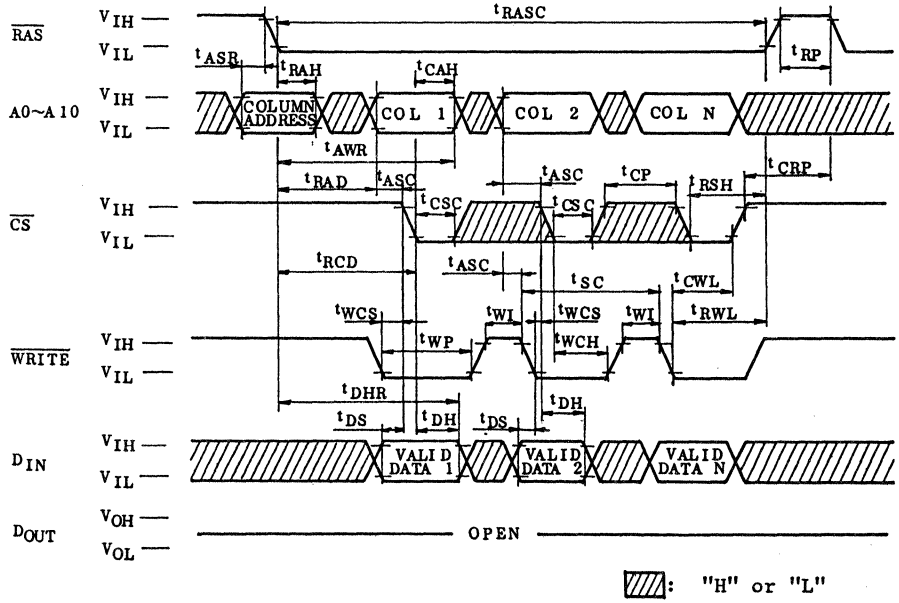
STATIC COLUMN MODE READ CYCLE IN THE TEST MODE



STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



TEST MODE

The TC514102J/Z is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig. 1 shows the block diagram of TC514102J/Z. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

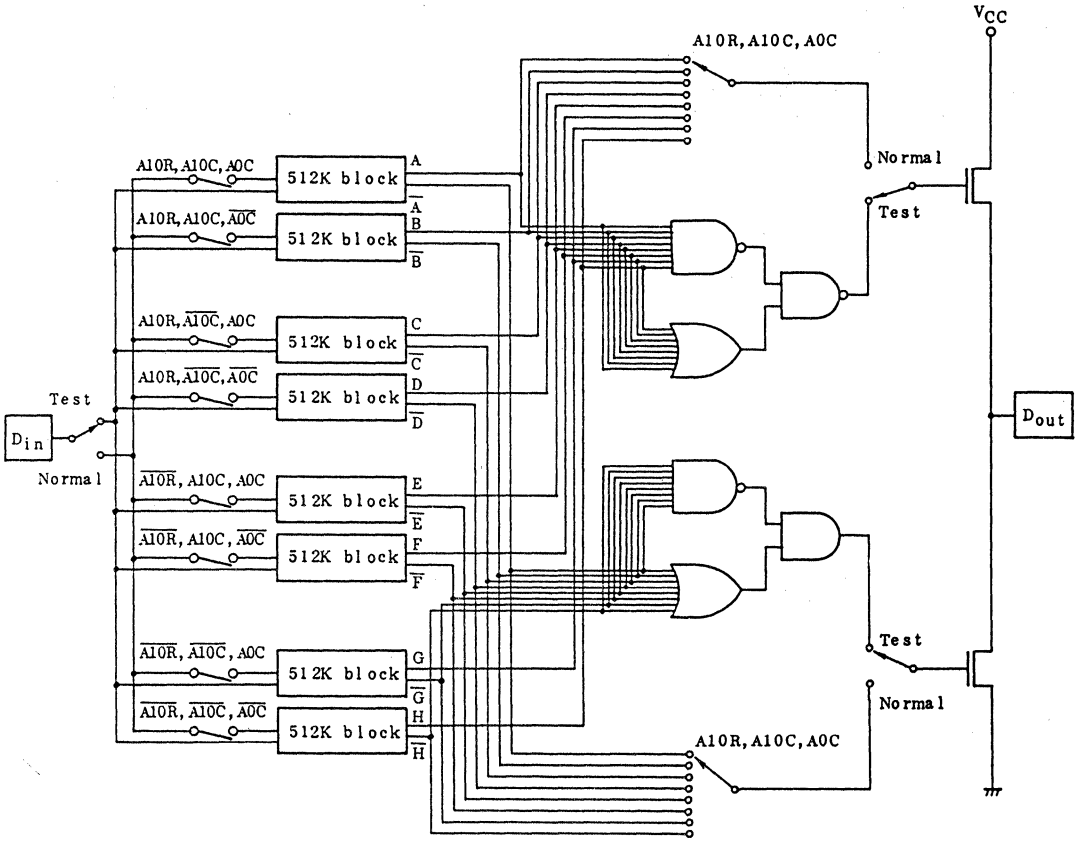


Fig. 1

4,194,304 WORD × 1 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514102AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514102AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514102AP/AJ/ASJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 1bit organization
- Fast access time and cycle time

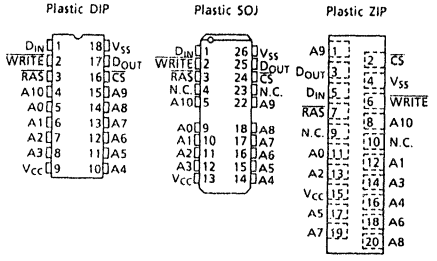
		TC514102AP/AJ/ASJ/AZ-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{SC}	Static Column Mode Cycle Time	35ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  660mW MAX. Operating
  (TC514102AP/AJ/ASJ/AZ-60)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1,024 refresh cycles/16ms
- Package TC514102AP : DIP18-P-300E
  TC514102AJ : SOJ26-P-350
  TC514102ASJ : SOJ26-P-300A
  TC514102AZ : ZIP20-P-400A

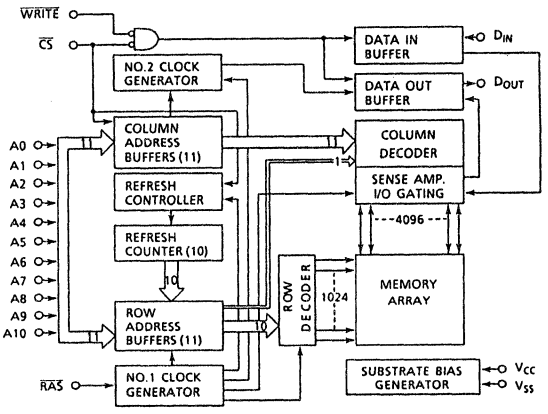
PIN NAMES

A0~A10	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	N.C.	No Connection
$\overline{CS}$	Chip Select Input		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514102AP/AJ/ASJ/AZ-60	–	120	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC514102AP/AJ/ASJ/AZ-60	–	120	mA	3, 5
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS} = \overline{CS}$ = VIL, Address Cycling: tSC = tSC MIN.)	TC514102AP/AJ/ASJ/AZ-60	–	85	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514102AP/AJ/ASJ/AZ-60	–	120	mA	3, 5
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IH} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ + 5.5V)		– 10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514102AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	135	–	ns	
t_{SC}	Static Column Mode Cycle Time	35	–	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	9, 14 15
t_{CAC}	Access Time from $\overline{CS}$	–	20	ns	9, 14
t_{AA}	Access Time from Column Address	–	30	ns	9, 15
t_{ALW}	Access Time from Last Write	–	55	ns	9, 16
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	–	ns	9
t_{OFF}	Output Buffer Turn-Off Delay	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Address	5	–	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	–	20	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	–	ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	60	200,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	60	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	200,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514102AP/AJ/ASJ/AZ-60		UNITS	NOTES
		MIN.	MAX.		
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$ (READ CYCLE)	70	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	–	ns	17
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	–	ns	
t_{LWAD}	Last Write to Column Address Delay Time	20	25	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	55	–	ns	
t_{RCS}	Read Command Set-up Time referenced to $\overline{CS}$	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	ns	13
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{WI}	Write Command Inactive Time	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	ns	12
t_{DH}	Data-In Hold Time	15	–	ns	12
t_{REF}	Refresh Period	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	20	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	60	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	–	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	5	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	15	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	–	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	30	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514102AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{WTS}	Write Command Set-Up Time	10	–	ns	
t_{WTH}	Write Command Hold Time	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATION CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%, Ta = 0~70°C) (Note6, 7, 8)

SYMBOL	PARAMETER	TC514102AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	115	–	ns	
t_{SC}	Static Column Mode Cycle Time	40	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	65	ns	9,14 15
t_{CAC}	Access Time from $\overline{CS}$	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	ns	9,15
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	75	20,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	ns	
t_{CSH}	$\overline{CS}$ Hold Time	65	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	20,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

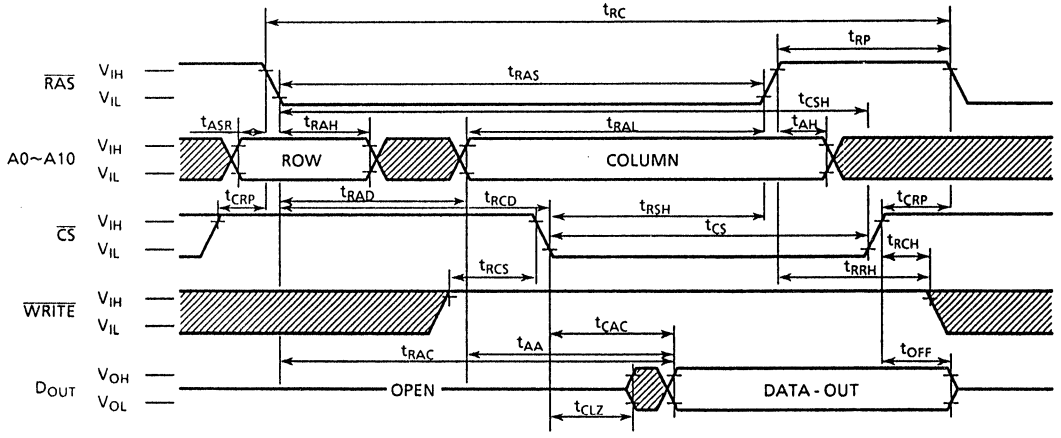
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$)	–	7	pF
C_O	Output Capacitance (D_{OUT})	–	7	pF

NOTES:

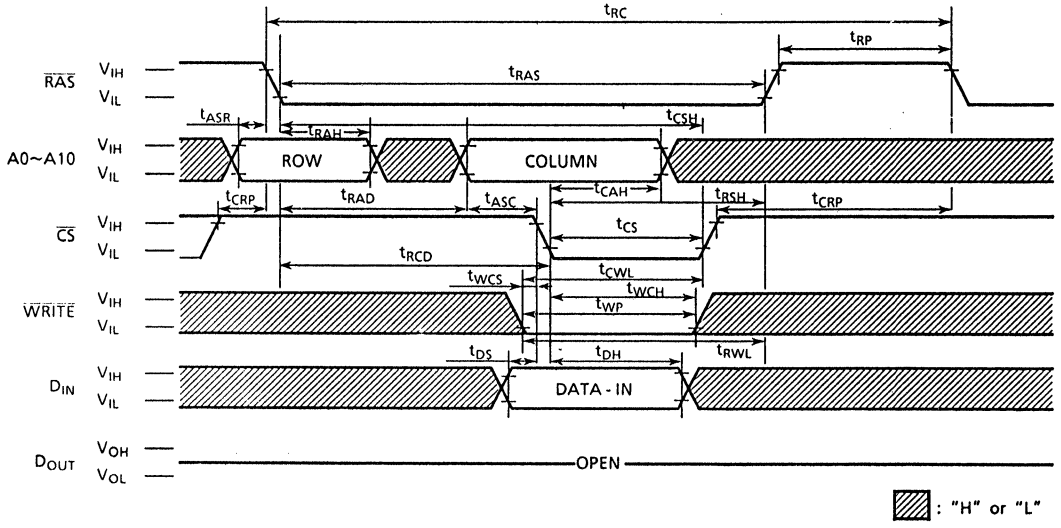
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$.
6. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refreh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (min.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
16. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met.
    t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
17. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

TIMING WAVEFORMS

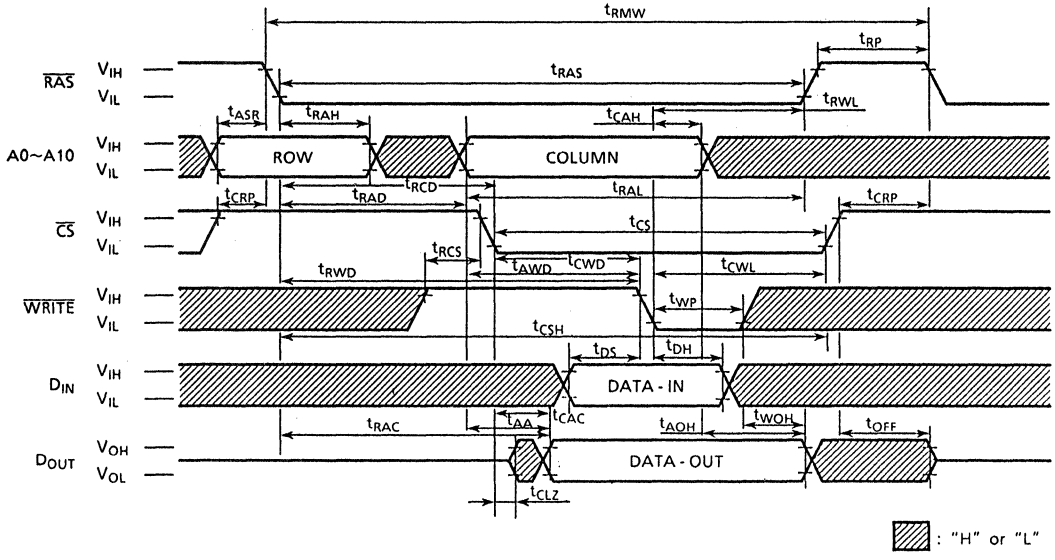
READ CYCLE



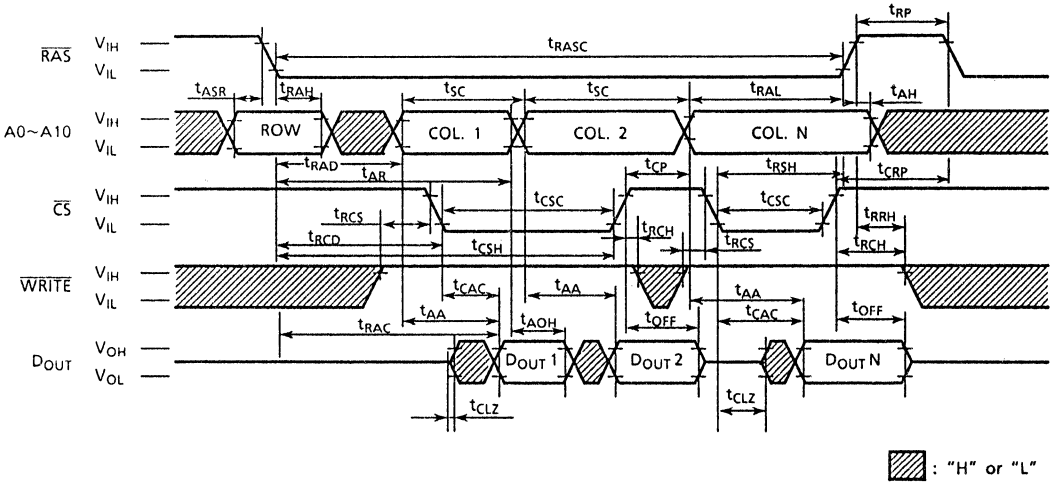
WRITE CYCLE (EARLY WRITE)



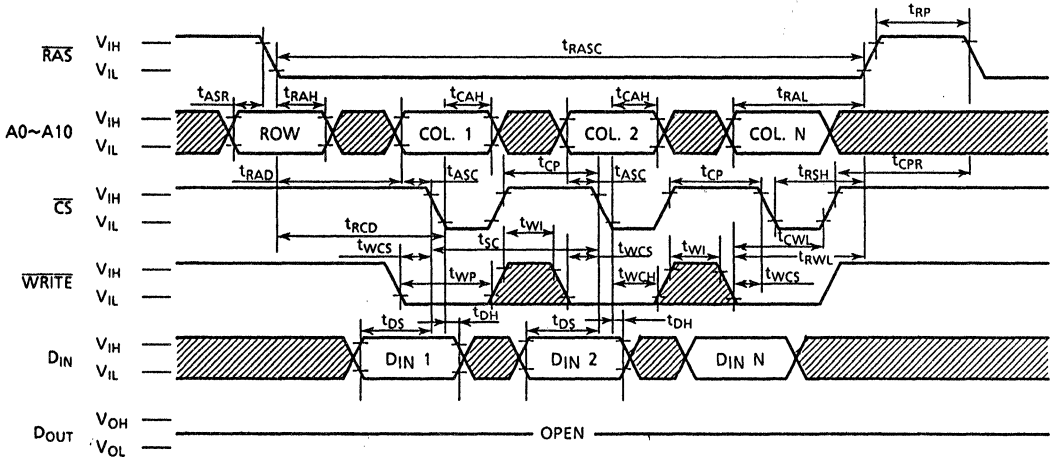
READ - MODIFY - WRITE CYCLE



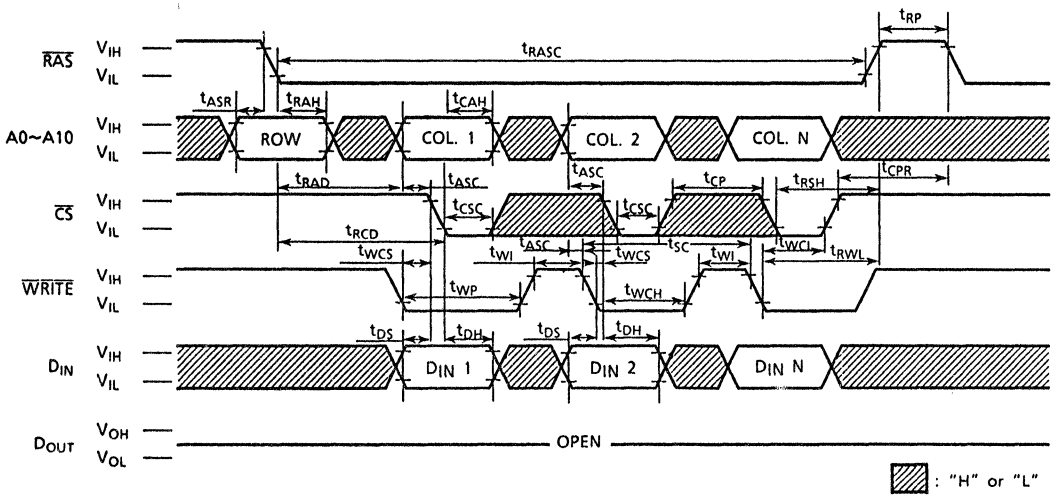
STATIC COLUMN MODE READ CYCLE



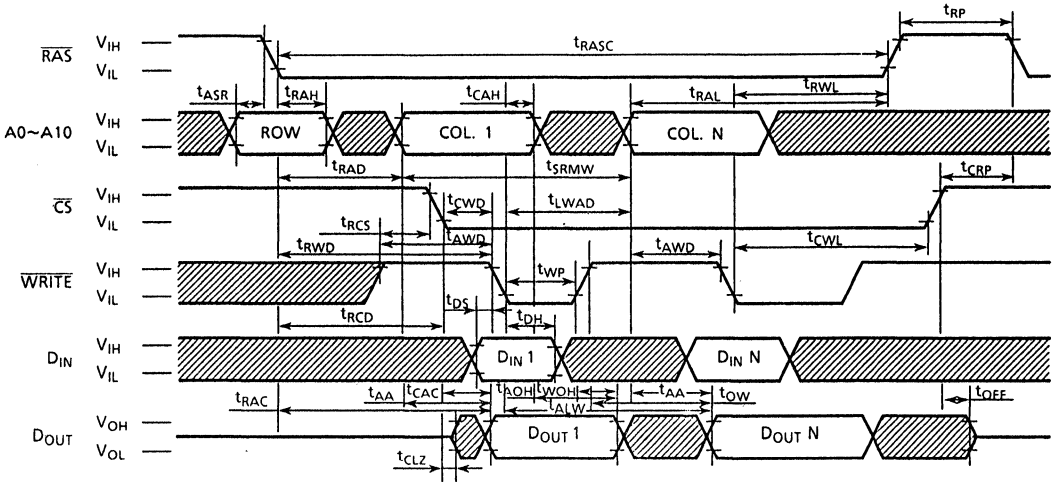
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



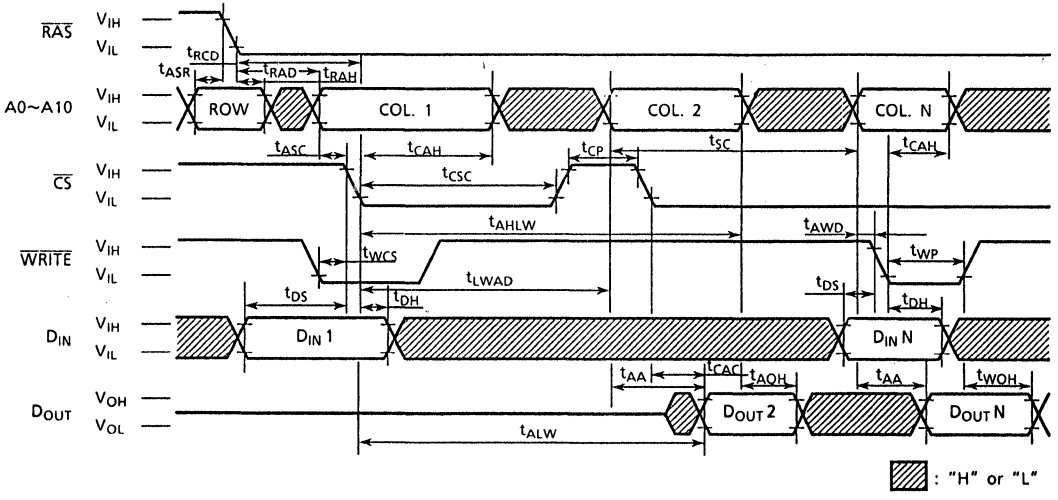
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



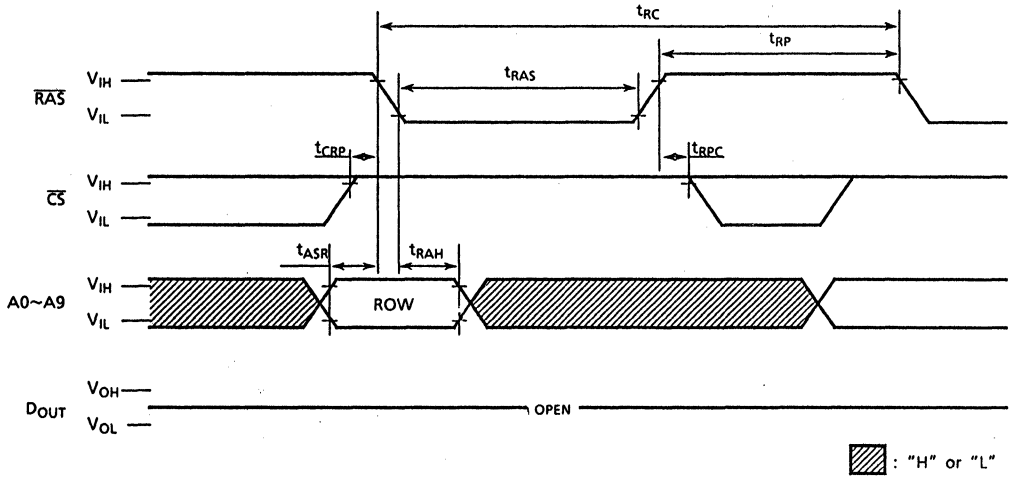
STATIC COLUMN MODE READ - MODIFY - WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

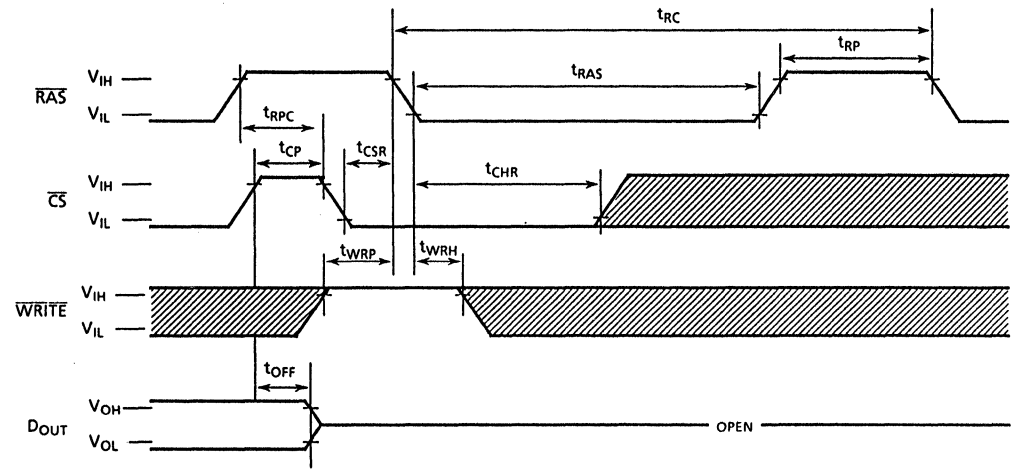


$\overline{RAS}$ ONLY REFRESH CYCLE



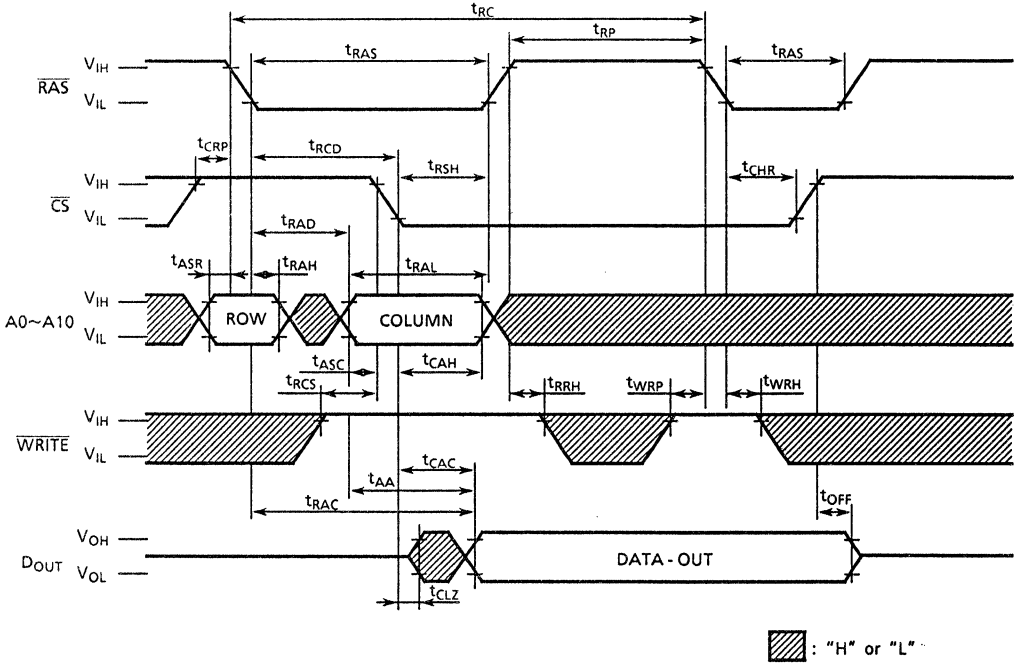
Note: $\overline{WRITE}$, A10 = "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

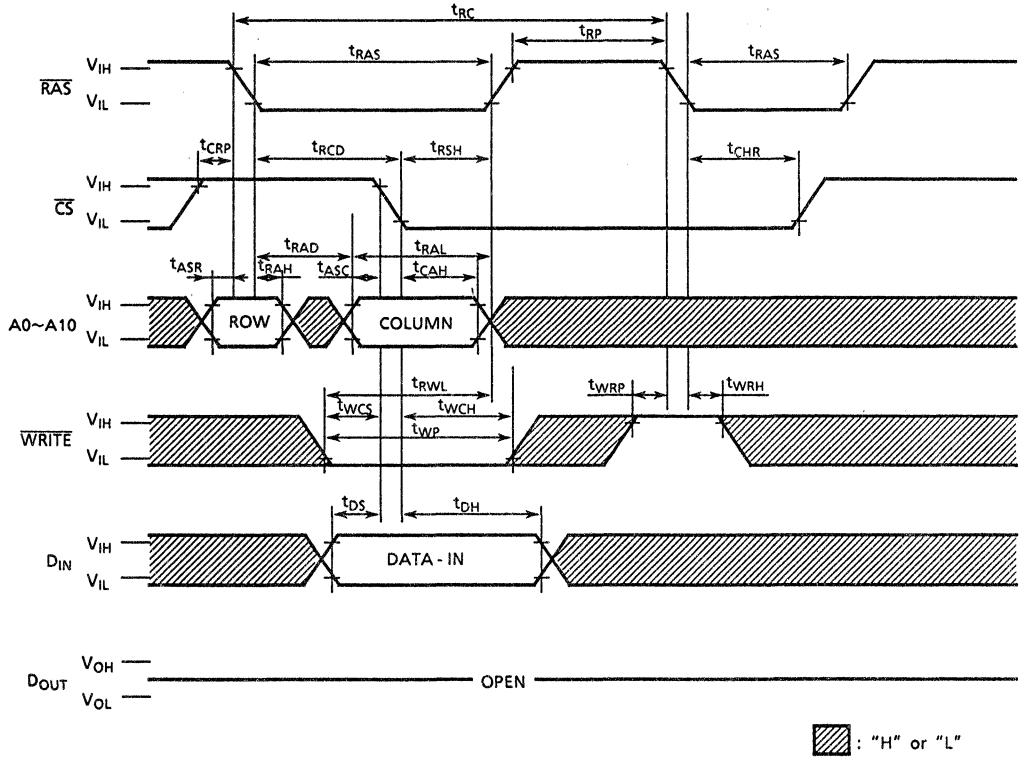


Note: A0~A10 = "H" or "L"

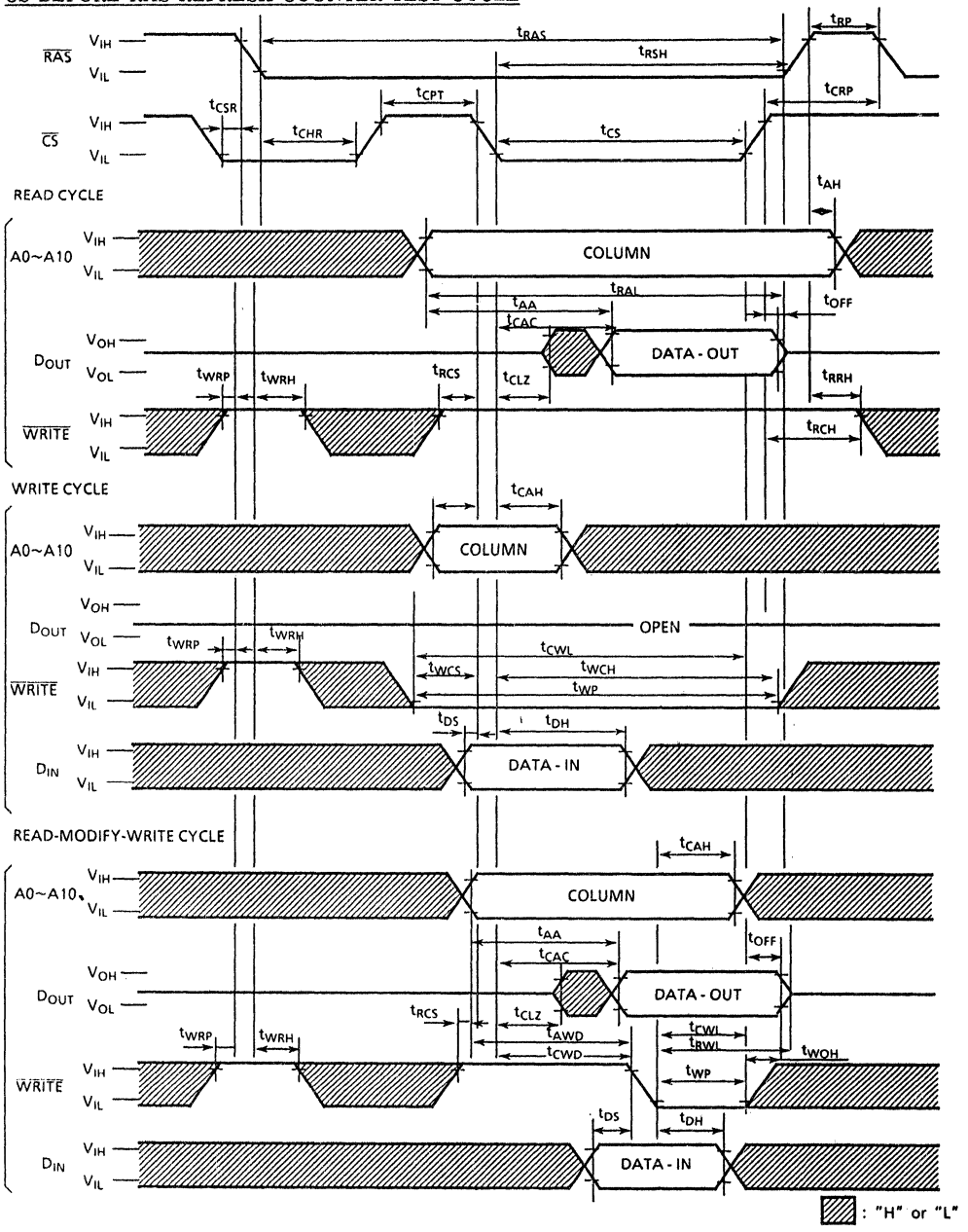
HIDDEN REFRESH CYCLE (READ)



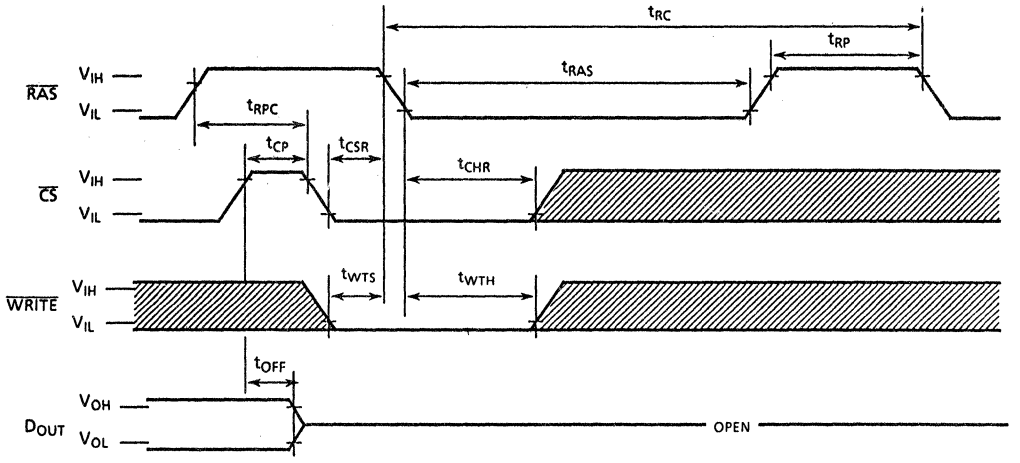
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, CS BEFORE RAS REFRESH CYCLE



Note: D_{IN}, A0~A10="H" or "L"

▨ : "H" or "L"

TEST MODE

The TC514102AP/AJ/ASJ/AZ is The RAM organized 4,194,304words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or" 0"s), the data output pin indicates a "1"shows the block diagram of TC514102AP/AJ/ASJ/AZ. In"Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device "Test Mode". And "$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle "or" $\overline{\text{RAS}}$ Only Refresh Cycle"puts it back into "Normal Mode".In the Test Mode, "$\overline{\text{WRITE}}$. $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" functiom reduces test times(1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

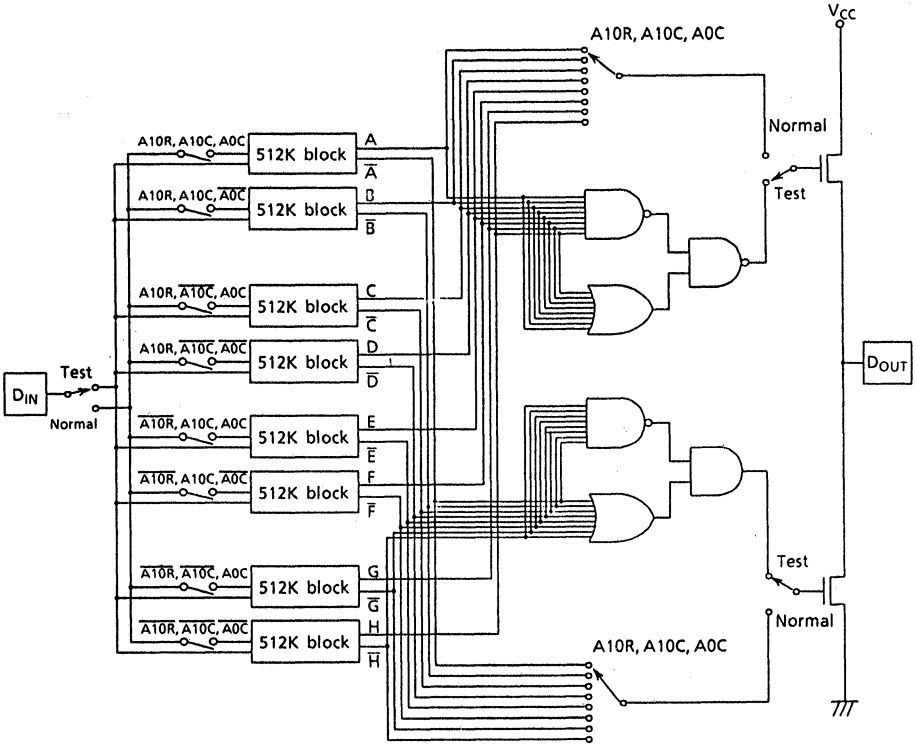


Fig. 1

4,194,304 WORD × 1 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514102AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514102AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514102AP/AJ/ASJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 1bit organization
- Fast access time and cycle time

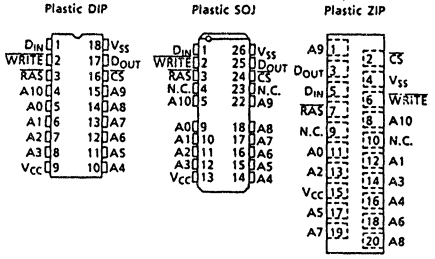
	TC514102AP/AJ/ASJ/AZ-70/-80/-10		
t_{RAC} $\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA} Column Address Access Time	35ns	40ns	50ns
t_{CAC} $\overline{CS}$ Access Time	20ns	20ns	25ns
t_{RC} Cycle Time	130ns	150ns	180ns
t_{SC} Static Column Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 550mW MAX. Operating (TC514102AP/AJ/ASJ/AZ-70)
  - 468mW MAX. Operating (TC514102AP/AJ/ASJ/AZ-80)
  - 413mW MAX. Operating (TC514102AP/AJ/ASJ/AZ-10)
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1,024 refresh cycles/16ms
- Package TC514102AP : DIP18-P-300E
  TC514102AJ : SOJ26-P-350
  TC514102ASJ : SOJ26-P-300A
  TC514102AZ : ZIP20-P-400A

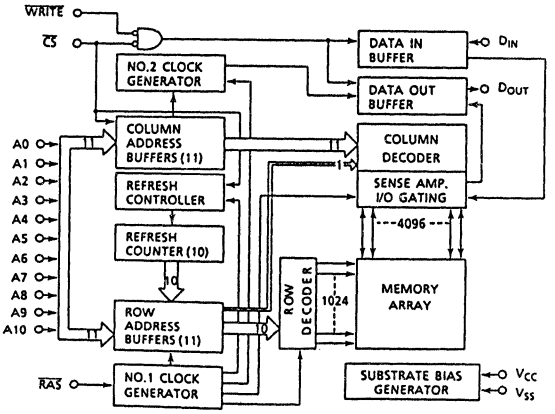
PIN NAMES

A0~A10	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	N.C.	No Connection
$\overline{CS}$	Chip Select Input		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514102AP/AJ/ASJ/AZ-70	–	100	mA	3, 4
		TC514102AP/AJ/ASJ/AZ-80	–	85		5
		TC514102AP/AJ/ASJ/AZ-10	–	75		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514102AP/AJ/ASJ/AZ-70	–	100	mA	3, 5
		TC514102AP/AJ/ASJ/AZ-80	–	85		
		TC514102AP/AJ/ASJ/AZ-10	–	75		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$ = $\overline{CS}$ = VIL, Address Cycling: tSC = tSC MIN.)	TC514102AP/AJ/ASJ/AZ-70	–	75	mA	3, 4
		TC514102AP/AJ/ASJ/AZ-80	–	65		5
		TC514102AP/AJ/ASJ/AZ-10	–	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514102AP/AJ/ASJ/AZ-70	–	100	mA	3, 5
		TC514102AP/AJ/ASJ/AZ-80	–	85		
		TC514102AP/AJ/ASJ/AZ-10	–	75		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IH} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ + 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514102AP/ AJ/ASJ/AZ-70		TC514102AP/ AJ/ASJ/AZ-80		TC514102AP/ AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	–	175	–	210	–	ns	
t_{SC}	Static Column Mode Cycle Time	40	–	45	–	55	–	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	70	–	80	–	100	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	9, 14 15
t_{CAC}	Access Time from $\overline{CS}$	–	20	–	20	–	25	ns	9, 14
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	9, 15
t_{ALW}	Access Time from Last Write	–	65	–	75	–	95	ns	9, 16
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Address	5	–	5	–	5	–	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	–	20	–	20	–	25	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	–	0	–	0	–	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	70	200,000	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	200,000	20	200,000	25	200,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{AWR}	Column Address Hold Time referenced to $\overline{RAS}$ (WRITE CYCLE)	55	–	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514102AP/ AJ/ASJ/AZ-70		TC514102AP/ AJ/ASJ/AZ-80		TC514102AP/ AJ/ASJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$ (READ SYCLE)	80	–	90	–	115	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	–	5	–	10	–	ns	17
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	–	20	–	25	–	ns	
t_{LWAD}	Last Write to Column Address Delay Time	20	30	20	35	25	45	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	65	–	75	–	95	–	ns	
t_{RCS}	Read Command Set-up Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	13
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{WI}	Write Command Inactive Time	10	–	10	–	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data-In Hold Time	15	–	15	–	20	–	ns	12
t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	20	–	20	–	25	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	70	–	80	–	100	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	–	40	–	50	–	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	40	–	40	–	50	–	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	10	–	10	–	15	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514102AP/AJ/ASJ/AZ-70		TC514102AP/AJ/ASJ/AZ-80		TC514102AP/AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WTS}	Write Command Set-Up Time	10	–	10	–	10	–	ns	
t_{WTH}	Write Command Hold Time	10	–	10	–	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATION CONDITIONS IN THE TEST MODE

(Vcc = 5V ± 10%, Ta = 0~70°C) (Note6, 7, 8)

SYMBOL	PARAMETER	TC514102AP/AJ/ASJ/AZ-70		TC514102AP/AJ/ASJ/AZ-80		TC514102AP/AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	155	–	185	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	160	–	180	–	215	–	ns	
t_{SC}	Static Column Mode Cycle Time	45	–	50	–	60	–	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	75	–	85	–	105	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	75	–	85	–	105	ns	9,14 15
t_{CAC}	Access Time from $\overline{CS}$	–	25	–	25	–	30	ns	9,14
t_{AA}	Access Time from Column Address	–	40	–	45	–	55	ns	9,15
t_{ALW}	Access Time from Last Write	–	70	–	80	–	100	ns	9, 16
t_{RAS}	$\overline{RAS}$ Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	75	20,000	85	20,000	105	20,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CS}$ Hold Time	75	–	85	–	105	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	20,000	25	20,000	30	20,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	45	–	55	–	ns	
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time	25	–	25	–	30	–	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	75	–	85	–	105	–	ns	
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	40	–	45	–	55	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

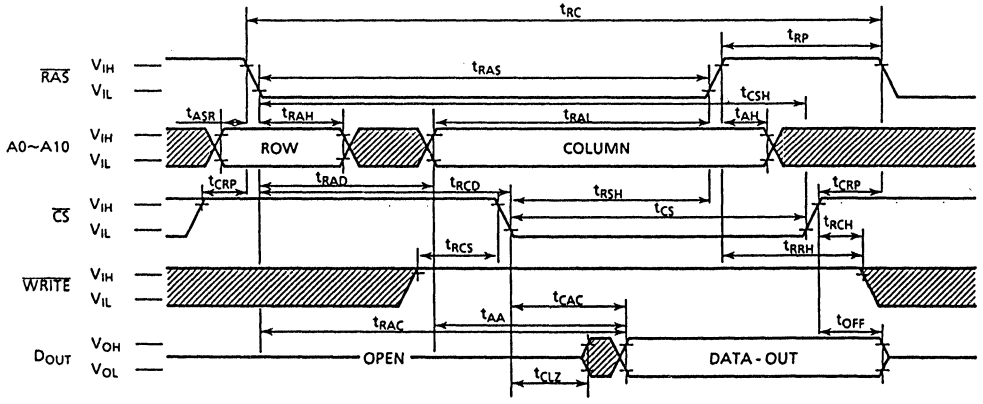
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$)	–	7	pF
C_O	Output Capacitance (D_{OUT})	–	7	pF

NOTES:

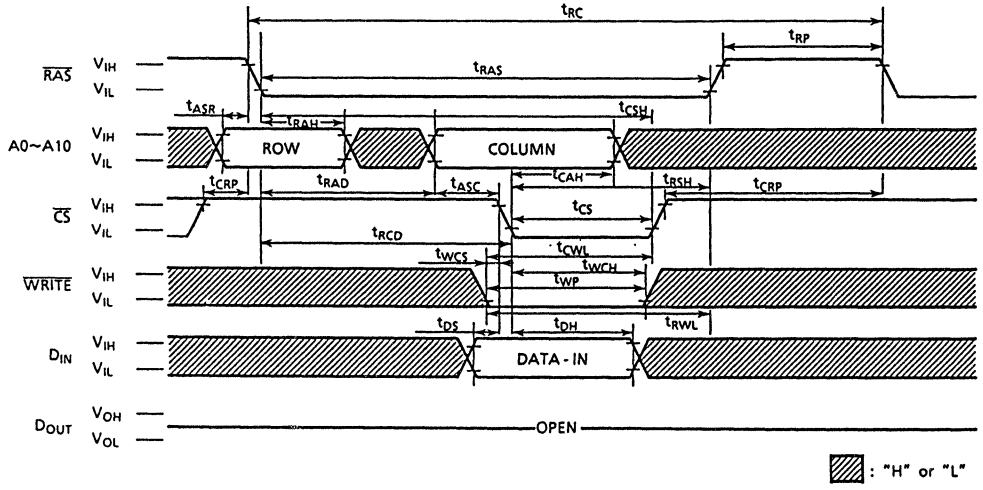
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refreh cycles are required.
7. AC measurements assume $t_T=5$ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (min.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
16. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
17. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

TIMING WAVEFORMS

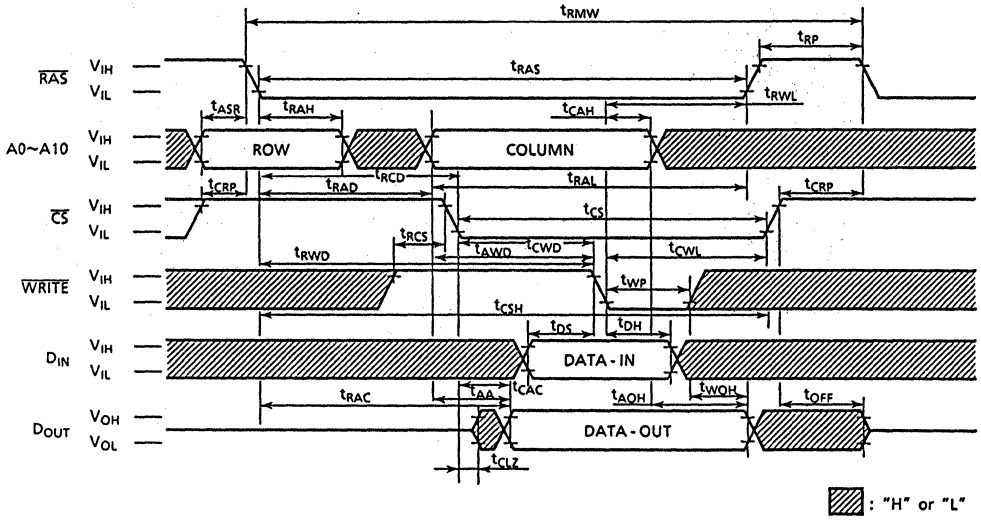
READ CYCLE



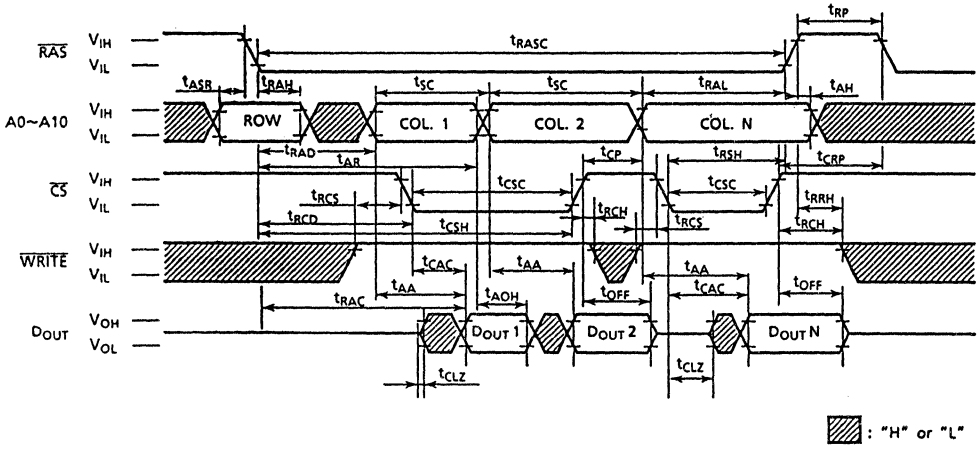
WRITE CYCLE (EARLY WRITE)



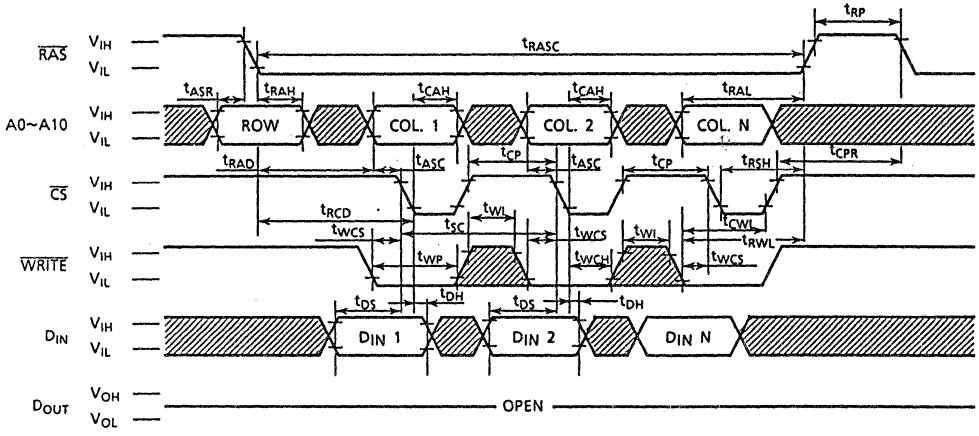
READ - MODIFY - WRITE CYCLE



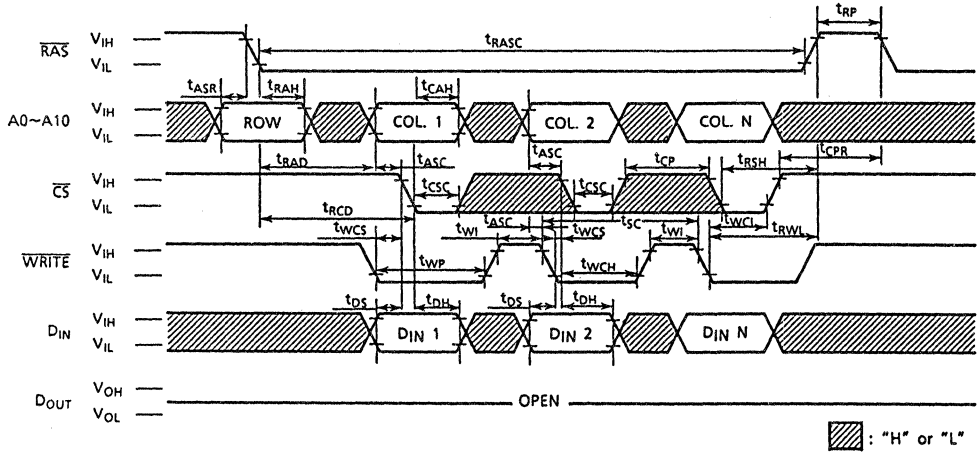
STATIC COLUMN MODE READ CYCLE



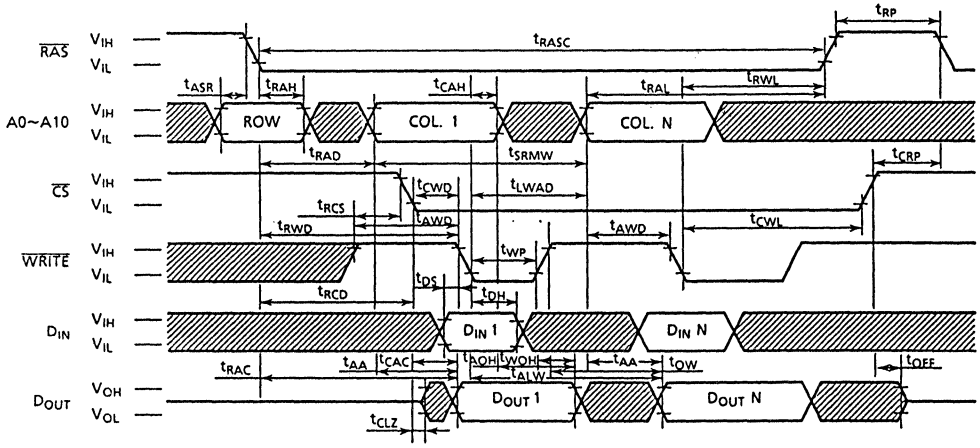
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



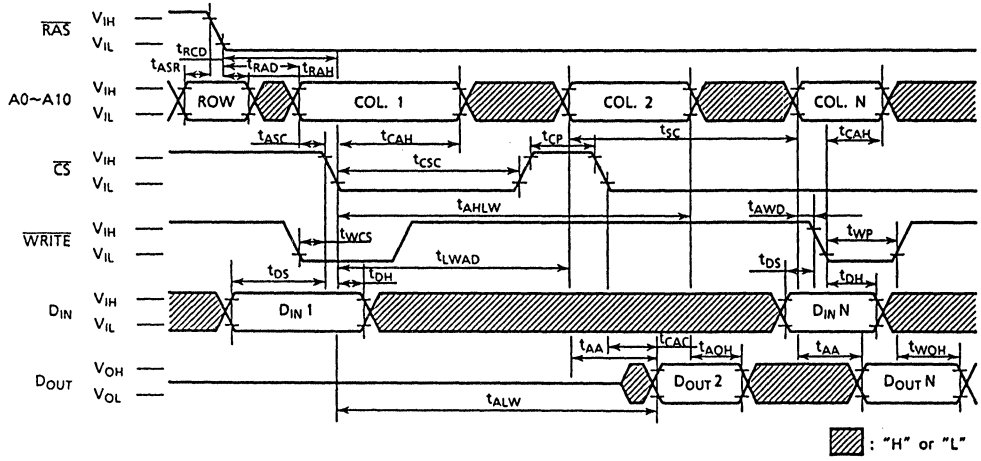
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



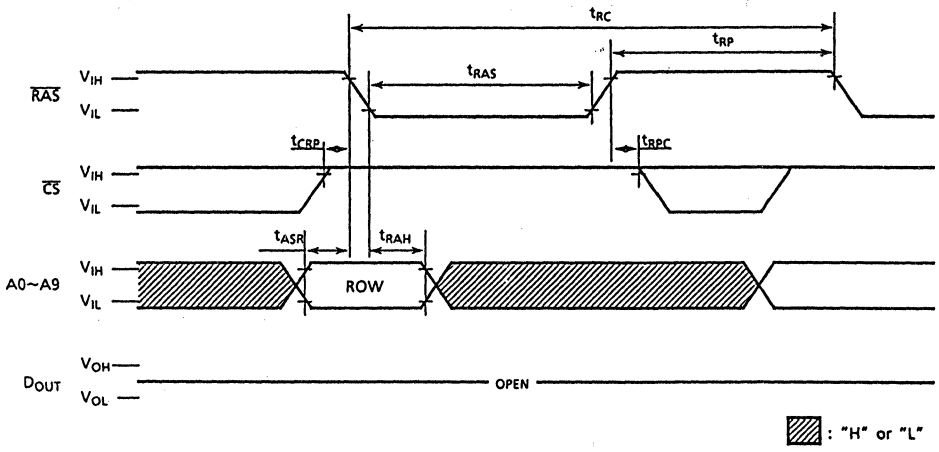
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

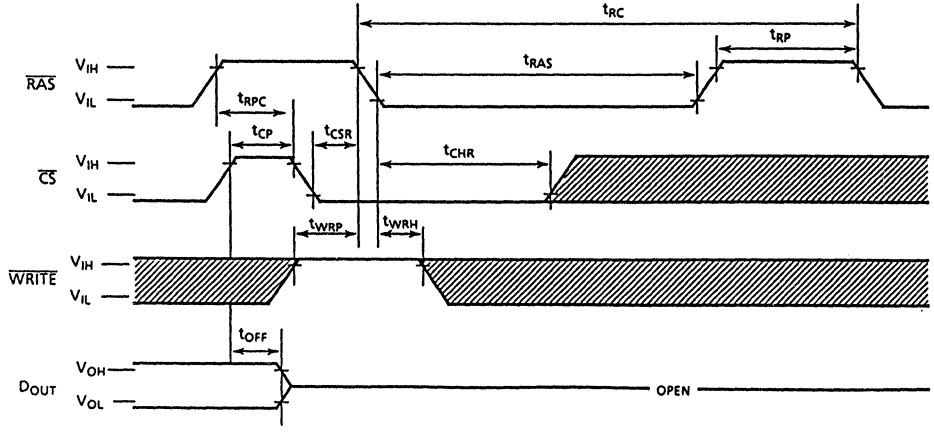


$\overline{RAS}$ ONLY REFRESH CYCLE



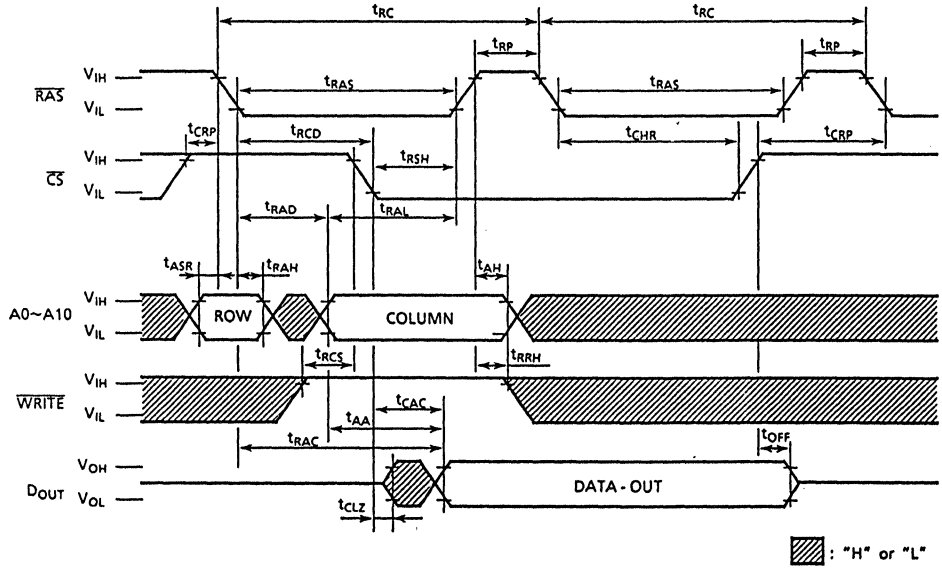
Note: $\overline{WRITE}$, A10 = "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

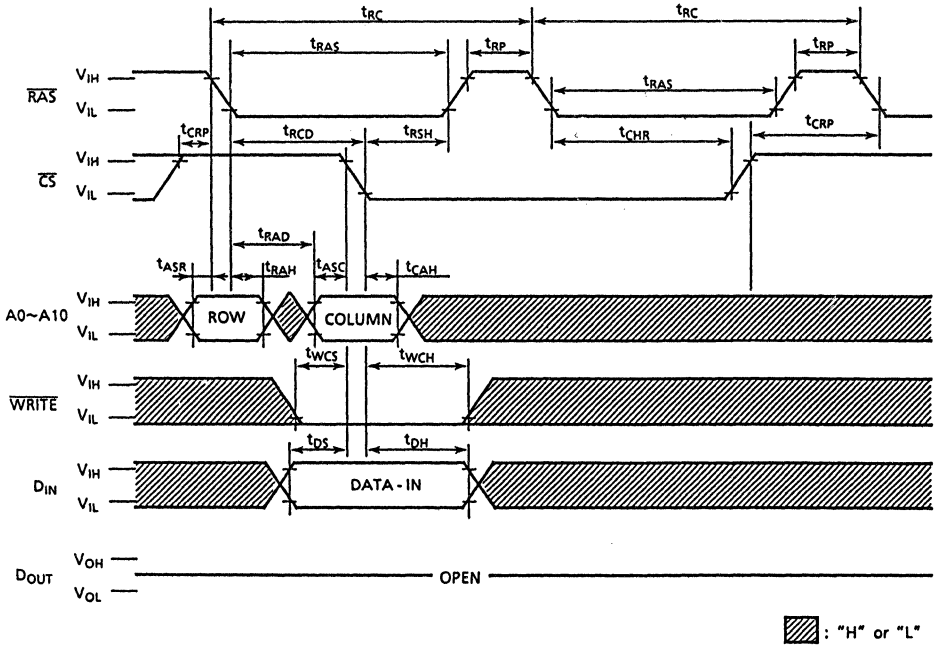


Note: A0~A10 = "H" or "L"

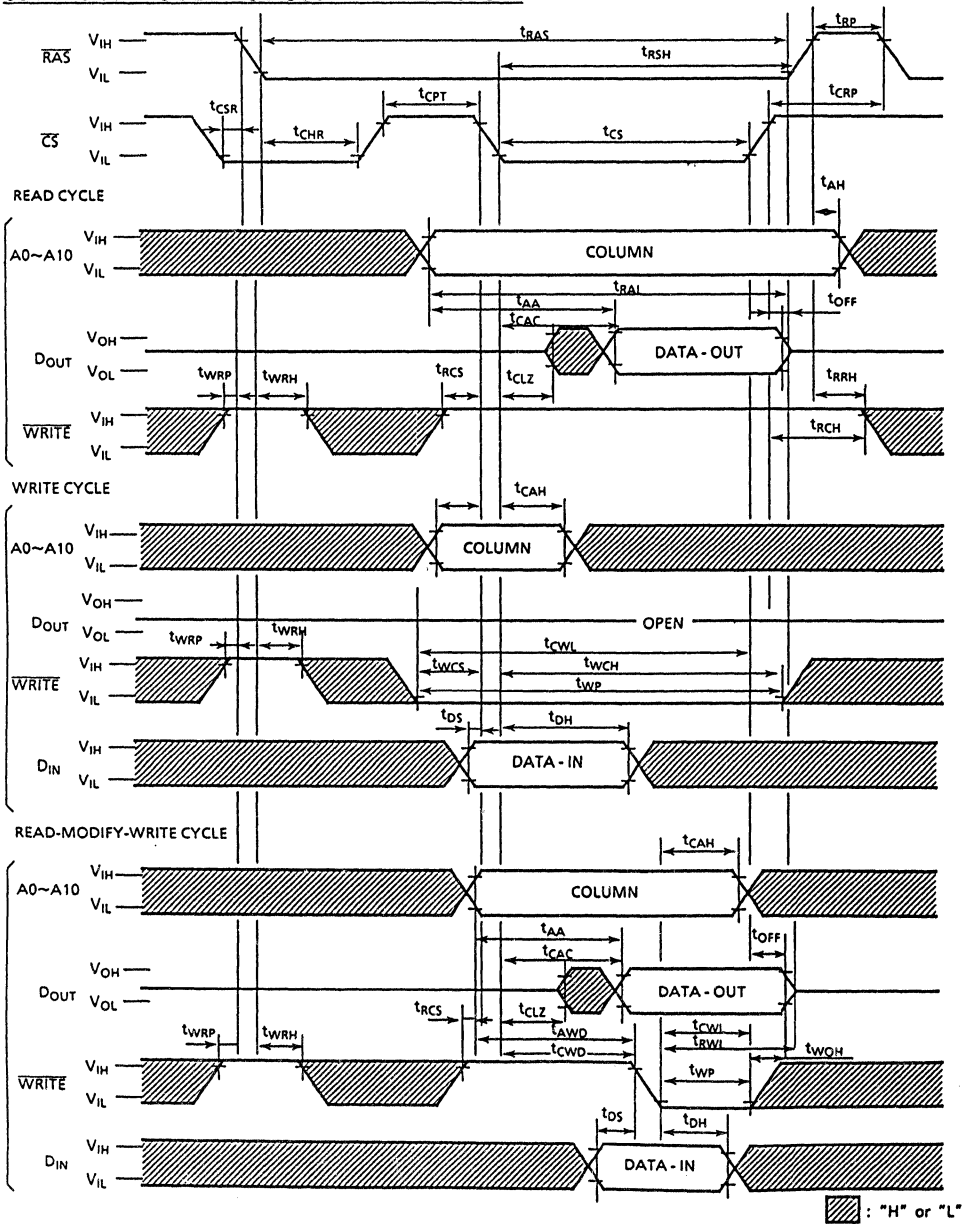
HIDDEN REFRESH CYCLE (READ)



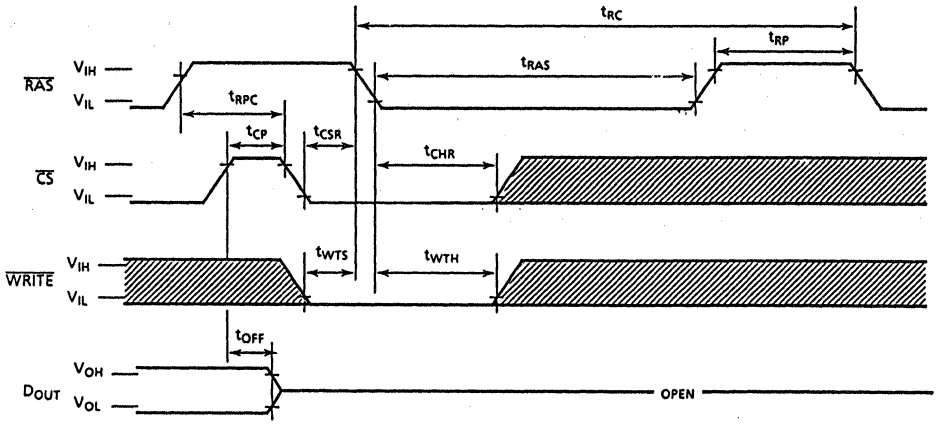
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, A0~A10="H" or "L"

▨: "H" or "L"

TEST MODE

The TC514102AP/AJ/ASJ/AZ is The RAM organized 4,194,304words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or" 0"s), the data output pin indicates a "1"shows the block diagram of TC514102AP/AJ/ASJ/AZ. In"Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device "Test Mode". And "$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle "or" $\overline{\text{RAS}}$ Only Refresh Cycle"puts it back into "Normal Mode".In the Test Mode, "$\overline{\text{WRITE}}$. $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" functiom reduces test times(1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

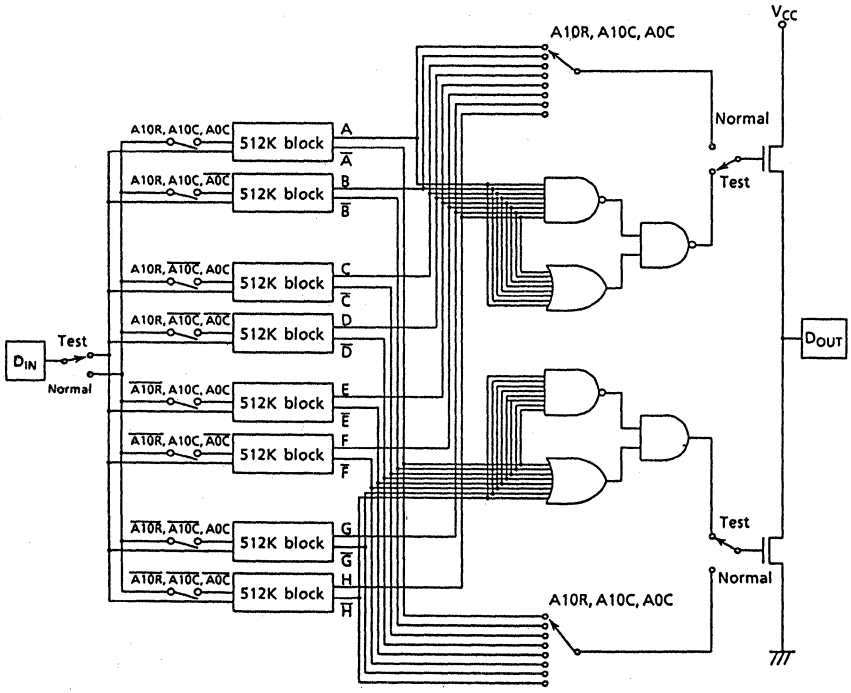


Fig. 1

1,048,576 WORD x 4 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514400J/Z is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514400J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514400J/Z to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

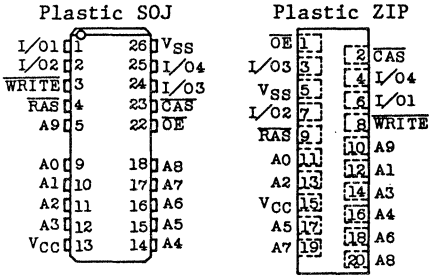
FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

		TC514400J/Z-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  578mW MAX. Operating (TC514400J/Z-80)
  495mW MAX. Operating (TC514400J/Z-10)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package Plastic SOJ: TC514400J
  Plastic ZIP: TC514400Z

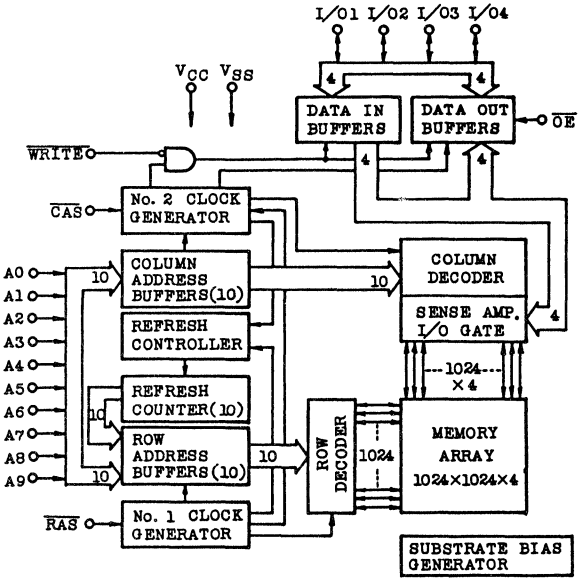
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ∿ I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	-1 ~ 7	V	1
Output Voltage	V_{OUT}	-1 ~ 7	V	1
Power Supply Voltage	V_{CC}	-1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	-55 ~ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514400J/Z-80	-	105	mA	3,4,5
		TC514400J/Z-10	-	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514400J/Z-80	-	105	mA	3,5
		TC514400J/Z-10	-	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC514400J/Z-80	-	70	mA	3,4,5
		TC514400J/Z-10	-	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514400J/Z-80	-	105	mA	3
		TC514400J/Z-10	-	90		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ~ 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514400J/Z -80		TC514400J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	205	-	245	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	60	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	105	-	125	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	40	-	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	55	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	-	55	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514400J/Z-80		TC514400J/Z-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	20	-	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	60	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	110	-	135	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	70	-	85	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time (Fast Page Mode)	75	-	90	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	25	-	ns	
t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	25	-	ns	
t_{WTS}	Write Command Set-Up Time(Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC514400J/Z -80		TC514400J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	155	-	185	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	105	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	30	ns	9,14
t_{AA}	Access Time from Column Address	-	45	-	55	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	60	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	105	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	50	-	60	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Output Capacitance (I/O1~I/O4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

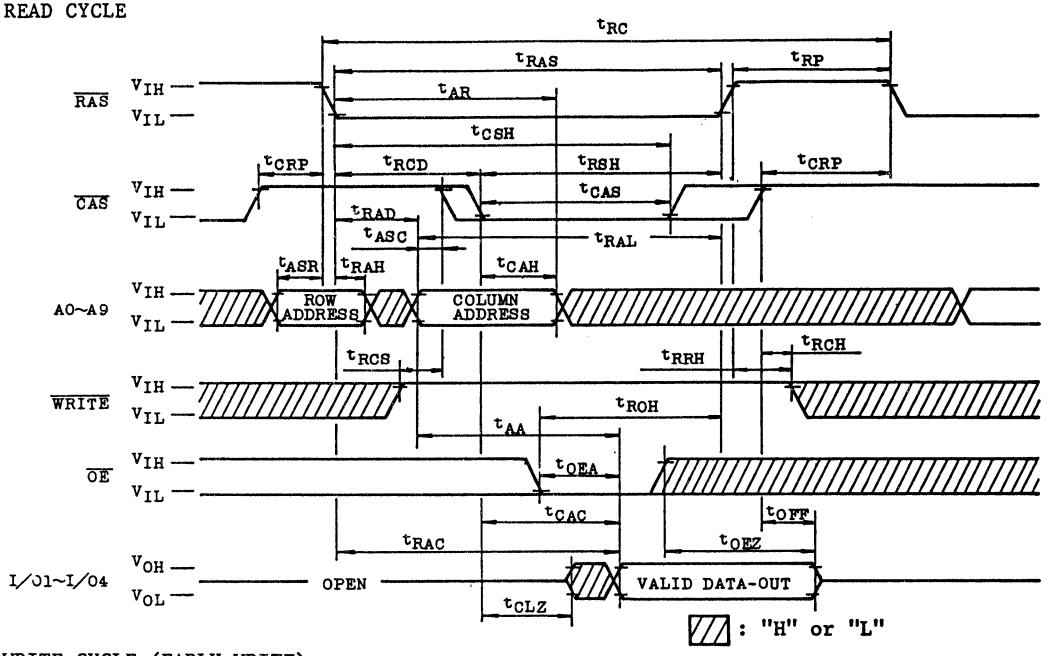
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWD} \geq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

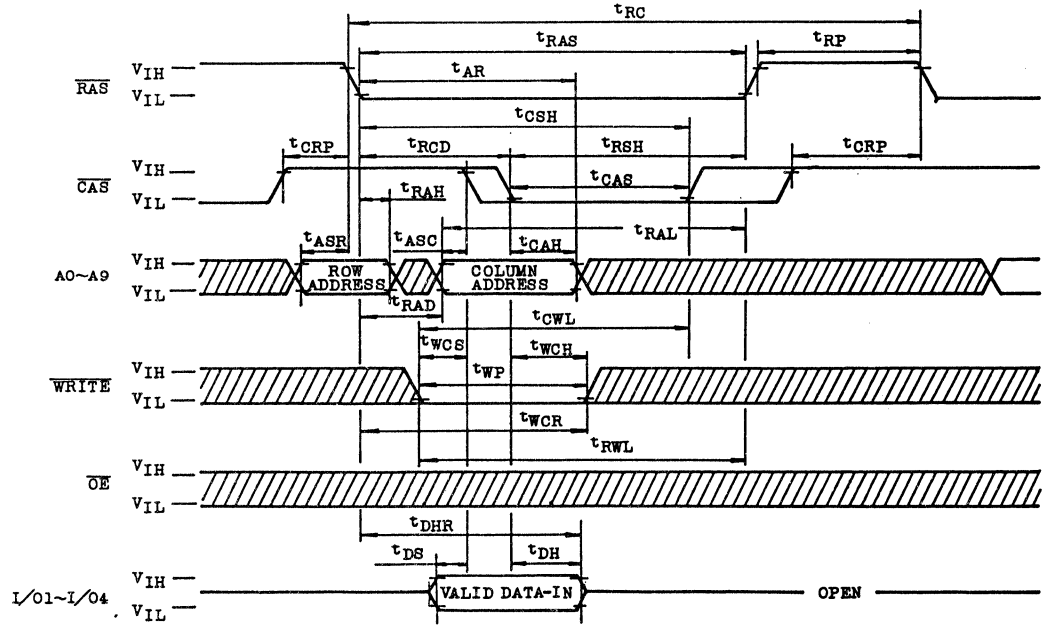
14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

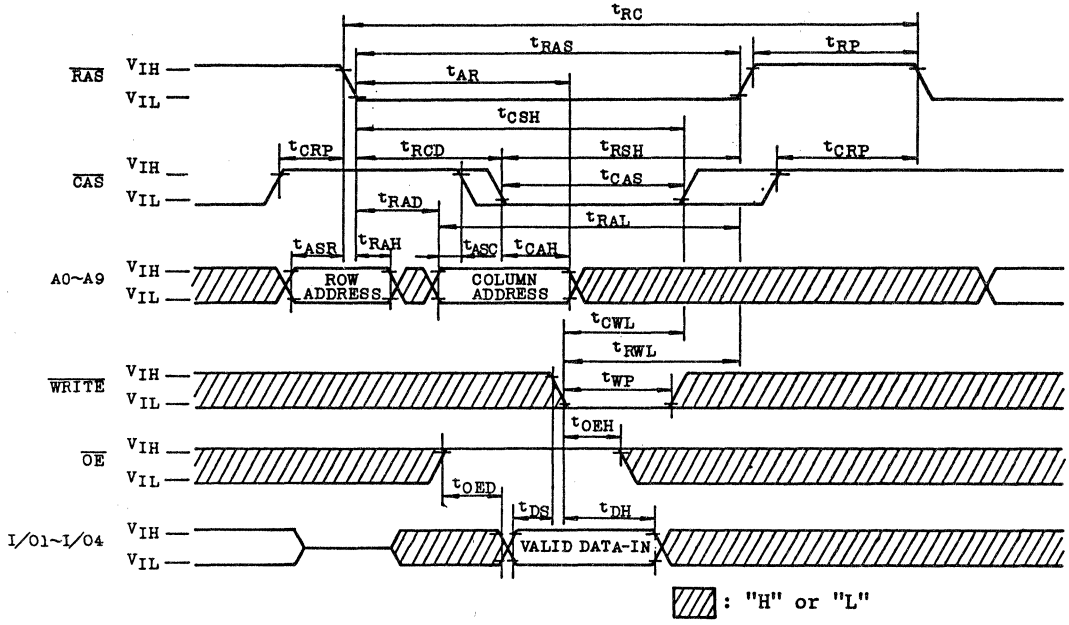
READ CYCLE



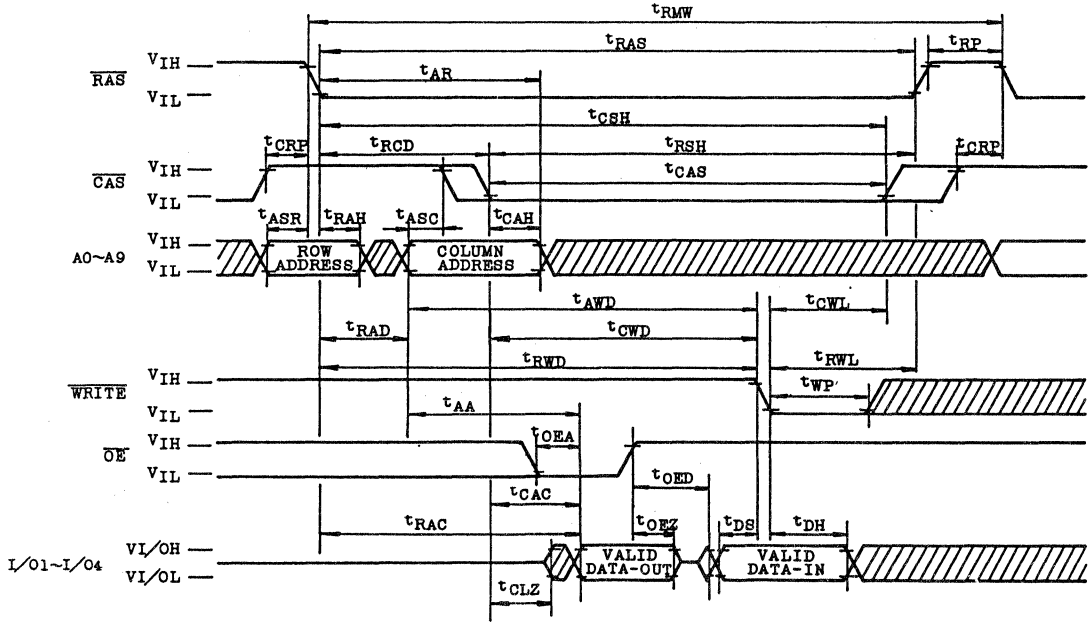
WRITE CYCLE (EARLY WRITE)



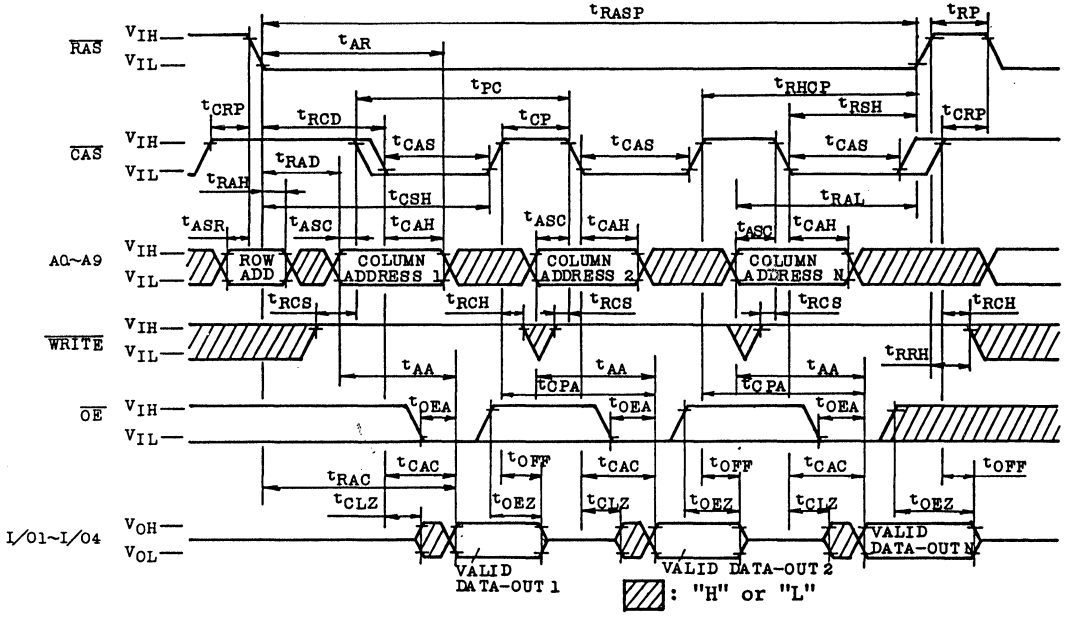
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



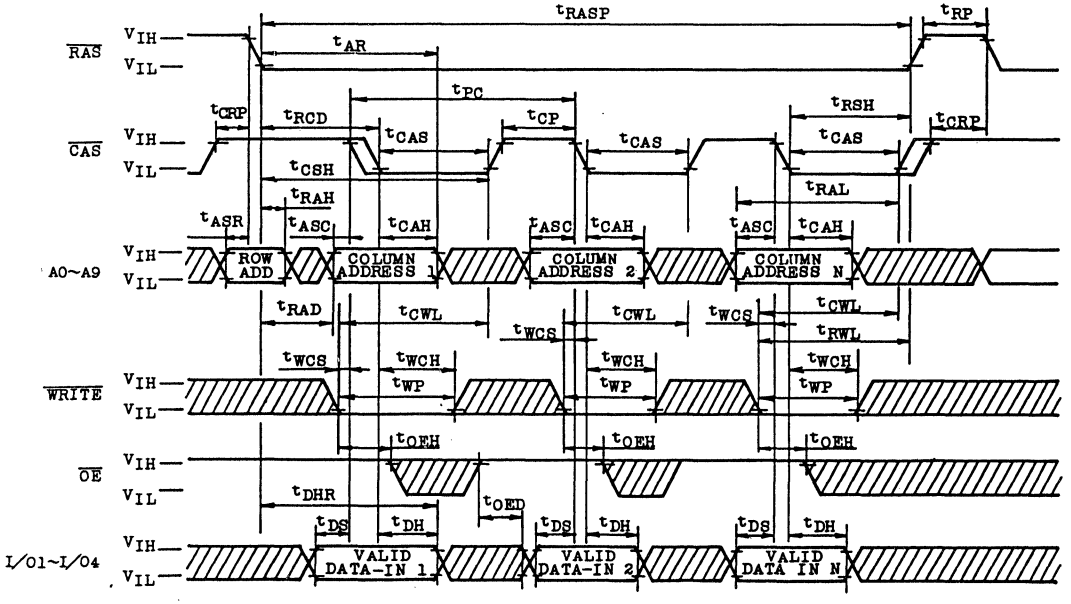
READ-MODIFY-WRITE CYCLE



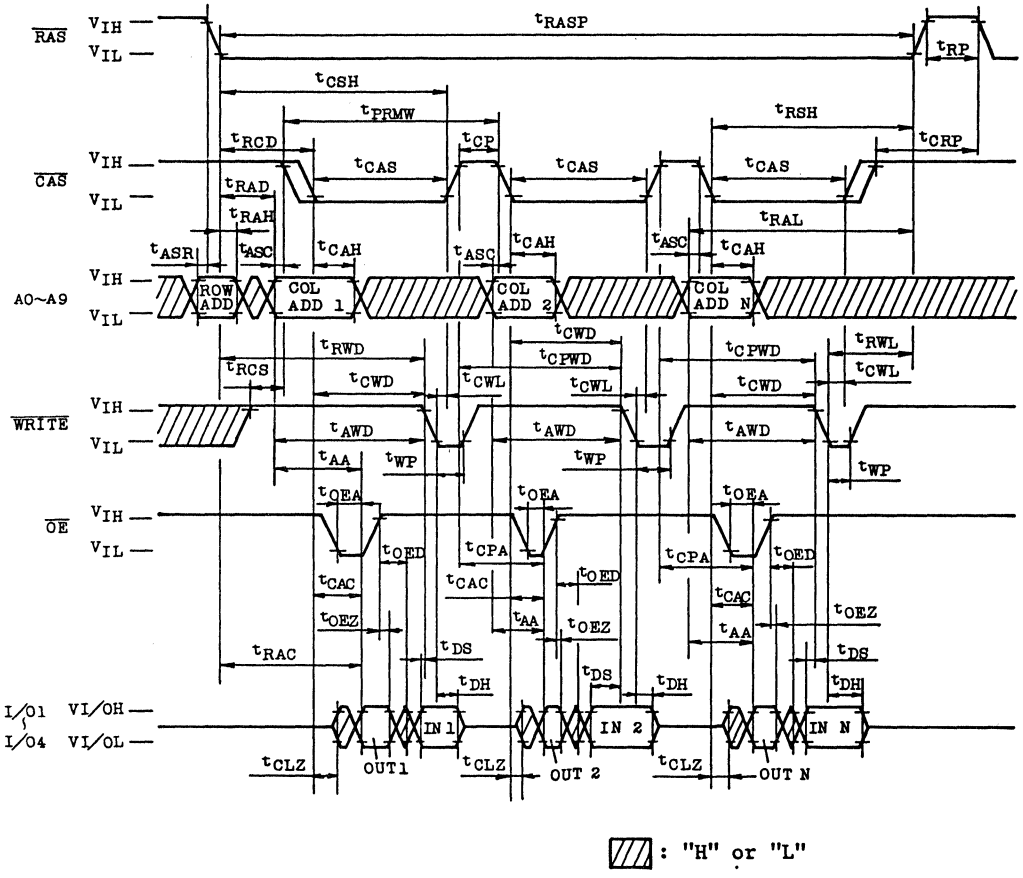
FAST PAGE MODE READ CYCLE



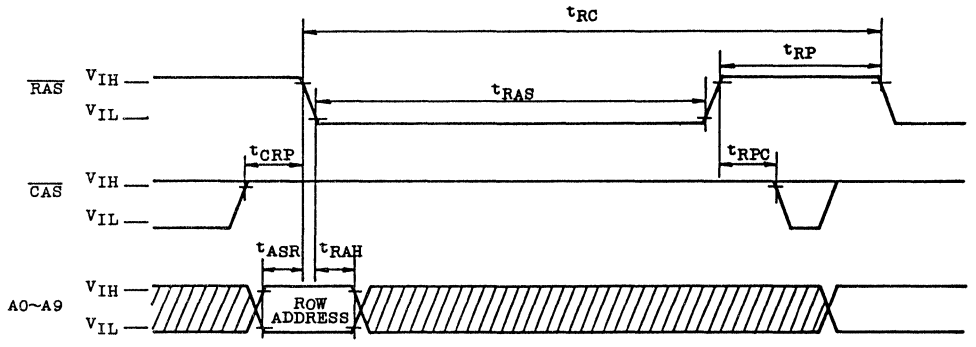
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

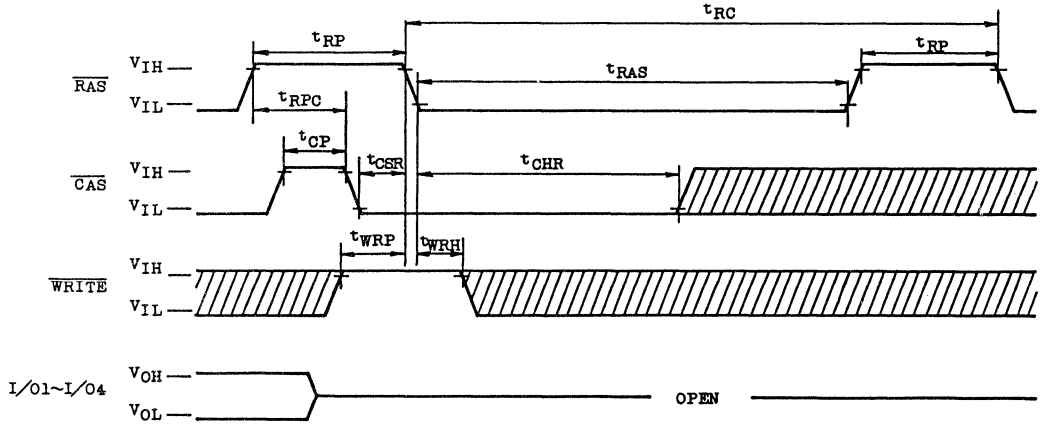


$\overline{RAS}$ ONLY REFRESH CYCLE



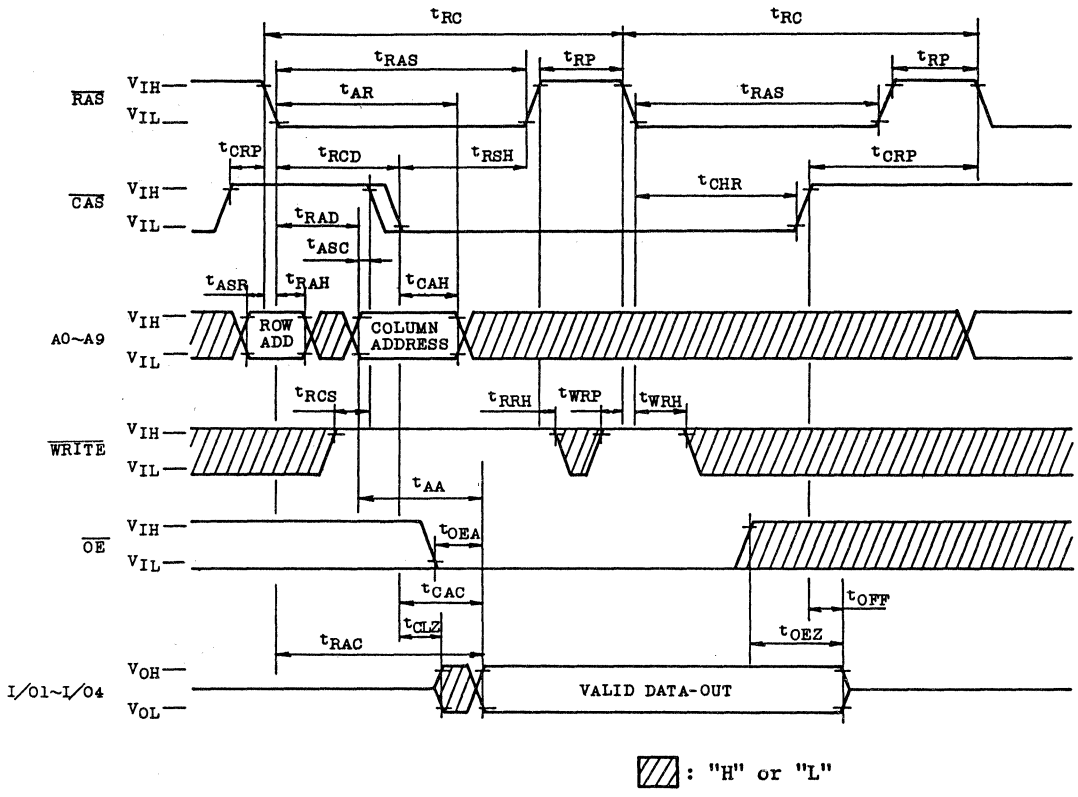
Note: $\overline{WRITE}$, $\overline{OE}$="H" or "L" ▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

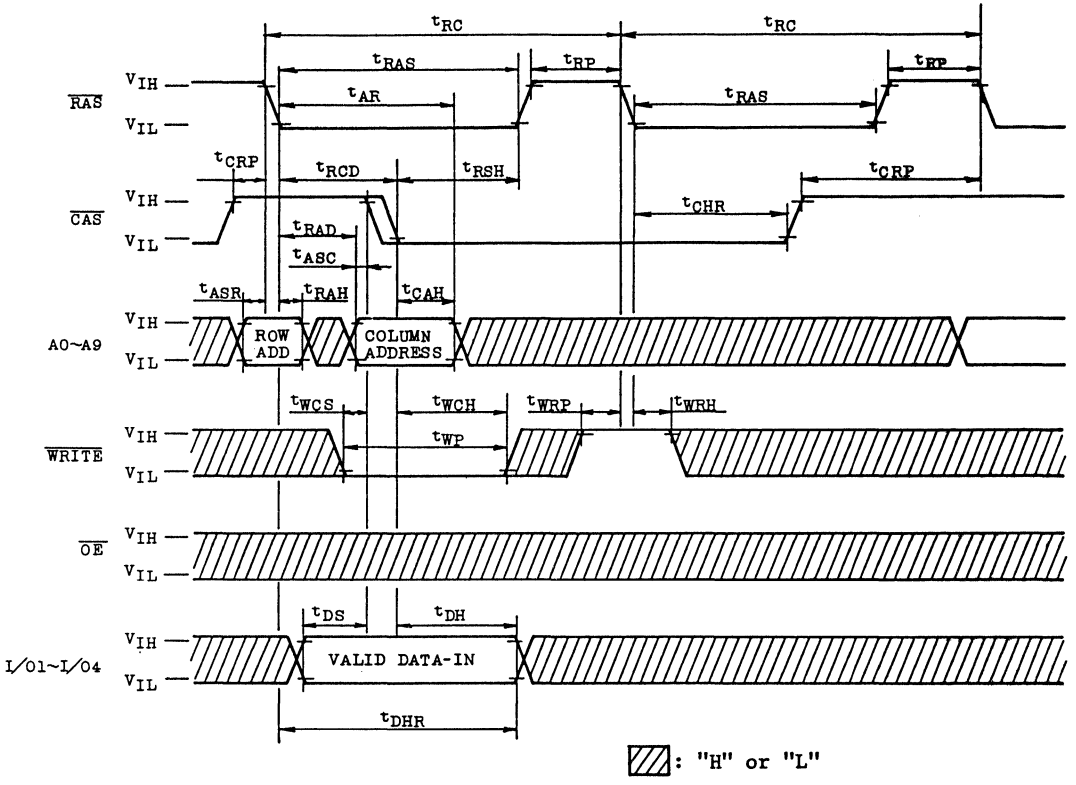


Note: $\overline{OE}$, A0 ∿ A9="H" or "L" ▨ : "H" or "L"

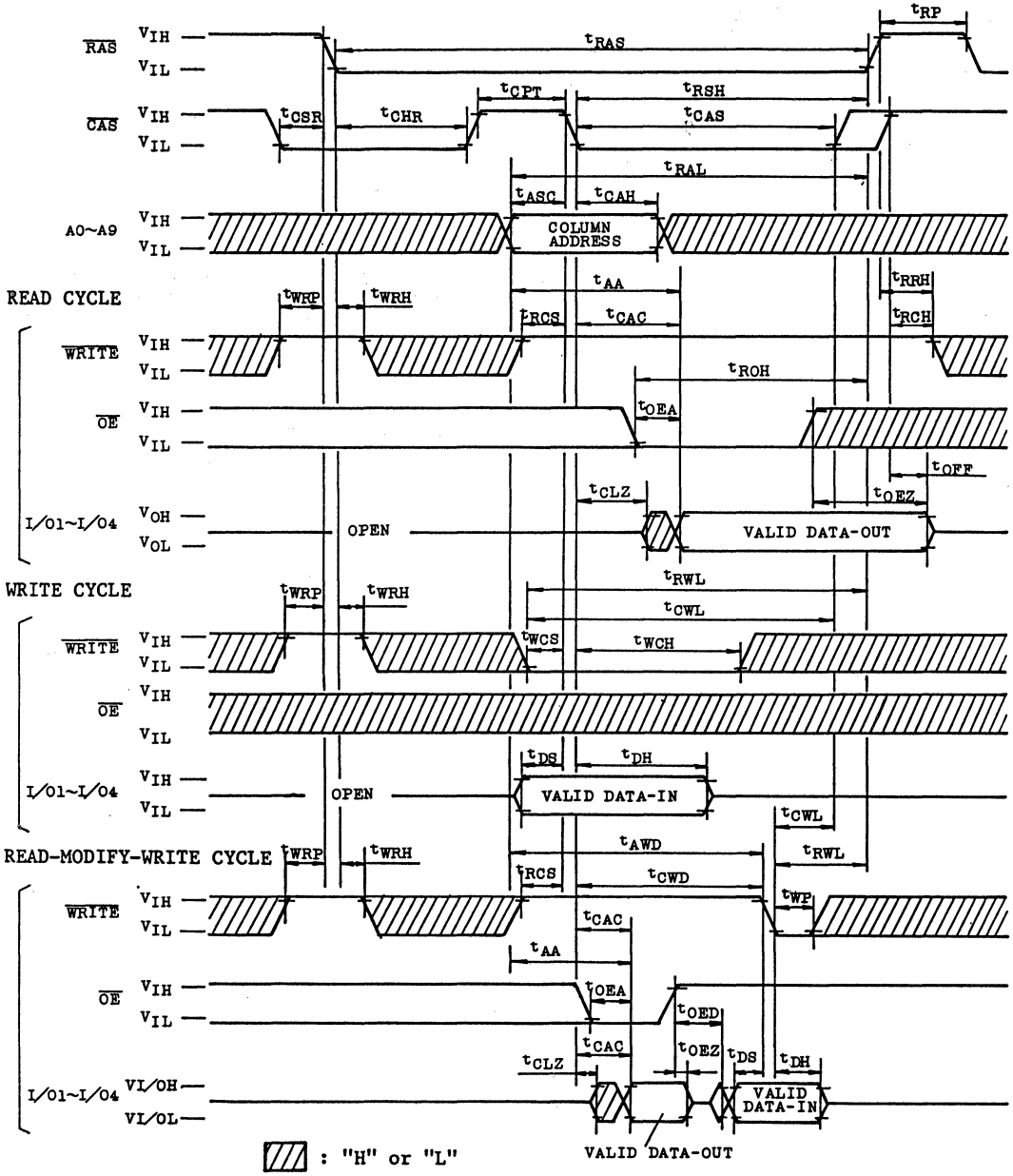
HIDDEN REFRESH CYCLE (READ)



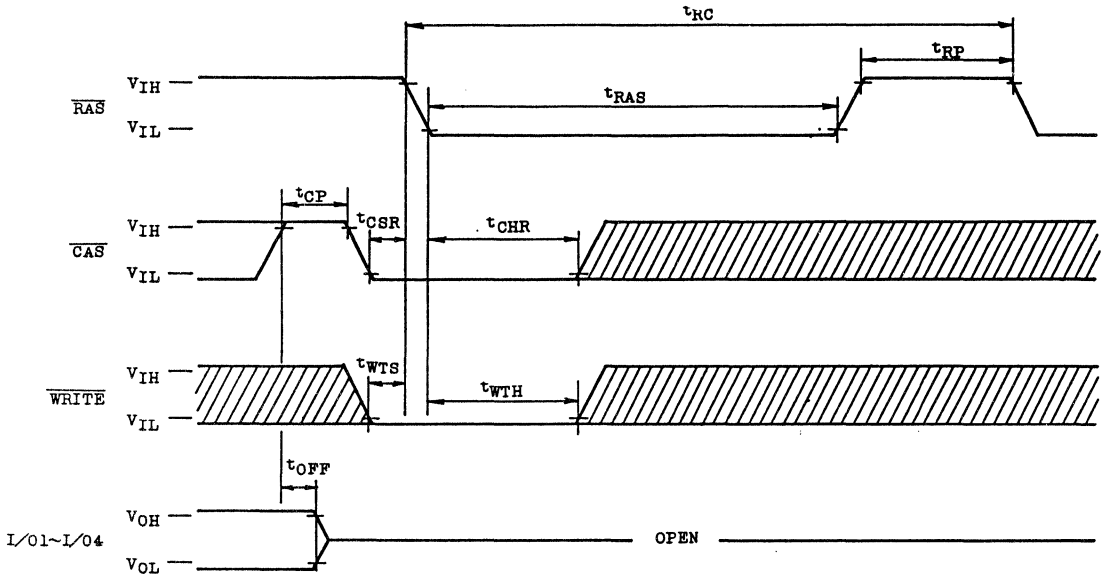
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



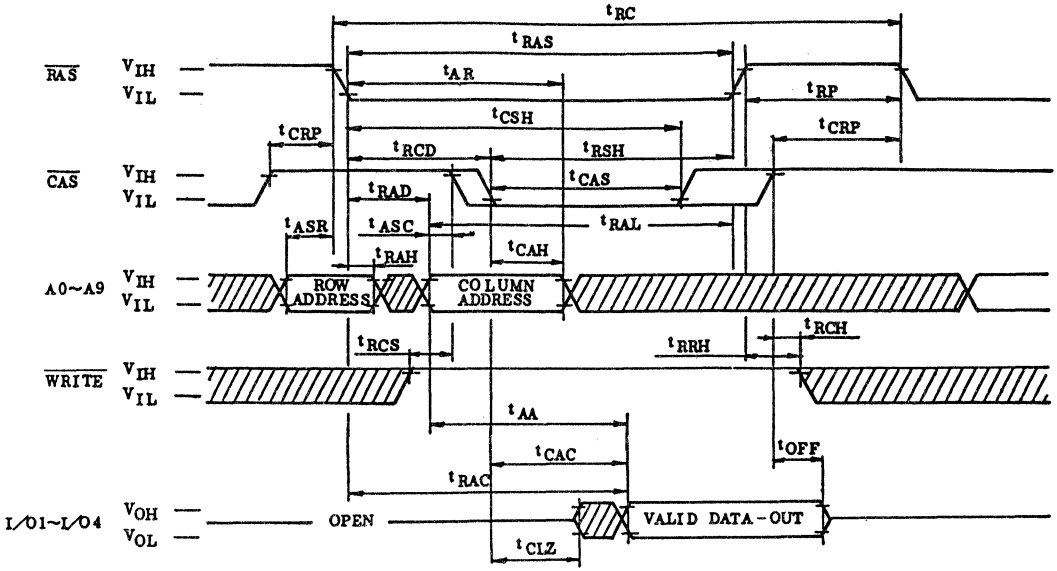
$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



$\overline{\text{OE}}$, A0 ∿ A9: "H" or "L"

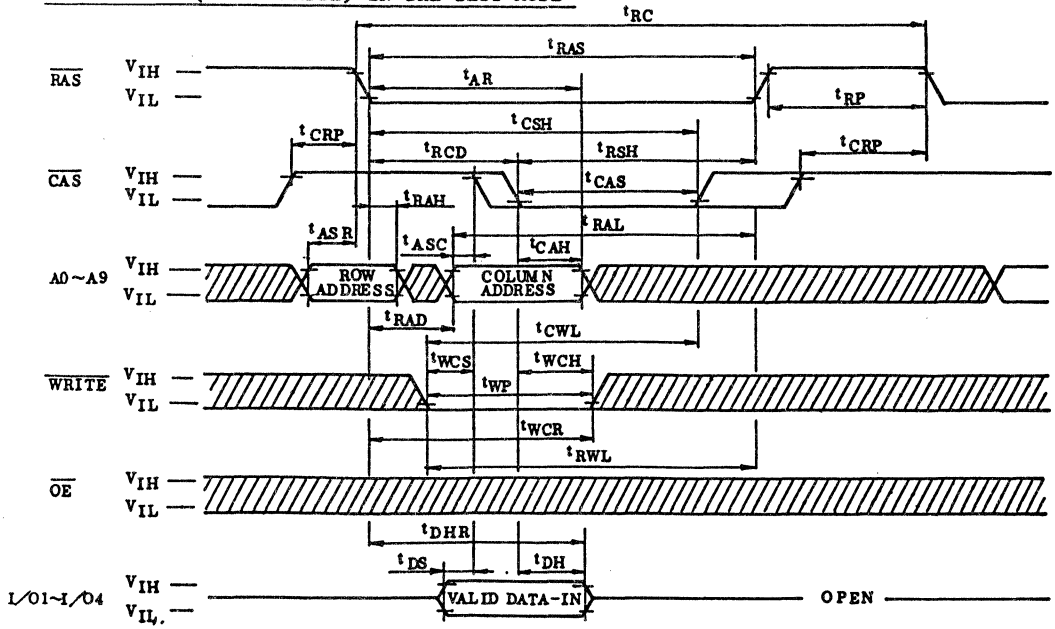
▨: "H" or "L"

READ CYCLE IN THE TEST MODE

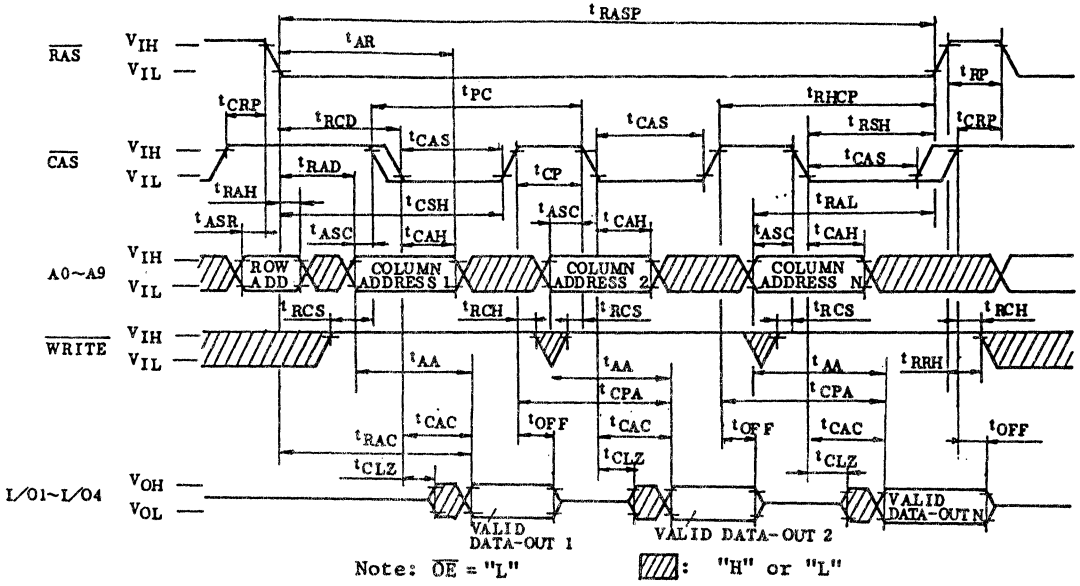


Note: $\overline{OE}$= "L" ▨ : "H" or "L"

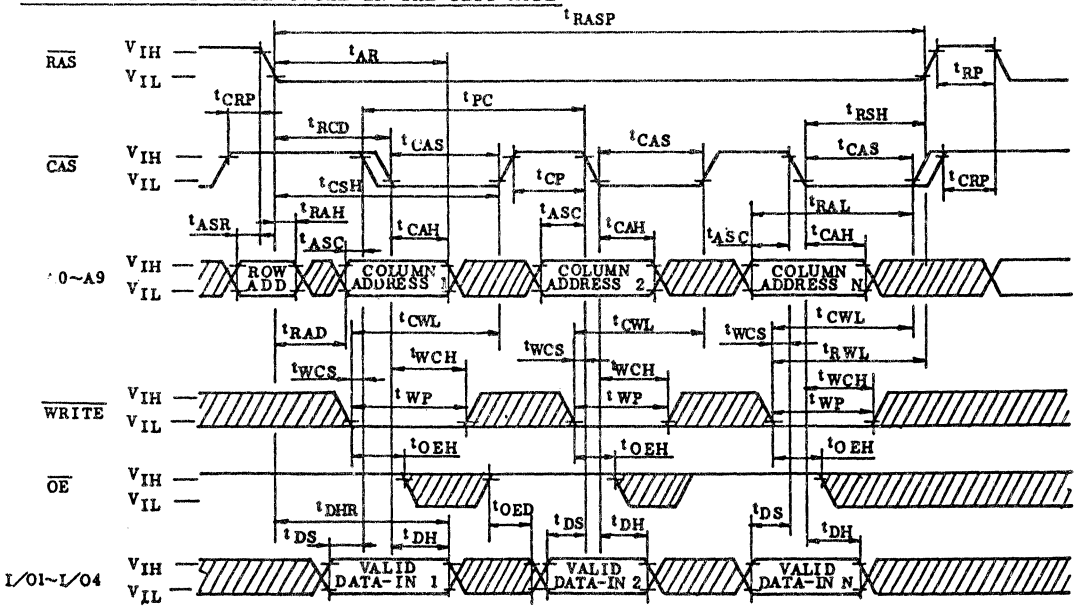
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



FAST PAGE MODE READ CYCLE IN THE TEST MODE



FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



TEST MODE

The TC514400J/Z is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Aoc is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514400J/Z. In "Test Mode", the 1M × 4 DRAM can be tested as if it were a 512K × 4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

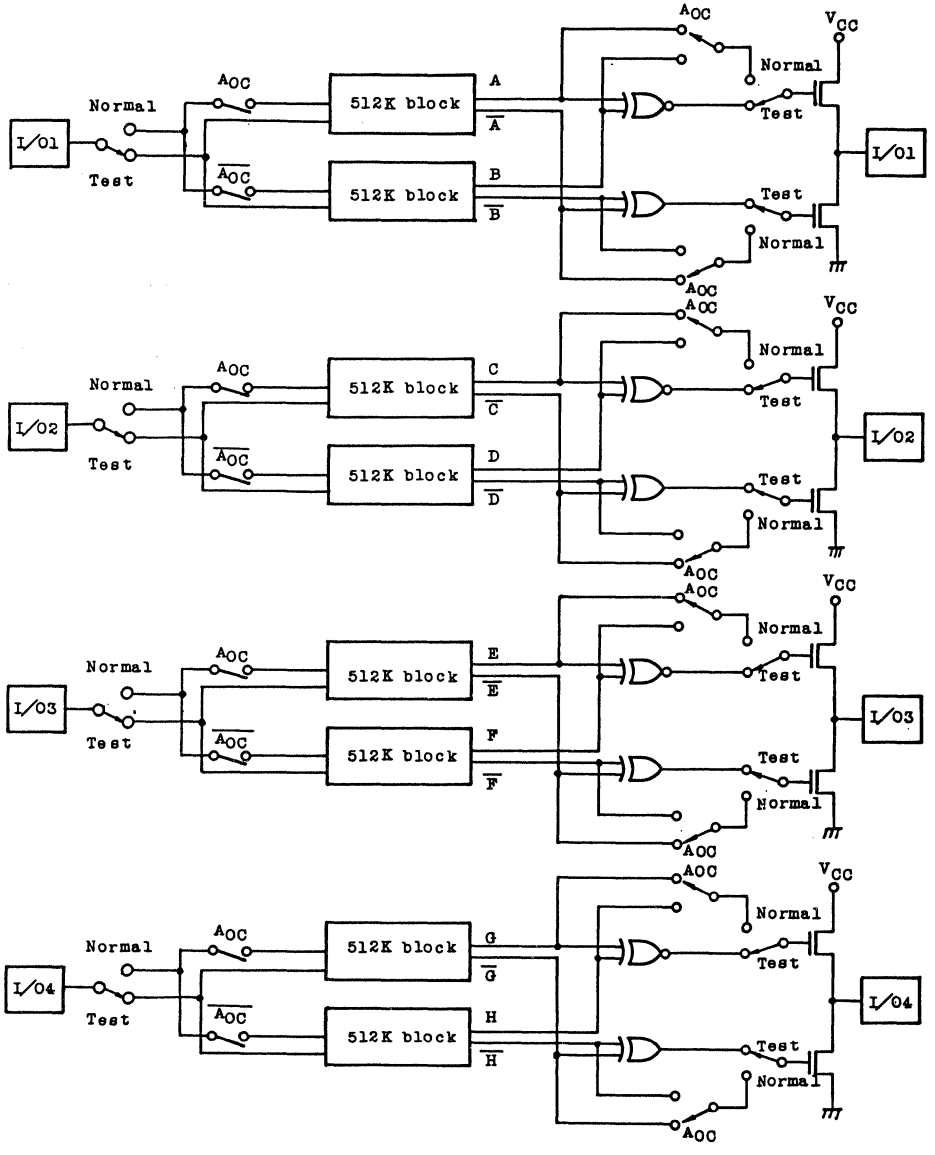


Fig. 1

NOTES

1,048,576 WORD x 4 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514400JL/ZL is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514400JL/ZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514400JL/ZL to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

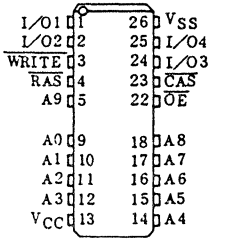
- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

		TC514400JL/ZL-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

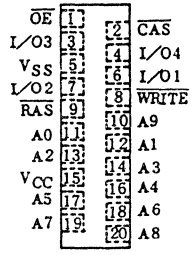
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  578mW MAX. Operating(TC514400JL/ZL-80)
  495mW MAX. Operating(TC514400JL/ZL-10)
  2.2mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package Plastic SOJ: TC514400JL
  Plastic ZIP: TC514400ZL

PIN CONNECTION

Plastic SOJ



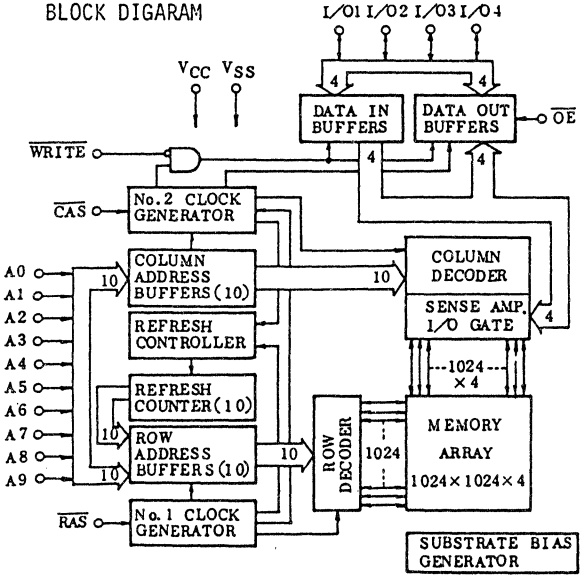
Plastic ZIP



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIGARAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ~ 7	V	1
Output Voltage	V_{OUT}	-1 ~ 7	V	1
Power Supply Voltage	V_{CC}	-1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	-55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C·sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514400JL/ZL-80	-	105	mA	3,4,5
		TC514400JL/ZL-10	-	90		
I_{CC2}	Standby Current Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514400JL/ZL-80	-	105	mA	3,5
		TC514400JL/ZL-10	-	90		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC514400JL/ZL-80	-	70	mA	3,4,5
		TC514400JL/ZL-10	-	60		
I_{CC5}	Standby Current Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	400	µA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514400JL/ZL-80	-	105	mA	3
		TC514400JL/ZL-10	-	90		
I_{CC7}	Battery Back Up Current Average Power Supply Current, Battery Back Up Mode ($\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$=V_{CC}-0.2V, $\overline{WRITE}$=V_{CC}-0.2V, A0 ~ 9=V_{CC}-0.2V or 0.2V, I/O1 ~ 4=V_{CC}-0.2V, 0.2V or OPEN: t_{RC}=125µs, t_{RAS}=t_{RAS} MIN. ~ 1µs)		-	500	µA	3,6
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	µA	
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	Output Level Outtut "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ~ 70°C)(Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514400JL/ZL-80		TC514400JL/ZL-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	205	-	245	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	60	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	105	-	125	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	ns	10.15.16
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	10,15
t_{AA}	Access Time from Column Address	-	40	-	50	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	55	ns	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	-	55	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514400JL/ ZL-80		TC514400JL/ ZL-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	12
t_{WCH}	Write Command Hold Time	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	13
t_{DH}	Data Hold Time	15	-	20	-	ns	13
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	128	-	128	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	60	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	110	-	135	-	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	70	-	85	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time (Fast Page Mode)	75	-	90	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	25	-	ns	
t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	20	0	20	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	25	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC514400JL/ ZL-80		TC514400JL/ ZL-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	155	-	185	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	105	ns	10.15.16
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	30	ns	10,15
t_{AA}	Access Time from Column Address	-	45	-	55	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	60	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	105	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	50	-	60	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (I/O1 ~ I/O4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified value are obtained with the output open.

5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.

6. t_{RAS}(max.)=1μs is only applied to refresh of battery-back up. t_{RAS}(max.)=10μs is applied to functional operating.

7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

8. AC measurements assume t_T=5ns.

9. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

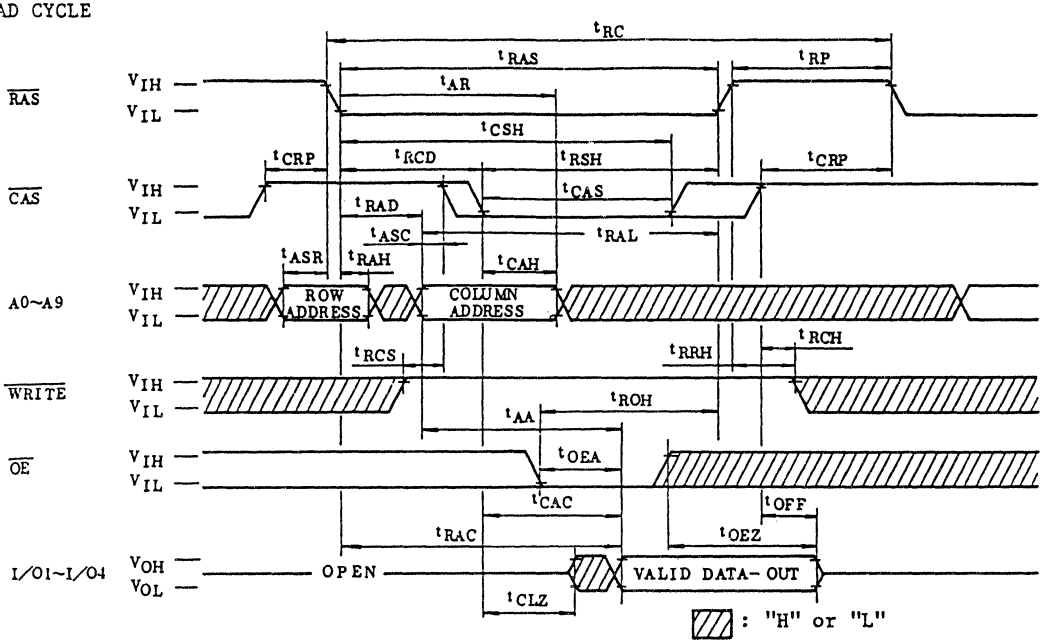
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.

14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPWD} \geq t_{CPWD}$(min.) (Fast Page Mode), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

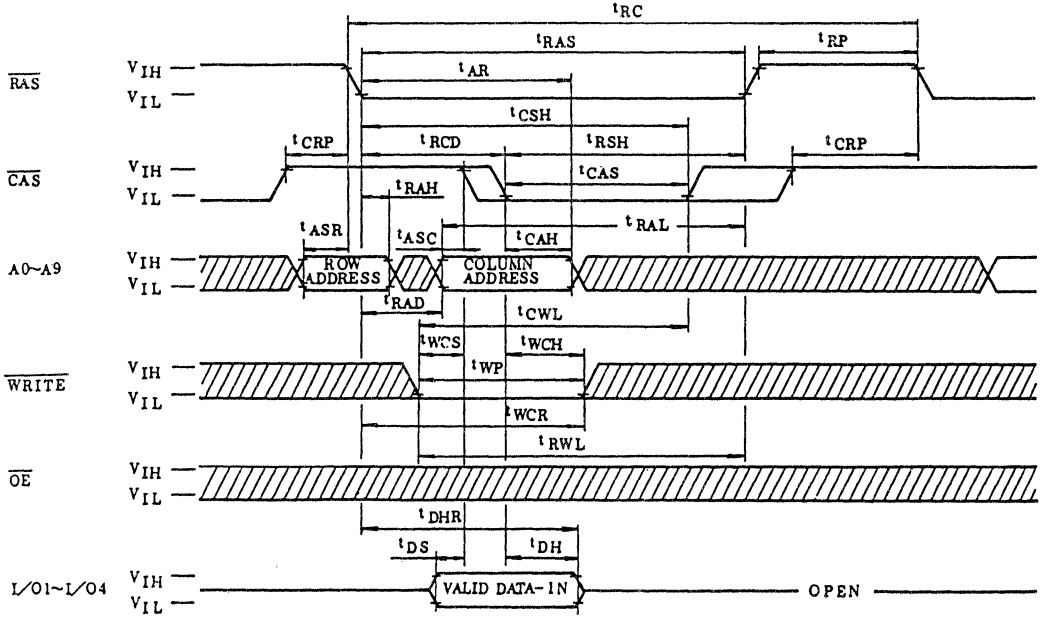
15. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

16. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

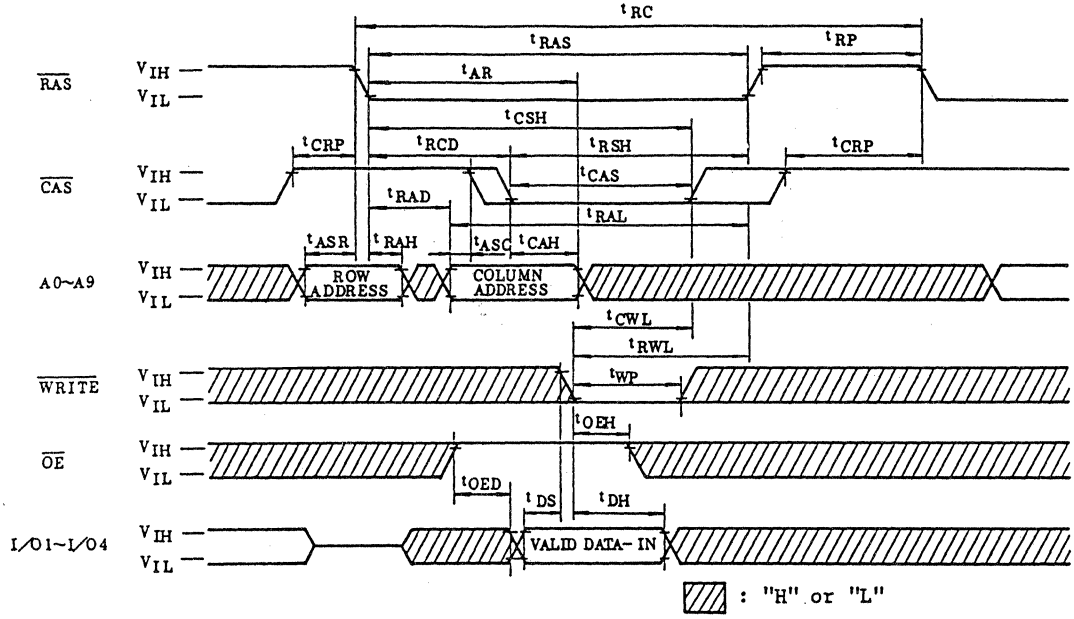
READ CYCLE



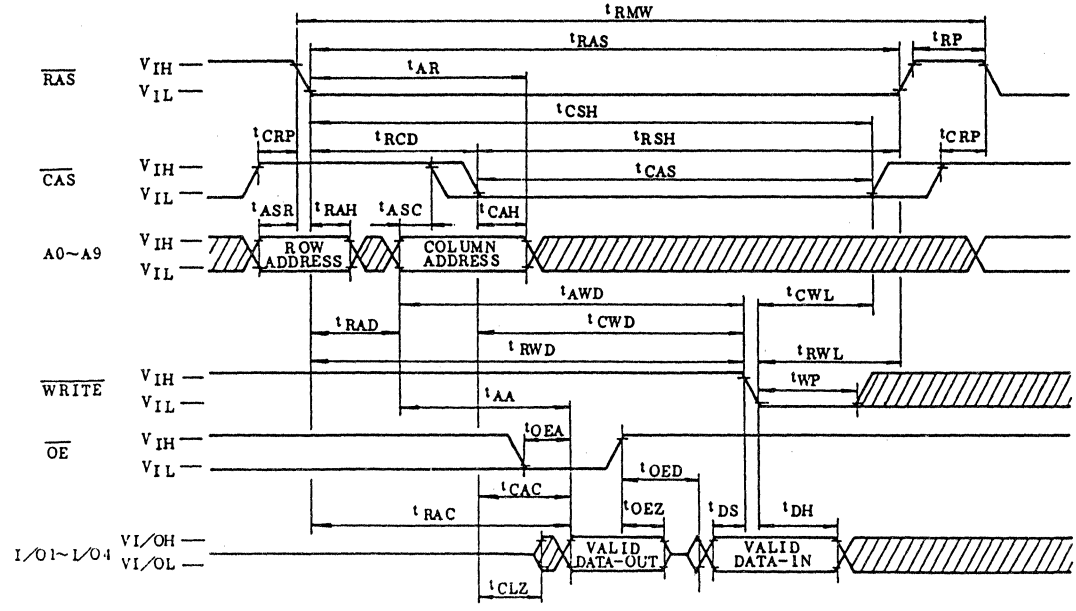
WRITE CYCLE (EARLY WRITE)



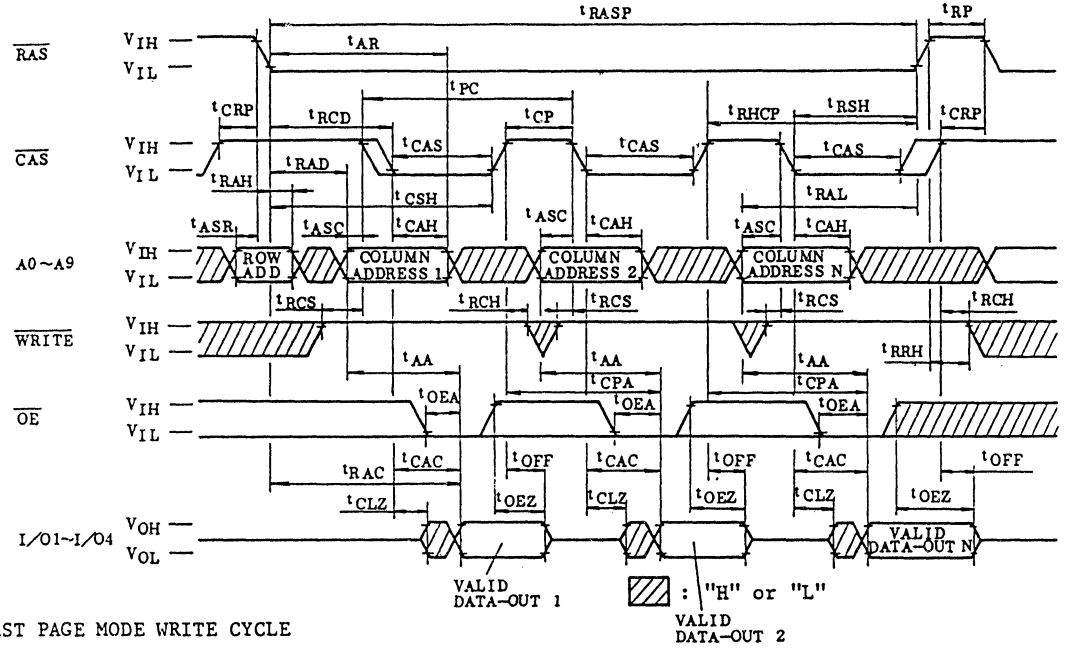
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



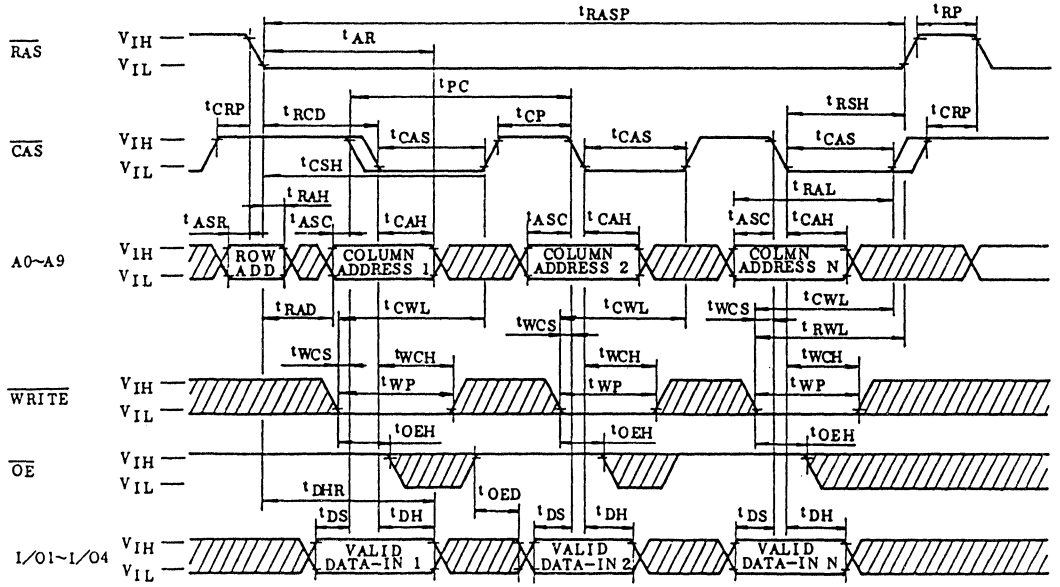
READ-MODIFY-WRITE CYCLE



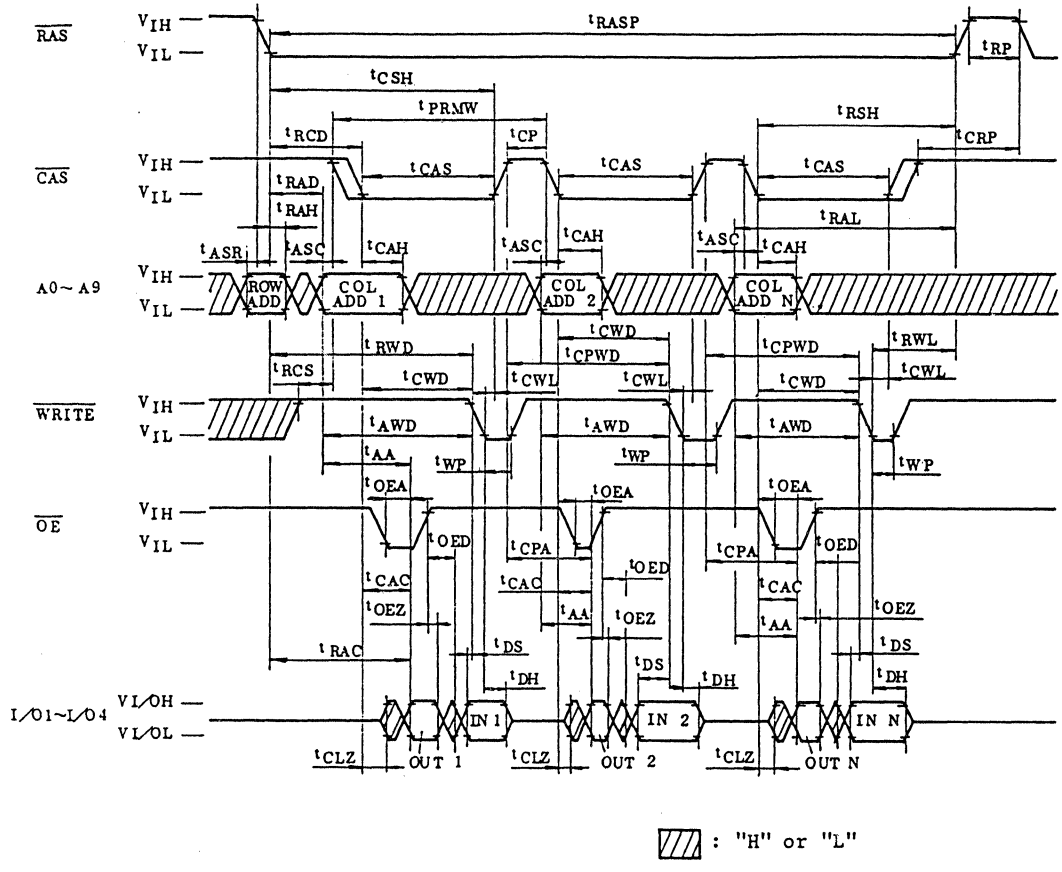
FAST PAGE MODE READ CYCLE



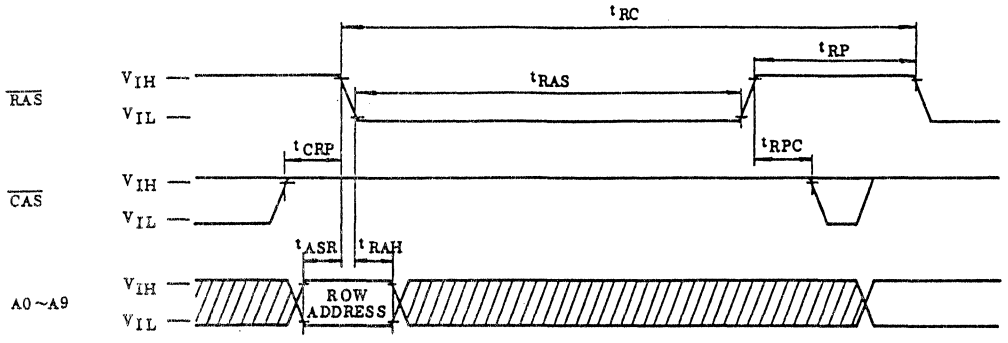
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

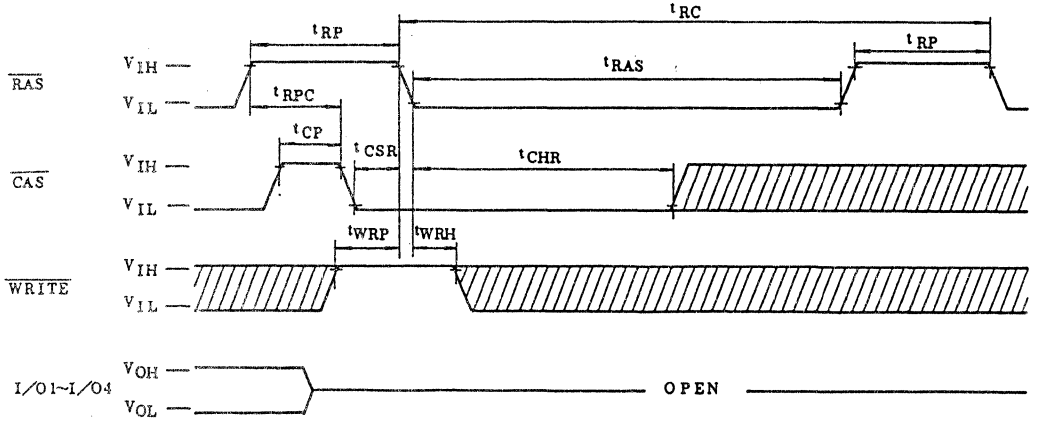


$\overline{RAS}$ ONLY REFRESH CYCLE



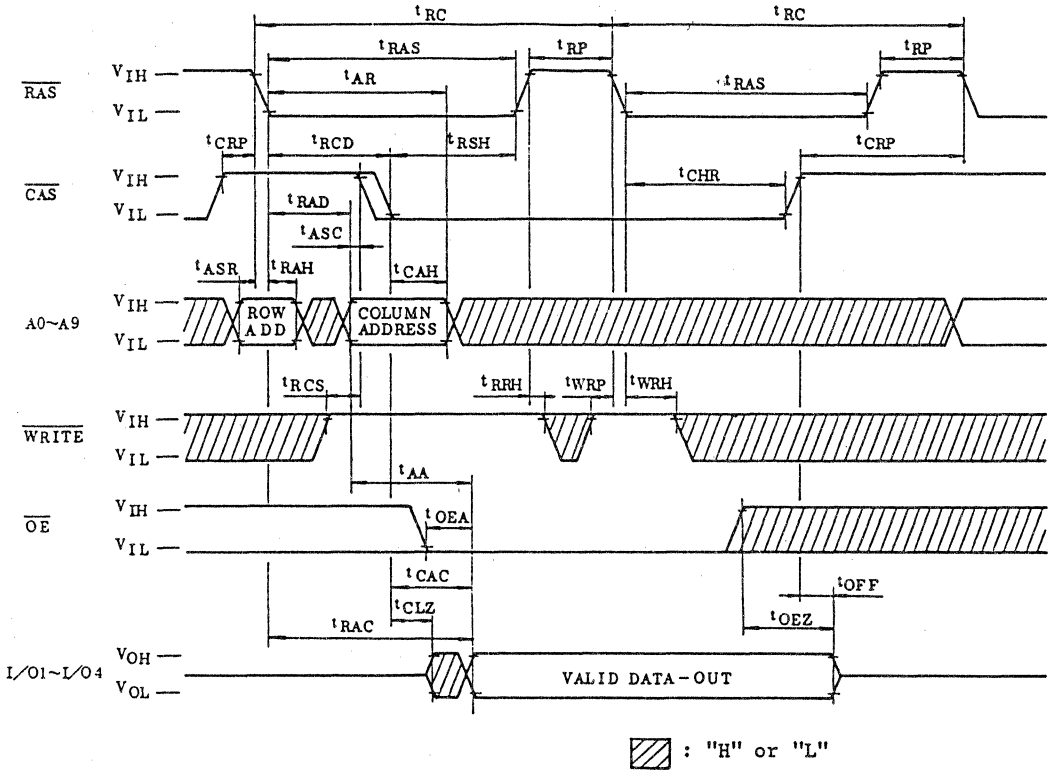
Note: $\overline{WRITE}$, $\overline{OE}$="H" or "L" ▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

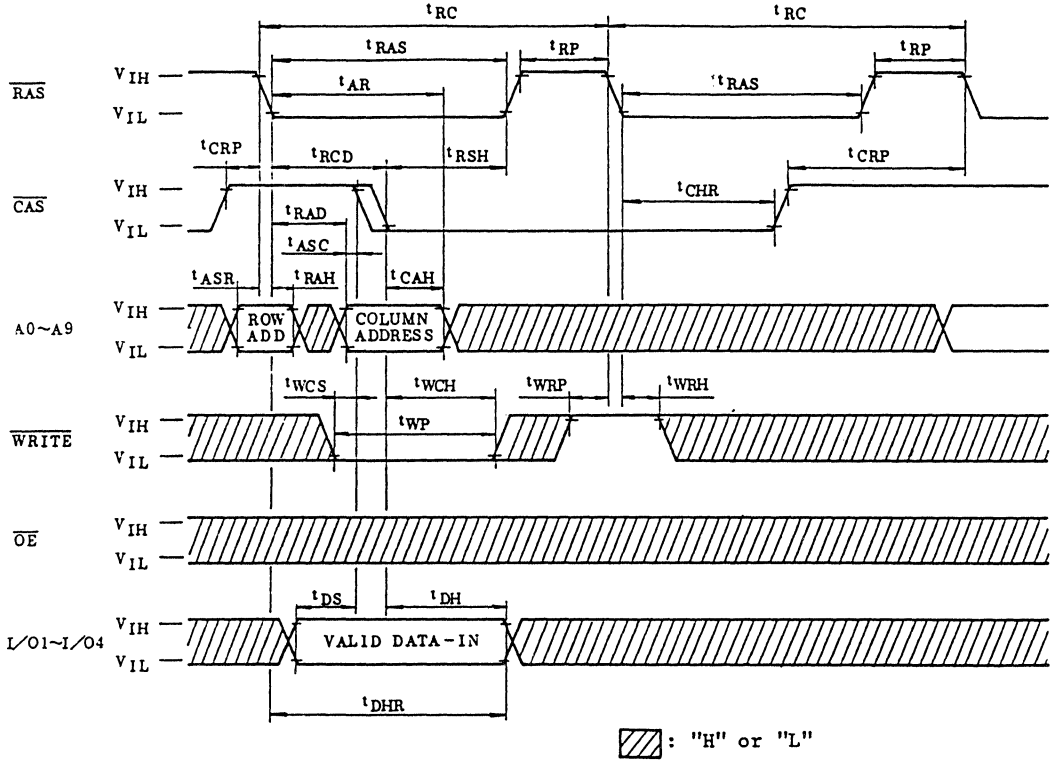


Note: $\overline{OE}$, A0 ∿ A9="H" or "L" ▨ : "H" or "L"

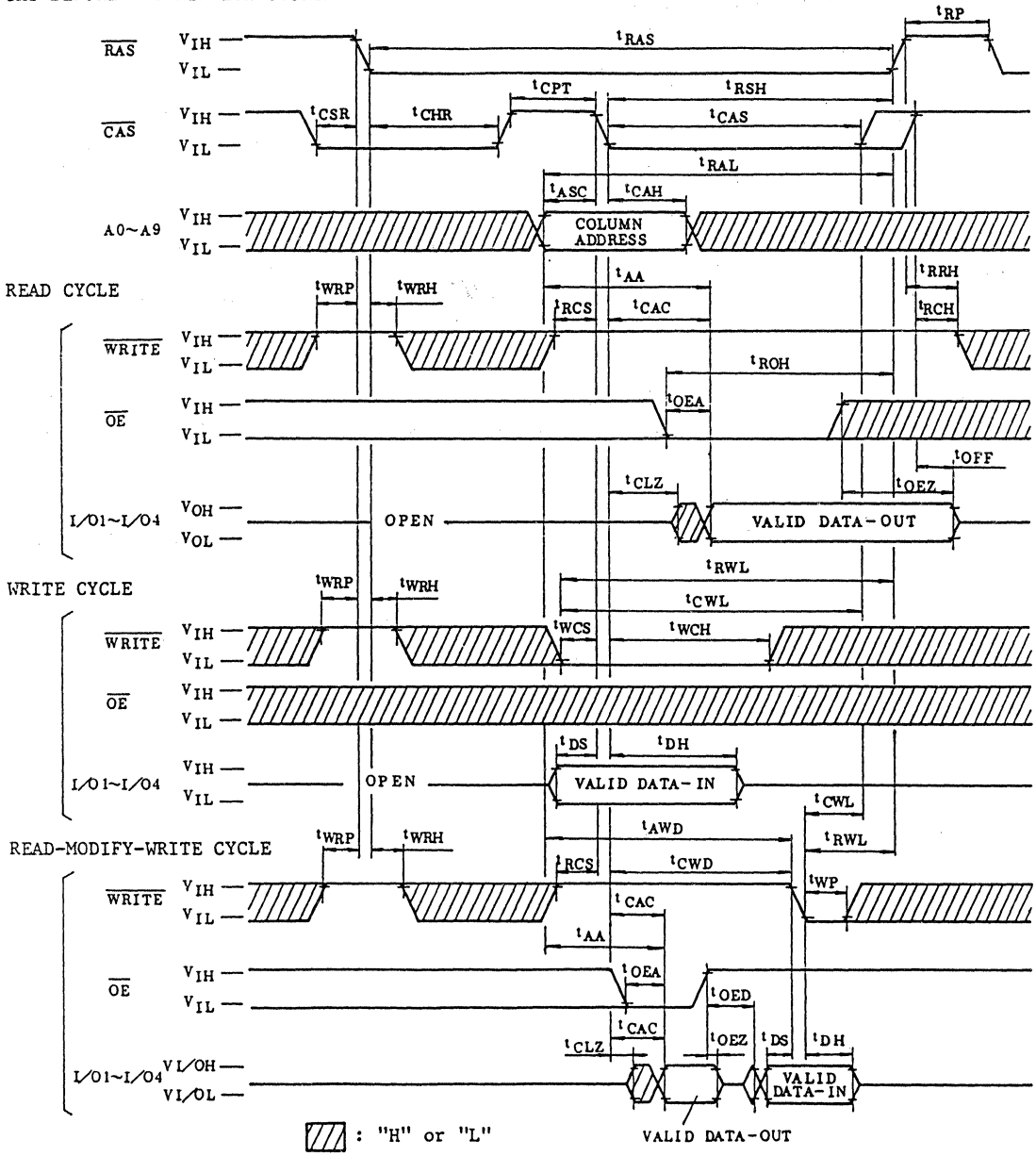
HIDDEN REFRESH CYCLE (READ)



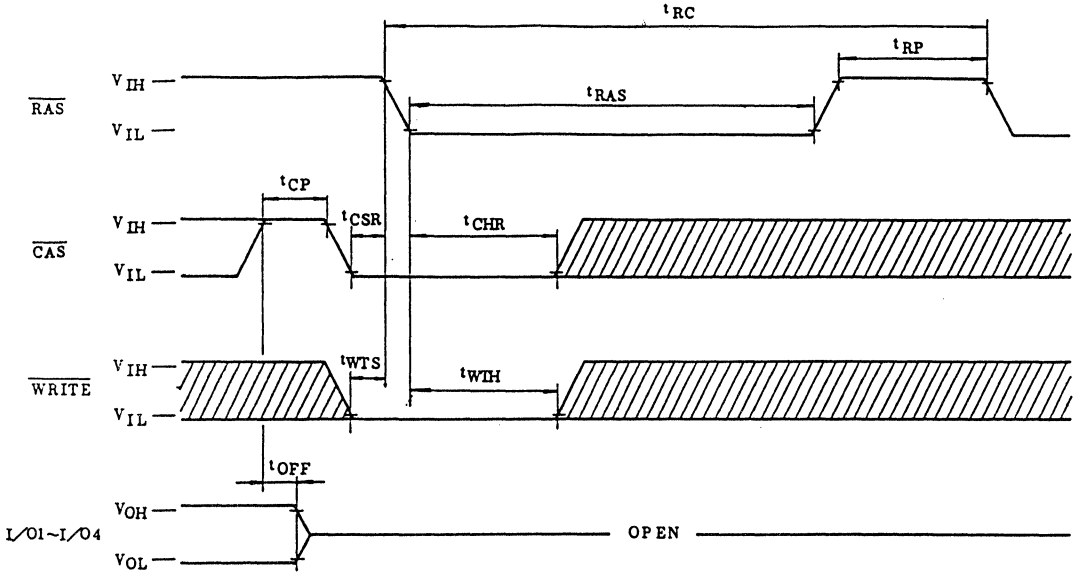
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

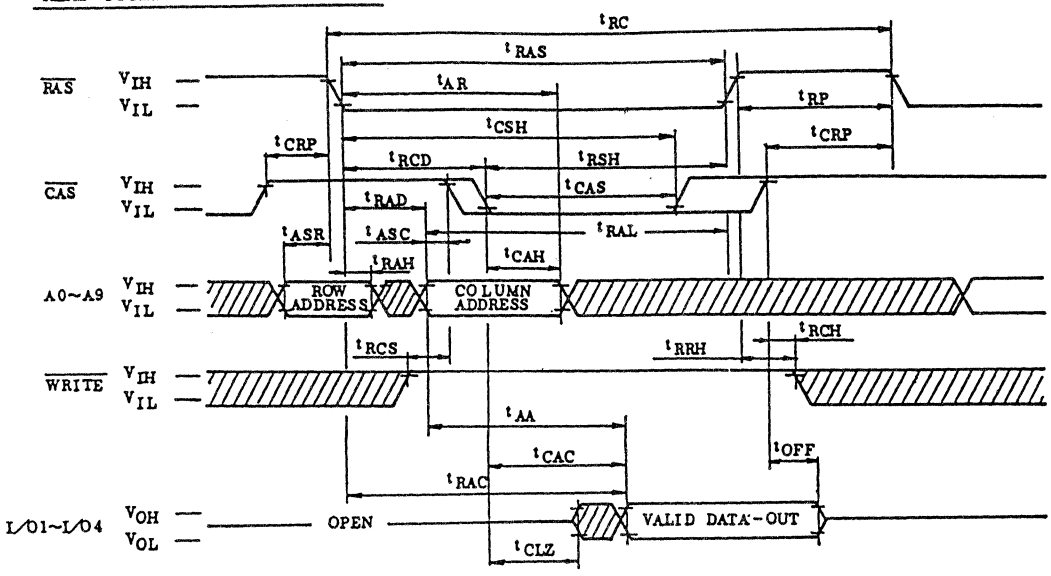


$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



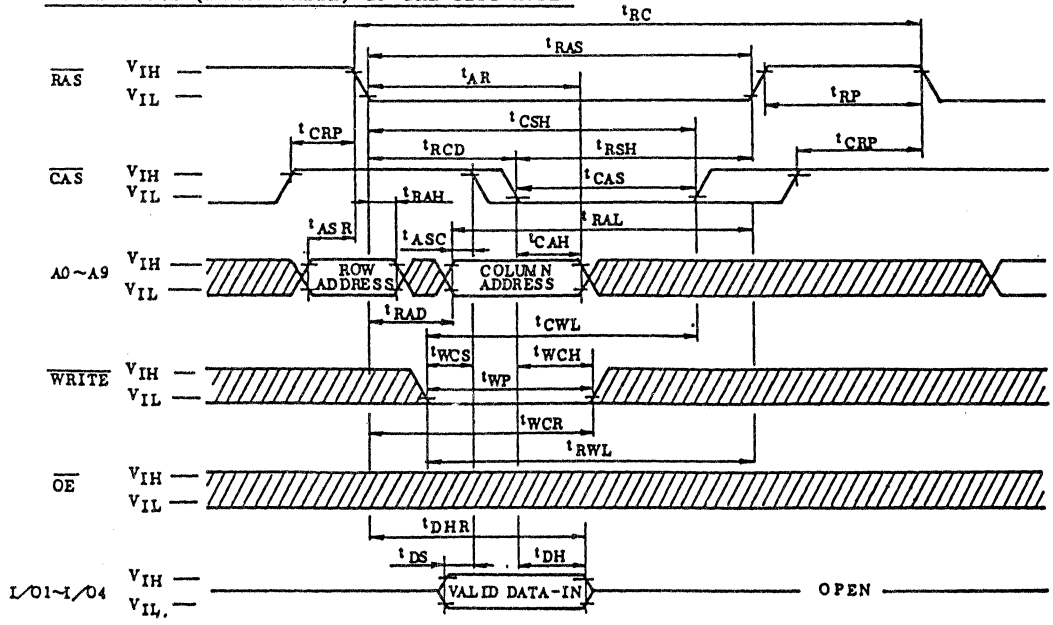
Note: $\overline{\text{OE}}$, A0 ~ A9: "H" or "L" ▨: "H" or "L"

READ CYCLE IN THE TEST MODE

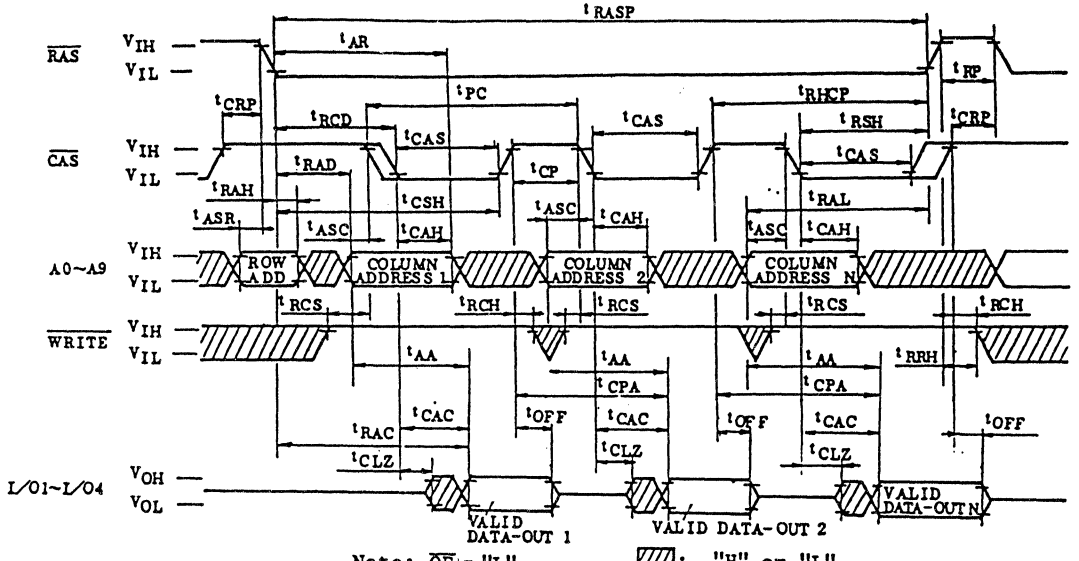


Note: $\overline{OE}$= "L" ▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE) IN THE TEST MODE

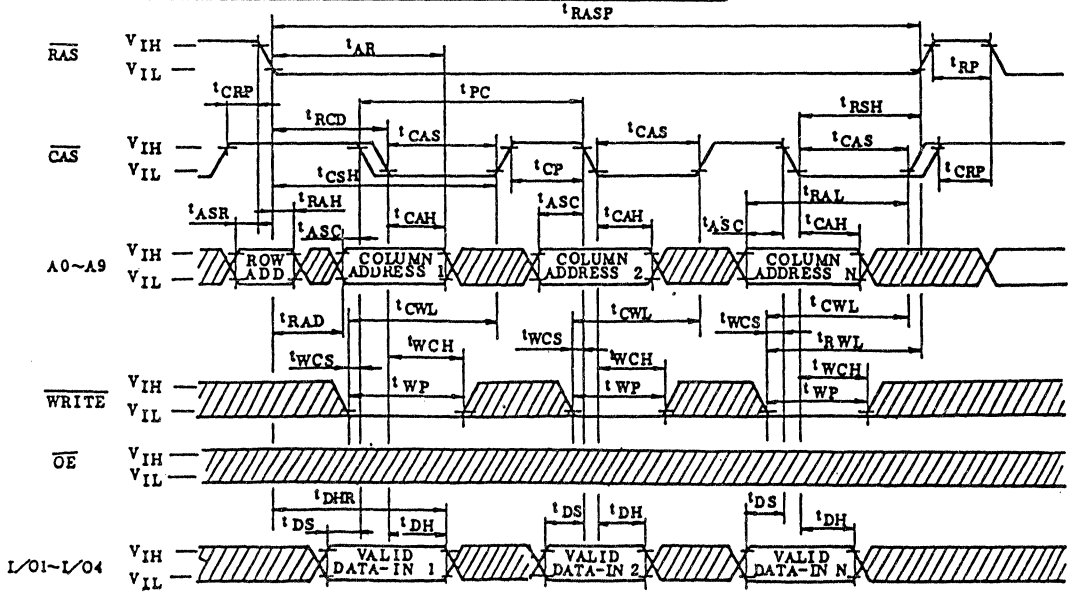


FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note: $\overline{OE}$ = "L" ▨: "H" or "L"

FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



TEST MODE

The TC514400JL/ZL is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{0C} is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".
If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514400JL/ZL. In "Test Mode", the 1M × 4 DRAM can be tested as if it were a 512K × 4 DRAM.
"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test patterns).

BLOCK DIAGRAM IN THE TEST MODE

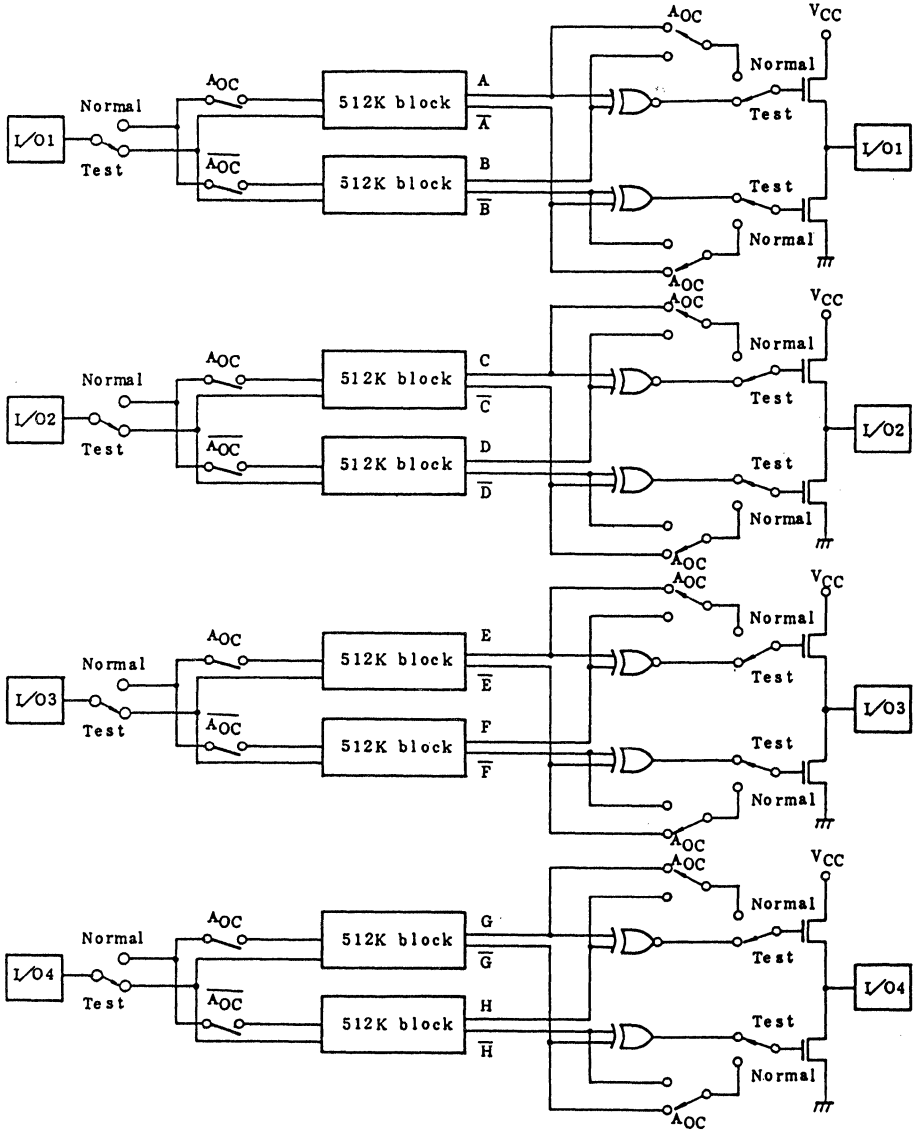


Fig. 1

NOTES

1,048,576 WORD ×4 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514400AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514400AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514400AP/AJ/ASJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

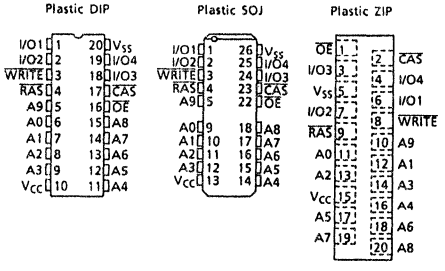
		TC514400AP/AJ/ASJ/AZ-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  660mW MAX. Operating (TC514400AP/AJ/ASJ/AZ-60)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC514400AP : DIP20-P-300C
  TC514400AJ : SOJ26-P-350
  TC514400ASJ : SOJ26-P-300A
  TC514400AZ : ZIP20-P-400A

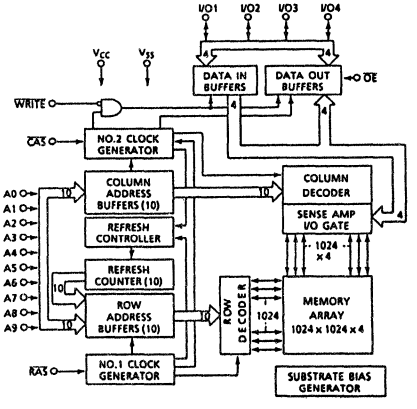
PIN NAMES

A0~A9	Address Inputs	$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe	I/O1~I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
$\overline{WRITE}$	Read/Write Input	V_{SS}	Ground

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514400AP/AJ/ ASJ/AZ-60	–	120	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC514400AP/AJ/ ASJ/AZ-60	–	120	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	TC514400AP/AJ/ ASJ/AZ-60	–	70	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514400AP/AJ/ ASJ/AZ-60	–	120	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514400AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	20	ns	9,14
t_{AA}	Access Time from Column Address	–	30	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514400AP/AJ/ASJ/AZ-60		UNITS	NOTES
		MIN.	MAX.		
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	12
t_{DH}	Data Hold Time	15	–	ns	12
t_{REF}	Refresh Period	–	16	ms	
t_{WCS}	Write Command Set-Up Time	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	–	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC514400AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	115	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	65	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	45	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	ns	

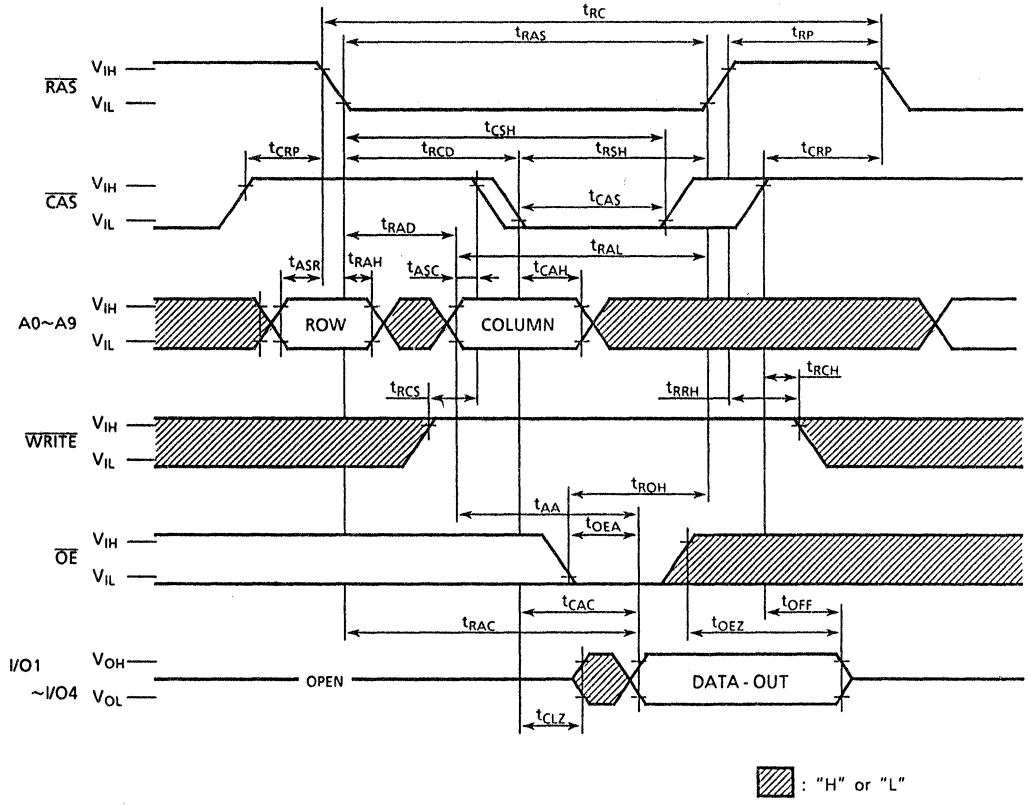
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/01~I/04)	–	7	pF

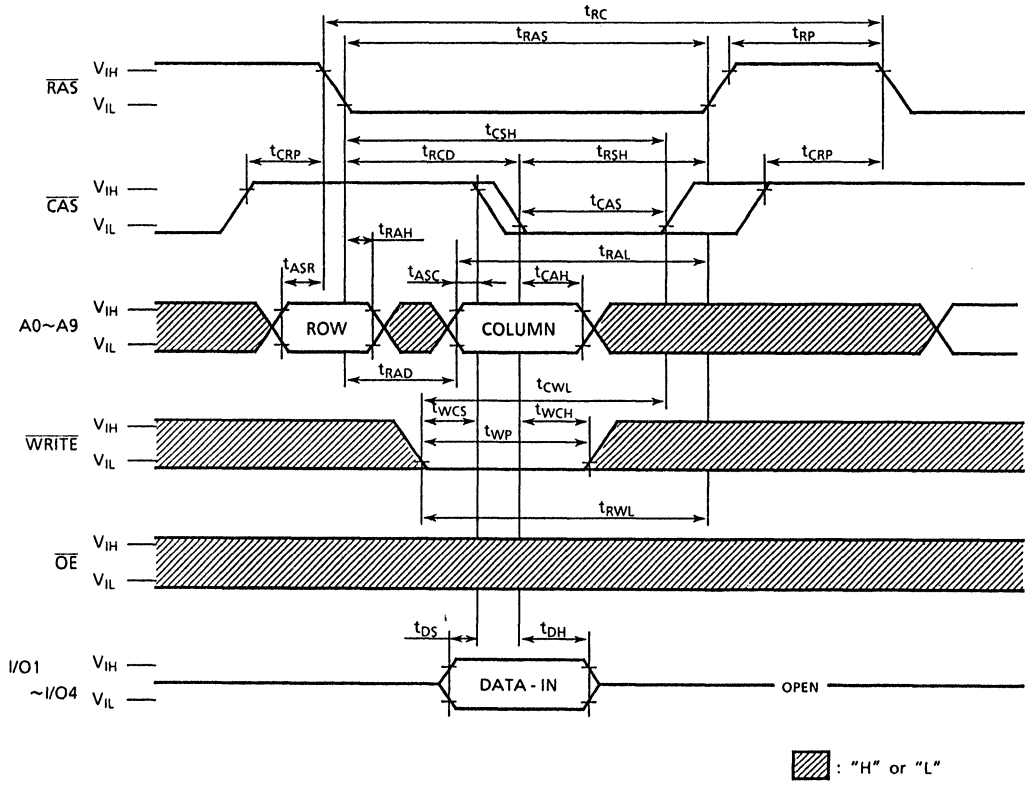
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

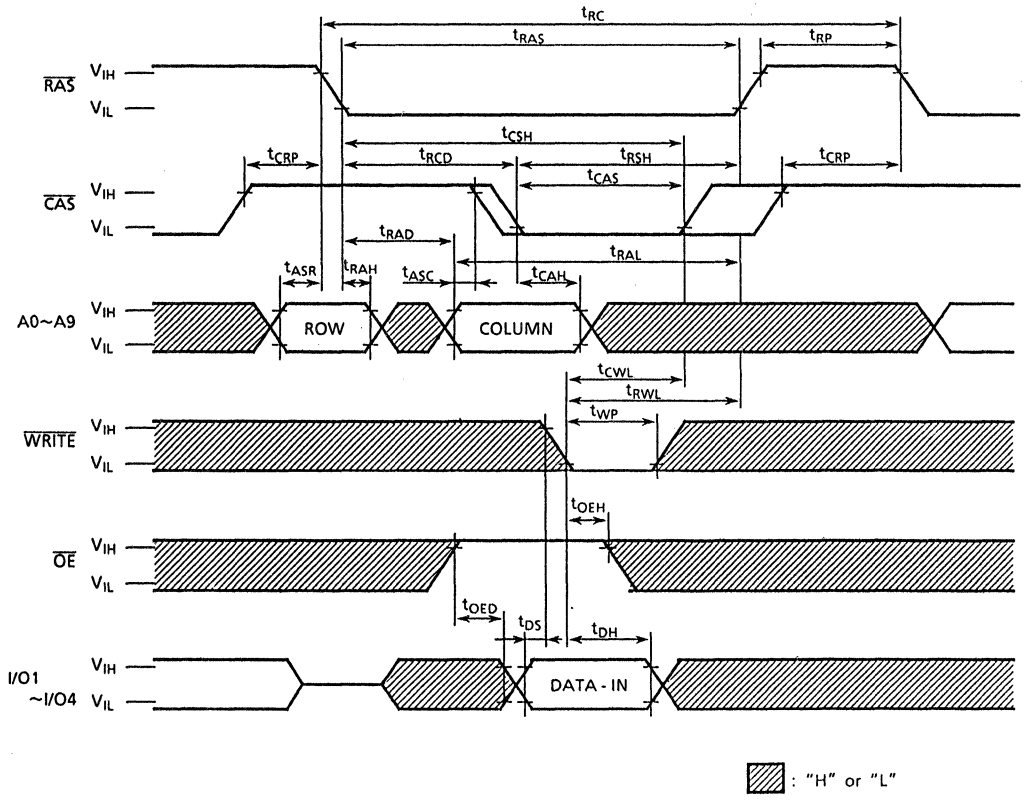
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tROH
tAA
tOEA
OE
tCAC
tOFF
tRAC
tOEZ
I/O1
~I/O4
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

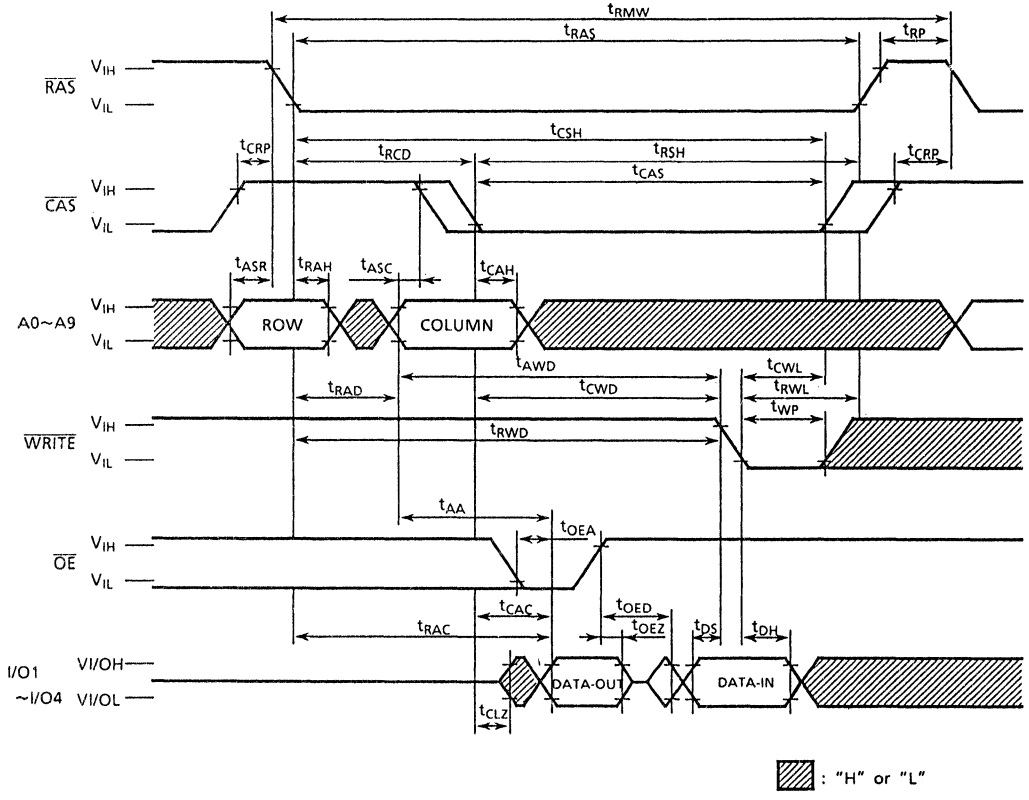
WRITE CYCLE (EARLY WRITE)



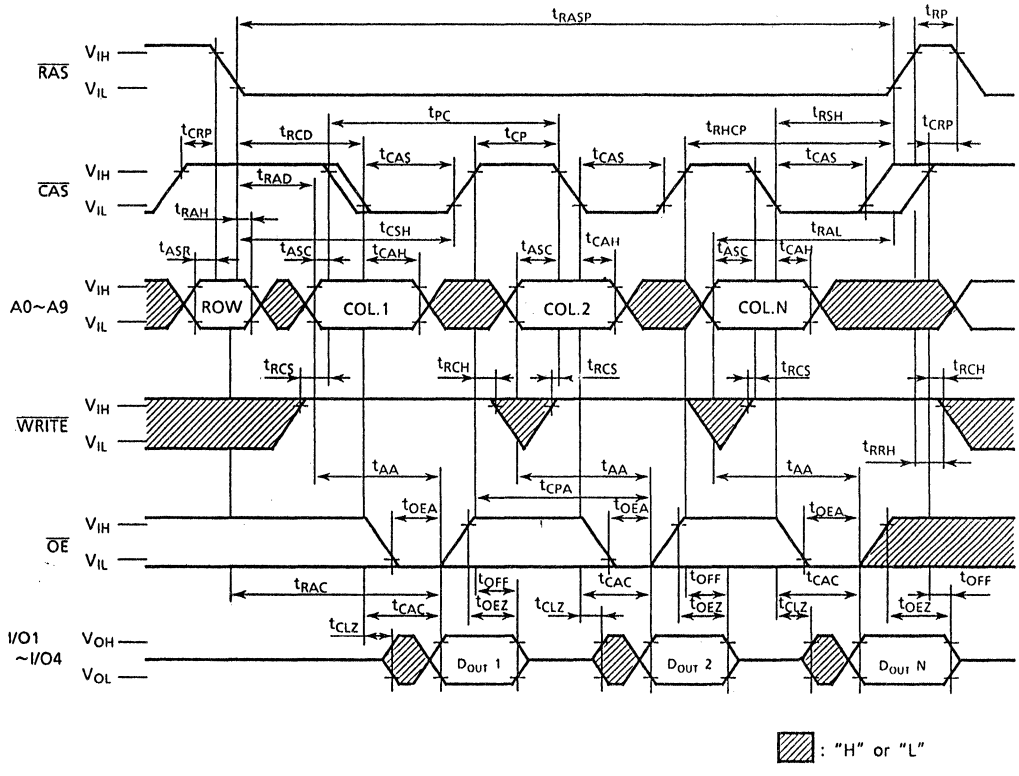
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



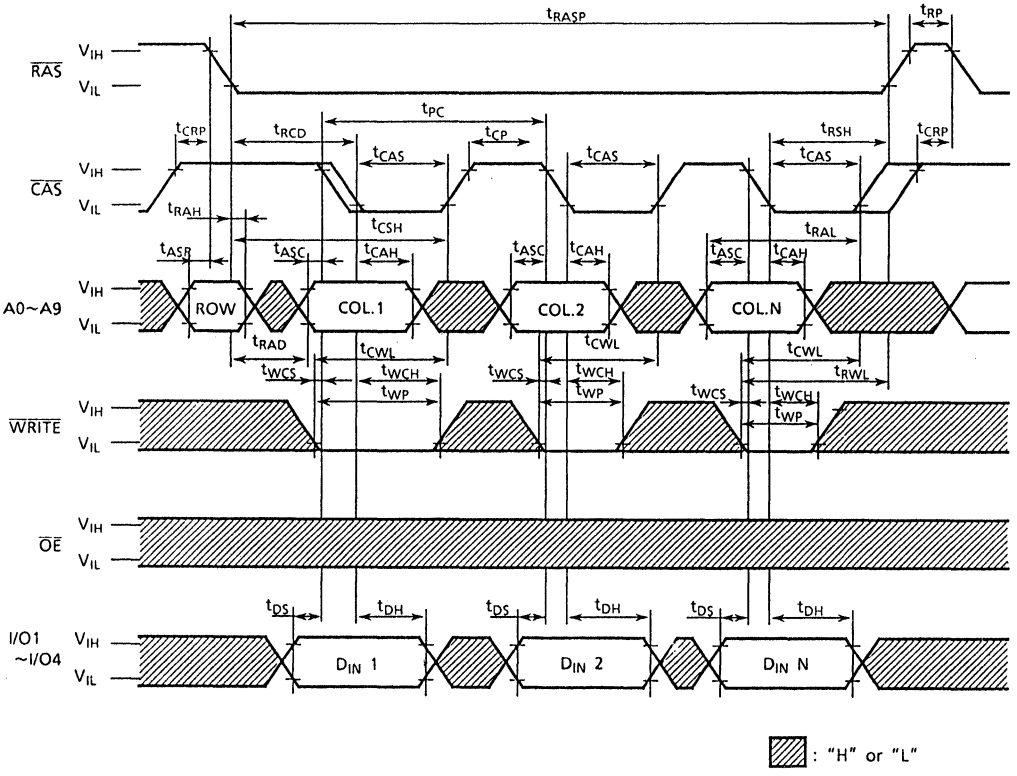
READ-MODIFY-WRITE CYCLE



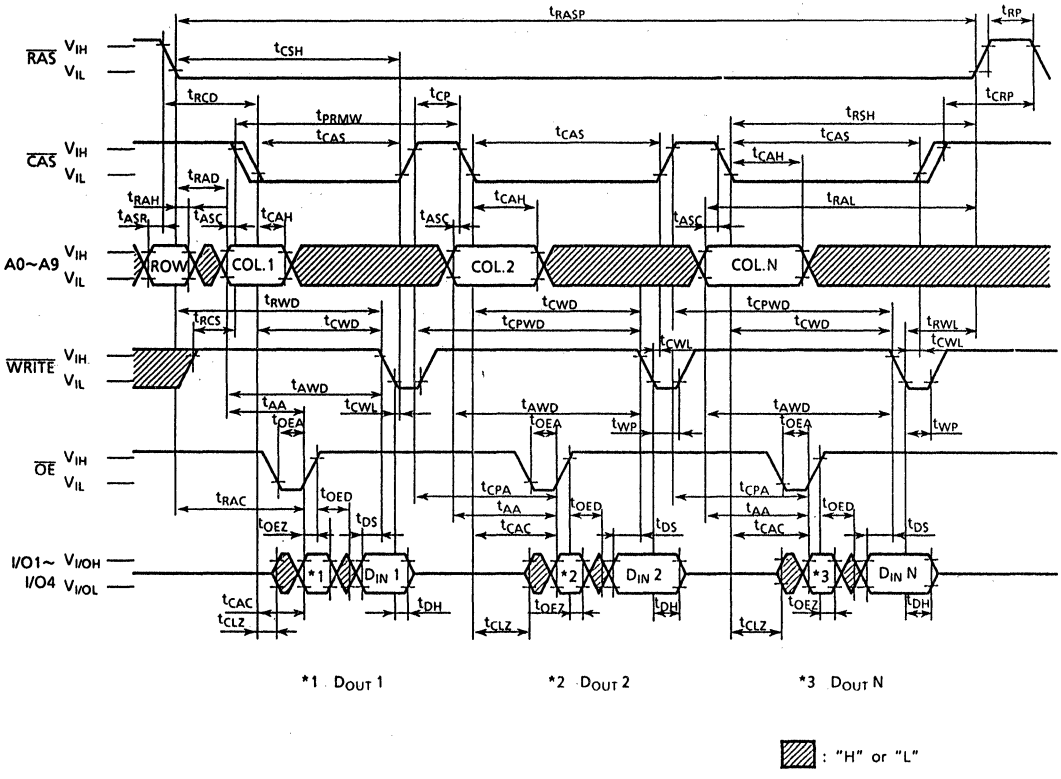
FAST PAGE MODE READ CYCLE



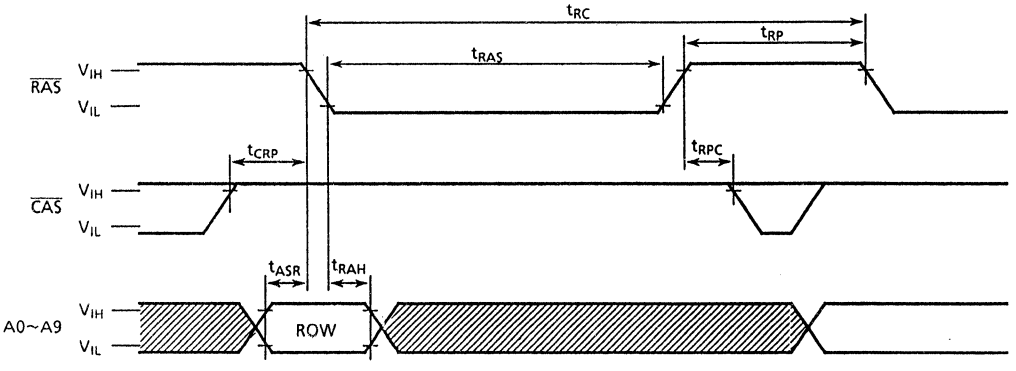
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



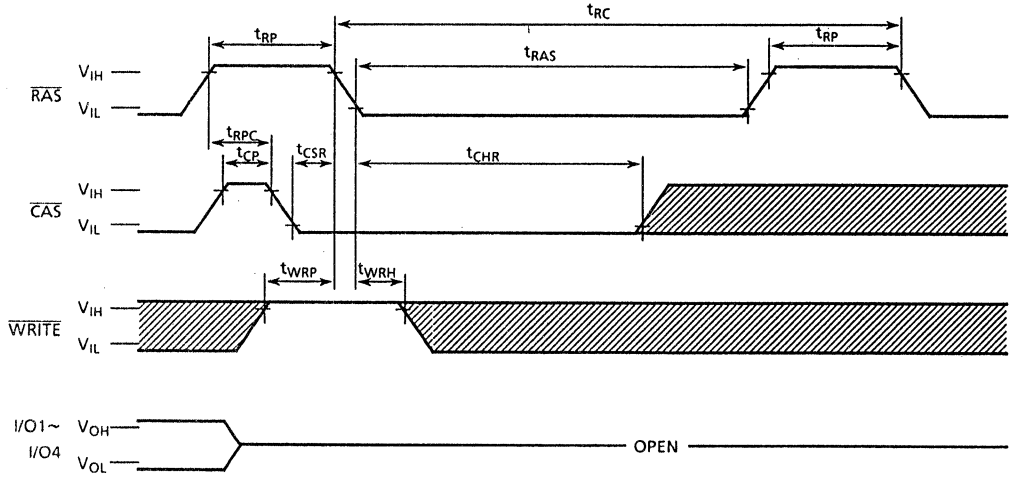
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

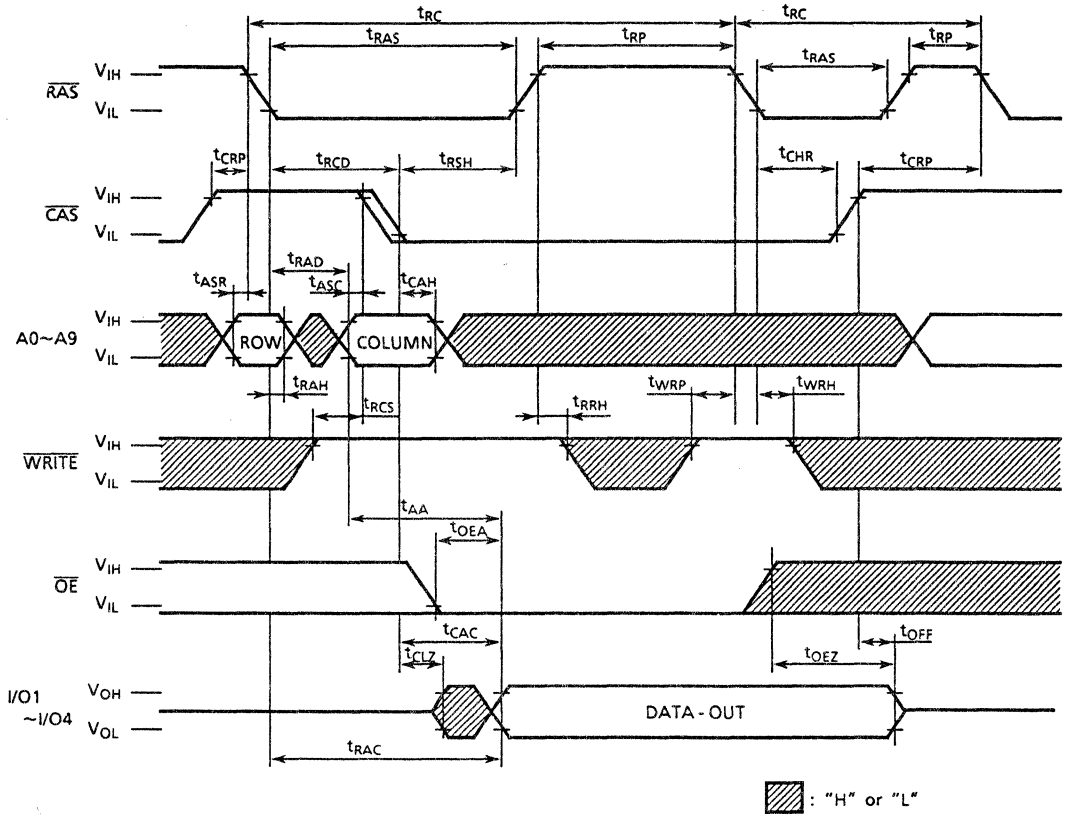
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



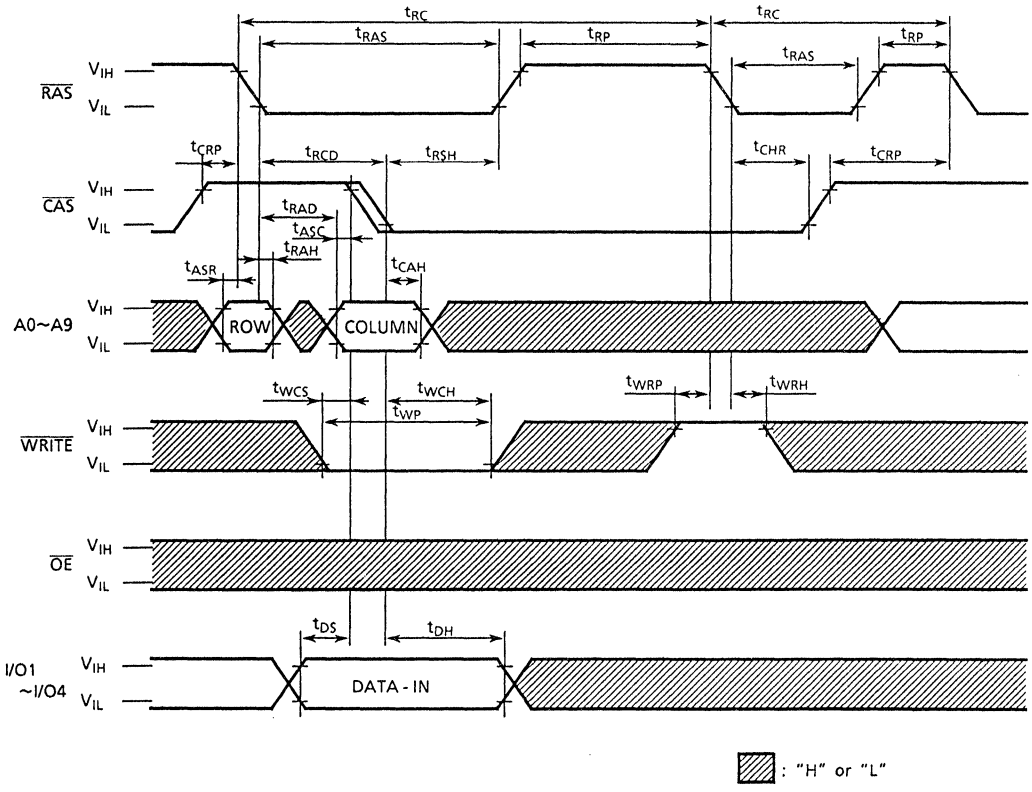
Note: $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

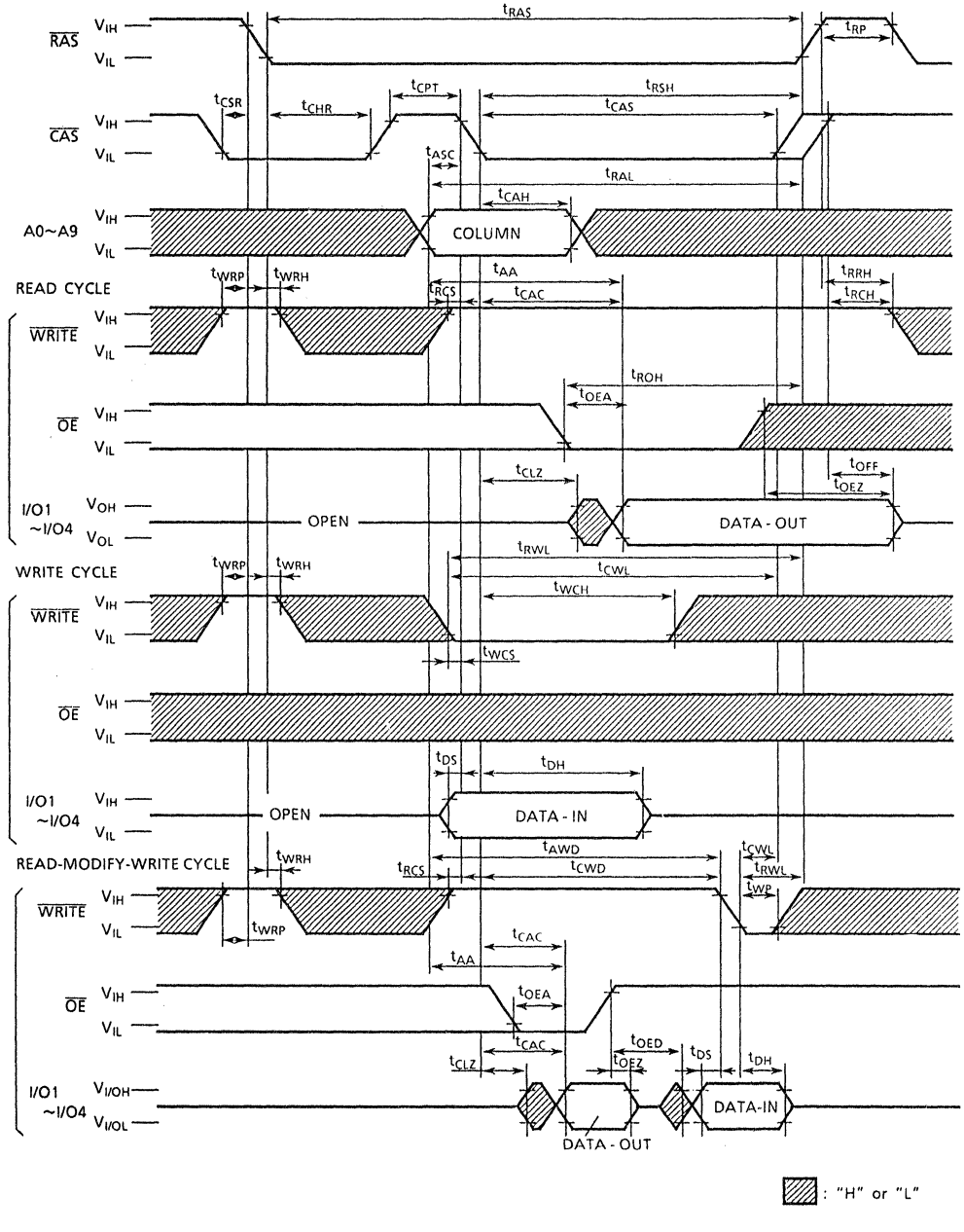
HIDDEN REFRESH CYCLE (READ)



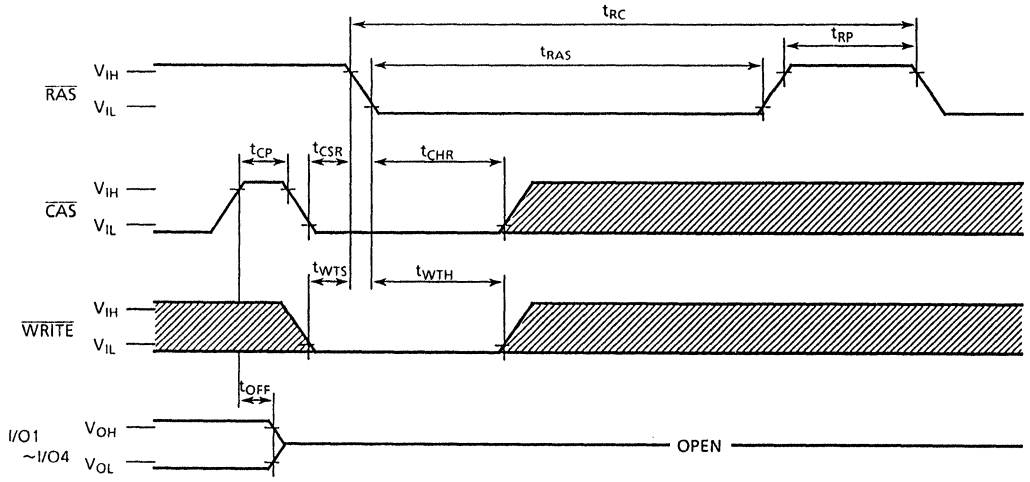
HIDDEN REEFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, CAS BEFORE RAS REFRESH CYCLE



Note: $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC514400AP/AJ/ASJ/AZ is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A0c is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".

If they were not equal, the I/O pin would indicate a "0". Fig.1 shows the block diagram of TC514400AP/AJ/ASJ/AZ. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

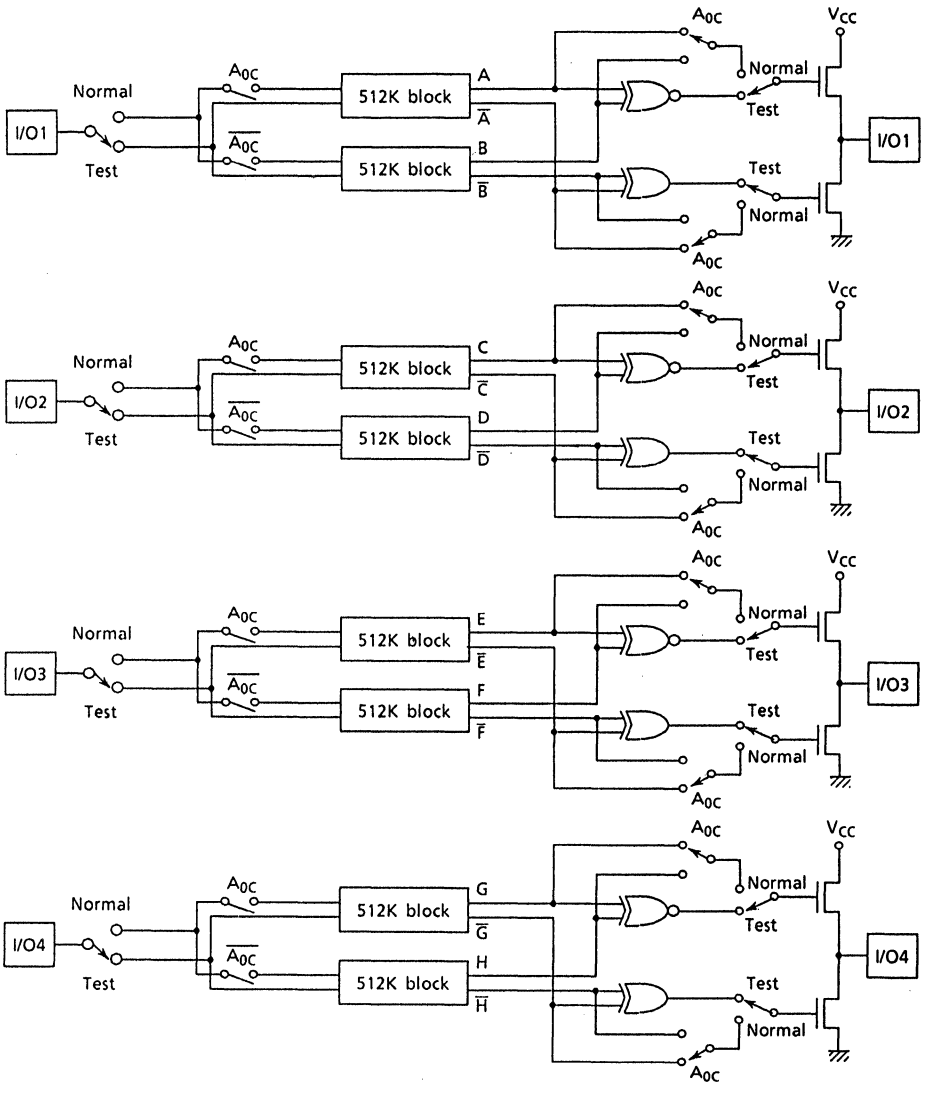


Fig. 1

NOTES

1,048,576 WORD ×4 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514400APL/AJL/ASJL/AZL is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514400APL/AJL/ASJL/AZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514400APL/AJL/ASJL/AZL to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

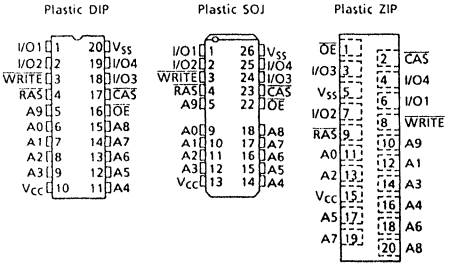
		TC514400APL/AJL/ASJL/AZL-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  660mW MAX. Operating (TC514400APL/AJL/ASJL/AZL-60)
  1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514400APL : DIP20-P-300C
  TC514400AJL : SOJ26-P-350
  TC514400ASJL: SOJ26-P-300A
  TC514400AZL : ZIP20-P-400A

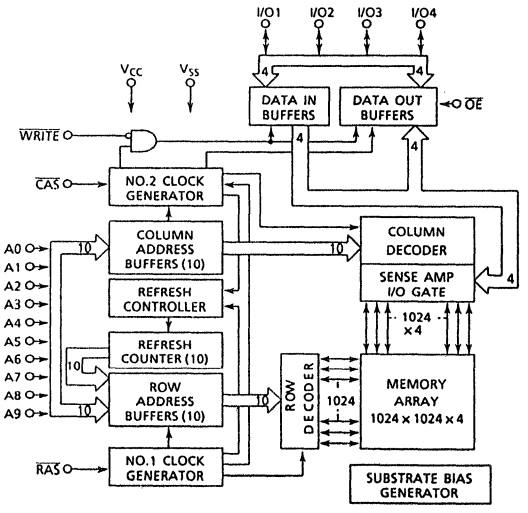
PIN NAMES

A0~A9	Address Inputs	$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe	I/O1~I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
$\overline{WRITE}$	Read/Write Input	V_{SS}	Ground

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514400APL/AJL/ASJL/AZL-60	–	120	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514400APL/AJL/ASJL/AZL-60	–	120	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514400APL/AJL/ASJL/AZL-60	–	70	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514400APL/AJL/ASJL/AZL-60	–	120	mA	3, 5
I_{CC7}	Battery Back Up Current Average Power Supply Current, Battery Back Up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} – 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V, A0~9 = V_{CC} – 0.2V or 0.2V, I/O1~4 = V_{CC} – 0.2V, 0.2V or OPEN : t_{RC} = 125µs, t_{RAS} = 300ns ~ 1µs)		–	400	µA	3, 6
I_{CC7}	Battery Back Up Current Average Power Supply Current, Battery Back Up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} – 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V, A0~9 = V_{CC} – 0.2V or 0.2V, I/O1~4 = V_{CC} – 0.2V, 0.2V or OPEN : t_{RC} = 125µs, t_{RAS} = t_{RAS} MIN. ~300ns)		–	300	µA	3, 6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514400APL/AJL/ASJL/AZL-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	10,15 16
t_{CAC}	Access Time from $\overline{CAS}$	–	20	ns	10,15
t_{AA}	Access Time from Column Address	–	30	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	ns	10
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514400APL/AJL/ASJL/AZL-60		UNITS	NOTES
		MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	12
t_{WCH}	Write Command Hold Time	10	–	ns	
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	13
t_{DH}	Data Hold Time	15	–	ns	13
t_{REF}	Refresh Period	–	128	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	–	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	ns	
t_{WTS}	Write Commamd Set-Up Time (Test Mode In)	10	–	ns	
t_{WTH}	Write Commamd Hold Time (Test Mode In)	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC514400APL/AJL/ASJL/AZL-60		UNITS	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	115	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	65	ns	10,15 16
t_{CAC}	Access Time from $\overline{CAS}$	–	25	ns	9,15
t_{AA}	Access Time from Column Address	–	35	ns	9,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	ns	10
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	–	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	ns	

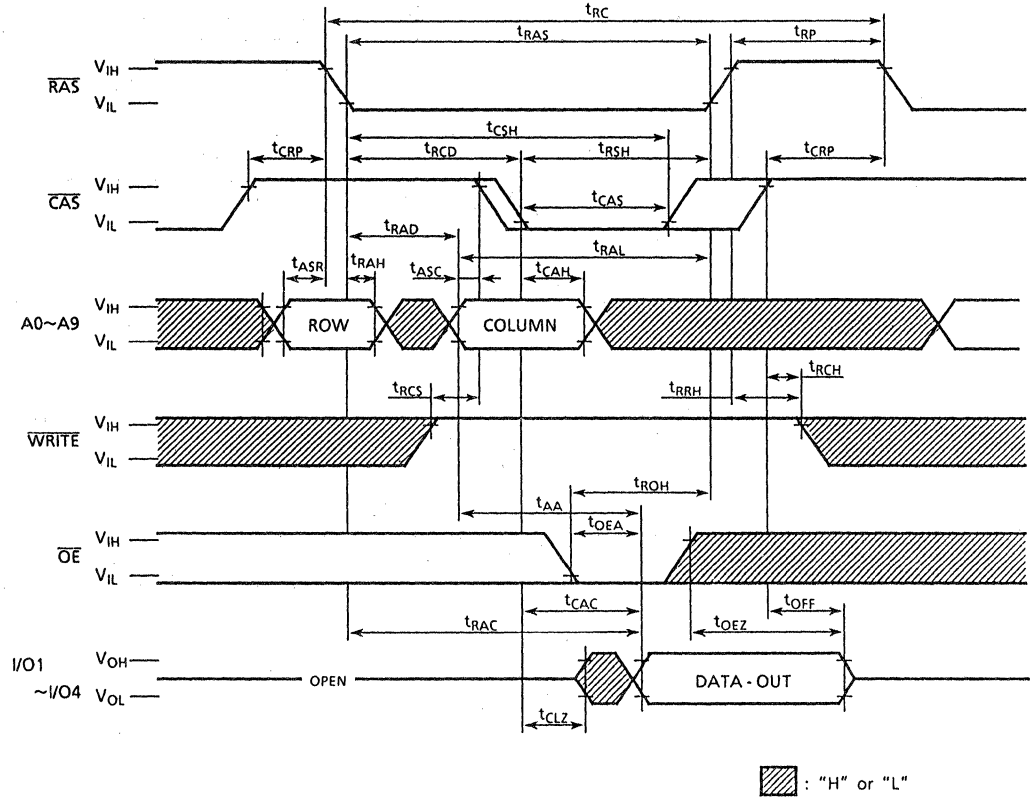
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	–	7	pF

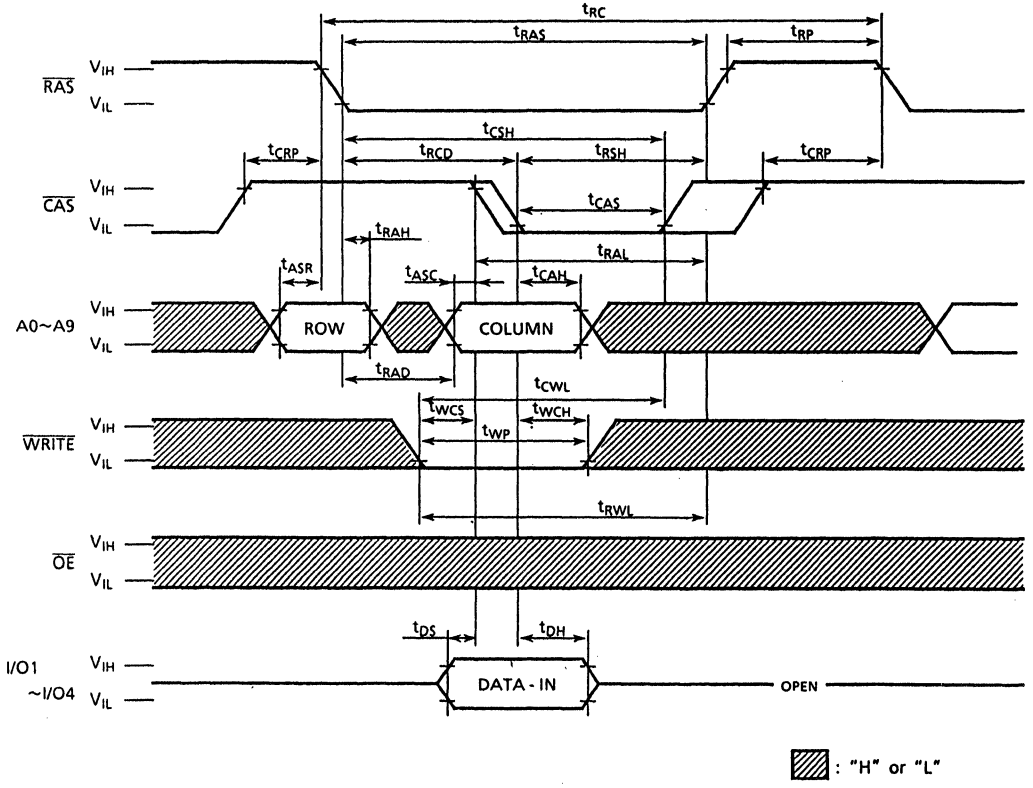
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. t_{RAS}(max.)=1μs is only applied to refresh of battery-back up. t_{RAS}(max.)=10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume t_T=5ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

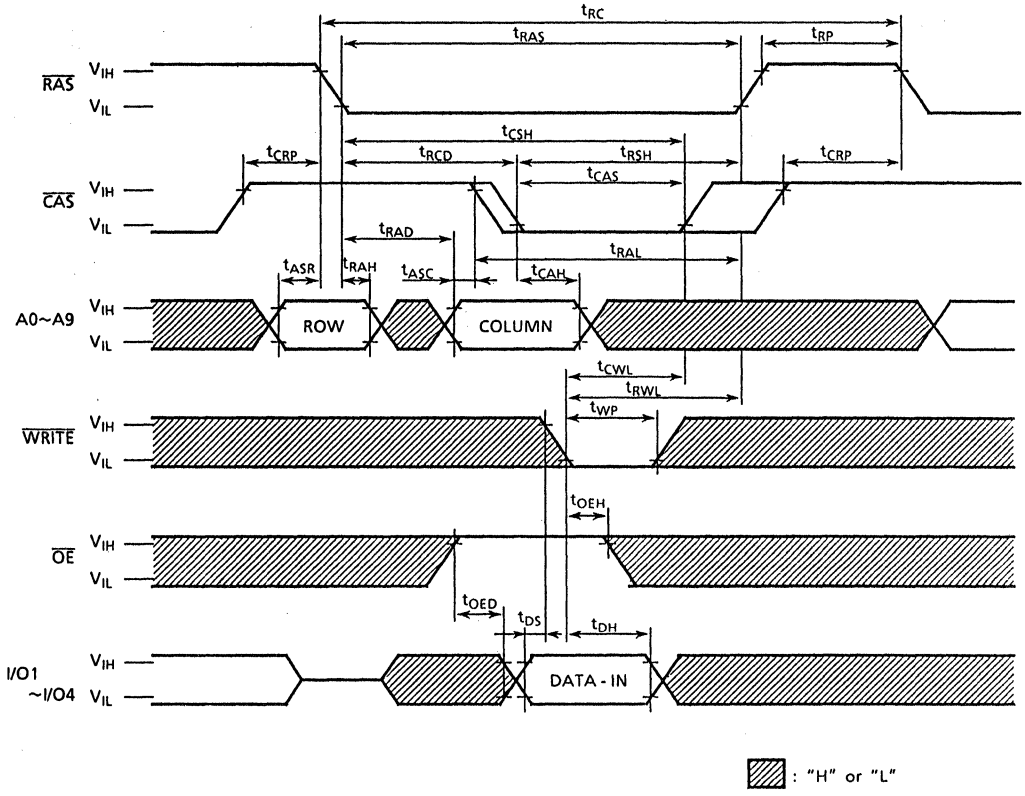
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tROH
tAA
tOEA
OE
tCAC
tOFF
tRAC
tOEZ
I/O1
~I/O4
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

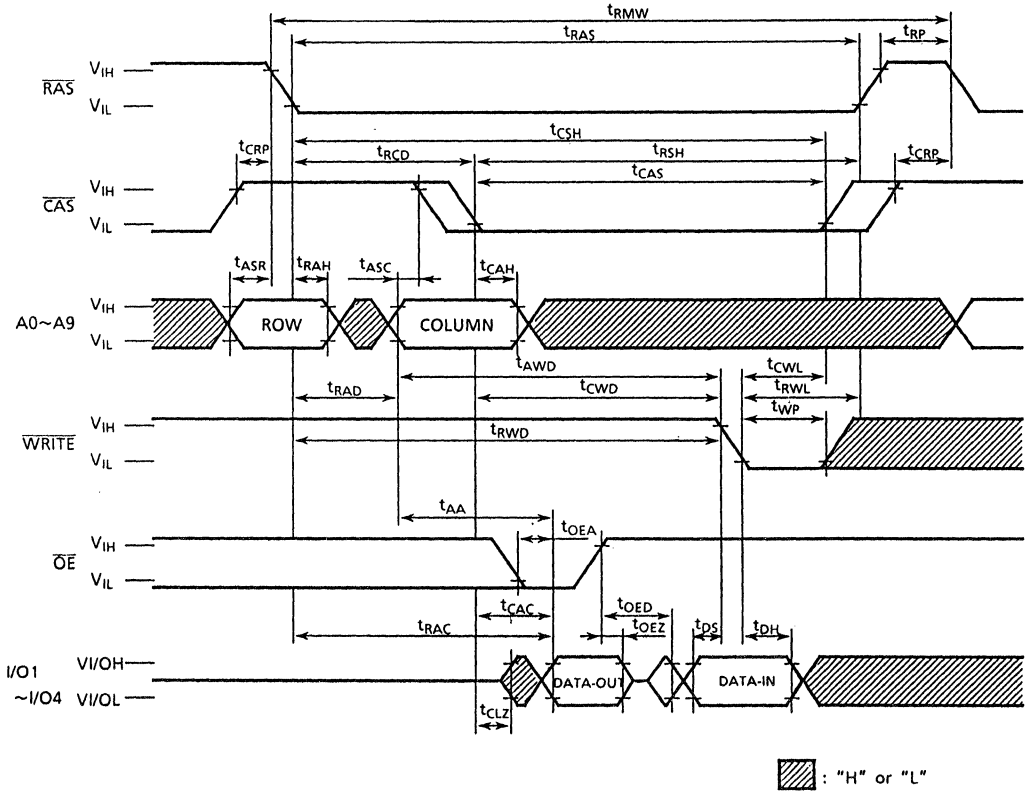
WRITE CYCLE (EARLY WRITE)



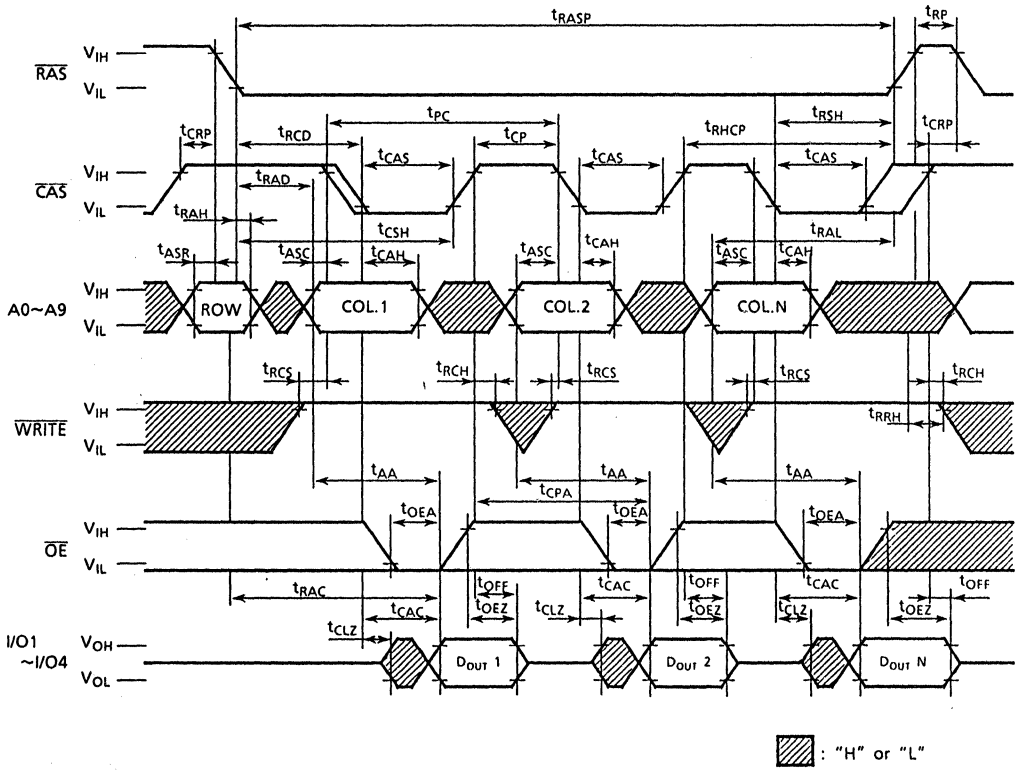
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



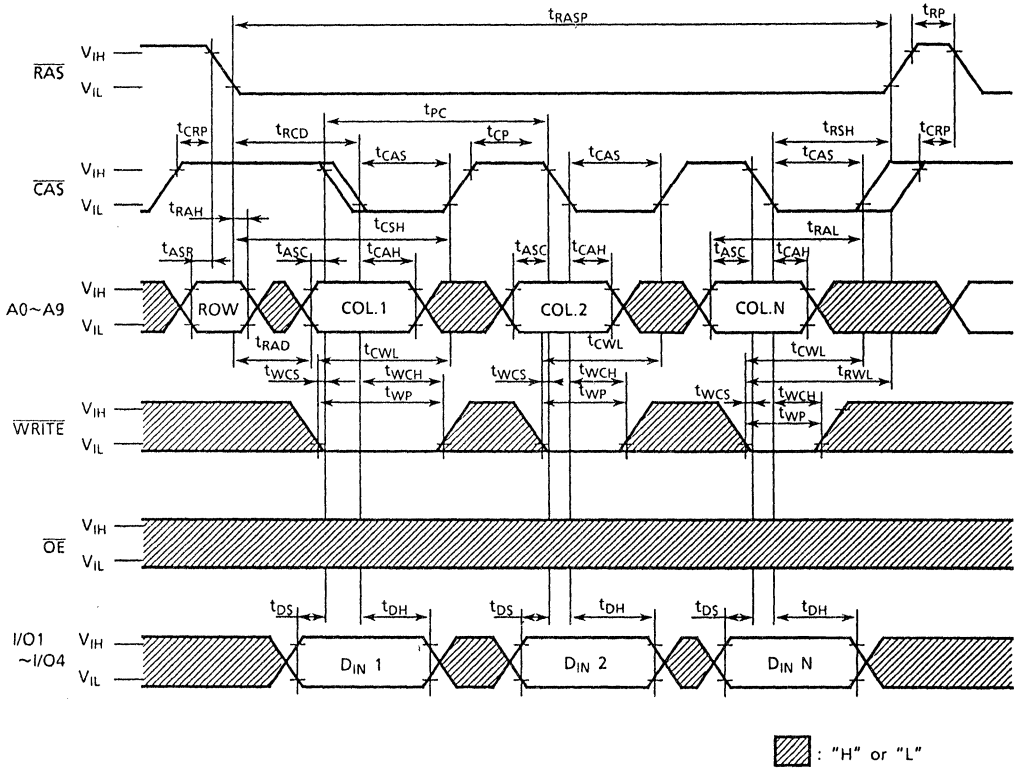
READ-MODIFY-WRITE CYCLE



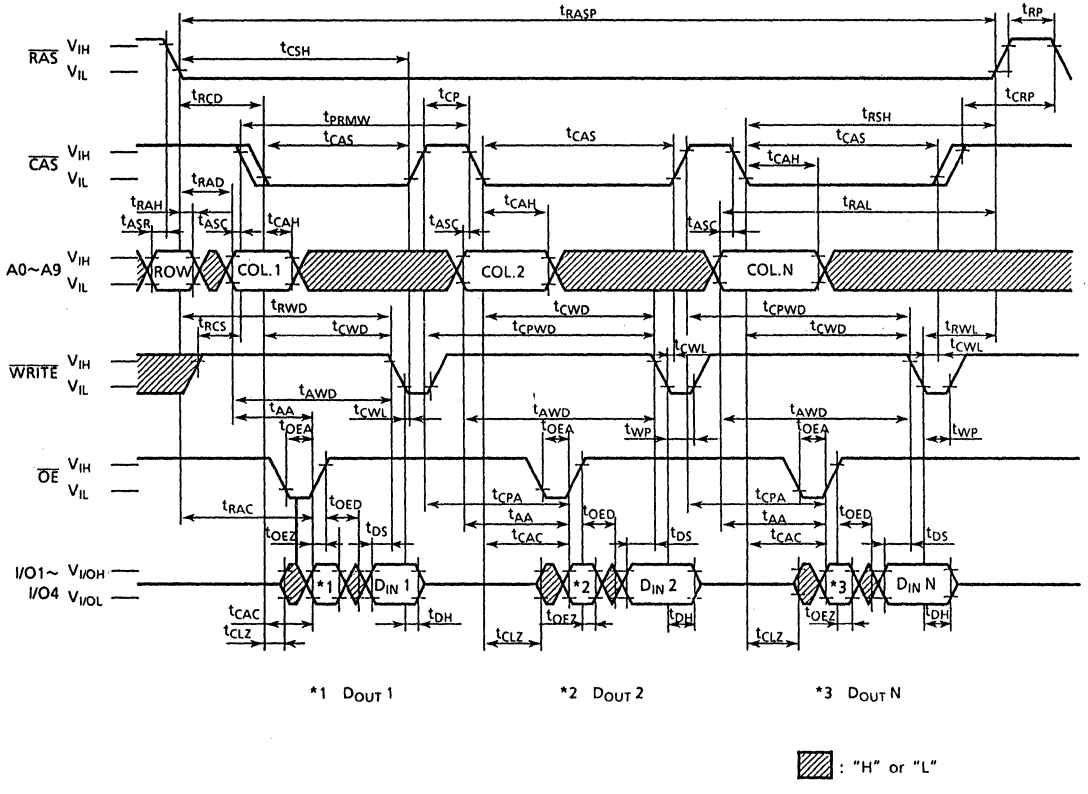
FAST PAGE MODE READ CYCLE



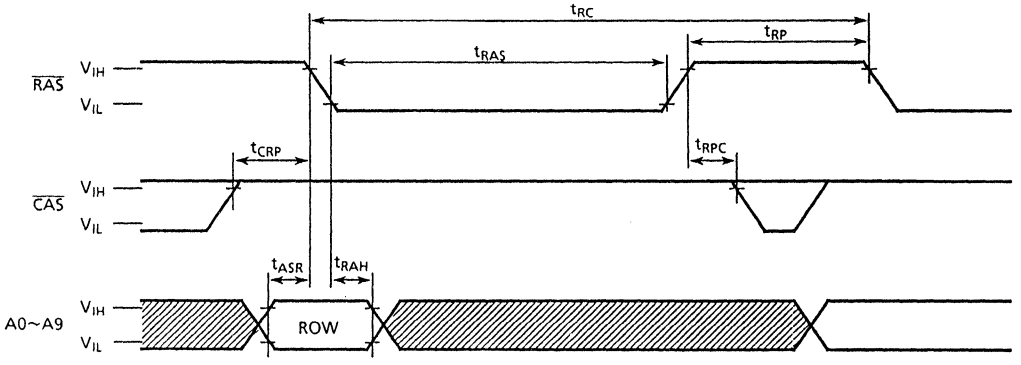
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



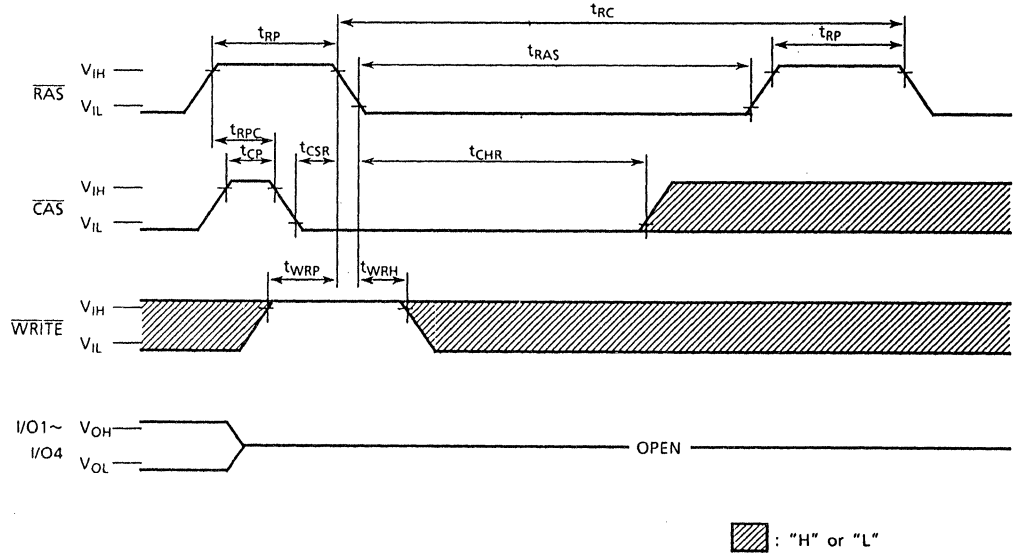
$\overline{RAS}$ ONLY REFRESH CYCLE



Noto : $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

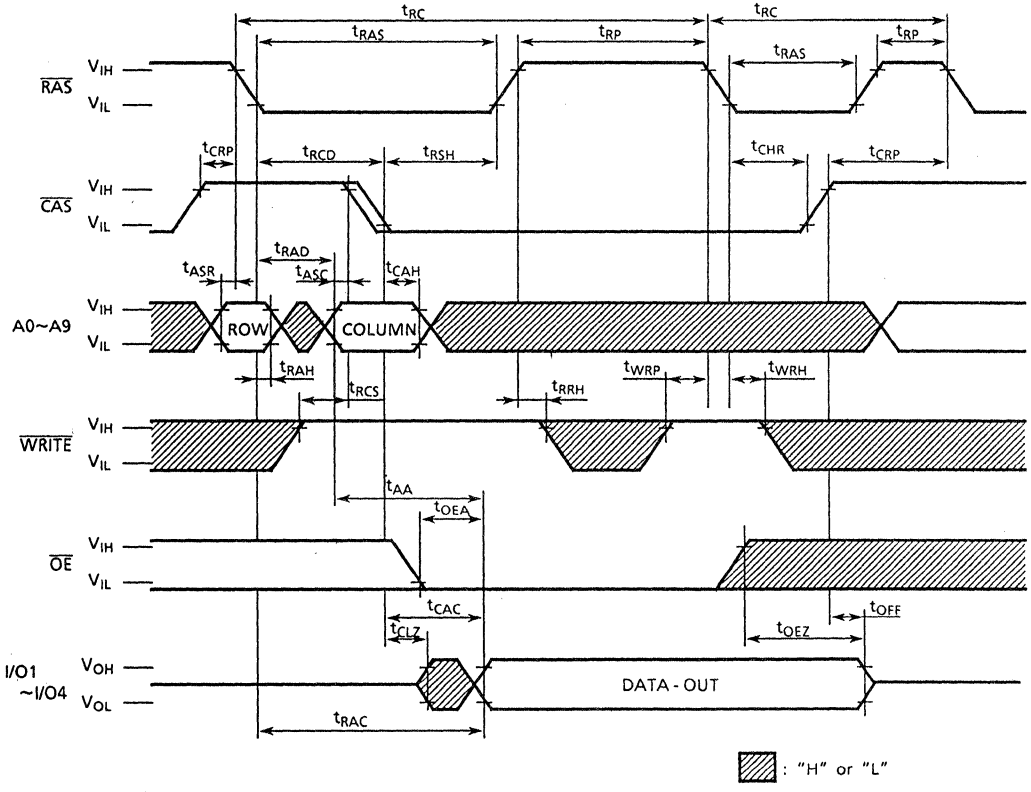
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



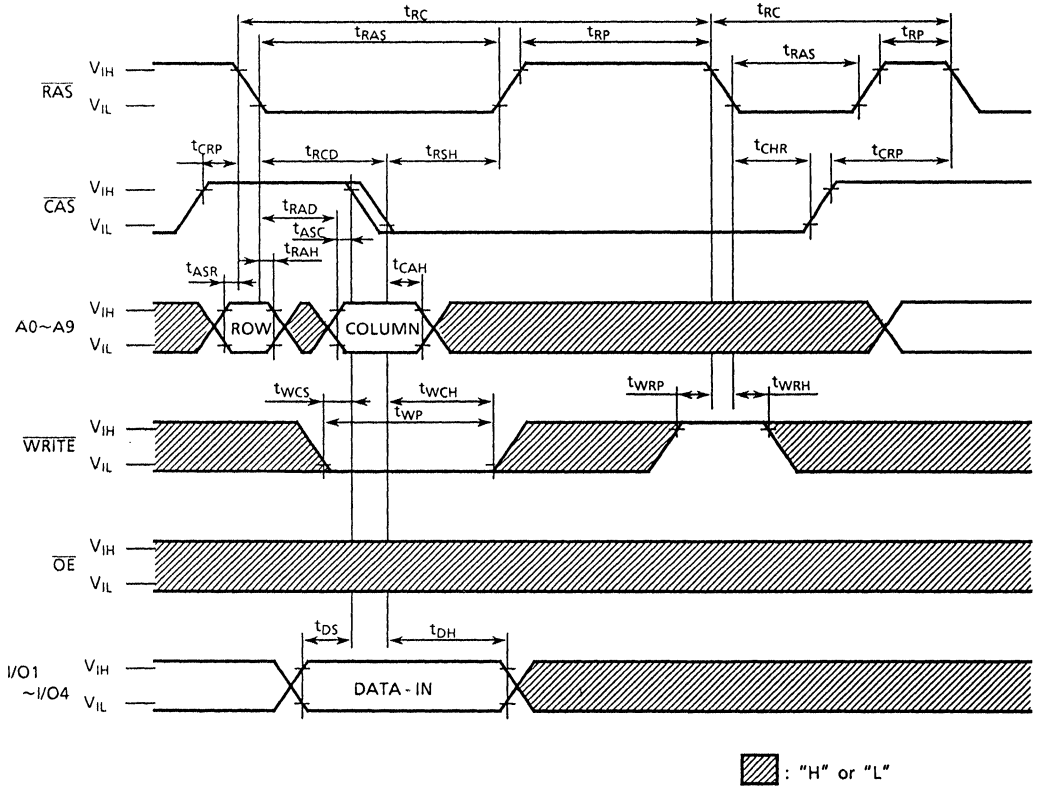
▨ : "H" or "L"

Note : $\overline{OE}$, A0~A9 = "H" or "L"

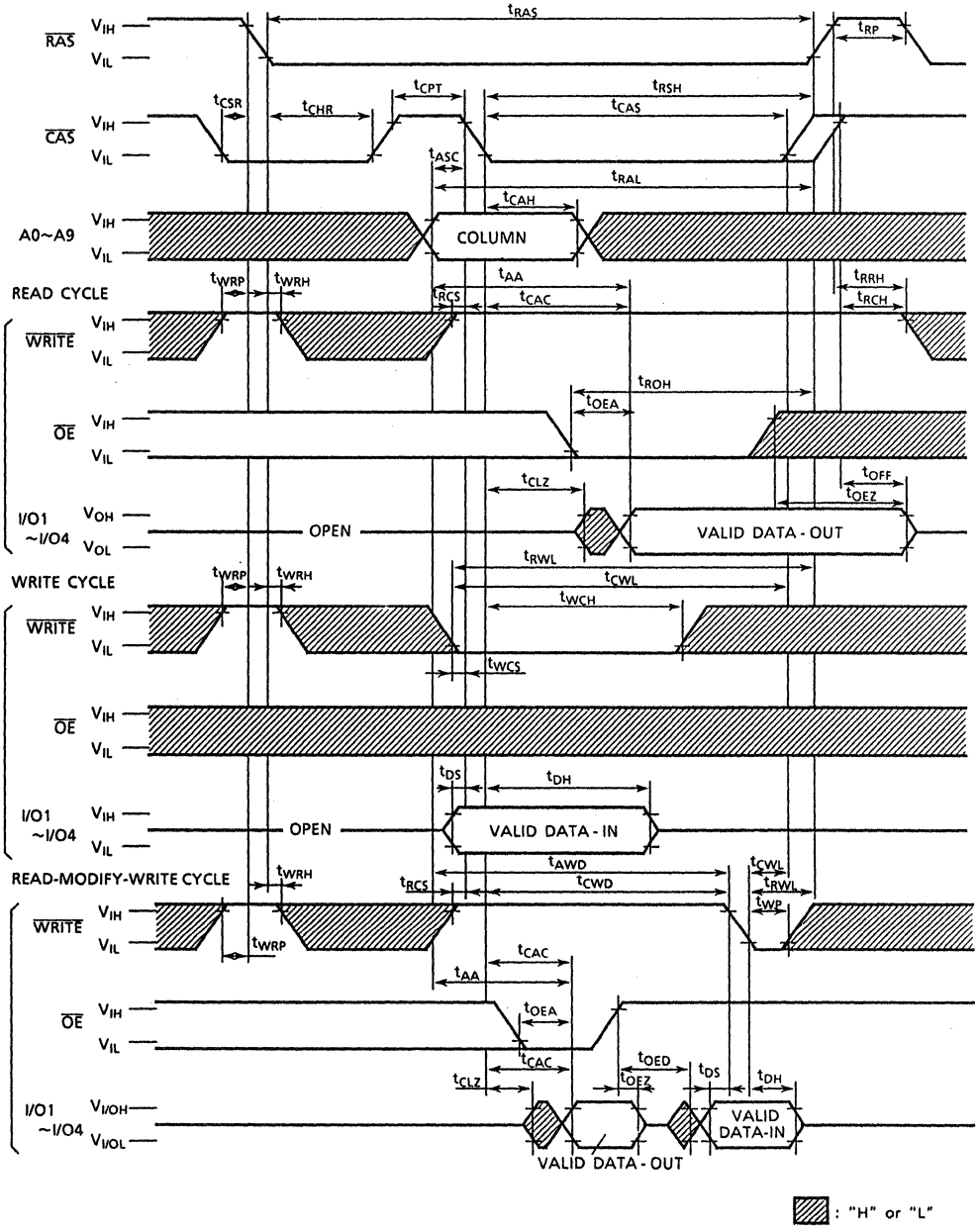
HIDDEN REFRESH CYCLE (READ)



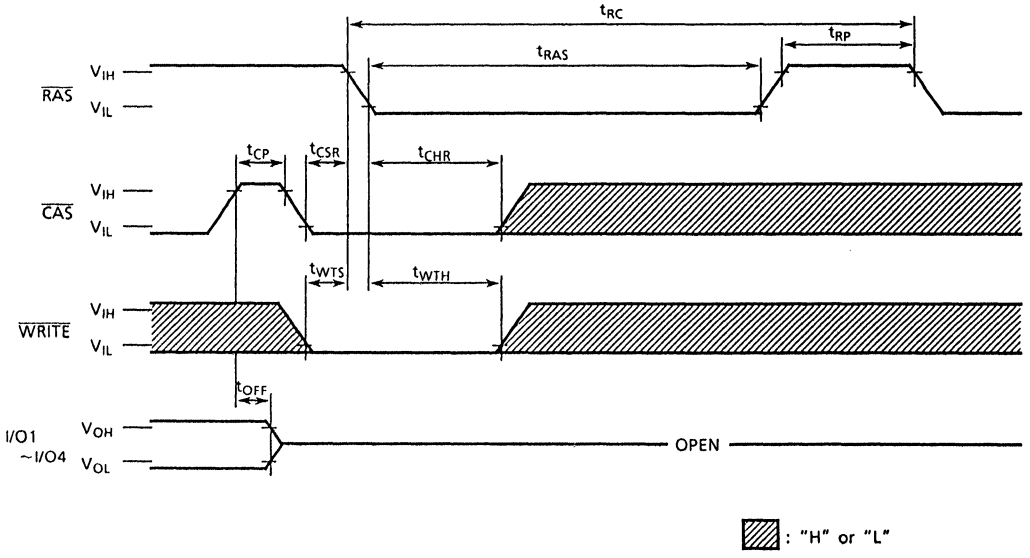
HIDDEN REEFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, CAS BEFORE RAS REFRESH CYCLE



Note : $\overline{OE}$, A0~A9 : "H" or "L"

TEST MODE

The TC514400APL/AJL/ASJL/AZL is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Aoc is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".

If they were not equal, the I/O pin would indicate a "0". Fig.1 shows the block diagram of TC514400APL/AJL/ASJL/AZL. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

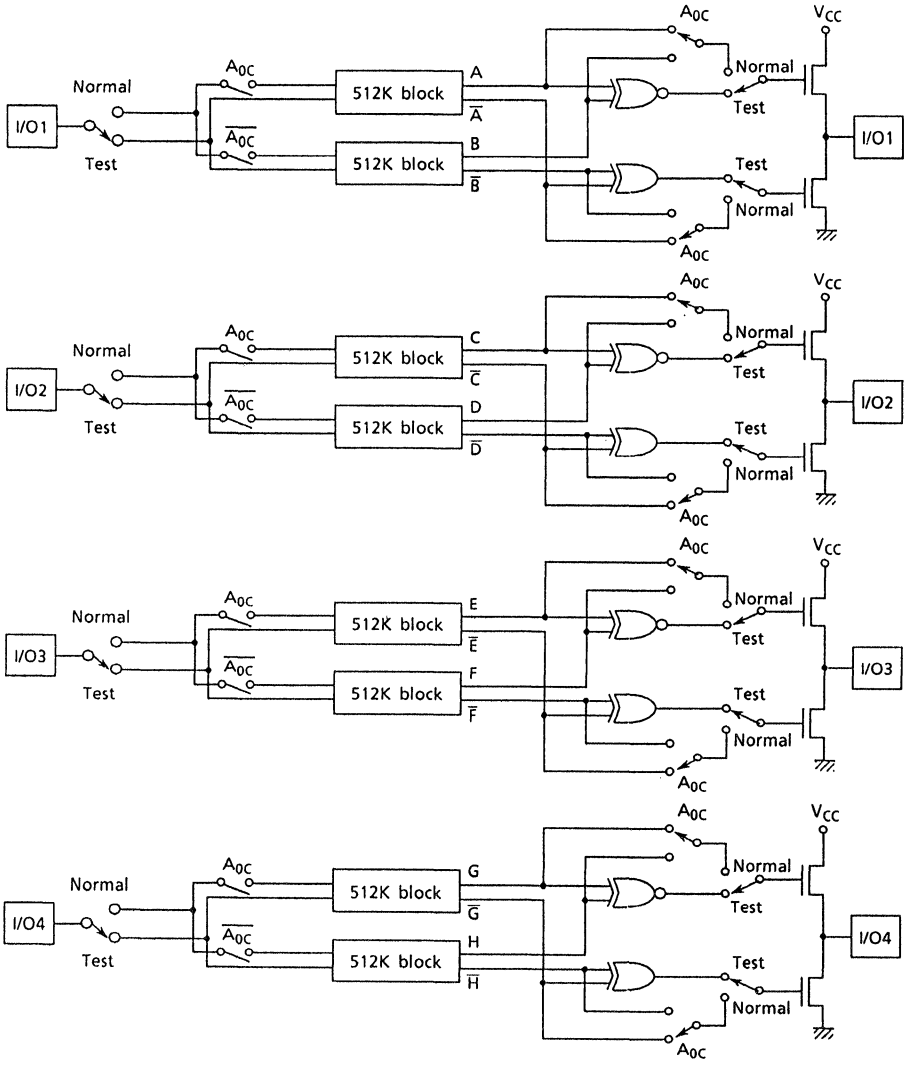


Fig. 1

NOTES

1,048,576 WORD ×4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514400AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514400AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514400AP/AJ/ASJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

		TC514400AP/AJ/ASJ/AZ -70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns	60ns

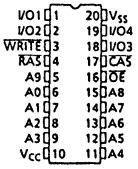
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 550mW MAX. Operating (TC514400AP/AJ/ASJ/AZ-70)
  - 468mW MAX. Operating (TC514400AP/AJ/ASJ/AZ-80)
  - 413mW MAX. Operating (TC514400AP/AJ/ASJ/AZ-10)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package
  - TC514400AP : DIP20-P-300C
  - TC514400AJ : SOJ26-P-350
  - TC514400ASJ : SOJ26-P-300A
  - TC514400AZ : ZIP20-P-400A

PIN NAMES

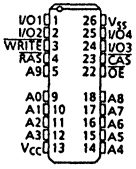
A0~A9	Address Inputs	$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe	I/O1~I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
$\overline{WRITE}$	Read/Write Input	V_{SS}	Ground

PIN CONNECTION (TOP VIEW)

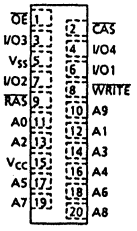
Plastic DIP



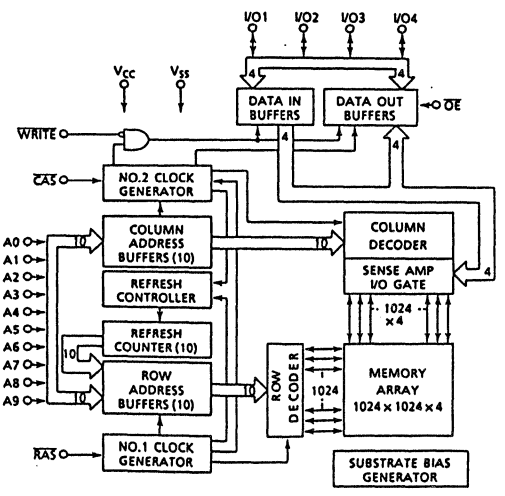
Plastic SOJ



Plastic ZIP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature·Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514400AP/AJ/ASJ/AZ-70	–	100	mA	3, 4
		TC514400AP/AJ/ASJ/AZ-80	–	85		5
		TC514400AP/AJ/ASJ/AZ-10	–	75		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514400AP/AJ/ASJ/AZ-70	–	100	mA	3, 5
		TC514400AP/AJ/ASJ/AZ-80	–	85		
		TC514400AP/AJ/ASJ/AZ-10	–	75		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514400AP/AJ/ASJ/AZ-70	–	70	mA	3, 4
		TC514400AP/AJ/ASJ/AZ-80	–	60		5
		TC514400AP/AJ/ASJ/AZ-10	–	55		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514400AP/AJ/ASJ/AZ-70	–	100	mA	3, 5
		TC514400AP/AJ/ASJ/AZ-80	–	85		
		TC514400AP/AJ/ASJ/AZ-10	–	75		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514400AP/AJ/ASJ/AZ-70		TC514400AP/AJ/ASJ/AZ-80		TC514400AP/AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	–	205	–	245	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	105	–	125	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	200,000	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514400AP/ AJ/ASJ/AZ-70		TC514400AP/ AJ/ASJ/AZ-80		TC514400AP/ AJ/ASJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	12
t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	–	70	–	85	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	–	75	–	90	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	25	–	ns	
t_{WTS}	Write Commamd Set-Up Time (Test Mode In)	10	–	10	–	10	–	ns	
t_{WTH}	Write Commamd Hold Time (Test Mode In)	10	–	10	–	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC514400AP/AJ/ASJ/AZ-70		TC514400AP/AJ/ASJ/AZ-80		TC514400AP/AJ/ASJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	155	–	185	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	190	–	210	–	250	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Cycle Read-Modify-Write Time	105	–	110	–	130	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	75	–	85	–	105	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	9,14
t_{AA}	Access Time from Column Address	–	40	–	45	–	55	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	50	–	60	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	75	200,000	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	75	–	85	–	105	–	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	–	50	–	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	45	–	55	–	ns	
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	55		55	–	65	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	105	–	115	–	140	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	70	–	75	–	90	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	75	–	80	–	95	–	ns	13
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	30	–	ns	

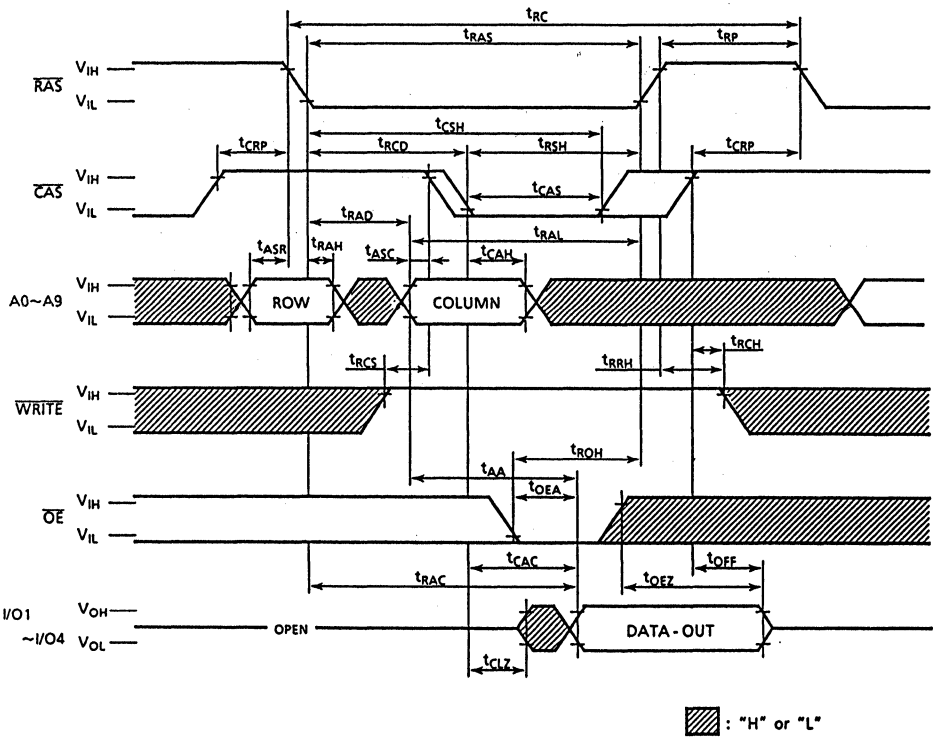
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/01~I/04)	–	7	pF

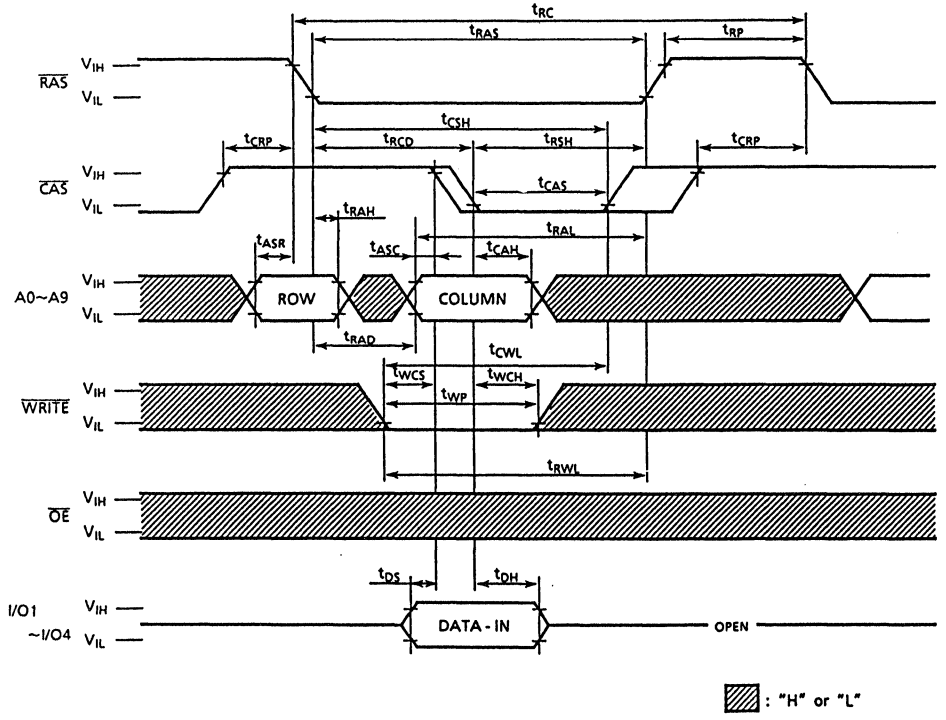
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T=5$ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

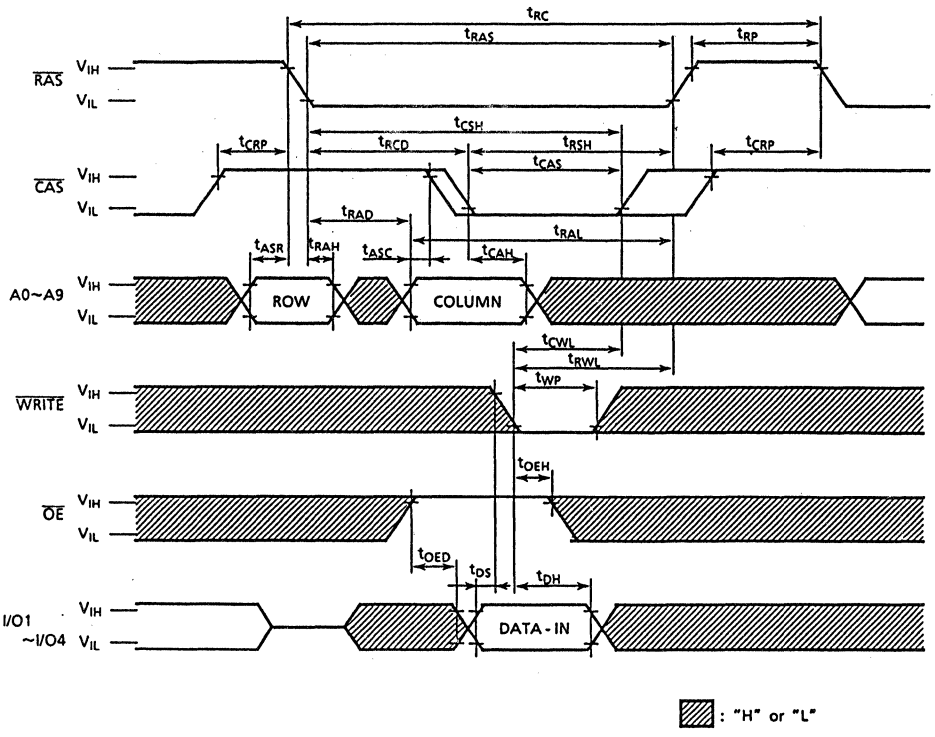
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tROH
tAA
tOEA
OE
tCAC
tOFF
tRAC
tOEZ
I/O1
~I/O4
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

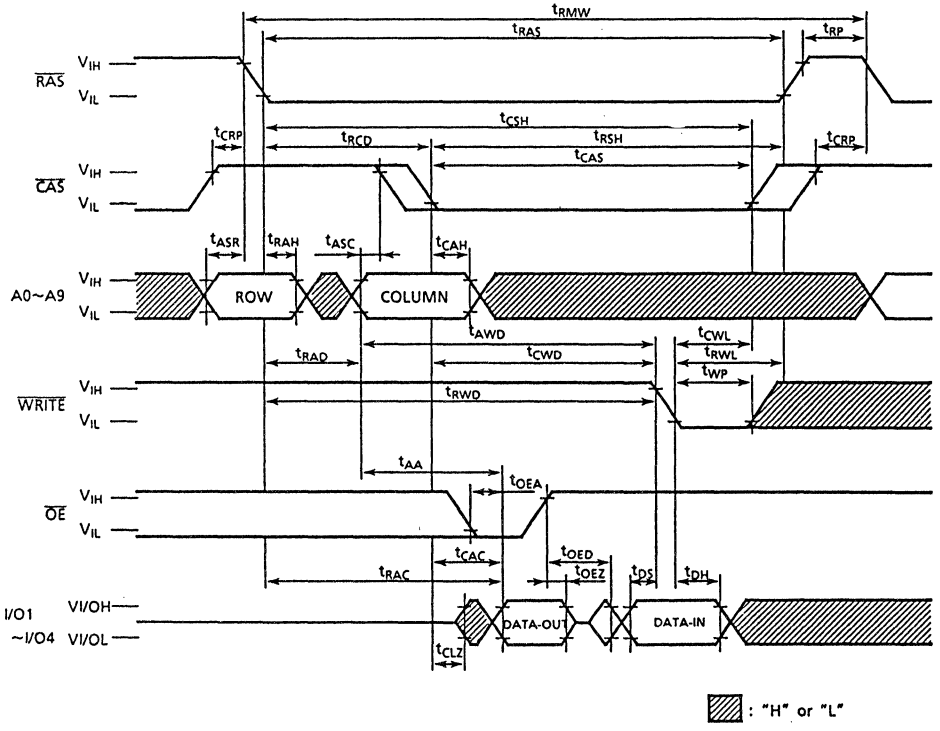
WRITE CYCLE (EARLY WRITE)



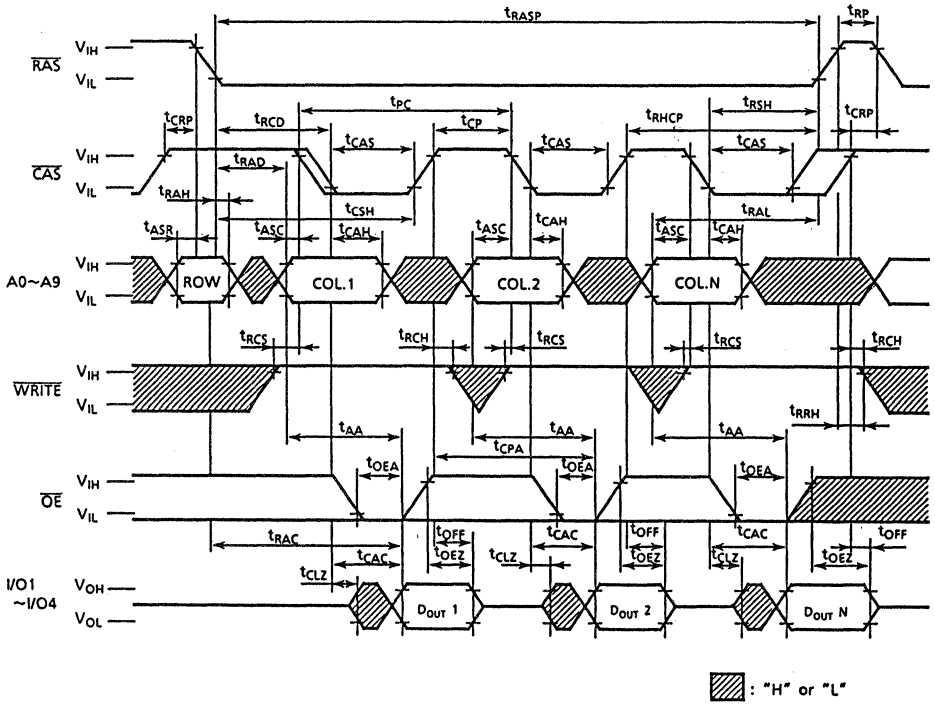
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



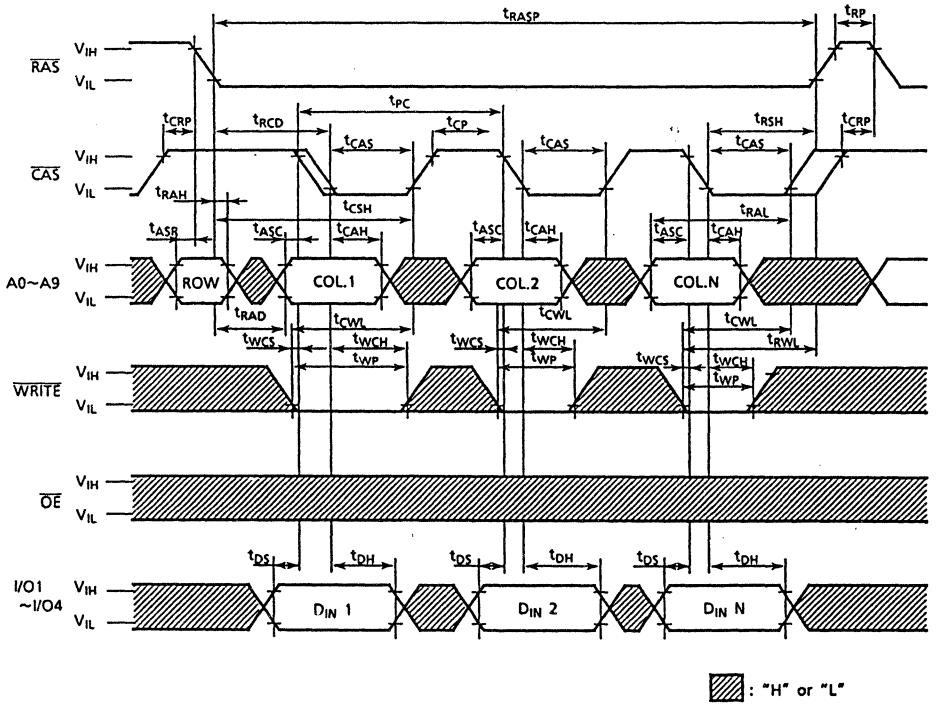
READ-MODIFY-WRITE CYCLE



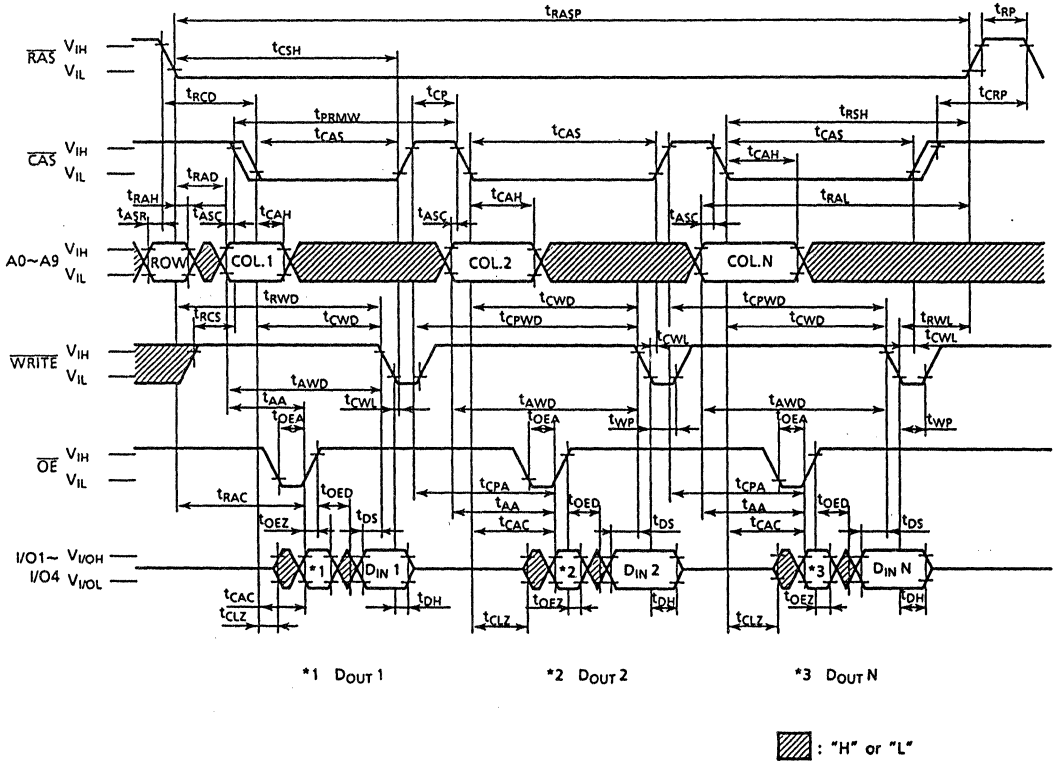
FAST PAGE MODE READ CYCLE



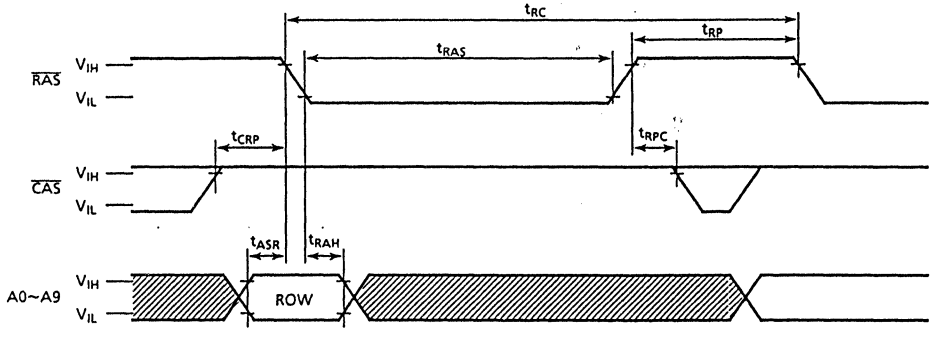
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



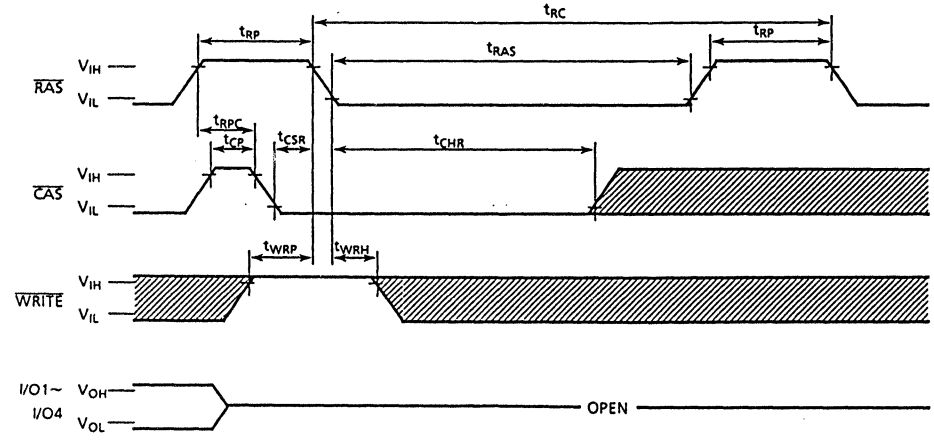
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

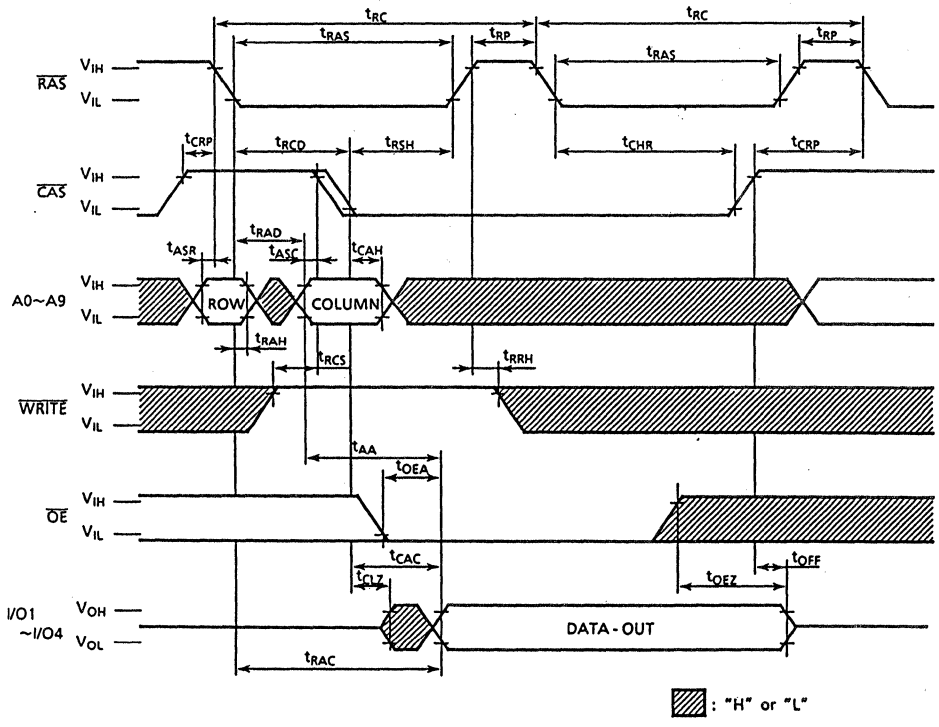
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



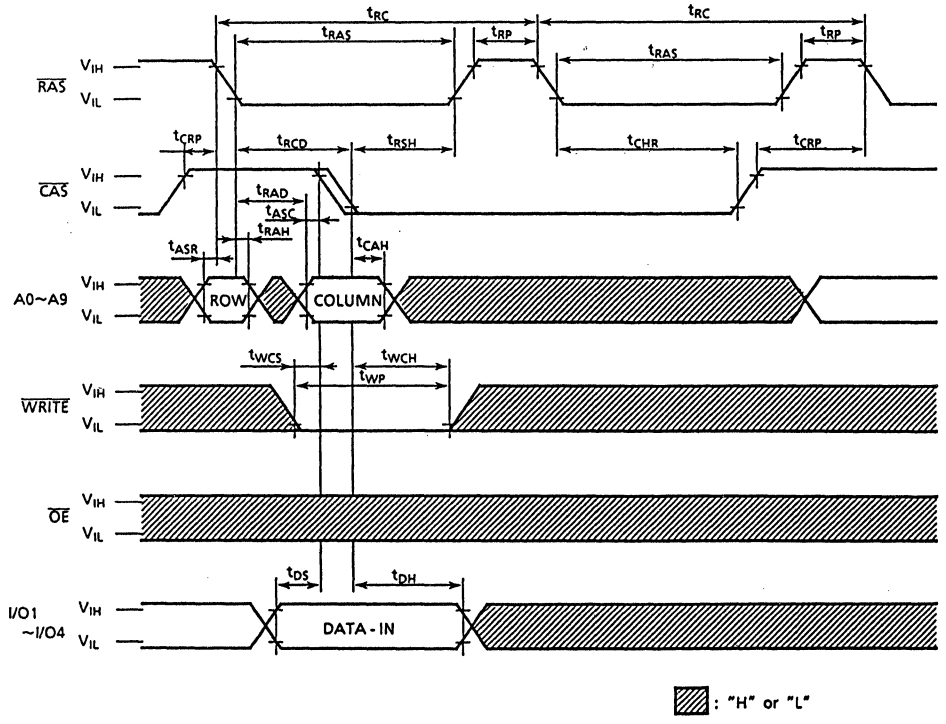
Note: $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

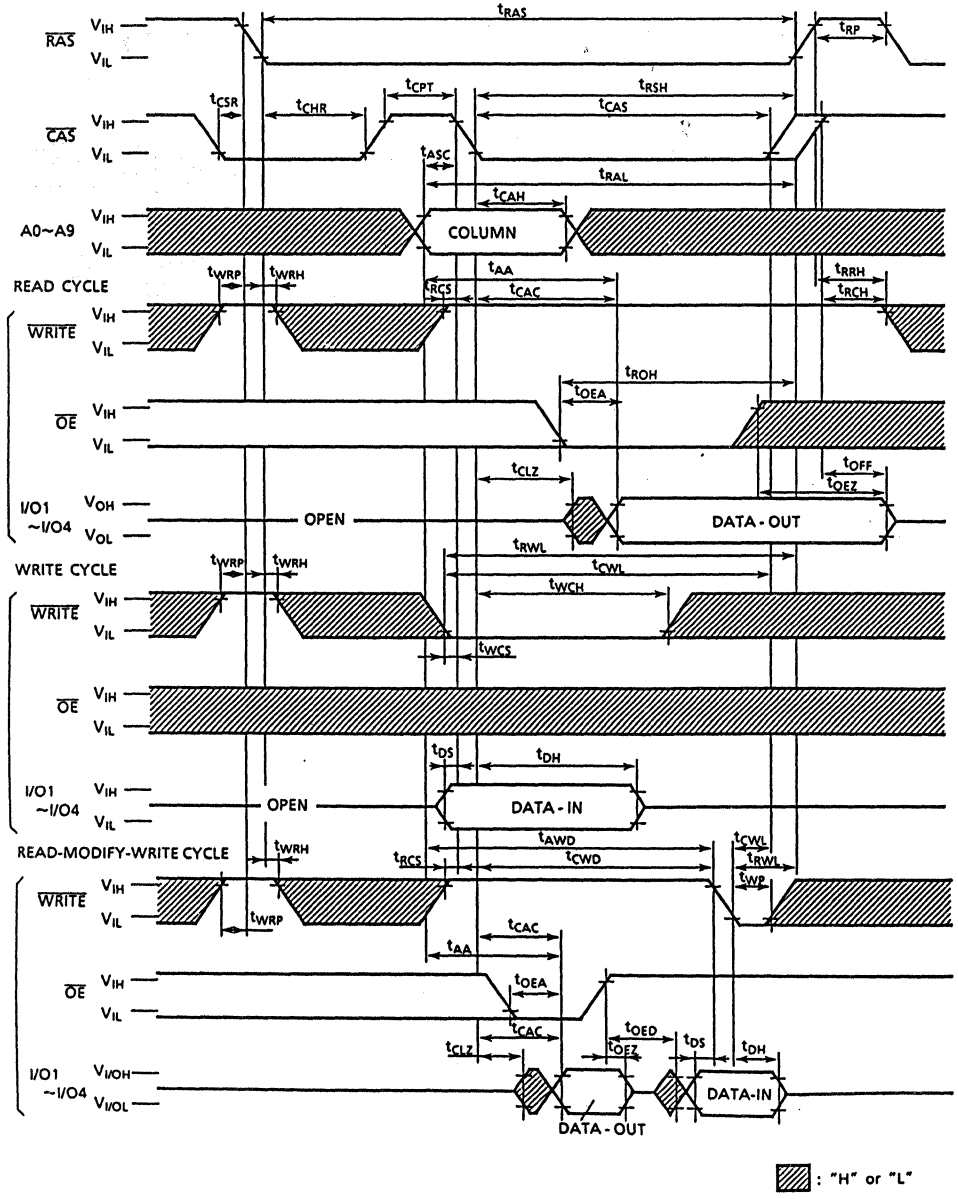
HIDDEN REFRESH CYCLE (READ)



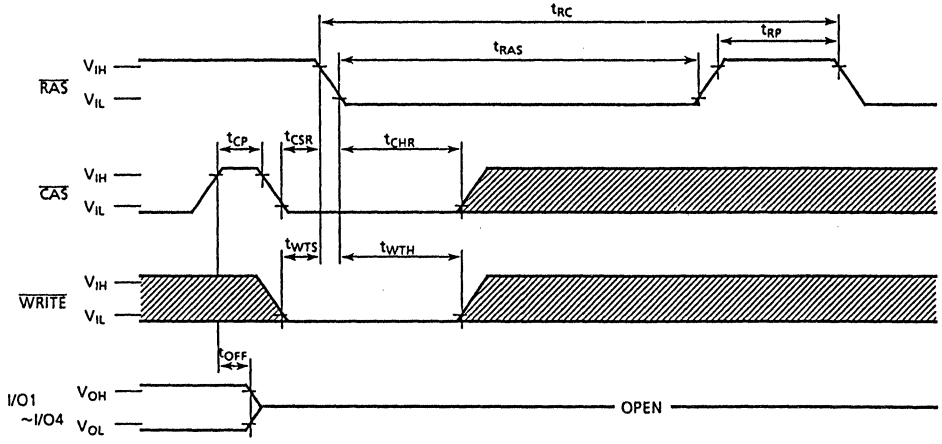
HIDDEN REEFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



WRITE, CAS BEFORE RAS REFRESH CYCLE



Note: $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC514400AP/AJ/ASJ/AZ is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A0c is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".

If they were not equal, the I/O pin would indicate a "0". Fig.1 shows the block diagram of TC514400AP/AJ/ASJ/AZ. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

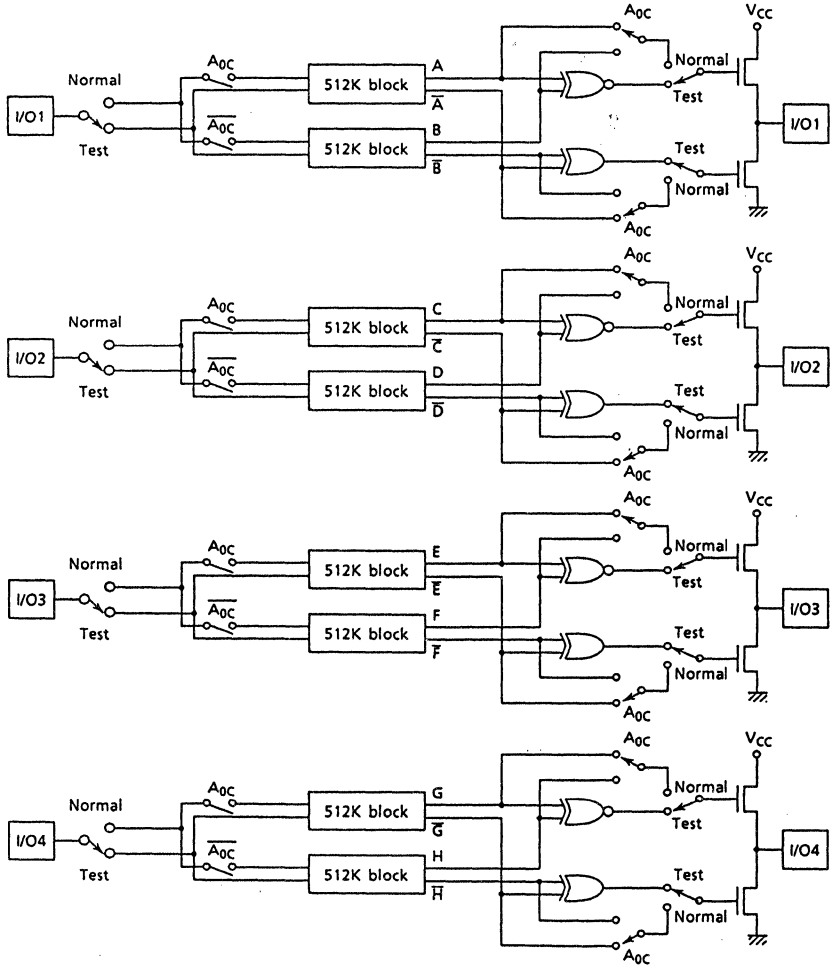


Fig. 1

NOTES

1,048,576 WORD ×4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514400APL/AJL/ASJL/AZL is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514400APL/AJL/ASJL/AZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514400APL/AJL/ASJL/AZL to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

		TC514400APL/AJL/ASJL/AZL -70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns	60ns

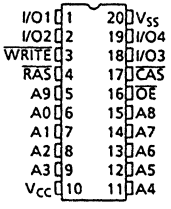
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  550mW MAX. Operating (TC514400APL/AJL/ASJL/AZL-70)
  468mW MAX. Operating (TC514400APL/AJL/ASJL/AZL-80)
  413mW MAX. Operating (TC514400APL/AJL/ASJL/AZL-10)
  1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514400APL : DIP20-P-300C
  TC514400AJL : SOJ26-P-350
  TC514400ASJL: SOJ26-P-300A
  TC514400AZL : ZIP20-P-400A

PIN NAMES

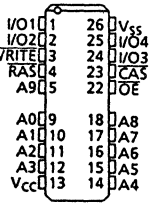
A0~A9	Address Inputs	$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe	I/O1~I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
$\overline{WRITE}$	Read/Write Input	V_{SS}	Ground

PIN CONNECTION (TOP VIEW)

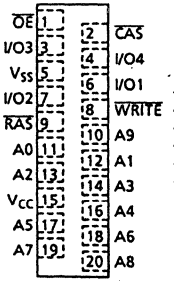
Plastic DIP



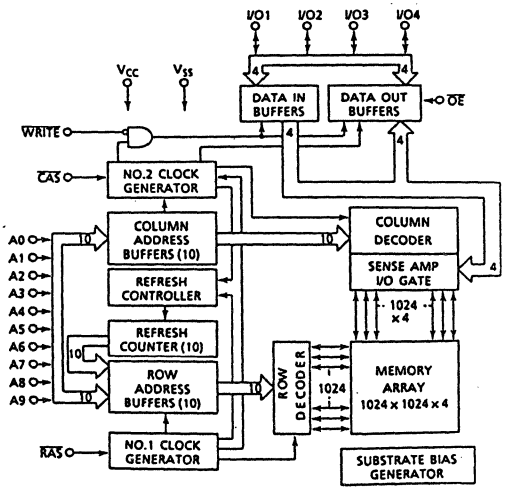
Plastic SOJ



Plastic ZIP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature·Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514400APL/AJL/ASJL/AZL-70	–	100	mA	3, 4
		TC514400APL/AJL/ASJL/AZL-80	–	85		5
		TC514400APL/AJL/ASJL/AZL-10	–	75		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514400APL/AJL/ASJL/AZL-70	–	100	mA	3, 5
		TC514400APL/AJL/ASJL/AZL-80	–	85		
		TC514400APL/AJL/ASJL/AZL-10	–	75		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514400APL/AJL/ASJL/AZL-70	–	70	mA	3, 4
		TC514400APL/AJL/ASJL/AZL-80	–	60		5
		TC514400APL/AJL/ASJL/AZL-10	–	55		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514400APL/AJL/ASJL/AZL-70	–	100	mA	3, 5
		TC514400APL/AJL/ASJL/AZL-80	–	85		
		TC514400APL/AJL/ASJL/AZL-10	–	75		
I_{CC7}	Battery Back Up Current Average Power Supply Current, Battery Back Up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} – 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V, A0~9 = V_{CC} – 0.2V or 0.2V, I/O1~4 = V_{CC} – 0.2V, 0.2V or OPEN : t_{RC} = 125µs, t_{RAS} = 300ns ~1µs)		–	400	µA	3, 6
I_{CC7}	Battery Back Up Current Average Power Supply Current, Battery Back Up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} – 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V, A0~9 = V_{CC} – 0.2V or 0.2V, I/O1~4 = V_{CC} – 0.2V, 0.2V or OPEN : t_{RC} = 125µs, t_{RAS} = t_{RAS} MIN. ~300ns)		–	300	µA	3, 6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514400APL/AJL/ASJL/AZL-70		TC514400APL/AJL/ASJL/AZL-80		TC514400APL/AJL/ASJL/AZL-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	–	205	–	245	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	105	–	125	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	10,15 16
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	10,15
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	–	55	ns	10
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	200,000	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514400APL/ AJL/ASJL/AZL-70		TC514400APL/ AJL/ASJL/AZL-80		TC514400APL/ AJL/ASJL/AZL-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	12
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	13
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	13
t_{REF}	Refresh Period	–	128	–	128	–	128	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	50	–	60	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	–	110	–	135	–	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	–	70	–	85	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	–	75	–	90	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	25	–	ns	
t_{WTS}	Write Commamd Set-Up Time (Test Mode In)	10	–	10	–	10	–	ns	
t_{WTH}	Write Commamd Hold Time (Test Mode In)	10	–	10	–	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC514400APL/ AJL/ASJL/AZL-70		TC514400APL/ AJL/ASJL/AZL-80		TC514400APL/ AJL/ASJL/AZL-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	155	–	185	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	190	–	210	–	250	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	55	–	65	–	ns	
t_{RMR}	Fast Page Mode Read-Modify-Write Cycle Time	190	–	210	–	250	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	75	–	85	–	105	ns	10,15 16
t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	9,15
t_{AA}	Access Time from Column Address	–	40	–	45	–	55	ns	9,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	50	–	60	ns	10
t_{RAS}	$\overline{RAS}$ Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	75	100,000	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	75	–	85	–	105	–	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	–	55	–	65	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	45	–	55	–	ns	
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	55	–	55	–	65	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	105	–	115	–	140	–	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	70	–	75	–	90	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	75	–	80	–	95	–	ns	14
t_{OEA}	$\overline{OE}$ Access Time from	–	25	–	25	–	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	30	–	ns	

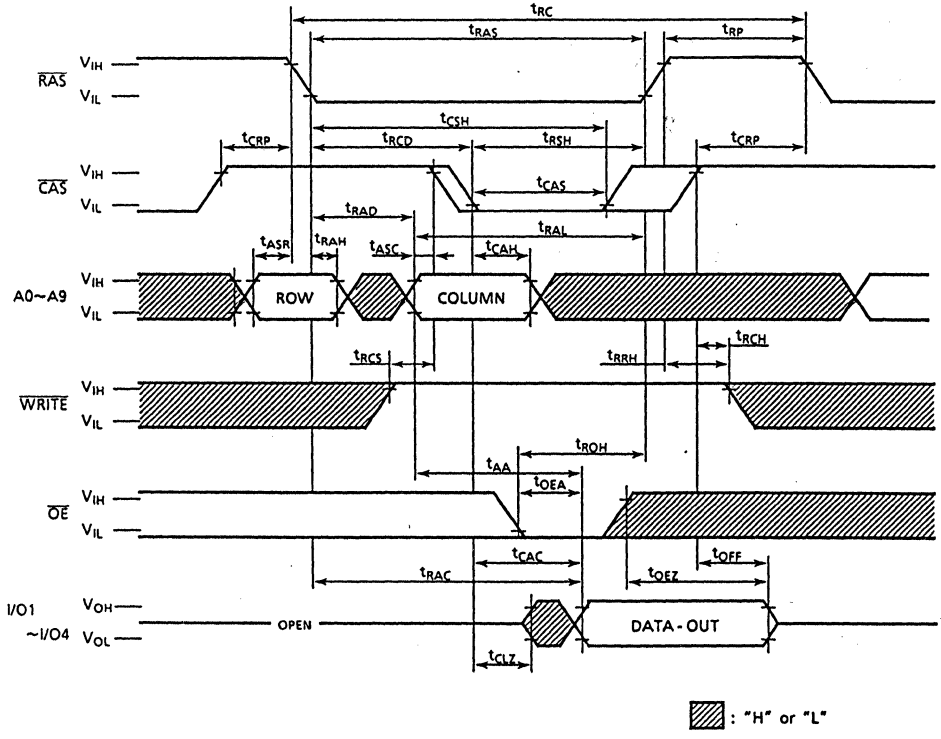
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	–	7	pF

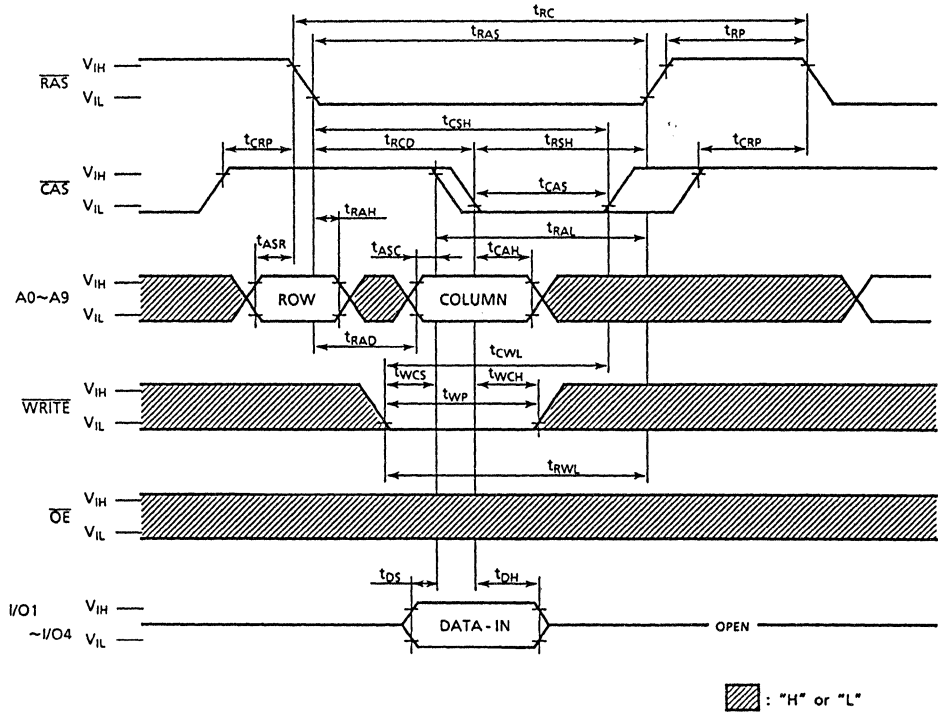
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. t_{RAS}(max.)=1μs is only applied to refresh of battery-back up. t_{RAS}(max.)=10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume t_T=5ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

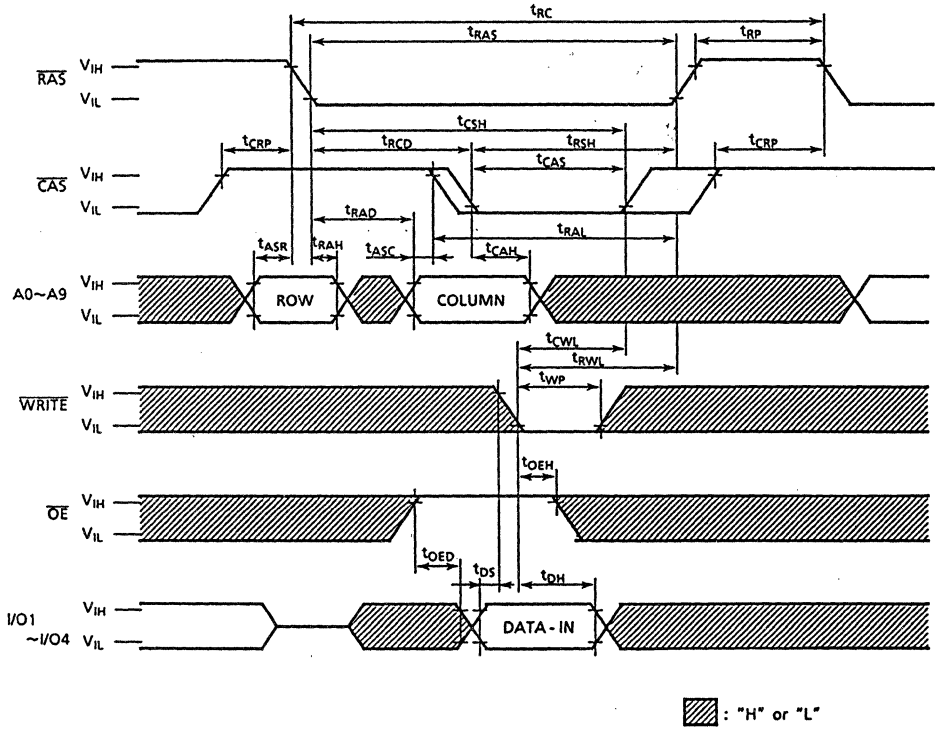
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tROH
tAA
tOEA
OE
tCAC
tOFF
tRAC
tOEZ
I/O1
~I/O4
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

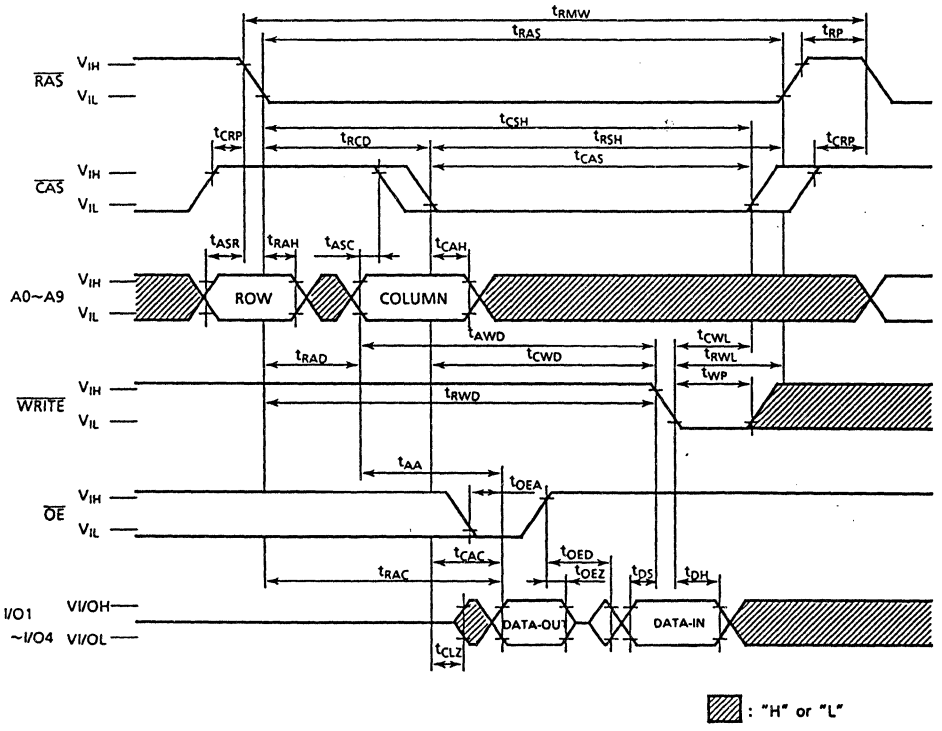
WRITE CYCLE (EARLY WRITE)



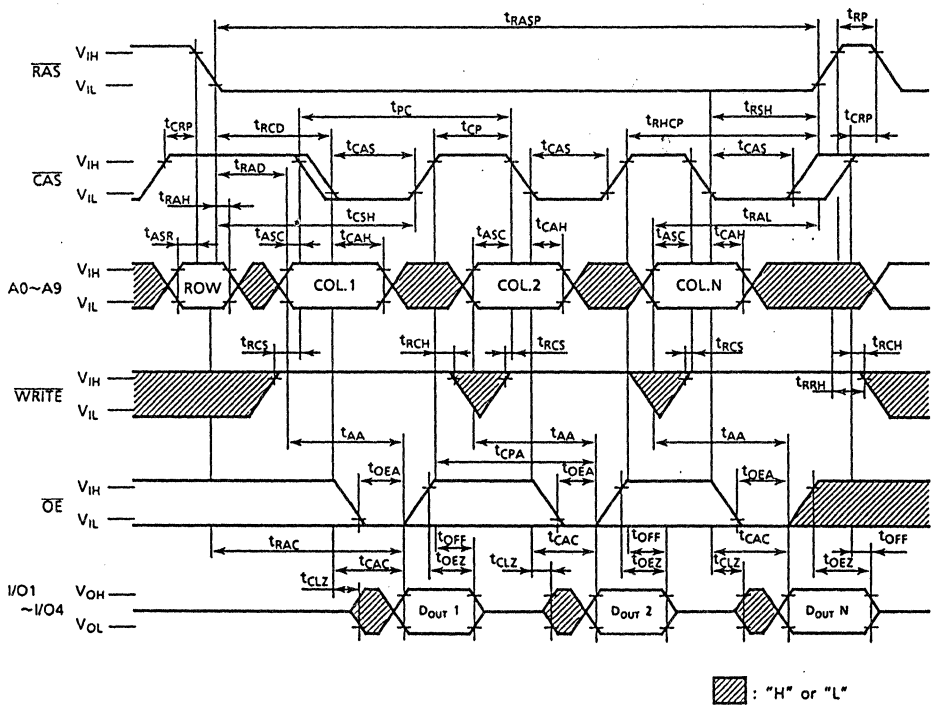
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



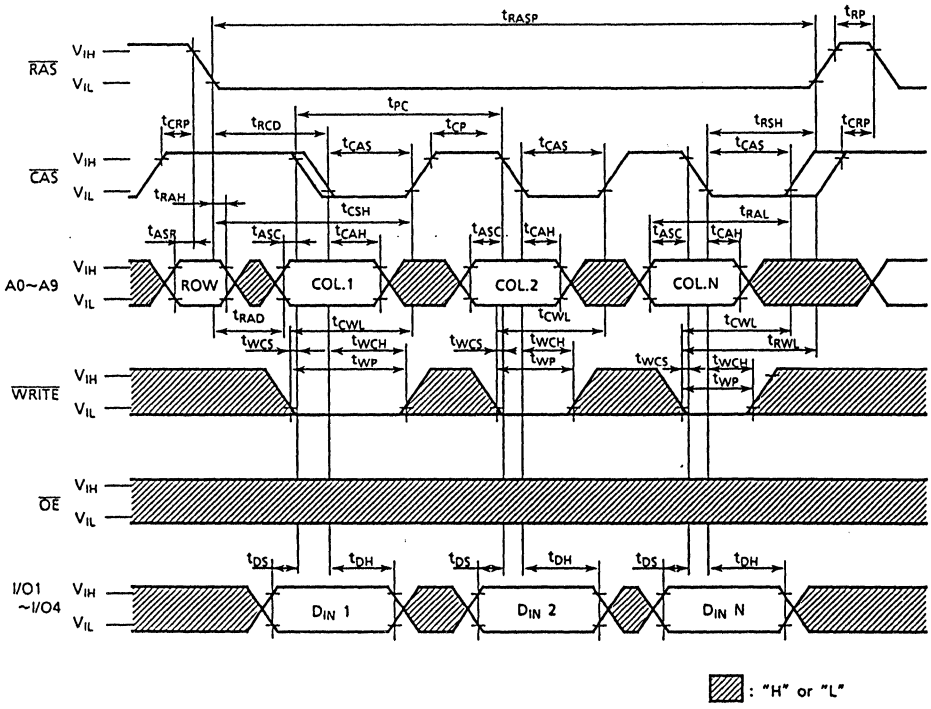
READ-MODIFY-WRITE CYCLE



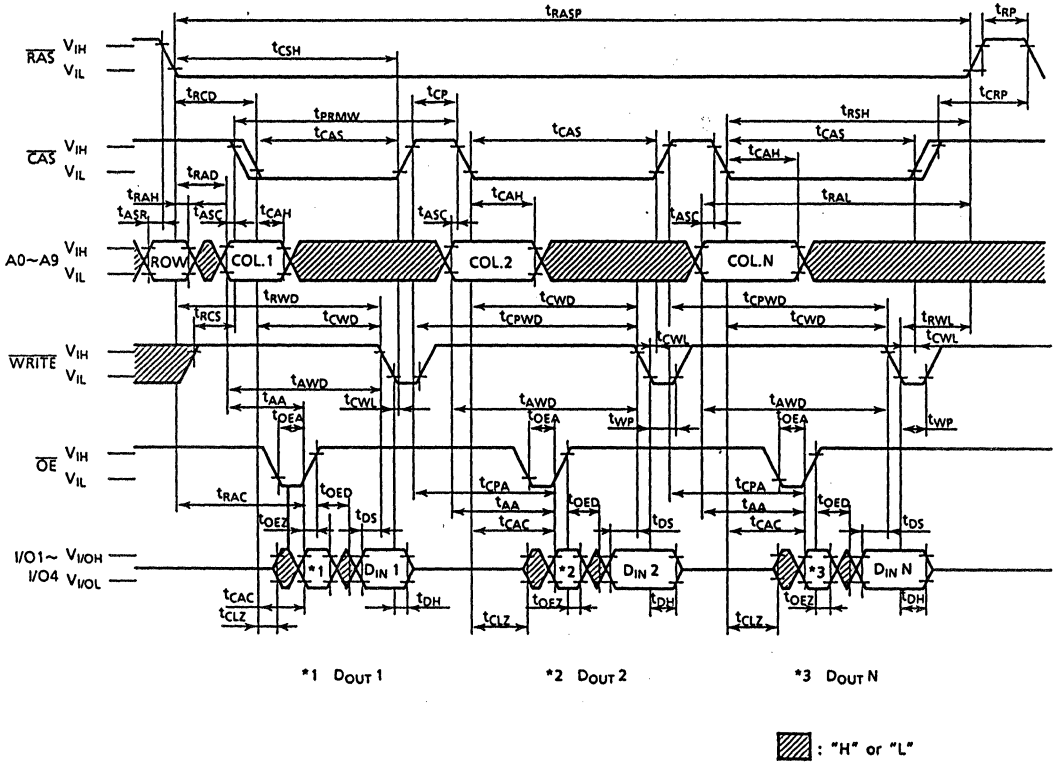
FAST PAGE MODE READ CYCLE



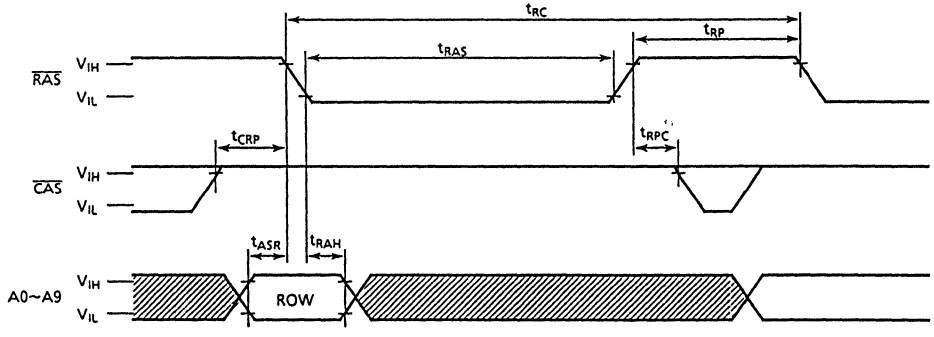
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



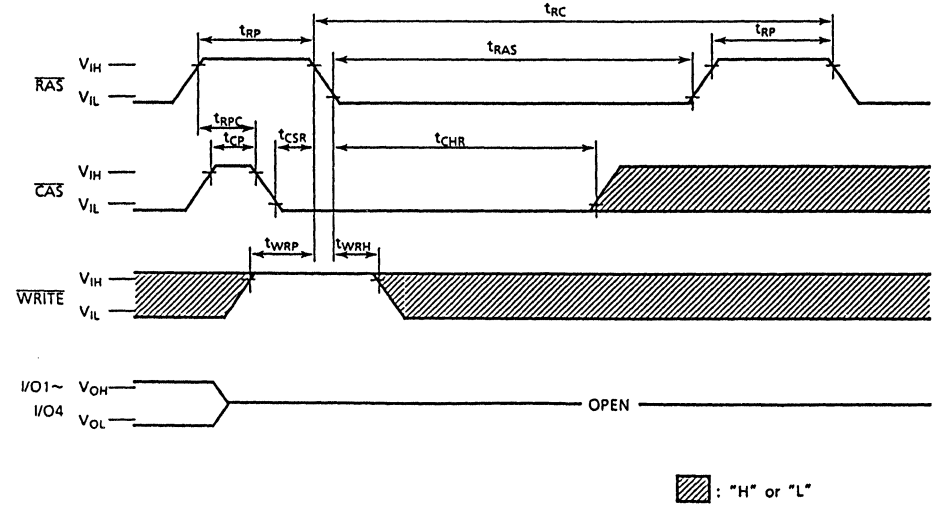
$\overline{RAS}$ ONLY REFRESH CYCLE



Noto: $\overline{WRITE}$, $\overline{OE}$="H" or "L"

▨: "H" or "L"

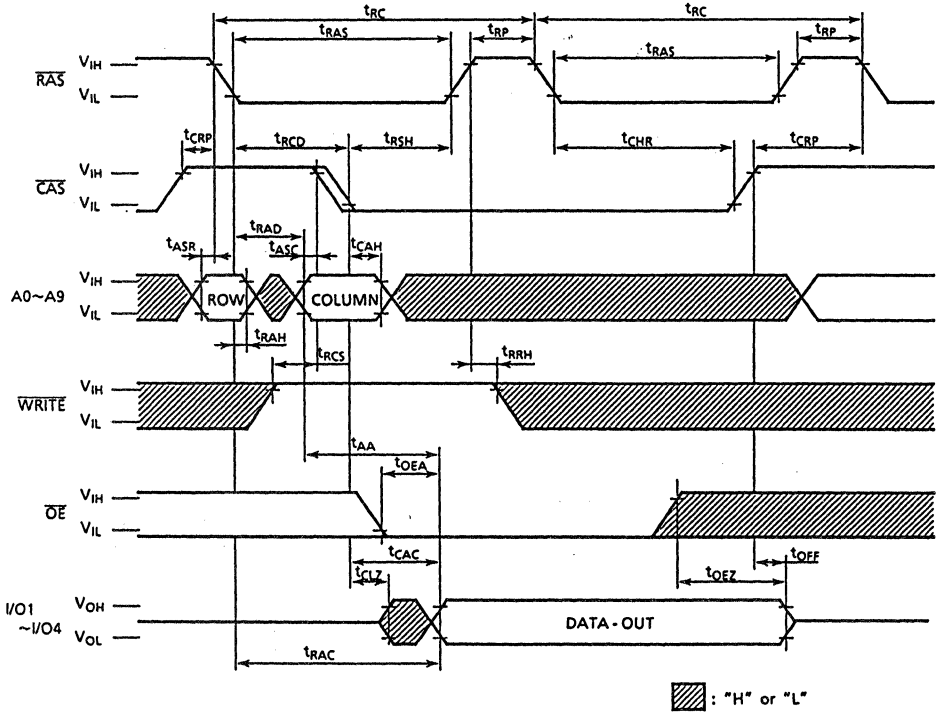
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



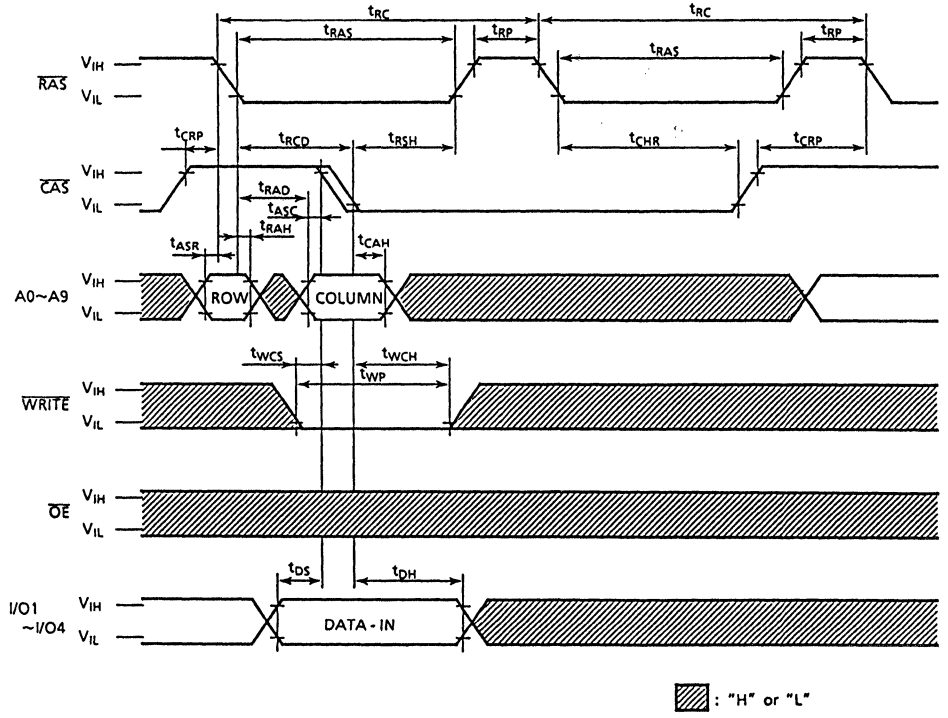
▨: "H" or "L"

Note: $\overline{OE}$, A0~A9="H" or "L"

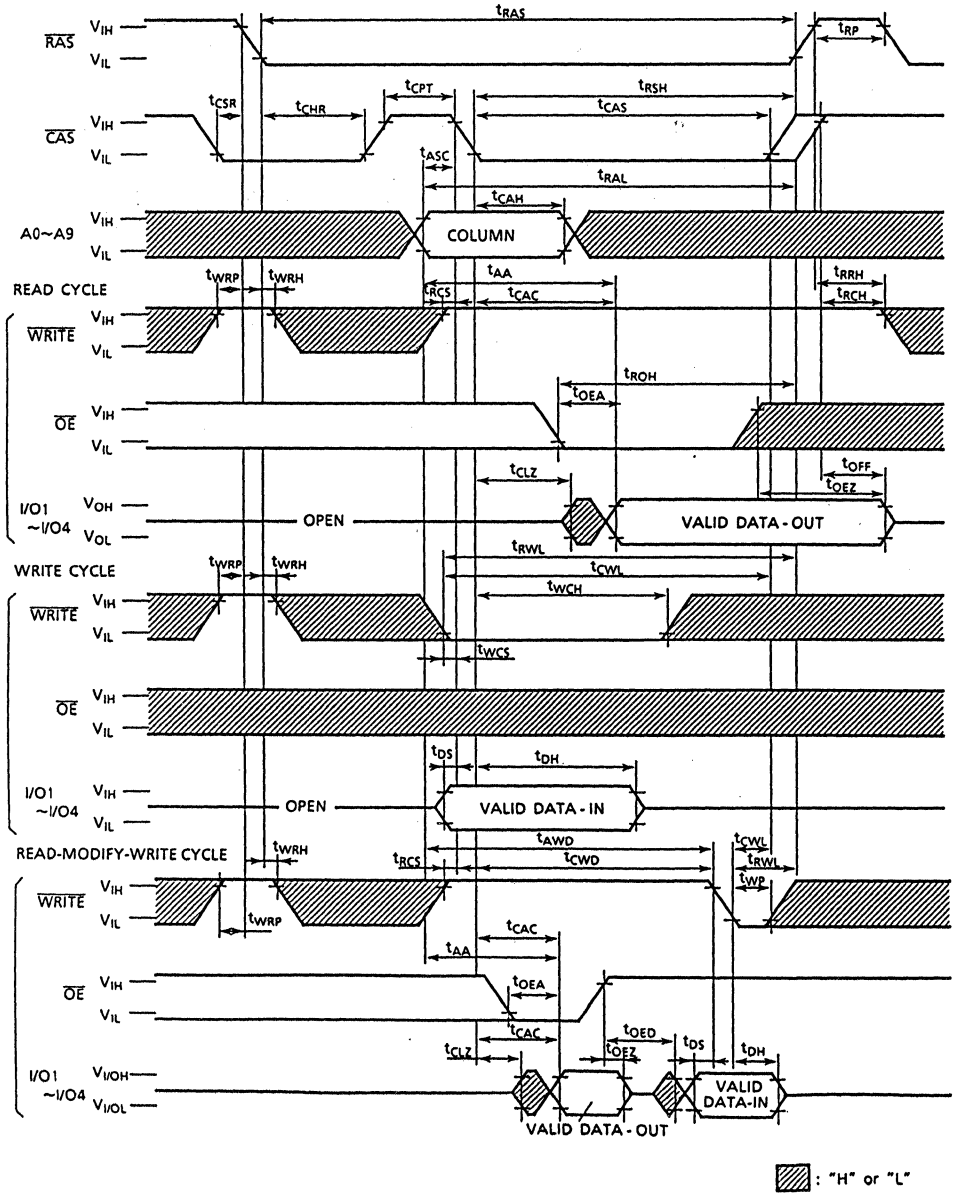
HIDDEN REFRESH CYCLE (READ)



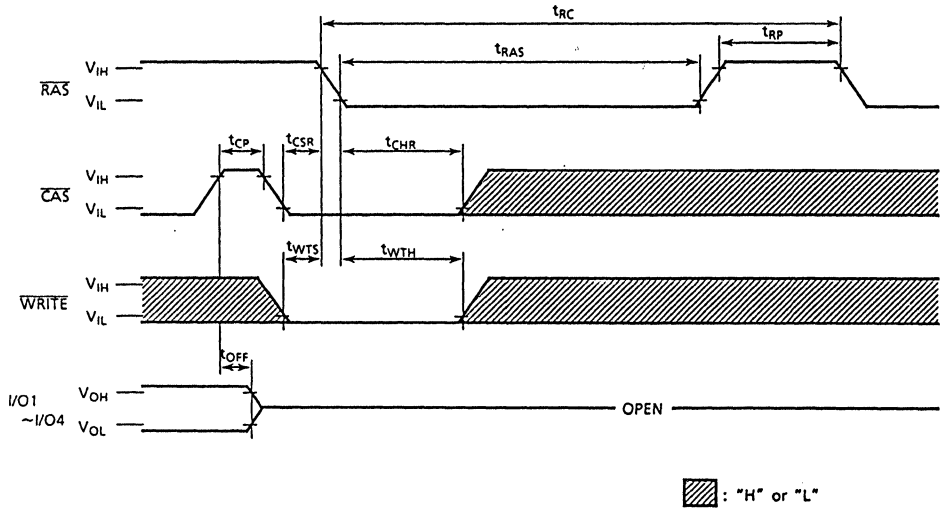
HIDDEN REEFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



WRITE, CAS BEFORE RAS REFRESH CYCLE



Note: $\overline{OE}$, A0~A9: "H" or "L"

TEST MODE

The TC514400APL/AJL/ASJL/AZL is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Aoc is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".

If they were not equal, the I/O pin would indicate a "0". Fig.1 shows the block diagram of TC514400APL/AJL/ASJL/AZL. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

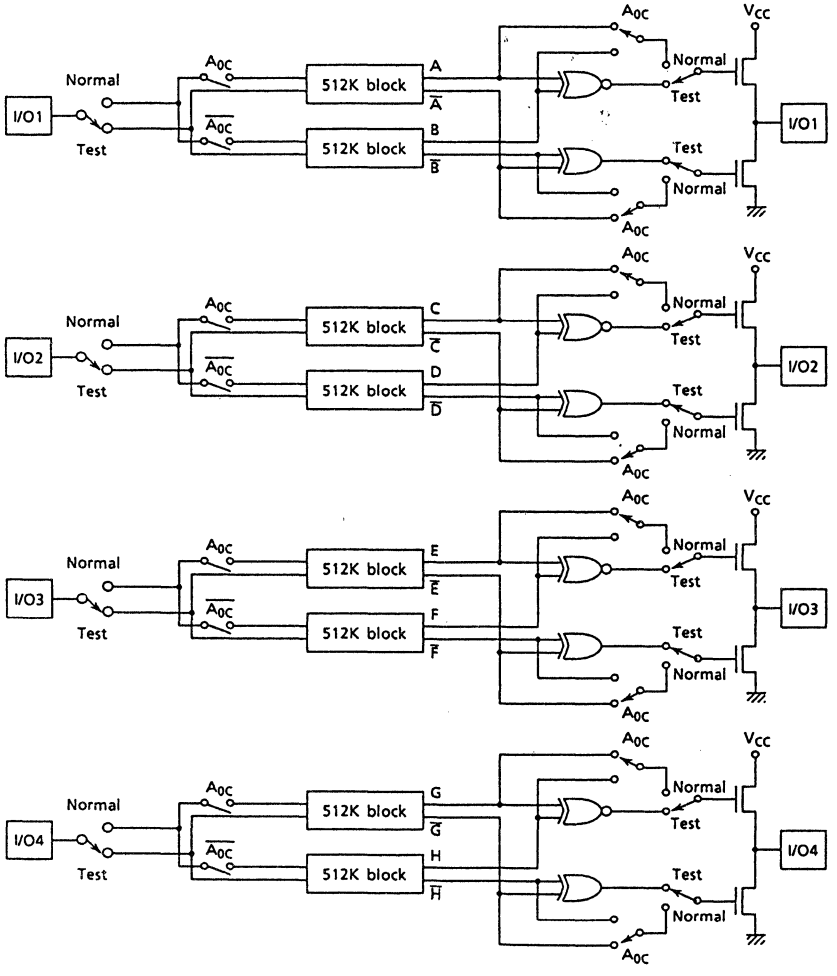


Fig. 1

NOTES

* This is advanced information and specifications are subject to change without notice.

1,048,576 WORD x 4 BIT DYNAMIC RAM

DESCRIPTION

The TC514402J/Z is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514402J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514402J/Z to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include sinlge power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

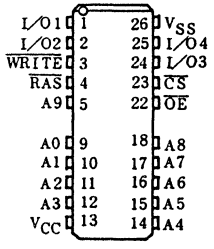
- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

		TC514402J/Z-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{SC}	Static Column Mode Cycle Time	45ns	55ns

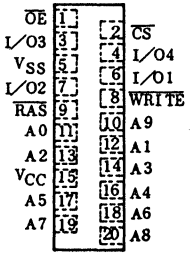
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  578mW MAX. Operating (TC514402J/Z-80)
  495mW MAX. Operating (TC514402J/Z-10)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Static Column Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package Plastic SOJ: TC514402J
  Plastic ZIP: TC514402Z

PIN CONNECTION (TOP VIEW)

Plastic SOJ



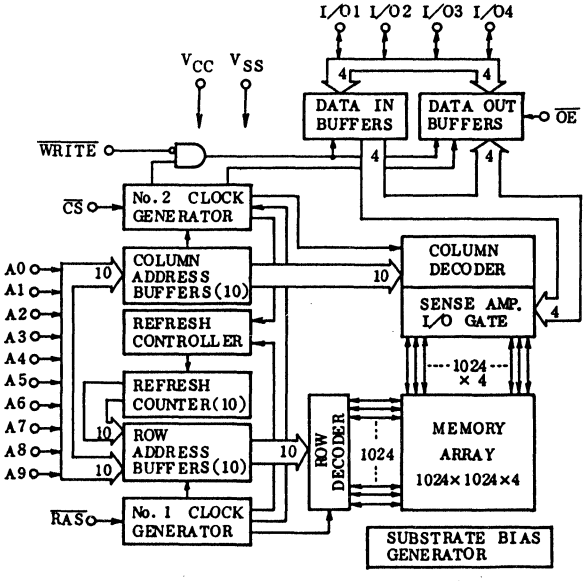
Plastic ZIP



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514402J/Z-80	-	105	mA	3,4,5
		TC514402J/Z-10	-	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514402J/Z-80	-	105	mA	3,5
		TC514402J/Z-10	-	90		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	TC514402J/Z-80	-	85	mA	3,4,5
		TC514402J/Z-10	-	75		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514402J/Z-80	-	105	mA	3
		TC514402J/Z-10	-	90		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514402J/Z -80		TC514402J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	205	-	245	-	ns	
t_{SC}	Static Column Mode Cycle Time	45	-	55	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	110	-	135	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	40	-	50	ns	9,15
t_{ALW}	Access Time from Last Write	-	75	-	95	ns	9,16
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	25	-	30	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CS}$ Hold Time	80	-	100	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	200,000	25	200,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	10	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	90	-	115	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	50	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514402J/Z -80		TC514402J/Z -10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	-	10	-	ns	17
t_{LWAD}	Last Write to Column Address Delay Time	20	35	25	45	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	75	-	95	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	20	-	ns	
t_{WCR}	Write Commadn Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{WI}	WRITE Inactive Time	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	20	-	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time	50	-	65	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	110	-	135	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	70	-	85	-	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	25	-	ns	
t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	25	-	ns	
t_{WTS}	Write Command Set-Up Time(Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514402J/Z -80		TC514402J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	155	-	185	-	ns	
t_{SC}	Static Column Mode Cycle Time	50	-	60	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	105	ns	9,14,15
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	30	ns	9,14
t_{AA}	Access Time from Column Address	-	45	-	55	ns	9,15
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	105	10,000	ns	
t_{RASC}	$\overline{TAS}$ Pulse Width (Static Column Mode)	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{TAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CS}$ Hold Time	85	-	105	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	200,000	30	200,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	

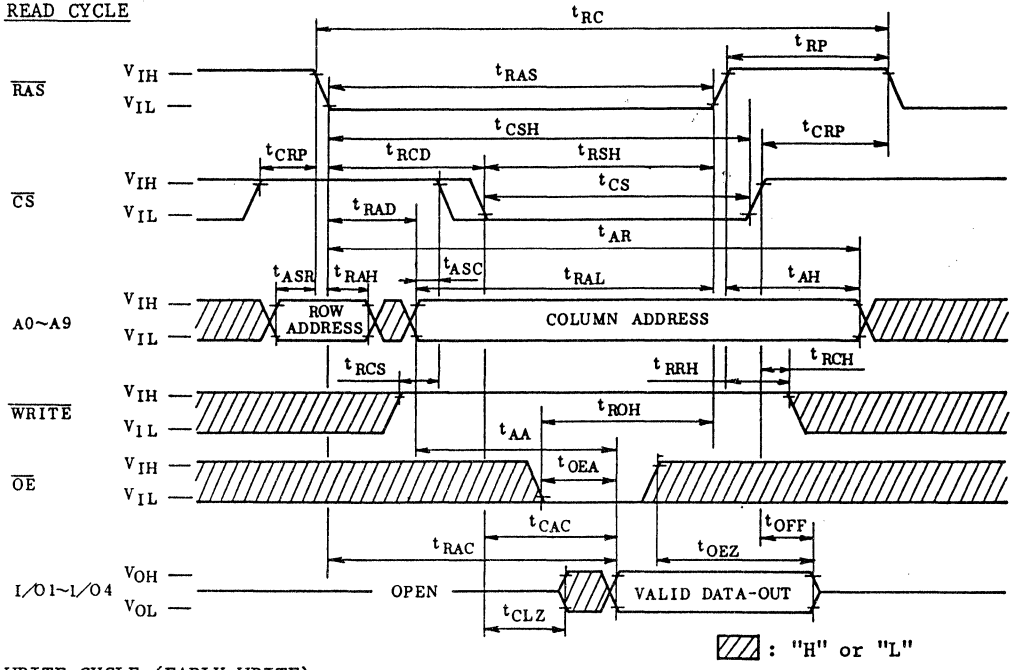
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	
C_O	Input Output Capacitance (I/O1∿I/O4)	-	7	

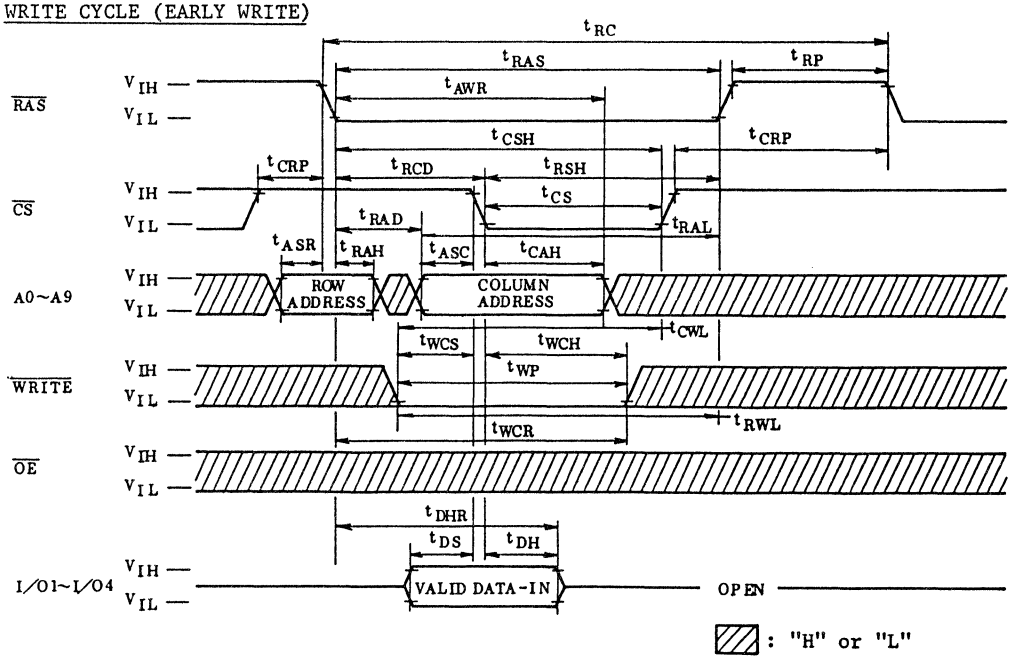
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specificied values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}$=V_{IL}.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=5ns.
8. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
16. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
17. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

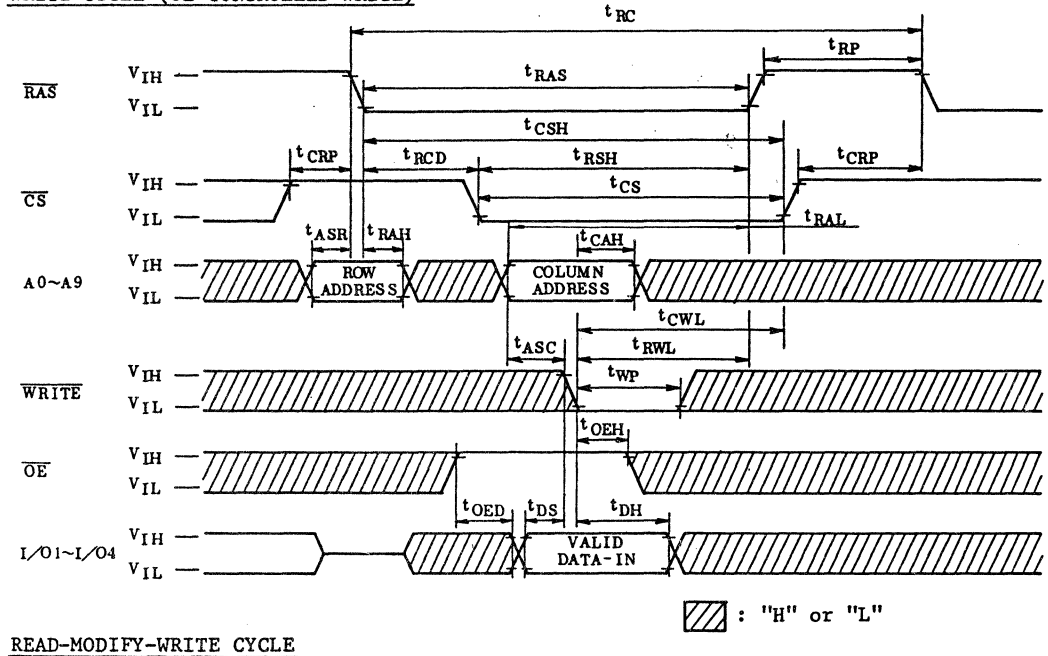
READ CYCLE



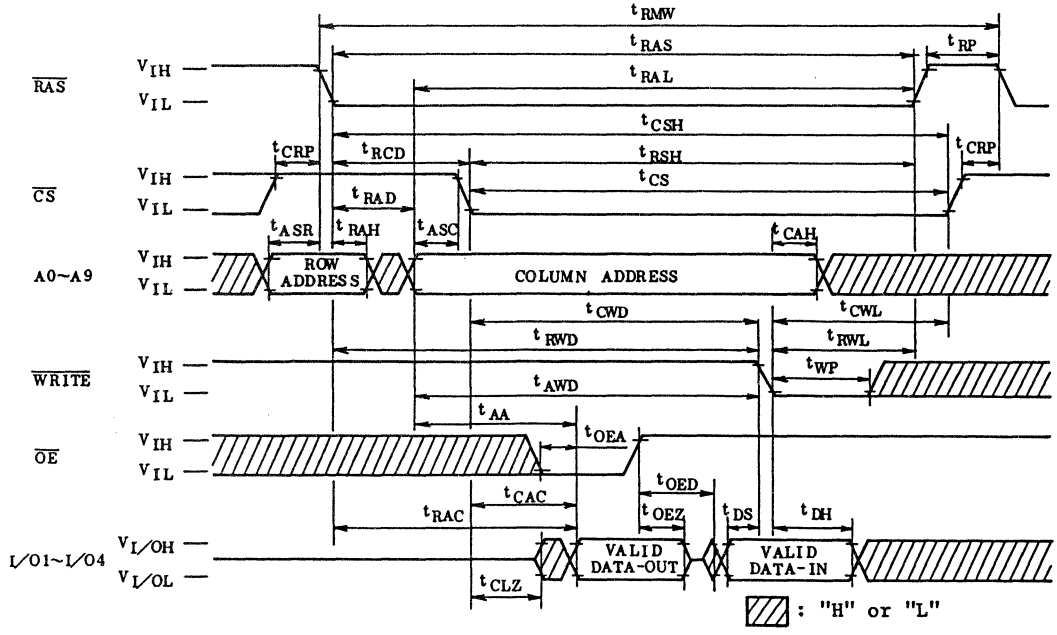
WRITE CYCLE (EARLY WRITE)



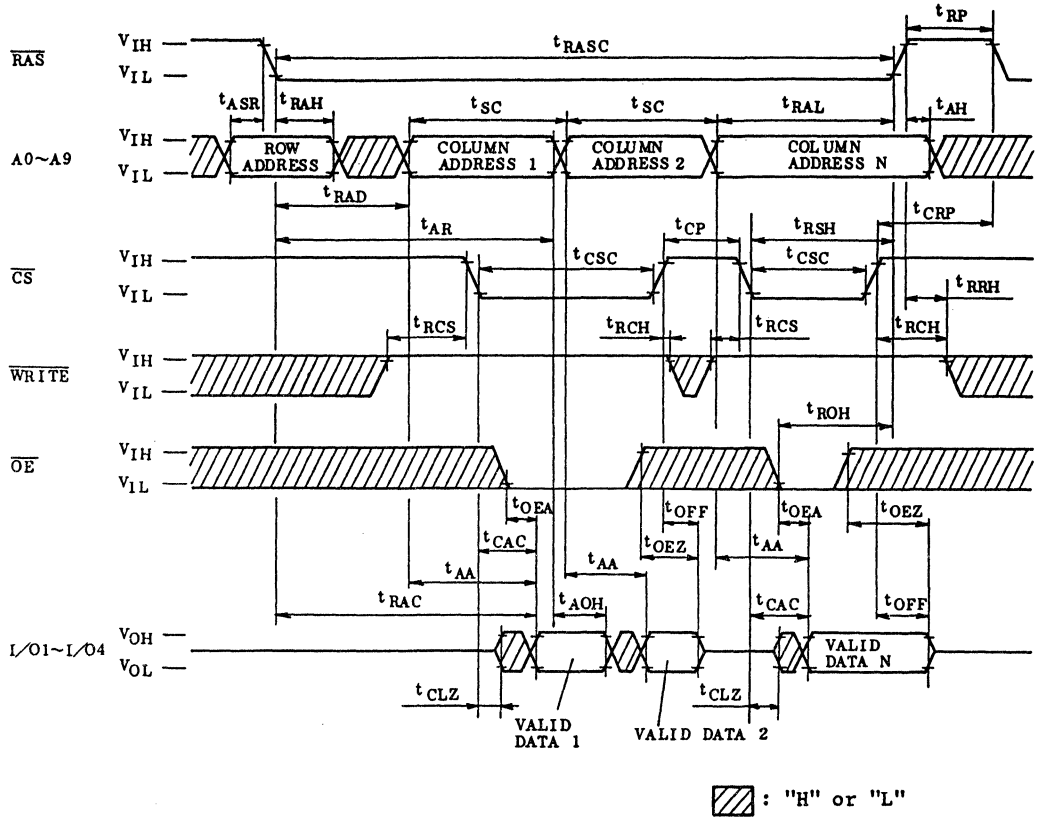
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



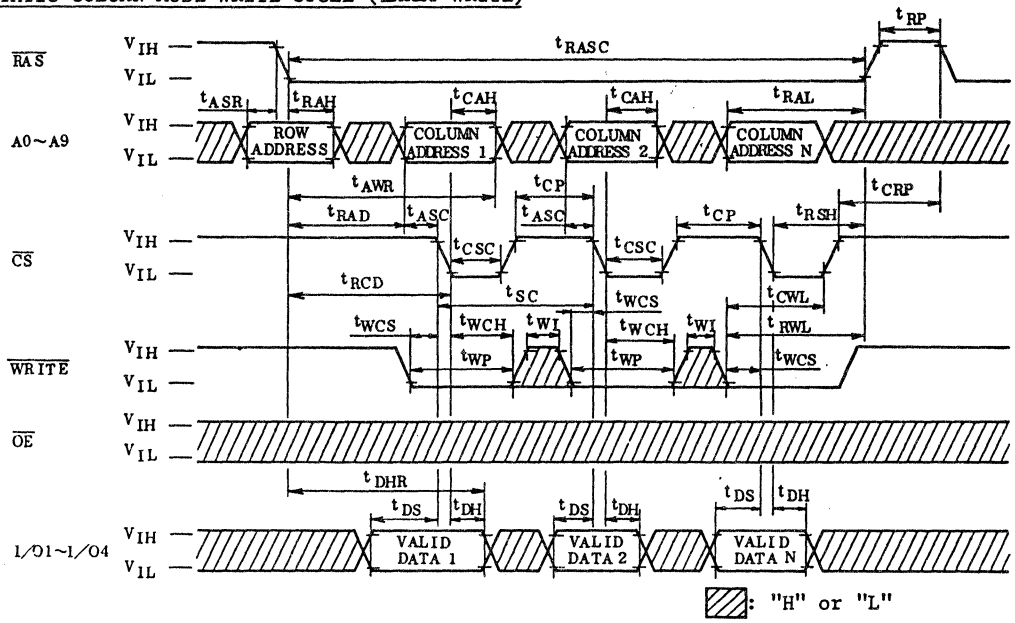
READ-MODIFY-WRITE CYCLE



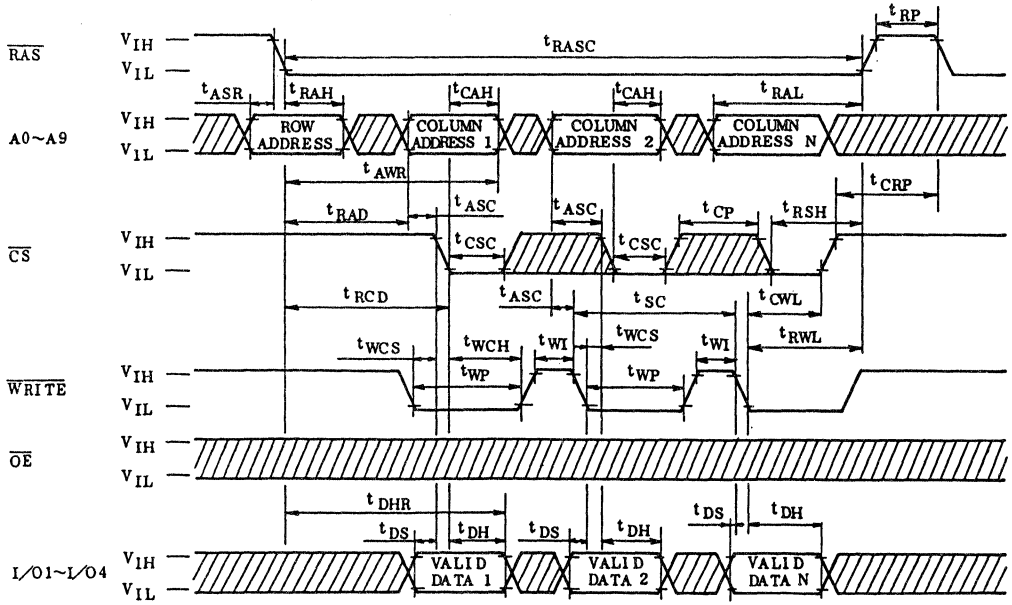
STATIC COLUMN MODE READ CYCLE



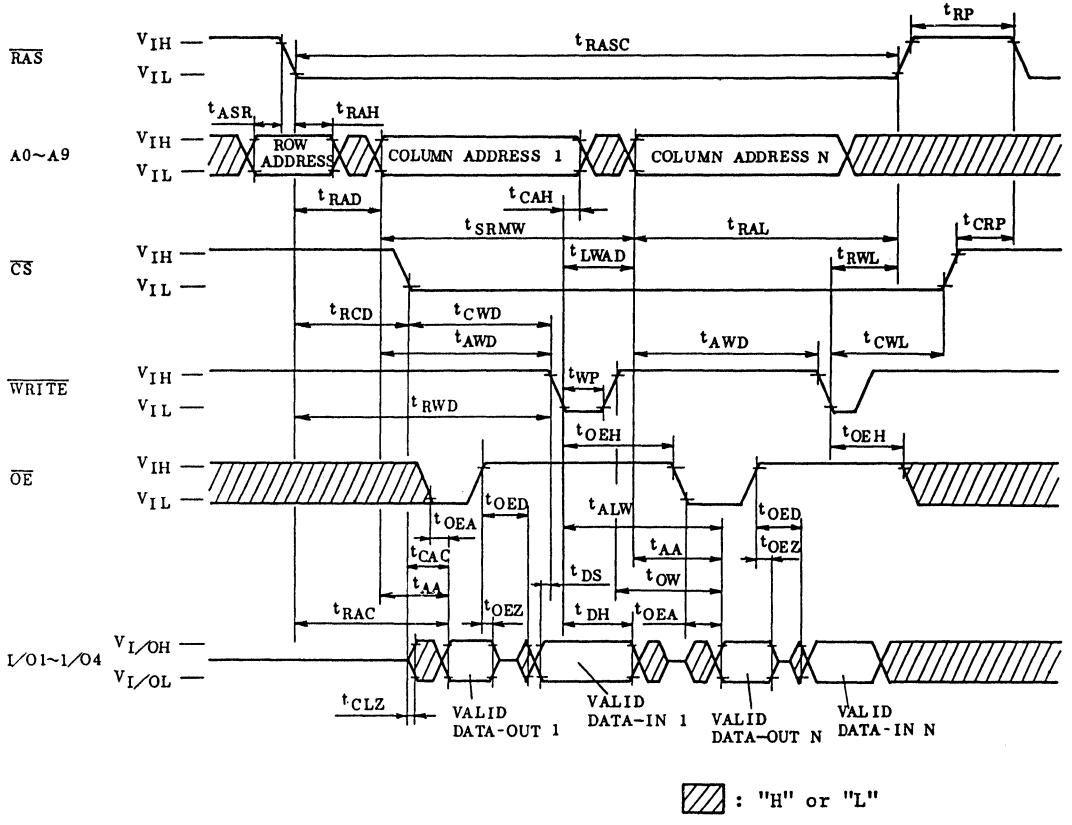
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



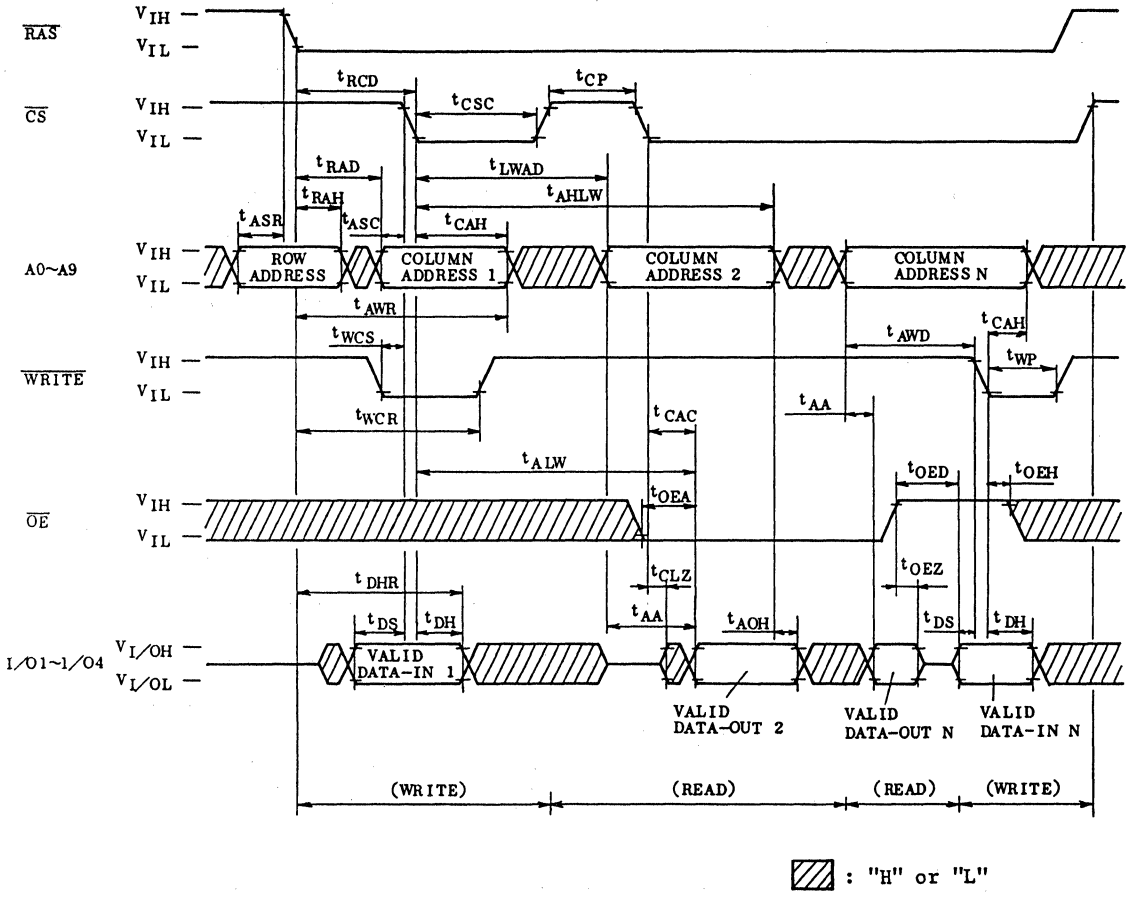
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



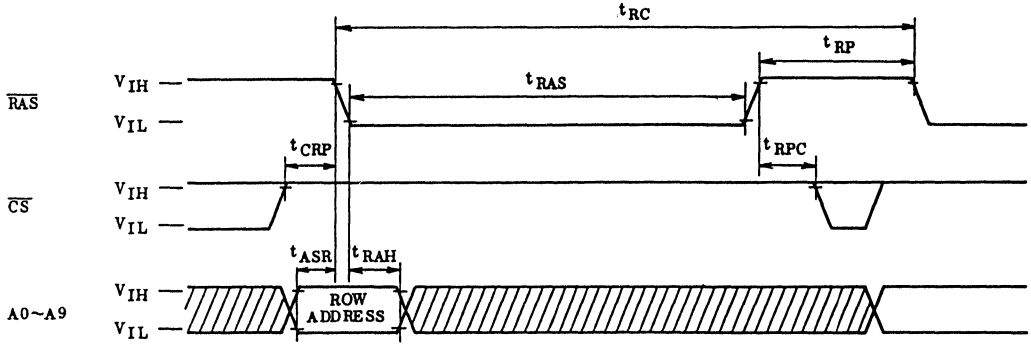
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE



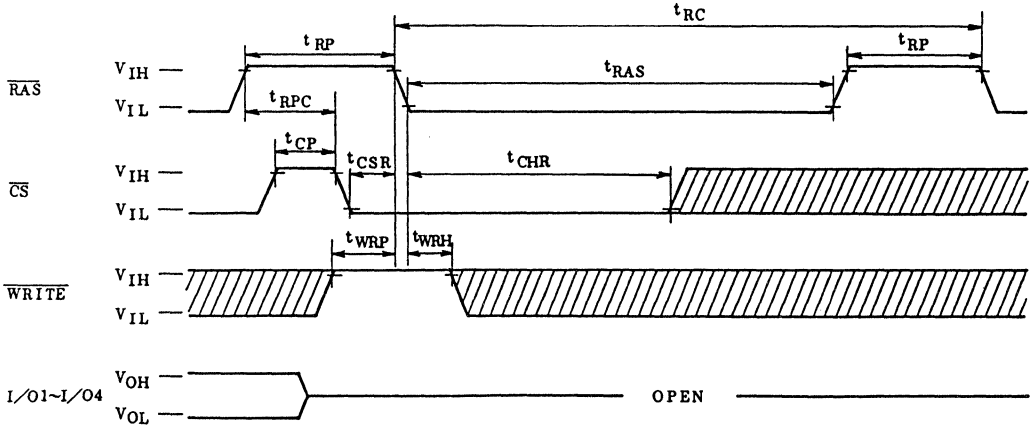
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$="H" or "L"

▨ : "H" or "L"

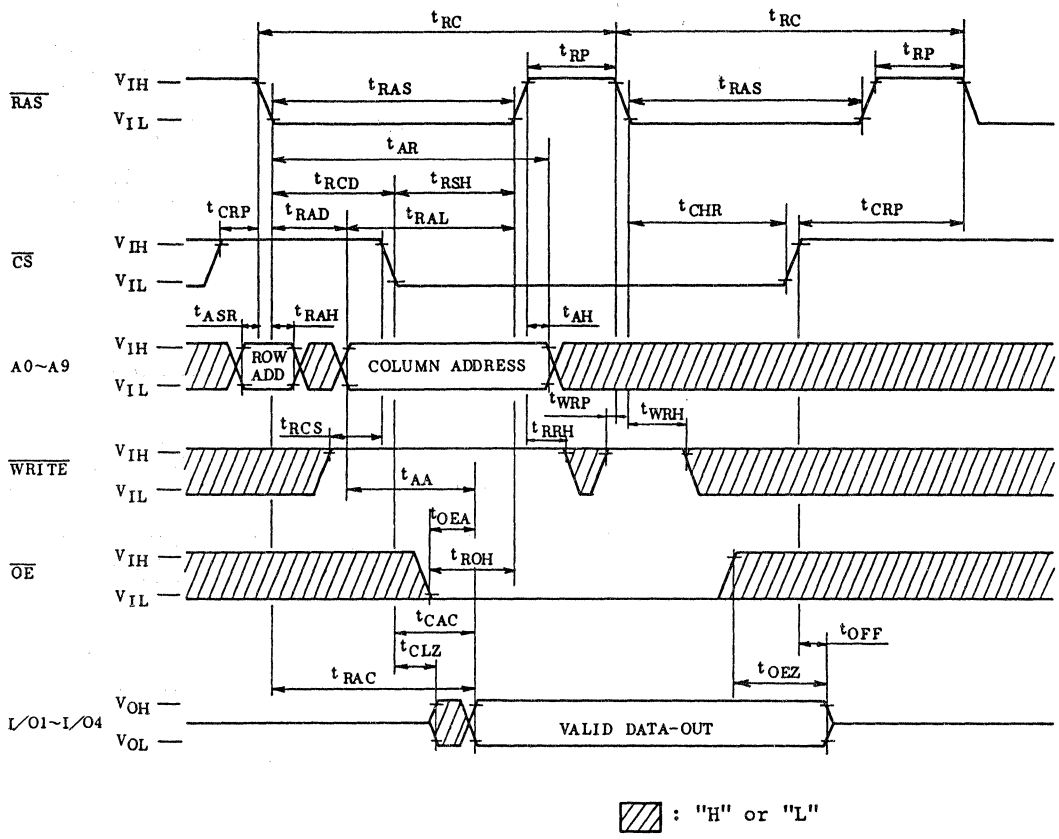
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



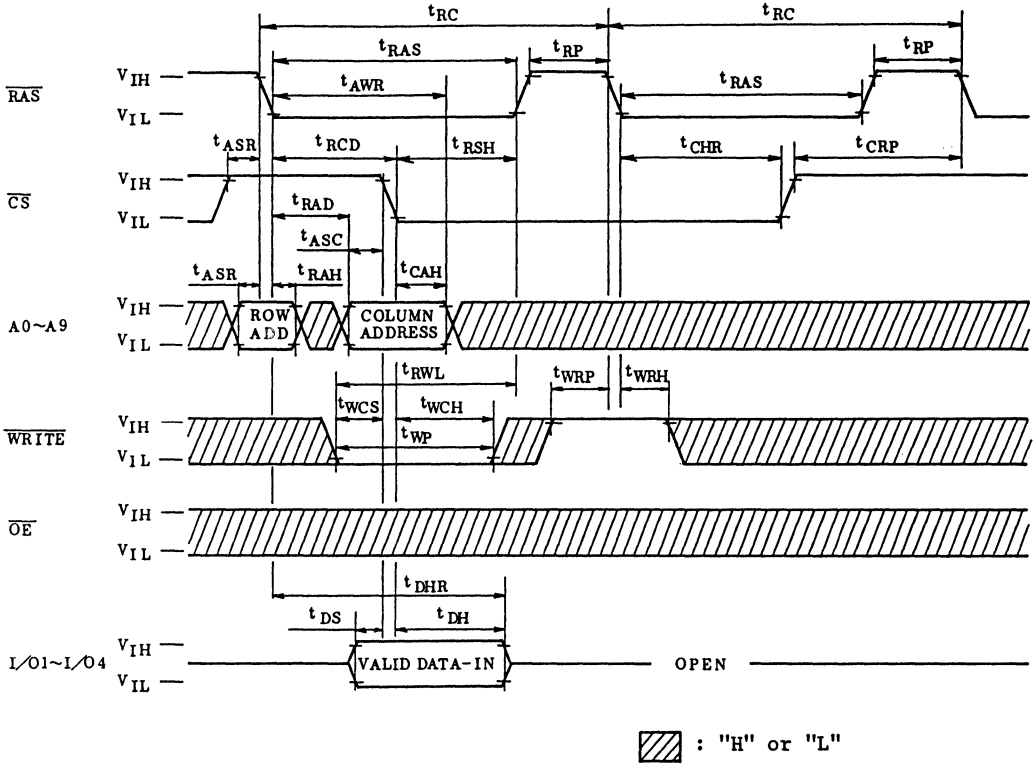
Note: $\overline{OE}$, A0 ∿ A9="H" or "L"

▨ : "H" or "L"

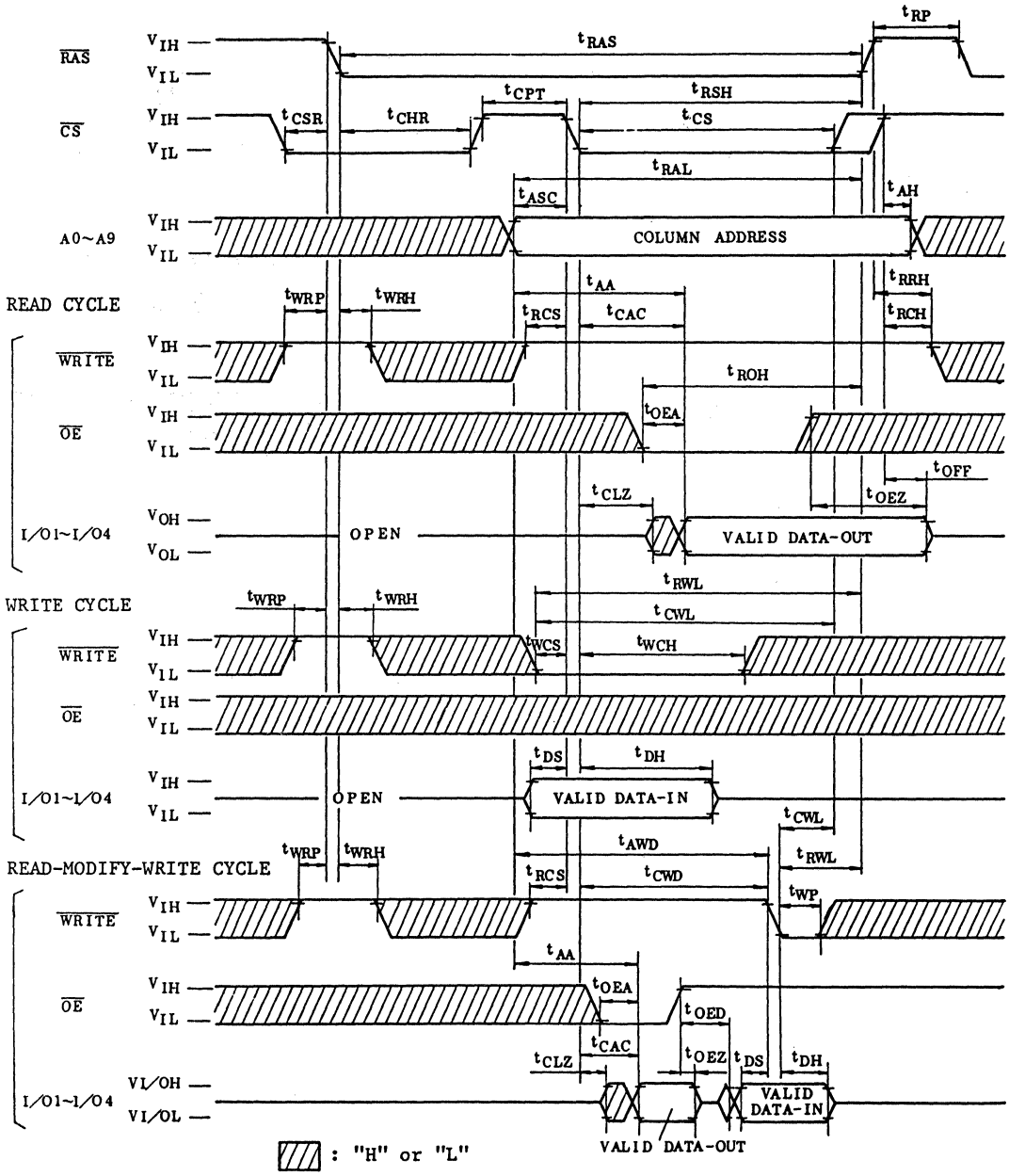
HIDDEN REFRESH CYCLE (READ)



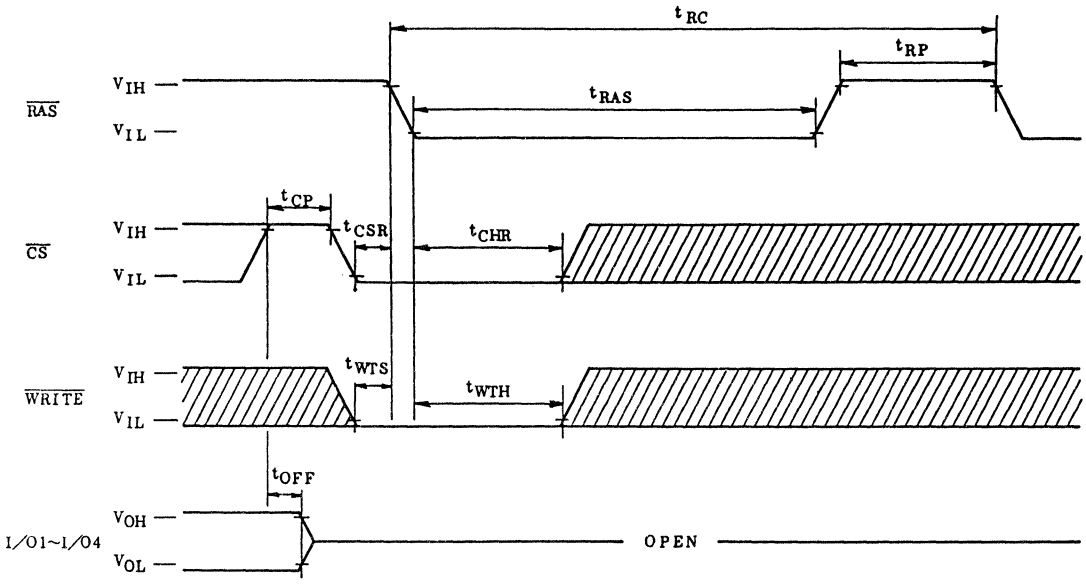
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



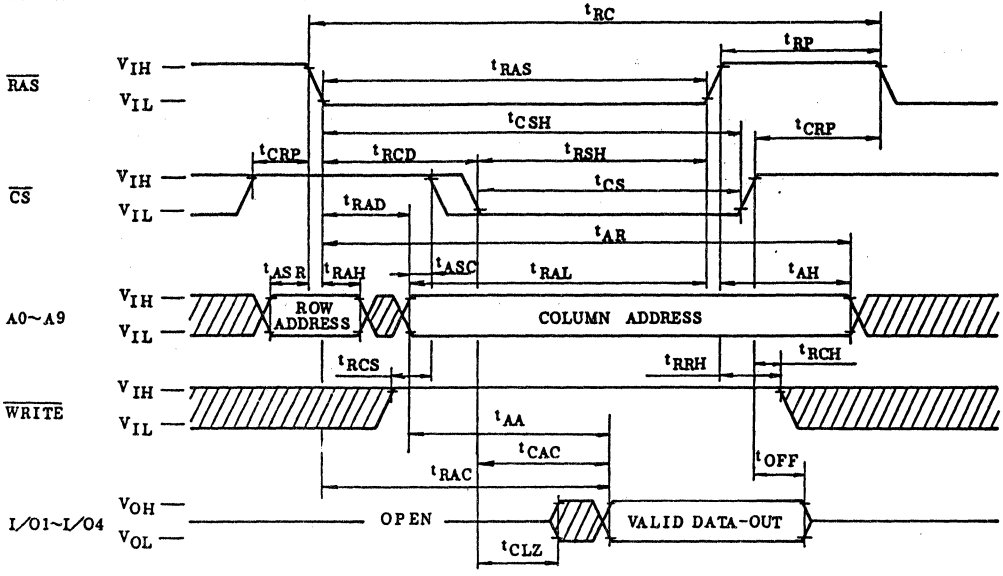
$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



Note: $\overline{\text{OE}}$, A0 ∿ A9: "H" or "L"

▨ : "H" or "L"

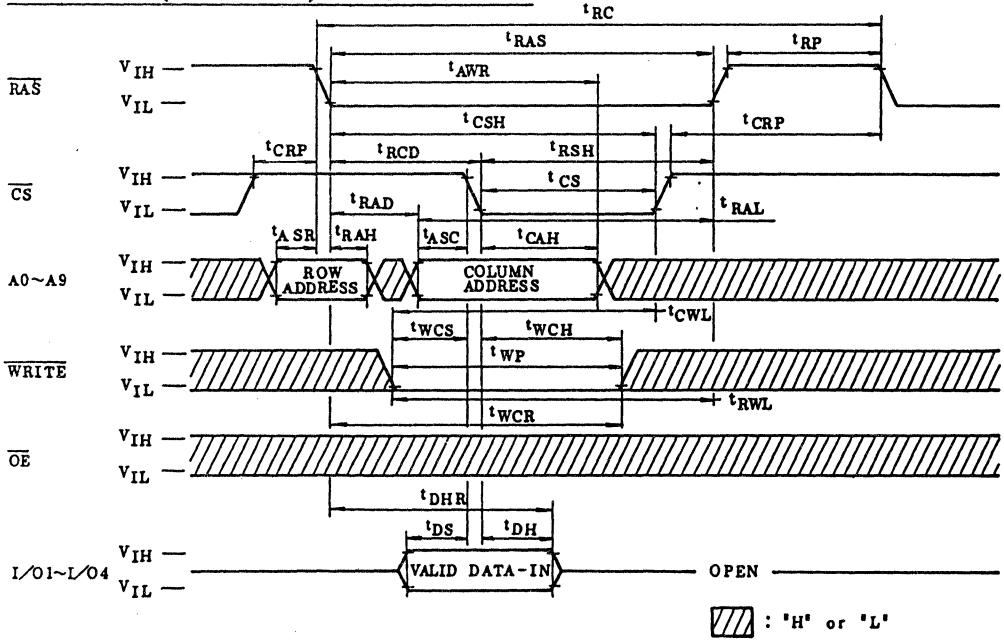
READ CYCLE IN THE TEST MODE



Note: $\overline{OE}$="L"

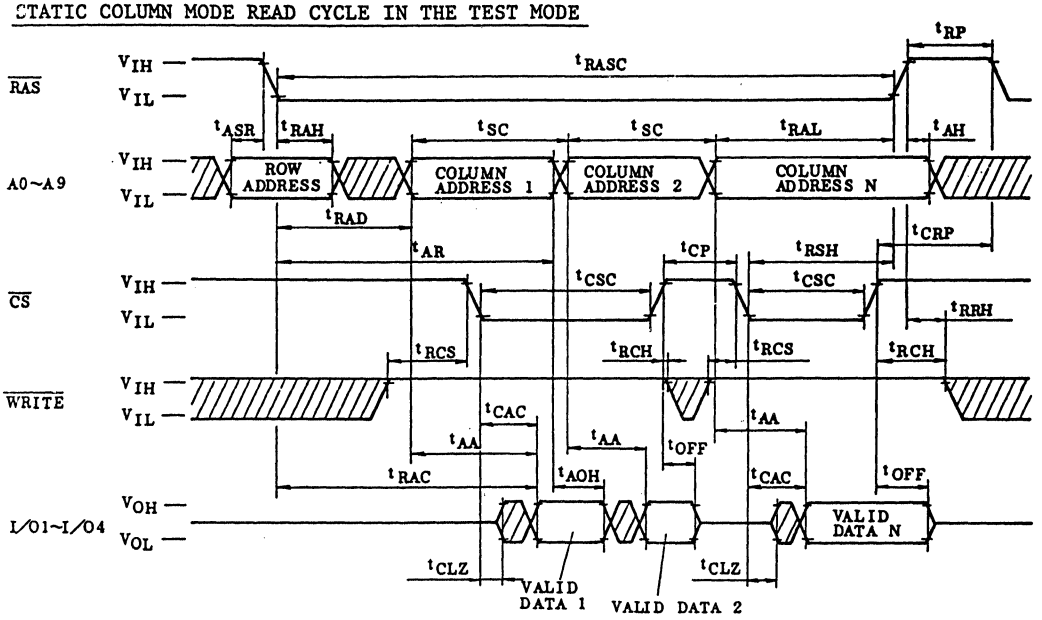
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



▨ : "H" or "L"

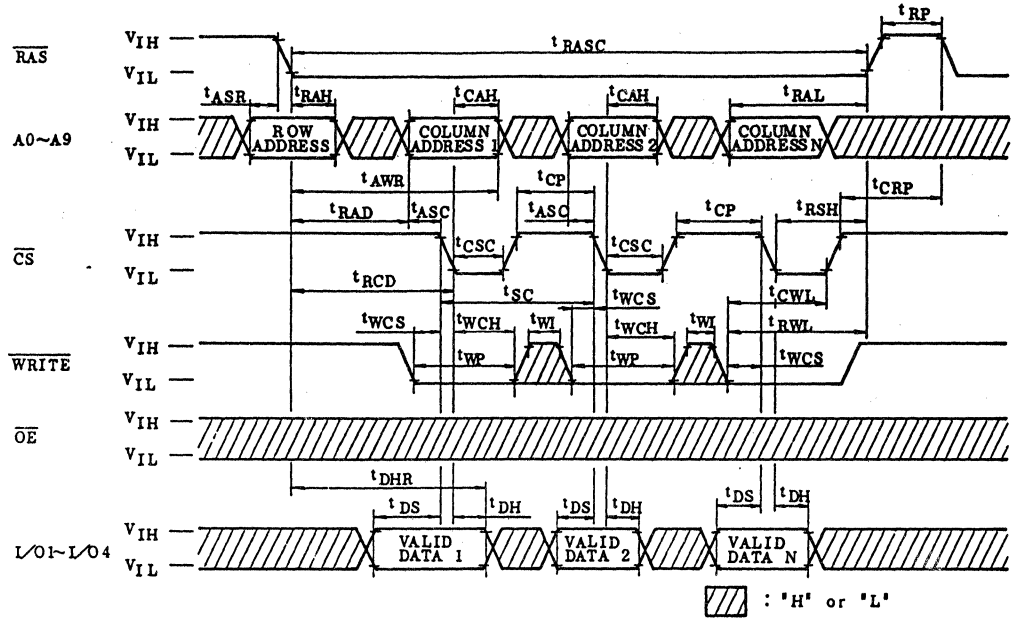
STATIC COLUMN MODE READ CYCLE IN THE TEST MODE



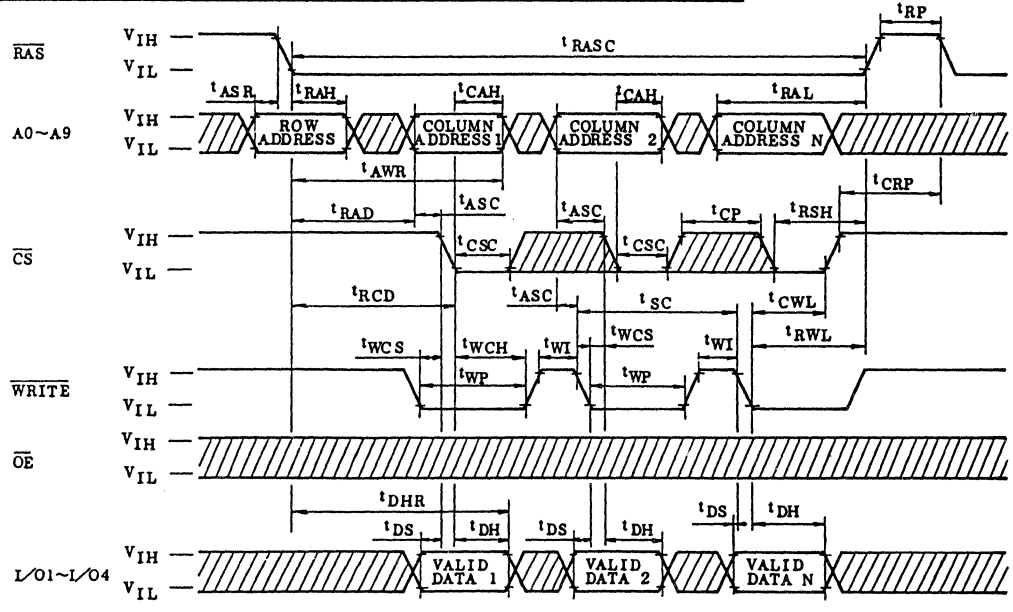
Note: $\overline{OE}$="L"

▨ : "H" or "L"

STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



TEST MODE

The TC514402J/Z is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. AOC is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514402J/Z. In "Test Mode", the 1M × 4 DRAM can be tested as if it were a 512K × 4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

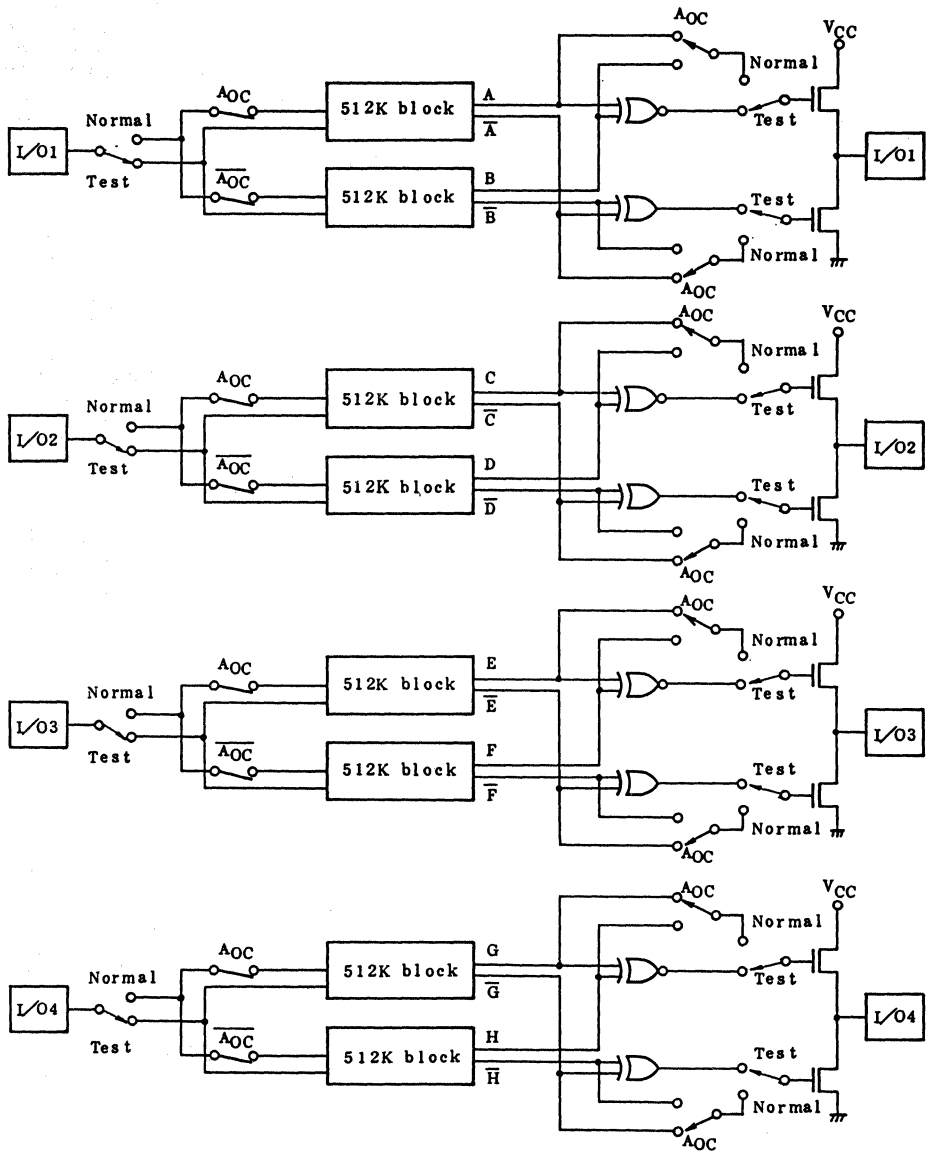


Fig. 1

1048,576 WORD × 4 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514402AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514402AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514402AP/AJ/ASJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performace logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

	TC514402AP/AJ/ASJ/AZ-60
t_{RAC} $\overline{RAS}$ Access Time	60ns
t_{AA} Column Address Access Time	30ns
t_{CAC} $\overline{CS}$ Access Time	20ns
t_{RC} Cycle Time	110ns
t_{SC} Static Column Mode Cycle Time	35ns

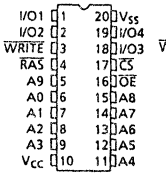
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  660mW MAX. Operating
  (TC514402AP/AJ/ASJ/AZ-60)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and outputs TTL Compatible
- 1024 refresh cycles/16ms
- Package
  TC514402AP : DIP20-P-300C
  TC514402AJ : SOJ26-P-350
  TC514402ASJ : SOJ26-P-300A
  TC514402AZ : ZIP20-P-400A

PIN NAMES

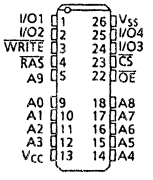
A0~A9	Address Inputs	$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe	I/O1~I/O4	Data Input/Output
$\overline{CS}$	Chip Select	V_{CC}	Power (+5V)
$\overline{WRITE}$	Read/Write Input	V_{SS}	Ground

PIN CONNECTION (TOP VIEW)

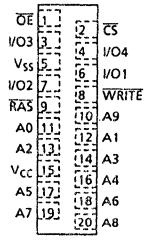
Plastic DIP



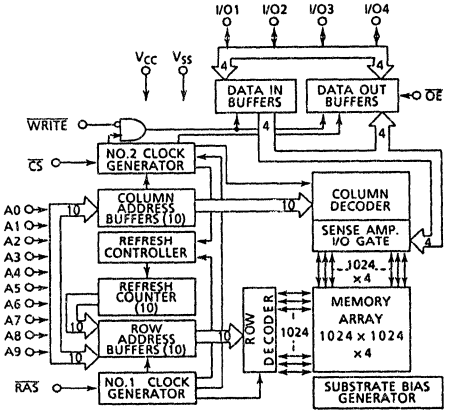
Plastic SOJ



Plastic ZIP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514402AP/AJ/ASJ/AZ-60	–	120	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC514402AP/AJ/ASJ/AZ-60	–	120	mA	3, 5
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, STATIC COLUMN Mode ($\overline{RAS} = \overline{CS} = V_{IL}$, Address Cycling: $t_{SC} = t_{SC}$ MIN.)	TC514402AP/AJ/ASJ/AZ-60	–	95	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514402AP/AJ/ASJ/AZ-60	–	120	mA	3, 5
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	–	ns	
t_{SC}	Static Column Mode Cycle Time	35	–	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	90	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	9,14 15
t_{CAC}	Access Time from $\overline{CS}$	–	20	ns	9,14
t_{AA}	Access Time from Column Address	–	30	ns	9,15
t_{ALW}	Access Time from Last Write	–	55	ns	9,16
t_{CLZ}	$\overline{CS}$ to output in Low-Z	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Addres	5	–	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	–	20	ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	60	200,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	60	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	200,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$ (READ CYCLE)	70	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	–	ns	17

SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-60		UNITS	NOTES
		MIN.	MAX.		
t_{LWAD}	Last Write to Column Address Delay Time	20	25	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	55	–	ns	
t_{RCS}	Read Command Set-up Time referenced to $\overline{CS}$	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	11
t_{WCH}	Write Command Hold Time (Output Data Disable)	10	–	ns	13
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{WI}	Write Command Inactive Time	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	ns	12
t_{DH}	Data-In Hold Time	15	–	ns	12
t_{REF}	Refresh Period	–	16	ms	
t_{WCS}	Write Command Set-UP Time (Output Data Disable)	0	–	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	50	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE Cycle)	90	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	–	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time($\overline{CS}$ before $\overline{RAS}$)	5	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time($\overline{CS}$ before $\overline{RAS}$)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	ns	

SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{WTS}	Write Command Set-Up Time	10	–	ns	
t_{WTH}	Write Command Hold Time	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time	10	–	ns	
t_{WRH}	WRITE to RAS Hold Time	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	115	–	ns	
t_{SC}	Static Column Mode Cycle Time	40	–	ns	
t_{RAC}	Access Time from $\overline{CS}$	–	65	ns	9,14 15
t_{CAC}	Access Time from $\overline{CS}$	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	ns	9,15
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	65	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	ns	
t_{CSH}	$\overline{CS}$ Hold Time	65	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	200,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	ns	

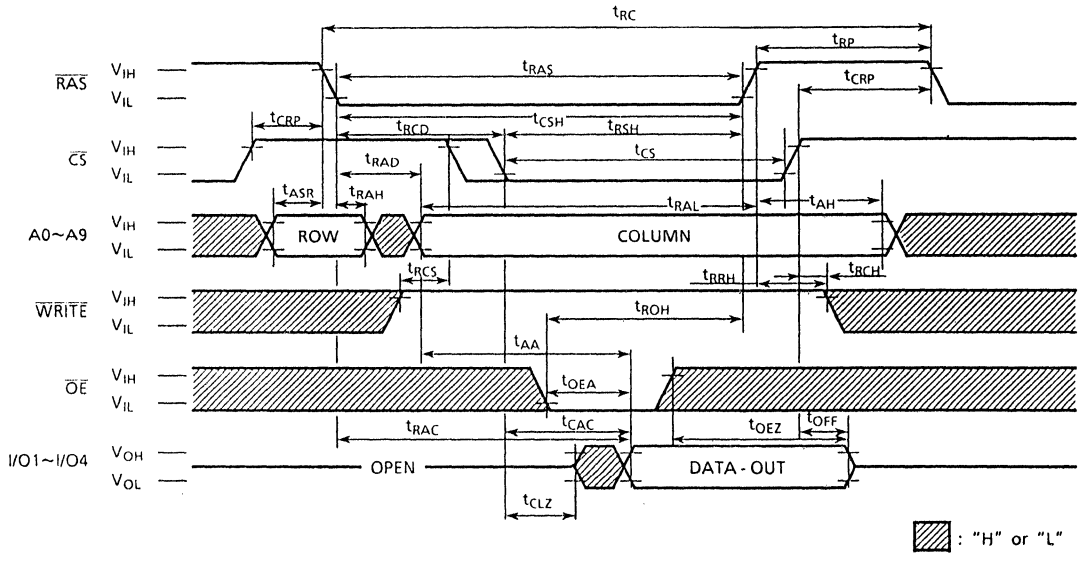
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	–	7	pF

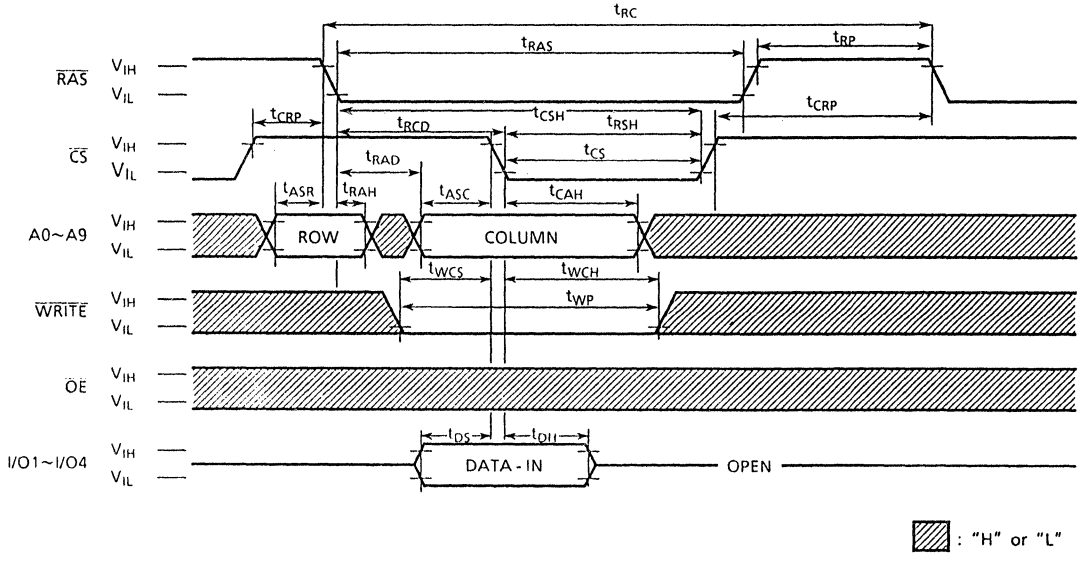
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ refresh cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.) the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
16. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met.
    t_{LWAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled by t_{AA}.
17. t_{AH} is the condition to latch column address ewhen $\overline{RAS}$ has rised up.

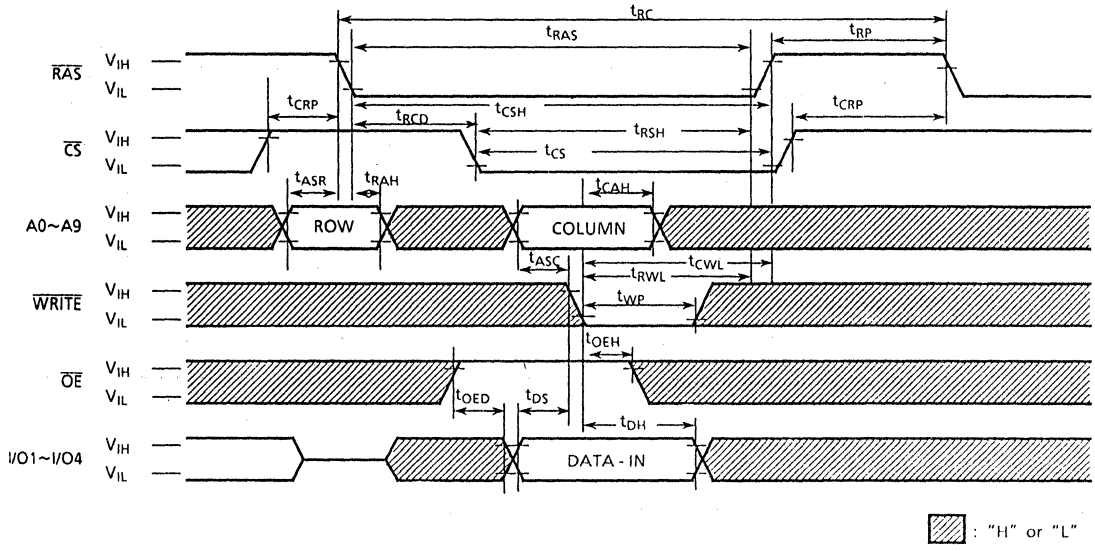
READ CYCLE



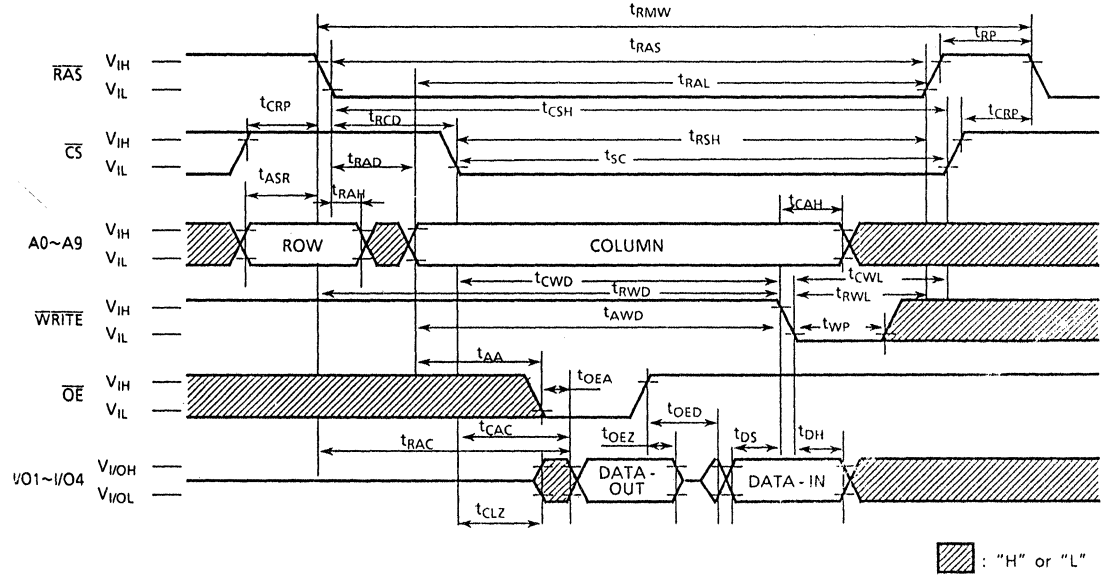
WRITE CYCLE (EARLY WRITE)



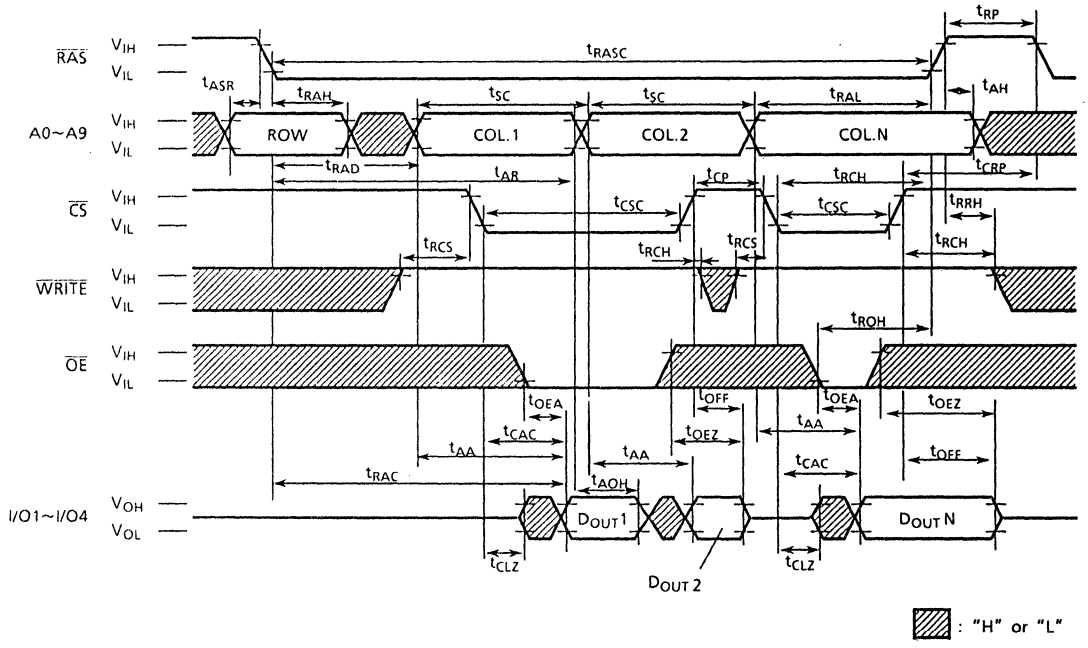
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



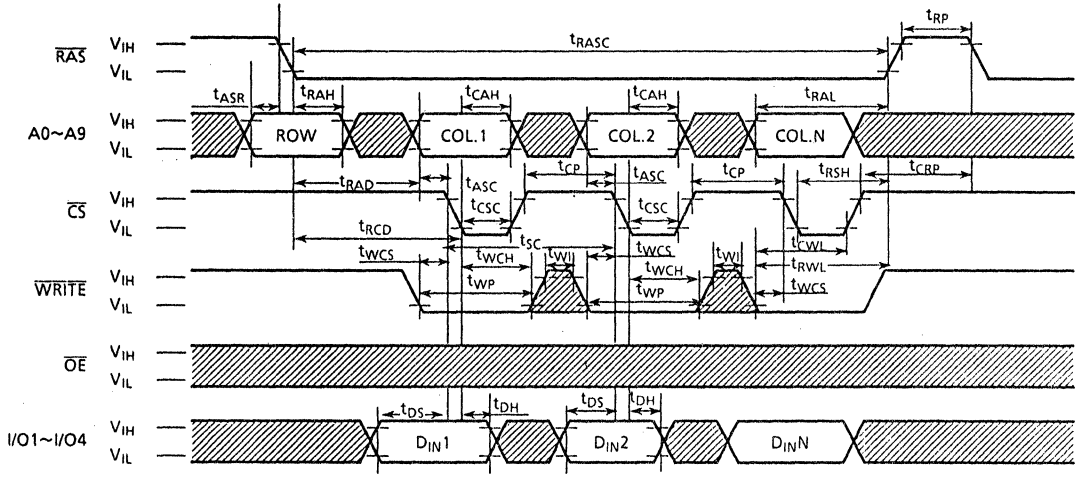
READ - MODIFY - WRITE CYCLE



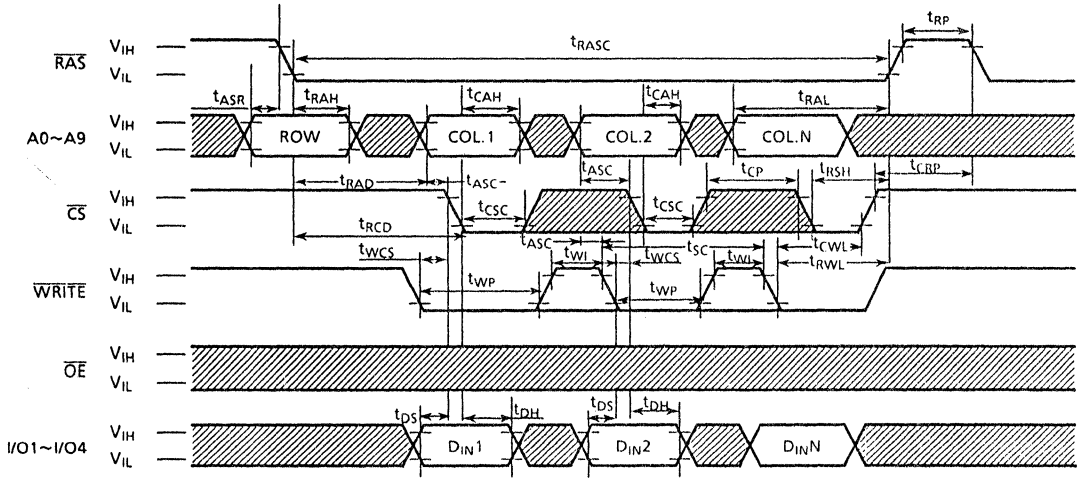
STATIC COLUMN MODE READ CYCLE



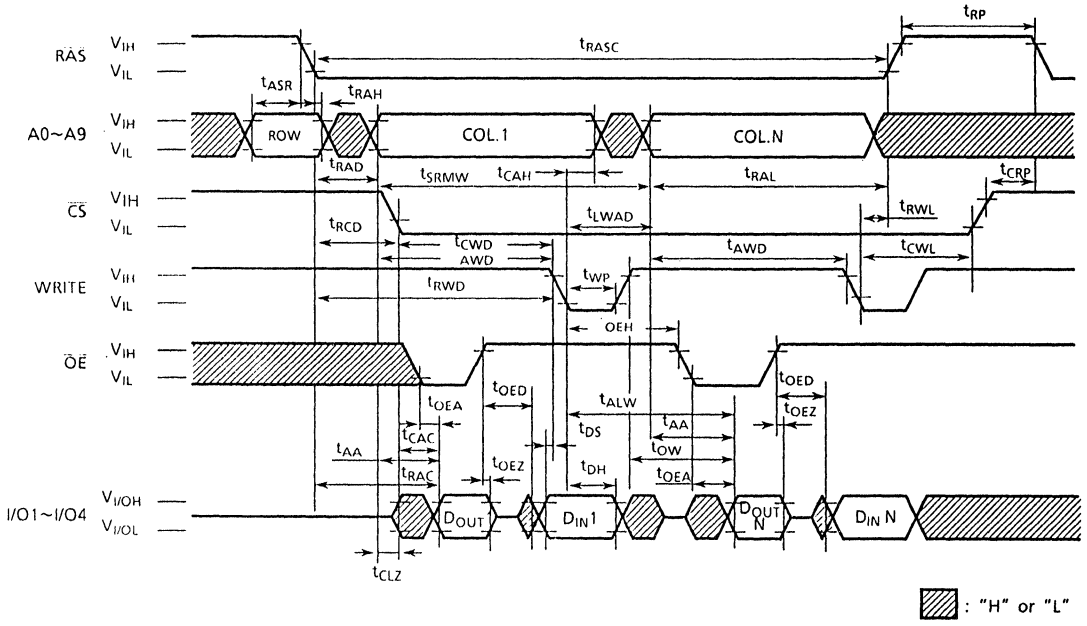
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



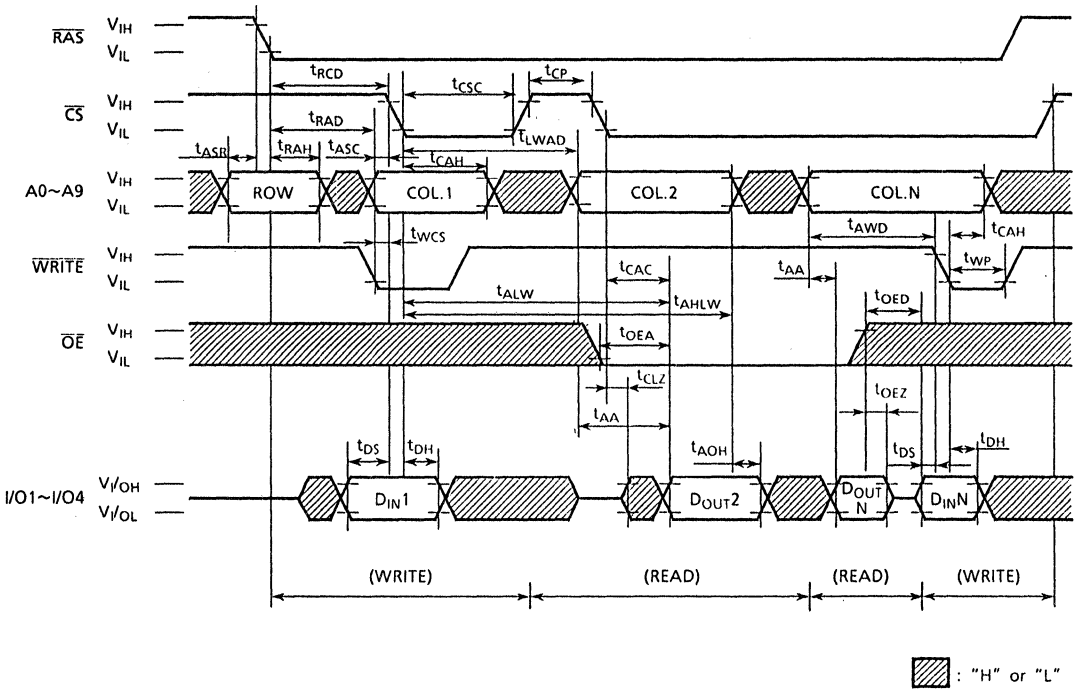
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



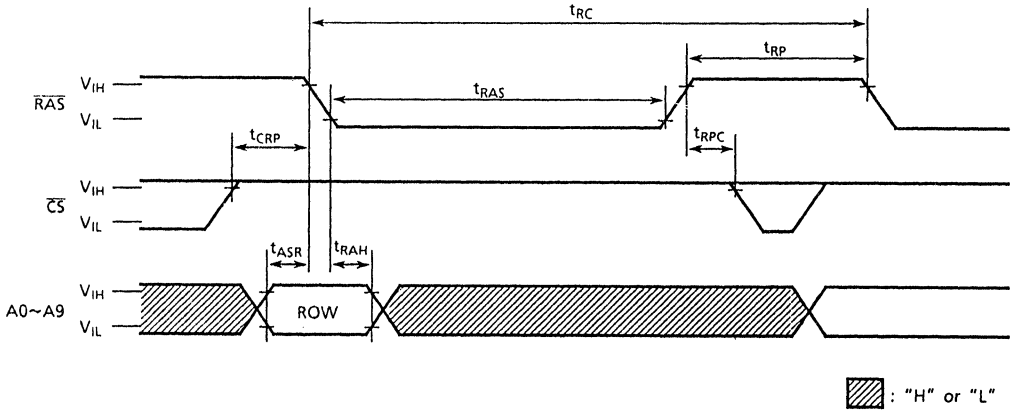
STATIC COLUMN MODE READ - MODIFY - WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

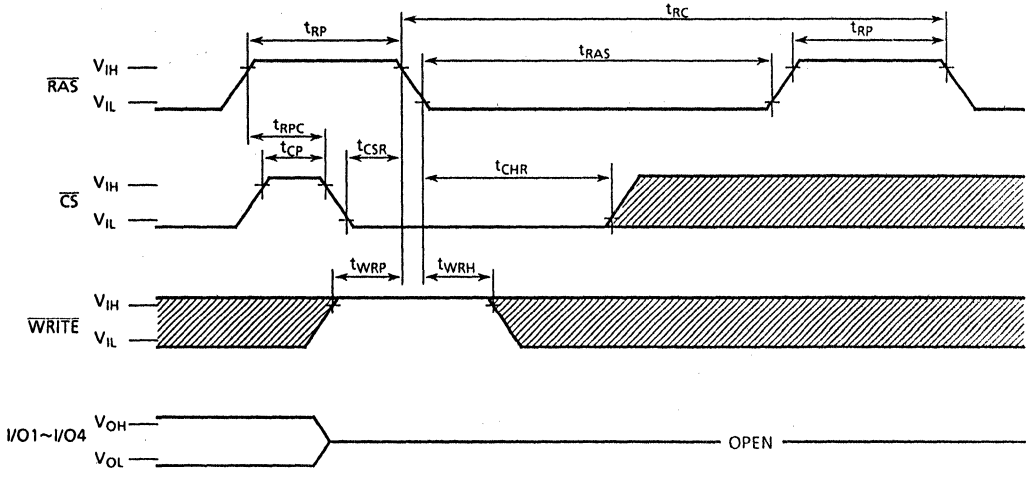


$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

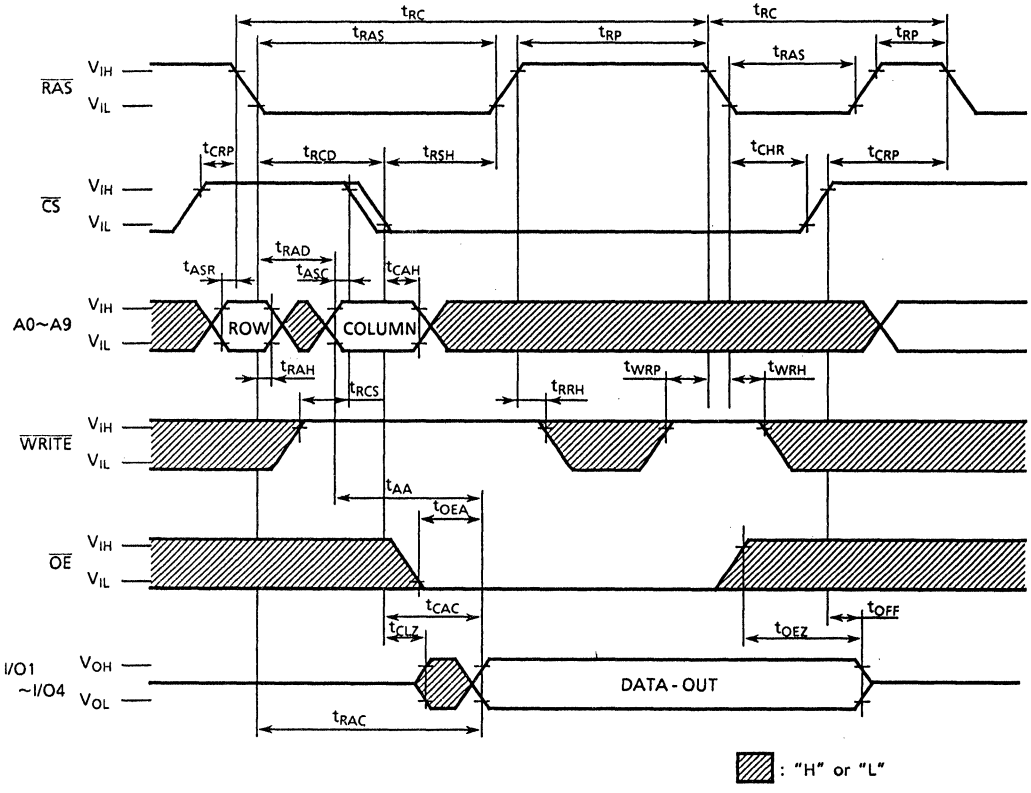
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



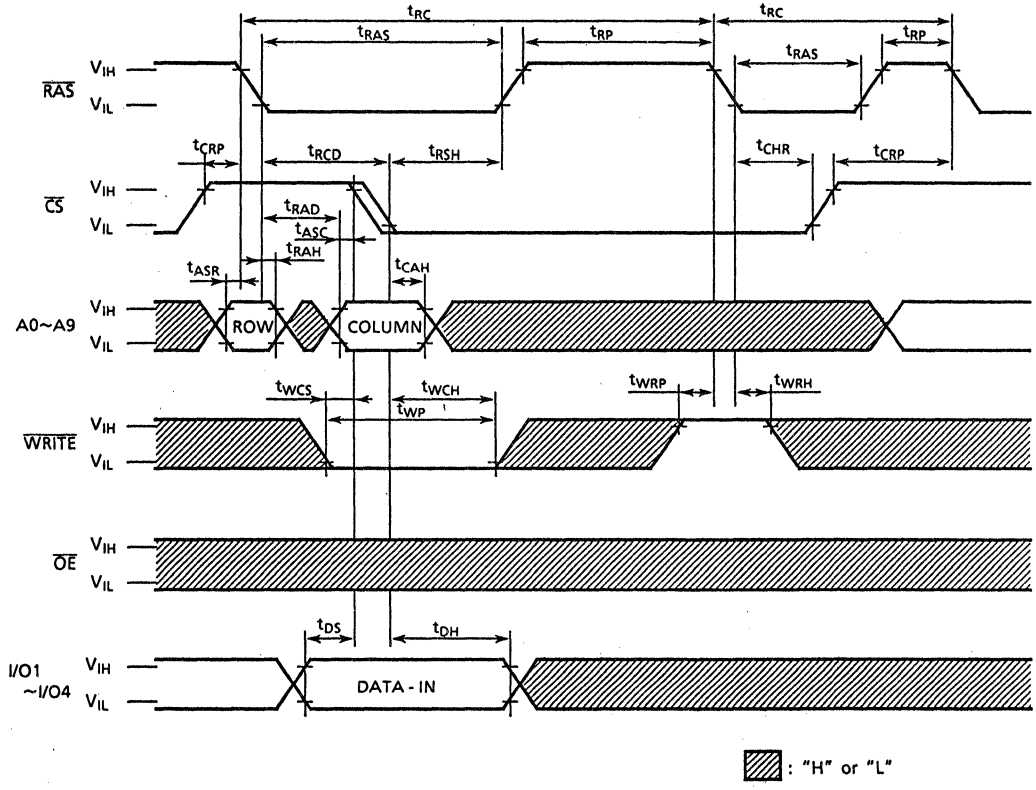
Note: $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

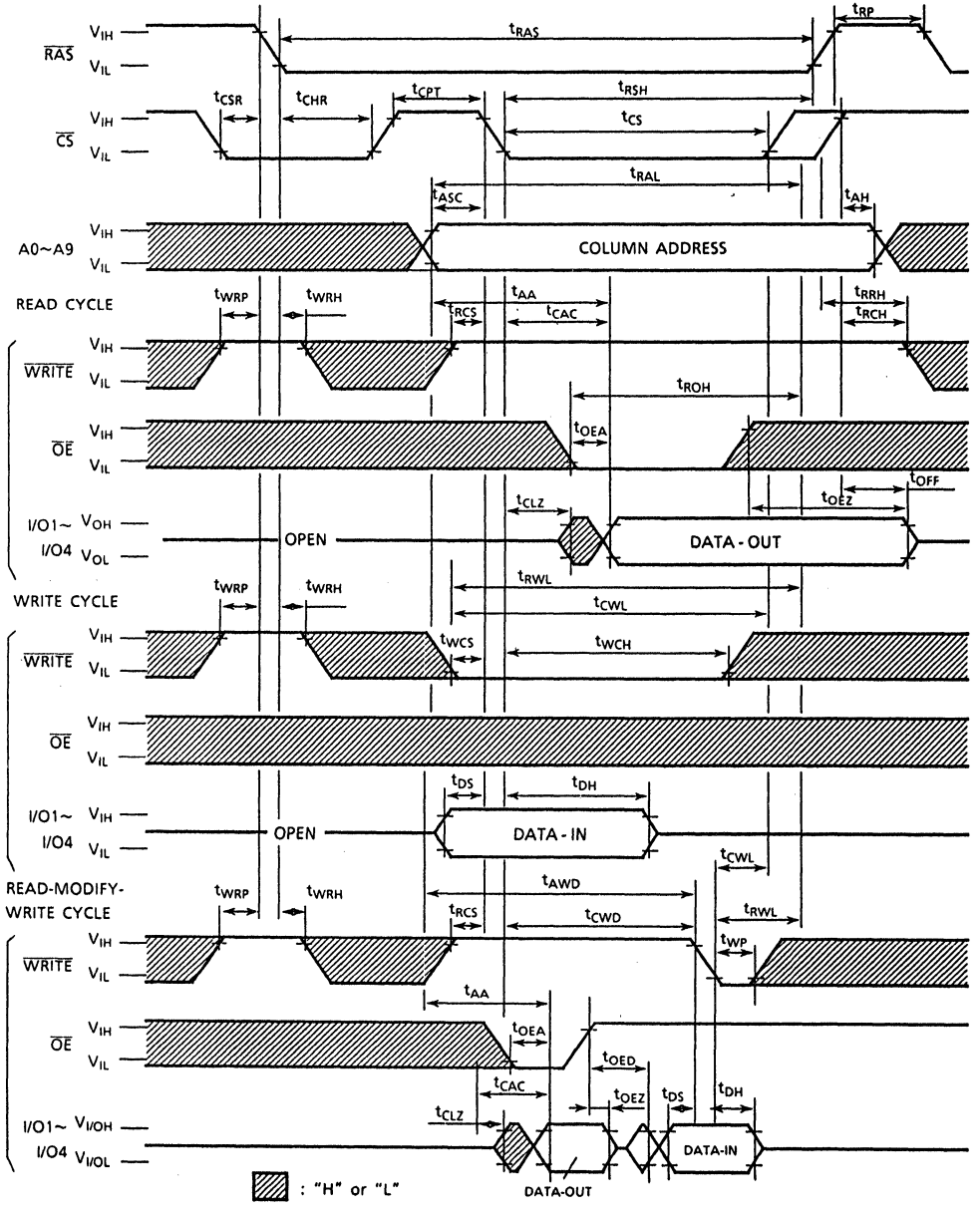
HIDDEN REFRESH CYCLE (READ)



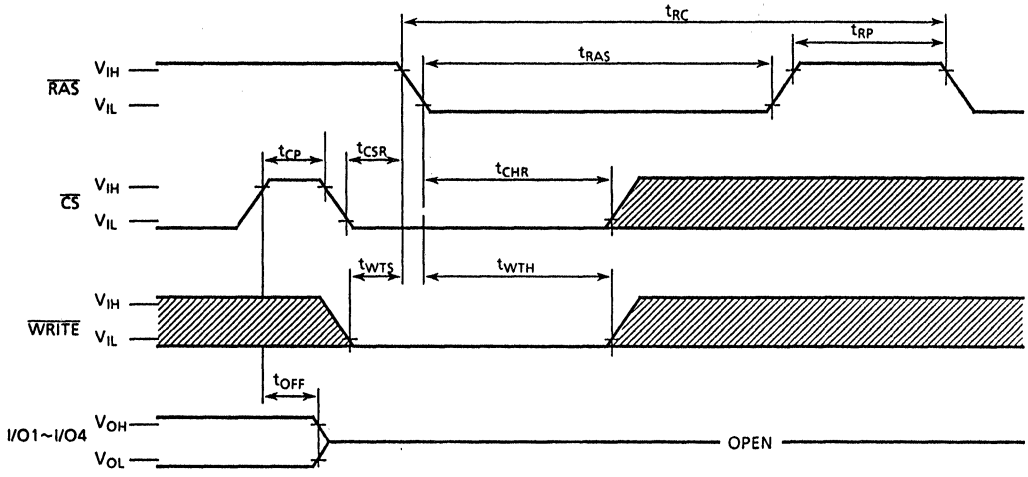
HIDDEN REEFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, CS BEFORE RAS REFRESH CYCLE



Note: $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC514402AP/AJ/ASJ/AZ is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A0C is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514402AP/AJ/ASJ/AZ. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle "or "$\overline{\text{RAS}}$ Only Refresh Cycle" put it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in cace of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

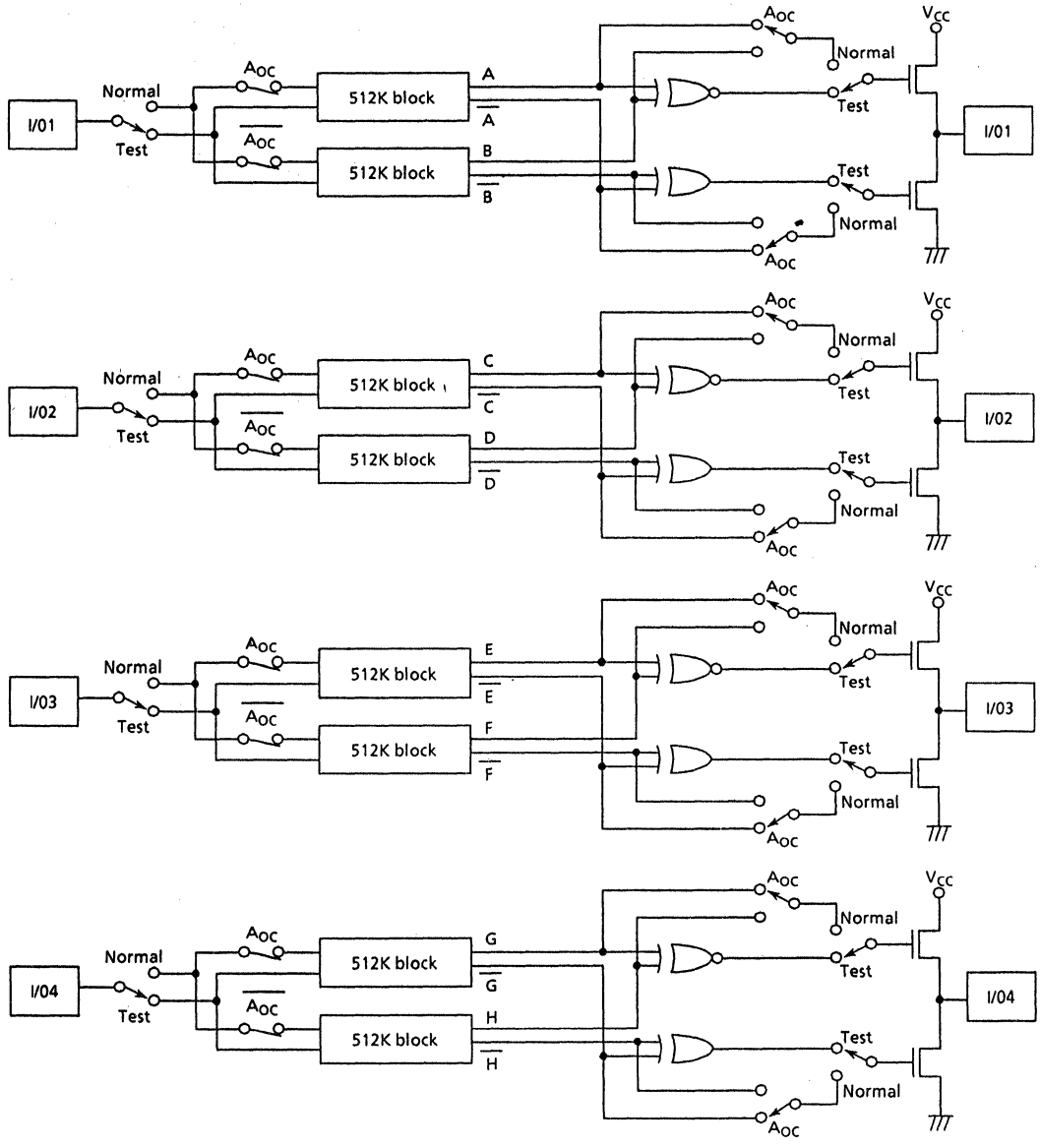


Fig. 1

1048,576 WORD × 4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514402AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514402AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514402AP/AJ/ASJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performace logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

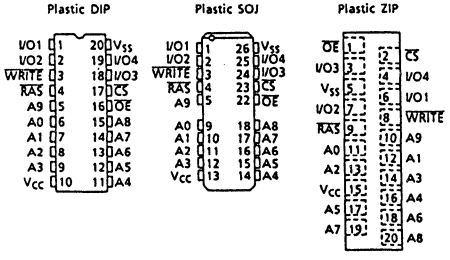
		TC514402AP/AJ/ASJ/ AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{SC}	Static Column Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 550mW MAX. Operating (TC514402AP/AJ/ASJ/AZ-70)
  - 468mW MAX. Operating (TC514402AP/AJ/ASJ/AZ-80)
  - 413mW MAX. Operating (TC514402AP/AJ/ASJ/AZ-10)
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and outputs TTL Compatible
- 1024 refresh cycles/16ms
- Package
  - TC514402AP : DIP20-P-300C
  - TC514402AJ : SOJ26-P-350
  - TC514402ASJ : SOJ26-P-300A
  - TC514402AZ : ZIP20-P-400A

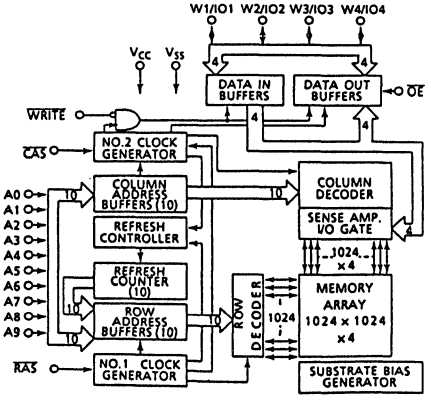
PIN NAMES

A0~A9	Address Inputs	$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe	I/O1~I/O4	Data Input/Output
$\overline{CS}$	Chip Select	V_{CC}	Power (+5V)
$\overline{WRITE}$	Read/Write Input	V_{SS}	Ground

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514402AP/AJ/ASJ/AZ-70	–	100	mA	3, 4 5
		TC514402AP/AJ/ASJ/AZ-80	–	85		
		TC514402AP/AJ/ASJ/AZ-10	–	75		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514402AP/AJ/ASJ/AZ-70	–	100	mA	3, 5
		TC514402AP/AJ/ASJ/AZ-80	–	85		
		TC514402AP/AJ/ASJ/AZ-10	–	75		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, STATIC COLUMN Mode ($\overline{RAS}$ = $\overline{CS}$ = V_{IL}, Address Cycling: t_{SC} = t_{SC} MIN.)	TC514402AP/AJ/ASJ/AZ-70	–	85	mA	3, 4 5
		TC514402AP/AJ/ASJ/AZ-80	–	75		
		TC514402AP/AJ/ASJ/AZ-10	–	70		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514402AP/AJ/ASJ/AZ-70	–	100	mA	3, 5
		TC514402AP/AJ/ASJ/AZ-80	–	85		
		TC514402AP/AJ/ASJ/AZ-10	–	75		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514402AP/ AJ/ASJ/AZ-70		TC514402AP/ AJ/ASJ/AZ-80		TC514402AP/ AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	–	205	–	245	–	ns	
t_{SC}	Static Column Mode Cycle Time	40	–	45	–	55	–	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	100	–	110	–	135	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	9,14 15
t_{CAC}	Access Time from $\overline{CS}$	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	9,15
t_{ALW}	Access Time from Last Write	–	65	–	75	–	95	ns	9,16
t_{CLZ}	$\overline{CS}$ to output in Low-Z	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Addres	5	–	5	–	5	–	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	–	20	–	20	–	30	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	70	200,000	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	200,000	20	200,000	25	200,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$ (READ CYCLE)	85	–	95	–	115	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	–	5	–	10	–	ns	17

SYMBOL	PARAMETER	TC514402AP/ AJ/ASJ/AZ-70		TC514402AP/ AJ/ASJ/AZ-80		TC514402AP/ AJ/ASJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{LWAD}	Last Write to Column Address Delay Time	20	30	20	35	25	45	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	65	–	75	–	95	–	ns	
t_{RCS}	Read Command Set-up Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time (Output Data Disable)	15	–	15	–	20	–	ns	13
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{WI}	Write Command Inactive Time	10	–	10	–	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data-In Hold Time	15	–	15	–	20	–	ns	12
t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time (Output Data Disable)	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	50	–	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE Cycle)	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	–	70	–	85	–	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time($\overline{CS}$ before $\overline{RAS}$)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time($\overline{CS}$ before $\overline{RAS}$)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	25	–	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	25	–	ns	

SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-70		TC514402AP/AJ/ASJ/AZ-80		TC514402AP/AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WTS}	Write Command Set-Up Time	10	–	10	–	10	–	ns	
t_{WTH}	Write Command Hold Time	10	–	10	–	10	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{WRH}	WRITE to RAS Hold Time	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-70		TC514402AP/AJ/ASJ/AZ-80		TC514402AP/AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	155	–	185	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	190	–	210	–	250	–	ns	
t_{SC}	Static Column Mode Cycle Time	45	–	50	–	60	–	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	105	–	115	–	140	–	ns	
t_{RAC}	Access Time from $\overline{CS}$	–	75	–	85	–	105	ns	9,14 15
t_{CAC}	Access Time from $\overline{CS}$	–	25	–	25	–	30	ns	9,14
t_{AA}	Access Time from Column Address	–	40	–	45	–	50	ns	9,15
t_{ALW}	Access Time from Last Write	–	70	–	80	–	100	ns	9,16
t_{RAS}	$\overline{RAS}$ Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	75	200,000	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CS}$ Hold Time	75	–	85	–	105	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	200,000	25	200,000	30	200,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	45	–	55	–	ns	
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time	60	–	60	–	70	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Dalay Time	105	–	115	–	140	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	70	–	75	–	90	–	ns	13
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	–	25	–	30	–	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	30	–	ns	

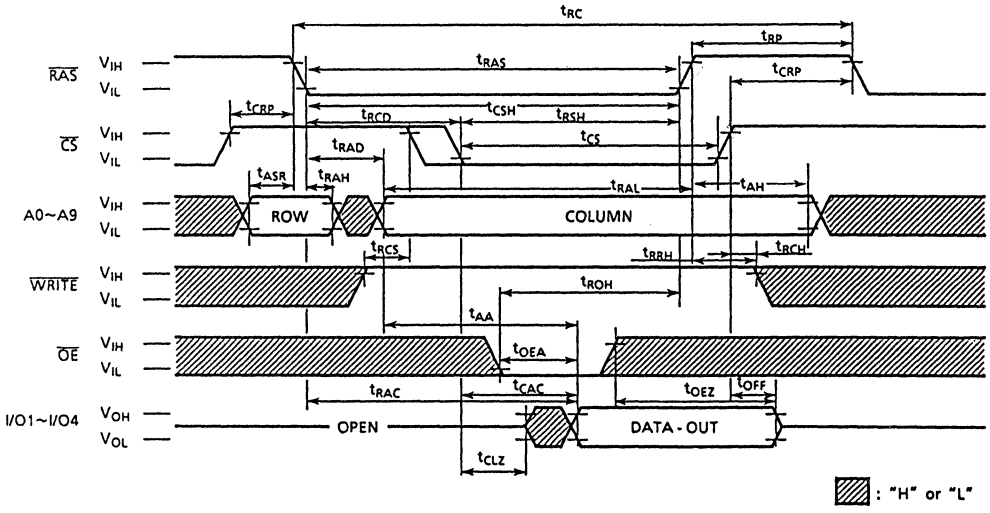
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	–	7	pF

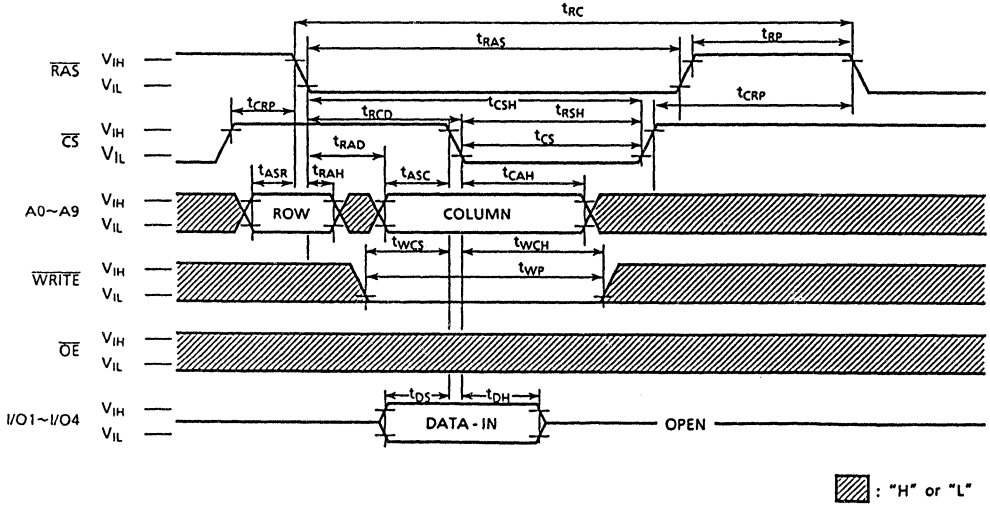
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.) the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
16. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met.
    t_{LWAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled by t_{AA}.
17. t_{AH} is the condition to latch column address ewhen $\overline{RAS}$ has rised up.

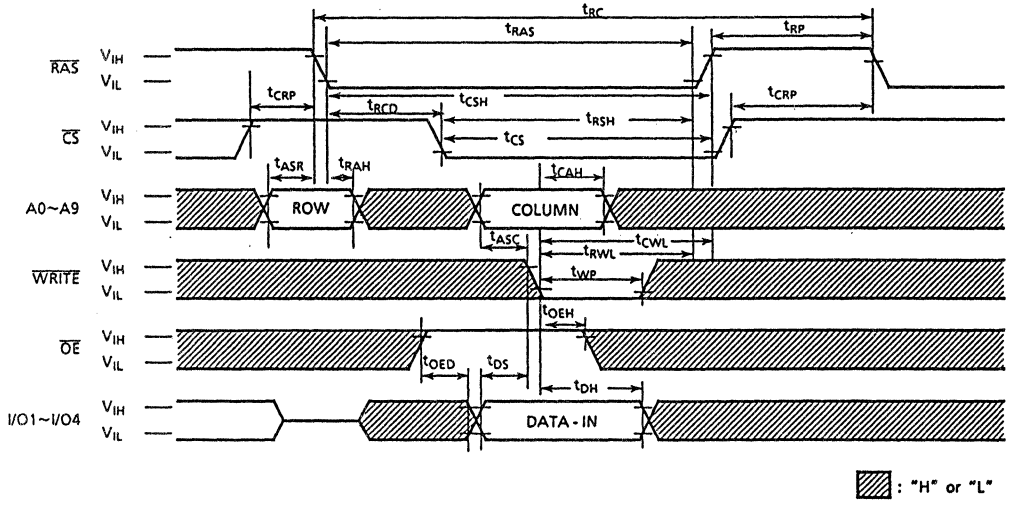
READ CYCLE



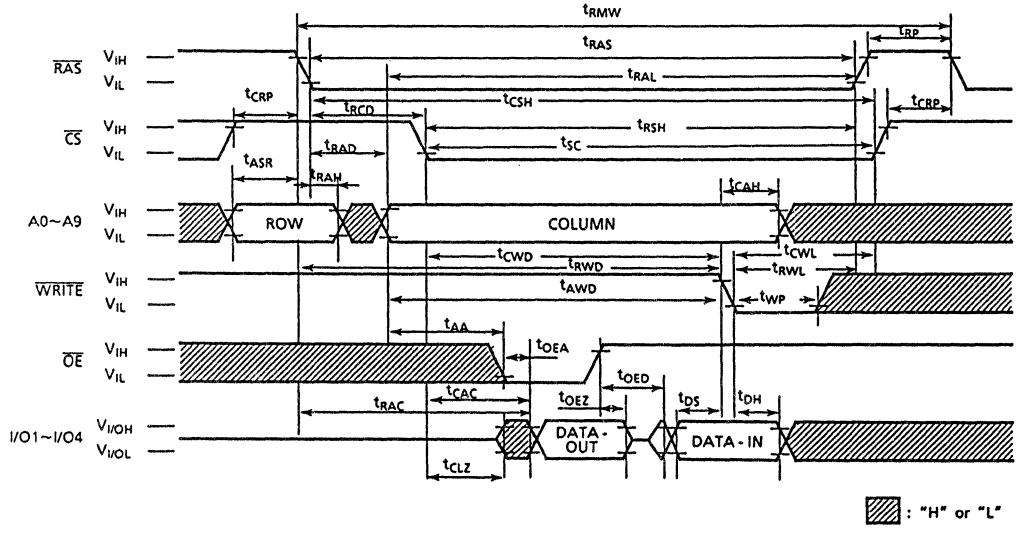
WRITE CYCLE (EARLY WRITE)



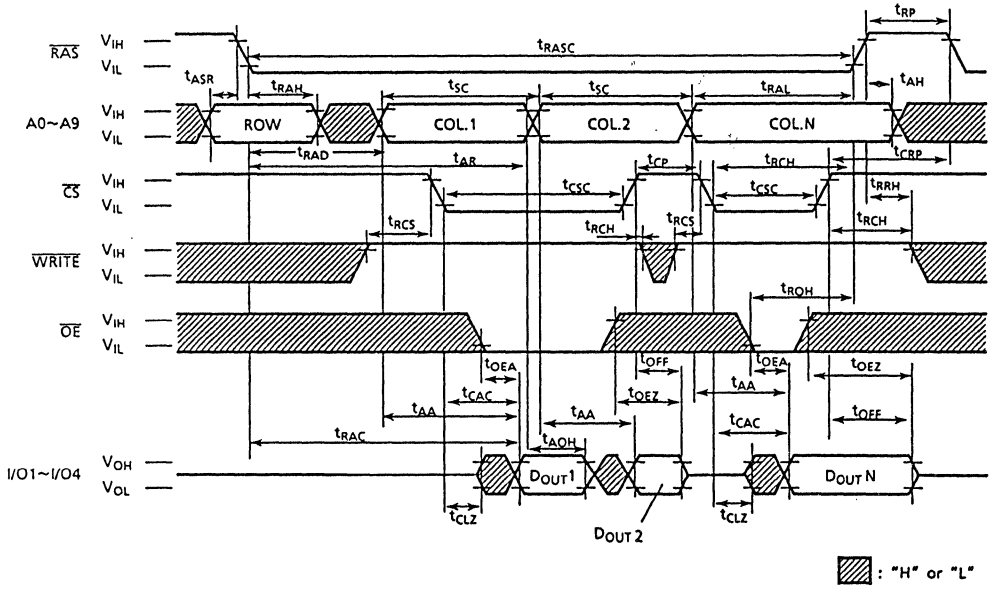
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



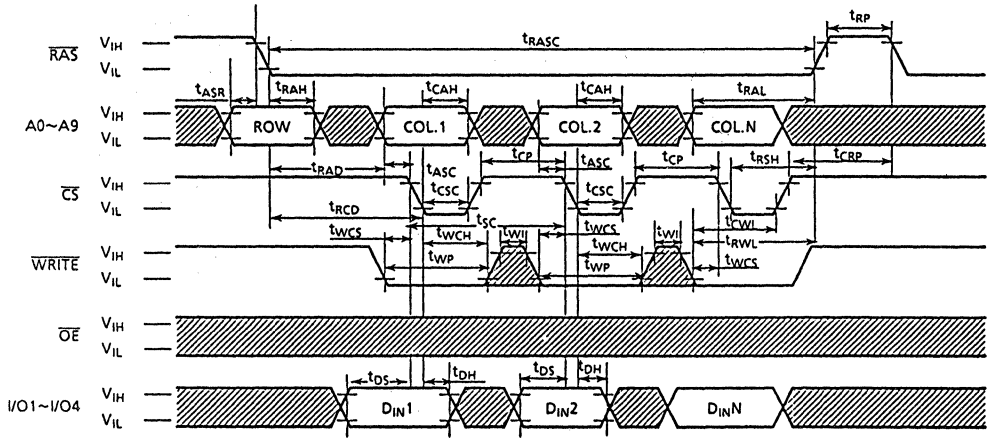
READ - MODIFY - WRITE CYCLE



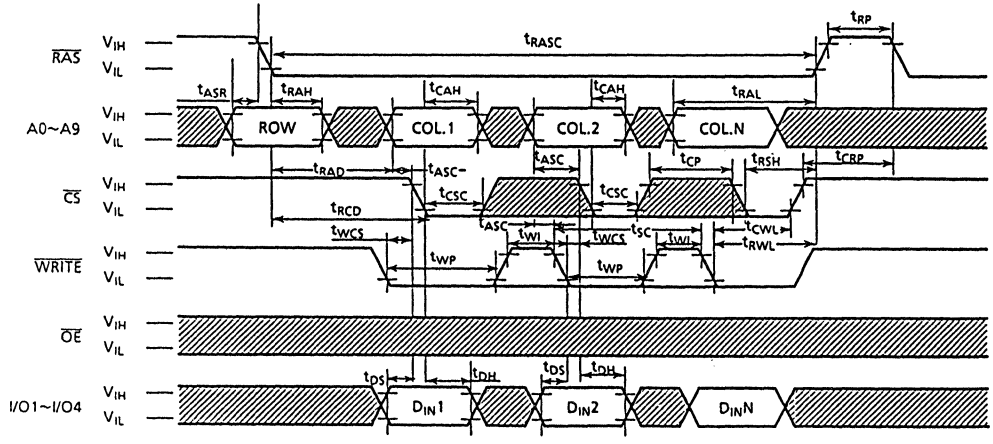
STATIC COLUMN MODE READ CYCLE



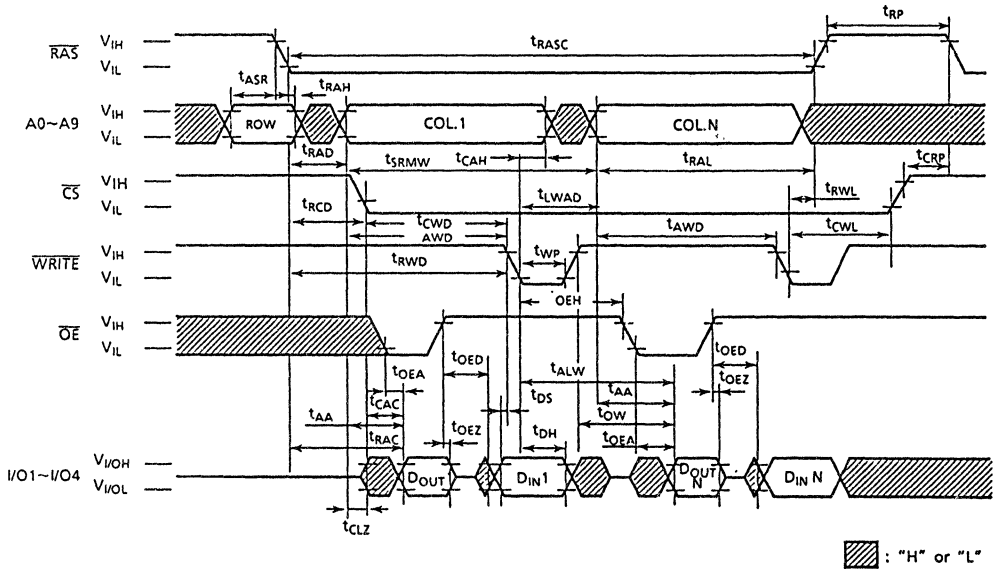
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



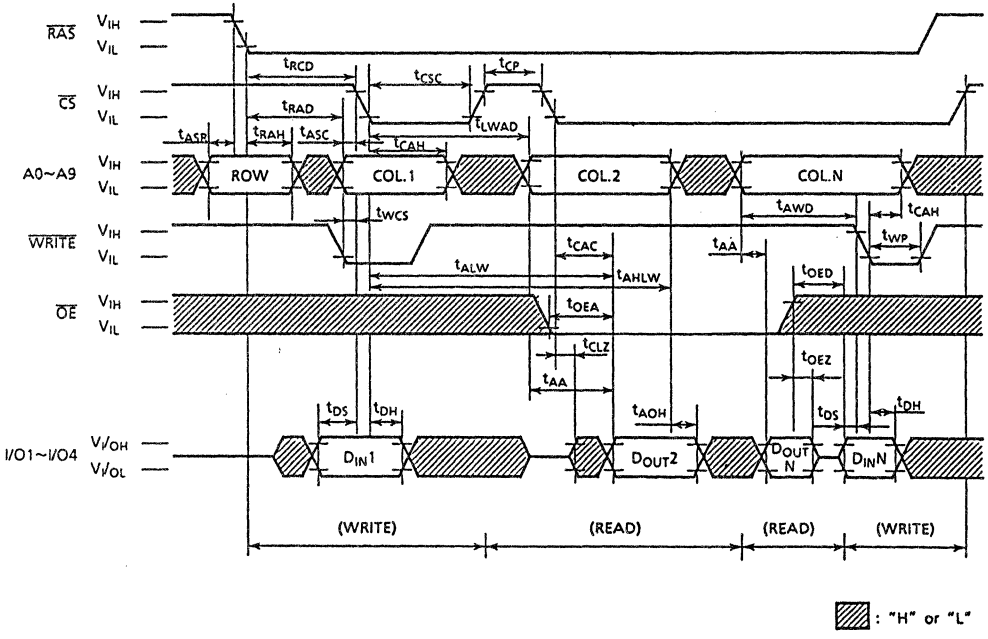
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



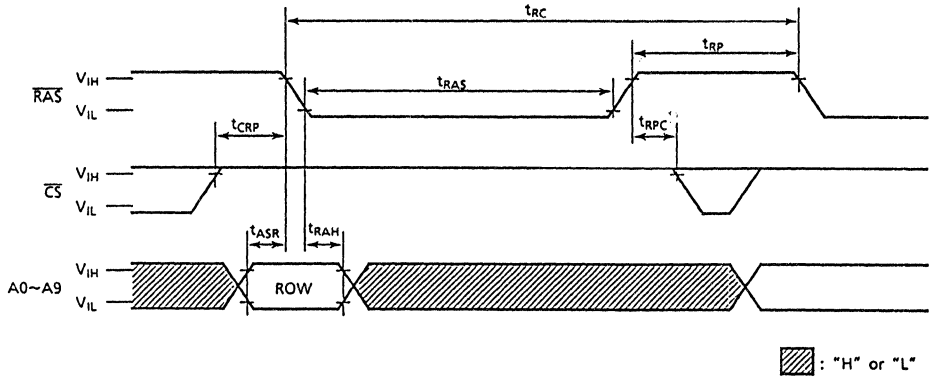
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

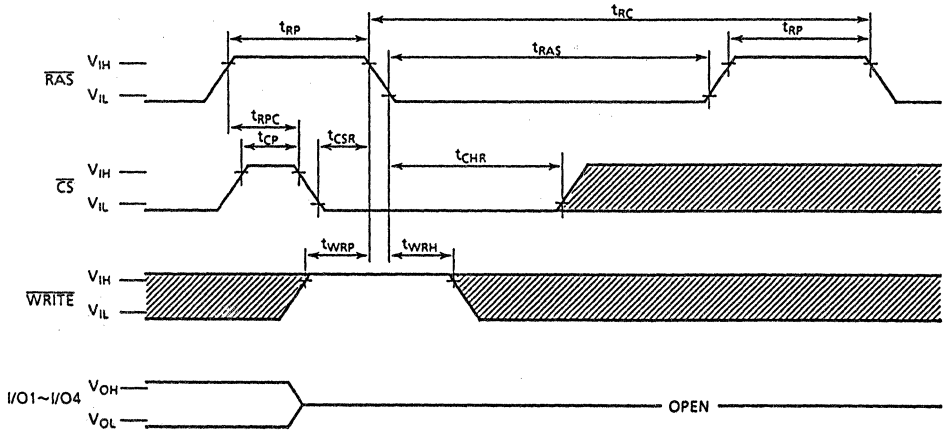


$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

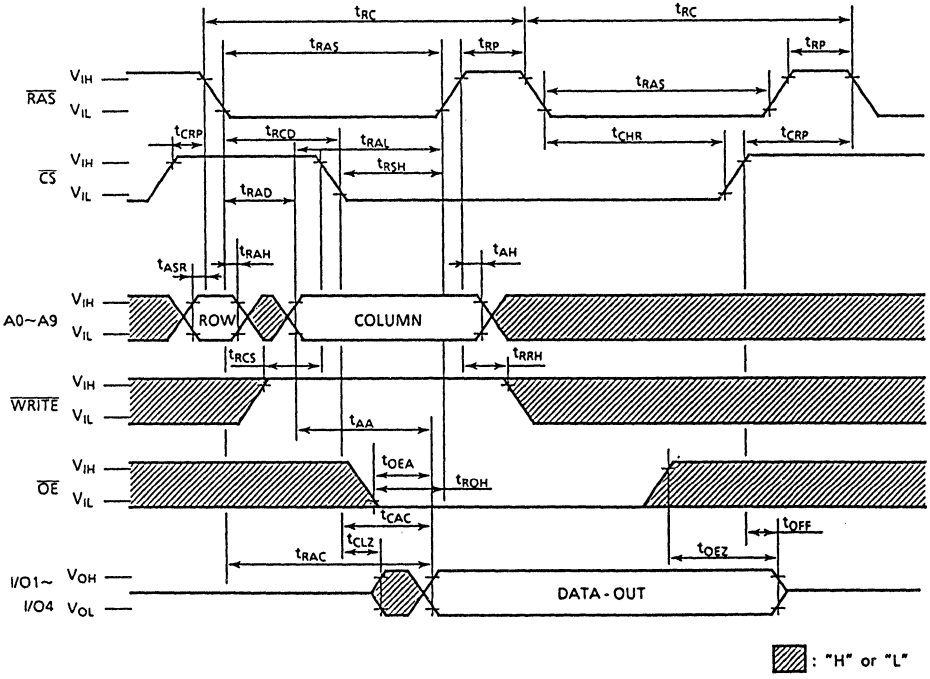
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



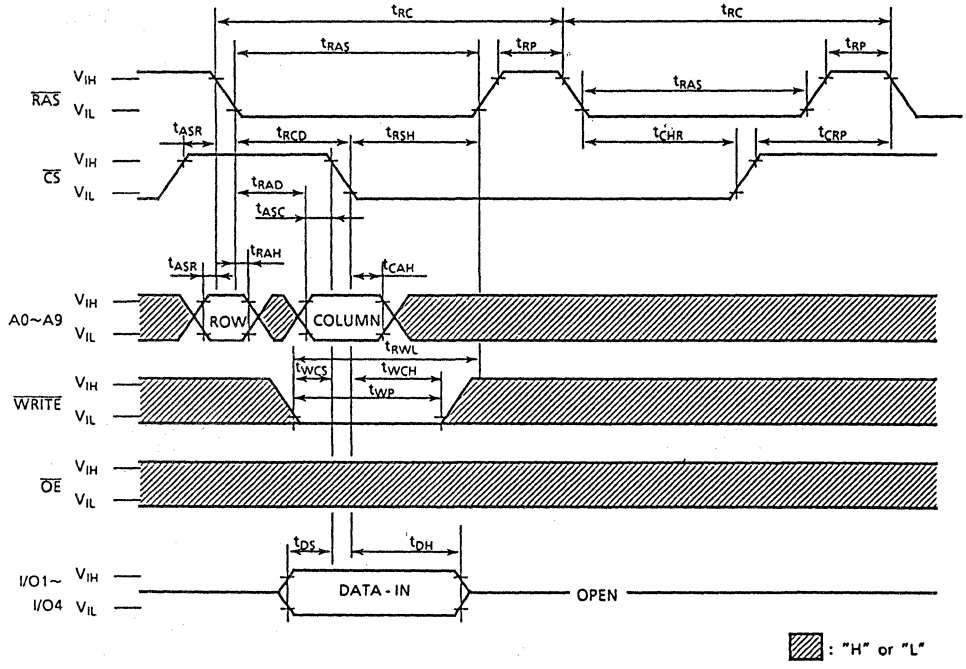
Note: $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

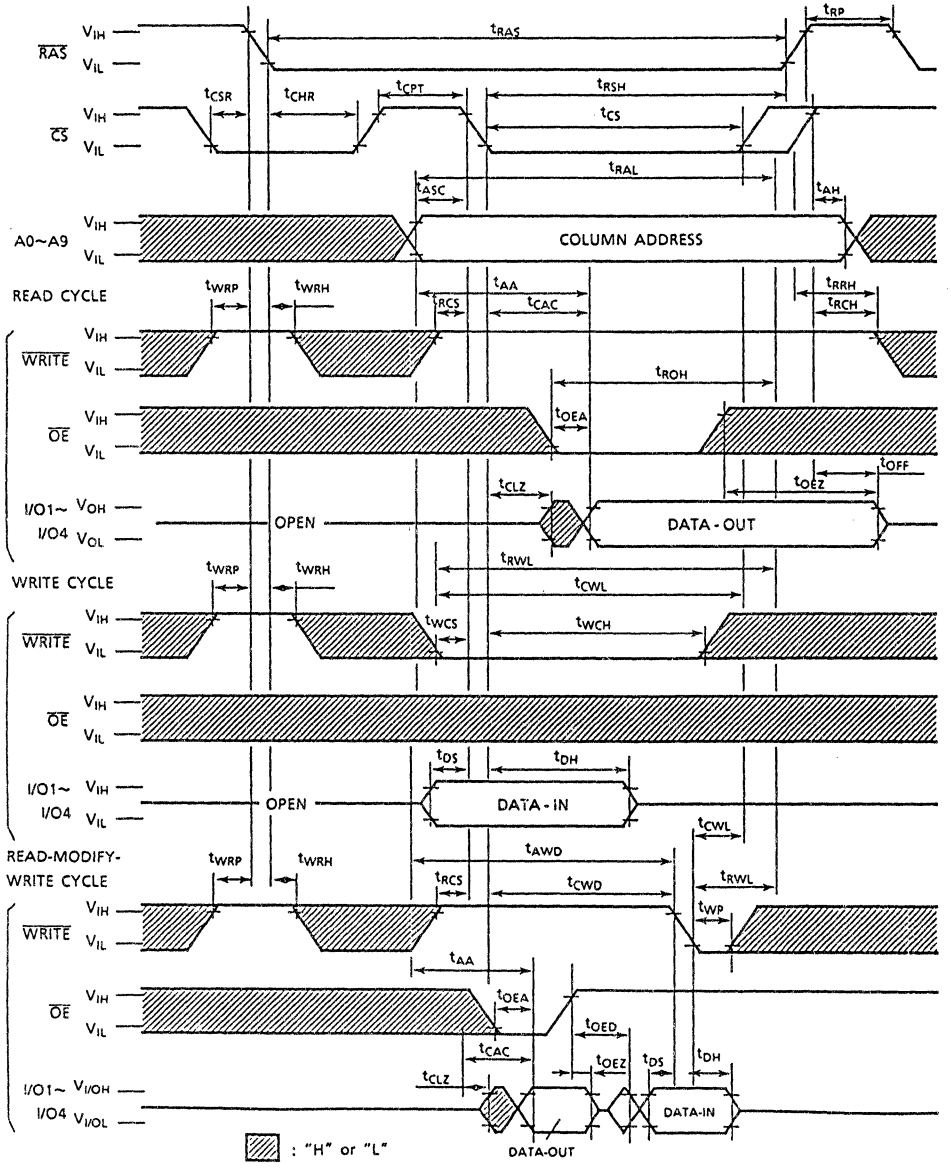
HIDDEN REFRESH CYCLE (READ)



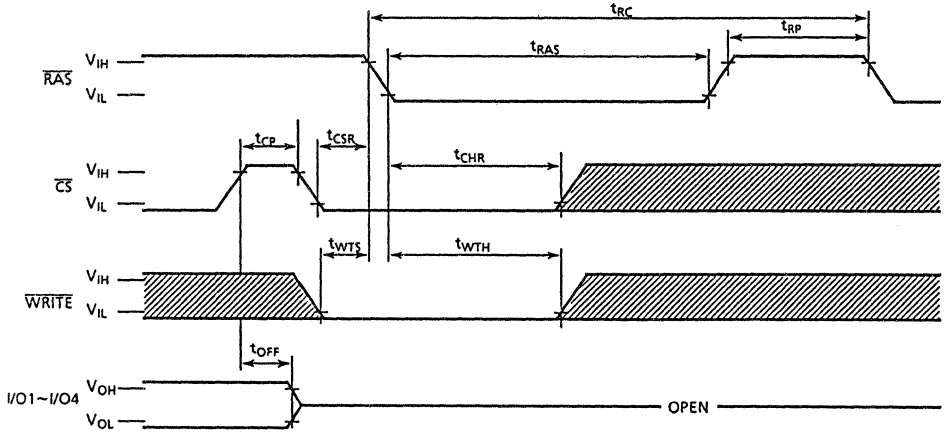
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC514402AP/AJ/ASJ/AZ is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A0C is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514402AP/AJ/ASJ/AZ. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle "or "$\overline{\text{RAS}}$ Only Refresh Cycle" put it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in cace of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

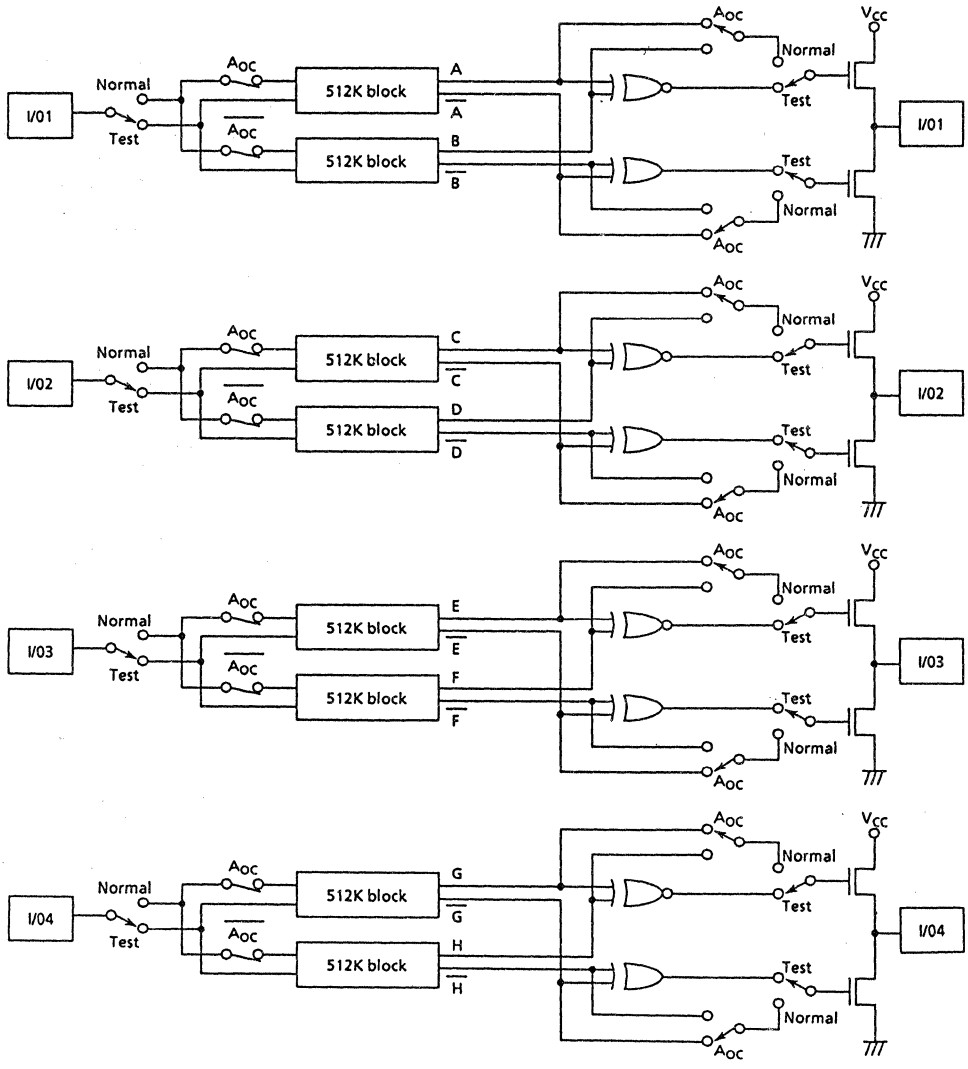


Fig. 1

* This is advanced information and specifications are subject to change without notice.

1,048,576 WORD x 4 BIT DYNAMIC RAM

DESCRIPTION

The TC514410J/Z is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514410J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514410J/Z to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

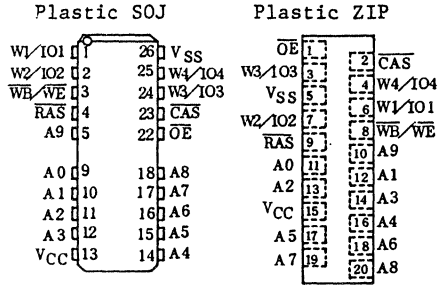
FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

		TC514410J/Z-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  578mW MAX. Operating (TC514410J/Z-80)
  495mW MAX. Operating (TC514410J/Z-10)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write Per Bit and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package Plastic SOJ: TC514410J
  Plastic ZIP: TC514410Z

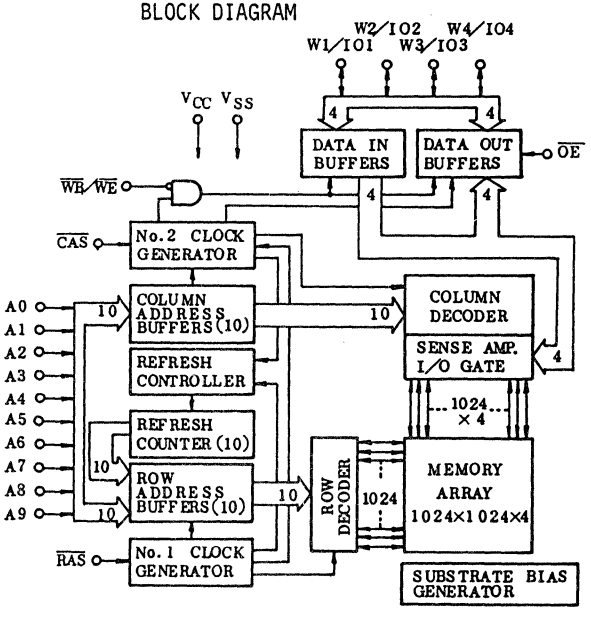
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{WE}$	Write Per Bit/Read/ Write Input
$\overline{OE}$	Output Enable
W1/IO1 ∿ W4/IO4	Write Selection/ Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514410J/Z-80	-	105	mA	3,4,5
		TC514410J/Z-10	-	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514410J/Z-80	-	105	mA	3,5
		TC514410J/Z-10	-	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC514410J/Z-80	-	75	mA	3,4,5
		TC514410J/Z-10	-	65		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514410J/Z-80	-	105	mA	3
		TC514410J/Z-10	-	90		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≦V_{IN}≦6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V≦V_{OUT}≦5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (L_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514410J/Z -80		TC514410J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	205	-	245	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	60	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	105	-	125	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	40	-	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	55	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	-	55	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514410J/Z -80		TC514410J/Z -10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	20	-	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	-	60	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	110	-	135	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time (Fast Page Mode)	75	-	90	-	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	70	-	85	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	25	-	ns	
t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	25	-	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	-	0	-	ns	
t_{WBH}	Write Per Bit Hold Time	10	-	10	-	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	-	0	-	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	-	10	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 6,7,8)

SYMBOL	PARAMETER	TC514410J/Z -80		TC514410J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	155	-	185	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	105	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	30	ns	9,14
t_{AA}	Access Time from Column Address	-	45	-	55	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	60	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	105	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	50		60		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (W1/I01~W4/I04)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Column Address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.

6. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume $t_T=5$ ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100 pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

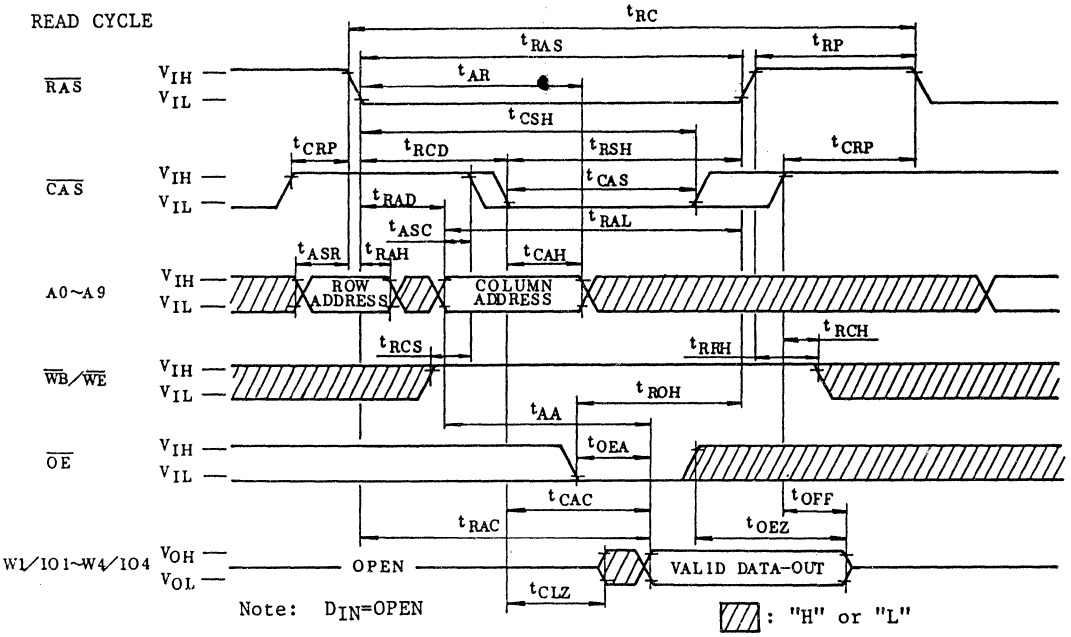
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to ($\overline{WB}$/) $\overline{WE}$ leading edge in read-modify-write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only, If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWD} \geq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

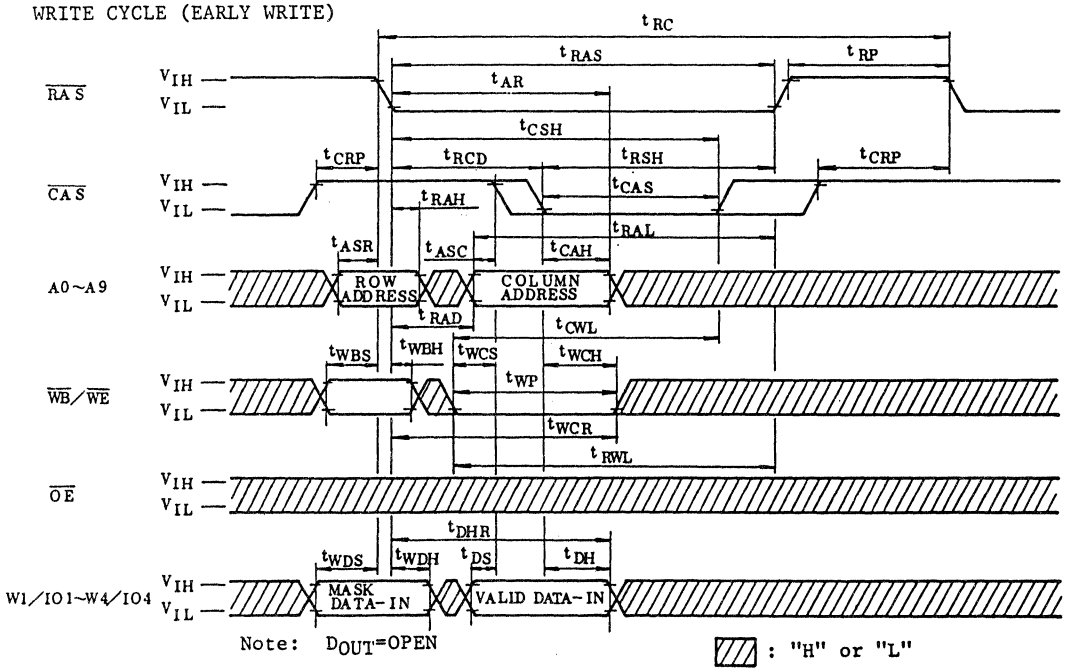
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

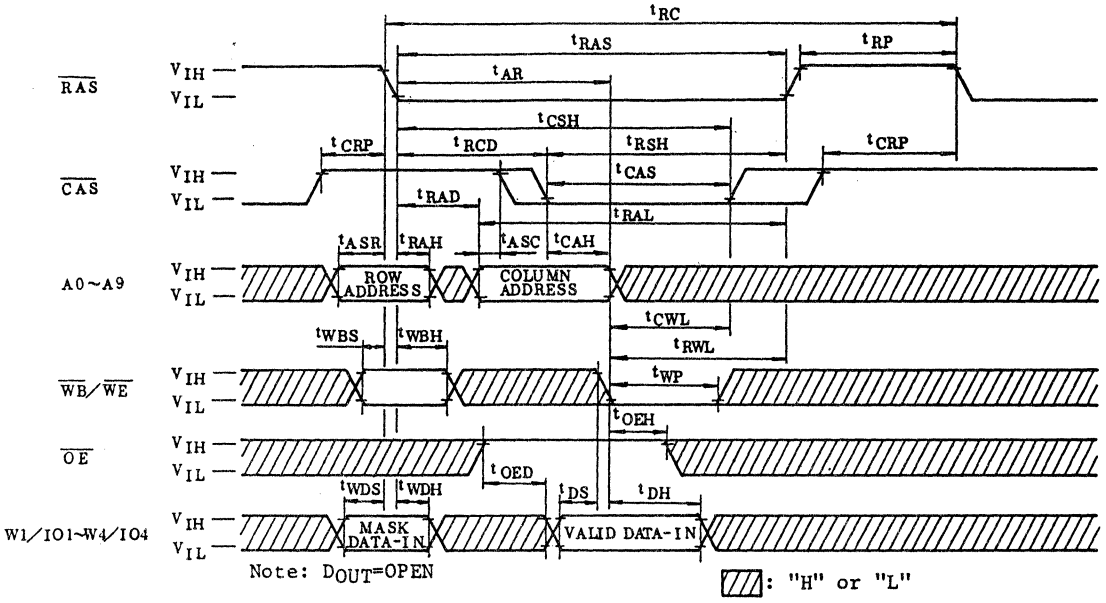
READ CYCLE



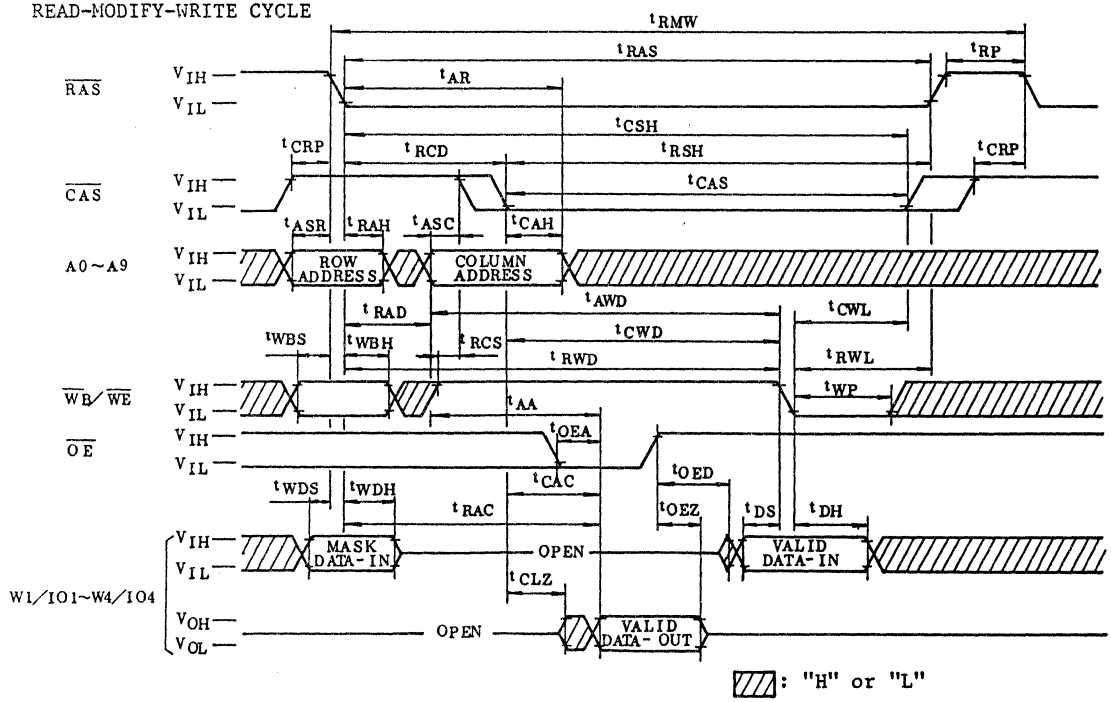
WRITE CYCLE (EARLY WRITE)



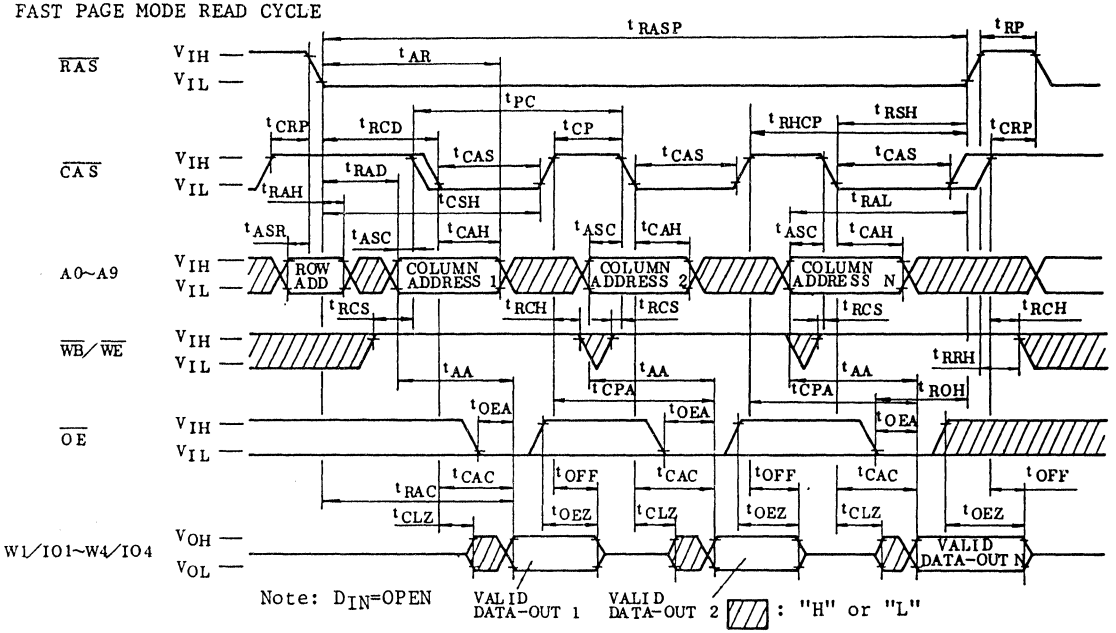
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



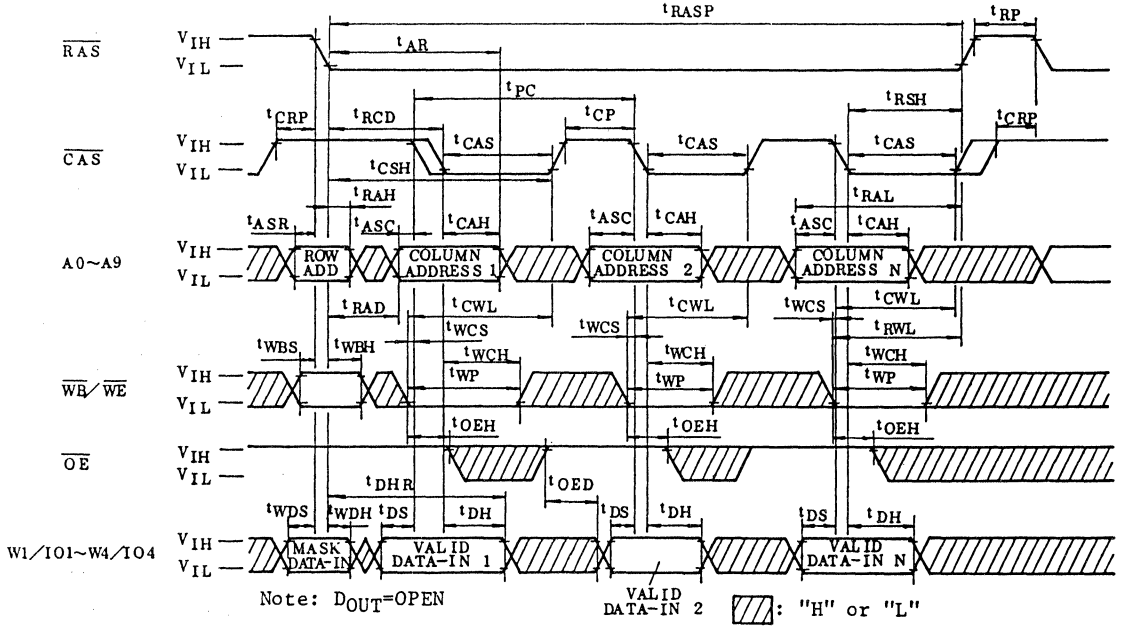
READ-MODIFY-WRITE CYCLE



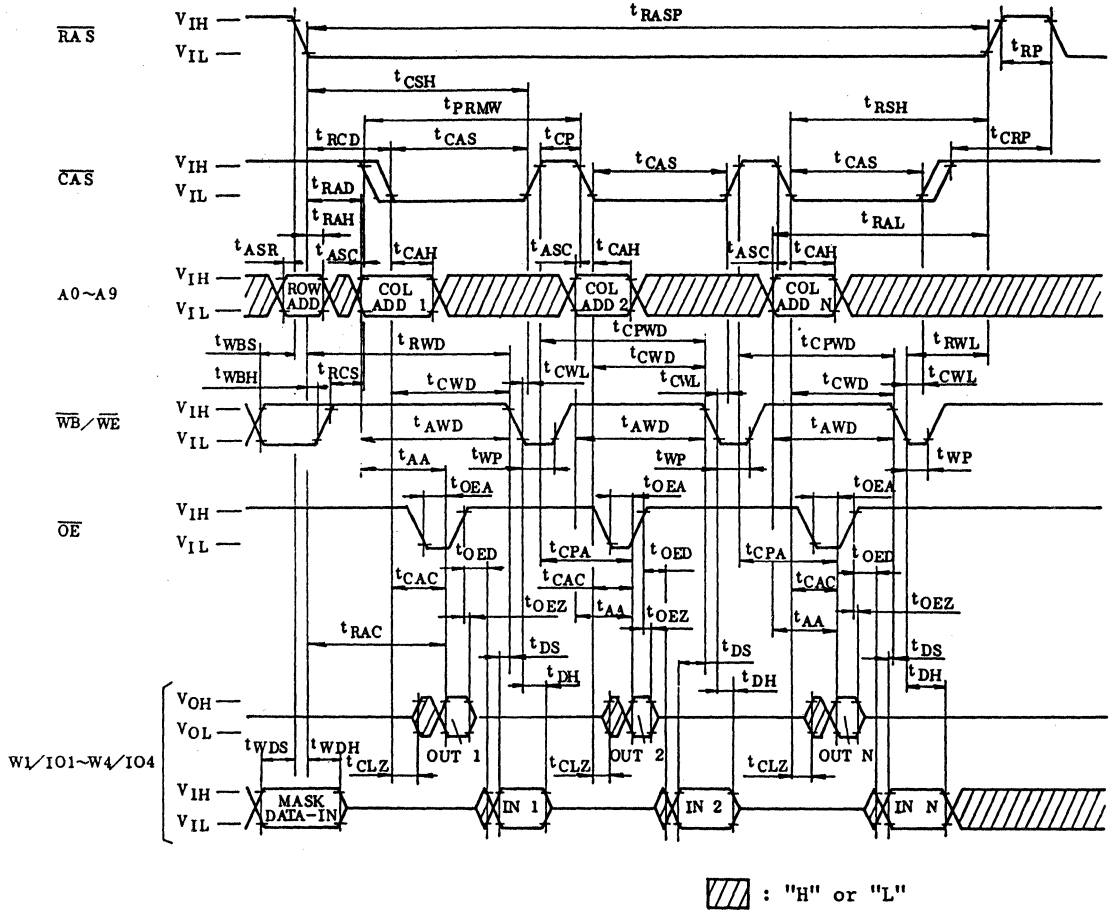
FAST PAGE MODE READ CYCLE



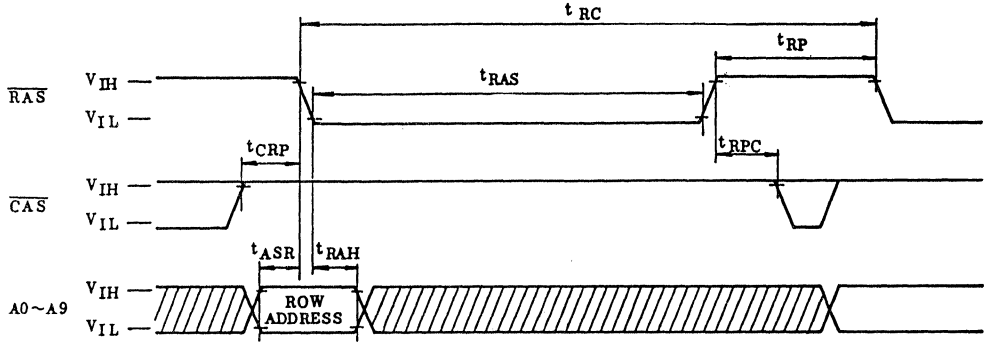
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



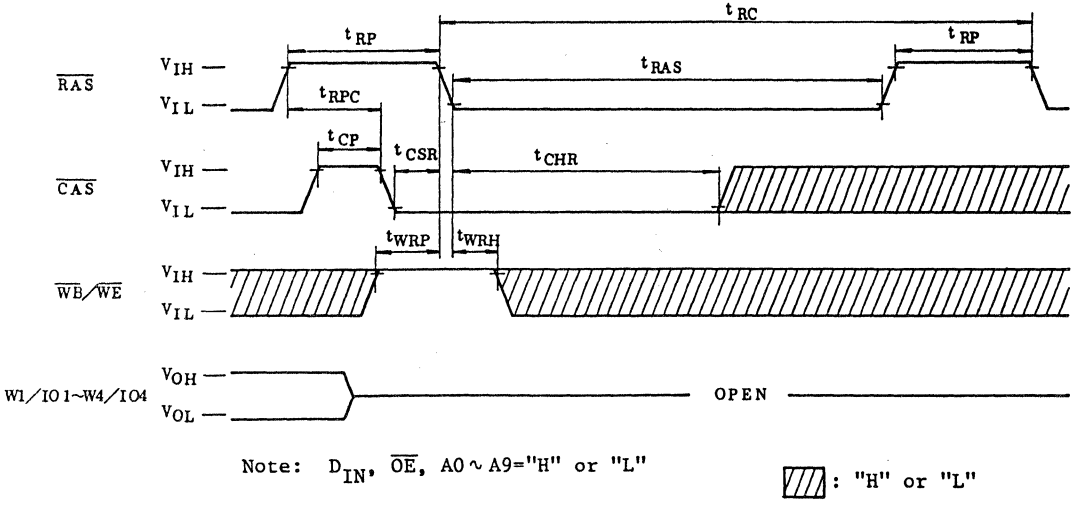
$\overline{RAS}$ ONLY REFRESH CYLCE



Note: $\overline{WB}/\overline{WE}$, $\overline{OE}$="H" or "L"

▨: "H" or "L"

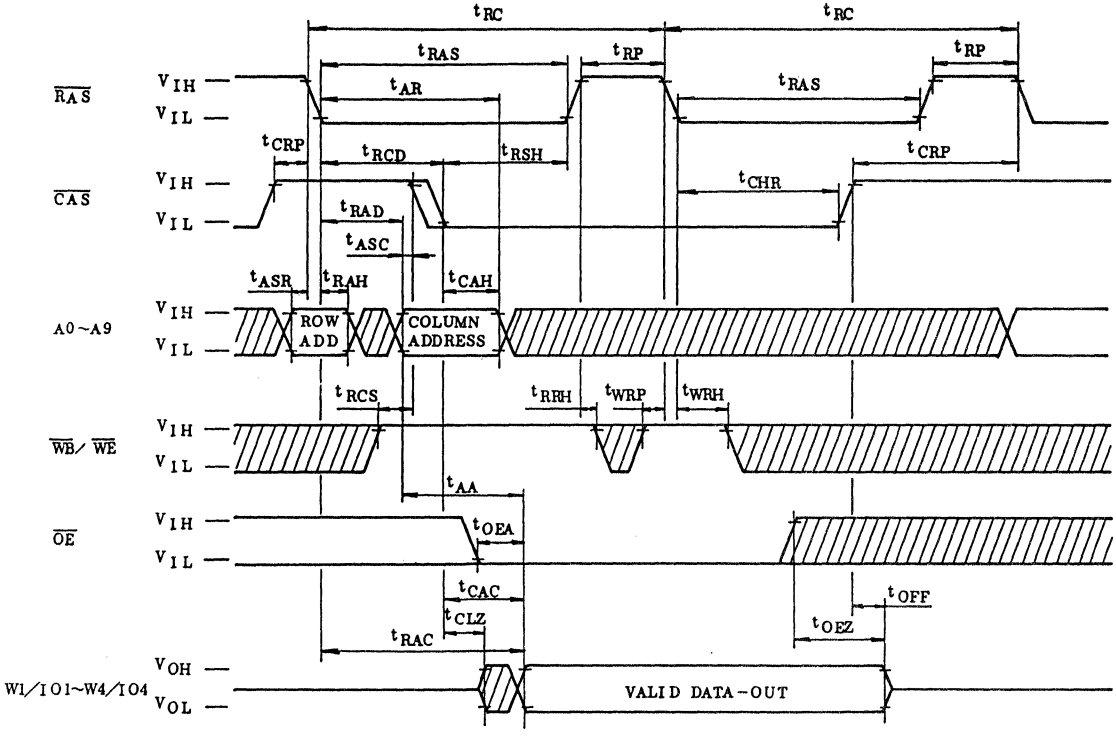
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0 ∿ A9="H" or "L"

▨: "H" or "L"

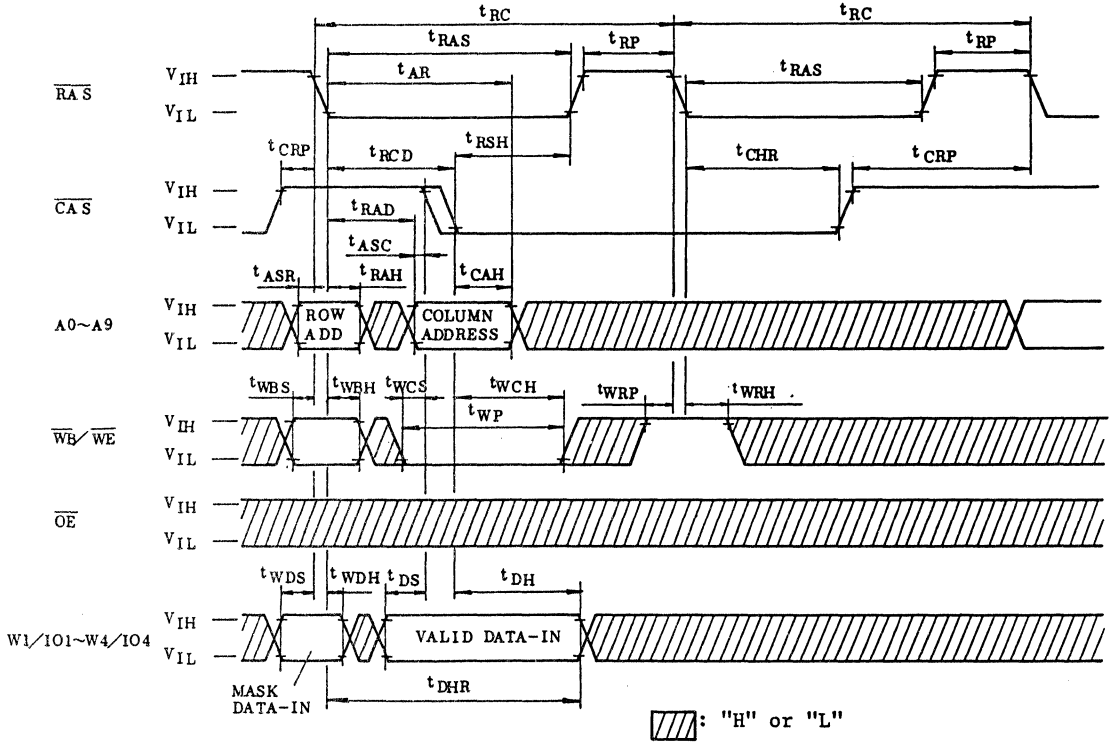
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN}=OPEN

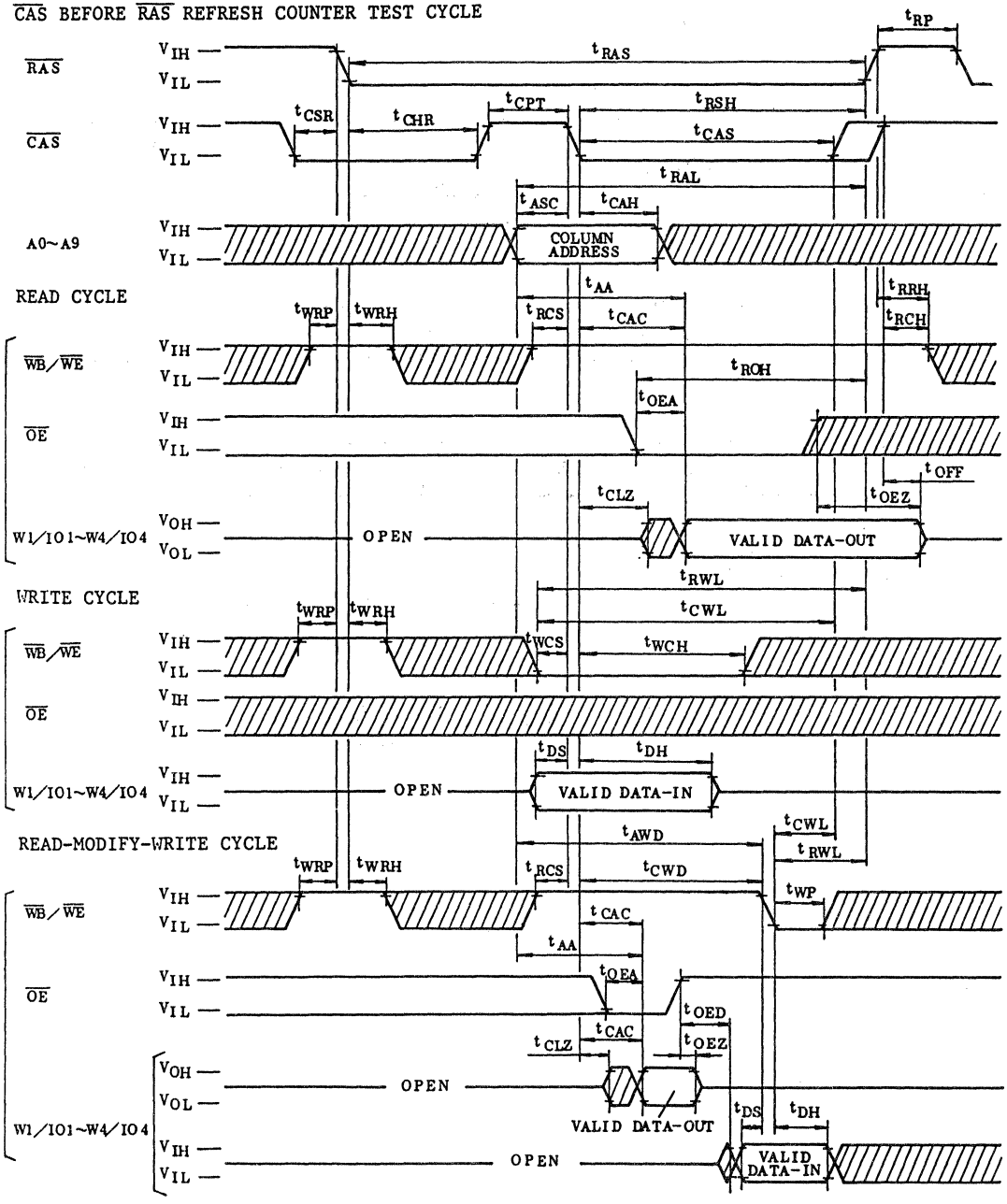
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (WRITE)

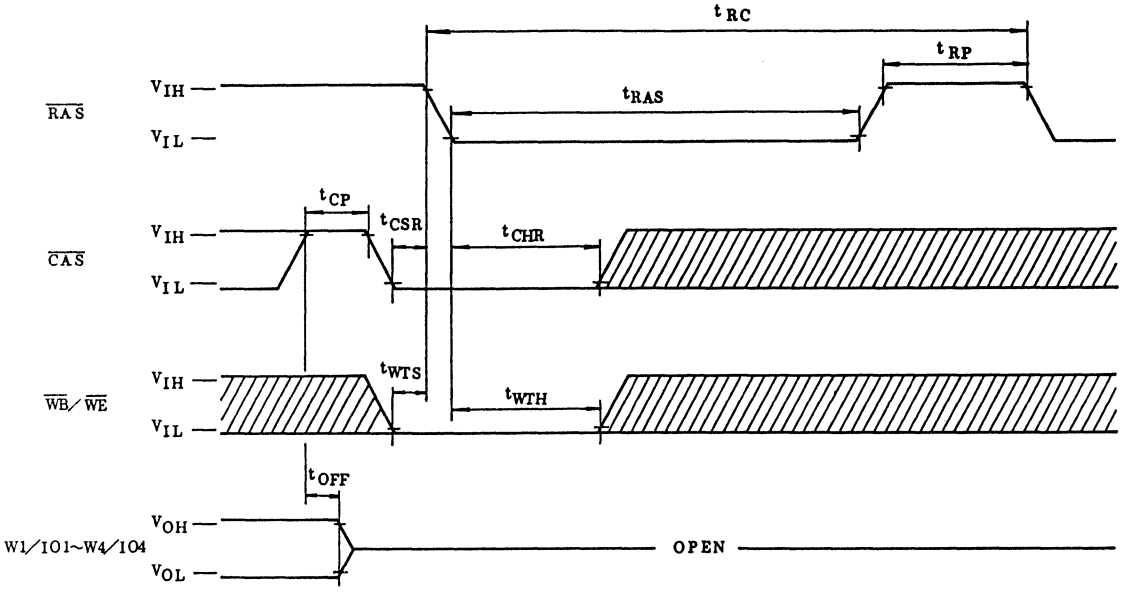


Note: D_{OUT}=OPEN

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

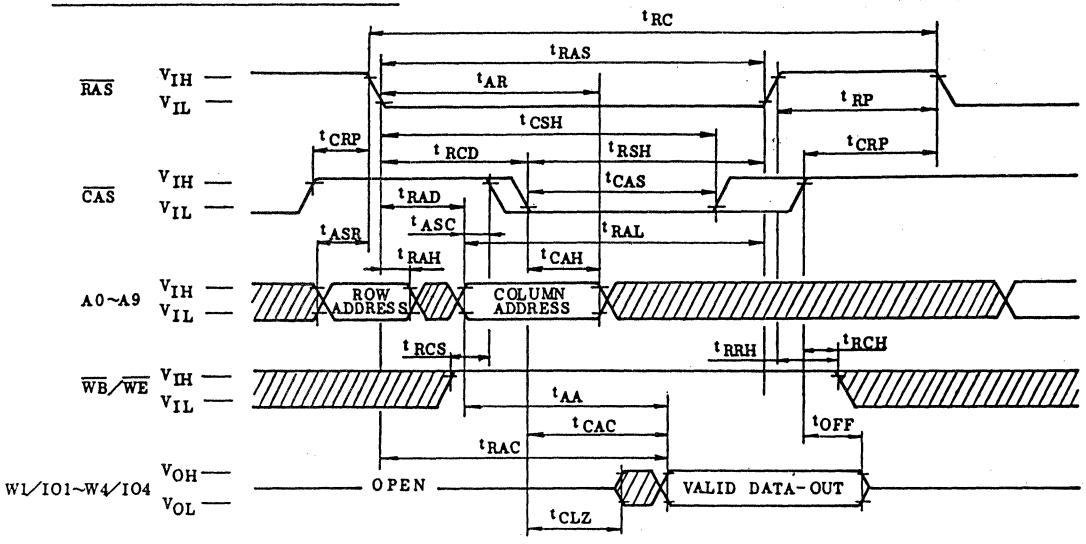


$\overline{WE}$, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



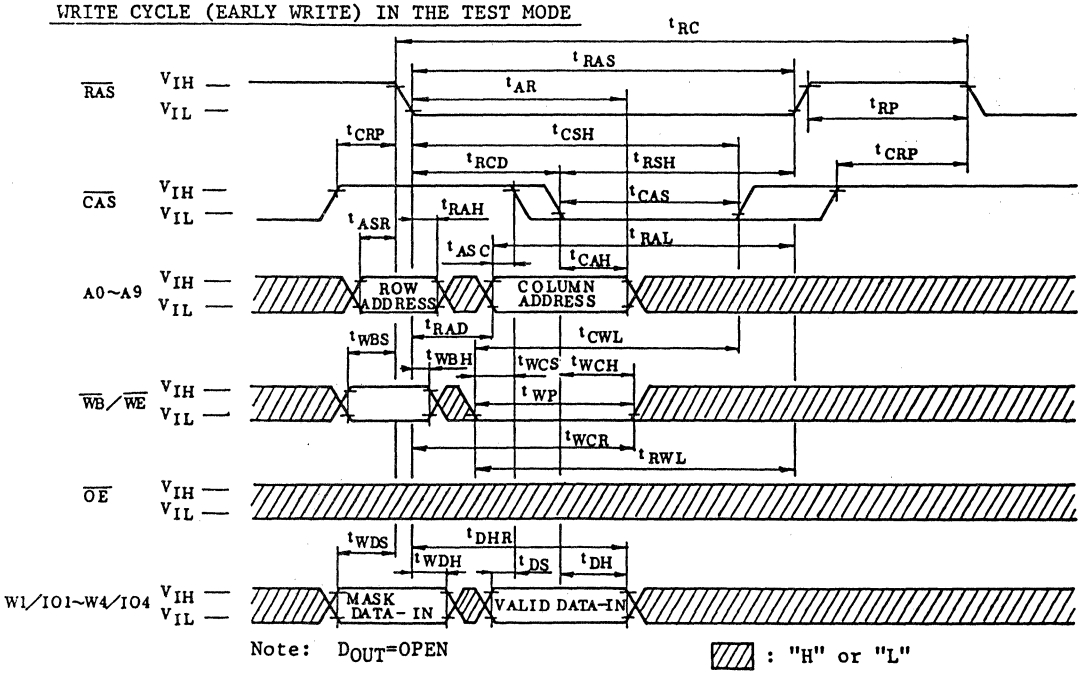
Note: D_{IN}, $\overline{OE}$, A0 ~ A9 = "H" or "L" ▨ : "H" or "L"

READ CYCLE IN THE TEST MODE



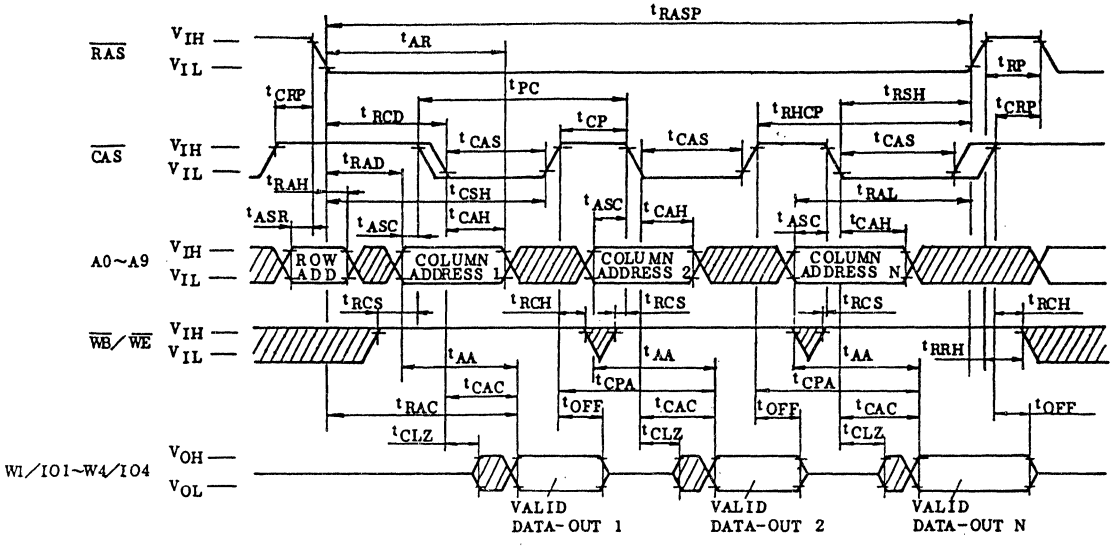
Note: D_{IN}=OPEN, $\overline{OE}$="L" ▨: "H" or "L"

WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



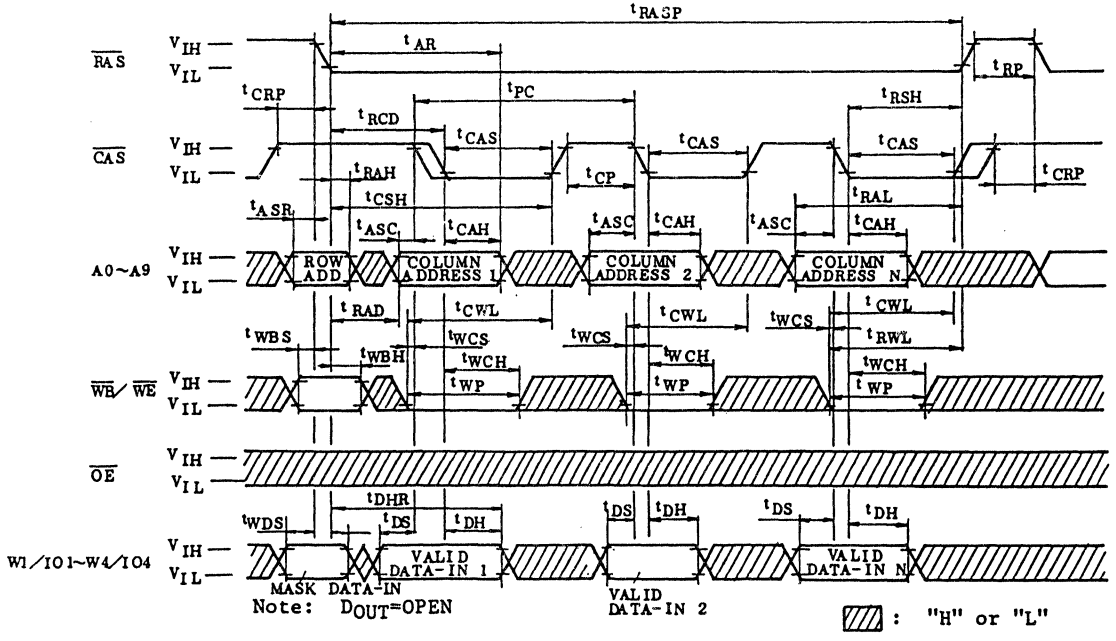
Note: D_{OUT}=OPEN ▨ : "H" or "L"

FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note: D_{IN}=OPEN, OE="L" ▨ : "H" or "L"

FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



Note: D_{OUT}=OPEN

▨ : "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC514410J/Z are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hole Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes data on (Wi)IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi(/IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition.
For those data bits of Wi(/IOi) that are kept low as $\overline{RAS}$ falls the write operation is inhibited on the chip. If $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the output. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 1024 row addresses (A0~A9) within each 16 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

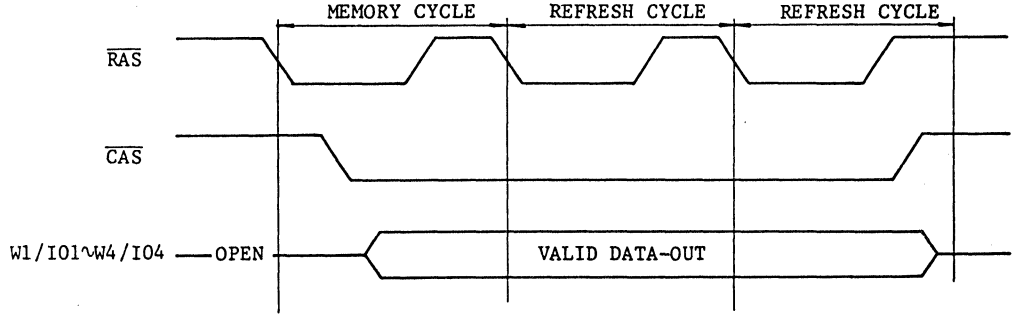
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514410J/Z offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC514410J/Z allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514410J/Z is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514410J/Z can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 1024 times.

③ Check "1" out of 1024 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 1024 times.

⑤ Check "0" out of 1024 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

TEST MODE

The TC514410J/Z is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{0C} is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514410J/Z. In "Test Mode", the 1M × 4 DRAM can be tested as if it were a 512K × 4 DRAM.

"$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

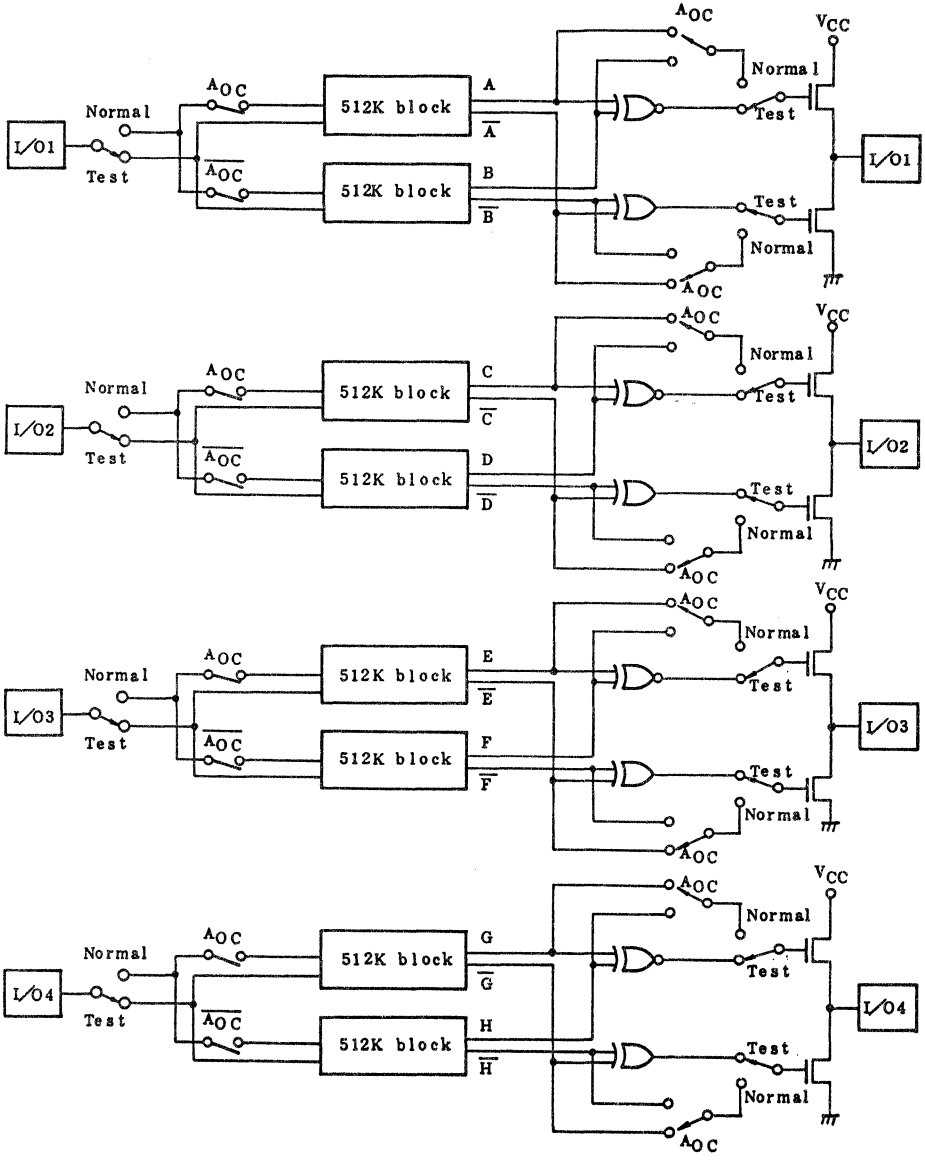


Fig. 1

1,048,576 WORD × 4 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514410AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514410AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514410AP/AJ/ASJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300 / 350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performace logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

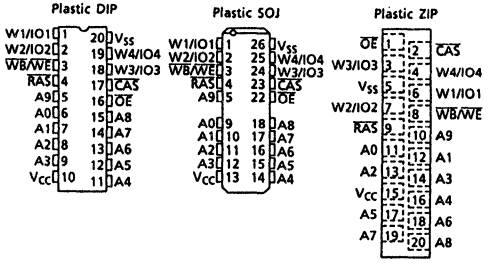
	TC514410AP/AJ/ASJ/AZ-60
t_{RAC} $\overline{RAS}$ Access Time	60ns
t_{AA} Column Address Access Time	30ns
t_{CAC} $\overline{CAS}$ Access Time	20ns
t_{RC} Cycle Time	110ns
t_{PC} Fast Page Mode Cycle Time	45ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  660mW MAX. Operating
  (TC514410AP/AJ/ASJ/AZ-60)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write per Bit, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL Compatible
- 1024 refresh cycles/16ms
- Package
  TC514410AP : DIP20-P-300C
  TC514410AJ : SOJ26-P-350
  TC514410ASJ : SOJ26-P-300A
  TC514410AZ : ZIP20-P-400A

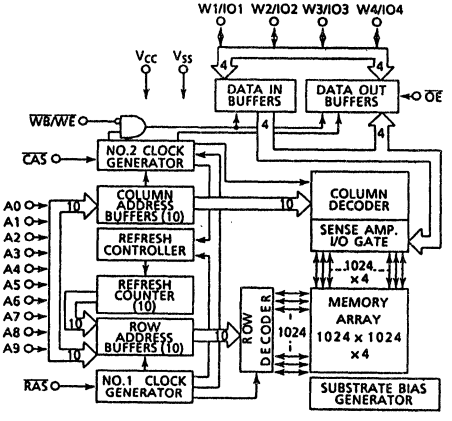
PIN NAMES

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/WE}$	Write Per Bit/Read/Write Input
$\overline{OE}$	Output Enable
W1/IO1~W4/IO4	Write Select/Date Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514410AP/AJ/ASJ/AZ-60	–	120	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514410AP/AJ/ASJ/AZ-60	–	120	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514410AP/AJ/ASJ/AZ-60	–	70	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514410AP/AJ/ASJ/AZ-60	–	120	mA	3, 5
$I_{I\ (L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test = 0V)		– 10	10	μA	
$I_{O\ (L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514410AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	20	ns	9,14
t_{AA}	Access Time from Column Address	–	30	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514410AP/AJ/ASJ/AZ-60		UNITS	NOTES
		MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	ns	
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	12
t_{DH}	Data Hold Time	15	–	ns	12
t_{REF}	Refresh Period	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	–	ns	
t_{WBH}	Write Per Bit Hold Time	10	–	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	–	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514410AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{WTS}	Write Command Set-up Time	10	-	ns	
t_{WTH}	Write Command Hold Width	10	-	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time	10	-	ns	
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514410AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	115	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	65	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	–	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	ns	

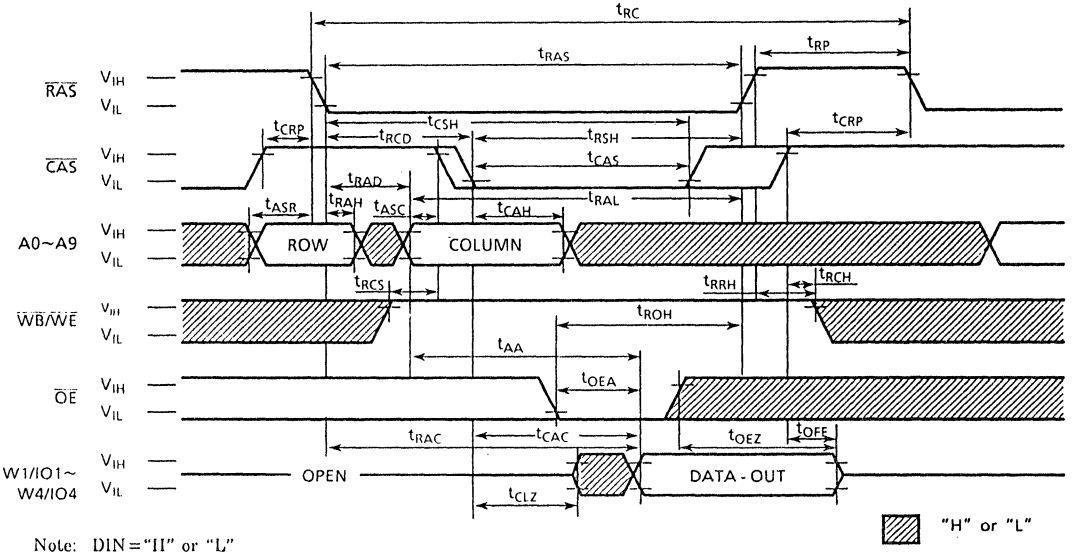
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (W1/IO1~W4/IO4)	–	7	pF

NOTES:

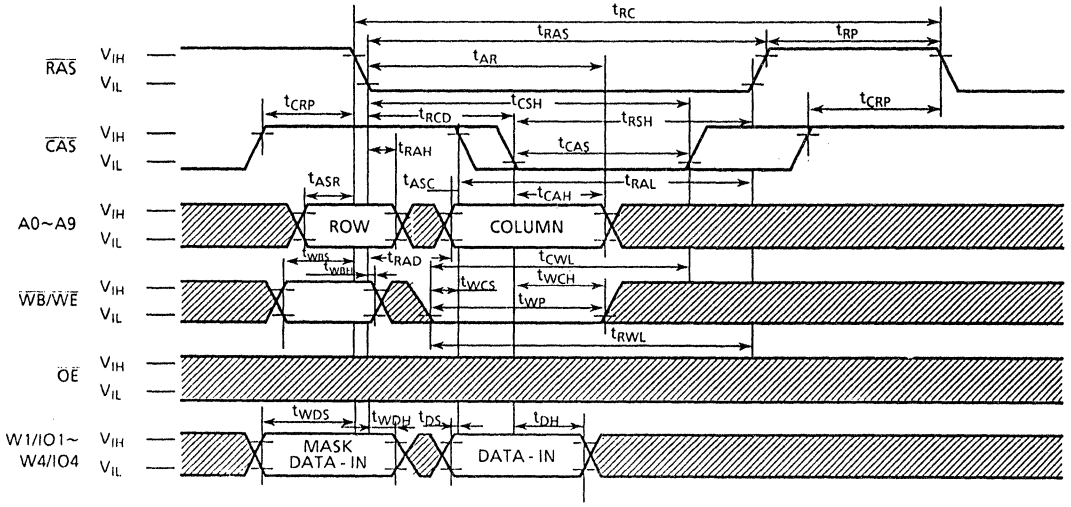
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE



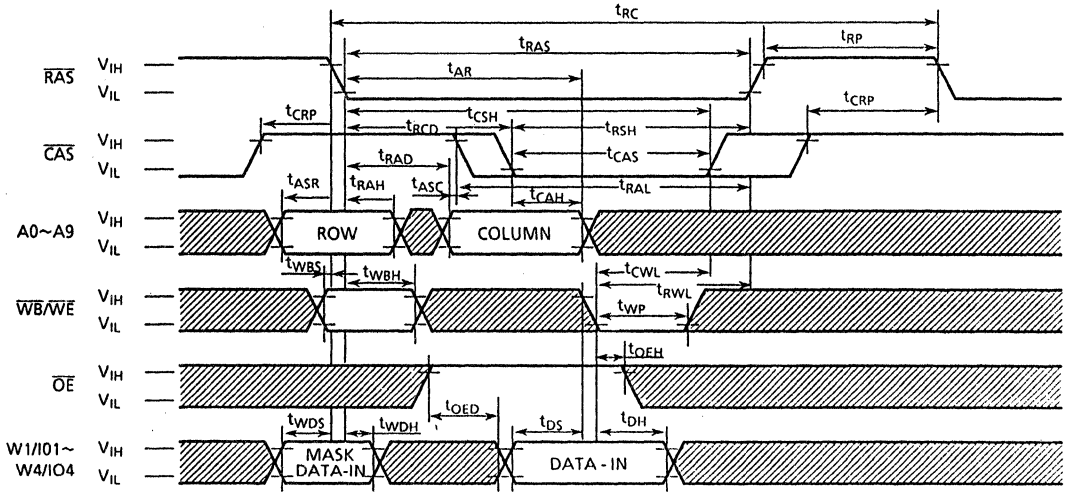
Note: DIN = "H" or "L"

WRITE CYCLE (EARLY WRITE)



Note: DOUT = OPEN

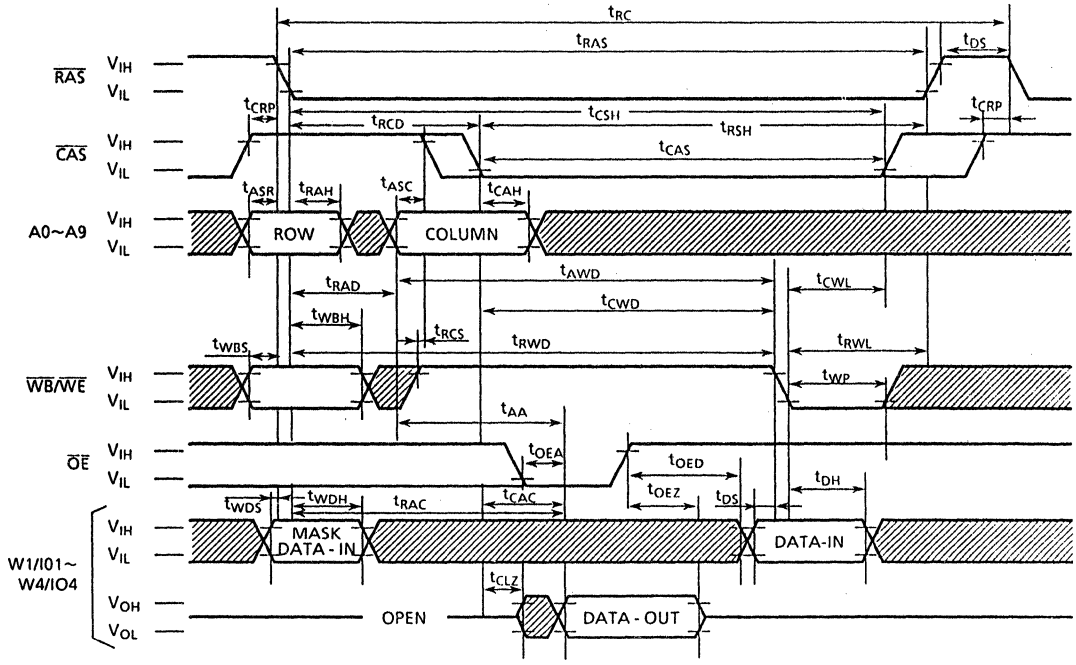
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



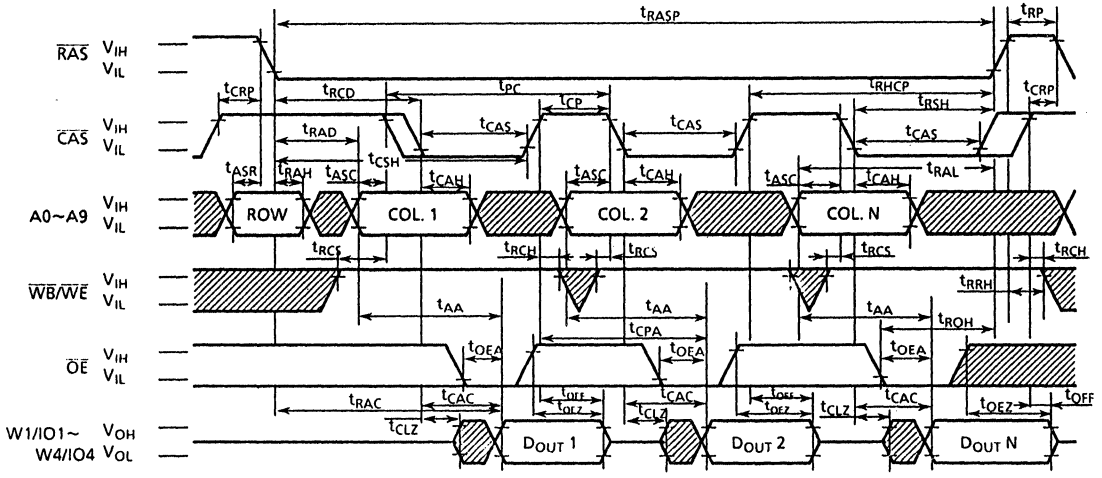
Note: D_{OUT} = OPEN

▨ : "H" or "L"

READ - MODIFY - WRITE CYCLE



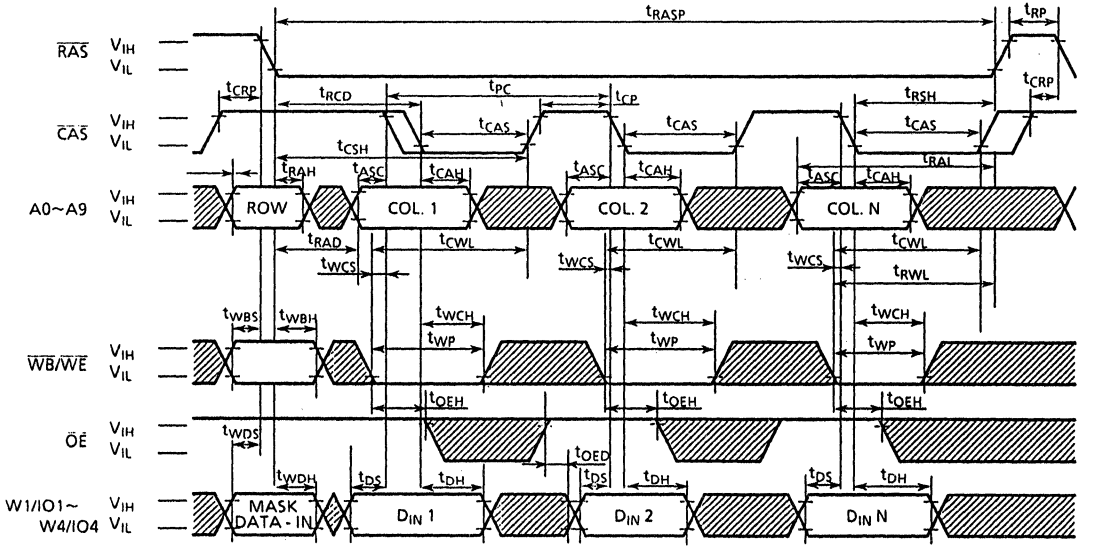
FAST PAGE MODE READ CYCLE



Note : D_{IN} = "H" or "L"

: "H" or "L"

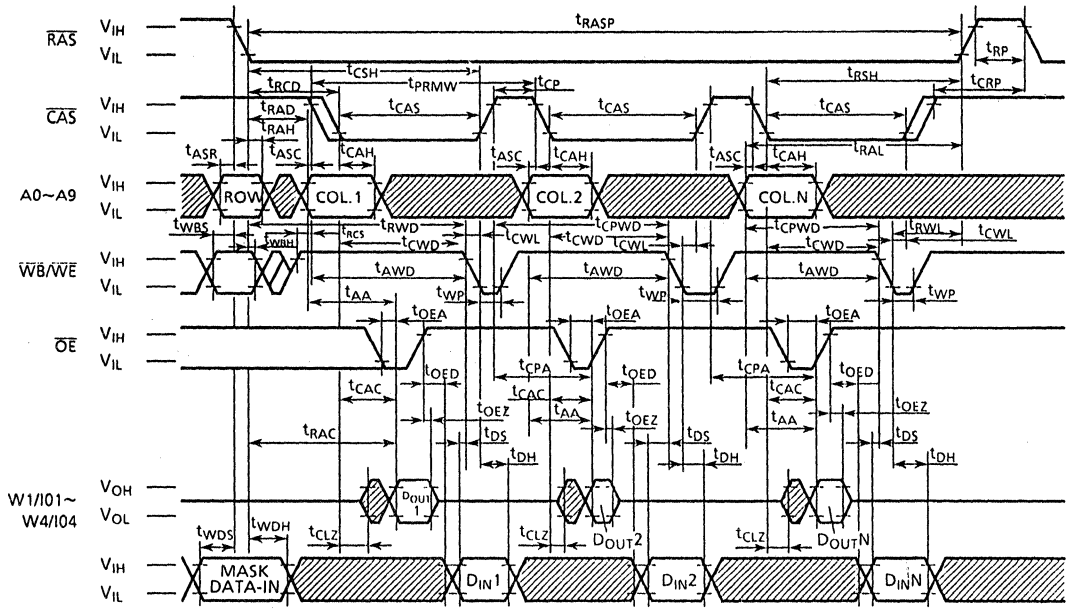
FAST PAGE MODE WRITE CYCLE



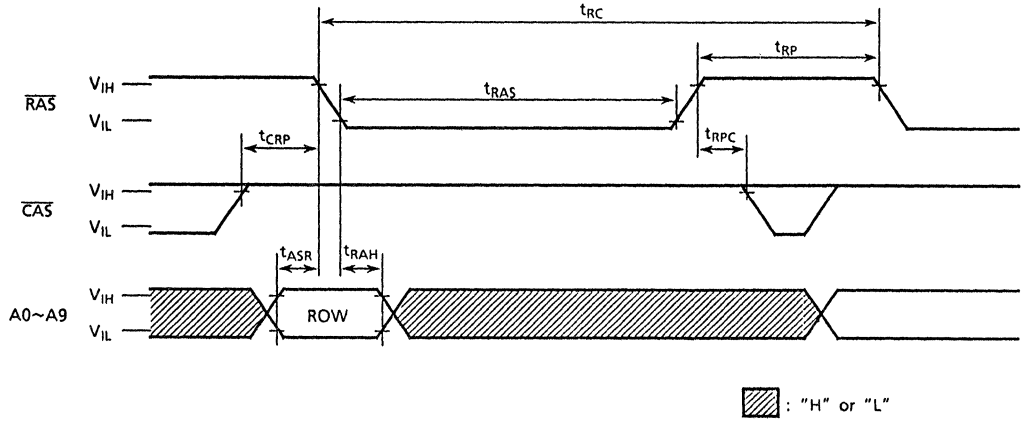
: "H" or "L"

Note : D_{OUT} = OPEN

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

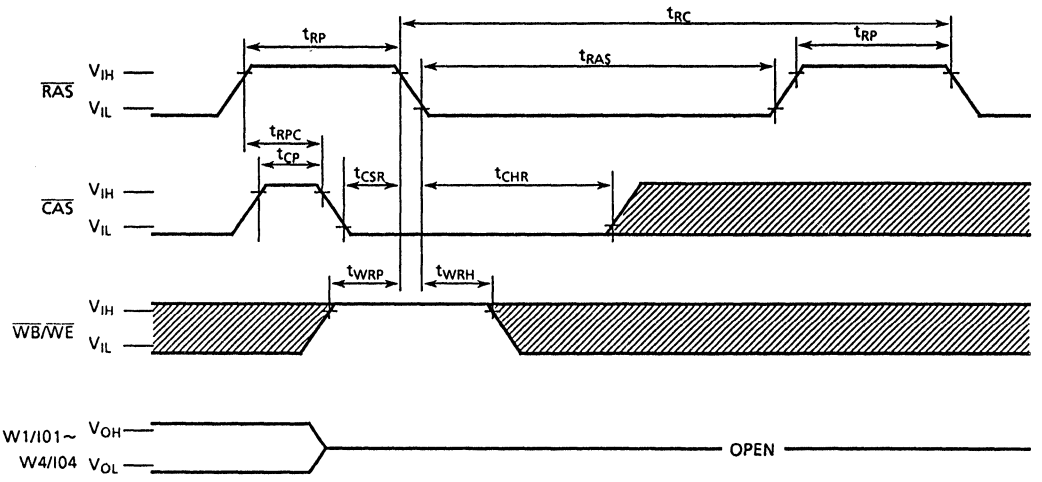


RAS ONLY REFRESH CYCLE



Note: WRITE, OE = "H" or "L"

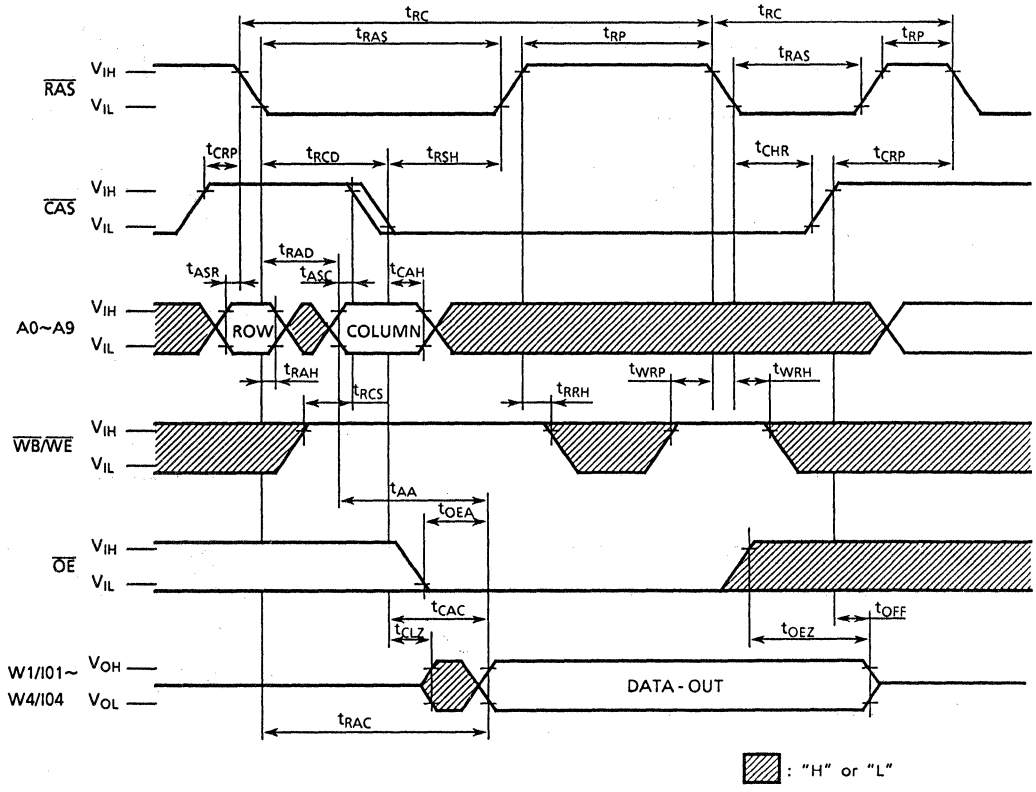
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



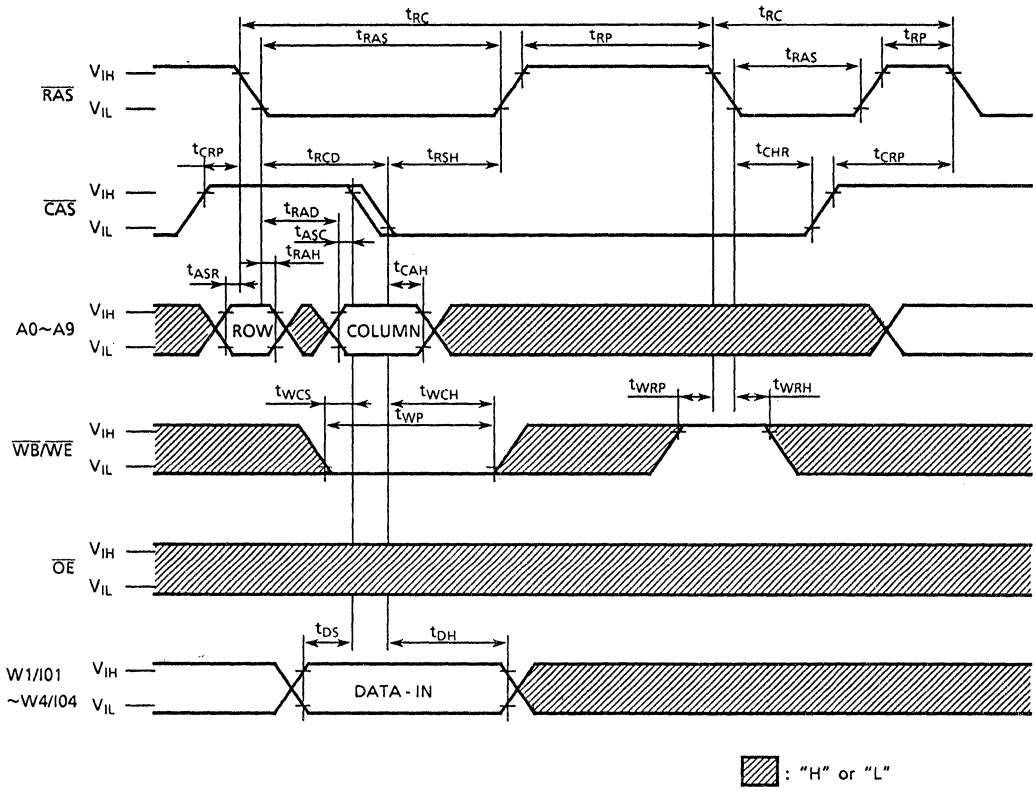
Note : D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

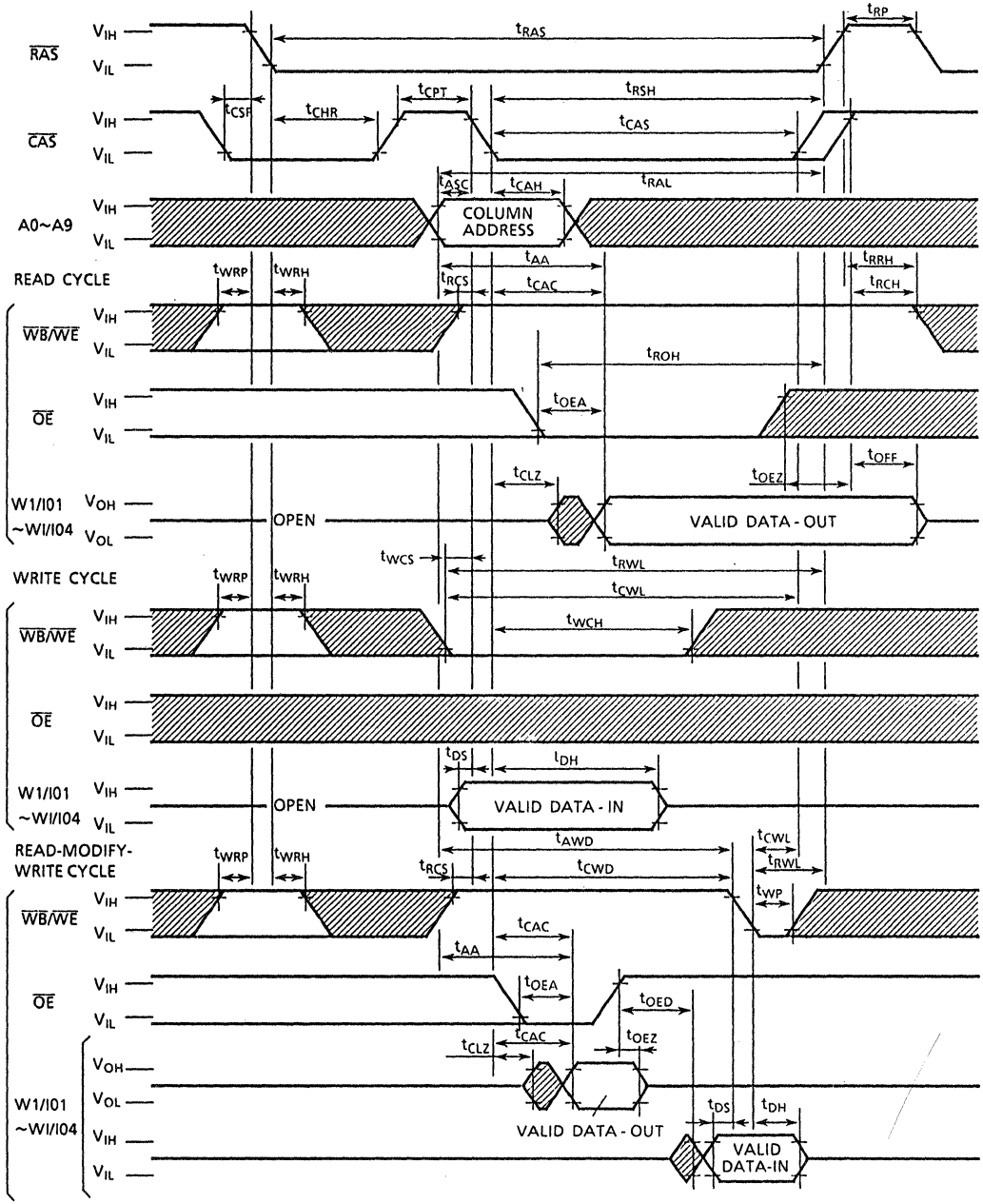
HIDDEN REFRESH CYCLE (READ)



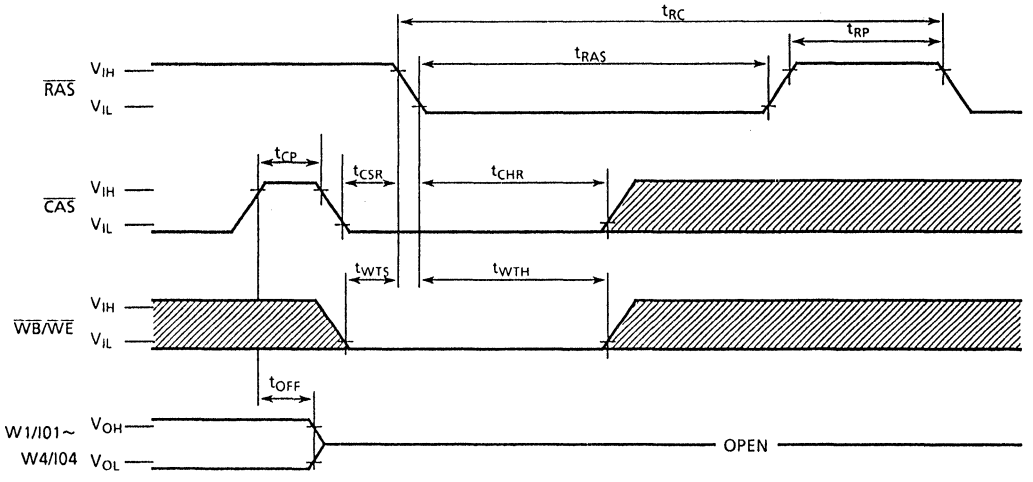
HIDDEN REEFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



$\overline{WE}$, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note : D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC51410AP/AJ/ASJ/AZ are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUTS

A write cycle is performed by bringing ($\overline{WB}$/) $\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/) $\overline{WE}$ strobes data on (Wi) IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi (/IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition. For those data bits of Wi (/IOi) that are kept low as $\overline{RAS}$ talls the write operation is inhibited on the chip if $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

DATA OUTPUTS

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valied after the access time has elapsed and remains valied while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffer are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the output. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0~A9) within each 16 millisecond time interval.
Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

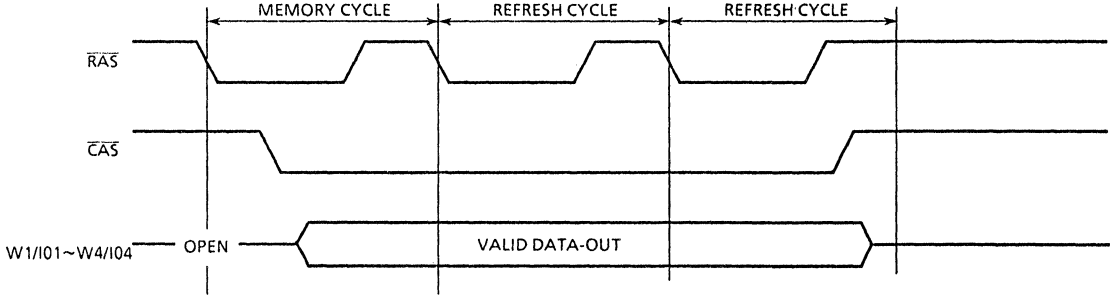
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514410AP/AJ/ASJ/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

PAGE MODE

The "Page-Mode" feature of the TC514410AP/AJ/ASJ/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514410AP/AJ/ASJ/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TC514410AP/AJ/ASJ/AZ can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. Repeat this operation 512 times.

⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

TEST MODE

The TC514410AP/AJ/ASJ/AZ is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{00} is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514410J/Z. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

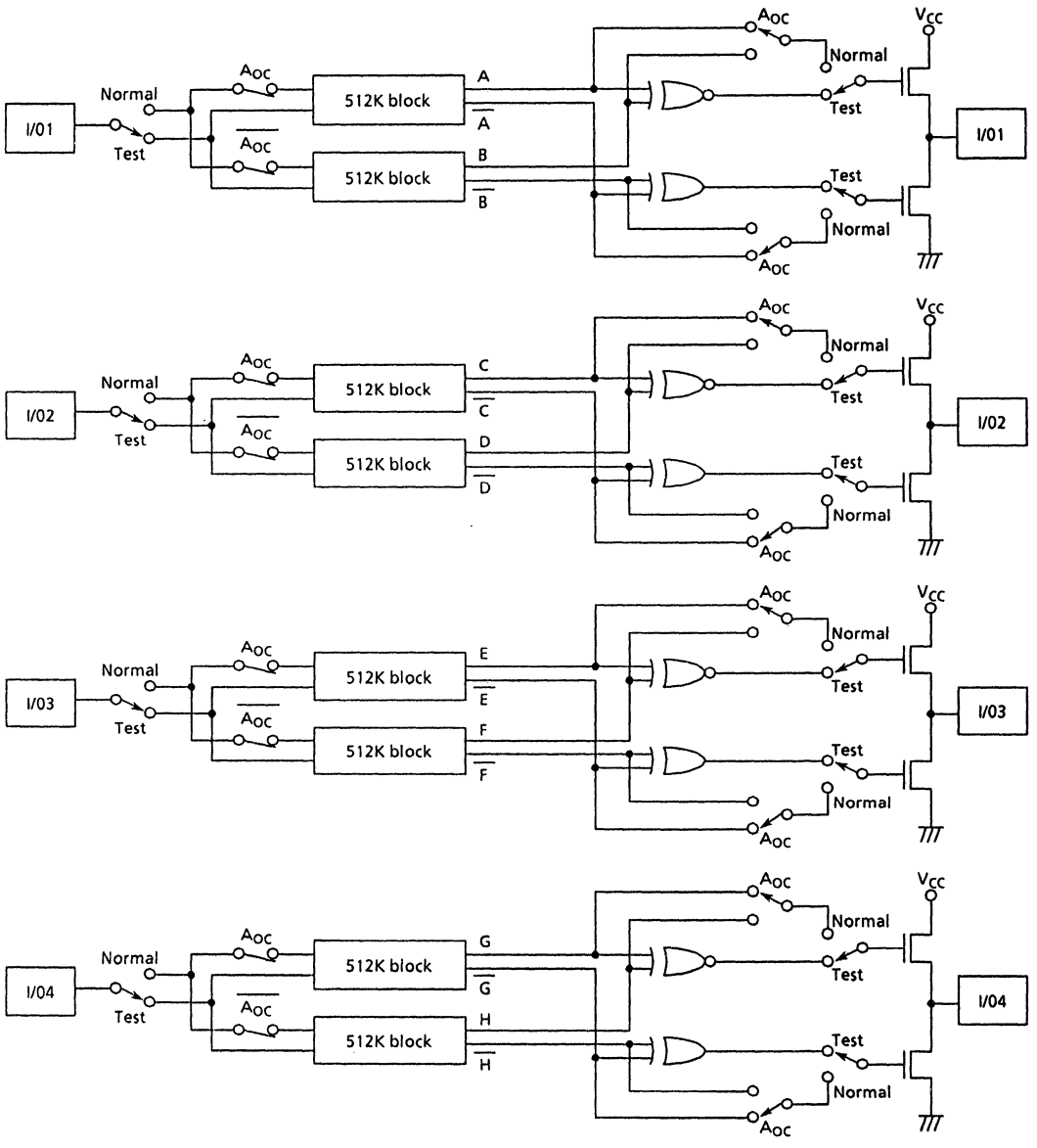


Fig. 1

NOTES

1,048,576 WORD × 4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514410AP/AJ/ASJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514410AP/AJ/ASJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514410AP/AJ/ASJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300 / 350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performace logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

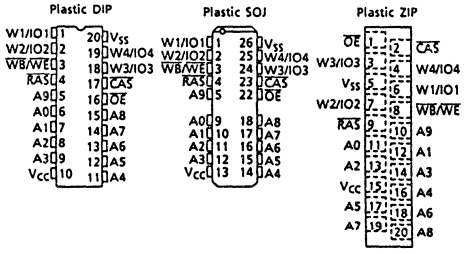
		TC514410AP/AJ/ASJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns	60ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 550mW MAX. Operating (TC514410AP/AJ/ASJ/AZ-70)
  - 468mW MAX. Operating (TC514410AP/AJ/ASJ/AZ-80)
  - 413mW MAX. Operating (TC514410AP/AJ/ASJ/AZ-10)
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write per Bit, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL Compatible
- 1024 refresh cycles/16ms
- Package
  - TC514410AP : DIP20-P-300C
  - TC514410AJ : SOJ26-P-350
  - TC514410ASJ : SOJ26-P-300A
  - TC514410AZ : ZIP2-P-400A

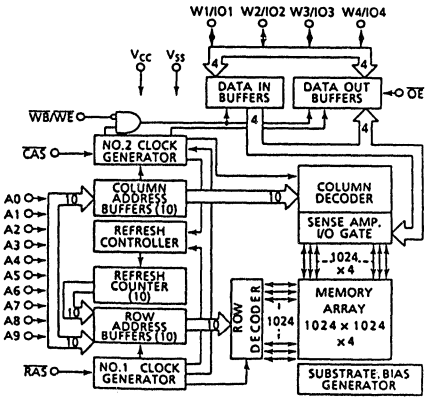
PIN NAMES

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/WE}$	Write Per Bit/Read/Write Input
$\overline{OE}$	Output Enable
W1/IO1~W4/IO4	Write Select/Date Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514410AP/AJ/ASJ/AZ-70	–	100	mA	3, 4 5
		TC514410AP/AJ/ASJ/AZ-80	–	85		
		TC514410AP/AJ/ASJ/AZ-10	–	75		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514410AP/AJ/ASJ/AZ-70	–	100	mA	3, 5
		TC514410AP/AJ/ASJ/AZ-80	–	85		
		TC514410AP/AJ/ASJ/AZ-10	–	75		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514410AP/AJ/ASJ/AZ-70	–	70	mA	3, 4 5
		TC514410AP/AJ/ASJ/AZ-80	–	65		
		TC514410AP/AJ/ASJ/AZ-10	–	55		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514410AP/AJ/ASJ/AZ-70	–	100	mA	3, 5
		TC514410AP/AJ/ASJ/AZ-80	–	85		
		TC514410AP/AJ/ASJ/AZ-10	–	75		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins not under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514410AP/ AJ/ASJ/AZ-70		TC514410AP/ AJ/ASJ/AZ-80		TC514410AP/ AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	–	205	–	245	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	105	–	125	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	200,000	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514410AP/ AJ/ASJ/AZ-70		TC514410AP/ AJ/ASJ/AZ-80		TC514410AP/ AJ/ASJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	12
t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	70	–	85	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	75	–	75	–	90	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	25	–	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	–	0	–	0	–	ns	
t_{WBH}	Write Per Bit Hold Time	10	–	10	–	10	–	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	–	0	–	0	–	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514410AP/ AJ/ASJ/AZ-70		TC514410AP/ AJ/ASJ/AZ-80		TC514410AP/ AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WTS}	Write Command Set-up Time	10	–	10	–	10	–	ns	
t_{WTH}	Write Command Hold Width	10	–	10	–	10	–	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time	10	–	10	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514410AP/AJ/ASJ/AZ-70		TC514410AP/AJ/ASJ/AZ-80		TC514410AP/AJ/ASJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	155	–	185	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	160	–	180	–	215	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	75	–	80	–	95	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	75	–	85	–	105	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	9,14
t_{AA}	Access Time from Column Address	–	40	–	45	–	55	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	50	–	60	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	75	10,000	85	10,000	105	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	75	200,000	85	200,000	105	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	75	–	85	–	105	–	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	–	50	–	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	45	–	55	–	ns	
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	–	55	–	65	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	105	–	115	–	140	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	70	–	75	–	90	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	80	–	80	–	95	–	ns	13
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	30	–	ns	

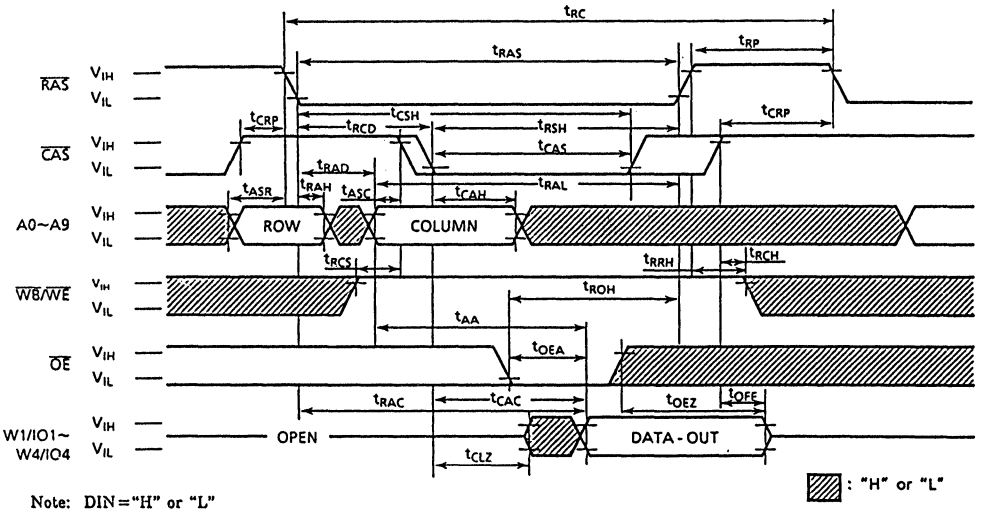
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/I01~I/I04)	–	7	pF

NOTES:

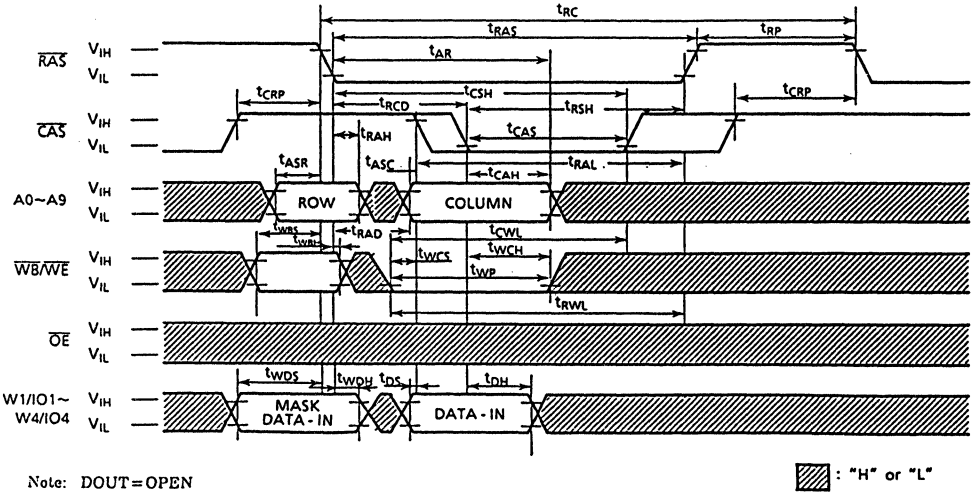
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE



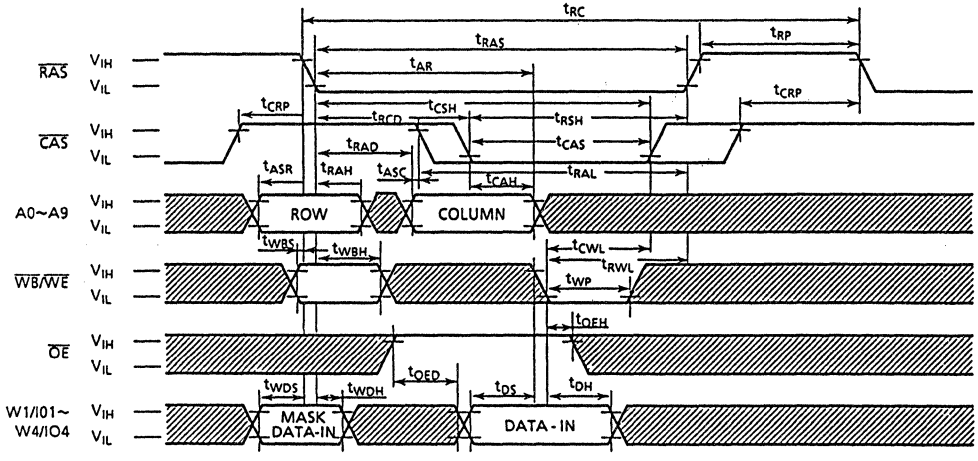
Note: DIN = "H" or "L"

WRITE CYCLE (EARLY WRITE)



Note: DOUT = OPEN

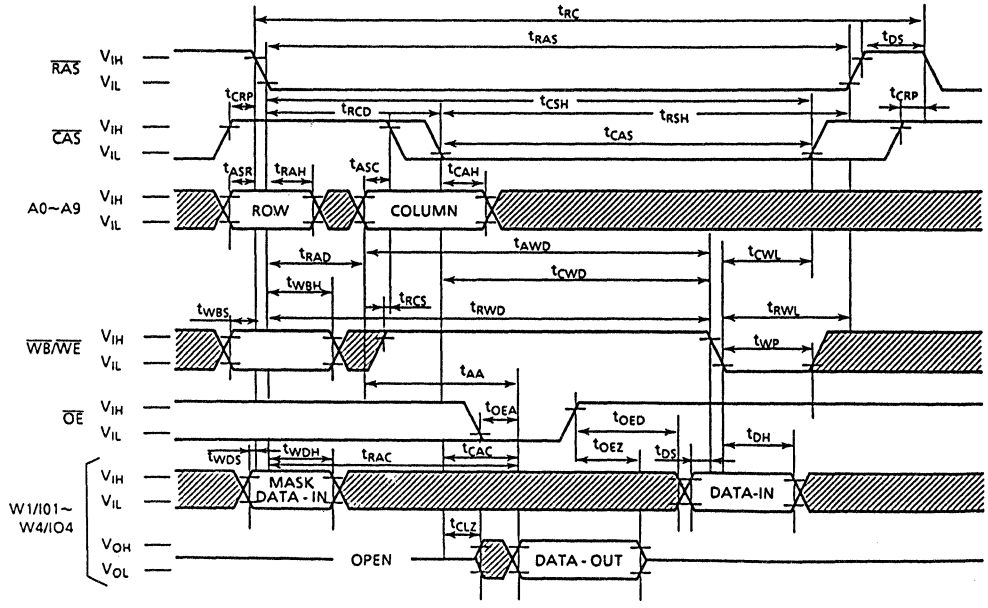
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



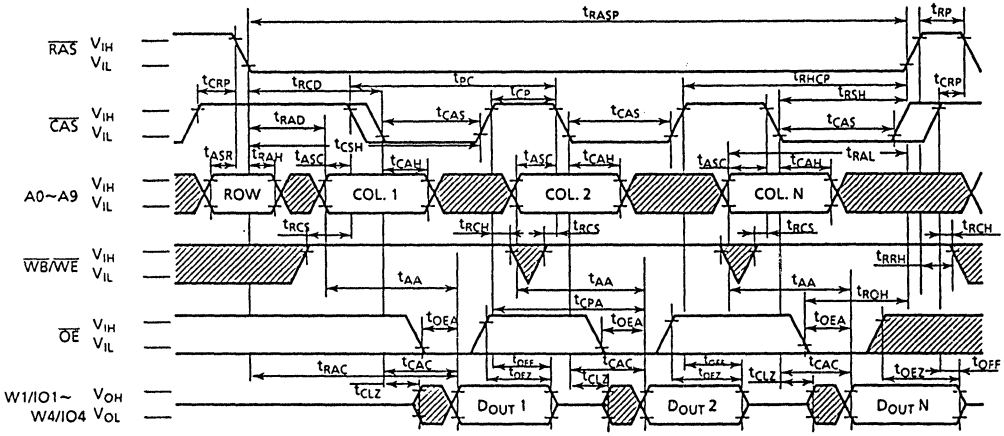
Note: D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



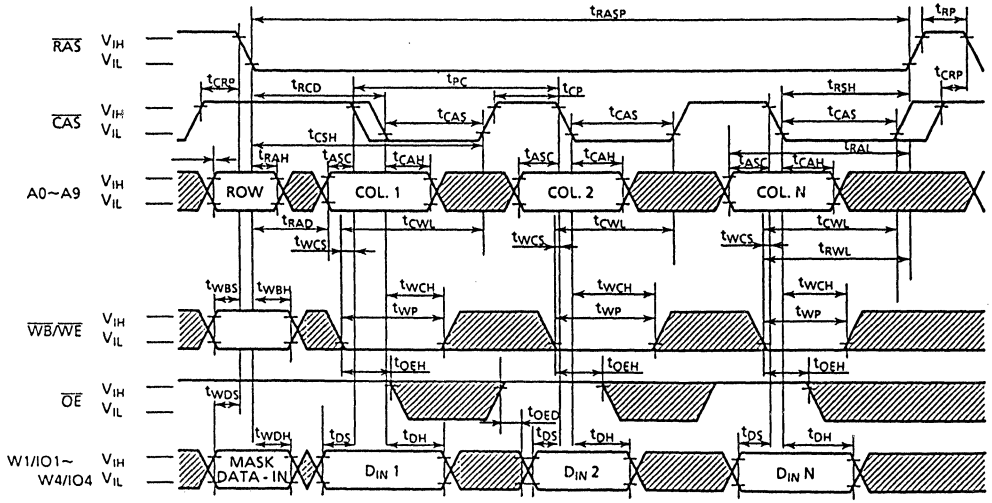
FAST PAGE MODE READ CYCLE



Note: D_{IN} = "H" or "L"

: "H" or "L"

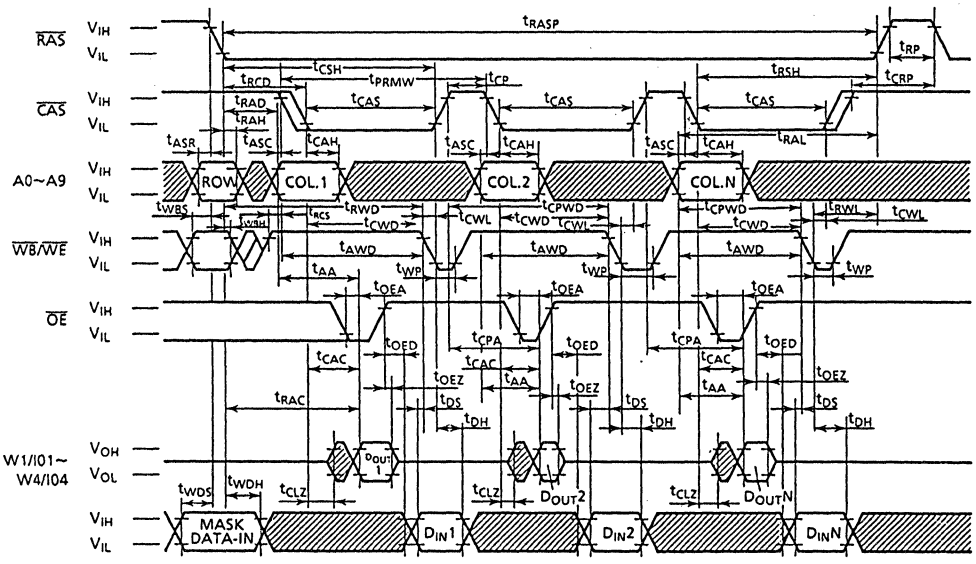
FAST PAGE MODE WRITE CYCLE



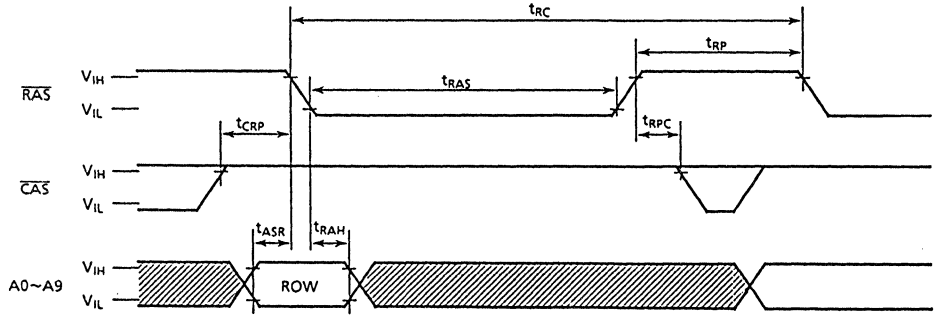
: "H" or "L"

Note: D_{OUT} = OPEN

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



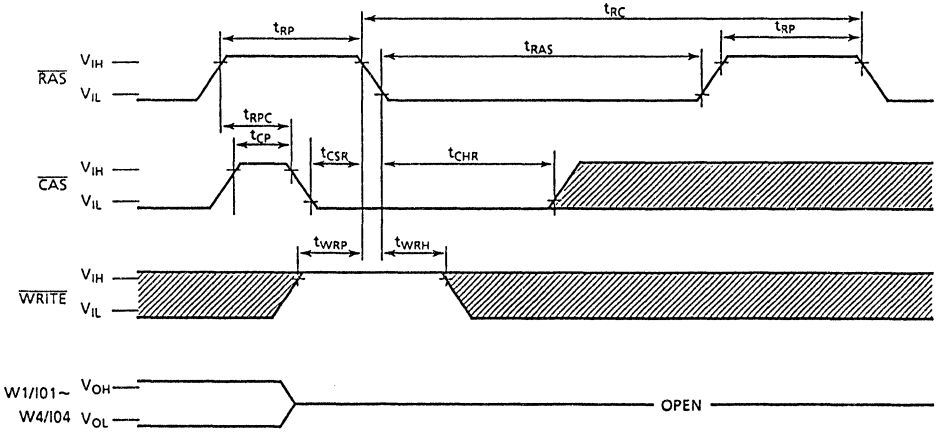
RAS ONLY REFRESH CYCLE



: "H" or "L"

Note: WRITE, OE = "H" or "L"

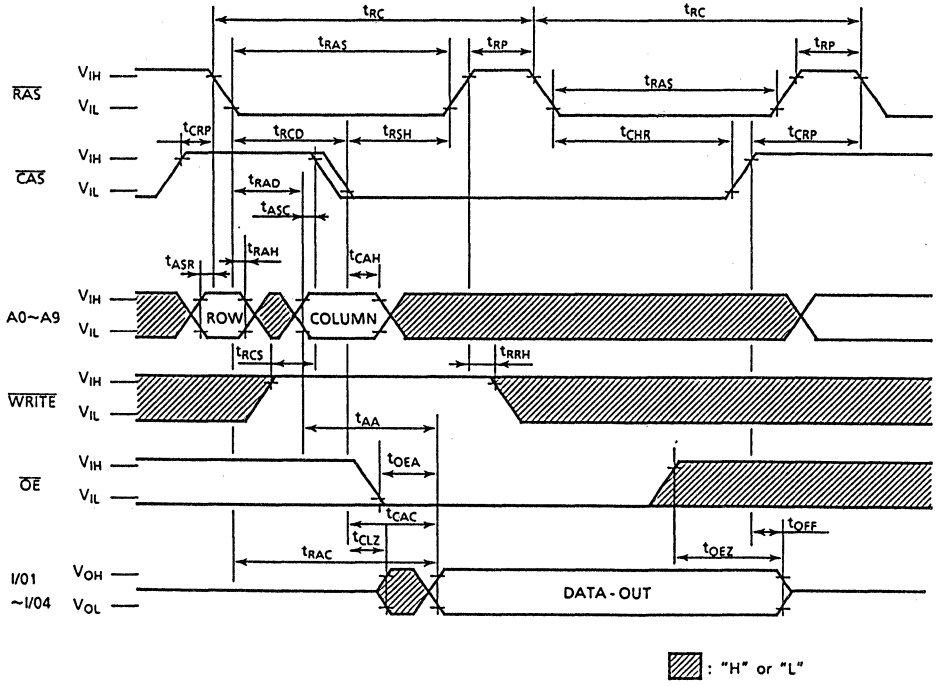
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



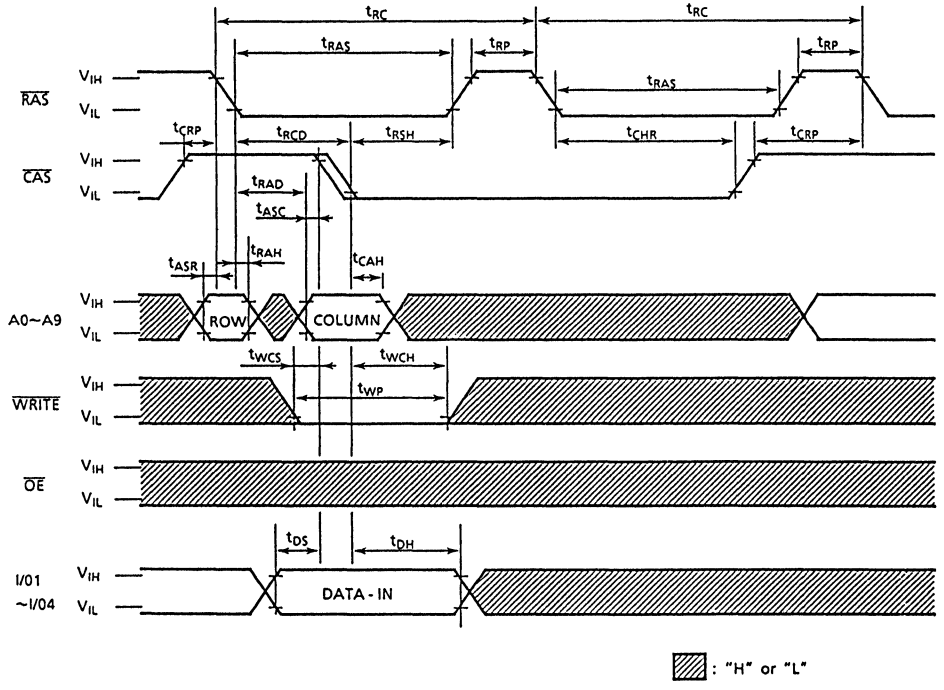
Note : D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

: "H" or "L"

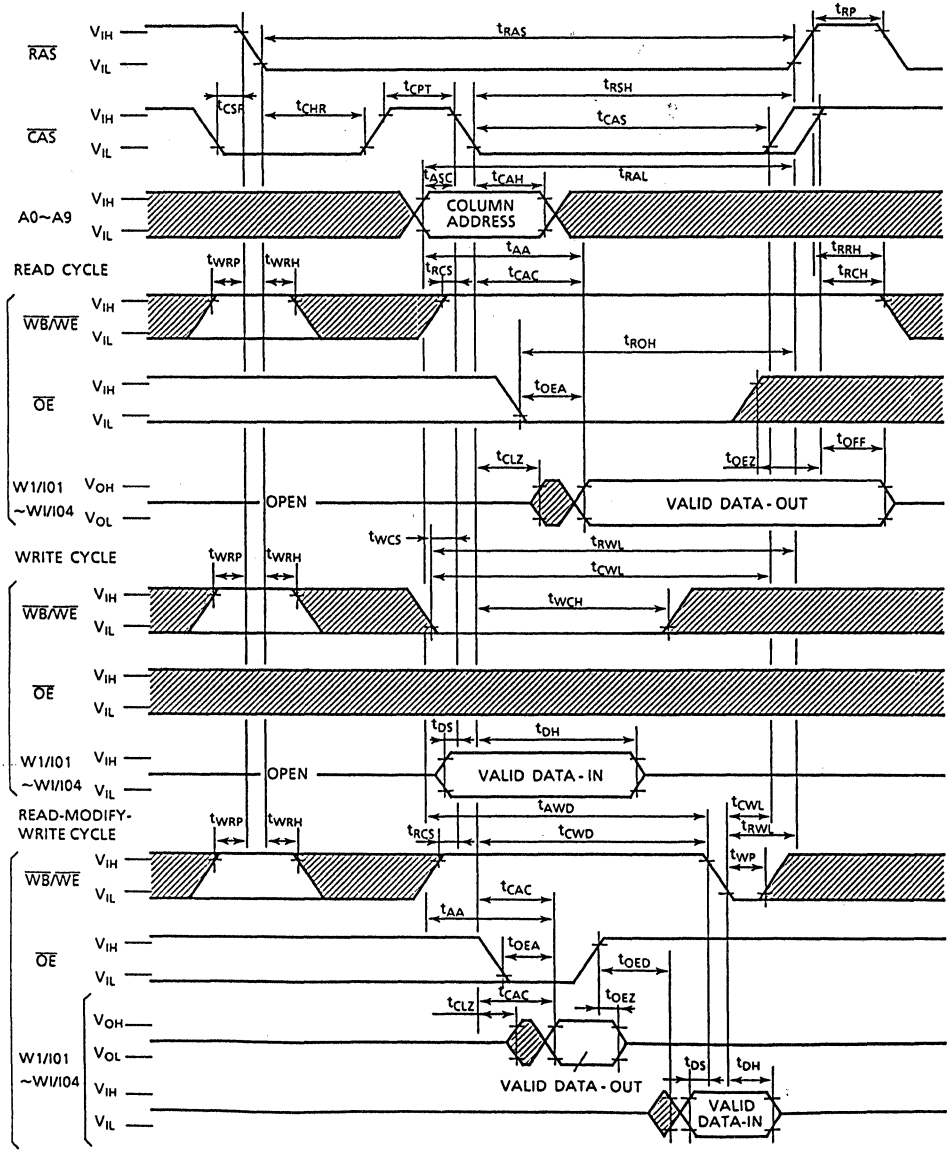
HIDDEN REFRESH CYCLE (READ)



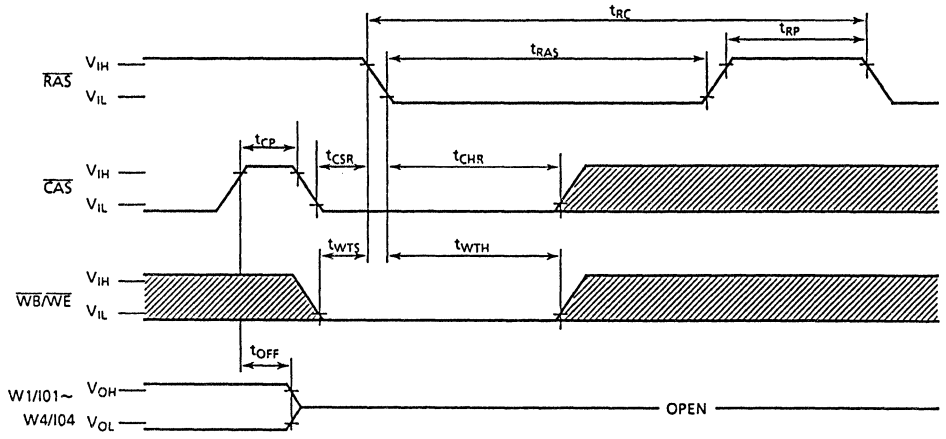
HIDDEN REEFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WE, CAS BEFORE RAS REFRESH CYCLE



Note : D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC51410AP/AJ/ASJ/AZ are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUTS

A write cycle is performed by bringing ($\overline{WB}$/) $\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/) $\overline{WE}$ strobes data on (Wi) IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi (/IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition. For those data bits of Wi (/IOi) that are kept low as $\overline{RAS}$ falls the write operation is inhibited on the chip if $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

DATA OUTPUTS

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valied after the access time has elapsed and remains valied while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffer are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the output. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0~A9) within each 16 millisecond time interval.
Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

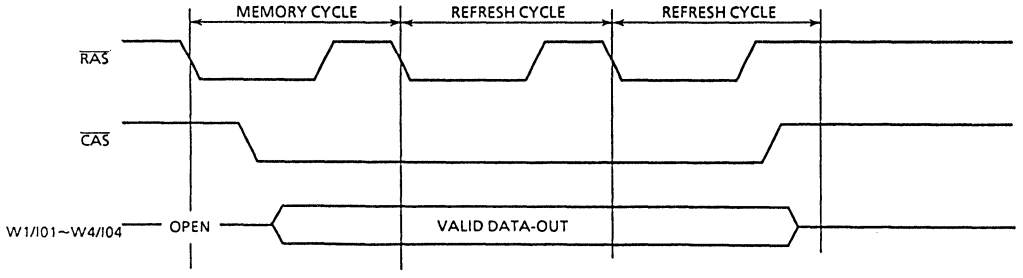
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514410AP/AJ/ASJ/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

PAGE MODE

The "Page-Mode" feature of the TC514410AP/AJ/ASJ/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514410AP/AJ/ASJ/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TC514410AP/AJ/ASJ/AZ can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.
② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.
③ Check "1" out of 512 bits at normal read mode, which was written at ②.
④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. Repeat this operation 512 times.
⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ to the complement data.

TEST MODE

The TC514410AP/AJ/ASJ/AZ is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{00} is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514410J/Z. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

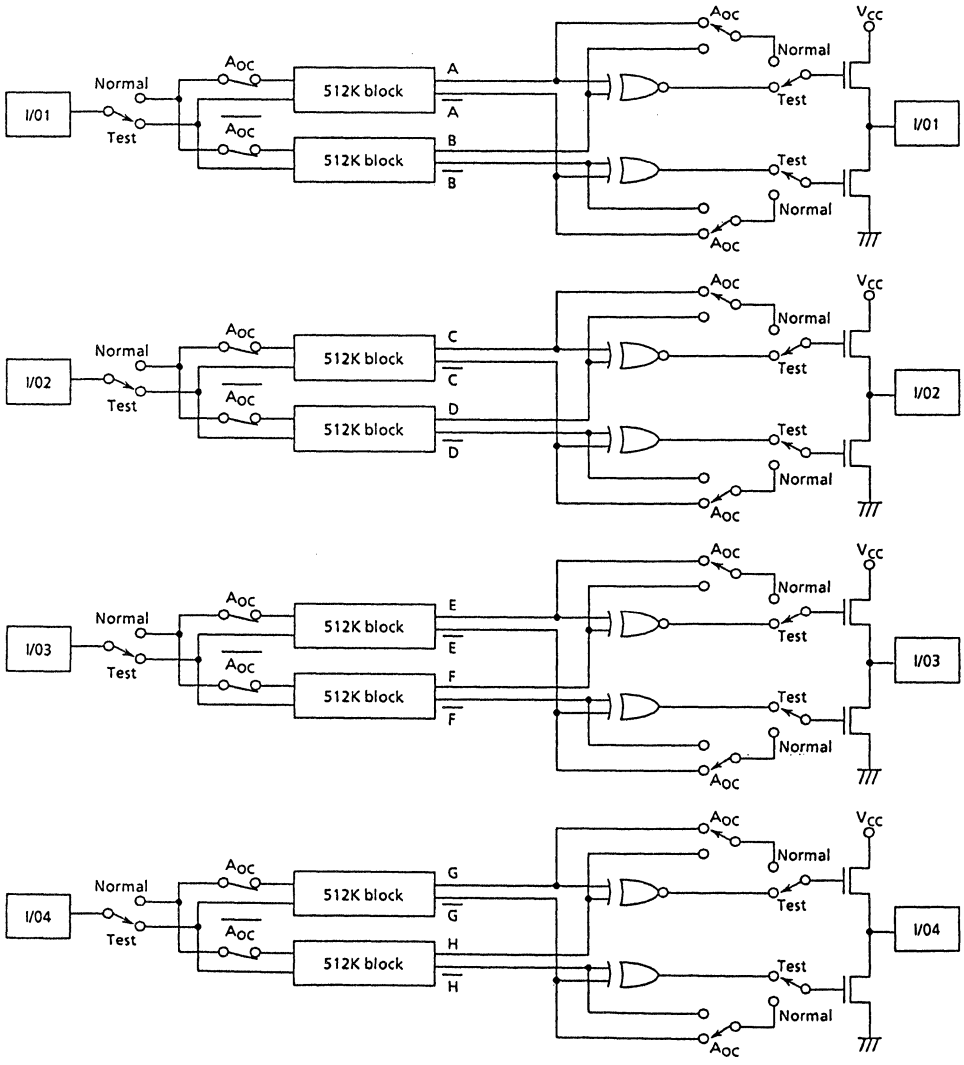


Fig. 1

NOTES

DYNAMIC RAM MODULES

4,194,304 WORDS×8 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM84000S is a 4,194,304 words by 8 bits dynamic RAM module which assembled 8 pcs of TC514000J on the printed circuit board.

The THM84000S is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

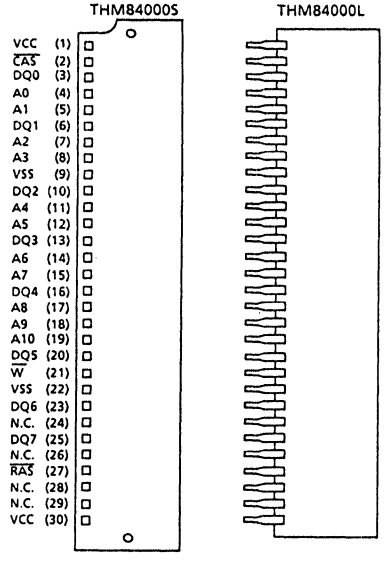
FEATURES

- 4,194,304 words by 8 bits organization
- Fast access time

		THM84000S/L-80	THM84000S/L-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low power 4,400mW MAX. Operating (THM84000S/L-80)
  3,740mW MAX. Operating (THM84000S/L-10)
  44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 refresh cycles/16ms

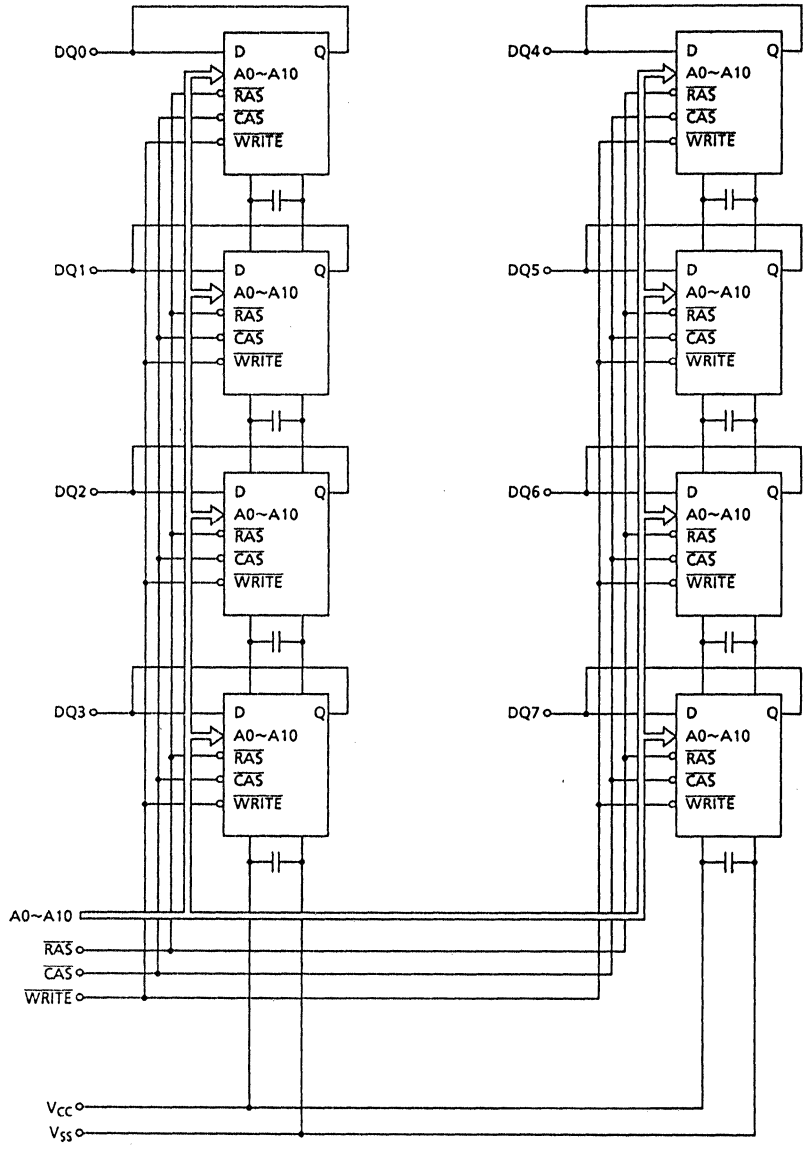
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A10	Address Inputs
DQ0~DQ7	Data Inputs/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	• Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx−80	–	800	mA	3, 4
		THMxxxxxx−10	–	680		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ V_{IH}: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx−80	–	800	mA	3
		THMxxxxxx−10	–	680		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC} = t_{PC}$ MIN.)	THMxxxxxx−80	–	480	mA	3, 4
		THMxxxxxx−10	–	400		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx−80	–	800	mA	3
		THMxxxxxx−10	–	680		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins not under Test = 0V)		−80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		−20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM84000S-80		THM84000S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	10
t_{WCH}	Write ommand Hold Time	15	–	20	–	ns	
t_{WCR}	Write ommand Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	THM84000S-80		THM84000S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	11
t_{DH}	Data Hold Time	15	–	20	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

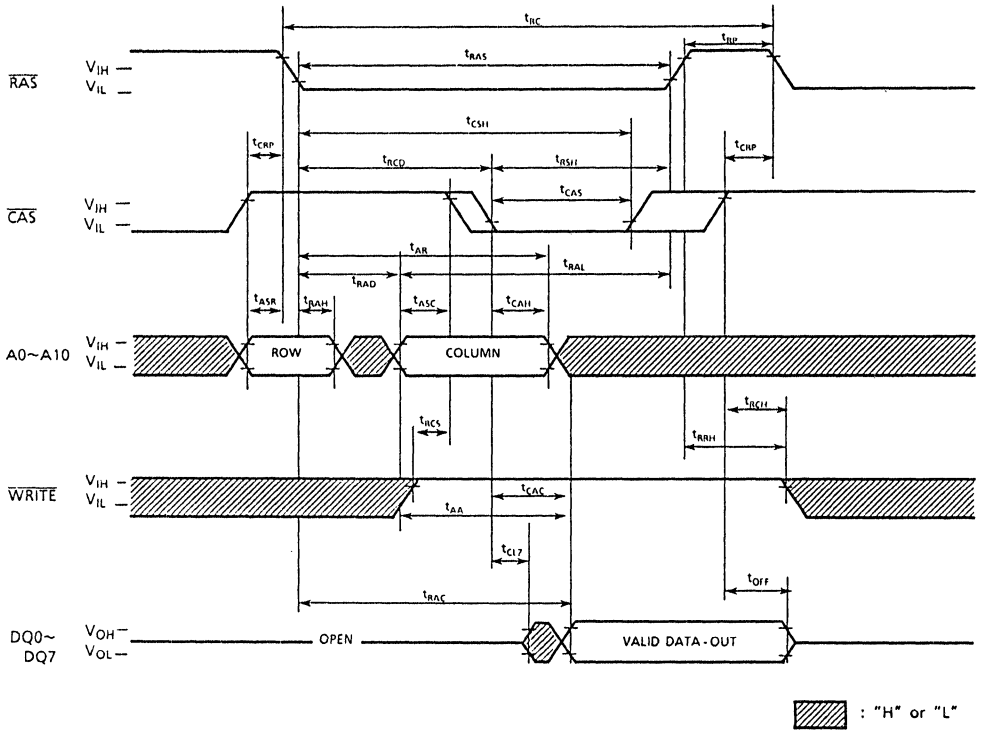
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{DQ}	I/O Capacitance (DQ0~DQ7)	–	15	pF

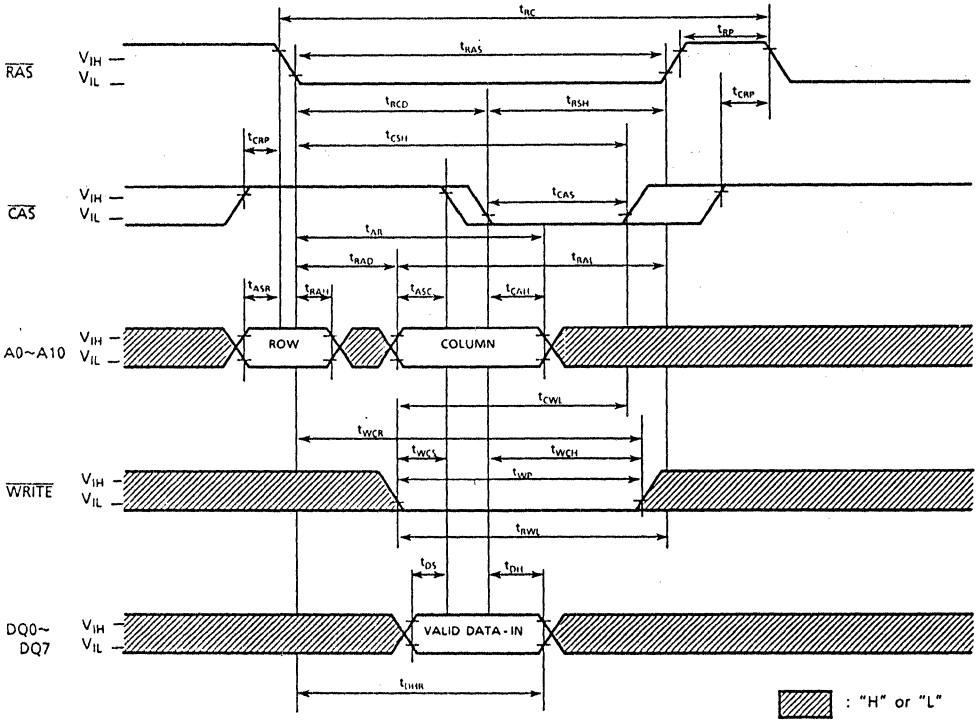
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

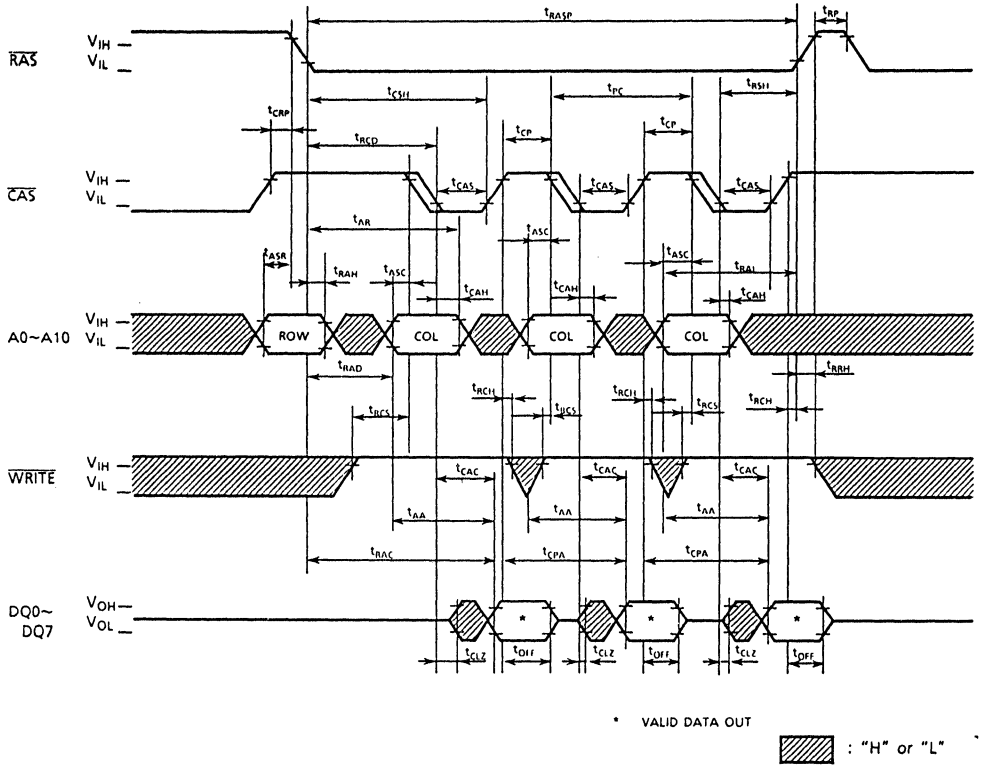
READ CYCLE


RAS
CAS
A0~A10
WRITE
DQ0~
DQ7
VIH
VIL
VOH
VOL
ROW
COLUMN
OPEN
VALID DATA-OUT
: "H" or "L"

EARLY WRITE CYCLE



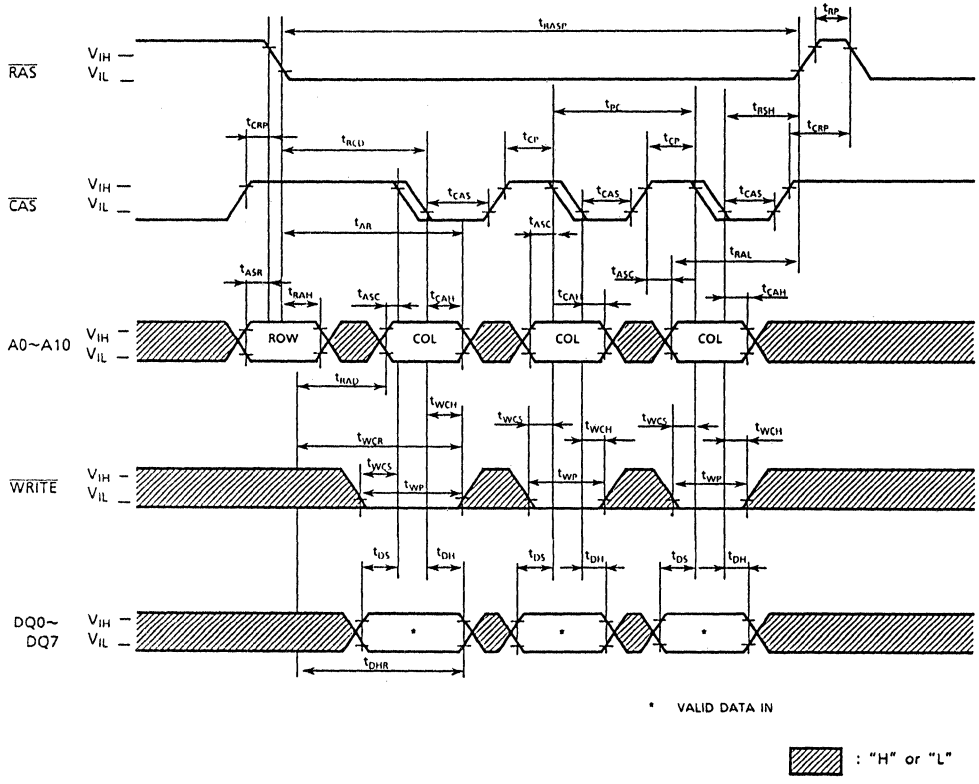
FAST PAGE MODE READ CYCLE



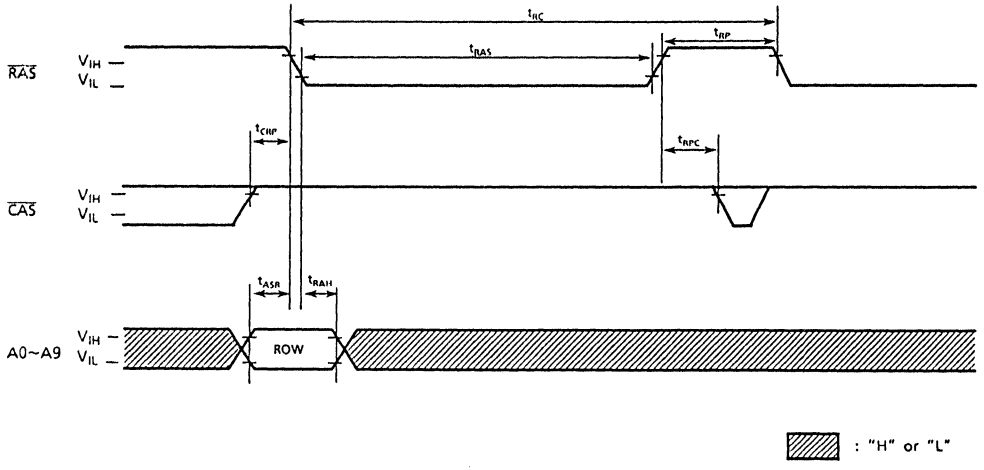
* VALID DATA OUT

▨ : "H" or "L"

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

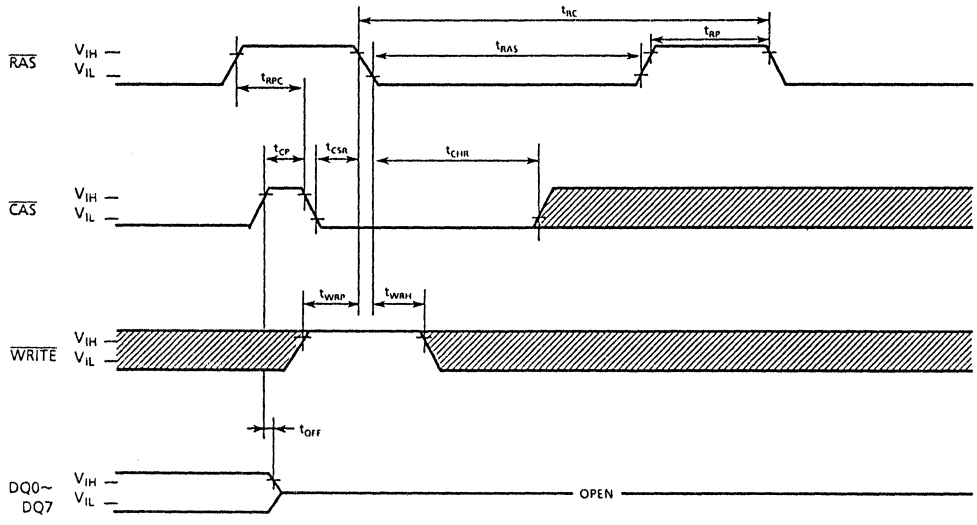


$\overline{RAS}$ ONLY REFRESH CYCLE



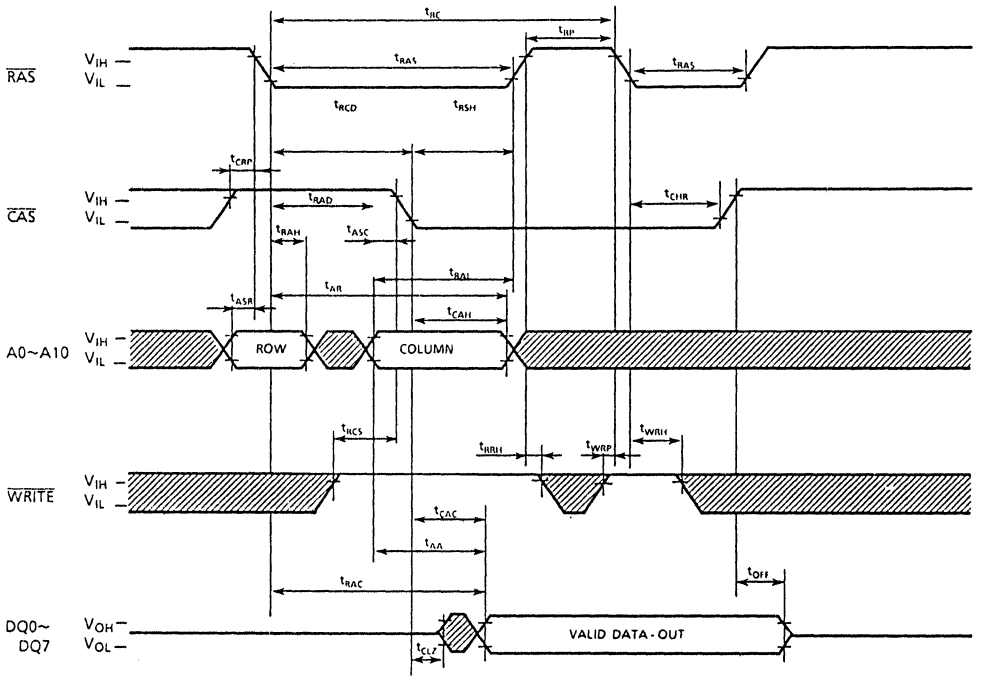
Note: $\overline{WRITE}$, A10 = "H" or "L"

CAS BEFORE RAS REFRESH CYCLE

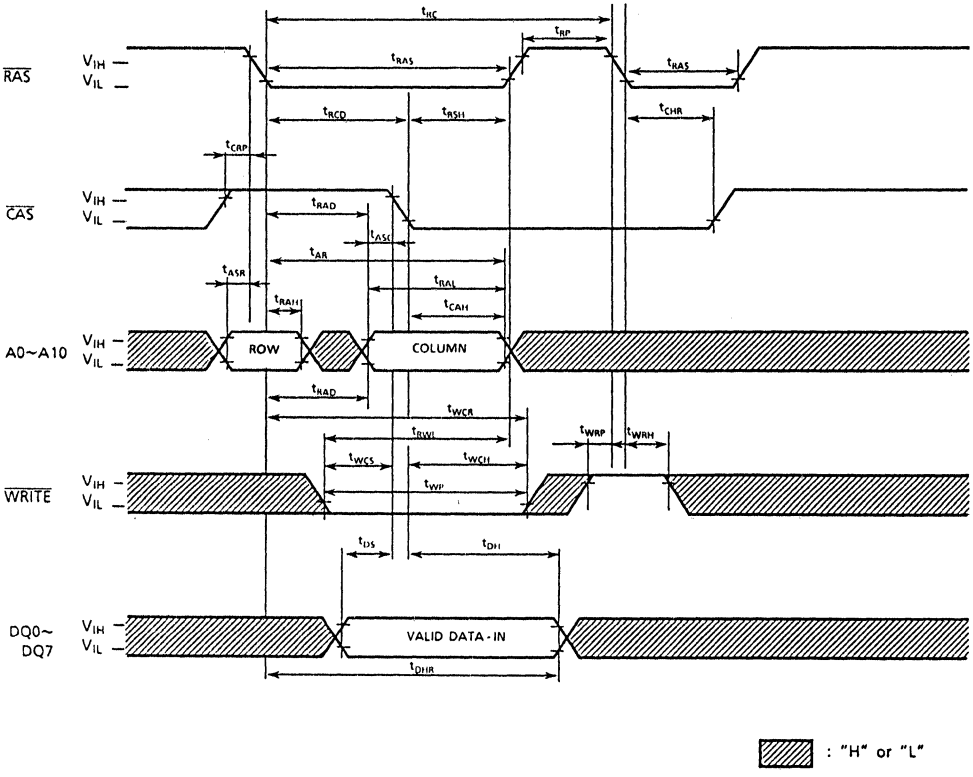


Note: A0~A10 = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

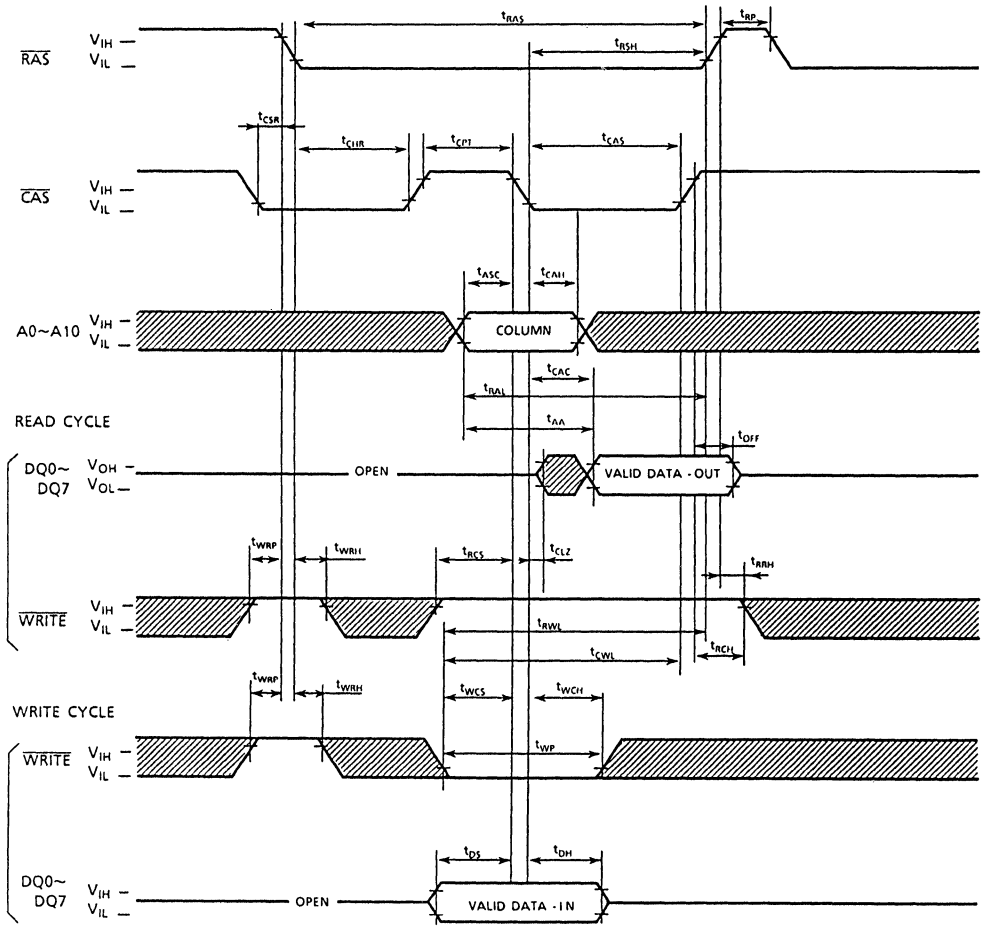


HIDDEN REFRESH CYCLE (WRITE)



: "H" or "L"

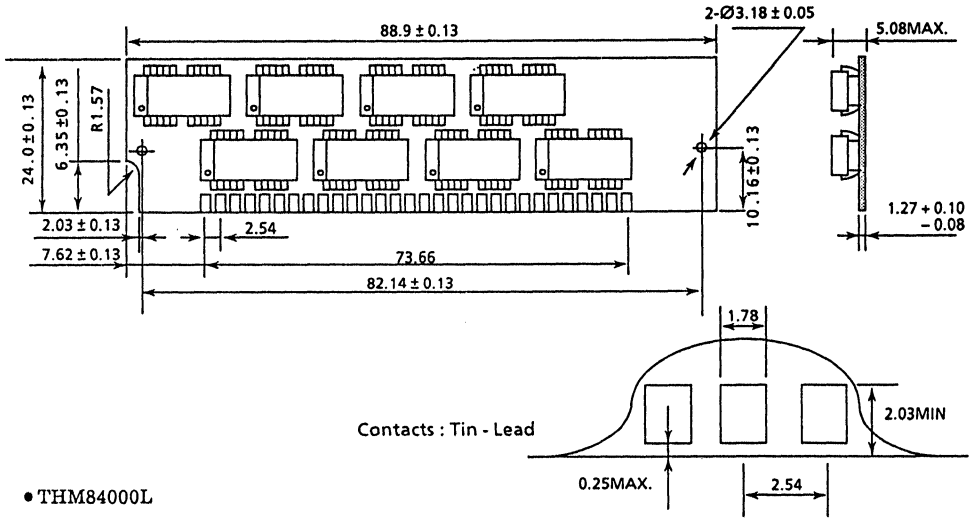
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



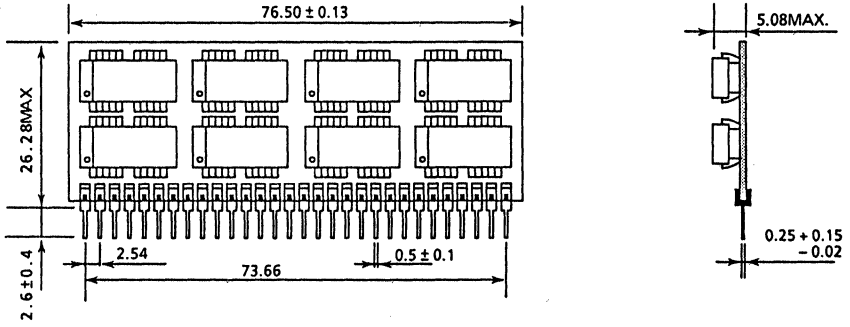
OUTLINE DRAWINGS

Unit in mm

• THM84000S



• THM84000L



1,048,576 WORDS × 32 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM321000S is a 1,048,576 words by 32 bits dynamic RAM module which assembled 8 pcs of TC514400J on the printed circuit board. The THM321000S can be as well used as 2,097,152 words by 16 bits dynamic RAM module, by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ·····, DQ15 and DQ31, respectively. The THM321000S is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

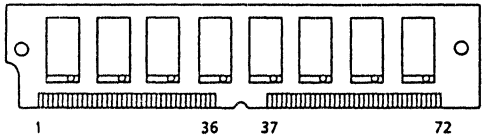
FEATURES

- 1,048,576 words by 32 bits organization
- Fast access time and cycle time

		THM321000S-80	THM321000S-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low power
  4,620mW MAX. Operating (THMxxxxx-80)
  3,960mW MAX. Operating (THMxxxxx-10)
  44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1024 Refresh cycles/16ms
- Tin-Lead Contact: THM321000S-80,10
- Gold Contact: THM321000SG-80,10

PIN CONNECTION (TOP VIEW)



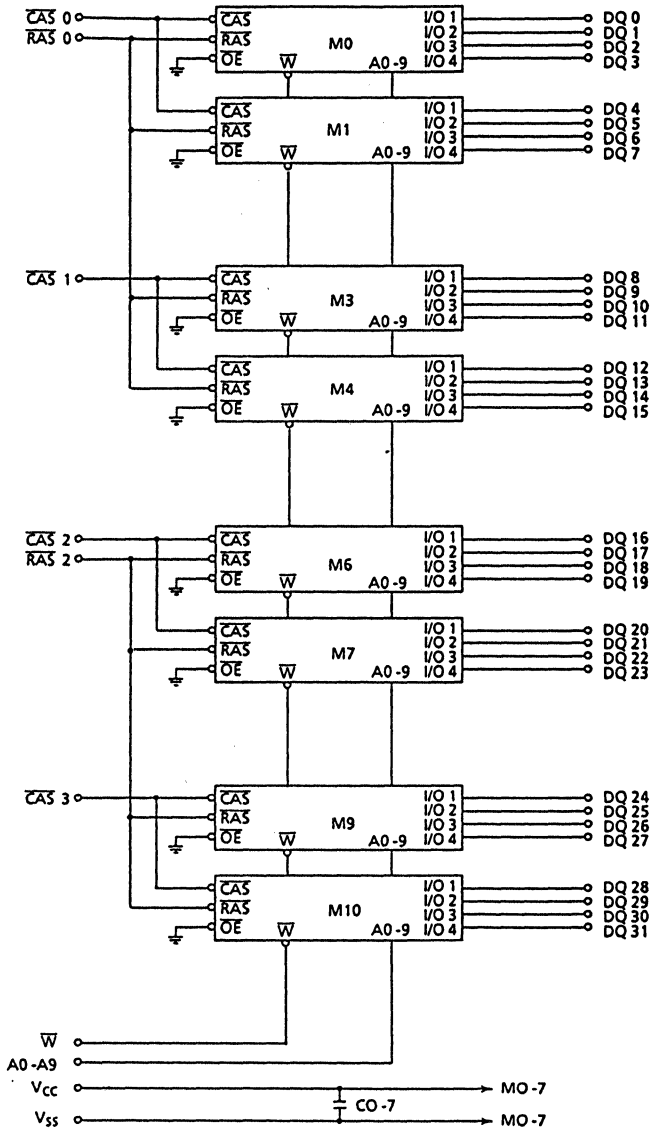
PIN NAMES

A0~A9	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	,55	DQ11	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	NC	45	NC	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

	-80	-10
PD0	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	NC	V_{SS}
PD3	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THM321000S-80	–	840	mA	3, 4
		THM321000S-10	–	720		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	THM321000S-80	–	840	mA	3
		THM321000S-10	–	720		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} MIN.)	THM321000S-80	–	560	mA	3, 4
		THM321000S-10	–	480		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THM321000S-80	–	840	mA	3
		THM321000S-10	–	720		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins not under Test = 0V)		– 80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
I_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM321000S-80		THM321000S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THM321000S-80		THM321000S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	ns	
t_{DS}	Date Set-Up Time	0	–	0	–	ns	11
t_{DH}	Date Hold Time	15	–	20	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

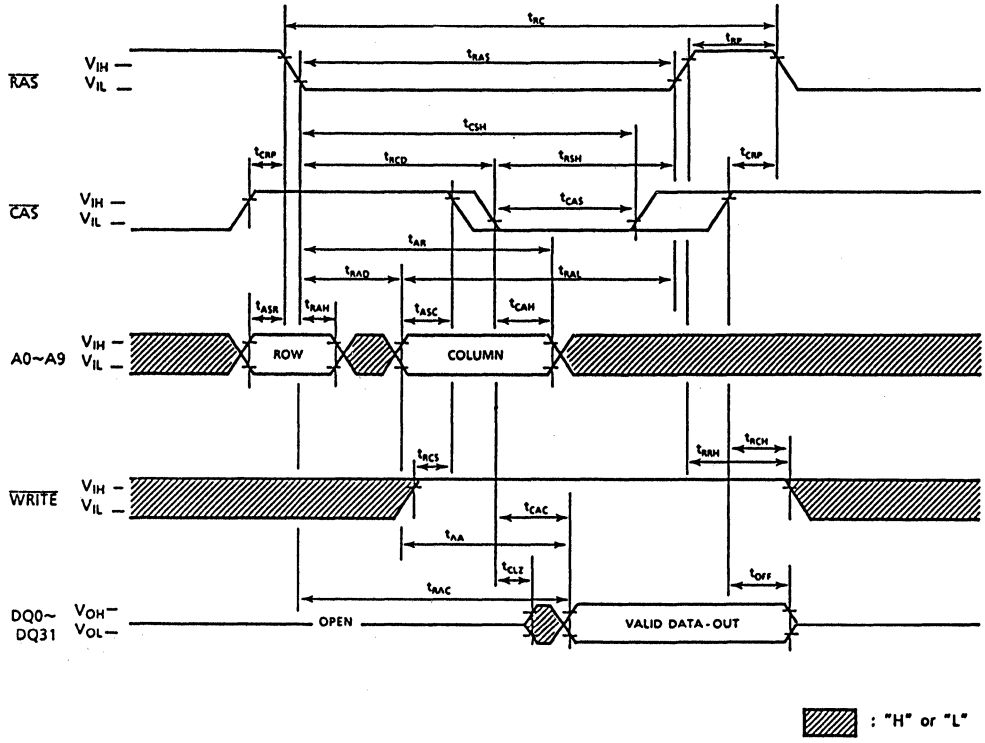
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A9)	–	60	pF
CI2	Input Capacitance ($\overline{W}$)	–	45	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	–	35	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	–	30	pF
CDQ1	I/O Capacitance (DQ0~31)	–	17	pF

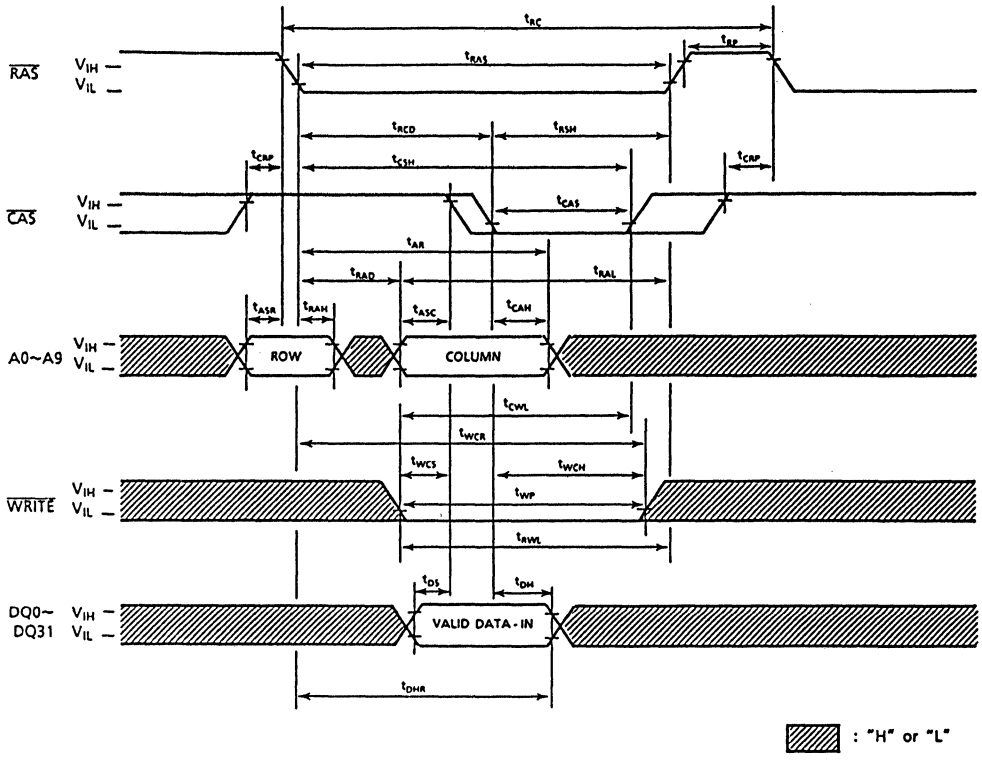
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
    t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met.
    t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

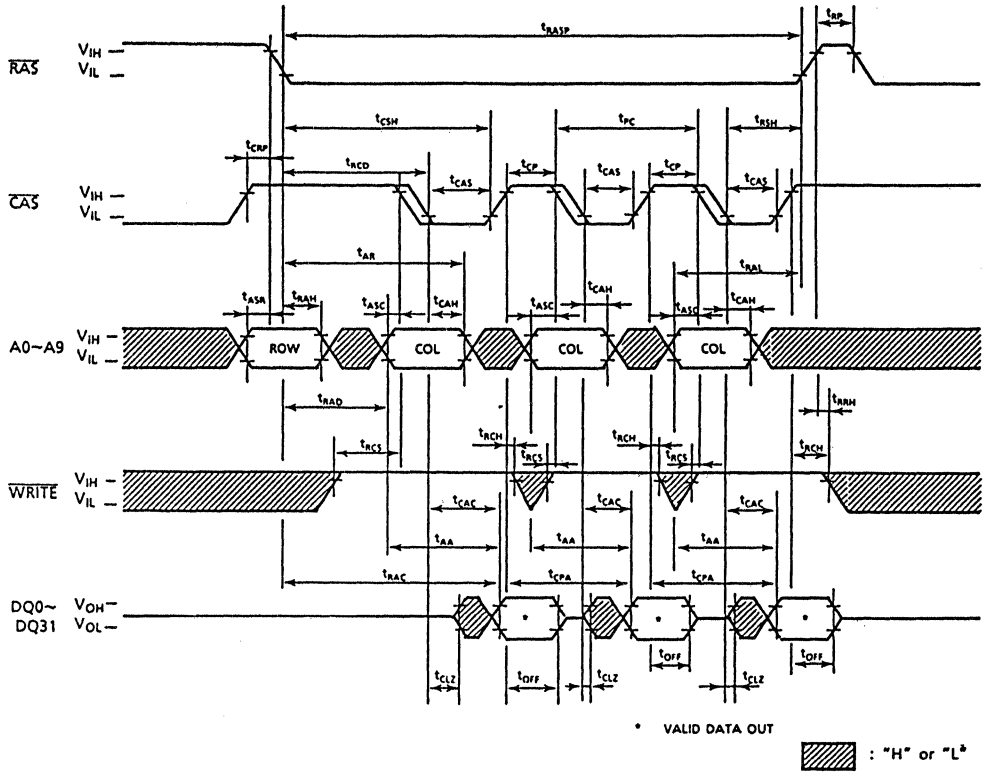
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tCAC
tAA
tCLZ
tOFF
tRAC
DQ0~
DQ31
VOH
VOL
OPEN
VALID DATA-OUT
: "H" or "L"

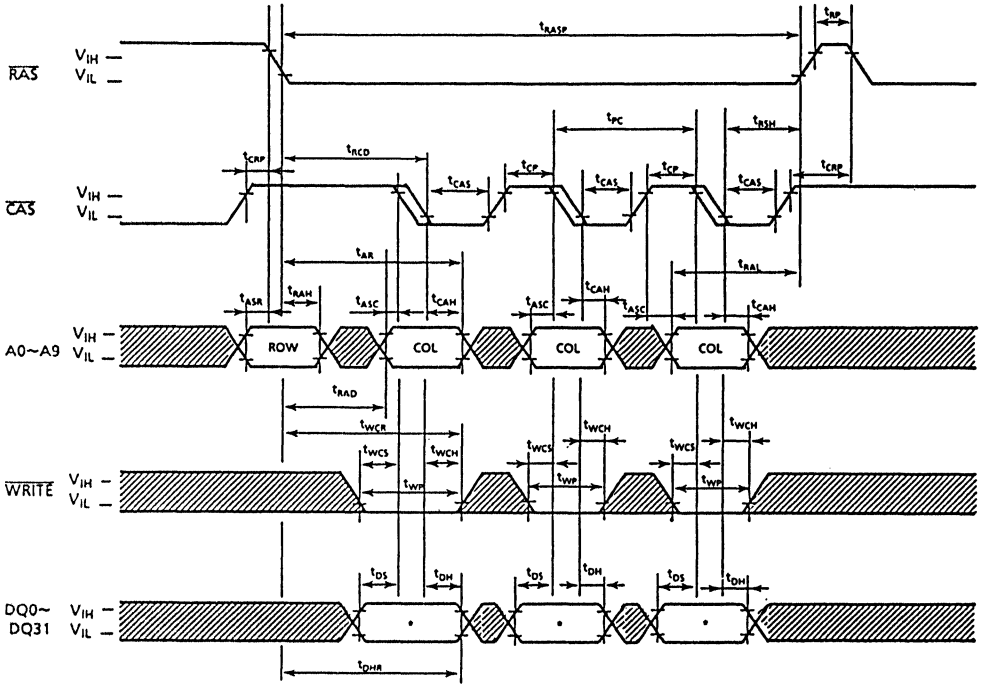
EARLY WRITE CYCLE



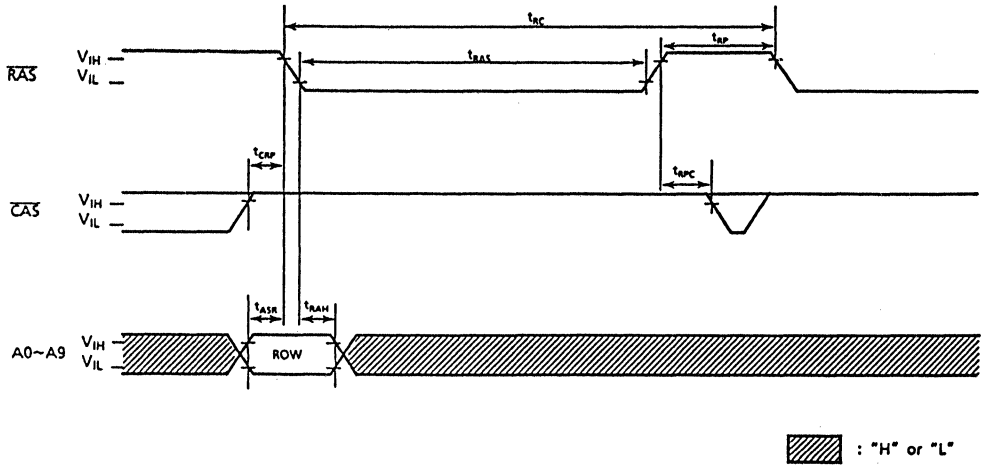
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

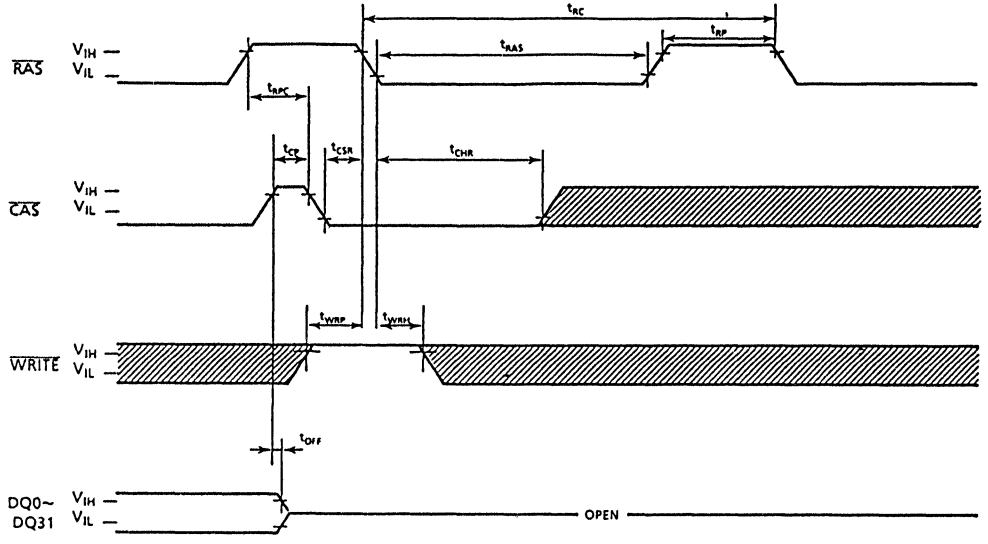


$\overline{RAS}$ ONLY REFRESH CYCLE



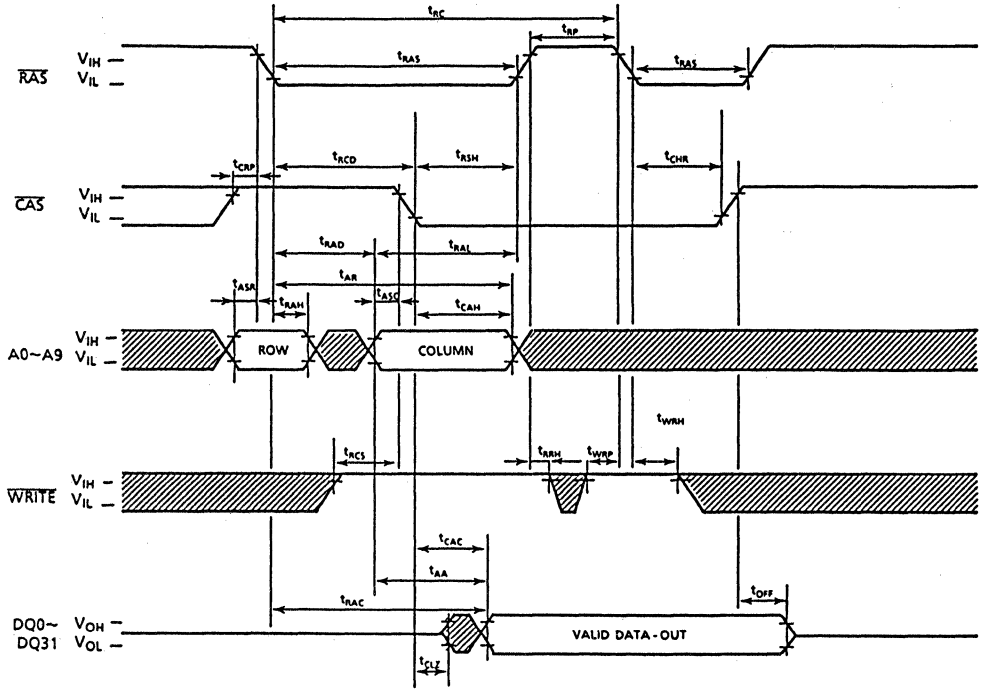
Note: $\overline{WRITE}$ = "H" or "L"

CAS BEFORE RAS REFRESH CYCLE

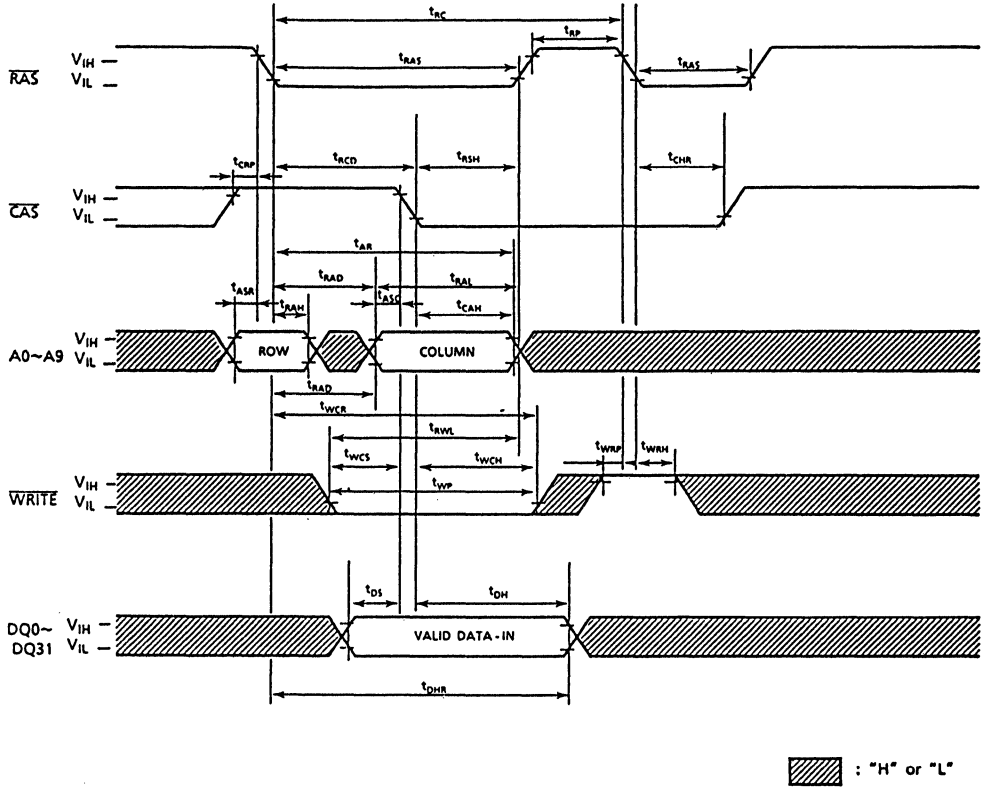


Note: A0~A9 = "H" or "L"

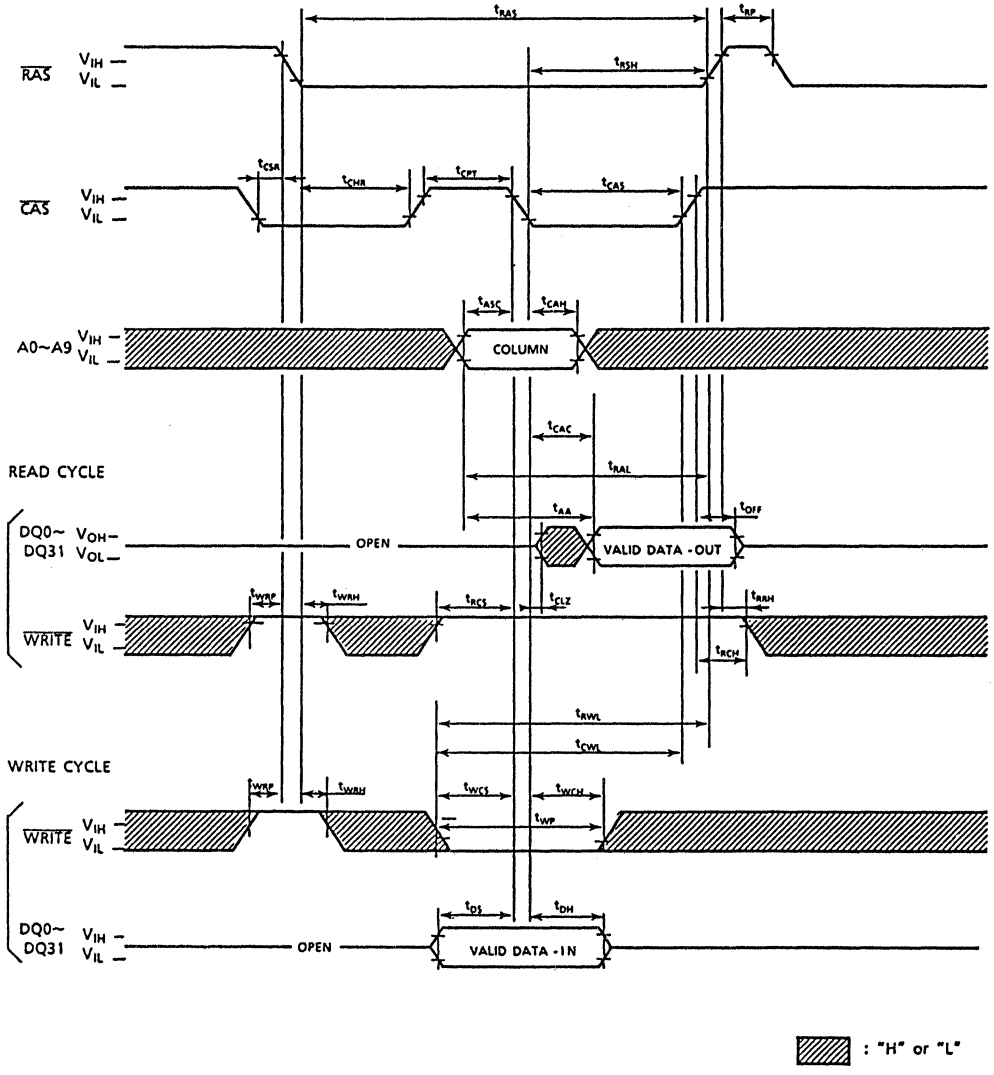
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

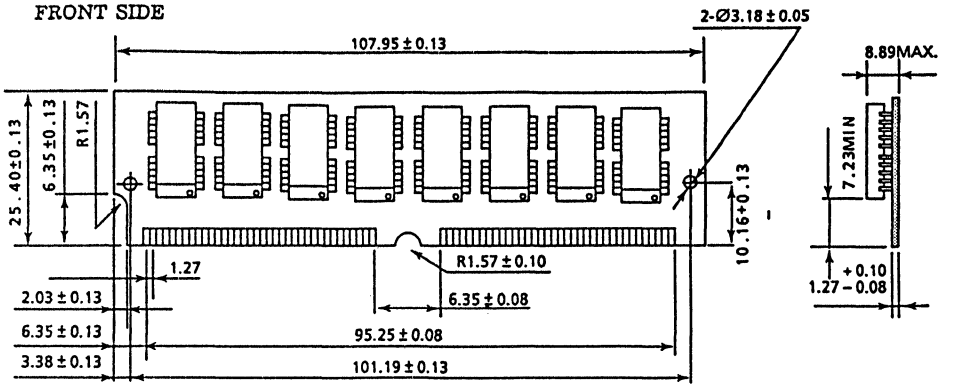


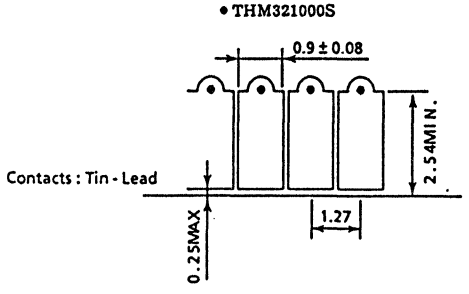
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

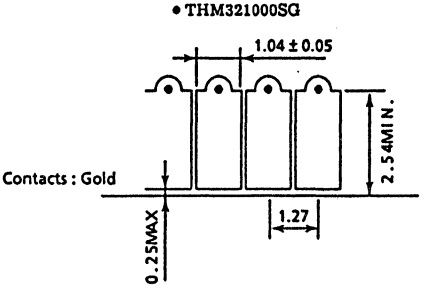


OUTLINE DRAWINGS

Unit in mm







NOTES

1,048,576 WORDS × 32 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM321020S is a 1,048,576 words by 32 bits dynamic RAM module which assembled 8 pcs of TC514400J on the printed circuit board. The THM321020S can be as well used as 2,097,152 words by 16 bits dynamic RAM module, by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ·····, DQ15 and DQ31, respectively. The THM321020S is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

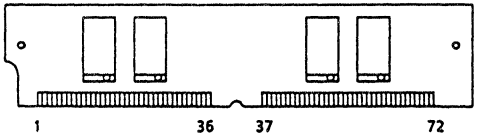
FEATURES

- 1,048,576 words by 32 bits organization
- Fast access time and cycle time

		THM321020 S-80	THM321020 S-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low power
  4,620mW MAX. Operating (THMxxxxx-80)
  3,960mW MAX. Operating (THMxxxxx-10)
  44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1024 Refresh cycles/16ms
- Tin-Lead Contact : THM321020S-80,10
- Gold Contact : THM321020SG-80,10

PIN CONNECTION (TOP VIEW)



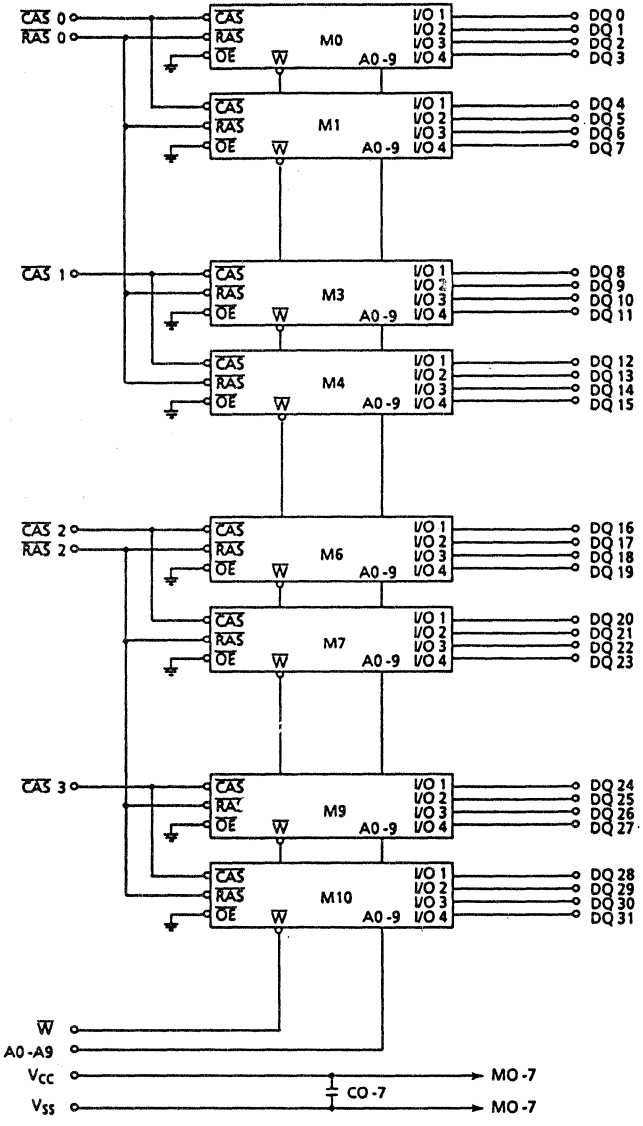
PIN NAMES

A0~A9	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	NC	45	NC	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

	-80	-10
PD0	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	NC	V_{SS}
PD3	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0~7.0	V	1
Output Voltage	V_{OUT}	-1.0~7.0	V	1
Power Supply Voltage	V_{CC}	-1.0~7.0	V	1
Operating Temperature	T_{OPR}	.0~70	°C	1
Storage Temperature	T_{STG}	-55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	THM321020S-80	–	840	mA	3, 4
		THM321020S-10	–	720		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	THM321020S-80	–	840	mA	3
		THM321020S-10	–	720		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC} = t_{PC}$ MIN.)	THM321020S-80	–	560	mA	3, 4
		THM321020S-10	–	480		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	THM321020S-80	–	840	mA	3
		THM321020S-10	–	720		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins not under Test = 0V)		–80	80	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		–10	10	µA	
I_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = –5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM321020S-80		THM321020S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THM321020S-80		THM321020S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	ns	
t_{DS}	Date Set-Up Time	0	–	0	–	ns	11
t_{DH}	Date Hold Time	15	–	20	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

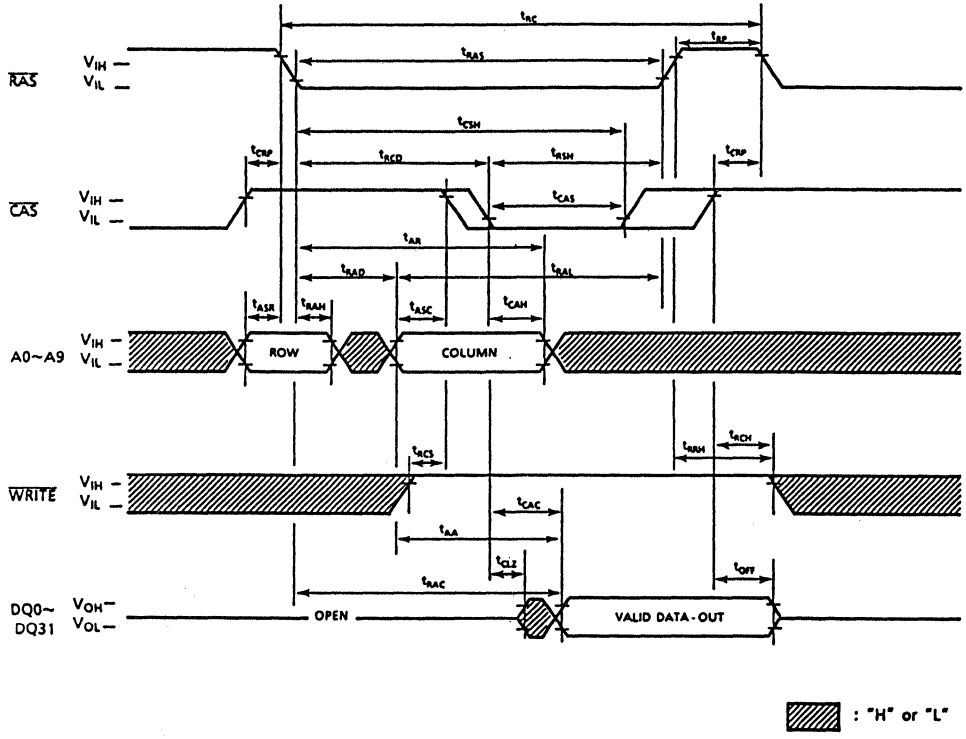
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A9)	–	88	pF
CI2	Input Capacitance ($\overline{W}$)	–	84	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	–	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	–	36	pF
CDQ1	I/O Capacitance (DQ0~31)	–	17	pF

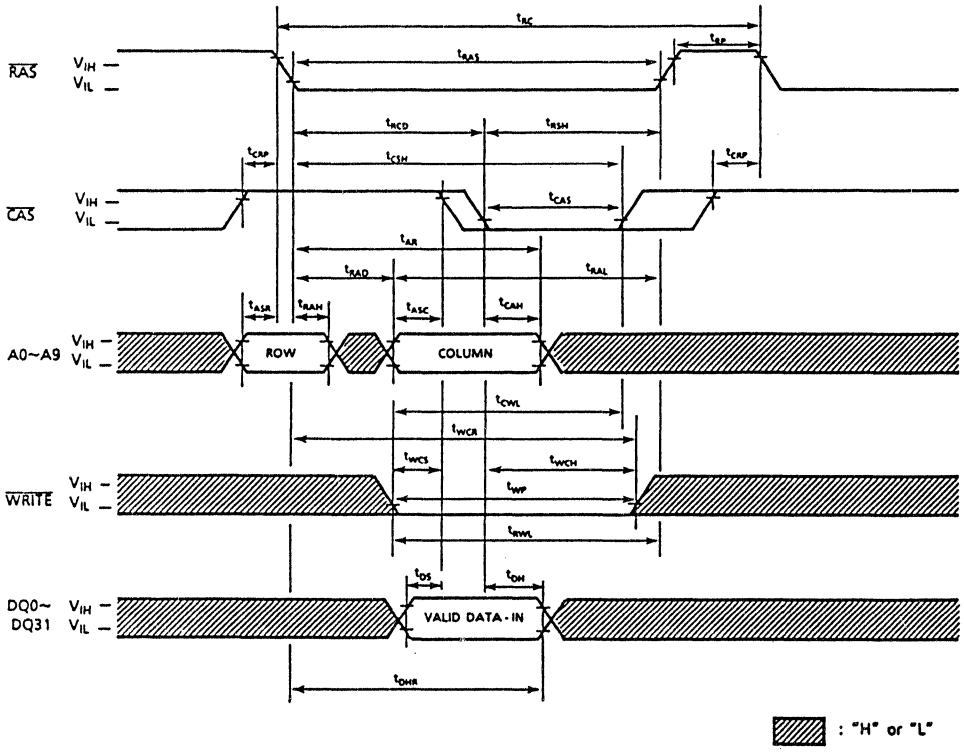
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5ns$.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

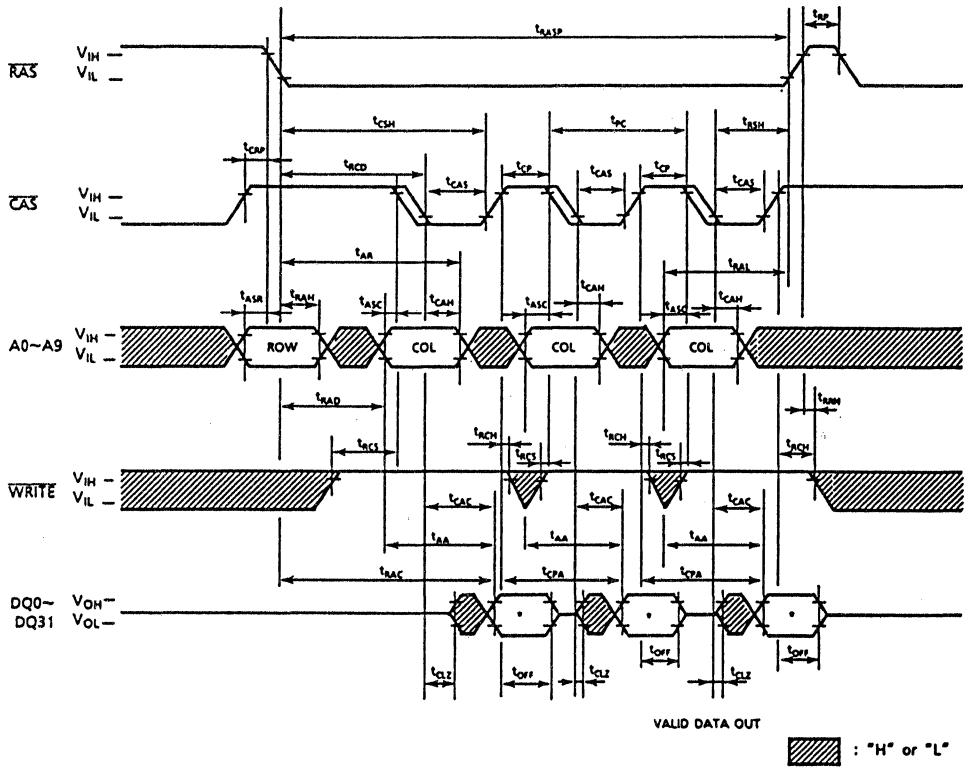
READ CYCLE


RAS
CAS
A0~A9
WRITE
DQ0~DQ31
VIH
VIL
VOH
VOL
ROW
COLUMN
OPEN
VALID DATA-OUT
: "H" or "L"

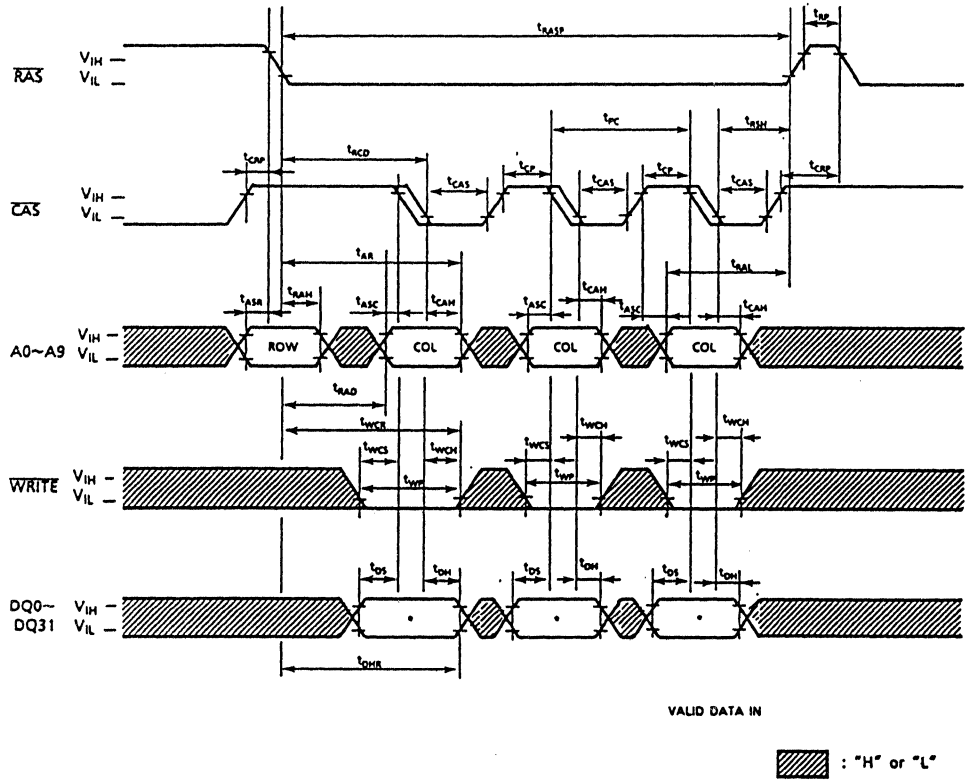
EARLY WRITE CYCLE



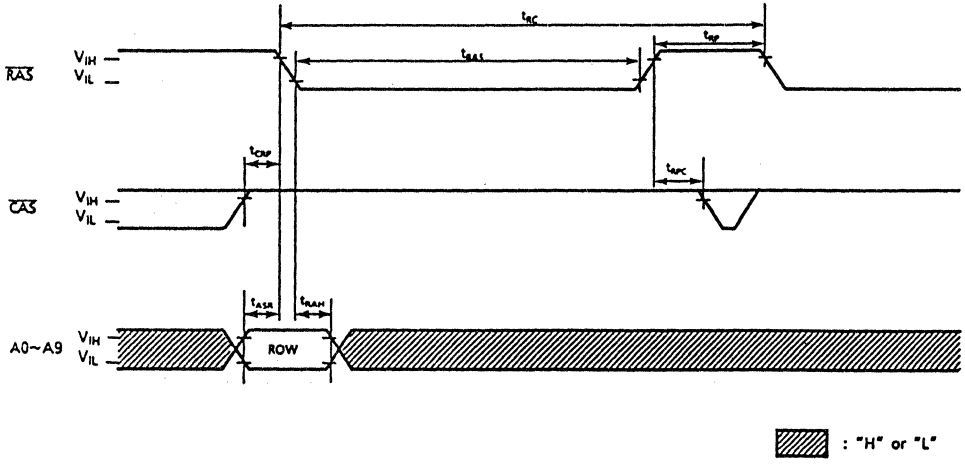
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

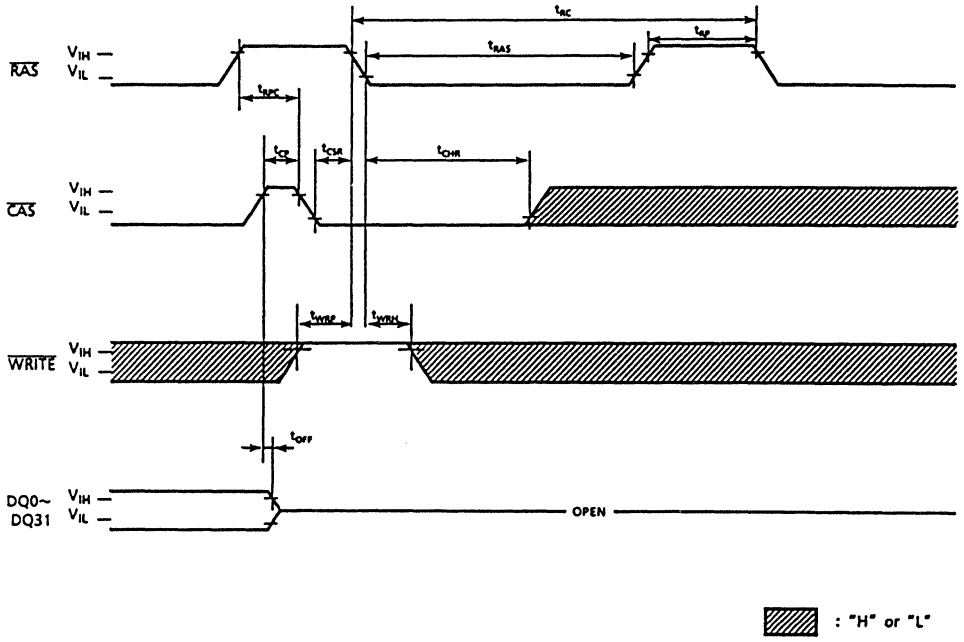


$\overline{RAS}$ ONLY REFRESH CYCLE



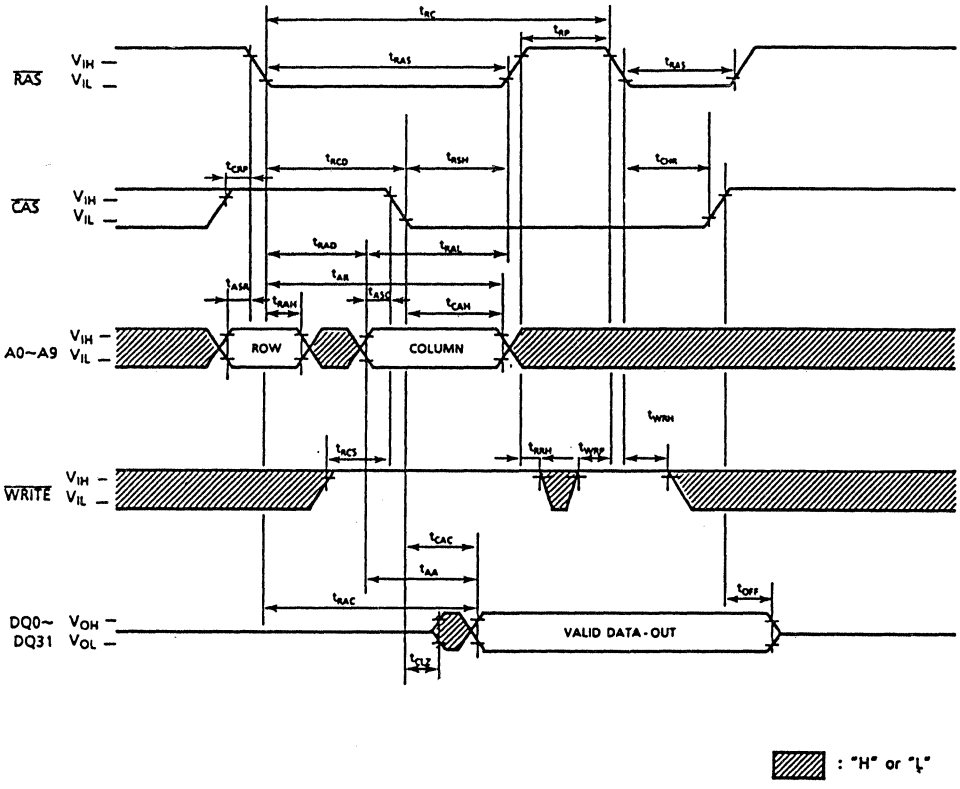
Note: $\overline{WRITE}$ = "H" or "L"

CAS BEFORE RAS REFRESH CYCLE

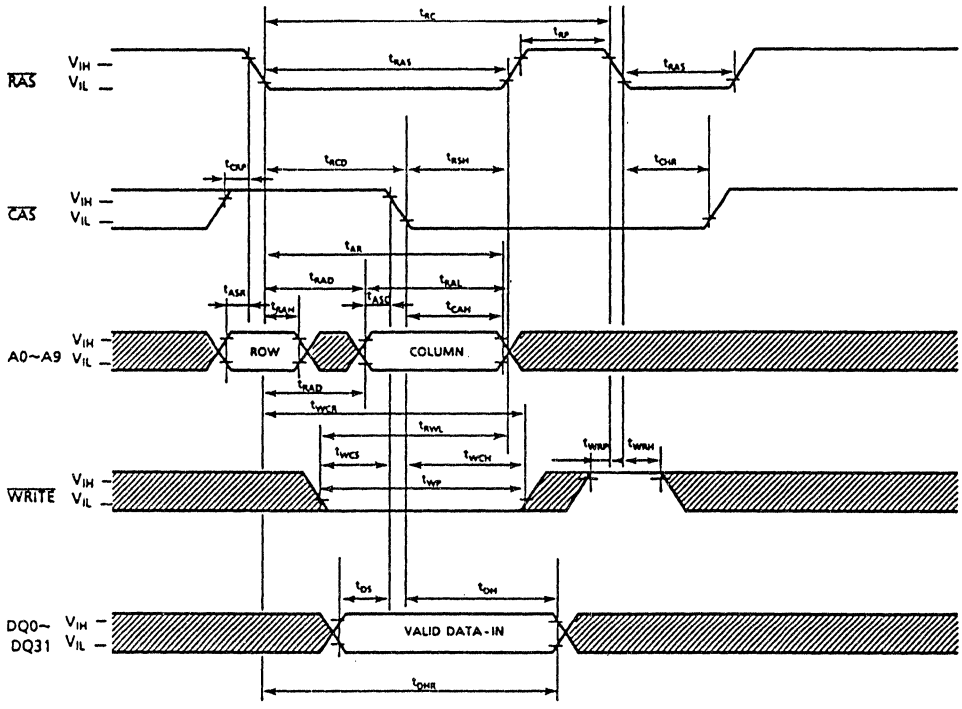


Note: A0~A9 = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

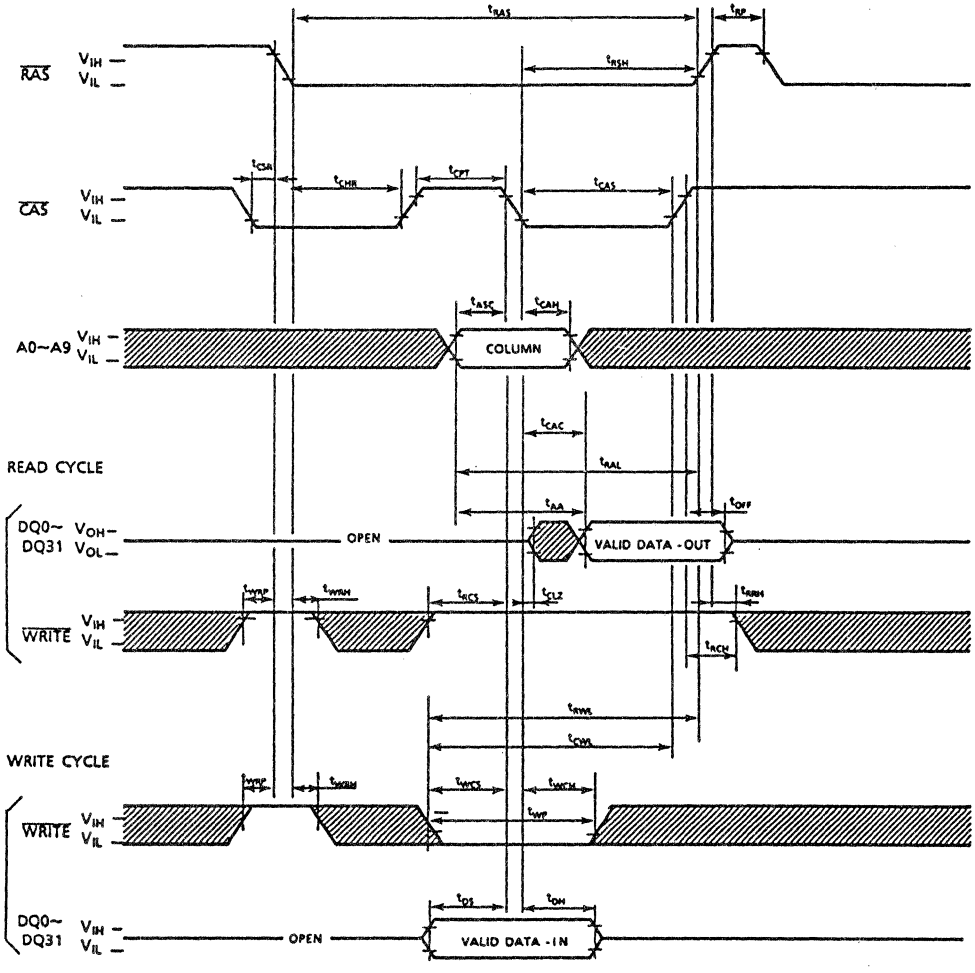


HIDDEN REFRESH CYCLE (WRITE)



: "H" or "L"

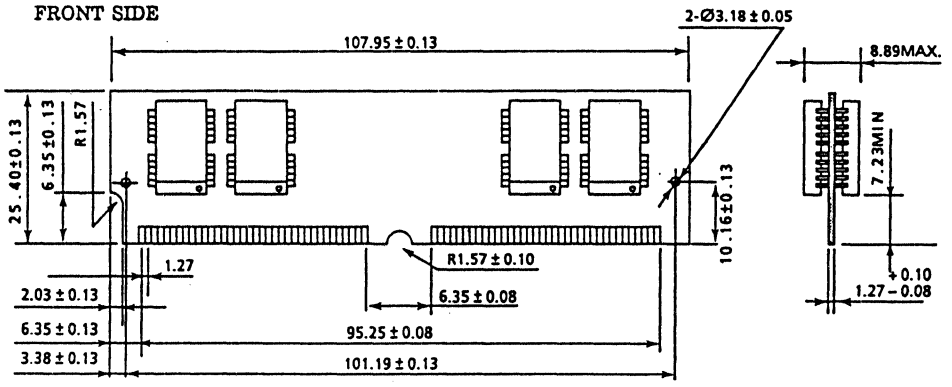
CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



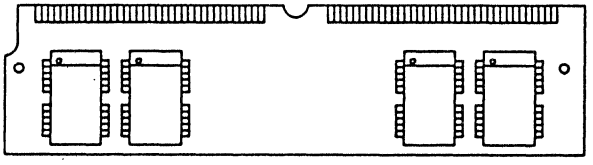
OUTLINE DRAWINGS

Unit in mm

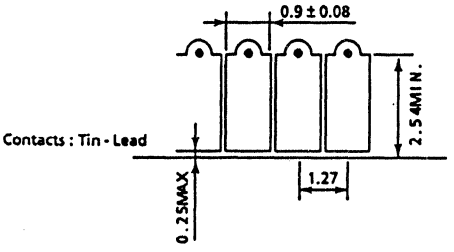
FRONT SIDE



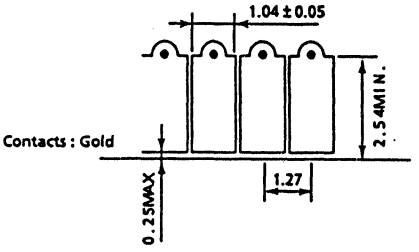
BACK SIDE



• THM321020S



• THM321020SG



NOTES

4,194,304 WORDS × 9 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM94000S/L is a 4,194,304 words by 9 bits dynamic RAM module which assembled 9 pcs of TC514100J on the printed circuit board.

The THM94000S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

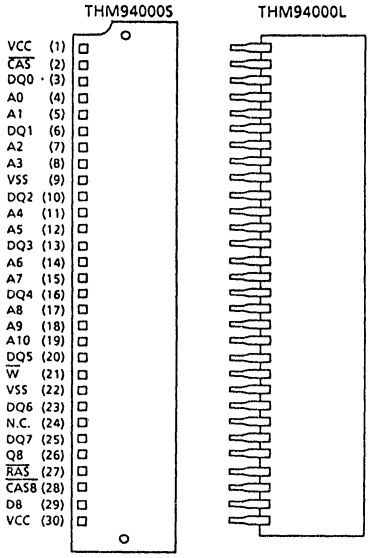
FEATURES

- 4,194,304 words by 9 bits organization
- Fast access time

		THM94000S/L-80	THM94000S/L-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low power 4,950mW MAX. Operating (THM94000S/L-80)
  4,212mW MAX. Operating (THM94000S/L-10)
  49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1,024 refresh cycles/16ms

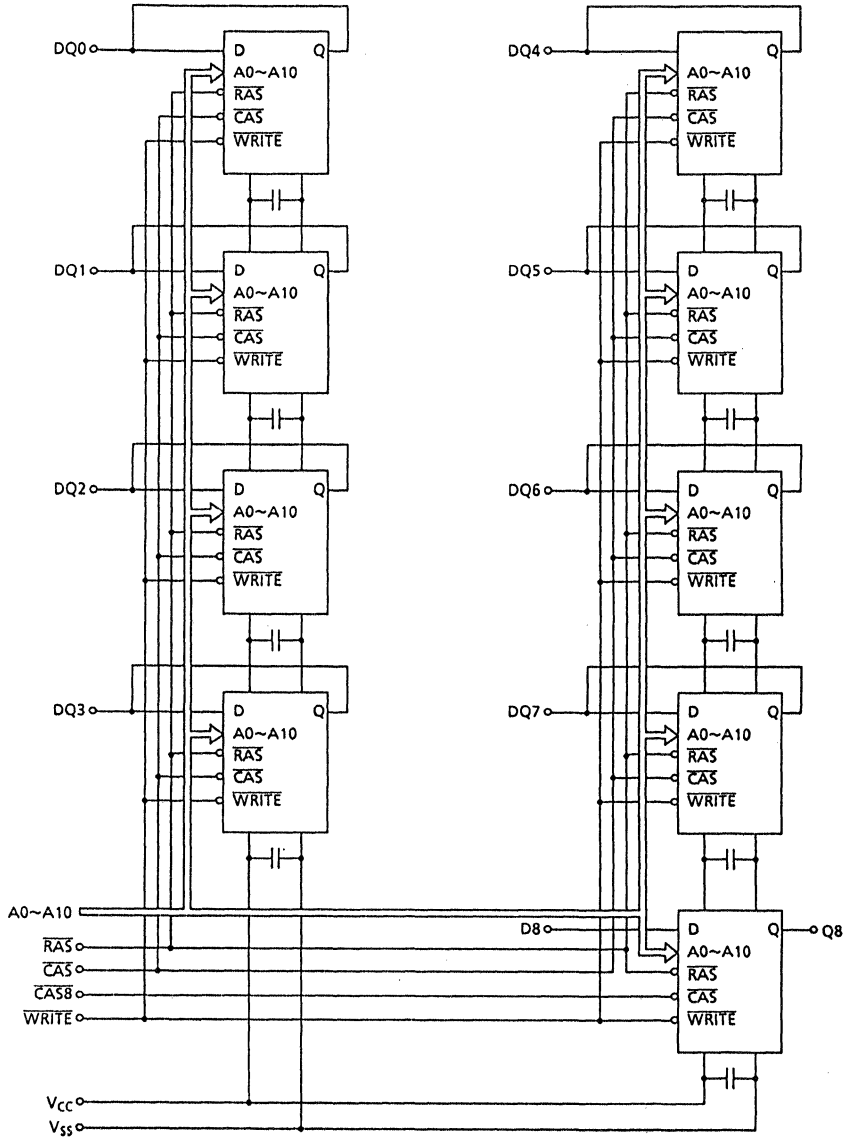
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A10	Address Inputs
DQ0~DQ7	Data Inputs/Outputs
D8	Data Inputs
Q8	Data Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxxx−80	–	900	mA	3, 4
		THMxxxxxx−10	–	765		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ V_{IH}: t_{RC} = t_{RC} MIN.)	THMxxxxxx−80	–	900	mA	3
		THMxxxxxx−10	–	765		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} MIN.)	THMxxxxxx−80	–	540	mA	3, 4
		THMxxxxxx−10	–	450		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		–	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxxx−80	–	900	mA	3
		THMxxxxxx−10	–	765		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins not under Test = 0V)		−90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		−20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = 5 − mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM94000S-80		THM94000S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	THM94000S-80		THM94000S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	11
t_{DH}	Data Hold Time	15	–	20	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

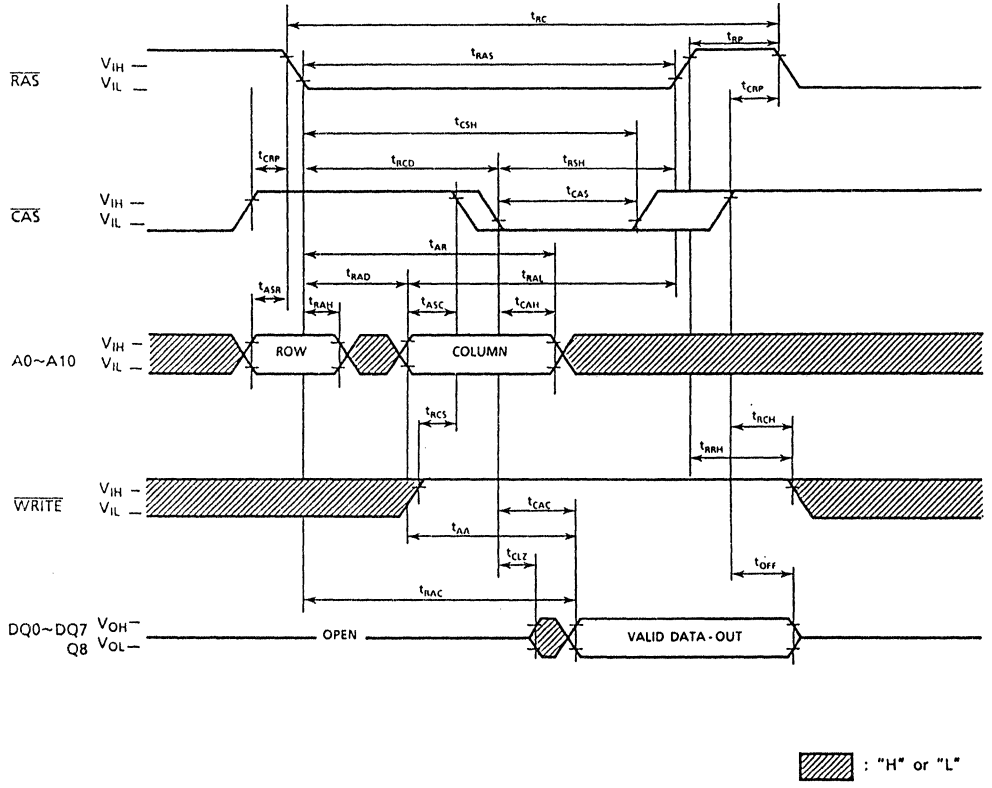
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{I2}	Input Capacitance (D8, $\overline{CAS8}$)	–	10	pF
C_{DQ}	I/O Capacitance (DQ0~DQ7)	–	15	pF
C_Q	Output Capacitance (Q8)	–	10	pF

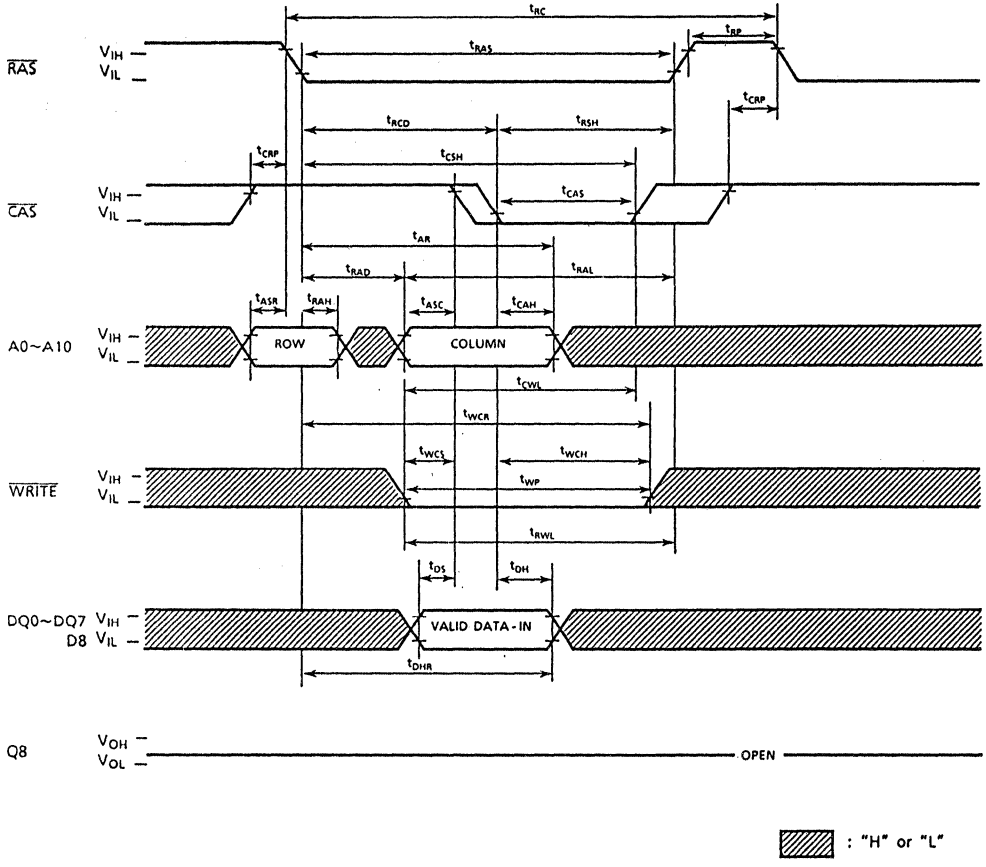
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

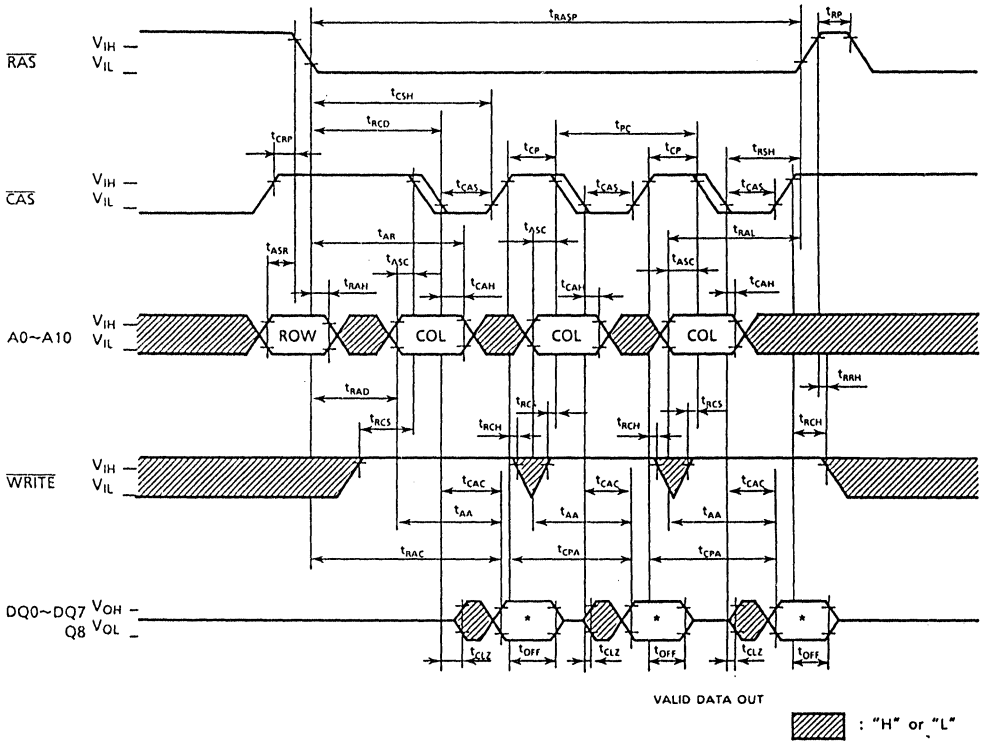
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCRP
tCSH
tCRP
tRCD
tRSH
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A10
VIH
VIL
ROW
COLUMN
tRCS
tRCH
tARH
WRITE
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DQ0~DQ7
Q8
VOH
VOL
OPEN
VALID DATA-OUT
: "H" or "L"

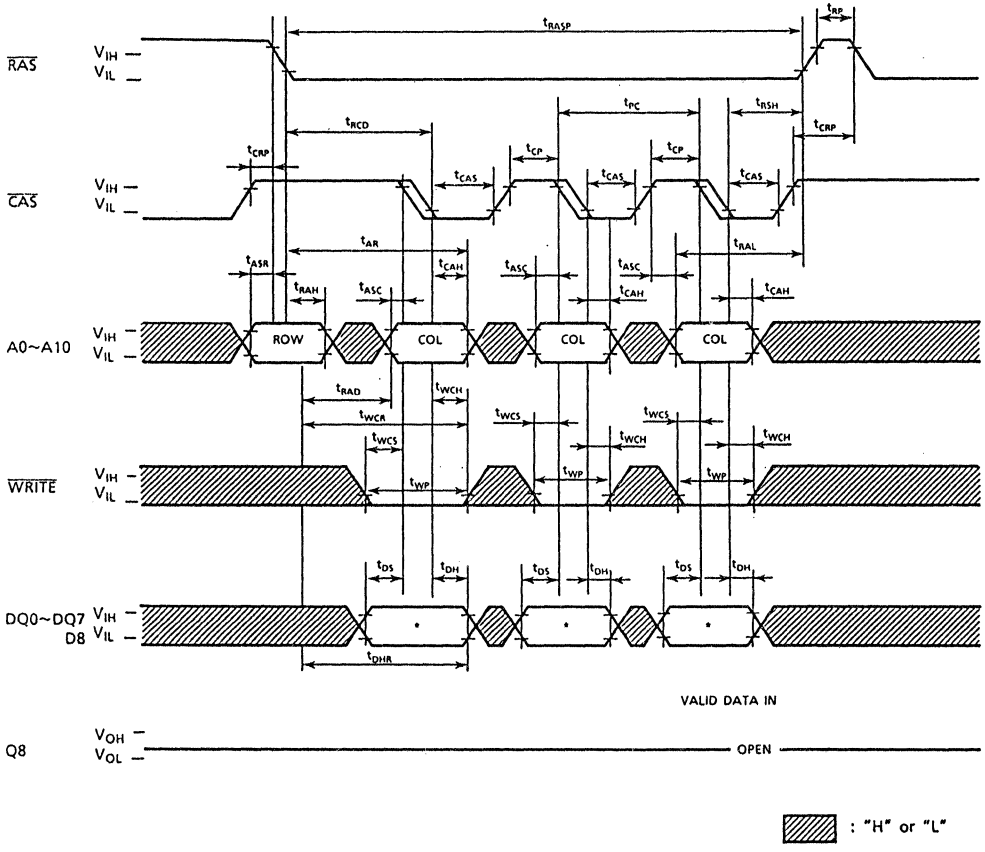
EARLY WRITE CYCLE



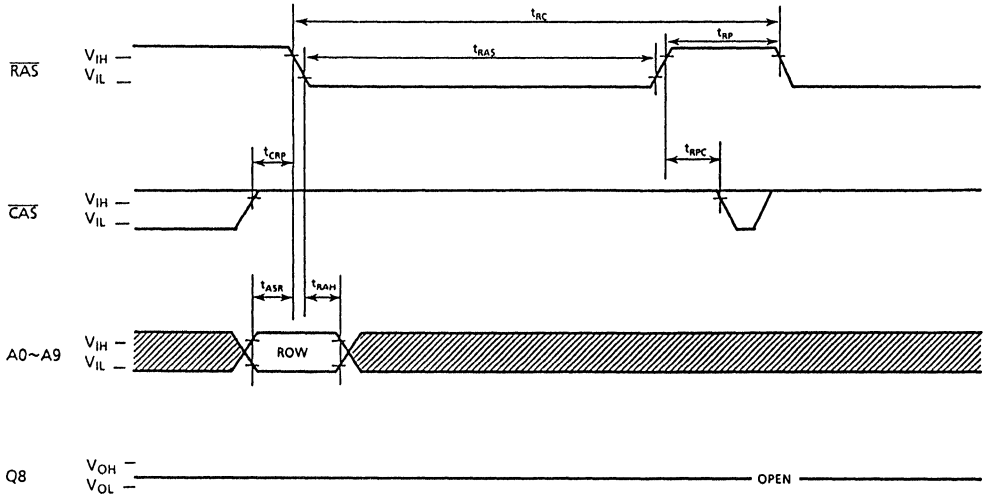
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



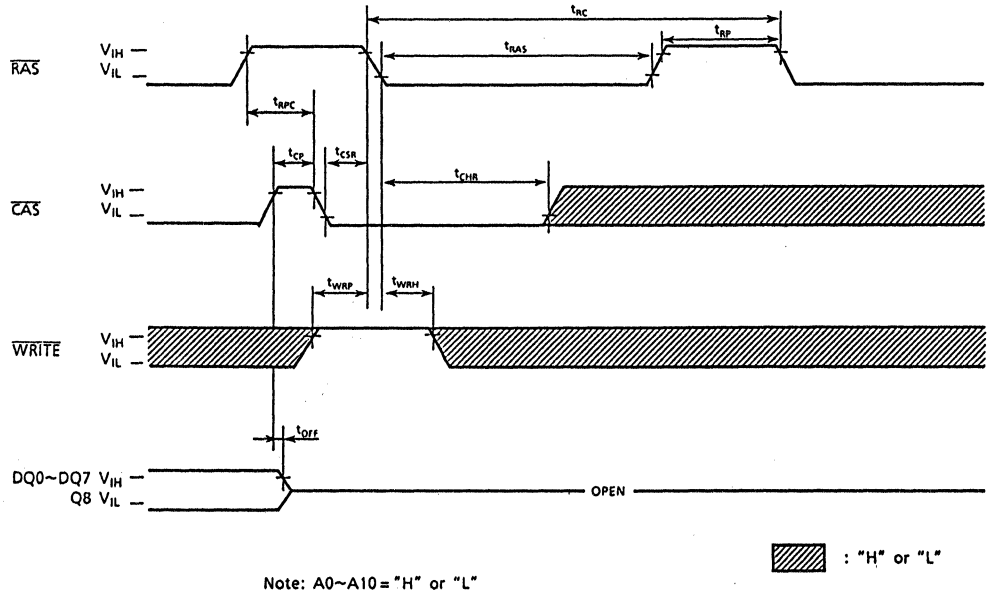
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, A10 = "H" or "L"

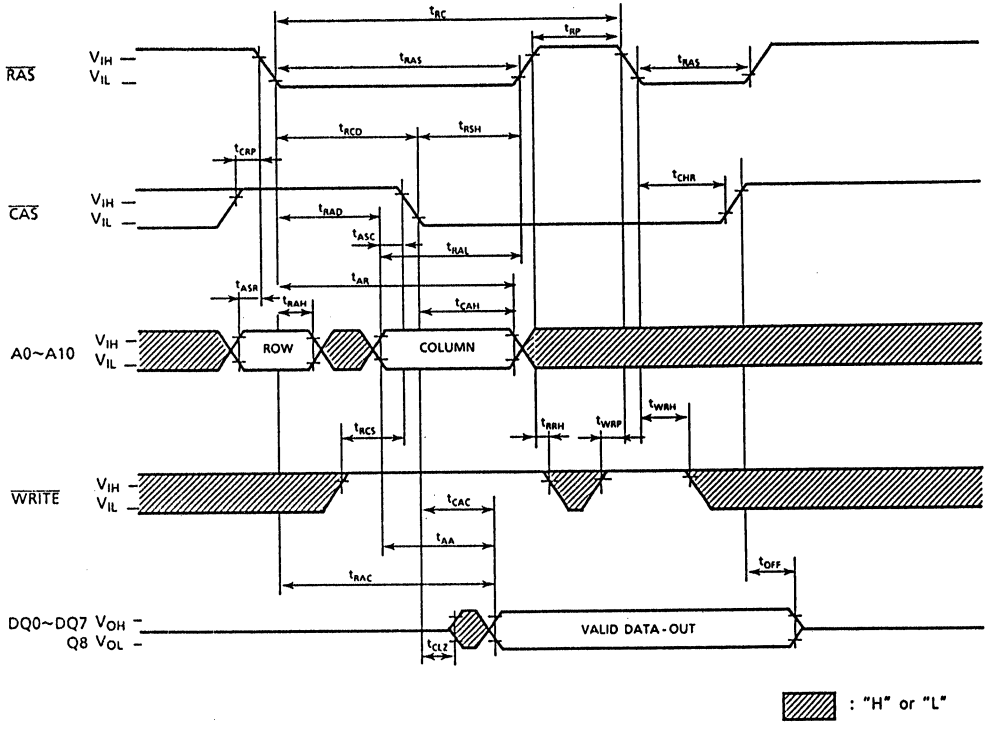
: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

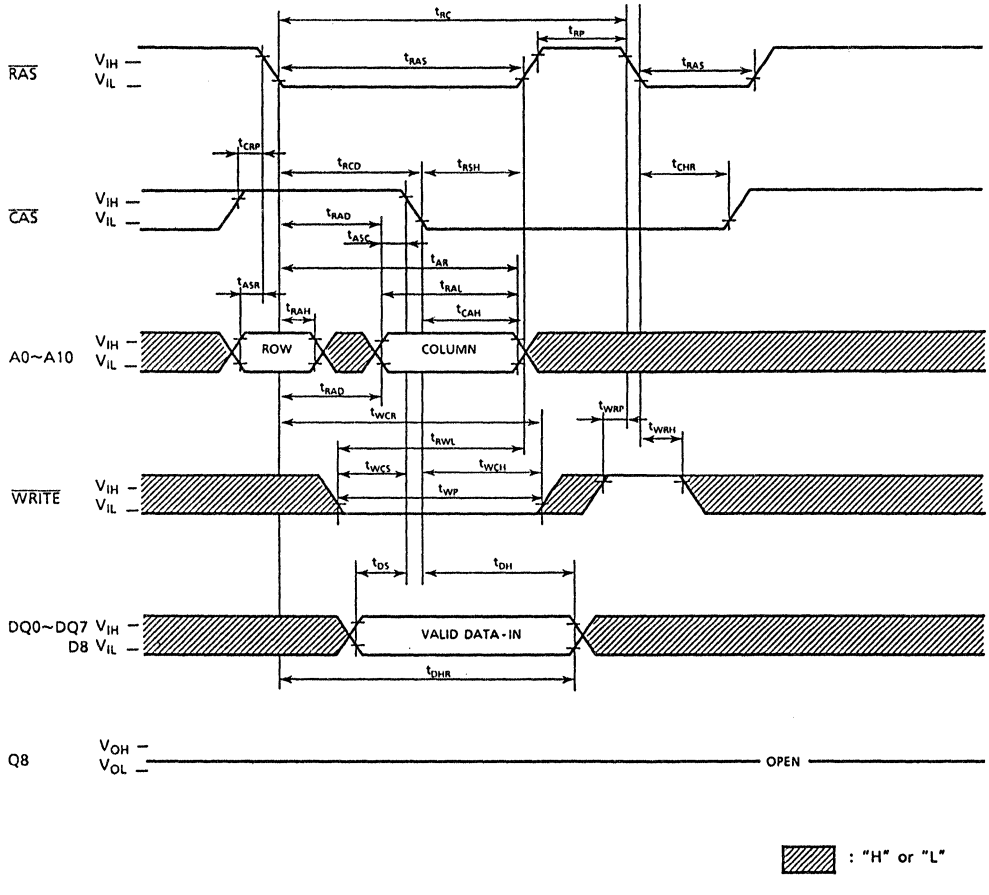


Note: A0~A10 = "H" or "L"

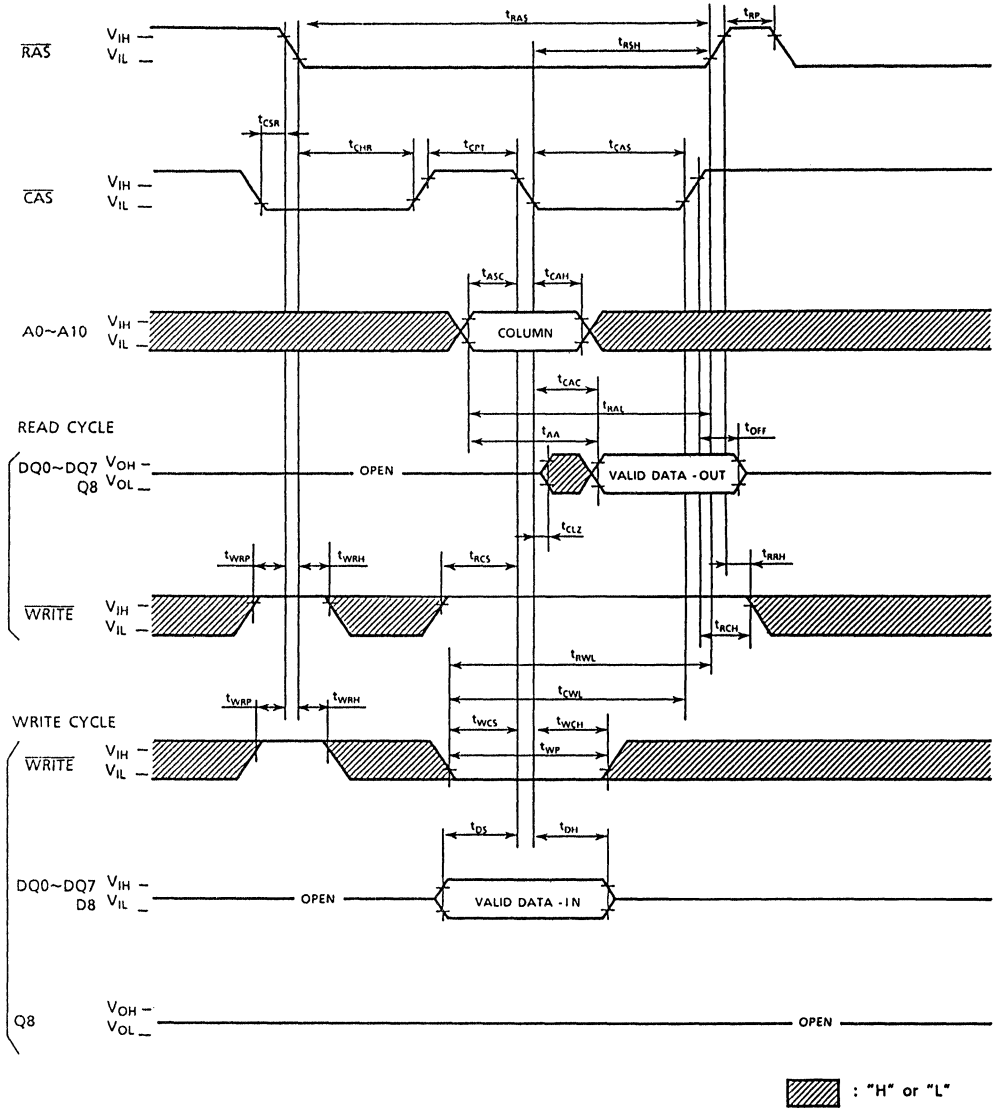
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



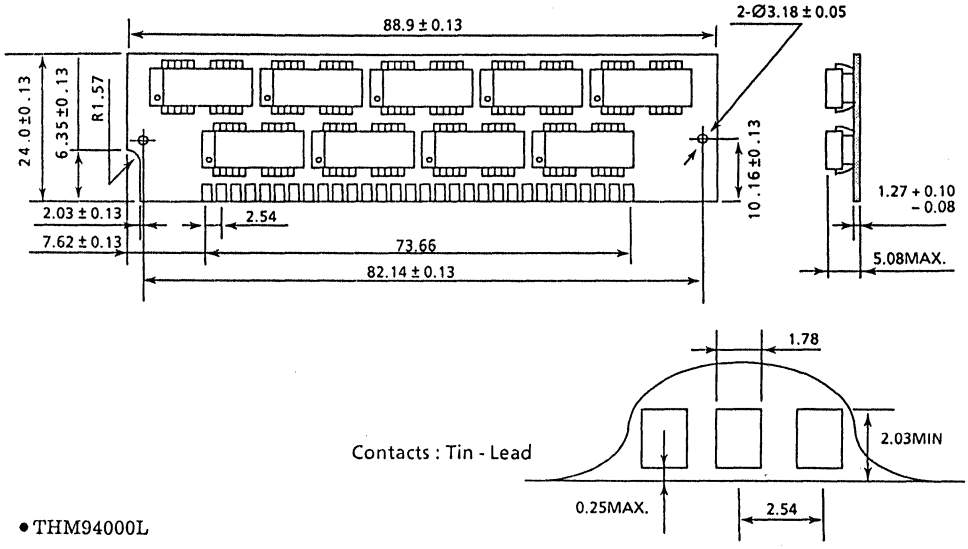
CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



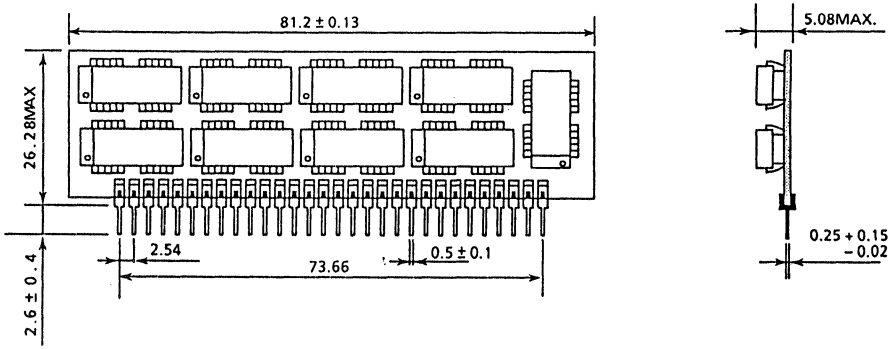
OUTLINE DRAWINGS

Unit in mm

• THM94000S



• THM94000L



1,048,576 WORDS×36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM361020S is a 1,048,576 words by 36 bits dynamic RAM module which assembled 8 pcs of TC514400J and 4 pcs of TC511000AJ on the printed circuit board. The THM361020S can be as well used as 2,097,152 words by 18 bits dynamic RAM module, by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ·····, DQ17 and DQ35, respectively. The THM361020S is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

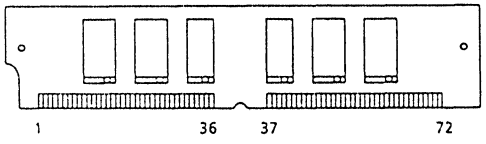
FEATURES

- 1,048,576 words by 36 bits organization
- Fast access time and cycle time

		THM361020 S-80	THM361020 S-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low power
  6,160mW MAX. Operating (THMxxxxxx-80)
  5,280mW MAX. Operating (THMxxxxxx-10)
  66mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1024 Refresh cycles/ 8ms (Burst Refresh)
- 1024 Refresh cycles/16ms (Distributed Refresh)
- Tin-Lead Contact : THM361020S-80,10
- Gold Contact : THM361020SG-80,10

PIN CONNECTION (TOP VIEW)



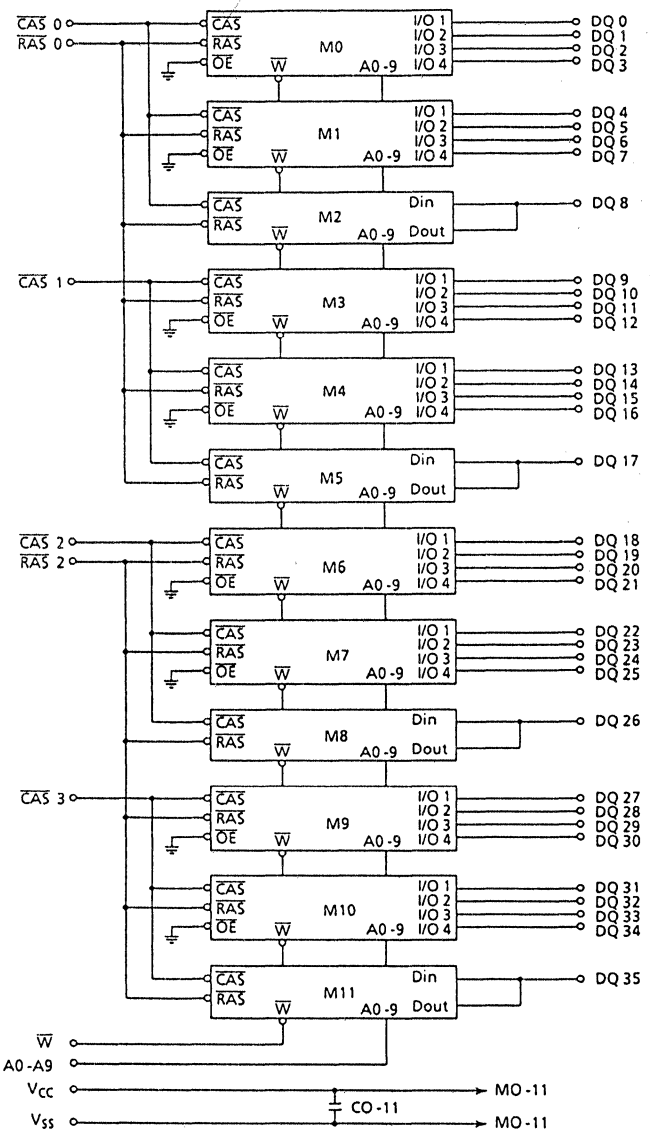
PIN NAMES

A0~A9	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

	-80	-10
PD0	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	NC	V_{SS}
PD3	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	7.2	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THM361020S-80	–	1120	mA	3, 4
		THM361020S-10	–	960		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	24	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	THM361020S-80	–	1120	mA	3
		THM361020S-10	–	960		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} MIN.)	THM361020S-80	–	760	mA	3, 4
		THM361020S-10	–	640		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	12	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THM361020S-80	–	1120	mA	3
		THM361020S-10	–	960		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins not under Test = 0V)		– 120	120	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
I_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM361020S-80		THM361020S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THM361020S-80		THM361020S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	ns	
t_{DS}	Date Set-Up Time	0	–	0	–	ns	11
t_{DH}	Date Hold Time	15	–	20	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

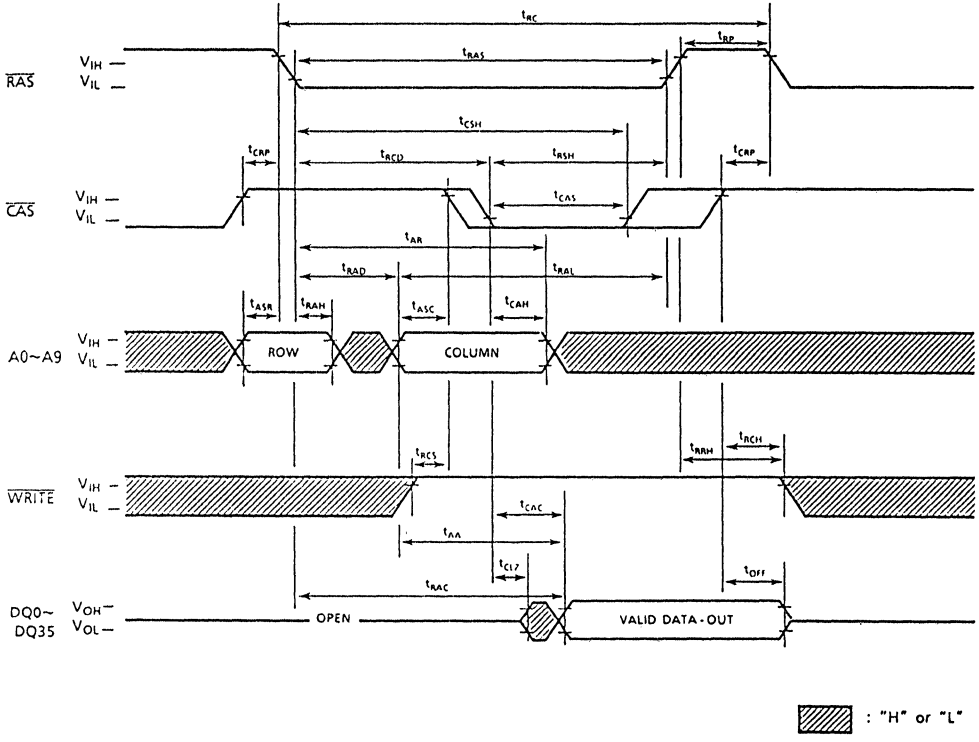
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A9)	–	88	pF
CI2	Input Capacitance ($\overline{W}$)	–	84	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	–	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	–	36	pF
CDQ1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	–	17	pF
CDQ2	I/O Capacitance (DQ8, 17, 26, 35)	–	22	pF

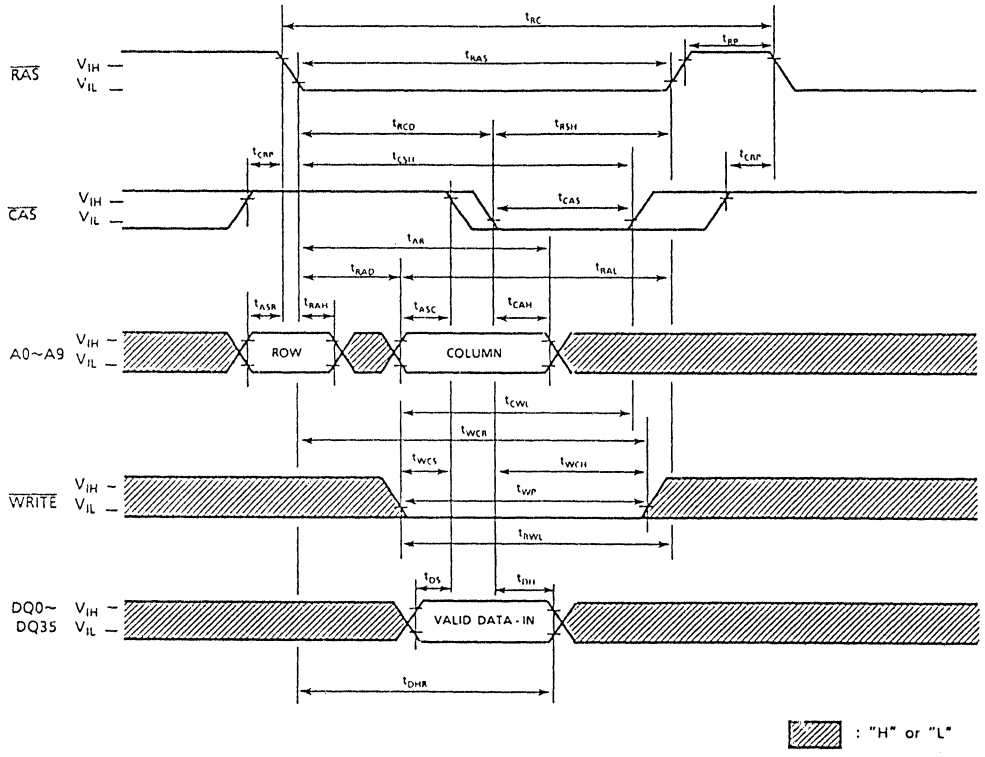
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5ns$.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
    t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met.
    t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

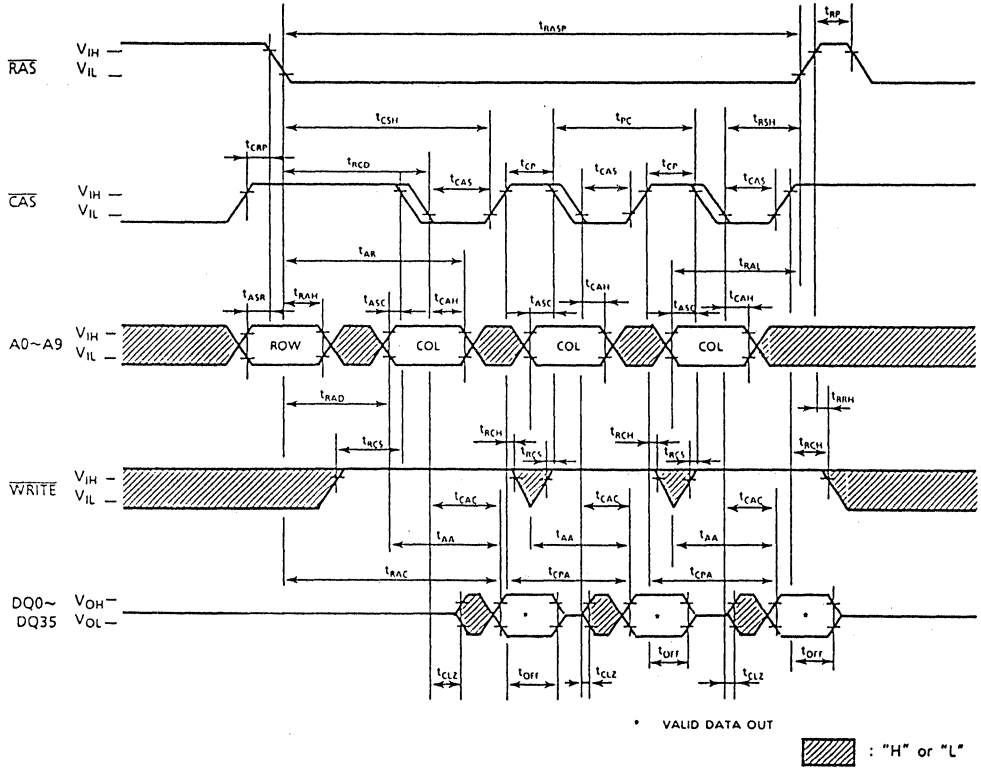
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tCAC
tAA
tCLZ
tOFF
tRAC
DQ0~
DQ35
VOH
VOL
OPEN
VALID DATA-OUT
: "H" or "L"

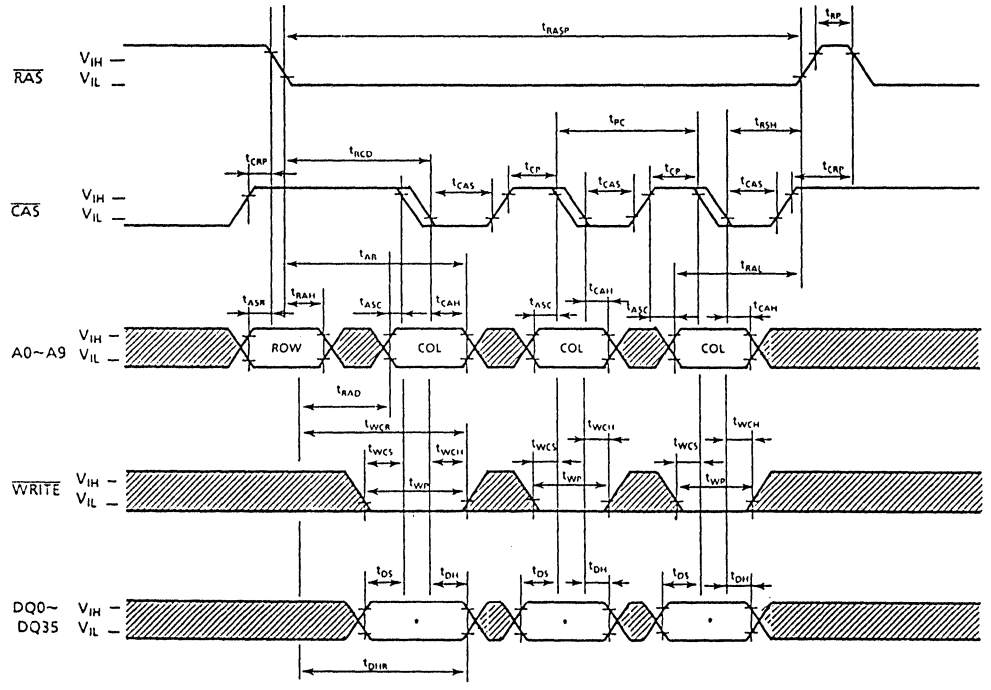
EARLY WRITE CYCLE



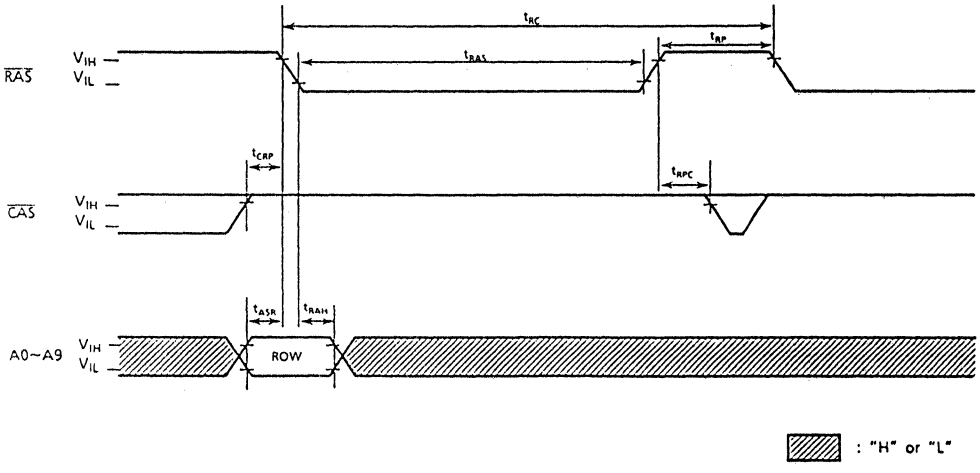
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

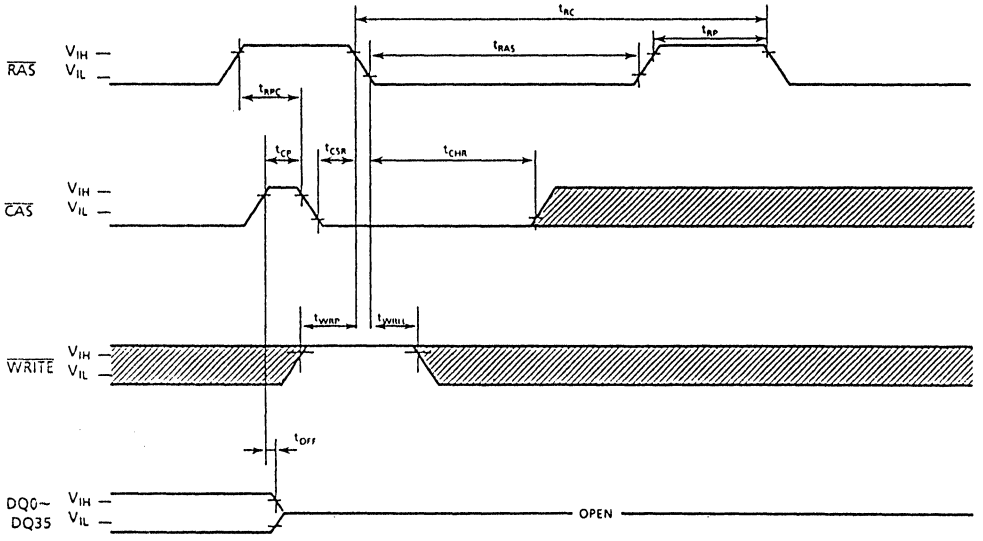


$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$ = "H" or "L"

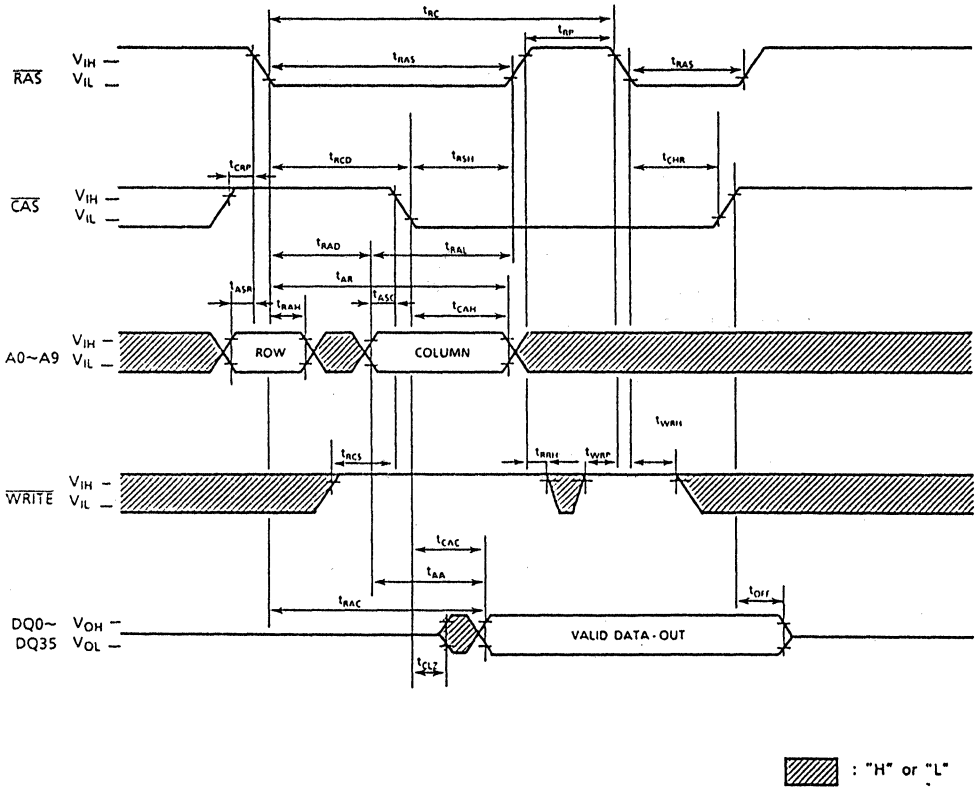
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



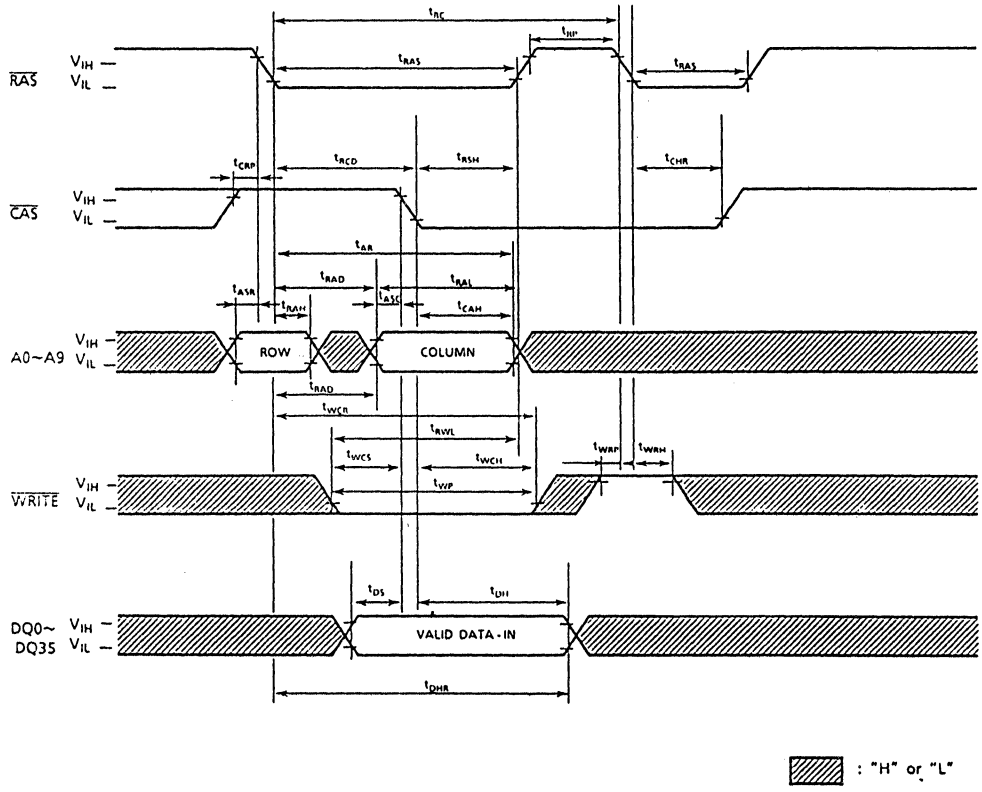
: "H" or "L"

Note: A0~A9 = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

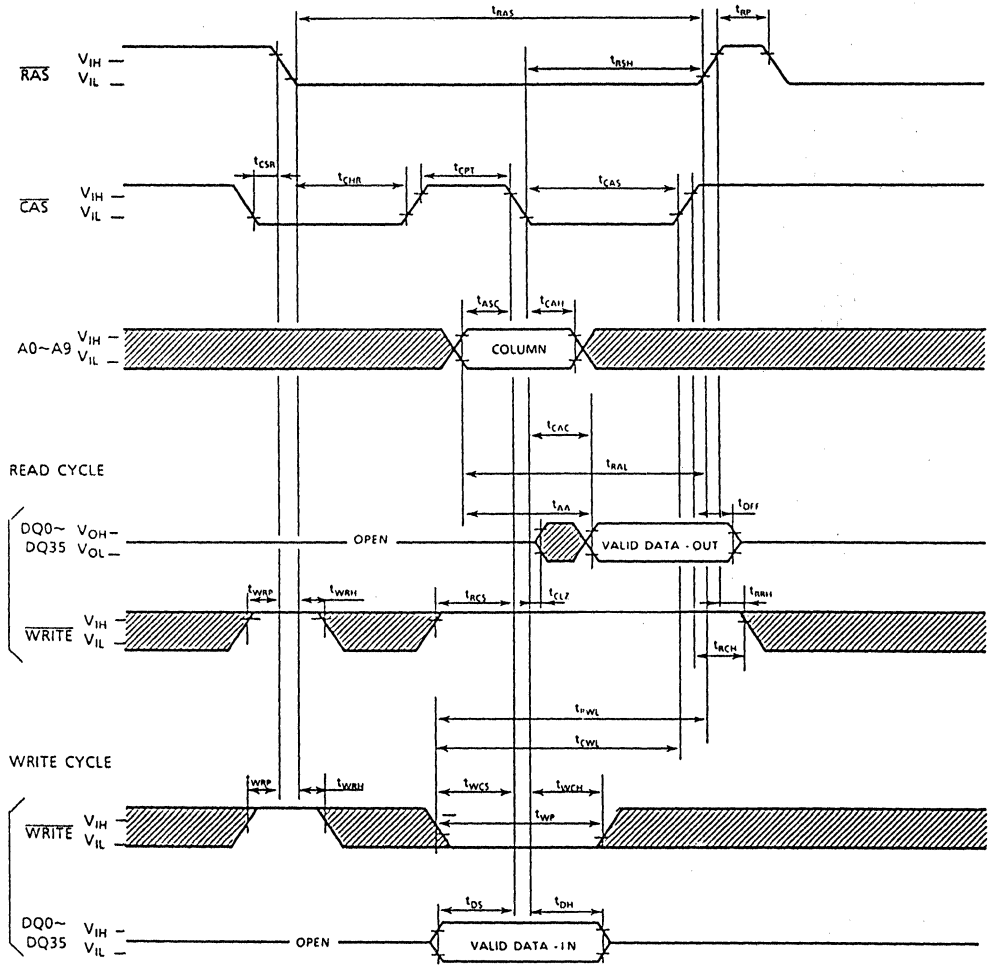


HIDDEN REFRESH CYCLE (WRITE)



: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

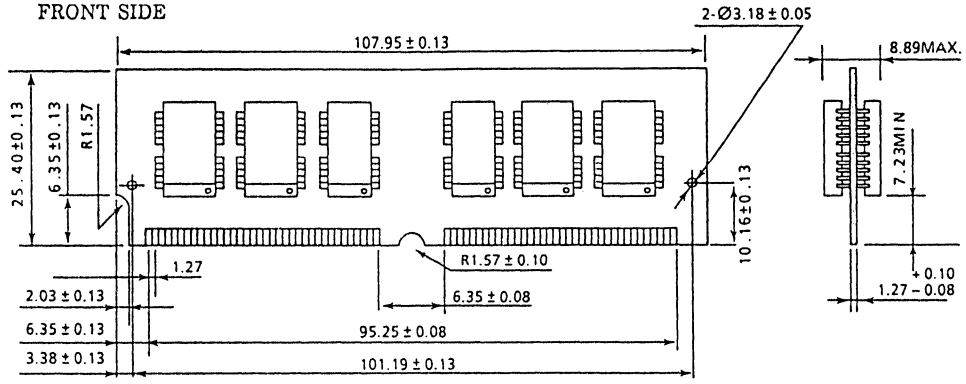


: "H" or "L"

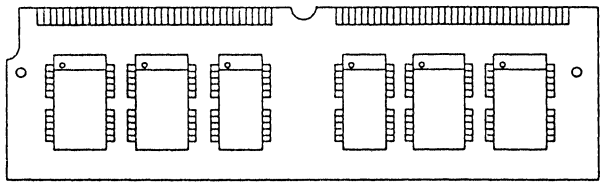
OUTLINE DRAWINGS

Unit in mm

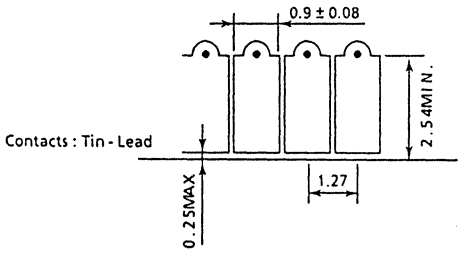
FRONT SIDE



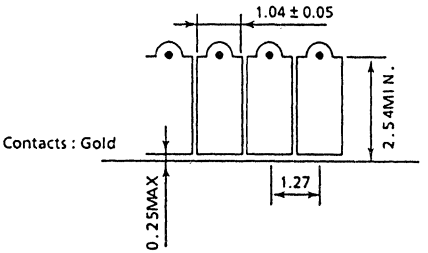
BACK SIDE



• THM361020S



• THM361020SG



NOTES

1,048,576 WORDS×40 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM401020SG is a 1,048,576 words by 40 bits dynamic RAM module which assembled 10 pcs of TC514400J on the printed circuit board.

The THM401020SG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

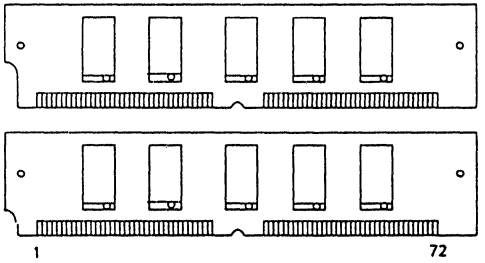
FEATURES

- 1,048,576 words by 40 bits organization
- Fast access time and cycle time

		THM401020 SG-80	THM401020 SG-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low power
  5,775mW MAX. Operating (THMxxxxxx-80)
  4,950mW MAX. Operating (THMxxxxxx-10)
  55mW MAX. Standby
- Read-Modify-write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1024 Refresh cycles/16ms
- Gold Contact
- JEDEC OUTLINE : THM401020SG-80, 10
- NON JEDEC OUTLINE : THM401040SG-80, 10

PIN CONNECTION (TOP VIEW)



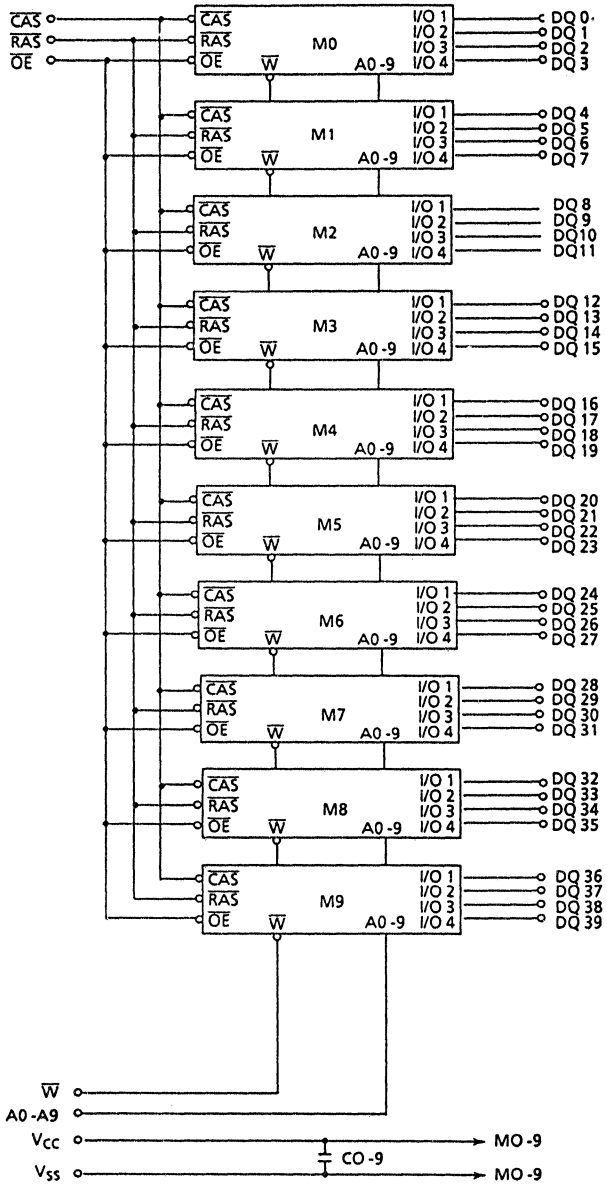
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	NC	55	DQ28	67	PD0
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS}$	56	DQ29	68	PD1
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD2
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD3
11	NC	23	DQ11	35	DQ17	47	$\overline{W}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	V_{SS}	60	DQ32	72	V_{SS}

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ39	Data Inputs/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

	-80	-10
PD0	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	NC	V_{SS}
PD3	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0~7.0	V	1
Output Voltage	V_{OUT}	-1.0~7.0	V	1
Power Supply Voltage	V_{CC}	-1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~125	°C	1
Soldering Temperature·Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	6.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	THM401020SG-80	–	1050	mA	3,4,5
		THM401020SG-10	–	900		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	20	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	THM401020SG-80	–	1050	mA	3,5
		THM401020SG-10	–	900		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC} = t_{PC}$ MIN.)	THM401020SG-80	–	700	mA	3,4,5
		THM401020SG-10	–	600		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	10	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	THM401020SG-80	–	1050	mA	3
		THM401020SG-10	–	900		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins not under Test = 0V)		– 100	100	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM401020 SG-80		THM401020 SG-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	205	–	245	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	105	–	125	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THM401020 SG-80		THM401020 SG-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	70	–	85	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	75	–	90	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	25	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

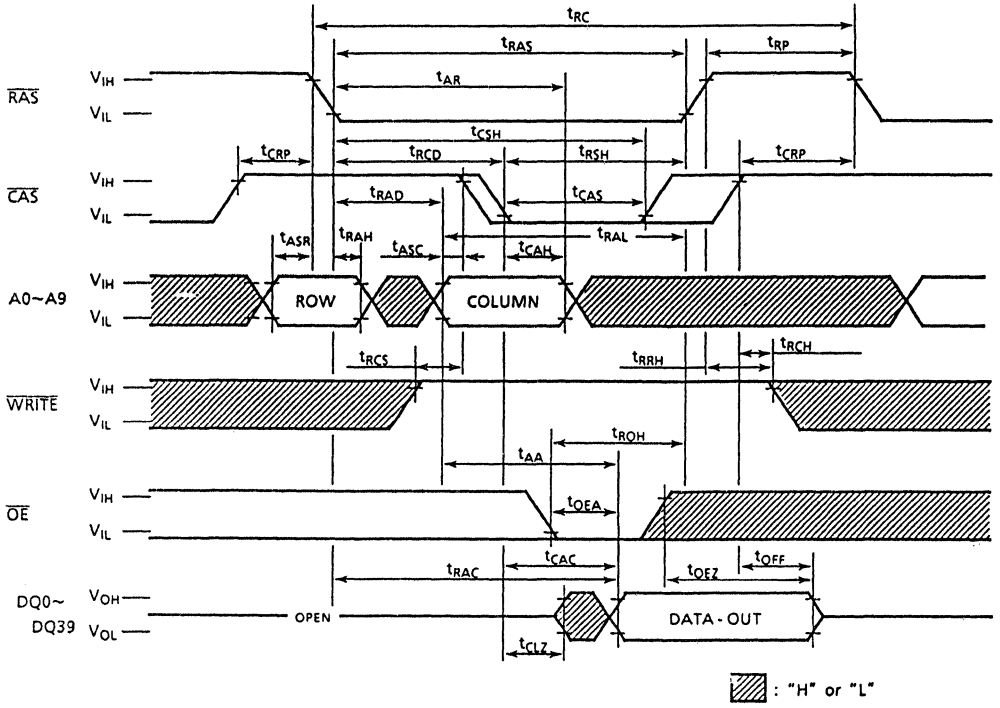
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A9)	-	65	pF
CI2	Input Capacitance ($\overline{W}$, $\overline{OE}$)	-	65	pF
CI3	Input Capacitance ($\overline{RAS}$)	-	50	pF
CI4	Input Capacitance ($\overline{CAS}$)	-	60	pF
CDQ	I/O Capacitance (DQ0~DQ39)	-	17	pF

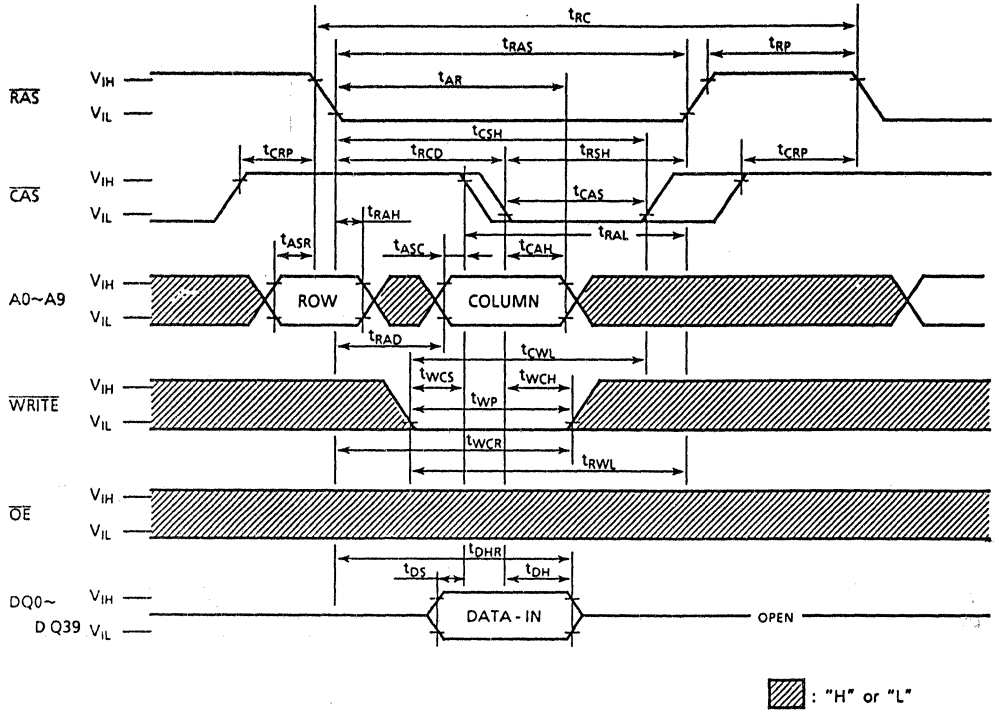
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified value are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

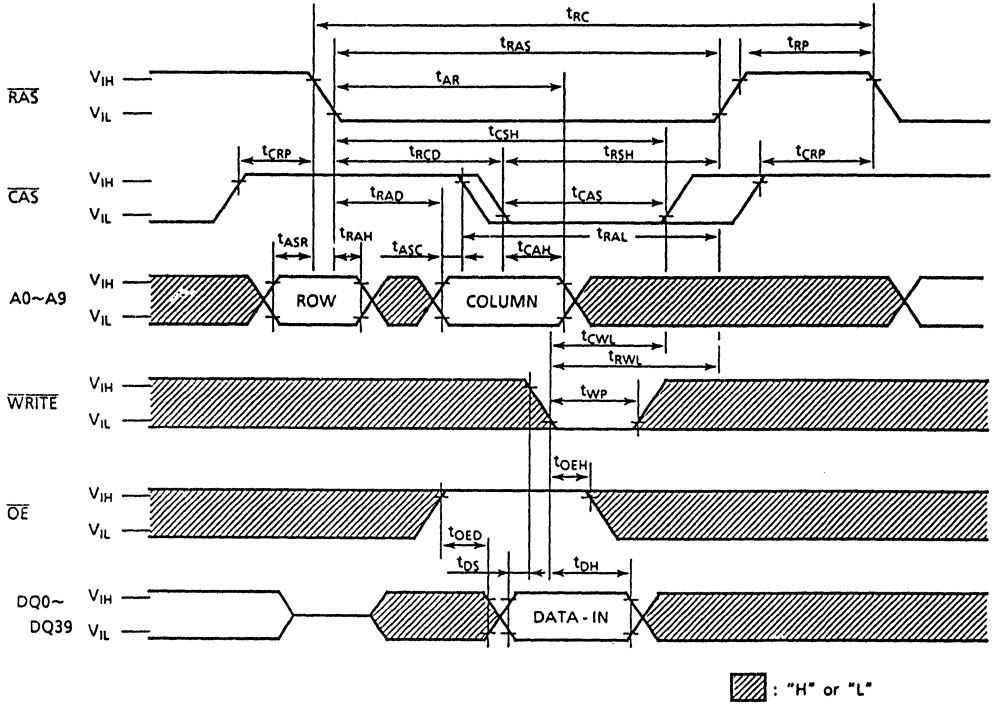
READ CYCLE


tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tRAD
tCAS
tASR
tRAH
tASC
tCAH
tRAL
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tROH
tAA
OE
tOEA
tCAC
tOFF
tRAC
tOEZ
DQ0~
DQ39
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

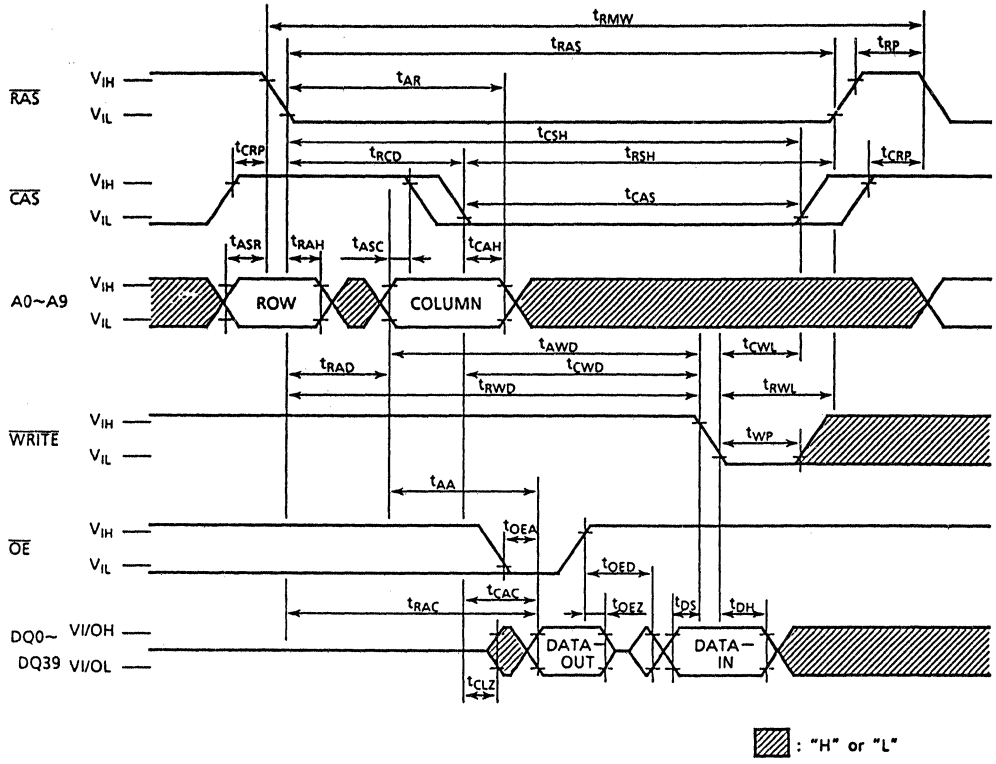
WRITE CYCLE (EARLY WRITE)



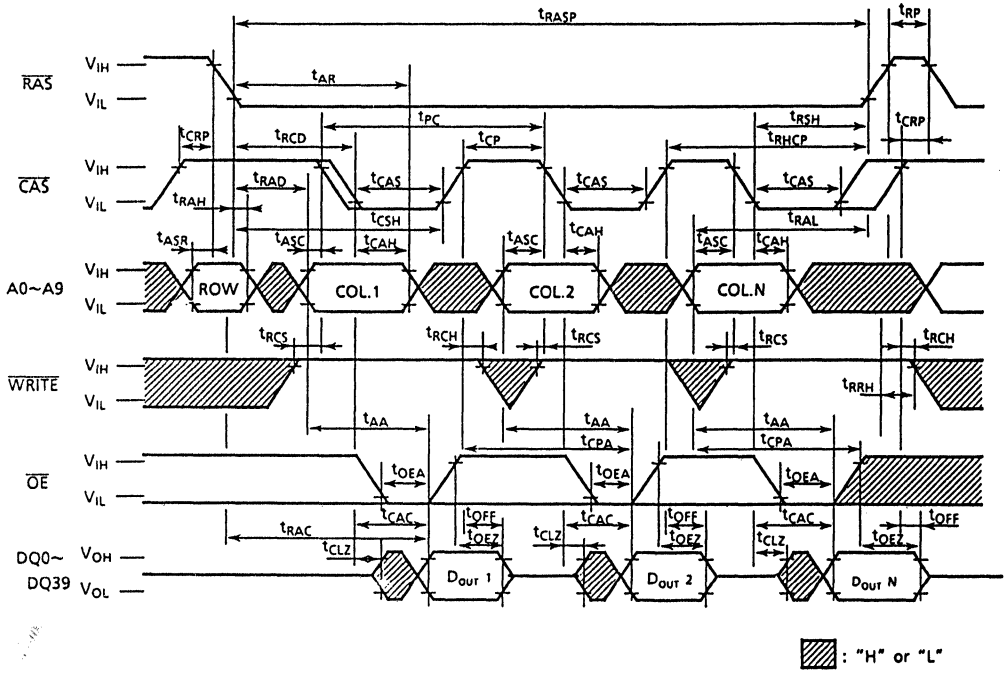
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



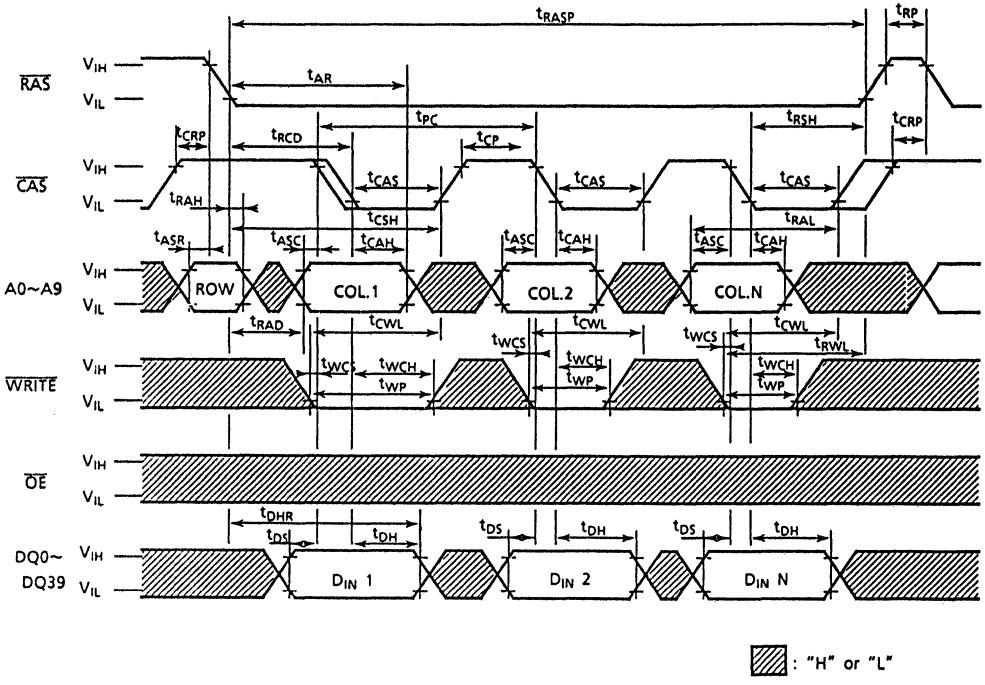
READ-MODIFY-WRITE CYCLE



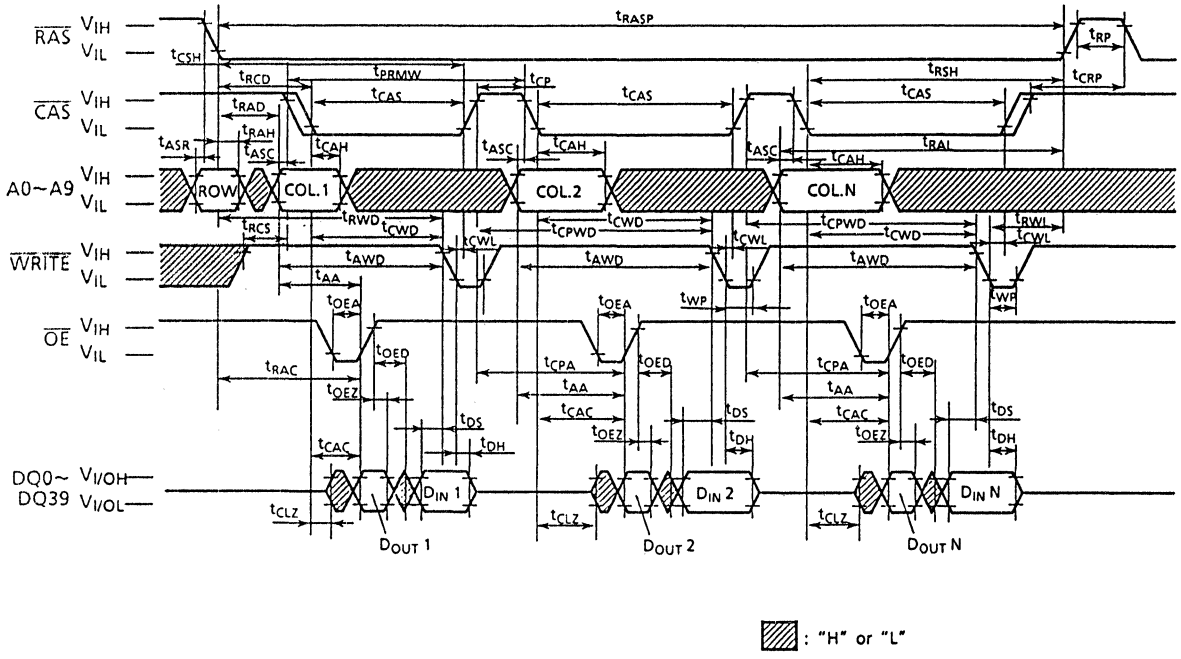
FAST PAGE MODE READ CYCLE



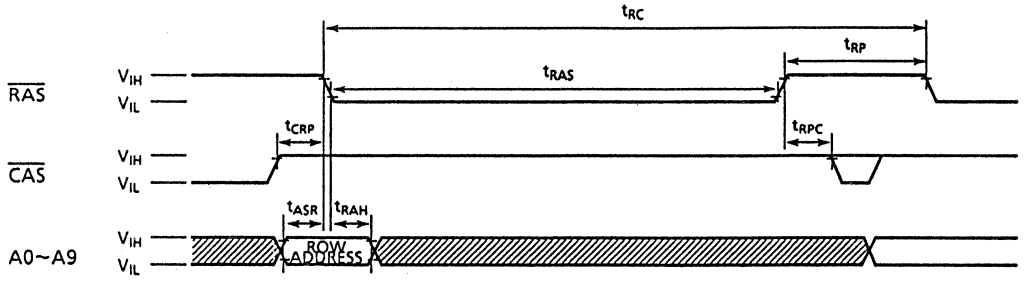
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



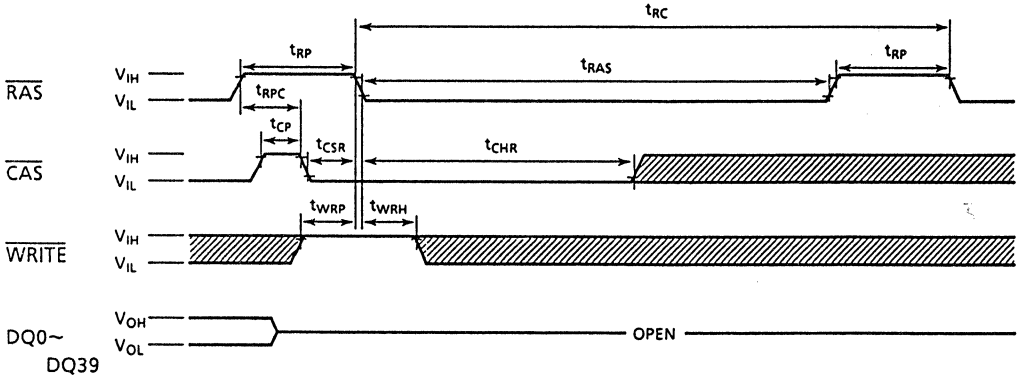
$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE : $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

: "H" or "L"

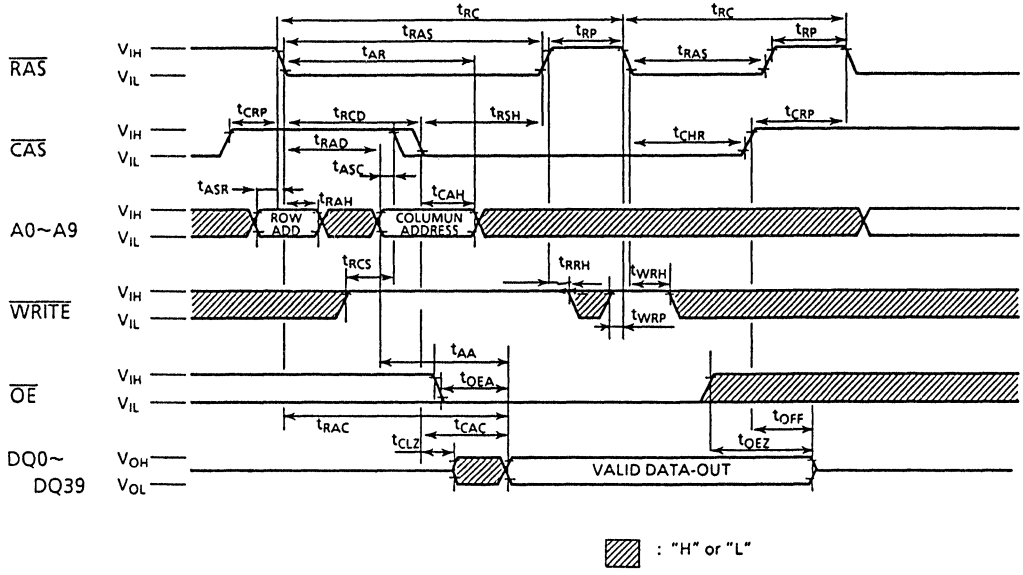
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



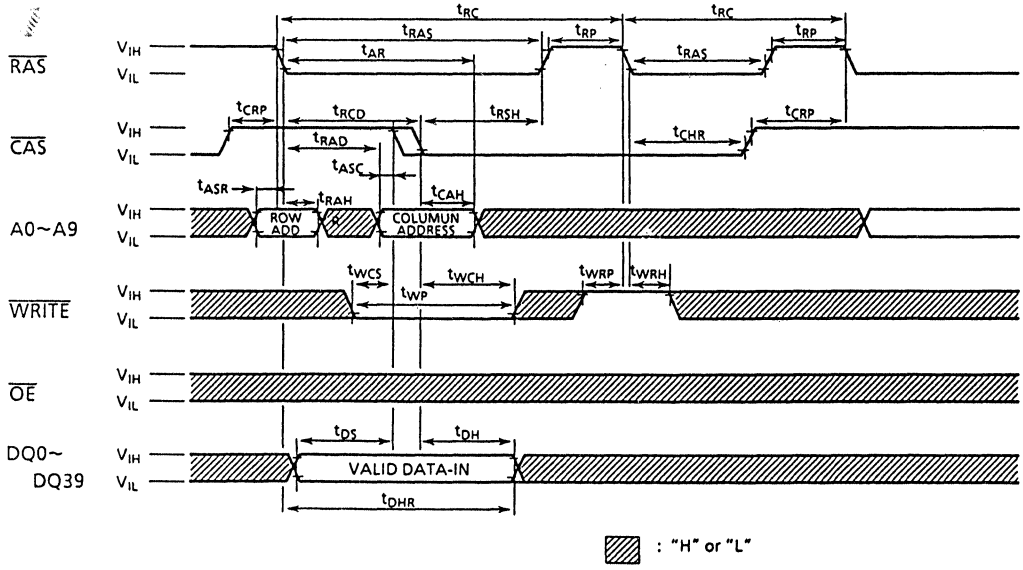
NOTE : $\overline{OE}$, A0~A9 = "H" or "L"

: "H" or "L"

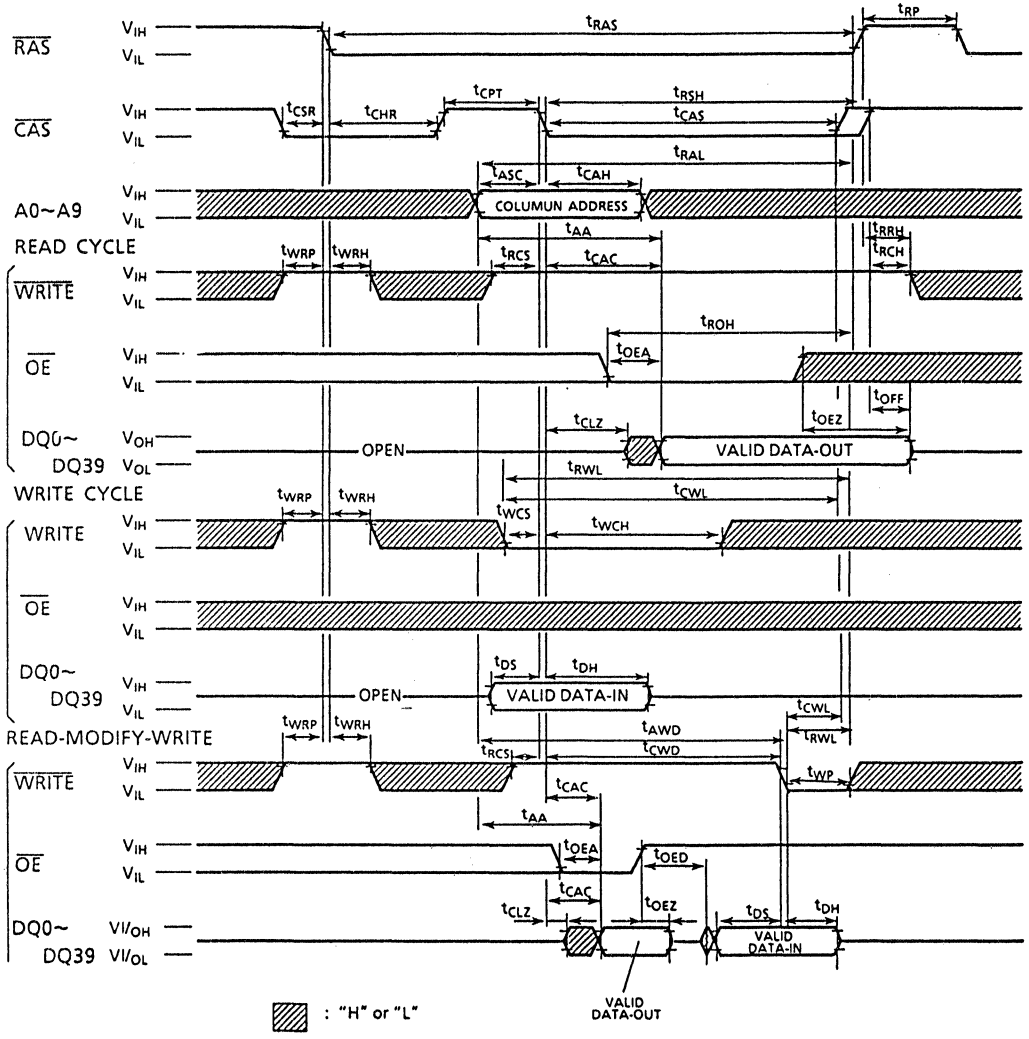
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE

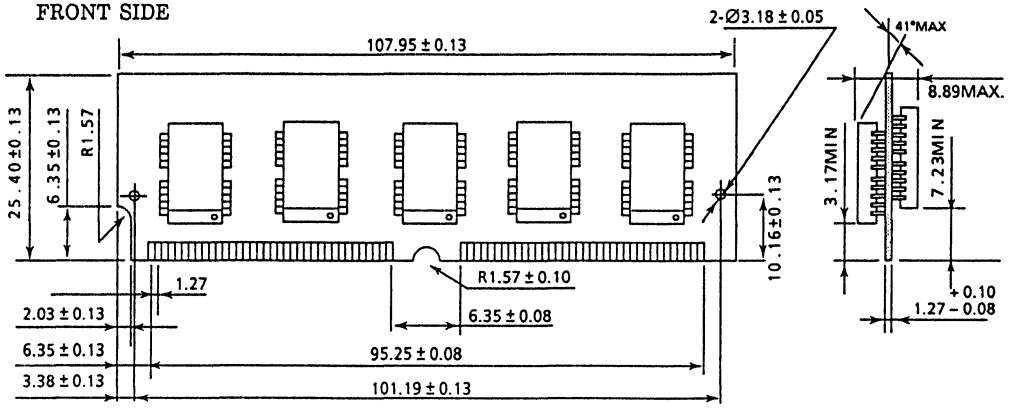


OUTLINE DRAWINGS

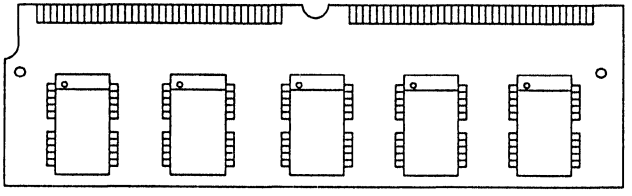
• THM401020SG

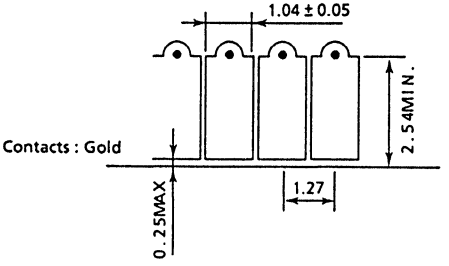
Unit in mm

FRONT SIDE



BACK SIDE





NOTES

2,097,152 WORDS X 32 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM322020S is a 2,097,152 words by 32 bits dynamic RAM module which assembled 16 pcs of TC514400J on the printed circuit board. The THM322020S can be as well used as 4,194,304 words by 16 bits dynamic RAM module, by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ·····, DQ15 and DQ31, respectively. The THM322020S is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

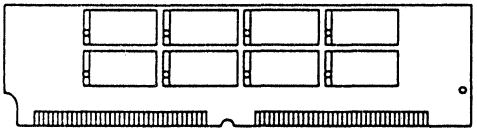
FEATURES

- 2,097,152 words by 32 bits organization
- Fast access time and cycle time

		THM322020 S-80	THM322020 S-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low Power
  4,708mW MAX. Operating (THMxxxxx-80)
  4,048mW MAX. Operating (THMxxxxx-10)
  88mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible.
- 1024 Refresh cycles/16ms
- Tin-Lead Contact : THM322020S-80, 10
- Gold Contact : THM322020SG-80, 10

PIN CONNECTION (TOP VIEW)



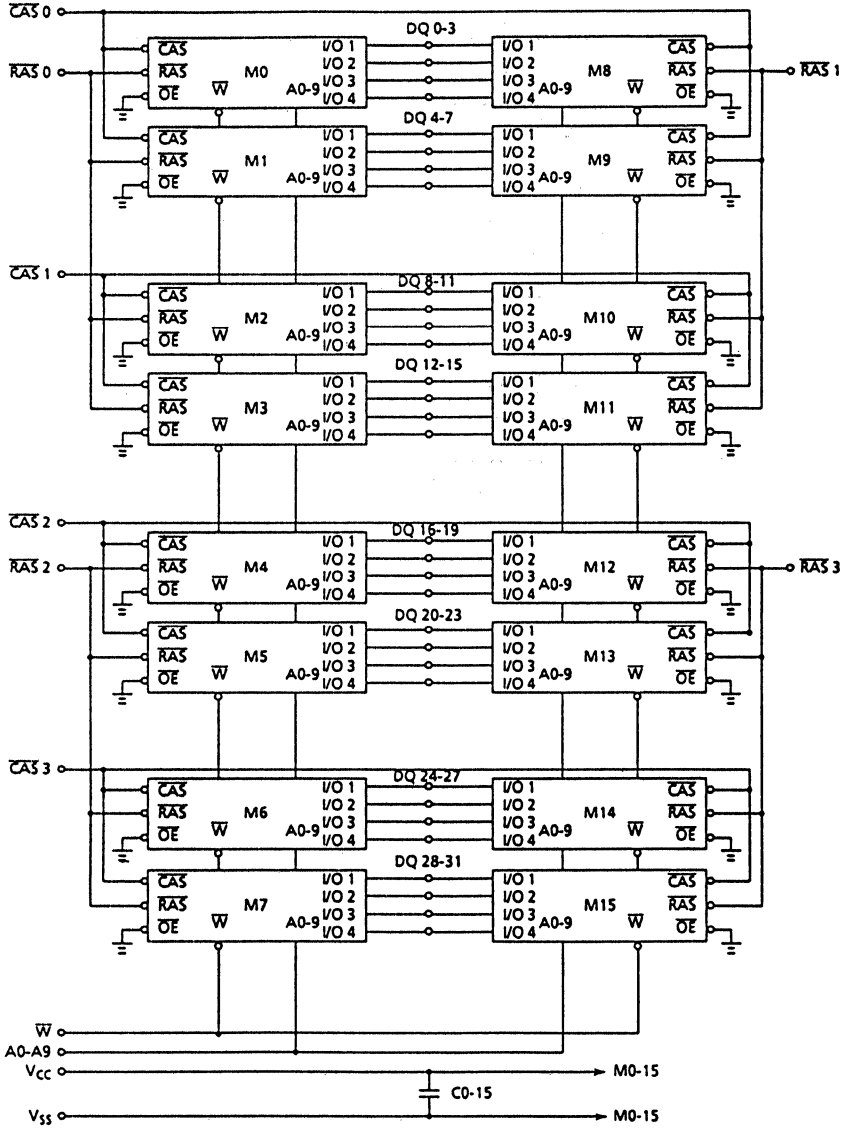
1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ31	Data Input/Output
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5V)
V_{SS}	Ground
PD	Presence Detect Pin

	-80	-10
PD0	NC	NC
PD1	NC	NC
PD2	NC	V_{SS}
PD3	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0~7.0	V	1
Output Voltage	V_{OUT}	-1.0~7.0	V	1
Power Supply Voltage	V_{CC}	-1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	7.2	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THM322020S-80	–	856	mA	3, 4
		THM322020S-10	–	736		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	32	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	THM322020S-80	–	856	mA	3
		THM322020S-10	–	736		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} MIN.)	THM322020S-80	–	576	mA	3, 4
		THM322020S-10	–	496		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	16	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THM322020S-80	–	856	mA	3
		THM322020S-10	–	736		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins not under Test = 0V)		– 160	160	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 20	20	µA	
I_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM3220205-80		THM3220205-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

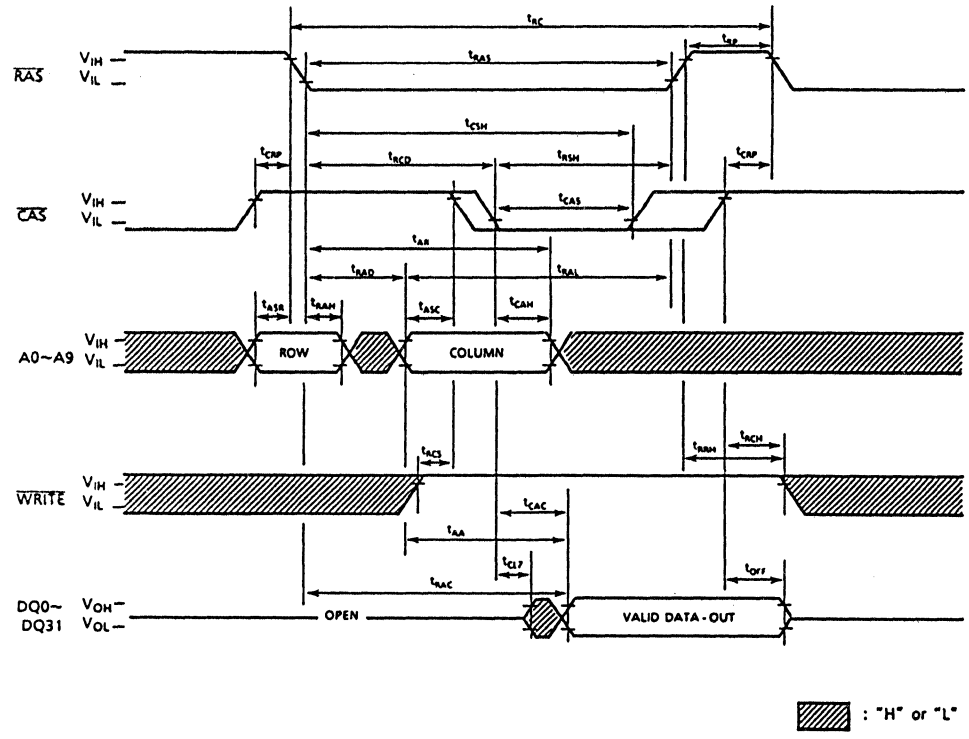
SYMBOL	PARAMETER	THM322020S-80		THM322020S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Date Set-Up Time	0	-	0	-	ns	11
t_{DH}	Date Hold Time	15	-	20	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-UP Time	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ before Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

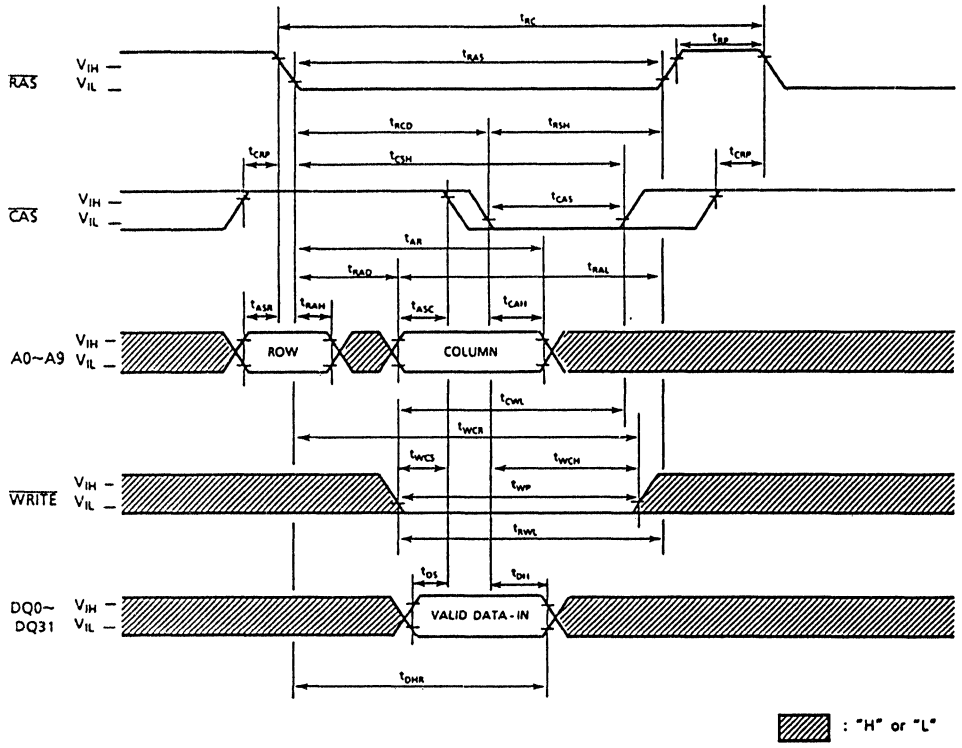
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A9)	-	161	pF
CI2	Input Capacitance ($\overline{W}$)	-	168	pF
CI3	Input Capacitance ($\overline{RAS0}$~ $\overline{RAS3}$)	-	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	42	pF
CDQ1	I/O Capacitance (DQ0~31)	-	29	pF

NOTES:

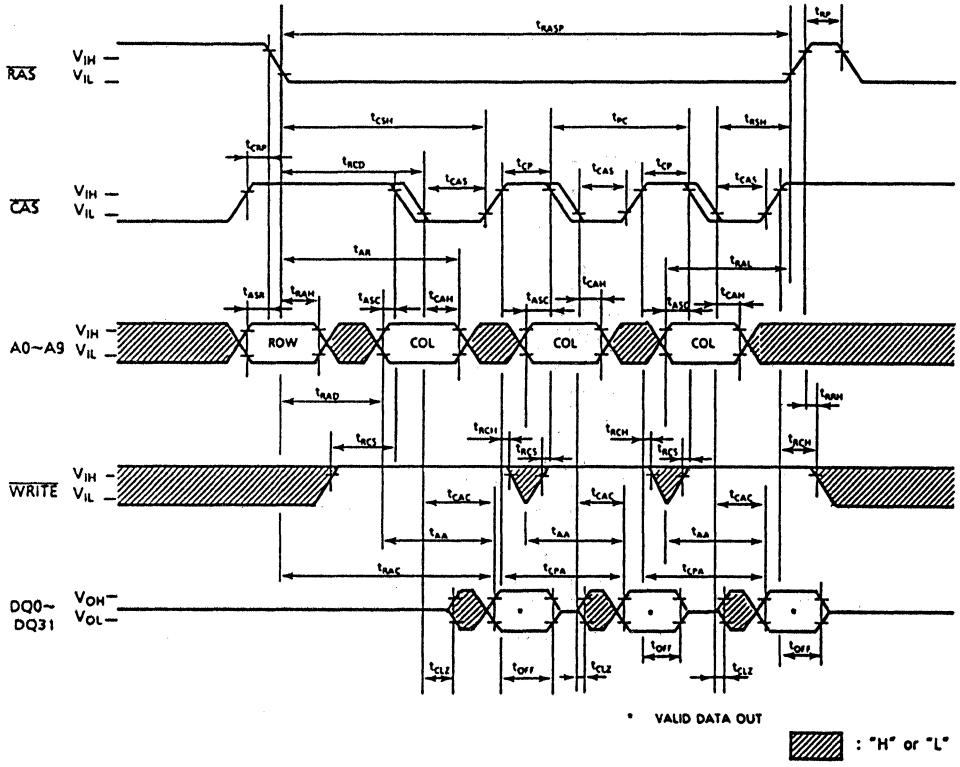
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5ns$.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
    t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met.
    t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.


RAS
CAS
A0~A9
WRITE
DQ0~
DQ31
VIH
VIL
VOH
VOL
ROW
COLUMN
OPEN
VALID DATA-OUT
: "H" or "L"

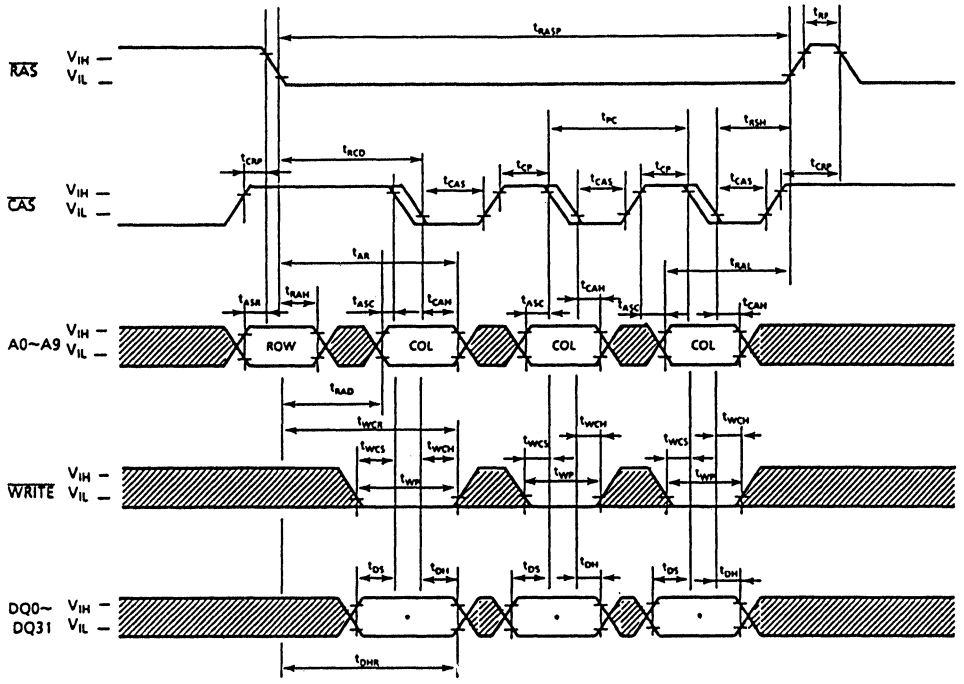
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE



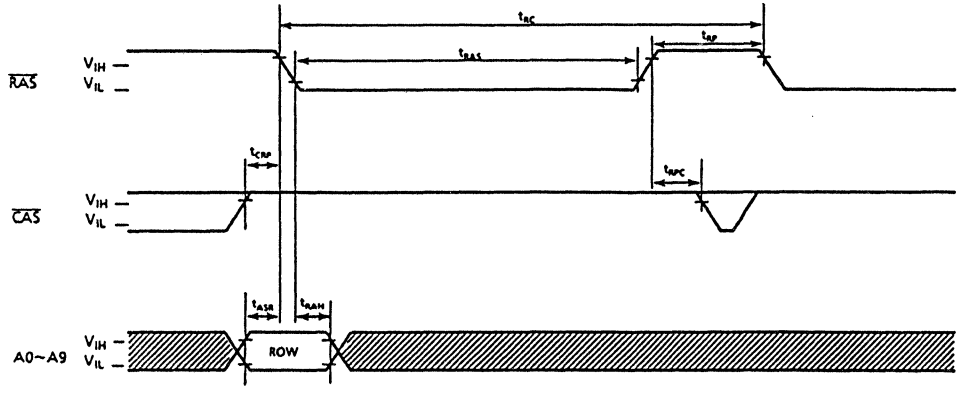
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



* VALID DATA IN

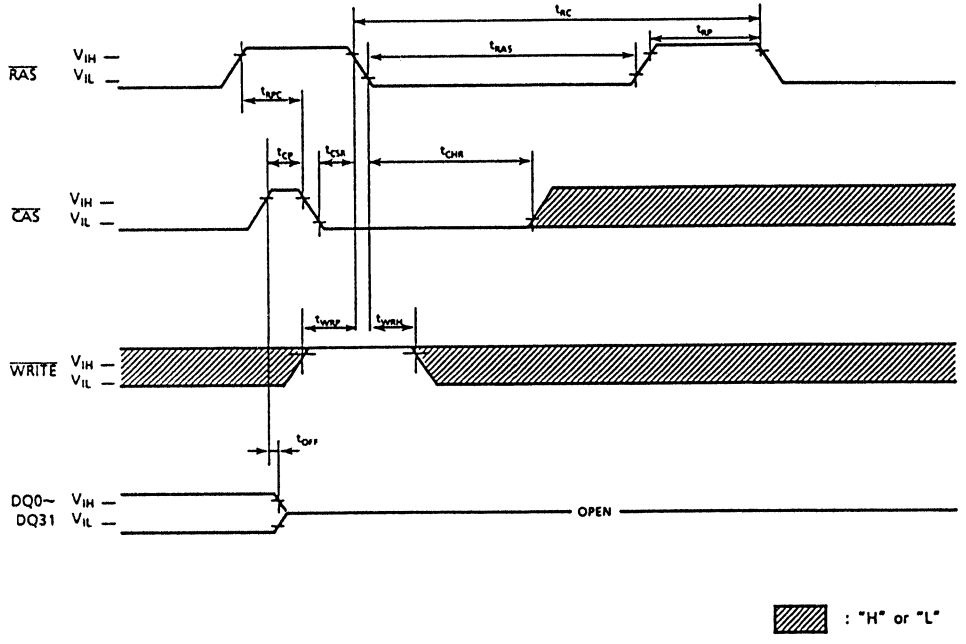
: "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



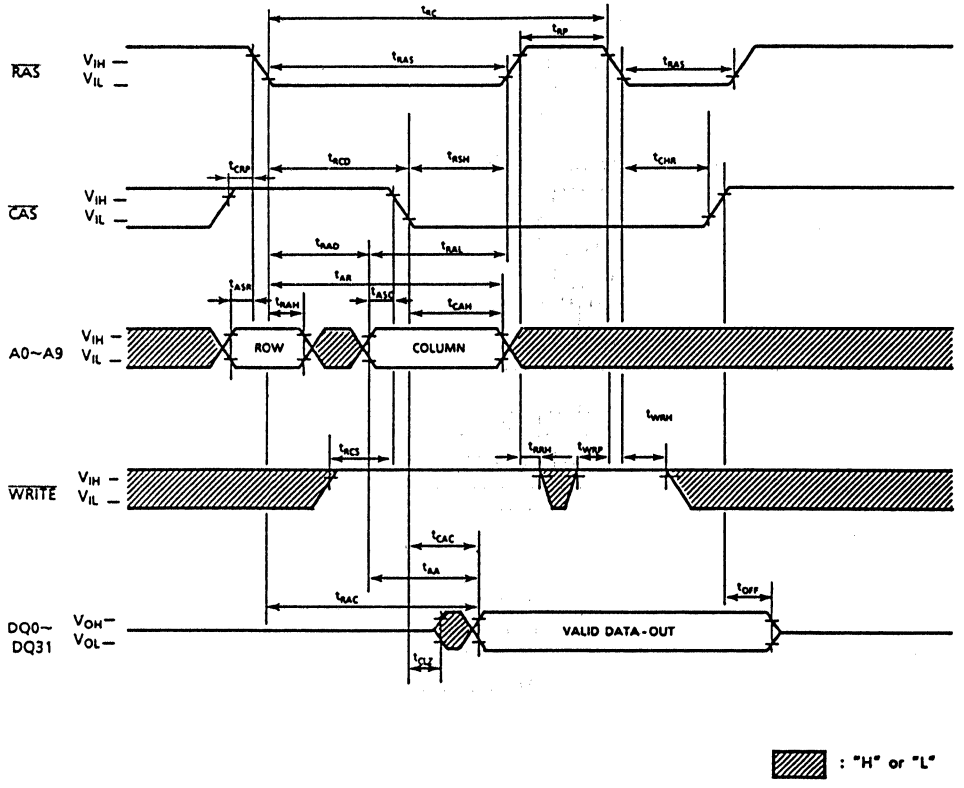
Note: $\overline{WRITE}$ = "H" or "L"

CAS BEFORE RAS REFRESH CYCLE

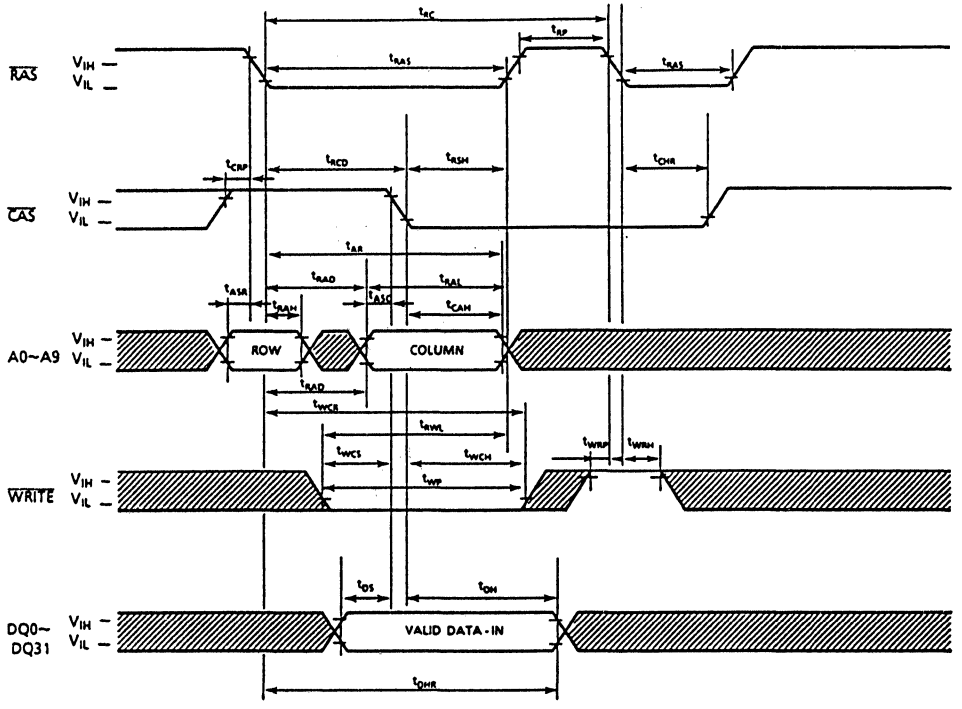


Note: A0~A9 = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

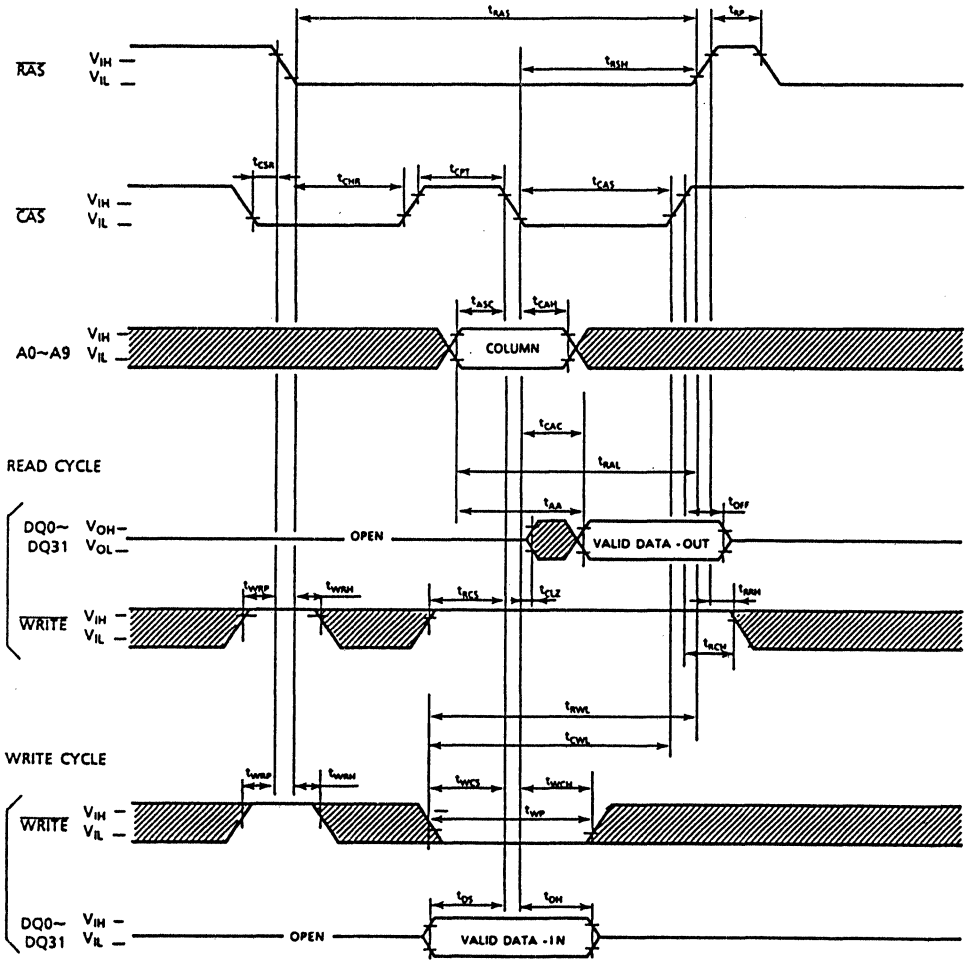


HIDDEN REFRESH CYCLE (WRITE)



: "H" or "L"

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE

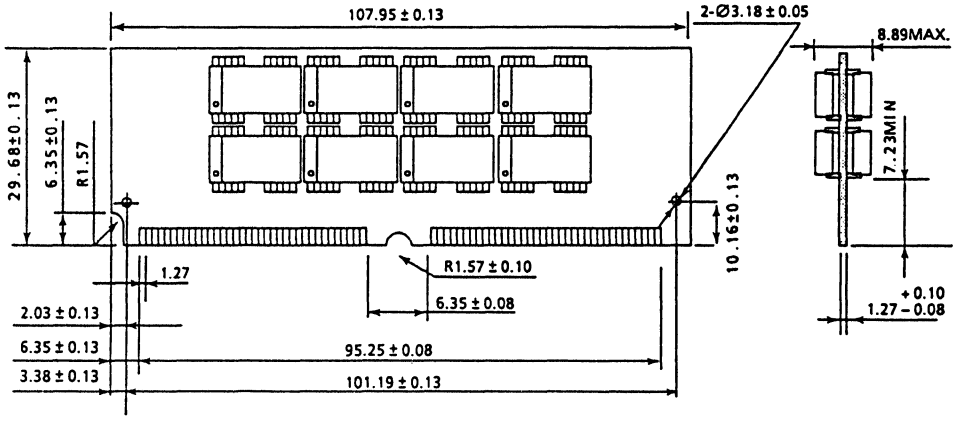


: "H" or "L"

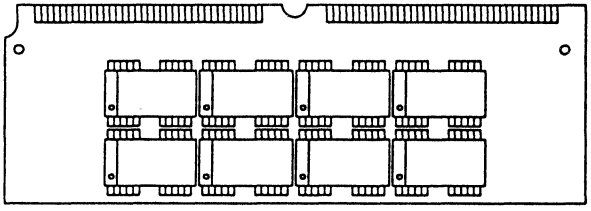
OUTLINE DRAWINGS

Unit in mm

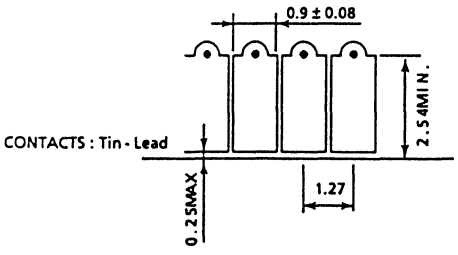
FRONT SIDE



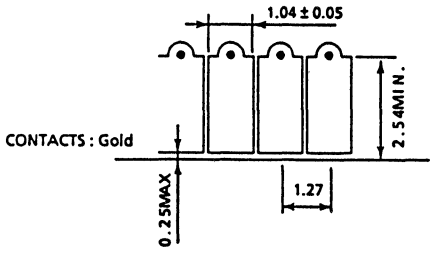
BACK SIDE



• THM322020S



• THM322020SG



NOTES

2,097,152 WORDS X 36 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM362020S is a 2,097,152 words by 36 bits dynamic RAM module which assembled 16 pcs of TC514400J and 8 pcs of TC511000AJ on the printed circuit board. The THM362020S can be as well used as 4,194,304 words by 18 bits dynamic RAM module, by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ·····, DQ17 and DQ35, respectively. The THM362020S is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

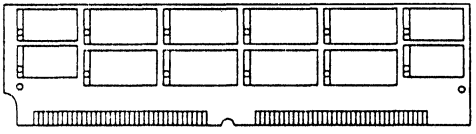
FEATURES

- 2,097,152 words by 36 bits organization
- Fast access time and cycle time

		THM362020 S-80	THM362020 S-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low Power
  - 6,292mW MAX. Operating (THMxxxxxx-80)
  - 5,412mW MAX. Operating (THMxxxxxx-10)
  - 132mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible.
- 1024 Refresh cycles/ 8ms (Burst Refresh)
- 1024 Refresh cycles/16ms (Distributed Refresh)
- Tin-Lead Contact : THM362020S-80, 10
- Gold Contact : THM362020SG-80, 10

PIN CONNECTION (TOP VIEW)



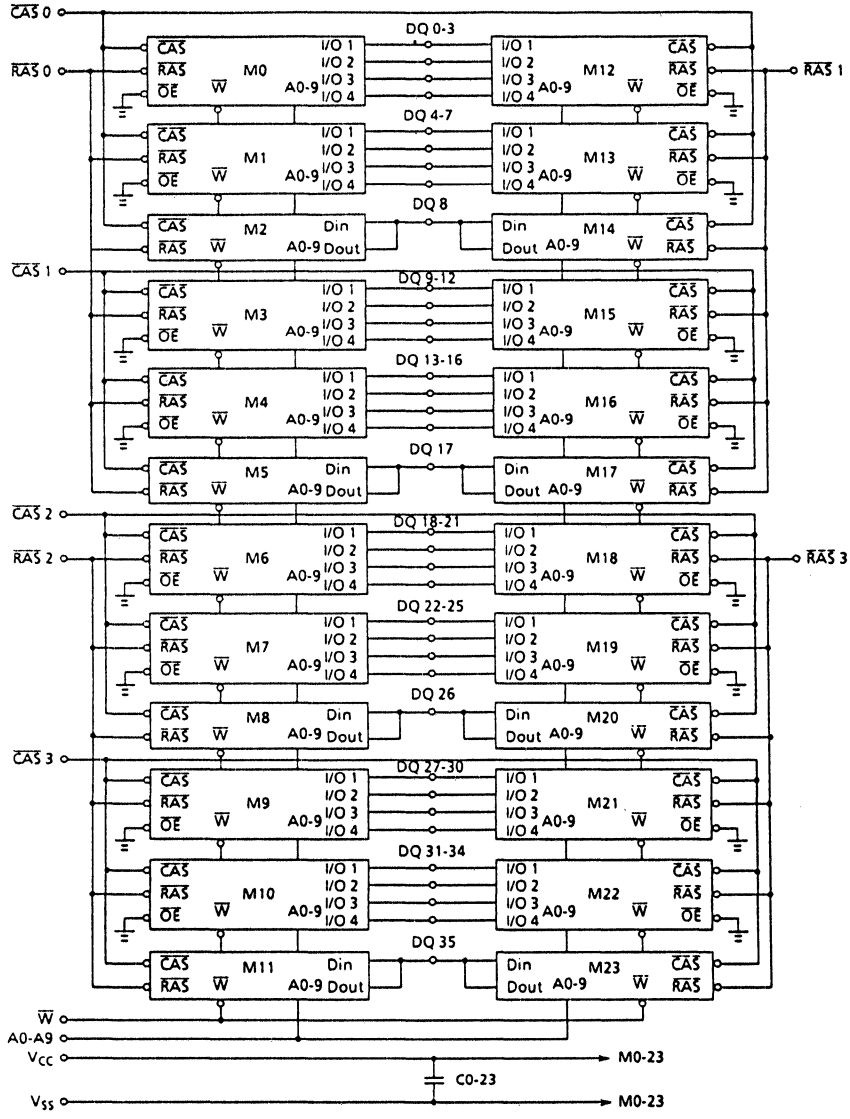
PIN NAMES

A0~A9	Address Inputs
DQ0~DQ35	Data Input/Output
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

	-80	-10
PD0	NC	NC
PD1	NC	NC
PD2	NC	V_{SS}
PD3	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0~7.0	V	1
Output Voltage	V_{OUT}	-1.0~7.0	V	1
Power Supply Voltage	V_{CC}	-1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	7.2	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THM362020S-80	–	1144	mA	3, 4
		THM362020S-10	–	984		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	48	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	THM362020S-80	–	1144	mA	3
		THM362020S-10	–	984		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} MIN.)	THM362020S-80	–	784	mA	3, 4
		THM362020S-10	–	664		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	24	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THM362020S-80	–	1144	mA	3
		THM362020S-10	–	984		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins not under Test = 0V)		– 240	240	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 20	20	μA	
I_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM362020S-80		THM362020S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THM362020S-80		THM362020S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Date Set-Up Time	0	-	0	-	ns	11
t_{DH}	Date Hold Time	15	-	20	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-UP Time	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ before Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

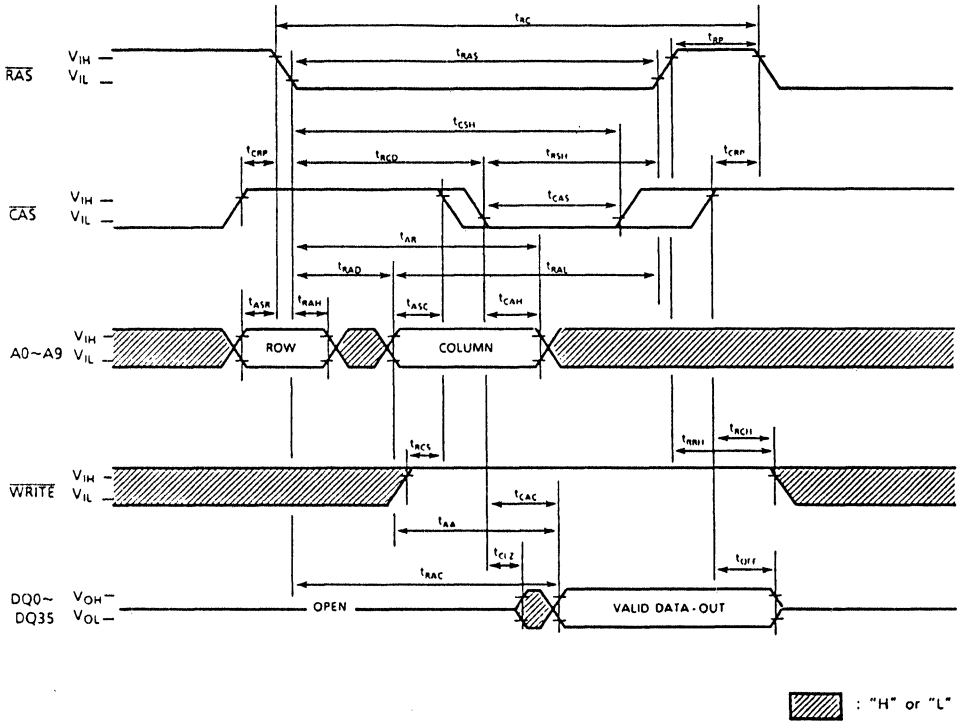
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A9)	-	161	pF
CI2	Input Capacitance ($\overline{W}$)	-	168	pF
CI3	Input Capacitance ($\overline{RAS0}$~ $\overline{RAS3}$)	-	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	42	pF
CDQ1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	-	29	pF
CDQ2	I/O Capacitance (DQ8, 17, 26, 35)	-	39	pF

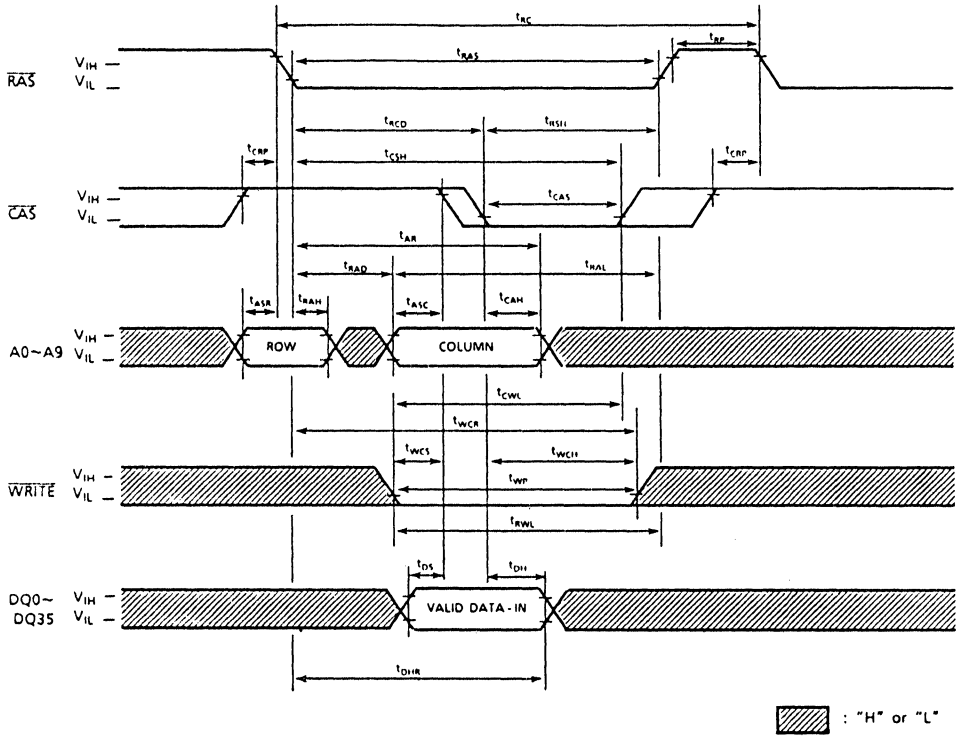
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5ns$.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
    t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met.
    t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

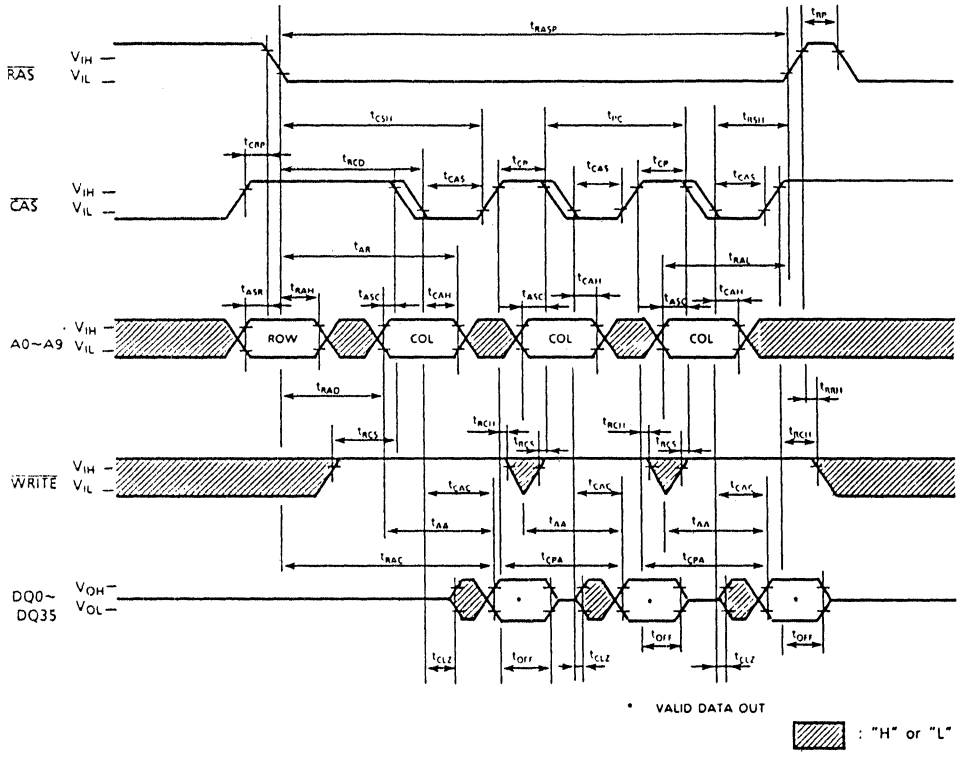
READ CYCLE


RAS
CAS
A0~A9
WRITE
DQ0~
DQ35
ROW
COLUMN
OPEN
VALID DATA-OUT
: "H" or "L"

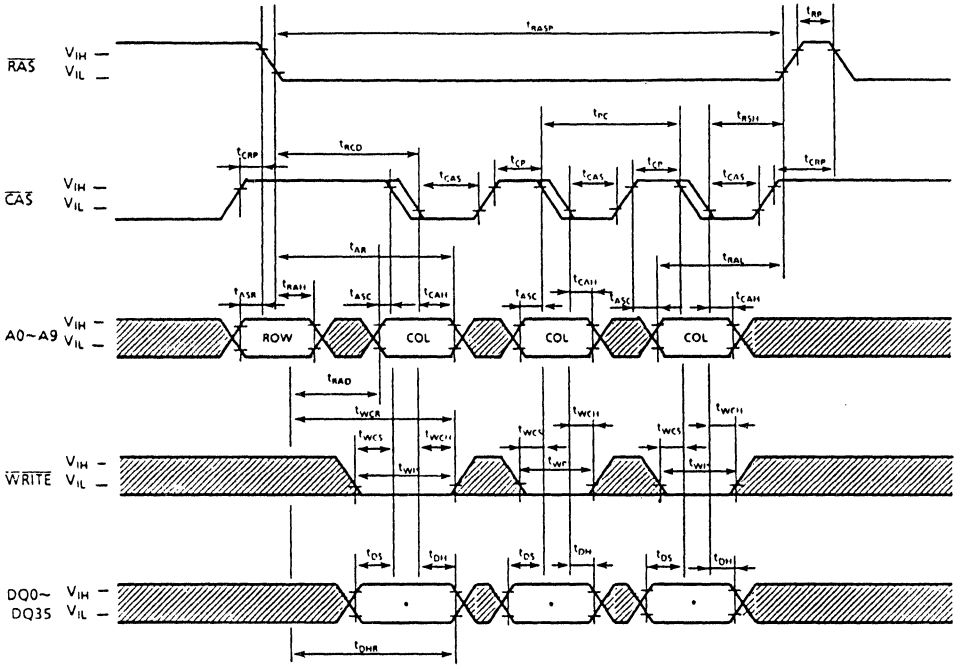
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE



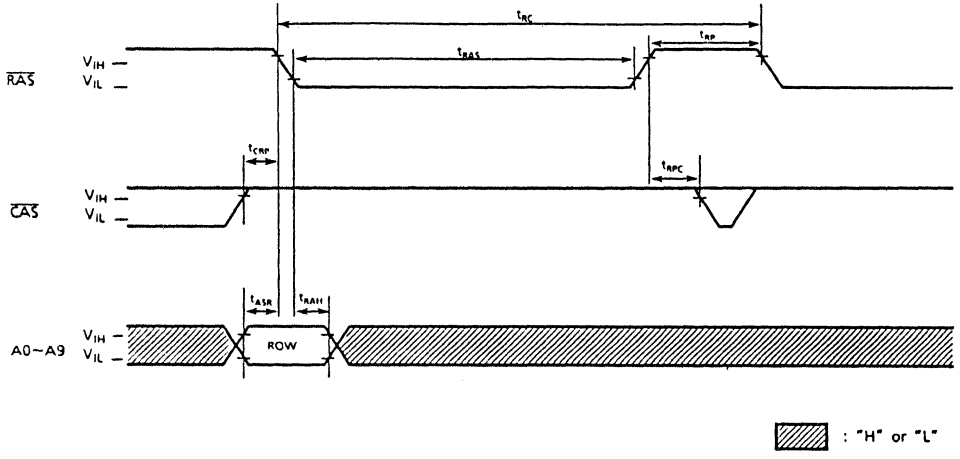
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



* VALID DATA IN

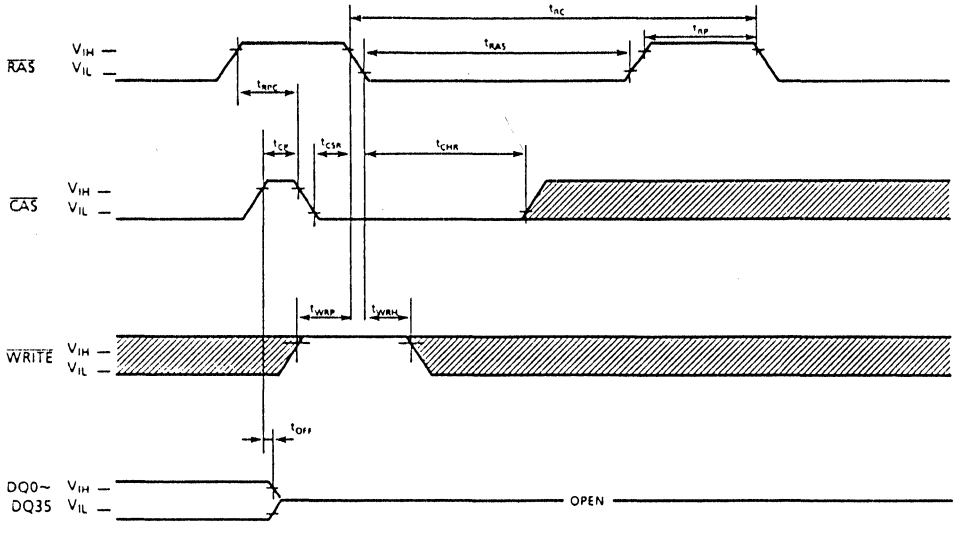
: "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



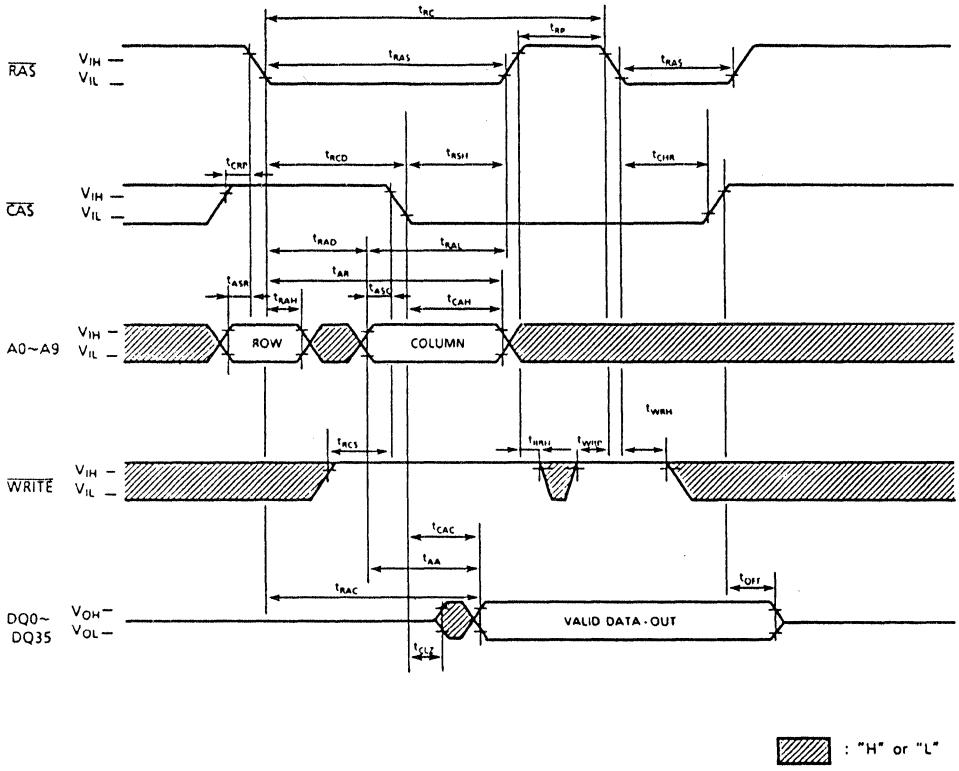
Note: $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

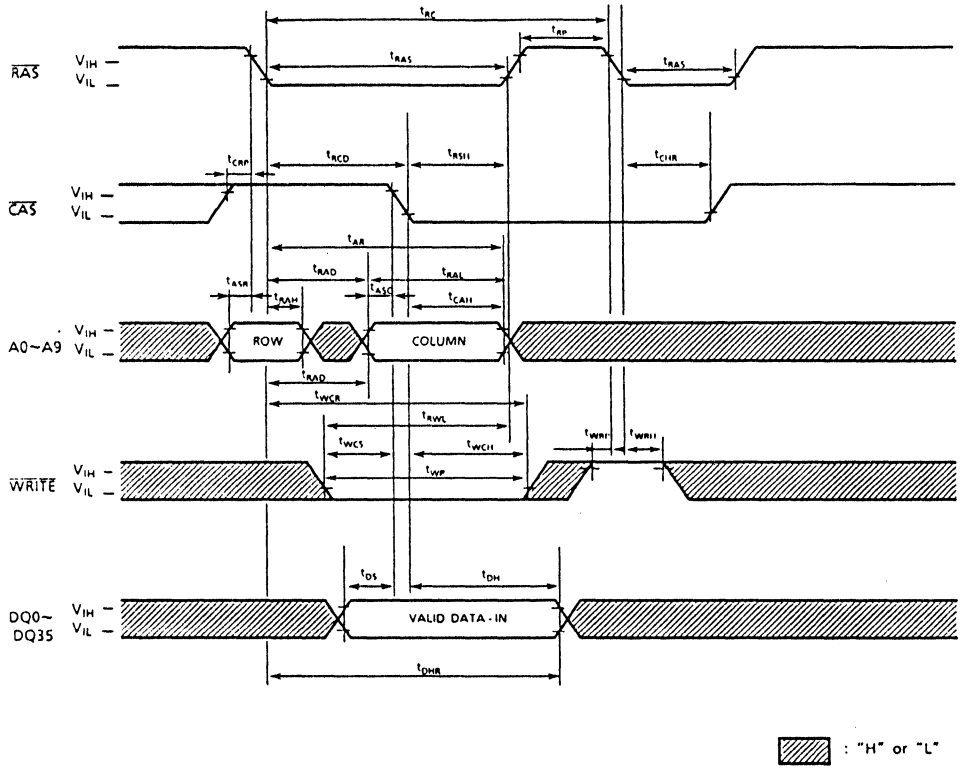


Note: A0~A9 = "H" or "L"

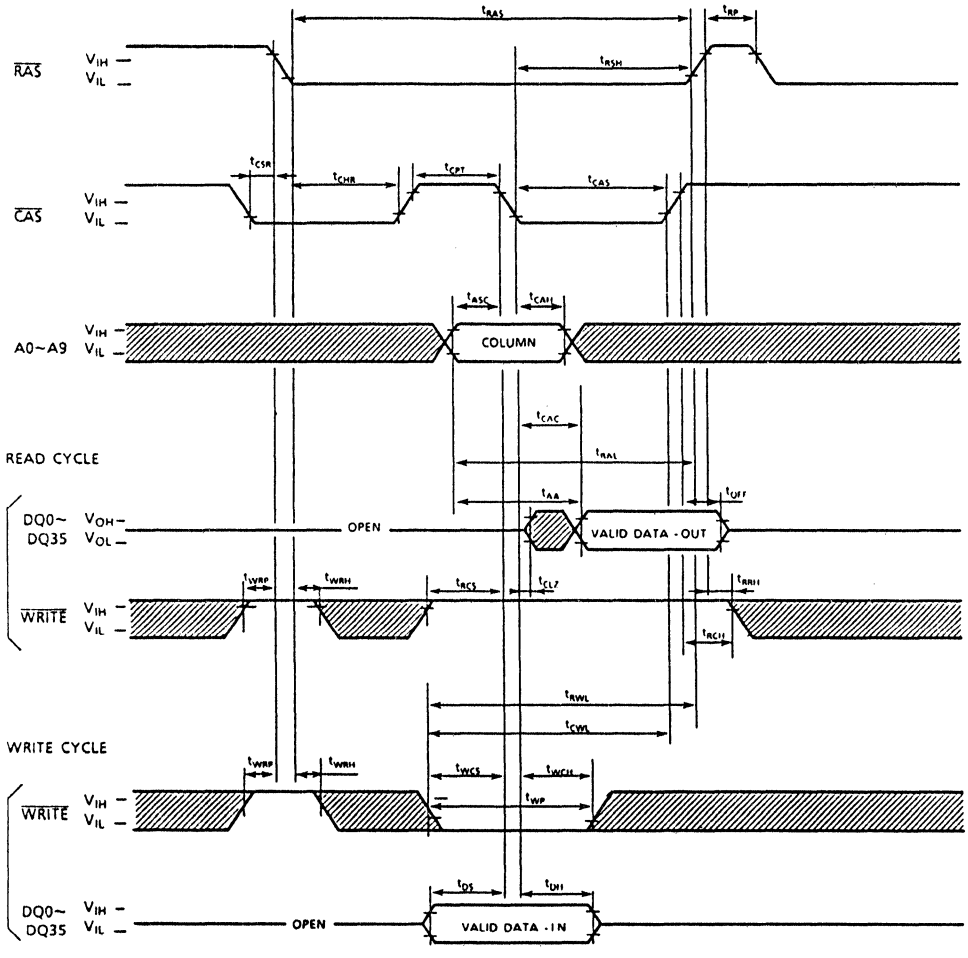
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



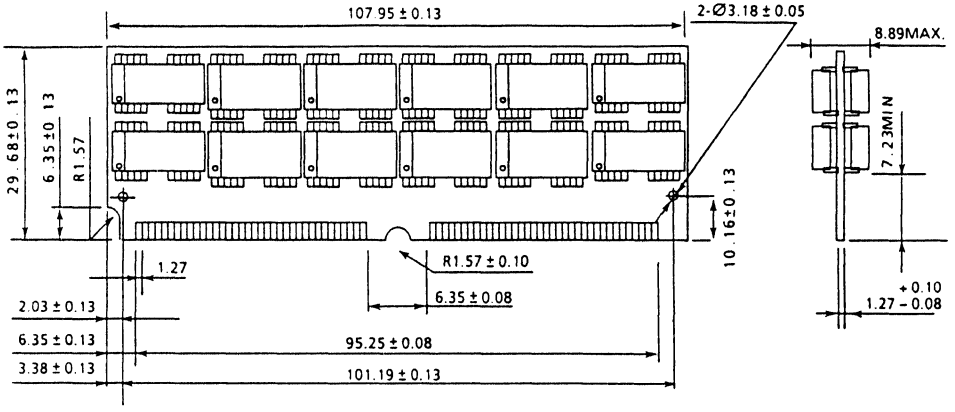
CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



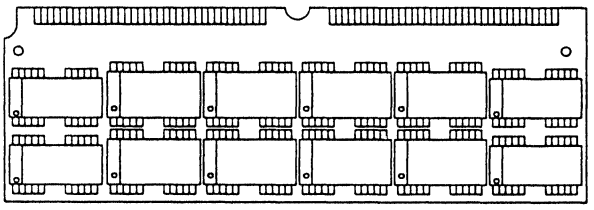
OUTLINE DRAWINGS

Unit in mm

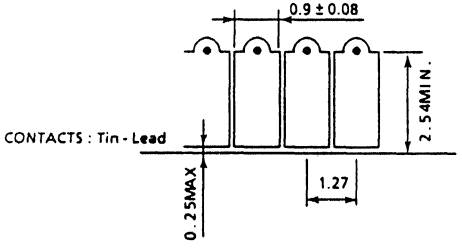
FRONT SIDE



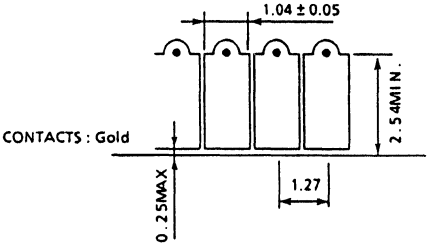
BACK SIDE



• THM362020S



• THM362020SG



NOTES

2,097,152 WORDS×40 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM402020SG is a 2,097,152 words by 40 bits dynamic RAM module which assembled 20 pcs of TC514400J on the printed circuit board.

The THM402020SG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

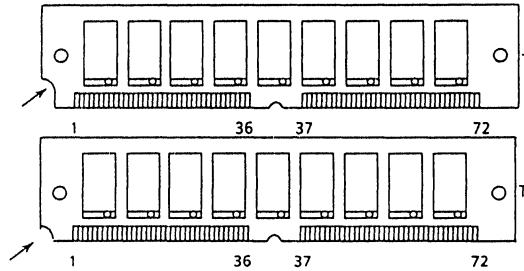
FEATURES

- 2,097,152 words by 40 bits organization
- Fast access time and cycle time

		THM402020 SG-80	THM402020 SG-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low power
  5,885mW MAX. Operating (THMxxxxxx-80)
  5,060mW MAX. Operating (THMxxxxxx-10)
  110mW MAX. Standby
- Read-Modify-write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1024 Refresh cycles/16ms
- Gold Contact
- JEDEC OUTLILNE : THM402020SG-80, 10
- NON JEDEC OUTLINE : THM402040SG-80, 10

PIN CONNECTION (TOP VIEW)



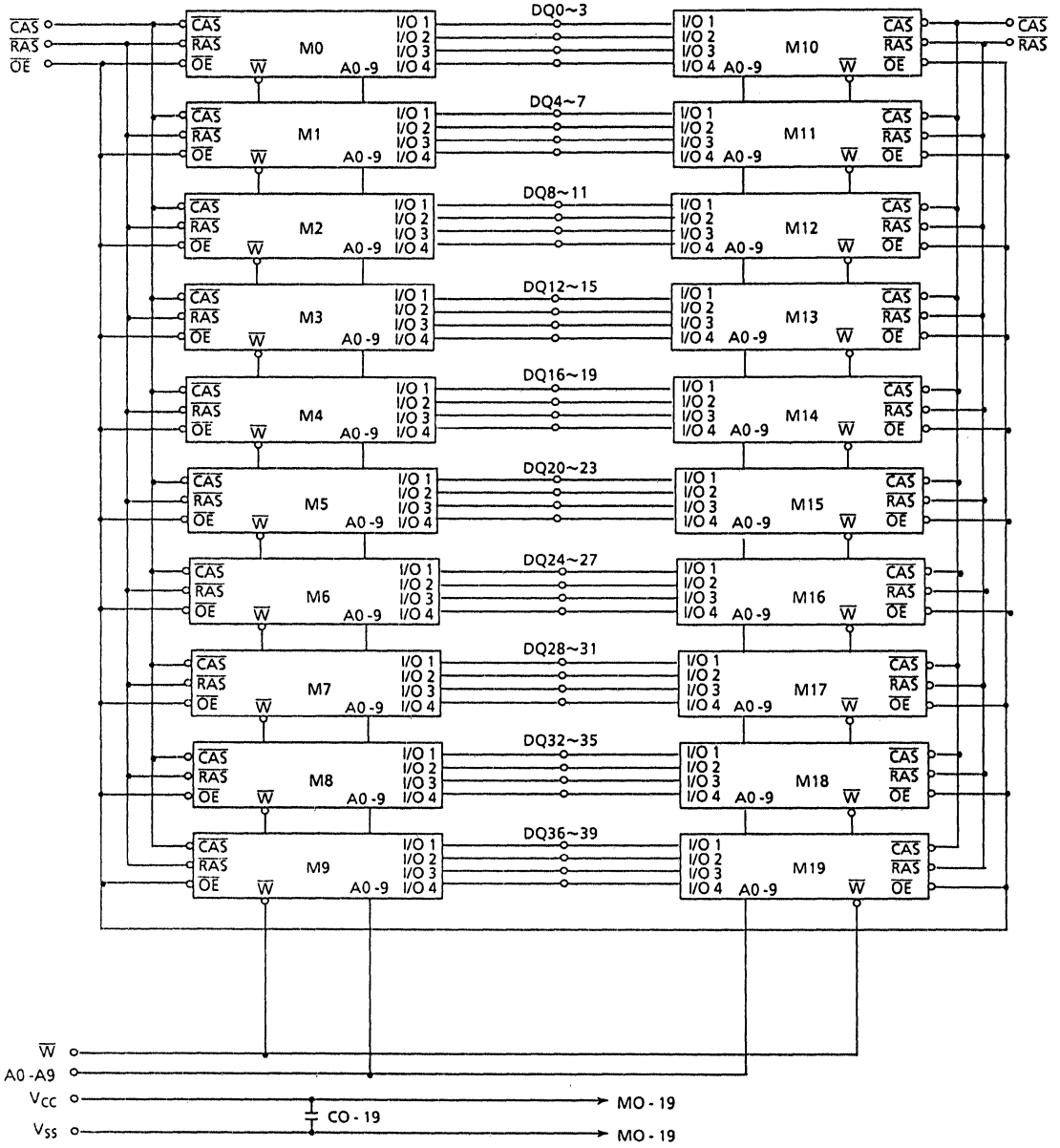
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	$\overline{CAS1}$	55	DQ28	67	PD0
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS0}$	56	DQ29	68	PD1
9	DQ7	21	DQ9	33	NC	45	$\overline{RAS1}$	57	DQ30	69	PD2
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD3
11	NC	23	DQ11	35	DQ17	47	$\overline{W}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	V_{SS}	60	DQ32	72	V_{SS}

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ39	Data Inputs/Outputs
$\overline{CAS0}$,$\overline{CAS1}$	Column Address Strobe
$\overline{RAS0}$,$\overline{RAS1}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

	-80	-10
PD0	NC	NC
PD1	NC	NC
PD2	NC	V_{SS}
PD3	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	6.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THM402020SG-80	–	1070	mA	3,4,5
		THM402020SG-10	–	920		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	40	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	THM402020SG-80	–	1070	mA	3,5
		THM402020SG-10	–	920		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} MIN.)	THM402020SG-80	–	720	mA	3,4,5
		THM402020SG-10	–	620		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	20	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THM402020SG-80	–	1070	mA	3
		THM402020SG-10	–	920		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test = 0V)		– 200	200	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM402020 SG-80		THM402020 SG-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	205	–	245	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	105	–	125	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM402020 SG-80		THM402020 SG-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	70	–	85	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	75	–	90	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	25	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

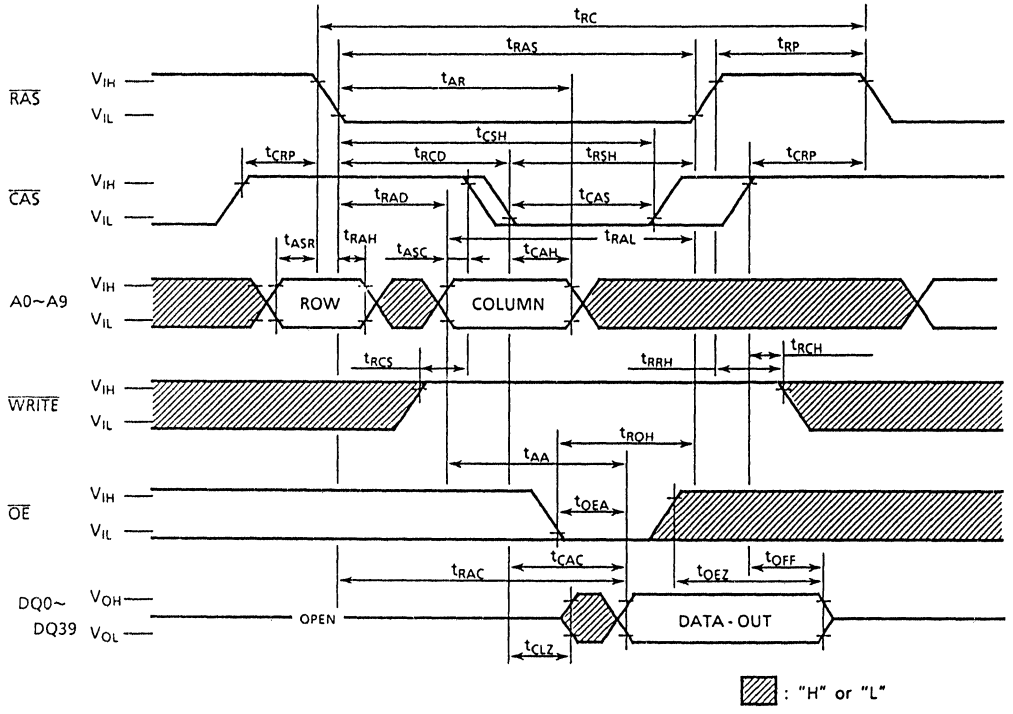
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A9)	-	130	pF
CI2	Input Capacitance ($\overline{W}$, $\overline{OE}$)	-	130	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$)	-	70	pF
CI4	Input Capacitance ($\overline{CAS0}$, $\overline{CAS1}$)	-	70	pF
CDQ	I/O Capacitance (DQ0~DQ39)	-	35	pF

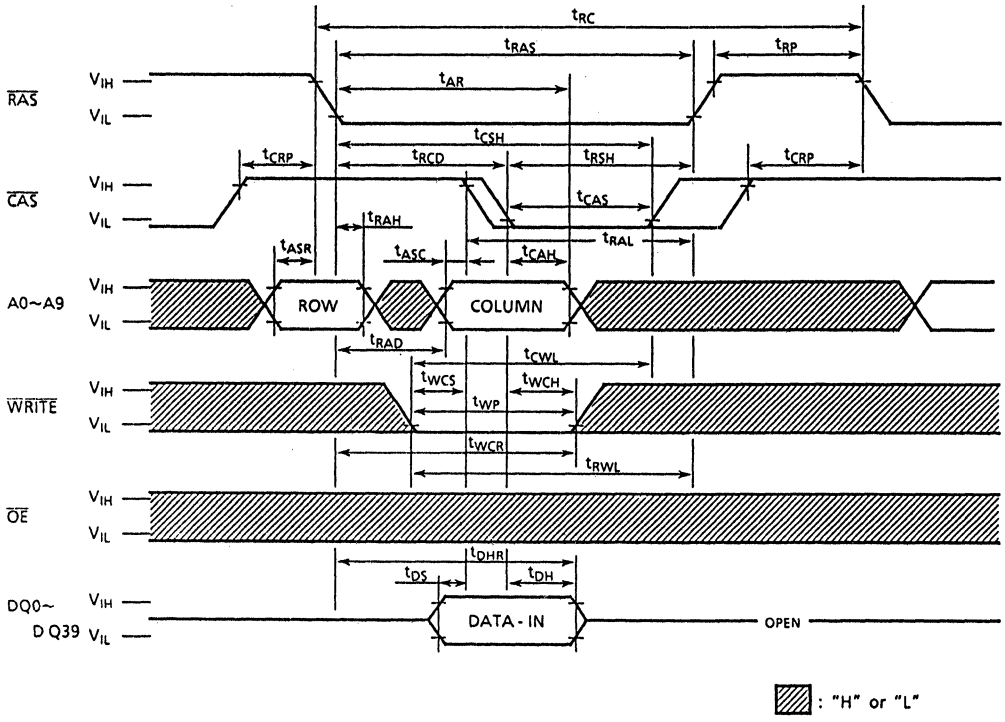
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified value are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

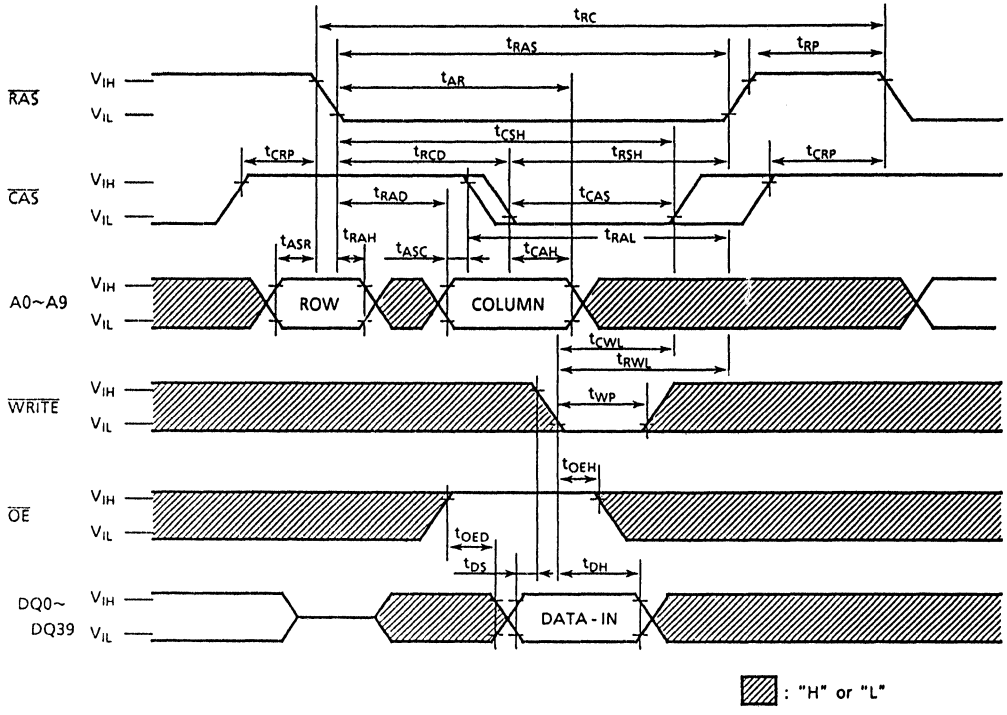
READ CYCLE


tRC
tRAS
tRP
tAR
tCSH
tCRP
tRCD
tRSH
tCRP
RAS
CAS
VIH
VIL
tRAD
tCAS
tASR
tRAH
tASC
tCAH
tRAL
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tROH
tAA
OE
tOEA
tRAC
tCAC
tOEZ
tOFF
DQ0~
DQ39
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

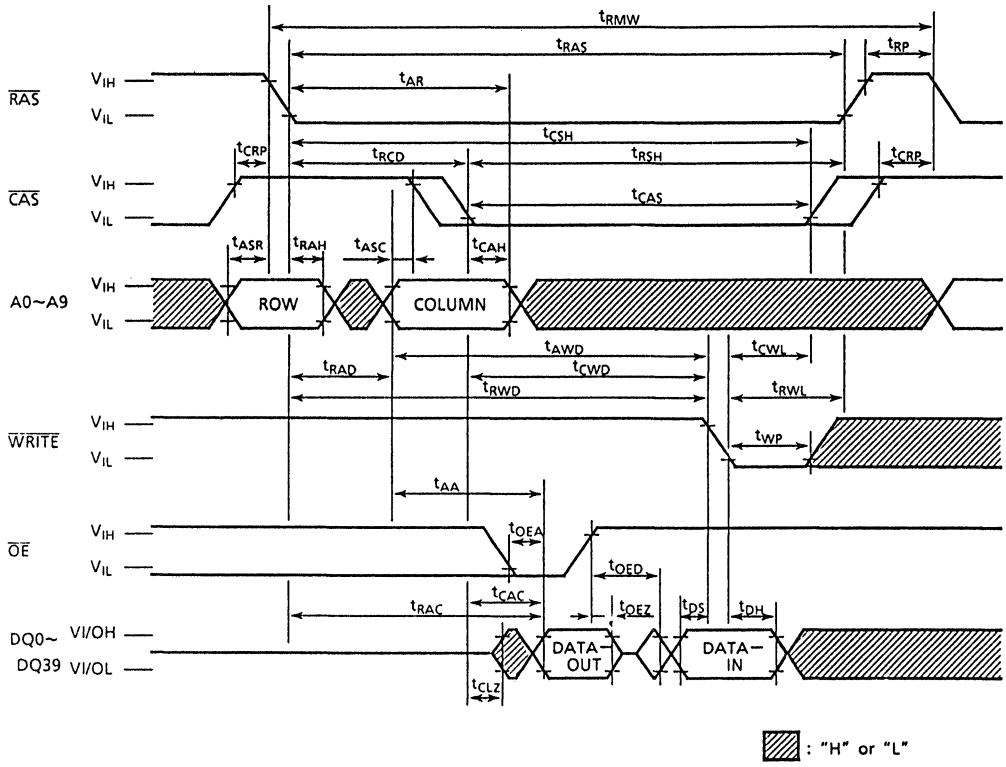
WRITE CYCLE (EARLY WRITE)



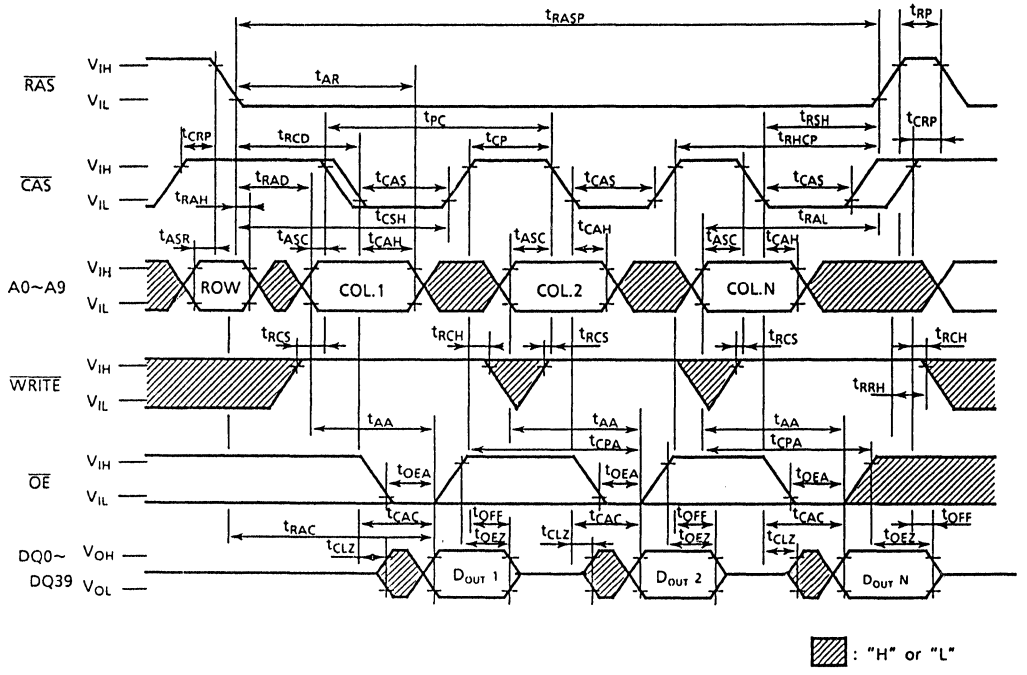
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



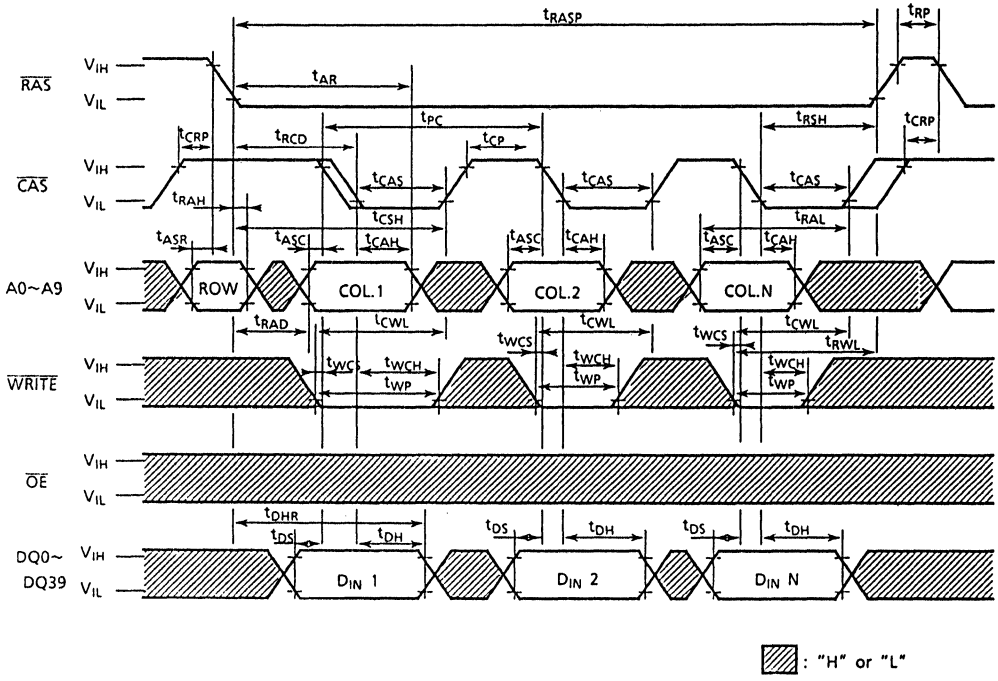
READ-MODIFY-WRITE CYCLE



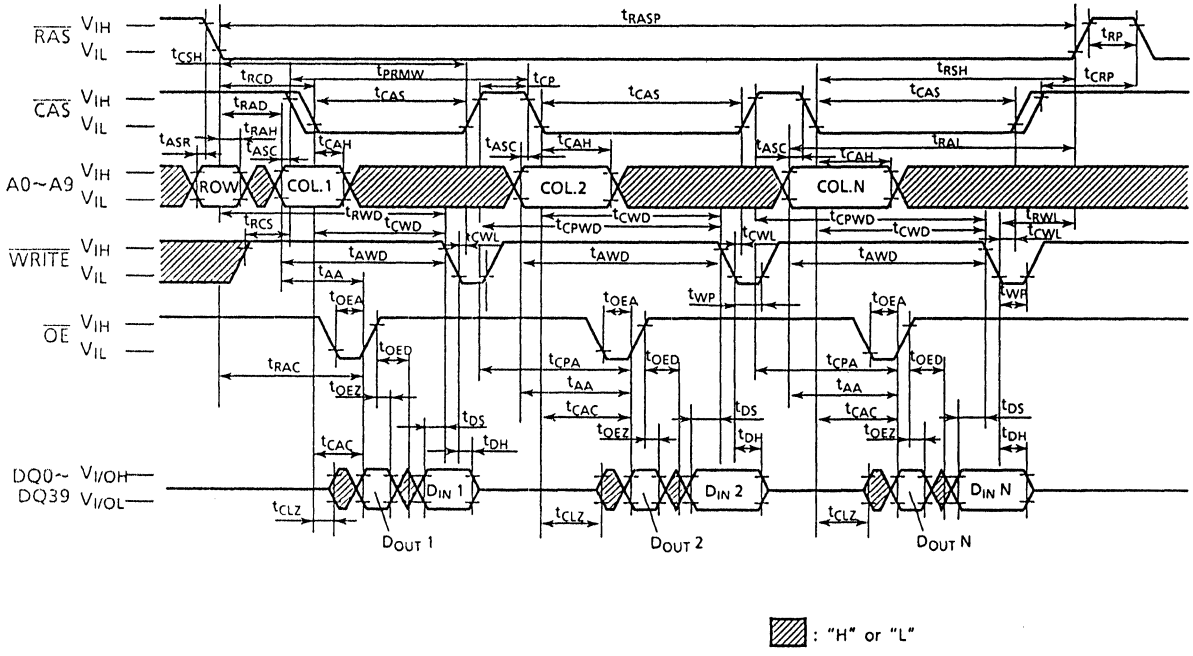
FAST PAGE MODE READ CYCLE



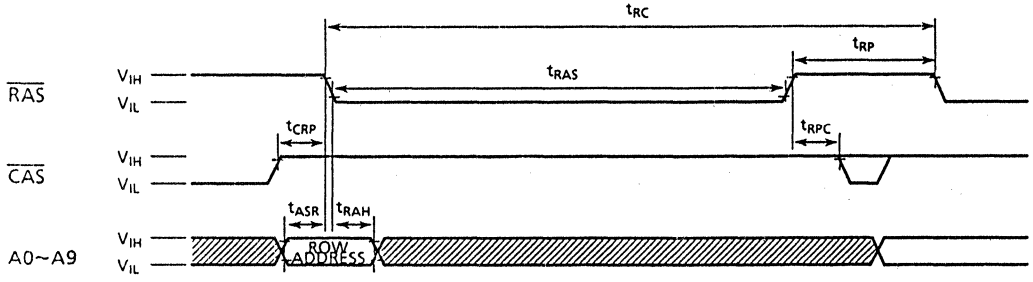
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



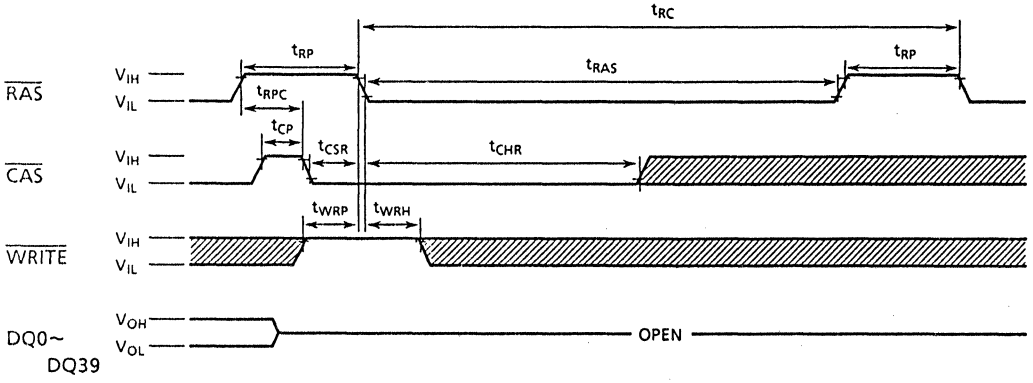
RAS ONLY REFRESH CYCLE



NOTE : $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

: "H" or "L"

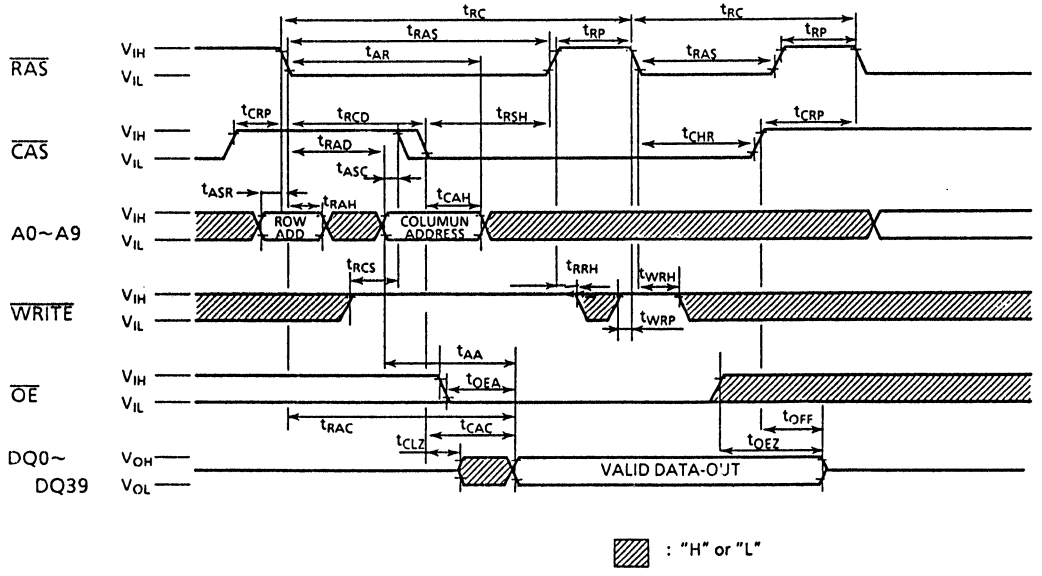
CAS BEFORE RAS REFRESH CYCLE



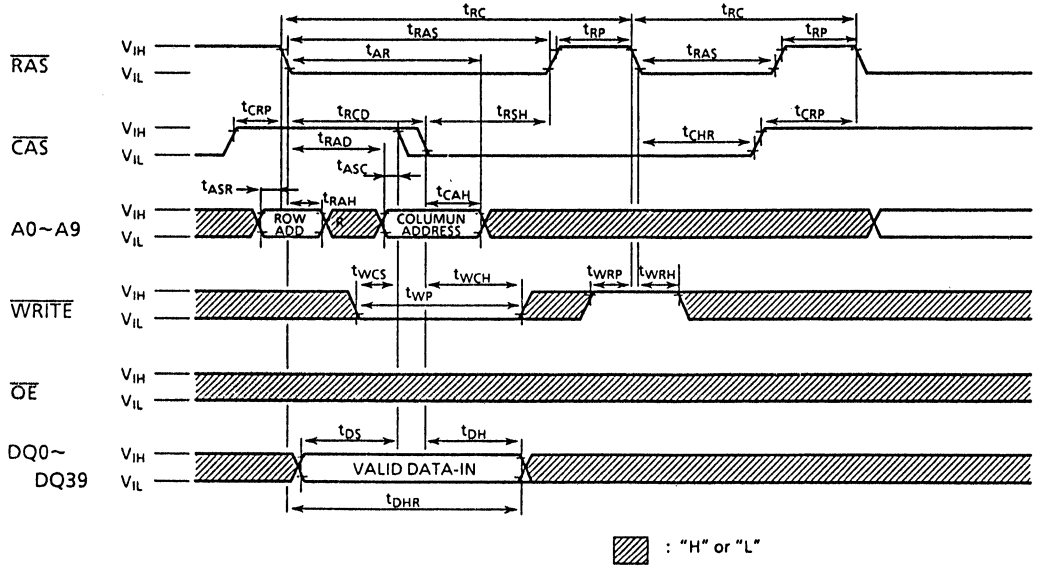
NOTE : $\overline{OE}$, A0~A9 = "H" or "L"

: "H" or "L"

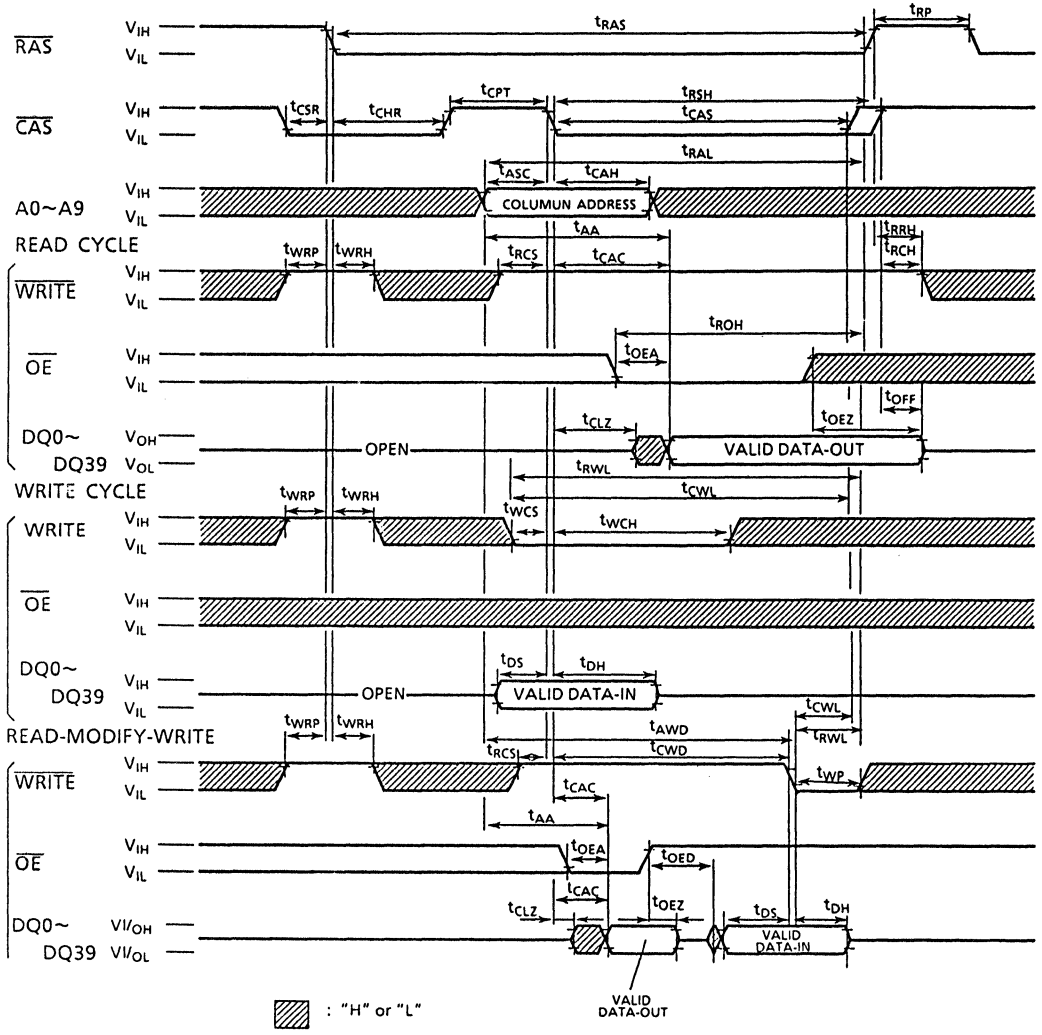
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE

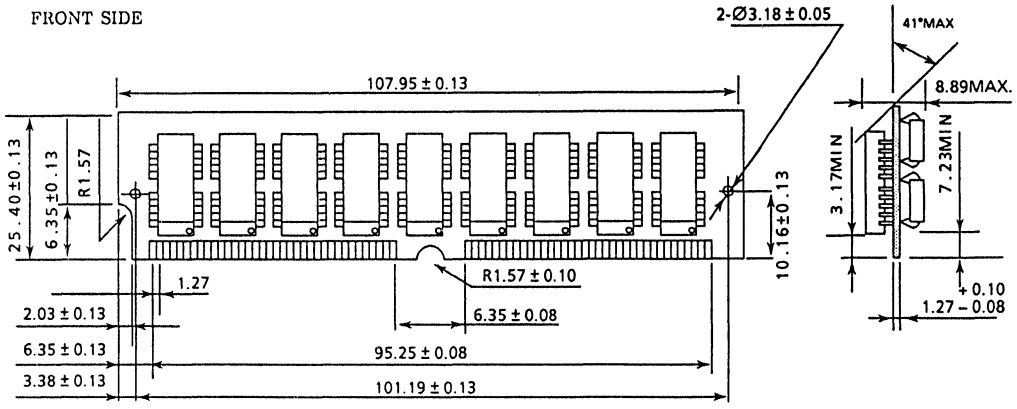


OUTLINE DRAWINGS

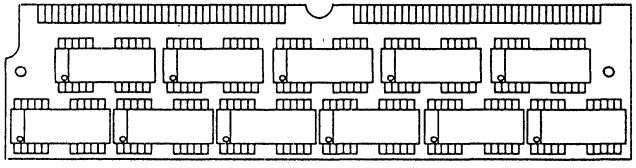
Unit in mm

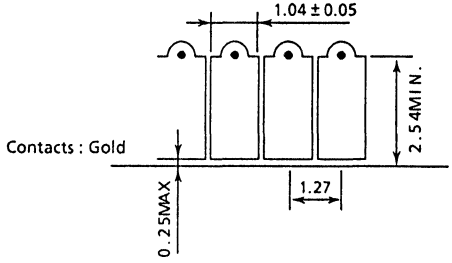
- THM402020SG

FRONT SIDE



BACK SIDE





NOTES

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