TOSHIBA

DATA BOOK

LOW VOLTAGE C²MOS LOGIC IC

1994

TC74LCX/LVQ/LVX SERIES

INTRODUCTION

Today's portable and battery-operated system designer is faced with the problem of keeping ahead when addressing system performance, long battery life, interfacing technology, and reliability. Toshiba's low voltage high performance C^2MOS logic families help designers achieve these goals.

TC74LCX SERIES: LOW VOLTAGE HIGH SPEED BUS DRIVER SERIES with 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX series has a propagation delay time of 4ns. Operation is guaranteed between 2V and 3.6V. The 24mA output drive current also makes it suitable for systems requirering higher driving capabilities.

A great feature of this family is its ability to operate at pure 3V or at both 3V and 5V in the same design without sacrificing performance. In addition to this, a power down protected I/O structure makes it possible to apply the signal to any I/O terminal even in a power down mode.

TC74LVQ SERIES: LOW VOLTAGE HIGH SPEED LOGIC SERIES with EQUIVALENT SPEED OF SCHOTTKEY TTL

The TC74LVQ series has been developed based on the 5V Advanced CMOS (AC) logic technology; the device performance is tuned to achieve better low voltage performance.

This series contains well known gates, flip - flops, MSI functions, and octals. Typical propagation delay time of the family is 6ns, and guaranteed output drive current is 12mA.

Since the design and process technology of this family is well established within Toshiba, the designer will be able to get highly reliable parts from the first design.

TC74LVX SERIES: LOW VOLTAGE HIGH SPEED LOGIC SERIES with INPUT LEVEL TRANSLATION CAPABILITY

The TC74LVX series of products were developed from the 5V VHC logic series. The series has a propagation delay time of 6.6ns, and the guaranteed output drive is 4mA.

This series also contains gate, flip - flops, MSI functions, and octals.

The TC74LVX series assures easy speed upgrades-(2 times) for sockets using HCMOS-which operates in excess of 30ns at low voltage. It's a time saving, cost effective selution to last minute product enhancements.

This data book presents technical information on TOSHIBA's TC74LCX / LVQ / LVX series.

The information contained herein is subject to change without notice.

TOSHIBA CORPORATION

MAY. 1994

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1-2 TC74LVQ / LVX Series Selection Guide

Function		Type No.	
		TC74LVQ Series	TC74LVX Series
GATE	NAND	LVQ00	LVX00
	NOR	LVQ02	LVX02
	AND	LVQ08	LVX08
	OR	LVQ32	LVX32
	INVERTER, BUFFER	LVQ04	LVX04
	EXCLUSIVE OR	LVQ86	LVX86
	SCHMITT TRIGGER	LVQ14	LVX14
BUFFER	BUS BUFFER	LVQ240, LVQ241, LVQ244	LVX125, LVX240, LVX244
	BUS TRANSCEIVER	LVQ245	LVX245
FLIP-FLOP	D-TYPE FLIP-FLOP	LVQ74, LVQ174, LVQ273	LVX74, LVX174, LVX273
	3-STATE	LVQ374	LVX374
LATCH	3-STATE	LVQ373, LVQ573	LVX373, LVX573
DECODER		LVQ138	LVX138
MULTIPLEXER (DIGITAL)		LVQ151, LVQ157	LVX157

2. PRODUCT OUTLINE OF THE TC74LVQ/LVX SERIES

2-1 Product Outline of The TC74LVQ / LVX Series

The TC74LVQ / LVX series has the following features.

(1) High Speed Operation: $tp_{LH} / tp_{HL} = 5ns$ (TYP.)
@$V_{CC} = 3.3V$, $C_L = 15pF$ (GATE)
$f_{MAX} = 150MHz$ (TYP.)
@$V_{CC} = 3.3V$, $C_L = 15pF$ (F / F)

(2) OUTPUT CURRENT: $|I_{OH}| / I_{OL} = 12mA$ (LVQ series)
$|I_{OH}| / I_{OL} = 4mA$ (LVX series)

(3) Low Power Dissipation: Same as high speed CMOS (74AC. 74HC) series.

(4) Ample Latch up Capacity: Total inputs and outputs ±300mA and above.

(5) Self-contained static electricity protective circuit:
±2000V (typ.) by MIL-STD-883 method
(All inputs and outputs.)

(6) Input voltage: $V_{IL} = 0.8V$ @$V_{CC} = 3V$ (Max.)
$V_{IH} = 2.0V$ @$V_{CC} = 3V$ (Min.)

(7) Low Noise: $V_{OLP} = 0.8V$ (Max.)

(8) 5-3V Level Shift (LVX series only): Power Down Protection is provided on all inputs.

(9) Package: JEDEC SOP, EIAJ SOP and SSOP

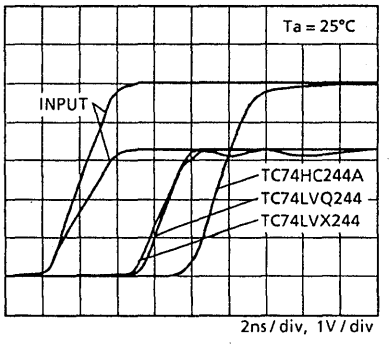
Table 2-1 Comparison of Logic Family Characteristics

Parameter	Symbol	3.3V Logic		5V Logic			unit	Test Condition
		LVQ Series (74LVQxxx)	LVX Series (74LVXxxx)	HC Series (74HCxxxA)	LS-TTL (74LSxxx)	ALS-TTL (74ALSxxx)		
Propagation Delay Time BUS BUFFER (244) typ.	t_{pd}	6.5	7.2	11	12	6.5	ns	Vcc = 3.3V (3.3V Logic) Vcc = 5V (5V Logic) Ta = 25°C CL = 50pF
Maximum Clock Frequency D-F / F (74) typ.	f_{MAX}	130	85	65	30	50	MHz	
Quiescent Power Dissipation GATE typ.	P_D	0.01μ	0.01μ	0.01μ	2m	5m	W	
Input Leakage Current GATE	I_{IH} I_{IL}	1.0 −1.0	1.0 −1.0	1.0 −1.0	20 −400	20 −200	μA	Over temp. and voltage range
Input Voltage	V_{IH} V_{IL}	2.0 0.8	2.0 0.8	3.5 1.5	2.0 0.8	2.0 0.8	V	Vcc = 3V (3.3V Logic) Vcc = 5V (5V Logic) Over temp. range
Output Current	I_{OH} I_{OL}	−12 12	−4 4	−4 / −6 4 / 6	−0.4 / −3 8 / 24	−0.4 / −3 8 / 24	mA	Vcc = 3V (3.3V Logic) Vcc = 4.5V (5V Logic) Over temp. range
Supply Voltage Range	Vopr.	2.0 ~ 3.6	2.0 ~ 3.6	2.0 ~ 6.0	4.75 ~ 5.25	4.5 ~ 5.5	V	
Operating Temperature	Ta	−40 ~ 85	−40 ~ 85	−40 ~ 85	0 ~ 70	0 ~ 70	°C	

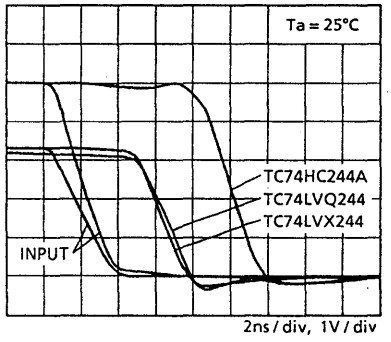
2-2 Featuers

(1) High Speed / Low Voltage Operation

The TC74LVQ / LVX series offer outstanding performance at low voltages such as V_{CC} = 3.3V when compared with 5V high speed logic families such as 74HC series, LS-TTL, etc. This is due to its delicated CMOS process technology. (refer to Fig. 2-1) And the TC74LVQ series offer high speed operation even under heavy load capacitance due to its lower output impedance. (refer to Fig. 2-2)



Condition
TC74LVQ244 V_{CC} = 3.3V, C_L = 15pF, R_L = 500Ω
TC74LVX244 V_{CC} = 3.3V, C_L = 15pF
TC74HC244A V_{CC} = 5.0V, C_L = 15pF



Condition
TC74LVQ244 V_{CC} = 3.3V, C_L = 15pF, R_L = 500Ω
TC74LVX244 V_{CC} = 3.3V, C_L = 15pF
TC74HC244A V_{CC} = 5.0V, C_L = 15pF

Fig. 2-1 Propagation Delay Time Comparison. (74LVQ, LVX and 74HC)

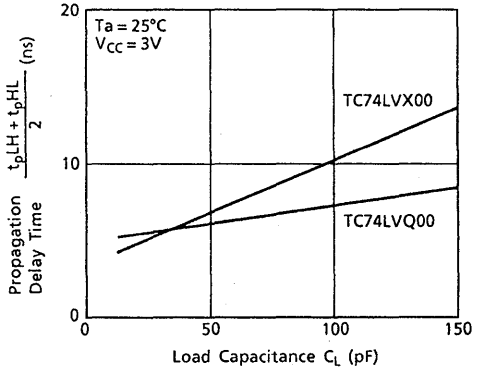


Fig. 2-2 Propagation Delay Time vs. Load Capacitance.

(2) Low Noise

The TC74LVQ / LVX series utilize Slew Rate Control (SRC) circuit which controls the output transition time in order to reduce the noise whith is generated at the time of output transition. This circuit effectively reduces noises such as the simultaneous switching noise, reflection noise of the transition line and so on. Fig. 2-3 shows the comparison of simultaneous switching noise.

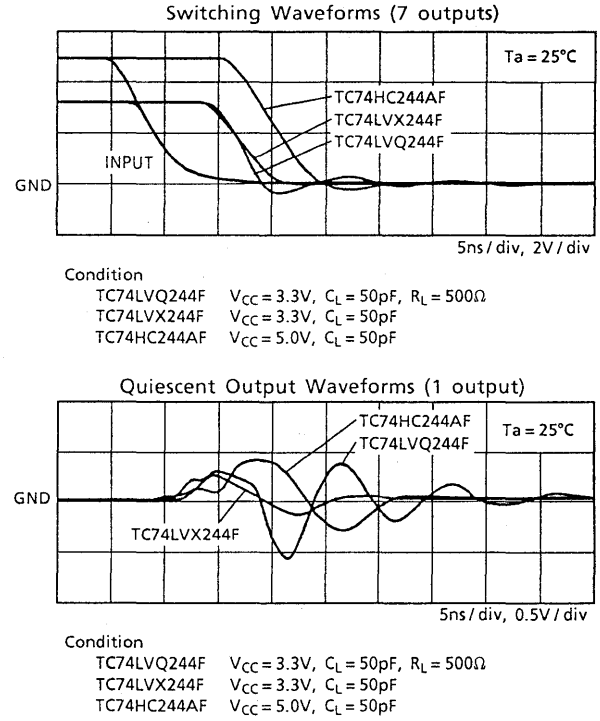
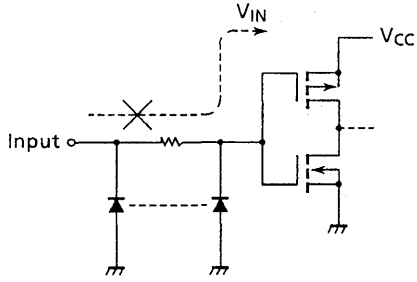


Fig. 2-3 Simultaneous Switching Noise Comparison. (74LVQ, LVX and 74HC)

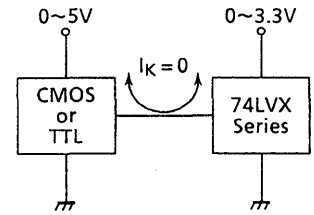
(3) Interface Ability (TC74LVX Series Only)

TC74LVX sevies utilizes no diode from input to V_{CC} for the input protection circuits (Fig.2-4). This allows up to 7V to be applied to the input regardless of the V_{CC} level. This power down protection circuit permits interfacing between systems which have different power supply voltages. For example, the TC74LVX series can be used for the applications such as level conversion from 5V to 3.3V (Except for the LVX 245), battery back up, etc. (Fig. 2-5)



- Even if the input voltage is higher than the power supply voltage, input current (I_{IN}) does not flow.

Fig. 2-4 Input Equivalent Circuit

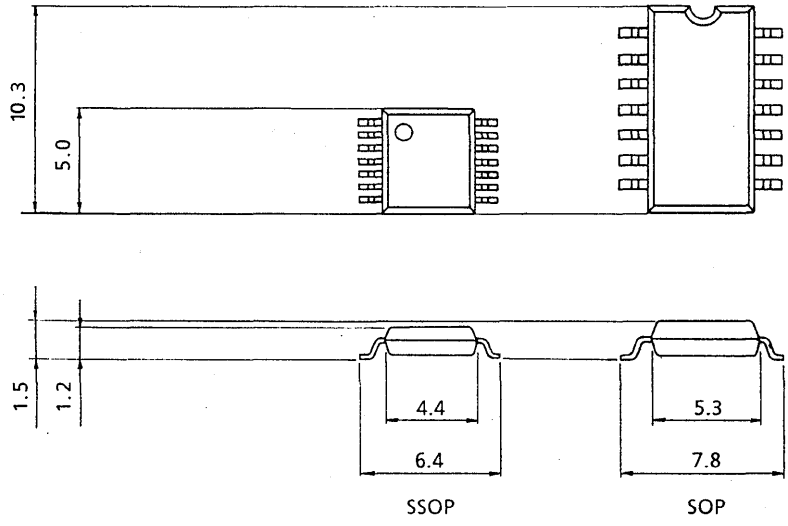


- Can be used for direct interfacing between 5 volt system and 3.3 volt system.
- Prevents device destruction due to mismatched supply and input voltages.

Fig. 2-5 Interface Ability

(4) Surface Mount Type Package (SOP, SSOP)

In addition to SOIC (JEDEC & EIAJ), SSOP which is a smaller, shrinked package is also available for the TC74LVQ / LVX series. Fig. 2-6 shows the comparison of the size between SOP and SSOP.



	SSOP	SOP
Ratio of board are a occupied when SOP = 1.0	0.40	1.00
Ratio of weight when SOP = 1.0	0.39	1.00

Fig. 2-6 Comparison of the size between SOP and SSOP (14pin type)

3. EXPLANATION OF RATINGS AND STANDARDS

3-1 Maximum Ratings

In general, the maximum rating value should not be exceeded in order to guarantee the life and reliability of integrated circuit products.

Absolute Maximum Ratings should not be exceed even for a moment.

When the device is used in excess of any maximum rating, the device may not recover, and in many cases, permanent damage will occur.

In designing the circuit, therefore, it is necessary to pay attention to fluctuations of supply voltage, characteristics of interconnecting parts, ambient temperature, and surges in input and output signal lines, and ensure that the maximum ratings will not be exceeded.

Table 3-1 indicates common absolute maximum ratings of TC74LVQ / LVX series. When individual maximum ratings and common ratings differ, the former shall control. For definitions of parameters, refer to Table 3-2.

Table 3-1 Absolute Maximum Ratings

(a) TC74LVQ Series

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC} / Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

(b) TC74LVX Series

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

Table 3-2

Parameter	Symbol	Explanation
Supply Voltage	V_{CC}	The voltage range in which the IC will not present breakdown, deterioration of characteristics or reduced reliability.
DC Input Voltage DC Output Voltage	V_{IN} V_{OUT}	The voltage range in which the IC will not present breakdown, deterioration of characteristics or reduced reliability.
Input Diode Current Output Diode Current	I_{IK} I_{OK}	The current value at which the IC will not present breakdown due to latch-up when input or output current flows. * Practically, the design in which DC current flows is not recommended. When this cannot be prevented, adopt a current value lower than this.
DC Output Current DC V_{CC}/Ground Current	I_{OUT} I_{CC}	Output current indicates the current value which can flow from one output. As V_{CC}/GND current includes output current, in an IC having multiple output terminals, substantial V_{CC}/GND current can flow.
Power Dissipation	P_D	Power consumption not causing breakdown of the over the entire operating temperature range.
Storage Temperature	T_{stg}	The ambient temperature range over which no deterioration of characteristics or a reliability occurs when left for a long time without supply voltage.
Lead Temp. and Time	T_L	The maximum time that the device may be subjected to the maximum lead temperature specified.

3-2 Recommended Operating Conditions

These are the conditions in which the operation of the TC74LVQ / LVX series is guaranteed, and when exceeded, operation is not guaranteed even if it is within the maximum rating of Table 3-1.

Commom recommended operating conditions of TC74LVQ series are shown in Table 3-3 (a). TC74LVX series are shown in Table 3-3 (b). When recommended operating conditions of each device and common recommended operating conditions differ, the former shall control. As to the meaning of each parameter, refer to Table 3-4.

Table 3-3 Common Recommended Operating Conditions

(a) TC74LVQ Series

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	Topr	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

(b) TC74LVX Series

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	Topr	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

Table 3-4

Parameter	Symbol	Explanation
Supply Voltage	V_{CC}	Supply voltage range guaranteeing normal operation of the IC.
Input Voltage Output Voltage	V_{IN} V_{OUT}	Supply voltage range guaranteeing normal operation of the IC.
Operating Temperature	Topr	Operating temperature range guaranteeing normal operation and electrical characteristics of the IC.
Input Rise and Fall Time	dt / dv	Rise and fall time range of input signal which will not cause malfunction due to oscillation of the output.

(1) Input circuit

When high voltage is applied to this gate electrode (input of CMOS IC), the oxide film directly under the gate sometimes breaks down. In TC74LVQ / LVX series, as shown in Fig. 3-1 protection circuit are added to all input terminals in order to protect the CMOS gate from such voltage.

TC74LVX series utilizes no diode from input to V_{CC} for the input protection circuits. This allows up to 7V to be applied to the input regardless of the V_{CC} level. This power down protection circuit permits interfacing between systems which have different power supply voltages. For example, the TC74LVX series can be used for the applications such as level conversion form 5V to 3.3V (Except for the LVX245), battery back up, etc. (Fig. 3-2)

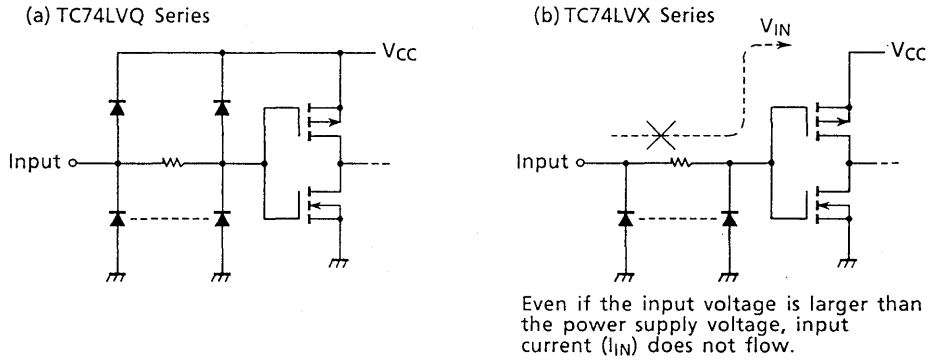


Fig. 3-1 Input Equivalent Circuit

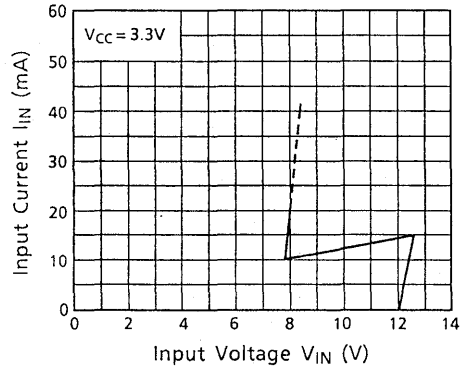


Fig. 3-2 Input Characteristics (TC74LVX Series)

3-3 DC Characteristics

Table 3-5 (a) shows DC characteristics of TC74LVQ series. For TC74LVX devices see Table 3-5(b).

For the meaning of each parameter, refer to Table 3-6. Table 3-5 is a standard DC characteristics table, and when it differ from individual characteristics, the later shall control.

In the TC74LVQ / LVX series, all devices meet or exceed this standard.

Table 3-5 DC characteristics

(a) TC74LVQ Series

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
3-State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND	GATE / SSI	3.6	—	—	2.5	—	25.0	μA
			MSI	3.6	—	—	4.0	—	40.0	μA

(b) TC74LVX Series

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0	1.5	—	—	1.5	—	V
				3.0	2.0	—	—	2.0	—	V
				3.6	2.4	—	—	2.4	—	V
Low - Level Input Voltage	V_{IL}			2.0	—	—	0.5	—	0.5	V
				3.0	—	—	0.8	—	0.8	V
				3.6	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
			I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	V
Low - level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	V
3-State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.25	—	±2.5	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND	GATE / SSI	3.6	—	—	2.0	—	20.0	μA
			MSI	3.6	—	—	4.0	—	40.0	μA

Table 3-6

Parameter	Symbol	Explanation
High - Level Input Voltage	V_{IN}	This is an input voltage capable of setting the input of the IC to a high level, and the minimum value is guaranteed. Judgment in this case is made by confirming that it is above the prescribed V_{OH} when output voltage should be at a high level, and below the prescribed V_{OL} when output voltage should be at a level.
Low - Level Input Voltage	V_{IL}	This is an input voltage capable of setting the input of the IC to a low level, and the maximum value is guaranteed. The method of judgment is the same as V_{IH}.
High - Level Output Voltage	V_{OH}	This is an output voltage such that when each input terminal is connected to V_{IH} or V_{IL}, the output level goes high. In this case, there is guaranteed a minimum value of output voltage obtainable when the specified output current (I_{OH}) flows out.
Low - level Output Voltage	V_{OL}	This is an output voltage such that when each input terminal is connected to V_{IH} or V_{IL}, the output level goes low. In this case, there is guaranteed a maximum value of output voltage obtainable when the specified output current (I_{OL}) flows out.
Input Leakage Current	I_{IN}	This is the current flowing at the input terminal when a voltage is impressed on the input terminal of IC. Normally, this current is so small that measurement is made with the maximum value of supply voltage.
3-State Output Off - State Current	I_{OZ}	This is the leakage current flowing at the output terminal when the output is in a high impedance state, the device having a three state output.
Quiescent Supply Current	I_{CC}	This is the current flowing from V_{CC} terminal into the IC when V_{CC} or GND level is held constant without changing the input voltage. The maximum value under all theoretical conditions allowable for the measured IC is guaranteed.

(1) Output Current Characteristics

The TC74LVQ series and TC74LVX series guarantee ±12mA drive current and ±4mA drive current, respectively (at V_{CC} = 3.3V, V_{OH} = 2.48V, V_{OL} = 0.44V) for both I_{OH} and I_{OL}. The designer can use either the TC74LVQ series or the TC74LVX series depends on the impedance conect to the output.

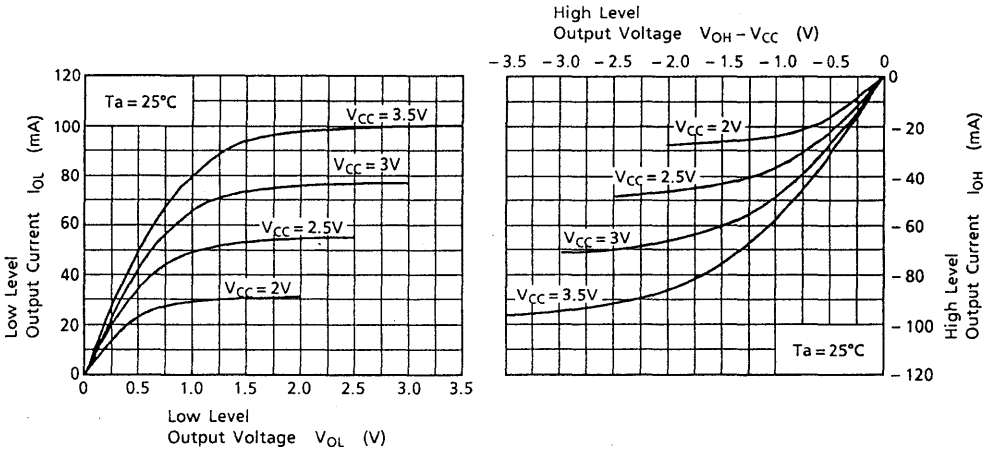


Fig. 3-3 Output Current Characteristics of TC74LVQ Series (typical)

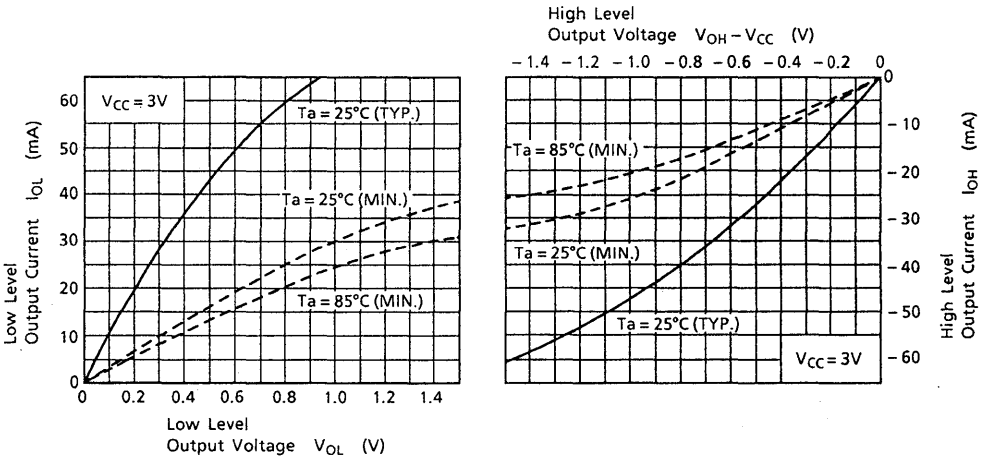


Fig. 3-4 Output Current Characteristics of TC74LVQ Series

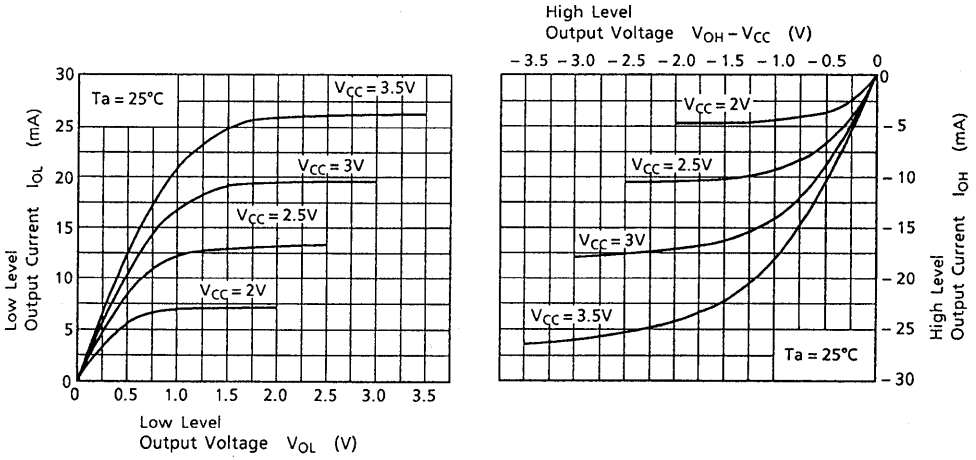


Fig. 3-5 Output Current Characteristics of TC74LVX Series (typical)

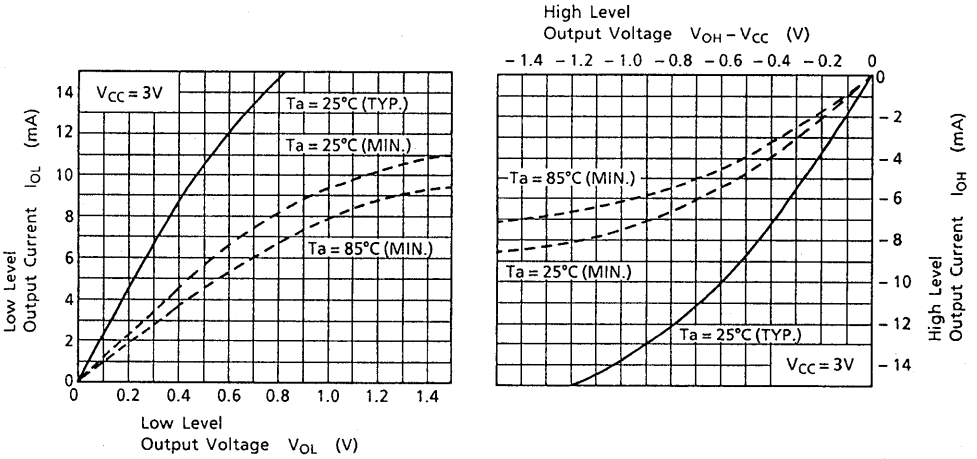


Fig. 3-6 Output Current Characteristics of TC74LVX Series

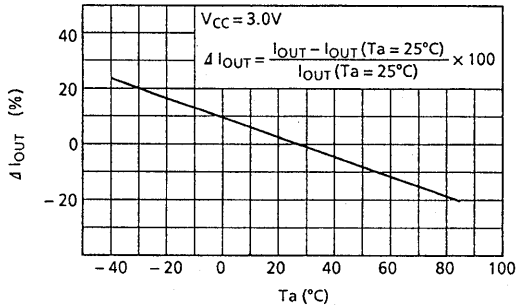


Fig. 3-7 Temperature vs. Output Current (typical)

3-4 AC Characteristics

AC characteristics guarantee transient characteristics of TC74LVQ / LVX products.

In general, the impressed input waveform is set so as to have an amplitude of V_{CC} to GND and rise and fall time of 3ns.

Table 3-7 explains the meaning of each parameter of the AC characteristics, Fig. 3-8 shows the output connection diagrams for measurement and Fig. 3-9 illustrates the measured waveforms.

Table 3-7

Parameter	Symbol	Explanation	Figure 3-9	
			LVQ	LVX
Propagation Delay Time	t_{PLH} t_{PHL}	The time between input signal application and output response detection. t_{PLH} is the case in which the output changes from low to high, and t_{PHL} is the case in which the output changes from high to low.	(i)	(iv)
Output Disable Time	t_{PLZ} t_{PHZ}	The time, between when signal is applied to the output control terminal and the 3-state output is set to a high impedance state.	(iii)	(vi)
Output Enable Time	t_{PZL} t_{PZH}	The time, between when signal is applied to the output control terminal and the 3-state output goes low or high from the high impedance state.		
Output Skew	t_{osLH} t_{osHL}	It is defined as the absolute value of difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either Low to High (t_{osLH}) or High to Low (t_{osHL}).	—	—
Maximum Clock Frequency	f_{MAX}	The maximum frequency at which the IC operates normally.	(ii)	(v)

Timing requirements are a prerequisite to the normal function of devices. (See Table 3-8)

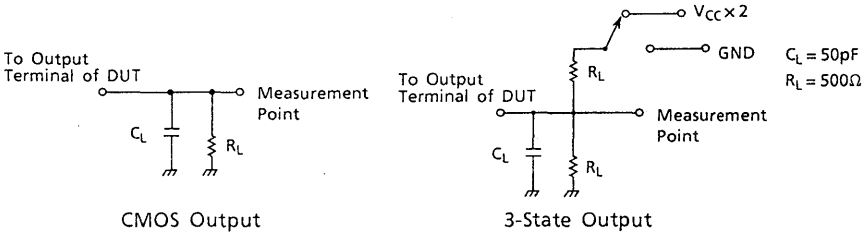
Table 3-8

Parameter	Symbol	Explanation	Figure 3-9	
			LVQ	LVX
Minimum Set-up Time	t_s	Regarding certain data, indicates the time in which the data must be applied and held before the input regarding that data (clock, etc.) changes. For example, when the data is read in at a rise of next clock pulse, it is necessary to apply data before the rising edge of the clock pulse, to a value at least equal to the minimum value of ts.	(ii)	(v)
Minimum Hold Time	t_h	Regarding certain data, indicates the time in which the data must be held after the input regarding that data (clock, etc.) has changed.		
Minimum Removal Time	t_{rem}	Indicates the minimum time after releasing of an asynchronous input (clear, preset, etc.) and until application of next input (clock, etc.).		
Minimum Pulse Width	t_w	Indicates the minimum pulse width that a clock input, etc. is acceptable as a normal signal.		

Parameter	Symbol	Explanation
Input Capacitance	C_{IN}	Indicates the capacitance between input and GND.
Output Capacitance	C_{OUT}	Indicates the capacitance associated with a 3-state output or a open drain output in the high impedance state.
Power dissipation Capacitance	C_{PD}	This is the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance.

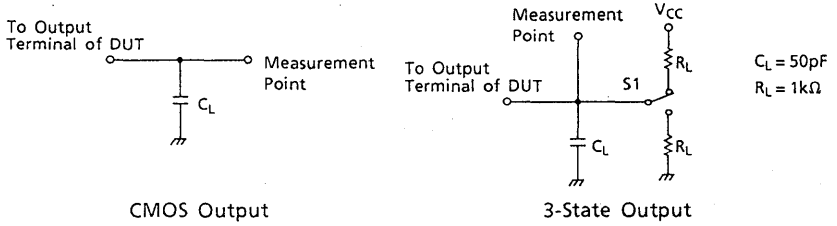
Fig. 3-8 Output Connection Diagram

(a) TC74LVQ series



Note) C_L includes the capacitance of probe, etc.

(b) TC74LVX series

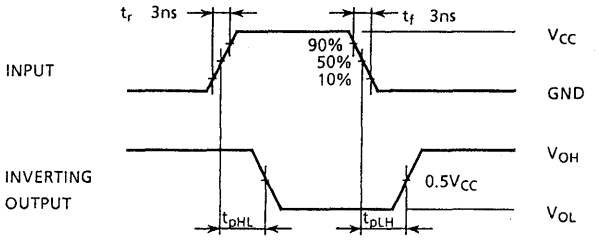


Note) C_L includes the capacitance of probe, etc.

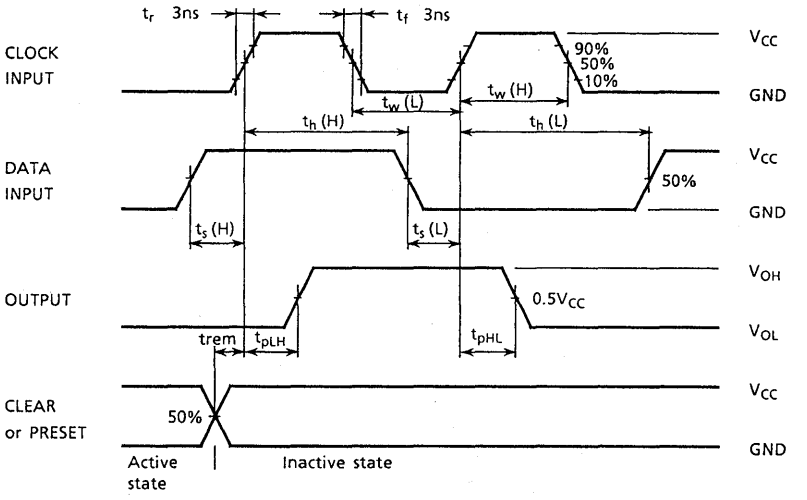
Fig. 3-9 Switching Characteristic Test Waveforms

(a) TC74LVQ series

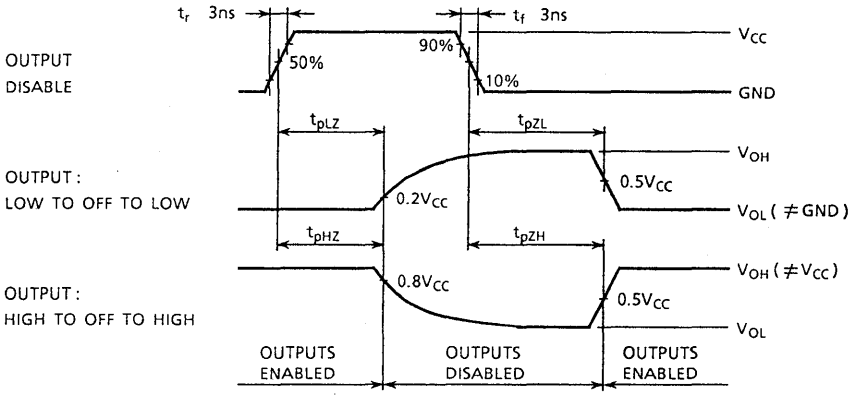
(i) t_{pLH} , t_{pHL}



(ii) t_w , t_s , t_h , t_{rem}

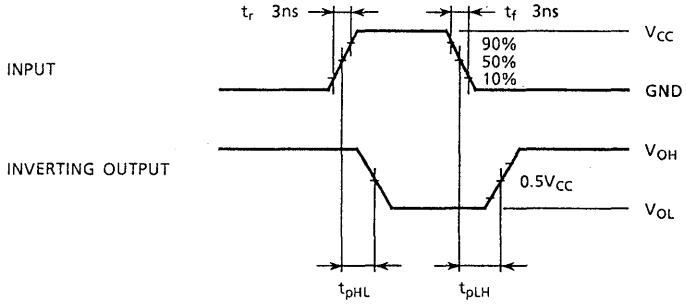


(iii) t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

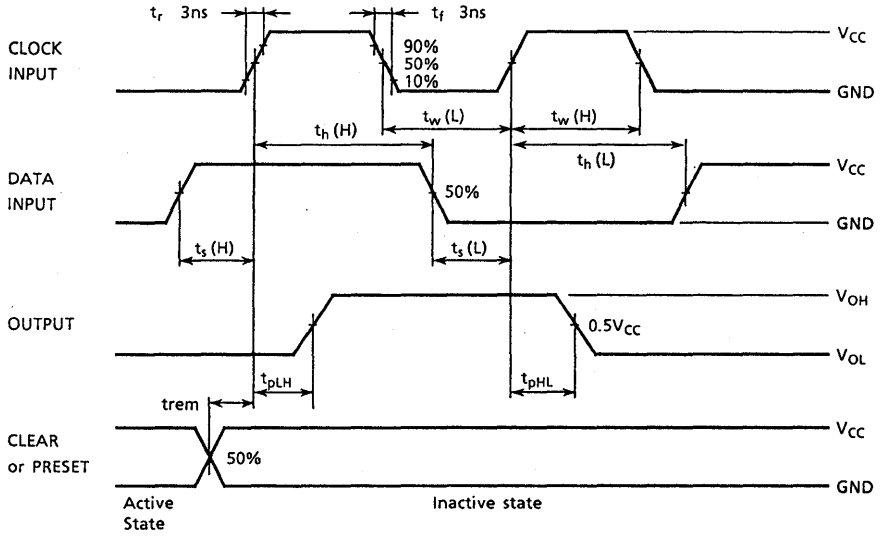


(b) TC74LVX series

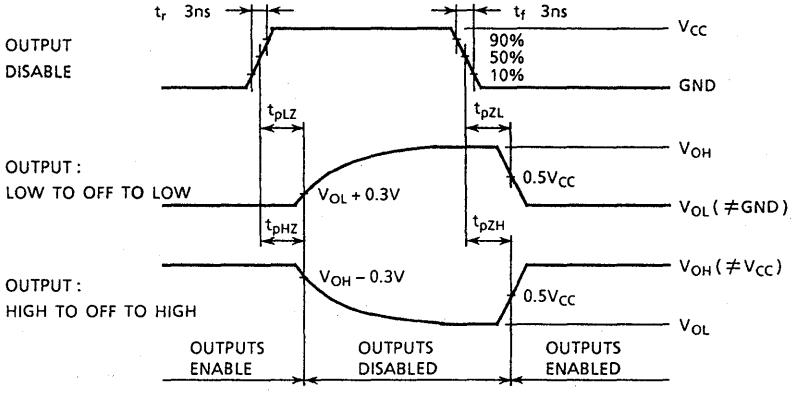
(iv) t_{pLH} , t_{pHL}



(v) t_w , t_s , t_h , t_{rem}



(vi) t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}



(1) Load Capacitance Characteristics of Propagation Delay Time.

In the TC74LVQ / LVX series, AC characteristics are guaranteed using a load capacitance of 50pF and 15pF (LVX only). Propagation delay time using load capacitance, other than the above is obtained by the following equation:

Propagation delay time in the case of load capacitance of XpF.

$$t_{pd}(X) = A(X - 50) + t_{pd}(50)$$

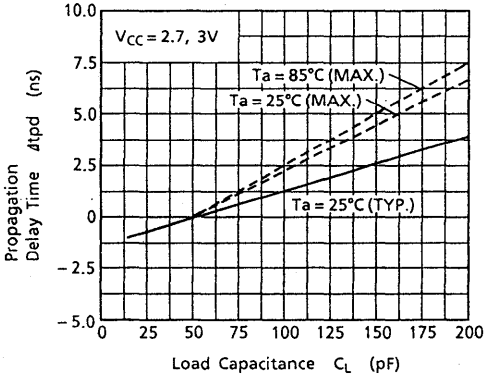
A: Propagation delay time increase rate per unit load capacitance (ns / pF)

Fig.3-10 shows propagation delay time vs. load capacitance at both $V_{CC} = 3V$ and $V_{CC} = 2.7V$, in a range exceeding 50pF.

The dotted line should be used by the designer due consideration of propagation delay time.

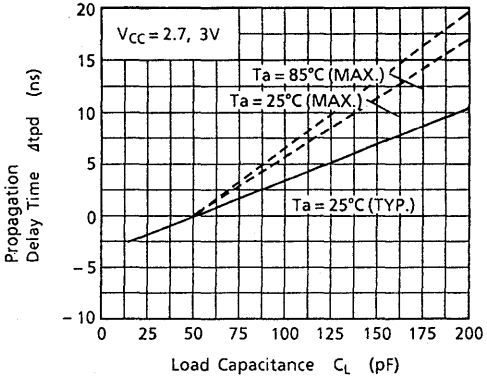
However guaranteed value is only the value specified at $C_L = 50pF$ or $C_L = 15pF$ (LVX only) in the individual Spec. Sheet.

(a) TC74LVQ Series



Propagation delay time increase rate per unit load capacitance
Ta = 25°C (TYP.) A = 0.026 (ns / pF)
Ta = 25°C (MAX.) A = 0.045 (ns / pF)
Ta = 85°C (MAX.) A = 0.05 (ns / pF)

(b) TC74LVX Series



Propagation delay time increase rate per unit load capacitance.
Ta = 25°C (TYP.) A = 0.07 (ns / pF)
Ta = 25°C (MAX.) A = 0.115 (ns / pF)
Ta = 85°C (MAX.) A = 0.13 (ns / pF)

Fig. 3-10 Propagation Delay Time vs. Load Capacitance.

(2) Temperature Characteristics Versus Propagation Delay Time

Fig. 3-11 shows temperature versus propagation delay time. The solid line in this figure indicates standard temperature dependence at the Gate of the IC.

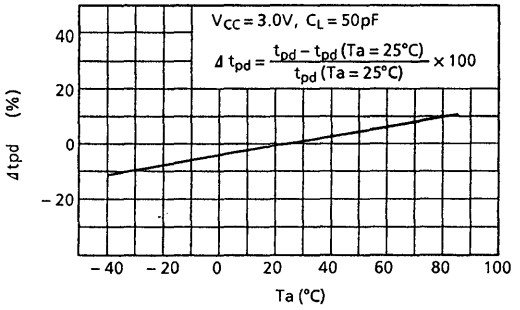


Fig.3-11 Temperature vs. Propagation Delay Time (typical)

(3) Output Skew Characteristics

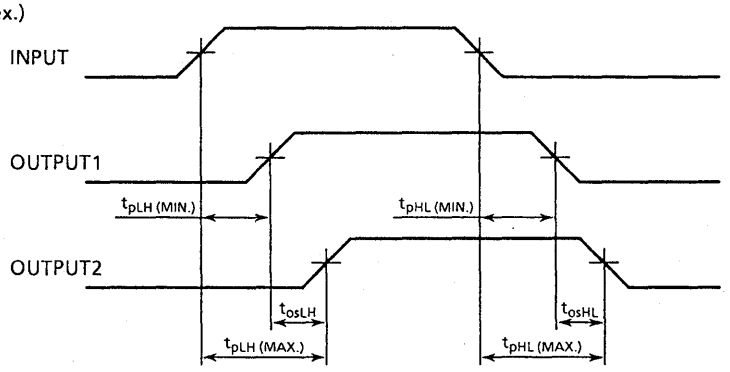
Output skew characteristics of TC74LVQ / LVX products.

This parameter guaranteed by design.

$t_{osLH} = |t_{pLH\,(MAX.)} - t_{pLH\,(MIN.)}|$

$t_{osHL} = |t_{pHL\,(MAX.)} - t_{pHL\,(MIN.)}|$

ex.)



(4) Power Dissipation

The power dissipation of CMOS device is composed of two components: static and dynamic.

The total power dissipation is the sum of static and dynamic power dissipation.

Static power dissipation is obtained by multiplying quiescent supply current by the supply voltage range.

Dynamic power dissipation is obtained through a more complex calculation described in paragraph below.

(a) Static power dissipation

In the case of CMOS ICs, under the condition in which inputs are fixed at V_{CC} or GND, either the N-channel FET or the P-channel FET turns off. For this reason, the current from V_{CC} to GND becomes only the reverse direction saturated current of the PN junction and the surface leakage current due to the stain in the chip surface, and is less than several nA at room temperature.

However, when the inputs are driven by another COMS IC, or the inputs are pulled-down to GND or pulled-up to V_{CC}, the static power dissipation is obtained as follows:

$$P_d\,(DC) = V_{CC} \cdot I_{CC}$$

(b) Dynamic power dissipation

The dynamic power dissipation of a MOS IC is calculated by summing a) and b) below:

a) The switching current obtained by charge and discharge of each capacitance added to gate output current when the gate in the circuit including the output buffer makes an inversion.

b) The through current flowing when the P-channel FET and the N-channel FET which constitute the gate during inversion time turn on briefly at the same time.

When rise and fall times of the input signal are small (about 3ns), through current of the gate is usually negligibly small in comparison with the switching current.

For this reason, the dynamic supply current is governed by internal capacitance of the IC and the charging and discharging current of the load capacity (C_L).

An example is given hare for $C_L = 0pF$.

For the inversion of internal gate outputs from low to high level, it is necessary that the electric charge corresponding to $Ci \cdot V_{CC}$ be supplied from the V_{CC} line to the internal capacitance Ci.

Therefore the value obtained by multiplying $Ci \cdot V_{CC}$ to the output inversion frequency (frequency : f) within a certain period corresponds to the mean current to be supplied from the Vcc line to the IC during that period.

In an actual IC, several gates operate simultaneously, and their respective internal capacity and inversion frequency are different.

Therefore, dynamic supply current in an IC is as follows:

$$I_{CC\,(opr.)} = V_{CC} \cdot \sum_{1}^{n} f_n \cdot C_{in}$$

fn : frequency of internal operated gate

As fn is divisible by an integer of input frequency (f_{IN}), the gate operating with fn / m frequency can be considered equivalent to the capacitance of Ci / m.

Hence, the above equation can by rewritten as:

$$I_{CC\,(opr.)} = V_{CC} \cdot f_{IN} \cdot \sum_{1}^{n} Ci / m_n$$

f_{IN} : input frequency

m : integer

The final term is defined as C_{PD}.

Dynamic power dissipation with load capacity is given by the following equation:

$$P_{D\,(opr.)} = C_{PD} \cdot V_{CC}^2 \cdot f_{IN} \cdot C_{PD}$$

Total dynamic power dissipation with load capacity is given by the following equation:

$$P_{D\,(opr.)} = C_{PD} \cdot V_{CC}^2 \cdot f_{IN} + \sum_{1}^{n} (C_{Ln} \cdot V_{CC}^2 \cdot f_{On})$$

C_L : load capacity

f_O : output frequency

n : integer of output

However, in specific applications such as crystal oscillators, supply current characteristics are controlled by through current, and the calculation result using C_{PD} can not be used.

(5) Standardized Capacitance Power Dissipation (C_{PD}) Test Procedure

The purpose of the C_{PD} value is to allow the user to estimate actual power consumption of his system. The table has been set up to exercise each device in the same manner as it would usually be used. Devices which are separable into independent sections are measured on a "per section" basis, the remaining are measured on a "per device" basis. Each devices unique set up is listed in the Table 3-9, "Pin Condition Table".

Measurements for all devices are to be made at $V_{CC} = 3.3V$ at $Ta = 25°C$ and, if the devices are tested at a high enough frequency, the DC supply current will contribute a negligible amount to the overall power consumption and can be ignored. For this reason, power consumption is measured at 1MHz.

Devices with 3-state outputs are measured in the enabled state.

Table 3-9 C_{PD} Test Conditions

TYPE NO.		Pin																									
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
00		P	H	C	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•	•	•	•	•
02		C	P	L	O	X	X	G	X	X	O	X	X	O	V	•	•	•	•	•	•	•	•	•	•	•	•	•	•
04		P	C	X	O	X	O	G	O	X	O	X	O	X	V	•	•	•	•	•	•	•	•	•	•	•	•	•	•
08		P	H	C	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•	•	•	•	•
14		P	C	X	O	X	O	G	O	X	O	X	O	X	V	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32		P	L	C	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•	•	•	•	•
74		H	Q	P	H	C	C	G	O	O	X	X	X	X	V	•	•	•	•	•	•	•	•	•	•	•	•	•	•
86		P	L	C	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•	•	•	•	•
125		L	P	C	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•	•	•	•	•
138		P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	•	•	•	•	•	•	•	•	•	•	•	•
151		X	X	L	H	C	C	L	G	L	L	P	X	X	X	X	V	•	•	•	•	•	•	•	•	•	•	•	•
157	1*	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	•	•	•	•	•	•	•	•	•	•	•	•
157	4*	P	L	H	C	L	H	C	G	C	H	L	C	H	L	L	V	•	•	•	•	•	•	•	•	•	•	•	•
174	1*	H	C	Q	X	O	X	O	G	P	O	X	O	X	X	O	V	•	•	•	•	•	•	•	•	•	•	•	•
174	6*	H	C	Q	Q	C	Q	C	G	P	C	Q	C	Q	Q	C	V	•	•	•	•	•	•	•	•	•	•	•	•
240		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	C	X	V	•	•	•	•	•	•	•	•
241		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	C	X	V	•	•	•	•	•	•	•	•
244		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	C	X	V	•	•	•	•	•	•	•	•
245		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	C	L	V	•	•	•	•	•	•	•	•
273	1*	H	C	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•	•	•	•	•
273	8*	H	C	Q	Q	C	C	Q	Q	C	G	P	C	Q	Q	C	C	Q	Q	C	V	•	•	•	•	•	•	•	•
373	1*	L	C	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•	•	•	•	•
373	8*	L	C	Q	Q	C	C	Q	Q	C	G	P	C	Q	Q	C	C	Q	Q	C	V	•	•	•	•	•	•	•	•
374	1*	L	C	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•	•	•	•	•
374	8*	L	C	Q	Q	C	C	Q	Q	C	G	P	C	Q	Q	C	C	Q	Q	C	V	•	•	•	•	•	•	•	•
573	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	C	V	•	•	•	•	•	•	•	•
573	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	C	C	C	C	C	C	C	C	V	•	•	•	•	•	•	•	•

* : number of sections active

— Explanation of symbol —

V = V_{CC} (+ 3.3V)

G = GND (0V)

H = logic 1 (V_{CC})

L = logic 0 (GND)

X = don't care. V_{CC} or GND. but not switching

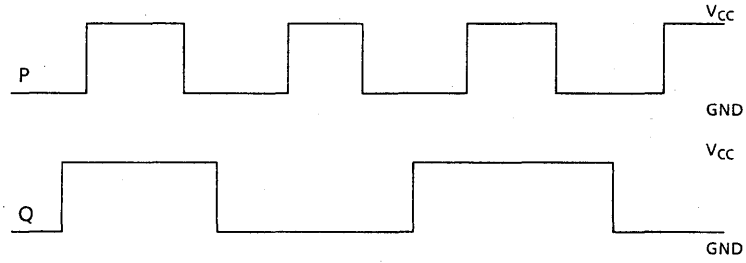
R = 1.0kΩ pull-up resistor to an additional 3.3V supply other than V_{CC} supply

O = open

C = 50pF load to GND.

P = 50% duty cycle input pulse. (shown below)

Q = 50% duty cycle half frequency out-of-phase input pulse (shown below)



Input Pulse Waveforms

3-5 Noise Characteristics

Noise characteristics caused by high-speed switching are specified for the TC74LVQ / LVX series.

These noise are generated by rush current flowing through the internal V_{CC} or GND lines of the devices when several outputs are switching simultaneously.

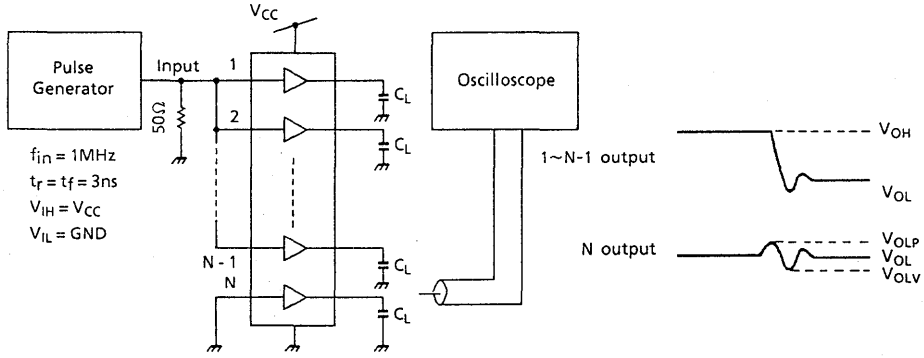
For the meaning of each parameter, refer to Table 3-10.

Fig. 3-12 shows the Noise Characteristics Measurement Circuit.

Table 3-10

Parameter	Symbol	Explanation
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	Maximum peak voltage induced into the output which is fixed at GND level when the other outputs are switching simultaneously.
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	Minimum peak voltage induced into the output which is fixed at GND level when the other outputs are switching simultaneously.
Minimum High Level Dynamic Input Voltage V_{IHD}	V_{IHD}	High level dynamic threshold voltage when all outputs are switching simultaneously.
Maximum Low Level Dynamic Input Voltage V_{ILD}	V_{ILD}	Low level dynamic threshold voltage when all inputs are switching simultaneously.

(1) Quiet Output Dynamic V_{OLP}, V_{OLV} Measurement Circuit



(2) Dynamic Input Voltage V_{IHD}, V_{ILD} Measurement Circuit

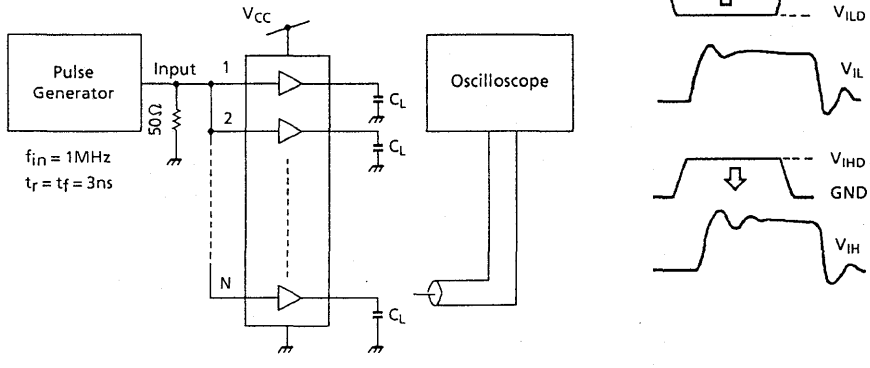


Fig. 3-12 Noise Characteristics Measurement Circuit

4. LOGIC SYMBOL AND TRUTH TABLE

4-1 How to Read MIL Type Logic Symbols

Table 4-1 shows the MIL type logic symbols used in high-speed CMOS IC. This logical chart is based on MIL-STD-806. Clocked inverter and transmission gate employ specific symbols.

Table 4-1 MIL Logic Symbols

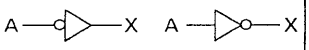
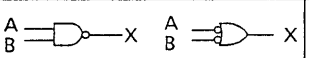
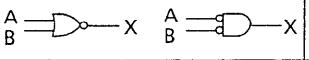
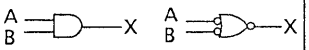
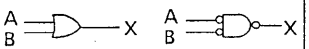
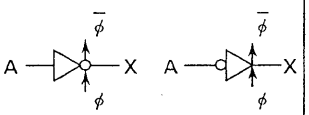
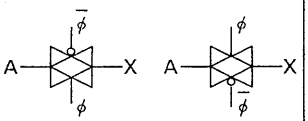
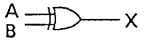
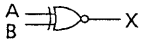
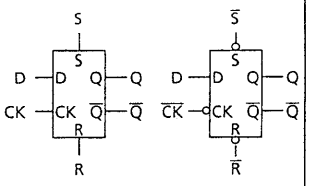
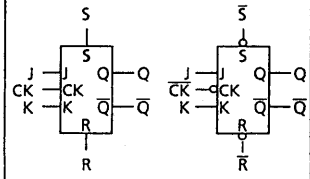
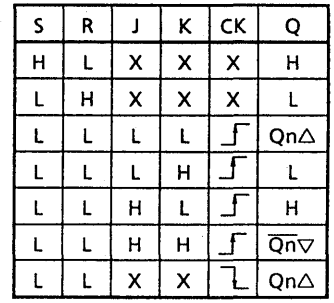
<table>
<tr><th>Circuit Function</th><th>Logic Symbols</th><th>Logical Equation or Truth Table</th></tr>
<tr><td>Inverter</td><td>  </td><td>$X = \overline{A}$</td></tr>
<tr><td>NAND Gate</td><td>  </td><td>$X = \overline{A \cdot B} = \overline{A} + \overline{B}$</td></tr>
<tr><td>NOR Gate</td><td>  </td><td>$X = \overline{A + B} = \overline{A} \cdot \overline{B}$</td></tr>
<tr><td>AND Gate</td><td>  </td><td>$X = A \cdot B = \overline{\overline{A} + \overline{B}}$</td></tr>
<tr><td>OR Gate</td><td>  </td><td>$X = A + B = \overline{\overline{A} \cdot \overline{B}}$</td></tr>
<tr><td>Clocked Inverter
(Note 1)</td><td>  </td><td>
<table>
<tr><th>ϕ</th><th>A</th><th>X</th></tr>
<tr><td>H</td><td>H</td><td>L</td></tr>
<tr><td>H</td><td>L</td><td>H</td></tr>
<tr><td>L</td><td>X</td><td>Z</td></tr>
</table>
X : Don't Care
Z : High Impedance
</td></tr>
<tr><td>Transmission Gate
(Note 2)</td><td>  </td><td>
<table>
<tr><th>ϕ</th><th>A</th><th>X</th></tr>
<tr><td>H</td><td>H</td><td>H</td></tr>
<tr><td>H</td><td>L</td><td>L</td></tr>
<tr><td>L</td><td>X</td><td>Z</td></tr>
</table>
X : Don't Care
Z : High Impedance
</td></tr>
<tr><td>EXCLUSIVE-OR Gate</td><td>  </td><td>$X = (A + B) \cdot (\overline{A} + \overline{B})$</td></tr>
<tr><td>EXCLUSIVE-NOR Gate</td><td>  </td><td>$X = (A \cdot B) + (\overline{A} \cdot \overline{B})$</td></tr>
<tr><td>D-Type Flip-Flop</td><td>  </td><td>
<table>
<tr><th>S</th><th>R</th><th>D</th><th>CK</th><th>Q</th></tr>
<tr><td>H</td><td>L</td><td>X</td><td>X</td><td>H</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>X</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>↑</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>↑</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>↓</td><td>Qn△</td></tr>
</table>
X : Don't Care
△ : No Change
</td></tr>
</table>

Table 4-1 (Cont'd)

Circuit Function	Logic Symbol	Logical Equation or Truth Table
J/K Type Flip-Flop		

S	R	J	K	CK	Q
H	L	X	X	X	H
L	H	X	X	X	L
L	L	L	L	↓	Qn△
L	L	L	H	↓	L
L	L	H	L	↓	H
L	L	H	H	↓	$\overline{Qn}$▽
L	L	X	X	↑	Qn△

X : Don't Care
△ : No Change
▽ : Toggle

Note 1) Clocked Inverter

A clocked inverter has the circuit shown in Fig. 4-1. In this figure, Q1 and Q2 are P-channel MOS FET, and Q3 and Q4 are N-channel MOS FET, and four FET are all connected in series from V_{CC} to GND.

If ϕ signal is at a high level, Q1 and Q4 turn on, and can be regarded as simply a inverter composed of Q2 and Q3. When ϕ signal is at a low level, both Q1 and Q4 turn off, and regurdless of the condition of the A input. the output, X is set to a high impedance condition cut off from both V_{CC} and GND.

That is to say, a clocked inverter can be used as a switch to turn off input and output.

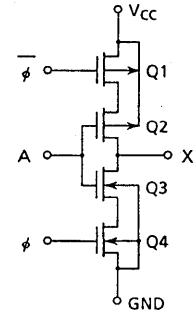


Fig. 4-1
Clocked Inverter

Note 2) Transmission Gate

A transmission gate has the circuit shown in Fig. 4-2. As shown in this figure, Q1 is a P-channel MOS FET and Q2 is an N-channel MOS FET which are connected in parallel. If ϕ signal is at a high level, both Q1 and Q2 turn on, and a signal can be applied in either direction. If ϕ signal is at a low level, both Q1 and Q2 turn off, and no signal can be passed.

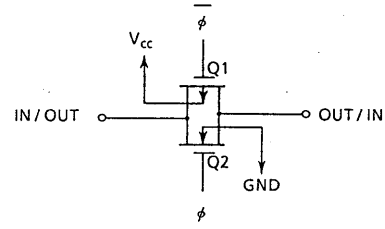


Fig. 4-2 Transmission Gate

4-2 How to Read a Truth Table

Table 4-2 indicates the definitions of symbols described in Truth Tables.

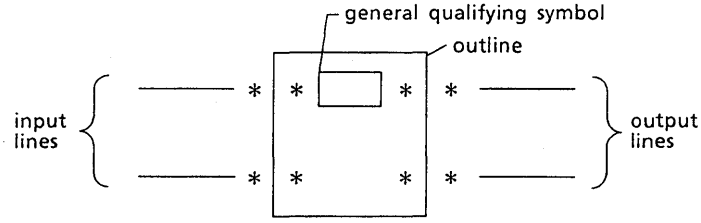
Table 4-2

Symbol	definition
H	High level (Indicates stationary input or output)
L	Low level (Indicates stationary input or output)
⎍	Indicates leading edge changing from "L" to "H"
⎏	Indicates trailing edge changing from "H" to "L"
X	Don't care (Either "H" or "L")
Z	High impedance state
a ····· h	Input level of stationary state of each input of A to H
Q_0	Level of Q just before the realization of input condition indicated in Truth Table.
Qn	Level of Q just before inputting of active edge (⎍ or ⎏)
⎍⎏	One "H" level pulse.
⎏⎍	One "L" level pulse.

4-3 Explanation of IEC Logic Symbols

(1) Symbol composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The purpose of general qualifying symbol is to accurately portray the logic function of the device.



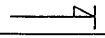
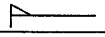
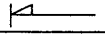
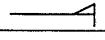
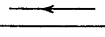
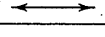
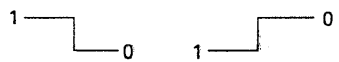
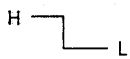
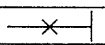
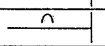
* : qualifying symbol locations for inputs and outputs

(2) Qualifying Symbols

(a) General Qualifying Symbols

Symbol	Definition
&	AND element
⩾1	OR element
=1	EXCLUSIVE OR element
=	Logic identify element. If all inputs have the same logic state then the output is at internal logic "1".
2K	Even element. If an even number of inputs are at internal logic "1" then the output is at internal logic "1".
2K+1	Odd element. If an odd number of inputs are at internal logic "1" then the output is at internal logic "1".
1	Buffer element without amplified output.
▷ or ◁	Buffer element with amplified output. The triangle points in the direction of signal flow.

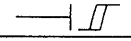
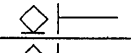
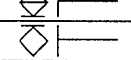
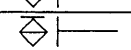
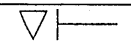
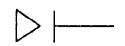
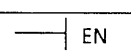
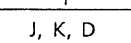
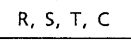
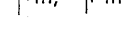
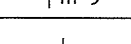
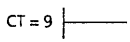
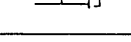
(b) Inputs and Outputs Qualifying Symbols

Symbol	Definition
	Logic negation at an input. An external logic "0" ("1") produces an internal logic "1" ("0").
	Logic negation at an output. An internal logic "0" ("1") produces an external logic "1" ("0").
	Porlarity indicator at an input. A "L" (Low) level active.
	Porlarity indicator at an output. A "L" level active.
	Porlarity indicator at an input where the signal flow is from right to left.
	Porlarity indicator at an output where the signal flow is from right to left.
	Indicator for direction of signal flow.
	Bidirection information flow (alternate).
	Dynamic input Positive logic. Negative logic. Porlarity indicate.  The above transitions set the internal logic active.
	Dynamic input Positive logic. Negative logic.  The above transitions set the internal logic active.
	Dynamic input Porlarity indicate.  The above transitions set the internal logic active.
	Non-logic connection.
	Input for analog signals.

(c) Symbols of internal connections

Symbol	Definition
	A logic "1" at the left-hand side produces a logic "0" at the right-hand side.
	Negated internal connection. A logic "1" at the left-hand side produces a logic "0" at the right-hand side.
	Dynamic internal connection. A transition from internal logic "0" to internal logic "1" at the left-hand side produces a transistory logic "1" at the right-hand side.
	Internal input (virtual). This input is always at internal logic "1" state unless this is overridden or modified.
	Internal output (virtual). This effect on the internal input connected to this output must be indicated by dependency notation.
	Schmitt-trigger. It has hysteresis characteristics.
	Retriggerable monostable element.
	Non-Retriggerable monostable element.
	Astable element
	Synchronous-starting astable element.
	Synchronous-stopping astable element.
SRGm	Shift register. "m" : number of bits.
CTRm	Binary counter. "m" : number of bits. cycle length : 2
CTRDIVm	Counter with cycle length m.
RCTRm	Ripple carry counter. "m" : number of bits. cycle length : 2
X/Y	Coder or code converter. X and Y may be replaced by appropriate indications of the codes used.
MUX	Multiplexer/data selector
DMUX or DX	Demultiplexer.
Σ	Adder.
P − Q	Subtractor.
CPG	Look-ahead carry generator.
π	Multiplier.
COMP	Comparator.
ALU	Arithmetic logic unit.
ROM	Read only memory.
RAM	Random access memory.
FIFO	First-in First-out memory.
I = 0	When power is switched ON, the element goes to internal logic "0"
I = 1	When power is switched ON, the element goes to internal logic "1"
	Delay element with specified delay times.

(d) Symbols inside the outline

Symbol	Definition
	Delayed output. The output change is delayed until the input that indicated the change returns to its initial external state or level.
	Schmitt trigger input.
	Open-drain output without internal pulled-up resistor.
	Open-drain output with internal pulled-up resistor.
	Open-source output without internal pulled-down resistor.
	Open-source output with internal pulled-down resistor.
	Three-state output.
	Buffered output. (The triangle points in the direction of signal flow)
	Enable input.
J, K, D	Information inputs of disable elements.
R, S, T, C	Control inputs of disable elements.
	Shift input. The direction of shift is to the right or down when the arrow points to the right, or to the left. "m" = 1, 2, 3 ···, however, the number may be omitted when "m" = 1.
	Counting input. Count-up or count-down are indicted by + and - respectively. The number "m" is the count per command and may be omitted when "m" = 1.
	Bit-grouping symbol. "m" is the highest power of 2 in the group.
	Content input. The internal logic "1" sets the element to the value "m".
	Content output. For example, when the input state is "1", the internal registor sets "9".
	Line-grouping symbol. The inputs enclosed by this symbol from a single logic input.
	Fixed-mode input. Fixed-state output. This input (output) is permanently at internal logic "1".

(3) Dependency Notation

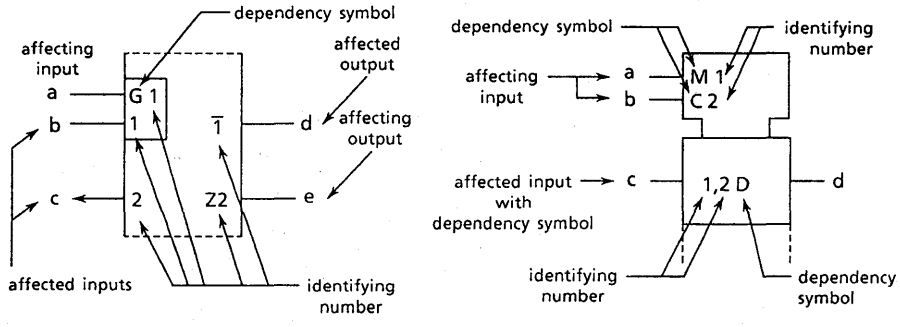
Dependency notation is the powerful tool that makes IEC Logic Symbols Compact and yet meaningful with IEC symbols, the relationships between inputs and outputs are clearly illustrated without the necessity to show all elements and interconnections involved.

In dependency notation, the terms "affecting" and "affected" are used.

(a) The general rules applied to dependency notation.

1) The input (or output) affecting other inputs or outputs is labelled with the letter symbol that indicates the relationship involved followed by an appropriately chosen identifying number.
2) Each input or output affected by that affecting input (or output) is labelled with that same number.
3) If it is the complement of the input's (or output's) internal logic state that dose the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs.
4) If the affected input or output has a label to denote its function, this label will have the identifying number of the affecting input as a prefix.
5) If two affecting inputs or outputs have the same letter and the same identifying number, they are ORed together.
6) If the labels denoting the function of affected inputs or outputs are numbers (ex. outputs of a coder), the identifying number of both affecting inputs and affected inputs or outputs is replaced by another character selected to avoid ambiguity, e.g., Greek letters.
7) If an input or output is affected more than one affecting input, each identifying number separated by a comma will appear in the label of the affected one. The normal reading order of these numbers is the same as the sequence of the affecting relationships.

Fig. 4-3 Example of dependency notation



(b) Symbols for dependency notation

Function	Symbol	Input State "1"	Input State "0"
AND	G	Permits action	Imposes "0" state
OR	V	Imposes "1" state	permits action
Negate (EX – OR)	N	Complements State	No effect
Interconnection	Z	Imposes action	Permits action
Control	C	Permits action	Prevents action
Set	S	S = 1 , R = 0	No effect
Reset	R	S = 0 , R = 1	No effect
Enable	EN	Permits action	Prevents action of input
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Address	A	Permits action (Address selected)	Prevents action (Address not Selected)

5. PRECAUTIONS IN DESIGNING CIRCUITS

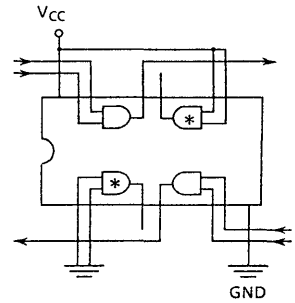
5-1 Input Processing

(1) Processing of unused gate

Inputs of CMOS IC have such a high impedance that the logic level becomes undefined under open input conditions. Should the floating input be at an intermediate level, the transistors of both P-channel and N-channel turn on, and unnecessary supply current flows.

Therefore, as shown in Fig. 5-1, be sure to connect unused input lines to V_{CC}, GND or other inputs and the output to the logic level as determined by the inputs.

In the case of CMOS, if a soldered part has poor contact, a malfunction of the system or an increase in supply current will occur. Therefore, care must be taken at the time of soldering.

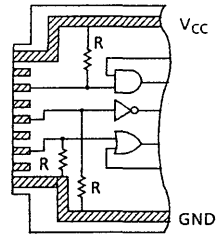


(* Unused gate)

Fig. 5-1
Treatment of Inputs

(2) Input processing of printed wiring board

When the input terminal of a printed wiring board is connected directly to a CMOS input, that input electrically floats. This condition is the same as a single IC being transported or stored. It is advisable, therefore, to connect this input to V_{CC} or GND through a resistance on the printed wiring board, as indicated in Fig.5-2



R : ≃100kΩ

Fig.5-2
Input processing of printed wiring Board

5-2 Design of Power Source

In general, CMOS has a small current consumption in comparison with bipolar digital IC's and, therefore, it needs only a small capacity power supply. However, from an operational standpoint, CMOS consumes power during transition, and therefore, it is necessary to keep the high frequency impedance of the power source at a low level.

It is advisable to make the wiring of the power source (V_{CC}) and GND lines thick and short, and insert, as a high frequency filter, a 0.001μF to 0.1μF capacitor between V_{CC} and GND for each IC.

Also, it is recommended that a capacitor of about 10μ F to 100μF be inserted between the power supply entrance and GND as a low frequency filter. As mean supply current differs considerably depending upon the operating frequency of the system, existence of capacitive load, and rise and fall of the input signal, supply voltage attention must be given especially in the case of a simple power source by using a Zener diode, or by battery drive. When there is overshoot or undershoot during the transition time of the supply power, use a filter, etc. so that the maximum rating is not exceeded.

5-3 On Output Short-circuit

In the TC74LVQ / LVX series, a buffer is added to the output, and both flow-out (I_{OH}) and flow-in (I_{OL}) current drive is possible. For this reason, excessive current flows in a CMOS output when the high level output line is shorted to the GND line or the low level output line is shorted to the V_{CC} line. Particularly, when the supply voltage is high, I_{OH} and I_{OL} are excessive and may damage the device; care must be taken not to cause an output short circuit.

It is, of course, impossible to directly connect ordinary outputs together, but in the case of an IC which has a 3 state output, a wired OR is permitted provided that no more than two outputs are enabled simultaneously.

Further, in order to improve drive capacity, it is possible to connect the gates in the same package as shown in Fig.5-3

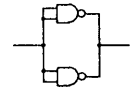


Fig.5-3
Example for increasing drive capacity

5-4 Effect on Input of Slow Rise and Fall Time

When a waveform with a slow rise / fall time is impressed on a CMOS input, it sometimes happens that the output tends to oscillate around V_{TH} (threshold voltage of circuit) of input waveform. This is because the CMOS gate becomes a linear amplifier equivalent in the vicinity of V_{TH}, and minute power source ripple and noise components are amplified and appear in the output.

In this case, there is a possibility of malfunction even though the input signal is within the standard value of Table 5-1. Therefore, care must be taken in design of sequence circuit clock inputs.

Table 5-1 Standard Value of Input Rise and Fall Time

Item	Symbol	Limit	Unit
Input Rise and Fall Time	dt/dV	0~100	ns/V

5-5 Wiring Precautions

(1) Output waveform distortion

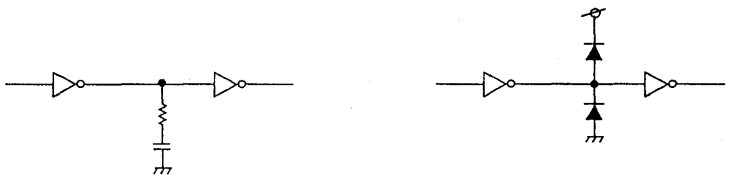
As, the output impedance of the TC74LVQ / LVX series is very low, distortion is sometimes caused in the output waveform depending upon the L component of the wiring, when the wiring connected to output end is long or when capacitance is connected between signal line and V_{CC} or GND. Therefore, when designing the printed wiring board, take care not to make signal wiring too long. In the clock signal line, distortion of the waveform causes malfunctions.

(2) Precautions for wiring arrangements

The output of TC74LVQ / LVX series has a fast rise and fall time, and makes a full swing between V_{CC} and GND; therefore it become a noise source to other signals. It is desirous to locate the output separately from a part which is sensitive to the noise of an analog circuit. Also, care must be taken for the reduction the number of loads and for the minimum of wiring length.

(3) Termination

From its physical and electrical characteristics, the TC74LVQ / LVX series is apt to cause overshoot and undershoot, and this leads to malfunction of the circuit or breakdown of passive IC's. These troubles can be prevented to some extent by terminating the end of signal line. Fig. 5-5 indicates examples of termination.



(a) Termination by RC components (b) Termination by Diodes

Fig. 5-5 Examples of Termination

(4) Fan out

In the case of the mutual interface between CMOS IC's, the input impedance of CMOS is so large that the limitation on fan out may not be great. However, there is a need to consider the increase in propagation time due to the effect of adding load capacitance and the increase in power consumption.

The input capacitance of CMOS is about 5pF per input. If 10 fan outs are taken, for example, load capacitance is 50pF Additionally, the line capacitance of the printed wiring board must also be taken into account. This shows that the processing speed of

system is controlled not only by the circuit components but also by fan out.

When designing a system using CMOS IC's, examine the fan out.

5-6 Latch-up

Latch-up is a phenomenon peculiar to CMOS, and is also called SCR (Silicon Controlled Rectifier) Phenomenon. During the normal operation, if excessive voltage and current caused by high noise or an accidental surge is applied to the input or output terminal, or a supply source suddenly fluctuates, abnormal current flows between V_{CC} and GND, and this abnormal current continues to flow even though the causitive signal is cut off, and finally damage is caused. Latch-up is the name given to this phenomenon.

Once latch-up takes place, the original operating condition is not restored unless the power supply is cut off or voltage is lowered, and an overcurrent continues to flow between V_{CC} and GND. If latch-up is not stopped, destruction of elements such as melting of wiring will take place.

(1) Cause of latch-up

Fig. 5-6 shows as equivalent circuit due to the parasitic element. NPN transistor Q_2 is formed in the P-well of NMOS side while PNP transistor Q_1 is formed in the N-substrate of PMOS side, and a parasitic resistor exists between terminals. As is shown from the current path through the medium of the parasitic element, these parasitic elements constitute a Thyristor.

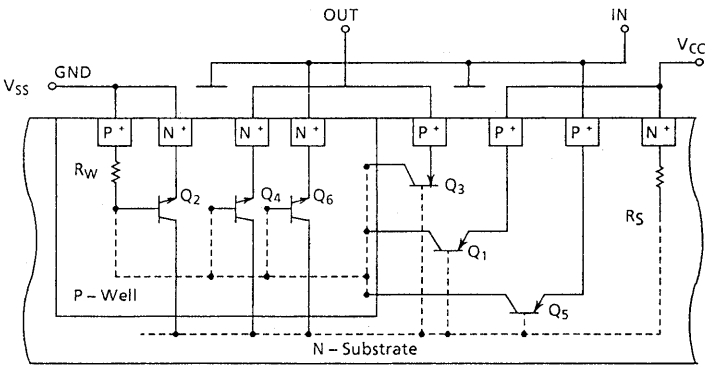


Fig. 5-6 Internal Equivalent Circuit of CMOS IC

For example, if current flows into the N-substrate from external sources, a voltage drop takes place in the resistor Rs of the N-substrate, and this turns on parasitic transistor Q_1, and current flows towards GND from V_{CC} through the medium of resistor Rw of P-Well. When current flows in Rw, voltage drop takes place at both ends of Rw, Q_2 turns on, and further supply current flows through Rs. As a result, the voltage drop at both ends of Rs furthers increases. Q_1 and Q_2 are left in the turn-on state, and the supply current continues to increase.

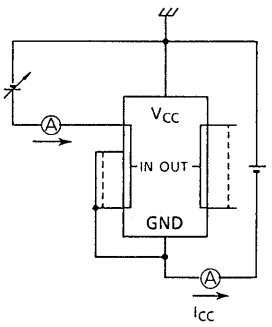
In this way, if the voltage drop takes place in resistance Rw of the P-Well and in resistance Rs of the N-substrate, latch-up occurs, and the following chain of events occur:

1) Input Voltage goes higher than $V_{CC} + V_F$
   (Q_5 turns on)
2) Input Voltage goes lower than $GND - V_F$
   (Q_6 turns on)
3) Output Voltage goes higher than $V_{CC} + V_F$
   (Q_3 turns on)
4) Output Voltage goes lower than $GND - V_F$
   (Q_4 turns on)
5) Supply voltage V_{CC} goes above the rated value causes breakdown.
   (Directly forces current in Rw or Rs)

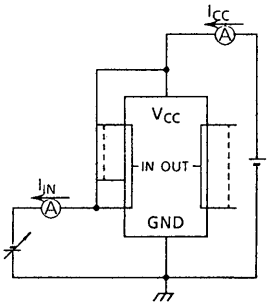
Here, V_F is the forward voltage between base and emitter of parasitic bipolar transistor $Q_3 - Q_4$.

(2) Latch-up strength measurement

Fig 5-7 illustrates techniques for measurement of latch-up strength. As indicated in Fig 5-7 latch-up is induced by forcing a current into the input terminal (+injection) or forcing a current out of the output terminal (−injection), and the current value at the time of latch-up is measured.



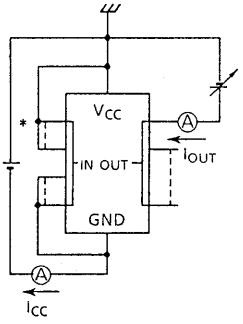
(a) Measurement circuit of + Injection strength of Input Terminal



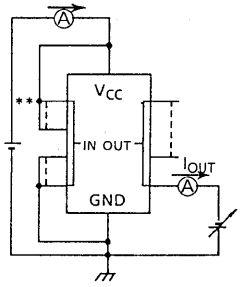
(b) Measurement circuit of − Injection strength of Input Terminal

* : Input condition to make measured terminal high level

** : Input condition to make measured terminal low level



(c) Measurement circuit of + Injection strength of Output Terminal



(d) Measurement circuit of − Injection strength of Output Terminal

Fig. 5-7 Latch-up Strength Measurement Circuits by Current Feeding System

(3) Countermeasures

As ample margin against latch-up is provided as explained in (2), there is no problem in using the TC74LVQ / LVX within specifications. However, since the interface part has the possibility of receiving excessive surges it is recommended that protective circuits be added as shown in Fig.5-8.

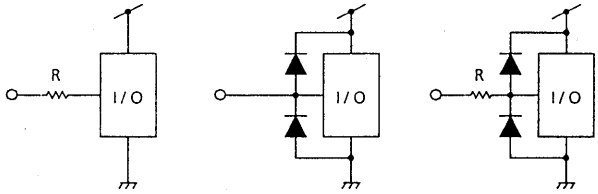
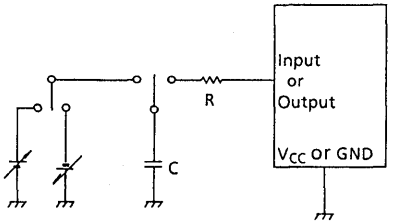


Fig. 5-8 Example of Latch up Prevention Methods

5-7 Electric Discharge and Noise Precautions

The TC74VQ / LVX series has ample margin for handling noises such as electric discharge. Fig.5-9 shows a circuit for ESD test and table 5-2 shows the result of ESD test for the representative parts.



EIAJ Method: C = 200pF, 0Ω
MIL-STD Method: C = 100pF, 1.5kΩ

Fig. 5-9 Test Circuit

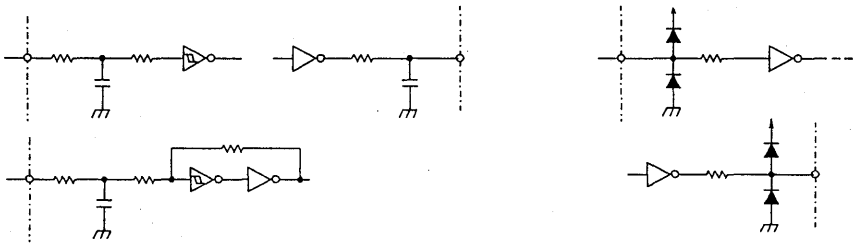
Table 5-2 Test Result

Name	EIAJ Method		MIL-STD Method	
	Input	Output	Input	Output
TC74LVQ00F	> ± 300V	> ± 300V	> ± 2000V	> ± 2000V
TC74LVQ244F	> ± 300V	> ± 300V	> ± 2000V	> ± 2000V
TC74LVX00F	> ± 300V	> ± 300V	> ± 2000V	> ± 2000V
TC74LVX244F	> ± 300V	> ± 300V	> ± 2000V	> ± 2000V

However, input and output signal lines are naturally long in many cases, and have distributed inductance or reactance.

Therefore, if directly connected to CMOS, these lines can give rise to various problems. Conceivable problems may be a malfunction due to induced noise, and the destruction of the input/output elements due to surge. To cope with these problems, reduction of signal line impedance (driving impedance) or insertion of noise eliminating circuits on the receiving side are done for the former, while surge protective measures are taken for the latter.

Fig.5-10 shows examples of providing noise and surge protection on the input side.

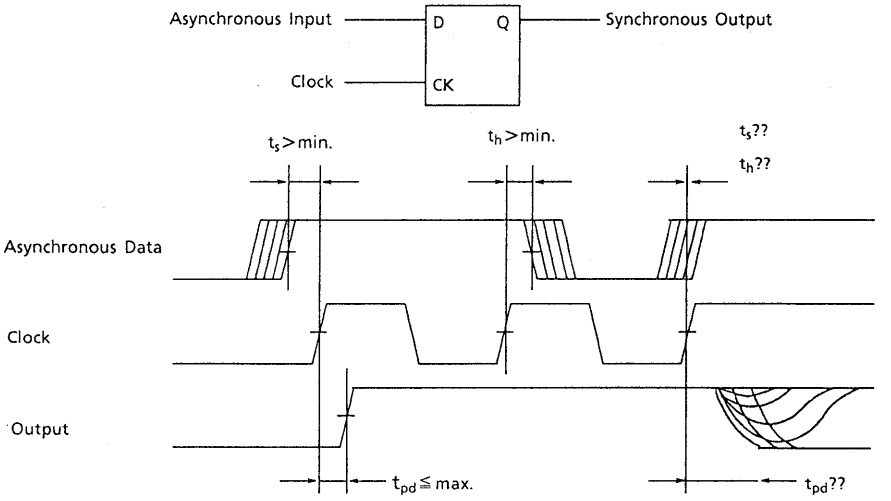


(a) Providing Noise Protection (b) Surge Protection

Fig. 5-10 Protection Circuits

5-8 Metastable Characteristics

When the set-up or hold-time of a flip-flop is violated, the device output response is uncertain. This phenomenon is called metastability.



The diagram as shown above describes the metastable state which can generate a glitch or increase the propagation delay time. The metastable state cannot be avoided, if the asynchronous signal is an input to a flip-flop which is clocked by the internal clock of a synchronous system.

Therefore,in order to avoid this problem, it is recommended that the timing requirements specified on the datasheet be observed, in case of using an asynchronous sync. signal, care must be taken regarding the output signal.

Fig.5-11 shows an example of solving this problem. In this case, if the difference in phase between CK1 and CK2 is the same as tpd (clock to output) of the first stage flip-flop, care must be taken.

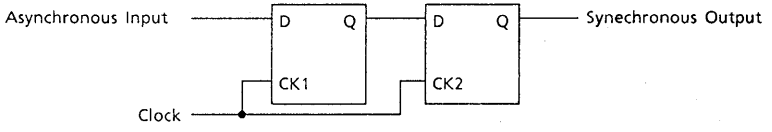


Fig. 5-11 Solving Metastability Problem

Note) if CK1 and CK2 cannot be used together, the synchronous clock signal used for CK1 should be phase shifted and would be applied as the clock of the second stage flip-flop (CK2). (ie. $\overline{CK2} = CK1$)

6. ASSEMBLING AND HANDLING PRECAUTIONS

6-1 Assembling

The following describes the recommended methods for attaching devices to PCB's.

Note) Solder dipping and Near IR reflow method should not be used for attaching SSOP devices to PCB's.

(1) Using a Soldering Iron

When attaching devices by means of a soldering iron, do not exceed 260°C soldering temperature and a soldering time of 10 seconds, using a groundel soldering iron.

(2) Infrared Reflow

1. Top and bottom heating is recommended with far and intermediate infrared. (Fig.6-1)

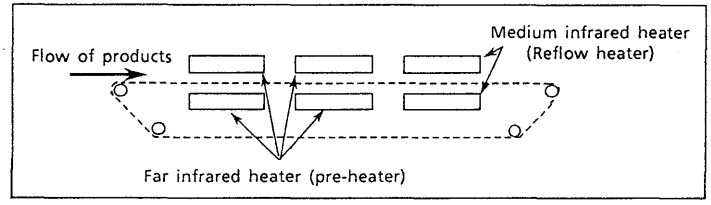


Fig. 6-1

2. Keep the temperature at the package surface and board surface below 240°C and over 210°C for no more than 30 seconds.
3. Figure 6-2 is an example of recommended temperature profile.
4. When using near infrared, note that the thermal stress is critical and is equivalent to the case for solder dipping. (Do not use for SSOP.)

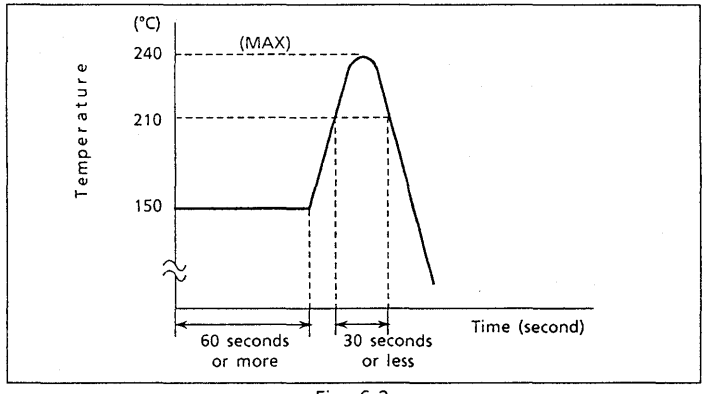


Fig. 6-2

(3) Hot Air Reflow

Similar to "(2) Infrared Reflow" for either hot air only or combination of hot air and far infrared.

1. Keep the temperature at the package surface and board surface below 240°C and over 210°C for no more than 30 seconds.
2. The recommended temperature profile is the same as for "(2) Infrared Reflow."

(4) Vapor Phase Solder

1. Florinate FC-70 or equivalent solvent is recommended.
2. Ambient temperature must not exceed 215°C for 30 seconds or 200°C for 60 seconds.
3. Figure 6-3 shows a recommended temperature profile for V.P.S.

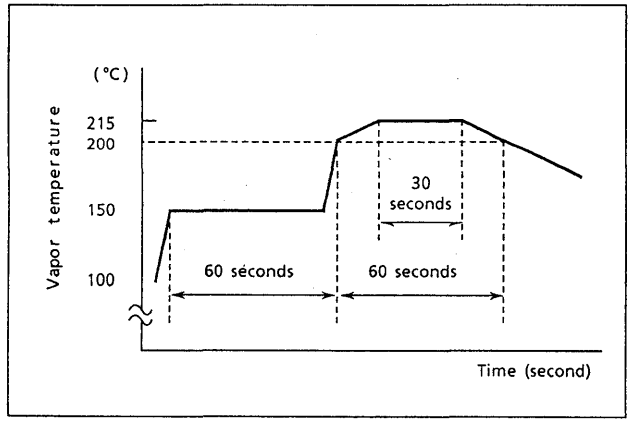
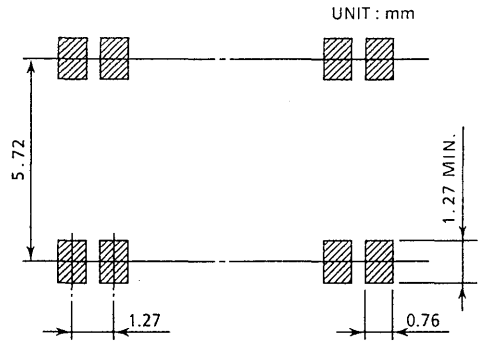


Fig. 6-3

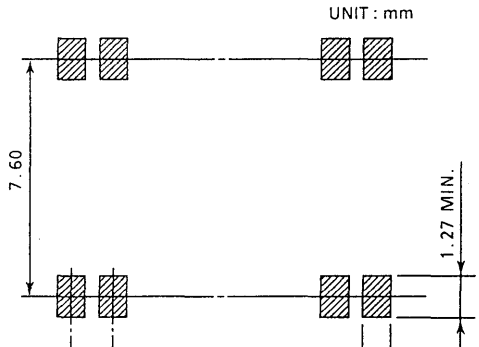
(5) Solder Dipping (Do not use for SSOP.)

1. Preheating should be 60 seconds or more at 150°C.
2. Solder flow should not exceed 10 seconds at 260°C.

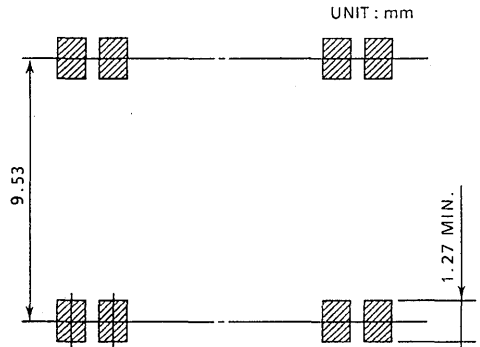
6-2 Mount Pad Dimension



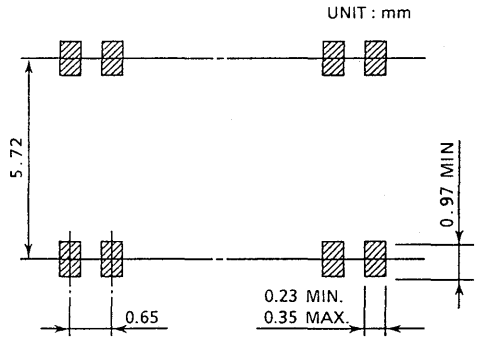
a) 150 mil Standard pad layout



b) 200 mil Standard pad layout



c) 300 mil Standard pad layout



d) SSOP Standard pad layout

6-3 Handling Precautions

(1) Transportation and Storage

As the input and output terminals of unmounted CMOS IC's are in a state of high impedance, they can receive induction from the surrounding charged body, space electric fields, and the human body.

For this reason, it is necessary, in transporting and storing them, to use dielectric mats, metal cases or aluminum foil boxes, so that each terminal of the IC will be at same potential.

As the TC74LVQ / LVX series are inserted in magazines and are given antistatic treatment at the time of shipment, do not remove devices from the magazines unnecessarily. Especially, avoid the use of plastic or vinyl containers which can create static charges.

(2) Assembling

When installing CMOS IC on the printed wiring board, it is necessary to protect the electric equipment, working stand and operators from static electricity by grounding. It is advisable to ground the working stand by spreading an electric semi-conductive sheet on the surface. (sheet resistibity should be $10^5\Omega \sim 10^8\Omega$ / cm^2.) Grounding of operators should be made through a resistance of about 1MΩ so as to prevent electric shock. It is convenient to make grounding through a metallic ring or metallic wrist bands. Also, it is advisable not to wear working clothes make of chemical fibers. Further, it is necessary to periodically check electric equipment to insure absence of electric leakage.

When shaping the lead during the packaging of IC's, it is advisable to use a pincet or similar jig, so that the device leads are not stressed at the package entrance.

When storing or transporting the completely assembled printed wiring board, short circuit the terminals of the printed wiring board or cover the entire board with aluminum foil, so that the input terminals of the IC are open.

(3) Soldering, washing

When soldering by use of a soldering iron, carry out the work at temperature of 260°C or below within 10 seconds. The reliability of TC74LVQ / LVX series are not affected when subjected to a temperature stress at the lead of 260°C for 10 seconds.

Use a soldering iron having no electrical leakage to the heated end. It is recommended to use a class A iron having an insulation resistance exceeding 10MΩ. When using soldering tank, it is necessary to ground the tank so as to prevent the electric potential of the soldering tank from affecting the work.

After soldering, the IC's on the printed wiring board, cleaning is done to remove flux,

etc. For this cleaning use a flux removing abluent or a cleaning method utilizing ultrasonic wave. Care must be taken in the selection of this solvent so as to prevent adverse effects to the package and marking of the CMOS IC.

When using ultrasonic cleaning, it is necessary to prevent stress due to resonance from being imparted to the IC or printed wiring board. Because of this, it is necessary to consider the method such that the main body becomes a shade against vibration, and also to use a cleaning time of less than 30 seconds.

If flux is not completely removed after soldering, there is a possibility that chemical substances such as chlorine or sodium could migrate inside of the IC package and react with other chemical substances inside the package. This chemical reaction can caues corrosion on the pellet and can change the electrical characteristics of the device. TOSHIBA recommends the use of rosin base flux in which the content of chlorine is below 0.2wt%. (ex. specified in JIS-A class)

(4) Adjustment, Test

When making adjustment and tests after the completion of printed wiring board, it is necessary to check for solder bridge or cracks on the printed wiring board before application of supply power. As CMOS systems require only a small supply current, it is well to apply current limiting during test by using a constant voltage power source.

Before inserting or removing printed wiring boards into or out of the test fixture, ensure that the power supply is off.

When inspecting each part of the printed wiring board with a probe, care must be taken to prevent contact of the tip of the probe with other signal or power lines. It is advisable to install a special test pin for use with probes.

When the tests are conducted under high or low temperature, it is necessary to ensure grounding of the constant temperature oven.

(5) Precaution in Using Products in Harsh Environment

A moisture-proof costing should be used on the devices if the devices are used in equipments which require high reliability or are used under bad condition such as corrosive gas, dust, etc.

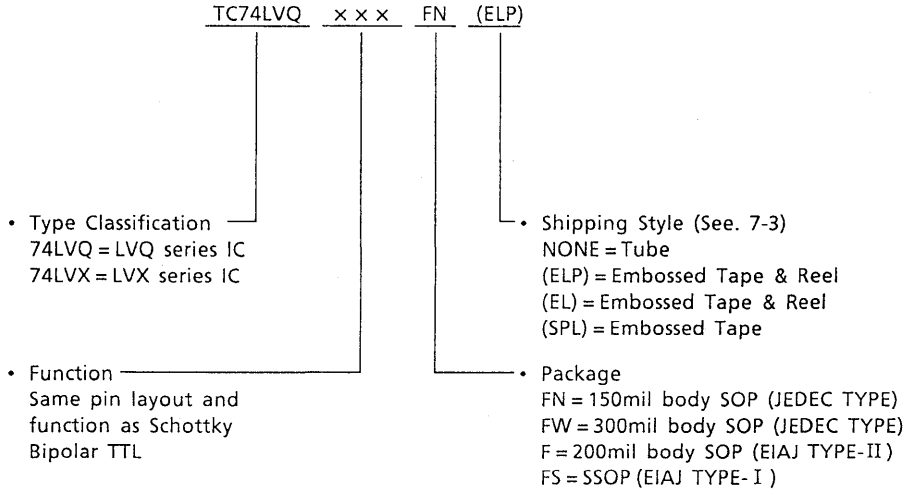
(6) Precaution near Flammable Material

TOSHIBA uses a resin material which is flame retardant (approved by UL94V-0 standard). However, since, the resin material is not non-flammable, there is a possibility that it will ignites and give off smoke when it burn. Therefore, these TOSHIBA parts must not be used near flammable materials.

7. SHIPPING STYLE AND ORDERING METHODS

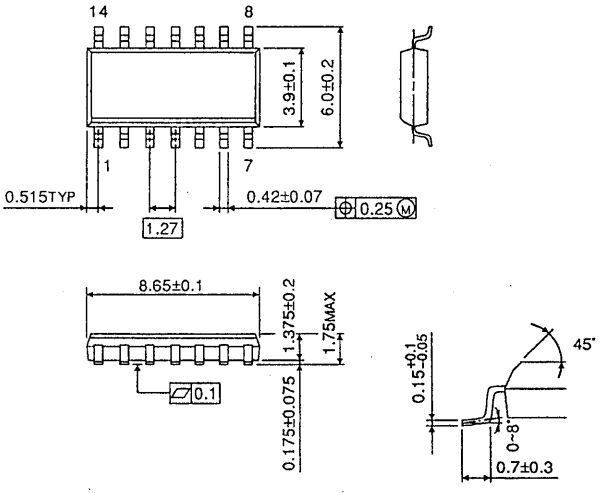
7-1 Method of Designating the TC74LVQ / LVX Series

TC74LVQ / LVX series is as shown below.



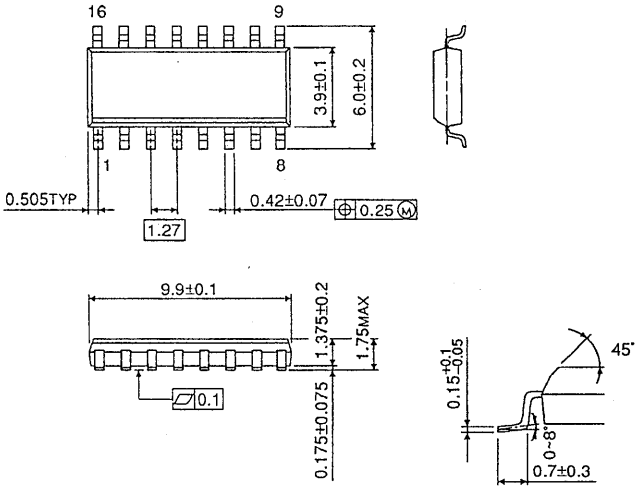
7-2 Package

SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150) Unit in mm



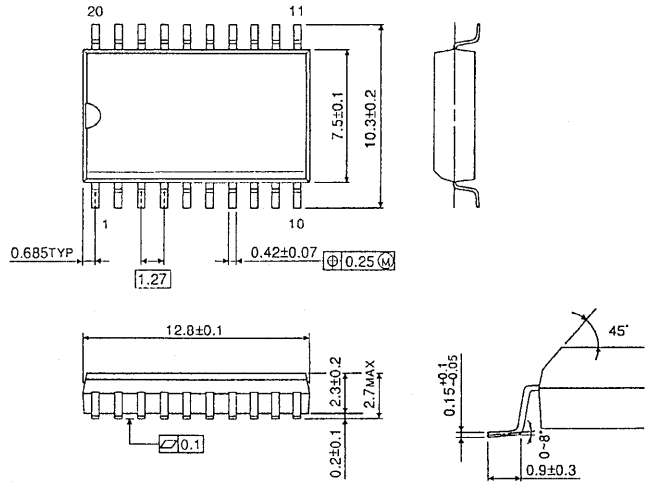
Weight : 0.12g (TYP.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150) Unit in mm



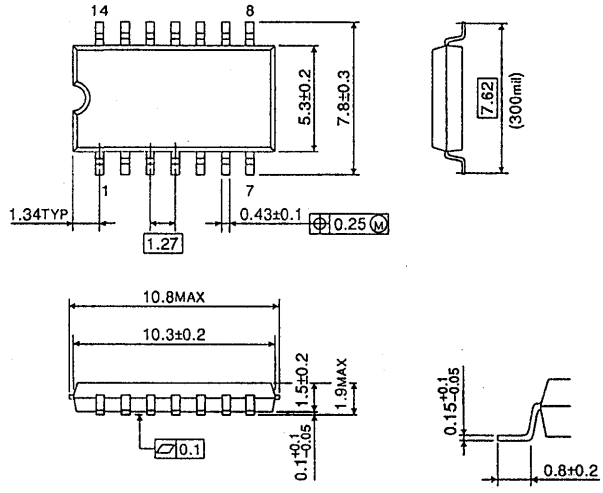
Weight : 0.13g (TYP.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300) Unit in mm



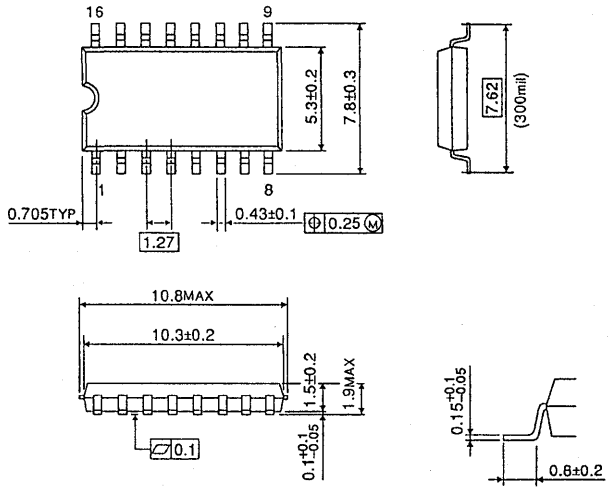
Weight : 0.46g (TYP.)

SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300) Unit in mm



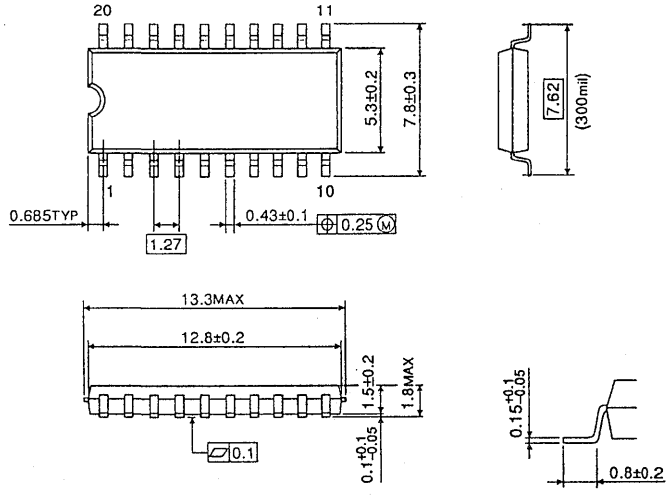
Weight : 0.18g (TYP.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300) Unit in mm



Weight : 0.18g (TYP.)

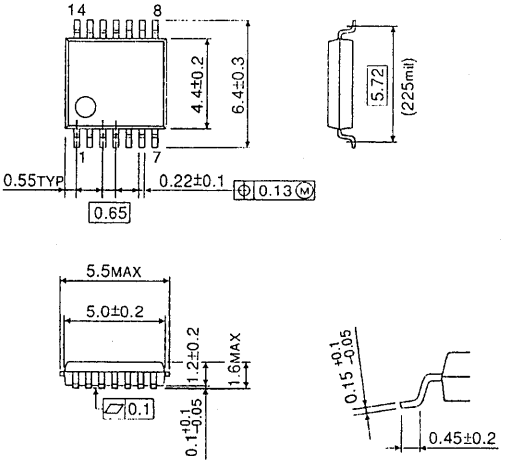
SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300) Unit in mm



Weight : 0.22g (TYP.)

SSOP 14PIN OUTLINE DRAWING (SSOP14-P-225)

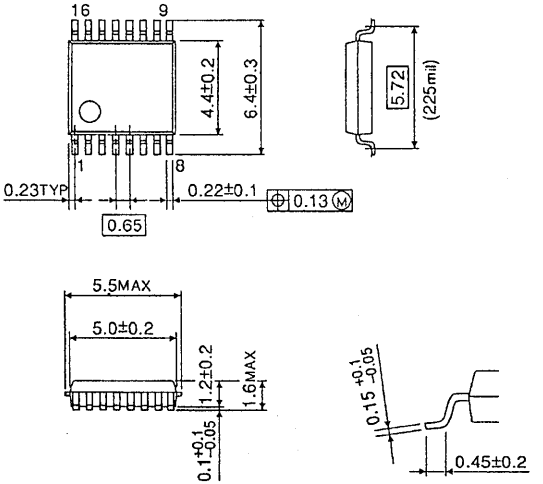
Unit in mm



Weight : 0.07g (TYP.)

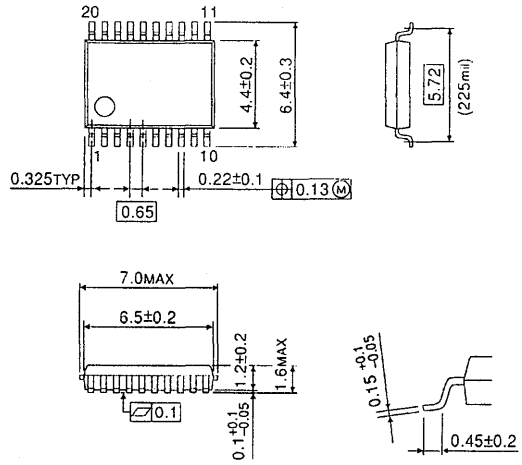
SSOP 16PIN OUTLINE DRAWING (SSOP16-P-225B)

Unit in mm



Weight : 0.07g (TYP.)

SSOP 20PIN OUTLINE DRAWING (SSOP20-P-225A) Unit in mm



Weight : 0.09g (TYP.)

7-3 Shipping Style and Ordering Methods

TC74LVQ/LVX products can be shipped in tubes or on tape and reel.

However, SSOP products are shipped on Tape & Reel in 2000 pcs or 50 pcs tape only.

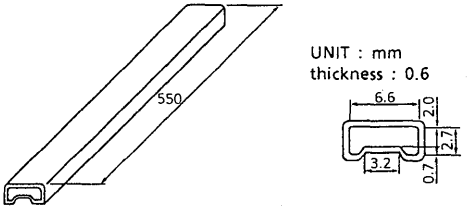
Suffix	Shipping Style	Package			
		JEDEC TYPE		EIAJ TYPE-II	EIAJ TYPE-I
		150 mil body	300 mil body	200 mil body	SSOP
		14, 16 pin	20 pin	14, 16, 20 pin	14, 16, 20 pin
		FN	FW	F	FS
NONE	Tube	○	○	○	N/A
(ELP) (EL)	Embossed Tape & Reel	○ 2500 pcs/reel	○ 1000 pcs/reel	○ 2000 pcs/reel	○ 2000 pcs/reel
(SPL)	Embossed Tape	N/A	N/A	N/A	○ 50 pcs/tape

○ : Available
N/A : Not Available

- Orders shall be placed in multiples of above minimum quantity per reel and tape, and part types will not be mixed on same reel.

(1) Tube Specification (SOP)

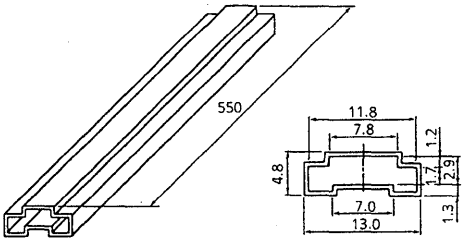
(150 mil body SOP)



Packaging

Package Type	Pin	n / tube
SOL14-P-150	14	50 pcs
SOL16-P-150	16	50 pcs

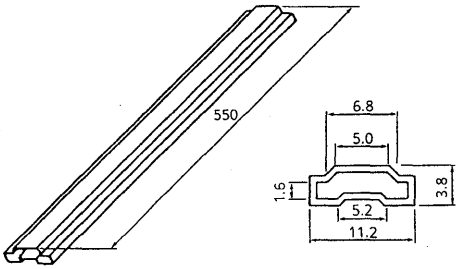
(300 mil body SOP)



Packaging

Package Type	Pin	n / tube
SOL20-P-300	20	40 pcs

(200 mil body SOP)



Packaging

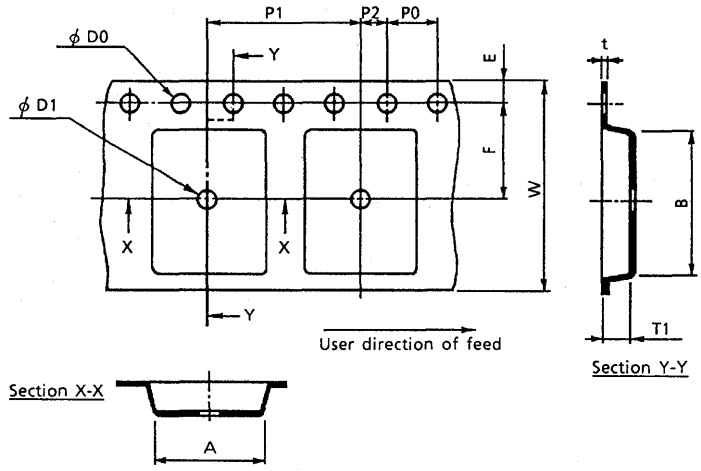
Package Type	Pin	n / tube
SOP14-P-300	14	50 pcs
SOP16-P-300	16	50 pcs
SOP20-P-300	20	40 pcs

Material : anti-electrostatic vinyl chloride
Both ends of the tube are sealed by synthetic rubber stoppers.

(2) Tape and Reel Specification (Embossed Tape & Reel)

(a) Taping Specification (150 / 300 mil SOP, 200 mil SOP, SSOP)

Package Type	Package Standard	Taping Standard
(150 / 300 mil) SOL14-P-150 SOL16-P-150 SOL20-P-300	 JEDEC MS-012-AB JEDEC MS-012-AC JEDEC MS-013-AC	EIA 418A
(200mil) SOP14-P-300 SOP16-P-300 SOP20-P-300	EIAJ TYPE II	EIAJ TE1612 EIAJ TE2412
(SSOP) SSOP14-P-225 SSOP16-P-225B SSOP20-P-225A	EIAJ TYPE I	EIAJ TE1608

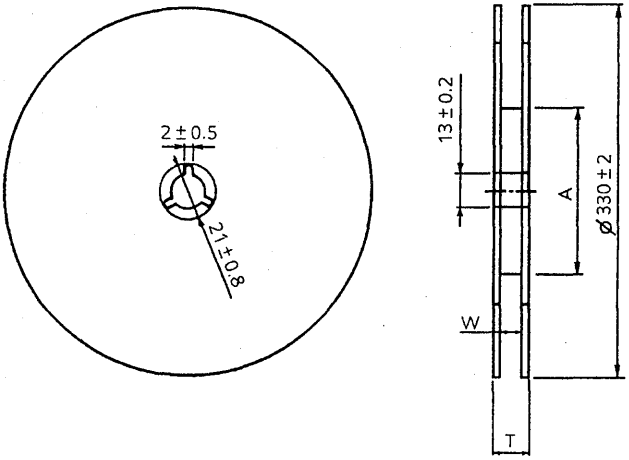


(UNIT : mm)

Package Type	A	B	W	F	E	P1	P2	P0	φD0	t	T1	φD1
(150/300 mil)												
SOL14-P-150	6.7 ±0.2	9.6 ±0.2	16.0 ±0.3	7.5 ±0.1	1.75 ±0.1	8.0 ±0.1	2.0 ±0.1	4.0 ±0.1	1.5 +0.1 −0.0	0.3 ±0.1	2.1 ±0.1	2.05 ±0.1
SOL16-P-150	7.0 ±0.2	10.5 ±0.2	16.0 ±0.3	7.5 ±0.1	1.75 ±0.1	8.0 ±0.1	2.0 ±0.1	4.0 ±0.1	1.5 +0.1 −0.0	0.3 ±0.1	2.1 ±0.1	1.55 ±0.1
SOL20-P-300	11.0 ±0.2	13.4 ±0.2	24.0 ±0.3	11.5 ±0.1	1.75 ±0.1	12.0 ±0.1	2.0 ±0.1	4.0 ±0.1	1.5 +0.1 −0.0	0.3 ±0.1	3.0 ±0.1	2.05 ±0.1
(200 mil)												
SOP14-P-300 SOP16-P-300	8.5 ±0.2	10.8 ±0.2	16.0 ±0.3	7.5 ±0.1	1.75 ±0.1	12.0 ±0.1	2.0 ±0.1	4.0 ±0.1	1.5 +0.1 −0.0	0.3 ±0.1	2.1 ±0.2	1.65 ±0.1
SOP20-P-300	8.3 ±0.2	13.2 ±0.2	24.0 ±0.3	11.5 ±0.1	1.75 ±0.1	12.0 ±0.1	2.0 ±0.1	4.0 ±0.1	1.5 +0.1 −0.0	0.3 ±0.1	2.2 ±0.2	2.0 ±0.2
(SSOP)												
SSOP14-P-225 SSOP16-P-225B	6.8 ±0.1	5.5 ±0.1	16.0 ±0.3	7.5 ±0.1	1.75 ±0.1	8.0 ±0.1	2.0 ±0.1	4.0 ±0.1	1.5 +0.1 −0.0	0.3 ±0.05	1.85 ±0.1	1.6 +0.1 −0.0
SSOP20-P-225A	6.8 ±0.1	7.0 ±0.1	16.0 ±0.3	7.5 ±0.1	1.75 ±0.1	8.0 ±0.1	2.0 ±0.1	4.0 ±0.1	1.5 +0.1 −0.0	0.3 ±0.05	1.85 ±0.1	1.6 +0.1 −0.0

Note) Resistance of the surface of the carrier tape shall be no more than $10^6\Omega \cdot cm$.
Po : Cumulative tolerance per 10 holes shall be no more than ±0.2 mm.

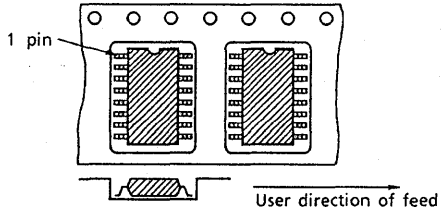
(b) Reel Mechanical Specification



UNIT : mm

Package Type	A	W	T
(150 mil) SOL14-P-150 SOL16-P-150	ø80 ± 1	17.5 ± 0.5	—
(300 mil) SOL20-P-300	ø80 ± 1	25.5 ± 0.5	—
(200 mil) SOP14-P-300 SOP16-P-300	ø80 ± 1	17.5 ± 0.5	—
(200 mil) SOP20-P-300	ø80 ± 1	25.5 ± 0.5	—
SSOP14-P-225 SSOP16-P-225B SSOP20-P-225A	ø100 ± 1	17.5 ± 0.5	21.5 ± 1.0

(c) Device Placement

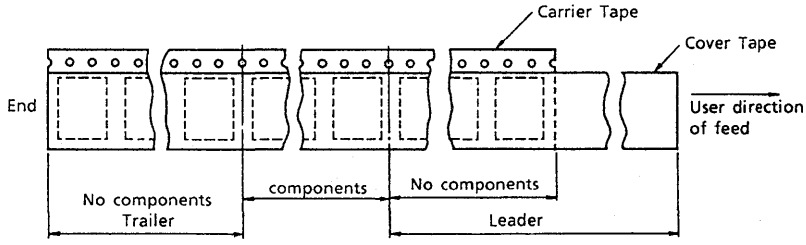


(TYPE L)

(d) Tape Leader and Trailer

Each carrier tape shall have, as a minimum, a leader and a trailer. A leader (at the beginning of the tape) and trailer (at the end of the tape) are delined as lengths of tape devoid of any devices.

	Cover Tape	Carrier Tape
Leader	500 mm min.	400 mm min.
Trailer	400 mm min.	400 mm min.



(e) Missing Devices

1. At no time will two or more consecutive divices be missing from a single reel.
2. Single missing device occurrence will be less than 0.1% (150 / 300 mil), 0.2% (200 mil, SSOP) per reel.

(f) Transportation and Storage

Care should be taken to minimize shock during transportation of the packaged reels and avoid excessive heat as this can change the peel strength of the cover tape. Storage shall be at a temperature below 45°C.

8. TC74LVQ SERIES TECHNICAL DATA SHEETS

TC74LVQ00F/FN/FS

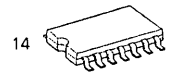
QUAD 2-INPUT NAND GATE

The TC74LVQ00 is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate and double - layer metal wiring C²MOS technology.

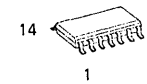
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

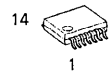
- High Speed ..... t_{pd} = 4.9ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2.5μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC00



F(SOP14-P-300)
Weight : 0.18g (TYP.)

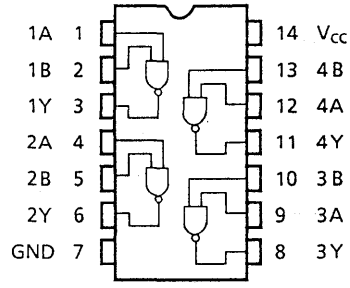


FN(SOL14-P-150)
Weight : 0.12g (TYP.)



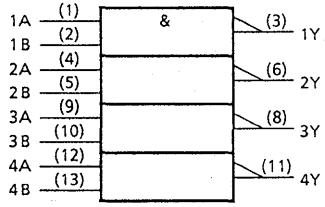
FS(SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH}	I_{OH} = −50μA I_{OH} = −12mA	3.0 3.0	2.9 2.58	3.0 —	— —	2.9 2.48	— —	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 12mA	3.0 3.0	— —	0.0 —	0.1 0.36	— —	0.1 0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.5	—	25.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	7.0 5.8	13.4 9.5	1.0 1.0	16.0 11.0	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	30	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\ \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.3	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

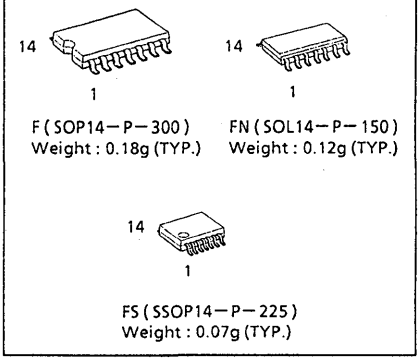
TC74LVQ02F/FN/FS

QUAD 2-INPUT NOR GATE

The TC74LVQ02 is a high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate and double-layer metal wiring C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 3.4ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2.5μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC02

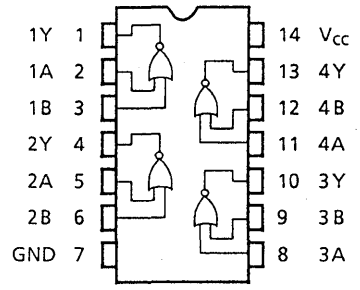


F(SOP14-P-300)
Weight : 0.18g (TYP.)

FN(SOL14-P-150)
Weight : 0.12g (TYP.)

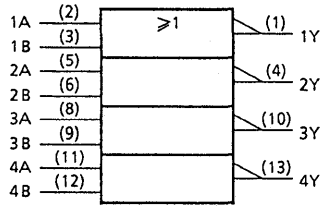
FS(SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IL}	I_{OH} = −50μA I_{OH} = −12mA	3.0 3.0	2.9 2.58	3.0 —	— —	2.9 2.48	— —	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 12mA	3.0 3.0	— —	0.0 —	0.1 0.36	— —	0.1 0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.5	—	25.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	5.2 4.3	10.6 7.5	1.0 1.0	12.0 8.0	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	26	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\ \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.3	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

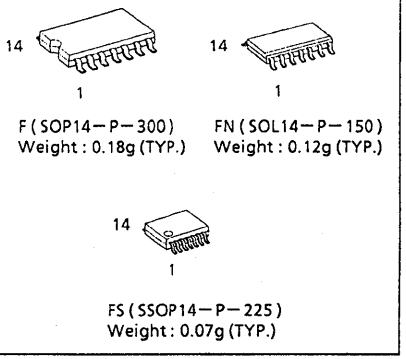
TC74LVQ04F/FN/FS

HEX INVERTER

The TC74LVQ04 is a high speed CMOS HEX INVERTER fabricated with silicon gate and double - layer metal wiring C^2MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 4.1ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2.5μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance ·· $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays ···· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC04

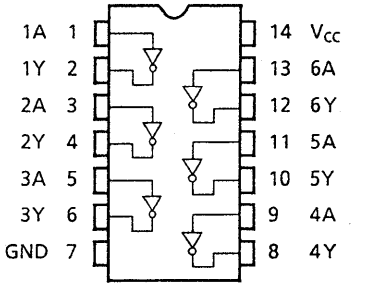


F (SOP14-P-300)
Weight : 0.18g (TYP.)

FN (SOL14-P-150)
Weight : 0.12g (TYP.)

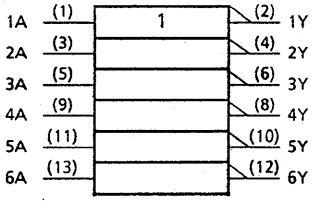
FS (SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS	OUTPUTS
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 150	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IL}$	$I_{OH} = -50\mu A$ $I_{OH} = -12mA$	3.0 3.0	2.9 2.58	3.0 —	— —	2.9 2.48	— —	V
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$	$I_{OL} = 50\mu A$ $I_{OL} = 12mA$	3.0 3.0	— —	0.0 —	0.1 0.36	— —	0.1 0.44	V
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		3.6	—	—	2.5	—	25.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	6.0 5.0	12.7 9.0	1.0 1.0	15.0 10.0	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	20	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLH\,m} - t_{pLHn}|$, $t_{osHL} = |t_{pHL\,m} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\,\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

TC74LVQ08F/FN/FS

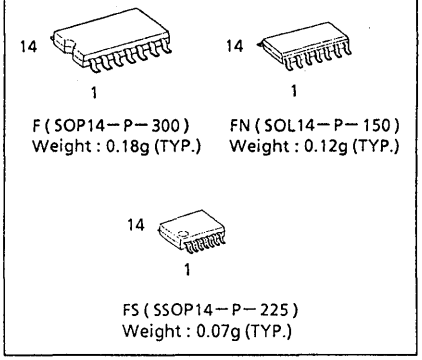
QUAD 2-INPUT AND GATE

The TC74LVQ08 is a high speed CMOS 2-INPUT AND GATE fabricated with silicon gate and double-layer metal wiring C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 4.7ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2.5μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC08

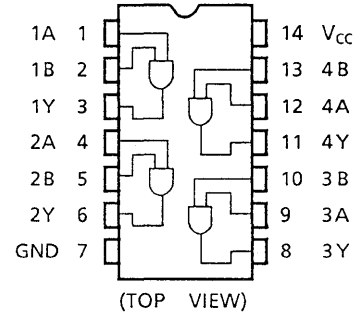


F (SOP14-P-300)
Weight : 0.18g (TYP.)

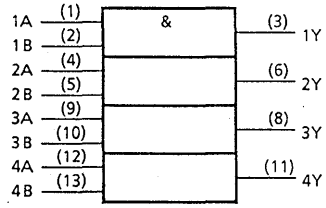
FN (SOL14-P-150)
Weight : 0.12g (TYP.)

FS (SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH}	I_{OH} = −50μA I_{OH} = −12mA	3.0 3.0	2.9 2.58	3.0 —	— —	2.9 2.48	— —	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 12mA	3.0 3.0	— —	0.0 —	0.1 0.36	— —	0.1 0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.5	—	25.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	6.7 5.6	13.4 9.5	1.0 1.0	15.0 10.5	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	22	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\ \Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

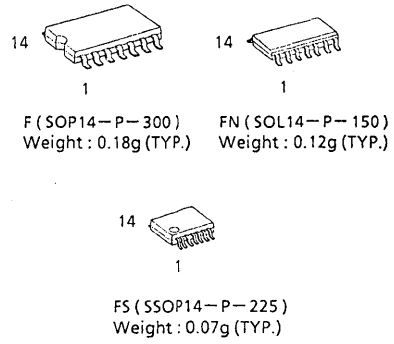
TC74LVQ14F/FN/FS

HEX SCHMITT INVERTER

The TC74LVQ14 is a high speed CMOS SCHMITT INVERTER fabricated with silicon gate and double - layer metal wiring C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. Pin configuration and function are the same as the TC74LVQ04 but the inputs have hysteresis and with its schmitt trigger function, the TC74LVQ14 can be used as a line receivers which will receive slow input signals.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed ..... t_{pd} = 6.1ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2.5μA(Max.) at Ta = 25°C
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC14

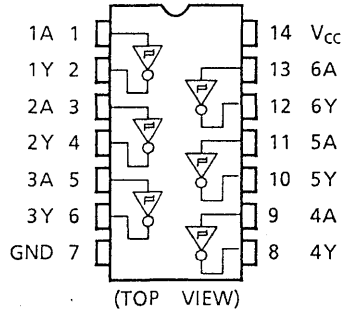


F (SOP14-P-300)
Weight : 0.18g (TYP.)

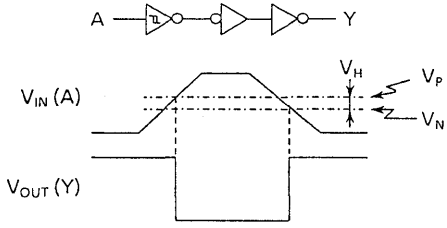
FN (SOL14-P-150)
Weight : 0.12g (TYP.)

FS (SSOP14-P-225)
Weight : 0.07g (TYP.)

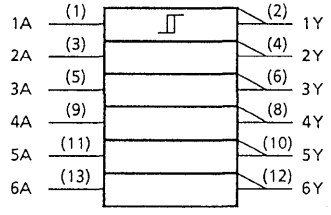
PIN ASSIGNMENT



SYSTEM DIAGRAM, WAVEFORM



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS	OUTPUTS
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 150	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Positive Threshold Voltage	V_P			3.0	—	—	2.2	—	2.2	V
Negative Threshold Voltage	V_N			3.0	0.9	—	—	0.9	—	V
Hysteresis Voltage	V_H			3.0	0.3	—	1.2	0.3	1.2	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IL}$	$I_{OH} = -50\mu A$ $I_{OH} = -12mA$	3.0 3.0	2.9 2.58	3.0 —	— —	2.9 2.48	— —	V
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$	$I_{OL} = 50\mu A$ $I_{OL} = 12mA$	3.0 3.0	— —	0.0 —	0.1 0.36	— —	0.1 0.44	V
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		3.6	—	—	2.5	—	25.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	8.4 7.0	19.0 13.5	1.0 1.0	22.0 15.0	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	29	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 6 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\ \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.2	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.9	V

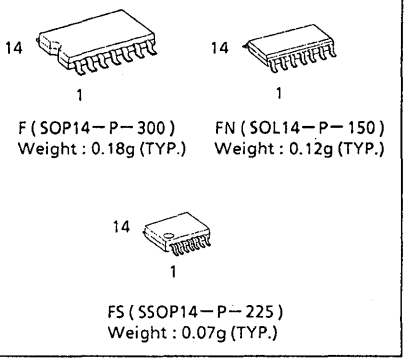
TC74LVQ32F/FN/FS

QUAD 2-INPUT OR GATE

The TC74LVQ32 is a high speed CMOS 2-INPUT OR GATE fabricated with silicon gate and double-layer metal wiring C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 4.1ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2.5μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC32

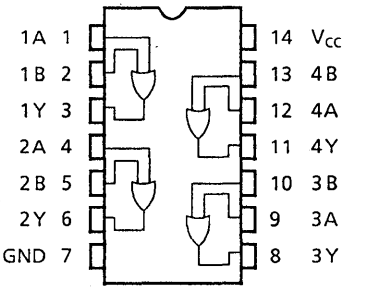


F (SOP14-P-300)
Weight : 0.18g (TYP.)

FN (SOL14-P-150)
Weight : 0.12g (TYP.)

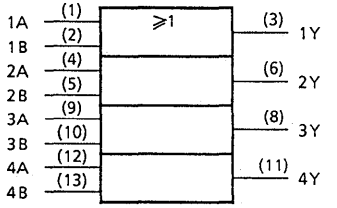
FS (SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.5	—	25.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	5.4 4.5	12.7 9.0	1.0 1.0	15.0 10.0	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	24	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\ \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

TC74LVQ74F/FN/FS

DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

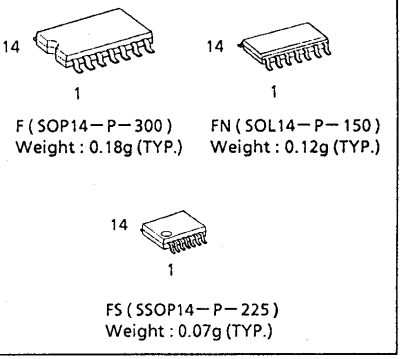
The TC74LVQ74 is a high speed CMOS D - FLIP FLOP fabricated with silicon gate and double - layer metal wiring C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

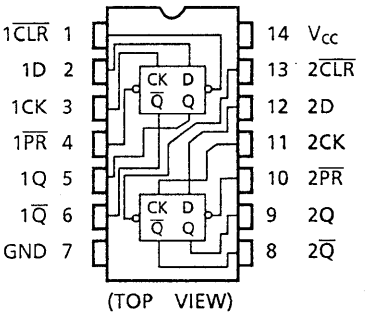
$\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input to an "L" level. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX} = 147MHz (typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2.5μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V; V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC74



PIN ASSIGNMENT

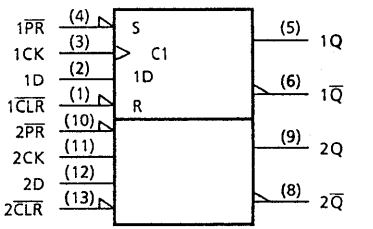


TRUTH TABLE

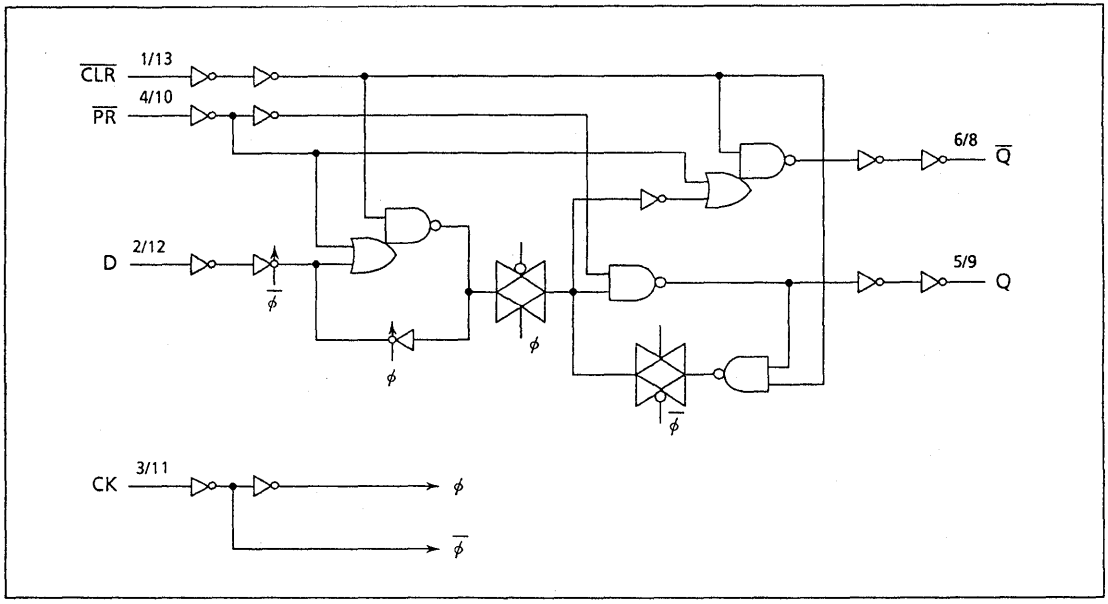
INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↓	L	H	—
H	H	H	↓	H	L	—
H	H	X	↑	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.5	—	25.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C	Ta = −40~85°C	UNIT
		V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$	2.7	9.0	10.0	ns
	$t_{W(H)}$	3.3 ± 0.3	7.0	7.0	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$	2.7	9.0	10.0	
		3.3 ± 0.3	7.0	7.0	
Minimum Set - up Time	t_s	2.7	7.5	8.5	
		3.3 ± 0.3	6.0	6.0	
Minimum Hold Time	t_h	2.7	1.0	1.0	
		3.3 ± 0.3	1.0	1.0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}	2.7	6.0	6.0	
		3.3 ± 0.3	4.0	4.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q , $\overline{Q}$)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	− −	9.0 7.5	19.7 14.0	1.0 1.0	23.0 16.0	ns
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ − Q , $\overline{Q}$)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	− −	8.4 7.0	16.9 12.0	1.0 1.0	19.0 13.5	
Maximum Clock Frequency	f_{MAX}		2.7 3.3 ± 0.3	55 70	110 130	− −	45 65	− −	MHz
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	− −	− −	1.5 1.5	− −	1.5 1.5	ns
Input Capacitance	C_{IN}	(Note 2)		−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		−	39	−	−	−	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	−	0.8	V

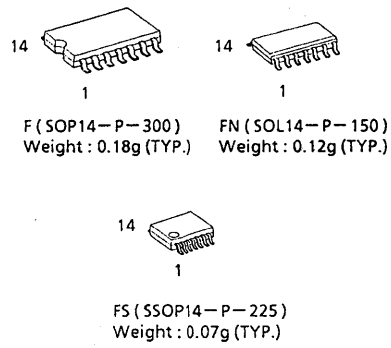
TC74LVQ86F/FN/FS

QUAD EXCLUSIVE OR GATE

The TC74LVQ86 is a high speed CMOS EXCLUSIVE OR GATE fabricated with silicon gate and double - layer metal wiring C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 5.6ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2.5μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance ·· $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays ···· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC86

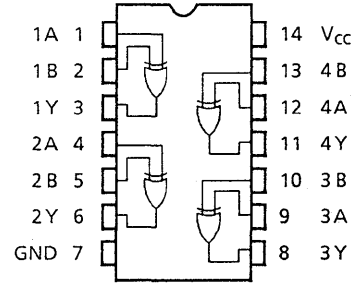


F (SOP14-P-300)
Weight : 0.18g (TYP.)

FN (SOL14-P-150)
Weight : 0.12g (TYP.)

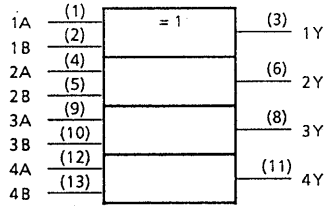
FS (SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.5	—	25.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	7.8 6.5	16.2 11.5	1.0 1.0	18.0 12.5	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	27	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\ \Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

TC74LVQ138F/FN/FS

3 – TO – 8 LINE DECODER

The TC74LVQ138 is a high speed CMOS DECODER fabricated with silicon gate and double - layer metal wiring C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ($\overline{Y}0$ - $\overline{Y}7$) will go low.

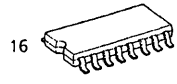
When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

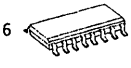
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed ..... t_{pd} = 7.2ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC138



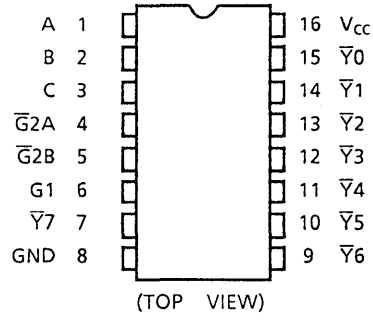
F (SOP16–P–300)
Weight : 0.18g (TYP.)



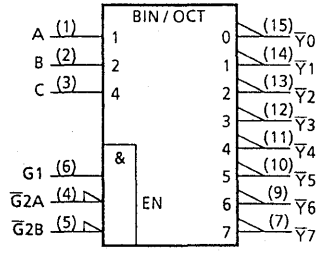
FN (SOL16–P–150)
Weight : 0.13g (TYP.)

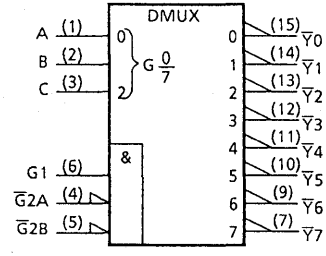
FS (SSOP16–P–225B)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



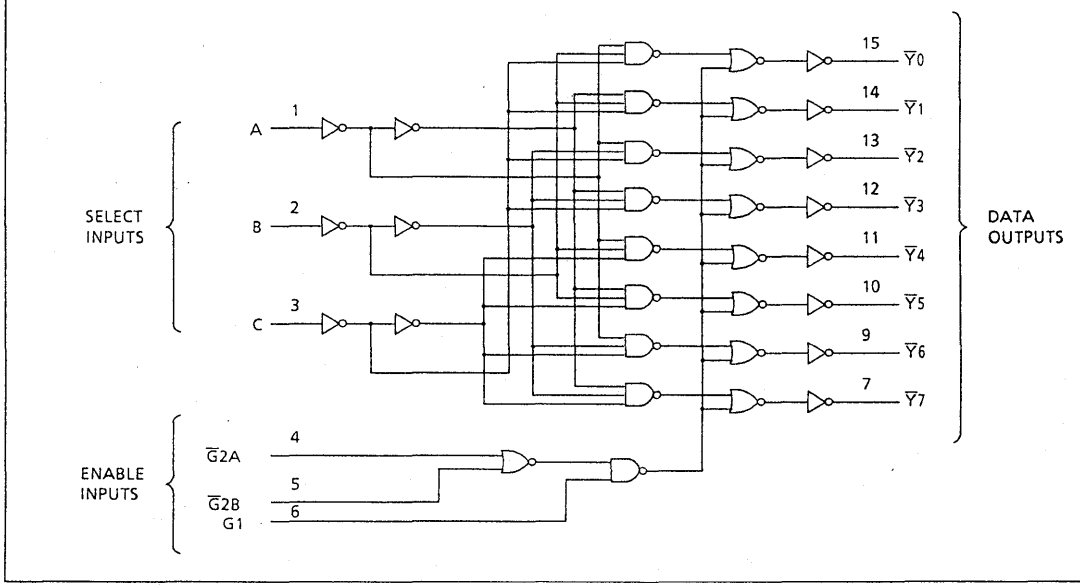


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G}$2A	$\overline{G}$2B	C	B	A	$\overline{Y}$0	$\overline{Y}$1	$\overline{Y}$2	$\overline{Y}$3	$\overline{Y}$4	$\overline{Y}$5	$\overline{Y}$6	$\overline{Y}$7	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y}$0
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y}$1
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y}$2
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y}$3
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y}$4
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y}$5
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y}$6
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y}$7

X : Don't Care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B, C − $\overline{Y}$)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	9.5 7.9	18.3 13.0	1.0 1.0	22.0 15.0	ns
Propagation Delay Time (G1 − $\overline{Y}$)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	8.5 7.1	21.8 15.5	1.0 1.0	24.0 16.5	
Propagation Delay Time ($\overline{G2}$ − $\overline{Y}$)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	10.1 8.4	21.1 15.0	1.0 1.0	23.0 16.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	2.5 2.5	— —	2.5 2.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	83	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\ \Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	—	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	—	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

TC74LVQ151F/FN/FS

8 – CHANNEL MULTIPLEXER

The TC74LVQ151 is a high speed CMOS MULTIPLEXER fabricated with silicon gate and double - layer metal wiring C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

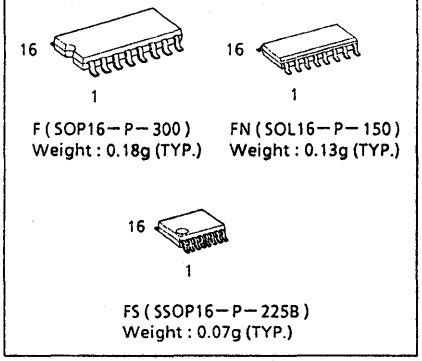
One of eight date input signals (D0 - D7) is selected by decoding of the three - bit address input (A, B, C). The selected data appears on two outputs: non - inverting (Y) and inverting (W).

The $\overline{\text{STROBE}}$ input provides two output conditions; a low level on the $\overline{\text{STROBE}}$ input transferrs the selected data to the outputs. A high level at the $\overline{\text{STROBE}}$ forces the Y output low and the W output high.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 7.5ns (typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC151

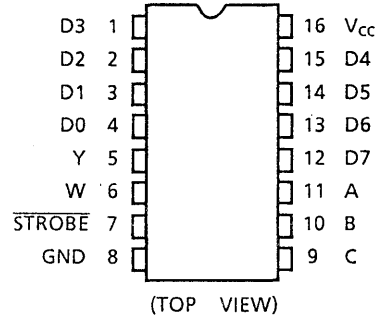


F (SOP16–P–300)
Weight : 0.18g (TYP.)

FN (SOL16–P–150)
Weight : 0.13g (TYP.)

FS (SSOP16–P–225B)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT

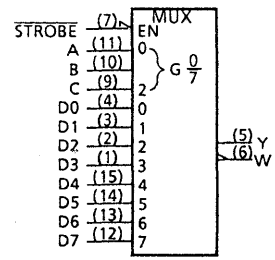


TRUTH TABLE

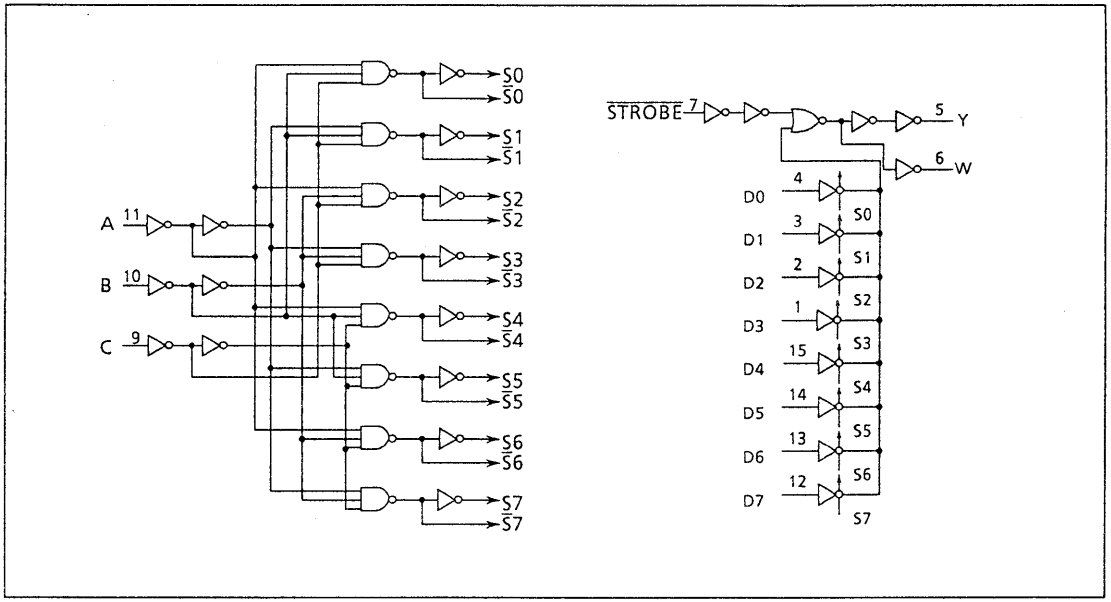
INPUTS				OUTPUTS	
SELECT			$\overline{\text{STROBE}}$	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{\text{D0}}$
L	L	H	L	D1	$\overline{\text{D1}}$
L	H	L	L	D2	$\overline{\text{D2}}$
L	H	H	L	D3	$\overline{\text{D3}}$
H	L	L	L	D4	$\overline{\text{D4}}$
H	L	H	L	D5	$\overline{\text{D5}}$
H	H	L	L	D6	$\overline{\text{D6}}$
H	H	H	L	D7	$\overline{\text{D7}}$

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns, C_L = 50pF, R_L = 500Ω)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (D − Y, W)	t_{pLH}		2.7	—	10.1	21.1	1.0	23.0	ns
	t_{pHL}		3.3 ± 0.3	—	8.4	15.0	1.0	16.0	ns
Propagation Delay Time (A, B, C − Y, W)	t_{pLH}		2.7	—	12.6	25.3	1.0	29.0	ns
	t_{pHL}		3.3 ± 0.3	—	10.5	18.0	1.0	20.0	ns
Propagation Delay Time ($\overline{STROBE}$ − Y, W)	t_{pLH}		2.7	—	8.9	18.3	1.0	20.0	ns
	t_{pHL}		3.3 ± 0.3	—	7.4	13.0	1.0	14.0	ns
Output to Output Skew	t_{osLH}	(Note 1)	2.7	—	—	1.5	—	1.5	ns
	t_{osHL}		3.3 ± 0.3	—	—	1.5	—	1.5	ns
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	61	—	—	—	pF

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\ \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	—	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	—	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

TC74LVQ157F/FN/FS

QUAD 2 - CHANNEL MULTIPLEXER

The TC74LVQ157 is a high speed CMOS MULTIPLEXER fabricated with silicon gate and double - layer metal wiring C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It consists of four 2 - input digital multiplexers with common select and strobe inputs.

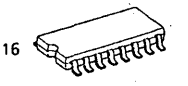
When the $\overline{\text{STROBE}}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level.

The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

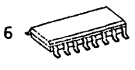
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

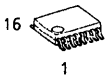
- High Speed ..... t_{pd} = 5.6ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC157



F(SOP16-P-300)
Weight : 0.18g (TYP.)

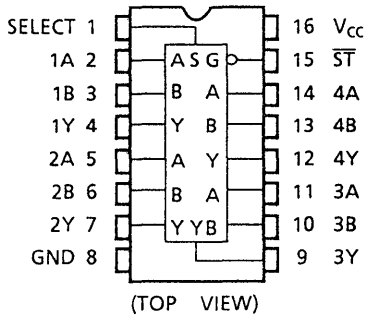


FN(SOL16-P-150)
Weight : 0.13g (TYP.)



FS(SSOP16-P-225B)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT

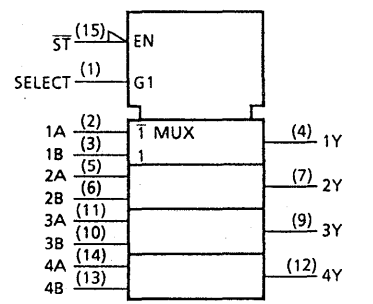


TRUTH TABLE

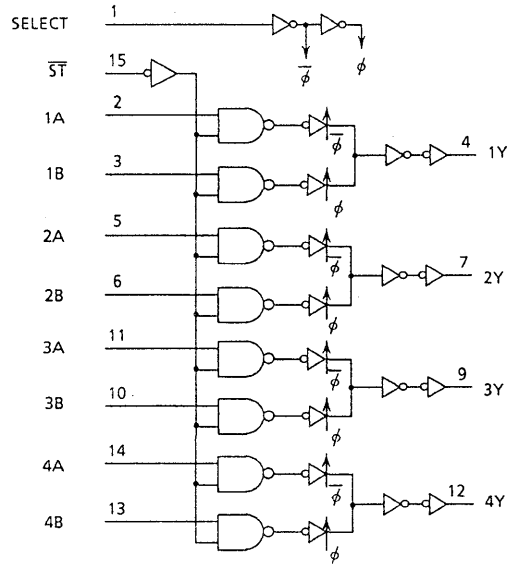
INPUTS				OUTPUTS
$\overline{\text{ST}}$	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns, C_L = 50pF, R_L = 500Ω)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B−Y)	t_{pLH}		2.7	—	7.8	12.7	1.0	15.0	ns
	t_{pHL}		3.3 ± 0.3	—	6.5	9.0	1.0	10.0	ns
Propagation Delay Time (SELECT−Y)	t_{pLH}		2.7	—	8.9	17.3	1.0	20.0	ns
	t_{pHL}		3.3 ± 0.3	—	7.4	12.3	1.0	14.0	ns
Propagation Delay Time ($\overline{ST}$−Y)	t_{pLH}		2.7	—	8.9	17.3	1.0	20.0	ns
	t_{pHL}		3.3 ± 0.3	—	7.4	12.3	1.0	14.0	ns
Output to Output Skew	t_{osLH}	(Note 1)	2.7	—	—	1.5	—	1.5	ns
	t_{osHL}		3.3 ± 0.3	—	—	1.5	—	1.5	ns
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	41	—	—	—	pF

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

And the total C_{PD} when n pcs. of Bit operate can be gained by the following equation:

$$C_{PD}(total) = 13 + 7 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	−	0.8	V

TC74LVQ174F/FN/FS

HEX D-TYPE FLIP FLOP WITH CLEAR

The TC74LVQ174 is a high speed CMOS HEX D - FLIP FLOP fabricated with silicon gate and double - layer metal wiring C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

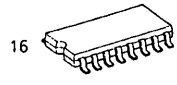
Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse.

When the $\overline{CLR}$ input is held low, the Q output are in the low logic level independent of the other inputs.

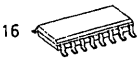
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

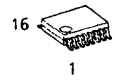
- High Speed ..... f_{MAX} = 165MHz (typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance ·· $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays ···· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC174



F (SOP16-P-300)
Weight : 0.18g (TYP.)

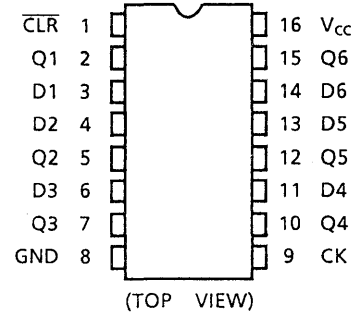


FN (SOL16-P-150)
Weight : 0.13g (TYP.)



FS (SSOP16-P-225B)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT

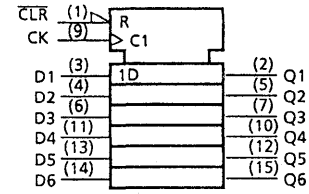


TRUTH TABLE

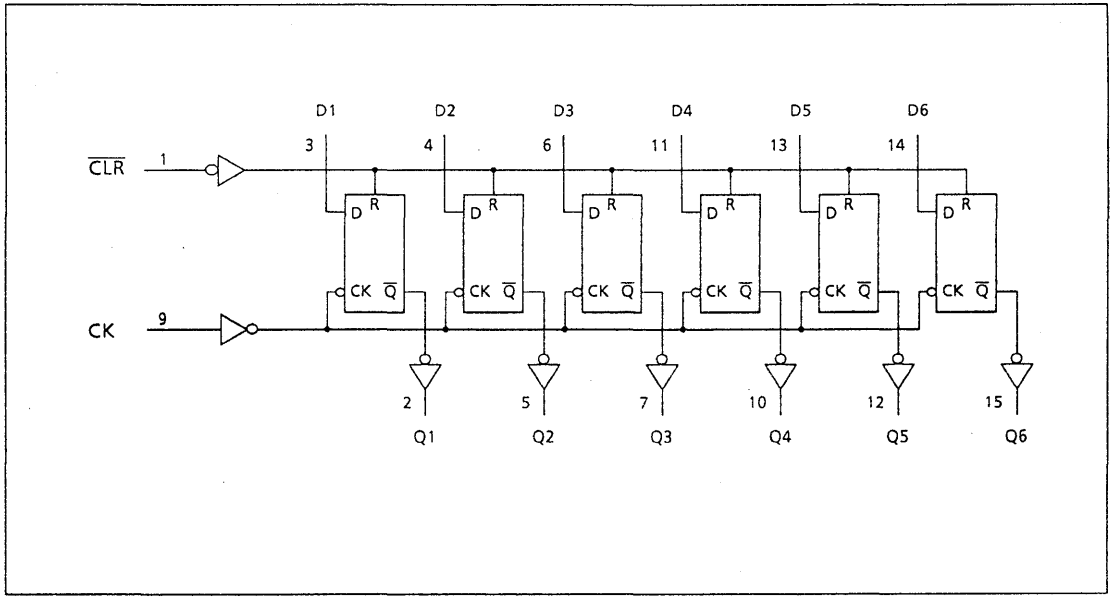
INPUTS			OUTPUTS	FUNCTION
$\overline{CLR}$	D	CK	Q	
L	X	X	L	CLEAR
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q_n	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 150	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C	Ta = −40~85°C	UNIT
		V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$	2.7	9.0	10.0	ns
	$t_{W(H)}$	3.3 ± 0.3	7.0	7.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$	2.7	9.0	10.0	ns
		3.3 ± 0.3	7.0	7.0	ns
Minimum Set - up Time	t_s	2.7	9.0	10.0	ns
		3.3 ± 0.3	7.0	7.0	ns
Minimum Hold Time	t_h	2.7	1.0	1.0	ns
		3.3 ± 0.3	1.0	1.0	ns
Minimum Removal Time ($\overline{CLR}$)	t_{rem}	2.7	7.5	8.5	ns
		3.3 ± 0.3	6.0	6.0	ns

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	8.2 6.8	16.2 11.5	1.0 1.0	19.0 13.0	ns
Propagation Delay Time ($\overline{CLR}$−Q)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	7.9 6.6	16.2 11.5	1.0 1.0	18.0 12.5	ns
Maximum Clock Frequency	f_{MAX}		2.7 3.3 ± 0.3	55 80	120 145	— —	50 70	— —	MHz
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	ns
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	36	—	—	—	pF

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total) = 25 + 11 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

TC74LVQ240F/FW/FS,TC74LVQ241F/FW/FS TC74LVQ244F/FW/FS

OCTAL BUS BUFFER
TC74LVQ240 INVERTED, 3-STATE OUTPUTS
TC74LVQ241 NON-INVERTED, 3-STATE OUTPUTS
TC74LVQ244 NON-INVERTED, 3-STATE OUTPUTS

The TC74LVQ240, 241 and 244 are high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate and double-layer metal wiring C²MOS technology.

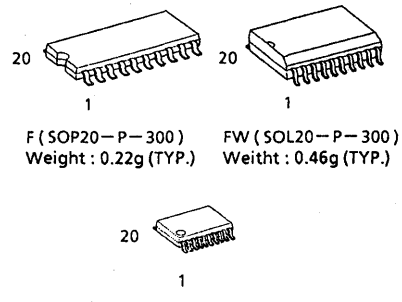
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. The TC74LVQ240 is an inverting 3-state buffer having two active-low output enables. The TC74LVQ241 and TC74LVQ244 are non-inverting 3-state buffers that differ only in that the LVQ241 has one active-high and one active-low output enable, and the LVQ244 has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 5.4ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC240/241/244



F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)

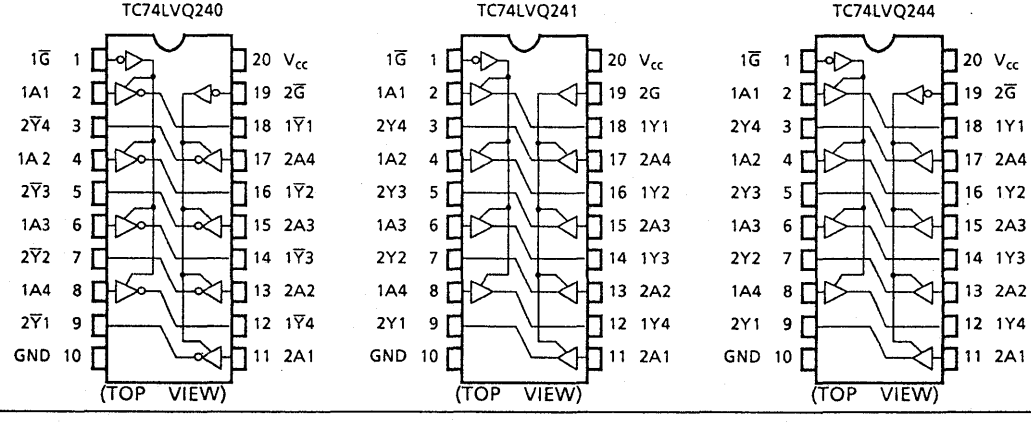
FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

TRUTH TABLE

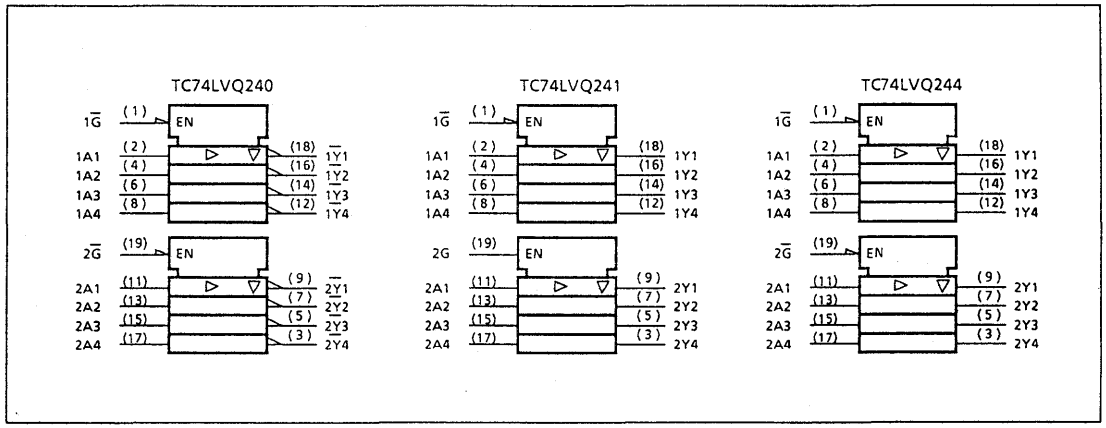
INPUTS			OUTPUTS	
$\overline{G}$	G△	A_n	Y_n	$\overline{Y}_n$△△
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

△ : for TC74LVQ241 only
△△ : for TC74LVQ240 only
X : Don't Care
Z : High Impedance

PIN ASSIGNMENT



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns, C_L = 50pF, R_L = 500Ω)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (TC74LVQ240)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	7.2 6.0	14.1 10.0	1.0 1.0	15.0 10.5	ns
Propagation Delay Time (TC74LVQ241/244)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	7.8 6.5	13.4 9.5	1.0 1.0	15.0 10.5	ns
Output Enable Time	t_{pZL} t_{pZH}		2.7 3.3 ± 0.3	— —	9.5 7.9	18.3 13.0	1.0 1.0	19.0 13.5	ns
Output Disable Time	t_{pLZ} t_{pHZ}		2.7 3.3 ± 0.3	— —	7.2 6.0	19.0 13.5	1.0 1.0	20.0 14.0	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	ns
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Output Capacitance	C_{OUT}			—	10	—	—	—	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	30	—	—	—	pF

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	−	0.8	V

TC74LVQ245F/FW/FS

OCTAL BUS TRANSCEIVER

The TC74LVQ245 is a high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

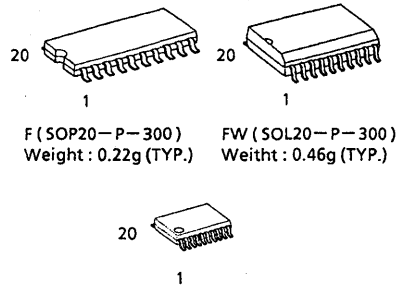
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed ..... t_{pd} = 5.8ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC245



F (SOP20-P-300)
Weight : 0.22g (TYP.)

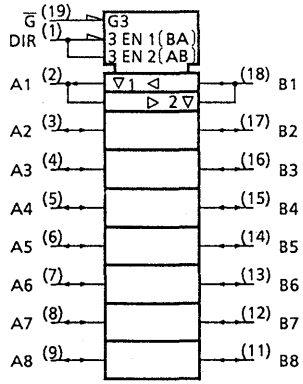
FW (SOL20-P-300)
Weitht : 0.46g (TYP.)

FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

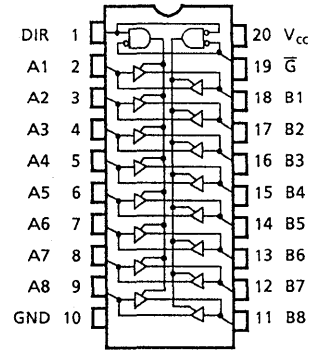
APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

IEC LOGIC SYMBOL



PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS	FUNCTION	
$\overline{G}$	DIR		A – BUS	B – BUS
L	L	A = B	OUTPUT	INPUT
L	H	B = A	INPUT	OUTPUT
H	X	Z	High Impedance	

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage (DIR, $\overline{G}$)	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Bus I/O Voltage	$V_{I/O}$	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage (DIR, $\overline{G}$)	V_{IN}	0~V_{CC}	V
Bus I/O Voltage	$V_{I/O}$	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns, C_L = 50pF, R_L = 500Ω)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}(V)	Ta = 25°C			Ta = −40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		2.7	—	8.0	14.1	1.0	17.0	ns
	t_{pHL}		3.3 ± 0.3	—	6.7	10.0	1.0	11.5	ns
Output Enable Time	t_{pZL}		2.7	—	10.7	18.3	1.0	20.0	ns
	t_{pZH}		3.3 ± 0.3	—	8.9	13.0	1.0	14.0	ns
Output Disable Time	t_{pLZ}		2.7	—	7.9	20.4	1.0	22.0	ns
	t_{pHZ}		3.3 ± 0.3	—	6.6	14.5	1.0	15.0	ns
Output to Output Skew	t_{osLH}	(Note 1)	2.7	—	—	1.5	—	1.5	ns
	t_{osHL}		3.3 ± 0.3	—	—	1.5	—	1.5	ns
Input Capacitance	C_{IN}	DIR, $\overline{G}$ (Note 2)		—	5	10	—	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn		—	13	—	—	—	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	38	—	—	—	pF

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.6	1.0	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.6	−1.0	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	−	0.8	V

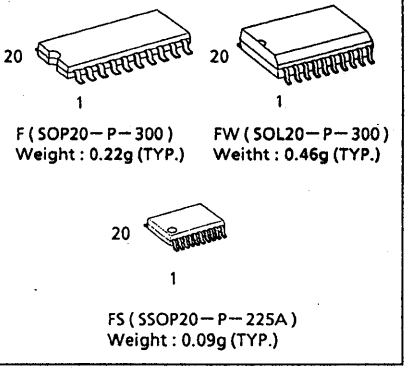
TC74LVQ273F/FW/FS

OCTAL D-TYPE FLIP FLOP WITH CLEAR

The TC74LVQ273 is a high speed CMOS OCTAL D - FLIP FLOP fabricated with silicon gate and double - layer metal wiring C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.
When the $\overline{CLR}$ input is held low, the Q outputs are in the low logic level independent of the other inputs.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX} = 160MHz (typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC273

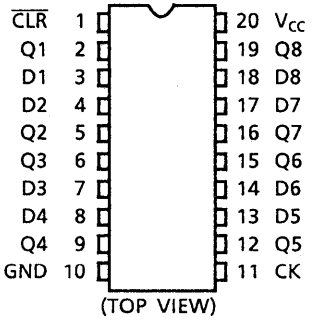


F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)

FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

PIN ASSIGNMENT



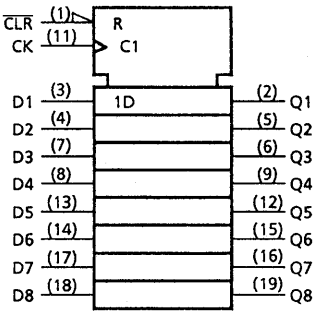
(TOP VIEW)

TRUTH TABLE

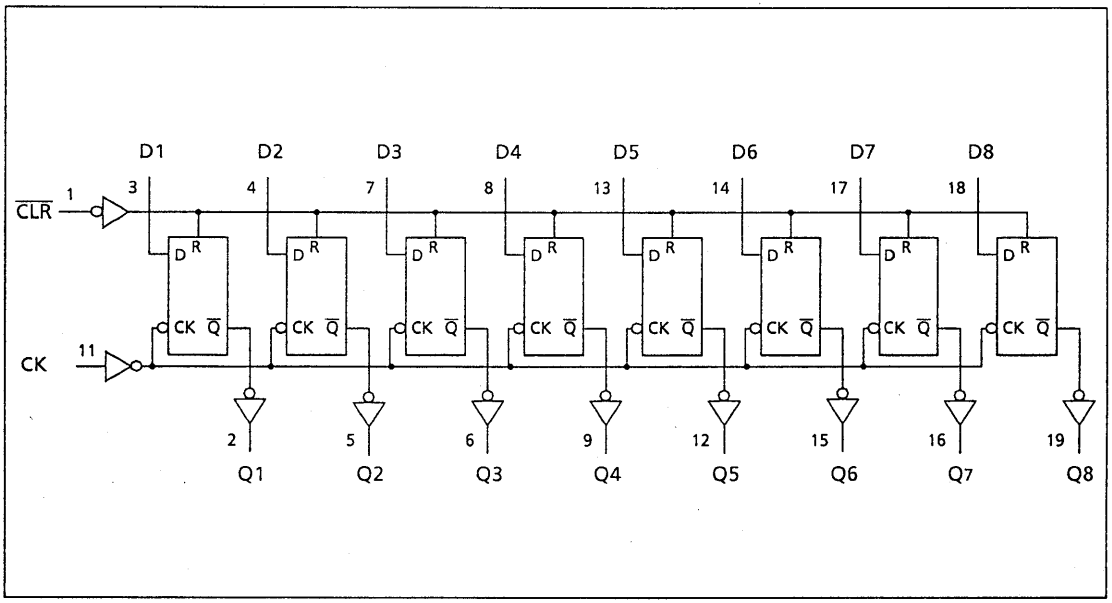
INPUTS			OUTPUTS	FUNCTION
$\overline{CLR}$	D	CK	Q	
L	X	X	L	CLEAR
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q_n	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C	Ta = −40~85°C	UNIT
		V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$	2.7	10.0	11.5	ns
	$t_{W(H)}$	3.3±0.3	8.0	8.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$	2.7	9.5	11.0	ns
		3.3±0.3	7.5	7.5	ns
Minimum Set - up Time	t_s	2.7	10.5	12.0	ns
		3.3±0.3	8.5	8.5	ns
Minimum Hold Time	t_h	2.7	0.0	0.0	ns
		3.3±0.3	0.0	0.0	ns
Minimum Removal Time ($\overline{CLR}$)	t_{rem}	2.7	9.0	10.0	ns
		3.3±0.3	7.0	7.0	ns

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	8.2 6.8	18.3 13.0	1.0 1.0	21.0 14.5	ns
Propagation Delay Time ($\overline{CLR}$−Q)	t_{pHL}		2.7 3.3 ± 0.3	— —	7.9 6.6	18.3 13.0	1.0 1.0	20.0 14.0	
Maximum Clock Frequency	f_{MAX}		2.7 3.3 ± 0.3	50 75	120 140	— —	40 65	— —	MHz
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	ns
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	40	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total) = 29 + 11 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

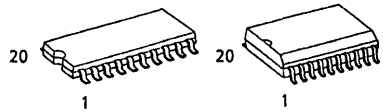
TC74LVQ373F/FW/FS

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74LVQ373 is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
This 8-bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

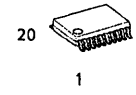
FEATURES:

- High Speed ..... t_{pd} = 6.6ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}|$ = I_{OL} = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC373



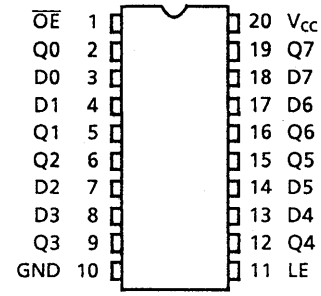
F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)



FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

PIN ASSIGNMENT



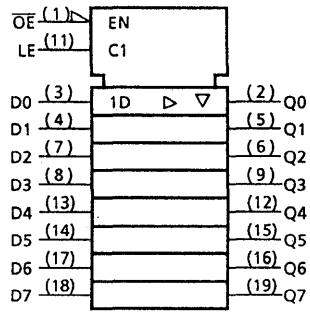
(TOP VIEW)

TRUTH TABLE

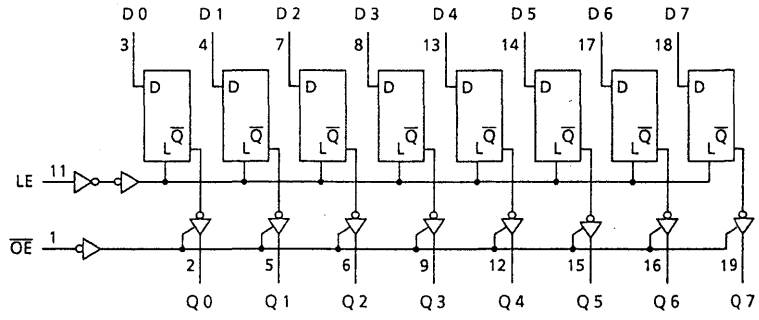
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Inpedance
Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	V
High - Leve Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	V
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	V
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C	Ta = −40~85°C	UNIT
		V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (LE)	$t_{W(H)}$	2.7	9.0	10.0	ns
		3.3 ± 0.3	7.0	7.0	ns
Minimum Set - up Time	t_s	2.7	7.5	8.5	ns
		3.3 ± 0.3	6.0	6.0	ns
Minimum Hold Time	t_h	2.7	1.0	1.0	ns
		3.3 ± 0.3	1.0	1.0	ns

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (LE − Q)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	9.0 7.5	17.6 12.5	1.0 1.0	19.0 13.5	ns
Propagation Delay Time (D − Q)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	8.5 7.1	15.5 11.0	1.0 1.0	17.0 12.0	
Output Enable Time	t_{pZL} t_{pZH}		2.7 3.3 ± 0.3	— —	8.5 7.1	18.3 13.0	1.0 1.0	19.0 13.5	
Output Disable Time	t_{pLZ} t_{pHZ}		2.7 3.3 ± 0.3	— —	7.6 6.3	20.4 14.5	1.0 1.0	22.0 15.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Output Capacitance	C_{OUT}			—	10	—	—	—	
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	38	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Latch)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(total) = 26 + 12 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

TC74LVQ374F/FW/FS

OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUT

The TC74LVQ374 is a high speed CMOS OCTAL FLIP FLOP with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

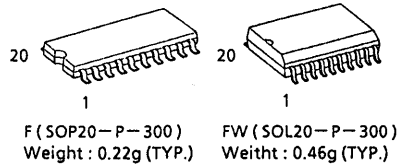
This 8-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX} = 135MHz (typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC374

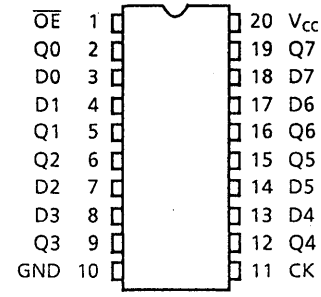


F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)

FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

PIN ASSIGNMENT



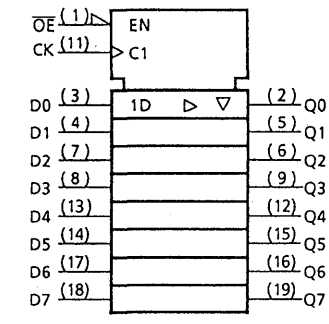
(TOP VIEW)

TRUTH TABLE

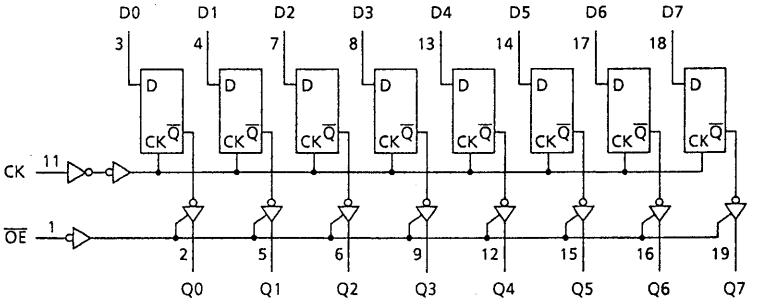
INPUTS			OUTPUTS
$\overline{OE}$	CK	D	
H	X	X	Z
L	↓	X	Q_n
L	↑	L	L
L	↑	H	H

X : Don't Care
Z : High Impedance
Q_n : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC}/Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C	Ta = −40~85°C	UNIT
		V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	2.7 3.3 ± 0.3	9.0 7.0	10.0 7.0	ns
Minimum Set - up Time	t_s	2.7 3.3 ± 0.3	11.5 9.0	13.0 9.0	
Minimum Hold Time	t_h	2.7 3.3 ± 0.3	0.0 0.0	0.0 0.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	9.7 8.1	19.0 13.5	1.0 1.0	21.0 14.5	ns
Output Enable Time	t_{pZL} t_{pZH}		2.7 3.3 ± 0.3	— —	8.5 7.1	18.3 13.0	1.0 1.0	20.0 14.0	
Output Disable Time	t_{pLZ} t_{pHZ}		2.7 3.3 ± 0.3	— —	6.4 5.3	20.4 14.5	1.0 1.0	22.0 15.0	
Maximum Clock Frequency	f_{MAX}		2.7 3.3 ± 0.3	50 70	100 120	— —	45 65	— —	MHz
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	ns
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Output Capacitance	C_{OUT}			—	10	—	—	—	
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	37	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(total) = 25 + 12 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

TC74LVQ573F/FW/FS

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74LVQ573 is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

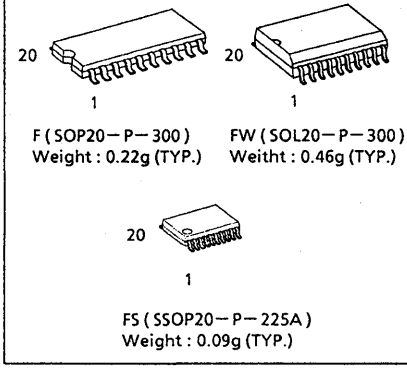
This 8-bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 5.7ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance .. $|I_{OH}| = I_{OL}$ = 12mA(Min.)
- Balanced Propagation Delays .... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC573

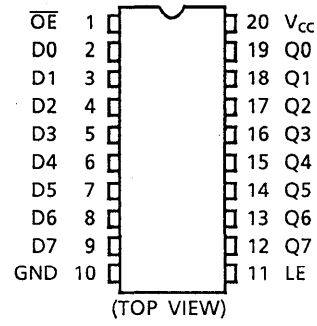


F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)

FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

PIN ASSIGNMENT



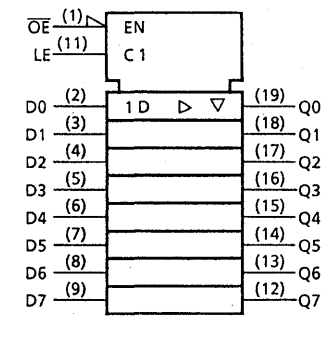
(TOP VIEW)

TRUTH TABLE

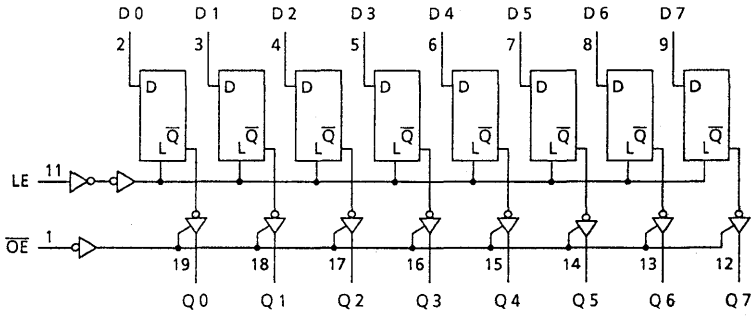
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Inpedance
Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			3.0	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			3.0	—	—	0.8	—	0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	
			I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C	Ta = −40~85°C	UNIT
		V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (LE)	$t_{W(H)}$	2.7	9.0	10.0	ns
		3.3 ± 0.3	7.0	7.0	
Minimum Set - up Time	t_s	2.7	9.0	10.0	
		3.3 ± 0.3	7.0	7.0	
Minimum Hold Time	t_h	2.7	1.0	1.0	
		3.3 ± 0.3	1.0	1.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC}(V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (LE – Q)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	7.9 6.6	16.9 12.0	1.0 1.0	19.0 13.5	ns
Propagation Delay Time (D – Q)	t_{pLH} t_{pHL}		2.7 3.3 ± 0.3	— —	7.7 6.4	14.8 10.5	1.0 1.0	17.0 12.0	
Output Enable Time	t_{pZL} t_{pZH}		2.7 3.3 ± 0.3	— —	8.5 7.1	18.3 13.0	1.0 1.0	19.0 13.5	
Output Disable Time	t_{pLZ} t_{pHZ}		2.7 3.3 ± 0.3	— —	8.0 6.7	20.4 14.5	1.0 1.0	22.0 15.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Output Capacitance	C_{OUT}			—	10	—	—	—	
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	32	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Latch)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(total) = 21 + 11 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.7	1.1	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.7	−1.1	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

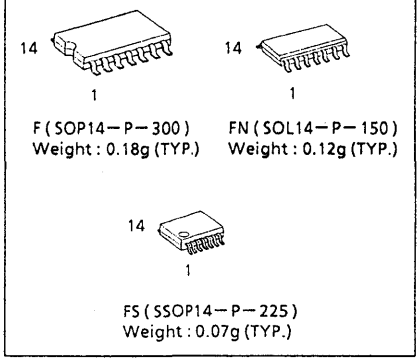
9. TC74LVX SERIES TECHNICAL DATA SHEETS

QUAD 2-INPUT NAND GATE

The TC74LVX00 is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed ..... t_{pd} = 4.1ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ... $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.5V (Max.)
- Pin and Function Compatible with 74HC00

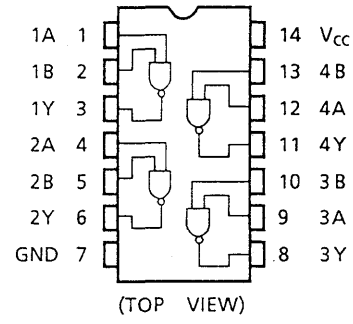


F (SOP14-P-300)
Weight : 0.18g (TYP.)

FN (SOL14-P-150)
Weight : 0.12g (TYP.)

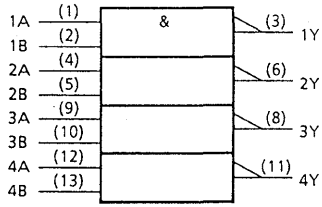
FS (SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.0	—	20.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		2.7	15	—	5.4	10.1	1.0	12.5	ns
	t_{pHL}			50	—	7.9	13.6	1.0	16.0	
			3.3 ± 0.3	15	—	4.1	6.2	1.0	7.5	
				50	—	6.6	9.7	1.0	11.0	
Output to Output Skew	t_{osLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	
	t_{osHL}		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	19	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

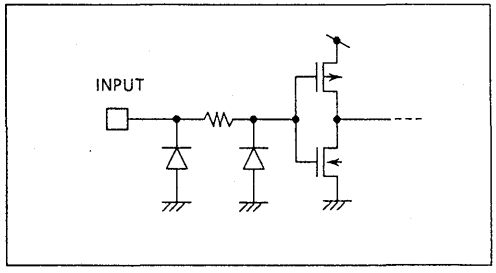
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



TC74LVX02F/FN/FS

QUAD 2-INPUT NOR GATE

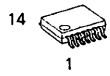
The TC74LVX02 is a high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed ..... t_{pd} = 4.5ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ... $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.5V (Max.)
- Pin and Function Compatible with 74HC02

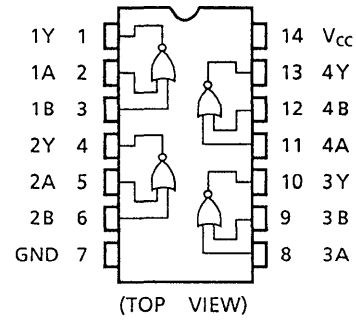
F (SOP14-P-300)
Weight : 0.18g (TYP.)

FN (SOL14-P-150)
Weight : 0.12g (TYP.)



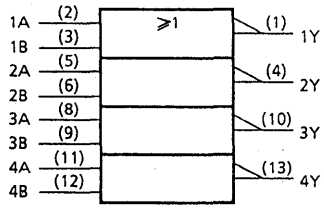
FS (SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	$V_{IN}=V_{IL}$	$I_{OH}=-50\mu A$ $I_{OH}=-50\mu A$ $I_{OH}=-4mA$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	$V_{IN}=$ V_{IH} or V_{IL}	$I_{OL}=50\mu A$ $I_{OL}=50\mu A$ $I_{OL}=4mA$	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		3.6	—	—	2.0	—	20.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7	15	−	5.9	10.7	1.0	13.5	ns
				50	−	8.4	14.2	1.0	17.0	
			3.3 ± 0.3	15	−	4.5	6.6	1.0	8.0	
				50	−	7.0	10.1	1.0	11.5	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	−	−	1.5	−	1.5	
			3.3 ± 0.3	50	−	−	1.5	−	1.5	
Input Capacitance	C_{IN}	(Note 2)			−	4	10	−	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			−	15	−	−	−	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

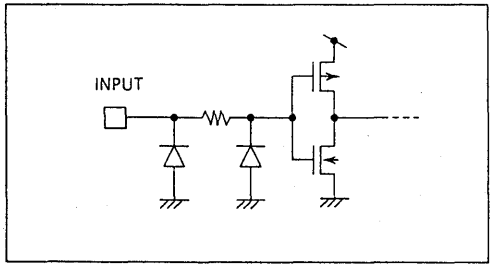
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	−	0.8	V

INPUT EQUIVALENT CIRCUIT



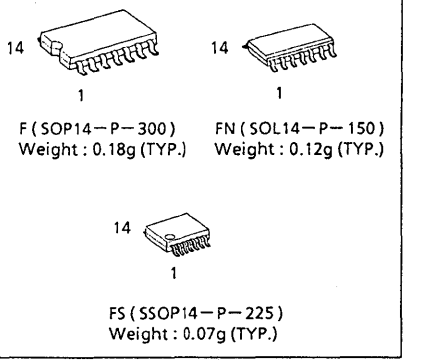
TC74LVX04F/FN/FS

HEX INVERTER

The TC74LVX04 is a high speed CMOS HEX INVERTER fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed ..... t_{pd} = 4.1ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays··· $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.5V (Max.)
- Pin and Function Compatible with 74HC04

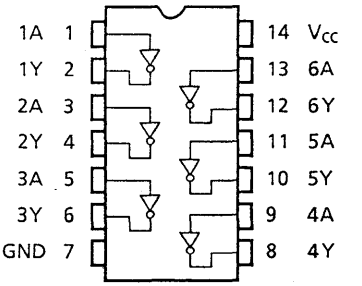


F (SOP14−P−300)
Weight : 0.18g (TYP.)

FN (SOL14−P−150)
Weight : 0.12g (TYP.)

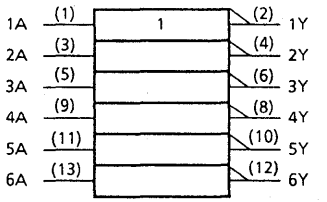
FS (SSOP14−P−225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS	OUTPUTS
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IL}$	$I_{OH} = -50\mu A$ $I_{OH} = -50\mu A$ $I_{OH} = -4mA$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$	$I_{OL} = 50\mu A$ $I_{OL} = 50\mu A$ $I_{OL} = 4mA$	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		3.6	—	—	2.0	—	20.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7	15	−	5.4	10.1	1.0	12.5	ns
				50	−	7.9	13.6	1.0	16.0	
			3.3 ± 0.3	15	−	4.1	6.2	1.0	7.5	
				50	−	6.6	9.7	1.0	11.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	−	−	1.5	−	1.5	
			3.3 ± 0.3	50	−	−	1.5	−	1.5	
Input Capacitance	C_{IN}	(Note 2)			−	4	10	−	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			−	18	−	−	−	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

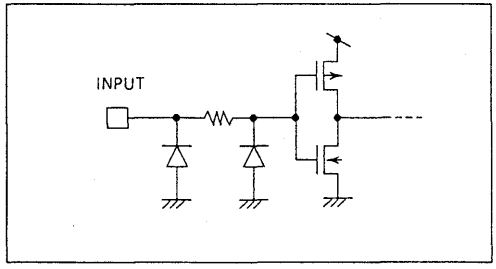
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 6 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	−	0.8	V

INPUT EQUIVALENT CIRCUIT



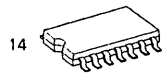
TC74LVX08F/FN/FS

QUAD 2-INPUT AND GATE

The TC74LVX08 is a high speed CMOS 2-INPUT AND GATE fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
The internal circuit is composed of 4 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

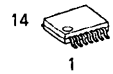
FEATURES:

- High Speed ..... t_{pd} = 4.8ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays··· $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.5V (Max.)
- Pin and Function Compatible with 74HC08



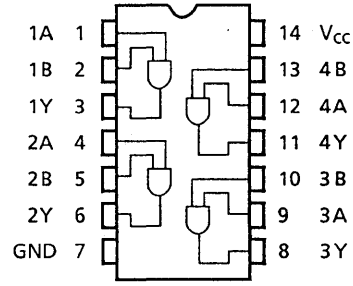
F (SOP14-P-300)
Weight : 0.18g (TYP.)

FN (SOL14-P-150)
Weight : 0.12g (TYP.)



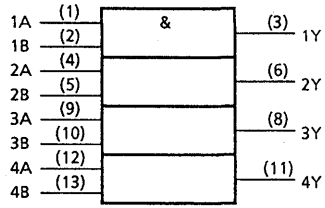
FS (SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.0	—	20.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7	15	−	6.3	11.4	1.0	13.5	ns
				50	−	8.8	14.9	1.0	17.0	
			3.3 ± 0.3	15	−	4.8	7.1	1.0	8.5	
				50	−	7.3	10.6	1.0	12.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	−	−	1.5	−	1.5	
			3.3 ± 0.3	50	−	−	1.5	−	1.5	
Input Capacitance	C_{IN}	(Note 2)			−	4	10	−	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			−	18	−	−	−	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

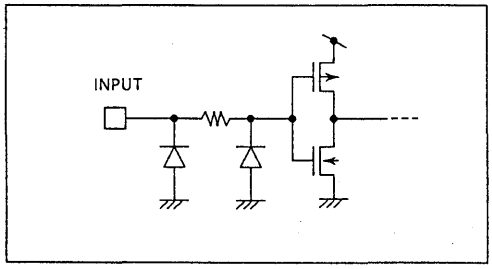
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	−	0.8	V

INPUT EQUIVALENT CIRCUIT



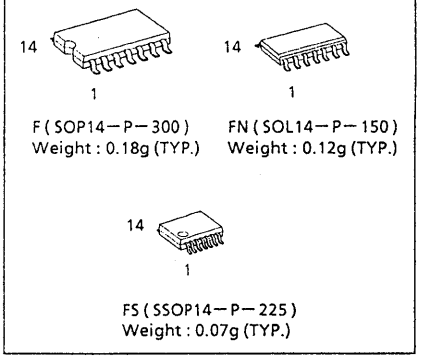
TC74LVX14F/FN/FS

HEX SCHMITT INVERTER

The TC74LVX14 is a high speed CMOS HEX SCHMITT INVERTER fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
Pin configuration and function are the same as the TC74LVX04 but the inputs have hysteresis and with its schmitt trigger function, the TC74LVX14 can be used as a line receivers which will receive slow input signals.
An input protection circuit endures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up.
This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed····· t_{pd} = 6.8ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation····· I_{CC} = 2μA(Max.) at Ta = 25°C
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays··· $t_{pLH} \simeq t_{pHL}$
- Low Noise ····· V_{OLP} = 0.5V (Max.)
- Pin and Function Compatible with 74HC14

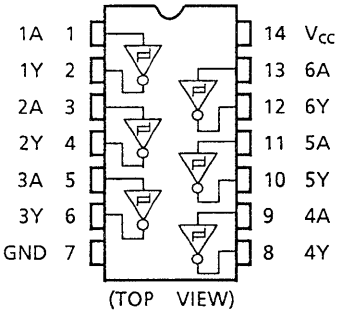


F (SOP14−P−300)
Weight : 0.18g (TYP.)

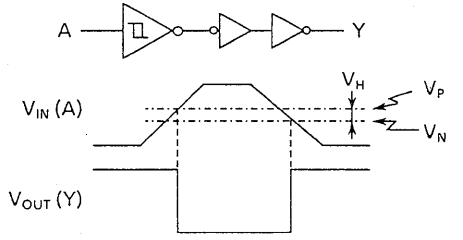
FN (SOL14−P−150)
Weight : 0.12g (TYP.)

FS (SSOP14−P−225)
Weight : 0.07g (TYP.)

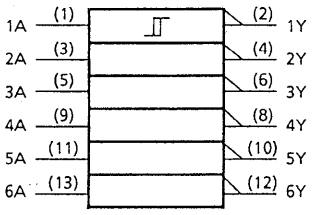
PIN ASSIGNMENT



SYSTEM DIAGRAM, WAVEFORM



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS	OUTPUTS
A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Positive Threshold Voltage	V_P			3.0	—	—	2.2	—	2.2	V
Negative Threshold Voltage	V_N			3.0	0.9	—	0.9	—	—	
Hysteresis Voltage	V_H			3.0	0.3	—	1.2	0.3	1.2	
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IL}$	$I_{OH} = -50\mu A$ $I_{OH} = -50\mu A$ $I_{OH} = -4mA$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$	$I_{OL} = 50\mu A$ $I_{OL} = 50\mu A$ $I_{OL} = 4mA$	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		3.6	—	—	2.0	—	20.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		2.7	15	—	8.7	16.3	1.0	19.5	ns
				50	—	11.2	19.8	1.0	23.0	
	t_{pHL}		3.3 ± 0.3	15	—	6.8	10.6	1.0	12.5	
				50	—	9.3	14.1	1.0	16.0	
Output to Output Skew	t_{osLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	
	t_{osHL}		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	21	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

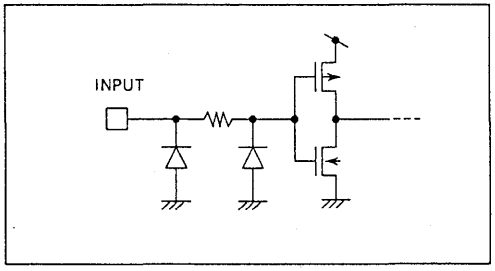
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 6 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.2	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.9	V

INPUT EQUIVALENT CIRCUIT



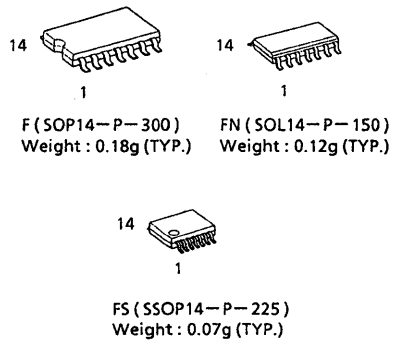
TC74LVX32F/FN/FS

QUAD 2-INPUT OR GATE

The TC74LVX32 is a high speed CMOS 2-INPUT OR GATE fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
The internal circuit is composed of 4 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed ..... t_{pd} = 4.4ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ... $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.5V (Max.)
- Pin and Function Compatible with 74HC32

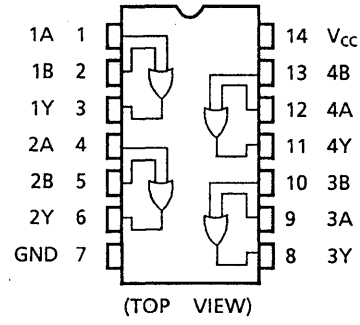


F (SOP14-P-300)
Weight : 0.18g (TYP.)

FN (SOL14-P-150)
Weight : 0.12g (TYP.)

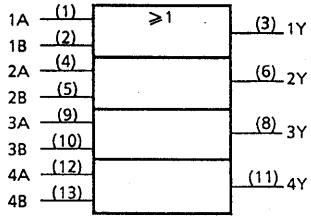
FS (SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.0	—	20.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		2.7	15	—	5.8	10.7	1.0	13.5	ns
				50	—	8.3	14.2	1.0	17.0	
	t_{pHL}		3.3 ± 0.3	15	—	4.4	6.6	1.0	8.0	
				50	—	6.9	10.1	1.0	11.5	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	14	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

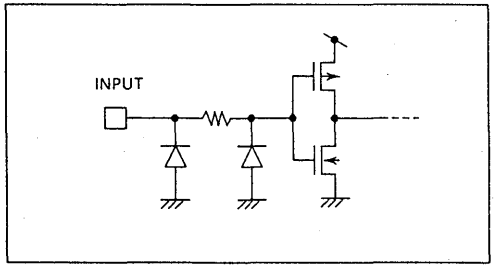
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



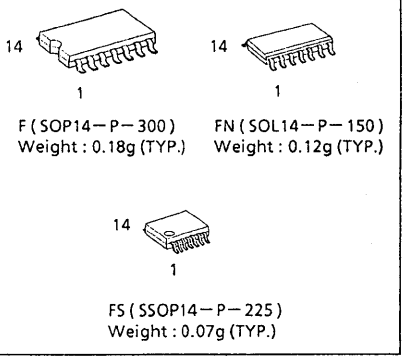
TC74LVX74F/FN/FS

DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

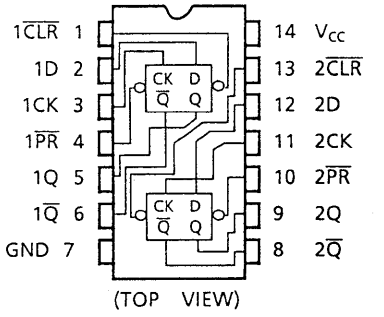
The TC74LVX74 is a high speed CMOS D - FLIP FLOP fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.
$\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input low.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed····· f_{MAX} = 145MHz(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ····· I_{CC} = 2μA(Max.) at Ta = 25°C
- Input Voltage Level····· V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays··· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC74



PIN ASSIGNMENT

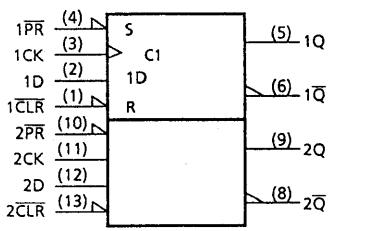


TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.0	—	20.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C	Ta = -40~85°C	UNIT
			V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		2.7 3.3 ± 0.3	8.5 6.0	10.0 7.0	ns
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		2.7 3.3 ± 0.3	8.5 6.0	10.0 7.0	
Minimum Set-up Time	t_s		2.7 3.3 ± 0.3	8.0 5.5	9.5 6.5	
Minimum Hold Time	t_h		2.7 3.3 ± 0.3	0.5 0.5	0.5 0.5	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.7 3.3 ± 0.3	6.5 5.0	7.5 5.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.7	15 50	− −	7.3 9.8	15.0 18.5	1.0 1.0	18.5 22.0	ns
			3.3 ± 0.3	15 50	− −	5.7 8.2	9.7 13.2	1.0 1.0	11.5 15.0	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.7	15 50	− −	8.4 10.9	15.6 19.1	1.0 1.0	18.5 22.0	
			3.3 ± 0.3	15 50	− −	6.6 9.1	10.1 13.6	1.0 1.0	12.0 15.5	
Maximum Clock Frequency	f_{MAX}		2.7	15 50	55 45	135 60	− −	50 40	− −	MHz
			3.3 ± 0.3	15 50	95 60	145 85	− −	80 50	− −	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	−	−	1.5	−	1.5	ns
			3.3 ± 0.3	50	−	−	1.5	−	1.5	
Input Capacitance	C_{IN}	(Note 2)			−	4	10	−	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			−	25	−	−	−	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

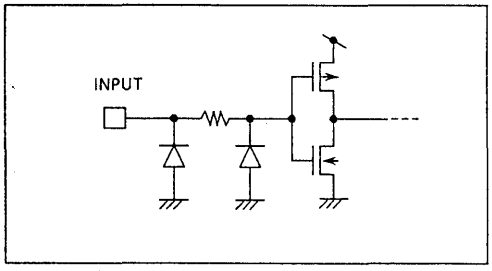
Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



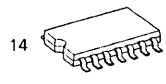
TC74LVX86F/FN/FS

QUAD EXCLUSIVE OR GATE

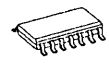
The TC74LVX86 is a high speed CMOS EXCLUSIVE OR GATE fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
The internal circuit is includes on output buffer, which provide high noise immunity and stable output.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

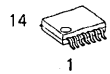
- High Speed ..... t_{pd} = 5.8ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 2μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ··· $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.5V (Max.)
- Pin and Function Compatible with 74HC86



F (SOP14−P−300)
Weight : 0.18g (TYP.)

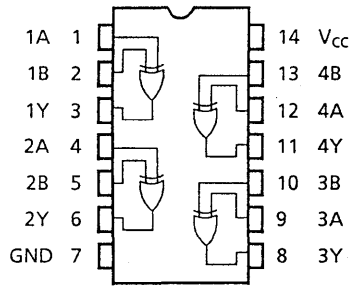


FN (SOL14−P−150)
Weight : 0.12g (TYP.)



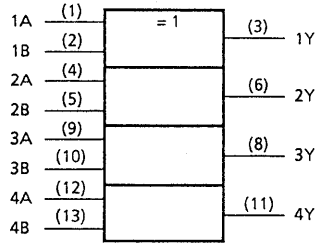
FS (SSOP14−P−225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.0	—	20.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7	15	—	7.5	14.5	1.0	17.5	ns
				50	—	10.0	18.0	1.0	21.0	
			3.3 ± 0.3	15	—	5.8	9.3	1.0	11.0	
				50	—	8.3	12.8	1.0	14.5	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	18	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

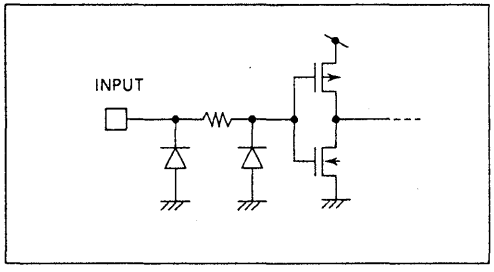
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



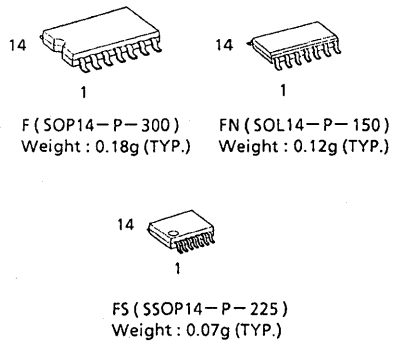
TC74LVX125F/FN/FS

QUAD BUS BUFFER

The TC74LVX125 is a high speed CMOS QUAD BUS BUFFER fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
This device requires the 3-state control input $\overline{G}$ to be set high to place the output into the high impedance.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed ..... t_{pd} = 4.4ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays··· $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.5V(Max.)
- Pin and Function Compatible with 74HC125

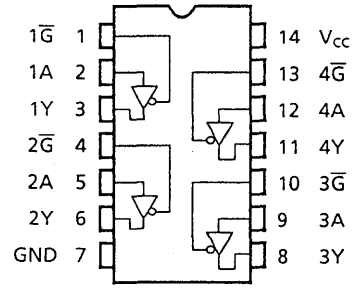


F (SOP14-P-300)
Weight : 0.18g (TYP.)

FN (SOL14-P-150)
Weight : 0.12g (TYP.)

FS (SSOP14-P-225)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



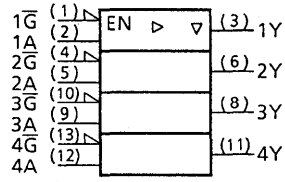
(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X : Don't Care
Z : High Impedance

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
3 - State Output off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.25	—	±2.5	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7	15	—	5.8	10.1	1.0	13.5	ns
				50	—	8.3	13.6	1.0	17.0	
			3.3 ± 0.3	15	—	4.4	6.2	1.0	8.5	
				50	—	6.9	9.7	1.0	12.0	
Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	2.7	15	—	5.3	9.3	1.0	12.5	
				50	—	7.8	12.8	1.0	16.0	
			3.3 ± 0.3	15	—	4.0	5.6	1.0	7.5	
				50	—	6.5	9.1	1.0	11.0	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	2.7	50	—	10.0	15.7	1.0	19.0	
			3.3 ± 0.3	50	—	8.3	11.2	1.0	13.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Output Capacitance	C_{OUT}				—	6	—	—	—	
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	14	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

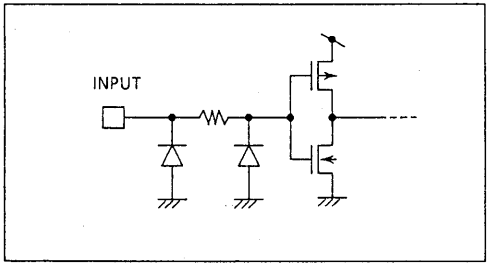
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



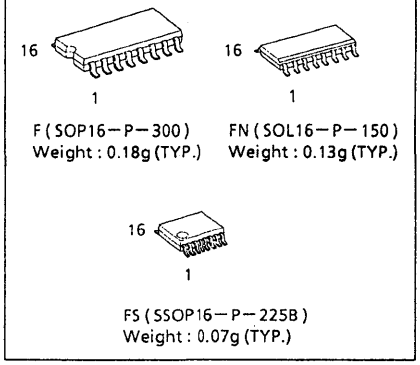
TC74LVX138F/FN/FS

3 – TO – 8 LINE DECODER

The TC74LVX138 is a high speed CMOS 3–TO–8 LINE DECODER fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ($\overline{Y}0 - \overline{Y}7$) will go low. When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.
G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed ..... t_{pd} = 5.5ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ··· $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.5V (Max.)
- Pin and Function Compatible with 74HC138

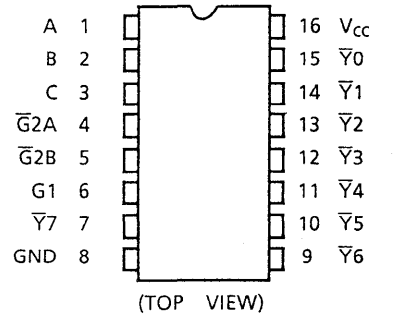


F (SOP16–P–300)
Weight : 0.18g (TYP.)

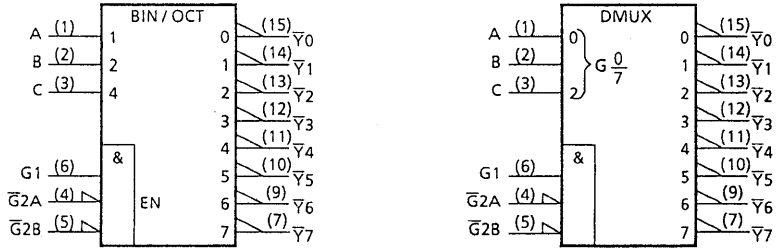
FN (SOL16–P–150)
Weight : 0.13g (TYP.)

FS (SSOP16–P–225B)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL

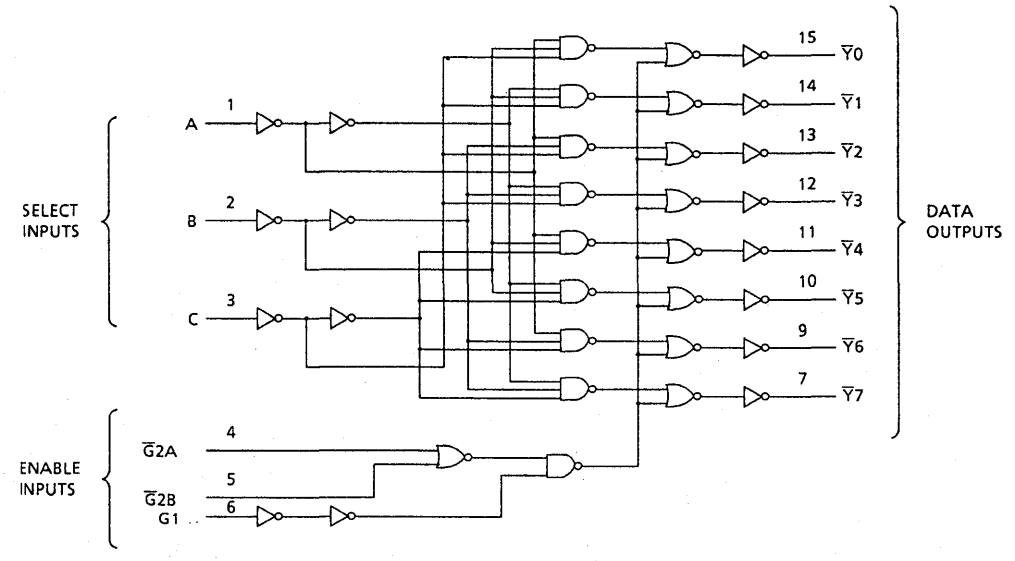


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G}$2A	$\overline{G}$2B	C	B	A	$\overline{Y}$0	$\overline{Y}$1	$\overline{Y}$2	$\overline{Y}$3	$\overline{Y}$4	$\overline{Y}$5	$\overline{Y}$6	$\overline{Y}$7	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y}$0
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y}$1
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y}$2
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y}$3
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y}$4
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y}$5
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y}$6
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y}$7

X : Don't Care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B, C − $\overline{Y}$)	t_{pLH}		2.7	15	−	7.1	13.8	1.0	16.5	ns
				50	−	9.6	17.3	1.0	20.0	
	t_{pHL}		3.3 ± 0.3	15	−	5.5	8.8	1.0	10.5	
				50	−	8.0	12.3	1.0	14.0	
Propagation Delay Time (G1 − $\overline{Y}$)	t_{pLH}		2.7	15	−	8.7	16.3	1.0	19.5	
				50	−	11.2	19.8	1.0	23.0	
	t_{pHL}		3.3 ± 0.3	15	−	6.8	10.6	1.0	12.5	
				50	−	9.3	14.1	1.0	16.0	
Propagation Delay Time ($\overline{G2}$ − $\overline{Y}$)	t_{pLH}		2.7	15	−	8.8	16.0	1.0	18.5	
				50	−	11.3	19.5	1.0	22.0	
	t_{pHL}		3.3 ± 0.3	15	−	6.9	10.4	1.0	11.5	
				50	−	9.4	13.9	1.0	15.0	
Output to Output Skew	t_{osLH}	(Note 1)	2.7	50	−	−	2.5	−	2.5	
	t_{osHL}		3.3 ± 0.3	50	−	−	2.5	−	2.5	
Input Capacitance	C_{IN}	(Note 2)			−	4	10	−	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			−	34	−	−	−	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

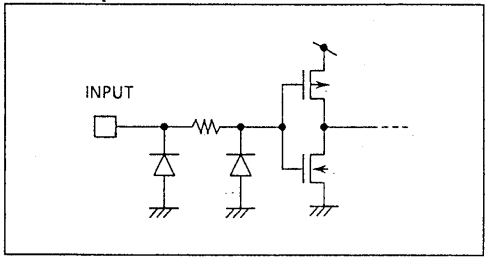
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	−	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	−	0.8	V

INPUT EQUIVALENT CIRCUIT



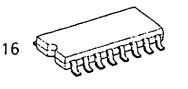
TC74LVX157F/FN/FS

QUAD 2-CHANNEL MULTIPLEXER

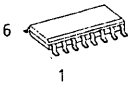
The TC74LVX157 is a high speed CMOS QUAD 2-CHANNEL MULTIPLEXER fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
This device consist of four 2-input digital multiplexers with common select and strobe inputs.
When the $\overline{\text{STROBE}}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level.
The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

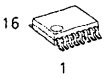
- High Speed ..... t_{pd} = 5.1ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays··· $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.5V (Max.)
- Pin and Function Compatible with 74HC157



F(SOP16-P-300)
Weight : 0.18g (TYP.)

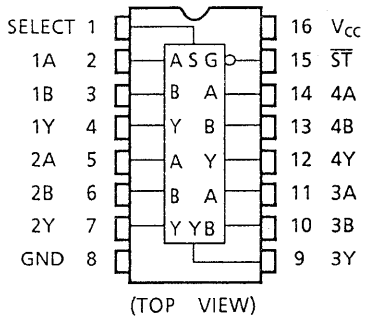


FN(SOL16-P-150)
Weight : 0.13g (TYP.)



FS(SSOP16-P-225B)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT

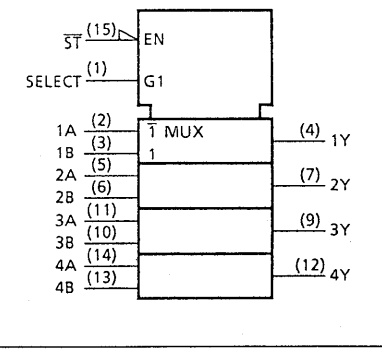


TRUTH TABLE

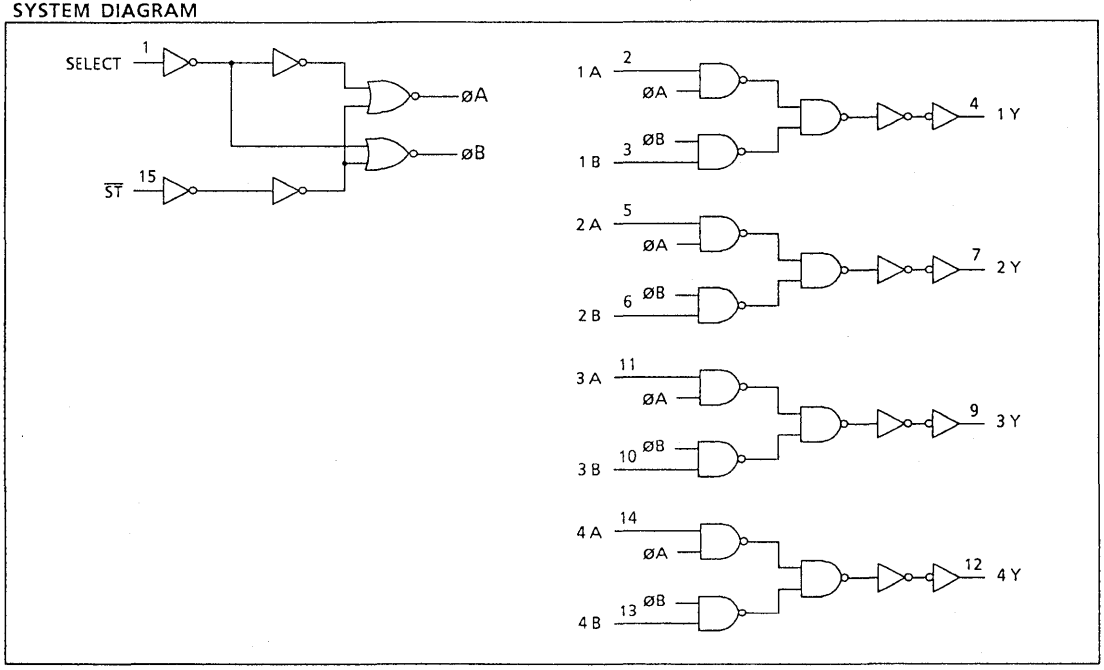
INPUTS				OUTPUTS
$\overline{\text{ST}}$	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	C_L (pF)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Propagation Delay Time (A, B − Y)	t_{pLH} t_{pHL}		2.7	15 50	— —	6.6 9.1	12.5 16.0	1.0 1.0	15.5 19.0	ns
			3.3 ± 0.3	15 50	— —	5.1 7.6	7.9 11.4	1.0 1.0	9.5 13.0	
Propagation Delay Time (SELECT − Y)	t_{pLH} t_{pHL}		2.7	15 50	— —	8.9 11.4	16.9 20.4	1.0 1.0	20.5 24.0	
			3.3 ± 0.3	15 50	— —	7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	
Propagation Delay Time ($\overline{ST}$ − Y)	t_{pLH} t_{pHL}		2.7	15 50	— —	9.1 11.6	17.6 21.1	1.0 1.0	20.5 24.0	
			3.3 ± 0.3	15 50	— —	7.2 9.7	11.5 15.0	1.0 1.0	13.5 17.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	20	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

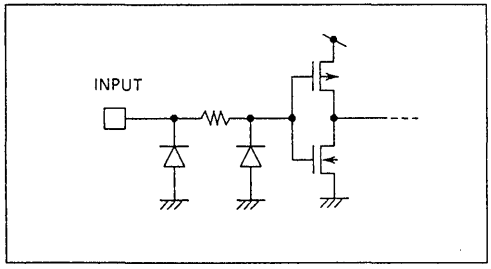
And the total C_{PD} when n pcs. of Gate operate can be gained by the following equation:

$$C_{PD}(total) = 13 + 7 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



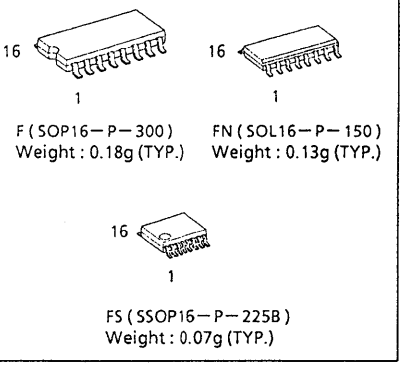
TC74LVX174F/FN/FS

HEX D-TYPE FLIP FLOP WITH CLEAR

The TC74LVX174 is a high speed CMOS HEX D - FLIP FLOP fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
Information signals applied to D inputs are transfered to the Q output on the positivegoing edge of the clock pulse.
When the $\overline{CLR}$ input is held low, the Q output are in the low logic level independent of the other inputs.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed····· f_{MAX} = 180MHz(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level····· V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays··· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74HC174

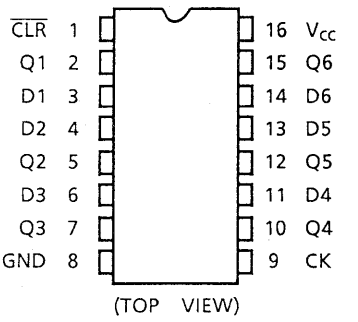


F (SOP16-P-300)
Weight : 0.18g (TYP.)

FN (SOL16-P-150)
Weight : 0.13g (TYP.)

FS (SSOP16-P-225B)
Weight : 0.07g (TYP.)

PIN ASSIGNMENT

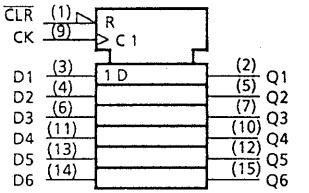


TRUTH TABLE

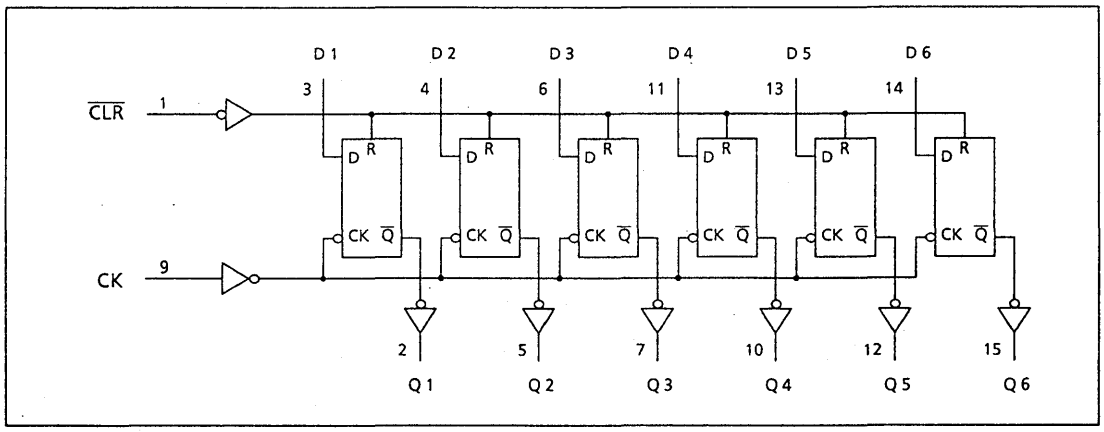
INPUTS			OUTPUTS	FUNCTION
$\overline{CLR}$	D	CK	Q	
L	X	X	L	CLEAR
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q_n	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	Ta = −40~85°C	UNIT
				LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		2.7 3.3 ± 0.3	6.5 5.0	7.5 5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		2.7 3.3 ± 0.3	6.5 5.0	7.5 5.0	
Minimum Set - up Time	t_s		2.7 3.3 ± 0.3	7.5 5.0	8.5 6.0	
Minimum Hold Time	t_h		2.7 3.3 ± 0.3	0.0 0.0	0.0 0.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.7 3.3 ± 0.3	4.5 3.0	4.5 3.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		2.7	15	—	7.6	14.5	1.0	17.5	ns
				50	—	10.1	18.0	1.0	21.0	
			3.3 ± 0.3	15	—	5.9	9.3	1.0	11.0	
				50	—	8.4	12.8	1.0	14.5	
Propagation Delay Time ($\overline{CLR}$−Q)	t_{pLH} t_{pHL}		2.7	15	—	7.9	15.0	1.0	18.5	
				50	—	10.4	18.5	1.0	22.0	
			3.3 ± 0.3	15	—	6.2	9.7	1.0	11.5	
				50	—	8.7	13.2	1.0	15.0	
Maximum Clock Frequency	f_{MAX}		2.7	15	65	130	—	55	—	MHz
				50	45	60	—	40	—	
			3.3 ± 0.3	15	115	180	—	95	—	
				50	65	95	—	55	—	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	29	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

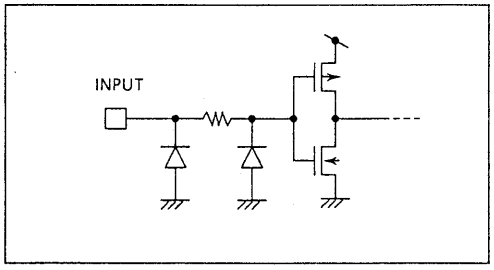
And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(total) = 19 + 10 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	−	0.8	V

INPUT EQUIVALENT CIRCUIT



TC74LVX240F/FW/FS
TC74LVX244F/FW/FS

OCTAL BUS BUFFER
TC74LVX240 INVERTED, 3-STATE OUTPUTS
TC74LVX244 NON-INVERTED, 3-STATE OUTPUTS

The TC74LVX240 and 244 are high speed CMOS OCTAL BUS BUFFERs fabricated using silicon gate C²MOS technology.

Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. These devices are suitable for low voltage and battery operated systems.

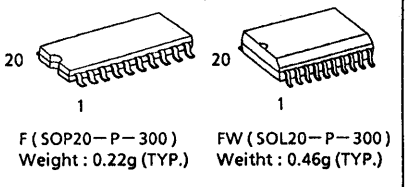
The TC74LVX240 is an inverting 3-state buffer while the TC74LVX244 is non-inverting. Both devices have two active-low output enables.

These devices are designed to be used in such applications as 3-state memory address drivers.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. These devices can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

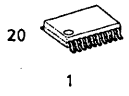
FEATURES:

- High Speed ..... t_{pd} = 4.7ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ... $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with 74HC240/244



F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)



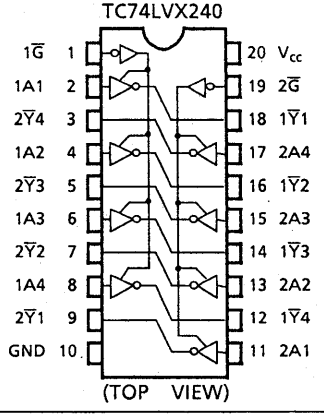
FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

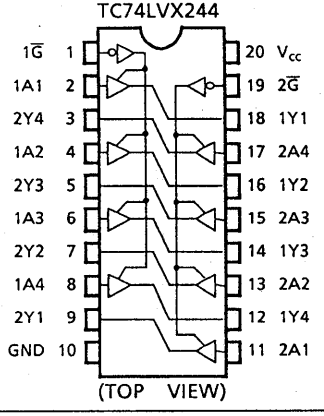
TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{G}$	A_n	$Y_{n(244)}$	$\overline{Y}_{n(240)}$
L	L	L	H
L	H	H	L
H	X	Z	Z

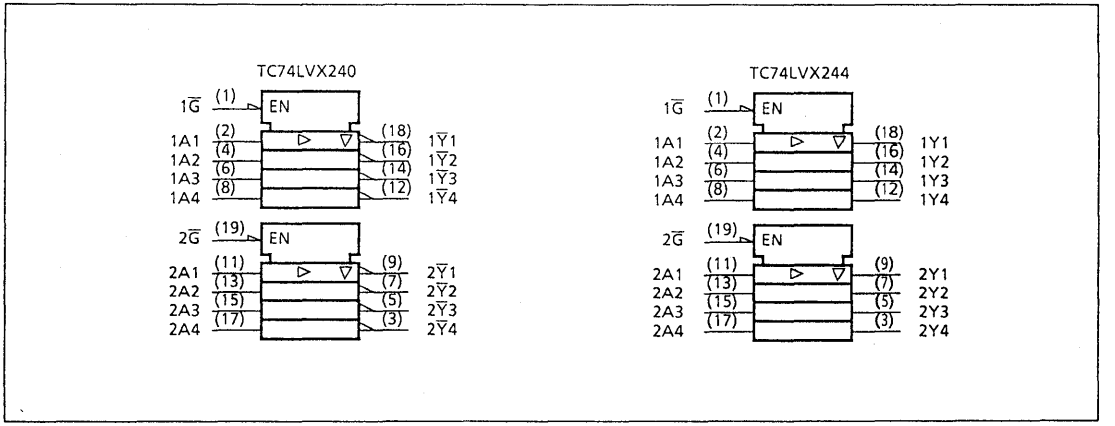
X : Don't Care
Z : High Impedance

PIN ASSIGNMENT





IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.25	—	±2.5	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	C_L (pF)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Propagation Delay Time (TC74LVX240)	t_{pLH} t_{pHL}		2.7	15 50	— —	5.7 8.2	10.1 13.6	1.0 1.0	12.5 16.0	ns
			3.3 ± 0.3	15 50	— —	4.3 6.8	6.2 9.7	1.0 1.0	7.5 11.0	
Propagation Delay Time (TC74LVX244)	t_{pLH} t_{pHL}		2.7	15 50	— —	6.1 8.6	11.4 14.9	1.0 1.0	13.5 17.0	
			3.3 ± 0.3	15 50	— —	4.7 7.2	7.1 10.6	1.0 1.0	8.5 12.0	
Output Enable Time	t_{pZL} t_{pZH}	R_L = 1kΩ	2.7	15 50	— —	7.1 9.6	13.8 17.3	1.0 1.0	16.5 20.0	
			3.3 ± 0.3	15 50	— —	5.5 8.0	8.8 12.3	1.0 1.0	10.5 14.0	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L = 1kΩ	2.7	50	—	11.6	16.0	1.0	19.0	
			3.3 ± 0.3	50	—	9.7	11.4	1.0	13.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	
			3.3 ± 0.3	50	—	—	1.5	—	1.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$) Continue

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = −40~85°C		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}	(Note 2)	−	4	10	−	10	pF
Output Capacitance	C_{OUT}		−	6	−	−	−	
Power Dissipation Capacitance (Note 3)	C_{PD}	TC74LVX240	−	17	−	−	−	
		TC74LVX244	−	19	−	−	−	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

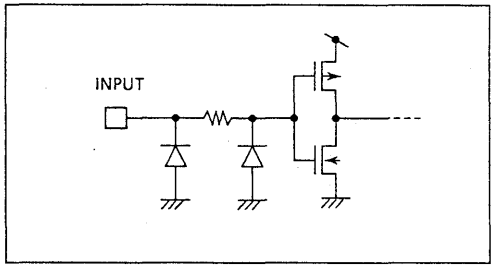
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	−	0.8	V

INPUT EQUIVALENT CIRCUIT



TC74LVX245F/FW/FS

OCTAL BUS TRANSCEIVER

The TC74LVX245 is a high speed CMOS OCTAL BUS TRANSCEIVER fabricated using silicon gate C²MOS technology.

Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. These devices are suitable for low voltage and battery operated systems.

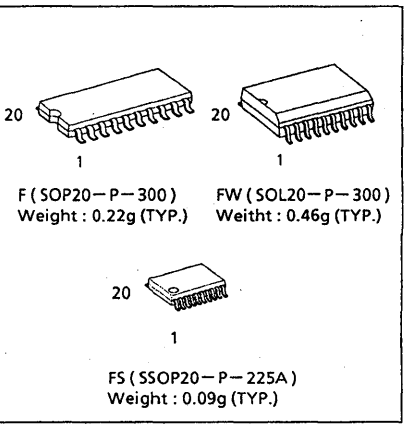
It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

FEATURES:

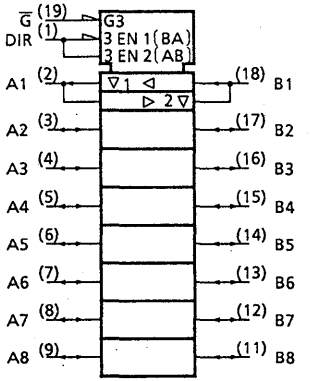
- High Speed ..... t_{pd} = 4.7ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ... $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with 74HC245



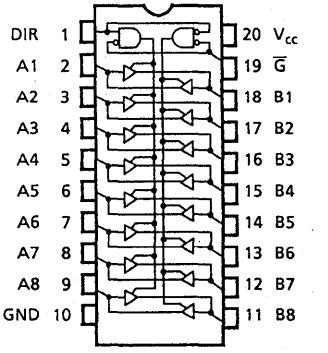
APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.
3) A parasitic diode is formed between the bus and Vcc terminals. Therefore bus terminal can not be used to interface 5V to 3V systems directly.

IEC LOGIC SYMBOL



PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS	FUNCTION	
$\overline{G}$	DIR		A – BUS	B – BUS
L	L	A = B	OUTPUT	INPUT
L	H	B = A	INPUT	OUTPUT
H	X	Z	High Impedance	

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage (DIR, $\overline{G}$)	V_{IN}	−0.5~7.0	V
DC Bus I/O Voltage	$V_{I/O}$	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage (DIR, $\overline{G}$)	V_{IN}	0~5.5	V
Bus I/O Voltage	$V_{I/O}$	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.25	—	±2.5	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7	15 50	— —	6.1 8.6	10.7 14.2	1.0 1.0	13.5 17.0	ns
			3.3 ± 0.3	15 50	— —	4.7 7.2	6.6 10.1	1.0 1.0	8.0 11.5	
Output Enable Time	t_{pZL} t_{pZH}	R_L = 1kΩ	2.7	15 50	— —	9.0 11.5	16.9 20.4	1.0 1.0	20.5 24.0	
			3.3 ± 0.3	15 50	— —	7.1 9.6	11.0 14.5	1.0 1.0	13.0 16.5	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L = 1kΩ	2.7	50	—	11.5	18.0	1.0	21.0	
			3.3 ± 0.3	50	—	9.6	12.8	1.0	14.5	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	DIR, $\overline{G}$ (Note 2)			—	4	10	—	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn			—	8	—	—	—	
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	21	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

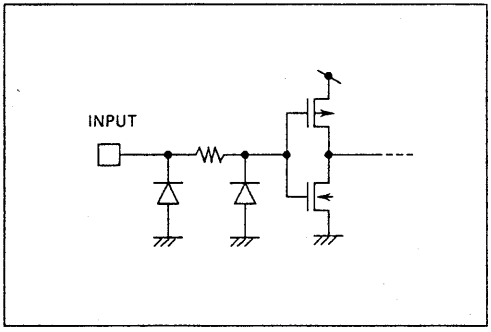
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

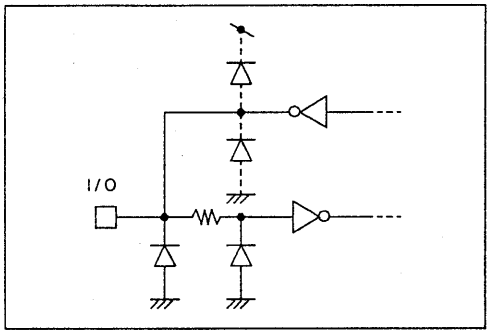
NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	−	0.8	V

INPUT EQUIVALENT CIRCUIT (DIR, $\overline{G}$)



BUS TERMINAL EQUIVALENT CIRCUIT (An, Bn)



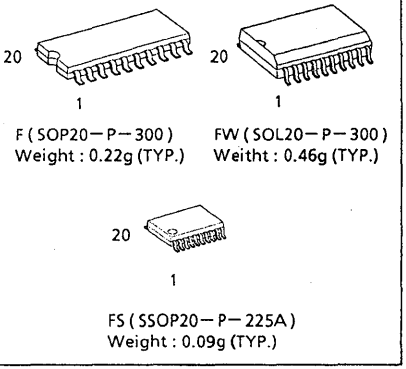
TC74LVX273F/FW/FS

OCTAL D-TYPE FLIP FLOP WITH CLEAR

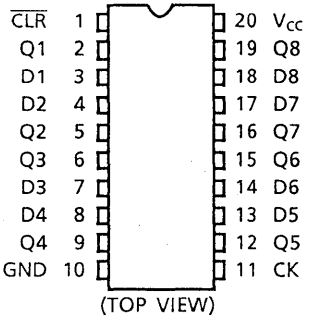
The TC74LVX273 is a high speed CMOS OCTAL D - FLIP FLOP fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.
When the $\overline{CLR}$ input is held low, the Q outputs are in the low logic level independent of the other inputs.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed····· f_{MAX} = 150MHz(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level····· V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays··· $t_{pLH} \simeq t_{pHL}$
- Low Noise ····· V_{OLP} = 0.8V(Max.)
- Pin and Function Compatible with 74HC273



PIN ASSIGNMENT

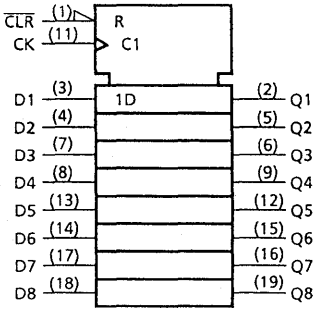


TRUTH TABLE

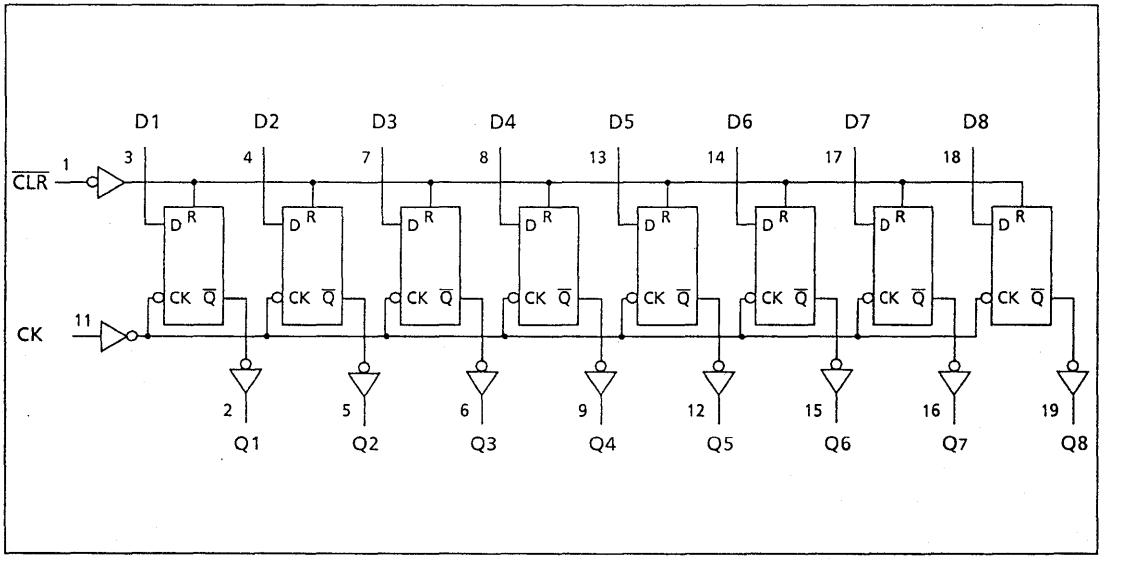
INPUTS			OUTPUTS	FUNCTION
$\overline{CLR}$	D	CK	Q	
L	X	X	L	CLEAR
H	L	↓	L	—
H	H	↓	H	—
H	X	↓	Q_n	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C	Ta = −40~85°C	UNIT
		V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	2.7 3.3 ± 0.3	8.0 5.5	9.5 6.5	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$	2.7 3.3 ± 0.3	7.5 5.0	8.5 6.0	
Minimum Set - up Time	t_s	2.7 3.3 ± 0.3	8.0 5.5	9.5 6.5	
Minimum Hold Time	t_h	2.7 3.3 ± 0.3	1.0 1.0	1.0 1.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}	2.7 3.3 ± 0.3	4.0 2.5	4.0 2.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		2.7	15	−	9.0	16.9	1.0	20.5	ns
				50	−	11.5	20.4	1.0	24.0	
			3.3 ± 0.3	15	−	7.1	11.0	1.0	13.0	
				50	−	9.6	14.5	1.0	16.5	
Propagation Delay Time ($\overline{CLR}$−Q)	t_{pHL}		2.7	15	−	9.3	17.6	1.0	20.5	
				50	−	11.8	21.1	1.0	24.0	
			3.3 ± 0.3	15	−	7.3	11.5	1.0	13.5	
				50	−	9.8	15.0	1.0	17.0	
Maximum Clock Frequency	f_{MAX}		2.7	15	55	110	−	55	−	MHz
				50	45	60	−	40	−	
			3.3 ± 0.3	15	95	150	−	80	−	
				50	60	90	−	55	−	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	−	−	1.5	−	1.5	ns
			3.3 ± 0.3	50	−	−	1.5	−	1.5	
Input Capacitance	C_{IN}	(Note 2)			−	4	10	−	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			−	31	−	−	−	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

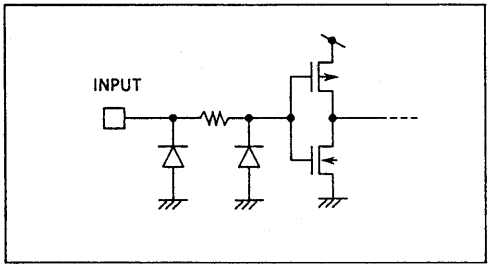
And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(total) = 22 + 9 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



TC74LVX373F/FW/FS

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74LVX373 is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.

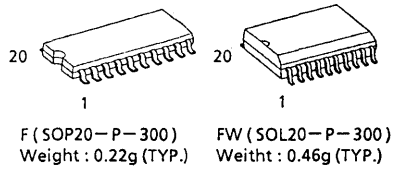
This 8-bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

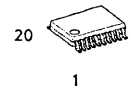
FEATURES:

- High Speed ..... t_{pd} = 5.8ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ... $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.8V(Max.)
- Pin and Function Compatible with 74HC373



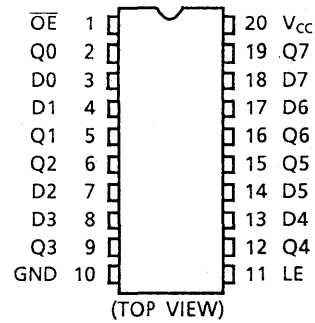
F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)



FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

PIN ASSIGNMENT



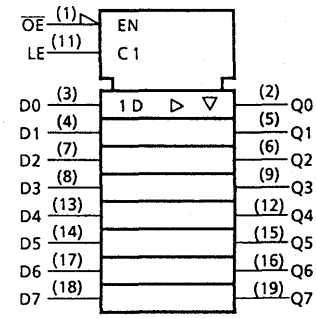
(TOP VIEW)

TRUTH TABLE

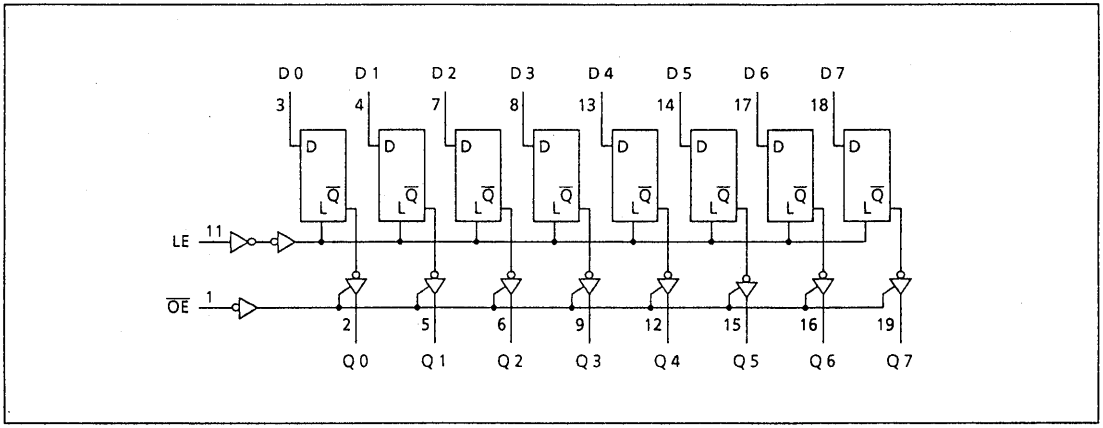
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
Qn : Q outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.25	—	±2.5	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION V_{CC} (V)	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$	2.7 3.3 ± 0.3	6.5 5.0	7.5 5.0	ns
Minimum Set - up Time	t_s	2.7 3.3 ± 0.3	6.0 4.0	6.0 4.0	
Minimum Hold Time	t_h	2.7 3.3 ± 0.3	1.0 1.0	1.0 1.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (LE − Q)	t_{pLH} t_{pHL}		2.7	15	—	7.5	14.5	1.0	17.5	ns
				50	—	10.0	18.0	1.0	21.0	
			3.3 ± 0.3	15	—	5.8	9.3	1.0	11.0	
				50	—	8.3	12.8	1.0	14.5	
Propagation Delay Time (D − Q)	t_{pLH} t_{pHL}		2.7	15	—	7.7	15.0	1.0	18.5	
				50	—	10.2	18.5	1.0	22.0	
			3.3 ± 0.3	15	—	6.0	9.7	1.0	11.5	
				50	—	8.5	13.2	1.0	15.0	
Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	2.7	15	—	7.7	15.0	1.0	18.5	
				50	—	10.2	18.5	1.0	22.0	
			3.3 ± 0.3	15	—	6.0	9.7	1.0	11.5	
				50	—	8.5	13.2	1.0	15.0	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	2.7	50	—	9.8	18.0	1.0	21.0	
			3.3 ± 0.3	50	—	8.2	12.8	1.0	14.5	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Output Capacitance	C_{OUT}				—	6	—	—	—	
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	27	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLH\,m} - t_{pLHn}|$, $t_{osHL} = |t_{pHL\,m} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per Latch)}$$

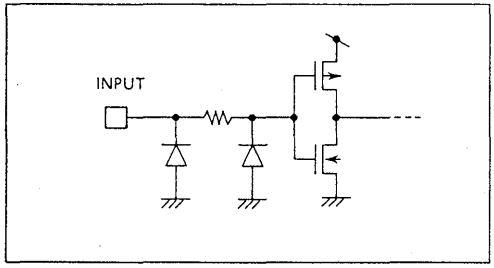
And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(total) = 14 + 13 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	−	0.8	V

INPUT EQUIVALENT CIRCUIT



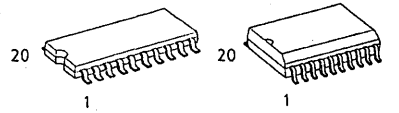
TC74LVX374F/FW/FS

OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUT

The TC74LVX374 is a high speed CMOS OCTAL D-FLIP FLOP fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
This 8-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input ($\overline{OE}$).
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

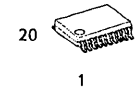
FEATURES:

- High Speed ..... f_{MAX} = 160MHz(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ··· $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.8V(Max.)
- Pin and Function Compatible with 74HC374



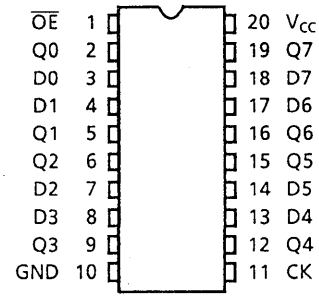
F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)



FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

PIN ASSIGNMENT



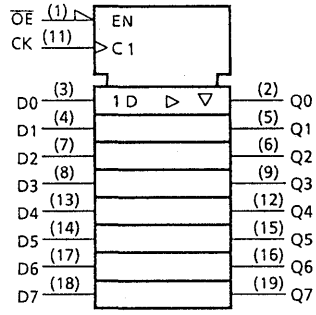
(TOP VIEW)

TRUTH TABLE

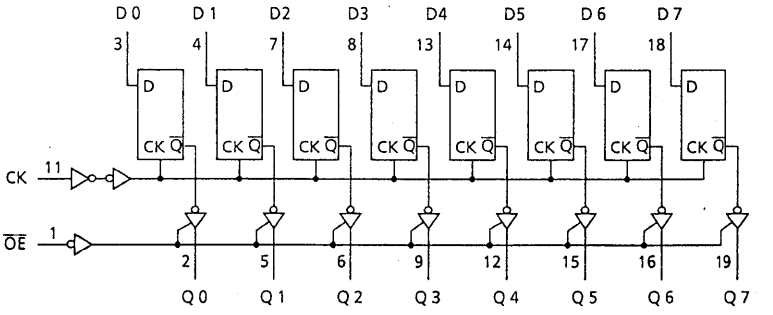
INPUTS			OUTPUTS
$\overline{OE}$	CK	D	
H	X	X	Z
L	↓	X	Q_n
L	↑	L	L
L	↑	H	H

X : Don't Care
Z : High Impedance
Q_n : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.25	—	±2.5	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C	Ta = −40~85°C	UNIT
		V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	2.7 3.3 ± 0.3	7.5 5.0	8.0 5.5	ns
Minimum Set - up Time	t_s	2.7 3.3 ± 0.3	6.5 4.5	6.5 4.5	
Minimum Hold Time	t_h	2.7 3.3 ± 0.3	2.0 2.0	2.0 2.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		2.7	15	—	8.5	16.3	1.0	19.5	ns
				50	—	11.0	19.8	1.0	23.0	
			3.3 ± 0.3	15	—	6.7	10.6	1.0	12.5	
				50	—	9.2	14.1	1.0	16.0	
Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	2.7	15	—	7.6	14.5	1.0	17.5	
				50	—	10.1	18.0	1.0	21.0	
			3.3 ± 0.3	15	—	5.9	9.3	1.0	11.0	
				50	—	8.4	12.8	1.0	14.5	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	2.7	50	—	11.5	18.5	1.0	22.0	
			3.3 ± 0.3	50	—	9.6	13.2	1.0	15.0	
Maximum Clock Frequency	f_{MAX}		2.7	15	60	115	—	50	—	MHz
				50	45	60	—	40	—	
			3.3 ± 0.3	15	100	160	—	85	—	
				50	60	95	—	55	—	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Output Capacitance	C_{OUT}				—	6	—	—	—	
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	32	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

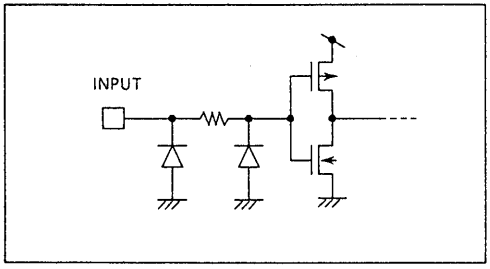
And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total) = 20 + 12 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	−	0.8	V

INPUT EQUIVALENT CIRCUIT



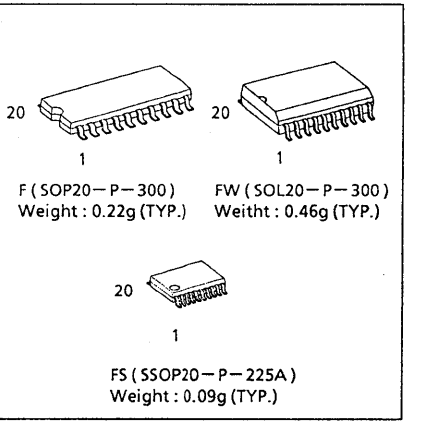
TC74LVX573F/FW/FS

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74LVX573 is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
This 8-bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

- High Speed ..... t_{pd} = 6.4ns(typ.) at V_{CC} = 3.3V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- Input Voltage Level ..... V_{IL} = 0.8V(Max.) at V_{CC} = 3V
  V_{IH} = 2.0V(Min.) at V_{CC} = 3V
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays··· $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.8V(Max.)
- Pin and Function Compatible with 74HC573

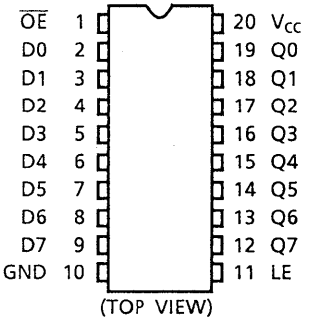


F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)

FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

PIN ASSIGNMENT

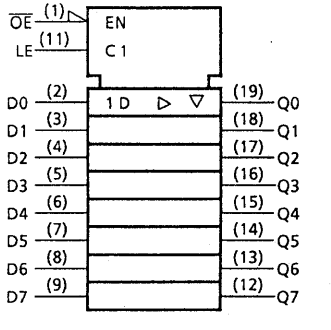


TRUTH TABLE

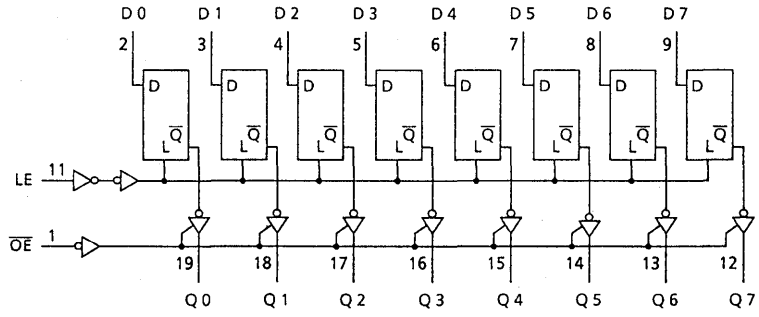
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
Qn : Q outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10sec	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0 3.0 3.6	1.5 2.0 2.4	— — —	— — —	1.5 2.0 2.4	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 3.0 3.6	— — —	— — —	0.5 0.8 0.8	— — —	0.5 0.8 0.8	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −50μA I_{OH} = −4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 —	— — —	1.9 2.9 2.48	— — —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0	— — —	0.0 0.0 —	0.1 0.1 0.36	— — —	0.1 0.1 0.44	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.25	—	±2.5	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	Ta = −40~85°C	UNIT
				LIMIT	LIMIT	
Minimum Pulse Width (LE)	$t_{W(H)}$		2.7 3.3 ± 0.3	6.5 5.0	7.5 5.0	ns
Minimum Set - up Time	t_s		2.7 3.3 ± 0.3	5.0 3.5	5.0 3.5	
Minimum Hold Time	t_h		2.7 3.3 ± 0.3	1.5 1.5	1.5 1.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (LE − Q)	t_{pLH} t_{pHL}		2.7	15	−	8.2	15.6	1.0	18.5	ns
				50	−	10.7	19.1	1.0	22.0	
			3.3 ± 0.3	15	−	6.4	10.1	1.0	12.0	
				50	−	8.9	13.6	1.0	15.5	
Propagation Delay Time (D − Q)	t_{pLH} t_{pHL}		2.7	15	−	7.6	14.5	1.0	17.5	
				50	−	10.1	18.0	1.0	21.0	
			3.3 ± 0.3	15	−	5.9	9.3	1.0	11.0	
				50	−	8.4	12.8	1.0	14.5	
Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	2.7	15	−	7.8	15.0	1.0	18.5	
				50	−	10.3	18.5	1.0	22.0	
			3.3 ± 0.3	15	−	6.1	9.7	1.0	12.0	
				50	−	8.6	13.2	1.0	15.5	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	2.7	50	−	12.1	19.1	1.0	22.0	
			3.3 ± 0.3	50	−	10.1	13.6	1.0	15.5	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	−	−	1.5	−	1.5	
			3.3 ± 0.3	50	−	−	1.5	−	1.5	
Input Capacitance	C_{IN}	(Note 2)			−	4	10	−	10	pF
Output Capacitance	C_{OUT}				−	6	−	−	−	
Power Dissipation Capacitance	C_{PD}	(Note 3)			−	29	−	−	−	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Latch)}$$

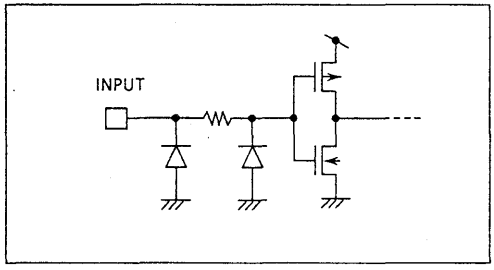
And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(total) = 21 + 8 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
		V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



10. NEW PRODUCT INFORMATION (1)

(DUAL SUPPLY OCTAL BUS TRANSCEIVER TC74LVX4245)

TC74LVX4245FS

(TENTATIVE)

DUAL SUPPLY OCTAL BUS TRANSCEIVER

The TC74LVX4245 is a dual supply , advanced high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 5V bus and a 3.3V bus in mixed 5V / 3.3V supply systems' it achieves high speed operation while maintaining the CMOS low power dissipation.

It is intended for 2 way asynchronous communication between data busses . The direction of data transmission is determined by the level of the DIR input.

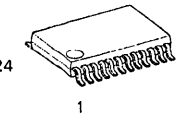
The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

The A - port interfaces with the 5V bus , the B - port with the 3.3V bus.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed ..... t_{pd} = 6.0ns (typ.) at $V_{CC}A$ = 5.0V / $V_{CC}B$ = 3.3V
- Low Power Dissipation ..... I_{CC} = 8μA (max.) at Ta = 25°C
- Symmetrical Output Impedance ..... I_{OUTA} = ±24mA (min.), I_{OUTB} = ±12mA (min.) at $V_{CC}A$ = 4.5V / $V_{CC}B$ = 3.0V
- Low Noise ..... V_{OLP} = 1.5V (max.)

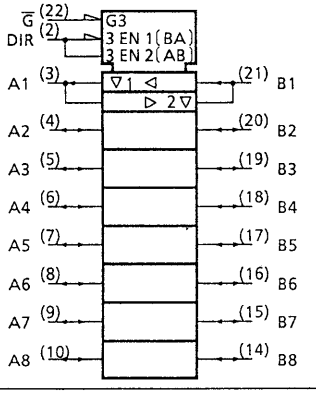


FS (SSOP24 - P - 300A)
Weight:0.14g (TYP.)

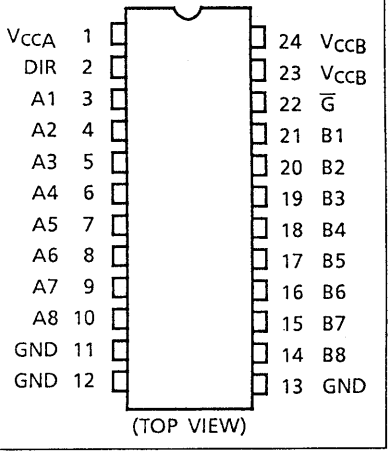
APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

IEC LOGIC SYMBOL



PIN ASSIGNMENT

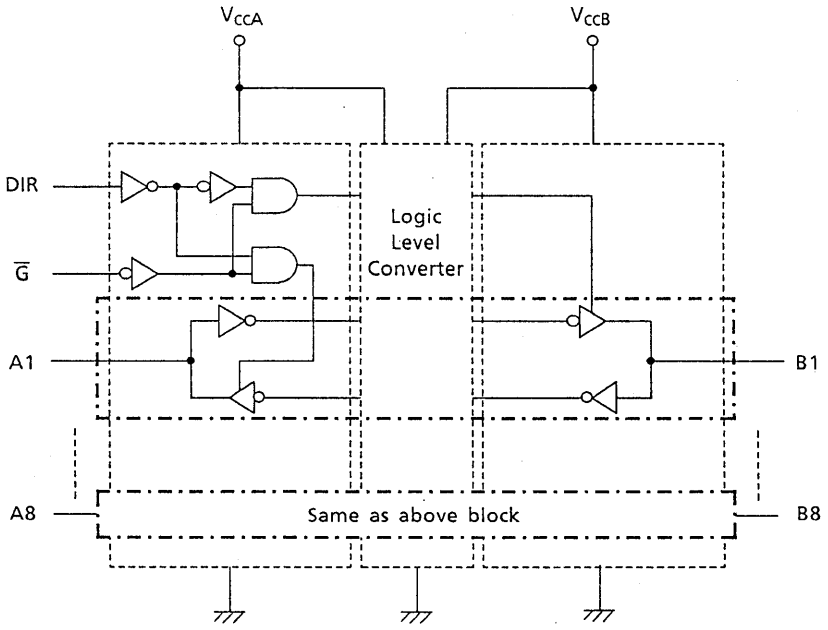


TRUTH TABLE

INPUTS		OUTPUTS	FUNCTION	
$\overline{G}$	DIR		A BUS	B BUS
L	L	A = B	OUTPUT	INPUT
L	H	B = A	INPUT	OUTPUT
H	X	Z	High Impedance	

X : Don't Care
Z : High Impedance

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CCA}	−0.5~7.0	V
	V_{CCB}	−0.5~7.0	
DC Input Voltage	V_{IN}	−0.5~V_{CCA} + 0.5	V
DC Bus I/O Voltage	$V_{I/OA}$	−0.5~V_{CCA} + 0.5	V
	$V_{I/OB}$	−0.5~V_{CCB} + 0.5	
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	$I_{I/OK}$	±50	
DC Output Current	I_{OUTA}	±50	mA
	I_{OUTB}	±50	
DC Vcc/Ground Current	I_{CCA}	±200	mA
	I_{CCB}	±100	
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature (10s)	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CCA}	4.5~5.5	V
	V_{CCB}	2.7~3.6	
Input Voltage	V_{IN}	0~V_{CCA}	V
Bus I/O Voltage	$V_{I/OA}$	0~V_{CCA}	V
	$V_{I/OB}$	0~V_{CCB}	
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dV	0~8 (V_{CCA} = 4.5~5.5V)	ns/V
		0~8 (V_{CCB} = 2.7~3.6V)	

DC ELECTRICAL CHARACTERISTICS (V_{CCA}) V_{CCB} = 2.7~3.6V

PARAMETER	SYMBOL	TEST CONDITION		V_{CCA} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IHA}	DIR, $\overline{G}$, An		4.5 ~ 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{ILA}	DIR, $\overline{G}$, An		4.5 ~ 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OHA}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OH} = −100μA I_{OH} = −24mA I_{OH} = −50mA*	4.5 4.5 5.5	4.4 3.86 —	4.5 — —	— — —	4.4 3.76 3.85	— — —	V
Low - Level Output Voltage	V_{OLA}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB}	I_{OL} = 100μA I_{OL} = 24mA I_{OL} = 50mA*	4.5 4.5 5.5	— — —	0.0 — —	0.1 0.36 —	— — —	0.1 0.44 1.65	V
3 - State Output Off - State Current	I_{OZA}	V_{INA} = V_{IHA} or V_{ILA} V_{INB} = V_{IHB} or V_{ILB} $V_{I/OA}$ = V_{CCA} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{INA}	V_{IN} (DIR, $\overline{G}$) = V_{CCA} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		5.5	—	—	8.0	—	80.0	μA
	I_{CCTA}	PER INPUT : V_{INA} = 3.4V OTHER INPUT : V_{CCA} or GND		5.5	—	—	2.3	—	2.5	mA

*: This specification indicates the capability of driving 75Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

DC ELECTRICAL CHARACTERISTICS (V_{CCB}) V_{CCA} = 4.5~5.5V

PARAMETER	SYMBOL	TEST CONDITION		V_{CCB} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IHB}	Bn		2.7 3.6	2.0 2.2	— —	— —	2.0 2.2	— —	V
Low - Level Input Voltage	V_{ILB}	Bn		2.7 3.6	— —	— —	0.8 0.8	— —	0.8 0.8	V
High - Level Output Voltage	V_{OHB}	V_{INA} = V_{IHA} or V_{ILA}	I_{OH} = −100μA I_{OH} = −8mA I_{OH} = −12mA	3.0 2.7 3.0	2.9 2.26 2.48	3.0 — —	— — —	2.9 2.20 2.40	— — —	V
Low - Level Output Voltage	V_{OLB}	V_{INA} = V_{IHA} or V_{ILA}	I_{OL} = 100μA I_{OL} = 8mA I_{OL} = 12mA	3.0 2.7 3.0	— — —	0.0 — —	0.1 0.31 0.31	— — —	0.1 0.40 0.40	V
3 - State Output Off - State Current	I_{OZB}	V_{INA} = V_{IHA} or V_{ILA} $V_{I/OB}$ = V_{CCB} or GND		3.6	—	—	±0.5	—	±5.0	μA
Quiescent Supply Current	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		3.6	—	—	5.0	—	50.0	μA
	I_{CCTB}	PER INPUT : V_{INB} = 3.0V OTHER INPUT : V_{CCB} or GND		3.6	—	—	0.35	—	0.50	mA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$, $V_{CCA} = 5.0 \pm 0.5V$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CCB} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (An ⇒ Bn)	t_{pLH} t_{pHL}	INPUT : An OUTPUT : Bn (DIR = "H")	2.7	−	7.1	9.5	1.0	10.5	ns
			3.3 ± 0.3	−	6.5	8.6	1.0	9.5	
3-State Output Enable Time ($\overline{G}$ ⇒ Bn)	t_{pZL} t_{pZH}		2.7	−	9.5	12.5	1.0	13.8	
			3.3 ± 0.3	−	8.6	11.4	1.0	12.5	
3-State Output Disable Time ($\overline{G}$ ⇒ Bn)	t_{pLZ} t_{pHZ}		2.7	−	5.3	9.1	1.0	10.0	
			3.3 ± 0.3	−	5.3	9.1	1.0	10.0	
Propagation Delay Time (Bn ⇒ An)	t_{pLH} t_{pHL}	INPUT : Bn OUTPUT : An (DIR = "L")	2.7	−	7.0	9.5	1.0	10.5	
			3.3 ± 0.3	−	6.4	8.6	1.0	9.5	
3-State Output Enable Time ($\overline{G}$ ⇒ An)	t_{pZL} t_{pZH}		2.7	−	8.5	11.6	1.0	12.7	
			3.3 ± 0.3	−	7.7	10.5	1.0	11.5	
3-State Output Disable Time ($\overline{G}$ ⇒ An)	t_{pLZ} t_{pHZ}		2.7	−	5.1	6.8	1.0	7.5	
			3.3 ± 0.3	−	5.1	6.8	1.0	7.5	
Output to Output Skew	t_{OSLH} t_{OSHL}	(Note 1)	2.7	−	−	1.5	−	1.5	
			3.3 ± 0.3	−	−	1.5	−	1.5	
Input Capacitance	C_{INA}	DIR, $\overline{G}$	3.3 ± 0.3	−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn	3.3 ± 0.3	−	13	−	−	−	
Power Dissipation Capacitance (Note 2)	C_{PDA}	A ⇒ B (DIR = "H")	3.3 ± 0.3	−	17	−	−	−	
		B ⇒ A (DIR = "L")	3.3 ± 0.3	−	25	−	−	−	
	C_{PDB}	A ⇒ B (DIR = "H")	3.3 ± 0.3	−	4	−	−	−	
		B ⇒ A (DIR = "L")	3.3 ± 0.3	−	4	−	−	−	

Note 1 Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Note 2 Cpd is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

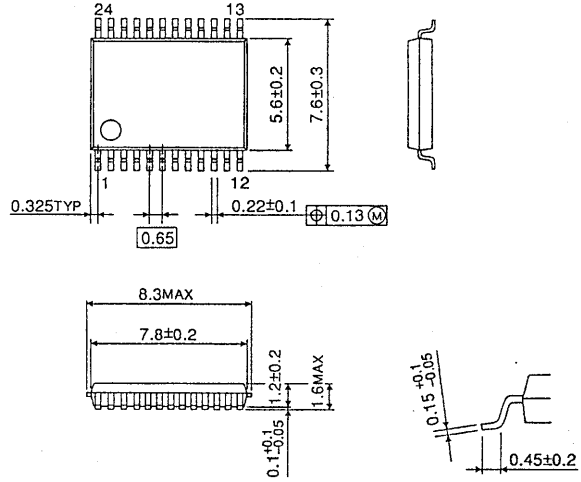
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C		UNIT
			V_{CCA}(V)	V_{CCB}(V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}(A)	$V_{OLP\,A}$	INPUT : Bn OUTPUT : An (DIR = "L")	5.0	3.3	1.0	1.5	V
Quiet Output Minimum Dynamic V_{OL}(A)	$V_{OLV\,A}$		5.0	3.3	−0.6	−1.2	V
Quiet Output Maximum Dynamic V_{OL}(B)	$V_{OLP\,B}$	INPUT : An OUTPUT : Bn (DIR = "H")	5.0	3.3	0.8	1.2	V
Quiet Output Minimum Dynamic V_{OL}(B)	$V_{OLV\,B}$		5.0	3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	$V_{IHD\,A}$	INPUT : An	5.0	3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	$V_{ILD\,A}$	INPUT : An	5.0	3.3	−	0.8	V
Minimum High Level Dynamic Input Voltage	$V_{IHD\,B}$	INPUT : Bn	5.0	3.3	−	2.0	V
Maximum Low Level Dynamic Input Voltage	$V_{ILD\,B}$	INPUT : Bn	5.0	3.3	−	0.8	V

SSOP 24PIN OUTLINE DRAWING (SSOP24 - P - 300A)

Unit: mm



Weight : 0.14g (TYP.)

11. NEW PRODUCT INFORMATION (2)

(TC74LCX Series Product Guide)

TC74LCX Series

LOW VOLTAGE HIGH SPEED BUS DRIVER SERIES WITH 5V TOLERANT INPUTS AND OUTPUTS

TC74LCX series has a propagation delay time of 4 ns. Operation is guaranteed between 2V and 3.6V. The 24mA output drive current also makes it suitable for systems requiring higher driving capabilities.
A great feature of this family is its ability to operate at pure 3V or at both 3V and 5V in the same design without sacrificing performance. In addition to this, a power down protected I/O structure makes it possible to apply the signal to any I/O terminal even in a power down mode.

(1) FEATURES

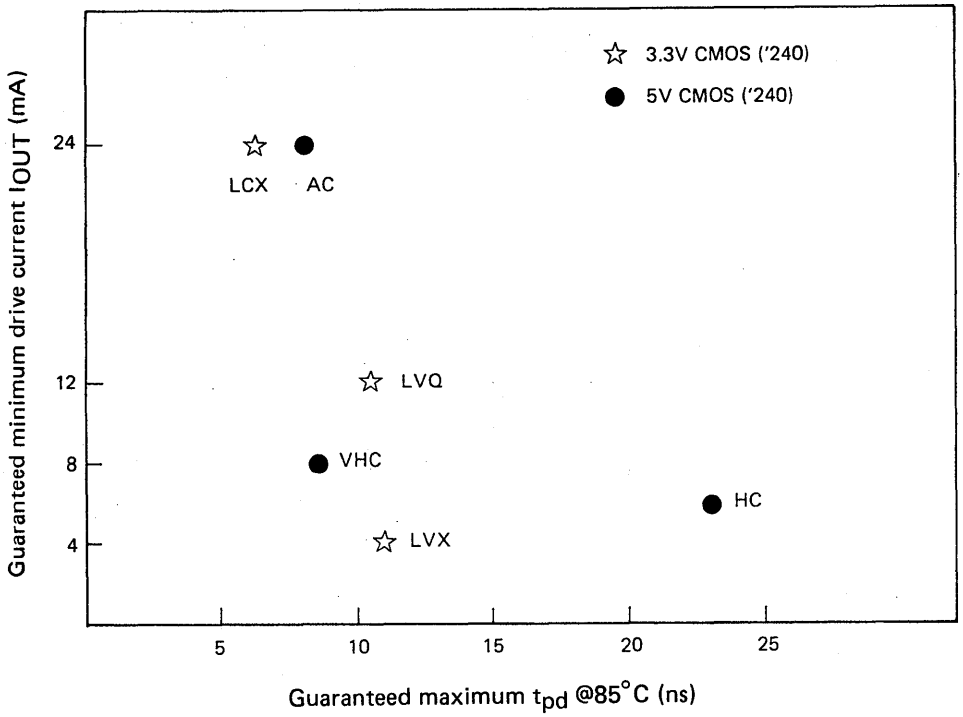
- ○ Low Voltage Operation .... V_{CC} = 2.0~3.6V
- ○ High Speed Operation ..... tpd = 6.5 ns Max. ('240 Type)
- ○ Output Current ..... I_{OH}/I_{OL} = ±24mA
- ○ Low Power Dissipation ..... I_{CC} = 10μA Max.
- ○ Latch-up Performance ..... ±300mA
- ○ ESD Performance ..... ±2000V (MIL-STD-883), ±200V (Machine Model)
- ○ Power Down Protection is provided all inputs and outputs.
- ○ Available in JEDEC SOP, EIAJ SOP and SSOP.
- ○ Pin and Function Compatible with the 74 series. (74AC/VHC/HC/F/ALS/LS etc.)

Comparison of Logic Family Characteristics

PARAMETER	SYMBOL	CMOS (3.3V Logic)			CMOS (5.0V Logic)			UNIT	Test Condition
		74LCX	74LVQ	74LVX	74AC	74VHC	74HC		
Propagation Delay Time ('240 Type)	tpd (Max.)	6.5	10.5	11	8	8.5	23.0	ns	(A), (B), (C)
Output Current	I_{OH} / I_{OL} (Min.)	± 24	± 12	± 4	± 24	± 8	± 4 (± 6)	mA	(A), (C)
Simultaneous Switching Noise ('240 Type)	V_{OLP} (Typ.)	0.8	0.5	0.3	1.2	0.7	0.5	V	(B)
Input Voltage	V_{IH} / V_{IL}	2.0 / 0.8			3.15 / 1.35			V	(A), (C)
Input Leakage Current	I_{IH} / I_{IL} (Max.)	± 1.0						μA	(C)
Quiescent Supply Current	I_{CC} (Max.)	10.0	40.0	40.0	80.0	40.0	40.0	μA	(C)
INPUT Power Down Protection		Yes	No	Yes	No	Yes	No	—	—
OUTPUT Power Down Protection		Yes	No	No	No	No	No	—	—

Test Condition : (A) Vcc = 3.0V (3.3V Logic), Vcc = 4.5V (5V Logic)
(B) C_L = 50pF
(C) Ta = –40~85°C

(a) High Speed Logic Positioning

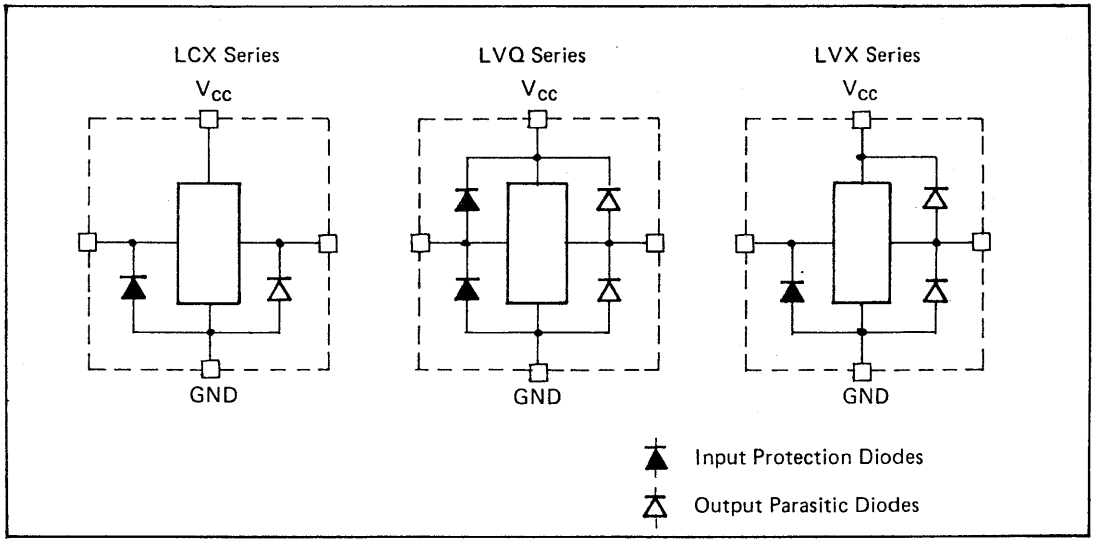


Features of each series

74LCX:	* ±24mA drive Bus application * Highest operating speed * 5V Tolerant Inputs & Outputs
74LVQ:	* ±12mA drive Gates, Flip Flops, MSIs, Octals * Low noise, high speed operation
74LVX:	* ±4mA drive Gates, Flip Flops, MSIs, Octals * Lowest noise, high speed (C_L < 50pF) * Best cost effective solution for Low Voltage random logic application * 5V tolerant Inputs

(b) I/O Equivalent Circuit & Interfacing

I/O Equivalent Circuit of each series



Applicable Voltage to I/O Terminals

	LCX	LVQ	LVX
Input Voltage Range			
(Operation)	0 ~ 5.5V	0 ~ Vcc	0 ~ 5.5V
(Power Down)	0 ~ 5.5V	0*	0 ~ 5.5V
Output Voltage Range			
(Output Enable)	0 ~ Vcc	0 ~ Vcc	0 ~ Vcc
(Output Disable)	0 ~ 5.5V	0 ~ Vcc	0 ~ Vcc
(Power Down)	0 ~ 5.5V	0*	0*

(*No signal is allowed.)

Interfacing Between 5V and 3V System

5V ⟶ 3V	3V ⟶ 5V	3V ⟷ 5V
(5V LOGIC) LVX LCX	(3V LOGIC) HCT VHCT ACT	LVX4245 LCX245

(2) TC74LCX Series TYPICAL ELECTRICAL CHARACTERISTICS

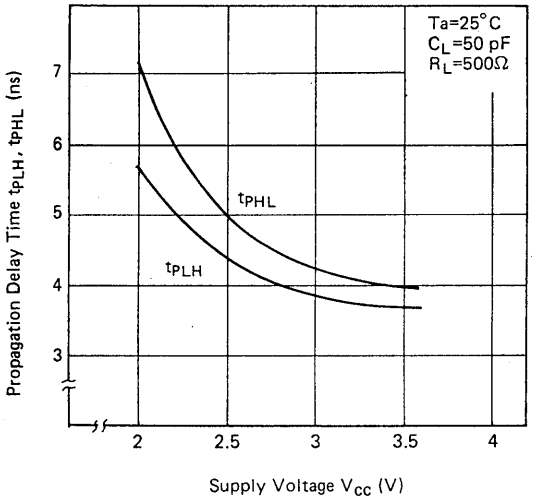


Fig. 12-1 Propagation Delay Time vs. Supply Voltage (LCX245)

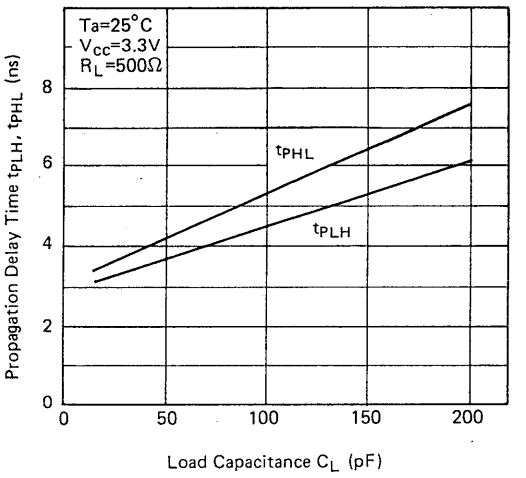


Fig. 12-2 Propagation Delay Time vs. Load Capacitance (LCX245)

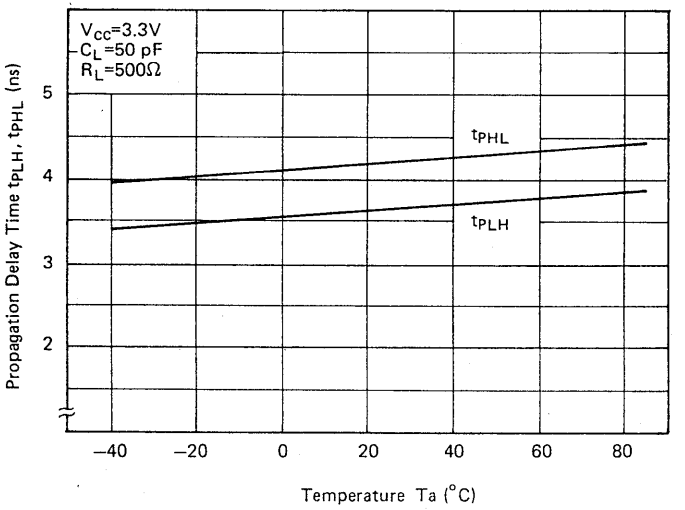


Fig. 12-3 Propagation Delay Time vs. Temperature (LCX245)

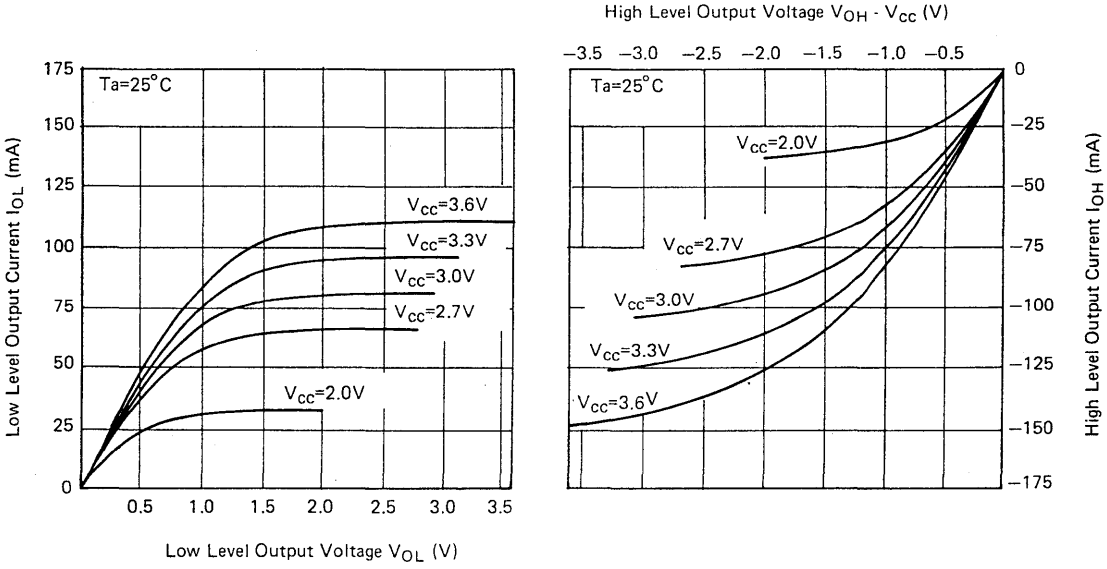


Fig. 12-4 Output Current Characteristics

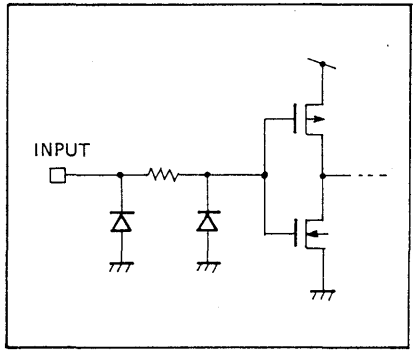


Fig. 12-5 Input Equivalent Circuit

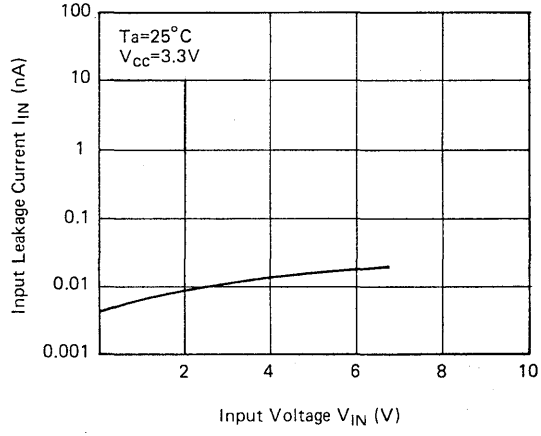


Fig. 12-6 Input Characteristics

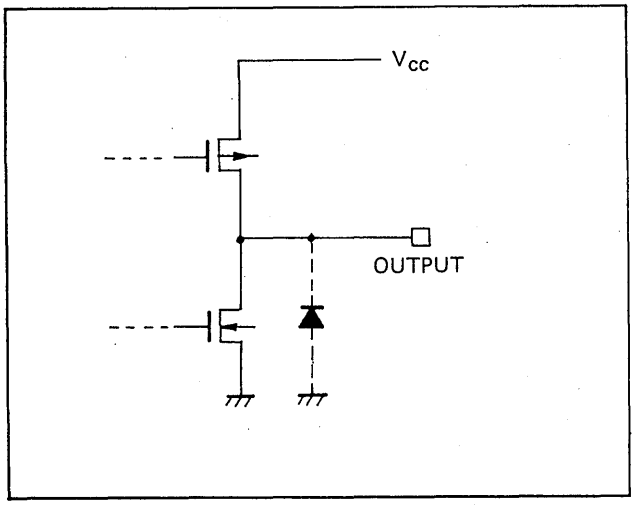


Fig. 12-7 Output Equivalent Circuit

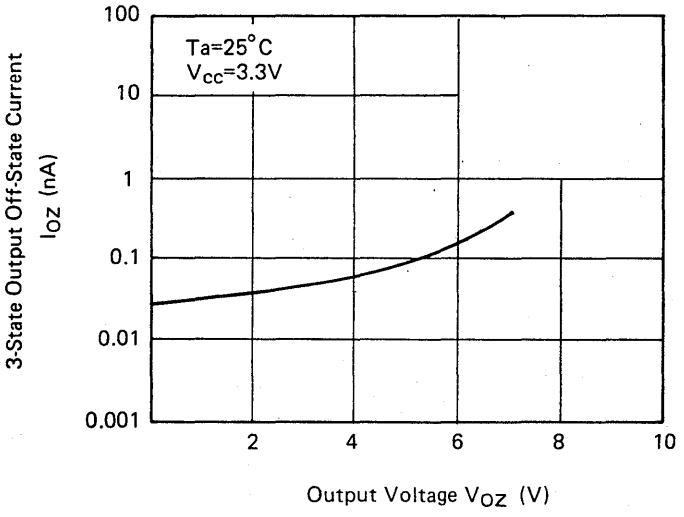


Fig. 12-8 Off-State (Output Disable) Output Characteristics

12. TC74LCX SERIES TECHNICAL DATA SHEETS

TYPE	FUNCTION	Pin	Page
TC74LCX 240F / FW / FS	OCTAL BUS BUFFER (3-STATE / INV.)	20	251
244F / FW / FS	OCTAL BUS BUFFER (3-STATE)	20	256
245F / FW / FS	OCTAL BUS TRANSCEIVER (3-STATE)	20	261
373F / FW / FS	OCTAL D-TYPE LATCH (3-STATE)	20	266
374F / FW / FS	OCTAL D-TYPE FLIP-FLOP (3-STATE)	20	271
TC74LCX 646FW	OCTAL BUS TRANSCEIVER / REGISTER (3-STATE)	24	276
652FW	OCTAL BUS TRANSCEIVER / REGISTER (3-STATE)	24	283

TC74LCX240F/FW/FS

(TENTATIVE)

LOW VOLTAGE OCTAL BUS BUFFER (INVERTED) WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX240 is a high parformance CMOS OCTAL BUS BUFFER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

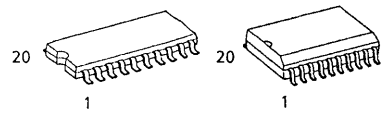
The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

The 74LCX240 is an inverting 3-state buffer having two active-low output enables. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.

FEATURES:

- Low Voltage Operation : V_{CC} = 2.0~3.6V
- High Speed Operation : t_{pd} = 6.5ns(max.) at V_{CC} = 3.0~3.6V
- Output Current : $|I_{OH}| / I_{OL}$ = 24mA(min.) at V_{CC} = 3.0V
- Latch-up Performance : ±300mA
- ESD Performance : ±2000V (Human Body Model)
  : ±200V (Machine Model)
- Available in JEDEC SOP, EIAJ SOP and SSOP
- Power Down Protection is provided on all inputs and outputs.
- Pin and Function Compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 240 type.



F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)

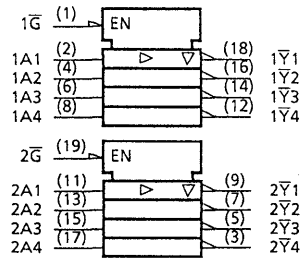
FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

TRUTH TABLE

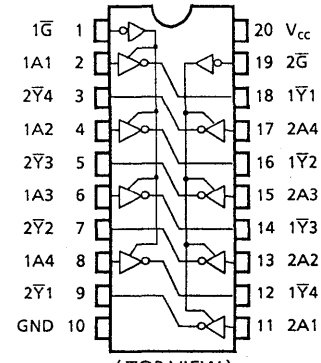
INPUTS		OUTPUTS
$\overline{G}$	A_n	
L	L	H
L	H	L
H	X	Z

X : Don't Care
Z : High Impedance

IEC LOGIC SYMBOL



PIN ASSIGNMENT



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE		UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0		V
DC Input Voltage	V_{IN}	−0.5~7.0		V
DC Output Voltage	V_{OUT}	−0.5~7.0 −0.5~V_{CC} + 0.5	(Off-State) (High or Low State)*	V
Input Diode Current	I_{IK}	−50		mA
Output Diode Current	I_{OK}	±50	(V_{OUT}<GND, V_{OUT}>V_{CC})	mA
DC Output Current	I_{OUT}	±50		mA
DC V_{CC}/Ground Current	I_{CC} / I_{GND}	±100		mA
Storage Temperature	T_{stg}	−65~150		°C

*: I_{OUT} absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE		UNIT
Supply Voltage	V_{CC}	2.0~3.6 1.5~3.6	(Operating) (Data Retention Only)	V
Input Voltage	V_{IN}	0~5.5		V
Output Voltage	V_{OUT}	0~5.5 0~V_{CC}	(Off-State) (High or Low State)	V
Output Current	I_{OH} / I_{OL}	±24 ±12	(Vcc = 3.0~3.6V) (Vcc = 2.7~3.0V)	mA
Operating Temperature	T_{opr}	−40~85		°C
Input Rise and Fall Time	dt/dV	0~10	(V_{IN} = 0.8~2V, V_{CC} = 3V)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = −40~85°C		UNIT
					MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.7~3.6	2.0	—	V
Low - Level Input Voltage	V_{IL}			2.7~3.6	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100μA	2.7~3.6	V_{CC} − 0.2	—	V
			I_{OH} = −12mA	2.7	2.2	—	
			I_{OH} = −18mA	3.0	2.4	—	
			I_{OH} = −24mA	3.0	2.2	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100μA	2.7~3.6	—	0.2	V
			I_{OL} = 12mA	2.7	—	0.4	
			I_{OL} = 24mA	3.0	—	0.55	
Input Leakage Current	I_{IN}	V_{IN} = 0~5.5V		2.7~3.6	—	±5.0	μA
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 0~5.5V		2.7~3.6	—	±5.0	μA
Power Off Leakage Current	I_{OFF}	V_{IN} / V_{OUT} = 5.5V (per Pin)		0	—	100	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	10.0	μA
		V_{IN} / V_{OUT} = 3.6~5.5V		2.7~3.6	—	±10.0	
Increase in I_{CC} per Input	ΔI_{CC}	V_{IH} = V_{CC} − 0.6V		2.7~3.6	—	500	μA

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}	(Fig. 1, 2)	7.5	1.5	6.5	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig. 1, 3)	9.0	1.5	8.0	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig. 1, 3)	8.0	1.5	7.0	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	—	—	1.0	ns

Note (1) Parameter guaranteed by design. ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

DYNAMIC SWITCHING CHARACTERISTICS (Input $t_r = t_f = 2.5$ns, $C_L = 50$pF, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	UNIT
				TYPICAL	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V

TBD : Actual performance will be noted upon completion of characterization.

CAPACITIVE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYPICAL	UNIT
Input Capacitance	C_{IN}		3.3	7	pF
Bus Input Capacitance	C_{OUT}		3.3	8	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10MHz (Note 1)	3.3	TBD	pF

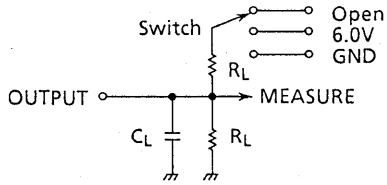
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

TBD : Actual performance will be noted upon completion of characterization.

TEST CIRCUIT

Fig . 1



C_L = 50pF
R_L = 500Ω

Parameter	Switch
tpLH, tpHL	Open
tpLZ, tpZL	6.0V
tpHZ, tpZH	GND

AC WAVEFORM

Fig. 2 (tpLH, tpHL)

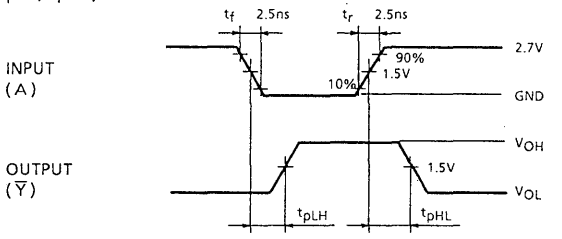
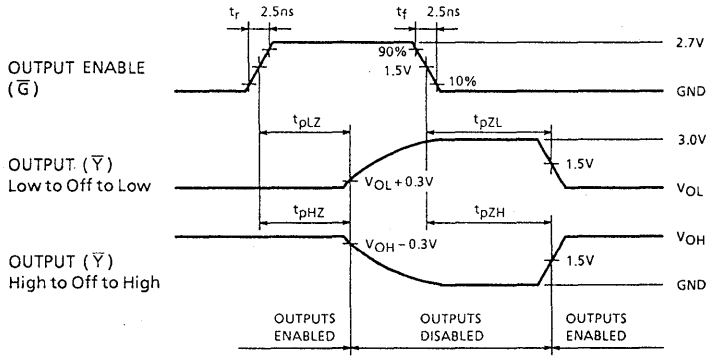


Fig. 3 (tpLZ, tpHZ, tpZL, tpZH)



TC74LCX244F/FW/FS

(TENTATIVE)

LOW VOLTAGE OCTAL BUS BUFFER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX244 is a high performance CMOS OCTAL BUS BUFFER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

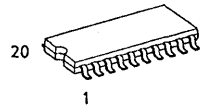
The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

The 74LCX244 is non-inverting 3-state buffer having two active-low output enable. This device is designed to be used with 3-state memory address drivers, etc.

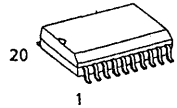
All inputs are equipped with protection circuits against static discharge.

FEATURES:

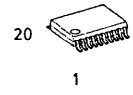
- Low Voltage Operation : V_{CC} = 2.0~3.6V
- High Speed Operation : t_{pd} = 6.5ns(max.) at V_{CC} = 3.0~3.6V
- Output Current : $|I_{OH}| / I_{OL}$ = 24mA(min.) at V_{CC} = 3.0V
- Latch-up Performance : ±300mA
- ESD Performance : ±2000V (Human Body Model)
  : ±200V (Machine Model)
- Available in JEDEC SOP, EIAJ SOP and SSOP
- Power Down Protection is provided on all inputs and outputs.
- Pin and Function Compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 244 type.



F (SOP20-P-300)
Weight : 0.22g (TYP.)



FW (SOL20-P-300)
Weitht : 0.46g (TYP.)



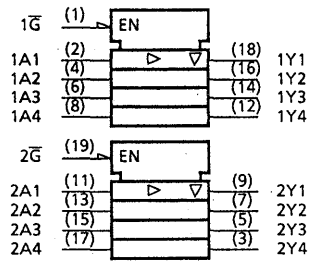
FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

TRUTH TABLE

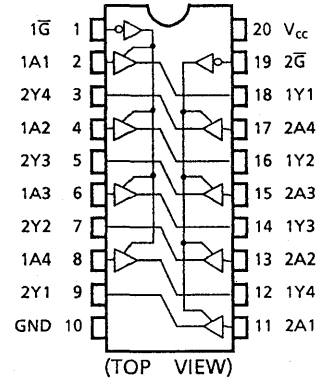
INPUTS		OUTPUTS
$\overline{G}$	A_n	
L	L	L
L	H	H
H	X	Z

X : Don't Care
Z : High Impedance

IEC LOGIC SYMBOL



PIN ASSIGNMENT



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0 (OFF-State) −0.5~V_{CC}+0.5 (High or Low State)*	V
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (V_{OUT}<GND, V_{OUT}>V_{CC})	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

*: I_{OUT} absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6 (Operating) 1.5~3.6 (Data Retention Only)	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (OFF-State) 0~V_{CC} (High or Low State)	V
Output Current	I_{OH}/I_{OL}	±24 (Vcc=3.0~3.6V) ±12 (Vcc=2.7~3.0V)	mA
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dV	0~10 (V_{IN}=0.8~2V, V_{CC}=3V)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = −40~85°C		UNIT
					MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.7~3.6	2.0	—	V
Low-Level Input Voltage	V_{IL}			2.7~3.6	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100μA	2.7~3.6	V_{CC} − 0.2	—	V
			I_{OH} = −12mA	2.7	2.2	—	
			I_{OH} = −18mA	3.0	2.4	—	
			I_{OH} = −24mA	3.0	2.2	—	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100μA	2.7~3.6	—	0.2	V
			I_{OL} = 12mA	2.7	—	0.4	
			I_{OL} = 24mA	3.0	—	0.55	
Input Leakage Current	I_{IN}	V_{IN} = 0~5.5V		2.7~3.6	—	±5.0	μA
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~5.5V		2.7~3.6	—	±5.0	μA
Power Off Leakage Current	I_{OFF}	V_{IN} / V_{OUT} = 5.5V (per Pin)		0	—	100	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	10.0	μA
		V_{IN} / V_{OUT} = 3.6~5.5V		2.7~3.6	—	±10.0	
Increase in I_{CC} per Input	ΔI_{CC}	V_{IH} = V_{CC} − 0.6V		2.7~3.6	—	500	μA

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}	(Fig. 1, 2)	7.5	1.5	6.5	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig. 1, 3)	9.0	1.5	8.0	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig. 1, 3)	8.0	1.5	7.0	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	—	—	1.0	ns

Note (1) Parameter guaranteed by design. ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

DYNAMIC SWITCHING CHARACTERISTICS (Input $t_r = t_f = 2.5$ns, $C_L = 50$pF, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	UNIT
				TYPICAL	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V

TBD : Actual performance will be noted upon completion of characterization.

CAPACITIVE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYPICAL	UNIT
Input Capacitance	C_{IN}		3.3	7	pF
Bus Input Capacitance	C_{OUT}		3.3	8	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10MHz (Note 1)	3.3	TBD	pF

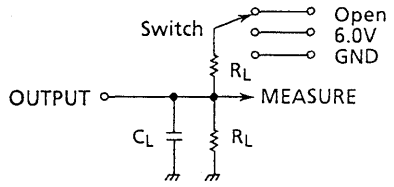
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

TBD : Actual performance will be noted upon completion of characterization.

TEST CIRCUIT

Fig . 1



C_L = 50pF
R_L = 500Ω

Parameter	Switch
tpLH, tpHL	Open
tpLZ, tpZL	6.0V
tpHZ, tpZH	GND

AC WAVEFORM

Fig. 2 (tpLH, tpHL)

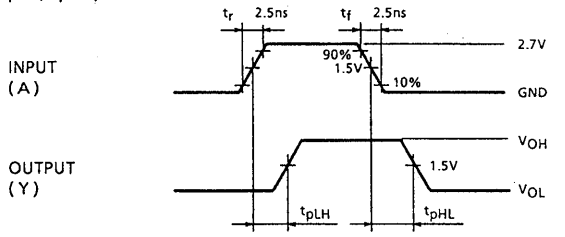
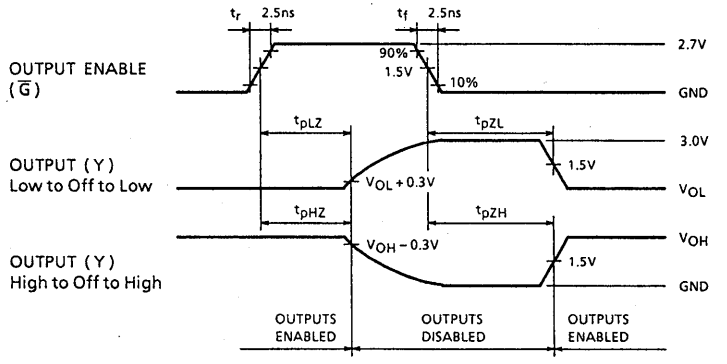


Fig. 3 (tpLZ, tpHZ, tpZL, tpZH)



TC74LCX245F/FW/FS

(TENTATIVE)

LOW VOLTAGE OCTAL BUS TRANSCEIVER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX245 is a high parformance CMOS OCTAL BUS TRANSCEIVER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

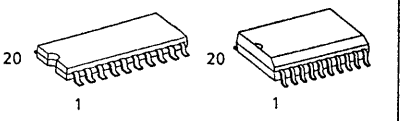
The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

The direction of data transmission is determined by the level of the DIR input. The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

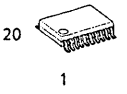
FEATURES :

- Low Voltage Operation : V_{CC} = 2.0~3.6V
- High Speed Operation : t_{pd} = 7.0ns(max.) at V_{CC} = 3.0~3.6V
- Output Current : $|I_{OH}| / I_{OL}$ = 24mA(min.) at V_{CC} = 3.0V
- Latch-up Performance : ±300mA
- ESD Performance : ±2000V (Human Body Model)
  : ±200V (Machine Model)
- Available in JEDEC SOP, EIAJ SOP and SSOP
- Bidirectional interface between 5V and 3.3V signals.
- Power Down Protection is provided on all inputs and outputs.
- Pin and Function Compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 245 type.



F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)

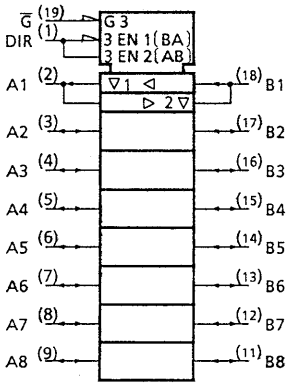


FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

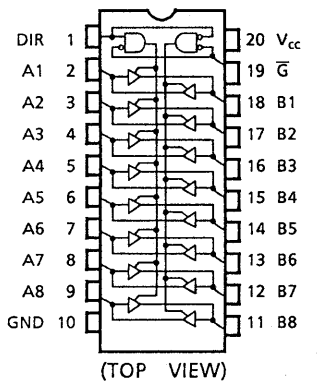
APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

IEC LOGIC SYMBOL



PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUT	FUNCTION	
$\overline{G}$	DIR		A BUS	B BUS
L	L	A = B	OUTPUT	INPUT
L	H	B = A	INPUT	OUTPUT
H	X	Z	High Impedance	

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE		UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0		V
DC Input Voltage (DIR, $\overline{G}$)	V_{IN}	−0.5~7.0		V
DC Bus I/O Voltage	$V_{I/O}$	−0.5~7.0 −0.5~V_{CC} + 0.5	(Off-State) (High or Low State)*	V
Input Diode Current	I_{IK}	−50		mA
Output Diode Current	I_{OK}	±50	(V_{OUT} < GND, V_{OUT} > V_{CC})	mA
DC Output Current	I_{OUT}	±50		mA
DC V_{CC}/Ground Current	I_{CC} / I_{GND}	±100		mA
Storage Temperature	T_{stg}	−65~150		°C

* : I_{OUT} absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE		UNIT
Supply Voltage	V_{CC}	2.0~3.6 1.5~3.6	(Operating) (Data Retention Only)	V
Input Voltage (DIR, $\overline{G}$)	V_{IN}	0~5.5		V
Bus I/O Voltage	$V_{I/O}$	0~5.5 0~V_{CC}	(Off-State) (High or Low State)	V
Output Current	I_{OH} / I_{OL}	±24 ±12	(V_{CC} = 3.0~3.6V) (V_{CC} = 2.7~3.0V)	mA
Operating Temperature	T_{opr}	−40~85		°C
Input Rise and Fall Time	dt/dV	0~10	(V_{IN} = 0.8~2V, V_{CC} = 3V)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = −40~85°C		UNIT
					MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.7~3.6	2.0	—	V
Low - Level Input Voltage	V_{IL}			2.7~3.6	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100μA	2.7~3.6	V_{CC} − 0.2	—	V
			I_{OH} = −12mA	2.7	2.2	—	
			I_{OH} = −18mA	3.0	2.4	—	
			I_{OH} = −24mA	3.0	2.2	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100μA	2.7~3.6	—	0.2	V
			I_{OL} = 12mA	2.7	—	0.4	
			I_{OL} = 24mA	3.0	—	0.55	
Input Leakage Current	I_{IN}	V_{IN} = 0~5.5V		2.7~3.6	—	±5.0	μA
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 0~5.5V		2.7~3.6	—	±5.0	μA
Power Off Leakage Current	I_{OFF}	V_{IN} / V_{OUT} = 5.5V (per Pin)		0	—	100	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	10.0	μA
		V_{IN} / V_{OUT} = 3.6~5.5V		2.7~3.6	—	±10.0	
Increase in I_{CC} per Input	ΔI_{CC}	V_{IH} = V_{CC} − 0.6V		2.7~3.6	—	500	μA

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}	(Fig. 1, 2)	8.0	1.5	7.0	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig. 1, 3)	9.5	1.5	8.5	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig. 1, 3)	8.5	1.5	7.5	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	—	—	1.0	ns

Note (1) Parameter guaranteed by design. ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

DYNAMIC SWITCHING CHARACTERISTICS (Input $t_r = t_f = 2.5$ns, $C_L = 50$pF, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	UNIT
				TYPICAL	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V

TBD : Actual performance will be noted upon completion of characterization.

CAPACITIVE CHARACTERISTICS

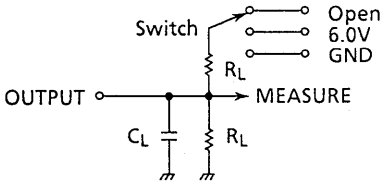
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYPICAL	UNIT
Input Capacitance	C_{IN}	DIR, $\overline{G}$	3.3	7	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn	3.3	8	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10MHz (Note 1)	3.3	20	pF

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

TEST CIRCUIT

Fig . 1



C_L = 50pF
R_L = 500Ω

Parameter	Switch
tpLH, tpHL	Open
tpLZ, tpZL	6.0V
tpHZ, tpZH	GND

AC WAVEFORM

Fig. 2 (tpLH, tpHL)

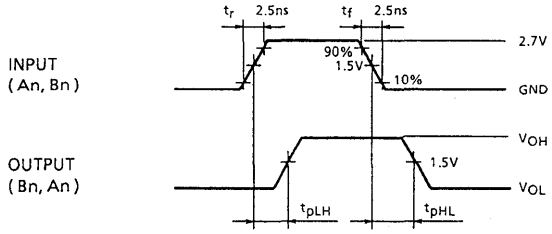
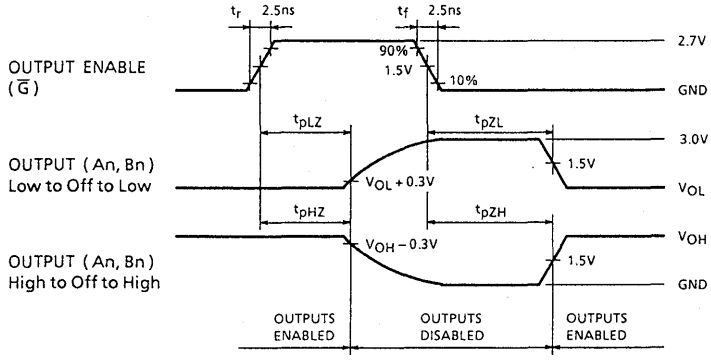


Fig. 3 (tpLZ, tpHZ, tpZL, tpZH)



TC74LCX373F/FW/FS

(TENTATIVE)

LOW VOLTAGE OCTAL D-TYPE LATCH WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX373 is a high parformance CMOS OCTAL D-TYPE LATCH. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

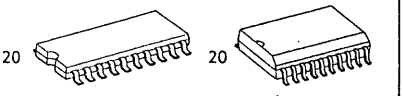
This 8-bit D-type latch is cintrolled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge.

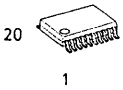
FEATURES:

- Low Voltage Operation : V_{CC} = 2.0~3.6V
- High Speed Operation : t_{pd} = 8.0ns(max.) at V_{CC} = 3.0~3.6V
- Output Current : $|I_{OH}| / I_{OL}$ = 24mA(min.) at V_{CC} = 3.0V
- Latch-up Performance : ±300mA
- ESD Performance : ±2000V (Human Body Model)
  : ±200V (Machine Model)
- Available in JEDEC SOP, EIAJ SOP and SSOP
- Power Down Protection is provided on all inputs. and outputs
- Pin and Function Compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 373 type.



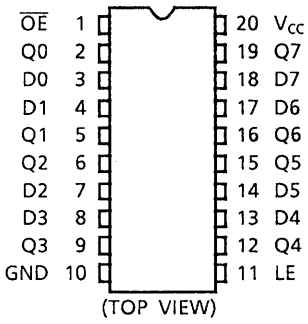
F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)



FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

PIN ASSIGNMENT

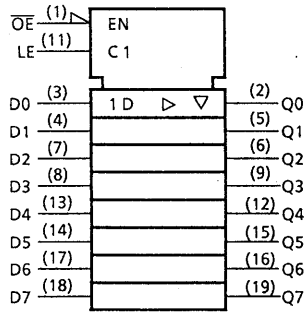


TRUTH TABLE

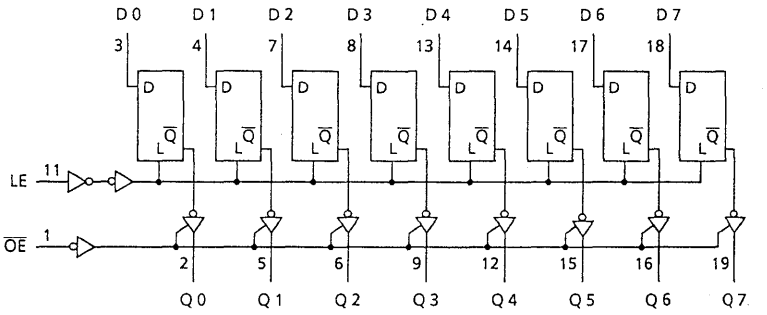
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0 (Off-State) −0.5~V_{CC}+0.5 (High or Low State)*	V
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (V_{OUT}<GND, V_{OUT}>V_{CC})	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

*: I_{OUT} absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6 (Operating) 1.5~3.6 (Data Retention Only)	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Off-State) 0~V_{CC} (High or Low State)	V
Output Current	I_{OH}/I_{OL}	±24 (V_{CC}=3.0~3.6V) ±12 (V_{CC}=2.7~3.0V)	mA
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dV	0~10 (V_{IN}=0.8~2V, V_{CC}=3V)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = −40~85°C		UNIT
					MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.7~3.6	2.0	−	V
Low-Level Input Voltage	V_{IL}			2.7~3.6	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100μA	2.7~3.6	V_{CC} − 0.2	−	V
			I_{OH} = −12mA	2.7	2.2	−	
			I_{OH} = −18mA	3.0	2.4	−	
			I_{OH} = −24mA	3.0	2.2	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100μA	2.7~3.6	−	0.2	V
			I_{OL} = 12mA	2.7	−	0.4	
			I_{OL} = 24mA	3.0	−	0.55	
Input Leakage Current	I_{IN}	V_{IN} = 0~5.5V		2.7~3.6	−	±5.0	μA
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~5.5V		2.7~3.6	−	±5.0	μA
Power Off Leakage Current	I_{OFF}	V_{IN} / V_{OUT} = 5.5V (per Pin)		0	−	100	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	−	10.0	μA
		V_{IN} / V_{OUT} = 3.6~5.5V		2.7~3.6	−	±10.0	
Increase in I_{CC} per Input	ΔI_{CC}	V_{IH} = V_{CC} − 0.6V		2.7~3.6	−	500	μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Minimum Pulse Width (LE)	$t_{W(H)}$	(Fig. 1, 2)	4.0	−	4.0	ns
Minimum Set-up Time	t_S	(Fig. 1, 2)	2.5	−	2.5	ns
Minimum Hold Time	t_h	(Fig. 1, 2)	1.5	−	1.5	ns

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Propagation Delay Time (D-Q)	t_{pLH} t_{pHL}	(Fig. 1, 2)	9.0	1.5	8.0	ns
Propagation Delay Time (LE-Q)	t_{pLH} t_{pHL}	(Fig. 1, 2)	9.5	1.5	8.5	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig. 1, 3)	9.5	1.5	8.5	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig. 1, 3)	8.5	1.5	7.5	ns
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	−	−	1.0	ns

Note (1) Parameter guaranteed by design. ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

DYNAMIC SWITCHING CHARACTERISTICS (Input $t_r = t_f = 2.5ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYPICAL	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	TBD	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	$V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	TBD	V

TBD : Actual performance will be noted upon completion of characterization.

CAPACITIVE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYPICAL	UNIT
Input Capacitance	C_{IN}		3.3	7	pF
Bus Input Capacitance	C_{OUT}		3.3	8	pF
Power Dissipation Capacitance	C_{PD}	$f_{IN} = 10MHz$ (Note 1)	3.3	TBD	pF

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per Latch)}$$

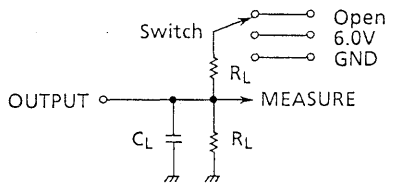
And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

$$C_{PD}(total) = \quad + \quad \cdot n$$

TBD : Actual performance will be noted upon completion of characterization.

TEST CIRCUIT

Fig . 1



$C_L = 50pF$
$R_L = 500\Omega$

Parameter	Switch
tpLH, tpHL	Open
tpLZ, tpZL	6.0V
tpHZ, tpZH	GND
tw, ts, th	Open

AC WAVEFORM

Fig . 2 (tpLH, tpHL, tw, ts, th)

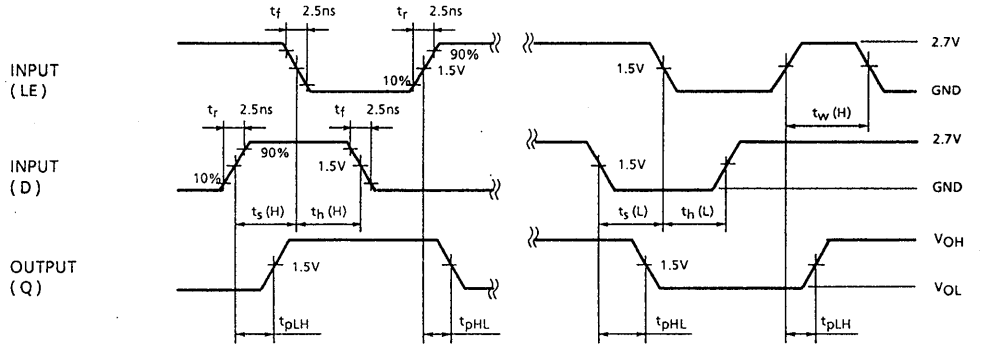
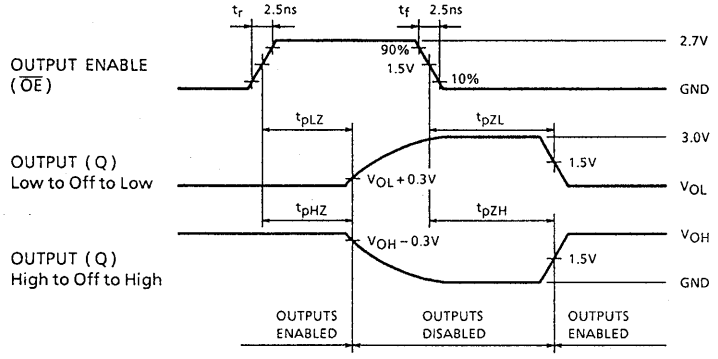


Fig. 3 (tpLZ, tpHZ, tpZL, tpZH)



TC74LCX374F/FW/FS

(TENTATIVE)

LOW VOLTAGE OCTAL D-TYPE FLIP FLOP WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX374 is a high performance CMOS OCTAL D-TYPE FLIP FLOP. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

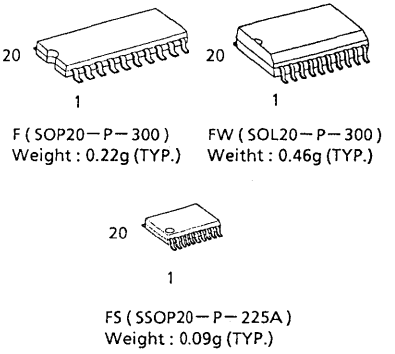
The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input ($\overline{OE}$). When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge.

FEATURES:

- Low Voltage Operation : V_{CC} = 2.0~3.6V
- High Speed Operation : t_{pd} = 8.5ns(max.) at V_{CC} = 3.0~3.6V
- Output Current : $|I_{OH}| / I_{OL}$ = 24mA(min.) at V_{CC} = 3.0V
- Latch-up Performance : ±300mA
- ESD Performance : ±2000V (Human Body Model)
  : ±200V (Machine Model)
- Available in JEDEC SOP, EIAJ SOP and SSOP
- Power Down Protection is provided on all inputs and outputs.
- Pin and Function Compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 374 type.

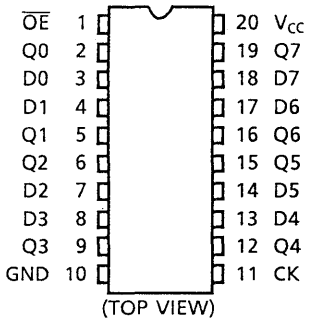


F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)

FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

PIN ASSIGNMENT



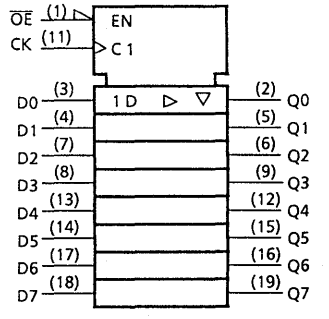
(TOP VIEW)

TRUTH TABLE

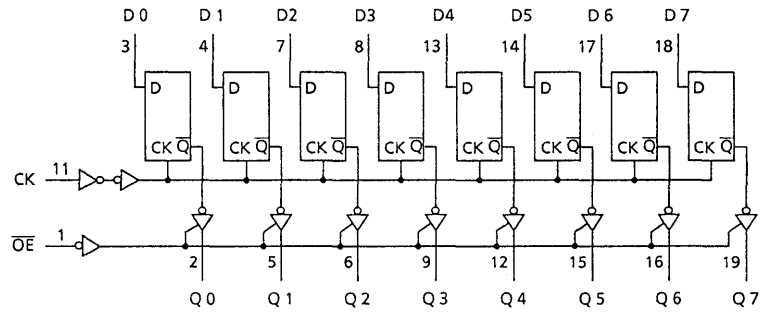
INPUTS			OUTPUTS
$\overline{OE}$	CK	D	
H	X	X	Z
L	↓	X	Q_n
L	↑	L	L
L	↑	H	H

X : Don't Care
Z : High Impedance
Q_n : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0 (Off-State) −0.5~V_{CC}+0.5 (High or Low State)*	V
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (V_{OUT}<GND, V_{OUT}>V_{CC})	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC} / I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

*: I_{OUT} absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6 (Operating) 1.5~3.6 (Data Retention Only)	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Off-State) 0~V_{CC} (High or Low State)	V
Output Current	I_{OH} / I_{OL}	±24 (V_{CC} = 3.0~3.6V) ±12 (V_{CC} = 2.7~3.0V)	mA
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~10 (V_{IN} = 0.8~2V, V_{CC} = 3V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = −40~85°C		UNIT
					MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.7~3.6	2.0	—	V
Low - Level Input Voltage	V_{IL}			2.7~3.6	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100μA	2.7~3.6	V_{CC} − 0.2	—	V
			I_{OH} = −12mA	2.7	2.2	—	
			I_{OH} = −18mA	3.0	2.4	—	
			I_{OH} = −24mA	3.0	2.2	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100μA	2.7~3.6	—	0.2	V
			I_{OL} = 12mA	2.7	—	0.4	
			I_{OL} = 24mA	3.0	—	0.55	
Input Leakage Current	I_{IN}	V_{IN} = 0~5.5V		2.7~3.6	—	±5.0	μA
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~5.5V		2.7~3.6	—	±5.0	μA
Power Off Leakage Current	I_{OFF}	V_{IN} / V_{OUT} = 5.5V (per Pin)		0	—	100	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	10.0	μA
		V_{IN} / V_{OUT} = 3.6~5.5V		2.7~3.6	—	±10.0	
Increase in I_{CC} per Input	ΔI_{CC}	V_{IH} = V_{CC} − 0.6V		2.7~3.6	—	500	μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$	(Fig. 2)	4.0	—	4.0	ns
Minimum Set − up Time	t_S	(Fig. 2)	2.5	—	2.5	ns
Minimum Hold Time	t_h	(Fig. 2)	1.5	—	1.5	ns

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Propagation Delay Time (CK − Q)	t_{pLH} t_{pHL}	(Fig. 1, 2)	9.5	1.5	8.5	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig. 1, 3)	9.5	1.5	8.5	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig. 1, 3)	8.5	1.5	7.5	ns
Maximum Clock Frequency	f_{MAX}		—	115	—	MHz
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	—	—	1.0	ns

Note (1) Parameter guaranteed by design. ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

DYNAMIC SWITCHING CHARACTERISTICS (Input $t_r = t_f = 2.5ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYPICAL	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	TBD	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	$V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	TBD	V

TBD : Actual performance will be noted upon completion of characterization.

CAPACITIVE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYPICAL	UNIT
Input Capacitance	C_{IN}		3.3	7	pF
Bus Input Capacitance	C_{OUT}		3.3	8	pF
Power Dissipation Capacitance	C_{PD}	$f_{IN} = 10MHz$ (Note 1)	3.3	TBD	pF

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per Latch)}$$

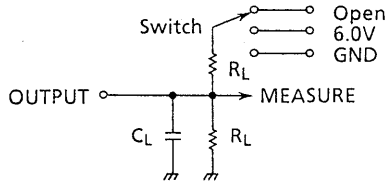
And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

$$C_{PD}(total) = \quad + \quad \cdot n$$

TBD : Actual performance will be noted upon completion of characterization.

TEST CIRCUIT

Fig . 1



$C_L = 50pF$
$R_L = 500\Omega$

Parameter	Switch
tpLH, tpHL	Open
tpLZ, tpZL	6.0V
tpHZ, tpZH	GND
tw, ts, th	Open

AC WAVEFORM

Fig . 2 (tpLH, tpHL, tw, ts, th)

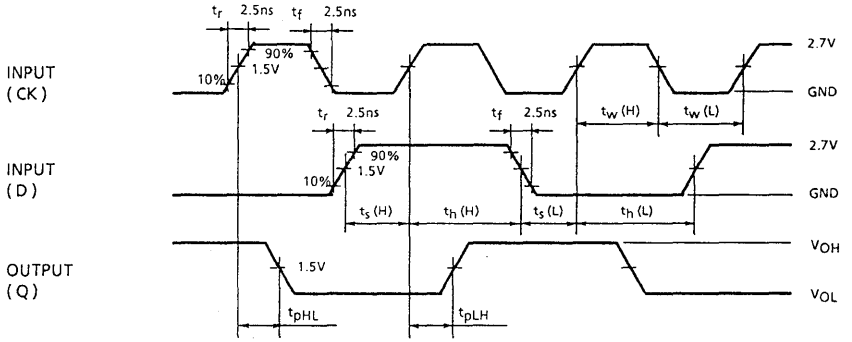
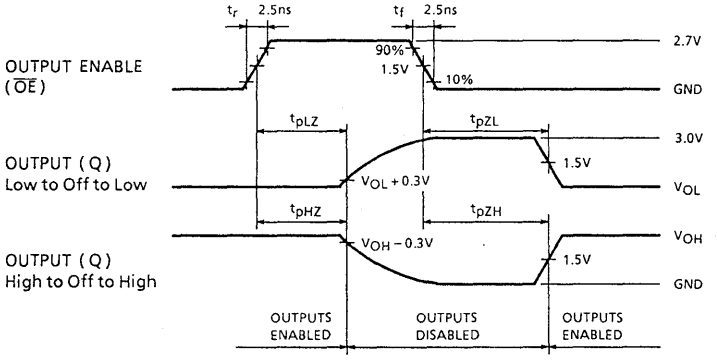


Fig. 3 (tpLZ, tpHZ, tpZL, tpZH)



TC74LCX646FW

(TENTATIVE)

LOW VOLTAGE OCTAL BUS TRANSCEIVER / REGISTER WITH 5V TOLERANT INPUTS AND OUTPUTS

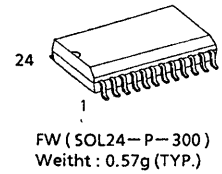
The TC74LCX646 is a high parformance CMOS OCTAL BUS TRANSCEIVER/REGISTER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. All inputs are equipped with protection circuits against static discharge.

FEATURES:

- Low Voltage Operation : V_{CC} = 2.0~3.6V
- High Speed Operation : t_{pd} = ns(max.) at V_{CC} = 3.0~3.6V
- Output Current : $|I_{OH}| / I_{OL}$ = 24mA(min.) at V_{CC} = 3.0V
- Latch-up Performance : ±300mA
- ESD Performance : ±2000V (Human Body Model)
  : ±200V (Machine Model)
- Available in JEDEC SOP
- Bidirectional interface between 5V and 3.3V signals.
- Power Down Protection is provided on all inputs and outputs.
- Pin and Function Compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 646 type.

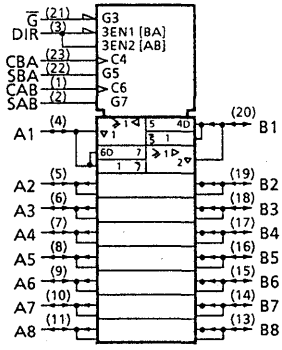


FW (SOL24-P-300)
Weitht : 0.57g (TYP.)

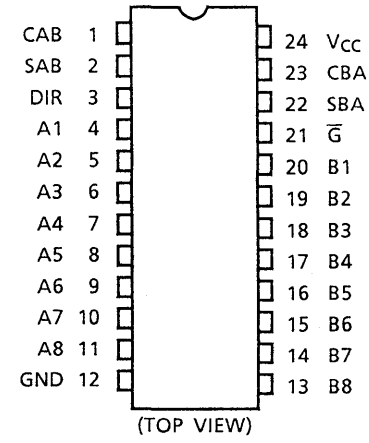
APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

IEC LOGIC SYMBOL



PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X*	X*	X	X	INPUTS Z	INPUTS Z	The output functions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus.
		↓	X*	L	X	L H	L H	The data on the A bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flop-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B Bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.

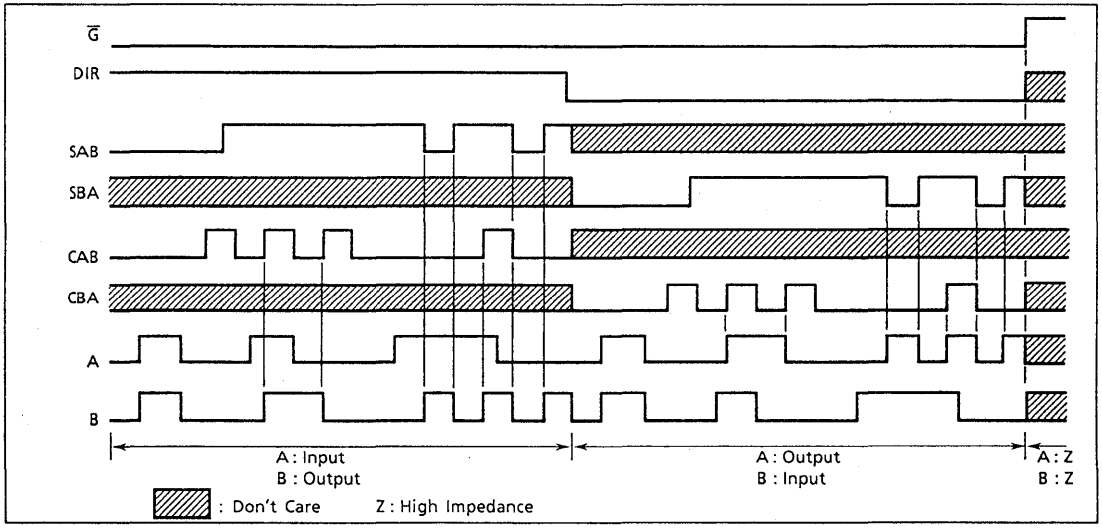
Notes: X: Don't Care

Qn: The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

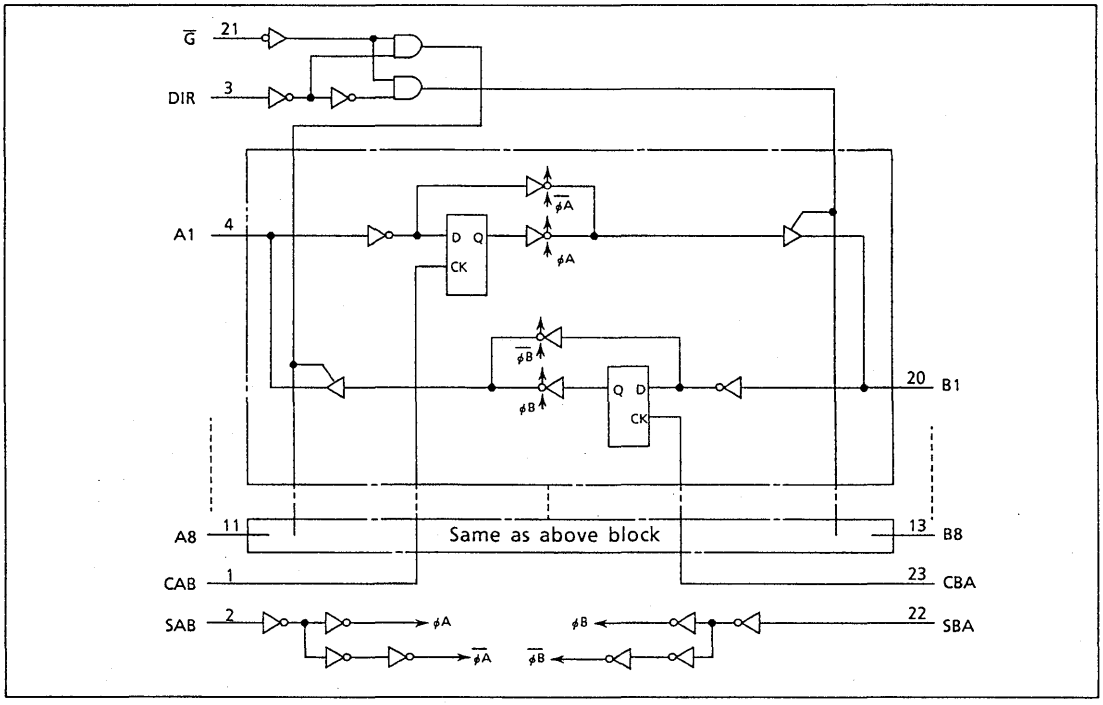
Z: High Impedance

*: The clocks are not internally gated with either $\overline{G}$ or DIR. Therefore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage (DIR, $\overline{G}$)	V_{IN}	−0.5~7.0	V
DC Bus I/O Voltage	$V_{I/O}$	−0.5~7.0 (Off-State) −0.5~V_{CC}+0.5 (High or Low State)*	V
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (V_{OUT}<GND, V_{OUT}>V_{CC})	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

* : I_{OUT} absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6 (Operating) 1.5~3.6 (Data Retention Only)	V
Input Voltage (DIR, $\overline{G}$)	V_{IN}	0~5.5	V
Bus I/O Voltage	$V_{I/O}$	0~5.5 (Off-State) 0~V_{CC} (High or Low State)	V
Output Current	I_{OH}/I_{OL}	±24 (Vcc=3.0~3.6) ±12 (Vcc=2.7~3.0)	mA
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dV	0~10 (V_{IN}=0.8~2V, V_{CC}=3V)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta=−40~85°C MIN.	Ta=−40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.7~3.6	2.0	—	V
Low-Level Input Voltage	V_{IL}			2.7~3.6	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−100μA	2.7~3.6	V_{CC}−0.2	—	V
			I_{OH}=−12mA	2.7	2.2	—	
			I_{OH}=−18mA	3.0	2.4	—	
			I_{OH}=−24mA	3.0	2.2	—	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=100μA	2.7~3.6	—	0.2	V
			I_{OL}=12mA	2.7	—	0.4	
			I_{OL}=24mA	3.0	—	0.55	
Input Leakage Current	I_{IN}	V_{IN}=0~5.5V		2.7~3.6	—	±5.0	μA
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=0~5.5V		2.7~3.6	—	±5.0	μA
Power Off Leakage Current	I_{OFF}	V_{IN}/V_{OUT}=5.5V (per Pin)		0	—	100	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		2.7~3.6	—	10.0	μA
		V_{IN}/V_{OUT}=3.6~5.5V		2.7~3.6	—	±10.0	
Increase in I_{CC} per Input	ΔI_{CC}	V_{IH}=V_{CC} − 0.6V		2.7~3.6	—	500	μA

TIMING REQUIRNENTS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Minimum Pulse Width	t_w (L) t_w (H)	(Fig. 1, 5)		−		ns
Minimum Set-up Time	t_s	(Fig. 1, 5)		−		ns
Minimum Hold Time	t_h	(Fig. 1, 5)		−		ns

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Propagation Delay Time (An, Bn − Bn, An)	t_{pLH} t_{pHL}	(Fig. 1, 2)		1.5		ns
Propagation Delay Time ($\overline{CAB}$, CBA − Bn, An)	t_{pLH} t_{pHL}	(Fig. 1, 5)		1.5		ns
Propagation Delay Time ($\overline{SAB}$, SBA − Bn, An)	t_{pLH} t_{pHL}	(Fig. 1, 2)		1.5		ns
3 − State output Enable Time ($\overline{G}$, DIR − An, Bn)	t_{pZL} t_{pZH}	(Fig. 1, 3, 4)		1.5		ns
3 − State output Disable Time ($\overline{G}$, DIR − An, Bn)	t_{pLZ} t_{pHZ}	(Fig. 1, 3, 4)		1.5		ns
Maximum Clock Frequency	f_{MAX}		−		−	MHz
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	−	−	1.0	ns

Note (1) Parameter guaranteed by design. ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

DYNAMIC SWITCHING CHARACTERISTICS (Input $t_r = t_f = 2.5$ns, $C_L = 50$pF, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	UNIT
				TYPICAL	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V

TBD : Actual performance will be noted upon completion of characterization.

CAPACITIVE CHARACTERISTICS

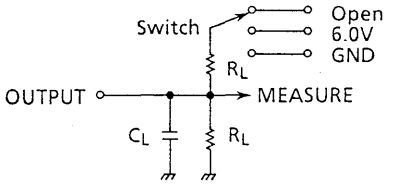
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYPICAL	UNIT
Input Capacitance	C_{IN}		3.3	7	pF
Bus Input Capacitance	$C_{I/O}$		3.3	8	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10MHz (Note 1)	3.3		pF

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

TEST CIRCUIT

Fig. 1



C_L = 50pF
R_L = 500Ω

Parameter	Switch
tpLH, tpHL	Open
tpLZ, tpZL	6.0V
tpHZ, tpZH	GND
tw, ts, th	Open

AC WAVEFORM

Fig. 2 (tpLH, tpHL)

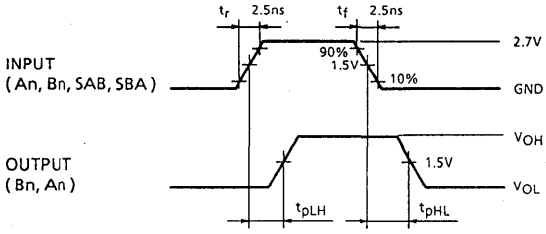


Fig. 3 (tpLZ, tpHZ, tpZL, tpZH)

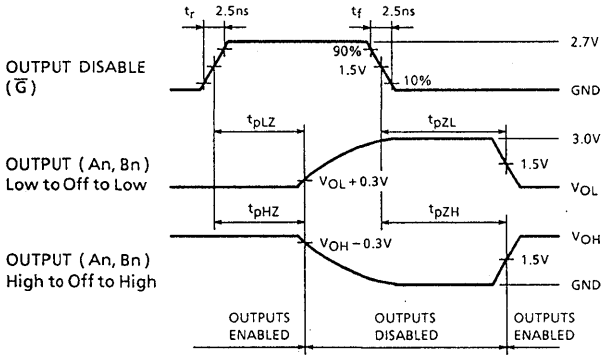


Fig. 4 (tpLZ, tpHZ, tpZL, tpZH)

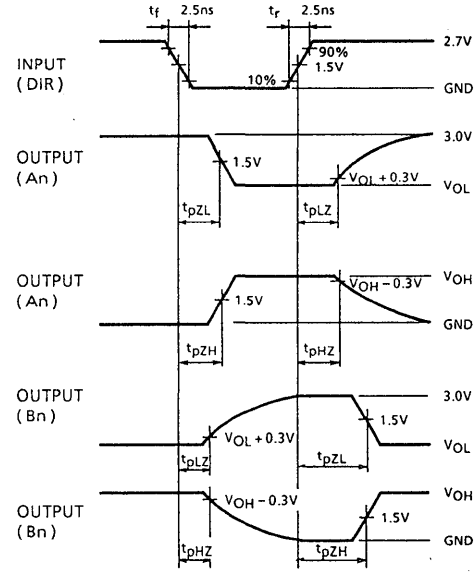
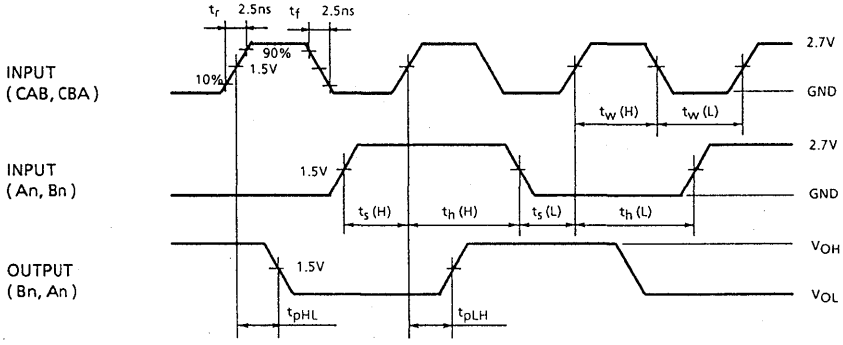


Fig. 5 (tpLH, tpHL, tw, ts, th)



TC74LCX652FW

(TENTATIVE)

LOW VOLTAGE OCTAL BUS TRANSCEIVER/REGISTER WITH 5V TOLERANT INPUTS AND OUTPUTS

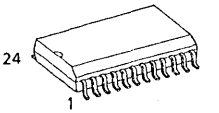
The TC74LCX652 is a high parformance CMOS OCTAL BUS TRANSCEIVER/REGISTER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. All inputs are equipped with protection circuits against static discharge.

FEATURES :

- Low Voltage Operation : V_{CC} = 2.0~3.6V
- High Speed Operation : t_{pd} = ns(max.) at V_{CC} = 3.0~3.6V
- Output Current : $|I_{OH}| / I_{OL}$ = 24mA(min.) at V_{CC} = 3.0V
- Latch-up Performance : ±300mA
- ESD Performance : ±2000V (Human Body Model)
  : ±200V (Machine Model)
- Available in JEDEC SOP
- Bidirectional interface between 5V and 3.3V signals.
- Power Down Protection is provided on all inputs and outputs.
- Pin and Function Compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 652 type.

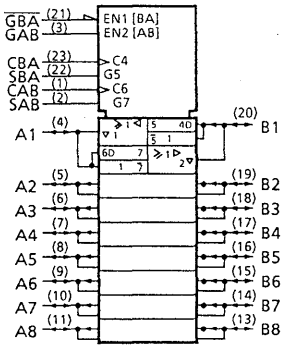


FW (SOL24-P-300)
Weitht : 0.57g (TYP.)

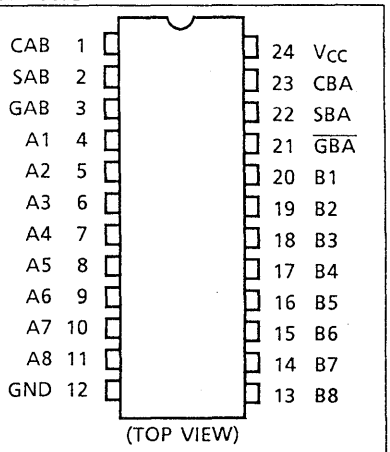
APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

IEC LOGIC SYMBOL



PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H	X*	X*	X	X	INPUTS Z	INPUTS Z	The output functions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
H	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus.
		↓	X*	L	X	L H	L H	The data on the A bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flop-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B Bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
H	L	X*	X*	H	H	OUTPUTS Qn	OUTPUTS Qn	The data in the A storage flop-flops are displayed on the B Bus, and the data in the B storage flop-flops are displayed on the A.

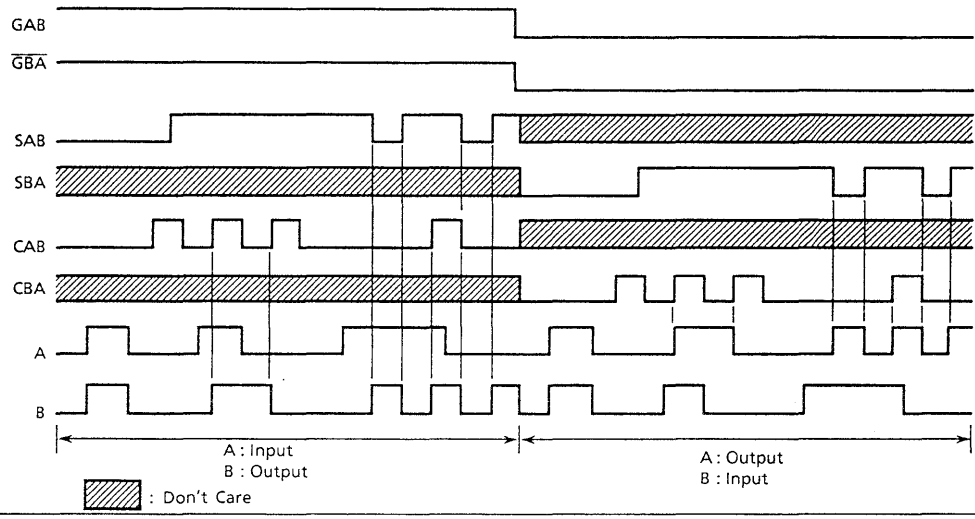
Notes: X: Don't Care

Qn: The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

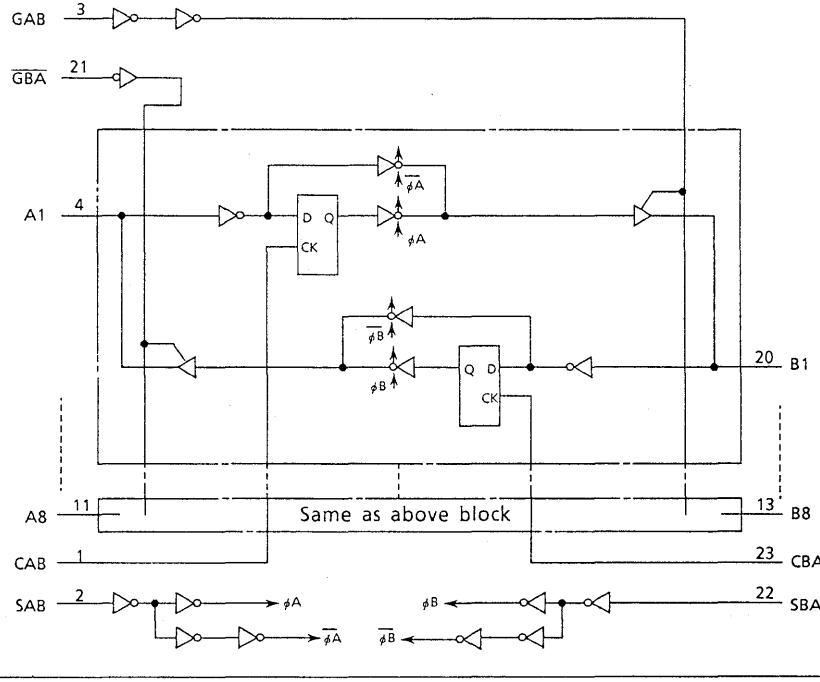
Z: High Impedance

*: The clocks are not internally gated with either GAB or $\overline{GBA}$. Therefore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage (DIR, $\overline{G}$)	V_{IN}	−0.5~7.0	V
DC Bus I/O Voltage	$V_{I/O}$	−0.5~7.0 (Off-State) −0.5~V_{CC}+0.5 (High or Low State)*	V
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (V_{OUT}<GND, V_{OUT}>V_{CC})	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC} / I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

* : I_{OUT} absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6 (Operating) 1.5~3.6 (Data Retention Only)	V
Input Voltage (DIR, $\overline{G}$)	V_{IN}	0~5.5	V
Bus I/O Voltage	$V_{I/O}$	0~5.5 (Off-State) 0~V_{CC} (High or Low State)	V
Output Current	I_{OH} / I_{OL}	±24 (Vcc = 3.0~3.6) ±12 (Vcc = 2.7~3.0)	mA
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dV	0~10 (V_{IN} = 0.8~2V, V_{CC} = 3V)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = −40~85°C		UNIT
					MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.7~3.6	2.0	−	V
Low-Level Input Voltage	V_{IL}			2.7~3.6	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100μA	2.7~3.6	V_{CC}−0.2	−	V
			I_{OH} = −12mA	2.7	2.2	−	
			I_{OH} = −18mA	3.0	2.4	−	
			I_{OH} = −24mA	3.0	2.2	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100μA	2.7~3.6	−	0.2	V
			I_{OL} = 12mA	2.7	−	0.4	
			I_{OL} = 24mA	3.0	−	0.55	
Input Leakage Current	I_{IN}	V_{IN} = 0~5.5V		2.7~3.6	−	±5.0	μA
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~5.5V		2.7~3.6	−	±5.0	μA
Power Off Leakage Current	I_{OFF}	V_{IN} / V_{OUT} = 5.5V (per Pin)		0	−	100	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	−	10.0	μA
		V_{IN} / V_{OUT} = 3.6~5.5V		2.7~3.6	−	±10.0	
Increase in I_{CC} per Input	ΔI_{CC}	V_{IH} = V_{CC} − 0.6V		2.7~3.6	−	500	μA

TIMING REQUIRNENTS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Minimum Pulse Width	t_w (L) t_w (H)	(Fig. 1, 5)		−		ns
Minimum Set-up Time	t_s	(Fig. 1, 5)		−		ns
Minimum Hold Time	t_h	(Fig. 1, 5)		−		ns

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Propagation Delay Time (An, Bn – Bn, An)	t_{pLH} t_{pHL}	(Fig. 1, 2)		1.5		ns
Propagation Delay Time (CAB, CBA – Bn, An)	t_{pLH} t_{pHL}	(Fig. 1, 5)		1.5		ns
Propagation Delay Time (SAB, SBA – Bn, An)	t_{pLH} t_{pHL}	(Fig. 1, 2)		1.5		ns
3 – State output Enable Time (GAB, $\overline{GBA}$ – Bn, An)	t_{pZL} t_{pZH}	(Fig. 1, 3, 4)		1.5		ns
3 – State output Disable Time (GAB, $\overline{GBA}$ – Bn, An)	t_{pLZ} t_{pHZ}	(Fig. 1, 3, 4)		1.5		ns
Maximum Clock Frequency	f_{MAX}		−		−	MHz
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	−	−	1.0	ns

Note (1) Parameter guaranteed by design. ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

DYNAMIC SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 2.5ns, C_L = 50pF, R_L = 500Ω)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	UNIT
				TYPICAL	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V

TBD : Actual performance will be noted upon completion of characterization.

CAPACITIVE CHARACTERISTICS

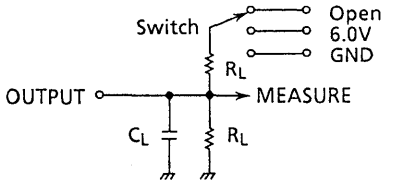
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYPICAL	UNIT
Input Capacitance	C_{IN}		3.3	7	pF
Bus Input Capacitance	$C_{I/O}$		3.3	8	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10MHz (Note 1)	3.3		pF

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

TEST CIRCUIT

Fig . 1



C_L = 50pF
R_L = 500Ω

Parameter	Switch
tpLH, tpHL	Open
tpLZ, tpZL	6.0V
tpHZ, tpZH	GND
tw, ts, th	Open

AC WAVEFORM

Fig. 2 (tpLH, tpHL)

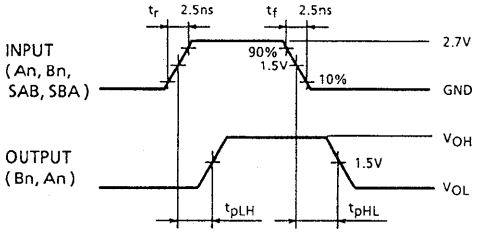


Fig. 3 (tpLZ, tpHZ, tpZL, tpZH)

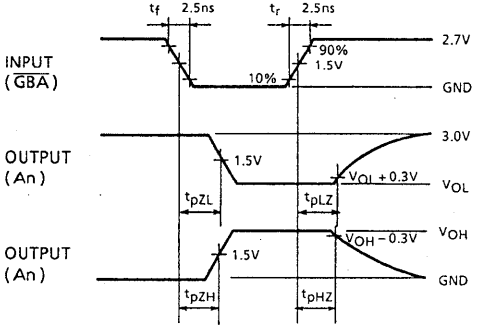


Fig. 4 (tpLZ, tpHZ, tpZL, tpZH)

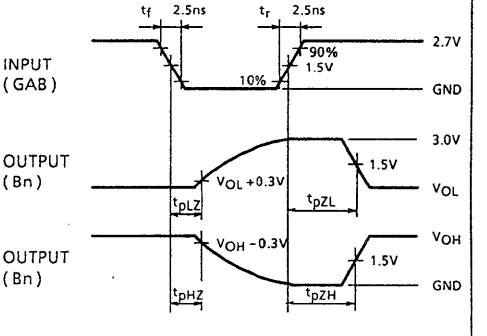
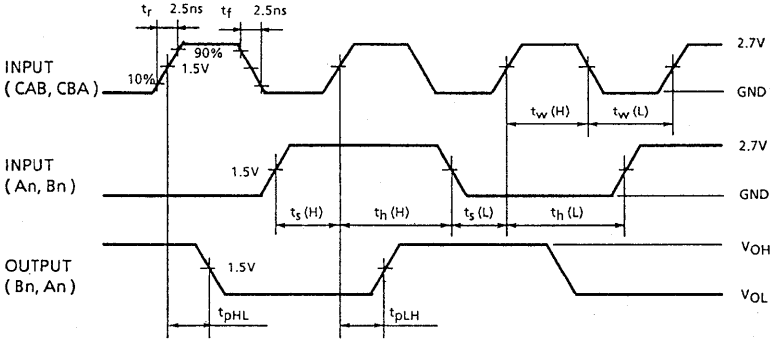


Fig. 5 (tpLH, tpHL, tw, ts, th)



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