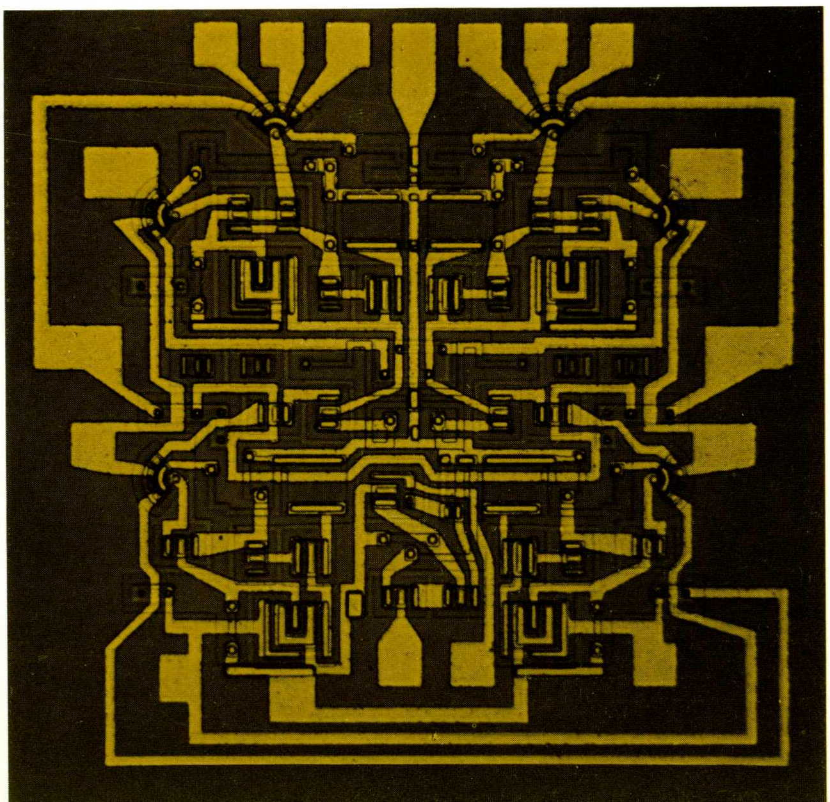
7/66

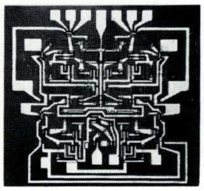
HLTTL

Transitron

electronic corporation Wakefield, Massachusetts



Wherever there's HLTTL . . . there's Transitron

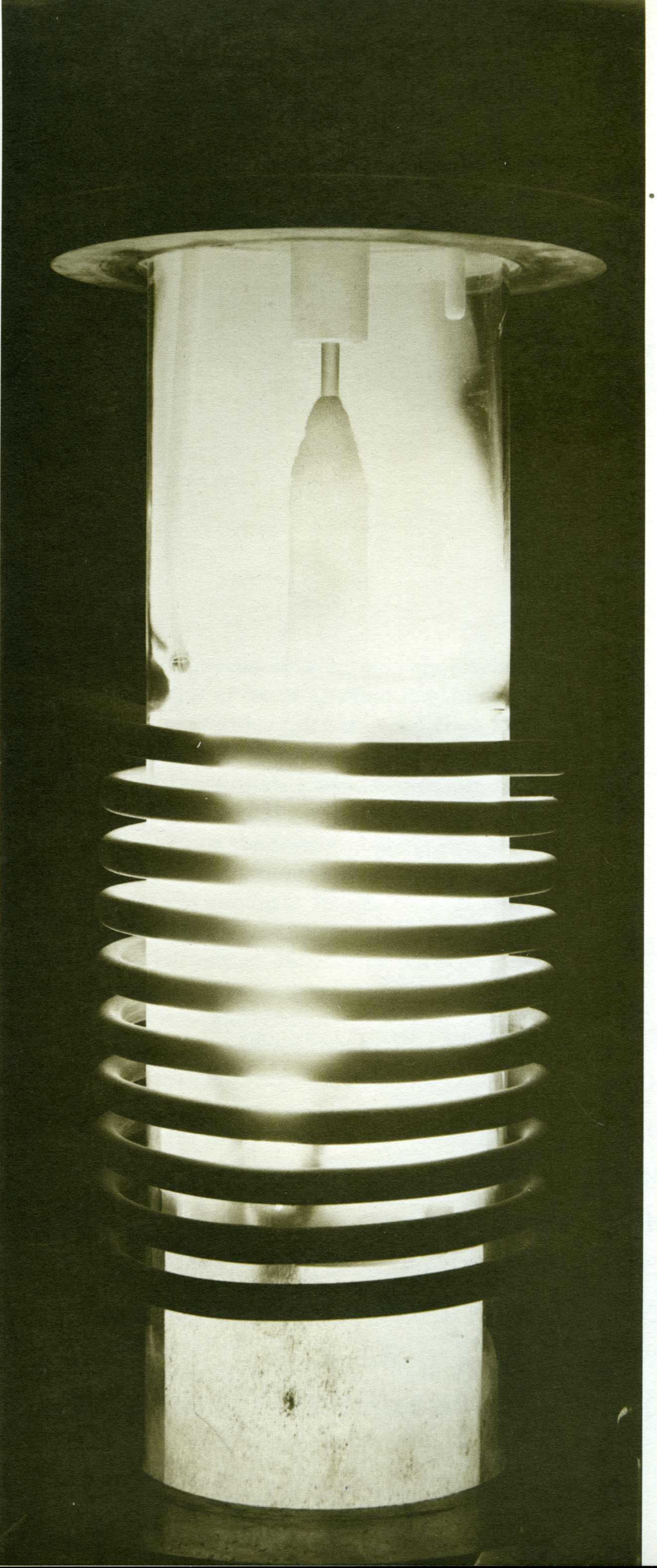


The Transitron philosophy in integrated circuits has resulted in the concentration of its production capability first on a family of digital monolithic circuits called High Level Transistor Transistor Logic (HLTTL). There is, of course, intention to manufacture linear integrated circuits and perhaps even other families of digital circuits in the near future. However, it is believed that the family of integrated circuits with the greatest appeal to circuit and system designers today and for the systems producer for the next several years is without question HLTTL. Therefore, the past year has been devoted almost entirely to the establishment of good manufacturing capability of such circuits. Transitron's concentration of effort on this family has resulted in an unprecedented number of different circuit functions and gates for the application of logic system designers; a strong improvement in the propagation delay, the radiation resistance and the output characteristic of the circuits; a new master slave flip-flop for single phase application; a willingness to do custom work within the basic HLTTL circuit concept for new functions; a similar willingness to alternate source other manufacturers' HLTTL functions and pin configurations; and finally a low cost set of HLTTL circuits for commercial application. All of this is detailed in the succeeding pages of this brochure. It has been our intent to make evident, by performance, the slogan, "Wherever There's HLTTL . . . There's Transitron." The industry response to this philosophy has been gratifying.

Contents

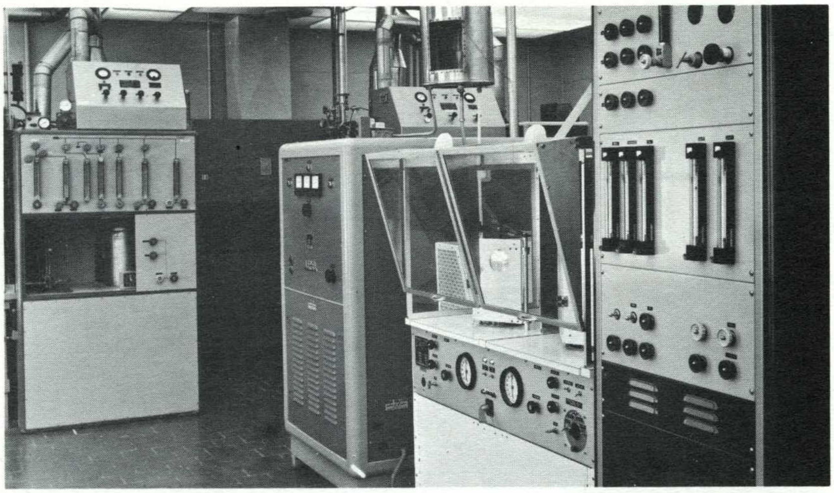
Transitron

Integrated Circuit Operations

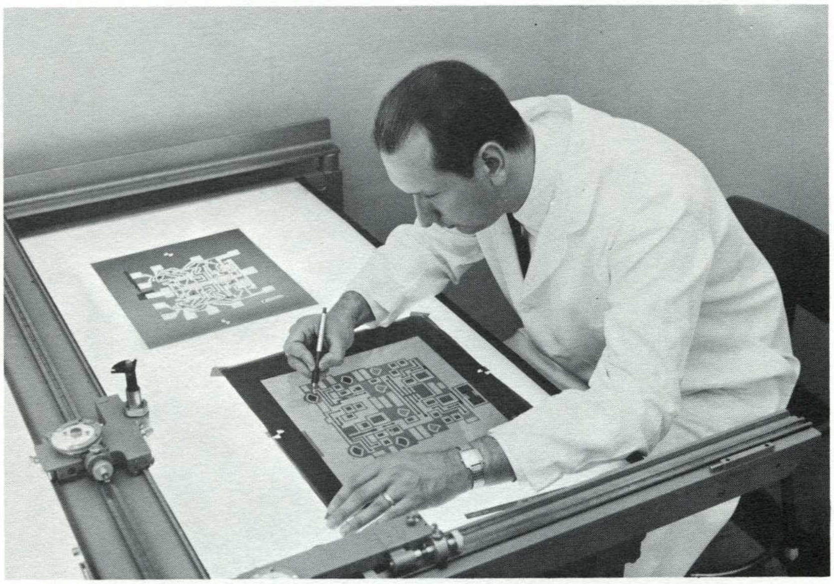


CRYSTAL GROWING — Single crystal Czochralski silicon crystals are grown in furnaces designed and built by Transitron. Dopants used are antimony, arsenic, phosphorous and boron. The crystals are cut, lapped and polished prior to further processing.

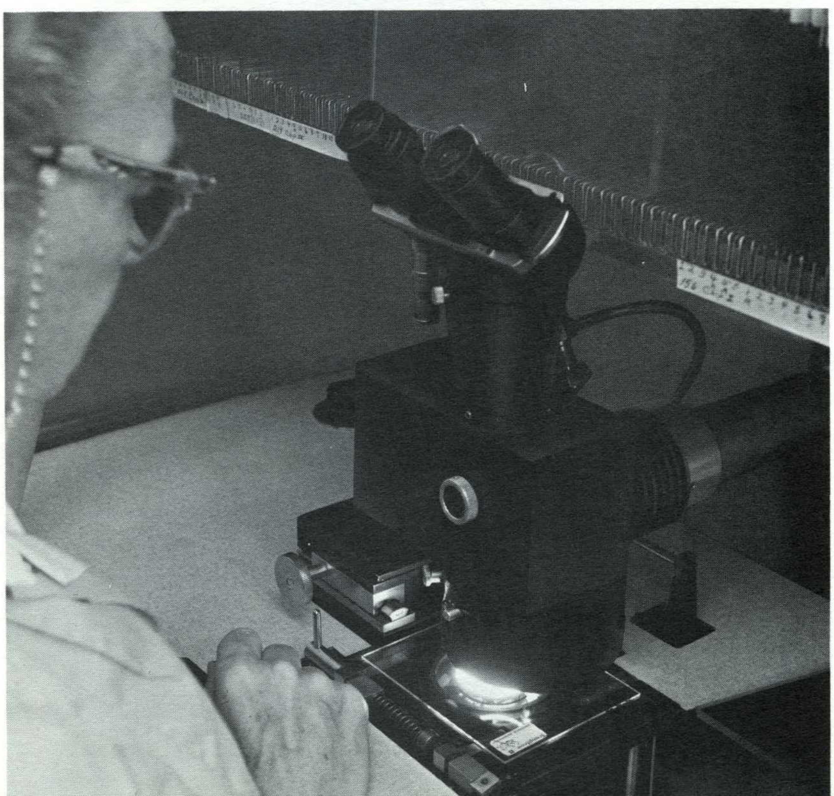
EPITAXIAL — Boron, arsenic, and phosphorous doped epitaxial layers are grown in a clean room. Laminar flow clean benches further reduce the foreign particle size to less than 3 microns during slice preparation and furnace loading and unloading. Layers are grown with resistivities ranging from 0.02 to 8 ohm-centimeters. Photomicrographic equipment and an Infrared Interferometer are utilized in addition to the standard electrical test equipment.

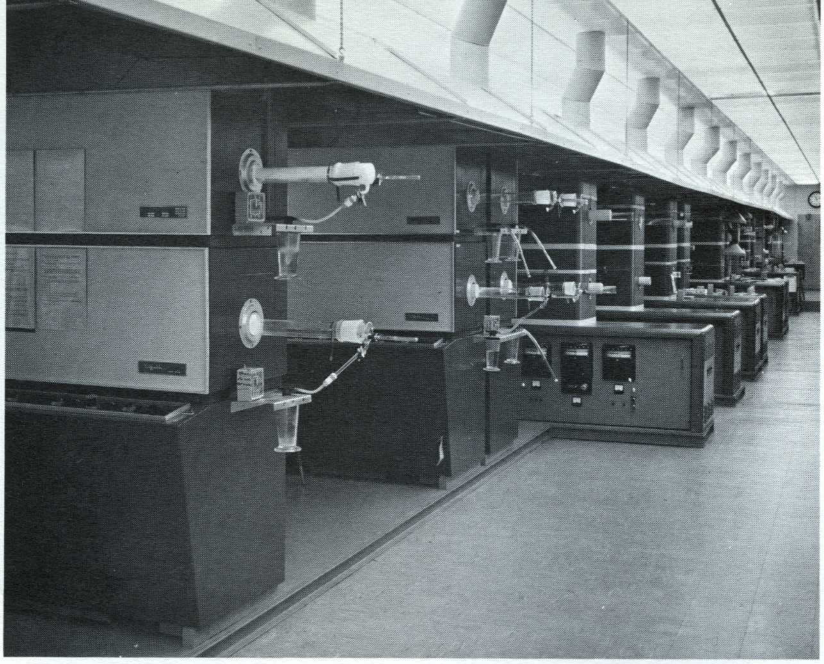


MASK MAKING — Integrated circuit photomasks are made in Transitron's photographic laboratory. Both the standard emulsion-on-glass type mask and evaporated chromium-on-glass masks are produced. An intermediate master is made from the original art work on a precision reduction camera capable of resolving a 3 micron line width. The master mask is then made from the intermediate mask on a Photorepeater, which has a positional error of less than .5 micron. A solid state counter and shaft encoder control stepping distance. Comparators, accurate to .5 micron in two coordinates are used to inspect the masks. With this equipment, and the processing techniques developed by Transitron, line widths of one micron and registration errors of less than one micron are achieved.

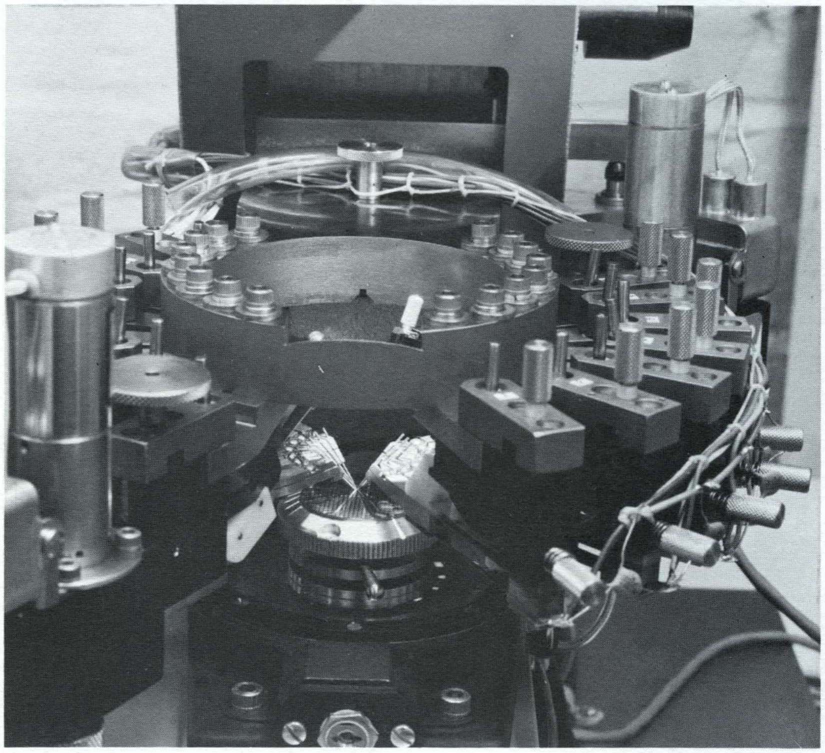


MASK ALIGNMENT — Mask alignment is performed on equipment designed and built at Transitron. This alignment equipment is a significant advancement over commercially available equipment and has a registration error of less than 0.5 micron.

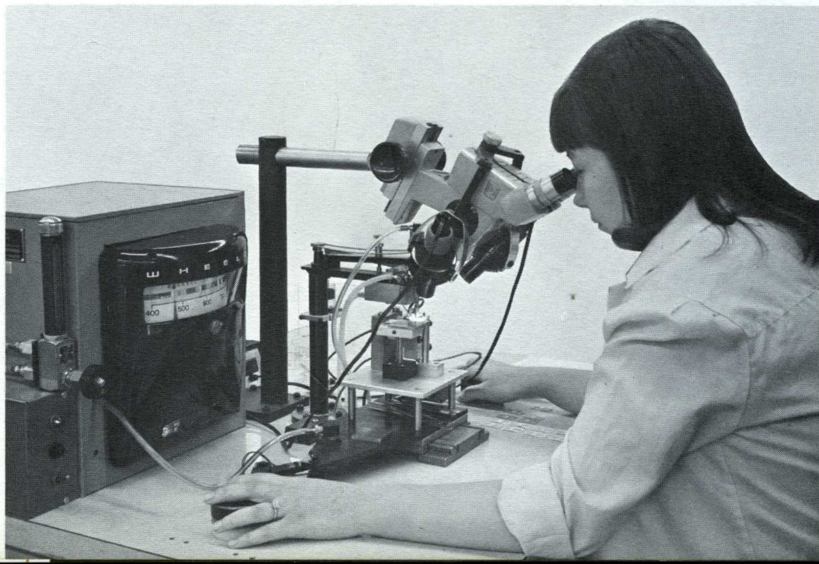




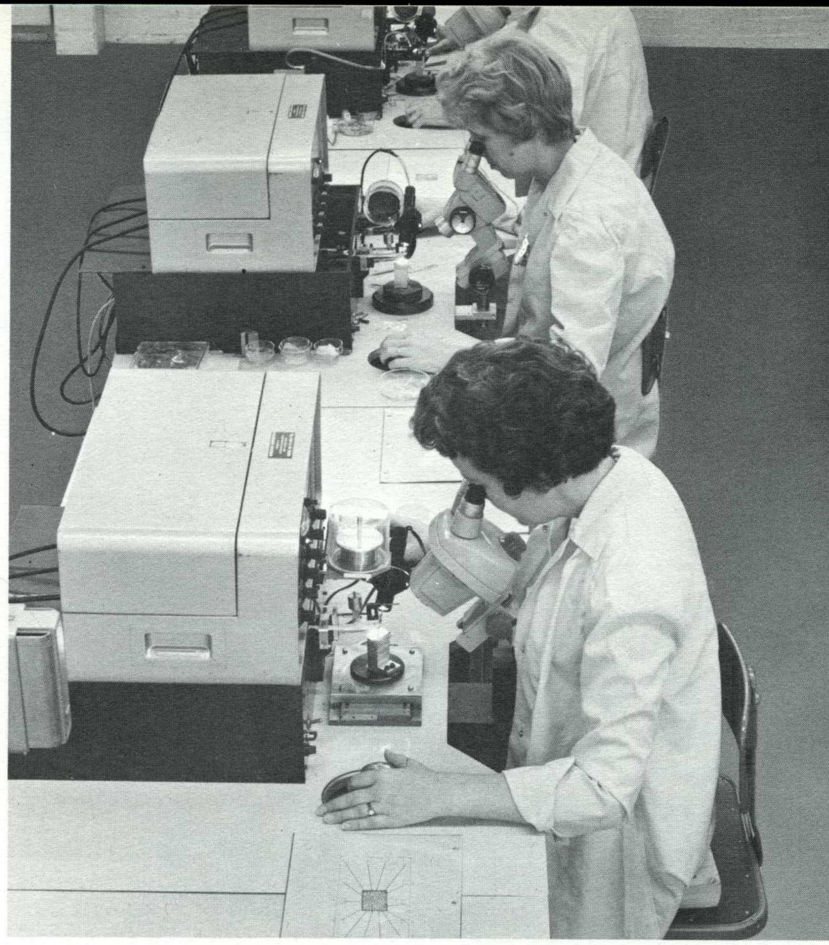
FURNACES — Diffusion is performed in single zone furnaces. The furnaces for diffusion of P-type and N-type dopants are physically separated in different controlled atmosphere rooms. These furnaces provide temperatures up to 1300°C with a temperature stability of ±0.5°C and are solid state module controlled.



MULTIPLE PROBE TESTING — Automatic test equipment is used for testing the dice on the slice prior to scribing and mounting in the package.



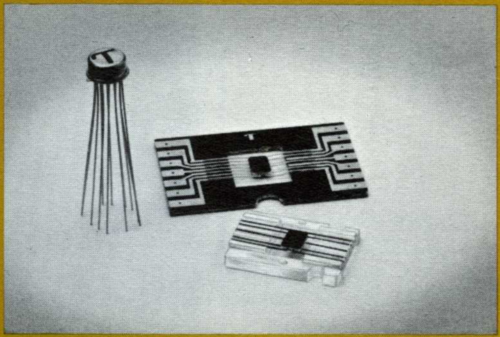
DIE MOUNTING — The integrated circuits are packaged using semi-automatic die mounting equipment. One of the unique features is the automatic die edge pickup which eliminates any possible surface damage.



BONDING — Aluminum leads are ultrasonically bonded to the integrated circuit, also using Transitron designed and fabricated equipment.

TESTING — Each Transitron integrated circuit is tested on automatic, high-speed, multiparameter test systems. These test systems, which were designed and constructed at Transitron, also include a punched paper tape output of test results for data logging and computer analysis of test data.

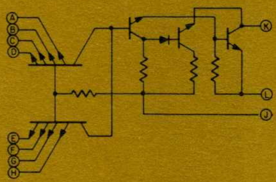
Transitron
electronic corporation



Transitron
HLTTL
Integrated Circuits

SINGLE 8-INPUT NAND/NOR GATE

TNG 3011	TNG 3011F
3012	3012F
3013	3013F
3014	3014F

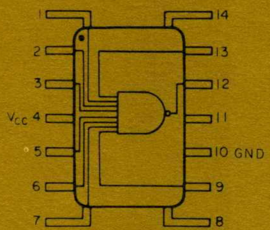


+LOGIC

$K = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$

−LOGIC

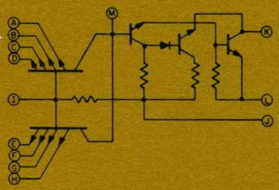
$K = \overline{A + B + C + D + E + F + G + H}$



PIN CONNECTION			
TO-5		Flat Package	
Circuit Letter	Pin No.	Circuit Letter	Pin No.
A	1	A	13
B	2	B	1
C	3	C	2
D	4	D	3
E	8	E	5
F	9	F	6
G	10	G	7
H	11	H	9
J	12	J	4
K	7	K	12
L	6	L	10

EXPANDABLE SINGLE 8-INPUT NAND/NOR GATE

TNG 3051F
3052F
3053F
3054F

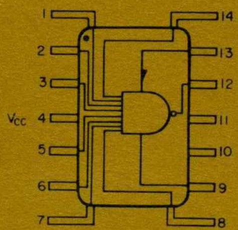


+LOGIC

$K = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot ---}$

−LOGIC

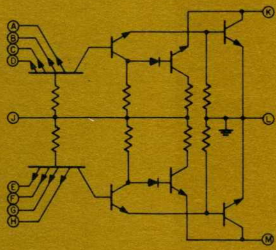
$K = \overline{A + B + C + D + E + F + G + H + ---}$



PIN CONNECTION (Flat Package)	
Circuit Letter	Pin Number
A	1
B	2
C	3
D	14
E	5
F	6
G	7
H	8
I	9
J	4
K	12
L	10
M	13

DUAL 4-INPUT NAND/NOR GATE

TNG 3111	TNG 3111F
3112	3112F
3113	3113F
3114	3114F



+LOGIC

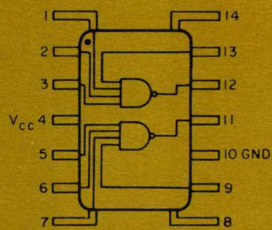
$K = \overline{A \cdot B \cdot C \cdot D}$

$M = \overline{E \cdot F \cdot G \cdot H}$

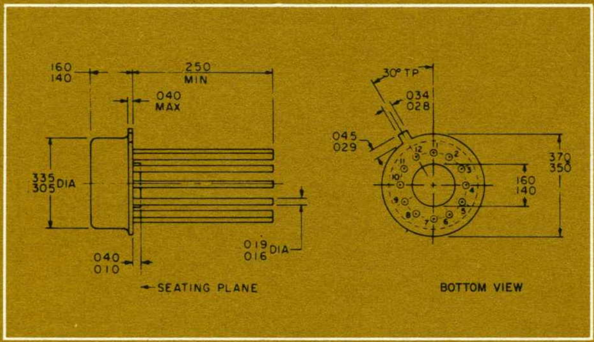
−LOGIC

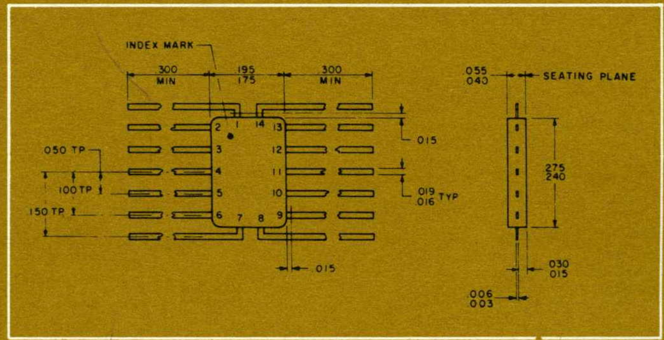
$K = \overline{A + B + C + D}$

$M = \overline{E + F + G + H}$



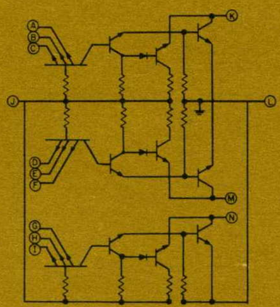
PIN CONNECTION			
TO-5		Flat Package	
Circuit Letter	Pin No.	Circuit Letter	Pin No.
A	1	A	13
B	2	B	1
C	3	C	2
D	4	D	3
E	8	E	5
F	9	F	6
G	10	G	7
H	11	H	9
J	12	J	4
K	5	K	12
L	6	L	10
M	7	M	11





TRIPLE 3-INPUT NAND/NOR GATE

TNG 3311F
3312F
3313F
3314F

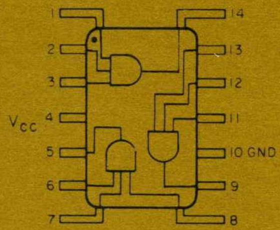


+LOGIC

$K=\overline{A\cdot B\cdot C}$ $M=\overline{D\cdot E\cdot F}$ $N=\overline{G\cdot H\cdot I}$

−LOGIC

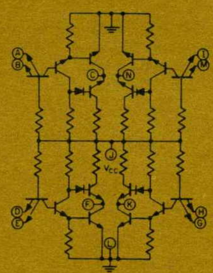
$K=\overline{A+B+C}$ $M=\overline{D+E+F}$ $N=\overline{G+H+I}$



PIN CONNECTION (Flat Package)	
Circuit Letter	**Pin Number**
A	1
B	2
C	3
D	6
E	7
F	8
G	11
H	12
I	13
J	4
K	14
L	10
M	5
N	9

QUAD 2-INPUT NAND/NOR GATE

TNG 3411F
3412F
3413F
3414F

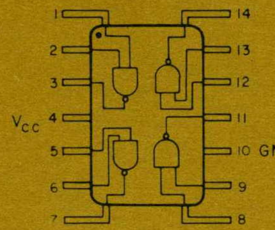


+LOGIC

$C=\overline{A\cdot B}$ $F=\overline{D\cdot E}$ $K=\overline{G\cdot H}$ $N=\overline{M\cdot I}$

−LOGIC

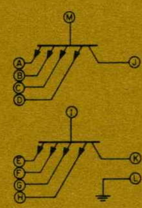
$C=\overline{A+B}$ $F=\overline{D+E}$ $K=\overline{G+H}$ $N=\overline{M+I}$

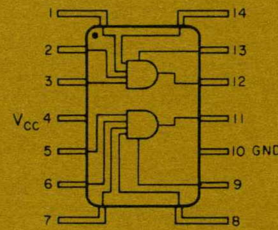


PIN CONNECTION (Flat Package)	
Circuit Letter	**Pin Number**
A	1
B	2
C	3
D	5
E	6
F	7
G	8
H	9
I	12
J	4
K	11
L	10
M	13
N	14

DUAL 4-INPUT AND EXPANDER

TNG 3511F
3512F



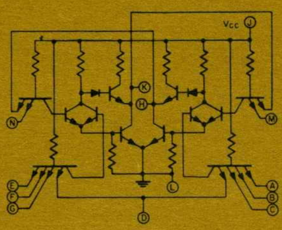


PIN CONNECTION (Flat Package)	
Circuit Letter	**Pin Number**
A	14
B	1
C	2
D	3
E	5
F	6
G	7
H	8
I	9
J	12
K	11
L	10
M	13

FOLD OUT →

GATED 2-PHASE FLIP-FLOP

TFF 3011 TFF 3011F
3012 3012F
3013 3013F
3014 3014F



+LOGIC

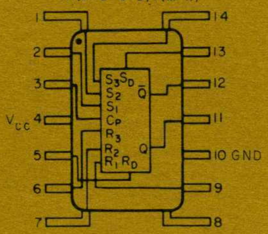
$K = (\bar{E} + \bar{F} + \bar{G} + \bar{D}) \cdot (\bar{N} + \bar{H})$

$H = (\bar{A} + \bar{B} + \bar{C} + \bar{D}) \cdot (\bar{M} + \bar{K})$

-LOGIC

$K = (\bar{E} \cdot \bar{F} \cdot \bar{G} \cdot \bar{D}) + (\bar{M} \cdot \bar{H})$

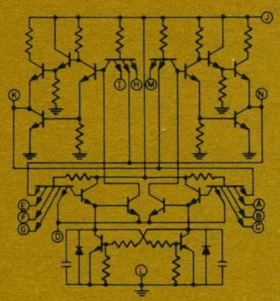
$H = (\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D}) + (\bar{M} \cdot \bar{K})$



PIN CONNECTION			
TO-5		Flat Package	
Circuit Letter	Pin No.	Circuit Letter	Pin No.
A	2	A	14
B	3	B	1
C	4	C	2
D	1	D	3
E	8	E	6
F	9	F	7
G	10	G	9
H	5	H	12
J	12	J	4
K	7	K	11
L	6	L	10
		M	13
		N	5

AC COUPLED J-K FLIP-FLOP

TFF 3211F
3212F
3213F
3214F

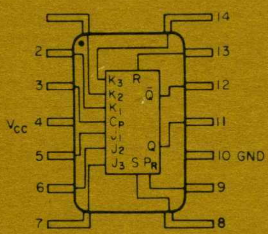


+LOGIC

$K = Q_N + 1 = J\bar{Q}_N + \bar{K}Q_N$

-LOGIC

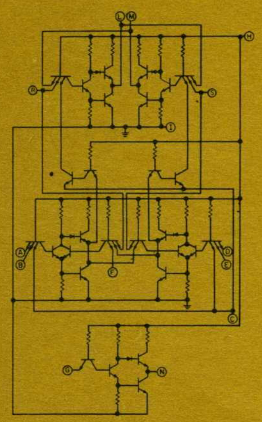
$N = Q_N + 1 = JQ_N + KQ_N$

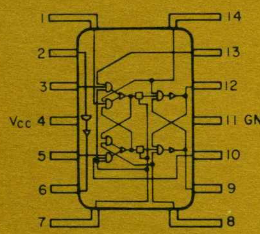


PIN CONNECTION (Flat Package)	
Circuit Letter	Pin Number
A	14
B	1
C	2
D	3
E	5
F	6
G	7
H	8
I	9
J	4
K	11
L	10
M	13
N	12

GENERAL PURPOSE MASTER-SLAVE FLIP-FLOP WITH BUFFER

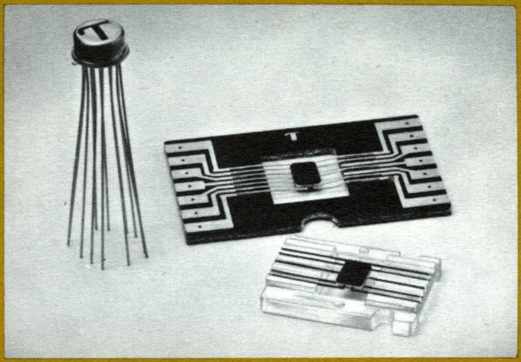
TFF 3115 TFF 3111F TFF 3115F
3116 3112F 3116F
3117 3113F 3117F
3118 3114F 3118F





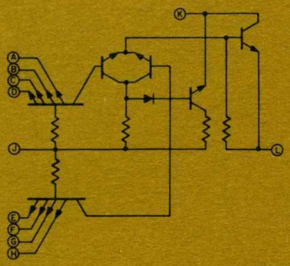
PIN CONNECTION			
TO-5		Flat Package	
Circuit Letter	Pin No.	Circuit Letter	Pin No.
A	8	A	5
C	2	B	10
D	5	C	7
F	11	D	3
G	10	E	13
H	12	F	1
I	6	G	2
L	7	H	4
M	4	I	11
N	1	L	9
R	9	M	12
S	3	N	6
		R	8
		S	14

Transitron
HLTTL
Integrated Circuits
(continued)



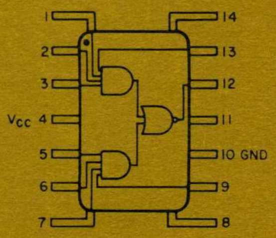
DUAL 4-INPUT OR GATE

TNG 3211 TNG 3211F
3212 3212F
3213 3213F
3214 3214F



+LOGIC
$K=\overline{(A\cdot B\cdot C\cdot D)+(E\cdot F\cdot G\cdot H)}$

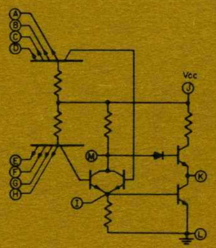
−LOGIC
$K=\overline{(A+B+C+D)\cdot(E+F+G+H)}$



PIN CONNECTION			
TO-5		Flat Package	
Circuit Letter	Pin No.	Circuit Letter	Pin No.
A	1	A	13
B	2	B	1
C	3	C	2
D	4	D	3
E	8	E	5
F	9	F	6
G	10	G	7
H	11	H	9
J	12	J	4
K	7	K	12
L	6	L	10

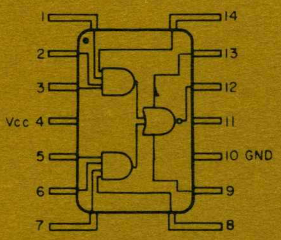
EXPANDABLE DUAL 4-INPUT OR GATE

TNG 3251F
3252F
3253F
3254F



+LOGIC
$K=\overline{(A\cdot B\cdot C\cdot D)+(E\cdot F\cdot G\cdot H)+---}$

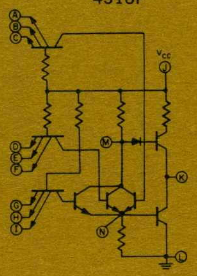
−LOGIC
$K=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot---}$



PIN CONNECTION (Flat Package)	
Circuit Letter	Pin Number
A	14
B	1
C	2
D	3
E	5
F	6
G	7
H	8
I	13
J	4
K	12
L	10
M	9

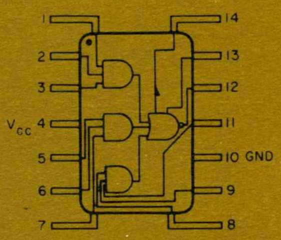
EXPANDABLE TRIPLE 3-INPUT OR GATE (MAJORITY DECISION GATE)

TNG 4315F
4316F
4317F
4318F



+LOGIC
$K=\overline{(A\cdot B\cdot C)+(D\cdot E\cdot F)+(G\cdot H\cdot I)+---}$

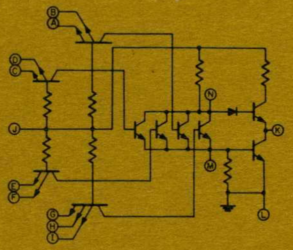
−LOGIC
$K=\overline{(A+B+C)\cdot(D+E+F)\cdot(G+H+I)\cdot---}$



PIN CONNECTION (Flat Package)	
Circuit Letter	Pin Number
A	1
B	2
C	3
D	5
E	6
F	7
G	8
H	9
I	11
J	4
K	12
L	10
M	13
N	14

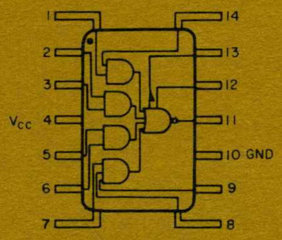
EXPANDABLE QUAD 2-INPUT OR GATE

TNG 4415F
4416F
4417F
4418F

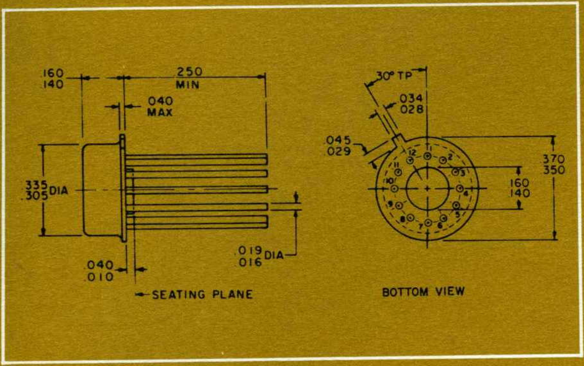


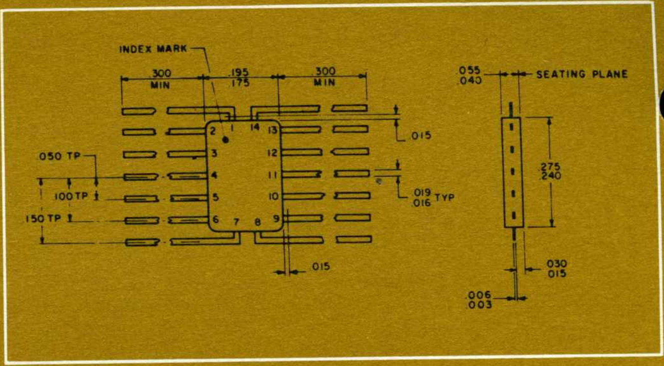
+LOGIC
$K=\overline{(A\cdot B)+(C\cdot D)+(E\cdot F)+(G\cdot H\cdot I)+---}$

−LOGIC
$K=\overline{(A+B)\cdot(C+D)\cdot(E+F)\cdot(G+H+I)\cdot---}$



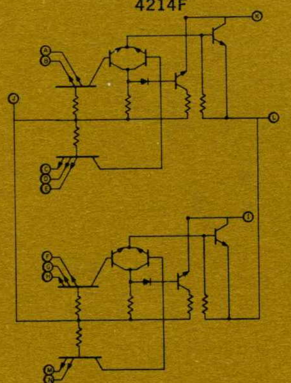
PIN CONNECTION (Flat Package)	
Circuit Letter	Pin Number
A	14
B	1
C	2
D	3
E	5
F	6
G	7
H	8
I	9
J	4
K	11
L	10
M	13
N	12





DUAL EXCLUSIVE OR GATE

TNG 4211F
4212F
4213F
4214F



+LOGIC

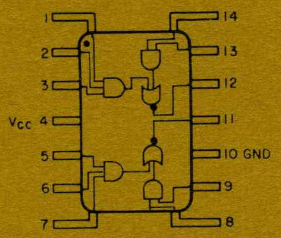
$I = \overline{(F \cdot G \cdot H) + (M \cdot N)}$

$K = \overline{(A \cdot B) + (C \cdot D \cdot E)}$

-LOGIC

$I = \overline{(F + G + H) \cdot (M + N)}$

$K = \overline{(A + B) \cdot (C + D + E)}$

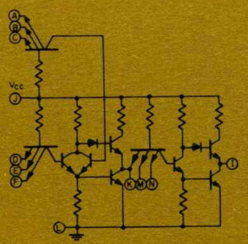


PIN CONNECTION (Flat Package)

Circuit Letter	Pin Number
A	13
B	14
C	1
D	2
E	3
F	5
G	6
H	7
I	11
J	4
K	12
L	10
M	8
N	9

EXCLUSIVE OR GATE WITH COMPLEMENT

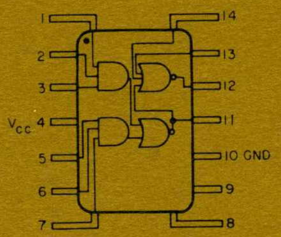
TNG 4611F
4612F
4613F
4614F



+LOGIC

$K = \overline{(A \cdot B \cdot C) + (D \cdot E \cdot F)}$ $\quad I = \overline{(K \cdot M \cdot N)}$

$I = (A \cdot B \cdot C) + (E \cdot F \cdot G) + \overline{M} + \overline{N}$

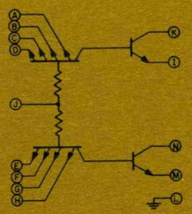


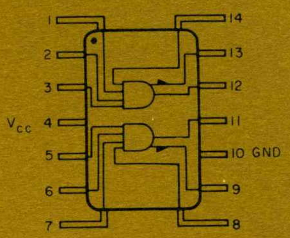
PIN CONNECTION (Flat Package)

Circuit Letter	Pin Number
A	1
B	2
C	3
D	5
E	6
F	7
I	12
J	4
K	11
L	10
M	13
N	14

DUAL 4-INPUT OR EXPANDER

TNG 4011F
4012F



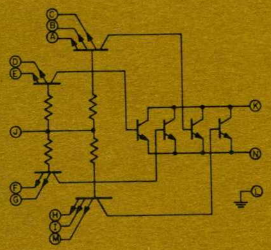


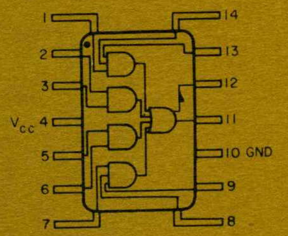
PIN CONNECTION (Flat Package)

Circuit Letter	Pin Number
A	1
B	2
C	3
D	14
E	5
F	6
G	7
H	8
I	13
J	4
K	12
L	10
M	9
N	11

QUAD 2-INPUT OR EXPANDER

TNG 4511F
4512F



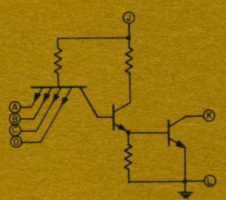


PIN CONNECTION (Flat Package)

Circuit Letter	Pin Number
A	13
B	14
C	1
D	2
E	3
F	5
G	6
H	7
I	8
J	4
K	11
L	10
M	9
N	12

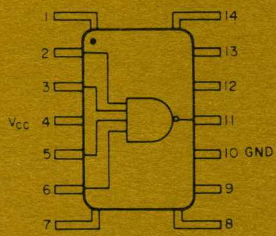
SINGLE 4-INPUT LAMP DRIVER

TNG 5321 TNG 5321F
5322 5322F
5323 5323F
5324 5324F



+LOGIC $K=\overline{A\cdot B\cdot C\cdot D}$

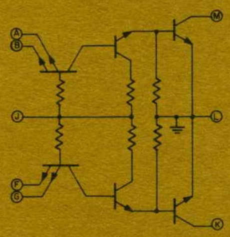
-LOGIC $K=\overline{A+B+C+D}$



PIN CONNECTION			
TO-5		Flat Package	
Circuit Letter	Pin No.	Circuit Letter	Pin No.
A	2	A	2
B	3	B	3
C	4	C	5
D	5	D	6
J	12	J	4
K	7	K	11
L	6	L	10

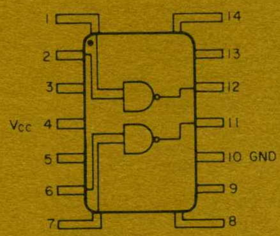
DUAL 2-INPUT LAMP DRIVER

TNG 5421 TNG 5421F
5422 5422F
5423 5423F
5424 5424F



+LOGIC $M=\overline{A\cdot B}$ $K=\overline{F\cdot G}$

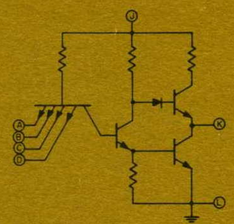
-LOGIC $M=\overline{A+B}$ $K=\overline{F+G}$



PIN CONNECTION			
TO-5		Flat Package	
Circuit Letter	Pin No.	Circuit Letter	Pin No.
A	2	A	1
B	3	B	2
F	9	F	6
G	10	G	7
J	12	J	4
K	7	K	11
L	6	L	10
M	5	M	12

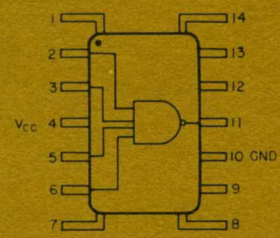
SINGLE 4-INPUT LINE DRIVER

TNG 5121 TNG 5121F
5122 5122F
5123 5123F
5124 5124F



+LOGIC $K=\overline{A\cdot B\cdot C\cdot D}$

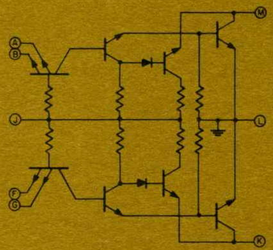
-LOGIC $K=\overline{A+B+C+D}$



PIN CONNECTION			
TO-5		Flat Package	
Circuit Letter	Pin No.	Circuit Letter	Pin No.
A	2	A	2
B	3	B	3
C	4	C	5
D	5	D	6
J	12	J	4
K	7	K	11
L	6	L	10

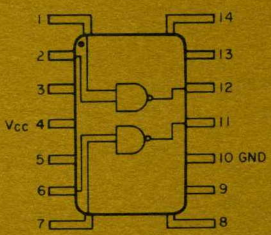
DUAL 2-INPUT LINE AND CLOCK DRIVER

TNG 5221 TNG 5221F
5222 5222F
5223 5223F
5224 5224F



+LOGIC $M=\overline{A\cdot B}$ $K=\overline{F\cdot G}$

-LOGIC $M=\overline{A+B}$ $K=\overline{F+G}$



PIN CONNECTION			
TO-5		Flat Package	
Circuit Letter	Pin No.	Circuit Letter	Pin No.
A	2	A	1
B	3	B	2
F	9	F	6
G	10	G	7
J	12	J	4
K	7	K	11
L	6	L	10
M	5	M	12

Transitron

HLTTL Circuit Listing

Type Number	Package	Circuit Description
TNG3011 thru 3014	F, T	Single 8 input Nand/Nor Gate
TNG3015 thru 3018	F, T	Single 6 input Nand/Nor Gate
TNG3041 thru 3044	F, T	Single 8 input Nand/Nor Gate with 10 nsec tpd
TNG3045 thru 3048	F, T	Single 6 input Nand/Nor Gate with 10 nsec tpd
TNG3051 thru 3054	F	Single 8 input Nand/Nor Gate, expandable
TNG3111 thru 3114	F, T	Dual 4 input Nand/Nor Gate
TNG3115 thru 3118	F, T	Dual 3 input Nand/Nor Gate
TNG3141 thru 3144	F, T	Dual 4 input Nand/Nor Gate with 10 nsec tpd
TNG3145 thru 3148	F, T	Dual 3 input Nand/Nor Gate with 10 nsec tpd
TNG3211 thru 3214	F, T	Dual 4 input Nand/OR Gate
TNG3215 thru 3218	F, T	Dual 3 input Nand/OR Gate
TNG3241 thru 3244	F, T	Dual 4 input Nand/OR Gate with 10 nsec tpd
TNG3245 thru 3248	F, T	Dual 3 input Nand/OR Gate with 10 nsec tpd
TNG3251 thru 3254	F	Dual 4 input Nand/OR Gate, expandable
TNG3311 thru 3314	F	Triple 3 input Nand/Nor Gate
TNG3411 thru 3414	F	Quad 2 input Nand/Nor Gate
TNG3511 and 3512	F, T	Dual 4 input AND expander Gate
TNG4011 and 4012	F, T	Dual 4 input OR expander Gate
TNG4211 thru 4214	F	Dual Exclusive OR Gate
TNG4251 thru 4254	F	Dual Exclusive OR Gate, expandable
TNG4311 thru 4314	F	Triple 3 input Nand/OR Gate
TNG4315 thru 4318	F	Triple 3 input Nand/OR Gate, expandable
TNG4411 thru 4414	F	Quad 2 input Nand/OR Gate
TNG4415 thru 4418	F	Quad 2 input Nand/OR Gate, expandable
TNG4511 and 4512	F	Quad 2 input OR expander Gate
TNG4611 thru 4614	F	Exclusive OR with complement
TNG5121 thru 5124	F	Single 4 input Line or Clock Driver
TNG5221 thru 5224	F	Dual 2 input Line or Clock Driver
TNG5321 thru 5324	F	Single 4 input Lamp Driver
TNG5421 thru 5424	F	Dual 2 input Lamp Driver
TFF3011 thru 3014	T, F	Dual 3 input Gated 2 phase flip-flop
TFF3015 thru 3018	T, F	Dual 2 input Gated 2 phase flip-flop
TFF3111 thru 3114	F	Master Slave Flip-Flop 4 input with Buffer
TFF3115 thru 3118	T, F	Master Slave Flip-Flop 2 input with Buffer
TFF3121 thru 3124	T, F	Master Slave Flip-Flop 4 input without Buffer
TFF3125 thru 3128	T, F	Master Slave Flip-Flop 2 input without Buffer
TFF3211 thru 3214	F	Charge Storage J-K flip-flop
TFF3251 thru 3254	F	Chg. Storage J-K flip-flop, Expandable for OR

Fan Out and Operating Temperature as Indicated by Type Number

Type No.	Fan Out	Temp. Range °C
___1 and ___5	15 (40)	−55 to +125
___2 and ___6	15 (40)	0 to + 75
___3 and ___7	7 (24)	−55 to +125
___4 and ___8	7 (24)	0 to + 75

NOTE: Package Key as follows:

(a) T = 12 lead, short cap, TO-5 package — For units in this package use type number as listed.

(b) F = 14 lead, .195 x .260 inch flat package — For units in this package use type numbers with F suffix (e.g., TNG3011F).

Transitron

HLTTL Integrated Circuit Manufacturers' Type Cross-reference and Pin Configuration Guide

Circuit Description	F.O.	Temp. Range	Transition Type No.	Sylvania Type No.	Texas Instr. Type No.	Pin Configurations Available from Transitron
Single 8 input Nand/Nor Gate	15	F	TNG3011F	SG60	General type SN5430	B, C, D
	15	R	TNG3012F	*SG62		
	7	F	TNG3013F	SG61		
	7	R	TNG3014F	*SG63		
Single 8 input Nand/Nor Gate, Expandable	15	F	TNG3051F	SG120		B
	15	R	TNG3052F	*SG122		
	7	F	TNG3053F	SG121		
	7	R	TNG3054F	*SG123		
Dual 4 input Nand/Nor Gate	15	F	TNG3111F	SG40	General type SN5420	B, C, D
	15	R	TNG3112F	*SG42		
	7	F	TNG3113F	SG41		
	7	R	TNG3114F	*SG43		
Triple 3 input Nand/Nor Gate	15	F	TNG3311F	SG190	General type SN5410	A, B, C
	15	R	TNG3312F	SG192		
	7	F	TNG3313F	SG191		
	7	R	TNG3314F	SG193		
Quad 2 input Nand/Nor Gate	15	F	TNG3411F	SG140	General type SN5400	B, C
	15	R	TNG3412F	*SG142		
	7	F	TNG3413F	SG141		
	7	R	TNG3414F	*SG143		
Dual 4 And Expander Gate	—	F	TNG3511F	SG180-181		B
	—	R	TNG3512F	SG182-183		
Dual 4 input OR Gate, Expandable	15	F	TNG3251F	SG110		B
	15	R	TNG3252F	*SG112		
	7	F	TNG3253F	SG111		
	7	R	TNG3254F	*SG113		
Exclusive OR Gate with Complement	15	F	TNG4611F	SG90		B
	15	R	TNG4612F	*SG92		
	7	F	TNG4613F	SG91		
	7	R	TNG4614F	*SG93		
Dual Exclusive OR Gates	15	F	TNG4211F		General type SN5450	A, C
	15	R	TNG4212F			
	7	F	TNG4213F			
	7	R	TNG4214F			
Triple 3 input OR Gate, Expandable	15	F	TNG4315F	SG100		B
	15	R	TNG4316F	*SG102		
	7	F	TNG4317F	SG101		
	7	R	TNG4318F	*SG103		
Quad 2 input OR Gate, Expandable	15	F	TNG4415F	SG50		B
	15	R	TNG4416F	*SG52		
	7	F	TNG4417F	SG51		
	7	R	TNG4418F	*SG53		
Dual 4 OR Expander Gate	—	F	TNG4011F	SG170-171	General type SN5460	B, C
	—	R	TNG4012F	SG172-173		
Quad 2 input OR Expander Gate	—	F	TNG4511F	SG150-151		B
	—	R	TNG4512F	SG152-153		
Single 2 input Line Driver	40	F	TNG5125F	*SG130		B
	40	R	TNG5126F	*SG132		
	24	F	TNG5127F	*SG131		
	24	R	TNG5128F	*SG133		
Dual 4 input Line Driver	40	F	TNG5211F		General type SN5440	C
	40	R	TNG5212F			
	24	F	TNG5213F			
	24	R	TNG5214F			
Dual 3 input Gated 2 phase flip-flop	15	F	TFF3011F	SF20		B
	15	R	TFF3012F	*SF22		
	7	F	TFF3013F	SF21		
	7	R	TFF3014F	*SF23		
4 input Master Slave flip-flop with Buffer	15	F	TFF3111F			A
	15	R	TFF3112F			
	7	F	TFF3113F			
	7	R	TFF3114F			
2 input Master Slave flip-flop with Buffer	15	F	TFF3115F			A
	15	R	TFF3116F			
	7	F	TFF3117F			
	7	R	TFF3118F			
4 input Master Slave flip-flop without Buffer	15	F	TFF3121F			A
	15	R	TFF3122F			
	7	F	TFF3123F			
	7	R	TFF3124F			
2 input Master Slave flip-flop without Buffer	15	F	TFF3125F			A
	15	R	TFF3126F			
	7	F	TFF3127F			
	7	R	TFF3128F			
Charge Storage J-K flip-flop	15	F	TFF3211F	SF50		B
	15	R	TFF3212F	*SF52		
	7	F	TFF3213F	SF51		
	7	R	TFF3214F	*SF53		

NOTES:

1. Under "Temperature Range" column, F equal −55°C to +125°C and R equal 0 to +75°C.
2. In "Sylvania type" column the * means that Transitron devices have a higher guaranteed fanout than the Sylvania type listed.
3. In "Pin Configuration" column where more than one configuration is listed, the standard Transitron configuration is denoted by a line under the letter (e.g., A)
4. Key to the pin configurations are as follows:

A = Transitron
B = Sylvania
C = Texas Instruments
D = Phoenix Gate

RATINGS

Voltage:	Min.	Typ.	Max.
Supply Voltage			8.0V
Supply Surge 1 sec			12.0V
Supply Operating	4.5	5.0	6.0V
Input Voltage			5.5V
Output Voltage			5.5V

Temperature and Power	Min.	Typ.	Max.
Operating	—55		+125°C
Storage	—65		+200°C
Thermal Gradient Junction—Air			.3°C/mW
Thermal Gradient Junction—Case			.1°C/mW
Power Diss. per Gate 50% Duty Cycle, $V_{cc} = 5V$		15mW	

Transitron
HLTTL specifications

$T_A = -55$ to 125°C

Gates and Flip Flops
F.O. = 15 and 7

Line Drivers
F.O. = 40 and 24

Lamp Driver
$I_L = 60$ mA

ELECTRICAL CHARACTERISTICS

(V_{cc} = 5V)	Values @ Temperature Ambient				
	Symbol	—55°C	25°C	+125°C	Units
V_{out} "1" $I_L = I_{L\text{"1"}}$	V_o "1"	2.8	3.2	3.35	V min.
@ V_{in} =		.45	.45	.45	V
V_{out} "1" Threshold $I_L = I_{L\text{"1"}}$	V_{oth} "1"	2.5	2.4	2.7	V min.
@ V_{in} =		1.0	1.2	.9	V
V_{out} "0" Threshold $I_L = I_{L\text{"0"}}$	V_{oth} "0"	.45	.45	.45①	V max.
@ V_{in} =		2.0	1.7	1.4	V
V_{out} "0" $I_L = I_{L\text{"0"}}$	V_o "0"	.40	.40	.45①	V max.
@ V_{in} =		2.8	2.8	2.8	V

GATES AND FLIP FLOPS (at all operating temperatures)

$I_{in\text{"0"}}$ = 1.33 mA max. @ V_{in} = 0V②③
$I_{L\text{"0"}}$ = 20 mA (F.O. = 15)
$I_{L\text{"0"}}$ = 10 mA (F.O. = 7)

$I_{in\text{"1"}}$ = 100 μA max. @ V_{in} = 4.5V②④
$I_{L\text{"1"}}$ = 1.5 mA (F.O. = 15)
$I_{L\text{"1"}}$ = .7 mA (F.O. = 7)

Power per Gate "ON" I_s = 6.0 mA max.⑤ [.9 mA per input node, 5.1 mA per output stage]
Power per Gate "OFF" I_s = 3.0 mA max.⑤ [1.8 mA per input node, 1.2 mA per output stage]
Circuit Bkdn. "OFF" 8V_{min} @ I_s = 5.0 mA⑤ [3.0 mA per input node, 2.0 mA per output stage]
Input Bkdn. 5.5V min. @ I_{in} = 1.0 mA④
Output Leakage Current = 250 μA max. @ V_{out} = 5.5V; V_{in} = 0V
Output Short Circuit Current = 45 mA max., 10 mA min. @ $V_{out} = V_{in}$ = 0V

Propagation Delay $t_{pd} = \frac{t_{on} + t_{off}}{2}$ = 18 nsec max. / = 10 nsec max. (High Speed Version) } F.O. = 1; C_L = 15 pf; T_A = 25°C⑥

LINE DRIVERS (at all operating temperatures)

$I_{in\text{"0"}}$ = 2.7 mA max. @ V_{in} = 0V③
$I_{L\text{"0"}}$ = 54 mA (F.O. = 40)
$I_{L\text{"0"}}$ = 32 mA (F.O. = 24)

$I_{in\text{"1"}}$ = 200 μA max. @ V_{in} = 4.5V④
$I_{L\text{"1"}}$ = 4.0 mA (F.O. = 40)
$I_{L\text{"1"}}$ = 2.4 mA (F.O. = 24)

Power per Gate "ON" I_s = 12.0 mA max.⑤ [1.8 mA per input node, 10.2 mA per output stage]
Power per Gate "OFF" I_s = 6.0 mA max.⑤ [3.6 mA per input node, 2.4 mA per output stage]
Circuit Bkdn. "OFF" 8V min. @ I_s = 10.0 mA⑤ [6.0 mA per input node, 4.0 mA per output stage]
Input Bkdn. 5.5 V_{min} @ I_{in-} = 1.5 mA④
Output Leakage Current = 300 μA max. @ V_{out} = 5.5V; V_{in} = 0
Output Short Circuit Current = 90 mA max., 20 mA min. @ $V_{out} = V_{in}$ = 0V

Propagation Delay $t_{pd} = \frac{t_{on} + t_{off}}{2}$ = 18 nsec max. @ F.O. = 1; C_L = 100 pf; T_A = 25°C⑥

LAMP DRIVERS (at all operating temperatures)

$I_{in\text{"0"}}$ = 2.7 mA max. @ V_{in} = 0V③
$I_{L\text{"0"}+}$ = 60 mA

$I_{in\text{"1"}}$ = 200 μA max @ V_{in} = 4.5V④
$I_{L\text{"1"}}$ = .5 mA into output terminal

Power per Gate "ON" I_s = 12.0 mA max.⑤ [1.8 mA per input node, 10.2 mA per output stage]
Power per Gate "OFF" I_s = 6.0 mA max.⑤ [3.6 mA per input node, 2.4 mA per output stage]
Circuit Bkdn. "OFF" 8V_{min} @ I_s = 10.0 mA⑤ [6.0 mA per input node, 4.0 mA per output stage]
Input Bkdn. 5.5V_{min} @ I_{in-} = 1.5 mA④
Output Leakage Current = 300 μA max. @ V_{out} = 8V; V_{in} = 0V

NOTES:
① .6V max. for lamp drivers
② One unit load
③ Other inputs @ 4.5V
④ Other inputs ground or open
⑤ Dependent on ckt function
⑥ Unused input @ logic "1" = 3.5V

Transitron
HLTTL specifications

$T_A = 0$ to $75°C$
Gates and Flip-Flops
F.O. = 15 and 7
Line Drivers
F.O. = 40 and 24
Lamp Drivers
$I_L = 60$ mA

RATINGS

Voltage	Min.	Typ.	Max.
Supply Voltage			7.0V
Supply Surge 1 sec			12.0V
Supply Operating	4.5	5.0	6.0V
Input Voltage			5.5V
Output Voltage			5.5V

Temperature and Power	Min.	Typ.	Max.
Operating	0		+ 75°C
Storage	—65		+200°C
Thermal Gradient Junction—Air			.3°C/mW
Thermal Gradient Junction—Case			.1°C/mW
Power Diss. per Gate 50% Duty Cycle $V_{cc} = 5.0V$		15mW	

ELECTRICAL CHARACTERISTICS

($V_{cc} = 5.0V$)	Values @ Temperature Ambient				
	Symbol	0°C	25°C	75°C	Units
V_{out} "1" $I_L = I_{L"1"}$	V_o "1"	3.0	3.1	3.15	V min.
@ V_{in}		.45	.45	.45	V
V_{out} "1" Threshold $I_L = I_{L"1"}$	V_{oth} "1"	2.5	2.4	2.5	V min.
@ V_{in}		1.1	1.2	1.1	V
V_{out} "0" Threshold $I_L = I_{L"0"}$	V_{oth} "0"	.45	.45	.45①	V max.
@ V_{in}		1.9	1.8	1.7	V
V_{out} "0" $I_L = I_{L"0"}$	V_o "0"	.40	.40	.45①	V max.
@ V_{in}		2.8	2.8	2.8	V

GATES AND FLIP FLOPS (at all operating temperatures)

$I_{in"0"} = 1.33$ mA max. @ $V_{in} = 0V$②③
$I_{L"0"} = 20$ mA (F.O. = 15)
$I_{L"0"} = 10$ mA (F.O. = 7)

$I_{in"1"} = 100\ \mu A$ max. @ $V_{in} = 4.5V$②④
$I_{L"1"} = 1.5$ mA (F.O. = 15)
$I_{L"1"} = .7$ mA (F.O. = 7)

Power per Gate "ON" $I_s = 6.0$ mA max.⑤ [.9 mA per input node, 5.1 mA per output stage]
Power per Gate "OFF" $I_s = 3.0$ mA max.⑤ [1.8 mA per input node, 1.2 mA per output stage]
Circuit Bkdn. "OFF" 7V min. @ $I_s = 5.0$ mA⑤ [3.0 mA per input node, 2.0 mA per output stage]
Input Bkdn. 5.5V min. @ $I_{in} = 1.0$ mA④
Output Leakage Current = 250 μA max. @ $V_{out} = 5.5V$; $V_{in} = 0V$
Output Short Circuit Current = 45 mA max., 10 mA min. @ $V_{out} = V_{in} = 0V$

Propagation Delay $t_{pd} = \frac{t_{on} + t_{off}}{2}$ = 18 nsec max. / = 10 nsec max. (High Speed Version) } F.O. = 1; $C_L = 15$ pf; $T_A = 25°C$⑥

LINE DRIVERS (at all operating temperatures)

$I_{in"0"} = 2.7$ mA max. @ $V_{in} = 0V$③
$I_{L"0"} = 54$ mA (F.O. = 40)
$I_{L"0"} = 32$ mA (F.O. = 24)

$I_{in"1"} = 200\ \mu A$ max. @ $V_{in} = 4.5V$④
$I_{L"1"} = 4.0$ mA (F.O. = 40)
$I_{L"1"} = 2.4$ mA (F.O. = 24)

Power per Gate "ON" $I_s = 12.0$ mA max.⑤ [1.8 mA per input node, 10.2 mA per output stage]
Power per Gate "OFF" $I_s = 6.0$ mA max.⑤ [3.6 mA per input node, 2.4 mA per output stage]
Circuit Bkdn. "OFF" 7V min. @ $I_s = 10.0$ mA⑤ [6.0 mA per input node, 4.0 mA per output stage]
Input Bkdn. 5.5 V_{min} @ $I_{in-} = 1.5$ mA④
Output Leakage Current = 300 μA max. @ $V_{out} = 5.5V$; $V_{in} = 0$
Output Short Circuit Current = 90 mA max., 20 mA min. @ $V_{out} = V_{in} = 0V$

Propagation Delay $t_{pd} = \frac{t_{on} + t_{off}}{2}$ = 18 nsec max. @ F.O. = 1; $C_L = 100$ pf; $T_A = 25°C$⑥

LAMP DRIVERS (at all operating temperatures)

$I_{in"0"} = 2.7$ mA max. @ $V_{in} = 0V$③
$I_{L"0"+} = 60$ mA

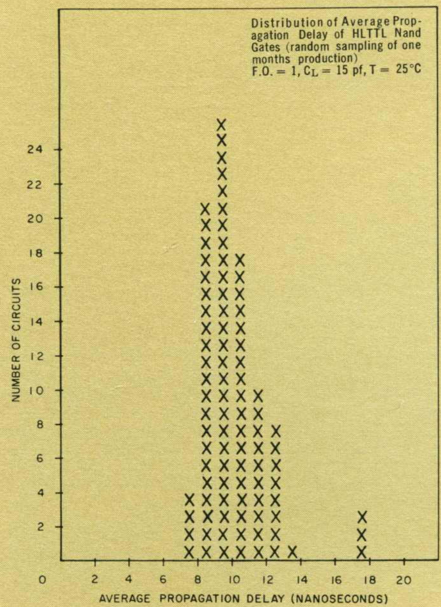
$I_{in"1"} = 200\ \mu A$ max @ $V_{in} = 4.5V$④
$I_{L"1"} = .5$ mA into output terminal

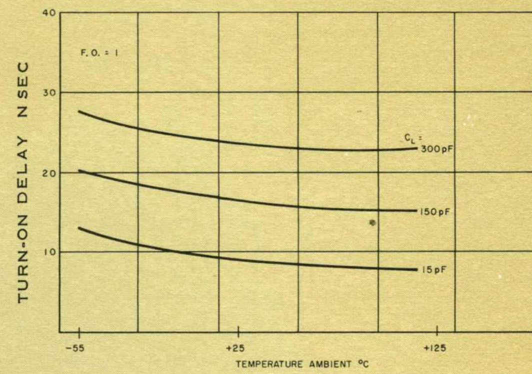
Power per Gate "ON" $I_s = 12.0$ mA max.⑤ [1.8 mA per input node, 10.2 mA per output stage]
Power per Gate "OFF" $I_s = 6.0$ mA max.⑤ [3.6 mA per input node, 2.4 mA per output stage]
Circuit Bkdn. "OFF" 7V min. @ $I_s = 10.0$ mA⑤ [6.0 mA per input node, 4.0 mA per output stage]
Input Bkdn. 5.5V_{min} @ $I_{in-} = 1.5$ mA④
Output Leakage Current = 300 μA max. @ $V_{out} = 8V$; $V_{in} = 0V$

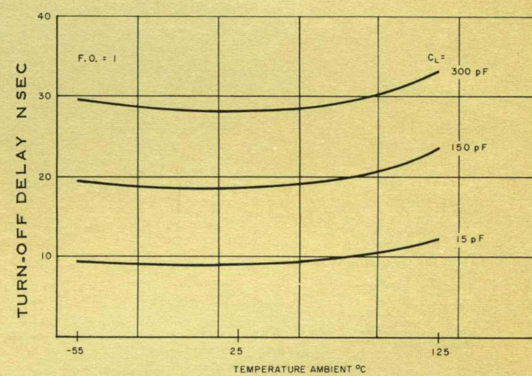
NOTES:
① .6V max. for lamp drivers
② One unit load
③ Other inputs @ 4.5V
④ Other inputs ground or open
⑤ Dependent on ckt function
⑥ Unused input @ logic "1" = 3.5V

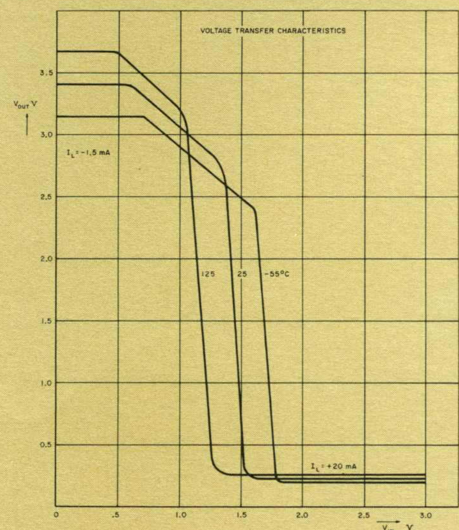
Transitron

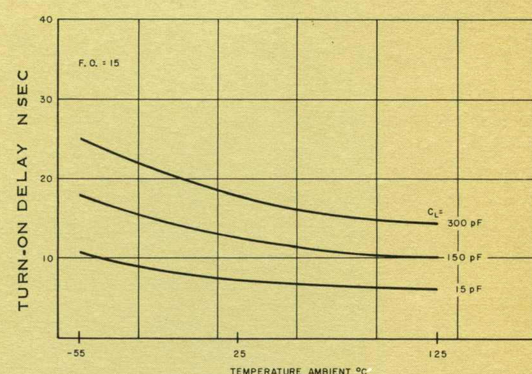
HLTTL Characteristics of

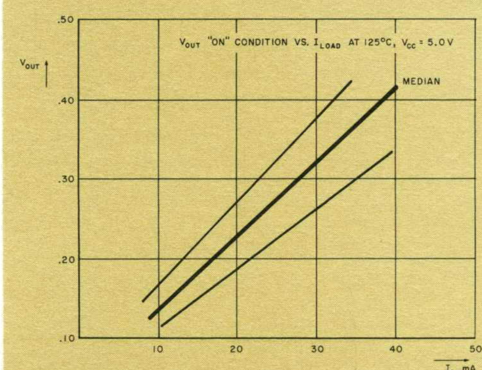


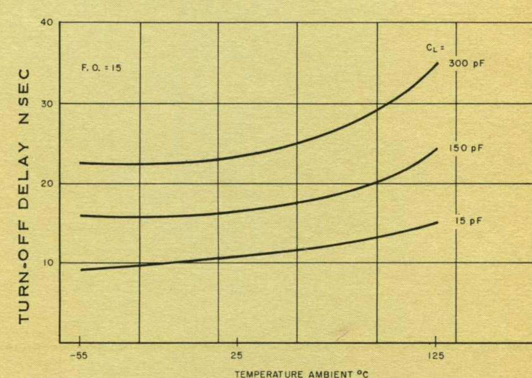


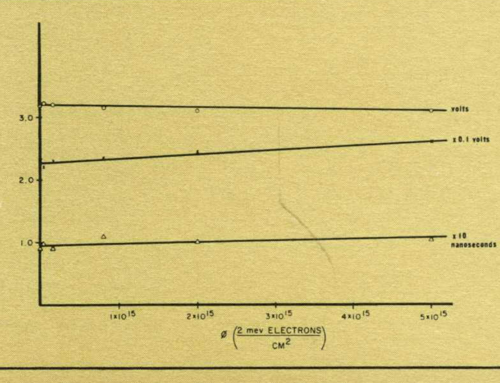












T = 25°C

△ t_{pd} (average propagation delay) F.O. = 1, C_L = 15 pf

X Output on state voltage at 20 ma, load current

○ Output off state voltage, V_{IN} = 0.8 volts, I_{OUT} = 2 ma

After $\phi = 5 \times 10^{15} \frac{2 \text{ Mev electrons}}{cm^2}$ (equivalent to approximately 2×10^{14} pile neutrons/cm^2) over 90% of circuits are still functional over temperature range of 0°C to 125°C under loading conditions of F.O. 7 with no sacrifice of noise margin

Transitron

HLTTL Commercial Series Integrated Circuits

High Level Transistor Transistor Logic has already become established as the state-of-the-art for saturated switching in military and industrial applications.

In developing a low-cost version of the premium military series, Transitron has placed HLTTL performance within practical reach for the designer of commercial equipment.

It should be emphasized that the cost reductions involved did not involve the chips themselves, which are actually identical to those used in the premium series. The savings lie primarily in the packaging and in the use of conservative specifications.

All units are packaged in an economical but extremely reliable hermetic, 8-lead TO-5 can, and are assembled by means of automated, high-volume production techniques previously perfected in transistor manufacturing operations.

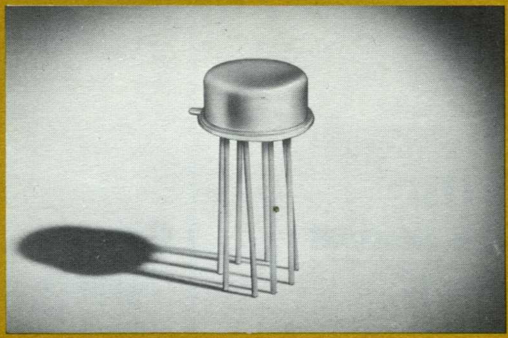
The use of performance specifications which are well within the design limits of the circuit chips has resulted in high production yields and has reduced the requirement for extensive testing.

With their outstanding combination of good fanout, speed, noise protection and capacitive driving capability, these circuits constitute the most flexible and logically powerful line ever introduced for commercial use.

Listing of Transitron Commercial Circuits

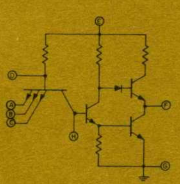
Type Number	Circuit Description
TNG3031	Single 4 input Nand/Nor Gate
TNG4131	Single 3 input Nand/Nor Gate, expandable
TNG4031	Single 4 input AND Expander Gate
TNG5131	Single 2 input Nand/Nor Gate, Expandable for OR function
TNG5031	Dual 2 OR Expander Gates
TNG3131	Dual 2 input Nand/Nor Gate
TNG3231	Dual 2 input Nand/OR Gate
TNG3331	Single 4 input Line Driver
TNG3431	Single 4 input Lamp Driver
TFF3031	Gated 2 phase flip-flop
TFF3131	Master Slave J-K flip-flop, 1 set
TFF3231	Charge Storage J-K flip-flop

Transitron
Commercial Circuits



SINGLE 3-INPUT NAND/NOR GATE EXPANDABLE

TNG 4131

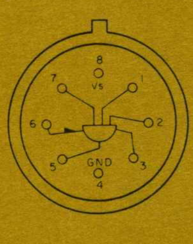


+LOGIC

$F = \overline{A \cdot B \cdot C \cdots}$

−LOGIC

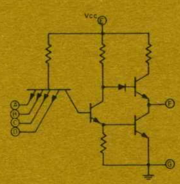
$F = \overline{A + B + C + \cdots}$



PIN CONNECTION (TO-5)	
Circuit Letter	Pin Number
A	1
B	2
C	7
D	3
E	8
F	5
G	4
H	6

SINGLE 4-INPUT NAND/NOR GATE

TNG 3031

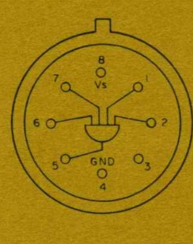


+LOGIC

$F = \overline{A \cdot B \cdot C \cdot D}$

−LOGIC

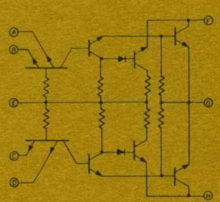
$F = \overline{A + B + C + D}$



PIN CONNECTION (TO-5)	
Circuit Letter	Pin Number
A	1
B	2
C	6
D	7
E	8
F	5
G	4

DUAL 2-INPUT NAND/NOR GATE

TNG 3131



+LOGIC

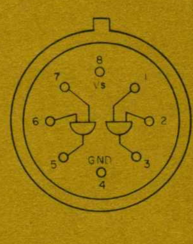
$F = \overline{A \cdot B}$

$H = \overline{C \cdot D}$

−LOGIC

$F = \overline{A + B}$

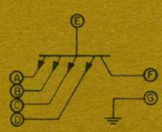
$H = \overline{C + D}$

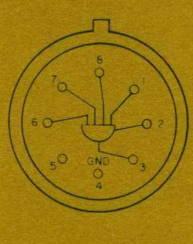


PIN CONNECTION (TO-5)	
Circuit Letter	Pin Number
A	1
B	2
C	6
D	7
E	8
F	3
G	4
H	5

4-INPUT AND EXPANDER

TNG 4031

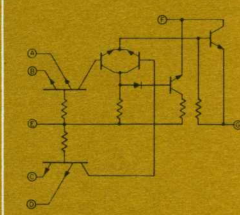




PIN CONNECTION (TO-5)	
Circuit Letter	Pin Number
A	1
B	8
C	6
D	7
E	2
F	3
G	4

DUAL 2-INPUT OR GATE

TNG 3231

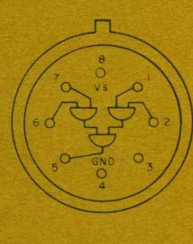


+LOGIC

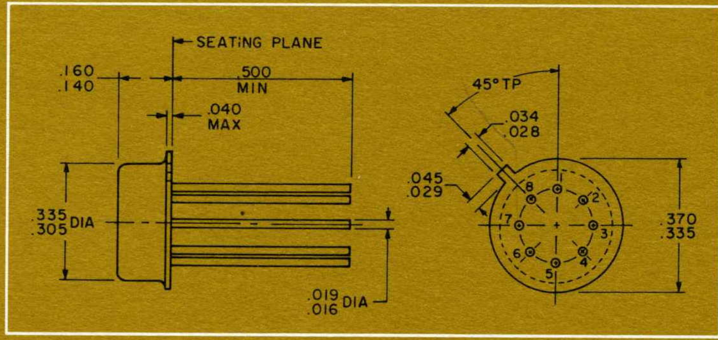
$F = (A \cdot B) + (C \cdot D)$

−LOGIC

$F = \overline{(A + B) \cdot (C + D)}$

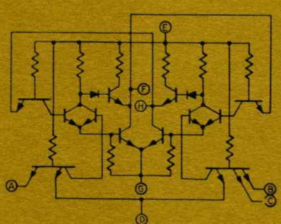


PIN CONNECTION (TO-5)	
Circuit Letter	Pin Number
A	1
B	2
C	6
D	7
E	8
F	5
G	4



GATED 2-PHASE FLIP-FLOP

TFF 3031



+LOGIC

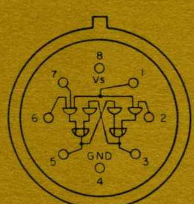
$F=(\bar{A}+\bar{D})\cdot\bar{H}$

$H=(\bar{B}+\bar{C}+\bar{D})\cdot\bar{F}$

-LOGIC

$F=(\bar{A}\cdot\bar{D})+\bar{H}$

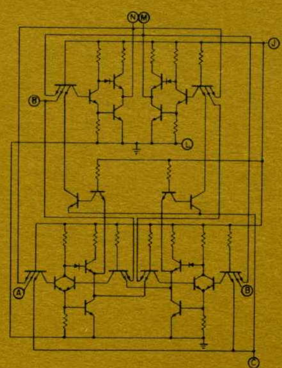
$H=(\bar{B}\cdot\bar{C}\cdot\bar{D})+\bar{F}$

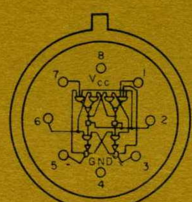


PIN CONNECTION (TO-5)	
Circuit Letter	Pin Number
A	2
B	6
C	7
D	1
E	8
F	3
G	4
H	5

MASTER-SLAVE J-K FLIP-FLOP

TFF 3131

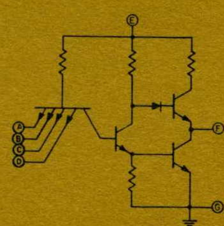




PIN CONNECTION (TO-5)	
Circuit Letter	Pin Number
A	1
B	7
C	6
J	8
L	4
M	5
N	3
R	2

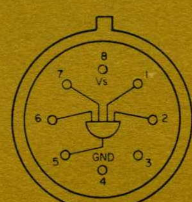
SINGLE 4-INPUT LINE DRIVER (FANOUT 20)

TNG 3331



+LOGIC $F=\overline{A\cdot B\cdot C\cdot D}$

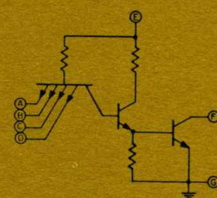
-LOGIC $F=\overline{A+B+C+D}$



PIN CONNECTION (TO-5)	
Circuit Letter	Pin Number
A	1
B	2
C	6
D	7
E	8
F	5
G	4

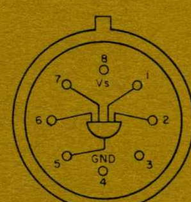
SINGLE 4-INPUT LAMP DRIVER

TNG 3431



+LOGIC $F=\overline{A\cdot B\cdot C\cdot D}$

-LOGIC $F=\overline{A+B+C+D}$



PIN CONNECTION (TO-5)	
Circuit Letter	Pin Number
A	1
B	2
C	6
D	7
E	8
F	5
G	4

Transitron
Commercial HLTTL Series

$T_A = 15$ to $55°C$

Gates and Flip-Flops
F.O. = 7
Line Drivers
F.O. = 20
Lamp Driver
$I_L = 50$ mA

RATINGS

Voltage	Min.	Typ.	Max.
Supply voltage			7.0V
Supply operating voltage	4.5	5.0	6.0V
Input voltage			5.0V
Output voltage			5.5V

Temperature and Power	Min.	Typ.	Max.
Operating	+15*		+55°C
Storage	−55		+125°C
Power per gate, 50% duty cycle, $V_{cc} = 5.0V$		15mW	

ELECTRICAL CHARACTERISTICS

($V_{cc} = 5.0V$.; $T_A = 25°C$)	Symbol	Value	Units
V_{out} "1" $I_L = I_{L"1"}$	V_o "1"	2.6	V min.
@ V_{in}		.45	V
V_{out} "1" threshold $I_L = I_{L"1"}$	V_{oth} "1"	2.5	V min.
@ V_{in}		1.0	V
V_{out} "0" threshold $I_L = I_{L"0"}$	V_{oth} "0"	.50①	V max.
@ V_{in}		2.0	V
V_{out} "0" $I_L = I_{L"0"}$	V_o "0"	.50①	V max.
@ V_{in}		2.8	V

GATES AND FLIP FLOPS

$I_{in"0"} = 1.33$ mA max. @ $V_{in} = 0V$②③
$I_{L"0"} = 10$ mA

$I_{in"1"} = 200$ μA max. @ $V_{in} = 3.0V$②④
$I_{L"1"} = 1.5$ mA

Power per Gate "ON" $I_s = 6.0$ mA⑤ [.9 mA per input node, 5.1 mA per output stage]
Power per Gate "OFF" $I_s = 3.0$ mA⑤ [1.3 mA per input node, 1.2 mA per output stage]
Circuit Bkdn. "OFF" 7V min. @ $I_s = 5.0$ mA⑤ [3.0 mA per input node, 2.0 mA per output stage]
Input Bkdn. 5.0V min. @ $I_{in} = 1.0$ mA④
Output Leakage 250 μA max. @ $V_{out} = 5.5V$ $V_{in} = 0V$
Output Short Ckt. Current = 45 mA max., 10 mA min. @ $V_{out} = V_{in} = 0V$
Propagation Delay $t_{pd} = \frac{t_{on} + t_{off}}{2} = 25$ nsec max. F.O. = 1 $C_L = 15$ pf⑥

LINE DRIVERS

$I_{in"0"} = 2.7$ mA max. @ $V_{in} = 0V$③
$I_{L"0"} = 27$ mA

$I_{in"1"} = 400$ μA max. @ $V_{in} = 3.0V$④
$I_{L"1"} = 4.0$ mA

Power per Gate "ON" $I_s = 12.0$ mA⑤ [1.8 mA per input node, 10.2 mA per output stage]
Power per Gate "OFF" $I_s = 6.0$ mA⑤ [3.6 mA per input node, 2.4 mA per output stage]
Circuit Bkdn. "OFF" 7V @ $I_s = 10.0$ mA⑤ [6.0 mA per input node, 4.0 mA per output stage]
Input Bkdn. 5.0V @ $I_{in} = 1.5$ mA④
Output Leakage 300 μA max. @ $V_{out} = 5.5V$, $V_{in} = oV$
Short Ckt. Current = 90 mA max., 20 mA min. @ $V_{out} = V_{in} = 0V$
Propagation Delay $t_{pd} = \frac{t_{on} + t_{off}}{2} = 25$ nsec max. F.O. = 1 $C_L = 100$ pf⑥

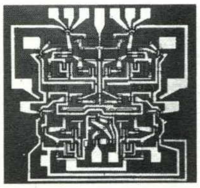
LAMP DRIVERS

$I_{in"0"} = 2.7$ mA max. @ $V_{in} = 0V$③
$I_{L"0"} = 50$ mA

$I_{in"1"} = 400$ μA max. @ $V_{in} = 3.0V$④
$I_{L"1"} = .5$ mA into output terminal

Power per Gate "ON" $I_s = 12.0$ mA⑤ [1.8 mA per input node, 10.2 mA per output stage]
Power per Gate "OFF" $I_s = 6.0$ mA⑤ [3.6 mA per input node, 2.4 mA per output stage]
Ckt. Bkdn. "OFF" 7V @ $I_s = 10.0$ mA⑤ [6.0 mA per input node, 4.0 mA per output stage]
Input Bkdn. 5.0V @ $I_{in} = 1.5$ mA④
Output Leakage 300 μA max. @ $V_{out} = 7.0V$, $V_{in} = 0V$

NOTES:
① .6V max. for lamp drivers
② One unit load
③ Other inputs @ 3.0V
④ Other inputs ground or open
⑤ Dependent on circuit function
⑥ Unused inputs @ Logic "1" = 3.5V



Transitron

Quality Assurance and Reliability

Transitron's Quality Assurance and Reliability Groups report to a Corporate Director who is responsible directly to the President for all aspects of quality assurance and reliability. Included in these groups are the key functions of incoming inspection, process control and outgoing inspection as well as the support functions such as the standards laboratories, life and environmental test facilities, and equipment calibration and certification. All functions operate according to procedures defined in Transitron's Quality Assurance and Reliability Manual.

Quality Assurance, being fully aware that quality and reliability must be inherent in a finished device, assists engineering in evaluation of new integrated circuit products and then works with and complements the manufacturing line in the production of integrated circuits. This effort begins with the quality assurance participation in generation and approval of both manufacturing procedures and engineering changes thereto, and is implemented by the more than forty control and inspection stations on the Transitron HLTTL production line. These stations include lot acceptance of incoming material, in-process control points, and 100% inspections (particularly visual inspections on metallizations and internal bonds). While all stations generate data for analysis and subsequent product improvement, unprecedented amounts of data are generated at several of the process control stations due to the inherent complexity of the circuits. For example, at one control station a sample of 10 circuits is taken several times a day and over 60 parameters per circuit are recorded and control chart plotted.

Further data pertinent to Transitron's HLTTL integrated circuits is generated by the reliability monitoring of the production line. This program samples production over successive six week periods, subjecting parts of the sample to the following tests consisting of:

1. Operating life at 125°C for 1000 hours; consisting of 500 hours in a ring counter, 500 hours in steady state on-off operation.
2. High temperature storage life at 200°C for 1000 hours.
3. Environmental tests per MIL-STD-750.

Subgroup I
- Solderability
- Temperature
- Moisture resistance

Subgroup II
- Terminal Strength

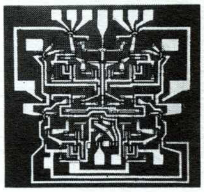
Subgroup III
- Shock
- Vibration fatigue
- Vibration variable frequency
- Constant acceleration

Subgroup IV
- Salt Atmosphere

To cope with the large volume of data anticipated from the integrated circuit operation, as well as the many other semiconductor operations within the Company, the Reliability Group has developed an extensive set of computer programs. The programs include failure rates and confidence limits, averages, standard deviations, frequency distributions and parameter delta shift analysis.

By using the computer programs to analyze both the process control data and the finished device reliability data, excellent information and direction can be fed back to the engineering and manufacturing groups in a timely fashion. The classic failure analysis — corrective action feedback cycle is greatly enhanced by the sophisticated data analysis techniques of examining parameter change distributions, often more informative than an occasional "end-point" failure.

Thus, Transitron's Quality Assurance and Reliability effort begins at the engineering level, monitors the production line, tests the finished product, and analyzes the total data accumulation to provide direction for maintenance of desired quality and reliability levels as well as for future product improvements.



Future

New packaging concepts and larger circuit functions can be expected to play a major role in our digital integrated circuit business.

As indicated at the beginning of this brochure, HLTTL is only the beginning. Other advanced digital families, memory circuits and linear circuits are certainly in Transitron's future. The success of the present production concentration on HLTTL is expected to be duplicated again and again, in these other areas in coming years.

Transitron electronic corporation

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Wherever there's electronics... there's Transitron

Transitron electronic corporation, 168 Albion Street, Wakefield, Massachusetts 01881

Bulletin TNG-1

Printed in U. S. A.

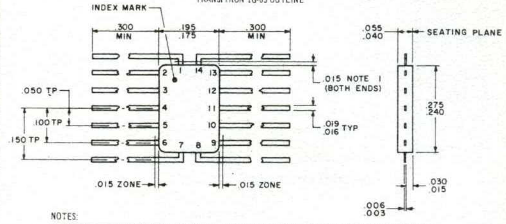
HLTTL NON-INVERTING GATES

This series of HLTTL Non-Inverting "AND" and "OR" gates have been added as basic elements of Transitron's planar epitaxial high speed HLTTL family of integrated circuits characterized by very low propagation delay and high capacitive driving capability. The circuits were designed primarily for application in systems where simplification and higher operating speeds are of prime importance since two levels of logic are replaced by one.

The unique design of this circuit series provides for (1) extremely sharp voltage transfer characteristics which result in noise margins in excess of 1.3 volts typically, (2) reduction of supply current during switching and (3) typical propagation delay times of 12 nanoseconds with 15 pf load and fanout of 1. Non-inverting high level driving capability is provided by the TNG6522 and TNG 6524. Some of the circuits offer the possibility of controlling the output transients through the use of an external capacitor between the output and base of the output transistor. This is particularly useful in applications where length of interconnections would result in excessive noise coupling.

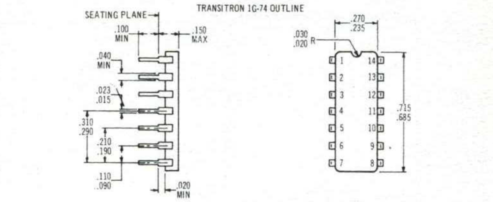
Expansion of logic capability is provided through the use of any of 3 expander gates. Use of these expanders requires interconnection of only one circuit terminal which provides for optimized pin utilization on both the gate and expander.

TRANSITRON 1G-65 OUTLINE

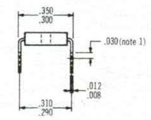


NOTES:
1. LEAD WIDTH, LEAD THICKNESS AND IRREGULARITIES IN BODY OUTLINE ARE NOT CONTROLLED IN THE ZONE.
2. THE NUMBERS SHOWN ON THE BODY DESIGNATE LEAD POSITIONS. A DEVICE MAY OMIT ONE OR MORE OF THE LEADS SHOWN, BUT ALL LEADS PRESENT MUST BE IDENTIFIED ON THE CONNECTION DIAGRAM BY MEANS OF THE LEAD-POSITION NUMBERS.
3. LEADS SHALL BE LOCATED WITHIN 0.005 OF TRUE POSITION. LEAD LOCATION DIMENSIONS ALSO APPLY TO CORRESPONDING LEADS ON THE OPPOSITE SIDES OF BOTH CENTERLINES OF THE BODY. LEAD LOCATION SHALL BE MEASURED WITHIN 0.030" OF SIDES OF BODY (OR EXTENSION OF SIDES).
4. DETAILED DRAWING 1G-65 IS AVAILABLE UPON REQUEST.

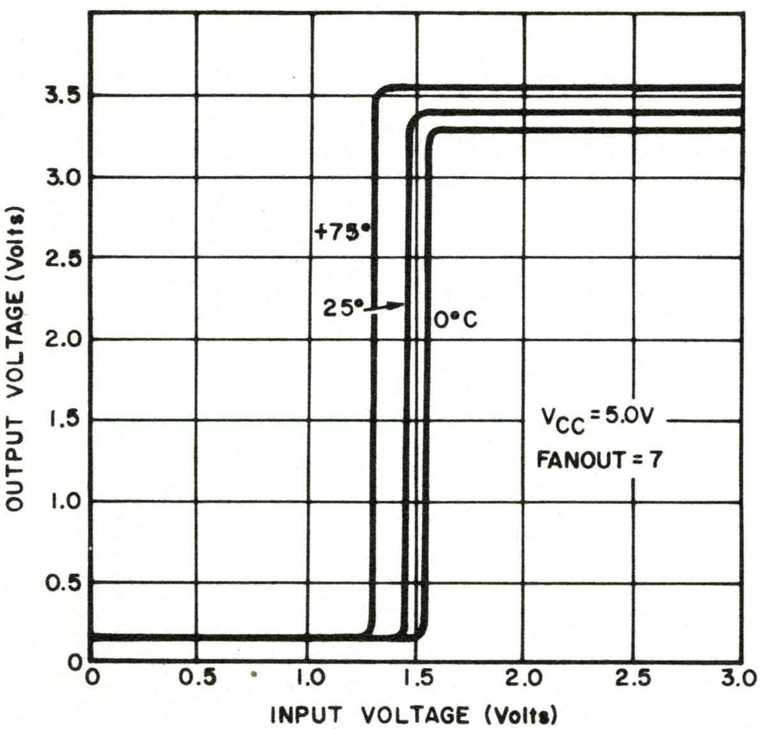
TRANSITRON 1G-74 OUTLINE



NOTES:
1. LEAD LOCATIONS SHALL BE MEASURED WITHIN THIS ZONE.
2. THE NUMBERS SHOWN ON THE BODY DESIGNATE LEAD POSITIONS. A LEAD SHALL BE IDENTIFIED BY MEANS OF ITS LEAD-POSITION NUMBER.
3. DETAILED DRAWING #1G-74 IS AVAILABLE UPON REQUEST.



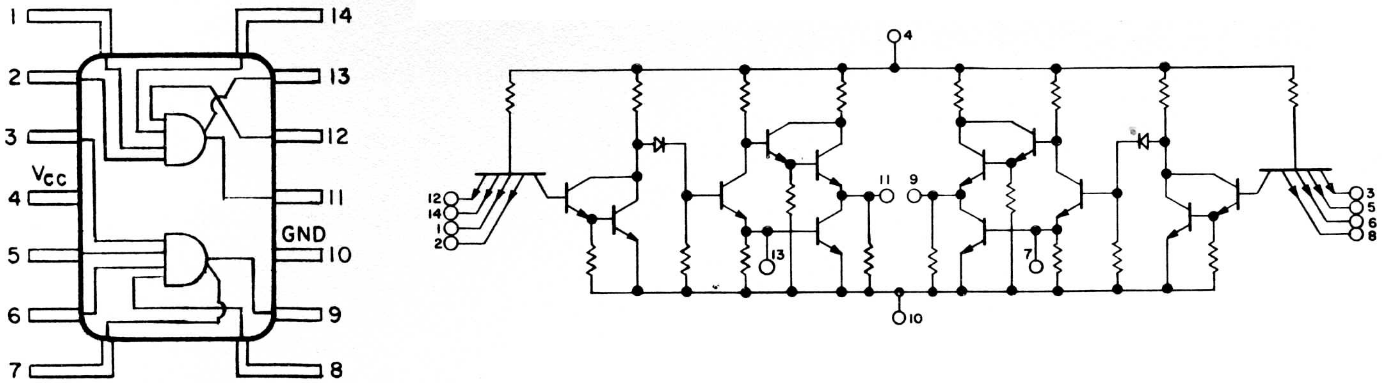
TYPICAL VOLTAGE TRANSFER CHARACTERISTICS



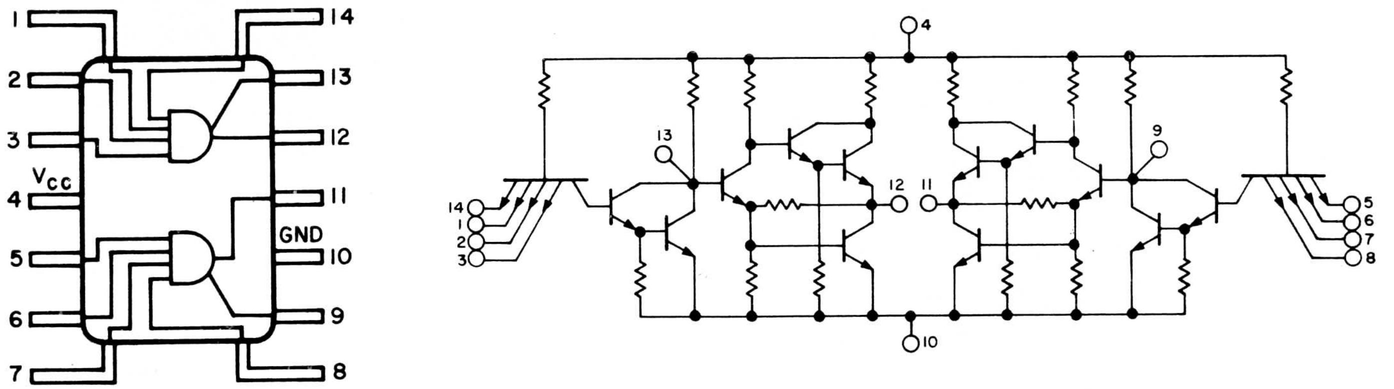
ELEMENTS

(1) TNG 6222 and 6224	Dual 4 input AND Gate with Transient control
(2) TNG 6252 and 6254	Expandable Dual 4 input AND Gate
(3) TNG 6262 and 6264	Expandable Dual 3 input AND Gate with Transient Control
(4) TNG 6522 and 6524	Expandable 4 input Driver Gate with Transient Control
(5) TNG 7252 and 7254	Expandable Dual 2 + 2 input OR Gate
(6) TNG 7712	8 + 3 input Expander Gates
(7) TNG 7812	4 + 4 + 3 input Expander Gate
(8) TNG 7912	Dual 2 + 3 input Expander Gates

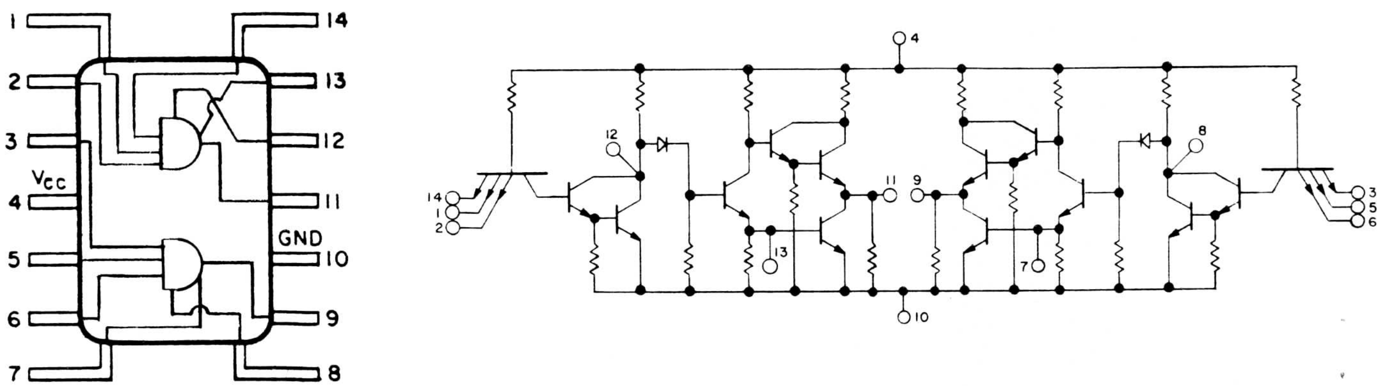
TNG 6222 / 6224



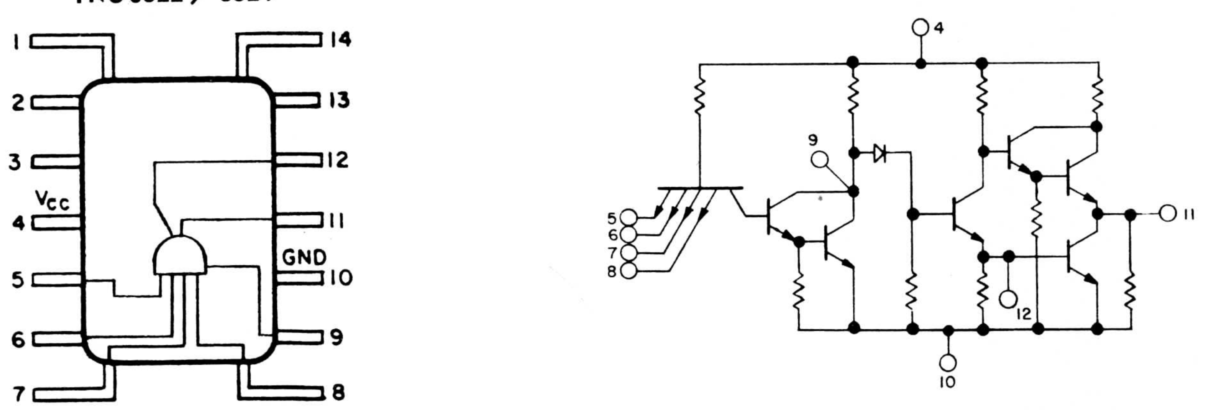
TNG 6252 / 6254



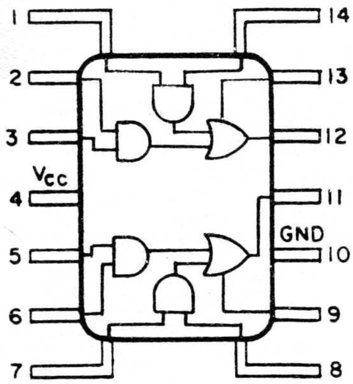
TNG 6262 / 6264

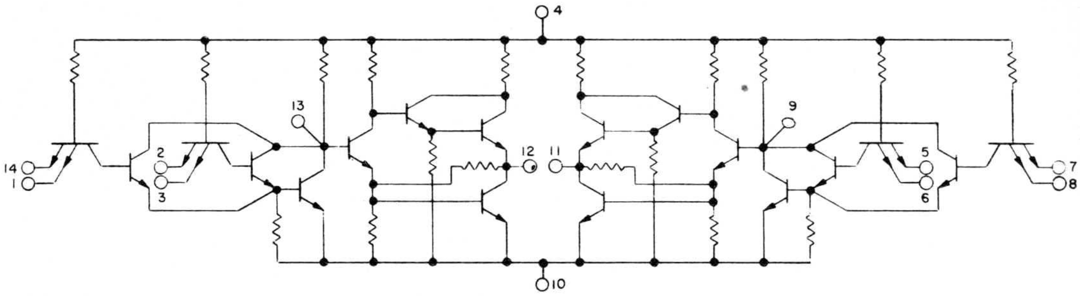


TNG 6522 / 6524

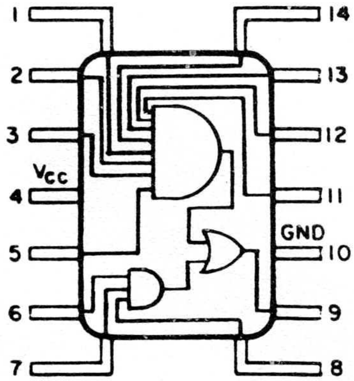


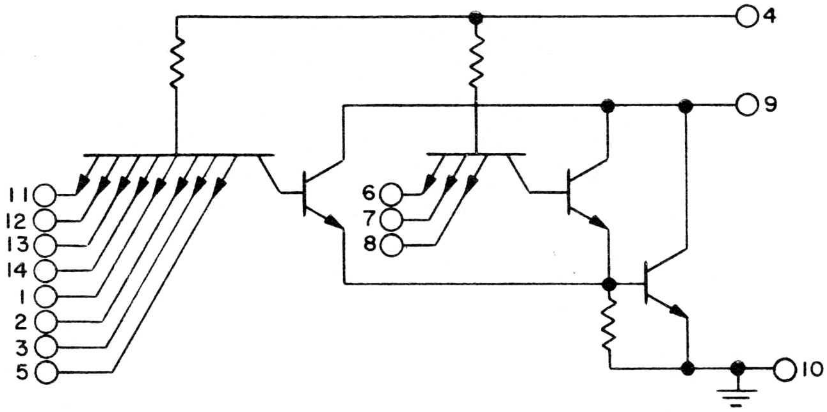
TNG 7252 / 7254



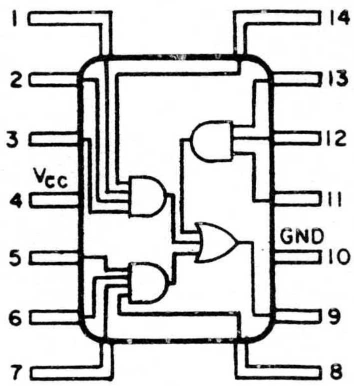


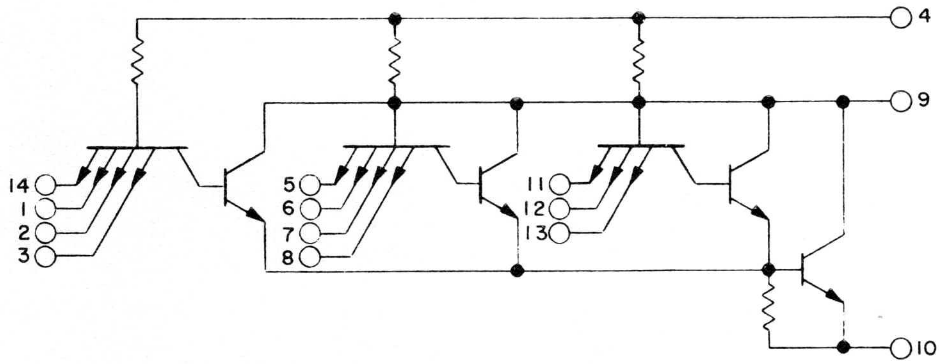
TNG 7712



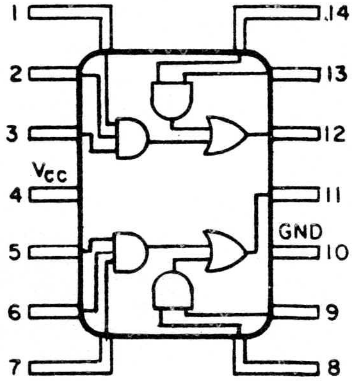


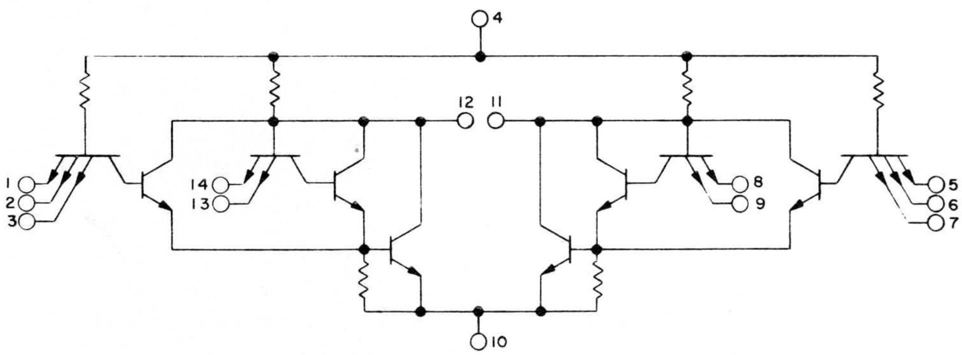
TNG7812





TNG 7912





RATINGS

VOLTAGE	Min	Typ	Max	Temperature and Power	Min	Typ	Max
Supply Voltage			7.0 V	Operating Temperature	0		+75°C
Supply Operating	4.5	5.0	6.0 V	Storage Temperature	−65		+200°C
Input Voltage			5.5 V	Thermal Gradient Junction – Air			0.3°C/mW
Output Voltage			5.0 V	Thermal Gradient Junction – Case			0.1°C/mW
				Power Dissipation per Gate 50% Duty Cycle V_{CC} = 5.0 V		40 mW	

ELECTRICAL CHARACTERISTICS

CIRCUIT PARAMETER (V_{CC} = 5.0 V)	Values @ Ambient Temperature				
	Symbol	0°C	+25°C	+75°C	Units
V_{OUT} "I" Threshold, $I_L = I_L$ "I"	V_{OTH} "I"	3.1	3.1	3.1	V min
@ V_{IN} =		1.90	1.80	1.70	V
V_{OUT} "O" Threshold, $I_L = I_L$ "O"	V_{OTH} "O"	0.40	0.40	0.40	V max
@ V_{IN} =		1.30	1.20	1.10	V

GATES (At All Operating Temperatures)

I_{IN} "O" = 1.33 mA max @ V_{IN} = 0 V ① ②

I_{IN} "I" = 100 μA max @ V_{IN} = 4.5 V ① ③

I_L "O" = 20 mA (F.O. = 15)

I_L "I" = 1.5 mA (F.O. = 15)

I_L "O" = 10 mA (F.O. = 7)

I_L "O" = 0.7 mA (F.O. = 7)

Power Per Gate "ON", I_S = 10.9 mA max ④ [1.4 mA Per Input Node, 9.5 mA Per Output Stage]
Power Per Gate "OFF", I_S = 9.4 mA max ④ [0.9 mA Per Input Node, 8.5 mA Per Output Stage]
Circuit Breakdown "ON", 7.0 V min @ I_S = 15.5 mA max ④ [2.0 mA Per Input Node, 13.5 mA Per Output Stage]
Circuit Breakdown "OFF", 7.0 V min @ I_S = 13.6 mA max ④ [1.6 mA Per Input Node, 12.0 mA Per Output Stage]
Input Breakdown, 5.5 V min @ I_{IN} = 1.0 mA ③
Output Short Circuit Current = 50.0 mA max, 20 mA min @ V_{OUT} = 0 V, V_{IN} = 4.5 V

Propagation Delay $t_{pd} = \frac{t_{on} + t_{off}}{2}$ = 18 nsec max F.O. = 1, C_L = 15 pf, T_A = 25°C ⑤

LINE DRIVERS (At All Operating Temperatures)

I_{IN} "O" = 1.33 mA @ V_{IN} = 0 V ① ②

I_{IN} "I" = 100 μA max @ V_{IN} = 4.5 V ① ③

I_L "O" = 54.0 mA (F.O. = 40.0)

I_L "I" = 4.0 mA (F.O. = 40.0)

I_L "O" = 32.0 mA (F.O. = 24.0)

I_L "I" = 2.4 mA (F.O. = 24.0)

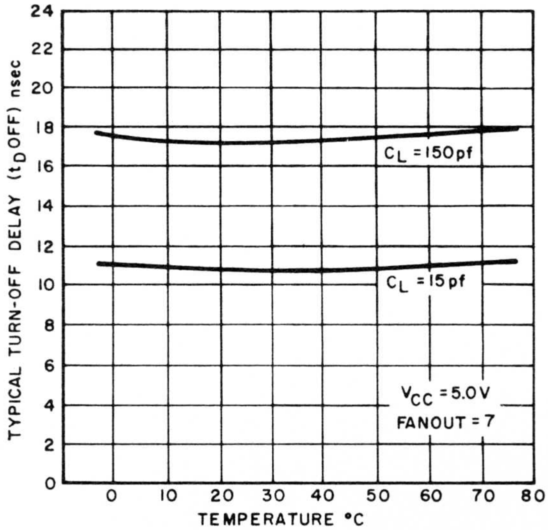
Power Per Gate "ON", I_S = 23.1 mA ④ [1.4 mA Per Input Node, 21.7 mA Per Output Stage]
Power Per Gate "OFF", I_S = 21.4 mA ④ [0.9 mA Per Input Node, 20.5 mA Per Output Stage]
Circuit Breakdown, "ON", 7.0 V min @ I_S = 35.2 mA ④ [2.0 mA Per Input Node, 33.2 mA Per Output Stage]
Circuit Breakdown "OFF", 7.0 V min @ I_S = 32.6 mA ④ [1.6 mA Per Input Node, 31 mA Per Output Stage]
Input Breakdown 5.5 V min @ I_{IN} = 1.0 mA ③
Output Short Circuit Current = 100 mA max, 40.0 mA min @ V_{OUT} = 0 V, V_{IN} = 4.5 V

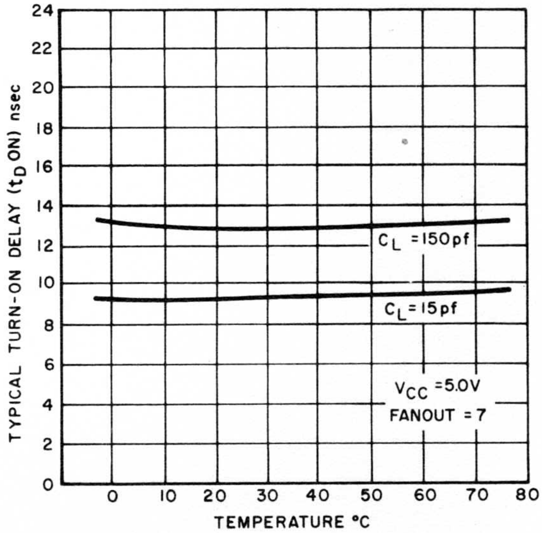
Propagation Delay $t_{pd} = \frac{t_{on} + t_{off}}{2}$ = 18.0 nsec max @ F.O. = 1.0, C_L = 100 pf, T_A = 25°C ⑤

NOTES:

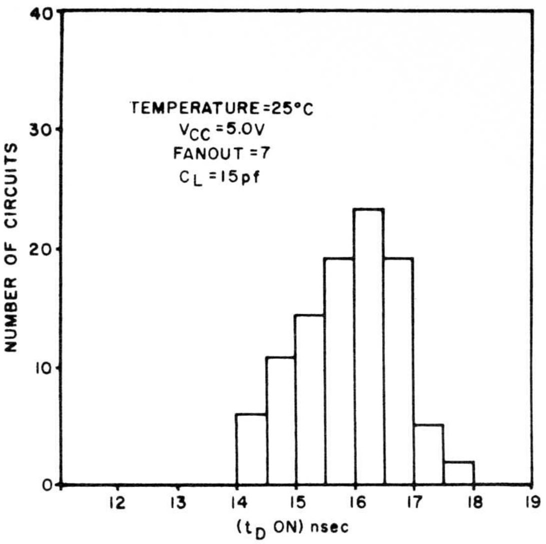
① One Unit Load
② Other Inputs @ 4.5 V
③ Other Inputs Ground Or Open
④ Dependent on CKT Function
⑤ Unused Inputs @ Logic "I" = 3.5 V

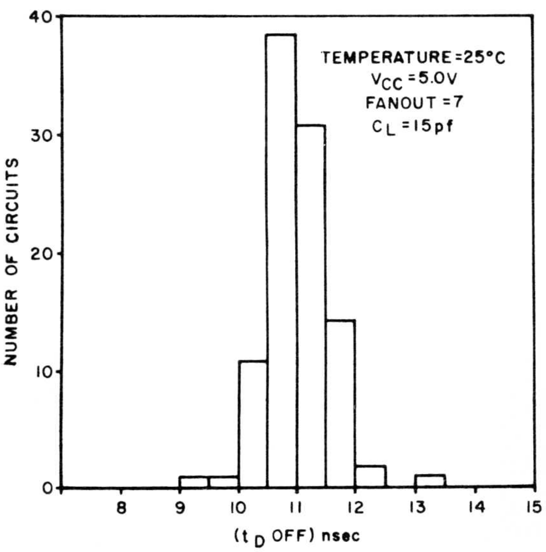
TURN-ON And TURN-OFF DELAY vs. TEMPERATURE For TNG 6252



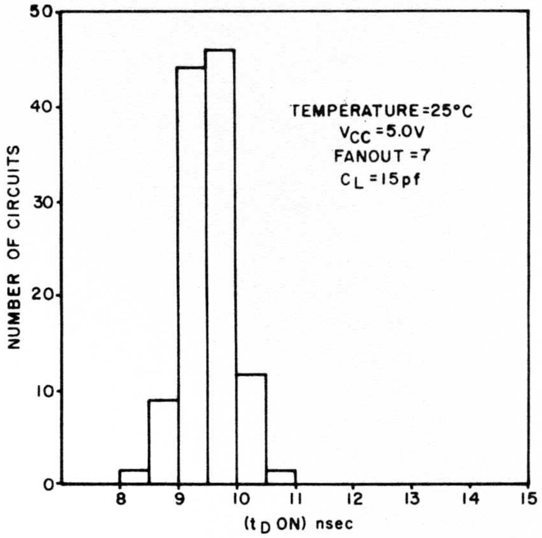


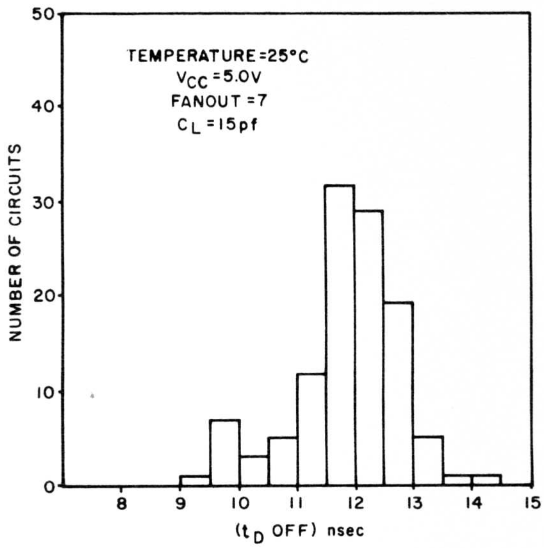
RANDOM SAMPLING TNG 6262





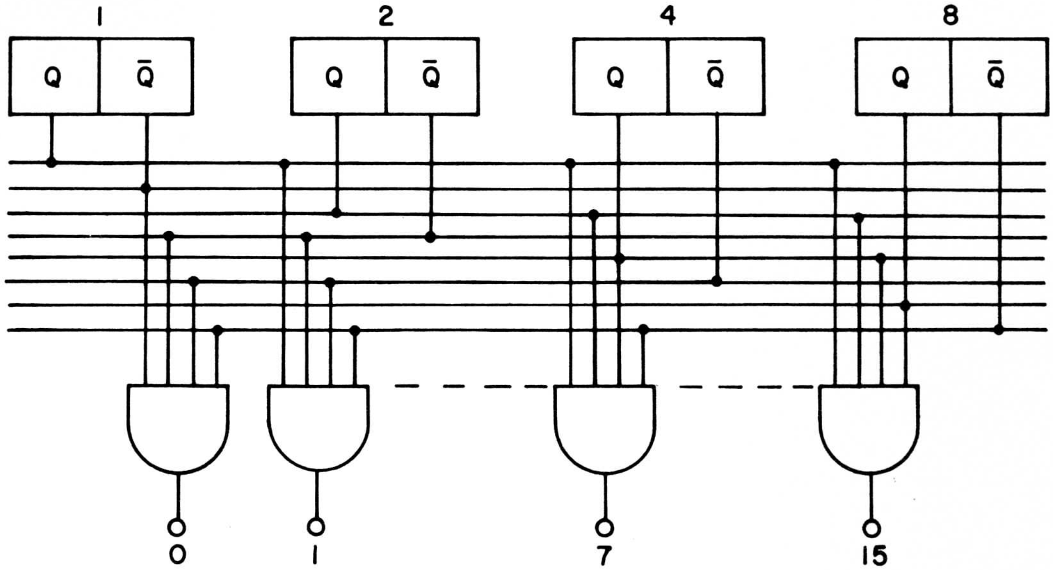
RANDOM SAMPLING TNG 6252





APPLICATION

DECODING



8 TNG 6252
8 Unit Loads per Register Side
1 Propagation Delay

ALTERNATIVES USING ONLY INVERTING GATES

16 TNG 4418	8 Unit Loads per Register Side,	1 Propagation Delay
8 TNG 3114 + 4 TNG 3414	8 Unit Loads per Register Side,	2 Propagation Delays
2 TNG 3414 + 8 TNG 4214	8 Unit Loads per Register Side,	2 Propagation Delays

Use of TNG 6252 Simplifies Design, Reduces Package Count and Maintains High Operating Speed.

Transitron

9/66

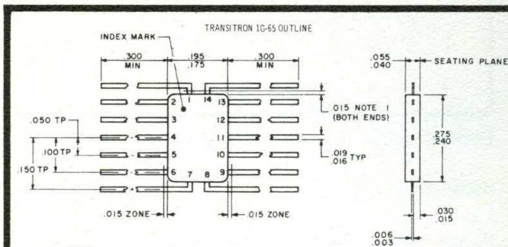
TECHNICAL DATA

HLTTL HIGH SPEED D TYPE FLIP-FLOP

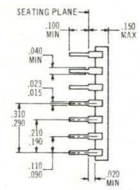
The TFF3512 and TFF 3514 are HLTTL raceless dual rank, high speed "D" type Flip-Flops. The flip-flops complement typically on a 50 megacycle input signal. The high operating speeds which are particularly insensitive to heavy loading have been achieved by dual steering of the second rank flip-flop.

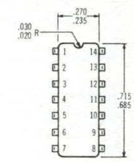
The flip-flop design which utilizes HLTTL technology provides the additional advantages of (1) maximum input gating to simplify the required external gating, (2) elimination of redundant inputs and the necessity to supply the data complement to form the "set" function, (3) connections for holding a logic "1" are incorporated into the flip-flop, (4) a built in clock buffer reduces the clock line driving requirements, (5) typical noise immunity in excess of 1.0 volt and (6) fanouts in excess of 15 with other characteristics and logic levels typical of HLTTL circuitry.

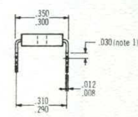
The high speed and extended gating capability of these units make them extremely desirable for arithmetic and general register applications.



NOTES:
1. LEAD WIDTH, LEAD THICKNESS AND IRREGULARITIES IN BODY OUTLINE ARE NOT CONTROLLED IN THE ZONE.
2. THE NUMBERS SHOWN ON THE BODY DESIGNATE LEAD POSITIONS. A DEVICE MAY OMIT ONE OR MORE OF THE LEADS SHOWN, BUT ALL LEADS PRESENT MUST BE IDENTIFIED ON THE CONNECTION DIAGRAM BY MEANS OF THE LEAD-POSITION NUMBERS.
3. LEADS SHALL BE LOCATED WITHIN 0.005 OF TRUE POSITION. LEAD LOCATION DIMENSIONS ALSO APPLY TO CORRESPONDING LEADS ON THE OPPOSITE SIDES OF BOTH CENTERLINES OF THE BODY. LEAD LOCATION SHALL BE MEASURED WITHIN 0.030" OF SIDES OF BODY (OR EXTENSION OF SIDES).
4. DETAILED DRAWING 1G-65 IS AVAILABLE UPON REQUEST.

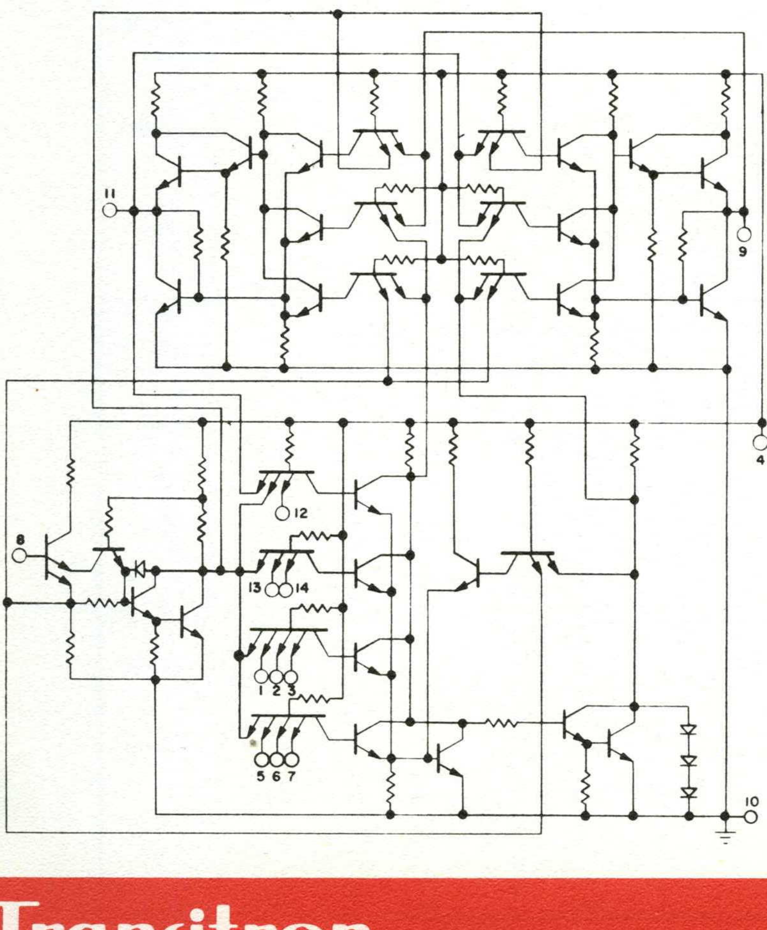




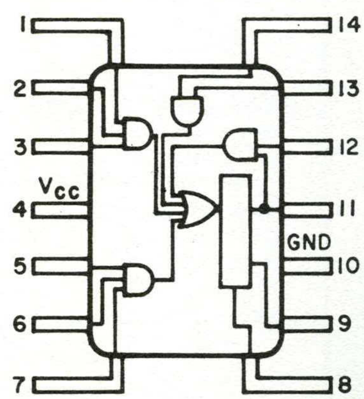


NOTES:
1. LEAD LOCATIONS SHALL BE MEASURED WITHIN THIS ZONE.
2. THE NUMBERS SHOWN ON THE BODY DESIGNATE LEAD POSITIONS. A LEAD SHALL BE IDENTIFIED BY MEANS OF ITS LEAD-POSITION NUMBER.
3. DETAILED DRAWING #1G-74 IS AVAILABLE UPON REQUEST.

CIRCUIT DIAGRAM



PIN CONFIGURATION



TRUTH TABLE:

D	H	Qn	Qn + 1
0	0	ϕ	0
1	0	ϕ	1
0	1	0	0
1	1	0	1
ϕ	1	1	1

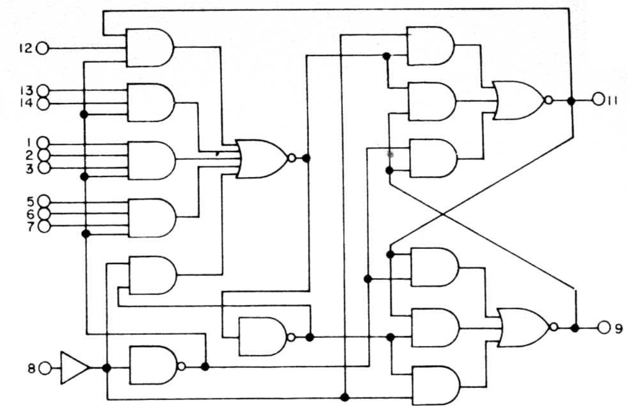
Where:
ϕ = Don't Care
n = Bit Time

Data; $D = D_1 \cdot D_2 \cdot D_3 + D_5 \cdot D_6 \cdot D_7 + D_{13} \cdot D_{14}$

Hold; $H = H_{12}$

(Subscripts = Package Pin Numbers)

LOGIC DIAGRAM



RATINGS

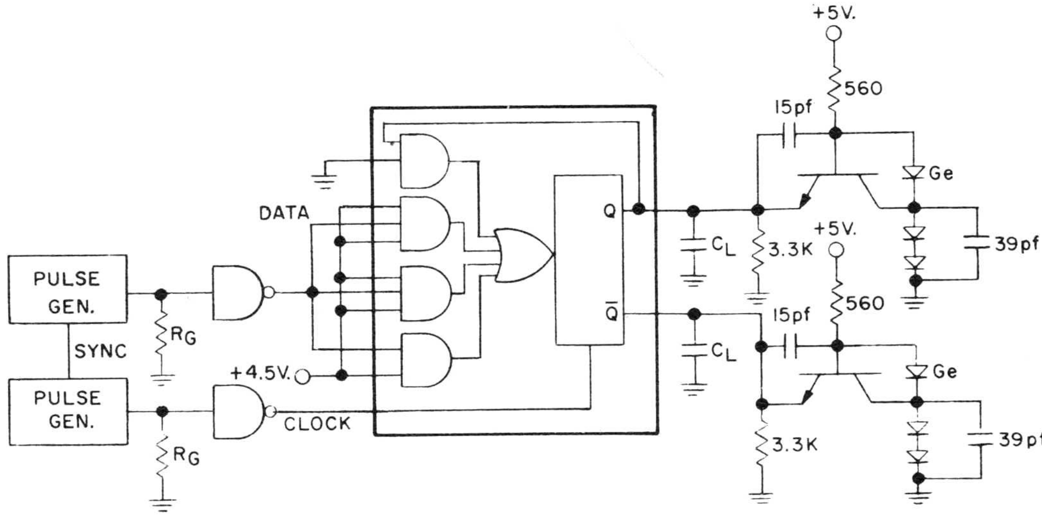
Voltage	Min	Typ	Max
Supply Voltage			7.0 V
Supply Operating	4.5	5.0	6.0 V
Input Voltage			5.5 V
Output Voltage			4.5 V

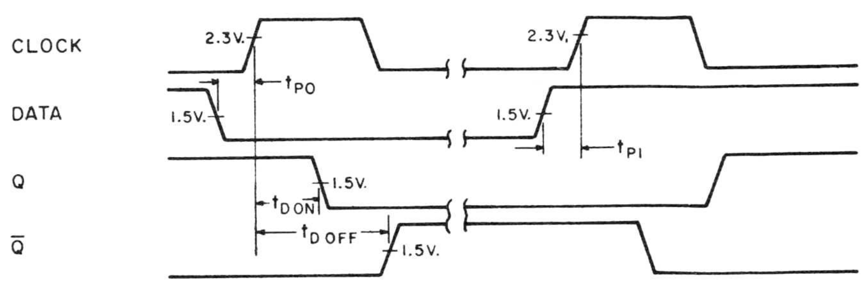
Temperature and Power	Min	Typ	Max
Operating Temperature	0		+75°C
Storage Temperature	−65		+200°C
Thermal Gradient Junction – Air			0.3°C/mW
Thermal Gradient Junction – Case			0.1°C/mW
Power Dissipation, 50% Duty Cycle, V_{CC} = 5.0 V		150 mW	

ELECTRICAL CHARACTERISTICS @ V_{CC} = 5.0 V

	Symbol	Temperature 0°C	+25°C	+75°C	Units
INPUT:					
Input Load Current (Data Inputs)	I_{IN} "0"	1.33	1.33	1.33	mA max
@ V_{IN} and Clock		0	0	0	V
Other Inputs (Q High)		+4.5	+4.5	+4.5	V
Input Load Current (Clock Input)	I_{CIN} "1"	1.0	1.0	1.0	mA max
@ V_{IN} =		+3.5	+3.5	+3.5	V
Other Inputs		Open	Open	Open	
Input Leakage Current (Data Inputs)	I_{IN} "1"	0.1	0.1	0.1	mA max
@ V_{IN} =		+4.5	+4.5	+4.5	V
Other Inputs: (1)		0	0	0	V
(2) (Q High, Clock Low)		+4.5	+4.5	+4.5	V
Input Leakage Current (Clock Input)	I_{CIN} "0"	0.25	0.25	0.25	mA max
@ V_{IN} =		0	0	0	V
Other Inputs		Open	Open	Open	
Input Breakdown Voltage (Data Inputs)	BV_{IN}	5.5	5.5	5.5	V min
@ I_{IN} =		1.0	1.0	1.0	mA max
Other Inputs: (1)		0	0	0	V
(2) (Q High, Clock Low)		Open	Open	Open	
OUTPUT:	I_{SC}	80	80	80	mA max
Output Short Circuit Current		20	20	20	mA min
@ V_{OUT} =		0	0	0	V
Other Output and Clock Input		0	0	0	V
Logic "0" Output Voltage	V_O "0"	0.40	0.40	0.40	V max
@ V_{IN} =		1.30	1.20	1.10	V
I_L "0" (F.O. = 15) =		20	20	20	mA
(F.O. = 7)		10	10	10	mA
Logic "1" Output Voltage	V_O "1"	3.0	3.0	3.0	V min
@ V_{IN} =		1.90	1.80	1.70	V
I_L "1" (F.O. 15) =		20	20	20	mA
(F.O. 7) =		10	10	10	mA
CIRCUIT:					
"0" Power Supply Current	I_S "0"	38	38	38	mA max
@ Inputs and Clock		0	0	0	V
Outputs		Open	Open	Open	
"1" Power Supply Current	I_S "1"	37	37	37	mA max
@ Inputs and Clock		Open	Open	Open	
Outputs		Open	Open	Open	
Breakdown Voltage	BV_S	7.0	7.0	7.0	V min
I_S =		60	60	60	mA
@ V (Inputs and Clock) =		0	0	0	V
Outputs		Open	Open	Open	

SWITCHING TEST CIRCUIT and WAVEFORMS





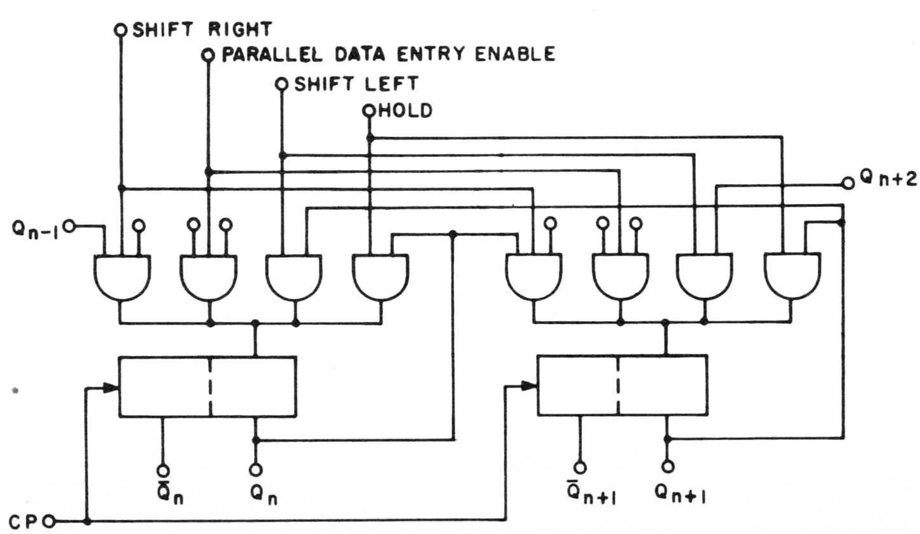
SWITCHING CHARACTERISTICS

(At V_{CC} = 5.0 V, T_A = 25°C, F.O. Load = 7, C_L = 15 pf.)

Turn-on Delay, $t_d$on	15 nsec. max
Turn-off Delay, $t_d$off	25 nsec. max
Preset "0" Time, t_{p0}	8 nsec. max
Preset "1" Time, t_{p1}	6 nsec. max

APPLICATION –

Register Illustrating the Logic Power of the TFF 3512 and TFF 3514



REGISTER, SHIFT LEFT, RIGHT, PARALLEL ENTRY, HOLD

TYPICAL CHARACTERISTICS