

DIGITAL COMPUTERS

RUGGEDIZED QUALITY COMPUTERS WITH MANY OUTSTANDING FEATURES

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COMP 16

COMP 18



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UNICOMP
incorporated

The UniComp computers, Models COMP-16 and COMP-18, are the first of a family of general purpose computers using high speed TTL circuits. UniComp computers offer the flexibility and capabilities normally found in much more expensive hardware. UniComp computers are designed to be placed wherever a general purpose computer is needed — in the factory, the laboratory, the school, the office, in mobile vans, on-board ship, and in adverse environments where reliability and dependability are essential. Unique features allow the COMP-16 and COMP-18 to be easily incorporated into other systems.

GENERAL DESCRIPTION

A list of TYPICAL APPLICATIONS for the UniComp computers is as follows:

- A powerful Stand Alone Computer
- Satellite to Larger Computers
- Scientific calculations
- Process Control
- Communication Switching
- Automation
- Diagnostics
- Data Terminal
- Batch Processor
- Data Acquisition
- Telemetry Data Handling
- Medical Electronics
- Data Concentrator/Controller
- Military Fire Control
- Message Store and Forward
- Numerical Control
- Navigation Computing
- Accounting
- Target Impact Prediction
- Supervisory Control
- Radar Data Tracking
- Coordinate Conversion
- Production testing
- Automated Test
- Information Storage & Retrieval
- Time Sharing

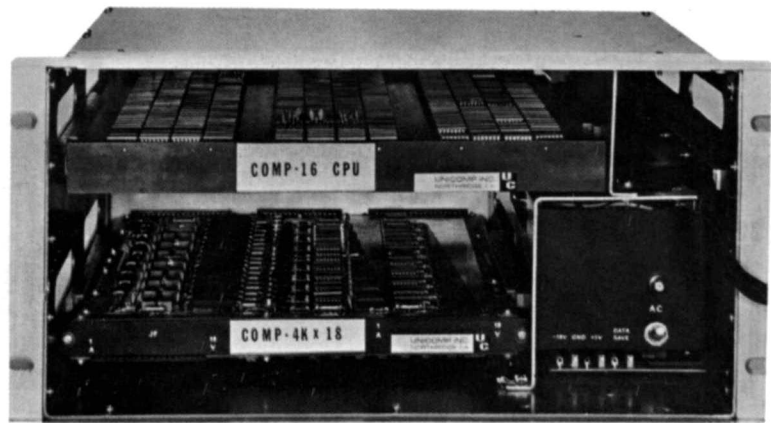


Figure A INTERIOR VIEW OF COMPUTER WITH DOOR OPEN

The COMP-16 and COMP-18 offer extensive computational and data handling capabilities through a simple yet powerful set of 31 command functions.

The repertoire of 31 functions allows ease of programming in mathematical and logical computations, as well as flexibility of input/output transfers and of real-time, on-line operations. The computers feature parallel data transfer, two's complement binary arithmetic, external direct memory access (DMA), and address modification via six memory index registers.

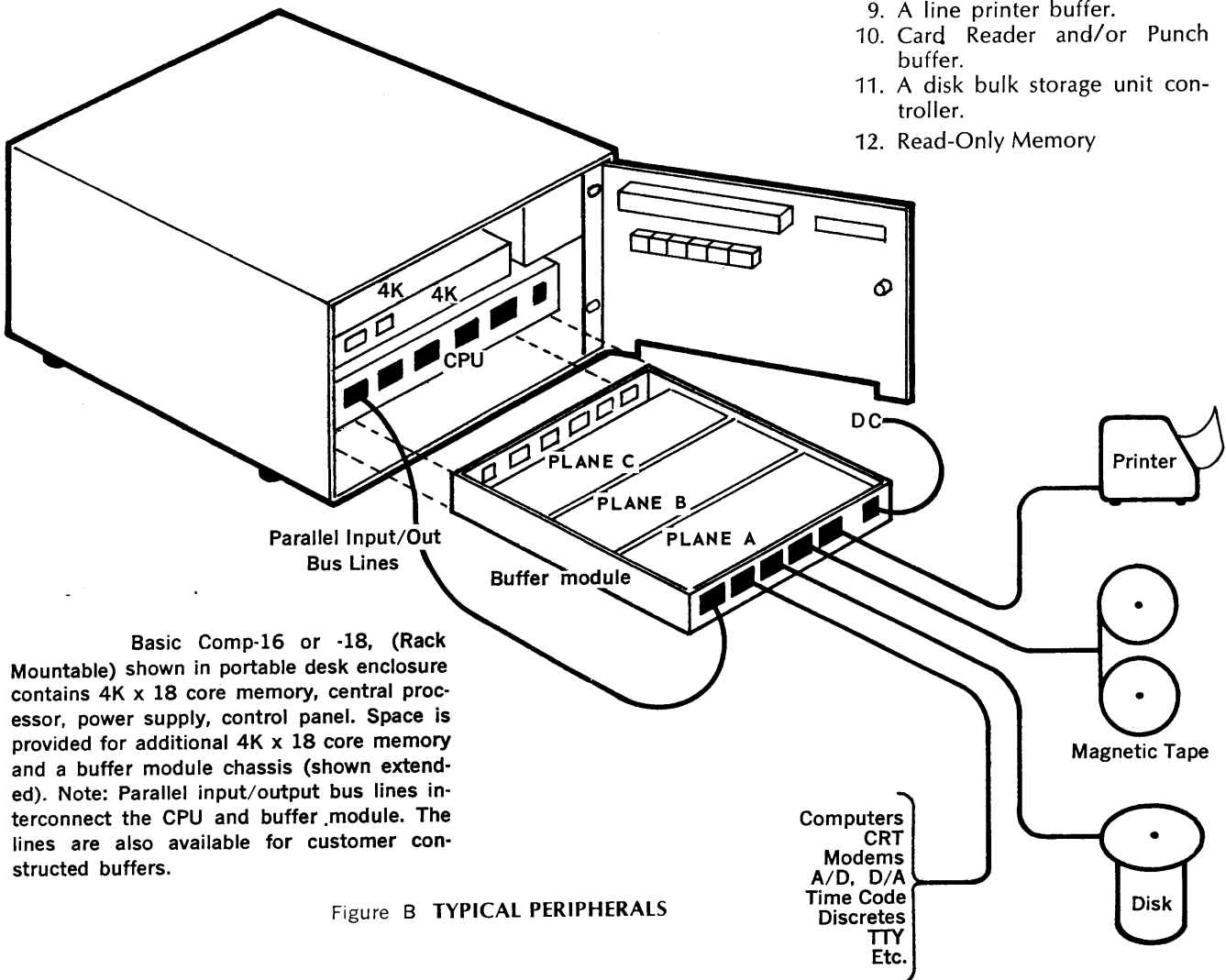
■ Optional Modules

The COMP-16 or 18 includes a number of optional modules, designed and integrated with the Central Processing Unit (CPU) to match a particular application.

■Interface Modules

Standard modules optionally available to augment the CPU for specific applications include the following:

1. Core memory, in increments of 4096 (.9 usec cycle time).
2. A hardware multiply/divide/square-root module (MDSR).
3. A real-time clock for registering relative time to a precision of 10^{-4} (DECIMAL) or 2^{-16} (BINARY) or for counting timing signals supplied by an external source.
4. An interrupt module for processing up to 64 external priority interrupts.
5. A teletype printer/keyboard/tape-unit buffer.
6. Photo-electric paper tape reader buffer.
7. Paper tape punch buffer.
8. Magnetic tape read/write controller (4 tape units per controller).
9. A line printer buffer.
10. Card Reader and/or Punch buffer.
11. A disk bulk storage unit controller.
12. Read-Only Memory



Basic Comp-16 or -18, (Rack Mountable) shown in portable desk enclosure contains 4K x 18 core memory, central processor, power supply, control panel. Space is provided for additional 4K x 18 core memory and a buffer module chassis (shown extended). Note: Parallel input/output bus lines interconnect the CPU and buffer module. The lines are also available for customer constructed buffers.

Figure B TYPICAL PERIPHERALS

Specifically tailored input/output buffer modules are available for other forms of input and output as follows:
(see figure B)

1. Discrete input and output units for electronic or contact closure signals.
2. Analog-to-Digital and Digital-to-Analog converters.
3. Digital-to-Synchro and Synchro-to-Digital converters.
4. Digital communication modems.
5. Time code receivers.
6. Shaft encoders.
7. Doppler receivers.
8. Computer to Computer Communication.
9. Data Terminals.

SYSTEMS CHARACTERISTICS

UNICOMP	COMP-16	COMP-18
Memory:		
Memory Cycle Time (us)	.9	.9
Memory Word Length (bits)	16	18
Minimum Memory Size (words)	4K	4K
Memory Increment Size (words)	4K	4K
Maximum Memory Size (words)	65K	262K
Parity Check	opt.	no
Memory Protect	opt.	opt.
CPU FEATURES:		
Instruction Word Length	16	18
Number of accumulators	1	1
Number of index registers	6	6
Bits for operation code	5	5
Bits for address modes	3	3
Addressing modes	4	4
Bits for address	8	10
Words directly addressable	256	1024
(in microseconds)	2.25	2.25
Words indirectly addressable	65K	65K
(in microseconds)	3.15	3.15
Indirect addressing, type	Single	Single
Arithmetic Operations:		
Store time for full word (us)	2.25	2.25
Add time for full word (us)	2.25	2.25
Fixed-point hardware mult/divide	opt.	opt.
Multiply time Hardware (us) (unsigned)	7.2	8.1
Divide time Hardware (us) (unsigned)	7.7	8.6
Multiply time Software (us)	330	360
Divide time Software (us)	450	505
I/O Capability:		
Data address output bus	16	18
Data path output bus	16	18
Direct memory address (DMA)	16	18
Data path input bus	16	18
Maximum DMA word transfer rate	1.1 MHZ	1.1 MHZ
Number of external priority interrupt levels provided in basic system	1	1
Maximum number of external interrupts	64	64
Response time (us) including time to save registers of interrupted program and initiate new program execution	4.5	4.5
Other Features:		
Power failure protect	std.	std.
Automatic restart after power failure	opt.	opt.
Real-time clock or internal timer	opt.	opt.
Software:		
Assembler (1 pass, 2 pass, both)	both	both
Relocatable assembler (yes, no)	yes	yes
Minimum core size necessary to use this relocatable assembler	4K	4K
Macro assembler capability	yes	yes
Conversational interpreter	BASIC	BASIC
Other Software packages are being developed or will be developed to meet specific requirements.		

COMMAND STRUCTURE

The COMP-16 or COMP-18 operates by performing arithmetic, logical and decision operations on data stored in its memory elements and/or received from input sources. The results of its operations are temporarily stored in memory for additional processing later, or supplied to output devices. The operations it performs are determined and controlled by a series of commands, also stored in its memory.

■ Command Format

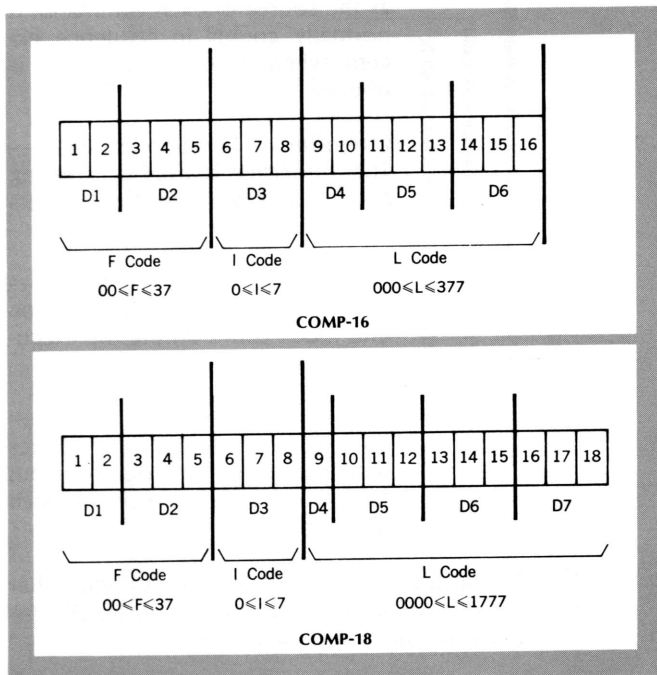
Each command stored in memory for COMP-16 or 18 execution is in three parts (see Command Format in Figure C). These three parts are:

The Function Code (F) tells what type of operation is to be performed by the command.

The Index Code (I) designates an index register and/or tells the type of addressing to be used by the command.

The address or Location Code (L) normally designates a memory cell in which a number is located to be used in the execution of the command. The L code can also be used as an operand, or as an input/output address.

The F code comprises five binary bits, and can designate any one of 31 functions to be performed. The I code comprises three bits and can designate one of six index registers (part of memory). The I code also designates one of four possible methods of addressing to be discussed. The L code comprises eight bits in the COMP-16 and 10 bits in the COMP-18. The L code has different meanings depending upon the method of addressing selected by the I code in a manner explained below.



Note: D1 - D7 are octal characters of command for Display and Teletype Format

Figure C COMMAND FORMAT

■ Addressing

As each command is executed an effective address is usually created. The effective address either refers to a memory location in which an operand is located, or to the number of shifts, or it designates an input/output code. In some commands there is no effective address; the operand is then part of the command.

There are basically four methods for creation of the effective address and/or operand. The method used is dependent upon the value of the (3 bit) I code as follows:

I Code

(octal)

■ Address Description ■

- 0 Direct Addressing — The L code is the effective address of the command.
- 1 - 5 Indexed Addressing — The effective address is obtained by the addition of the L code portion of the command to the contents of the Index Register designated by the I code (i.e. 1 to 5).
- 6 The effective address or operand is dependent upon the value of the F code (see below).
- 7 Indirect Addressing — The effective address is obtained from the memory location designated by the L code.

An I code of 6 with a Function Code of 10 to 17 (arithmetic and logic functions — see Function Code List) indicates that the L code of the command is to be used as an operand. For all other function codes, an I code of 6 has the same meaning as I codes of 1 to 5 (i.e. it designates an index register). The index registers are actually memory locations, specifically locations 101 to 105 (octal), with 106 being an index register when I = 6 designates an indexed command.

The four modes of addressing provide a powerful means for circumventing the problems created in computers whose address code is limited in length. Double word commands and “paging” are not necessary. Since indexed and indirect addressing allow addresses to comprise a full word, up to 65,536 locations can be addressed by any command of the COMP-16. (262,144 locations in the COMP-18).

■ Operating Registers

The COMP-16 and 18 have five operating registers as follows:

A register or Accumulator — This is the main arithmetic and operational register. It is normally the source or destination of information for each command execution.

P register or Program Counter — The P register (or counter) keeps track of the memory location used as the source of each command. It normally counts in sequence except when a jump command is obeyed.

L register or Location Address — The L register is used in creating and holding the effective address of the command.

FI register or Function/Index — This register holds the Function and Index codes during the execution of a command.

M register or Memory Register — This register temporarily stores data being put into or taken out of memory, and is part of each 4k memory module.

The FI register is 8 bits in length. All the other registers are either 16 bits or 18 bits in length, for the COMP-16 and 18, respectively.

COMP-16 AND COMP-18 LOGIC DESCRIPTIONS

The COMP-16 and COMP-18 are designed and built on the Bus principle which means all communication between elements of the COMP-16 and COMP-18 are performed by means of communication buses. Figure D shows the mechanism of these buses. Four buses are used for communication between the basic elements; these basic elements are as follows:

1. The four computational registers.
2. The Arithmetic, Logic, and Transfer (ALT) Unit, part of the CPU.
3. Various Memory Modules.
4. Miscellaneous Input-Output Interface Units.

A Control Decode and Timing Unit is used to decode the Command Function Code and Index Register Code (F & I) and supply control signals to all elements. It also performs the timing function.

In normal operation information from some element (e.g., a register) is supplied to the Addend Bus, transferred through the ALT unit to the Sum Bus, and then supplied to some other element (e.g., another register). Simultaneously, the contents of the A or L register may be put on the Augend Bus and supplied to the ALT unit and an arithmetic or logical operation performed, with the results going on the Sum Bus.

If information is to be transferred to (or from) memory, or to (or from) an I/O interface unit, an address is placed on the address bus simultaneously with transfers through the ALT unit. For example, if a word is to be read from a memory unit, the address is put on the Address Bus from one of the registers. The requested word is placed on the Addend Bus by a memory unit, passed through the ALT unit onto the Sum Bus, and then to one of the registers. An arithmetic or logical operation can be performed by the ALT unit during a transfer from memory.

An Input/Output buffer module makes use of the buses in the same way that the rest of the COMP-16 or COMP-18 uses them. Transfers to or from an I/O buffer module may be under control of program, as previously described, or they can be controlled by the I/O buffer unit itself by means of the Direct Memory Access (DMA) feature.

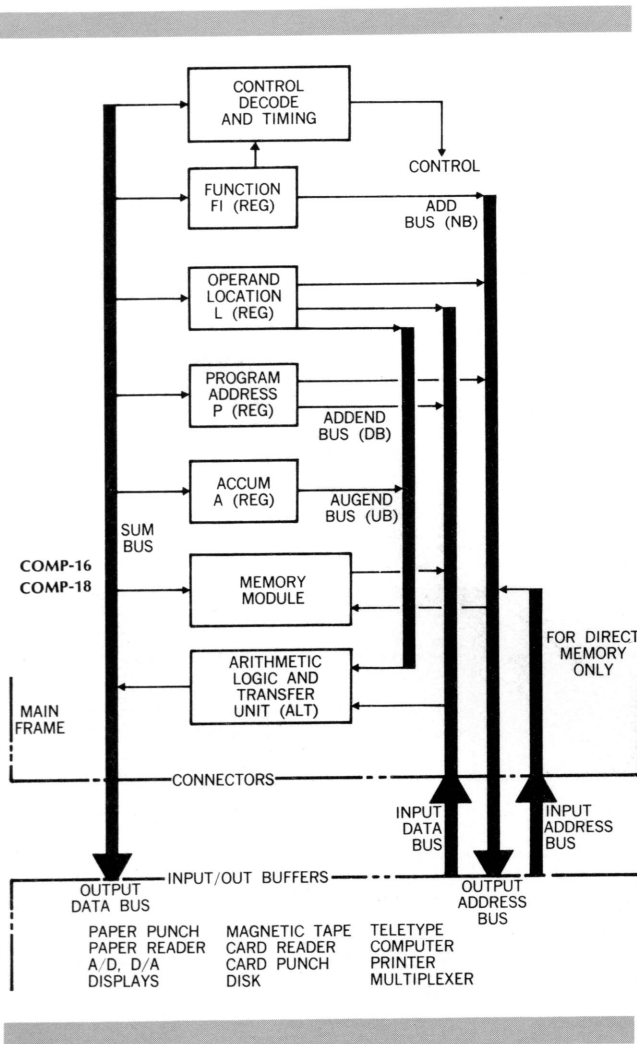


Figure D COMPUTER BUS STRUCTURE

The direct-memory access feature of the COMP-16 or COMP-18 provides for non-programmed data transfers to and from memory. The DMA function provides the capability of data transfers to and from memory without program intervention. It allows a peripheral device option to request the transfer of one or more words of data while temporarily halting the processing of the stored program.

DIRECT MEMORY ACCESS

To prevent several peripheral device options from requesting data transfers at the same time, a priority scheme determines the order in which the requests may occur. During the interval in which the transfer takes place, the stored program is stopped for at least .9 microsecond. This cycle stealing does not disturb the contents of the operational registers.

In this way, the program may proceed normally at the conclusion of the transfer. With the DMA feature, the data-transfer rate after the first data word transfer can be as high as 1.1 million words per second. The time to transfer the first word in this mode is a function of the operations being performed by the computer at the time of the request. The time delay for a one word transfer is 2.25 to 4 microsecond.

Devices which operate at very high speeds or which require very rapid responses from the computer utilize the DMA feature. The DMA feature is highly effective for devices that transfer large

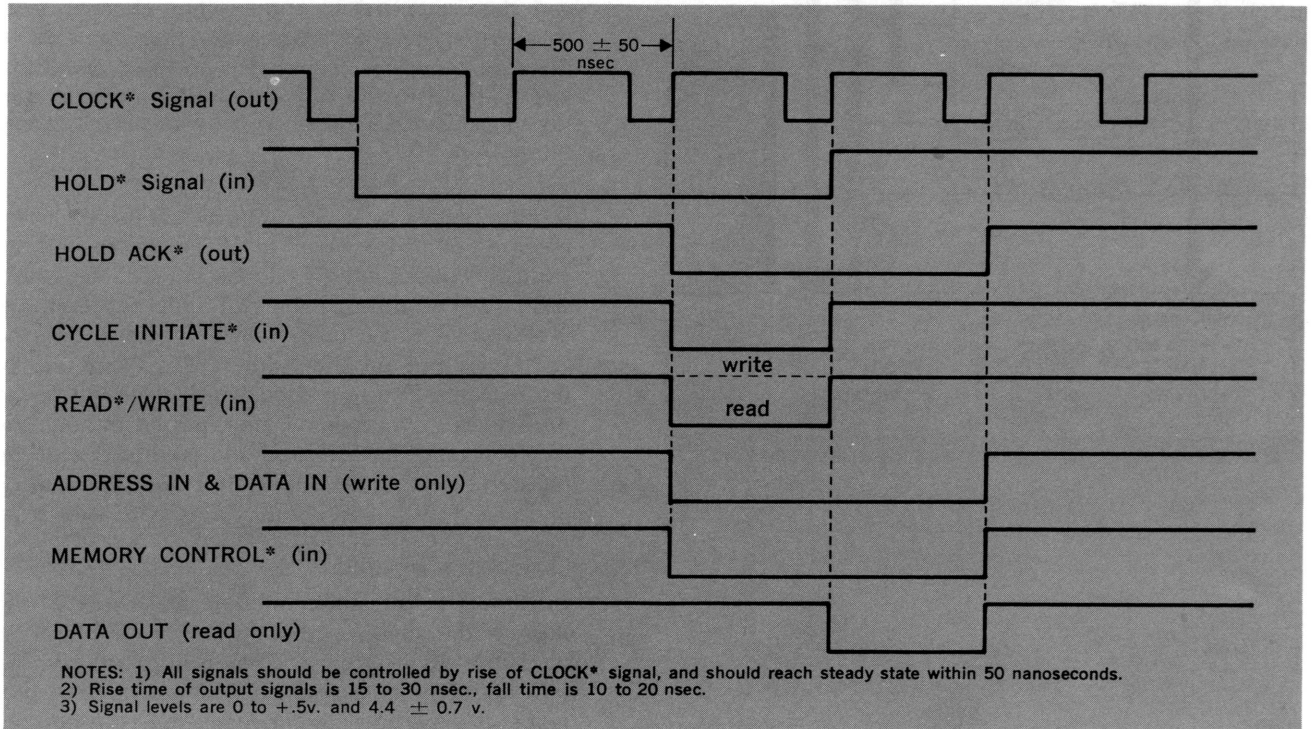


Figure E WAVEFORMS - DIRECT MEMORY ACCESS

amounts of data in block form; e.g., high speed magnetic tape systems, random access disk files, CRT display systems, high-speed drum memories, high speed communications devices or high-speed computer to computer memory transfers.

The COMP-16 and COMP-18 computers utilize a .9 microsecond internal random-access lithium core memory in sizes ranging from the basic standard memory of 4096 words to 65536 sixteen (16) bit words in the COMP-16 to 262,144 words in the COMP-18.

The core memory provides random-access storage for both instructions to be performed and information to be handled. The basic memory holds 4096-16 or 18 bit words in the standard Comp computers. Optional equipment extends the memory capacity in banks of 4096 words or expands the COMP-16 word length to 17 bits to provide parity checking.

In addition to the main core memory, a set of 48 (non-destruct) memory locations are used to store constants and instructions for an initial load of programs. This feature is called the "Bootstrap Loader" and is standard in both computers.

■ Simultaneous Running Memory Option

The Simultaneous Running Memory (SRM) option allows high-speed external devices to obtain access to part of the memory on an exclusive basis as required, yet allows access to that same memory by the CPU when exclusive external access is not required.

The SRM feature allows one or more external devices to use one part (or bank) of memory at the same time that the CPU uses another. A minimum of two banks of 4096 words of memory is required. In many applications a third bank is desirable.

Typical external devices which can make use of the SRM are:

1. High speed disk or drum memories
2. High speed magnetic tapes
3. High speed A/D converters
4. CRT display units
5. Very high speed communications terminals

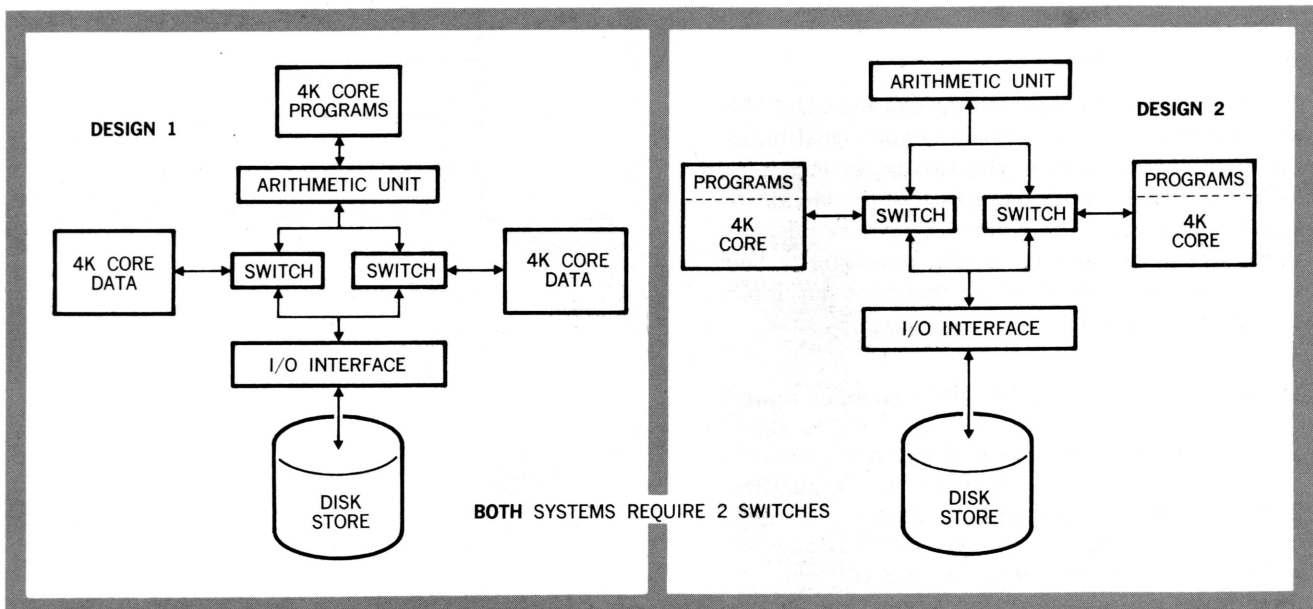


Figure F SIMULTANEOUSLY RUNNING MEMORIES

The COMP-16 and COMP-18 Input/Output section is designed to interface with any number of devices, both standard and non-standard in nature. Standard accessories to the COMP-16 and COMP-18 include a number of devices for supplying data to the computer and accepting data from the computer. Each of these devices utilizes, an input/output buffer or controller specifically designed to interface the COMP-16's or COMP-18's input/output section to the specific device. The standard devices include:

- A Teletype ASR-33 or ASR-35 printer / keyboard / tape-reader / punch
- Magnetic Tape Units
- High speed paper tape readers
- High speed paper tape punch
- A real-time clock
- Card reader and/or punch
- Line Printer
- A disk bulk storage unit

The types of non-standard devices which can be used with the COMP-16 and COMP-18 are virtually unlimited. Each such device can be interfaced directly to the standard input/output buses of the COMP-16 and COMP-18, or a special input/output buffer controller may be designed to supply suitable input/output characteristics for the device. Typical special devices which can be connected to the COMP-16 and COMP-18 are:

- Analog-to-Digital converters, with or without multiplexers
- Synchro-to-Digital converters, with or without multiplexers
- Digital-to-Analog converters
- Digital-to-Synchro converters
- Communication modems
- Displays

■ Standard I/O Interface

The standard input/output interface of the COMP-16 and COMP-18 comprises two multiple signal buses plus two control signals. The two buses include a 16 or 18 signal input/output bus, and a 16 or 18 signal address bus. The control signals include one signal which indicates on output operation (called OUT) and one signal which indicates an input operation (called RIN).

When the COMP-16 or COMP-18 supplies output data, it places an address on the 16 or 18 signal address bus, all signals in parallel, and 16 or 18 bit numerical value on the I/O data bus, in parallel; it then creates a signal on the OUT control line indicating that the address and output data are valid. Any one of a number of devices connected to these buses will recognize the address on the address bus when the OUT signal occurs, and will accept the data on the I/O data bus.

INPUT/OUTPUT

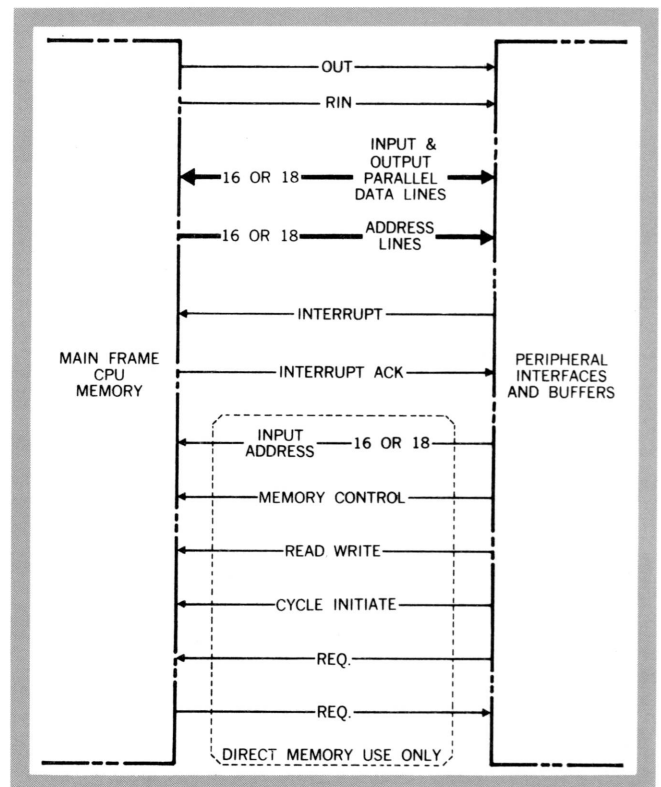


Figure G INPUT/OUTPUT LINES

The COMP-16 or COMP-18 accepts input data on the I/O data bus whenever it supplies the RIN control signal. When the RIN signal occurs, the COMP-16 or COMP-18 also supplies a 16 or 18 bit parallel address on the address bus. This address is recognized by one of the devices connected to the buses, which supplies the input data to the COMP-16 or COMP-18 on the I/O data bus.

The voltage levels of the input and output signals vary between ground level and +4.5 volts (± 1.0 v.). The false or quiescent level of all signals is +4.5 volts. The true or active level is ground. The OUT signal is 500 nanoseconds in width, with fall and rise times of less than 30 nanoseconds. The RIN signal is 1.0 usec in width, with 30 nanosecond fall and rise times. The output data and address signals will remain steady while the OUT signal is true; the same is true of the address signals when the RIN signal is true. The input data signals must be steady during the last 200 nanoseconds of the time that the RIN signal is true.

■ Teletype Input/Output

A standard buffer is designed to interface the Teletype ASR-33 or the ASR-35 send-receive units to the COMP-16 or COMP-18 input-output section as described above. A two wire connection is used between this buffer and the ASR; thus, any standard ASR which uses the ASCII 8-level code can be used with the COMP-16 or COMP-18.

In the quiescent state, the ASR interface unit supplies a positive current in the two lines of 60 milliamps. When a key is depressed on the ASR, or the tape reader is started, the ASR interrupts the current in the line, which is sensed by the input buffer. The input signal is "time sequenced" into

11 different time segments per character, each segment exactly 9.1 msec. long. During each segment the current may (or may not) be interrupted by the ASR depending upon the character being transmitted.

When the COMP-16 or COMP-18 supplies data to the ASR, it also interrupts the current supplied to the ASR during a series of 11 timed segments.

■ Direct Memory Access

The DMA feature of the COMP-16 and COMP-18 allows a peripheral controller to transfer data directly between the memory of the computer and the peripheral. The Input/Output bus used for standard I/O is used for data transfer to and from memory. In addition, an input address bus of 16 or 18 bits plus four input and one output control lines are used for memory communication.

A DMA operation starts with a request by the controller over a request line for access to the memory. The computer temporarily stops operating and acknowledges the request over the Request Acknowledge Signal Line. The controller then uses the remaining control lines for making its access.

It takes .9 usec to make access to the memory. (See Waveform Figure E) However, it normally takes about 3 usec for the computer to stop operating so that the access can be made.

■ Interrupt Function

The interrupt function of the COMP-16 and COMP-18 computers provides the capability for peripheral devices to request the computer to execute an instruction independent of the stored computer program. In order to prevent several peripheral device

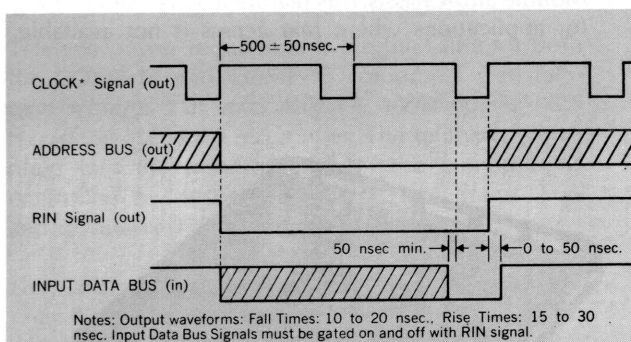
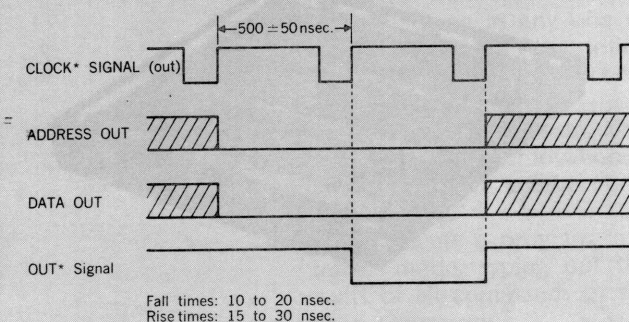


Figure I OUTPUT WAVEFORMS

Figure H INPUT WAVEFORMS



options from requesting interrupts at the same time, a hard-wired daisy chain priority scheme determines the order in which the requests may occur. Requests will normally originate in interface units. During the interrupt, the computer is directed to the memory location specified by the interrupting device and the instruction found at that address is executed.

The interrupt option is a hard-wired module in the computers. The number of interrupts is limited only by the size of the core memory of the COMP-16 or COMP-18. The practical limit of external interrupts is 64. The Function Code 01, Mnemonic INT, and Operational Description-Jump to Fixed Address if Interrupted, is hard-wired in the COMPs 16/18 and is automatic from external devices. The Function Code 01 is not available to the programmer as a useful instruction.

CONSTRUCTION

The basic COMP-16 and COMP-18 Computers are each housed in a single 8³/₄ inch rack mountable chassis, (see Figure A) that contains the power supply, Central Processor Unit, core memory and control panel. Space is provided in the same main chassis to accommodate additional 4096 words of core memory and a Buffer Module Sub-Chassis which can be wired to operate and control various peripheral devices. (see Figure J for Buffer Module Configuration)

When further expansion is desired, the parallel input/output BUS lines of the computer are used to operate additional memory or interface buffering for peripheral devices.

Each additional chassis can accommodate up to 16,384 words of core memory (including a dual power supply to handle the extra power required). Additional chassis can accommodate (2) memory banks, (2) Buffer Module Sub-Chassis, and power supplies for use in extensive interface buffering such as disk controllers, etc.

As noted in (Figure B and J) inter-connection can be made either from the front or rear of the Buffer Module Sub-Chassis. This feature allows front cabling for applications where rear access is not available.



Figure J CPU AND BUFFER MODULE CHASSIS

The Computer measures $8\frac{3}{4}$ inches high, 19 inches wide, and 22 inches deep. The basic chassis utilizes a hinged, swing-out front panel for easy access to the wiring and inter-cabinet cabling located just behind the front panel. Cabling to other devices, such as the Teletype or other input/output accessories can pass through either the back or the front panels.

The CPU and Buffer Sub-Chassis can be removed from the front; installation, operation and trouble shooting can be done from the front. The main chassis is mounted on slides for easy removal of the entire unit from a cabinet.

The computer logic is constructed using silicone encapsulated, integrated circuits, including medium scale integration (MSI) circuits and high speed TTL circuits. The circuit chips are firmly affixed on horizontal flat planes which are part of the module chassis. Three flat planes are used in both the CPU, and Buffer Module Sub-Chassis.

The front panel has a minimum of operational controls used primarily for program checkout, bootstrap loading of programs, and maintenance. An attractive six (for COMP-16) or seven (for COMP-18) digit display can be used for octal display of any one of the four operational registers selected by a momentary pushbutton.

■ Environment and Power Requirements

The operating temperature range of the Comp computers is 0°C to 50°C . Relative humidity can be up to 95% without condensation. The cooling is blower forced ambient air. Power requirements are 115-220 volts A.C. $\pm 10\%$; single phase from 50 to 400 Hz $\pm 10\%$. The computer draws 2.5A and dissipates 250 watts. During shipping or storing of the system, the ambient temperature may vary between 0°C and 65°C .

Teletype power requirements are the same for both the COMP-16 and COMP-18 computers. The teletype requires 115 volts A.C. ($\pm 10\%$) 60 Hz ($\pm .5$ Hz), or 50 Hz ($\pm .75$ Hz) power. The teletype, which plugs into the front or back of the computer, is controlled by its own on/off switch, draws 2.0A and dissipates 150 W.

The CPU and Buffer Modules are constructed on "Flat Planes". Each plane accepts 124 in-line chips. Vcc and ground are distributed by etched circuitry on both sides of the plane. This concept reduces noise, cross talk, voltage drop and allows increased operational throughput. The flat planes are shrouded by a ruggedized aluminum chassis measuring 2 inches by $16\frac{7}{8}$ inches by 15 inches deep.

Software available with the COMP-16 and COMP-18 includes a number of functional packages, each described in its own manual.

■ UniCap Assembler

UniCap is an assembler which operates in one or two pass modes on a 4K memory COMP-16 or COMP-18 with a Teletype ASR-33 Automatic Send/Receive Unit. UniCap will convert a source program written symbolically, absolutely, or in combination thereof into an object program for running on the computer.

The UniCap program accepts monocode (one-to-one) mnemonic operations and polycode (one-to-many) mnemonic operations in the source program. In addition to input, paper tape and printer outputs are possible with UniCap.

UniCap allows a sort of conversational communication between the operator and the computer as the operator enters and checks out programs.

UniCap performs four different operations in communication with the operator.

1. It accepts data typed on the keyboard for specific memory locations in any one of four formats:
 - A) Mnemonic
 - B) Octal numeric
(sign and five digits) for Comp - 16
(sign and six digits) for Comp - 18
 - C) Octal command
(six octal digits) for Comp - 16
(seven octal digits) for Comp - 18
 - D) Binary
2. It supplies data from memory to the Teletype in any one of the above formats for printing or for printing and punching tape.
3. It will accept a typed instruction to jump to any other location in memory to start another program running.
4. It will execute a program in a "trace" mode, typing out the results of all commands or selected commands.

■ BASIC* Language

BASIC is an easily learned, general purpose conversational language that uses statements closely resembling simple English and algebra. The simplicity of the language structure makes it possible to begin programming immediately. Prior knowledge of the organization and operation of the Comp computers is not necessary. BASIC is used in schools, business and industry as an ideal language for general problem solving applications.

■ Sub-Routine Library

The Sub-Routine Library is a package of commonly used routines for data conversion and arithmetic

functions. Included in the Mathematical Function Sub-Routines are:

- Trigonometric sine/cosine
- Trigonometric arctangent
- Natural logarithms
- Exponentials
- Square Root
- Arithmetic Sub-Routines

Includes single and extended precision fixed and floating point operations for add, subtract, multiply and divide. Extended precision is up to 7 words.

Other documentation available includes, peripheral description, reference manual, and maintenance manual.

FUNCTION LIST

F CODE	MNEMONIC	OPERATIONAL DESCRIPTION	F CODE	MNEMONIC	OPERATIONAL DESCRIPTION
00	HLT	Jump to Effective Address and if the Halt Command switch is ON, stop computing.	22	JAP	Jump to Effective Address if (ACC) is positive.
01	INT	Jump to Fixed Address if Interrupted. (Not available to programmer.)	23	JAN	Jump to Effective Address if (ACC) is negative.
02	INC	Increment Designated I register and if it is negative, Jump to the location whose address is the sum of the A register and Program Counter. (L is the increment value.)	24	JEP	Jump to Effective Address if Accumulator has an even number of one's.
03	JPR	Record present value of program location counter in word 107 and Jump to effective address.	25	JNC	Jump if there was No Carry to the Left of bit 1 on the last ADD or SUB command obeyed.
04	SPC	Store the contents of the Program Location Counter in Effective Address.	26	JOF	Jump to Effective Address if Overflow has been set.
05	STA	Store (ACC) in Effective Address.	27	JMP	Jump to Effective Address Unconditionally.
06	RIN	Read in Data. Put Effective Address on external lines and read input lines into Accumulator.	30	SLA	Shift (ACC) Left Arithmetically, a number of places specified by the Effective Address, (Sign unchanged).
07	OUT	Output Data. Put (ACC) and Effective Address on external lines.	31	SLX	Shift (ACC) Left End-Around through exchange bit, the number of shifts specified by the effective address.
10	LAP	Load Accumulator with Operand.	32	SLL	Shift (ACC) Left Logically, a number of places specified by Effective Address. (Sign shifts also).
11	LAN	Load Accumulator Negatively with Operand.	33	SLE	Shift (ACC) Left End-Around, a number of places specified by the Effective Address.
12	ADD	Add Operand to (ACC) and put the sum in Accumulator.	34	SRA	Shift (ACC) Right Arithmetically, a number of places specified by the Effective Address, (sign copies into next bit, but remains unchanged).
13	SUB	Subtract Operand from (ACC) and store the difference in the Accumulator.	35	SRX	Shift (ACC) Right End-Around through exchange bit, the number of shifts determined by the effective address.
14	AND	Logical AND of (ACC) with Operand.	36	SRL	Shift (ACC) Right Logically, a number of places specified by the Effective Address, (sign is copied into next bit and set to zero.)
15	ANI	Logical AND of (ACC) with Operand inverted.	37	SRE	Shift (ACC) Right End-Around, a number of places specified by the Effective Address.
16	LOR	Logical OR of (ACC) with Operand.			
17	EXO	Exclusive OR of (ACC) with Operand.			
20	JAZ	Jump to Effective Address if (ACC) is zero.			
21	JNZ	Jump to Effective Address if (ACC) is non-zero.			

Note: (ACC) means "Contents of Accumulator"
Exchange Bit (F = 31 & 35) records the carry propagated from bit 1 on addition or subtraction.

GENERAL SPECIFICATIONS COMP-16 AND COMP-18 DIGITAL COMPUTERS

TYPE:

General Purpose Stored Program
 Parallel Data Transfer
 Designed for Rugged Use
 Specially Tailored to Users Application

30 bits by 30 bits
 producing 30 bits 1250 usec
 34 x 34 to 34 for
 COMP-18 1450

MEMORY:

.9 us Core
 16 Bit Word and 18 Bit Word
 Parity check Optional with COMP-16

e) Hardware MDSR (option) Operation times.

Multiply—
 16 bits x 16 bits = 32 bits (unsigned) 7.2 usec
 15 bits x 15 bits = 30 bits (signed) 9.0 usec
 18 bits x 18 bits = 36 bits (unsigned) 8.1 usec
 17 bits x 17 bits = 34 bits (signed) 9.9 usec
Divide (Quotient plus remainder)—
 32 bits/16 bits = 16 bits (unsigned) 7.7 usec
 30 bits/15 bits = 15 bits (signed) 9.5 usec
 36 bits/18 bits = 18 bits (unsigned) 8.6 usec
 34 bits/17 bits = 17 bits (signed) 10.4 usec
Square Root—
 32 bits → 16 bits + Remainder 21.6 usec
 36 bits → 18 bits + Remainder 24.3 usec
 All quantities treated as intergers.

LOADER:

Hardware, standard; operates with Teletype or
 Photoreader (or other media optional)

BASIC COMMAND FUNCTIONS:

Arithmetic and Logic	8
Store	2
Branching	9
Shift	8
Input/Output	2
Indexing	1
Halt & Unconditional Jump	1
—	
Total	31

OPERAND ADDRESSING TYPES:

Direct
 Indirect
 Indexed
 No Address

INDEX REGISTERS:

Six, Part of Core Memory
 All Registers Indexable by a number from 1 to 255

SPEED:

a) Add and Store Functions			
Direct addressing		2.25 usec	
No addressing		1.8 usec	
Indexed or Indirect addressing		3.15 usec	
b) Jump Commands			
Direct addressing		1.8 usec	
Indexed or Indirect addressing		2.7 usec	
c) Shift Commands			
Direct addressing		2.25 + .9 n usec	
Indexed or Indirect addressing		3.15 + .9 n usec	
			(where n is number of shifts)
d) Programmed Multiply			
15 bits by 15 bits	COMP-16	COMP-18	
producing 15 bits			290 usec
17 x 17 to 17 for			
COMP-18			340
15 bits by 15 bits			
producing 30 bits			430 usec
17 x 17 to 34 for			
COMP-18			505

INTERRUPTS:

Optional up to 64

ARITHMETIC:

Parallel 16 or 18 bit, Binary 2's Complement

CONSTRUCTION:

Rugged Aluminum Chassis
 Epoxy Circuit Boards
 Plug-in Integrated Circuits
 Wire Wrap Wiring
 Complete Front Access to all elements and
 cabling (optional)
 Swing Out Front Panel

FRONT PANEL DISPLAYS AND CONTROLS:

- a) Power ON/OFF Switch
- b) Run/Idle Switch plus indicator
- c) Single Cycle Step Switch plus internal halt indicator
- d) Halt Command Enable Switch plus indicator
- e) Loader Selector Switch
- f) Two Program Address Selectors (word 0 and word 400)
- g) Five Register Display Selectors
- h) Set of Six Octal Indicators for Register Display. (Seven indicators for COMP-18)

All switches pushbutton indicating type, either momentary or toggle.

SIZE:

Basic Cabinet: 8-3/4" high by 22" deep, made for 19" relay rack
 Additional Cabinets of same type added as needed.

WEIGHT:

45 pounds for minimum system, not including peripherals

Continued

LOGIC:

Integrated Circuit TTL, 5 volt supply

POWER:

115-220 VAC, 60 CPS, 3 wire 250 watts, minimum system, DC Voltages: +5V, -18V.

INTERCONNECTION:

Either front panel or rear panel connections may be ordered.

CUMULATIVE OUTSTANDING FEATURES

The following is a list of outstanding features and characteristics of the UniComp Computers. The features cumulatively derived constitute more computer value for the dollar and a true justification for their selection.

BOOTSTRAP LOADER

Flexible and powerful, hardwired, capable of loading from virtually any medium. Saves operator time and program loading time.

HALT ENABLE

Simplified operation and program checkout convenience due to the Halt Enable switch feature on the control panel.

EXPANDABLE MEMORY

Modular, fast .9 microsecond memory, expandable to 65K Addressable Words. (Or More).

CONTROL PANEL SIMPLICITY

Operator convenience and ease through Control Panel simplicity, easily learned, no data entry required from control panel.

COMMAND LIST

Programmer convenience and rapid productivity due to powerful and easily learned Command List.

ADDRESS MODES

Programming time saved due to the simplicity of using four addressing modes 1) Direct, 2) Indirect, 3) Indexed, 4) No Address Mode which provides immediate operand since operand is part of command.

6 INDEX REGISTERS

Programming and machine time saved due to availability of 6 Index Registers.

SINGLE WORD COMMAND

Simplified program storage. Complicated programs made simpler by the use of Single Word Commands. Programs are easier to revise or to prepare initially.

PHYSICAL SIZE

Office, laboratory, industrial, or other facility space required for installation and operation is minimal due to the computers' Small Physical Size — 8³/₄" H x 19" W x 22" D.

SOFTWARE

All programs are written to be relocatable — no restrictions to relocating programs, thus saving time, and providing programmer convenience and flexibility.

INPUT/OUTPUT

Standard and custom application oriented UniComp Input/Output system is designed to provide the user with expandability and flexibility through full parallel word transfer buses including control signal lines. The user can readily integrate the Comp-16 and/or Comp-18 Computers into virtually any system. Full 32 (36) signal I/O bus for 16 (18) bit address plus 16 (18) bit data.

OCTAL DISPLAYS

The programmer and/or machine operator is readily assisted in program checkout and program start up and loading functions by visual observations of Octal Number Displays on the operator's panel.

DIRECT MEMORY ACCESS

Standard automatic Input/Output feature allows external devices to request information from or to provide data directly to memory via the Direct Memory Access feature. Provides Real-time communications capability.

CONSTRUCTION

Heavy gage aluminum construction, anodized and irridited finishes, provides adverse and corrosive environment protection, light weight — easily portable, ruggedized construction. Optional additional portable chassis with power supply.

INSTALLATION

Easy access to the internal cabinet is provided by the swing out front panel providing maintainability ease, flexibility of installation by user selection of front or rear cable connections.

PRICE

Overall quality, operational characteristics, ease of use, ruggedness, and outstanding features make a best value.

■ Training

UniComp provides a user training course for customers at the factory in Northridge, California. The course consists of basic theory, logic, instruction on programming languages, and application systems.

■ Maintenance Training

Maintenance training courses for customers are available at the factory or at the customer's facility. The course includes basic theory, computer organization, logic operation, timing, and fault diagnosis.

■ Customer Service Contract

Customer service contracts are available to provide on-site preventive maintenance and repair. Maintenance service is also available on an on-call basis with factory trained personnel. Many services and assistance are offered to the UniComp customer such as customizing the computer interface, system engineering, program assistance, program translation, training, and maintenance.

UniComp welcomes the opportunity to discuss your problem and its solution.