THE PLATO IV TERMINAL :

DESCRIPTION OF OPERATION

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FORWARD

This manual contains the logic diagrams and description of operations for the PLATO IV student terminal. Also included are timing diagrams which depict each mode of terminal operation.

A block diagram description and logic symbol description precede the detailed circuit description.

Photographs of each of each of the printed circuit cards are included to aid in servicing the terminal.

Several engineering design changes have been incorporated in the terminal beginning with serial number 262. These changes are noted in the descriptions of operation and additional schematic diagrams including the changes are shown when appropriate.

INTERCHANGEABILITY OF PRINTED CIRCUIT BOARDS

Board No.	Serial No's. 1-261	Serial No's. Above 261	Interchangeable	Explanation
A02 A03	214976 214975	215533 215532	no	These boards are not interchangeable due to clock drivers being changed to the A03 board. If they were interchanged, they would have to be interchanged as a pair, and the following wiring changes would have to be made to the old terminals. J02-B03 Cont. Clock to J03-A19 DG15 was on J03-B09. This would have to be green wired to A03-B10 and the wire on J03-B09 moved to J03-B10. -12Vdc would then have to be wired to J03-B09. Also, the board sizes are different.
A04	214974	none		New terminal does not use A04.
A05	214973	215531	yes	Except for board size.
A06	214972	215530	yes	Except for board size.
A07	214971	215529	yes	Except for board size.
A08	214970	215528	yes	Except for board size.
A09	214969	215534	no	New board uses -5Vdc and old board doesn't. If -5Vdc was wired to J09-B05, it would be interchangeable except for board size.
A10/11	214968	215527	yes	Except for board size.
A12	214967	215526	yes	Except for board size.
A13	214966	215525	no	New and old boards have different ROM's; otherwise, they are the same except for board size.
A14	214965	215524	yes	Except for board size.
A15	214964	215523	yes	Except for board size.
A16	214963	215522	yes	Except for board size.

PLACEMENT

The PLATO Terminal is designed to fit on a standard 30" desk top with keyset connected and placed against the front. At least 2 inches clearance at the back is required for the flow of exhaust air. The terminal operating environment is for room temperature conditions ranging from 20° to 40°C and moderate humidity.
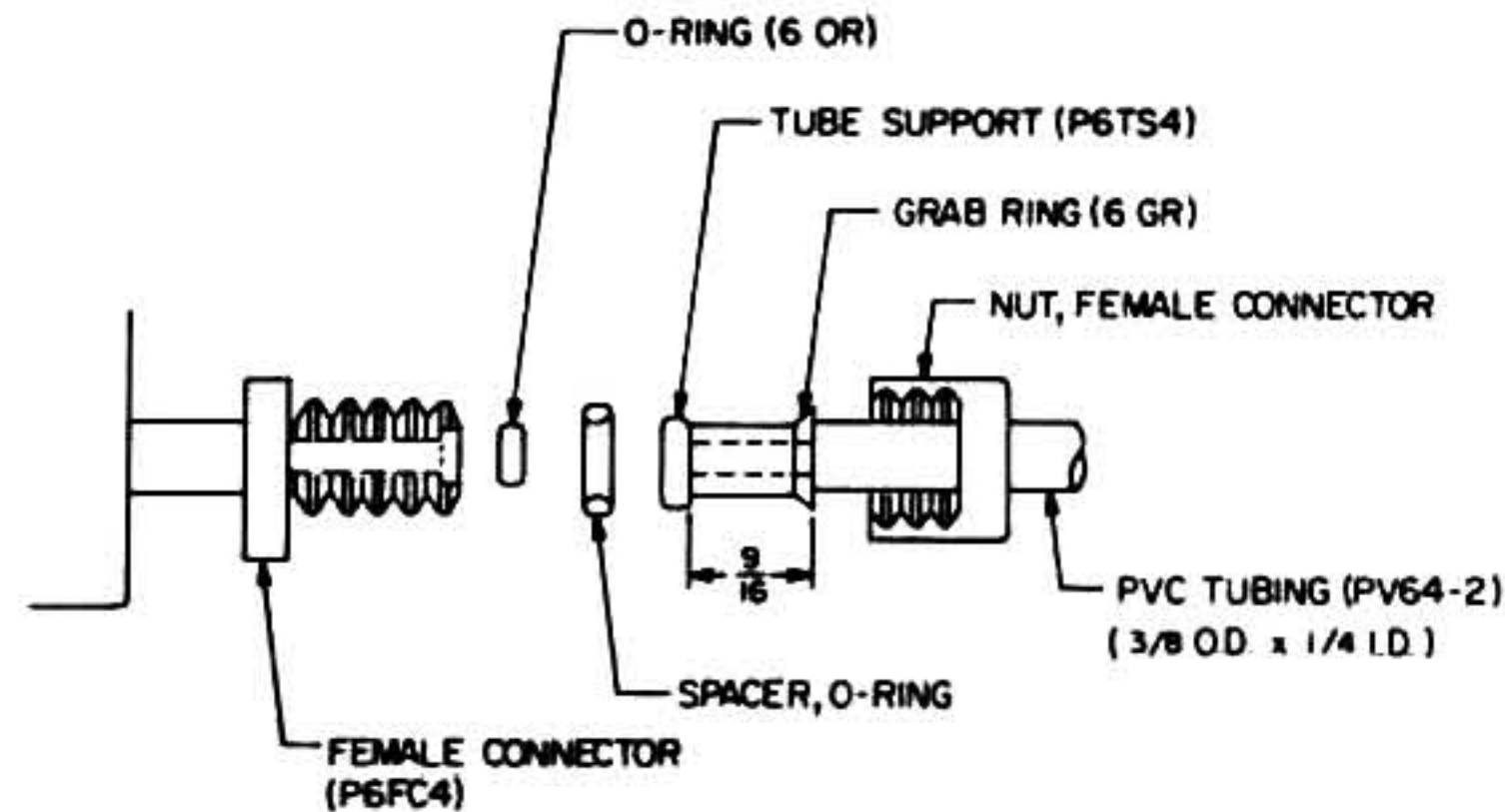
INPUT POWER REQUIREMENTS

Electrical

The terminal requires electrical input power of 115 VAC, 50-60 Hz, 5A maximum. A power cord is included with each terminal.
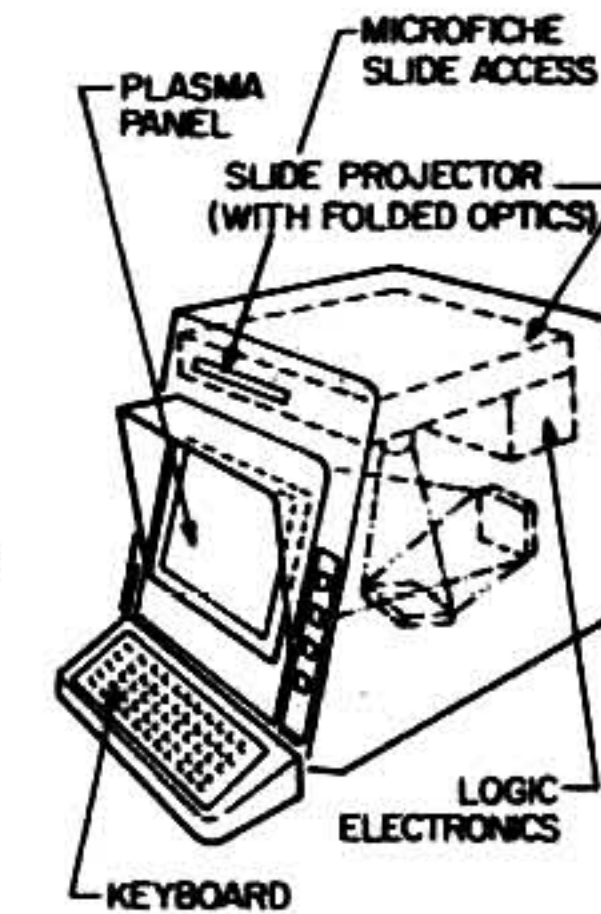
Pneumatic

Pneumatic power is required to operate the slide projector. A source pressure of 10-12 psi should be provided through 3/8 O.D. x 1/4 I.D. PVD tubing (PV64-2). The diagram below illustrates the pneumatic connector mating assembly connection to the terminal. The terminal is shipped with the mating assembly consisting of Nut, Grab Ring, Tube Support, Spacer and O-ring screwed into the female connector P6FC4. After unscrewing the Nut, the tube support should be placed in the end of the PVC tubing. Then the Nut, Grab Ring, Spacer and O-Ring are placed over the tubing in the order and orientation shown. This assembly may now be plugged into any terminal using connector P6FC4. The connector and fitting are manufactured by Parker Hannifin, Inc.

O-RING (6 OR)

TUBE SUPPORT (P6TS4)

GRAB RING (6 GR)

NUT, FEMALE CONNECTOR

PVC TUBING (PV64-2)
(3/8 OD x 1/4 I.D.)

$\frac{9}{16}$

SPACER, O-RING

FEMALE CONNECTOR
(P6FC4)

MECHANICAL

Height:	22 inches
Width:	18 inches
Depth (with Keyboard):	30 inches
Weight:	130 pounds
Power:	115V, 60 Hz, 5A
	50°F to 100°F
	10% to 80%
	relative humidity

MICROFICHE SLIDE ACCESS

PLASMA PANEL

SLIDE PROJECTOR (WITH FOLDED OPTICS)

LOGIC ELECTRONICS

KEYBOARD

PLASMA PANEL	Screen Area:	8.3 inches square (512 × 512 lines > 250,000 addressable points.)
	Luminance:	Avg. point luminance exceeds 50 fl.
	Capacity:	2048 1/8-inch character. Up to 4250 inches of vectors (.033 inch grid).
	Write/Erase Speed:	180 characters/second. > 600 inches/second graphics.
	Viewing time:	Until erased.
	Full Screen Bulk Erase	400 µs.

Panel Assembly Includes Self-contained X-Y Decode and Driver Circuits.

SLIDE PROJECTOR	Luminance:	> 20 fl screen luminance
	Capacity:	256 1/4-inch microfiche images
	Speed:	Random image access within .3 second

LOGIC ELECTRONICS: Input/Output interface (20 bits/word, 60 words/second)

Character generator	180 char/second
Line generator	60 lines/second
256 Character memory	128 rom and 128 Alterable

KEYSET HOOKUP

The keyset connects to the front of the terminal through a flexible cable approximately 2-1/2 feet long. The connector may be locked in place with the retaining springs mounted on the chassis mating half of the connector. The flexible cord may be folded under the chassis if it is desirable to place the keyset against the front of the terminal.

DATA INPUT (OUTPUT)

Data input (output) from (to) the computer or communications network is at J34, the Serial Data connector. This connector is located on the rear of the terminal and is identified by the marking "PHONE". The connector is a 4 pin Molex type 1490P using male contact 1434. The mating connector required is a Molex type 1490R using female contact 1433.

PROJECTOR LAMP

Prior to initial power turn-on a check should be made to determine if the projector lamp is installed. This is done by removing the top cover which pops off by gently lifting at front and/or rear. The lamp is located in the center of the slide selector mechanism. Care should be taken not to get finger prints on the lower portion of the lamp as this shortens operating life. The lamp can be replaced by first lifting the retaining spring lever located to the side of the lamp holder assembly. Replace with standard lamp type EKP, General Electric.

POWER TURN-ON

When all input-output connections and other conditions described above have been satisfied the terminal is ready for turn-on. The power on switch is at the lower right under the front ledge. When the power switch is actuated, the projector lamp may or may not turn-on. If it turns on it will go out within 5 seconds when the terminal generates "auto reset". The "auto reset" signal initializes all terminal circuitry. (On terminals with serial numbers less than 262 the clear switch must be depressed to initialize the terminal.)

Within 2 or 3 seconds after turn-on, the plasma panel borders will light. The borders can be seen at the edge of the display area although they are partially masked by the front panel structure.

```
                        CAUTION

  If terminal is turned off, do not turn on again for at
  least 10 seconds as this may damage high voltage
  circuitry which drive the borders.
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A check should be made to verify the fans are running. This may be done by placing a hand at the rear of terminal to detect air flow. A fan is also located under the top cover to cool the slide selector lamp and film. This fan may be checked by opening the film access door located on the upper front panel or by removing the top cover.

FILM LOADING

Microfiche film strips used in the slide selector are loaded by opening the access door mentioned above. Opening the door causes the film carriage to move to the home location (with air input activated). The film strip is inserted in the plastic holder and the locating holes are placed over the locating rods. When the door is closed, the film carriage returns to its previous index location. This location is randomly determined when power is first applied to the terminal. Thereafter, it is determined by input data from whatever controller is used to exercise the terminal.

CONTROLS

The main control interface for the terminal is through the keyset which transmits data to the computer. Two front panel switches and an indicator are also provided. Their functions are described in subsequent paragraphs.

Clear Switch

The white CLEAR switch is a momentary single-pole, double-throw type switch used for initializing the terminal, clearing the "Abort" mode, and erasing the display. Actuation of the CLEAR switch will also turn off the projector lamp if it is on.

Error Indicator

When the terminal detects a parity error on input data, it enters the "Abort" mode and turns on the red ERROR indicator. The indicator remains on as long as the terminal is in the ABORT mode. The terminal remains in the abort mode until it is cleared by an appropriate input word from the computer or by actuation of the ERROR switch.

Error Switch

The red ERROR switch is a momentary single-pole, single throw type switch. Actuation of the error switch clears the ABORT mode.

The block diagram depicts the main functional units in the terminal. The terminal is designed to process 21 bit words which arrive serially at a rate of up to 60 words per second or 1260 bits per second. The terminal transmits 12 bit words back to the computer. Both input and output word formats are described later.

MODEM (MODULATOR - DEMODULATOR)

The terminal is designed to operate on voice grade telephone circuits using frequency shift keyed (FSK) modulated signals. The demodulator section of the modem recovers the data from the FSK signal and supplies it as a digital signal to the terminal. The modulator section of the modem converts the out-going digital signal into a FSK signal for transmission over telephone circuits.

Two types of modems are supplied for use with the terminal. The PLATO IV modem is designed for use with full duplex (4 wire) circuits of up to 5 miles in length. The 202 modem is designed for use on half-duplex (2 wire) circuits such as the direct dial (DDD) telephone network or dedicated (schedule 4) circuits. Each of these modems is described in detail later in this manual.

SERIAL INPUT REGISTER (SIR)

The SIR is a 20 bit shift register which receives the data from the demodulator section of the modem. After a 20 bit word has been assembled in this register, Terminal control is signaled to begin processing the word.

DATA REGISTER (D)

This 20 bit register is the main distribution center of the terminal. Terminal control transfers an incoming word from the SIR to D and from here the word may be delivered to any of the internal registers in the terminal or to external equipment connected to the terminal.

MODE REGISTER (M)

The 4 bit M register directs the Terminal Control section in the processing of the incoming words. This register specifies the operating mode of the terminal and the write-erase conditions for the plasma panel.

X REGISTER

This 9 bit register specifies the horizontal addresses of information on the plasma panel.

Y REGISTER

This register specifies the vertical addresses of information on the plasma panel. Address X = 0, Y = 0 is located at the lower left corner of the panel.

MEMORY ADDRESS REGISTER (MAR)

The 11 bit MAR supplies character address information to the character generator.

CHARACTER GENERATOR

The character generator contains four memories each of which contains the points for plotting 64 characters. Two of the memories are read-only memories (ROM) and two are shift register memories (SRM). The SRM memories are loaded by the computer with special character or graphical data as required by the terminal user. Characters may be plotted from any memory at a rate of 180 per second. The character generator is described in more detail later.

LINE GENERATOR

The line generator contains the registers and circuits for plotting lines on the plasma panel. Lines of any length may be drawn at a rate of up to 60 lines per second. The line generator is described in more detail later.

ECHO REGISTER

The Echo register is a 7 bit register which can be loaded by the computer and its contents transmitted back to the computer (echoed) automatically.

WORD COUNT REGISTER (WC)

The 7 bit WC register maintains a record of the number of non-NOP words received by the terminal. Each time a non-NOP word is received by the terminal the WC is incremented by 1. Upon receipt of a word with a parity error, the terminal transmits the contents of the WC to the computer and enters the ABORT mode by operation. The WC contains the address of the word containing the error.

Once in the ABORT mode the terminal will refuse to accept any incoming words except for a LDM instruction. Receipt of the word will clear the ABORT mode and return the terminal to normal operation.

SERIAL OUTPUT REGISTER (SOR)

Data to be transmitted to the computer from the various sources internal and external to the terminal is entered into the SOR. From here the data is shifted into the modulator section of the modem and transmitted to the computer.

AUXILIARY EQUIPMENT

Three 15 bit output channels and two 8 bit input channels are provided to permit computer controlled operation of equipment external to the terminal.

One output channel is used to operate a random access slide selector which projects slides on the rear of the plasma panel.

A second output channel is used to operate an audio response unit which can play back a pre-recorded message to the terminal operator.

The third output channel is for use of other equipment as desired.

One input channel is used with the Touch Panel. This is an optional optical input device attached to the front of the terminal. With this device the terminal operator may enter data about objects on the plasma panel merely by pointing with his finger at the objects.

The remaining input channel is free to be used by other equipment as required.

Block Diagram

NO. GB-792

7
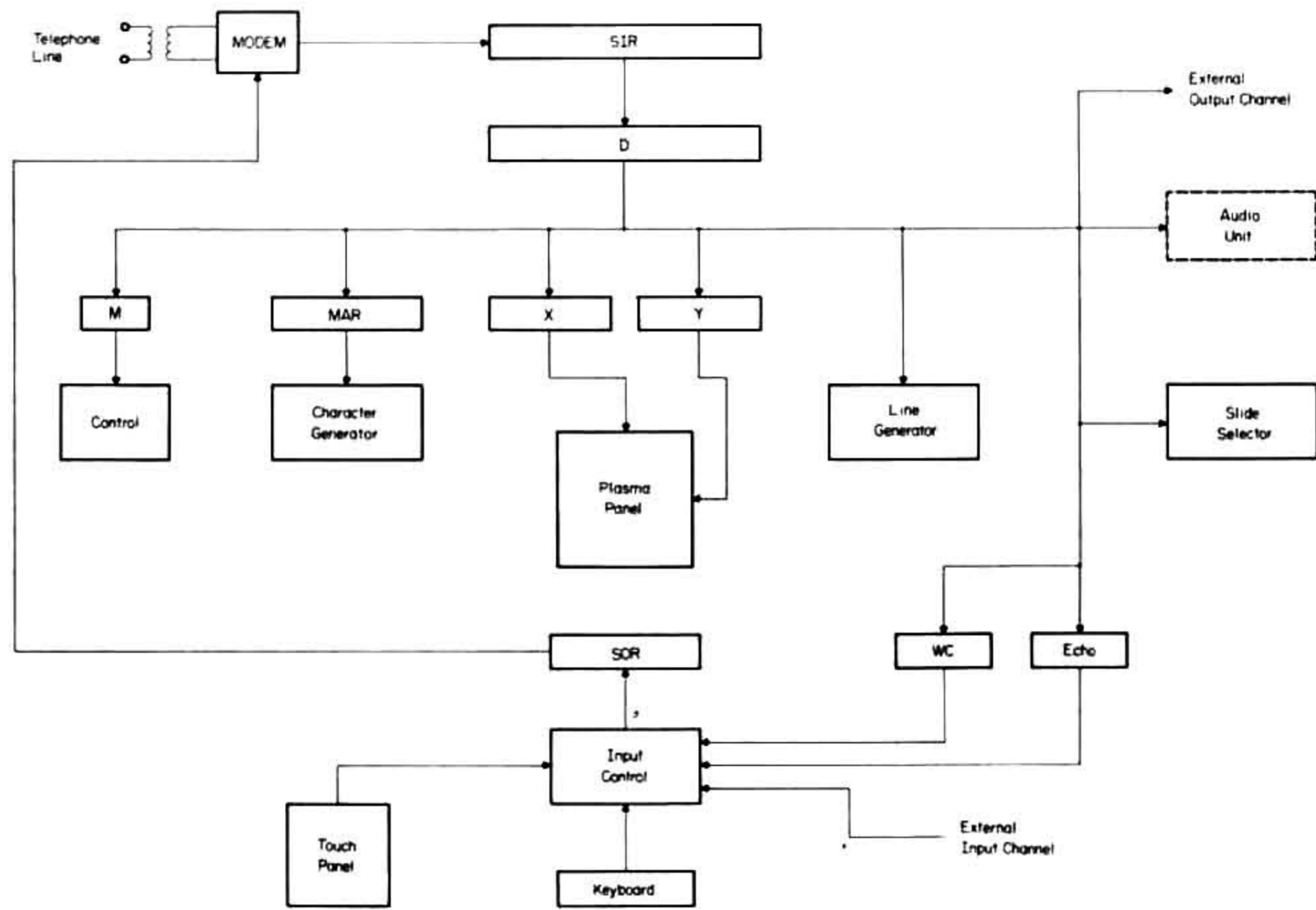
The data to be processed by the terminal consists of 21 bit words with the format shown in Figure 1. Bit 20, the message start bit, is always a "one". This bit is used to synchronize the modem. It is removed from the data by the modem before the data is supplied to the terminal and as a result is not shown in any of the word formats.
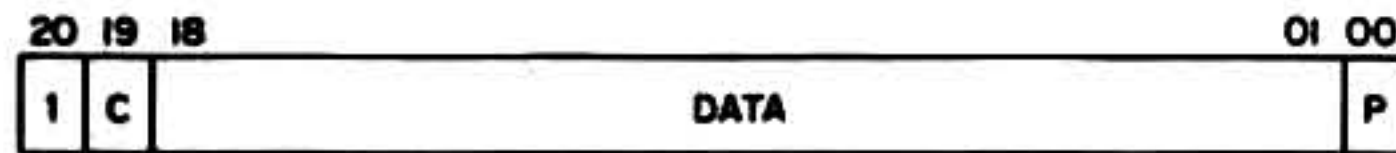

Figure 1.

Bit 00   Parity bit - odd parity
Bits 01 - 18   Data
Bit 19   Control bit - 0 = control word
                                - 1 = data word

Bit 20   Message start bit

Terminal words may be of two types; control words and/or data words. Data words (c = 1) contain the data to be processed by the terminal while control words (c = 0) are instructions used to establish certain conditions within the terminal. The control word format is shown in Figure 2.
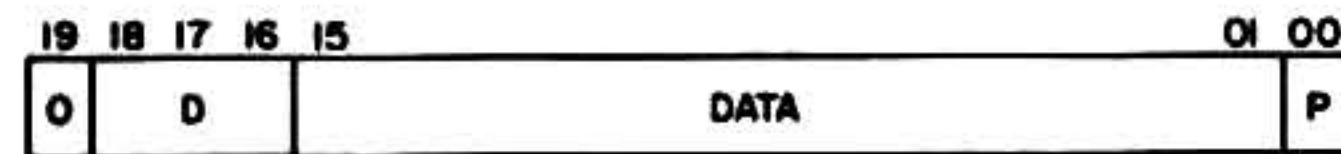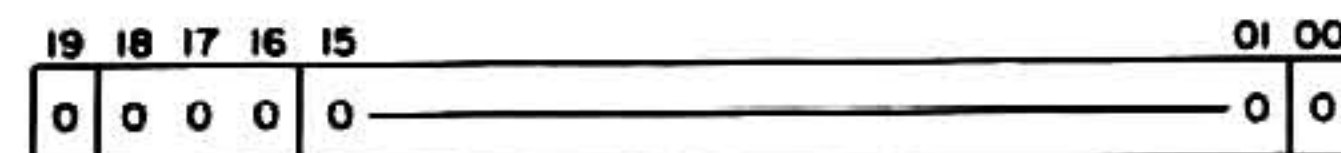

Figure 2.

Bits 01 - 15   Data
Bits 16 - 18   Destination of data within the terminal as described below.

D = 000 (NOP)

This word is a NOP (no-operation) instruction. The word is input by the terminal but the terminal condition is not altered in any way.

D = 001 (LDM) LOAD MODE

This instruction loads the Mode register (M) with bits 01-05. In addition, if bit 14 (WC) is a "1" the Word Count register will be loaded with bits 07-13. Receipt of an LDM instruction while the terminal is in the ABORT mode will load the Word Count register but will not alter the Mode register. Bit 15 is used to actuate or inhibit external devices attached to the terminal. Receipt of an LDM instruction with bit 15 = 1 will inhibit all inputs from external devices. These devices will remain inhibited until receipt of an LDM instruction with bit 15 = 0.
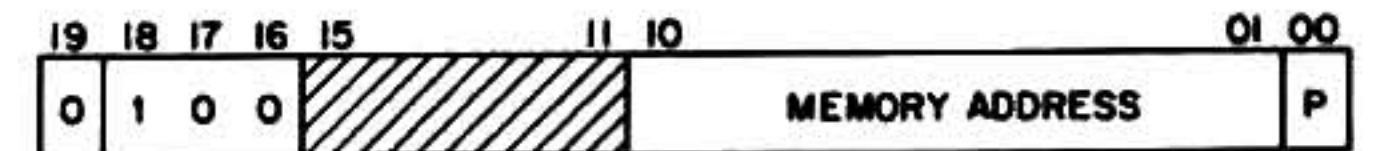
D = 010 (LDC) LOAD CO-ORDINATE
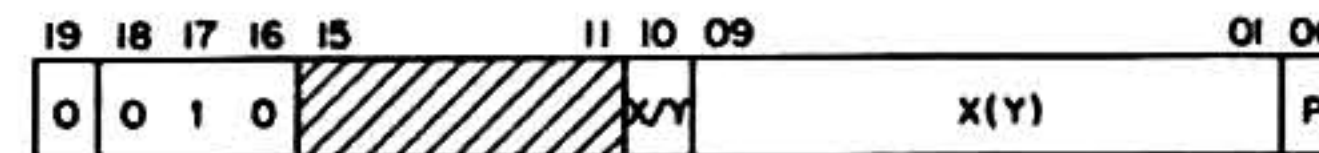
This instruction loads the X register (bit 10 = 0) or the Y register (bit 10 = 1) with bits 01-09. Bits 11-15 are unused.

D = 011 (LDE) LOAD ECHO

This instruction loads the terminal output register (SOR) with bits 01-07. This word is then transmitted back to the computer center.

D = 100 (LDA) LOAD MEMORY ADDRESS

This instruction loads the Memory Address Register (MAR) with bits 01-10. Bits 11-15 are unused. This data word specifies the first storage address to be used upon entry into a Mode 2 operation.

D = 101 (SSL) LOAD SLIDE
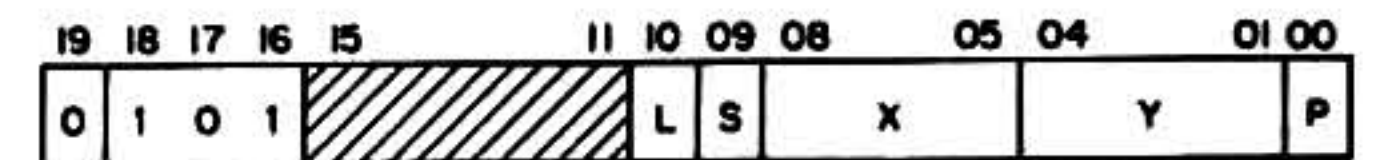
This instruction is used to operate the slide projector. Bits 01-08 select one of 256 slides for display on the plasma panel. Bit 09 controls the projector shutter. For normal operation this bit is always "0". However, if this bit is a "1", the shutter will be closed and remain closed until receipt of a load slide command with bit 09 = "0". Bit 10 controls the projector lamp. The lamp will be turned on if bit 10 is a "1" and off if bit 10 is a "0".

D = 110 (AUD) LOAD AUDIO
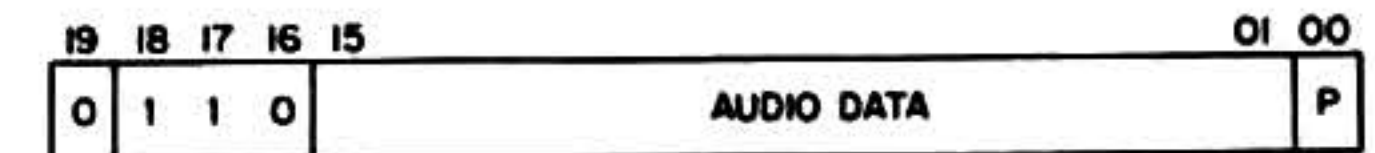
This instruction is used to control the audio response unit. The audio response unit requires two of these instructions per audio operation. The formats of each of these instructions is described below.
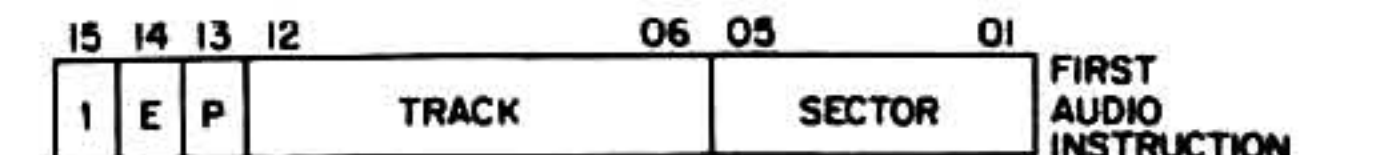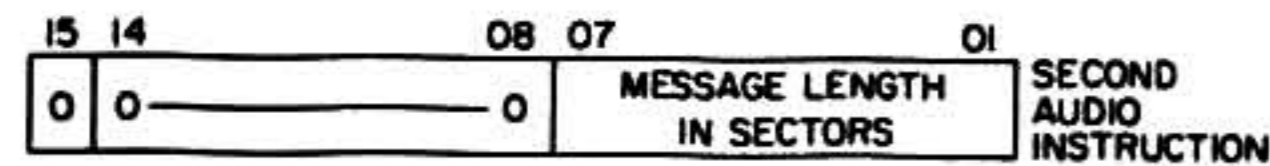
Bits 01 -12 — Specify the message starting address; bits 01-05 specify one of 32 sectors and bits 06 - 12 one of 128 tracks.

Bits 13 - 14 — Specify playback or erase as follows:

00 - erase/rec
01 - record
10 - erase
11 - play

Bit 15 — Always "1". Identifies first of two audio instructions.

15 14	08 07	01	
0	0 ——————— 0	MESSAGE LENGTH IN SECTORS	SECOND AUDIO INSTRUCTION

Bits 01 - 07 — Specify length of message in terms of sectors. One sector equals ~1/3 seconds.

Bits 08 - 14 — Unused

Bit 15 — Always "0" - identifies second audio instruction.

D = 111 (EXT) LOAD EXTERNAL CHANNEL

19 18 17 16 15	01 00	
O 1 1 1	EXTERNAL DATA	P

This instruction transfers bits 01 - 15 to any equipment attacheded to the external output channel of the terminal.

MODE WORD

For each mode of terminal operation there is an associated mode word which directs the terminal processing of incoming data. Once placed in any given mode the terminal remains in that mode until receipt of a new LDM instruction. The mode word format is shown in Figure 3.
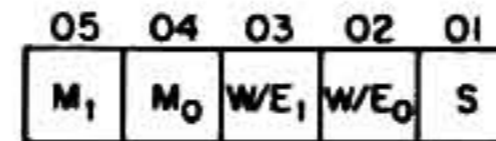
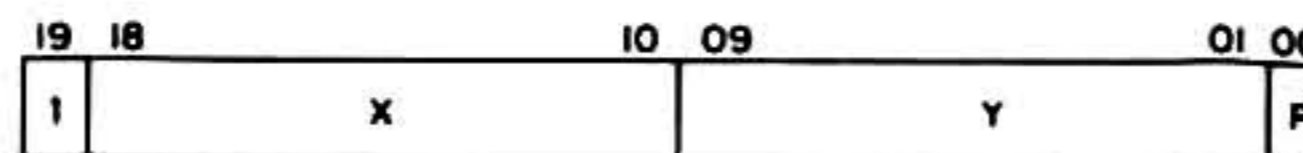| 05	04	03	02	01
M_1	M_0	W/E_1	W/E_0	S

Figure 3.

Bit 01 — Screen Command. If this bit is a "1", the entire display panel is erased at the time the Mode Word is loaded into the M register.

Bits 02 - 03 — Select write or erase function as follows:

W/E_1	W/E_0	
X	0	Erase
0	1	Write
1	1	Write; suppress all background erase operations.

Bits 04 - 05 — Specify operating mode

MODE 0

19 18	10 09	01 00	
1	X	Y	P

Mode 0 is a point plotting mode. Each mode 0 data word specifies the address of a point on the panel to be written or erased. The W/E_0 bit in the mode word determines which operation is performed.

MODE 1

19 18	10 09	01 00	
1	X_i	Y_i	P
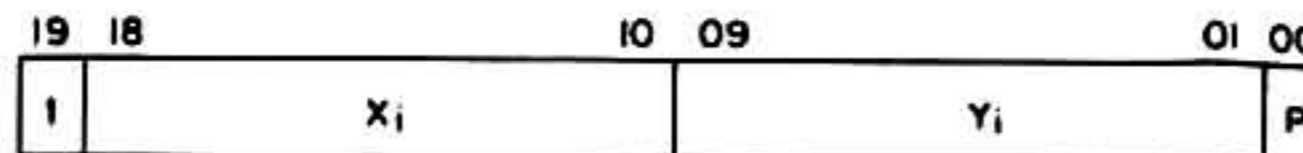
Mode 1 is a line drawing mode. Each data word specifies the terminal coordinates of a line, the origin of which is contained in the X and Y registers.

The terminal point of a given line is also interpreted as the origin of the next line. Line origins may be relocated, however, by the use of the LDC command without exiting from Mode 01.

MODE 2

19 18 17 16	01 00	
1 ////	MEMORY DATA WORD	P
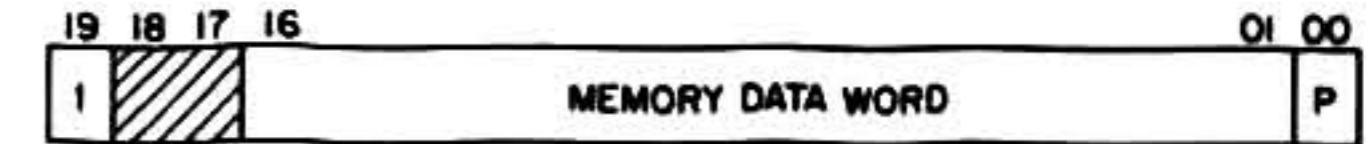
Mode 2 is a load terminal memory mode. Each mode 2 data word contains a 16 bit word to be stored in the memory location specified by the present contents of the memory address register (MAR). Up to 1024 16 bit words may be stored in the terminal. After the data has been stored the MAR is automatically incremented by 1. Thus, data may be stored sequentially in memory by transmitting only Mode 2 data words. The contents of the MAR may be changed at any time via the LDA instruction.

The data, when displayed on the panel, appears as a vertical column with bit 01 at the bottom and bit 16 at the top. Eight of these words stored at consecutive addresses comprise one character which may be displayed on the panel via Mode 3.

MODE 3

19 18	13 12	07 06	01 00	
1	CHAR 1	CHAR 2	CHAR 3	P
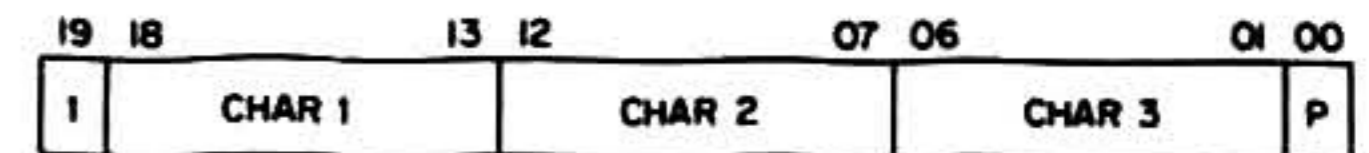
Mode 3 is a character plotting mode. The data words in this mode contain three 6 bit character codes. Four 64 character memories are provided in the terminal. Memories M_0 and M_1 are read-only memories (ROM) which contain the characters shown in Table 1. Memories M_2 and M_3 are shift register memories (SRM), each containing 512 x 16 bit words, the contents of which are loaded via mode 2. The contents of 8 consecutive addresses are displayed as one character. Al characters are displayed within an 8 x 16 matrix as shown in Figure 4. The top three and the bottom rows of the matrices for all characters from M_0 and M_1 are always unfilled.

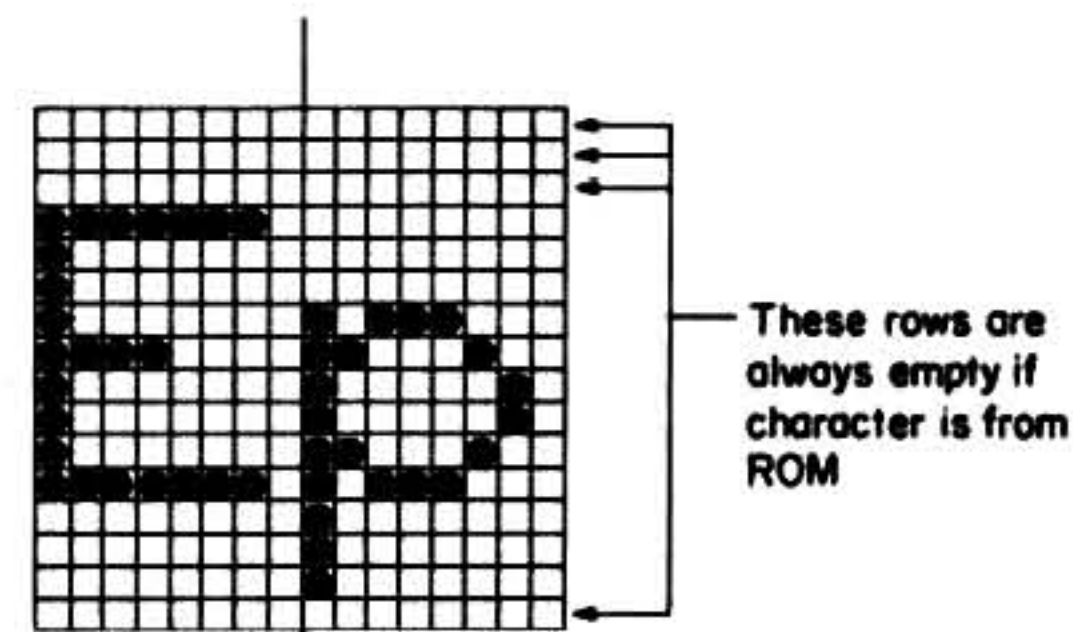| ADDRESS (OCTAL)	M0 CHAR	M1 CHAR	ADDRESS (OCTAL)	M0 CHAR	M1 CHAR
0	:	#	40	5	↑
1	a	A	41	6	→
2	b	B	42	7	↓
3	c	C	43	8	←
4	d	D	44	9	~
5	e	E	45	+	Σ
6	f	F	46	−	Δ
7	g	G	47	*	∩
10	h	H	50	/	∪
11	i	I	51	(	(
12	j	J	52	)	)
13	k	K	53	$	&
14	l	L	54	=	≠
15	m	M	55	SP	SP
16	n	N	56	,	|
17	o	O	57	.	o
20	p	P	60	↕	≡
21	q	Q	61	[	α
22	r	R	62	]	β
23	s	S	63	%	δ
24	t	T	64	×	λ
25	u	U	65	⊙	μ
26	v	V	66	'	π
27	w	W	67	"	ρ
30	x	X	70	!	σ
31	y	Y	71	;	ω
32	z	Z	72	<	≤
33	0	−	73	>	≥
34	1	..	74	—	θ
35	2	^	75	?	φ
36	3	´	76	>	\
37	4	`	77	UNCOVER	UNCOVER

Table 1. Character Codes

Figure 4.

Character write/erase is controlled by the write/erase bits in the mode word. If $W/E_0 = 1$, characters are written; if $W/E_0 = 0$ characters are erased. If $W/E_1 = 0$, the background or normally unfilled portion of each character matrix will be erased, if $W/E_1 = 1$ the background remains unaltered.

CONTROL CHARACTERS

The "uncover" code (77) is used to gain access to 12 control characters which are used to control display format in Mode 3 operations.

Upon receipt of a 77 code, the terminal interprets the next character code as a control character rather than a memory address. Following execution of the control character normal Mode 3 operations are resumed. A description of each control function is given below.

UNCOVER (77)

This code instructs the terminal to obey the next character address as a control function. If several uncover codes are sent in sequence, the first non-uncover code will be treated as the control character.

BACKSPACE (10)

This character decreases by 8 the panel x address, i.e., moves one character position to the left. A backspace over a display character does not erase the character.

TAB (11)

This character increases by 8 the panel x address, i.e., moves one character position to the right. A tab over a displayed character does not erase the character.

LINE FEED (12)

This character decreases by 16 the panel y address, i.e., moves down one character position. A line feed over a displayed character does not erase the character.

VERTICAL TAB (13)

This character increases by 16 the panel y address, i.e., moves up one character position. A vertical tab over a displayed character does not erase the character.

FORM FEED (14)

This character sets the panel address to the upper left corner (x = 0, y = 496). This is the first character position on the top line of the display. No displayed data is erased in this operation.

CARRIAGE RETURN (15)

This character clears (sets to 0) the panel x address and decreases by 16 and y address. The screen address is thus set to the first character position on the line immediately below the present line. No displayed data is erased in this operation.

SUPERSCRIPT (16)

This character increases the panel y address by 5. All characters received following this code appear as shown in Figure 5. This selection may be removed by a subscript (17) code. No data is erased in a subscript operation.
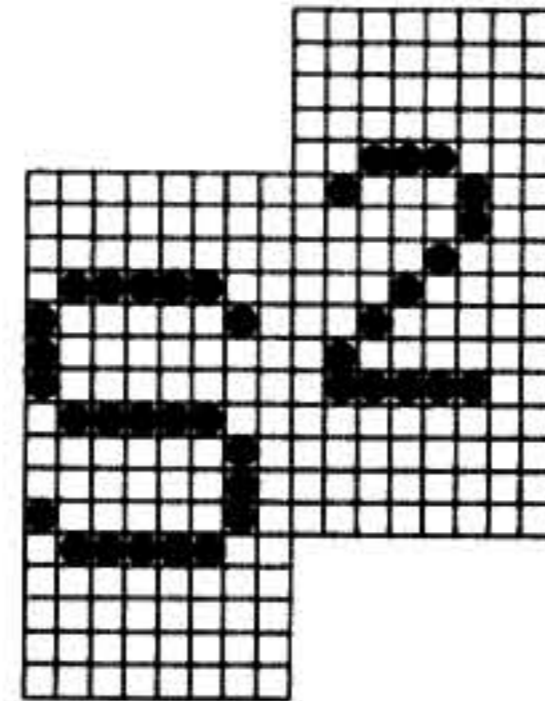
Figure 5.

SUBSCRIPT (17)

This character decreases by 5 the panel y address. All characters received following this code appear as shown in Figure 6. This character may be used to remove a superscript selection (16) and the superscript code may be used to remove this selection. No data is erased in a superscript operation.
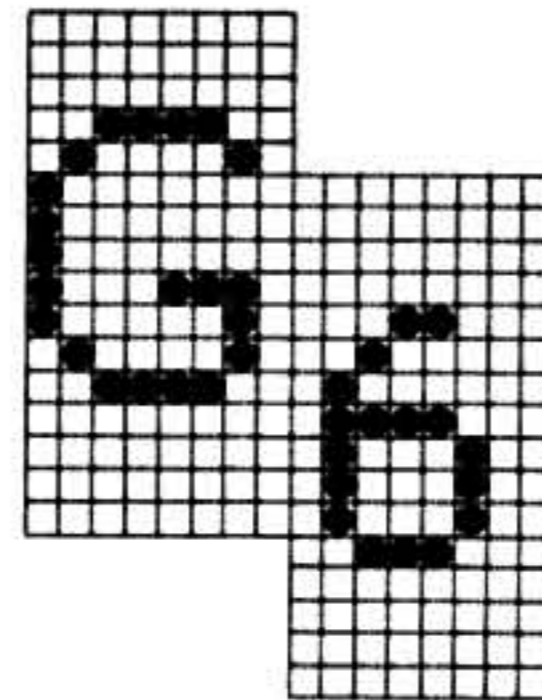

Figure 6.

SELECT M_0 (20)

This code selects character memory 0. All succeeding characters will be read from the memory until receipt of a difference memory select code.

SELECT M_1 (21)

This code selects character memory 1. All succeeding characters will be read from this memory until receipt of a different memory select code.

SELECT M_2 (22)

This code selects character memory 2. All succeeding characters will be read from this memory until receipt of a different memory select code.

SELECT M_3 (23)

This code selects character memory 3. All succeeding characters will be read from this memory until receipt of a different memory select code.

CIRCUIT DESCRIPTION

The logic circuits used in the PLATO IV terminal are implemented using standard transistor-transistor-logic (TTL) integrated circuits. A logical "one" is represented by a voltage of from +2.4 to +5 volts and a logical "zero" by a voltage of from 0 to +.4 volts.

SIGNAL NOMENCLATURE

Signal lines on the logic diagrams are provided with a label that identifies, often in a shortened form, the function which the signal performs. If the logical "one" state of the signal performs the labeled action, the label appears as, for example, CLEAR X; while if the logical "zero" state performs the action, the label appears with a bar over it; in this example $\overline{\text{CLEAR X}}$.

NAND

The NAND circuit provides a logical "zero" output if and only if all of the inputs are a logical "one". If one or more of the inputs is a logical "zero", the output will be a logical "one". NAND circuits may have from two to eight inputs. The symbol for a 2-input NAND circuit is shown is Figure 7. The N in the symbol specifies which integrated circuit package contains the circuit while i, j and k specify pin numbers on the integrated circuit package. This labeling scheme applies as well to the other logic elements to be described in the following paragraphs.
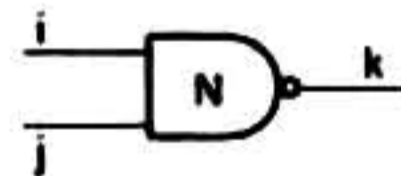
Figure 7. NAND Symbol

NOR

The NOR circuit provides a logical "zero" output if one or more of the inputs is a logical "one". If all of the inputs are a logical "zero" the output will be a logical "one". NOR circuits used in this terminal have only two inputs. The NOR symbol is shown is Figure 8.
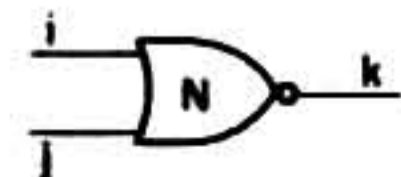
Figure 8. NOR Symbol

INVERTER

The inverter provides an output that is a logical inversion of its input. The inverter symbol is shown in Figure 9. NAND and NOR circuits may also be used as inverters by connecting all of the

Figure 9. Inverter Symbol

inputs together. Examples of these circuits are shown in Figure 10.

Figure 10. NANDs AND NORs used as inverters

WIRED - OR

Open collector TTL circuits may be paralleled to perform the AND-OR-NOT function. This paralleling of gates is often referred to as a "wired-or" or "wired-and" circuit. An example of such a circuit is shown in Figure 11. The output of this circuit will be a
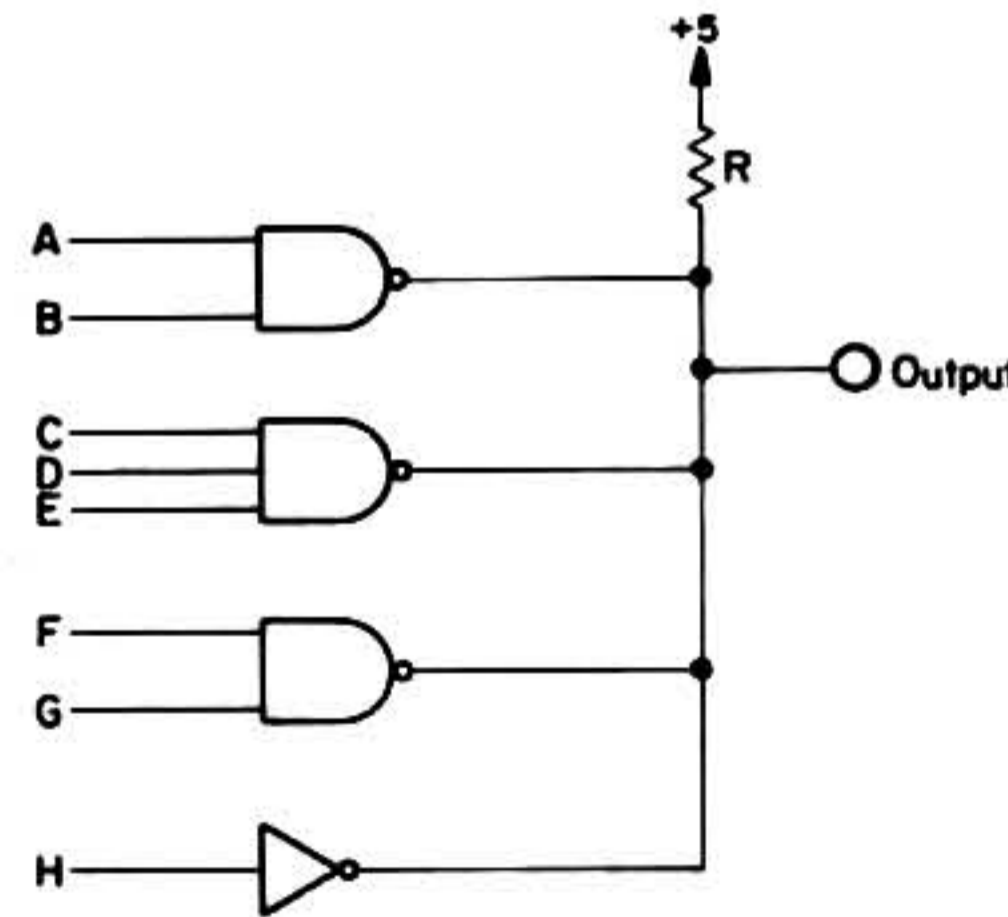
Figure 11. Wired-Or

"zero" if all of the inputs to any one of the gates are "ones". Thus if A and B are both "ones", or if C, D and E are all "ones", or if F and G are both "ones" or if H is a "one", the output will be a "zero". The output of this circuit will a "one" if one or more of the inputs to each circuit is a zero.

EXCLUSIVE OR

The EXCLUSIVE OR circuit provides a logical "zero" output if both of the inputs are logical "ones" or both are logical "zeros". If the inputs are not of the same logical state, the output will be a logical "one". The symbol for the EXCLUSIVE OR circuit is shown in Figure 12. The EXCLUSIVE OR circuit has the property that if one input is held at a logical "zero", the output will always be
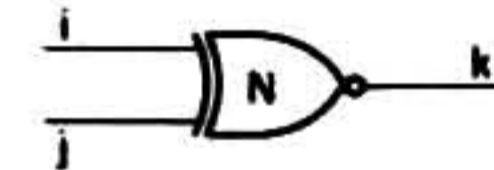
Figure 12. EXCLUSIVE OR Symbol

logically equal to the other input, while if one input is held at a logical "one", the output will always be the logical inversion of the other input.

FLIP FLOPS (FF)

The flip flop functions as a storage device which has two stable states designated as set and clear. The most basic type of flip flop is composed of two NAND circuits as shown in Figure 13. This flip flop is set when the A output is a "one" and the B output is a
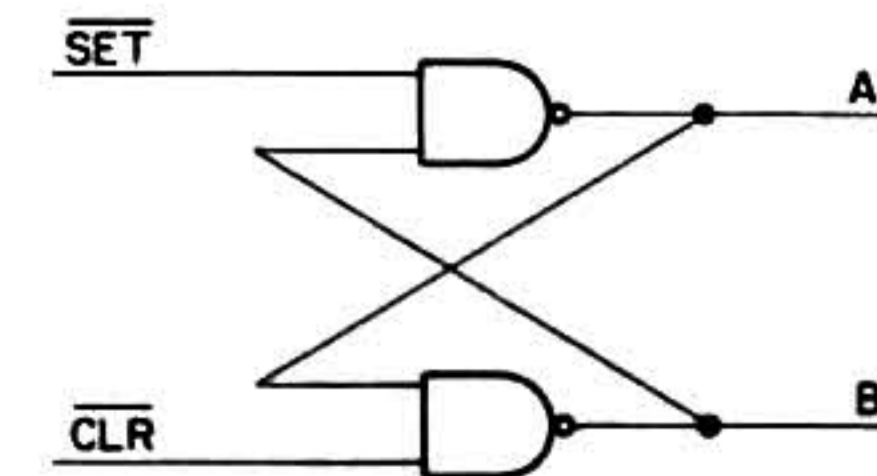
Figure 13. Simple Flip Flop

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"zero" and the flip flop is cleared when the A output is a "zero" and the B output is a "one". The flip flop is set by the occurrence of a "zero" on the $\overline{SET}$ input and cleared by the occurrence of a "zero" on the $\overline{CLR}$ input.

The Latch flip flop, shown in Figure 14, is most often used in storage registers. This flip flop is set when Q is a "one" and cleared when Q is a "zero". When the GATE input is a "one" the state
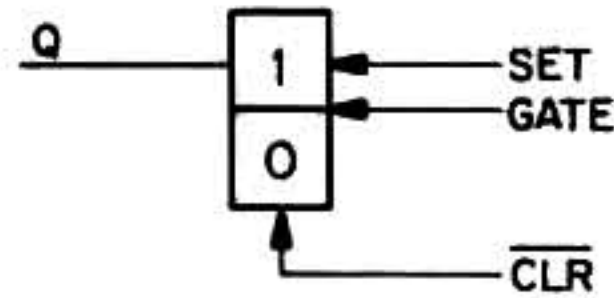

Figure 14. Latch Flip Flop Symbol

of the SET input is entered and stored in the flip flop. The flip flop is cleared by a "zero" on the $\overline{CLR}$ input. Operation of the Latch flip flop is illustrated by the waveforms in Figure 15.
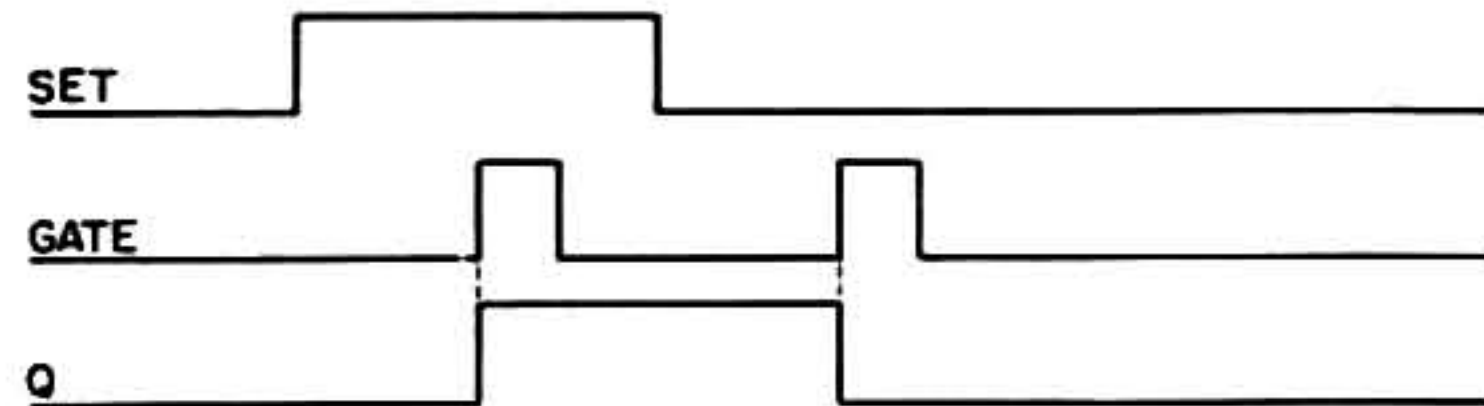

Figure 15. Latch FF Waveforms

The JK flip flop, shown in Figure 16, is used in counters, shift registers and as control elements. The state of this flip flop is determined by the state of the J and K inputs at the time the CLOCK
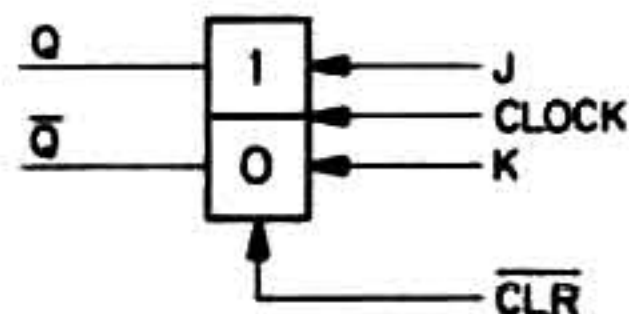

Figure 16. JK Flip Flop Symbol

input is a "one" as follows: if J and K are both "zero", the state of the flip flop remains unchanged; if J is a "one" and K a "zero", the flip flop is set; if J is a "zero" and K a "one", the flip flop is cleared; if J and K are both "one", the state of the flip flop is inverted. This last operation is referred to as "toggling" the flip flop. The flip flop may be cleared by a "zero" on the $\overline{CLR}$ input. Waveforms depicting the operations of the J K flip flop are shown in Figure 17. Note that the flip flop output changes on the trailing, i. e. "one" to "zero" transition, of the CLOCK signal.
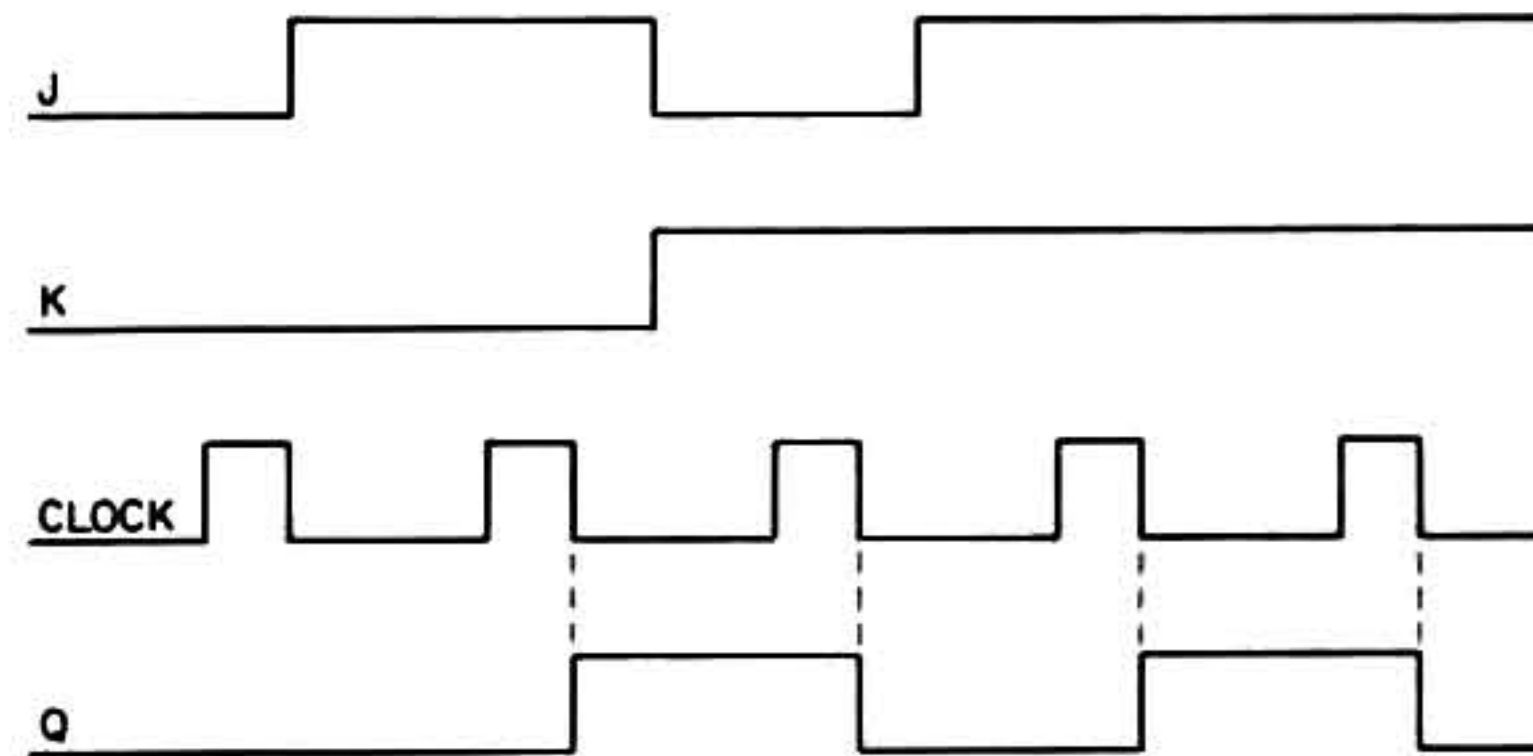

Figure 17. JK FF Waveforms

The type D flip flop, shown in Figure 18 is also used in counters, shift registers and as a control flip flop. The state of the D input is stored in this flip flop each time the $\overline{CLOCK}$ input makes a "zero"
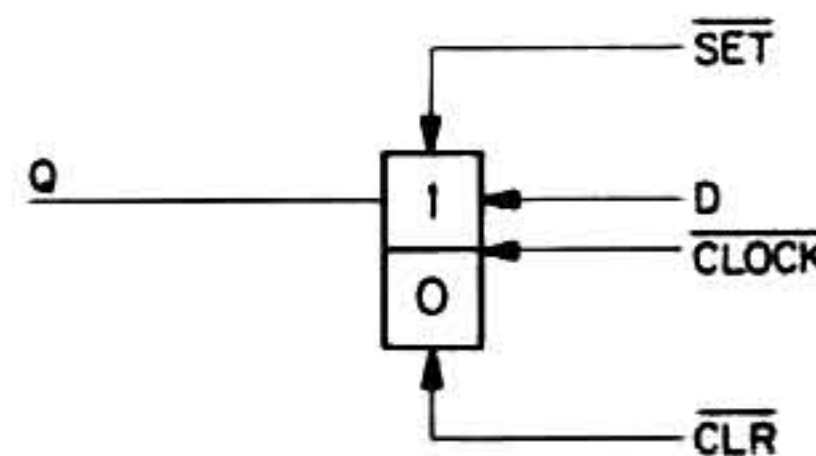
Figure 18. Type D Flip Flop Symbol

to "one" transition. The flip flop may be set by a "zero" on the $\overline{SET}$ input and cleared by a "zero" on the $\overline{CLR}$ input. Waveforms depicting the operation of this flip flop are shown in Figure 19. Note that this flip flop changes state on the "zero" to "one" transition of the $\overline{CLOCK}$ signal.
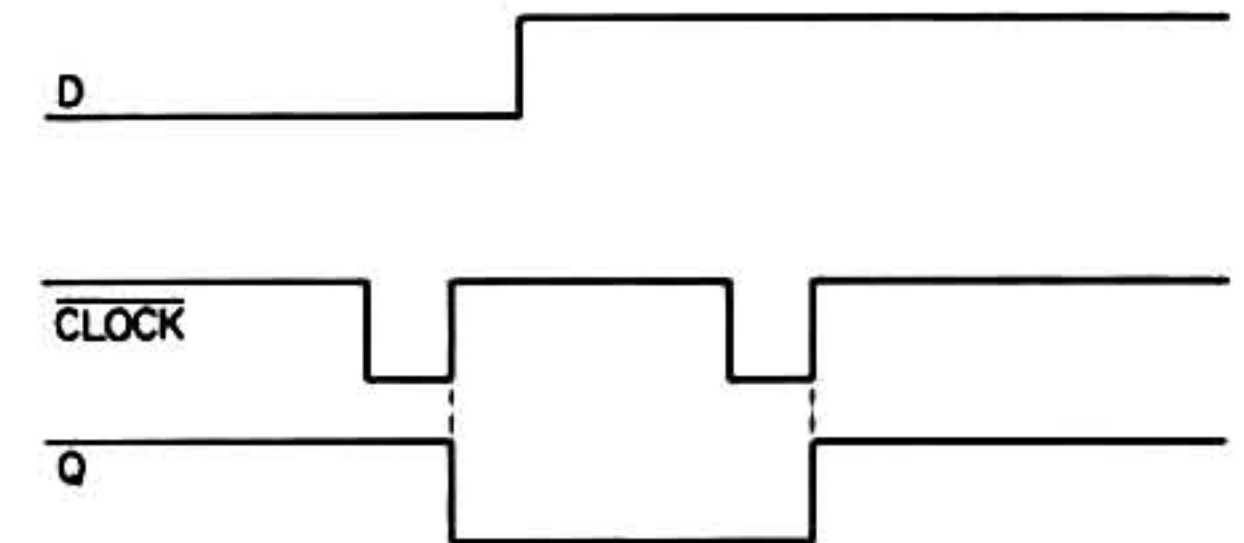
Figure 19. D Flip Flop Waveforms

DELAY CIRCUIT

Capacitive delay circuits as shown in Figure 20 are sometimes used to delay "one" signals a prescribed time. The time is fixed by the valve of the capacitor and the internal resistance of the logic circuit connected to the output of the delay circuit. The resistor (R) is used primarily to return the capacitor voltage to +5 volts at the conclusion of the delay.

Figure 20. Capacitor Delay Circuit

TEST POINTS

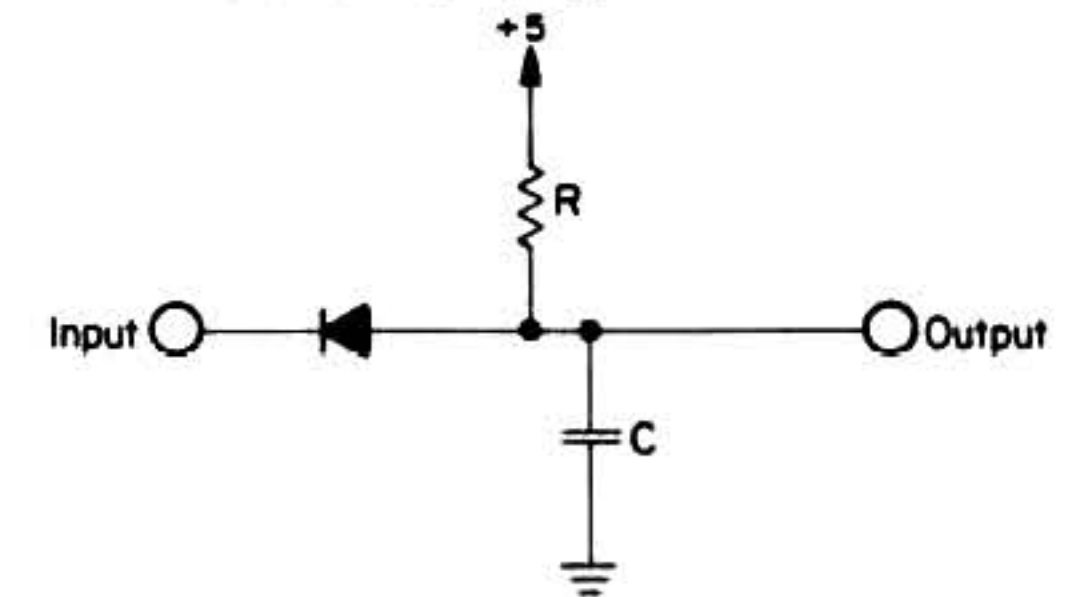Test points are provided on all printed circuit cards to permit viewing the logic signals on an oscilloscope. These test points may be numbered from 1 through 12 with test point 1 always located at the top of the card. The test points appear on the logic diagram as shown in Figure 21.

TP3 ○——————— ③———————

Figure 21. Test Point Symbol

Test points on d.c. voltages are color coded as follows:

+12V = yellow
+ 5V = red or orange
Gnd = black
- 5V = green
-12V = blue

CARD CONNECTIONS

Edge connector labels appear on the logic diagrams as shown in Figure 22. The letter A refers to the back side and B to the front (component) side of the card while the number refers to the pin

| A10 | | B27 |

Figure 22. Edge Connector Symbol

number in the connector. On all cards, A1 and A31 are always ground and A3 is always +5 VDC.

TERMINAL CONTROL

The basic control element is a shift register. Each time the INPUT DATA READY signal is generated a "one" is inserted into the first stage of the register. This "one" is then shifted through the register by the CLOCK (in some cases $\overline{CLOCK}$) signal at a 1 mHz rate until the processing of the data is completed at which time the $\overline{EXIT}$ signal is generated.

A simplified diagram illustrating the use of the shift register to generate timing signals is shown in Figure 23. The output of each flip flop in the register is combined with the CLOCK signal to generate a timing signal T_i. The diagram depicts how both positive and negative timing signals may be generated. Negative timing signals $\overline{T}_0$, $\overline{T}_1$, and $\overline{T}_2$ are generated in NAND circuits using CLOCK and the "one" side of the flip flops. Positive timing signals, T_3 and T_4 in this case, are generated in NOR circuits using $\overline{CLOCK}$ and the "zero" side of the flip flops. In the actual control circuits positive or negative timing signals are generated as required by the circuits at that time.

The combination of shift register and logic gates as shown in Figure 23 is referred to as the main timing chain or control chain and the timing signals generated by the timing chain will be referred to as time T_i. These signals are combined with other logic circuits in the terminal to generate gate signals which transfer the contents of one register to another, increment (count) registers, and to generate a variety of control signals required to process data within the terminal.

At various stages in the control chain logic circuits are inserted to permit the control to remain at that point for some number of clock times, or to jump back to some previous point in the control to repeat an operation, or to permit termination of control (generate the $\overline{EXIT}$ signal) if conditions necessitate. These circuits, for the most part, appear in the Mode 1 (line mode) and Mode 3 (character mode) control chain.

Figure 27. Simplified Control Circuit
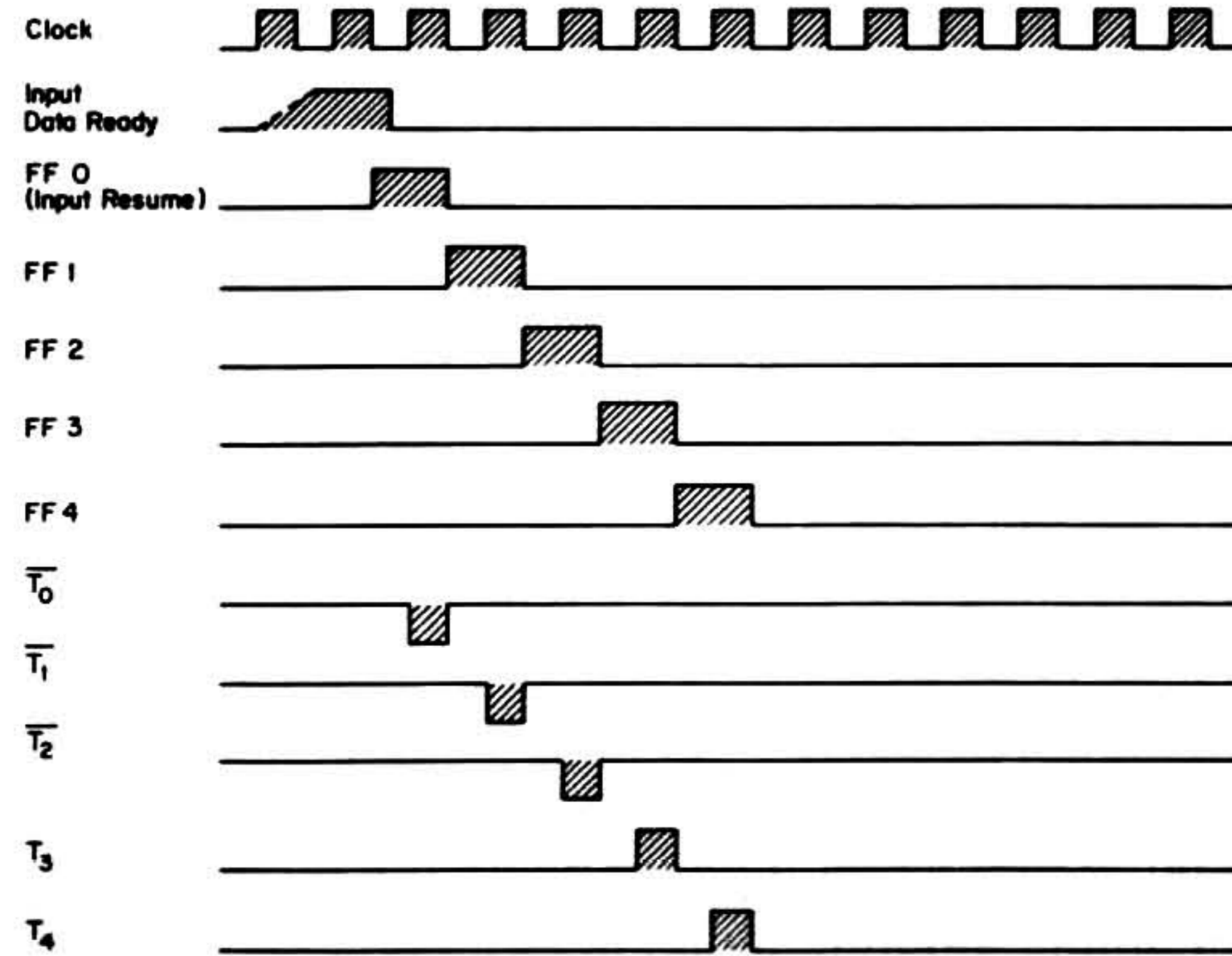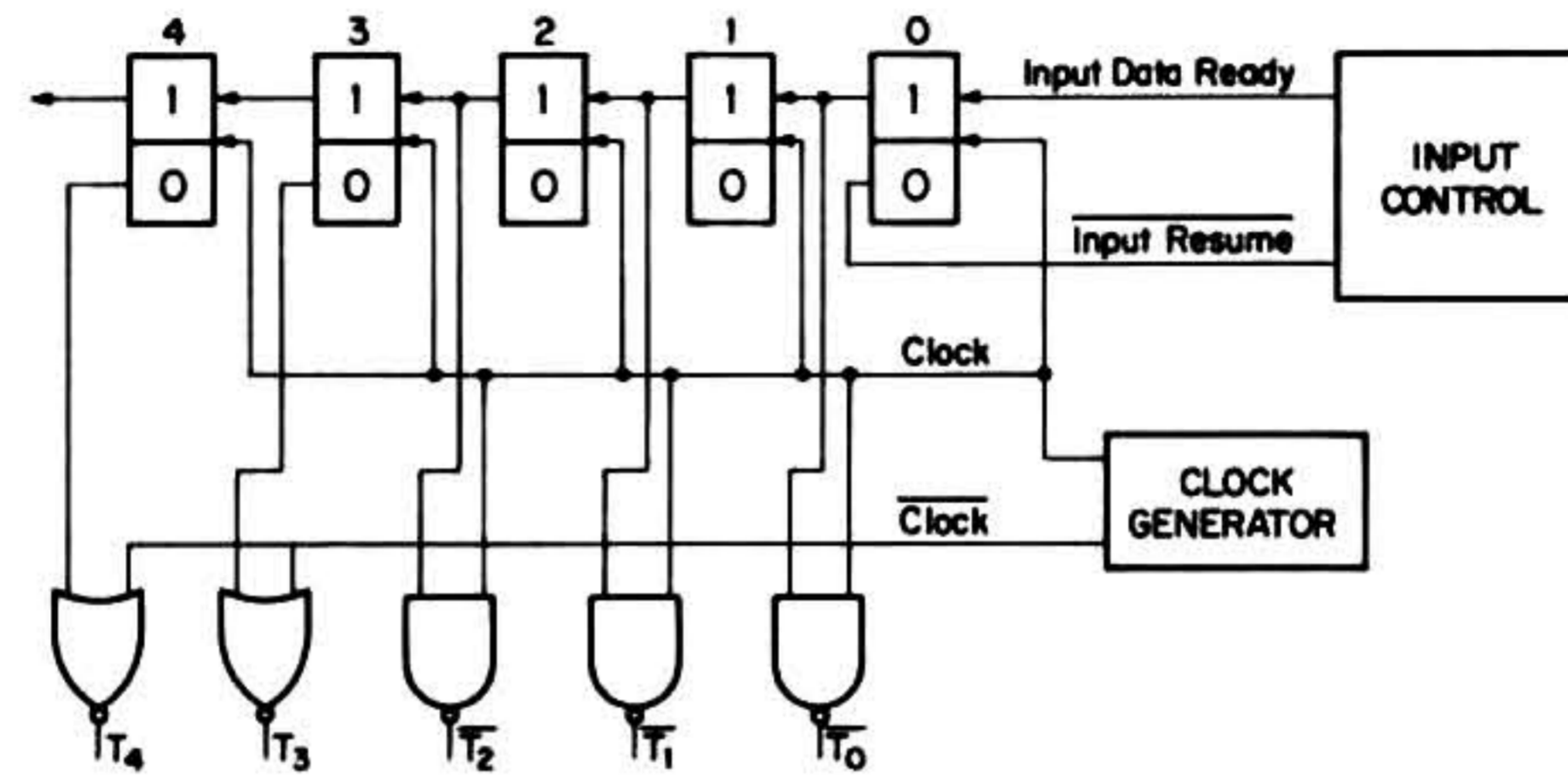
The timing diagrams identify for each clock time in the control sequence the operations which must be performed to correctly process the words received by the terminal.
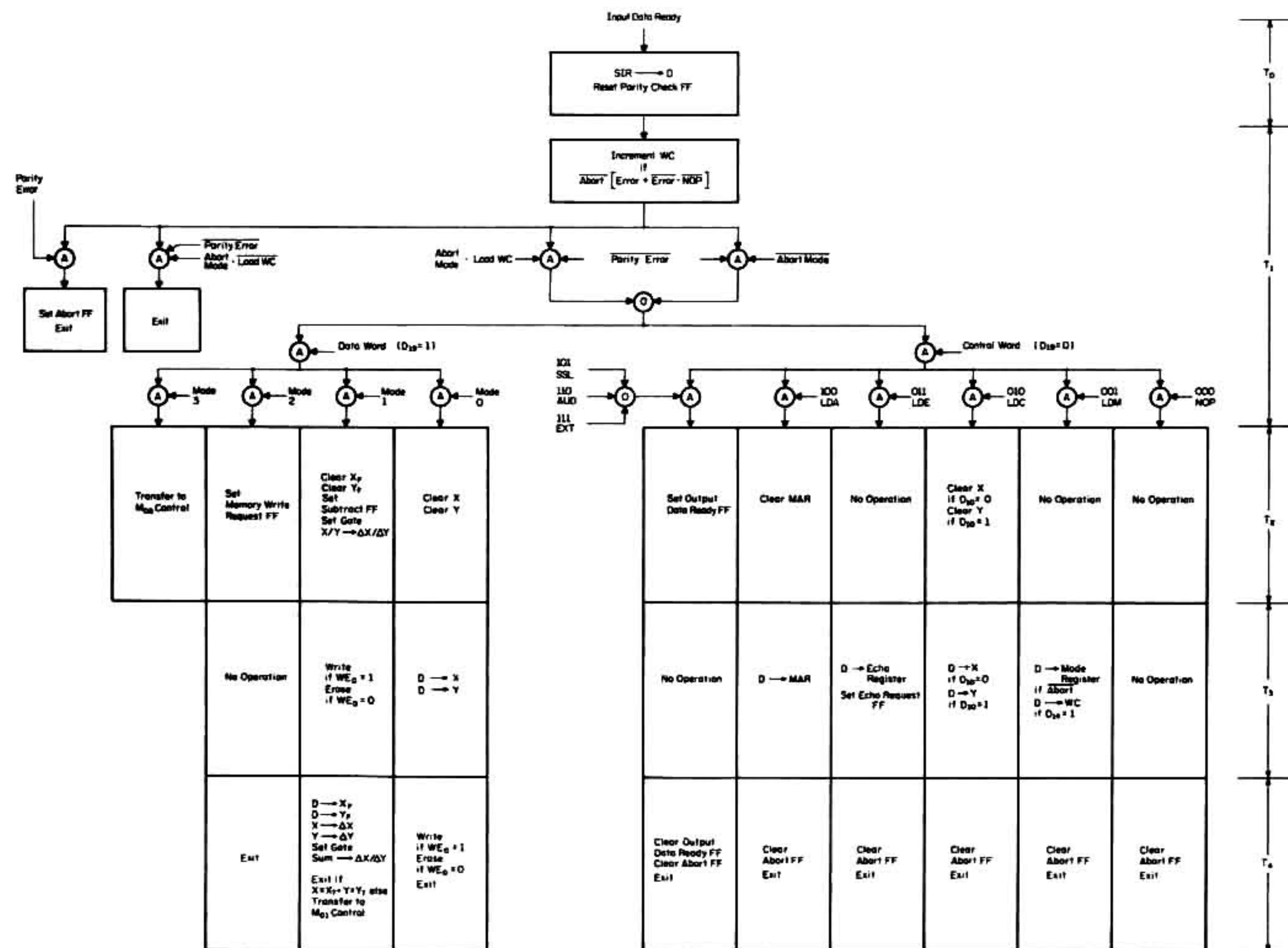
Three timing diagrams are provided; one for time T_0 through T_4; another for Mode 1 and a third for Mode 3. All words received by the terminal, with the exception of Mode 3 data words, require the use of T_0 - T_4 control for all or a part of their processing. A separate control sequence is initiated at time T_2 which processes Mode 3 words. The Mode 1 timing diagram contains timing information beginning with time T_5. With the exception of Mode 1 and Mode 3 data words, the processing of all words is completed at time T_4.

In using the timing diagrams the following points should be noted:

1. The symbol Ⓐ denotes a logical "and" condition.

2. The symbol Ⓞ denotes a logical "or" condition.

3. The above symbols are used to show the flow of control. They may or may not exist as actual logical circuits in the terminal.

4. Registers are generally denoted by one or more letters; i.e., X identifies the X Register, WC the Word Count Register; MAR the Memory Address Register.

5. The horizontal arrow → symbolizes a parallel transfer between two registers.

6. In the case of the D register transfers, only the bits of D required by the receiving register are actually transferred. Refer to the word format section for the bits required by each register.

The Mode 1 timing diagram is shown in the line generator section and the Mode 3 timing diagram is shown in the character generator section of this manual.

Input Data Ready

SIR ⟶ D
Reset Parity Check FF

Increment WC
if
$\overline{Abort}$ [Error + $\overline{Error}$ · $\overline{NOP}$]

Parity Error

Parity Error

$\overline{Abort}$ · Load WC

Abort Mode · Load WC

Parity Error

Abort Mode

Set Abort FF
Exit

Exit

Data Word (D₁₉ = 1)

Control Word (D₁₉ = 0)

101 SSL
110 AUD
111 EXT

100 LDA
011 LDE
010 LDC
001 LDM
000 NOP

Mode 3   Mode 2   Mode 1   Mode 0

Transfer to M₁₀ Control	Set Memory Write Request FF	Clear Xₚ, Clear Yₚ, Set Subtract FF, Set Gate, X/Y ⟶ ΔX/ΔY	Clear X, Clear Y
No Operation	Write if WE₀ = 1, Erase if WE₀ = 0	D ⟶ X, D ⟶ Y	
Exit	D ⟶ Xₚ, D ⟶ Yₚ, X ⟶ ΔX, Y ⟶ ΔY, Set Gate, Sum ⟶ ΔX/ΔY, Exit if X=X₀, Y=Y₀ else Transfer to M₀₁ Control	Write if WE₀ = 1, Erase if WE₀ = 0, Exit	

Set Output Data Ready FF	Clear MAR	No Operation	Clear X if D₁₈ = 0, Clear Y if D₁₈ = 1	No Operation	No Operation
No Operation	D ⟶ MAR	D ⟶ Echo Register, Set Echo Request FF	D ⟶ X if D₁₈ = 0, D ⟶ Y if D₁₈ = 1	D ⟶ Mode Register if $\overline{Abort}$, D ⟶ WC if D₁₈ = 1	No Operation
Clear Output Data Ready FF, Clear Abort FF, Exit	Clear Abort FF, Exit	Clear Abort FF, Exit	Clear Abort FF, Exit	Clear Abort FF, Exit	Clear Abort FF, Exit

T₀
T₁
T₂
T₃
T₄

T₀ - T₄ Timing Diagram

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The line generator contains two identical sections; one for computing the x coordinates and one for computing the y coordinates of a line.

Each section contains:

1. A 9 bit final coordinate register (X_f, Y_f),

2. a 9 bit increment register (Δx, Δy),

3. a 9 bit adder for adding or subtracting the contents of the increment register to and from the contents of the final coordinate register,

4. gating circuits for entering information into the final coordinate register from the D register or the adder,

5. gating circuits for entering information into the increment register from the present coordinate registers (X,Y) or the adder,

6. gating circuits for supplying the contents and the complement of the contents of the increment register to the adder,

7. gating circuits for incrementing or decrementing the X and Y registers,

8. a comparison circuit which compares the contents of the final coordinate register with the contents of the D register.

The following is a description of line generator operation as shown in the T_0 - T_4 and Mode 1 timing diagrams.

Time 0   Terminal control loads the word into the D register. The upper half of this word specifies the x coordinate (x_t) and the lower half specifies the Y coordinate (y_t) of the end point of a line.

Time 1   An error check is made on the word, the WC is incremented and control continues in Mode 1.

Time 2   The final coordinate registers (X_f and Y_f) are cleared. The gating circuits on the adder inputs are set to receive the complement of the increment registers (Δx and Δy). The gating logic on the input to the increment registers is set to receive the contents of the X and Y registers.

Time 3   The point on the plasma panel specified by the contents of the X and Y registers is written, if in write mode, or erased if in erase mode.

Time 4   The upper 9 bits of the D register are transferred to the X_f register and the lower 9 bits to the Y_f register. The contents of the X and Y registers are transferred to the Δx and Δy registers, respectively. The gating logic on the input to the increment registers is set to receive the output of the adder. At this time, if the contents of the D register are equal to the contents of the X and Y registers, the line drawing process is terminated. This is the trivial case of drawing a line of 0 length (end point address equals starting point address). In the more general case, the process continues with the next step.

Time 5   The output of the adders is transferred to the increment registers. This operation enters the quantities X_f-X and Y_f-Y into the ΔX and ΔY registers. The X and Y direction flip flops X_D and Y_D are set to "0" if overflow occurs in the adders (ΣX_9 = 1 or ΣY_9 = 1 respectively). If no overflow occurs the flip flops are set to "1". These flip flops indicate the direction the X and Y registers must be advanced in the line drawing process.

Time 6   The final coordinate registers, X_f and Y_f, are cleared.

Time 7   The output of the adder is transferred to the increment registers, Δx and Δy, if the corresponding direction flip flop X_D or Y_D = 0. No operation occurs to an increment register if the direction flip flop is "1". This operation complements the quantity in an increment register if it is negative.

Time 8   The final coordinate registers X_f and Y_f, are both set equal to 1/2 (100000000). The gating circuits on the adders are set to receive the contents of the increment registers. (Set ADD) The increment registers are set to shift.

Time 9   The contents of both increment registers are shifted left until one or both registers has a "1" in its most significant bit (Δx_8 or Δy_8). Following this step, the contents of the line generator registers are:

$$(\Delta x) = \frac{x_t - x_o}{2^{9-n}} \qquad (\Delta y) = \frac{y_t - y_o}{2^{9-n}} \qquad (X_f) = (Y_f) = \frac{1}{2}$$

where x_t and y_t are the end points of a line just received by the terminal, x_o and y_o are the initial contents of the X and Y registers in the terminal, and n is the number of left shifts performed in this step.

Time 10   The contents of the increment registers are added to the contents of the final coordinate registers and the sum placed into the final coordinate registers:

$$x_{f_{i+1}} = x_{f_i} + \Delta x \qquad y_{f_i} = y_{f_i} + \Delta y$$

If overflow occurs in the adders, Σx_9 or Σy_9 = 1, the corresponding X or Y register is incremented if its direction flip flop is a "1" or decremented if it is "0".

Time 11   The point on the panel specified by the present contents of the X and Y registers is written, if in write mode, or erased if in erase mode. The contents of the X and Y registers are compared to the contents of the D register (x_t and y_t), if these quantities are not equal, control returns to step 10; if they are equal the line drawing process is terminated.

The line drawing process may be described by the following equations:

$$x = x_o + \frac{x_t - x_o}{2^{9-n}} \quad T + \frac{1}{2}$$

$$y = y_o + \frac{y_t - y_o}{2^{9-n}} \quad T + \frac{1}{2}$$

where:

x_o, y_o = initial contents of X and Y registers.

x_t, y_t = terminal coordinates of line as specified by contents of D register.

n = number of shifts required in Time 9

T = number of passes through Time 10 above.

The quantity 1/2 is added to effect automatic "round off".

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Line Generator Block Diagram

The character generator contains four 512 word memories, two of which are read only memories (ROM) and two of which are shift register memories (SRM). The ROM memories, designated M_0 and M_1, contain data for the characters shown in Table 1 while the SRM memories, designated M_2 and M_3, contain data which is loaded by the computer according to the needs of the terminal user.

The character generator as shown in the block diagram contains:

1. Two ROM and two SRM memories.
2. The 11 bit memory address register (MAR).
3. Gating logic for entering data into the MAR from the D register.
4. The character counter.
5. Memory output logic.
6. Load-circulate logic for the SRM.
7. The SRM address register and comparison circuit.
8. A 16 line to 1 line bit multiplexor (MPX).
9. A 4 bit scanner which operates the MPX.
10. Mode 03 control.
11. Non plot control.

MAR

Bits A_9 and A_{10} specify which of the four memories is to be used. These bits are set by the memory select codes described previously in the Word Format section. Bits A_3 through A_8 specify one of 64 character addresses within a memory. Bits A_0 through A_2, the column select bits, specify one of 8 columns (words) of data which compose a character.

GATING LOGIC - CHARACTER GENERATOR

The gating logic on the input to the MAR selects which of the 3 six bit character codes specified by a Mode 3 word and held in the D register is to be loaded into bits $A_3 - A_8$.

This logic is also used to load the 10 bit store address specified by a LDA control word into bits $A_0 - A_9$. In this operation A_{10} is always set to "one".

The character counter specifies to the gating logic which bits of the D register are to be loaded into the MAR.

MEMORY OUTPUT LOGIC

This circuit selects which memory outputs are to be supplied to the bit multiplexor.

SCANNER - BIT MULTIPLEXOR (MPX)

The scanner and PMX are used to specify to Mode 3 control the contents of each bit of the character data words. Figure 24 illustrates the direction of the scanning sequence. This is also the sequence in which the character is plotted on the plasma panel.

MODE 3 - CONTROL

Mode 3 control generates the timing signals required to operate the character generator. The Mode 3 timing diagram illustrates the sequence of operations used to process each Mode 3 data word.

A six bit character code is loaded into $A_3 - A_8$ of the MAR and bits $A_0 - A_2$ are set to "zero". The word specified by this address is read from memory and supplied to the bit multiplexor where it is scanned and displayed on the panel. The column select bits are then incremented by one and a new word is read from memory and displayed. These operations continue until 8 successive 16 bit words have been read from memory and plotted on the panel.

After a character has been processed, the character counter is incremented and the next character is processed. This sequence continues until all 3 characters in a Mode 3 word have been processed.

NON-PLOT CONTROL

Non plot control is used to process the Mode 3 control characters. These characters are not displayed on the plasma panel; they alter the contents of the X and/or Y registers or bits $A_9 - A_{10}$ of the MAR. Operation of this control is described by the Non-Plot timing diagram.

SRM CONTROL

Each SRM memory contains sixteen 512 bit shift registers, one stage from each of which is shown in the Character Generator block diagram.

Each stage contains:

1. A 512 bit shift register.
2. Load-circulate logic to enter data into or circulate data already in the shift register.
3. Logic for reading data from the shift register.
4. A flip flop for holding data read from the shift register.

The SRM control circuit consists of a 9 bit address counter which specifies the address of the word appearing at the output (and input) of the shift register and a comparison circuit which compares the contents of this counter with the contents of the MAR.

During Mode 2 operations the SRM control generates the SELECT 0-511 or SELECT 512-1023 signal when the MAR address is equal to the SRM address. These signals allow data to be entered into the appropriate shift register by the load-circulate logic.

During Mode 3 operations, if the SRM is selected, the SRM control generates the GATE SRM signal when the MAR address is equal to the SRM address. This signal stores the data at the output of the shift register (selected by A_9) in the flip flop. This data is then supplied to the bit multiplexor for processing.
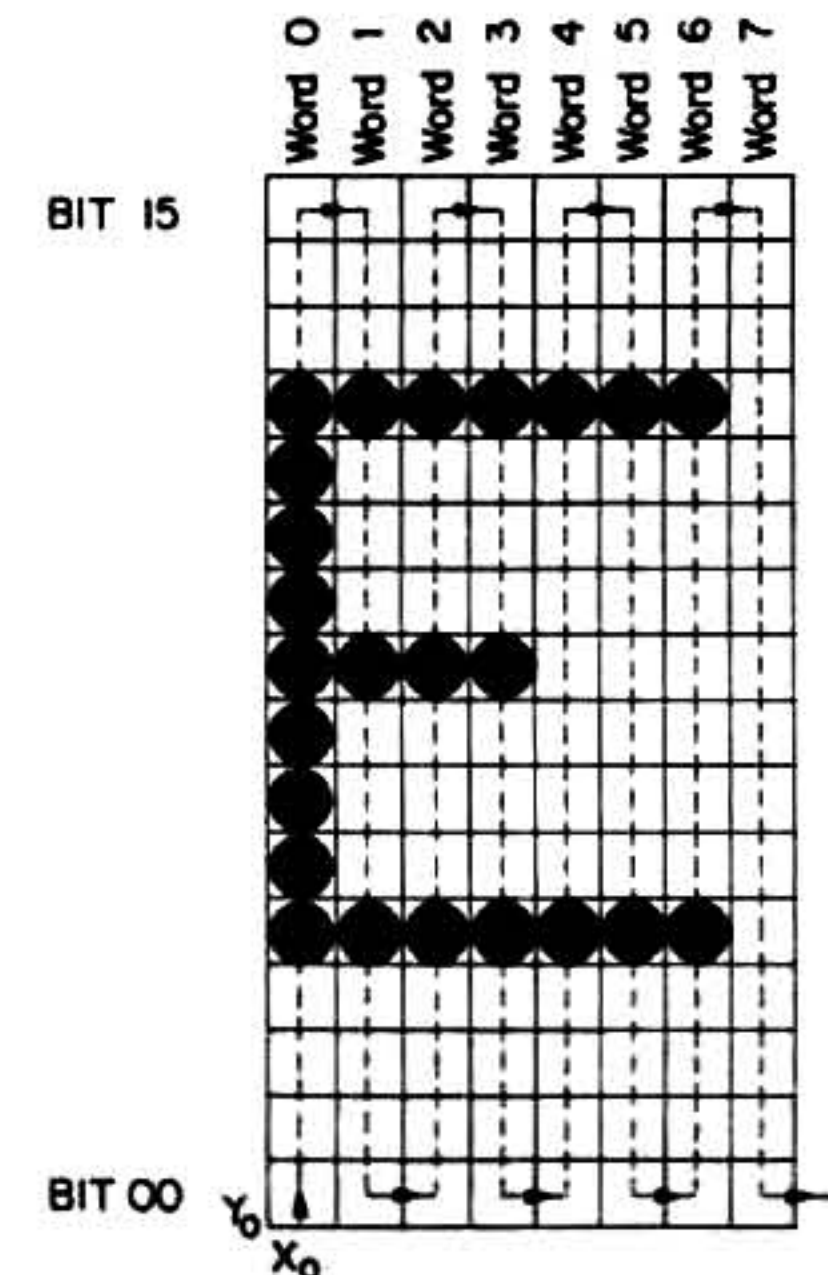

Figure 24. Character Scan Sequence

Mode 3 Timing Diagram

Character Generator

NO. GB-790

GENERAL

This card contains the master oscillator (clock) circuit, the write and erase circuits, and the timing circuits which generate times T_0 through T_4.

CLOCK

Transistors Q_1, Q_2, Q_3 and half of circuit U13 comprise a 1 mHz oscillator which generates the CLOCK signal used throughout the terminal. The CLOCK and CLOCK signals are supplied to the other cards in the terminal by circuit U12. The CONT. CLOCK signal is supplied only to card 14 (SRM Control).

Half of circuit U13 and U6 convert the 1 mHz clock signal into two 500 kHz signals and supplies these signals to the shift register memory (SRM) clock driver circuits. Transistors Q_4, Q_5, Q_6 and Q_7 supply the ϕ_2 CLOCK signal and Q_8, Q_9, Q_{10} and Q_{11} supply the ϕ_1 CLOCK signal to the SRM on card 3.

INPUT COUNTER

Circuit U9 and half of U17 comprise a 5 bit counter which counts the MODEM SHIFT pulses generated in the modem. After 20 shift pulses have been received, the INPUT DATA READY signal is generated at U10 pin 8. This signal indicates to the main timing chain that a 20 bit word has been assembled in the SIR and that the terminal may commence processing the word. The main timing chain responds to the INPUT DATA READY signal with the INPUT RESUME signal which clears the bit counter removing the INPUT DATA READY signal and resets the modem with the RESET MODEM signal.

PARITY CHECK CIRCUIT

The parity check circuit is composed of flip flop U17 and circuit U2. Each time a "one" appears in the data stream the PARITY CHECK flip flop is toggled. An error is present in the word received if this flip flop is a "one" when the INPUT DATA READY signal is initiated. The PARITY CHECK flip flop is reset, if it is a "one", at clock time T_0 from the main timing chain.

TIMING AND LOGIC CIRCUITS

Time T_0 is generated at U11 pin 13, time T_1 at U15 pin 13, time $\overline{T_2}$ at U17 pin 6, time $\overline{T_3}$ at U17 pin 8 and time $\overline{T_4}$ at U7 pin 11. These signals are used to process all control words (D_{19} = 0) and all data words (D_{19} = 1) with the exception of Mode 3. If a Mode 3 word is being processed, control is transferred, at time T_1, to Mode 3 control by the M_{03} TRANSFER signal at U15 pin 4.

In the processing of Mode 1 words, control is transferred, at time T_4, to Mode 1 control by the M_{01} TRANSFER signal at U8 pin 6.

ABORT MODE

At time T_1, if the PARITY ERROR signal is a "one", the ABORT flip flop (circuit U21) is set and the EXIT signal is generated at pin 10 of U4.

WRITE/ERASE CIRCUITS

Flip flop U18 generate the WRITE REQUEST and ERASE REQUEST signals to the plasma panel. These flip flops are set by the WRITE and ERASE signals which originate throughout the control section.

The plasma panel responds to the WRITE (or ERASE) REQUEST by removing the READY signal. This action sets the PANEL BUSY flip flop (U19) and removes the REQUEST signal by clearing the write and erase flip flops. When the panel has completed the requested operation, the READY signal is returned to "one". (A write or erase operation requires 20 μ sec.)

The CLOCK (and CLOCK) signals are inhibited at U12 pins 1, 2 and 5 while the write or erase or PANEL BUSY flip flops are set. This action suspends terminal operations until the panel has completed the requested operation.

The timing diagram for WRITE (ERASE) operations is shown below.

23
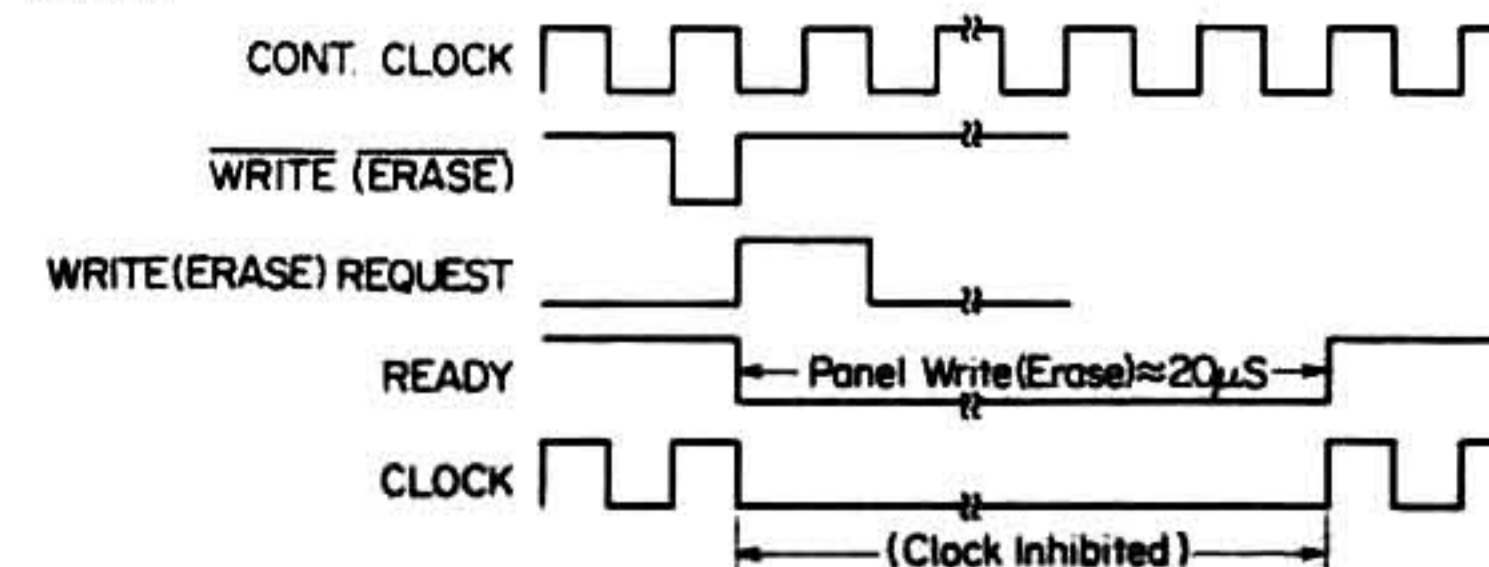
(Serial No. Above 261)

The major differences between this card and the one on the
previous page are:

1.   The removal of the SRM clock-driver circuit which is
     relocated on card A3.

2.   The addition of the auto-reset circuit (circuit U3)
     which automatically initializes the terminal upon
     turn-on.

3.   The addition of the serial output interfan circuits
     (circuits U6 - U12) for operating the AUDIO and EXT OUT
   channels. The use of these circuits eliminates card A4.
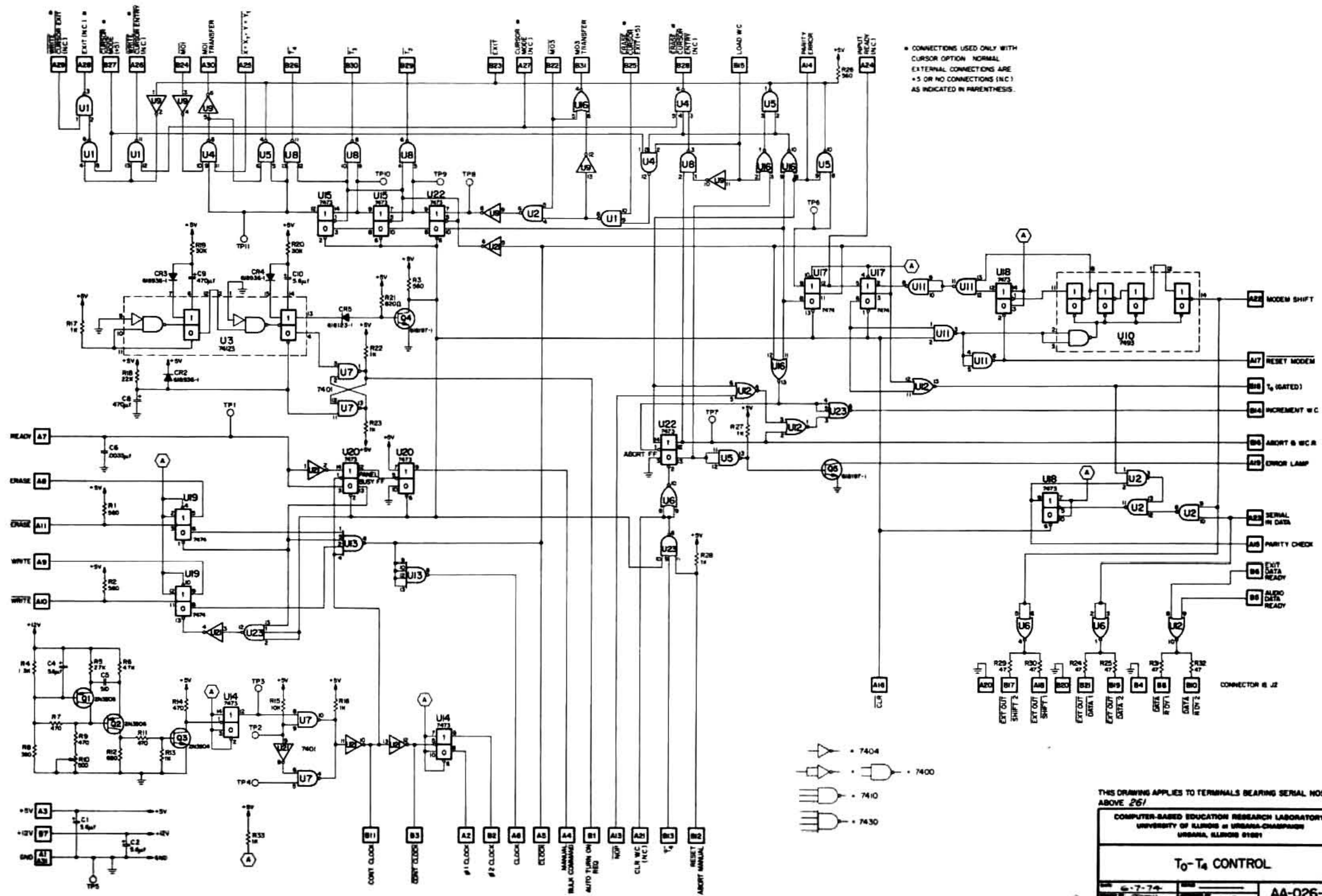
25

SRM

This card contains the shift register memory (SRM) which is used to store the data for characters in memories M_2 and M_3. The SRM is organized as two 512 word by 16 bit memories. Circuits U9 through U24 comprise the shift register. Each of those circuits is a dual 512 bit shift register. (These circuits may be either Intel 1403 or Signetics 2503). One register in each of these circuits contains bit i for all words from address 0 through 511 while the other contains bit i for all words from address 512 through 1023.

Data to be stored in the SRM is supplied by the D register (card 7). Circuits U1 through U8 are used to enter data into the SRM and to circulate the data already stored. The memory select lines for each memory, SELECT 0-511 and SELECT 512-1023 specify whether new data is to be entered into or previously stored data is to be circulated. If a memory select line is a "zero", data is circulated while if the select line is a "one" new data is entered into the SRM. The memory select lines originate on card 14.

Circuits U25 through U28 specify from which memory data is to read. If bit 9 (A_9) of the memory address register (MAR) on card 14 is a "zero", data will be read from M_2 while if A_9 is a "one" data, will be read from M_3.

The data read from the SRM is stored in a 16 bit register composed of circuits U29 and U30. The data is stored in this register by the GATE SRM signal (pins B20 and B21) which originates on card 14.

The outputs of this register are supplied to card 13.
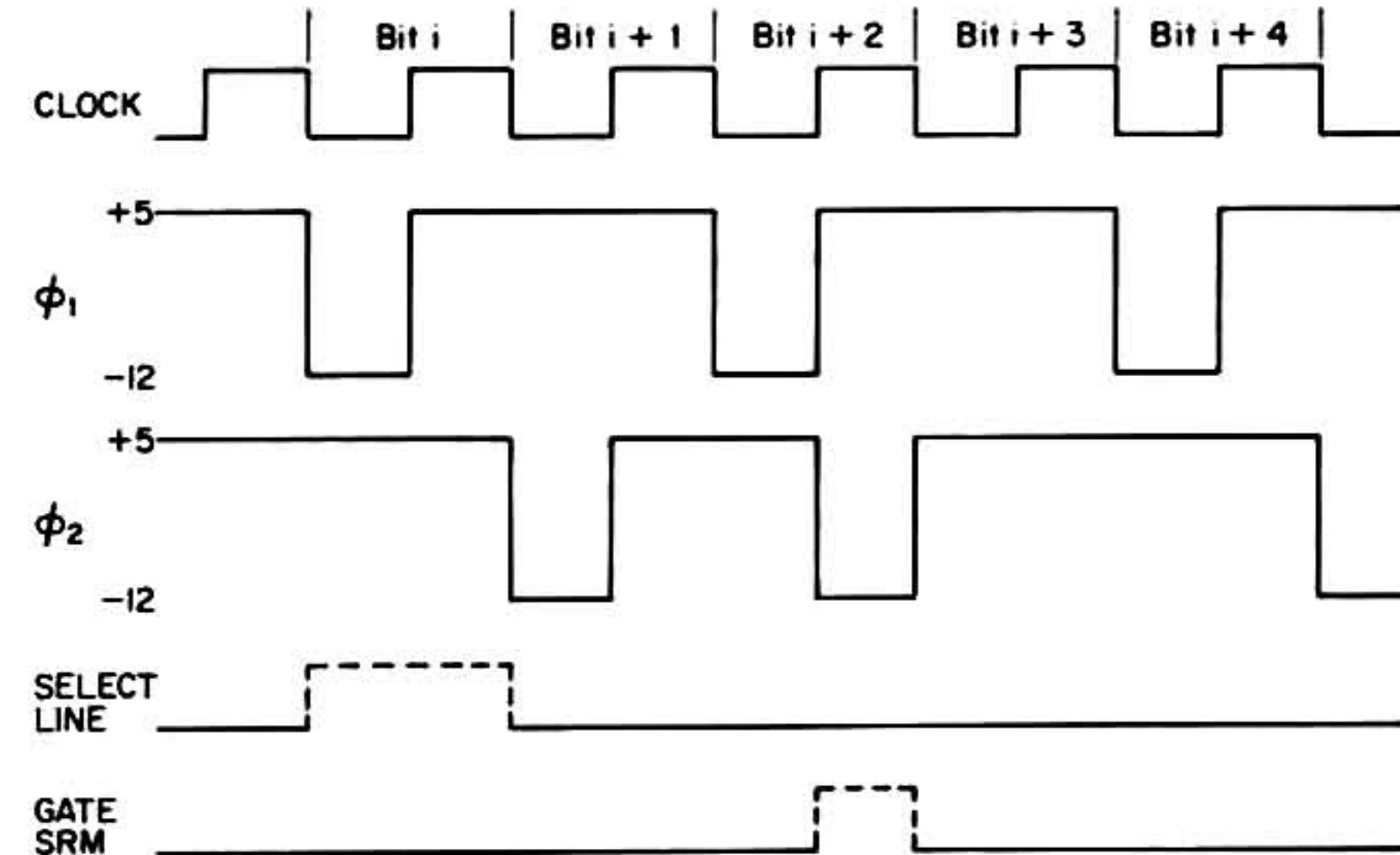
SRM Timing Diagram
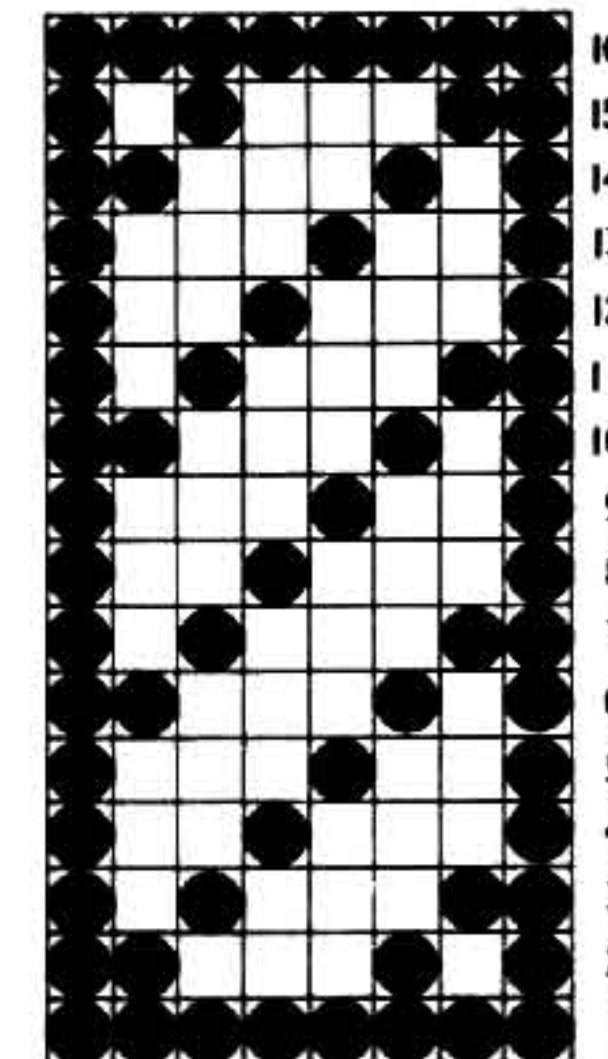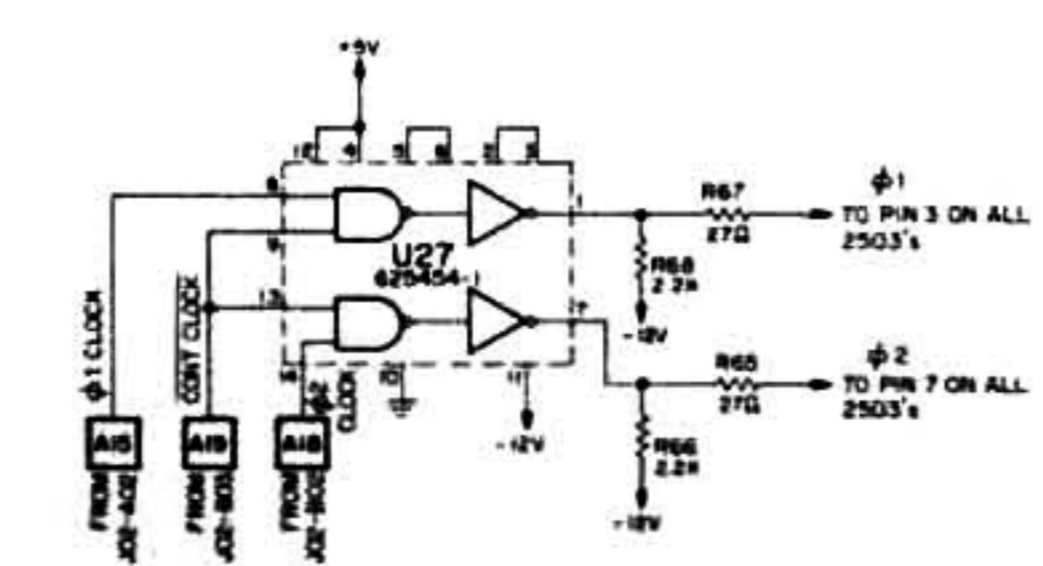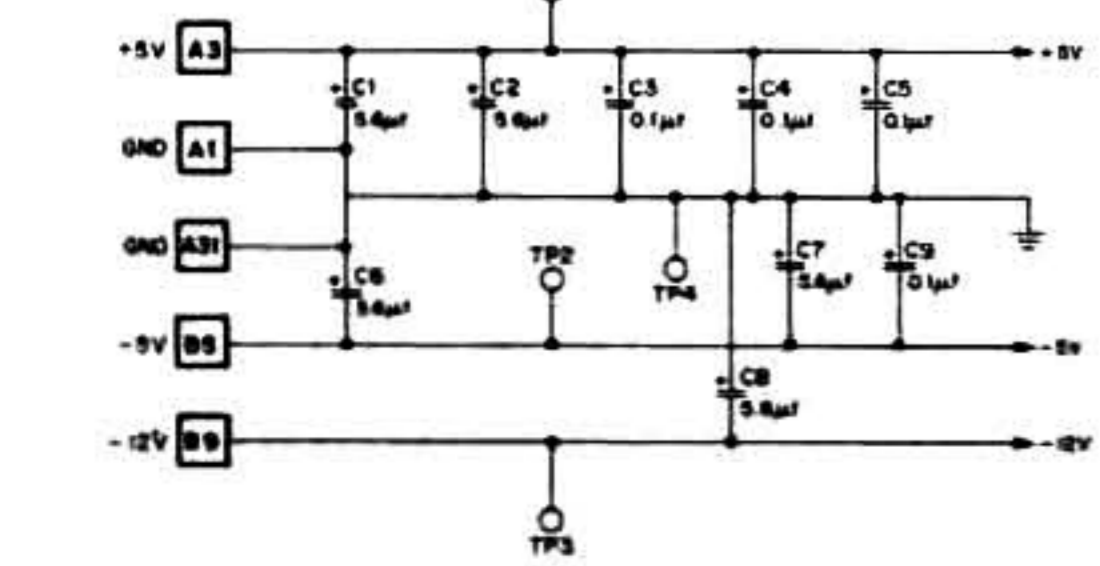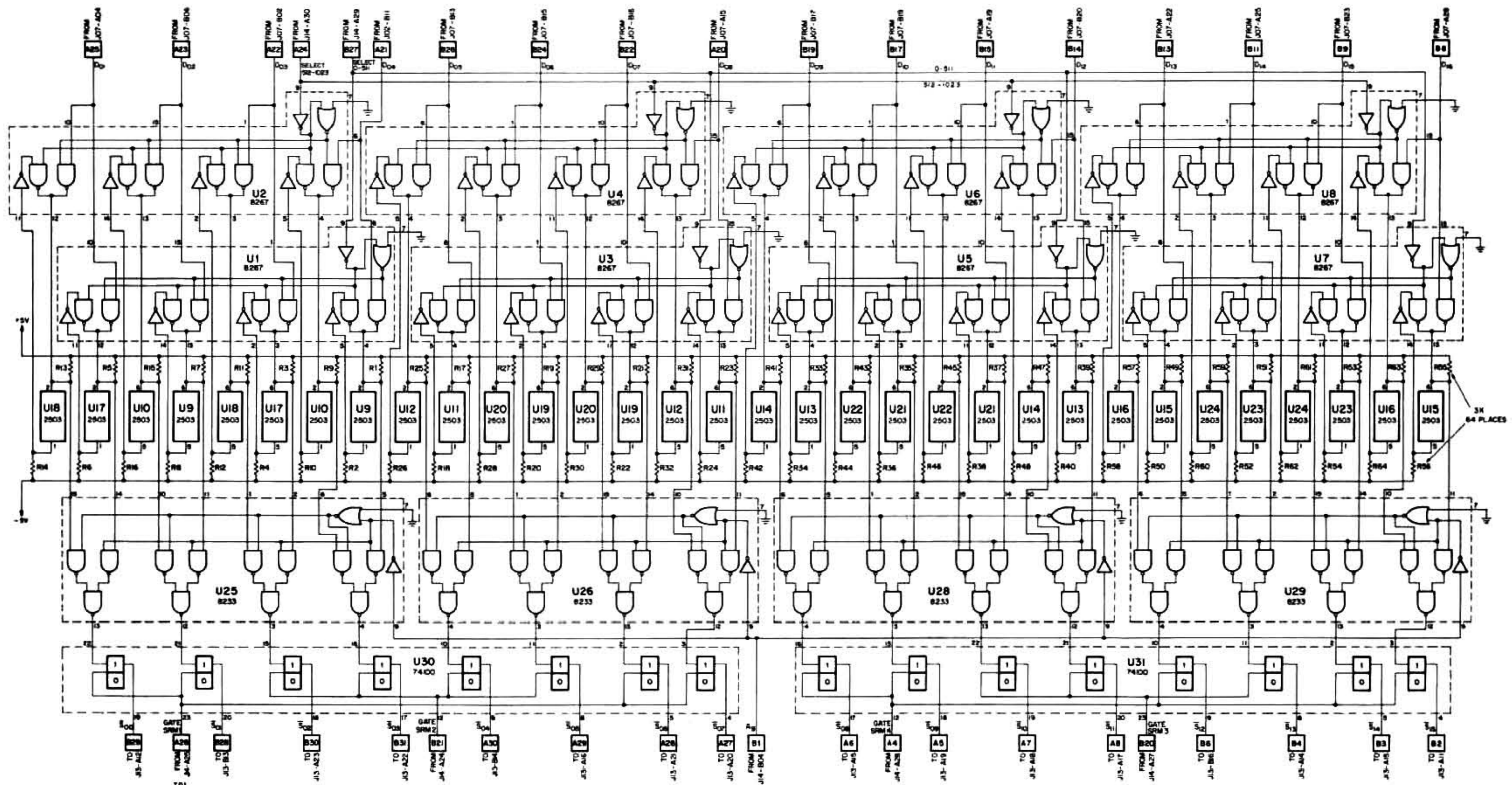

Mode 03 Test Pattern Using Program "TESTOR"

CARD 3 - SRM

(Serial No. Above 261)

The only difference between this Card 3 and that on
the previous page is the addition of the clock driver
circuit (circuit U27).

OUTPUT DRIVERS

This card contains the inverters which supply data to external devices connected to the terminal. These circuits supply 15 bits of data from the D register to the EXTERNAL OUTPUT connectors (J25) and the AUDIO connector (J28).

Audio data should be sampled during the presence of the $\overline{\text{AUDIO}}$ $\overline{\text{DATA RDY}}$ signal which is generated when a LOAD AUDIO (AUD) control word is being processed.

External output data should be sampled during the presence of the $\overline{\text{EXT DATA RDY}}$ signal which is generated when a LOAD EXTERNAL CHANNEL (EXT) control word is being processed.

On terminals with serial No. 262 and above Card 4 is not used. The serial interface on Card #2 is used instead.

OUTPUT DRIVERS

GENERAL

This card contains the Word Count register (WC), the Echo register, and the Serial Output register (SOR). Data from all sources, both internal and external to the terminal, is entered into the SOR and transmitted to the computer center. Internal sources of data in-include the WC and Echo registers. External sources of data include the keyset (KST), the External Input (EXT) channel, and the Touch Panel (TCH).

WORD COUNT REGISTER (WC)

The WC is a 7 bit counting register contained in circuits U16 and U18. This register is loaded with bits D_{07} - D_{13} of the D register when a Load Mode (LDM) control word with bit 14 (D_{14}) set is received by the terminal. The register is loaded by the $\overline{\text{GATE D} \rightarrow \text{WC}}$ signal which occurs at time T_{03} and which originates on card 8.

The WC is incremented by the INC WC signal which occurs at time T_{01}.

ECHO REGISTER

The Echo register is contained in circuits U2 and U4. This register is an 8 bit register in which the most significant bit (E_7) is always a "one". This register is loaded with bits D_{01} - D_{07} of the D register when a Load Echo (LDE) control word is received. The register is loaded by the GATE D $\rightarrow$ ECHO 2 and GATE D $\rightarrow$ ECHO 1 signals generated at time T_3. These signals originate on card 6.

INPUT CIRCUITS

Circuits U8, U10 and part of U22 interface the KST and EXT signals to the bit multiplexors.

BIT MULTIPLEXORS

Circuits U3, U5, U7, U11, U15, U17, U21, and U23 comprise the bit multiplexers. Each of these circuits switches one bit from each of the data sources to the SOR. Signals S_0, S_1 and S_2 from a scanner located on card 6 determine which data source is switched to the SOR.

SERIAL OUTPUT REGISTER (SOR)

The SOR is an 11 bit shift register composed of circuits U14 and U19. The lower 8 bits of this register are loaded by the $\overline{\text{TRANSFER}}$ signal and the upper 2 bits by the TRANSFER signal. The lower 8 bits of the SOR contain the data while the upper 2 bits specify the source of the data. The parity bit is generated on card 6. The SOR word format is shown below.

10 09 08 07				01 00
0	0	0	KEYBOARD DATA	P

10 09 08 07				01 00
0	0	1	ECHO CODE	P

10 09 08		05 04		01 00
0	1	TOUCH X	PANEL Y	P

10 09 08				01 00
1	0	EXTERNAL DATA		P

10 09 08 07				01 00
1	1	0	WORD COUNT	P

10 09 08 07 06					01 00
1	1	1	1	/////TURN ON/////	P

10 09 08 07 06					01 00
1	1	1	0	UNUSED	P

Note: The terminal turn-on code is used only in terminals reading serial No. above 261.

OUTPUT REGISTERS

UNIVERSITY OF ILLINOIS
COORDINATED SCIENCE LABORATORY

J-5

NO. GB-774

OPERATION

Flip flop U12 and circuit U6 convert the SCANNER CLOCK signal into the SAMPLE and STROBE signals. (If a PLATO modem is being used, both the SCANNER CLOCK and XMIT CLOCK will be the same 1260 Hz signal; if a 202 modem is being used, the SCANNER CLOCK will occur at a 1260 Hz rate while the XMIT CLOCK signal occurs at a 126 Hz rate.)

The SAMPLE signal samples the DATA RDY lines and advances the scanner. If a DATA RDY signal is present it is stored in the associated request flip flop. If a request flip flop is set and the associated reply flip flop is not set, a request for data transmission will occur at the output of the nor circuit (U13 or U15). The STROBE signal samples these requests in circuit U14. If the request presently specified by the scanner is a "one", the TRANSFER and TRANSFER signals are generated by circuit U14 (pins 5 and 6). The TRANSFER (and TRANSFER) signals:

1. Load the SOR on card 5.
2. Set the TRANSFER flip flop (U12).
3. Clear the PARITY flip flop (U21).
4. Set the START BIT flip flop (U23).
5. Set the associated reply flip flop from an output of U3.

After the TRANSFER flip flop has been set, the XMIT CLOCK signal is routed through U17 pin 18 and becomes the SHIFT signal. This signal is supplied to the modem (card 9), the SOR (card 5) and to the bit counter (U24) and other circuits on this card. At the same time further SAMPLE and STROBE signals are inhibited at pin 1 of U6.

SHIFT pulses are generated until all 12 bits (start bit plus 10 data bits plus parity bit) have been transmitted. The contents of the PARITY flip flop are switched into the data stream by the COUNT 10 signal and circuit U18. After 12 bits have been transmitted a COUNT 12 signal is issued at pin 11 of U6 which clears the TRANSFER flip flop and permits SAMPLE AND STROBE to be resumed.

Part of circuit U5 is used as an INHIBIT flip flop to inhibit the transmission of data from the External Channel or the Touch Panel. This flip flop is set by the GATE D + M signal (if D15 is a "one") when a Load Mode (LDM) instruction is received.
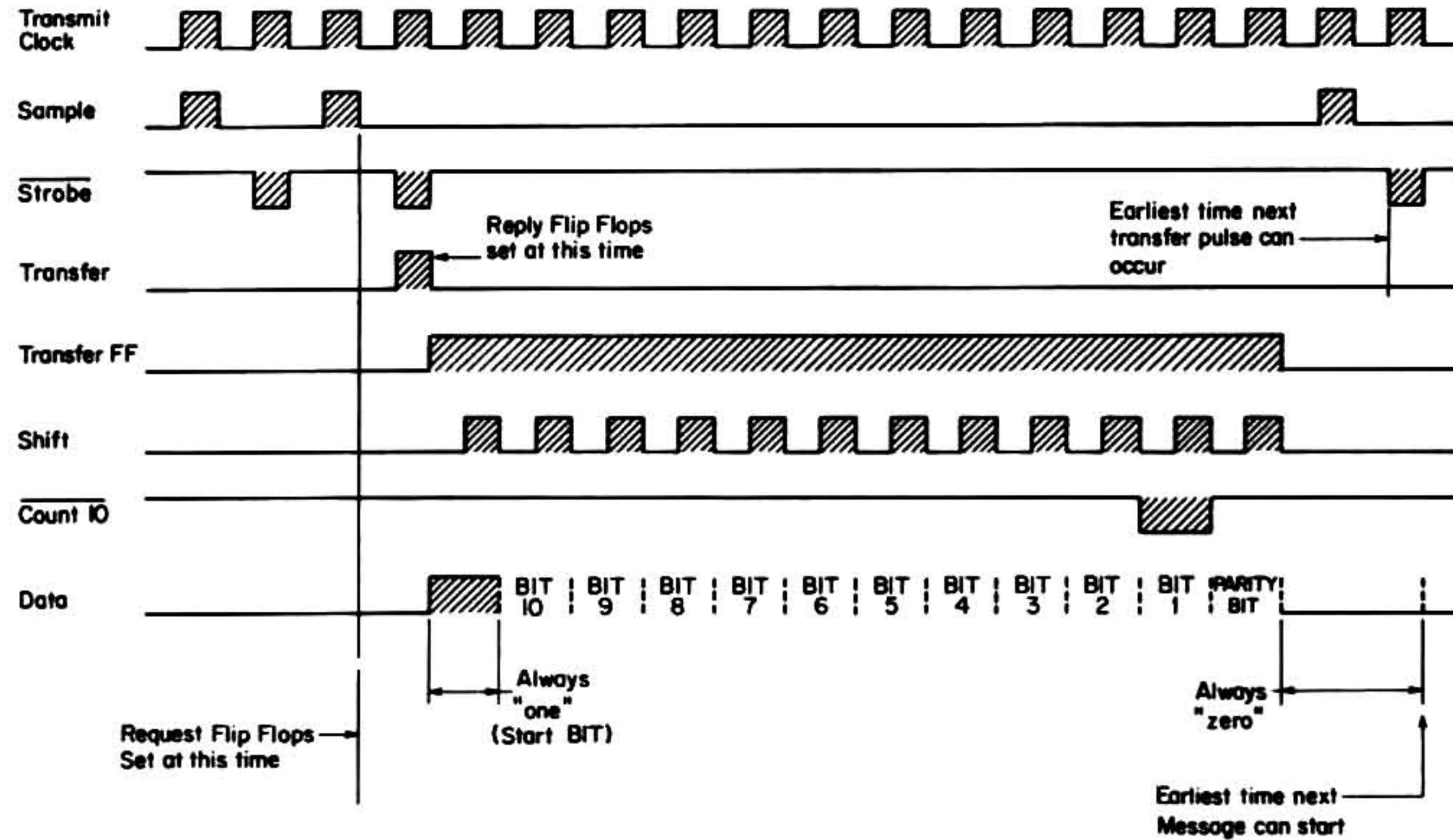
Output Control Timing Diagram

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COORDINATED SCIENCE LABORATORY

OUTPUT CONTROL

J-6

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SERIAL INPUT REGISTER (SIR)

The SIR is contained in circuits U21, U22, and U24. Serial data from the modem (card 9) is shifted into the SIR by the $\overline{\text{MODEM}}$ $\overline{\text{SHIFT}}$ signal (pin B31), also generated by the modem. After 20 bits have been shifted into this register, the GATE D signal, generated at clock time T_0, transfers the contents of the SIR to the Data (D) register.

DATA REGISTER (D)

The 20 bit D register is composed of circuits U16, U17, U18, U19, and U20. The least significant bit of this register is loaded with the PARITY CHECK signal generated on card 2. If this bit is a "one", a parity error has occurred in the received data.

Circuits U11, U12, U13, U14, and U15 interface the D register to the rest of the terminal electronics.
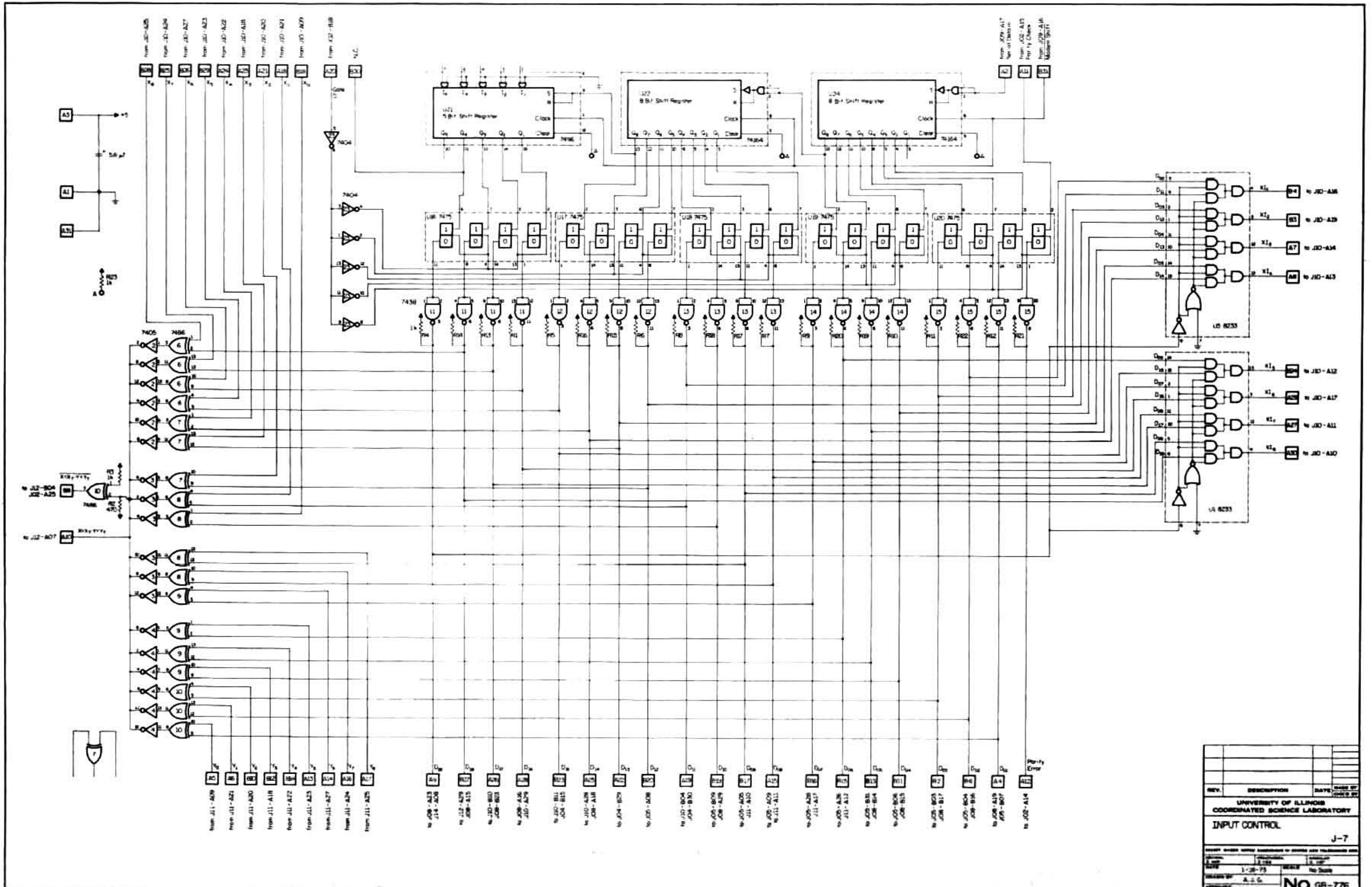
X SWITCH

Circuits U1 and U5 specify which bits of the D register are to be transferred to the X register on card 10 (circuit U20 on card 8 is also a part of the X switch). If bit 19 (D_{19}) of the D register is a "zero", the lower nine bits D_{01} through D_{09}, will be sent to the X register. This condition occurs when a Load Co-ordinate (LDC) control word is being processed.

If D_{19} is a "one", the upper 9 bits of the D register, D_{10} through D_{18} are sent to the X register. This condition occurs in Mode 0 and Mode 1.

END POINT CIRCUIT

Circuits U2, U3, U4, U6, U7, U8, U9, and U10 make up the end point circuit used in Mode 1 (line mode). This circuit compares the contents of the X and Y registers with the contents of the D register which specifies the end point of a line in Mode 1. When X and Y are equal to D, a "one" is generated on pin A10 and a "zero" on pin B8, indicating the end of a line.

GENERAL

This card contains the Mode Register and other circuits which generate control signals required by other control cards.

MODE REGISTER

Circuit U4 contains the Mode register. This register is loaded with bits D_{03} - D_{05} of the D register by the GATE D → M signal generated during the processing of a Load Mode (LDM) control word. The lower two bits of this register specify the write/erase state while the upper two bits specify the data processing mode of the terminal. Circuit U21 and part of U22 decode the upper two bits into the four mode signals $\overline{M_{00}}$, $\overline{M_{01}}$, $\overline{M_{02}}$, and $\overline{M_{03}}$ and supply these signals to other control cards. During the processing of a control word (D_{19} = 0) all of these mode signals are forced to a "one".

CONTROL WORD CIRCUITS

During the processing of control words (D_{19} = 0), circuit U15 decodes bits D_{16}, D_{17} and D_{18} which specify the type of control word. Circuits U9, U14, U16, U17 and U18 combine the outputs of the decoder with timing signals from card 2 and generate the signals required to process each of the control words. See T_0 - T_4 timing diagram for the signals required to process each control word.

MODE 1 LOGIC

Circuit U1, U2, U7 and part of U13 are a part of Mode 1 control. Flip flop U1 supplies the SUBTRACT signal to the adders and complement gates on cards 10 and 11. The SUBTRACT signal is generated at time T_2 by the action of U13 pins 1, 2 and 3, and removed by the $\overline{SET}$ $\overline{ADD}$ signal generated at time T_8.

Flip flop U2, pin 8, is used to set the input gate on the ΔX and ΔY registers. This flip flop is cleared at time T_2 which generates the X/Y → ΔX/ΔY signal, and set at time T_4.

MODE 2 CIRCUITS

Flip flop U2, pin 12, supplies the WRITE REQUEST signal to the SRM. This flip flop is set at time T_2 and cleared by the $\overline{WRITE\ RESUME}$ from SRM control.

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GENERAL

This is the modem normally supplied with the PLATO terminal. This modem is designed for operation on full duplex (4 wire) telephone circuits of up to a few miles in length. Input signal range is from +3 to -20 dbm.

MODULATOR SECTION

Transistors Q_1, Q_2, Q_3, and Q_4 comprise a 5.04 kHz multivibrator which is used to drive a counter (U10) which acts as a frequency divider supplying both 2520 and 1260 Hz signals. The 1260 Hz signal is used as the XMIT CLOCK signal and is supplied to card 6 and also used to clock the data into this card at pin B11. The data resides in the SOR located on card 6. The data (SERIAL DATA) signal changes only on the negative ("one" to "zero") transition of the XMIT CLOCK signal.

Circuit U9 selects one cycle of the 1260 Hz signal if the data (TP1) is a "one" or two cycles of the 2520 Hz signal if the data is a "zero". The composite signal is passed through a low pass filter (R27, R28, C10, C11, and L1) which removes the high frequency components and transforms the signal into an approximation of a sine wave.

The signal is then amplified by Q_5 and delivered to the telephone line. The gain adjustment (R_{33}) should be set to deliver a 2.1 volt peak to peak signal between pins B13 and B15.

DEMODULATOR SECTION

The demodulator is designed to process signals of the same form as those generated in the modulator.

The incoming signal is passed through a limiting amplifier U1 and digital comparator U2 which converts the sine wave back into a digital waveform. The signal is then supplied simultaneously to a two-stage counter (U5) and an integrator-comparator (Q_6 and U3). The integrator-comparator removes the high frequency pulses ("zeroes") from the waveform while the counter provides an output for each pair of pulses. However, since the output of the integrator-comparator will clear the counter (via pin 5 of U6), the counter will provide an output only following two short pulses (a "zero"). The counter thus becomes a "zeroes" detector while the integrator-comparator serves as a "ones" detector.

The output of the integrator-comparator and the counter set the data flip flop (U6) to the appropriate state and trigger the shift pulse circuit composed of flip flop U7 and part of circuit U4. The data flip flop is set on the leading edge while the MODEM SHIFT signal is generated on the trailing edge of the data signals thus insuring that the DATA signal is established in advance of the MODEM SHIFT signal. The DATA and MODEM SHIFT signals are supplied to the SIR or card 7.

The first bit in every word, always a "1", sets the MESSAGE START flip flop (U7) which allows the remaining bits in the word to trigger the shift pulse circuit. A counter located on card 2 counts the MODEM SHIFT pulses and following receipt of 20 pulses issues the RESET MODEM signal (B20). This signal clears the MESSAGE START flip flop inhibiting further MODEM SHIFT pulses until the next word arrives.
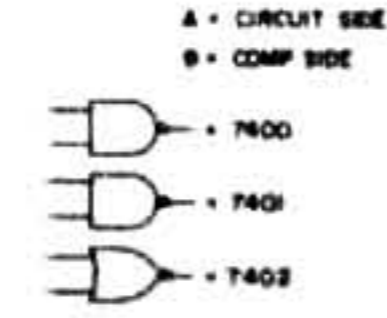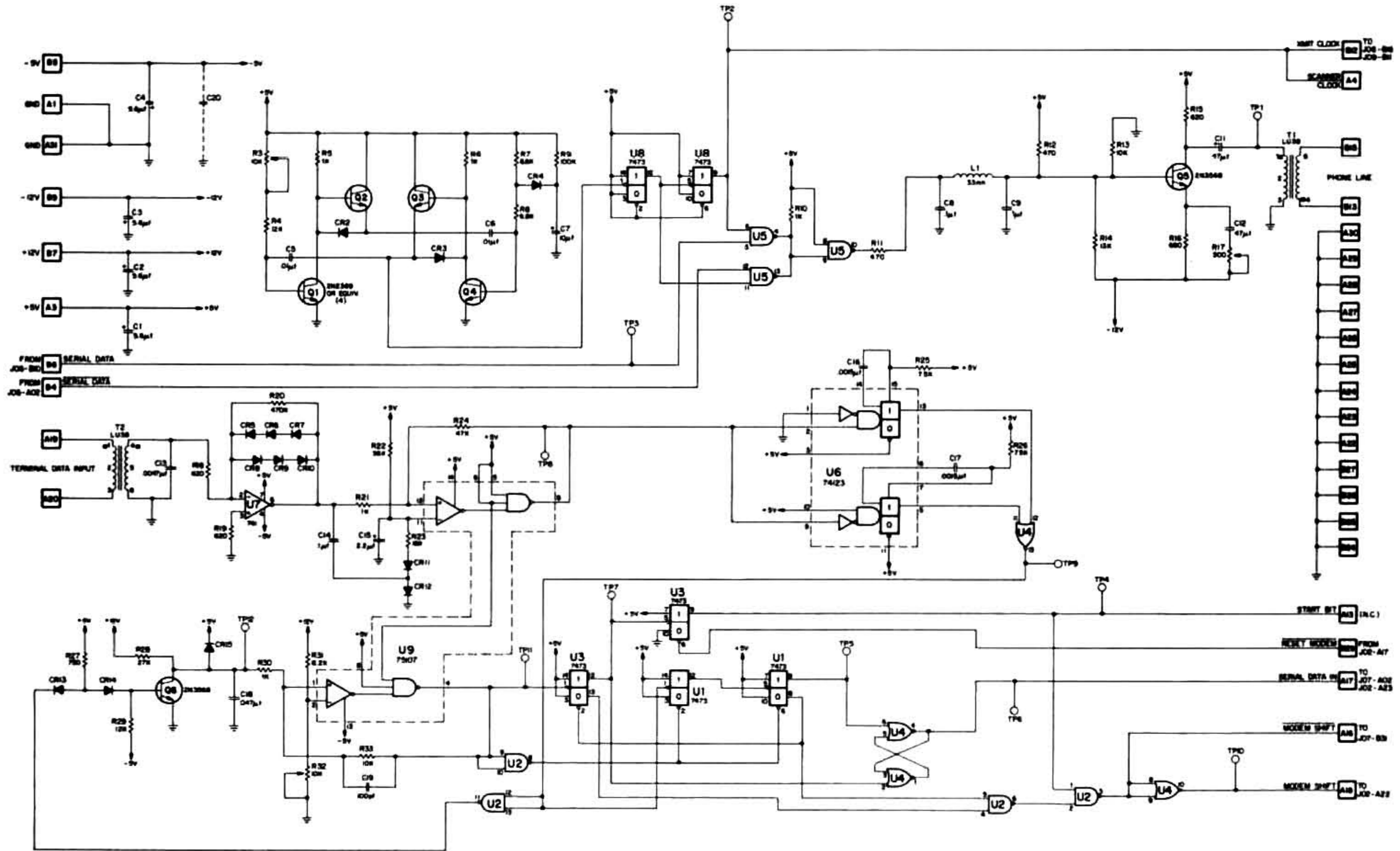
GENERAL

This modem permits the PLATO terminal to be operated on a half duplex (one pair of wires) telephone circuit. With this modem the terminal may be operated on the direct dial (DDD) telephone network or on dedicated (Schedule 4) lines. This modem is normally interfaced to the telephone network by a data access arrangement (DAA) supplied by the telephone company.

Data received by the terminal (forward channel) arrives at a rate of 1260 bits per second in the form of a frequency shifted (FSK) signal with a "zero" represented by 2200 Hz signal and a "one" by a 1200 Hz signal.

Data is transmitted by the terminal (reverse channel) at a rate of 126 bits per second in the form of an amplitude modulate (AM) 387 Hz signal. A "one" is represented by the presence and a "zero" by the absence of the 387 Hz signal.

OPERATION

Circuits 8, 9, 10, 11, and 12 are counters which count down the output of a 5.16096 mHz crystal oscillator (TP2) and generate the 1260 Hz SCANNER CLOCK signal (A4), the 126 Hz XMIT CLOCK signal (B11) and a 387 Hz square wave signal (TP12). Both the XMIT CLOCK and SCANNER CLOCK signals are supplied to the Output Control circuit on card 6.

The 387 Hz square wave is turned off for a "zero" or on for a "one" at the input to amplifier U17 by the action of transistors 2N5485 and MPS3703 and the flip flop in Circuit 7. The data to be transmitted is shifted into this flip flop by the XMIT CLOCK signal.

Amplifiers U17 and U14 comprise a low pass filter which converts the 387 Hz square wave into a 387 Hz sine wave. Amplifier U14 adjusts the amplitude of the 387 Hz before applying it to the telephone line. The gain of this amplifier should be adjusted until a signal of 2.1 volts (peak to peak) is observed at TP10.

The reverse channel signal and forward channel signal are supplied to amplifier U13 which subtracts the 387 Hz signal component of the composite waveform. Circuits U13 and U15 are 387 Hz notch filters which remove any remaining 387 Hz signal components. The signal is then supplied to a delay equalizer (U18) and limiter U15. The limiter limits the amplitude of the received signal to approximately 1.5 volts peak to peak.

The delay equalizer circuit is used to compensate for delay in the telephone network which may be present in longer circuits (100 miles or more). This circuit can be switched in or out as required.

The output of the limiter is supplied to the demodulator circuit U16, which converts the received signal into the $\overline{\text{REC DATA}}$ signal. (TP3) This signal is then supplied to the resynchronizer composed of circuits 3, 4, 5, and part of 6.

Each time the $\overline{\text{REC DATA}}$ signal makes a "one" to "zero" transition, a pulse is generated at pin 8 of circuit 6 which clears a counter (circuit 4). Each time the counter reaches the count of 7 a pulse is supplied at pin 6 of circuit 5. This pulse will occur in the middle of a data bit interval. If the DATA signal is a "one", the START flip flop (TP15) will be set permitting the generation of $\overline{\text{SHIFT}}$ and SHIFT signals (TP1). These signals are supplied to card 7 and card 2. After 20 SHIFT pulses have occurred, a $\overline{\text{RESET}}$ signal is generated on card 2 which clears the START flip flop to await the receipt of the next word.

202 MODEM

MARK II

AA-030-4

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GENERAL

Cards 10 and 11 are identical cards with card 10 containing the X register and all but the most significant bit of the X section of the line generator and card 11 containing the Y register and all but the most significant bit of the Y section of the line generator.

X (Y) REGISTER

Circuits U4, U10, and half of U11 contain the X(Y) register. The least significant bit, $X_0(Y_0)$, is contained in U11. This register is a 9 bit register which may be parallel loaded or counted forward (up) or backwards (down).

The X register is loaded with the output of the X switch (XI_0 - XI_8) on card 2 and the Y register is loaded with the least significant nine bits (D_{01} - D_{09}) of the D register on card 2. These registers are loaded by the $\overline{\text{GATE X}}$ and $\overline{\text{GATE Y}}$ signals.

The X_D (Y_D) flip flop, part of U11, indicates the direction the X(Y) register is to be counted. If this flip flop is a "one", the register will be incremented by the $\overline{\text{CLOCK X(Y)}}$ signal; if this flip flop is a "zero", the register will be decremented by the $\overline{\text{CLOCK X(Y)}}$ signal. Circuit U5 supplies the count up (pin 6) and count down (pin 12) signals to the upper 8 bits of the register.

The X_D (Y_D) flip flop is set by the $\overline{\text{SET X(Y) FWD}}$ signal, cleared by the $\overline{\text{SET X(Y) RVS}}$ signal, and toggled (inverted from its present state) by the TOGGLE $X_D(Y_D)$ signals.

LINE GENERATOR

The remaining circuits on this card are used in generating lines in Mode 1. Circuits U2 and U8 comprise the ΔX (ΔY) register, circuits U14 and U20 the X_f (Y_f) register and circuits U13 and U19 comprise an 8 bit adder.

Circuits U3 and U8 provide the gating circuits which allow the ΔX (ΔY) register to be loaded with the output of the adder or the contents of the X(Y) register. If the $X \rightarrow \Delta X$ ($Y \rightarrow \Delta Y$) signal is a "one", the contents of the X(Y) register are supplied as input to the ΔX (ΔY) register. If the $X \rightarrow \Delta X$ ($Y \rightarrow \Delta Y$) signal is a "zero" the output of the adder is supplied as inputs. The data supplied by U3 and U8 is loaded into the register by the CLOCK ΔX (ΔY) signal and the condition that the SUBTRACT signal (pin B8) is a "one". If the SUBTRACT signal is a "zero" when the CLOCK ΔX (ΔY) signal occurs, the data already stored in the register will be shifted left one bit position.

Circuits U15 and U21 provide gating circuits which permit the X_f (Y_f) registers to be loaded with the output of the adder or the contents of the D register. If the SUBTRACT signal is a "one", the contents of the D register are supplied as inputs; if the SUBTRACT signal is a "zero", the output of the adder is supplied as inputs. (If the SUBTRACT signal is a "one" and the NULL $X_f \cdot Y_f$ signal is a "one", zeroes are supplied as inputs.) Data is loaded into the X_f (Y_f) register by the CLOCK $X_f \cdot Y_f$ signal.

Circuits U1 and U7 act as a complement gate between the ΔX (ΔY) register and the input to the adder. If the SUBTRACT signal is a "one", the complement of the ΔX (ΔY) register is supplied to the adder, while if the SUBTRACT signal is a "zero" true (actual) contents of the ΔX (ΔY) register are supplied.

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GENERAL

This card contains the most significant bit (bit 8) of the line generator plus the timing circuits which generate the signals required in a Mode 1 (line mode) operation.

LINE GENERATOR

Circuit U14 contains the most significant bit of the ΔX and X_F (ΔX_8 and X_{F8}). Circuit U20 contains the most significant bit of the ΔY and Y_F registers (ΔY_8 and Y_{F8}). Circuits U7 and U13 are each 2 bit adders. Circuit U19 acts as a complement gate between the ΔX (ΔY) register and the inputs to the adder. If the SUBTRACT signal is a "one", the complement of these registers is supplied to the adder, if the SUBTRACT signal is a "zero", the true (actual) contents of the registers are supplied to the adder.

Circuit U5, part of U6, and part of U21 provide gating circuits which permit the ΔX and ΔY registers to be loaded with the output of the adder, the contents of the X and Y registers, or the contents of the previous stage (ΔX_7, ΔY_7) of these registers during a shift operation.

Half of circuit U3 and inverter U4 provide the control signals which operate the gating circuits. If the $X/Y \rightarrow \Delta X/\Delta Y$ signal is a "one" and the SUBTRACT signal is a "one", the contents of the X and Y registers (X_8 and Y_8) are supplied as inputs to the ΔX and ΔY registers. If the $X/Y \rightarrow \Delta X/\Delta Y$ signal is a "zero" and the SUBTRACT signal is a "one", the outputs of the adder are supplied as inputs. If the SUBTRACT signal is a "zero", the contents of the previous stage of these registers (ΔX_7 and ΔY_7) are supplied as inputs.

Circuits U15 and part of U3 provide the gating circuits for loading the X_F and Y_F registers with the outputs of the adder or the contents of the D register (D_{09} to Y_{F8} and D_{18} to X_{F8}).

Circuit U2, and inverters U8 and the outputs of the adders (S_{X9} and S_{Y9}) specify the signals to set the X and Y direction flip flops on cards 10 and 11.

TIMING CIRCUITS

The remaining circuits on this card generate the timing signals (T_5 through T_{11}) required in Mode 1. This control is initiated by the M_{01} TRANSFER signal (pin A13) from card 2 and terminates with the $\overline{\text{EXIT}}$ signal (pin A6).

Time T_5 is generated at U16 pin 10; time T_6 at U16 pin 13, time T_7 at U16 pin 4; time T_8 at U16 pin 1; time T_9 at U17 pin 4; time T_{10} at U17 pin 10; and time T_{11} at U17 pin 13.

GENERAL

This card contains the read-only memory (ROM), the memory data switch (MDS) and bit multiplexor (MPX) all of which are used in plotting characters. (Mode 3).

ROM

The read-only memory is contained in circuits U3, U4 and U5. These circuits contain the data required to plot the characters in character memory 0 (M_0) and 1 (M_2). See Table 1 for a list of these characters.

Circuits U3 and U4 are each organized as 512 words of 8 bits each while circuit U5 contains 1024 words of 4 bits each. A character is stored in the ROM as 8 successive columns of data 12 bits high. The upper 8 bits of character addresses 0 through 63 are stored in U3 and the upper 8 bits of characters 64 through 127 are stored in U4. The lower 4 bits of all 128 characters are stored in U5.

The outputs of circuits U3 and U4 are tied together, as only one of these circuits is selected at one time. These circuits are selected by the presence of a "zero" on pin 3. If address bit A_9 is a "zero", circuit U3 is selected, while if A_9 is a "one", circuit U4 is selected.

Address information, A_0 through A_9, is supplied by the memory address register (MAR) located on card 14. The address bits are interfaced to the ROM by circuits U1 and U2. The output of these circuits swing from 0 to +12 volts.
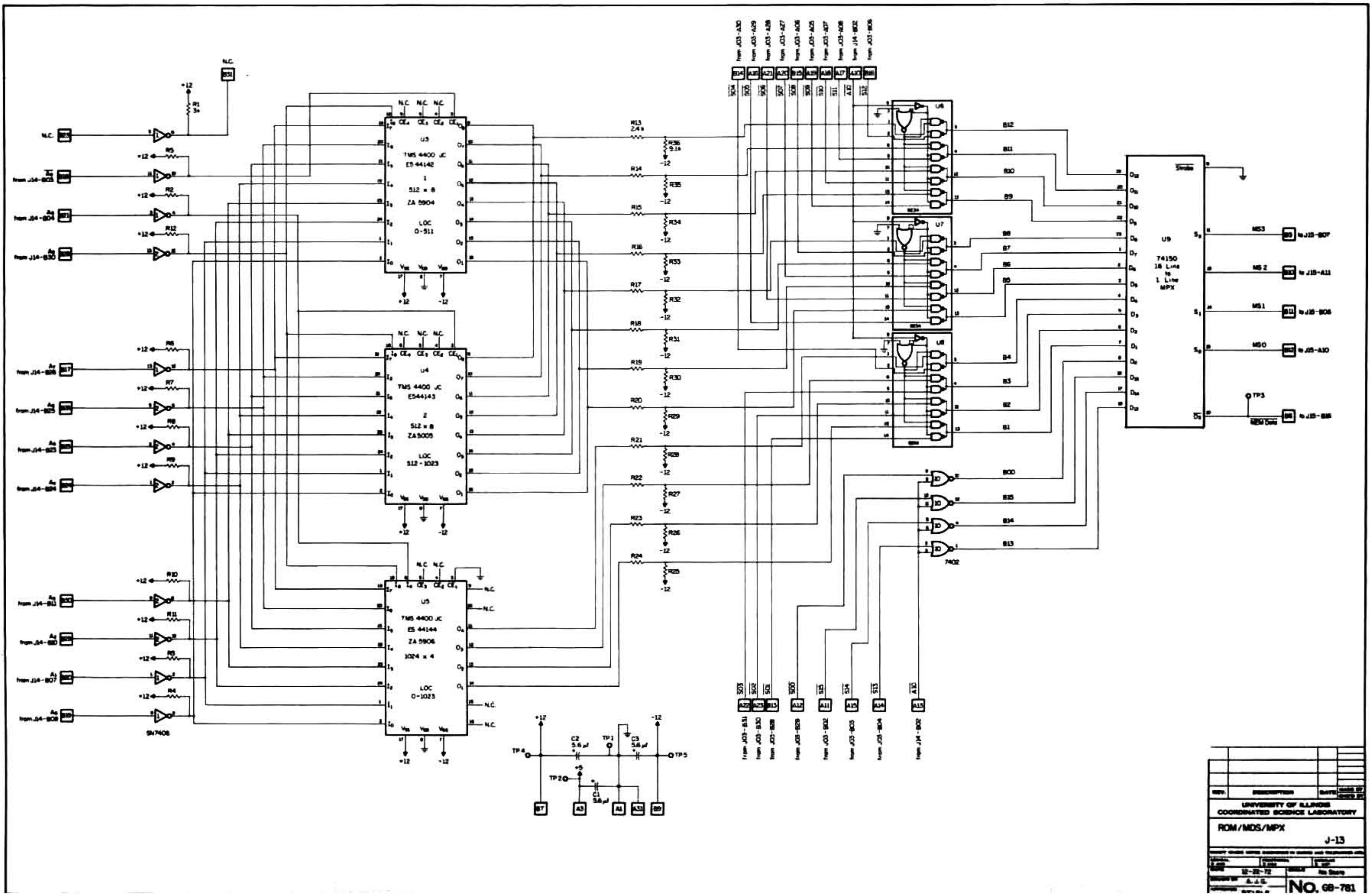
MDS

The memory data switch (MDS), circuits U16, U7, U8 and U9 specify whether ROM or shift register memory (SRM) data is to be supplied to the bit multiplexor (MPX). SRM data is supplied from card 3. If bit 10 (A_{10}) of the MAR is a "zero", ROM data is supplied to the MPX while if A_1 is a "one", SRM data is supplied.

A character is actually 16 bits high when displayed on the plasma panel. While the SRM contains 16 bit words, ROM data consists of 12 bit words. When ROM characters are being displayed, circuit U10 forces the bottom bit (B_{00}) and the top 3 bits (B_{13}, B_{14}, B_{15}) of the character data to be "zero". See Figure 4 in the word format section.

MPX

Circuit U9 is a 16 line to 1 line multiplexer. Each of the 16 data lines (B_{00} through B_{15}) is sampled by a scanner located in Mode 3 control (card 15). The scanner outputs, MS_0 through MS_3 specify which bit of data is to be processed. This data is supplied to Mode 3 control as the $\overline{MEM\ DATA}$ signal on pin B6. (Also TP3).

GENERAL

This card contains the memory address register (MAR) and a portion of the shift register memory (SRM) control.

MAR

The MAR is an 11 bit counting register contained in circuits U7, U11, and U23. The organization of this register is shown below.

10 9 8	3 2	0
MEM	Character Address	Column Select

Bits A_9 and A_{10} specify which of the four memories is to be addressed. Memories 00 (M_0) and 01 (M_1) are ROMs, and memories 10 (M_2) and 11 (M_3) are SRMs. These bits may be set by the memory select codes in a Mode 3 (character mode) operation or by a Load Memory Address (LDA) control word. In the latter case A_{10} is always set to "one" and A_9 is set to the value of D_{10}. Circuit U12 provides the logic for setting these bits.

Bits A_3 through A_8 specify the address of the character to be read from the memory. This character address is obtained from one of the three character addresses held in the D register during a Mode 3 operation. Circuits U3, U4, and U5 select which of these character addresses will be loaded into the MAR. A character counter located on card 15 generates the CHAR 1 and CHAR 0 signals which specify to circuit U3, U4, and U5 which character address to select.

As each character address is loaded into the MAR, the column select bits A_0 through A_2 are set to "zero". A character is composed of sixteen bit words located at consecutive addresses. After each 16 bit word has been read from memory and plotted on the plasma panel, the column select bits are incremented by 1 and the next word is read and plotted. This operation continues until 8 successive words have been read from memory and plotted at which time a new character address may be loaded into bits A_3 through A_8.

During the Mode 2 operation (load memory mode) the MAR is incremented by 1 after each word is stored in the SRM.

SRM ADDRESS REGISTER

Circuits U8 and U9 comprise the SRM address register. The most significant bit (A_8) of this register is located in circuit U21. This register indicated the address of the word present at the output (and simultaneously at the input) of the SRM.

Circuits U10, U14 and parts of U15, U16 and U20 compare the contents of the MAR with the SRM address register. When these two registers are equal the SRM = MAR signal is generated (TP-9).

SRM CONTROL

Circuits U1, U13, U19 and flip flop U21 make up a portion of the SRM control circuit. Write operations (in Mode 2) are initiated by the occurrence of the WRITE REQUEST signal (pin B29). This signal and bit A_9 of the MAR and the occurrence of the SRM = MAR signal open one of the gates into the SRM (SELECT 0-511 or SELECT 512-1023) allowing data to be stored in the SRM. After the data is stored, the WRITE RESUME signal is supplied by U21, indicating the completion of the operation.

Read operations are initiated by the READ REQUEST signal (pin B5). This signal and the occurrence of the MAR = SRM signal generate the READ RESUME signal at pin 8 of U19 and the GATE SRM 1 through GATE SRM 4 signal at the output of the U1. The GATE SRM signals each load 4 bits of memory data into the register on card A3. The READ RESUME signal indicates the completion of the read operation.

MAR/SRM CONTROL

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J-14

NO. GB-782

55

GENERAL

This card generates the timing and control signals required to plot characters in Mode 3. Contained on this card are the timing circuits (time T_2 - T_7), a character counter which maintains a record of which of the three characters in a Mode 3 word is currently being processed and a bit scanner which scans each of the 8 sixteen bit words which make up a character.

TIMING

Circuits U7, half of U9, U13 and U15 generate the required clock pulses. T_2 is generated at pin 10 of U7, T_3 at pin 1 of U7, T_5 at pin 13 of U7, T_6 at pin 1 of U9, and T_7 at pin 10 of U9.

CHARACTER COUNTER

Each Mode 3 word specifies 3 character addresses. Circuit U16 and half of U23 specify which of these characters is currently being processed. The outputs of this circuit, CHAR 0 and CHAR 1, are supplied to card 14 wlhere they are used to load the MAR.

The character counter is cleared at time T_2 and incremented at time T_7 or by NON-PLOT EXIT if the character count is less than 2. This action occurs at U23 pin 3. If the character count is 2 when either of the above signals occurs, the $\overline{\text{EXIT}}$ signal is generated at pin 10 or U10 terminating Mode 3 control.

During a Load Memory Address (LDA) control word operation, D_{19} is a "zero" which forces both CHAR 0 and CHAR 1 to be "ones". This action, allows the MAR on card 14 to be loaded with the 10 bit memory address instead of a 6 bit character address.
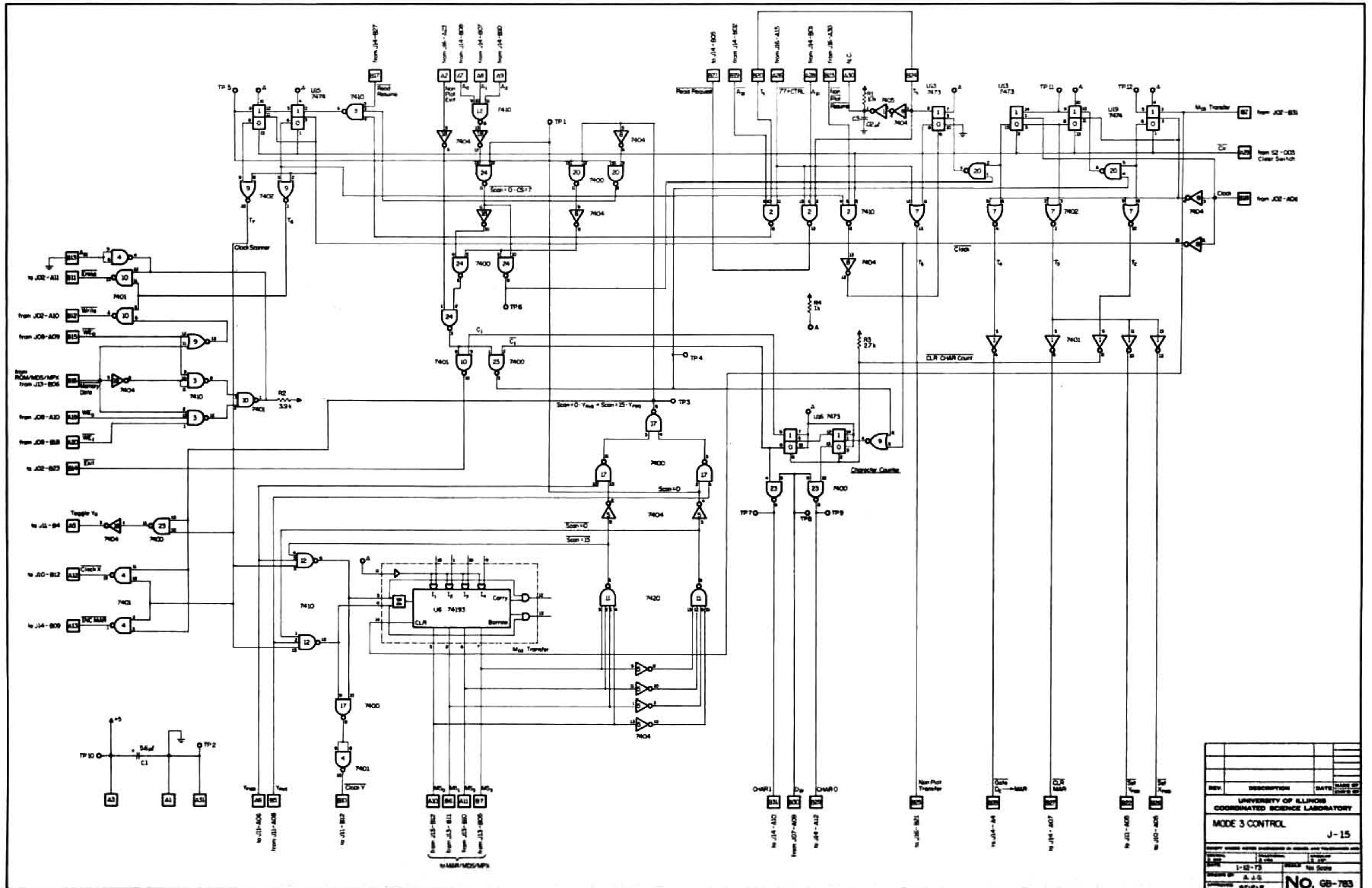
BIT SCANNER

Circuit U6 is an up-down counter the outputs of which (MS_0 through MS_3) are used to scan each of the eight 16 bit words which make up a character. Bit 0 is always the bottom bit and bit 15 the top bit in these words. The outputs of this counter are supplied to the multiplexor on card 13. Circuits U11, U12, U17, U23 and U4 also use the outputs of the bit scanner to specify the direction and X and Y registers and the bit counter are to be advanced. See the Mode 3 timing diagram for a description of operation.

WRITE/ERASE CIRCUITS

Circuits U3 and U10 combine the $\overline{\text{MEMORY DATA}}$ signal and the write/erase information (WE_0 and WE_1) in the Mode Register and generate the WRITE or ERASE signals which write or erase information on the plasma panel.

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MODE 3 CONTROL

J-15

NO. GB-783

57

GENERAL

This card provides the timing and control signals required to process the control characters in Mode 3. These characters are non-plotting characters, i.e. they do not result in the plotting of information on the plasma panel; only the contents of the X and/or Y registers are changed. These characters and their octal codes are:

Uncover	77
Backspace (BS)	10
Tab	11
Line Feed (LF)	12
Vertical Tab (VT)	13
Form Feed (FF)	14
Carriage Return (CR)	15
Superscript (SO)	16
Subscript (SI)	17
Memory Select 0	20
Memory Select 1	21
Memory Select 2	22
Memory Select 3	23

CHARACTER DECODE

Circuits U6, U11, U12, U17, U18, U23, and half of U10 decode the character address held in bits A_3 through A_8 of the MAR. The outputs of the decoding circuits are supplied to U21 where they are used to generate the signals which set the X and Y direction flip flops (on cards 10 and 11), and to circuits U9 and U16 where they are used to generate the $\overline{CLRX}$, $\overline{CLRY}$ and $\overline{CLOCK\ X}$, $\overline{CLOCK\ Y}$ signals.

CONTROL

Circuits U2, half of U3, and U8 generate the timing signals for processing the non-plot characters.

Non-plot control is initiated by the NON-PLOT TRANSFER which occurs at time T_5 in Mode 3 control on card 15. Circuits U2, half of U3, and U8 generate the three timing signals T_6, T_7 and T_8 used in processing the non-plot characters. T_6 is generated at pin 13 of U8, T_7 at pin 1 of U8 and T_8 at pin 10 of U8. At the conclusion of T_8 control is returned to Mode 3 control by the NON-PLOT EXIT signal on pin A23.

Circuits U14 and U15 provide a means of locking the control in time T_7 for either 1, 4, 8, or 16 clock pulses. If the character being processed is an uncover code or one of the Memory Select codes, control remains at T_7 for 1 clock time by the action of U15 (pins 11, 12 and 13). If the character is a Superscript or Subscript, control remains at T_7 for 4 clock times by the action of U15 (pins 8, 9 and 10). If the character is a Backspace or Tab, control remains at T_7 for 8 clock times by the action of U15 (pins 4, 5 and 6). If the character is a Line Feed, Vertical Tab, Form Feed or Carriage Return, control remains at T_7 for 16 clock times by the action of U15 (pins 1, 2, and 3).
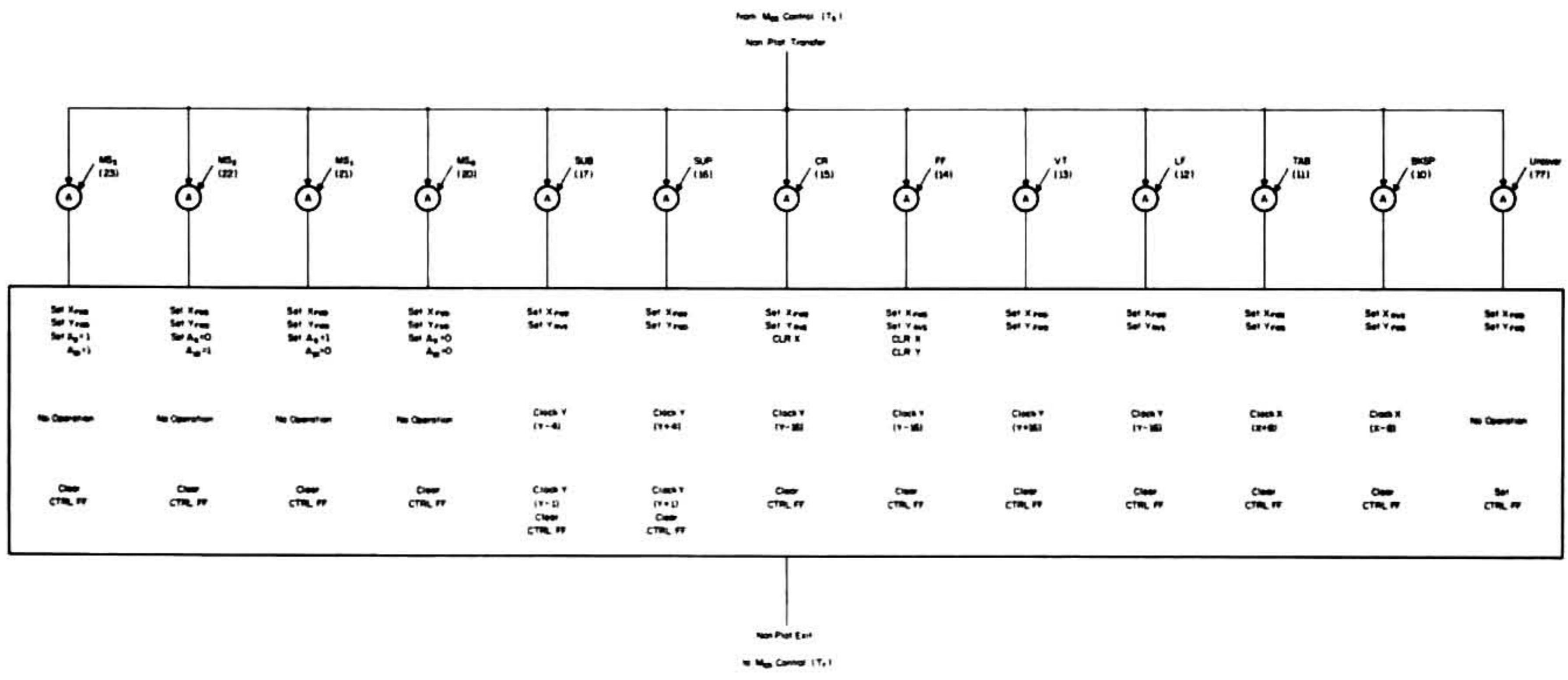
Circuit U9 (pins 1, 2 and 3) provide a means of resetting the T_8 flip flop (U3) at the conclusion of control operations. If the character being processed is on Uncover (77), the CTRL flip flop (U3) is set at T_8; if not the CTRL flip flop is cleared at T_8. See the Non-Plot timing diagram for a description of operation of this circuit.
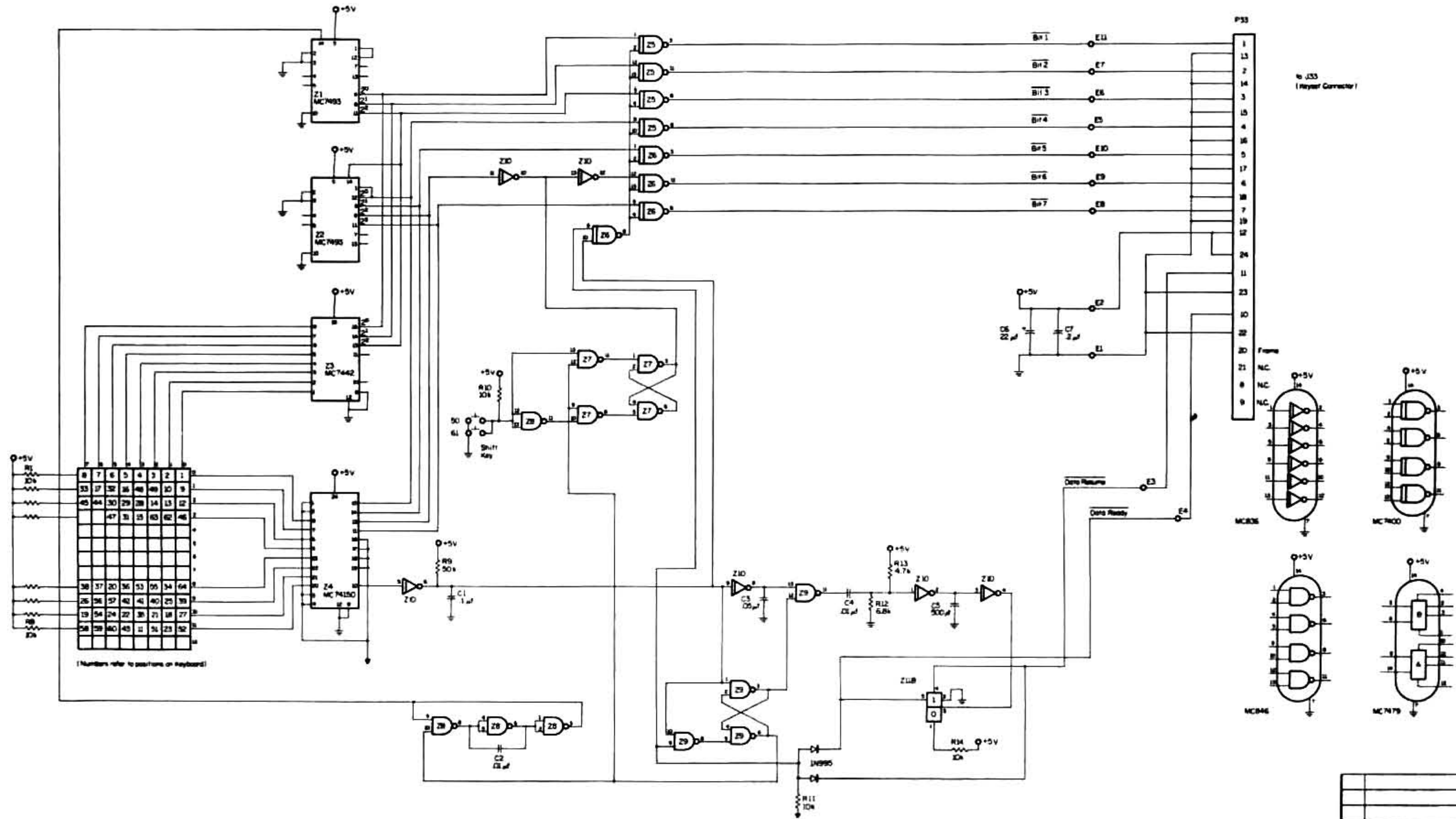
NON PLOT CONTROL & CHAR. DECODE   J-16

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Non Plot Timing Diagram

Note:
1. Each key has two different inputs. The octal number below the box is the input when a key is pressed singly (normal state), and the number above the box is the input when the "Shift" key is held down as a key is pressed (shift state).
   The "Shift" key alone does not initiate input data transfer, but merely causes an addition of 040 (octal) to a normal input.
2. There is a total of 124 different inputs.
3. The input codes 036, 037, 076, and 077 are not used.
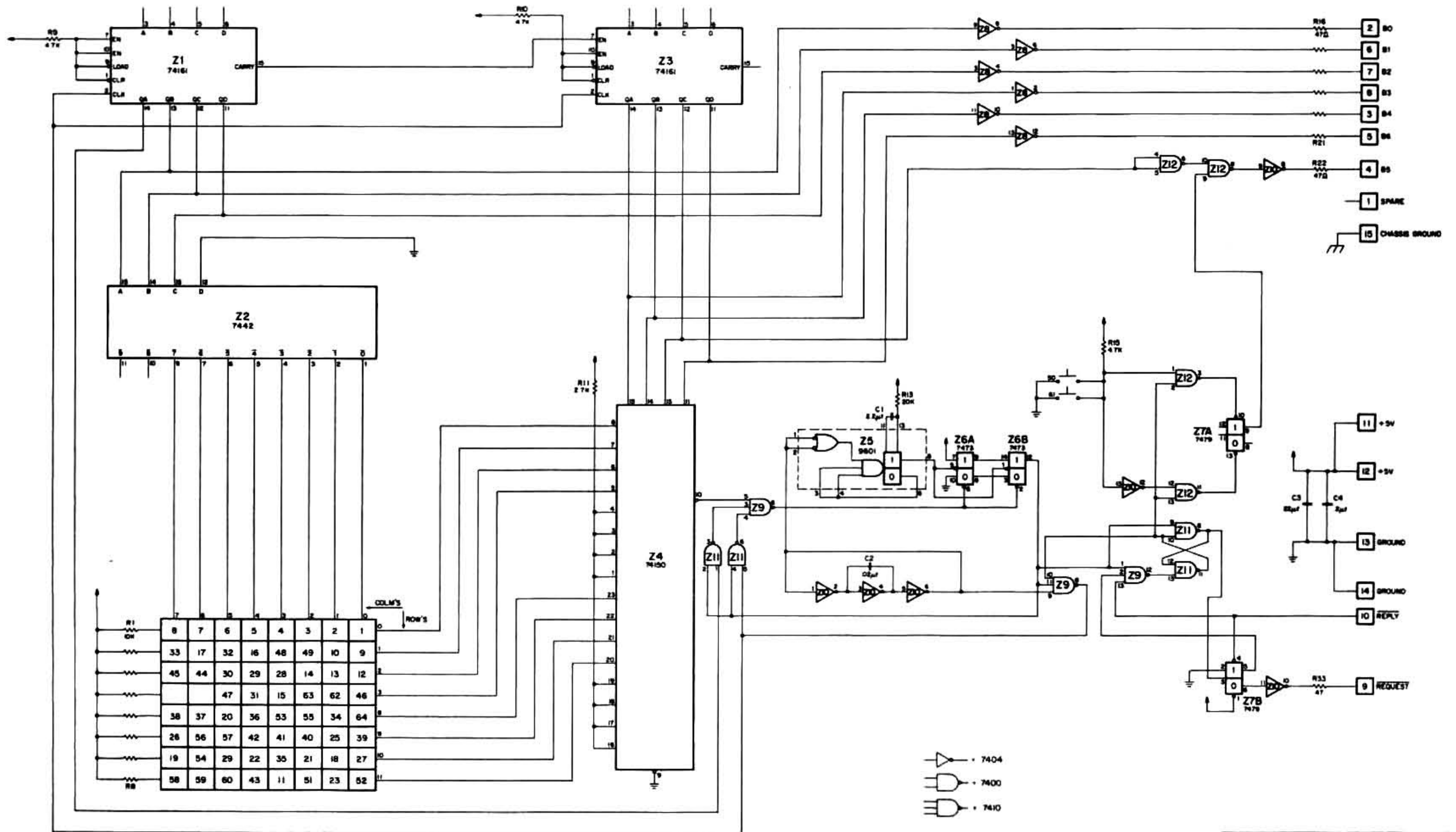4. The numbers at end of rows identify keytop locations on P.C. board.

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URBANA, ILLINOIS 61801

KEYSET LAYOUT
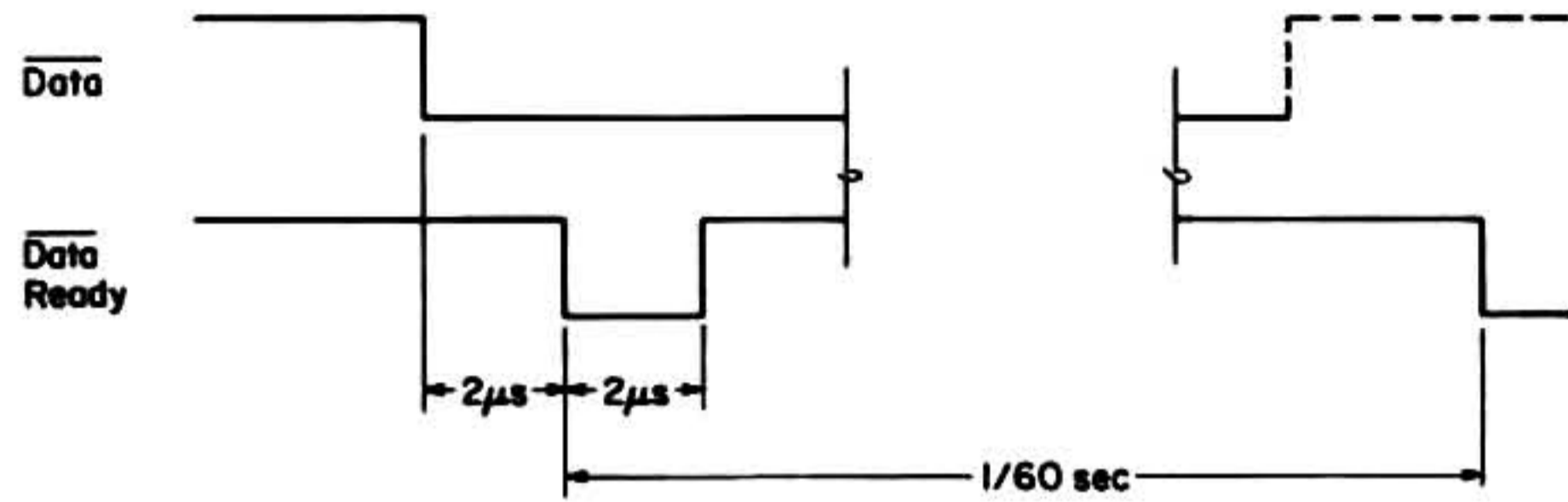FOR SERIAL NOS 262 AND ABOVE

7-15-74   RTL   AA-047-4
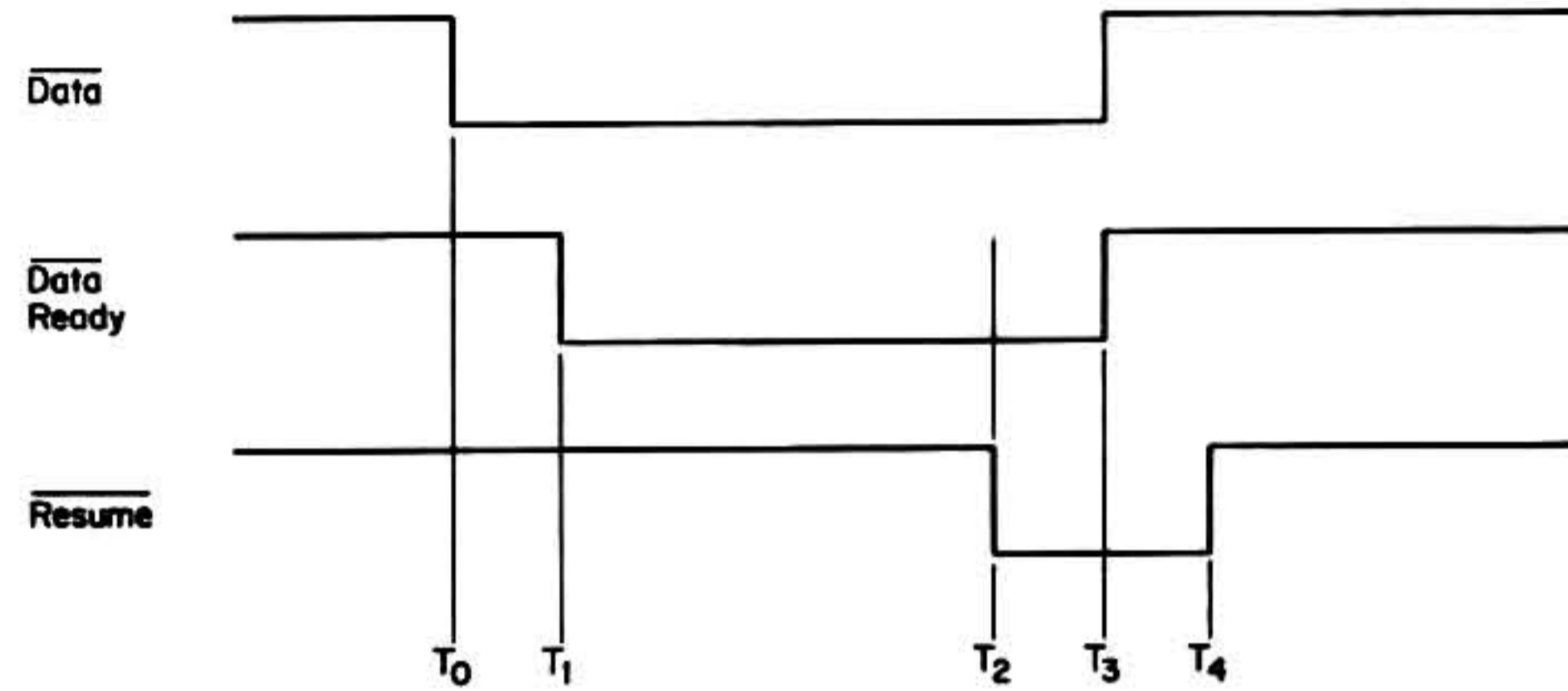
64

Waveforms for External Output Channel, Audio Store and Slide Selector

(Serial No's 1 - 261)

Interface Circuits

Waveforms for Keyset and/or External Input Channel

The data is established at time T_0. The Data Ready signal (T_1) may be issued any time after T_0.

The Data Ready signal remains present until receipt of the Resume signal at time T_2. Time T_2 may occur any time after T_1.

The Resume signal remains present until the Data Ready signal is removed at time T_3.

T_3 may occur any time after T_2. T_4 may occur any time after T_3.
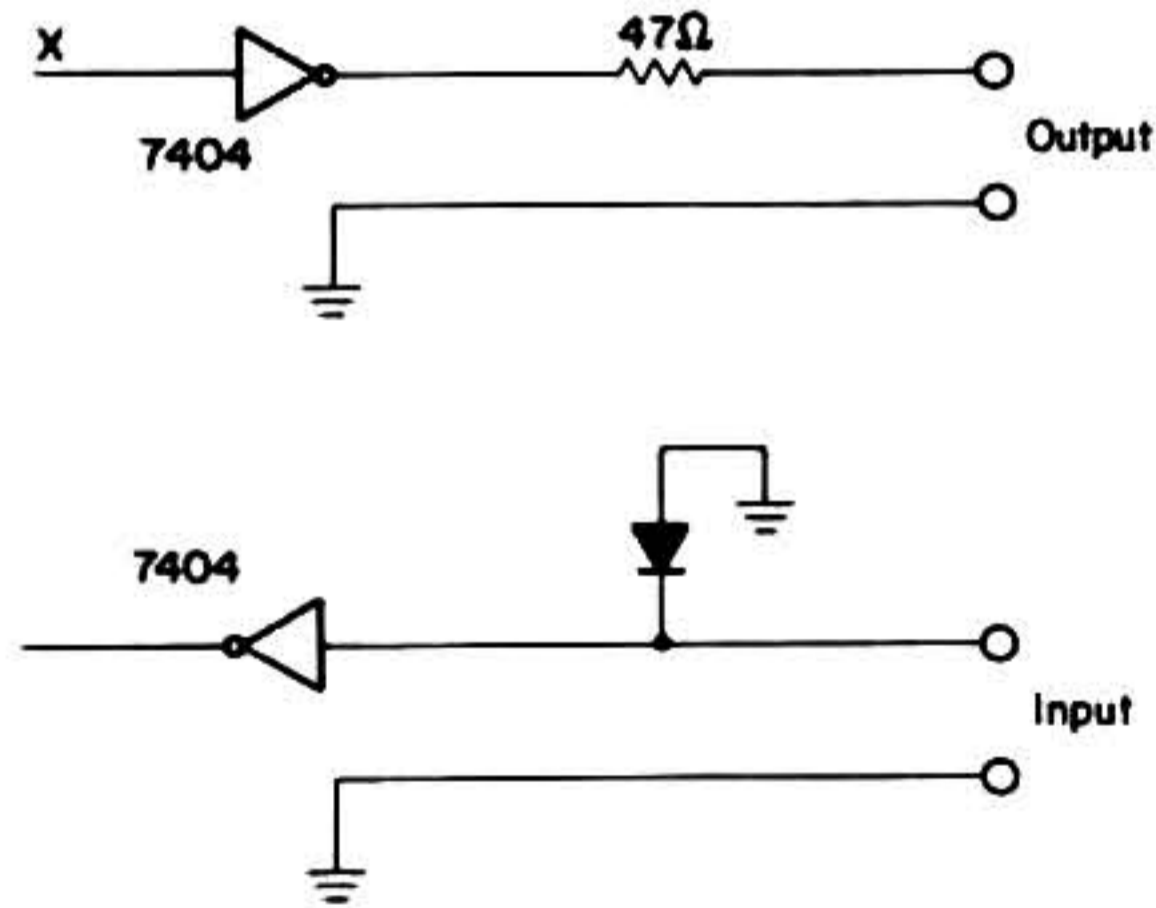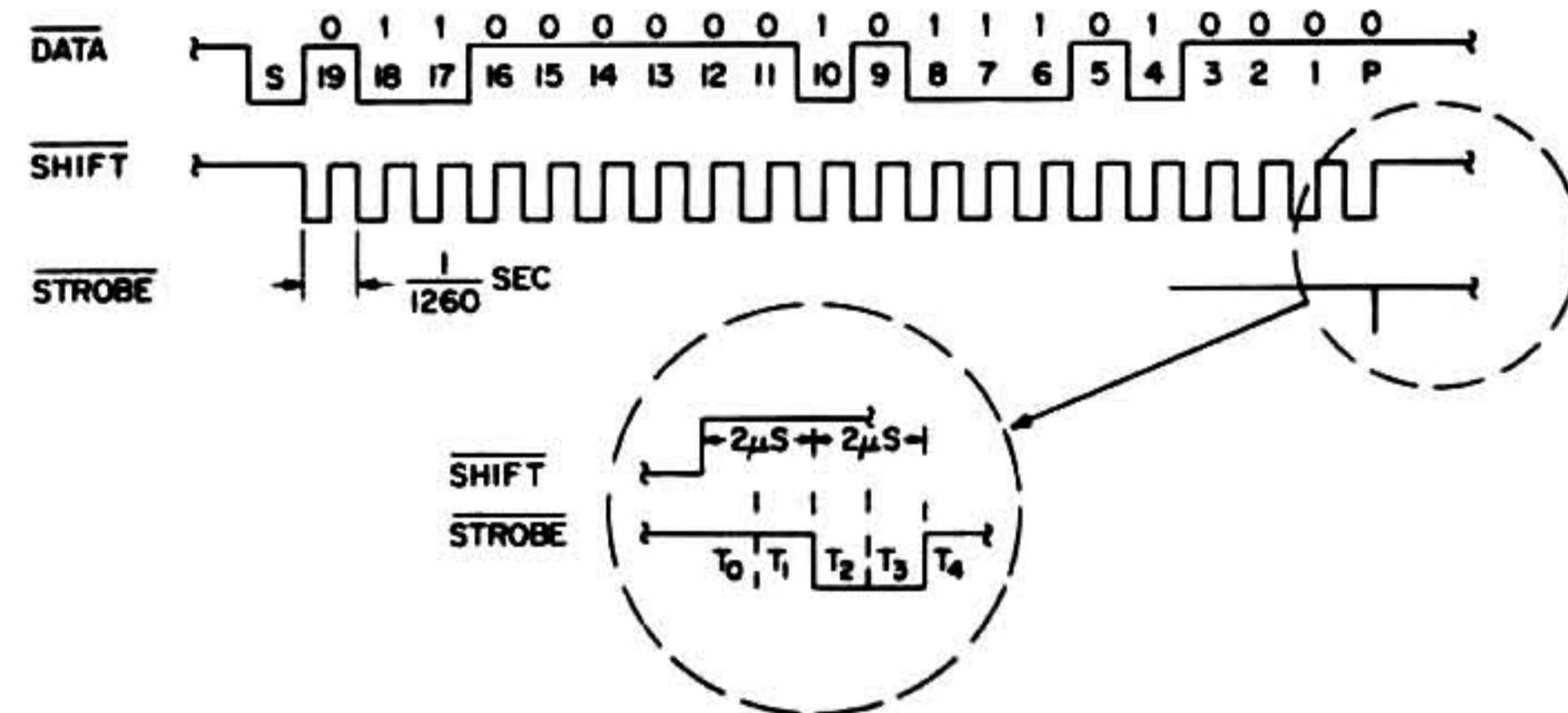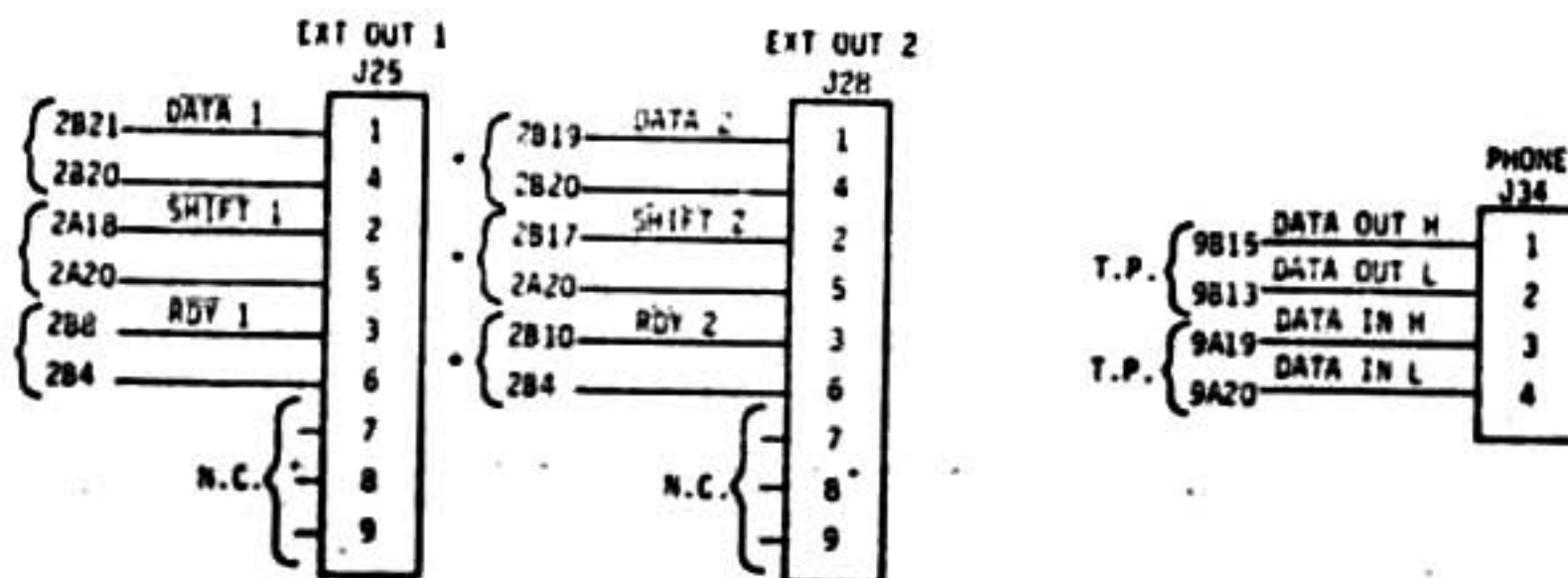

Serial Output Channel Timing

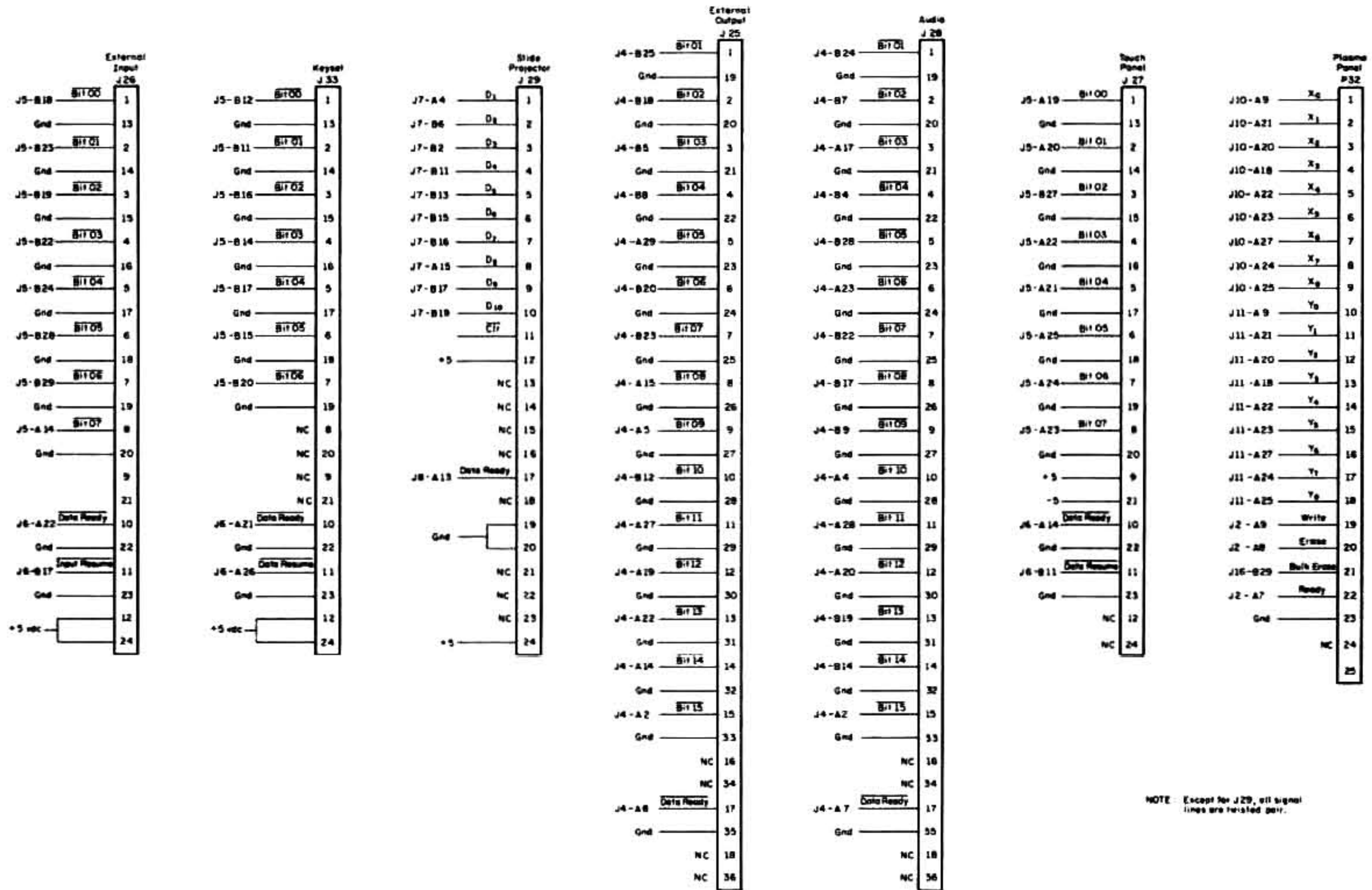# ERRATA SHEET

pp. 67

On terminals bearing serial number 262 and above the
connections for J25, J28 and J34 are as shown below:

External Input J26

J5-B18	BIT 00	1
Gnd		13
J5-B25	BIT 01	2
Gnd		14
J5-B19	BIT 02	3
Gnd		15
J5-B22	BIT 03	4
Gnd		16
J5-B24	BIT 04	5
Gnd		17
J5-B28	BIT 05	6
Gnd		18
J5-B29	BIT 06	7
Gnd		19
J5-A14	BIT 07	8
Gnd		20
		9
		21
J6-A22	Data Ready	10
Gnd		22
J6-B17	Input Resume	11
Gnd		23
+5 vdc		12
		24

Keyset J33

J5-B12	BIT 00	1
Gnd		13
J5-B11	BIT 01	2
Gnd		14
J5-B16	BIT 02	3
Gnd		15
J5-B14	BIT 03	4
Gnd		16
J5-B17	BIT 04	5
Gnd		17
J5-B15	BIT 05	6
Gnd		18
J5-B20	BIT 06	7
Gnd		19
	NC	8
	NC	20
	NC	9
	NC	21
J6-A21	Data Ready	10
Gnd		22
J6-A26	Data Resume	11
Gnd		23
+5 vdc		12
		24

Slide Projector J29

J7-A4	D1	1
J7-B6	D2	2
J7-B2	D3	3
J7-B11	D4	4
J7-B13	D5	5
J7-B15	D6	6
J7-B16	D7	7
J7-A15	D8	8
J7-B17	D9	9
J7-B19	D10	10
	Clr	11
+5		12
NC		13
NC		14
NC		15
NC		16
J6-A13	Data Ready	17
NC		18
Gnd		19
		20
NC		21
NC		22
NC		23
+5		24

External Output J25

J4-B25	BIT 01	1
Gnd		19
J4-B18	BIT 02	2
Gnd		20
J4-B5	BIT 03	3
Gnd		21
J4-B8	BIT 04	4
Gnd		22
J4-A29	BIT 05	5
Gnd		23
J4-B20	BIT 06	6
Gnd		24
J4-B23	BIT 07	7
Gnd		25
J4-A15	BIT 08	8
Gnd		26
J4-A5	BIT 09	9
Gnd		27
J4-B12	BIT 10	10
Gnd		28
J4-A27	BIT 11	11
Gnd		29
J4-A19	BIT 12	12
Gnd		30
J4-A22	BIT 13	13
Gnd		31
J4-A14	BIT 14	14
Gnd		32
J4-A2	BIT 15	15
Gnd		33
NC		16
NC		34
J4-A6	Data Ready	17
Gnd		35
NC		18
NC		36

Audio J28

J4-B24	BIT 01	1
Gnd		19
J4-B7	BIT 02	2
Gnd		20
J4-A17	BIT 03	3
Gnd		21
J4-B4	BIT 04	4
Gnd		22
J4-B28	BIT 05	5
Gnd		23
J4-A23	BIT 06	6
Gnd		24
J4-B22	BIT 07	7
Gnd		25
J4-B17	BIT 08	8
Gnd		26
J4-B9	BIT 09	9
Gnd		27
J4-A4	BIT 10	10
Gnd		28
J4-A28	BIT 11	11
Gnd		29
J4-A20	BIT 12	12
Gnd		30
J4-B19	BIT 13	13
Gnd		31
J4-B14	BIT 14	14
Gnd		32
J4-A2	BIT 15	15
Gnd		33
NC		16
NC		34
J4-A7	Data Ready	17
Gnd		35
NC		18
NC		36

Touch Panel J27

J5-A19	BIT 00	1
Gnd		13
J5-A20	BIT 01	2
Gnd		14
J5-B27	BIT 02	3
Gnd		15
J5-A22	BIT 03	4
Gnd		16
J5-A21	BIT 04	5
Gnd		17
J5-A25	BIT 05	6
Gnd		18
J5-A24	BIT 06	7
Gnd		19
J5-A23	BIT 07	8
Gnd		20
+5		9
-5		21
J6-A14	Data Ready	10
Gnd		22
J6-B11	Data Resume	11
Gnd		23
NC		12
NC		24

Plasma Panel P32

J10-A9	X0	1
J10-A21	X1	2
J10-A20	X2	3
J10-A18	X3	4
J10-A22	X4	5
J10-A23	X5	6
J10-A27	X6	7
J10-A24	X7	8
J10-A25	X8	9
J11-A9	Y0	10
J11-A21	Y1	11
J11-A20	Y2	12
J11-A18	Y3	13
J11-A22	Y4	14
J11-A23	Y5	15
J11-A27	Y6	16
J11-A24	Y7	17
J11-A25	Y8	18
J2-A9	Write	19
J2-A8	Erase	20
J16-B29	Bulk Erase	21
J2-A7	Ready	22
Gnd		23
NC		24
		25

NOTE: Except for J29, all signal lines are twisted pair.

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Input-Output Connections
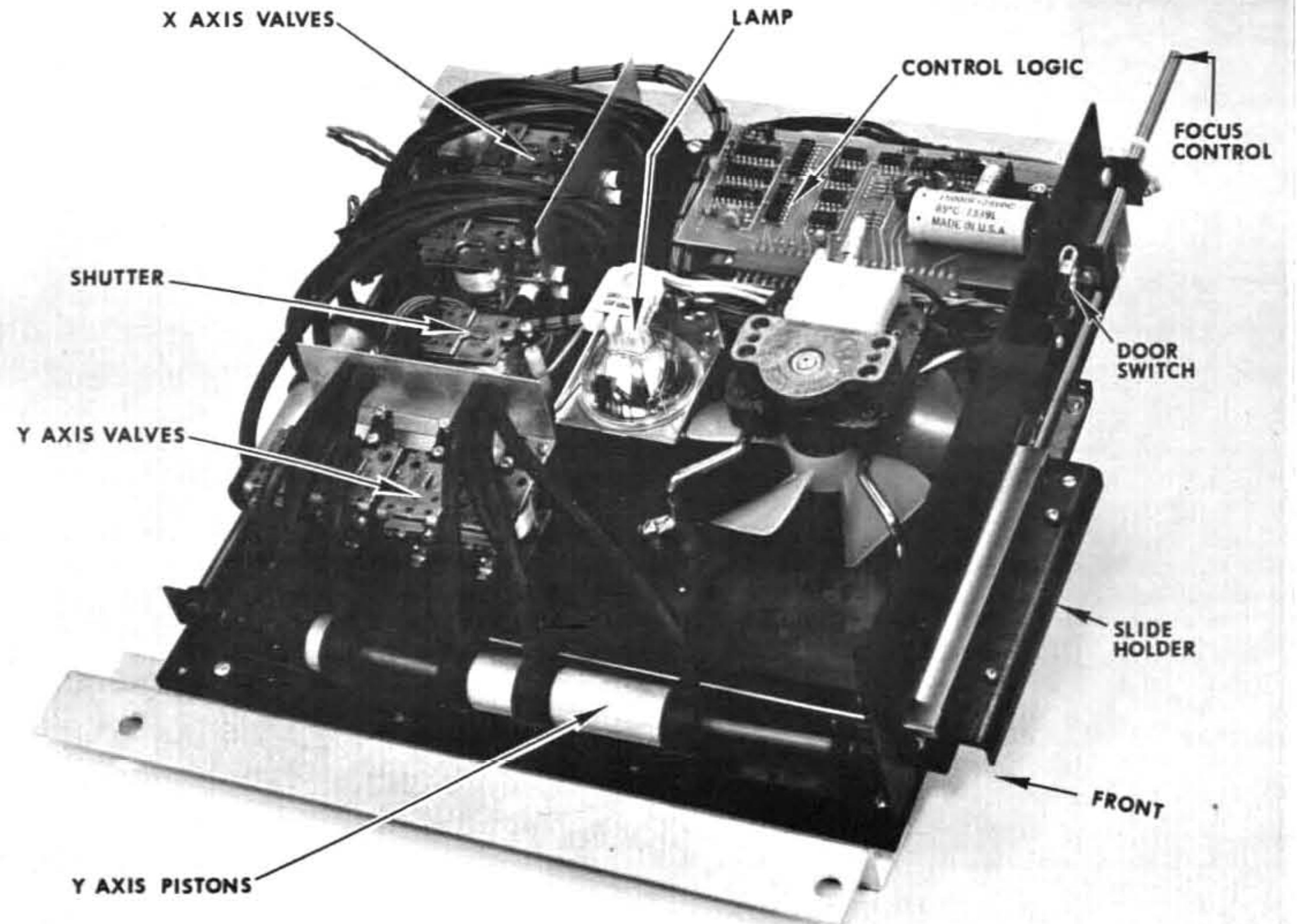
A random access slide projector is located in the top compartment of the terminal. It projects microfiche slides onto the rear of the plasma panel. The selection process is controlled directly by the computer which enters data words to the terminal specifying X, Y coordinates, shutter operation, and lamp on/off conditions. The X, Y coordinates specify one of 16 positions in the front to back (Y) location and left to right (X) location for a total of 256 available image selections. The "home" location of the carriage coordinate 0, 0, is full forward and to the extreme left.

Positioning of the film carriage is achieved with pneumatic cylinders. The cylinder stroke lengths are binary weighted (8, 4, 2, 1). Eight cylinders, four in X and four in Y, are used. The source pressure required to actuate the cylinders properly should be 10-12 psi provided through a 3/8 O.D. x 1/4 I.D. PVC tubing (PV64-2).

A microfiche is loaded in the slide projector by opening the front access door of the terminal. This action actuates a switch which causes the film carriage to be driven to the "home" location. In this location, the microfiche can be inserted in the plastic holder and placed over the locating pins of the carriage. The home image is in the upper right corner of the microfiche. Note that image locations are always apparent opposites of carriage locations and must be kept in mind when planning image addresses for new microfiche.

NOTES

CR1 - CR9, IN4148

I1, PROJECTION LAMP, TYPE EXP, 80W, 30V

T1, ESSEX-STANCOR TYPE RT-204

SLIDE PROJECTOR

FOR SERIAL NO'S 262 AND ABOVE

7-18-74

RTL

AA-049-4

The approximate location and orientation of all connectors used in the PLATO system are shown in Figure 25. Connector locations are numbers sequentially J1 through J34. J1 through J23 are located on the printed circuit board card cage. Some locations are spare slots where cards and connectors are not mounted . The normally unoccupied locations are J1, J4, and J17 through J23. Those connectors which mate to systems(s) external to the terminal and keyset are shown in the lower rear view of Figure 25. Table 2 identifies all connectors used on the terminal along with the corresponding part numbers required for mating external cables.

Part Number	Designation	Mating Part	Function	Source
185634-1	J2, J3, J5 to J16	----	P. C. Board Edge Connector	Magnavox
205207-1 (HSG) 205311-4 (SOCKET)	P32, J33	205208-1 (HSG) 1-205310-0 (PIN)	Plasma Panel, Keyset	Amp Inc.
1-480617-9 (HSG) 350019-1 (SOCKET)	J25, J28	1-480616-9 (HSG) 350036-1 (PIN)	Ext Out 1, Ext Out 2	Amp Inc.
1-480627-9 (HSG) 350019-1 (SOCKET)	J26, J27, J29	1-480626-9 (HSG) 350036-1 (PIN)	Ext in, Touch, Slide Projector	Amp Inc.
180735-1 (RECEIPT) 1381 (FEMALE PIN)	J30	180734-2 (PLUG) 1380 (MALE PIN)	Slide Projector, Power (Molex equivalent is 11369R and 1369P respectively for Receptacle and Plug)	Magnavox Molex
180820-1 (PLUG) 1434 (MALE PIN)	J34	180821-1 (RECPT) 1433 (FEMALE PIN)	Phone Line Input/ Output (Molex equivalent, 1490P and 1490R respectively for Plug and Receptacle)	Magnavox Molex

Table 2. PLATO Terminal Connectors
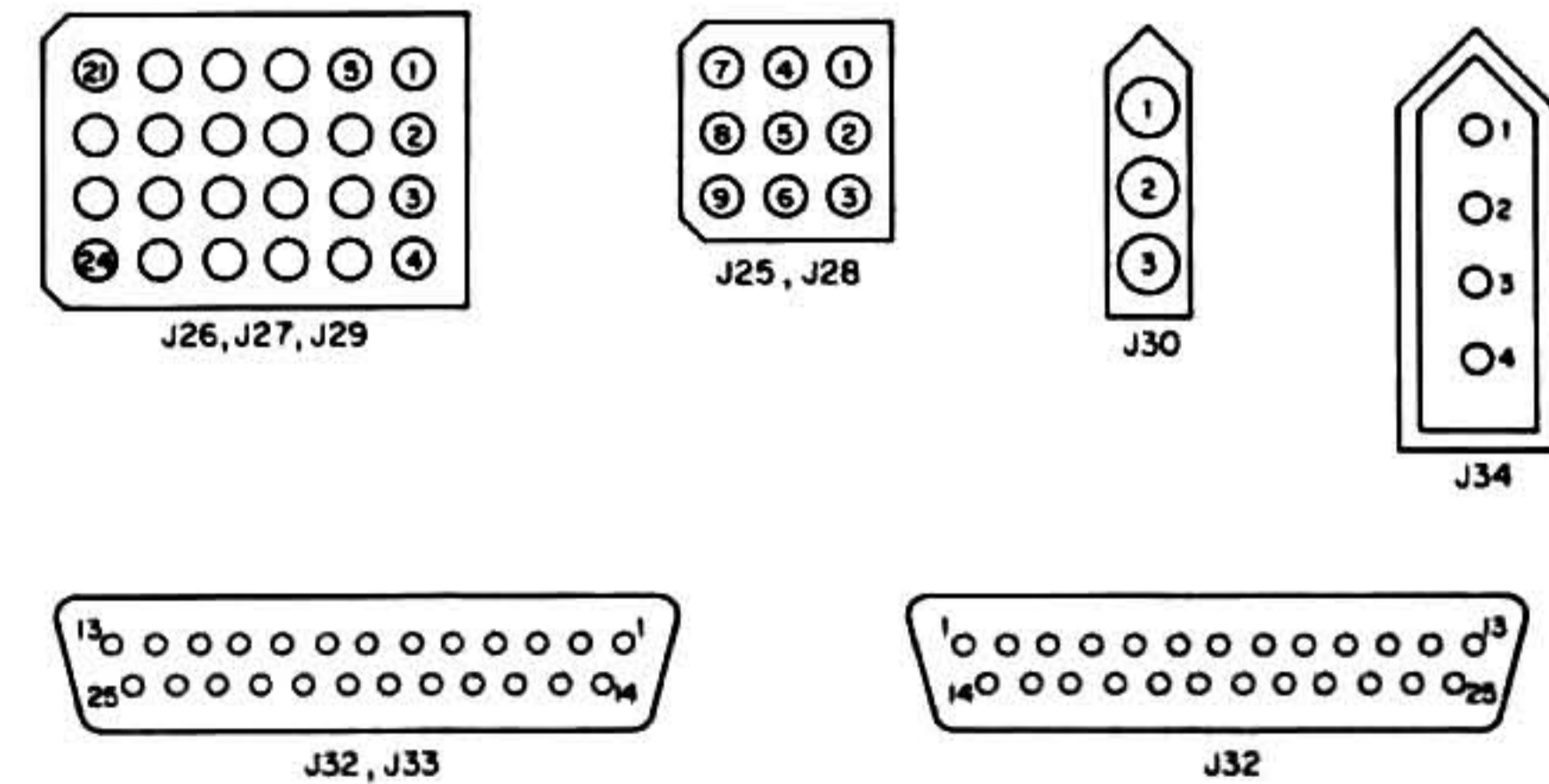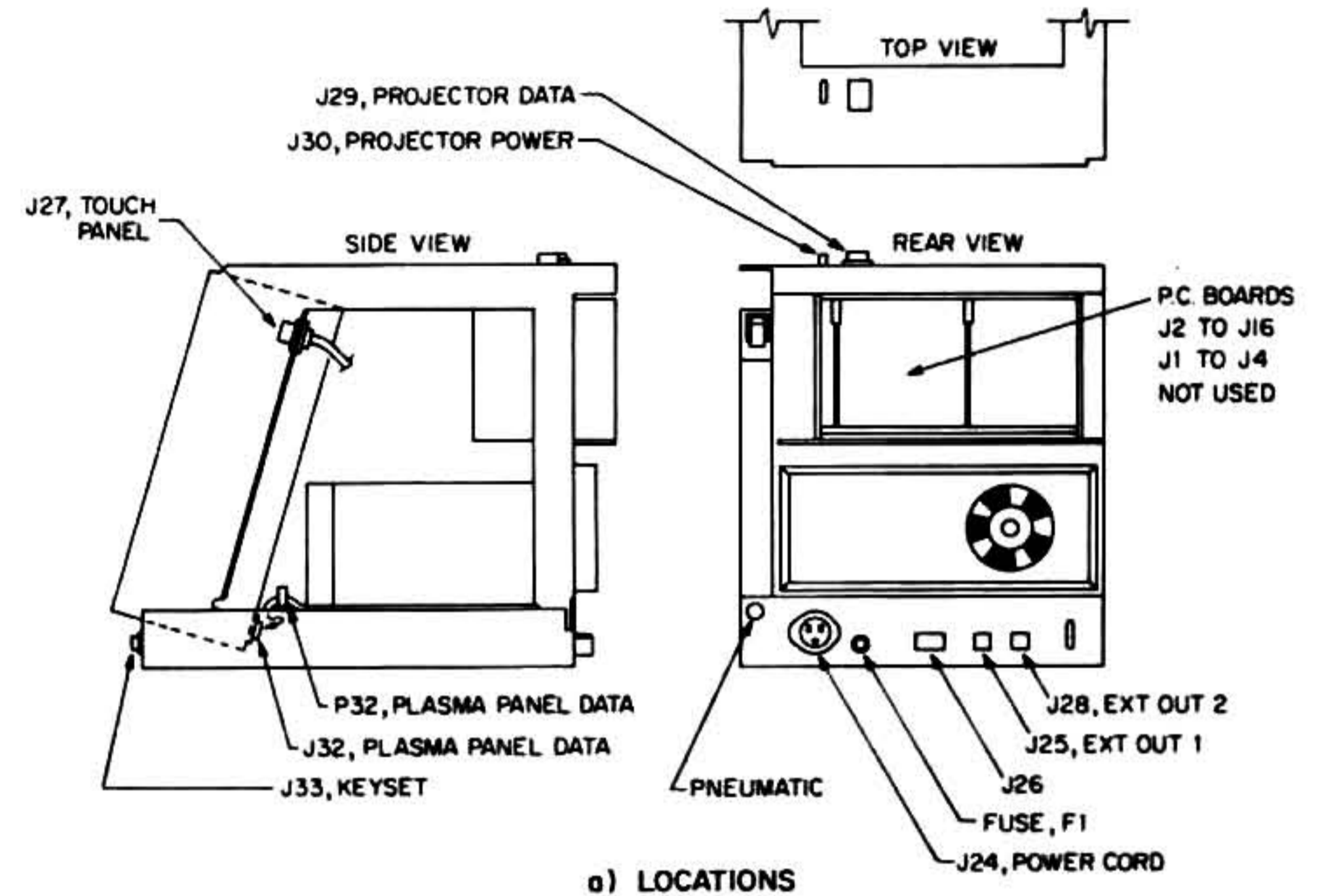
a) LOCATIONS

b) PIN ORIENTATION AS VIEWED FROM MATING SIDE

Figure 25 Connector Locations and Pin Orientation

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General

The touch panel is an optional input device which allows the operator to touch the display panel and input positional information directly to the computer. The touch panel is a 16 X 16 array of light beams projected just above the display surface. Whenever both an X and Y light beam have been interrupted, for example, by a figure touching the display, the address of the finger position is transmitted to the computer.

The electronics consists of the scanning system, the light sources the detectors, and the control logic. The scanning system employed eliminates any optical collimation problems. The scanning is controlled by a counter (U12) operated by a 100 KHz oscillator (U1). The outputs of the counter are decoded and used to sequentially address (select) the light sources and detectors.

The light sources are infrared light emitting diodes (LED) type MLED-900, arranged in a matrix configuration. This matrix is driven by transistors Q_1 through Q_8. The outputs of the counter are used to drive these transistors and cause two of the diodes to turn on, one in the X array and one in the Y array. In this manner each diode pair is sequentially pulsed and the array scanned.

The detectors are silicon phototransistors, type MRD 450. The detectors are located directly across the display from the LED's. Every fourth detector shares a common amplifier and voltage comparator. Only four amplifiers per axis are required because of the natural optical collimation of the light beams. For example, although detectors 0, 4, 8, and 12 are all selected (by circuit U20) when LED 0 is on, the light is primarily received by the 0 detector while the other detectors sharing the amplifier receive very little light.

The voltage comparator contains hysteresis to eliminate false inputs from room light and partially broken beams. The hysteresis voltage is generated by circuit U30, diodes CR1, CR2 and resistors R68, R69. The lower voltage threshold is used to detect a broken light beam while, after detection of both a broken X and Y beam, the higher voltage threshold is used to detect an unbroken light beam.

A set of four X detectors and four Y detectors is selected by circuit U20 for each pair of LED's that are pulsed. When a broken beam is detected, the X address is stored in U13 and the Y address in U14. When both X and Y addresses have been accumulated, this information is sent to the terminal (see card 5). Scanning continues and with each scan any new detected positions are compared by circuits U15, U16 and U17 with the previous detected position (stored in U13 and U14). If the positions agree (i.e., the object has not moved), scanning continues, whereas if they disagree the system resets. Touch inputs for the PLATO IV system are limited to approximately 10/sec by delay circuit U29 and flip flop U31.

Circuit Operation

A 100 KHz oscillator (U1) and circuits U2, U3, U4 and U5 generate the timing signals required to operate the touch panel. These signals include LED GATE, RESET GATE, $\overline{\text{LATCH RESET}}$, $\bar{\phi}_3$ and ϕ_1 and the clock signal for counter U12.

The outputs of the counter are decoded by circuits U6, U7, U8 and U9 and are used to select the matrix drive transistors Q_1 through Q_8. The two lower order bits of the counter select one of transistors Q_5-Q_8 while the two higher order bits select one of transistors Q_1 - Q_4. The LED GATE signal (TP2) applied to U9 turns on the selected transistor generating a 500ma 40 usec current pulse which produces a light pulse detectable by the phototransistors.

The detected signal from the phototransistors is coupled through a .047 ufd capacitor to an amplifier (U18 or U22) where it is amplified 100 times and supplied to the voltage comparator circuit (U19 or U20).

The outputs of the comparators are supplied to multiplexer U20 which is also driven by the lower order 2 bits of counter U12. The outputs of the multiplexer (pins 7 and 9) are trains of pulses representing the light pulses from the LED's. If light pulses are detected, they are stored in the X and Y detect flip flops (U24). These flip flops are sampled by ϕ_1 and cleared by ϕ_3. If a flip flop is "0" when sampled by ϕ_1 (i.e., no light pulse detected because beam was interrupted, the corresponding latch flip flop (U26) is set which stores the present address (X or Y) into U13 or U14. In the event that only one interrupted beam is detected during a scan, both X and Y latch flip flops are reset by U23.

When both the X and Y latch flip flops have been set, the GO signal is generated (TP10) initiating the DATA READY signal from U31 to the terminal. After receipt of the DATA RESUME signal indicating the data has been transferred, the DATA READY flip flop is cleared and timing circuit U32 is triggered. This circuit produces a short audio beep indicating to the user that the position has been transmitted.

Circuits U23, U25, U27 and U29 prevent multiple inputs of the same position by comparing the present detected position to the previous detected position. Flip flops U25 will be set if the present address is the same as the previous address.

Maintenance

Always check to see that dirt or other objects are not blocking any of the detectors of LED's. The system has numerous test points to help in troubleshooting the electronics. The most important is the sync test point (TP1). The sync pulse is produced when the scan is in the last position. By triggering the scope on its negative edge, the trace will start at the beginning of a scan. If the pulse is present it also indicates the clock and counter and power supply are operating. If not present, check the power, clock, and counter circuits.

Other test points to check are the outputs of the time multiplexor, TP3 and TP4. These signals should consist of 16 pulses, each representing a light beam. Check the X and Y output signals by raising the panel above the table a couple of inches; this will decrease the amount of light reflections from the table top. Then interrupt a position, which will raise the threshold on the voltage comparators to the high level. If any signals are missing or extremely weak, check the amplifier stage. If everything is okay, then the phototransistor is probably weak and needs to be replaced.
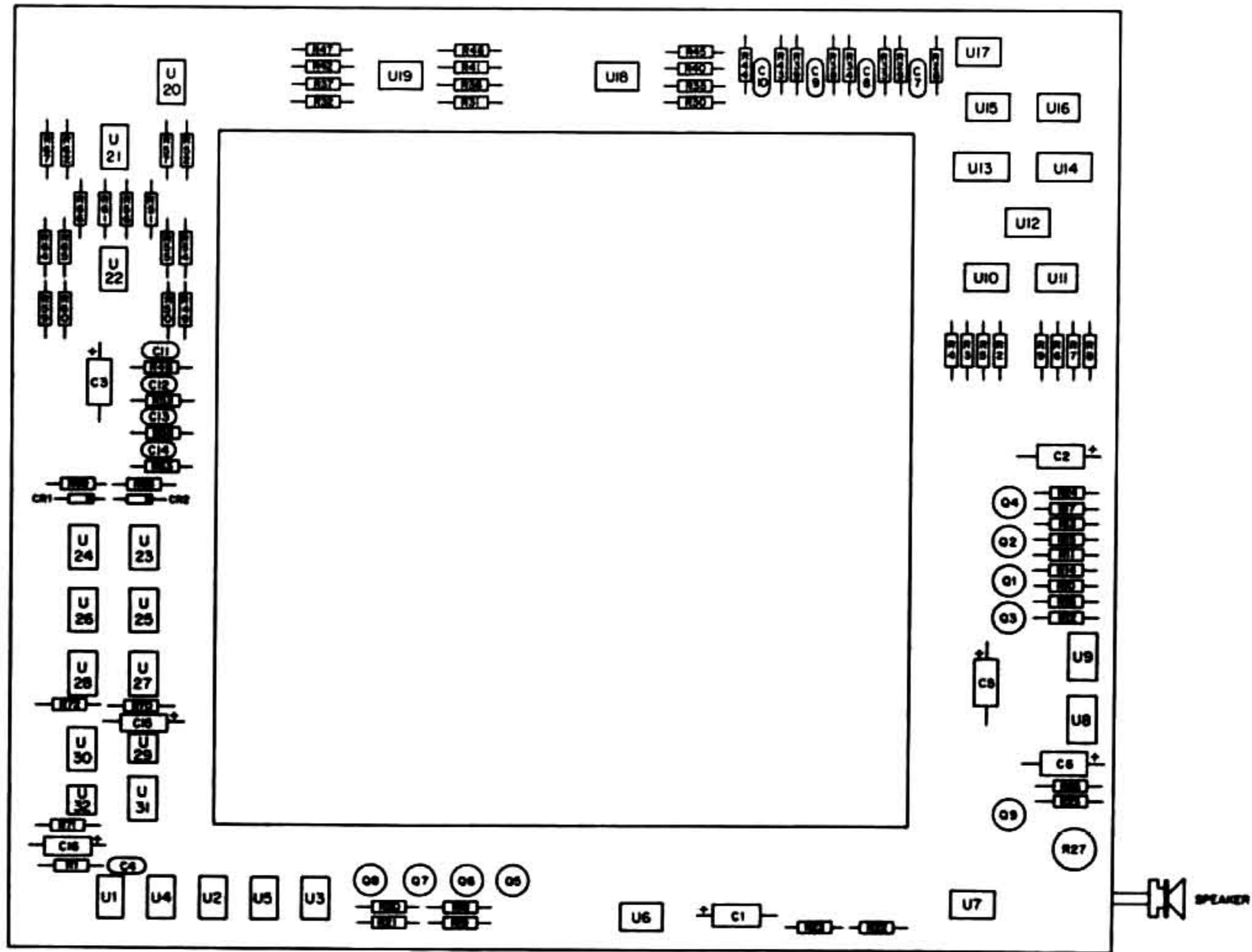
TOUCH PANEL SCANNER

SHEET 1 OF 2
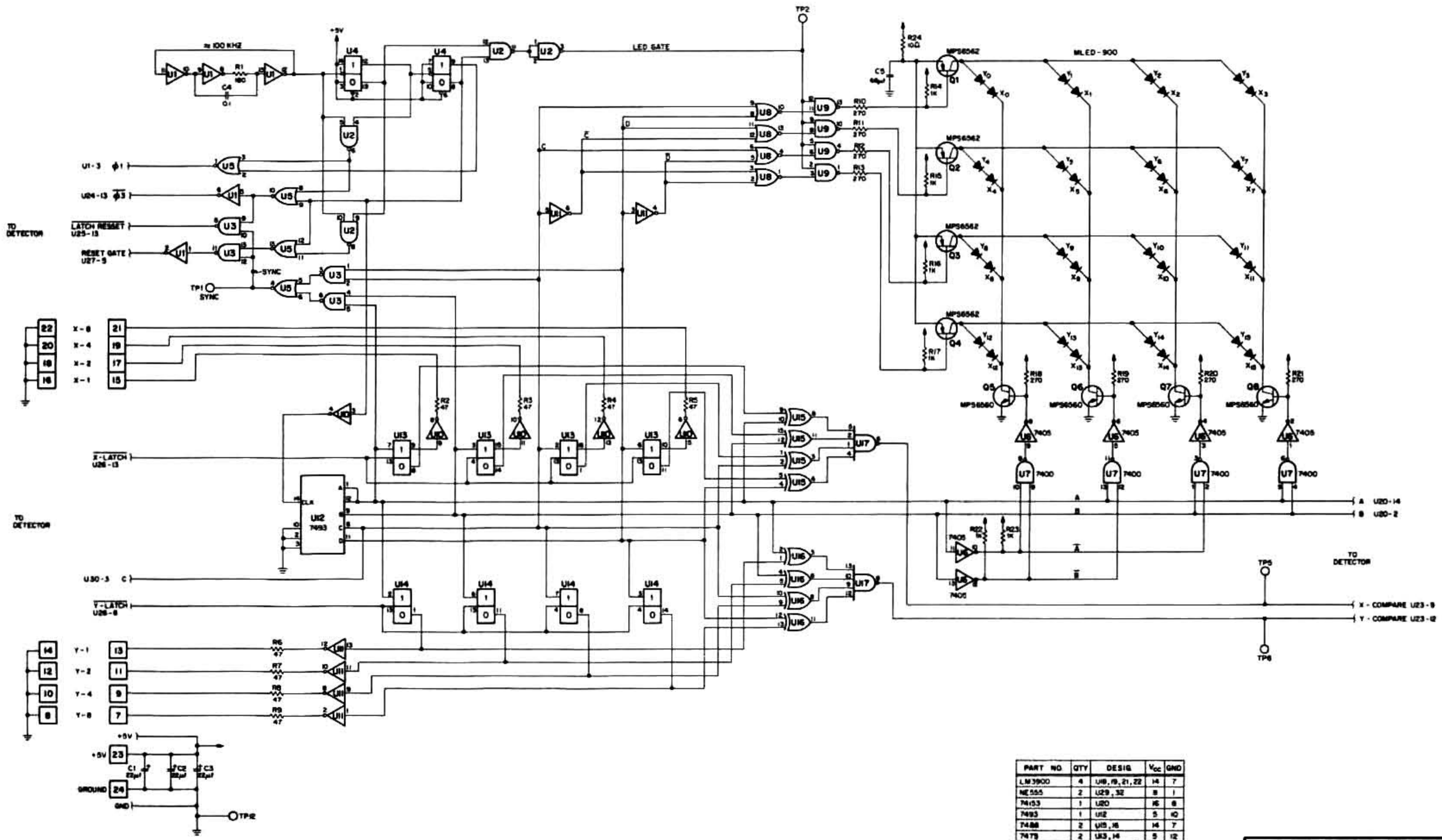
PART NO.	QTY	DESIG.	V$_{cc}$	GND
LM3900	4	U18,19,21,22	14	7
NE555	2	U29,32	8	1
74153	1	U20	16	8
7493	1	U12	5	10
7488	2	U15,16	14	7
7473	2	U13,14	5	12
7474	3	U24,25,31	14	7
7473	2	U4,26	4	11
7420	1	U17	14	7
7405	1	U8	14	7
7404	4	U1,10,11,28	14	7
7402	4	U6,8,25,30	14	7
7401	1	U9	14	7
7400	4	U2,3,7,27	14	7

7-29-74

AA-053-4

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TOUCH PANEL LAYOUT

AA-054-4

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TOUCH PANEL DETECTOR/CONTROL

SHEET 2 OF 2

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AA-053-4

Card 2

CARD 2

Card 3

CARD 3

Card 4

Card 5

Card 6

Card 7

Card 8

Card 9

CARD 9

Card 9 (202)

CARD 9

Card 10/11

Card 12

Card 13

Card 14

Card 15

Card 16

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URBANA, ILLINOIS 61801

POWER DISTRIBUTION DIAGRAM
FOR SERIAL NO'S 262 AND ABOVE

DATE 7-23-74	SCALE	
DRAWN BY RTL	APPROVED BY L. Hedges	AA-051-2

POWER SUPPLY

NO. GB-789

After approximately six months of operation, minor adjustments of the plasma panel power supply may be required. Symptoms which indicate such adjustment is necessary are a failure to always erase selected cells or a tendency to write cells not addressed.

Using a dc voltmeter, set the voltages to the values shown in the diagram below.

Note: If a digital voltmeter is used, it must be isolated from the ac line.

There are three types of plasma panel power supplies in use, MD-16, MD-30 and MDT. The voltage test points and adjustments for the MD-30 and MDT are shown on the diagram below.

If an MD-16 power supply is present the adjustment procedure is:

1. Adjust the sustaince up to 2 turns counter clockwise to correct erroneous writing or up to 2 turns clockwise to correct a failure to erase.

2. If the above adjustment fails to correct the problem, return the sustainer adjustment to its original position and adjust both the X and Y pulser adjustments up to a 1/4 turn clockwise to correct writing problems or counter clockwise to correct erasing problems.
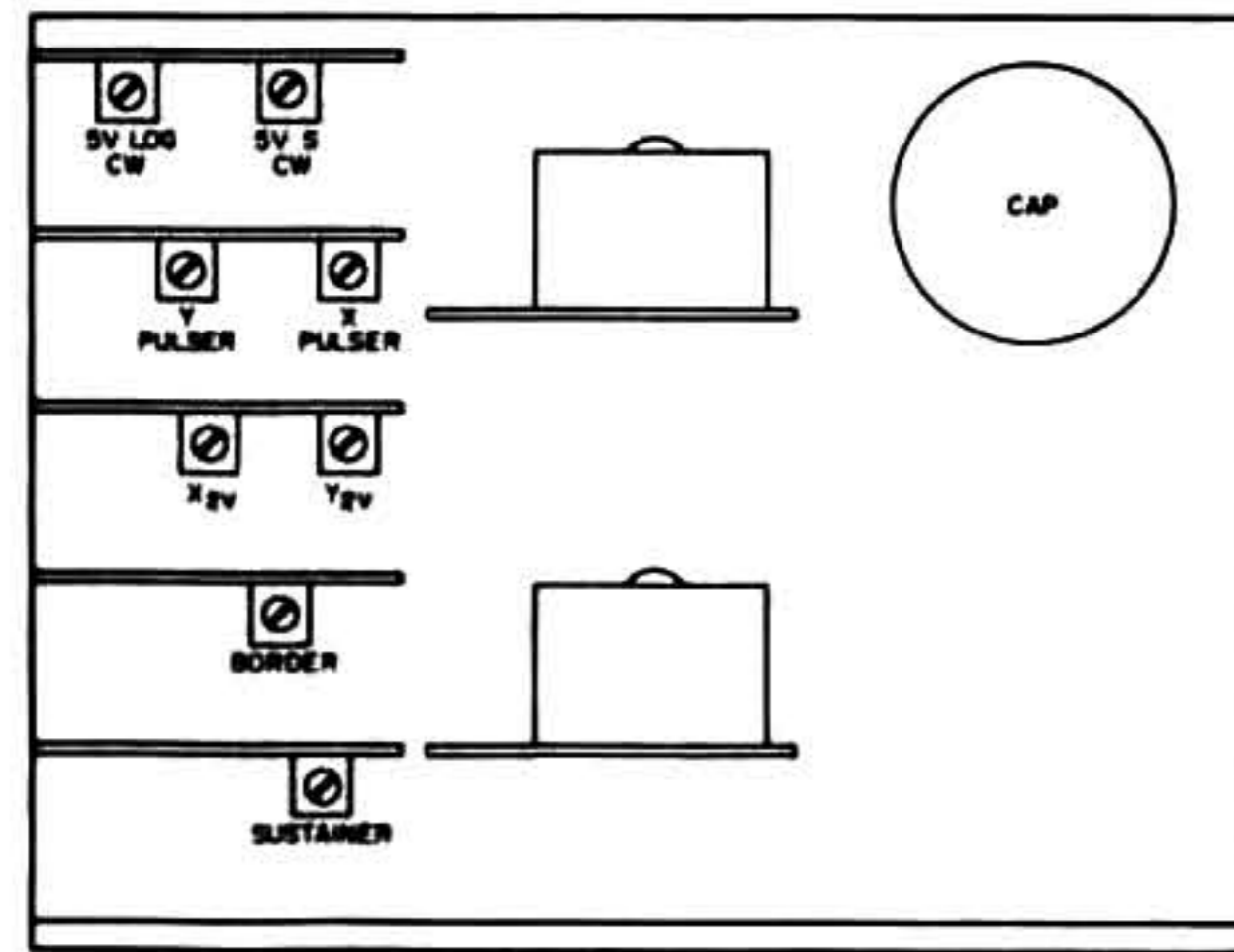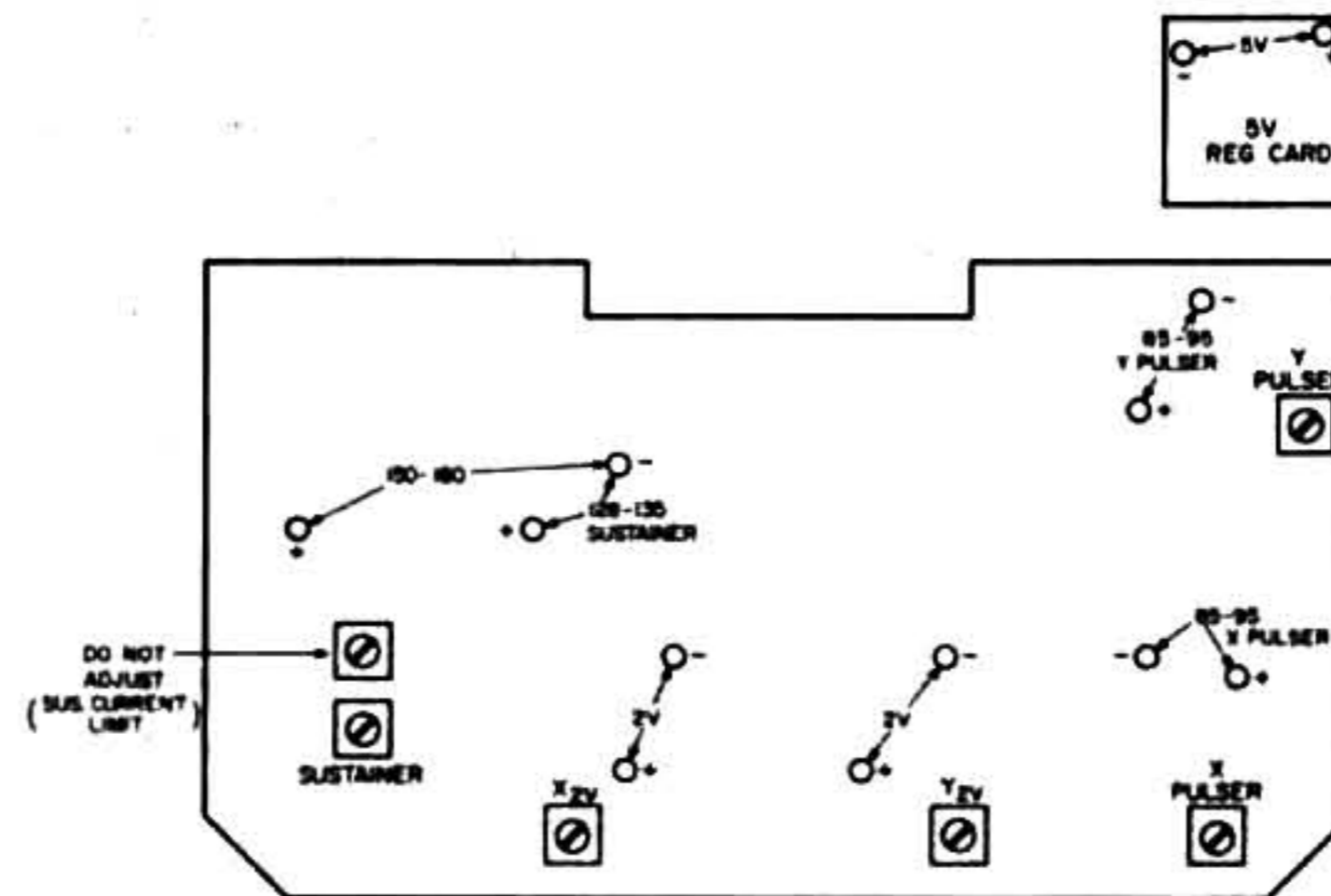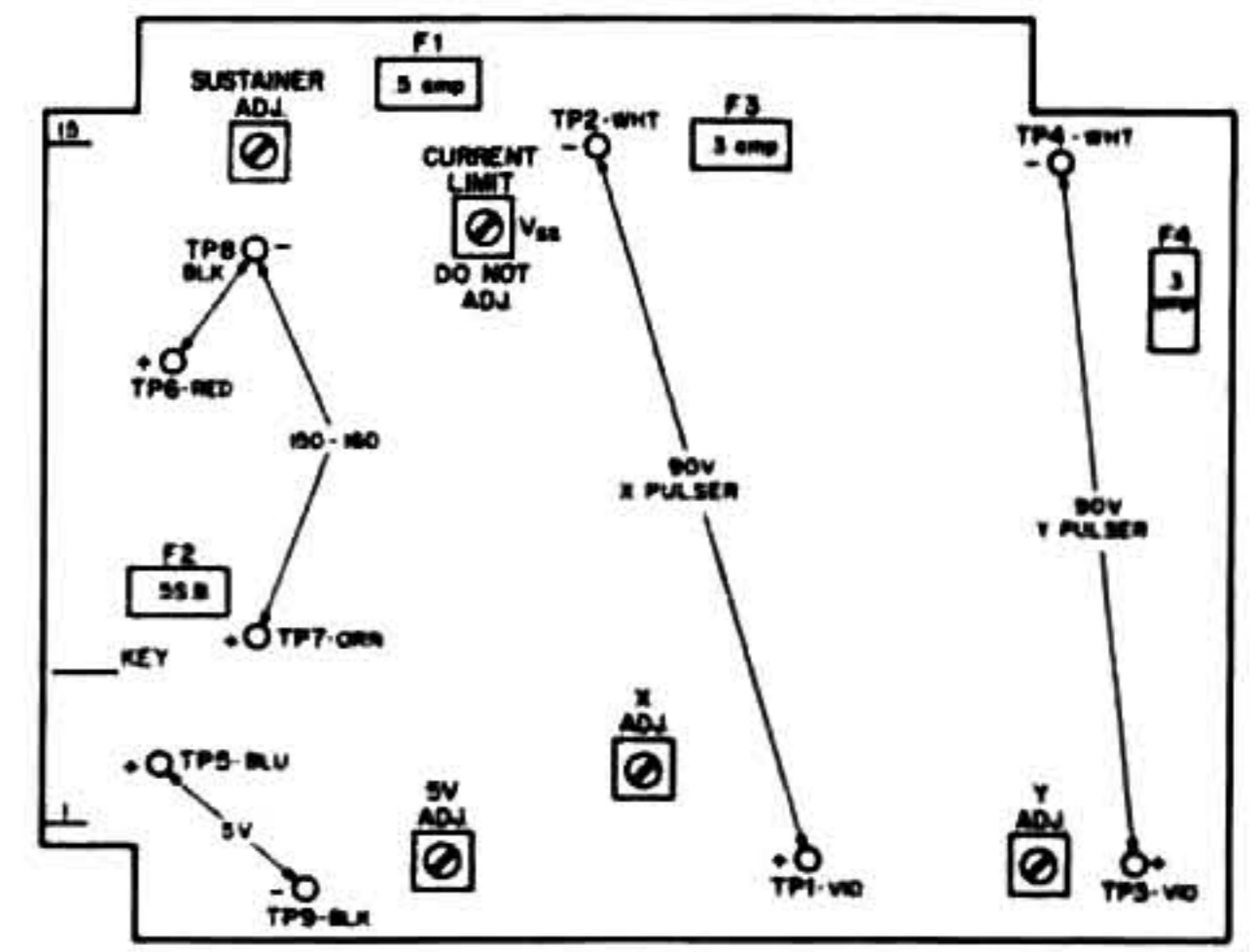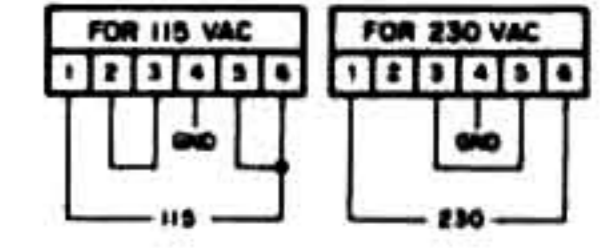
PLASMA PANEL POWER SUPPLY ADJUSTMENTS

SCHEDULED MAINTENANCE

Clean Air Filter

The air filter on the rear of the terminal must be removed
and cleaned approximately every 2 months (1 month in non-air
conditioned areas).

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                    CAUTION

    Failure to clean the air filter periodically may
    result in a temperature rise within the terminal
    and eventual damage.
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The filter can be reached by removing the rear cover and pulling it
from the holding bracket. Cleaning in warm water with a mild de-
tergent is satisfactory. This maintenance should be performed with
power OFF.

Clean Mirror Assembly

Occasionally, dust will collect on the mirrors used to rear
project slide images on the front screen. It is good practice to
wipe the mirrors with a soft cloth at the same time the filters
are cleaned. Perform this maintenance with power OFF.

UNSCHEDULED MAINTENANCE

Unscheduled maintenance should be performed to correct observ-
able deterioration in performance which occurs as a result of normal
operation but on an irregular basis.

Clean Film Carriage Clamp Assembly

This assembly is located in the slide projector just above the
lens. If collects dirt from the microfiche film strip during opera-
tion which may eventually impair clarity of projected images.