I/O Dataspec.

PRODUCT **Analog Input**

MODEL **620-850 thru 853**

DATE **November 30, 1972**

varian data machines

ANALOG INPUT MODULES

INTRODUCTION

The Models 620-850 through -853, Analog Input Modules (AIM) are options for use with the Varian 620 series and V73 computers. The AIM provides an analog multiplexer (MUX), analog-to-digital converter (ADC), sample and hold amplifier and programmable timer.

The MUX accepts middle or high level analog signals which are sequentially or randomly selected, sampled and held for conversion by the ADC. The ADC outputs a 13-bit or 10 bit word in binary two's complement format to the computer. The timer can be used to establish time intervals for system control.

GENERAL DESCRIPTION

The MUX tranfers external analog signals in differential or single-ended form to the ADC. The content of each analog MUX channel addressed is converted to an equivalent 13-bit or 10-bit digital value. The AIM is designed to function in either of two operating modes: Sequential or Random. The Sequential Mode allows the MUX channels to be scanned and sequentially selected. Each scan starts with the first channel and a channel advance signal increments the MUX to the next higher channel. At the end of a scan cycle, the MUX is set to the first channel and an end-of scan interrupt is provided.

The Random Mode allows the MUX channel address selection to be determined under computer program control. This mode permits the selection of MUX channels in any sequence.

The ADC employs the successive approximation technique for conversion. Its conversion rate is 13 microseconds for 13 bits with a sample-and-hold-amplifier settling time of 6 microseconds, thus providing a 50 kHz throughput rate or 5 microseconds for 10 bits with the same sample-and-hold amplifier settling time, thus providing 100 kHz throughput rate. The ADC can be initiated by the computer, the Programmable Timer or an external pulse. The Programmable Timer provides an internal and external control capability. Under internal control, the Timer sets a timing interval through a data word which it receives from the computer. The Timer decrements the data word until the zero state is reached. The Timer then emits a pulse, restores the original data word and again initiates the cycle. Under external control, the Timer can be inhibited at any time by an external signal level which holds the Timer at its load point. Timing intervals start at the instant the external signal level is removed or set to a high logic state. New timing intervals can be sent by the computer while the Timer is externally inhibited.

AIM data transfers can occur by programmed output command execution or under the optional Buffer Interlace Controller (BIC) control. When operating under program control, data transfers are initiated by the computer and are executed under input/output instruction control. When operating with a BIC, data transfers are initiated by the computer and are executed without input/output instruction control. The BIC permits automatic, high- or low-speed, block data transfers between the AIM and the computer memory without disturbing the sequence of the main program.

The Models 620-850 through -853 AIM represent a minimal capability providing 16 different or single-ended analog channels. This basic configuration can be readily expanded up to 256 analog channels. The Models 620-860A, 861A Multiplexer Expansion Modules provide plug-in expansion in increments of 16 differential or 16 single-ended channels. Larger systems can be configurated by repeating the AIM expansion with maximum capability up to 2048 channels.

PREREQUISITES

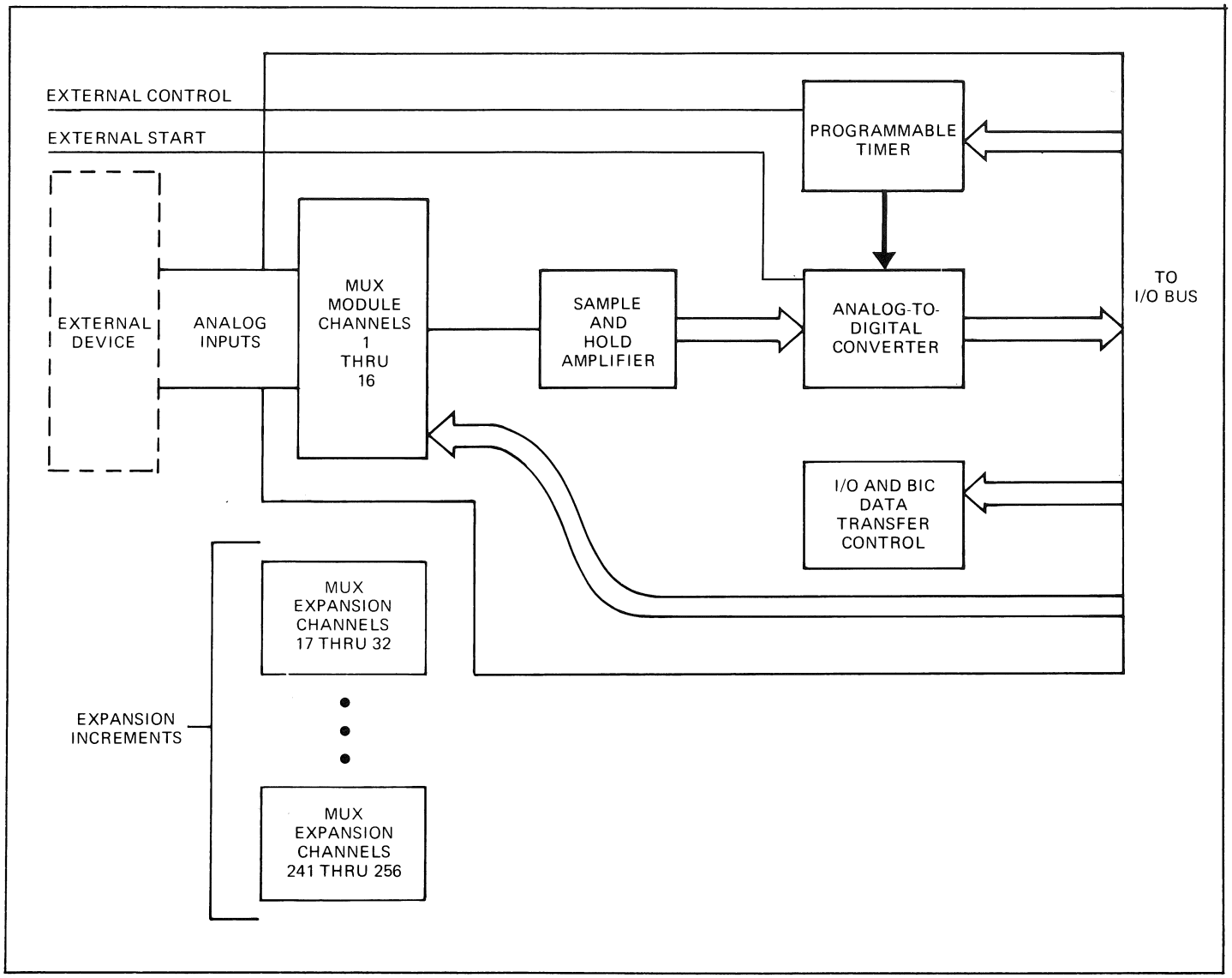
- 620 or V73 System Computer
- Expansion Chassis (requirements determined on individual system basis)
- 620-88 Analog Power Supply (requirements determined on individual system basis)
- 620-20 Buffer Interlace Controller (BIC) (optional)
- 620 Peripheral Backplane Wiring Panel (requirements determined on individual system basis).

SOFTWARE

A comprehensive software package is provided comprising a Test Program and an I/O Driver Program. The Test Program is an effective tool in determining the operational status of the AIM.

The I/O Driver Program provides convenient access to the AIM without detailed knowledge of the hardware. The program can be used by itself or embedded in an operating system. The I/O Driver Program consists of the following two independent routines: Programmed Data Transfers and Direct Memory Access Data Transfers. These routines permit the user to specify the following parameters:

- Channel selection technique (Random or Sequential)
- Last channel specification for Sequential Mode or channel list specification for Random Mode
- Destination array and quantity of incoming data
- Time between each data point.
- An error address to which control will pass when any one of several error conditions is detected.



MODULE FLOW DIAGRAM

SPECIFICATION

Multiplexer
- Gain and Accuracy
  - Voltage Gain ..... +1 or +10
  - Accuracy ..... ±0.01% of F.S.
  - Gain Temp. Coefficient ..... ±10 PPM/°C
- Input Specifications
  - Signal Voltage ..... ±10V or ±1V
  - Maximum Source Impedance ..... 1K ohms
  - Common Mode Voltage plus Signal Voltage ..... ±10 volts
  - Absolute Maximum ..... ±15 volts
- "ON" Channel Specifications
  - Switch Impedance ..... 500 ohms (typical)
  - Input Impedance ..... 10^9 ohms, 80 pF
  - Common Mode Rejection ..... 80 dB, 0 to 60 Hz
- "OFF" Channel Specifications
  - Impedance ..... 10^{10} ohms, 4 pF

NOTE: All switches open when power is turned off.
- Output Specifications
  - Output Voltage Range ..... ±10 volts
  - Output Current ..... 100 mA
  - Output Impedance ..... 20 ohms
  - Voltage Drift ..... ±50 μV/°C
- Dynamic Response
  - Frequence Response ..... (Tracking error with F.S. peak-to-peak sine wave applied to a single On Channel. 1K source impedance)
  - Accuracy of .01% ..... 250 Hz
  - Accuracy of .1% ..... 2500 Hz
- Crosstalk

  ON Channel 1K to ground <1 mV. F.S. peak-to-peak 1 kHz sine wave appled to 15 OFF Channels.

Settling Time to .01% of 10 volts: 10 microseconds. (Switching between two channels with dc voltage of +10V and -10V on each channel respectively).

Digital Outputs
- End of Scan ..... Low True Signal which begins when the ADC starts to convert the data for the "Last Channel" of the Multiplexer Sequential Mode, and ends when the ADC starts to convert the next time. Held High when the Multiplexer is in the Random Mode. Fanout: 10 logic loads. Maximum capacitive load: 1000 pF.
- Control Flip/Flop ..... R-S flip/flop which is set High True by the EXC 3YY, and is reset by EXC0YY, EXC1YY, EXC2YY or System Clear. Also may be wire-ored and reset by pulling down the output.

Analog to Digital Converter
- Resolution ..... 13 or 10 binary bits
- Output Format ..... two's complement
- Conversion Accuracy ..... ±.012% of Full Scale ±1/2 LSB
- Conversion Time . 13 microseconds, maximum (13 bits) 5 microseconds, maximum (10 bits)
- Throughput Rate ..... 50 kHz, maximum (13 bits) 100 kHz, maximum (10 bits)
- Temperature Coefficient ..... ±50 μV/°C, maximum
- Warm up Time ..... Essentially Zero
- Full Scale Range ..... ±10V

Digital Outputs
- BUSY ..... High (true) during Analog to Digital Conversion. Available fanout: 8 logic loads. Maximum capacitive load: 100 pF.
- STORE ..... Low (true) during the last 1 microsecond of the BUSY signal. Available fanout: 10 logic loads. Maximum capacitive load: 1000 pF.
- Output Enable ..... High (true) during the time ADC data is on the E-Bus (1.90 microseconds). Available fanout: 20 logic loads. Maximum capacitive load: 100 pF.

Digital Inputs
- EXT START ..... 1K ohms to +5V, Lower to start ADC. Must raise and relower to restart ACD.
- EXT SENSE ..... 5.6K ohms to +5V, Low true sense input. Computer may test the status of this input with a SEN 2YY instruction.

Sample & Hold
- Gain and Accuracy
  - Voltage Gain ..... +1
  - Accuracy ..... ±0.01%
  - Gain Temp Coefficient ..... ±10 PPM/°C
- Track Mode
  - Full Power Response ..... 75 kHz (F.S. peak-to-peak sine wave)
  - Slew rate 4V/microsecond
  - Settling Time to ±1mV ..... 4 microseconds
- Input Characteristics, Single Ended
  - Signal Range ..... ±10V
  - Maximum Rating, without damage ..... ±15V
  - Input Impedance ... 50K ohms in parallel with 5000 pF
  - Offset Voltage ..... ±2 mV maximum
  - VS Temperature ..... ±50 μV/°C

Output Characteristics
- Signal Range ..... ±10V
- Noise, RMS Wide Band, (Hold Mode) ..... 1 mV peak-to-peak
- Decay Rate in, Hold Mode ..... ±10 mV/Second
- Feedthrough 20V step, (Hold Mode) ..... -80 dB

Switching Characteristics
- Aperature Time, Maximum ..... 100 nanoseconds
- Offset Pedestal, Maximum ..... ±2 mV
- Acquisition Time, Maximum ..... 4 microseconds

Programmable Timer
- Clock frequency ..... 1.0 MHz ±0.01% (13 bits)
  2.0 MHz ±0.01% (10 bits)
- Clock drift ..... ±1 PPM/°C
- Clock stability ..... ±0.01 PPM/day
- Resolution ..... 16 Binary Bits
  (Computer E-Bus 2^0 - 2^{15})
- Programmed PRF ..... 1 MHz to 15.26 Hz (13 bits)
  2 MHz to 30.52 Hz (10 bits)
  1 microsecond to 65.535 milliseconds (13 bits)
  .5 microsecond to 32.167 milliseconds (10 bits)
- Timer Output ..... 100 nanosecond pulse to ground.
  1K ohms to +5V sinks 100 mA.
  Maximum capacity load: 1000 pF.
- CLC Output ..... 100 nanoseconds pulse from low to high. TTL output.
  Available fanout: 6 logic loads.
  PRF = 1.0 MHz ±0.1% (13 bits)
  2.0 MHz ±.01% (10 bits)
- Timer Clock Input ..... 1 TTL load.
  Maximum PRF = 25 MHz.
  Increments counter on low to high transition.

Temperature Range
- Specifications ..... 0°C to 50°C
- Operating ..... -25°C to 70°C
- Storage ..... -55°C to +100°C

Power ..... +5 Vdc ±5% 2000 mA
±15 Vdc ±3%; 165 mA
+20 Vdc ±5%; 15 mA
-22 Vdc ±5%, 5 mA

Physical Characteristics ..... Dimensions: two printed circuit boards 7-3/4 x 12 x 1/2 inches
Connectors: two 122 terminal Card edge connector
Four 44 terminal Card edge connectors

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