USER'S GUIDE
ANALOG-TO-DIGITAL CONVERTER MODULE
for use with
Varian 620 or V73 Series Computers

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1. INTRODUCTION

1.1 GENERAL

The Analog-to-Digital Converter Module (ADCM) is a hardware option that interfaces Varian 620 and V-73 series computers to external analog devices. Two ADCM models are available to provide either 13-bit or 10-bit analog-to-digital resolution. An ADCM includes four functional features:

- An Analog-to-Digital Converter (ADC), which converts analog input signals to either 13-bit or 10-bit digital data words for input to the computer.
- A Sample and Hold Amplifier, which monitors analog input between conversions and provides a constant voltage source representing analog input to the ADC during conversion.
- A Programmable Timer, which generates a train of timing pulses, with the pulse rate determined by a computer program.
- External Sense Input Logic, which allows a computer program to test the status of an external device by sampling the logic level present on an external sense input line.

In a maximum configuration, the ADCM may be used in conjunction with Varian Multiplexer and Multiplexer Expansion Modules to accommodate as many as 256 single-ended or differential analog input channels. As many as eight ADCMs can be attached to a single computer. Refer to the Multiplexer Manual (Varian Publication No. 03-996-807) for details regarding this interface capability.

Simple installation procedures allow the ADCM to be installed either at the factory or on-site at the user's facility. A comprehensive software test package is provided with the ADCM for post-installation checkout of its operational status.

In addition, the module is fully supported by standard Varian software and input/output options.

1.2 FUNCTIONAL DESCRIPTION

The elements responsible for performing the four basic ADCM functions (analog-to-digital conversion, sample and hold, timing pulse generation, and External Sense decode) are shown in Figure 1-1.

Each ADCM has a unique device address, which is set at time of installation, and its own device address decode logic. The unique device address is used by the computer to select a particular ADCM for operation. Eight device addresses (60_8 to 67_8) are reserved for ADCMs.

Sample and Hold

A sample and hold circuit continuously monitors the analog input signal during the intervals between data conversions. At the start of a conversion, it stores the most recent input voltage level and provides the ADC with a constant voltage for the conversion.

Conversion

The actual data conversion can be initiated by one of three means:

- Program Control — Data conversion can be started using an External Control (EXC) Instruction.
- Programmable Timer Control — Pulses from the timer can start the ADC.
- External Control — The ADC can be initiated by an external start signal, whose source is determined by the user.

The ADC performs data conversion as a series of discrete operations. The current amplitude of the analog input signal is converted to either a 13-bit or 10-bit binary number that corresponds to the input voltage level. The 13 bits include 12 data bits and a sign bit, in two's complement format. Similarly, the 10-bit number consists of nine data bits and a sign bit. Digital outputs from the ADCM are presented to the E-bus via buffer registers, which store the data between conversions.

Data transfers from the ADCM to the computer may be under direct program control or under control of the optional Buffer Interlace Controller (BIC). When operating under program control, the computer initiates data transfer in response to the execution of a programmed input/output control instruction. When operating under the hardware BIC option, data transfers are initiated and executed without program instruction control. Thus, the BIC minimizes software overhead and permits data to be transferred at high speeds without interrupting the processing sequence of the main computer program.

Sense Interface

The ADCM sense interface logic provides the program with three types of sense information — external sense, data sense, and timer sense. The logic level present on the External Sense input line defines the status of an external device. A true level on the Data Sense line informs the program that a new data word has been set into the buffer register. A true level on the Timer Sense line informs the program that the programmable timer has generated a timing pulse.

Note that if the computer is equipped with a Program Interrupt Module (PIM) option, interrupts may be set by the ADC DATA READY signal and the TIME INTERVAL COMPLETE signal. Thus, the PIM option may be used to simplify the programming task of checking the input sense lines.

Programmable Timer

The programmable timer generates a pulse each time its decrementing counter reaches zero in a count cycle. The counter begins counting down from a binary number which is set in its buffer register by a data transfer out program instruction. The original value for this number remains in the buffer register until a new value is received.

The timer may be operated in either a continuous or a single cycle mode. In continuous mode, the timer pulse generated at the end of a count cycle starts a new cycle. In single cycle mode, each new count cycle must be started by a signal from an external device which is connected to the timer. In either mode of operation, the duration of the timer interval is set in the buffer register by programmed instructions.

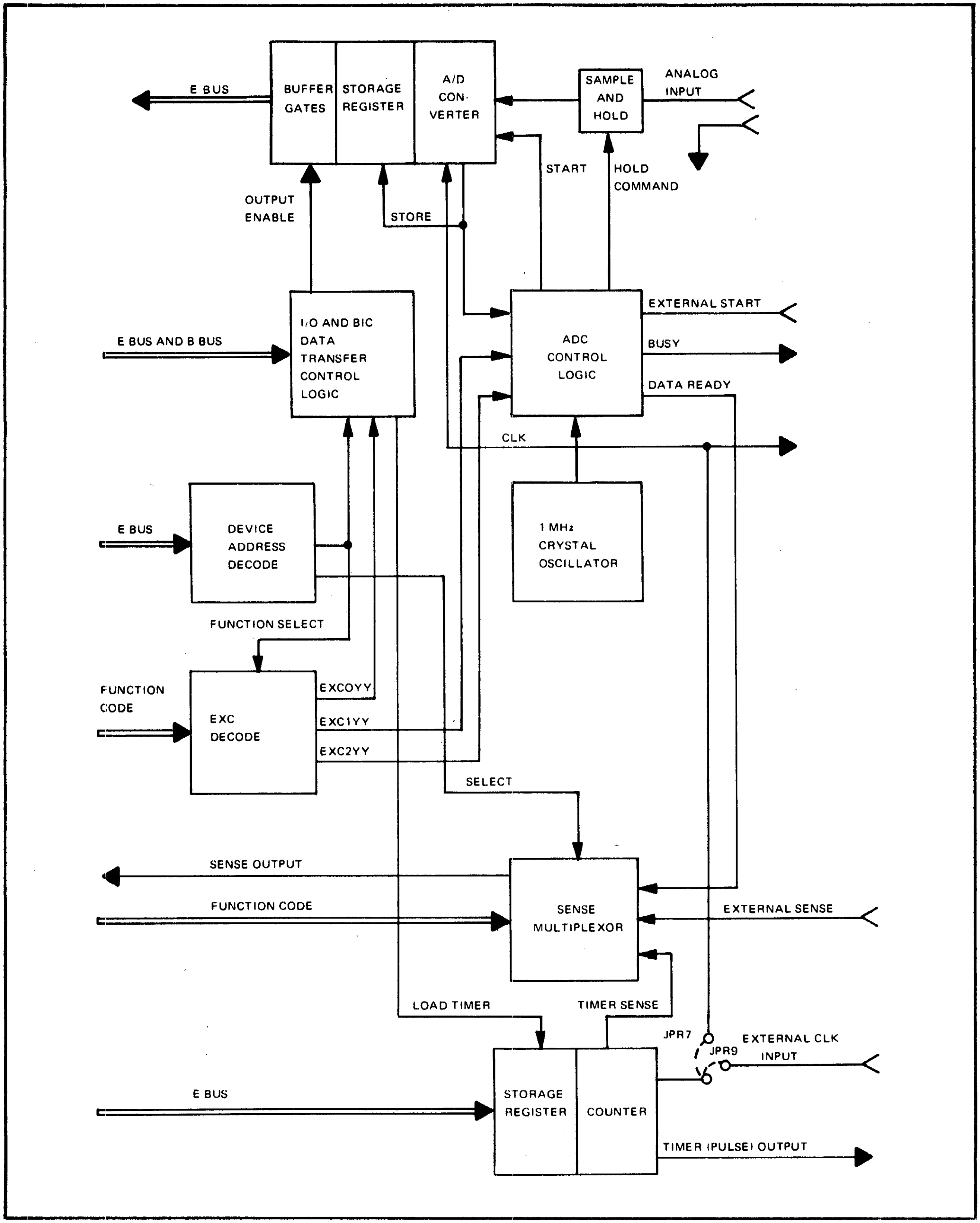


Figure 1-1. ADCM Block Diagram

2. PROGRAMMING

2.1 INTRODUCTION

This section describes Assembly Language programming techniques for operating the ADCM and presents instructions for using the software test package for checkout of the ADCM. The ADCM functions which are programmed include setting the timer pulse interval, checking the status of a sense line, and directing ADC operations. More detailed programming information may be found in the 620 series or V-73 system handbooks.

2.2 CHECKING SENSE LINES

Three programming instructions are used to check the status of sense lines associated with the ADCM:

SEN 0YY	Checks if a data word is ready to be transmitted to the computer.
SEN 01YY	Senses if the timer has counted down to zero.
SEN 02YY	Tests the state of the external sense input line, which indicates the status of some external device.

where YY specifies the ADCM device address, which may be any octal number from 60 to 67.

2.3 SETTING TIMER INTERVAL

The ADCM timer may be programmed to provide a timing pulse at a predefined interval. This is accomplished by using assembly language programming instructions to define the interval to the computer and to transfer the defined value from the computer to the timer buffer register.

The defined value for the timer interval is transmitted from the computer to the timer buffer register as a 16-bit number (less than or equal to 65535). The clock decrements this number at the rate of one count per microsecond (two counts per microsecond in a 10-bit converter) and issues a timer pulse when the count reaches zero. In continuous mode, the timer automatically resets itself to the value in the buffer register and begins a new cycle. In single cycle mode, the next cycle must be initiated by an external signal. The timer mode is prewired to user specifications, but may be changed after installation.

The DATA assembler directive may be used to define the timer interval value to the computer. After this value has been defined, it may be loaded into the timer buffer register either directly from memory or via the computer's input/output registers. Thus, one of three statements is used to load the buffer register:

OAR	0YY	Output value from A Register to buffer registers
OBR	0YY	Output value from B Register to buffer registers
OME	0YY	Output value from memory to buffer registers

where YY is the device address of timer buffer register, which may be any octal number from 60 to 67. Note that when the OAR or OBR instruction is used, it must be preceded by the appropriate load instruction (LDA or LDB) to load the computer input/output register.

The status of the timer can be sensed by issuing a SEN 01YY instruction. A true sense response on the ADCM Sense line 1 indicates that the timer has decremented to zero; a false level indicates that it has not. The timer continues operation whether or not the sense line is sampled. A true sense response resets the line to false after completion of the sense instruction.

2.4 PROGRAMMING ADC OPERATION

Data may be transferred from the analog input into the computer in one of three ways:

1. Under total control of a user program. In this mode of operation, the program continuously monitors the ADC to provide correct timing.
2. Under control of a Buffer Interlace Controller (BIC). The BIC implicitly utilizes the computer's interrupt structure to eliminate the need for the program to wait for ready signals from the ADC.
3. Under control of an interrupt service routine which is initiated by the Real Time Clock or an input to a Priority Interrupt Module (PIM). This method makes explicit use of the interrupt structure. This method of programming is difficult and should not be attempted by beginners. The service routine itself uses program control and is similar to method number 1. The difference in this method is in the interaction of the service routines with other sequences of instructions being executed in the computer. This interaction is not unique to the ADC module and, for that reason, is not described in this manual.

All of the computer instructions which are used to program the ADCM are described in this section. Note that all of these instructions are not required in any single mode of operation. In the descriptions of program instructions, the symbol YY is used to designate the two octal digits of the device address wired for the module.

Several options are possible by placing jumper connections both on the ADCM and on the backplane of the slot. These options are mentioned in other sections of this manual. The programming instructions given in this section apply to the wiring combinations which are used most frequently.

These combinations are:

- The timer output pulse is wired to the external start (conversion) of the ADC.

- The timer counter is wired to accept pulses from the clock circuit on the module. Pulses are generated at the rate of one per microsecond. Hence the maximum timer interval is 65,535 microseconds.

Note that, therefore, the external start input is always receiving inputs since the timer is always running. Therefore, this input should be gated out by EXC 03YY if it is not going to be used.

<u>Analog to Digital Conversion</u>

The following program instructions are used to initilize and direct analog-to-digital conversion:

EXC 01YY — Begins analog-to-digital conversion. Input is sampled continuously until conversion begins, at which time the analog value is fixed by a "hold" circuit until conversion is complete.

EXC 02YY — Opens a gate circuit which permits conversion to be initiated by the external start input (normally wired to the timer output pulse). An open gate does not prevent EXC 01YY from also starting the conversion cycle.

EXC 03YY — Closes the gate circuit opened by EXC 02YY. EXC 03YY should be used prior to a data run when it is desired to initiate each conversion by EXC 01YY only. That is, possible false starts are locked out.

SEN 0YY — Indicates data is ready as a result of an analog-to-digital conversion. This data ready line is set false (not ready) when conversion begins and resumes its true condition (ready) when conversion is complete. It remains true until reset by an input instruction. The conversion process requires about 13 to 14 microseconds. Another conversion should not begin until the input circuit has sufficient time to settle on a new value (approximately 6 microseconds).

Data Input

Data may be input to the computer using the following program instructions:

CIA (INA) 0YY
CIB (INB) 0YY
CIAB (INAB) 0YY
IME 0YY, < MEM LOC>

These instructions enter the result of a conversion cycle into (respectively):

A register
B register
A and B registers
Memory location (MEM LOC)

Each of the instructions resets the data ready input (SEN 0YY). Therefore a "dummy" input instruction should be given prior to a data run. The dummy input acquired in this manner may be ignored.

Timer Control

The timer control instructions are as follows:

OAR 0YY	Enters a 16-bit word (0 to 65,535) into the timer register,
OBR 0YY	synchronizes the start of the timed interval, and resets
OME 0YY, < MEM LOC>	the timer ready signal. The timer register represents the

number of clock periods in the interval. Normally, the timer is driven by an internally generated clock cycle of one microsecond.

SEN 01YY — Senses timer ready (interval complete). If found ready, the timer ready signal is reset to "not ready." The timer cycles continuously, setting the ready signal at the end of each cycle.

BIC Data Transfer

The following instruction is used to connect the ADCM to a BIC:

EXC 0YY — Connects the ADCM for BIC transfer. The BIC set-up sequence must be performed prior to connecting the BIC.

2.5 PROGRAMMING EXAMPLES

The following examples illustrate typical program instructions which may be used to direct ADCM operation. The examples assume a 13-bit ADCM with device address 60_8.

Example 1 — High Speed Under Program Control

In this example, each conversion cycle is begun by a computer instruction at the maximum acquisition rate (50 kHz). One hundred data points are acquired and stored in memory beginning at the memory address labelled FIRST. The program runs from the address labelled START. When all data is acquired, the computer halts at the address labelled DONE.

```
        ,ORG      ,0500
*       This Example Uses Program Control Exclusively
*       Data is Acquired at the Maximum Rate = 1 Sample Every 20
*       Microseconds. The Timer on the ADC Module is Used to Time
```

```
*        Conversion Cycle.  Of the Total 20 Microseconds, 13 — 14
*        Microseconds are Required for Conversion and 6 Microseconds
*        Are Required for the Sample and Hold Input to Settle on the
*        Analog Input.
ADC    ,SET     ,0060          Define Device Address for the ADC Module
START,EXC      ,0300+ADC      Close the External Start Gate
       ,LDB     ,COUNT         Use B Register as Counter for # Sample Points
       ,LDX     ,FIRST         Use X Register to Point to Data Buffer
       ,CIA     ,ADC           Clear Data Ready Line with Dummy Input
       ,LDA     ,TIME
       ,OAR     ,ADC           Load and Synchronize Timer for Sample Rate
LOOP   ,EXC     ,0100+ADC      Start A to D Conversion Cycle
       ,NOP     ,              Need Two NOP's in Loop to Permit Operation
       ,NOP     ,              Of System Interrupts (Like BIC and PF/R)
       ,SEN     ,ADC, TAKE     Go Take Data When Conversion Cycle Complete
       ,JMP     ,LOOP+1        Else Wait
TAKE   ,JBZ     ,DONE          All Data Taken When B REG = 0
       ,CIA     ,ADC           Take Digital Value From Conversion Process
       ,STA     ,0, 1          Store in Memory (Data Buffer)
       ,IXR     ,              Point to Next Location in Buffer
       ,DBR     ,              Count the Sample Point Taken
CHECK, SEN     ,0100+ADC, LOOP   Wait for Timer Interval Complete
       ,NOP     ,              NOP's Make This an Interruptible Loop
       ,NOP     ,
       ,JMP     ,CHECK         Wait in Check Loop Until Interval Up
DONE   ,HLT     ,0             Finished
COUNT, DATA    ,100           #Sample Point in this Data Run
FIRST  ,DATA    ,BUFF          Beginning Address of Data Buffer in Memory
TIME   ,DATA    ,20            20 Microseconds = Min Conversion Cycle
BUFF   ,BSS     ,100           Reserve 100 Locations for Data (Data Buffer)
       ,END     ,
```

Example 2 - Data Acquired Via BIC Transfer

In this example, the BIC is used to acquire data. Note the following points:

1. The first data point is acquired through a programmed start (EXC 0100 + ADC). All other conversion cycles are started by the timer. This command could be omitted; in which case, the first conversion cycle would not take place until one timer interval was completed.

2. A BIC can be wired to multiple devices but may be used by only one device at a time. Therefore, it is necessary to check for BIC busy before setting up for this operation. Normally, after connecting a device to a BIC, the program does not simply wait for the BIC to complete its job; it usually executes some other sequence of instructions.

```
        ,ORG    ,01000
*       This Example Shows Data Transfer Under BIC Control
ADC     ,SET    ,060          Define Device Address for ADC Module
BIC     ,SET    ,020          Define Device Address for BIC
*       Close External Start Gate to Prevent Inadvertant Input
        ,EXC    ,0300+ADC     Close Gate
BRDY    ,SEN    ,BIC, GO      Go If BIC Not Busy With Some Other Device
        ,NOP    ,             Provide Interruptible Loop for Wait
        ,NOP    ,
        ,JMP    ,BRDY         Check BIC Again
GO      ,EXC    ,BIC + 1      Prepare BIC to Receive Instructions
        ,LDA    ,FIRST        Get First Location of Data Buffer
        ,LDB    ,LAST         Get Last Address of Data Buffer
        ,OAR    ,BIC          Output First to BIC
```

```
       ,OBR    ,BIC + 1         Output Last to BIC
       ,CIA    ,ADC             Reset Data Ready Input From ADC
       ,LDA    ,TIME            Get Timer Interval
       ,OAR    ,ADC             Reset Timer to Known Interval
       ,EXC    ,0200 + ADC      Open Ext Start Gate to Let Timer Pulses In
       ,EXC    ,BIC             Enable the BIC - But Don't Go Yet
       ,EXC    ,ADC             Connect ADC to BIC - Begin Transfer
       ,OAR    ,ADC             Start and Synchronize Timer for Real
       ,EXC    ,0100 + ADC      Start First Conversion Cycle
WAIT   ,SEN    ,BIC + 1, ERROR  Error if Can't Complete all Data Transfers
       ,SEN    ,BIC, DONE       Finished with all Data Transfers
       ,NOP    ,                Interruptible Loop
       ,NOP    ,
       ,JMP    ,WAIT            Instead of Wait, Could Do Other Things
ERROR, CIA     ,BIC             Get Address for Last Successful Transfer
       ,HLT    ,07              A Reg Should be Less than Contents of Last
DONE   ,TZA    ,                Normal Finish With A = 0
       ,HLT    ,0
FIRST  ,DATA   ,BUFF            First Word of Data Buffer
LAST   ,DATA   ,BEND            Last Word of Data Buffer
TIME   ,DATA   ,1000            Min = 20 Microsecs; Max = 65,535 Microsecs
BUFF   ,BSS    ,100             Reserve 100 Words for Data Buffer
BEND   ,BES    ,0               Label Last Word of Buffer
       ,END    ,
```

2.6 ADC/MULTIPLEXER SOFTWARE DRIVERS

The software support modules supplied with the ADCM provide a means of convenient access to an ADCM/Multiplexer combination without detailed user knowledge of hardware. The modules may be used by themselves or embedded in an operating system.

Two types of software modules are supplied to accommodate both programmed data transfers and direct memory access data transfers. These two types of modules may be coresident in memory or they may be used individually. The programmed data transfer module provides a higher degree of flexibility in the order of channel selection, timing, and data synchronization with an external source transfer mode. This flexibility is paid for in software overhead which limits the maximum data acquisition rate to 10 kHz (20 kHz for 10-bit version) using a 620/i or 620/L. Proportionally higher rates can be achieved using the faster 620/f or V-73. The direct memory transfer technique (using a BIC) will provide data rates up to 50 kHz (100 kHz for 10-bit version), with other processing proceeding concurrently. This mode is limited to sequential channel or single channel input.

This section describes these software modules and presents programming examples of their use. In the descriptions and examples, the following device address assignments are assumed:

Address (Octal)	Device
060	ADCM
040	Multiplexer
020-021	BIC, No. 1
022-023	BIC, No. 2
024-025	BIC, No. 3
026-027	BIC, No. 4

Programmed Data Transfer

The programmed ADC data transfer module (PADC) permits the user to specify:

- Channel selection technique (random or sequential).
- Last channel to be read for sequential mode or channel list specification for random mode.

- Quantity of input data and location at which the data is to be stored in the computer memory.
- Time interval between the sampling of individual channels within the scan.
- Time interval between successive starts of the channel-scanning process.
- An error address to which control is to pass if an error is detected in the module arguments.

The PADC module is called with the following assembly language sequence:

```
CALL PADC, MODE, CHANNELS, TIME, TIME PERIODS, NUM,
DESTINATION, EXIT
```

All entries in the calling sequence are either direct addresses or indirect addresses which point to the actual arguments. Multiple levels of indirect addresses are permitted. The arguments are defined as follows:

MODE — An integer value which specifies the technique for channel selection. A value of zero specifies sequential channel selection starting at channel 1 and ending at the value of CHANNELS for each scan. A value greater than zero specifies random channel selection and the number of entries in the CHANNELS array. For each scan in a random selection, the CHANNELS vector determines the order of selection.

CHANNELS — An integer vector; the values in the CHANNELS array determine the channel and order of selection for each scan. The size of this vector is determined by the value of MODE. When MODE = 0 (sequential channel selection), the size is one element which represents the number of the last channel to be collected during each scan. When MODE is greater than zero, its value represents the size of the CHANNELS vector.

TIME — An integer value which specifies the number of microseconds between each data sample in the scan. Therefore, TIME represents the elapsed time between the start of each frame. If TIME is zero, each sampling will be synchronized to an external signal. The user should allow 50 microseconds (25 microseconds for 10-bit version) per channel collected within a scan to maintain proper time sychronization. For example, if seven channels are to be collected during each scan, the value of TIME should be at least 350 microseconds (175 microseconds for the 10-bit version).

TIME PERIODS — An integer value which specifies the number of time periods of TIME microseconds to elapse between each start of the channel-scanning process. That is, the scan interval, or time between scan starts, is (TIME x TIME PERIODS) microseconds in length.

NUM -- An integer value which specifies the total number of data values to be collected and transferred to the DESTINATION vector.

DESTINATION — An integer array which is to receive the incoming data. At least NUM words must be allocated to accommodate the data. As each data value is input, it is placed in the next sequential location of DESTINATION.

EXIT — A program label to which control is to be transferred when illegal arguments are detected. The following conditions cause an error exit:

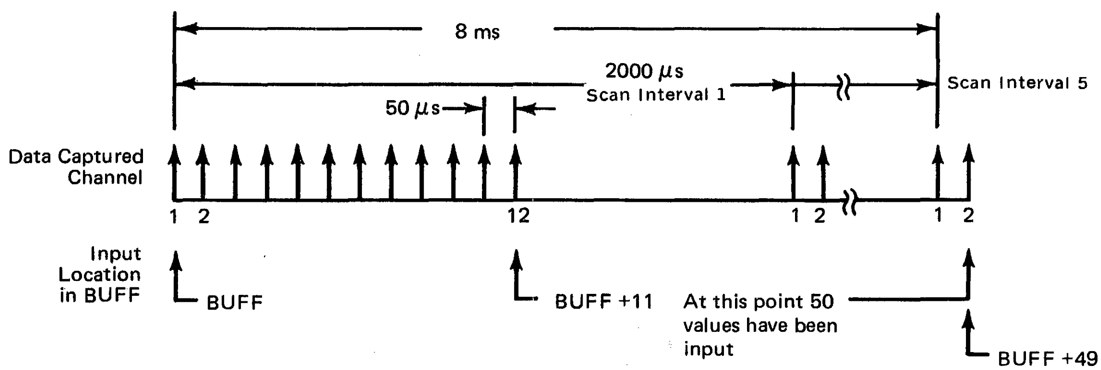
MODE less than 0.
CHANNELS not between 1 and 256, inclusive.
TIME PERIODS less than MODE for random mode.
TIME PERIODS less than CHANNELS for sequential mode.
TIME less than 0.
NUM less than or equal to 0.

Figures 2-1 and 2-2 show examples of the use of the PADC module to perform both sequential and random channel collection.

Problem Statement:

Acquire 50 data values from channels 1 through 12, with an individual channel data rate of 500 Hz. Scan interval is 2000 microseconds.

Timing Diagram:



Programmed Solution:

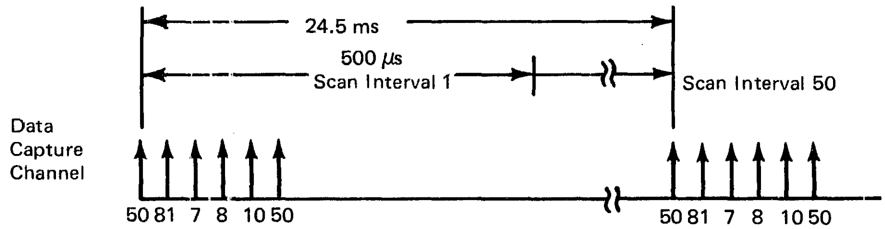
```
        ...
        CALL PADC, S, CADR, T, TP, NR, BUFF, ERR
        ...
ERR     HLT                 HLT COMPUTER IF ARG ER
        ...
S       DATA 0              SELECT SEQUENTIAL MODE
CADR    DATA 12             LAST CHANNEL ADDRESS
T       DATA 50             50 MICROSECONDS/CHANNEL
TP      DATA 40             SCAN INTERVAL IS 40 TIME PERIODS
NR      DATA 50             ACQUIRE 50 VALUES
BUFF    BSS 50              RESERVE 50 WORDS OF STORAGE
```

Figure 2-1. Programmed Data Transfer-Sequential Selection

Problem Statement:

Acquire 300 data values from channels 10, 7, 8, 50, and 81. The individual channel data rate should be 2 kHz for channels 10, 7, 8, and 81, and 4 kHz for channel 50. The order of channel selection is 50, 81, 7, 8, and 10 for each scan.

Timing Diagram:



Programmed Solution:

```
                 . . .
                 CALL    PADC,R,ADRS,T,TP,N, (BADR)*, BADARG
                 . . .
BADARG           CALL    ERPT        PRINT ERROR MESSAGE
                 . . .
R                DATA    6           LENGTH OF 'ADRS'
*    CHANNEL SELECT VECTOR
ADRS             DATA    50
                 DATA    81
                 DATA    7
                 DATA    8
                 DATA    10
                 DATA    50          REPEAT FOR TWICE DATA RATE
*
T                DATA    500         50 MICROSECONDS PER READ
TP               DATA    10          10 TIME PERIODS PER INTERVAL
N                DATA    300         300 INPUT VALUES
BADR             DATA    BUFFER POINTER TO BUFFER
                 . . .
BUFFER           BSS     300         RESERVE 300 WORDS
```

Figure 2-2. Programmed Data Transfer — Random Selection

Direct Memory Data Transfer

Two direct memory transfer modules (DADC and SADC) utilize the BIC option and permit the user to acquire data from the ADCM/Multiplexer at a maximum rate (50 kHz for 13-bit or 100 kHz for 10-bit conversion), while the CPU can be working on an entirely different process. To do this, the user calls DADC to initiate the data transfer. Control will be returned immediately after initiation so that the user may proceed with independent processing. At the user's convenience, SADC may be called to determine whether or not the data transfer is complete.

DADC Module

The DADC module is called with following assembly language sequence:

CALL DADC, BICNR, MODE, CHAN, TIME, NUM, DEST, EXIT

All entries in the calling sequence are either direct or indirect addresses of the actual arguments. Multiple levels of indirect addresses are permitted. The arguments are defined as follows:

BICNR — An integer value which specifies the BIC that is to be used for the data transfer. The range of BICNR is from one to four corresponding to BICs using device addresses $20\text{-}21_8$ to $26\text{-}27_8$.

MODE — An integer value which specifies whether sequential channels are to be scanned (MODE = 0) or data from an individual channel is to be acquired (MODE $\neq$ 0).

CHAN — An integer value which determines the channels to be acquired. If MODE = 0 (sequential scan), CHAN represents the number of the last channel to be collected. If MODE $\neq$ 0 (single channel input), CHAN represents the number of the channel to be acquired.

TIME — An integer value which specifies the time in microseconds between each data input. This value must be greater than or equal to 20 to prevent invalid conversions.

NUM - An integer value which specifies the total number of data values to be collected and transferred to the DEST vector.

DEST- An integer array which is to receive the incoming data. At least NUM words must be allocated to accommodate the data. As each data value is input, it is placed in the next sequential location of DEST.

EXIT - A program label to which control is to be transferred when illegal arguments are detected. The following conditions cause an error exit:

BICNR not between 1 and 4, inclusive.

CHAN not between 1 and 256, inclusive.

TIME less than 20.

NUM less than or equal to 0.

Figures 2-3 and 2-4 show examples of the use of DADC, in conjunction with SADC, to perform direct memory data transfers.

SADC Module

The SADC module checks the status of a previously initiated direct memory data transfer. SADC is called with the following assembly language sequence:

```
CALL SADC, STATUS
```

The single entry in the calling sequence can be either a direct address or an indirect address which points to the actual argument. The argument is defined as follows:

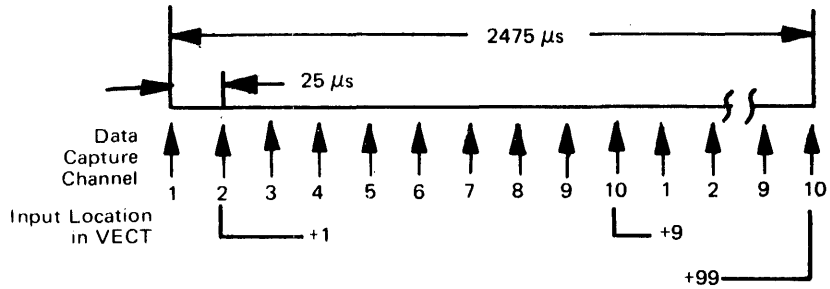
STATUS - This argument receives a value of 0, 1, or 2 to indicate the status of the transfer operation:

Value	Meaning
0	Operation not complete
1	Operation complete; no errors
2	Operation aborted

Problem Statement:

Acquire 100 data values using the sequential scan mode starting from channel 1 through channel 10. The time between each data input should be 25 microseconds. The BIC with device address 20_8 - 21_8 will be used for the data transfer.

Timing Diagram:



Programmed Solution:

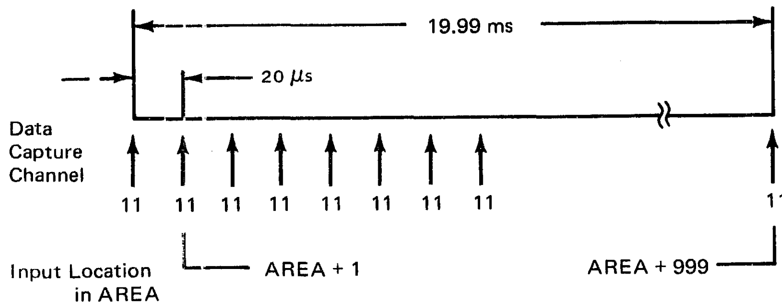
```
*INITIATE DATA TRANSFER
     CALL   DADC = 1, =0, =10, =25, =100, VECT, ERR
     . . .
     . . .      Concurrent processing
     . . .

*WAIT FOR COMPLETION
WAIT    CALL SADC, STATE          CHECK STATUS
        LDA STATE                 TEST STATUS WORD
        JAZ WAIT                  IF 0 CONTINUE WAITING
        . . .
        . . .
STATE   DATA**                    STATUS WORD
ERR     HLT                       HALT ON ERROR
VECT    BSS     100               RESERVE 100 WORDS
```

Figure 2-3. Direct Memory Transfer — Sequential Scan

Problem Statement:

Acquire 1000 points at the fastest possible rate from channel 11. The BIC with device address 24_8-25_8 should be used to accomplish the direct memory transfer.

Timing Diagram:



Programmed Solution:

```
* INITIATE DATA TRANSFER
                CALL DADC, = 3, M, = 11, T, = 1000, (BUFF)*, GOOF
                ...
* TEST FOR TRANSFER COMPLETION
NO              CALL SADC, FLAG
                LDA  FLAG
                JAZ  NO              WAIT FOR COMPLETION
                ...
GOOF            HLT                  ERROR HALT
M               DATA 5               SELECT ONE CHANNEL INPUT
T               DATA 20              MIN TIME = 20 MICROSECONDS
FLAG            DATA**               STATE FLAG
BUFF            DATA (AREA)
AREA            BSS 1000             RESERVE 1000 WORDS
```

Figure 2-4. Direct Memory Transfer - Single Channel

2.7 TEST PROGRAMS

A set of test programs (binary paper tape, Part No. 03-994092) is provided for ADCM checkout. The set consists of six programs which may be selected through the Test Executive Program. The programs, numbered 0 through 6, are as follows:

Test No.	Description
0	Returns control to the Test Executive Program after performing other tests.
1	Reads one channel in random mode.
2	Reads N channels in sequential mode.
3	Reads N channels in random mode under timer control.
4	Reads one channel in random mode under BIC control.
5	Reads N channels in random mode under BIC control.
6	Tests timer.

These programs may be selected in any order and may be run as often as desired with different parameters. The device addresses of the modules need be entered only once but may be changed by re-entering the supervisor from the Test Executive Program.

Note that these tests accommodate a full complement of hardware consisting of the following modules: ADCM, Multiplexer, and BIC. The following table indicates which tests should be run with various hardware configurations.

	Test Number					
	1	2	3	4	5	6
ADCM, MUX, BIC	x	x	x	x	x	x
ADCM, MUX	x	x	x			x
ADCM, BIC	x			x		x
ADCM	x					x

The minimum computer configuration on which the tests may be run is a 620 or V-73 series computer with 4K of memory and a teletype or other terminal on device code 01.

An ADCM/MUX test shoe is required for running these tests. It can be purchased from Varian (Part No. 03-950399).

Supervisor Program

A simple supervisor or test program selector is provided as part of the test package to allow the user to select individual tests and return control to the Test Executive Program. The Test Executive Program is a standard Varian software option which must be loaded and run prior to initiation of the ADCM test package. Instructions for operating this program are given in the Test Program Manual. The ADCM test package is loaded through the Test Executive.

When the Test Executive Program is running, the "L." command may be used to load the test package and transfer control to its supervisor. If the test package is already loaded, the "G500." command may be used to transfer control to the supervisor.

When the supervisor is activated, it responds by issuing a carriage return/line feed and by starting to print a series of prompting messages. The user must enter a valid response to each message as it is printed. An invalid response causes the message to be repeated. The first message is:

ADC, MUX AND TIMER TEST SUPERVISOR
ENTER ADC-TIMER DEVICE ADDRESS?

The user must enter the assigned octal number between 060 and 067 followed by a period. The supervisor will then print:

ENTER MUX DEVICE ADDRESS?

The user must enter the assigned octal number between 040 and 077 followed by a period. The supervisor will then print:

ENTER BIC DEVICE ADDRESS?

The user must enter any of the following assigned octal numbers: 020, 022, 024, or 026 followed by a period.

The three device addresses entered at this time will be used throughout the six tests, where applicable. To change address selections, the supervisor must be reactivated from the Test Executive Program or run from location 500. After the device addresses have been entered, the supervisor will print:

ENTER TEST NO.?

The user should enter any number between 0 and 6 followed by a period. The supervisor will then transfer control to the selected test program, which will request additional parameters and perform its specified functions.

Sense Switches

Throughout the operation of all ADCM tests, the sense switches may be used to perform special functions. The normal mode of operation is to reset all sense switches, but the following functions may be performed by setting the sense switches:

SS1	Sense switch 1 suppresses teletype printouts of test results and error messages. This function is useful to speed up the continuous execution of a test so that an oscilloscope may be used to monitor signals.
SS2	Sense switch 2 causes a test to repeat indefinitely without user intervention.

SS3 — Sense switch 3 terminates the execution of a test and returns control to the supervisor. If sense switch 3 is set when the supervisor requests a new test number, the following message will be printed:

RESET SENSE SWITCH 3

A new test may be selected after SS3 is reset.

Test Program Results

The same set of statistics is printed by the test programs for Tests 1, 2, 3, 4, and 5. After accepting the input readings, the test programs calculate and print the following items:

Minimum value in millivolts

Average value in millivolts

Maximum value in millivolts

The following frequency of occurrence readings are also calculated and printed:

Below (average value minus one count)

Average value minus one count

Average value

Average value plus one count

Above (average value plus one count)

In tests 2, 3, and 5, where several multiplexer channels are read, the statistics for odd and even numbered channels are calculated separately since their values are of opposite signs.

Test 1 — Read One Channel in Random Mode

In this test, the ADC is used to read a selected channel under program control in random mode 64 times. When the test program is activated, it will print:

ENTER CHANNEL NO. ?

The user should enter any channel number between 1 and 256 in decimal format followed by a period. Any other response will cause the message to be repeated. If no multiplexer is being used, any channel number may be entered since it will have no effect. In this case, the test signal must be connected directly to the ADC across pins J2-37 and J2-38.

The program acquires 64 input readings before printing the test statistics. Note that in all data printouts, the ADC quantizes the signal input at 2.4 millivolts per bit, but the printout omits references to fractional data. (In the 10-bit converter, ADC resolution is 19.5 millivolts per bit.)

Test 2 — Read N Channels in Sequential Mode

In this test, the ADC is used to read N sequential multiplexer channels. One word is read on each channel under program control and stored in a core buffer. The test statistics are printed on the teletype along with each channel reading. Using the test shoe, all odd numbered channels are wired together and all even numbered channels are wired together. Therefore, all even channels will have one reading and all odd numbered will have another. When the test program is activated, it will print:

ENTER NO. OF CHANNELS?

The user should enter any decimal number between 1 and 256 followed by a period to indicate the highest numbered channel. Any other response will cause the message to be repeated.

The program then reads the selected channels from channel 1 to the selected upper limit sequentially. The test results are printed first for the odd numbered channels and then for the even numbered channels. The value of each channel input is then printed eight readings per line. The first number of each line is the initial channel number on that line of print.

Test 3 — Read N Channels in Random Mode Under Timer Control

This test exercises the ability of the multiplexer to receive random channel addresses from the program and for the ADC to read the specified channels under program control. The timer is used to start an ADC conversion every 500 microseconds. A table of multiplexer channel addresses is used to direct the multiplexer selection. Each channel on a multiplexer card is read and stored into another core buffer for statistical reduction. The test will accommodate up to 16 cards having 16 channels each.

The test results are found for the odd and even numbered channels and are printed on the teletype. All readings that are not within plus or minus one count of the averages will be printed on the teletype.

To perform this test, a test shoe must be installed on all of the multiplexer cards being tested so that test voltages will be provided to all channels. The test shoe must be installed on J1 of the ADC to cause external ADC starts with the timer.

When the test program is activated, it will print:

ENTER NO. OF MUX CARDS?

The user should enter any decimal number between 1 and 16 followed by a period. Any other response will cause the message to be repeated. The program will read the data into the core buffer and list the odd statistics and then the even statistics. Then all channels which deviate by more than plus or minus one count from the average will be listed. The channels are listed in the order in which they are acquired. The odd numbered channels are read in ascending order interlaced with the even channels in descending order for each card one at a time. Card one will have the following channel selection sequence: 1, 16, 3, 14, 5, 12, 7, 10, 9, 8, 11, 6, 13, 4, 15, and 2.

Test 4 — Read One Channel in Random Mode Under BIC Control

This test program reads a specified channel on the multiplexer 64 times under BIC control. The 64 words are automatically transferred to a memory buffer via the BIC at the maximum ADC data conversion rate of 50 kHz (100 kHz for the 10-bit converter). The timer is used to initiate the acquisition of each word. The test results are printed at the conclusion of data acquisition.

Note that to cause external ADC starts with the timer, the special test shoe must be plugged into the ADC connecting J1-37 to J1-39 and J1-27 to J1-41.

When the program is activated, it will print:

ENTER CHANNEL NO.?

The user should enter any decimal number between 1 and 256 followed by a period. Any other response will cause the message to be repeated. The program then reads the data, computes the results, and prints them on the teletype.

Test 5 — Read N Channels Random Mode Under BIC Control

This test exercises the ability of the multiplexer to receive random channel addresses under BIC control. Each time the ADC is started, the BIC transfers a new channel address to the multiplexer from a table of channel addresses in core. The channel is read by the ADC under program control and stored into a table in memory. The test program will accommodate up to 16 multiplexer cards having 16 channels each.

Note that a test shoe must be installed on all of the multiplexer cards being tested so that test voltages will be provided to all channels.

When the test program is activated, it will print:

ENTER NO. OF MUX CARDS?

The user should enter any decimal number between 1 and 16 followed by a period. Any other response will cause the message to be repeated. The program will read the data into the core buffer and list the odd statistics followed by the even statistics. Then all channels which deviate by more than plus or minus one count from the average will be listed. The channels are listed in the order in which they are acquired. The odd channels are read in ascending order interlaced with even channels in descending order for each card one at a time. Card one will have the following channel selection sequence: 1, 16, 3, 14, 5, 12, 7, 10, 9, 8, 11, 6, 13, 4, 15, and 2.

Test 6 — Timer Test

This test program checks the ADCM programmable timer. The test program sets the timer to time out every 50 milliseconds. The program counts 100 of these intervals and indicates the end of the cycle by ringing the teletype bell and printing an asterisk, "*". Six of these 5-second intervals are exercised. The last teletype bell should occur exactly 30 seconds after the test is started.

Note that the timer test runs twice as fast with the 10-bit ACDM. The teletype bell will ring every 2.5 seconds and the last bell should occur exactly 15 seconds after the test is started.

In order for the timer to run, it is necessary to install the special test shoe which connects ADC J1-27 to J1-41. This has the effect of connecting the 1 MHz oscillator to the counter. If an external time base is used, it should be connected at J1-41.

3. THEORY OF OPERATION

3.1 INTRODUCTION

The theory of operation presented in this section and in Section 4 assumes an ADCM with a 13-bit converter. The basic principles of operation are the same for the 10-bit version even though slight hardware differences exist between the two modules.

3.2 GENERAL THEORY

The amplitude of the analog input signal is represented to the computer in 16-bit binary two's complement by a 12-bit binary number and an extended sign bit. The value of the number is determined by bits 0 through 11 and the sign by bits 12 through 15. A logical 1 in bit positions 12 through 15 indicates that the number is negative, and a logical 0 indicates that the number is positive or zero.

NOTE

In this manual, logical 1 and logical 0 will each have two definitions. Their use is determined by where the signals appear; all logic signals that leave or enter the ADC are ground-true and all signals internal to the module are +5 Vdc-true.

	E-bus (nominal)	ADCM (nominal)
Logical 1	0 Vdc	+5 Vdc
Logical 0	+3 Vdc	0 Vdc

The binary value of each bit position is determined by the successive approximation technique. For each approximation, a comparison is made between a current proportional to the analog input voltage and the current generated in a ladder network. The successive approximation is carried out in 13 stages.

At State 1, the polarity of the input current sets the sign bit. At each of the succeeding stages, a new comparison is made that determines the binary level of the corresponding bit (logical 1 or logical 0). The level is determined by removing an amount of positive reference current that is proportional to the weighted value of the bit. If the polarity of the remaining current is still positive, the bit is set to 1; if the polarity is negative, the bit is set to 0 and the current that was removed is restored. After the thirteenth comparison is made, all 13 bits are set into the data buffer register, where they are stored until the next conversion is complete.

The following paragraphs provide a detailed discussion of the analog-to-digital conversion.

3.3 DETAILED THEORY

Figure 3-1 illustrates the principal elements responsible for carrying out the analog-to-digital conversion.

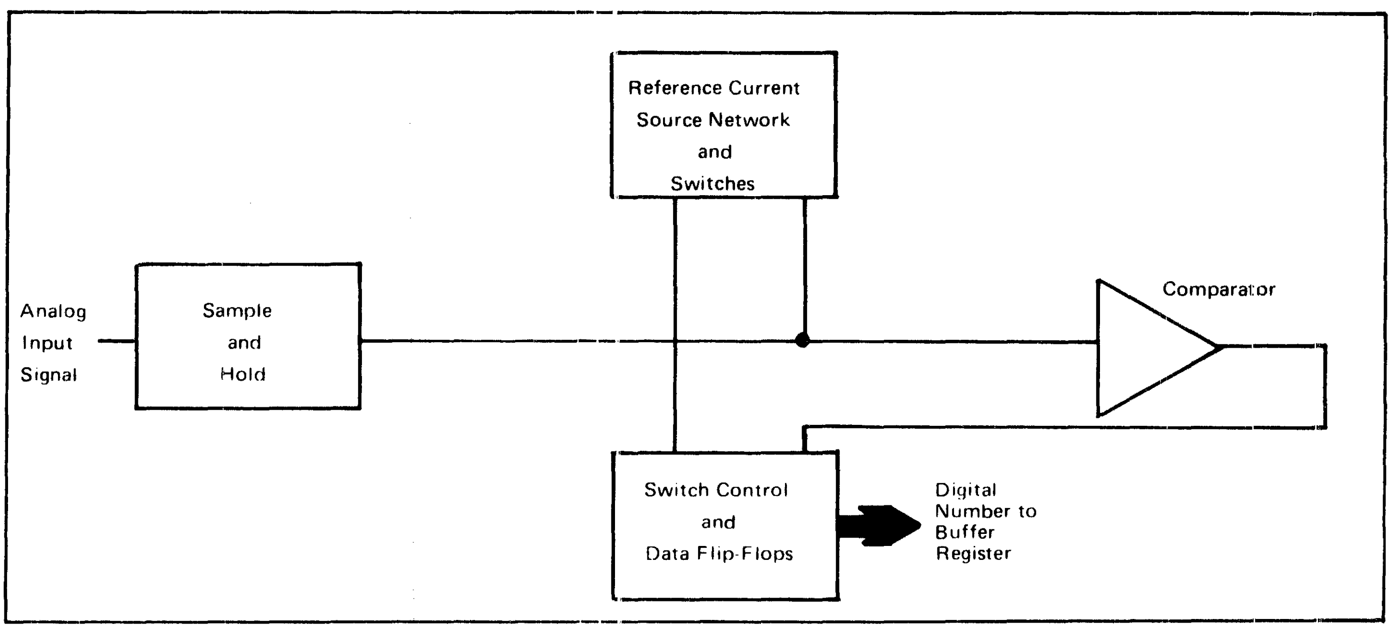


Figure 3-1. ADC Block Diagram

Reference Current and Switches

The reference current is provided to the summing junction by two stable reference voltage sources: -10 Vdc and +10 Vdc.

The negative reference current is provided through a partially variable resistor that is calibrated to match the positive reference current of bits positions 0 through 11. The negative reference current remains constant through all 13 stages of the conversion. The positive reference current is provided through 13 resistors, one for each bit position of the digital number. The resistor values are related in binary fashion, with the smallest resistor at bit position 12 (sign bit) and the largest at bit position 0 (least significant bit).

The current from the negative reference voltage offsets the summing junction by an equivalent of −9.9976 volts. The parallel resistance of the resistors for bit positions 0 through 11 is equivalent to the resistance of the negative reference resistor; thus, the resistor network for bits 0 through 11 will null the negative offset when all the switches controlling current through these resistors are closed.

During data conversion, current is provided to the summing junction by three sources: −10 Vdc reference, +10 Vdc reference, and the analog input voltage of unknown amplitude and polarity. The positive reference current is increased or decreased in an attempt to null the effect of the three voltages on the summing junction. If the analog input voltage is plus full scale (+9.9976 volts), it will exactly null the negative reference. All switches will be open by the end of the conversion, removing all positive reference current from the summing junction. If the analog input voltage is minus full scale (−10 volts), all positive reference current is needed to null the combined effect of the input voltage and the negative reference. All switches will be closed by the end of the conversion, adding full positive reference current to the summing junction.

Table 3-1 compares the bit values of ADCM binary output for key analog input values; the corresponding states of each bit switch and the octal and decimal values of the digital output are also shown.

The current through each bit position resistor is controlled by a current steering switch. Figure 3-2 illustrates a current steering switch for a single bit position.

When the flip-flop controlling the switch is set, diode CR1 is back biased and current through resistor R1 flows to the summing junction. If the flip-flop is reset, CR1 is forward biased and the reference current is steered through CR1 to the −15 Vdc sink.

Current provided by the analog input voltage is algebraically summed with the current provided by the positive and negative precision references.

This sum determines the polarity of the output of an inverting amplifier and comparator that are connected in series. (See Figure 3-2.) If the algebraic sum is positive, the output of the comparator will be a logical 1 and, if the sum is negative,

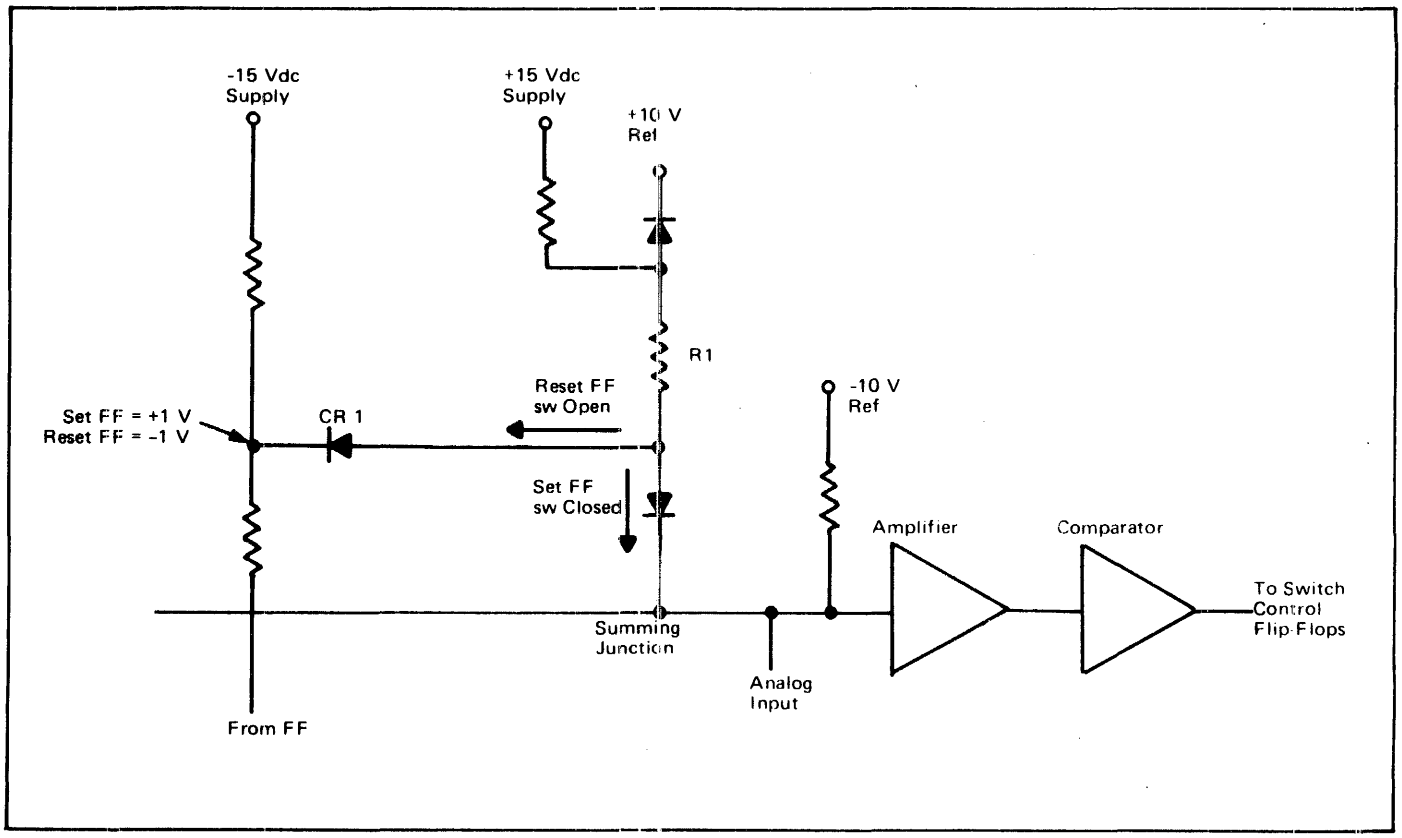


Figure 3-2. Current Steering Switch

the output will be a logical 0. The comparator output is buffered and applied to the D input of the set of flip-flops that control the current steering switches. The following paragraphs describe the logic that controls the current steering switches through a data conversion sequence.

Switch Control

A set of 13 D-type flip-flops and a 12-stage shift register form the heart of the logic that controls an analog-to-digital conversion. All the flip-flops, except flip-flop 2_0, open and close the current steering swtiches in the positive reference current source network. They also set logical 1's or 0's into the data buffer register. The flip-flops are controlled, in turn, by the shift register.

Between conversion operations, the flip-flops are prepared for the start of a new conversion. Relative high levels on Clk, Hold, Store and Sample cause flip-flops 2^1 through 2^{11} to be set and flip-flop 2^{12} to be reset. Flip-flop 2^0 is part of the data buffer register.

The Q output of those flip-flops that are set (high) close the current steering switches that they control. The Q output of a reset flip-flop (low) opens its switch. Consequently, before the start of a conversion, switch 12 (sign bit) is open and switches 0 through 11 are closed.

When the Start ADC logic is initiated (refer to Section 4), the signal Hold goes low and sets a logical 0 into position 11 of the shift register and logical 1's into positions 0 through 10. Busy and Clock go high when Hold goes low, with the trailing edge of Clock, the 0 set into position 11 of the shift register is clocked to the shift register's output and resets flip-flop 2^{11}. The Q output of flip-flop 2^{11} clocks flip-flop 2^{12}.

At this time, flip-flop 2^{12} is set or reset according to the logic level present at its D input. This input will be high if the analog input voltage has negative polarity and will be low if the analog input voltage has positive polarity.

If flip-flop 2^{12} is set, the sign bit switch is closed and a logical 0 will be set into bit position 12 (sign bit) of the data buffer register at the end of the conversion. If it is reset, the sign bit switch remains open and a logical 1 is set into position 12 of the buffer register at the end of the conversion.

When flip-flop 2^{11} resets, it also opens the switch in bit position 11. This removes the positive reference current contributed by that bit position. This initiates the second attempt at nulling the summing junction.

The trailing edge of the next clock pulse moves the 0 in the shift register to position 10, resetting flip-flop 2^{10}. The Q output of flip-flop 2^{10} clocks flip-flop 2^{11}. Flip-flop 2^{11} sets or resets according to the logic level present at its D input. If flip-flop 2^{11} sets, switch 11 closes and a logical 0 is set into position 11 of the data buffer register at the end of the conversion. If flip-flop 2^{11} resets, switch 11 remains open and a logical 1 is set into position 11 of the data buffer register at the end of the conversion. This sequence is repeated with the trailing edge of each clock pulse until flip-flop 2^{1} is reset.

The trailing edge of the last (twelfth) clock pulse in the conversion opens switch 0 directly (via two inverters) for the final approximation. Flip-flop 2^{0} is clocked by the transistion of the Start ADC logic from the conversion (Busy) state to the Sample state. This transition occurs when the last clock pulse generates the signal Store. When flip-flop 2^{0} is clocked, it sets or resets in the same manner as the other flip-flops in the sequence. Flip-flop 2^{0} is the buffer register for bit position 0 of the digital number.

Sample and Hold

The amplitude of the analog input voltage is continuously monitored between conversions by the sample circuit shown in sheet 1 of Appendix D. This circuit is capable of tracking a waveform of 20 volts peak-to-peak.

During the Sample period, the signals Sample and Hold, which originate in the Start ADC logic, are both high and test point 6 is low. This switches off transistors Q1 and Q2. With Q2 off, the field-effect transistor switches Q3 and Q4, which control the analog input to the storage capacitors, are conducting. As long as they are conducting, the voltage at the storage capacitors follows the input voltage.

When the Start ADC logic is set, Hold goes low and test point 6 goes high (sample goes low on the leading edge of the next clock pulse). This turns Q1 and Q2 on, switching Q3 and Q4 off. The voltage present at the storage capacitors at the instant Q3 and Q4 stop conducting is held during the Hold period.

During the Hold period, the stored potential in the capacitors provides the summing junction with a steady current that represents the input voltage. The period from the initiation of the conversion (Start ADC signal) to the time Q3 and Q4 are fully open is less than 100 nanoseconds. This period is called the aperture time. When the conversion cycle is complete, Q3 and Q4 close again. The time it takes the voltage level at the storage capacitors to reach the new analog input voltage level is called the recovery or acquisition time. The maximum recovery time for the Sample and Hold Circuit is 7 μs. This time would be required if the potential at the storage capacitor were at either plus or minus full scale when Q3 and Q4 closed and the input voltage were at the other end of the scale.

Power Supplies and Reference Voltages

Four regulated power supplies, +5 Vdc, +15 Vdc, —15 Vdc, and −22 Vdc are provided by circuits located on a power supply module.

The +10 Vdc and −10 Vdc precision reference voltages are provided by voltage regulators contained on the ADCM.

Output of the negative reference, as measured at test point 3, is within the range +8.5 Vdc to +9.5 Vdc. This output is stable to within $\pm$0.1 mV. Coarse and fine adjustments set the amount of constant offset current provided to the summing junction by the negative reference. With all the switches open, this offset current is provided entirely by the output amplifier feedback loop, and the amplifier output voltage is at plus full scale.

Output of the plus reference source is +10 Vdc $\pm$ 0.1 mV. The feedback resistance of this circuit may be calibrated with both coarse and fine adjustment.

				COMPUTER INPUT AND SWITCH SETTINGS												
Scale Values				EB12 EB15	EB 11	EB 10	EB 09	EB 08	EB 07	EB 06	EB 05	EB 04	EB 03	EB 02	EB 01	EB 00
RANGE	DECIMAL	OCTAL	V_{in}	SW 12	SW 11	SW 10	SW 09	SW 08	SW 07	SW 06	SW 05	SW 04	SW 03	SW 02	SW 01	SW 00
+ Full Scale	+4095	007777	+ 9.9976	0	1	1	1	1	1	1	1	1	1	1	1	1
				0	0	0	0	0	0	0	0	0	0	0	0	0
+ Half Scale	+2048	004000	+ 5.0000	0	1	0	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	1	1	1	1	1	1
+ 1 LSB	+1	000001	+ 0.0024	0	0	0	0	0	0	0	0	0	0	0	0	1
				0	1	1	1	1	1	1	1	1	1	1	1	0
0	0	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	1	1	1	1	1
- 1 LSB	-1	177777	- 0.0024	1	1	1	1	1	1	1	1	1	1	1	1	1
				1	0	0	0	0	0	0	0	0	0	0	0	0
- Half Scale	-2048	174000	- 5.0000	1	1	0	0	0	0	0	0	0	0	0	0	0
				1	0	1	1	1	1	1	1	1	1	1	1	1
- Full Scale +1	-4095	170001	- 9.9976	1	0	0	0	0	0	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	1	1	1	1	1	0
- Full Scale	-4096	170000	-10.000	1	0	0	0	0	0	0	0	0	0	0	0	0
				1	1	1	1	1	1	1	1	1	1	1	1	1

Table 3-1. ADC Output Scale

4. I/O INTERFACE THEORY OF OPERATION

4.1 PROGRAM CONTROLLED DATA TRANSFER

Program controlled data transfer in operations occur in three stages:

A. Start ADC – An EXC instruction starts the ADC and an analog-to-digital conversion cycle takes place.

B. Data Sense – A Sense instruction tests for the availability of a new data word.

C. Data Transfer In – A data transfer in instruction is executed.

The ADCM logic involved in these stages of a data transfer operation is described in the following paragraphs.

Start ADC

The program instruction EXC 01YY sets the appropriate device address on E-bus lines EB00 through EB05, places function code 1 on EB06 through EB08, and places a logical 1 on EB11. The control pulse, FRYX, then strobes the function code into the function decode logic.

The decode logic output $\overline{\text{EXC1}}$ is selected and sets the Hold flip-flop. The low Q output of this flip-flop causes the control switches in the Sample and Hold circuit to be turned off, capturing the instantaneous analog input voltage.

On the next leading edge of a clock pulse, the Sample/Busy flip-flop resets. The high Busy output gates clock pulses into the shift register that sequences the ADC logic through the conversion cycle.

Each succeeding clock pulse causes a bit (logical 1 or logical 0) to be set into the control flip-flop register. The last clock pulse in the conversion sequence generates a Store pulse, indicating that the data word is complete and is being stored.

The Store pulse conditions the Sample/Busy flip-flop to be set with the trailing edge of the clock pulse that generated Store. When this flip-flop sets, the low-to-high transition of Sample clocks the least significant bit into its latch.

Data Sense

The leading edge of Store sets the Data Sense flip-flop. Data Sense conditions the Sense 0 gate in preparation for a Sense 0 instruction from the program.

When the program issues a Sense 0 instruction, the function decode logic selects the line Select 0.

This enables the Sense 0 gate, providing a logical 1 to the SERX line on the I/O bus. The Data Sense flip-flop remains set until a data transfer in operation is completed.

Data Transfer

The program executes a data transfer in operation from an ADCM with one of the assembler data transfer-in instructions (refer to Section 2). The ADCM is selected and a logical 1 on EB13 sets the DTIS (Data Transfer In) flip-flop. DTOS (Output Enable) gates the contents of the data buffer register onto the E-bus lines EB00 through EB15. EB00 through EB11 carry the data bits, with the least significant bit on EB00 and the most significant bit on EB11. The sign bit is gated onto EB12 through EB15 via four line drivers. This is done to accommodate the 13-bit data word format to the 16-bit format required by the computer.

Output Enable resets the Data Sense flip-flop in preparation for a new conversion sequence.

4.2 BIC CONTROLLED DATA TRANSFER

BIC-controlled data transfer in operations may be started by the program, the programmable timer, or EXT Start.

If the program is used to start the ADC, the EXC 01YY instructions will occur at intervals determined by program delays or from sensing the timer. If the output of the timer is used, J1-37 must be connected to J1-39, or optionally, jumper 5 must be installed.

For timer starts or external starts, the data transfer operation must be preceded by an EXC 02YY instruction to set the Program flip-flop. This places the clock input to the Hold flip-flop under the influence of either the timer output or Ext Start.

An EXC 02YY instruction is followed by an EXC 0YY instruction. This sets the BIC Enable flip-flop, preparing the ADCM's BIC interface logic to be connected to the BIC. The ADCM is connected to the BIC when DCEX from the BIC sets the Connected flip-flop. When the BIC receives the output of the Connected flip-flop, CDCX, indicating that the ADCM has been connected, it resets DCEX. The Connected flip-flop remains set, however, until the BIC requests a disconnect by issuing DESX.

The logic remains in this state until the Data Sense flip-flop is set at the end of a conversion. When Data Sense goes true, the output of the Connected flip-flop is gated through to the BIC as TRQX. This pulse requests the BIC to transfer the data word just converted to the computer. The BIC responds to TRQX and TAKX, which results in the data gating signal, Output Enable.

The sequence is repeated each time a new Start ADC signal initiates another conversion cycle. When Data Sense again goes true, the data transfer phase begins. The BIC interrupts the sequence by resetting the Connected flip-flop with DESX.

When the Connected flip-flop resets, the low-to-high transition of its Q output resets the BIC Enable and Program flip-flops.

4.3 PROGRAMMABLE TIMER

The programmable timer consists of a 16-bit down counter and a buffer register. The counter decrements from some number provided by the computer program until the contents of the counter equal zero. At zero, a 100 nanosecond negative going pulse called TMR is generated.

The 16-bit starting number is transferred to the buffer register on EB00 through EB15 with a data transfer out operation. The data transfer must be under program control.

At the start of a data transfer out operation, the ADCM is selected with its device address; Function Select and EB14 set the DTOS flip-flop. The program sets the output word on the E-bus and loads it into the timer buffer register with control pulse DRYX.

One-microsecond (0.5-microsecond in 10-bit version) clock pulses cause the timer to count to zero and generate a TMR pulse. When operating in a continuous mode, the pulse gates the starting number from the buffer register into the timer and the count begins again. In the single-cycle mode, the EXT TMR Control jumper is connected, a relative high level is then required on the EXT TMR Control input to reload the timer. After the timer is reloaded, EXT TMR Control returns to ground.

Timer Sense

The TMR pulse also resets the Timer Sense flip-flop. Output of the Timer Sense flip-flop conditions the Sense 1 flip-flop to be set by a Sense 1 instruction from the program.

The output of the Sense 1 flip-flop goes true with the trailing edge of the Sense 1 instruction. This indicates to the program that the timer has counted to zero but prevents that signal from reaching the computer until the computer is ready to receive it. This synchronizing is necessary to avoid starting a signal race in the computer logic.

The TMR Sense and Sense 1 flip-flops are both reset the next time a new starting number is loaded into the timer.

5. INSTALLATION

5.1 PREREQUISITES

Each ADCM requires one card slot in either the mainframe or Memory Expansion/Peripheral Controller frame. No special slots are reserved for use by ADCM; its location in the frame is determined solely by considerations of convenience in backplane wiring.

A Power Supply Module (Part No. 620-88) must be installed when using an ADCM. If a Power Supply Module has been previously installed and sufficient current is available, an additional module need not be installed.

5.2 INSTALLATION AND INTERCONNECTION

An ADCM is installed vertically, with its component side to the installer's left in 620/i and 620/L computers, and horizontally in the 620/f computer. Figure 5-1 illustrates a typical installation.

> **CAUTION**
>
> Do not install ADCMs in slots that have been previously wired for power; if the intended slot is already wired, remove any connections to power before installing the ADCM to protect its components. Refer to Table 5-1 for proper power connections.

The card is installed with the double pin edge pointing toward the installer. Proper orientation is important since the cards are not keyed.

Connection to the computer I/O-bus and to the BIC option B-bus is provided through backplane wiring. All pin assignments for I/O-bus and B-bus are listed in Appendix B of this manual.

Connections to external instruments include, for each ADCM, one analog signal input, one external sense input, and one programmable timer pulse output. Connector pins are also available for external control inputs to the ADC start logic and the programmable timer. Pin assignments for these connections are also listed in Appendix B. Recommended connector types for J1 and J2 are identified in the summary of key specifications in Appendix C.

Power Supply Wiring

Connections to the ADCM must be made for four power supply voltages and senses, an analog ground, a digital ground, and digital ground sense. Table 5-1 lists the pin assignments on the ADCM wirewrap backplane for these connections. When the ADCM is used with other modules (AOMs, MUXs, etc.) similar voltages should be tied together, and the voltage sense line should be brought from the midpoint of the voltage tie-line to a voltage sense line on the power supply wirewrap backplane. The voltage and sense points for the power supply backplane are given in the Power Supply Manual (Publication No. 03-996-812). This manual also contains detailed information regarding power supply checkout.

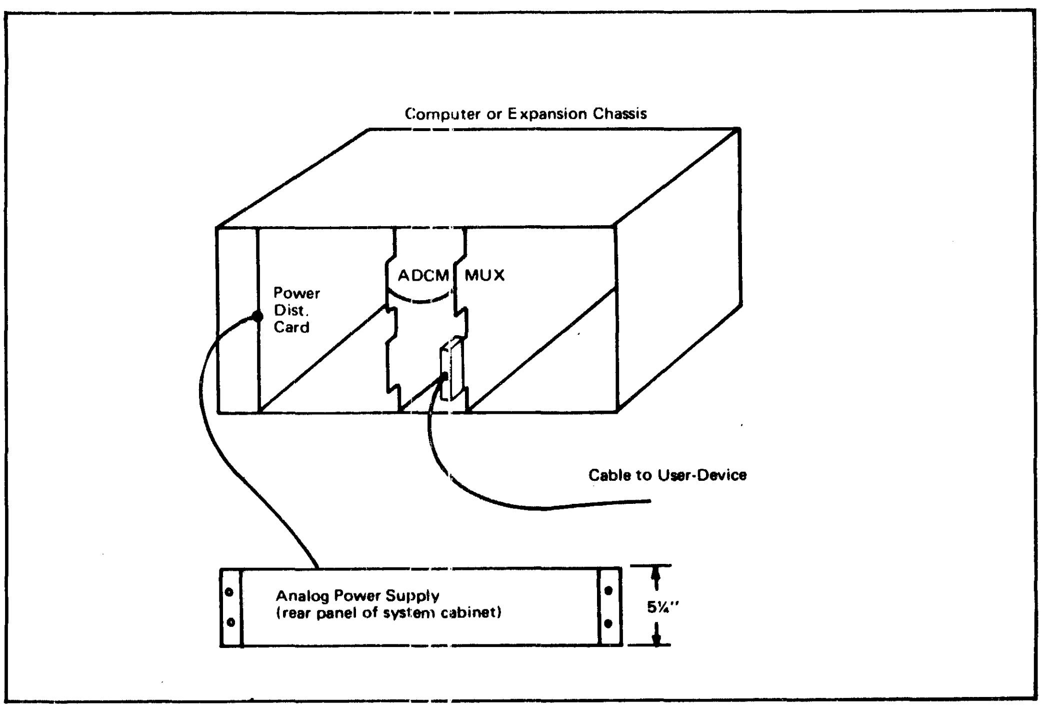


Figure 5-1. Typical Module Installation

Table 5-1. ADCM Wirewrap Backplane Pin Connections for Power Supply

Power Supply Voltage	ADCM Pins
Digital Ground	P1-1, 22, 48, 51, 100, 122, and J1-2
+ 5 Vdc	P1-118, 121
+15 Vdc	P1-111
−15 Vdc	P1-113
−22 Vdc	P1-109
Analog Ground	P1-115

Device Address Wiring

Table 5-2 lists the jumper connections required to wire a device address for an ADCM. Note that P1-74 (Enable) is not normally used. It is available, however, and may be used as an additional addressing condition. For example, if two ADCM modules have the same device address, the Enable input can be used to permit only one module to respond to that address at a given time.

Table 5-2. Device Address Wiring

Address	Wire Wrap Jumpers		
060	P1-71 to P1-72	P1-68 to P1-69	P1-65 to P1-66
061	P1-71 to P1-72	P1-68 to P1-69	P1-64 to P1-66
062	P1-71 to P1-72	P1-67 to P1-69	P1-65 to P1-66
063	P1-71 to P1-72	P1-67 to P1-69	P1-64 to P1-66
064	P1-70 to P1-72	P1-68 to P1-69	P1-65 to P1-66
065	P1-70 to P1-72	P1-68 to P1-69	P1-64 to P1-66
066	P1-70 to P1-72	P1-67 to P1-69	P1-64 to P1-66
067	P1-70 to P1-72	P1-67 to P1-69	P1-64 to P1-66

PIM Wiring

If the computer has the PIM option, then interrupts may be provided by wiring P1-84 to the PIM to enable an interrupt at the completion of an analog-to-digital conversion, and by wiring P1-73 to the PIM to enable an interrupt at the completion of a timer interval.

5.3 INSTALLATION EXAMPLE

Frequently, an ADCM is installed in conjunction with a Multiplexer Module. The following example illustrates typical steps involved in wiring a system which consists of an ADCM, a 16-channel MUX, and a Power Supply Module. These steps are:

1. Wire ADCM and MUX Power Supply
2. Wire ADCM device address
3. Wire MUX device address
4. Wire MUX channel address for 16-channel operation
5. Wire MUX output to ADCM
6. Attach analog input cable to MUX

The interconnections involved in Steps 1 through 4 are shown in Tables 5-3 through 5-5. Step 5 is shown in Figure 5-2, and Step 6 is shown in Figure 5-3. More detailed information on MUX installation may be found in the Multiplexer Manual. Note that to simplify backplane wiring, the ADCM and MUX should be installed in adjacent card slots.

DC Power

The wirewrap interconnections for the power supply for this sample configuration are shown in Table 5-3.

Table 5-3. Typical Power Supply Wiring

From Power Supply Patchboard		To ADC	To MUX
+15 V	P1-102	P1-111	P1-111
-15 V	P1-106	P1-113	P1-113
+20 V	P1-75		P1-107
-22 V	P1-79	P1-109	P1-109
+5 V	P1-89	P1-118	
+5 V	P1-90		P1-118
AGND	P1-111	P1-115	
AGND	P1-112		P1-115
DGND	P1-97	P1-122	
DGND	P1-98		P1-122

Device Address

In this example the ADCM is assigned device address 60_8, and the MUX is assigned device address 61_8, as shown in Table 5-4.

Table 5-4. Typical Device Address Assignments

Signal Name	ADC to ADC		MUX to MUX	
EB-0	P1-65	P1-66		
EB-1	P1-68	P1-69		
EB-2	P1-71	P1-72		
EB-0			P1-65	P1-66
EB-1			P1-68	P1-69
EB-2			P1-71	P1-72
EB-3			P1-74	P1-78
EB-4			P1-77	P1-78

MUX Channel Addresses Wiring

The MUX channel address jumpers for 16-channel operation are shown in Table 5-5.

Table 5-5. Wirewrap Jumpers for 16-Channel MUX Operation

Signal Name	MUX to MUX		ADC
Decode-0	P1-91	P1-80	
Decode-1	P1-93	P1-81	
BUSY		P1-101	P1-75

MUX Output to ADCM

The MUX output signal is provided by means of a shielded twisted pair cable from the MUX to the ADCM, as shown in Figure 5-2.

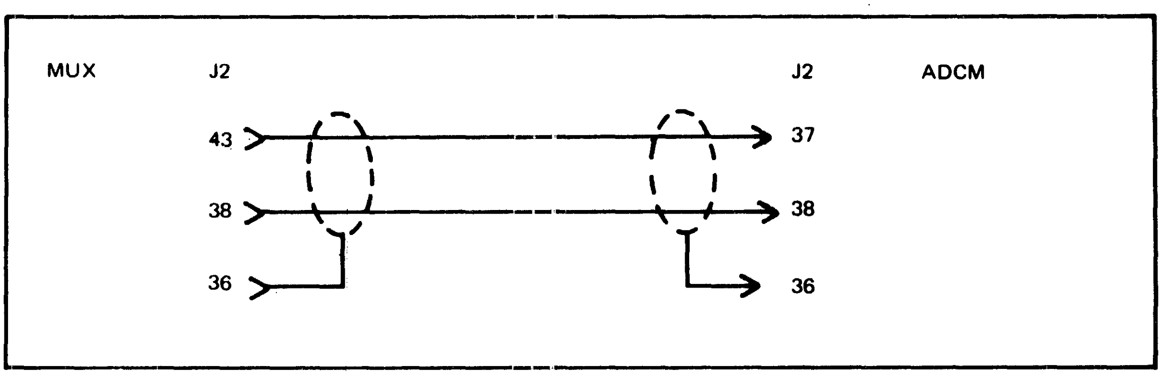


Figure 5-2. MUX Output to ADCM

Analog Input Wiring

Figure 5-3 shows typical input wiring where differential input leads are connected to MUX J1-9 (high) and J1-7 (low) and the ground line is connected to J1-8 (analog ground).

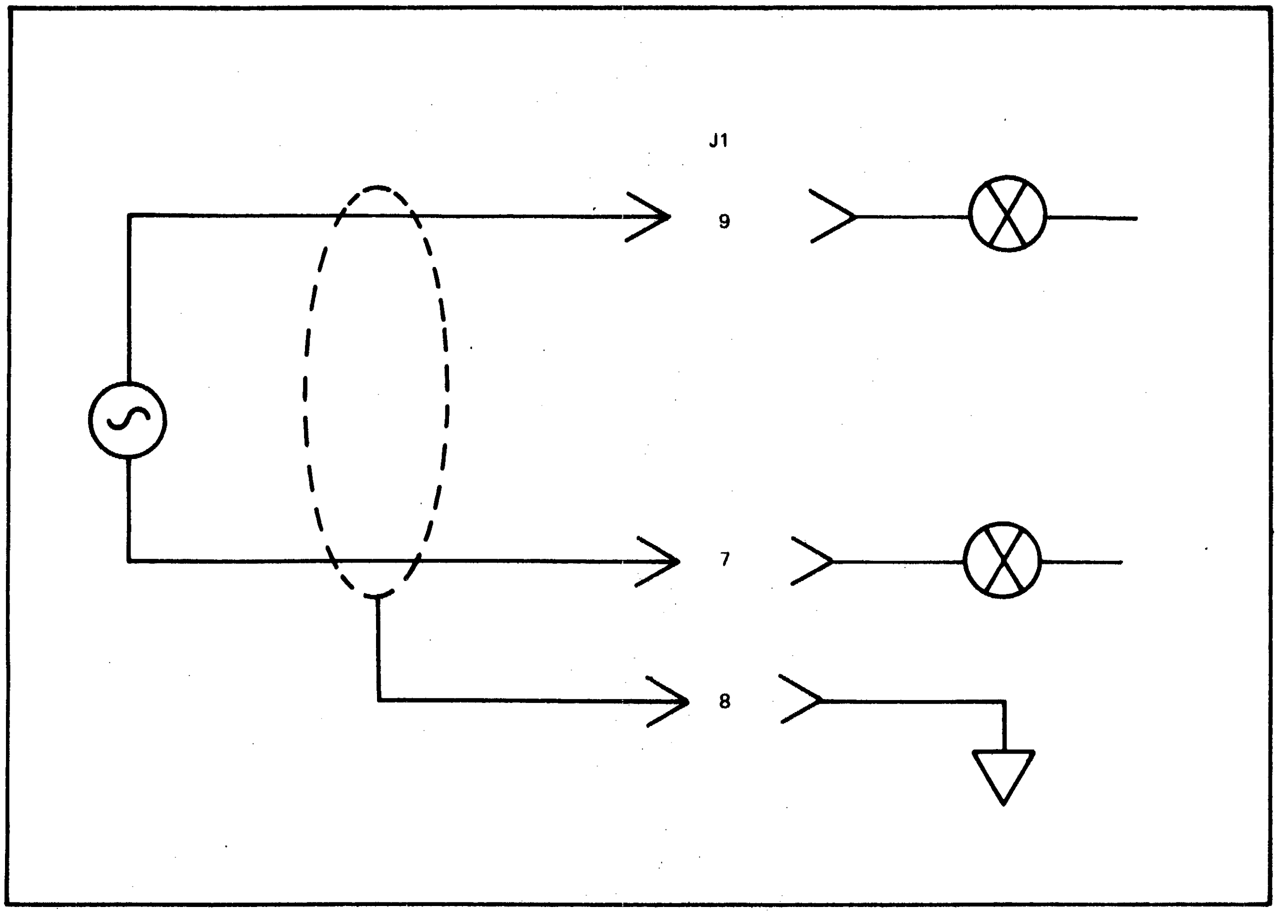
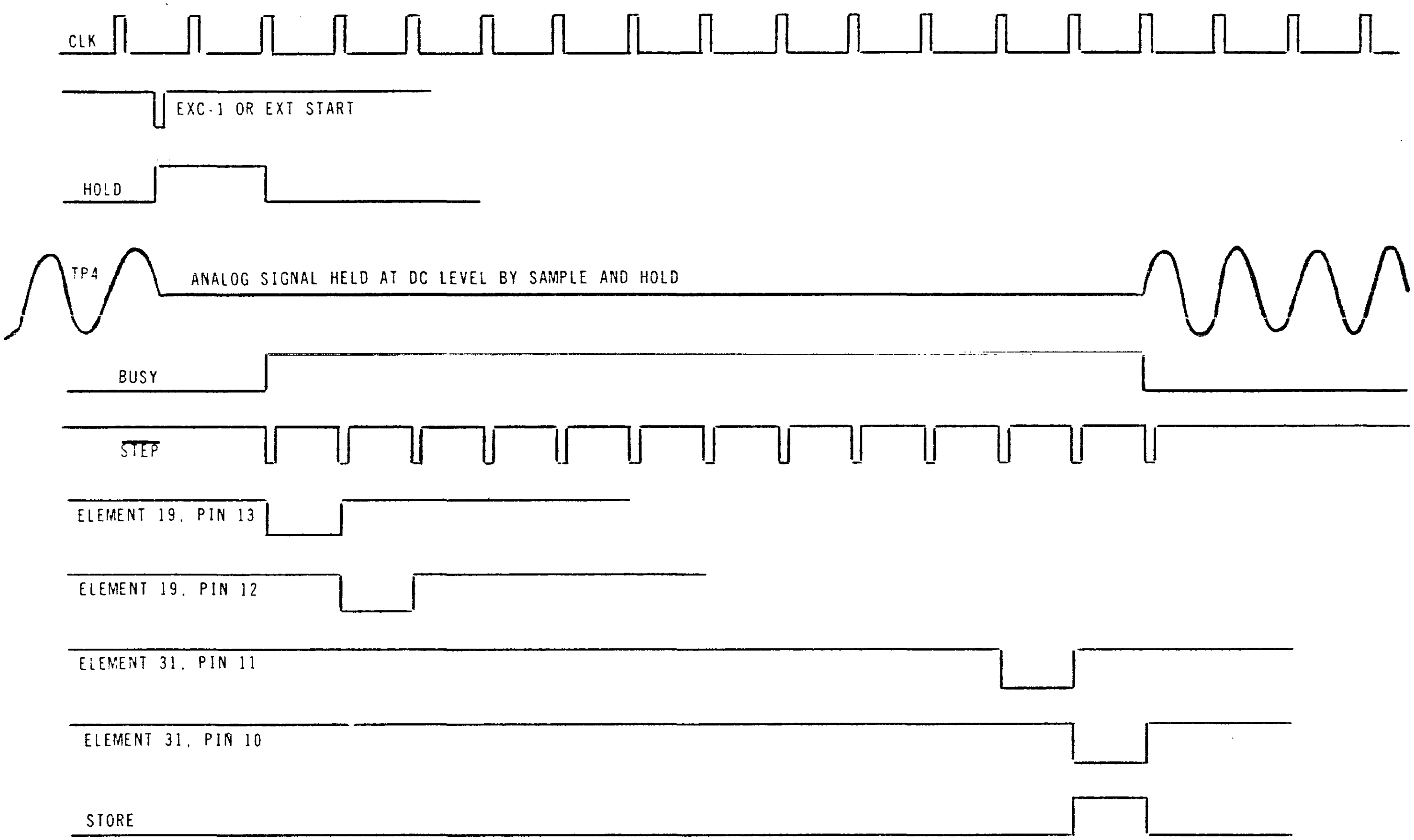


Figure 5-3. Differential Input Connections to MUX

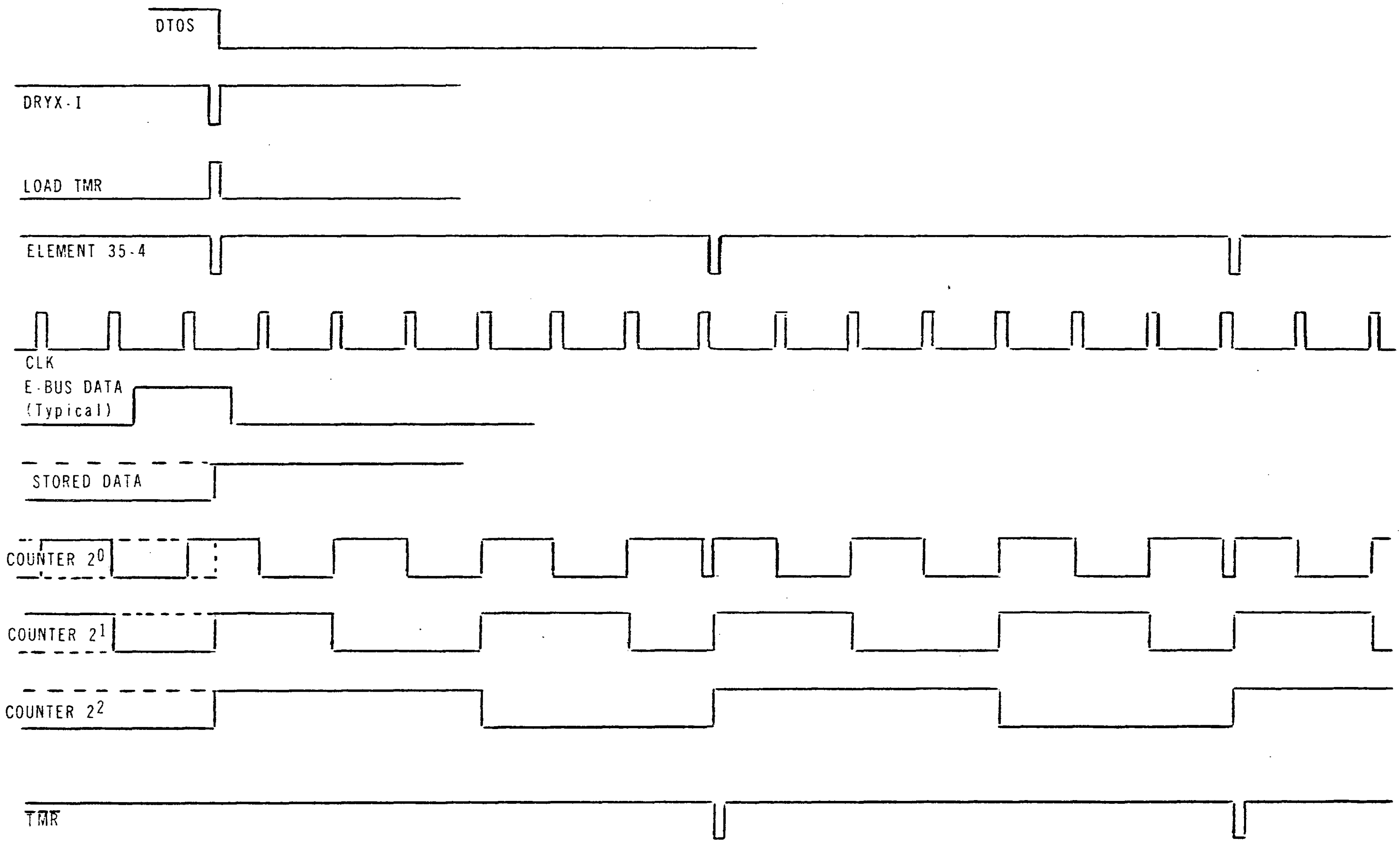
APPENDIX A

TIMING DIAGRAMS



Timing Diagram: ADC Module

Timing Diagram: Programmable Timer



NOTE: In this example, the Timer is loaded with a count of 7 and subsequently emits a pulse every 7 μSEC

APPENDIX B

ADCM PIN ASSIGNMENTS

BACKPLANE WIRING

Pin No.	Name	Name Function
P1-1	Digital Ground	Digital Ground
-2	EB00-I	EB00-I One bit of device address, timer word or data word
-3	Digital Ground	Digital Ground
-4	EB01-I	EB01-I One bit of device address, timer word or data word
-5	Digital Ground	Digital Ground
-6	EB02-I	EB02-I One bit of device address, timer word or data word
-7	Digital Ground	Digital Ground
-8	EB03-I	EB03-I One bit of device address, timer word or data word
-9	Digital Ground	Digital Ground
-10	EB04-I	EB04-I One bit of device address, timer word or data word
-11	EB05-I	EB05-I One bit of device address, timer word or data word
-12	EB06-I	EB06-I One bit of EXC or SEN code, timer word or data word
-13	EB07-I	EB07-I One bit of EXC or SEN code, timer word or data word
-14	EB08-I	EB08-I One bit of EXC or SEN code, timer word or data word
-15	EB09-I	EB09-I One bit of timer word or data word
-16	EB10-I	EB10-I One bit of timer word or data word
-17	EB11-I	EB11-I One bit of timer word or data word
-18	EB12-I	EB12-I One bit of timer word or sign bit
-19	EB13-I	EB13-I One bit of timer word or sign bit
-20	EB14-I	EB14-I One bit of timer word or sign bit
-21	EB15-I	EB15-I One bit of timer word or sign bit
-22	Digital Ground	Digital Ground
-23	Not used	Not used
-24	Digital Ground	Digital Ground
-25	Not used	Not used
-26	Digital Ground	Digital Ground
-27	FRYX-I	FRYX-I Device address tag line
-28	Digital Ground	Digital Ground
-29	DRYX-I	DRYX-I Gates timer word into buffer register
-30	Digital Ground	Digital Ground

BACKPLANE WIRING (Cont.)

Pin No.	Name	Name Function
P1-31	SERX-I	SERX-I Sense input to computer
-32	Digital Ground	Digital Ground
-33	Not used	Not used
-34	Digital Ground	Digital Ground
-35	Not used	Not used
-36	Digital Ground	Digital Ground
-37	Not used	Not used
-38	Digital Ground	Digital Ground
-39	Not used	Not used
-40	Digital Ground	Digital Ground
-41	Not used	Not used
-42	Not used	Not used
-43	SYRT-I	SYRT-I Resets system logic
-44	IUAX-I	IUAX-I Interrupt acknowledge from computer
-45	Not used	Not used
-46	Not used	Not used
-47	Not used	Not used
-48	Digital Ground	Digital Ground
-49	TRQX-B	TRQX-B Transfer request from ADCM to BIC
-50	Not used	Not used
-51	Digital Ground	Digital Ground
-52	Not used	Not used
-53	Digital Ground	Digital Ground
-54	CDCX-B	CDCX-B Notifies BIC that ADCM is connected
-55	Digital Ground	Digital Ground
-56	DCEX-B	DCEX-B Connect signal from BIC
-57	Digital Ground	Digital Ground
-58	TAKX-B	TAKX-B Transfer request acknowledge from BIC
-59	Digital Ground	Digital Ground
-60	DESX-B	DESX-B Disconnect from BIC
-61	Not used	Not used
-62	Not used	Not used
-63	Not used	Not used
-64	EB00 +	EB00 + Jumper connection for wiring device address
-65	EB00-	EB00 - Jumper connection for wiring device address
-66	EB0I +	EB0I + Jumper connection for wiring device address
-67	EB01 +	EB01 + Jumper connection for wiring device address
-68	EB01-	EB01 - Jumper connection for wiring device address
-69	EB1I +	EB11 + Jumper connection for wiring device address
-70	EB02 +	EB02 + Jumper connection for wiring device address

BACKPLANE WIRING (Cont.)

Pin No.	Name	Name Function
P1-71	EB02	EB02 Jumper connection for wiring device address
-72	EB2I +	EB2I + Jumper connection for wiring device address
-73	TIMER OUT	TIMER OUT For external use of timer
-74	ENABLE	ENABLE Not normally used
-75	BUSY	BUSY Notifies multiplexer that ADC is converting
-76	Not used	Not used
-77	Not used	Not used
-78	Not used	Not used
-79	Not used	Not used
-80	Not used	Not used
-81	Not used	Not used
-82	Not used	Not used
-83	OUTPUT ENABLE	OUTPUT ENABLE Gates data onto E-bus
-84	STORE	STORE Indicates that conversion is complete
-85	DTOS	DTOS Timer word transfer request to computer
-86	Not used	Not used
-87	CLK	CLK For external use of CLK pulses
-88	Not used	Not used
-89	DTIS	DTIS Request to transfer data to computer
-90	Not used	Not used
-91	Not used	Not used
-92	Not used	Not used
-93	Not used	Not used
-94	Not used	Not used
-95	Not used	Not used
-96	Not used	Not used
-97	Not used	Not used
-98	Not used	Not used
-99	Not used	Not used
-100	Digital Ground	Digital Ground
-101	ERR	ERR Sets Data Sense condition
-102	Not used	Not used
-103	Not used	Not used
-104	Not used	Not used
-105	Not used	Not used
-106	Not used	Not used
-107	Not used	Not used
-108	Not used	Not used
-109	-20 Vdc	-20 Vdc
-110	Not used	Not used

APPENDIX B (Continued)

Pin No.	Name	Name Function
P1-111	+15 Vdc	+15 Vdc
-112	Not used	Not used
-113	-15 Vdc	-15 Vdc
-114	Not used	Not used
-115	Analog Ground	Analog Ground
-116	Not used	Not used
-117	Not used	Not used
-118	+5 Vdc	+5 Vdc
-119	Not used	Not used
-120	Not used	Not used
-121	+5 Vdc	+5 Vdc
-122	Digital Ground	Digital Ground

TERMINAL EDGE CONNECTOR WIRING

Pin No.	Name	Name Function
J1-1	Not used	Not used
-2	Digital Ground	Digital Ground
-3	Not used	Not used
-4	Digital Ground	Digital Ground
-5	Not used	Not used
-6	Digital Ground	Digital Ground
-7	Not used	Not used
-8	Digital Ground	Digital Ground
-9	Not used	Not used
-10	Digital Ground	Digital Ground
-11	Not used	Not used
-12	Digital Ground	Digital Ground
-13	Not used	Not used
-14	Digital Ground	Digital Ground
-15	Not used	Not used
-16	Digital Ground	Digital Ground
-17	Not used	Not used
-18	Digital Ground	Digital Ground
-19	Not used	Not used
-20	Digital Ground	Digital Ground
-21	Not used	Not used
-22	Digital Ground	Digital Ground
-23	Not used	Not used
-24	Digital Ground	Digital Ground
-25	Not used	Not used

TERMINAL EDGE CONNECTOR WIRING (Cont.)

Pin No.	Name	Name Function
J1-26	Digital Ground	Digital Ground
-27	2^0	2^0
-28	Digital Ground	Digital Ground
-29	Not used	Not used
-30	Digital Ground	Digital Ground
-31	Not used	Not used
-32	Digital Ground	Digital Ground
-33	Not used	Not used
-34	Digital Ground	Digital Ground
-35	EXT SEN	EXT SEN Input connection for EXT SEN line
-36	Digital Ground	Digital Ground
-37	EXT START	EXT START Input connection for EXT START line
-38	Digital Ground	Digital Ground
-39	Timer Out	Timer Out Output connection for timer pulses
-40	Digital Ground	Digital Ground
-41	EXT TMR CNTL	EXT TMR CNTL Input connection for EXT TMR CNTL line
-42	Digital Ground	Digital Ground
-43	Not used	Not used
-44	Digital Ground	Digital Ground
J2-1	Not used	Not used
-2	Analog Ground	Analog Ground
-3	Not used	Not used
-4	Analog Ground	Analog Ground
-5	Not used	Not used
-6	Analog Ground	Analog Ground
-7	Not used	Not used
-8	Analog Ground	Analog Ground
-9	Not used	Not used
-10	Analog Ground	Analog Ground
-11	Not used	Not used
-12	Analog Ground	Analog Ground
-13	Not used	Not used
-14	Analog Ground	Analog Ground
-15	Not used	Not used
-16	Analog Ground	Analog Ground
-17	Not used	Not used
-18	Analog Ground	Analog Ground
-19	Not used	Not used
-20	Analog Ground	Analog Ground
-21	Not used	Not used
-22	Analog Ground	Analog Ground

TERMINAL EDGE CONNECTOR WIRING (Cont.)

Pin No.	Name	Name Function
J2-23	Not used	Not used
-24	Analog Ground	Analog Ground
-25	Not used	Not used
-26	Analog Ground	Analog Ground
-27	Not used	Not used
-28	Analog Ground	Analog Ground
-29	Not used	Not used
-30	Analog Ground	Analog Ground
-31	Not used	Not used
-32	Analog Ground	Analog Ground
-33	Not used	Not used
-34	Analog Ground	Analog Ground
-35	Not used	Not used
-36	Analog Ground	Analog Ground
-37	SIG +	SIG + Input connection for + analog signal
-38	Analog Ground	Analog Ground
-39	Not used	Not used
-40	Analog Ground	Analog Ground
-41	Not used	Not used
-42	Analog Ground	Analog Ground
-43	SIG -	SIG - Input connection for - analog signal
-44	Analog Ground	Analog Ground

APPENDIX C: SPECIFICATIONS

ANALOG-TO-DIGITAL CONVERTER

Resolution	13 binary bits 10 binary bits
Output Format	Two's complement
Conversion Accuracy	± 0.012% of full scale, ± 1/2 LSB (13-bit) ± 0.05% of full scale, ± 1/2 LSB (10-bit)
Conversion Time	10 μsec, maximum (13-bit) 5 μsec, maximum (10-bit)
Temperature Coefficient	± 50 mV/°C, maximum
Warm-Up Time	Essentially zero
Full Scale Range	± 10 V
Digital Outputs	
BUSY	High (true) during Analog-to-Digital conversion. Available fanout: 8 logic loads. Maximum capacitive load: 100 pF.
STORE	Low (true) during last 1 μsec of the BUSY signal. Available fanout: 10 logic loads. Maximum capacitive load: 1000 pF.
Output Enable	High (true) during the time ADC data is on the E-Bus (1.90 μ sec). Available fanout: 20 logic loads. Maximum capacitive load: 100 pF.
Digital Inputs	
EXT START	1 kΩ to +5 V; low true sense input. Computer may test the status of this input with a SEN 2YY instruction.
EXT SENSE	5.6 kΩ to + 5 V; low true sense input. Computer may test the status of this input with a SEN 2YY instruction.

PROGRAMMABLE TIMER

Clock Frequency	1.0 MHz ± 0.01% (13-bit) 2.0 MHz ± 0.01% (10-bit)

Clock Drift	± 1 PPM/°C
Clock Stability	± 0.01 PPM/day
Resolution	16 binary bits (computer E-Bus $2^0 - 2^{15}$)
Programmed PRF	1 MHz to 15.26 Hz (13-bit) 2 MHz to 30.52 Hz (10-bit) 1 μsec to 65.535 milliseconds (13-bit) 0.5 μsec to 32.767 milliseconds (10-bit)
Timer Output	100 nanosecond pulse to ground. 1 kΩ to + 5 V sinks 100 mA. Maximum capacity load 1000 pF.
CLK Output	100 nanosecond pulse from low to high. TTL output. Available fanout: 6 logic loads. PRF = 1.0 MHz ± 0.01% (13-bit) 2.0 MHz ± 0.01% (10-bit)
Timer Clock Input	1 TTL load. Maximum PRF = 10 MHz. Increments counter on low to high position.

SAMPLE AND HOLD

Gain and Accuracy	
Voltage Gain	+1
Accuracy	± 0.01% of FS
Gain Temperature Coefficient	± 10 PPM/°C
Track Mode, Single Ended	
Full Power Sine Wave	65 kHz
Slew Rate	4 V/μsec
Settling Time to	± 1 mV, 4 μsec
Track Mode, Differential	
Full Power Sine Wave	15 kHz
Slew Rate	1/μsec
Settling Time to	± 1 mV, 30 μsec
Input Characteristics, Single Ended	
Single Range	± 10 V
Maximum Rating (without damage)	± 15 V

Input Impedance	50 kΩ in parallel with 5000 pF.
Offset Voltage	± 2 mV maximum
VS Temperature	± 50 mV/°C
Input Characteristics, Differential	
Signal Range	± 10 V
Maximum Rating (without damage)	± 30 V
Input Impedance	50 kΩ
Common Mode Rejection	80 dB, 0 to 60 Hz
Offset Voltage	± 2 mV, maximum
VS Temperature	± 100 mV/°C
Output Characteristics	
Signal Range	± 10 V
Noise, RMS Wideband (hold mode)	± 1 mV peak-to-peak
Decay Rate in, hold mode	± 10 mV/sec
Feedthrough 20 V Step (hold mode)	- 80 dB
Switching Characteristics	
Aperture Time, Maximum	100 nanoseconds
Offset Pedestal, Maximum	± 2 mV
Acquisition Time, Maximum	6 μsec

POWER

+15 Vdc ± 0.1%; 150 mA
-15 Vdc ± 1% ; 150 mA
-22 Vdc ± 2%; 2 mA
+5 Vdc ± 5%; 1275 mA

TEMPERATURE RANGE

Specification	0° to 50°C
Operating	-10° to 70°C
Storage	-55° to 85°C

PHYSICAL CHARACTERISTICS

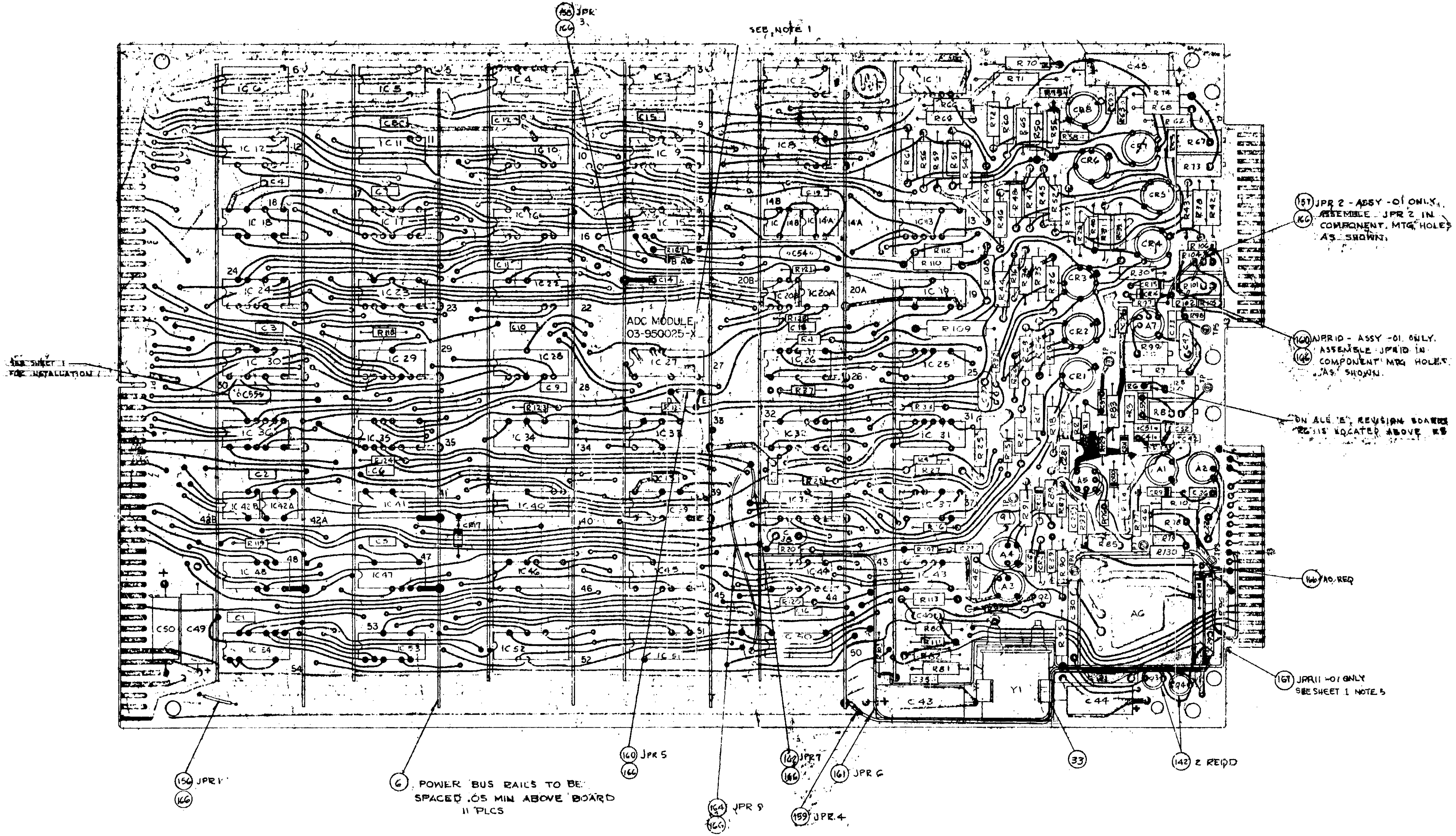
Dimensions	One printed circuit board 7-3/4 x 12 x 1/2 inches
Connectors	Two 44-terminal card edge connectors One 122-terminal card edge connector

MODULE PERFORMANCE SUMMARY

Accuracy	± 0.025% of FS
Accuracy (with Multiplexer)	± 0.040% of FS
Throughput Rate	55 kHz, maximum (13-bit) 105 kHz, maximum (10-bit)
Throughput Rate (with Multiplexer)	50 kHz, maximum (13-bit) 100 kHz, maximum (10-bit)

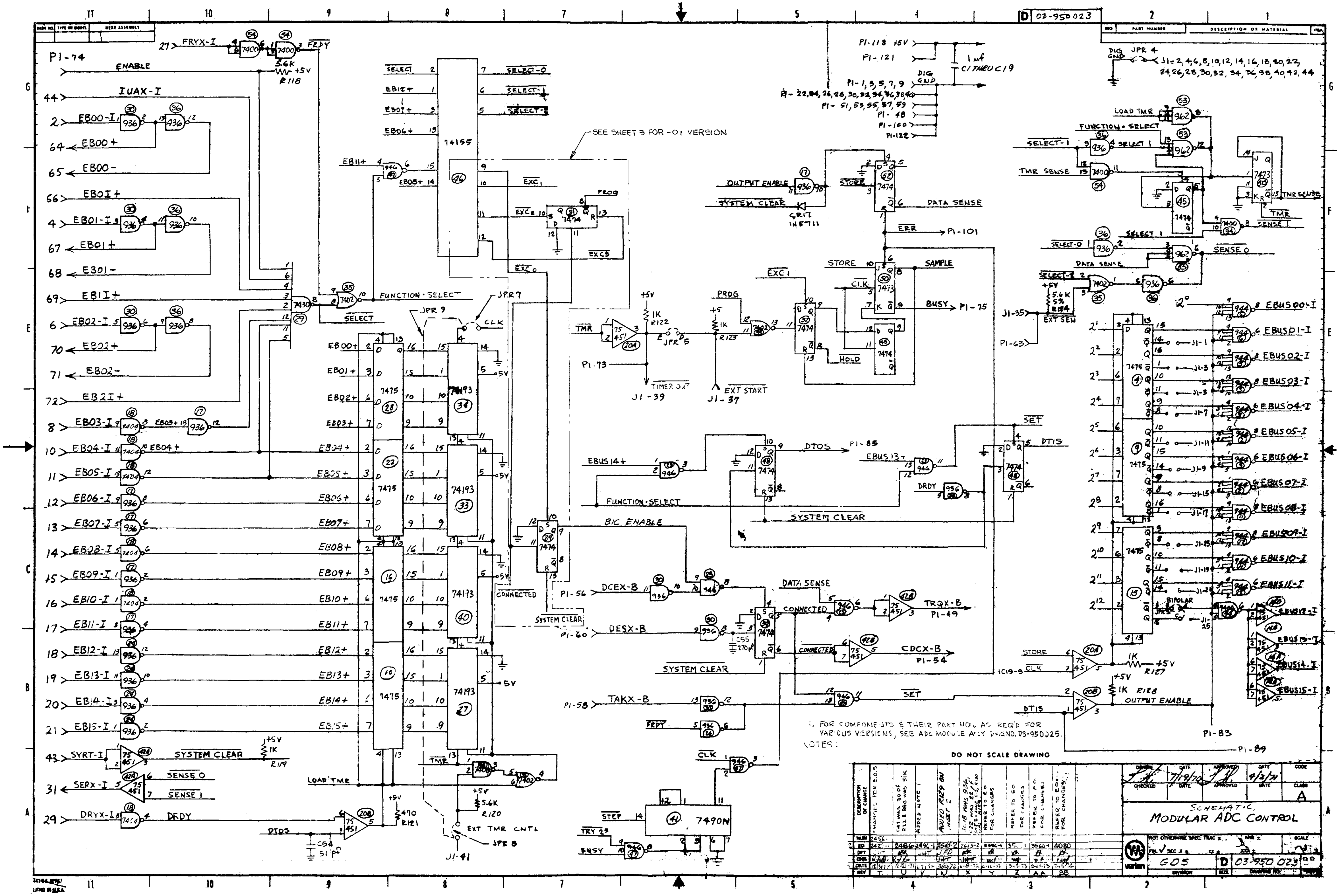
APPENDIX D

SCHEMATICS, ASSEMBLIES AND PARTS LISTS



MARK IN BLACK DASH NO. & CURRENT ASSY REV LETTER

NOTES


D 03-950023
SEE SHEET 3 FOR -01 VERSION
1. FOR COMPONENTS & THEIR PART NOS AS REQ'D FOR VARIOUS VERSIONS, SEE ADC MODULE ASSY DWG NO. 03-950025.
NOTES:
DO NOT SCALE DRAWING
SCHEMATIC, MODULAR ADC CONTROL
GDS
D 03-950 023
FUNCTION · SELECT
SYSTEM CLEAR
DATA SENSE
BIC ENABLE
CONNECTED
OUTPUT ENABLE
LOAD TMR
EXT TMR CNTL
TIMER OUT
EXT START
74155
7474
7475
74193
7490N
7473

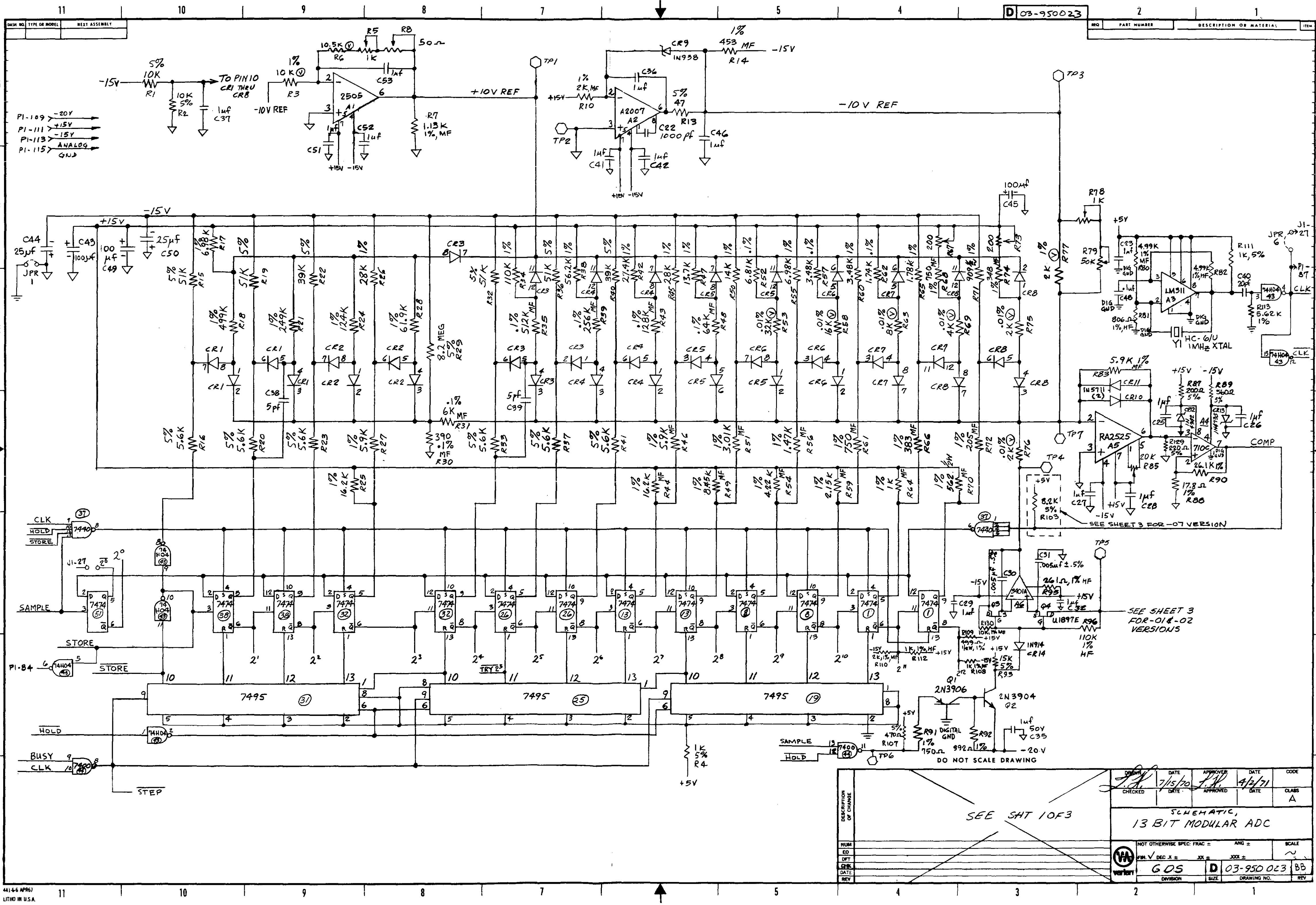
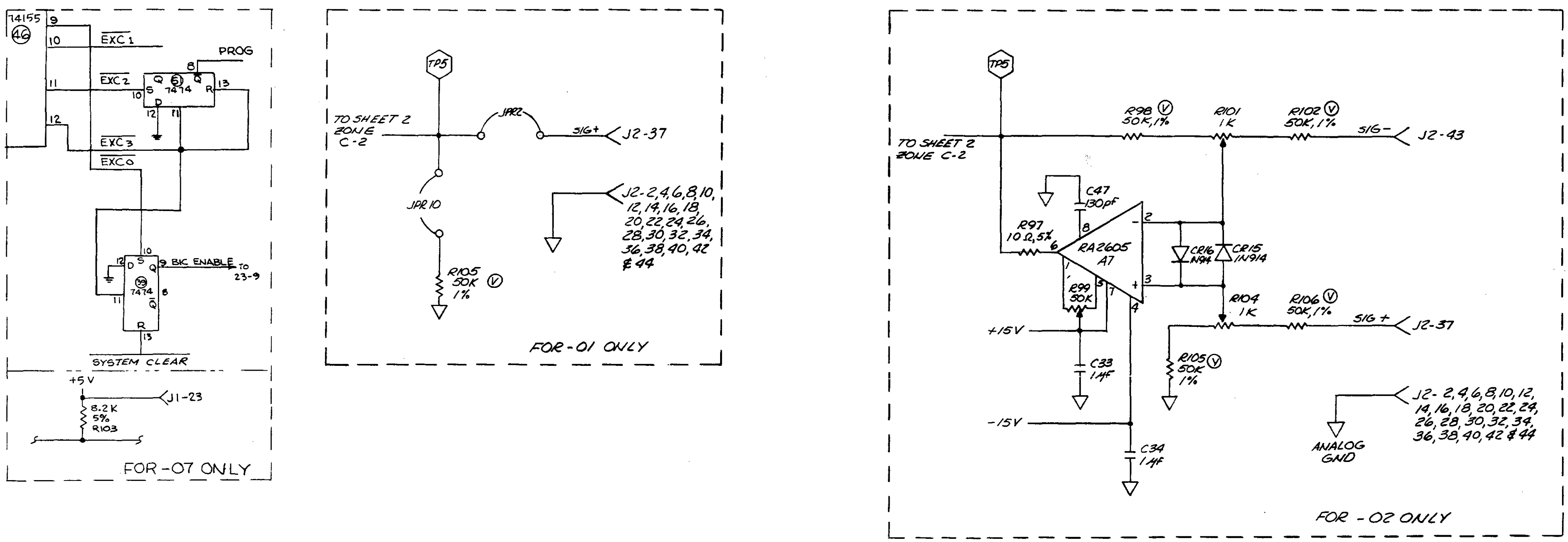


Figure D-1, Sht 2



DO NOT SCALE DRAWING

SEE SHEET 1 OF 3

DRAWN J. DAY	DATE 9/14/71	APPROVED	DATE	CODE
CHECKED	DATE 9/16/71	APPROVED	DATE	CLASS A

SCHEMATIC, 13 BIT MODULAR ADC

varian GDS — SIZE D — DRAWING NO. 03-950 023 — REV BB

D 03-950 023

4416-6 APR67
LITHO IN U.S.A.

Figure D-1, Sht 3

ADC MODULE, 03-950025

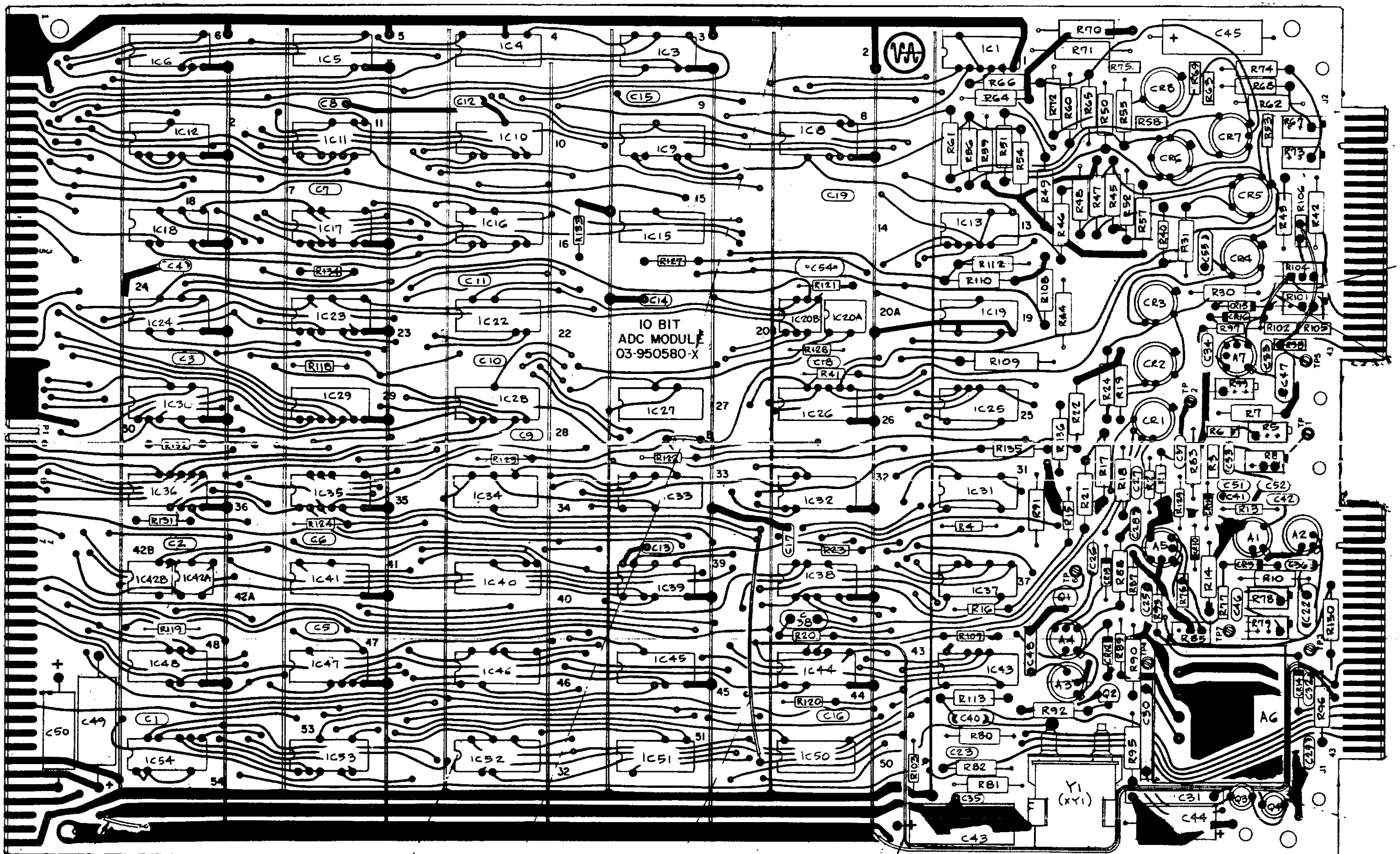
Schematic Reference	Description	Varian Part No.
IC1, 18, 13, 26		
32, 38, 39, 45,		
48, 51, 52	IC Element - 7474	62-600 365
IC39, 45, 48, 51, 52		
~~IC2, 3, 5, 6, 11, 12~~	~~IC Element - 944~~	62-600 306
IC4, 9, 10, 15, 16		
~~22, 28,~~ IC10, 16		
22, 28	IC Element - 7475	62-600 351
IC17, 24, 30, 36	IC Element - 936	62-600 309
IC19, 25, 31	IC Element - 7495	62-600 406
IC20A, 14A &B,		
42A &B, 20B,		
42A &B	IC Element - 75451	62-600 260
IC23, 47	IC Element - 946	62-600 303
IC27, 33, 34, 40	IC Element - 74193	62-600 367
IC29	IC Element - 7430	62-600 359
IC35	IC Element - 7402	62-600 356
IC37	IC Element - 7440	62-600 310
IC41	IC Element - 7490 N	62-600 350
IC43	IC Element - 74H04	62-600 012
IC44, 54	IC Element - 7400	62-600 355
IC46	IC Element - 74155	62-600 271
IC50	IC Element - 7473	62-600 362
~~IC 53~~	~~IC Element - 962~~	62-600 300
IC18	IC Element - 7404 N	62-600 013
Y1	Crystal	66-479 984
A1	Amplifier, 2505	62-600 219
A2	Amplifier, 42007	62-600 235
A3	Amplifier, LM311	62-600 208
A4	Amplifier, μA710 C	62-600 190
A5	Amplifier, 2525	62-600 204
A6	Amplifier, 3401 A	78-199 966
A7	Amplifier, 2605	62-600 203
CR1-CR8	Diode Array, CA3039	62-600 091
CR9	Diode, 1N938	66-300 938
CR10, 11, 17	Diode, 1N5711	66-981 101
CR12	Diode, 1N4742	66-304 742
CR13	Diode, 1N4735	66-304 735
CR14	Diode, 1N914	66-304 148
CR15, 16		
R1, 2	Res, F.C. 10 K, 1/4 W, 5%	32-301 510
R4, 111, 119, 122,		
123, 127, 128	Res, F.C. 1 K, 1/4 W, 5%	32-301 410
R13	Res, F.C. 47 Ω, 1/4 W, 5%	32-301 247
R15, 19, 32, 36	Res, F.C. 51 K, 1/4 W, 5%	32-301 551

ADC MODULE, 30-950025 (Cont'd)

Schematic Reference	Description	Varian Part No.
R16,20,23,33 37,41,118,120 124	Res, F.C. 5.6 K, 1/4 W, 5%	32-301 456
R29	Res, F.C. 8.2 MEG, 1/4 W, 5%	32-301 782
R93	Res, F.C., 15 K, 1/4 W, 5%	32-301 515
R97	Res, F.C. 10Ω, 1/4 W, 5%	32-301 210
R103	Res, F.C. 8.2 K, 1/4 W, 5%	32-301 482
R107,R121	Res, F.C. 470 Ω, 1/4 W, 5%	32-301 347
R87	Res, F.C. 200 Ω, 1/4 W, 5%	32-301 320
R89	Res, F.C. 560 Ω, 1/4 W, 5%	32-301 356
R129	Res, F.C. 220 Ω, 1/4 W, 5%	32-301 322
R22,R40	Res, F.C. 39 K, 1/4 W, 5%	32-301 539
R7	Res, MF, 1.13 K, 1/4 W, 1%	31-224 113
R10,110	Res, MF, 2 K, 1/4 W, 1%	31-224 200
R14	Res, MF, 453 Ω, 1/4 W, 1%	31-223 453
R17,55	Res, MF, 6.98 K, 1/4 W, 1%	31-224 698
R18	Res, MF, 499 K, 1/4 W, 1%	31-226 499
R21	Res, MF, 249 K, 1/4 W, 1%	31-226 249
R24	Res, MF, 124 K, 1/4 W, 1%	31-226 124
R25,44	Res, MF, 16.2 K, 1/4 W, 1%	31-225 162
R26,45	Res, MF, 28 K, 1/4 W, 1%	31-225 280
R27,46,83	Res, MF, 5.9 K, 1/4 W, 1%	31-224 590
R28	Res, MF, 61.9 K, 1/4 W, 1%	31-225 619
R34,R96	Res, MF, 110 K, 1/4 W, 1%	31-226 110
R38	Res, MF, 56.2 K, 1/4 W, 1%	31-225 562
R42	Res, MF, 27.4 K, 1/4 W, 1%	31-225 274
R47	Res, MF, 13.7 K, 1/4 W, 1%	31-225 137
R49	Res, MF, 8.45 K, 1/4 W, 1%	31-224 845
R50	Res, MF, 14 K, 1/4 W, 1%	31-225 140
R51	Res, MF, 3.01 K, 1/4 W, 1%	31-224 301
R54	Res, MF, 4.22 K, 1/4 W, 1%	31-224 422
R56	Res, MF, 1.47 K, 1/4 W, 1%	31-224 147
R59	Res, MF, 2.15 K, 1/4 W, 1%	31-224 215
R60	Res, MF, 3.48 K, 1/4 W, 1%	31-224 348
R61,68,91	Res, MF, 750 Ω, 1/4 W, 1%	31-223 750
R64,108,112	Res, MF, 1 K, 1/4 W, 1%	31-224 100
R65	Res, MF, 1.78 K, 1/4 W, 1%	31-224 178
R66	Res, MF, 383 Ω, 1/4 W, 1%	31-223 383
R72	Res, MF, 205 Ω, 1/4 W, 1%	31-223 205
R74	Res, MF, 348 Ω, 1/4 W, 1%	31-223 348
R80,82	Res, MF, 4.99 K, 1/4 W, 1%	31-224 499
R90	Res, MF, 26.1 K, 1/4 W, 1%	31-225 261
R92	Res, MF, 392 Ω, 1/4 W, 1%	31-223 392
R95	Res, MF, 261 Ω, 1/4 W, 1%	31-223 261
R130	Res, MF, 10 K, 1/4 W, 1%	31-225 100
R113	Res, MF, 5.62 K, 1/4 W, 1%	31-224 562
R88	Res, MF, 17.8 Ω, 1/4 W, 1%	31-222 178
R81	Res, MF, 806 Ω, 1/4 W, 1%	31-223 806
R70	Res, MF, 562 Ω, 1/2 W, 1%	31-614 654

ADC MODULE, 30-950025 (Cont'd)

Schematic Reference	Description	Varian Part No.
R71	Res, MF, 909 Ω, 1/2 W, 1%	31-614 653
R109	Res, MF, 499 Ω, 1/2 W, 1%	31-614 655
R53	Res, MF, 32 K, .01%	31-239 053
R58	Res, MF, 16 K, .01%	31-239 052
R63	Res, MF, 8 K, .01%	31-239 051
R69	Res, MF, 4 K, .01%	31-239 050
R75,R76	Res, MF, 2 K, .01%	31-239 059
R98,102,105, 106	Res, MF, 50 K, 1%	31-239 058
R6	Res, MF, 10.5 K, 1%	31-239 057
R77	Res, MF, 2 K, 1%	31-239 031
R3	Res, MF, 10 K, 1%	31-239 033
R30	Res, MF, 390 Ω, .1%	31-613 347
R31	Res, MF, 6 K,	31-613 281
R35	Res, MF, 512 K	31-613 339
R39	Res, MF, 256 K	31-613 340
R43	Res, MF, 128 K	31-613 344
R48	Res, MF, 64 K	31-613 343
R52	Res, MF, 6.81 K	31-613 342
R57	Res, MF, 3.48 K	31-613 345
R62	Res, MF, 1.74 K, .1%	31-613 346
R5,R78,101,104	Res, VAR, W.W. 1 K	37-577 311
R8	Res, VAR, W.W. 50 Ω	37-577 308
R67,R73	Res, VAR, W.W. 200 Ω	37-577 310
R79,99	Res, VAR, W.W. 50 K	37-577 315
R85	Res, VAR, W.W. 20 K	37-577 314
Q1	Transistor, 2N3906	62-903 906
Q2	Transistor, 2N3904	62-903 904
Q3,Q4	Transistor, FET, U1897E	62-798 125
C1-19,23,25-29, 32-37,41,42,46,51-53, C2,4,5,8,9,12,13, 14,16,19,23	Cap, CER, 1 μf, 200 V, 10%	41-228 009
C22	Cap, CER, 1000 pf, 100 V, 5%	41-159 599
C30,C31	Cap, Mylar, .005 μf, 100 V, 1/2%	41-718 754
C38,C39	Cap, CER, 5 pf, 500 V, 10%	41-159 505
C40,	Cap, CER, 20 pf, 500 V, 5%	41-159 573
C43,45,49	Cap, Elect, 100 μf, 25 V	41-506 258
C44,50	Cap, Elect, 25 μf, 25 V	41-506 255
C47	Cap, CER, 130 pf, 500 V, 5%	41-159 566
C48	Cap, CER, .1 μf, 25 V, 20%	41-206 993
C55	Cap, 270 pf, 500V	41-159 601
C54	Cap, MICA, 51 pf, 500V,5%	41-159 584


10 BIT
ADC MODULE
03-950580-X

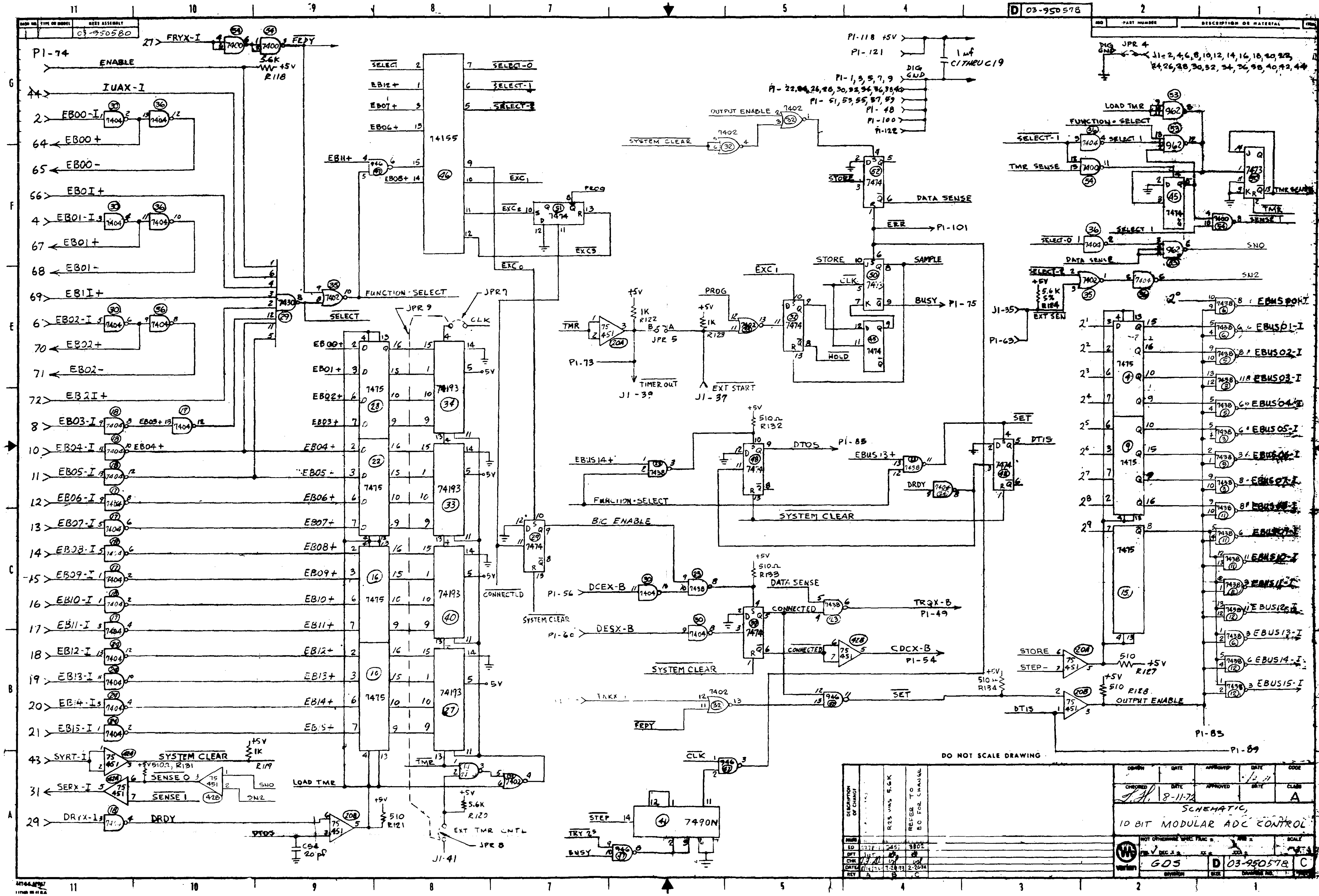


Figure D-2, Sht 1

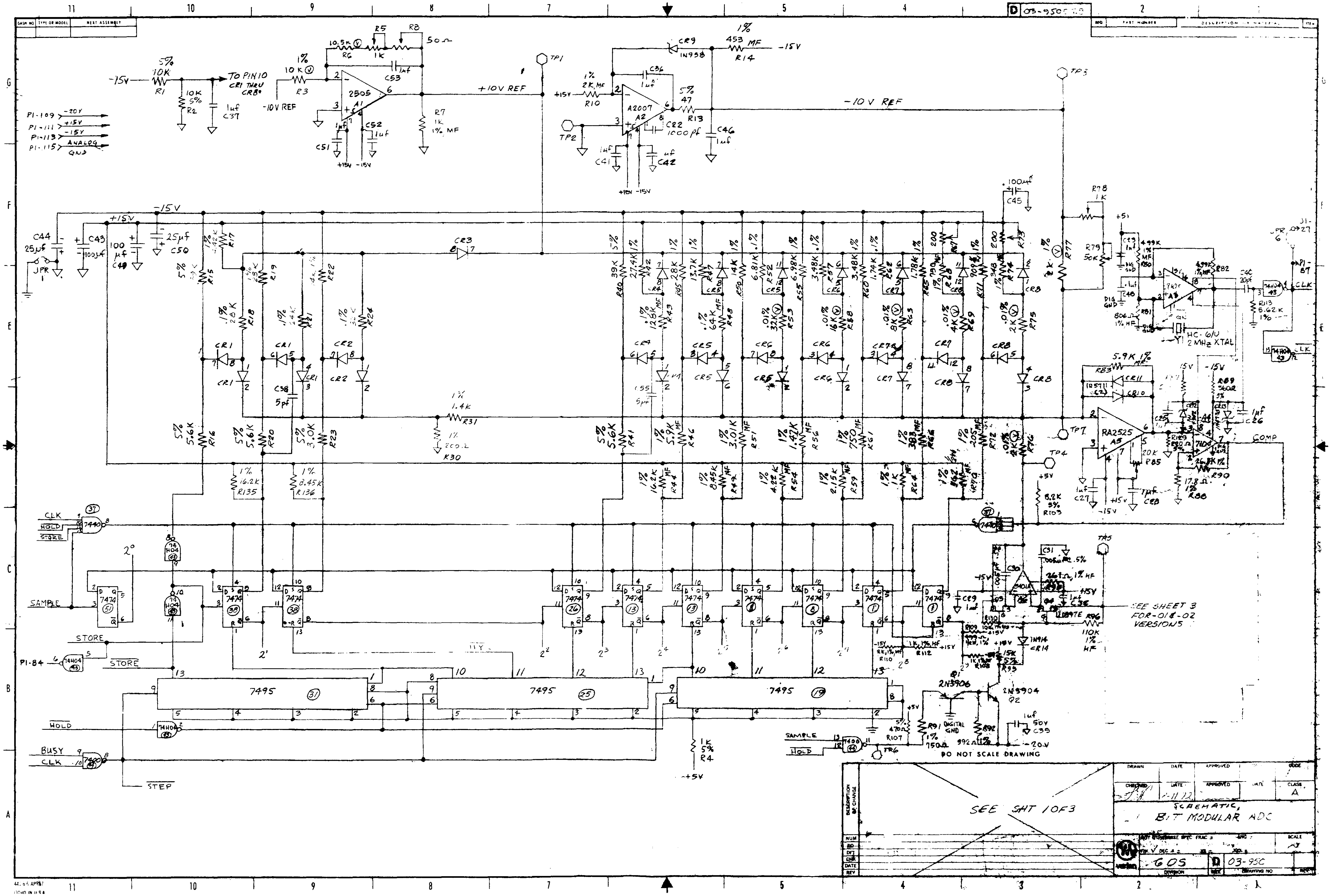


Figure D-2, Sht 2

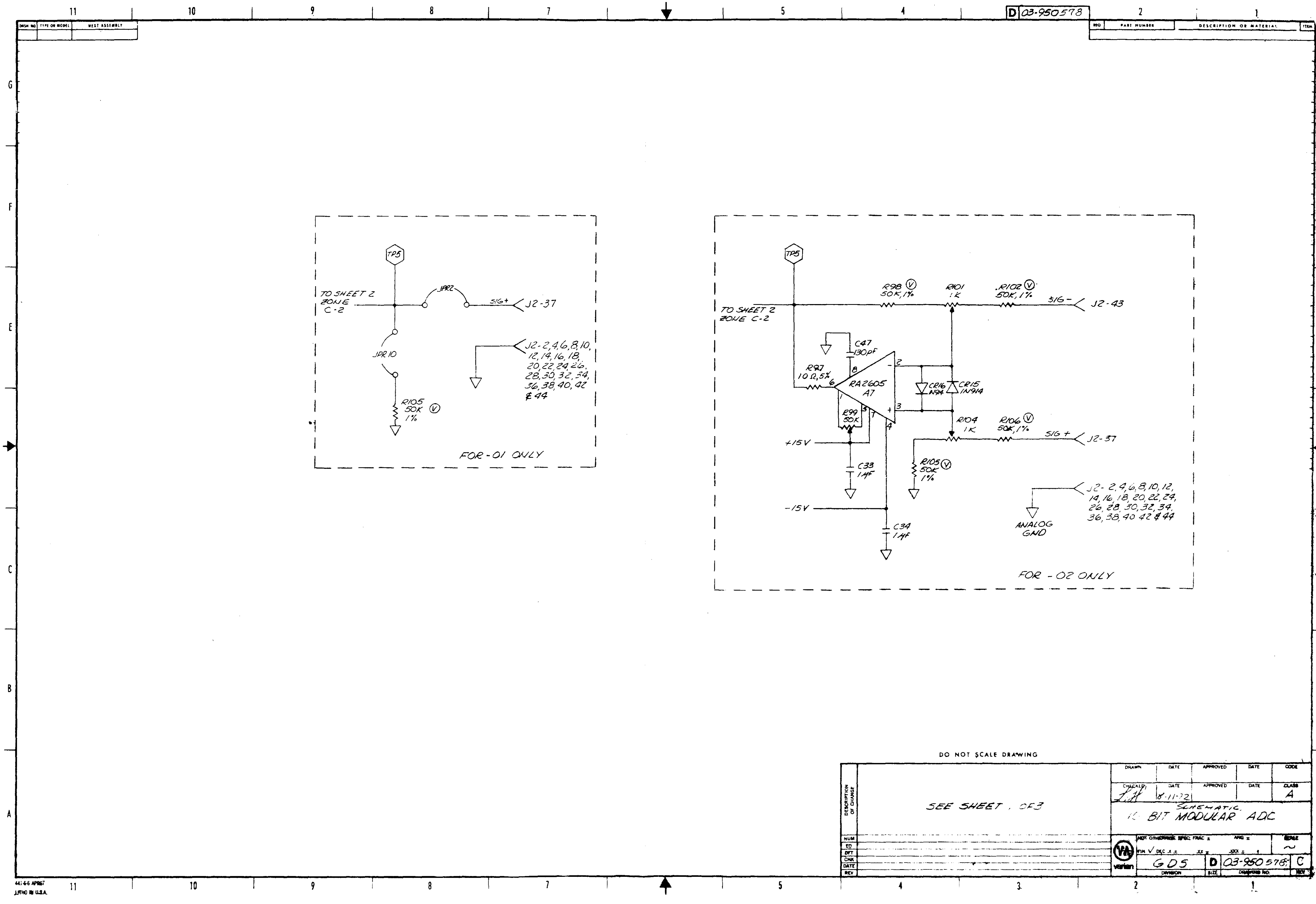


Figure D-2, Sht 3

10 BIT ADC MODULE, 03-950580

Schematic Reference	Description	Varian Part No.
TP1-TP7	Terminal, Swage	16-229 857
IC1, 8, 15, 26, 38, 39, 45, 48, 51, 52	IC Element - 7474	62-600 365
IC4, 9, 10, 15, 16, 22, 28	IC Element - 7475	62-600 351
IC3, 5, 6, 11, 12, 23	IC Element - 7438	62-600 373
IC19, 25, 31	IC Element - 7495	62-600 406
IC20A, 20B, 42A, 42B	IC Element - 75451	62-600 260
IC 47	IC Element - 946	62-600 303
IC 27, 33, 34, 40	IC Element - 74193	62-600 367
IC29	IC Element - 7430	62-600 359
IC32, 35	IC Element - 7402	62-600 356
IC37	IC Element - 7440	62-600 310
IC41	IC Element - 7490N	62-600 350
IC43	IC Element - 74H04	62-600 012
IC44, 54	IC Element - 7400	62-600 355
IC46	IC Element - 74155	62-600 271
IC50	IC Element - 7473	62-600 362
IC53	IC Element - 962	62-600 300
IC17, 18, 24, 30, 36	IC Element - 7404N	62-600 013
Y1	Crystal	66-481 592
A1	Amplifier, 2505	62-600 219
A2	Amplifier, A2007	62-600 235
A3, A4	Amplifier, μA710C	62-600 190
A5	Amplifier, 2525	62-600 204
A6	Amplifier, 3401A	78-199 966
A7	Amplifier, 2605	62-600 203
CR1-CR8	Diode Array, CA3039	62-600 091
CR9	Diode, 1N938	66-300 938
CR10, 11, 17	Diode, 1N5711	66-981 101
CR12	Diode, 1N4742	66-304 742
CR13	Diode, 1N4735	66-304 735
CR14, 15, 16	Diode, 1N914	66-304 148
R1, R2	Res. F.C. 10 K, 1/4 W, 5%	32-301 510
R4, 119, 122, 123	Res. F.C. 1 K, 1/4, 5%	32-301 410
R13	Res. F.C., 47 Ω, 1/4 W, 5%	32-301 247
R19	Res. F.C., 51 K, 1/4 W, 5%	32-301 551
R16, 20, 23, 41, 118, 120, 124	Res, F.C., 5.6 K, 1/4 W, 5%	32-301 456
R127, 128, R131, 134	Res., F.C., 510 Ω, 1/4 W, 5%	32-301 351
R93	Res., F.C., 15 K, 1/4 W, 5%	32-301 515
R97	Res., F.C., 10 Ω, 1/4, 5%	32-301 210

Schematic Reference	Description	Varian Part No.
R103	Res., F.C., 8.2 K, 1/4 W, 5%	32-301 482
R107,R121	Res., F.C., 470 Ω, 1/4 W, 5%	32-301 347
R87	Res, F.C., 200 Ω, 1/4 W, 5%	32-301 320
R89	Res. F.C., 560 Ω, 1/4 W, 5%	32-301 356
R129	Res. F.C., 220 Ω, 1/4 W, 5%	32-301 322
R15,R40	Res. F.C., 39 K, 1/4 W, 5%	32-301 539
R10,110	Res. MF, 2 K, 1/4 W, 1%	31-224 200
R14	Res. MF, 453 Ω, 1/4 W, 1%	31-223 453
R55	Res. MF, 6.98 K, 1/4 W, 1%	31-224 698
R17	Res. MF, 4.42 K, 1/4 W, 1%	31-224 442
R30	Res. MC, 200 Ω, 1/4 W, 1%	31-223 200
R44, 135	Res. MC, 16.2 K, 1/4 W, 1%	31-225 162
R45	Res. MC, 28 K, 1/4 W, 1%	31-225 230
R46,83	Res. MC, 5.9 K, 1/4 W, 1%	31-224 590
R96	Res. MC, 110 K, 1/4 W, 1%	31-226 110
R31	Res. MC, 1.4 K, 1/4 W, 1%	31-224 140
R42	Res. MC, 27.4 K, 1/4 W, 1%	31-225 274
R47	Res. MC, 13.7 K, 1/4 W, 1%	31-225 137
R49,R136	Res. MC, 8.45 K, 1/4 W, 1%	31-224 845
R22,50	Res. MC, 14 K, 1/4 W, 1%	31-225 140
R51	Res. MC, 3.01 K, 1/4 W, 1%	31-224 301
R54	Res. MC, 4.22 K, 1/4 W, 1%	31-224 422
R56	Res. MC, 1.47 K, 1/4 W, 1%	31-224 147
R59	Res. MC, 2.15 K, 1/4 W, 1%	31-224 215
R60	Res. MC, 3.48 K, 1/4 W, 1%	31-224 348
R61,68,91	Res. MC, 750 Ω, 1/4 W, 1%	31-223 750
R7,64,108,112	Res. MC, 1 K, 1/4 W, 1%	31-224 100
R65	Res. MC, 1.78 K, 1/4 W, 1%	31-224 178
R66	Res. MC, 383 Ω, 1/4 W, 1%	31-223 383
R72	Res. MC, 205 Ω, 1/4 W, 1%	31-223 205
R74	Res. MC, 348 Ω, 1/4 W, 1%	31-223 348
R80,82	Res. MC, 4.99 K, 1/4 W, 1%	31-224 499
R90	Res. MC, 26.1 K, 1/4 W, 1%	31-225 261
R92	Res. MC, 39.2 Ω, 1/4 W, 1%	31-223 392
R95	Res. MC, 261 Ω, 1/4 W, 1%	31-223 261
R130	Res. MC, 10 K, 1/4 W, 1%	31-225 100
R113	Res. MC, 5.62 K, 1/4 W, 1%	31-224 562
R88	Res. MC, 17.8 Ω, 1/4 W, 1%	31-222 178
R81	Res. MF, 506 Ω, 1/4 W, 1%	31-223 806
R70	Res. MF, 562 Ω, 1/2 W, 1%	31-614 654
R71	Res. MF, 909 Ω, 1/2 W, 1%	31-614 653
R109	Res. MF, 499 Ω, 1/2 W, 1%	31-614 655
R53	Res. MF, 32 K, .10%	31-239 053
R58	Res. MF, 16 K, .10%	31-239 052
R63	Res. MF, 8 K, .01%	31-239 051
R69	Res. MF, 4 K, .10%	31-239 050
R75,R76	Res. MF, 2 K, .10%	31-239 059

Schematic Reference	Description	Varian Part No.
R98,102,105		
106	Res. MF, 50 K, 1%	31-239 058
R105	Res. MF, 50 K, 1%	31-239 058
R6	Res. MF, 10.5 K, 1%	31-239 057
R77	Res. MF, 2 K, 1%	31-239 031
R3	Res. MF, 10 K, 1%	31-239 033
R18,43	Res. MF, 128 K, .1%	31-613 344
R21,48	Res. MF, 64 K, .1%	31-613 343
R52	Res. MF, 6.81 K, .1%	31-613 342
R57	Res. MF, 3.48 K, .1%	31-613 345
R62	Res. MF, 1.74 K, .1%	31-613 346
R24	Res. MF, 32 K, .1%	31-613 348
R5,R78,25,78		
101,104	Res. VAR, W.W, 1 K	37-577 311
R8	Res. VAR. W.W., 50 Ω	37-577 308
R67,R73	Res. VAR. W.W., 200 Ω	37-577 310
R79,R99	Res. VAR. W.W., 50 K	37-577 315
R85	Res. VAR. W.W., 20 K	37-577 314
Q1	Transistor, 2N3906	62-903 906
Q2	Transistor, 2N3904	62-903 904
Q3,Q4	Transistor, Fet, U1897E	62-798 125
C1-19,23,25-		
29,32-37,41,42,46,		
51-53	Cap. Cer, 1 μf, 200 V, 10%	41-228 009
C22	Cap. Cer, 1000 pf, 100 V, 5%	41-159 599
C30,C31	Cap. Mylar, .005 μf, 100 V, 1/2%	41-718 754
C38,C55	Cap. Cer, 5 pf, 500 V, 10%	41-159 505
C40,C54	Cap. Cer, 20 pf, 500 V, 5%	41-159 573
C43,45,49	Cap. Elect, 100 μf, 25 V	41-506 258
C44,50	Cap. Elect, 25 μf, 25 V	41-506 255
C47	Cap. Cer, 130 pf, 500 V, 5%	41-159 566
C48	Cap. Cer, .1 μf, 25 V, 20%	41-206 993
JPR	Wire, Bus, Bare #24 AWG	81-099 924
JPR2	Wire, Bus, Bare #24 AWG	81-099 924
JPR4	Wire, Insul. Blk #24 AWG	81-293 700
JPR5(A-B)	Wire, Bus, Bare #24 AWG	81-099 924
JPR6	Wire, Insul, Red #24 AWG	81-293 702
JPR9	Wire, Bus, Bare #24 AWG	81-099 924
JPR10	Wire, Bus, Bare #24 AWG	81-099 924