BUFFER INTERLACE CONTROLLER

an option for the

Varian Data Machines

Computer Systems

Specifications are subject to change without notice.
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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1
GENERAL DESCRIPTION

The Buffer Interlace Controller (BIC) is a special-purpose hardware option for use with Varian computer systems. This manual is divided into six sections:

- Features and specifications
- Installation and interconnection
- Operation
- Theory of operation
- Maintenance
- Mnemonics list

Volume 2 of this manual is assembled when the hardware is shipped and contains engineering documents such as logic diagrams, parts list, and installation drawings.

There are two versions of the BIC available. One version (without key bits) is for systems that do not have the memory map option and the other version (with key bits) is for systems that do have the memory map option.

The function of the BIC is to free the processor to perform other program functions during block word transfers between memory and peripheral controllers. Cycle-stealing trap requests inhibit the processing of a stored program for only the memory cycle required to transfer one word of data between memory and a peripheral controller. Operation register contents are not changed by the transfer, thus freeing the processor to execute an instruction from the stored program between successive data word transfers.

The BIC will perform DMA transfers at the peripheral device rate up to a maximum rate defined as follows:

$$R_{max} = \frac{1}{\frac{1}{R_{CPU\ max}} + T_{IUCX}}$$

where: R_{max} is the maximum rate through a BIC (words/second)
R_{CPU} is the maximum DMA rate for the processor (words/second)
T_{IUCX} is the period of interrupt clock (seconds)

As an example, the maximum DMA rate for a Varian 70 series computer with core memory and a 990 nanosecond interrupt clock period is 361,800 words/second. The maximum rate through the BIC is then:

$$R_{max} = \frac{1}{\frac{1}{361{,}800} + (990 \times 10^{-9})} = 266{,}383 \text{ words/second}$$

The BIC monitors trap requests initiated by the peripheral controllers.

Up to ten peripheral controllers can be connected to one BIC. Using standard I/O device addressing, a computer system can include up to four BICs.

The BIC is considered to be an I/O controller. Priorities for optional controllers having trap or interrupt capabilities are established by the order of their placement in the priority chain. The BIC is a system priority device; however the peripheral devices connected to it have no priority of their own.

Table 1-1 lists the BIC specifications.

Table 1-1. BIC Specifications

Parameter	Description
Organization	Contains input receivers and output drivers, two 16-bit address registers, a 4-bit key register, and a sequence control circuit
Control capability	Up to ten peripheral controllers
I/O transfer rate	Synchronized to peripheral device rate
I/O signal limits (rise/fall)	Minimum 10 nanoseconds; maximum 100 nanoseconds
Logic levels (internal)	High = +2.4 to +5.0V dc Low = 0 to +0.4V dc
Logic levels (I/O bus)	High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Size	Contained on one 7-3/4-by 12-inch (19.7 x 30.3 cm) printed-circuit board

(continued)

Table 1-1. BIC Specifications *(continued)*

Parameter	Description
Interconnection	Interfaces with I/O cable through backplane connector; connects to peripheral controllers through the backplane connector or through a cable
Connectors	One 122-terminal card-edge connector (mates with female connector at backplane) and two 44-terminal card-edge connectors (each mates with a 44-terminal connector on B cable for special configurations)
Power	+5V dc at 0.6A
Operating environment	0 to 50 degrees C; 10 to 90 percent relative humidity without condensation

SECTION 2
INSTALLATION

The BIC has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. If damage exists:

- Notify the transportation company
- Notify Varian Data Machines
- Save all packing material

2.1 PHYSICAL DESCRIPTION

The BIC circuits are contained on a single printed-circuit (PC) board (p/n 44P0689). As illustrated in figure 2-1, the board contains three connectors P1, J1, and J2. Connectors J1 and J2 are wired in parallel and contain the peripheral control lines. Connector P1 also contains the same peripheral control lines as well as all I/O bus control signals for the BIC. Connectors J1 and J2 are used for special configurations.

2.2 INTERCONNECTION

When two or more BIC controllers are installed in the same chassis, the B cable signals are connected only to the controller or controllers with which each BIC communicates. There are no B cable signals between BICs. If the BIC and the peripheral controllers are installed in different chassis, the interconnection is made through the J1 and J2 connectors. Figure 2-2 illustrates BIC/peripheral interconnections.

2.3 INTERFACE DATA

All BIC input/output signals utilize receiver/driver stages to buffer internal circuits and external lines. The BIC interfaces with the computer via the "—I" signal lines and with peripheral controllers via the "—B" signal lines listed in table 2-1. The corresponding pin number of circuit card edge connector P1 follows each signal mnemonic (see logic diagram 91C0459). Refer to section 6 for definitions of the mnemonics.

Table 2-1. BIC Inputs and Outputs

INPUTS				OUTPUTS			
BCDX-B	52	EB10-I	16	DCEX-B	56	EB12-I	18
BIMES-I	93	EB11-I	17	DESX-B	60	EB13-I	19
CDCX-B	54	EB12-I	18	EB00-I	2	EB14-I	20
DRYX-I	29	EB13-I	19	EB01-I	4,68,69	EB15-I	21
EB00-I	2	EB14-I	20	EB02-I	6,71,72	INTX-	75
EB01-I	4,65	EB15-I	21	EB03-I	8	IOK1-I	109
EB02-I	6,70	FRYX-I	27	EB04-I	10	IOK2-I	110
EB03-I	8	IUAX-I	44	EB05-I	11	IOK3-I	112
EB04-I	10	IUCX-I	45	EB06-I	12	IOK4-I	113
EB05-I	11	PRMX-I	37	EB07-I	13	PRNX-I	42
EB06-I	12	SYRT-I	43	EB08-I	14	SERX-I	31
EB07-I	13	TROX-B	50	EB09-I	15	TAKX-B	58
EB08-I	14	TRQX-B	49	EB10-I	16	TPIX-I	33
EB09-I	15			EB11-I	17	TPOX-I	35

Many peripheral controllers, under software control, can transfer data either by programmed I O or via BIC control. Controllers for peripherals such as discs and drums usually are not able to transfer data via programmed I/O due to their high transfer rates. Figure 2-3 shows a computer system with peripheral controllers that operate with and without BIC. Figure 2-4 is typical interface logic.

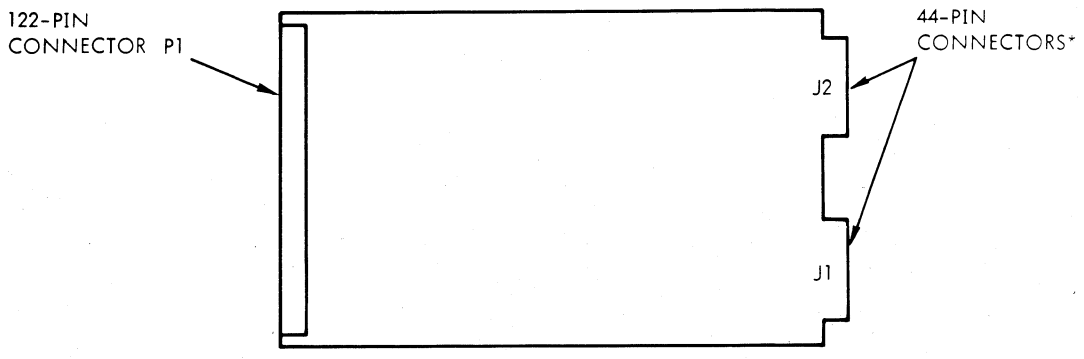

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Figure 2-1. BIC Board (Component Side)

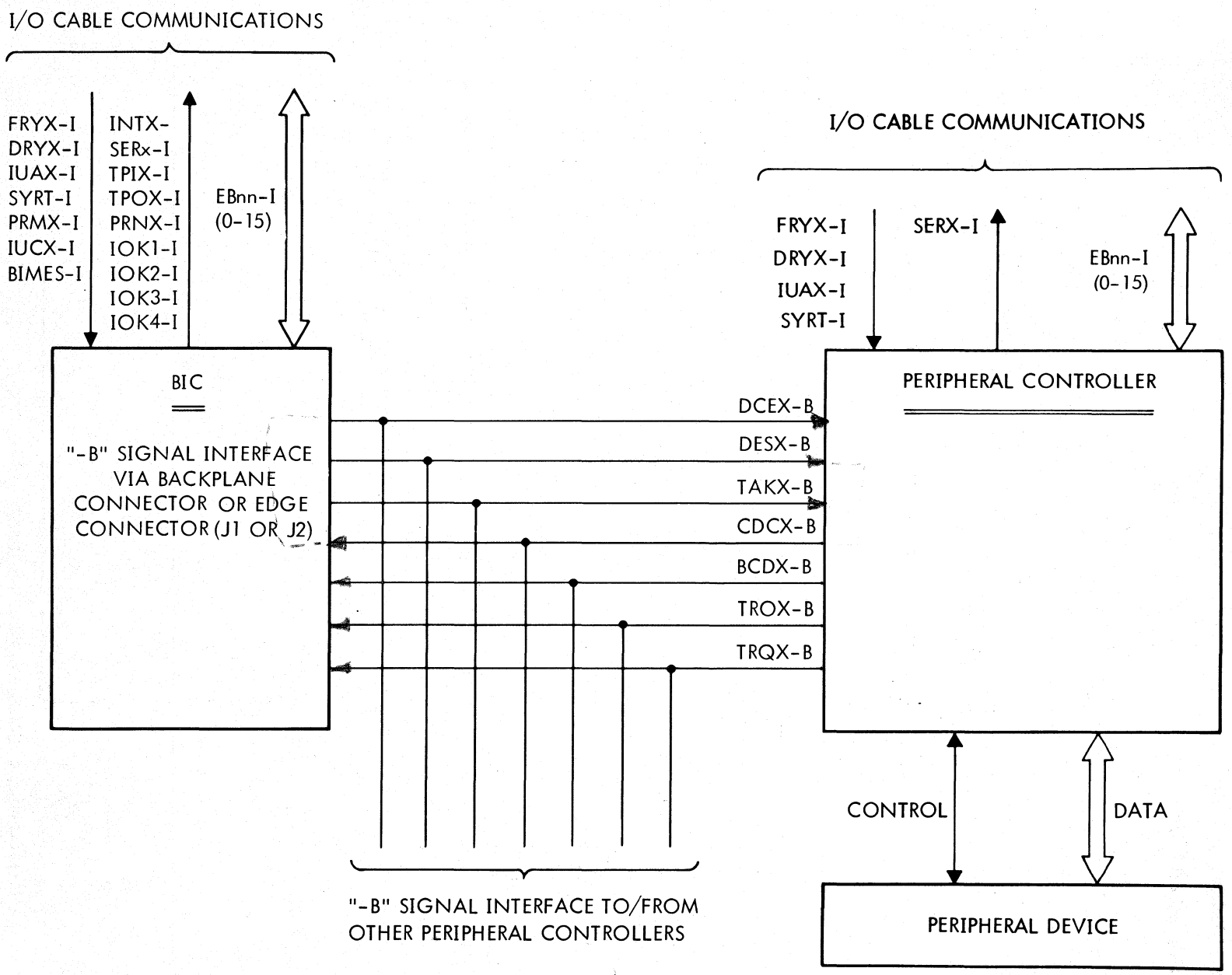

Figure 2-2. BIC/Peripheral Controller Interface

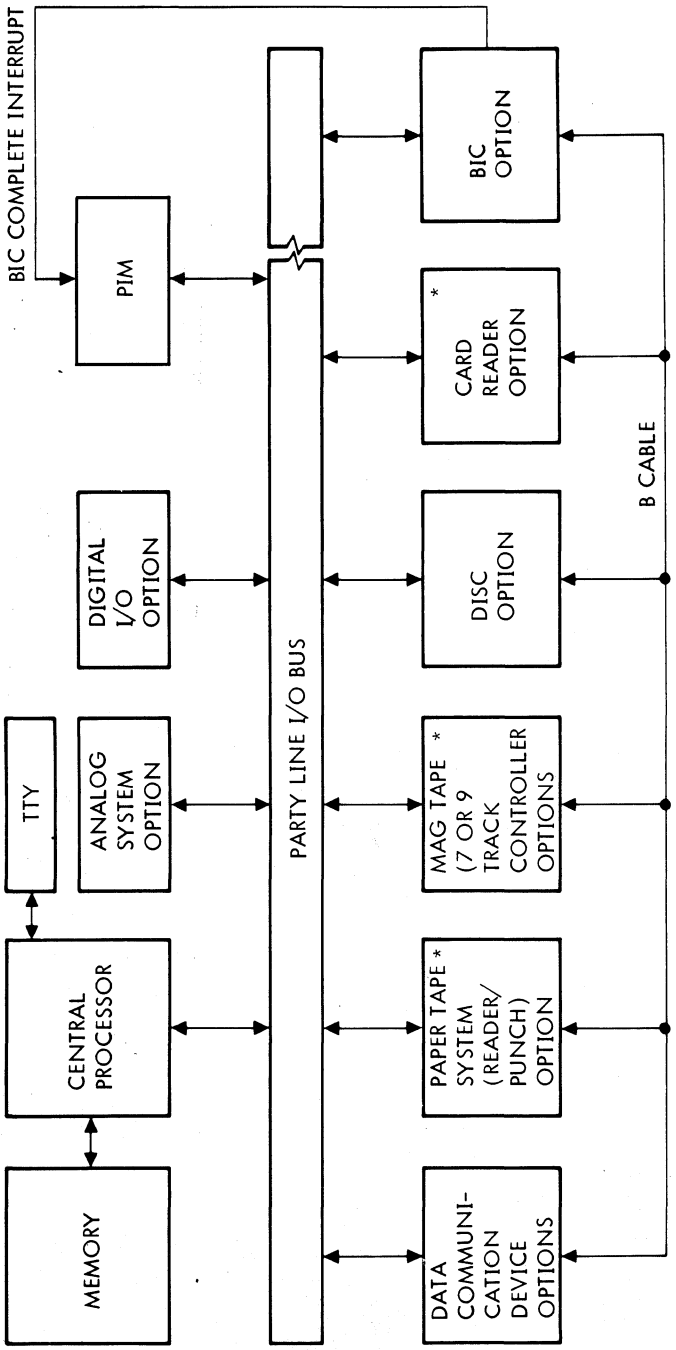

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Figure 2-3. Interface for Peripheral Devices with and

INSTALLATION

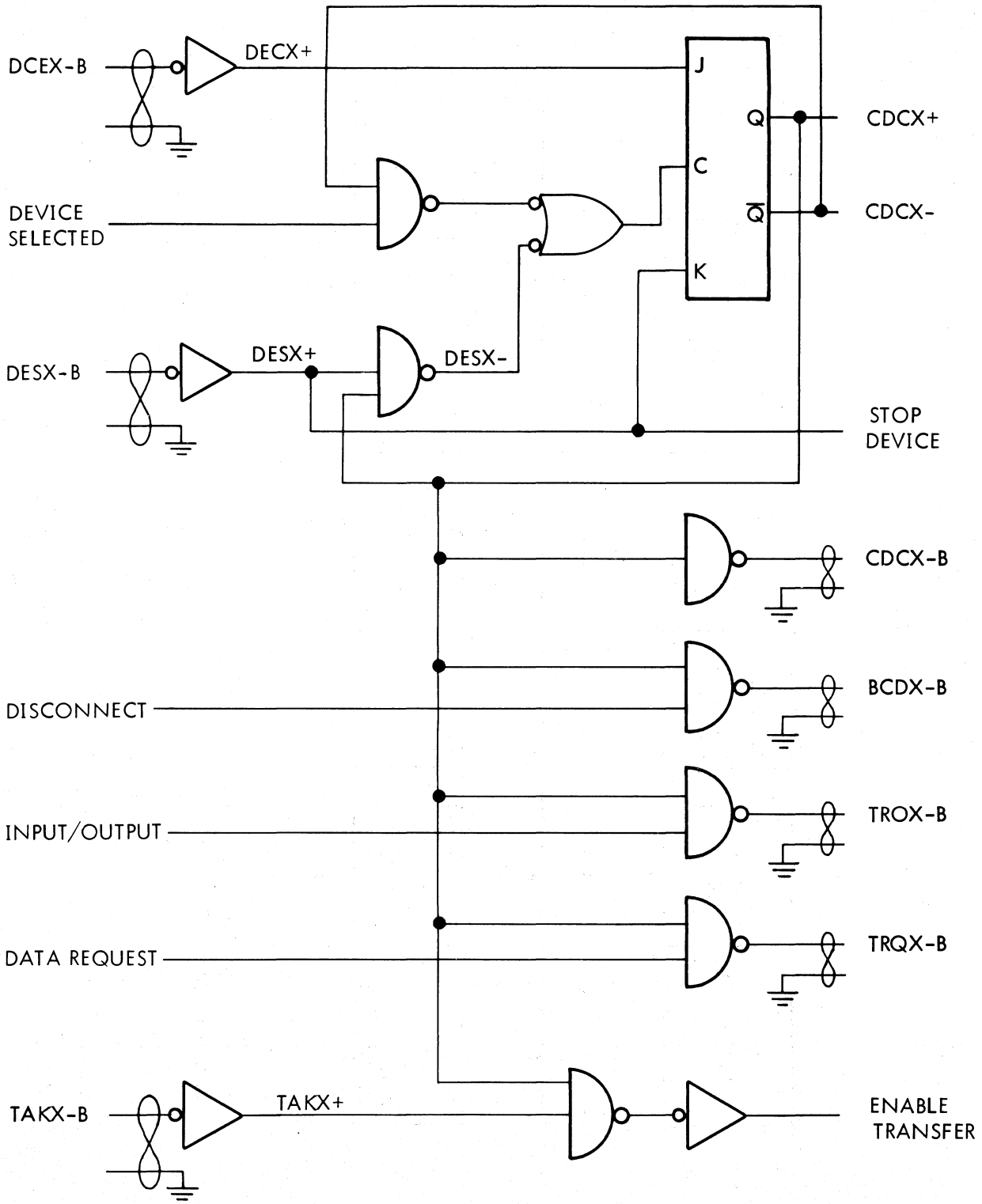

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Figure 2-4. Typical B Cable Interface Logic

SECTION 3
OPERATION

The BIC has no operating controls or indicators. It operates under program control.

3.1 I/O INSTRUCTIONS

The BIC responds to the instructions listed in table 3-1. Two device addresses are assigned to each BIC to differentiate functions directed by the I/O instruction. Addresses 020 through 027 are reserved for BICs. Address/instruction codes in table 3-1 are for the first BIC in a system. If additional BICs are installed, the addresses shown should be incremented by two for each additional BIC (i.e., second BIC addresses should be 022 and 023).

Table 3-1. I/O Instructions

Mnemonics	Octal Code	Description
		External Control
EXC 020	100020	Activate BIC
EXC 021	100021	Initialize
EXC 0321	100321	Enable loading of key bits
		Transfer
OAR 020	103120	Load initial register from A
OBR 020	103220	Load initial register from B
OME 020	103020	Load initial register from memory
OAR 021	103121	Load final register from A
OBR 021	103221	Load final register from B
OME 021	103021	Load final register from memory
INA 020	102120	Read initial register into A
INB 020	102220	Read initial register into B
IME 020	102020	Read initial register into memory
CIA 020	102520	Read initial register into cleared A
CIB 020	102620	Read initial register into cleared B
		Sense
SEN 020	101020	Sense BIC not busy
SEN 021	101021	Sense abnormal device stop
SEN 0121	101121	Senses if BIC has been stopped due to a memory-map error

3.2 PROGRAMMING CONSIDERATIONS

The user writes the programs that use the BIC. When preparing a program for use with the BIC, the programmer first initializes then senses the status of the BIC and the selected peripheral controller. After a not-busy response is received from both the BIC and the peripheral controller, the BIC address registers are loaded with the initial and final memory addresses of the block of data to be transferred, a BIC activate enable instruction is placed on the I/O cable, and the transfer is started. Although the program requires loops for use with sense instructions and to handle abnormal conditions, transfer of the data block is accomplished by the BIC without further program instructions.

The key bit register (for memory map option) is loaded by first issuing the "Enable (loading of) Key Bit Register" instruction (0100321) followed by one of the "Load Final Register" instructions (0103021, 0103121, 0103221).

3.3 SAMPLE PROGRAM

Table 3-2 shows a typical service routine for the BIC, a Teletype paper tape punch operation under BIC control. Using DAS symbols with corresponding machine language

Table 3-2. Typical Service Routine

Memory Location	Octal Code	Label	Operation	Variable Field	Comments
001000			,ORG	,01000	
001000	101020	BIC0	,SEN	,020,BIC1	CK BIC NOT BUSY
001001	001007 R				
001002	100401		,EXC	,0401	INIT TTY
001003	100021		,EXC	,021	INIT BIC
001004	005000		,NOP	,	
001005	001000		,JMP	,*-3	

(continued)

OPERATION

Table 3-2. Typical Service Routine *(continued)*

Memory Location	Octal Code	Label	Operation	Variable Field	Comments
001006	001002 R				
001007	101101	BIC1	,SEN	,0101,BIC2	CK TTY WRITE READY
001010	001014 R				
001011	005000		,NOP	,	
001012	001000		,JMP	,*-3	
001013	001007 R				
001014	103120	BIC2	,OAR	,020	SET BIC I REG
001015	103221		,OBR	,021	SET BIC F REG
001016	100020		,EXC	,020	ACTIVATE BIC
001017	100101		,EXC	,0101	CONNECT WRITE REG
001020	101020		,SEN	,020,BIC3	CK BIC NOT BUSY
001021	001025 R				
001022	005000		,NOP	,	
001023	001000		,JMP	,*-3	
001024	001020 R				
001025	101021	BIC3	,SEN	,021,BIC5	CK ABN STOP
001026	001032 R				
001027	007400		,ROF	,	
001030	102520	BIC4	,CIA	,020	INPUT BIC I REG
001031	000000		,HLT	,	
001032	007401	BIC5	,SOF	,	SET ABN FLAG
001033	001000		,JMP	,BIC4	
001034	001030 R				
	000000		,END	,	

octal codes, the program covers memory locations 01000 through 01034.

Once the program is loaded, the operator must insert the initial punch buffer address into the A register and the final address into the B register for each run. When started, the program will:

a. initialize the BIC and Teletype punch

b. initiate the data transfer

c. read the contents of the BIC initial register into the A register at the completion of the transfer

d. set the overflow indicator if the termination was abnormal

e. halt

The punch buffer must contain only ASCII characters. The first character is 0222 (punch on) and the last is 0224 (punch off).

SECTION 4
THEORY OF OPERATION

The BIC is functionally divided into address registers and a sequence control circuit (figure 4-1). A functional description of these circuits is provided in the following paragraphs.

4.1 ADDRESS REGISTERS

The two address registers contain the memory locations of output or input data, depending on the I/O instruction. The initial register stores the address of the first input or output word, and is incremented during each data-word transfer. When the block transfer is complete, the initial register contains the address + 1 of the last data word to be transferred.

The final register stores the address of the last word to be transferred. Unless the peripheral device is abnormally stopped, the address in the final register will be one less than the address in the initial register when the block transfer is complete. When the initial and final registers reach comparison, the block word transfer is complete.

The key-bit register stores the four key bits that are used with the memory map. The key-bit register is not used on systems without the memory map. The enable instruction sets a flip-flop which directs the data being transferred by a load (of final register) instruction, into the key-bit register. The flip-flop is reset when the transfer is complete.

4.2 SEQUENCE CONTROL

The sequence control circuit generates the control signals which coordinate address and data transfer between the processor, BIC, and the peripheral controllers. The data are not routed through the BIC but are directly transferred between the peripheral controller and memory.

Under program control, the processor senses that the BIC is not busy and prepares the BIC to receive the initial and final data addresses. The processor then senses that the selected peripheral controller is not busy and loads the initial and final registers and the key register. The BIC is then activated and the peripheral controller is started. The BIC then assumes control of the data transmission, allowing the processor operational registers to be used by the program for other functions.

Data transfer is accomplished between memory and the peripheral controller via the I/O bus. The BIC counts the words transferred and when the data block transfer is complete, disconnects the peripheral controller and assumes a not-busy state. Data transfer may also be terminated upon request from the peripheral controller.

4.3 OPERATING SEQUENCE

The following paragraphs describe the sequence of operations of the BIC. Refer to the block diagram (figure 4-1), the timing diagram (figure 4-2), and the logic diagram 91C0459 in volume 2.

4.3.1 Initial Conditions

The processor senses the BIC for a not-busy condition. The sense instruction places the BIC device address and a function code on the I/O bus. The BIC responds with a low SERX-I if it is not busy (CDCX-B low). The processor then executes the initialize instruction which generates a low INIT- which prepares BIC for receiving the initial and final addresses of the block data to be transferred.

The initial register is loaded from the I/O bus when data ready DRYX—I returns high and LIxx— is low.

The final register is loaded from the I/O bus when DRYX—I returns high, and LFRX + is high.

4.3.2 Device Selection

The processor executes the activate BIC instruction which causes DCEX-B to go low. This signal is sent to all peripheral controllers connected to the BIC. The processor then executes an instruction to select a peripheral device. This instruction with DCEX-B low, connects the selected device to the BIC and starts the device.

The connected peripheral controller sends a low CDCX-B to the BIC causing DCEX-B to go high, thus disabling the selection of any other peripheral controllers. When CDCX-B goes low, the connected peripheral controller also selects the state of TROX-B. When data is to be transferred to memory, a high TROX-B is sent. If data is to be transferred to memory, a low TROX-B is sent.

4.3.3 Data Address

When the connected peripheral controller is ready for the data transfer, it sends a low TRQX-B to the BIC. The BIC then sends a TPIX-I or low TPOX-I to the processor, depending on the state of TROX-B.

When the processor is ready for the data transfer, it sends a low IUAX—I to the BIC. IUAX—I going low generates a low TAKX—B which is sent to the peripheral controller to initiate the transfer. The BIC then causes OIRX + to go high which gates the memory address, that is in the initial register plus the key bits onto the I/O bus. The connected peripheral controller is thus enabled. FRYX—I, from the processor, going high terminates the address phase of the BIC. FRYX—I going high causes CLEX— to go high, which

THEORY OF OPERATION

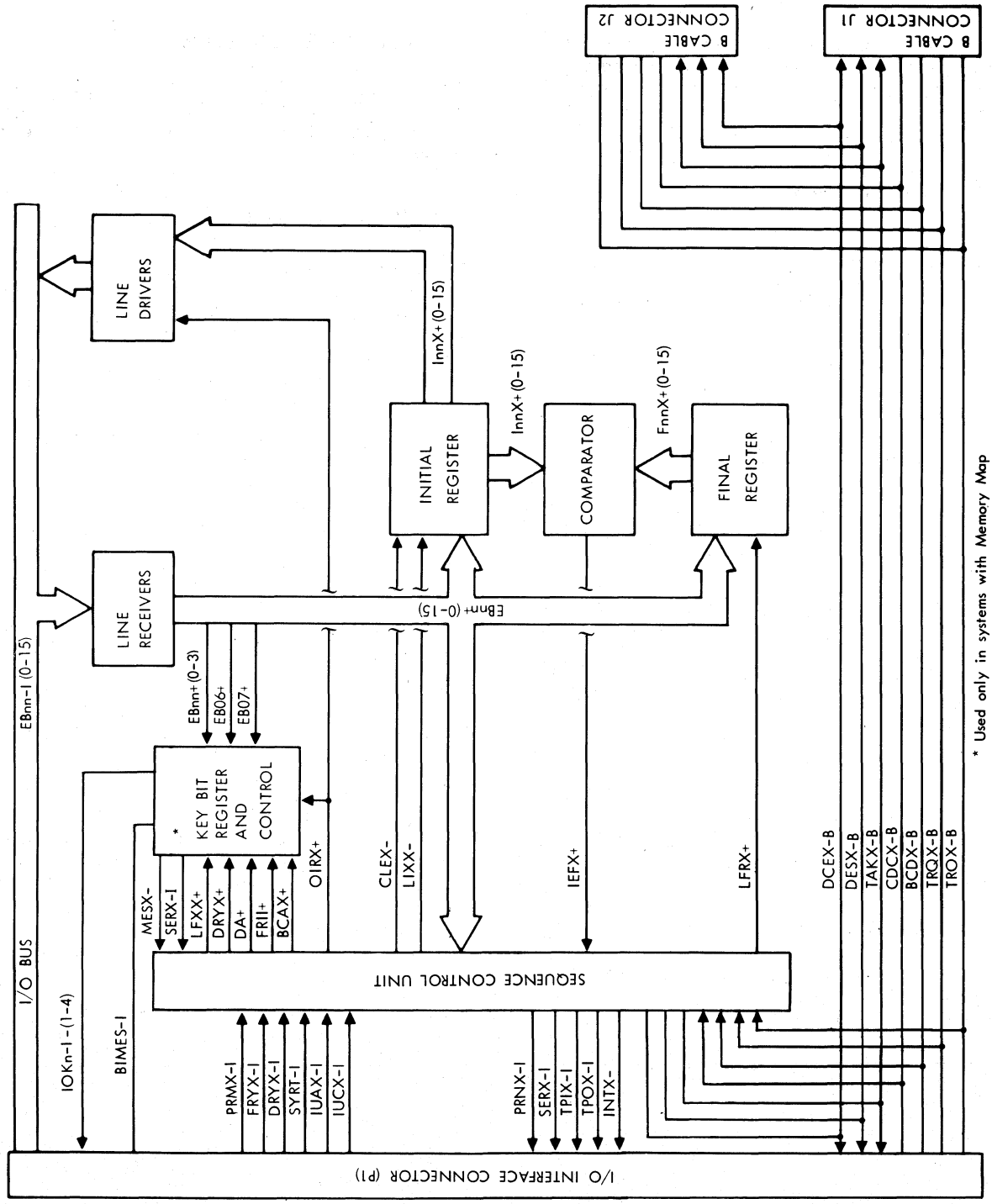

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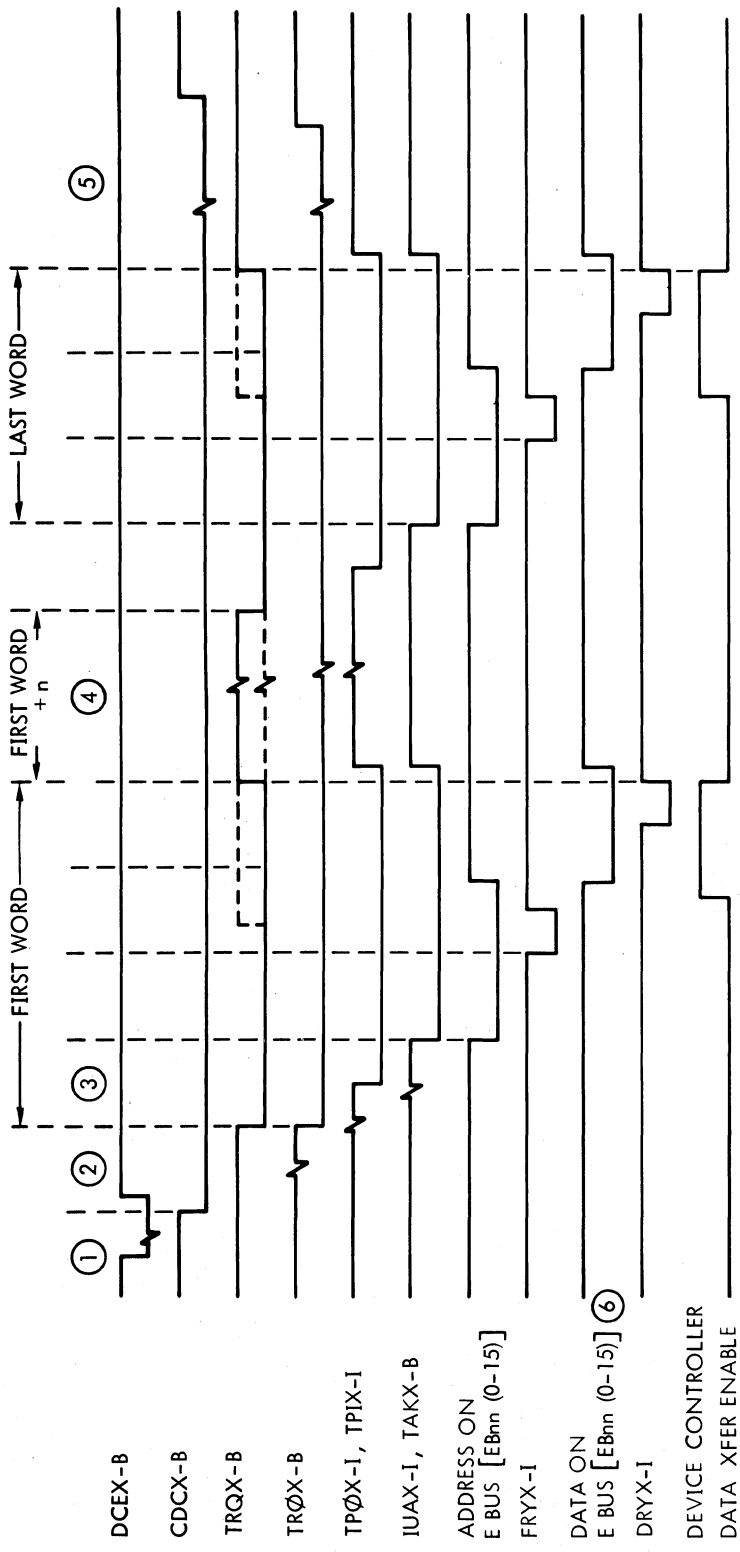
Figure 4-1. BIC Block Diagram



NOTES:

① TIMING REQUIRED TO ISSUE THE COMMAND TO CONNECT THE DEVICE.

② TIME REQUIRED FOR DEVICE TO REQUEST FIRST DATA TRANSFER AFTER STARTING.

③ TIME REQUIRED TO SERVICE CURRENT AND/OR HIGHER PRIORITY REQUESTS FOR I/O ACCESSES.

④ SIGNAL TRQX-B MAY BE BROUGHT LOW (TRUE) AGAIN, AS EARLY AS THE TRAILING EDGE OF DRYX-I. HOWEVER, SIGNAL TRQX-B MUST HAVE BEEN HIGH FOR AT LEAST 50 NANOSECONDS BEFORE GOING LOW.

⑤ END OF DATA BLOCK. SIGNAL CDCX MAY REMAIN HIGH BETWEEN BLOCKS.

⑥ INCLUDES KEY BITS IF PRESENT [IOKn-I (0-3)].

⑦ FOR DMA TIMING REFER TO THE APPLICABLE SYSTEM HANDBOOK.

Figure 4-2. BIC Trap Sequence Timing

causes the initial register to be incremented to the next memory address.

4.3.4 Data Transfer

The data transfer may be an output from or an input to the processor. For output, the processor places the data on the I/O bus, and the data is strobed into the peripheral controller by DRYX-I going high. For input, the peripheral controller places the data on the I/O bus when FRYX-I goes high and removes the data when DRYX-I goes high. BIC keeps TAKX-B low until the end of the transfer when IUAX-I goes high.

4.3.5 Transfer Termination

When the contents of the initial and final registers become equal, the comparator circuit generates a high IEFX—. This creates a low DESX—B which is sent to the peripheral controller. The peripheral controller then causes CDCX—B to go high. This causes the BIC to assume a not busy state. The transfer of data is thus terminated.

When an abnormal device stop occurs, the peripheral controller terminates the transfer without regard to the contents of the initial and final registers. The peripheral controller generates a low BCDX—B. This causes a low DESX—B to be sent to the peripheral controller. The peripheral controller responds with a high CDCX—B. This causes the BIC to assume a not busy state. The transfer of data is thus terminated. After an abnormal device stop, the processor can read the contents of the initial register to determine the number of words that were transferred. The number in the initial register will be the address of the last word transferred plus one.

An abnormal device stop can occur as a result of any of the following situations: 1) the length of the data block is unknown, and the device has detected the end of the data; 2) the peripheral controller has detected an invalid operation of the device; 3) the processor has issued an instruction to stop the operation of the peripheral device.

Another abnormal stop is created when an error is detected by the memory map during a BIC operation. The error causes BIMES—I to go low. This causes a low DESX—B to be sent to the peripheral controller. The peripheral controller responds with a high CDCX—B. This causes the BIC to assume a not busy state. The transfer of data is then terminated.

SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting to troubleshoot the BIC. The Varian MAINTAIN II test program system (Test Programs Manual, 98 A 9952 06x)* contains a BIC test program used to test various phases of the BIC operation. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommended for maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit, or equivalent.

b. Multimeter, Triplett type 630 or equivalent.

c. Soldering iron, 39-watt pencil type.

d. Card extender VDM p/n 44P0540.

*The x at the end of the document number is the revision number and can be any digit 0 through 9.

5.2 CIRCUIT-COMPONENT IDENTIFICATION

All reference designations used in the logic diagram appear on the BIC board adjacent to each component. Component part numbers can be found in the parts list in volume 2.

5.3 CIRCUIT-BOARD REPAIR

If it has been determined that circuit-board repair is required, it is recommended that the Varian Data Machines customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits.

SECTION 6
MNEMONICS

Table 6-1 provides an alphabetized list of the signal mnemonics used in the BIC.

Table 6-1. Mnemonics

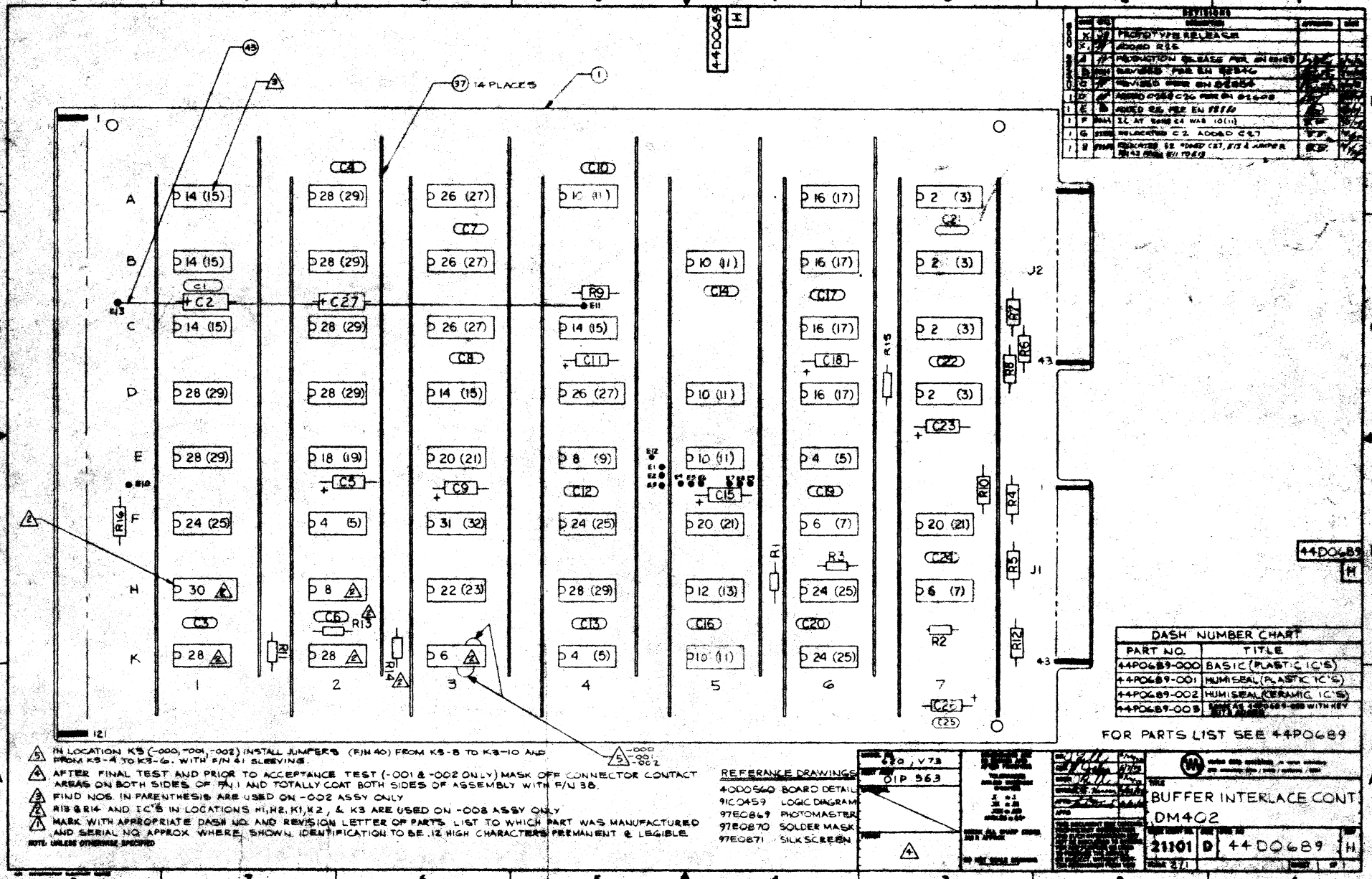
Mnemonic	Description
ACEX	Activate enable. Stores activation of BIC.
ADSX	Abnormal device stop. Stores end of data from peripheral controller.
BCAX	Buffer controller activate. Stores the activation of the BIC and the peripheral controller.
BCDX	Buffer controller deactivate. Initiates termination of data transfer by the peripheral controller.
~~BIMES~~	BIC map error stop. Stores the map error indication during a BIC operation.
CARx	Carry out. Increments the next higher position of the initial register on overflow.
CDCX	Controller device connected. Indicates that the peripheral controller to be connected is connected.
CLEX	Clock enabled. Enables the initial register to be incremented.
DA	Device address decode. Gates the device address from the I/O bus.
DCEX	Device connect enable. Enables the selection of a peripheral device.
DESX	Device stop. Stores the requirement to stop the peripheral device.
DRYX	Data ready. Indicates the I/O bus contains a word of data.
DSTX	Device stop enable. Stores the end of the data transfer.
EBii	E-bus bit. Address or function code bits from the I/O bus.
~~EKBR~~	Enable loading of key bit register. Gates the key bits into the key-bit register.
FRYX	Function ready. Indicates the I/O bus contains an address.
FiiX	Final register bit. Stores bit ii of the final address.
IEFX	Initial equals final. Indicates that the contents of the initial register is equal to the contents of the final register.
IFMX	Initial equals final memory. Clears the BIC active flip-flop when the contents of the initial register is equal to the contents of the final register.
INIT	Initialize. Resets BIC flip-flops to their initial condition.
INTX	Interrupt request. Used to request an interrupt when the block transfer is complete.
~~IOKi~~	Key-bit register output i to I/O bus.
IUAX	Interrupt acknowledge. Indicates that the processor is ready to send or receive data.
IUCX	Interrupt clock. Provides timing for servicing BIC.
IiiX	Initial register data bit. Stores bit ii of the initial address.
LFRX	Load final register. Loads data on I/O bus into final register.
LFXX	Load final. Gates the I/O bus contents into the key-bit register when EKBR is set.
LIXX	Load initial register. Loads data on I/O bus into initial register.
~~MESX~~	Map error stop. Indicates that there was a memory map error during a BIC operation.

(continued)

MNEMONICS

Table 6-1. Mnemonics *(continued)*

Mnemonic	Description
OIRX	Output initial register. Gates contents of initial register and key-bit register onto the I/O bus.
PLUP	Pullup voltage.
PRMX	Priority in. Gives priority to BIC.
PRNX	Priority out. Passes priority to next in line after BIC is serviced.
RIXX	Read initial register. Stores requirement of processor to read contents of initial register.
RTPD	Reset trap detect. Resets the trap request detection flip-flop.
SERX	Sense response. Indicates whether the BIC is busy.
SYRT	System reset. Generates initialize signal when SYSTEM RESET is pressed.
TAKX	Trap acknowledge. Indicates that the requirements for data transfer have been met.
TCOX	Trap command. Synchronizes trap request with interrupt clock.
TPDX	Trap request detect. Detects the peripheral controller request for a trap.
TPIX	Trap in. Indicates that the BIC is ready to transfer data to the processor.
TPOX	Trap out. Indicates that the BIC is ready to transfer data from the processor.
TROX	Trap out (from peripheral). Indicates the direction (in or out) of the data transfer.
TRQX	Trap request. Indicates that the peripheral controller is ready for a data transfer.



DASH NUMBER CHART	
PART NO.	TITLE
44P0689-000	BASIC (PLASTIC IC'S)
44P0689-001	HUMISEAL (PLASTIC IC'S)
44P0689-002	HUMISEAL (CERAMIC IC'S)
44P0689-003	[illegible]

FOR PARTS LIST SEE 44P0689

5 IN LOCATION K3 (-000, -001, -002) INSTALL JUMPER (P/N 40) FROM K3-8 TO K3-10 AND FROM K3-4 TO K3-6. WITH P/N 41 SLEEVING.

4 AFTER FINAL TEST AND PRIOR TO ACCEPTANCE TEST (-001 & -002 ONLY) MASK OFF CONNECTOR CONTACT AREAS ON BOTH SIDES OF P/N 1 AND TOTALLY COAT BOTH SIDES OF ASSEMBLY WITH P/N 38.

3 FIND NOS. IN PARENTHESIS ARE USED ON -002 ASSY ONLY

2 R13 & R14 AND IC'S IN LOCATIONS H1, H2, K1, K2, & K3 ARE USED ON -008 ASSY ONLY

1 MARK WITH APPROPRIATE DASH NO. AND REVISION LETTER OF PARTS LIST TO WHICH PART WAS MANUFACTURED AND SERIAL NO. APPROX WHERE SHOWN. IDENTIFICATION TO BE .12 HIGH CHARACTERS PERMANENT & LEGIBLE.

NOTE: UNLESS OTHERWISE SPECIFIED

REFERANCE DRAWINGS

44D0560	BOARD DETAIL
91C0459	LOGIC DIAGRAM
97E0869	PHOTOMASTER
97E0870	SOLDER MASK
97E0871	SILK SCREEN

430 , V73
DIP 563

TITLE
BUFFER INTERLACE CONT
DM402

21101 | D | 44D0689 | H

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4 W, 5%
2. THIS DRAWING CONSISTS OF THE FOLLOWING SHEETS: 1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, 10.0, 11.0, 12.0, 13.0

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
R 16	
C 27	
E13	

REFERENCE DRAWINGS	
BOARD DETAIL	40D0560
ARTWORK	97E0869
SOLDERMASK	97E0870
SILKSCREEN	97E0871
ASSEMBLY	44D0689

DR C. WARNER	5-29-73	
CHK R Taylor	6-7-73	
DSGN J. ZOLL	5-2-73	
ENGR T.E. Nunan	6-21-73	
APPD	6/4/73	
APPD		

varian data machines /a varian subsidiary
2722 michelson drive / irvine / california / 92664

TITLE
LOGIC DIAGRAM - DM402
BUFFER INTERLACE CONTROLLER

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0459	G

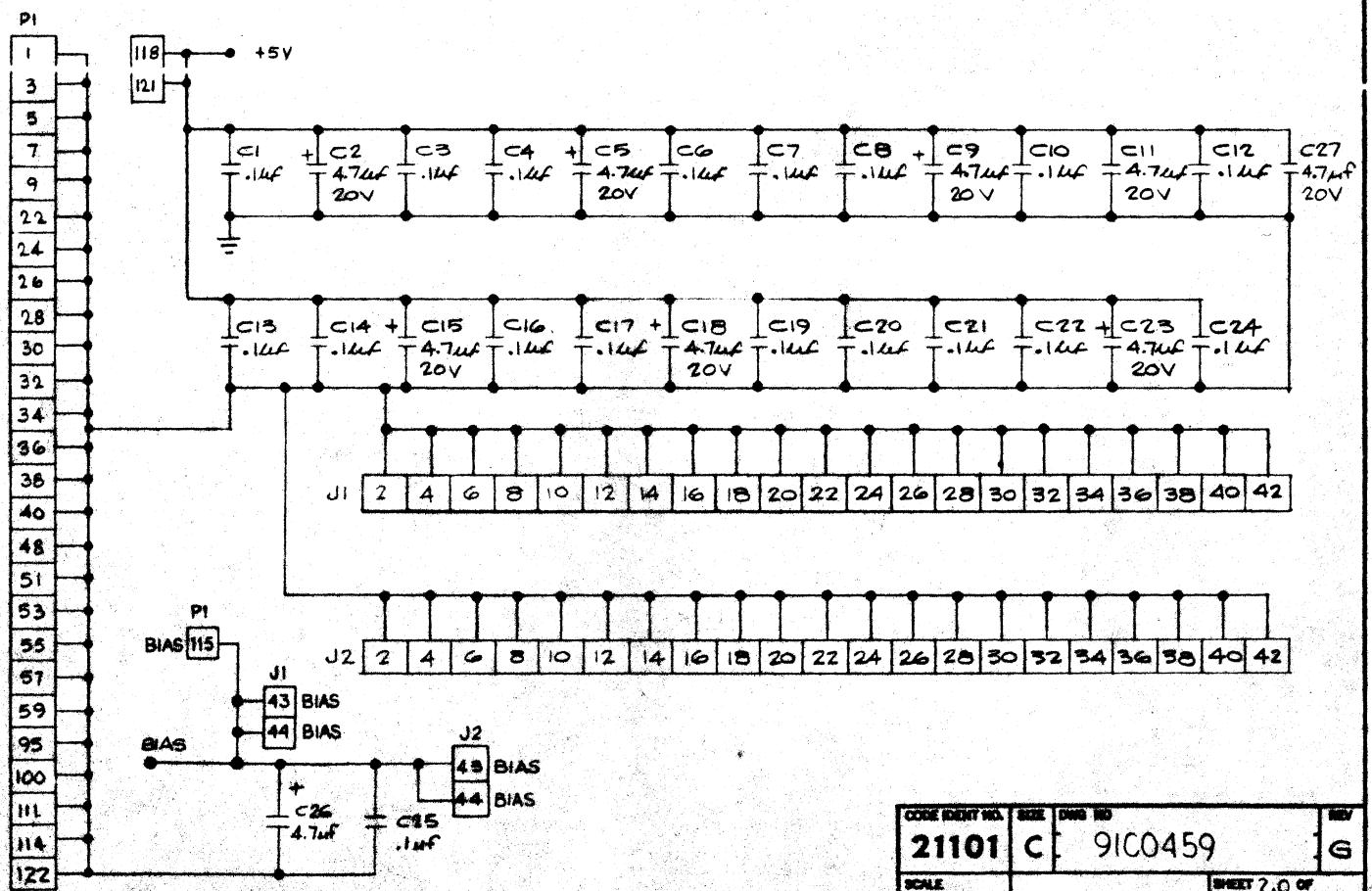
SCALE | SHEET 1.0 OF

REVISIONS					
SYSTEM	DASH	EN#	DESCRIPTION	APPROVED	DATE
	A		PRODUCTION RELEASE PER EN 82123		4/21/73
	B		REVISE PER EN 82854		9/20/73
1	C		ADDED C25 & C26 PER EN 82605		3/26/74
1	D		ADDED E16 - WAS N/U PER EN 82880		5-16-74
	—	83154	ADDED DEVICE ADDRESS BLOCK AND NOTE'S 1,2 & 3 TO SHT 5.		8/15/74
1	E	83164	F2 PIN 6 WAS TO SIGNAL TCØX+, THE IC AT C4 WAS 74H04		8/15/74
	F	83218	ADDED GND TO PINS P1-48, 100, 111 & 114 SHT 2 & 4, ADDED POWER AND GND DIST. FOR IC's TO SHT 2		8/15/74
	—	83335	SH & D ZONE C-3 E5 WAS: 7404 13; 74H04		10/4/74
	G	83345	ADDED C27 AND E13		10/4/74

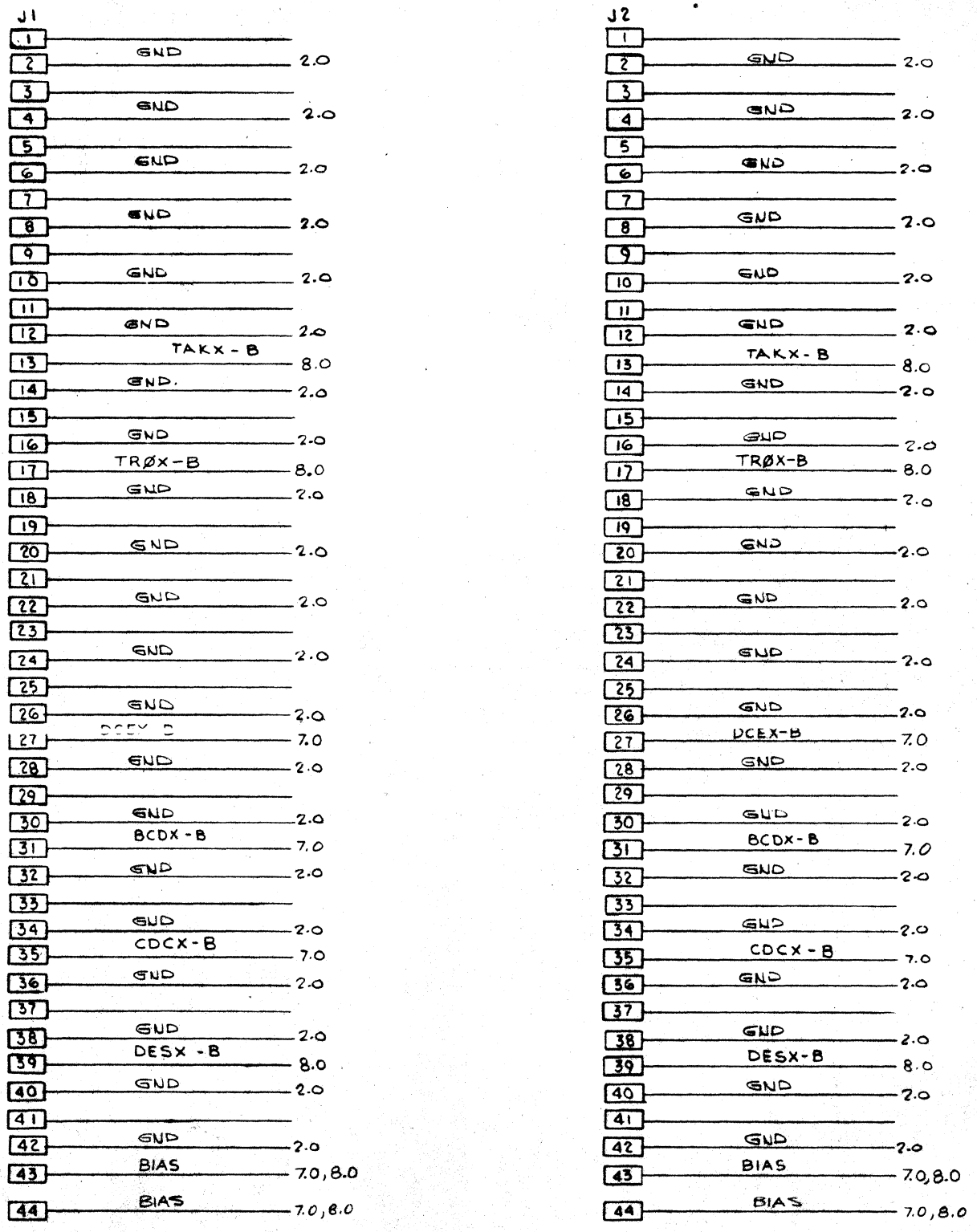
TABLE OF CONTENTS

NOTE: POWER AND GROUND DISTRIBUTION

FOR 16 PIN IC PIN 16 = +5 V PIN 8 = GND EXCEPT AS LISTED BELOW
FOR 14 PIN IC PIN 14 = +5V PIN 7 = GND EXCEPT AS LISTED BELOW
EXCEPTIONS:
I.C. AT F2, K4 AND E6 PIN 4 = +5 PIN 11 = GND
I.C. AT A7, B7, C7 AND D7 PIN 5 = +5 PIN 12 = GND



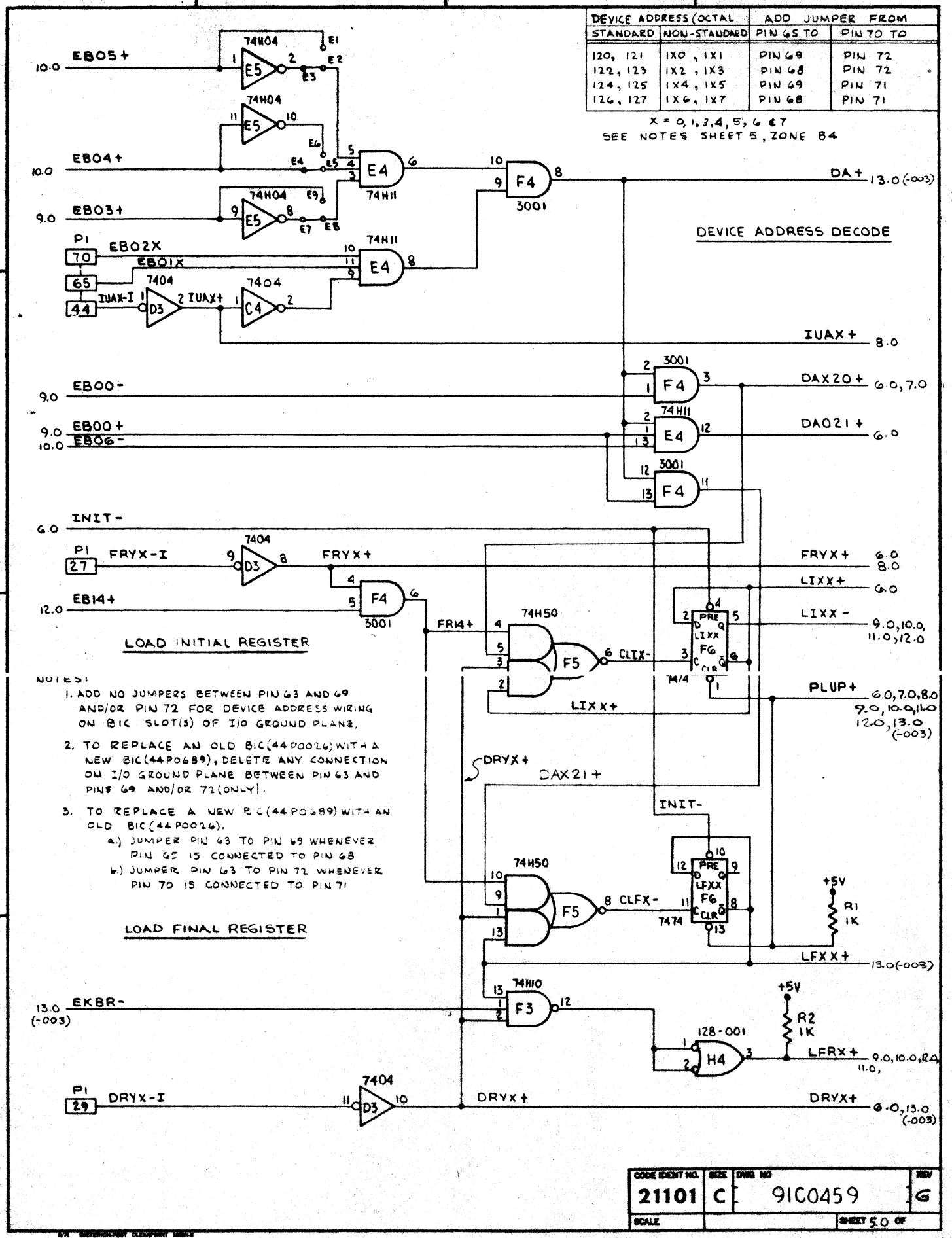
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	G
SCALE		SHEET 2.0 OF	



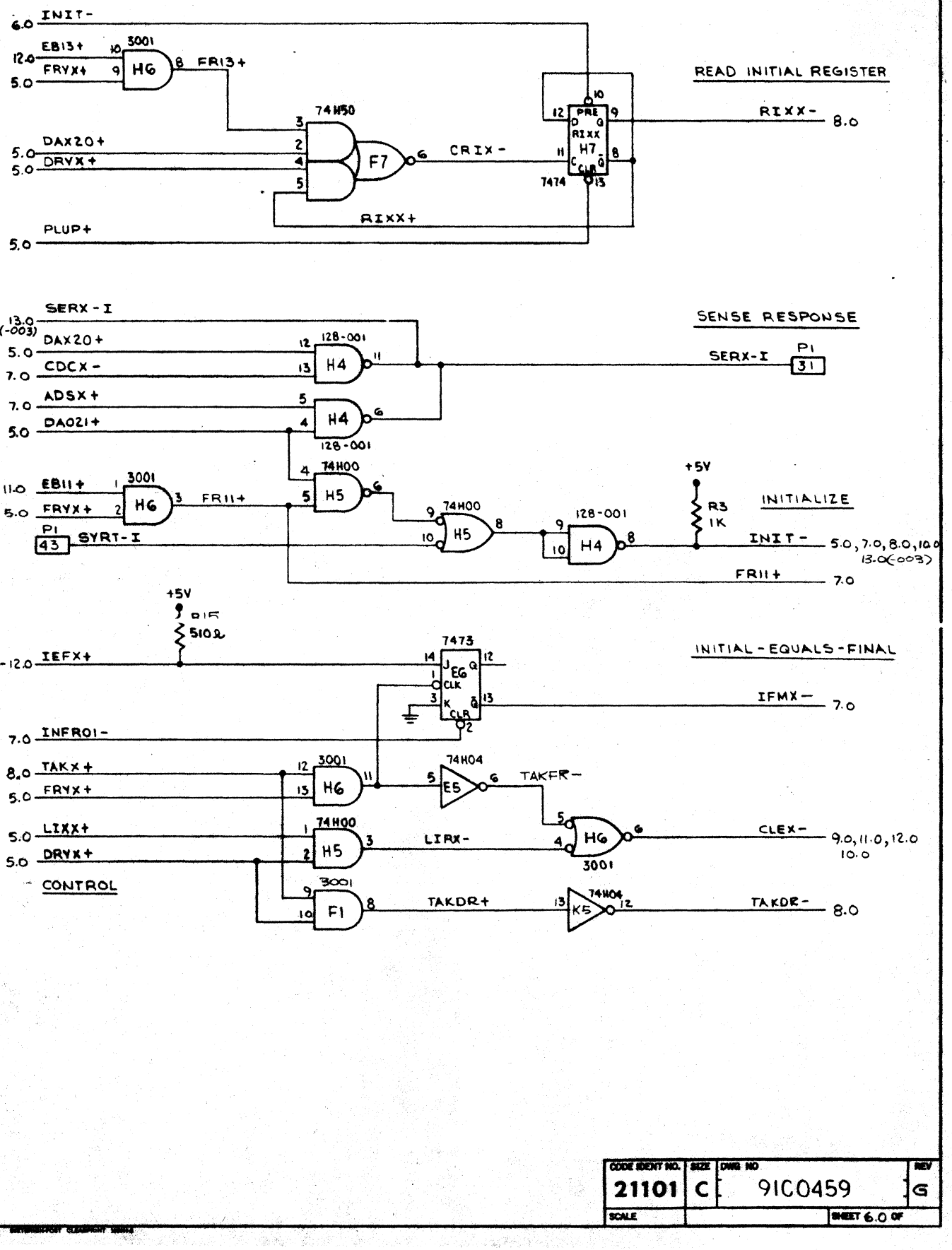
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	G
SCALE			SHEET 3.0 OF

P1											
1	GND	2.0	43	PRNX-I	8.0	84			125		
2	EB00-I	9.0	43	SYRT-I	6.0	85			126		
3	GND	2.0	44	IUAX-I	5.0	86			127		
4	EB01-I	9.0	45	IUCX-I	7.0	87			128		
5	GND	2.0	46			88			129		
6	EB02-I	9.0	47			89			130		
7	GND	2.0	48	GND	2.0	90			131		
8	EB03-I	9.0	49	TRQX-B	8.0	91			132		
9	GND	2.0	50	TRØX-B	8.0	92			133		
10	EB04-I	10.0	51	GND	2.0	93	BIMES-I	13.0	134		
11	EB05-I	10.0	52	BCDX-B	7.0	94			135		
12	EB06-I	10.0	53	G.D	2.0	95	GND	2.0	136		
13	EB07-I	10.0	54	CDCX-B	7.0	96			137		
14	EB08-I	11.0	55	G D	2.0	97			138		
15	EB09-I	11.0	56	DCEX-B	7.0	98			139		
16	EB10-I	11.0	57	G D	2.0	99			140		
17	EB11-I	11.0	58	TAKX-B	8.0	100	GND	2.0	141		
18	EB12-I	12.0	59	G D	7.0	101			142		
19	EB13-I	12.0	60	DESX-B	8.0	102			143		
20	EB14-I	12.0	61			103			144		
21	EB15-I	12.0	62			104			145		
22	GND	2.0	63			105			146		
23			64			106			147		
24	GND	2.0	65	EB01X	5.0	107			148		
25			66			108			149		
26	GND	2.0	67			109	IØK1-I	13.0	150		
27	FRYX-I	5.0	68	EB01+	9.0	110	IØK2-I	13.0			
28	GND	2.0	69	EB01-	9.0	111	GND	2.0			
29	DRYX-I	5.0	70	EB02X	5.0	112	IØK3-I	13.0			
30	GND	2.0	71	EB02+	9.0	113	IØK4-I	13.0			
31	SERX-I	6.0	72	EB02-	9.0	114	GND	2.0			
32	GND	2.0	73	PRMY-I	8.0	115	BIAS	7.0,8.0			
33	TPIX-I	8.0	74			116					
34	GND	2.0	75	INTX-	8.0	117					
35	TPOX-I	8.0	76			118	+5V	2.0			
36	GND	2.0	77			119					
37	PRMX-I	8.0	78			120					
38	GND	2.0	79			121	+5V	2.0			
39			80			122	GND	2.0			
40	GND	2.0	81								
41			82								
			83								

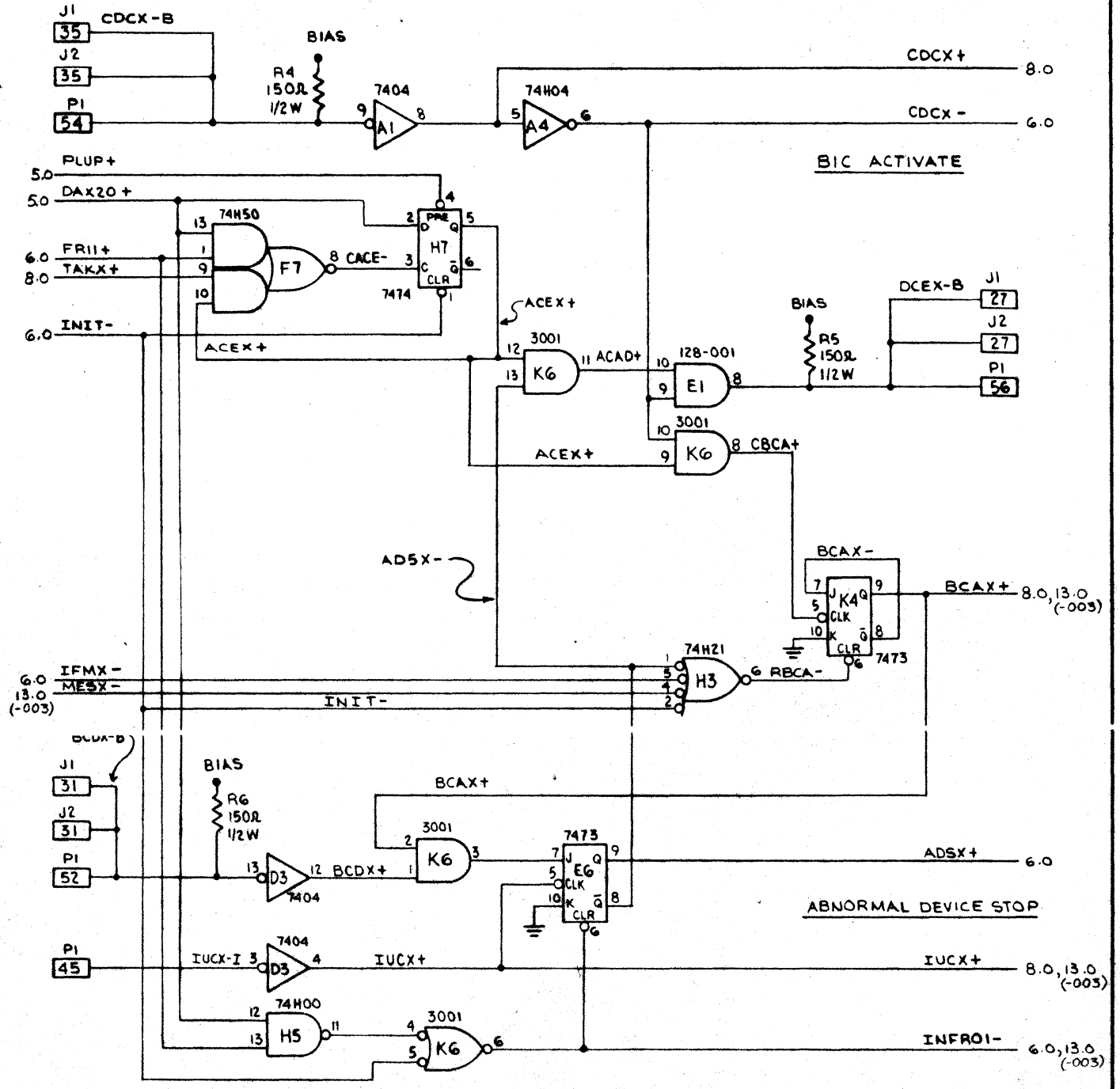
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0459	G
SCALE			SHEET 4.0 OF



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0459	G
SCALE		SHEET 5.0 OF	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0459	G
SCALE		SHEET 6.0 OF	



CODE IDENT NO.	SIZE	DWG NO	REV
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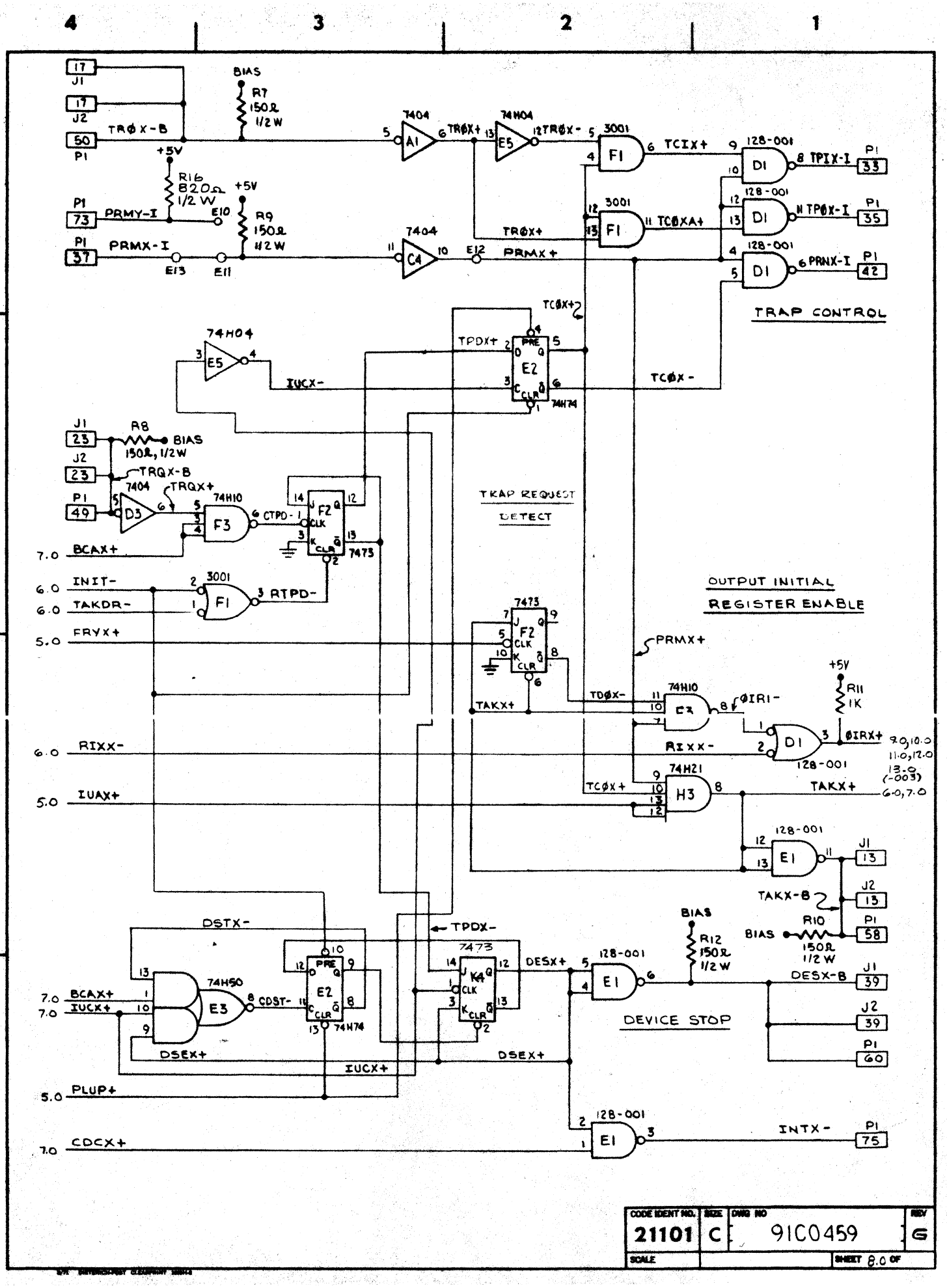
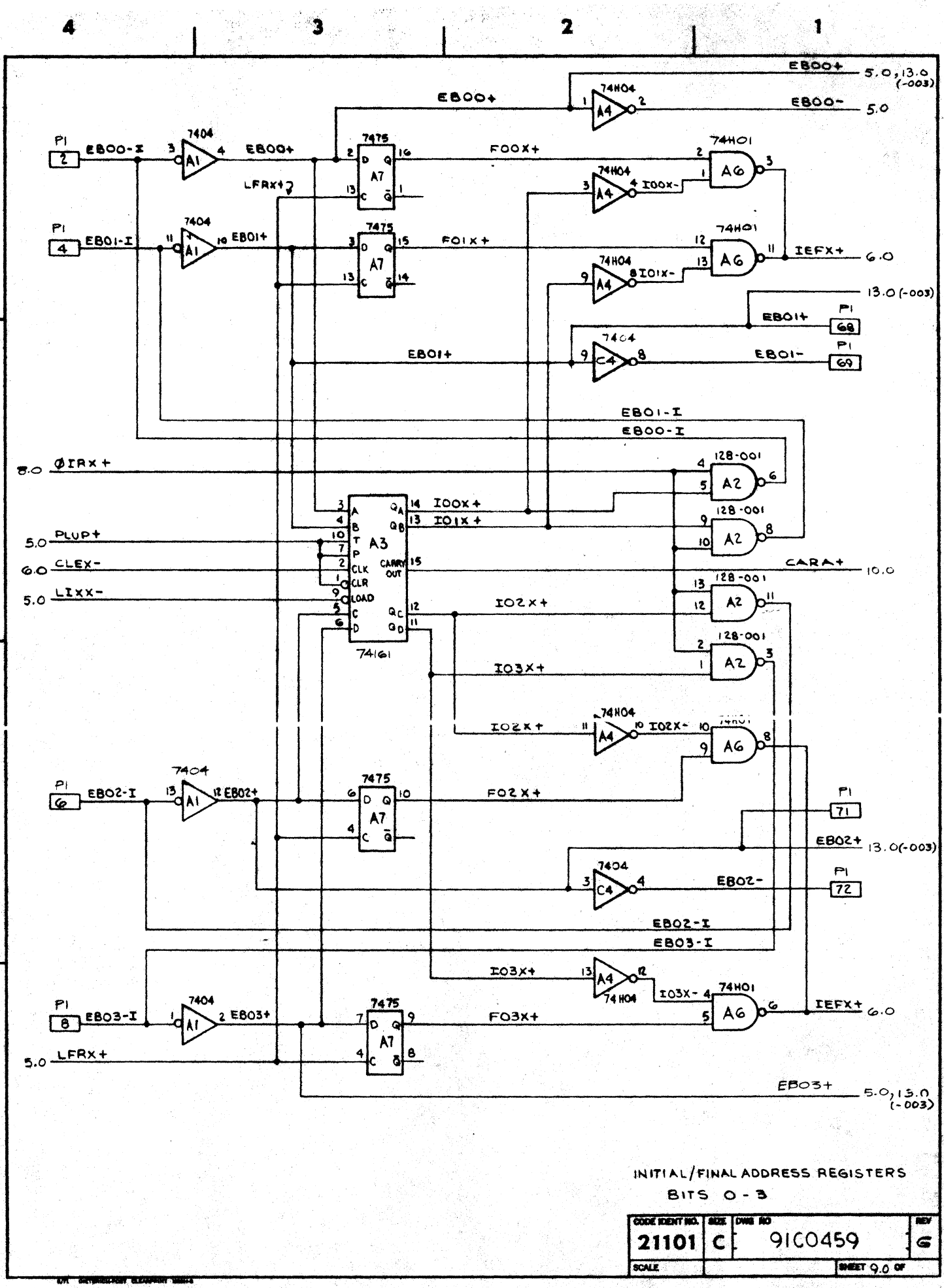
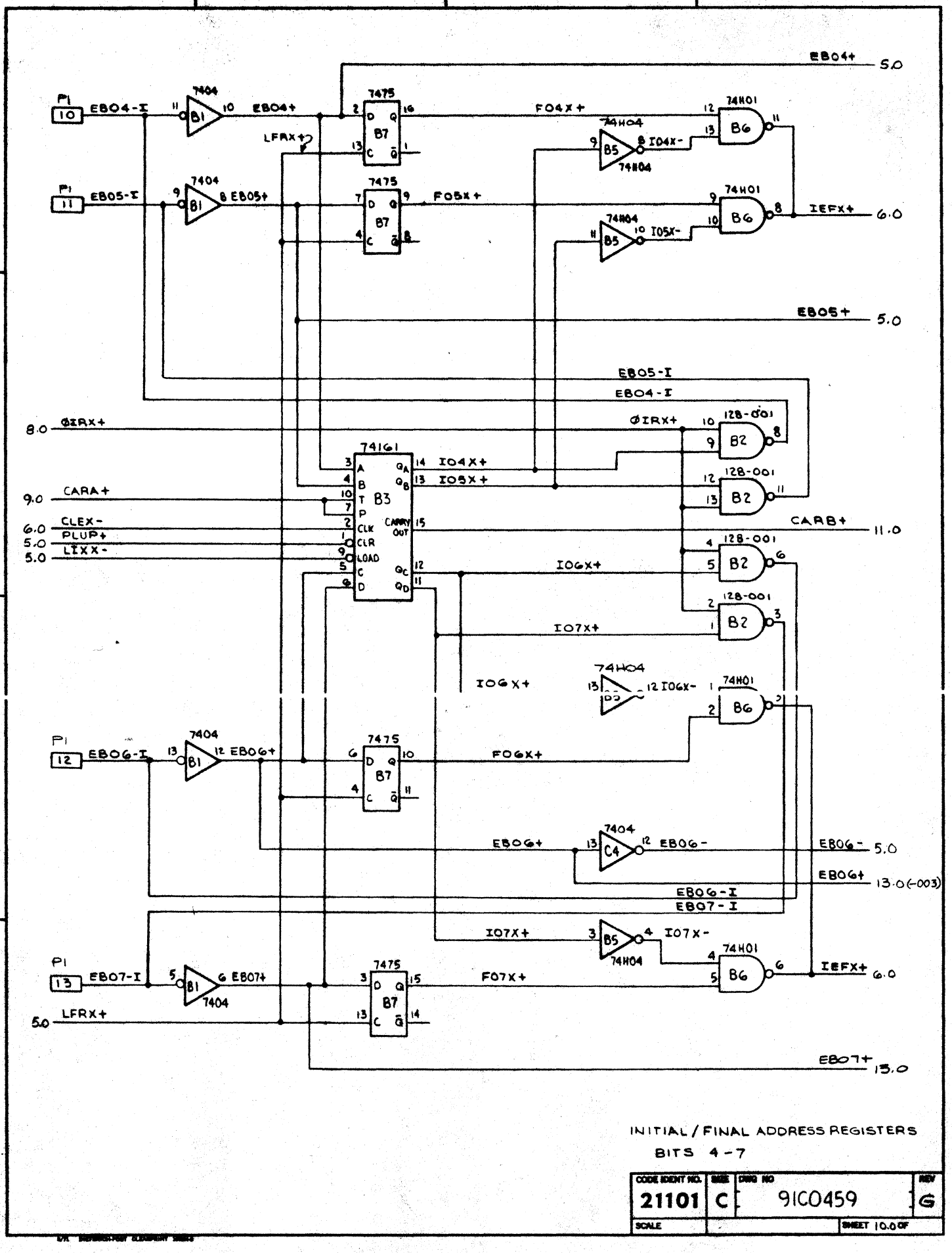
SCALE			SHEET 7.0 OF

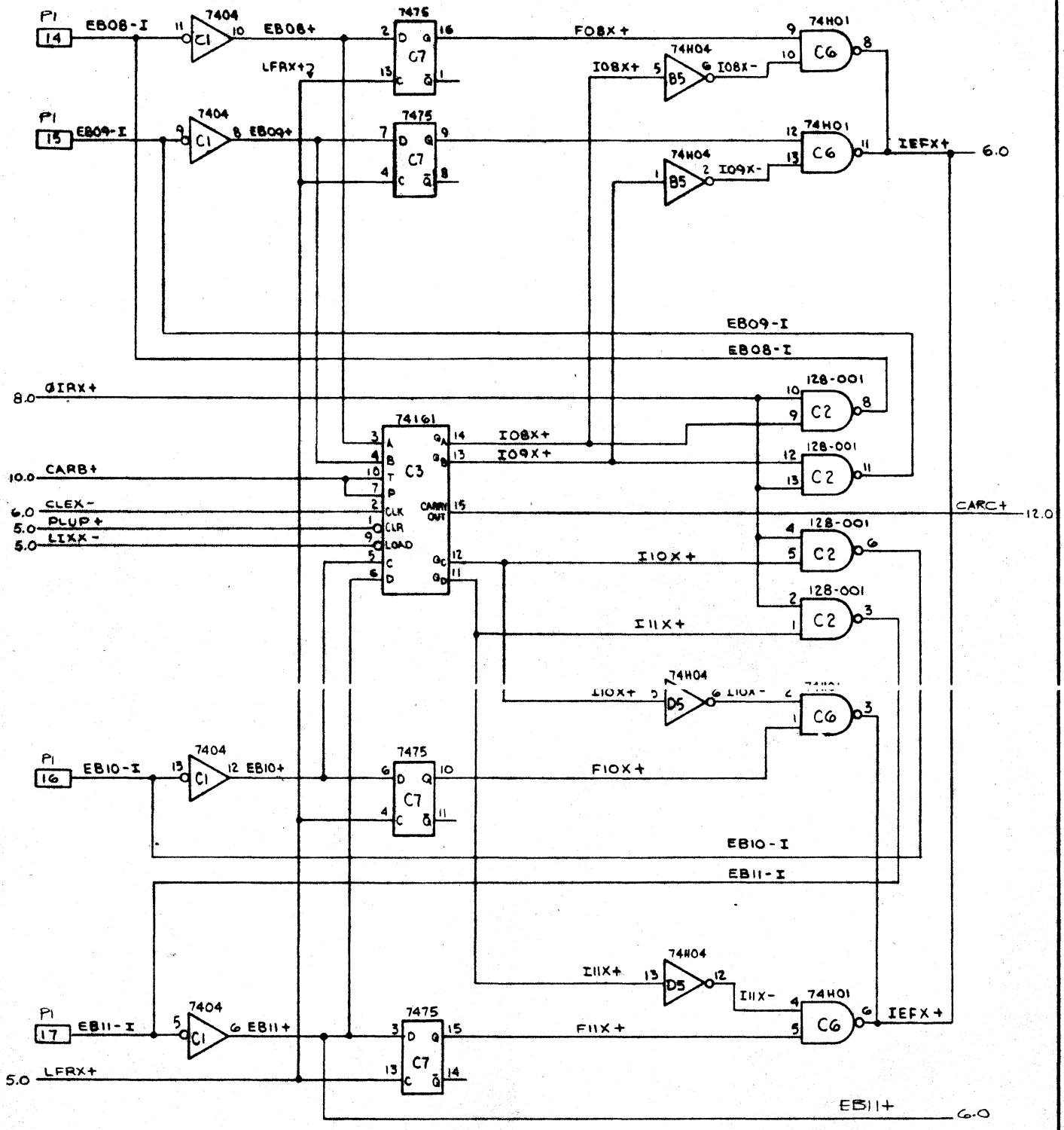

TRAP CONTROL
TRAP REQUEST DETECT
OUTPUT INITIAL REGISTER ENABLE
DEVICE STOP
BIAS
TRØX-B
PRMY-I
PRMX-I
TRØX+
TRØX-
TCIX+
TPIX-I
TCØXA+
NTPØX-I
PRMX+
PRNX-I
TCØX+
TPDX+
IUCX-
TCØX-
BCAX+
INIT-
TAKDR-
RTPD-
ERYX+
CTPD-
PRMX+
TDØX-
TAKX+
ØIRI-
ØIRX+
RIXX-
RIXX+
IUAX+
TAKX+
TAKX-B
DSTX-
TPDX-
DESX+
DESX-B
BCAX+
IUCX+
CDST-
DSEX+
IUCX+
DSEX+
PLUP+
CDCX+
INTX-
R7 150Ω 1/2W
R16 820Ω 1/2W
R9 150Ω 1/2W
R8 150Ω, 1/2W
R11 1K
R12 150Ω 1/2W
R10 150Ω 1/2W
7404
74H04
3001
128-001
74H10
74H21
74H50
74H74
7473
CODE IDENT NO. 21101
SIZE C
DWG NO 9100459
REV G
SCALE
SHEET 8.0 OF



INITIAL/FINAL ADDRESS REGISTERS
BITS 0 - 3

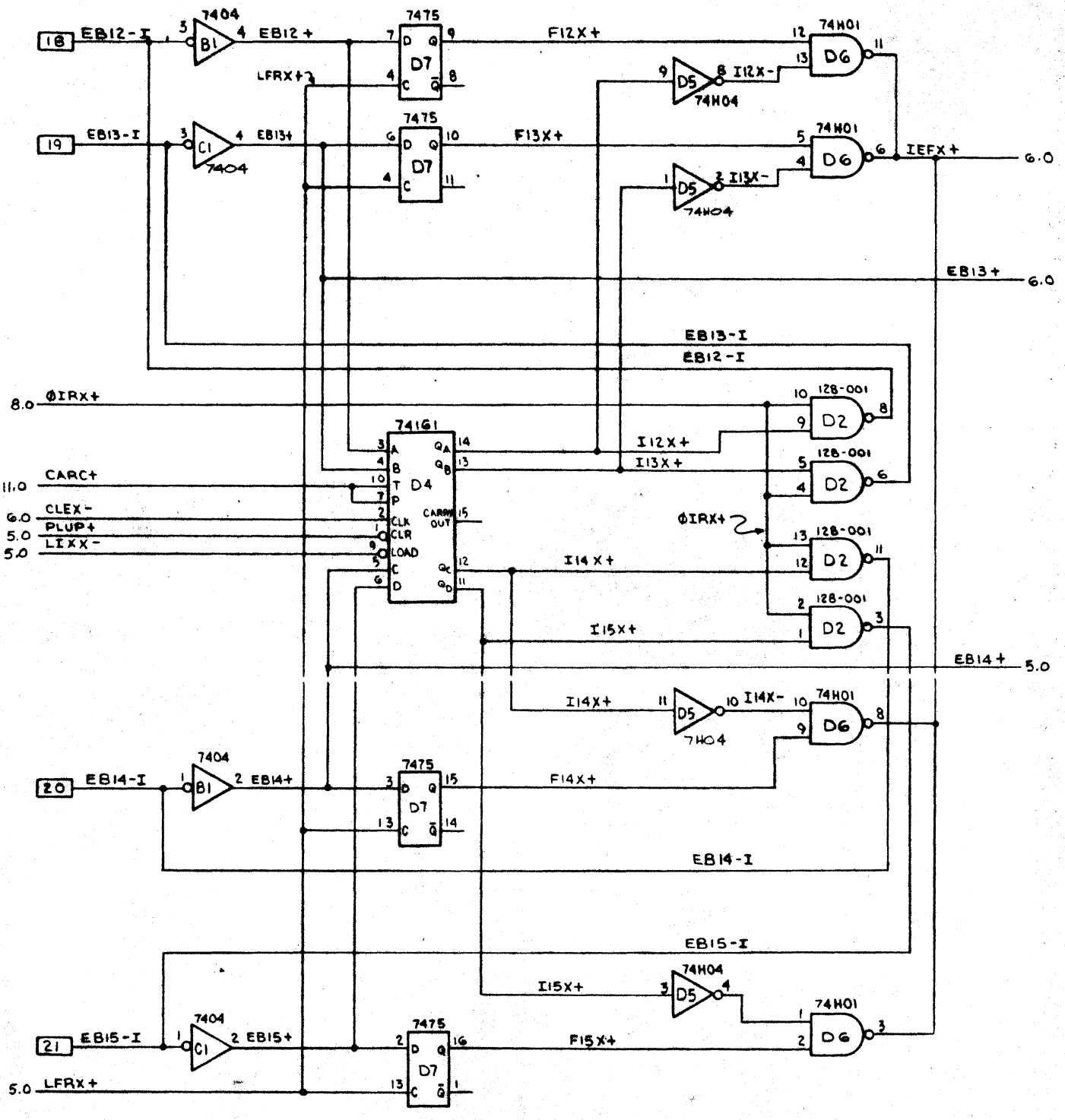
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	G
SCALE		SHEET 9.0 OF	


4
3
2
1
D
C
B
A
P1
10
EB04-I
7404
B1
EB04+
7475
B7
LFRX+
F04X+
74H04
B5
IO4X-
74H01
B6
IEFX+
6.0
EB04+
5.0
P1
11
EB05-I
EB05+
F05X+
IO5X-
EB05+
5.0
EB05-I
EB04-I
8.0
ØIRX+
74161
B3
IO4X+
IO5X+
9.0
CARA+
CLEX-
6.0
PLUP+
5.0
LIXX-
5.0
CARRY OUT
CARB+
11.0
128-001
B2
IO6X+
IO7X+
IO6X+
IO6X-
P1
12
EB06-I
EB06+
F06X+
EB06+
EB06-
5.0
EB06+
13.0(-003)
EB06-I
EB07-I
IO7X+
IO7X-
P1
13
EB07-I
EB07+
F07X+
IEFX+
6.0
5.0
LFRX+
EB07+
15.0
INITIAL / FINAL ADDRESS REGISTERS
BITS 4-7
CODE IDENT NO.
21101
SIZE
C
DWG NO
9100459
REV
G
SCALE
SHEET 10.0 OF



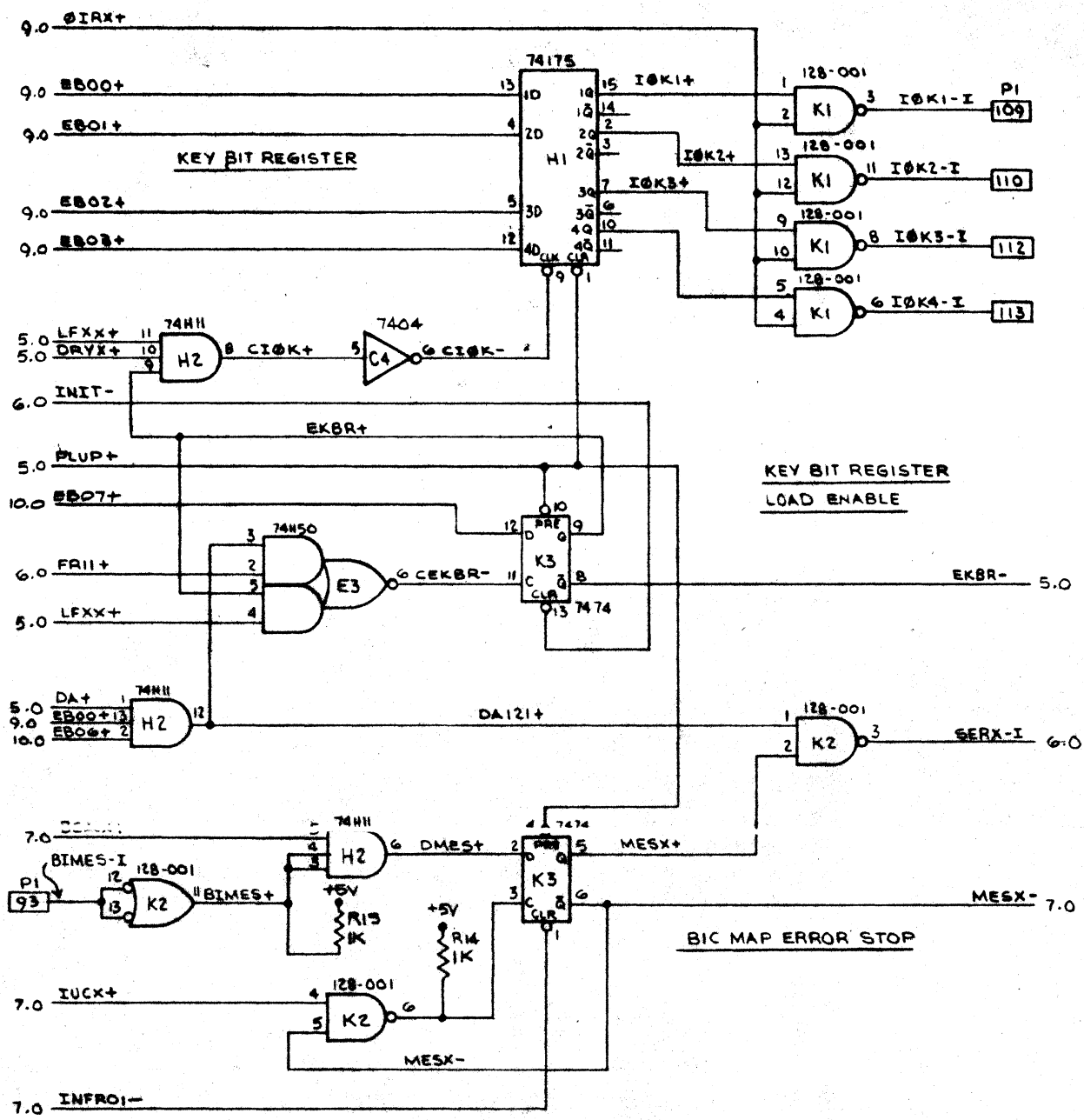
INITIAL / FINAL ADDRESS REGISTERS
BITS 8-11

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	G
SCALE		SHEET 11.0 OF	



INITIAL / FINAL ADDRESS REGISTERS
BITS 12 - 15

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	G
SCALE			SHEET 12.0 OF



-003 ONLY

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100459	G
SCALE		SHEET 13 OF	

REVISIONS

REV	EN	SPEC CODE	DESCRIPTION	DR	APPD
G	82603	1	QTY F/N 36 WAS: 17, QTY F/N 56 WAS: 7, ASSY REV LTR WAS: C, LOGIC REV LTR WAS: B, F/N 1 REV LTR WAS D	MH	5-23-74
F	82769	1	REV LTR OF FIND NO 1 WAS: E	DMF	5-28-74
G	82880	1	ADDED FIND NO. 42, 4000560-000 WAS F, 44D0689 WAS D, 91C0459 WAS C	R.D.	6/3/74
—	82966	1	REV. LTR OF F/N 1 WAS G	SO	6/28/74
H	83026	1	REV. LTR OF F/N 1 WAS: H	JJ	8/8/74
J	83164	1	REV. LTR OF REF DWG 44D0689 WAS: E, 91C0459 WAS: D F/N 1 WAS: J - QTY OF F/N 10 WAS: 6, F/N 11 WAS: 6, F/N 14 WAS: 4, F/N 15 WAS: 4	R.D.	9/5/74
K	83218		REV. LTR. OF REF DWG 91C0459 WAS: E, F/N 1 REV. LTR WAS: K	R.D.	9/25/74
L	83335		REV. LTR. OF 44D0689 WAS: K	—	10/1/74
M	83345		REV. LTR. OF 44D0689 WAS: "G", 91C0459 WAS: "F", F/N 1 WAS: "L". F/N 36 QTY WAS: 8 ADDED C27 TO REMARKS ADDED F/N 43	GRL	10/1/74

DR	J. ZOLL	5.11.73
CHK	R. JORDON	5.31.73
DSGN		
ENGR	T. HANSON	6.15.73
APPD		
APPD		

NEXT ASSEMBLY
01P1563

MODEL NO.
620, V73

CODE IDENT NO. 21101

varian data machines /a varian subsidiary
2722 michelson drive / irvine / california / 92664

TITLE PARTS LIST
BUFFER INTERLACE CONTROL - DM402

SIZE	DWG NO.	REV
A	44P0689	M

SHEET 1 OF 5

varian data machines
a varian subsidiary

DWG. NO. 44P0689

QUANTITY REQ'D PER DASH NO.					CODE IDENT: 21101		
003	002	001	000	FIND NO.	PART NUMBER	DESCRIPTION	REMARKS
REF	REF	REF	REF	–	44D0689	ASSEMBLY	
REF	REF	REF	REF	–	91C0459	LOGIC DIAGRAM	
REF	REF	REF	REF	–	97E0869	PHOTOMASTER	
REF	REF	REF	REF	–	97E0870	SOLDER MASK	
REF	REF	REF	REF	–	97E0871	SILKSCREEN	
1	1	1	1	1	40D0560-0001	PW BOARD	
4	–	4	4	2	49A0003-000	INTEG CIRCUIT	
–	4	–	–	3	49A0503-000		
3	–	3	3	4	49A0002-000		
–	3	–	–	5	49A0502-000		
3	–	2	2	6	49A0012-000		
–	2	–	–	7	49A0512-000		
2	–	1	1	8	49A0022-000		
–	1	–	–	9	49A0522-000	INTEG CIRCUIT	

NEXT ASSY 01R1563 | MODEL NO. 620/73 | APPD T.C.H. 6-15-73

REV	X	X1	A	B	C	D
EN NO.			82123	82246	82292	82354
DATE	5/11/73	5/31/73	5/31/73	9/5/73	9/5/73	9.26.73
DR	QZ	LC	RG	RGH	RGH	RGH
CHK			RGJ	TCH	TCH	TCH

TITLE: PARTS LIST
BUFFER INTERLACE
CONT DM402

DWG NO. 44P0689 REV A

SHEET 2 OF 5

varian data machines
a varian subsidiary

DWG NO. 44P0689

QUANTITY REQ'D PER DASH NO.								PARTS LIST			CODE IDENT: 21101
				003	002	001	000	FIND NO.	PART NUMBER	DESCRIPTION	REMARKS
				5	-	5	5	10	49A0023-000	INTEG CIRCUIT	
				-	5	-	-	11	49A0523-000		
				1	-	1	1	12	49A0039-000		
				-	1	-	-	13	49A0539-000		
				5	-	5	5	14	49A0040-000		
				-	5	-	-	15	49A0540-000		
				4	-	4	4	16	49A0042-000		
				-	4	-	-	17	49A0542-000		
				1	-	1	1	18	49A0082-001		
				-	1	-	-	19	49A0082-000		
				3	-	3	3	20	49A0093-001		
				-	3	-	-	21	49A0093-000		
				1	-	1	1	22	49A0094-001		
				-	1	-	-	23	49A0094-000		
				4	-	4	4	24	49A0104-000		
				-	4	-	-	25	49A0104-001	INTEG CIRCUIT	

NOTES:

DWG NO. 44P0689 REV C

SHEET 3 OF 5

A-0017-001C

varian data machines
a varian subsidiary

DWG NO. 44P0689

QUANTITY REQ'D PER DASH NO.						PARTS LIST			CODE IDENT: 21101
				003	002	001	000	FIND NO.	PART NUMBER	DESCRIPTION	REMARKS
				4	-	4	4	26	49A0127-000	INTEG CIRCUIT	
				-	4	-	-	27	49A0127-001		
				9	-	7	7	28	49A0128-001		
				-	7	-	-	29	49A0128-003		
				1	-	-	-	30	49A0178-000		
				1	-	1	1	31	49A0554-001		
				-	1	-	-	32	49A0554-000	INTEG CIRCUIT	
				6	4	4	4	33	65N2500-102	RESISTOR, 1K, 1/4W, ±5%	R1-3, 11, 13, 14 (R13, 14, USED ON -003 ONLY)
				8	8	8	8	34	65N5000-151	RESISTOR, 150Ω, 1/2W, ±5%	R4-10, 12
				18	18	18	18	35	71A0004-100	CAPACITOR, .1uf	C1, 3, 4, 6, 7, 8, 10, 12, 13, 14, 16, 17, 19, 20, 21, 22, 24, 25
				9	9	9	9	36	71A0200-475	CAPACITOR, 4.7uf, 20V	C2, 5, 9, 11, 15, 18, 23, 26, 27
				14	14	14	14	37	53C0194-000	BUS BAR	

NOTES:

DWG NO. 44P0689 REV M

SHEET 4 OF 5

A0017-001C

varian data machines

DWG NO. 44P0689

QUANTITY REQ'D PER DASH NO.								FIND NO.	PART NUMBER	DESCRIPTION	REMARKS
				008	002	001	000				
				-	0	0	-	38	90A0011-000	HUMISEAL	
				1	1	1	1	39	65N2500-511	RESISTOR, 510Ω, 1/4 W, ± 5%	R15
				-	0	0	0	40	53A0003-001	WIRE, JUMPER	30 AWG
				0	0	0	0	41	54A0001-124	SLEEVING	
				1	1	1	1	42	65N5000-821	RES 820Ω 1/2W ± 5%	RK6
				0	0	0	0	43	53A0701-000	WIRE, JUMPER, GRN	30 AWG

NOTES:

DWG NO. 44P0689

SHEET 5 OF 5

CODE IDENT: 21101

3100-2100-C

Addendum 1

Buffer Interlace Controller
Varian Document Number 98 A 9902 115

The following addition should be made to the Buffer Interlace Controller manual.

Page	Action
2-1	Add note following Table 2-1.

Note: On systems without memory map the BIMES-I and BTMES-I signals are floating. They must be pulled up by adding the following jumpers.

a. On each groundplane slot, add the following jumper:

   Pin 93 (BIMES-I) to pin 73 (PRMY-I)

b. On each PMA/BTC groundplane slot, add the following jumper:

   Pin 96 (BTMES-I) to pin 73 (EXPU+)

Issued: July 19, 1974