

WANG

3106

**CONTROL DATA CORPORATION
REMOVABLE STORAGE DRIVE
THEORY OF OPERATION
REPAIR AND REPLACEMENT**

Models:

**PA3A1
PA3A2**

Volume 2

**Customer Engineering Reprint
Product Maintenance Manual**

741-1490

PREFACE

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot, and repair the Removable Storage Drive.

First Edition (June, 1984)

This is the first reprint of Control Data Corporation's RSD, Volume 2. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as Product Update Bulletins (PUB's) or subsequent editions.

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CDC® REMOVABLE STORAGE DRIVE
PA3A1
PA3A2

THEORY OF OPERATION
GENERAL MAINTENANCE INFORMATION
TROUBLE ANALYSIS
ELECTRICAL CHECKS
REPAIR AND REPLACEMENT

Volume 2

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
01 (2-16-82)	Preliminary release
02 (5-14-82)	Preliminary manual update
03 (2-18-83)	Preliminary release of manual to cover Theory of Operation only.
04 (3-16-83)	Preliminary manual update to include sections on maintenance.
A (6-14-83)	Original release documenting series code 04 and below units. This edition obsoletes all previous editions.
B (7-26-83)	Manual revised to incorporate series code 05 technical and editorial changes.
C (9-26-83)	Manual revised to incorporate series code 06 technical and editorial changes.
D (1-25-84)	Manual revised to incorporate series codes 07 and 08 technical and editorial changes.

REVISION LETTERS I, O, Q
AND X ARE NOT USED.

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of this manual.

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PREFACE

This manual contains maintenance information for the CONTROL DATA® PA3A1 and PA3A2 Removable Storage Drives (RSDs). It is prepared for customer engineers and other technical personnel directly involved with maintaining the RSD.

The information in this manual is presented as follows:

- Section 1 - Theory of Operation. Describes power functions, electromechanical functions, interface, unit selection, servo surface decoding, sector detection, seek functions, head selection, read/write functions, and fault detection.
- Section 2 - General Maintenance Information. Contains information on warnings and precautions, maintenance tools and materials, testing the drive, and accessing the drive for maintenance.
- Section 3 - Trouble Analysis. Contains procedures and information to assist in troubleshooting the drive.
- Section 4 - Electrical Checks. Provides electrical test procedures.
- Section 5 - Repair and Replacement. Contains procedures and information on the replacement and adjustment of drive assemblies.

The following manuals apply to the RSD and are available from Control Data Corporation, Literature Distribution Services, 308 North Dale Street, St. Paul, MN 55103:

<u>Publication No.</u>	<u>Title</u>
83324480	PA3A1 and PA3A2 Hardware Maintenance Manual, Volume 1 (contains general description, operation, installation and checkout information, and parts data)

(Continued on Next Page)

Publication No.

Title

83324490	PA3A1 and PA3A2 Hardware Maintenance Manual, Volume 2 (contains theory of operation and maintenance)
83324630	PA3A1 and PA3A2 Hardware Maintenance Manual, Volume 3 (contains diagrams)
83322440	CDC Microcircuits, Volume 1 (provides functional descriptions for integrated circuits)
83324440	CDC Microcircuits, Volume 2 (provides functional descriptions for integrated circuits)

WARNING

To ensure the integrity of safety features built into these drives, installation and maintenance must be performed only by qualified service personnel using designated CDC/MPI parts. Also, in case of fire or other emergency, isolate the drives from main power by disconnecting the drive power plugs from their site power receptacles. In situations where pulling the plugs is not possible or practical, use the system main power disconnect to isolate the drives from main power.

WARNUNG

Um das einwandfreie Funktionieren der eingebauten Schutzvorrichtungen zu gewährleisten, darf die Installation und Wartung nur von qualifiziertem Service-Personal unter Verwendung von Original CDC/MPI Teilen durchgeführt werden. Beim Ausbrechen von Feuer oder in anderen Notfällen ist die Verbindung zum Hauptstromnetz dadurch zu unterbrechen, dass die Stecker der Antriebe aus den Steckdosen gezogen werden. Sollte dies nicht möglich oder unpraktisch sein, ist der Hauptstromunterbrecher des Systems zu bedienen, um die Antriebe vom Hauptstromnetz zu trennen.

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ABBREVIATIONS

A	Ampere	CLK	Clock
ABV	Above	CLR	Clear
ac	Alternating Current	cm	Centimeter
ADD	Address	CNTR	Counter
ADDR	Address	COMP	Comparator
ADJ	Adjust	CON'T	Control
ADRS	Address	CONTD	Continued
AGC	Automatic Gain Control	CT	Center Tap
ALT	Alternate	CYL	Cylinder
AM	Address Mark	D/A	Digital to Analog
AME	Address Mark Enable	dc	Direct Current
AMP	Amplifier, Ampere	DET	Detect
ASSY	Assembly	DIFF	Differential
BLW	Below	DIV	Division
C	Celsius	DLY	Delay
CB	Circuit Breaker	DRVR	Driver
CDA	Complete Drive Assembly	ECL	Emitter Coupled Logic
CDC	Control Data Corporation	ECO	Engineering Change Order
CH	Channel	EN	Enable
CHK	Check	ENBL	Enable

ABBREVIATIONS (Contd)

EXT	External	IND	Index
F	Fahrenheit, Fuse	INTRPT	Interrupt
FCO	Field Change Order	I/O	Input/Output
FDBK	Feedback	IPB	Illustrated Parts Breakdown
FIG	Figure	IPS	Inches per Second
FLT	Fault	kg	Kilogram
FSD	Fixed Storage Drive	kPa	Kilopascal
ft	Foot	kW	Kilowatt
FTU	Field Test Unit	lb	Pound
FWD	Forward	LED	Light Emitting Diode
GND	Ground	LSI	Large Scale Integration
HD	Head	LTD	Lock to Data
HEX	Hexagon	m	Meter
Hg	Mercury	MAX	Maximum
HR	High Resolution	MB	Megabyte
HYST	Hysteresis	MEM	Memory
Hz	Hertz	MHz	Megahertz
IC	Integrated Circuit	mm	Millimeter
IDENT	Identification	MPI	Magnetic Peripherals, Inc.
in	Inch		

ABBREVIATIONS (Contd)

MPU	Microprocessor Unit	PS	Power Supply
MRK	Mark	PWR	Power Supply
ms	Millisecond	RCVR	Receiver
MTR	Motor	RD	Read
mV	Millivolt	RDY	Ready
NC	No Connection	REF	Reference
NORM	Normal	REQ	Request
NRZ	Non Return to Zero	RES	Resolution
ns	Nanosecond	REV	Reverse, Revision
OC	On Cylinder	RGTR	Register
OS	One-Shot	r/min	Revolutions Per Minute
OSC	Oscillator	RSD	Removable Storage Drive
P	Plug	RTZ	Return to Zero
PD	Peak Detect	R/W	Read/Write
pF	Picofarad	s	Second
PG	Page	S/C	Series Code
PHH	Phillips Head	SEC	Second
PLO	Phase Lock Oscillator	SEL	Select
PROC	Procedure	SEQ	Sequence
PROG	Programmable	SPD	Speed

ABBREVIATIONS (Contd)

SS	Sector Switch	W	Watts
T	Tracks to go	W/	With
TF	Thread Forming	W/O	Without
TIM	Timer	W PROT	Write Protect
TP	Test Point	W+R	Write or Read
TSP	Troubleshooting Procedure	W·R	Write and Read
TTL	Transistor-Transistor Logic	WRT	Write
V	Volts, Voltage	XFR	Transfer
Vbb	Bias Voltage	Ω	Ohms
VCC	Bias Voltage	\$	Hexadecimal Address
VCO	Voltage Controlled Oscillator	uF	Microfarad
		us	Microsecond

SECTION

1

THEORY

OF

OPERA-

TION

THEORY OF OPERATION

INTRODUCTION

The theory of operation section describes drive operations and the hardware used in performing them. It is divided into the following major areas (refer to figure 1-1):

- Power Functions - Describes how the drive provides the voltages necessary for drive operation.

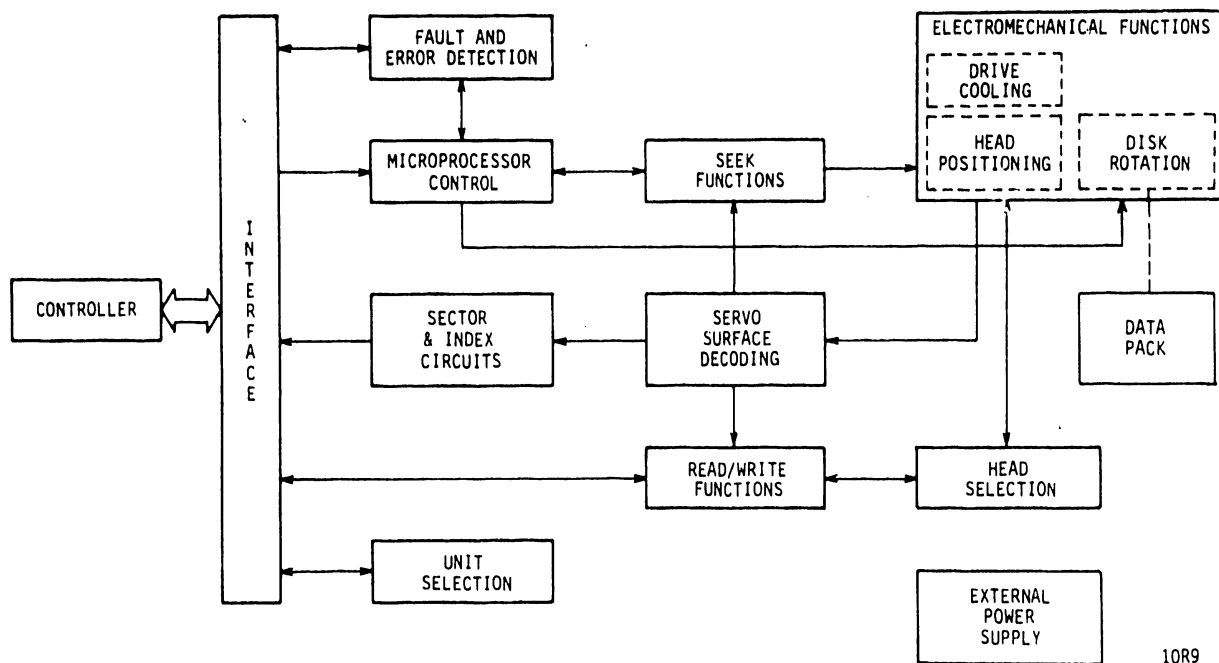


Figure 1-1. Drive Functional Block Diagram

- Electromechanical Functions - Provides a physical and functional description of the mechanical and electromechanical portions of the drive disk rotation, head positioning, and air flow systems.
- Interface - Describes the signal lines connecting the drive and controller. It also describes the I/O signals carried by these lines and how they are processed by the drive logic.
- Unit Selection - Explains how the controller logically selects the drive so the drive will respond to controller commands.
- Servo Surface Decoding - Explains how the decoding of the data read from the servo surface by the servo head is used to locate the radial position of the heads during a seek movement, the rotational position of the disks (indicated by the Index signal) when the heads are on track, and the exact speed of the disks (indicated by the 1.612 MHz clock signal).
- Sector Detection - Explains how the drive derives the sector pulses that are used to determine the angular position, with respect to index, of the read/write heads.
- Seek Functions - Explains how the servo logic controls the movements of the head positioning mechanism in positioning the heads over the disks.
- Head Selection - Explains the head selection process.
- Read/Write Functions - Describes how the drive processes the data that it reads from and writes on the disk.
- Fault Detection - Describes the conditions that the drive interprets as faults.

The descriptions in this section are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in volume 3 of the hardware maintenance manual should take precedence over those in this section if there is a conflict between the two.

POWER FUNCTIONS

GENERAL

Power functions are processes that take place within the power supply and the drive when the drive is powered up and powered down. These processes depend on whether the drive is set up for local or remote operation. In all cases, the power up and power down sequences are controlled through MPU programming that monitors whether start conditions are present and whether certain interlock and operating conditions are satisfactory. The following areas of the power functions will be discussed in detail:

- Power Distribution -- Describes how power is distributed to the drive circuitry.
- Local/Remote Power Sequencing -- Explains how the drive may be powered up either at the drive or by the controller.
- Power On Sequence -- Describes how the drive circuitry is initialized when power is applied and how the drive is prepared for normal operation.
- Power Off Sequence -- Describes how the drive is powered down, including unloading the heads and stopping the disk rotation.

POWER DISTRIBUTION

The power supply, which is external to the drive, provides the drive with basic dc supply voltages when circuit breaker CB1 is placed in the ON position. The drive itself has no ac power requirements. All drive circuitry, including the electronics, cooling fan, and drive motor, is operated with the dc supply voltages. The ac power cable connects the power supply (through CB1) to site ac power. The power supply can be conditioned for operation with any standard ac input voltage, as described in the Installation and Checkout section of Hardware Maintenance Manual, Volume 1.

The dc power cable connects the power supply to the drive. When CB1 is ON, this cable transmits four basic dc supply voltages to the drive electronics. These voltages are +5 V, -5 V, +24 V, and -24 V. The -5, -24, and +24 V supplies are protected against overload by pop-out circuit breakers on the power supply. The dc power cable also contains signal lines, which are enabled by control circuitry in the drive, to switch on 40 Vdc power to the drive motor and produce disk rotation.

There are secondary power supplies on the drive's Control Board that develop additional bias voltages for certain integrated circuits. One supply steps down the +24 V input and develops a regulated +15 V source. Another supply steps down the -24 V input and develops a regulated -15 V source. A third supply steps down the -15 V supply to develop a regulated bias of -8.3 V for the servo preamp chip.

The drive has circuitry that monitors the various supply voltages and disables write and/or servo functions when dc power is unreliable. For more information about voltage faults, refer to the Fault and Error Conditions discussion.

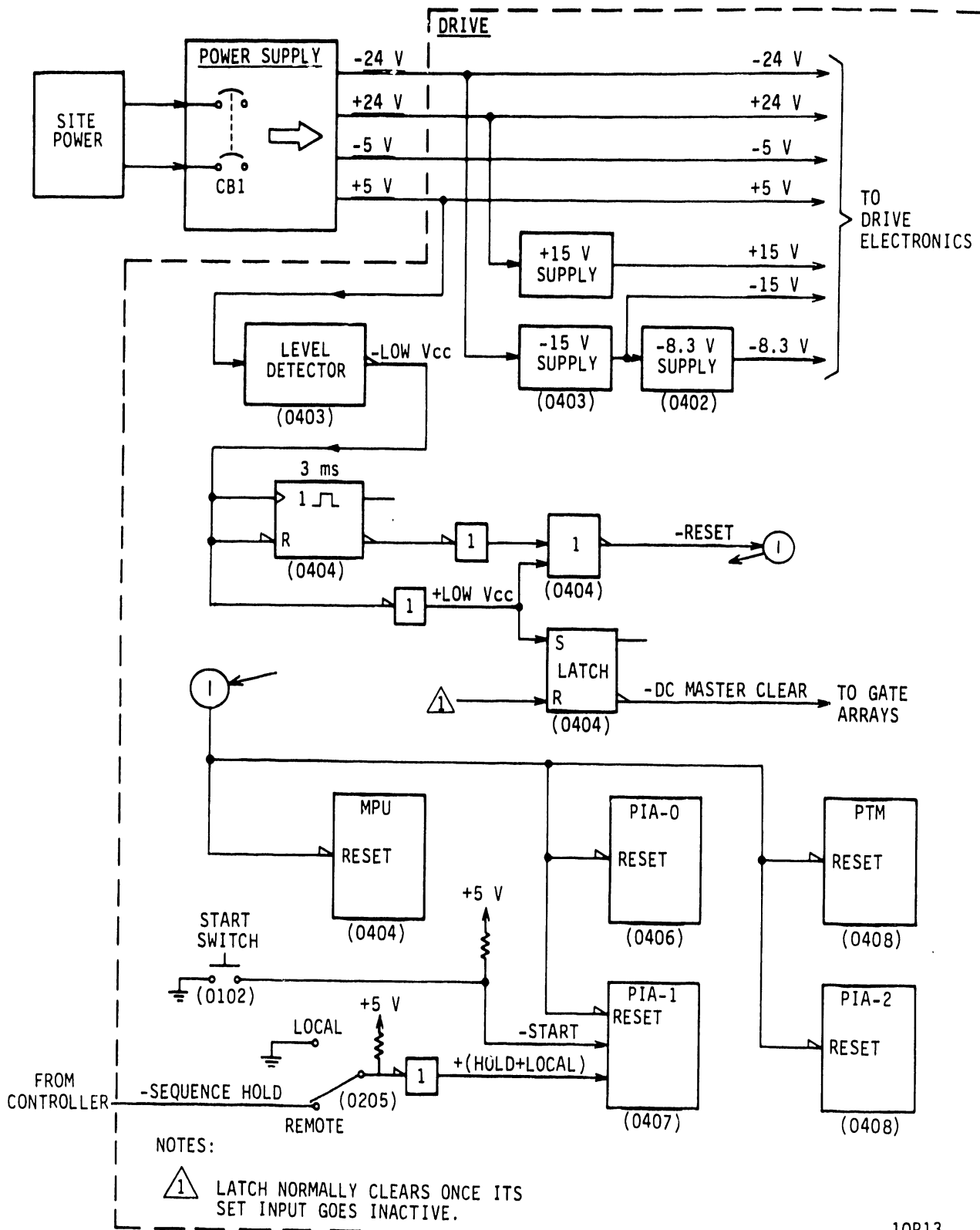
LOCAL/REMOTE POWER SEQUENCING

The local/remote feature selects whether or not the controller can control starting and stopping the drive motor. Part of drive installation is setting the LOCAL/REMOTE switch (on the drive I/O Board) for either local or remote operation. The LOCAL/REMOTE switch setting determines start conditions for the drive motor during power up. With the LOCAL/REMOTE switch in LOCAL, start conditions require only that the START switch is in the On position. With the LOCAL/REMOTE switch in REMOTE, start conditions require that the START switch is in the On position and that the controller has activated the Sequence Hold signal.

In a system of several drives set up for remote operation, the Sequence Hold command affects all drives simultaneously. When Sequence Hold goes active, it enables all drives to start their drive motors at the same time. When Sequence Hold goes inactive, it causes all drives to stop their drive motors at the same time.

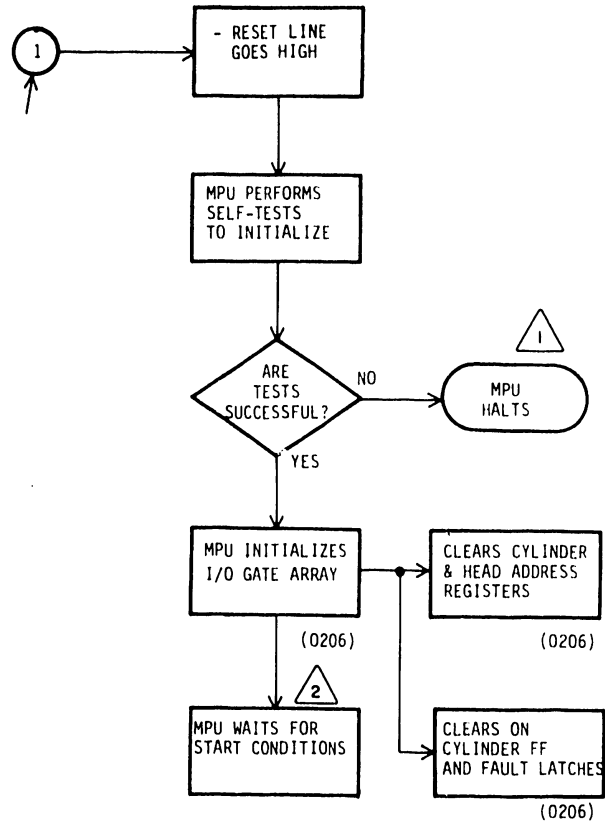
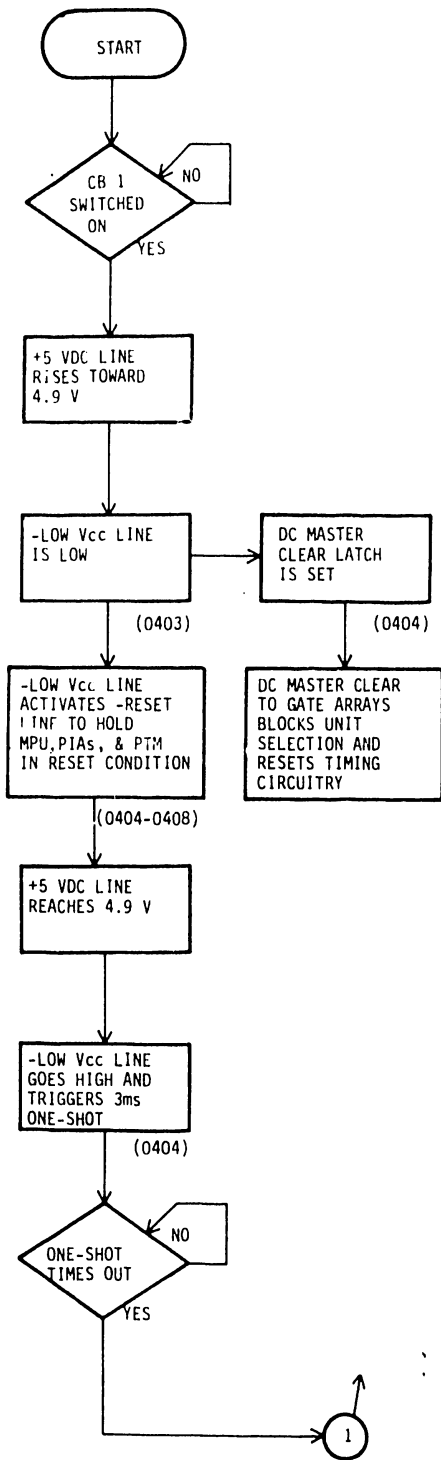
POWER ON SEQUENCE

The power on sequence takes place in two steps. Power on initialization occurs when dc power is applied to the drive. Following successful initialization, a load operation occurs each time that start conditions become available. Figure 1-2 is a simplified diagram of the power on circuitry, and figure 1-3 is a flowchart of the sequence. The following paragraphs describe power on initialization in detail and summarize the load operation. More information about load operations is given under Seek Functions.



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Figure 1-2. Power On Circuitry



NOTES:

1 INDICATIONS OF MPU HALT ARE GIVEN IN TEXT. DRIVE MUST BE POWERED OFF AND ON AGAIN IN EVENT OF MPU HALT.

2 REFER TO LOAD OPERATION FLOWCHART UNDER SPEC FUNCTIONS FOR EVENTS THAT FOLLOW START CONDITIONS.

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Figure 1-3. Power On Sequence Flowchart

Placing power supply circuit breaker CBI ON enables dc power to the drive. A level detector on the Control Board monitors the +5 Vdc input from the power supply and sets the -Low Vcc line high when this input reaches +4.9 V. Until this time, the DC Master Clear latch is set, and its output, the -DC Master Clear signal, remains low. In the Sector Counter Gate Array, the low -DC Master Clear signal resets the sector counter and the servo pattern decode circuitry. In the Address Decode Gate Array, the low -DC Master Clear signal disables the interface by blocking unit selection, and it resets timing circuitry that develops Index and Cylinder pulses. In dual channel drives, the low -DC Master Clear signal blocks unit selection by either controller.

The -Reset line to the MPU goes low when -DC Master Clear goes low, and it is held low by a one-shot for about 3 ms after the -Low Vcc line goes high. When -Reset goes high, the MPU performs three self-test operations to initialize itself. These tests are as follows:

- The MPU performs a checksum calculation on the ROM contents. This test validates that the MPU's firmware instructions are readable.
- The MPU tests its internal RAM by writing information into it and reading it back.
- The MPU initializes its PIAs by sending data to them and reading it back.

If the first two tests fail, the MPU halts and all the individual fault LEDs on the Control Board remain lit. If the third test fails, the MPU tries to light the First Seek LED and halts. None of these tests can produce an operating panel FAULT indication, and there is no way to clear these faults except for turning CBI OFF.

With the self-tests complete, the MPU initializes the circuitry within the I/O Gate Array. The MPU communicates with the I/O Gate Array via I/O Control lines 1, 2, and 3. The MPU pulses I/O Control lines 1 and 2 with a serial code that clears the Cylinder Address register (CAR), the Head Address register (HAR), the On Cylinder FF, and the Fault latches.

The MPU requires that the drive motor is stopped and the heads are unloaded prior to unlocking the front door. To do this, it checks motor speed by counting -Motor Sensor pulses with the PTM #3 counter and looks at the -Heads Loaded Switch line at PIA-1. If these checks are satisfactory, the MPU issues the Unlock Door command at PIA-1 to energize the Door Unlock Solenoid, allowing the door to be opened for installing or exchanging disk packs.

At this point, power on initialization is complete. This process will not be repeated until dc power is removed and reapplied to the drive (via CBI). The MPU waits for start conditions by monitoring the START switch and (in remote operation) the Sequence Hold signal from the controller.

When start conditions are present, the MPU directs the load operation. The load operation energizes the drive motor to bring the disks up to speed and loads the heads to position them over the disks at track 0. Details of the load operation are given under Seek Functions. When the load operation is complete, the drive waits for commands from the controller.

POWER OFF SEQUENCE

The power off sequence unloads the heads and stops the drive motor. There are two conditions that initiate a power off sequence. One is a loss of start conditions, and the other is a loss of dc power to the drive. Both conditions produce retract operations: the first, a normal retract; and the second, an emergency retract. These retract operations are discussed in detail under Seek Functions. The drive motor comes to a stop after the retract is completed. The following paragraphs describe both types of power off sequences.

A loss of start conditions occurs when the START switch is pressed to release it from the Start position or (in remote operation) when the controller deactivates Sequence Hold. The MPU monitors the start conditions and commands a normal retract when they are removed. The MPU issues the -Retract command to withdraw the heads from the disk pack under servo control. When the heads are fully retracted, the contacts on the Heads Loaded switch open, indicating to the MPU that the retract is complete. The MPU then drops the Motor Run command to disable the Motor Speed Control, and dynamic braking stops the drive motor. The MPU monitors drive motor speed by counting -Motor Sensor pulses and issues the Unlock Door command at PIA-1 when the motor has stopped. This energizes the Door Unlock Solenoid, allowing the door to be opened for disk pack removal. The drive remains in this condition until start conditions reappear.

A loss of dc power results when power supply circuit breaker CBI is switched OFF or when there is a loss of site ac power. When the dc voltages drop, an emergency retract takes place under hardware control. The emergency retract operation requires no MPU intervention, and it uses voltage generated by the decelerating drive motor to drive the heads outward to the unloaded position. With a loss of dc power, the drive motor coasts to a stop.

ELECTROMECHANICAL FUNCTIONS

GENERAL

Certain drive functions are a result of the electromechanical devices using drive power and working under the control of drive logic circuitry. These functions include disk rotation, head positioning, and drive cooling and ventilation.

DISK ROTATION

General

Disk rotation is accomplished by an electromechanical system that engages the disks to the spindle during data pack installation, accelerates the disks to 3600 r/min during power up, stops disk rotation with dynamic braking during power down, and disengages the disks from the spindle during data pack removal. The mechanical and electrical aspects of this system are discussed in the following paragraphs.

Mechanical Description

The mechanical components used for disk rotation are a linkage system that engages and disengages the disks and the spindle, and a drive motor that rotates the disks.

Pack and Spindle Linkage

The pack and spindle linkage is controlled by opening and closing the front door during data pack installation and removal. When an operator closes the front door after inserting a data pack in the drive, several things happen. One set of levers moves the data pack toward the spindle, and the shaft on the disk hub enters the spindle receptacle. A second set of levers activates a bayonet lock within the spindle receptacle, which locks the shaft on the disk hub to the spindle and allows the spindle to rotate the disk hub. Interlock switches sense whether the door is locked and whether a data pack is in place; these interlock conditions must be satisfied before the powering up the drive motor is enabled.

The front door is locked by a solenoid while the disks are rotating. However, when the disks are not rotating, opening the door operates the two sets of levers with the following results. The bayonet lock in the spindle releases the shaft on

the disk hub, and the pack receiver moves the data pack away from the spindle until it lines up with the front door opening. The pack retainer releases the data pack from the pack receiver so that it can be removed from the drive.

Drive Motor

The drive has a direct drive system for disk rotation with the drive motor mounted concentrically on the spindle. The motor has a three-phase stator surrounded by a four-pole rotor. The motor speed control (described in the next topic) provides pulsed excitation to the three stator windings. To keep the stator pulses in phase with rotor position, the speed control uses feedback from sensors located in the motor. These sensors employ the Hall Effect to sense flux reversals from the rotor magnets. As the rotor magnets pass each sensor, its output line toggles.

In addition to rotating the disks, the drive motor produces air flow through the data pack and positioner assembly. Air flow is circulated in a closed loop by an impeller attached to the rotor of the drive motor (see Air Flow System discussion).

Electrical Description

General

Electrical operation of the drive motor is discussed in two functional areas:

- Motor Control System -- discusses how the drive motor is started and how its speed is regulated.
- Dynamic Motor Braking -- discusses how the drive motor is decelerated and the front door is unlocked.

Motor Speed Control

The motor speed control regulates operation of the drive motor. Subject to interlocks, the microprocessor issues a command to start the drive motor during the power on sequence (see Power On Sequence discussion). The motor speed control activates the 40 V dc output of the power supply and uses this power source to excite the stator windings in the drive motor. The control and status lines between these system elements are shown in figure 1-4.

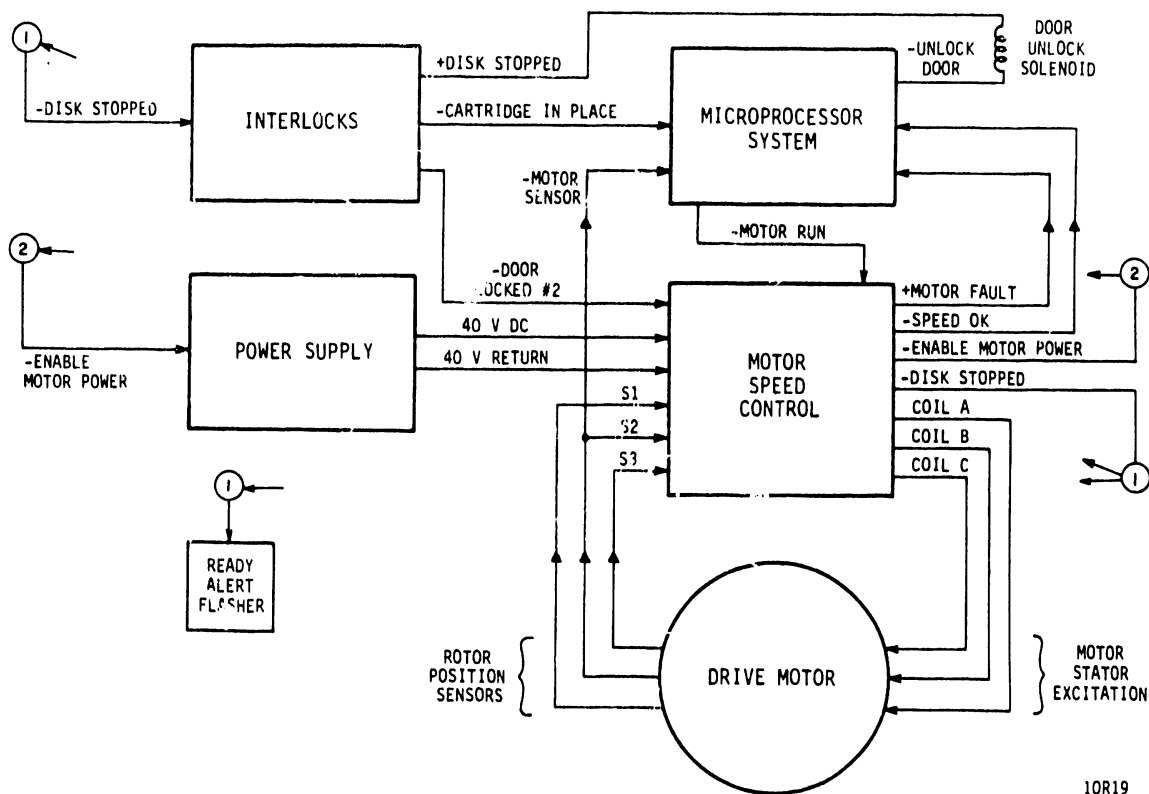


Figure 1-4. Motor Speed Control System Diagram

To start the drive motor, the microprocessor drops the -Motor Run line. The drive motor receives power as long as this line is held low. With the -Motor Run and the -Door Locked #2 lines low, the motor speed control issues the -Enable Motor Power command to switch on the 40 V dc output of the power supply.

The motor speed control divides each shaft rotation of the motor into twelve 30° segments. During each segment, a current path is selected through two of the three stator coils. These stator excitations are timed so that, in each segment, the selected stators exert a counterclockwise torque on the permanent magnets of the rotor.

Rotational position of the motor shaft is relayed to the motor speed control by sensors S1, S2, and S3 located inside the motor. The sensors are positioned at 30° intervals. Each sensor employs the Hall Effect to output a digital level that switches when the polarity of the local magnetic field reverses. The waveforms of S1, S2, and S3 are shown in figure 1-5.

The motor speed control regulates motor speed by modulating the width of the pulses applied to the stator coils. The motor speed is kept within the following range: 3580 r/min (16.49 ms/rev) to 3634 r/min (16.78 ms/rev). The pulses have maximum width until the rotation time decreases to 16.78 ms. Then the pulse width decreases linearly to a near-zero value corresponding to a rotation time of 16.49 ms.

Figure 1-6 shows simplified logic for the motor speed control. The control modulates the motor pulses as follows: Once per rotation, a signal called +360° Pulse goes active. This signal triggers a 16.49 ms reference delay, derived by subdividing the 4 MHz clock in the motor speed control. This reference delay corresponds to one motor rotation at the maximum allowable speed. A comparator circuit outputs a pulse that is active from the end of the reference delay until the next 360° Pulse. The active time for the comparator output pulse determines the on-time of the +Drive Enable line during each 30° segment of motor rotation. Power is applied to the stator windings only when +Drive Enable is high. This condition is updated once per motor rotation, and the duty cycle of the motor is readjusted to keep the motor speed within its specified range.

Three status outputs are generated by the motor speed control and are used as follows:

- +Motor Fault -- indicates to the MPU that the drive motor has a bad magnetic sensor.
- -Speed OK -- indicates to the MPU that the drive motor speed is between 3580 and 3634 r/min and that no motor fault is present.
- -Disk Stopped -- indicates to the interlock circuitry that the last disk rotation exceeded two seconds.

Dynamic Motor Braking

Dynamic motor braking decelerates the drive motor during a power off sequence. Dynamic braking occurs when power is

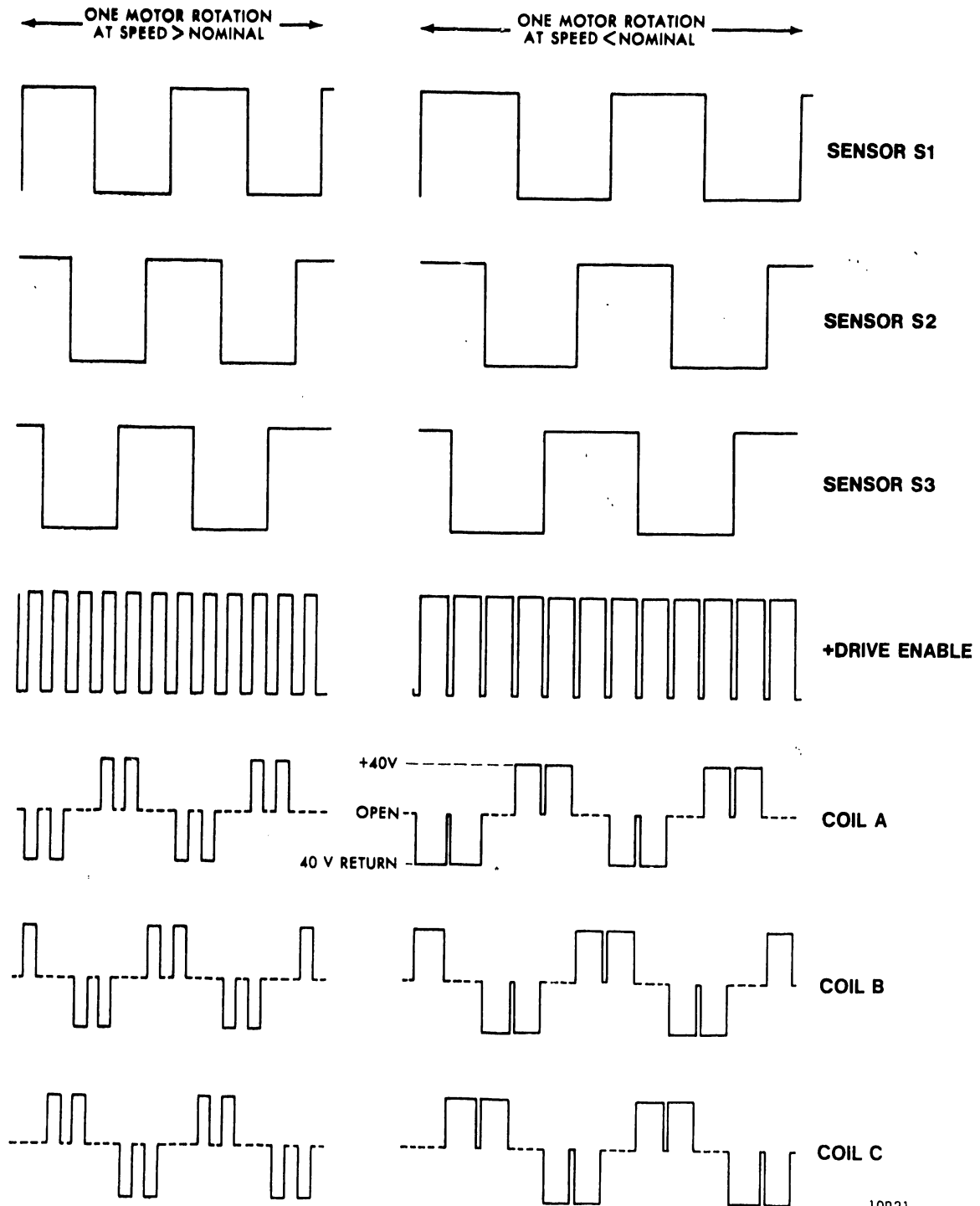
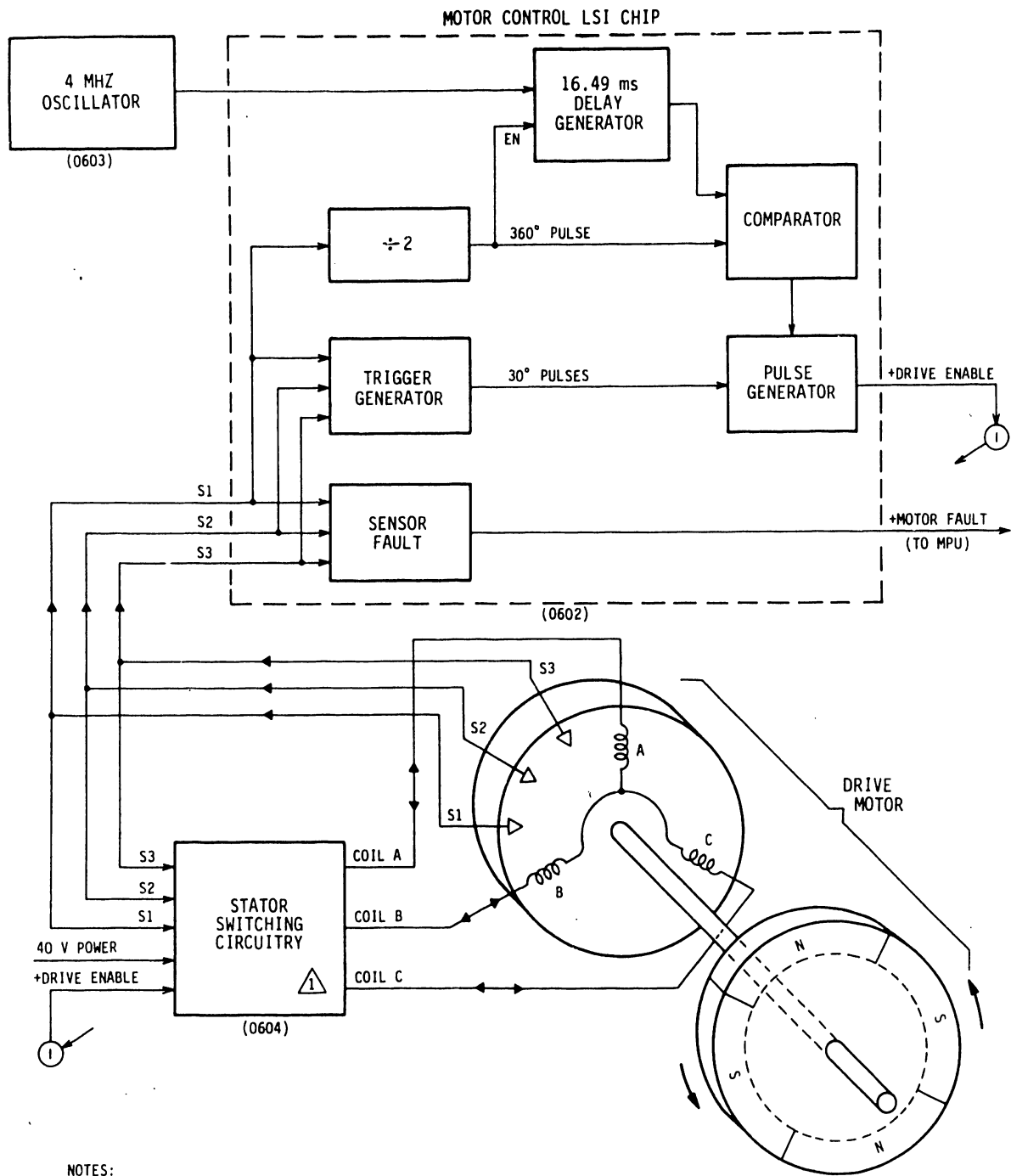


Figure 1-5. Speed Control Waveforms and Timing



NOTES:
 ⚠ REFER TO SPEED CONTROL WAVEFORMS AND TIMING DIAGRAM FOR INPUT AND OUTPUT WAVEFORMS OF THIS CIRCUIT.

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Figure 1-6. Motor Speed Control Simplified Logic

removed from the drive motor. As the motor continues to rotate, it acts as a generator. The generated current is dissipated in a resistive load, converting the rotational energy into heat.

Dynamic braking begins when the microprocessor deactivates the -Motor Run line to the motor speed control. This causes the motor speed control to turn off the 40 V power supply output so that no power source is connected to the stator switching circuitry. The generator output appears across the 40 V input lines because timing signals continue to be applied to the stator switching circuitry. Initially, the speed control activates Brake A, connecting a 4.3 ohm resistor across the generator output. When the motor speed drops to 2440 r/min, the speed control activates Brake B also; this connects a 2 ohm resistor in parallel with the 4.3 ohm resistor. Reducing the load resistance increases the braking action, and the motor stops rotating.

The motor speed control activates the -Disk Stopped line to indicate that braking is complete. This output to the interlock circuitry allows the microprocessor to energize the Door Unlock Solenoid and turns off the flasher circuit for the Ready indicator to show that power down is complete. At this time, the data pack can be removed from the drive.

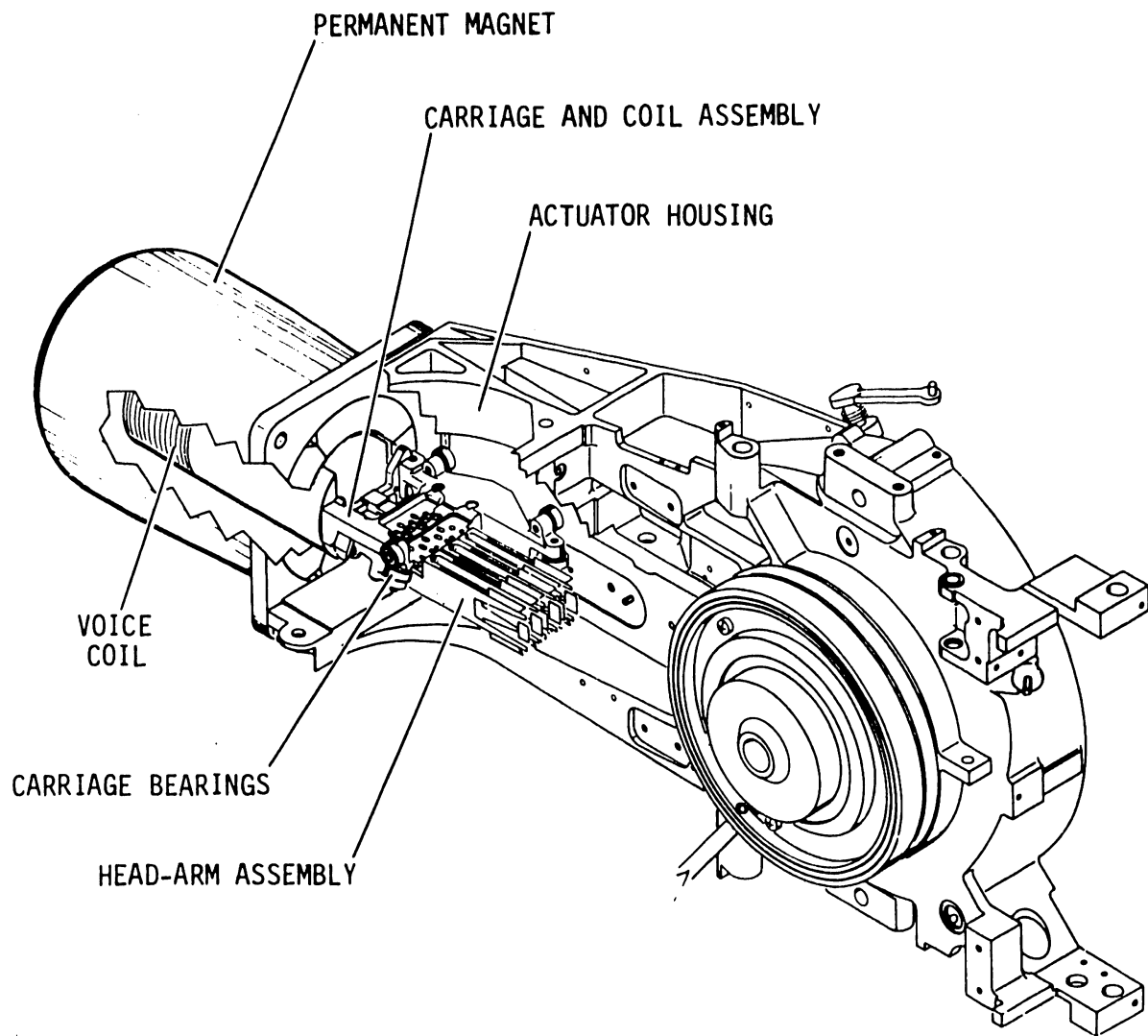
HEAD POSITIONING

General

Data is written on and read from the disk by the heads. The drive must position the heads over a specific data track before a read or write operation can be performed. Head positioning is performed by the actuator mechanism which is an integral part of the drive. The actuator is controlled by inputs received from the servo circuits (refer to the discussion on Seek Functions).

Actuator and Magnet Physical Description

The actuator (shown in figure 1-7) consists of the actuator housing, the carriage and voice coil assemblies, and the head-arm assemblies. The head-arm assemblies, with the heads mounted at their front, are mounted at the forward end, and the voice coil at the opposite end, of the carriage assembly. The carriage assembly fits within and is provided with horizontal movement into/out of the permanent magnet by wheels riding along a carriage track. During head positioning, the carriage rides the track towards or away from the magnet and out over the disk surfaces.



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Figure 1-7. Actuator and Magnet Assembly

Actuator and Magnet Functional Description

The voice coil is mounted at the opposite end of the arm assembly and moves in and out of the magnet as the servo signals change. The magnet is mounted on the housing in a position which allows the voice coil to move as the field in the coil changes. This small in and out motion of the voice coil in the magnet provides the motion for the heads over the disk surface. The movement of the carriage and voice coil (and therefore the heads) is controlled by positioning signals from the servo logic. The positioning signals are derived in the analog servo system and processed by the power amplifier. The output of the power amplifier is a current signal which is applied to the voice coil.

The current from the power amplifier causes a magnetic field in the voice coil which either aids or opposes the field around the permanent magnet. This reaction either draws the voice coil into the magnet or forces it away, depending on the polarity of the current through the voice coil. The acceleration of the voice coil is dependent on the amplitude of the voice coil current.

HEADS

General

The heads are magnetic devices that record data on, and read data from, the disk surface (the servo head, however, reads prerecorded data but cannot write). Each head is mounted at the end of a supporting arm. Head and arm together are called a head-arm assembly. The head-arm assemblies are attached to the front of the actuator assembly (figures 1-7 and 1-8).

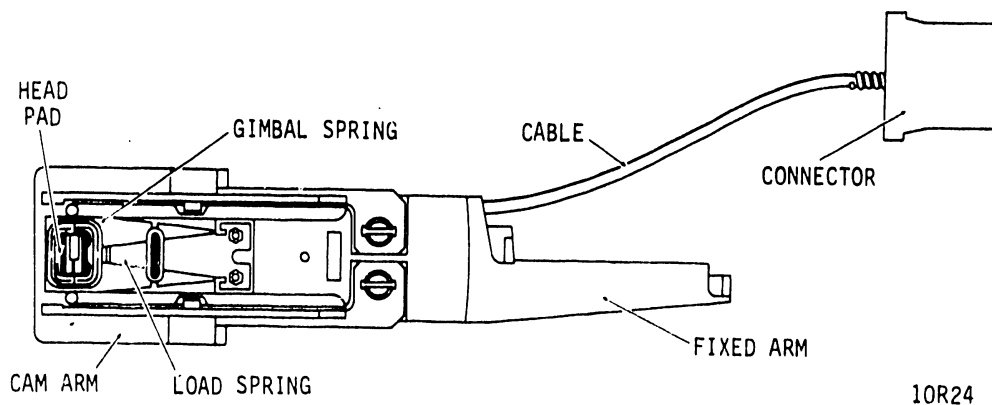


Figure 1-8. Data Heads

The drive has 5 movable data heads and one servo head. The data (or read/write) heads are used to record data on and read data from the disk data surfaces. The servo head is used to read prerecorded data from the servo disk surface for use by the drive analog servo circuits.

The following paragraphs describe the physical characteristics of the movable head-arm assemblies and how they function during head load and retract sequences. Further information about the heads is found in the discussions on seek and read/write functions.

Head-Arm Assembly

Each head-arm assembly consists of a fixed arm, cam arm, load springs, gimbal spring, and the head (figure 1-8). The head-arm assemblies are mounted at the front of the actuator carriage and follow the in/out motion of the carriage created by the reaction of the voice coil magnetic field to the field of the permanent magnet. The rigid arm by itself does not provide the action necessary for the heads to load or unload. The head load spring forces its associated head toward the disk surface; the gimbal spring allows the head free axial movement along its vertical and horizontal axes independent from the rigid arm.

Read/write information is transferred to and from the heads through the head-arm cables. One end of each cable connects to a head and the other end has a plug which connects to the Read/Write Preamp board.

Head Loading

In the retract (non-operating) condition the actuator is retracted so that the actuator is pulled away and the heads are withdrawn from the disks (in the unload/retract position). When the system powers up, the program turns on the drive motor. When the drive motor is rotating the disks at acceptable speed, the program moves the actuator in to track 0. During normal operation the system utilizes the cushion of air created by disk rotation to prevent actual head/disk contact. While they remain loaded over the disks, the heads continue to fly on this cushion of air.

The head load spring forces the head toward the disk surface, while the cushion of air pushes against the head to resist its closer approach. The air cushion pressure varies directly with disk speed, so that at proper speed the forces of the head load

spring pressing the head towards the disk surface and the opposing force of the air cushion resisting the closer approach of the head are balanced such that the heads fly at the correct height above the disk.

If the disk drops below speed, the air cushion pressure decreases and the head load springs force the heads closer to the disk surface. Sufficient loss of speed would cause the heads to stop flying and contact the disk. This is called head landing. Because insufficient disk speed causes head landing, heads are not moved into the data areas until the disks have come up to speed. For the same reason, the heads are retracted from the disk surfaces when the speed drops below a safe operating level.

AIR FLOW SYSTEM

The air flow system is divided into two parts, one for the drive unit and the other for the sealed data pack.

The drive air flow system (figure 1-9) provides continuous air replacement and circulation to dissipate the heat generated by drive operation. The main component of the drive air flow system is the fan that is mounted on the rear panel. The fan motor is driven from the -24 V power from the external power supply. The fan pulls ambient air through the input and primary filter of the front panel. The fan circulation travels over the electronics, cooling these assemblies before leaving the drive through the back panel. The system intake port is located on the front panel. This port is covered by the primary filter which keeps large particles from being drawn into the system.

The air flow system for the data pack is a self-contained closed loop system (figure 1-10). The system consists of an impeller (fan) which is attached to the drive motor, and an absolute filter located beneath the actuator. The rotation of the motor rotates these fan blades. The motion of the blades forces air through the hose into the absolute filter, and through the filter into the data pack.

INTERFACE

GENERAL

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals, and read/write data transfers.

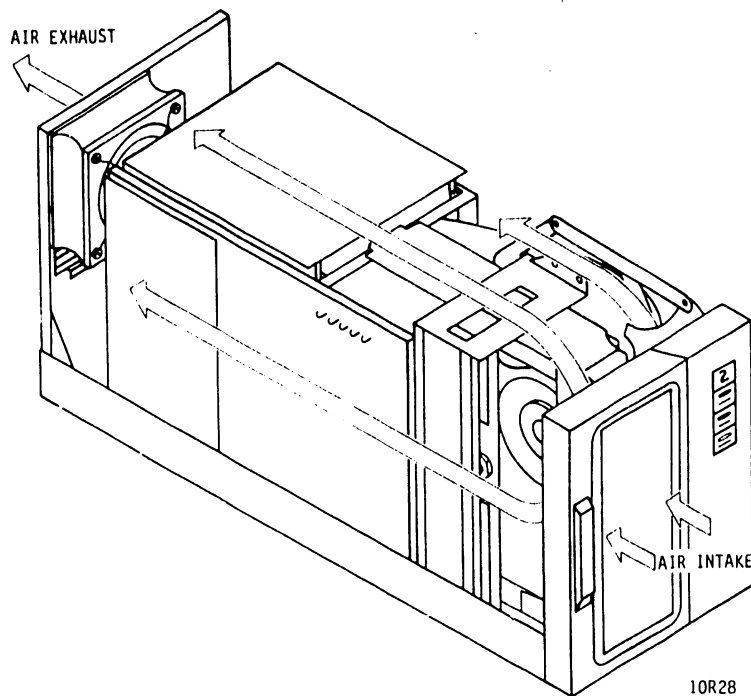


Figure 1-9. Drive Air Flow System

The interface consists of the I/O cables and the logic required to process the signals sent between drive and controller.

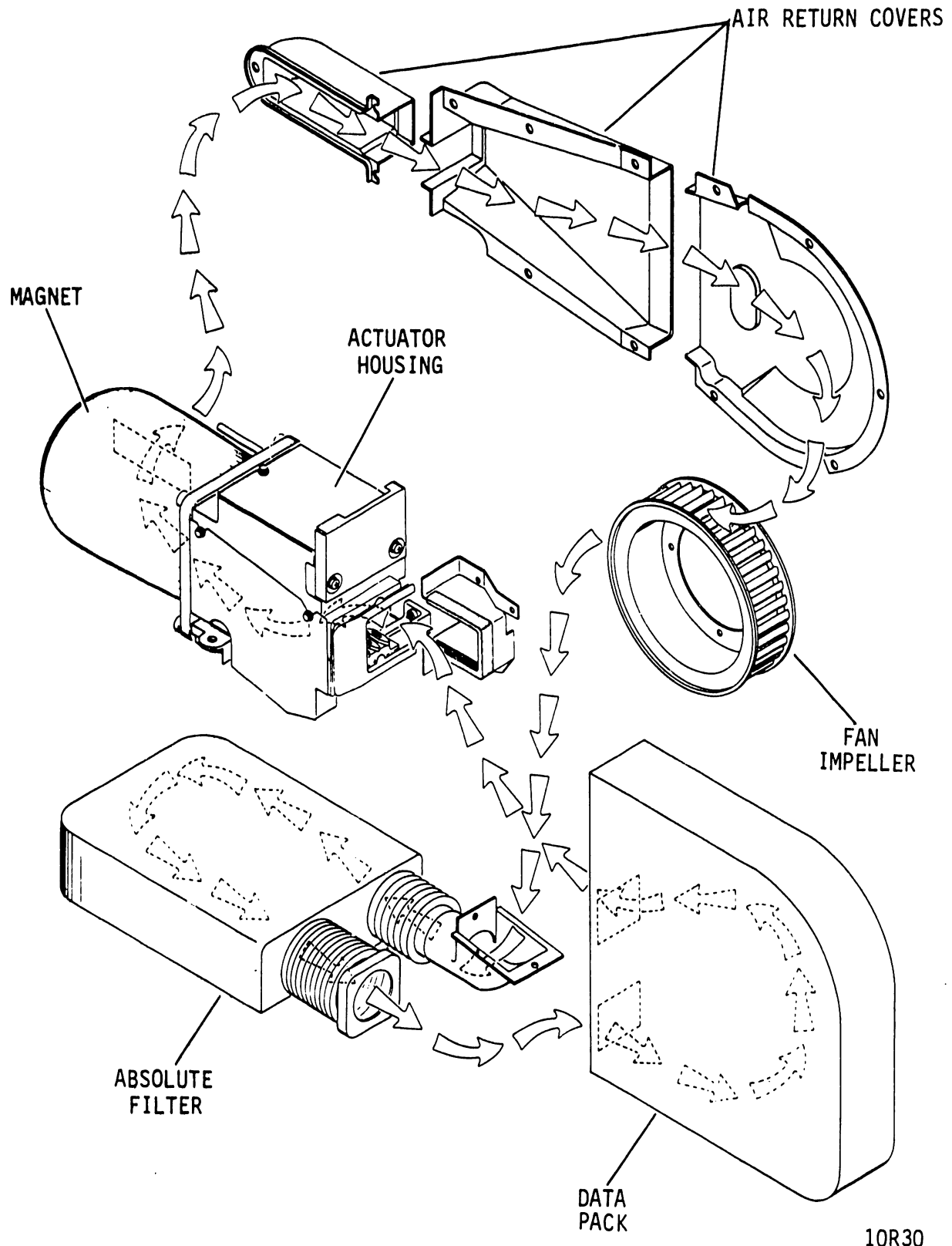
The following discussion describes both the I/O cables and I/O signal processing.

I/O CABLES

The drive has two I/O cables per channel, consisting of an A cable and a B cable. These cables contain all the lines going between the drive and controller.

The A cable carries commands and control information to the drive and status information to the controller.

The B cable carries read/write data, clock, and status information between drive and controller. Figure 1-11 shows all lines (except those not used) in the A and B cables. The functions of each of these lines is explained in table 1-1.



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Figure 1-10. Closed Loop Air Flow

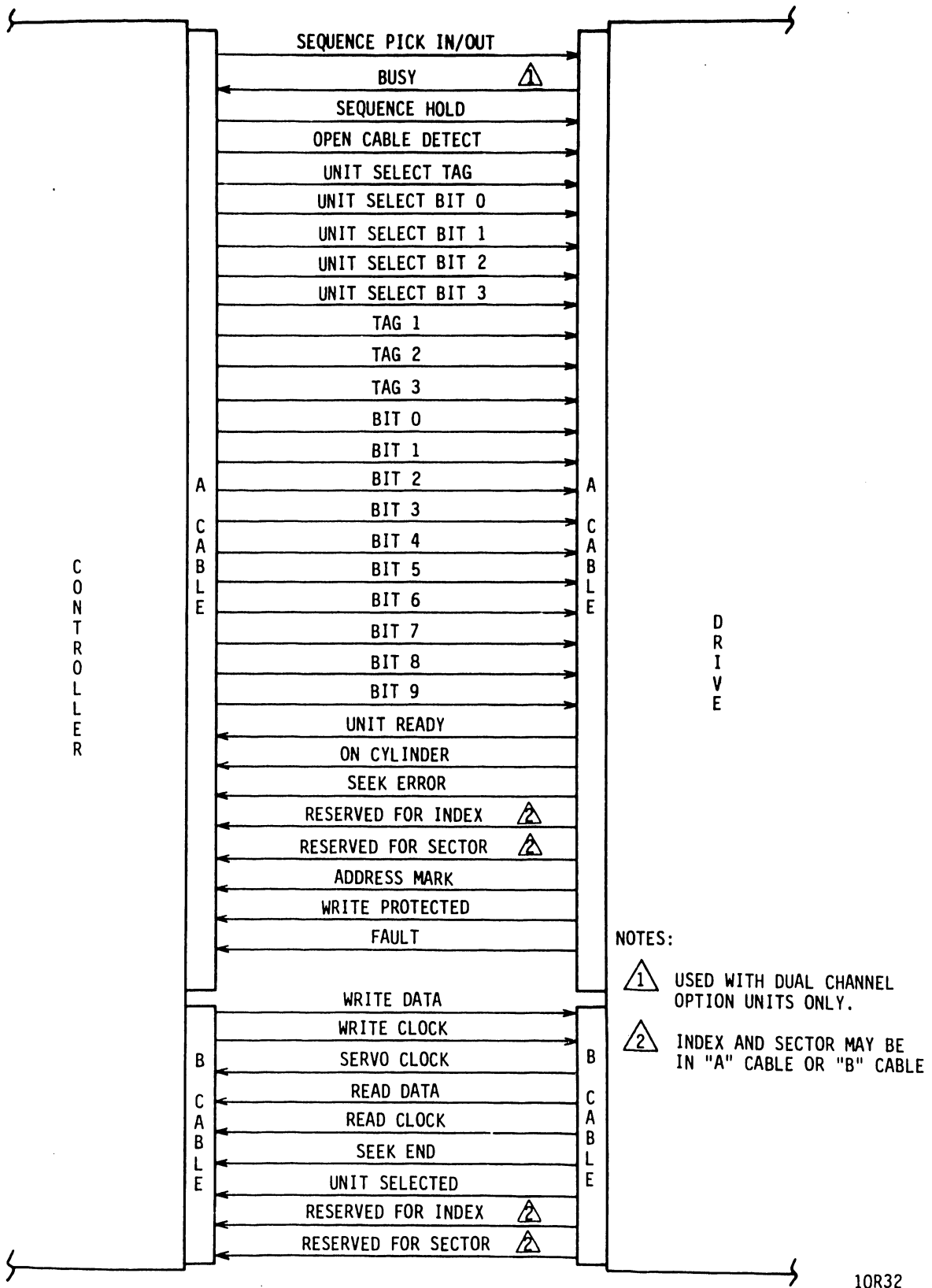


Figure 1-11. Interface Lines

TABLE 1-1. INTERFACE LINES

Signal	Meaning
Function: Power Up Sequencing	
<p>Sequence Hold</p> <p>Sequence Pick In</p> <p>Sequence Pick Out</p>	<p>A ground from the controller on this line starts the power on cycle when the drive's LOCAL/REMOTE switch is in the REMOTE position and the START switch on the operator panel is pressed.</p> <p>This line is not used in this drive.</p> <p>This line is connected to Sequence Pick In. It transfers the sequence pick immediately to the next drive connected in a daisy chain configuration.</p>
Function: Controller Selecting Drive	
<p>Unit Select Tag</p>	<p>This signal gates Unit Select lines into logical number compare circuit. Unit is selected after 600 ns (maximum) internal time lapse. Drive will not process commands until selected.</p> <p>When the Unit Select Tag is accompanied by Bus Bit 9 active, this indicates a priority select status in dual channel systems. The drive is unconditionally selected and reserved by the channel issuing this command provided that both channels are enabled and a priority select condition does not exist on the other channel.</p>
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Unit Select Bits 0, 1, 2, and 3	A binary code is placed on these four lines to select a drive. The binary code must match the logical address of the drive determined by the logical address plug inserted in the operator panel. Drives can be numbered 0 through 7. Bit 3 must be inactive for a unit selection to occur.
Unit Selected	This signal indicates the drive has accepted a Unit Select request. This line must be active before drive will respond to any command from controller.
Open Cable Detect	A voltage is supplied by the controller to override the bias voltage at drive receiver. If the A cable is disconnected or if controller power is lost, unit selection and/or controller commands are inhibited.
Function: Drive Indicates Operational Status	
Unit Ready	Unit Ready indicates that the drive is up to speed, that the servo head is positioned on cylinder, and that no fault condition exists.
Index	This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero.
Sector	This signal is derived from the servo tracks. The number of sector signals that occur for each revolution of the disk is selected by switches on the Control board.
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Busy	Used only in dual channel drives, this signal is generated when a controller attempts to select or reserve a drive that has already been selected and/or reserved by the other controller. This signal is sent to the controller attempting the selection.
Write Protected	This signal indicates that the drive write circuits are disabled. The write protect mode is enabled by switches on the Control board and the operator panel, by an interlock switch activated by a write-protected data pack, or by a fault condition. Attempting to write while the write protect mode is active results in a fault condition.
On Cylinder	This signal indicates that the servo head is positioned at a track. This line goes inactive if the positioner drifts off cylinder.
Seek End	This signal indicates either an on cylinder status or seek error status resulting from a seek operation that has terminated.
Seek Error	<p>This signal indicates that the drive was unable to complete a seek within 250 ms, that the positioner has moved outside the recording field, or that the drive was commanded to seek beyond cylinder 822.</p> <p>The seek error can be cleared by an RTZ command or by a power up operation.</p>
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
<p>Fault</p> <p>Address Mark</p>	<p>When this line is active, it indicates that one or more of the following faults exist:</p> <ul style="list-style-type: none"> • First Seek fault • DC voltage fault • Write fault • Write or read attempted while off cylinder • Write gate during a read operation <p>When an address mark has been found, this line goes high.</p>
<p>Function: Controller Sends Commands to Drive</p>	
<p>Bits 0 through 9 (Bus Lines)</p> <p>Tag 1 (Cylinder Select)</p>	<p>These ten lines carry data to the drive. The meaning of the data is a function of the active tag line.</p> <p>This tag line gates the data on the bus lines to the drive Cylinder Address register. The bus bits have the significance listed below.</p> <p>Bus bits 0-9, with the value shown below, encode the cylinder address for the seek operation. Cylinder addresses above 822 are illegal and will encode a seek error.</p>
<p>Table Continued on Next Page</p>	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning		
Tag 3 (Contd)	<u>Bus Bit</u>	<u>Name</u>	<u>Function Performed</u>
	0	Write Gate	Enables write driver. Not accepted if there is a seek error or fault status.
	1	Read Gate	Enables read circuitry. Leading edge triggers the read chain circuit to synchronize on an all zeros pattern. Not accepted if there is a seek error or fault status.
	2	Servo Offset Plus	Offsets the positioner 100 microinches toward the spindle from the on cylinder position. Disables On Cylinder for 2.75 ms.
	3	Servo Offset Minus	Offsets the positioner 100 microinches away from the spindle from the on cylinder position. Disables On Cylinder for 2.75 ms.
	4	Fault Clear	A pulse sent to drive that clears the Fault flip-flop provided that the fault condition no longer exists.
Table Continued on Next Page			

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning		
Tag 3 (Contd)	<u>Bus Bit</u>	<u>Name</u>	<u>Function Performed</u>
	5	Address Mark Enable	When this signal occurs with a Write Gate, an address mark is written. When this signal occurs with a Read gate, an address mark search is initiated.
	6	RTZ	A pulse sent to the drive to move the positioner to track zero. It also resets the Head Address register, Cylinder Address register, and Seek Error flip-flop.
	7	Data Strobe Early	Enables the read comparator to strobe the data at a time earlier than nominal.
	8	Data Strobe Late	Enables the read comparator to strobe the data at a time later than nominal.
9	Release	Used with dual channel option only, it clears channel reserved and channel priority select reserve status. (Refer to Unit Selection discussion.)	
Table Continued on Next Page			

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Functions: Read, Write, and Clocks	
Read Data	This line transmits data recovered from the disk. This data is transmitted in NRZ form to the controller.
Read Clock	This clock is derived from, and is synchronous with, the detected data. Read Clock defines the beginning of a data cell and is transmitted continuously.
Write Data	This line transmits NRZ data from the controller to the drive for recording on the disk surface with 2-7 encoding.
Write Clock	This clock is the Servo Clock retransmitted to the drive during a write operation. Write Clock must be synchronized to the NRZ data and must be transmitted 250 ns prior to Write Enable.
Servo Clock	Servo Clock is a phase-locked 9.67 MHz signal generated from the servo track tribits. Servo Clock is continuously transmitted.

I/O SIGNAL PROCESSING

I/O signals from the controller initiate and control all drive operations except local power on. The I/O signals are sent to receivers in the drive and are routed from the receivers to the appropriate drive logic. The drive in turn sends information concerning the operation back to the controller via the drivers. Figure 1-12 shows the basic logic involved in the routing of the I/O signals.

Certain I/O signals cannot be transmitted or received unless the drive is selected. These signals include the tag and bus bit signals from the controller and the status bits to the controller.

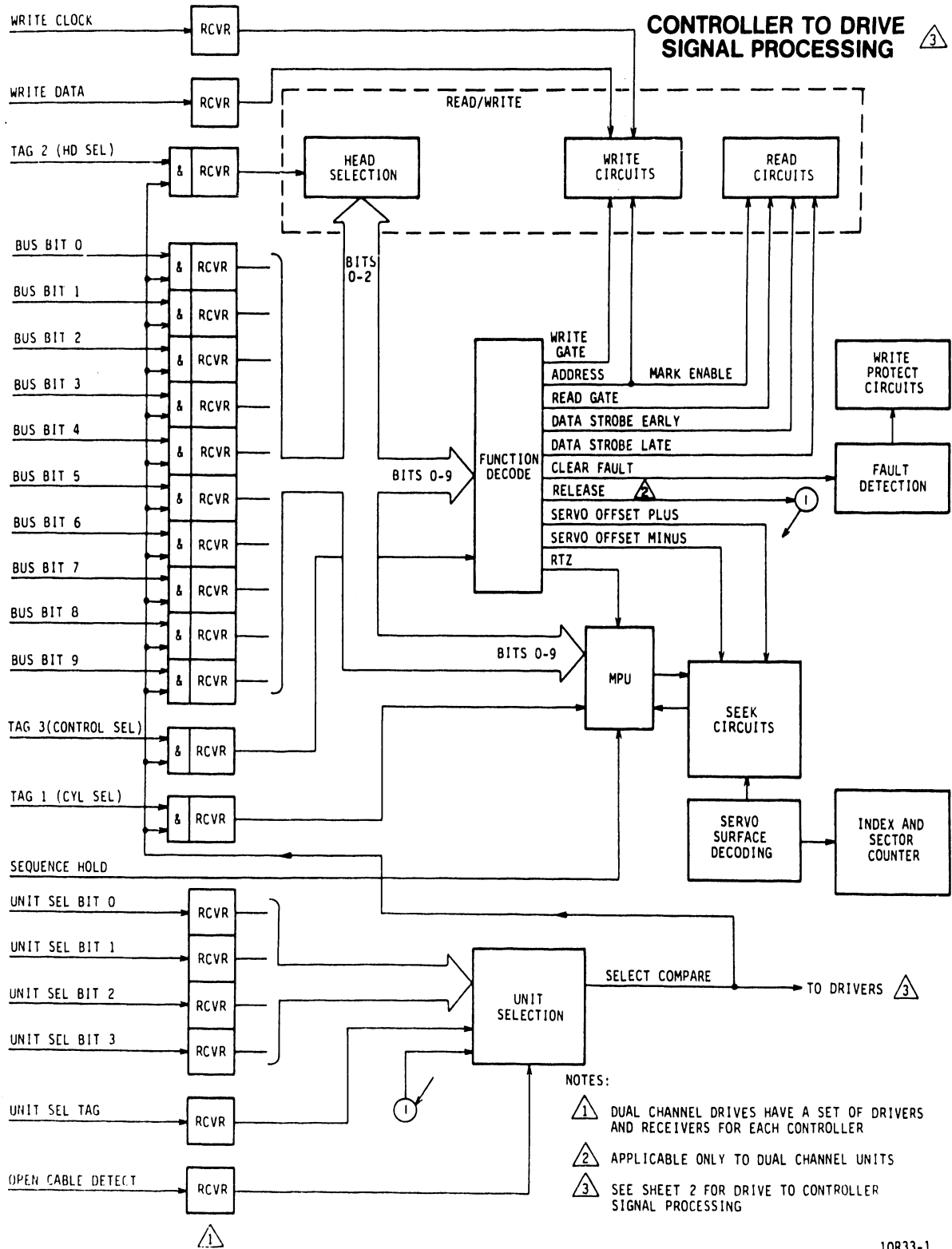
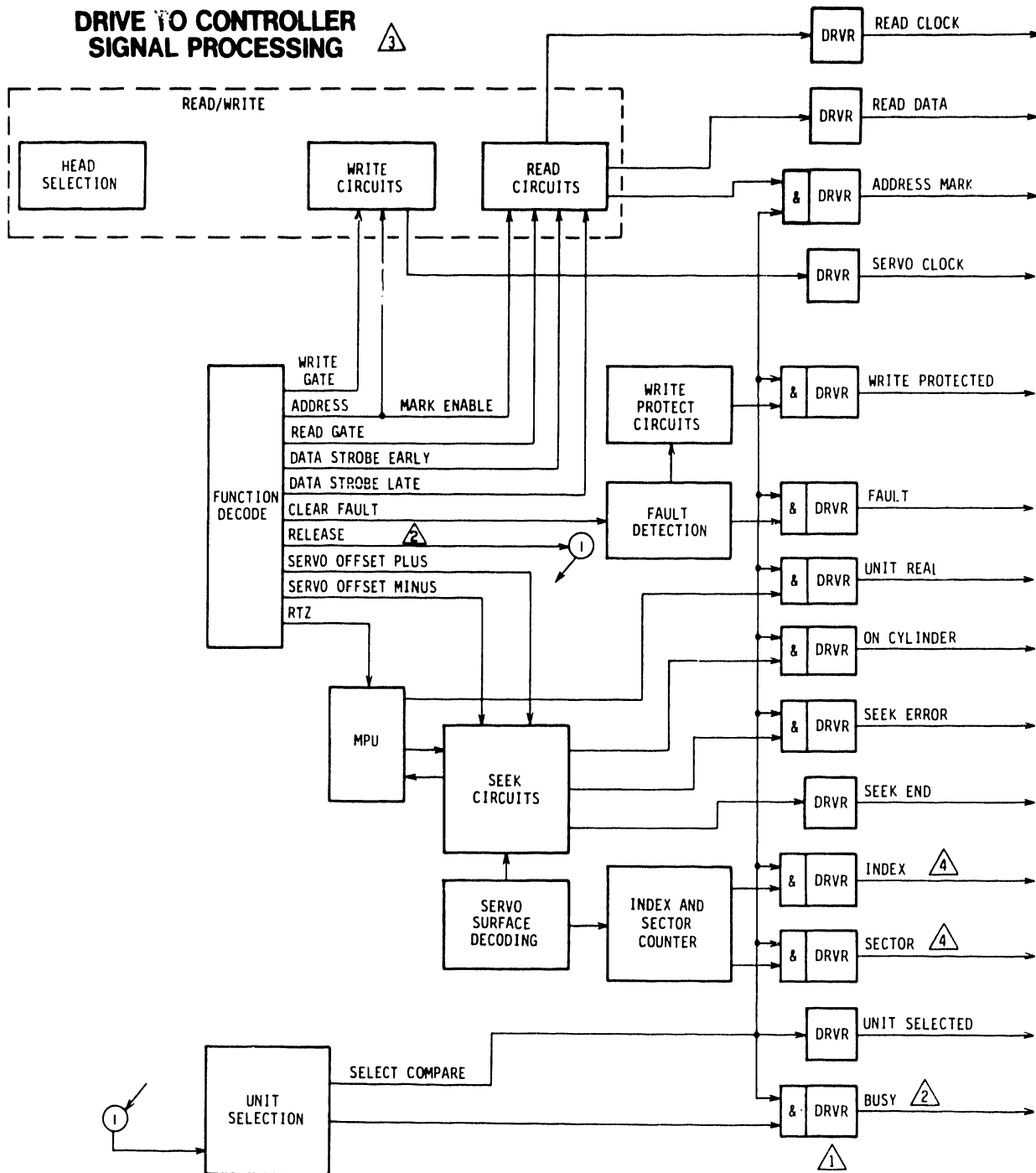


Figure 1-12. I/O Signal Processing (Sheet 1 of 2)

DRIVE TO CONTROLLER SIGNAL PROCESSING ³



NOTES:

- ¹ DUAL CHANNEL DRIVES HAVE A SET OF DRIVERS AND RECEIVERS FOR EACH CONTROLLER
- ² APPLICABLE ONLY TO DUAL CHANNEL UNITS
- ³ SEE SHEET 1 FOR CONTROLLER TO DRIVE SIGNAL PROCESSING
- ⁴ INDEX AND SECTOR SIGNALS ARE SENT CONTINUOUSLY WHEN INDEX/SECTOR JUMPER PLUG IS IN "B" POSITION

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Figure 1-12. I/O Signal Processing (Sheet 2)

All commands (except unit select) are sent to the drive via the tag and bus bit lines. The tag lines define the basic operation to be performed and the bus bits further define and modify the basic operation. Table 1-1 explains the functions of all tag and bus lines.

UNIT SELECTION

GENERAL

The drive must be selected before it will respond to any commands from the controller. This is the case because the tag and bus bit receivers, as well as certain drivers, are not enabled until the drive is selected.

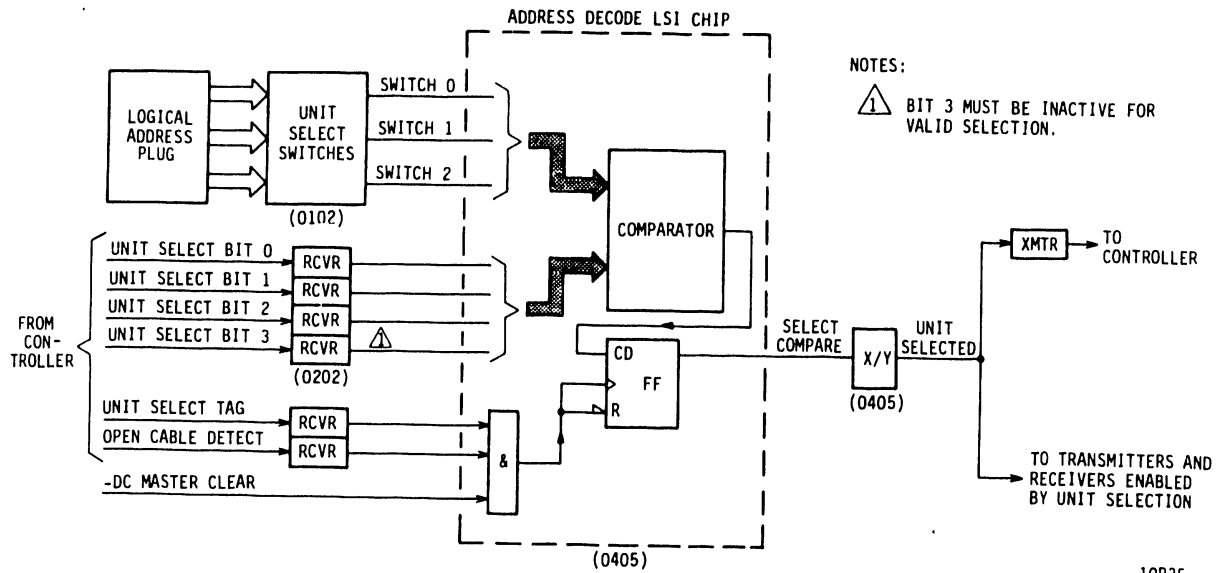
In both single and dual channel units, the select sequence is initiated by a Unit Select Tag signal from the controller. However, the sequence performed is different depending on whether a single or dual channel is being considered. Since only one controller can communicate with the drive at a time, dual channel logic must solve the problem of priority when more than one controller wants to select the drive at the same time. The following paragraphs describe both single and dual channel selection.

SINGLE CHANNEL UNIT SELECTION

The single channel unit select sequence (see figure 1-13) starts when the controller sends the Unit Select Tag accompanied by a logical address on the four unit select lines.

When the drive recognizes the Unit Select Tag, it compares its own logical address (as indicated by the logical address plug) to the address sent by the controller. The drive's logical address is determined by the logical address plug which fits into the operator panel. Depending on the plug used, this address can be any number from 0 to 7. If no plug is used, the number is 7.

If the address sent by the controller is the same as that of the drive and the Open Cable Detect signal is active (indicating the A cable is connected and controller has power), the drive enables its Select Compare signal.



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Figure 1-13. Unit Select Logic (Single Channel)

The Select Compare signal enables the receivers and drivers to the controller and also enables the Unit Selected signal. The drive is now ready to respond to further commands from the controller.

DUAL CHANNEL UNIT SELECTION

General

Dual channel drives are connected to, and can be selected by, either of two controllers. However, because the drive is capable of responding to only one controller at a time, the controllers must compete for use of the drive. For this reason, there are functions associated with dual channel selection that are not necessary when selecting single channel units.

The functions controlling dual channel selection are as follows:

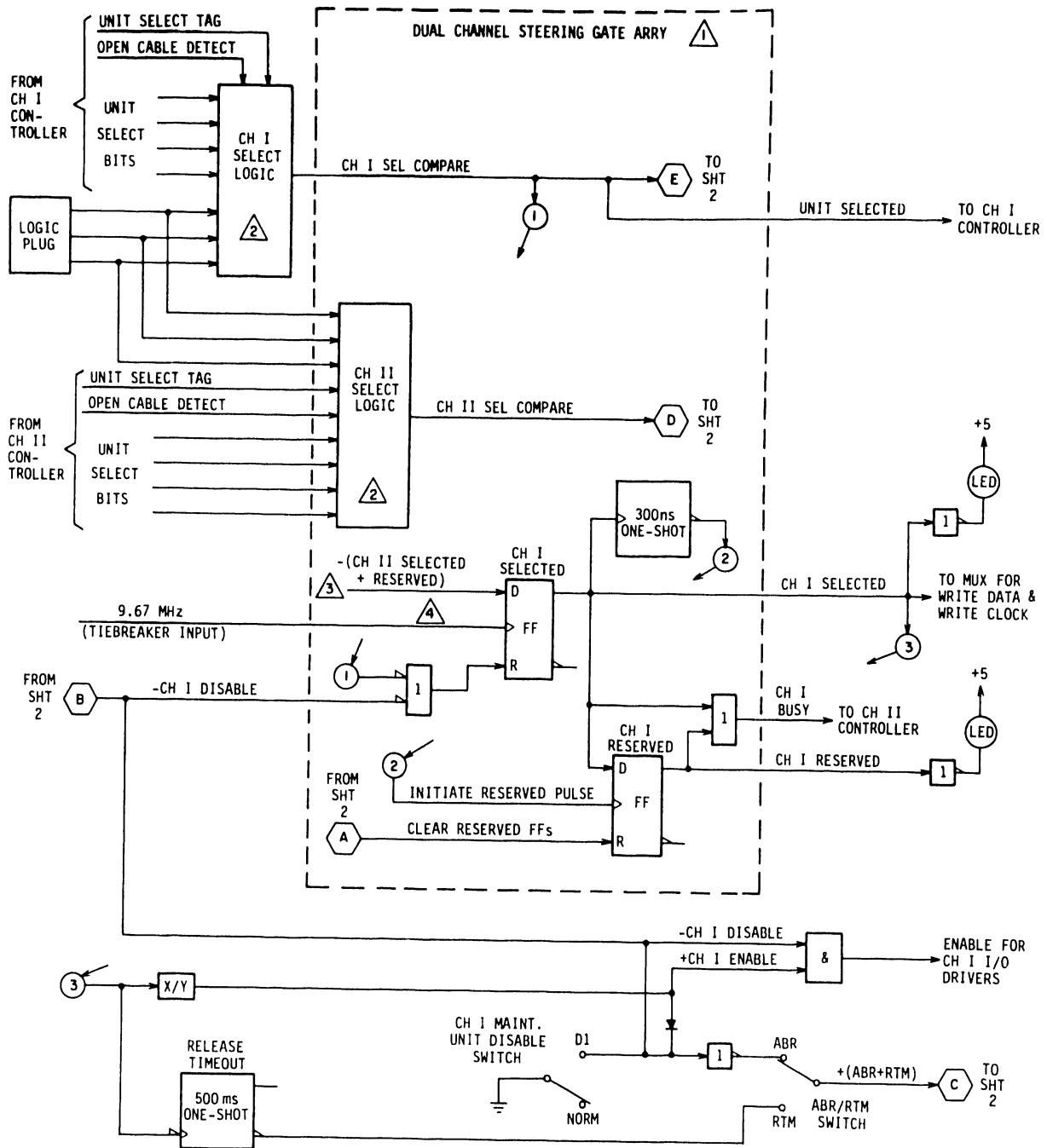
- Select - Logically connects the drive to the controller, thus enabling it to respond to commands from the selecting controller.
- Reserve - Reserves the drive so it can be selected at any time by the reserving controller, but prevents it from being selected by the other controller.
- Release - Releases drive from reserved condition.
- Priority Select - Allows controller to force select the drive by disabling the interface to the controller having the drive selected or reserved.
- Maintenance Disable - Allows disabling either channel interface during maintenance.

The following discussions describe each of these functions. It should be noted that because these functions are basically the same regardless of which channel is involved, they are described only as they relate to Channel I. Figure 1-14 shows the select logic associated with channel I selection and table 1-2 describes the major elements on this figure. Figure 1-15 is a flowchart of the dual channel unit select and reserve functions.

Select and Reserve Function

The drive is both selected and reserved during the same sequence and this sequence is initiated by a Unit Select Tag accompanied by a logical address. However, the drive can be successfully selected and reserved only if none of the following conditions exist:

- Drive is already selected and reserved by other controller.
- Drive is not selected but is reserved by other controller.
- Channel to drive attempting selection has been disabled by either a priority or maintenance disable function.

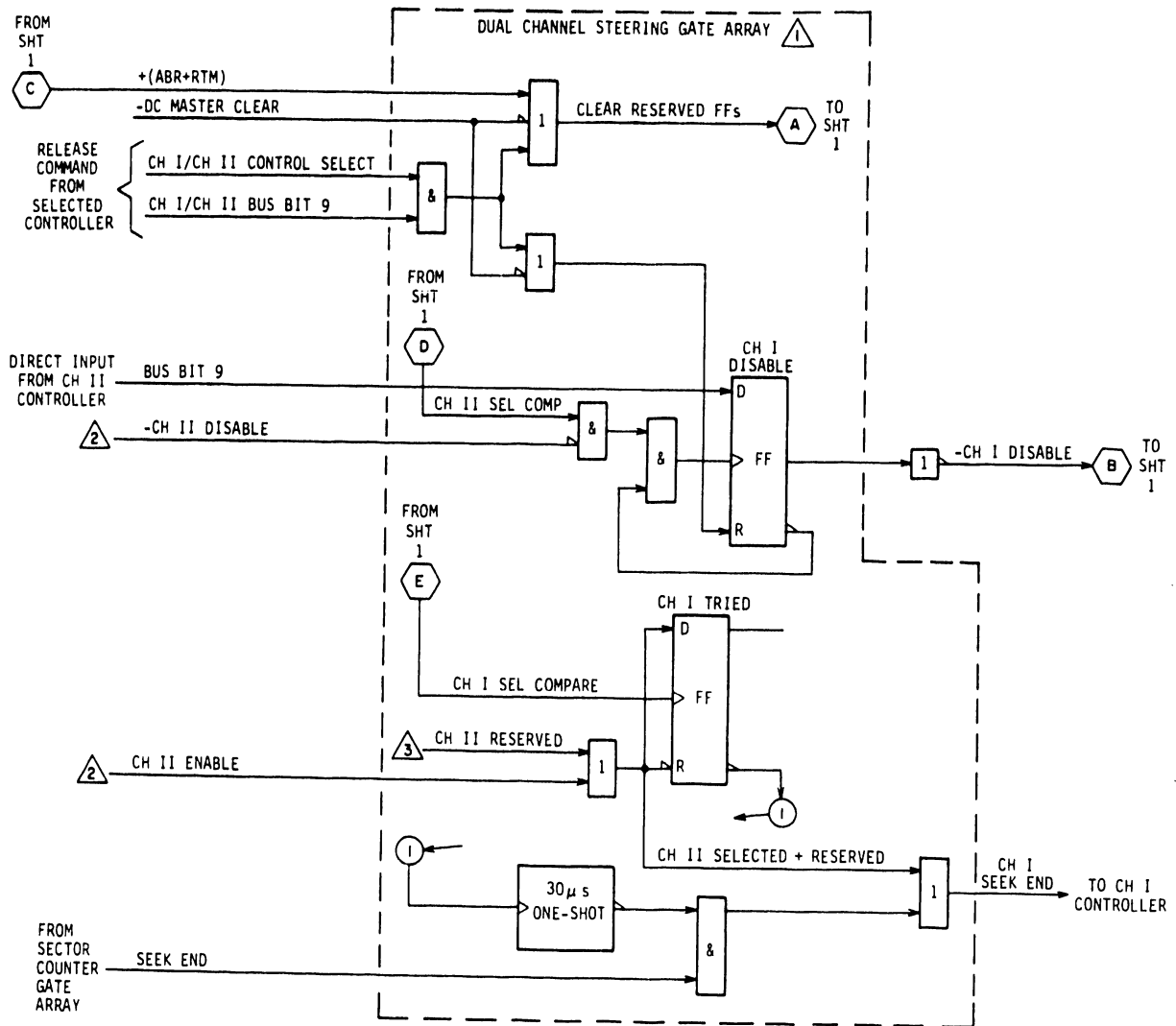


NOTES:

- ① GATE ARRAY CIRCUITS ARE SHOWN ON SHEET 2 ALSO. FOR EACH CHANNEL I FF SHOWN, THERE IS A COMPARABLE CHANNEL II FF.
- ② FOR DETAILS, SEE DIAGRAM FOR SINGLE CHANNEL UNIT SELECTION.
- ③ SIGNAL DERIVED FROM CH II SELECTED FF AND CH II RESERVED FF.
- ④ INVERTED TIEBREAKER SIGNAL CLOCKS CH II SELECTED FF.

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Figure 1-14. Channel I Dual Channel Logic (Sheet 1 of 2)

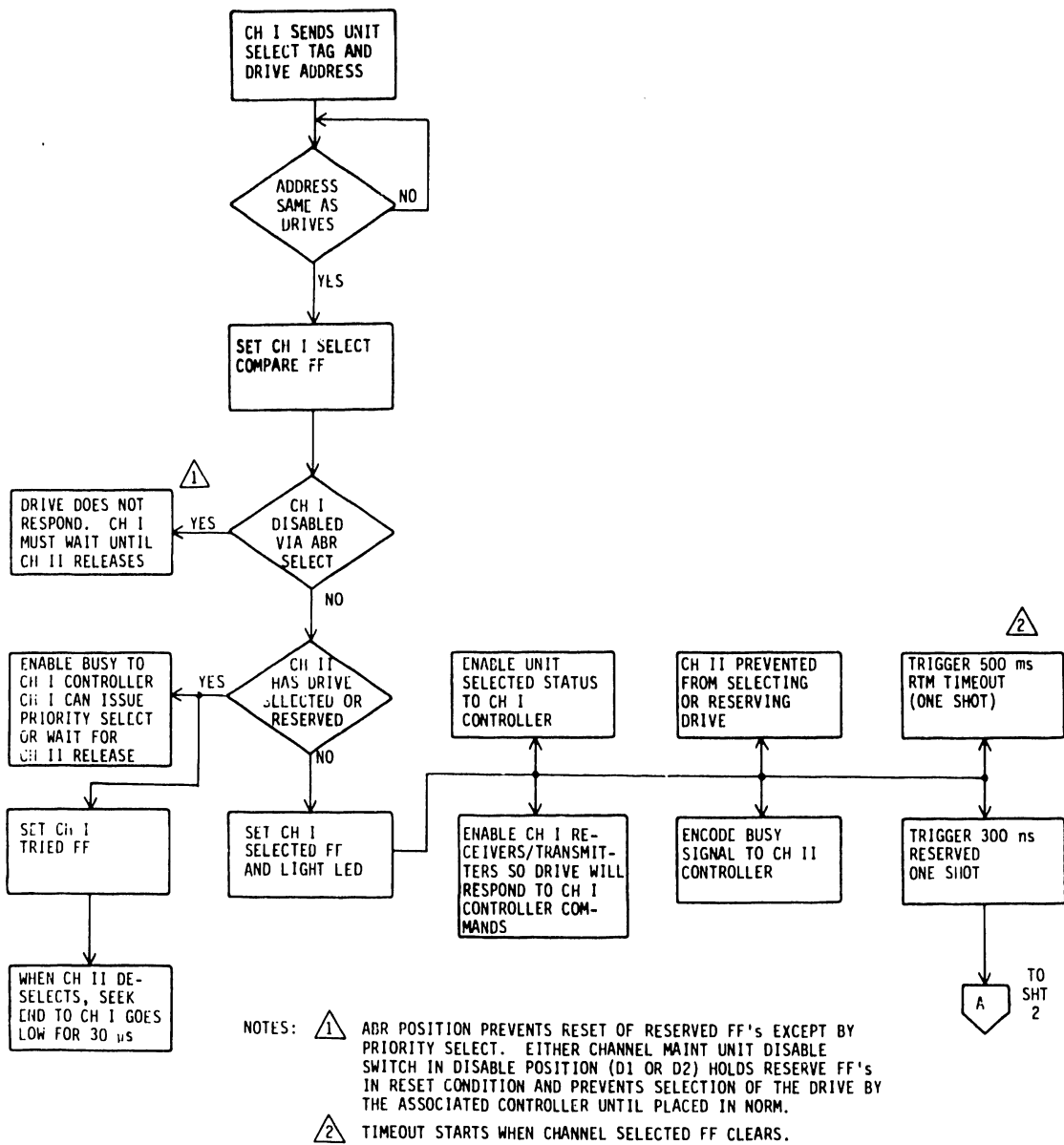


NOTES:

- ① GATE ARRAY CIRCUITS ARE SHOWN SHEET 1 ALSO. FOR EACH CHANNEL I FF SHOWN, THERE IS A COMPARABLE CHANNEL II FF.
- ② SIGNALS DERIVED FROM CHANNEL II OUTPUTS OF GATE ARRAY.
- ③ SIGNAL DERIVED FROM CH II RESERVED FF.

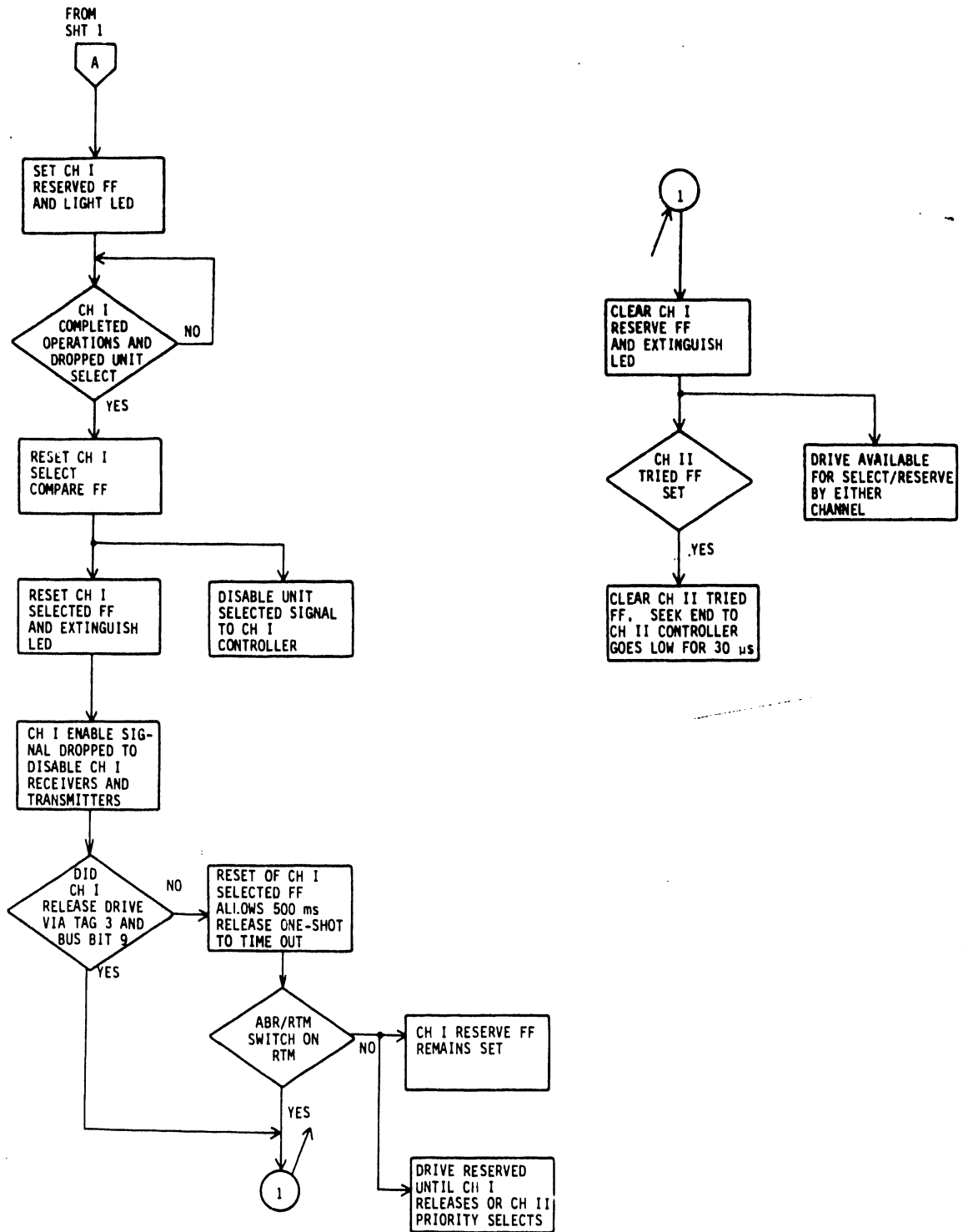
10R36-2

Figure 1-14. Channel I Dual Channel Logic (Sheet 2)



10R37-1

Figure 1-15. Dual Channel Selection Flowchart (Sheet 1 of 2)



10R37-2

Figure 1-15. Dual Channel Selection Flowchart (Sheet 2)

TABLE 1-2. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS

Element*	Function
ABR/RTM Switch	Determines whether the drive will be in ABR (absolute reserve) or RTM (reserve timeout) mode. If switch is in RTM position, drive is released from reserved condition 500 ms (nominal) after being deselected. If switch is in ABR position, drive remains reserved until it receives either a release or priority select command.
Release Timeout One Shot	Deselecting drive causes this one shot to generate a 500 ms (nominal pulse). If drive is in RTM mode the trailing edge of this pulse clears the reserved FF.
Channel I Disable FF	Sets if drive receives Priority Select command. This causes drive to be selected and reserved for controller issuing command and disables channel to other controller.
Channel I Maintenance Unit Disable Switch	Disables channel I whenever it is set to DI (disable) position. It must be in NORM position during normal operations.
Channel I Reserved FF	Sets during select and reserve sequence. When set it keeps drive reserved to channel I until channel I releases or channel II issues a Priority Select command.
Channel I** Selected FF	Sets during select and reserve sequence and enables drivers and receivers to channel I controller.
Channel I Select and Compare Logic	Compares logical address of drive with that sent by controller (see Single Channel Unit Selection).
Table Continued on Next Page	

TABLE 1-2. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS (Contd)

Element*	Function
Initiate Reserved Pulse	Generates 300 ns pulse whenever Select Compare signal goes true. Leading edge of this pulse clocks Channel I and Channel II Reserve FF.
Channel I Select Tried FF	Sets if channel I tries to select and reserve drive while it is already selected and/or reserved by channel II. When drive is deselected and released by Channel II, this FF clears and thereby triggers the Select Tried one shot.
Select Tried One Shot	Generates 30 microsecond pulse whenever either Tried FF clears. This pulse is sent to controller (associated with the Channel Tried FF that triggered the one shot) via the Seek End line.
<p>* Includes only those elements directly concerning channel I and shown in figure 1-14.</p> <p>**The Channel Selected FF's are alternately clocked by the 9.67 MHz clock signal to prevent simultaneous selection.</p>	

The following paragraphs describe how the drive is initially selected and also how it responds to a Unit Select Tag when it is selected, reserved, or disabled.

Assuming the drive is available (not selected, reserved, or disabled) and it receives a Unit Select Tag and logical address from the controller on channel I, it compares the address received with that indicated by its logical address plug. If the two addresses are the same, the drive enables the Channel I Select Compare signal. The logic used to generate this signal is identical to that used in the single channel units (refer to figure 1-13).

The Select Compare signal causes the Channel I Selected FF to set, thereby enabling the receivers and drivers to the Channel I controller and triggering the 300 ns Reserve one-shot. The output pulse from this one-shot clocks and sets the Channel I Reserved FF. With these FFs set, the drive sends Unit Selected to the channel I controller indicating that it is ready to accept further commands.

Providing channel II does not issue a priority select command (see Priority Select Function discussion), the drive remains selected to channel I until the controller on channel I drops its Unit Select Tag or changes the logical address to another drive. At this time, the drive's Channel I Selected FF clears, thus disabling the drive drivers and receivers for that channel. This also disables the Unit Selected signal thus informing the controller that the drive will no longer respond to commands. However, the drive remains reserved to channel I (allowing channel I to reselect while preventing channel II from selecting) until the Channel I Reserve FF is also Clear. This is cleared by either a release or priority select function (refer to these discussions).

If channel I attempts to select and reserve the drive while it is selected and reserved by channel II, the Channel I Select Compare signal is still generated as during the initial select and reserve sequence. However, the Channel I Select and Reserve FFs do not set, and therefore the attempt is unsuccessful. The drive still sends the Channel I Unit Selected signal to the controller, but, in this case, it is accompanied by the Channel I Busy signal. The Busy signal indicates that the drive is being used by channel II.

The drive also sets its Channel I Tried FF, thus recording the unsuccessful attempt. When the drive is no longer selected or reserved by channel II, this FF clears, causing Seek End to the channel I controller to go low for 30 microseconds. This informs the controller that the drive is no longer selected or reserved.

If the channel I controller tries to select the drive while channel I is disabled (either by a priority select or maintenance disable function), the attempt's unsuccessful and no response is sent back to the channel I controller.

Release Function

The release function will release the drive from either a reserved or priority selected condition. There are two types of release functions:

- Timeout release pulse
- Release command

The timeout release pulse is capable of releasing the drive from only the reserved condition. This pulse is generated by the 500 ms Timeout Release one-shot and releases the drive by clearing the Reserve FF. The pulse is triggered when the drive is selected (Select FF sets) and times out 500 ms after the drive is deselected (Select FF clears).

Whether or not the one shot has any effect on the Release FF depends on the position of the ABR/RTM switch. If this switch is in the RTM (reserve timeout) position, the FF clears when the one-shot times out, thus making the drive available to the other channel. However, if this switch is in ABR (absolute reserve) position, the one-shot has no effect on the FF and the drive remains reserved.

A Release command will release the drive from both the reserved and priority selected conditions. This command is initiated by the reserving and/or priority selecting controller when it issues a Tag 3 (Control Select) with Bus Bit 9 active. This clears the Reserve and Disable FFs and allows the other controller to select the drive.

Priority Select Function

If the drive is selected and reserved, the other controller can force selection by issuing a Priority Select command (Unit Select Tag accompanied by drive logical address and Bus Bit 9). This command will disable the channel to the controller presently using the drive and also select and reserve the drive to the controller issuing the Priority Select command.

For example if channel I has the drive and channel II wants to select, channel II issues a Priority Select command. In this case, the command sets the Channel I Disable FF which in turn results in clearing the Channel I Selected and Reserved FFs. It also sets the Channel II Selected and Reserved FFs, thereby selecting and reserving the drive for channel II.

Once the Disable FF is set, that channel (in this case channel I) is disabled until the other controller (in this case channel II) issues a command to clear it.

Maintenance Disable Function

It is also possible to disable either channel by setting the Maintenance Unit Disable switch for that channel (refer to figure 1-14) to the DI or DII position.

DRIVE SERVO SYSTEM

The drive writes data on and reads data from the disk data recording areas under the directions of the controller. These operations cannot be done randomly, however, for when the controller wishes to retrieve data, it must be able to find the exact location where that data has been stored. This problem is resolved by mapping the disks into discrete sections called "Tracks" which are narrow concentric bands that cover the entire circumference of the circle. The tracks are then further subdivided into equal areas called "Sectors".

After the controller has selected the unit with which it wishes to perform an operation, it must then direct the drive to the specific location on the data recording surface where it wants the operation to be performed. The operation of positioning the heads over the desired track is called a Seek operation. The drive servo system under the direction of the microprocessor unit (MPU) performs the Seek operation to position the heads by using information read from the servo surface by the servo head.

The data recording areas of each of the disks (5 surfaces total) are divided into 823 tracks, and these are assigned sequential number addresses from 0, which is located on the outer edge of the recording area, through 822 which is located on the inner edge of the data recording surface closest to the hub. Since there are five data recording surfaces, each with 823 tracks with addresses 0 through 822, the controller must select one of five possible tracks with the same address number. This further selection is done by assigning numbers to the data recording surfaces (and the heads associated with the disk surfaces) from 0 through 4.

Once a particular track is selected, the controller then further narrows down location selection by addressing one of five heads located at the selected track. Each track is subdivided into equal segments called "Sectors". This division is accomplished by the setting of a group of switches called Sector

switches (see the discussion called Sector Detection). When the controller has selected the unit, the track, and the head, then it waits for the particular sector(s) where it wishes to write (store) or retrieve (read) data. Another option for locating an area on a track to be operated upon is by writing an Address Mark at a specific location on the track, and then looking for the mark at the beginning of a read operation.

When the controller commands the drive to go to a track/head/sector where it wishes to perform a read or write operation, the drive servo system under the direction of the MPU performs the positioning (Seek) operation. The MPU program uses information read from the servo surface by the servo head to do the Seek operation. The following discussion will describe servo surface decoding and then describe seek functions.

SERVO SURFACE DECODING

GENERAL

The servo surface is a prerecorded disk surface in the data pack that provides three basic types of information to the drive electronics. Information from the servo surface is read by the servo head. The servo head is mounted on the same positioner as the data heads; thus, movements of the servo head across the servo surface correspond exactly to movements of the data heads across the data surfaces.

The three types of information available from the servo surface are as follows:

- Radial movement of the heads, indicated by the Position signal
- Rotational position of the disks, indicated by the Index signal
- Exact speed of the disks, indicated by the 1.612 MHz Clock signal.

The significance of each type of information for drive operation and the development of the basic feedback signals from the servo signal are presented under the following topics:

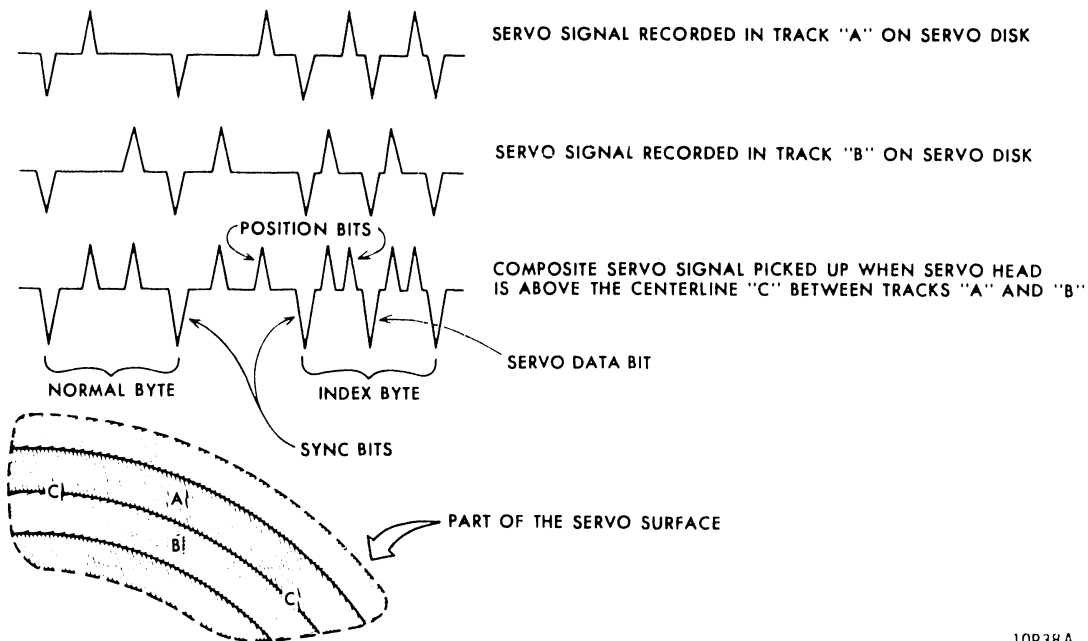
- Tribit Recording Scheme
- Servo Surface Format
- Tribit Decoder Circuit Operation

TRIBIT RECORDING SCHEME

Servo information consists of tribit coding on a series of concentric tracks located on the servo surface. The pattern of flux reversals alternates from track to track. Each track has eighty segments, each consisting of a special five-byte code followed by 79 normal servo bytes.

Unless the servo head is positioned directly over one servo track, the signal it detects is a composite of signals from the two tracks nearest the head. Figure 1-16 shows servo information recorded on two adjacent tracks and the signal detected when the servo head is halfway between the tracks.

In figure 1-16, two normal bytes are followed by an index byte. Each normal byte contains three bits -- a sync bit and two position bits. The sync bits have negative polarity and are recorded on all tracks. The position bits have positive polarity and are staggered from track to track so that they make separate contributions to the composite servo signal.



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Figure 1-16. Tribit Pattern

The index byte shown in figure 1-16 has a sync bit, an extra negative pulse called a servo data bit, and four position bits (twice the number of position bits in the normal byte). Adjacent tracks have coinciding sync and servo data bits as well as staggered position bits.

The special five-byte codes appearing 80 times per disk rotation contain different combinations of index bytes and normal bytes, depending on what the code designates on the disk surface. The different codes and their relation to the disk format are explained under the next topic. Each five-byte code is followed by 79 normal bytes. Thus, for each disk rotation, the servo head detects 80×84 or 6720 servo bytes.

The relative amplitude of the position bits within each servo byte is used to indicate the precise position of the servo head and, therefore, the data heads. When the data heads are located at the centerline of a data track, the servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent tribit signals. The amplitude of each position bit within a servo byte is proportional to the read coil overlap of the recorded servo tracks. With the head centered, each adjacent servo track contributes equal position bit amplitudes. As the head moves away from its centered position toward one servo track, the track being approached makes a greater contribution to the detected position bits than the one being left. The tribit demodulator converts this variation into the position signal used by the seek circuitry (see Position Demodulation).

Figure 1-17 shows the detected servo signal for three different servo head positions. In one of the three cases, the servo head is located on the centerline between two servo tracks, and the position bits have equal amplitudes. In the other two cases, the servo head is located on either side of the centerline, and the position bits have different amplitudes.

SERVO SURFACE FORMAT

The servo surface, through its encoding format, establishes the format of the disk data surfaces. The servo surface format divides the disk surfaces into four zones, an 823-track data zone, two guardbands, and a buffer zone. The guardbands indicate areas of the disk that cannot be used for recording of data. The outer guardband consists of 22 tracks on the outer portion of the disk, and the inner guardband consists of 80 tracks on the inner portion of the disk. The buffer zone consists of 4 tracks located between the outer guard band and

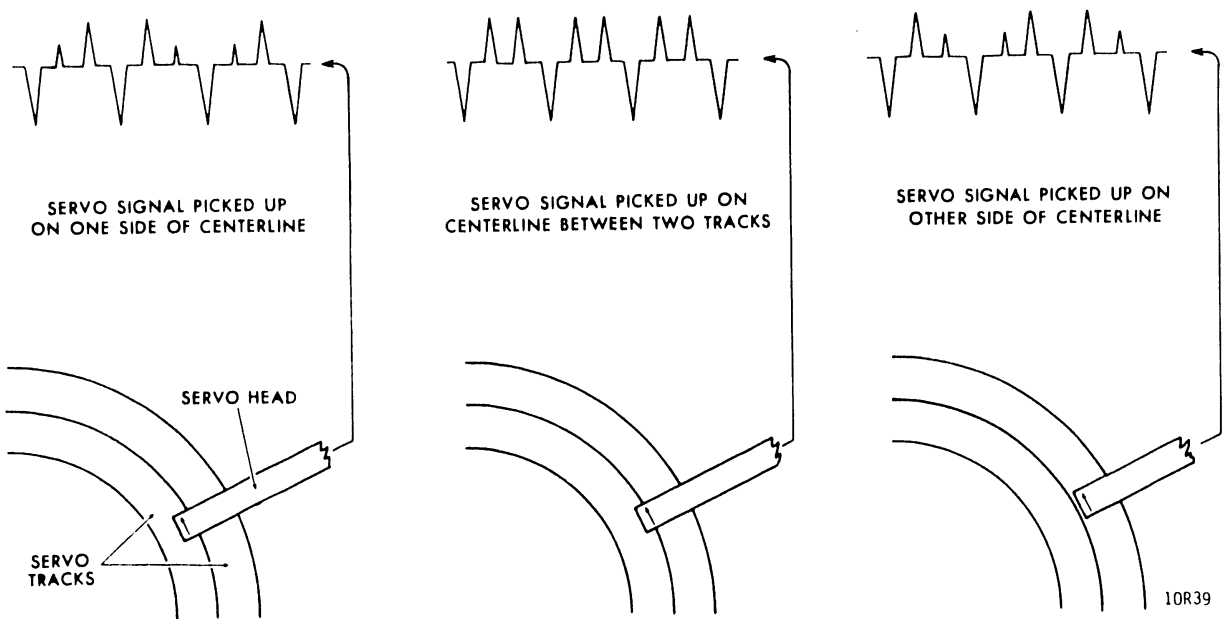
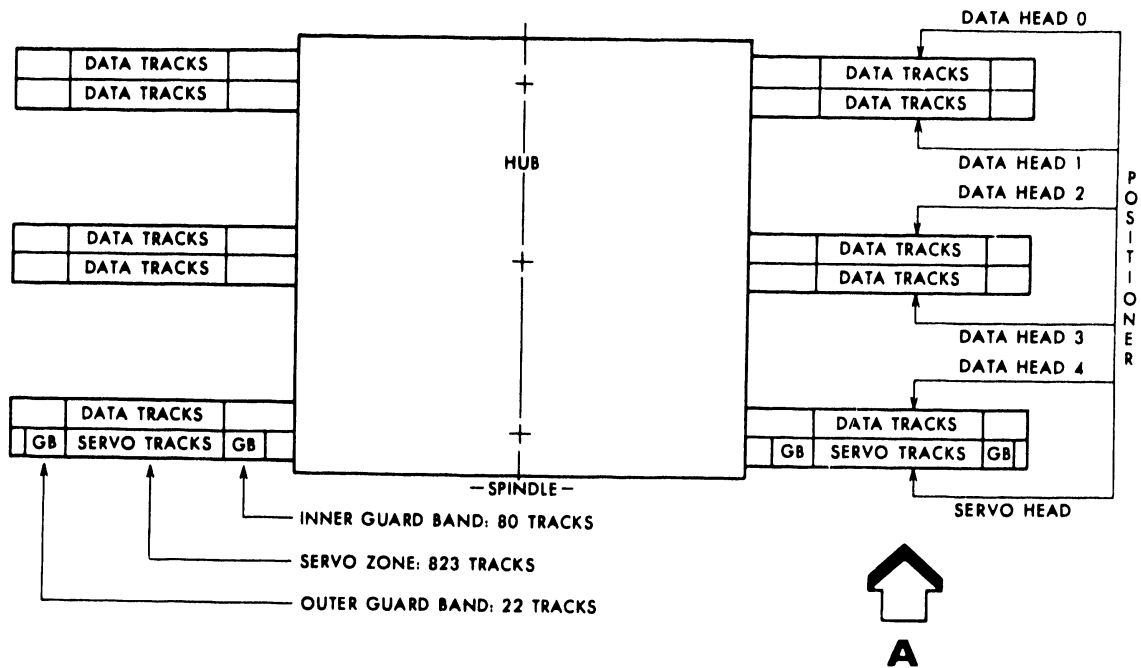


Figure 1-17. Tribit Signal Variations

the data zone. In addition, all four zones contain an encoded "reference line" which establishes the logical beginning of each track. When this reference is decoded, the drive sends the Index signal to the controller via the interface.

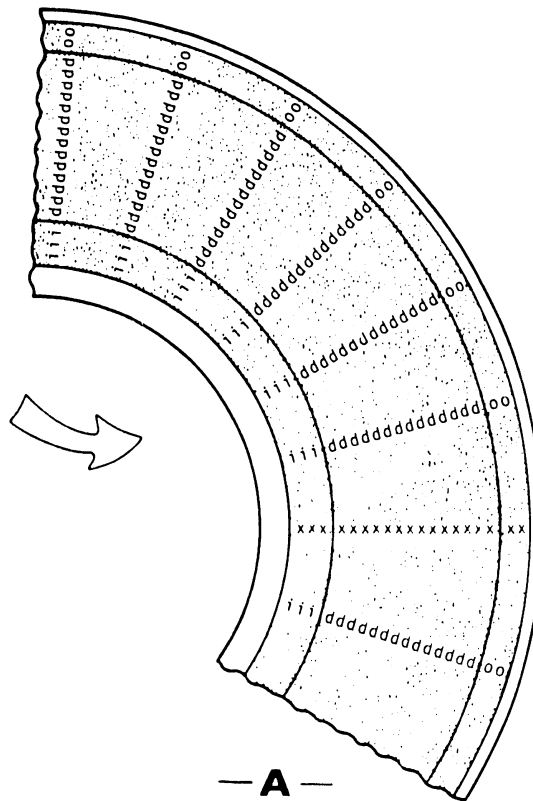
Figure 1-18 shows the positioning of heads on the data pack disk surfaces and explains, in the exploded portion of the drawing, how formatting information is encoded on the disk. As described in the Tribit Recording Scheme discussion, five-byte codes are used as format indicators. Each of the five bytes is either an index byte (labelled "1") or a normal byte (labelled "0"). With the two bytes labelled in this manner, each five-byte code can be designated as a five-bit pattern number. Thus, Index, with a pattern number of 11011, is encoded on the disk by two index bytes, followed by a normal byte and two more index bytes. This pattern marks the logical beginning of each servo track. The remaining 79 coded patterns spaced around each servo track depend on the zone for that track. The outer guardband is encoded with pattern 10111, the data zone and buffer zone with pattern 10101, and the inner guardband with pattern 11101.



FIVE-BYTE INDICATOR PATTERNS:

- x = INDEX . . . CODE 11011
- d = DATA ZONE . . . CODE 10101
- i = INNER GUARD BAND . . . CODE 11101
- o = OUTER GUARD BAND . . . CODE 10111
WITH 3-TRACK BUFFER ZONE
(CODE 10101) ADJACENT TO DATA ZONE

SHADED AREAS  BETWEEN INDICATOR PATTERNS SHOW TRACK SEGMENTS WHERE 79 NORMAL SERVO BYTES ARE RECORDED



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Figure 1-18. Servo Disk Format

Refer to the Index and Guardband Decoding discussion for a description of the circuitry that performs this decoding.

TRIBIT DECODER CIRCUIT OPERATION

General

Operation of the tribit decoder circuitry is discussed first in terms of its relation to other systems within the drive. This is followed by explanations of the individual functions performed by the decoder.

System Overview

Decoding the information present in the servo signal is essential for other functional areas of drive operation. Figure 1-19 is a functional block diagram showing signal flow between the tribit decoder and these other functional areas.

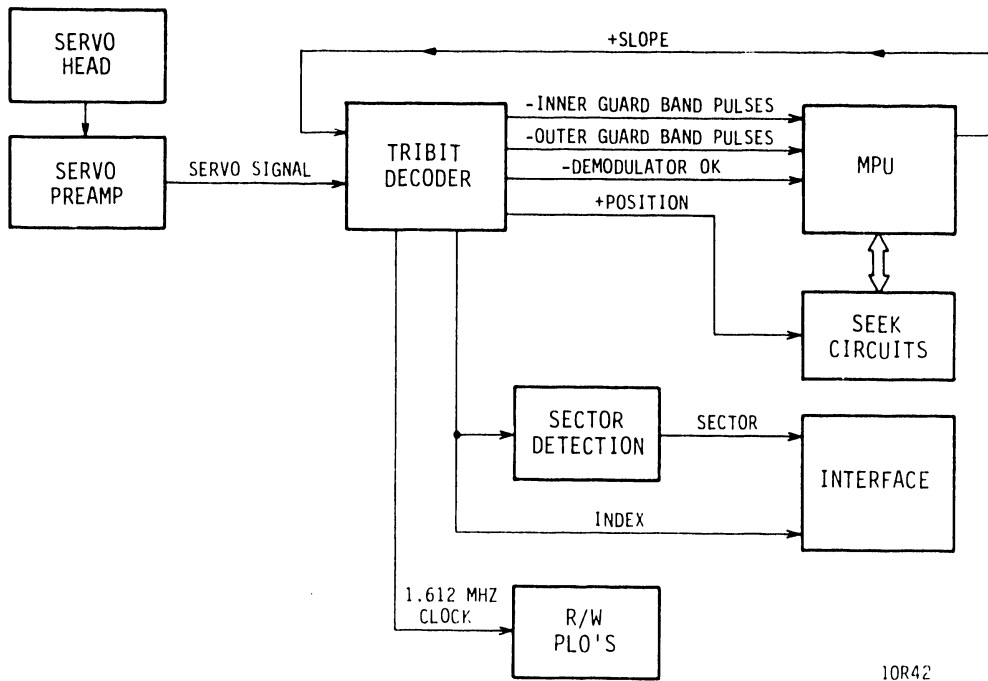


Figure 1-19. Tribit Decoder System Diagram

Inputs to the decoder come from the servo preamp and the MPU. The servo preamp amplifies the signal detected by the servo head. The +Slope signal, supplied by the MPU, sets up the phase of the decoded Position signal so that it can be used by the seek circuits.

The MPU monitors three output signals from the decoder. During normal seek operations, the servo head remains over the data zone. Thus, when the Inner or Outer Guard Band Pulses go active, the MPU reacts by altering the seek protocol. Improper decoder operation can affect seek reliability. For this reason, the MPU monitors the -Demodulator OK line.

Data transfers to and from the disk must be coordinated with respect to the rotational position of the disk. The Index signal is decoded and is input to the Sector Detection circuitry which, in turn, generates a given number of Sector pulses per disk rotation. The controller coordinates data transfers based upon the Index and Sector pulses transmitted to it via the interface.

The 1.612 MHz Clock from the decoder is used by the R/W PLO circuitry to form a 9.67 MHz Servo Clock. The Servo Clock operates at exactly six times the frequency of the 1.612 MHz Clock, and it tracks the rotational velocity of the disk. The controller transfers data to the disk in sync with the Servo Clock. This compensation in the rate of data transfers to the disk makes the written data pattern independent of disk speed.

The remaining topics within this discussion cover the operation of circuits within the tribit decoder. Figure 1-20 is a block diagram showing these circuits and their interconnections.

Position Demodulation

The control logic subdivides each tribit pattern into four equal intervals in order to regulate measurement of position bit amplitudes by the "A" and "B" Sample and Hold circuits. The Preset gate, active during the first interval, initializes both sampling circuits following the sync bit in each tribit pattern. The two Peak Detect gates, active in the second or third interval, select the position bit to be measured by each sampling circuit. In any two consecutive tribit patterns, a servo track provides one position bit in the second time interval and one position bit in the third time interval. The same two tribit patterns, derived from an adjacent servo track,

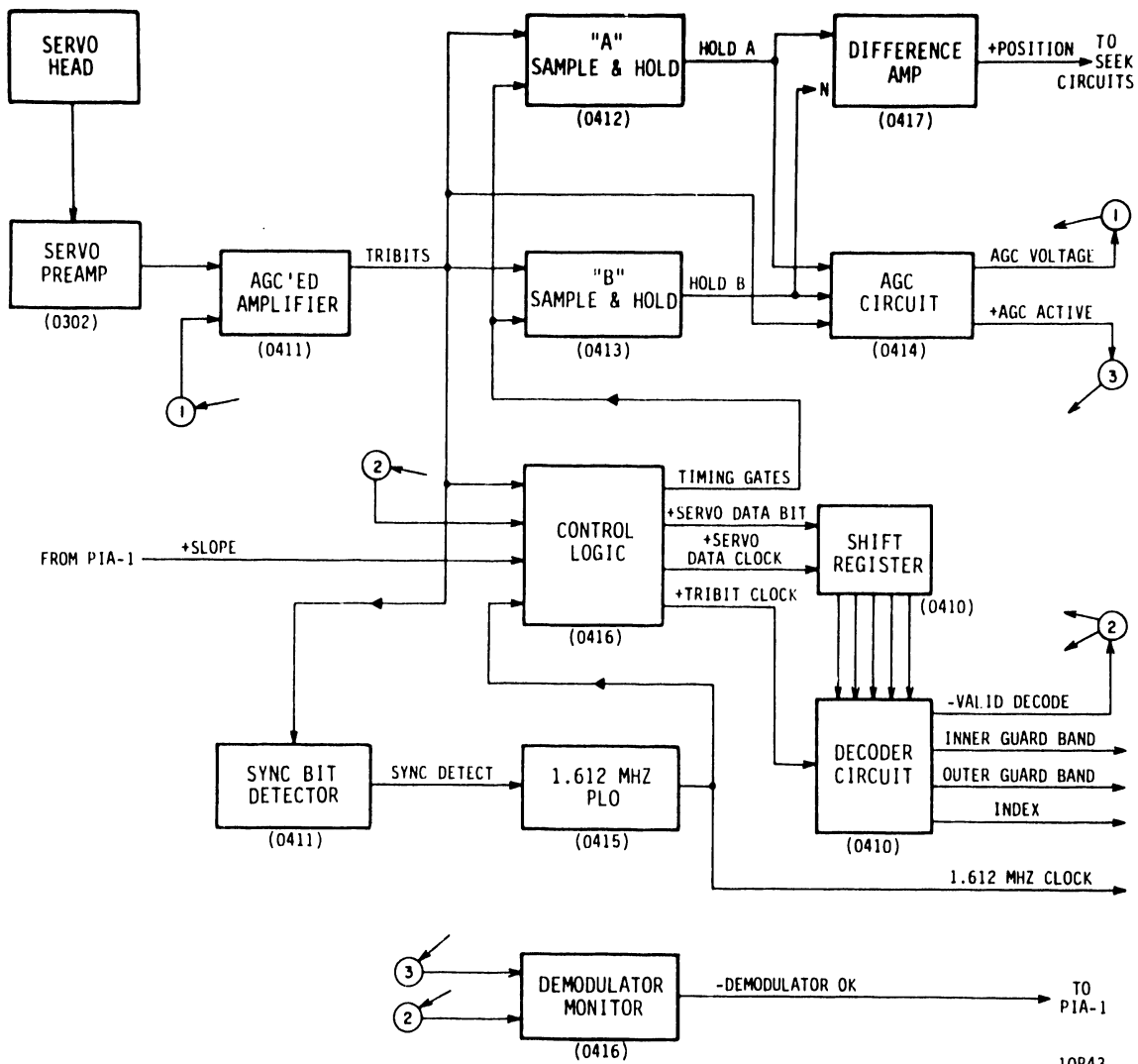


Figure 1-20. Tribit Decoder Block Diagram

contain position bits in the opposite time slots. Thus, the Peak Detect "A" gate alternates its active time between the second and third time intervals. For a tribit pattern where Peak Detect "A" is active during the second interval, Peak Detect "B" is active during the third interval. The Transfer gate, active during the fourth interval, inputs the two sampled voltages into the two associated hold circuits where the Hold "A" and Hold "B" signals are adjusted to reflect the latest amplitudes of the position bits.

The Hold "A" and Hold "B" signals follow the peak amplitude of the position bits detected on the two tracks nearest to the servo head. The Hold "A" and Hold "B" signals are input to a difference amplifier to derive the Position signal, an analog

signal which is proportional to (Hold "A" - Hold "B"). The Position signal is positive when the servo head is closer to a track containing "A" position bits and is negative when the servo head is closer to a track containing "B" position bits. When the data heads are positioned directly over a data track, the servo heads are centered between two servo tracks and the Position signal is zero.

With one exception, movement of the servo head from one track to an adjacent track reverses the polarity of the Position signal. This is true when the servo head crosses tracks in the guard bands and the data zone. However, the buffer zone, located between the outer guard band and data zone, has four consecutive tracks that are recorded with identical (not alternating) position information. Thus, as the servo head moves across these tracks, the Position signal stays negative and does not cross zero as it does in the other zones.

Initialization of the control logic determines which group of position bits is measured by the "A" Sample and Hold circuit and which group is measured by the "B" Sample and Hold circuit. The first step in initialization resolves the ambiguity present in the tribit modulation scheme. In successive tribit patterns from a given servo track, the position bit alternates between two possible locations. Throughout drive operation, the -Valid Decode signal is returned to the control logic immediately after each five-byte format code appearing at regular intervals on the servo track. At this time, the Peak Detect "A" and "B" gates are forced to match the format of the tribits as they were recorded on the servo surface. The second step in initialization occurs each time a new seek is commanded. By setting the level of the +Slope signal, the MPU can cause the waveforms of the Peak Detect "A" and "B" gates to be interchanged. Interchanging Peak Detect "A" and "B" inverts the Position signal and allows the MPU to ensure that the +Position signal will have the required slope as the seek circuits position the heads at their new destination. This slope requirement is discussed further under Seek Functions.

Tribit Decoder PLO

The PLO in the tribit decoder generates a clock signal that establishes the basic timing for the tribit decoder control logic and is used as the reference frequency to develop Servo Clock. The PLO oscillates at a nominal frequency of 1.612 MHz, which is four times the repetition rate of sync bits in the

detected servo signal. The PLO is part of a phase-locked loop that phase modulates the PLO to keep its output under the control of the sync bit repetitions. Thus, any variation in the rotational speed of the disk produces a proportional variation in the 1.612 MHz clock frequency.

Figure 1-21 is a block diagram of the phase-locked loop, and figure 1-22 is a timing diagram for the circuit.

As shown in the block diagram, the tribit signal is input to a zero cross detector which produces a Sync Detect pulse at every Sync bit and Servo Data bit in the servo signal. To prevent Servo Data bits from affecting the PLO frequency, the Servo

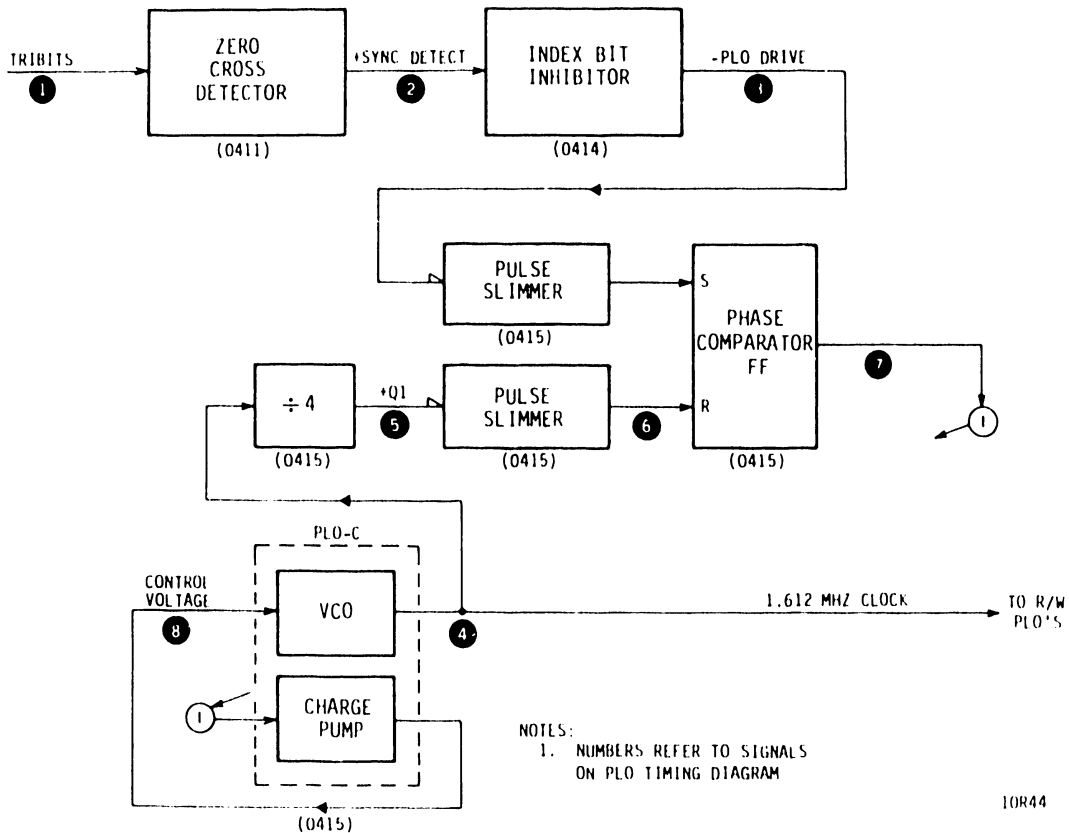
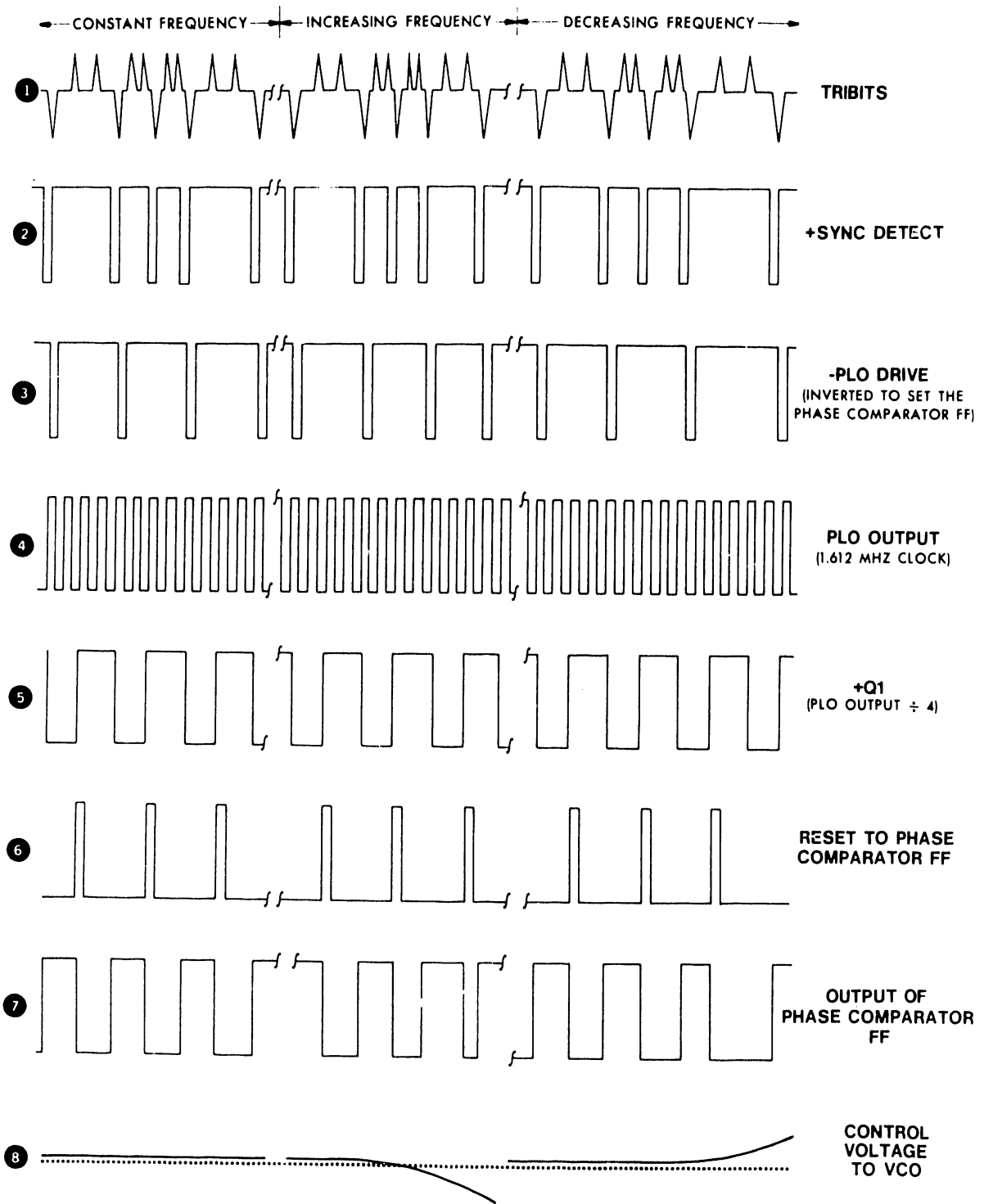


Figure 1-21. PLO Block Diagram



NOTE:

1. NUMBERS REFER TO SIGNALS ON PLO BLOCK DIAGRAM

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Figure 1-22. PLO Timing

Data Bit Inhibitor produces -PLO Drive pulses only for the Sync bits in the Sync Detect signal. The -PLO Drive pulses are narrowed, inverted, and applied to the Set input of the Phase Comparison FF. At approximately the midpoint between -PLO Drive pulses, a Reset pulse is applied to the Phase Comparator FF. The Reset pulse is developed as follows: the 1.612 MHz output of the PLO is divided by four to produce the Q1 signal, a square wave whose frequency matches the repetition rate of the Sync bits. The negative transitions of Q1 coincide with the -PLO Drive pulses, and the positive transitions are 180° out of phase with the negative transitions. A pulse slimmer circuit reduces the length of the Q1 positive oscillation to produce a narrow Reset pulse for the Phase Comparator FF.

The Phase Comparator FF causes the PLO to shift in frequency when the set interval and the cleared interval of the FF are not equal. This frequency shift is governed by the charge pump within the PLO. The charge pump supplies a control voltage to the voltage-controlled oscillator (the VCO is also part of the PLO): the charge pump looks at the set and cleared intervals of its input signal (from the Phase Comparator FF) and varies the control voltage from its normal value depending on the balance of the two intervals. The control voltage, in turn, shifts the VCO frequency as needed to phase lock the VCO signal, via the feedback loop, to the -PLO Drive signal.

Three timing situations are shown in figure 1-22. When the VCO frequency is correct, the set and cleared intervals of the Phase Comparison FF are equal, the control voltage is normal, and the frequency of the VCO stays the same. When the VCO frequency is too high, the Reset input to the Phase Comparison FF is early, and the FF is cleared longer than it is set. This causes the charge pump to shift the control voltage more positive than normal which, in turn, decreases the VCO frequency. When the VCO frequency is too low, the Reset input to the Phase Comparison FF is late, and the FF is set longer than it is cleared. This causes the charge pump to shift the Control Voltage more negative than normal which, in turn, increases the VCO frequency.

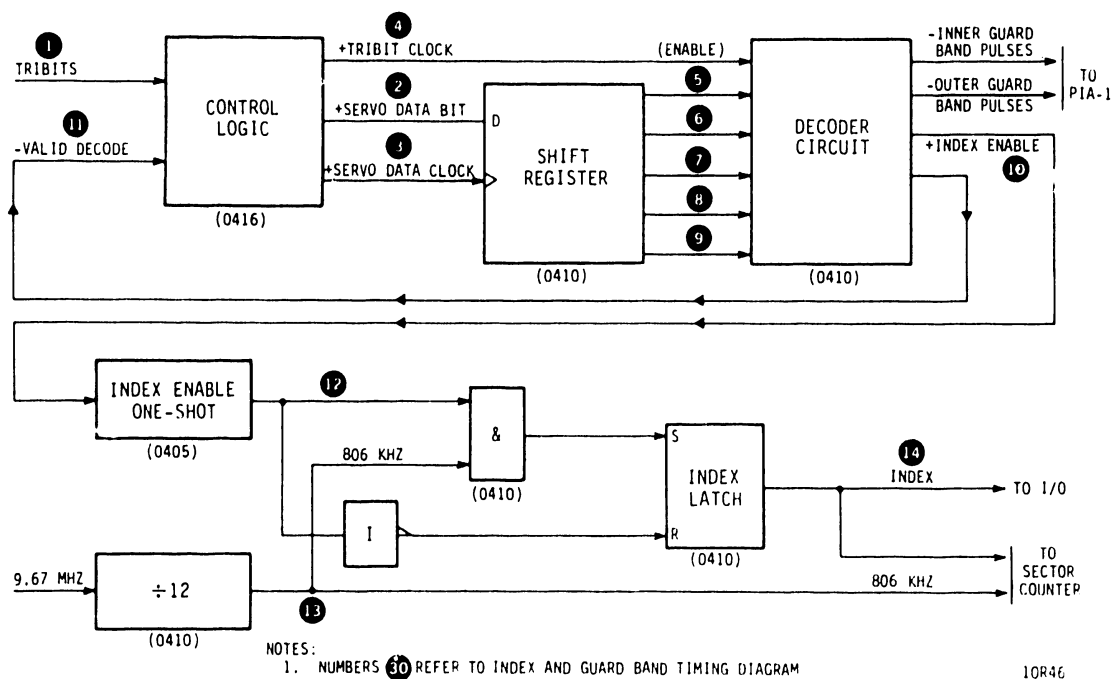
Index and Guard Band Decoding

The index and guard band decoding circuitry produces output pulses each time the servo head detects format indicators on the servo surface. This circuitry also originates the -Valid Decode signal which is used to initialize the position demodulating circuitry. Refer to Servo Surface Format for a description of the format indicators and their location on the servo disk.

Figure 1-23 is a block diagram of the index and guard band decoding circuitry. Figure 1-24 shows the timing relations when the index pattern is decoded from the servo signal. In guard band decoding, the same timing relations apply, but the servo signal input is different.

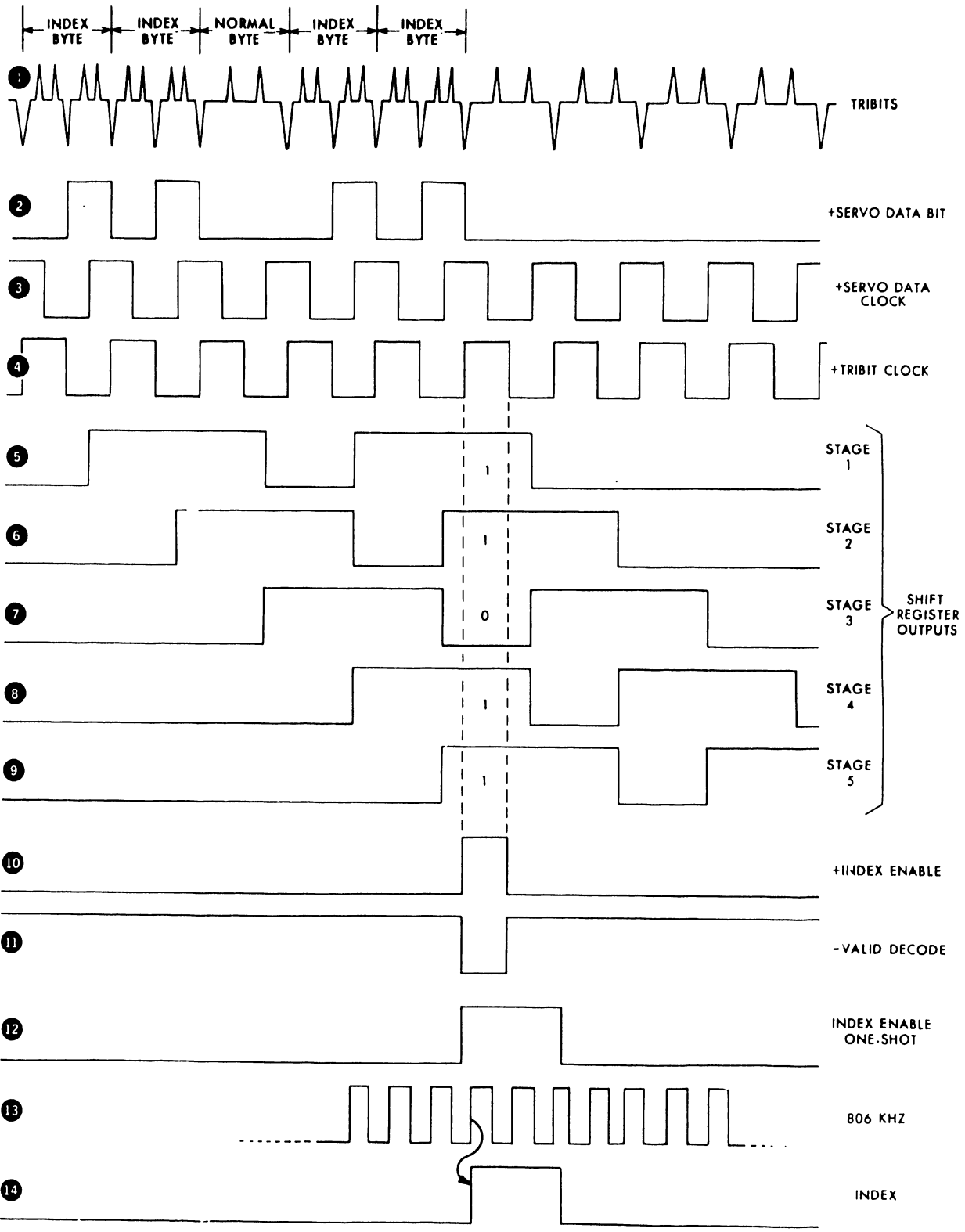
Index and guard band information is decoded from the servo signal in three steps. The control logic develops intermediate signals from the servo tritbit pattern. These signals, in turn, operate a shift register that contains information about the last servo bytes detected. Finally, the decoder samples the shift register contents each byte, and when the register contents match one of the format indicators, the decoder activates the corresponding output line.

As shown in figure 1-24, the +Servo Data Bit line goes active when a Servo Data bit occurs and stays active until the next Sync bit. The +Servo Data Bit signal is the D-input to a five-stage shift register. A timing signal, called +Servo Data Clock, is developed by the control logic. The leading edge of +Servo Data Clock, which occurs just prior to each sync bit, shifts the +Servo Data Bit signal into the shift register. Thus, the shift register indicates whether each of the last five servo bytes were index bytes or normal bytes. A decoder circuit monitors the five outputs of the shift register. The decoder circuit is enabled only during the first half of each servo byte, when the control logic activates the +Tribit Clock line.



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Figure 1-23. Index and Guard Band Decoding Circuitry



NOTES:
 1. NUMBERS 30 REFER TO SIGNALS ON INDEX AND
 GUARD BAND DECODING CIRCUITRY DIAGRAM

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Figure 1-24. Timing Relations in Index Decoding

The decoder recognizes specific patterns in the shift register by activating its output lines as follows:

- When the register contains 11011, there are active pulses on the +Index Enable and -Valid Decode lines.
- When the register contains 10111, there are active pulses on the -Outer Guard Band Pulses and -Valid Decode lines.
- When the register contains 11101, there are active pulses on the -Inner Guard Band Pulses and -Valid Decode lines.
- When the register contains 10101, there is an active pulse on the -Valid Decode line. This code is produced by format indicators in the data zone and has no individual decoder output.

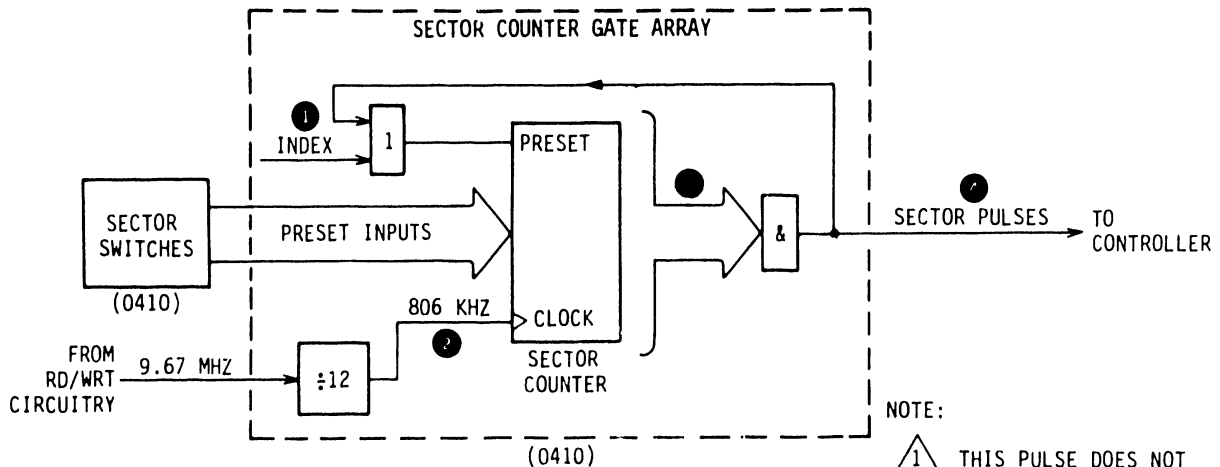
Additional circuitry extends the Index pulse to 2.5 microseconds and synchronizes the timing of Index to the Sector pulses produced by the Sector Counter. The Index Enable pulse triggers a 2.5 microsecond one-shot. The one-shot output is ANDed with an 806 kHz clock, the timing signal for the Sector Counter, to set the Index latch. The Index latch is cleared when the Index Enable one-shot output goes inactive. Operation of the Sector Counter is described under Sector Detection.

Sector Detection

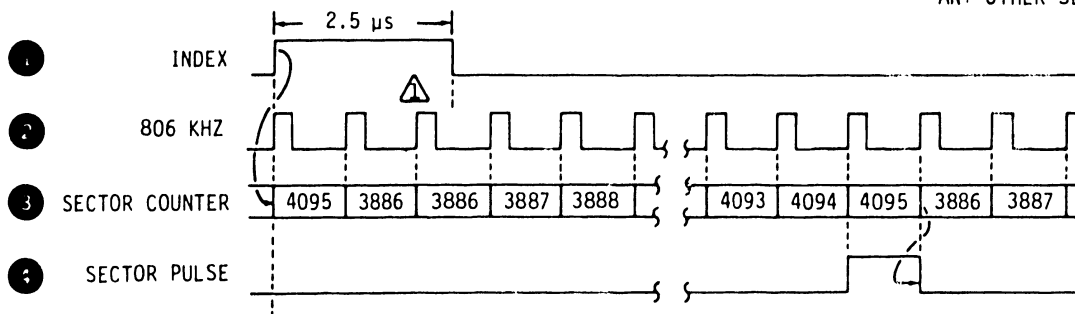
The sector detection circuit (figure 1-25) generates signals which are used by the drive to determine the angular position of the heads with respect to index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disks. The Sector pulses logically divide the disk into areas called sectors.

The Sector pulses are generated by the Sector counter which generates a pulse each time it reaches its maximum count (4095). The counter is incremented by the 806 kHz clock pulses. These clock pulses are derived from the 9.67 MHz Servo Clock and represent the beginning of each data byte. The Index pulse resets the counter allowing 13 440 clock pulses per revolution of the disk.

The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution. This is done by pre-setting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors,



NOTE:
 1 THIS PULSE DOES NOT INCREMENT COUNTER BECAUSE INDEX IS STILL ACTIVE; THEREFORE, SECTOR 000 ALWAYS CONTAINS ONE MORE 806 KHZ PULSE THAN ANY OTHER SECTOR.



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Figure 1-25. Sector Detection - Logic and Timing

the counter would have to count 210 clock pulses in each sector (13 440 divided by 64) and the counter would be preset to 3886. In this case, the counter starts at 3886 and increments each clock time until it reaches the maximum count (4095). Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (210) presets the counter back to 3886 (thus disabling the Sector pulse) and the counter begins the next sector.

The sector length is varied by presetting the sector switches located on the control board. Refer to Volume 1 of the maintenance manual for details regarding the setting of the sector switches.

SEEK FUNCTIONS

GENERAL

During seek operations, the drive positions the heads over the desired cylinder on the disk. The drive servo circuits, under the direction of a microprocessor unit (MPU), control this function. The drive servo circuits translate MPU instructions into electromechanical motion to position the read/write heads accurately and to allow the transfer of magnetic pulses to and from a disk storage surface. The two main topics of this section describe servo circuit operation and the sequencing of events in different types of seeks. Since these subjects are interrelated, they are preceded by an overview of system operation that explains the roles played by the interface and the MPU, and that describes the servo functions in general terms.

SYSTEM OVERVIEW

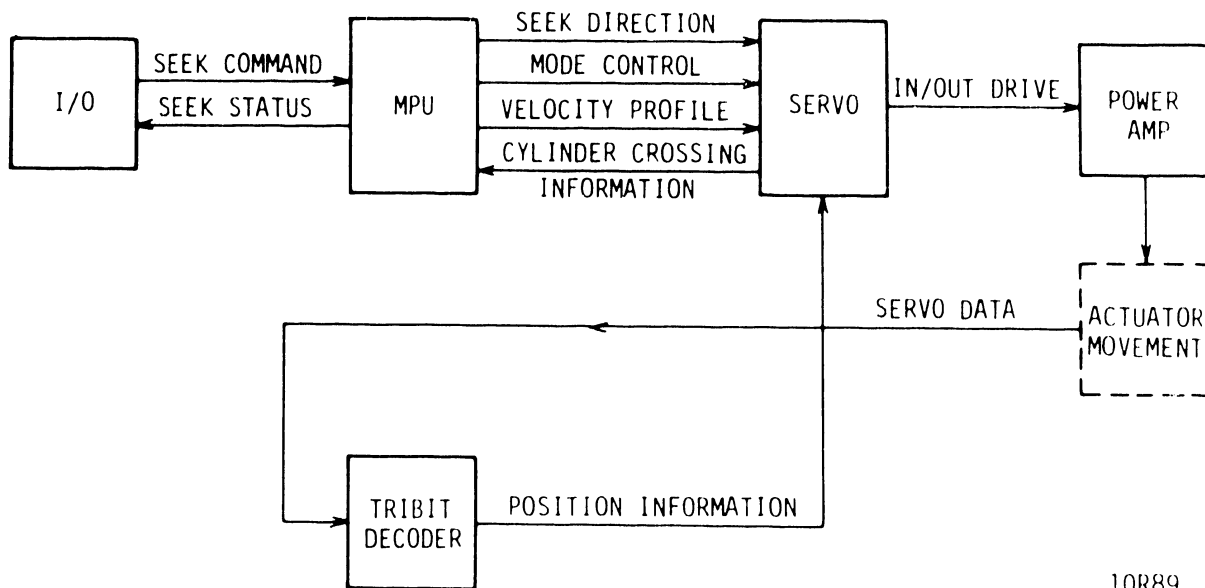
Each seek operation can be described in terms of four basic drive activities. These activities are shown in terms of general information flow between major drive functional elements in figure 1-26. These activities occur in the following sequence:

- Command -- The interface processes the command from the controller that instructs the drive to seek to a different cylinder on the disks.
- Control -- The MPU interprets the seek command, then translates the command into a sequence of controls sent to the servo circuitry. These controls dictate the direction of the seek, specify actuator velocity throughout the seek, and step the servo through its operating modes.
- Execution -- The servo circuitry executes the seek in response to control information received from the MPU. This execution is accomplished in three modes: the coarse mode, during which the actuator is moved at a controlled velocity toward its destination; the settle-in mode, in which the actuator locks in to its final position; and the track-following mode, in which the actuator position is maintained until another seek is commanded. The servo controls current to the voice coil to move the actuator/heads via in and out drive signals to the power amp. Position information from the tribit decoder serves as a feedback source to the servo loop and is converted into cylinder crossing information for the MPU.

- Status -- The MPU informs the controller via the interface whether or not the seek was accomplished successfully. This indicates whether or not a reliable data transfer can be performed on the selected cylinder.

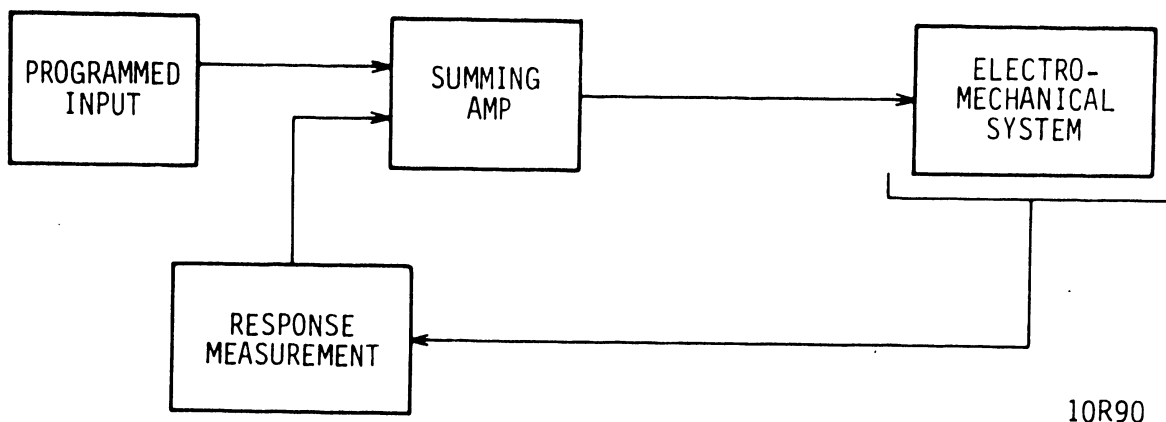
The concept of a closed loop is essential to understanding the operation of the servo system. Figure 1-27 shows a generalized servo loop that illustrates several principles governing the servo loops in the drive. The inputs to the summing amp are added, and any departure of the sum away from zero indicates that the system is unbalanced. To compensate for the imbalance, the summing amp issues a correction signal to the mechanical system. The response of the mechanical system is converted into an electrical signal which is an input to the summing amp. Mechanical movement continues until the system balance is restored, corresponding to a null in the summing amp inputs.

The drive employs two basic servo loops, a coarse loop used in the coarse mode and a fine loop used in the settle-in and track-following modes. In figure 1-28, the model of figure 1-27 is used to show the coarse servo loop in simplified form. In the coarse loop, the actuator moves at a prescribed velocity from the original cylinder address to the final cylinder address. The summing amp receives two inputs -- one signal represents the prescribed (desired) velocity of the actuator and the other represents the measured velocity of the



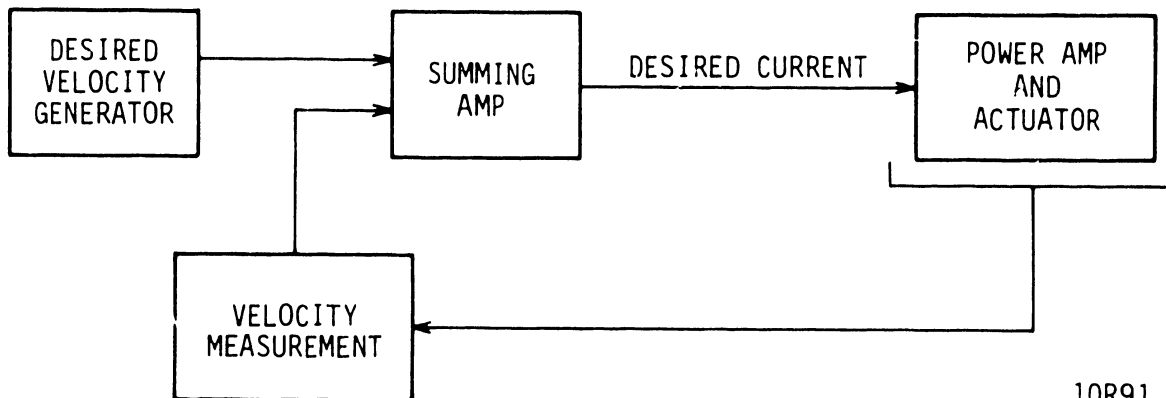
10R89

Figure 1-26. Seek Functions Block Diagram



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Figure 1-27. Generalized Servo Loop



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Figure 1-28. Simplified Coarse Servo Loop

actuator. When the desired velocity exceeds the measured velocity, desired current is produced to accelerate the actuator. When the measured velocity exceeds the desired velocity, desired current is produced to decelerate the actuator. The actuator is allowed to coast when the two inputs are equal.

In figure 1-29, the model of figure 1-27 is used to show the fine servo loop in simplified form. In the fine loop, the heads settle-in to their destination position and then maintain their position on track. The summing amp has no programmed input. Its only input is the Position signal, which is nulled at track center and varies positive or negative depending on how far the heads are displaced from track center. Any displacement of the heads from track center is adjusted by the fine loop until the summing amp input is nulled.

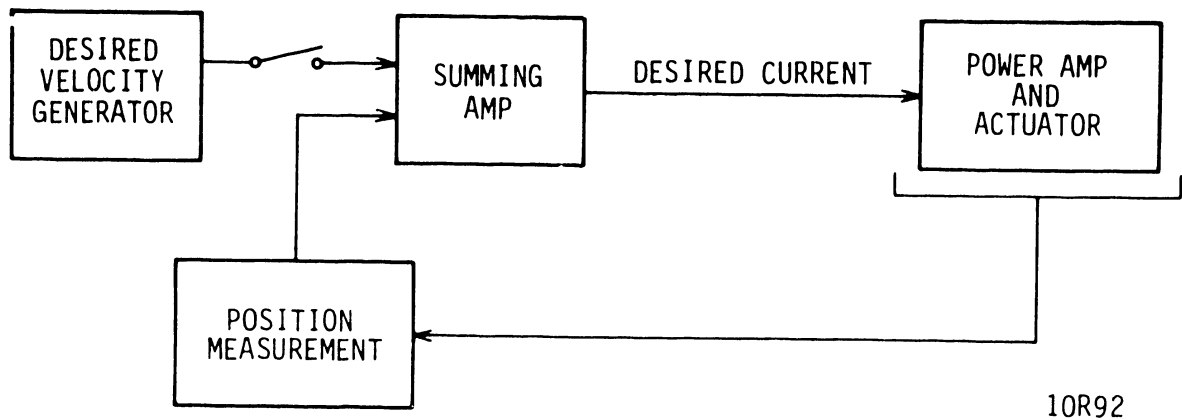


Figure 1-29. Simplified Fine Servo Loop

The following paragraphs discuss the circuit operation of these loops in more detail and then go on to describe the sequence of events in typical seeks.

SERVO CIRCUIT FUNCTIONS

General

Servo circuit functions are discussed in terms of the three basic loops within the servo circuitry (coarse, fine, and load/retract loops). The coarse loop and the fine loop have some circuit elements in common. These common circuit elements are described in detail under Coarse Loop Operation and are mentioned briefly under Fine Loop Operation. Seek operations follow defined sequences in which the MPU exercises control over the servo circuitry. These sequences are described under the next topic, Types of Seeks.

Coarse Loop Operation

General

The servo system, operating in the coarse loop, moves the heads from the existing cylinder address to within one half track of the new address. Figure 1-30 is an overall block diagram of the coarse loop circuitry. Discussion of the coarse loop is presented in the following topics:

- Microprocessor Control System
- Desired Velocity Generation

- Cylinder Pulse Detection
- Velocity Measurement
- Summing Amp
- Power Amp Driver
- Power Amplifier

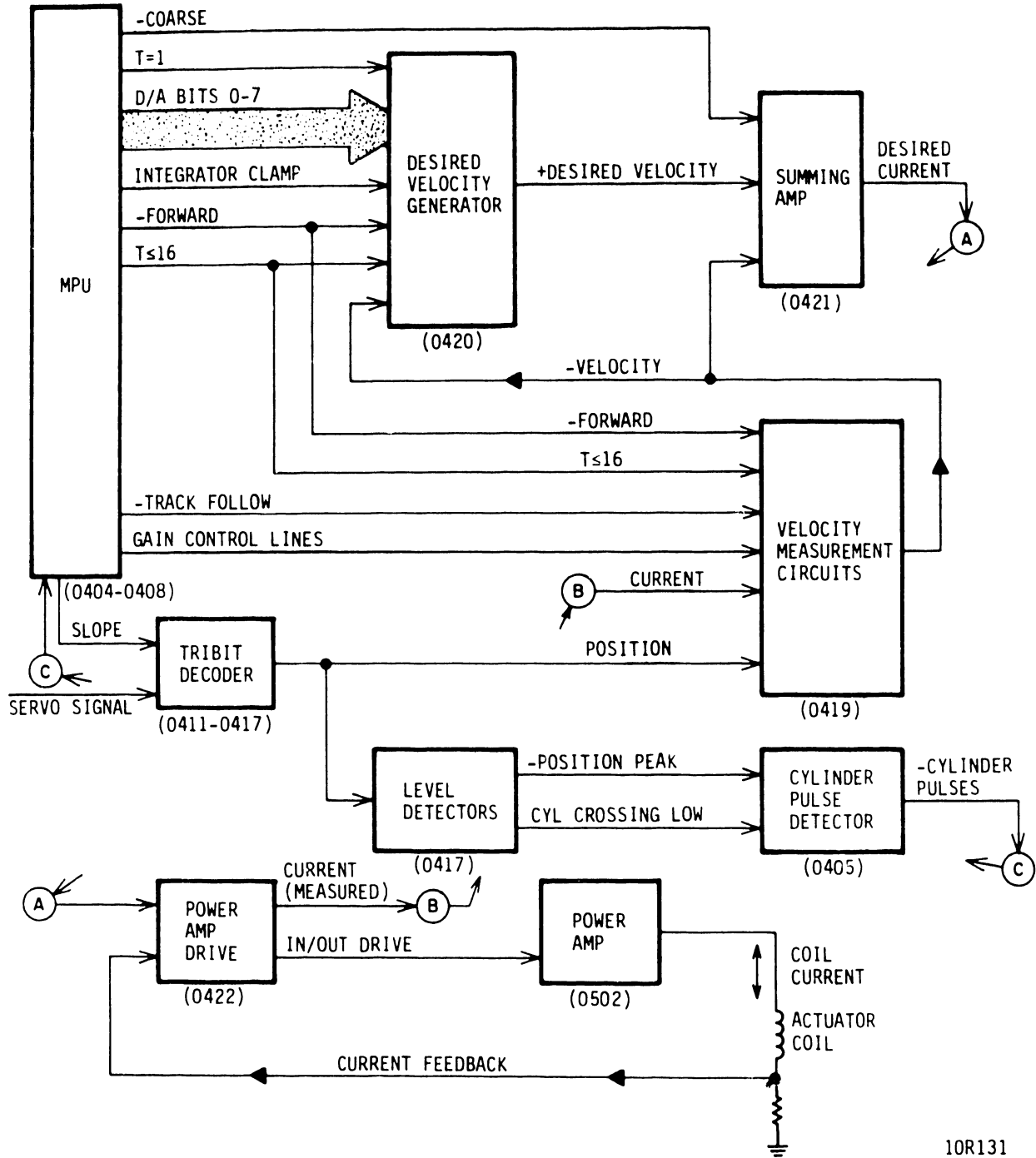
Microprocessor Control System

The microprocessor control system monitors various functions of the drive and executes most of the control sequences required for seek functions. The following paragraphs provide a general description of the components and signal paths in the microprocessor system, and describe the role of the microprocessor system pertaining to seek functions. Figure 1-31 is a block diagram of the microprocessor system. Readers interested in internal operation of the microprocessor and its peripheral chips may refer to the CDC Microcircuits Manual for more information.

The microprocessor control system consists of a 6802 microprocessor unit (MPU), a 4K-byte read-only memory (ROM), three peripheral interface adapter (PIA) chips, and a programmable timing module (PTM). The MPU communicates with its peripheral chips via an 8-bit bidirectional data bus, a 16-bit address bus, and several control lines. Circuitry within the Address Decode Gate Array monitors Address lines 12 through 14 and develops chip select signals for each peripheral chip whenever the Valid Memory Address line is active. The MPU sets the Read line to read data from a peripheral or clears the line to write data into a peripheral. The Phase 2 Clock, developed by a crystal-controlled oscillator in the MPU, provides a timing reference for the system.

The firmware instructions for the MPU reside in the ROM. Detailed information about the MPU programming is beyond the scope of this manual. However, the various sequences which the MPU performs are outlined under Power Functions and Types of Seeks. The ROM also contains a lookup table that specifies a velocity profile for normal seeks.

The PIAs allow the MPU to monitor the digital levels of certain signals developed in hardware external to the microprocessor system. In addition, the MPU can output various command signals via the PIAs. Certain PIA input signals form maskable interrupts to the MPU. When unmasked, these interrupts inform the MPU of status changes that require switching to a different routine within its firmware. The specific PIA inputs and



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Figure 1-30. Coarse Loop Block Diagram

outputs are listed in figure 1-31 and are referenced in the applicable circuit descriptions. A set of PIA lines requiring additional explanation includes I/O Control lines 1, 2, and 3. I/O Control lines 1 and 2 go from PIA-0 to the I/O Gate Array. These lines allow the MPU to perform various operations inside the gate array, such as setting the On Cylinder and Seek Error FFs, multiplexing cylinder and head addresses out of the array, and reading various fault statuses via the I/O Control 3 line.

Within the PTM, counter #2 allows the MPU to count tracks-to-go in a seek. This counter is decremented during seeks by cylinder pulses. Counter #3 is used by the MPU to generate timeouts for various operations and to make speed checks of the drive motor.

The MPU system performs the following basic functions during drive operation:

- It monitors start and interlock conditions to initiate load and retract operations.
- It starts and stops the drive motor, and it checks motor speed.
- It monitors the Seek Interrupt line and executes normal seeks.
- It specifies the desired actuator velocity during coarse seeks.
- It monitors the RTZ Interrupt line and executes RTZ seeks.
- It controls the On Cylinder and Seek Error FFs in the I/O Gate Array.

These functions are described in detail in the remainder of Seek Functions. In addition, the MPU exchanges fault status with the I/O Gate Array. This activity is discussed under Fault and Error Conditions.

Desired Velocity Generation

The desired velocity circuit generates the +Desired Velocity signal, a changing analog voltage that indicates the desired velocity of the actuator throughout the coarse mode of the seek. Throughout the seek, the MPU refers to a table in the ROM that specifies desired velocity in binary form as a function of the number of tracks to go (T), which is the number of track crossings remaining until the heads reach their destination.

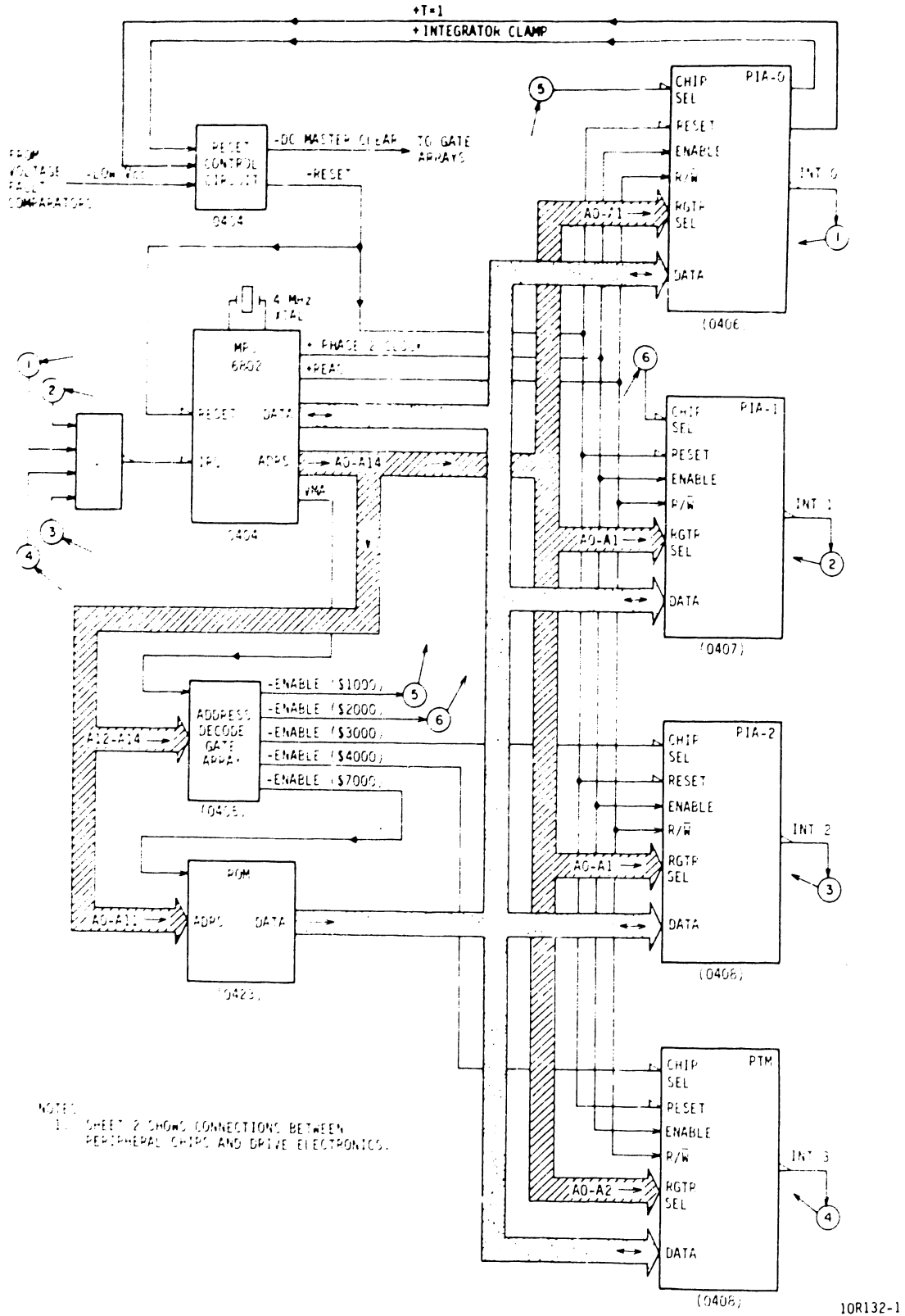
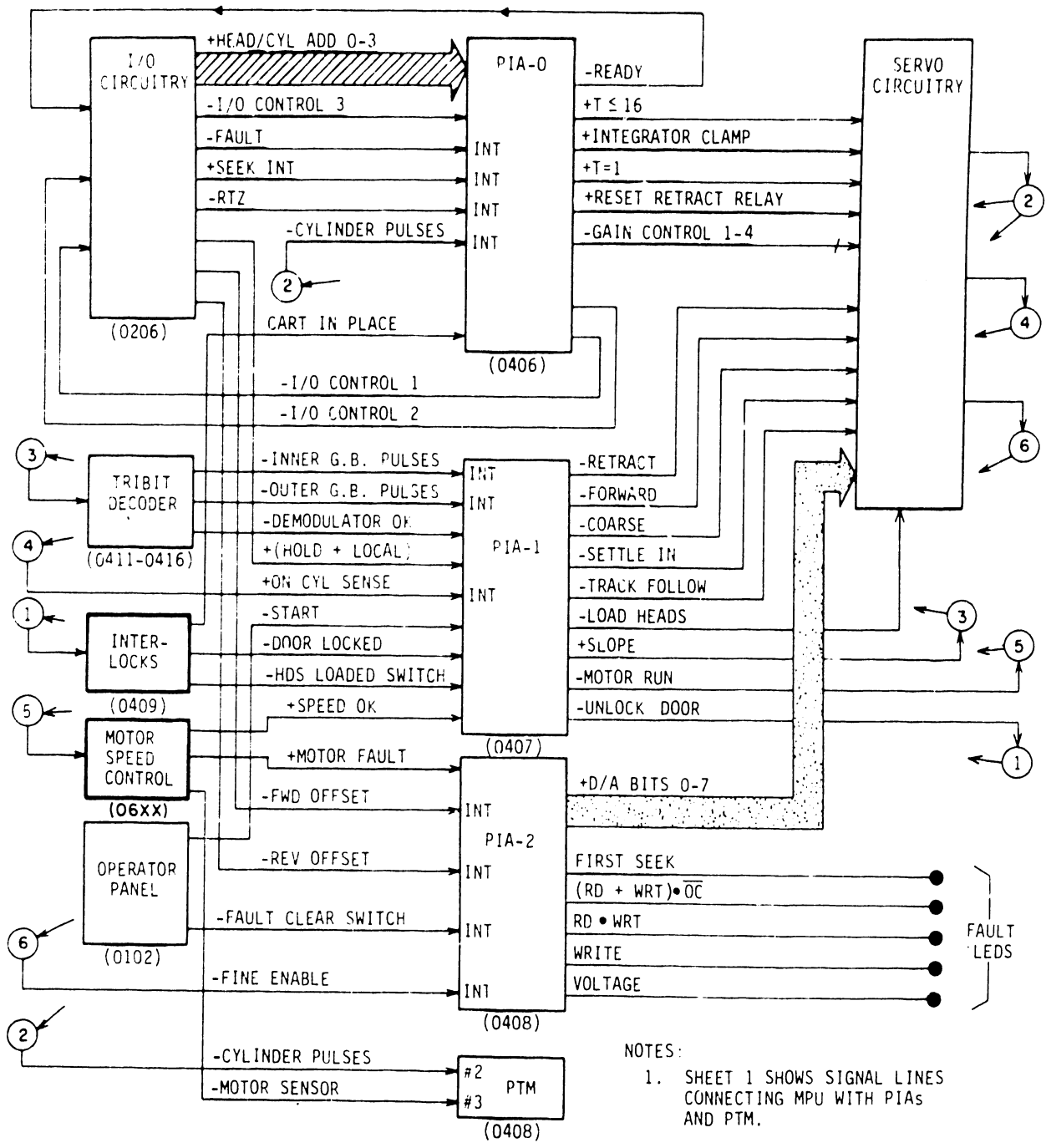


Figure 1-31. Microprocessor Control System (Sheet 1 of 2)



10R132-2A

Figure 1-31. Microprocessor Control System (Sheet 2)

The velocity table is organized in a manner that allows one table of values to be used for all seeks. The maximum velocity of the table is for 255 tracks, and as the values decrease, a velocity profile is developed whereby velocity is proportional to the square root of the distance remaining. This profile produces constant deceleration of the heads in order to minimize seek times while controlling the approach of the heads to their final position. The organization of tabulated velocity in terms of tracks to go makes it possible to use one table for all seeks. Different seek lengths start at different points within the table. For example, the velocity specified when $T=30$ is the same regardless of the total seek length.

The desired velocity circuit provides a ramp signal from the D/A (Digital to Analog) Converter based upon the eight D/A Bits it receives from the ROM table via PIA-2 (see figure 1-32). When $T \leq 16$, however, the two uppermost D/A bits are masked out at the D/A and are used elsewhere, and the Integrator Clamp signal is input via PIA-0 to provide a sawtooth signal from the Velocity Integrator to add fill-in current to the ramp as the heads approach the selected track. At each cylinder crossing, the MPU refers to a count of tracks to go in PTM Counter #2 and outputs the current value of tabulated velocity using the D/A Bits. Each change in the D/A Bits results in a stepped change in the D/A ramp. Typical waveforms for the desired velocity circuit are given in figure 1-33.

The sawtooth from the Velocity Integrator compensates for the stepped nature of the D/A ramp by filling in the sudden changes in the ramp. When $T < 40$, the sawtooth output is obtained by integrating the -Velocity signal from the velocity circuit. This output is clamped to zero each time a cylinder crossing occurs. D/A Bits 6 and 7 are reserved for controlling the degree of filling provided by the sawtooth in the final portion of the seek (when $T \leq 16$). These bits are set or cleared according to the ROM velocity table, but they are masked out of the D/A Converter input when $T \leq 16$. In the final tracks of the seek, when the velocity signal being integrated is reduced, the portion of the sawtooth applied to the +Desired Velocity signal is increased accordingly.

The sawtooth from the Velocity Integrator serves an additional purpose in the final track of coarse mode. Integrating velocity gives an indication of displacement. Each time the sawtooth reaches a specified value corresponding to a 1/2 track displacement from the last cylinder crossing, a level detector which monitors the sawtooth issues the -Fine Enable signal. With $T < 1$, the MPU looks for this signal and reacts by switching servo operation from the coarse mode to the settle-in mode.

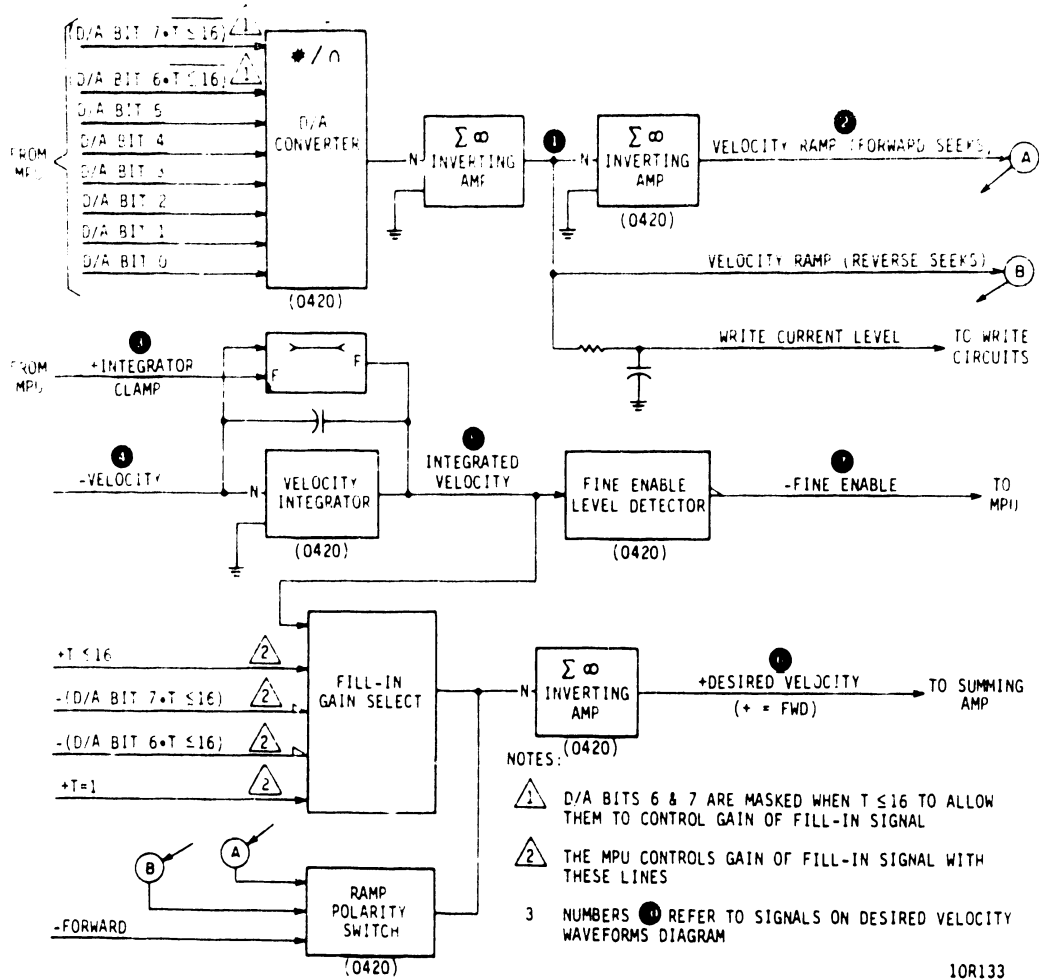
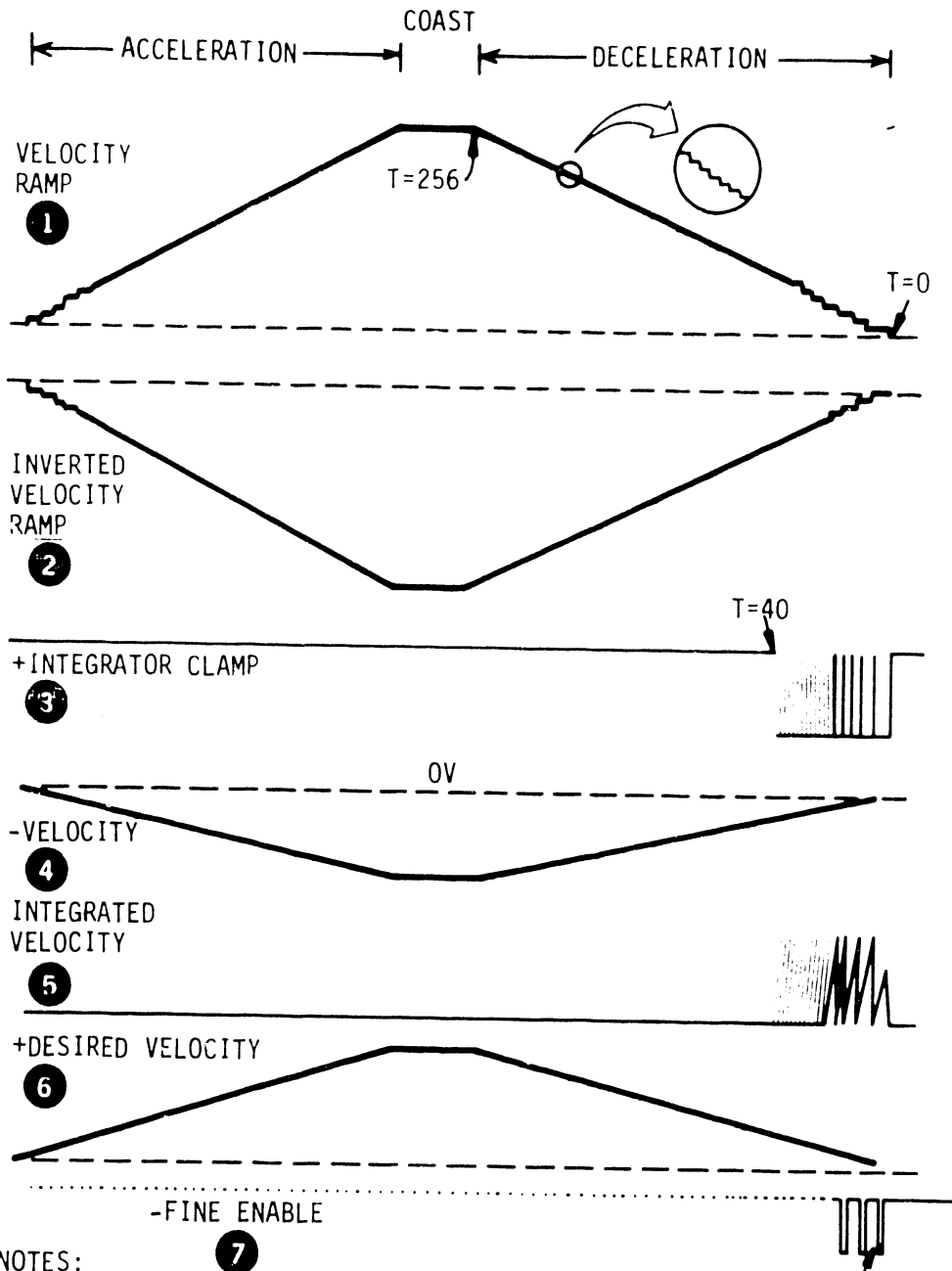


Figure 1-32. Desired Velocity Circuit

Cylinder Pulse Detection

A Cylinder Pulse is generated each time the heads cross a servo track during the coarse seek operation. Cylinder pulses serve two purposes. First, they decrement Counter #2 in the PTM, keeping its difference count equal to the number of tracks to go in the seek; this points the MPU to the correct tabulated velocity value which is stored in ROM. Second, for $T < 40$ the +Integrator Clamp line goes active during cylinder pulses to clamp the sawtooth output of the Velocity Integrator to zero. Thus, the sawtooth waveform returns to zero each time that the D/A Converter gets a revised input (see Desired Velocity Generation discussion).



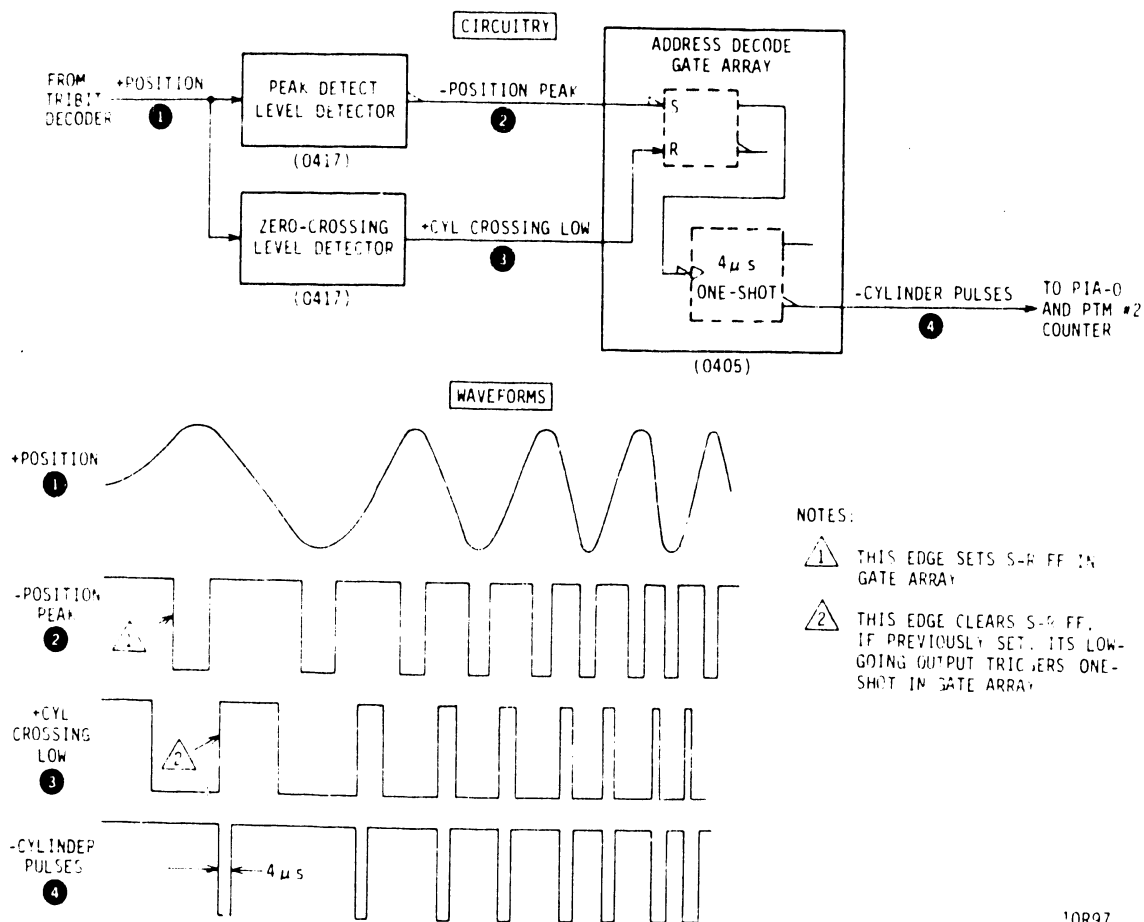
NOTES:

1. AFTER T=1, MPU LOOKS FOR THIS EDGE TO SWITCH SERVO TO FINE LOOP OPERATION.
2. NUMBERS 30 REFER TO SIGNALS ON DESIRED VELOCITY CIRCUIT DIAGRAM.
3. THESE WAVEFORMS APPLY TO LONG FORWARD SEEK.

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Figure 1-33. Desired Velocity Waveforms

During a seek, the Position signal from the Tribit Decoder alternates between positive and negative values (see Servo Surface Decoding discussion). Each zero-crossing of the Position signal corresponds to a cylinder crossing. Figure 1-34 provides a simplified block diagram and waveforms for this circuit. To ensure that only one Cylinder Pulse is generated as the Position signal crosses zero, two sets of level detectors monitor its amplitude. One set of level detectors activates the -Position Peak line during each peak of the Position signal. With the -Position Peak line active, a one-shot in Address Decode Gate Array is conditioned to accept a trigger from the second set of level detectors. As the +Position signal crosses zero volts, these level detectors activate the +Cyl Crossing Low line, and trigger the one-shot to produce a 4 microsecond Cylinder pulse.



10R97

Figure 1-34. Cylinder Pulse Circuitry and Waveforms

Velocity Measurement

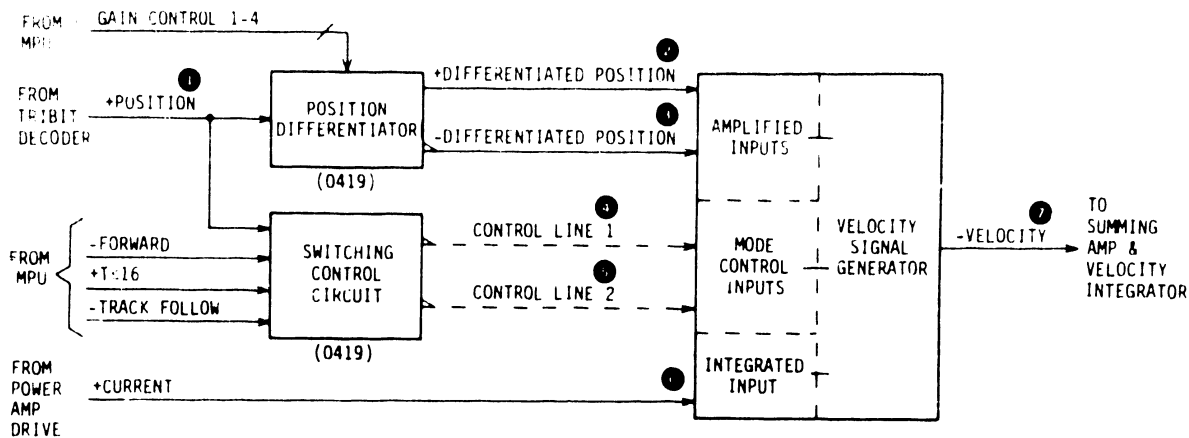
A continuous indication of actuator velocity is needed during the coarse seek mode. The -Velocity signal is developed and introduced to the coarse loop so that the servo loop can force actual velocity to match desired velocity. The -Velocity signal is negative during a forward movement (positive during a reverse movement), and its amplitude is proportional to velocity.

As part of the First Load operation, the MPU does a calibration procedure (a series of 128-track seeks) where it adjusts the gain of the velocity measurement circuit in order to compensate for gain variations in the servo disk. The gain is adjustable in steps depending on which combination of the four gain control lines is set. Upon finding the optimum combination of settings, the MPU maintains that combination (output from PIA-0) until another First Load operation is necessary.

Figure 1-35 is a simplified block diagram of the velocity measurement circuits. Velocity measurement is a sequenced operation in which the switching control circuit selects different signal inputs for the Velocity Signal Generator and determines the operating mode of the Velocity Signal Generator.

The sequencing pattern repeats itself with every complete oscillation of the +Position signal. Each oscillation of the +Position signal has four distinct regions, as shown in figure 1-36. The positive peak region is followed by a linear region with constant falling slope. Then there is a negative peak region followed by a linear region with constant rising slope. The switching control circuit monitors the +Position signal with two level detectors, one that senses the positive peak region and another that senses the negative peak region.

In each sequence pattern, the switching control circuit activates one control line during one linear region and the other control line during the other linear region. During the linear regions, the differentiated position outputs are proportional to velocity because velocity is the time rate of position change. So during linear regions, the switching control circuit places the Velocity Signal Generator in the amplifying mode and selects the differentiated input of the proper polarity in each region. In the first linear region of the coarse seek (the first 1/2 track), the MPU selects one of the control lines by setting or clearing the +T<16 line at PIA-0 and by clocking the +T<16 level into the Last Peak Latch when the -Track Follow line goes positive. Through the rest of the seek, the circuit is self-running. The detected position sig-



NOTES:

1. NUMBERS ● REFER TO SIGNALS ON VELOCITY MEASUREMENT WAVEFORMS DIAGRAM.

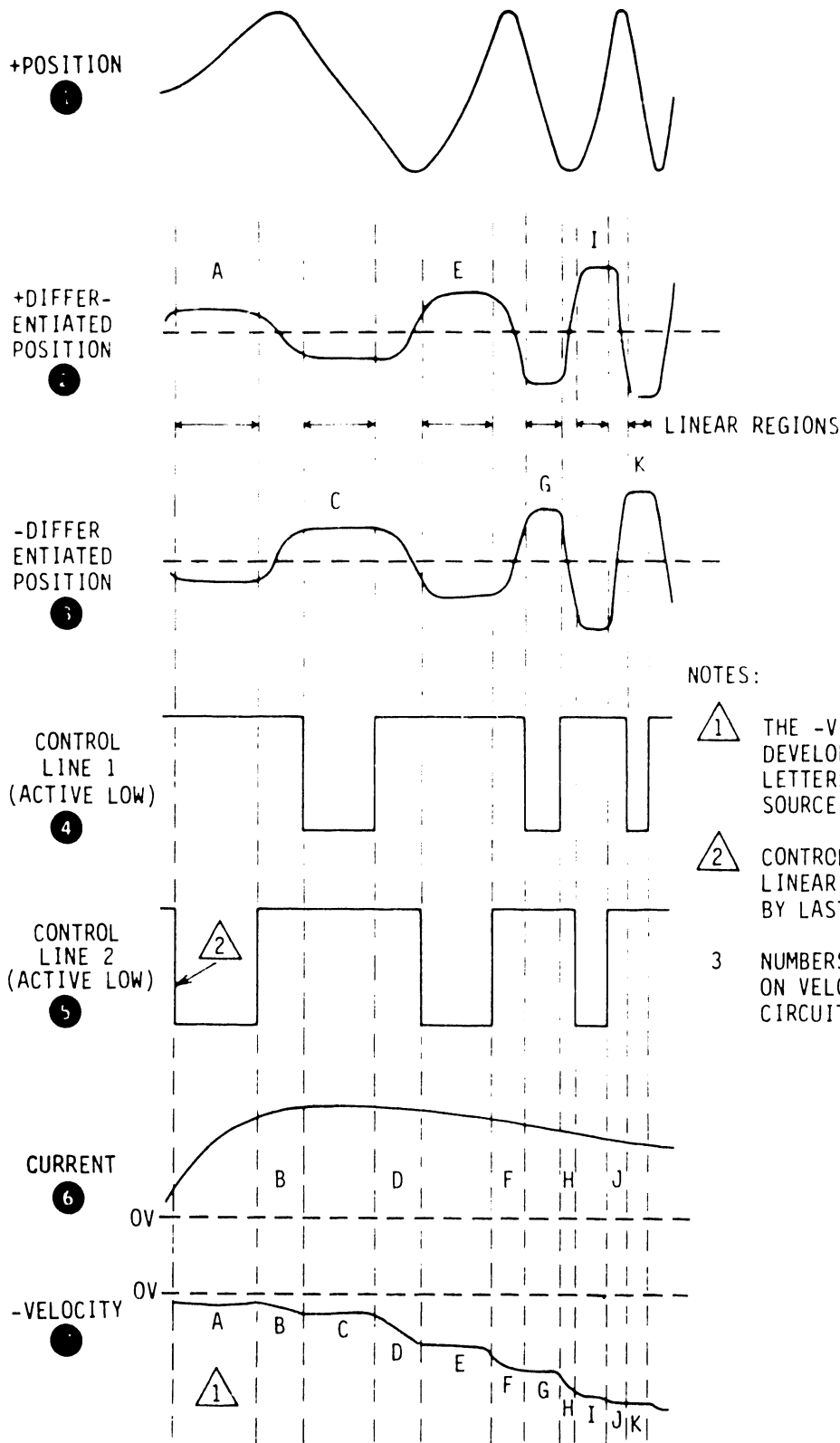
10R135A

Figure 1-35. Velocity Measurement Circuits

nal peaks alternately set and clear the latch, and the latch alternately activates the two control lines in successive linear regions. The proper input polarity to the Velocity Signal Generator is a function of the latch state and the level of the -Forward line; this makes the -Velocity signal polarity match the seek direction.

When the +Position signal is in the peak regions and thus neither control line is active, the switching control circuit allows the Velocity Signal Generator to integrate its Current input. This fills in the gaps in the -Velocity Signal at times when no differentiated position signal is available.

The Current signal is derived in the Power Amp Drive by amplifying Current Feedback sampled at the actuator. Any acceleration or deceleration of the actuator produced by the servo loop is proportional to this current. Velocity is the integral of acceleration; therefore, when the Velocity Signal Generator integrates the Current signal, it is deriving a velocity signal during Position signal peaks.



NOTES:

- ① THE -VELOCITY SIGNAL IS DEVELOPED FROM 3 SOURCES. LETTERS A THRU K IDENTIFY SOURCE FOR EACH REGION
- ② CONTROL LINE FOR FIRST LINEAR REGION IS ACTIVATED BY LAST PEAK LATCH
- 3 NUMBERS ③ REFER TO SIGNALS ON VELOCITY MEASUREMENT CIRCUIT DIAGRAM

10R136

Figure 1-36. Velocity Measurement Waveforms

Summing Amp

The servo system operates, in each mode, to null the input to the summing amp. The MPU selects the signal input to the summing amp via PIA-1 by enabling one of two analog gates. In coarse loop operation, the -Coarse line is active, and velocity information is input to the Summing Amp. In fine loop operation, the -Settle In line is active and position information is input to the Summing Amp (see discussion of Fine Loop Operation).

The Summing Amp input in coarse loop operation is the sum of the +Desired Velocity and -Velocity signals. When measured velocity is equal to desired velocity, these signal inputs add to zero, and -Desired Current, the output of the Summing Amp, is zero. With unmatched inputs, the -Desired Current line has a voltage level that indicates both the magnitude and the polarity of actuator current that will bring the servo system into balance. Zener diodes in the feedback path of the Summing Amp prevent amplifier saturation by keeping the output amplitude between -10 volts and +10 volts. When -Desired Current is negative, the resulting actuator current will accelerate the heads in a forward seek or decelerate the heads in a reverse seek.

Power Amp Drive

The Power Amp Drive generates In Drive or Out Drive currents as inputs to the Power Amp in response to the voltage level on the -Desired Current line from the Summing Amp. Together, the Power Amp Drive and the Power Amp make up a current feedback amplifier. Through a feedback loop that monitors actuator current, the Power Amp Drive adjusts the current in the In Drive line or the Out Drive line as necessary to produce the actuator current specified by the -Desired Current signal. Figure 1-37 shows the Power Amp Drive in simplified form, and the following paragraphs provide a detailed description of its circuit operation.

The Current Sense signal, an analog voltage proportional to actuator current, is applied to an op amp which amplifies it to produce the +Current signal. The +Current signal is a positive voltage when the actuator exerts inward force and a negative voltage when the actuator exerts outward force. At a second op amp, the +Current and -Desired Current signals are added, inverted and amplified to produce the +Current Error signal. The +Current Error signal is zero when the actuator current matches the desired current specified by the servo loop. A mismatch makes the +Current Error signal go positive or negative as required to bring the actuator current to the desired value. In this manner, the Power Amp Driver and Power Amp are a closed loop current amplifier.

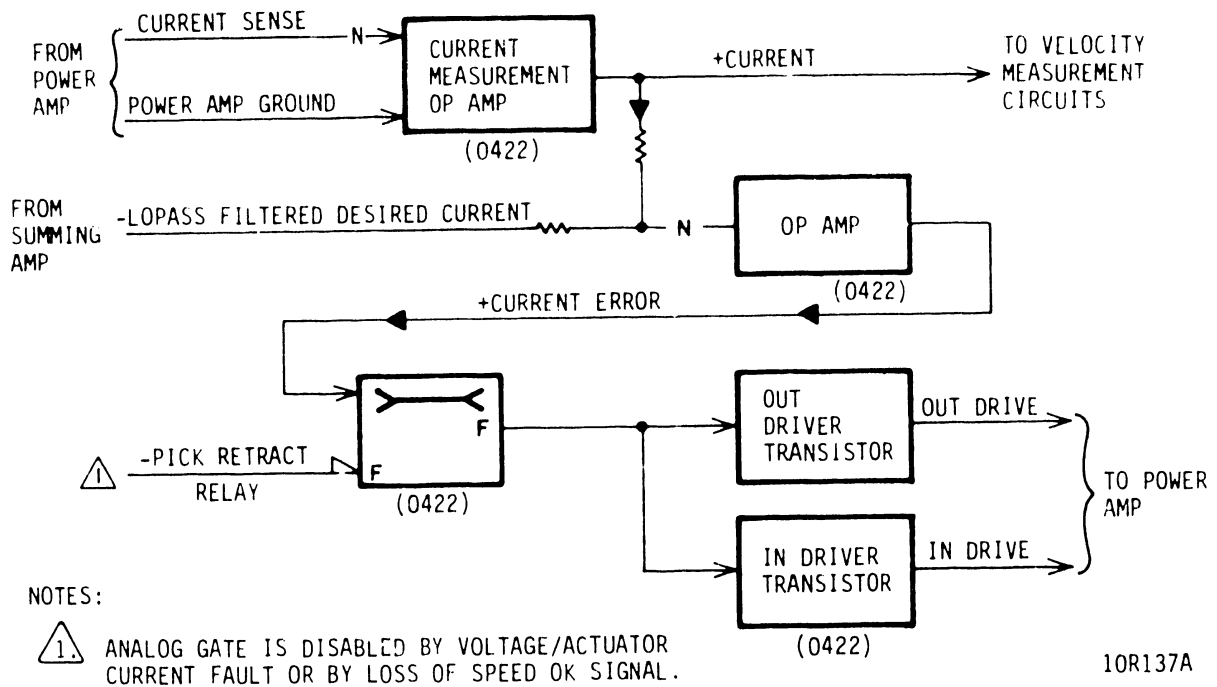


Figure 1-37. Power Amp Drive Circuitry

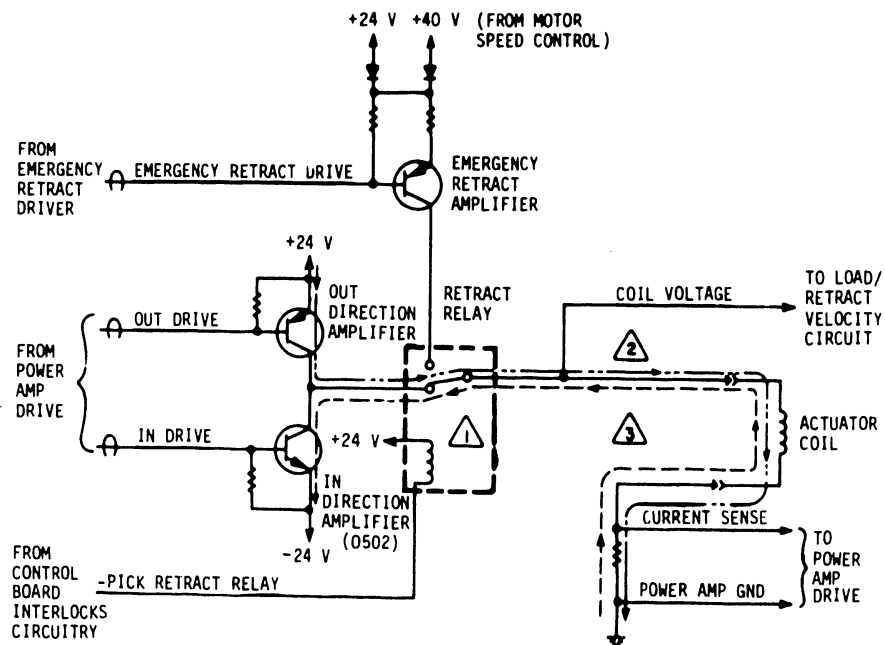
The +Current Error signal is input to an analog gate which is enabled by the -Pick Retract Relay signal (true if there is neither a voltage/actuator current fault nor a Speed OK fault). A voltage/actuator current fault or not Speed OK condition will disable the analog gate and block the input to the power amp driver transistors. This disables the servo until the fault condition is cleared. With the analog gate enabled, the +Current Error signal is fed to the inputs of the In and Out Driver transistors.

When the error voltage is positive, it cuts off the Out Driver transistor and regulates the current in the In Drive output line. When the error voltage is negative, it cuts off the In Driver transistor and regulates the current in the Out Drive output line. When the error voltage changes sign, it reverses the direction of actuator current, thereby reversing the force applied to the actuator.

Power Amp

The Power Amp, acting on inputs from the Power Amp Drive, produces the actuator current required by the servo loop. Figure 1-38 is a simplified drawing of the Power Amp circuitry.

When positive actuator current is required, the Power Amp Drive generates current in the In Drive line. The In Direction Amplifier amplifies this input current and regulates (positive) current flow from ground through the sampling resistor and the actuator coil to -24 V. The negative voltage on the Current Sense line is supplied to the Power Amp Drive to complete the loop regulating the amplifier (see discussion of Power Amp Drive). Negative actuator current forces the actuator to accelerate during a forward move and to decelerate during a reverse move.



NOTES:

1. RETRACT RELAY IS SHOWN ENERGIZED. A VOLTAGE/ACTUATOR CURRENT FAULT OR LOSS OF SPEED CAUSES RELAY TO DEENERGIZE.
2. ——— SHOWS FLOW OF (POSITIVE) OUT DIRECTION CURRENT.
3. - - - - SHOWS FLOW OF (POSITIVE) IN DIRECTION CURRENT.

10R138

Figure 1-38. Power Amp Circuitry

When negative actuator current is required, the Power Amp Drive generates current in the Out Drive line. The Out Direction Amplifier amplifies this input current and regulates (positive) current flow from +24 V through the actuator coil and the sampling resistor to ground. In this case, the voltage on the Current Sense line is positive. Positive actuator current forces the actuator to accelerate during a reverse move and to decelerate during a forward move.

During emergency retract operations, the Retract Relay is deenergized and the Emergency Retract Power Amplifier regulates actuator current. This operation is discussed under Load/ Retract Servo Loops.

Fine Loop Operation

General

The servo system shifts from the coarse loop to the fine loop when there is 1/2 track remaining in the seek. Fine loop operation continues until the beginning of the following seek. Figure 1-39 is a simplified block diagram of the fine loop circuitry. Discussion of the fine loop is presented in the following topics:

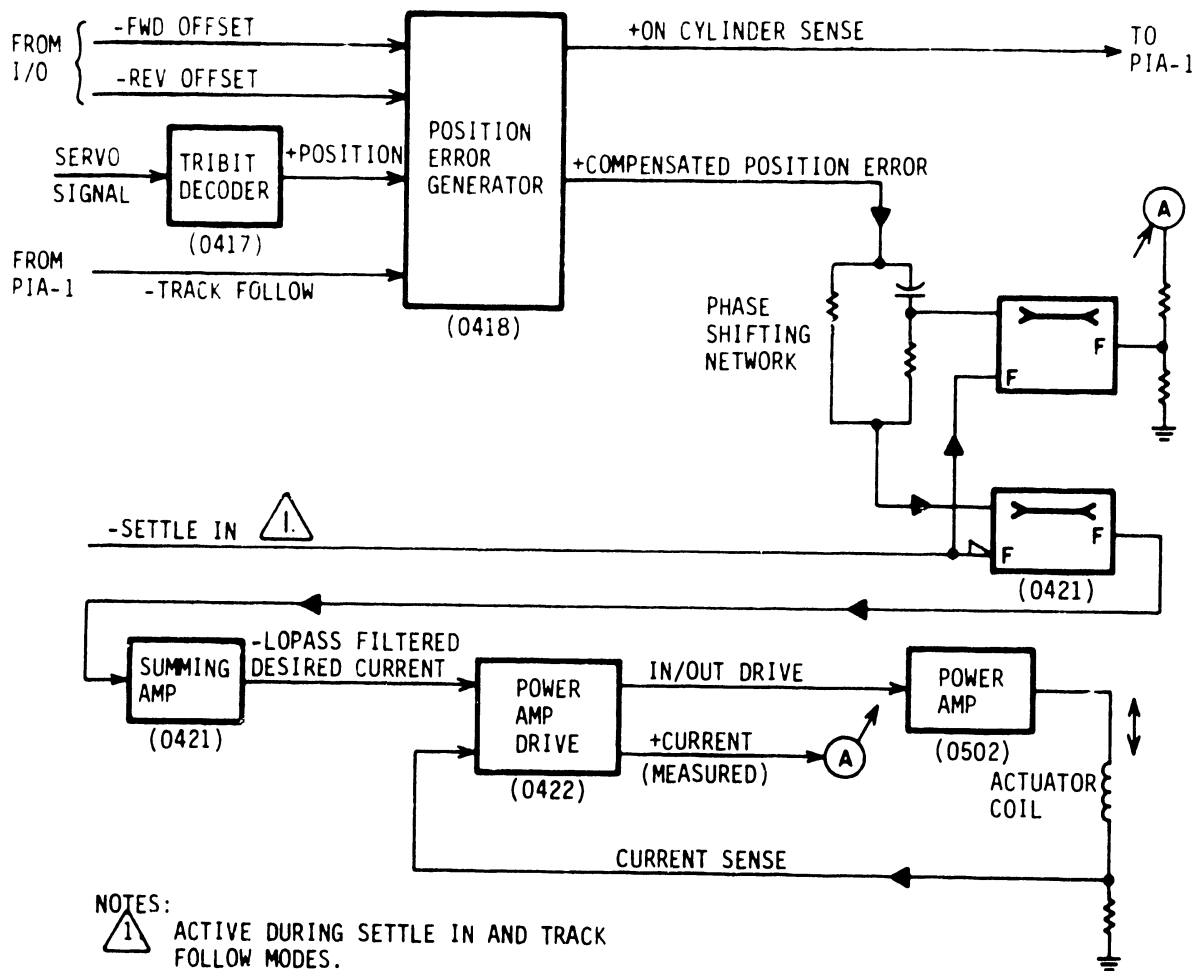
- Position Error Generation
- Fine Loop Actuator Movement

Position Error Generation

In fine loop operation, the servo system adjusts the position of the actuator to null the input signal to the Summing Amp. The Summing Amp input developed for fine loop operation is different for settle in and for track-following modes. However, both of these error signals basically derive from the +Position signal from the Tribit Decoder.

At the start of a seek, the MPU sets or clears the +Slope input to the Tribit Decoder to ensure that +Position goes positive as the heads move inward and negative as the heads move outward from their destination track. The +Position signal is zero with the heads exactly on track. This relationship is true for every destination track on the disk. Thus, with some modification, +Position is a suitable error signal for the Summing Amp in the fine loop. The modification takes into account the following considerations:

- Stability of fine servo loop -- requires the addition of a differentiated correction to the error signal.



10R139

Figure 1-39. Fine Loop Block Diagram

- Servo offsets -- allow the controller to reposition the heads to either side of track center to recover read errors.
- Increased gain in track-following mode -- gives the servo more responsive control when keeping the heads on track.

Figure 1-40 shows the position error circuitry in simplified form.

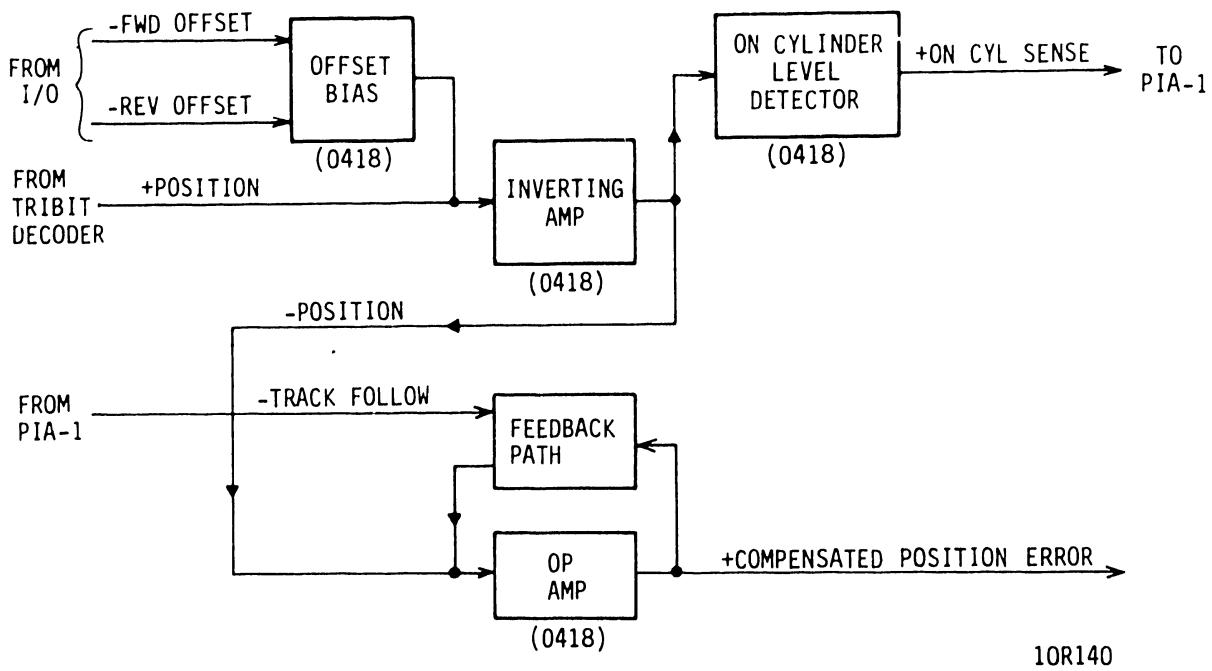


Figure 1-40. Position Error Circuitry

The position error circuitry consists of two op amps and a level detector. The first op amp inverts -Position and applies it with an optional offset to the second inverting op amp and the level detector. An offset, a dc shift of the position signal, results when the controller issues a Servo Offset command in order to recover marginal read data. When the I/O Gate Array decodes Servo Offset Plus (Tag 3 and Bus bit 2), it activates -FWD Offset, and the Offset Bias circuit shifts the position signal about 0.75 V negative. When the I/O Gate Array decodes Servo Offset Minus (Tag 3 and Bus bit 3), it activates -REV Offset, and the Offset Bias circuit shifts the position signal about 0.75 V positive. Servo Offset Plus displaces the heads inward from track center.

The -Position signal from the first op amp inputs both the On Cylinder level detector and the second op amp. The second op amp develops the +Compensated Position Error signal which is used as an error signal for both the settle-in and track-following modes. This op amp has an analog gate in its feedback path that makes its operation different in settle-in mode than it is in track-following mode.

For both settle-in and track-following, the +Compensated Position Error signal passes through a phase-shifting network before being applied to the Summing Amp input. This network, shown in figure 1-39, consists of a resistor which is in parallel with a series-RC differentiator. Adding a differentiated component to the error signal improves the stability of the fine servo loop. Prior to settle-in ($T > 1/2$ track), an analog gate presets the capacitor charge by sampling the +Current signal to permit a smooth transition from the coarse to the settle-in mode. When -Settle-In goes active, it disables that analog gate, allowing the phase-shifting network to operate. A second analog gate is switched on to pass the error signal on to the Summing Amp input.

When the position signal drops to 0.75 V, the On Cylinder level detector activates +On CYL Sense signal to generate an interrupt via PIA-1. The MPU responds to this interrupt by activating the -Track Follow line, and issuing On Cylinder status to the I/O Gate Array. The servo enters track-following mode to maintain the heads on track until a new seek command appears.

When -Track Follow goes active, an analog gate modifies the feedback path for the second op amp in the position error circuitry. This change increases the low-frequency gain of that amplifier to provide tighter servo control in track-following.

Thus, the Summing Amp receives a different input in each seek mode. Response of the servo circuitry to the Summing Amp input is summarized in the next topic.

Fine Loop Actuator Movement

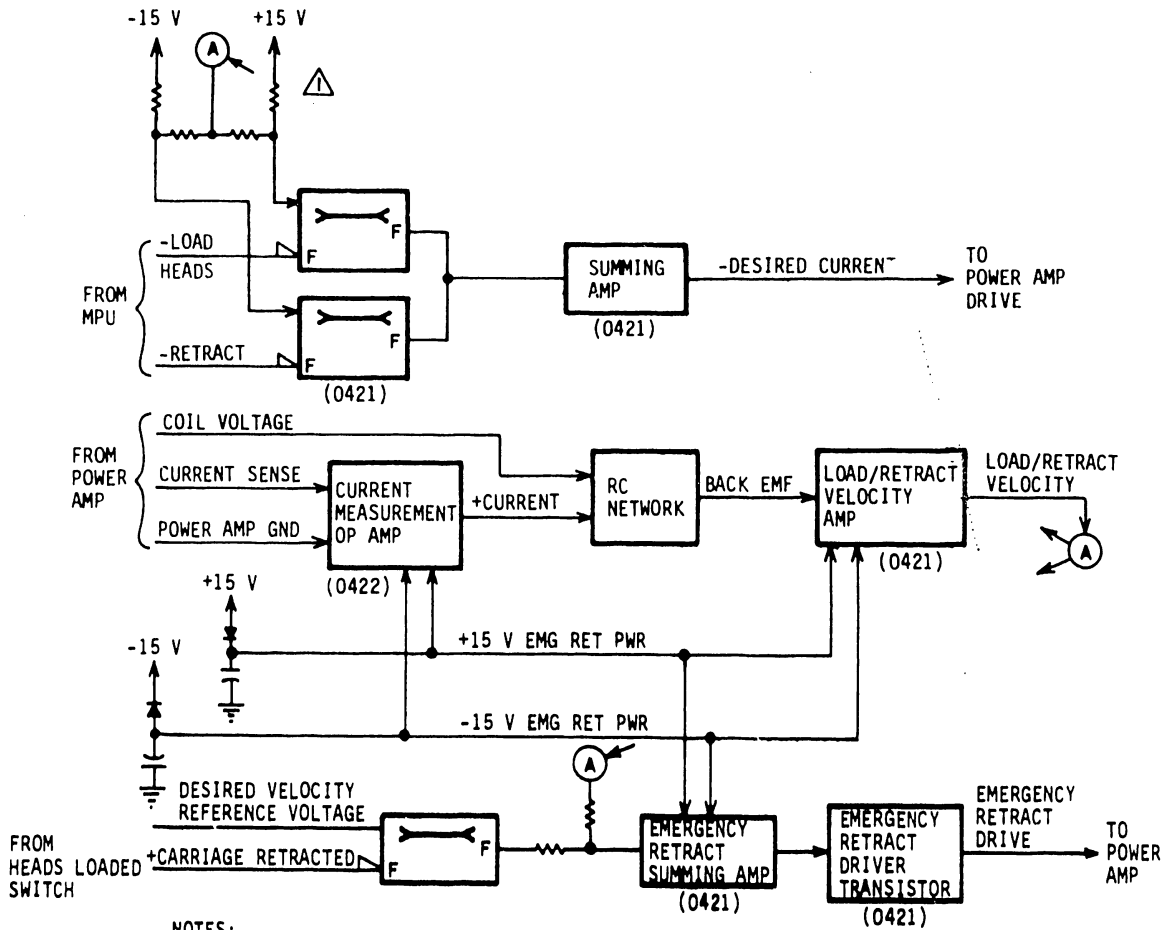
In the fine loop, as in the coarse loop, the Summing Amp develops the -Desired Current signal in response to its input error signal. The Power Amp Drive and Power Amp, acting as a current feedback amplifier, develop current in the actuator to match the -Desired Current input signal. This actuator current moves the heads toward track center. As the heads move toward track center, the position error signal goes to zero. The loop is balanced when the heads are at track center and the Summing Amp input is nulled. With a positive Summing Amp input, -Desired Current is negative; this results in positive actuator current and inward force on the heads.

For details about this circuit operation, refer to the following topics presented under Coarse Loop Operation:

- Summing Amp
- Power Amp Drive
- Power Amp

Load/Retract Servo Loops

The load servo loop moves the actuator inward from the fully retracted position at a constant velocity. The normal and emergency retract servo loops move the actuator outward to the fully retracted position at a constant velocity. All three loops differ in their external control; however, they employ similar operating principles. Figure 1-41 is a block diagram of the servo loops. They are described in the following paragraphs.



NOTES:

- VOLTAGE DIVIDER PROVIDES FIXED LEVELS OF DESIRED VELOCITY FOR NORMAL RETRACT AND FOR LOAD.

10R141A

Figure 1-41. Load/Retract Loops Block Diagram

In all three loops, the actuator is driven to balance the measured load/retract velocity signal against a fixed desired velocity. The desired velocity signal for each case is developed by a fixed dc reference potential applied to the loop while actuator motion is required. The load/retract velocity circuit develops a velocity signal by measuring the back-emf induced in the actuator coil. The back-emf is obtained indirectly at the circuit input, where measurements of actuator current and potential are applied to an R-C network. The load/retract velocity signal is a negative analog voltage during inward motion and a positive analog voltage during outward motion. Furthermore, since it is independent of the servo position signal, this velocity signal is valid for any position of the servo head.

The load and normal retract servo loops are switched into operation by MPU commands applied to their respective analog gates. The MPU issues the Load Heads command to switch on one analog gate that applies both a positive dc reference voltage and the load/retract velocity signal to the Summing Amp. The MPU issues the Retract command to switch on a different analog gate that applies a negative dc reference voltage but the same velocity signal to the Summing Amp. As in the coarse and fine loops, the Summing Amp develops the -Desired Current signal in response to its input error signal. The Power Amp Driver and Power Amp, acting as a current feedback amplifier, develop current in the actuator to match the -Desired Current input signal. This current moves the heads inward at 4 ips in a load or outward at 10 ips in a normal retract. Current continues to flow in the actuator until the MPU drops the Load or Retract command. Details about the operation of the Summing Amp, Power Amp Driver, and Power Amp are given under Coarse Loop Operation.

The emergency retract servo loop is switched into operation when the Retract Relay in the Power Amp deenergizes, allowing the Emergency Retract Power Amplifier to supply current to the actuator (see Emergency Retract Operations). As long as the heads are loaded, the Emergency Retract Summing Amp has two inputs -- a negative potential representing desired velocity and the load/retract velocity signal. To bring the load/retract velocity up to desired velocity, the Emergency Retract Summing Amp forward biases the Emergency Retract Driver. This driver inputs -Emergency Retract Drive current to the Power Amp board to bias the Emergency Retract Amplifier. This amplifier delivers current to the actuator coil to move the heads outward at 10 ips. The process continues until the heads are unloaded. At this time, an analog gate switches off to null the summing amp input.

The emergency retract servo loop must operate at times when power loss occurs. For this reason, the chips in the load/retract velocity circuit and the Emergency Retract Summing Amp are supplied with operating voltages (+15 Vdc) by slowly discharging capacitors. In addition, the Emergency Retract Power Amplifier has two voltage sources -- +24 Vdc from the power supply and the voltage generated by the decelerating drive motor. The power amplifier develops actuator current from the source with the highest potential.

TYPES OF SEEKS

General

The drive has four basic types of seeks: the load operation, normal seek, return to zero (RTZ) seek, and retract operation. The load and RTZ operations use both the outward and inward movements to move the actuator to track 0. The Retract operation is an outward movement that moves the heads completely out of the disk pack. Normal seek operations can be either inward or outward movements, depending upon where the new address is located relative to the present address. The four basic seek operations are discussed in the following text.

Load Operation

The load operation is an MPU-controlled sequence that starts the drive motor, moves the heads from the retracted position to track 0, scans the disks, and calibrates the velocity measurement circuitry. A load operation cannot take place until power on initialization is successfully completed. Refer to the Power Functions discussion for details about power on initialization. The load operation is described in the following paragraphs and is flowcharted in figure 1-42.

When power on initialization is complete, the MPU waits for start conditions before initiating the load operation. The MPU requires that the START switch is placed in the Start position and (in remote operation) that Sequence Hold is available from the controller. With start conditions present, the MPU looks at three interlock inputs to the PIAs to ensure that a data pack is in place, that the heads are unloaded, and that the front door is locked. These checks indicate that it is safe to start the drive motor.

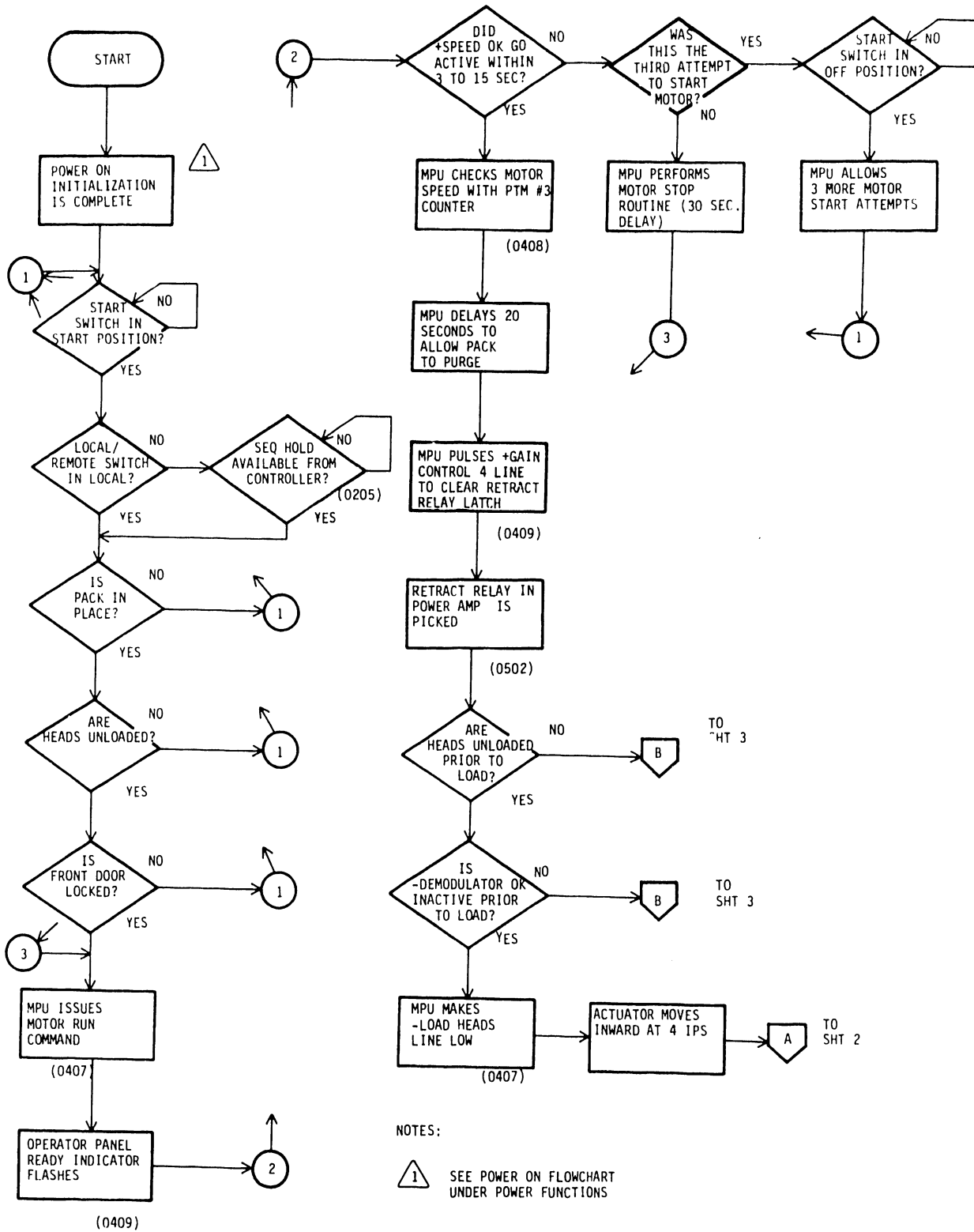


Figure 1-42. Load Operation Flowchart (Sheet 1 of 3)

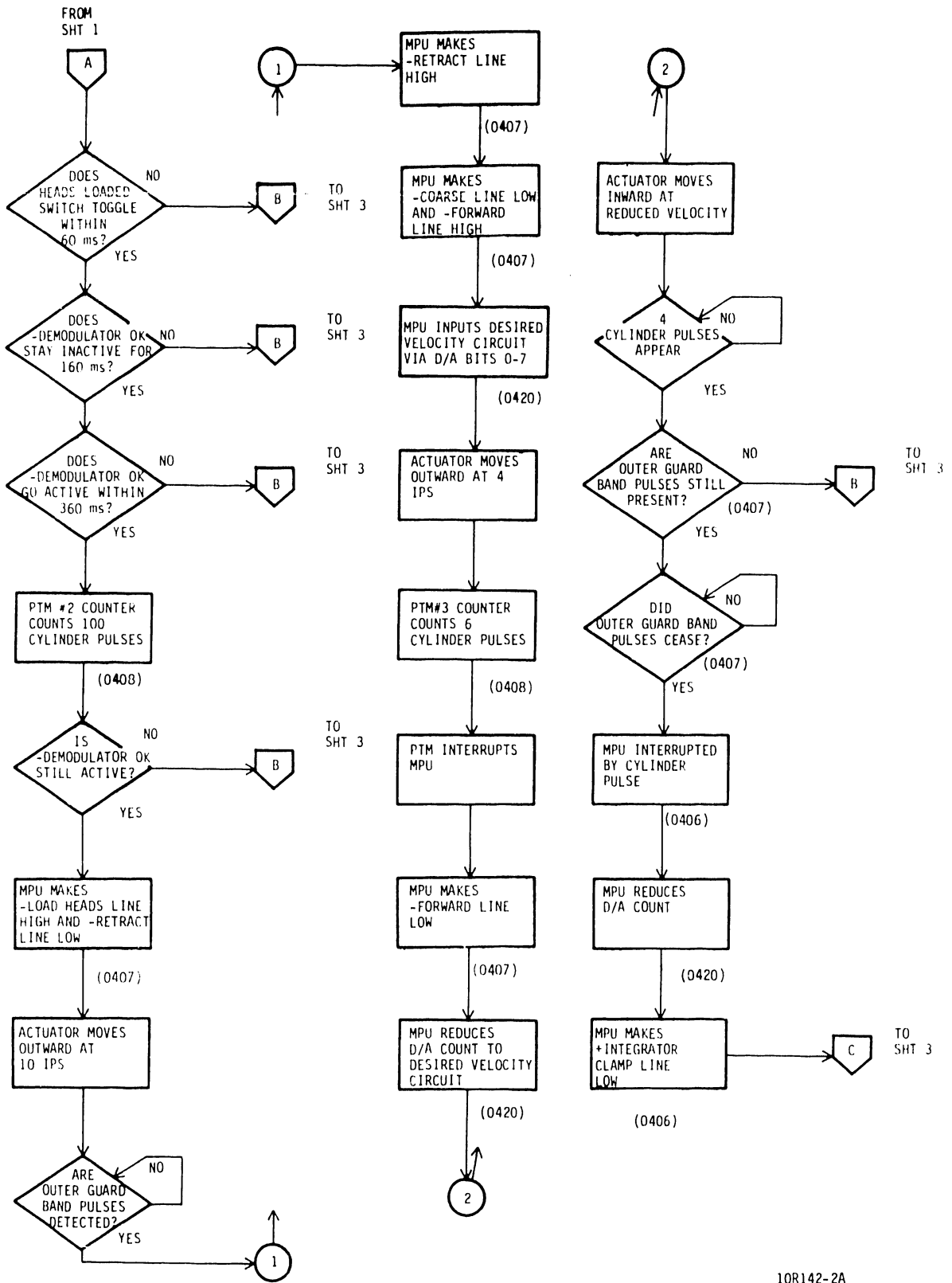
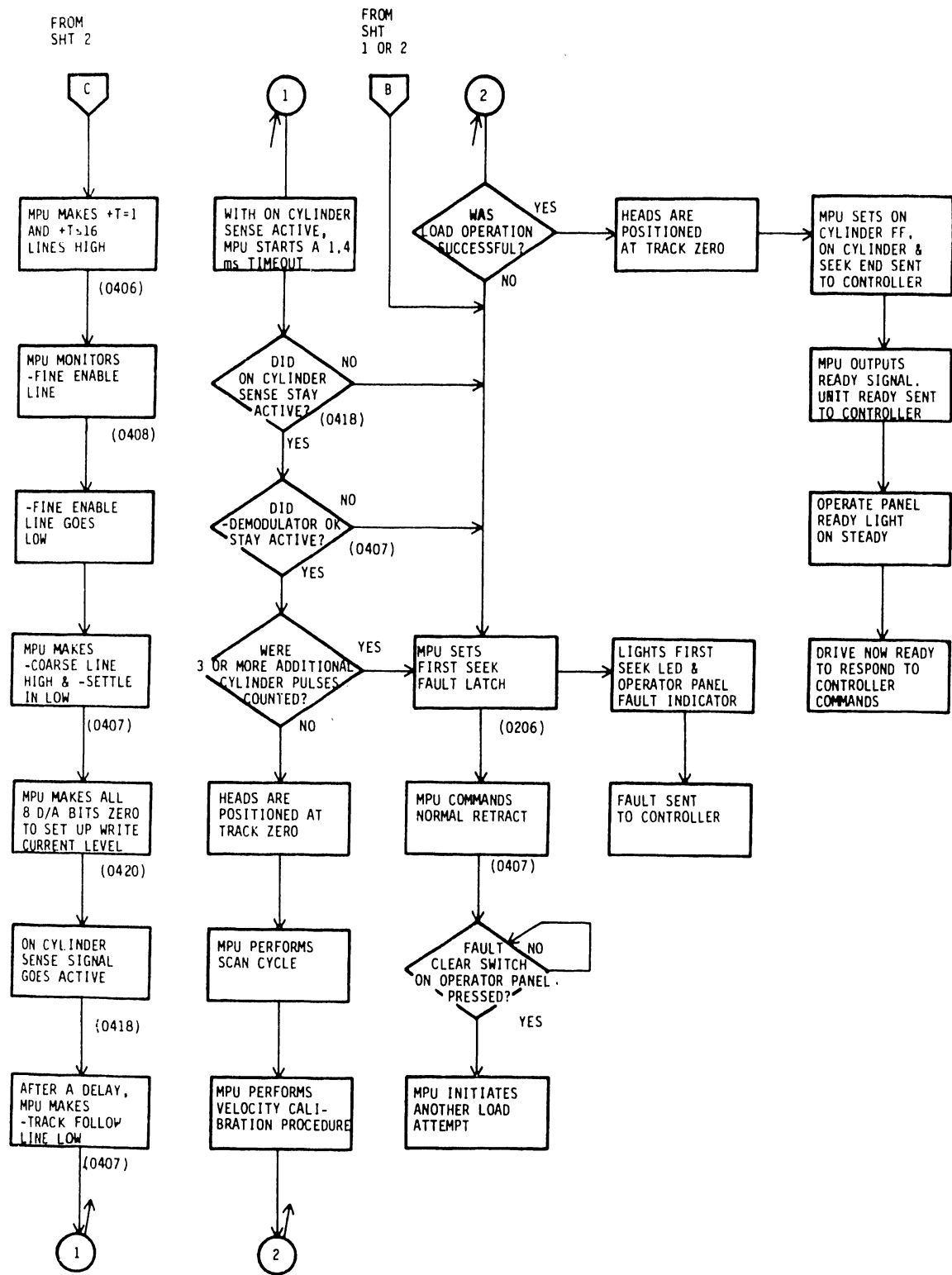


Figure 1-42. Load Operation Flowchart (Sheet 2)



10R142-3

Figure 1-42. Load Operation Flowchart (Sheet 3)

The MPU starts the drive motor by issuing the Motor Run command to the Motor Speed Control (via PIA-1) and requires that the +Speed OK line from the Motor Speed Control goes high after a delay from 3 to 15 seconds. Operation of the Motor Speed Control and drive motor is discussed under Electromechanical Functions. With Speed OK, the MPU doublechecks motor speed by counting -Motor Sensor pulses entering PTM #3. The MPU allows 20 seconds to elapse before loading the heads to ensure adequate filtering of the air in the disk pack.

To start the heads moving inward, the MPU picks the retract relay in the power amp and issues the Load Heads command. To activate the -Pick Retract Relay signal, the MPU clears the Retract Relay latch by pulsing the Gain Control 4 line to clock the low D-input (-Motor Run) into the latch. When the retract relay is energized, actuator control switches from the Emergency Retract amplifier to the In Direction amplifier. The heads move inward under control of the load servo loop at 4 ips.

During the load seek, the MPU monitors both the -Demodulator OK and the -Heads Loaded Switch lines. The MPU requires that the following normal conditions exist:

- The heads start from the unloaded position.
- The Tribit Decoder is inactive when the heads are unloaded.
- The heads loaded switch toggles within the first 60 ms of the load seek.
- The Tribit Decoder becomes stable after 160 ms but within 360 ms of the start of the load seek.

When the -Demodulator OK line goes low, indicating that the Tribit Decoder is active, the MPU orders the PTM #2 counter to count 100 Cylinder Pulses prior to reversing head motion. The heads continue to move inward at 4 ips for 100 tracks, and their motion takes them into the data zone to the point where their direction changes. Figure 1-43 shows the carriage trajectory during the load seek. At the turning point, the MPU drops the Load Heads command, validates the -Demodulator OK signal, and issues the Retract command.

The servo continues to use the load/retract loop; however, the switchover from load to retract changes the specified velocity from 4 ips inward to 10 ips outward. The servo continues this movement until the MPU is interrupted by Outer Guard Band

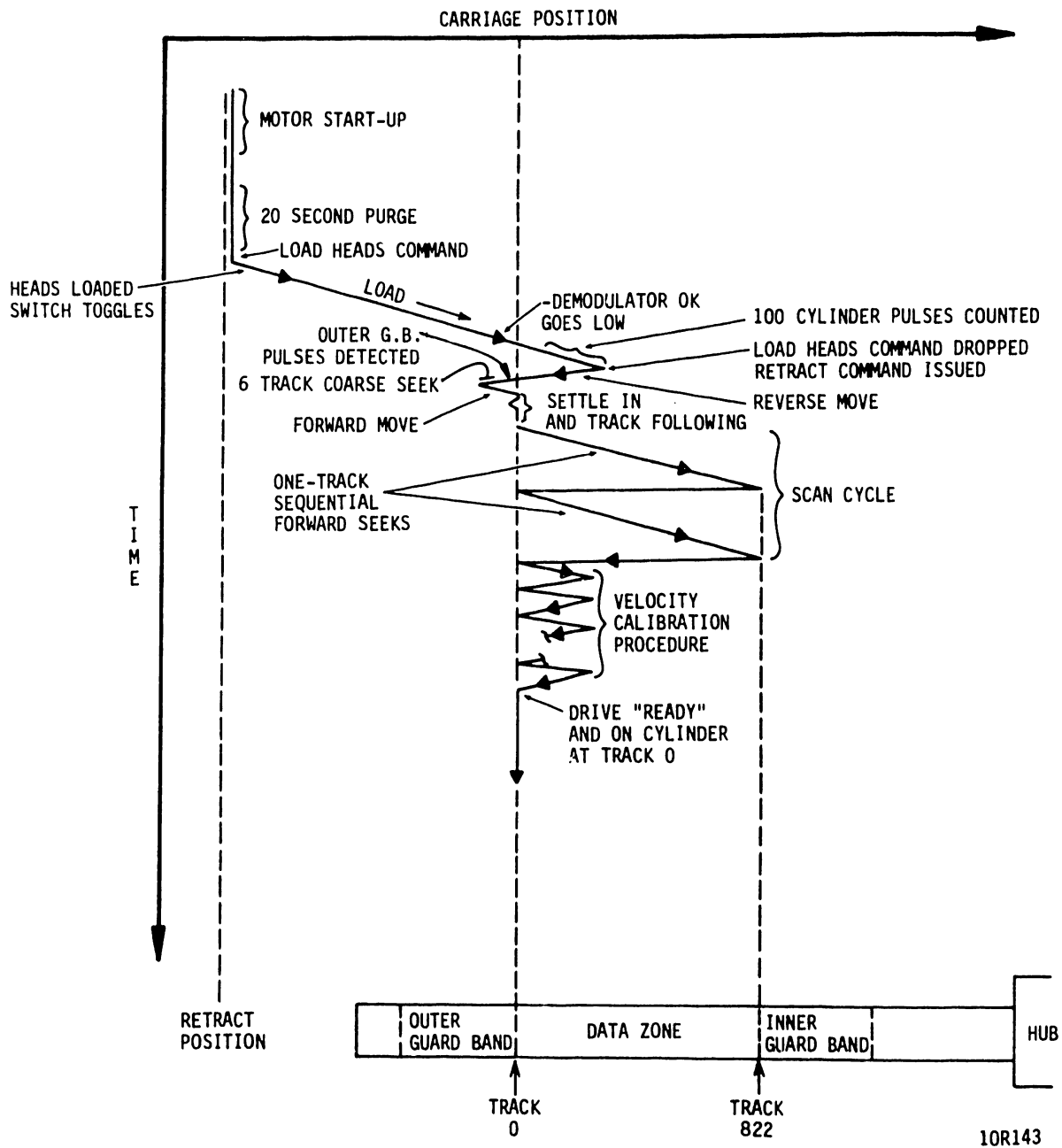


Figure 1-43. Load Seek Trajectory

Pulses when the heads move out of the data area. The MPU reacts by dropping the Retract command and by using the coarse servo loop to move the heads outward an additional six tracks into the outer guard band. To do this, the MPU makes the -Forward line high and the -Coarse line low and generates a D/A converter input corresponding to a desired velocity of 4 ips.

When PTM #3 has counted the six Cylinder Pulses for this move, it interrupts the MPU. The MPU reacts by changing several coarse loop inputs. It issues the Forward command to make the heads seek inward and reduces the desired velocity specified by D/A bits 0-7. The MPU requires that four cylinder pulses appear before Outer Guard Band Pulses cease (or it sets the First Seek fault latch). After Outer Guard Pulses cease, the MPU waits for one additional cylinder pulse representing the last track crossing before track 0.

When this cylinder pulse interrupts the MPU, the MPU reduces the D/A Converter velocity signal further (via D/A bits 0-7) and activates the Velocity Integrator by clearing the +Integrator Clamp line. The MPU also sets the +T=1 and the +T<16 lines to control the level of Integrated Velocity contributing to the Desired Velocity signal. With a constant D/A input from the MPU and the Velocity Integrator ramping up, the Desired Velocity signal approaches zero as the Integrated Velocity signal subtracts more and more from the D/A Converter velocity signal.

The MPU monitors the -Fine Enable signal. This signal goes low with approximately 1/3 of a track to go. The MPU reacts by switching the -Coarse signal high and the -Settle In signal low via PIA-1 to place the servo in the first (track-capture) phase of the fine servo loop. At this point, the MPU inputs the eight most significant cylinder address bits (all zeros) to the D/A Converter so that it can generate Write Current Level.

The MPU looks for the On Cylinder Sense signal (which goes high when the Position signal reaches 0.75 V) from the servo level detect circuits, and (after a delay) issues the Track Follow command via PIA-1. The Track Follow signal adds a low frequency gain boost to the positioning loop. The MPU again checks for an active On Cylinder Sense signal, and then allows a 1.4 millisecond timeout to ensure that the actuator has settled on track. At the end of the timeout, the MPU performs the scan cycle and the velocity calibration procedure if the settle-in occurred without excessive overshoot (less than three cylinder pulses seen after On Cylinder Sense went high) and if the -Demodulator OK line remained low (indicating a reliable servo signal). Otherwise, the MPU sets the First Seek fault latch and terminates the load operation.

In the scan cycle, the MPU commands two seek sequences. Each sequence consists of forward one-track seeks starting at track 0 and ending at track 822, followed by a seek to track 0. The velocity calibration procedure follows the scan cycle.

In the velocity calibration procedure, the MPU commands a series of 128-track normal seeks where it adjusts the gain of the velocity measurement circuit in order to compensate for gain variations in the servo disk. The gain is adjustable in steps depending on which combination of the four gain control lines is set. Upon finding the optimum combination of settings, the MPU maintains that combination (output from PIA-0) until the first load operation is repeated.

With the velocity calibration procedure complete, the heads are positioned at track 0. If the load operation was successful, the MPU issues the Ready signal at PIA-0 and sets the On Cylinder FF in the I/O Gate Array. The front panel Ready indicator lights, and On Cylinder, Seek End, and Unit Ready status appear on the interface. The MPU then waits for further instructions from the controller.

If the load operation was unsuccessful, the MPU performs a normal retract, sets the First Seek fault latch, and lights the front panel FAULT indicator. This fault can be cleared only by operation of the Fault Clear switch. Pressing the Fault Clear switch initiates another load attempt with a maximum of three tries allowed by the MPU.

Normal Seek

Normal seeks are initiated by controller command and implemented by the drive servo circuitry. The normal seek is the operation used to move the heads from one location to another on the disk surface. The same track can also be selected, but a zero track seek requires no actuator movement and the operation is handled by the I/O Gate Array.

The normal seek occurs in two directions, reverse (from the center towards the outer edge) and forward (from the outer edge towards the center). Going from a higher-numbered track to a lower-numbered one involves an out direction movement of the actuator, while going from a lower-numbered track to a higher-numbered one involves an in movement. Figure 1-44 is a detailed flowchart showing the normal seek operation.

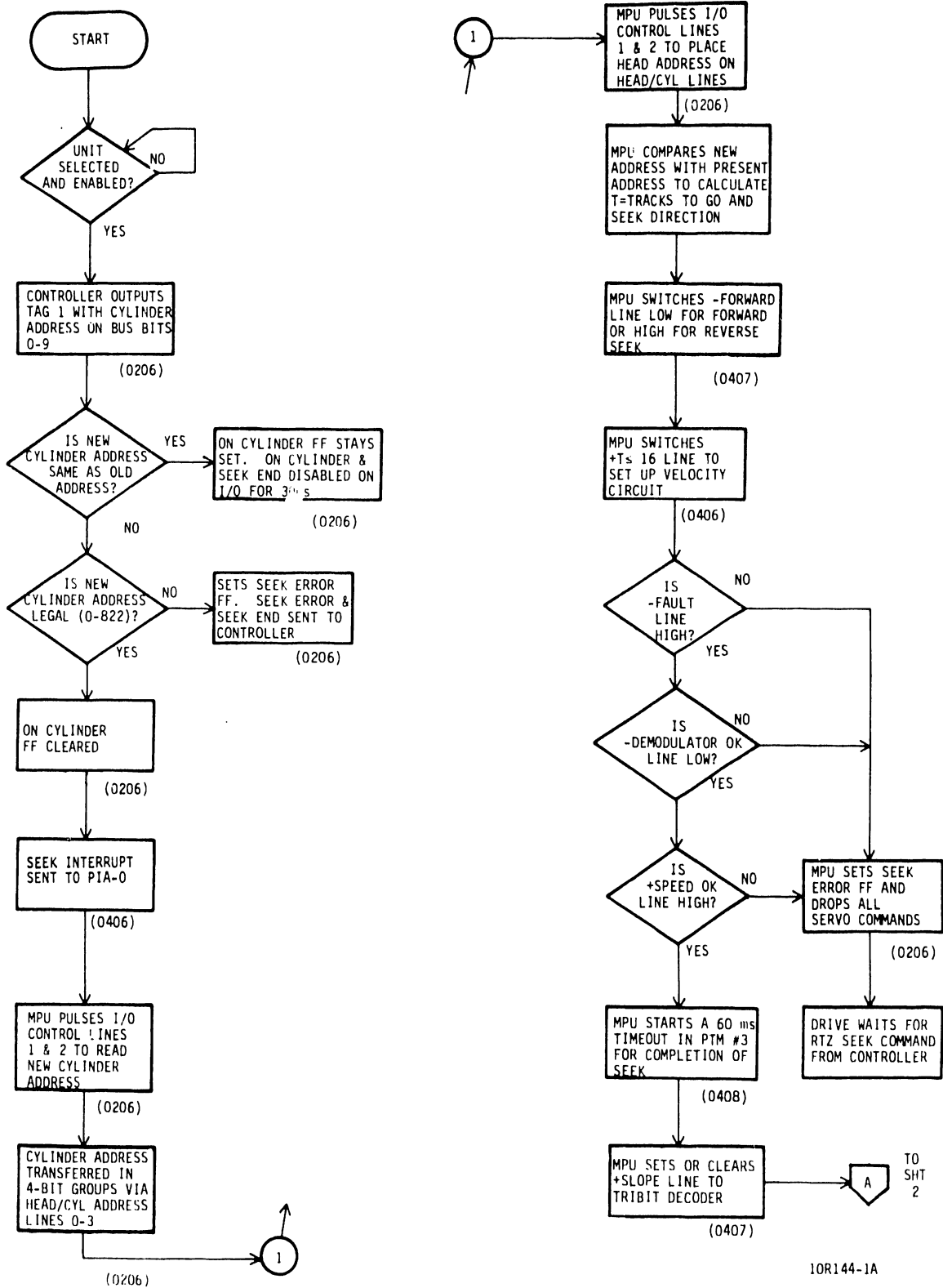
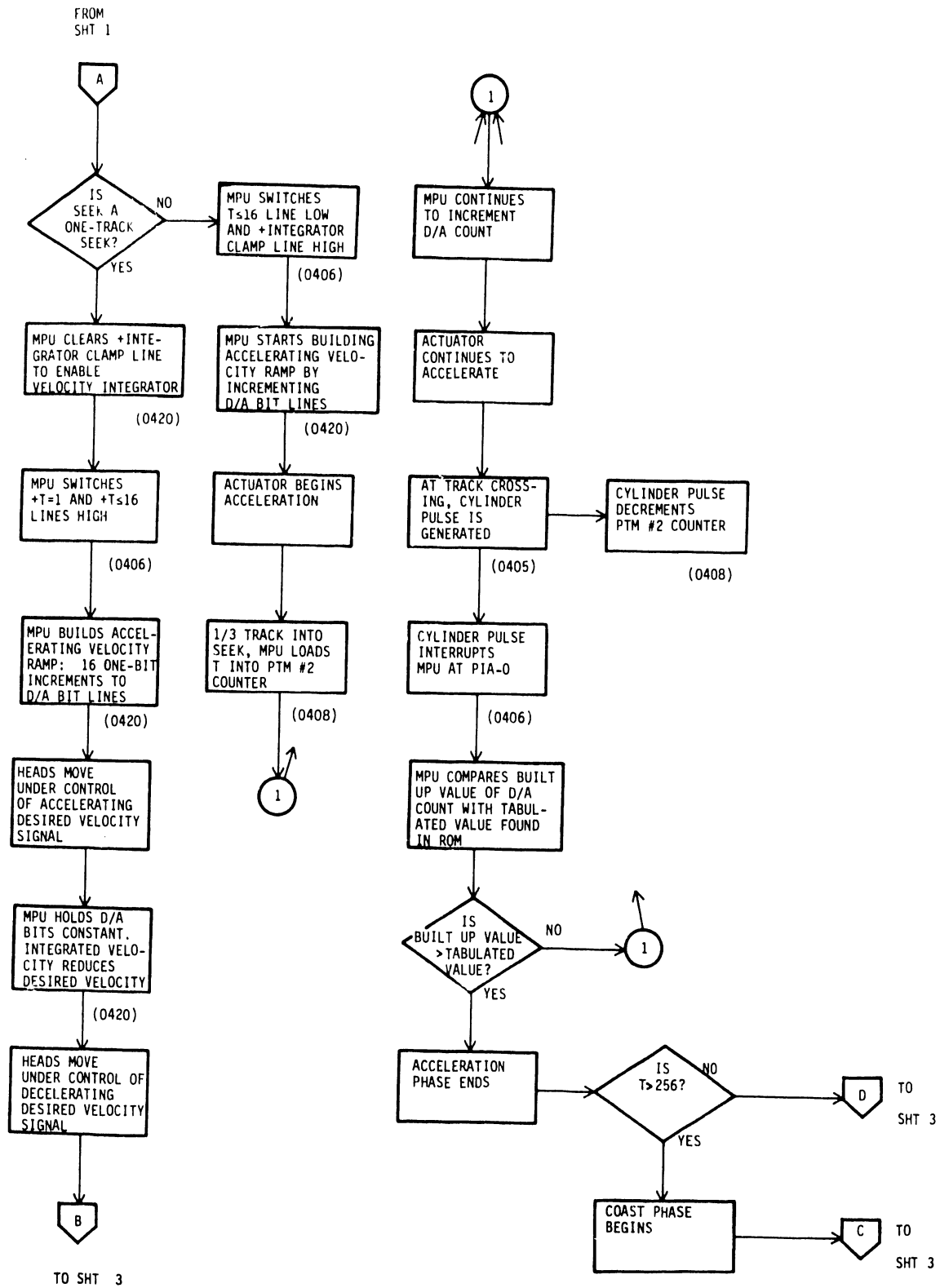
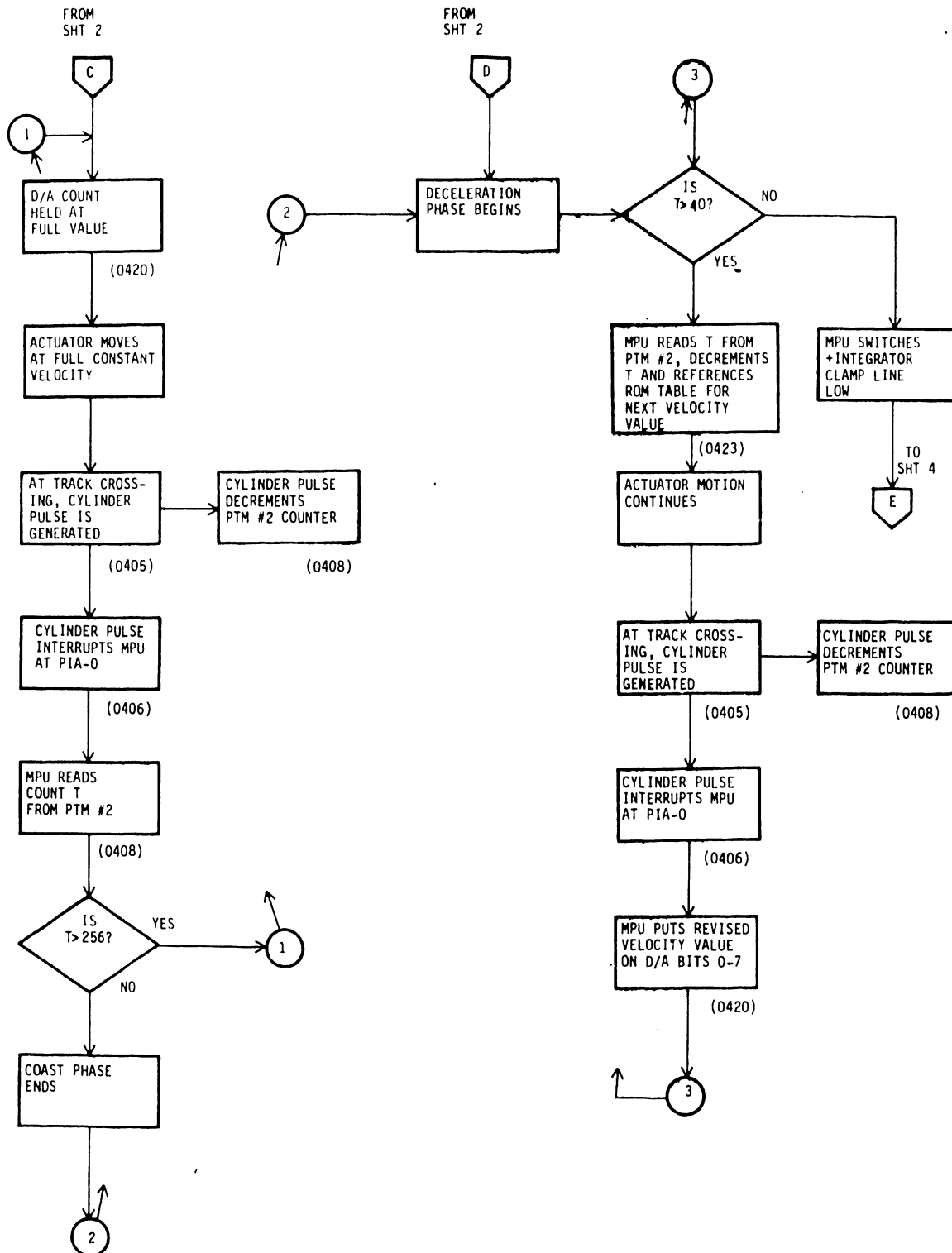


Figure 1-44. Normal Seek Flowchart (Sheet 1 of 5)



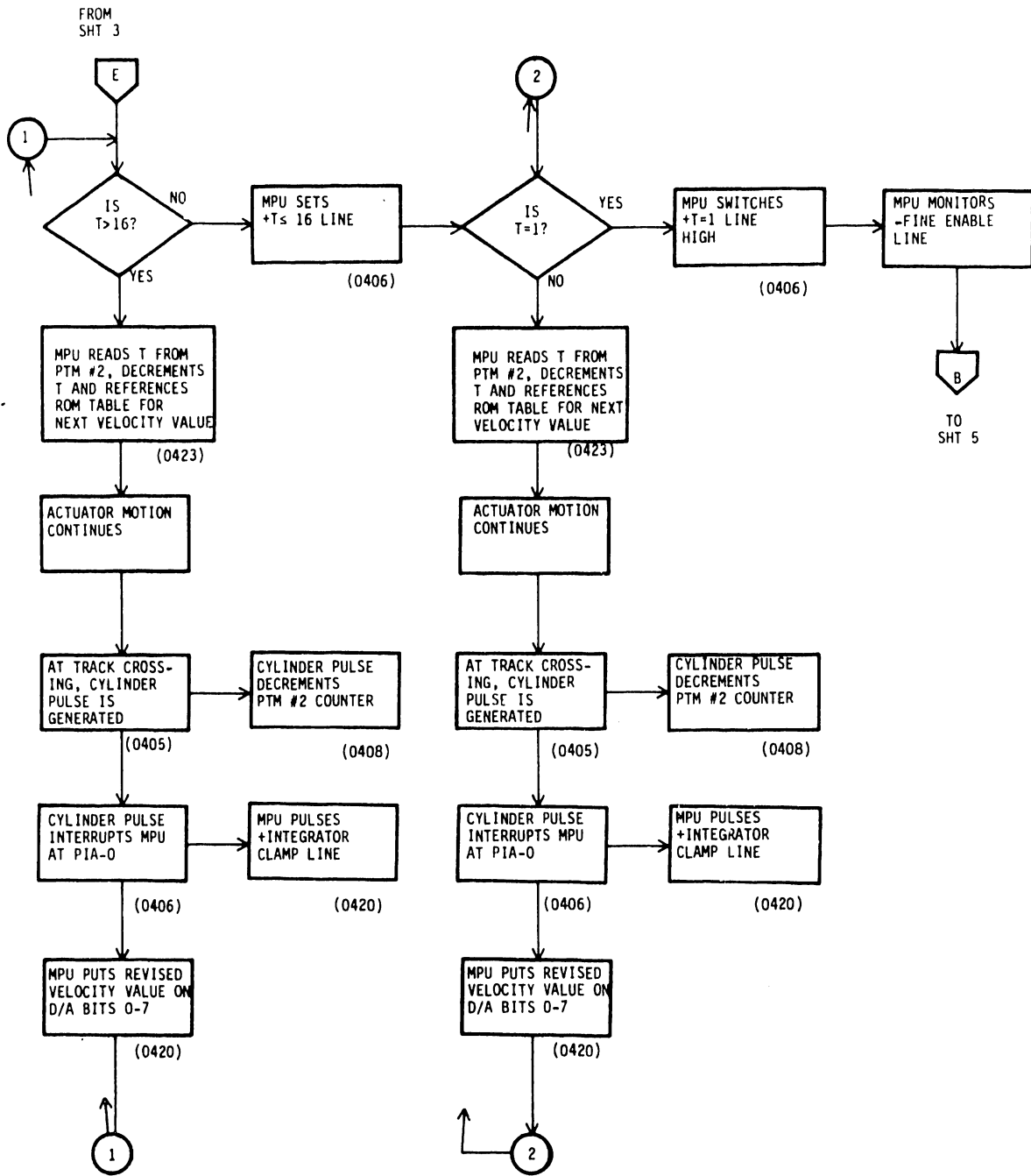
10R144-2

Figure 1-44. Normal Seek Flowchart (Sheet 2)



10R144-3

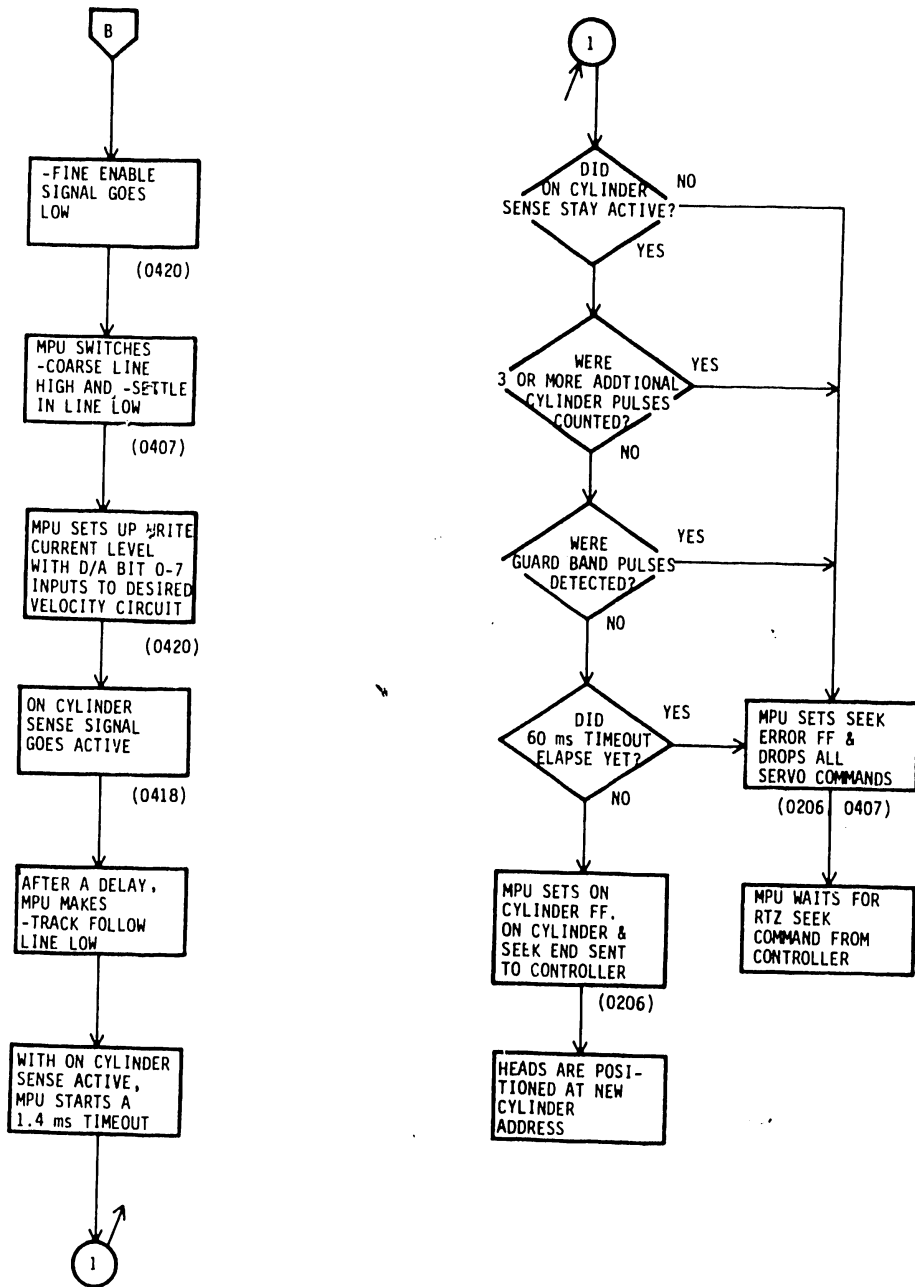
Figure 1-44. Normal Seek Flowchart (Sheet 3)



10R144-4

Figure 1-44. Normal Seek Flowchart (Sheet 4)

FROM SHT 2
OR SHT 4



10R144-5A

Figure 1-44. Normal Seek Flowchart (Sheet 5)

With the drive in the unit ready and on cylinder conditions, the controller initiates a normal seek by raising the Tag 1 (Cylinder Select) signal and placing the desired cylinder address on the Bus bits 0 through 9. The address is gated into the Cylinder Address register (in the I/O Gate Array) by the Cylinder Select Tag.

Inside the I/O Gate Array several processes take place. If the controller issues a seek command to an address greater than track 822, a decoder inside the gate array recognizes this as an illegal address and sets the Seek Error FF. The On Cylinder line remains set, and no Seek Interrupt is enabled to PIA-0. If a new seek command leaves the Cylinder Address register contents unchanged (a zero-track seek), the On Cylinder line remains set and no Seek Interrupt is enabled to PIA-0. If a new seek command requires a seek to a different (legal) seek address, however, the Cylinder Select tag clears the On Cylinder FF and triggers a one-shot that sends Seek Interrupt to PIA-0. The MPU responds to this interrupt by initiating a seek routine.

The MPU transfers the destination cylinder address from the I/O Gate Array into its RAM via PIA-0 by pulsing the I/O Control 1 and 2 lines. These control lines operate a multiplexer in the gate array to place the address, four bits at a time, on Head/Cylinder Address lines 0-3. After reading the cylinder address, the MPU pulses the control lines to cause the Head Address to be multiplexed onto Head/Cylinder Address lines 0-3.

The seek operation from this point until the on cylinder condition is achieved is under the control of the MPU programming. The program compares the new address with the present address (stored in RAM memory) to calculate the difference between the two (T =tracks to go) and the direction of the move (in or out).

In all seeks, the MPU presets certain signal lines to condition the coarse servo loop. The -Forward line is switched low for in direction seeks or high for out direction seeks. The MPU initializes the velocity measurement circuit by setting or clearing the Last Peak latch. It uses the $T_{<16}$ line to set or clear the latch when the -Track Follow line goes high. The MPU checks to make sure that there is no fault condition and that the Speed OK and Demodulator OK signals are active. If these conditions are met, the MPU loads the PTM #3 counter with a 60 millisecond timeout count (so that a Seek Error will be indicated if the seek is not completed at the end of the timeout). The MPU sets or clears the +Slope line to the tribit decoder circuit to ensure that the decoded position signal has the proper phase at the destination track. The MPU then starts the seek by making the -Track Follow line high and the -Coarse line low and by introducing an accelerating velocity profile to the Desired Velocity circuit.

The remaining coarse seek is very different for one-track seeks than it is for longer seeks. For one-track seeks, the MPU clears the +Integrator Clamp line, allowing the Velocity Integrator to generate the Integrated Velocity signal. The MPU also sets the $T=1$ and the $T<16$ lines to control the level of Integrated Velocity contributing to the Desired Velocity signal, and it builds an accelerating velocity profile by incrementing the D/A bits input to the D/A Converter one bit at a time. After 16 increments, the MPU holds the D/A input constant, and a decelerating velocity profile results as the Integrated Velocity signal ramps up. The Integrated Velocity signal subtracts more and more from the D/A Converter velocity signal to bring the Desired Velocity signal toward zero. The MPU monitors the -Fine Enable line, and it switches from coarse to fine loop operation when -Fine Enable goes low.

For seeks greater than one track, a different coarse seek sequence is managed by the MPU. The MPU builds an accelerating velocity ramp by incrementing the D/A bits entering the D/A Converter every 43 microseconds. At approximately 1/3 of a track into the seek, the MPU loads T , the number of tracks to go, into the PTM #2 counter. (A cylinder pulse, generated as the heads cross each track, decrements PTM #2 directly to keep the count T current.) The MPU continues to increment the D/A bit count, building up the velocity profile, until deceleration conditions are reached. This happens when the D/A count reaches the value specified in the PROM velocity table for the current value of T . For the remainder of the coarse seek, the MPU controls the D/A count based upon the velocity table. For long seeks, the D/A count stays at maximum (all bits set) and the carriage coasts at full velocity prior to actual deceleration.

Throughout the deceleration portion of the coarse seek, the MPU updates the D/A count at each cylinder crossing and activates the velocity integrator circuit once $T<40$. The MPU clamps integrated velocity to zero by pulsing the +Integrator Clamp line at each cylinder crossing and adjusts the level of the Integrated Velocity signal by means of four control lines to the circuit: $T<16$, $T=1$, D/A bit 6, and D/A bit 7.

When $T=1$, the MPU monitors the -Fine Enable signal. This signal goes low with approximately 1/3 of a track to go. The MPU reacts by switching the -Coarse signal high and the -Settle In signal low via PIA-1 to place the servo in the first (track-capture) phase of the Fine Servo loop. At this point, the MPU inputs the eight most significant cylinder address bits to the D/A Converter so that it can generate Write Current Level.

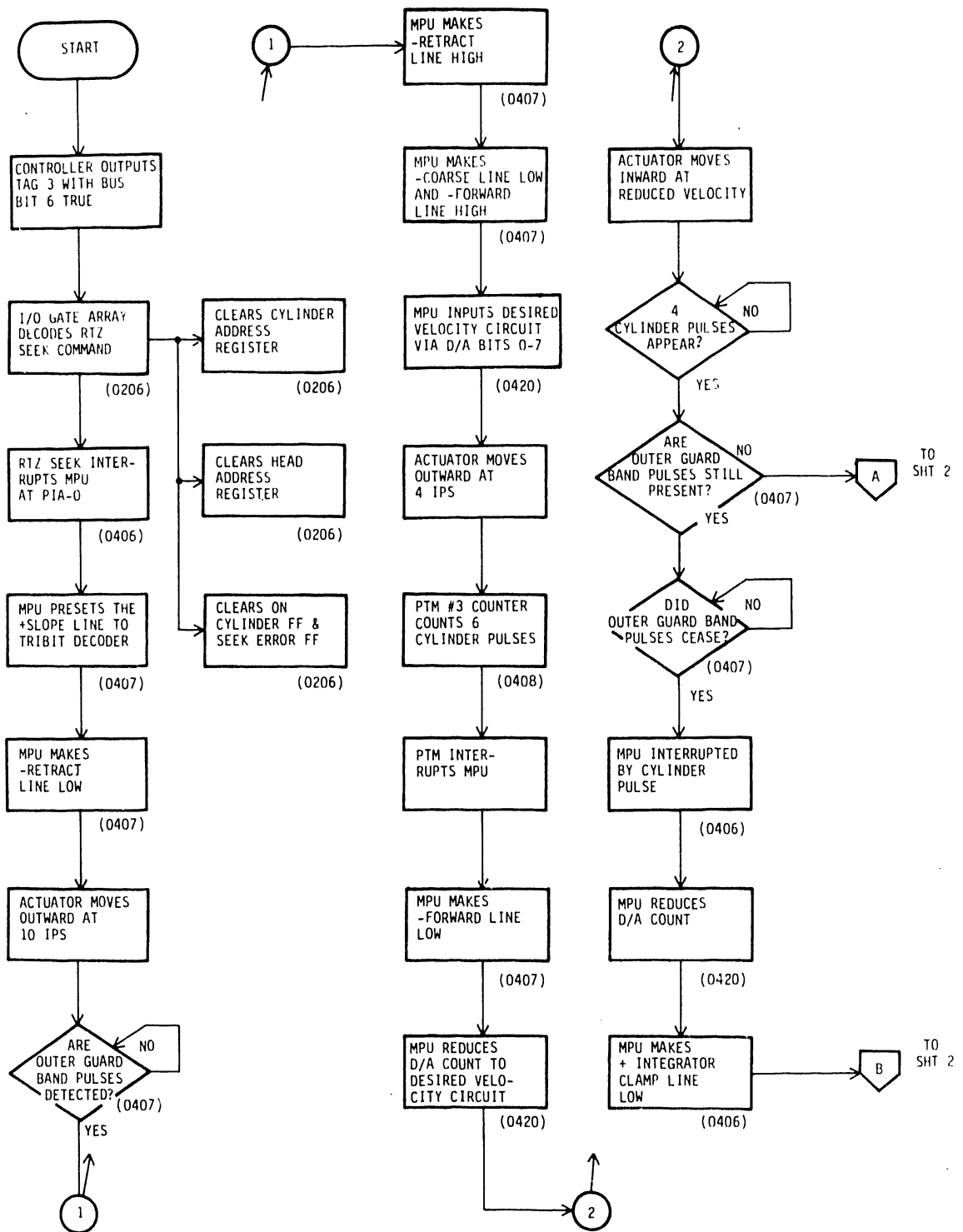
The MPU looks for the On Cylinder Sense signal (which goes high when the Position signal reaches 0.75 V) from the servo level detect circuits, and (after a delay) activates the Track Follow signal via PIA-1. The Track Follow signal adds a low frequency gain boost to the positioning loop. The MPU again checks for an active On Cylinder Sense signal, and then allows a 1.4 millisecond timeout to ensure that the actuator has settled on track. At the end of the timeout, the MPU ends the seek routine by setting either the On Cylinder FF or the Seek Error FF in the I/O Gate Array using I/O Control lines 1 and 2. It sets the On Cylinder FF provided that the -Demodulator OK line stayed low (indicating a reliable servo signal), that no guard band pulses were detected, and that settle-in occurred without excessive overshoot (less than three additional cylinder pulses detected). Otherwise, the MPU sets the Seek Error FF. In either case, the MPU then waits for further commands from the controller.

Return to Zero Seek

The Return to Zero (RTZ) seek is the operation that moves the heads from any location on the disk to track 0. Although the MPU uses an RTZ seek as part of the load operation, the controller can command RTZ seeks also. Both types of RTZ seeks are identical, except for the status presented if they fail. If the RTZ seek in a load operation is unsuccessful, the MPU lights the First Seek fault indicator, and a reattempt occurs only if the Fault Clear switch is pressed. If a controller-initiated RTZ seek is unsuccessful, the MPU sets the Seek Error FF, and Seek Error is active on the I/O. In this case, the drive waits for another RTZ command from the controller.

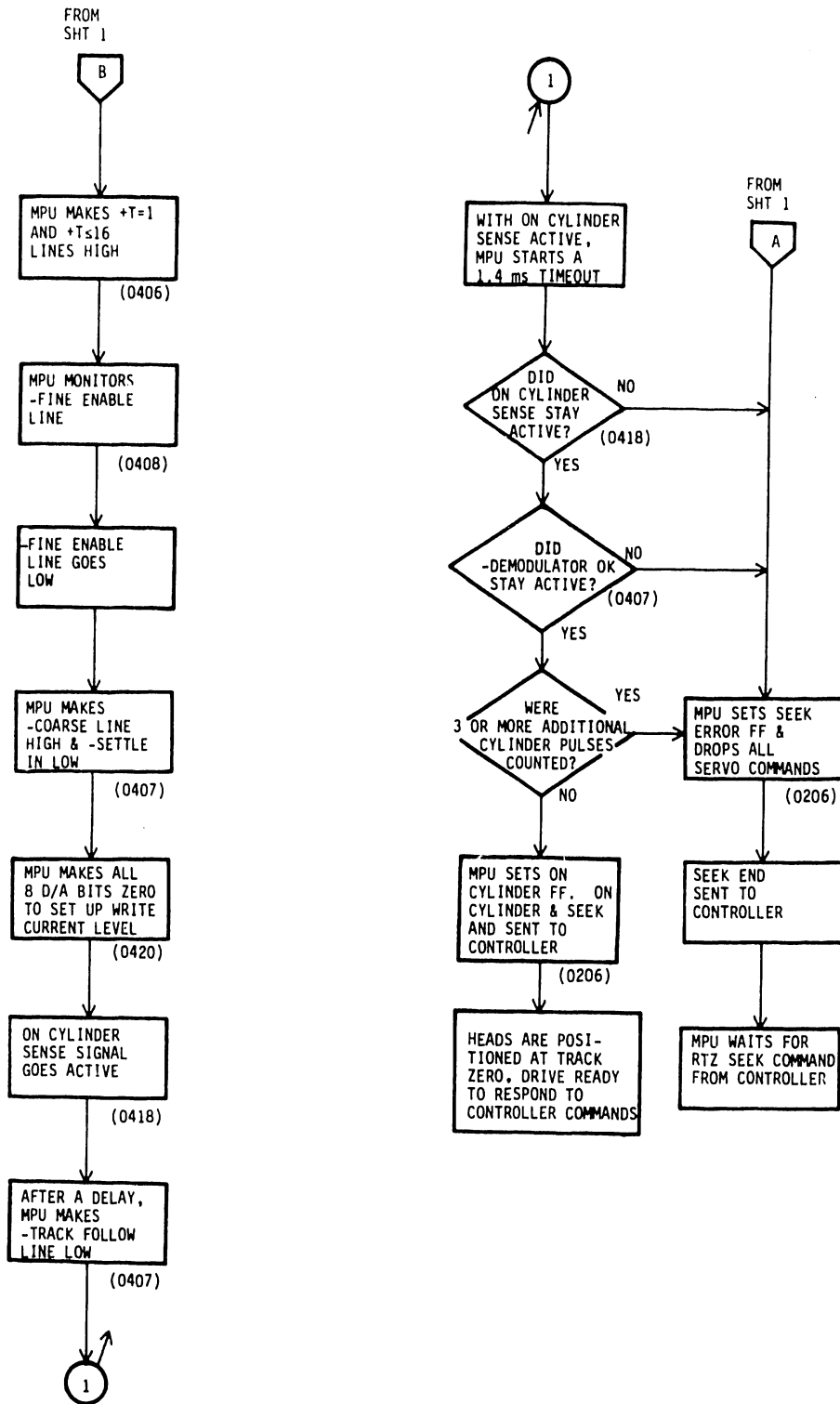
This discussion pertains specifically to the controller-initiated RTZ seek. This seek is flow-charted in figure 1-45. Refer to the Load Operation discussion for details about the RTZ portion of the load operation.

The controller initiates an RTZ operation by outputting Tag 3 (Control Select) along with Bus bit 6. The RTZ Seek command is decoded on the I/O Gate Array where it clears the Cylinder and Head Address registers, the On Cylinder FF, and Seek Error FF (all in the I/O Gate Array). In addition, the I/O Gate Array sends the RTZ interrupt to PIA-0 on the Control Board to generate an interrupt to the MPU.



10R145-1

Figure 1-45. Return to Zero (RTZ) Seek (Sheet 1 of 2)



10R145-2

Figure 1-45. Return to Zero (RTZ) Seek (Sheet 2)

The MPU reads the RTZ interrupt and initiates the RTZ. In the first portion of the RTZ, the servo uses the same loop as in normal retract operations. This loop monitors actuator velocity by measuring the back-emf induced in the actuator coil as it moves through the field of the permanent magnet. The retract portion begins when the MPU issues the Retract command at PIA-1. This enables both the measured retract velocity signal and a constant dc potential representing a desired velocity of 10 ips to the summing amp. The servo responds by moving the actuator outward at a controlled velocity of 10 ips.

The servo continues this movement until the MPU is interrupted by Outer Guard Band Pulses when the heads move out of the data area. The MPU reacts by dropping the Retract command and by using the coarse servo loop to move the heads outward an additional six tracks into the outer guard band. To do this, the MPU switches the -Forward line high and the -Coarse line low and generates a D/A converter input corresponding to a desired velocity of 4 ips.

When PTM #3 has counted the six Cylinder Pulses for this move, it interrupts the MPU. The MPU reacts by changing several coarse loop inputs. It issues the Forward command to make the heads seek inward and reduces the desired velocity specified by D/A bits 0-7. The MPU requires that four cylinder pulses appear before Outer Guard Band Pulses cease (or it generates Seek Error). After Outer Guard Pulses cease, the MPU waits for one additional cylinder pulse representing the last track crossing before track 0.

When this cylinder pulse interrupts the MPU, the MPU reduces the D/A Converter velocity signal further (via D/A bits 0-7) and activates the Velocity Integrator by clearing the +Integrator Clamp line. The MPU also sets the +T=1 and the +T \leq 16 lines to control the level of Integrated Velocity contributing to the Desired Velocity signal. With a constant D/A input from the MPU and the Velocity Integrator ramping up, the Desired Velocity signal approaches zero as the Integrated Velocity signal subtracts more and more from the D/A Converter velocity signal.

The MPU monitors the -Fine Enable signal. This signal goes low with approximately 1/3 of a track to go. The MPU reacts by switching the -Coarse signal high and the -Settle In signal low via PIA-1 to place the servo in the first (track-capture) phase of the fine servo loop. At this point, the MPU inputs the eight most significant cylinder address bits (all zeros) to the D/A Converter so that it can generate Write Current Level.

The MPU looks for the On Cylinder Sense signal (which goes high when the Position signal reaches 0.75 V) from the servo level detect circuits, and (after a delay) issues the -Track Follow command via PIA-1. The Track Follow signal adds a low frequency gain boost to the positioning loop. The MPU again checks for an active On Cylinder Sense signal, and then allows a 1.4 millisecond timeout to ensure that the actuator has settled on track. At the end of the timeout, the MPU ends the RTZ operation by setting either the On Cylinder FF or the Seek Error FF in the I/O Gate Array, using I/O Control lines 1 and 2. It sets the On Cylinder FF provided that the -Demodulator OK line stayed low (indicating a reliable servo signal) and that settle-in occurred without excessive overshoot (less than three cylinder pulses seen after On Cylinder Sense went high). Otherwise, the MPU sets the Seek Error FF. In either case, the MPU then waits for further commands from the controller.

Retract Operations

General

Retract operations withdraw the heads from the disk surfaces, forcing them out of the disk pack until they reach the fully unloaded position. When the heads are loaded over the disk surfaces, they fly on a cushion of air created by the spinning of the disks. Retract operations take place during the power off sequence or in the event of malfunctions in the power supply, servo positioning, or motor speed control circuitry that might lead to contact between the heads and disks. The following paragraphs describe the initiating conditions and the sequences involved in both normal retracts and emergency retracts.

Normal Retract Operations

Normal retract operations are initiated and controlled by the MPU in the following circumstances:

- When there is a problem forcing the MPU to abort a load operation.
- When the heads are loaded and the -Demodulator OK line goes high, indicating that the Tribit Decoder is inactive.
- When the MPU detects a loss of start conditions and initiates a power off sequence.

In addition, the MPU uses the retract function for portions of the outward movements in load operations and RTZ seeks, as described in the topics covering these operations.

The MPU initiates the normal retract operation by issuing the Retract command at PIA-1. This enables an analog gate that supplies the summing amp with the measured retract velocity signal and with a constant potential representing a desired velocity of 10 ips. As described under Servo Circuit Functions, the Power Amp Driver develops Out Drive Current that regulates the Out Direction Amplifier in the Power Amp board. Closed loop operation maintains the actuator velocity at 10 ips outward until the heads are unloaded. When the heads are fully retracted, the contacts on the Heads Loaded switch open, indicating to the MPU that the retract is complete. The MPU responds by dropping the Retract command and waiting for conditions that initiate another load operation.

Emergency Retract Operations

Emergency retract operations take place under hardware control and require no MPU intervention. They occur in the following circumstances:

- When a (Voltage + Actuator Current) Fault appears. This fault indicates a loss or drop in one or more dc voltages from the power supply or a malfunction in the power amp producing an overcurrent condition in the actuator.
- When the Motor Speed Control drops Speed OK, indicating that the drive motor speed is unacceptable (slower than 3578 r/min or faster than 3634 r/min).

Either condition deenergizes the Retract Relay in the Power Amp board, allowing the Emergency Retract Power Amplifier to supply current to the actuator coil. A circuit description of the servo loop that controls emergency retracts is given under Servo Circuit Functions. This servo loop moves the actuator at a controlled outward velocity of 10 ips. When the heads are fully retracted, the contacts of the Heads Loaded switch open. This removes the input bias to the loop. At this time, Emergency Retract Drive is cut off.

HEAD OPERATION AND SELECTION

GENERAL

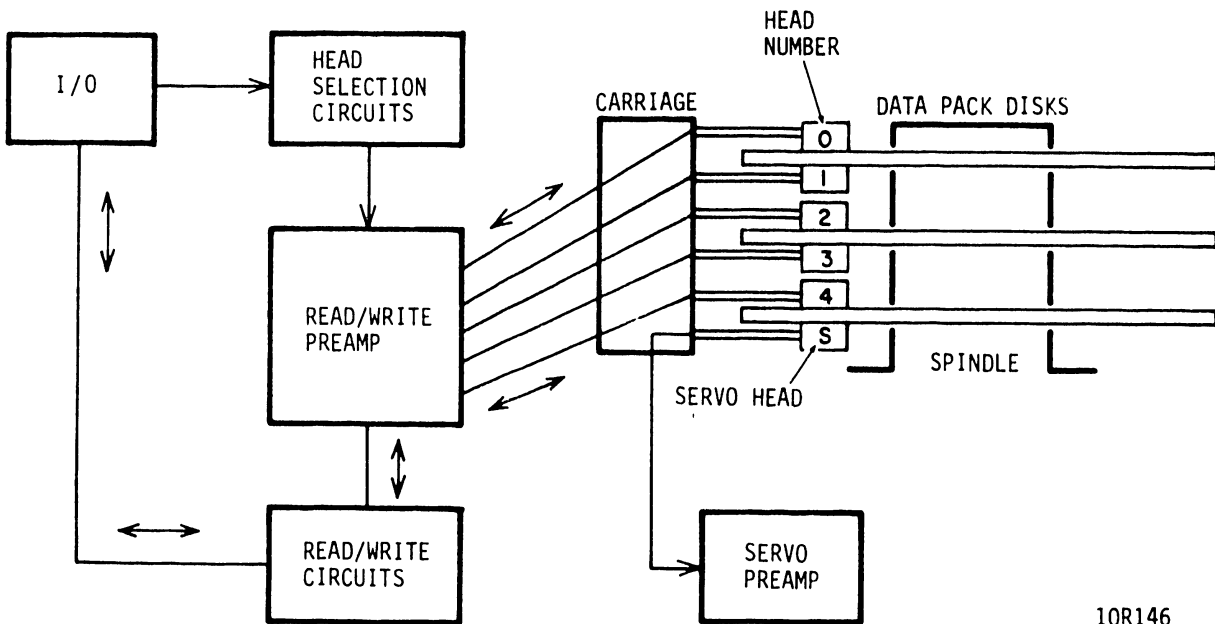
Information is recorded on and read from the disk by the read/write heads (refer to figure 1-46). The drive requires one read/write head for each recording surface in the data pack as shown. The drive has five recording surfaces. For this reason, before a read or write can be performed, the controller must command the drive to select the head located over the disk surface where the data is to be read or written.

The following discusses how the heads read and write the data and also how the desired head is selected.

HEAD FUNCTIONAL DESCRIPTION

Each read/write head has two opposing coils wound on the same core. The coils interface to the read/write circuitry via an LSI chip in the R/W Preamp. In response to the signal inputs, the LSI chip selects one of the five heads, and either provides current switching for the head in write operations or amplification of voltage induced in the head in read operations. Refer to Read/Write Functions for details about the R/W Preamp.

During write operations, the read/write head develops a changing flux pattern on the disk surface passing beneath it. The R/W Preamp supplies the selected head with a source of write current. At each transition of the write data signal, the preamp disables one coil and enables the other. Since the two coils have opposing windings, this switching reverses the flux across the gap in the head (see figure 1-47). The flux field magnetizes the iron oxide particles bound to the disk surface.



10R146

Figure 1-46. Read/Write Heads

Each particle is then the equivalent of a miniature bar magnet with a north pole and a south pole. The writing process orients the poles to store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of write current switching while its amplitude depends on the amount of current (the greater the current, the more oxide particles that are affected).

Information (data) is written by switching the current through the head. Switching between the two head coils reverses the direction of the flux field across the gap. The flux change defines a data bit.

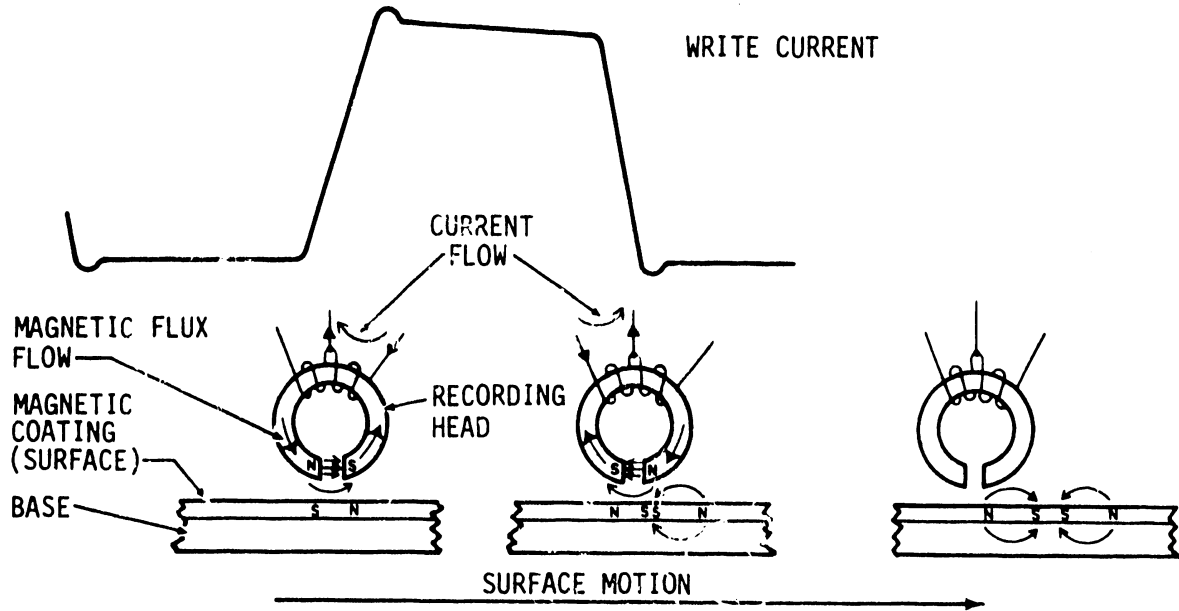
New data is written simply by writing over any data which may already be on the disk. The write current is zoned to ensure proper saturation level for best head resolution (refer to discussion on Write Current Control). The write current is maximum on the outer tracks and minimum for the inner tracks.

During a read operation, disk motion beneath the head causes the stored flux to induce a voltage in the heads (refer to figure 1-48). This voltage is analyzed by the Read circuit to define the data recorded on the disk. Each flux reversal (produced while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

HEAD SELECTION

A head must be selected before a read or write operation can be performed. Prior to head selection, the controller issues a cylinder select command. Under MPU control, the servo system moves the heads to the cylinder specified by the controller. By selecting a head, the controller specifies a particular track within that cylinder. Head selection starts when the controller sends the drive a Head Select (Tag 2) command and a head address. The head address is sent on Bus bits 0 through 2.

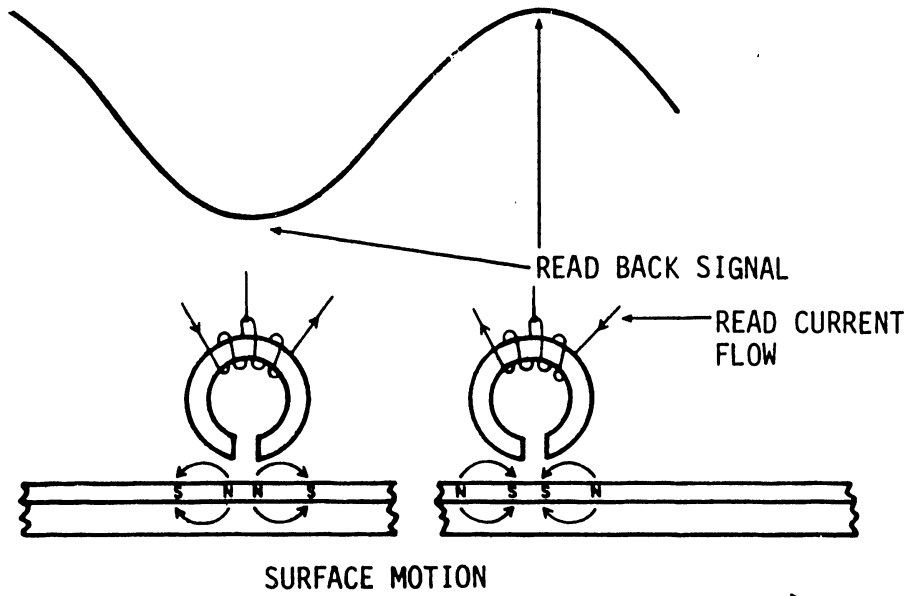
The Head Select tag gates the address into the Head Address register (HAR) in the I/O Gate Array. Figure 1-49 shows the head selection circuits. The cylinder address and the head address are multiplexed out of the gate array on +Head/Cylinder Address lines 0-3. The MPU controls this multiplexing with I/O Control lines 1 and 2. In the initial phase of a seek, the Head/Cylinder Address lines transfer the new cylinder address to the MPU. With this transfer complete, the lines carry head address information. Thus, whenever the heads are on cylinder, +Head Address line 0 reflects HAR bit 0, and so forth.



NOTE: (RELATIVE HEAD TO SURFACE MOTION, RECORDING (WRITE OPERATION))

10R129

Figure 1-47. Writing Data



NOTE: RELATIVE HEAD TO SURFACE MOTION, REPRODUCING (READ OPERATION)

10R130

Figure 1-48. Reading Data

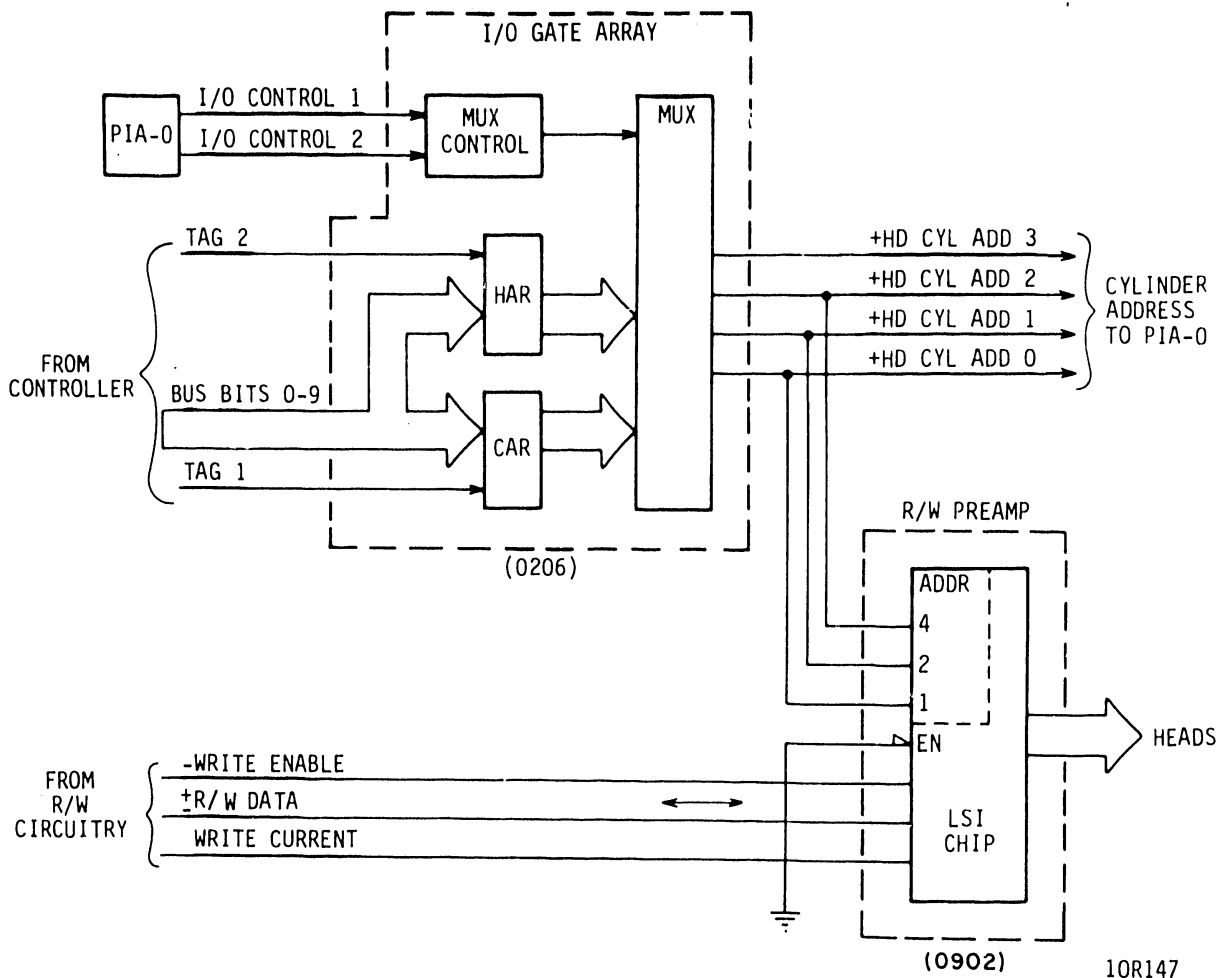


Figure 1-49. Head Selection Circuits

The Head/Cylinder Address lines go from the I/O board to the Data Latch board via the Control board. The Data Latch board sends Head/Cylinder Address lines 0-2 on to the R/W Preamp. (Head/Cylinder Address line 3 is not used for head selection in this drive.) The LSI chip in the preamp controls all five heads and enables one of the heads depending on +Head/Cylinder Address lines 0-2, which connect to its addressing inputs. If the preamp receives an illegal head address (5 through 7), no head is selected. A Write Fault occurs if the drive attempts to write data with no head selected. Table 1-3 shows the combination of address lines that selects each head.

READ/WRITE FUNCTIONS

GENERAL

When the drive is on cylinder and has a head selected, it is ready to perform a read or write operation. The controller initiates a read or write operation by sending a Control Select (Tag 3) along with the proper bus bit (Bit 0 for Write Gate and Bit 1 for Read Gate). During a write operation, the drive receives data from the controller and writes it on the disk. During a read operation, the drive recovers data from the disk and transfers it to the controller.

Figure 1-50 is a block diagram of the read/write circuits. The remainder of the discussion describes the read/write circuits and is divided into the following areas:

- Basic Read/Write Principles -- Explains the principles of recording and recovering data from a magnetic disk.
- Write Circuits -- Describes the circuits used by the drive to record data on the disk.
- Read Circuits -- Describes the circuits used by the drive to recover data from the disk.

BASIC READ/WRITE PRINCIPLES

Principles of 2-7 Recording

The drive employs two modulation schemes for read/write data transfers. The controller transfers data on the interface with Non Return to Zero (NRZ) modulation in a write operation. Write circuitry in the drive encodes the incoming data by changing it to 2-7 modulation. Transfers between the read/write circuitry and the disk use 2-7 modulation. Therefore, in a read operation, read circuitry in the drive must decode the 2-7 read data to create NRZ data which is suitable for the controller. The following paragraphs define both modulation schemes and the explain why 2-7 modulation is used in the drive.

NRZ data is transferred at a nominal rate of 9.67 MHz. Each data bit is defined throughout an interval called a bit cell, and the nominal duration of each bit cell is 103 ns. For consecutive cells indicating binary 1, the read or write interface line is driven at the active level. For consecutive cells indicating binary 0, the read or write interface line is driven at the inactive level. Thus, NRZ data lines return to zero only when the transferred data changes from binary 1 to binary 0.

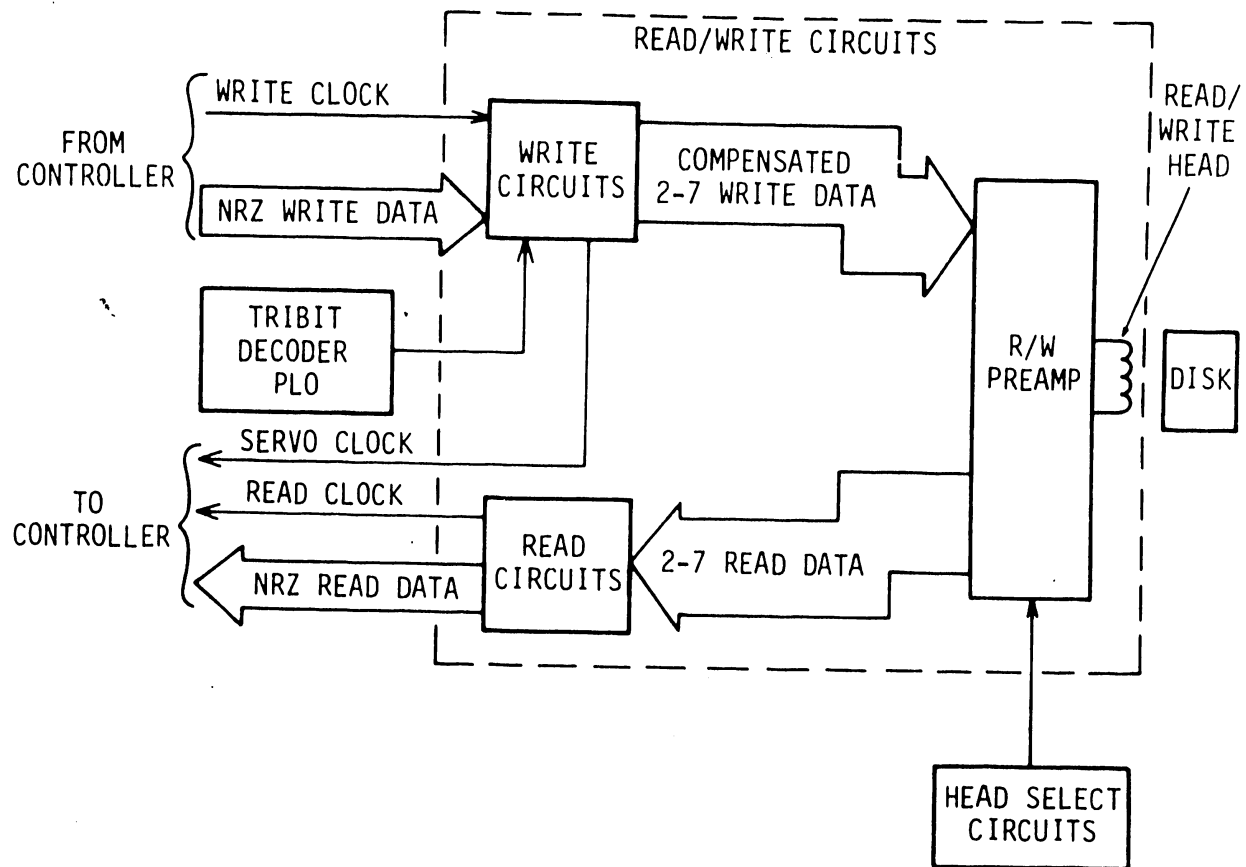
TABLE 1-3. HEAD SELECT ADDRESSING

Head Selected	+Head/Cylinder Address Lines*		
	0	1	2
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
Illegal Addresses	1	0	1
	0	1	1
	1	1	1

*+Head/Cylinder Address line 3 is not used for head selection in this drive.

For disk transfers, the 2-7 scheme is superior to the NRZ scheme in two ways. First, it reduces the average rate of flux reversals on the disk; this permits greater recording density on the disk. Second, the recording bandwidth, or range from the minimum to maximum flux reversal rate, is limited; with narrowed bandwidth, the read/write circuitry has fewer noise problems.

The translation between NRZ modulation and 2-7 modulation is a translation of seven basic code words, as shown in table 1-4. Any string of NRZ data can be expressed as a series of these individual code words. The corresponding 2-7 data string is a series of translated code words where each 2-7 code word has replaced its corresponding NRZ word. So, the write circuitry encodes the NRZ data as 2-7 data, and the read circuitry decodes the 2-7 data as NRZ data.



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Figure 1-50. Read/Write Circuits

Each 2-7 code word has twice as many bits as its related NRZ code word. Therefore, the 2-7 bit cell is half the NRZ bit cell or 51.5 ns, nominal. As the 2-7 data is written on the disk, the head changes its flux each time the code contains a binary 1. Although 2-7 uses twice the bit rate of NRZ, binary ones appear in 2-7 code less frequently than level changes occur in the corresponding NRZ code. Therefore, use of 2-7 code allows data to be written more densely on the disk.

The name 2-7 derives from the fact that preceding and following each occurrence of binary 1 in the code, there are at least two zeros and as many as seven zeros.

TABLE 1-4. TRANSLATION BETWEEN NRZ AND 2-7 CODES

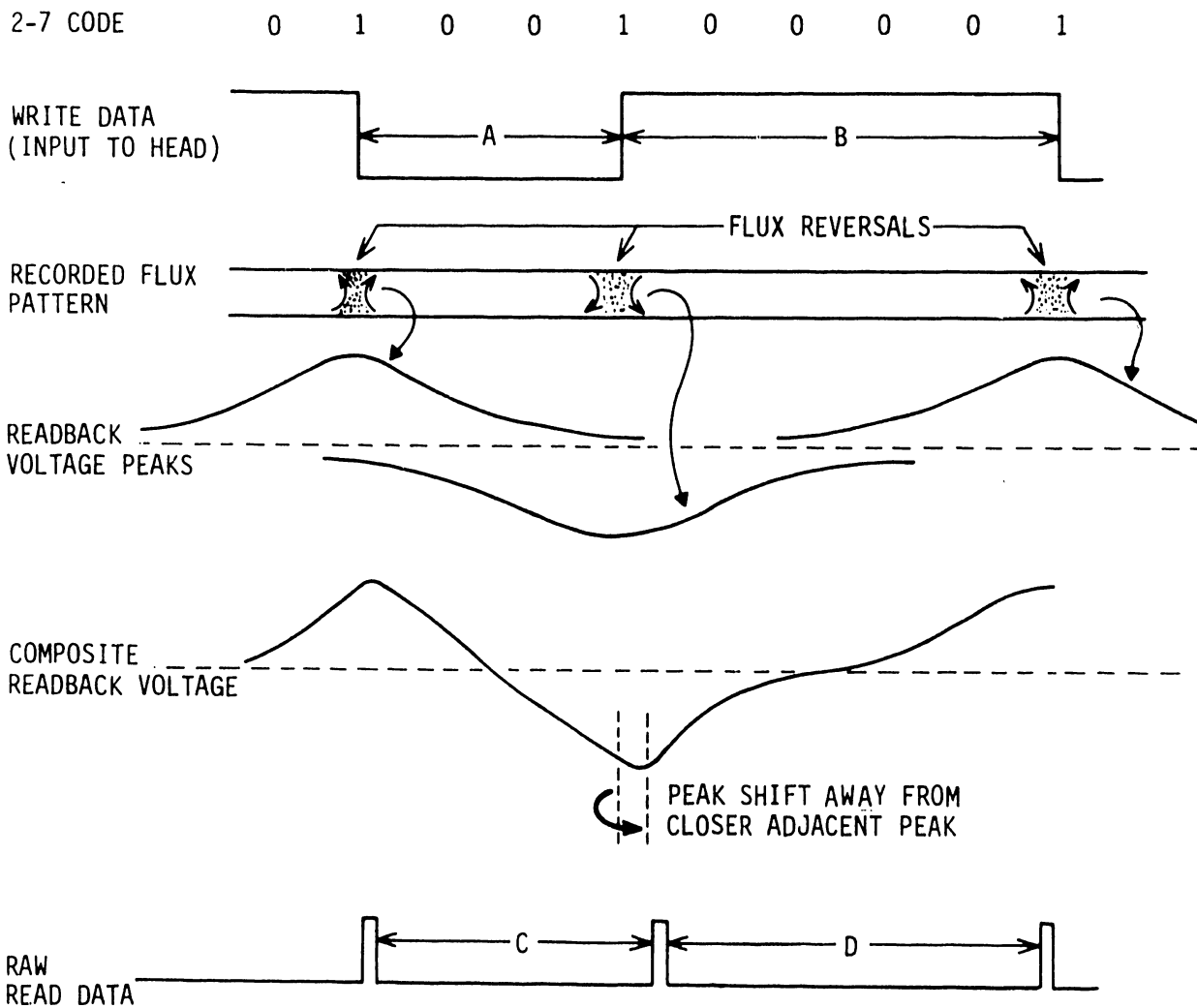
NRZ Code Words	2-7 Code Words
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

Peak Shift

Peak shift is a predictable effect that would complicate decoding of the 2-7 read signal if it were not compensated in the write circuitry. The following paragraphs explain why peak shift occurs and how write compensation reduces the effect of peak shift.

Figure 1-51 shows selected write and read signals that are relevant to the description of peak shift. The write data line toggles each time a binary 1 appears in the 2-7 data string. Each toggle of write data reverses the magnetic flux in the data head to produce a region of changing recorded flux in the disk surface. The flux reversal on the disk has a finite length on the disk because of the shape of the flux pattern from the head gap and the inability of the head to reverse its magnetic flux instantaneously.

In read operations, the data head develops a composite readback voltage as it intercepts changing flux from the disk surface. Each flux reversal creates a readback voltage peak, as shown in figure 1-51. The composite readback voltage, developed by the head passing over a flux reversal, is a superposition of the peak caused by that flux reversal and by the leading and trailing edges of the peaks caused by the adjacent flux reversals. Any difference in the contributions of the two adjacent peaks will shift the central peak away from the closer adjacent peak.



WITHOUT WRITE COMPENSATION, $C > A$ AND $D < B$,
AND INACCURATE READ DECODING WOULD BE POSSIBLE

10R72 A

Figure 1-51. Peak Shift Waveforms

Accurate decoding in read operations requires that the raw read data signal has timing intervals identical to those in the write data signal. Peak shift lengthens certain intervals and shortens other intervals in a manner that is predictable from the spacing of adjacent peaks. Write compensation anticipates this problem by advancing or delaying each write transition by an amount that depends on the number of binary 0s leading and trailing the binary 1 producing that transition. When the number leading exceeds the number trailing, write compensation delays the write transition. When the number trailing exceeds the number leading, write compensation advances the write transition. When the two numbers are equal, the transition occurs without compensation. Thus, compensated write data drives the heads, and the raw read data contains the same timing as the uncompensated write data.

The discussion of Write Compensation under Write Circuits includes a table that defines the compensation shift for each possible data pattern.

WRITE CIRCUITS

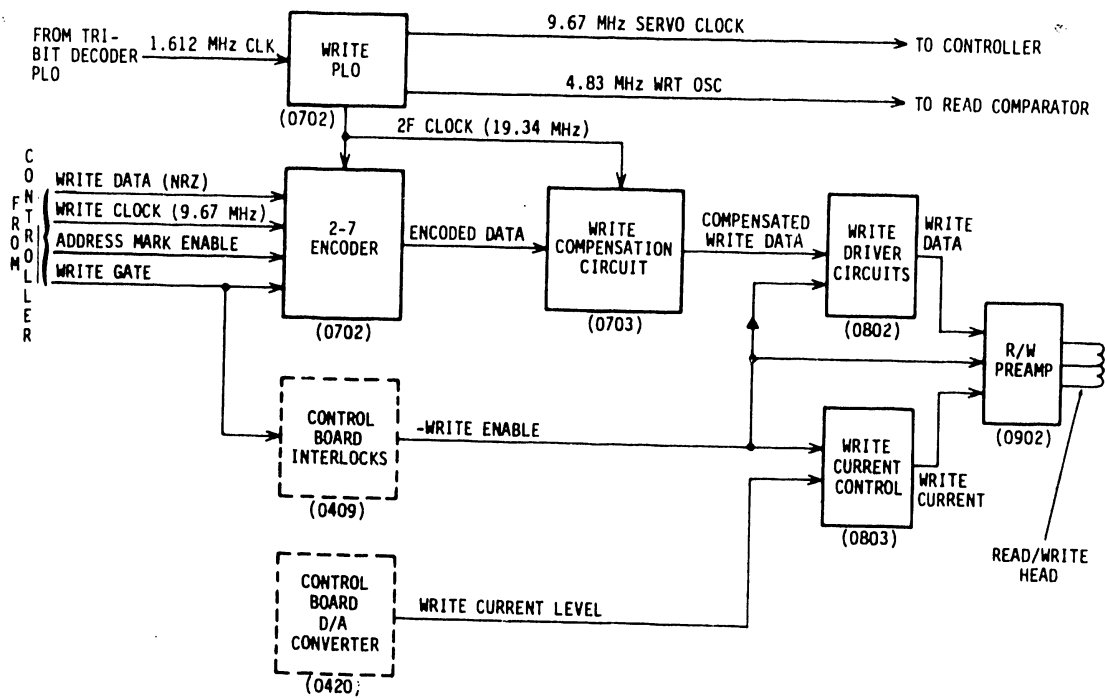
General

The write circuit operation is initiated by Tag 3 (Control Select) with Bus Bit 0 true. This allows the drive to start processing serial NRZ data received from the controller. NRZ data is synchronized to the 9.67 MHz Servo Clock derived from the Write PLO. The Write Data is received via the Write Data line and is first sent to the 2-7 encoder circuit. This circuit converts the data to 2-7 modulation and sends it to the write compensation circuit. Write compensation modifies the data timing to compensate it for peak shift (refer to discussion on basic read/write principles for more information concerning peak shift). The compensated data is then processed by the write driver circuit. The write driver circuit provides the data signal that controls current switching in the R/W pre-amp, and the current being switched is supplied by the write current control.

Figure 1-52 shows the write circuits and table 1-5 briefly explains their function.

Write PLO

The Write PLO circuitry uses a phase-locked loop to generate the 19.34 MHz (2F) Write Clock. As shown in figure 1-53, this circuitry consists of frequency dividers, a coincidence comparator, a charge pump, and a voltage-controlled oscillator (VCO). The frequency dividers and coincidence comparator are located in the Write Compensation and PLO ECL Logic Array.



10R73

Figure 1-52. Write Circuits Block Diagram

The phase-locked loop uses the 1.612 MHz Clock from the Tribit Decoder PLO as a frequency reference (refer to the Servo Surface Decoding discussion). The Write VCO operates under loop control to generate the 19.34 MHz (2F) Write Clock, at twelve times the frequency of the reference clock. Two divisions by two and one division by three of the VCO output develop a 1.612 MHz feedback signal that can be compared to the reference clock to adjust the loop operation.

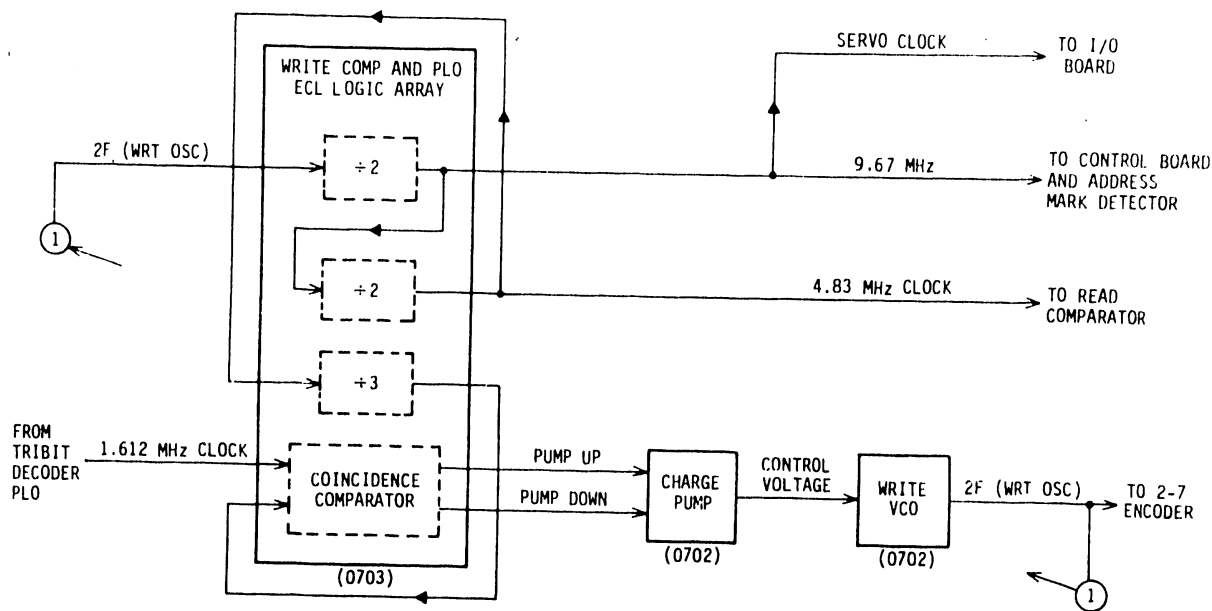
The loop reaches phase lock by comparing the coincidence of the leading edges of the reference and feedback clocks. Each time the feedback clock leads the reference clock, the coincidence comparator pulses the Pump Down line. Pump Down pulses cause the charge pump to vary the Control Voltage signal as necessary to reduce the Write VCO frequency until the reference and feedback clocks are coincident (phase-locked). Each time the feedback clock lags the reference clock, the coincidence comparator pulses the Pump Up line. Pump Up pulses cause the charge pump to vary the Control Voltage signal as necessary to increase the Write VCO frequency until phase lock occurs.

TABLE 1-5. WRITE CIRCUIT FUNCTIONS

Circuit	Function
Write PLO	Generates the 19.34 MHz Write Clock which is divided by two to develop the 9.67 MHz Servo Clock.
2-7 Encoder	Converts the NRZ data from the controller to 2-7 data.
Write Compensation Circuit	Compensates the data for problems caused by peak shift.
Write Driver Circuits	Produces a write signal that changes polarity each time the compensated 2-7 data goes to a binary 1.
Write Current Control	Produces a write current amplitude that is suited to the diameter of the track being recorded. Recording requires less current as the diameter is reduced.
R/W Preamp	Switches the write current between two opposing head coils as the signal from the write driver circuits changes polarity.

The Write PLO circuit operates continuously whenever the servo signal is being decoded. The PLO provides the following outputs to other circuits:

- 2F (WRT OSC) signal to the 2-7 Encoder circuit.
- 9.67 MHz Servo Clock to the controller (via the interface). This is returned to the drive as Write Clock.
- 9.67 MHz clock to several timing circuits on the Control Board.
- 4.83 MHz clock to the Read Comparator circuit.



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Figure 1-53. Write PLO Block Diagram

2-7 Encoder

The 2-7 Encoder converts NRZ data into 2-7 data. As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven NRZ code words and seven 2-7 code words. The encoder recognizes the coding in the write data string as a succession of the seven NRZ words, and outputs a series of 2-7 code words, each one translated from its NRZ equivalent. Table 1-4, presented under Basic Read/Write Principles, shows the translation used between the two groups of seven code words. The 2-7 encoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

The encoder uses synchronous timing circuitry controlled by two clock inputs, the 9.67 MHz Write Clock from the controller and the 19.34 MHz 2F Clock from the Write PLO (see figure 1-54). The encoder has a synchronizer that develops a 9.67 MHz internal clock in phase with the 2F Clock. This internal clock shifts NRZ data into a pattern recognition circuit. Each time this circuit recognizes one of the seven NRZ code words, it parallel-loads an output shift register and starts looking for the following word.

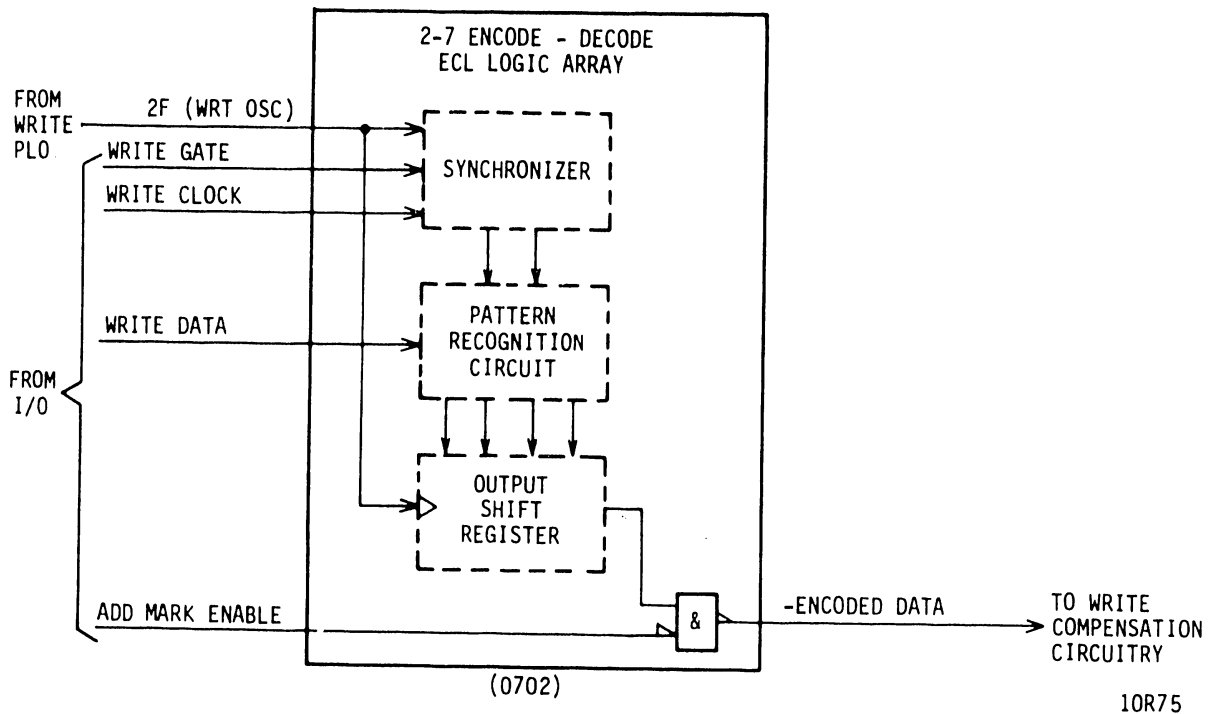


Figure 1-54. 2-7 Encoder Block Diagram

The output shift register shifts its contents on each rising edge of the 2F Clock. The active low serial output of the register is -Encoded Data. This line is active for binary ones and inactive for binary zeros in the 2-7 data unless an address mark is being written. During an address mark, there are no transitions in the written flux, and a segment of the data track is erased. To command an address mark, the controller issues Tag 3 along with Bus bit 0 (Write Gate) and Bus bit 5 (Address Mark Enable). When Bus bit 5 goes inactive, the encoder resumes normal operation.

The encoder begins translating NRZ code words with the first binary zero in the NRZ data occurring on or after the second rising edge of Write Clock. Encoder operation proceeds continuously, processing all NRZ data input to it until Write Gate goes inactive.

Write Compensation Circuit

The write compensation circuit modifies the timing of transitions in the encoded 2-7 data in a manner that compensates for peak shift (refer to discussion on basic read/write principles).

Encoded 2-7 data contains isolated bit cells at binary one preceded and followed by from two to seven bit cells at binary zero. Each time the data changes from binary zero to binary one, the head reverses its flux direction. Write compensation shifts this positive-going edge away from its nominal timing, and this timing change is related to the number of zeros preceding and trailing a binary one in the data pattern.

The write compensation function takes place in the Write Compensation and PLO ECL Logic Array (see figure 1-55). This chip is capable of following four different compensation schemes as dictated by its "A" and "B" inputs. In this drive, input "A" is pulled low and input "B" is tied high. This selection, and the delays with which the 2F Clock enters chip inputs P1 through P9, produce specified time shifts for each possible data pattern. Table 1-6 specifies the delay for each data pattern relative to the nominal delay present in the circuitry. In the table, negative delays represent earlier timing and positive delays represent later timing.

Uncompensated data enters the circuit via the -Encoded Data line. This data is clocked into a 13-bit shift register. The delay line develops the clock input by delaying the 2F clock. When the center bit of the shift register contains a binary one, the circuit looks at the number of register bits which are zero on each side of the center bit. Depending on the number of leading zeros and trailing zeros, one of the delayed clocks P1 through P9 is applied to an AND gate along with the center bit of the register. Thus, the AND gate sees the center register bit go active, followed by the applied clock going active; with both inputs active, the gate outputs a compensated write data pulse. The positive edge of the compensated data pulse is timed by the clock selected.

Table 1-6 specifies the clock input gated out of the write compensation circuit for each possible data pattern. Note that a majority of the data patterns use the P5 clock and have the nominal delay.

After being write compensated, the data is transmitted to the write driver circuit.

TABLE 1-6. WRITE COMPENSATION FOR EACH DATA PATTERN

		Number of Trailing Zeros					
		2	3	4	5	6	7
Number of Leading Zeros	2	0 ns* P5**	-2 ns P4	-4 ns P3	-6 ns P2	-6 ns P1	-6 ns P1
	3	+4 ns P6	0 ns P5	0 ns P5	-2 ns P4	-2 ns P4	-2 ns P4
	4	+8 ns P7	0 ns P5	0 ns P5	0 ns P5	0 ns P5	0 ns P5
	5	+10 ns P8	+4 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5
	6	+10 ns P9	+4 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5
	7	+10 ns P9	+4 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5
<p>*Top entry gives delay relative to nominal timing where negative numbers show early timing and positive numbers show late timing.</p> <p>**Bottom entry indicates which delayed clock enables a compensated output pulse.</p>							

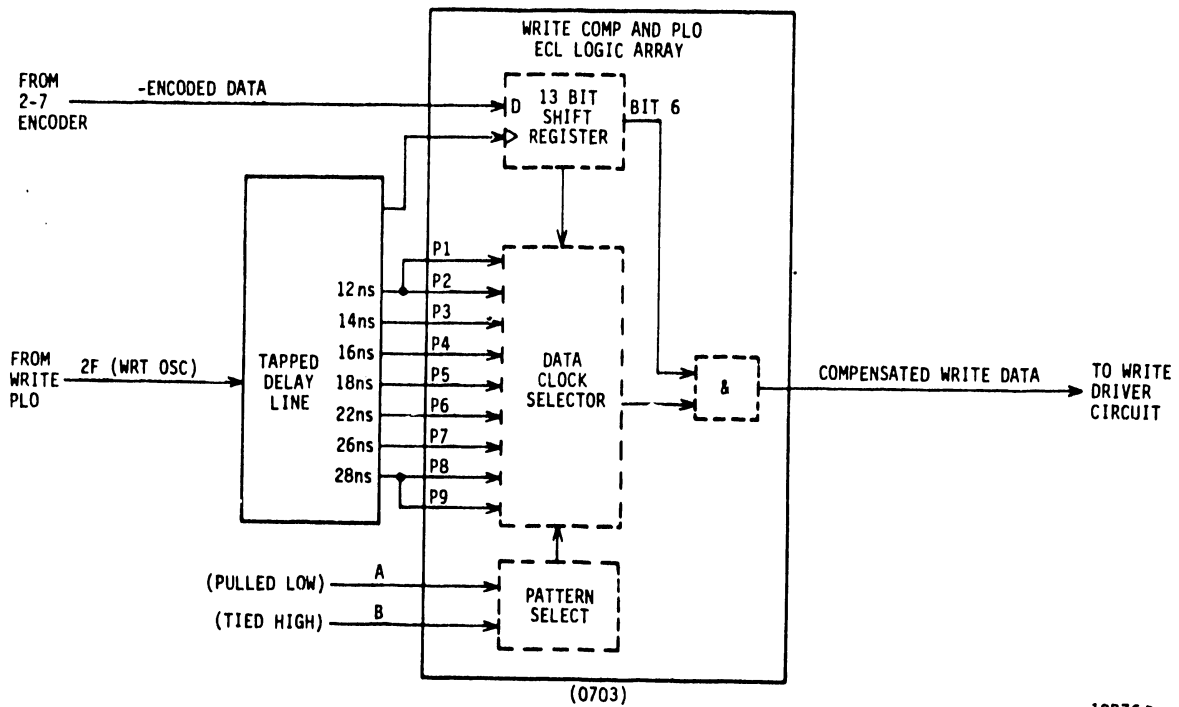


Figure 1-55. Write Compensation Block Diagram

Write Driver Circuit

The compensated write data is sent to the Data Latch board and is applied as the clock input to a latch. This latch changes state with each positive edge at its clock input. Complementary outputs of the latch drive a push-pull transistor amplifier. Each time the latch changes state, it switches on the transistor that was cut off and switches off the transistor that was conducting. Each transistor drives one of the R/W Data lines going to the R/W Preamp. During a write operation, these lines alternate going low at each rising edge of compensated write data.

The write driver circuit operates only when the -Write Enable line is active (low). With -Write Enable inactive, the latch remains cleared, and both push-pull transistors are cut off to prevent the R/W Preamp from enabling write current to the data head. The -Write Enable line comes from the Control board and is active only when all the following are true:

- Write Gate is active
- Write Protect is not active

- No faults exist
- Speed OK is active
- Retract Relay latch is cleared

Write Current Control

The write current control, located on the Data Latch board, is a dc current supply that provides a source of write current for the data head. Figure 1-56 is a simplified block diagram of the write current control and R/W preamp. The current supply is switched on when -Write Enable is active (low) and is biased by a control voltage on the Write Current Level line coming from the Control board. As the cylinder address increases (with the data head closer to the spindle), less write current is needed. Write Current Level, a function of track diameter, adjusts the Write Current amplitude to meet this requirement.

At the end of a seek, the MPU inputs the eight higher-order cylinder address bits to the D/A Converter in the Desired Velocity Generator via D/A bits 0 - 7. At this time, the servo is in the Track Following mode, and the Desired Velocity Generator is removed from the servo loop. The D/A Converter develops an analog voltage on the Write Current Level line. Being unaffected by the two lower-order cylinder address bits, the Write Current Level line is reduced slightly each time the cylinder address is increased by four tracks.

R/W Preamp

The R/W Preamp contains an LSI chip that selects a data head and either switches write current through the head or amplifies the read signal detected by the head (see figure 1-56). These paragraphs concentrate on the preamp's write function and assume that head selection has occurred.

The LSI chip functions as a write driver when the -Write Enable line goes active (low). The chip develops a regulated voltage source and connects that source to the centertap for its associated heads. Each data head has two opposing coils wound on the same core, and a flux reversal occurs when write current is switched off in one coil and on in the other coil.

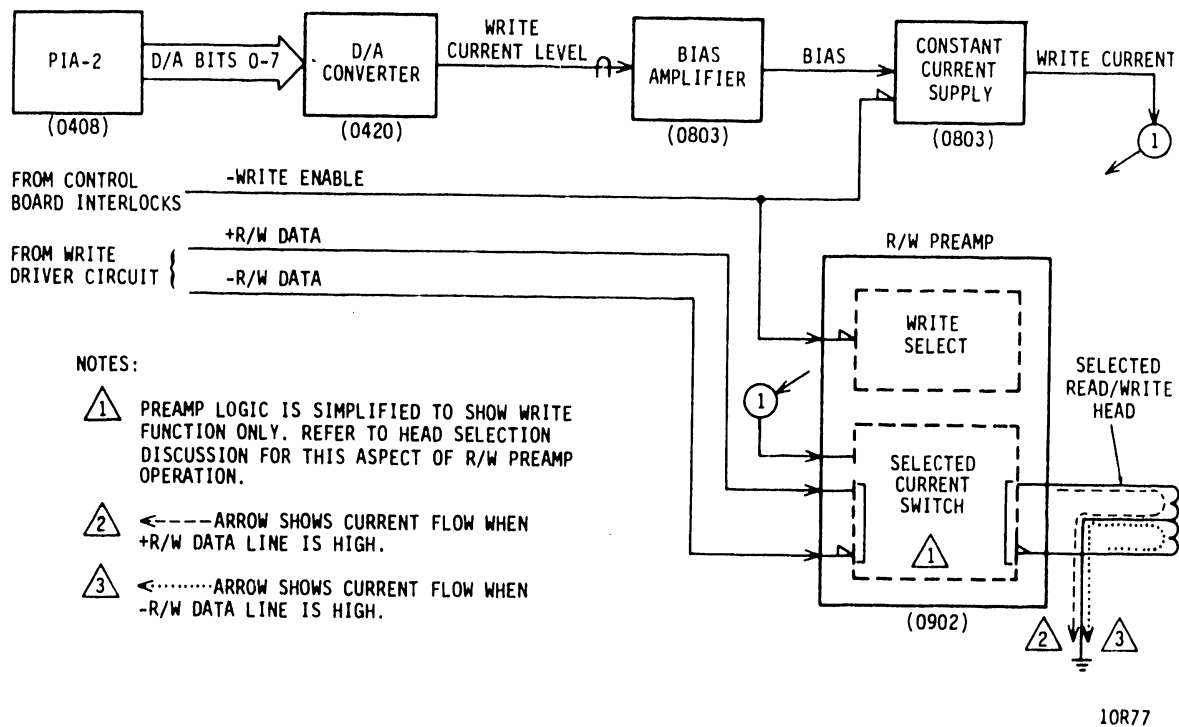


Figure 1-56. Write Current Control and R/W Preamp

Throughout a write operation, Write Current from the Write Current Control is always flowing through one of the head coils. The Write Driver circuit inputs two R/W Data lines to the R/W Preamp. When each of these lines goes low, the LSI chip switches the Write Current through the head coil associated with that line. This switching action produces a recorded flux reversal on the disk surface.

While an address mark is being written, there is no switching action, and an unchanging flux is recorded on the disk. Thus, writing an address mark erases a segment of the data track.

READ CIRCUITS

General

Read operations are initiated by a Control Select (Tag 3) with Bus bit 1 true. This enables the preamp circuits, which sense the data written on the disk and generate analog read data signals.

The analog data goes to the Data Latch circuit which changes it into digital 2-7 data.

The Read Comparator and PLO circuit generates a 19.34 MHz Read Clock signal that is phase-locked to the 2-7 read data. The 2-7 Decoder changes the 2-7 data to NRZ data synchronized to a 9.67 MHz Read Clock. Both data and clock are then sent to the controller.

Figure 1-57 shows the main elements in the read circuits and table 1-7 briefly describes each of these elements. The following paragraphs further describe the read circuits.

R/W Preamp

The R/W Preamp contain an LSI chip that selects a data head and either switches write current through the head or amplifies the read signal detected by the head. These paragraphs concentrate on the preamp's read function and assume that head selection has occurred.

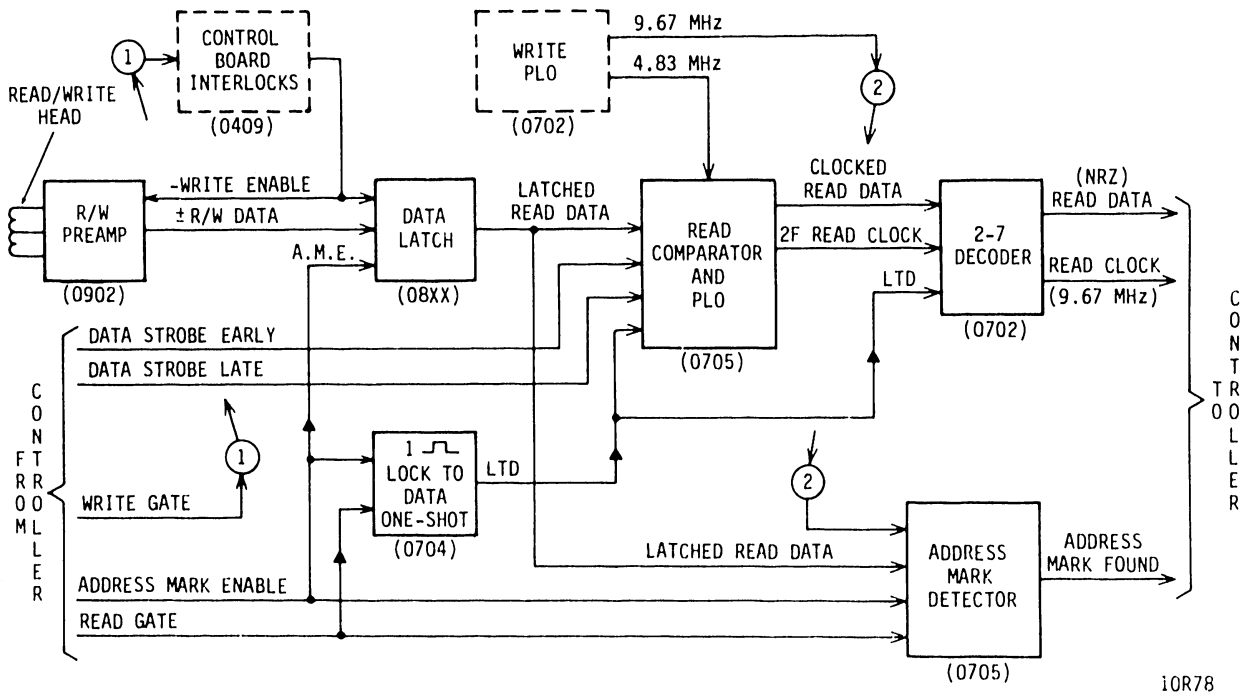


Figure 1-57. Read Circuits Block Diagram

TABLE 1-7. READ CIRCUIT FUNCTIONS

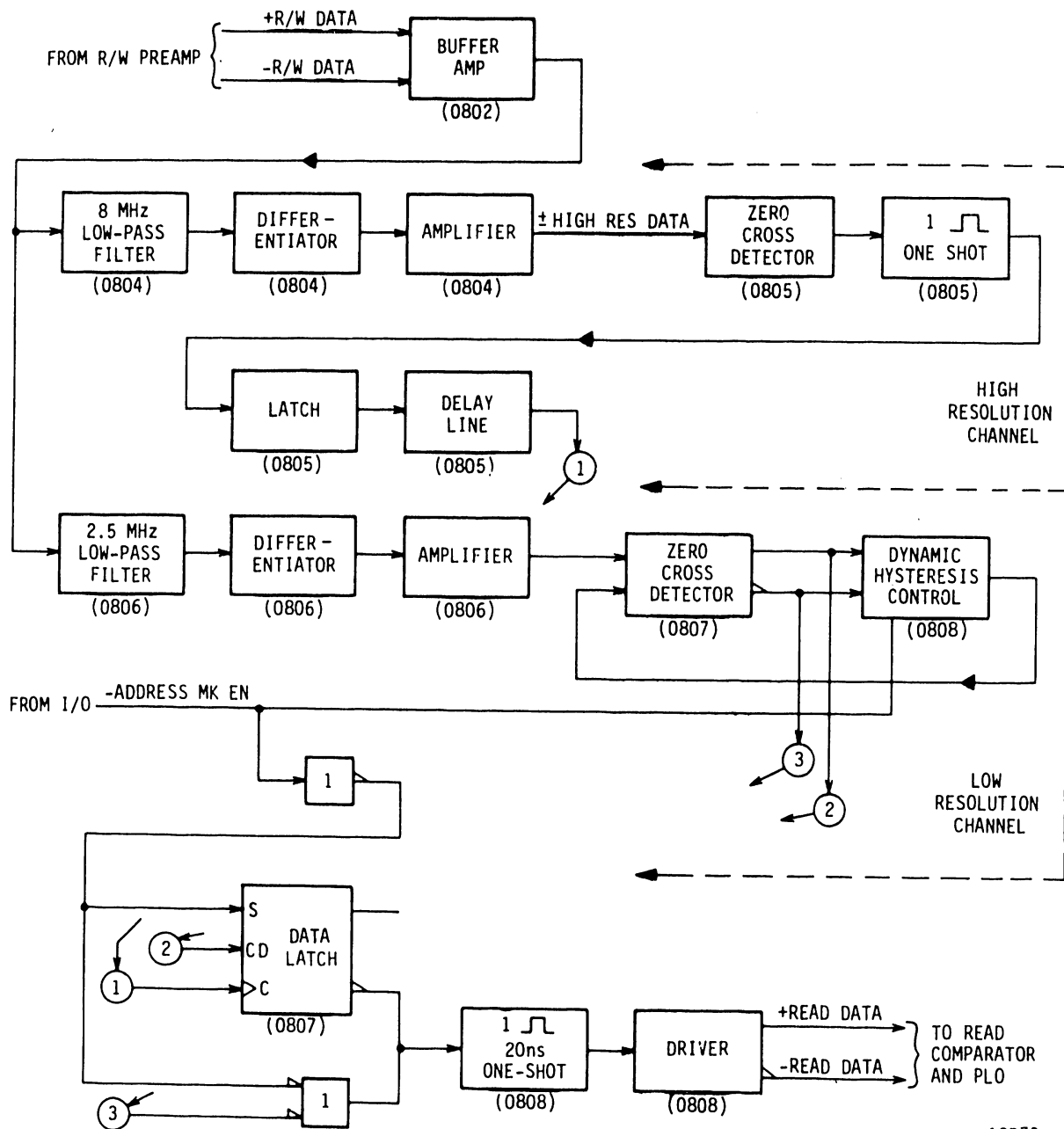
Circuit	Function
R/W Preamp	Processes the analog signal from the data head so that it can be used by the Data Latch circuit.
Data Latch Circuit	Changes the analog 2-7 data into digital 2-7 data. This data is sent to the Read Compensation circuit.
Read Comparator and PLO Circuit	Develops a 19.34 MHz Read Clock that is synchronized to 2-7 read data.
2-7 Decoder	Translates data coding from 2-7 to NRZ modulation and generates 9.67 MHz Read Clock synchronized to NRZ data. NRZ data is sent to the controller with the 9.67 MHz Read Clock.
Address Mark Detector	Detects the address mark and transmits an Address Mark Found to the controller.

The LSI chip functions as a read preamp when the -Write Enable line is inactive (high). The chip contains a separate differential amplifier for each head, and head selection enables the differential amplifier associated with the desired head. In read operations, both coils in the selected head develop a readback pulse when the head passes over a written flux reversal on the disk. The head coil centertap is not used, and the other two coil leads provide a differential input to the preamp.

The differential amplifier selected in the chip amplifies the read signal and sends it on the R/W Data lines to read circuitry on the Data Latch board.

Data Latch Circuit

The Data Latch circuit (refer to figure 1-58) receives analog read data from the R/W Preamp and converts it into digital data.



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Figure 1-58. Data Latch Block Diagram

The input signal is amplified by the Buffer Amp provided that $\overline{\text{Write Enable}}$ is inactive (high). The $\overline{\text{+Read Analog Data}}$ output from the Buffer Amp splits into two parallel signal paths, the high resolution channel and the low resolution channel. Each channel contains independent wave-shaping circuitry that prepares an input to the Data Latch FF. The high resolution channel supplies delayed clock pulses to the Data Latch FF, and the low resolution channel supplies a D-input to the Data Latch FF. Successive clock pulses toggle the FF when the D-input has changed. Each transition of the Data Latch FF triggers a 20 ns one-shot that pulses the $\overline{\text{+Read Data}}$ output lines once for each written flux transition sensed by the data head.

Splitting the analog data signal into two paths and combining the high and low resolution channels in the Data Latch FF is a system that discriminates against high frequency noise components in the Read Analog Data but maintains the timing of the data transitions. The low resolution channel uses a low-pass filter (rolling off at 2.5 MHz) followed by a zero-cross detector to develop a digital waveform similar to the Write Data waveform used in recording. However, filtering out the high frequency components of the input signal lowers the timing resolution of the channel's output signal. The high resolution channel uses a low-pass filter (rolling off at 8 MHz) followed by a zero-cross detector and a delayed pulse-forming circuit. With its wider bandwidth, this channel closely follows the timing present at its input. Each change in the low resolution signal is clocked into the Data Latch FF by a delayed clock pulse from the high resolution channel. Erroneous clock pulses from the high resolution channel do not toggle the Data Latch FF because they do not follow a change in the FF's D-input.

The Data Latch circuitry switches into a different operating mode during an address mark search. In an address mark search, the pulses on the $\overline{\text{+Read Data}}$ output lines cease when the head is passing over an address mark, which is a previously erased segment of the track. An address mark search is initiated when $\overline{\text{-Address Mark Enable}}$ goes active (low), which happens when the controller issues Control Select (Tag 3) with Bus bits 1 and 5 active. This holds the Data Latch FF set and uses the output of the low resolution channel to trigger the 20 ns one-shot that pulses the $\overline{\text{+Read Data}}$ output lines. The low resolution signal is sufficient for an address mark search because the read signal is not being demodulated. To regulate operation of the zero-cross detector in the low resolution channel and to prevent unwanted output pulses during an address mark, the dynamic hysteresis control circuit adjusts the switching thresholds of the zero-cross detector. In this way, noise pulses arising during the address mark are prevented from producing transitions in the low resolution signal.

The $\overline{\text{+Read}}$ Data goes from the Data Latch circuitry to the Read/Write PLO board where it is decoded to NRZ data and the synchronized Read Clock is generated.

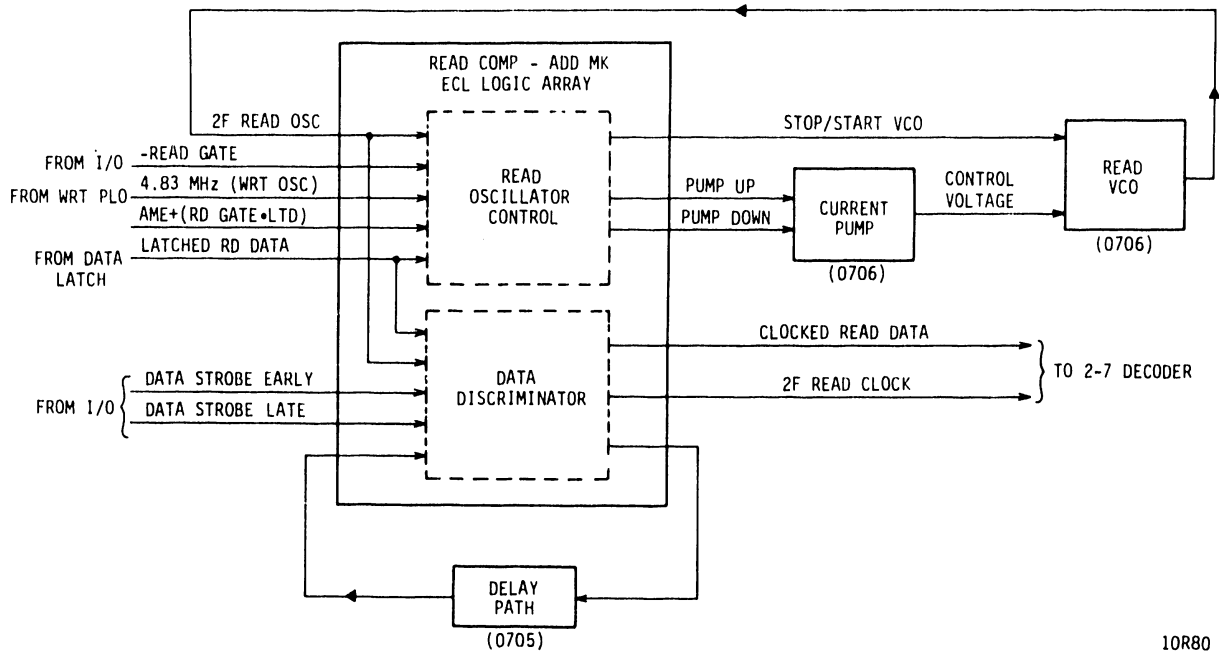
Read Comparator and PLO

The Read Comparator and PLO circuitry uses a phase-locked loop to generate the 19.34 MHz Read Clock, and processes latched read data from the Data Latch board to develop clocked read data. Data Strobe commands from the controller condition the timing of clocked read data relative to the read clock to provide a means of error recovery to the read circuitry.

Figure 1-59 is a simplified block diagram of the Read Comparator and PLO circuitry. The phase-locked loop uses the Read Oscillator Control portion of the Read Comparator - Address Mark ECL Logic Array to regulate operation of the Current Pump and to provide stop/start control of the Voltage-Controlled Oscillator (VCO). The Current Pump supplies a Control Voltage signal to the VCO that determines the frequency of the 2F RD OSC signal output from the VCO. The 2F RD OSC signal is fed back to the Read Oscillator Control to complete the loop.

The phase-locked loop locks the VCO frequency to one of two reference signals. When the drive is reading data ($\overline{\text{-Read Gate}}$ and AME low), the phase-locked loop uses the pulse train on the Latched Read Data line as a timing reference. In this case, the Read Oscillator Control uses a quadrature comparator to drive the Pump Up and Pump Down lines as necessary to keep the rising edges of the 2F RD OSC signal coincident with the rising edges of $\overline{\text{+Latched RD Data}}$ pulses. For each Latched RD Data pulse, the quadrature comparator outputs a variable-length pulse on the Pump Up line, followed by a fixed-length pulse on the Pump Down line. When the Pump Up and Pump Down pulses differ in length, the Control Voltage to the VCO varies accordingly to phase shift the VCO and bring it into phase lock.

When the drive is not reading data ($\overline{\text{-Read Gate}}$ high or AME high), the phase-locked loop maintains the VCO frequency close to the value it has during read operations. In this mode, a coincidence comparator in the ECL Logic Array monitors the phase difference between the 4.83 MHz WRT OSC signal (derived from the Write PLO) and the 2F RD OSC signal fed back from the VCO. When the rising edge of the 4.83 MHz signal leads the rising edge of the 2F signal, this comparator pulses the Pump Up line to increase the Read VCO frequency. Conversely, when the rising edge of the 4.83 MHz signal lags the rising edge of the 2F signal, this comparator pulses the Pump Down line to decrease the Read VCO frequency.



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Figure 1-59. Read Comparator and PLO Block Diagram

The Read Oscillator Control circuitry uses the Stop/Start VCO line to control VCO operation while switching between the quadrature and coincidence comparators. The Stop/Start VCO line goes active for approximately 200 ns after the Latched RD Data pulse following a change in the Read Gate signal. While the Stop/Start VCO line is active, the VCO is inhibited, and its control voltage is held constant. This enables the Read PLO to phase lock within 2 microseconds during the switching transitions.

The Data Discriminator portion of the Read Comparator - Address Mark ECL Logic Array conditions the 2F Read Clock and Clocked Read Data signals for use in the 2-7 Decoder (see figure 1-59). With nominal timing, pulses on the Clocked Read Data line are active for one 2F bit cell (51 ns), and positive transitions of the 2F Read Clock coincide with the center of Clocked Read Data pulses. For error recovery, the controller can issue a Data Strobe Early or a Data Strobe Late command to shift this timing either way from its nominal value. The controller commands Data Strobe Early by issuing Tag 3 (Control

Select) with Bus bit 7 active. The Data Discriminator responds by routing the clock signal through a 2.9 ns delay path. This process delays the 2F Read Clock relative to the Clocked Read Data pulses. The controller commands Data Strobe Late by issuing Tag 3 with Bus bit 8 active. The Data Discriminator responds by routing the data signal through a 2.9 ns delay path. This process delays the Clocked Read Data pulses relative to the 2F Read Clock.

The Clocked Read Data and 2F Read Clock signal are input to the 2-7 Decoder, which converts the read data from 2-7 code into NRZ form and generates the 9.67 MHz Read Clock.

2-7 Decoder

The 2-7 Decoder converts 2-7 data into NRZ data and generates the 9.67 MHz Read Clock from the 19.34 MHz Read Clock. Both inputs, the 2-7 data and the 19.34 MHz Read Clock, come from the Read Comparator and PLO circuitry.

As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven 2-7 code words and seven NRZ code words. The decoder recognizes the coding in the 2-7 read data input as a succession of the seven 2-7 words, and outputs a series of NRZ code words, each one translated from its 2-7 equivalent. Table 1-4, presented under Basic Read/Write Principles, shows the translation used between the two groups of seven code words. The 2-7 decoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

Figure 1-60 is a simplified block diagram of the 2-7 Decoder. The decoder synchronizes after the +Lock to Data input goes inactive (low). This occurs 2 microseconds after Read Gate goes active unless an address mark search is in progress. If an address mark search is in progress, +Lock to Data goes inactive 2 microseconds after Address Mark Enable goes inactive, provided that Read Gate stays active. Once +Lock to Data goes inactive, synchronization occurs when the 2-7 input data contains three or more binary zeros followed by a binary one. This binary one sets up the proper phase of the 9.67 MHz Read Clock relative to the NRZ Data output line and initiates the decoding process. The clock and decoding operations are discussed in the following paragraphs.

The 9.67 MHz Read Clock is generated from the 19.34 MHz Read Clock as this signal clocks a divide-by-two FF. The Q-output of the FF is inverted and supplied to the D-input through a gate that is enabled as a result of synchronization. Synchronization selects which positive edge of the 19.34 MHz Read Clock determines the positive edge of the 9.67 MHz Clock.

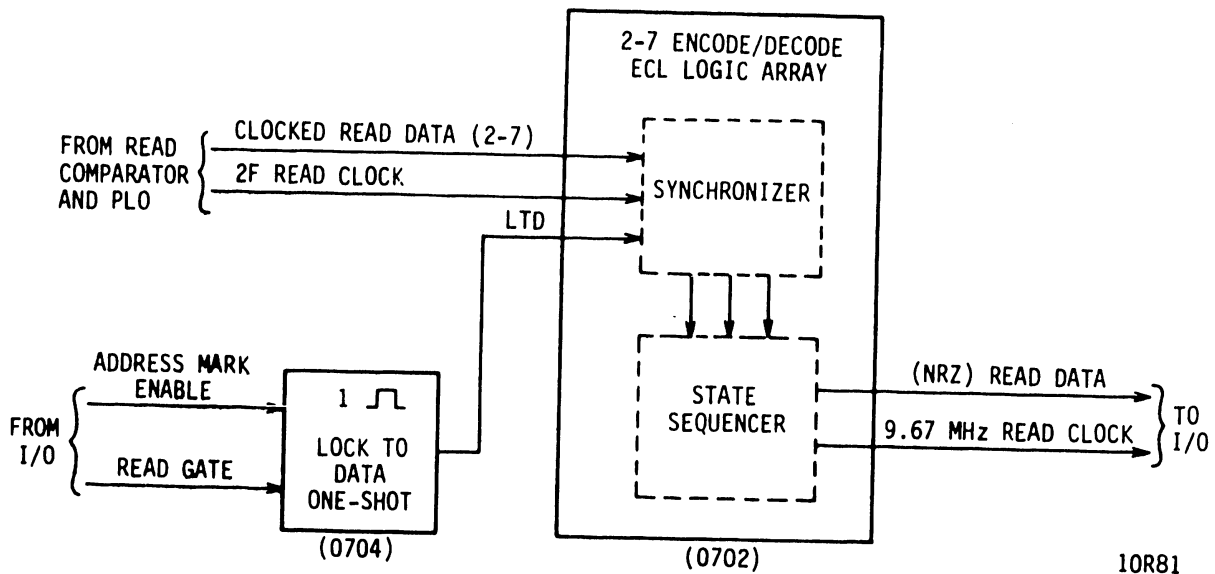


Figure 1-60. 2-7 Decoder Block Diagram

The decoding function is performed by a state sequencer. The state sequencer has eight FFs, and each of the eight states corresponds to one of the FFs being set. It operates by shifting states on each falling edge of the 9.67 MHz Read Clock. Thus, the interval for each state is one NRZ bit cell (103 ns). Two factors determine the current state of the sequencer. These are the previous state and the binary values of the last two 2-7 data bits input to the circuit. Therefore, at any time the state of the sequencer reflects the recent decoder inputs. The binary level decoded on the NRZ Data lines is state-dependent. During two of the states (NRZ bit cells), the output is binary zero, and during the other states, the output is binary one. In summary, the way the sequencer maps one state into the next state implements the specified translation from 2-7 data words into NRZ data words.

The decoder output stays low until synchronization occurs, and there is a processing delay of four 2-7 bit cells within the decoder.

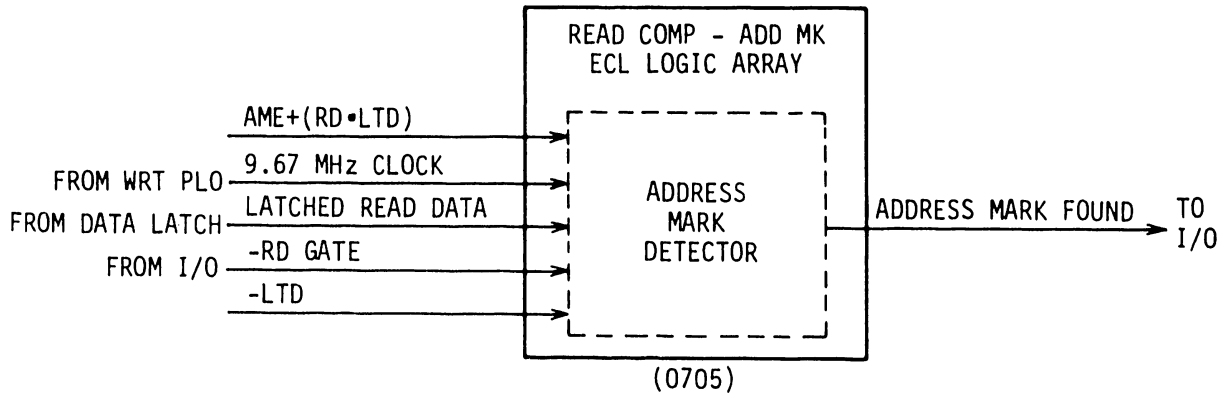
The decoder sends the +NRZ Read Data and +Read Clock outputs to the I/O board to be transmitted on the Interface to the controller.

Address Mark Detection

The Address Mark Detector, which is part of the Read Comparator - Address Mark ECL Logic Array, monitors the Latched RD Data signal from the Data Latch board during an address mark search. If a gap of 2.1 to 3.6 microseconds is detected between incoming read pulses, the detector sets the Address Mark Found line, and the I/O circuitry sets the Address Mark line on the interface.

Figure 1-61 shows the input and output signals for the Address Mark Detector. An address mark search occurs when the controller issues Tag 3 (Control Select) with Bus bits 1 and 5 active. In this situation, the -Read Gate line is low and the AME line is high. Together, these two signal inputs enable the Address Mark Detector.

The detector contains a counter circuit which is driven by the 9.67 MHz Clock signal from the Write PLO until it is reset by incoming read pulses. If the counter is clocked up over an interval from 20 to 36 clock periods, the Address Mark Found line is set. This line remains set until the lock-to-data interval ends (2 microseconds after Address Mark Enable is cleared) or until -Read Gate goes high.



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Figure 1-61. Address Mark Detector Block Diagram

The detector also contains a discriminator that distinguishes between read data gaps, caused by media defects, and gaps indicating address marks. If a defect is crossed, the discriminator inhibits the Address Mark Found output.

FAULT AND ERROR CONDITIONS

GENERAL

The following paragraphs describe those conditions which are interpreted by the drive as errors. These errors are divided into two categories: (1) those that generate the Fault signal and (2) those that do not generate the Fault signal. Included in the following descriptions are a list of conditions that produce each error status, the effect of that status on drive operation, and actions that clear the status indication to return the drive to normal operation.

ERRORS INDICATED BY FAULT SIGNAL

General

The drive has monitoring circuitry that recognizes five types of error conditions. When any of these error conditions occurs, it sets the respective latch in the I/O Gate Array. An OR circuit in the gate array receives inputs from the five latches; if one or more of the latches is set, the OR circuit activates the Fault line. The Fault line remains active until the latches are cleared.

When the Fault line goes active, it lights the FAULT indicator on the operator panel, disables write operations, and issues Fault and Write Protected status to the controller. The active Fault line interrupts the MPU at PIA-0 (see figure 1-62). The MPU responds by dropping the Ready signal and by communicating with the I/O Gate Array to identify the fault. The Unit Ready line to the controller goes inactive, and the READY indicator on the operator panel flashes until the fault is cleared.

Communication between the MPU and the I/O Gate Array takes place via I/O Control lines 1-3. Upon receiving the Fault interrupt, the MPU pulses I/O Control lines 1 and 2 to operate a multiplexer inside the gate array. The multiplexer's inputs include the five fault latches inside the gate array, and its output is carried to PIA-0 by the I/O Control 3 line. There are five individual fault LEDs on the Control board, each corresponding to a fault latch in the gate array. Having read the status of the latches, the MPU lights the corresponding LED(s) via outputs of PIA-2.

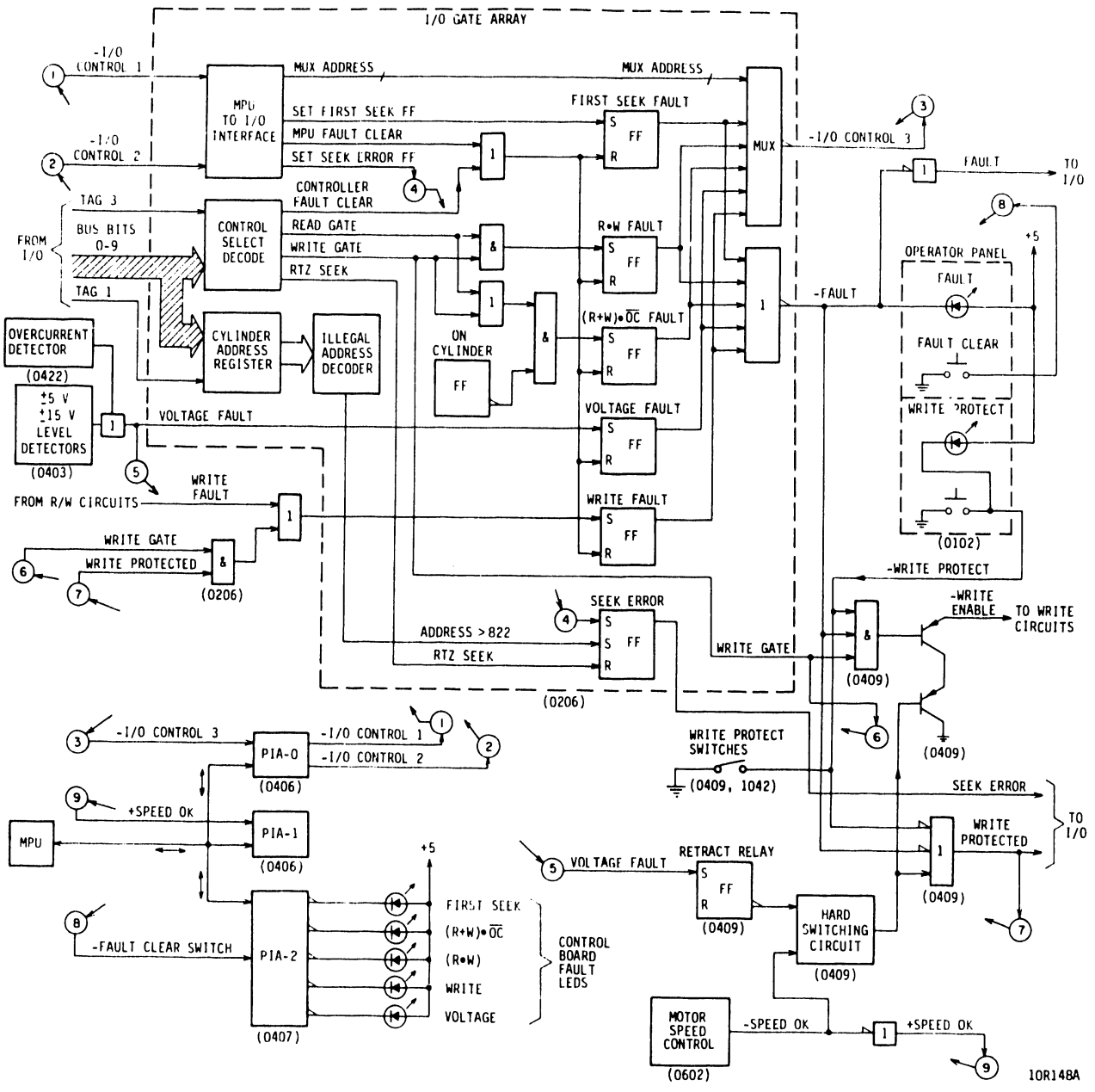


Figure 1-62. Fault and Error Detection Circuitry

Provided the error condition or conditions no longer exist, the Fault signal is cleared by the following:

- Controller Fault Clear command (Tag 3 with Bus bit 4)
- Fault Clear switch on operator panel
- Powering down the drive

The controller Fault Clear command is decoded inside the I/O Gate Array to develop a reset input for the five latches. When the Fault Clear switch is pressed, it interrupts the MPU at PIA-2. The MPU responds by pulsing the I/O Control 1 and 2 lines with a code that develops a reset input for the five latches. In either case, the reset input will clear a latch only if it is no longer being set by the error condition. In the process of removing and reapplying power to the drive, the fault circuitry is initialized as part of the power sequence, and any pre-existing fault status is lost.

The following paragraphs describe the individual fault conditions which set each of the latches in the I/O Gate Array and thus activate the Fault signal.

Voltage or Actuator Current Fault

This fault is generated whenever either the +15 or +5 voltages are detected to be below satisfactory operating levels or the actuator current exceeds an allowable level. Threshold detectors on the Control board activate the Overcurrent line if the actuator current reaches 5.9 amperes or activate the Voltage Fault line if any of the following voltages drop:

- The +15 V supply drops to 14.35 V.
- The +5 V supply drops to 4.83 V.
- The -5 V supply drops to -4.90 V.
- The -15 V supply drops to -14.46 V.

These two lines, Overcurrent and Voltage Fault, are ORed to develop the -(Voltage + Actuator Current) Fault signal. When this signal goes low, it sets the individual fault latch in the I/O Gate Array and sets the Retract Relay latch in the interlocks circuitry on the Control board. Setting the Retract Relay latch adds an additional degree of write protection, needed to safeguard existing data on the disks by inhibiting the write circuitry while a voltage problem exists. A hard switching

circuit deactivates the -Write Enable line when the Retract Relay latch is set and keeps it inactive for about 1/2 second after the Retract Relay latch is cleared. This supplements the write protection normally invoked when the Fault line is active or when the drive is placed in the Write Protect mode.

When the Retract Relay latch is set, the resulting Pick Retract Relay signal disables the servo input to the Power Amp Drive and energizes the Pick Retract relay on the Power Amp board to enable emergency retract power to the voice coil to drive the heads out to the retract position. Emergency retracts are discussed under Seek Functions.

An additional voltage detector circuit detects when the +5 V supply drops to 4.73 V, making MPU operation unreliable. This condition generates a -Low Vcc signal to produce the Reset signal for the MPU chips and the DC Master Clear signal for the gate arrays.

Read or Write and Off Cylinder

This fault is generated if the drive is in an off cylinder condition and it receives a Read or Write gate from the controller. The I/O Gate Array decodes both gates from Tag 3 commands and contains the On Cylinder FF. When the On Cylinder FF is cleared and either gate goes active, logic in the gate array sets the associated fault latch.

Write Fault

A write fault is encoded if any of the following conditions exist:

- Write Gate received while drive is in Write Protected mode
- No Write Current input to the write driver when Write Enable is active
- No write data transitions when the Write Gate is active (except when the Address Mark Enable signal is active)
- Head open (bad head detected)
- An invalid head address received (addresses 5 through 7)

When the controller selects an illegal head, an error is not detected until the controller attempts to write with that head. Since no head has been selected, there will be no Write Current to the write driver and the Write Fault will be encoded.

All conditions except the first one, which is detected on the I/O board, activate the Unsafe line coming from the LSI chip in the R/W Preamp. Gating circuitry on the Data Latch board develops the Write Fault signal from the Unsafe signal provided that Write Enable is active and Address Mark Enable is inactive. The gating circuitry keeps the Write Fault line inactive during transitions between read and write operation; at these times, the Unsafe line may contain pulses in normal operation. The Write Fault line or the combination of Write Protect and Write Gate lines active sets the associated latch in the I/O Gate Array.

Read and Write Fault

This fault is generated whenever the drive receives a Read Gate and a Write Gate simultaneously. This condition is detected internally in the I/O Gate Array to set the associated latch.

First Seek Fault

First Seek fault, as opposed to Seek Error, results from error conditions that occur during power on initialization and the load operation. Seek Error, on the other hand, indicates error conditions that occur during normal seeks and RTZ seeks. First Seek faults generate an active Fault signal while Seek Errors activate the Seek Error and Seek End lines to the controller. Seek Errors are discussed in the next topic, and the error conditions that cause a First Seek fault are described in the following paragraphs.

Unlike the other individual fault latches, the latch for First Seek fault is set by the MPU. To set the latch, the MPU inputs the I/O Gate Array with a specific pulse code on I/O Control lines 1 and 2. The error conditions resulting in a First Seek fault are monitored by the MPU during the power on initialization and load operation. Assuming that the MPU is operational, it sets the associated latch in the I/O Gate Array if any of the following tests fail:

- When the load begins, the Heads Loaded switch indicates that the heads are unloaded. The switch toggles within the first 60 ms of the load seek.
- Demodulator OK is inactive at the start of the load and stays inactive for the first 80 ms (minimum). Demodulator OK goes active within 360 ms and remains stable throughout the rest of the load.

- After actuator turnaround in the outer guard band, four cylinder pulses are counted before Outer Guard Band Pulses cease (to indicate valid guard band decoding).
- During the first 1.4 ms of track-following, less than three cylinder pulses are detected.
- No seek error occurs during the scan cycle.

The MPU aborts the load operation when a First Seek fault is indicated. Although a controller Fault Clear command will reset the Fault signal, the MPU waits until the operator panel Fault Clear switch is pressed before attempting another load.

ERRORS NOT INDICATED BY FAULT SIGNAL

General

Two types of errors do not generate the Fault status -- seek errors and the motor speed error. The seek error has an associated status FF, while the motor speed error does not.

Motor Speed Error

The -Speed OK signal is developed by circuitry in the Motor Control Gate Array on the Motor Speed Control board. When the spindle speed falls below 3580 r/min, the -Speed OK signal goes high. The -Speed OK signal is used by several circuits on the Control board (see figure 1-62), and these uses are outlined in the following paragraphs.

An interlocks circuit monitors the -Speed OK line to provide write protection if the line goes low. Write protection is needed to safeguard existing data on the disk by inhibiting the write circuitry while a motor speed error exists. A hard switching circuit deactivates the -Write Enable line when -Speed OK goes high and keeps it inactive for about 1/2 second after -Speed OK goes low again.

When -Speed OK goes high, it activates the -Pick Retract Relay line. When the -Pick Retract Relay line goes low, it deenergizes the Retract Relay in the Power Amp board, allowing the Emergency Retract Power Amplifier to supply current to the actuator coil. The emergency retract circuitry moves the heads to the retracted position. This operation is discussed under Emergency Retract Operations (part of Seek Functions).

The MPU has two methods for restoring motor speed when -Speed OK goes high. The MPU checks the +Motor Fault line at PIA-1. If +Motor Fault is active, the MPU drops and then issues the Motor Run command in order to reset the motor fault circuitry in the Motor Control Gate Array. If +Motor Fault is inactive, the MPU keeps the Motor Run command active and tries to bring the motor back up to speed. In either case, the MPU drops the Unit Ready signal to the controller during the low speed condition.

Seek Error

Seek Error is a status signal sent to the controller indicating error conditions that occur during normal seeks and RTZ seeks. The Seek Error signal is active when the Seek Error FF, located in the I/O Gate Array, is set.

If the controller commands a cylinder select, specifying a cylinder address greater than 822, this condition is recognized by a decoder circuit connected to the Cylinder Address Register (CAR). The decoder output feeds one of the set inputs to the Seek Error FF. Detection of this condition is internal to the I/O Gate Array, which contains the CAR, the decoder, and the Seek Error FF.

During normal seeks and RTZ seeks, the MPU tests certain error conditions. If any tests fail, the MPU sets the Seek Error FF in the I/O Gate Array. These tests include the following:

- Demodulator OK is active at the start and end of normal seeks, and it is active throughout RTZ seeks.
- Fault stays inactive throughout seeks.
- The time required for a normal seek is less than the 60 ms timeout allowed by the MPU.
- During the first 1.4 ms of track-following, less than three cylinder pulses are detected (normal or RTZ seeks).
- Less than three guard band pulses are detected at PIA-1 during one seek. Inner and outer guard band pulses are counted in normal seeks. Only inner guard band pulses are counted during RTZ seeks.

- After actuator turnaround in the outer guard band (RTZ seeks), four cylinder pulses are counted before Outer Guard Band Pulses cease (to indicate valid guard band decoding).
- The MPU gets a reset input to force it out of a hang condition.

If any of these tests fails, the MPU sets the Seek Error FF using I/O Control lines 1 and 2 (see figure 1-61).

A Seek Error status signal is generated to the controller via the I/O transmitters. The Seek Error signal is also input to the Sector Counter Gate Array (on the Control board) where it encodes a Seek End status signal to be sent to the controller.

In the event of a Seek Error, the MPU drops all servo commands, allowing the heads to remain in their current position over the disks. The seek error condition cannot be cleared except by a controller RTZ command. An attempt by the controller to perform a read or write operation while the seek error condition exists will result in the generation of a Read or Write and Off Cylinder fault.

SECTION

2

GENERAL

MAINT-

ENANCE

INFOR-

MATION

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

This section contains general information relating to maintenance of the drive. A person performing maintenance should be familiar with the information in this section in addition to being thoroughly familiar with drive operation. Information is divided into the following areas:

The general maintenance information is divided into the following areas:

- Warnings and Precautions - Lists warnings and precautions that must be observed when working on the drive.
- Electrostatic Discharge Protection - Provides instructions for the proper handling of electrostatically sensitive devices.
- Testing the Drive - Provides information concerning the electrical testing of the drive.
- Accessing Assemblies for Maintenance - Identifies the various parts of the drive, and describes how to access these parts for maintenance.

WARNINGS AND PRECAUTIONS

Observe the following warnings and precautions at all times. Failure to do so may cause equipment damage and/or personal injury.

- Use care while working with the power supply because line voltages are present.
- Do not operate the drive over an extended period of time without the top cover installed.
- Always deenergize drive before removing or installing circuit boards, cables, or any other electrical component.
- Observe the precautions listed under Electrostatic Discharge Protection.
- Keep hands away from actuator during seek operations. Under certain conditions, emergency retract voltage may be present, causing sudden reverse motion and head unloading.
- Use caution while working near heads. Do not touch the head pads under any circumstances. If contact is made with the head pad, head must be replaced. Heads cannot be cleaned in the field.
- Keep all watches, disk packs, meters, and other test equipment away from magnet area.
- Do not remove or install connectors while power is on. Circuit boards are easily damaged by transient voltage spikes which may be generated by removing or installing connectors when power is on.
- Do not use customer data packs for testing purposes. See paragraph on disk packs.
- Do not use the CE alignment pack unless specifically directed to do so. These packs contain prerecorded alignment data that can be destroyed if test procedures require the drive to write. The CE alignment pack cannot be generated in the field.
- Keep all metal tools away from flex leads while power is applied in order to prevent damage to the power amplifier.
- If power to voice coil is lost and heads fail to retract, swing read/write boards up to maintenance position, remove top air (head access) cover and carefully pull carriage back to the retract position.

- If the power supply is placed on a bench for testing, position the supply so that all ventilation holes are open to allow proper air flow to internal components.
- Do not attempt to open front door when the heads are extended into the disk pack area or damage to heads will result. See paragraph on Overriding Front Door Interlock.
- Always remove the data pack when the drive is moved from one location to another. Failure to do so could cause damage to heads and data pack.

ELECTROSTATIC DISCHARGE PROTECTION

All drive electronic assemblies are sensitive to static electricity, due to the electrostatically sensitive devices used within the drive circuitry. Although some of these devices such as metal-oxide semiconductors are extremely sensitive, all semiconductors as well as some resistors and capacitors may be damaged or degraded by exposure to static electricity.

Electrostatic damage to electronic devices may be caused by a direct discharge of a charged conductor, or by exposure to the static fields which surround charged objects. To avoid damage to drive electronic assemblies, service personnel must observe the following precautions when servicing the drive:

- Ground yourself to the drive - whenever the drive electronics are or will be exposed; connect yourself to ground with a wrist strap (see table 2-1). Connection may be made to any metal assembly or to the ground lug at the rear of the drive. As a general rule, remember that you, the drive, and the circuit cards must all be at ground potential to avoid potentially damaging static discharges.
- Keep boards in conductive bags - when circuit boards are not installed in the drive, keep them in conductive static shielding bags (see table 2-1). These bags provide absolute protection from direct static discharge and from static fields surrounding charged objects. Remember that these bags are conductive and should not be placed where they might cause an electrical short circuit.
- Remove boards from bags only when you are grounded - all boards received from the factory are in static shielding bags, and should not be removed unless you are grounded.
- Turn off power to drive before removing or installing any circuit boards.
- Never use an ohmmeter on any circuit board.

MAINTENANCE TOOLS AND MATERIALS

GENERAL

The maintenance procedures described in this manual require the use of certain special tools, test equipment, and materials. These are listed in table 2-1 along with the appropriate CDC part number. Note that the list only includes special tools. It is assumed that the service person has normal maintenance tools.

TABLE 2-1. MAINTENANCE TOOLS AND MATERIALS

Description	Part Number
AETN Head Alignment Card	CDC 54026900**
AETN Power Cable	CDC 92774400**
AETN Signal Cable	CDC 76041700**
AJWN (Servo Status Display Card)	CDC 54058100
AJWN Signal Cable	CDC 81787000
C/E Pack	CDC 95175103
Coil Alignment Tool	CDC 92555212
Data Pack	CDC 95175100
Feeler Gauge, Set 0.0015 thru 0.025 in	CDC 12210940
Field Test Unit (TB216A)	CDC 82338800
Foam Swabs (50 per box)	CDC 12218463
Head Adjustment Tool	CDC 75018805**
Head Alignment Kit	CDC 92333500
Jumpers, Pkg. (for logic board pins)	CDC 77612622

Table Continued on Next Page

TABLE 2-1. MAINTENANCE TOOLS AND MATERIALS (Contd)

Description	Part Number
Oscilloscope, Dual Trace	Tektronix 475A or equivalent
Pin Straightener	CDC 87369400
Pressure Gauge, Differential (optional)	CDC 73040100
Rail Alignment Fixture (Lower)	CDC 92555215
Rail Alignment Fixture (upper)	CDC 92555213
Scope Probe Tip (Hatchet type)	CDC 12212885
Screwdriver Bit, Hex Head (3/32 in)	CDC 87016701
Screwdriver, Torque (2 to 35 lbf·in)	CDC 12218425
Static Shielding bags and Ground Wrist Straps	*
Volt/ohmmeter	Ballantine 345 or equivalent digital volt- meter
Wire Seating Tool (for power harness)	CDC 12263607
<p>* See Accessories in Parts Data (Section 4 of Hardware Maintenance, Volume 1).</p> <p>** Part of Head Alignment Kit</p>	

Use of the items listed in table 2-1 is described in the procedures in which they are required. Additional information is provided on the JWN Servo Status Display Board (see section 3, Trouble Analysis) and the field test unit (see Testing the Drive).

TESTING THE DRIVE

GENERAL

During testing and troubleshooting, the drive is normally required to perform various operations such as reading and writing test data. Either a field test unit (FTU) or system software can be used to control the drive during these operations.

FIELD TEST UNIT

The TB216A is the FTU recommended for use with the drive (see table 2-1 for part number). The TB216A allows the drive to be operated and controlled independent of the rest of the system. The following, outlines the procedure for connecting the FTU to the drive. For specific instructions on connecting and operating the FTU, see the FTU manual.

CAUTION

To avoid possible damage to interface circuitry, always deenergize drive, controller, and FTU before removing or installing I/O cables.

During testing, the FTU I/O cables must be connected to the drive in place of the system I/O cables. Before disconnecting the system I/O cables, disable the controller and set the power supply circuit breaker CBl to the OFF position. In a daisy chain system, power off all the drives.

When the system is powered down, remove the system I/O cables from the drive to be tested. Connect the FTU A cable to drive connector J3 and the FTU B cable to drive connector J2. Connect a terminator to drive connector J4. See the installation section of hardware maintenance volume 1 for the terminator and its CDC part number. In a daisy chain system, make whatever connections are necessary to ensure that the other drives remain under system control, and restore power to the other drives.

At the completion of testing, restore the drive to normal operation by reversing the process outlined above.

SYSTEM SOFTWARE

The drive may also be tested by use of microdiagnostic test programs. This requires use of the controller and the appropriate software. In this type of testing, the drive communicates with the controller as in normal online operations. Special I/O connections are unnecessary.

Refer to manuals or other documentation applicable to the specific system or subsystem for information concerning the system software routines.

DATA PACKS

The maintenance procedures refer to three types of data packs: (1) customer (2) scratch and (3) CE. All three are physically identical, but are used for different purposes.

A customer pack refers to a pack used by the customer for data storage during normal on-line operations.

The CE pack contains special prerecorded information used during Head Alignment. Use care to ensure that this data is not destroyed or altered.

A scratch pack is simply a pack that does not contain customer or other information that must not be destroyed. Therefore, it can be used in maintenance procedures where a danger exists that the data pack could be damaged or its information altered.

DATA PACK INSTALLATION-REMOVAL

Refer to the operation section of the Hardware Maintenance Manual Volume 1, for information on pack installation and removal.

IDENTIFYING TEST POINTS

The drive circuit boards have test points to aid in signal tracing during maintenance and troubleshooting. These test points appear, physically, as shown on figure 2-1 and may be located anywhere on the component side of the circuit boards. The logic diagrams show the test points schematically.

The diagrams and maintenance procedures identify a test point by referring to the coordinate locator code and in some cases letter designator. TPG620 (B) is an example of a test point reference. Here, G620 is the component locator and "B" is the letter designator. The coordinate locator code indicates where the test point is located on the board. The introduction to diagrams section explains how to use the coordinate locators. The letter designators are letters, silk screened onto the board, that progress in alphabetical order from left to right and top to bottom. See figure 2-2. Not all test points have letter designators. In the procedures, the letter designator is always in parentheses, following the locator code.

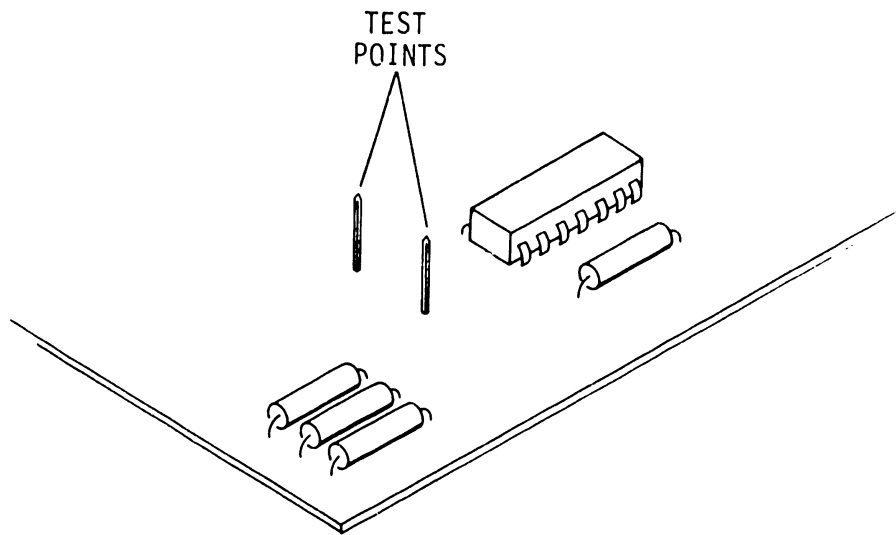
ACCESSING ASSEMBLIES FOR MAINTENANCE

The major drive assemblies and components are shown on figure 2-3. These parts are accessed by extending the drive on its slides and removing the top cover.

Extend the drive by using a screwdriver or similar tool to lift the cabinet latch and pulling the drive forward. See figure 2-3. When extending the drive, exercise caution to ensure that the equipment rack remains stable. Also, take care that the system cabling is not damaged when sliding the drive in and out of the rack.

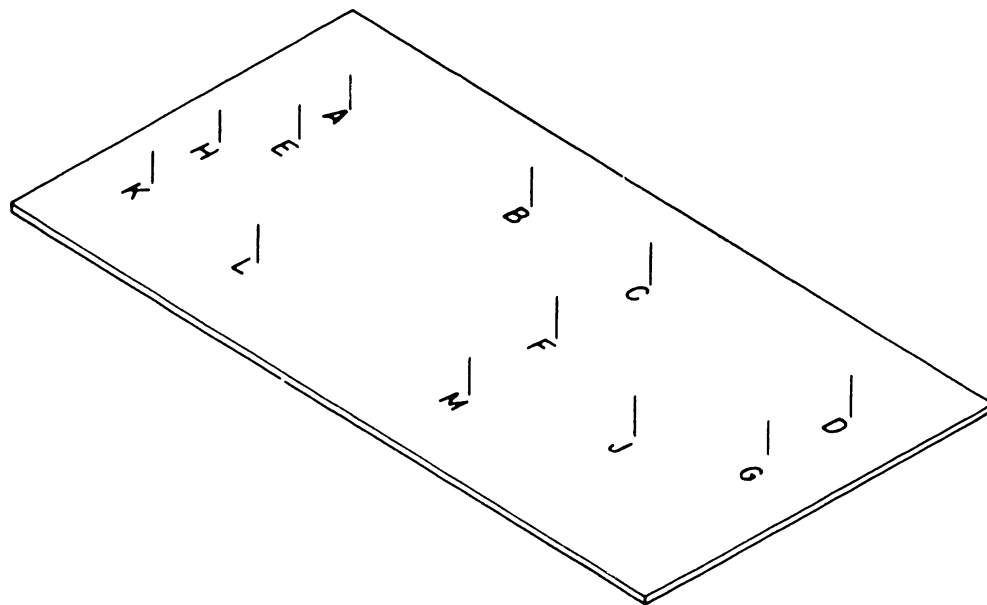
If it is necessary to remove the drive from the slides, see Entire Drive Removal procedure in section 5 of this manual. Section 5 also contains a top cover removal procedure and procedures for removing most of the other field replaceable parts, including the circuit boards.

Extending the drive and removing the top cover allows access to most circuit board test points. As shown on figure 2-3, the EBN/EDN, PGX, and PEX boards are readily accessible. The PFX is reached by raising the PGX (which is hinge mounted), to the upright position. The PMX board is mounted between the slide rails at the rear of the drive and slides out for maintenance when the attaching cables are removed. The PDX board is mounted to the back side of the PFX board on plastic clips. The PCX and UUN boards can be accessed by performing Main Logic Maintenance Position procedure.



10R109

Figure 2-1. Test Points



10R110

Figure 2-2. Test Point Letter Designators

ACCESSING DECK ASSEMBLY PARTS

The following procedures describe how to gain access to deck assembly parts during maintenance. Each procedure is assigned a unique number. The numbers are used elsewhere in the manual to reference the procedures. The procedures in this section are organized into the following category: 21XX.

2101 - MAIN LOGIC - MAINTENANCE/NORMAL POSITION

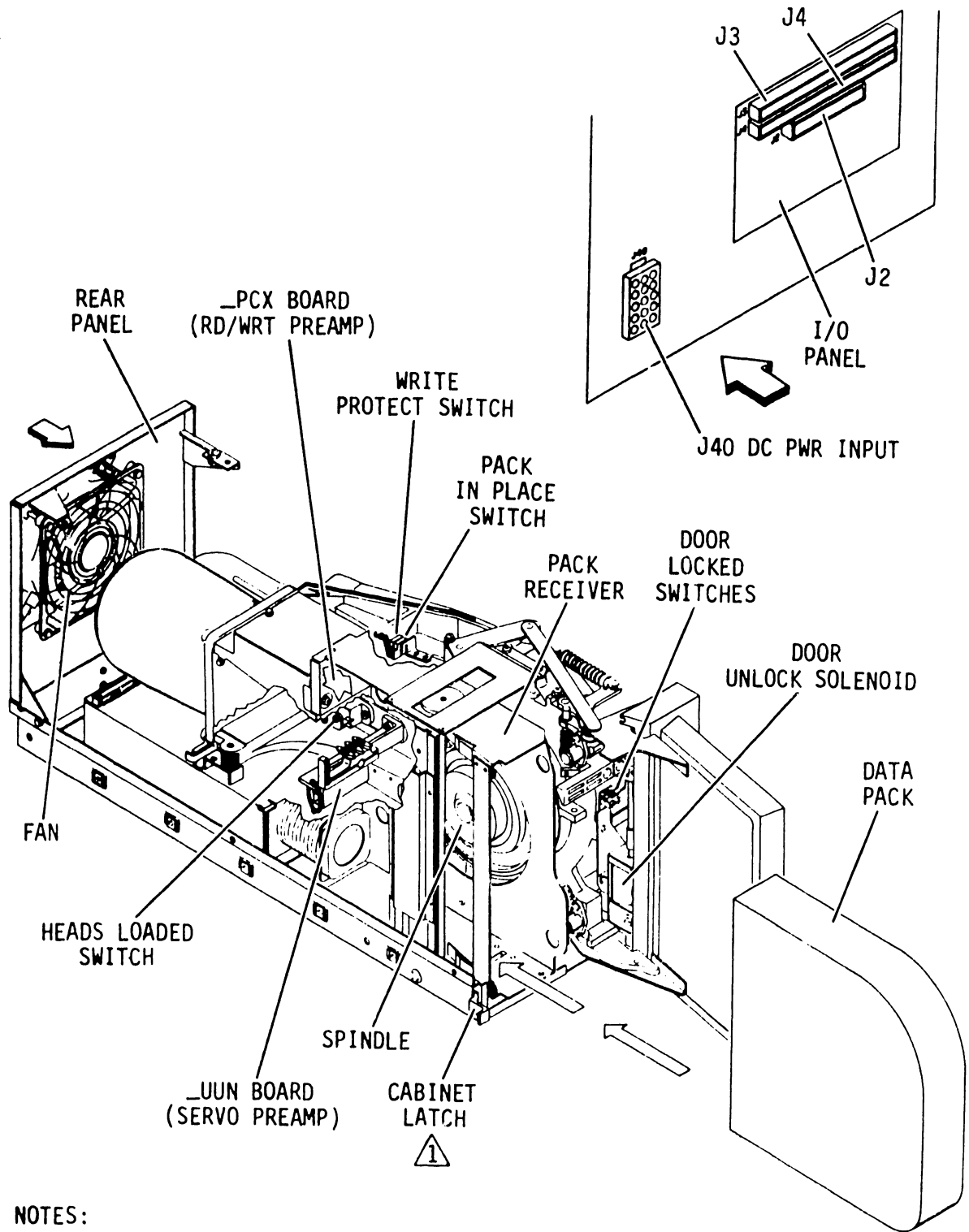
This procedure describes how to swing out the control board bracket assembly.

MAINTENANCE POSITION

CAUTION

With the top cover removed, electrostatic sensitive components are exposed and may be seriously damaged by static electricity. To avoid possible damage, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual.

1. Perform top cover removal procedure (proc 5102).
2. Disconnect P22 and P43 from _PDX board.
3. Disconnect P25, P26 and P28 from _PEX board and feed P25 and P26 cables between the read/write boards and _PEX board bracket.
4. Disconnect P42 from _PCX board.
5. Remove the two screws securing read/write boards to vertical and rear panel brackets. Swing boards up and lock into place. See figure 2-4.
6. Unlock the two quarter turn fasteners securing _PEX board bracket to drive frame. Lift bracket assembly up and swing out.



NOTES:

⚠ LIFT LATCH TO EXTEND DRIVE

10R240-1A

Figure 2-3. Component Locator (Sheet 1 of 6)

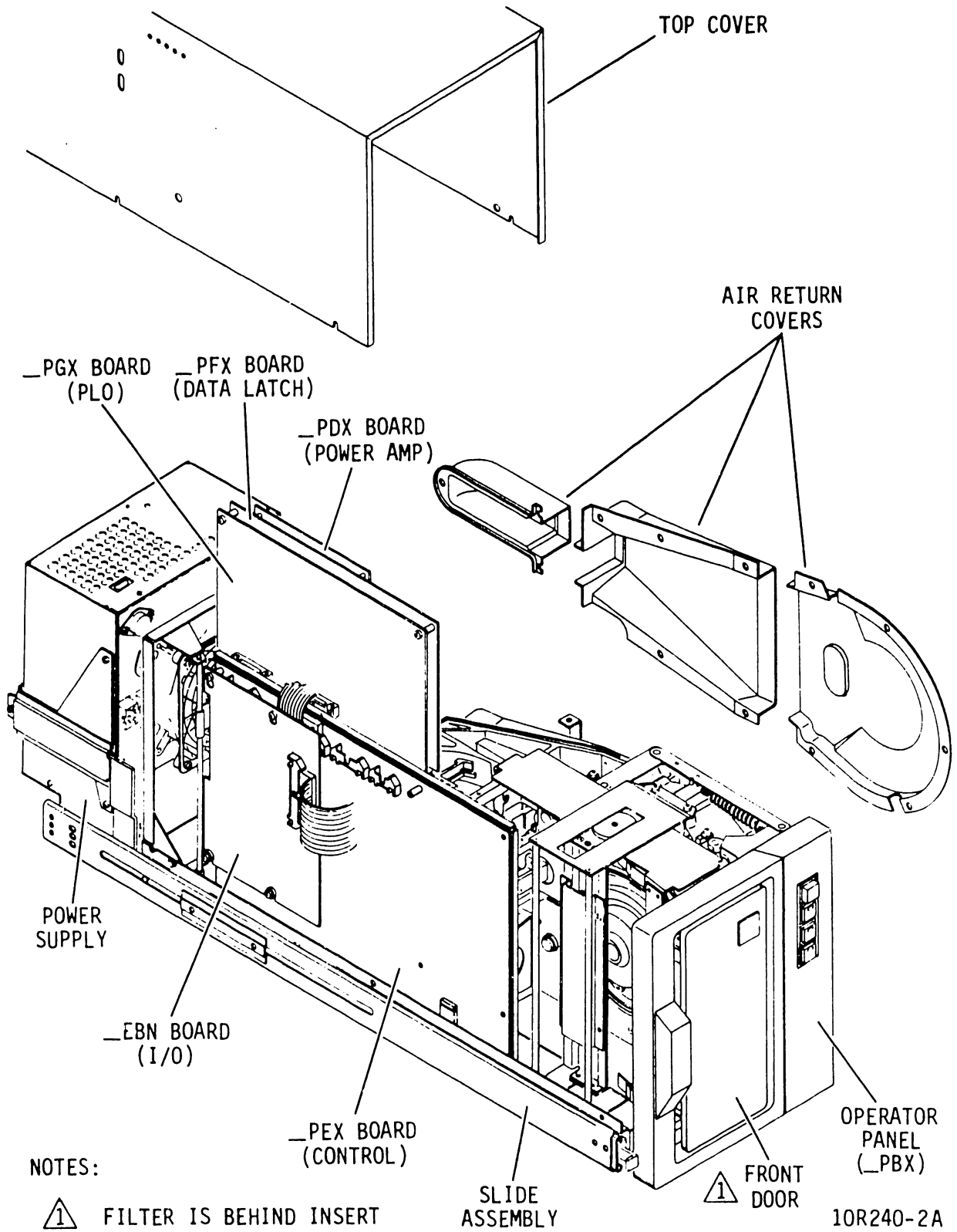
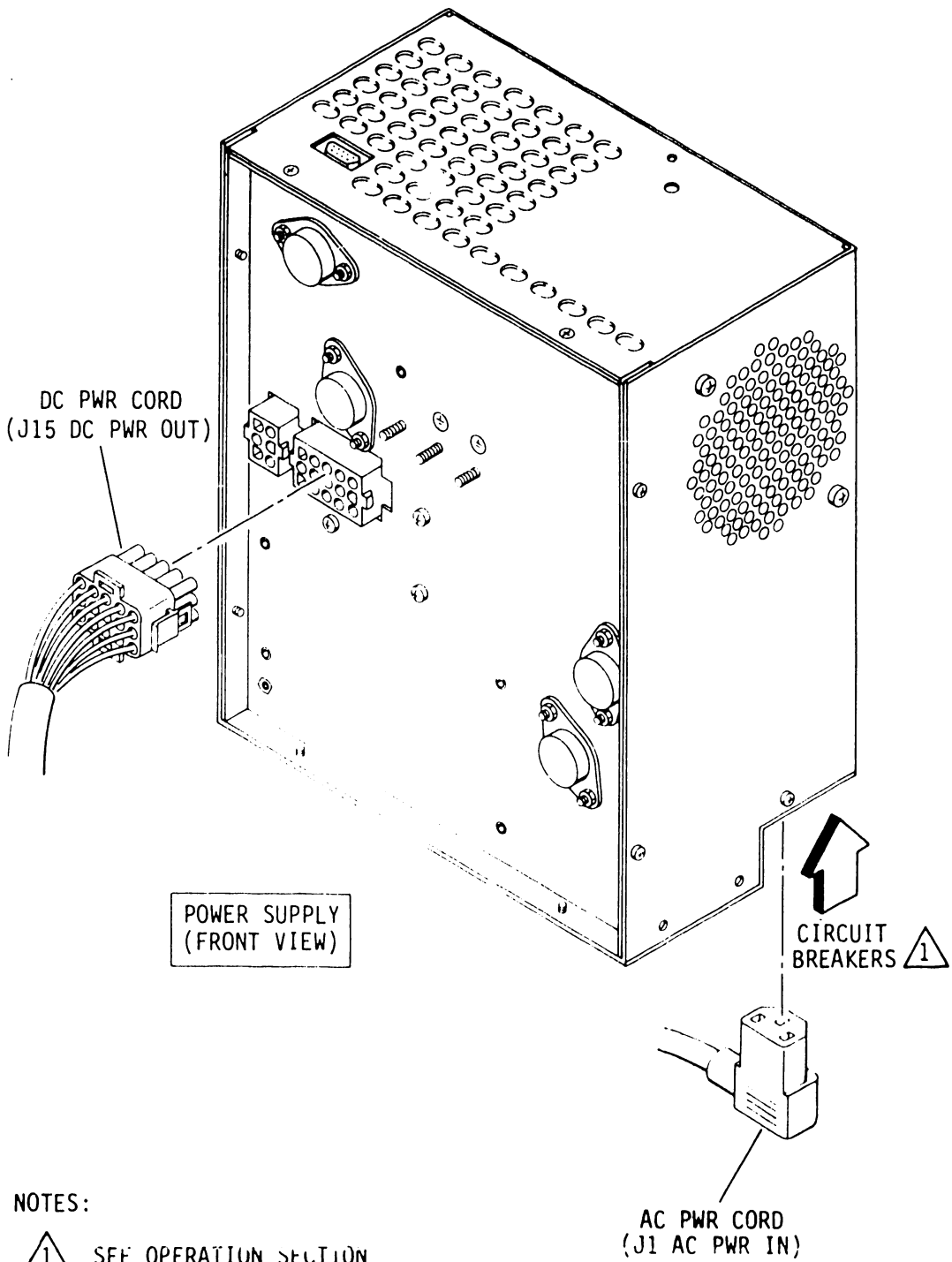


Figure 2-3. Component Locator (Sheet 2)

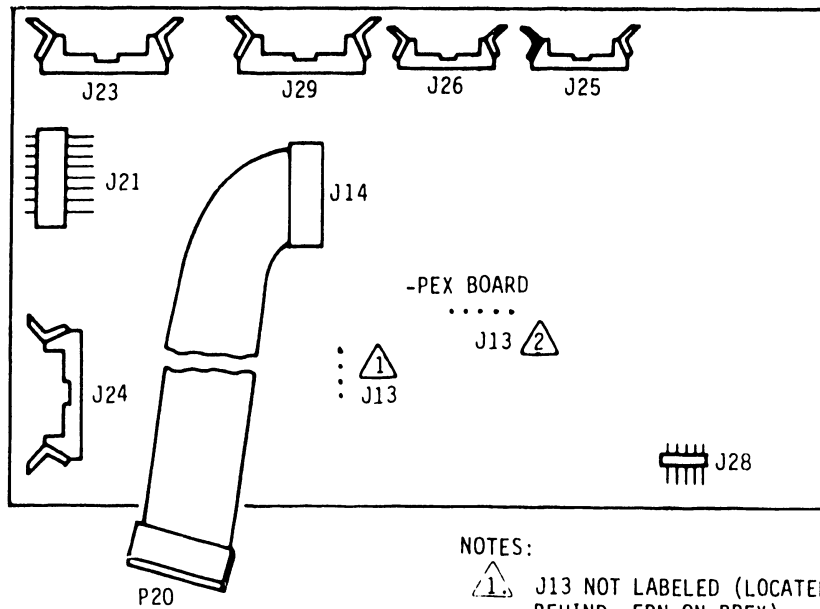
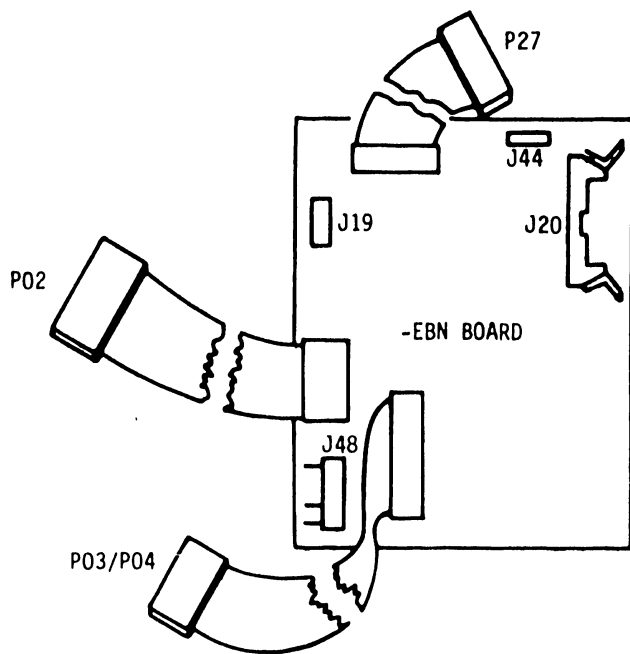


NOTES:

SEE OPERATION SECTION
OF MAINT. VOL. 1

10R240-3

Figure 2-3. Component Locator (Sheet 3)

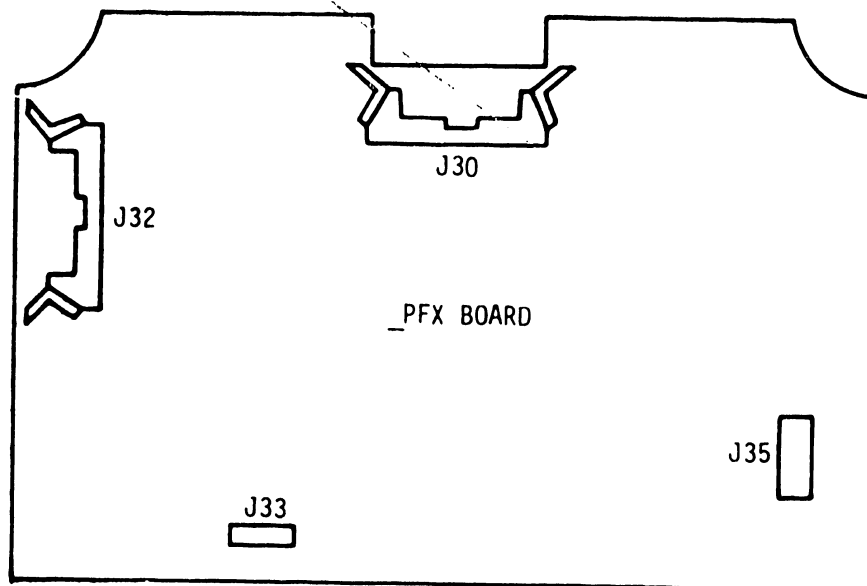
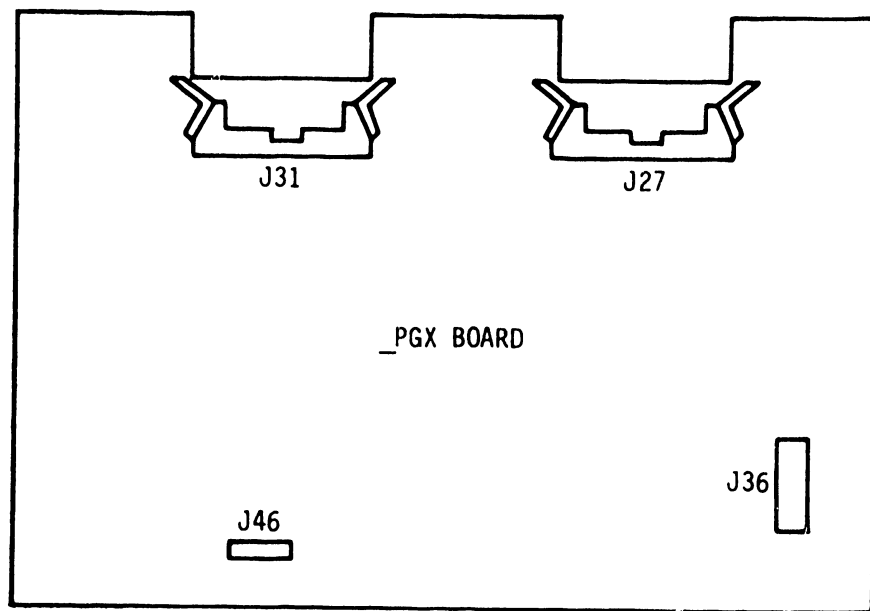


NOTES:

- ⚠ J13 NOT LABELED (LOCATED BEHIND _EBN ON BPEX).
- ⚠ J13 LABELED ON CPEX AND ABOVE.

10R240-4

Figure 2-3. Component Locator (Sheet 4)



10R240-5

Figure 2-3. Component Locator (Sheet 5)

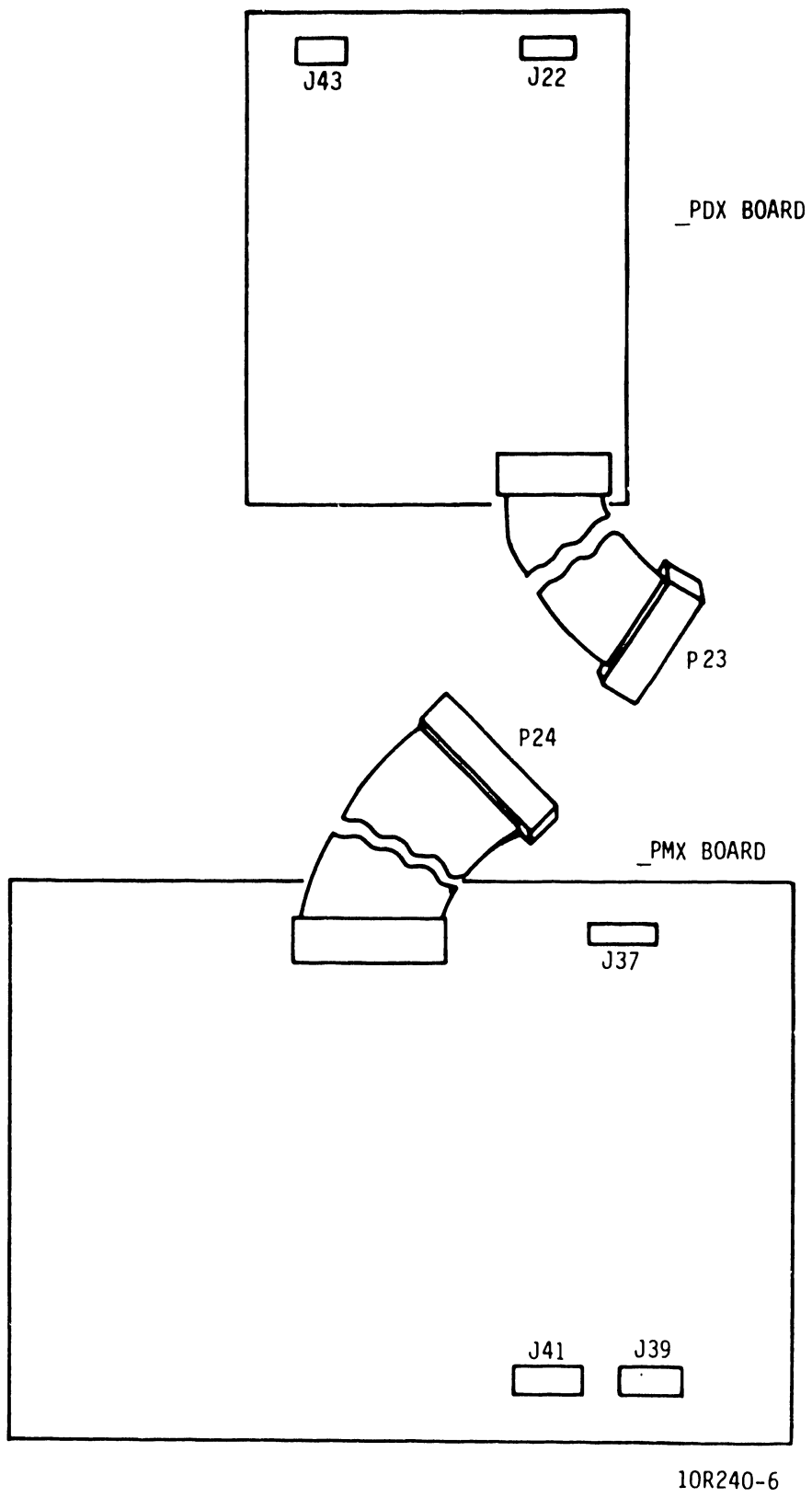


Figure 2-3. Component Locator (Sheet 6)

NORMAL OPERATING POSITION

1. Feed P25 and P26 cables between read/write boards and the _PEX board bracket.
2. Ensure that the P28 cable from _UUN board is guided into place; then swing _PEX board bracket back to its normal (operating) position and lock into place with quarter turn fasteners. See figure 2-4.
3. Swing read/write boards down (onto support brackets) and secure into place.
4. Connect P42 to J42 on _PCX board.
5. Connect P22 to J22 and P43 to J43 on _PDX board.
6. Connect P25 to J25, P26 to J26 and P28 to J28 on _PEX board.
7. Perform top cover replacement procedure (proc 5102).

2102 - MAIN LOGIC - REMOVAL/REPLACEMENT

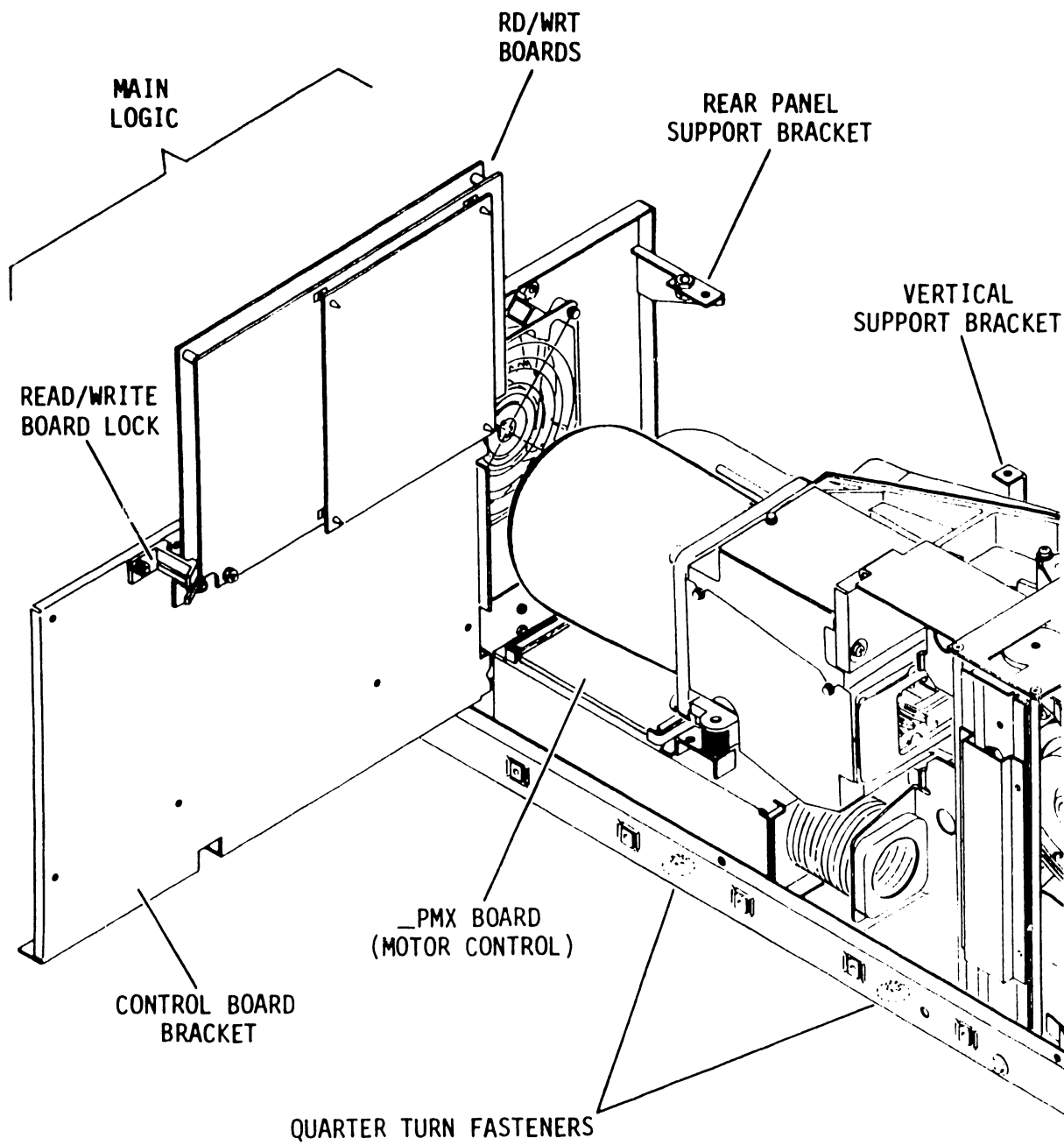
This procedure describes how to remove and replace the main logic and rear panel assembly.

REMOVAL

CAUTION

With the top cover removed, electrostatic sensitive components are exposed and may be seriously damaged by static electricity. To avoid possible damage, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual.

1. Perform top cover removal procedure (proc 5102).
2. Disconnect P22 and P43 from _PDX board.
3. Disconnect P25, P26 and P28 from _PEX board and feed P25 and P26 cables between read/write boards and the _PEX board bracket.
4. Disconnect P42 from _PCX board .



10R241

Figure 2-4. Main Logic (Maintenance Position)

5. Remove screw securing read/write boards to vertical support bracket (located at coordinates K802 on _PGX board). See figure 2-5.
6. Slide _PMX board out far enough to gain access to P37 and P39. Do not attempt to disconnect P24 (ribbon cable) that goes to the _PEX board. Carefully slide _PMX board out and lay it on the _PGX board.
7. Remove I/O cables and disconnect DC power cable at J40 from drive.
8. Unlock the two quarter turn fasteners securing control board bracket to drive frame. Refer to figure 2-4.

NOTE

Ensure _PMX board does not fall out of slides when main logic is removed or replaced.

9. Loosen screws attaching rear panel to frame. Remove entire assembly from drive (main logic and rear panel).

REPLACEMENT

1. Install main logic and rear panel assembly to drive and lock control board bracket into position. See figure 2-5.
2. Install I/O cables and connect DC power cable (P40 to J40).
3. Carefully slide _PMX board into position and connect P37 to J37 and P39 to J39.
4. Guide P25 and P26 cables between read/write boards and the _PEX board bracket.
5. Secure read write/boards to vertical support bracket.
6. Connect P42 to J42 on _PCX board.
7. Connect P25 to J25, P26 to J26 and P28 to J28 on _PEX board.
8. Connect P22 to J22 and P43 to J43 on _PDX board.
9. Perform Top Cover Replacement procedure (proc 5102).

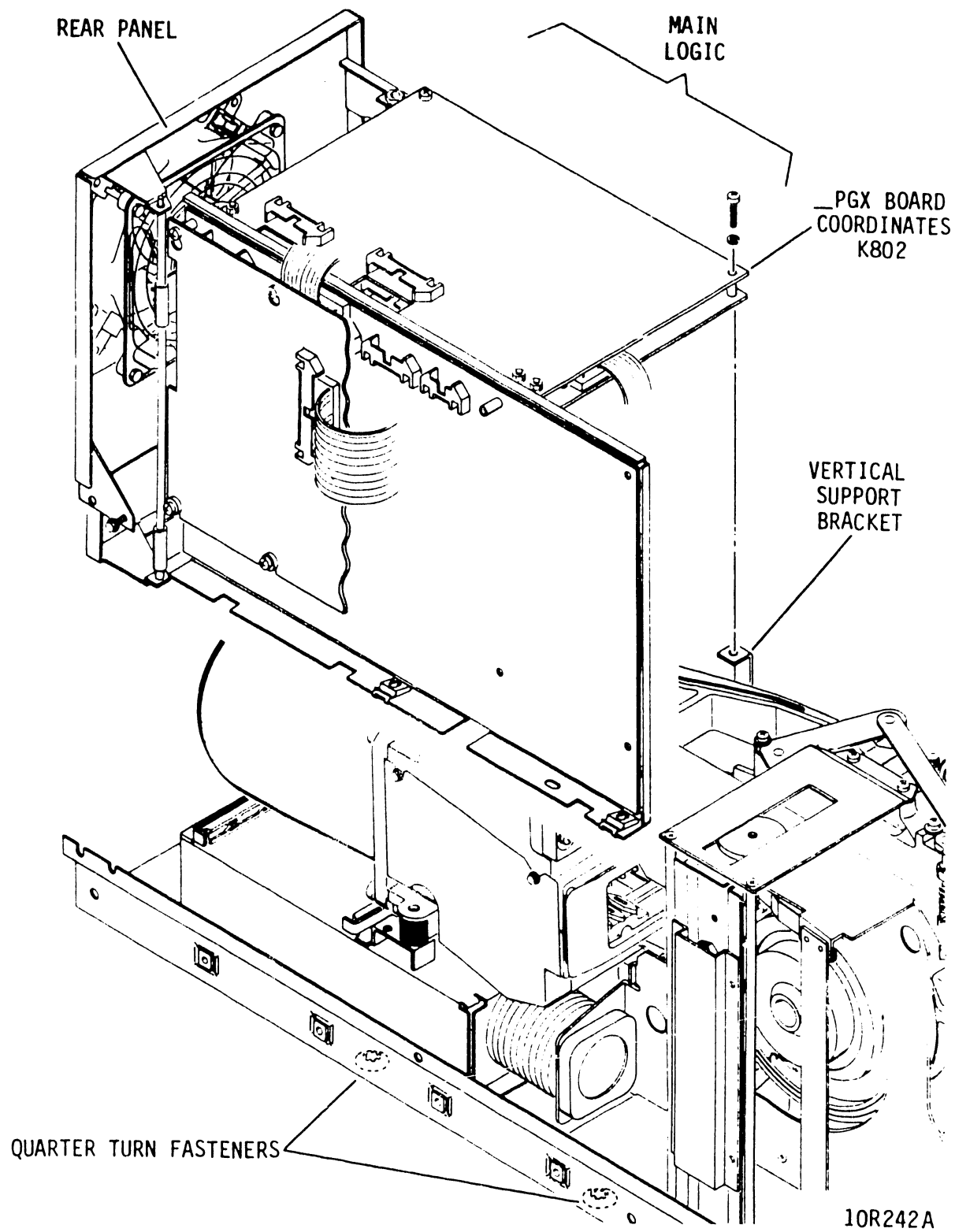


Figure 2-5. Main Logic (Removal/Replacement)

2103 - OVERRIDING FRONT DOOR INTERLOCK

This procedure describes how to override the front door interlock when a malfunction prevents normal operation of the door unlock solenoid.

1. Perform top cover removal procedure (proc 5102).
2. Place main logic in the maintenance position (proc 2101).
3. Remove top air cover to gain access to heads.
4. Ensure that the heads are in the fully retracted position. If they are extended, manually retract carriage.

CAUTION

Do not attempt to open front door when heads are extended into the pack area or damage to pack and heads will result.

5. Referring to figure 2-6, use a thin blade such as a standard six inch scale or knife blade, between door seal and base pan to push shaft of door unlock solenoid upward while pulling door handle to open front door.

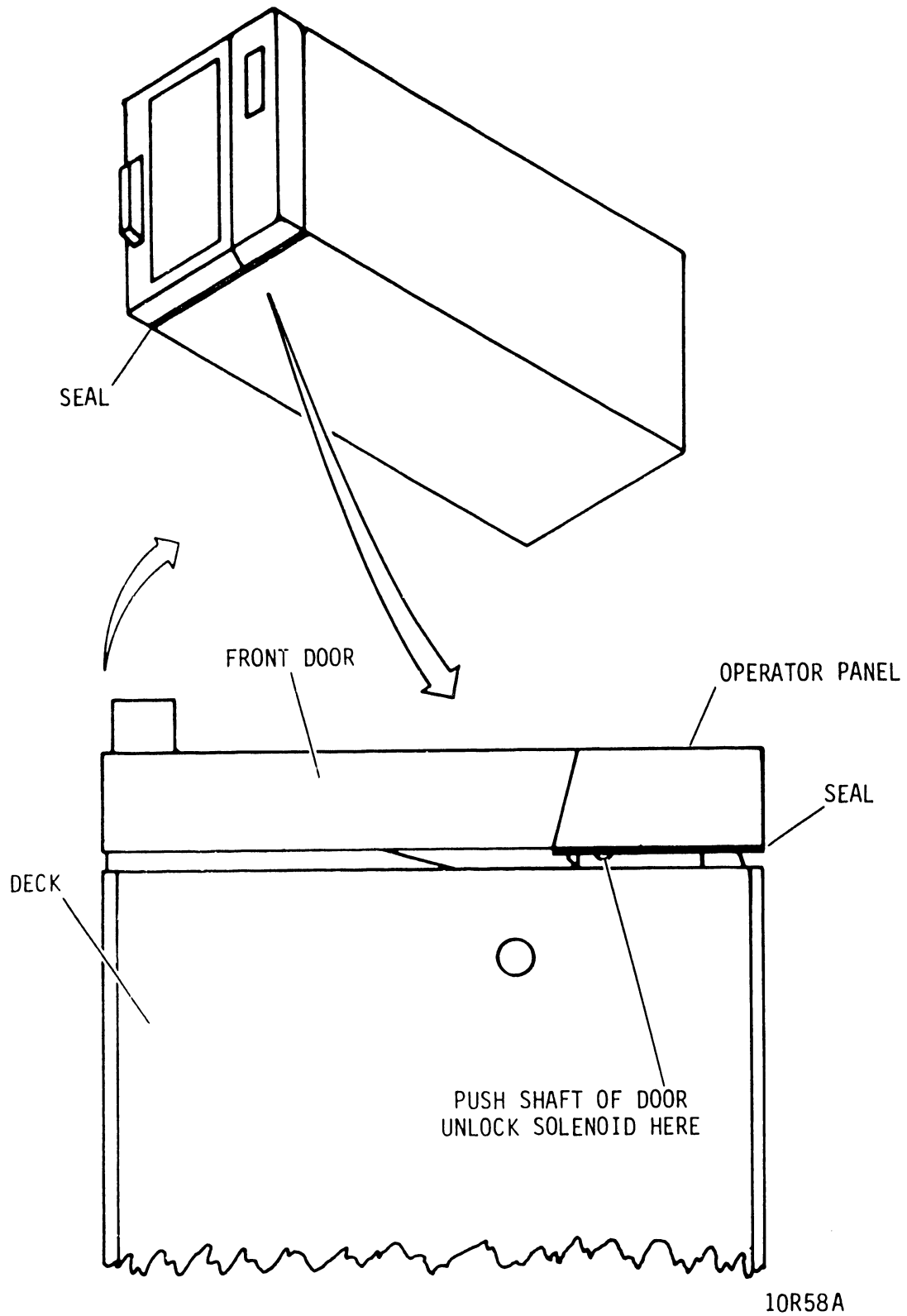


Figure 2-6. Releasing Door Unlock Solenoid

SECTION

3

TROUBLE

ANALYSIS

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

The trouble analysis section contains information on isolating and correcting problems causing improper drive operation. Persons performing troubleshooting should be thoroughly familiar with drive operation and with all information in the general maintenance section of this manual (particularly the warnings and precautions).

Because of the many types of malfunctions that may occur, the information in this section will not provide a solution to every problem. The intention, therefore, is to solve common problems and to provide a starting point for the rest. The final recommendation in all cases is to call field support.

Trouble analysis information is divided into two parts:

- Troubleshooting procedures
- Servo Status Codes

The troubleshooting procedures describe how to isolate and correct common drive problems. The procedures cover all the major areas of drive operation: power, servo, read and write. The servo status codes apply specifically to the servo system and describe the status codes presented by the MPU during servo operation. Probable causes and corrective actions are also included with the servo status code definitions.

Many of the corrective actions in this section refer to procedures given in Section 4 - Electrical Checks and Section 5, Repair and Replacement. All procedures are referred to by number. For example, a reference to procedure 4201 refers to 4201 - Tribit Check in section 4. The first digit always indicates the section (4 or 5) where the procedure is found.

TROUBLESHOOTING PROCEDURES

The troubleshooting procedures describe how to isolate and correct common drive problems. Figure 3-1 is an example of a troubleshooting procedure and explains the format. The following paragraphs explain how to use the troubleshooting procedures.

Before starting a procedure, ensure that all assumptions have been satisfied. The assumptions along with other advisory information is given in the introductory paragraph to the procedure and describe conditions that must exist for the procedure to be valid.

When the assumptions are satisfied, proceed to the first step of the procedure. After performing the action or answering the question, follow the line down to the next step. For a question, follow the line beneath the appropriate Y (yes) or N (no) response. Continue until a corrective action is reached.

After taking the first recommended action, retest the unit. If the test results do not change, try recommended action 2, and so on, being sure to retest after each action. The corrective actions which are easier to perform (checking a signal or changing a circuit board, for example) are listed before the more difficult tasks such as replacing the carriage. If the corrective actions do not solve the problem, call field support.

The procedures appear in the following order:

- TSP1 - Power Check: Provides an overall check of drive power.
- TSP2 - +5 Volt Check: Shows how to isolate problems in the +5 volt loads.
- TSP3 - +24 Volt Load Check: Shows how to isolate problems in the +24 volt loads.
- TSP4 - First Seek Check: Provides possible causes for the drive failing to successfully complete a first seek.

- TSP5 - Direct or RTZ Seek Check: Provides possible causes for the drive failing to successfully complete a direct or RTZ seek.
- TSP6 - Write Check: Provides information for isolating cause of write errors.
- TSP7 - Read Check: Provides information for isolating cause of read errors.
- TSP8 - Address Mark Check: Provides possible causes for read or write address mark problems.

INDICATES THAT THIS IS SHEET 1
OF TROUBLESHOOTING PROCEDURE 1
(TSP31-1). SHEET 2 WOULD BE TSP31-2

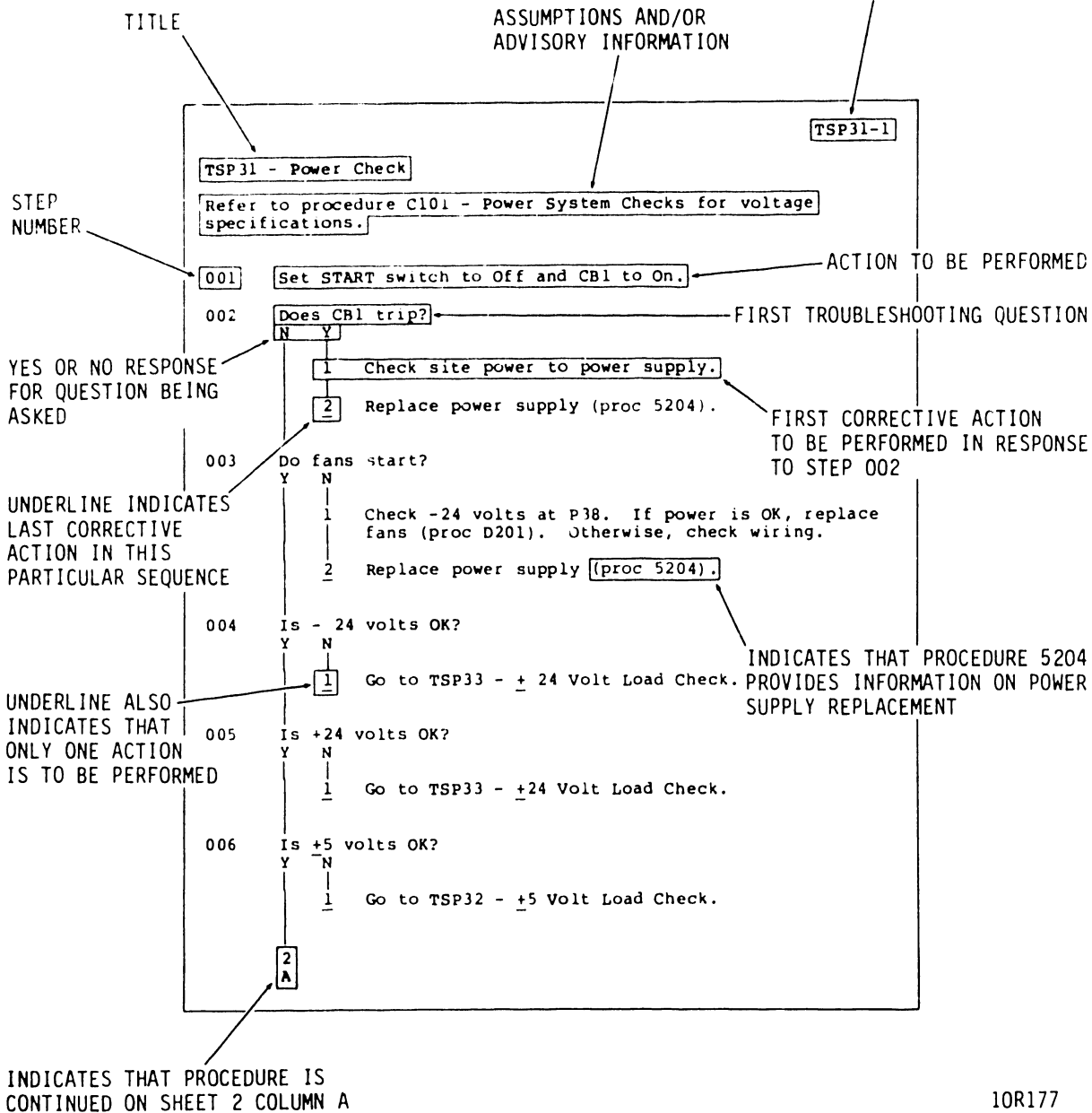


Figure 3-1. Example of Troubleshooting Procedure

TSP1 - Power Check

Refer to procedure 4101 - Power System Checks for voltage specifications.

001 Set START switch to Off and CBI to On.

002 Does CBI trip?

- | | | |
|---|----------|---|
| N | Y | |
| | | |
| | 1 | Ensure power supply is set at proper voltage. |
| | | |
| | 2 | Check site power to power supply. |
| | | |
| | <u>3</u> | Replace power supply (proc 5203). |

003 Does fan start?

- | | | |
|---|----------|--|
| Y | N | |
| | | |
| | 1 | Check -24 volts at P38 or P48 (<u>_</u> EBN/ <u>_</u> EDN).
If power is OK, replace fan (proc 5201).
Otherwise, check wiring. |
| | | |
| | <u>2</u> | Replace power supply (proc 5203). |

004 Is - 24 volts OK?

- | | | |
|---|----------|---|
| Y | N | |
| | | |
| | <u>1</u> | Go to TSP3 - <u>±</u> 24 Volt Load Check. |

005 Is +24 volts OK?

- | | | |
|---|----------|---|
| Y | N | |
| | | |
| | <u>1</u> | Go to TSP3 - <u>±</u> 24 Volt Load Check. |

006 Are ±5 volts OK?

- | | | |
|---|----------|--|
| Y | N | |
| | | |
| | <u>1</u> | Go to TSP2 - <u>±</u> 5 Volt Load Check. |

007 Is -8.3 volts OK?

- | | | |
|---|---|--|
| Y | N | |
| | | |
| 2 | 2 | |
| A | B | |

A	B	
1	1	
	<u>1</u>	Disconnect P28 and recheck -8.3 volts. If -8.3 volts is OK, replace _UUN (proc 5306). If -8.3 volts is still abnormal, replace _PEX (proc 5304).
008	Are <u>+40</u> volts OK?	
Y	N	
	1	Disconnect P37 and recheck. If voltage is normal, replace _PMX (proc 5308). Otherwise, proceed to next action.
	<u>2</u>	Disconnect P22 and recheck. If voltage is normal, replace _PDX (proc 5307).
009	Power Check OK. If problem persists, call field support.	

TSP2 - ± 5 V Load Check

This check isolates problems with ± 5 volts. Refer to procedure 4101 - DC Power Check for voltage specifications.

- 001 Deenergize drive and check for short circuits between:
 | o +5 volts or -5 volts and ground.
 | o +5 volts and -5 volts.
 | o ± 5 volts and ± 24 volts.
- 002 Do any short circuits exist?
 N Y
 | 1 Remove loads (one at a time) to isolate short.
 | 2 Inspect wiring and boards.
- 003 Remove all loads, except P21 (PEX) from ± 5 volts by disconnecting P19 (EBN/EDN), P24 and P39 (PMX), P35 (PFX), P36 (PGX), P32 (PCX), P26 (operator panel), then recheck voltages.
- 004 Are ± 5 volts OK?
 Y N
 | 1 Check wiring and power supply.
 | 2 Replace PEX (proc 5304).
- A
- 005 Deenergize drive, add PMX to +5 volt load by connecting P24 and P39, then recheck voltages.
- 006 Is +5 volts OK?
 Y N
 | 1 Replace PMX (proc 5308).
- 007 Deenergize drive, add operator panel to +5 volt load by connecting P26, then recheck voltages.

```

A
1
|
008 Is +5 volts OK?
Y   N
|   |
|   1   Replace operator panel (proc 5202).
|
|
009 Deenergize drive add _EBN/EDN to ±5 volt load by connect-
    ing P19, then recheck voltages.
|
|
010 Are +5 volts OK?
Y   N
|   |
|   1   Replace _EBN/_EDN (proc 5303).
|
|
011 Deenergize drive, add _PGX to ±5 volt load by connecting
    P36, then recheck voltages.
|
|
012 Are +5 volts OK?
Y   N
|   |
|   1   Replace _PGX (proc 5301)
|
|
013 Deenergize drive, add _PFX to ±5 volt load by connecting
    P35, then recheck voltages.
|
|
014 Are +5 volts OK?
Y   N
|   |
|   1   Replace _PFX (proc 5302).
|
|
|   1   Replace power supply (proc 5203).  If problem per-
|   sists call field support.
|
|
015 Deenergize drive, add _PCX to ±5 volt load by connect-
    ing P32, then recheck voltages.
|
|
|   Are ±5 volts OK?
|   Y   N
|   |   |
|   |   1   Replace _PCX (proc 5305).
|   |
|   |

```

TSP3 - +24 Volt Load Check

This check isolates problems with +24 volts. Refer to procedure 4101 - Power Checks for voltage specifications.

- 001 Deenergize drive and check for short circuits between:
 | o +24 volts and -24 volts and ground.
 | o +24 volts and -24 volts.
 | o +24 volts and +5 volts.
- 002 Do any short circuits exist?
 N Y
 | |
 | 1 Remove loads (one at a time) to isolate short.
 | |
 | 2 Inspect wiring and boards.
- 003 Remove all loads, except P21 (PEX) from +24 volts by
 disconnecting P37 (PMX), P22 (PDX), P19 (EBN/EDN)
 and P38 or P48 (EBN/EDN) (fan), then recheck voltages.
- 004 Are +24 volts OK?
 Y N
 | |
 | 1 Check wiring and power supply.
- 005 Deenergize drive, add PMX to +24 volt load by connecting
 P37, then retest.
- 006 Is +24 volts OK?
 Y N
 | |
 | 1 Replace PMX (proc 5308).
 | |
 | 2
 | A

A
 1
 |
 007 Deenergize drive, add PDX to +24 volt load by connecting
 P22, then retest.
 |
 008 Are +24 volts OK?
 Y N
 | |
 | 1 Replace PDX (proc 5307).
 |
 009 Deenergize drive, add EBN/EDN to +24 volt load by con-
 necting P19, then recheck voltages.
 |
 010 Are +24 volts OK?
 Y N
 | |
 | 1 Replace EBN/EDN (proc 5303).
 |
 011 Deenergize drive, add fan to +24 volt load by connecting
 P38 or P48 (EBN/EDN), then retest.
 |
 012 Are +24 volts OK?
 Y N
 | |
 | 1 Replace fan (proc 5201).
 |
 013 Replace power supply (proc 5203). If problem persists,
 call field support.

TSP4 - First Seek Check

```

001  Initiate first seek as follows:
      |   a. Set LOCAL/REMOTE switch to local.
      |   b. Set CB1 & START switch to ON.
      |
002  Does READY indicator light?
      | N   Y
      |   |
003  |   Drive has successfully completed first seek.
      |   |
004  |   Do all fault LEDs light?
      |   | N   Y
      |   |   |
005  |   |   Are ±5 volts OK?
      |   |   | Y   N
      |   |   |   |
      |   |   |   | 1   Check ±5 volts. See TSP2.
      |   |   |   |   |
      |   |   |   |   | 2   Check connection at J28 (_PEX).
      |   |   |   |   |
      |   |   |   |   | 1   Replace _PEX (proc 5304).
      |   |   |   |   |
006  |   |   Is operator panel fault light on?
      |   |   | N   Y
      |   |   |   |
      |   |   |   | Is cooling fan operating?
      |   |   |   | Y   N
      |   |   |   |   |
      |   |   |   |   | 1   Check for loose connectors at P38 on fan or
      |   |   |   |   |   | J48 on _EBN/_EDN.
      |   |   |   |   |   |
      |   |   |   |   |   | 2   If _24 volts is present at P38 (on older
      |   |   |   |   |   |   | fans) or J48 on _EBN/_EDN, replace fan (proc
5201). |   |   |   |   |   |   |
      |   |   |   |   |   |   | 3   Replace _EBN/_EDN (proc 5303).
      |   |   |   |   |   |   |
007  |   |   Does First Seek Fault LED light?
      |   |   | Y   N
      |   |   |   |
      |   |   |   | 2   2
      |   |   |   | A   B

```


	A	B	
	1	1	
008			Is Fine Position signal at a dc level between +5 volts and -5 volts?
		Y N	
			1 Check <u>±</u> 5 volts. See TSP2.
			<u>2</u> Replace <u>_</u> PEX (proc 5304).
		1	Check J25 (<u>_</u> PEX) to interlock cabling.
		2	Replace <u>_</u> PEX (proc 5304).
		<u>3</u>	Check that all interlocks work properly.
009			Does Volt Fault LED light?
	N Y		
	2	2	
	A B		
	A B		
	1	1	
		1	Check all power harness connections.
		2	Check power when drive is not seeking. See TSP1.
		3	Replace <u>_</u> PMX (proc 5308).
		4	Replace <u>_</u> PEX (proc 5304).
		<u>5</u>	Replace power supply (proc 5203).
010			Is motor running?
	N Y		
011			Are tribits OK?
		Y N	
			1 Check connections at J28 (<u>_</u> PEX).
			<u>2</u> Replace <u>_</u> PEX (proc 5304).
	3	3	
	C	D	

	C	D	
	2	2	
012			Does Fine Position signal wander between +5 volt and -5 volts?
			Y N
			1 Check J23 (_PEX) to P23 (_PDX) connection.
			2 Check J43 (_PDX) connection to voice coil.
			3 Check Power Amp Driver (proc 4206).
			4 Replace _PDX (proc 5307).
			5 Replace _PEX (proc 5304).
			6 Replace _UUN (proc 5306).
			1 Check connection at J28 (_PEX).
			2 Replace _PEX (proc 5304).
			3 Replace _UUN (proc 5306).
013			Is Motor Run signal active (_PEX, TP-K)?
			N Y
			1 Replace _PMX (proc 5208).
			2 Replace motor (proc 5209).
014			Is Start signal active (_PEX, G738 Pin 13)?
			Y N
			1 Check J26 connections (operator panel to _PEX).
			2 Replace operator panel (proc 5204).
			3 Replace _PEX (proc 5304).
			1 Replace _PEX (proc 5304).

TSP5 - Direct or RTZ Seek Check

This test assumes that the following conditions exist: (1) drive is operating under control of TB216 and (2) first seek was successfully completed.

```

001  Does FAULT indicator light or is Seek Error active?
      Y   N
      |   |
002  |   Direct or RTZ seek is OK.
      |   |
003  Does Write or Write and Read Fault LED light?
      N   Y
      |   |
      |   1  Read/write problem.  See TSP 6 or 7.
      |   |
004  Does Volt Fault LED light?
      N   Y
      |   |
      |   1  Power problem.  See TSP 1.
      |   |
005  Does On Cylinder go active?
      N   Y
      |   |
006  Does error always occur at or near the same cylinder?
      Y   N
      |   |
      |   1  Check cable connections between J28 (_PEX) and
      |   |   J34 (_UUN).
      |   |
      |   2  Replace data pack (proc 5206).
      |   |
      |   3  Replace _PEX (5304).
      |   |
      |   4  Replace _UUN (proc 5306).
      |   |
      |   1  Check servo tracks (proc 4207).
      |   |
      |   |
      |   2
      |   A

```

A
1
|
007 Does error always occur when seeking to or near the same
cylinder?
N Y
| 1 Check servo tracks (proc 4207).
| 2 Replace _PEX (proc 5304).
| 3 Replace _EBN/_EDN (proc 5303).

1 Check cabling connections between J28 (_PEX) and
J34 (_UUN).
2 Replace _EBN/_EDN (proc 5303).
3 Replace _PEX (proc 5304).
4 Replace _UUN (proc 5306).

TSP6 - Write Check

This check assumes that the drive is performing write or write format operations under control of the TB216.

```

001  Does Volt Fault LED light?
      N   Y
      |   |
      |   | 1 Power problem. Go to TSP1.
      |   |
002  Does Read and Write Fault LED light?
      N   Y
      |   |
      |   | 1 Check I/O connections.
      |   | 2 Check _EBN/_EDN to J27 (_PGX) cabling.
      |   | 3 Replace _EBN/_EDN (proc 5302).
      |   | 4 Replace _PGX (proc 5303).
      |   |
003  Does Read or Write and Not On Cylinder Fault LED light?
      N   Y
      |   |
      |   | 1 Servo problem. Go to TSP 4 or 5.
      |   |
004  Does Write Fault LED light?
      N   Y
005  |   | Is problem head related?
      |   | N   Y
006  |   | Is Write Unsafe active (_PFX, TP-N320)?
      |   | Y   N
      |   | |   |
      |   | |   | 1 Replace _PCX (proc 5305).
      |   | |   |
      2   2   2
      A   B   C

```

A	B	C
1	1	1
		1 Check head/cylinder address bits on _PFX. If bits are OK, check for loose head connectors on _PCX. Otherwise, proceed to next action.
		2 Replace _PCX (proc 5305).
		3 Check I/O connections.
		4 Check J20 (_EBN/_EDN) to J14 (_PEX) cabling.
		5 Replace _EBN/_EDN (proc 5303).
		6 Replace _PEX (proc 5304).
		7 Replace _PFX (proc 5302).
007	Is Write Unsafe active (_PFX, TP-N320)?	
	Y	N
		1 Check for data at output of _PFX. If data is absent, perform 4303 - Write Data Check.
		2 Check head/cylinder address bits on _PFX. If bits are OK, check for loose head connectors on _PCX. Otherwise, proceed to next action.
		3 Replace _PCX (proc 5305).
		1 Perform procedure 4303 - Write Data Check.
		2 Replace _PFX (proc 5302).
		3 Replace _PGX (proc 5301).
		4 Replace _PEX (proc 5304).
		5 Replace _PCX (proc 5305).
	3	
	D	

```

D
2
|
008 Perform procedure 4303 - Write Data Check.
|
009 Is the 1.612 MHz clock OK?
Y  N
|  |
|  1 Servo problem. See TSP 4 or 5.
|  |
|  |
010 Is the 2F clock OK?
Y  N
|  |
|  1 Replace _PGX (proc 5301).
|  |
|  |
011 Is the 9.67 Mhz clock OK?
Y  N
|  |
|  1 Replace _PGX (proc 5301).
|  |
|  2 Replace _EBN/_EDN (proc 5303).
|  |
|  |
012 Are Write Gate, Write Clock, and Write Data present?
Y  N
|  |
|  1 Check I/O connections.
|  |
|  2 Check _EBN/_EDN to J27 (_PGX) cabling.
|  |
|  3 Replace _EBN/_EDN (proc 5303).
|  |
|  4 Replace _PGX (proc 5301).
|  |
|  |
013 Is Write Data Compensated present?
Y  N
|  |
|  1 Replace _PGX (proc 5301).
|  |
|  |
014 Is Read/Write Data to preamplifier present?
N  Y
|  |
015 | Write Data Check OK. If problems persist, call field
|  | support.
|  |
4
D

```

016 D
3
|
Is Write Enable OK?
Y N
|
1 Check J29 (_PEX) to J30 (_PFX) cabling.
|
2 Check J20 (_EBN/_EDN) to J14 (_PEX) cabling.
|
3 Replace _PEX (proc 5304).
|
4 Replace _PFX (proc 5302).
|
1 Check J31 (_PGX) to J30 (_PFX) cabling.
|
2 Replace _PFX (proc 5302).
|
3 Replace _PCX (proc 5305).

TSP7 - Read Check

This check assumes that the drive is performing read operations under control of the TB216.

```

001   Does Volt Fault LED light?
      N   Y
      |   |
002   |   | 1   Power problem.  See TSP1.
      |   |
003   Does Read and Write Fault LED light?
      N   Y
      |   |
      |   | 1   Check I/O connections.
      |   | 2   Check _EBN/_EDN to J27 (_PGX) cabling.
      |   | 3   Replace _EBN/_EDN (proc 5303).
      |   | 4   Replace _PGX (proc 5301).
      |   |
004   Does Read or Write and Not On Cylinder Fault LED light?
      N   Y
      |   |
      |   | 1   Servo problem.  See TSP 4 or 5.
      |   |
005   Is address mark detected?
      Y   N
      |   |
      |   | 1   Perform procedure 4403 - Read AM Check and go to
      |   |       TSP8.
      |   |
006   Is there a data error?
      Y   N
      |   |
007   |   | Read operation is OK.
      |   |
      |   | 2
      |   | A

```

A
 1
 008 Are errors head related?
 N Y

1 Check head/cylinder address bits on _PFX. If bits are bad, suspect:

a. cabling problem.

b. _EBN/_EDN, _PXX, _PFX, or _PCX.

c. Replace data pack.

2 Check for loose head connectors on _PCX.

3 Replace _PFX (proc 5302).

4 Replace _PGX (proc 5301).

5 Replace _PCX (proc 5205).

6 If errors continue at one specific head location, replace that head (proc 5212).

009 Perform procedure 4402 - Read Data Check.

010 Is Read Gate active?
 Y N

1 Check I/O connections.

2 Check _EBN/_EDN to J27 (_PGX) cabling.

3 Replace _EBN/_EDN (proc 5303).

4 Replace _PGX (proc 5301).

011 Is 1.612 Mhz Clock present?
 Y N

1 Servo problem. See TSP 4 or 5.

012 Is Read Clock and 2F Read Oscillator OK?
 Y N

1 Replace _PGX (proc 5301).

3
 B

- B
2
|
- 013 Is head and preamplifier output present?
Y N
|
1 Check J32 (_PFX) to J42 (_PCX) cabling.
|
2 Check for loose head connectors on _PCX.
|
3 Replace data pack.
|
4 Replace _PCX (proc 5305).
|
5 Replace _PFX (proc 5302).
|
6 If problem continues at one specific head
location, replace that head (proc 5212).
- 014 Is Latched Read Data present?
Y N
|
1 Replace _PFX (proc 5302).
- 015 Is NRZ Read Data present?
Y N
|
1 Replace _PGX (proc 5301).
- 016 Is Read Gate and Lock to Data timing present?
Y N
|
1 Replace _PGX (proc 5301).
|
1 Replace _PFX (proc 5302).
|
2 Replace _PGX (proc 5301).
|
3 Replace _PEX (proc 5304).
|
4 Replace _PCX (proc 5305).

TSP8 - Address Mark Check

The following check assumes that the drive is under control of the TB216.

001 Perform procedure 4403 - Read AM Check.

002 Is AM Enable active?

Y N

- | | | |
|--|---|---|
| | 1 | Check I/O connections. |
| | 2 | Check _EBN/_EDN to J27 (_PGX) cabling. |
| | 3 | Check J31 (_PGX) to J30 (_PFX) cabling. |
| | 4 | Replace _PFX (proc 5302). |
| | 5 | Replace _PGX (5301). |

003 Is AM Found active?

Y N

- | | | |
|--|---|---------------------------|
| | 1 | Replace _PGX (proc 5301). |
| | 2 | Replace _PFX (proc 5302). |

004 Is AM proper length?

Y N

005 Perform procedure 4304 - Write AM Check.

006 Is AM Enable active?

Y N

- | | | |
|--|---|--|
| | 1 | Check I/O connections. |
| | 2 | Check _EBN/_EDN to J27 (_PGX) cabling. |
| | 3 | Replace _EBN/_EDN (5303). |
| | 4 | Replace _PGX (5301). |

2 2

A B

A	B
1	1
007	Is data absent during AM?
	Y N
	<u>1</u> Replace _PFX (proc 5302).
008	Write AM Check OK. If problem persists call field support.
009	Is lock to data timing OK?
	Y N
	<u>1</u> Replace _PGX (proc 5301).
010	Read AM Check OK. If problem persists, call field support.

SERVO STATUS CODES

GENERAL

The servo status codes are two digit hexadecimal codes, generated by the MPU, that indicate the operational status of the drive servo system. Whenever the drive is in a power on condition (dc power active), the MPU is periodically checking the operation of the servo system and generating appropriate status codes. The codes can be visually monitored by connecting the servo status display card (_JWN) to a test jack on the _PEX board. The following discussions explain how to install the display card and defines the various codes.

INSTALLING THE SERVO STATUS DISPLAY CARD (-JWN)

1. Set START switch and CB1 to off.
2. Connect one end of signal cable to display card and the other end to test jack at location J260 of _PEX board. See figure 3-2.
3. Proceed with testing.

SERVO STATUS CODE DEFINITIONS

Table 3-1 is a summary of all the status codes and table 3-2 provides definitions of each code. Each status code definition is divided into three parts:

1. Description: Basic definition of what type of problem the code indicates, during what operations the code appears, what additional error indications are present with the code, and how to initiate a retry or recovery from the error.
2. Probable Causes: What general areas could cause the problem. The purpose here is to provide a general idea of what functional areas could be causing the problem.
3. Actions: What specific things to check to correct the problem. Perform each action and retest the drive before proceeding to the next action. If all actions have been performed and the problem persists, call field support.

When interpreting the status codes it is important to know that not all codes appearing on the display indicate errors. Some indicate that the operation is still in progress, others that the operation has been successfully completed.

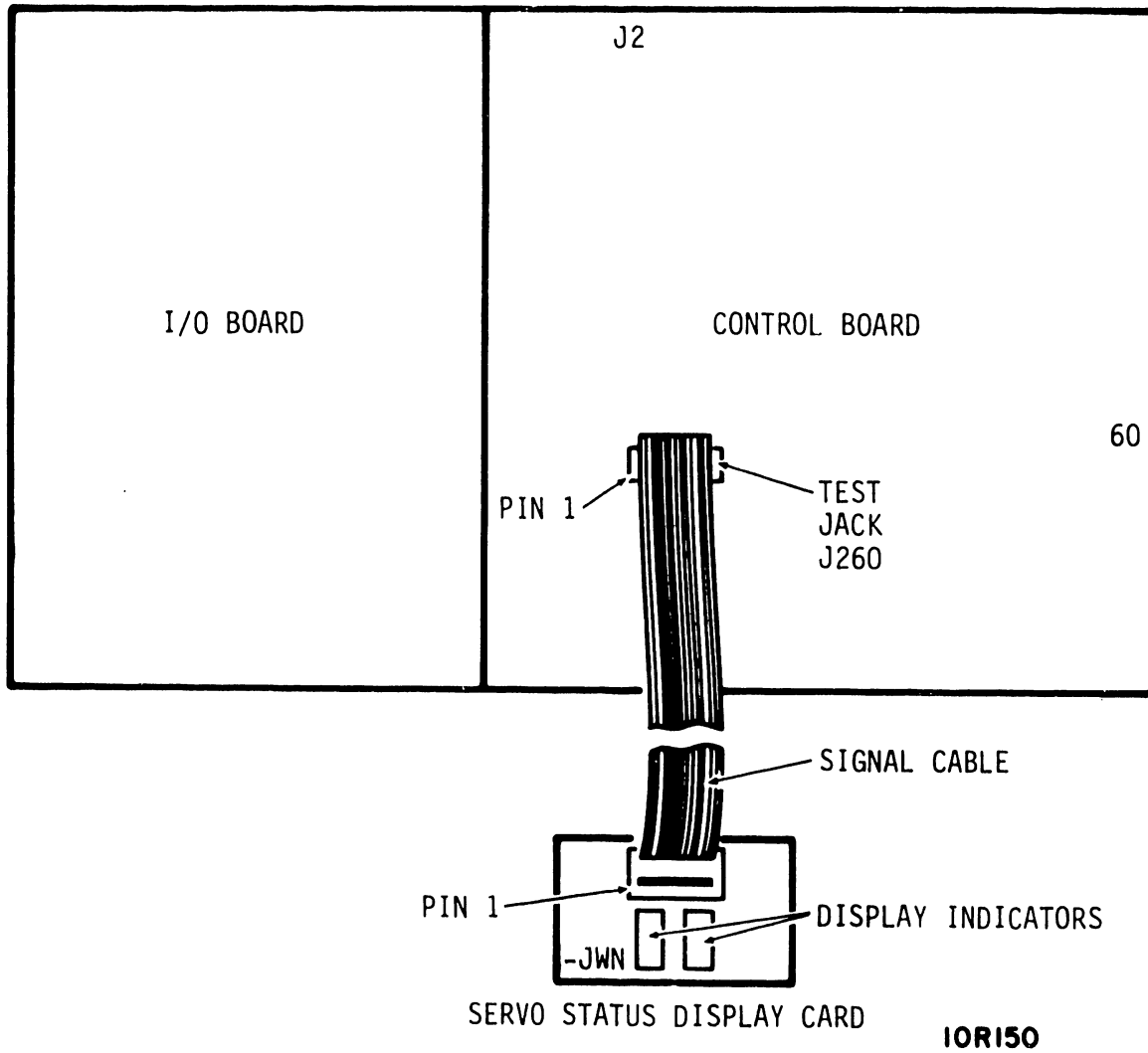


Figure 3-2. Servo Status Display Card Installation

When an operation is in progress, the status is continually changing. Most codes flash on and off very rapidly and are not recognizable. Others will remain for several seconds.

If an operation is successful the display shows the upper eight bits of the destination cylinder address. For example: after a power on or seek to cylinder 0 the display shows 00, after a seek to cylinder 822 the display shows CD. The destination is displayed until another seek is initiated or an error occurs.

If an error occurs, the status indicates the type of error and where in the sequence the error occurred. The error code will remain active until the proper action is taken to reset it (depends on nature of error).

It is possible for an error code to be the same as the desired destination address. Therefore, unless it is obvious from other indications that an error has occurred, always check the On Cylinder signal. If On Cylinder is active the seek was successfully completed.

TABLE 3-1. STATUS CODE SUMMARY

Status Code	Description
	<u>Normal Motor Stop</u>
01	Unloading Heads
02	Stopping Motor
03	Motor Stopped and Door Unlocked

Table Continued on Next Page

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	<u>Normal Motor Start</u>
04	Data Pack Not In Place
05	Door Locked When It Should Be Unlocked
06	Can't Lock Door
07	Heads Not Unloaded
08	Motor Start In Progress
09	Speed OK Too Soon
0A	Too Long To Get Up To Speed Retry
0B	Too Long To Get Up To Speed (Sensor Fault)
0C	Too Many Startup Failures (No Sensor Fault)
0D	Too Many Startup Failures (Sensor Fault)
0E	Motor Speed Too High
0F	Motor Speed Too Low
10	Speed Loss Recovery With Seek Error
	<u>Motor Start During Recovery From Speed Drop</u>
11	Unloading Heads
12	Stopping Motor
14	Data Pack Not In Place
Table Continued on Next Page	

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
<u>Motor Start During Recovery From Speed Drop (Contd)</u>	
15	Door Locked When It Should Be Unlocked
16	Can't Lock Door
17	Heads Not Loaded
18	Motor Start In Progress
19	Speed OK Too Soon
1A	Too Long To Get Up To Speed Retry
1B	Too Long To Get Up To Speed (Sensor Fault)
1C	Too Many Startup Failures (No Sensor Fault)
1D	Too Many Startup Failures (Sensor Fault)
1E	Motor Speed Too High
1F	Motor Speed Too Low
<u>Normal Load</u>	
20	Demodulator OK With Heads Unloaded
21	Heads Loaded Before Load Begins
22	Fault After Power Amplifier Driver Enabled
23	Heads Loaded Timeout
24	Demodulator OK Too Soon
Table Continued on Next Page	

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	<u>Normal Load (Contd)</u>
25	Demodulator OK Too Late
26	Cylinder Pulse Timeout
27	Fault After Load Complete
28	Code 22 And Too Many Retries
29	Code 23 And Too Many Retries
2A	Code 24 And Too Many Retries
2B	Code 25 And Too Many Retries
2C	Code 26 And Too Many Retries
2D	Code 27 And Too Many Retries
	<u>Normal RTZ</u>
30	Can't Move In From Outer Guardband
31	Lost Demodulator Active Before Turnaround
32	Can't Stop During Backup
33	Timeout During RTZ
34	Backup Into Outer Guardband
35	Turnaround
Table Continued on Next Page	

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
<u>Normal RTZ (Contd)</u>	
36	Out Of Guardband Too Soon
37	Can't Find Cylinder Pulse At Track -1
38	Find Fine Enable
39	Settle In On Track 0
<u>Normal Guard Bands</u>	
40	Inner Guardband Detected During Normal Seek
41	Inner Guardband Detected During On Cylinder Routine
42	Inner Guardband Detected While On Cylinder
43	Outer Guardband Detected During Normal Seek
44	Outer Guardband Detected During On Cylinder Routine
45	Outer Guardband Detected While On Cylinder
<u>Normal Seek Timeout</u>	
46	Seek Timeout
<u>(Normal) Can't Stop On Track During On Cylinder Routine</u>	
47	Too Long To Get On Cylinder Sense
48	Demodulator Active Lost During On Cylinder Routine
49	Too Many Cylinder Pulses During Settle In
4A	Too Many On Cylinder Dropouts
Table Continued on Next Page	

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	<u>Normal On Track</u>
4B	Off Cylinder
4C	Lost Demodulator Active While On Cylinder
4E	Voltage Fault While On Cylinder
	<u>(Normal) Illegal Cylinder Address Greater Than 822</u>
4D	Illegal Cylinder Address
	<u>Reset Dummy RTZ Mode Canceled</u>
50	Recovery From Low Vcc Reset
51	Recovery From MPU Hang Reset.
52	Recovered From Low Vcc Reset And Subsequent Speed Loss
53	Recovered From MPU Hang Subsequent Speed Loss
5C	Fan Fault
5D	First Seek Fault
5E	Demodulator OK After Unload
5F	PIA Test Failure
80	Fault Before Seek Begins
90	Recovered From Speed Loss
Table Continued on Next Page	

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	<u>Load And Fault Detected Before Seek Error Was Set</u>
A0	Demodulator OK With Heads Unloaded
A1	Heads Loaded Before Load Begins
A2	Fault After Power Amplifier Driver Enabled
A3	Heads Loaded Timeout
A4	Demodulator OK Too Soon
A5	Demodulator OK Too Late
A6	Cylinder Pulse Timeout
A7	Fault After Load Complete
A8	Code 22 And Too Many Retries
A9	Code 23 And Too Many Retries
AA	Code 24 And Too Many Retries
AB	Code 25 And Too Many Retries
AC	Code 26 And Too Many Retries
AD	Code 27 And Too Many Retries
Table Continued on Next Page	

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	<u>RTZ And Fault Detected Before Seek Error Was Set</u>
B0	Can't Move In From Outer Guardband
B1	Lost Demodulator OK Before Turnaround
B2	Can't Stop During Backup
B3	Timeout During RTZ
B4	Backup Into Outer Guardband
B5	Turnaround
B6	Out Of Guardband Too Soon
B7	Can't Find Cylinder Pulse At Track -1
B8	Find Fine Enable
B9	Settle In On Track 0
	<u>Guard Bands And Fault Detected Before Seek Error Was Set</u>
C0	Inner Guardband Detected During Normal Seek
C1	Inner Guardband Detected During On Cylinder Routine
C2	Inner Guardband Detected While On Cylinder
C3	Outer Guardband Detected During Normal Seek
C4	Outer Guardband Detected During On Cylinder Routine
C5	Outer Guardband Detected While On Cylinder
Table Continued on Next Page	

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	<u>Seek Timeout And Fault Detected Before Seek Error Was Set</u>
C6	Seek Timeout
	<u>Can't Stop On Track During On Cylinder Routine And Fault Detected Before Seek Error Was Set</u>
C7	Too Long To Get On Cylinder Sense
C8	Demodulator Active Lost During On Cylinder Routine
C9	Too Many Cylinder Pulses During Settle In
CA	Too Many On Cylinder Dropouts
	<u>On Track And Fault Detected Before Seek Error Was Set</u>
CB	Off Cylinder
CC	Lost Demodulator Active While On Cylinder
CE	Voltage Fault While On Cylinder
	<u>Illegal Cylinder Address Greater Than 822 And Fault Detected Before Seek Error Was Set</u>
CD	Illegal Cylinder Address
	<u>Reset Dummy RTZ Mode Active</u>
D0	Recovery From Low Vcc Reset
D1	Recovery From MPU Hang Reset
D2	Recovered From Low Vcc Reset And Subsequent Speed Loss
D3	Recovered From MPU Hang Subsequent Speed Loss
	<u>MPU Power On Test</u>
FF	MPU Failed Power On Test

TABLE 3-2. STATUS CODE DEFINITIONS

Code	Description
01	<p><u>Title:</u> Unloading Heads</p> <p><u>DESCRIPTION:</u> The MPU sets code 01 while it is unloading the heads. This status lasts approximately .2 seconds under normal conditions. If the heads unload, the motor stop sequence begins and the status changes to 02. If the MPU does not detect the heads unloaded condition the status remains at 01 and the motor continues to run.</p> <p><u>PROBABLE CAUSES:</u> Problem in servo retract loop. Heads loaded switch circuit giving wrong indication.</p> <p><u>ACTIONS:</u></p> <ol style="list-style-type: none"> 1. If heads are unloaded: <ol style="list-style-type: none"> a. Check heads loaded switch and associated wiring. b. Replace _PEX board (proc 5304). 2. If heads are not unloaded: <ol style="list-style-type: none"> a. Check coil for continuity and shorts. b. Check power amplifier driver outputs from _PEX board (proc 4206). If output is abnormal, replace _PEX board (proc 5304). c. Replace _PDX board (proc 5307). d. Replace carriage and coil assembly (proc 5205, 5206).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
02	<p><u>Title:</u> Stopping Motor</p> <p><u>DESCRIPTION:</u> The MPU sets this status during the braking period. When the motor is stopped (normally requires 30 seconds), the status changes to 03. If the MPU does not detect a motor stop it leaves the status at 02.</p> <p><u>PROBABLE CAUSES:</u> Indicates a problem with the motor control circuits or a brake failure.</p> <p><u>ACTIONS:</u></p> <ol style="list-style-type: none"> 1. If motor is running, replace _PMX board (proc 5308). 2. If motor is not running, check for the presence of motor sense pulses at E219-2 on the _PMX board. <ol style="list-style-type: none"> a. If pulses are present, check wiring and if that is OK, replace _PMX board (proc 5308). b. If pulses are not present, replace _PEX board (proc 5304).
03	<p><u>Title:</u> Motor Stopped And Door Unlocked</p> <p><u>DESCRIPTION:</u> The MPU sets code 02 when it detects that the motor is stopped. This code will be displayed following a normal stop sequence. Code will remain at 03 until microprocessor sees START switch turned on and sequence hold from I/O board.</p> <p><u>PROBABLE CAUSES:</u> N.A.</p> <p><u>ACTIONS:</u> N.A.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
04	<p><u>Title:</u> Data Pack Not In Place</p> <p><u>DESCRIPTION:</u> The MPU sets this status prior to starting the motor if it detects that the pack is not in place. This condition stops the power on sequence.</p> <p><u>PROBABLE CAUSES:</u> Data pack not inserted or pack in place switch is bad.</p> <p><u>ACTIONS:</u></p> <ol style="list-style-type: none"> 1. Check that pack is inserted. 2. If pack is in place, check wiring to switch. If wiring is OK, replace switch (proc 5214).
05	<p><u>Title:</u> Door Locked When It Should Be Unlocked</p> <p><u>DESCRIPTION:</u> The MPU uses this status in conjunction with code 06 to verify door lock operation. Prior to starting the motor, the MPU inactivates the Lock Door signal which should deenergize the solenoid. If the switch still indicates a door locked condition, code 05 is displayed and the power on sequence stops. No other error indications appear.</p> <p><u>PROBABLE CAUSES:</u> Defective or stuck solenoid. Door lock signals not generated properly.</p> <p><u>ACTIONS:</u></p> <ol style="list-style-type: none"> 1. Check that -Lock Door and +Disk Stopped signals are inactive. <ol style="list-style-type: none"> a. If they are active, replace _PEX board (proc 5304). b. If they are inactive, replace solenoid (proc 5215).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
06	<p><u>Title:</u> Can't Lock Door</p> <p><u>DESCRIPTION:</u> After checking the unlock function (see code 05) the MPU checks tries to lock the door. If the switch indicates that the door is unlocked, code 06 is displayed and the power on sequence stops.</p> <p><u>PROBABLE CAUSES:</u> Defective solenoid or door lock signal not generated.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check that -Lock Door and +Disk Stopped are active. <ol style="list-style-type: none"> a. If they are active, replace _PEX board (proc 5305). b. If they are inactive, replace solenoid (proc 5215).
07	<p><u>Title:</u> Heads Not Unloaded</p> <p><u>DESCRIPTION:</u> Before starting the motor, the MPU checks to ensure the heads are retracted. If the heads loaded switch indicates that the heads are not retracted, code 07 is displayed and the power on sequence stops.</p> <p><u>PROBABLE CAUSES:</u> Problem in servo retract loop. Heads loaded switch circuit giving wrong indication.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. If heads are unloaded: <ol style="list-style-type: none"> a. Check heads loaded switch and associated wiring. b. Replace _PEX board (proc 5304).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>2. If heads are loaded:</p> <ul style="list-style-type: none"> a. Check power amplifier driver outputs from _PEX (proc 4206). If output is abnormal, replace _PEX board (proc 5304). b. Replace _PDX board (proc 5307). c. Replace carriage and coil assembly (proc 5205, 5206).
08	<p><u>Title:</u> Motor Start In Progress</p> <p><u>DESCRIPTION:</u> Indicates that the interlocks are OK. This will start the motor and purge the data pack. Code 08 is displayed (for approximately 30 seconds) until either an error occurs or the heads successfully reach cylinder 0 and code 00 appears.</p> <p><u>PROBABLE CAUSES:</u> N.A.</p> <p><u>ACTIONS:</u> N.A.</p>
09	<p><u>Title:</u> Speed OK Too Soon</p> <p><u>DESCRIPTION:</u> Indicates that, during the power on sequence, it took less than 3 seconds for the motor to get up to speed. This condition stops the power on sequence.</p> <p><u>PROBABLE CAUSES:</u> A pack is not in place or faulty speed detection circuits.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check that pack is in place. 2. Replace _PMX board (proc 5308). 3. Replace _PEX board (proc 5304).
OA	<p><u>Title:</u> Too Long To Get Up To Speed Retry</p> <p><u>DESCRIPTION:</u> Indicates that drive is performing a re-try after the motor did not come up to speed within 15 seconds of starting. OA is displayed only during the stop routine after a start failure. Display changes back to O8 during the start routine. If after three tries the motor does not come up to speed, the motor stops and display changes to OC.</p> <p><u>PROBABLE CAUSES:</u> See code OC.</p> <p><u>ACTIONS:</u> See code OC</p>
OB	<p><u>Title:</u> Too Long To Get Up To Speed (Sensor Fault)</p> <p><u>DESCRIPTION:</u> Indicates that the drive is performing a re-try after the motor did not come up to speed and a sensor fault was detected. OA is displayed only during the stop routine after a start failure. The display changes back to O8 during the start routine. If after three tries the motor does not come up to speed, the motor stops and display changes to OC.</p> <p><u>PROBABLE CAUSES:</u> See code OD</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>ACTIONS:</u> See Code OD</p>
OC	<p><u>Title:</u> Too Many Startup Failures (No Sensor Fault)</p> <p><u>DESCRIPTION:</u> Indicates that the drive has failed three times to bring the motor up to speed (see code OA). Setting START Switch to Off and back to On causes three more attempts.</p> <p><u>PROBABLE CAUSES:</u> Power supply, motor control circuits, or motor.</p> <p><u>ACTIONS:</u></p> <ol style="list-style-type: none"> 1. Check J40 to J37, P24 to J24, and J39 to motor wiring. 2. Check -Door Locked #2 signal on _PMX board. If signal is inactive: <ol style="list-style-type: none"> a. Check door locked switches. b. Check _PEX board (signal feeds through _PEX). 3. Check +40 volts from power supply (proc 4101). 4. Replace _PMX board (proc 5308). 5. Replace motor & cable assembly (proc 5209).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
OD	<p><u>Title:</u> Too Many Startup Failures (Sensor Fault)</p> <p><u>DESCRIPTION:</u> Indicates that the drive has failed three times to bring the motor up to speed (see code OA) and a sensor fault has been detected (see code OB). Setting START Switch to Off and back to On causes three more attempts.</p> <p><u>PROBABLE CAUSES:</u> Motor or motor control board</p> <p><u>ACTIONS:</u></p> <ol style="list-style-type: none"> 1. Replace _PMX board (proc 5308). 2. Replace motor & cable assembly (proc 5209).
OE OF	<p><u>Title:</u> Motor Speed Too High</p> <p><u>Title:</u> Motor Speed Too Low</p> <p><u>DESCRIPTION:</u> Indicates that the motor speed is too high (OE) or too low (OF). The MPU performs this check after it receives the Up to Speed signal from the _PMX board. When this condition exists, the drive keeps the motor running while continuing, indefinitely, to check motor speed. The heads do not load.</p> <p><u>PROBABLE CAUSES:</u> Problem with motor speed control or speed detection circuits.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>ACTIONS:</u></p> <ol style="list-style-type: none"> 1. Check motor sensor signal at TP E836-7 on _PEX board. <ol style="list-style-type: none"> a. If signal is present and is a 120 Hz square wave, replace _PEX board (proc 5304). b. If signal is absent or not a 120 Hz square wave, replace _PMX board (proc 5308). 2. Replace motor & cable assembly (proc 5209).
10	<p><u>Title:</u> Speed Loss Recovery With Seek Error</p> <p><u>DESCRIPTION:</u> Indicates that drive has recovered from a speed loss and that seek error occurred during the recovery sequence. The heads are on cylinder 0 and Seek Error is active. On Cylinder and Ready signals will go active when the drive receives an RTZ command.</p> <p><u>PROBABLE CAUSES:</u> Motor failure, motor cable or connector, motor control board, or power supply.</p> <p><u>ACTIONS</u></p> <p>If more failures occur:</p> <ol style="list-style-type: none"> 1. Replace power supply (proc 5203). 2. Replace motor & cable assembly (proc 5209). 3. Replace _PMX board (proc 5308).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
<p>11 thru 1F</p>	<p><u>Title:</u> Motor Start During Recovery From Speed Drop.</p> <p><u>DESCRIPTION:</u> Same as codes 01 through 0F but occur during recovery from a loss of speed. The codes covered in this discussion are listed below with the corresponding code (without speed drop) given in parentheses.</p> <p style="padding-left: 40px;">11 (01) 12 (02) 14 (04) 15 (05) 16 (06) 17 (07) 18 (08) 19 (09) 1A (0A) 1B (0B) 1C (0C) 1D (0D) 1E (0E) 1F (0F)</p> <p><u>PROBABLE CAUSES:</u> See codes 01 through 0F.</p> <p><u>ACTIONS:</u> See Codes 01 through 0F.</p>
<p>20</p>	<p><u>Title:</u> Demodulator OK With Heads Unloaded</p> <p><u>DESCRIPTION:</u> Indicates that the drive detected Demodulator OK active before the heads were loaded and tri-bits were present. This error is detected during a heads load sequence. When the drive displays code 20, the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active (first seek only). ● Seek Error and Seek End lines go active (except during first seek). ● Motor continues to run but heads remain unloaded.
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load.</p> <p><u>PROBABLE CAUSES:</u> Bad tribit decoder circuit</p> <p><u>ACTION</u></p> <p>1. Replace _PEX board (proc 5304).</p>
21	<p><u>Title:</u> Heads Loaded Before Load Begins</p> <p><u>DESCRIPTION:</u> Indicates that the heads loaded switch indicated a heads loaded condition before the heads moved forward from the retracted position. This error is detected during a load sequence. When the drive displays code 21, the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active (first seek only). ● Seek Error and Seek End lines go active (except during first seek). ● Motor continues to run but heads remain unloaded. <p>If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>PROBABLE CAUSES:</u> Defective heads loaded switch or foil short on _PEX board.</p> <p><u>ACTION</u></p> <ol style="list-style-type: none"> 1. Replace heads loaded switch (proc 5213). 2. Replace _PEX board (proc 5304).
22	<p><u>Title:</u> Fault After Power Amplifier Driver Enabled</p> <p><u>DESCRIPTION:</u> Indicates that the drive detected a fault condition after the Retract Relay latch was set. Setting the Retract Relay latch enables the drive circuit input to the power amplifier. The purpose of a check at this time is to detect a voltage fault before enabling the load gate and moving the heads forward. When the drive displays code 22, the following error indications also appear.</p> <ul style="list-style-type: none"> • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active. • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run but heads remain unloaded. <p>If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, a controller Fault Clear followed by another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 28 and the Fault Clear switch must be pressed to continue.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>PROBABLE CAUSES:</u> Voltage fault as a result of enabling power amplifier inputs. Extraneous fault, such as Read and Write, caused by I/O problem.</p> <p><u>ACTIONS</u></p> <p>Check LEDs for cause of fault condition.</p> <ol style="list-style-type: none"> 1. If voltage fault exists: <ol style="list-style-type: none"> a. Check \pm 24 volts (proc 4101). If voltages are abnormal, go to \pm24 Volt Load Check (TSP3). b. Check driver outputs from <u>PEX</u> board (proc 5304). c. Replace <u>PDX</u> board (proc 5307). 2. If a fault other than voltage exists: <ol style="list-style-type: none"> a. Check I/O cabling. b. Replace <u>PEX</u> board (proc 5304).
23	<p><u>Title:</u> Heads Loaded Timeout</p> <p><u>DESCRIPTION:</u> Indicates that the heads loaded switch did not transfer within 60 milliseconds of when the load gate was enabled. When the drive displays code 23, the following error indications also appear.</p> <ul style="list-style-type: none"> • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<ul style="list-style-type: none"> ● Seek Error and Seek End lines go active (except during first seek). ● Heads unload but motor continues to run. <p>If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 29 (A9) and the Fault Clear switch must be pressed to continue.</p> <p>PROBABLE CAUSES: Electrical or mechanical problem in load/retract servo loop or bad heads loaded switch.</p> <p><u>ACTION</u></p> <ol style="list-style-type: none"> 1. If heads move out and then retract, replace heads loaded switch (proc 5213). 2. If heads do not move out: <ol style="list-style-type: none"> a. Check drive outputs from _PEX board (proc 5304). b. Check coil for continuity and shorts. c. Replace _PDX board (proc 5307). d. Replace carriage and coil assembly (proc 5205, 5206).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
24	<p><u>Title:</u> Demodulator OK Too Soon</p> <p><u>DESCRIPTION:</u> Indicates that, during a load sequence, the Demodulator OK signal went active within 160 milliseconds after the heads started moving forward. When the drive displays code 24, the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active (first seek only). ● Seek Error and Seek End lines go active (except during first seek). ● Heads unload but motor continues to run. <p>If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 29 and the Fault Clear switch must be pressed to continue.</p> <p><u>PROBABLE CAUSES:</u> Bad tribit decoder circuit, noisy servo preamp, or defective servo head.</p> <p><u>ACTION:</u></p> <ol style="list-style-type: none"> 1. Replace _PEX board (proc 5304). 2. Replace _UUN board (proc 5306). 3. Replace servo head (proc 5212).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
25	<p><u>Title:</u> Demodulator OK Too Late</p> <p><u>DESCRIPTION:</u> Indicates that, during a load sequence, Demodulator OK did not go active within 360 milliseconds after the heads started moving forward. When the drive displays code 25, the following error indications also appear.</p> <ul style="list-style-type: none"> • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Heads unload but motor continues to run. <p>If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 29 and the Fault Clear switch must be pressed to continue.</p> <p><u>PROBABLE CAUSES:</u> Bad tribit detection circuit or bad servo disk.</p> <p><u>ACTION</u></p> <ol style="list-style-type: none"> 1. Check cabling between servo head and _UUN board. 2. Check cabling between _UUN and _PEX boards.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>3. Check servo surface (proc 4207). If results are abnormal, check servo head and then replace pack.</p> <p>4. Replace _UUN board (proc 5306).</p> <p>5. Replace _PEX board (proc 5304).</p> <p>6. Remove and inspect servo head for visible damage and replace if necessary (proc 5212). If servo head is replaced, inspect all other heads for possible damage.</p>
26	<p><u>Title:</u> Cylinder Pulse Timeout</p> <p><u>DESCRIPTION:</u> Indicates that, during a load sequence, the MPU did not detect 100 cylinder pulses within 360 milliseconds after Demodulator OK went active. When the drive displays code 26, the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active (first seek only). ● Seek Error and Seek End lines go active (except during first seek).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
26	<p><u>Title:</u> Cylinder Pulse Timeout</p> <ul style="list-style-type: none"> ● Heads unload but motor continues to run. <p>If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 2C and the Fault Clear switch must be pressed to continue.</p> <p><u>PROBABLE CAUSES:</u> Demodulator failure, bad servo disk or cylinder pulse detection circuits.</p> <p><u>ACTION</u></p> <ol style="list-style-type: none"> 1. Replace _PEX board (proc 5304). 2. Check servo surface (proc 4207). If results are abnormal check servo head and then replace pack. 3. Check cabling between servo head and _UUN board. 4. Check cabling between _UUN and _PEX boards. 5. Replace _UUN board (proc 5306). 6. Replace servo head (proc 5212).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
27	<p><u>Title:</u> Fault After Load Complete</p> <p><u>DESCRIPTION:</u> Indicates that, during a load sequence, the MPU detected a fault just prior to the time that the heads turn around and move back into the guard-band. When the drive displays code 27, the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active (first seek only). ● Seek Error and Seek End lines go active (except during first seek). ● Heads unload but motor continues to run. <p>If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 2D and the Fault Clear switch must be pressed to continue.</p> <p><u>PROBABLE CAUSES:</u> Voltage fault due to defective voltage regulator, power supply, power amplifier, or voice coil. Extraneous fault, such as Read and Write, caused by I/O problem.</p> <p><u>ACTIONS</u></p> <p>Check LEDs for cause of fault condition.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>1. If voltage fault exists:</p> <ul style="list-style-type: none"> a. Check ± 24 volts (proc 4101). If voltages are abnormal, go to (TSP3) ± 24 Volt Load Check. b. Check coil for continuity and shorts. c. Replace _PDX board (proc 5307). d. Replace _PEX board (proc 5304). e. Replace voice coil (proc 5205). <p>2. If a fault other than voltage exists:</p> <ul style="list-style-type: none"> a. Check I/O cabling. b. Replace _EBN/_EDN board (proc 5303).
<p>28 thru 2D</p>	<p><u>Title:</u> Error Conditions With Too Many Retries.</p> <p><u>DESCRIPTION:</u> Indicates that more than five RTZ error recovery attempts were made following the associated error (codes 22 through 27). After five attempts, the MPU sets one of the codes 28 through 2D and prevents further retries. Pressing the Fault Clear switch clears the error and allows five more retries. The codes covered in this discussion are listed below with the corresponding code (without too many retries) given in parentheses.</p> <p>28 (22) 29 (23) 2A (24) 2B (25) 2C (26) 2D (27)</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>PROBABLE CAUSES:</u> See codes 22 through 2D.</p> <p><u>ACTIONS:</u> See codes 22 through 2D.</p>
30	<p><u>Title:</u> Can't Move In From Outer Guardband</p> <p><u>DESCRIPTION:</u> Indicates, during a load or RTZ, that heads were moving in too fast to allow a turnaround in the data zone. Attempting a turnaround could result in the heads moving completely through the data zone, resulting in loss of servo control. When the drive displays code 30, the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active (first seek only). ● Seek Error and Seek End lines go active (except during first seek). ● Heads unload but motor continues to run. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, the drive automatically performs one retry. If the retry fails it is necessary to command another RTZ to clear the seek error and initiate another attempt.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>PROBABLE CAUSES:</u> Problem with velocity circuits.</p> <p><u>ACTIONS</u></p> <p>1. Initiate RTZ, if error repeats, replace _PEX board (proc 5304).</p>
31	<p><u>Title:</u> Lost Demodulator Active Before Turnaround</p> <p><u>DESCRIPTION:</u> Indicates that during retract portion of RTZ, Demodulator Active went inactive. This indicates that the heads may have moved back through the outer guardband to the outer surface of the disk, without generating outer guardband pulses. When the drive displays code 31, the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active (first seek only). ● Seek Error and Seek End lines go active (except during first seek). ● Heads unload but motor continues to run. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, the drive automatically performs one retry. If the retry fails it is necessary to command another RTZ to clear the seek error and initiate another attempt.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>PROBABLE CAUSES:</u> Bad servo disk, loose connection or failure that causes load/retract loop to lose feedback.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check cabling between servo head _UUN board. 2. Check cabling between _UUN board and _PEX board. 3. Check servo surface (proc 4207). If results are abnormal: <ol style="list-style-type: none"> a. Replace pack. b. Replace servo head (proc 5212). 4. Replace _PEX board (proc 5304). 5. Replace _UUN board (proc 5306).
32	<p><u>Title:</u> Can't Stop During Backup</p> <p><u>DESCRIPTION:</u> Indicates that during backup portion of a load or RTZ seek, the heads were moving too fast to allow a successful turnaround. When the drive displays code 32, the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active (first seek only). ● Seek Error and Seek End lines go active (except during first seek). ● Heads unload but motor continues to run.
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, the drive automatically performs one retry. If the retry fails it is necessary to command another RTZ to clear the seek error and initiate another attempt.</p> <p><u>PROBABLE CAUSES:</u> Problem with velocity circuits</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check coil for shorts. 2. Check position signal (proc 4207). 3. Initiate RTZ, if error repeats, replace _PEX board (proc 5304). 4. Replace _PDX board (proc 5307).
33	<p><u>Title:</u> Timeout During RTZ</p> <p><u>DESCRIPTION:</u> Indicates that during the backup portion of a load or RTZ, too much time elapsed before the heads reached the outer guardband. When the drive displays code 33, the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active (first seek only).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<ul style="list-style-type: none"> • Seek Error and Seek End lines go active (except during first seek). • Heads unload but motor continues to run. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, the drive automatically performs one retry. If the retry fails it is necessary to command another RTZ to clear the seek error and initiate another load.</p> <p><u>PROBABLE CAUSES:</u> Failure in velocity circuits, bad power amplifier or power amplifier driver circuits.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check coil for continuity and shorts. 2. Replace _PDX board (proc 5307). 3. Replace _PEX board (proc 5304). 4. Inspect and clean rails and carriage bearings (proc 5208).
34	<p><u>Title:</u> Backup Into Outer Guardband</p> <p><u>DESCRIPTION:</u> Code 34 is set when the outer guardband is detected during the backup phase of a load or RTZ seek. It normally remains set only until turnaround, when the code changes to 35. If the display stays at 34, it indicates either a timeout (too long to count 6 cylinder pulses) or Demodulator OK inactive error. The following error indications appear in addition to code 34.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Heads unload but motor continues to run. <p>If the error occurs during an RTZ:</p> <ul style="list-style-type: none"> • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another load.</p> <p><u>PROBABLE CAUSES:</u> Bad tribit decoder circuit or servo disk.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check servo surface (proc 4207). If results are abnormal replace pack. 2. Check for loose cable between servo head and _UUN board.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>3. Replace _PEX board (proc 5304).</p> <p>4. Inspect and clean rails and carriage bearings (proc 5208).</p>
35	<p><u>Title:</u> Turnaround</p> <p><u>DESCRIPTION:</u> Code 35 is set at the turnaround point following the backup phase of a load or RTZ seek. This is the point where six cylinder pulses have been counted, reverse is cleared, and forward is set. Code 35 normally remains set only until the heads move forward four tracks thus bringing the heads to track -1 (preceding cylinder 0) and changing the code to 37. If the display stays at 35, it indicates either a timeout (too long to count 4 cylinder pulses) or Demodulator OK inactive error. The following error indications appear in addition to code 35 Seek LED lights (first seek only).</p> <p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> ● First Seek LED lights. ● FAULT indicator lights and Fault line goes active (first seeks only). ● Heads unload but motor continues to run. <p>If the error occurs during an RTZ:</p> <ul style="list-style-type: none"> ● Seek Error and Seek End lines go active. ● Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another load.</p> <p><u>PROBABLE CAUSES:</u> Bad tribit decoder circuit or servo disk.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check servo surface (proc 4207). If results are abnormal replace pack. 2. Check for loose cable between servo head and _UUN board. 3. Replace _PEX board (proc 5304). 4. Inspect and clean rails and carriage bearings (proc 5208).
36	<p><u>Title:</u> Out Of Guardband Too Soon</p> <p><u>DESCRIPTION:</u> Indicates, during a load or RTZ, that the drive detected less than four cylinder pulses before the heads moved out of the outer guardband. When the drive displays code 36, the following error indications also appear.</p> <p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> ● First Seek LED lights. ● FAULT indicator lights and Fault line goes active (first seeks only). ● Heads unload but motor continues to run.
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurs during an RTZ:</p> <ul style="list-style-type: none"> ● Seek Error and Seek End lines go active. ● Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check for loose cable between servo head and _UUN board. 2. Check servo surface (proc 4207). If results are abnormal replace pack. 3. Replace _PEX board (proc 5304). 4. Inspect and clean rails and carriage bearings (proc 5208).
37	<p><u>Title:</u> Can't Find Cylinder Pulse At Track -1</p> <p><u>DESCRIPTION:</u> Indicates that, during a load or RTZ, either Demodulator OK went inactive or too much time elapsed while the drive was looking for track -1 (track preceding cylinder 0). When the drive displays code 37, the following error indications also appear.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> ● First Seek LED lights. ● FAULT indicator lights and Fault line goes active (first seeks only). ● Heads unload but motor continues to run. <p>If the error occurs during an RTZ:</p> <ul style="list-style-type: none"> ● Seek Error and Seek End lines go active. ● Motor continues to run. ● If error is due to Demodulator OK going inactive, the heads unload. If it is a timeout error, the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check servo surface (proc 4207). If results are abnormal replace pack. 2. Check for loose cable between servo head and _UUN board.
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>3. Replace _PEX board (proc 5304).</p> <p>4. Inspect and clean rails and carriage bearings (proc 5208).</p>
38	<p><u>Title:</u> Find Fine Enable</p> <p><u>DESCRIPTION:</u> Indicates that, during a load or RTZ, either Demodulator OK went inactive or too much time elapsed while the drive was waiting for Fine Enable to go active. When the drive displays code 38, the following error indications also appear.</p> <p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> ● First Seek LED lights. ● FAULT indicator lights and Fault line goes active (first seeks only). ● Heads unload but motor continues to run. <p>If the error occurs during an RTZ:</p> <ul style="list-style-type: none"> ● Seek Error and Seek End lines go active. ● Motor continues to run. ● If error is due to Demodulator OK going inactive, the heads unload. If it is a timeout error, the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>PROBABLE CAUSES:</u> Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check servo surface (proc 4207). If results are abnormal replace pack. 2. Check for loose cable between servo head and _UUN board. 3. Replace _PEX board (proc 5304). 4. Inspect and clean rails and carriage bearings (proc 5208).
39	<p><u>Title:</u> Settle In On Track 0</p> <p><u>DESCRIPTION:</u> Code 39 is set when the heads are within 1/2 track of cylinder 0. It normally remains set only until the heads are on cylinder and the display changes to 0. If the display stays at 39, it indicates that either Demodulator OK went inactive or too much time elapsed before on cylinder went active. The following error indications appear in conjunction with code 39 (B9).</p> <p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> ● First Seek LED lights. ● FAULT indicator lights and Fault line goes active (first seeks only). ● Heads unload but motor continues to run.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurs during an RTZ:</p> <ul style="list-style-type: none"> ● Seek Error and Seek End lines go active. ● Motor continues to run. ● If error is due to Demodulator OK going inactive, the heads unload. If it is a timeout error, the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another load and seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check servo surface (proc 4207). If results are abnormal replace pack. 2. Check for loose cable between servo head and _UUN board. 3. Replace _PEX board (proc 5304). 4. Inspect and clean rails and carriage bearings (proc 5208).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
40	<p><u>Title:</u> Inner Guardband Detected During Normal Seek</p> <p><u>DESCRIPTION:</u> Indicates that guardband pulses were detected while the heads were moving over the data zone. When the drive displays code 40, the following error indications also appear:</p> <ul style="list-style-type: none"> ● Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. ● Seek Error and Seek End lines go active. <p>An RTZ command clears the seek error and initiates a seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Cylinder pulses missed or miscounted during seek. Could be caused by bad cylinder pulse detection circuits, pack with defects, bad tribit decoder circuits, or electrical noise generated by nearby equipment.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Look for bad tracks on servo surface (proc 4207). If results are abnormal, replace pack. 2. Replace _PEX board (proc 5304).
41	<p><u>Title:</u> Inner Guardband Detected During On Cylinder Routine</p> <p><u>DESCRIPTION:</u> Indicates guardband pulses were detected while the heads were settling into the on cylinder position. When the drive displays code 41, the following error indications also appear:</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> ● First Seek LED lights ● FAULT indicator lights and Fault line goes active (first seeks only). ● Heads unload but motor continues to run. <p>If the error occurs during an RTZ or normal seek:</p> <ul style="list-style-type: none"> ● Seek Error and Seek End lines go active. ● Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates a seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Look for bad tracks on servo surface (proc 4207). If results are abnormal, replace pack. 2. Replace _PEX board (proc 5304).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
42	<p><u>Title:</u> Inner Guardband Detected While On Cylinder</p> <p><u>DESCRIPTION:</u> Indicates that inner guardband pulses were detected while the heads were on cylinder. When the drive displays code 42, the following error indications also appear:</p> <ul style="list-style-type: none"> • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error and Seek End lines go active. <p>An RTZ command clears the seek error and initiates a seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Look for bad tracks on servo surface (proc 4207). If results are abnormal, replace pack. 2. Replace _PEX board (proc 5304).
43	<p><u>Title:</u> Outer Guardband Detected During Normal Seek</p> <p><u>DESCRIPTION:</u> Indicates that guardband pulses were detected while the heads were moving over the data zone. When the drive displays code 43, the following error indications also appear:</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<ul style="list-style-type: none"> • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error and Seek End lines go active. <p>An RTZ command clears the seek error and initiates a seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Cylinder pulses missed or miscounted during seek. Could be caused by bad cylinder pulse detection circuits or by electrical noise generated by nearby equipment.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Look for bad tracks on servo surface (proc 4207). If results are abnormal, replace pack. 2. Replace _PEX board (proc 5304).
44	<p><u>Title:</u> Outer Guardband Detected During On Cylinder Routine</p> <p><u>DESCRIPTION:</u> Indicates guardband pulses were detected while the heads were settling into the on cylinder position. When the drive displays code 44, the following error indications also appear:</p> <p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Heads unload but motor continues to run.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurs during an RTZ or normal seek:</p> <ul style="list-style-type: none"> ● Seek Error and Seek End lines go active. ● Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates a seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Look for bad tracks on servo surface (proc 4207). If results are abnormal, replace pack. 2. Replace _PEX board (proc 5304).
45	<p><u>Title:</u> Outer Guardband Detected While On Cylinder</p> <p><u>DESCRIPTION:</u> Indicates that inner guardband pulses were detected while the heads were on cylinder. When the drive displays code 45, the following error indications also appear:</p> <ul style="list-style-type: none"> ● Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces.
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<ul style="list-style-type: none"> ● Seek Error goes active. <p>An RTZ command clears the seek error and initiates a seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Look for bad tracks on servo surface (proc 4207). If results are abnormal, replace pack. 2. Replace _PEX board (proc 5304).
46	<p><u>Title:</u> Seek Timeout</p> <p><u>DESCRIPTION:</u> Indicates that during a normal seek the drive took longer than 60 milliseconds to reach on cylinder. When the drive displays code 46, the following error indications also appear.</p> <ul style="list-style-type: none"> ● Seek error and Seek End lines go active. ● Motor continues to run but servo system is disabled and the heads, although loaded, drift freely over the disk surfaces. <p>An RTZ clears the seek error and initiates a seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Problem with voice coil or velocity circuits.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check coil for continuity and shorts. 2. Replace _PEX board (proc 5304). 3. Replace _PDX board (proc 5307).
47	<p><u>Title:</u> Too Long to Get On Cylinder Sense</p> <p><u>DESCRIPTION:</u> Indicates that too much time elapsed from Fine Enable going active to On cylinder going active. When the drive displays code 47, the following error indications also appear:</p> <p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> • First Seek LED lights and Seek Error line goes active. • FAULT indicator lights and Fault line goes active (first seeks only). • Heads unload but motor continues to run. <p>If the error occurs during an RTZ or normal seek:</p> <ul style="list-style-type: none"> • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates a seek to cylinder 0.</p>

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>PROBABLE CAUSES:</u> On cylinder sense circuits not functioning or a mechanical problem that slows the carriage as it approaches on cylinder.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Use servo test mode (proc 4207) to check carriage movement. 2. Replace _PEX board (proc 5304).
48	<p><u>Title:</u> Demodulator Active Lost During On Cylinder Routine</p> <p><u>DESCRIPTION:</u> Indicates that Demodulator OK went inactive as the heads approached on cylinder. When the drive displays code 48, the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active (first seek only). ● Seek Error and Seek End lines go active (except for first seek). ● Heads unload but motor continues to run. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another load and seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Bad servo disk, bad tribit decoder circuits, loose cabling in feedback loop.</p>
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>ACTIONS</u></p> <p>Perform sequential forward seeks with read.</p> <ol style="list-style-type: none"> 1. If error occurs at same cylinder each time, replace pack. 2. If error occurs at random locations: <ol style="list-style-type: none"> a. Check for loose cable connections between servo head and _UUN board. b. Check for loose cable connections between _UUN board and _PEX boards. 3. If problem still exists, replace _PEX board (proc 5304).
49	<p><u>Title:</u> Too Many Cylinder Pulses During Settle In</p> <p><u>DESCRIPTION:</u> Indicates that three or more cylinder pulses were detected during settle in thus indicating excessive overshoot. Excessive overshoot can result in the heads settling on the wrong cylinder. When the drive displays code 49, the following error indications also appear:</p> <p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> ● First Seek LED lights. ● FAULT indicator lights and Fault line goes active (first seeks only). ● Heads unload but motor continues to run.
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurs during an RTZ or normal seek:</p> <ul style="list-style-type: none"> ● Seek Error and Seek End lines go active. ● Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another load and seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Velocity or cylinder pulse detection circuits.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Look for bad tracks on servo surface (proc 4207). If results are abnormal, replace pack. 2. Replace <u>PEX</u> board (proc 5304).
4A	<p><u>Title:</u> Too Many On Cylinder Dropouts</p> <p><u>DESCRIPTION:</u> Indicates that On Cylinder Sense took too long to stabilize during the settle in phase. When the drive displays code 4A, the following error indications also appear:</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the error occurs during a first seek:</p> <ul style="list-style-type: none"> ● First Seek LED lights. ● FAULT indicator lights and Fault line goes active (first seeks only). ● Heads unload but motor continues to run. <p>If the error occurs during an RTZ or normal seek:</p> <ul style="list-style-type: none"> ● Seek Error and Seek End lines go active. ● Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Cylinder pulses missed or miscounted during seek. Could be caused by bad cylinder pulse detection circuits, defective pack, bad tribit decoder circuits, or electrical noise generated by nearby equipment.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Look for bad tracks on servo surface (proc 4207). If results are abnormal, replace pack. 2. Replace _PEX board (proc 5304).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
4B	<p><u>Title:</u> Off Cylinder</p> <p><u>DESCRIPTION:</u> Indicates that either On Cylinder Sense went inactive or cylinder pulses were detected while On Cylinder was active. When the drive displays code 4B, the following error indications also appear.</p> <ul style="list-style-type: none"> ● On Cylinder goes inactive ● Seek Error goes active. ● Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk. <p>An RTZ command clears the seek error and initiates a seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Bad servo disk, loose cabling in feedback loop, or poor tracking due to mechanical or electrical noise problems.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. If error occurs at same cylinder each time: <ol style="list-style-type: none"> a. Replace pack. b. Inspect and clean rails and carriage bearings (proc 5208). 2. If error occurs at random locations: <ol style="list-style-type: none"> a. Use servo test mode (proc 4207) to check carriage movement.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>b. Check for loose cable connections between servo head and _UUN board.</p> <p>c. Check for loose cable connections between _UUN and _PEX boards.</p> <p>d. Replace _PEX board (proc 5304).</p> <p>e. Replace servo head (proc 5212).</p>
4C	<p><u>Title:</u> Lost Demodulator Active While On Cylinder</p> <p><u>DESCRIPTION:</u> Indicates that Demodulator OK went inactive while the heads were on cylinder. When the drive displays code 4C, the following error indications also appear.</p> <ul style="list-style-type: none"> ● On Cylinder goes inactive ● Seek Error goes active. ● Motor continues to run but heads unload. <p>An RTZ command clears the seek error and initiates a load and seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Bad servo disk, bad tribit decoder circuits, loose cabling in feedback loop.</p> <p><u>ACTIONS</u></p> <p>Perform sequential forward seeks with read.</p> <ol style="list-style-type: none"> 1. If error occurs at same cylinder each time, replace pack.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>2. If error occurs at random locations:</p> <ul style="list-style-type: none"> a. Use servo test mode (proc 4207) to check position signal. b. Check for loose cable connections between servo head and _UUN board. c. Check for loose cable connections between _UUN and _PEX boards. <p>3. If problem still exists, replace _PEX (proc 5304).</p>
4D	<p><u>Title:</u> Illegal Cylinder Address</p> <p><u>DESCRIPTION:</u> Indicates that, during a normal seek, the MPU received too high a cylinder address (greater than 822). When the drive displays code 4D, the following error indications also appear.</p> <ul style="list-style-type: none"> ● On Cylinder goes inactive. ● Seek Error and Seek End Go Active ● Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p><u>PROBABLE CAUSES:</u> Illegal address sent to _PEX by _EBN/EDN board (defective I/O board).</p> <p><u>ACTIONS</u></p> <ul style="list-style-type: none"> 1. Replace _EBN/_EDN board (proc 5303). 2. Replace _PEX board (proc 5304). 3. Replace _PFX board (proc 5302).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
4E	<p><u>Title:</u> Voltage Fault While On Cylinder</p> <p><u>DESCRIPTION:</u> Indicates that the MPU detected a voltage fault while On Cylinder was active. When the drive displays code 4E, the following error indications also appear.</p> <ul style="list-style-type: none"> ● READY indicator goes out and Ready line goes inactive. ● Seek Error goes active. ● FAULT indicator lights and Fault line goes active. ● Motor continues to run but emergency retract unloads heads. <p>If the fault is no longer present, a Controller Fault Clear followed by an RTZ or pressing Fault Clear switch clears the fault and initiates a load and seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Power failure within drive, power supply or site power.</p> <p><u>ACTIONS</u></p> <p>Check LEDs for cause of fault condition.</p> <ol style="list-style-type: none"> 1. If voltage fault exists go to Power Check (TSP1).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
50	<p><u>Title:</u> Recovering From Low Vcc Reset</p> <p><u>DESCRIPTION:</u> Indicates that recovery from low Vcc re-set has taken place. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase.</p> <p>When MPU initialization is complete, Seek Error and Seek End go active. The Fault line also goes active and the FAULT indicator lights.</p> <p>The drive proceeds to bring the motor up to speed but will not load the heads until the fault condition is cleared (via controller Fault Clear signal or pressing Fault Clear switch). If the fault is cleared and load is successful, Ready goes active when the MPU is ready to perform normal servo actions. Seek error stays set until an RTZ is received.</p> <p><u>PROBABLE CAUSES:</u> Momentary power supply or site power failure.</p> <p><u>ACTIONS</u></p> <p>1. If more resets occur check site power, power supply, and drive power wiring.</p>
51	<p><u>Title:</u> Recovering From MPU Hang Reset</p> <p><u>DESCRIPTION:</u> Indicates that the drive is re-executing the power on sequence routine in an attempt to recover from an MPU hang condition. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase. When MPU initialization is complete, Seek Error and Seek End go active.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the recovery is successful, Ready goes active but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. An RTZ clears the seek error and initiates a seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Chip failure in MPU system causing instruction to be read incorrectly from EPROM.</p> <p><u>ACTIONS</u></p> <p>1. Replace _PEX board (proc 5304)</p>
52	<p><u>Title:</u> Recovered From Low Vcc Reset and Subsequent Speed Loss</p> <p><u>DESCRIPTION:</u> Indicates that the heads are after recovery from a low Vcc reset followed by a loss of speed error. Seek Error is active. Ready remains active. On Cylinder remains inactive until the drive receives an RTZ.</p> <p><u>PROBABLE CAUSES:</u> Momentary power supply or site power failure.</p> <p><u>ACTIONS</u></p> <p>1. If more resets occur check site power, power supply, and drive power wiring.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
53	<p><u>Title:</u> Recovered From MPU Hang And Subsequent Speed Loss</p> <p><u>DESCRIPTION:</u> Indicates that the heads are floating after recovery from an MPU hang followed by a loss of speed error. Seek Error is active. Ready remains active. On Cylinder remains inactive until the drive receives an RTZ.</p> <p><u>PROBABLE CAUSES:</u> Microprocessor failed or conditions existed that caused it to hang in an illegal mode.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Replace _PEX board (proc 5304).
5C	<p><u>Title:</u> Fan Fault</p> <p><u>DESCRIPTION:</u> Indicates that the drive cooling fan has failed. If the fan fault stays set for greater than 400 MS, the drive will stop (similar to using start switch to stop drive). During this period, the MPU will continually attempt to clear the fault. If the MPU is successful in clearing the fault, the drive will start; (provided no other faults are present).</p> <p><u>PROBABLE CAUSES:</u> Clogged air filter, defective cooling fan or dc voltage is missing from fan cable.</p> <p><u>ACTION</u></p> <ol style="list-style-type: none"> 1. If fan is running: <ol style="list-style-type: none"> a. Check air filters. Clean or replace primary filter. Replace absolute filter (proc 5105). b. Replace _EBN/_EDN (Proc 5303).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>2. If fan is not running:</p> <p>a. If -24 volts is present at fan connector, replace fan (proc 5201).</p> <p>b. If -24 volts is not present, go to -24 Volt Power Check (TSP3).</p> <p>c. Replace <u>_EBN/_EDN</u> board (proc 5303).</p>
5D	<p><u>Title:</u> First Seek Fault</p> <p><u>DESCRIPTION:</u> Indicates that a seek error occurred during the initial drive start up (scan cycle). The scan cycle begins before the Ready and On Cylinder lines go active.</p> <p><u>PROBABLE CAUSES:</u> Bad tribits on the disk pack. Particle contamination on rails and/or bearings; other types of hardware interference. Problem in the <u>_PEX</u> board seek circuits.</p> <p><u>ACTION</u></p> <ol style="list-style-type: none"> 1. Use servo test mode (proc 4207) to check position signal and carriage travel. 2. Replace pack. 3. Check for loose cable between servo head and <u>_UUN</u> board. 4. Inspect and clean rails and bearings (proc 5208). 5. Replace <u>_PEX</u> board (proc 5304).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
5E	<p><u>Title:</u> Demodulator OK After Unload</p> <p><u>DESCRIPTION:</u> Indicates that, during a power off sequence, the Demodulator OK signal was still active after the heads loaded switch indicated that the heads were unloaded. When the drive detects this condition, it keeps the motor running until dc power is removed from the drive (CBI set to OFF).</p> <p><u>PROBABLE CAUSES:</u> Defective heads loaded switch, bad tribit decoder circuit or defective retract circuit in power amp board.</p> <p><u>ACTIONS</u></p> <p>Check if heads are loaded.</p> <ol style="list-style-type: none"> 1. If heads are over disk and heads loaded signal is present at heads loaded switch, replace switch (proc 5213). 2. If heads are retracted, replace _PEX board (proc 5304). 3. If problem still exists, replace _PDX board (proc 5307).
5F	<p><u>Title:</u> PIA Test Failure</p> <p><u>DESCRIPTION:</u> Indicates that, during power on initialization, the MPU detected a PIA failure. When this occurs the drive stops the power on sequence and keeps all fault LEDs lighted. To clear the error and initiate a retry, set CBI to Off and then back to On.</p> <p><u>PROBABLE CAUSES:</u> Bad PIA or defective chip in MPU system.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check that no test probe tips are shorting out PIA outputs. 2. Replace _PEX board (proc 5304).
80	<p><u>Title:</u> Fault Before Seek Begins</p> <p><u>DESCRIPTION:</u> Indicates that a fault condition existed when a normal or RTZ seek was commanded. When the drive displays code 80, the following error indications also appear.</p> <ul style="list-style-type: none"> ● Seek Error and Seek End go active. ● Ready goes inactive. ● FAULT indicator lights and Fault line goes active. ● For a voltage fault, the motor continues to run but heads are unloaded via emergency retract. ● For other than a voltage fault, the motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. <p>If the fault is no longer present, a Controller Fault Clear followed by an RTZ or pressing Fault Clear switch clears the fault and initiates a load and seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Any of the possible fault conditions.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check fault LEDs on _PEX board.
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description																																										
90	<p><u>Title:</u> Recovered From Speed Loss</p> <p><u>DESCRIPTION:</u> Indicates that drive has recovered from a speed loss. The heads are loaded but floating and Seek Error is active. On Cylinder and Ready will go active when the drive receives an RTZ.</p> <p><u>PROBABLE CAUSES:</u> Motor control circuit, motor failure or power supply failure.</p> <p><u>ACTIONS</u></p> <p>If more failures occur:</p> <ol style="list-style-type: none"> 1. Replace <u>PMX</u> board (proc 5308). 2. Replace power supply (proc 5203). 3. Replace motor and cable assembly (Proc 5209). 																																										
AO thru CE	<p><u>Title:</u> Error conditions with FAULT present.</p> <p><u>DESCRIPTION:</u> The following codes correspond to codes previously listed, except that the FAULT line is active when they are observed. The codes covered in this discussion are listed below with the corresponding (NO FAULT) code given in parentheses.</p> <table border="0" data-bbox="363 1486 1354 1709"> <tr> <td>A0 (20)</td> <td>A1 (21)</td> <td>A2 (22)</td> <td>A3 (23)</td> <td>A4 (24)</td> <td>A5 (25)</td> </tr> <tr> <td>A6 (26)</td> <td>A7 (27)</td> <td>A8 (28)</td> <td>A9 (29)</td> <td>AA (2A)</td> <td>AB (2B)</td> </tr> <tr> <td>AC (2C)</td> <td>AD (2D)</td> <td>BO (30)</td> <td>B1 (31)</td> <td>B2 (32)</td> <td>B3 (33)</td> </tr> <tr> <td>B4 (34)</td> <td>B5 (35)</td> <td>B6 (36)</td> <td>B7 (37)</td> <td>B8 (38)</td> <td>B9 (39)</td> </tr> <tr> <td>CO (40)</td> <td>C1 (41)</td> <td>C2 (42)</td> <td>C3 (43)</td> <td>C4 (44)</td> <td>C5 (45)</td> </tr> <tr> <td>C6 (46)</td> <td>C7 (47)</td> <td>C8 (48)</td> <td>C9 (49)</td> <td>CA (4A)</td> <td>CB (4B)</td> </tr> <tr> <td>CC (4C)</td> <td>CD (4D)</td> <td>CE (4E)</td> <td></td> <td></td> <td></td> </tr> </table>	A0 (20)	A1 (21)	A2 (22)	A3 (23)	A4 (24)	A5 (25)	A6 (26)	A7 (27)	A8 (28)	A9 (29)	AA (2A)	AB (2B)	AC (2C)	AD (2D)	BO (30)	B1 (31)	B2 (32)	B3 (33)	B4 (34)	B5 (35)	B6 (36)	B7 (37)	B8 (38)	B9 (39)	CO (40)	C1 (41)	C2 (42)	C3 (43)	C4 (44)	C5 (45)	C6 (46)	C7 (47)	C8 (48)	C9 (49)	CA (4A)	CB (4B)	CC (4C)	CD (4D)	CE (4E)			
A0 (20)	A1 (21)	A2 (22)	A3 (23)	A4 (24)	A5 (25)																																						
A6 (26)	A7 (27)	A8 (28)	A9 (29)	AA (2A)	AB (2B)																																						
AC (2C)	AD (2D)	BO (30)	B1 (31)	B2 (32)	B3 (33)																																						
B4 (34)	B5 (35)	B6 (36)	B7 (37)	B8 (38)	B9 (39)																																						
CO (40)	C1 (41)	C2 (42)	C3 (43)	C4 (44)	C5 (45)																																						
C6 (46)	C7 (47)	C8 (48)	C9 (49)	CA (4A)	CB (4B)																																						
CC (4C)	CD (4D)	CE (4E)																																									
Table Continued on Next Page																																											

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>When the drive displays one of the A0 through CE codes the following error indications also appear.</p> <ul style="list-style-type: none"> ● First Seek LED lights (first seek only). ● FAULT indicator lights and Fault line goes active. ● Seek Error and Seek End lines go active (not during first seek). ● Motor continues to run but heads remain unloaded. <p>If the fault condition no longer exists, a Controller Fault Clear followed by an RTZ or pressing the Fault Clear switch clears the fault and initiates another load.</p> <p><u>PROBABLE CAUSES:</u> Voltage fault caused by failure within drive, site power, or power supply. Extraneous fault, such as read and write, caused by I/O problem.</p> <p><u>ACTIONS:</u></p> <p>Check LEDs for cause of fault condition.</p> <ol style="list-style-type: none"> 1. If voltage fault exists: <ol style="list-style-type: none"> a. Check ± 24 volts (proc 4101). If voltages are abnormal, go to ± 24 Volt Load Check (TSP3). b. Replace power supply (proc 5203). 2. If a fault other than voltage exists: <ol style="list-style-type: none"> a. Check I/O cabling. b. Replace <u>EBN/_EDN</u> board (proc 5303).
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
D0	<p><u>Title:</u> Recovering From Low Vcc Reset</p> <p><u>DESCRIPTION:</u> Indicates that recovery from low Vcc has taken place. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase.</p> <p>When MPU initialization is complete, Seek Error and Seek End go active. The Fault line also goes active and the FAULT indicator lights. Code D0 remains set until the Fault line goes inactive.</p> <p>The drive proceeds to bring the motor up to speed but will not load the heads until the fault condition is cleared (via controller Fault Clear signal or pressing Fault CLeAr switch). If the fault is cleared and load is successful, Ready goes active when the MPU is ready to perform normal servo actions. Seek error stays set until an RTZ is received.</p> <p><u>PROBABLE CAUSES:</u> Momentary power failure.</p> <p><u>ACTIONS:</u></p> <ol style="list-style-type: none"> 1. If more resets occur, check site power, power supply and drive power wiring.
D1	<p><u>Title:</u> Recovering From MPU Hang Reset</p> <p><u>DESCRIPTION:</u> Indicates that the drive is re-executing the power on sequence routine in an attempt to recover from an MPU hang condition. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase. When MPU initialization is complete, Seek Error and Seek End go active. Code D1 remains set until the Fault line goes inactive.</p>
<p>Table Continued on Next Page</p>	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	<p>If the recovery is successful, Ready goes active but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. An RTZ clears the seek error and initiates a seek to cylinder 0.</p> <p><u>PROBABLE CAUSES:</u> Chip failure in MPU system causing instruction mode to be read incorrectly from EPROM.</p> <p><u>ACTIONS:</u></p> <ol style="list-style-type: none"> 1. Replace _PEX board (proc 5304).
FF	<p><u>Title:</u> MPU Failed Power On Test</p> <p><u>DESCRIPTION:</u> Indicates that MPU failed power on initialization test. When this occurs, the drive stops the power on sequence and keeps all fault LEDs lighted. To clear the error and initiate a retry, set CB1 to OFF and then back to ON.</p> <p><u>PROBABLE CAUSES:</u> Bad MPU, RAM, or other failure preventing MPU from operating.</p> <p><u>ACTIONS</u></p> <ol style="list-style-type: none"> 1. Check for a failure in the +5 volts and +24 volts power supply (proc 4101). 2. Replace _PEX board (proc 5304).

SECTION

4

ELEC-

TRICAL

CHECKS

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

This section contains electrical checks intended for use in isolating problems causing improper drive operation. These procedures should be used in conjunction with the troubleshooting information in section 3.

If the drive appears to be operating properly, failure to meet a specification given here does not in itself indicate improper drive operation. The person performing these procedures should be thoroughly familiar with drive operation and with all information in the general maintenance section of this manual (particularly the warnings and precautions).

Each electrical check procedure is assigned a unique number. The numbers are used elsewhere in the manual to reference the procedures. The procedure numbers are organized into five categories: 41XX - power checks, 42XX - servo checks, 43XX - write checks, 44XX - read checks, and 45XX - miscellaneous.

The procedures appear in the following order.

- 4101 - Power Checks
- 4201 - Tribit Check
- 4202 - Position Signal Check
- 4203 - Servo Offset Check
- 4204 - On Cylinder Check
- 4205 - Cylinder Pulse Check

- 4206 - Power Amp Driver Check
- 4207 - Servo Test Mode
- 4301 - Write Fault Grounding
- 4302 - Write PLO Check
- 4303 - Write Data Check
- 4304 - Write Address Mark Check
- 4305 - Write Current Check
- 4401 - Read PLO Check
- 4402 - Read Data Check
- 4403 - Read Address Mark Check
- 4501 - Index Check
- 4502 - Sector Check

4101 - POWER CHECKS

The following procedure provides an overall check of the dc voltages used by the drive. Table 4-1, shows the voltages required by each drive component. See the diagrams section of hardware maintenance manual volume 3 for specific information concerning voltage test points.

1. Command continuous seeks between cylinders 0 and 274.

CAUTION

Because some of the voltage measurements are taken on adjacent pins, it is possible to touch both pins simultaneously, thus causing a short circuit. A short circuit will cause serious damage to drive electronics assemblies. Therefore, use extreme caution when performing the following steps.

2. Connect voltmeter ground lead to J19-4 (ground).
3. Measure between J19-4 and the appropriate connection points to check the following voltages:

<u>Voltage</u>	<u>Connection</u>	<u>Specification</u>
+5 volts	J19-7 (_EBN/_EDN)	+4.90 to +5.25 volts
-5 volts	J19-1 (_EBN/_EDN)	-4.90 to -5.30 volts
-8.3 volts	J28-6 (_PEX)	-8.1 to -8.5 volts
+24 volts	J19-5 (_EBN/_EDN)	+21.6 to +26.4 volts
-24 volts	J19-6 (_EBN/_EDN)	-21.6 to -26.4 volts
+40 volts	J40-7 (pwr input)	+36 to +42 volts (Motor must be running to observe + 40 volts)

4. Proceed to next test or return drive to online operation.

SERVO CHECKS

4201 - TRIBIT CHECK

1. Connect oscilloscope as shown on figure 4-1.
2. Command direct seek to cylinder 0.
3. Observe that the relationship between +Servo Tribit and -Servo Tribit signals is similar to that on figure 4-1.
4. Connect oscilloscope as shown on figure 4-2.
5. Observe that the +Tribit signal is similar to that on figure 4-2.
6. Proceed to next test or return drive to online operation.

4202 - POSITION SIGNAL CHECK

1. Connect oscilloscope as shown on figure 4-3.
2. Command continuous seeks between cylinders 0 and 274.
3. Observe that the peak to peak value of +Position signal remains between 9 and 10 volts over the period of a complete seek.
4. Command continuous seeks between cylinders 0 and 822 and observe that +Position is as described in step 3 (see figure 4-4).
5. Return drive to online operation.
6. Proceed to next test or return drive to online operation.

TABLE 4-1. DC VOLTAGE DISTRIBUTION

Component	Voltage					
	+5V	-5V	-8.3V	+24V	-24V	+40V
_PEX	X	X	X	X	X	
_PGX	X	X				
_PFX	X	X				
_EBN/_EDN	X	X		X	X	
_PDX				X	X	X
_PMX	X			X		X
_PCX	X	X				
_UUN			X			
Fan					X	
Motor	X					X
Op Pnl (_PBX)	X					

4203 - SERVO OFFSET CHECK

This procedure checks the amount of head offset caused by a servo offset command. The measurement is made on the Position signal. The Position signal has an average dc level of zero, when there is no offset and the heads are on cylinder.

OSCILLOSCOPE SETUP

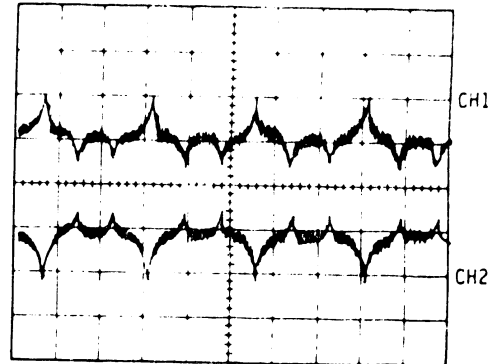
INPUT			
CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	5.0 mv/cm	J28-04 ON_PEX	-SERVO
CH 2	5.0 mV/cm	J28-02 ON_PEX	+SERVO

TRIGGERING		
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1 μ S/CM MODE:

NOTES:



10R246

Figure 4-1. Servo Signal Waveform

OSCILLOSCOPE SETUP

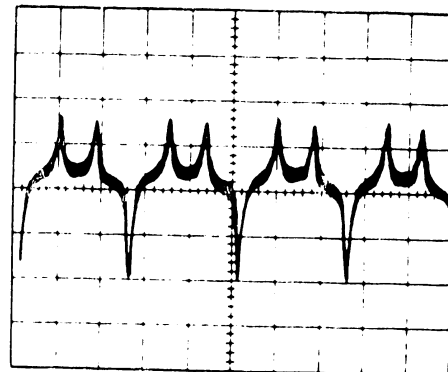
INPUT			
CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/OM	CHIP N356 PIN 10 ON_PEX	+TRIBIT
CH 2			

TRIGGERING		
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1 μ S/CM MODE:

NOTES:



10R247

Figure 4-2. Tribits Waveform

OSCILLOSCOPE SETUP

INPUT

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	J13-05 ON _PEX	+POSITIVE
CH 2			

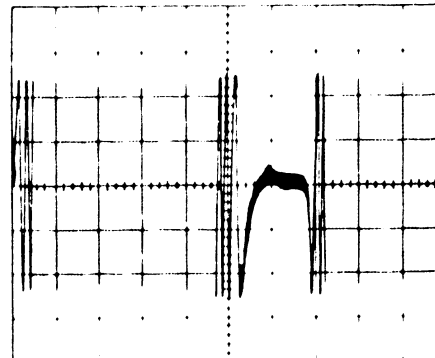
TRIGGERING

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+EXT	TF-H656 (W) ON _PEX	-FORWARD

SCOPE GND TO GND ON LOGIC CARD
USE X10 PROBES UNLESS OTHERWISE NOTED

TIME/DIV: 5 MS/CM MODE CH 1

NOTES:



10R248

Figure 4-3. Position Signal (Tracks 0-274)

1. Connect digital voltmeter between J13-4 on _PEX board and ground (chassis). On units with older _PEX boards, J13 is located behind __EBN/__EDN board. Remove __EBN/__EDN board from screw posts to gain access to J13.
2. Command direct seek to cylinder 0 and observe that meter indicates 0 ± 50 millivolts.
3. Command a read operation with positive (forward) offset. Observe that meter indicates an average dc offset as follows:
 - a. Between +1.35 and +1.65 volts, for units with BPEX board.
 - b. Between +0.60 and +0.90 volts, for units with other _PEX boards.
4. Command a read operation with negative (reverse) offset. Observe that meter indicates an average dc offset as follows:
 - a. Between -1.35 and -1.65 volts, for units with BPEX board.

OSCILLOSCOPE SETUP

INPUT

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	J13-05 ON _ PEX	+POSITION
CH 2			

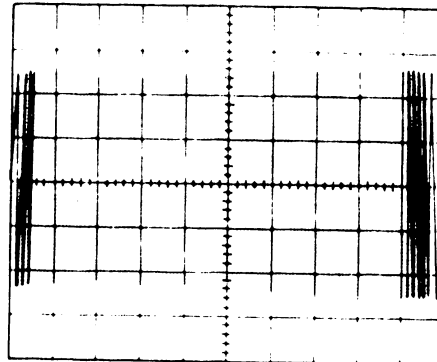
TRIGGERING

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+EXT	TP-H656 (W) ON _ PEX	-FORWARD

SCOPE GND TO GND ON LOGIC CARD
USE X10 PROBES UNLESS OTHERWISE NOTED

TIME/DIV: 5 MS/CM MODE: CH1

NOTES:



10R249

Figure 4-4. Position Signal (Tracks 0 to 822)

- b. Between -0.60 and -0.90 volts, for units with other _PEX boards.
5. Proceed to next test or return drive to online operation.

4204 - ON CYLINDER CHECK

This procedure verifies that On Cylinder goes active.

1. Connect oscilloscope as follows:
 - a. Connect channel 1 to TP-D617(G) (+ On Cylinder) on _EBN/_EDN board.
 - b. Trigger + Internal.
 - c. Set other controls as appropriate to make measurement in step 3.

2. Command continuous seeks between cylinders 0 and 1.
3. Observe that + On Cylinder goes active.
4. Proceed to next test or return drive to online operation.

4205 - CYLINDER PULSE CHECK

This procedure verifies the presence and pulse width of drive cylinder pulses.

1. Connect oscilloscope as follows:
 - a. Connect channel 1 to TP-H422(M) (-Cylinder Pulses) on _PEX board.
 - b. Trigger + Internal.
 - c. Set other controls as appropriate to make measurements in step 3.
2. Command continuous seeks between cylinders 0 and 822.
3. Observe that Cylinder Pulses are present and have a pulse width greater than 1.25 microseconds.
4. Proceed to next test or return drive to online operation.

4206 - POWER AMP DRIVER CHECK

Perform the following procedure if the MPU is unable to load heads and a failure in the power amp circuit is suspected.

1. Connect oscilloscope as follows:
 - a. Trigger + Internal.
 - b. Measure the dc voltage level at both ends of resistors D323 (Out Drive) and D623 (In Drive) on the _PEX board.
2. Evaluate results as follows:
 - a. The Out Drive signal is active if the voltage drop across D323 is greater than 2 Volts.
 - b. The In Drive signal is active if the voltage drop across D623 is greater than 2 Volts.

3. If both signals are active simultaneously, the _PEX board is defective. A defect in this circuit could cause the _PDX board to fail also.
4. Proceed to next test or return drive to online operation.

4207 - SERVO TEST MODE

Perform the following procedure when it is suspected that the data pack servo track or servo head is defective. This procedure may also be used to check servo demodulator and position circuits.

1. Press START switch to unload heads and stop drive motor.
2. Remove the screws securing read/write boards to vertical and rear panel support brackets. Swing boards up and secure into place.
3. Remove top air cover to gain access to carriage.
4. Connect oscilloscope as shown on figure 4-5.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2 V/CM	J13-05	+ POSITION
CH 2		ON _PEX	

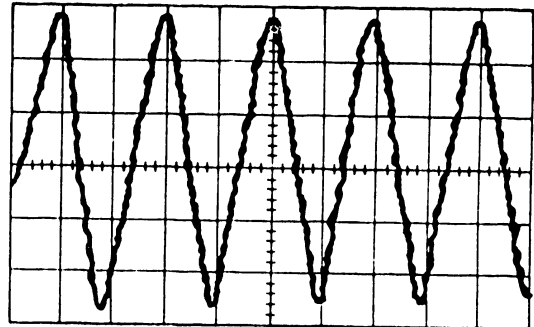
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT./CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED

TIME/DIV: 2 MS/CM MODE:

NOTES:



10R262

Figure 4-5. Normal Servo Tracks

CAUTION

Do not manually load or unload heads or damage to heads and disk surface may result.

NOTE

When the servo test jumper is installed and the heads are over the disk, pressing the START switch will not unload the heads or stop the drive motor. Removing the jumper will unload the heads. Pressing the Fault Clear Switch will allow the drive to complete a first seek.

5. Place a jumper across J737 (TP-AC) and J637 (TP-AB) on the PEX board. This will allow the heads to float over the disk surface.
6. Press START switch to start drive motor. Wait for Fault Indicator to light.
7. When FAULT indicator lights, press the Fault Clear switch to load heads.

WARNING

Because the emergency retract circuit can be activated (due to voltage fault), keep hands away from carriage area. Use a small screwdriver or equivalent to manually move carriage.

8. Slowly, move carriage (back and forth) over the full length of travel, while observing the +Position signal.
 - a. The +Position signal is normal if it appears as shown in figure 4-5.
 - b. If the +Position signal appears similar to figure 4-6, the servo track is defective. Replace data pack and repeat steps 1 through 8.
9. Remove jumper from PEX board and press START switch to stop drive motor and unload heads.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2 V/CM	J13-05 ON _PEX	+ POSITION
CH 2			

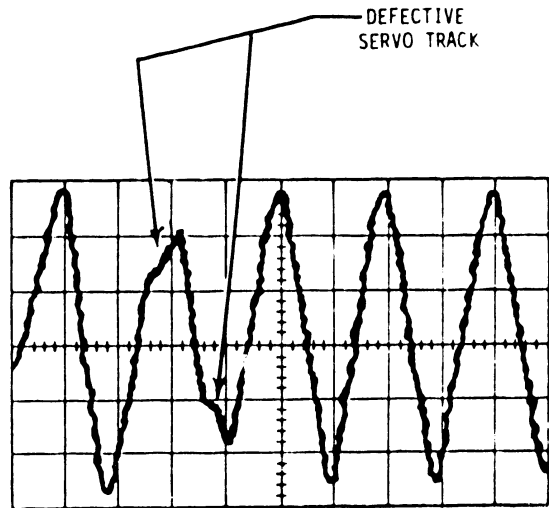
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT./CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 2 MS/CM MODE:

NOTES:



10R263

Figure 4-6. Defective Servo Tracks

10. Replace top air cover and return read/write boards to normal position.
11. Proceed to next test or return drive to online operation.

WRITE CHECKS

The following procedures, 4301 through 4305, check various aspects of drive write circuit operation. Figure 4-7 is a block diagram showing the major components in the write circuits and the test points used in the procedures.

4301 - WRITE FAULT GROUNDING

If a write fault condition exists, the drive write circuits are disabled. This makes it difficult to test the write circuits and isolate the problem. Grounding the Write Fault signal at the point where it leaves the __PGX board disables the write fault function thus allowing the drive to perform write operations even though fault conditions exist. The following procedure describes the proper method for grounding the Write Fault signal.

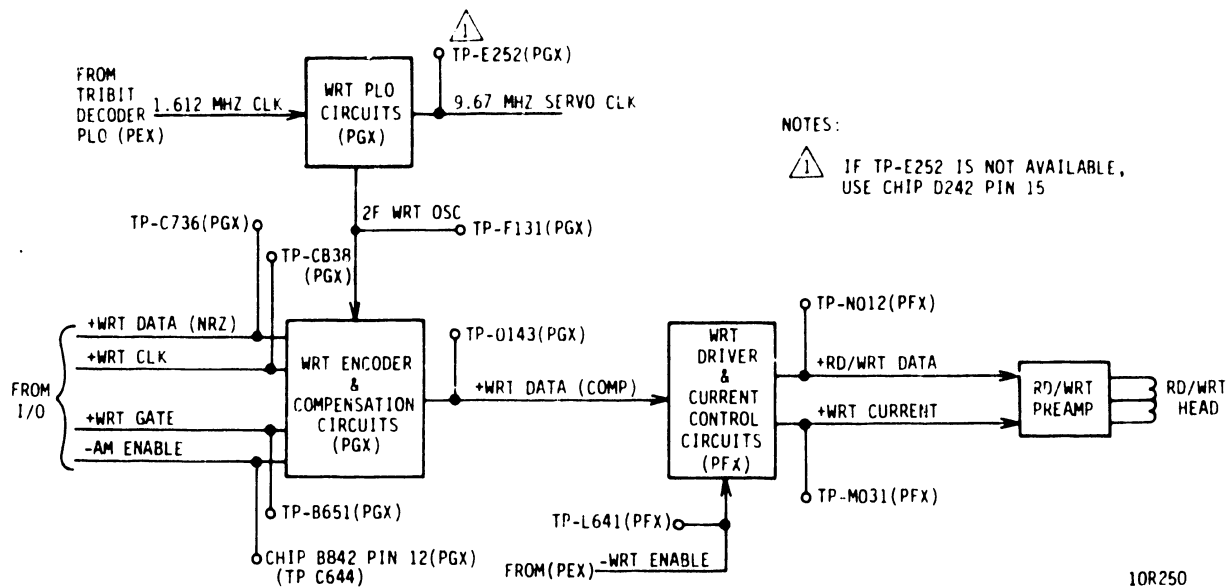


Figure 4-7. Write Circuits Test Points

CAUTION

Perform this procedure only during troubleshooting when a write fault condition interferes with isolating the problem.

1. Remove power from drive as follows:
 - a. Press START switch to stop motor and unload heads.
 - b. Set CB1 to off.

CAUTION

Be certain to remove jumper wire when testing is complete. Failure to remove wire can result in loss of customer data.

2. Connect jumper wire between TP-C642 (Write Fault) and TP-A460 (ground) on _PGX board.

3. Power up drive and perform tests. Monitor TP-C643 (Fault) on _PGX board to determine if write fault condition persists. When testing is complete, remove jumper wire.

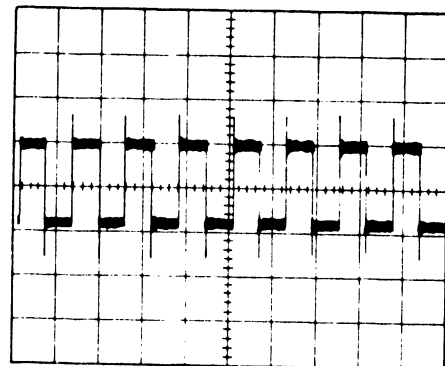
4302 - WRITE PLO CHECK

This procedure checks the operation of the write PLO. The PLO provides timing signals used, during write operations by both the drive and controller.

1. Connect oscilloscope and observe that 1.612 MHz Clock frequency is approximately as shown on figure 4-8.
2. Connect oscilloscope and observe that 9.67 MHz Clock frequency is approximately as shown on figure 4-9.
3. Connect oscilloscope and observe that 2F Write Oscillator timing is approximately 19.34 MHz (see figure 4-10).
4. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INP'T.			
CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C439 ON _PGX	1.612 MHZ CLK
CH 2			
TRIGGERING:			
SLOPE/SOURCE		CONNECTION	SIGNAL NAME
-INT CH1			
SCOPE GND TO GND ON LOGIC CARD. USE X10 PROBES UNLESS OTHERWISE NOTED.			
TIME/DIV: 0.5 μ S/CM		MODE:	
NOTES:			



10R155

Figure 4-8. 1.612 MHz Clock Timing

4303 - WRITE DATA CHECK

This procedure checks for the presence of write data at various points in the write circuits (see figure 4-7). If the signals at these points are correct, it indicates the circuits are performing their basic functions. This procedure will normally be performed because of a write problem. In that case, a write fault condition may exist and it will be necessary to perform procedure 4301 - Write Fault Grounding to perform a write operation.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track, or use a scratch pack.

1. Command drive to seek to desired cylinder and select desired head.
2. Command drive to write a 1010... pattern.
3. Connect oscilloscope and observe that Write Gate and Write Enable appear as shown on figure 4-11.

OSCILLOSCOPE SETUP

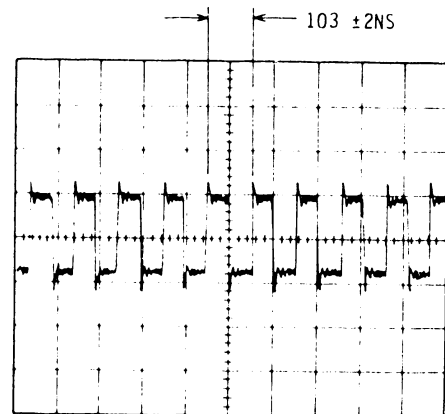
INPUT:			
CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-E252	+9.67 MHZ CLK
CH 2		ON_PGX	
		⚠	
TRIGGERING:			
SLOPE/SOURCE		CONNECTION	SIGNAL NAME
-INT CH1			

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.1 μ S/CM MODE:

NOTES:

⚠ IF TP-E252 IS NOT AVAILABLE, USE CHIP D242 PIN 15



10R156

Figure 4-9. 9.67 MHz Clock Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.2 V/CM	TP-F131 ON_PGX	+2F WRT OSC
CH 2			

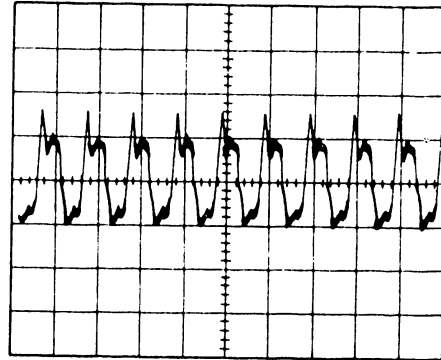
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.05 μ S/CM MODE:

NOTES:



10R157

Figure 4-10. 2F Write Oscillator Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-B651 ON_PGX	+WRT GATE
CH 2	2.0 V/CM	TP-L641 ON_PFX	-WRT ENABLE

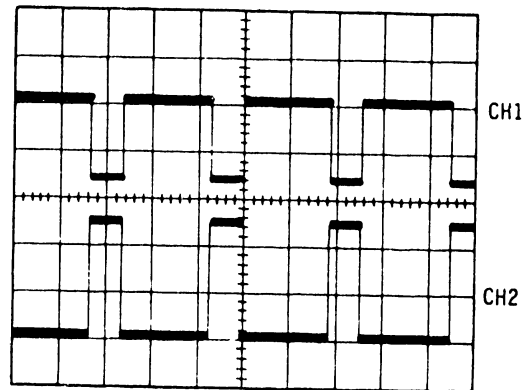
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.1 MS/CM MODE: ALT

NOTES:



10R158B

Figure 4-11. Write Gate Timing

4. Check inputs to write encoder and compensation circuits. Timing relationships between these signals, NRZ write data and write clock, must be correct before encoding and write compensation can be properly performed.
 - a. Connect oscilloscope as shown on figure 4-12 and observe that Write Clock frequency is approximately 9.67 MHz.
 - b. Observe that timing relationship between Write Data (NRZ) and Write Clock is similar to that on figure 4-12. Write Clock should go positive at approximately the center of the data "1" pulses.
5. Check input to write driver and current control circuits.
 - a. Connect oscilloscope as shown on figure 4-13.
 - b. Observe that Write Data (Compensated) pulses are similar to those on figure 4-13.
6. Check output of write driver and current control circuits. This ensures that data is being sent to the read/write preamplifier.

OSCILLOSCOPE SETUP

INPUT:			
CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C736 ON -PGX	+WRT DATA (NRZ)
CH 2	0.5 V/CM	TP-C838 ON -PGX	+WRT CLK

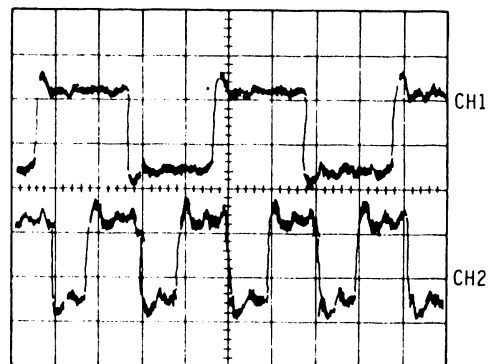
TRIGGERING:		
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50NS/CM MODE: ALT

NOTES:

1. DISREGARD ANY GHOST IMAGES.



10R159A

Figure 4-12. Write Data to Clock Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D143 ON _PGX	+WRT DATA COMP
CH 2	0.5 V/CM	TP-F131 UN _PGX	+2F WRT OSC

TRIGGERING:

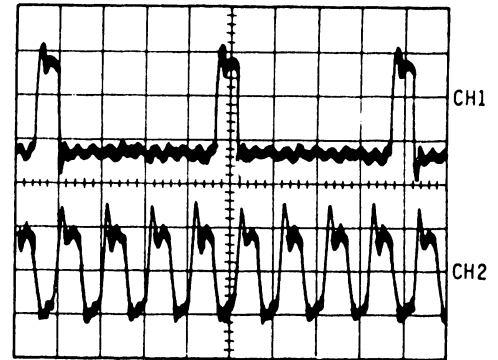
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.05 μ S/CM MODE: ALT

NOTES:

1. DISREGARD ANY GHOST IMAGES.



10R160

Figure 4-13. Compensated Write Data Timing

- a. Move oscilloscope channel 2 probe to TP-N012 on _PFX board (see figure 4-14).
 - b. Observe that signals are approximately as shown on figure 4-14.
7. Proceed to next test or return drive to online operation.

4304 - WRITE ADDRESS MARK CHECK

This procedure verifies that the drive is not writing during the time that Address Mark Enable is active.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track, or use a scratch pack.

1. Command continuous write format with address mark operations using a 1010... data pattern.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D143 ON _PGX	+WRT DATA COMP
CH 2	0.2 V/CM	TP-N012 ON _PFX	+RD/WRT DATA

TRIGGERING:

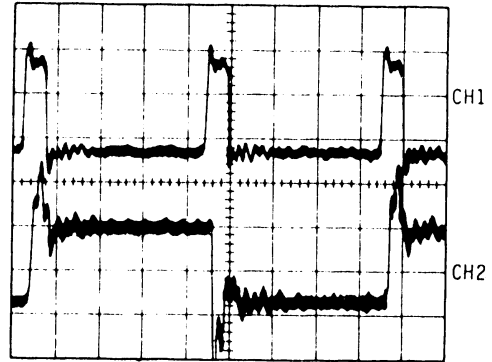
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH2		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.1 μ S/CM MODE: ALT

NOTES:

1. DISREGARD ANY GHOST IMAGES.



10R161

Figure 4-14. Write Driver Output

2. Connect oscilloscope as shown on figure 4-15.
3. Observe that there are no data "1" pulses during the time that Address Mark Enable is Active.
4. Proceed to next test or return drive to online operation.

4305 - WRITE CURRENT CHECK

This procedure checks for the presence of write current to the read/write preamplifier.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track, or use a scratch pack.

1. Command drive to seek to desired cylinder and select desired head.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-C644 ON_PGX	-AM ENABLE
CH 2	0.5 V/CM	TP-D143 ON_PGX	+WRT DATA COMP

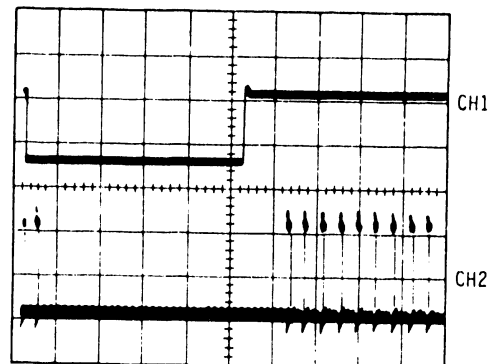
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 μ S/CM MODE: ALT

NOTES:



10R162

Figure 4-15. Write Address Mark Timing

2. Command a continuous write or write format operation using a 1010... pattern.
3. Connect oscilloscope and observe that signals are approximately as shown on figure 4-16.
4. Proceed to next test or prepare drive for online operation.

READ CHECKS

The following procedures, 4401 through 4404, check various aspects of drive read circuit operation. Figure 4-17 is a block diagram showing the major components in the read circuits and the test points used in the procedures.

4401 - READ PLO CHECK

This procedure checks the operation of the read PLO circuits (see figure 4-17). The read PLO provides timing signals used during read operations.

OSCILLOSCOPE SETUP

INPUT:			
CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-M031 ON_PFX	WRT CURRENT
CH 2	0.2 V/CM	TP-N012 ON_PFX	+RD/WRT DATA

TRIGGERING:		
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 μ S/CM MODE: CHOP

NOTES:

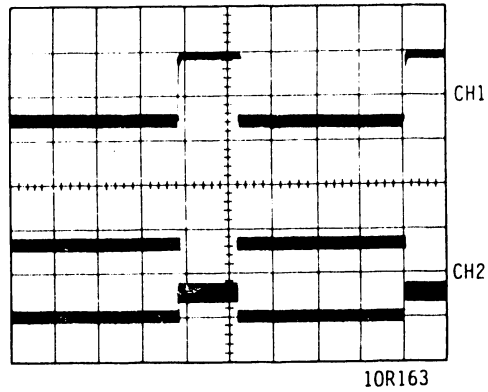


Figure 4-16. Write Current Timing

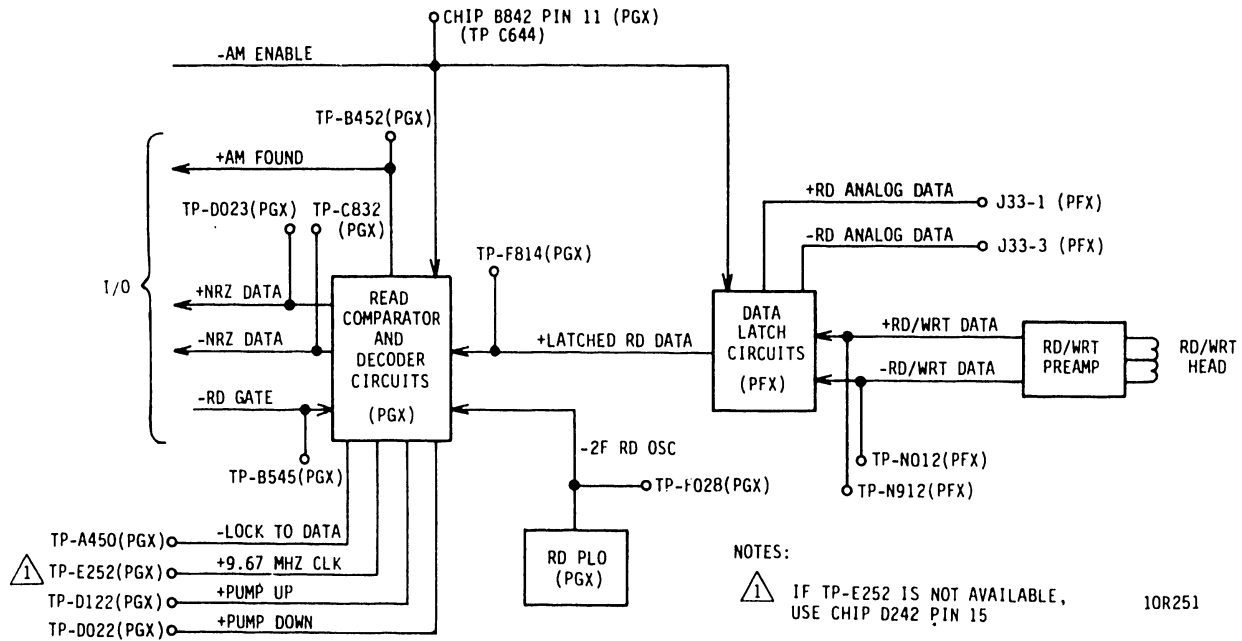


Figure 4-17. Read Circuits Test Points

1. Connect oscilloscope as shown on figure 4-18 and observe that 2F Read Oscillator frequency is approximately 19.34 MHz.
2. Connect oscilloscope as shown on figure 4-19 and observe that the + Pump Up and + Pump Down signals are coincident.
3. Command drive to write a 1010... pattern using any head.
4. Command drive to perform continuous read operations.
5. Observe that + Pump Up and + Pump Down signals have the same timing relationship shown on figure 4-20.
6. Proceed to next test or return drive to online operation.

4402 - READ DATA CHECK

This procedure checks the operation of the heads, preamplifier, data latch, read comparator, and 2-7 decoder circuits.

1. Perform Write Data Check (proc 4303).
2. Perform Read PLO Check (proc 4401).

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

3. Command drive to seek to desired cylinder and select desired head.
4. Command drive to write a 1010... pattern and then to perform continuous read operations.
5. Check output of heads and preamplifier.
 - a. Connect and setup oscilloscope as shown on figure 4-21.
 - b. Observe that Read/Write data appears approximately as shown.
6. Check the Latched Read Data signal and its timing relationship with the 2F Read oscillator signal.
 - a. Connect oscilloscope as shown on figure 4-22 and observe that Latched Read Data pulse width is as shown.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-F208 ON _FGX	-2F RD OSC
CH 2			

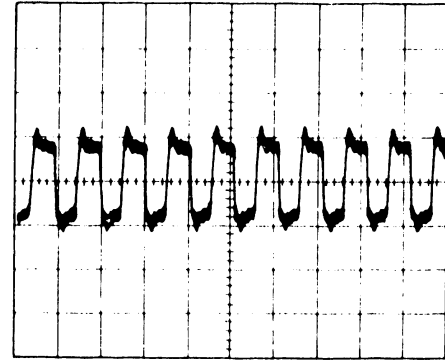
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE:

NOTES:



10R164A

Figure 4-18. 2F Read Oscillator Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D122 ON -PGX	+PUMP UP
CH 2	0.5 V/CM	TP-D022 ON -PGX	+PUMP DOWN

TRIGGERING:

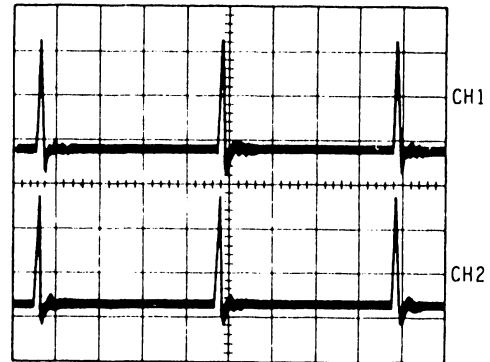
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

1. MEASUREMENT IS VALID ONLY IF DRIVE IS NOT READING
2. OBSERVE THAT CH1 AND CH2 SIGNALS ARE COINCIDENT.



10R165

Figure 4-19. Pump Up/Down Timing (Not Reading)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D122 ON_PGX	+PUMP UP
CH 2	0.5 V/CM	TP-D022 ON_PGX	+PUMP DOWN

TRIGGERING:

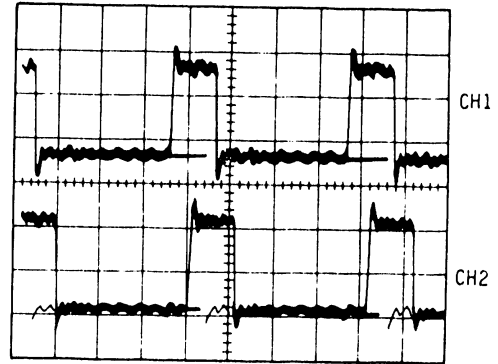
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

1. SIGNALS ARE OUT OF PHASE DURING READ



10R166

Figure 4-20. Pump Up/Down Timing (Reading)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	50 MV/CM	TP-M912 ON_PFX	-RD/WRT DATA
CH 2	50 MV/CM	TP-N012 ON_PFX	+RD/WRT DATA

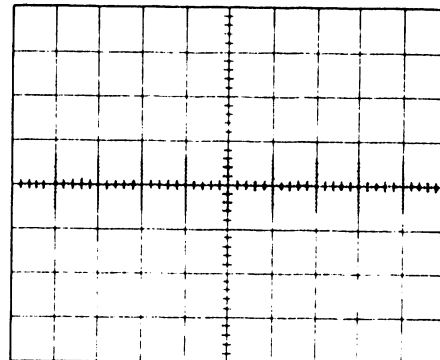
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-EXT	TP-B545 ON_PGX	-RD GATE

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 20 μ S/CM MODE: INVERT CH2
AND ADD

NOTES:



10R167A

Figure 4-21. Read Preamplifier Output

- b. Observe that Latched Read Data pulses are approximately coincident with 2F Read Oscillator pulses (see figure 4-22).
 - c. Observe that the data pattern is correct (see figure 4-22).
7. Check Read Data to Read Clock Timing.
- a. Connect oscilloscope as shown on figure 4-23 and observe that Read Clock frequency is approximately 9.67 Mhz.
 - b. Observe that Read Data to Read Clock timing is approximately as shown. Read Clock should go positive approximately at the center of the data "1" pulses.
 - c. Observe that the NRZ data has a 1010... pattern.
8. Check Read Gate to Lock to Data timing.
- a. Connect oscilloscope as shown on figure 4-24.
 - b. Observe that -Lock to Data goes low at the proper time (see figure 4-24).
9. Proceed to next test or return drive to online operation.

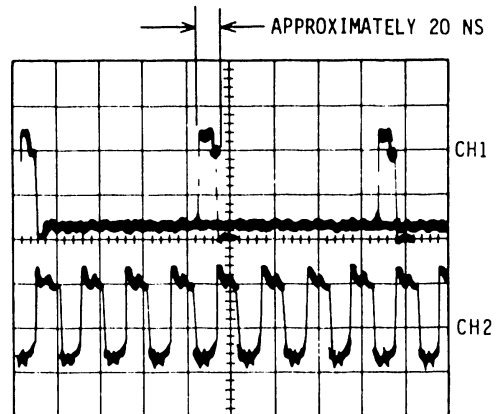
OSCILLOSCOPE SETUP

INPUT:			
CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-F814 ON _PGX	+LATCHED RD DATA
CH 2	0.5 V/CM	TP-F208 ON _PGX	-2F RD OSC
TRIGGERING:			
SLOPE/SOURCE		CONNECTION	SIGNAL NAME
+INT CH1			

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:



10R168

Figure 4-22. Latched Read Data Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D023 ON _PGX	+NRZ RD DATA
CH 2	0.5 V/CM	TP-C833 ON _PGX	+RD CLK

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

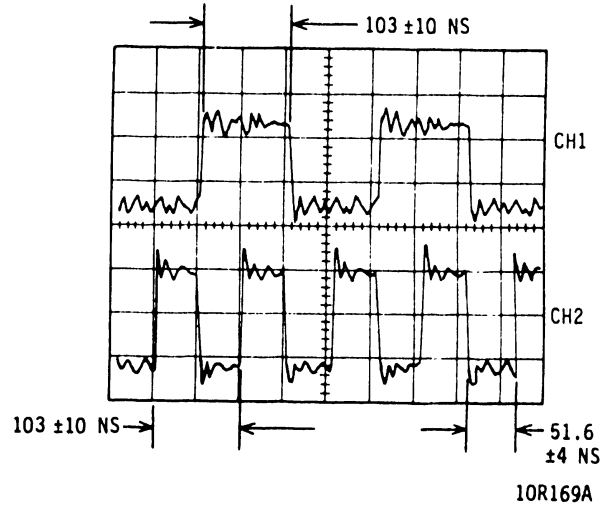


Figure 4-23. NRZ Read Data Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-B545 ON _PGX	-RD GATE
CH 2	2.0 V/CM	TP-A450 ON _PGX	-LOCK TO DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 μS/CM MODE: ALT

NOTES:

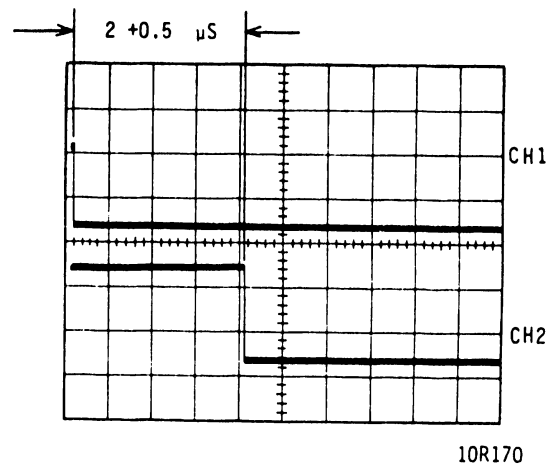


Figure 4-24. Read Gate to Lock to Data Timing

4403 - READ ADDRESS MARK CHECK

This procedure checks for the presence of address marks and verifies that the timing is correct.

CAUTION

To avoid possible loss of customer data, select a head and cylinder that will result in data being written on an unused track, or use a scratch pack.

1. Command continuous write and then read address mark operations using using a 1010.. pattern.
2. Connect oscilloscope as shown on figure 4-25.

NOTE

In "A Intensified" horizontal mode, the brightened marker highlights the segment of the sweep that is displayed later in "B Delayed" horizontal mode.

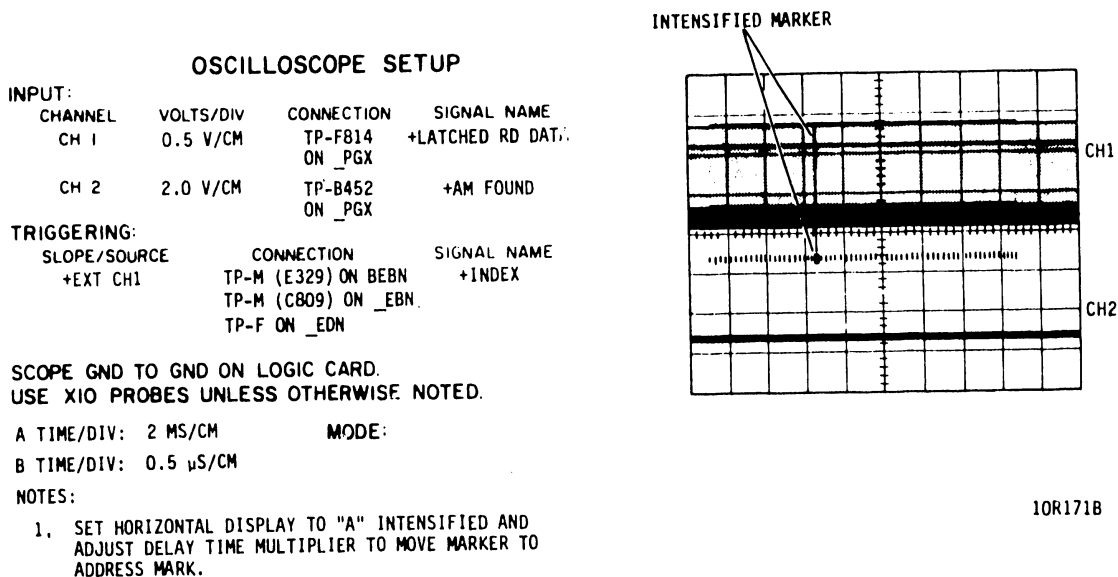


Figure 4-25. Scope Setup for AM Found Timing

3. Adjust DELAY TIME MULTIPLIER on oscilloscope to move intensified marker into data pattern (see figure 4-25). To minimize display instability, use first address mark area following index.
4. Referring to figure 4-26 position oscilloscope HORIZ DISPLAY switch to B DELAYED and TRIGGERING to +EXT CH I.
5. Check that the length of the address mark area is within the limits shown on figure 4-26. If it is outside these limits the address mark detection circuits may not function properly.
6. Observe that Address Mark Found goes active immediately following the address mark area.
7. Connect oscilloscope as shown on figure 4-27.
8. Observe that +Lock to Data goes active at the proper time (see figure 4-27).
9. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:			
CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-FB14 ON _PGX	+LATCHED RD DATA
CH 2	2.0 V/CM	TP-B452 ON _PGX	+AM FOUND
TRIGGERING:			
SLOPE/SOURCE		CONNECTION	SIGNAL NAME
+EXT CH1		TP-M (E329) ON BEBN TP-M (C809) ON _EBN TP-F ON _EDN	+INDEX

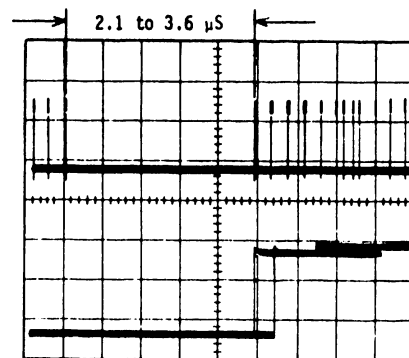
SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

A TIME/DIV: 2 NS/CM MODE:

B TIME/DIV: 0.5 μS/CM

NOTES:

1. SET HORIZONTAL DISPLAY TO "B" (DELAYED) AND ADJUST DELAY MULTIPLIER AS REQUIRED.



10R172B

Figure 4-26. AM Found Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-C644 ON _PGX	-AM ENABLE
CH 2	2.0 V/CM	TP-A450 ON _PGX	+LOCK TO DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 μ S/CM MODE: ALT

NOTES:

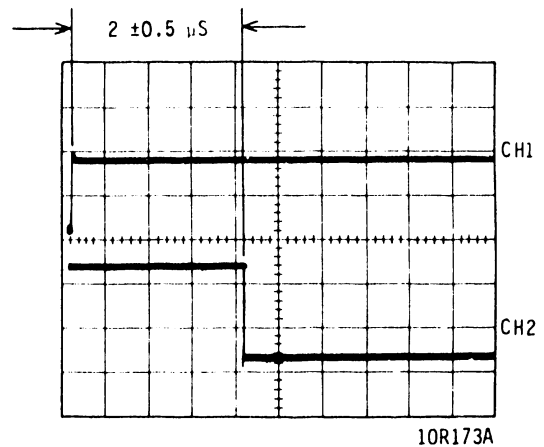


Figure 4-27. AM to Lock To Data Timing

MISCELLANEOUS LOGIC CHECKS

4501 - INDEX CHECK

This procedure checks that Index is present and has the proper pulse width. It also checks the time between successive Index pulses which is an indication of disk pack rotational speed.

1. Connect oscilloscope as shown on figure 4-28.
2. Observe that the Index pulse width is between 2.2 and 2.8 microseconds.
3. Connect oscilloscope as shown on figure 4-29.
4. Observe that the time between Index pulses is between 16.5 and 16.8 milliseconds.
5. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:
 CHANNEL VOLTS/DIV CONNECTION SIGNAL NAME
 CH 1 2.0 V/CM TP-M (E329) ON BEBN +INDEX
 TP-M (C809) ON _EBN
 TP-F ON _EDN

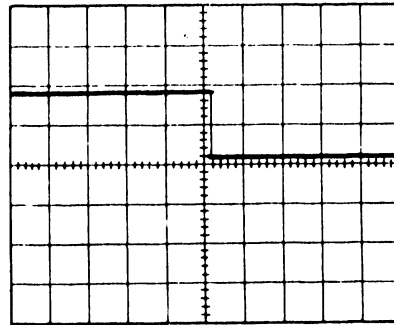
CH 2

TRIGGERING:
 SLOPE/SOURCE CONNECTION SIGNAL NAME
 +INT CH1

SCOPE GND TO GND ON LOGIC CARD.
 USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 μ S/CM MODE:

NOTES:



10R174A

Figure 4-28. Index Pulse Timing

OSCILLOSCOPE SETUP

INPUT:
 CHANNEL VOLTS/DIV CONNECTION SIGNAL NAME
 CH 1 2.0 V/CM TP-M (E329) ON BEBN +INDEX
 TP-M (C809) ON _EBN
 TP-F ON _EDN

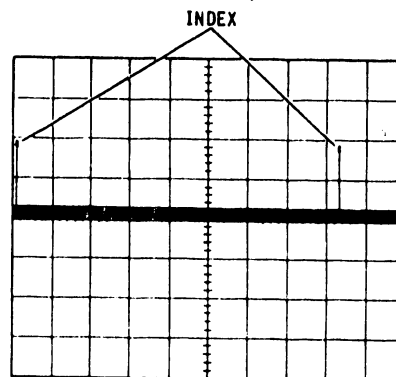
CH 2

TRIGGERING:
 SLOPE/SOURCE CONNECTION SIGNAL NAME
 +INT CH1

SCOPE GND TO GND ON LOGIC CARD.
 USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 2 MS/CM MODE:

NOTES:



10R175 A

Figure 4-29. Index to Index Timing

4502 - SECTOR CHECK

This procedure checks for the presence of sector pulses and that they have the proper width.

1. Connect oscilloscope as shown on figure 4-30.
2. Observe that the Sector pulse width is between 1.05 and 1.45 microseconds.
3. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

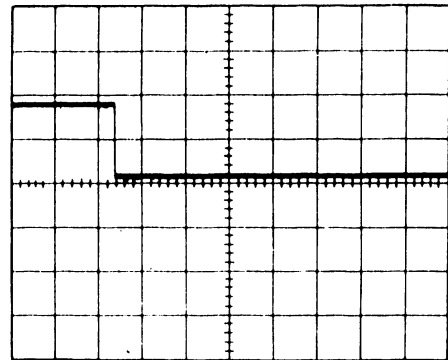
INPUT:			
CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/cm	TP-J716 (Z)	+SECTOR
		ON _PEX	
CH 2			

TRIGGERING:		
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 μ S/CM MODE:

NOTES:



10R252

Figure 4-30. Sector Pulse Timing

SECTION

5

REPAIR

AND

REPLACE-

MENT

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

Repair of the drive is limited to replacement of defective parts and assemblies. This section describes removal and replacement and, where applicable, adjustment of all major field replaceable parts and assemblies. The information here should be used in conjunction with that in the parts data section of Hardware Maintenance Volume 1.

If adjustments are required as a result of replacing a part, it is specified in the replacement procedure. If an adjustment is included, and there is some doubt as to the need for replacement, perform the adjustment prior to replacing the part.

The procedures in this section assume that the drive is mounted on slides in an equipment rack or cabinet. But unless otherwise specified, it is not necessary to remove the drive from the slides to perform maintenance. All procedures require that power be removed from the drive and power supply. The person performing the maintenance should be familiar with the operation of the drive and with all information in the general maintenance section of this manual (particularly the warnings and precautions).

Each procedure is assigned a unique number. The numbers are used elsewhere in the manual to reference the procedures. The procedures and numbers are organized into three categories: 51XX - mechanical, 52XX - electromechanical, and 53XX - electronic (circuit boards).

The procedures appear in the following order:

- 5101 - Entire Drive Removal & Replacement
- 5102 - Top Cover Removal & Replacement
- 5103 - Front Panel Removal & Replacement
- 5104 - Slide Removal & Replacement
- 5105 - Absolute Filter Removal, Replacement & Testing
- 5201 - Fan Removal & Replacement
- 5202 - _PBX Operator Panel Removal & Replacement
- 5203 - Power Supply Removal & Replacement
- 5204 - Magnet Removal & Replacement
- 5205 - Coil Assembly Removal, Replacement & Alignment
- 5206 - Carriage Removal & Replacement
- 5207 - Upper & Lower Rails Removal & Replacement
- 5208 - Rails & Bearings Inspection & Cleaning
- 5209 - Motor & Cable Assembly Removal & Replacement
- 5210 - Spindle Removal, Replacement & Adjustment
- 5211 - Spindle Lockshaft Adjustment
- 5212 - Head Arm Removal, Replacement & Alignment
- 5213 - Heads Loaded Switch Removal, Replacement & Adjustment
- 5214 - Pack in Place & Write Protect Switches Removal, Replacement & Adjustment
- 5215 - Door Unlock Solenoid Removal, Replacement & Adjustment
- 5216 - Door Locked Switches Removal, Replacement & Adjustment

- 5301 - _PGX Board Removal & Replacement
- 5302 - _PFX Board Removal & Replacement
- 5303 - _EBN/_EDN Board Removal & Replacement
- 5304 - _PEX Board Removal & Replacement
- 5305 - _PCX Board Removal & Replacement
- 5306 - _UUN Board Removal & Replacement
- 5307 - _PDX Board Removal & Replacement
- 5308 - _PMX Board Removal & Replacement

5101 - ENTIRE DRIVE REMOVAL & REPLACEMENT

The following procedure provides instructions for removing and replacing the entire drive and assumes that the drive is mounted on slides in an equipment rack. If the drive is to be replaced with another and the inner slides are required for the replacement unit, see procedure 5104 - Slide Removal and Replacement procedure. Two persons may be required to lift the drive on and off the slide assemblies.

REMOVAL

1. Perform power supply removal procedure (proc 5203).
2. Disconnect I/O cables from J2, J3, and J4 on drive.
3. Press slide lock release and pull drive from slide assemblies.
4. Move drive to desired location.

MOUNTING

1. Going to the equipment rack, push intermediate slides to fully retracted positions inside outer slides. Refer to figure 5-3.
2. Lift drive into position in front of rack and guide inner slides into intermediate slides. Push until lock releases engage, then pull drive to fully extended position.

3. Connect I/O cables to drive connectors J2, J3, and J4.
4. Perform power supply replacement procedure (proc 5203).

5102 - TOP COVER REMOVAL & REPLACEMENT

REMOVAL

CAUTION

With the top cover removed, electrostatic sensitive components are exposed and may be seriously damaged by static electricity. To avoid possible damage, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual.

1. Extend drive to fully extended position.
2. Remove power from drive as follows:
 - a. Press START switch to release it from Start position.
 - b. Wait for Ready indicator to stop flashing, then set CBI to OFF.
3. Loosen screws securing bottom edge of cover to drive.

CAUTION

Cover must be carefully lifted from the center to avoid possible damage to adjacent components.

4. Carefully lift off cover.

REPLACEMENT

CAUTION

When replacing cover, use care to avoid damaging logic boards.

1. Carefully place cover on drive.
2. Tighten screws to secure cover to drive.
3. Push drive back to closed position in rack.

5103 - FRONT PANEL REMOVAL & REPLACEMENT

REMOVAL (S/C 01)

1. Perform operator panel removal procedure (proc 5202).
2. Open pack access door and remove screws securing both sections of front panel to drive. Remove panels from drive. See figure 5-1.
3. Loosen hardware securing filter, retaining screen and retaining clips.
4. Rotate retaining clips and remove retaining screen and filter from panel.

REPLACEMENT (S/C 01)

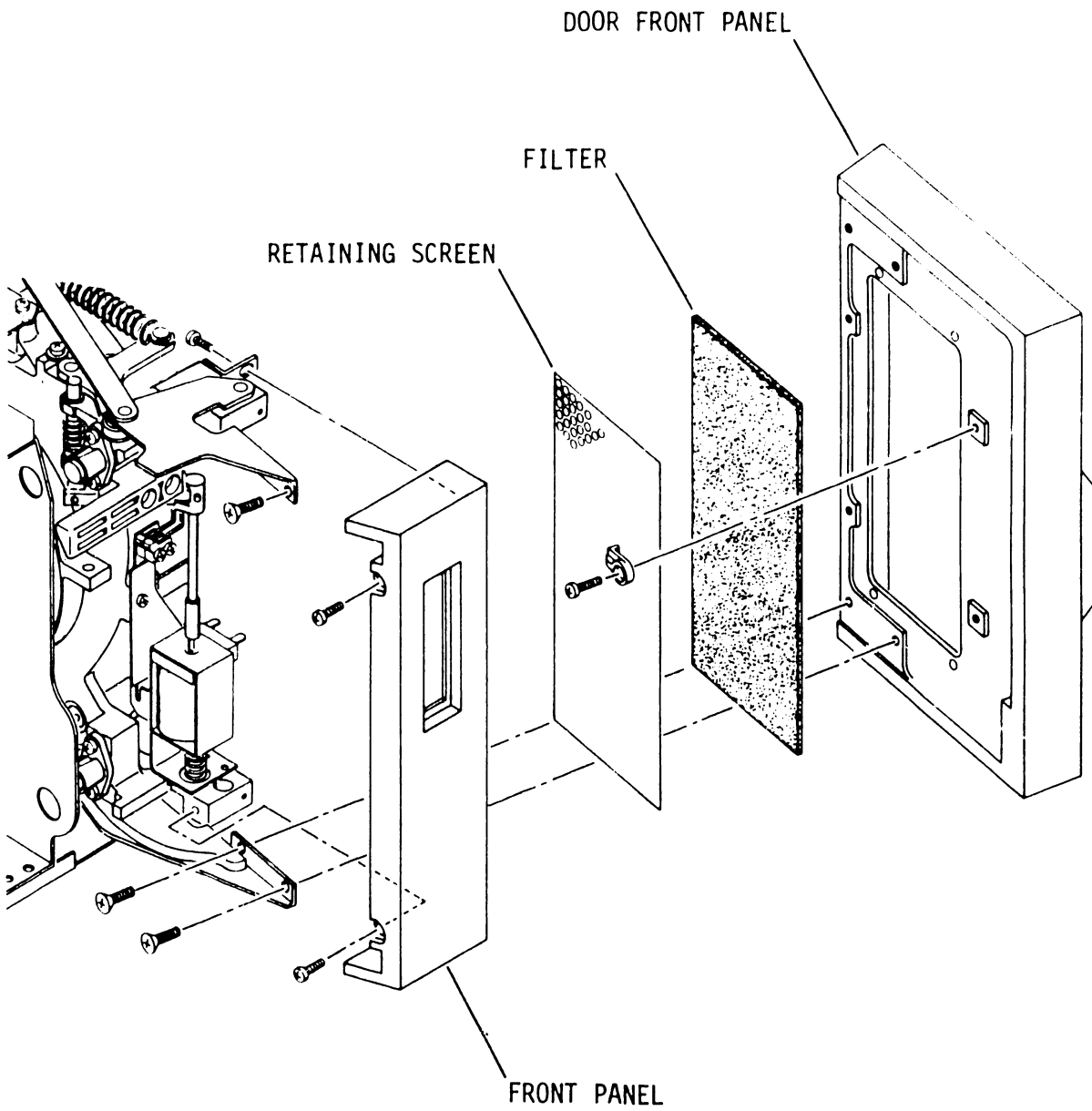
1. Install filter into front panel.
2. Loosely, install right panel, then left panel.
3. Align both sections of front panel to drive, install screws and fasten securely. See figure 5-1
4. Perform operator panel replacement procedure (proc 5202).

REMOVAL (S/C 02 & ABV)

1. Remove front panel insert by pulling forward to disengage catches that hold the insert in the front panel. See figure 5-2.
2. Remove primary filter.
3. Remove screws securing both front panel sections to drive and lift panel off drive.

REPLACEMENT (S/C 02 & ABV)

1. Put front panel in place (centered over switches), insert screws and fasten securely
2. Install primary filter.
3. Replace front panel insert, by aligning catches to slots in front panel and pushing on insert until catches snap into place.



10R209

Figure 5-1. Front Panels Replacement (S/C 01)

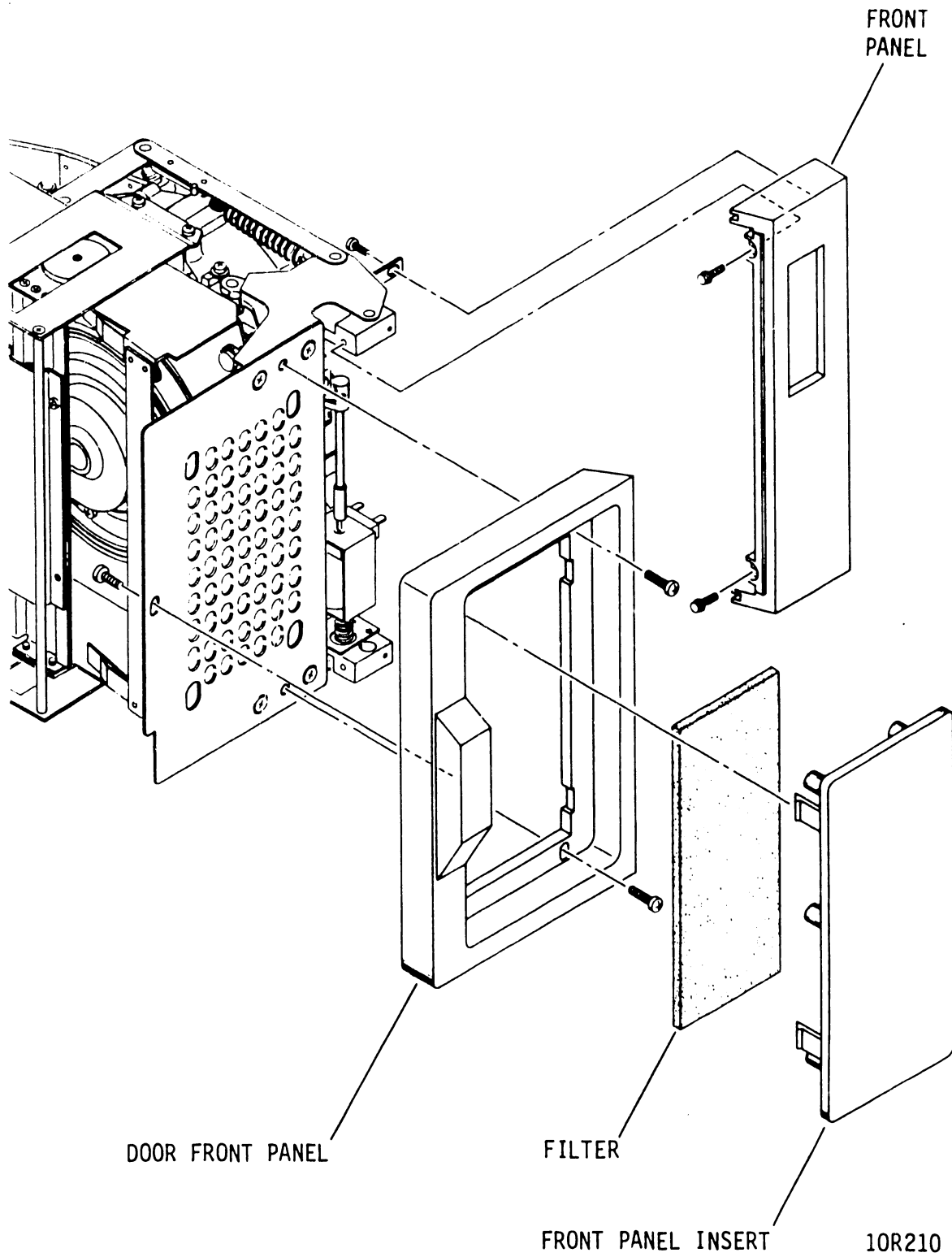


Figure 5-2. Front Panels Replacement (S/C 02 & Above)

5104 - SLIDE REMOVAL & REPLACEMENT

This procedure describes how to remove and replace the inner slide assemblies. This procedure is used to replace a defective inner slide or if the inner slides must be removed from one drive and installed on another.

REMOVAL

1. Perform Entire Drive Removal procedure (proc 5101).
2. Remove power supply mounts (if used) by removing attaching hardware.
3. Remove screws securing inner slide to drive. Remove insulator and slides. See figure 5-3.

REPLACEMENT

1. Mount inner slides and insulator on drive by installing screws through holes in inner slides into square nuts in drive. Figure 5-3 defines which slide component is used on the right-hand side of the drive.
2. Install power supply mounts (if used) with attaching hardware.
3. Perform Entire Drive Replacement procedure (proc 5101).

5105 - ABSOLUTE FILTER REMOVAL, REPLACEMENT & TESTING

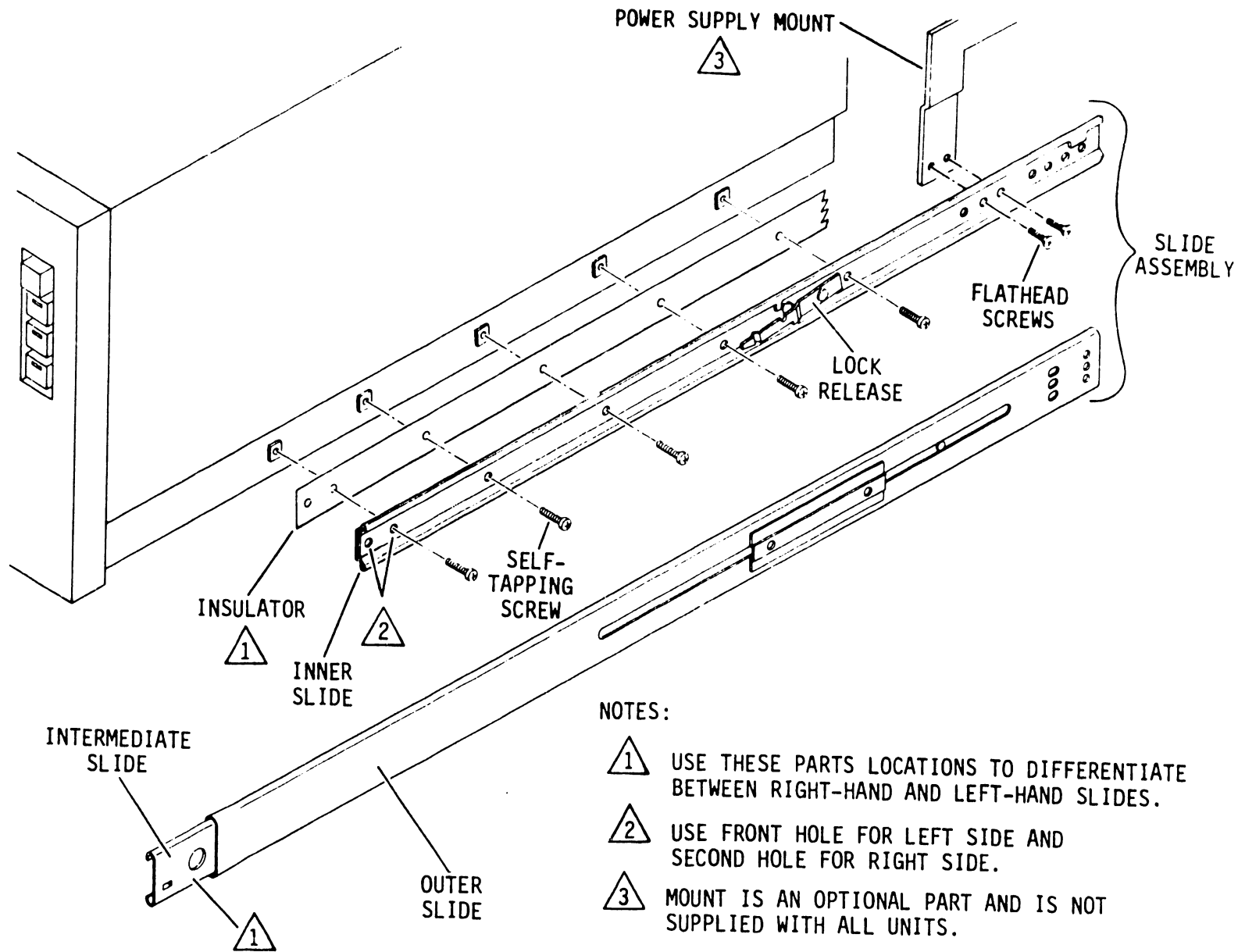
An adequate supply of clean air to the pack area is essential for proper operation of the drive. The absolute filter traps all dirt particles too small to be stopped by the primary filter. If the filter becomes too clogged to yield a sufficient airflow, it must be replaced. Its useful life depends on the drives operating environment.

TESTING

Perform the following procedure whenever there is doubt about the ability of the filter to pass air into the pack receiver area. Refer to table 2-1, Maintenance Tools and Materials for differential pressure gauge part number.

1. Extend drive to fully extended position
2. Install pack and apply power to drive.

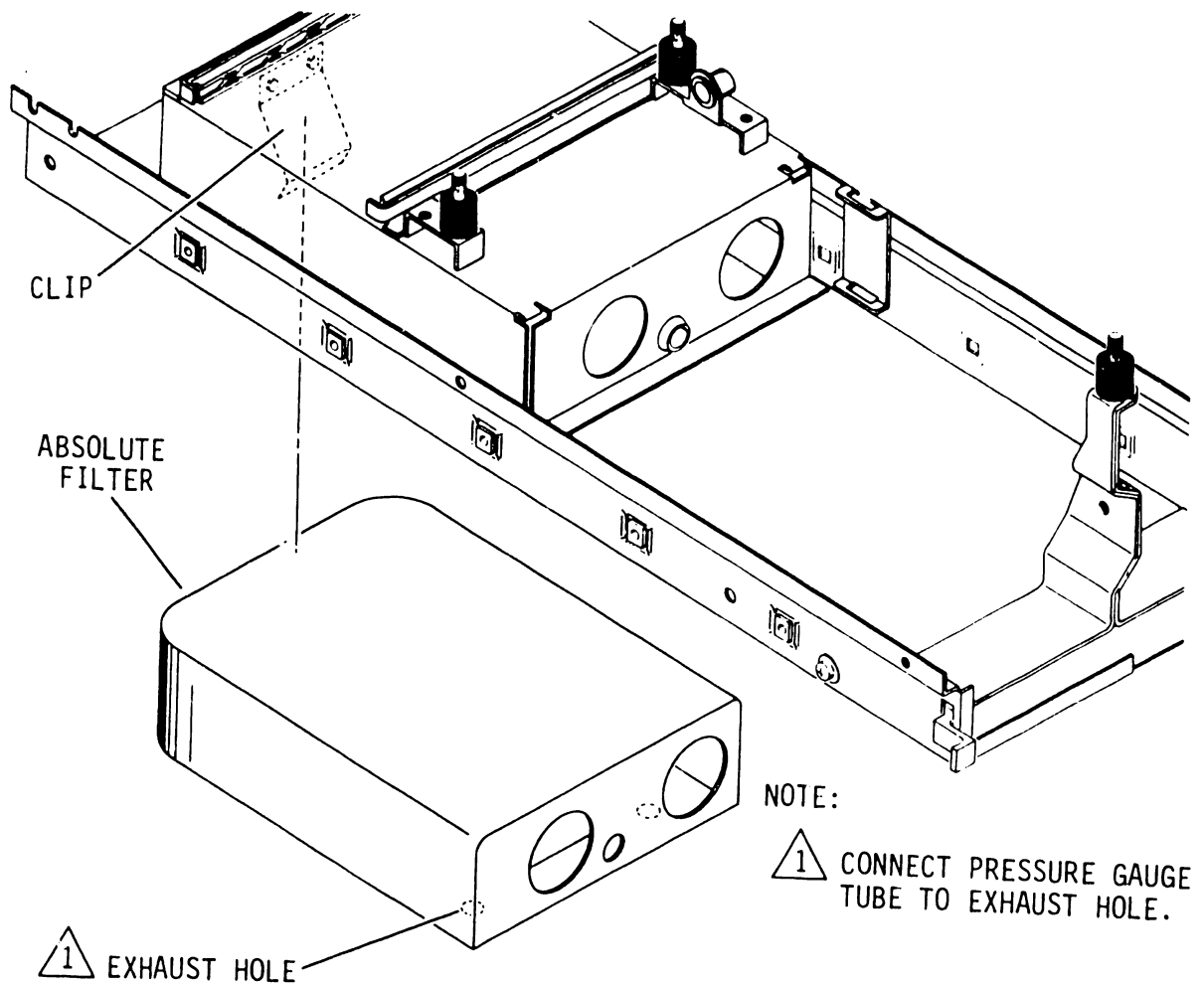
Figure 5-3. Slide Removal and Replacement



NOTES:

- ① USE THESE PARTS LOCATIONS TO DIFFERENTIATE BETWEEN RIGHT-HAND AND LEFT-HAND SLIDES.
- ② USE FRONT HOLE FOR LEFT SIDE AND SECOND HOLE FOR RIGHT SIDE.
- ③ MOUNT IS AN OPTIONAL PART AND IS NOT SUPPLIED WITH ALL UNITS.

3. Remove plastic plug from absolute filter exhaust hole. See figure 5-4.
4. Ensure heads are on cylinder 0.
5. Insert tubing (attached to pressure gauge) into filter exhaust hole. Pressure should be greater than 0.1 inch-water with top cover installed or 0.2 inch-water with top cover removed.
6. If pressure is less than amount specified in step 5, replace absolute filter.



10R238

Figure 5-4. Absolute Filter Replacement and Testing

7. Install top cover.
8. Remove tubing from filter exhaust hole and replace plastic plug.

REMOVAL

1. Extend drive to fully extended position.
2. Insert a flat-blade screwdriver (or equivalent) into clip securing absolute filter. See figure 5-4.
3. Pry the clip back and remove absolute filter.

REPLACEMENT

1. Extend drive to fully extended position.
2. Install absolute filter through bottom of drive as shown in figure 5-4.
3. Install top cover, if previously removed.
4. Push drive back to closed position in rack.

5201 - FAN REMOVAL & REPLACEMENT

REMOVAL

1. Perform Top Cover Removal procedure (proc 5102).
2. Disconnect cable from J48 on I/O board.

NOTE

Cable J38 from DC harness to fan is used on older units only.

3. Disconnect cable from J38 on fan (if used).
4. On units with power supply attached directly to slides, remove screws securing front of power supply to slides and tilt supply back far enough to allow access to hardware securing fan to rear panel. On units with power supply attached to bracket and mounts, remove hardware securing bracket to mounts, and slide supply back far enough to allow access to fan hardware.

5. Hold fan and remove screws securing outer finger guard and fan to rear panel. See figure 5-5.
6. Remove guard and lift fan up and out of rear panel.
7. Remove hardware that secures inner finger guard to fan and remove guard from fan.

REPLACEMENT

CAUTION

Installing fan backwards or reversing fan leads will result in improper airflow. This will cause overheating and premature component failure.

1. Install inner finger guard on fan.

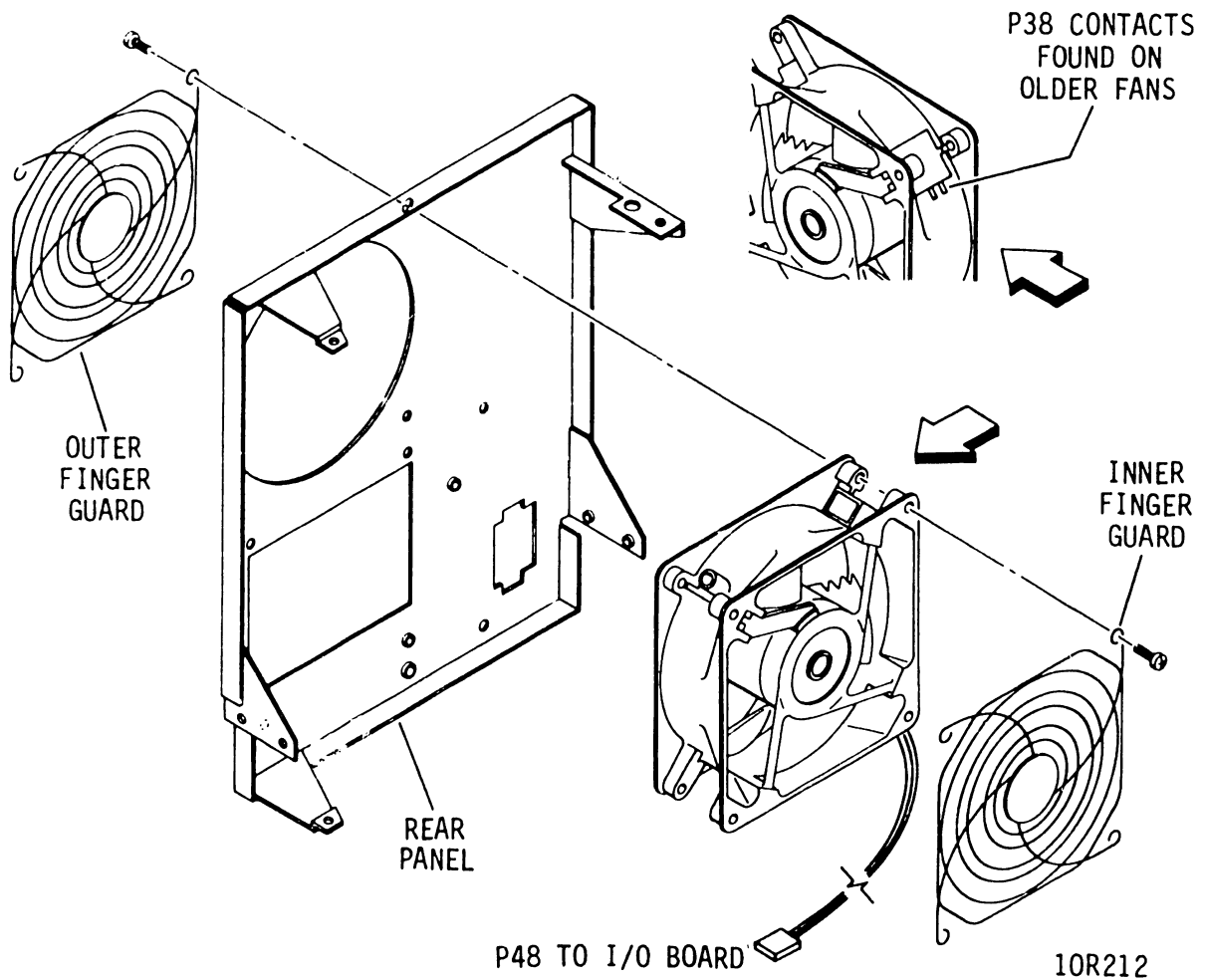


Figure 5-5. Fan Removal and Replacement

2. Orient fan so P48 cable is on left bottom when facing rear of drive. See figure 5-5.
3. Align outer finger guard outside and fan to inside of rear panel, then install and tighten screws.
4. On older fans, connect P38 wires to fan ensuring that black wire goes to + terminal and blue wire to - terminal.
5. Connect cable J48 to I/O board.
6. Move power supply into operating position. Install and tighten mounting screws.
7. Perform Top Cover Replacement procedure (proc 5102).

5202 - --PBX OPERATOR PANEL REMOVAL AND REPLACEMENT

The operator panel cannot be repaired and, except for the lenses, must be replaced as an assembly. The lenses can be replaced separately and are removed by carefully prying them from the switches. See figure 5-6. The following describes removal and replacement of the entire operator panel.

REMOVAL

1. Perform Top Cover Removal procedure (proc 5102).
2. Remove power from drive as follows:
 - a. Press START switch to release it from Start position.
 - b. Wait for Ready indicator to stop flashing, then set CBI to OFF.
3. Remove the screws securing read/write boards to vertical and rear panel support brackets (proc 2101). Swing boards up and lock into place.
4. Open front door and disconnect P26 from _PEX board and remove cable from cable clips.
5. Depress retainer springs on operator panel switches and push forward to remove entire assembly from front panel. See figure 5-6.

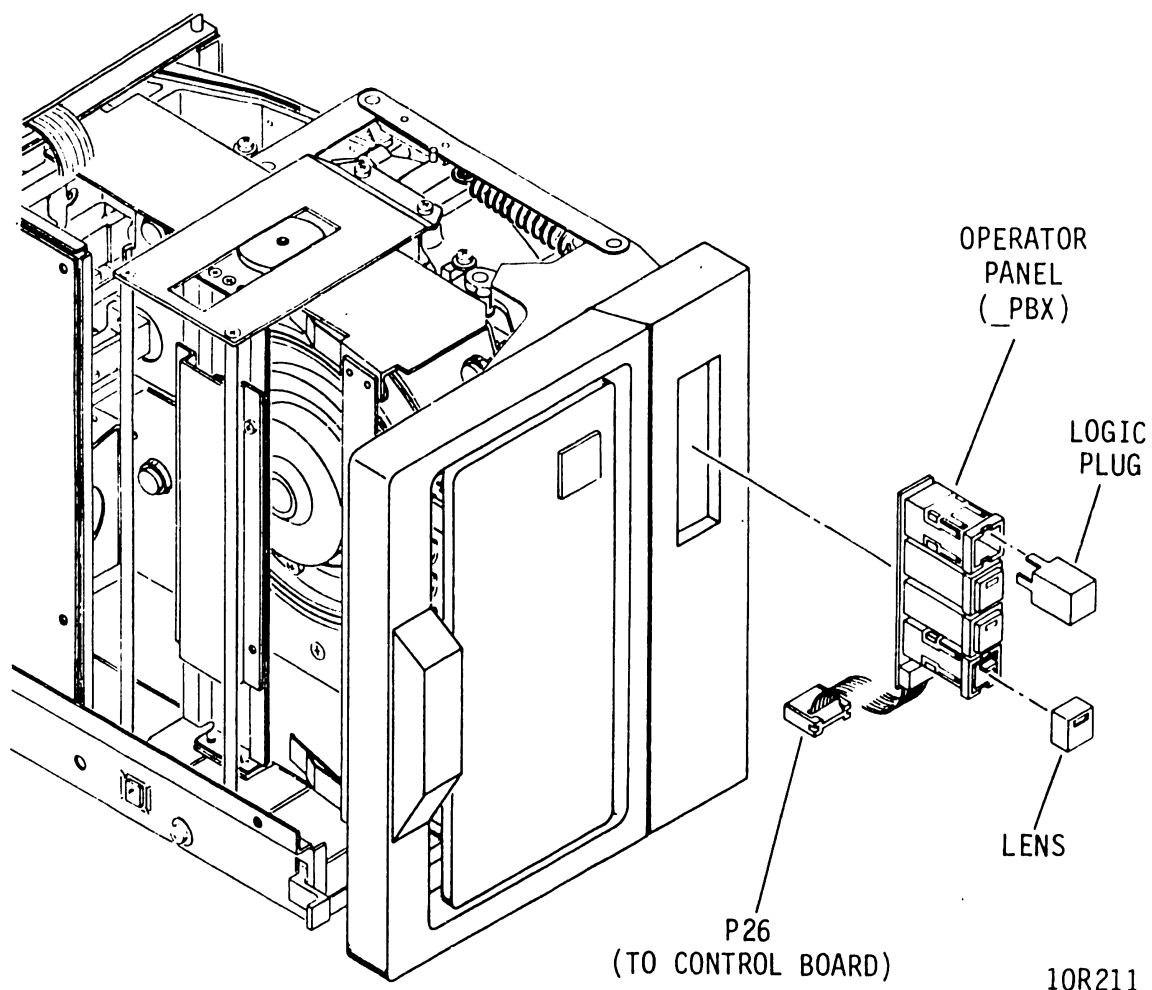


Figure 5-6. Operator Panel Removal and Replacement

REPLACEMENT

1. Thread P26 and cable through bracket and hole in front panel.
2. Snap operator panel assembly into place in front panel. See figure 5-6.
3. Connect P26 to J26 on _PEX board.
4. Carefully route P26 cable along cable clips and secure into place.
5. Return read write/boards to down position and secure into place.
6. Perform Top Cover Replacement procedure (proc 5102).

5203 - POWER SUPPLY REMOVAL & REPLACEMENT

The following procedure provides instructions for removing and replacing the power supply when it is slide mounted behind the drive. See figure 5-7. A second person may be needed to support the power supply while the mounting hardware is being removed and installed.

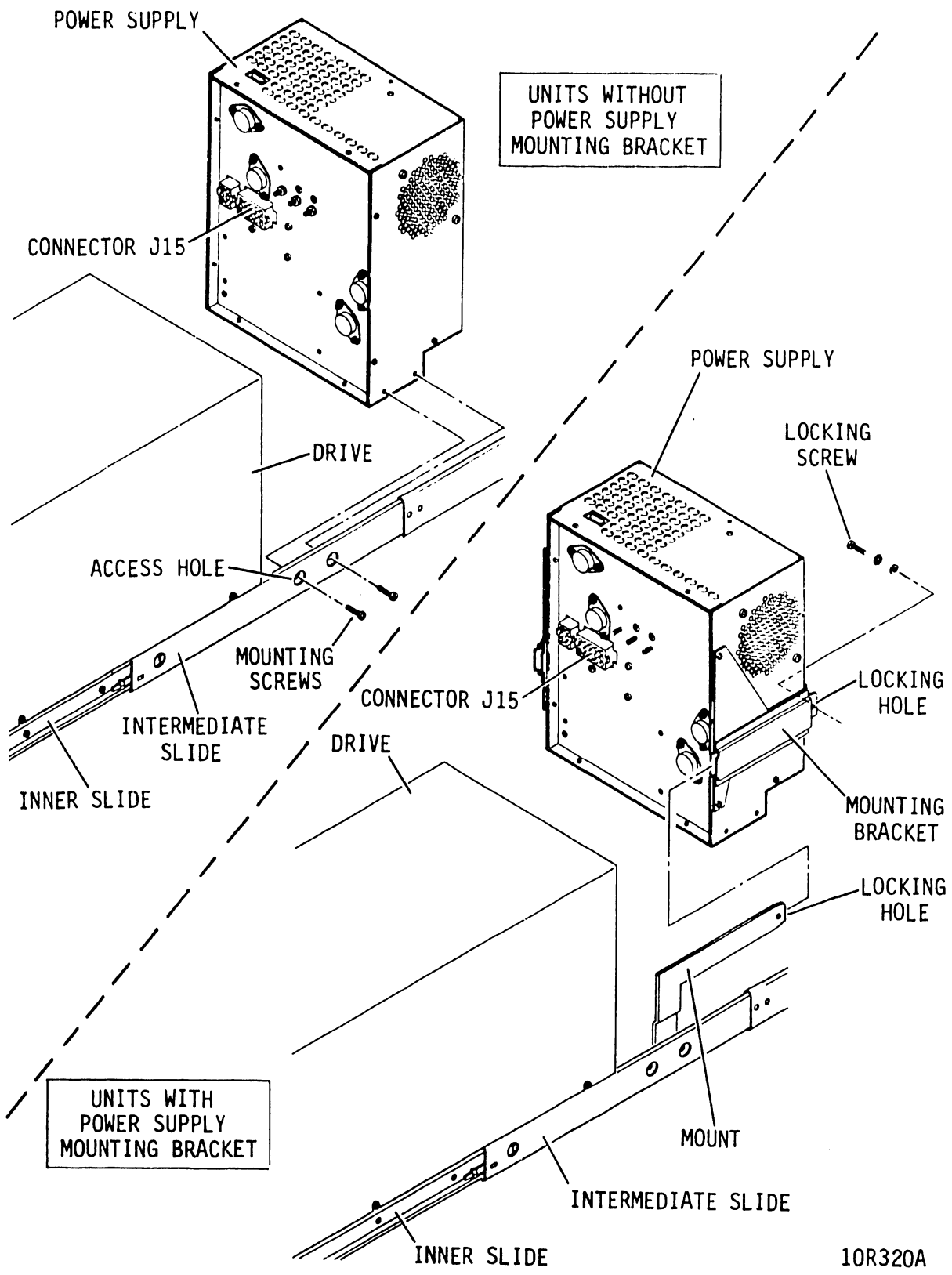
REMOVAL

1. Lift cabinet latch and pull drive to fully extended position.
2. Remove power from drive as follows:
 - a. Press START switch to release it from Start position.
 - b. Wait for Ready indicator to stop flashing, then set CBI to OFF.
3. Disconnect ac power cable from AC INPUT connector J1 on power supply.
4. On units with power supply attached directly to slides, remove screws securing front of power supply to slides and tilt supply back far enough to allow access to J40 on drive. On units with power supply attached to bracket and mounts, remove hardware securing bracket to mounts and slide supply back far enough to allow access to J40 on drive.
5. Disconnect ground wire from back panel and dc power cable from J40 on drive and J15 on power supply.
6. On units with power supply attached directly to slides, press slide lock releases and pull drive forward just far enough to allow access to power supply rear mounting screws. Remove rear mounting screws.

CAUTION

After removing supply, push drive back into rack unless replacement supply is to be installed immediately.

7. Remove power supply.



UNITS WITH
POWER SUPPLY
MOUNTING BRACKET

UNITS WITHOUT
POWER SUPPLY
MOUNTING BRACKET

10R320A

Figure 5-7. Power Supply Removal and Replacement

REPLACEMENT (UNITS WITHOUT MOUNTING BRACKET)

1. Press slide lock releases and pull drive forward just enough to allow power supply rear mounting screws to be installed.
2. Align holes in slides to those in power supply, then install and tighten power supply rear mounting screws. See figure 5-7.
3. Push drive back into rack until slide lock releases engage.
4. Tilt supply back and connect ground wire to back panel and dc power cable between J40 on drive and J15 on supply.
5. Install and tighten power supply front mounting screws.
6. Connect ac power cable to AC INPUT connector J1.
7. Push drive back to closed position in rack.

REPLACEMENT (UNITS WITH MOUNTING BRACKET)

1. Position power supply so that mounts and matching slots in bracket are aligned as shown in figure 5-7. Slide power supply toward drive until locking holes in bracket align with locking holes in mounts.
2. Connect dc power cable between J40 on drive and J15 on supply.
3. Secure supply bracket to mounts with mounting hardware.
4. Connect ac power cable to AC INPUT connector J1.
5. Push drive back to closed position in rack.

5204 - MAGNET REMOVAL & REPLACEMENT

REMOVAL

1. Remove power from drive as follows:
 - a. Press START switch to release it from Start position.
 - b. Wait for Ready indicator to stop flashing, then set CBI to OFF.

2. Disconnect I/O cables, ground wire from back panel and DC power cable (J40) from drive.
3. Remove main logic and rear panel assembly from drive (proc 2102).

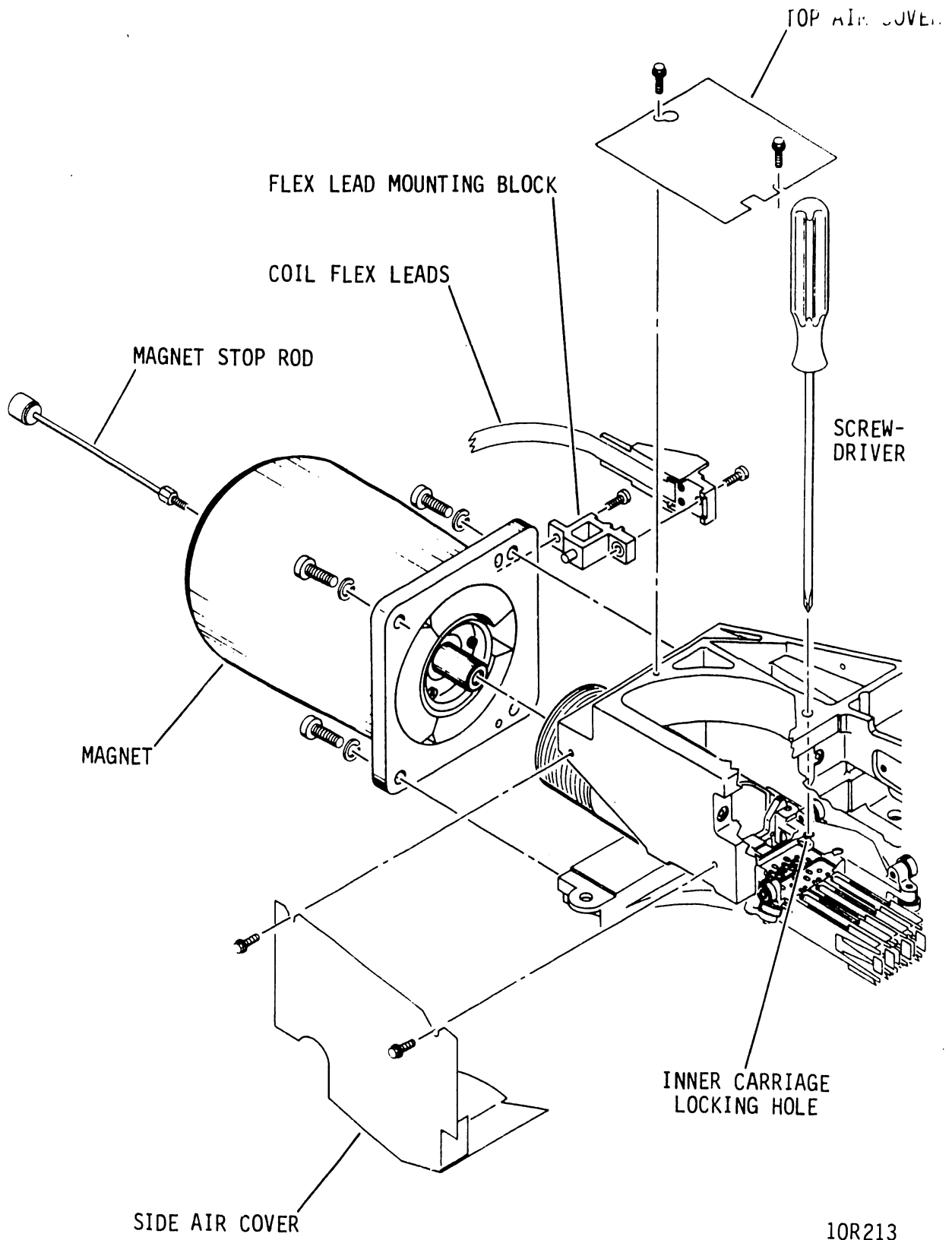
CAUTION

While the heads are fully extended into the pack area, do not attempt to open pack access door. Damage to heads will result.

4. Remove top and side air covers.
5. Manually release carriage lock, fully extend heads into pack area and install a screwdriver into inner carriage locking hole. See figure 5-8.
6. Remove magnet air return cover.
7. Loosen screw securing coil flex leads to the mounting block and carefully slide leads out of block.
8. Loosen magnet stop rod using a flatblade screwdriver (access stop rod from rear center of magnet). Remove stop rod from drive.
9. Remove screws securing magnet to carriage housing.
10. Remove flex lead mounting block from magnet.
11. Carefully remove magnet from carriage housing.

REPLACEMENT

1. Ensure that the carriage is fully extended into inner pack area (see Removal procedure step 4).
2. Attach magnet to housing with allen screws.
3. Attach flex lead mounting block to new magnet. See figure 5-8.
4. Install magnet stop rod.
5. Remove screwdriver from inner track locking hole and retract heads to unloaded position.
6. Install coil flex leads to mounting block.



10R213

Figure 5-8. Magnet Removal and Replacement

7. Install magnet air return cover.
8. Install top and side air covers.
9. Replace main logic and rear panel assembly (proc 2102).
10. Connect I/O cables, ground wire to back panel and DC power cable (J40) to drive.

5205 - COIL ASSEMBLY REMOVAL, REPLACEMENT & ALIGNMENT

The coil alignment fixture (see table 2-1, Maintenance Tools and Materials) must be used whenever the coil is replaced or alignment is necessary.

REMOVAL

1. Perform magnet removal procedure (proc 5204).
2. Remove allen screws securing coil to the carriage. See figure 5-9.
3. Remove coil from carriage.

REPLACEMENT & ALIGNMENT

1. Position coil on carriage and loosely fasten with allen screws. See figure 5-9.

NOTE

Do not tighten allen screws until after coil alignment has been completed.

2. Position coil alignment fixture on the magnet locating pins (adjacent to the deck casting). See figure 5-10.
3. Depress carriage lock and extend coil until coil bobbin passes through fixture.
4. Center coil in the coil alignment fixture, so that the bobbin does not rub when coil is moved back and forth.
5. When coil is centered, tighten coil allen screws to 0.9 N·m (6 lbf·in), then recheck coil for free movement.

6. Fully extend carriage and lock into position.
7. Remove coil alignment fixture and perform Magnet Replacement procedure (proc 5204).

5206 - CARRIAGE REMOVAL & REPLACEMENT

The Carriage Removal & Replacement procedure must be performed in a clean environment. Care must be taken to ensure that there are no foreign particles on carriage bearings, rails, or tools to be used.

REMOVAL

1. Perform Magnet Removal procedure (proc 5204).
2. Perform Head Arm Removal procedure (proc 5212).

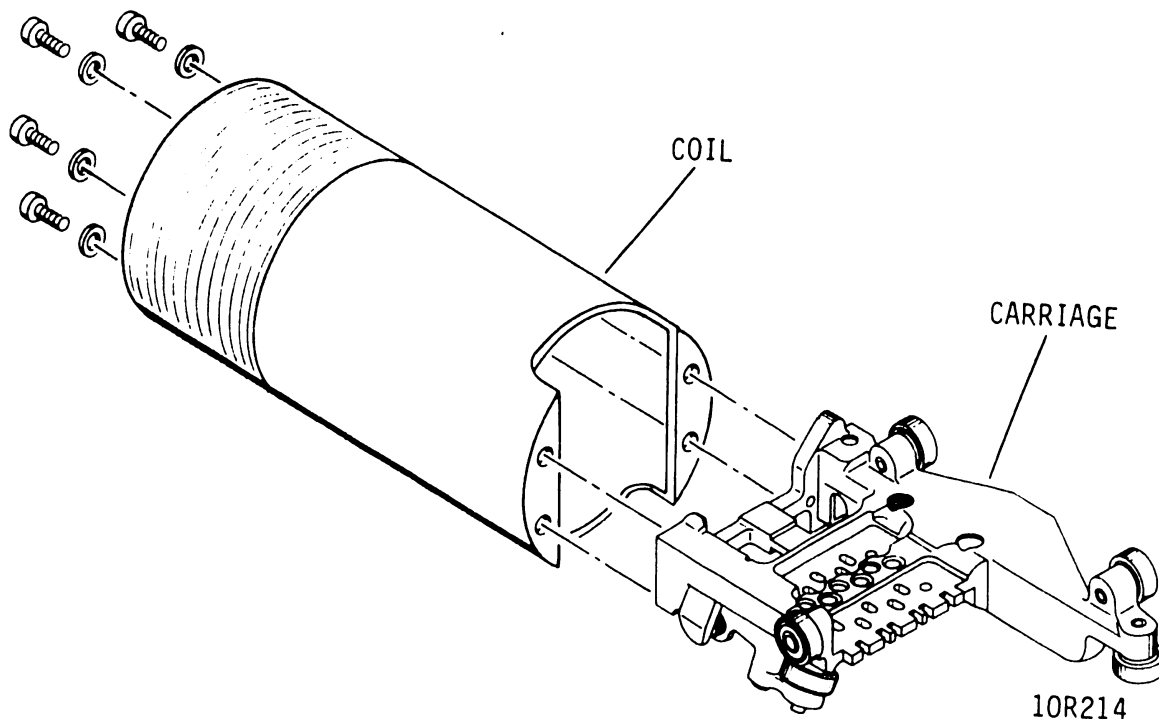
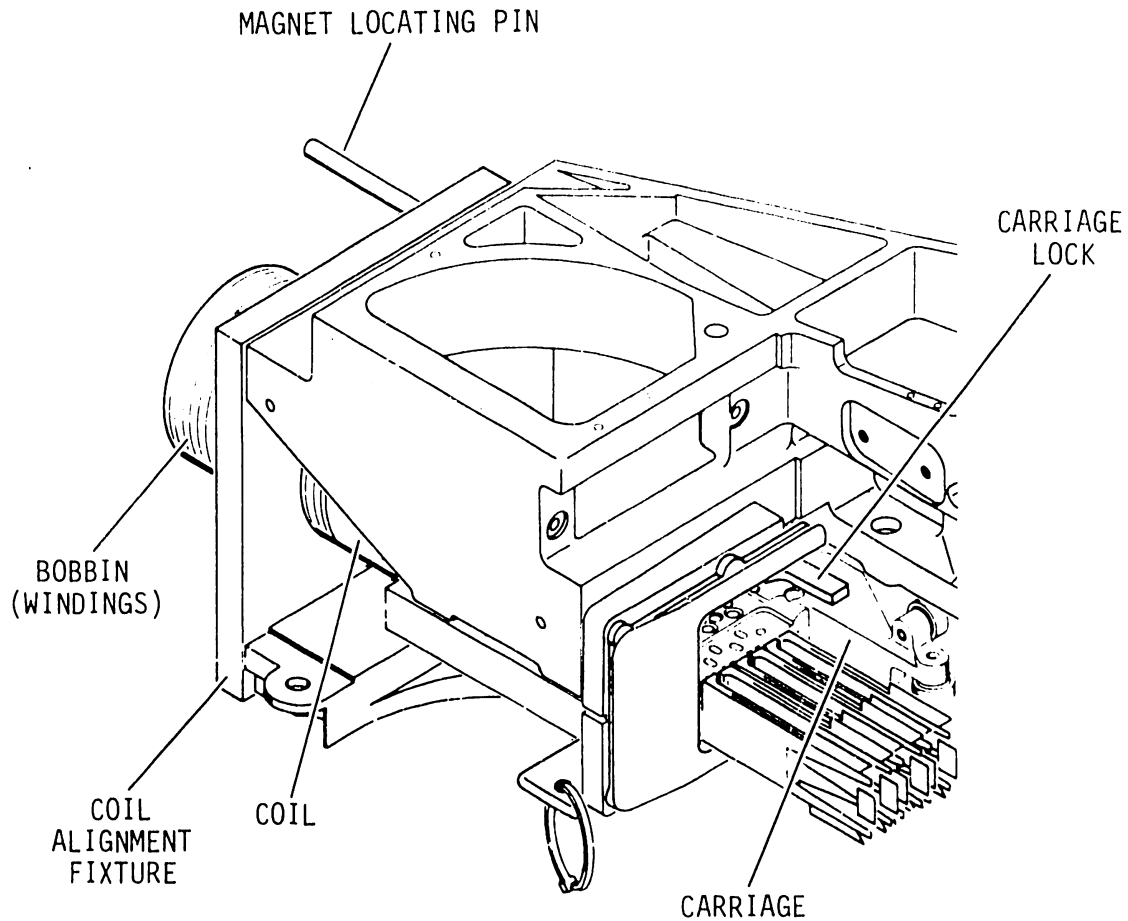


Figure 5-9. Coil Assembly Removal and Replacement



10R215

Figure 5-10. Coil Alignment

3. Disconnect carriage ground strap from housing. See figure 5-11.
4. Carefully remove carriage and coil assembly from housing.
5. Remove ground strap from carriage.
6. Remove allen screws securing coil to carriage and remove coil.

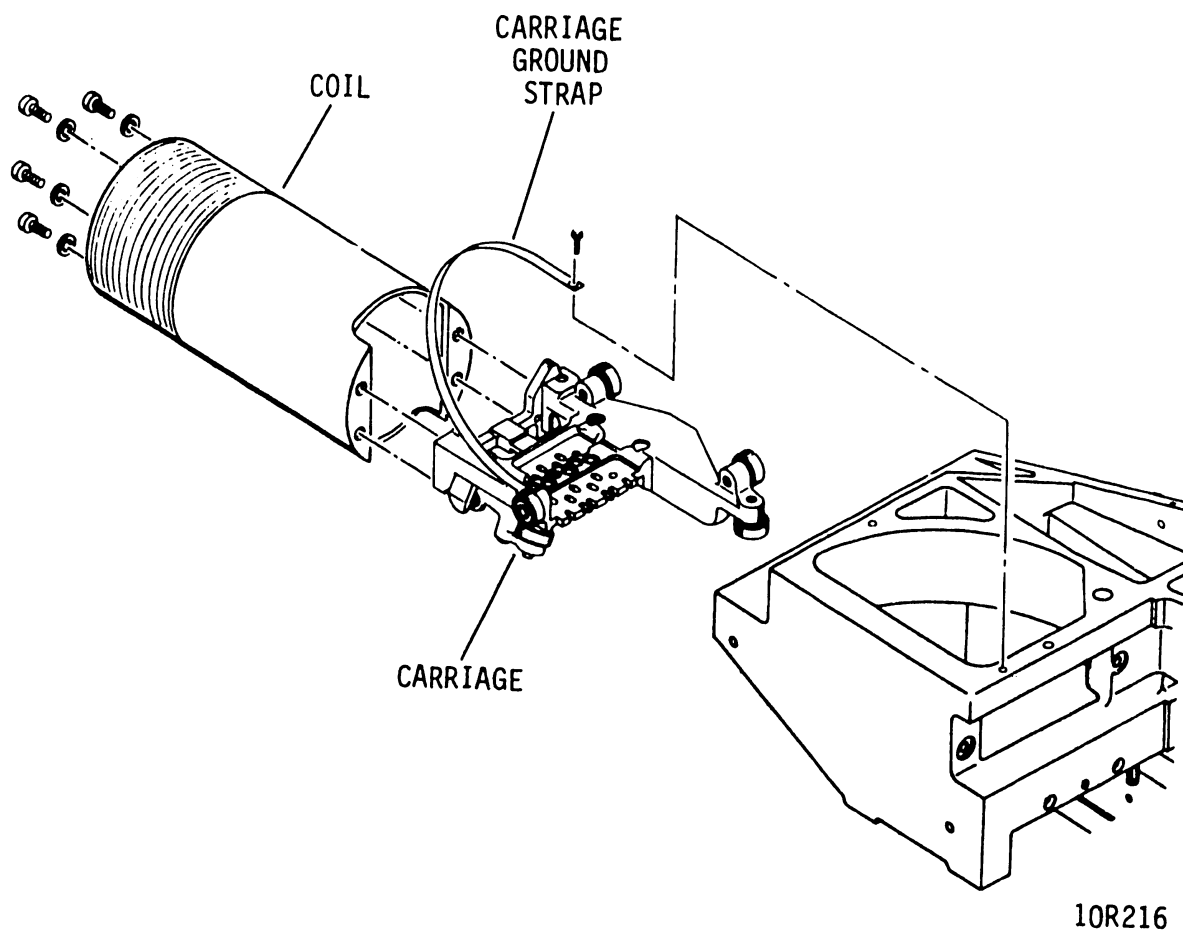


Figure 5-11. Carriage Removal and Replacement

REPLACEMENT

1. Loosely attach coil to carriage with allen screws. See figure 5-11.
2. Attach ground strap to carriage.
3. Carefully install carriage and coil assembly into housing.

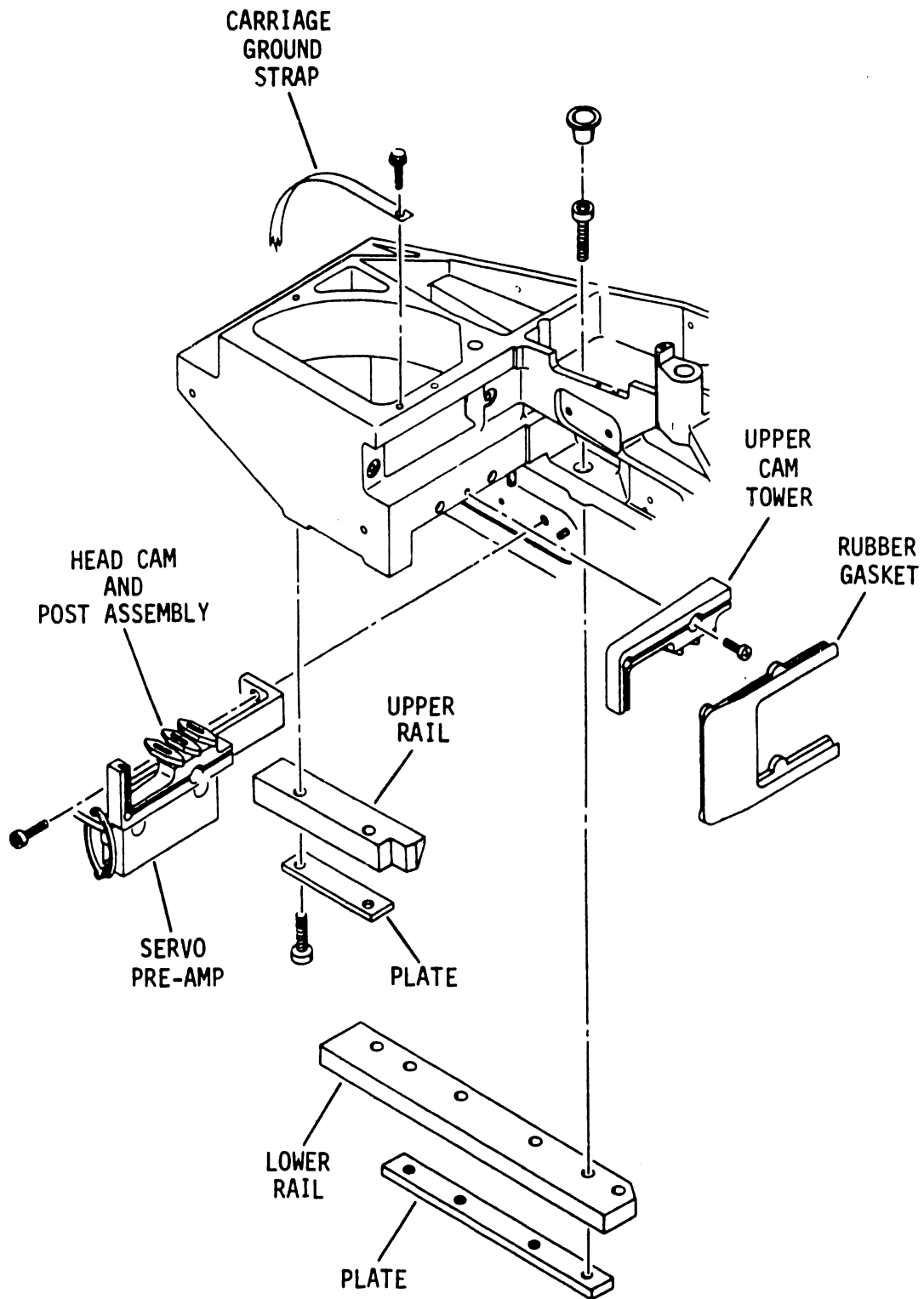
4. Perform head arm replacement procedure (proc 5212).
5. Connect carriage ground strap to housing.
6. Align coil to carriage as shown in the coil replacement and alignment procedure (proc 5205).
7. Perform magnet replacement procedure (proc 5204).
8. Perform head alignment procedure (proc 5212).

5207 - UPPER & LOWER RAILS REMOVAL & REPLACEMENT

Removal and replacement of rails must be performed in a clean environment and care must be taken to ensure that no particles are allowed on the spindle, rails, or tools to be used. Rail alignment fixtures (see table 2-1, Maintenance Tools and Materials) are necessary to perform rail alignment.

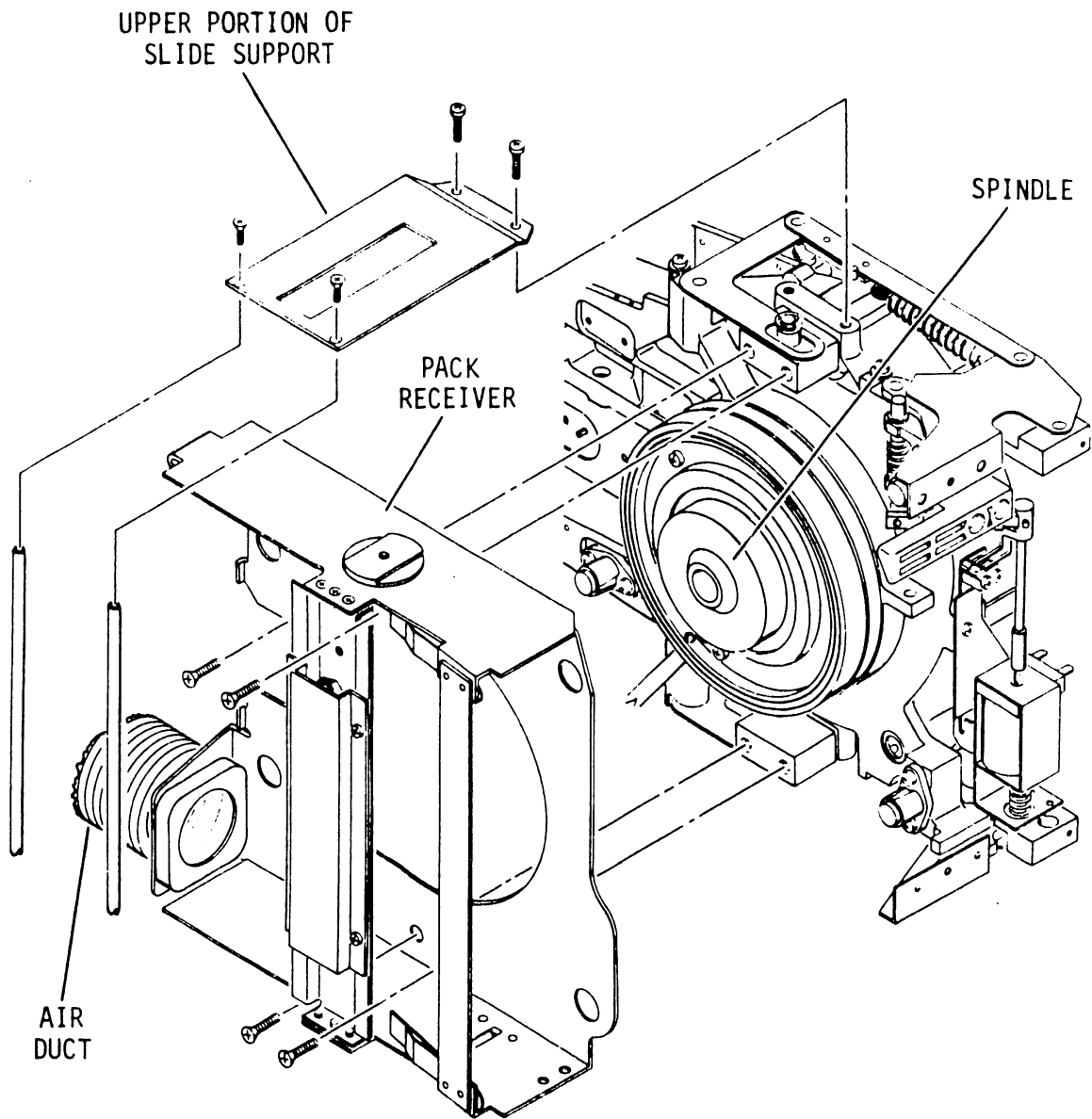
REMOVAL

1. Perform magnet removal procedure (proc 5204).
2. Disconnect servo and read write head cables from connectors.
3. Disconnect carriage ground strap from housing (see figure 5-12).
4. Remove carriage and coil assembly (with servo and read write heads still installed on carriage).
5. Detach air inlet duct (see figure 5-13) from pack receiver. Move duct away from inlet to avoid damage when pack receiver is removed.
6. Override front door interlock and open front door (proc 2103).
7. Remove upper portion of slide support.
8. Remove four screws securing pack receiver to drive. Carefully remove pack receiver from drive.
9. Remove screws securing pack receiver support ring to spindle (refer to figure 5-17). Disconnect air tube from ring and remove ring (and spacer, if used) from drive.



10R217A

Figure 5-12. Upper and Lower Rails Removal and Replacement



10R220A

Figure 5-13. Pack Receiver Removal and Replacement

10. Close front door.
11. Remove rubber gasket from cam towers.
12. Remove upper cam tower.
13. Remove head cam and post assembly.
14. Remove center air return cover.
15. Remove plugs covering lower rail attaching screws.

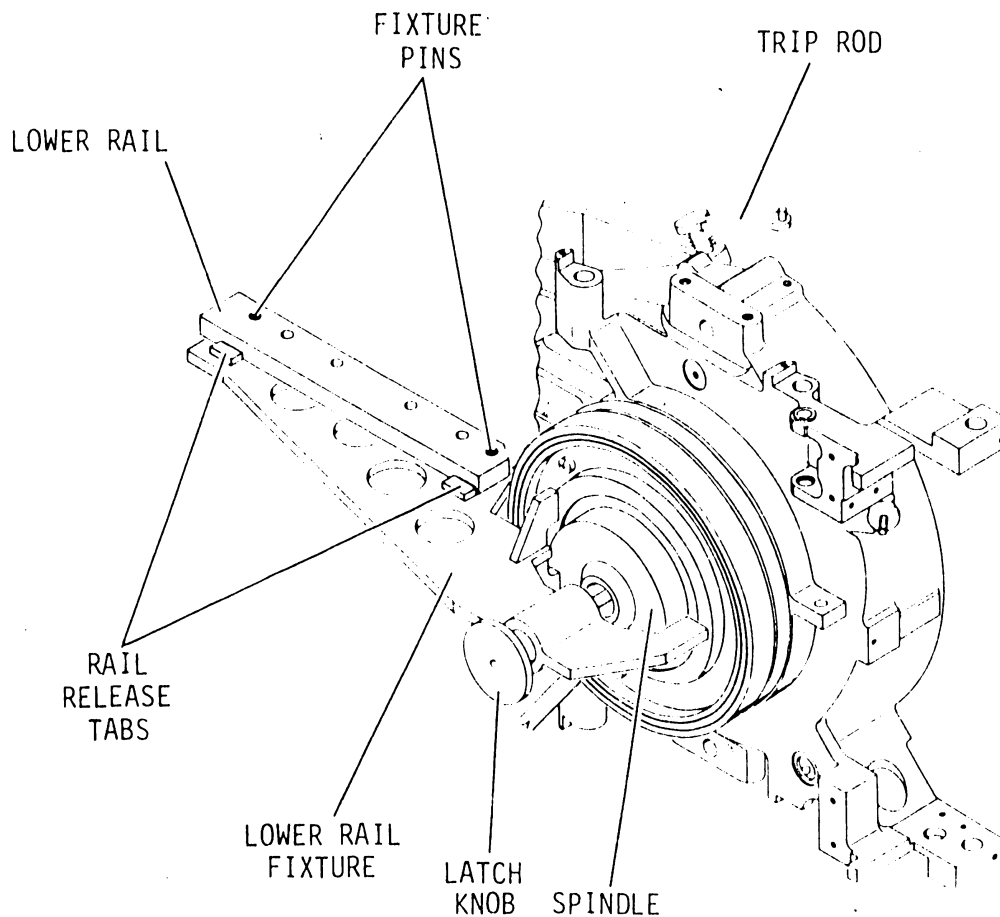
NOTE

In the following step, loosen, but do not remove, attaching screws if this procedure is being performed for rail alignment rather than rail replacement.

16. Remove upper and lower rails.

REPLACEMENT

1. Loosely install upper and lower rails with attaching screws.
2. Install lower rail fixture onto lower rail and spindle (see figure 5-14).
3. Hold lower rail in position and secure by gradually tightening screws sequentially from one to the next, until all screws are tightened to 2 N·m (18 lbf·in).
4. Release fixture from lower rail. Pivot the trip rod arm and push down on fixture latch knob to release fixture from spindle. Remove fixture from drive.
5. Slide upper rail fixture onto upper and lower rails (see figure 5-15).
6. Apply even pressure to both ends of upper rail and, while holding upper rail in place, secure by gradually tightening screws sequentially from one to the next, until all screws are tightened to 2 N·m (18 lbf·in).
7. Check rail alignment by sliding fixture from one end of rails to the other and ensuring that the gap between fixture and rail is even on both ends.



10R218

Figure 5-14. Lower Rail Installation

8. Remove fixture from rails.
9. Install plugs over screws attaching lower rail.
10. Install head cam and post assembly with attaching screws.
11. Install upper cam tower (see figure 5-12). Ensure that upper cam tower does not interfere with carriage lock during installation.
12. Install rubber gasket on cam towers.
13. Open front door and connect air tube to pack receiver support ring. Install support ring (and spacer, if used) on spindle.

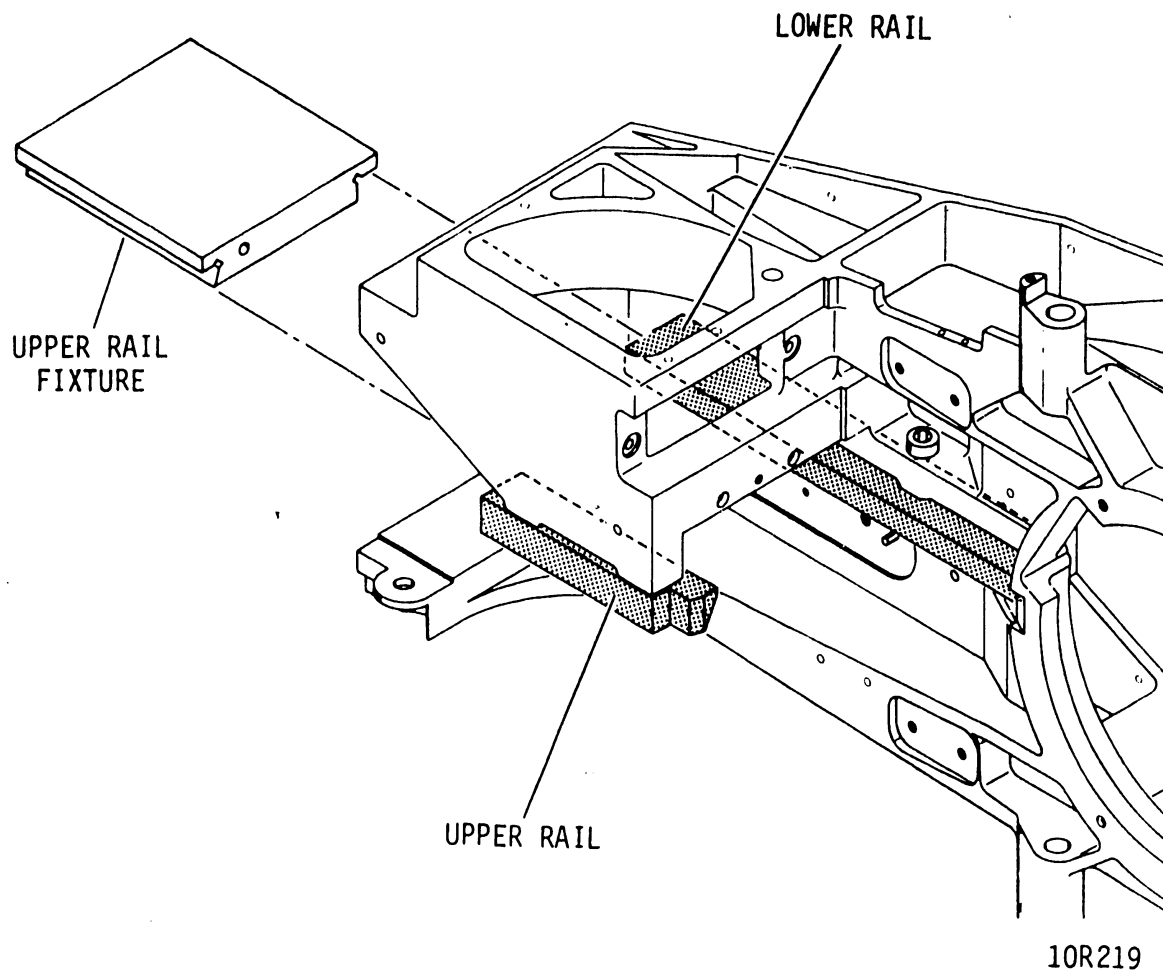


Figure 5-15. Upper Rail Installation

14. Install pack receiver (see figure 5-13).
15. Install slide support and close front door.
16. Connect air inlet duct to pack receiver.
17. Carefully insert carriage and coil assembly into housing. Ensure that the head arms slide smoothly onto the head cams.
18. Connect servo and read/write head cables to connectors.
19. Connect carriage ground strap to housing.
20. Install center air return cover.

21. Perform magnet replacement procedure (proc 5204).
22. Perform head alignment procedure (proc 5212).

5208 - RAILS & BEARINGS INSPECTION & CLEANING

In order to ensure that the carriage is able to move freely along the rails, it is essential that the rail and bearing surfaces be kept clean. Any obstruction to free movement of the carriage may cause seek or read errors. Ensure that power is removed from the drive and that the pack is removed from the spindle.

1. Place main logic in maintenance position (proc 2101).
2. Remove top and side air covers to gain access to carriage and rails.

CAUTION

Do not clean carriage or rails with cotton swabs or any type of cleaning solvent. Dry clean carriage and rails with foam tip swabs only. See table 2-1 (Maintenance Tools and Materials) for foam tip swab CDC part number.

3. Grasp carriage through top opening of housing.
4. Release carriage lock and slowly push carriage forward until heads clear cams.
5. Gently slide carriage and coil assembly back and forth along full length of rails. While moving coil, be aware of any possible irregularity (bumps or jerks) in movement. A sudden irregularity indicates dirt on rails or bearings. Do not confuse pressure of flex leads and head leads with a sudden irregularity in motion. Pressure from leads is a smooth motion.
 - If a sudden irregularity in motion was noted in previous step proceed to next step.
 - If no sudden irregularity in motion was noted, cleaning is not required. Proceed to step 8.

6. Clean rail and bearing surfaces with a dry foam tipped swab. Access front portion of rails and bearings from interior of pack area. Access the remainder of rails and bearings through top opening of housing. Move carriage back and forth while cleaning in order to ensure all surfaces are reached.
7. When rail and bearing cleaning is completed, repeat step 5 to ensure that carriage moves freely without sudden irregularities in its motion. If carriage now moves smoothly throughout its travel, proceed to step 8. If sudden irregularities persist, visually inspect rails and bearings using a strong light. Look for deterioration (not normal wear) of rails or bearing surfaces. Surface deterioration requires replacement of defective parts.
8. Return carriage to heads unloaded position (fully retracted).
9. Install top and side air covers and return main logic to normal operating position (proc 2101).

5209 - MOTOR & CABLE ASSEMBLY REMOVAL & REPLACEMENT

The following procedure describes how to remove and replace the motor and cable assembly. Ensure that the data pack has been removed, the front door is closed, and the heads are in the retracted (locked) position.

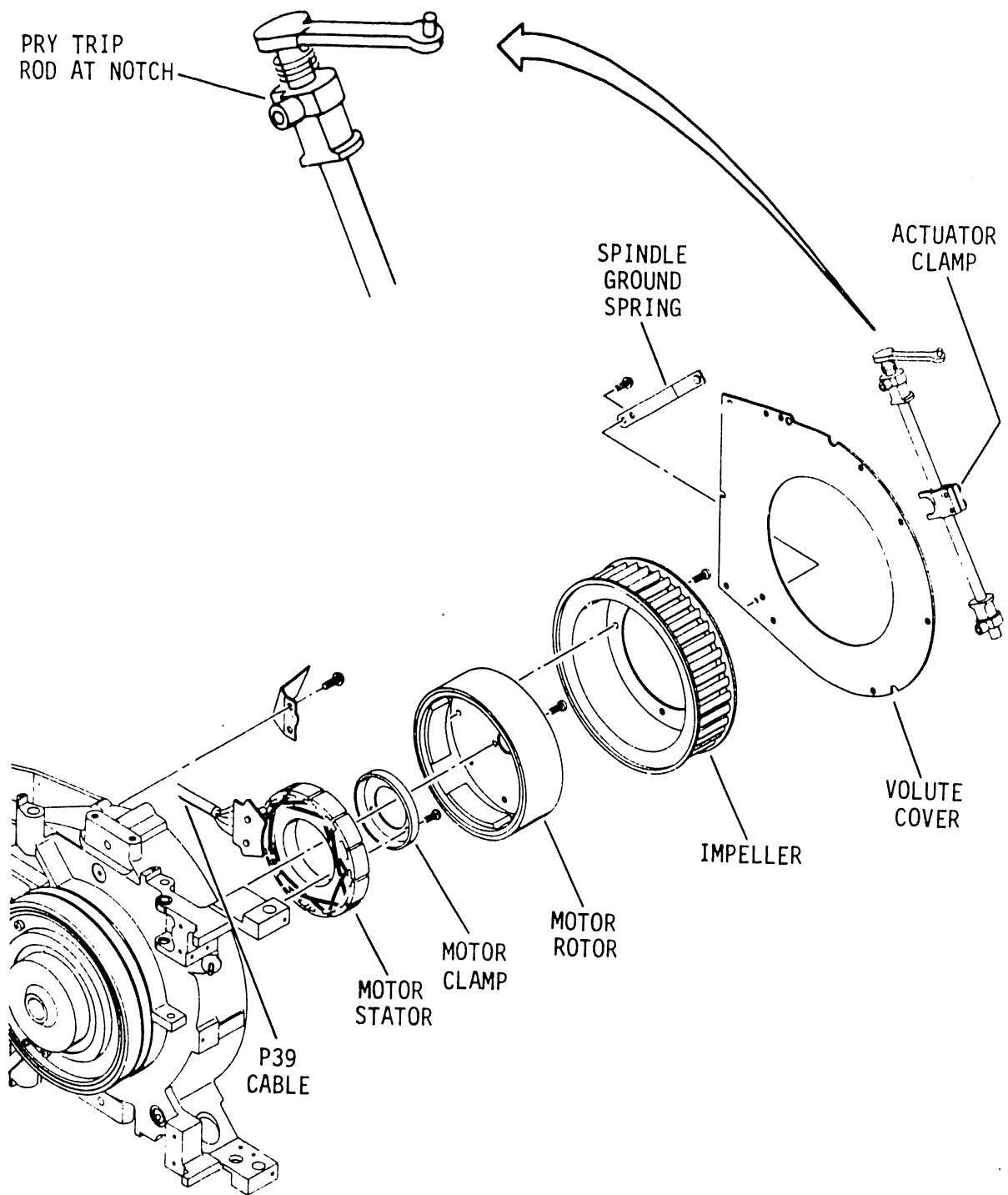
REMOVAL

1. Place main logic in the maintenance position (proc 2101).
2. Remove all three air return covers.
3. Remove spindle ground spring (see figure 5-16).
4. Loosen screws securing actuator clamp to spindle lock-shaft.

CAUTION

Do not attempt to grasp and pull trip rod loose or damage will result to trip rod inserts.

5. Carefully pry loose each end of the trip rod (at notch next to nylon inserts) with a flat blade screwdriver. Remove trip rod.



10R221B

Figure 5-16. Motor and Cable Assembly Removal and Replacement

6. Remove volute cover.
7. Remove four screws securing impeller on motor rotor. Remove impeller.
8. Remove screws securing motor rotor to spindle. Remove rotor (firm pulls are necessary).
9. Remove motor cable strain relief clamp.
10. Remove screws securing motor clamp to spindle. Remove clamp.

NOTE

Perform step 11a if motor is being removed only to provide access to other components. Perform step 11b if motor is defective and is to be replaced.

11. Remove stator and cable as follows:
 - a. Carefully move motor stator and cable away from spindle area.
 - b. Disconnect P39 from _PMX board, cut cable tie securing motor cable to base, and remove motor stator and cable from drive.

REPLACEMENT

1. Install stator and cable as follows:
 - a. Attach stator to spindle using motor clamp and hardware shown in figure 5-16. Position cable assembly and install cable strain relief clamp.
 - b. Secure motor cable and P43 voice coil cable to base with a cable tie.
 - c. Connect P39 to _PMX board.
2. Install rotor on spindle.
3. Install impeller on rotor.
4. Close front door. Hold volute cover in place, load trip rod spring, and install trip rod on drive.
5. Perform spindle lockshaft adjustment (proc 5211).

6. Install spindle ground spring.
7. Install air return covers.
8. Place main logic in the normal operating position (proc 2101).

5210 - SPINDLE REMOVAL & REPLACEMENT

The following procedure describes how to remove and replace the spindle assembly and how to adjust the lockshaft actuator. It is necessary to align upper and lower rails whenever spindle is removed.

REMOVAL

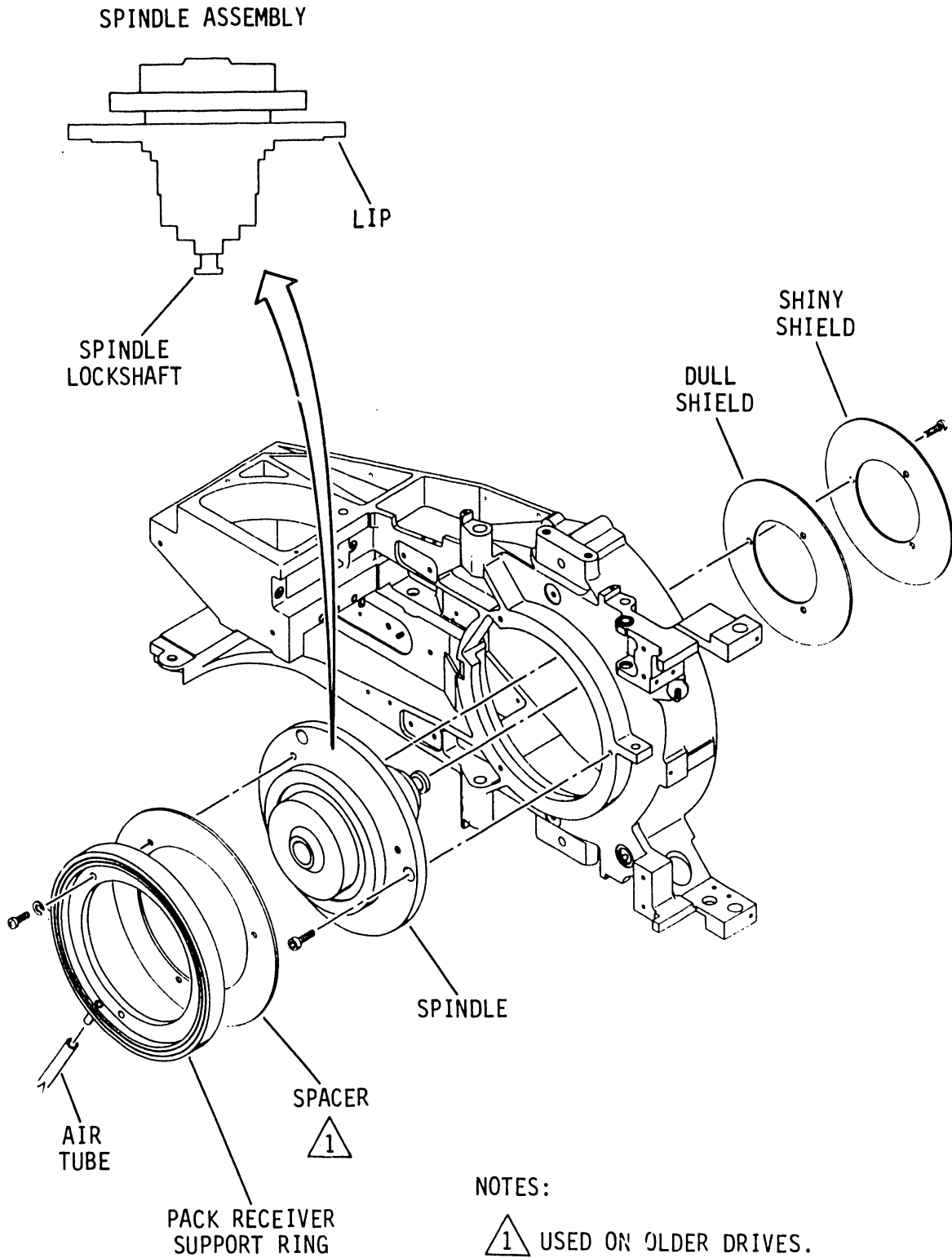
1. Perform motor and cable assembly removal procedure (proc 5209).
2. Remove two metal shields from spindle by removing attaching hardware (refer to figure 5-17).
3. Prepare for rail alignment by performing upper & lower rails removal procedure (proc 5207).
4. Remove spindle.

REPLACEMENT

CAUTION

When installing spindle assembly, ensure that the spindle lip (see figure 5-17) is seated properly into drive housing prior to tightening screws. Failure to do so will cause damage to heads and pack.

1. Install spindle (see figure 5-17).
2. Perform upper and lower rails replacement procedure (proc 5207).
3. Install two metal shields on spindle (with the dull shield next to spindle and the shiny shield next to motor stator) with attaching hardware.
4. Perform motor and cable assembly replacement procedure (proc 5209).



10R222

Figure 5-17. Spindle Removal and Replacement

5211 - SPINDLE LOCKSHAFT ADJUSTMENT

1. Remove spindle air return cover.
2. Position lockshaft actuator on trip rod as follows:
 - a. Loosen the two set screws on the lockshaft actuator (see figure 5-18).
 - b. Position actuator on trip rod by sliding the actuator until fork in actuator is centered about the spindle lockshaft, to within ± 3 mm (0.12 in).
3. Adjust gap between actuator and end of spindle lockshaft by rotating the actuator on the trip rod until gap is 0.50 to 1 mm (0.020 to 0.040 in).
4. Tighten set screws after adjustments are completed.
5. Install air return cover.

5212 - HEAD ARM REMOVAL, REPLACEMENT & ALIGNMENT

The following procedures describe two methods of removing and replacing heads. The first procedure describes how to remove and replace servo or read/write heads with the carriage and coil assembly installed in the drive. The second procedure describes how to remove and replace the servo or read/write heads with the carriage and coil assembly removed from the drive. The first procedure (with carriage and coil assembly installed in the drive) is recommended when one or two heads are to be replaced. An alignment procedure follows removal and replacement. Head alignment must be performed each time a head is replaced.

REMOVAL (CARRIAGE AND COIL ASSEMBLY INSTALLED)

1. Remove pack from drive and place main logic in the maintenance position (proc 2101).
2. Remove top and side air covers to gain access to heads.

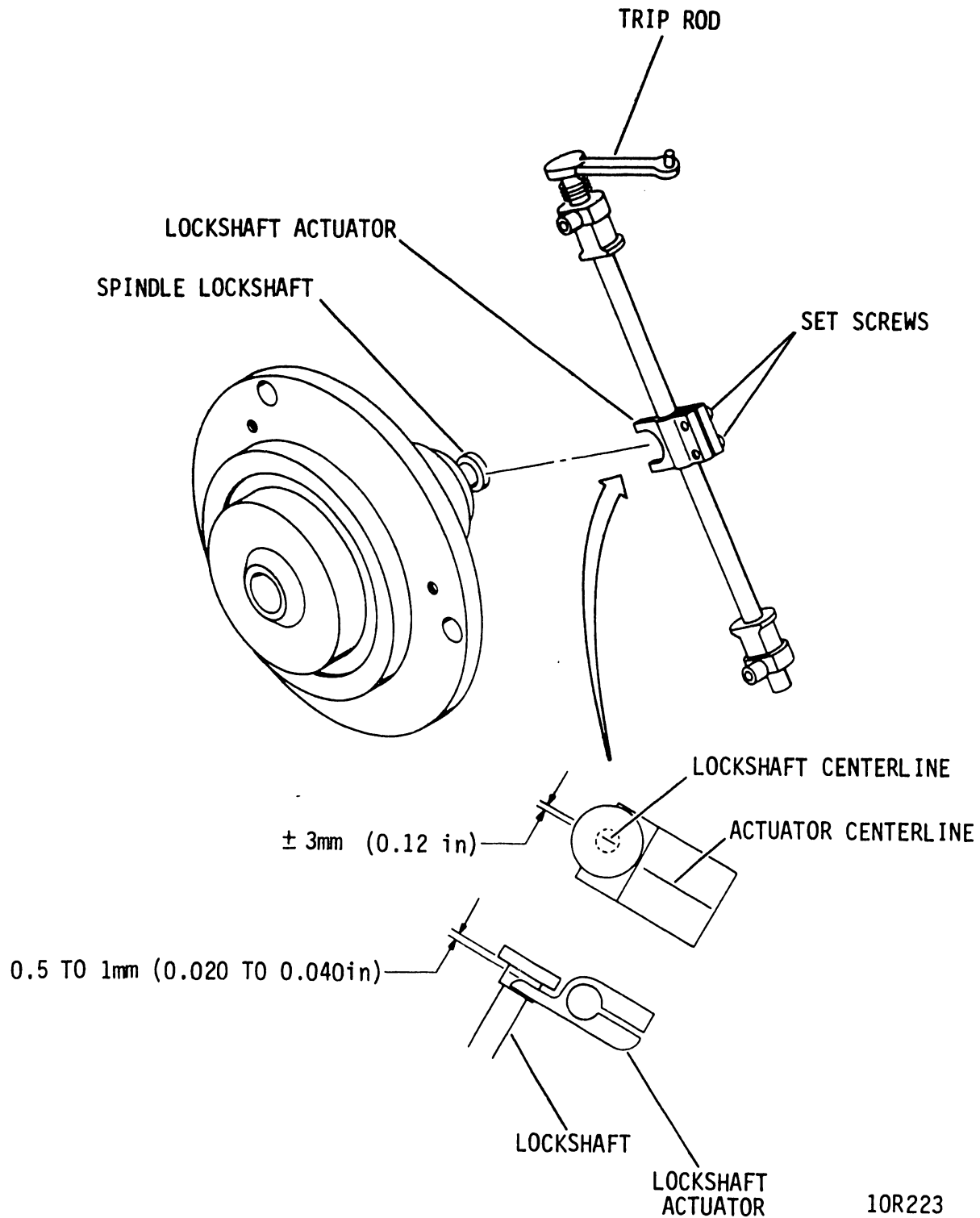


Figure 5-18. Spindle Lockshaft Adjustment

3. Disconnect head connector as follows:
 - a. If a read/write head is to be replaced, use a small flat blade screwdriver and the index finger of other hand to carefully loosen the head connector from read/write preamp board.
 - b. If a servo head is to be replaced, carefully grasp the connector with a long nose pliers and wiggle connector loose from servo preamp board.
4. Manually release carriage lock and move heads forward, until head cam arms are riding on cam towers and there is a maximum separation between head pads. Extend heads until edges of cam arm can be grasped from inside pack area (approximately 13 mm (0.5 in) past rubber seal). See figure 5-19 and 5-20.

CAUTION

Head pads and gimbal springs are extremely delicate and easily damaged. When removing or replacing a head, grasp it carefully and only by edges of cam arm. Also ensure that contact is not made as the head slides by adjacent head pads. This sliding type of contact will damage both the head pads and gimbal springs. Fully extending the heads into the pack area will also result in contact between adjacent head pads. But this type of contact will not cause damage.

5. Hold the carriage in this position with the left hand through the side access hole. At this position, there is maximum separation between adjacent head pads.

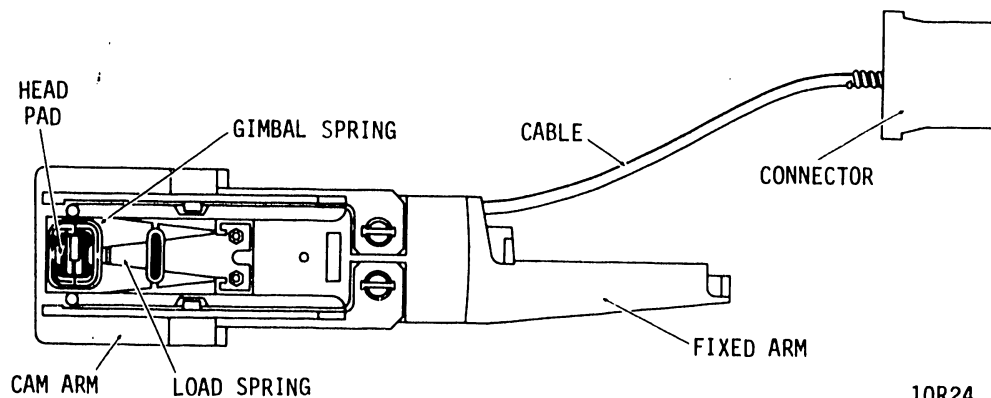
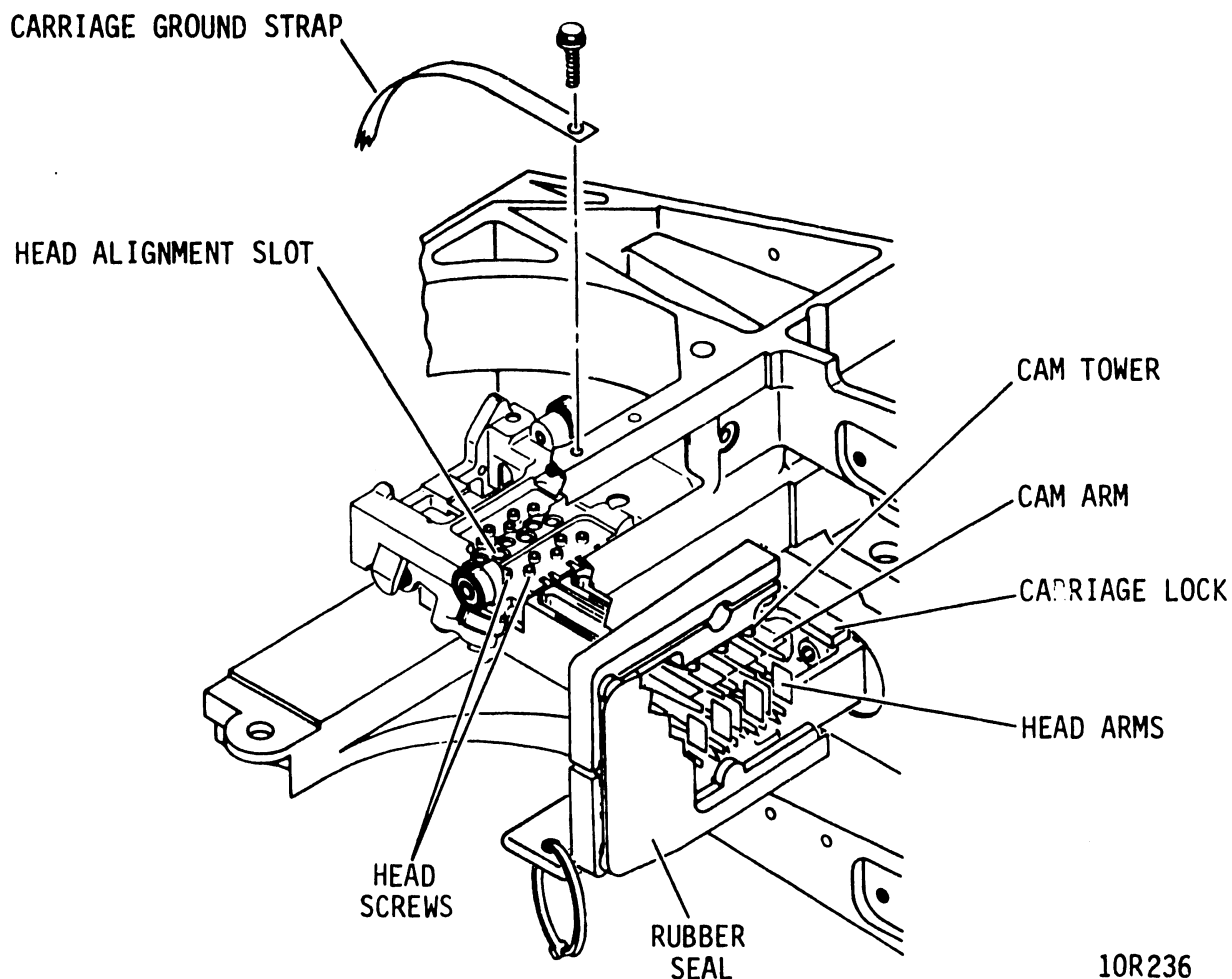


Figure 5-19. Head Arm



10R236

Figure 5-20. Head Arm Removal and Replacement

6. Using a 3/32 allen wrench, fully loosen the two head screws securing fixed arm to carriage (screws are captive in carriage).
7. Place allen wrench into the head alignment slot and carefully push on side of fixed arm to tilt head down approximately 3 mm (1/8 in). This will eliminate interference from captive screws as head is pushed forward.
8. Remove head by holding it in the slightly tilted position, grasping edges of cam arm and pushing gently on rear of fixed arm until it is clear of the slot. Then feed the head cable connector through the vacated slot and fully extend the carriage to avoid contact with adjacent head pad as cable and connector are removed.

REPLACEMENT (CARRIAGE AND COIL ASSEMBLY INSTALLED)

1. Fully extend the carriage and feed the head cable connector through the slot vacated by head. Hold in place and slowly retract carriage. Grasp head connector (long nose pliers may be used), and continue to retract the carriage until the existing head cam arms are riding on cam towers. See figures 5-19 and 5-20.
2. Hold the carriage in place (cam arms on cam towers) and carefully install new head. Ensure that the head is installed with the fixed arm in a slightly tilted (downward) position, so that the captive head screws do not interfere with head installation.
3. Push up on side of fixed arm, to seat fixed arm in both front and rear notches on carriage. Center fixed arm oval shaped hole in carriage head alignment slot.
4. Hold the head arm in position and secure with the two head mounting screws using a 3/32 allen wrench. Tighten head screws to 0.6 N·m (5 lbf·in).
5. Carefully install head connector.
6. Install side air cover.
7. Perform head alignment procedure.

REMOVAL (CARRIAGE AND COIL ASSEMBLY REMOVED)

1. Remove pack from drive.
2. Remove main logic and rear panel assembly (proc 2102).
3. Remove top and side air covers to gain access to heads.
4. Disconnect head connectors as follows:
 - a. For the read/write heads, use a small flat blade screwdriver and the index finger of other hand to carefully loosen the head connector from read/write preamp board.
 - b. For the servo head, carefully grasp the connector with a long nose pliers and wiggle connector loose from servo preamp board.
5. Perform magnet removal procedure (proc 5204).

6. Disconnect carriage ground strap from carriage. See figures 5-19 and 5-21.
7. Disconnect coil flex leads from mounting block.

CAUTION

Head pads and gimbal springs are extremely delicate and easily damaged. When removing or replacing a head, grasp it carefully and only by edges of cam arm. Also ensure that contact is not made as the head slides by adjacent head pads. This sliding type of contact will damage both the head pads and gimbal springs. Fully extending the heads into the pack area will also result in contact between adjacent head pads. But this type of contact will not cause damage.

8. Carefully remove carriage and coil assembly from housing.
9. Using a 3/32 allen wrench, fully loosen the two head screws securing fixed arm to carriage (screws are captive in carriage).
10. Hold fixed arm in place and with the other hand grasp edges of cam arm. Move head pad away from adjacent head pad and remove head assembly from carriage.

REPLACEMENT (CARRIAGE AND COIL ASSEMBLY REMOVED)

1. Grasp edges of cam arm to pull head pad away from adjacent head pad, and with the other hand guide fixed arm into front and rear notches in carriage. See figure 5-21.
2. Center fixed arm oval shaped hole in carriage head alignment slot.
3. Hold the head arm in position and secure with the two head mounting screws using a 3/32 allen wrench. Tighten head screws to 0.6 N·m (5 lbf·in).
4. Carefully install carriage and coil assembly into drive.
5. Connect coil flex leads to mounting block.
6. Connect carriage ground strap to carriage housing.

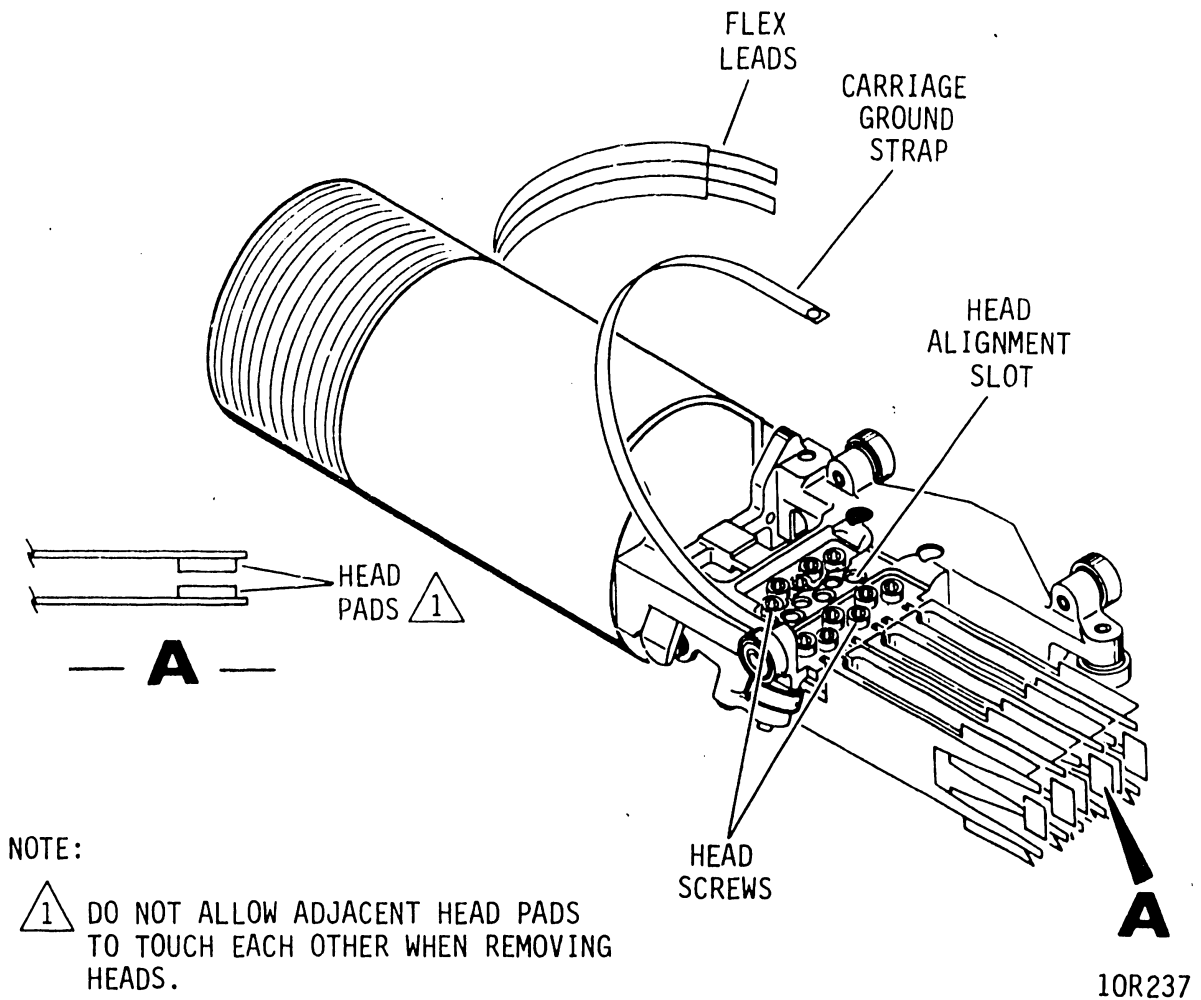


Figure 5-21. Head Arm Replacement With Carriage Removed

7. Carefully connect head connectors to preamp boards.
8. Perform magnet replacement procedure (proc 5204).
9. Install side air cover.
10. Replace main logic and rear panel assembly (proc 5212).
11. Perform head alignment procedure.

HEAD ALIGNMENT

General

Alignment of the heads is checked under the following conditions:

- After replacing one or more head arm assemblies.
- When misalignment of one or more heads is suspected. (For example, inability to read a pack written on another drive).
- After removal or replacement of carriage assembly.

If it is determined that a head is misaligned, the head arm is adjusted to bring the alignment of the head within specifications.

Head alignment is performed by using a field test unit (FTU) or by using the controller, microprogram diagnostics, head alignment board, oscilloscope and null (or digital) Meter (refer to Maintenance Tools and Materials in section 2 for tools required to perform head alignment). This procedure applies only to the method using an FTU. Refer to the FTU maintenance manual for switch settings and functions called for in this procedure.

When performing head alignment, give special consideration to the following:

Thermal Stabilization - In order to ensure accuracy during head alignment, it is important that the drive, CE pack, and FTU be at their normal operating temperature. This requires that all three be connected and allowed to operate (pack turning and heads loaded to cylinder zero) for a minimum of 50 minutes.

If head alignment is being performed on more than one drive, and provided that the pack was taken immediately from a previous drive, and provided that the drive under test has been operating with heads loaded for a minimum of 50 minutes preceding tests; then CE pack only requires an 8 minute stabilization time.

Alignment Tool - Use only the head alignment tool (non-magnetic) specified in the maintenance tools and materials table. Use of a different tool may cause damage to head arm or carriage. Always inspect the adjustment end of tool prior to use. Tool must be free of nicks and scratches and must have a polished surface where it enters the carriage alignment hole. If any aluminum deposits are present, polish tool surface with crocus cloth. Any other polishing medium will damage the tool.

Do not use a defective tool; repair or replace tool if damage exists. When using tool, position it so that pin in end of tool engages alignment slot in head arm. The tool should slip easily through the alignment hole in the carriage and into the alignment slot in the head arm. If anything more than a small amount of force is required to adjust the head, the tool is probably binding in the hole of the carriage. Ensure that alignment tool is kept perpendicular to hole in carriage at all times.

Carriage Locking - During the alignment procedure (when the heads are over the alignment track) a screwdriver must be installed in the Align Track Lock hole in the rail bracket assembly. This locks the carriage over the alignment track. Failure to install the screwdriver would allow the carriage to retract if any emergency retract signal were generated. Since your hands are in the actuator during the head alignment procedure, the retract could be dangerous.

CAUTION

Should an emergency retract condition be generated when the screwdriver is in the Align Track Lock hole, the following results may occur:

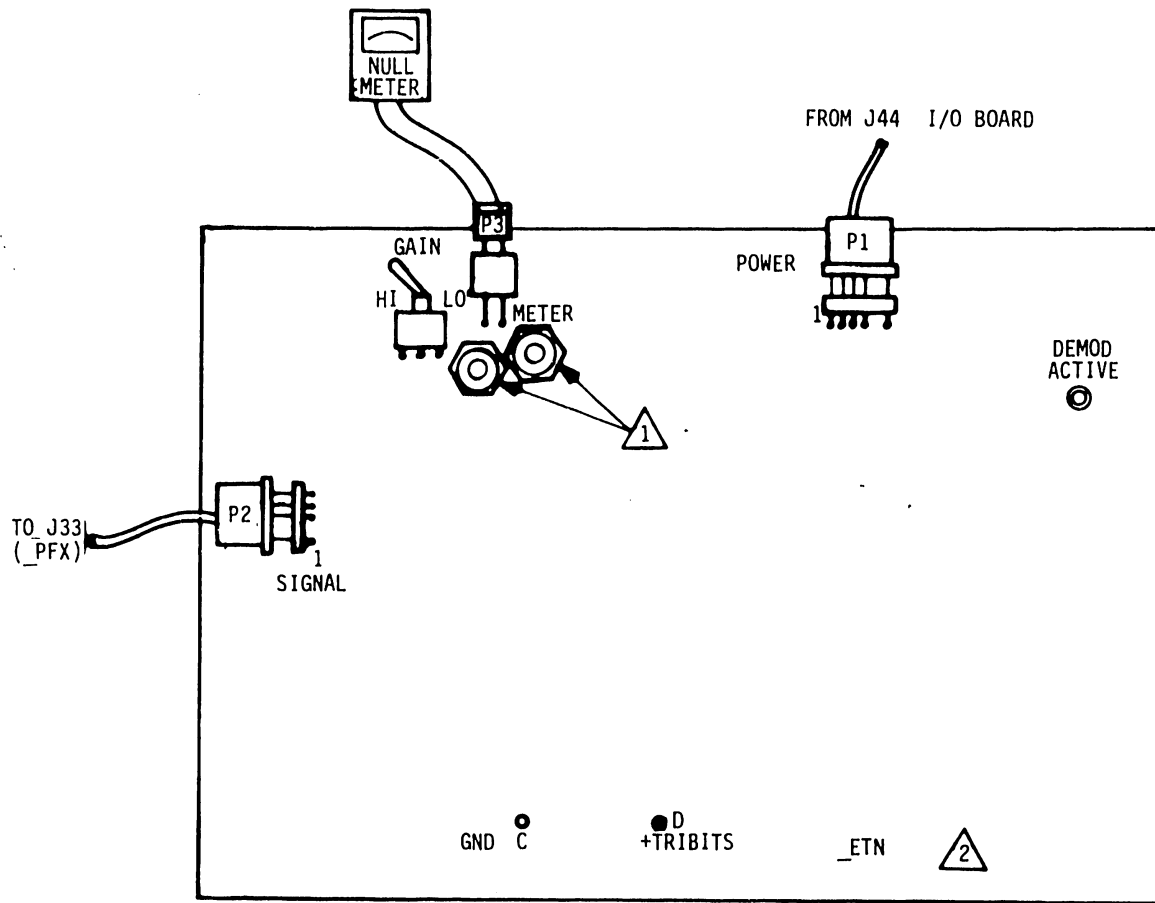
- Blown fuses.
- Tripped AC circuit breaker
- Blown power amplifier transistors, and
- Unretracted heads on a stationary CE pack.

Carefully observe the instructions regarding the installation and removal of the screwdriver into Align Track Lock hole.

Procedure

1. Install CE pack and ensure that the write protect tab on CE pack is in the Write Protect position (refer to Volume 1, Pack Installation).
2. Set CBI on power supply OFF.
3. Perform top cover removal procedure (proc 5102).
4. Remove the two screws securing read/write boards to vertical and rear panel support brackets.

5. Swing boards up and lock into position.
6. Remove top air cover to gain access to heads.
7. Connect FTU to drive. Refer to FTU maintenance manual for installation instructions.
8. Install terminator on I/O connector.
9. Check servo offset as follows:
 - a. Set CBI to ON and press START switch to start drive motor and load heads.
 - b. Connect digital voltmeter between J13-4 on _PEX board and ground (chassis). On older _PEX boards J13 is located behind _EBN/_EDN board. Remove _EBN/_EDN board from screw posts to gain access to J13.
 - c. Command direct seek to cylinder 400 and observe that meter indicates 0 ± 50 millivolts.
 - d. If unit does not meet specifications stated in step 9-c, remove CE pack and perform servo checks found in section 4.
 - e. If unit meets specifications stated in step 9-c, press START switch to stop drive motor and unload heads. Set CBI to OFF and go to step 10.
10. Connect cables to _ETN head alignment board as follows:
 - a. Connect meter cable from null (or digital) meter to METER. See figure 5-22.
 - b. Connect oscilloscope to test point C (GND) and test point D (+TRIBITS).
 - c. Install signal cable from J33 on _PFX board to SIGNAL.
 - d. Connect power cable from J44 on _EBN/EDN board to POWER.
11. Set CBI on power supply to ON.
12. Press START switch to start drive motor and load heads.
13. Perform thermal stabilization.
14. Command continuous seeks between cylinders 400 and 401 for 30 seconds.



NOTES:

10R243

- 1 CONNECT METER TO P3
OR BANANA PLUG CONNECTORS
- 2 COMPONENT SIDE OF BOARD

Figure 5-22. Head Alignment Setup

15. Command a direct seek to cylinder 400.
16. Select each read/write head individually and observe that DEMOD ACTIVE light on _ETN board is on and the +TRIBITS signal is similar to that shown in Figure 5-23. Physical head locations are shown in Figure 5-24.
17. Set gain switch on _ETN card to HI.

CAUTION

If the null meter indicates an offset error of greater than 175 mV (plus or minus) of zero range, those heads are excessively misaligned. Therefore, to avoid possible loss of data, transfer data from packs written with those heads to other storage before proceeding with alignment.

- a. When using same CE pack as used for last alignment on this unit, offset error cannot exceed 175 mV (plus or minus) of zero range. If all offsets are within this range, alignment is satisfactory. Proceed to step 30.
 - b. When using a different CE pack than the one used for last alignment, offset error cannot exceed 325 mV (plus or minus) of zero range. If all offsets are within this range, alignment is satisfactory. Proceed to step 30.
 - c. If any offsets are outside acceptable range, as defined in steps A or B (whichever applies), these heads are misaligned. Proceed to step 17.
18. Press START switch to stop drive motor and unload heads.
 19. Ensure head arm mounting screws are tightened to 0.6 N m (5 lbf in).
 20. Press START switch to start drive motor and load heads.
 21. Command continuous seeks between cylinders 400 and 401 for 30 seconds.
 22. Command a direct seek to cylinder 400 and install screwdriver in Align Track Lock hole.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2V	TP-D ON-ETN	+TRIBITS
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT	CH-1	+TRIBITS

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 2 μ SEC / CM MODE: INT

NOTES: GROUND SCOPE PROBE AT TP-C (-ETN) BOARD.

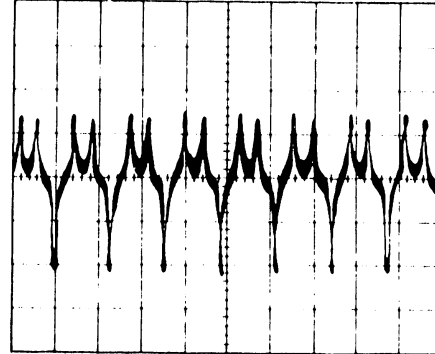


Figure 5-23. Head Alignment Waveform

CAUTION

Use extreme care to avoid short circuit contact with read/write or power amp boards when installing or removing head alignment tool and torque screwdriver.

NOTE

When performing head alignment, the force exerted during adjustment can move the heads from the alignment cylinder (400) to an adjacent cylinder. This will result in an improper alignment. In most cases this condition may be prevented by installing a jumper clip between test points AC (J737) and AB (J637) on the PEX board; however, be sure to remove the jumper clip before commanding the drive to perform another seek. If a SEEK ERROR condition exists, perform the following steps:

- a. Remove jumper clip from PEX board.

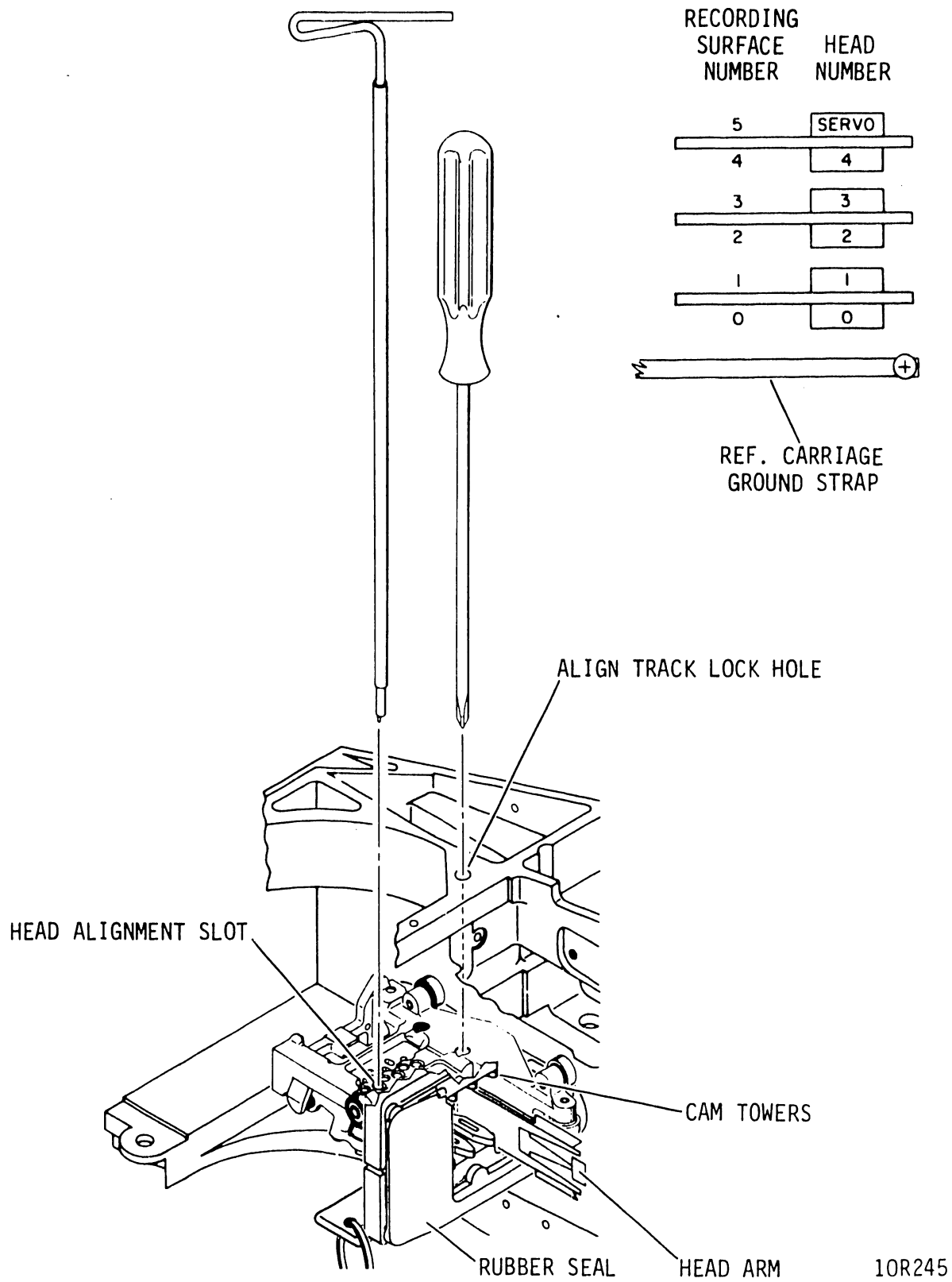


Figure 5-24. Head Arm Alignment

- b. Remove screwdriver from Align Track Lock hole.
- c. Command a Return to Zero (RTZ) seek.
- d. Command a direct seek to cylinder 400 and install screwdriver and jumper clip as stated above. Proceed to step 23.

23. Align read/write heads as follows:

- a. Set head alignment card GAIN switch to the "LO" position.
- b. Select head to be aligned.

WARNING

To prevent personal injury in case of an emergency retract, install a screwdriver in Align Track Lock hole prior to positioning head alignment tool. Be sure to remove screwdriver before next seek is performed. See figure 5-24.

- c. Install head alignment tool so that tool pin engages head-arm alignment slot.
 - d. Observe oscilloscope and adjust head to obtain balanced tribit pattern as shown in figure 5-23.
 - e. Set head alignment card GAIN switch to the "HI" position.
 - f. Observe null meter and adjust head until offset is within 50 mV (plus or minus) of zero.
 - g. Repeat steps a through f for all heads to be aligned.
24. Remove screwdriver from the Align Track Lock hole.
25. Press START switch to load and unload heads twice.
26. Press START switch to start drive motor and load heads.
27. Command continuous seeks between cylinders 400 and 401 for 30 seconds.

28. Command a direct seek to cylinder 400. Offset error cannot exceed 175 mV (plus or minus) of zero range.
29. If any heads exceed the limits stated in step 28, re-adjust them as directed in steps 21 through 25.
30. Perform the following to ensure that heads will remain aligned under normal operating conditions:
 - a. Perform 5 minutes of continuous seeks between cylinders 0 and 822.
 - b. Command direct seek to cylinder 400.
 - c. Check alignment of each head adjusted. If any heads are outside the acceptable range (as defined in step 28), repeat this procedure starting with step 21.
31. Press START switch to stop drive motor.
32. Remove C/E Alignment pack and set CBI on power supply to OFF.
33. Disconnect test setup.
34. Replace top air cover.
35. Return read/write boards to normal position.
36. Replace top cover (proc 5102).
37. Restore drive to on-line operation.

5213 - HEADS LOADED SWITCH REMOVAL, REPLACEMENT & ADJUSTMENT

REMOVAL

1. Place main logic in the maintenance position (proc 2101).
2. Remove top and side air covers.
3. Remove screws securing heads loaded switch to bracket. See figure 5-25. Remove switch from bracket.
4. Label switch wire locations and unsolder wires from switch.

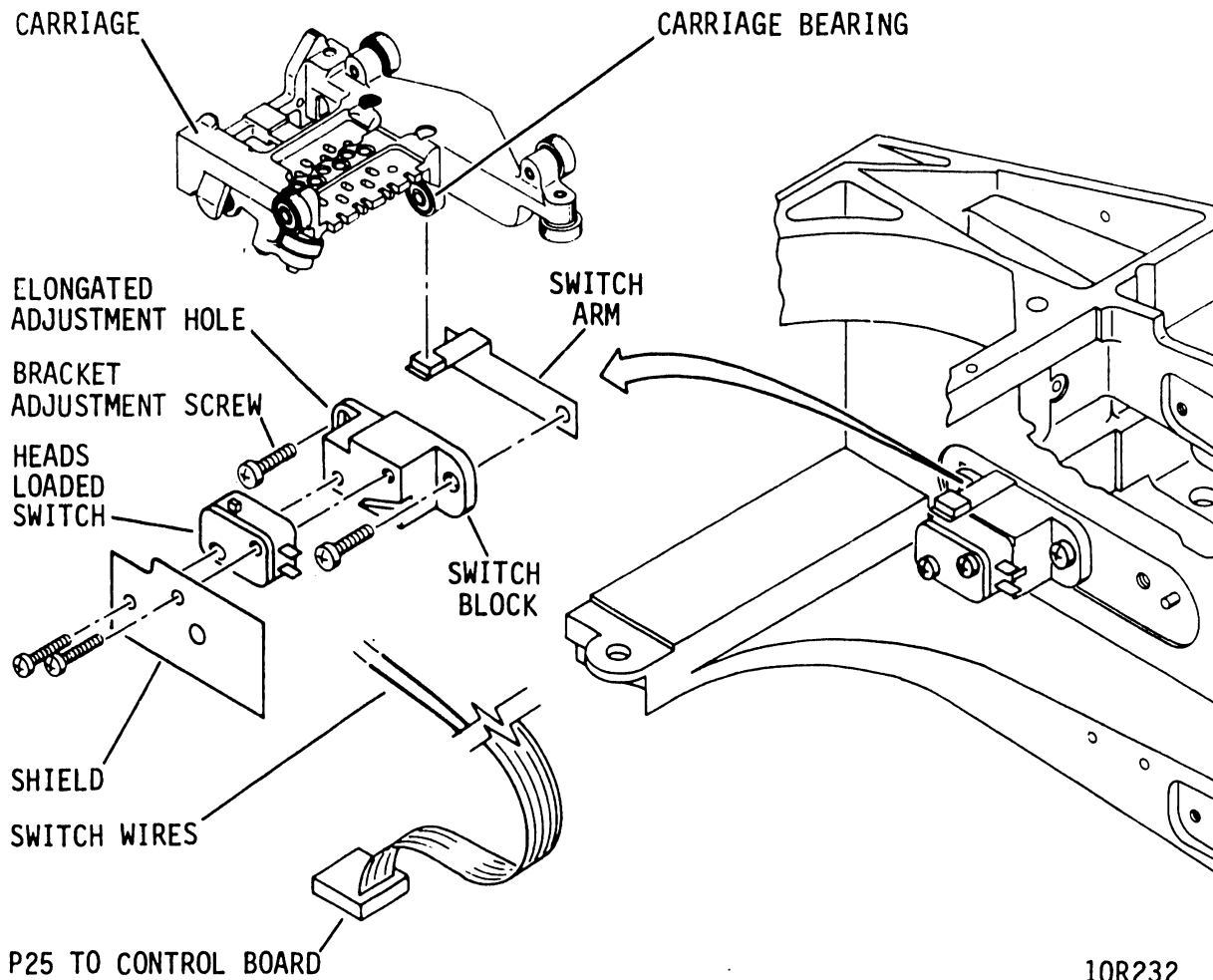


Figure 5-25. Heads Loaded Switch Replacement and Adjustment

REPLACEMENT AND ADJUSTMENT

1. Solder wires to new switch.
2. Install switch to bracket and secure in place. See figure 5-25.
3. Perform heads loaded switch adjustment as follows:
 - a. Remove pack from drive.
 - b. Disconnect P25 from _PEX board.
 - c. Connect ohmmeter between P25-01 and P25-02.

d. Check adjustment as follows:

- Move carriage to fully retracted position. Meter should indicate infinity (contacts open).
- Move carriage 13 mm (0.5 in) forward of fully retracted position. Meter should indicate 0 ohms (contacts closed).

e. If adjustment is necessary, loosen screw on heads loaded bracket (located on magnet side of bracket). Adjust switch to meet requirements of 3-c and 3-d.

f. Connect P25 to J25 on _PEX board.

4. Install top and side air covers.

5. Place main logic in normal operating position (proc 2101).

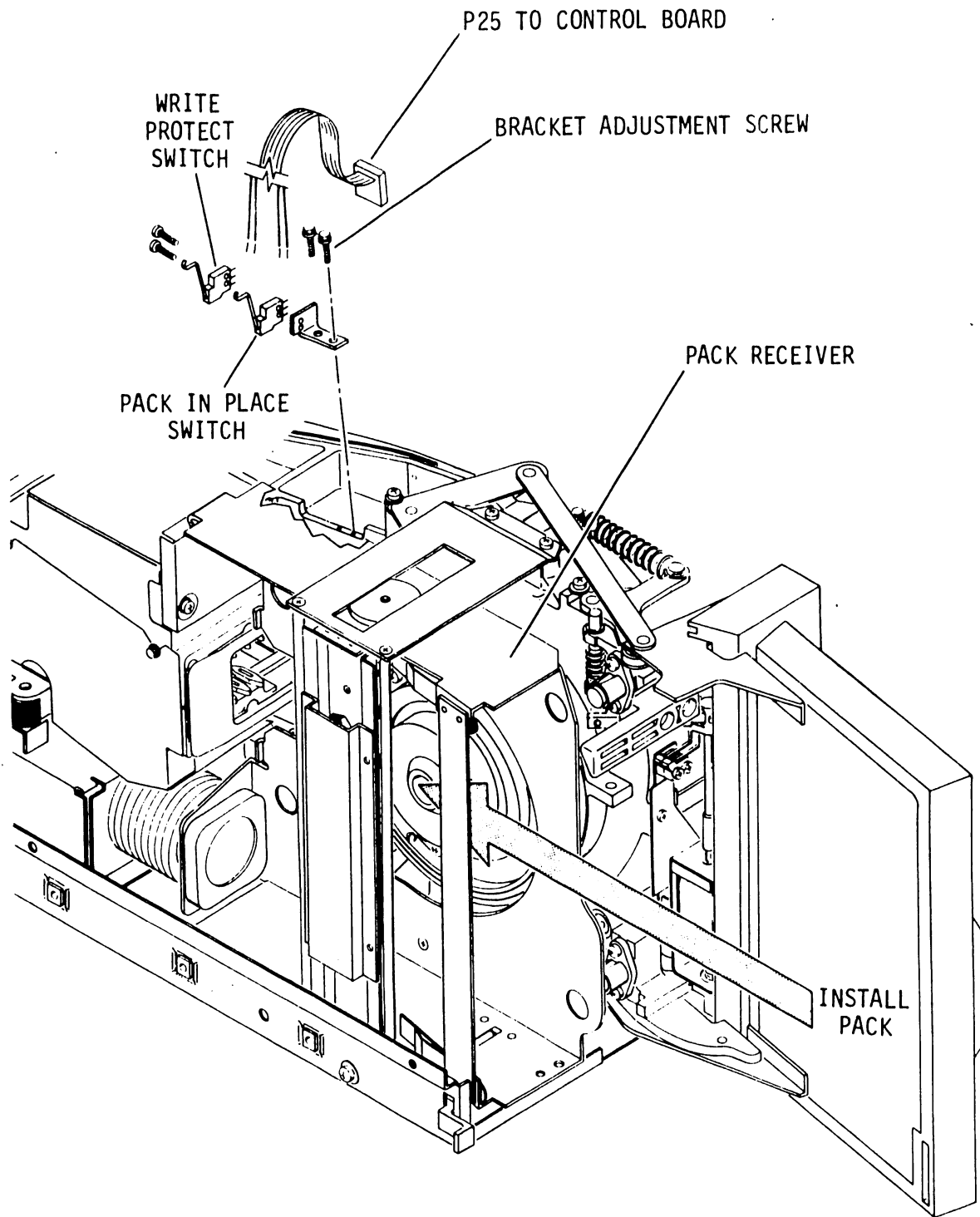
5214 - PACK IN PLACE & WRITE PROTECT SWITCHES REMOVAL, REPLACEMENT & ADJUSTMENT

REMOVAL

1. Perform top cover removal procedure (proc 5102).
2. Remove screws securing read/write boards to vertical and rear panel support brackets. Swing boards up and lock in place.
3. Remove screws securing pack in place and write protect switches to bracket. See figure 5-26. Remove switch(s) to be replaced.
4. Label switch wire locations and unsolder wires from switch(s).

REPLACEMENT AND ADJUSTMENT

1. Solder wires to new switch(s).
2. Install switches to bracket and secure in place. See figure 5-26.
3. Perform pack in place switch adjustment as follows:
 - a. Disconnect P25 from _PEX board.



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Figure 5-26. Pack in Place and Write Protect Switches

- b. Connect ohmmeter between P25-04 and P25-05.
 - c. Check adjustment as follows:
 - Install pack and close front door. Meter should indicate 0 ohms (contacts closed).
 - Open front door and unload pack. Meter should indicate infinity (contacts open).
 - d. If adjustment is necessary, loosen screw on switch bracket. Move switch up or down to achieve specifications stated in steps 3-b and 3-c.
 - e. Connect P25 to J25 on _PEX board.
4. Perform write protect switch adjustment as follows:
 - a. Disconnect P25 from _PEX board.
 - b. Connect ohmmeter between P25-04 and P25-03.
 - c. Check adjustment as follows:
 - Install pack (without write protect tab recessed) and close front door. Meter should indicate infinity (contacts open).
 - Remove pack and move tab to outer (write protect) position. Meter should indicate 0 ohms (contacts closed).
 - d. If adjustment is necessary, loosen screw on switch bracket and adjust to meet requirements of 3-b and 3-c.
 - e. Connect P25 to J25 on _PEX board.
 5. Perform Top Cover Replacement procedure (proc 5102).

5215 - DOOR UNLOCK SOLENOID REMOVAL, REPLACEMENT & ADJUSTMENT

REMOVAL

1. Perform top cover removal procedure (proc 5102).
2. Open front door (proc 2103).
3. Remove operator panel section of front panel (proc 5103).

4. Move front panel off to one side (with operator panel still installed). Close front door.
5. Remove the two wires from quick disconnect terminals on solenoid. See figure 5-27.
6. Loosen screws securing solenoid bracket to drive, to gain access to solenoid screws.
7. Remove screws securing solenoid to bracket. Lift plunger arm up and remove solenoid from bracket.
8. Remove retainer ring and spring from solenoid plunger.

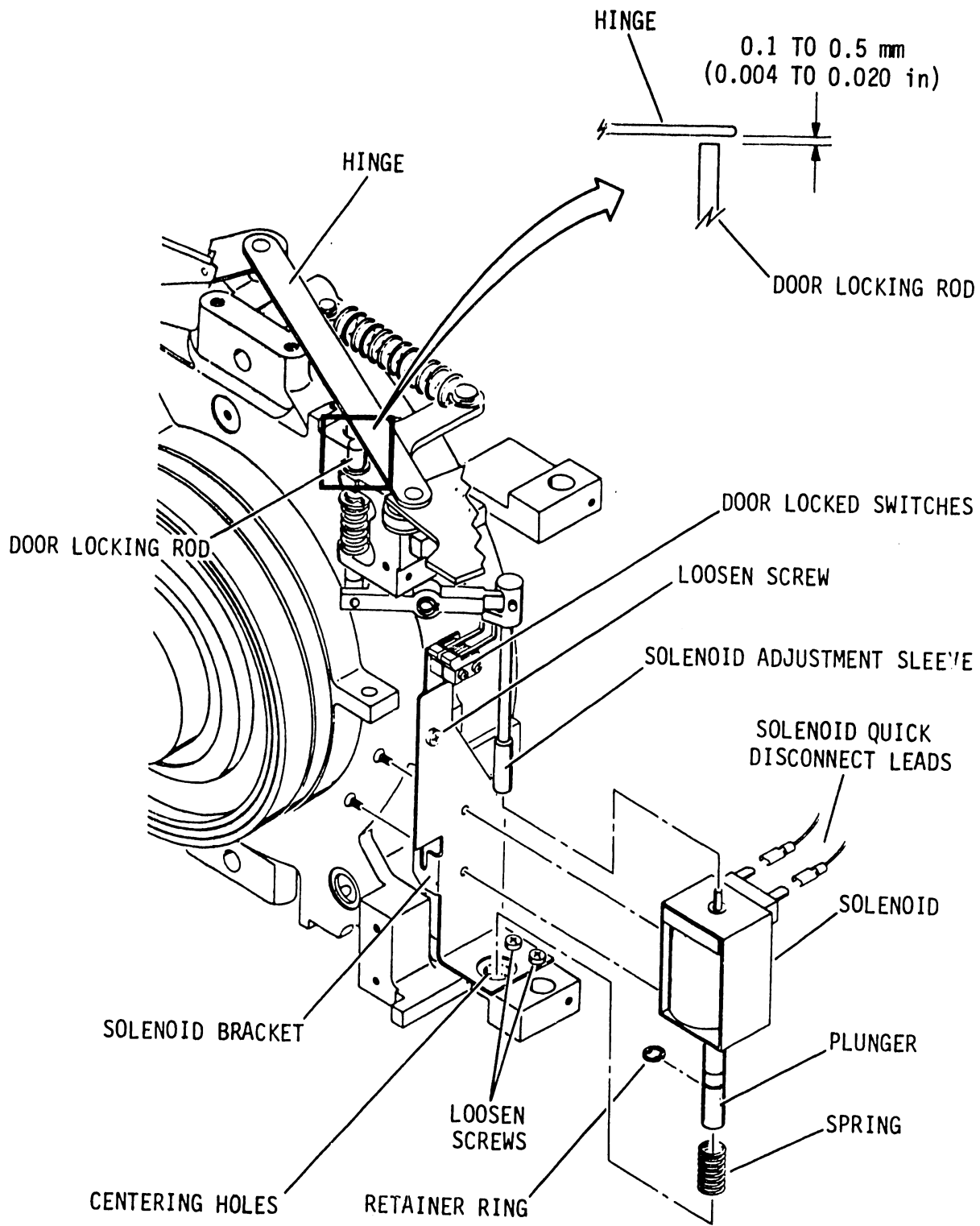
REPLACEMENT AND ADJUSTMENT

1. Install spring and retainer ring to solenoid plunger. See figure 5-27.
2. Install solenoid onto bracket and secure in place.
3. Align solenoid assembly by centering hole in bracket over hole in deck. Secure bracket to deck.
4. Install the two wires to quick connect terminals on solenoid.
5. Apply dc power to drive and open front door.

NOTE

The solenoid hinge linkage on S/C 01 & 02 units cannot be adjusted. If distance between door locking rod to hinge arm exceeds specifications stated in step 6, replace old linkage (see parts data Vol 1).

6. For units S/C 03 & ABV, adjust solenoid sleeve (shown in figure 5-27) so that the door locking rod is 0.1 to 0.5 mm (0.004 to 0.020 in) below the hinge arm when front door is open.
7. Close front door and remove dc power.
8. Ensure that front door does not open with dc power removed.
9. Ensure that the door locked switches are adjusted properly (proc 5216).



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Figure 5-27. Door Unlock Solenoid Replacement and Adjustment

10. Remove power from drive and install front panel (proc 5103).
11. Close front door and perform top cover replacement procedure (proc 5102).

5216 - DOOR LOCKED SWITCHES REMOVAL, REPLACEMENT & ADJUSTMENT

REMOVAL

1. Perform top cover removal procedure (proc 5102).
2. Open front door (proc 2103).
3. Remove operator panel section of front panel (proc 5103).
4. Move front panel off to one side (with operator panel still installed). Close front door.
5. Label switch wire locations and unsolder wires from switches. See figure 5-28.
6. Remove screws securing door locked switches to bracket.
7. Remove door locked switches from bracket.

REPLACEMENT & ADJUSTMENT

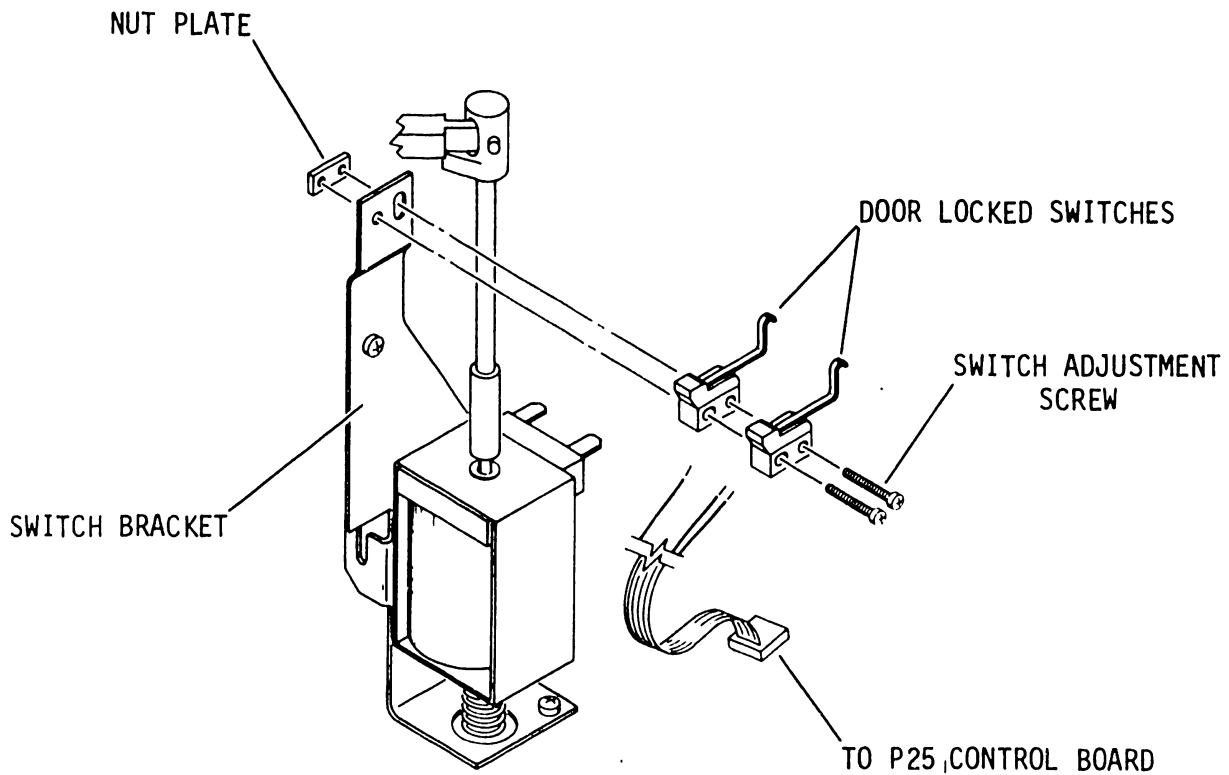
1. Install switches to bracket. See figure 5-28.
2. Solder wires to switches.
3. Perform door locked switches adjustment procedure as follows:
 - a. Apply dc power to drive.
 - b. Check adjustment as follows:
 - Open front door. Switch terminals with white and gray wires should be at a + 5 volt level.
 - Close front door. Switch terminals with white and gray wires should be at a ground level.
 - c. If adjustment is necessary, loosen screw on switch bracket and adjust switches to meet requirements of step 3-b.

4. Install front panel (proc 5103).
5. Perform top cover replacement procedure (proc 5102).

5301 - _PGX BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (proc 5102).
2. Disconnect P27, P31, and P36 from _PGX board.
3. Remove attaching hardware and lift _PGX board off _PFX board. See figure 5-29.



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Figure 5-28. Door Locked Switches Replacement and Adjustment

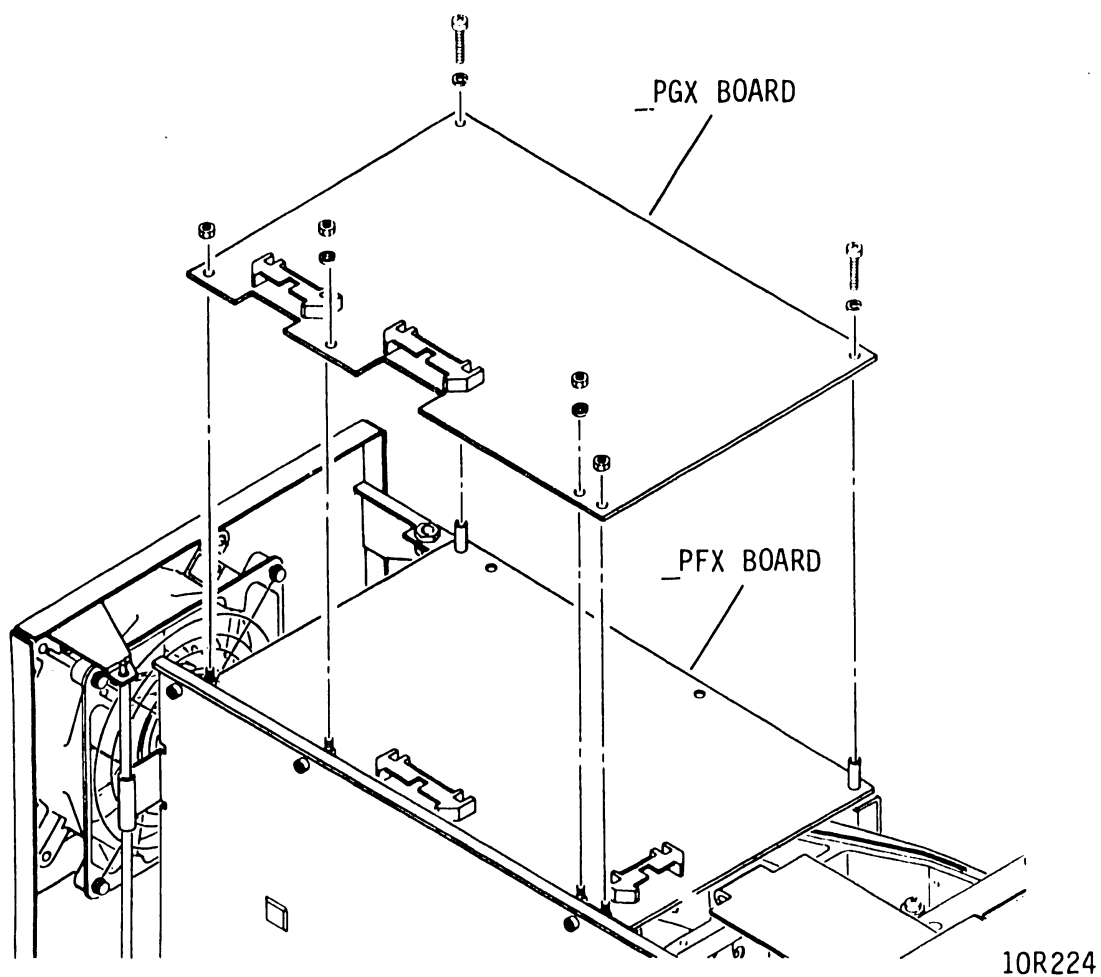


Figure 5-29. _PGX Removal and Replacement

REPLACEMENT

1. Set _PGX board in place on top of _PFX board, align holes, and secure with attaching hardware. See figure 5-29.
2. Connect P27 to J27, P31 to J31 and P36 to J36 on _PGX board
3. Perform top cover replacement procedure (5102).

5302 - _PFX BOARD REMOVAL & REPLACEMENT

The data latch board is mounted beneath the read/write PLO (see figure 5-30). To remove the data latch board it is necessary to first remove the read/write PLO. This is explained in the procedure.

REMOVAL

1. Perform top cover removal procedure (proc 5102).
2. Remove two screws securing _PGX board to bracket and swing board to upright position.
3. Disconnect P30, P32 and P35 from _PFX board.

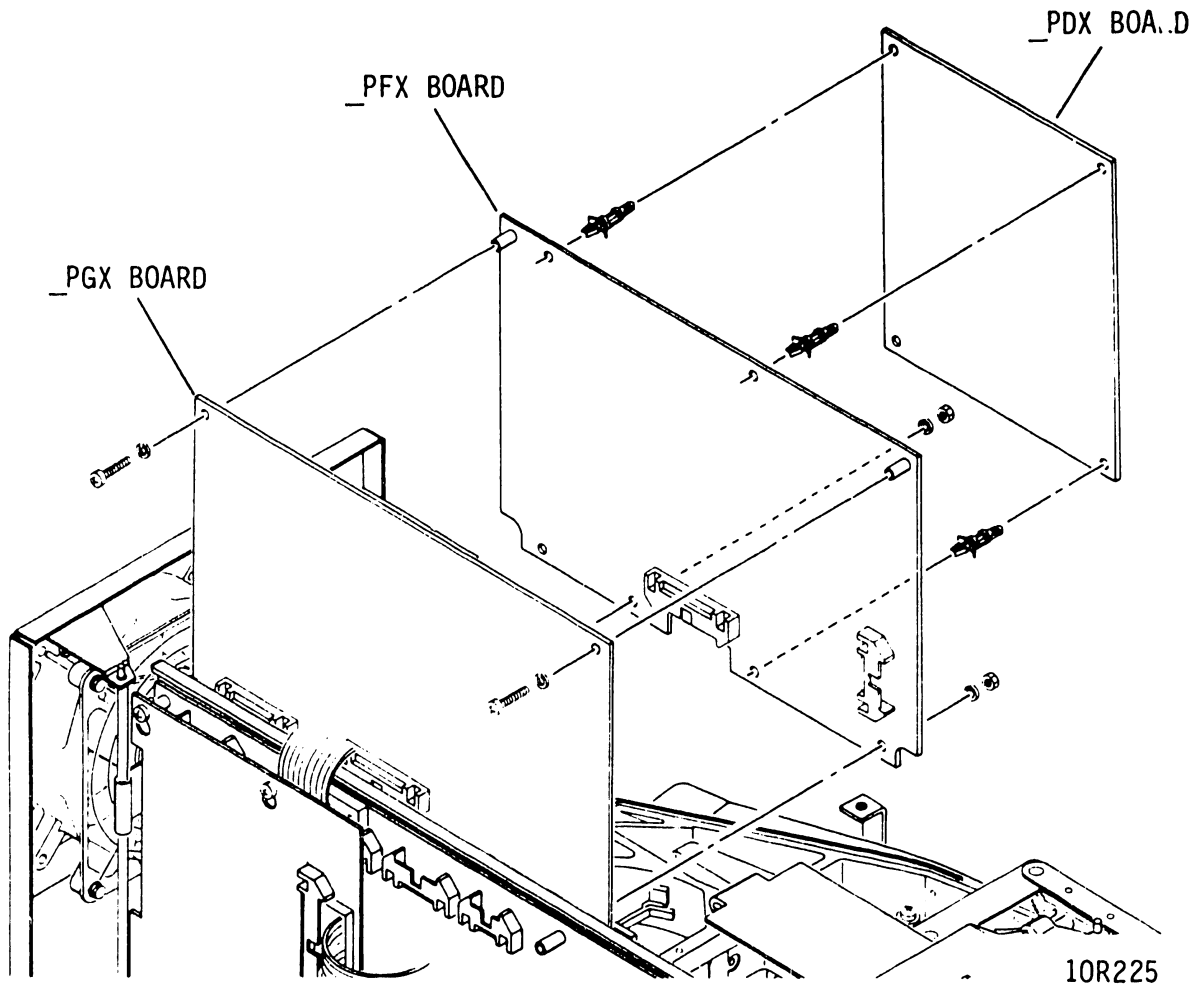


Figure 5-30. _PFX Removal and Replacement

4. Swing _PFX board to upright position and lock into place.
5. Push in on plastic clips and remove _PDX board from _PFX board.
6. Remove attaching hardware and lift ___PFX board from drive. See figure 5-30.

REPLACEMENT

1. Set board in place on top of mounting plate, align holes and secure with attaching hardware. See figure 5-30.
2. Attach _PDX board to plastic clips on _PFX board.
3. Swing _PFX board halfway down and connect P30 to J30 and P32 to J32, by reaching under _PFX board and pushing on back side of connector.
4. Connect P35 to J35 on _PFX board.
5. Move _PGX board to normal operating position and secure with two screws.
6. Perform top cover replacement procedure (proc 5102).

5303 - -EBN/-EDN BOARD REMOVAL & REPLACEMENT

The ___EBN/___EDN board is mounted on the ___PEX board, and is connected to the I/O plate via cables and connectors J2, J3, and J4 (see figure 5-31).

REMOVAL

1. Perform top cover removal procedure (proc 5102).
2. On units with power supply attached directly to slides, remove screws securing front of power supply to slides and tilt supply back far enough to allow access to hardware that secures I/O plate to rear panel. On units with power supply attached to bracket and mounts, remove hardware securing bracket to mounts and slide supply back far enough to allow access to hardware that secures I/O plate to rear panel.
3. Remove I/O cables and/or terminator from J2, J3 and J4.
4. Disconnect P27 from ___PGX board, and P19, P20 and P48 from ___EBN/___EDN board.

5. Remove screws securing I/O plate to rear panel and slide plate out with J2, J3, and J4 attached.
6. Remove connectors J2, J3, and J4 from I/O plate (see figure 5-31).
7. Loosen screws securing EBN/EDN board to drive, then slide board up to free it from screws and remove from drive.

REPLACEMENT

1. Connect P19 to J19, P20 to J20 and P48 to J48 prior to mounting EBN/EDN board.

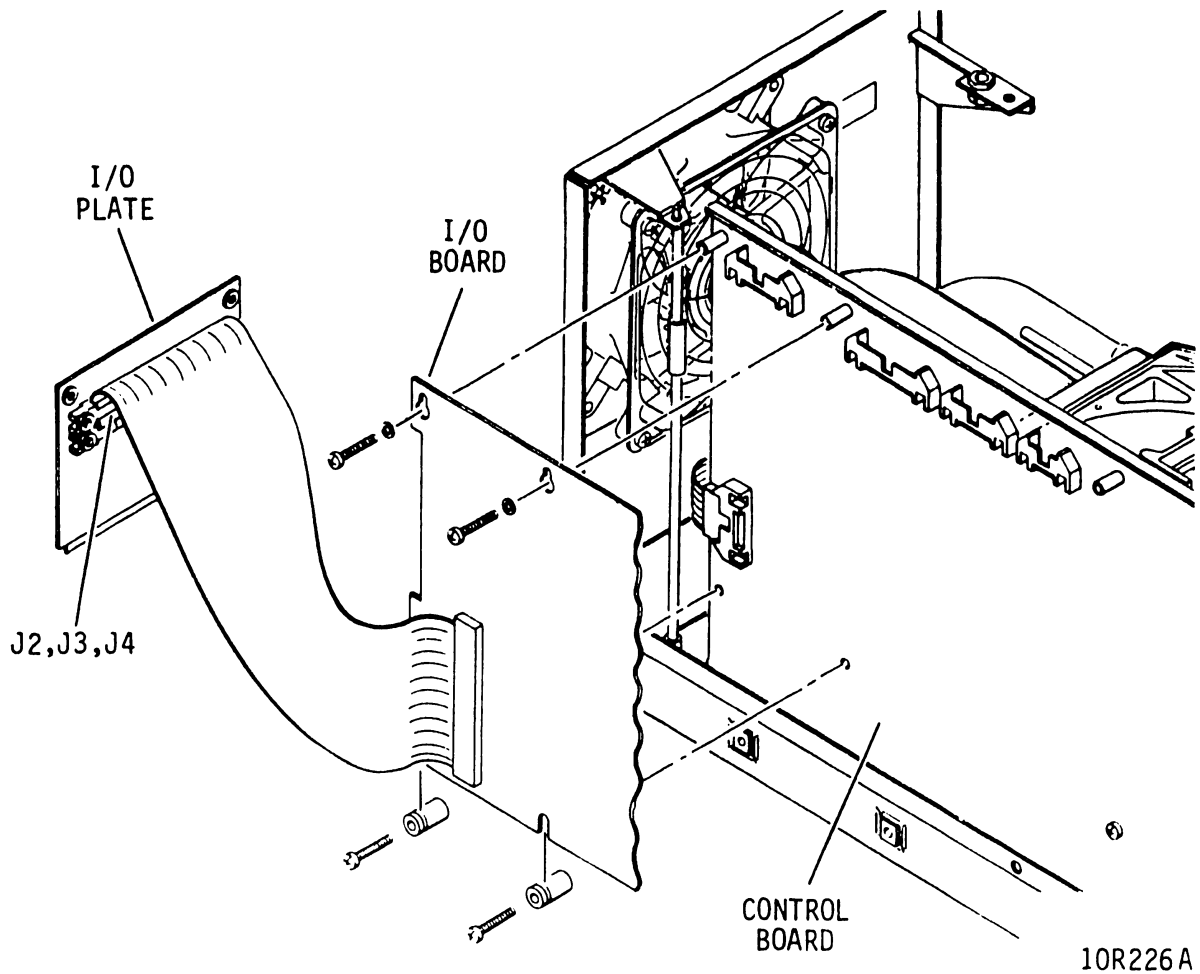


Figure 5-31. EBN/EDN Removal and Replacement

2. Fit __EBN/__EDN board over mounting screws and tighten screws. See figure 5-31.
3. Connect P27 to J27 on _PGX board.
4. Fit J2, J3, and J4 into I/O plate and secure with screws.
5. Slide I/O plate into rear panel and secure with screws.
6. Move power supply into operating position and secure with attaching hardware.
7. Ensure that all switches on the board are set as indicated in the installation section of Hardware Maintenance Volume 1.
8. Perform top cover replacement procedure (proc 5102).

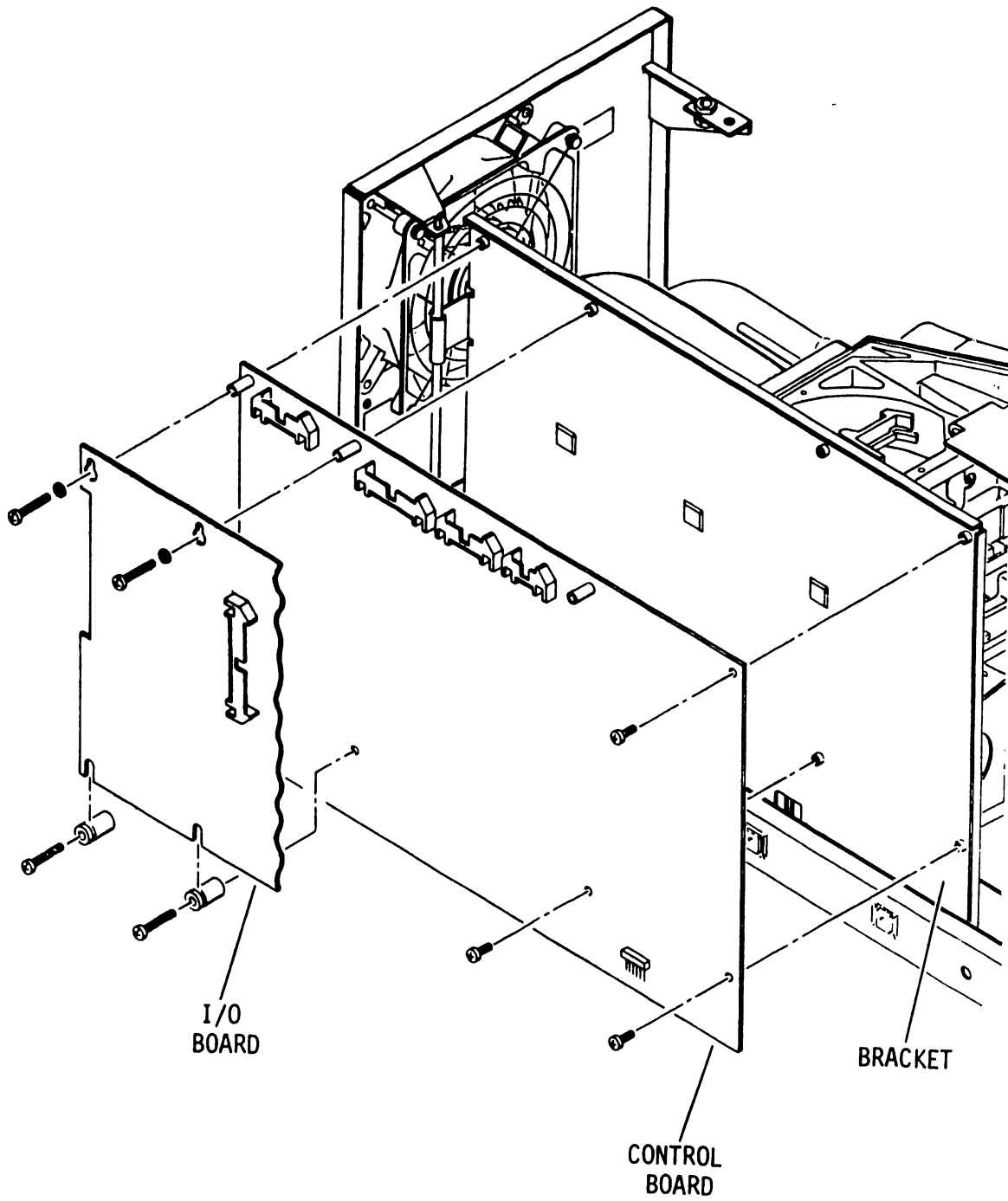
5304 - -PEX BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (proc 5102).
2. Carefully, pry P14 from chip socket and remove cable from _PEX board.
3. Disconnect P27 from _PGX read write board.
4. Loosen screws securing __EBN/__EDN I/O board and lift board up and off to side.
5. Disconnect P23, P25, P26 and P29 from _PEX board.
6. Remove screws and screw posts attaching __PEX board to bracket. Disconnect P21, P24 and P28 as __PEX board is removed from drive. See figure 5-32 .

REPLACEMENT

1. Connect P21 to J21, P24 to J24 and P28 to J28 as _PEX board is being mounted.
2. Align _PEX board to mounting holes in bracket, then install screws and screw posts, and tighten securely. See figure 5-32.
3. Connect P23 to J23, P25 to J25, P26 to J26, and P29 to J29 on _PEX board.



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Figure 5-32. _PEX Removal and Replacement

4. Fit I/O board onto mounting screws and tighten screws.
5. Carefully, connect P14 to J14 socket on _PEX board.
6. Connect P27 to J27 on _PGX board.
7. Ensure that all switches on the board are set as indicated in the installation section of Hardware Maintenance Volume 1.
8. Perform top cover replacement procedure (proc 5102).

5305 - _PCX BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Place main logic in the maintenance position (proc 2101).
2. Remove top air cover to gain access to head cables.
3. Disconnect P42 and read/write head cable connectors from the _PCX board.
4. Remove the two screws securing _PCX board, shield and cover to drive. Remove assembly from drive. See figure 5-33 .
5. Remove _PCX board from assembly.

REPLACEMENT

1. Place cover and shield on _PCX board and install on drive (use shorter screw on inside hole). See figure 5-33.
2. Connect P42 to J42 and read/write head cables to _PCX board.
3. Replace top air cover.
4. Return main logic to normal operating position (proc 2101).

5306 - _UUN BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Place main logic in the maintenance position (proc 2101).
2. Remove side air cover.

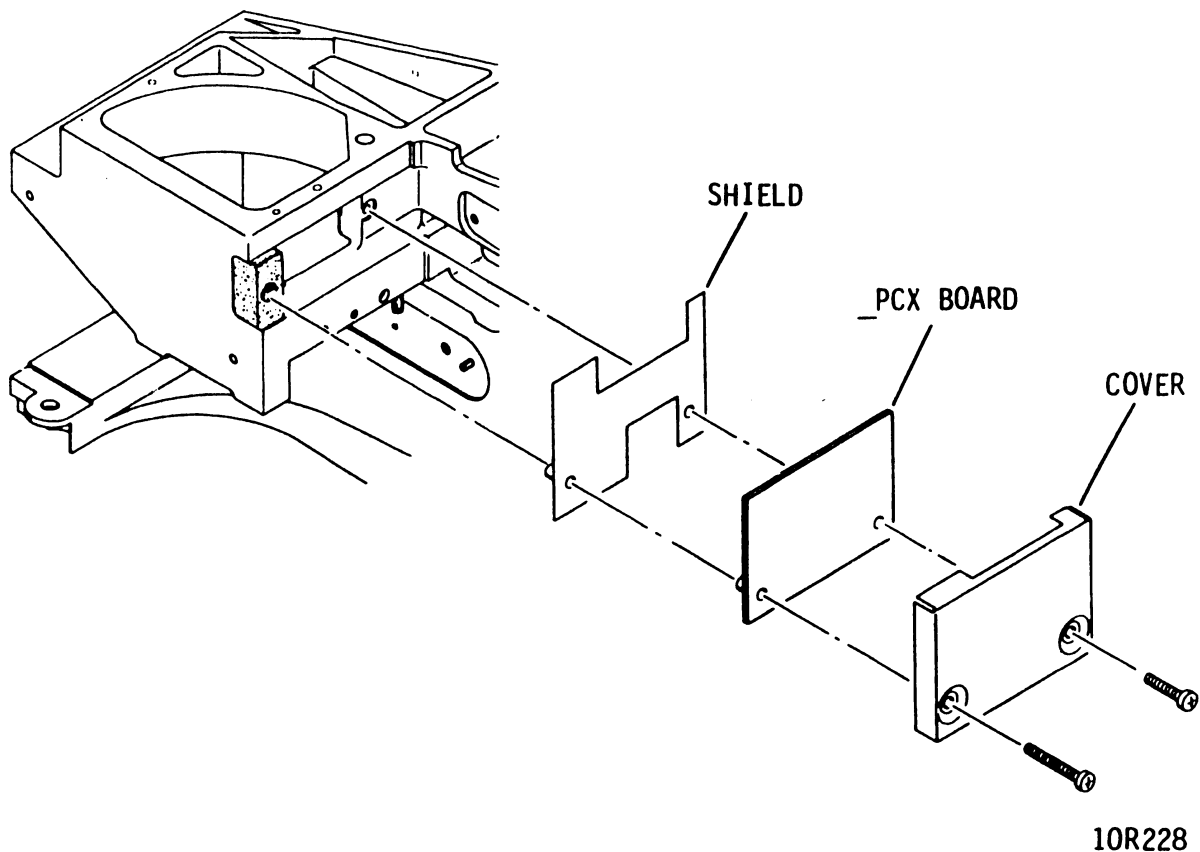
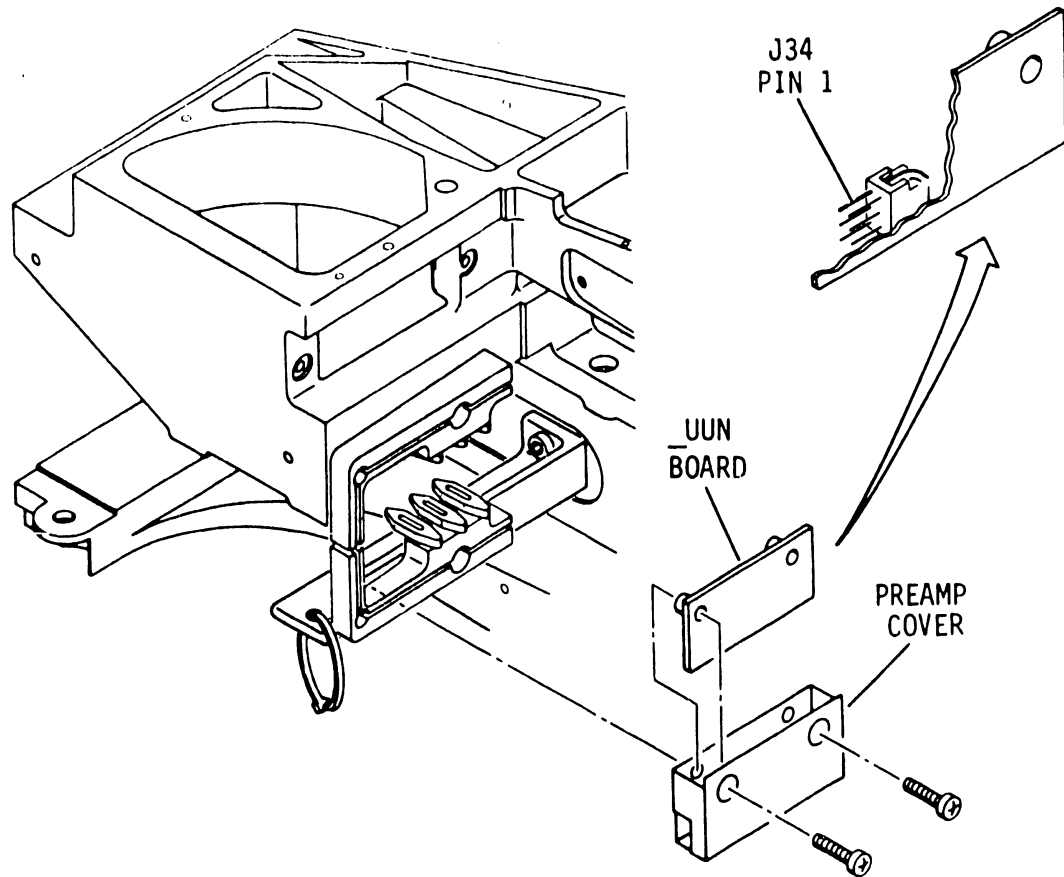


Figure 5-33. _PCX Removal and Replacement

3. Remove the servo head connector from servo preamp board.
4. Remove the two screws securing the servo preamp assembly to drive. See figure 5-34.
5. Disconnect P34 from _UUN card and remove card from assembly.

REPLACEMENT

1. Install _UUN card to assembly and connect P34 to J34.
2. Position servo preamp assembly and secure to drive. See figure 5-34.



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Figure 5-34. _UUN Removal and Replacement

3. Connect servo head connector to _UUN card.
4. Install side air cover.
5. Place main logic in the normal operating position (proc 2101).

5307 - -PDX BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (proc 5102).
2. Disconnect P23 from _PEX control board and feed cable between read/write boards and _PEX board bracket.

3. Remove screws securing read/write boards to support brackets. Swing boards up and lock into place.
4. Disconnect P22 and P43 from _PDX board.
5. Push in on plastic clips to remove _PDX board from _PFX board. See figure 5-35.

REPLACEMENT

1. Install _PDX board onto plastic clips on bottom of _PFX board. See figure 5-35.
2. Connect P22 to J22 and P43 to J43 on _PDX board.
3. Swing read/write boards halfway down. Feed P23 cable between read/write boards and _PEX board bracket.
4. Connect P23 to J23 on _PEX board.
5. Position read/write boards on support brackets and secure into place.
6. Perform top cover replacement procedure (proc 5102).

5308 - _PMX BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure.
2. Disconnect P20 from _EBN/_EDN I/O board.
3. Loosen screws securing _EBN/_EDN I/O board and lift board up and out far enough to gain access to P24 on _PEX control board. See figure 5-36.
4. Disconnect P24 from _PEX board and guide cable through back of unit.
5. Slide _PMX board out far enough to gain access to J37 and J39 connectors.
6. Disconnect P37 and P39 from _PMX board.
7. Remove _PMX board from drive.

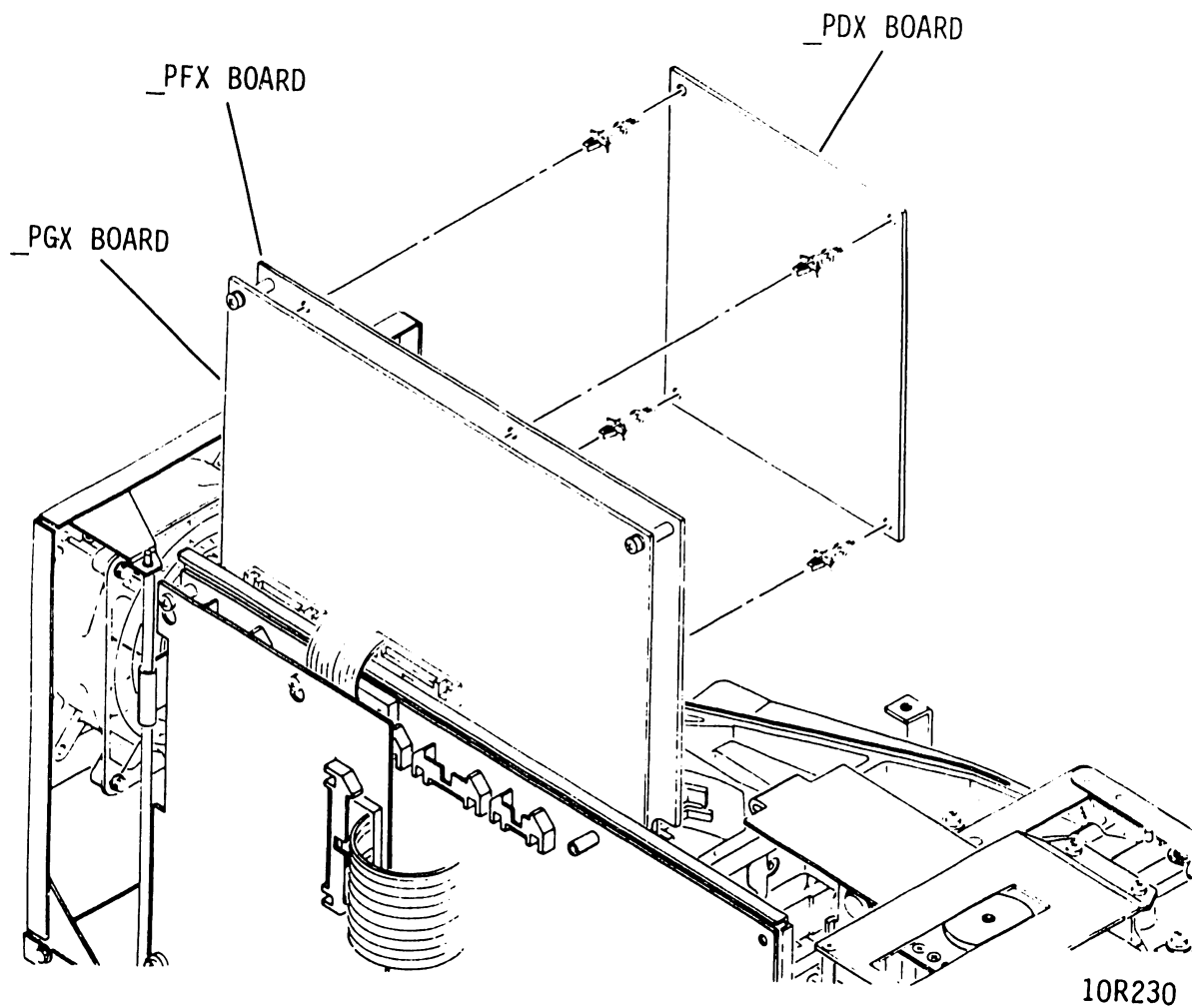


Figure 5-35. PDX Removal and Replacement

REPLACEMENT

1. Slide PMX board in place far enough to connect P37 and P39. See figure 5-36.
2. Connect P37 to J37 and P39 to J39 on the PMX board. Slide board into position.
3. Feed P24 cable along back of unit and connect P24 to J24 on PEX board.
4. Fit EBN/EDN board over mounting screws and secure into place.
5. Connect P20 to J20 on EBN/EDN board.
6. Perform top cover replacement procedure (proc 5102).

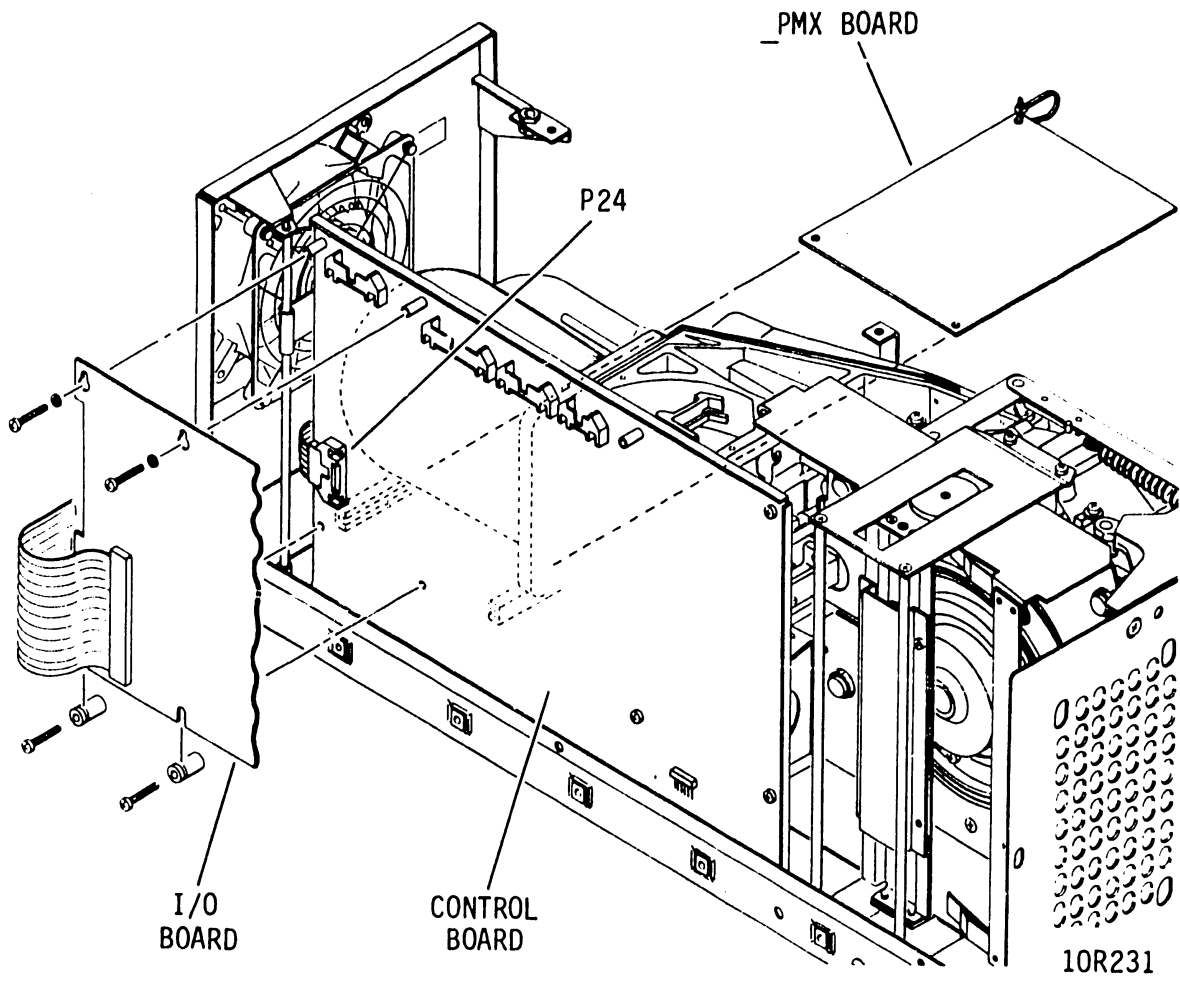


Figure 5-36. PMX Removal and Replacement

END