CUSTOMER ENGINEERING DIVISION

MODEL 928 SYSTEMS 10/20/30

FIELD-LEVEL MAINTENANCE MANUAL

PRELIMINARY VOLUME 3 THEORY OF OPERATION

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SECTION 1
INTRODUCTION

1.1 SCOPE

This preliminary maintenance manual is Volume 3, the last of three initial volumes planned for publication on Wang Model 928 Word Processing Systems 10, 20 and 30.

The contents of each volume will include the subject matter as listed below.

VOLUME I

A basic Service Manual that includes System Installation, Operation, Simplified Theory of Operation including block diagrams, system diagnostics and aspects of servicing and compatibility of system software and sub-units. This document will be made available to all service personnel.

VOLUME II

Will contain a complete set of schematics, ECNs, Bill of Materials (BOM), Mnemonics listings, Furniture, etc. This document will be made available to all service personnel.

VOLUME III

Detailed Theory of Operation for all 928 WP systems. This document will be distributed to Area, District and Subsidiary service offices. Copies will be available from Area offices to interested service personnel only on a request basis.

1.2 PURPOSE

The purpose of this volume is to provide a system theory of operation for interested field personnel. Its intended use is directed to those individuals which may now be able to direct field repairs of equipment which had heretofore been returned to the factory. This volume provides a ready reference to more fully understand the 928 system of operation.

1.3 DESCRIPTION

For purposes of this volume, the 928 word processing system has been divided into four major subdivisions as follows:

A. Master - (CPU, Storage, Floppy Disk, Hard Disk)
B. Workstation - (CRT, Keyboard)
C. Printer - (Daisy)
D. Options - (Matrix Printer, PIO, T.C., etc.)

The 10A, 20 and 30 systems are composed of various combinations of the above listed subdivisions.

The information contained in this volume is primarily concerned with the detailed theory of operation via the printed circuit boards used in the subdivisions mentioned above.

The theory is presented at the chip/component level.

Each subdivision is considered a separate information area within itself; i.e., all PCBs of Master, all PCBs of Workstation, all PCBs of Printer, Options (varied selection).

The topics of discussion (the PCBs) within each subdivision are arranged in numerical sequence according to the PCB part numbers

within that section; e.g., Subdivision=Section 2=Master, the first topic is Master Memory (PCB #7201), the second topic is Master CPU (PCB 7202), the third topic is Master Disk Controller (PCB 7203), etc.

For common PCBs, such as power supplies/regulators and motherboards, only a brief statement and the schematic are provided.

If this volume is read from front cover to rear cover, it may be noticed that there are some information areas which appear repetitive. However, it is the basic philosophy of this volume to enable an individual to refer to any part for reference and information. Therefore, relative situations occur to many independent operations but this relatively must be expressed each time in order to fully explain the operation; hence the appearance of repetitive operations - (relative situations common to many opeations).

The following questions and subsequent answers can locate specific areas within this volume.

Which major subdivision do I wish to examine (choice of 4 areas)?

Once in the appropriate subdivision, which board do I wish to examine (paragraphs are numbered sequentially in relation to the PCB part number)?

What illustrations are available to me? (Each major paragraph has as a minimum the board schematics at the end of the paragraph. In most cases a block diagram and timing diagram are available at the beginning of each section - usually as the 2nd and 3rd page of that section.)

Are the appendices of any aid to me? (appendices, located at rear of volume contain relevant text/table material)

1.4 BLOCK DIAGRAMS

Block diagrams are provided for each printed circuit board discussed in detail. The text of this volume is written directly to the block diagrams and schematics. The block diagram for each PCB gives a ready reference of operation and direct general tie-in to the schematic.

The block diagrams can be readily referenced to a specific page by examining the list of illustrations located in the front matter at the beginning of this volume.

1.5 TIMING DIAGRAMS

In most cases, an overall timing diagram has been provided at the beginning of each major subdivision (usually as the 2nd or 3rd page of the section). For the Wang options subdivision, the timing diagrams are contained within the major paragraph being discussed. In some instances specific timing diagrams have been illustrated within the subparagraphs to permit a closer look at a major operational element.

Timing diagrams can be readily referenced to a specific page by examining the list of illuatrations located in the front matter at the beginning of this volume.

1.6 SCHEMATICS

Schematic illustrations are provided for every printed circuit board. Therefore, in some cases such as power supplies/regulators and motherboards, only a brief statement may exist due to the simplicity of the intended operation. However, a schematic illustration will always be available as the last page(s) of that PCB discussion regardless of descriptive brevity.

The schematic illustrations can be readily referenced to a specific page by examining the list of illustrations located in the front matter at the beginning of this volume.

1.7 APPENDICES

As an aid to understanding this theory of operation, four appendices are presented for easy reader reference.

1.7.1 APPENDIX A - Mnemonic Code

All the menmonics used in this volume and on the schematics are presented in Appendix A.

1.7.2 APPENDIX B - Glossary

Because of the moot definitions of many words and phases, a glossary of terms is presented as Appendix B so that the reader will never be in question concerning a specific definition.

1.7.3 APPENDIX C - Related Publications

Where possible reference has been made to those documents which either initially explain on further enhance the contents of this volume; and these relevent publications have been listed in Appendix C.

1.7.4 APPENDIX D - R7 Prom Flow Diagram

A flow diagram of the R7 Prom is presented in Appendix D to aid the reader in understanding the basic "start-up" sequence of the system.

1.8 "BARRED"/LOW SIGNALS

For ease of preparation and to aid reading clarity the typical "barred" signal symbol has been replaced by an asterisk.

e.g., $\overline{\text{SIE}}$ ("Barred" Signal) = *SIE (Asterisk Signal)

SECTION 2

MASTER THEORY OF OPERATION

SECTION 2
MASTER THEORY OF OPERATION

2.1 MASTER MEMORY - 7201

2.1.1 GENERAL DESCRIPTION (Figures 2-1 and 2-4)

Master memory #1 PCB 7201 contains 16K of RAM memory divided into 4 banks of 4K each. A PROM memory is installed on the board containing 1K of memory. There are provisions for an additional 3K of PROM memory for future use. Both RAM and PROM memories are bank selectable. The addressing of RAM memory is shared by three functions controlled by a Priority Function Decoder. The three functions are in order of priority:

1) DMA (Direct Memory Access)
2) 8080A (Microprocessor addressing)
3) REFRESH (a periodic recharge of RAM memory)

The master memory board includes the 8080 READ/WRITE decoder, memory data access buffers and registers with associated enabling clocks and FIFO control. FIFO control is a logic timing arrangement for internal DMA bidirectional 256-byte data transfers between the system disk, master memory and slave memory units. A 256-byte FIFO (RAM) memory is an intermediate temporary storage area on the Master data link board during data transfers. FIFO control furnishes the address control and I/O buffer clocks for FIFO when storing and accessing the 256 bytes of data being transferred.

2.1.2 8080 ADDRESS BUS - PROM

The 8080 address bus is used to access PROM memory. The single 1K PROM chip presently being used is L18. The storage capacity of L18 is 1024 8-bit bytes, requiring 10 address bits A0 through A9. A10 and A11 are used for BANK decoding. BCD to DECIMAL decoder L43 is used for BANK select (L18 is Bank 0). Address

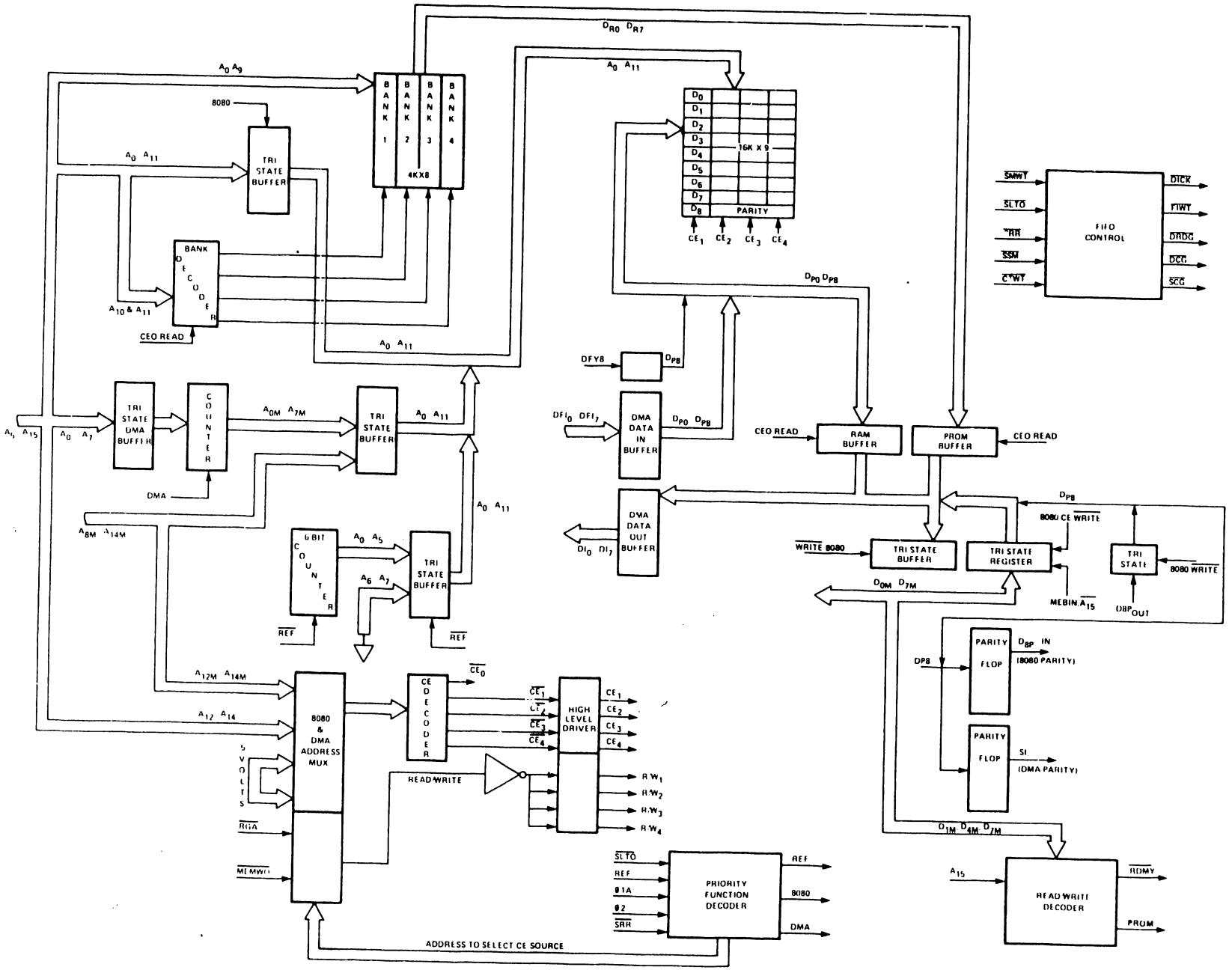


Figure 2-1 Master Memory-Block Diagram

bits 10 and 11 will be low at the input of L43 decoder producing a low output enabling L18. C and D inputs to L43 are tied together and controlled by the 8080/DMA address multiplexer logic which consists of L60, L56 and L77. The decode procedure will be discussed below. L56-1 output is a low while L77-7 output is a high, producing a low at the output of gate L69-3 which is wired back to L43 pins 12 and 13. PROM L18 contains the start-up BOOTSTRAP program required to bring the word processing system to its READY state. See Appendix D for the flow chart of the R7 PROM (L18) bootstrap program.

2.1.3 8080A ADDRESS BUS - RAM

The access to the master RAM memory using the 8080 address bus is enabled when the PRIORITY FUNCTION DECODER output from L91-10 (8080) is active low. This low level is applied to L19 and L20, pins 1 and 15 gating A0-A11 address lines direct to RAM memory. The twelve address lines will access 4096 bytes of data with parity from any one of the 4 selected banks. The decode for selecting one of the four RAM memory banks is located in the 8080/DMA address multiplexer logic.

2.1.4 8080/DMA ADDRESS MULTIPLEXER

Two DUAL 4-line to 1-line data selector/multiplexers L60 and L77 are used to select the desired RAM memory bank and enable the selected bank for a READ or WRITE. The multiplexed high address bits for the 8080 bus (A12, A13 and A14) and DMA bus (A12m, A13m and A14m) are combined with the address (A,B) function select inputs for the bank decode. The address bits are coded from the PRIORITY FUNCTION DECODER L92, pins 5 and 9 and represent the 3 binary combinations 00(DMA), 01(REF), and 10(8080). A BCD to DECIMAL memory bank decoder L56 has a five selection output. All outputs from L56 are active when low. A PROM read decode is a low at output L56-1. Outputs from L56-2, 3, 4 or 5 will enable one of the four RAM banks. Chip Enable (CE) is the clock for the R/W of RAM memory. CE is generated in the master clock and is 409.5 ns in duration. L14 and L55 are dual drivers required to enable all four RAM memory banks. The drivers are enabled by four L40 NAND gates used as OR gates for 8080 and REFRESH functions. The

READ/WRITE command for RAM memory is applied to all banks simultaneously from Hex Inverter Driver Buffer L30 which has all inputs tied together. The R/W signal from L77-7 Selector/Multiplexer is decoded from the DMA disk signal RGA and the 8080 signal*MEMWO. If the output at L77-7 is low, a WRITE is selected whereas a high output selects a READ.

2.1.5 PRIORITY FUNCTION DECODER

The priority of the DMA, 8080 and REFRESH functions for accessing RAM memory are as stated. For 8080 functions, the READ/WRITE decoder will be pertinent to this discussion. An explanation of the decoder follows:

A dual D-type edge-triggered F/F L88 latches either the DMA or the REFRESH requests by resetting the previously preset F/Fs making either output active low. An asynchronous DMA request at L75-pins 9 and 10 requires inputs*SLTO (Master select) and*SRR (Disk Read Request). The request is latched on the trailing edge of the input signal. A REF signal also clocks its request on the trailing edge. These requests, once set, will remain set until processed and reset. The request is synchronized by a *PHASE 2 clock at the input of D-type F/F L89 with an override reset of a permanently wired preset gate. The output of L89 is active low for either DMA or REF for the duration of*PHASE 2. At the input of L90 (8-line to 3-line priority decoder) the 8080 function from the 8080 R/W decoder L96-6 joins the DMA and REF inputs at pin 6 for priority selection at outputs A0 and A1 (outputs are active low).

The selected priority function is then clocked into L92 latch at PHASE 1A time which is 58.5 ns after PHASE 2 goes active. The output pins 5 and 9 are select bits used by L60 and L77 for address and R/W multiplexing as well as for function decode outputs at L91. The dual 2-line to 4-line decoder L91 receives inputs from L92 which are decoded into (two output) active low control signals which provide the following:

1) DMA--The output at L91-9 enables the address buffers L44 and L45, increments the 256 byte DMA address counter L42 and clocks the data read into the 4-bit D-type 3-state registers L82 and L83 onto the DMA out bus.

If the decode is a DMA write, buffers L63 and L64 are enabled for data in from the DMA bus. Three gates L79, L84 and L97 are logically arranged to control the DMA data in and out. Parity is checked in the data link for all bytes to and from master memory. The DMA out of L91-7 is used to reset the original DMA request which is a preset.

2) REFRESH--The REF request is an active low and processed identical to the DMA. REF is a clock 585ns in duration which occurs every 19 us but lowest on the priority list. REF at the output of L91-11 enables all four drivers for all RAM banks to allow the same row in each bank to be refreshed simultaneously during each CE. This method provides all 64 rows of each bank to be refreshed a minimum of every 1.2 ms. Maximum time allotted for REF is approximately 2 ms. This same REF signal also gates the row address onto the address bus from HEX inverter buffers L3 and L4. Signal REF from L91-5 resets the REF request F/F.

3) 8080 READ/WRITE DECODER--The 8080 R/W decoder utilizes address bit A15 and the READ or WRITE status byte to initiate a R/W function. The address bit A15 must be low for accessing master memory. A WRITE status word will gate a low output from L94-12 to L95-2. When L95 is clocked by PHASE 2 and SYNC from gate L96-8, a reset of the WRITE F/F produces an active low at L95-5 for a period of 585 ns gating a low output at L96-6. This low is the 8080 write request at L90-6. The same procedure for an 8080 read occurs when a READ status byte and address bit A15 enable an active low at gate L94-6. The 8080 R/W request is inverted twice by two NAND gates to generate RDMY at L97-11. RDMY

(READ MEMORY) is active low and forces the 8080 into a busy (WAIT) state to insure that the accessed data from memory is stable on the data bus. An 8080 R/W function at the dual output of L91 of the priority function decoder enables the 8080 address buffers L19 and L20. The other output at L91-6 resets the 8080 R/W request and also presents a positive going delayed clock through L79 to L98-3. L98-6 is set low inhibiting PHASE 1A from resetting the 8080 function until the next SYNC pulse and PHASE 1A pulse are coincident at gate L97-6 clearing the inhibit. This is a cycle steal to guarantee the access of good data. A preset of L98 F/F #2 is used to inhibit a parity check of PROM data in the Master CPU during start-up and reset. A low signal from L69-3 to L84-13 sets PROM. PROM is also cleared by the same clear gate that clears F/F #1.

2.1.6 DMA ADDRESS BUS

The 8080 address bus is split into 8-HIGH ORDER and 8-LOW ORDER bits for all DMA addressing functions. DMA addressing is multiplexed for controlling 1-BYTE and 256-BYTE transfers. The scheme for DMA addressing of MASTER MEMORY is identical to the 8080. Twelve address bits (A0m-A11m) are used for accessing the same number of addresses and A12m-A14m for bank selection. The DMA high and low order byte address bits are routed to the data link for addressing the slave units. The DMA addressing of master memory for a WRITE command will require a data transfer from the disk controller whereas a READ of master memory would be a data transfer to the disk controller. The DMA low order address bus is multiplexed for 1-byte and 256-byte transfers using L58 and L59. The output bits (A0m-A7m) are routed to the 7214 data link board. If the select is 1-byte, the actual low order address goes to data link. If the select is 256-byte, the low order address output to the data link is all zeroes. L41 and L42 are binary counters that are not presettable but are cleared by signal OB/C prior to any 256-byte transfers. The counters are incremented and HEX inverter buffers L44 and L45 are enabled during each DMA priority decode providing sequential 256-byte low order addresses to

memory for each R/W command. High order address bits (A8m-A11m) are routed from the Master CPU to permit 4K addressing. Each byte of data is addressed to or from memory while under the DMA control of the PRIORITY FUNCTION DECODER.

2.1.7 ROW REFRESH CIRCUIT

A REF signal from the Master CPU is sent to master memory every 19 us providing a clock for latching the refresh request into L88-11. When the request is processed, the output from L91-5 (REF) enables HEX inverter buffers L3 and L4 which present ROW address bits A0-A5 onto the address lines. Address lines A6-A11 are inhibited during refresh. Two 4-bit binary counters L1 and L2 are clocked by each REF pulse for 64 counts and continues to repeat the count incrementing the 64 row addresses and recharging each row approximately every 1.2 ms.

2.1.8 FIFO CONTROL

The FIFO control logic is intermediate timing circuitry required to transfer data bidirectionally over the DMA data bus. The internal transfer of data is involved with the DISK and the DATA LINK paths to and from the SLAVES. The transfers are timed to meet the slower access time required to perform the disk read and write functions. Data on the DMA bus read from the disk or data read from slave memory to the DMA bus requires a temporary storage area called FIFO (256 byte RAM storage) to adjust to the transfer timing sequences generated by FIFO CONTROL.

2.1.8.1 FIFO Control - 256 Byte Write (Read Disk and Write Data to Slave)

In this type of operation, 256 bytes of data will be transferred to the Master Data Link FIFO memory from the disk controller. When the FIFO memory is filled, a 256 byte Write to slave memory will be initiated by the Master Data Link (MDL) across the coaxial cable.

When the FIFO memory is completely emptied, OPCOM (Operation Complete) will be generated by the MDL to clear the DMA control circuitry on the Master CPU.

The Master CPU selects the disk drive for accessing data (READ). The Master then sends the TRACK and SECTOR data to the disk controller for the area to be accessed.

The MCPU then selects the SLAVE that will receive the data and issues the address (PAGE OF MEMORY) where the 256 bytes of data will be stored.

When the disk drive READ head is on TRACK the MCPU will read the disk controller sector counter. When the READ head is one sector from the sector to be read, the MCPU issues an*OUT B command which causes the disk controller to read the next sector. *OUT B also sets the Data Read*(DRD) F/F on the MCPU and causes the Slave Memory Write*(SMWT) signal to go active. *SMWT is the DMA R/W signal.

The following events occur during the 256-BYTE WRITE:

1) The 256 Byte transfer signal (256 BYTR) is presented to the Instruction buffer at L96-6 on the Master Data Link to initiate a DMA transfer to slave memory after the FIFO memory has been loaded from disk.

2) While the disk controller performs the read, it generates the signal*SRR (Set Read Request) after each byte (eight bits) has been read from the disk and serially loaded into the controller S/P register. *SRR is routed to the FIFO CONTROL logic on the Master memory board.

3) SRR*is NORed with*DRDG (Disk Read Gate) to develop a*FICK (First In Clock) signal that will load the disk data into the input buffer register for FIFO on the MDL.

4) SRR*is also used to generate a*DCG (Disk Counter Gate) and FIWT*(FIFO Write) signal (outputs from FIFO CONTROL) which will first write the data into the FIFO*(FIWT) and then step the FIFO address counter to the next logical address *(DCG).

5) This sequence will continue until the FIFO is full (256 Bytes):

   a) Read serial data from the disk and assemble 8 bits in the disk controller S/P register.

   b) Develop*SRR on the controller which generates a*FICK on the FIFO control used to write data into the input buffer of the FIFO memory.

   c) The trailing edge of*SRR clocks a FIFO write request into F/F L73-8 on the next PHASE 2 clock. This generates*DCG and*FIWT to write data from the FIFO input buffer to FIFO.

   d) The trailing edge of*DCG will increment the FIFO address register to the next logical address.

   e) When the FIFO is full, the DCE F/F on the the MDL will set and flag this condition. DCE (Disk data complete) is ANDed with 256 BYTR and SMWT producing signal 256SD initiating an Operational Start (OPS) for transferring data to the selected slave.

The portion of FIFO CONTROL used to access data from FIFO and write it onto the system disk during a 256-byte read of the selected slave memory is as follows:

2.1.8.2 FIFO Control - 256 Byte Read
(Read Slave Memory and Write to Disk)

In order to perform a slave memory 256 byte transfer to a system disk, data must be read from the slave memory and transmitted to the Master Data Link (MDL). The data will be written into FIFO memory on the MDL. There is no requirement, as there was in the case of a slave memory write, for the disk controller to wait until the FIFO is full to commence addressing data from FIFO and writing it onto the disk.

When the slave desires to transmit data to the disk, it will initiate a request to the master to perform a disk write from a specific page of slave memory and from a selected slave.

The Master CPU will put the page address into the page address register, select the slave memory to be accessed and the system disk drive which is to write the data.

The Master CPU will then output to the disk controller the track and sector of the disk to be written, and begin reading the sector counter to determine when the head is one sector away from the sector to be written. When this occurs, the MCPU will issue an OUT 0C command (Disk Write).

The data transfer from the slave to FIFO memory is covered in the MDL discussion. The FIFO CONTROL does not become active until the signal*SSM (Send Slave Memory data) becomes active on the MDL.

SSM*becomes active after the first byte of data is loaded into FIFO from slave memory.

The following steps are performed by FIFO CONTROL:

a) SSM*develops*SCG and*FICK clocks. *FICK will clock the data, assembled by the MDL S/P register, into the input buffer of the FIFO. *SCG will enable a*FIWT to write the first data word from the buffer into FIFO.

b) The trailing edge of*SCG will increment the slave address to the next logical FIFO address.

c) After each word is loaded into the S/P register the above steps are repeated until 256 bytes of data have been received by FIFO memory on the MDL.

d) Because there is no requirement for the disk controller to wait until the FIFO has completely loaded, the controller will issue an*SRR when it is at the point where it must write the first byte of data onto the disk.

e) SRR*will again activate the FIFO control to output disk data in clock*DICK that loads the FIFO output buffer and a DCG*that will step the FIFO address counter to the next address to be read. *DICK enables the data byte onto the disk Data In bus*DIO-DI7.

f) SRR*will be generated 256 times for the complete page of data. When FIFO is emptied the DCE F/F will again flag the end of a 256 byte read of slave memory and the write of 256 bytes to the disk.

2.1.9 MASTER MEMORY DATA BUSSES

Access to master memory for external R/W operations include PROM and RAM memories. PROM is a read only device and accessed by the logical decode of memory bank select and R/W decode at the output of L69-3 which enables data out of buffers L61 and L62 with no parity. The PROM data is then latched by L80 and L81 onto the 8080 bidirectional bus by a memory read and address bit A15 (not active). Data is written into RAM from the 8080 bus during an 8080 function when gate L84-3 enables inverter buffers L65 and L66. A parity bit is stored with each byte. Data from the data link with parity (DF10-DF17, DPY) is written into RAM when inverter buffers L63 and L64 are enabled by a DMA function and decoded WRITE signal at the output of L84-8. Data read from RAM and gated onto the DMA bus (DIO-DI7, SI1) is clocked into latches L82 and L83. The parity bit SI1 is controlled separately by a HEX inverter buffer L63 and picked up on the data link board with serial data. The clock is a negative going pulse of 409.5 ns duration being enabled by CE which is the length of time that the data appears on the DMA bus. The clock is gated out of L97-3 which also clocks the parity bit out of L68 for the 8080 bus as well as the DMA bus. Two separate clocks are used for gating each parity bit separately onto their respective busses.

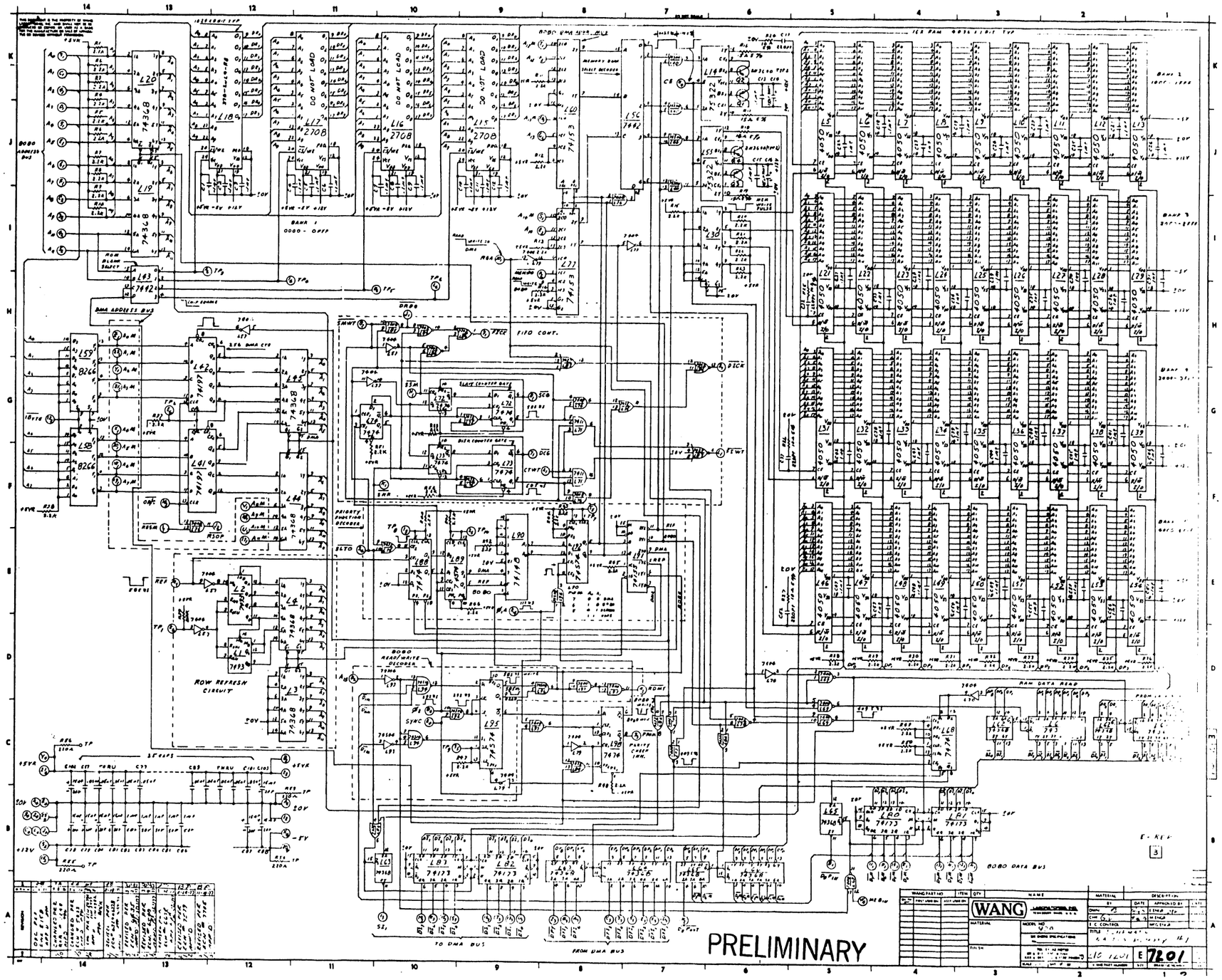


Figure 2-2 Master Memory-Schematic Illustration — Sheet 1

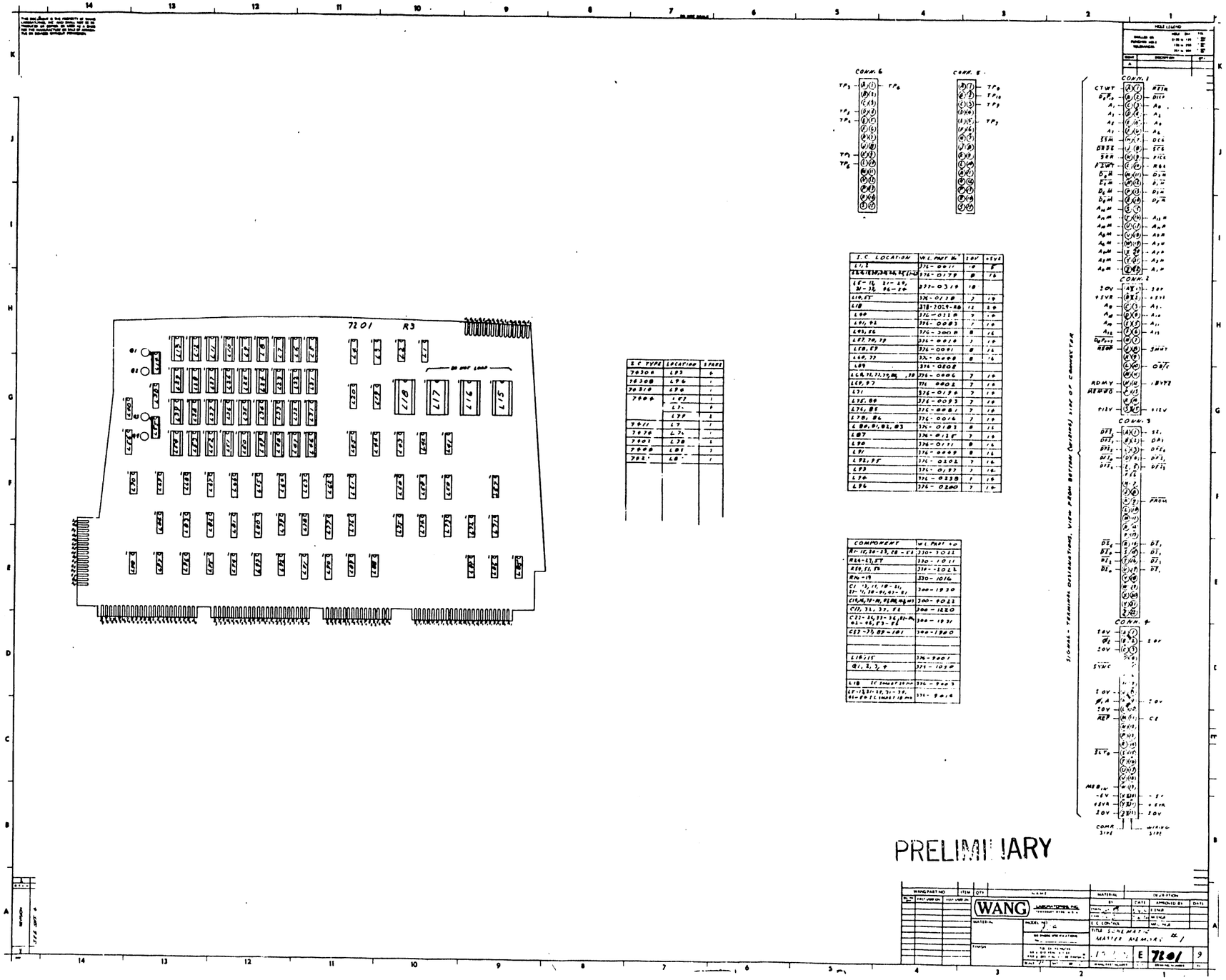


Figure 2-2 Master Memory-Schematic Illustration — Sheet 2

2.2 MASTER CENTRAL PROCESSING UNIT (CPU) - 7202

2.2.1 GENERAL DESCRIPTION 8080A MICROPROCESSOR (Figures 2-3 and 2-4)

The 8080A microprocessor L71 is a single chip packaged in a 40 pin dual in-line plastic housing that allows for easy interfacing. The 8080A has a 16-bit address bus, an 8-bit bidirectional data bus and fully decoded, TTL-compatible control outputs. The 16 address bits support up to 65K of mixed RAM and PROM memory as well as having the capability of addressing up to 256 input and 256 output ports (maximum number presently used is 21). The timing clocks used for the 8080A are generated from an external 17.10 megahertz crystal oscillator. The following discussions will include all circuitry used on PCB 7202 (MASTER CPU) that is required to support the word processing functions of the 8080A.

2.2.2 SYSTEM (MASTER CLOCK) TIMING

The master clock timing circuitry consists of eight D-type flip-flops L55 and L56 in MSI package (74174) driven by a 17.10 MHZ crystal oscillator. The F/Fs operate as frequency dividers to generate the critical PHASE 1 and PHASE 2 clocks used to control the 8080A (see Figure 2-5 A & B). These two clocks, when referenced to the master clock frequency CK (58.5 ns), operate at a divide by 10 frequency, each clock occurring at a 585 ns rate. PHASE 1 and PHASE 2 are none overlapping clocks (see Figure 2-4) and are used as the STATE time clocks, T1, T2, T3, etc., for each 8080A instruction Machine Cycle Time (MCT). 8080 instructions (78 total) are a minimum of one MCT in duration and a maximum of five. (See Figure 2-5A.)

Internally, the 8080A generates additional control clocks SYNC, DBIN and WR using Phase 1 and Phase 2. These clocks provide the timing for the following functions:

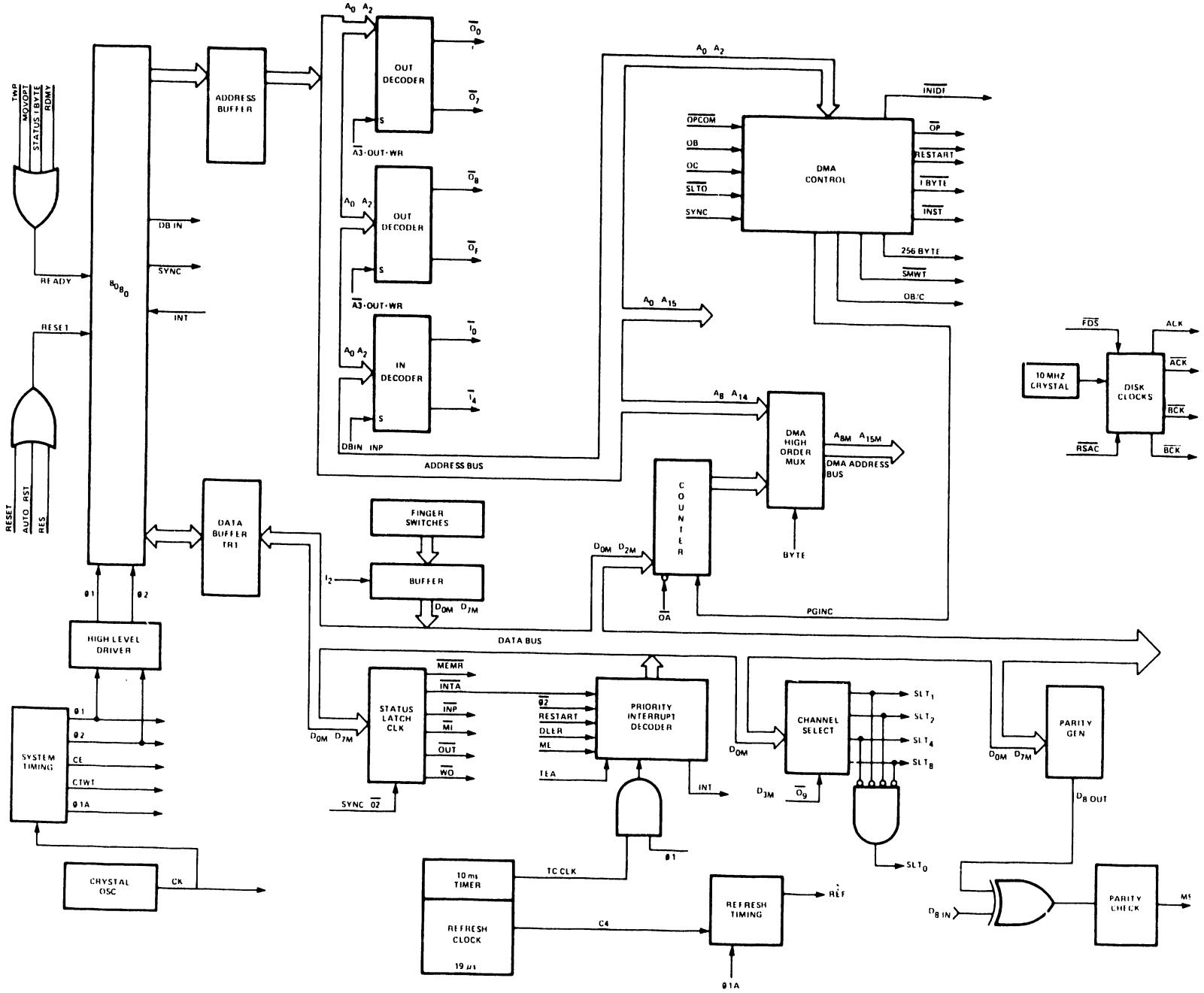


Figure 2-3 Master CPU Block Diagram

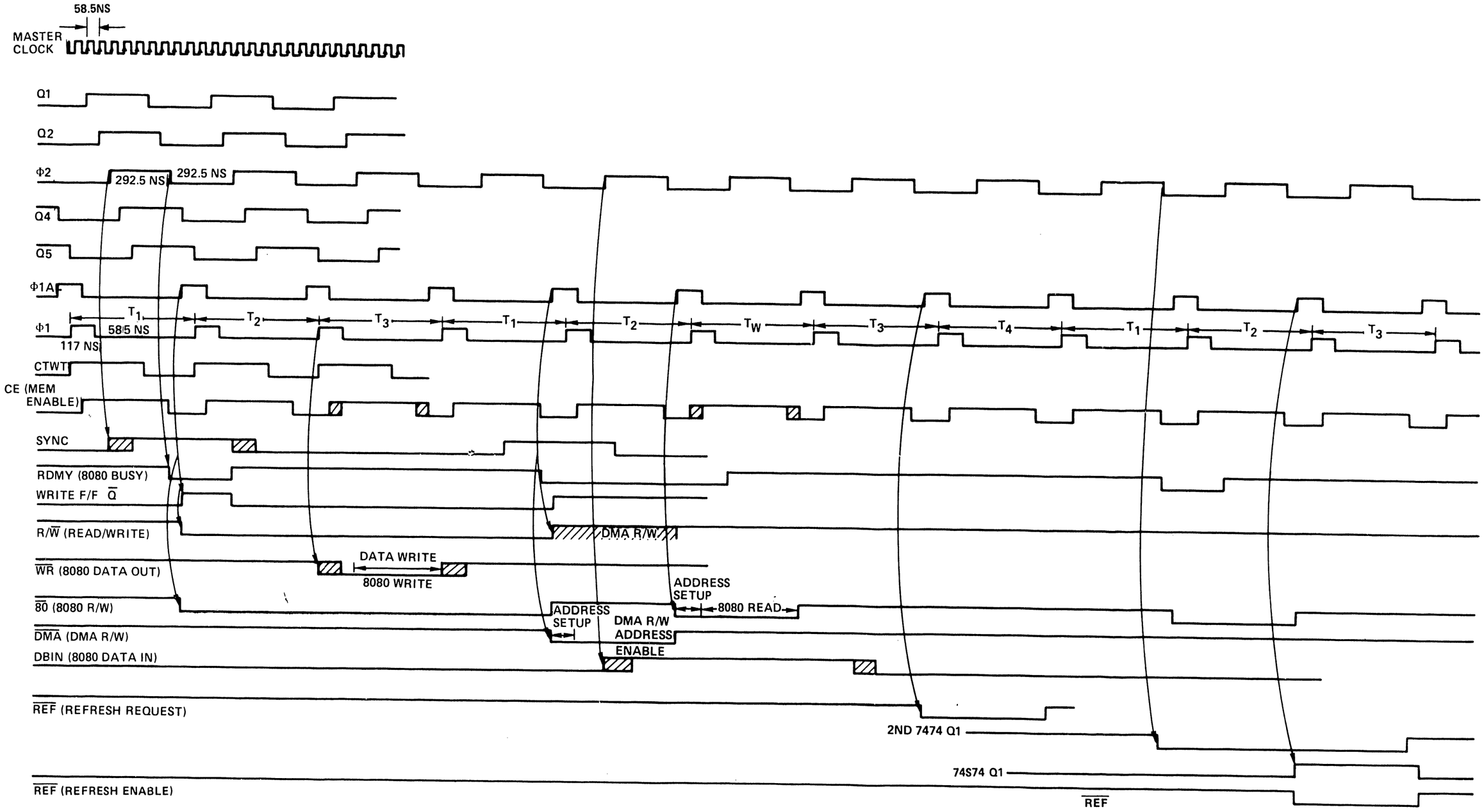


Figure 2-4 Master CPU-Timing Diagram (Includes Master Memory Timing)

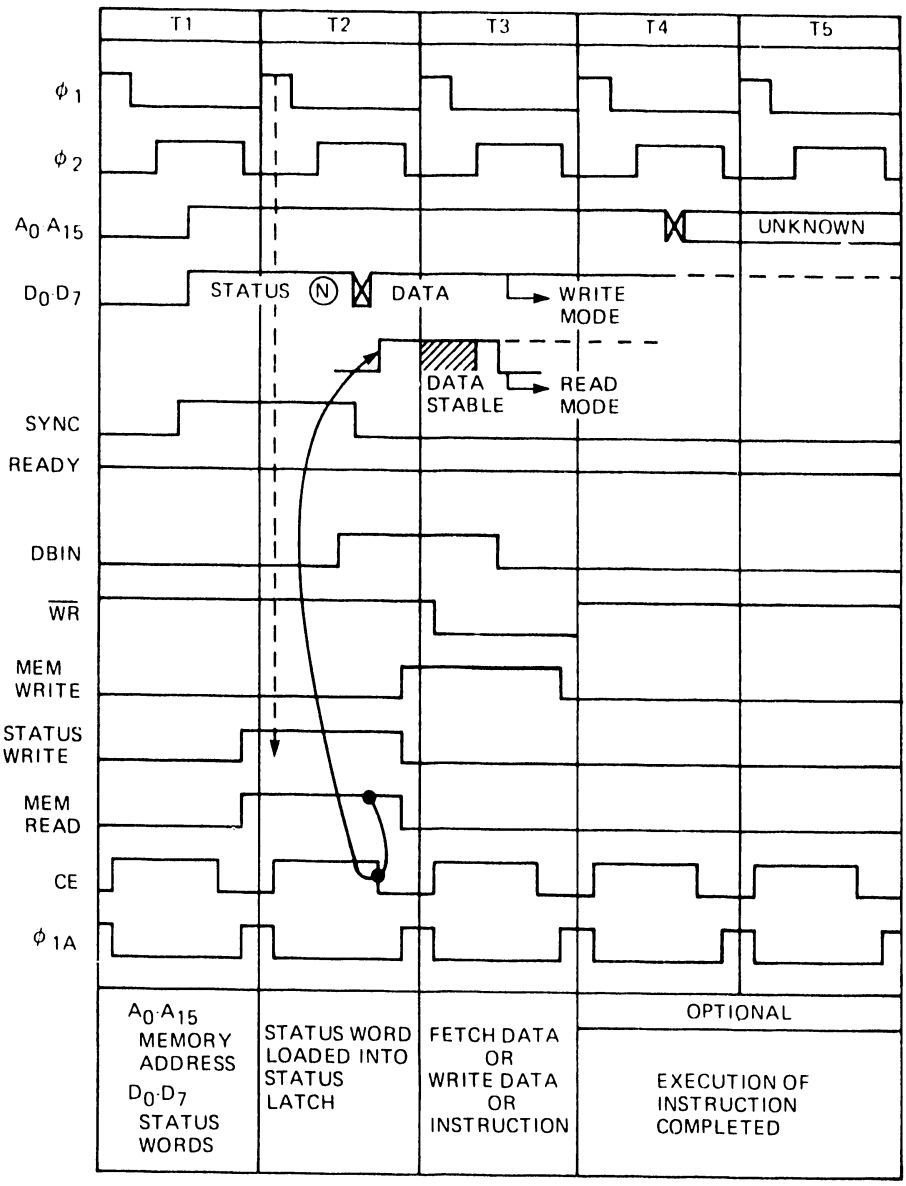


Figure 2-5A Basic 8080 Instruction Cycle

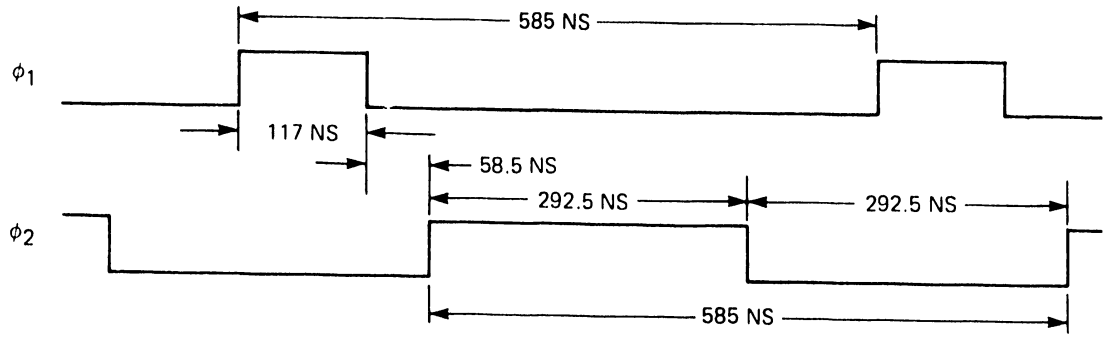


Figure 2-5B ϕ1 and ϕ2 Clock Timing

SYNC-The 8080A identifies the machine cycle in progress by issuing an eight-bit STATUS word on the data lines D0-D7 during the first state (T1) of every machine cycle. During the SYNC interval, the new status word is latched into the status register where it is held for the entire machine cycle providing control signals for external circuitry.

DBIN-This signal always occurs during the input of data to the 8080A on the bidirectional data lines after a fetch, memory read or peripheral inputs to the processor. The signal is generated by a Phase 2 clock during T2 state.

WR-The 8080A generates this signal for the synchronization of all external OUTPUT transfers. The negative leading edge of WR is referenced to the rising edge of the first PHASE 1 clock pulse following state T2.

Other clocks that are produced by Master Timing are CE, CTWT and PHASE 1A. These clocks will be described during the discussion of other areas of the Master.

2.2.3 STATUS REGISTER

The status register L4 latches status words issued from the 8080A microprocessor data bus during SYNC time and in turn uses the direct control outputs to perform the following operations:

1) MEBIN-1 Byte transfer input from slave memory to master CPU and from master memory to master CPU. *MEMR is debug input to perform 1 byte transfer.
2) *INP-Used to decode address of input port that is going to be active this MCT.
3) *M1-Provides an output that indicates the CPU is in the first MCT fetching the first byte of an instruction, i.e. Instruction Fetch.

4) *OUT-Provides a signal that indicates the output device addressed has output data on the bus when WR becomes active, i.e.: Output Port.

5) *MEMWO-Provides an output that will write or read master and slave memories. If active it will write, inactive will read.

6) *INTA-This interrupt acknowledge generated by the 8080 CPU is used to acknowledge an interrupt. INTA will gate the RST instruction onto the 8080 data bus. RST contains the variable 3 bit field which will cause the 8080 program counter to be loaded with the address of the first instruction of the interrupt service routine. This variable 3 bit field will change in accordance with the priority of the calling interrupt.

Each status word is clocked into the register when the positive transition of the clock occurs. SYNC and PHASE 2 are ANDed at L69 to load the status word. See STATUS WORD TABLE for active data bits used for each word (Table 2-1).

2.2.4 IN/OUT COMMAND DECODERS

The 8080A CPU is designed with INPUT and OUTPUT ports to permit communications with the outside world. The outside world being the associated peripherals that make up the WORD PROCESSING systems 10, 20 and 30 which include WORK STATIONS, PRINTERS and other options. The logic used for performing the output commands are BCD to DECIMAL decoders L74 and L75. See Table 2-2 for all IN/OUT commands. At the present time there are 16 OUTPUT commands which can be selected by using the 8080A address bits A0 through A3. A3 is NANDed with OUT and WR at L41 (2 gates) to the MSB (D) of the decoders. The OUTPUT instruction consists of three MCTs. The first MCT loads the FETCH (M1) status word into the status register and performs instruction FETCH. The second MCT is a memory READ. The third MCT loads the status word OUTPUT WRITE which produces signals OUT and WR which ANDed with address bit A3, synchronize the external transfer of the DEVICE identification number (Output Port).

TABLE 2-1

8080 STATUS WORDS AND DEFINITIONS

STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE
D_0	INTA	0	0	0	0	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1
D_2							
D_3							
D_4	OUT	0	0	0	0	1	0
D_5	M_1	1	0	0	0	0	1
D_6	INP	0	0	0	1	0	0
D_7	MEMR	1	1	0	0	0	0

MACHINE CYCLE NO. 1

928 ONLY

TABLE 2-2

INPUT/OUTPUT COMMANDS - MASTER CPU

COMMAND	DESCRIPTION
Trap 0	Startup
Trap 8	Parity error or data link error from the slave
Trap 16	Clock Tick
Trap 24	Debug (Debug option only)
Trap 32	Parity error on master
Out 00	Traps selected slave to 00
Out 01	Selects disk drive
Out 02	Character to line printer (Debug option only)
Out 03	Move + (Move option only)
Out 04	Move - (Move option only)
Out 05	Step head forward (floppy/seek (Hard Disk))
Out 06	Step head backward (floppy)/Restore (Hard Disk)
Out 07	Load first header byte
Out 08	Load second header byte
Out 09	Select Slave
Out 0A	Page (memory) address
Out 0B	READ
OUT 0C	WRITE
Out 0D	FORMAT
Out 0E	COMPARE (move option only)
Out 0F	Clear the coaxial channel
In 00	Input disk status
In 01	Read disk sector counter
In 02	Read program level switches
In 03	Load Head
In 04	Unload Head
In 05	Printer status (Debug only)
In 06	Keyboard (Debug only)
In 07	Input CPU status of selected slave
In 08	READ 256 Bytes (move option only)
In 09	WRITE 256 Bytes (move option only)

The IN COMMAND DECODER logic consists of one BCD to DECIMAL decoder L76. There are six IN commands I0-I4 and I7 requiring address bits A0, A1 and A2. See Table 2-2 for identifying IN commands. The MSB (D) input at L76 inhibits any IN commands by remaining high except during an IN instruction. The output pin 6 of OR gate L39 is active low when doing an IN instruction permitting only the three low order address bits to select the IN read device. Most of the IN/OUT commands will be covered in the following discussions.

2.2.5 TRI-STATE DATA BUFFER

The 8080A data bus buffers are bidirectional consisting of four high speed HEX TRI-STATE INVERTERS. L59 and L60 are the input buffers enabled by*DBIN. L58 and L61 are output buffers enabled with W0 and not *SYNC. The buffers are in a high Z state when disabled which permit DIRECT MEMORY ACCESS (DMA) to be performed while the 8080A is forced into a WAIT (busy) state. In essence, the data bus is disconnected from the processor. The unidirectional non-inverting 8080A address buffers L46, L47 and L48 are enabled at all times allowing the address lines to remain active during DMA sequences. DMA operations are performed on a cycle stealing basis and access to Master memory is arbitrated on the Master memory board. The address buffers are non-inverting.

2.2.6 PROGRAM LEVEL SWITCHES (Finger operated)

A set of finger switches are mounted on the 7202 Master CPU board and labeled SW #1. They are set to specific positions for decoding the correct software that is to be used on WANG WP Systems 10, 10A, 20 and 30. The PROGRAM PROTECT STATUS circuitry consists of the switch and two HEX TRI-STATE buffers L35 and L36. The outputs of the buffers are connected to the 8080A bidirectional DATA bus. The code setting of these switches, when compared with the software code, determines whether the initial code setting from the buffers is correct. If not, the machine will hang and no processing will be done. A number (2) will appear on the CRT screen indicating that the code setting is incorrect. An IN02 (I2) is used to READ the code.

Signal SW 8 at pin X1 is connected to a toggle switch located inside the front panel of the MASTER CPU of every WP system 30. This Utility Load Transfer Switch (ULTS) when closed (Down-0 volts) selects the SYSTEM HARD DISK operation used with SYSTEM 30.

2.2.7 CHANNEL SELECT

Presently, the maximum number of channels available on any WP System is fourteen. The channel select circuitry will only furnish sixteen using the binary combinations furnished by four DATA BUS bits D0M-D3M. The Master is selected by*SLT0. The selection of any channel is done with OUT instruction (09). *SLT0 is routed to the MASTER MEMORY 7201 board for determining priority of functions. SLT1, 2, 4 and 8 are wired to the DATA LINK 7214 board for selecting the desired channel to the slave peripheral.

2.2.8 PRIORITY INTERRUPT DECODER

The 8080A has a built-in capacity to handle external interrupt requests. The priority interrupt circuitry allows the external devices as well as the MASTER to interrupt the current program for any of the below listed reasons. The interrupt (INT) 8080A input is asynchronous therefore a request can originate at any time during any MCT. Internal circuitry will reclock the request to correspond to the internal clock. The Master currently supports five interrupts. If more than one interrupt occurs at the same time, the order of priority is as listed below.

1) RESET-TRAP 0-Used for startup.
2) TRAP 8-Parity error when master reads slave memory with bad parity, or an error in coaxial transmission occurred (DLER).
3) TRAP 16-Clock tick (TCCLK).
4) TRAP 24-Debug (Involves the use of a software DEBUG monitor).
5) TRAP 32-Parity error when master reads its own memory with bad parity (ME).

The priority interrupt decoder uses two dual D-type edge-triggered F/Fs, L37 and L49 for latching TRAPS 8, 16, 24 and 32. If a TRAP 8 (DLER) was to occur, the following events would take place. Pin 5 of L37 goes high making pin 5 of L13 high. This quadruple D-type edge-triggered F/F latches the interrupt when clocked by AND gate L69. Inactive status word INTA (high) is ANDed with the trailing positive going edge of PHASE 2 gating the interrupt bit into an 8-line to 3-line decoder L14 making output pin 9 high (code 100).

L14-14 goes low inverted by L7 and applied to the 8080A interrupt (INT). This input sets the 8080A INTE F/F internally initializing the interrupt routine which cannot start until the current instruction is completed. The INTERRUPT machine cycle which follows the enabled interrupt request consists of three MCTs. The 8080A issues the status word INTA (INTERRUPT ACKNOWLEDGE) which is inverted and NANDed with DBIN gating a coded RESTART (RST) 8 bit byte onto the 8080A data lines from buffers L1 and L2. The RESTART (RST) is a single byte instruction and the interrupt codes are buried in data line bits D3m, D4m and D5m. The interrupt timing sequence Machine Cycle Times 2 and 3 are used to store the PROGRAM COUNTER into two locations designated by the STACK POINTER. The RST instruction byte sent to the 8080 will be decoded into the trap addresses. Each of these call codes is multiplied by a factor of 8 thus producing the addresses presently used in the TRAP table above. The code presented to the data bus is also presented to a BCD to DECIMAL decoder L24 which generates the CLEAR signal for the interrupt latch, in this case CL1. A BCD to DECIMAL decoder L24 output will reset the latch that contained the interrupt.

2.2.9 TCCLK-(10 ms timer-CLOCK TICK)

All TRAPS are self explanatory with the exception of TCCLK. This 10 ms timer interrupt circuitry is used for disk (Floppy/Hard) processing. Due to the nature of the disk drives (slower access and write time) and the associated controller, all disk processing occurs

during TCCLK interrupts. The clock tick circuit consists of four synchronous 4-bit counters L9, L10, L11 and L12 arranged to count down PHASE 1 clocks generating a clock (C4) that occurs every 19 us and a tick clock (TCCLK) that is generated every 10 ms.

2.2.10 REFRESH TIMING-(C4 clock)

Clock C4 is the gating signal for REFRESH. Master memory consists of TMS 4050 high speed dynamic Random Access Memory (RAM) chips. A precharge (refresh) of the cell matrix is required approximately every 2 ms or less. By addressing any row, all 64 bits in that row are refreshed. A period of every 19 us has been selected as the clock refresh time. The refresh clock is applied to row addresses A0-A5 in 64 counts which takes a period of approximately 1.2 ms with no time sharing.

A presettable binary counter latch L64 is cleared at TURN ON time. A count of four REF signals are required to set L64-2 high. This provides burst refreshing after a high speed memory move. C4 clocks occur every 19 us, therefore permitting the machine cycle (M1) output to enable L33 F/F to be clocked during each instruction by DBIN. Every DBIN clock produces a REF clock which is fed back to gate L39-10. *REF clears L53 for the next C4 clock. Prior to the four count of the L64 counter the refresh clocks occur at a high rate, but settles down to a refresh occurring at the desired rate of every 19 us.

2.2.11 DMA, 1-BYTE, 256-BYTE CONTROL LOGIC

The organization of all memory in the 928 system is central to the MASTER CPU even though it is multiport in nature. The memory is organized into a number of banks each supported by an 8080A microprocessor. Each 8080A can access its own memory by means of 16-bit addressing. The MASTER, however, can address all banks of memory via the processor communication channel using 24 bits of addressing (8

bits of which are used to select the bank). The master, in addition to being able to directly READ and WRITE from or to slave memory, can also command the disk to READ or WRITE from or to a selected bank of memory.

The control logic required for data transfers utilizing the processor communication channel (DMA) is designed to prevent other functions from taking place while DMA transfers are in progress. Data can only be transferred in single (1-byte) or 256 bytes of data (BLOCK OF DATA). A block of data represents the maximum data that can be transferred in one DMA priority period.

A 1-byte READ/WRITE is the method used to address slaves (OUT commands), check status of slaves and retrieve semaphore requests using (IN) commands. A precise protocol is used for all data transfers. The STATUS of each slave must be certified before addressing the desired data. The protocol requires a header byte be sent to each slave prior to any type data transfer. The header byte serves the purpose of identifying the operation when decoded in the slave as well as certifying the operation of the data link. The STATUS byte is then read into the 8080A for checking before any data is transferred. The STATUS byte is retrieved from the SLAVE as follows:

2.2.11.1 STATUS

STATUS F/F is set with INP and ADDRESS 7 at gate L21 with clock*PHASE 2 SYNC. L43 output pins 8 and 9 are signals *STATUS and *INST which control the loading of a header byte into the data buffer of the DATA LINK board and clock the STATUS byte from the slave onto the 8080A data bus. Signal *STATUS is low gating a high output from gate L54-11. The positive transition clocks the STATUS/1-BYTE F/F L33 setting the Q output low and forcing the 8080A into a wait state. *INST initiates the transfer of the STATUS byte from the slave into the master data link and*SEMST is true when DBIN is clocked. Signal OPCOM from the data link indicates that the STATUS byte transfer is complete.

When OPCOM is true, the J-K F/F L79-12 is set, driving L27-3 high. This allows L65 to count from a deficit value to full count with a CARRY OUT (CO) which is used to delay the clearing of the operation until it is completed. J-K F/F L79 is set by the CO bit and*PHASE 2 clock generating*OP which clears L79 and*STATUS/1BT latch at L33-13. The Q side of L79 is used to clock L28 with PHASE 2. L28-9 ANDed with PHASE 1 gates a low from L6-6 and a low from L27-6 (OPC) clearing the STATUS latch L43.

2.2.11.2 RESTART

A RESTART instruction is initiated by an interrupt and in this case it is a data link error. The 8080A issues an OUT 0 which clocks L32 F/F RSTRT. A header byte issued by the 8080A follows the RSTRT signal to the data link board clearing the error. This procedure will be repeated several times if required. If the error cannot be cleared, the system will lock up until the error is repaired. OPCOM is used to clear RSTRT and the procedure is the same as above.

2.2.11.3 1-BYTE READ

A 1-BYTE READ is processed by the 8080A issuing an OUT 9 with a data byte address for the channel selected. Any slave channel selected forces signal SLTO to go high. SLTO is ANDed with address bit A15 at gate L52 enabling F/F L43 to be set with clock*PHASE 2 SYNC. The outputs of L43 are signals*1-BYTE at L43-6 and*1-BYTR at the output of L66-6. *1-BYTR is routed to the DATA LINK board for starting the 1-byte read. *1-BYTE gates the high and low order address bits onto the DMA address bus. *1-BYTE also gates the output of L54-11 high enabling*SEMST for signal DBIN which gates the single byte of data on to the 8080A data bus. OPCOM goes low sfter the read is completed. The 1-BYTR at L43-5 is ANDed with MEBIN to produce a deficit count of 7 us in L65 before the 1-BYTE operation is terminated.

2.2.11.4 1-BYTE WRITE

A 1-BYTE WRITE is similar to a read. *OUT9 clocks the selected addressed channel out of L17 register and the 1-BYTE F/F L43 is clocked set by*PHASE 2 SYNC. *1-BYTR is inverted by L72 and connected to L52-12. *1-BYTE enables the slave high order address on to the DMA bus and 1-BYTR ANDed with MEMWO gates a high input to L38-11 producing an active*SMWT. *SMWT starts the DATA LINK operation of writing the address and data to the addressed slave. Once the data byte is written the data link sends*OPCOM terminating the 1-BYTE write operation.

2.2.11.5 256-BYTE READ

A 256-BYTE READ is similar to the 256-BYTE WRITE, however, the procedure of performing a READ vs a WRITE must be clarified. A disk Read operation requires the Master to select the type disk (FLOPPY or HARD) that the data will be READ from and the selection of the channel to which the data will be transferred performing a WRITE sequence. The reverse will be true for disk Write which requires a read of the slave memory and the transfer of data to the disk for writing. When a channel is selected for a R/W, SLTO is inactive (HIGH) which enables both D-type F/Fs L53 and L62 to be set by either OUT B or OUT C. Upon receipt of an OUT B, a read of 256 bytes from the selected disk to the appropriate bank and page of the selected channel will commence. OUT B clock sets L62-9 high (DRD) enabling*SMWT. L62-8 is set low (DRD) enabling the clock that sets L53-9 high gating L52-8 high (256 BYTR). These two signals*SMWT and 256 BYTR initiate the write sequence for the 256 byte transfer to the data link. L63 is used as an OR gate for OUT B and OUT C to generate a clear pulse OB/C for the DMA low order address counter mounted on the memory board. This occurs prior to every 256 byte transfer. At this state of the transfer the data is stored in an intermediate storage area called FIFO located on the data link board. The final transfer will be discussed in DATA LINK as well as the method used to store the data in FIFO.

2.2.11.6 256-BYTE WRITE

The 256-BYTE WRITE commences after the channel select has been completed. SLTO enables L53 F/F which is set when OUT C is issued. L53-9 enables signal 256 BYTR and SMWT is inactive. A 256 byte READ of the selected slave memory commences and data is transferred from the slave to the FIFO storage area on the data link board. The 256 bytes are then transferred from FIFO and written on the disk by FIFO CONTROL and signals from the disk controller which in turn is controlled by the master.

2.2.12 DMA ADDRESS BUS AND PAGE ADDRESS COUNTER

The PAGE ADDRESS COUNTER consists of two synchronous 4-bit counters L15 and L16 used to count pages (PAGE=256 bytes). The page counter will increment after each 256 byte transfer. The page count is multiplexed with the high order address bits from the 8080A to allow 1-byte and 256-byte transfers to be executed using signal 1-BYTE control. 1-BYTE will be true for 1-byte transfers. The incrementing page signal PGINC will occur prior to each 256 byte transfer (1) when 256 BYTR is selected or (2) when the master has been selected for multiple reads from the disk. *SLTO NORed with*INIDF enable signal 256 BYTR to produce a*PGINC (Page Increment) after each 256 byte transfer.

2.2.13 PARITY GENERATOR AND PARITY CHECK CIRCUIT

Parity generator L3 generates a parity bit D8pout for each data byte issued from the 8080A and stored in memory. The parity bit is stored in memory with the byte. Conversely each data byte read from memory going to the 8080A via the data bus has its parity bit D8Pin checked. D8Pin is generated on the memory board and wired to the Master CPU at L5-9. L5 is an exclusive OR gate having signal DP8out connected to L5-10. Either of these two inputs indicate a parity error, setting up a memory error (ME) condition by enabling the input to L30-12. The signal for clocking F/F L30 comes from L29-6. This 4-input NAND gate requires the following inputs:

1) MEBIN active.
2) PROM not active.
3) TB not active.
4) READY F/F L68-9 set to enable L69-9 which ANDed with PHASE 1 GATES the output of L69-6 low for the period of PHASE 1. The trailing edge of PHASE 1 sets the L30 F/F which sets the (ME) F/F L49 in the PRIORITY INTERRUPT DECODER. The TB F/F L30-6 is used to inhibit the clock for setting the (ME) F/F during 1-BYTE transfers. The parity checks for 1-BYTE transfers are processed in the DATA LINK.

2.2.14 RESET AND READY/BUSY

Reset (RESM) and R/B are inputs to the 8080A microprocessor and are used for the following reasons:

RESET-An external RESET signal of three clock period duration or more will restore the internal program counter to address 0000HEX thereby commencing program execution at its starting point. A reset of the operating registers and a prior operation are also cleared by a Reset Machine signal (RESM) and RSOP. The initiating three reset inputs are applied to NAND gate L8. Input RESET is a microswitch located inside the front grill of the Master CPU. AUTO-RESET signal is generated in the power supply board 7206 during startup. RES is an input from the DEBUG unit.

READY/BUSY-All memory cycle times require at least three clock times T1, T2, and T3. If the 8080A processor has to wait for the data being accessed from memory than a WAIT state is added to the MCT. The memory board 7201 generates a RDMY signal causing a longer access time hence when the RDMY goes low the READY input to the 8080A goes low freezing the processing of the instruction for one or more WAIT states until memory releases the wait response. L40 is a three input AND gate and RDMY is the only active input other than the DEBUG (TWR). MOVOPT is a potential future option.

2.2.15 A & B CLOCK GENERATOR FOR DISK

The A & B clock generator for the Floppy and Hard disk is designed for disk Write and Read operations. The 10 mhz crystal is used for both disks, however, the logic is arranged to provide two sets of clocks. The frequency of the clocks for the hard disk occur 10 times faster than the clocks for the floppy, however, the phase relationship for the A and B clocks for each disk remain the same. These clocks illustrated on Figure 2-6 are used for controller bit time and clock time and represent the timing of internal controller functions. The generator is controlled by two signals provided by the disk controller board 7203 namely*FDS (Floppy Disk Select) and*RSAC (Resync Allow Clock).

2.2.15.1 A & B Clocks for Floppy

The Floppy Disk Select*(FDS) signal from the controller board 7203 is true (low) when the floppy is to be used. D-type F/F L62 toggles for each 10 mhz clock (divide by 2) while L51 F/F remains reset having been cleared by*RSAC. The output of NOR gate L38-10 clocks the synchronous 4-bit counter L50 that was previously loaded with a deficit count of 10. Each clock has a width of 200 ns and occurs at a 500 KHZ rate hence the time required to fill the counter and produce a Carry Out is 2 us. Each CO alternately produces an A clock and a B clock and reloads the counter with a count of 6 after each clock. *RSAC is the clearing signal for the A & B clock generator and also inhibits its operation.

2.2.15.2 A & B Clocks for the Hard Disk

The Hard disk is selected by*FDS signal being high. *FDS enables the L51 F/F to be set when the L50 counter is initially filled after the*RSAC signal is released. The CO signal is inverted by L72 reloading the counter and clocking the L51 F/F set. Setting L51 provides a D input to the counter and logically conditions the output

of NOR gate L38-10 to clock the counter with 100 ns clocks generated by the 10 mhz crystal oscillator. After each CO the counter will be loaded with a deficit count of 2 which will produce alternate A & B clocks at the times shown in Figure 2-6.

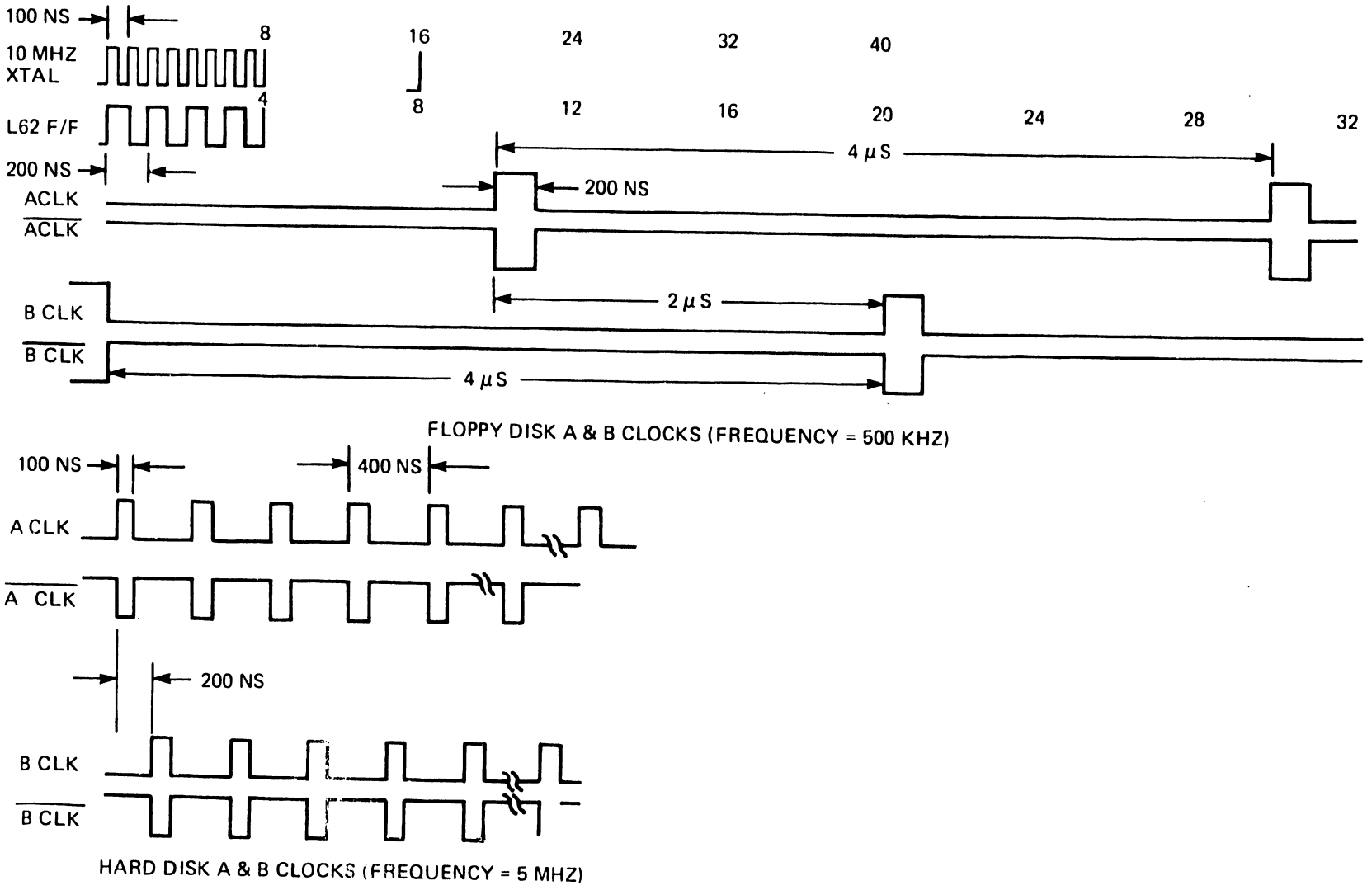


Figure 2-6 A & B Clock Generator-Timing Diagram

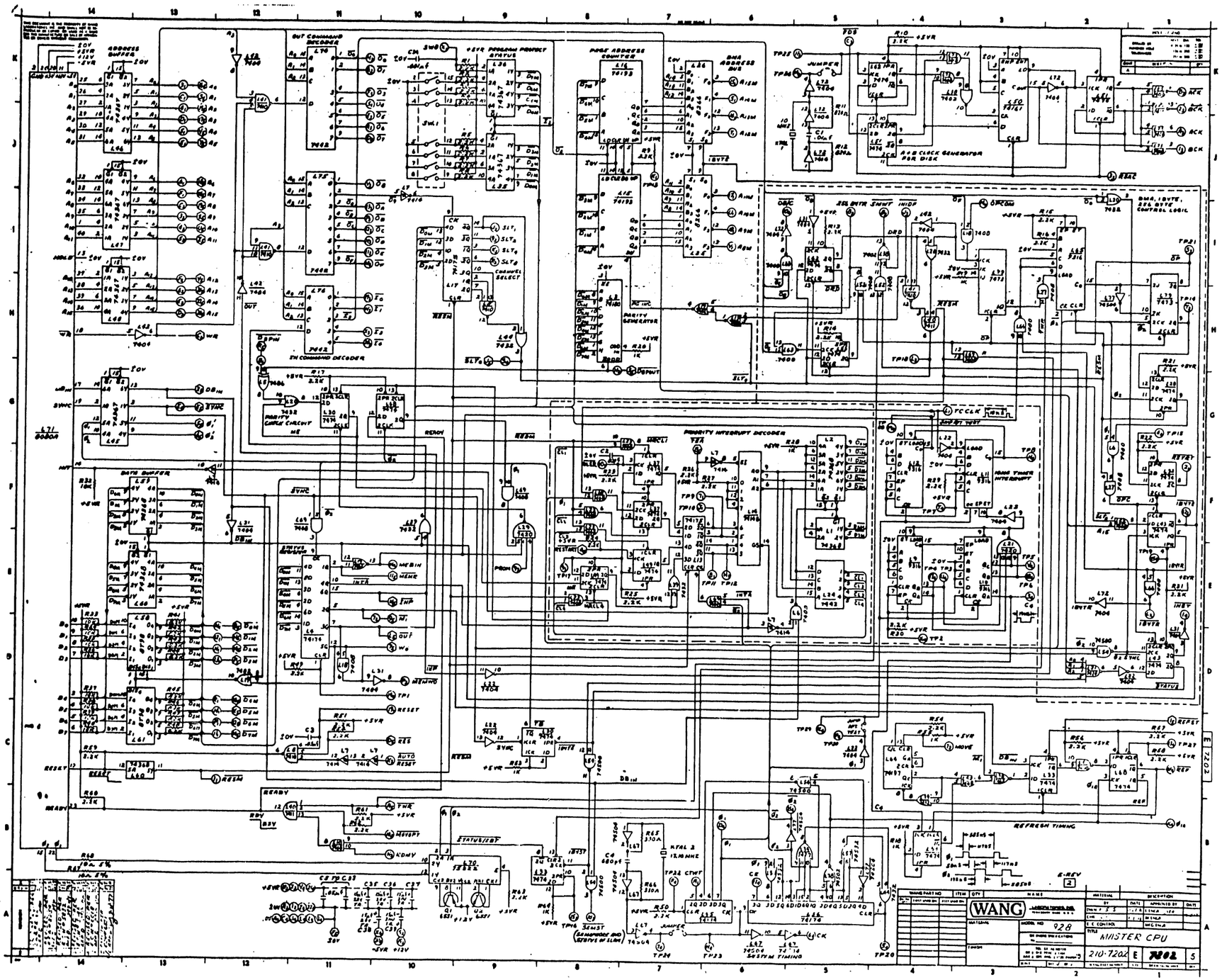
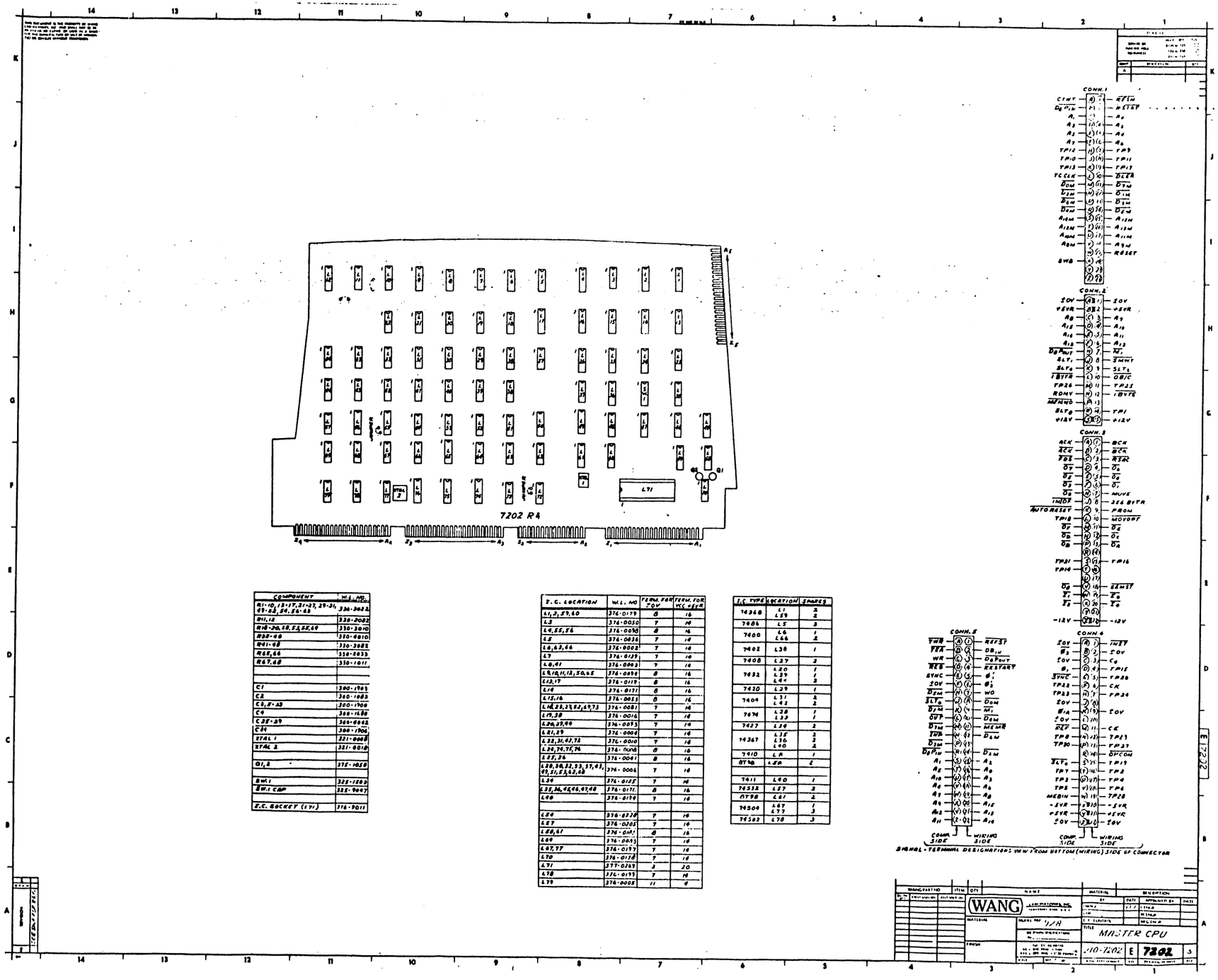


Figure 2-7 Master CPU-Schematic Illustration — Sheet 1



COMPONENT	W.L. NO.
R1-10, 13-17, 21-23, 29-31, 49-52, 54, 56-58	330-3682
R11, 12	330-2002
R18-20, 18, 53, 55, 59	330-3010
R52-48	330-6810
R41-48	330-3882
R65, 66	330-3833
R67, 68	330-1011
C1	300-1903
C2	300-1883
C3, 5-33	300-1900
C4	300-1438
C 35-39	300-6902
C34	300-1904
XTAL 1	331-9008
XTAL 2	331-9010
Q1, 2	375-1058
SW.1	325-1503
SW.1 CAP	325-9007
I.C. SOCKET (L71)	376-9011

I.C. LOCATION	W.L. NO.	TERM. FOR +5V	TERM. FOR VCC +5V+R
L1,2,59,60	376-0179	8	16
L3	376-0050	7	14
L4,55,56	376-0098	8	16
L5	376-0038	7	14
L6,63,66	376-0002	7	14
L7	376-0139	7	14
L8,61	376-0003	7	14
L9,10,11,12,50,65	376-0096	8	16
L13,17	376-0119	8	16
L14	376-0171	8	16
L15,16	376-0083	8	16
L18,23,33,62,69,73	376-0081	7	14
L19,30	376-0016	7	14
L20,29,49	376-0073	7	14
L21,27	376-0004	7	14
L22,34,42,72	376-0010	7	14
L24,74,75,76	376-0048	8	16
L25,26	376-0041	8	16
L28,36,37,38,39,43,44,45,47,48,68,71,77,78	376-0064	7	14
L31	376-0135	7	14
L32,34,45,46,47,48	376-0171	8	16
L40	376-0134	7	14
L50	376-0230	7	14
L57	376-0105	7	14
L58,61	376-0141	8	16
L64	376-0043	7	14
L67,77	376-0177	7	14
L70	376-0138	7	14
L71	377-0269	2	20
L78	376-0193	7	14
L79	376-0005	11	4

I.C. TYPE	LOCATION	SHARES
74368	L1 L59	2 2
7485	L5	3
7400	L6 L46	1 2
7402	L38	1
7408	L27	2
7432	L20 L39 L41	1 1 3
7420	L29	1
7404	L31 L43	2 2
7474	L28 L33	1 1
7427	L26	3
74367	L35 L36 L40	3 2 2
7410	L8	1
8T98	L66	2
7411	L60	1
74S32	L37	2
8T98	L61	2
74S04	L67 L77	1 3
74S03	L70	3

Figure 2-7 Master CPU-Schematic Illustration — Sheet 2

2.3 MASTER DISK CONTROLLER - 7203

2.3.1 GENERAL DESCRIPTION (Figures 2-8 and 2-9)

The Disk Controller board 7203 is the interface between the Word Processing Master Central Processing Unit (MCPU) and two disk drives. The WANG word processing system WPS 20 has two floppy disk drives and the WPS 30 is equipped with one floppy and one hard disk drive. The hard disk is commonly referred to as the Fixed/Removable disk. Both floppy and hard disk drive types are controlled by a series of input and output commands issued by the MCPU which permits the selected system disk to transfer data to and from any selected bank of memory via the processor communication channel (DMA). The commands for both floppy and hard disk drives are general enough to permit incorporation into a single system. The characteristic details of the disk drives are available in WANG published documents (Refer to APPENDIX C); therefore only the logical descriptions of circuitry and signals on the disk controller board will be found in this document.

The two primary operating functions, controlled by the disk controller and performed by the drives, are the "READ" and "WRITE" commands (OUT 0B and OUT 0C) respectively (Figure 2-9). These commands result in data being read from the disk and transferred to a memory bank or a write to the disk of data transferred from a memory bank. The data is transferred in 256 byte quantities, at one byte intervals. The 928 memory is multiport, therefore the selection of any memory (Master or Slave) is accessible for disk READ/WRITE transfers.

The time required to internally transfer data is strictly a factor of the type of disk drive selected. The Hard disk can read and write data at 10 times the rate of the floppy drive. This situation requires that the disk controller must also be capable of processing the data at the higher rate. The A and B clock generator is designed to operate at these two rates; generating clocks that will fill the requirements. See MCPU for details on the A and B clock generator. Refer to paragraph 2.2.15.

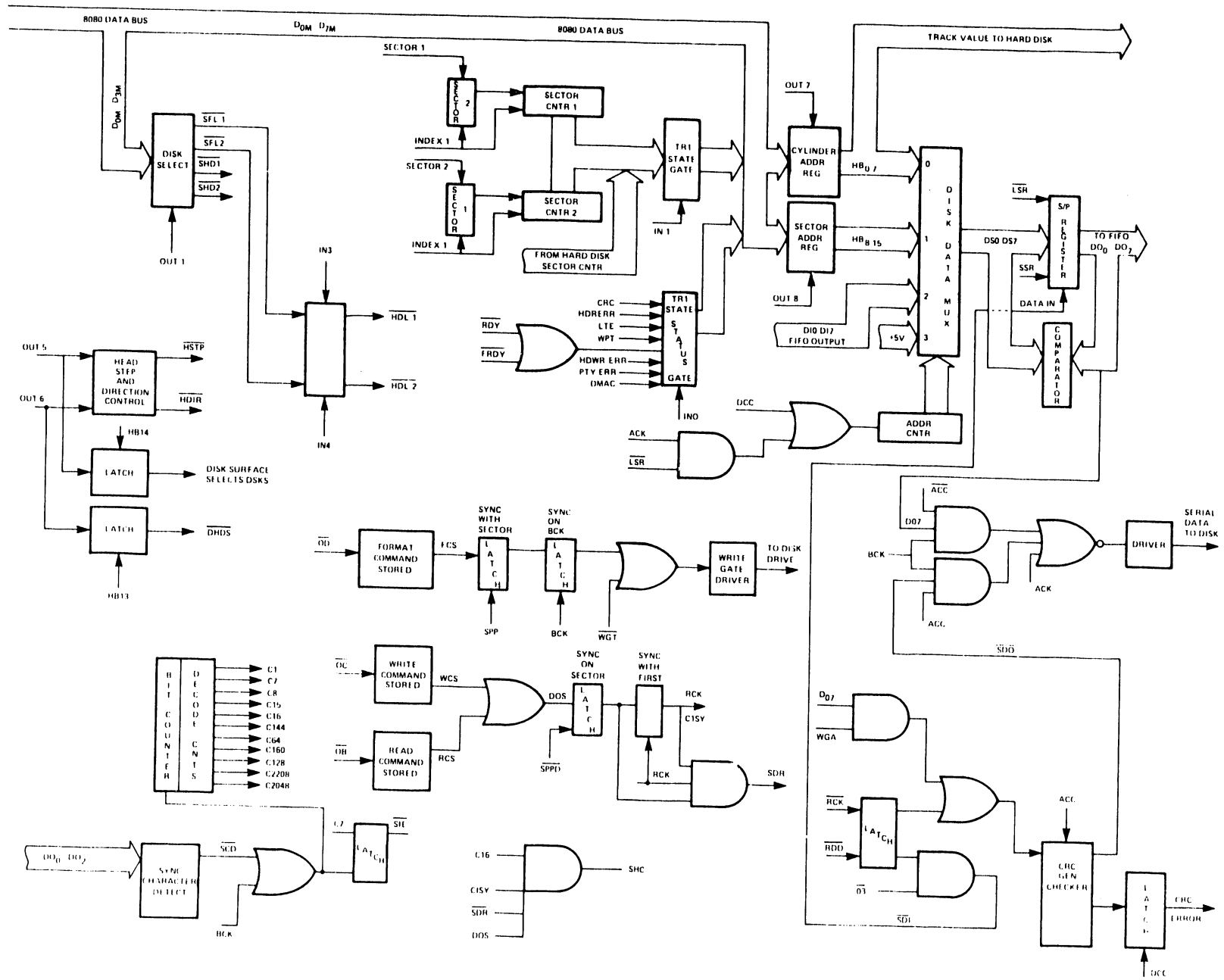


Figure 2-8 Master Disk Controller-Block Diagram

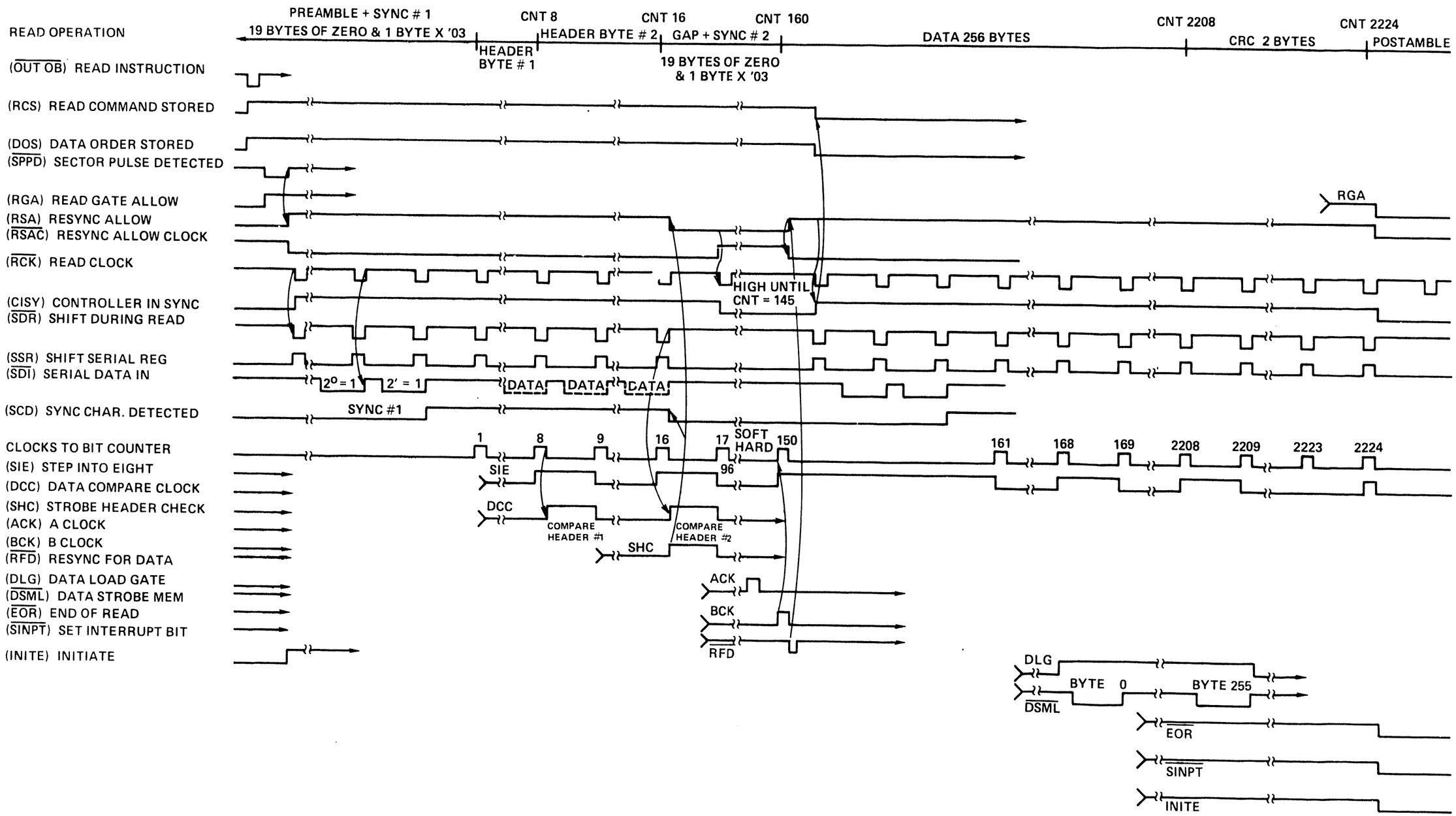


Figure 2-9 Master Disk Controller-Timing Diagrams Read-Sheet 1

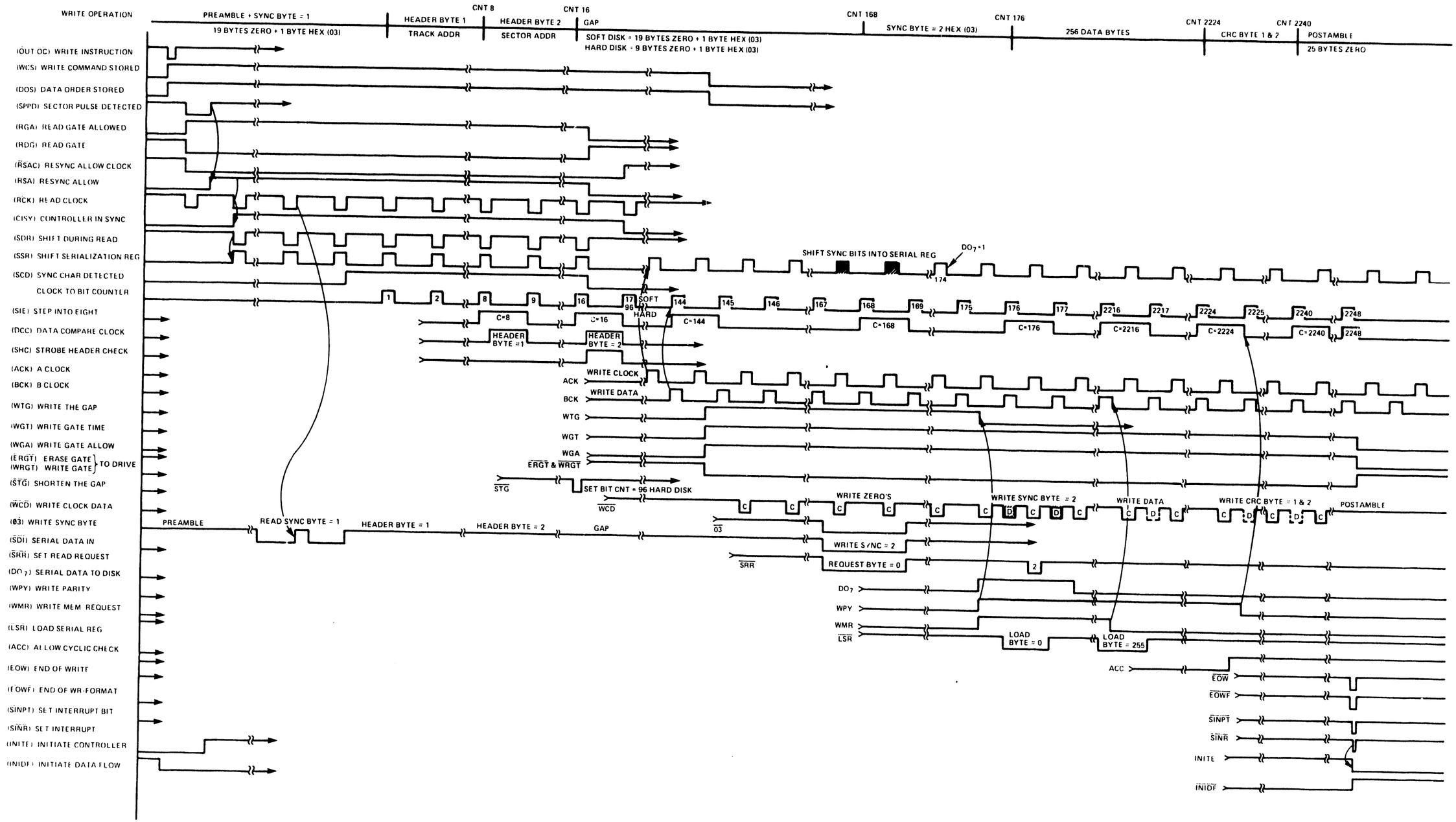
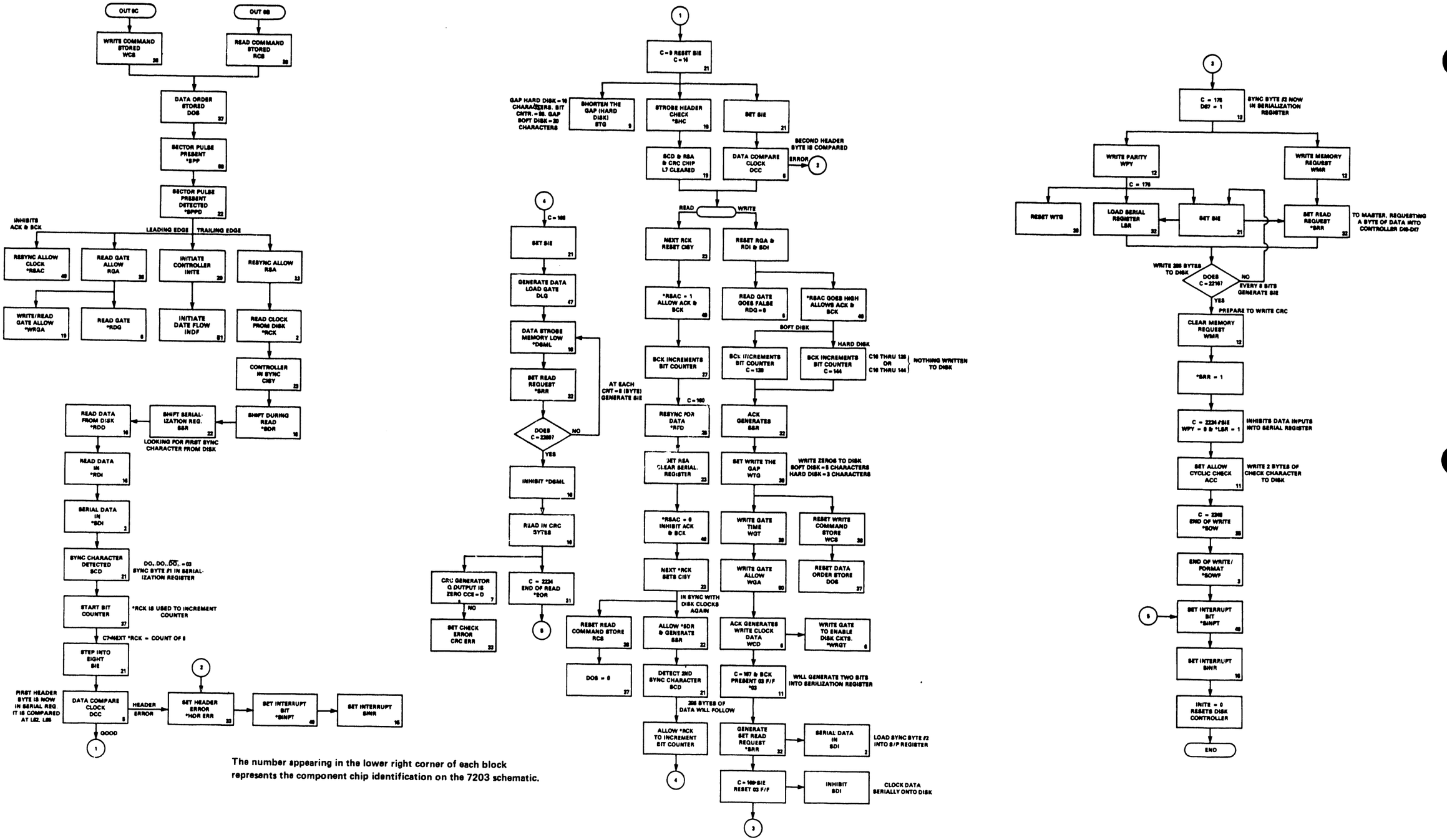


Figure 2-9 Master Disk Controller-Timing Diagrams Write-Sheet 2



The number appearing in the lower right corner of each block represents the component chip identification on the 7203 schematic.

Figure 2-10 Master Disk Controller-Flow Chart (Read/Write Operations)

The disk controller board generates output signals that are routed to the MCPU and the Master Data Link (MDL). These signals initiate and provide the control for processing data required by the two types of disk drives. Controller output signals are also routed to the disk drives for control purposes.

A third operation performed by the Master Disk controller is the formatting of the floppy and hard disk surfaces. The FORMAT operation will be discussed in some detail with an accompanying event chart. Refer to Paragraph 2.3.7 and Figure 2-13.

Because of the similarities in controlling the floppy and hard disk drives a description of each sequential operation for each type of drive will be discussed. Prior to the selection/generation of the major commands listed below, a series of selections and identifications must be processed between the DISK, MCPU and Master Memory through the logic of the Master Disk Control board.

THREE MAJOR COMMANDS

1. O_B Command -- READ
2. O_C Command -- WRITE
3. O_D Command -- FORMAT

2.3.2 DISK SELECT

2.3.2.1 FLOPPY

The MCPU selects either floppy disk drive #1 or #2 by issuing a 1 or 2 code on data bus lines*D0m-D3m. SEE CHART BELOW. The 4-bit cod is then clocked into a D-type F/F register L59 by an OUT 01 command from the 8080.

SELECT CODES FOR FLOPPY AND HARD DISKS

	D0m	D1m	D2m	D3m	CODE #
FLOPPY #1	0	1	1	1	= 1
FLOPPY #2	1	0	1	1	= 2
HARD DISK #1	1	1	0	1	= 4
HARD DISK #2*	1	1	1	0	= 8
NOTE:*Hard Disk #2 not presently used.					

The floppy disk has 77 tracks and each track is divided into 32 sector marks of equal length. Only one side of the floppy disk is usable. The present specifications require a sector to store 256 bytes of data and it was therefore necessary to use two sectors for storing the 256 bytes. Doubling up the sectors has reduced the number to 16 identifiable sectors per track. With the disk rotating at 360 RPM a means of selecting the TRACK and SECTOR for commencing a read or write is accomplished by the MCPU performing the following operations:

1. LOAD THE HEAD - An output from L59-2*(SLF1) will select floppy 1 which when ORed with an IN 3 command will preset L53 causing*HLD1 (Head Load 1) to go active. The same procedure holds true for floppy 2 gating*HDL2.

2. STEP R/W HEAD TO TRACK - Positioning the R/W head requires a Head Direction*(HDIR) signal and a Head Step*(HSTP) pulse. An*OUT5 command from the MCPU will preset F/F L53 and generate a low at L56-3 triggering the one-shot MV L54 causing the head to step one track in the forward direction. An *OUT6 command will clear the L53 F/F changing direction and causing the head to step one track in a backward direction. These timed actions are under processor program control.

3. SECTOR COUNTERS - The floppy 1 and 2 sector counters are identical and only sector counter 1 will be discussed. The*INDEX 1 signal from the floppy disk is generated when the punched index hole on the disk is detected at the start of the sector count causing L84 (section 2) to preset. SECTOR 1 signals toggle the L84 F/F for each punched sector hole detected on the floppy disk

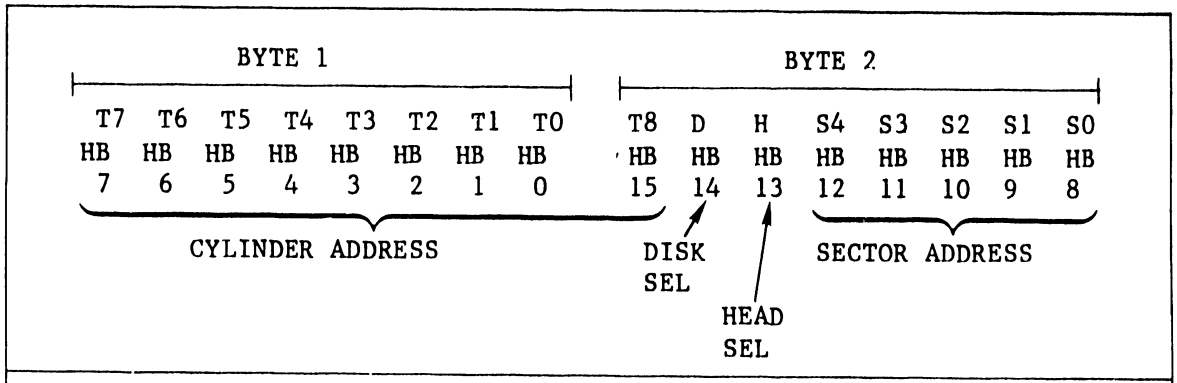
(Total 32) enabling a total output of 16 sector counts. These counts are stored in a 4-bit binary counter and presented to tri-state buffers L71 and L73 via the output of NAND gates L68 and L69 when enabled by (Select Floppy 1) SLF1. An*IN01 command from the 8080 is used to monitor the sector count until it is one count from the intended read sector before issuing a READ or WRITE command. During the sector count period each count*SPP is routed to the 8080 data bus buffer input at L73-10 via NAND gate output L68-11. This Sector Pulse Present*(SPP) pulce indicates that the sector counter is operating. Further discussions of disk operations will clarify the uses for the*SPP pulses that are applicable to both disk types.

2.3.2.2 FIXED/REMOVABLE (HARD)

The hard disk (Fixed/Removable) has a permanently mounted disk (platter) and a removable disk (platter). Each platter has two sides that are used for storing data; therefore a total of four surfaces. Each of these surfaces has 408 tracks (cylinders) and each track has 24 sectors. Each sector will store 256 bytes of data. The storage capacity of these four surfaces exceeds 10,000,000 bytes of data.

The selection of the FIXED or REMOVABLE platter of the hard disk, the surface of the selected platter (top or bottom), track (cylinder address) and sector addresses of the selected surface are all included in two HEADER bytes that are issued by the Master CPU. These two header bytes are delivered to the disk controller with*OUT7 and*OUT8 commands. Table 2-3 describes the 16 bits used in the header bytes.

TABLE 2-3
HEADER BYTES



HB0-HB7(T7 to T0)= Low 8 order bits of cylinder address
HB8(T8)= High order bit of cylinder address
HB14--D = DISK = 0 ---Fixed disk
D = DISK = 1---Removable disk
HB13 H = 0---Bottom head
H = 1---Top head
HB8-HB12--(S4 to S0)= Sector address

The selection of hard disk #1 starts when the MCPU issues the select code shown above. Refer to paragraph 2.3.2.1. *OUT1 from the 8080 clocks the code into F/F register L59. The HEADER bytes 1 and 2 are loaded into the cylinder and sector address registers namely L60, L75, L61 and L76. Nine bits of cylinder (TRACK) address are routed to the hard disk via NAND gates L86, L85 and the ninth bit via L44. These nine bits*(HDT0-HDT8) are required for addressing 408 tracks on each disk surface.

The output from L59 causes the output from OR gate L52-11 to go high removing the preset from F/Fs L57. With header byte bits*HB13 and*HB14 from the sector address register at the D input of both L57 F/Fs, an*OUT5 command from the 8080 will clock the F/Fs to the specified state. This selects the fixed or removable disk*(DSKS)and the top or bottom surface*(DHDS) of the selec ed disk. Refer to the header byte chart above.

Outputs from the disk select register L59 to L68 NAND gates are not currently used. *SHDI and*SHD2 are hard disk select signals to be used for a future chaining configuration for additional disk storage.

If the hard disk is selected the output at AND gate L56-11 gates signal*FDS high. *FDS is routed to the A and B clock generator on the MCPU which causes the generator to produce higher frequency A and B clocks for use in the disk controller. The inverted FDS signal goes to the D inputs of F/Fs L42. An*OUT5 will clock the L42 (1) F/F reset generating*HDST (Head Step).

HDST*drives an internal disk servo system and the R/W head to the track specified by the 9-bit cylinder address. The address was previously sent to the disk internal address register to control head movement. *HDST will be held active until an Address Acknowledge Clock (*AAC) is sent from the disk presetting the L42 F/Fs. *AAC indicates that the head is positioned at the specified cylinder (TRACK). An*OUT6 command is used to reset the L42 (2) F/F producing a*RSTR (RESTORE) signal that will cause the cylinder servo to drive the R/W head to track zero. This command is issued prior to the 8080 retrying a failed operation.

2.3.3 SECTOR ADDRESS - HARD

The sector seek for the hard disk R/W commands is performed by reading the sector count direct from the disk hardware. Five sector bits*(S1-S5) and a*SPPH (SECTOR PULSE PRESENT HARD) signal are used to monitor the presence of sector pulses and the actual sector number. One sector count prior to the specified sector will initiate the R/W command to commence the selected operation. The value of the hardware sector count register (driven by the detection of notches cut into the metal hub of the disk) is delivered to the low five order bits (D0m-D4m)*of the 8080 accumulator from TRI-STATE buffers L71 and L73. IN01*(I1) command is used by the 8080 to monitor the sector count.

2.3.4 INPUT STATUS

The input status of the selected disk to the 8080 accumulator is checked after a R/W transfer of data has been completed. Two 4-bit D

type F/F registers L72 and L74 are clocked by*IN00 (IO) after each transfer. Each status bit is described below and will be further discussed during the description of the disk operations. The eight status bits are defined as follows when active (low).

1. Bit 0 =*CRC ERR - If CRC (Cyclic Redundancy Check) from previous disk READ is bad.
2. Bit 1 =*HDR ERR - If header bytes do not match.
3. Bit 2 =*LTZ - If the R/W head is positioned at TRACK 00 the signal will be low - (Not used as a status bit). This signal indicates to the host system that the R/W head is positioned properly for seeking a desired track.
4. Bit 3 =*WPT - Active if floppy write protected.
5. Bit 4 =*DK RDY - If disk is not physically ready; power not on; disk not in drive etc. Requires operator intervention.
6. Bit 5 =*HDWR ERR - Hardware error if electronic failure, i.e., write check, sync bits not detected, seek incomplete, etc. An implied hardware malfunction which possibly can be corrected by a retry (RESTART) of the disk operation.
7. Bit 6 =*PTY ERR - If parity error or*DLER (Data Link Error) occurred during a DMA write operation.
8. Bit 7 =*DMAC - DMA completed/Seek completed.

2.3.5 READ OPERATION - FOR FLOPPY AND HARD DISKS (Figures 2-10 and 2-11)

The following discussion will include the READ operation for accessing data from either the floppy or hard disk. The operation for a write is very similar to a read therefore much of the read operation discussed will be applicable to the write operation (paragraph 2.3.6). The interface signals from and to the disk controller will be identified and indications to their source and destination will be included.

2.3.5.1 *OUT B - READ OPERATION

OUT B*is a read command issued by the MCPU during the startup (IPL) period and prior to the system being brought up to a steady state condition. During word processing periods all disk read operations are requested by one of the peripherals and commanded by the Master CPU.

OUT B*initiates a read of 256 bytes of data from either a floppy or hard disk. The selection of the type disk is normally automatic and depends on the system model. The disk READ operation proceeds as follows:

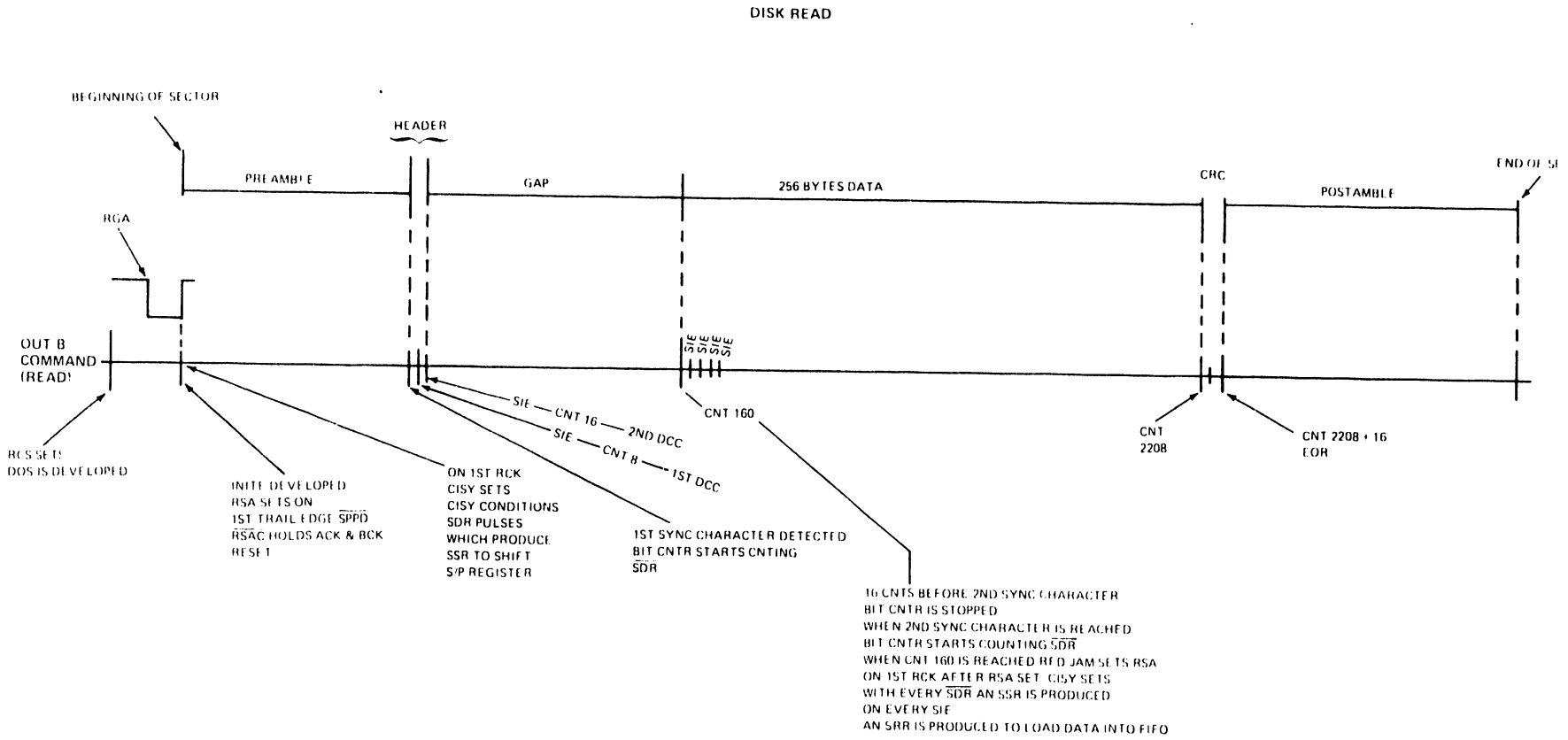


Figure 2-11 Master Disk Controller-Sector Read Event Chart

1. The*OUT B command is stored in a D-type F/F that is preset producing output signal Read Command Stored (RCS) at L38-9.

2. OUT B*also gates the Surface Operation signal*(SOP) output at AND gate L5-12 that clears the status bits*CRC ERR and*HDR ERR at the output of F/Fs L33.

3. RCS gates signal Data Order Stored (DOS) at the output of L37-6. DOS is NANDed with Sector Pulse Present (SPP) producing signal Sector Pulse Present Detected*(SPPD) at L22-3.

4. SPPD*is the enabling signal for four functions required to start the read operation:

   a) The leading edge of*SPPD gates signal*RSAC at the output of AND gate L49-12. *RSAC is the inhibit signal for the A and B clock generator on the MCPU board. Refer to paragraph 2.2.15.

   b) The leading edgeof *SPPD presets the Read Gate Allow (RGA) F/F at L36-5.

      1. RGA produces signal*RDG (read gate) at the output of L6-6 that is routed to the HARD DISK (only). *RDG activates the selected read head.

      2. RGA is routed to Master Memory to select the DMA read operation.

      3. RGA F/F output L36-6 gates signal Write Read Gate Allow (WRGA)*at L19-11 enabling L48 F/F to set.

   c) The trailing edge of*SPPD clocks the Initiate Enable (INITE) F/F reset at L29-6. *INITE gates*INDF (Initiate Data Flow) active at the output of L51-11 which is routed to the MCPU and MDL for controlling the transfer of data.

   d) The trailing edge of*SPPD also clock sets the enabled Resync Allowed (RSA) F/F at L23-5. RSA is inverted to perpetuate the A and B clock inhibit signal*RSAC.

      1. RSA enables the Read Clock*(RCK) from the disk drive to set the Controller In Sync (CISY) F/F L23-9. *RCK is the syncing clock.

5. With RSA and CISY active, the leading edge of the inverted RCK clocks (generated for each bit read from the disk) will gate Shift During Read*(SDR) pulses out of NAND gate L18-6.

6. SDR*pulses gate Shift Serialization Register (SSR) clock pulses out of NAND gate L22-8 to the clock inputs of the Disk Data S/P registers L79 and L82. At this point in time the controller is looking for the first sync bit. The first sync bit is the seventh bit of the twentieth byte (HEX 03) formatted in the preamble field.

7. Read Data*(RDD) are serial data bit pulses accessed from the disk which preset the Read Data In (RDI) F/F at L16-8. *RDD and*RCK signals alternately set and reset the F/F for active data bits.

8. The*03 F/F L11-6 was cleared by INITE 3 enabling RDI to gate Serial Data In*(SDI) to the J/K inputs of S/P register L79.

9. The decode of the three SYNC 1 bits (011) by L20 and L22 produces a low which is presented to the D input of the*SCD (Sync Character Detected) F/F L21-9 causing it to reset on the next*SDR clock.

10. SCD*enables*SDR (RCK) clocks to start incrementing the data bit counter while loading the S/P register with the first header byte. The clocks are gated via gates L20-10 and L37-11 to the data bit counter which consists of three synchronous 4-bit counters L26, L27 and L28.

11. When the bit counter reaches the seven count, signal C7 enables the SIE (Step Into Eight) F/F to set on the next*SDR clock at L21-5.

12. SIE, when set, indicates that the first header byte is loaded into the S/P register. SIE is the gating signal at the input of two AND gates in series which produce signal DCC (Data Compare

Clock) at L5-6. DCC is used to compare the header byte from the 8080 with the header byte read from the disk. DCC clocks two D-type F/Fs L34 that control the address inputs A and B to four Dual 4-line to 1-line data selector/multiplexers L77, L78, L80 and L81.

13. The header comparator consists of eight exclusive OR gates L62 and L65 whose common bus output will enable the*HDR ERR F/F to reset at L33-9 if the comparison fails.

14. If a header comparison error occurs, the*HDR ERR will gate a Set Interrupt Bit*(SINPT) at the output of L49-8. *SINPT will enable the Set Interrupt*(SINR) signal at the output of L15-6 that will initiate an interrupt routine and clear the READ command.

15. A good header comparison will clear the SIE at count 9 and proceed to load the first bit of header byte 2. At count 15, C7 has again enabled the SIE F/F to set on the next clock.

16. The next*SDR clock sets the SIE F/F, increments the data bit counter to C16 and gates the second DCC for the second header byte comparison. If the second header compare fails, return to step 13.

17. C16 gates signal*SHC (Strobe Header Check) at the output of L18-12 which performs the following functions:
    a) Clears the CRC chip L7.
    b) Presets the SCD F/F L21 inhibiting the*SDR (RCK) clocks to the data bit counter.
    c) Clears the RSA F/F L23.

NOTE:

If the HARD DISK is selected,*FDS will be a high signal at the output of L56-11. This condition will enable the Data Bit counter to (SHORTEN THE

GAP) by adjusting the bit count as required for hard disk operation. The read operation for the hard disk during the GAP period is only 10 bytes as opposed to the floppy's 20 bytes. The adjusted count is performed as follows:

d) Bit counts C16 and NOT*(C64 and*C128) are ANDed at the output of L40-8. This output NANDed with*FDS and DOS at C16 time loads the middle bit counter L28 with a 96 count. (The 96 count represents the two header byte counts 16, and ten of the gap count bytes (80) not formatted onto the hard disk.)

18. The next*SDR (RCK) clock resets the CISY F/F L23-9 enabling the output*RSAC of AND gate L49-12 to go high. This signal releases the inhibit on the A and B clock (ACK, BCK) generators.

19. BCK is substituted for RCK to increment the data bit counter up to count C160. (The remaining ten gap bytes.)

20. Bit count C160 at L14-3 enables signal*RFD (Resync For Data) at L25-8 performing the following functions:
    a) Clears the S/P register.
    b) Presets the RSA F/F which turns around and inhibits*RFD.

21. The preset of RSA F/F enables the D input of the CISY F/F which is set on the next*RCK clock.

22. The setting of CISY F/F causes the following events to occur:
    a) Enables*RSAC to again inhibit the A and B clock generator.
    b) Enables the RCS F/F to reset gating signal DOS low.
    c) Enables the*SDR clocks to generate the SSR clocks to commence shifting the data into the S/P register.

23. The last three bits of the GAP count 011 are the SYNC 2 character bits which designate the start of the data field (256 bytes). The three sync bits are again decoded enabling the*SCD F/F to reset on the next*SDR*(RCK) permitting the controller to resync with disk clocks.

24. The READ of 256 bytes commences with the*SDR pulses incrementing the data bit counter. At count C=168 the SIE F/F is set enabling AND gate L3-6 to clock set the enabled L16 F/F producing an output at AND gate L47-8. The output DLG (Data Load Gate) is routed to the MDL for controlling the selection of data read from the disk requiring parity checks. This procedure is repeated for every byte of data read from the disk until the 256 bytes are transferred.

25. The output from F/F L16-5 is also NANDed with*SDR and SIE to gate signal*DSML (Data Strobe Memory Load) which gates the output of L32-8 producing signal*SRR (Set Read Request). *SRR is routed to master memory initiating the transfer of data read from the disk to Master Memory or to FIFO.

26. When the data bit count reaches C2208 the 256th byte is transferred and the output at AND gate L17-12 is conditioned to go high when*SDR is clocked. At count 2209, (C1) is active generating a low at L31-6 clearing L16-5 F/F inhibiting*DSML at L18-8.

27. Two CRC (Cyclic Redundancy Check) bytes, written onto the disk after the write of 256 bytes, represent a check of SYNC 2 and the 256 bytes. The read of these two bytes back into the CRC chip L7 is a parity check of the same data. If the read check produces a zero output at L7-15 the signal Cyclic Check Error (CCE) will be low and a*CRC ERR will not occur at the input L72-14. These two bytes represent an additional 16 data bit counts bringing the total count to C2224.

28. The C2208 count enabling the high output from L17-12 is NANDed with the additional C16 count at the output of L31-8 generating signal*EOR (End Of Read). *EOR performs the following sequences:

    a) EOR*is a clock for setting the*CRC ERR F/F L33-6 if an error occurs.

    b) EOR*gates signal*ERWF (End Of Read/Write Format) at the output of L47-11 which in turn gates signal*SINPT (Set Interrupt bit). *SINPT gates*SINR (Set Interrupt) used to clear the READ command, operation and controller.

2.3.6 WRITE OPERATION - FLOPPY AND HARD DISKS (Figures 2-10 and 2-12)

2.3.6.1 General Information

The disk write command is, in operation, similar to the disk read command in that each operation commences with events that parallel each other until the decision to READ or WRITE is reached. The initial difference is the storing of the write command*OUT 0C that starts the disk write operation. Refer to Figures 2-10 and 2-12 as an aid to follow the sequence related in the read operation up to the event where the write decision is made.

The write selection is made under the following conditions:

1. The header bytes have been read and compared.
2. The data bit counter is at count C16.
3. The RGA F/F is enabled to reset when clocked with SHC.
4. RCS is inactive.

2.3.6.2 Decision to Write - Start of Gap

1. The controller is now at that point where the selection of a read or write operation is to be conditioned and selected.

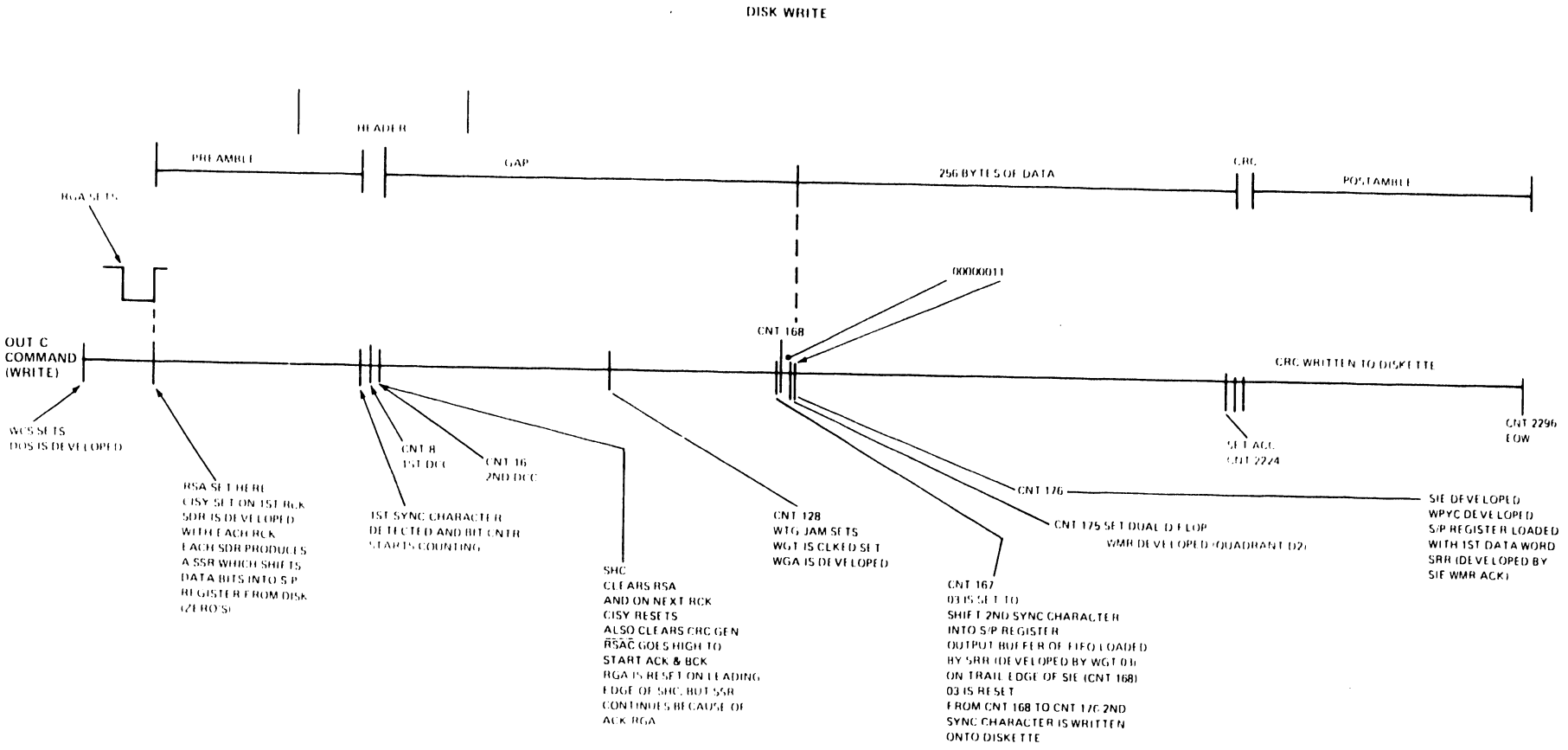


Figure 2-12 Master Disk Controller-Sector Write Event Chart

2. The Read Gate Allow (RGA) F/F is reset on the leading edge of Strobe Header Check (SHC) clock. L16-5 goes low clearing the Read Data In F/F L16-8 enabling Read Data In (RDI) and Serial Data In*(SDI). The low RGA signal at L36-5 also inhibits the read gate*RDG at L6-6 with CISY F/F reset.

3. With the RSA and CISY F/Fs reset and*SPPD inactive, the Resync Allow Clock*(RSAC) inhibit is released at the output of L49-12 enabling the A and B clock generator to operate.

4. The bit counter is incremented by the B Clock (BCK) for both the soft and hard disks when enabled by setting SCD F/F L21.

5. With the Floppy disk selected, the BCK will increment the data bit counter to count C128. (No data will be written onto the floppy disk.) FDS, WCS and C128 will gate a low at the output of L22A-12 presetting the Write The Gap (WTG) F/F L39.

6. With the Hard (Fixed/Removable) disk selected, the BCK will increment the data bit counter to count C144. (Again there is no data written on the disk.) C144 enables the WTG F/F to set on the next*ACK when ANDed with WCS.

7. With RGA F/F reset the ACK is enabled at the output of NAND gate L22-6 generating Shift Serial Register (SSR) clocks at L22-8.

8. WTG F/F is set at either count producing a clock at output L39-9 that causes the following actions:
   a) Sets the Write Gate Time (WGT) F/F L39-5.
   b) Resets the Write Command Stored (WCS) F/F L38.
   c) Clears the Data Order Stored (DOS).
   d) Produces signal Write Gate Allow (WGA) at the output of OR gate L50-11. WGA is inverted at L4-1.

NOTE:

SSR pulses shift zeros into and out of the S/P register which are written onto the disk. The data bit counter will be incremented for each zero written to the disk. Five bytes of zeros are required to write the gap for the floppy disk to bring the data bit count to C168 (C128 + 40 = C168). Three bytes of zeros are required to write the gap for the hard disk to bring the data bit count to C168 (C144 + 24 = C168).

9. WGA is the enabling signal that allows zeros to be written onto the disk. *ACK clocks are enabled at the output of NAND gate L1-3 which are ANDed with WGA to produce Write Clock Data signals WCD*(Floppy) and*WCDH (Hard) that are routed to each type disk.

10. WGA*enables the write gate*WRGT/ERGT output at Q1 which is also routed to the disk units enabling the write process.

11. When the data bit count reaches 167 (C160 + C7), the process of generating the last two bits of the last byte to be written onto the GAP field of the sector is initiated. These two bits at the end of the last byte represent the SYNC 2 character HEX 03 (011). The SYNC 2 character is written on the disk during a Write operation. The SYNC 2 character is included in the last byte to be written in the GAP. The SYNC 2 bits are used to detect and resync the controller at the start of the data field.

12. C160 and WTG generate a high at the output of OR gate L50-3 that is NANDed with C7 and*BCK to preset the*03 F/F L11-6 enabling SDI*(Serial Data In) to enter ones into the last two bits of the S/P register.

13. The preset of the 03 F/F also enables the output of NAND gate L10-3 to generate a Set Read Request*(SRR) developed by WGT and 03.

14. At count 168 the trailing edge of*SIE resets the 03 F/F inhibiting*SDI.

15. At data bit count 175, the first one (1) bit of SYNC 2 appears at the DO7 output of the S/P register L82-11 causing the following functions to occur:
    a) DO7 NANDed with WGT and*C2048 gates a low at the output of L13-6 presetting two L12 F/Fs while generating Write Memory Request (WMR).
    b) DO7 is entered into the CRC gen/comp L72.
    c) The sync bit is written to the disk.
    d) The WTG F/F is reset when the output from AND gate L51-6 goes low.

16. At count 176 the last SYNC 2 bit is written to the disk and SIE F/F is set enabling the*(SRR) which requests the first byte of data to be written onto the disk.

17. SIE enables Write Parity Clock*(WPYC) which is used to clock a parity error F/F on the MDL for every one of the 256 bytes of data to be written on the disk.

18. WPYC*conditions the selector/multiplexer with Load Serial Register*(LSR) signal at the output of L32-12 causing the following operations to occur:
    a) LSR*is NORed with*ACK at output L55-13 to clock F/F L34-6 to a reset state.
    b) The A and B address inputs to the selector/multiplexers L77, L78, L80 and L81 are now (11) which select the Data In bus*(DI0-DI7).
    c) LSR*also enables the parallel loading of the first byte of data into the S/P register to be written onto the disk.

19. The beginning of the data field is indicated by the following:
    a) The data bit count is 176.

b) SIE F/F is set indicating the last byte of the GAP has been written on the disk.

c) WPYC*is developed and sent to data link for parity check.

d) The S/P register is loaded with the first data word.

20. As the first byte of data is serially shifted out of the S/P register by the SSR clocks, the data bit count is incremented bit for bit. At the end of each eight bit count the SIE F/F is set causing the following events to repeat for the remaining 255 bytes to be written on the disk.

a) The*SRR is enabled to request another byte from FIFO.

b) WPYC*is sent to clock a parity error.

c) LSR*enables the parallel load of the requested byte into the S/P register.

d) The SSR pulses shift the data bits out of the S/P register and signals*WRGT and*WCD control the serial write of the data bits on to disk.

21. The controller will continue requesting and writing data to the disk until a data bit count of 2216 is registered. Bit counts C2208, C8 are NANDed with*BCK at the output of L13-8 producing a clock that resets the WMR F/F at L12-5 inhibiting*SRR. L12-9 is reset on the next BCK inhibiting*WPYC and*LSR.

22. The data bit count continues to 2224 shifting the last byte out of the S/P register onto the disk. C2208 and C16 enable the Allow Cyclic Check*(ACC) F/F L11 to set on the next*ACK.

23. The ACC F/F is toggled by each*ACK for reset and by each*ACC clock for preset. The*ACC clock is used to access two Cyclic Redundancy Check (CRC) word bytes that were written into L7 during the write of 256 bytes. These two bytes are accessed by enabling the Check Word Enable with*ACC and clocking the CRC with the output from L8-8 to the input of L7-1. The data bit count continues to increment while the two bytes are serially clocked

out at L7-12. The data is labelled as Serial Data Out (SDO) which is ANDed with ACC and BCK at the output of L8-12. This enables the*ACK to send the two CRC bytes to the*WCD outputs. The data bit count is at 2248.

24. ACC,*BCK, C8 and C64 are NANDed at the output of L25-6 generating End Of Write*(EOW) which initiates a Set Interrupt Bit*SINPT that gates the Set Interrupt*SINR resetting the disk controller. The total data bit count adds up to C=2296.2.3.7.

2.3.7 FORMAT - FLOPPY/HARD (Figures 2-8 and 2-13)

2.3.7.1 General Information

It is assumed in this discussion that the disk drive has been selected and the status checked to be sure that the disk is in operational condition. The R/W head must be loaded and positioned at the proper track. The input sector value is monitored by the 8080 DMA bus. The microprocessor issues a FORMAT OUT 0D command when one sector away from the starting sector.

Floppy - Transition between sectors 14 and 15.
Hard - Transition between sectors 22 and 23.

NOTE:
To format a sector, the head must be positioned and loaded in that sector prior to the sector which is tube written.

The 8080 continually reads the status (IN 00) to be sure that the sector format was completed successfully. For unsuccessful completions, the 8080 will delay 750 us, then issue a clear channel (OUT 0F) command before retrying the operation. For 928 systems the sectors are formatted contiguously on all tracks. The Format command does not change the data in the data portion of a sector. The command only writes the Preamble and the Header bytes. Before the FORMAT command can be issued, the cylinder (track) and sector address registers must be loaded with the appropriate Track and Sector address.

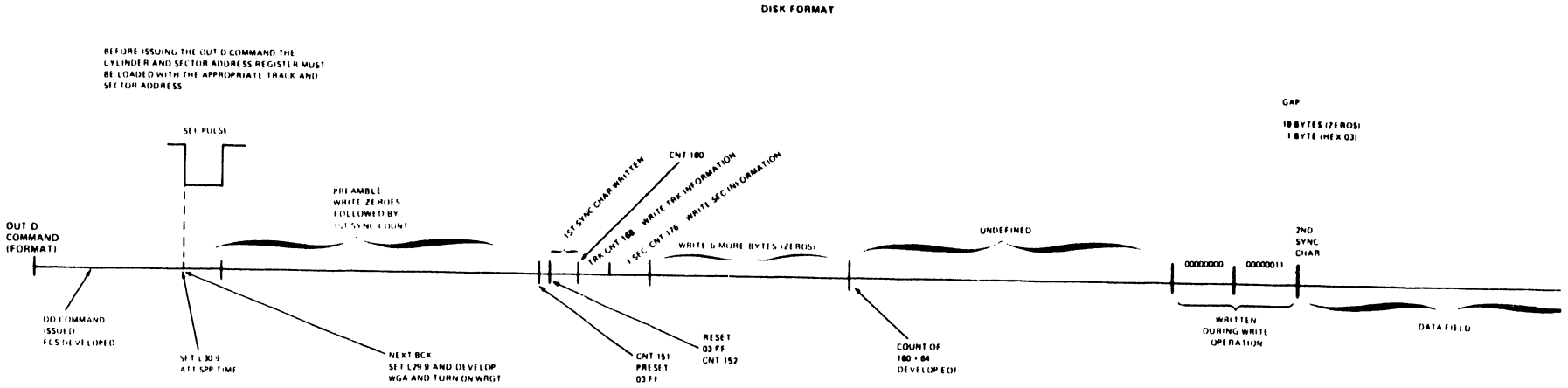


Figure 2-13 Master Disk Controller-Sector Format Event Chart

2.3.7.2 OUT OD - FORMAT COMMAND

OUT OD*(OD)*is stored in the Format Command Stored (FCS) F/F producing a high at output L30-6 enabling the following functions:

1. FCS is ANDed with SPP at L3-11 generating a clock that sets the conditioned L30-9 F/F.

2. L30-9 conditions the L29-9 F/F to set on the next BCK.

3. L29-9 gates Write Gate Allow (WGA) active at L50-11.

4. WGA turns on*WRGT/ERGT via Q1 transistor. This output is routed to the disk drives. *ACK at the output of L1-3 is ANDed with WGA at output L3-3 to commence writing zeroes in the preamble section of the addressed sector via L6-3 (WCDH-hard)*or L15-10 (WCD-floppy).*

5. BCK continues to increment the data bit counter for every ACK*used to write zeroes on the disk that is being formatted.

6. The first sync character (SYNC 1) is written onto the disk in the following manner:
   a) When the bit count 151 is reached, the 03 F/F L11 is preset enabling*SDI (Serial Data In) to the J/K input of the S/P register. C144 ANDed with FCS at L14-8 produces an output at L50-3 that is NANDed with C7 and BCK to preset F/F L11-6 output (03). 03 enables*SDI (Serial Data In) to the J/K input of the S/P register.
   b) ACK is used to gate the SSR (Shift Serialization clock) at the output of L22-8 to shift in the last two bits of SYNC 1.
   c) The 03 F/F is cleared at the data bit count 152 when the SIE F/F L21 is reset. SIE F/F is set at C7 of each byte count and reset at count 8.

d) During data bit counts 153-160 the SYNC 1 byte is written onto the disk. SSR (ACK) clocks continue to shift data out of the S/P register while the BCK enables each bit of data at the output of L8-6 to the*WCD and*WCDH outputs.

7. At data bit count C160 signal*LSR (Load Serial Register) is generated at the output of L31-11 to L50-6 gating the output of AND gate L32-12 low. Header byte 1 is parallel loaded into the S/P register and serially written onto the disk during data bit counts C161 to C168. *LSR also enables the*ACK to increment the Data Selector/Multiplexers address for Header byte 2 by resetting L34-6 F/F.

8. At data bit counts 169-176, SSR pulses shift the sector address (Header Byte 2) out of the S/P register and write it onto the disk. A write of six more bytes (Zeroes) brings the data bit count to C160 + C64.

9. C64 is ANDed with*BCK at the output of L42A-6. L42A-6 is NANDed with C160 and L29-9 gating*EOF (End Of Format) at L43-8. *EOF gates*EOWF at the output of L3-8 initiating the Set Interrupt bit clearing the Format operation.

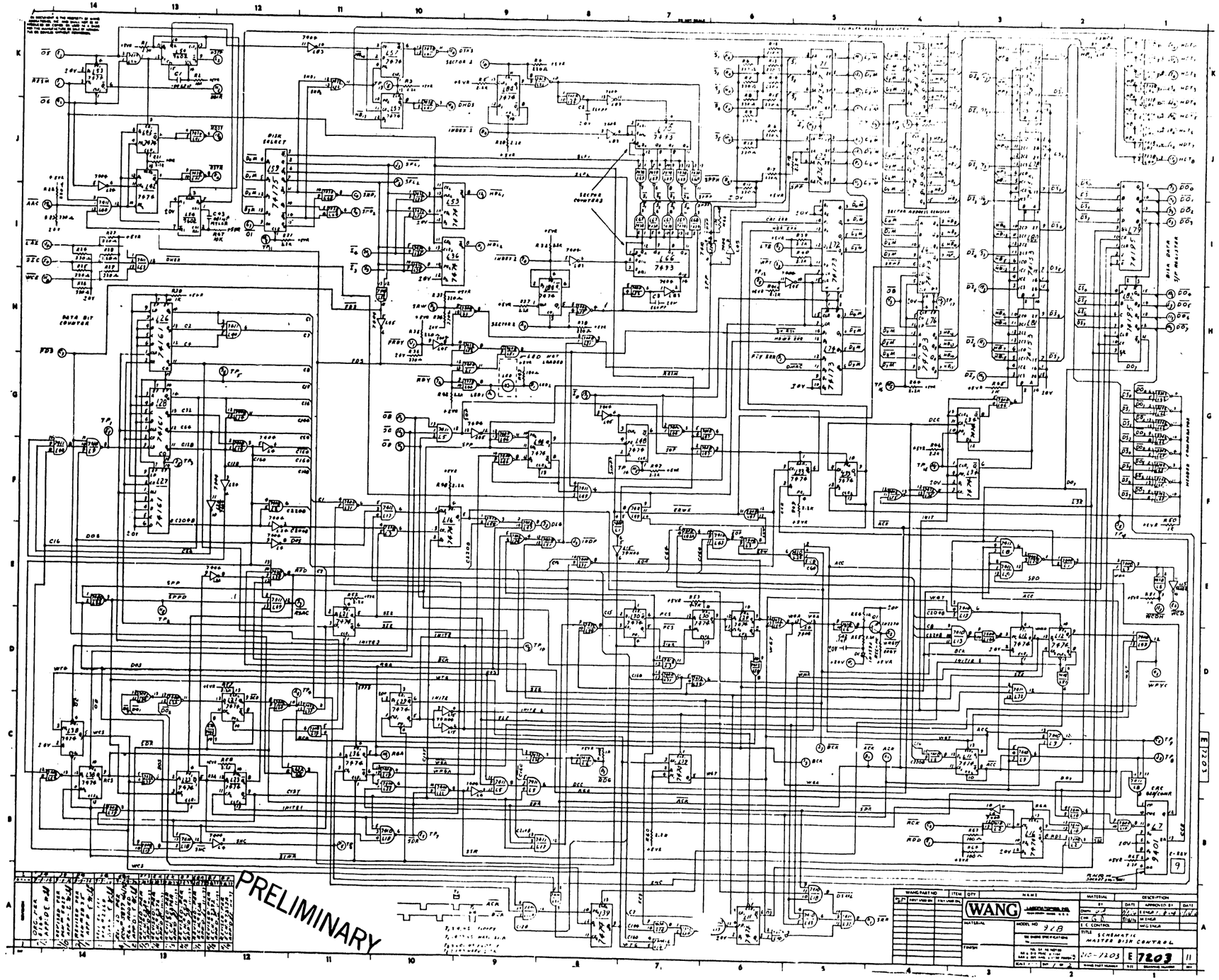


Figure 2-14 Master Disk Controller-Schematic Illustrations — Sheet 1

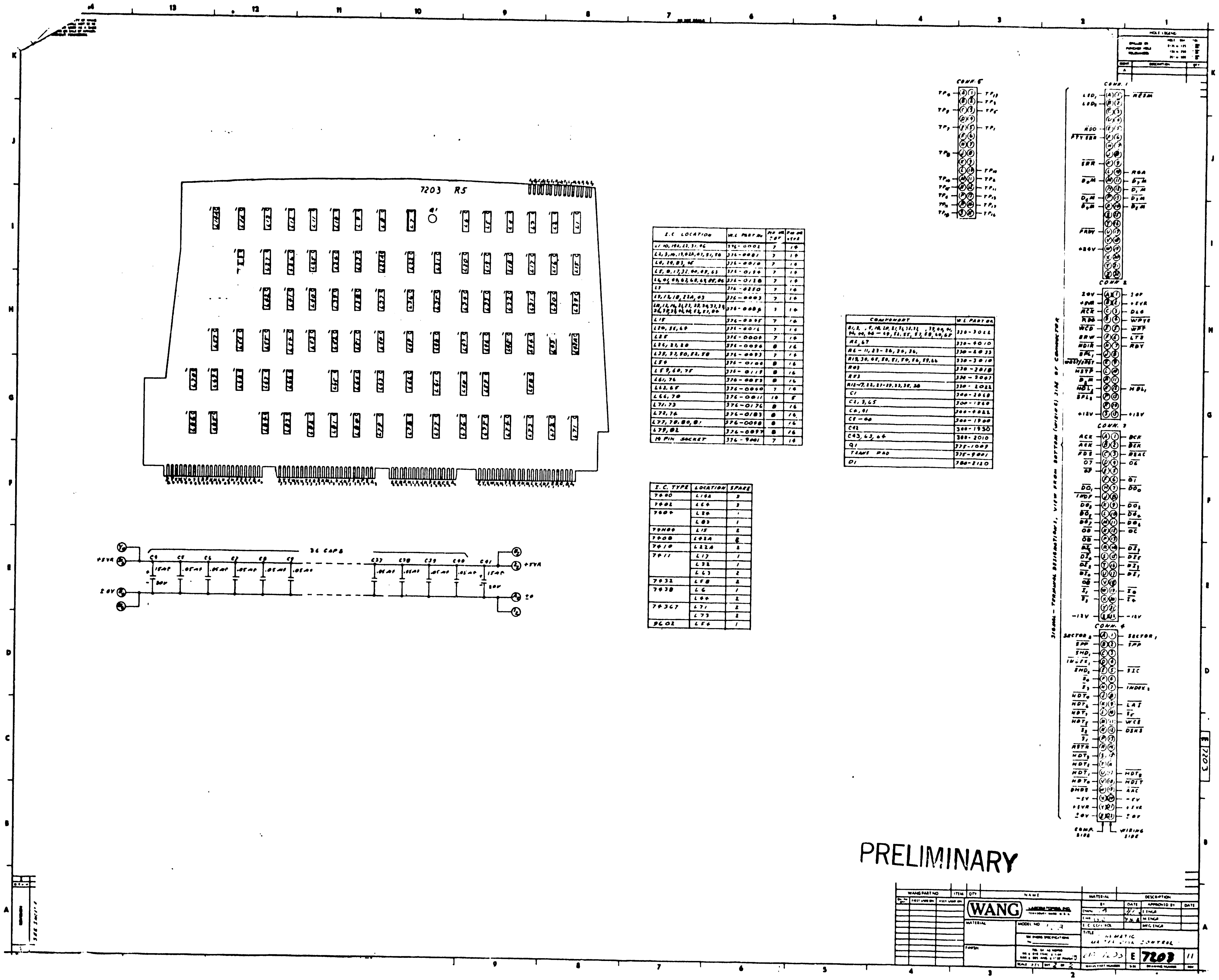


Figure 2-14 Master Disk Controller-Schematic Illustrations — Sheet 2

2.4 MASTER MOTHERBOARD (7205)

The master motherboard is presented because it is the only available semblance of a wiring diagram for the master section. A signal can be traced using the motherboard but the "Seek & Locate" method must be employed to identify a specific signal.

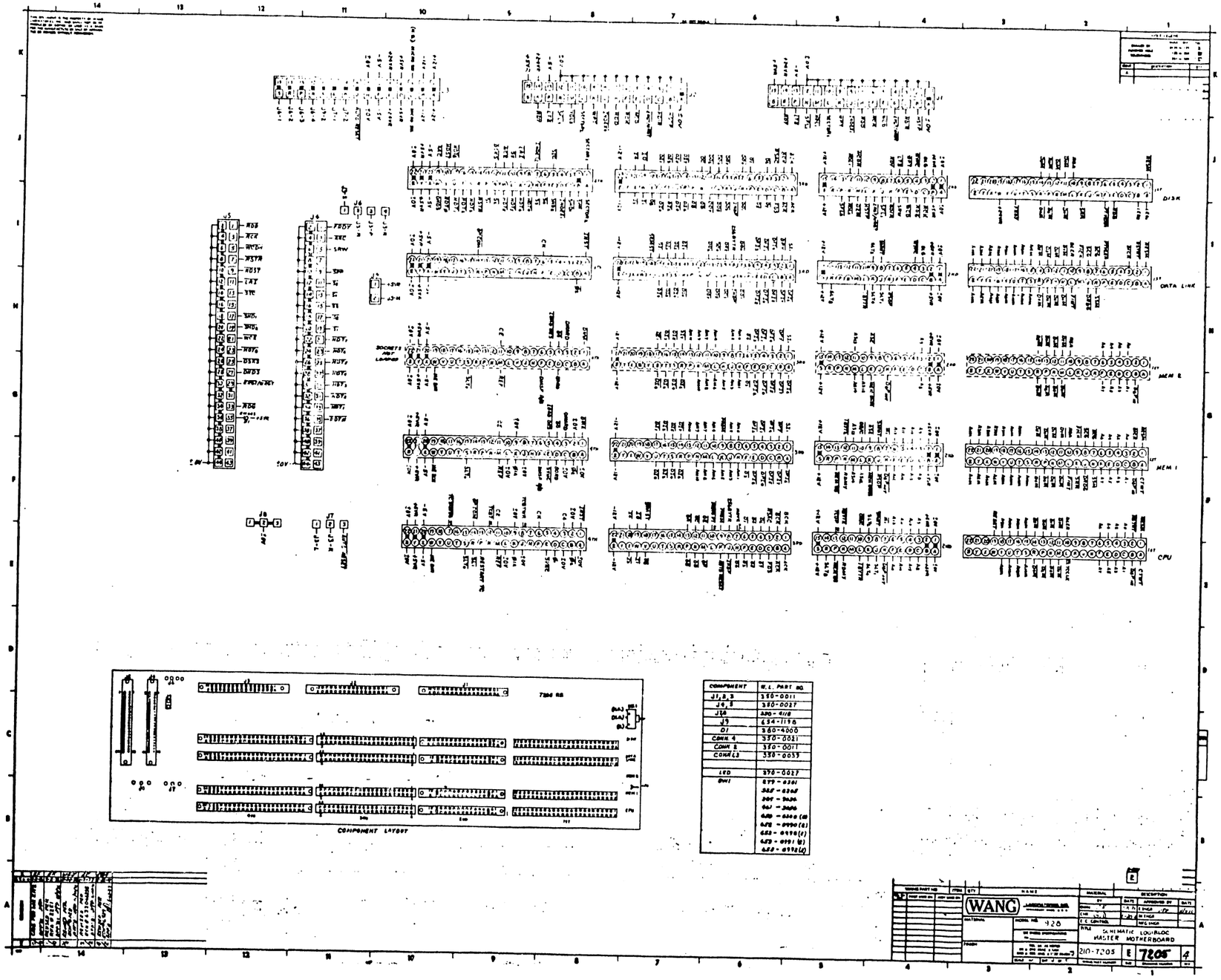
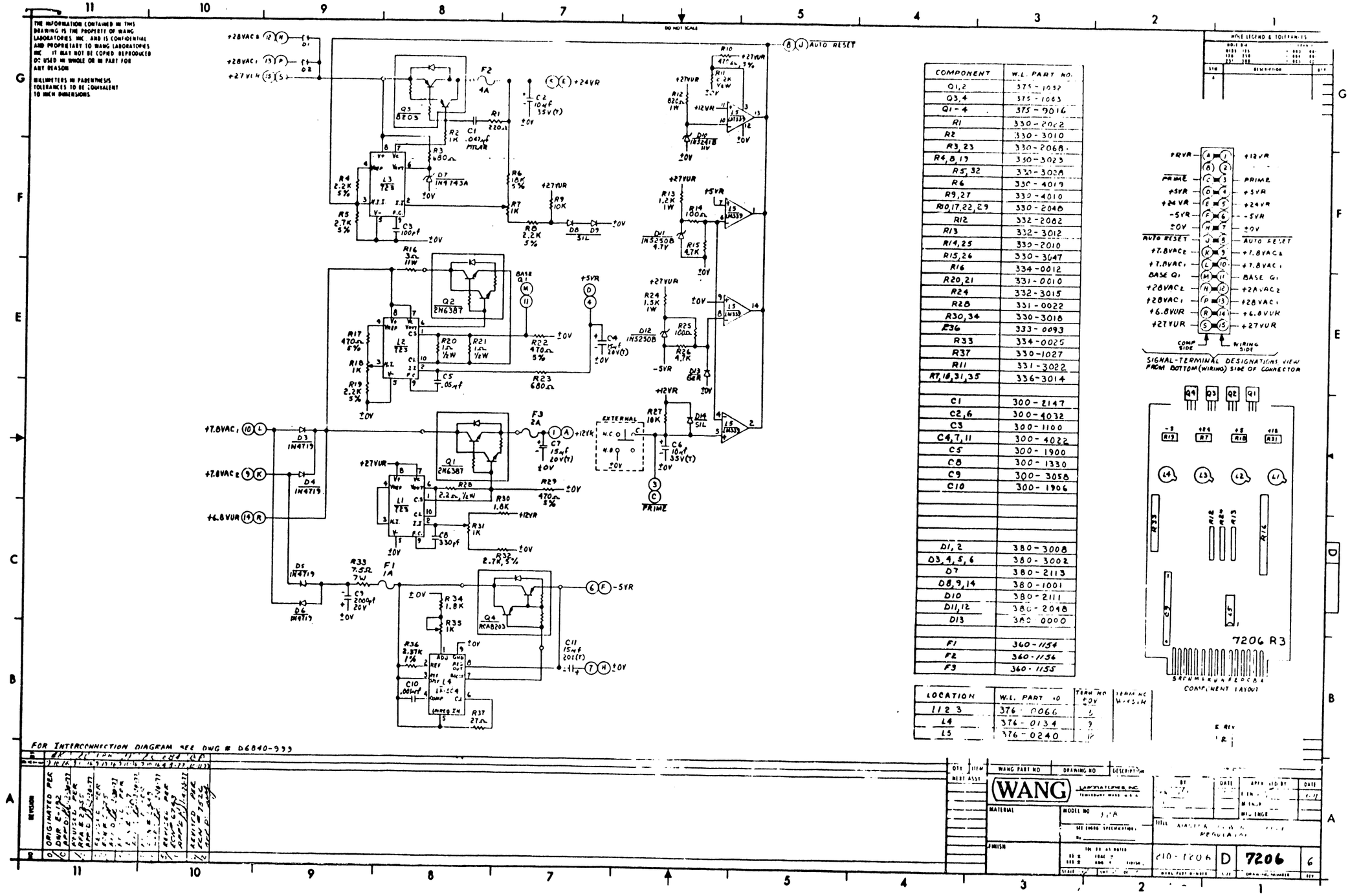


Figure 2-15 Master Motherboard Schematic Illustration

2.5 MASTER POWER SUPPLY/REGULATOR (7206)

The master power supply regulator board supplies the operational voltages for the master section. The schematic is presented as figure 2-16 for reference purposes.



COMPONENT	W.L. PART NO.
Q1,2	375-1052
Q3,4	375-1063
Q1-4	375-9016
R1	330-2062
R2	330-3010
R3,23	330-2068
R4,8,19	330-3023
R5,32	330-3028
R6	330-4019
R9,27	330-4010
R10,17,22,29	330-2046
R12	332-2082
R13	332-3012
R14,25	330-2010
R15,26	330-3047
R16	334-0012
R20,21	331-0010
R24	332-3015
R28	331-0022
R30,34	330-3018
E36	333-0093
R33	334-0025
R37	330-1027
R11	331-3022
R7,18,31,35	336-3014
C1	300-2147
C2,6	300-4032
C3	300-1100
C4,7,11	300-4022
C5	300-1900
C8	300-1330
C9	300-3058
C10	300-1906
D1,2	380-3008
D3,4,5,6	380-3002
D7	380-2113
D8,9,14	380-1001
D10	380-2111
D11,12	380-2048
D13	380-0000
F1	360-1154
F2	360-1156
F3	360-1155

LOCATION	W.L. PART NO	TERM NO QTY	TERM NO WANG P/N
1 2 3	376-0066	6	
L4	376-0134	9	
L5	376-0240	12	

SIGNAL	PIN
+12VR	4
PRIME	3
+5VR	6
+24VR	5
-5VR	7
±0V	1
AUTO RESET	8
+T.8VAC B	9
+T.8VAC A	10
BASE Q1	11
+28VAC B	12
+28VAC A	13
+6.8VUR	14
+27VUR	15

Figure 2-16 Master Power Supply/Regulator-Schematic Illustration

2.6 MASTER DATA LINK--7214

2.6.1 GENERAL DESCRIPTION (Figures 2-17 and 2-18)

The Master Data Link board (7214) is the only link to all slave microprocessors. The link to all slaves is via a dual balanced coaxial line that is flexible and available in lengths from 25 feet up to 2000 feet. Presently the number of data link channels available to the customer are 2, 3, 6 and 14 which depends on the system allotment and options desired. All data transfers via the data link are over the processor communication channel (Direct Memory Access) bus.

The DMA data transfers are as follows:

1) Disk to Slave via Master Data Link
2) Disk to Master Memory via Master Data Link
3) Slave to Disk via Master Data Link
4) Master Memory to Disk via Master Data Link

The common denominator is the Master Data Link for all DMA transfers. The type of data transfers using the DMA bus will be detailed in the following discussion.

2.6.2 DMA CONTROL

2.6.2.1 IN STATUS (INST)

When the Master CPU (8080) interrogates the Status of a slave unit, it receives one byte of information which includes the ID number of the Slave and the status bits. The Status byte accessed from a workstation will include status bits (NR,BP,PR,LE)-(See Mnemonics listing) and a 4-bit ID code. The MASTER must first select the slave channel with an OUT 9 command. (See Master CPU).

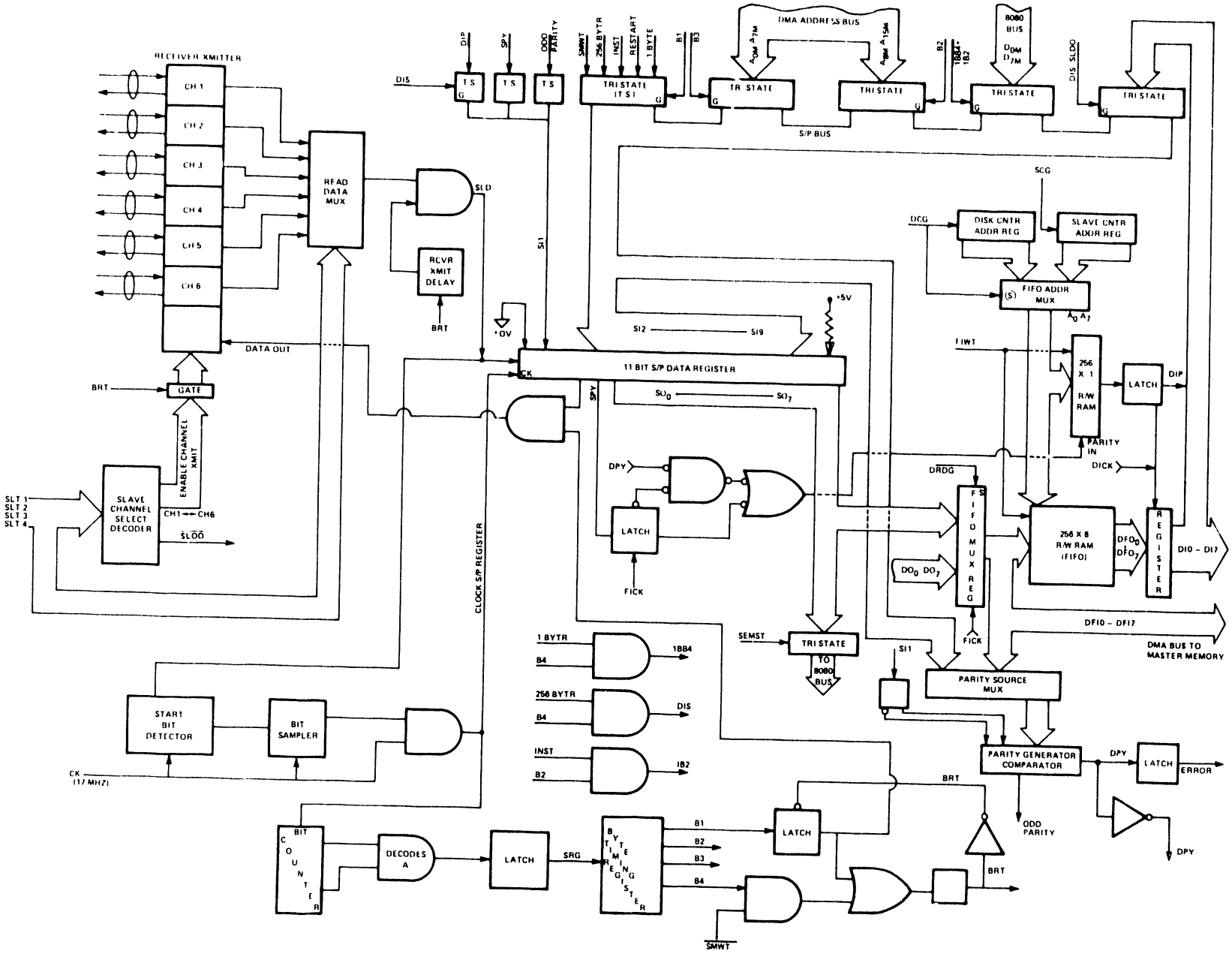


Figure 2-17 Master Data Link-Block Diagram

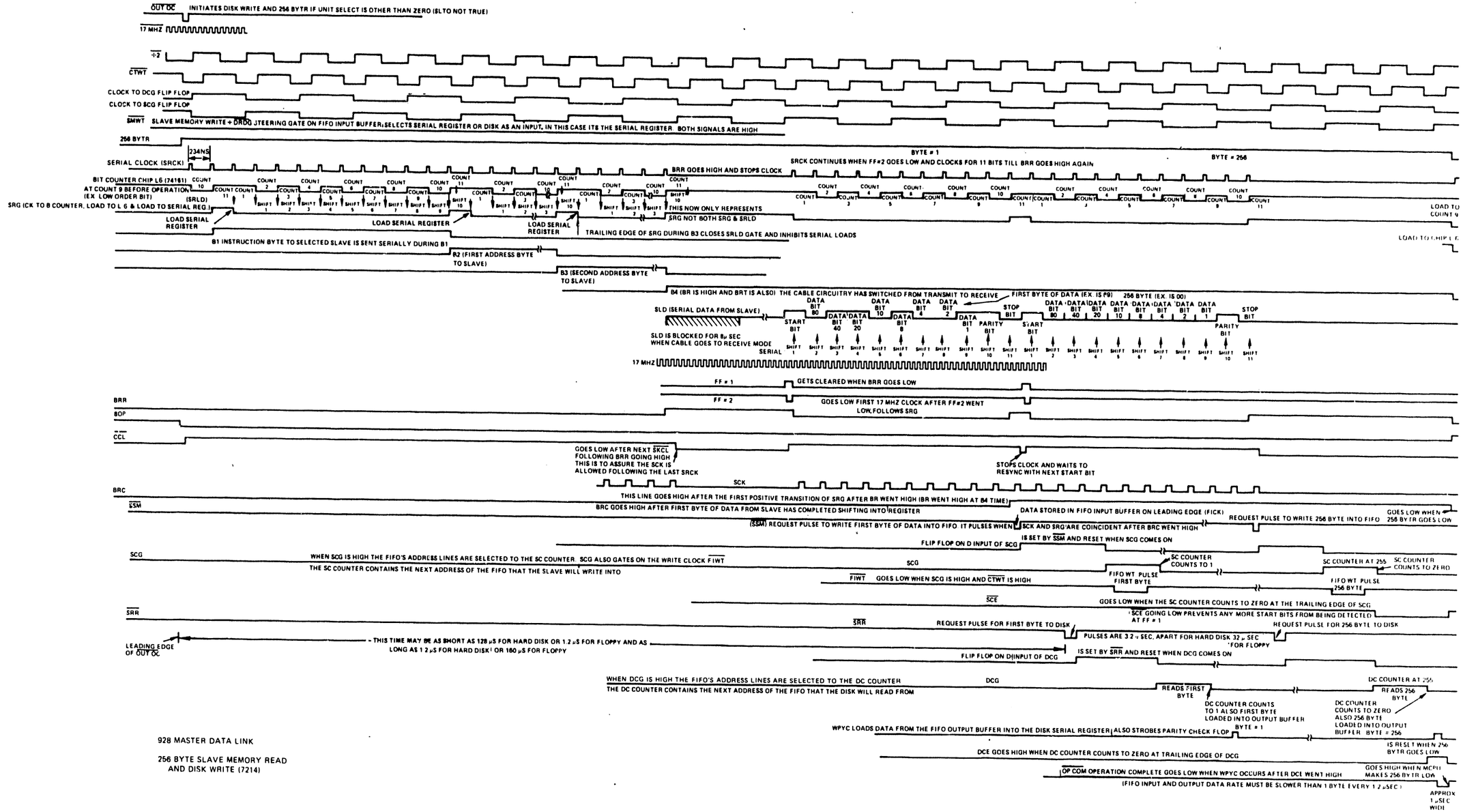


Figure 2-18 Master Data Link-Timing Diagram — Sheet 1

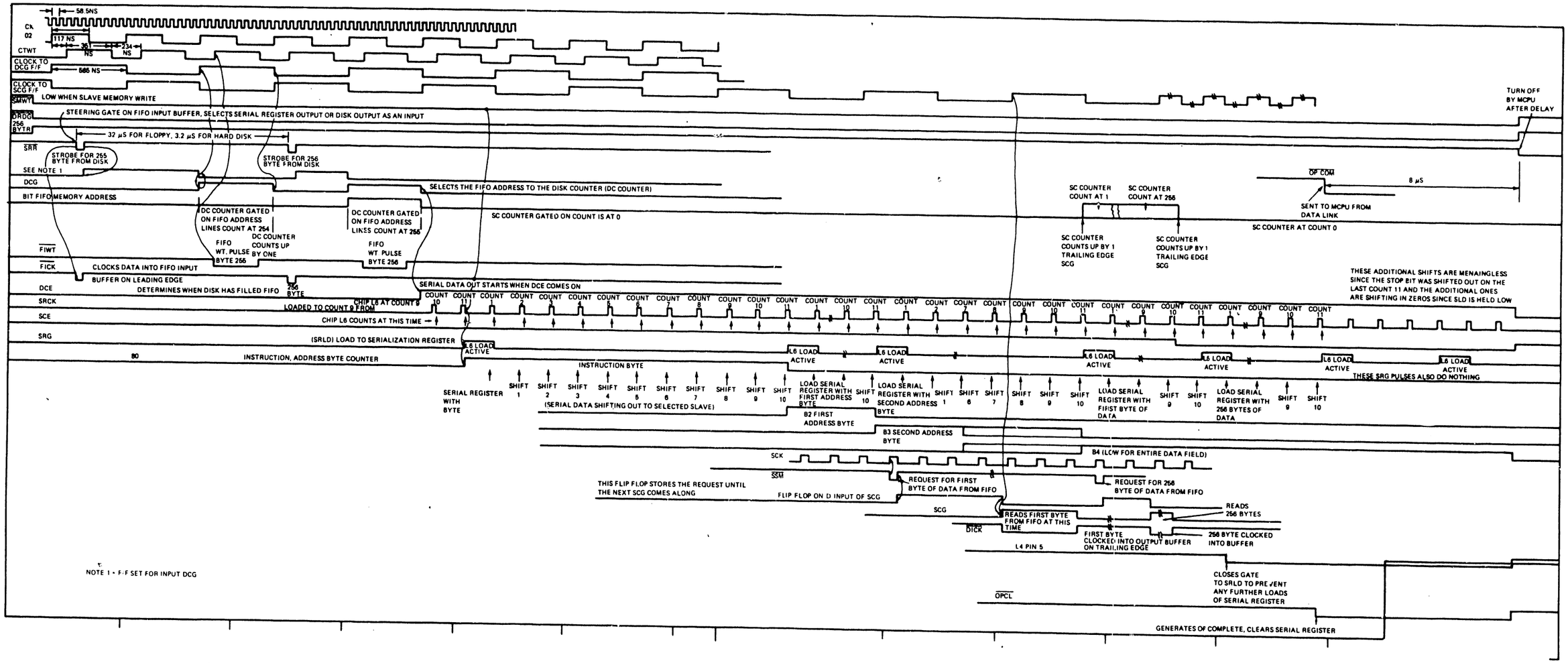


Figure 2-18 Master Data Link-Timing Diagram — Sheet 2

The Master will then issue an address 7 with an INP command (IN7) which sets the IN STATUS F/F on the Master CPU board. Signal*INST is activated and routed to the Master Data Link instruction buffer L96. The Status F/F is used to gate the READY/BUSY input low (BUSY) to the Master 8080 with the*STATUS/1BT input. *INST also initiates an Operation Start (OPS) on the MDL.

Prior to Operation Start (OPS), NOR gate L5-4 is high which is presented to the D input of Bit Counter L6-6. This high and a preset of L53(2) SRG F/F will present a low to the LOAD input of L6. To load the counter with a count of 9 requires an SRCK clock which is generated in the following manner:

1) The Bit Counter and OPS inputs to AND gate L46 produce a low at pin 8 which enables a reset of count 8 F/F L53 (section 1) on the next CK. L53-5 reset output (8OP) enables L99-6 to go low which removes the clear signal for the L100 Bit Sampler F/Fs permitting the SRCK and SCK clocks to be generated.

2) SRCK clocks at the output of L84-8 are used to clock the Bit Counter L6, SRG F/F L53 (section 2) and the S/P registers L47, L48 and L61.

3) Each SRCK clock increments the Bit Counter until the bit count reaches 10 which conditions the SRG F/F to reset on the next SRCK clock via L68-6. This develops SRG as a high and*SRG as a low.

4) The Bit Counter will be clocked by SRCK to a count of 11 when SRG F/F resets. *SRG going low produces a load*SRLD signal that loads the STATUS Header/Instruction byte into the S/P registers but not until B1 time. *SRG also enables the reload of the Bit Counter with a one (1) and also conditions the set of the SRG F/F on the next SRCK.

5) On the leading edge of SRG at the output of L77-6 the Byte Timing register L14 shifts in a one (1) setting byte time to B1. B1 will open the Instruction buffers L92 and L96 to present the STATUS instruction byte to the S/P register which will load on the*SRLD clock. The next SRCK clock will also reload the Bit counter with a count of one (1). B1 is inverted by L76 and routed to multiplexer L11 generating B1S*which enables the STATUS instruction to the input of the S/P register.

6) During B1 time the S/P register is in the shift right mode and on every SRCK clock the S/P register will shift one bit and the Bit Counter will count SRCK clocks. Data is transmitted out of the S/P register in this manner.

7) When the Bit Counter reaches the count of 10 again the SRG F/F will reset on the next SRCK clock and the Bit Counter incremented to count 11.

8) SRG F/F when reset clocks the Byte Timing shift register to B2 time.

9) During B2 time the STATUS word will be returned from the Slave and shifted into the S/P register.

10) INST*and*B2 are ORed at L67-8 producing*1B2 as a low.

11) 1B2*enables signal BR at the output of NAND gate L45-3 which clocks the D-type F/F L41 into a reset state producing BRT and*BRT. BRT when high indicates a RECEIVE mode of operation.

12) Prior to BRT being set, the Receive/Transmit logic which consists of F/F L39 and a synchronous counter L40 were cleared and preloaded with a deficit count of 12 respectively. BRT initiates a receive delay of 7us (12 PHASE 2 clocks) before enabling Slave Data (SLD) at L22-12.

13) The Start Bit Detect circuit L101 will monitor incoming Slave Data (SLD) looking for a Start bit at least 58 ns in duration.

14) When the Start bit is captured on the next CK, L101-8 will go low enabling the Bit Sampler L100 to sync with the incoming STATUS word.

15) The Bit Sampler will produce an SRCK clock for every data bit received (11). The required time for loading one byte is 2.57 us. The SRCK clocks are counted by the Bit Counter.

16) When the Bit Counter reaches the count of 10 (one count from having the entire STATUS word assembled in the S/P register) the SRG F/F is conditioned to reset on the next SRCK clock.

17) On the 11th SRCK clock the SRG F/F is reset, signal*SRG goes low and the Bit Counter goes to count 11. *SRG again enables the Bit Counter to reload with a one (1) and the SRG F/F to set on the next SRCK clock.

18) The reset of SRG F/F produced a clock setting the BRC F/F L44-9 which was enabled in step 11 by signal BR. *BRC gates a low out of L67-6 which produces a low out of AND gate L84-12 clearing the START BIT DETECT circuit L101 and conditions the Bit Sampler to clear.

19) Operation Complete*OPCOM is generated from a low at L21-8 NAND gate with inputs BRC &*SKCL & (INST +*1BYTR).

20) OPCOM*is routed to the Master CPU board 7202 and clock sets the JK F/F L79-12 inhibiting the LOAD input to the delay counter L65 (loaded with a deficit count of 2).

21) After two PHASE 2 clocks are counted the JK F/F output L79-9 is conditioned to set on the trailing edge of the second PHASE 2 clock producing OP.

22) OP*will clear the STATUS/1BT (Busy) F/F to the 8080 READY input so the CPU can access the data held in the S/P register. OP enables L28 D-type F/F which is set on the next PHASE 2 clock. The output at L28-9 is NANDED with PHASE 1 generating*OPC clearing the INST F/F L43 (2).

23) Once INSTATUS is cleared on the Master CPU then OPS is removed on the Data Link. OPS going low will initialize all MDL counters and F/Fs for any succeeding operation.

2.6.3 256 BYTE WRITE--MASTER DATA LINK
(Disk data transfer to Slave memory)

The 256 BYTE WRITE operation requires the reading of data from the disk in single sequential bytes in 256 byte quantities and transferring the bytes to a selected slave unit where the 256 bytes are sequentially written into the slaves memory. All data transferred in this direction must be processed through the Master Data Link. A temporary memory for storing 256 bytes of data read from the disk is required on the Data Link board prior to writing the data to slave memory. This 256 byte memory is called FIFO (FIRST IN-FIRST OUT). When the data read from disk fills FIFO then a 256 Byte Write to slave memory is initiated by the Master Data Link across the coaxial cable.

When FIFO is completely empty the Master Data Link generates OPCOM which is used to clear the DMA control circuitry on the Master CPU.

If the Master Data Link is to perform a 256 Byte Write then a 256 byte read from the system disk must be performed. The Master CPU (MCPU) will send information to the Disk Controller board that will

permit the desired data to be accessed. The MCPU will also select the slave that is to receive the data as well as issue the PAGE address where the data is to be stored.

When the Disk Drive head is positioned over the desired track to be read, the MCPU will read the sector counter. One sector before the read commences, the MCPU will issue an OUT B command to start the Read. Out B also clock sets the DRD F/F on the MCPU gating signal*SMWT active (Slave Memory Write). *SMWT is the DMA R/W signal.

The following events occur during the 256 Byte Write operation:

1) The 256 BYTR (256 BYTE TRANSFER) signal from the MCPU will be presented to the Instruction Buffer via the inverter gate L76-12 initiating a DMA transfer to the selected slave when FIFO has been loaded from Disk.

2) As the Disk Controller 7203 performs the disk read, it will generate the signal Set Read Request*SRR every time 8 bits have been accessed from the disk and assembled in the S/P register of the Disk Controller.

3) SRR*is routed to the FIFO CONTROL logic located on the Master Memory board. Refer to Master Memory 7201.

4) SRR*is NORed with*DRDG (Disk Read Gate) signal to produce a FICK (First In Clock) which will gate the disk data into multiplexed storage registers L64 and L65 via Data Out bus*DO0-DO7. *DRDG is used to control Word Select (WS) for loading the storage registers prior to loading data into FIFO memory chips L49 and L50.

5) SRR*also initiates the generation of a Disk Counter Gate*DCG and a FIFO Write*FIWT signal. *FIWT enables the R/W of FIFO RAM memory and*DCG then clocks the FIFO address counter to the next sequential location in memory.

6) This sequence will continue for 256 bytes until FIFO is full. *DCG clocks address counters L15 and L17 until a carry out CO is presented to D-type F/F L32-12.

7) A full FIFO then produces a Disk Complete Enable (DCE) signal on the next*DCG clock at L32-9. This full state of FIFO (DCE) is ANDed with 256 BYTR and SMWT generating 256SD (256 Slave Data) at the output of L46-12.

8) 256SD will initiate an Operation Start OPS at the output of L5-4.

9) The Master Data Link (MDL) is always initialized at the end of each operation therefore the bit counter L6 is preloaded with a count 9 and the SRG F/F is preset.

10) Under these conditions a low is presented to the input of the count 8, L53 (1) F/F which is reset on the next CK after OPS. This presents a low to the input of L99-5 and a low at the output L99-6 enabling the Bit Sampler to produce SRCK, SCK and SKCL clocks.

11) Each SRCK clock is used to increment the Bit Counter. When the count of 10 is reached the SRG F/F is conditioned to reset on the next SRCK. The reset causes SRG to go high and*SRG to go low and the Bit Counter incremented to count 11.

12) SRG*is routed to the input of NOR gate L28 producing Serial Register Load*(SRLD) at pin 8. The leading edge of SRG is used to clock the Byte Timing register L14-10 via AND gate L77-6. The Byte Timing register will shift in a one to generate B1 time.

13) During B1 time the Instruction Buffer L92, L96 is gated onto the Serialization In (SI) bus by*B1S and presented to the S/P register L61, L47, L48 and the parity generator L97 via two selector/multiplexers L80 and L81.

14) The parity generator produces an odd parity which is gated onto the SI1 bus line and presented to the S/P register at the same B1 time.

15) The SRG F/F in the reset state enables the input at L53-12 allowing the next SRCK clock to set SRG and reload the Bit Counter to a count of 1. During the next 11 counts the S/P register will be shifted right transmitting the byte of data onto the coaxial cable via the channel driver to the selected slave data link. This first instruction byte is used to inform the Slave Data Link of the type of operation the Master Data Link is about to perform (in this case, a 256 BYTE WRITE).

16) As the last bit is shifted out of the S/P register the SRG F/F is again reset by SRCK.

17) SRG on its leading edge will advance the BYTE TIMIMG register to the B2 state.

18) During the B2 state the high order address byte on the DMA address bus will be gated onto the SI bus with the*B2S clock from L11-4 enabling DMA address buffers L93 and L94. The high order address will contain the PAGE of slave memory that will receive the data from the Disk.

19) With the SRG F/F set, the high order address is loaded and shifted out of the S/P register during the next 11 SRCK clocks to the slave data link.

20) On the 11th bit clock the SRG is reset again advancing the Byte Timing to B3 time. B3 enables L11-12 signal*B3S gating the Low Order address onto the SI bus from address buffers L94 and L95 and into the S/P register on the next SRCK.

21) During B3, the low order address will be transmitted to the slave data link. As the 11th bit is transmitted, SRCK will reset the SRG again, only this time data from the FIFO will be loaded into the S/P register.

22) To do this, signal*SSM (Send Slave data to Memory) will go active. *SSM logically consists of ANDing inputs*(B34 & SCE &*256SD) & BRC with 256 BYTR and (SRG and SCK) at the output of L29-6.

23) SSM*is routed to the Master Memory board (FIFO CONTROL) as a clock for initiating the data transfer to the slave. *DICK (Data In Clock) gates the first byte of data presented at the input of FIFO output registers L51 and L52 onto the Data In (DI) bus. Address counters L16 and L18 are at address 00. The Data In bus is routed to buffers L66 and L78 prior to loading the S/P register.

24) SSM*also initiates a Slave Counter Gate*SCG clock which advances the FIFO address counters to the next logical address.

25) SRG F/F was active in producing*SSM and also advanced the Byte Timing to B4 where it will lock up and hold B4 for the duration of the 256 byte transfer.

26) B4 is NANDed with 256 BYTR at the output of L60-11 to generate a Data In Strobe*DIS. *DIS will enable the Tri-State Buffers L66 and L78 to gate data from the FIFO output register into the S/P register. *DIS will also gate Data In Parity (DIP) via Tri-State Buffer L92 into the S/P register.

27) The data in the S/P register will be transferred to the slave data link during the next 11 SRCK clocks. Once the data byte is transferred to the slave data link it will be stored in slave memory starting at the first location of the PAGE pointed to by the previously transmitted two byte address.

28) On the 11th count of the Bit Counter the SRG F/F will reset generating another*SSM to initiate the next data word transfer. This operation continues until 256 bytes of data are stored in slave memory.

29) The FIFO is empty after the 256th byte is transferred. This condition is flagged by a Slave Counter Carry out signal (SCCY) indicating the last address of a FIFO read at L18-15. SCCY enables D-type F/F L12-2 which is clocked by the last*SCG from FIFO control producing a Slave data Complete*SCE signal and returning the FIFO address counter to 00.

30) SCE*and*SMWT are ORed at L13-3 enabling L4-5 F/F to go low on the last*SRG clock while enabling L4-9 F/F to reset on SRG clock. L4-9 reset flags Operation Complete*OPCOM at L7-12 to the Master CPU DMA control.

31) OPCOM*will clear the DMA control circuitry as explained in the STATUS section by resetting the DRD F/F. The reset will also reinitialize the Master Data Link by clearing OPS.

2.6.4 256 BYTE READ-MASTER DATA LINK

To perform a 256 Byte Read transfer from a selected Slave to a Disk, data will be accessed (Read) from the slave memory and transferred to the Master Data Link via the slave data link. Once the data is in the MDL it will be written into FIFO.

There is no requirement for the Disk Controller to wait until the FIFO is full to commence reading the data from FIFO and writing it onto the disk. (This procedure differs from the case of a slave memory write).

When the slave is ready to transfer data to the system disk, the slave will initiate a request to the Master to perform a Disk Write from a specific Page in slave memory of the requesting slave unit. Therefore, the MCPU will load the Page address into the Page Address register, select the slave that requested the transfer and select the Disk Drive which is to write the data.

The MCPU will then issue the TRACK and SECTOR information to the Disk Controller for the disk that will write the data. The MCPU will monitor the sector counter until the Write head is one sector from the sector to be written. When this occurs the MCPU will issue an OUT C command (Disk Write).

The following steps occur while performing the 256 Byte Read:

1) The OUT C command clocks the L53-9 F/F set on the MCPU board enabling the 256 BYTR signal. The*SMWT (Slave Memory Write), however, will not be active because the request is a Read.

2) The 256 BYTR is presented to the Instruction Buffer L96 and NANDed with*SMWT at L30-6 gating OPS active as well as 256DW (256 Disk Write) at the output of inverter L31-6.

3) The Bit Counter L6 is loaded with count 9, and it will require two SRCK clocks to reset the SRG F/F.

4) SRCK clocks will go active from the decoding of the Bit Sampler which is turned on by the Count 8 F/F being reset on the first CK after OPS becomes active. BRR is not active and a low at L99-6 is the controlling enable for the Bit Sampler.

5) When SRG F/F is reset at the 11th SRCK clock the Byte Timing register will shift in the Byte 1 (B1) time.

6) B1 is used to gate the Instruction Buffer presenting the Instruction Byte to the S/P register. SRCK is used to clock the Instruction Byte into the S/P register and SRG being active reloaded the Bit Counter to count 1.

7) During the next 11 counts, the Instruction Byte will be transferred to the selected slave by shifting the data to the right out of the S/P register.

8) As the last bit is shifted out of the S/P register the SRG F/F is reset generating another clock for the Byte Timing register shifting in Byte 2 time (B2). B2 reloads the S/P register with the DMA High Order address byte which is gated onto the SI bus and loaded with*SRLD and the Bit Counter is reloaded with a count of 1.

9) The next 11 bit counts will shift the High Order address byte out of the S/P register over the link to the slave.

10) Again on the 11th count the SRG F/F is active stepping the Byte Timing count to B3 and the S/P register will be in the*SRLD load mode. B3 will enable the DMA Low Order address buffer into the S/P register which is clocked by the same SRCK that reloads the Bit Counter to count 1 and sets the SRG F/F. On the trailing edge of*SRG, the B3RC output of L12-8 F/F will go active inhibiting anymore*SRLD signals to the S/P register.

11) During the next 11 counts, the DMA Low Order address will be shifted out to the slave data link.

12) On the 11th count SRG will reset clocking the Byte Timing register to B4 and reload the Bit Counter to count 1. Since the Master Data Link is now at B4 and*SMWT is not active, BR (Byte Read) at L45-3 is active. Because the Slave Data load (SLD) is inhibited until the Receive/Transmit (R/T) circuit times out, the Bit Sampler will be inhibited from producing any more SRCK clocks until the Start Bit Detector receives the START bit from the slave.

13) BR active clocks the BRT F/F reset permitting the R/T delay circuit to time out in 7us and enabling AND gate L22-12 to gate the Start bit to L101-2.

14) When the Start bit is detected the Bit Sampler will commence producing SRCK clocks. SRCK clocks will be used to shift data into the S/P register and increment the Bit Counter.

15) When the 11th clock count has been reached by the Bit Counter, the*BRC F/F L44-8 will set on the leading edge of the SRG clock gating*SSM (Send Slave data to Memory) at the output of L29-6.

16) SSM*goes to FIFO control (MM) initiating a*SCG and a*FICK clock. *FICK will clock the data assembled in the S/P register into the FIFO input buffer register L64 and L65. *SCG will gate a*FIWT clock to write the first data byte from the buffer into the FIFO. The trailing edge of*SCG will increment the FIFO address counter to the next logical address.

17) Steps 15 and 16 will be repeated until 256 bytes of data have been stored in FIFO.

18) Because there are no restrictions for the disk controller to wait until the FIFO is completely loaded before data can be accessed, the disk controller will issue an*SSR when it is ready to write the first byte of data on the disk.

19) SRR*is presented to the FIFO CONTROL on Master Memory board initiating the Disk Counter Gate*DCG and the Data In Clock DICK*.

20) DICK*gates data into the FIFO output register buffer and onto the Data In (DI) bus which is routed to the Disk Controller board 7203. *DCG steps the disk address to the next FIFO address to be read.

21) SSR*will be generated 256 times by the Disk Controller (once for each byte). When FIFO read has been completed, signal DCE will be clocked active flagging the empty condition at L32-9.

22) DCE enables F/F L39-8 to go active when a*WPYC (Write Parity Clock) is issued by the Disk Controller on the last byte transferred from FIFO. This ends the 256 byte transfer to disk from slave memory by flagging *OPCOM via AND gate L36-3. *OPCOM is routed to the MCPU for the termination of this DMA operation.

2.6.5 1 BYTE WRITE--MASTER CPU TO SLAVE MEMORY

The 1 BYTE WRITE is utilized by the Master to write data into Slave memory one byte at a time. The MCPU initiates the one byte transfer by performing a standard memory write except when the memory write is to a slave, the slave must be selected and the memory address must be greater than 32K.

These specified conditions will enable the 1-BYTE F/F to set in the MCPU DMA control logic area.

A 1-BYTE transfer will enable the DMA ADDRESS 4-bit multiplexer L25, L26 to switch from the PAGE address counter to the 8080 address bus in order to determine the specific location to be accessed in slave memory.

The DMA address multiplexer will truncate the A15 address bit (32K) so the slave address will be within the first 32K of Slave memory.

When the 1-BYTE F/F sets on the MCPU, the 8080 is forced into the BUSY condition. The 8080 will remain BUSY until the MDL completes the transfer operation.

The steps for a 1-BYTE WRITE operation are as follows:

1) A*1-BYTR will be presented to the Instruction Buffer L96 initiating an Operational Start OPS.
2) The instruction byte and the two bytes of address will be transferred to the slave in the identical manner as a 256 BYTE WRITE.
3) However, when the Byte Timing register L14 steps to B4, the signal*1B4W from L45-8 will enable the L4-9 F/F to reset on a SRG clock generating*OPCOM. This conditions the MCPU DMA to reset the 1-BYTE WRITE operation and remove the BUSY condition from the 8080.
4) The*1-BYTR ORed with*B4 produces a*1BB4 signal which gates the data on the 8080 bus onto the SI bus via buffers L78 and L79 and into the S/P register. This is done during the LOAD mode. Data is loaded on the next SRCK clock.
5) During the next 11 counts of the Bit Counter, the S/P register data bits will be shifted and transferred to the slave data link thus ending the 1-BYTE WRITE transfer.

2.6.6 1-BYTE READ-SLAVE MEMORY TO MASTER CPU

When the MCPU initiates a 1-BYTE READ from a slave memory, it will first select the slave whose memory is to be read. The Master will then read the address of the slave memory plus 32K.

The 32K address bit A15 is used to distinguish a slave memory location read versus the Master memory read.

The following steps are performed to process a 1-BYTE read:

1) When the MCPU enters the address for accessing a slave memory location, the A15 address bit is used for enabling the 1-BYTR F/F to be set, (the same procedure as a 1-BYTE WRITE) as well as the DMA address multiplexer for 8080 addressing.
2) OPS is gated active by the*1-BYTR signal from the DMA logic on the MCPU.
3) The 1-BYTE READ Header/Instruction byte and the two address bytes are loaded and transferred out of the S/P register by SRCK clocks as previously discussed in the 256 BYTE READ transfers.
4) As the 11th bit of the second address byte is transferred to the slave, the SRG F/F is active advancing the Byte Timing register to B4.
5) A B4 and*SMWT will enable the clock input to the BRT F/F L41-8 resetting BRT active and initiating the 7us turn around delay. During the delay period, data is inhibited from entering the Master Data Link.
6) After the delay has timed out, the START BIT DETECTOR will monitor slave data (SLD) waiting for a start bit on which to sync.
7) When synced on the start bit, the Bit Sampler will commence producing SRCK clocks which will clock shift data bits into the S/P register and increment the Bit Counter.

8) After the data byte is transferred into the S/P register signal Semaphore Status*SEMST is issued by the MCPU enabling the data byte onto the 8080 bus from data buffers L62 and L79.

9) At the count of 11 the SRG F/F will reset enabling the output of NAND gate L21-8 to go low producing*OPCOM at L7-12 which resets the 1-BYTE READ operation in the DMA section of the MCPU.

10) Single byte operations do not utilize the FIFO.

2.6.7 RESTART--MASTER DATA LINK

When a slave is first powered ON, a WTR (TRAP) circuit generates a power on reset. This is a preset of a F/F which holds the local 8080 reset in a not running condition.

The Master will load the first page of the slave memory with an IPL (Initial Program Load) program. This program is basically a BOOT STRAP loader which will communicate with the Master to request the remainder of the STEADY STATE program.

After loading the first 256 bytes of data (IPL) the MASTER will issue a RESTART command which will take the reset of the local 8080 and set the status of the slave processor to a running condition.

The following steps occur during a RESTART:

1) The Master CPU will issue an OUT 0 command which will set the RESTART F/F.

2) RSTRT*will be presented to the Instruction Buffer L96 and gate OPS active via L29-12 to L5-4.

3) When OPS goes active the Bit Counter is initially loaded with count 9 and the Bit Sampler enabled to produce SRCK clocks.

4) SRCK clocks the Bit Counter to 10 enabling the SRG F/F to reset on the 11th count. SRG clocks the Byte Timing register shifting in B1 time.

5) B1 will gate the Instruction Buffer data to the S/P register that has been enabled by*SRLD which went active because the SRG F/F was reset.

6) On the next SRCK the S/P register will commence shifting the data out, the bit counter will be loaded with a count of one and the SRG F/F will set.

7) During the next 10 counts of B1 time the instruction will be shifted and transferred out of the S/P register to the slave.

8) As the Bit Counter is stepped to count 11 the SRG F/F goes active generating the clock that resets L4-9 that is enabled by a low from L21-12 with inputs*RSTRT and B1. The reset flags*OPCOM to end the RESTART command.

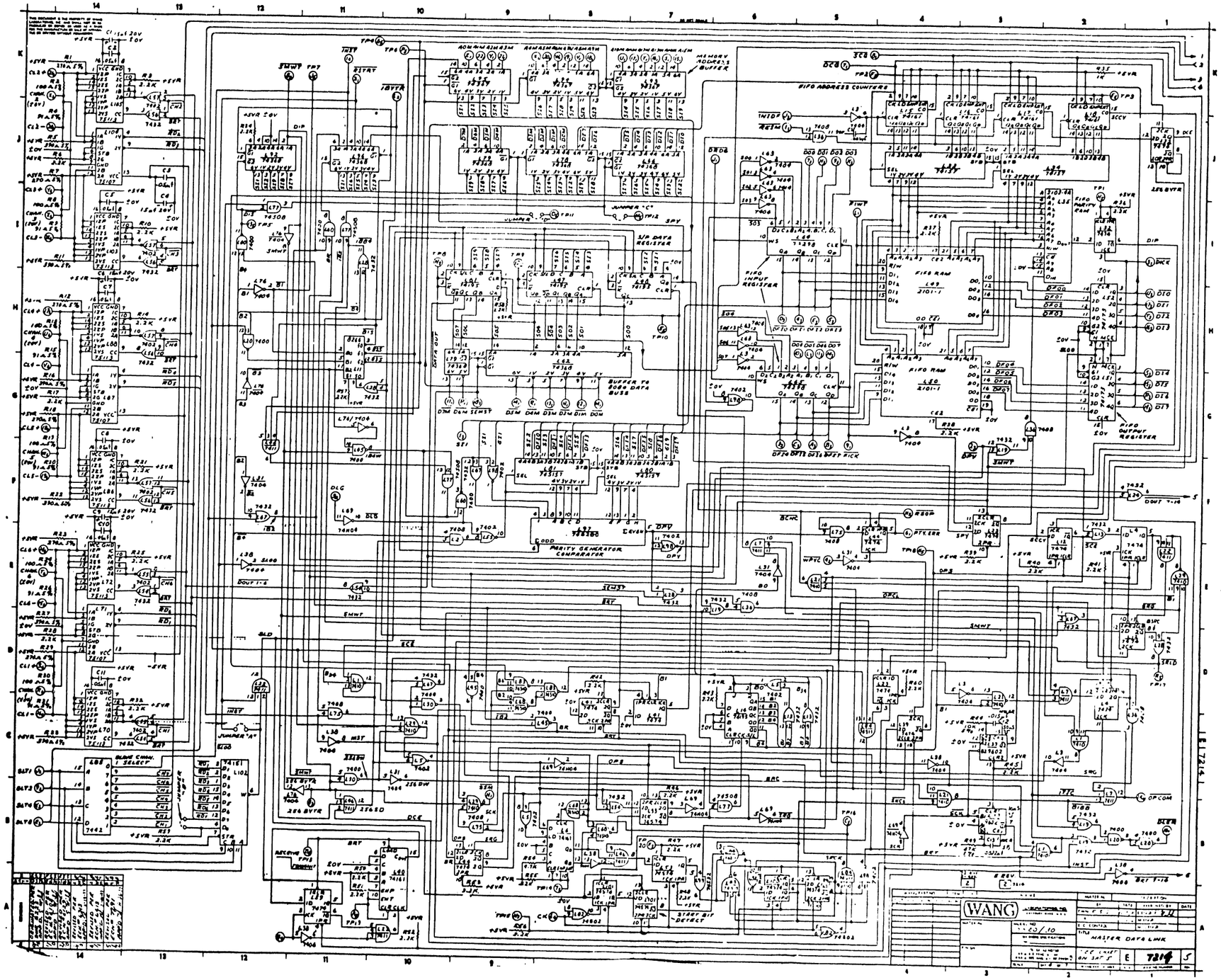


Figure 2-19 Master Data Link-Schematic Illustration — Sheet 1

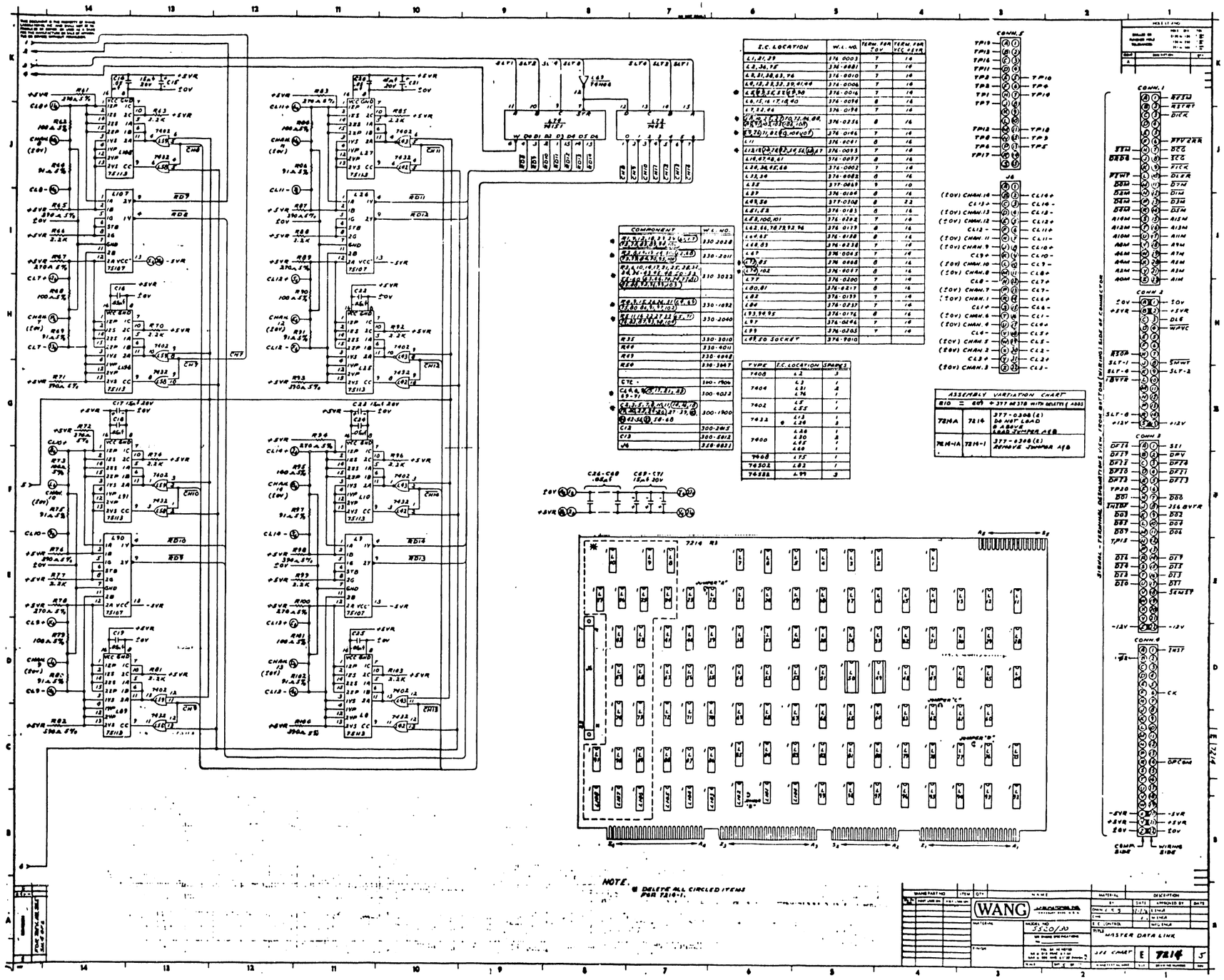


Figure 2-19 Master Data Link-Schematic Illustration — Sheet 2

SECTION 3

WORKSTATION THEORY OF OPERATION

SECTION 3

WORKSTATION THEORY OF OPERATION

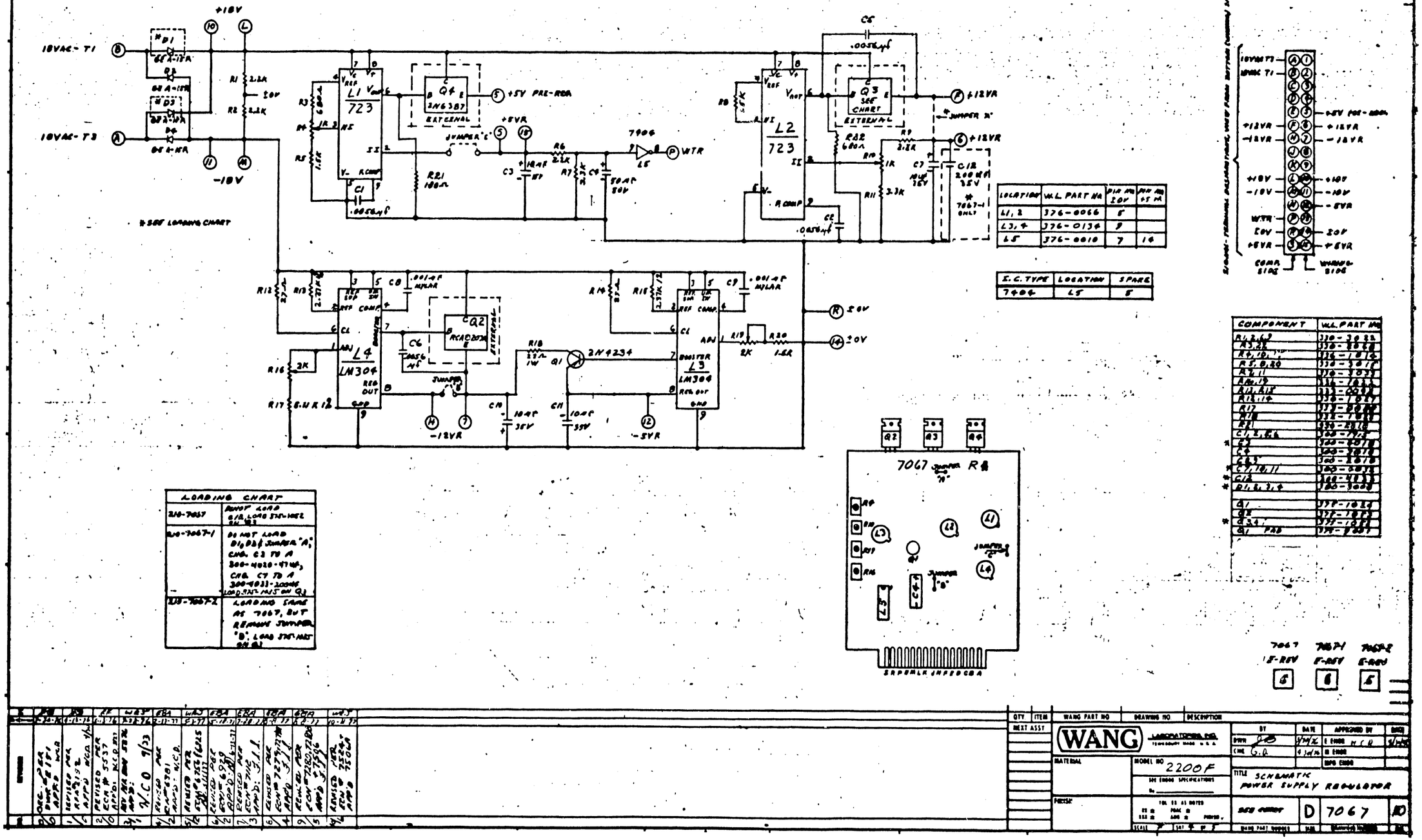
3.1 WANG MOTOROLA MONITOR - POWER SUPPLY REGULATOR (7067)

This power supply regulator is presented as figure 3-1 to:

1) Show the different loading configurations of the basic 7067, the 7067-1 and the 7067-2.
2) To provide the reader with a ready in-section reference to the operating voltages.

DO NOT SCALE

DIMENSIONS IN PARENTHESIS ARE MILLIMETERS. TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.



LOCATION	WL. PART NO	PIN NO 20V	PIN NO +5 M
L1, 2	376-0066	5	
L3, 4	376-0136	9	
L5	376-0010	7	14

I.C. TYPE	LOCATION	SPARE
7906	L5	5

LOADING CHART	
210-7067	SHORT LOAD C18, LOAD SPEC-SHEET SH. #3
210-7067-1	DO NOT LOAD D1, D2 & JUMPER "A", CHG. C2 TO A 300-4020-47MF, CHG. C7 TO A 300-4021-100MF LOAD SPEC-SHEET ON Q1
210-7067-2	LOADING SAME AS 7067, BUT REMOVE JUMPER "B". LOAD SPEC-SHEET ON Q1

COMPONENT	WL. PART NO
R1,2,6,9	330-3022
R3,21	330-6822
R4,10,11	330-1522
R5,8,20	330-3322
R7,12	330-3922
R16,19	330-2022
R17,R18	330-6222
R20	330-1522
R13	330-8222
R14	330-2222
R15	330-2822
C1,3,5,6	300-7022
C2	300-6022
C4	300-3922
C8,9	300-2822
C7,10,11	300-0822
C12	300-4122
D1,2,3,4	300-3022
Q1	370-1022
Q2	370-1822
Q3,4	370-1022
Q1 PAD	370-2022

7067 1ST-REV | 7067-1 1ST-REV | 7067-2 1ST-REV

QTY	ITEM	WANG PART NO	DRAWING NO	DESCRIPTION
NEXT ASSY				

WANG LABORATORIES, INC.

	BY	DATE	APPROVED BY	DATE
DRWN				
CHK				

MATERIAL | MODEL NO 2200F | TITLE SCHEMATIC POWER SUPPLY REGULATOR

SIZE D | 7067 | REV

Figure 3-1 Workstation W/Motorola Monitor Regulator-Schematic Illustration

3.2 CRT CONTROL (7225) - WITH WIDE PLATEN OPTION (7235) (WIDE PLATEN = HORIZONTAL SCROLL)

3.2.1 GENERAL DESCRIPTION (FIGURE 3-2)

The CRT CONTROL board 7225/7235 consists of the WORKSTATION 8080 microprocessor and operating clocks, CRT memory storage area and associated screen raster logic, Keyboard control logic and data controls.

3.2.2 8080 WORKSTATION PROCESSOR (FIGURE 3-3)

The workstation 8080A microprocessor is used to perform the same operations as the 8080 in the master. It addresses its own memory for reading and writing, and uses the same bidirectional data bus with the same function decoder. The similarity exists also for the 8080 clocks but additional clocks are generated for the internal logic used for the following differences.

1) CRT screen display memory (DATA & CONTROLS)
2) KEYBOARD control logic (INPUTS and INTERRUPTS)
3) WIDE PLATEN OPTION (7235 only)

3.2.3 CRT CONTROL--7225 (7235 will be discussed separately)

The workstation CRT display is a 12" screen with a complete chassis assembly and the necessary controls for adjusting the display. There are two front panel operator controls for brightness and contrast. All other CRT controls are internal and should only be adjusted for a component failure or maintenance reasons. The raster for the display is generated by a ROW and CHARACTER counter. The ROW and CHARACTER counters are timing logic required to present the data

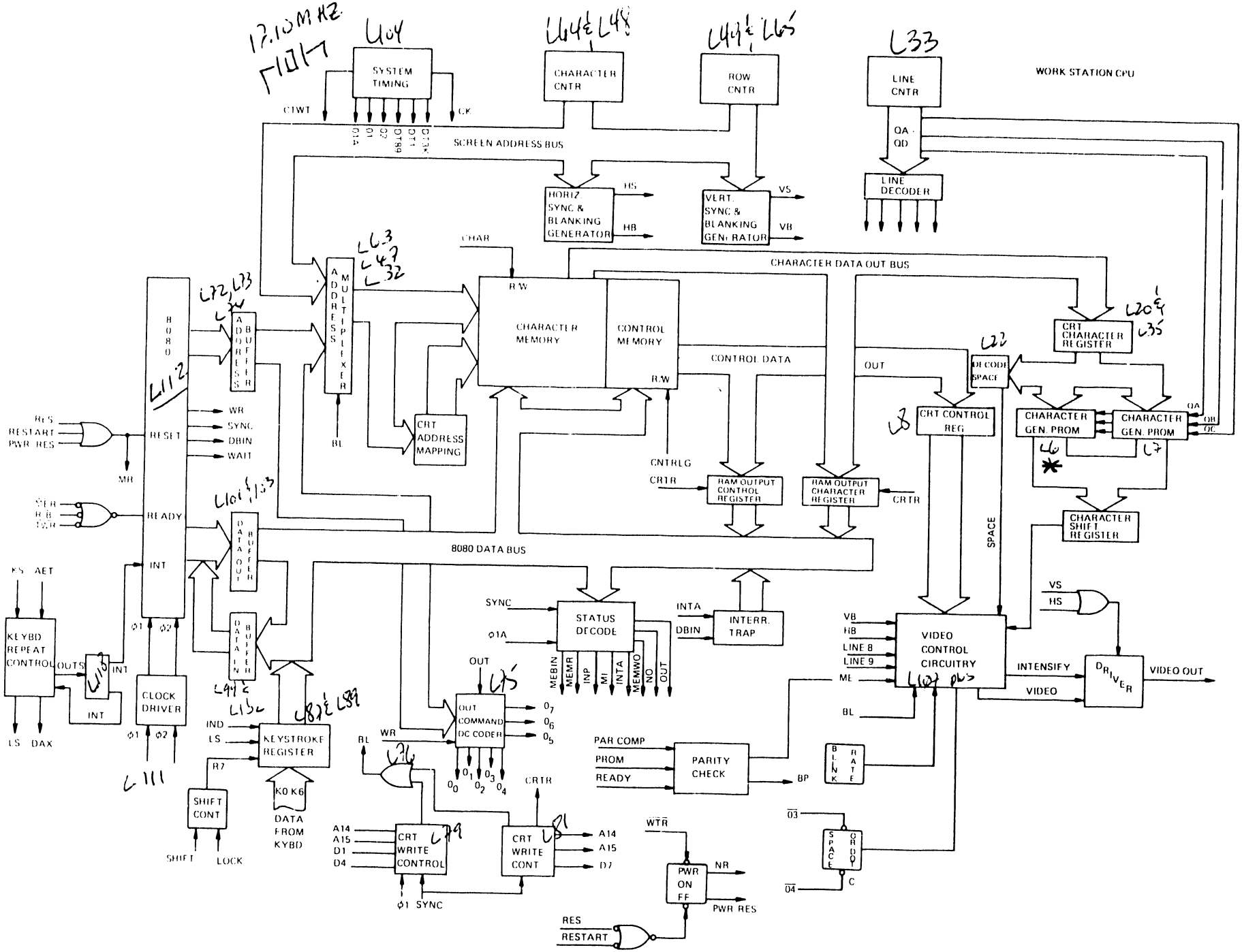


Figura 3-2 Workstation CRT Control-Block Diagram

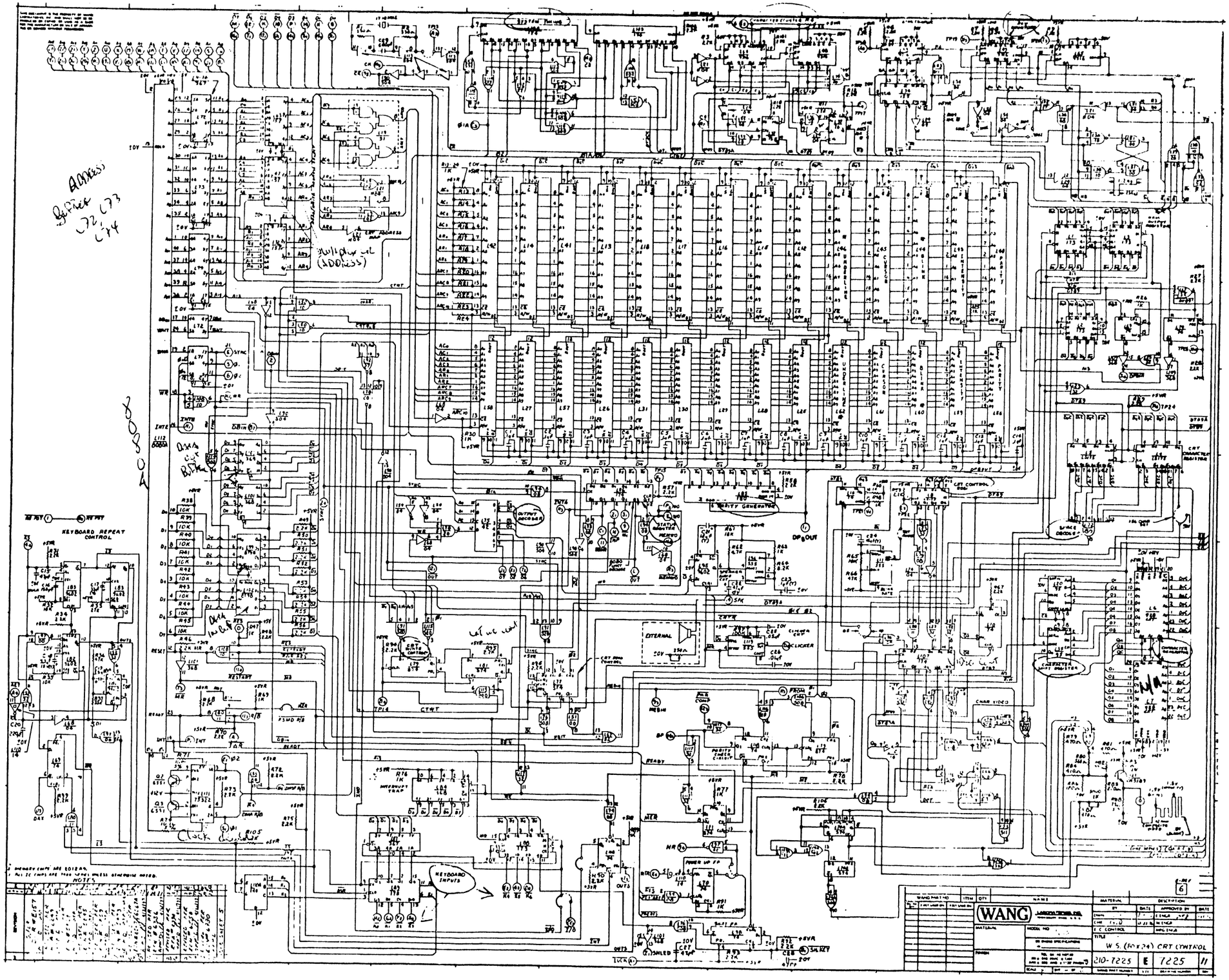


Figure 3-8 (7225) Workstation CRT Control-Schematic Illustration — Sheet 1

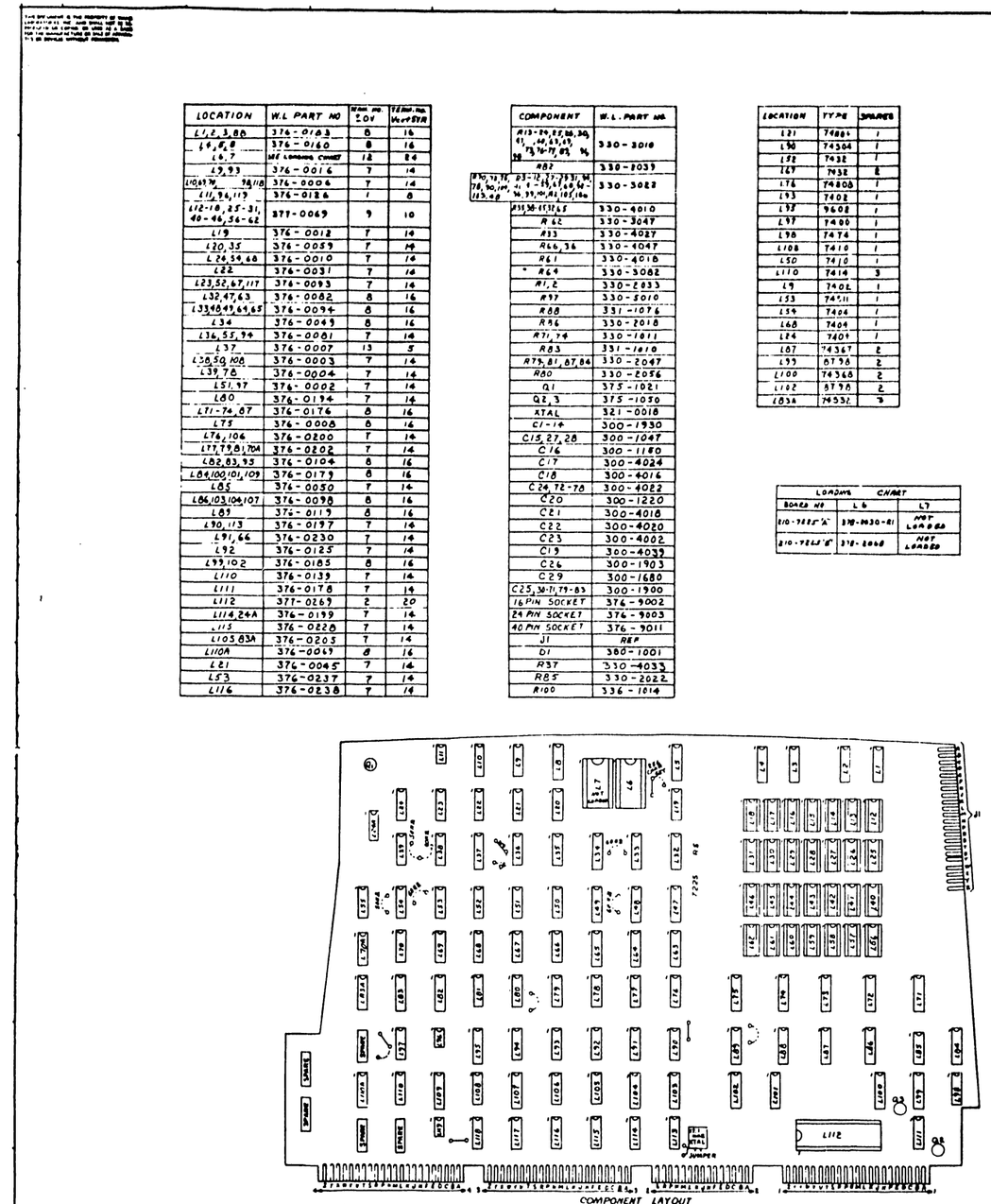
LOCATION	W.L. PART NO	TERM. NO. 5 OV	TERM. NO. +5VR or +5VR
L1,2,3,86	376-0183	8	16
L4,5,8	376-0160	8	16
L6,7	SEE LOADING CHART	12	24
L9,93	376-0016	7	14
L10,63,76,98,118	376-0006	7	14
L11,96,119	376-0126	1	8
L12-18, 25-31, 40-46, 56-62	377-0069	9	10
L19	376-0012	7	14
L20,35	376-0059	7	14
L26,59,68	376-0010	7	14
L22	376-0031	7	14
L23,52,67,117	376-0093	7	14
L32,47,63	376-0082	8	16
L33,49,64,65	376-0094	8	16
L34	376-0049	8	16
L36,55,94	376-0001	7	14
L37	376-0007	13	5
L38,50,106	376-0003	7	14
L39,78	376-0004	7	14
L51,97	376-0002	7	14
L60	376-0194	7	14
L71-74,87	376-0176	8	16
L75	376-0008	8	16
L76,104	376-0200	7	14
L77,79,81,108	376-0202	7	14
L82,83,93	376-0104	8	16
L84,100,101,109	376-0179	8	16
L85	376-0050	7	14
L86,103,106,107	376-0098	8	16
L89	376-0119	8	16
L90,113	376-0197	7	14
L91,66	376-0230	7	14
L92	376-0125	7	14
L99,102	376-0185	8	16
L110	376-0139	7	14
L111	376-0178	7	14
L112	377-0269	2	20
L114,24A	376-0199	7	14
L115	376-0228	7	14
L105,83A	376-0205	7	14
L110A	376-0049	8	16
L21	376-0045	7	14
L53	376-0237	7	14
L116	376-0238	7	14

COMPONENT	W.L. PART NO.
R13-20, 22, 35, 36, 39, 41, 42, 43, 45, 73, 74-77, 89, 94, 98	330-3018
R82	330-3039
R10, 12, 15, 23-25, 27-31, 34, 78, 90, 91, 93, 95, 96, 99, 101, 102, 105, 106, 115, 116	330-3023
R58, 59-61, 63, 65	330-4010
R 62	330-3047
R33	330-4027
R46, 56	330-4047
R61	330-4018
* R64	330-3082
R1, 2	330-2833
R97	330-5010
R88	331-1076
R96	330-2018
R71, 72	330-1811
R83	331-1810
R75, 81, 87, 84	330-2047
R80	330-2056
Q1	375-1021
Q2, 3	375-1030
XTAL	321-0018
C1-14	300-1930
C15, 27, 28	300-1047
C16	300-1180
C17	300-4024
C18	300-4016
C 24, 72-76	300-4022
C20	300-1220
C21	300-4018
C22	300-4020
C23	300-4002
C19	300-4039
C26	300-1903
C29	300-1680
C25, 30-71, 79-83	300-1900
16 PIN SOCKET	376-9002
24 PIN SOCKET	376-9003
40 PIN SOCKET	376-9011
J1	REF
D1	380-1001
R37	330-4033
R85	330-2022
R100	336-1014

LOCATION	TYPE	SPARES
L21	74804	1
L30	74S04	1
L52	7432	1
L67	7432	2
L76	74804	1
L93	7402	1
L95	9602	1
L97	7400	1
L98	7474	1
L108	7410	1
L50	7410	1
L110	7414	3
L9	7402	1
L53	74S11	1
L54	7404	1
L68	7404	1
L84	7404	1
L87	74367	2
L93	8T96	2
L100	74368	2
L102	8T98	2
L83A	74S32	3

LOADING CHART		
BOARD NO	L6	L7
210-7225-A	378-8030-81	NOT LOADED
210-7225-B	378-8068	NOT LOADED

NOTES:
1. REMOVE L94,106,L60,L68 AND ADD TWO (2) 10K Ω RESISTORS FOR WORD PROCESSING VERSION, R103, 104
2. FOR DATA ENTRY VERSION, DELETE TWO (2) 10K Ω RESISTORS, R103, 104 AND ADD L94, L96, L60, L68



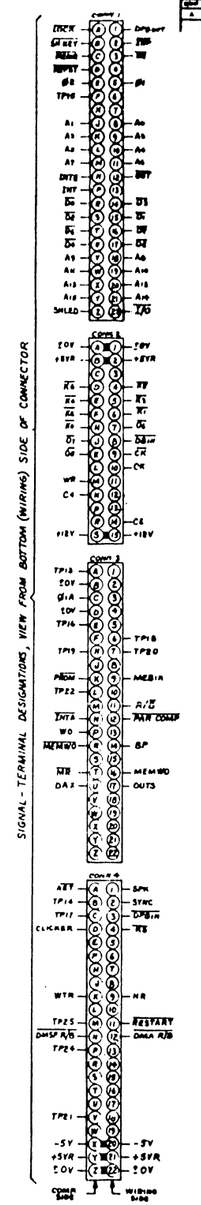


Figure 3-8 (7225) Workstation CRT Control-Schematic Illustration — Sheet 2

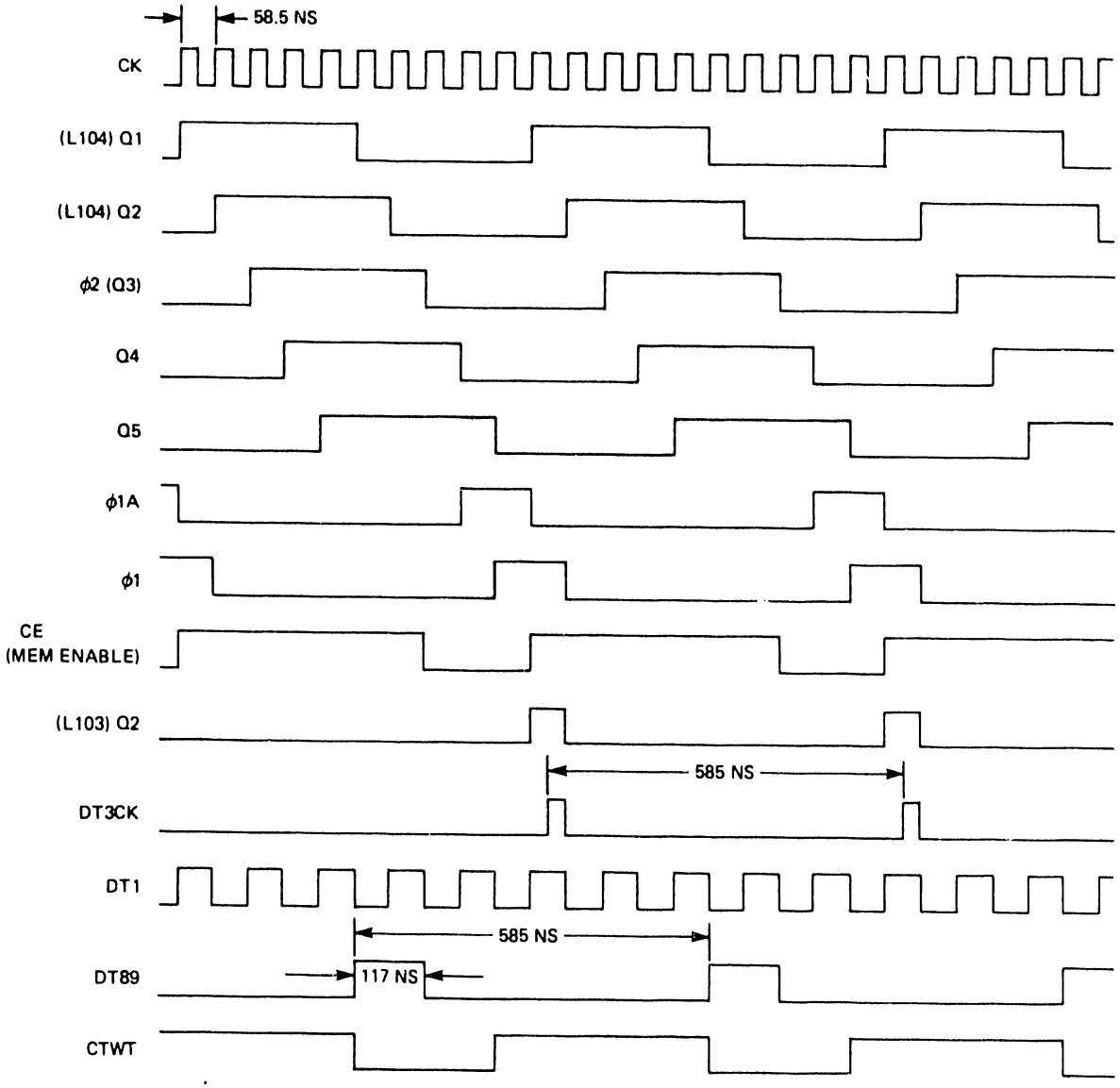


Figure 3-3 Workstation CPU-Timing Diagram

on the display screen in synchronization with the video signals accessed from the CRT memory. The screen has a capacity to display a total of 1920 characters on 24 rows with 80 characters per row (80 characters horizontally). Each row consists of 11 scan lines of which 8 are used to display characters, 2 are used for underscore and cursor, and 1 scan line is used for the space between rows. Each character displayed is made up from an 8 x 8 dot matrix. It should be realized that displaying a full row of characters requires addressing a maximum of 640 locations in CRT memory.

3.2.4 CHARACTER COUNTER (Horizontal counter)--60 HZ (FIGURE 3-4)

The character counter counts the number of characters in each scan line (80 CHAR.) which is repeated for a total of 24 rows x 11 scans per row = 264 scans per visible field.

One scan line for 80 characters requires 58.5 us which includes the 80 characters written on the screen and the blanking time required to retrace the scan for the next line.

The actual character count is extended to 99 counts allowing 11 us of time to generate a Horizontal Blank (HB) pulse and Horizontal Sync (HS) pulse for the horizontal oscillator located in the chassis of the display unit (MFRd by WANG). The character counter consists of two synchronous 4-bit counters L48 and L64 that count up sequentially to a maximum count of 99 which is used to load zeroes into the counter and repeat the next 99 count for each succeeding scan line.

Signal DT89 is inverted by L21 to*DT89A and used for clocking the character counter. *DT89A is the 8 and 9 clocks of CK which occurs every 585 ns for a period of 117 ns. At the count of 80, character counts C4 and C6 enable the K input to J-K F/F L37-16 which is reset by DT89 clock generating*HB (HOR. BLANK). An additional four DT89

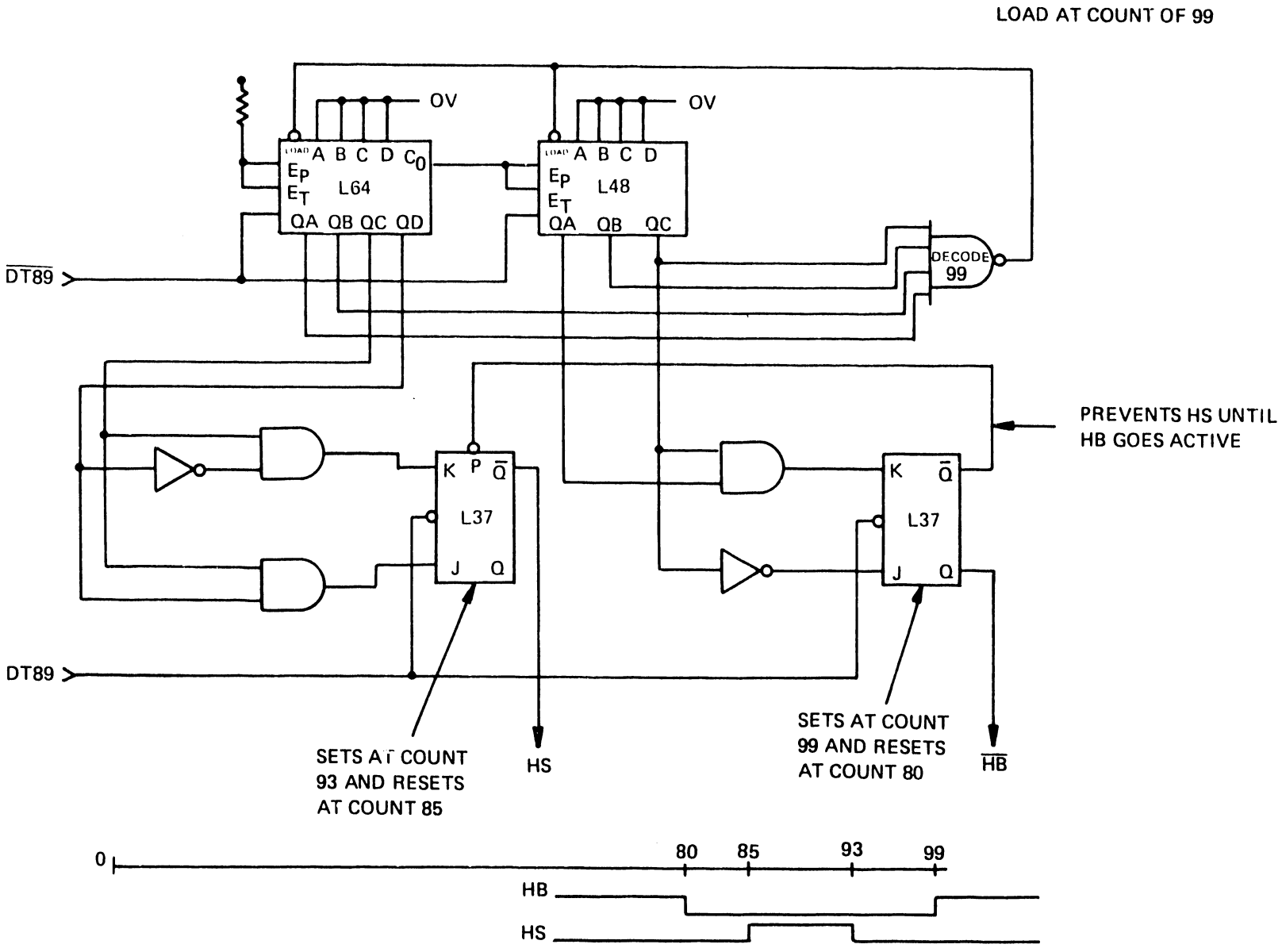


Figure 3-4 Workstation CRT Character Counter-Block Diagram

counts of approximately 2.34 us enables J-K F/F L37-10 output to be reset producing signal HS (HOR. SYNC). See timing diagram for the (column)character counts required to complete the blanking and sync circuitry. Character counts C0-C6 are routed to the multiplexers L47 and L63 for addressing CRT memory.

3.2.5 ROW AND LINE COUNTERS--60 HZ (FIGURE 3-5)

The LINE counter will count 11 scan lines for each row and increment the ROW counter for a total of 24 visible rows (0-23) which adds up to a total of 264 scan lines. An additional scan line count of 21 will occur during the vertical blank and vertical sync period. This time period permits a retrace of the scan to the top of the screen for the start of the next display field.

The total time for a vertical scan plus retrace is 16.666 ms or 60 vertical scans per second. Line counter L33 is a synchronous 4-bit counter that is loaded with zeroes prior to each line count and clocked by the HS after each scan. The line counter outputs QA, QB and QC are used for addressing the character generator PROMS L6 and L7 to sync the writing of the dot matrix on the 8 scan lines used for displaying data. Counter output QD is ANDed with signal BLA to disable character video during a blanking period or during scan line times 8, 9 and 10. The Q outputs are also connected to the inputs of a dual 2-line to 4-line decoder L34. A low output at L34-5 indicates 11 lines have been written and the Row counter is to be incremented. The low is inverted by L54 to enable the ROW counters L49 and L65 which are also clocked by HS. The procedure of counting lines and incrementing rows continues until row counter outputs R3 and R4 (24 ROWS) are ANDed at the input of L51. The output of L51-11 is inverted by L21 and becomes the vertical blanking (VB) signal. Simultaneously, the R0, R1 and R2 row counts (0's) are NORed at gate L92 gating a high at pin 12 which ANDed with VB produces a high at L36-8. This signal ANDed with HS and an inverted LINE 0 (Line counter cleared) produces a

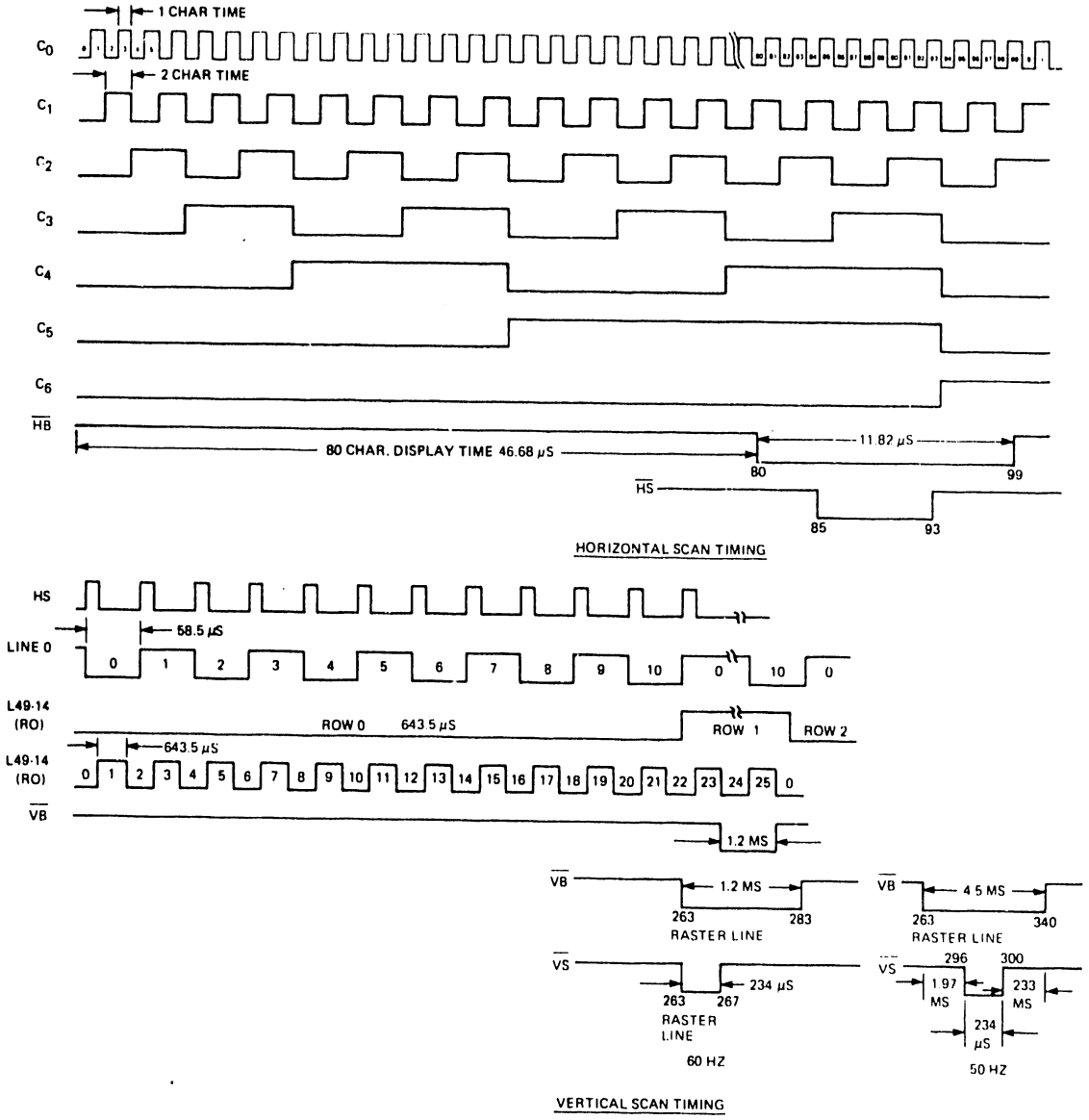


Figure 3-5 Workstation CRT Horizontal and Vertical Scan-Timing Diagram

Vertical Sync VS pulse at the output of F/F L51-6. VB and VS occur at scan line count 264. The LINE count continues for another 21 lines which is the blanking period of 1.2 ms. See Figure 3-4 for details. A reset of the VS F/F occurs on line count 268. A reload of the ROW counter requires a VB and either a R0 or a LINE 9 (ROW 25-SCAN LINE 9).

3.2.6 CRT MEMORY ADDRESSING (FIGURE 3-6)

The CRT screen Character and Control bit memory is made up of 28-2102 R/W static RAM chips that are addressed by row and column selection. Each chip is organized into a 1024 X 1 bit configuration. The memory is organized into two areas, one for characters and the other for display controls bits. Address bits A14 and A15 will select the control bit areas in the 48K to 50K range whereas the character addresses are in the 56K to 58K range requiring the address bit A13. A13 is the controlling address bit for the R/W of two CRT memory areas.

Data and control bits for display are grouped as follows:

1) (DATA= 1-BYTE + PARITY)
2) (CONTROL= 4 BITS + PARITY)

These data are written into CRT memory by the 8080 after accessing the data from WORKSTATION memory. This arrangement requires a multiplexing system which includes L32, L47 and L57. Data read from CRT memory for display is controlled by CHARACTER and ROW counter signals that are multiplexed with the 8080 address bus. The steps for writing display characters and control bits into CRT are as follows:

3.2.6.1 8080 WRITE CRT (FIGURE 3-6)

Address bits A15, A14 and A13 are required for writing characters, A13 is not required for writing control bits. A STATUS word WRITE on the 8080 data bus is NANDed with A14 and A15 at NAND gate L91 producing a low at the input of D-TYPE F/F L79-2. A PHASE 1 and SYNC

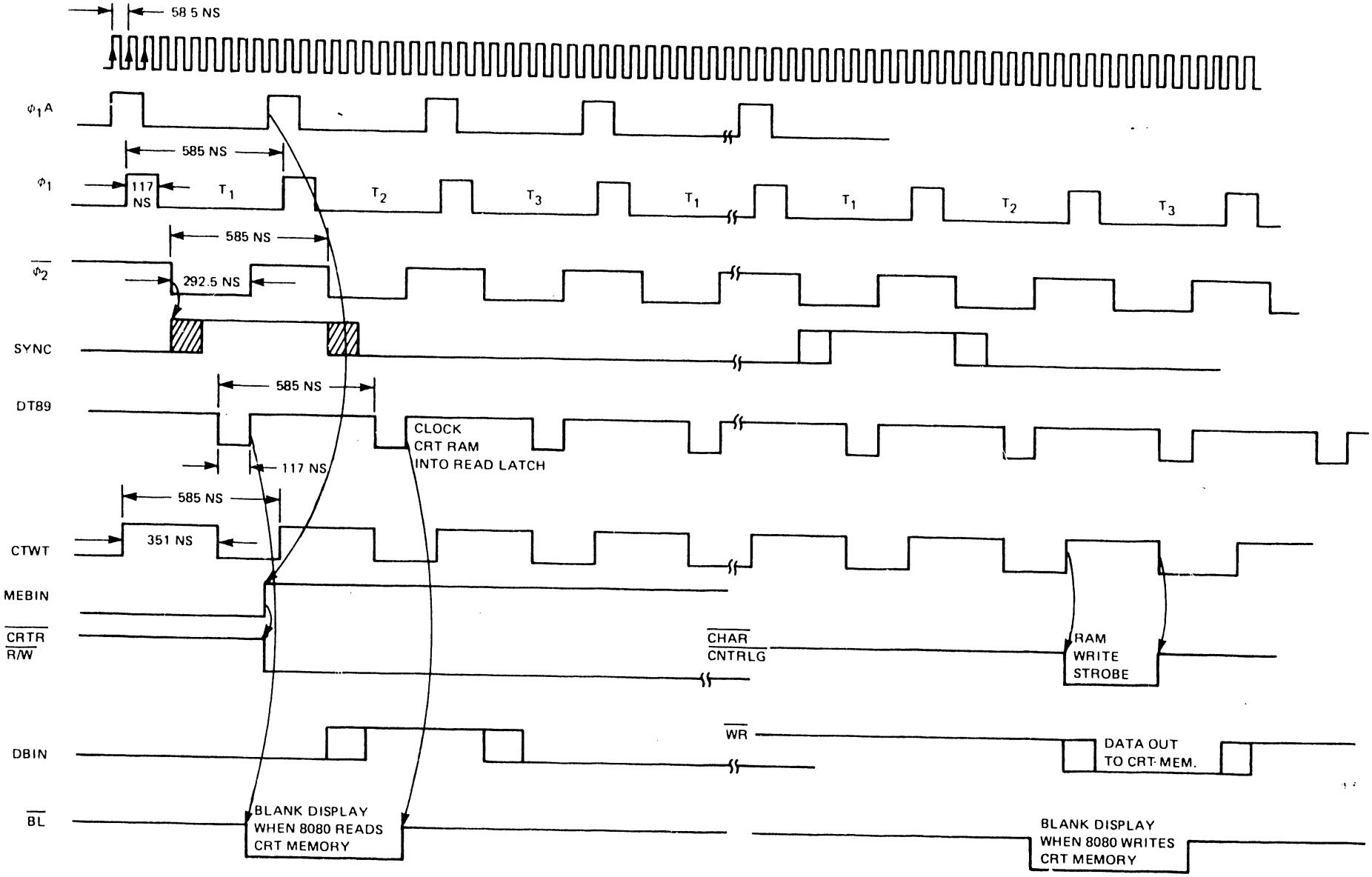


Figure 3-6 Workstation CRT RAM Read/Write (by 8080)-Timing Diagram

clock resets L79 and enables the preset F/F L81 to be reset by a DT89A clock. A low out at L81-5 gates a low at L76-3 (BL) which is used to select the 8080 address bus for CRT memory addressing and also blank any video display. L81-6 is a high at write time and is ANDed with address bit A13 and clock signal CTWT (CRT WRITE) producing signal CHAR enabling a character write of CRT memory. If A13 is inactive, it is inverted by L68 enabling signal CNTRLG which permits a write into the control area of CRT memory. The CE for accessing CRT memory is generated in the CRT address mapping logic. Address mapping is a sectionalizing method to utilize the full capacity of CRT memory.

3.2.6.2 8080 READ CRT MEMORY (FIGURE 3-6)

A READ status word on the 8080 data bus is data bit D7 inverted and NANDed with A15 and A14 and a SYNC pulse at gate L91-8 enabling PHASE 2 clock to reset D-TYPE F/F L77-9 enabling the same BL signal as the write. The 8080 address bus can then access character or control areas. Character data is latched into 4-bit D-TYPE F/F registers L1 and L3 and the parity bit is latched into L70. The L77 dual D-TYPE F/F #2 initiated the READ sequence it also preset #1 which is reset by PHASE 2 but not until the 8080 status word MEBIN has gated a low out of L51-8. Signal CRTR, A13 and R/W enable DT89 clock to gate the character onto the 8080 data bus. Control data when accessed is latched into L2 with its parity latched into L69. The same enabling signals and clock pertain to a read of control data.

3.2.6.3 CRT MEMORY READ FOR DISPLAY

During this operation the 8080 address lines are substituted by the CHARACTER and ROW counter inputs to the MUX chips. Signals CHAR and CNTRLG are disabled in the READ mode so that both character and control locations can be accessed at the same time. As each character count occurs, a line count on one of the 24 rows has also counted. The matrix of these two signals intersect at some location in CRT memory. DT89 is the clock for character and control bits, therefore a

maximum of 80 addresses are read per line. To present this data on the display screen, the data accessed must be presented to the character generator. Character data is latched into two quadruple D-TYPE F/F registers L4 and L5 with the DT89 clock. The latched data is presented to the address inputs of character generator chips L6 and L7 (L7 not loaded). Line counts QA, QB and QC with data bits DOC-D6C access the coded character DOT MATRIX programmed into the L6 PROM. The outputs of the character generator are fed directly to L20 and L35 (2-4 bit parallel load shift registers). The MODE control when high permits parallel loading (max-8 DOT CODE) during DT89 time. Between each DT89 clock there is time for eight 58.5 ns CK clocks. These clocks are used to shift out the dot matrix serially to the character video logic for display. In company with the data are the control bit(s) used for blinking, intensity, etc.

3.2.7 CHARACTER VIDEO AND CRT CONTROL BITS (FIGURE 3-7)

The characters displayed on the screen are really 12 bits in length. Each character addressed has its associated control bits(s) addressed also. The four control bits are represented as data and treated separately but timed to perform with its own character. The control bits are as follows:

Data Bit	Name
D4S	UNDERLINE (twelve bit)
D5S	CURSOR (eleven bit)
D6S	BLINK (ten bit)
D7S	INTENSITY (nine bit)

Because the 8080 can only address one byte (8 bits) at a time, it is necessary to have a different address base to control these four bits. CRT CONTROL memory is accessed similar to CRT CHARACTER memory. The memory is organized as partially loaded addresses from 48K up to 56K. The high order address byte is used for ROW selection while the low order address points to the column selection for CRT

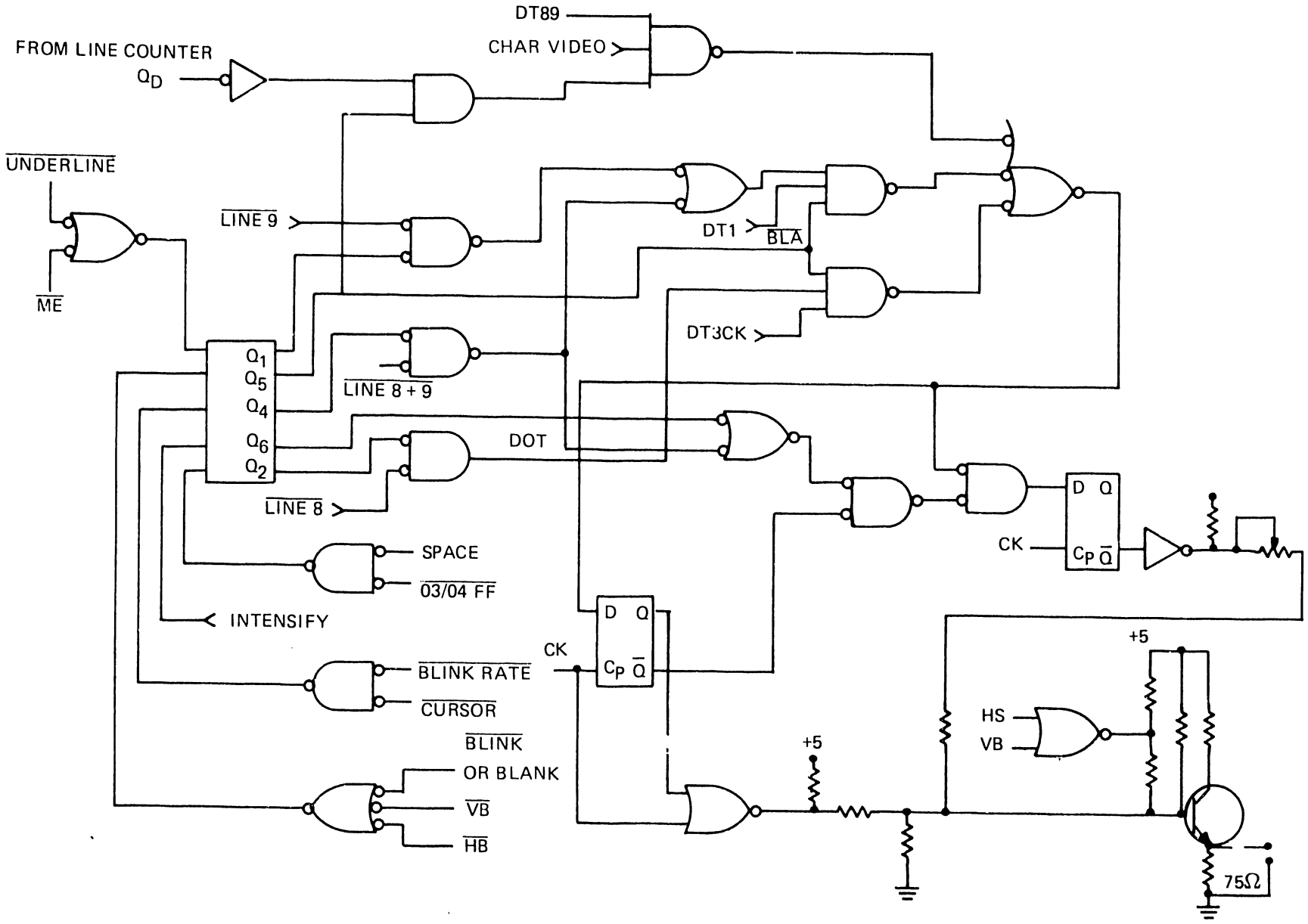


Figure 3-7 Workstation CRT Video-Block Diagram

control bits. During a character display time the associated control bit will be latched into a D-TYPE F/F L8 or L10 at DT89 time. The blanking signal BL is introduced into the latch for inhibiting video during 8080 R/W operations. BL is latched into CRT control register L8 at the same time the character is latched into L4 and L5 by*DT89 clock. L8-10 goes low producing a low at L36-6 and L80-12 which is latched into L107 at DT89 time, generating a low out at L107-12. This low signal*BLA conditions the logic for a high output at gates L66-6, L66-8 and L116-8 generating a high at L53-8 setting D-TYPE F/F L70A-5 output high. This high ORed with CK at gate L24A-1 forces the base of transistor Q1 to go low blanking all video signals. Without signal BLA*enabled, the following controls can be activated.

1) CHAR VIDEO at L66-6 until inhibited by line count QD.
2) CURSOR or UNDERLINE display at L66-8 activated during line scan 8 and 9 or line 9 respectively.
3) SPACE DOTS displayed at DT3CK time from L116-8.

3.2.7.1 CHARACTER VIDEO BITS

CHAR VIDEO bits (dots) are clocked out of the character shift register to L66-1 where they are ANDed with DT89A and the output of L106-8 producing a low until signal QD is active after the eighth display line is on the screen. The CURSOR display bit when latched is ORed at L23 with a monostable oscillator that produces a BLINK rate for the cursor (80/min. approx.). The blinking cursor is latched into L107 and presented to L105-4. This signal is ORed with the LINE 8 and 9 output of L76-6 to generate a low at L116-input pins 13 and 2 producing a high out that is ANDed with DT1 and BLA to gate a low at the output of L66-8.

3.2.7.2 UNDERLINE CONTROL BIT

UNDERLINE control bit D4S is latched in L10 and routed to L36-1 via a jumper. The UNDERLINE bit can also be presented to L36-1 by bit 7 of CRT CHARACTER memory when loaded into the CRT CHARACTER register

L4 via a jumper. Another OR condition exists at the input of L36-2 for indicating a ME (Memory Error). The input to L116-1 serves as dual purpose of displaying an underscore or a full screen of LINE 9 scans indicating a memory error.

3.2.7.3 INTENSITY CONTROL BIT

INTENSITY control bit D7S is latched into L8 and then into L107. The output at L107-15 is active low and ANDed with an active low CURSOR gating a low at the output of L94-6. With L70A reset, pin 6 is high presenting a low to L70A-12 gating a low output from L24A-10 which, when applied to the base circuitry of Q1 video amplifier, highlights the cursor. The DOT-SPACE display is initiated by the SPACE DECODER L22-8 when no character is loaded into the CRT CHARACTER REGISTER. This low output is loaded into latch L107. A low output at L107-5 is ORed with a DOT/NO DOT output from the L10-6 F/F. OUT 3 presets L10 for a DOT, an OUT 4 clears for NO DOT. DOT ANDed with DT3CK and BLA will enable the DOT display.

3.2.8 KEYBOARD CONTROL LOGIC

KEYBOARD entry to the WORKSTATION 8080 CPU is accomplished by entering fixed keyboard alphanumeric codes and other type-writer character codes into latching registers via keyboard data lines K0-K6. Whenever a key is depressed on the keyboard, an interrupt is generated by the logic forcing a program jump to TRAP 0 (address 0000). A key strobe (KS) signal accompanies each key stroke sent from the keyboard to the CRT keyboard control logic triggering section 1 of one-shot multivibrator L83-7 producing a 500 ns LOAD STROBE (LS) pulse used for clocking keyboard data K0-K6 into latching registers L88 and L89. After LS times out, it triggers section 2 of L83 pin 10 disabling L82 (section 1) by gating L52-6 high. The trailing edge of KS (100 us) triggers one-shot multivibrator L82 (section 2) by gating L97-8 low producing signal OUTS at L82-10 which times out in 10 ms

after clocking D-TYPE F/F L118. Section 2 of L83 times out in 285 ms enabling L52-6 to trigger section 1 of L82 for 100 ms producing a low at L52-11 which inhibits another key stroke for an extended period of 100 ms.

An interrupt from L118-5 to the 8080 INT input L112-14 will start the interrupt sequence. The 8080 will issue an Interrupt Acknowledge (INTA) status word at the start of the next MCT which is clocked into the status register L86 at SYNC and PHASE 1A time. At DBIN time a RESTART instruction with a 3-bit interrupt address embedded in it will be jammed onto the data bus from data buffer L84 by gating a low from L117-11 which also clears the interrupt F/F L118. D-TYPE F/F L69 was previously preset by MASTER RESET (MR) as a result of the key stroke interrupt setting L69-6 signal DAX high and inhibiting any more key strokes for 10 ms. DAX is used to inhibit an X axis priority encoder mounted on the 7229 keyboard. Signals LS, INT and OUTS when timed out or reset, provide a clock for resetting L69 with a positive going signal from L80-6. An INO command is issued by the 8080 consisting of address bits A0-A2, DBIN and INP all ANDed together to gate an active low output from L78-8 enabling the key stroke data onto the data bus and into the processors accumulator.

AET is an automatic enabling signal input from the keyboard for repeat keys usch as cursor directional keys and space bar. AET enables the input at L97-10 for continuous key strobes and key stroke interrupts providing cursor movement vertically at a rate of 15 characters per second, and horizontal movement at 30 characters per second. The two speed controls for repeat keys is decoded by the BCD to decimal decoder L111 from K0-K2 key codes. The output from the decoder either grounds the +5V input to the NAND gate L97 or permits it to remain high. If the resistor R37 is grounded, the repeat rate will be 15; if not, resistors R37 and R36 will be paralleled to produce a repeat rate of 30 characters per minute. Other repeat keys are PERIOD, BACKSPACE and UNDERSCORE.

SHIFT and LOCK keys on the keyboard provide for uppercase character display by controlling the MSB (Bit 8) of each character code. The SHIFT key is generally used for single characters whereas the LOCK provides upper case characters until released. Shift register L98 is a D-TYPE F/F that can be clocked by the SHIFT key after the upper case code has been entered. A low input from the shift key at L76-9 causes a low output at L76-8 illuminating the shift lamp on the keyboard and enabling the 8th bit for UC. Release of the shift key causes the F/F to reset producing a high at L76-8 and inhibiting any more UC characters. The LOCK key, when locked, presets the F/F presenting a low at bit 8 continuously during all key strokes which are UC until released.

3.2.9 OUT COMMANDS (TABLE 3-1)

Presently only five OUT commands are being untilized on CRT CPU board 7225. They are as follows:

OUT 0--The clicker is an audible sound that can be adjusted on the rear of the WORKSTATION by the operator for loudness. The clocker sound is issued by the software for each key stroke as an acceptable key code.

OUT 1--Operates a buzzer which will alert the operator of some illegal action. A rear control is also available for adjusting the loudness of the buzzer.

OUT 2--Used for wide platen option (SEE 7235).

OUT 3--Generates DOTS for character spaces.

OUT 4--Sets all DOTS to spaces. (The use of DOTS is to help the operator distinguish spaces from TAB zones when editing).

3.2.10 IN COMMAND (TABLE 3-1)

IN 00--Used to read the pending key stroke that is latched in the character buffer into the 8080 accumulator.

TABLE 3-1

INPUT/OUTPUT COMMANDS - WORKSTATION

CRT CPU COMMAND SIGNAL	SIGNAL DESCRIPTION	
Trap 0	Restart and presence of key	
Out 00	sound clicker	
Out 01	sound buzzer	
Out 02	wide platen setting	
Out 03	set spaces to dots	
Out 04	set dots to spaces	
Out 05	count from move	(Math pack option only)
Out 06	select CRT character set 1	(dual prom option)
Out 07	select CRT character set 2	(dual prom option)
Out 09	Compare	(Math pack option only)
Out 10	Move +	(Math pack option only)
Out 11	Move -	(Math pack option only)
Out 12	DECIMAL ADD	(Math pack option only)
Out 13	DECIMAL SUBTRACT	(Math pack option only)
Out 14	DECIMAL SHIFT +	(Math pack option only)
Out 15	DECIMAL SHIFT -	(Math pack option only)
In 00	Read pending key	

3.2.11 PARITY CHECKER AND GENERATOR

DP8out is the parity bit generated by L85 parity generator representing ODD parity during and 8080 write into CRT memory. This parity is stored with the byte of data. Data accessed from WORK-STATION memory via the 8080 data bus and written into CRT memory also was stored with a parity bit called DP8in when accessed. During the transfer of each data byte, a comparison of parity bits is performed on the DATA LINK 7227 using an EXCLUSIVE OR gate to monitor the correct parity from memory to the CRT. This parity compare (PARCOMP) is monitored by L117-8, the input gate for the PARITY CHECK circuit. If an error occurs, a high input to D-TYPE F/F L118 will cause pin 8 to go low indicating a memory error (ME). A high at L118-9 will enable L81 to be clocked by PHASE 2 producing a Bad Parity status bit (BP) at pin 9. L81-8 generates a Memory Error (MER) that forces the READY line low and the 8080 into a WAIT state until the Master Reset clears all registers and returns the program to location 0000. The ME also fills the display screen with LINE 9's.

3.2.12 POWER UP F/F

A power up F/F L70 is controlled by a signal WTR from the power regulator board 7067 in the workstation and RESET or RESTART inputs from a switch o software. In a preset state, the Not Running (NR) status bit at L97-6 would be high and inhibit any operations. L70 can be cleared by enabling L55-3 with a RES or RESTART.

3.2.13 CRT CONTROL BOARD--7235 WITH WIDE PLATEN OPTION

The CRT control board 7235 includes the wide platen option (HORIZONTAL SCROLL) that permits the operator to increase the number of charactecters per row from a maximum of 80 to a maximum of 158. The increased number of characters displayed requires an increased capacity for CRT memory therefore doubling the memory size for an approximate doubling of the display area. A change of memory chips on

7235 using TMS 4050 has resulted in a 4K memory with control bits. Except for additional OUT commands, the differences between the 7225 and 7235 boards differ only as explained above.

3.2.14 HORIZONTAL SCROLL

The extended horizontal screen will always appear as the normal screen when observed on the display, however, in actuality it will overlap the original screen by as much as 79 columns or as little as 2 columns. The operator selects the desired number of columns when creating a document which can be extended to a maximum of 158 (two less characters than two full screens). The operator is required to extend the FORMAT line by touching the FORMAT key and moving the cursor across the format line until it reaches the 80th character position. From this position, the screen will automatically scroll to the left one character space for each cursor move to the right. When the operator reaches the desired character limit, the RETURN key is touched, followed by the EXECUTE key. The number of characters desired beyond the 80th will be stored in a memory location that will be accessed each time the character count exceeds 80. An OUTPUT WRITE status word (WO) is issued from the STATUS REGISTER L85 and NORed with a SYNC clock generating an enable at L115-4. This signal gates the valude of the starting column for the scroll (STORED IN MEMORY) out of the accumulator of the 8080 via data buffers L99 and L102 into the column counter latches L1 and L5 by an OUT2 command clock. This value is the starting column for the left margin of the CRT display. The CRT will then display the next 80 characters from that starting column. If OUT2 sent a value of 18 to the column counter, then the 80th character from the left would be 97. See WANG'S WP OPERATOR'S GUIDE #700-4044B for operating details using WIDE PLATEN OPTION.

The character counter (COLUMN COUNTER) requires additional logic as compared to the 7225 board because the Horizontal Scroll Option requires software inputs for character counts. L15 and L20 are the added counters producing an extra column count (COL7) for the extended

screen. ROW counts (R0-R4) and the character "99" line count are used to control the column counter. A BCD to DECIMAL decoder L52 receives the row count from the row counters L46 and L62. The combined logic of the decoder and character count "99" generate a clear pulse for blanking ROW 0 and ROW 23 of the scroll display. The 0 through 79 character display screen for ROW 0 and ROW 23 will remain intact for all scroll work. The LOAD pulse for the column counters L15 and L20 after each scan line is enabled by the decoder inputs to L46 generating a low at pin 3 permitting character count "99" to reset the count to the selected left margin. The L46-3 enable is low for all scan lines inclusive of ROW 1 through ROW 22.

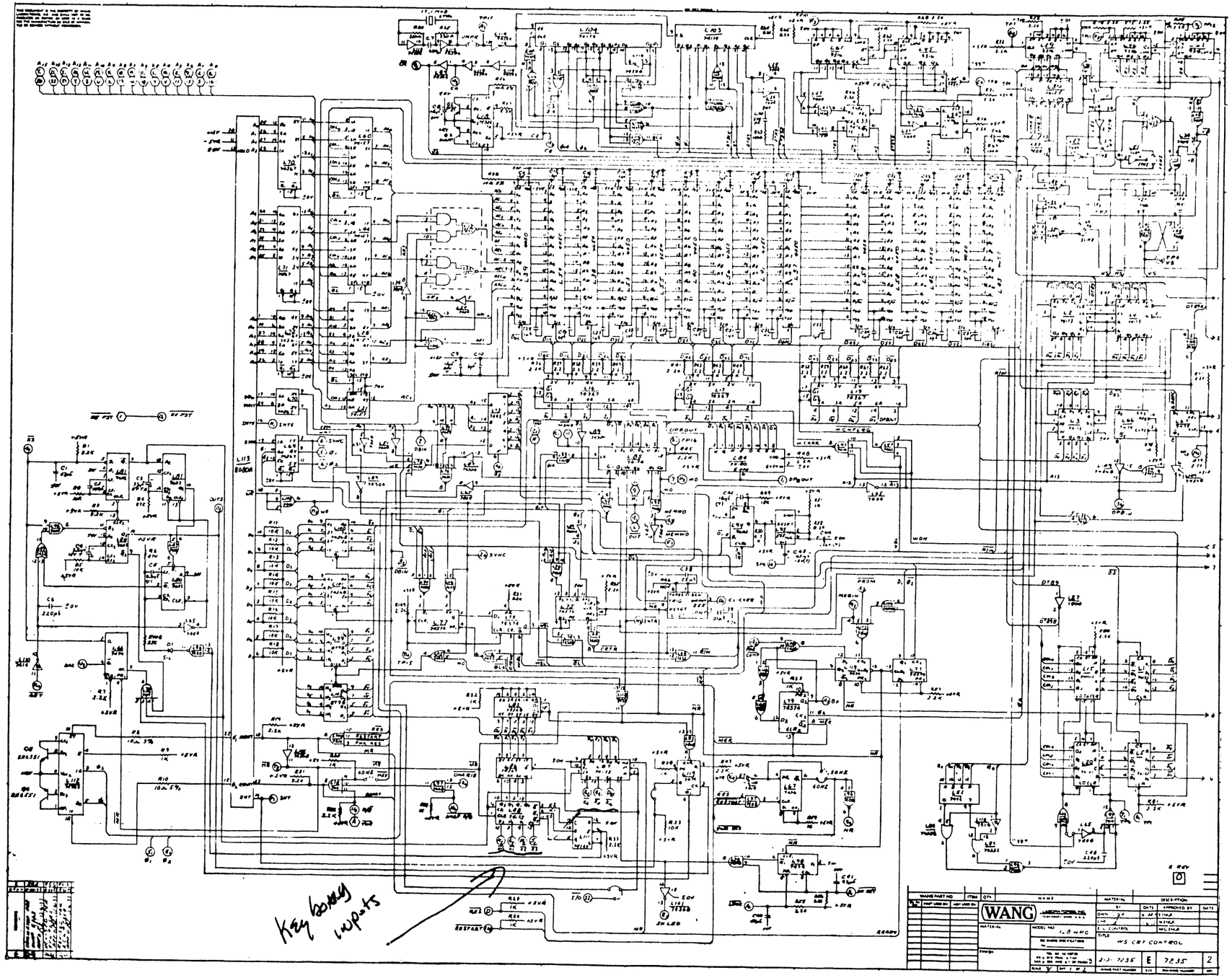


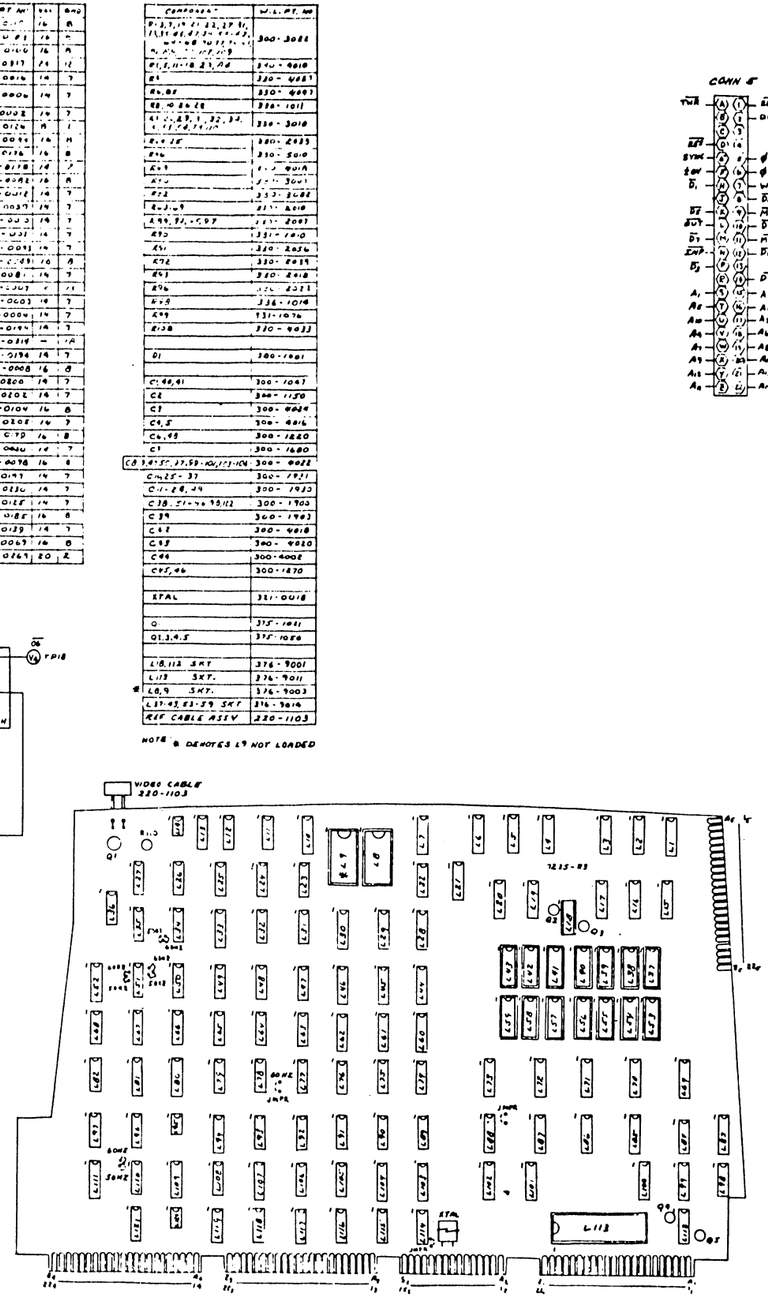
Figure 3-8 (7235) Workstation CRT Control-Schematic Illustration — Sheet 3

3-23 & 3-24
S22 3-4A & 3-4B

LOCATION	WIRE WRAP NO.	SIZE	GND
L1, 2, 88	376-0001	16	8
L2, 3, 4, 87	376-0002	16	8
L6, 7, 10	376-0006	16	8
L8,	377-0317	14	12
L11, 12	376-0016	16	7
L13, 64, 65, 98, 114, 181	376-0004	16	7
L15, 99, 96, 116	376-0002	16	7
L19, 100, 102	376-0124	16	8
L21, 22, 23, 24, 25, 26, 27, 182	376-0014	16	7
L28, 29, 30, 31, 32, 33, 34, 183	376-0126	16	8
L118, 119	376-0118	16	7
L120, 121, 122, 123	376-0082	16	8
L124	376-0012	16	7
L125, 126	376-0003	16	7
L127, 128, 129, 130	376-0021	16	7
L131, 132, 133, 134	376-0009	16	7
L135	376-0081	16	8
L32, 93, 97	376-0008	16	7
L38	376-0007	16	7
L39, 40, 104, 105, 113	376-0003	16	7
L35, 42, 74, 75	376-0004	16	7
L36, 115	376-0104	16	7
L41, 42, 43, 44, 59	377-0319	14	14
L52, 78	376-0194	16	7
L54, 73	376-0008	16	8
L76, 94	376-0820	16	7
L77, 78, 79	376-0202	16	7
L80, 81, 96	376-0104	16	8
L82, 108	376-0208	16	7
L83, 100, 101, 109	376-0178	16	8
L84	376-0820	16	7
L85, 103, 104, 107	376-0078	16	8
L89, 116	376-0177	16	7
L92	376-0214	16	7
L91	376-0128	16	7
L98, 106	376-0182	16	8
L110	376-0129	16	7
L111	376-0069	16	8
L113	377-0264	20	2

CONNECTOR	W.L. PT. NO.
P1,2,3,4,11,12,13,14,15,16,17,18,19,20,21,22,23,24	300-3088
P5,6,7,8,9,10	300-3089
P25,26,27,28,29,30	300-4018
P1	320-4087
P4,5	320-4007
P8,10,26,28	320-1011
P2,3,6,7,9,11,12,22,24,27,29,30	320-3018
P1,2,5	320-2023
P4	320-5010
P6	320-5009
P10	320-5011
P12	320-2022
P13,14	321-4018
P15,16,17,18	321-2007
P20	321-1010
P21	320-2024
P22	320-2019
P23	320-2018
P24	321-2021
P4-9	336-1014
P29	131-1076
P25B	320-4033
P1	300-1001
C1,40,41	300-1047
C2	300-1150
C3	300-0824
C4,5	300-4016
C6,45	300-1220
C7	300-1680
C8,9,42,43,44,47,48,49,50,51,52,53,54	300-4022
C10,25-33	300-1731
C11-24,46	300-1933
C34,35,36,37,38,39,40,41	300-1903
C39	300-1943
C42	300-4018
C43	300-4020
C44	300-4002
C45,46	300-1870
XTAL	331-0018
Q	315-1041
Q1,3,4,5	315-1026
L18,112 SKT	376-9001
L113 SKT.	376-9011
L8,9 SKT.	376-9003
L37-43,63-69 SKT	376-9016
RIF CABLE ASSY	220-1103

NOTE * DENOTES L9 NOT LOADED



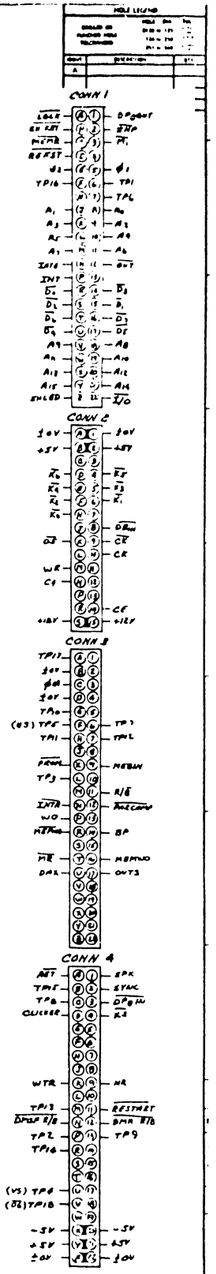


Figure 3-8 (7235) Workstation CRT Control-Schematic Illustration — Sheet 4

3.3 WORK STATION MEMORY #1---7226

3.3.1 GENERAL DESCRIPTION (Figure 3-9)

Work Station (WS) Memory has a capacity of 16K bytes. The memory is divided into four (4) Banks of 4K requiring individual selection and addressing capabilities. This memory can be accessed by the Workstation 8080 data bus during internal processing and during DMA operations it can be accessed by the Master CPU utilizing the DMA address and data busses via the workstation Data Link. The following discussion will include the logical requirements for a Read and Write via the 8080 address and data bus, and a Read and Write utilizing the DMA address and data bus.

3.3.2 MEMORY---8080 WRITE

The 8080 address bus requires twelve bits A0-A11 for addressing 4K of data from any one of four Banks. Address bits A12-A15 are used for selecting the desired Bank and the R/W operations.

The DMA select input for address Selector/Multiplexers L67, L12, L24 and L38 is low for 8080 addressing. Address bits A0-A11 are enabled to each memory Bank through Tri-State Buffers L13 and L25 by signal refresh (REF) which is low for a period of 567 ns every 585 ns.

The most significant address bits A12-A15 are enabled to the inputs of the Memory Bank Select Decoder L49 via mutiplexer L67. A12 and A13 decode into four (4) output signals that are individually applied to the four sections of NAND gates L57. Signals A14 and A15 are inactive for 8080 R/W operations. The four L57 NAND gates are used as OR gates to permit chip enable (CE) for memory refresh as well as 8080 and DMA (R/W) operations.

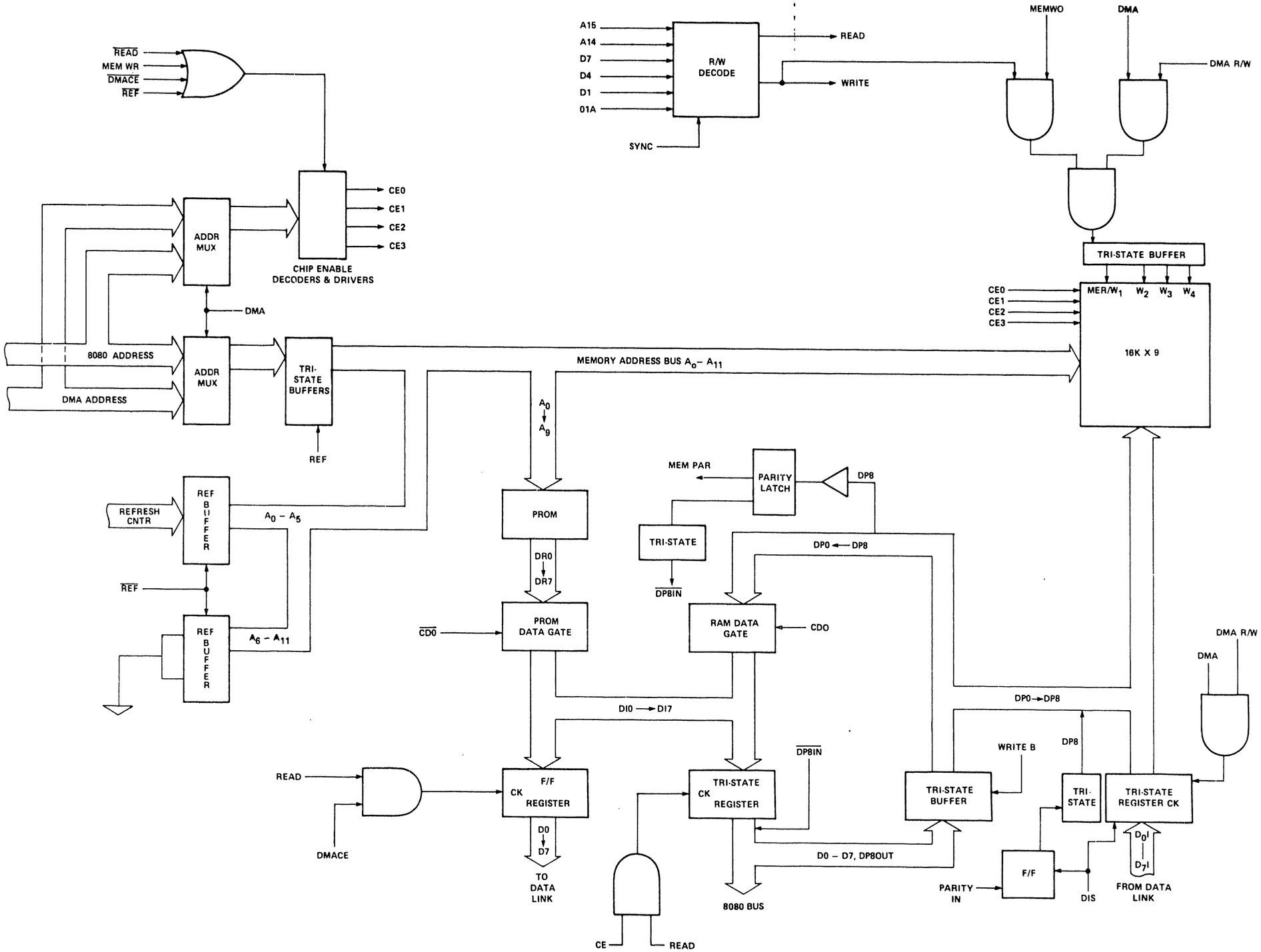


Figure 3-9 Workstation Memory-Block Diagram 7226

A CE clock from the timing circuits of the CRT CPU board is used to enable each section of Drivers L11 and L35 to activate one of the four CE0-CE3 (Chip Enable) signals that select the desired Bank for a 8080 Write. A decode of 0 selects CE0 with a jumper that is connected to L57-13 from L49-1 grounding the pull-up while active.

The remaining enables required to perform an 8080 WRITE start with the 8080 issuing a memory (WRITE) Status Word onto the Data bus*D0-D7. The WRITE Status Word bits D1 and D4 are routed directly to NAND gate L59 where the SYNC clock and A14A15 signals are combined to gate a low input to L64 F/F which resets with a PHASE 1A clock. The reset provides a high input to L72-2 Write F/F which is set by the next PHASE 1A clock. There are two outputs at L72-5 (8080 MEM WRITE) and L72-6 (WRITE B). The L72-5 output enables the AND/NOR gate L74 with a MEMWO (Memory Write) signal from the status register of the CRT/CPU board 7225. This produces the memory R/W strobes (MER/W1, 2, 3, and 4) at the output of TRI-STATE Buffer L23.

The L72-6 output enables the data bytes onto the memory I/O bus via data input buffers L68 and L69. *WRITE B also enables a low to the D input of the Bank Select Decoder L49.

3.3.3 MEMORY---8080 READ

The 8080 READ of Workstation memory follows the same procedure as for a WRITE when addressing the desired BANK and location in the Bank. The actual read of data requires a Status Word bit D7 issued from the 8080 that is NANDed with SYNC and A14A15 gating a low from L65-12 resetting the #1 section of L64 F/F.

L64-5 enables a low*READ to AND gate L73 which produces a low to the D input of the Bank Select Decoder (NOT PRESENTLY DECODED). L64-6 output is high enabling L66-8 to go low when CE is active. On the trailing edge of CE the data from memory will be clocked into output

registers L60 and L61 including the parity bit that is clocked from L54-8 into buffer L53. A14A15 is NANDed with MEBIN (Memory Byte In) from the CRT/CPU status register at L66-11 to enable the accessed data onto the 8080 bus.

The memory strobes are always enabled for an 8080 READ. A pull-up resistor is presently used to make signal*CD0 high inhibiting the TEST PROM output at TRI-STATE buffers L52 and L53 (NO PROM INSTALLED). Signal CD0 at L58-12 is always low enabling memory output buffers L55 and L56 to gate data onto the 8080 or DMA bus. Because CD0 is always low the preset of L72 (#2 F/F) is inhibited from producing the signal*PROM which is used to clock the memory error F/F on the CRT.

3.3.4 MEMORY---DMA WRITE

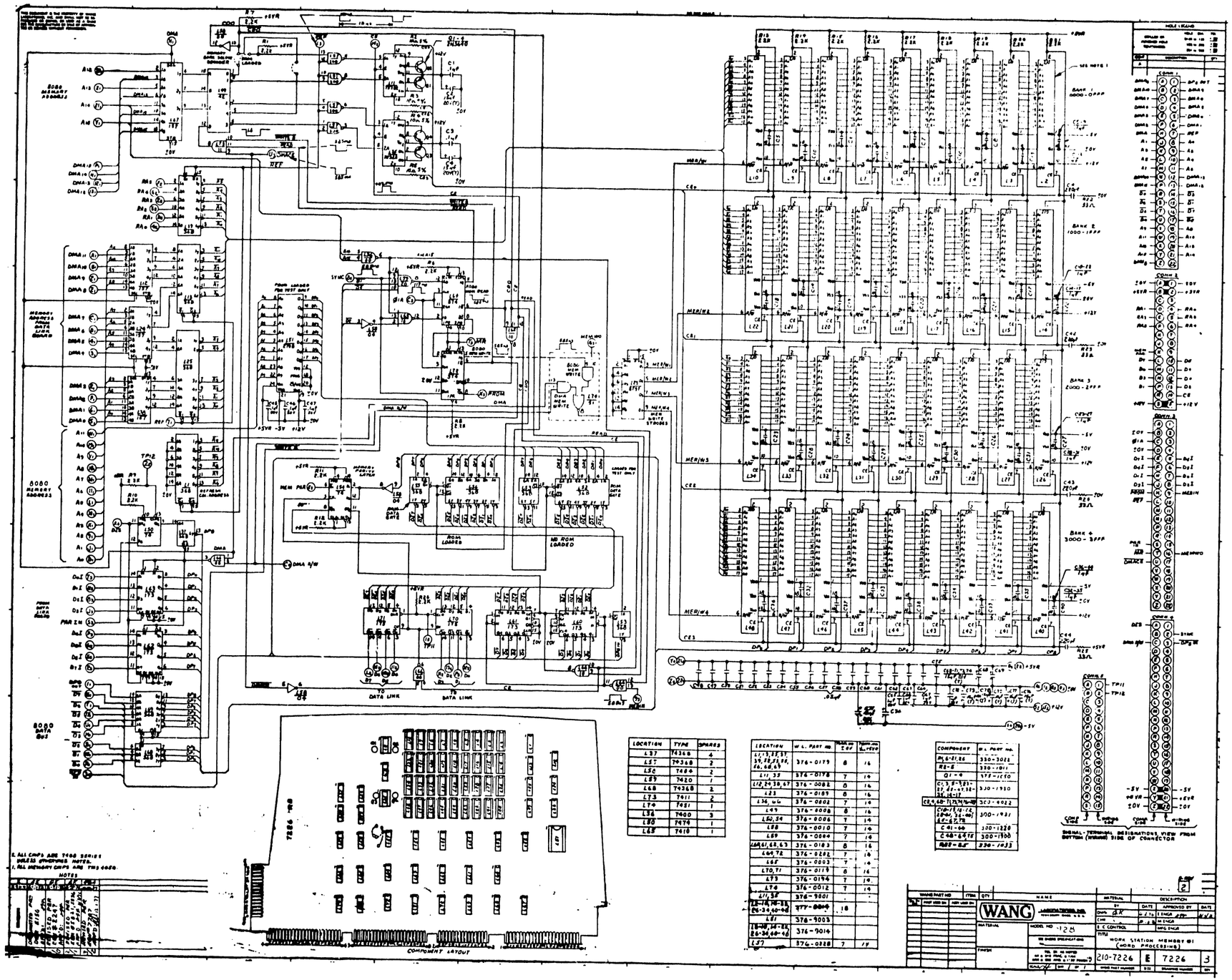
The DMA WRITE operation is initiated when the Work Station Data Link Board 7227 receives the HEADER/INSTRUCTION byte from the Master CPU indicating a 1-BYTE or 256-BYTE WRITE.

The signal DMA R/W is active high (WRITE) when the instruction is clocked into the data link Instruction register. DMA R/W enables the DI (Data In) bus from the DATA LINK at L66-2 and the AND/OR gate L74-1 for activating the four memory write strobes.

Signal DMA is generated on the Data Link at T2 time from the byte timing register which also causes*DMACE to go active. Signal DMA selects the DMA address from multiplexers L67, L12, L24 and L38; gates data into the TRI-STATE D-TYPE registers L62 and L63 from the data link and turns ON the four memory write strobes from L23. *DMACE inhibits the D input to the L49 decoder during the DMA WRITE. The only active signal for a DMA write of 256 bytes of data into memory after the first byte is the CE.

3.3.5 MEMORY---DMA READ

The DMA READ of WS memory is initiated by 1-BYTE or 256-BYTE READ Header/Instruction word issued by the master to the slave (WS) data link and decoded into control signals DMA R/W and DMA. The only difference from the WRITE operation is that DMA R/W is a low (see Header Byte data in 7227 discussion). Signal DMA R/W being low inhibits the DI registers L62 and L63 and the Memory Write Strobes at L23. The only active signals required for a DMA Read are the DMA,*DMACE and CE. DMA selects the DMA address bus, CE provides the CHIP ENABLE for accessing data from memory and*DMACE inhibits the D input to the decoder and enables L66-6 to go low allowing data to be transferred to the data link multiplexers and S/P registers via data lines D0-D7.



LOCATION	TYPE	SPARES
L37	74368	4
L57	74368	2
L5c	7486	2
L89	7420	1
L68	74368	2
L73	7811	2
L70	7451	1
L31	7400	3
L80	7474	1
L69	7410	1

LOCATION	W.L. PART NO.	TRACE ON COMP.	TRACE ON SOLDER
L1/3,33,37, 39,43,53,54, 56,68,69	376-0179	8	16
L11, 35	376-0178	7	14
L12,24,38,67	376-0082	8	16
L23	376-0187	8	16
L36, 44	376-0002	7	14
L49	376-0008	8	16
L50,34	376-0006	7	14
L58	376-0010	7	14
L59	376-0009	7	14
L60,61,62,63	376-0183	8	16
L64,72	376-0282	7	14
L67	376-0003	7	14
L70,71	376-0179	8	16
L73	376-0194	7	14
L74	376-0012	7	14
L11,58	376-9001	-	-
L2-L10, 14-L19, 26-34,40-48	377-0049	18	
L51	376-9003		
L15-L18, 14-L23, 26-30,40-48	376-9014		
L27	376-0228	7	14

COMPONENT	W.L. PART NO.
R1,6-21,24	330-3021
R2-5	330-1011
Q1-6	378-1150
C1,3-13,21-27,32-42,44-52,54-57,59-67,69-78	330-1930
C2,4,43-53,74,76-80	300-4022
C14-17,19-20, 28-31, 58-68	370-1931
C18,72	300-1220
C1-6,71	330-1220
C68-69,73	300-1900
R22-27	330-7933

NOTES
1. ALL CHIPS ARE 7400 SERIES UNLESS OTHERWISE NOTED.
2. ALL MEMORY CHIPS ARE TMS 4060.

SIGNAL - TERMINAL DESIGNATIONS VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

Figure 3-10 Workstation Memory-Schematic Illustration

3.4 WORKSTATION DATA LINK---7227

3.4.1 GENERAL DESCRIPTION (Figures 3-11 and 3-12)

The only interface the WORKSTATION has with the MASTER CPU is a coaxial cable that connects between the DATA LINK of the master to the DATA LINK of the slave workstation. DMA data transfers are asynchronous and bidirectional at a rate of 4.28 megahertz. Data is transferred by byte serially over the link and reformatted to parallel within the data link of each unit. Prior to transferring data using the data link, a STATUS Header/Instruction byte from the master precedes any data transfers. The Workstation data link can perform the following command transfers.

1) RESTART
2) STATUS
3) 1-BYTE READ
4) 1-BYTE WRITE
5) 256-BYTE READ
6) 256-BYTE WRITE

3.4.2 HEADER BYTE (TABLE 3-2)

One of the above listed transfer functions is issued to the selected slave after the STATUS of the slave has been checked. Each function has its own Header/Instruction byte, and in the case of the STATUS and RESTART the only byte issued. The other four functions involve data transfers, however, the Header/Instruction byte will be the messenger of what is to be done. The Header/Instruction byte, address bytes and data bytes are transferred in 11 bit bytes. The three extra bits are a START bit, STOP bit and PARITY. All bytes are transferred over the link with the START bit first and the three most significant bits D5-D7 next which contain the HEADER code 101. If this code is in error the operation is aborted. The instruction portion of the byte is contained in the five least significant bits D0-D4.

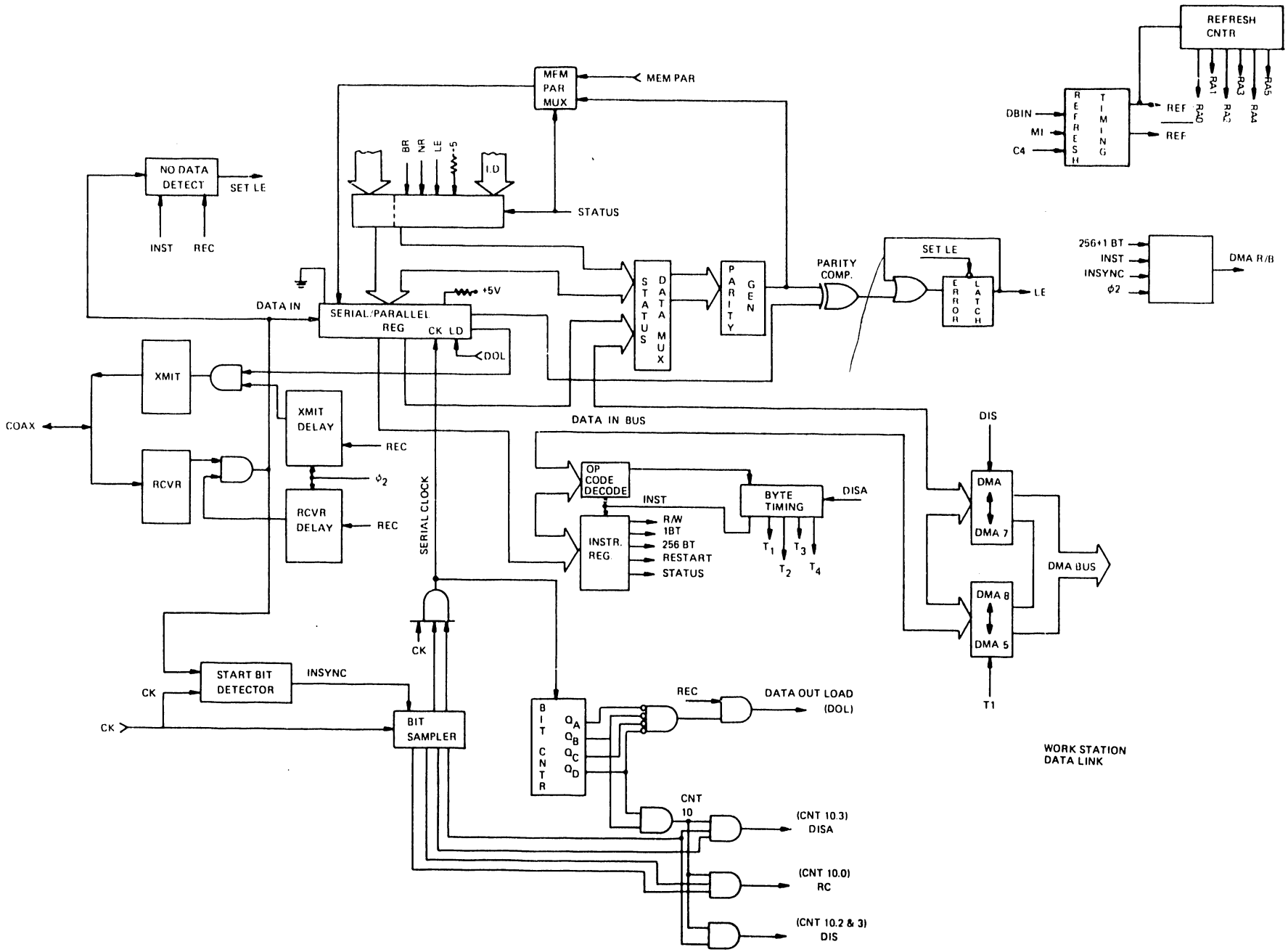
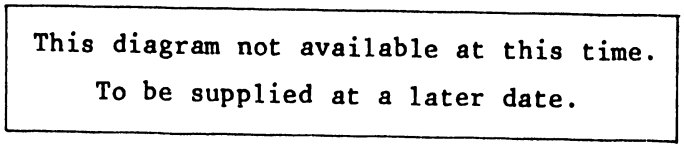


Figure 3-11 Workstation Data Link-Block Diagram 1227



Figuro 3-12 Workstation Data Link-Timing Diagram

TABLE 3-2

HEADER INSTRUCTION BYTE DESCRIPTION

HEADER/INSTRUCTION BYTE

Time	0	MSB							LSB		
BITS	1	2	3	4	5	6	7	8	9	10	11
	START	D7	D6	D5	D4	D3	D2	D1	D0	PARITY	STOP
	1 (SYNC BIT)	1	0	1	X	X	X	X	X	X	0

TIME 0 HEADER INSTRUCTION

D7	D6	D5	D4	D3	D2	D1	D0	PARITY	COMMAND
1	0	1	1	0	0	0	0	1	STATUS
1	0	1	0	1	0	0	0	1	RESTART
1	0	1	0	0	1	0	0	1	256 BYTE READ
1	0	1	0	0	1	0	1	0	256 BYTE WRITE
1	0	1	0	0	0	1	0	1	1-BYTE READ
1	0	1	0	0	0	1	1	0	1-BYTE WRITE

	MASTER		SLAVE (CRT OR PRINTER)
1.	STATUS		
		HEADER BYTE	
		STATUS BYTE	
2.	RESTART	HEADER BYTE	CLEARS DATA LINK
3.	1-BYTE READ	HEADER BYTE	
		LOW ORDER ADDRESS	
		HIGH ORDER ADDRESS	
	1-BYTE		DATA
4.	1-BYTE WRITE	HEADER BYTE	
		LOW ORDER ADDRESS	
		HIGH ORDER ADDRESS	
	DATA		1-BYTE
5.	256 BYTE READ	HEADER BYTE	
		DMA HIGH ORDER ADDRESS	
		DMA LOW ORDER ADDRESS = 0000	
			STARTING ADDRESS
	256 BYTES		DATA
6.	256 BYTE WRITE	HEADER BYTE	
		DMA HIGH ORDER ADDRESS	
		DMA LOW ORDER ADDRESS = 0000	
			STARTING ADDRESS
	DATA		256 BYTES

The above listed header bytes in Table 3-2 are decoded in the Workstation data link and processed as described below.

3.4.3 HEADER/INSTRUCTION BYTE AND START BIT DETECTOR

Prior to using the workstation data link for transferring data, the status of the link must be checked. The procedure used to process the status and other commands will be discussed after the method of processing the HEADER/INSTRUCTION byte in the data link is covered. The data link is in the receive mode (REC) when idle.

When the REC mode first goes active the data link will not accept any data until the receive delay of 7 us has timed out. Prior to the REC mode L27 (9316 counter) was loaded with a deficit count of 12 and L16 F/F was cleared enabling the counter to be incremented with PHASE 2 clocks. A full counter after 12 clocks (7 us) will produce a carry out (CO) that conditions the L16-2 D-type F/F to set on the trailing edge of the PHASE 2 clock. A low at L16-6 (TCL) inhibits anymore clocks, enables DATA IN at L5-6 from the line receiver L60 to the serialization registers and removes the jam clear from the START BIT detector and the IN SYNC F/Fs L45.

When the Header/Instruction byte is received at the input of line receiver L60, the start bit detector must sync with the first data bit (START BIT) received which will always be at a one level. The one level bit will be captured by the L45-12 D-type F/F when set by input clock (CK) and presented to the L45-2 D F/F via the output of L34-6 AND gate. When data is detected after the START BIT detector is set, then the input to F/F L45-2 will enable it to set producing IN SYNC at L45-6. The Q output L45-5 of IN SYNC is fed back to L38-9 to create a latch up condition during the input of the next 10 data bits.

*IN SYNC will enable gate L35 with L4A F/F reset allowing L34 to clock (CK at a 17.1 mhz rate) a two bit Gray Code counter L46 whose count sequence will be 10, 11, 01, 00. The gray counter (Bit Sampler) will, at the count of 00, gate CK to the output of AND gate L44-8 for the following functions:

1) Shift data into SERIALIZATION registers L41, L42 and L43.
2) Clock the L47 four bit counter.
3) Clear the START BIT detector when the L47 Bit Counter reaches the binary count of 10.

When the L47 Bit Counter reaches the count of 10 and the Bit Sampler is at its second count (11) the AND gate L49-6 will output signal clock DISA. DISA is used to clock the Byte Timing register L21.

The HEADER/INSTRUCTION byte is always the first byte of data to flow during any transfer, therefore it is necessary to decode both the header code 101 and the command (instruction) code. See chart above.

Once the header byte is serially loaded into the serialization registers, data bits D5, D6 and D7 (header code) are decoded by three NAND gates labeled L9. From L9-8 the decode goes to the D1 input L21-3 of the Byte Timing register and clocked in by DISA. The Q1 output of L21-2 will be an active high signal INST which latches itself through inverter L10 to L9-10 and 11 and remains latched during successive DISA clocks. INST when active is used for clocking the five bit instruction word into the L20 instruction register. The instruction register decodes the 5 bit instructions to signals R/W, 1BT, 256BT, RESTART and STATUS. These bits are active in combinations also.

3.4.4 STATUS

The Header/Instruction command STATUS is issued by the Master over the Data Link to retrieve information from a slave unit as to its present state (same procedure as discussed under HEADER/INSTRUCTION BYTE). The byte of data retrieved from a Workstation (slave) and transferred back to the Master will consist of the following:

NR (Not Running)
BP (Bad Parity)
LE (Line Error)
PR (Power On)

The four status bits above will be accompanied by an ID code that occupies the other four bits of the Status byte which identify the slave selected.

Once the status instruction is clocked into L20 instruction register the output signal STATUS at L20-12 is active high. Status when active will gate the Data Link into the TRANSMIT mode via L4-3 going high.

At Bit Count 10 and the Bit Sampler at count 00 the Bit Counter L47 is loaded with zeroes on the 11th clock producing a high at the output of NOR gate L36-6. This output is NANDed with*REC (high) at the output of L35-3 generating*DOL which will load the STATUS word into the S/P register from the STATUS selected multiplexers L32 and L33. STATUS is also ANDed with DOL from L25-8 to switch the L30, L31 multiplexers to output the STATUS word to the L19 parity generator. When*REC goes high, the transmit data delay logic becomes active inhibiting any transmission for 8 us. *REC removes the load and clear inputs to L28-9 and L29-13 respectively to allow PHASE 2 clocks to increment the L28 counter. Since the L28 counter was initially loaded with a deficit count of 14, it will require 14 clocks (8 us) to produce a Carry Out that will enable L29 to set.

The Q output L29-9 at 8us timeout will perform the following:

1) Allow the Bit Sampler L46 (Gray Code Counter) and Bit Counter to start counting 17.1 MHZ clocks (CK) by removing the preset on L4A F/F enabling the reset on the next CK.
2) Enable the transfer of data out of the serialization register to the line driver L50 via AND gate L39-8.

The L4A F/F will reset on the next CK. This permits AND gate L34-8 to gate CK's to the Bit Sampler and Bit Counter. Every time the Bit Sampler reaches a count of 00, a clock pulse will be gated out of AND gate L44-8 to the clock inputs of the serialization register. The

S/P shift Register is in the Shift Right mode. Each clock at the output of L44-8 causes a bit to shifted out and transmitted to the line driver and onto the coaxial cable.

When the Bit Counter reaches a count of 10 the Bit Sampler continues its count to 11 enabling another DISA clock which produces a T1 output from the Byte Timing register L21.

The Bit Sampler clock proceeds to the fourth count 00 sending the last Bit clock (11) to the serialization register concluding the transfer of the entire STATUS word. The last clock also clocks a reload of L47 bit counter with zeroes because L47-9 went low at the 10 count. Zeroes will be decoded by the NOR gate L36-6 and ANDed with REC producing DOL at inverter L25-8. DOL, STATUS and T1 are ANDed at L11 pin 12 and routed to the 8 pin NAND gate L12 whose output will generate a Data Link Clear(*DLCL). *DLCL will clear the Byte Timing register and the Instruction Register ending the Status operation. The Data Link is also restored to the REC mode which clears the transmit delay logic producing a Character In Clear signal(*CICL) at L7A-3 which will clear the S/P register.

3.4.5 RESTART

The Restart instruction is used to reset the 8080 CPU in the SLAVE and to clear the NR (Not Running) Status. The Restart instruction is loaded into the Instruction Register as already outlined for other instructions.

As soon as Restart goes active the L26-12 one shot MV is fired to generate a 20 us pulse. This pulse is routed to the CRT control 8080 CPU input RESET which initializes the program counter to address 0000 and produces a Master Reset (MR) for clearing all operational registers.

Restart will also be NANDed with signal Reset Clear RC at the input of L14. L14-8 will go low at the input of the 8 input NAND gate L12-2 producing a Data Link CLear*(DLCL) to end the Restart instruction. RC is generated when the Bit Counter is at count 10 and the Bit Sampler is at the fourth count of 00. At this time the 11th bit of the Restart byte is completely loaded into the serialization register and the Bit Counter is clocked to reload with zeroes.

Once*DLCL is clocked it is used to clear the Instruction Register L20 and the Byte Timing register L21.

3.4.6 256 BYTE WRITE

A 256 Byte Write command transfer INSTRUCTION word when loaded into the Instruction register L20 will cause the 256 BT and R/W to go high while the master is transferring data to a slave.

If a line error is not active (high), it will AND with R/W at the output of L3-8 producing signal DMA R/W which goes to slave memory for controlling DMA input access.

The high output R/W is inverted causing NAND gate L2-6 to go low. STATUS is low (not being processed). These two lows will logically provide a low at L4-3 which is the receive mode*(REC).

The second byte shifted into the serialization register after the 256 BT WRITE Header/Instruction word will be the high order address bits of a 16 bit address (2 bytes required). This address byte will be clocked into high order address registers L53 and L54 by a T1 clock which occurs on the second DISA. The first DISA clocked INST. (HEADER DECODE).

The third byte shifted into the serialization register will be the low order address byte and it will be clocked into the low order address registers L51 and L52. Prior to loading the third byte the

Data Link is in T1 time and NOT T2 time, permitting AND gate L3-11 (which decodes this condition) to enable the load input for the L51 and L52 low order address registers.

At T2 time and NOT T3, NAND gate output L22-3 enables EP input to the low order address register. Therefore, the next DIS and DISA clock (which occur simultaneously) will gate the low order address into L51 and L52, and set the Data Link at T2 time.

The first data word is shifted into the serialization register during T2 time as T3 time is counting. At the 11th count DIS and DISA are generated and the data word in the serialization register is clocked into a TRI STATE register on the memory board 7226 by signal DIS. The memory board will write the data word into the address specified by the High and Low order address register on the Data Link board. DISA also clocks Byte Timing to T3. T3 will from now to the end of the transmission will keep EP high permitting the Low Order Address register to count DIS pulses which increment the address to the next higher address location for the page of data. T3 accomplishes this via the L22-3 and L4-11 gates which causes the input EP to go high allowing the counters to count DIS clocks after the first address has been written.

The data flow will continue in this manner until the Carry Out (CO) from L52-15 is active indicating 256 bytes of data have been received and written into memory. 256BT, R/W, CEA and CO are NANDed at L13-6 for a 256 BTYE clear Receive signal that clears the data link*DLCL and ends the instruction.

3.4.7 256 BYTE READ

A 256 Byte Read instruction word will be decoded in the same manner as the write instruction. The Data Link will be in the receive mode only during the time that is required to load the starting address for accessing memory. Signal INST is generated by decoding

the header and clocking BYTE TIMING with DISA. INST is the clock for loading the 256-BYTE READ instruction into the instruction register. The second DISA will clock T1 which loads the high order address into RAM address registers L53 and L54 from the serialization register. The low order address is the third byte and when loaded into the serialization register will produce the third DISA clock and DIS. DISA clock shifts T2 into the Byte Timing register causing the receive *REC line to go high (TRANSMIT). T2 causes L2-6 to go high producing a high at L4-3. Signal DIS clocks the low order address into registers L51 and L52. Data Link time T2 and NOT T3 produce a low at the output of L22-3 which NORed with the REC line will enable EP to start counting addresses for accessing RAM. Data accessed from RAM is loaded into Data Selector/Multiplexers L32 and L33. STATUS is used to select Data (A) when not active.

The REC line going high at T2 time also enables the 8 us turn around transmit data delay counter L28 that was loaded with a deficit count of 14 prior to the transmit mode of operation. The counter is clocked by PHASE 2 until full with carry out (CO) enabling D-type F/F L29-9 to set, permitting AND gate L39-8 to enable DATA OUT to L50 output driver. L29-9 also removes the preset on L4A enabling the BIT SAMPLER and BIT COUNTER to produce the clock and SHIFT/LOAD enable for clocking data out of the serialization register to the output Driver L50.

3.4.8 WORKSTATION---1-BYTE WRITE

A 1-Byte Write will be performed with the data link in the REC mode. The 7 us receive delay will time out before the 1-Byte Header/Instruction word is serially clocked into the S/P register. DISA shifts INST into the Byte Timing register L21 which clocks the 1-Byte Write instruction into L20 (Instruction register). The following events occur:

1) The 1BT and R/W outputs from L20 are both high when the Master is writing to a slave.

2) 1-BT and INST produce a low at the output of L50A which resets L58 F/F gating the 8080 Ready Control signal*DMA R/B low causing the 8080 to WAIT (BUSY) until the 1-BYTE Write is performed.

3) If the line error is not active when ANDed with R/W, a DMA R/W will be generated at the output of L3-8 which goes to slave memory.

4) Signal R/W is inverted by L25 presenting a low to AND gate L2 which carries through to an OR condition at L4. Status input being low develops a low output at L4-3 labeled*REC which is the receive mode of operation.

5) The second byte of data serially loaded into the S/P register is the high order byte of a 16 bit address. This byte is presented to L53 and L54 address registers via the DI bus. The second DISA clock will shift T1 time into the BYTE TIMING register which clocks the high order address into the address registers.

6) The third byte of data shifted into the S/P register is the low order address presented to registers L51 and L52. (The low order address is a specific address issued from the 8080 master selected by 1-BYTE from multiplexers L58 and L59 on the Master Memory board.)

   The Byte Timing is shifted to T2 time with another DISA, however, a T1 and inverted T2 time will gate an output at L3-11 which is inverted by L8 loading the low order address.

7) Also a T2 and NOT T3 gate a low at the output of L22-3 which produces a low at the output of L4-11 and inhibits the low order address registers from counting.

8) The fourth byte is the data byte shifted into the S/P register and presented to the DI bus for a write into memory at T3 time.

9) With the BIT COUNTER at count 10 and the BIT SAMPLER at 00 the output signal RC at L49-8 clocks the DMA timing F/Fs L16 and L15 generating signal CEA. CEA (Completion of 1BT WRITE) is NANDed with T3, 1BT and R/W producing a low at L13-8 *DLCL which is used to clear the operation.

3.4.9 WORKSTATION---1-BYTE READ

A 1-BYTE READ operation requires the data link to be in the receive mode while the Header/Instruction byte (1BT READ) and the two bytes of address are being serially clocked into the S/P register. Up to this point the operation is identical to the 1BT WRITE. The operation proceeds as follows:

1) AT INST time, the instruction is clocked into the instruction register L20 producing R/W (a low) and 1BT (a high). DMA R/W is active low for a READ.
2) The second byte (high order address) is clocked into the S/P register and loaded into address registers L53 and L54 at T1 time.
3) The third byte (low order address) is loaded into address registers in the identical manner as a 1BT WRITE at T2 time. T2 time ANDed with 1BT and inverted R/W produces a high output at L2-6 and L4-3 gating the data link into a transmit mode.

   Signal DMA becomes active at the output of L3-3. Transmit mode also enables the turn around Transmit delay of 8 us to time-out by causing the Load input on L28 to go high. T2 and not T3 time gates a low at the output of L22-3 that clears the S/P register.
4) PHASE 2 clocks fill the L28 counter and produce a Carry Out (CO) that enables D-type F/F to set gating a high output at L29-9. This high enables the AND gate at L39-9 for DATA OUT to the line driver L50 and removes the preset on D-type F/F L4A permitting the next CK signal to switch L4A-5 low.
5) The low enables the Bit Sampler and Bit Counter to count. When the Bit Counter reaches the count of 10 and the Bit Sampler at count 11, signal DIS A is again generated shifting T3 into the Byte Timing register. Durihg this counting period no data was transferred.

6) DMA and DMA R/W during the above counting period accessed the addressed word in memory which is waiting to be clocked onto the Data Out bus to the Data Link.

7) At Bit count 10 and Bit Sampler count 00, signal RC at the output of AND gate L49-8 clocks the DMA TIMING F/F L16 enabling F/F L15 to set generating signal*DMACE at pin 6. This signal gates the Data Byte to be transferred from memory into Data Link multiplexers L33 and L36.

8) At Bit Count 11 the last S/P register clock is generated at the output of L44-8 which clock loads the Bit Counter to all zeroes producing a high at the output of L36-6. Transmit mode NANDed with this output produce signal*DOL that clocks the DATA byte into the S/P register (Byte is parallel loaded).

9) A repeat count of the Bit Sampler and Bit Counter for serially clocking the Data Byte out of the S/P register to the line driver occurs. When the Bit Counter reaches count 10 and the Bit Sampler is at count 11, another DISA shifts T4 time into Byte Timing.

10) At Bit Count 11 the Bit Counter is cleared generating another*DOL signal. *DOL is ORed with a low output from L14-6 (a NAND of T4 and 1BT) at L38-11 which produces a Data Link Clear*DLCL terminating the 1-Byte Read operation.

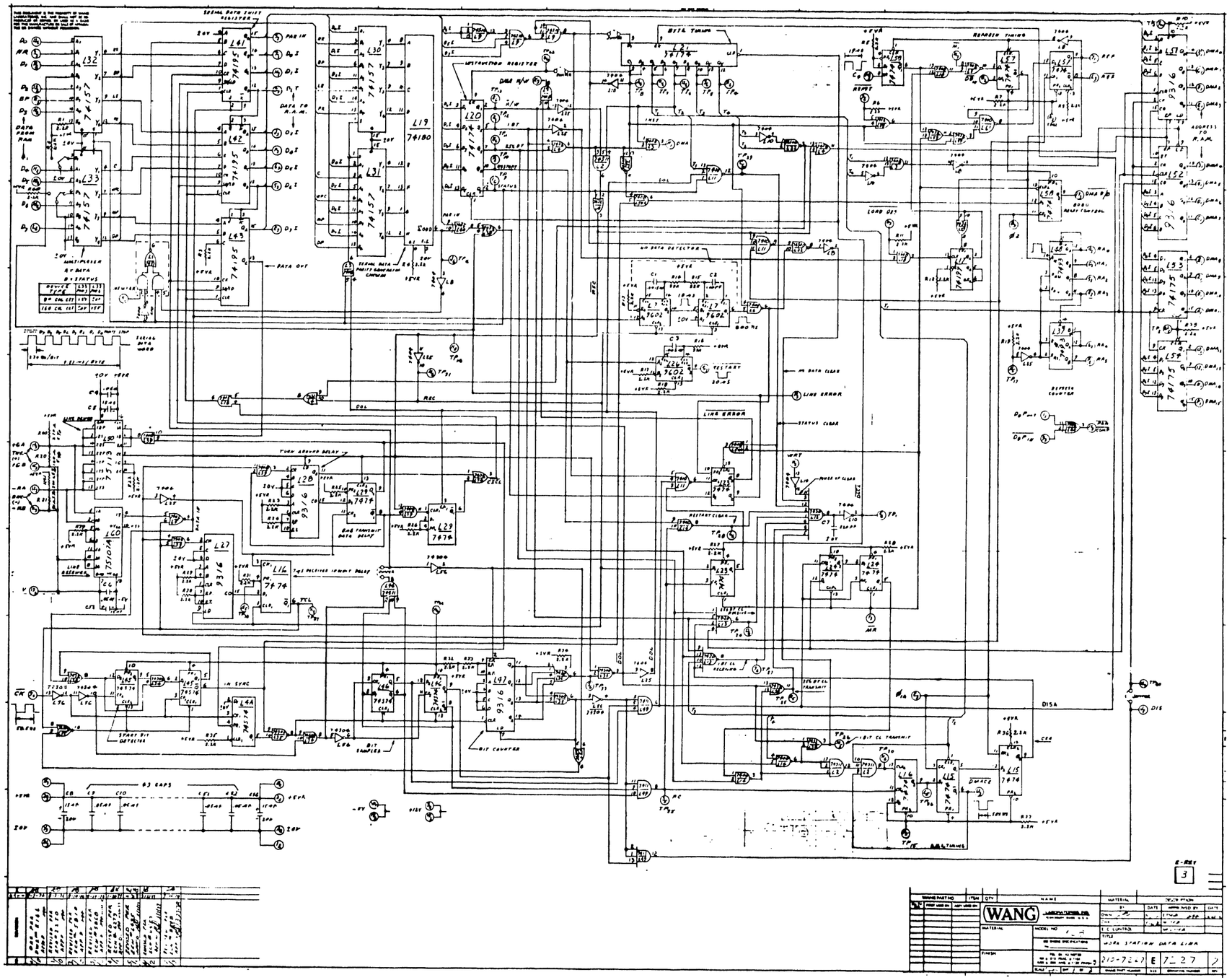


Figure 3-13 Workstation Data Link-Schematic Illustration — Sheet 1

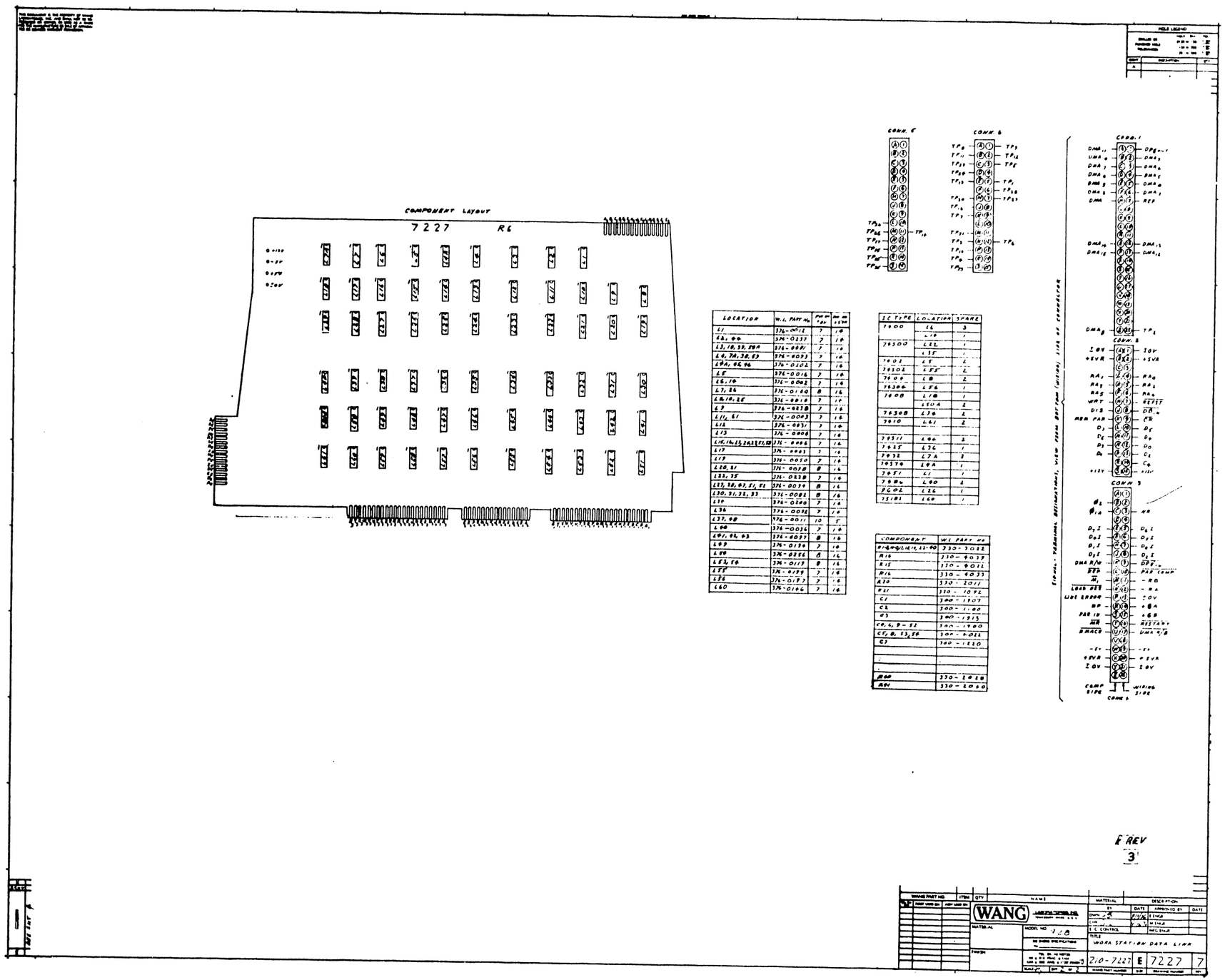


Figure 3-13 Workstation Data Link-Schematic Illustration — Sheet 2

3.5 MOTHERBOARD (7228)

As in the case of the master motherboard, the workstation motherboard is presented because it is the only semblance available of a wiring diagram for this section. A signal can be traced on the motherboard but the "Seek & Find" method must be employed to identify the signal.

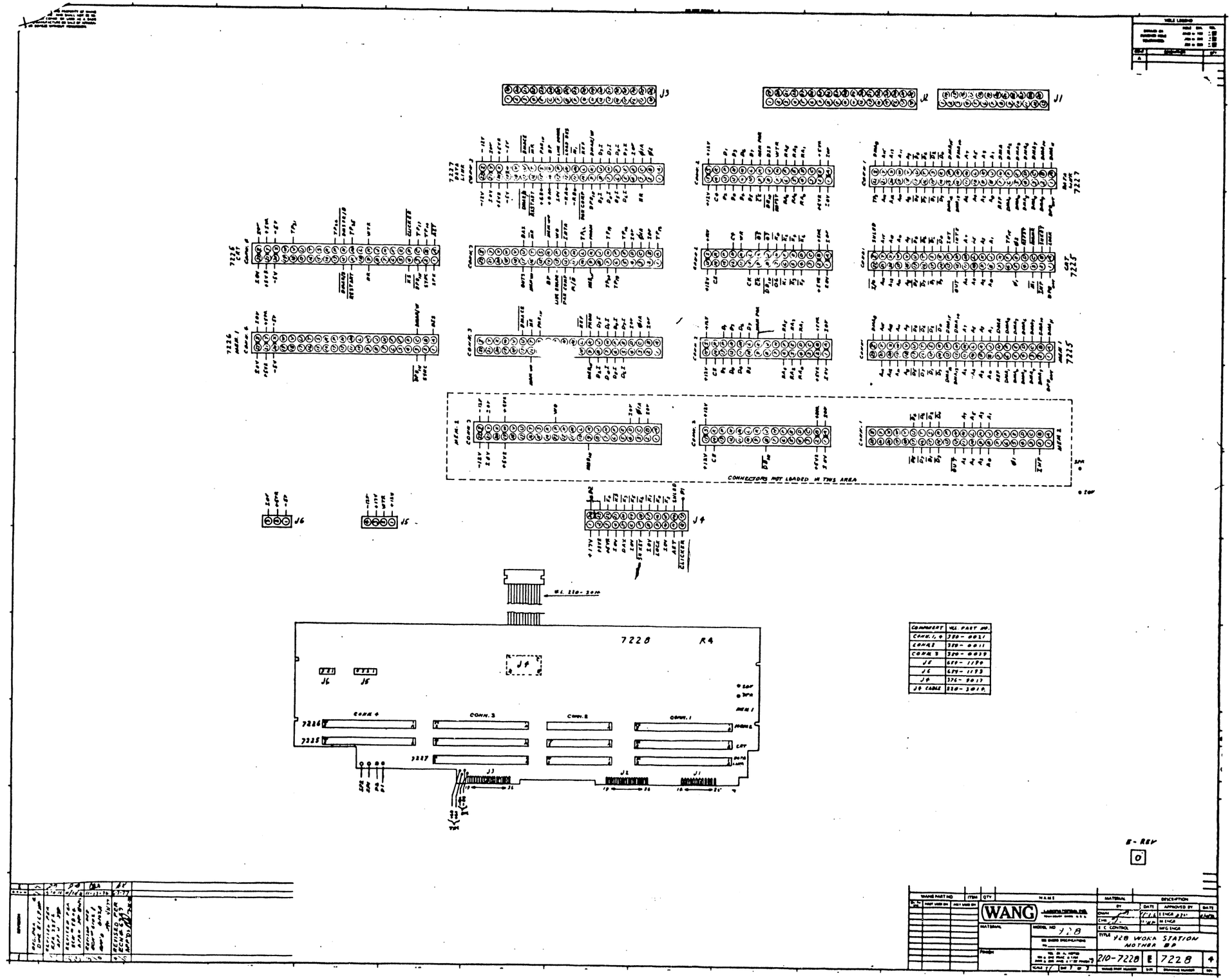


Figure 3-14 Workstation Motherboard-Schematic Illustration

3.6 KEYBOARD (7229)

Whenever a key is struck on the keyboard, the hardware forces a trap to location 0.

The contanets of the character buffer of the keyboard will be transferred to the processor's accumulator upon issuing an IN 00.

Figure 3-15 contains the layout of the American Keyboard. Above each key is the code delivered to the processor accumulator when an IN 00 is issued. Space, period, backspace, underscore, cursor north, south, east, and west are repeat keys.

Table 3-3 is a conversion table between the external and desired internal character set. the software upon detecting a keystroke will convert the key codes to suitable ASCII key codes.

Tables 3-4 and 3-5 list the full ASCII internal character set.

The keyboard will also contain a clicker which will sound whenever an OUT 00 is issued. This command will be issued by the software whenever a keystroke is accepted.

Table 3-6 represents the special screen graphics.

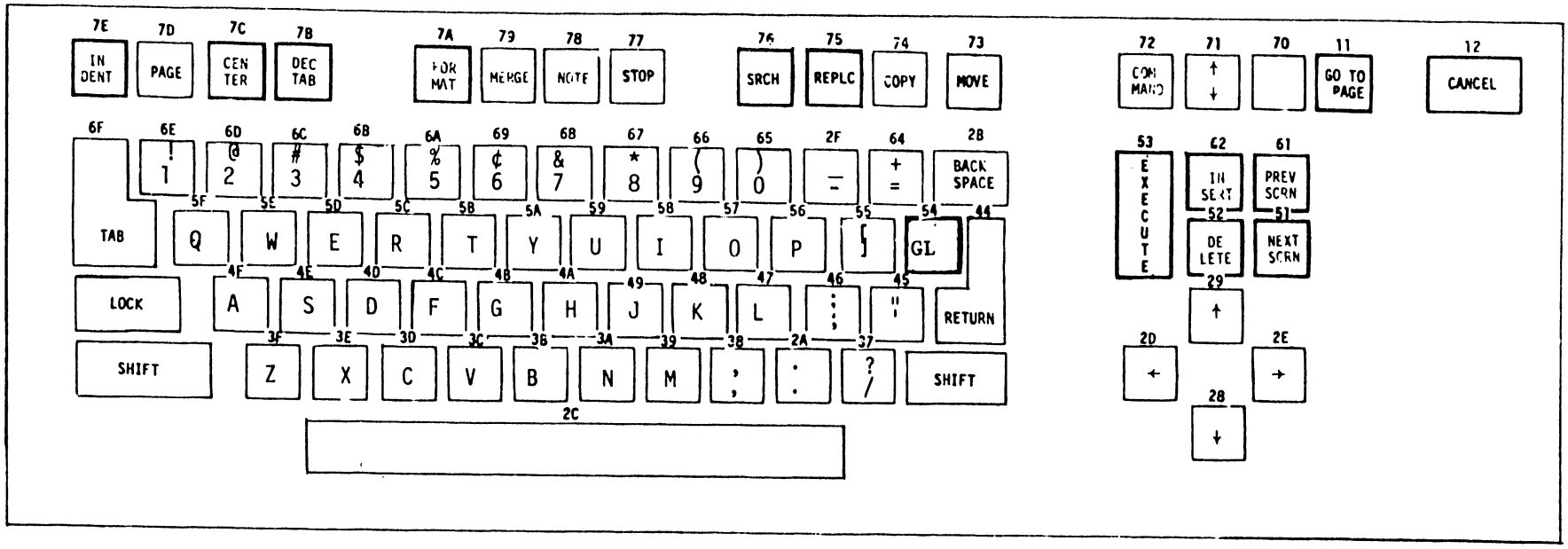


Figure 3-15 1260 American Keyboard

TABLE 3-3

TRANSLATION TABLE

(EXTERNAL TO INTERNAL KEYCODE)

External To Internal Keycode Translation Table

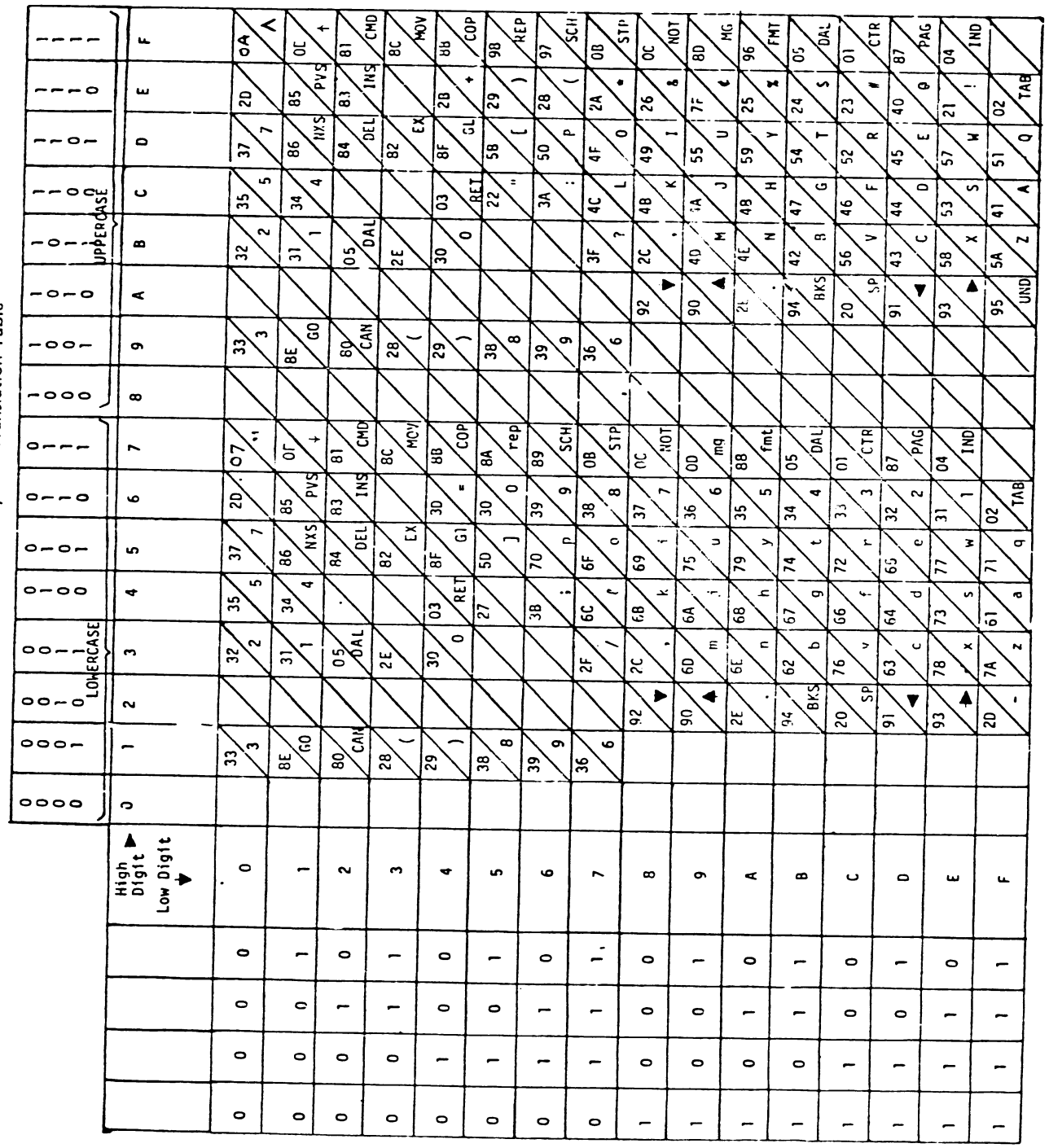


TABLE 3-4

1260 INTERNAL KEYCODE - (ASCII) CHARACTER VALUES

b 7	0	0	0	0	0	0	0	0	1	1
b 6	0	0	0	0	1	1	1	1	0	0
b 5	0	0	1	1	0	0	1	1	0	0
b 4	0	1	0	1	0	1	0	1	0	1

b 3	b 2	b 1	b 0	High digit ---> / Low digit	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0		â*	SP	0	@	P	°	p	CAN	CN
0	0	0	1	1	CTR	ê*	!	1	A	Q	a	q	CMD	CW
0	0	1	0	2	TAB	î*	"	2	B	R	b	r	FX	CS
0	0	1	1	3	RET	ô*	#	3	C	S	c	s	INS	CE
0	1	0	0	4	IND	û*	¤	4	D	T	d	t	DEL	PKS
0	1	0	1	5	DAL	ä*	%	5	E	U	e	u	PVS	UND
0	1	1	0	6		ë*	&	6	F	V	f	v	NXS	FMT
0	1	1	1	7	¨*	ï*	'	7	G	W	g	w	PRG	SCH
1	0	0	0	8	´*	ö*	(	8	H	X	h	x	fmt	REP
1	0	0	1	9	*	ü*	)	9	I	Y	i	v	sch	COP
1	0	1	0	A	^*	à*	*	:	J	Z	j	z	rep	
1	0	1	1	B	STP	è*	+	;	K	[	k	§*	cop	
1	1	0	0	C	NOT	ù*	,	<*	L	*	l	£*	MOV	
1	1	0	1	D	MG	Ä*	-	=	M	]	m	é*	MG	
1	1	1	0	E	↑	Ö*	.	>*	N	ß*	n	Ç*	GO	
1	1	1	1	F	↓	Ü*	/	?	O	¶*	o	¢	GL	

The * items are not available on the American keyboard.

TABLE 3-5

ABBREVIATIONS

(RE: TABLE 3-4)

Abbreviation	Key
BKS	Backspace
CAN	Cancel
CMD	Command
CTR	Center
cop	Copy (l.c.)
COP	Copy (u.c.)
CE	Cursor East (right)
CN	Cursor North (up)
CS	Cursor South (down)
CW	Cursor West (left)
DAL	Decimal Tab
DEL	Delete
EX	Execute
fmt	format (L.C.)
FMT	Format (U.C.)
GL	Glossary
GO	Go To Page
IND	Indent
INS	Insert
mg	Switch Document (L.C.)
MG	Don't Switch Document(U.C.)
MOV	Move
NOT	Note
NXS	Next Screenload
PVS	Previous Screenload
PAG	Page
RET	Return
rep	Replace (L.C.)
REP	Replace (U.C.)
SP	Space Bar
sch	Search (L.C.)
SCH	Search (U.C.)
STP	Stop Code
TAB	Tabulation
UND	Underscore

TABLE 3-6

SPECIAL SCREEN GRAPHICS

Location	Graphic Symbol	Graphic Interpretation
00	blank	skip, used for tab zone region
01	◆	center
02	▶	tab
03	◀	return
04	→	indent
05	└	decimal tab
06	|	graphic
0B	▬	stop
0C	!!	memo
0D	↕	switch read

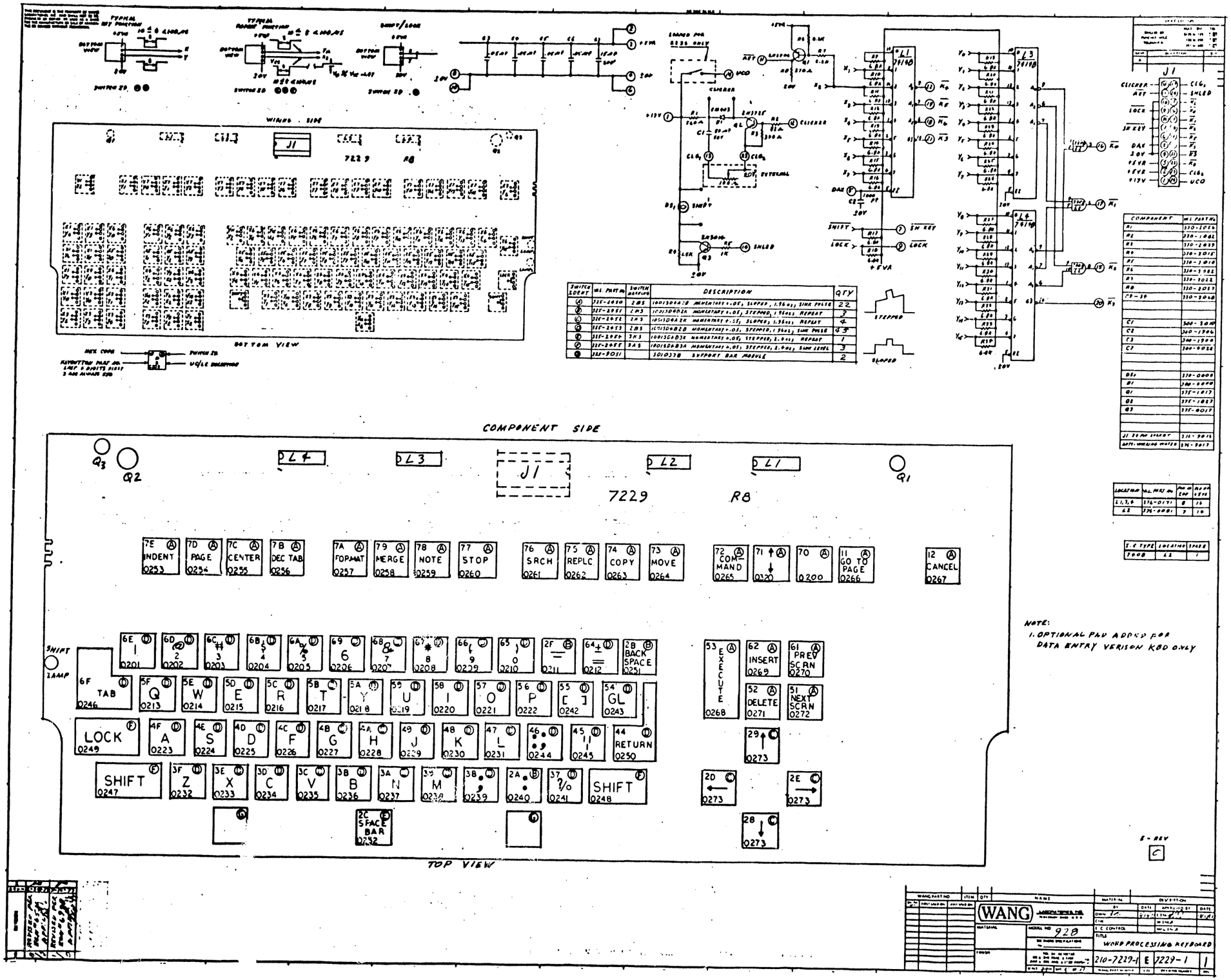


Figure 3-16 Workstation Keyboard-Schematic Illustration

SECTION 4

PRINTER THEORY OF OPERATION

SECTION 4
PRINTER THEORY OF OPERATION

4.1 FRONT CONTROL PANEL (6762-1)

The control panel keyboard is presented here as figure 4-1 to allow the reader a ready reference of switch connections and loading.

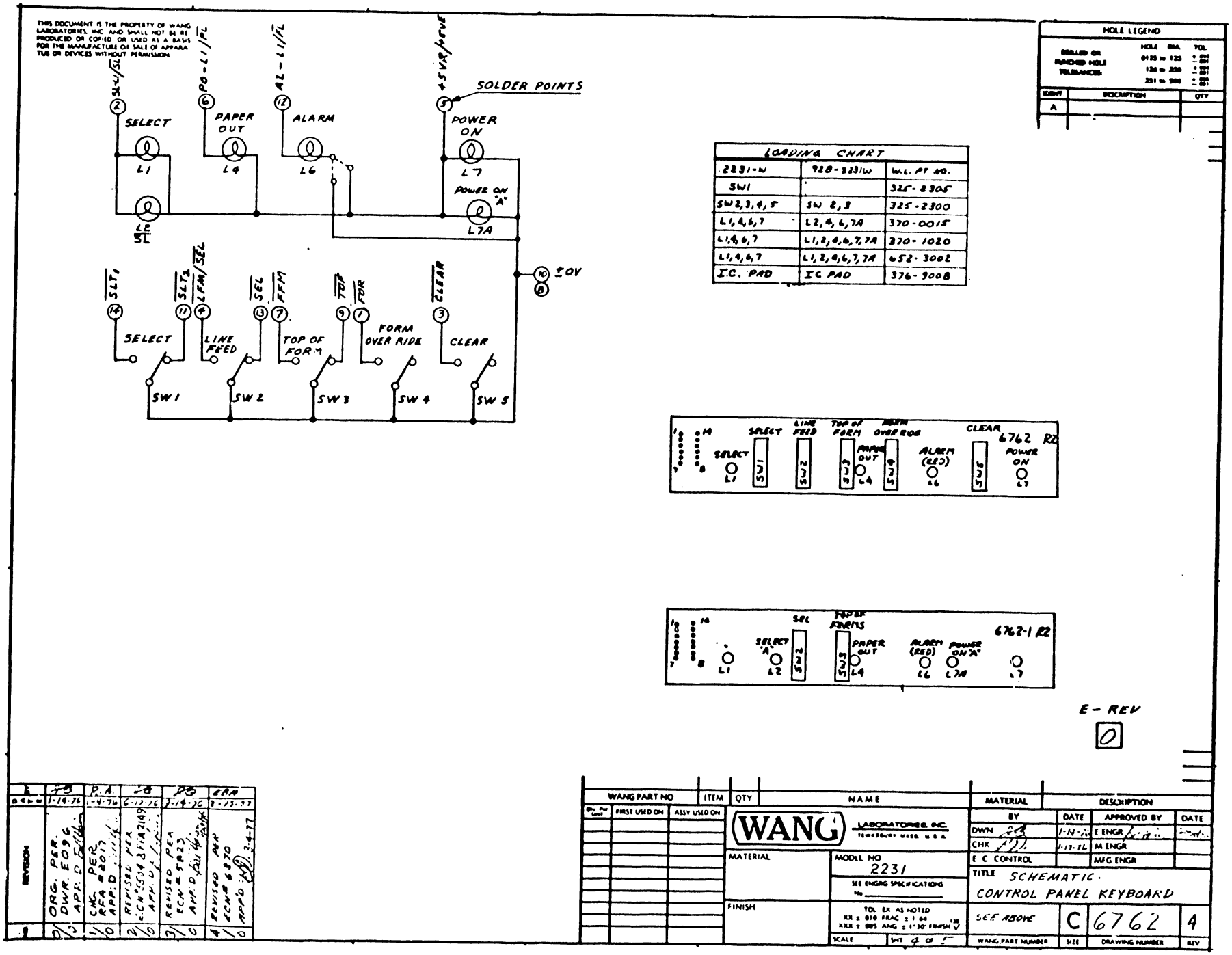


Figure 4-1 Printer Front Control Panel-Schematic Illustration

4.2 POWER SUPPLY/REGULATOR (7249)

The power supply/regulator is presented here as figure 4-2 to provide the reader with an in-section reference to the operating voltages, and component layout.

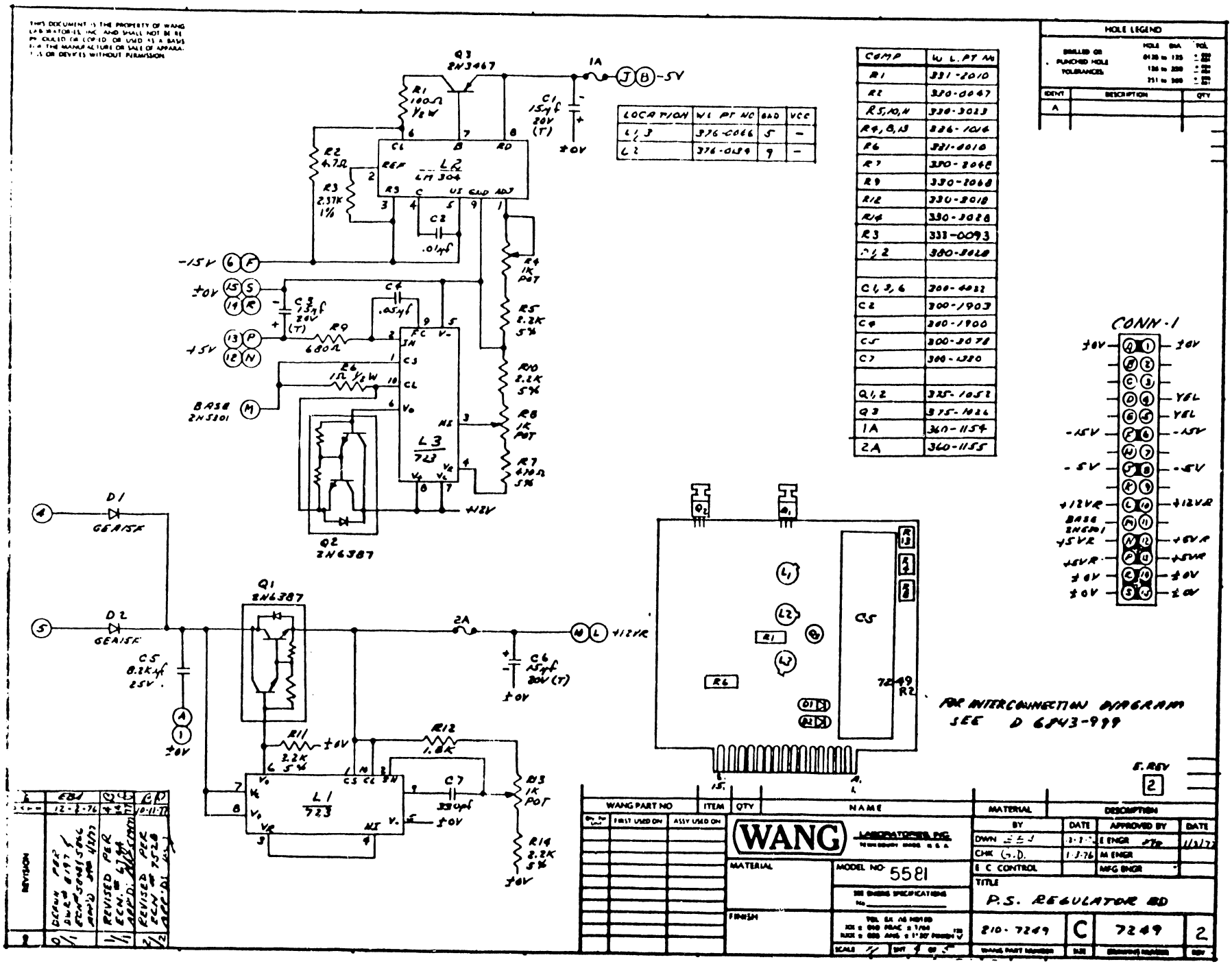


Figure 4-2 Printer Power/Supply Regulator Schematic Illustration

4.3 I/O BOARD FOR 928 MATRIX & DAISY PRINTERS & PIO-7346

4.3.1 GENERAL DESCRIPTION

The I/O board for the Matrix printer, Daisy printer and Photocomposition Input Option (Paper Tape Punch for Phototypesetter) consists of a section of the Data Link Control Logic and the Input/Output commands that are issued by the Printer CPU. The IN/OUT commands control each of the three options:

1) Line Printer
2) Daisy Printer
3) PIO

The Data Link control logic on the I/O board 7346 is an extension of the data link installed on Printer CPU board 7348. To simplify the discussion the complete data link has been described on the 7348 board. Reference must be made to each drawing as described.

4.3.2 PRINTER PROCESSOR IN/OUT COMMANDS (Figure 4-3 and Table 4-1)

The Printer I/O board has been designed to adapt to three different options available to Wang customers. These options include a DAISY printer, Matrix (Line) printer or the PIO. The PIO (Photocomposition Interface) unit is a Model 5508 consisting of a self contained Paper Tape Punch and an electronic "Translator". The I/O board controls for these options are IN/OUT commands issued by the Printer 8080 CPU. The commands are coded 8080 address bits A0-A3 that are presented to two BCD to DECIMAL decoders L8 and L22. The decoders are selected by a write (WR) for OUT commands and a read (DBIN) for IN commands.

4.3.3 DAISY PRINTER CONTROL

The DAISY printer responds to three basic commands, each driven by a two byte code from the 8080 data bus. The 8080 data bus is presented to three TRI-STATE QUAD D-TYPE F/Fs L29, L30 and L31. The

TABLE 4-1

PRINTER PROCESSOR I/O COMMANDS

1. Matrix Printer

OUT 08 - delivers 8 bits of data or control to the 8080 output ports.

OUT 0A - send the contents of the output ports to the printer.

OUT 0C - resets the printer.

OUT 0E - lamp control.

OUT 0B - deselects the printer.

IN 02 - delivers status from the printer.

IN 03 - deliver control information from the printer.

2. Daisy Printer

OUT 08 - sends low byte of data to the 8080 output ports.

OUT 09 - sends the high byte of data to the 8080 output ports.

OUT 0A - sends the contents of the output ports to the printer. The accumulator of the 8080 designates what the data is for - vertical, horizontal motion, or print information.

OUT 0B - deselect the printer.

OUT 0C - sound alarm.

OUT 0D - ribbon control.

OUT 0E - lamp control.

IN 02 - daisy status.

IN 03 - daisy control information.

Debug:

IN 06 - read keystroke.

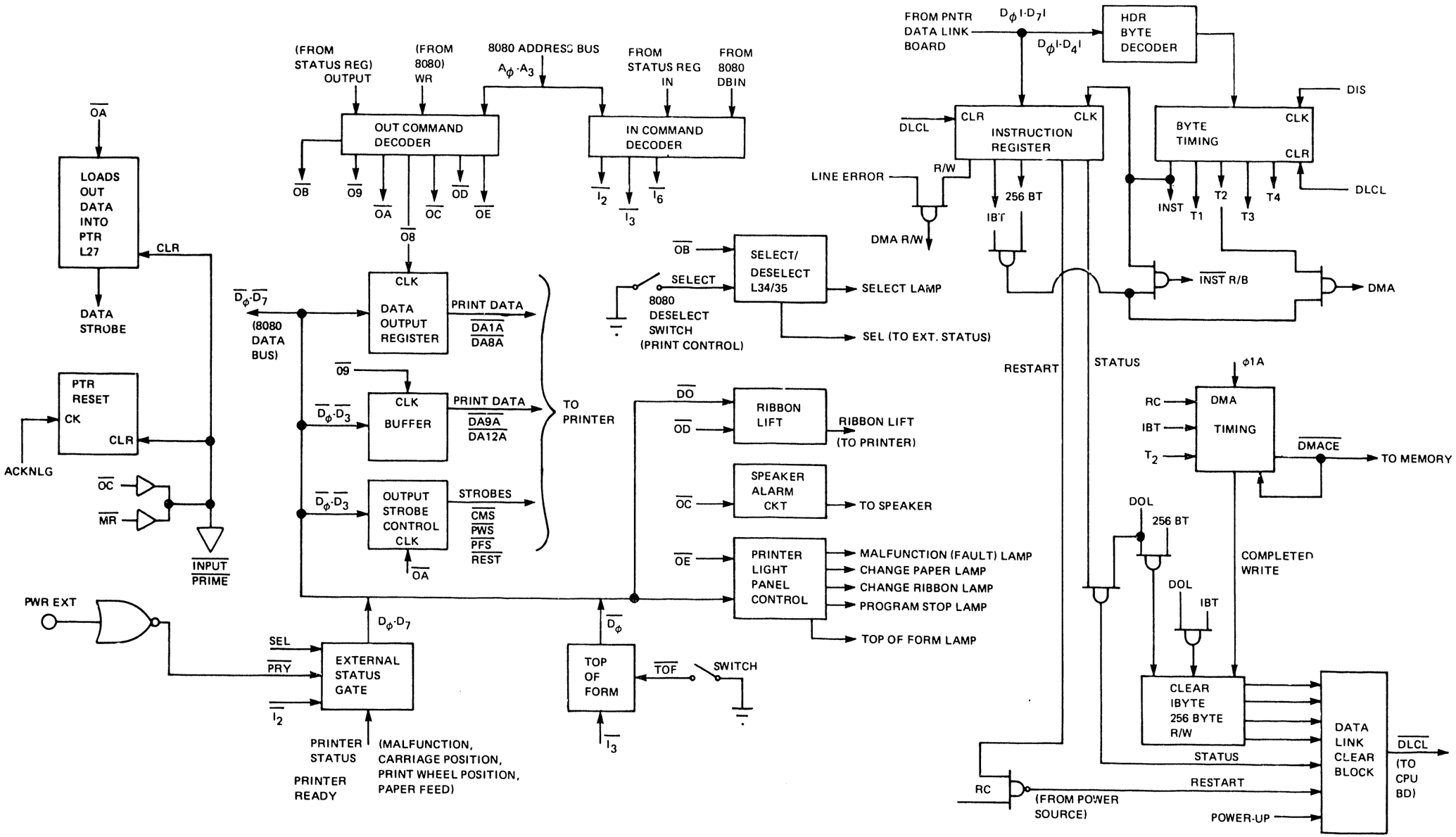


Figure 4-3 Printer I/O Board-Block Diagram

output code lines to the Daisy are DA1A-DA12A. The low byte (DA1A-DA8A) and high byte (DA9A-DA12A) are codes that command Horizontal and Vertical incremental movements for the carriage and platen. The Print command uses only the low byte.

1. OUT8*command sends the low byte to the printer.
2. OUT9*command sends the high byte to the printer.

A D-type F/F register L33 and buffer L32 is the output strobe control for each of the three movements including a Restore.

The strobes are indentified as follows:

CMS*= Carriage motion strobe
PWS*= Print wheel strobe
PFS*= Paper feed strobe
REST*= Restore

OUT 0A*is the command for strobing the required movement coded in the high and low bytes.

OUT 0B* is used to deselect the Daisy by clearing the SELECT L34 F/F. Clearing the F/F enables itself for a select by tying the*Q output back to the D input. A select (SEL) input to L35-5 F/F from the daisy keyboard will clock the select. The keybord select button if depressed again will deselect the printer.

OUT 0C*initiates an alarm which is controlling a speaker indicating an operator error. A one-shot MV L7 triggers a timer L21 (Speaker audio circuit) that results in a short audio tone.

OUT 0D*controls the Ribbon Lift*(RLT). The 8080 data bus bit*D0 selects one of the two colors to be printed. L34 F/F latches the bit and buffer L15 gates it into the printer.

OUT 0E*is used to clock 8080 data bus bits*D0-D3 into F/F lamp driver register L18 for displaying Fault Lamp (FL), out of Paper Lamp (PL), Ribbon Lamp (RL) and Program Stop Lamp (PSL).

IN 02* enables STATUS bits from the printer onto the 8080 data bus via buffer L16.

IN 03* enables control information on Top Of Form (TOF) into the 8080 on data bus bit*D0 via buffer L15.

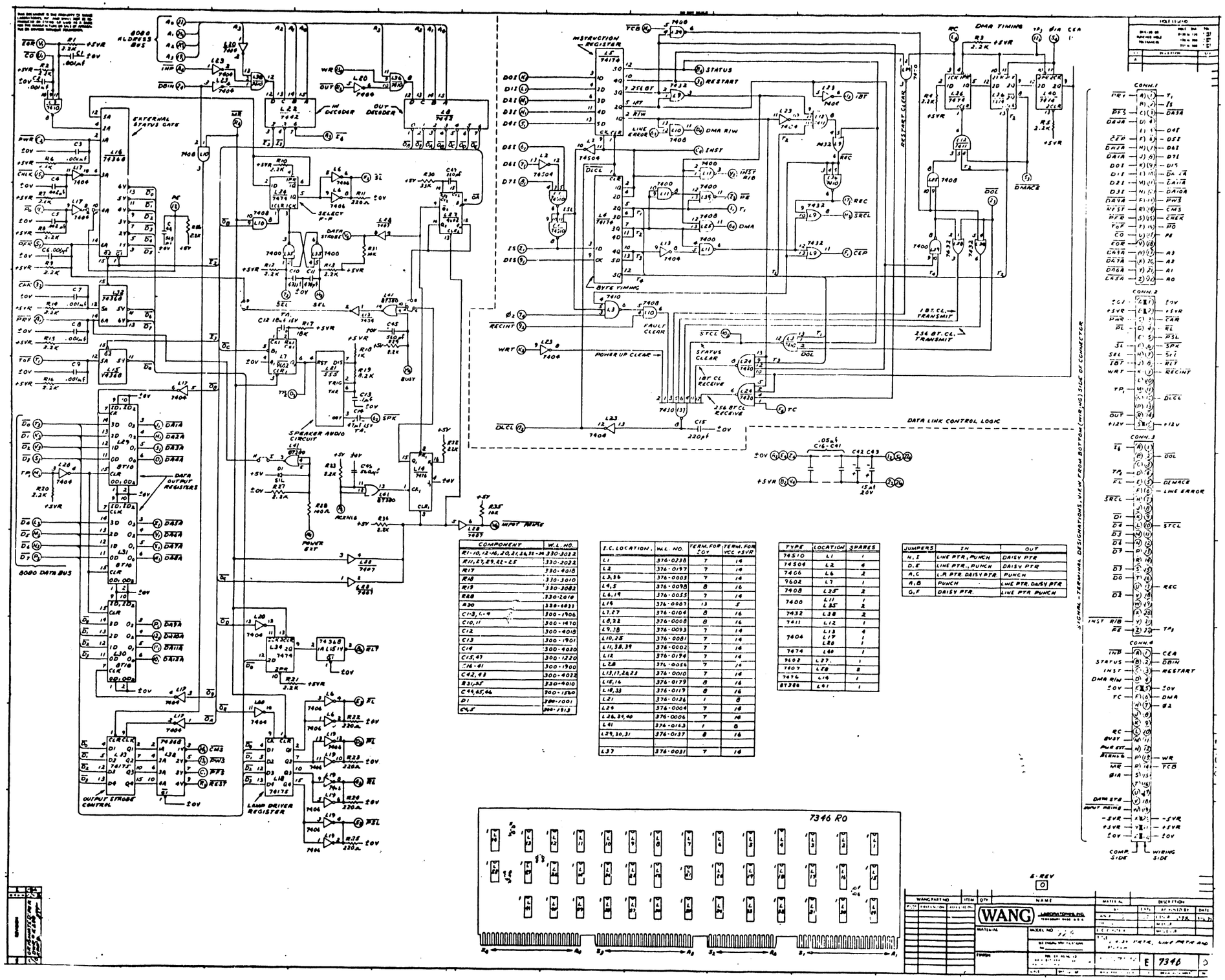
4.3.4 MATRIX PRINTER CONTROL

OUT 8*- Same as daisy
OUT 9*- Same as daisy
OUT A*- Same as daisy
OUT B*- Same as daisy
OUT C*- Generates an*INPUT PRIME signal that resets the printer.
OUT E*- Same as daisy
IN 2* - Same as daisy
IN 3* - Same as daisy

4.3.5 PHOTOCOMPOSITION INPUT OPTION -

A +5V ON signal is generated when power is applied to the Tape Punch by the front panel rocker switch. This signal is routed to the I/O board as a POWER EXT signal and applied to the input of NOR gate L41 gating a low output at L41-3. When jumpered (H,I) to the input of buffer L32, this signal is read into the 8080 by an INPUT*IN 02 command via the data bus bit*D0 indicating the Punch is Ready*(PRY).

An OUT command*OUT 0A is used to trigger a one-shot MV output L27-9 which generates a Data Strobe*(DTSB) which is routed to the Tape Punch starting the tape punching process. *DTSB also sets F/F L35 which in turn clocks the SELECT F/F L34 generating select signals SEL,*SEL and*SL which lights the select lamp on the punch. Select F/F



COMPONENT	W.L. NO.
R1-10, 12-16, 20, 21, 26, 31-34, 38-M	330-3032
R11, 17, 19, 22-25	330-3018
R17	330-4018
R18	330-3010
R19	330-3082
R28	330-2018
R30	338-6033
C1-3, 5-9	300-1906
C10, 11	300-1470
C12	300-4018
C13	300-1901
C14	300-6030
C15, 17	300-1220
C16-61	300-1900
C42, 43	300-4022
R31, 35	330-9010
C44, 45, 46	300-1340
D1	300-1001
C45	300-1913

I.C. LOCATION	W.L. NO.	TERM. FOR 5V	TERM. FOR VCC +5VR
L1	376-0238	7	14
L2	376-0197	7	14
L3,36	376-0003	7	14
L4,5	376-0098	8	16
L6,19	376-0053	7	14
L16	376-0067	13	5
L7,27	376-0104	8	16
L8,32	376-0008	8	16
L9,38	376-0093	7	14
L10,25	376-0081	7	14
L11,38,39	376-0002	7	14
L12	376-0196	7	14
L28	376-0056	7	14
L13,17,20,23	376-0010	7	14
L18,16	376-0179	8	16
L18,33	376-0119	8	16
L21	376-0126	1	8
L29	376-0004	7	14
L22,34,40	376-0006	7	14
L41	376-0143	1	8
L29,30,31	376-0137	8	16
L37	376-0031	7	14

TYPE	LOCATION	SPARES
74S10	L1	1
74S04	L2	4
7406	L6	2
9602	L7	1
7408	L25	2
7400	L11 L35	1 2
7432	L38	2
7411	L12	1
7404	L13 L17 L20	4 1 1
7474	L40	1
9602	L27	1
7407	L28	8
7474	L14	1
8T26	L41	1

JUMPERS	IN	OUT
N, I	LINE PTR., PUNCH	DAISY PTR
D, E	LINE PTR., PUNCH	DAISY PTR
A, C	L.R. PTR. DAISY PTR.	PUNCH
A, B	PUNCH	LINE PTR. DAISY PTR.
G, F	DAISY PTR.	LINE PTR. PUNCH

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (W/R, WO.) SIDE OF CONNECTOR

4-REV O

4-10

Figure 4-4 Printer I/O Board-Schematic Illustration

also gates data bit*D1 onto the 8080 data bus. L27-10 is jumpered (A,B) to the input of NOR gate L41 and again at the output of L13-2 (D,E) which is gated onto the*D0 bit of the 8080 data bus. A BUSY signal returned from the punch latches the data bit which is recognized by the 8080 as a Punch Ready signal. Refer to WPNL #30 for cabling details from the TRANSLATOR to the PUNCH.

4.4 PRINTER/PIO MEMORY---7347

4.4.1 GENERAL DESCRIPTION

The printer memory board 7347 has a memory capacity of 12K divided into three 4K banks. The printer being a slave unit must have a memory that can be accessed by its own processor (8080) and the Master processor via the DMA (Processor Communication Channel). The logic for accessing printer memory is similar to the WS memory, however, the layout of circuitry and control signals requires the following details.

4.4.2 PRINTER/PIO MEMORY---8080 WRITE

An 8080 WRITE to printer memory requires that signal DMA is not active (low). A low at the select inputs of multiplexers L3, L38 and L20 will enable the 12 address bits A0-A11 to the inputs of Tri-State buffers L4 and L21. The buffers are inhibited during Refresh periods of 18ns every 585ns. The high four address bits A12-A15 are selected by a non-active DMA at multiplexer L67 and presented to a BCD to DECIMAL decoder L51. The decoder outputs activate the Chip Enable Drivers L15 and L32 via the L33 NAND gates for enabling one of the three RAM memory Banks. The L33 gates perform an OR operation for the REFRESH and CE (Chip Enable) cycles used to turn on the CE Drivers during these arbitrated priority controlled operations. Refresh (REF) signal enables the ROW counters L39 and L40 and the refresh column address buffer L5. A complete refresh of RAM memory is required at least every 2ms.

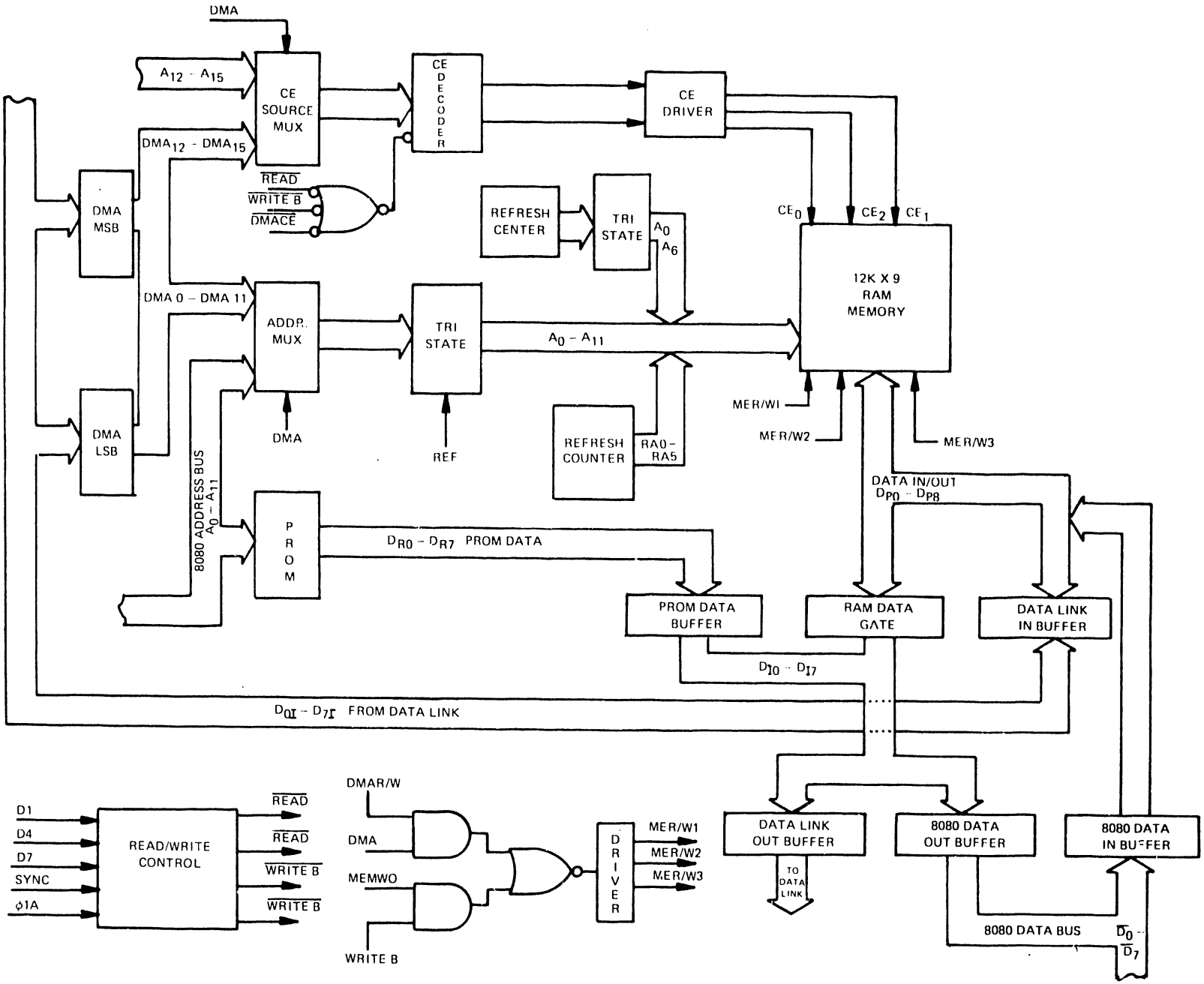


Figure 4-5 Printer Memory-Block Diagram

Jumpers A and B at the output of the decoder are used to activate the Test Prom L56. Signal*CD0 must be actively low to access prom data from data buffers L57 and L58. Conversely the CD0 is an inhibit to the output RAM data gates L58 and L59.

On any Basic 8080 instruction cycle (MCT) the address bus is active at T1 time before any status word is on the data bus. The status word (WRITE) appears halfway through T1 time on the 8080 bus with active data bits*D1 and*D4 that are NANDed with a SYNC and A14A15 signal producing a low at the output of L53-6.

D-type F/F L35 is enabled to reset at PHASE 1A clock time enabling F/F L34 to set on the next PHASE 1A clock (at this time the data byte is on the 8080 bus). *WRITE B and WRITE B are now active enabling data buffers L64 and L65 to memory and inhibiting the D input to decoder L51. WRITE B is ANDed with MEMWO at AND/OR gate L16-6 producing memory WRITE strobes*(MER/W1,2,3)at the output of buffer L50.

If the transfer of data is 256 bytes, the active signals needed for transferring the remaining bytes is the CE clock and MEMWO signal decoded at the status register of the CPU at the beginning of each 8080 write instruction. The address is also incremented by the 8080 at the same time.

4.4.3 PRINTER/PIO MEMORY----8080 READ

The 8080 READ of Printer Memory follows the same procedure as the WRITE when addressing the Bank and location in the selected Bank.

The READ Status Word byte is identified by bit*D7 which is inverted and NANDed with SYNC from the 8080 and address bits A14A15, producing a low at L52-12. This low resets the #1 section of F/F L35 generating a*READ and READ at the output pins 5 and 6 respectively.

READ*is a low inhibiting the D input of the L51 decoder. READ is NANDed with CE generating a clock for storing the parity bit (DP8) in the MEMPAR F/F L69. MEM PAR is routed to the S/P register in the data link section of the Printer CPU board.

If signal CD0 is not active (the pull-up resistor at the input of the inverter L17-9 is 5V) then a read of memory is enabled at RAM data buffers L58 and L59. On the next CE the parity bit DP8 will be clocked into the MEM PAR F/F and out at L69-6 to buffer L65. The RAM data byte will also be stored in D-type registers with Tri-State outputs L62 and L63. The data byte and parity will then be enabled onto the 8080 data bus by NANDing A14A15 and MEBIN.

If a Chip Enable decode gates CD0 active high a*PROM signal will be preset at L34-8 when L52-8 goes low. CD0 also inhibits a RAM memory READ from buffers L58 and L59. *CD0 enables the TEST PROM data to the D-Type registers with Tri-State outputs L62 and L63. A positive transition at the output of L68-11 clocks the data into the registers. A14A15 NANDed with MEBIN enables the data and parity onto the 8080 bus.

4.4.4 PRINTER/PIO MEMORY---DMA WRITE

The DMA WRITE operation is initiated when the Printer I/O board 7346 for the Matrix Printer, Daisy printer and Photocomposition Input Options has the Header/Instruction word stored and decoded in the Data Link Control Logic. See the I/O board 7346 for details.

Once the Header/Instruction byte is clocked into the S/P register on the Printer CPU board 7348, the byte is presented to the I/O board 7346 on the data link Data In (DI) bus. The I/O board contains the Data Link Control Logic required to decode the Header and the Instruction word. The signals decoded are DMA R/W and DMA.

DMA R/W conditions the memory write strobes and the Data In (DI) bus. No action occurs until DMA signal is active.

After the Header/Instruction byte is stored and decoded the High Order Address is the second byte to be loaded into the S/P register. Signal Data In Strobe (DIS) is generated on the Printer CPU board 7348 after each byte is loaded into the S/P register. DIS is routed to the Memory board for data control. DIS also clocks the Byte Timing register on the I/O board producing a T1 clock that loads the High Order address into the F/F registers L2 and L36. When the Low Order Address is loaded into S/P register, signal DIS again clocks the Byte Timing register generating T2 time and also loads the Low Order Address into counters L19 and L37. T2 activates DMA enabling the memory write strobes at the output of buffer L50. As each byte of data is written into memory, signal DIS increments the low address counter and enables the data on the DI bus to be latched into F/F registers L54 and L55 with the 3-state outputs. DMA R/W is NANDed with DMA at L52-6 which enables the data to memory for 1-byte or 256 byte transfers. Parity In (PAR IN) bit is separated from its byte of data at the output of the S/P register on the Printer CPU and routed to the D-type F/F L18 and buffer L1 on the memory board. The parity bit rejoins the byte at the input to memory. Once the transfer is complete the instruction and byte timing registers on the I/O board are cleared.

4.4.5 PRINTER/PIO MEMORY--DMA READ

A DMA READ commences when the Master CPU issues a 1-BYTE or 256-BYTE READ Header/Instruction byte to the Printer I/O board 7346. The procedure is the same as the DMA write with the Header/Instruction byte start bit being detected and the 8 bits serially loaded into the S/P register and presented to the Instruction register via the Data In (DI) bus. Signal DIS, which occurs after the instruction byte is loaded into S/P and the Header is decoded, clocks the Byte Timing register to INST and DMA R/W appears as a low input to Printer memory. DMA R/W inhibits the memory write strobes at the output of L50 and disables the DI bus at registers L54 and L55. The DMA READ

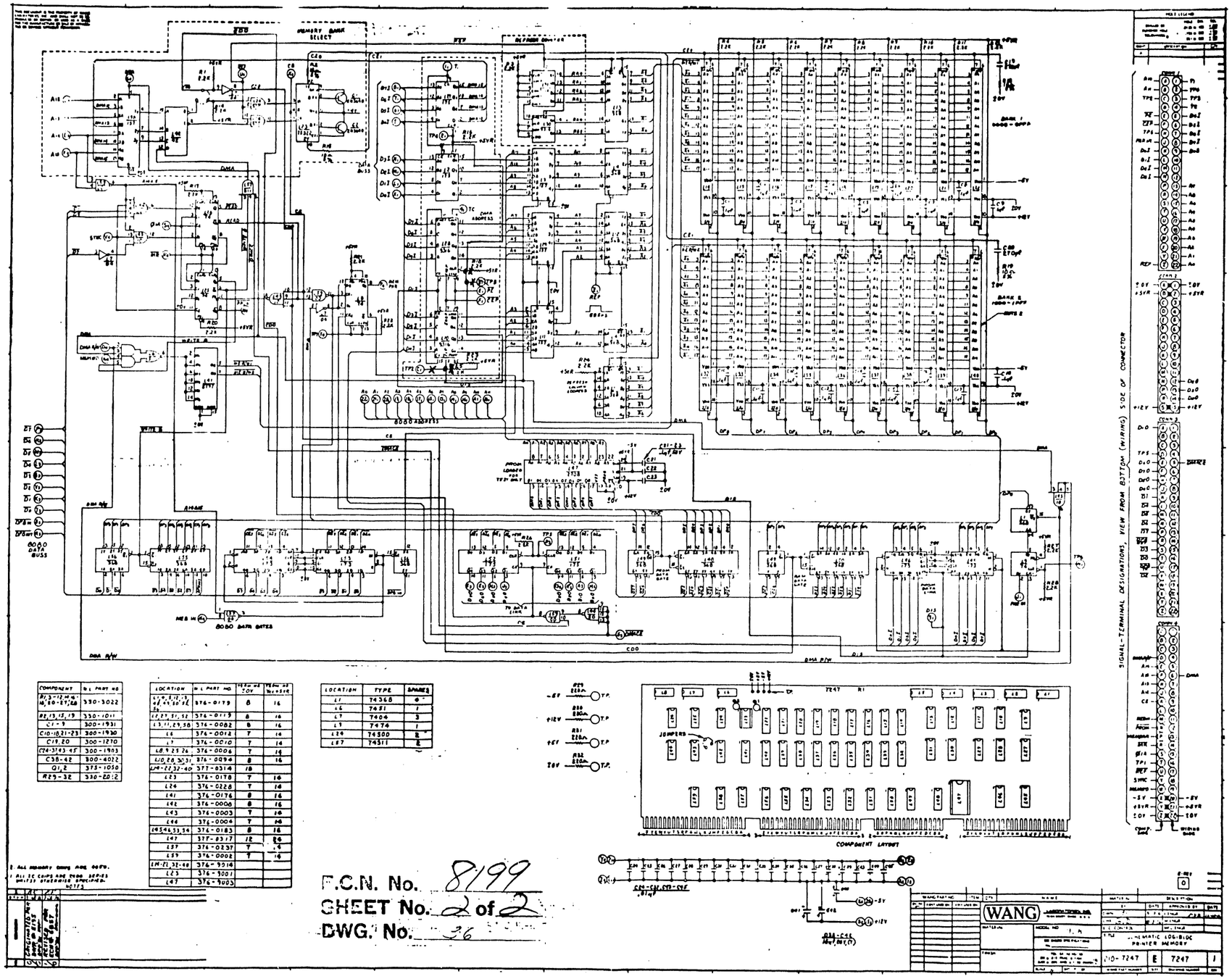
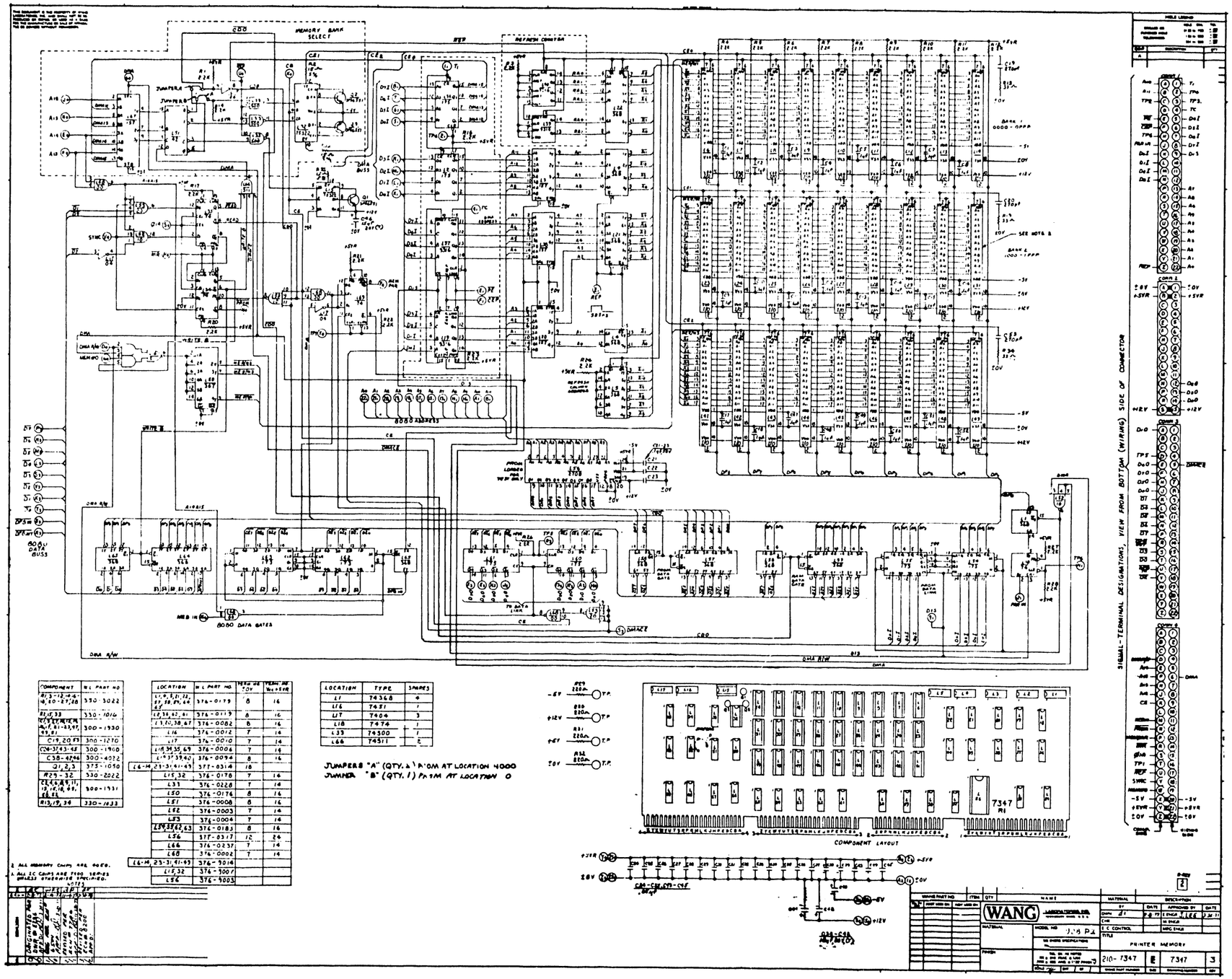


Figure 4-6 Printer Memory-Schematic Illustration — Sheet 1



COMPONENT	W.L. PART NO
R1,3-12,14-16, 18,20-27,28	330-3022
R2,17,33	330-1016
RT1,R4,R5,R7, R13,R31-33,97, 99,81	300-1930
C19,20,F3	300-1270
C24-37,43-48	300-1900
C38-42,44	300-4022
Q1,2,3	375-1050
R29-32	330-2022
CR1,6,8,9,11, 13,16,18,69, CR,RR	900-1931
R13,19,36	330-1033

LOCATION	W.L. PART NO.	TERM. AS 7DV	TERM. AS +5VR
U1,9,21,32, 57,58,59,64 65	376-0179	8	16
U2,34,42,61	376-0119	8	16
U3,10,38,67	376-0082	8	16
U16	376-0012	7	14
U17	376-0010	7	14
U18,35,45,69	376-0006	7	14
U4-8,37,39,40	376-0094	8	16
U4-36,21-31,41-49	377-0314	18	1
U15,32	376-0178	7	14
U33	376-0228	7	14
U50	376-0176	8	16
U51	376-0008	8	16
U52	376-0003	7	14
U53	376-0004	7	14
U54,55,62,63	376-0183	8	16
U56	377-0317	12	24
U66	376-0237	7	14
U68	376-0002	7	14
U4-36,23-31,41-49	376-9014		
U15,32	376-9007		
U56	376-9003		

LOCATION	TYPE	SHARES
U1	74368	4
U16	7431	1
U17	7404	3
U18	7474	1
U33	74300	1
U66	74S11	2

JUMPER8 "A" (QTY. 4) FROM AT LOCATION 4000
JUMPER "B" (QTY. 1) FROM AT LOCATION 0

NOTES
1. ALL MEMORY CHIPS ARE 4096.
2. ALL IC CHIPS ARE 7400 SERIES UNLESS OTHERWISE SPECIFIED.

Figure 4-6 Printer Memory-Schematic Illustration — Sheet 2

address bytes (High Order and Low Order) are latched at T1 and DIS (which occurs at T2). T2 activates DMA permitting a decode of the 4 high DMA address bits for selecting the desired Bank and enabling the address into buffers L4 and L21. The CE signal is the final enable required to access memory and data flows from memory to RAM output buffers L58 and L59. CDO enables the Ram data buffers when the Test Prom is disabled. DMA data is directed to the Data Out (DO) bus via F/F registers L60 and L61. The Data Out bus leads to the data link. Signal*DMACE is generated in the DMA timing section of the I/O board at PHASE 1A time. When*DMACE goes low it produces a high at L53-8. This high NANDed with CE at coincidence enables data accessed from memory onto the DO bus.

4.5 PRINTER/PIO CPU BOARD----7348

4.5.1 GENERAL DESCRIPTION

The PRINTER/PIO CPU board 7348 is used to process data for customer options which include the Daisy Hy-Type II Printer, Matrix (Line) printer or a Photocomposition Input Option (PIO). The PIO interface, Model 5508, consists of a self contained Paper Tape Punch and a "Black Box" Translator containing the same logic boards used for the printers. The CPU contains the 8080 microprocessor with input and output buffers for address and data bus and the standard Status register. Other 8080 support logic includes the system and refresh timing, a parity check circuit and the reset logic. The remaining circuitry is the data link control logic that is shared between the 7348 board and the I/O board 7346.

The DMA 1-Byte and 256-Byte transfer operations for the printer are the same as the workstation. Primarily the printer is a receiver for data to be printed and will be in a REC (Receive) mode most of the time.

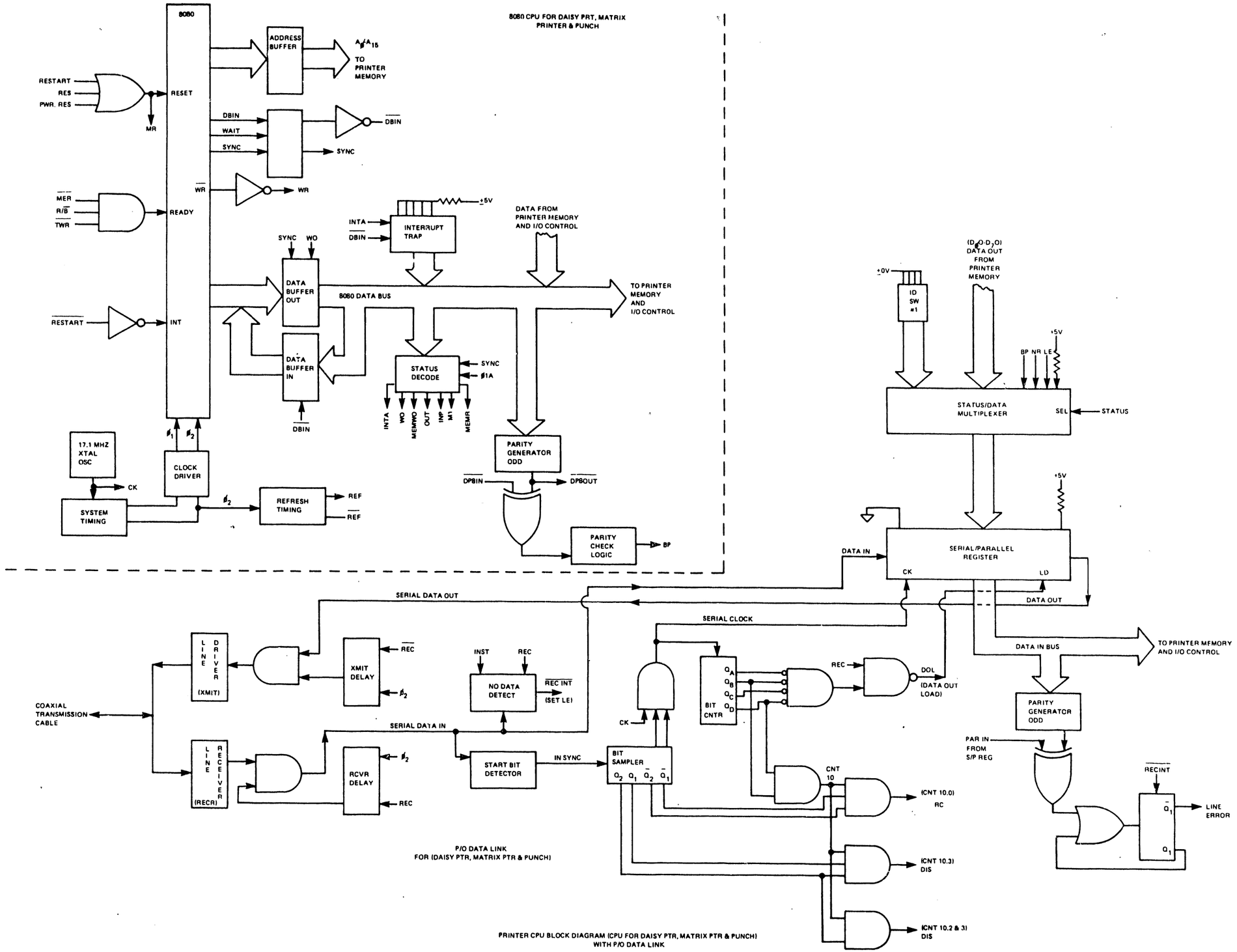


Figure 4-7 Printer CPU-Block Diagram

NOTE:

The following discussion on PRINTER/PIO data link DMA operations will include the data link logic associated with two boards 7346 (I/O BD FOR 928 MATRIX and DAISY PRINTERS and PIO) and 7348 (CPU BD FOR 928 MATRIX and DAISY PRINTERS and PIO).

4.5.2 DMA TRANSFER OPERATIONS-- 1-BYTE STATUS

The STATUS of the printer is checked by the Master prior to any data transfers, as are all slave units. The printer data link transmit and receive mode of operation changes (switch of mode) will automatically set up an inhibit delay for that mode for data transfers to and from the data link. Initially a status check of the printer data link will start with the data link in the idle or receive (REC) state.

The REC mode has a turn around delay of 7 us by preloading the L13 counter with a deficit count of 12 and clearing the 7 us receiver inhibit delay F/F L8 permitting PHASE 2 clocks to increment the counter at L29-11.

After 12 PHASE 2 clocks (7 us) a Carry Out bit enables the delay F/F output L8-6 to go low when set on the next PHASE 2 clock. This low removes the jam clear on the Start Bit Detector F/F L36; disables the PHASE 2 clocks to the counter and enables DATA IN from the Line Receiver L28 to the output of L58-1. The START bit of the status Header/Instruction byte is routed to the start bit detector L36-2 F/F via L35-8.

The start bit (always a 1) will, when detected, be latched by the Start Bit Detector F/F L36 when clocked by signal CK enabling AND gate L19-11 to set the In-Sync F/F L36 on the next CK. The In-Sync F/F output L36-9 is fed back to L35-10 creating a latch up of the Start Bit Detector during the loading of the STATUS word into the S/P register.

In-Sync F/F output L36-8 enables the L37 Bit Sampler F/Fs by removing the clear signal with a high at L56-3. This enables L55-3 to produce clocks at the output of inverter L22-10. The L37 Bit Sampler F/Fs (Gray Counter) will generate four counts 10, 11, 01 and 00 at a 17.1 mhz rate.

At the fourth count of the Bit Sampler 00, a Serial Register Clock (SRC) will be gated at the output of AND gate L54-6 which performs the following functions:

1) Shifts the bits of data into the SERIALIZATION registers L42, L43 and L44.
2) Clocks the Bit Counter L39.
3) Clears the Start Bit Detector L36 when the Bit Counter L39 reaches the binary count of 10 (includes Start bit, 8 data bits and a parity bit loaded into the S/P register).
4) At the bit count of 10 and the Bit Sampler at its second count (11), the output signal DIS (Data In Strobe) at AND gate L52-11 will be active. DIS is used to clock the Byte Timing register on the I/O board 7346 shifting in the signal INST which clocks the STATUS instruction into the instruction register. The STATUS bit issued from the Instruction register at L5-12 gates the Data Link into the "TRANSMIT" mode with a low output at L36-6. The transmit turn around delay of 8 us is initiated.

Another DIS signal is generated at the output of AND gate L20-8 which when ANDed with Header decode signal IS (Instruction Start) and a preset output from F/F L60-9 produces a clock at L41-6. This clock will set the L60 (section 1) F/F generating a*LINE ERROR if the parity bit generator L47-6 output does not compare with the PAR IN bit.

Two one-shot multivibrators L66 are set to time out in approximately 19 us if data is not present on the DATA IN bus during this period. The second one-shot 800 ns pulse NANDed with INST produces

a*RECINT signal that will preset the parity F/F generating LINE ERROR*and initiating a FAULT data link clear*DLCL on the I/O board at L10-6.

Signal*LINE ERROR is used to inhibit the output signal DMA R/W at AND gate L10-11 on the I/O board.

With a bit count of 10 and the Bit Sampler at the fourth count (00), signal (RC) at L20-6 clocks the L60 (section 2) F/F to a reset state enabled by a low REC (Xmitmode) level disabling the parity F/F clock. The Bit Counter is clocked and cleared by a load signal gating a high at the output of NOR gate L38-6.

This high is NANDed with the inverted REC at the input of L56 producing signal*DOL. *DOL enables a parallel load of the STATUS byte into the S/P register by generating a SH/LD clock. Signal DOL at the output of L22-8 is ANDed with STATUS at the output of L62-6 providing a select of the status word via multiplexers L45 and L46 to the parity generator L47. The resultant parity bit is routed to L61-6 output via inverter L27 and gated into the parity bit slot of the S/P register. The STATUS word consists of three status bits and a ID number for identifying the slave unit. SW #1 is used to select the ID. See schematic 7348.

At INST time the status instruction gated the data link into the (XMIT MODE) enabling the Transmit turn around delay logic to time out. Counter L30 was loaded with a deficit count of 14 and L14 F/Fs were cleared. PHASE 2 clocks (14) fill the counter in 8 us producing a Carry Out (CO) that enables the D-type F/F L14 to set. L14-5 enables Data Out to the Line Driver L12 via AND gate L29-8 and enables L53 F/F to reset on the next CK.

L14-6 inhibits the PHASE 2 clocks into the counter and clears the second section of L14 F/F.

The transfer of the STATUS word out of the S/P register to the Master CPU commences when the transmit turn around delay times out and the preset is removed from L53-4.

D-type F/F L53 is reset on the next CK. NAND gate L56-3 is conditioned to go high when L53 is reset allowing the Bit Sampler to count producing the SRC clocks that shift the Status word out of the S/P register.

When the Bit Counter reaches a count of 10 the Bit Sampler continues its count to (11) enabling another DIS clock to shift in T1 time in the Byte Timing register on the I/O board.

The Bit Sampler continues its count to 00 producing the 11th SRC clock which completes the status byte transfer. T1 initiates the STCL*signal on the I/O board used to clear the LINE ERROR F/F L60 and the Data Link Clear*(DLCL).

DLCL*clears the instruction register restoring the printer data link to the REC mode, clears the transmit turn around delay logic enabling L14-8 to be clocked low by DOL which gates a low at the output of L26-11 clearing the S/P register.

4.5.3 PRINTER RESTART

The RESTART Header/Instruction word is used to reset the Printer 8080 CPU and clear the NR (Not Running) status bit. Restart is loaded into the Instruction register in the same manner as discussed above for the Status.

The Restart bit goes active when signal DIS clocks the Byte Timing register after the complete byte has been loaded into the S/P register. Restart clocks the one-shot MV L11-9 output low for a period of 20 us. This pulse is used to clear L18 F/F generating a low

signal out of NAND gate L10-3 that is routed to L63 multiplexer clearing the NR bit. The pulse also is applied to NAND gate L9 causing a reset of the 8080 and a Master Reset*(MR) of all operational registers.

Signal RC is generated when the Bit count is 10 and the Bit Sampler is at count (00). RC is NANDed with RESTART on the I/O board generating*DLCL which terminates the RESTART operation.

4.5.4 PRINTER--256 BYTE WRITE

A 256-BYTE Write for any of the three selected options available with the CPU board 7348 will be identical. The transfer of 256 bytes to be written into memory will be a DMA operation with the DATA LINK in the REC mode. The serial loading of the HEADER/INSTRUCTION byte for a 256-Byte Write is identical to the Status discussion.

At the Bit Count of 10 and the Bit Sampler at count 11, signal DIS at the output of AND gate L52-11 is routed to the I/O board to clock the Byte Timing register L4 which shifts in the INST control bit. INST clocks the 256-Byte Write instruction into the L5 instruction register. The instruction register will issue two high output signals, 256BT and R/W. Each succeeding byte of address and data is serially loaded into the S/P register and made available to the Data In (DI) bus in a parallel format.

A parity check is performed on each byte prior to its transfer from the CPU board. The parity checker/generator L47 checks the Parity for all received and transmitted data. The instruction byte when clocked into the instruction register on the I/O board 7346 by signal INST remains there until the instruction is complete or aborted. A DMA 256-BT signal at the output of OR gate L9-3 is NANDed with INST gating signal*INST R/B at the output of L11-3. This signal is routed to the CPU board enabling L18 F/F to reset at PHASE 2 time

forcing the 8080 into a Busy/Wait state with a low at the output of L20-12. The DMA address bytes (High Order and Low Order) are serially and sequentially loaded into the S/P register and transferred to the memory address registers on board 7347 while DIS shifts T1 and T2 time into the Byte Timing register L4. See memory for details.

The R/W signal is ANDed with LINE ERROR (not active) to produce a high signal DMA R/W at the output of L10-11. The next signal generated is*PE (parallel enable) that requires T1 and not T2 at L39-11. At T2 time signal DMA goes active at L25-11. At T2 and not T3 time a low is gated at the output of L11-6 which ORed with*REC produces an output at L9-11 named CEP. All four signals are routed to memory.

The fourth byte serially loaded into the S/P register is the first data byte to be stored in memory. At bit count 10 and the bit sampler at count 11 signal DIS shifts in T3 time in the Byte Timing register and clocks the Low Order address counter to the next address.

The fifth byte of data at bit count 10 shifts in T4 time and increments the Low Order address counter. The Byte Timing register locks up at T4 time. This procedure continues for the period required to write 255 bytes of data. On the 256th byte of data a carry out from the Low Order address counter on the memory board called Transfer Complete (TC) is NANDed with 256BT, CEA from the DMA Timing logic and R/W producing a*DLCL that terminates the operation.

4.5.5 PRINTER--256-BYTE READ

A 256-Byte READ Header/Instruction byte will be serially loaded and clocked into the instruction register L5 in the same manner as a 256-byte write with signal DIS shifting in INST time. The data link will be in the REC mode only long enough to load the starting address bytes for accessing memory. The High Order address is serially loaded at T2 time during the loading of the High Order and Low Order address

bytes. The T2 condition automatically gates the data link into the Transmit mode when AND gate output L12-8 goes high causing the output at L36-6 to go low. This sets up a READ operation of the printer memory. T1 and T2 Enable signals*PE and*CEP from the I/O board to condition the Low Order Address counter on the memory board. R/W signal is a low for a read operation and is ANDed with LINE ERROR (not active) to gate a low DMA R/W signal to the memory board. Signal DMA is active at T2 time which is the gating signal for accessing 256 sequential memory locations.

REC when gated low at L36-6 on the I/O board is ORed with a low from L11-6 that gates a low signal*SRCL at L9-8. *SRCL clears the S/P register at the output of L62-3.

REC also initiates the 8 us transmit delay by enabling the L30 counter to be filled with PHASE 2 clocks from a deficit count of 14. A carry out after 8 us will enable L14 to set clocking L14-5 high enabling data out at L29-8 to the Line Driver L12 and also releasing the preset on L53 F/F. L53 will reset on the next CK. L14-6 inhibits any more PHASE 2 clocks to the counter.

The reset of L53 F/F enables CK signals at the output of L55-3 to the Bit Sampler F/Fs L37. The F/Fs go through a gray count of four states 10, 11, 01 and 00 producing a SRC clock every 234 ns at the output of L54-6.

Each SRC clock performs the following functions:

1) Shifts data bits of each successive byte read from memory out of the S/P register to the line driver.
2) Clocks the L39 Bit Counter.

When the Bit Counter reaches the count of 10 and the Bit Sampler is at the second count 11, signal DIS is generated at L52-11 shifting in T3 at the Byte Timing register and incrementing the low order address counter. At the bit count of 10 and the fourth count of the

Bit Sampler 00 the eleventh SRC loads the Bit counter with zeroes which generates a high at the output of NOR gate L38-6. This high NANDed with REC produces*DOL at L56-6 loading the next byte of data into the S/P register to be transferred to the disk. This process of accessing printer memory and transmitting the data out of the data link to be written onto the disk is continued until 256 bytes of data have been transferred.

A*DLCL will terminate the 256 byte read operation when the last DOL*is ORed with TCB at L38-6.

4.5.6 PRINTER --1-BYTE WRITE

A 1-BYTE WRITE is used by the Master CPU to write a single byte of data into Slave (Printer/PIO) memory (generally associated with semaphore data).

The Master initiates the 1-Byte transfer by performing a standard memory write except that a memory write to a slave requires that the slave must first be selected and the memory address above 32K. See Master CPU for initiating a 1-Byte write.

The Printer/PIO data link will be in the REC mode for a 1-Byte Write instruction. The 7 us receiver inhibit delay will time out prior to serially loading the Header/Instruction byte.

While serially loading the 1-Byte Write instruction with the bit count 10 and the Bit Sampler at count 11, signal DIS at the output of L52-11 shifts INST into the Byte Timing register L4 on the I/O board.

INST clocks the 1-Byte write instruction into L5 register and the following events occur:

1. The 1BT and R/W outputs from L5 are both ones.

2. 1BT and INST gate a low signal*INST R/B at the output of L11-3. This signal enables the reset of L18 F/F which gates the 8080 into a Busy state with a low at L20-12.

3. If the LINE ERROR is not active when ANDed with R/W, the output signal DMA R/W will be active high at L10-11.

4. R/W is inverted by L23 presenting a low to AND gate L12 which carries through to an OR condition at L9. Status being inactive gates a low at the output of L9-6 which is inverted by NAND gate L36-6 producing signal REC. This high signal routed to the CPU gates the Receive mode of operation.

5. The High Order address is the second byte serially loaded into the S/P register onto the DI bus. At bit count 10 and the bit Sampler at count 11, signal DIS shifts T1 time into the Byte Timing register L4 and T1 is routed to the memory board for clocking the H.O. address into the address registers.

6. The Low Order address is the third byte serially loaded and transferred to the memory address registers.

   (The Low Order address for a 1-Byte Write is a specific address issued by the Master 8080 selected by multiplexers on the Master memory board.)

7. T1 and NOT T2 generate signal*PE at L39-11 which will load the L.O. address into the memory registers on the next clock.

8. AT bit count 10 and the bit sampler at count 11, signal DIS is generated shifting the Byte Timing to T2 time. T2 and 1BT gate signal DMA at the output of L25-11 initiating the write sequence for storing the third byte (Data). T2 and NOT T3 gate a low at the output of L11-6 which carries through L9-11 generating *CEP which enables the L.O. address to be clocked into the registers by DIS clock.

9. The fourth byte is the data byte serially shifted into the S/P register and onto the Data In bus. Signal DIS follows shifting in T3 time. The data byte is enabled onto the memory bus and stored at the designated location.

10. The termination of the 1-Byte Write operation commences when the bit count is 10 and the bit sampler is at count 00 generating signal RC at the output of L20-6. RC clocks the first of two enabled DMA Timing L26 F/Fs. The second F/F is clocked by PHASE 1A which enables a third L40 F/F to be clocked by PHASE 1A providing a CEA signal. CEA is the completion of a 1-Byte Write operation when NANDed with T3, R/W, and 1BT to gate a low at the output of L24-8 clearing the data link*DLCL.

4.5.7 PRINTER--1-BYTE READ

A 1-BYTE READ operation commences with the printer data link in the Receive mode during the loading of the Header/Instruction byte and the high and low order address bytes. At this point in time the operation is identical to the 1-Byte Write with one exception. The instruction register outputs differ. The operation proceeds as follows:

1. At INST time, the instruction is clocked into the instruction register L5 gating outputs R/W (low) and 1BT (high). R/W ANDed with an inactive LINE ERROR gates a DMA R/W signal from L10-11 that is active low.

2. The second byte is the High Order address serially loaded into the S/P register and clocked into the memory address registers at T1 time generated at L4-5.

3. The third byte is the Low Order address byte that is clocked into the memory register counters in the same manner as discussed in the 1-Byte Write. T1 and NOT T2 gate*CE at output L39-11. T2

and 1BT gate DMA active at output L25-11. T2 and NOT T3 gate CEP*at output L9-11 providing the enables for the DIS clock to latch the address byte and shift T2 time into the Byte Timing register.

4. T2 is the enabling signal for the switch from Receive to Transmit mode when NANDed with 1BT and the inverted R/W signal at output L12-8. This high output carries through OR gate L9 to the output of NAND gate L36-6 which is a low REC signal. Signal*SRCL is generated at output L9-8 and routed to L62 on the CPU board for clearing the S/P register.

5. On the CPU board REC goes low in the Transmit mode enabling the 8 us turn around Transmit delay logic. REC also enables the second section of L14 F/F to set gating a low signal from L14-8 that carries through OR gate L26-11, and L62-3 to hold a clear on the S/P register during the 8 us transmit delay.

6. Fourteen PHASE 2 clocks fill the L30 counter providing a Carry Out that enables the first section of L14 to set on the next clock. L30-11 goes high when the counter is full removing the clear signal on the S/P register.

7. L14-5 enables the L29 AND gate for Data Out bits from the S/P register to the line driver L12, as well as enabling L53 F/F to reset.

8. L14-6 inhibits PHASE 2 from clocking the L30 counter and enables the other section of L14-8 to reset inhibiting a clear signal to the S/P register.

9. The reset of L53 provides an enable at the output of NAND gate L56-3 to permit CKs at the output of AND gate L55-3. The clocks enable the Bit Sampler and Bit Counter to count.

10. When the bit count reaches 10 and the Bit sampler is at count 11 another DIS shifts in T3 time at the Byte Timing register. During T3 time the data was not present in the S/P register.

11. At bit count 10 and the bit sampler at count 00 the RC signal at the output of L20-6 clocks the DMA TIMING F/F L26 on the I/O board producing a*DMACE signal that enables the addressed data byte onto the memory Data Out bus into Multiplexers L63 and L64.

12. The eleventh SRC clock clears the Bit Counter (loaded with zeroes) generatihg a high at the output of NOR gate L38-6 which NANDed with REC produces signal*DOL loading the addressed data byte into the S/P register for transmission.

13. A repeat of the bit count produces the SRC clocks to shift the data bits out of the S/P register to the Line Driver L12. At bit count 10 and bit sampler count 11 signal DIS shifts in T4 time. T4 and 1BT are NANDed at the output of L39-8 which is ORed with DOL*to generate a*DLCL that terminates the 1-Byte Read operation.

4.5.8 PRINTER--8080 CPU

The 8080 microprocessor is utilized in the same manner as the Master and Workstation. The address buffers, data buffers and status register are identical to the Master and Workstation.

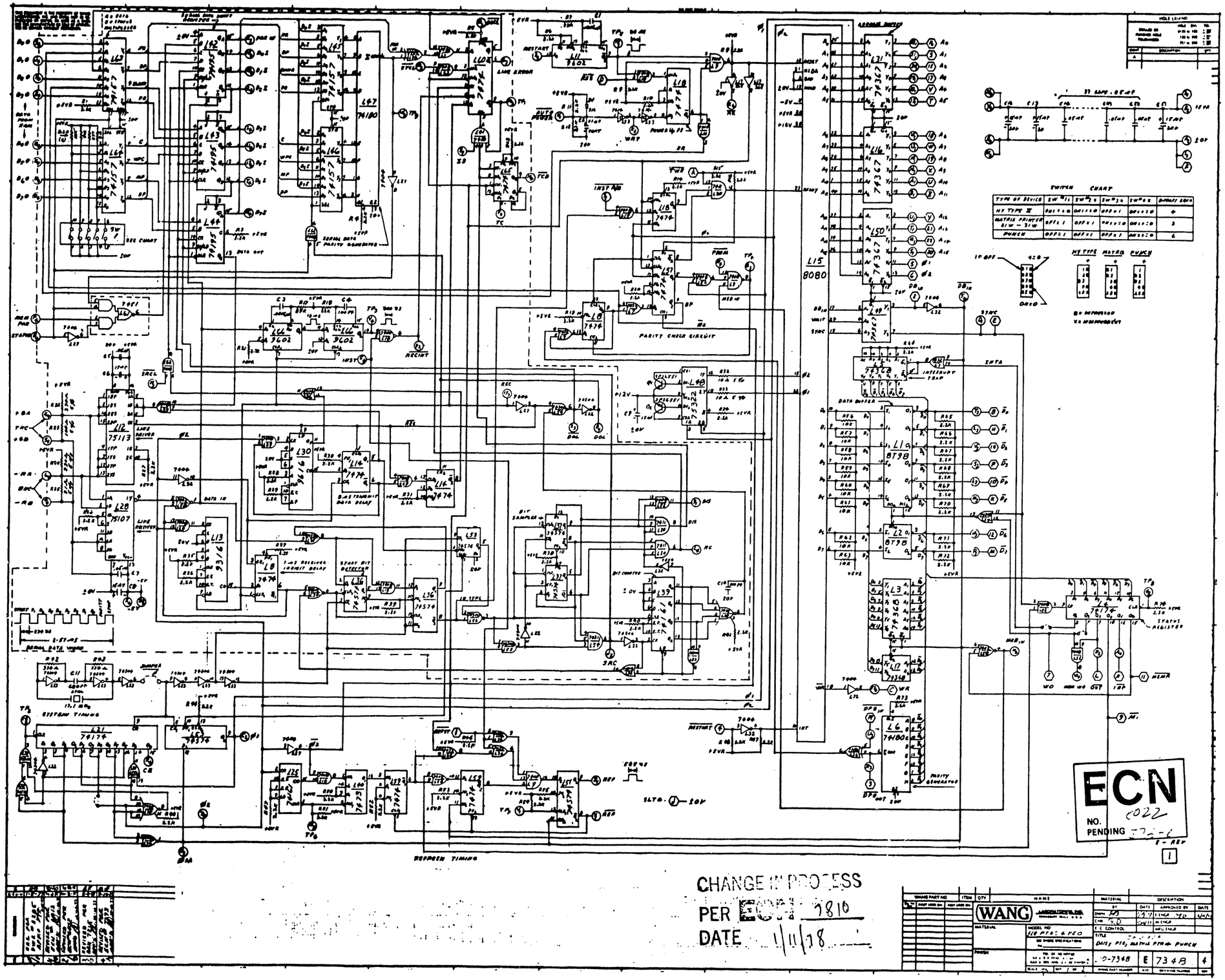
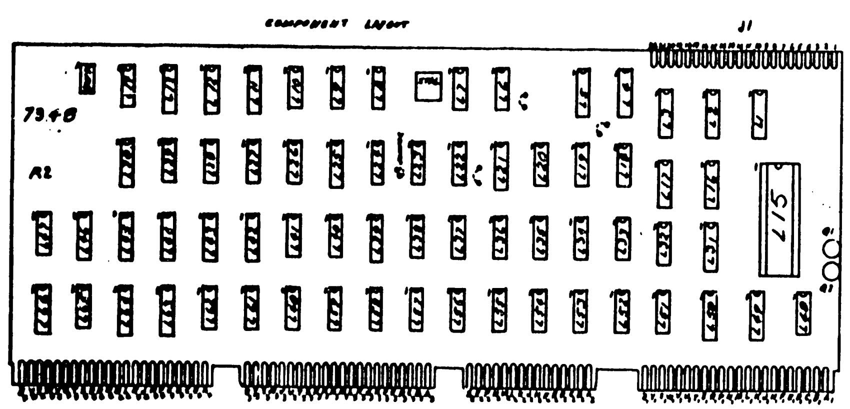
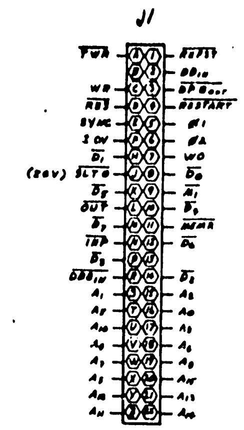
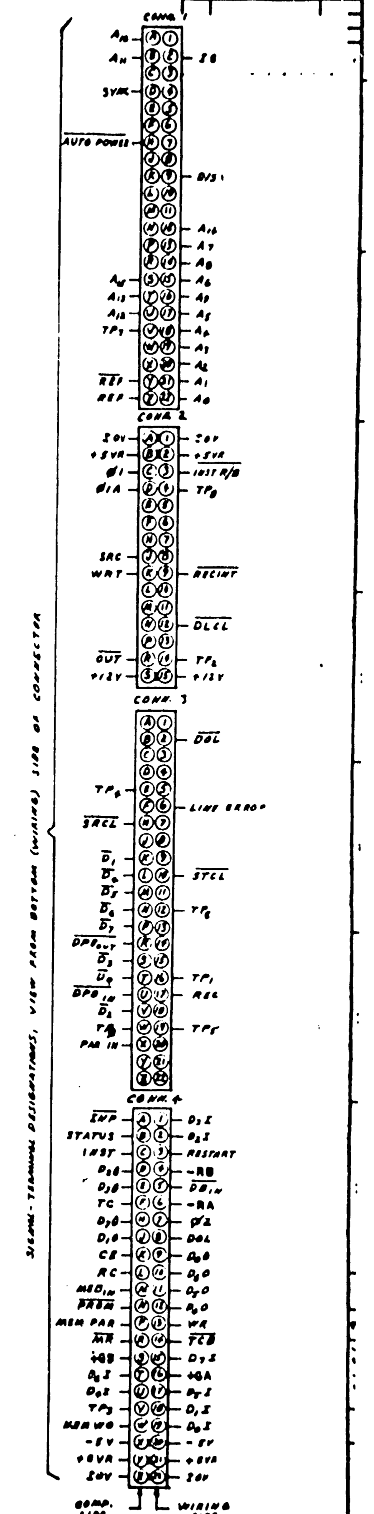


Figure 4-8 Printer CPU-Schematic Illustrations — Sheet 1







I.C. LOCATION	WL PART NO	PIN NO GND	PIN NO +5VR
L1, 2	376-0185	8	16
L3, 5, 17	376-0177	8	16
L4, 21	376-0098	8	16
L6, 47	376-0050	7	14
L7, 26	376-0073	7	14
[illegible]	376-0006	7	14
L9, 41	376-0001	7	14
L10	376-0002	7	14
L11, 66	376-0104	8	16
L12	376-0256	8	16
L13, 25, 30, 39	376-0094	8	16
L15	377-0269	2	20
L16, 31, 49, 50	376-0176	8	16
L18, 29, 52, 62	376-0081	7	14
L20	376-0194	7	14
L22, 23	376-0197	7	14
L24	376-0036	7	14
L35	376-0208	7	14
L27, 32	376-0010	7	14
L28	376-0146	7	14
L33	376-0139	7	14
L34	376-0199	7	14
L36, 37, 54, 53	376-0202	7	14
L38	376-0092	7	14
L40	376-0005	11	4
L42, 43, 44	376-0097	8	16
L45, 46, 63, 64	376-0082	8	16
L48	376-0170	7	14
L57	376-0237	7	14
L55	376-0200	7	14
L56	376-0228	7	14
L58	376-0016	7	14
L61	376-0012	7	14

COMPONENT	WL PART NO
R1-6, 8-11, 13-16, 18, 19, 21, 26-28, 30-44, 46-58, 64-77	330-3088
R7	330-4033
R17	330-4039
R18	330-4022
R22	330-2020
R23	330-2011
R20	330-2040
R25	330-1092
R32, 33	330-1011
R42, 43	330-2033
R55-63	330-4010
R12	330-3033
C1	300-1913
C2	300-4010
C3	300-1907
C4, 10	300-1100
C5, 7, 14-50	300-1900
C6, 8, 9, 12, 13, 51	300-4022
C11	300-1680
SW 1	325-1501
D1	380-1001
Q1, 2	375-1050
XTAL 17.1 MHz	321-0018
LIT 40 PIN SOCKET	376-9011

I.C. TYPE	LOCATION	SPARE
7400	L10	2
74S00	L56	1
7402	L58	1
7404	L27	2
	L32	1
74S04	L22	2
7408	L62	1
74S08	L55	3
7410	L41	2
74S11	L59	2
7414	L33	4
7451	L61	1
7473	L40	1
7486	L39	2
74367	L49	2
74S74	L51	1
74368	L17	2
8T98	L2	2
9602	L11	1

CHANGE IN PROCESS
PER ... 7810
DATE 1/11/78

WANG
CPU FOR DAISY PTR, MATRIX PTR & PUNCH
E 7348 4

Figure 4-8 Printer CPU-Schematic Illustrations — Sheet 2

SECTION 5 WANG OPTIONS

SECTION 5
WANG OPTIONS

5.1 INTRODUCTION

This section presents a limited number of WANG options to the 928 Word Processing System. Only brief statements have been made for the matrix Line Printer Option (LPO) and the Photo Input Option (PIO). However, considerable detailed information has been compiled on the Telecommunications. In any case, this section dealing with the WANG Option will be more fully updated and detailed with the final Volume III edition.

5.2 LINE PRINTER OPTION (LPO) (5521/5531)

The Line Printer Option results in a choice of one of two matrix line printers, Models 5521 and 5531, and a printer interface (270-0391). The interface with either line printer is an option which supplements the daisy printer, offering a faster and greater printing capacity.

This option is furnished with a slightly modified 2221W or 2231W printer mounted on a printer stand with Interface (Part #270-0391) also mounted on the same stand. The Interface and printers have been adapted to the 928 WP System 20 and 30.

The operating specifications for the 5521/5531 printers can be found in the original maintenance manuals for Models 72 (2221W) and 61 (2231W). The manual identification numbers are 03-0027-0 and 03-0029-0 respectively.

5.2.1 928 PRINTER INTERFACE ASSEMBLY (WL #270-0391)

Electrically and mechanically, the LPO Interface assembly differs slightly from the PIO Interface. The interface is assembled to adapt to both printer options (5521/5531). For a more detailed view of the LPO, refer to WPNL #30.

5.3. PHOTOCOMPOSITION INPUT OPTION (PIO)

5.3.1. GENERAL DESCRIPTION

The PIO option (5508) consists of a self-contained paper tape punch and an electronic translator (PIO Interface). These two units produce TTS (TeleTypeSetting Code) punched paper tape for use with any photocomposer accommodating six-level punched paper tape. When the PIO is connected (using a coaxial cable) to a 928 system Master CPU channel output, the electronic translator (Interface) will enable the tape punching operation.

5.3.2. PIO DESCRIPTION AND CODES

Any document that is to be punched onto a phototypesetting tape (Punch Output) is stored on a 928 disk in the form of work station CRT display character codes. The function of the WPS software is to translate the CRT codes to a format suitable for input to the PIO. The present implementation translates the CRT display character codes to 6-level (Tape Channels 0 through 5) TTS codes. The PIO is capable of punching tape at the following rates:

50 Characters per second at 60 Hz.
44 Characters per second at 50 Hz.

A. TTS Codes

There are 64 possible TTS codes along with the keystrokes necessary to produce them. Though most of the TTS codes have a direct Wang equivalent keystroke, some do not. In order to produce these unmatched codes, it is necessary to use a two keystroke sequence. The first keystroke in the sequence can be either an (open bracket) or a (closed bracket); the second keystroke in the sequence designates the desired TTS code.

B. Shift and Unshift

In order to relieve the operator of the time consuming task of inserting shift and unshift codes, the software automatically takes care of all case changes. For example, the sequence "a Wang" will preclude the following TTS sequence; a, space, shift, W, unshift, a, n, g.

C. Illegal Characters

In the process of punching a document, it is possible to encounter characters that do not have an equivalent TTS code. Whenever this happens, the software will punch the visual message "ILLEGAL CHARACTER IN PAGE XXX JUST BEFORE YYYYYYYYY" where XXX is the page number where the illegal character is located and YYYYYYYYY are the ten characters immediately following the illegal character. This should help the operator locate and correct the error. After the message is punched, the job is terminated.

D. For a more detailed view of the PIO refer to WPNL #30.

5.4 TELECOMMUNICATIONS

5.4.1 GENERAL DESCRIPTION (FIGURES 5-1 AND 5-2)

Telecommunications (TC) is supported on the Wang Word Processing System (WWPS) by "black box" single-channel telecommunications processors called Channels. Each Channel has the ability to support a variety of asynchronous and synchronous communication protocols when loaded with the appropriate microcode. This document describes the Channel hardware.

The Channel is a self-contained unit with an integral power supply. It has no operator controls or status indicators except for a power-on light, a light indicating the status of the Data Set Ready modem signal, a button which opens the connection to the Data Terminal Ready modem signal and an ACTIVITY light which is lit during transmission/reception. It attaches to a WWPS master processor by a double coaxial cable. The Channel is connected to the WWPS master processor in a manner similar to that of a workstation or a printer processor. It can be connected to a communications line by either an EIA RS-232-C / CCITT V.24 modem interface or an optional current-loop interface. The Channel also contains an EIA RS-366 / CCITT V.11 interface for the connection to an automatic calling unit (ACU).

The following P.C. boards comprise the Channel:

1)	210-7353	DATA LINK BOARD
2)	210-7354	MEMORY BOARD
3)	210-7355	CPU BOARD
4)	210-7356	MODEM AND ACU INTERFACE BOARD
		OR
	210-7357	CURRENT LOOP INTERFACE BOARD
5)	210-7358	POWER SUPPLY REGULATOR BOARD
6)	210-7359	MOTHERBOARD

Each Channel will be supplied with only one interface board, either a 210-7356 or a 210-7357 board.

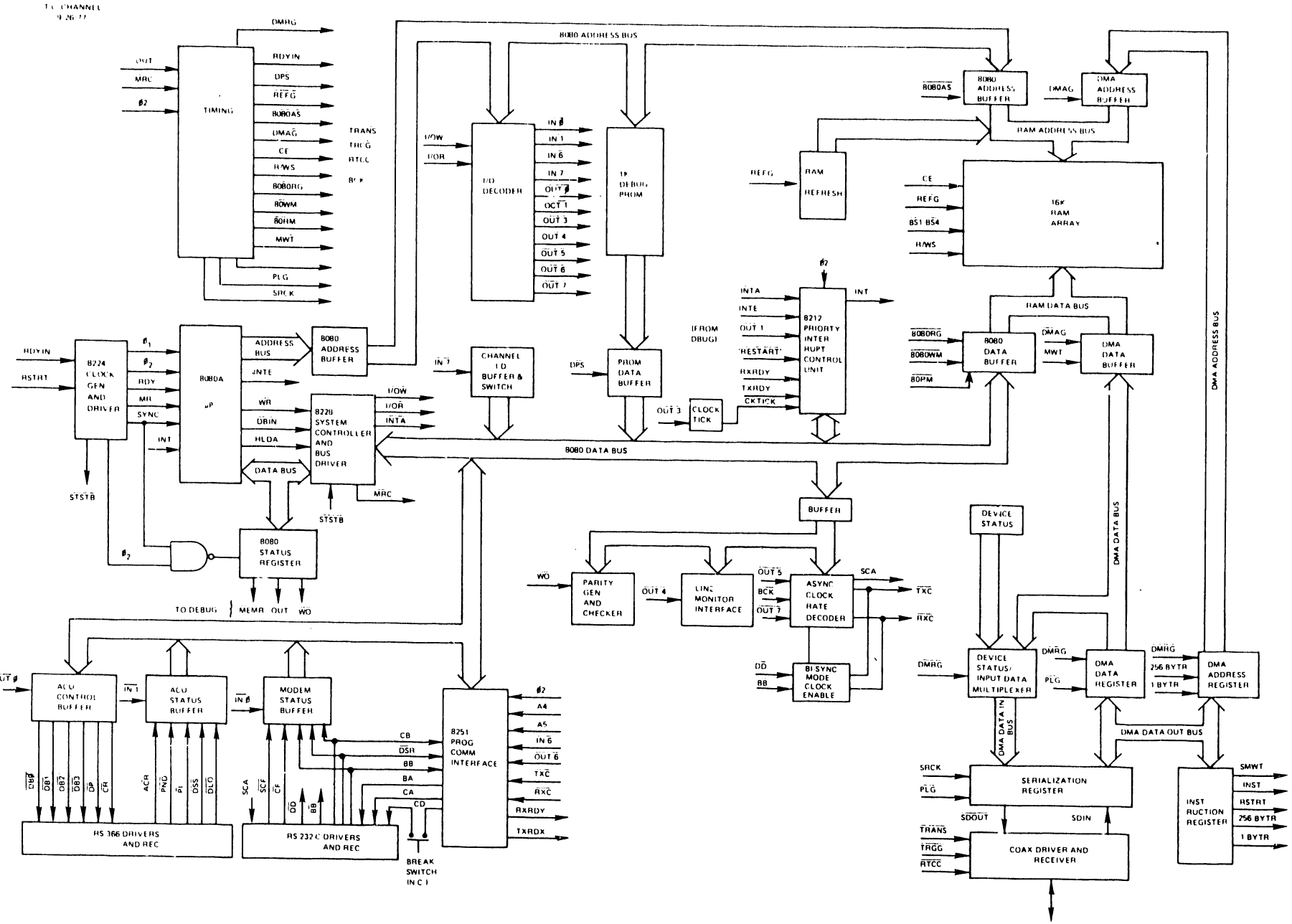


Figure 5-1 T.C. Channel System-Block Diagram

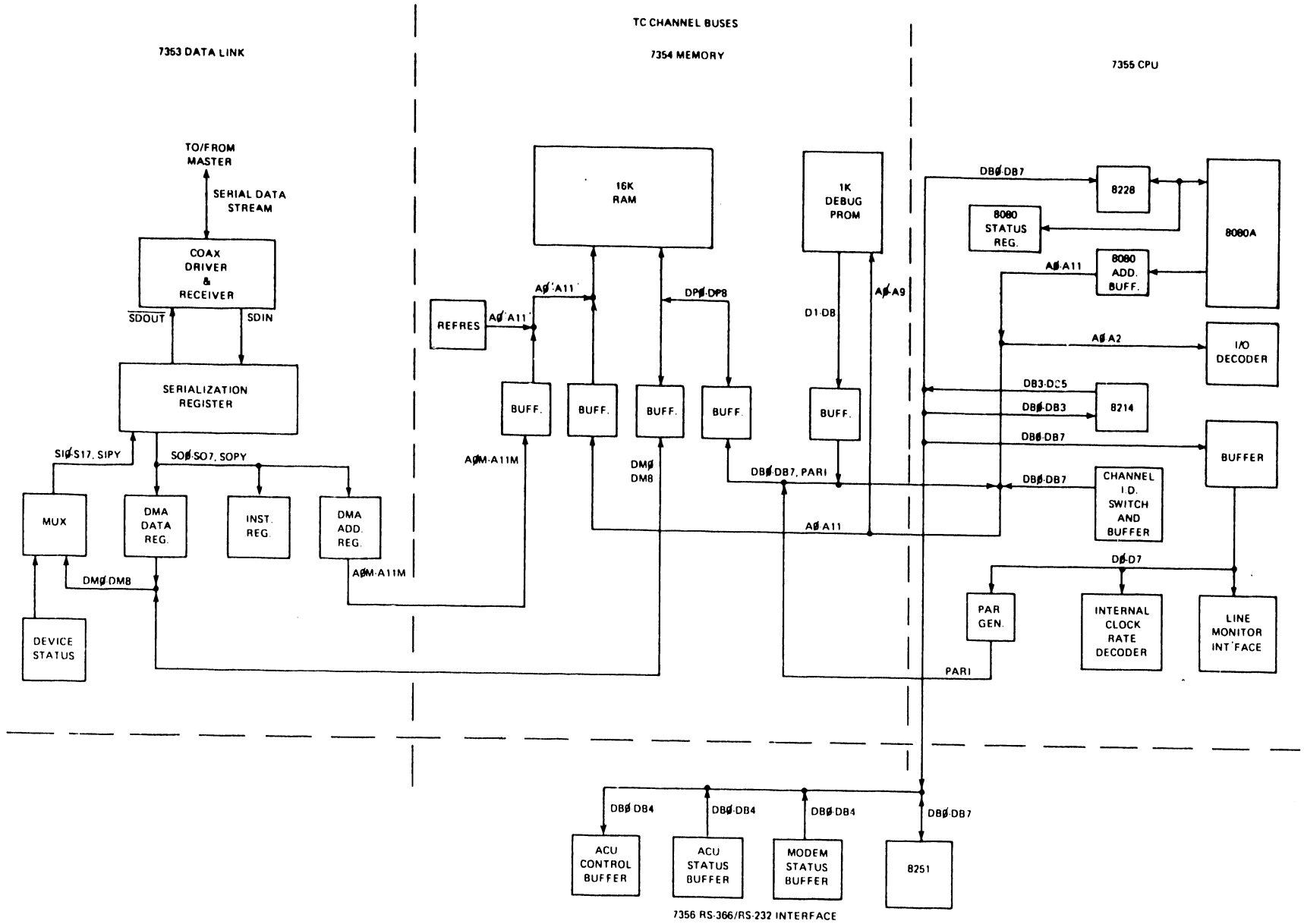


Figure 5-2 T.C. Channel Buses-Block Diagram

5.4.2. INTERNAL ARCHITECTURE (FIGURES 5-1 AND 5-2)

The Channel contains an INTEL 8080 microprocessor with 16K bytes of read/write Random Access Memory (RAM) and 1K bytes of Programmable-Read-Only-Memory (PROM). The origin of the RAM is hex'0000' in the 8080's address space and the origin of the PROM is hex'4000'. The PROM is used for software debugging purposes. The Channel contains a 10 millisecond interval timer, a programmable universal synchronous/asynchronous receiver transmitter (USART, an INTEL 8251 chip), and a clock for controlling transmission timing which can be set to values ranging from 50 to 9600 bits/second (bps). The debug console, interval timer, and the USART transmitter-ready and the receiver-ready conditions can interrupt the 8080.

5.4.3 SYSTEM BUSES (FIGURE 5-2)

The following mnemonics have been used to refer to data carried on internal buses throughout the Channel (please refer to the Channel system block diagram):

A0-A15	:	16 address bits on 8080 address bus
A0M-A14M	:	15 address bits on DMA address bus
$\overline{A0}$'-$\overline{A11}$'	:	12 address bits on RAM address bus
$\overline{D0}$-$\overline{D7}$	:	8 data bits on buffered 8080 data bus
DB0-DB7, PARI,PARO*	:	8 data bits and 1 parity bit on 8080 data bus
DM0-DM8	:	8 data bits and 1 parity bit on DMA data bus
DP0-DP8	:	8 data bits and 1 parity bit on RAM data bus
SI0-SI7, SIPY	:	8 data bits and 1 parity bit on serialization register input data bus
SO0-SO7, SOPY	:	8 data bits and 1 parity bit on serialization register output data bus

Note: PARI (Parity In) is the parity bit used in a 8080 RAM Write operation and PARO (Parity Out) is the parity bit used in 8080 RAM Read operation.

5.4.4 CPU BOARD

5.4.4.1 GENERAL (FIGURE 5-3)

The Channel CPU board contains the 8080 microprocessor (L3) and the related timing and control logic for independent system operation. This board provides the Input and Output commands used to control external devices, interrupt control signals, control and timing signals for 8080 read, write, or RAM refresh cycles, control and timing signals for RAM priority accessing. Please refer to the CPU block diagram.

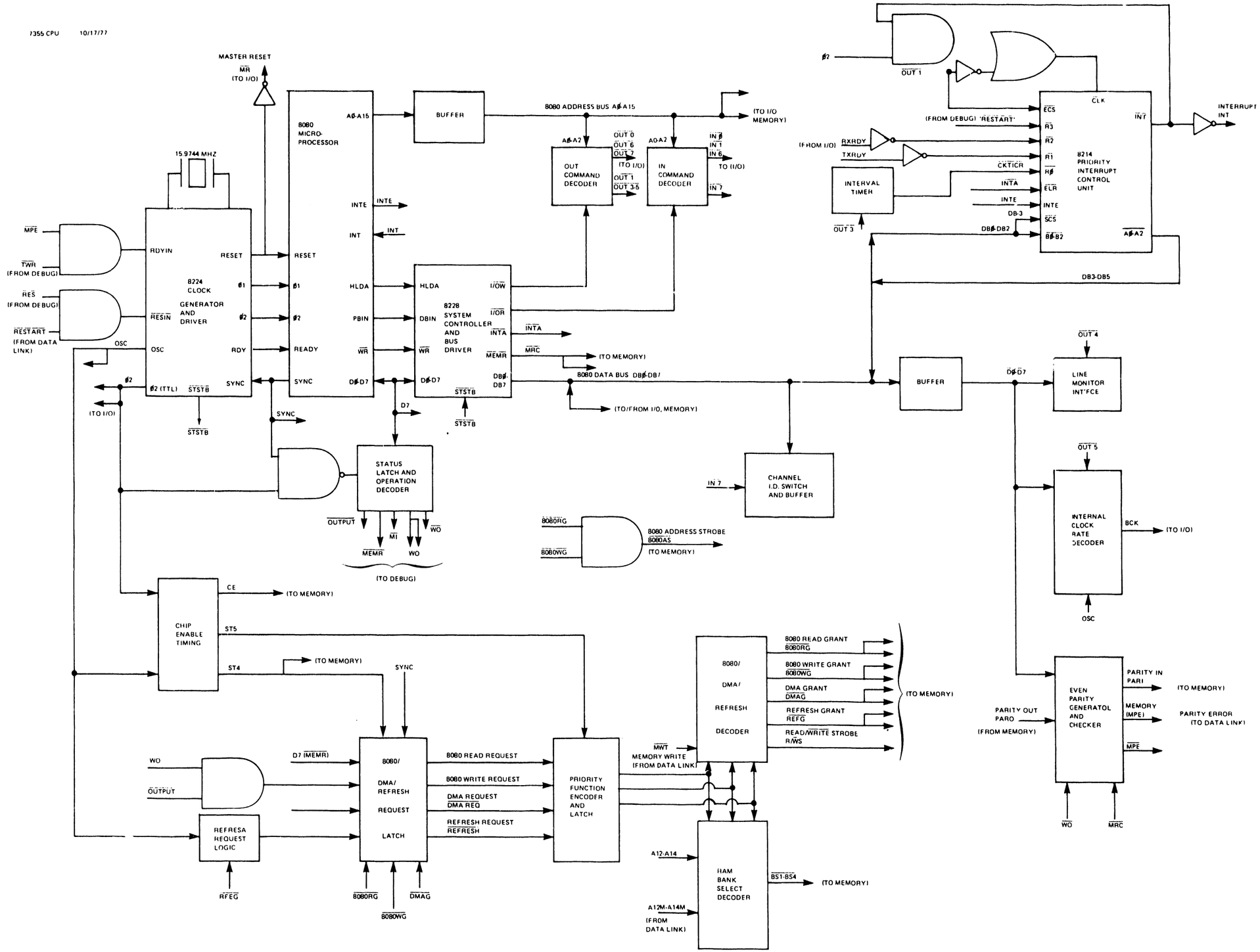


Figure 5-3 T.C. CPU-Block Diagram

The 8080 has a 16-bit 3-state unidirectional address bus (A0-A15) which is connected to non-inverting 3-state buffers that are always enabled. The 8080 also has a 8-bit bidirectional 3-state data bus (D0-D7) which is connected to a System Controller and Bus Driver chip (L2, INTEL 8228 chip) which in turn directly drives the system 8-bit bidirectional 3-state data bus (DB0-DB7). In addition, the 8080 provides and accepts several timing and control signals. Timing for the 8080 is provided by the Clock Generator and Driver chip (L35, INTEL 8224 chip) which uses a 15.9744 MHz crystal to generate the two different phase clocks (Ø1 and Ø2). The following subsections will describe in detail the functional components that comprise the Channel's CPU board.

5.4.4.2 8080 CONTROL AND TIMING LOGIC

A. 8224 CLOCK GENERATOR AND DRIVER

The 8224 chip (L35) is a Clock Generator and Driver chip for the 8080 CPU. It is controlled by a single external crystal whose frequency is 9 times the processor speed. Also included are circuits to provide power-up reset, advance status strobe, and synchronization of ready.

The crystal frequency selected for the 8080 CPU is 15.9744 MHz which provides a processor state time of 563 ns (1.77493 MHz). The Ø1 and Ø2 outputs of the 8224 are high level MOS compatible and are directly connected to the 8080 CPU Ø1 and Ø2 clock inputs The 8224 also supplies a TTL level Ø2 (L35-6) which is used to generate the RAM timing signals and to clock the 8080 Status Latch and Function Decoder (L1). This clock is also provided externally to the Debug unit and to the 8251 on either the 7356 or the 7357 interface board. The 8224 provides a buffered oscillator output (OSC,L35-12) whose frequency is equal to the crystal frequency (period = 62.6 ns). This signal is used to generate timing signals used by the RAM timing logic and by the internal clock rate decoder.

The 8224 synchronizes and provides the RESET and READY control signals to the 8080 CPU. The signals $\overline{\text{RESTART}}$ (from the 7353 data link board) and $\overline{\text{RES}}$ (from the Debug unit) are AND'ed together to generate the RESET input to the 8224 (L35-2). The RESET signal is inverted and provided to the 7356/7357 Interface board as the signal $\overline{\text{MR}}$ (Master Reset) If either signal goes low (active), the 8080 CPU will be reset; that is, the content of the program counter will be cleared and the program will start at location hex'0000' in the RAM. The signals $\overline{\text{MPE}}$ (memory parity error) and $\overline{\text{TWR}}$ (from the Debug unit) are AND'ed together to generate the READY input to the 8224 (L35-3). If either signal goes low (active), the 8080 CPU will enter the WAIT (NOT READY) state until both signals are high again. A parity error detected on the 8080 data bus or the Debug unit single stepping the 8080 CPU will cause the 8080 CPU to enter the WAIT state.

The signal $\overline{\text{STSTB}}$ (Status Strobe) is generated by the 8224 using the SYNC timing signal from the 8080 CPU and several signals internal on the 8224. This signal is provided to the System Controller and Bus Driver chip (8228 chip) and is used to clock the 8080 CPU status information from the 8080 data bus (D0-D7).

B. 8228 SYSTEM CONTROLLER AND BUS DRIVER

The 8228 chip (L2) is a System Controller and Bus Driver chip for the 8080 CPU. It generates all signals required to directly interface the 8080 CPU to RAM, PROM, and I/O components.

An 8-bit, bidirectional bus driver is provided to buffer the 8080 data bus (D0-D7) from the system data bus (DB0-DB7) which interfaces to memory and I/O devices. The bidirectional bus driver is controlled by the input signals $\overline{\text{STSTS}}$ (STATUS STROBE from the 8224), HLDA (HOLD ACKNOWLEDGE), DBIN (DATA BUS IN) and $\overline{\text{WR}}$ (WRITE, all from 8080 CPU), and by an internal gating array in the 8228. The signal DBIN indicates that the 8080 data bus is in the input (read) mode, and the signal $\overline{\text{WR}}$ indicates that the 8080 data bus is in the output (write) mode. The data on the 8080 data bus is stable while the $\overline{\text{WR}}$ signal is low (active). The active high signal HLDA indicates that the 8080 address bus and data bus will go into a high impedance state following a read or write operation.

The signal $\overline{\text{STSTS}}$ is used to clock the 8080 status information which is present on the 8080 data bus at the beginning of each 8080 CPU machine cycle. This status information indicates externally what type of activity will occur during that cycle. The $\overline{\text{STSTS}}$ signal goes low (active) after the falling edge of the Ø2 clock signal in the first processor state time (T1) and the valid 8080 status information is clocked into a internal status latch in the 8228. This status information, along with the signals DBIN, $\overline{\text{WR}}$, and HLDA generates the active low control signals $\overline{\text{I/OW}}$ (OUTPUT WRITE), $\overline{\text{I/OR}}$ (INPUT READ), $\overline{\text{INTA}}$ (INTERRUPT ACKNOWLEDGE), and $\overline{\text{MEMR}}$ (MEMORY READ). The signals $\overline{\text{I/OW}}$ and $\overline{\text{I/OR}}$ are used to enable the Output Command Decoder (L16) and the Input Command Decoder (L15) respectively. The signal $\overline{\text{INTA}}$ is provided to the Priority Interrupt Control Unit chip (INTEL 8214 chip) and the signal $\overline{\text{MEMR}}$ (renamed $\overline{\text{MRC}}$) is provided to Even Parity Generator and Checker logic and to the 7354 memory board

C. 8080 STATUS LATCH AND OPERATION DECODER

A 74LS175 (L1, quadruple D-type flip-flop) is used as a 8080 Status Latch and Operation Decoder. The 8080 status information is present on the 8080 data bus at the beginning of each 8080 CPU machine cycle. This status information indicates externally what type of activity will occur during that cycle. The signals Ø2 and SYNC are NAND'ed together and the output signal (L10-3) is used to clock (L1-9) the 8080 status information into the latch. This causes the status latch to be clocked by the falling edge of the Ø2 clock during the first 8080 CPU state time (T1). The D-inputs of the flip-flops are connected to D1, D4, D5, and D7 bits of the 8080 data bus, and this provides for the following operation decode:

INPUT	OUTPUT	MACHINE CYCLE OPERATION
D1 (L1-13)	$\overline{WO}$ (L1-14) $\overline{WO}$ (L1-15)	MEMORY WRITE or OUTPUT WRITE
D4 (L1-5)	$\overline{OUT}$ (L1-6)	OUTPUT WRITE
D5 (L1-12)	$\overline{MI}$ (L1-11)	INSTRUCTION FETCH
D7 (L1-4)	$\overline{MEMR}$ (L1-3)	MEMORY READ

The signals $\overline{MEMR}$, $\overline{MI}$, and WO are provided to the Debug Unit. The signals WO and $\overline{OUT}$ are provided to generate a 8080 Read Request and the signal $\overline{WO}$ is provided to the Even Parity Generator and Checker logic.

5.4.4.3 OUT COMMAND DECODER

A 7442 (L16, BCD to decimal decoder) is used as an Out Command Decoder. When the signal $\overline{I/OW}$ (L2-27 to L16-12) goes low (active), the Decoder is enabled and the three 8080 address bits A0-A2 are decoded as the Output Commands $\overline{OUT0}$-$\overline{OUT7}$. The significance of the Output Commands are as follows:

$\overline{OUT0}$	Set the ACU Control Signals
$\overline{OUT1}$	Set Interrupt Mask
$\overline{OUT2}$	Output Character to Debug Unit Printer
$\overline{OUT3}$	Clear the Interval Timer Interrupt
$\overline{OUT4}$	Display Character on Line Monitor
$\overline{OUT5}$	Set Internal Clock Rate
$\overline{OUT6}$	Sets 8251 into the Write Mode
$\overline{OUT7}$	Set Secondary Request to Send and USART Clock mode

Output commands $\overline{OUT0}$,$\overline{OUT6}$, and $\overline{OUT7}$ are provided to either the 7356 or the 7357 interface board. $\overline{OUT1}$ is provided to the Priority Interrupt Control Unit (8214); $\overline{OUT2}$ is provided to the Debug Unit; $\overline{OUT3}$ is provided to the Interval Timer (clock tick); $\overline{OUT4}$ is provided to the Line Monitor Interface; $\overline{OUT5}$ is provided to the Internal Clock Rate Decoder

5.4.4.4 IN COMMAND DECODER

A 7442 (L15, BCD to decimal decoder) is used as an IN Command Decoder. When the signal $\overline{I/OR}$ (L2-25 to L15-12) goes low (active), the Decoder is enabled and the three 8080 address bits A0-A2 are decoded as the Input Commands $\overline{IN0}$, $\overline{IN1}$, $\overline{IN6}$, $\overline{IN7}$. The significance of the Input Commands are as follows:

$\overline{IN0}$	Read Modem Status Signals
$\overline{IN1}$	Read ACU Status
$\overline{IN6}$	Sets 8251 into the Read Mode
$\overline{IN7}$	Sense Channel ID Switches

Input commands $\overline{IN0}$, $\overline{IN1}$, and $\overline{IN6}$ are provided to either the 7356 or the 7357 interface board. $\overline{IN7}$ is provided to the Channel ID Switch Buffer.

5.4.4.5 CHANNEL ID SWITCHES AND BUFFER

A set of eight Channel ID Switches and two 74 LS367 (L23 and part of L34, 3-state bus drivers) are used to provide a Channel ID for software purposes. When the Input Command $\overline{IN7}$ (L15-9 to L23-1,15 and L34-15) goes low (active), the 74 LS367's are enabled and the switches information is gated onto the 8080 data bus (DB0-DB7). The switch polarity is inverted with the ON position being read as a "0" and the OFF position being read as a "1". The 8080 IN7 instruction and required data is formatted as follows:

INSTRUCTION	
IN	X'07'

DATA								
SW 8	SW 7	SW 6	SW 5	SW 4	SW 3	SW 2	SW 1
MSB							LSB

5.4.4.6 LINE MONITOR INTERFACE

A 16-pin IC connector (J1) provides the Line Monitor Interface. The IC connector is connected to the buffered 8080 data ($\overline{D0}$-$\overline{D7}$). This bus is buffered from the 8080 data bus (DB0-DB7) by two 74 LS368's (L25 and part of L36, 3-state inverting bus drivers) which are always enabled. The Line Monitor has the display characteristics of a 2200 system CRT. When the Output Command $\overline{OUT4}$ (L16-5 to J1-2) goes low (active), the Line Monitor will input an ASCII character from the buffered 8080 data bus ($\overline{D0}$-$\overline{D7}$). In addition to displaying the ASCII graphic characters, it also responds to the following control characters:

X'0A'	Line Feed
X'0D'	Carriage Return
X'01'	Cursor Home
X'03'	Clear Screen

The 8080 OUT4 instruction and required data is formatted as follows:

INSTRUCTION		
OUT	X'04'	

DATA
ASCII CHARACTER
MSB LSB

5.4.4.7 INTERNAL CLOCK RATE DECODER

A Internal Clock Rate Decoder is used to provide, in certain transmission modes, transmitter/receiver timing signals to the USART on either the 7356 or 7357 interface board. The D-inputs of two 74175's (L27 and L37, quadruple D-type flip-flops) are connected to the buffered 8080 data bus ($\overline{D0}$-$\overline{D7}$) and they are clocked by the rising edge of the Output Command signal $\overline{OUT5}$. The $\overline{Q}$ outputs of these flip-flops are connected to the A, B, C, and D (preset) inputs of two 74161's (L28 and L38, synchronous 4-bit counter) These two counters are configured as a synchronous 8-bit counter with its preset inputs comimg from $\overline{D0}$-$\overline{D7}$ with $\overline{D0}$ as the LSB. The 1.2288 MHz (814 ns) counter clock, $\overline{BCK}$, is derived from L31-11 by dividing the oscillator output of the 8224 (L35-12), OSC, by 13. Half of a 7473 (L42, dual J-K flip-flop) is used to provide the final USART clock signal, BCK (L42-9) to either the 7356 or 7357 interface board. L42 is used as a toggle flip-flop which is toggled by the carry-output (L38-15) of the counter. This carry-output also presets (loads) the counter. The USART clock rate can be set to 1 of 256 values depending upon the preset data.

The 8080 OUT5 instruction and required data is formatted as follows:

INSTRUCTION		
OUT	X'05'	

DATA
CLOCK RATE SELECT CODE
MSB LSB

This Output Command will set the bits/sec rate of the internal clock. In the asynchronous transmission mode, the clock rate will be set to 16 or 64 times the desired transmission speed, while in the synchronous transmission mode (only if external timing is not provided), the clock rate will equal the transmission speed. This is why the Clock Rate Select Code is different for the two transmission modes. (Refer to Table 5-1.)

TABLE 5-1
CLOCK RATE SELECTION CODE

CLOCK RATE	ASYNC CLOCK RATE SELECT CODE	USART CLOCK DIVIDER	SYNC CLOCK RATE SELECT CODE
50	X'40'	64	
75	X'80'	64	
100	X'A0'	64	
110	X'A9'	64	
134.5	X'B9'	64	
150	X'C0'	64	
200	X'D0'	64	
300	X'E0'	64	
600	X'C0'	16	
1200	X'E8'	16	
1800	X'EB'	16	
2400	X'F0'	16	
		1	X'01'
3600	X'F6'	16	
4800	X'F8'	16	
		1	X'80'
7200	X'FB'	16	
9600	X'FC'	16	
		1	X'C0'

5.4.4.8 EVEN PARITY GENERATOR AND CHECKER

An Even Parity Generator and Checker circuit is provided to generate and check a parity bit from the 8080 buffered data bus $\overline{D0}$-$\overline{D7}$. It generates a even parity bit PARI (Parity In) which is written to the RAM during a 8080 Write operation and it checks the parity bit PARO (Parity Out) which is read from the RAM during a 8080 Read operation . A 74180 (L26, 8-bit odd/even parity generator/checker) has its 0-7 inputs connected to $\overline{D0}$-$\overline{D7}$.

The selection of the operation of either a parity generator or a checker is controlled by Write Output signal ($\overline{WO}$) from the 8080 Status Latch and Function Decoder (L1-15). This signal, along with the signal PARO is inputed to both a 7408 (L12, AND gate) and a 7400 (L13, NAND gate). L12-8 is connected to the Odd input of the 74180 (L26-4) and L13-8 is connected to the Even input (L26-3). When the 8080 is performing a Write operation, $\overline{WO}$ will be low (active), causing L12-8 to drive low and L13-8 to drive high. In this mode, the 74180 will generate a even parity bit, PARI, at its Odd Out output (L26-5). PARI is provided to the 7354 Memory board and to the Debug Unit. When the 8080 is performing a Read operation, $\overline{WO}$ will be high (disabled), causing the PARO input to L12 and L13 to be gated through to the 74180. In this mode, PARI going high (active) is used to indicate a parity error. PARI is connected to L33-12, the D-input of a 7474 (L33, dual D-type flip-flop). L33 is clocked by the rising edge of the signal $\overline{MRC}$ (Memory Read) from the 8228 (L2-24). This occurs after the 8080 data is read. The Q output (L33-9) provides the active high signal MPE (Memory

Parity Error) to the 7353 Data Link board and the Q output (L33-8) provides the active low signal MPE to L12-13 for the Ready logic to the 8224. This flip-flop can be cleared by either signal RESTART (from the Data Link board) or DPS (Debug Prom Selected, from the Memory board) going low (active).

5.4.4.9 INTERVAL TIMER

A Interval Timer is provided to supply "CLOCK TICK" interrupt request to the Priorty Interrupt Control Unit (8214) every 10 milliseconds. In this way, the 8080 CPU is able to time events, such as transmission time-outs.

The Interval Timer consists of a 555 (L11, timer) which is set for a period of 10 ms. The output of the Timer (L11-3) is connected to one input of two crossed-coupled 7400 gates (L10, NAND), which is a simple RS flip-flop. The other input of the RS flip-flop is connected to the Output Command signal OUT3, which when issued has the effect of clearing the Interval Timer interrupt request. The output of the RS flip-flop (L10-11) produces the Clock Tick signal CKTICK which is connected to the 8214 (L24-15). The 8080 OUT3 instruction is formatted as follows:

INSTRUCTION	
OUT	X'03'

5.4.4.10 8214 PRIORITY INTERRUPT CONTROL UNIT

The 8214 (L24) is a Priority Interrupt Control Unit chip which provides for an eight level priority interrupt scheme. The 8214 can accept eight requesting levels; determine the highest priority, compare this priorty to a software controlled current status register and issue an interrupt to the 8080 CPU along with vector information to identify the service routine.

An interrupt request is generated by four conditions for the 8080 CPU. If all enabled interrupt requests are simultaneously present, the one having the highest priorty will be taken. Interrupting conditions in order of highest priority are:

A. 'RESTART' : The restart button on the Debug Unit is pushed.

B. RXRDY : The Receiver Ready condition occurs when a complete character is received by the USART. Receive Enable of the USART must be ON for the condition to occur, and therefore functions as a selective enable for the interrupt. The interrupt request condition is cleared by either reading the received data character from the USART or by turning the Receive Enable OFF.

C. $\overline{\text{TXRDY}}$: The Transmitter Ready condition occurs when the USART transmitter gains buffer space to input a character for transmission. The transmitter is double buffered and can input a character while the previous character is being transmitted. Transmit Enable of the USART must be ON for the condition to occur, and therefore functions as a selective enable for the interrupt. The interrupt request condition is cleared when a character is output to the transmitter or by turning the Transmit Enable OFF.

D. $\overline{\text{CKTICK}}$: The interval timer, a free running clock, generates a "clock tick" interrupt request.

An Interrupt Mask is used to define which interrupt conditions are enabled. The Output Command $\overline{\text{OUT1}}$ is used to output the interrupt mask to the 8214. The 8080 OUT1 instruction and required data is formatted as follows:

INSTRUCTION	
OUT	X'01'

DATA
INTERRUPT MASK
MSB LSB

INTERRUPT MASK CODE	ENABLED CONDITIONS			
	DEBUG	RECEIVE	TRANSMIT	CLOCK
X'0F'	X	X	X	X
X'07'	X	X	X	
X'06'	X	X		
X'05'	X			

The Output Command signal $\overline{\text{OUT1}}$ has two functions. It is connected to the $\overline{\text{ECS}}$ input (L24-23), and when this input goes low (active), the Mask is set by the bits supplied from the 8080 data bus bits DB0-DB3. DB0-DB2 are connected to the Current Status ($\overline{\text{B0}}$-$\overline{\text{B2}}$) inputs and DB3 is connected to the Status Group Select ($\overline{\text{SGS}}$) input of the 8214. The signal $\overline{\text{OUT1}}$ is also used to either clear a false Interrupt signal $\overline{\text{INT}}$ that might be present after the power-up sequence or to clear the Interrupt signal after it has been serviced. It is gated with the 8214 clock logic.

The four interrupt request signals mentioned above are connected to Request Level inputs of the 8214 as follows (the $\overline{R0}$ input has the lowest priority level. :

$\overline{R3}$ (L23-18) -'$\overline{RESTART}$' (Debug Unit)

$\overline{R2}$ (L23-17) - $\overline{RXRDY}$ (7356/7357 Interface board)

$\overline{R1}$ (L23-16) - $\overline{TXRDY}$ (7356/7357 Interface board)

$\overline{R0}$ (L23-15) - $\overline{CKTICK}$ (10 ms Interval Timer)

The clock signal provided to the 8214 (L7-3 to L24-6) inorder to clock its internal Interrupt flip-flop is the Ø2 clock signal which is disabled by the Interrupt signal $\overline{INT}$ going low (active). The 8080 control signal INTE (Interrupt Enable) is AND'ed with the signal $\overline{TEA}$ from the Debug Unit to produce the INTE input to the 8214 (L41-6 to L24-7). This is an active high signal that allows the 8214 to clock out an Interrupt signal ($\overline{INT}$).

As soon as one of the four request lines goes low (active), if that request is enabled by the Interrupt Mask, and if the interrupts are enabled by the active high signal INTE (Interrupt Enable), the signal $\overline{INT}$ (L24-5) will go low (active) on the rising edge of the next Ø2 clock input signal. The signal $\overline{INT}$ is gated to the 8214 clock logic and will disable any further Ø2 clock signals from clocking the 8214 until a $\overline{OUT1}$ is issued. This also causes the 8214 to keep the $\overline{INT}$ signal low until the $\overline{OUT1}$ is issued. This signal indicates to the 8080 CPU that a system interrupt has occured.

After the interrupt request is accepted by the 8214, the $\overline{A0}$-$\overline{A2}$ outputs of the 8214, which are connected to the DB3-DB5 bits of the 8080 data bus, are used to encode the special RESTART instruction RST which causes the program counter of the 8080 CPU to point to the location of the interrupt service routine. The RST instruction is similiar to a CALL instruction, and as such, the completion of the instruction stores the old program counter contents on the STACK. The 8080 acknowledges the interrupt by setting the Interrupt Acknowledge signal $\overline{INTA}$ low (active) from the 8228 (L2-23), which is connected to the $\overline{ELR}$ input of the 8214 (L24-11). This disables the $\overline{A0}$-$\overline{A2}$ outputs of the 8214. The control signal INTE will go low, thus disabling any further interrupts until the signal is set high (active) again by the software.

5.4.4.11 MEMORY TIMING

The Memory Timing logic provides the timing and control for accessing the Channel's memory, either RAM or PROM. In the case of the RAM, three operations may take place, a 8080 CPU READ/WRITE, DMA (Master CPU) READ/WRITE, or a RAM Refresh. Inorder to avoid problems of contention, that is two or more memory operations trying to occur simultaneously, the requests for these particular operations must be arranged in a priority sequence. This logic performs that function along with providing the proper memory timing signals. The concept of 8080 "Cycle Stealing" is used here. During any 8080 CPU state time in which a 8080 Read/Write operation is not occurring, a DMA or Refresh operation can take place and "steal" that particular state time for its own operation. In effect, a DMA or Refresh operation can occur during any unused state time, which will not slow the 8080 CPU's instruction execution time. In this manner the system's overall speed is maximized.

The basic timing signals are generated by a 74164 (L20, 8-bit shift register). The serial input of the 74164 (L20-1) is connected to the Ø2 clock signal (L35-6). The clock input of the 74164 (L20-8) is connected to the OSC clock signal (L35-12). The parallel outputs (Q2, Q4, Q5) represent the Ø2 clock signal shifted by half-multiples of the OSC clock's period (62.6 ns). The output signals used and the phase shifts are:

SIGNAL	SHIFT (NS)
ST2 (L20-4)	93.9
ST4 (L20-6)	219.1
ST5 (L20-10)	281.7

A. CHIP ENABLE (CE)

The Chip Enable signal CE (L29-9) provided to the 7353 Memory board is generated by a 74S74 (L29, D-type flip-flop). The preset input (L29-10) is connected to the ST2 signal and the clock input (L29-11) is connected to the ST4 signal. This causes the Q output (L29-9) to produce an active high CE signal during each 8080 CPU state time. The CE signal goes high (active) with the falling edge of the ST2 signal, and goes low with the rising edge of the ST4 signal. Since the CE signal is essentilly a free running signal ocurring during every state time, the RAM Bank Select Decoder will determine if a valid RAM memory operation will take place for each CE signal.

B. 8080/DMA/REFRESH REQUEST LATCH

Two 74S74's are used as a 8080/DMA/REFRESH Request Latch (L8 and L9, D-type flip-flops). Their purpose is to store the four different memory access requests, which are in order of priority:

1. 8080 READ
2. 8080 WRITE

3. DMA READ/WRITE
4. REFRESH

The 8080 Read Request is provided by connecting the signal D7 (L34-5), which is the MEMR (Memory Read) 8080 status bit, to the 1D input of the 8080 Read Request latch (L8-2). The $\overline{Q1}$ output (L8-6) produces the latched request signal. The clock signal for the latch (L21-3 to L8-3) is produced by ANDing the signals SYNC and ST4, which stores the request on the rising edge of ST4. The latch is cleared by the 8080 Read Grant signal ($\overline{8080RG}$) which indicates that the request has been accepted and the 8080 Read RAM/PROM operation will occur.

The 8080 Write Request is generated by ANDing the 8080 status signals WO (Memory/Output Write) and $\overline{OUT}$ (Output Write) which produces a active high signal indicating a 8080 Memory Write operation will take place. This signal is connected to the 2D input (L41-3 to L8-12) of the 8080 Write Request latch. The Q2 output (L8-9) produces the latched request signal. The clock signal for the latch (L22-12 to L8-11) is produced by NANDing the signals SYNC and ST4, which stores the request on the falling edge of ST4. The latch is cleared by the 8080 Write Grant signal ($\overline{8080WG}$) which indicates that the request has been accepted and the 8080 Write RAM operation will occur.

The DMA Read/Write Request signal ($\overline{DMAR}$) is supplied from the 7353 Data Link board. It is connected to the D1 input (L9-2) of the DMA Read/Write Request latch. The Q1 output (L9-5) produces the latched request signal $\overline{DMAREQ}$. The latch is clocked by the rising edge of ST4 (L43-5 to L9-3). The latch is cleared by the DMA Read/Write Grant signal ($\overline{DMAG}$) which indicates that the request has been accepted and the DMA Read/Write memory operation will occur.

The Refresh Request signal generated from the OSC clock signal. The OSC signal is first divided by 13 (L31), then by 8 (L44), and finally by 2 (L42) to produce a 13 microsecond active low Refresh Request signal. It is connected to the D2 input (L9-12) of the Refresh Request latch. The $\overline{Q2}$ output (L9-8) produces the latched request signal $\overline{REFRESH}$. The latch is clocked by the rising edge of ST4 (L43-5 to L9-11). The latch is cleared by the Refresh Grant signal ($\overline{REFG}$) which indicates that the request has been accepted and the RAM Refresh operation will occur.

C. PRIORITY FUNCTION ENCODER AND LATCH

A Priority Function Encoder (L19) and Latch (L18 and L29) are used to determine the priority of the requests from the 8080/DMA/REFRESH Request Latch. A 74148 (L19, 8-line-to-3-line priority encoder) is used to encode the request priorities. The 8080 Read Request is assigned the highest priority (L8-6 to L19-4); next is the 8080 Write Request (L10-8 to L19-3); next is the DMA Read/Write Request (L9-5 to L19-2), and the lowest priority is for the Refresh Request (L9-8 to L19-1). The 8080 Write Request can be inhibited by the $\overline{TWR}$ signal from the Debug Unit going low (active).

The A0-A2 outputs of the Priority Encoder represent the binary three bit code (octal) of the highest priority input. The highest priority is a octal 000 and the lowest priority is a octal 011. These outputs are latched onto three 74S74's (L18 and L29, D-type flip-flops) by the rising edge of the ST5 signal. The Q outputs are decoded into the corresponding Request Grant, Read/Write Strobe (R/$\overline{WS}$), and RAM Bank Select signals ($\overline{BS1}$-$\overline{BS4}$).

REQUEST	A2	A1	A0
8080 READ	0	0	0
8080 WRITE	0	0	1
DMA	0	1	0
REFRESH	0	1	1

D. 8080/DMA/REFRESH DECODER

A 74155 (L17, 2-line-to-4-line decoder) is provided to decode the A0-A2 output signals (encoded highest priority Request) of the Priority Encoder and Latch into the corresponding Operation Grant signal. The 8080 Read Grant ($\overline{8080RG}$), 8080 Write Grant ($\overline{8080WG}$), DMA Grant ($\overline{DMAG}$), and Refresh Grant ($\overline{REFG}$) signals are provided to the 7354 Memory board to provide the control signals for these operations. The $\overline{DMAG}$ signal also goes to the 7353 Data Link board. An additional signal, 8080 Address Strobe ($\overline{8080AS}$) is provided to the 7354 Memory board, which is generated by ANDing the signals $\overline{8080RG}$ and $\overline{8080WG}$ together.

E. READ/WRITE LOGIC

A 74153 (L30, 4-line-to-two-line multiplexer) is used to generate a Read/Write Strobe (R/$\overline{WS}$) from the A0-A2 output signals (encoded highest priority Request) of the Priority Encoder and Latch for the 7354 Memory board. The R/$\overline{WS}$ is as follows (1= READ and 0= WRITE):

REQUEST	A2	A1	A0	R/WS
8080 READ	0	0	0	1
8080 WRITE	0	0	1	0
DMA	0	1	0	$\overline{MWT}$
REFRESH	0	1	1	

The state of the R/$\overline{WS}$ for a DMA operation depends on the state of the Memory Write signal ($\overline{MWT}$) from the 7353 Data Link board.

F. RAM BANK SELECT DECODER

A RAM Bank Select Decoder is used to generate the Bank Select signals $\overline{BS1}$-$\overline{BS4}$ which are used to select a RAM bank (4K module) on the 7354 Memory board.

The A and B address inputs of a 74153 (L40, 4-line-to-1-line multiplexer) are connected to the A0-A1 output signals (encoded highest priority Request) of the Priority Encoder and Latch. The 74153 will present the following signals at its 1Y and 2Y outputs:

REQUEST	A	B	1Y	2Y
8080 READ	0	0	A12	A13
8080 WRITE	0	1	A12	A13
DMA	1	0	A12M	A13M
REFRESH	1	1	0	0

The A12 and A13 8080 address bits are use to select one bank of RAM memory for a 8080 Read/Write operation (the A12M and A13M DMA address bits perform the same function for a DMA Read/Write operation). In the case of a Refresh operation, the arbitrary low (0) outputs were selected.

The 1Y and 2Y outputs of L40 are connected to the A and B select inputs of a 74155 (L39, 2-line-to-4-line demultiplexer). The $\overline{Y0}$-$\overline{Y3}$ outputs produce the Bank Select signal ($\overline{BS1}$-$\overline{BS4}$) for the 7354 Memory board. The 74155 outputs can be disabled by either the A2 output signal (encoded highest priority Request) of the Priority Encoder and Latch going high (this indicates that no memory operation will take place) or by the 2Y output of L30 (75153, 4-line-to-1-line multiplexer) going high. The A and B address inputs of L30 are connected to the A0-A1 output signals (encoded highest priority Request) of the Priority Encoder and Latch. The 74153 will present the following signals at its 2Y output:

REQUEST	A	B	1Y
8080 READ	0	0	A14
8080 WRITE	0	1	A14
DMA	1	0	A14M
REFRESH	1	1	0

The A14 8080 address bit is used to select eiher the RAM or PROM for a 8080 memory operation (the A14M DMA address bit performs the same function for a DMA memory operation). In the case of a Refresh operation, the arbitary low (0) output was selected. If the 1Y output is low, then L39 is enabled and the RAM is selected; otherwise the PROM will be selected (no RAM bank enabled). The A14/A14M address bit is used to select the PROM since the origin of the PROM is hex'4000' (A14/A14M bit is high).

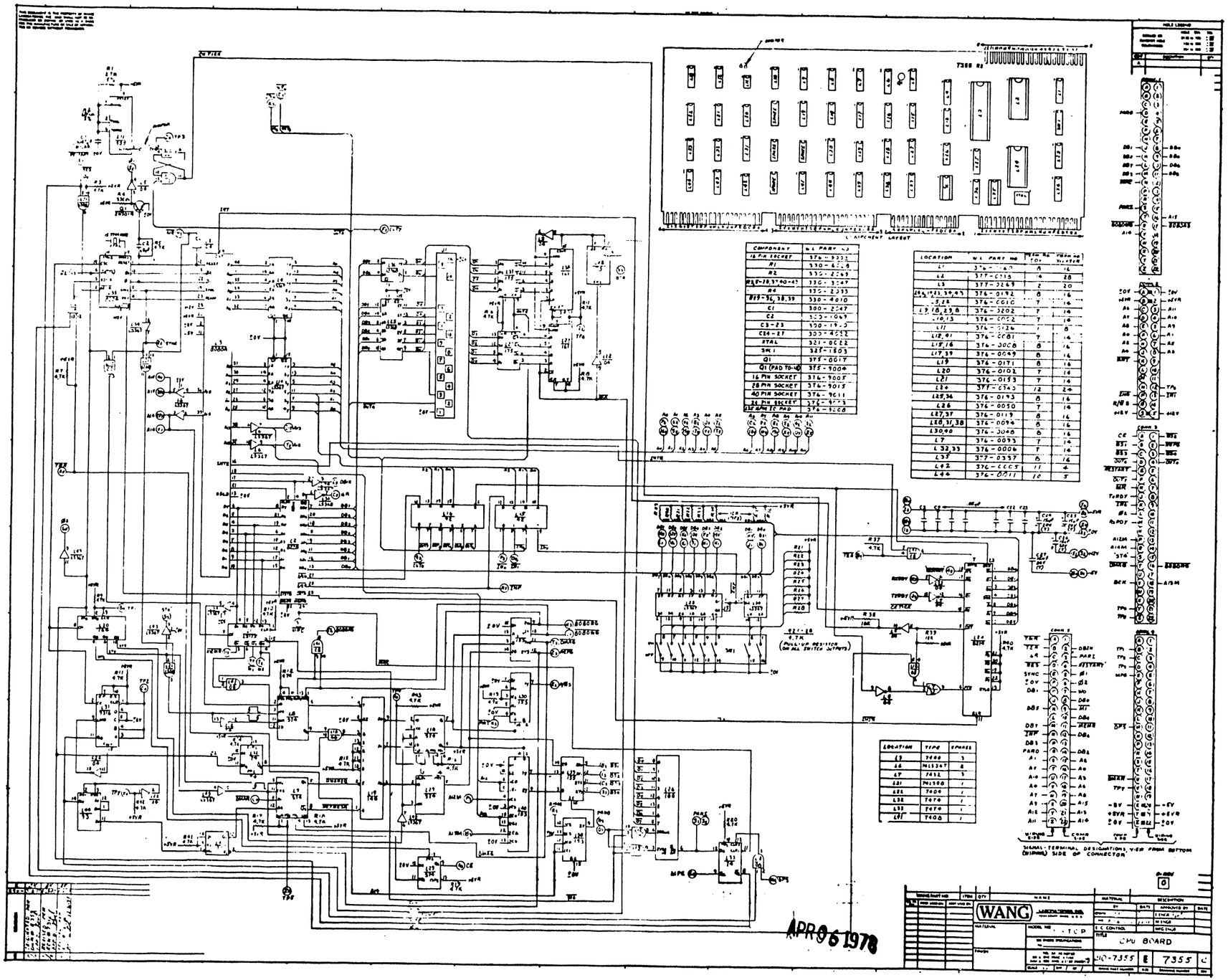


Figure 5-4 T.C. CPU-Schematic Illustration

5.4.5 MODEM AND ACU INTERFACE BOARD

5.4.5.1 GENERAL

The Channel Modem and ACU Interface board contains the USART (8251), RS-232-C modem interface, and the RS-366 Automatic Calling Unit (ACU) interface. Please refer to the Modem and ACU Interface block diagram.

5.4.5.2 8251 (USART)

The 8251 (L16) is a Programmable Universal Synchronous/ Asychronous Receiver/Transmitter (USART). The 8251 uses the Ø2 clock signal from the 7355 CPU board. The 8251 is reset by the Master Reset (MR) from the 7355 CPU board. The 8080 data bus (DB0-DB7) is connected to the data bus inputs of the 8251.

The 8251 interfaces to the RS-232-C modem interface with six signals. Inputted to the 8251 are the signals Received Data (BB), Clear-to-Send (CB), and Data Set Ready ($\overline{DSR}$). Outputted by the 8251 are the signals Transmitted Data (BA), Request-to-Send (CA), and Data Terminal Ready (CD). The Data Terminal Ready signal is connected to the Break Switch which can turn the signal OFF when activated.

The two output signals of the 8251, TXRDY (Transmitter Ready) and RXRDY (Receiver Ready), are provided to the 7355 CPU board and are used as interrupt signals. TXRDY indicates that the transmitter buffer is ready to accept a data character from the 8080 CPU, and RXRDY indicates that the receiver buffer contains a character that is ready to be input to the 8080 CPU.

The 8251 clock signals $\overline{RXC}$ (Receiver Clock) and $\overline{TXC}$ (Transmitter Clock) are provided by the Asynchronous/Synchronous Clock Mode Selecter. In the asynchronous mode, the clocks are provided internally by the Internal Clock Rate Decoder on the 7355 CPU board (BCK signal). In the synchronous mode, the clocks are provided externally from the RS-232-C modem interface signals Transmitter Clock (DB) and Receiver Clock (DD). A 74157 (L11, quad two input multiplexer) is used to select the clock mode. This multiplexer is also used to control the modem interface signal Secondary Request to Send (SCA). The 8080 Output Command $\overline{OUT7}$ is used to set the clock mode and the SCA signal. The 8080 OUT7 instruction and required data is formatted as follows:

INSTRUCTION	
OUT	X'07'

DATA	
	S
- - - C - - -	A
	A
MSB	LSB

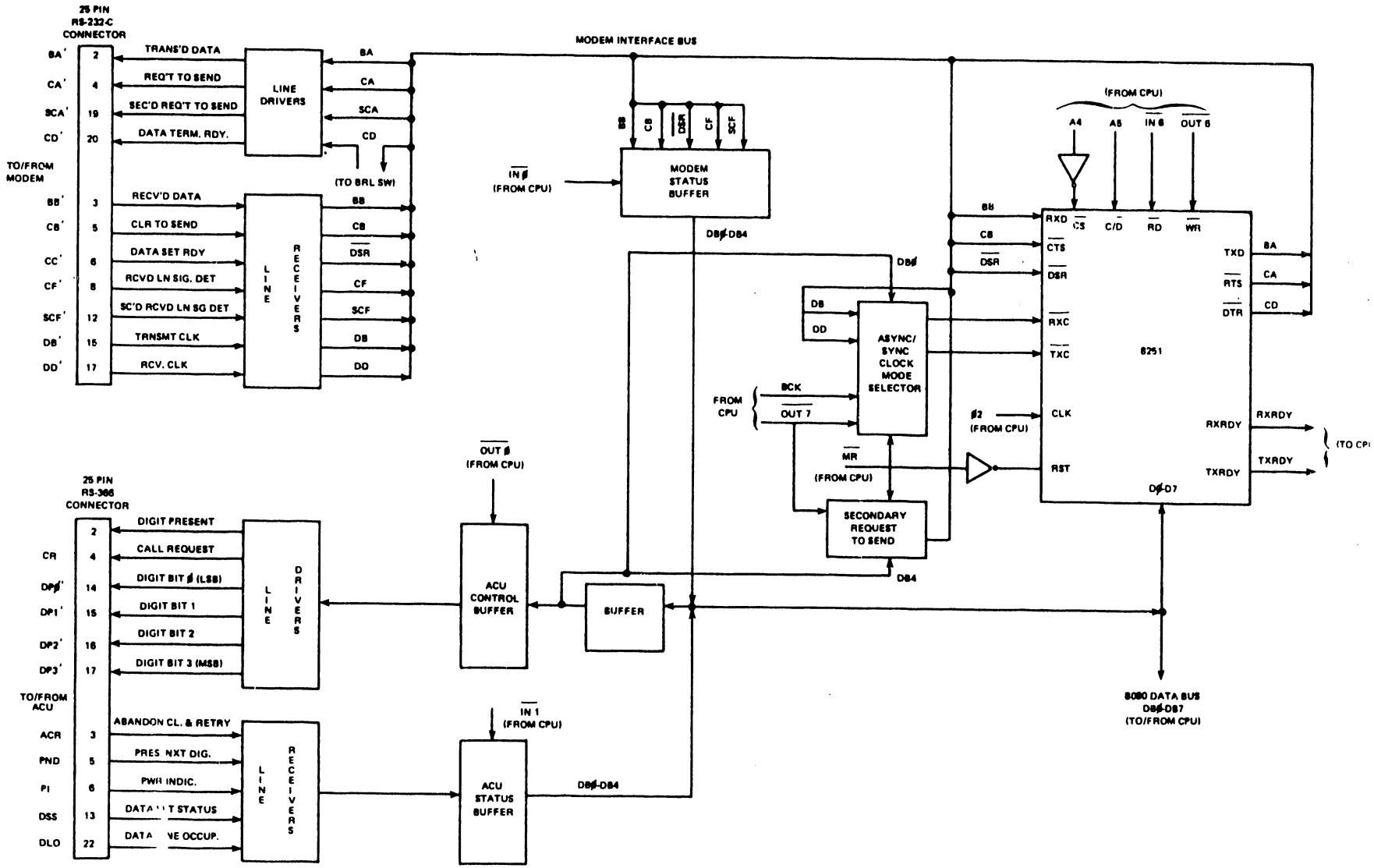


Figure 5-5 T.C. Modem Interface Bus-Block Diagram

Two D-type flip-flops (L10, 7474) are used to latch the Select Asynchronous Clock bit (SAC) and SCA bit. The $\overline{OUT7}$ signal clocks these bits into the latch from the 8080 Data Bus (DB0 and DB4). In the asynchronous mode (SAC=1), the BCK signal is inputed to the 8251 receiver/transmitter clock inputs and the SCA signal can be set ON (SCA bit =1) or OFF (SCA bit =0). In the synchronous mode (SAC=0), the 8251 transmission timing is provided from the modem interface signals DD and DB. Also in this mode, the internal clock signal BCK drives the modem interface signal SCA. This permits the synchronous transmission between the Channel and another system through a direct cable connection when the appropriate modifications to the 24 Pin Jumper is made.

The 8251 operation is controlled by the following inputs from the 7355 CPU board: $\overline{A4}$ (8080 Address bit) to Chip Select ($\overline{CS}$), A5 (8080 Address bit) to Control/Data (C/$\overline{D}$), $\overline{IN6}$ (Input Command 6) to Read ($\overline{RD}$), and $\overline{OUT6}$ (Output Command 6) to Write ($\overline{WR}$). The combination of the $\overline{IN6}$ and $\overline{OUT6}$ along with the A4 and A5 bits produces the additional Input and Output Commands as follows:

OUT16	Output character to 8251 for Transmission
IN16	Input Received Character from 8251
OUT36	Set 8251 Mode/Command Data
IN36	Read 8251 Status

A. OUT16

A character to be transmitted is output to the 8251. This clears the Transmitter Ready condition (TXRDY) and the interrupt condition which it causes. If a transmission character of fewer than 8 bits is being used, the character to be transmitted is assumed to be right adjusted in the byte output from the 8080 accumulator. The 8080 OUT16 instruction and required data is formatted as follows:

INSTRUCTION		DATA
OUT	X'16'	CHARACTER TO BE TRANSMITTED
		MSB LSB

B. IN16

A received character is input from the 8251. This clears the Receiver Ready condition (RXRDY) and the interrupt condition that it causes. If a transmission character of fewer than 8 bits is being used, the received character is assumed to be right adjusted in the byte input into the 8080 accumulator. The 8080 IN16 instruction and required data is formatted as follows:

INSTRUCTION	
IN	X'16'

DATA
RECEIVED DATA CHARACTER
MSB LSB

C. OUT36

The interpretation of the byte of data output by the SET 8251 Mode/Command instruction is determined by the state of the 8251. Following a reset of the 8251, which can be caused by either a hardware reset (MR) or a software reset (bit in the Command Word), the first byte output by this instruction is a Mode Word. If the Mode Word selected asynchronous mode, all bytes subsequently output by the instruction (unless they specify an internal reset) are Command Words. If the Mode Word selected synchronous mode, the next one or two bytes, as determined by the Mode Word, output by the instruction define the synchronous pattern. All bytes then subsequently output by the instruction are Command Words. The 8080 OUT36 instruction and required data is formatted as follows:

INSTRUCTION	
OUT	X'36'

DATA
MODE WORD
SYNC CHARACTER or COMMAND WORD
MSB LSB

SYNCHRONOUS MODE WORD

S		P					
C	0	E	E	L	L	0	0
S		P	N	2	1		

MSB LSB

ASYNCHRONOUS MODE WORD

		P					C
S	S	E	E	L	L	1	R
2	1	P	N	2	1		D

MSB LSB

SCS	Single Character Synchronization (Double if not set)
EP	Even Parity Generate/Check (if PEN is set)
PEN	Parity Enable
L2,L1	Transmission Character Length (in bits): 00=5; 01=6; 10=7; 11=8.
S2,S1	Number of Stop Bits: 00=invalid; 01=1; 10=1.5; 11=2.
CRD	Clock Rate Devider: 0=16X; 1=64X

COMMAND WORD

!		R		B	R	D	T !
!	E	I	T	E	R	x	T x !
!	H	R	S	R	K	E	R E !

MSB LSB

EH	Enter Hunt Mode (Applicable to Synchronous Only)
IR	Internal Reset 8251
RTS	Request to Send Modem Signal
ER	Error Reset of Framing, Overrun, and Parity Error Status.
BRK	Send Break on Transmit Data Signal (Break lasts until BRK is cleared)
RxE	Receive Enable
DTR	Data Terminal Ready Modem Signal
TxE	Transmit Enable

D. IN36

The 8251 Status Register is read. The 8080 IN36 instruction and required data is formatted as follows:

INSTRUCTION

!		!
! IN	!	X'36' !
!		!

DATA

!						T	R	T !
!	-	-	F	O	P	x	x	x !
!			E	E	E	E	R	R !

MSB LSB

FE	Receiver Framing Error (Applicable to asynchronous only)
OE	Receiver Overrun Error
PE	Receiver Parity Error
TxE	Transmitter Empty
RxR	Receiver Ready (This bit generates an interrupt)
TxR	Transmitter Ready (This bit generates an interrupt. If the Transmitter is not enabled the interrupt will not be generated, but TxR will be seen as set when read)

5.4.5.3 MODEM INTERFACE

The Channel contains a 25-pin EIA RS-232-C / CCITT V.24 interface to a modem. 75150's (L4 and L5, line drivers) and 75154's (L12 and L13, line receivers) are used to interface to the modem. The signal polarity and voltage of the driven and detected signals are as follows:

CONTROL SIGNAL	DATA SIGNAL	APPLIED VOLTAGE	DETECTED VOLTAGE
ON	SPACE (0)	+8	+5 to +15
OFF	MARK (1)	-8	-5 to -15

The pin assignments of the signals only used by the Channel are as follows:

PIN	EIA	CCITT	SOURCE	SIGNAL DESCRIPTION
1	AA	101		PROTECTIVE GROUND
2	BA	103	CHANNEL	TRANSMITTED DATA
3	BB	104	MODEM	RECEIVED DATA
4	CA	105	CHANNEL	REQUEST TO SEND
5	CB	106	MODEM	CLEAR TO SEND
6	CC	107	MODEM	DATA SET READY
7	AB	102		SIGNAL GROUND
8	CF	109	MODEM	RECEIVED LINE SIGNAL DETECTOR
11,19	SCA	120	CHANNEL	SECONDARY REQUEST TO SEND
12	SCF	122	MODEM	SECONDARY RECEIVED LINE SIGNAL DETECTOR
15	DB	114	MODEM	TRANSMIT SIGNAL ELEMENT TIMING
17	DD	115	MODEM	RECEIVER SIGNAL ELEMENT TIMING
20	CD	108.2	CHANNEL	DATA [illegible]

5.4.5.4 MODEM STATUS BUFFER

A 74367 is used as a Modem Status Buffer (L1, three-state buffers). The Buffer is connected to the 8080 data bus (DB0-DB4) and is enabled by the Input Command $\overline{IN0}$. The 8080 IN0 instruction and required data is formatted as follows:

INSTRUCTION	
IN	X'00'

DATA							
					S		
-	-	-	B	C	C	C	C
			B	B	C	F	F
MSB							LSB

BB	Received Data (polarity is inverted)
CB	Clear to Send
CC	Data Set Ready
SCF	Secondary Received Line Signal Detector
CF	Received Line Signal Detector

5.4.5.5 ACU INTERFACE

The Channel contains a 25-pin EIA RS-366-C / CCITT V.11 interface to a Automatic Calling Unit (ACU). 75150's (L6, L7 and L8, line drivers) and 75154's (L12 and L15, line receivers) are used to interface to the ACU. The signal polarity and voltage of the driven and detected signals are as follows:

CONTROL SIGNAL	DATA SIGNAL	APPLIED VOLTAGE	DETECTED VOLTAGE
ON	0	+8	+5 to +15
OFF	1	-8	-5 to -15

The pin assignments of the signals used by the Channel are as follows:

PIN	CHANNEL	CCITT	SOURCE	SIGNAL DESCRIPTION
1				FRAME GROUND
2	DP	211	CHANNEL	DIGIT PRESENT
3	ACR	205	ACU	ABANDON CALL AND RETRY
4	CR	202	CHANNEL	CALL REQUEST
5	PND	210	ACU	PRESENT NEXT DIGIT
6	PI	213	ACU	POWER INDICATION
7		201		SIGNAL GROUND
13	DSS	204	ACU	DATA SET STATUS
14	DB0'	206	CHANNEL	DATA BIT 0 (LSB)
15	DB1'	207	CHANNEL	DATA BIT 1
16	DB2'	208	CHANNEL	DATA BIT 2
17	DB3'	209	CHANNEL	DATA BIT 3 (MSB)
22	DLO	203	ACU	DATA LINE OCCUPIED

A ACU Control Buffer (L3) and a ACU Status Buffer (L2 and L14) are used to interface the ACU to the 8080 data bus. The Input Command $\overline{IN1}$ causes the ACU Status Buffer to be read, and the Output Command $\overline{OUT0}$ sets the control signals in the ACU Control Buffer. The 8080 IN1 and OUT0 instructions and required data are formatted as follows:

INSTRUCTION	
IN	X'01'

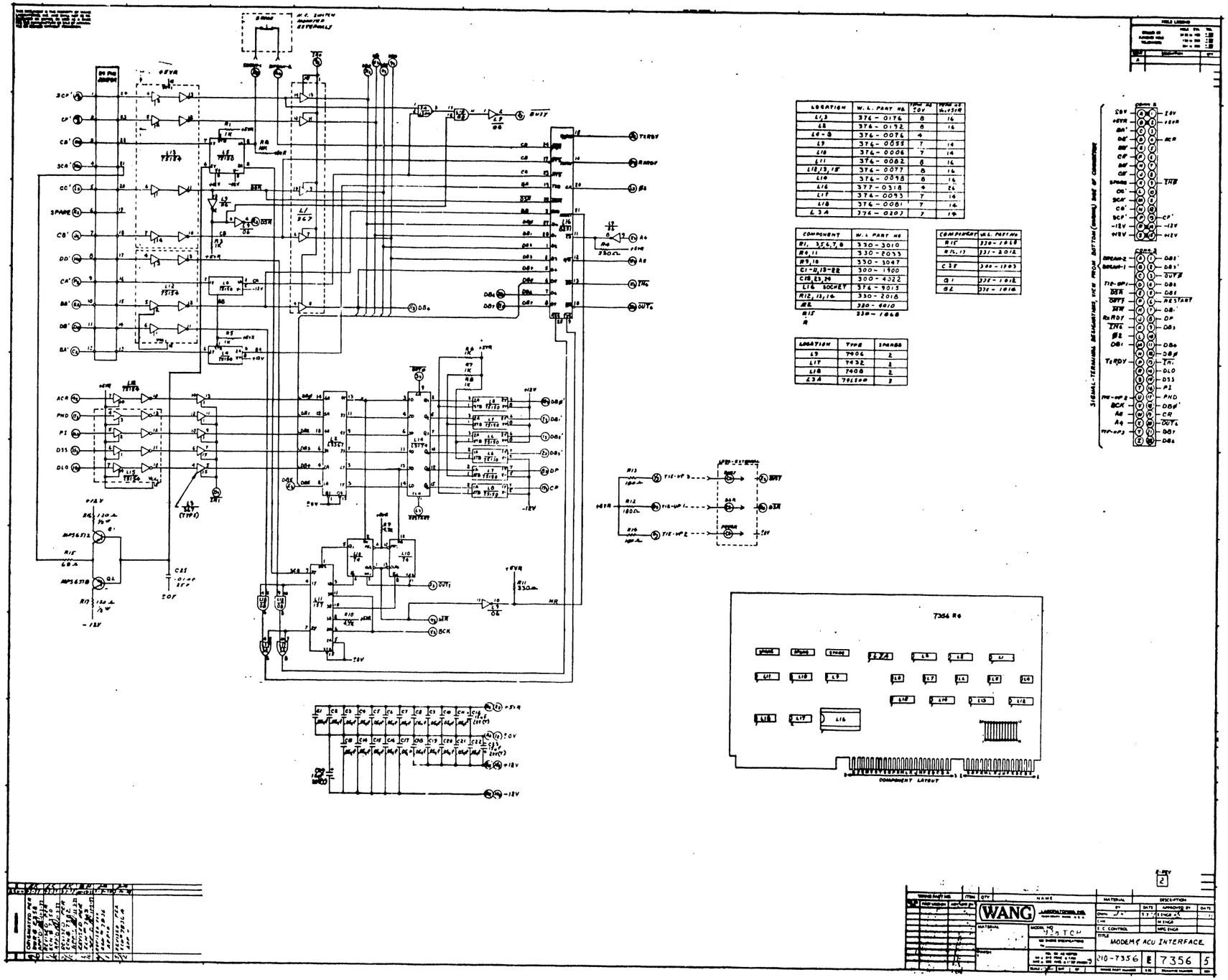
DATA							
		D	D		P	A	
-	-	-	L	S	P	N	C
		O	S	I	D	R	
MSB							LSB

DLO	Data Line Occupied
DSS	Data Set Status
PI	Power Indication
PND	Present Next Digit
ACR	Automatic Call and Retry

INSTRUCTION	
OUT	X'00'

DATA								
				D	D	D	D	
-	-	C	D	B	B	B	B	
		R	P	3	2	1	0	
MSB							LSB	

CR	Call Request
DP	Digit Present
DB3	Digit Bit 3 (high order bit)
DB2	Digit Bit 2
DB1	Digit Bit 1
DB0	Digit Bit 0 (low order bit)



LOCATION	W.L. PART NO.	TYPE NO. 20V	TYPE NO. MULTIPIN
L1,3	376-0176	8	16
L2	376-0192	8	16
L4-8	376-0076	4	
L9	376-0055	7	14
L10	376-0006	7	14
L11	376-0082	8	16
L12,13,15	376-0077	8	16
L14	376-0098	8	16
L16	377-0318	4	24
L17	376-0093	7	14
L18	376-0081	7	14
L19A	774-0207	7	14

COMPONENT	W.L. PART NO.
R1, 3,5,6,7,8	330-3010
R4,11	330-2033
R9,10	330-3047
C1-11,13-22	300-1900
C12,23,24	300-4022
L16 SOCKET	376-9015
R12, 13, 16	330-2016
R2	330-6010
R15	330-1068

COMPONENT	W.L. PART NO.
R15	330-1068
R14,17	331-2012
C23	300-1903
Q1	331-1012
Q2	331-1016

LOCATION	TYPE	SPARES
L9	7404	2
L17	7432	3
L18	7408	2
L19A	74S200	3

Figure 5-6 T.C. Modem and ACU Interface-Schematic Illustration

MILLIMETERS IN PARENTHESIS. TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS.

DO NOT SCALE

HOLE LEGEND & TOLERANCES			
HOLE DIA		TOLERANCE	
.035	.136	± .003	.001
.116	.250	± .005	.001
.251	.500	± .005	.001
SYM.	DESCRIPTION		QTY
A			

SOCKETS		
LOC	TYPE	QP.
L1	7404	5

LOCATION	WL. PT. NO.	V_{CC}	GND
L1	376-0010	14	7
L2	376-0077	16	8
L3	376-0076	8	4

COMPONENT	WL PT NO.
R1,4,6	330-3022
R2	330-2068
R3,7	330-2039
R5	330-3047
R8,9	330-3010
RLY 1,2	320-0062
D1,5	380-4000
D2,3	380-1001
D4	380-2039
Q1	375-0017
Q2	375-1017
C1,3,4	300-4023
C2	300-1900

CONN #1

±5V	A1	±5V
±8V	B1	±8V
	C1	BA
	D1	DB
	E1	BB
	F1	DD
	H1	CB
-12V	R1	-12V
+12V	S1	+12V

CONN #2

RD	A2	
	B2	
	C2	
	D2	
	E2	
	F2	
	H2	
	J2	
TDSG	K2	
LOOP IN	L2	
VOLT OUT	M2	
LOOP OUT	N2	
	P2	
	R2	
	S2	
	T2	
	U2	
	V2	
	W2	
	X2	
	Y2	
	Z2	
	AA2	
	BB2	

QTY	ITEM	WANG PART NO	DRAWING NO	DESCRIPTION
NEXT ASSY				

WANG LABORATORIES INC. TEWKSBURY MASS U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	EBA	9-9-77	E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO 7638 TCC

SEE ENGRG SPECIFICATIONS No.

FINISH

TOL ES AS NOTED
XX ± FRAC ±
XXX ± ANG ±
FINISH

SCALE NONE SHT 1 OF 1

TITLE TCP CURRENT LOOP

210-7357 | D | 7357 | 0

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

E.REV 0

Figure 5-7 T.C. Current Loop Interface-Schematic Illustration

5.4.6 MEMORY BOARD

5.4.6.1 GENERAL

The 7354 Memory board contains 16K bytes of Random Access Memory (RAM) and 1K bytes of Programmable Read Only Memory (PROM). The origin of the RAM is hex'0000' in the 8080's address space and the origin of the PROM is hex'4000'. The RAM can be accessed by both the 8080 CPU and the WWPS master processor via a Direct Memory Access (DMA), while the PROM can be accessed by only the 8080 CPU. Please refer to the 7353 Memory Board block diagram.

5.4.6.2 RAM ADDRESS BUS

The RAM is arranged into four banks (4k byte modules). Each bank is comprised of nine 4050 chips (4096 X 1 dynamic RAM). The 4050's address inputs are connected to RAM Address Bus (A0'-A11'). Three three-state buffers are connected to this bus; the 8080 Address Buffer (L42 and L45), the DMA Address Buffer (L43 and L46), and the RAM Refresh Buffer (L44 and L47).

The 8080 Address Buffer is connected to the 8080 Address Bus (A0-A11) and is enabled by the 8080 Address Strobe ($\overline{8080AS}$) which is provided from the 7355 CPU board. The DMA Address Buffer is connected to the DMA Address Bus (A0M-A11M) and is enabled by the DMA Grant signal ($\overline{DMAG}$) which is provided from the 7353 Data Link board. The RAM Refresh Buffer is connected to a 6 bit counter (L48 and L49) to generate the addresses (A0'-A5') required for RAM refreshing. The high order address bits (A6'-A11') are not needed and are tied low. The Refresh Grant signal ($\overline{REFG}$, from 7355 CPU board) is used to increment the Refresh counter and to enable the RAM Refresh Buffer.

5.4.6.3 RAM READ/WRITE AND CHIP SELECT LOGIC

The Read/Write input signal required by the RAM is provided by a 74367 (L53, three-state bus driver). Four inputs are connected to the Read/Write Strobe (R/$\overline{WS}$, from the 7355 CPU board) and four output Read/Write signals (R/$\overline{W1}$-R/$\overline{W4}$) are generated, one for each RAM bank. If R/$\overline{WS}$ = 0, then the RAM will be placed into the WRITE mode, and if R/$\overline{WS}$ = 1 , then the RAM will be placed into the READ mode.

The Chip Enable signal required by the RAM is provided by the Chip Enable Driver (L10 and L29, TTL to MOS driver). The Chip Enable signal (CE, from the 7355 CPU board) is used to enable the driver. The inputs to the driver are the Bank Select signals ($\overline{BS1}$-$\overline{BS4}$, from the 7355 CPU board) ANDed with the Refresh Grant signal ($\overline{REFG}$). The output of the drivers are the high level signals CE1-CE4, with one connected to each RAM bank. If CE1-CE4 = 1, then the chip is selected and a Read/Write /Refresh operation can take place. For a Read/Write operation, only one RAM bank will be enabled and for a Refresh operation, all four banks are enabled.

5.4.6.4 RAM DATA BUS

The RAM's data input/output terminals are connected to the RAM Data Bus (BP0-DP8). Three three-state buffers are connected to this bus; the 8080 Write Data Buffer (L41 and L51), the 8080 Read Data Buffer (L39, L40, and L50), and the DMA Data Buffer (L57 and L58).

The 8080 Write Data Buffer is connected to the 8080 Data Bus (DB0-DB7) and to the Parity In bit (PARI, from 7355 CPU board) and is enabled by the 8080 Write Memory signal ($\overline{80WM}$, from RAM/PROM Decoder). The 8080 Read Data Buffer is connected to the 8080 Data Bus (DB0-DB7) and to the Parity Out bit (PARO, from 7355 CPU board) and is enabled by the 8080 Read Memory signal ($\overline{80RM}$, from RAM/PROM Decoder). The 8080 Read Grant signal ($\overline{8080RG}$, from 7355 board) clocks the data into the buffer. The DMA Data Buffer (bi-directional) is connected to the DMA Data Bus (DM0-DM8) and is enabled by the signals DMA Grant ($\overline{DMAG}$, from 7353 Data Link board) and the signal Memory Write ($\overline{MWT}$, from 7353 Data Link board). If $\overline{MWT}$ = 0, then a DMA Write operation will take place , and if $\overline{MWT}$ = 1, then a DMA Read operation will take place.

5.4.6.5 RAM/PROM DECODER

A RAM/PROM Decoder (L49-A, 74155 - two line to four line decoder) is provided to select either the RAM or the PROM for 8080 CPU memory operations. The actual selection between the RAM and PROM is controlled by the 8080 Address bits A14 and A15. If A14 = A15 = 0, then the RAM is selected. If A14 = 1 and A15 = 0, then the PROM is selected. If A15 = 1, then neither is selected. When the RAM is selected, the output signals 8080 Read Memory ($\overline{80RM}$) and 8080 Write Memory ($\overline{80WM}$) are generated from the input signals 8080 Write Grant ($\overline{8080WG}$, from 7355 CPU board) and Memory Read ($\overline{MRC}$, from 7355 CPU board). When the PROM is selected, the signal Debug PROM Select ($\overline{DPS}$) is generated.

5.4.6.6 PROM

A Debug PROM (L51-A, 2708) is provided for software debugging purposes. The PROM is addressed by the 8080 Address bits A0-A7 and is constantly enabled. The PROM's data bus is connected to the 8080 Data Bus (DB0-DB7) via a three-state buffer (L41 and L51-B, 74LS367), which is enabled by the signal Debug PROM Select ($\overline{DPS}$) from the RAM/PROM Decoder.

TABLE 5-2

7353 DATA LINK BOARD MNEMONICS

TERM	DESCRIPTION
ACY	ADDRESS CARRY
A0M-A14M	DMA ADDRESS BITS
B1	BYTE STATE 1 (INSTRUCTION)
B2	BYTE STATE 2 (1st ADDRESS)
B3	BYTE STATE 3 (2nd ADDRESS)
B4	BYTE STATE 4 (DATA 1 to 256)
CAR	CARRY (transmission delay counter)
CG	CLEAR GATE
CK	MASTER CLOCK
CLP	COMPLETE PULSE
CPE	COAX PARITY ERROR
C1	CLEAR 1
C2	CLEAR 2
DMAG	DMA GRANT
DMAR	DMA REQUEST
DMRG	DMA REQUEST or GRANT
DM0-DM8	DMA DATA BITS
EC	ERROR COUNT
GP	GATE PULSE
GATE	GATED SIGNAL
INST	INPUT STATUS (INSTATUS) INSTRUCTION
IRC	INSTATUS/RESTART COMPLETE
MWT	MEMORY WRITE
MPE	MEMORY PARITY ERROR
OPS	OPERATION STOP
PLG	PARALELL LOAD GRANT
PRRES	POWER-ON RESET
RCS	RESTART COMPLETE STROBE
RESET	RESET STATUS BIT
RESTART	DEVICE RESTART
RSTP	RESTART TELE-PROCESSOR
RSTRT	RESTART INSTRUCTION
RTCC	RECEIVER INHIBIT DELAY
RTD	RECEIVER TIME DELAY
SD	SERIALIZATION REGISTER OUTPUT DATA PARITY ERROR
SDIN	SERIAL DATA IN
SDOUT	SERIAL DATA OUT
SIPY	SERIALIZATION REGISTER INPUT DATA PARITY BIT
SI0-SI7	SERIALIZATION REGISTER INPUT DATA BITS
SMWT	SLAVE MEMORY WRITE INSTRUCTION
SOPY	SERIALIZATION REGISTER OUTPUT DATA PARITY BIT
SO0-SO7	SERIALIZATION REGISTER OUTPUT DATA BITS
SRCK	SERIALIZATION REGISTER CLOCK
ST4	STATE TIME 4
S4-S7	DEVICE I.D. BITS
TCK	INSTRUCTION REGISTER CLOCK
TG	TIME-OUT GATED SIGNAL
TO	TIME-OUT
TRANS	TRANSMITTER ENABLE
TRCG	TRANSMITTED DATA STROBE
1BC	1 BYTE TRANSFER COMPLETE
1BYTR	1 BYTE TRANSFER INSTRUCTION
256BC	256 BYTE TRANSFER COMPLETE
256BYTR	256 BYTE TRANSFER INSTRUCTION
256DRC	256 BYTE READ COMPLETE
+DATA	DIFFERENTAL SERIAL DATA TO MASTER
-DATA	

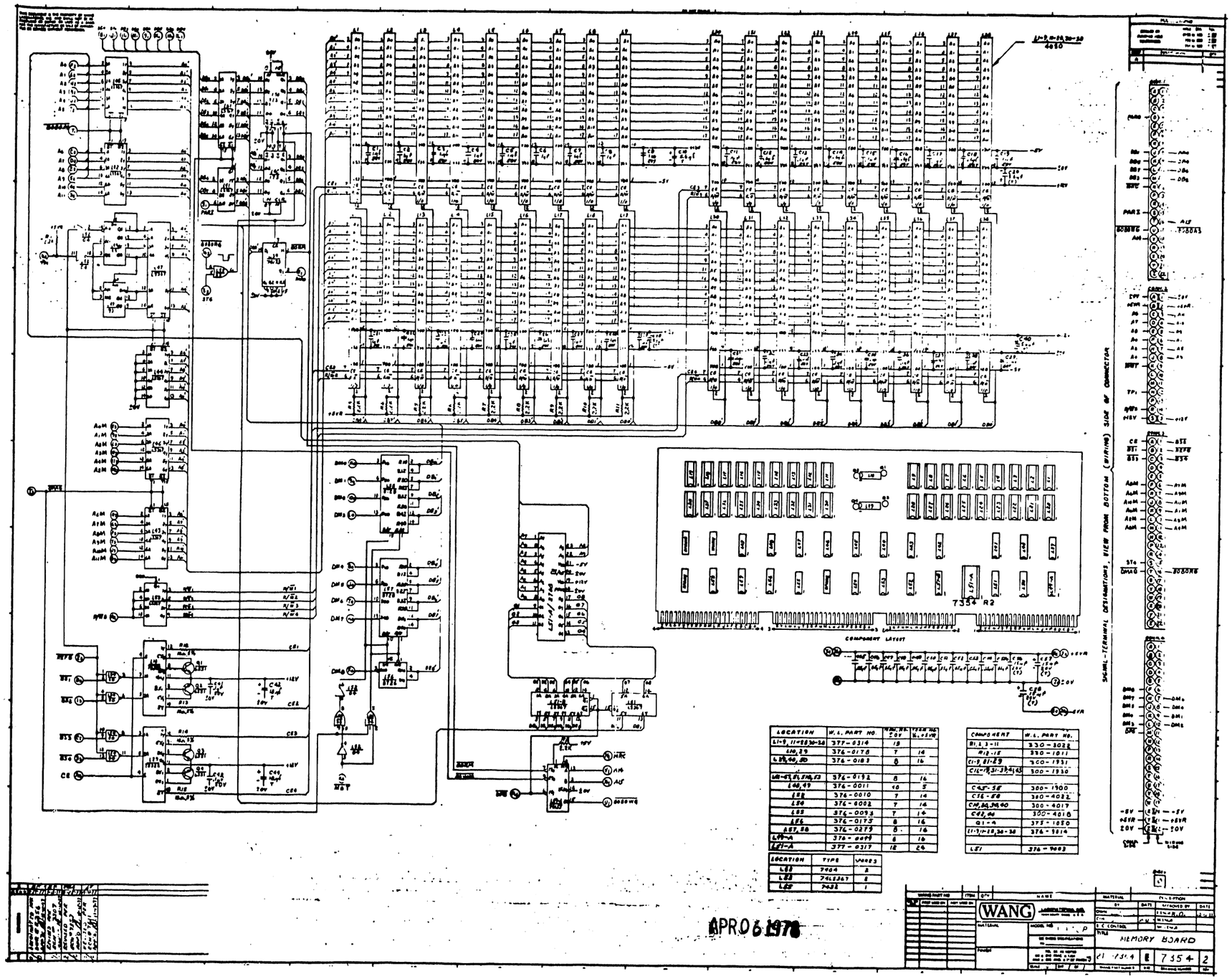


Figure 5-8 T.C. Memory-Schematic Illustration

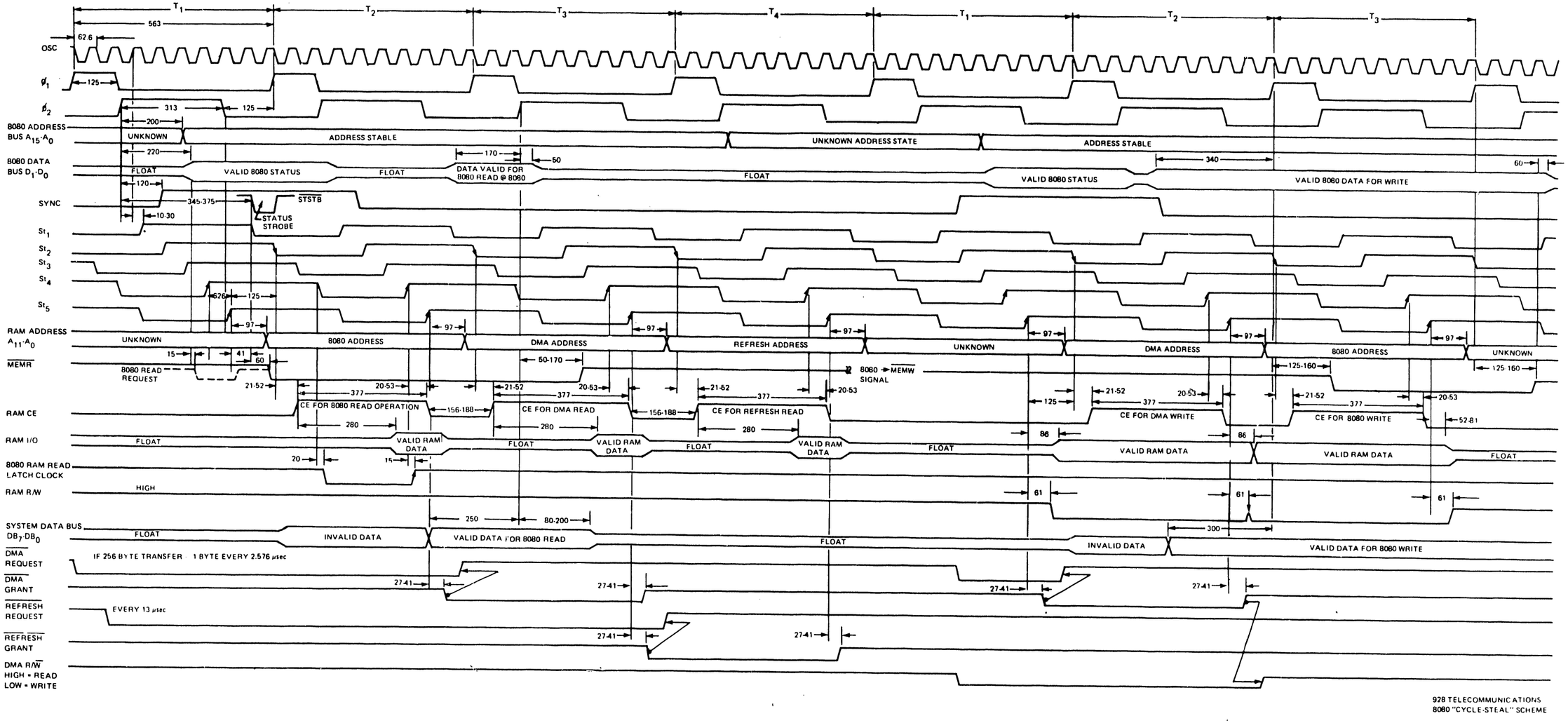


Figure 5-9 T.C. Timing Diagrams — 8080 "Cycle Steal" Scheme — Sheet 1

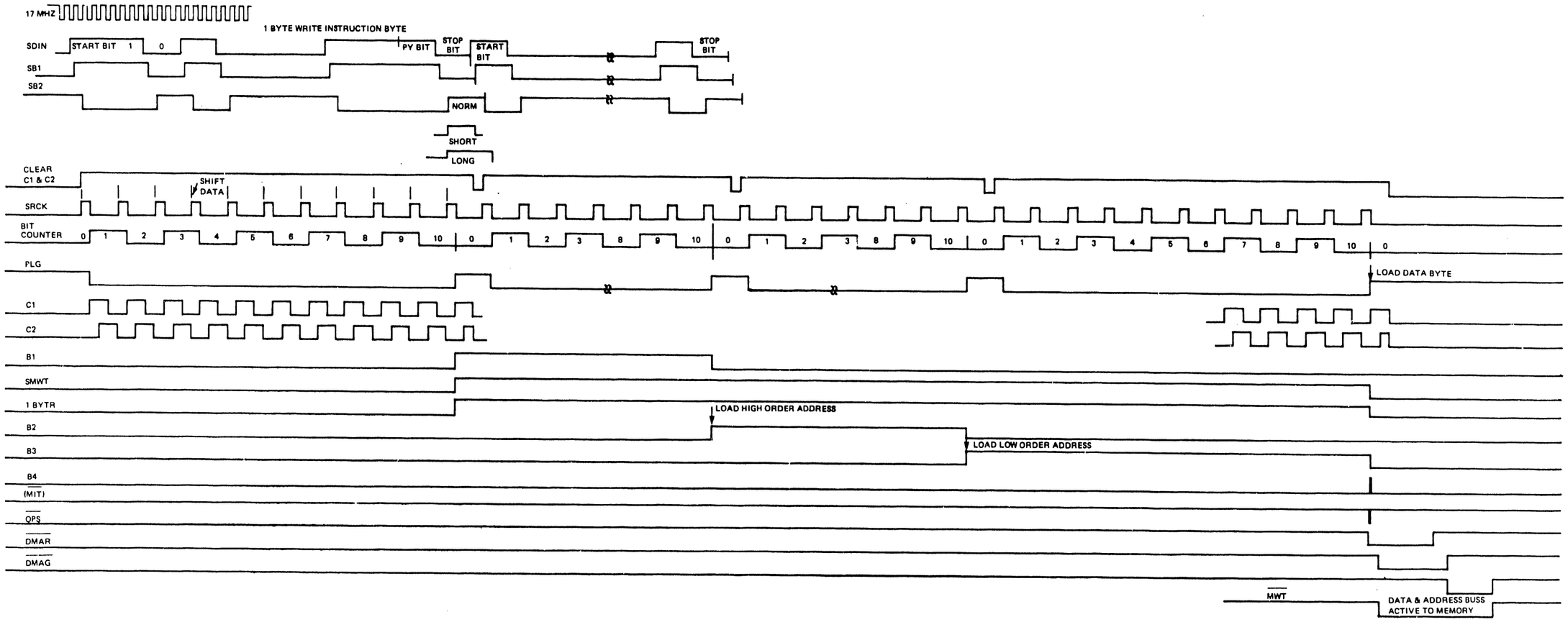


Figure 5-9 T.C. Timing Diagrams — 1 Byte Write Tele-Slave — Sheet 2

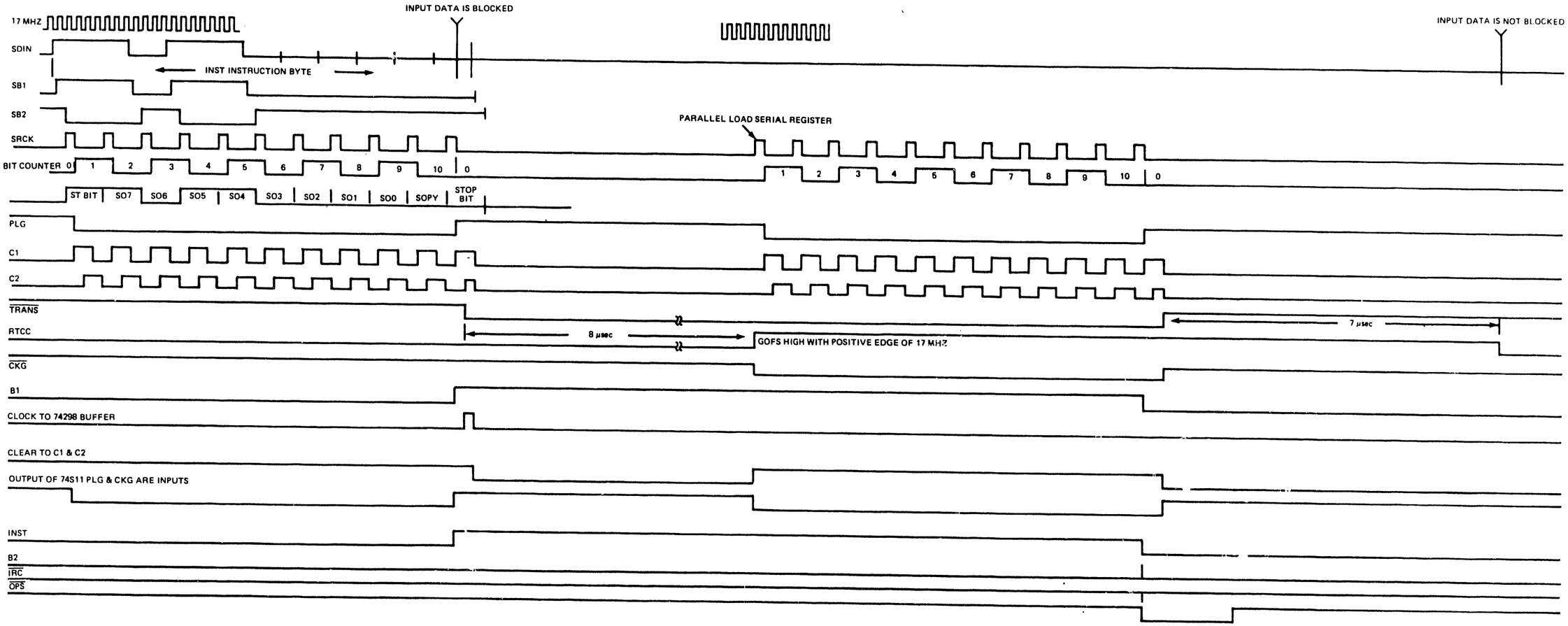


Figure 5-9 T.C. Timing Diagrams — IN-STATUS-OP, IN Tele-Slave — Sheet 3

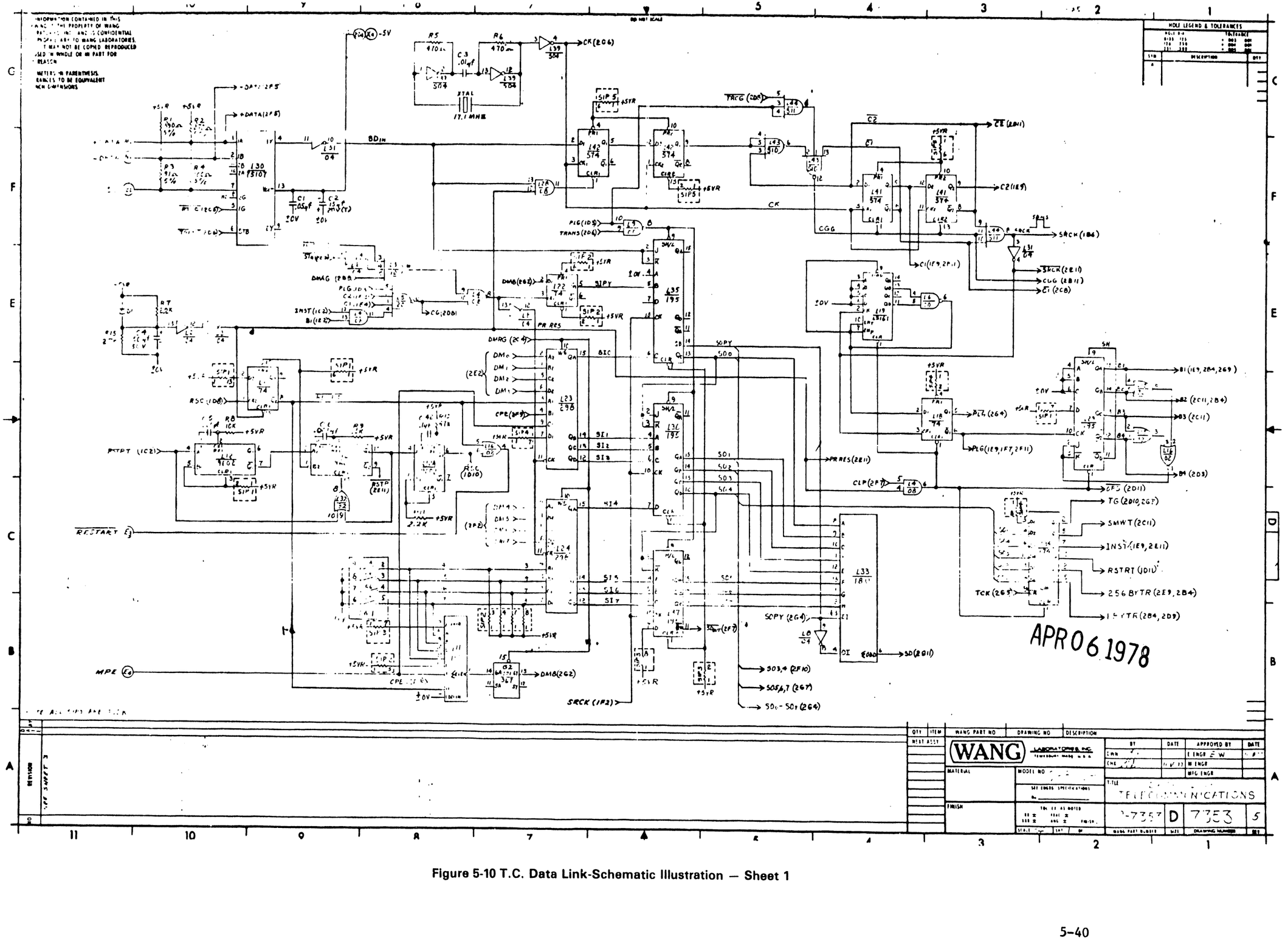


Figure 5-10 T.C. Data Link-Schematic Illustration — Sheet 1

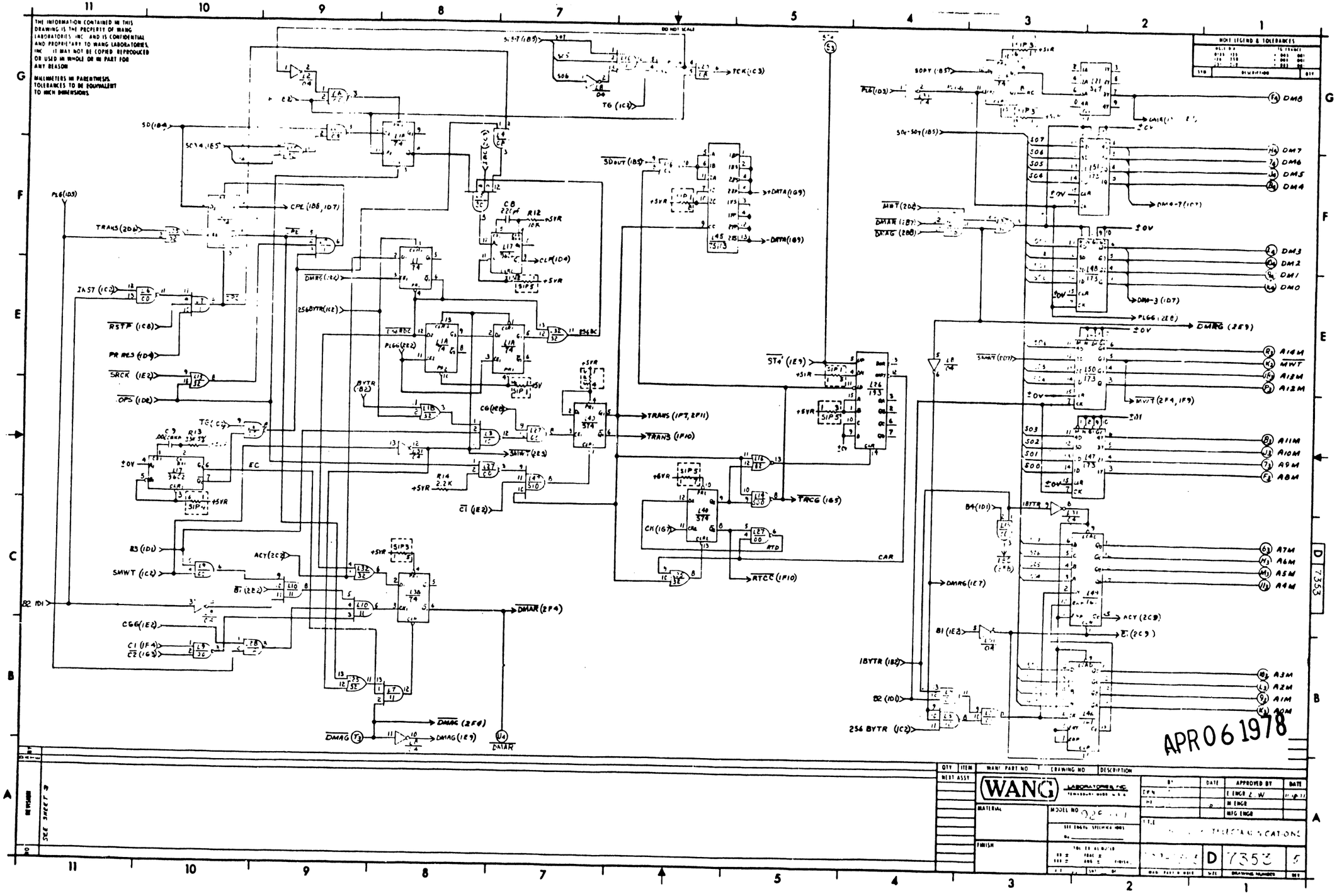


Figure 5-10 T.C. Data Link-Schematic Illustration — Sheet 2

LOCATION	W.I. PART NO.	TYPE
L1A,1B,22,38	376-0006	7474
L2,P,31	376-0010	7404
L3	376-0003	7410
L4,20,28	376-0001	7409
L5	376-0004	7420
L6,9,13,27	376-0002	7400
L7,10	376-0194	7411
L11,33	376-0050	74180
L12,12A,17	376-0104?	9602
L14	376-0228	74S00
L15,23,32,1B	376-0093	7432
L16	376-0016	7402
L19	376-0233	MLS161
L21	376-0176	74367
L23,24	376-0138	74298
L26	376-0053	74193
L29,35,36,37	376-0097	74195
L30	376-0146	75107
L34	376-0098	74174
L37	376-0197	74S04
L40,41,42	376-0202	74S74
L43	376-0238	74S10
L44	376-0237	74311
L45	376-0286	75113
L46,49	376-0094	74161
L47,48,50,51	376-0183	74193

COMPONENT	W.I. PART NO.	TYPE
D1	380-1001	SIL.
SW1	325-1501	5 BANK DIP
XTAL	321-0018	17.1 MHz
SIP1-5	333-0804	8-2K SIP RES.
R1	330-2047	39Ω ¼W 5%
R2	330-2025	270Ω ¼W 5%
R3	330-1057	910Ω ¼W 5%
R4	330-2011	100Ω ¼W 5%
R5,6	330-2047	47Ω ¼W 5%
R7,11,18	330-3022	2.2K ¼W 5%
R8,9,12	330-4011	1K ¼W 5%
R10	330-4047	47K ¼W 5%
R13	330-4034	33K ¼W 5%
R15	330-3027	2.7K ¼W 5%
C1,10-38	300-1500	.05μF 12V
C2,7,39-41	300-4022	15μF 20V TA
C3	300-1903	.01μF 25V
C4	308-3010	50pF 50V
C5,8	300-1220	22pF CER
C6	300-1906	.001μF 200V
C9	300-5012	.0033μF 500V 5%
C42	300-1930	.1μF 50V

LOCATION	TYPE	SPARES
L1	7404	2
L1B	7432	3
L12A	9602	1
L13	7400	3
L14	74S00	3
L27	7400	1
L28	7408	2
L39	74S04	3
L44	74311	1

SIGNAL INDEX

MNEMONIC	SHEET-ZONE
AcM-AioM	2C1
B1-B6	1D1
DMc-DM8	2F1
-DATA	1F11
+DATA	1F11
TRC	2F8
45±BC	2B7
IBVTR	1B2
731 BVTR	1C2
CPF	2B9
CAIAG	2B9
CAIAR	2C7
INST	1C2
IPE	2F10
AIRE	1B9
MWT	2E1
SP3	1C2
PLG	1D3
25±RDC	2E8
RESTART	1C11
RSTRT	1C2
RTCC	2C5
SDIN	1F9
SDOUT	1B5
SMWT	1C2
SRCK	1K2
5V6'	2G5
TRANS	2D6

HOLE LEGEND & TOLERANCES

HOLE DIA	TOLERANCE
PLTD THRU	.003
.116	.004
.154	.003
.196	.003

SYM	DESCRIPTION	BY
A		

COMPONENT LAYOUT

7383 RL

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

APR 06 1978

QTY	ITEM	WANG PART NO	DRAWING NO	DESCRIPTION
NEXT ASSY				

WANG

MATERIAL

FINISH

MODEL NO 2288TCP

TITLE DATA LINK TELECOMMUNICATIONS

DRAWN BY	DATE	APPROVED BY	DATE

2288-7353	D	7353	5

Figure 5-10 T.C. Data Link-Schematic Illustration — Sheet 3

DIMENSIONS IN PARENTHESIS, MILLIMETERS TO BE EQUIVALENT TO INCH DIMENSIONS.

LOCATION	W.L. PART NO.	TP Sw. No. +5V
L1, 3	376-0066	5
L2	376-0240	
L4, 5	376-0134	9
L6	376-0074	

LOCATION	TYPE	SPARES
L2	LM339	2

COMPONENT	W.L. PART NO.
R1,2	332-3010
R3	334-0002
R4	330-2068
R6,12,22,31	330-3015
R7,18,34	330-3033
R8,17,25	330-3022
R9	337-2033
R10,19,30	330-5012
R11	330-3018
R13	330-5010
R15	334-0015
R21	330-1022
R23	334-0014
R24	334-0003
R26	330-1027
R27	330-4033
R28	330-2082
R29,32	336-1022
R33	330-3056
C1	300-3078
C2	300-3021
C3,4,8,9	300-1915
C5,6,7,10,13,14	300-1900
C12,18	300-1906
C15	300-4032
C11,16	300-4022
D1,2	380-3008
D3,4	380-4000
D5-9	380-1001
D10	380-2229
Q1,2	375-1052
Q3	375-1053
Q4	375-1024
Q5	375-1017
C17	300-4018
R5,16	336-1014
R20	330-3027
R19	330-3010

HOLE LEGEND & TOLERANCES

PART No.	TOLERANCE
0125 125	± .003 .005
150 150	± .004 .006
221 .221	± .005 .007

SYM	DESCRIPTION	DATE

CONN. 1

± 0V	A 1	± 0V
+12VR	B 2	
	C 3	+12VR
+5VR	D 4	
	E 5	+5VR
	F 6	
	H 7	
	J 8	
	K 9	
	L 10	
	M 11	
	N 12	
	P 13	
	R 14	
+5REG	S 15	+5REG

CONN. 2

	A	1
	B	2
+5VRS	C	3
	D	4
	E	5
	F	6
	H	7
18VAC T2	J	8
18VAC T1	K	9
	L	10
	M	11
	N	12
	P	13
± 0V	R	14
-12VR	S	15
-5VR	T	16

SIGNAL-TERMINAL DESIGNATION, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

COMPONENT LAYOUT

APR 06 1978

QTY	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
NEXT ASSY				

WANG LABORATORIES, INC.

BY	DATE	APPROVED BY	DATE
DWN		ENGR	
CHK		MFG ENGR	
		MFG ENGR	

MATERIAL — MODEL —

FINISH

TITLE: REGULATOR

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-7358	D	7358	1

E-REV [1]

Originated 8/4/77 per ECN 1-1-11

Revised per ECN 1-1-11

Figure 5-11 T.C. Power Supply Regulator-Schematic Illustration

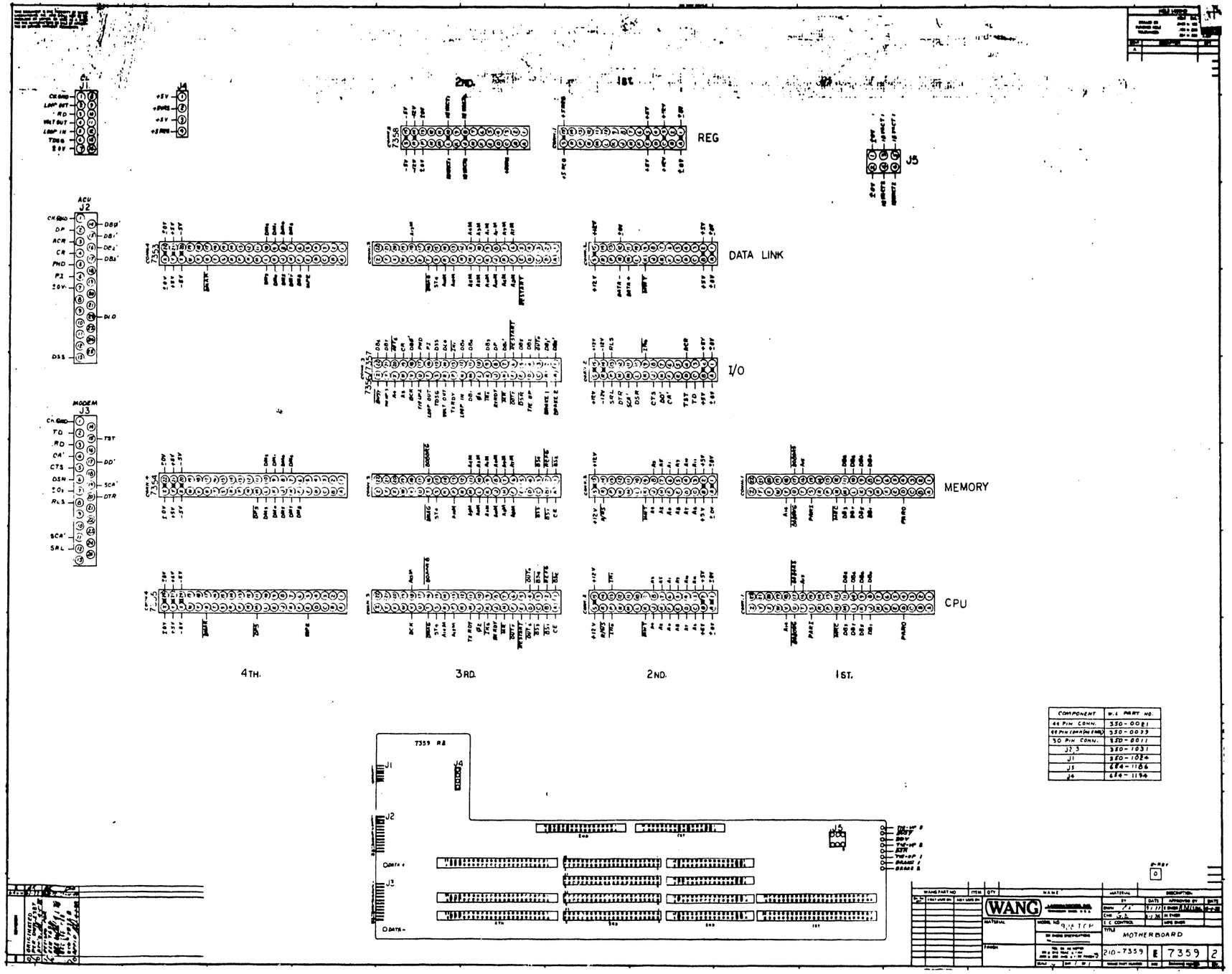


Figure 5-12 T.C. Motherboard-Schematic Illustration

APPENDIX A

APPENDIX A

928 MNEMONIC CODE

CODE	DESCRIPTION
AAC	Track Address Acknowledge (Hard Disk)
ACC	Allow Cyclic Check
ACK	"A" Disk Timing Clocks (Floppy/Hard)
AC0-AC6	Column Memory Address (CRT Memory)
AET	Automatic Enable for Repeat Keys
ARC7-ARC10	Row/Column Address (CRT Memory)
AR0-AR4	Row Memory Address (CRT Memory)
AUTO POWER	Power Up Spike Test Point
AUTO RESET	Reset of Master via Power Turn-On
A0-A15	Address Bits from 8080
A_0M-$A_{15}M$	DMA Address Bus to Data Link from Master CPU and Memory
BCK	"B" Disk Timing Clocks (Floppy/Hard)
BCNC	256 Byte Count Not Complete
BL	Blank CRT Screen
BLA	Blank CRT Screen
BP	Bad Parity
BR	Byte Read
BRC	Byte Read Complete
BRR	Byte Read Reset
BRT	Byte Read/Reset Transmit (Enables Data Out to Slaves)
BRT 7-14	Enables Data Out to Channels (7-14)
B0	Byte Zero Clock - Clears Serialization Register.
B1	Loads 256 Byte Instruction into Serilization Register
B1BB	Byte 1 is a Bad Byte
B1S	B1 (Byte 1) Clock Strobe

B2	Loads High-Order Address Byte First (Byte 2)
B2S	B2 (Byte 2) Clock Strobe
B3	Loads Low-Order Address Byte Second (Byte 3)
B3RC	Byte 3 Read Clock
B3S	B3 (Byte 3) Clock Strobe
B34	Combination of B3 (Byte 3) and B4 (Byte 4) Clocks
B4	Byte 4 Active for 256 Bytes of Data Transfer
CAR	Carriage Read Status Bit (From Printer)
CCE	Cyclic Check Error
CCL	Counter Clear
CD0	Chip Select Drive Memory Bank 0
CE	Chip Enable
CE0-CE3	Chip Enable Memory Bank 0-3
CEA	Completion of 1 Byte/256 Byte Write
CEP	Chip Enable Parallel
CHAR	Select R/W Character (CRT Memory)
CHAR VIDEO	Character Video Display Dots to CRT
CHEK	Printer Malfunction Status
CH1-CH7	I/O Master Data Link Channel Select
CI	Character Inhibit
CICL	Character-In Clear
CISY	Controller In Sync
CK	Timing Clock Pulses (17.10 MHz)
CL1-CL4	Clear Interrupt Latches (Master CPU)
CL1-C16(±)	Channel Line Levels (Data Link)
CMS	Carriage Motion Strobe to Printer
CNTRLG	Select Control Bit R/W (CRT Memory)
CO	Cover Open Status Bit (PROM Printer)
CRC ERROR	Cyclic Redundancy Check Error
CRTR	Character
CTWT	CRT Write Clock Controls FIFO Timing during 256 Byte Disk Read and Slave Memory Write
C0-C6	Column Character Count
C4	Refresh Logic Clock

C1 C2208	Bit Counter Outputs (Disk Controller)
C4R	Refresh Clock
DATA OUT (DOUT 1-6) (DOUT 7-14)	Data Link Data Out (Serial) to 14 Slaves
DATA STROBE (DTSB)	Strobes Data from the output ports into the printer
DAX	Inhibits any more Keystrokes for approximately 10 ms
DA1A-DA12A	Data Lines to Printer (I/O)
DBIN	Data Bus In Clock to 8080
DCC	Data Compare Clock
DCE	Data Read from Disk to FIFO Complete
DCG	Disk Counter Clock (Increments Addresses for Loading Disk Data into FIFO)
DE	Data Entry
DFI0-DFI7	Data First In (From Disk to Master Memory)
DFO0-DFO7	Data First Out (From FIFO to Serialization Register or Disk)
DHDS	Disk Head Select (Hard)
DHER	Disk Hardware Error (Hard)
DICK	Data In Clock (Clocks Data into FIFO Output Latch)
DIP	Data In Parity
DIS	Data In Strobe
DISA	Data In Strobe for Address
DI0-DI7	Data In to S.R. for Slaves, Master or Disk (From FIFO)
DLCL	Data Link Clear
DLER	Data Link Error
DLG	Data Load Gate (From Disk) Selects Disk Word on MDL for Parity Check during Disk Read
DL RES	Data Link Reset
DMA	Direct Memory Access
DMA_0-DMA_{15}	DMA Memory Address Bits (Includes Bank Select)
DMAC	Direct Memory Access Complete
DMACE	DMA Chip Enable (Read PROM/RAM)

DMA R/B	DMA Ready/Busy 8080 Control
DMA R/W	DMA Read/Write Control
DOL	Data Out Parallel Load of S/P Register
DOS	Data Order Stored
DOT	Dot for CRT Display
DO0-DO7	Data Out Read from Disk to FIFO
DO7	Serial Data to Disk from Controller
DP8	Parity Bit In/Out of Memory
DPY	Data Parity to Memory from MDL Parity Checker
DP_8IN	Parity Bit Out of CRT Memory and W.S. Memory to W.S. Data Link
DP_8OUT	Parity Bit In to Memory
DP_0-DP_7	Bidirectional Memory Bus (RAM)
DRD	Data Read Signal Initiates 256 Byte Disk Read
DRDG	Data Read Gate/Word Select Gate for Data from Disk or Serilization Register
DR_0-DR_7	PROM Data Out (ROM)
DSKS	Disk Select (Hard) (Removable/Fixed Platter)
DSML	Data Strobe Memory Load
DT1	One Dot Video Time
DT3CK	Video Dot Space
DT89	CRT Load Clock
D_0-D_7	8080 Bidirectional Data Bus
D0C-D7C	CRT Memory Character Data Out to Display (W.S.)
D0I-D7I	Data In from Data Link
D_0M-D_7M	Bidirectional DMA Bus to Master 8080, Memory and Data Link
D4S-D7S	Control Bit Data Out of CRT Memory to Display (W.S.)
D8PC	Parity Bit for Character Data Out to Display
D8S	Parity Bit for Control Bit Data to Display
EOF	End Of Format
EOR	End Of Read
EOW	End Of Write
EOWF	End Of Write Format
ERGT	Erase Gate

ERWF	End Of Read/Write Format
FCS	Format Command Stored
FDS	Floppy and Hard Disk Select
FICK	First In Clock (Latches Data for Transfer into FIFO)
FIWT	Writes Data into and Reads Data Out of FIFO
FL	Fault Lamp (Printer Indicator)
FRDY	File Ready (Hard)
HB	Horizontal Blank
HB0 HB15	Header Byte Bits 0 15
HDIR	Head Direction In/Out (Floppy)
HLD1	Head Load #1 (Floppy)
HDL2	Head Load #2 (Floppy)
HDR ERR	Header Address Error
HDWR ERR	Hardware Error
HDST	Head Disk Step (Hard)
HDT0 HDT8	Hard Disk Track (Cylinder) Address Bits
HS	Horizontal Sync
HSTP	Head Step (Floppy) In or Out
INDEX 1,2	Index Pulses for Timing Sector Count (Soft)
INIDF, INDF	Initiate Data Flow
INITE, INITE 1, INITE 3	Initiate Enable
INP	Input Instruction - 8080 Addresses Peripheral Device for Data Transfer IN
INPUT PRIME	Resets Printer
INST	In Status (From Addressed Slave)
INST	Instruction and Header Byte Decode Enable to Slaves
INST R/B	Instruction Ready/Busy sets DMA R/B
IN SYNC	Start Bit Detected and Synced
INT	Keyboard Interrupt to 8080
INTA	Interrupt Acknowledge (Status Word)
INTE	Interrupt Enable (8080 Interrupt F/F set to allow Interrupts to be processed)
INTS	Intensity Control Bit for CRT

IS	Instruction Start
ISL	Instruction Start Latch
K0-K6	Keyboard Data
KS	Keyboard Strobe
LAI	Logical Address Interlock (Hard)
LE	Line Error
LINE ERROR	Data Link Parity Error
LINE0-LINE9	Raster Line Count
LOAD DES	Load Destination (Move OPT)
LOCK	Shift Key Lock
LS	Keyboard Input Load Strobe
LSR	Load Serialization Register
LTZ	Logical Track Zero Signal from Floppy Drive
MEBIN	Memory Byte-In Read Clock to 8080
MEMPAR	Memory Parity Bit for Data Link Data Out
MEMR	8080 Memory Read (Status Bit)
MEMWO	8080 Memory Write (Status Bit)
MER	Memory Error
MER/W1-MER/W4	Memory Read/Write Strobes
MOVE	Initiates High Speed 256 Byte Transfers between Memories
M1	Memory Cycle Time 1
MP	Matrix Printer
MR	Master Reset
MRCL1,4	Clears Memory and Data Link Error Interrupts
M_1	8080 Machine Cycle 1 (Fetch) of Instruction
NR	Not-Running (Printer and Workstation Status Bit)
OP	Operation Reset
OPCL	Operation Clear
OPCOM	Operation Complete
OPS	Operation Start
OUT	Output Instruction (8080 Addresses Peripheral Device and Transfers Data OUT)
OUTS	Keyboard Strobe Interrupt to 8080
PAR IN	Parity In From Data Link

PAR COMP	Parity Compare
PAR OUT	Parity Out of Parity Gen/Chkr from Data Link
PE	Parallel Enable for Data In
PFS	Paper Feed Strobe to Printer
PFR	Paper Feed Ready from Printer/Punch
PL	Paper Out Lamp
PO	Paper Out from Printer
PR	Power On
PROM	Inhibits Parity Error when Reading PROM
PRY	Printer Ready/Punch Ready
PSL	Program Stop Lamp
PTY ERR	Parity Error
PWR	Print Wheel Ready
PWS	Print Wheel Strobe
PWR RES	Power Reset for 8080
QA-QD	Line Counters
-RA,-RB	Receive Coax Line (Red)
RA0-RA5	Refresh Address Rows
R/B	READY/BUSY
RC	Receive Complete
RCK	Read Clock
RCS	Read Command Stored
RDD	Read Data
RDG	Read Gate
RDI	Read Data In
RDY	Ready Floppy
RD1-RD7	Channel Select Read from Slave
RDMY	8080 Read Memory Inhibit during DMA Transfer Inhibits 8080 R/W during DMA (Busy)
READY/BUSY	8080 In Processing State when High-Busy-Low when Bus is in DMA
READ	Memory Read Decoded from Address and Data Bus
REC	Receive Mode of Operation (From Instruction Register)
RECINT	Receive Interrupt caused by 20 us Time-Out (No Data)

REF	Refresh Signal for RAM Memory
REFST	Refresh Start from Debug
RES	Reset from Debug
RESET	Initializes the Current 8080 Program to Location Address "0000"
REST	I/O Restore Command to Printer
RESTRT	An Interrupt that causes a Retry of an Operation that was caused by a Data Link Error
RESM	Reset Machine
RFD	Resync For Data
RGA	Read Gate Allow (R/W) signal from Disk
RL	Out of Ribbon Lamp
RLT	Ribbon Lift
ROCO	Printer Signal Indicating Ribbon Out/Cover Open
RSA	Resync Allowed
RSAC	Resync Allow Clock
RSOP	Reset Operation
RSTR	Restore Hard Disk R/W Head to Cylinder Track 0
RSTRT	Used to Reset Slaves via Data Link Headed Byte (Restart)
R/W	(Read/Write) Instruction Register Bit Write=1, Read=0
R0-R4	Row Character Counter
SCCY	Slave Counter Address (Carry Out) Last Address of FIFO Read
SCD	Sync Character Detected
SCE	256 Byte Read of FIFO Complete (Slave Data Complete)
SCG	Slave Counter Gate (From FIFO Control)
SCK	Serial Clock
SDI	Serial Data In
SDO	Serial Data Out
SDR	Shift During Read
SECTOR 2,1	Sector Pulse From Floppy Disk Drive
SEL	Select Push-Button on Printer initiates SELECT/DESELECT Logic
SEMST	Semaphore Status of Slave (1-Byte)

SFL1, SFL2	Select Floppy 1 and 2
SHC	Strobe Header lCheck
SHD1,2	Select Hard Disk 1 and 2
SHLED	Shift Key Indicator Lamp Enable on Keyboard (upper case)
SH KEY	Shift Key
SIC	Seek Incomplete (Hard)
SIE	Step Into Eight
SINPT	Set Interrupt Bit
SINR	Set Interrupt
SI0-SI10	Data Loaded In for Serialization or Parallel Formatting
SL	Select Lamp on Printer
SLO0	Select Zero, Master Select on Data Link
SLD	Data in from Slaves (Slave Data)
SLT1-2,4,8	Select Device (Up to 14) Device Channel Select
SLT0	Master Select for DMA Disk Read
SMCL	Slave Memory Clear
SMWT	Master CPU Signal for Slave Memory Write (1 Byte or 256 Byte Transfer)
SO0-SO7	Parallel Data Out of Serialization Register
SOP	Surface Operation
SPK	Audio Speaker
SPP	Sector Pulse Present
SPPD	Sector Pulse Present Detected
SPPF	Sector Pulse Presetn Floppy
SPPH	Sector Pulse Present Hard Disk
SPY	Parity Bit for Data to be Serialized for Data Link Transfer
SRC	Serialization Register Clock (PTR)
SRCL	Serialization Register Clear (PTR)
SRCK	Serial Register Shift Clock
SRG	Serialization Register Gate
SRLD	Serialization Register Load
SSM	Send Serial Data to Slave Memory Request

SRR	Set Read Request (928 Memory)
SRW	Seek/Read/Write (Hard)
SSR	Shift Serialization Register Clock
STATUS/1 BT	1 Byte Status Read of a Slave via DMA (Master CPU Busy)
STATUS	Header Word Instruction for Status Request
STCL	Clears Status Instruction
STG	Shorten the Gap (Not used on print)
SYNC	Output 8080 Sync Clock which identifies the beginning of every Machine Cycle
S1 S5	Sector Count from Hard Disk Register
TC	Carry Out of 256 Byte (Write) Transfer - Clears Instruction
TCB	Carry Out of 256 Byte (Read) Transfer - Clears Instruction
TCCLK	10 MS Tick Clock Interrupt
TCOP	Telecom Operation
TCL	Start Bit Detect and Sync F/Fs enabled (Time Out Clear)
TEA	Debug Disable Interrupts
TOF	Top of Form
TWR	Debug RDY/BSY Control
T1	Byte Timing Pulse for Latching Hi-Order DMA Address Byte
T2	Byte Timing Pulse for Loading Lo-Order DMA Address Byte
T3	Byte Timing Pulse for 1-Byte Transfer
T4	Byte Timing Pulse for 256-Byte Transfer
VB	Vertical Blank (Vertical Retrace)
VS	Vertical Sync
WAIT	8080 Processor in WAIT State (READY Line Low)
WCD	Write Clock Data (Floppy)
WCDH	Write Clock Data (Hard Disk)
WCE	Write Check Error
WCS	Write Command Stored

WGA	Write Gate Allow
WGT	Write Gate Time
WMR	Write Memory Request
WO	8080 Memory Write
WPC	Wide Platen CRT (Slave ID Code)
WPT	Write Protect
WPY	Write Parity
WPYC	Write Parity Clock
WR	8080 Output used with OUT Instruction to Write to Peripheral Devices
WRT	Power Up Clear for Printer Data Link
WRGA	Write/Read Gate Allow
WRGT/ERGT	Write Gate/Erase Gate
WRITE A	Write Memory Control
WRITE B	Write to Memory from 8080
WTG	Write The Gap
WTR	Wolftrap (Power Reset) from J5 of Power Supply (POWER-UP CLEAR)
$0_1, 0_2$	Timing Clocks for 8080 (Phase 1, Phase 2)
1 BT	Instruction Bit for 1 Byte Transfer
256 BT	Instruction Bit for 256 Byte Transfer
1B2	1 Byte Transfer B2 Clock
1B4W	1 Byte Transfer B4 Write Clock
1BB4	One Byte transfer B4 Clock
1 BYST	
1 BYTE	1 BYTE
1BYTR	One Byte Transfer
1TIC	1 Byte Transfer is Complete
256 Byte	256 Byte Read
256 BYTR	256 Byte Transfer
256DW	256 Bytes of Data to be Written on Disk
256 SD	256 Bytes of Slave Data to be transferred
8080	8080 Processor
-6A,+6B	Transmit Coax Line (Green)

APPENDIX B

APPENDIX "B"
GLOSSARY

TO BE SUPPLIED

This Appendix will be completed and incorporated during publication of the final issue of Volume 3.

APPENDIX C

APPENDIX "C"
RELATED PUBLICATIONS

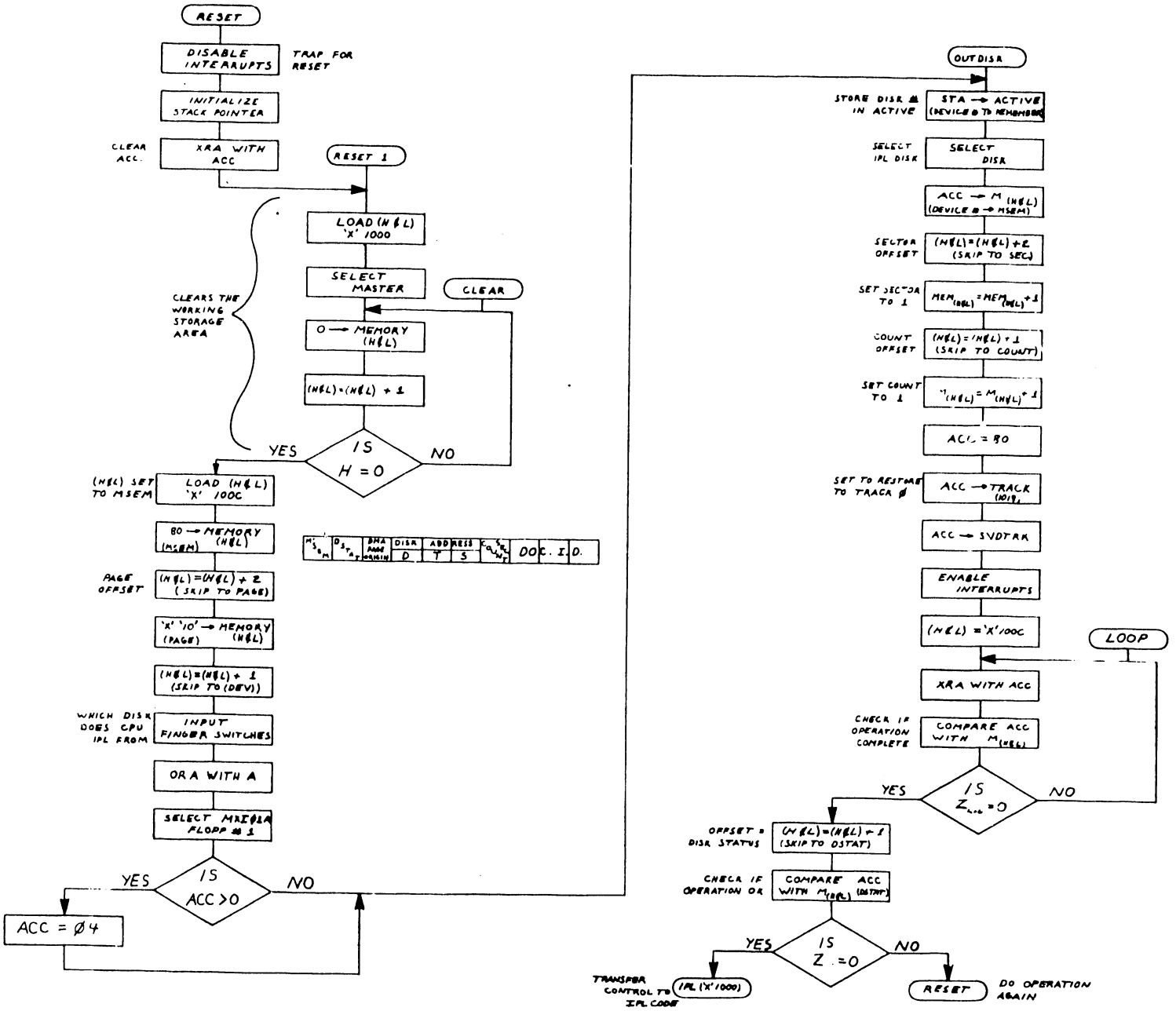
TITLE/ORIGINATOR	DOC #	ISSUED BY AND DATE
Word Processing Newsletters (WPNL's - WANG)	Various	Wang Labs Inc. Cust. Eng. Div. Various
Field Level Maintenance Manual Model 928 Systems 10/20/30 Volume 1	03-0034-P1	Wang Labs Inc. Cust. Eng. Div. March 77
Field Level Maintenance Manual Model 928 Systems 10/20/30 Volume 2	03-0034-PL	Wang Labs Inc. Cust. Eng. Div. March 77
Field Level Maintenance Guide Diablo Series 40 Disk Drives	03-0057	Wang Labs Inc. Cust. Eng. Div. July 77
CDC Hawk Disk Training Guide (Reprint of CDC Document)	03-0059	Wang Labs Inc. Cust. Eng. Div. October 77
Field Level Maintenance Guide No. 1 Matrix Printers Models 72, 61, 77 Series 101, 102, 306	03-0060	Wang Labs Inc. Cust. Eng. Div. October 77

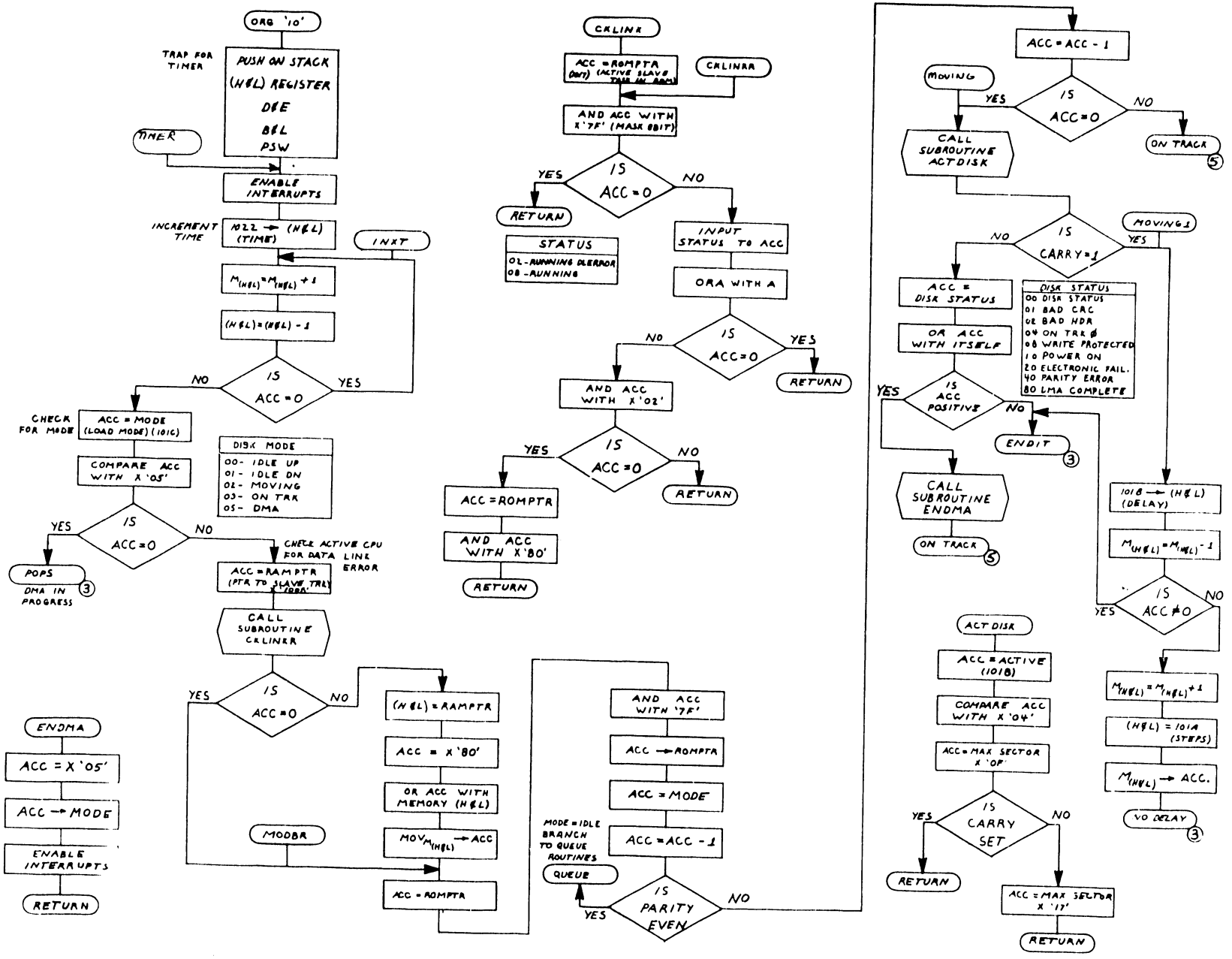
APPENDIX D

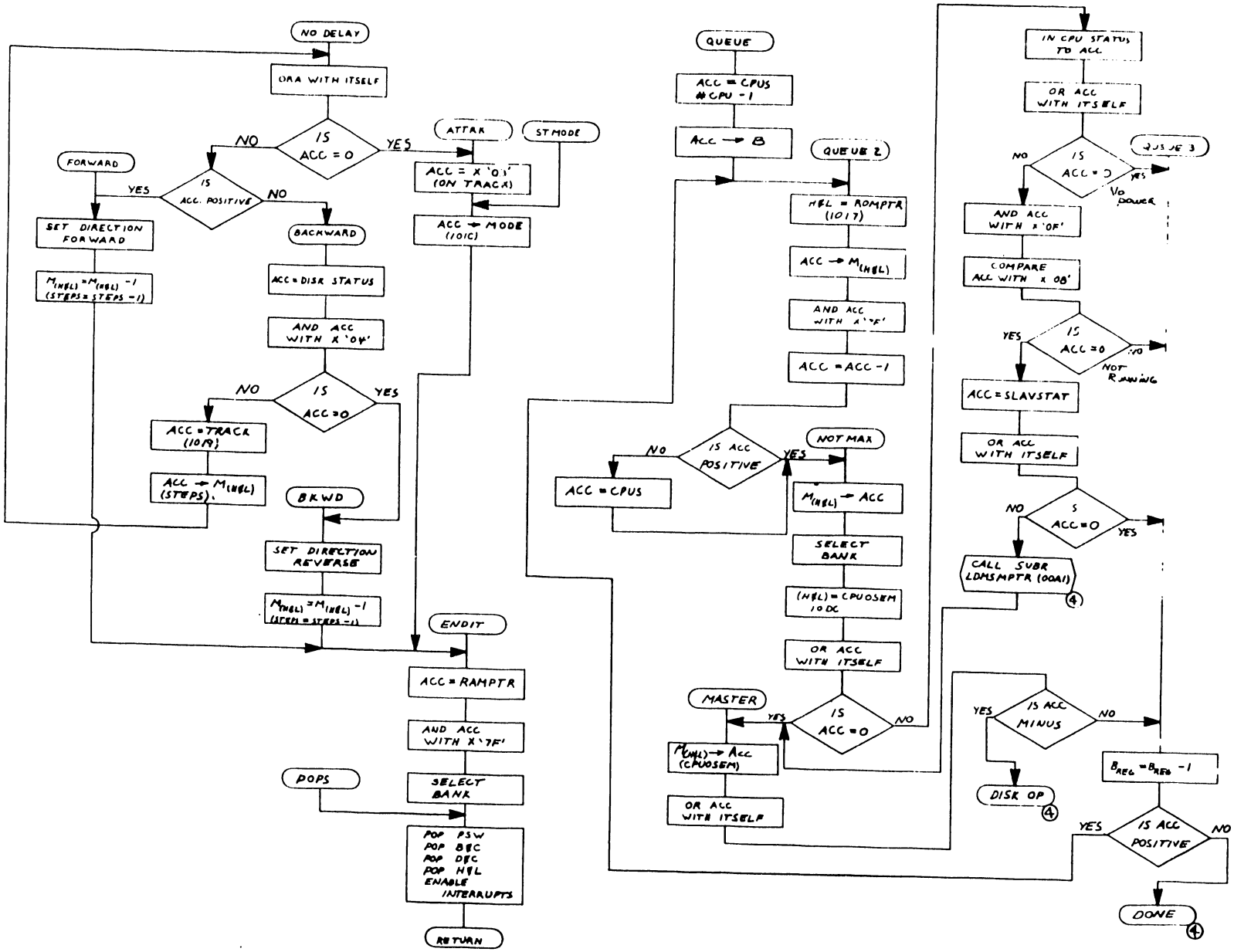
APPENDIX "D"

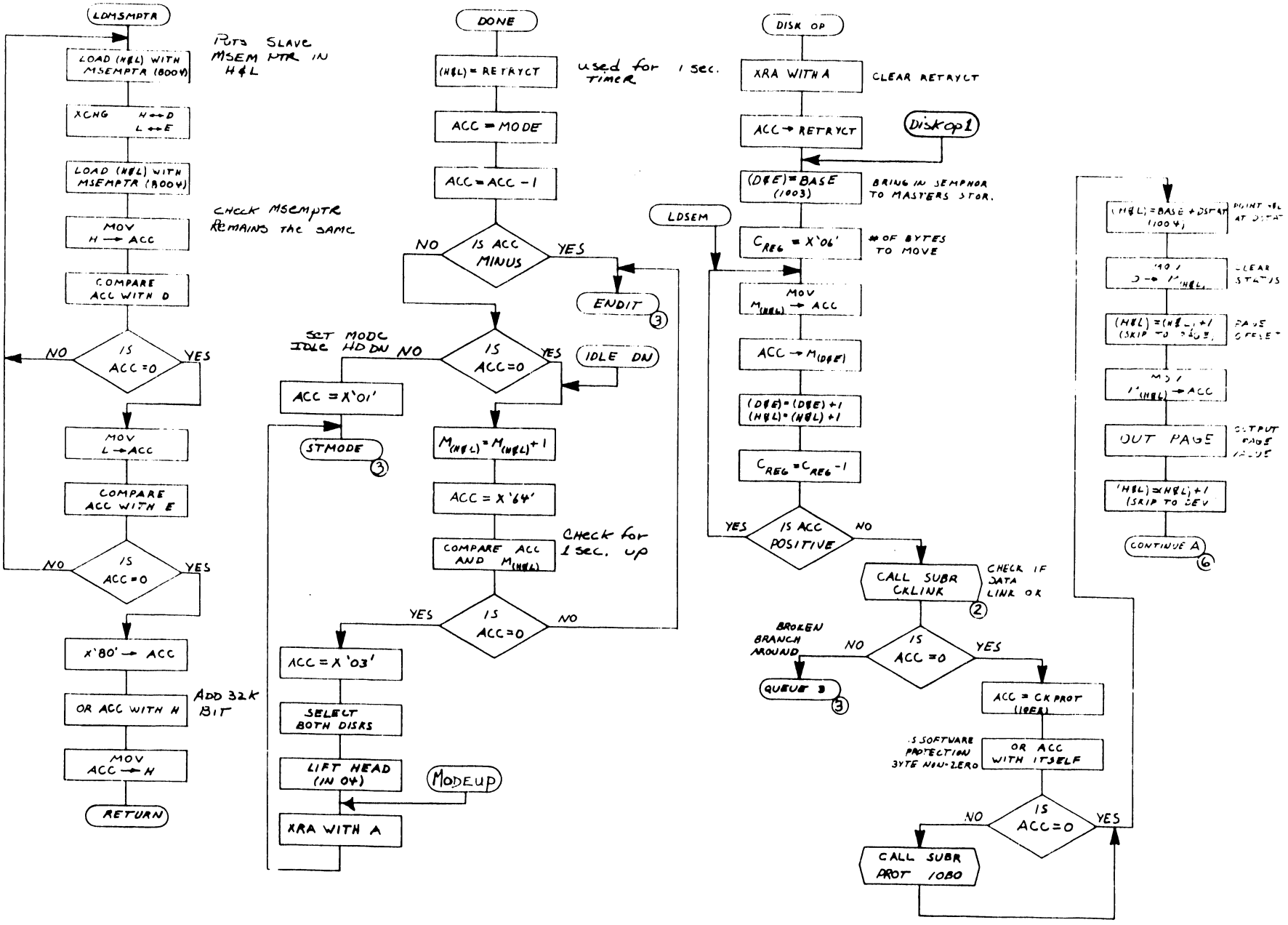
R7 PROM

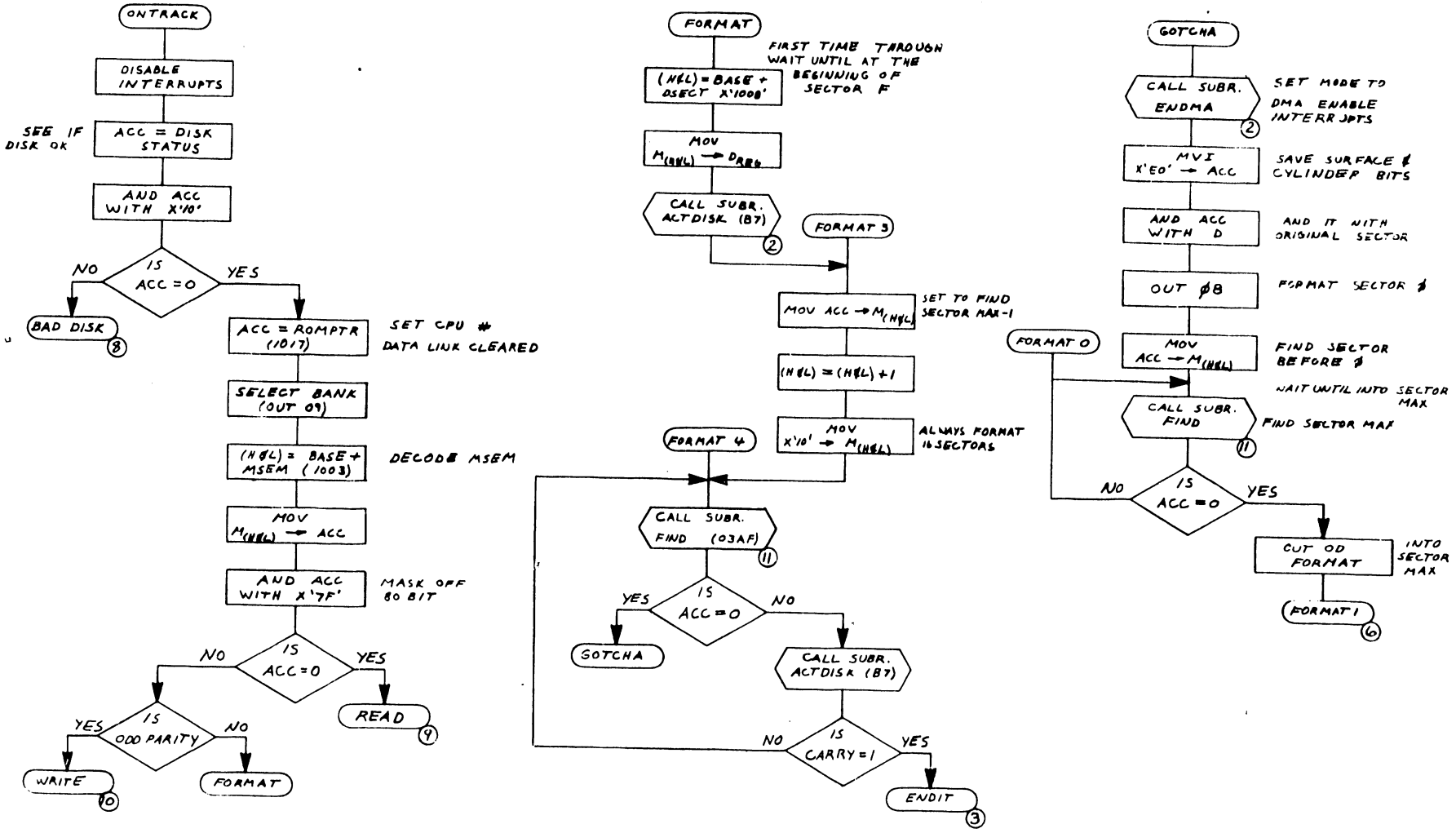
FLOW DIAGRAM

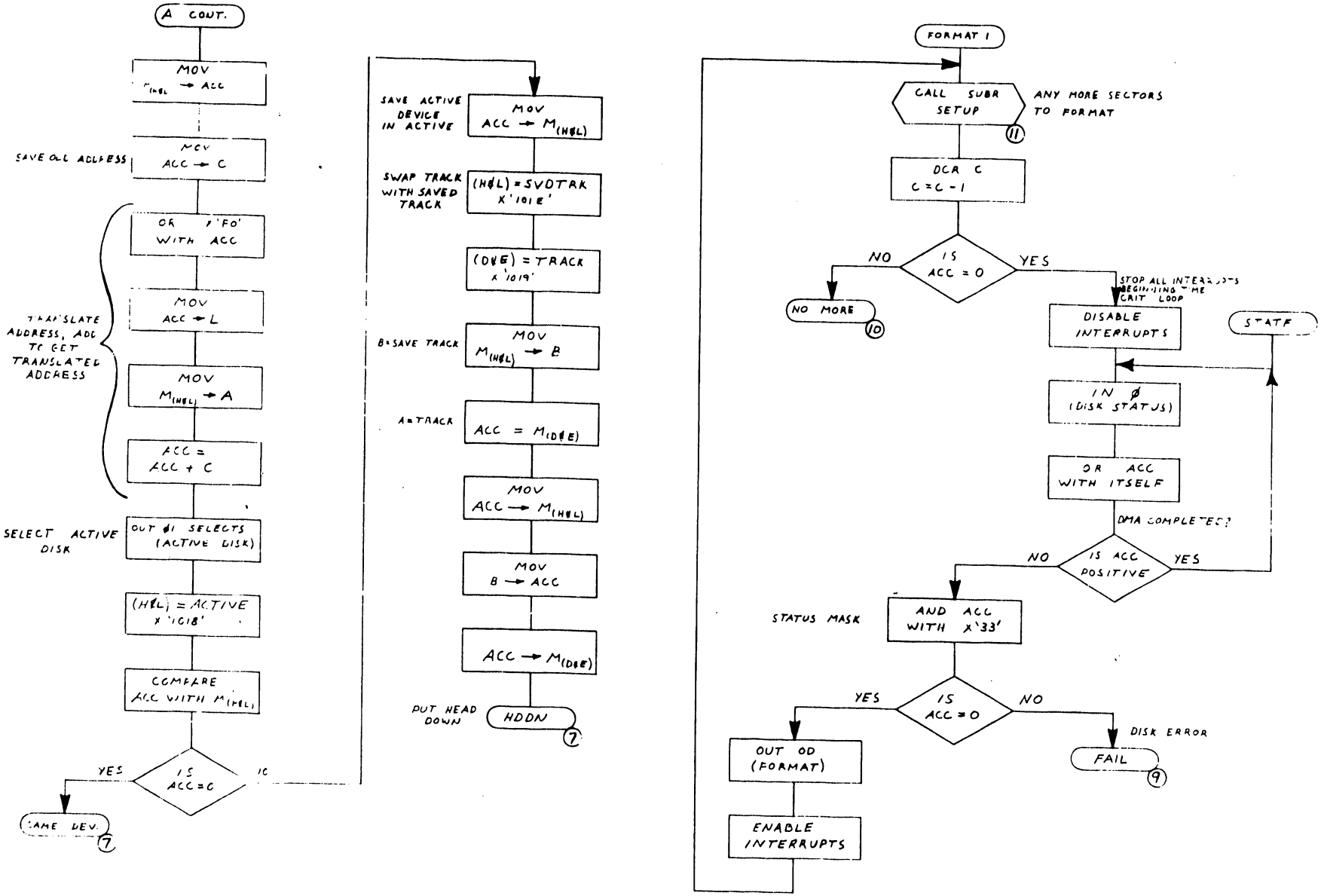

RESET
DISABLE INTERRUPTS
TRAP FOR RESET
INITIALIZE STACK POINTER
CLEAR ACC.
XRA WITH ACC
RESET 1
LOAD (H&L) 'X' 1000
SELECT MASTER
CLEAR
CLEARS THE WORKING STORAGE AREA
0 → MEMORY (H&L)
(H&L)=(H&L) + 1
YES
IS H = 0
NO
(H&L) SET TO MSEM
LOAD (H&L) 'X' 100C
80 → MEMORY (MSEM) (H&L)
PAGE OFFSET
(H&L)=(H&L) + 2 (SKIP TO PAGE)
'X' '10' → MEMORY (PAGE) (H&L)
(H&L)=(H&L) + 1 (SKIP TO (DEV))
WHICH DISK DOES CPU IPL FROM
INPUT FINGER SWITCHES
ORA WITH A
SELECT MXI&LA FLOPP # 1
YES
IS ACC > 0
NO
ACC = Ø4
MSEM
DSTAT
DMA ADDR CHANGE
DISK
ADDRESS
CMD WRT
DOC. I.D.
OUTDISR
STORE DISK # IN ACTIVE
STA → ACTIVE (DEVICE # TO REMEMBER)
SELECT IPL DISK
SELECT DISK
ACC → M (H&L) (DEVICE # → MSEM)
SECTOR OFFSET
(H&L)=(H&L)+2 (SKIP TO SEC)
SET SECTOR TO 1
MEM(H&L) = MEM(H&L) + 1
COUNT OFFSET
(H&L)=(H&L) + 1 (SKIP TO COUNT)
SET COUNT TO 1
M(H&L) = M(H&L) + 1
ACC = 80
SET TO RESTORE TO TRACK Ø
ACC → TRACK (HDIS)
ACC → SVDTRK
ENABLE INTERRUPTS
(H&L) = 'X' 100C
LOOP
XRA WITH ACC
CHECK IF OPERATION COMPLETE
COMPARE ACC WITH M(H&L)
YES
IS Z = 0
NO
OFFSET = DISK STATUS
(H&L)=(H&L) + 1 (SKIP TO DSTAT)
CHECK IF OPERATION OK
COMPARE ACC WITH M(H&L) (DSTAT)
YES
IS Z = 0
NO
TRANSFER CONTROL TO IPL CODE
IPL ('X' 1000)
RESET
DO OPERATION AGAIN

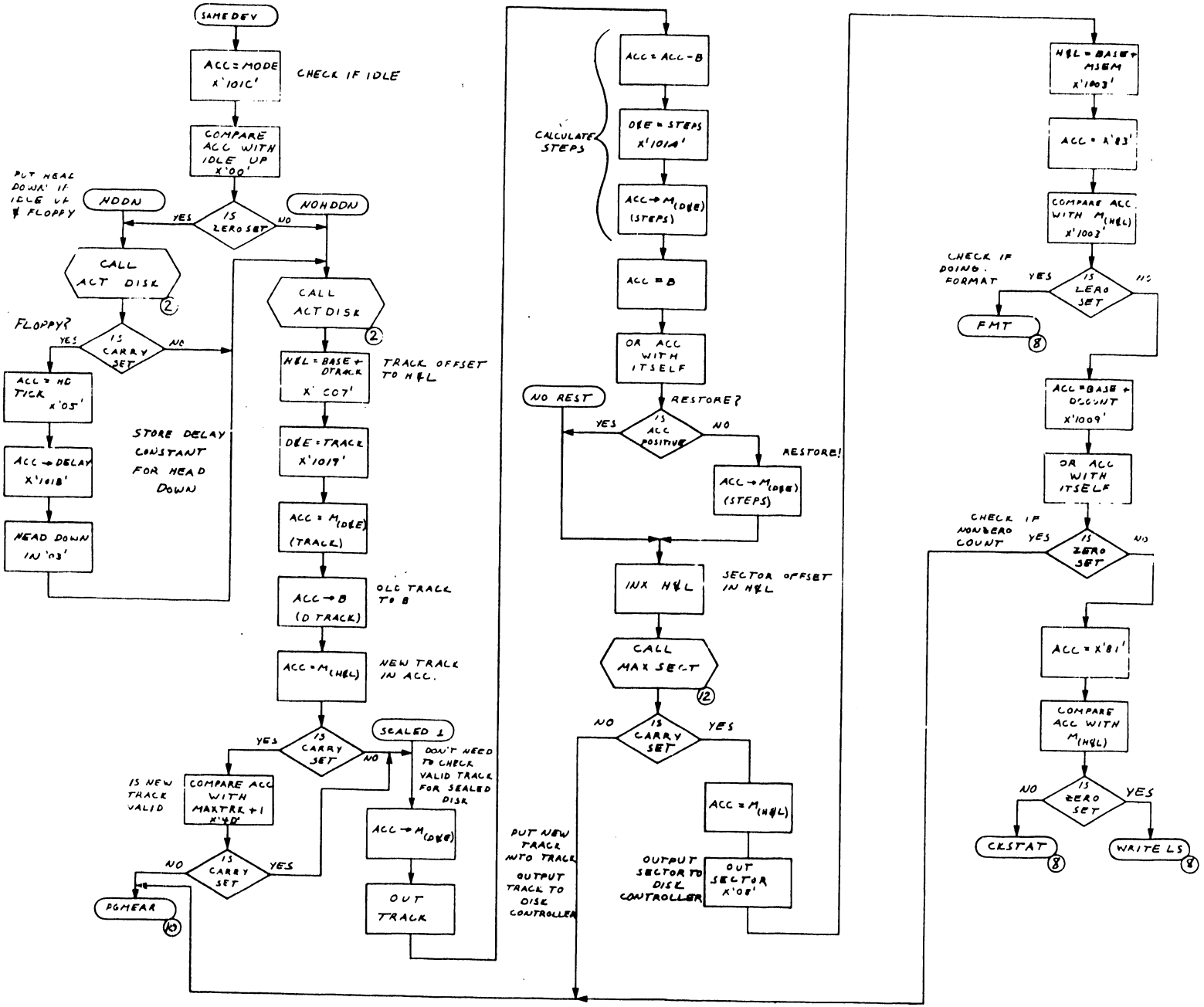

ORG '10'
TRAP FOR TIMER
PUSH ON STACK
(H&L) REGISTER
D&E
B&L
PSW
TIMER
ENABLE INTERRUPTS
INCREMENT TIME
1022 → (H&L) (TIME)
INXT
M(H&L) = M(H&L) + 1
(H&L) = (H&L) - 1
IS ACC = 0
NO
YES
CHECK FOR MODE
ACC = MODE (LOAD MODE) (101C)
COMPARE ACC WITH X '05'
DISK MODE
00- IDLE UP
01- IDLE DN
02- MOVING
03- ON TRK
05- DMA
IS ACC = 0
YES
NO
POPS
DMA IN PROGRESS
CHECK ACTIVE CPU FOR DATA LINE ERROR
ACC = RAMPTR (PTR TO SLAVE TBL) 1080
CALL SUBROUTINE CKLINKR
IS ACC = 0
YES
NO
(H&L) = RAMPTR
ACC = X '80'
OR ACC WITH MEMORY (H&L)
MOV M(H&L) → ACC
MODBR
ACC = ROMPTR
ENDMA
ACC = X '05'
ACC → MODE
ENABLE INTERRUPTS
RETURN
CKLINK
ACC = ROMPTR (DATA) (ACTIVE SLAVE TABLE IN ROM)
CKLINKR
AND ACC WITH X '7F' (MASK 8BIT)
IS ACC = 0
YES
NO
RETURN
STATUS
02 - RUNNING ON ERROR
08 - RUNNING
INPUT STATUS TO ACC
ORA WITH A
IS ACC = 0
NO
YES
RETURN
AND ACC WITH X '02'
IS ACC = 0
YES
NO
RETURN
ACC = ROMPTR
AND ACC WITH X '80'
RETURN
AND ACC WITH '7F'
ACC → ROMPTR
ACC = MODE
ACC = ACC - 1
MODE = IDLE BRANCH TO QUEUE ROUTINES
QUEUE
IS PARITY EVEN
YES
NO
ACC = ACC - 1
MOVING
IS ACC = 0
YES
NO
ON TRACK (5)
CALL SUBROUTINE ACTDISK
IS CARRY = 1
NO
YES
MOVING 1
ACC = DISK STATUS
OR ACC WITH ITSELF
DISK STATUS
00 DISK STATUS
01 BAD CRC
02 BAD HDR
04 ON TRK 0
08 WRITE PROTECTED
10 POWER ON
20 ELECTRONIC FAIL.
40 PARITY ERROR
80 LMA COMPLETE
IS ACC POSITIVE
YES
NO
ENDIT (3)
CALL SUBROUTINE ENDMA
ON TRACK (5)
1018 → (H&L) (DELAY)
M(H&L) = M(H&L) - 1
IS ACC ≠ 0
YES
NO
M(H&L) = M(H&L) + 1
(H&L) = 101A (STEPS)
M(H&L) → ACC.
VO DELAY (3)
ACTDISK
ACC = ACTIVE (1018)
COMPARE ACC WITH X '04'
ACC = MAX SECTOR X '0F'
IS CARRY SET
YES
NO
RETURN
ACC = MAX SECTOR X '11'
RETURN

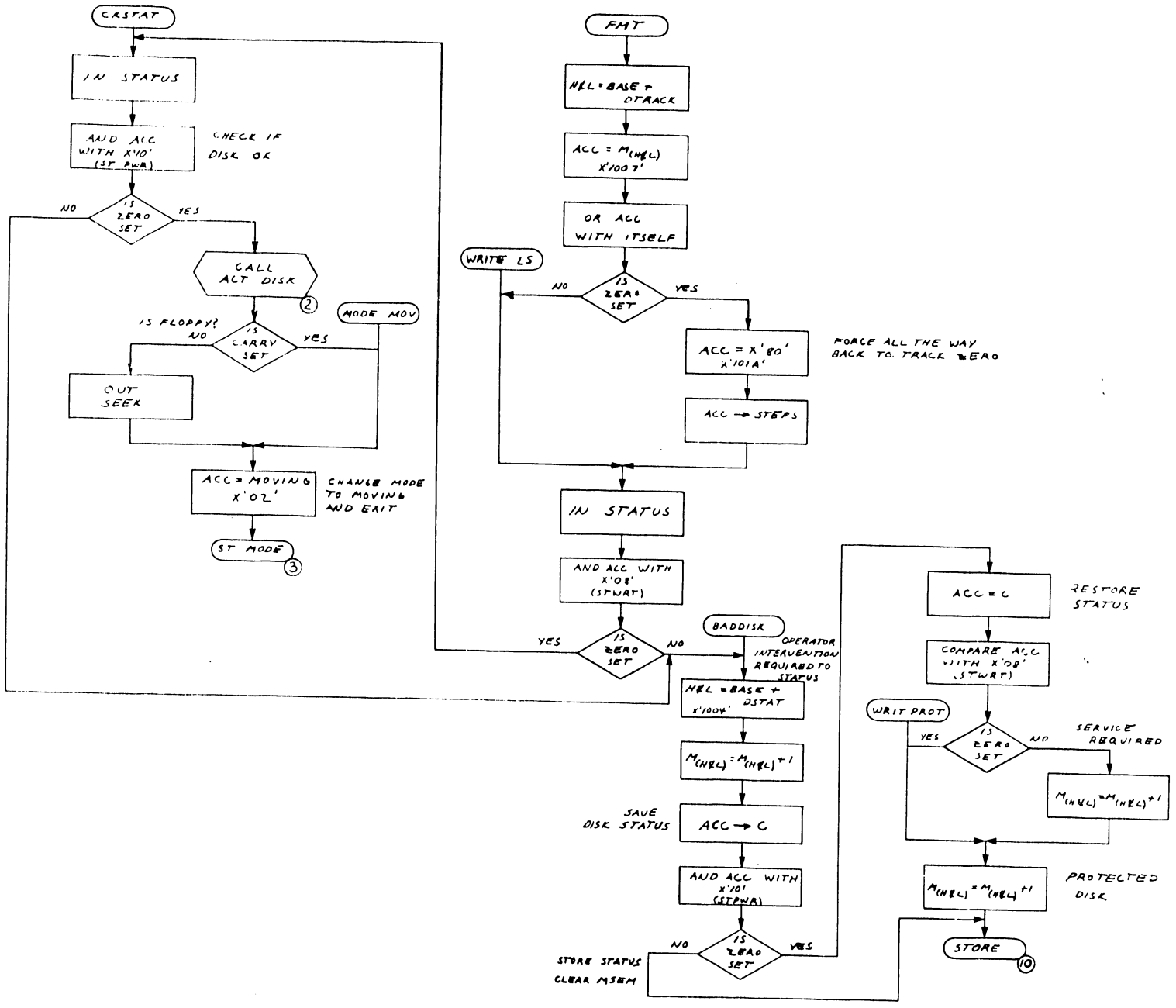

NO DELAY
ORA WITH ITSELF
IS ACC = 0
NO
YES
ATTAR
ST MODE
ACC = X '01' (ON TRACK)
ACC → MODE (101C)
FORWARD
IS ACC. POSITIVE
YES
NO
SET DIRECTION FORWARD
BACKWARD
ACC = DISK STATUS
AND ACC WITH X '04'
IS ACC = 0
ACC = TRACK (1019)
ACC → M(HL) (STEPS).
BKWD
SET DIRECTION REVERSE
M(HL) = M(HL) - 1 (STEPS = STEPS - 1)
ENDIT
ACC = RAMPTR
AND ACC WITH X '7F'
SELECT BANK
POPS
POP PSW
POP BC
POP DE
POP HL
ENABLE INTERRUPTS
RETURN
QUEUE
ACC = CPUS #CPU - 1
ACC → B
QUEUE 2
HL = RAMPTR (1017)
ACC → M(HL)
AND ACC WITH X '7F'
ACC = ACC - 1
IS ACC POSITIVE
NO
YES
ACC = CPUS
NOT MAX
M(HL) → ACC
SELECT BANK
(HL) = CPUOSEM 10DC
OR ACC WITH ITSELF
IS ACC = 0
NO
YES
MASTER
M(HL) → Acc (CPUOSEM)
OR ACC WITH ITSELF
IN CPU STATUS TO ACC
OR ACC WITH ITSELF
IS ACC = 0
NO
YES
Vo POWER
AND ACC WITH X '0F'
COMPARE ACC WITH X '08'
IS ACC = 0
YES
NO
NOT RUNNING
ACC = SLAVSTAT
OR ACC WITH ITSELF
S ACC = 0
NO
YES
CALL SUBR LDMSMPTR (00A1)
4
IS ACC MINUS
YES
NO
DISK OP
4
B_REG = B_REG - 1
IS ACC POSITIVE
YES
NO
DONE
4

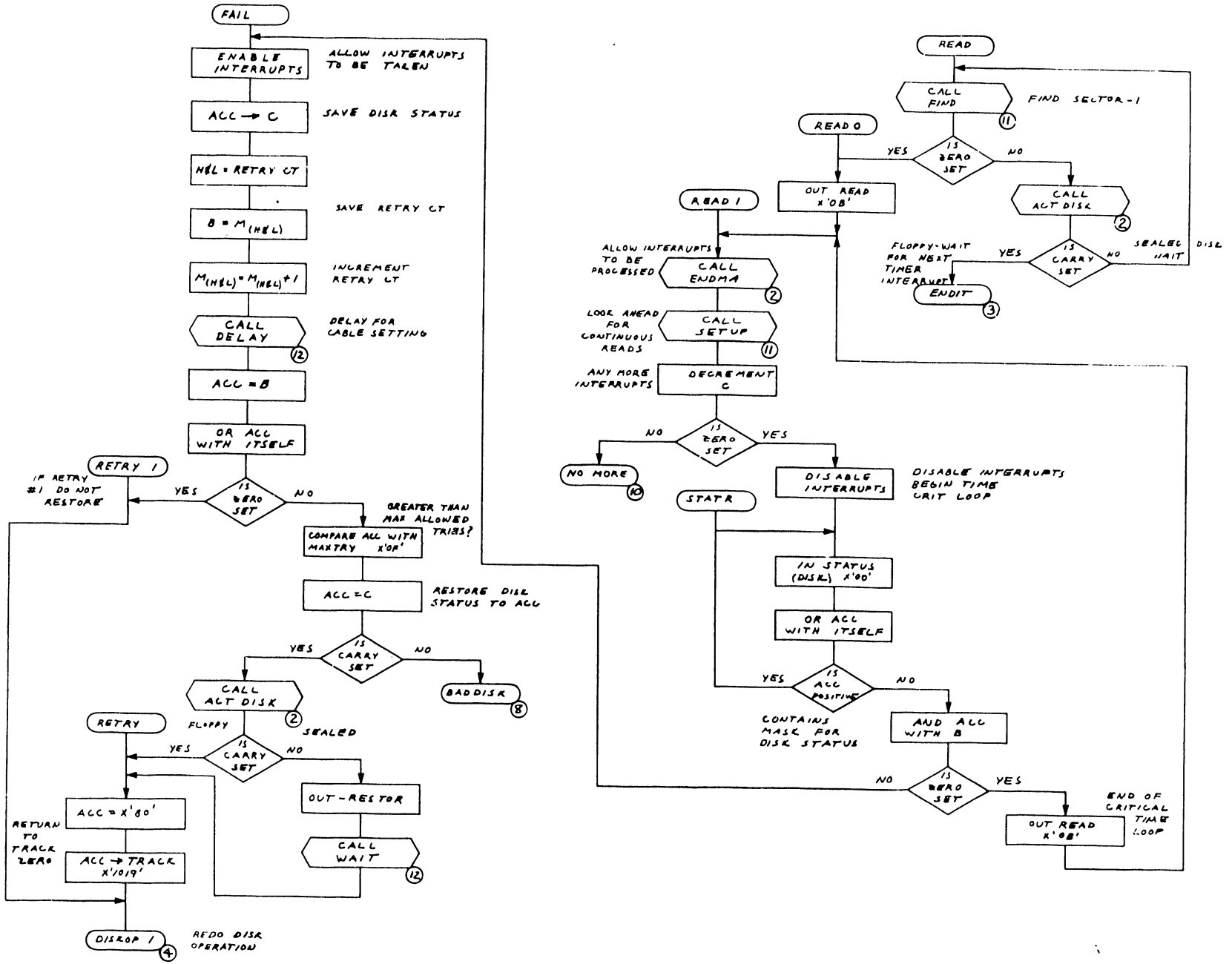

LDMSMPTR
LOAD (H&L) WITH MSEMPTA (800H)
PUTS SLAVE MSEM PTR IN H&L
XCHG H↔D L↔E
LOAD (H&L) WITH MSEMPTR (800H)
CHECK MSEMPTR REMAINS THE SAME
MOV H → ACC
COMPARE ACC WITH D
IS ACC =0
NO
YES
MOV L → ACC
COMPARE ACC WITH E
IS ACC =0
NO
YES
X'80' → ACC
ADD 32K BIT
OR ACC WITH H
MOV ACC → H
RETURN
DONE
(H&L) = RETRYCT
used for 1 sec. TIMER
ACC = MODE
ACC = ACC - 1
IS ACC MINUS
NO
YES
ENDIT
3
SET MODE IDLE HD DN
NO
IS ACC=0
YES
IDLE DN
ACC = X'01'
STMODE
3
M(H&L) = M(H&L) + 1
ACC = X'64'
COMPARE ACC AND M(H&L)
Check for 1 sec. up
YES
IS ACC=0
NO
ACC = X'03'
SELECT BOTH DISKS
LIFT HEAD (IN 04)
MODEUP
XRA WITH A
DISK OP
XRA WITH A
CLEAR RETRYCT
ACC → RETRYCT
Diskop1
(D&E) = BASE (1003)
BRING IN SEMPHOR TO MASTERS STOR.
LDSEM
C_REG = X'06'
# OF BYTES TO MOVE
MOV M(H&L) → ACC
ACC → M(D&E)
(D&E) = (D&E) + 1
(H&L) = (H&L) + 1
C_REG = C_REG - 1
YES
IS ACC POSITIVE
NO
CALL SUBR CKLINK
CHECK IF DATA LINK OR
2
BROKEN BRANCH AROUND
NO
IS ACC =0
YES
QUEUE 3
3
ACC = CK PROT (10EA)
:S SOFTWARE PROTECTION BYTE NON-ZERO
OR ACC WITH ITSELF
NO
IS ACC=0
YES
CALL SUBR PROT 1080
(H&L) = BASE + DSTAT (1004)
POINT H&L AT DSTAT
'40' → M(H&L)
CLEAR STATUS
(H&L) = (H&L) + 1 (SKIP TO PAGE OFFSET)
PAGE OFFSET
M(H&L) → ACC
OUT PAGE
OUTPUT PAGE VALUE
(H&L) = (H&L) + 1 (SKIP TO DEV
CONTINUE A
6

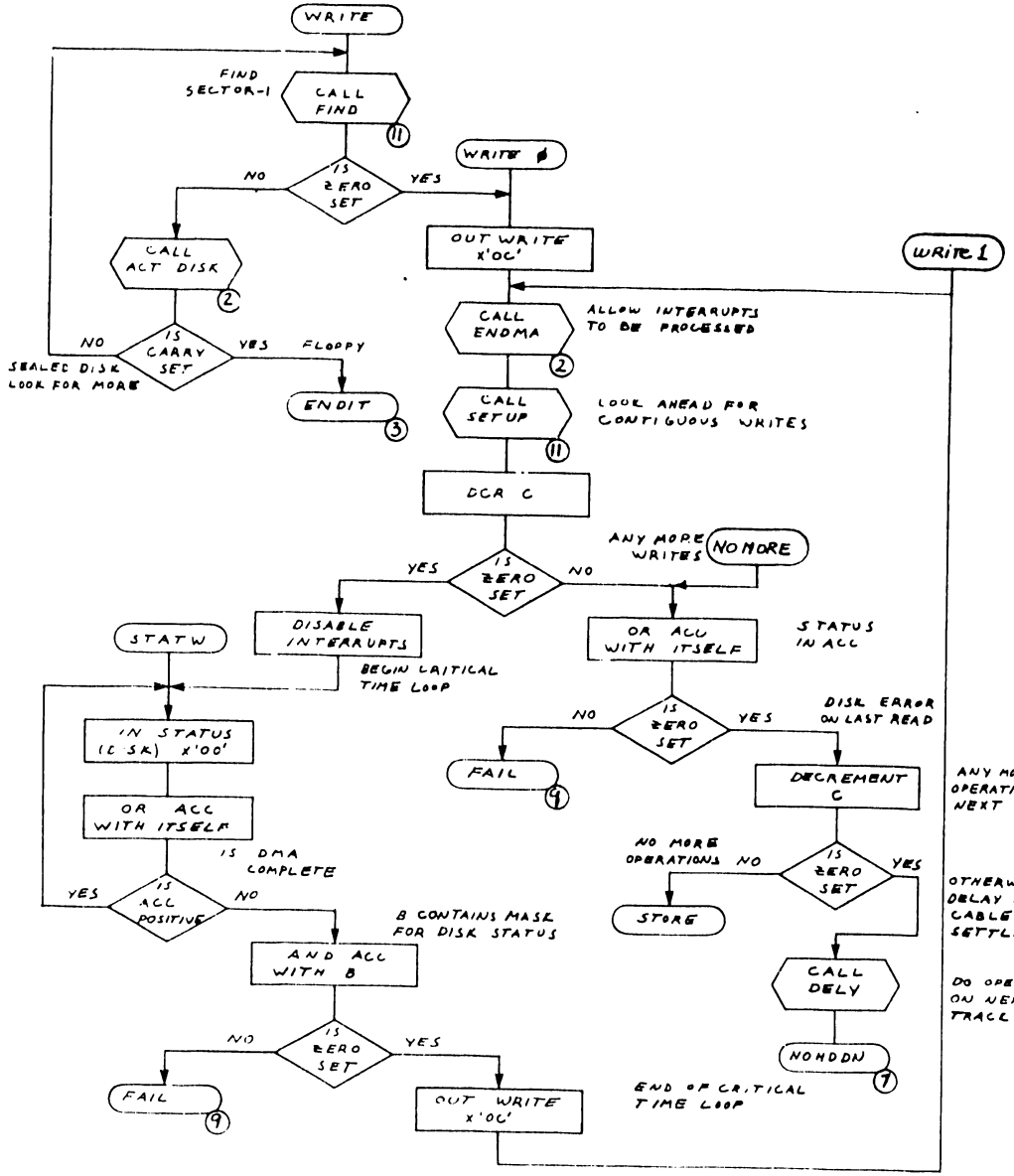

ONTRACK
DISABLE INTERRUPTS
SEE IF DISK OK
ACC = DISK STATUS
AND ACC WITH X'10'
IS ACC = 0
NO
YES
BAD DISK
8
ACC = ROMPTR (1017)
SET CPU # DATA LINK CLEARED
SELECT BANK (OUT 09)
(H&L) = BASE + MSEM (1003)
DECODE MSEM
MOV M(H&L) → ACC
AND ACC WITH X'7F'
MASK OFF 80 BIT
IS ACC = 0
NO
YES
READ
9
IS ODD PARITY
YES
NO
WRITE
10
FORMAT
FORMAT
FIRST TIME THROUGH WAIT UNTIL AT THE BEGINNING OF SECTOR F
(H&L) = BASE + DSECT X'1008'
MOV M(H&L) → DRR6
CALL SUBR. ACTDISK (B7)
2
FORMAT 3
MOV ACC → M(H&L)
SET TO FIND SECTOR MAX-1
(H&L) = (H&L) + 1
MOV X'10' → M(H&L)
ALWAYS FORMAT 16 SECTORS
FORMAT 4
CALL SUBR. FIND (03AF)
11
IS ACC = 0
YES
NO
GOTCHA
CALL SUBR. ACTDISK (B7)
IS CARRY = 1
NO
YES
ENDIT
3
GOTCHA
CALL SUBR. ENDMA
2
SET MODE TO DMA ENABLE INTERRUPTS
MVI X'E0' → ACC
SAVE SURFACE & CYLINDER BITS
AND ACC WITH D
AND IT WITH ORIGINAL SECTOR
OUT ø8
FORMAT SECTOR ø
FORMAT 0
MOV ACC → M(H&L)
FIND SECTOR BEFORE ø
WAIT UNTIL INTO SECTOR MAX
CALL SUBR. FIND
11
FIND SECTOR MAX
IS ACC = 0
NO
YES
OUT OD FORMAT
INTO SECTOR MAX
FORMAT 1
6

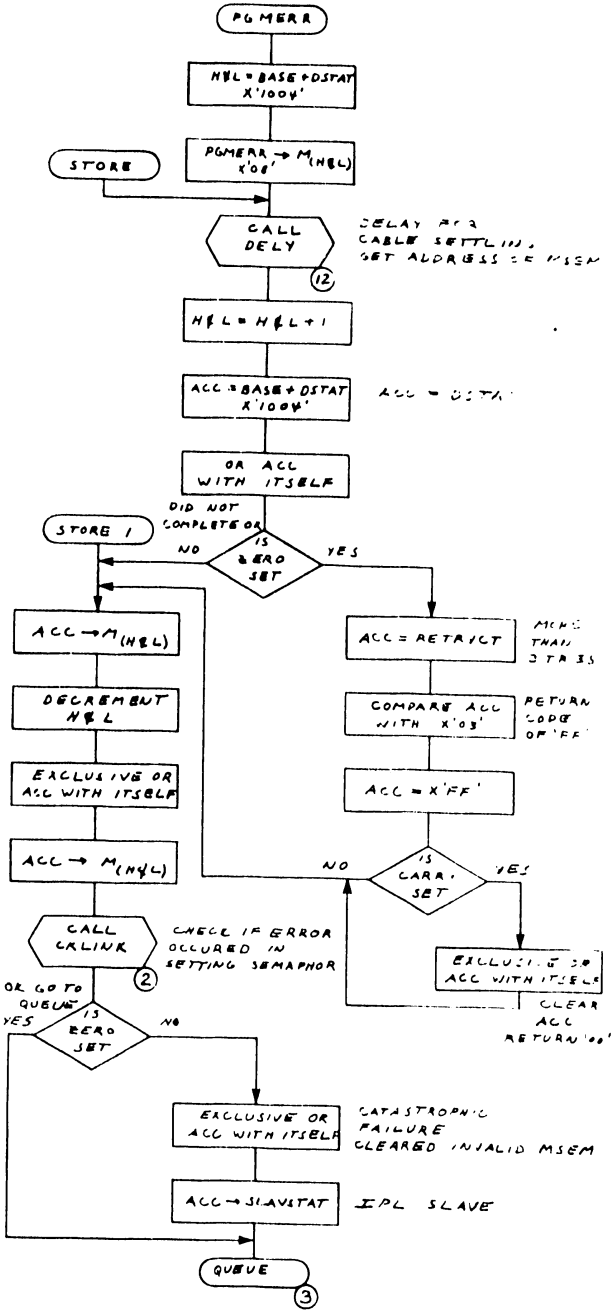

A CONT.
MOV M(H&L) → ACC
SAVE OLD ADDRESS
MOV ACC → C
OR X'F0' WITH ACC
MOV ACC → L
TRANSLATE ADDRESS, ADD TO GET TRANSLATED ADDRESS
MOV M(H&L) → A
ACC = ACC + C
SELECT ACTIVE DISK
OUT ØI SELECTS (ACTIVE DISK)
(H&L) = ACTIVE X'1018'
COMPARE ACC WITH M(H&L)
YES
IS ACC=C
SAME DEV.
7
SAVE ACTIVE DEVICE IN ACTIVE
MOV ACC → M(H&L)
SWAP TRACK WITH SAVED TRACK
(H&L) = SVDTRK X'101E'
(D&E) = TRACK X'1019'
B=SAVE TRACK
MOV M(H&L) → B
A=TRACK
ACC = M(D&E)
MOV ACC → M(H&L)
MOV B → ACC
ACC → M(D&E)
PUT HEAD DOWN
HDDN
7
FORMAT 1
CALL SUBR SETUP
11
ANY MORE SECTORS TO FORMAT
DCR C
C=C-1
NO
IS ACC = 0
YES
NO MORE
10
STOP ALL INTERRUPTS BEGINNING TIME CRIT LOOP
DISABLE INTERRUPTS
STATF
IN Ø (DISK STATUS)
OR ACC WITH ITSELF
DMA COMPLETE?
NO
IS ACC POSITIVE
YES
STATUS MASK
AND ACC WITH X'33'
YES
IS ACC = 0
NO
DISK ERROR
FAIL
9
OUT ØD (FORMAT)
ENABLE INTERRUPTS

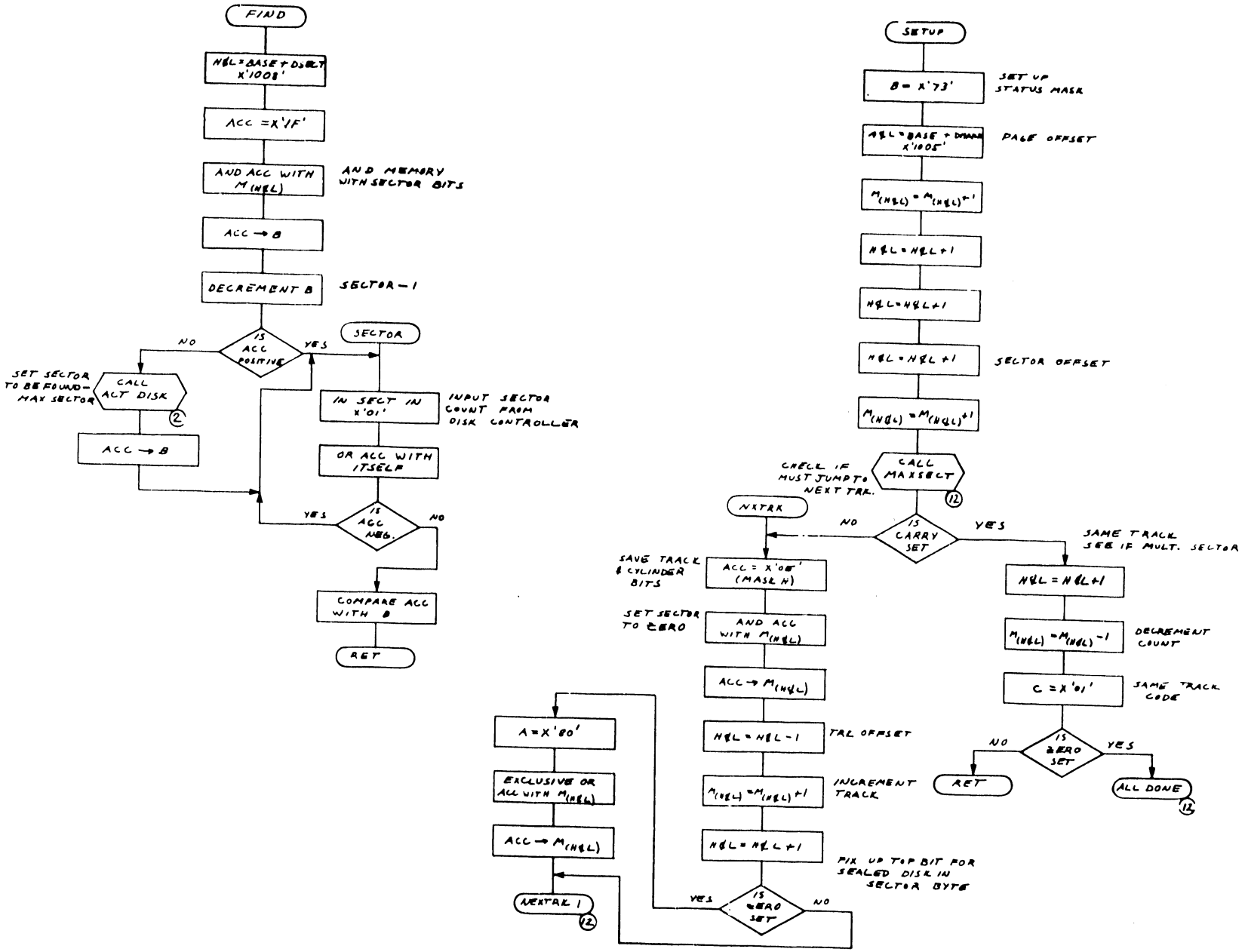

SAMEDEV
ACC=MODE X'101C'
CHECK IF IDLE
COMPARE ACC WITH IDLE UP X'00'
PUT HEAD DOWN IF IDLE UP & FLOPPY
NODN
IS ZERO SET
YES
NO
NOHDDN
CALL ACT DISK
2
FLOPPY?
IS CARRY SET
YES
NO
ACC = HD TICK X'05'
ACC → DELAY X'1018'
HEAD DOWN IN '03'
STORE DELAY CONSTANT FOR HEAD DOWN
CALL ACT DISK
2
H&L = BASE + DTADR X'C07'
TRACK OFFSET TO H&L
DEE = TRACK X'1019'
ACC = M(DEE) (TRACK)
ACC → B (D TRACK)
OLD TRACK TO B
ACC = M(H&L)
NEW TRACK IN ACC.
IS CARRY SET
YES
NO
SEALED 1
DON'T NEED TO CHECK VALID TRACK FOR SEALED DISK
IS NEW TRACK VALID
COMPARE ACC WITH MAXTRK+1 X'4D'
IS CARRY SET
NO
YES
ACC → M(DEE)
OUT TRACK
PGMEAR
10
ACC = ACC - B
CALCULATE STEPS
DEE = STEPS X'101A'
ACC → M(DEE) (STEPS)
ACC = B
OR ACC WITH ITSELF
RESTORE?
NO REST
IS ACC POSITIVE
YES
NO
RESTORE!
ACC → M(DEE) (STEPS)
INX H&L
SECTOR OFFSET IN H&L
CALL MAX SECT
12
IS CARRY SET
NO
YES
ACC = M(H&L)
OUTPUT SECTOR TO DISK CONTROLLER
OUT SECTOR X'08'
PUT NEW TRACK INTO TRACK
OUTPUT TRACK TO DISK CONTROLLER
H&L = BASE + MSEM X'1003'
ACC = X'83'
COMPARE ACC WITH M(H&L) X'1002'
CHECK IF DOING FORMAT
IS LEAD SET
YES
NO
FMT
8
ACC = BASE + DSCONT X'1009'
OR ACC WITH ITSELF
CHECK IF NONZERO COUNT
IS ZERO SET
YES
NO
ACC = X'81'
COMPARE ACC WITH M(H&L)
IS ZERO SET
NO
YES
CKSTAT
8
WRITE LS
8

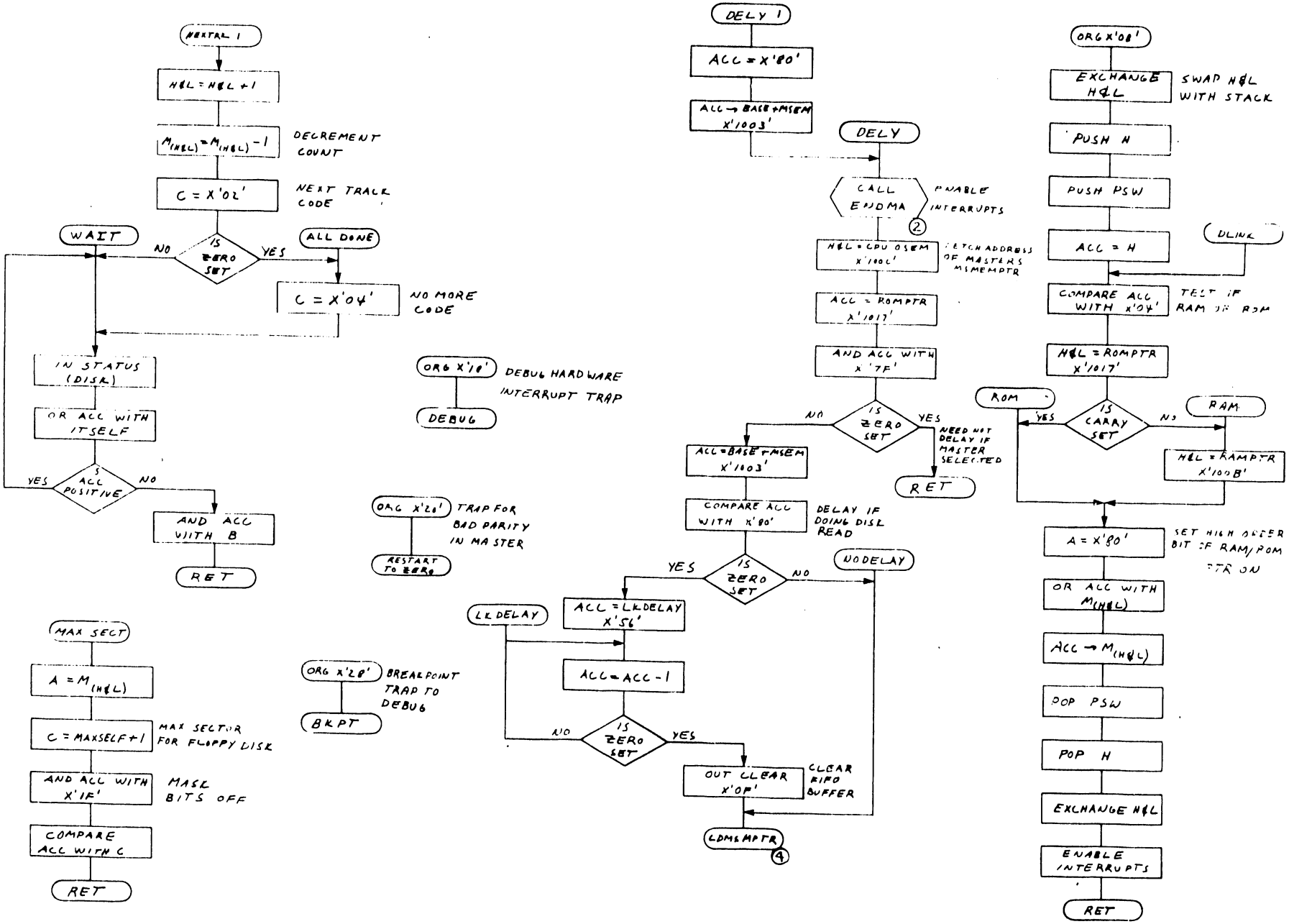

CRSTAT
IN STATUS
AND ACC WITH X'10' (ST PWR)
CHECK IF DISK OK
IS ZERO SET
NO
YES
CALL ALT DISK
2
MODE MOV
IS FLOPPY?
NO
IS CARRY SET
YES
OUT SEEK
ACC = MOVING X'02'
CHANGE MODE TO MOVING AND EXIT
ST MODE
3
FMT
HL = BASE + DTRACK
ACC = M(HL) X'1007'
OR ACC WITH ITSELF
WRITE LS
IS ZERO SET
NO
YES
ACC = X'80' X'101A'
FORCE ALL THE WAY BACK TO TRACK ZERO
ACC → STEPS
IN STATUS
AND ACC WITH X'08' (STWRT)
BADDISK
IS ZERO SET
YES
NO
OPERATOR INTERVENTION REQUIRED TO STATUS
HL = BASE + DSTAT X'100A'
M(HL) = M(HL) + 1
SAVE DISK STATUS
ACC → C
AND ACC WITH X'10' (STPWR)
IS ZERO SET
NO
YES
STORE STATUS
CLEAR MSEM
ACC = C
RESTORE STATUS
COMPARE ACC WITH X'08' (STWRT)
WRIT PROT
IS ZERO SET
YES
NO
SERVICE REQUIRED
M(HL) = M(HL) + 1
M(HL) = M(HL) + 1
PROTECTED DISK
STORE
10


FAIL
ENABLE INTERRUPTS
ALLOW INTERRUPTS TO BE TAKEN
ACC → C
SAVE DISK STATUS
H&L = RETRY CT
B = M(H&L)
SAVE RETRY CT
M(H&L) = M(H&L)+1
INCREMENT RETRY CT
CALL DELAY 12
DELAY FOR CABLE SETTING
ACC = B
OR ACC WITH ITSELF
RETRY 1
IF RETRY #1 DO NOT RESTORE
IS ZERO SET
YES
NO
GREATER THAN MAX ALLOWED TRIES?
COMPARE ACC WITH MAXTRY X'0F'
ACC = C
RESTORE DISK STATUS TO ACC
IS CARRY SET
YES
NO
BADDISK 8
CALL ACT DISK 2
FLOPPY SEALED
RETRY
IS CARRY SET
YES
NO
OUT-RESTOR
CALL WAIT 12
ACC = X'80'
RETURN TO TRACK ZERO
ACC → TRACK X'0019'
DISKOP 1 4
REDO DISK OPERATION
READ
CALL FIND 11
FIND SECTOR-1
READ 0
IS ZERO SET
YES
NO
OUT READ X'0B'
CALL ACT DISK 2
READ 1
FLOPPY-WAIT FOR NEXT TIMER INTERRUPT
IS CARRY SET
YES
NO
SEALED DISK WAIT
ENDIT 3
ALLOW INTERRUPTS TO BE PROCESSED
CALL ENDMA 2
LOOK AHEAD FOR CONTINUOUS READS
CALL SETUP 11
ANY MORE INTERRUPTS
DECREMENT C
IS ZERO SET
NO
YES
NO MORE 10
DISABLE INTERRUPTS
DISABLE INTERRUPTS BEGIN TIME CRIT LOOP
STATR
IN STATUS (DISK) X'00'
OR ACC WITH ITSELF
IS ACC POSITIVE
YES
NO
CONTAINS MASK FOR DISK STATUS
AND ACC WITH B
IS ZERO SET
NO
YES
END OF CRITICAL TIME LOOP
OUT READ X'0B'


WRITE
FIND SECTOR-1
CALL FIND
11
IS ZERO SET
NO
YES
CALL ACT DISK
2
IS CARRY SET
NO
YES
FLOPPY
SEALED DISK LOOK FOR MORE
ENDIT
3
WRITE 0
OUT WRITE X'0C'
WRITE 1
CALL ENDMA
2
ALLOW INTERRUPTS TO BE PROCESSED
CALL SETUP
11
LOOK AHEAD FOR CONTIGUOUS WRITES
DCR C
ANY MORE WRITES
NO MORE
IS ZERO SET
YES
NO
DISABLE INTERRUPTS
BEGIN CRITICAL TIME LOOP
OR ACC WITH ITSELF
STATUS IN ACC
STATW
IN STATUS (C SK) X'00'
OR ACC WITH ITSELF
IS DMA COMPLETE
IS ACC POSITIVE
YES
NO
B CONTAINS MASK FOR DISK STATUS
AND ACC WITH B
IS ZERO SET
NO
YES
FAIL
9
OUT WRITE X'0C'
END OF CRITICAL TIME LOOP
IS ZERO SET
NO
YES
FAIL
4
DISK ERROR ON LAST READ
DECREMENT C
ANY MORE OPERATIONS ON NEXT TRACK
NO MORE OPERATIONS
NO
YES
STORE
OTHERWISE DELAY FOR CABLE SETTLING
CALL DELY
DO OPERATIONS ON NEXT TRACK
NOHDDN
7


PGMERR
H&L = BASE + DSTAT X'100H'
PGMERR → M(H&L) X'08'
STORE
CALL DELY
12
DELAY FOR CABLE SETTLING, SET ADDRESS OF MSEM
H&L = H&L + 1
ACC = BASE + DSTAT X'100H'
ACC = DSTA
OR ACC WITH ITSELF
DID NOT COMPLETE OR
STORE 1
IS ZERO SET
NO
YES
ACC → M(H&L)
DECREMENT H&L
EXCLUSIVE OR ACC WITH ITSELF
ACC → M(H&L)
CALL CALINK
2
CHECK IF ERROR OCCURED IN SETTING SEMAPHOR
OR GO TO QUEUE
IS ZERO SET
YES
NO
ACC = RETRYCT
MORE THAN 3 TRIES
COMPARE ACC WITH X'03'
RETURN CODE OF 'FF'
ACC = X'FF'
IS CARR SET
NO
YES
EXCLUSIVE OR ACC WITH ITSELF
CLEAR ACC RETURN '00'
EXCLUSIVE OR ACC WITH ITSELF
CATASTROPHIC FAILURE CLEARED INVALID MSEM
ACC → SLAVSTAT
IPL SLAVE
QUEUE
3


FIND
H&L=BASE+DISKT X'1008'
ACC=X'1F'
AND ACC WITH M(H&L)
AND MEMORY WITH SECTOR BITS
ACC→B
DECREMENT B
SECTOR-1
IS ACC POSITIVE
NO
YES
SECTOR
SET SECTOR TO BE FOUND-MAX SECTOR
CALL ACT DISK
2
ACC→B
IN SECT IN X'01'
INPUT SECTOR COUNT FROM DISK CONTROLLER
OR ACC WITH ITSELF
IS ACC NEG.
YES
NO
COMPARE ACC WITH B
RET
SETUP
B=X'73'
SET UP STATUS MASK
H&L=BASE+DISKA X'1005'
PAGE OFFSET
M(H&L)=M(H&L)+1
H&L=H&L+1
H&L=H&L+1
H&L=H&L+1
SECTOR OFFSET
M(H&L)=M(H&L)+1
CHECK IF MUST JUMP TO NEXT TRK.
CALL MAXSECT
12
NXTRK
NO
IS CARRY SET
YES
SAME TRACK SEE IF MULT. SECTOR
SAVE TRACK & CYLINDER BITS
ACC=X'0E' (MASK N)
SET SECTOR TO ZERO
AND ACC WITH M(H&L)
ACC→M(H&L)
H&L=H&L-1
TRK OFFSET
M(H&L)=M(H&L)+1
INCREMENT TRACK
H&L=H&L+1
FIX UP TOP BIT FOR SEALED DISK IN SECTOR BYTE
IS ZERO SET
YES
NO
A=X'80'
EXCLUSIVE OR ACC WITH M(H&L)
ACC→M(H&L)
NXTRK 1
12
H&L=H&L+1
M(H&L)=M(H&L)-1
DECREMENT COUNT
C=X'01'
SAME TRACK CODE
IS ZERO SET
NO
YES
RET
ALL DONE
12


NEXTAL 1
H&L = H&L + 1
M(H&L) = M(H&L) - 1
DECREMENT COUNT
C = X'02'
NEXT TRACK CODE
WAIT
NO
IS ZERO SET
YES
ALL DONE
C = X'04'
NO MORE CODE
IN STATUS (DISK)
OR ACC WITH ITSELF
YES
ACC POSITIVE
NO
AND ACC WITH B
RET
ORG X'10'
DEBUG HARDWARE INTERRUPT TRAP
DEBUG
ORG X'20'
TRAP FOR BAD PARITY IN MASTER
RESTART TO ZERO
MAX SECT
A = M(H&L)
C = MAXSELF+1
MAX SECTOR FOR FLOPPY DISK
AND ACC WITH X'1F'
MASK BITS OFF
COMPARE ACC WITH C
RET
ORG X'28'
BREAKPOINT TRAP TO DEBUG
BKPT
DELY 1
ACC = X'80'
ACC → BASE+MSEM X'1003'
DELY
CALL ENDMA
ENABLE INTERRUPTS
2
H&L = CPU OSEM X'100C'
FETCH ADDRESS OF MASTERS MSMEMPTR
ACC = ROMPTR X'1017'
AND ACC WITH X'7F'
NO
IS ZERO SET
YES
NEED NOT DELAY IF MASTER SELECTED
RET
ACC = BASE+MSEM X'1003'
COMPARE ACC WITH X'80'
DELAY IF DOING DISK READ
YES
IS ZERO SET
NO
NODELAY
LKDELAY
ACC = LKDELAY X'56'
ACC = ACC - 1
NO
IS ZERO SET
YES
OUT CLEAR X'0F'
CLEAR FIFO BUFFER
LDMSMPTR
4
ORG X'08'
EXCHANGE H&L
SWAP H&L WITH STACK
PUSH H
PUSH PSW
ACC = H
DLINK
COMPARE ACC WITH X'04'
TEST IF RAM OR ROM
H&L = ROMPTR X'1017'
ROM
YES
IS CARRY SET
NO
RAM
H&L = RAMPTR X'100B'
A = X'80'
SET HIGH ORDER BIT OF RAM/ROM PTR ON
OR ACC WITH M(H&L)
ACC → M(H&L)
POP PSW
POP H
EXCHANGE H&L
ENABLE INTERRUPTS
RET

END