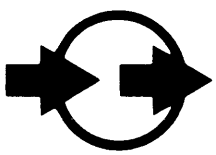
TC-30 STREAMER TAPE ADAPTER

HARDWARE MANUAL



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HARDWARE MANUAL

Preliminary

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P91000943 September, 1983 Supplement: 2

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PREFACE

This hardware manual provides information necessary for the installation and operation of the Western Peripherals Model TC-30 Streamer Drive Tape Adapter, used with the DEC PDP-11 family of computer systems.

The manual is divided into the following sections:

Section I	General Description
Section II	Installation
Section III	Programming
Section IV	Tape Interface
Section V	Tape Format
Section VI	Computer Interface
Appendix A	Signal Glossary

RELATED DOCUMENTS

P91000950	Western Peripherals TC-30 Tape Adapter Logic Manual
P91000448	Western Peripherals DEC-Compatible Tape Diagnostic Manual
ANSI X30.39-1973	Recorded Magnetic Tape for Information Interchange (1600 CPI, Phase Encoded)
ANSI X3.40-1973	Unrecorded Magnetic Tape for Information Interchange (9-track 200 and 800 CPI, NRZI; and 1600 CPI, PE}

SECTION I

GENERAL DESCRIPTION

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SECTION I - GENERAL DESCRIPTION

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SECTION I

GENERAL DESCRIPTION

INTRODUCTION

The Western Peripherals Model TC-30 is a streamer drive tape adapter which is compatible with the DEC PDP-11 family of computer systems. Contained on a single standard-sized quad-wide printed circuit board, the tape adapter provides the interface for a tape system of up to eight industry-compatible formatted streamer tape drives, using the phase encoded or NRZI tape recording format.

EMULATION - SOFTWARE COMPATIBILITY

The tape adapter is compatible with DEC PDP-11 operating systems supporting the TM-11/TU-10 tape subsystem. The standard TM-11 register addresses and vector are used, with various alternates available via jumper selection.

The tape adapter operates in two modes (depending on tape drive capability); both the streaming and start-stop modes are supported. In the start-stop mode, the tape subsystem is software compatible with operating systems that can handle the standard DEC TM-11 tape subsystem. In the tape streaming mode, the tape adapter uses the same standard TM-11 registers to simplify the system interface. However, additional software considerations are required for the high throughput of the streaming mode.

HARDWARE COMPATIBILITY

The Model TC-30 Magnetic Tape Adapter interfaces the DEC PDP-11 system via the processor Unibus. The tape adapter mounts inside the cabinet of the host PDP-11 computer and plugs directly into an available slot in its Unibus.

TAPE UNIT INTERFACE

Standard "A" and "B" formatter interface cables are used to connect the tape drives to the tape adapter through the two connectors on the top edge of the tape adapter board. Mixed drives are supported by the tape adapter, including streaming, non-streaming, and dual-mode drives operating in the PE and/or

NRZI format. Contact our Marketing department for a list of drives which are compatible with the TC-30 Tape Adapter.

DATA BUFFERING

The tape adapter has a 64 character buffer to allow greater flexibility in assigning priorities on the bus without encountering bus grant late errors.

TAPE FORMATS

The tape adapter uses the standard nine track 1600 bit per inch (bpi) phase encoded and 800 bpi NRZI tape formats. In PE, each tape block contains a 41 character preamble of 40 tape characters with all-zero bits followed by one character of all-one bits. The preamble is followed by the data field which also contains an odd parity bit for each data character. Following the data field is the postamble, which is the mirror-image of the preamble.

Like PE, the data field of the NRZI format contains an odd parity bit for each data character. Following the data field are the Cyclic Redundancy Check (CRC) and Longitudinal Redundancy Check (LRC) characters to ensure data integrity.

DATA BLOCK SIZE

The maximum data block size is only limited by the Byte/Record Counter to a full 64K byte block. The minimum recommended data block size can vary from system to system where the generated tapes will be used.

SPECIFICATIONS

COMPUTER INTERFACE - SOFTWARE

PDP-11 Interface Protocol - DEC TM-11/TU-10 (Modified):
Unibus Register Addressing Assignments -
Standard = 772520-772532 (octal)
Optional= 772020-772760 (status register, in modulo 40 increments, via option jumpers).
Unibus Interrupt Vector - Standard = 224 (octal)
Optional = 0 - 377 (via option jumpers).
PDP-11 Bus Level - Bus level 4, 5, 6, or 7;
(level 5 is standard).

COMPUTER INTERFACE - HARDWARE

Unibus (fits in a standard SPC Unibus slot).
Bus Loading - One standard Unibus load.
Data Buffer - 64 bytes, Read and Write.
DMA Addressing - up to 22 bits.
DMA Uni-bus Transfer Time (bus efficiency) - 1 us/word Read and Write (T BSY time).
DMA Transfer Rate - 640 Kbytes/sec. (maximum)

TAPE DRIVE INTERFACE

Formatted Tape Drive Protocol -
Industry Standard (Pertec) for formatted drive.
Streaming and non-streaming up to eight drives.
Tape Interface Cabling - Two 50 conductor 3M-type ribbon cables with edge connectors on both ends.

SIZE One Standard PDP-11 Quad PC Board

POWER +5 volts @ 2.5 amps power consumption (estimated).
-15 volts @ 60 ma power consumption (estimated).

ENVIRONMENT

Operating temperature	0 to 55 degrees centigrade
Storage temperature	10 to 70 degrees centigrade
Relative humidity	10% to 90% (without condensation)

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SECTION II

INSTALLATION

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SECTION II - INSTALLATION

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SECTION II

INSTALLATION

INTRODUCTION

This section provides the necessary information to successfully set the options and to install the TC-30 Tape Adapter into the DEC PDP-11 computer system. The tape adapter consists of one standard-sized quad-wide printed circuit board which plugs into a standard backplane in the computer mainframe or expansion chassis. One cable set (two cables) is provided for each drive. A diagnostic tape and a complete set of documentation is included with each tape adapter.

These installation instructions are for the standard tape adapter assembly number 60001286 (documented by schematic 75001107). If your board has a different part number, contact Western Peripherals for information concerning the proper installation of your tape adapter board.

UNPACKING AND INSPECTION

After removal of the tape adapter components from the shipping container, visually inspect them for physical damage. Check off each item on the enclosed packing list. In case of damage, retain all packaging material and notify the carrier to make a report. Be sure all minor parts and small items are found before discarding any shipping material.

PREPARATION

Locate the position in the computer where the tape adapter will be installed. Remember that the location in the system determines the bus priority. The tape adapter should work well if placed anywhere in the bus. You may want to adjust the position of the devices on the bus to take advantage of the priority structure of the bus to reduce bus grant late errors in the various devices in the system.

Refer to the tape drive manual to install the tape drives. The tape drives must be prepared and the processor checked-out before the tape adapter can be expected to operate properly.

ADDRESS SELECTION

The tape adapter is normally shipped with addresses 772520 - 772534 selected. In systems where the standard address group is already in use, an alternate address group may be selected for the tape adapter in the range from 772020 to 772760 by setting the address jumper configuration according to the following table. Check these jumpers to ensure the desired address range is selected. These jumpers are found at location 13F on the board, and are illustrated on schematic page 3 in the logic manual.

DESIRED REGISTER ADDRESSES	ADDRESS JUMPERS (E#)							
	49-50	48-49	51-52	52-53	55-56	54-55	45-46	46-47
772020 - 772034	OUT	IN	OUT	IN	OUT	IN	OUT	IN
772060 - 772074	OUT	IN	OUT	IN	OUT	IN	IN	OUT
772120 - 772134	OUT	IN	OUT	IN	IN	OUT	OUT	IN
772160 - 772174	OUT	IN	OUT	IN	IN	OUT	IN	OUT
772220 - 772234	OUT	IN	IN	OUT	OUT	IN	OUT	IN
772260 - 772274	OUT	IN	IN	OUT	OUT	IN	IN	OUT
772320 - 772334	OUT	IN	IN	OUT	IN	OUT	OUT	IN
772360 - 772374	OUT	IN	IN	OUT	IN	OUT	IN	OUT
772420 - 772434	IN	OUT	OUT	IN	OUT	IN	OUT	IN
772460 - 772474	IN	OUT	OUT	IN	OUT	IN	IN	OUT
772520 - 772534 *	IN	OUT	OUT	IN	IN	OUT	OUT	IN
772560 - 772574	IN	OUT	OUT	IN	IN	OUT	IN	OUT
772620 - 772634	IN	OUT	IN	OUT	OUT	IN	OUT	IN
772660 - 772674	IN	OUT	IN	OUT	OUT	IN	IN	OUT
772720 - 772734	IN	OUT	IN	OUT	IN	OUT	OUT	IN
772760 - 772774	IN	OUT	IN	OUT	IN	OUT	IN	OUT

* Standard Configuration

VECTOR SELECTION

The tape adapter is normally shipped with standard vector 224 selected. In systems where the standard vector is already in use, an alternate vector may be selected for the tape adapter in the range from 0 to 377 by setting the address jumper configuration according to the following table. These jumpers are located on the board between ICs 18F - 21F, and are illustrated on schematic page 7 in the logic manual.

VECTOR BIT NUMBER	FOR A ZERO BIT, CONNECT:	FOR A ONE BIT, CONNECT:	TO:
0 LSB	E77 *	E79	E78
1	E80 *	E82	E81
2	E83	E85 *	E84
3	E86 *	E88	E87
4	E65	E67 *	E66
5	E68 *	E70	E69
6	E71 *	E73	E72
7	E74	E76 *	E75

ALL UNSPECIFIED JUMPERS MUST BE REMOVED OR CUT.
STANDARD JUMPERS (*) ARE PROVIDED IN ETCH.

STANDARD VECTOR CONFIGURATION

In the standard vector configuration, bits 2, 4, and 7 are set to ones while the remaining bits are all set to zeros, as illustrated below.

STANDARD VECTOR:	2			2			4		
BINARY BIT CONFIGURATION:	-	1	0	0	1	0	1	0	0
BIT NUMBER:	-	7	6	5	4	3	2	1	0

The proper jumper settings for this Vector 224 configuration are E77-E78, E80-E81, E85-E84, E86-E87, E67-E66, E68-E69, E71-E72, and E76-E75. All these jumpers are provided in etch.

BUS LEVEL SELECTION

The tape adapter is normally shipped with bus level 5 set in etched jumpers. In systems where another bus level is to be used, bus level 4, 6, or 7 may be specified for the tape adapter by rearranging the bus level jumper configuration according to the following table. These jumpers are found on the board at IC locations 12H and 13H and are illustrated on schematic page 2 in the logic manual.

BUS LEVEL				JUMPER CONNECTION
4	5 *	6	7	
IN	OUT	OUT	OUT	13H 4-13
OUT	IN	OUT	OUT	13H 3-14
OUT	OUT	IN	OUT	13H 2-15
OUT	OUT	OUT	IN	13H 1-16
IN	IN	IN	OUT	12H 1-16
IN	IN	OUT	IN	12H 2-15
IN	OUT	IN	IN	12H 3-14
OUT	IN	IN	IN	12H 4-13
OUT	OUT	OUT	IN	13H 5-12
OUT	OUT	IN	OUT	13H 11-6
OUT	IN	OUT	OUT	13H 7-10
IN	OUT	OUT	OUT	13H 8-9
OUT	OUT	OUT	IN	12H 8-9
OUT	OUT	IN	OUT	12H 7-10
OUT	IN	OUT	OUT	12H 6-11
IN	OUT	OUT	OUT	12H 5-12

* - STANDARD JUMPERS ARE PROVIDED IN ETCH.

MISCELLANEOUS OPTIONS

Some miscellaneous functions have been provided to allow additional flexibility. The tape adapter may be used with formatters which do or do not store end-of-tape status and those formatters with only start-stop operation as well as those with full streaming capability.

You can choose to do byte-swapping for standard IBM tapes in the controller rather than in your software. This mode is software selectable through bit 10 of either the MTC or the MTRD register.

Expanded addressing (22-bit) options are available (if your machine has that capability). One option enables or disables 22-bit bus addressing input and the other enables or disables the extended address output.

The following table lists these miscellaneous functions and options which may be selected by jumpers. The jumpers to install and remove are listed as well as their physical board location. Standard jumpers are generally etched onto the back of the board. The page number listed in the last column is where you'll find the schamatic illustration of the jumper in the logic manual.

FUNCTION	INSTALL JUMPER	REMOVE JUMPER	LOC-PAGE
TAPE ADAPTER STORES EOT (STANDARD)	E32-E33	E31-E32	20E
FORMATTER STORES EOT (OPTIONAL)	E31-E32	E32-E33	8
FORMATTERS WITH STREAMING CAPABILITY (STANDARD)	E7-E8	E8-E9	4H
FORMATTERS WITH START-STOP CAPABILITY ONLY (OPTIONAL)	E8-E9	E7-E8	14
IBM PACKING MODE CONTROLLED BY BIT 10 OF TU-10 REGISTER (STANDARD)	E29-E30	E28-E29	12D
IBM PACKING MODE CONTROLLED BY BIT 10 OF COMMAND REGISTER (OPTIONAL)	E28-E29	E30-E29	15
22-BIT ADDRESSING OUTPUT (ENABLED-STANDARD)	E19-E20	E18-E19	9H
22-BIT ADDRESSING OUTPUT (DISABLED-OPTIONAL)	E18-E19	E19-E20	2
22-BIT ADDRESSING INPUT (DISABLED-STANDARD)	E12-E13	E11-E12	13D
22-BIT ADDRESSING INPUT (ENABLED-OPTIONAL)	E11-E12	E12-E13	3

FORMATTER INTERFACE CONFIGURATION

Drives may be used in the system with varying interface configurations. Specify the features of the interface for each tape drive by setting the configuration jumpers on the tape adapter board according to the following table. It lists the interface control options for the extended gap and streaming modes. The jumpers to install and remove are listed as well as their physical board location.

Some of the standard jumpers are etched onto the back of the board. Others are only implemented by adding jumpers. In any case, each jumper should be checked to ensure the board contains proper configuration. The page number listed in the last column is where you'll find the schamatic illustration of the jumper in the logic manual.

FUNCTION	INSTALL JUMPER	REMOVE JUMPER	LOC-PAGE
COMMAND REGISTER BIT 13 (DEN 5) CONTROLS 1.2 INCH GAP FUNCTION (STD)	E63-E64	E62-E63	9A
COMMAND REGISTER BIT 13 (DEN 5) CONTROL FUNCTION DISABLED (OPTIONAL)	E62-E63	E63-E64	6
COMMAND REGISTER BIT 14 (DEN 8) CONTROLS STREAMING FUNCTION (STD)	E59-E60	E58-E59	9A
COMMAND REGISTER BIT 14 (DEN 8) CONTROL FUNCTION DISABLED (OPTIONAL)	E58-E59	E59-E60	6

TAPE ADAPTER INSTALLATION

Place the tape adapter board into the selected card slot in the backplane, assuring that it seats properly and makes a good connection.

The DMA Non-Processor Grant and the Bus Grant lines are daisy-chained from one backplane connector to the next. To maintain continuity, unused backplane connector slots are usually jumpered with a jumper card and a jumper wire.

The Bus Grant jumper card is installed in unused "D" connectors. Western Peripherals supplies part number P01310093 for this purpose. The DMA Non-Processor Grant jumper is connected between pins A1 and B1 on the backside of any unused "C" connectors.

Any open slots between the tape adapter and the processor must have these jumpers installed. Be sure to check for and remove the DMA Non-Processor Grant jumper wire at the tape adapter's backplane connector. Also, be sure the computer's Uni-Bus is properly terminated.

INTERCONNECTIONS

The tape drive's formatter is connected to the tape adapter via two connectors located on the top edge of the tape adapter board. Both of the connectors are 50-pin flat ribbon cable connectors which provide paths for select, control, status and data between the tape adapter and the formatter. Typically, one formatter can control up to four tape drives. Some formatters have a daisy-chain connection to add another formatter in a daisy-chain fashion to the first unit. Western Peripherals provides a special cable with double connectors for formatters without daisy-chain connectors.

CHECKOUT

With your tape subsystem installed, you can now run the test programs contained in the diagnostic tape supplied with your tape adapter.

JUMPER REFERENCE LIST

This list summarizes the various option jumpers, their locations, and their schematic reference pages.

JUMPER NUMBER	JUMPER FUNCTION	BOARD LOCATION	SCHEMATIC PAGE
E58-E60	1.2 INCH GAP CONTROL	9A	6
E62-E64	STREAMING CONTROL	9A	6
E7-E9	STREAMING FEATURE	20H	14
E45-E56	ADDRESS SELECT	13F	3
E11-E13	22 BIT ADDRESSING OPTION	13D	3
E28-E30	IBM MODE CONTROL	12D	15
E31-E33	EOT STORAGE OPTION	20E	8
E65-E88	VECTOR SELECT	18F-21F	7
E18-E20	22 BIT ADDRESSING OPTION	9H	2

SECTION III

PROGRAMMING

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SECTION III - PROGRAMMING

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SECTION III

PROGRAMMING

INTRODUCTION

This section contains machine-level programming reference information which describes the registers of the tape adapter. Also contained in this section is information on the operation of the tape adapter including addressing, register transfers, data transfers, and interrupts.

PROGRAMMED I/O INSTRUCTIONS

Programmed I/O instructions are used to specify the starting address in computer memory, the byte count, and the command function to be performed. Programmed I/O instructions are also used to transfer status and address information from the tape adapter to the computer. The registers are summarized in the following paragraph.

REGISTER SUMMARY

The following table summarizes the registers of the tape adapter.

REGISTER	DESIGNATION	FUNCTION	STANDARD ADDRESS
Status	MTS	READ	772520
Command	MTC	W/R	772522
Byte/Record Counter	MTBRC	W/R	772524
Current Memory Address	MTCMA	W/R	772526
Data Buffer	MTD	READ	772530
TU-10 Drive	MTRD	W/R	772532
Extended Memory Address	--	W/R	772534

REGISTER ADDRESSING

The registers of the tape adapter occupy bus address locations 772520 through 772534 and are addressed by the CPU with the tape adapter being the slave device. These addresses are placed on the bus in the same way that memory is addressed. The tape adapter latches the address until the completion of the transfer.

TAPE ADAPTER REGISTER DESCRIPTIONS

STATUS REGISTER (MTS) 772520

The status register contains only read bits, providing the CPU with status indications from both the tape drive and the tape adapter.

REGISTER BIT ASSIGNMENTS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ILL COM	EOF	---	PAR ERR	B/G LT	EOT	R/L ERR	---	NXM ERR	SEL REM	BOT	---	SLO DWN	WRT LOK	RWS	T/U RDY

MTS BIT 15 ILLEGAL COMMAND - When and illegal command is received, the CU RDY bit remains true, and the command is disregarded. The Illegal Command bit is set for any of the following conditions and sets the Error Summary Bit in the Command Register:

a. Any tape command initiated during a tape operation (CU RDY bit is false).

b. Any tape command where the selected drive is not on-line (Select Remote bit is false).

c. Any write command on a drive which is file protected.

MTS BIT 14 END OF FILE - The EOF bit is set when a file mark character is detected during a Read, Space Forward or Space Reverse operation. The EOF bit sets the Error Summary bit in the Command Register.

MTS BIT 13 (NOT USED) - Always equals zero.

MTS BIT 12 PARITY ERROR - The Parity Error bit is set when the tape adapter detects a parity error, or Postamble error during a Read, Write, or Write with Extended Record Gap operation. The Parity Error bit does not affect the transfer of data. During a Write operation, the entire record will be transferred onto tape or in a Read operation, the entire record will be transferred to memory. The Parity Error bit will set the Error Summary bit in the Command Register.

MTS BIT 11 BUS GRANT LATE - The Bus Grant Late bit is set when the maximum internal buffering capacity (full in Read; empty in Write) is exceeded and information is lost during an operation. This condition causes an immediate termination of the Read or Write operation in progress. This bit will also be set during a Read operation when the internal buffer of the tape adapter is

not emptied before the tape begins to stop. The Error Summary bit in the Command Register will be set when the BGL bit is true.

MTS BIT 10 END OF TAPE - The End of Tape bit is set when the EOT marker is encountered while the tape is moving in the forward direction. The bit will be reset when the EOT marker is passed while perfprming a Rewind or Space Reverse operation. The Error Summary bit in the Command register will be set when the EOT bit is true.

MTS BIT 9 RECORD LENGTH ERROR - The Record Length Error bit will be set during a Read operation when the length of the record being read exceeds the memory allocation as indicated by the Byte/Record Counter. When the Byte/Record Counter indicates the end of the memory allocation, data transfer will stop and the tape adapter will continue to advance the tape to the next inter-record gap. A Record Length Error stops the incrementing of the Byte/Record Counter and the Current Memory Address Register and set the Error Summary bit in the Command Register.

MTS BIT 8 (NOT USED) - Always equals zero.

MTS BIT 7 NON-EXISTENT MEMORY ERROR - The Non-existent Memory bit is set during direct memory operations (when the tape adapter is bus master and is performing data transfers with the bus) and the tape adapter does not receive a Slave Sync response within 14 microseconds after it issues the Master Sync signal. When the Nonexistent Memory error bus time-out is detected, the Read or Write operation is terminated, stopping the tape in the inter-record gap, and setting the Error Summary bit in the Command Register.

MTS BIT 6 SELECT REMOTE - The Select Remote bit is set when the addressed tape drive is on-line and cleared when the addressed tape unit is off-line, powered off, or disconnected.

MTS BIT 5 BEGINNING OF TAPE - The Beginning of Tape bit is set when the tape drive detects the Load Point mark at the beginning of the magnetic tape.

MTS BIT 4 (NOT USED) - Always equals zero.

MTS BIT 3 SLOWING DOWN - The Tape Slowing Down (or Settle Down) bit is set whenever the tape unit is stopping after any motion command.

MTS BIT 2 WRITE LOCK - The Write Lock bit is set to prevent the software from attempting to write information on the tape when the operator has removed the write-enable ring from the supply reel on the tape drive.

MTS BIT 1 REWIND STATUS - The Rewind Status bit is set by the selected drive when it receives a Rewind command from the tape adapter or operator panel and is cleared by the selected drive when the tape arrives at BOT, completing the Rewind operation.

MTS BIT 0 TAPE UNIT READY - The Tape Unit Ready bit is set when the selected tape unit is stopped and is cleared when the tape adapter begins to execute a function command.

COMMAND REGISTER (MTC) 772522

REGISTER BIT ASSIGNMENTS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR SUM	DEN 8	DEN 5	PWR CLR	PAR EVN	DRV. SELECT			CTL UNT RDY	INT ENB	EXT ADD		FUNCTION			GO
					4	2	1			17	16	4	2	1	

MTC BIT 15 ERROR SUMMARY - Set as a function of bits 7-15 of the Status Register (MTS) being set. This bit is cleared as the result of an Initialize or a Go command to the tape unit.

MTC BITS 14, 13 DRIVE MODE SELECTION - These bits set the operating mode of the tape unit. In the streaming mode, the computer must supply commands quickly enough to avoid causing excessive repositioning operations in the drive. The extended gap mode provides extra time before repositioning will occur.

Den 8/Bit 14: 1 = Normal operation (12.5/25 ips)
0 = Streaming mode (100 ips)
Den 5/Bit 13: 1 = Normal gap (0.6")
0 = Extended gap (1.2")

MTC BIT 12 POWER CLEAR - This bit provides the means for the processor to clear the tape adapter and the tape drives without clearing other devices in the system. The Power Clear bit is always read back by the processor as a zero.

MTC BIT 11 LATERAL PARITY EVEN - This bit, when set, selects even lateral parity for diagnostic purposes. Otherwise, odd parity is generated and checked during all data transfer operations.

MTC BITS 10-8 DRIVE SELECT 4, 2, 1 - These bits specify one of the eight possible tape units. All operations defined in the MTC register and all status conditions defined in the MTS register refer to the unit indicated by these bits.

MTC BIT 7 CONTROL UNIT READY - This bit is cleared at the start of a tape operation and is set at the end of a tape operation to indicate that the tape adapter is ready to accept a new command.

MTC BIT 6 INTERRUPT ENABLE - When this bit is set, an interrupt occurs whenever either the Controller Ready bit or the Error Summary bit goes true or whenever a rewinding tape unit arrives at BOT. In addition, an interrupt occurs for an instruction that sets the INT ENB bit but does not set the GO bit.

MTC BITS 5, 4 EXTENDED ADDRESS 17, 16) - These bits access the two of the most significant bits of the Current Memory Address Register, providing bits 16 and 17 for the memory addressing capability.

MTC BITS 3 - 1 COMMAND FUNCTION BITS 4, 2, 1 - These bits select one of eight command functions:

FUNCTION BITS 4	2	1	FUNCTION
0	0	0	OFF LINE
0	0	1	READ
0	1	0	WRITE
0	1	1	WRITE EOF
1	0	0	SPACE FORWARD
1	0	1	SPACE REVERSE
1	1	0	WRITE W/ ERG
1	1	1	REWIND

a. OFF LINE COMMAND. This command which places the selected drive off-line, is usually preceded by a rewind command after completing all operations on the reel of tape. The tape adapter does not go Busy, leaving it free for use with other drives in the system.

b. READ COMMAND. The program must specify a byte count (in two's complement - or negative - form) and an initial address. The tape adapter reads a single record from tape and sends the data via DMA operations to the locations specified by the Address Register until the EOR gap is encountered or the Byte Counter overflows, whichever occurs first. For operations with variable length records, a large byte count ensures that the entire record will be read. The length of the record of unknown size can then be determined after it is read by comparing the Byte Counter at the end of the operation to its initial setting. The setting of Bus Grant Late status during the record indicates that information has been lost, but data transfers continue until the byte counter overflows or the EOR gap is detected.

c. WRITE COMMAND. The program must specify a (negative) byte count and an initial bus address. If Write Lock is true, GO sets Illegal Command, and the tape adapter rejects the operation. Otherwise, the tape adapter makes an immediate data request for the first word, and writes the data it receives from the locations specified by the address counter onto the magnetic tape until either the byte counter overflows or a Bus Grant Late or Non-Existent Memory error occurs, at which time the tape adapter terminates the record.

d. WRITE END OF FILE COMMAND. Unless Write Lock is set, GO starts the tape adapter into operation to write a file mark. With Write Lock true, the command is rejected.

e. SPACE FORWARD COMMAND. The program must specify a (negative) byte count equal to the number of records to be spaced. If BOT is true, GO sets the Illegal Status bit, and the tape adapter does not go into operation. Otherwise, the tape adapter spaces reverse over the given number of records, but it stops the tape automatically upon encountering a file mark or the Load Point. To space over a file, the program can simply specify a zero (maximum) byte count.

g. WRITE WITH EXTENDED RECORD GAP COMMAND. The operation of this command results in a three and one-half inch length of tape being erased before the data is written. This provides a method of erasing a bad record from a damaged portion of tape before rewriting the data farther down on the tape. A Space Reverse One Record operation generally precedes this command.

h. REWIND COMMAND. This command initiates a rewind operation in the addressed tape drive, which rewinds the tape onto the supply reel at high speed, and stops at BOT. the tape adapter does not go Busy, leaving it free for further use by the program during the rewind operation.

BYTE/RECORD COUNT REGISTER (MTBRC) 772524

REGISTER BIT ASSIGNMENTS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BYTE/RECORD COUNT															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

The MTBRC is a 16-bit binary counter which is used to count bytes of memory during Read or Write operations, or to count records in a Space Forward or Space Reverse operation. When used in a Write or Write with Extended Record Gap operation, the MTBRC is initially set by the program to the 2's complement of the number of bytes to be transferred from memory to tape. The MTBRC increments by one immediately after each byte memory access or by two after each word transfer. The MTBRC overflows to zero after the last byte of the record has been read from memory. Bus transfers are terminated by this byte count zero condition.

When the MTBRC is used in a Read operation, it is set to the 2's complement of a number equal to or greater than the maximum expected record length, indicating the memory allocation for the read data. A Record Length Error occurs when the actual record length is greater than the allocated memory, as indicated by the MTBRC overflowing before the EOR gap is detected.

When the MTBRC is used in a Space Forward or Space Reverse operation, it is set to the 2's complement of the number of

records to be spaced over. It is incremented by one each time a record passes the head whether the tape is moving in the forward or reverse direction.

CURRENT MEMORY ADDRESS REGISTER (MTCMA) 772526

REGISTER BIT ASSIGNMENTS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CURRENT MEMORY ADDRESS															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

The MTCMA register contains 16 of the 22 memory address counter bits which is used, in DMA operations, to provide the memory address for data transfers in Read Write and Write with Extended Record Gap operations. Prior to issuing a command, the memory address counter is set to the memory address to be used for the first data transfer. The memory address counter is incremented by one immediately after each byte transfer and by two after each word transfer. Thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address of the word following the final transfer for the record. After a Bus Grant Late or Non-Existent Memory error condition, the MTCMA contains the address of the location in which the failure occurred.

DATA BUFFER (MTD) 772530

REGISTER BIT ASSIGNMENTS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA BUFFER															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

The data buffer is a register which is used for diagnostic purposes. After the completion of an operation, the contents of the last data word transferred are placed into the data register and made available to the diagnostic program.

TU-10 READ LINES (MTRD) 772532

REGISTER BIT ASSIGNMENTS

15	14	13	12	11	10	09	08 07 06 05 04 03 02 01 00
TMR	---	---	GAP S/D	CPE	IBM PAK	PE I/D	NOT USED

In addition to its use for diagnostic purposes, this register receives additional command bits from the CPU and provides additional status information from the tape adapter and from the tape drive.

TRD BIT 15 TIMER - This read-only bit provides the diagnostic program with the output of a 10 KHz timer. This timer bit, having a 50% duty cycle, is used by the diagnostic program for measuring the time duration of tape operations.

MTRD BIT 14 AND BIT 13 (NOT USED)

MTRD BIT 12 GAP SHUT-DOWN BIT - This bit indicates the tape adapter's post-record positioning time period.

MTRD BIT 11 CORRECTABLE PARITY ERROR - This bit is true in the Read Mode when a phase encoded tape is being corrected because of a single channel dropout.

MTRD BIT 10 IBM PACK MODE - When this Write/Read bit is set by the CPU, The IBM Pack mode is set, enabling the controller's internal byte swapping circuity. IBM/industry-compatible tape may then be read or written by the tape adapter.

MTRD BIT 9 P.E. IDENTIFICATION - When read, this bit is true to indicate the Identification Burst of a phase encoded tape is being read by the tape adapter.

MTRD BITS 8-0 (NOT USED)

EXTENDED ADDRESS REGISTER (EAR) 772534

REGISTER BIT ASSIGNMENTS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NOT USED				CURRENT MEM ADD				NOT USED							
				21	20	19	18								

This register is a write-only port for the 22-bit extended address bits CA18 through CA21. The read function of this register is undefined. However, as it is currently implemented, when it is read, it displays the data word register used for DMA transfers.

EAR BITS 11-08 CURRENT MEMORY ADDRESS BITS 21-19 - These bits represent the extended bits of the memory address register function. These are write-only bits. The Current Memory Address Register (MTCMA) contains bits CA00 through CA15.

EAR BITS 15-12, 07-00 (NOT USED)

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SECTION IV

TAPE INTERFACE

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SECTION IV - TAPE INTERFACE

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SECTION IV

TAPE INTERFACE

FORMATTED TAPE DRIVE INTERFACE

This section defines the interface to the tape formatter for the streaming or non-streaming tape units controlled by the tape adapter. This interface is based on the industry standard interface for 1/2 inch formatted tape units, While basic industry conventions such as cabling, electrical characteristics, data and command transfer characteristics, and timing have been maintained, the interface deletes DENSITY SELECTION, EDIT functions, and CLIP LEVEL selection in favor of several functions unique to streaming tape transports. These additional functions include: (1) SPEED/MODE CHANGE command for selecting streaming or start-stop modes, and (2) GAP LENGTH control for selecting 0.6 or 1.2 inch interrecord gaps.

Two 50-conductor 3M-type ribbon cables are used for interconnection between the satndard or streaming transport formatter and the tape adapter. These cables are connected between the card edge connectors of the tape adapter and the streaming formatter PC board. Cable length can be a maximum of 6.0 meters (20 feet).

The formatter input circuits are designed such that either a disconnected wire or removal of power at the transmitter results in a false signal being interpreted at the receiver end. All lines between the tape adapter and the drive's formatter are low-true and driven by tri-state devices,

The following tables provide a list of pins and a definition of terms as used on the interface between the tape adapter and the formatter.

CONNECTOR	SIGNAL PIN	RETURN PIN	SIGNAL	CONNECTOR	SIGNAL PIN	RETURN PIN	SIGNAL
J1	2	1	$\overline{\text{FFBY}}$	J2	1	5	$\overline{\text{FRDP}}$
	4	3	$\overline{\text{FLWD}}$		2	5	$\overline{\text{FRDO}}$
	6	5	$\overline{\text{FWD4}}$		3	5	$\overline{\text{FRD1}}$
	8	7	$\overline{\text{FGO}}$		4	5	$\overline{\text{FLDP}}$
	10	9	$\overline{\text{FWDO}}$		6	5	$\overline{\text{FRD4}}$
	12	11	$\overline{\text{FWD1}}$		8	7	$\overline{\text{FRD7}}$
	14	13	SPARE		10	9	$\overline{\text{FRD6}}$
	16	15	NOT USED		12	11	$\overline{\text{FHER}}$
	18	17	$\overline{\text{FREV}}$		14	13	$\overline{\text{FFMK}}$
	20	19	$\overline{\text{FREW}}$		16	14	$\overline{\text{FID}}$
	22	21	$\overline{\text{FWDP}}$		18	17	$\overline{\text{FFEN}}$
	24	23	$\overline{\text{FWD7}}$		20	19	$\overline{\text{FRD5}}$
	26	25	$\overline{\text{FWD3}}$		22	21	$\overline{\text{FEOT}}$
	28	27	$\overline{\text{FWD6}}$		24	23	$\overline{\text{FOFL}}$
	30	29	$\overline{\text{FWD2}}$		26	25	NOT USED
	32	31	$\overline{\text{FWD5}}$		28	27	$\overline{\text{FRDY}}$
	34	33	$\overline{\text{FWRT}}$		30	29	$\overline{\text{FRWD}}$
	36	35	NOT USED		32	31	$\overline{\text{FFPT}}$
	38	37	$\overline{\text{FLGAP}}$		34	33	$\overline{\text{FRSTR}}$
	40	39	$\overline{\text{FERASE}}$		36	35	$\overline{\text{FDWDS}}$
	42	41	$\overline{\text{FWFM}}$		38	37	$\overline{\text{FDBY}}$
	44	43	NOT USED		40	39	NOT USED
	46	45	$\overline{\text{FTADO}}$		42	41	$\overline{\text{FCER}}$
	48	47	$\overline{\text{FRD2}}$		44	43	$\overline{\text{FONL}}$
J1	50	49	$\overline{\text{FRD3}}$		46	45	$\overline{\text{FTAD1}}$
					48	47	$\overline{\text{FFAD}}$
				J2	50	49	$\overline{\text{FSMC}}$

Table 4-1 I/O Cable Pin Assignments

SIGNAL	DEFINITION	DESCRIPTION
$\overline{\text{FFAD}}$	Formatter Address	This signal level selects one of two possible transports attached to transport interface: 1. $\overline{\text{FFAD}}$ False = Address 0 2. $\overline{\text{FFAD}}$ True = Address 1 The transport's address is predetermined by a strap on the formatter PWA.
$\overline{\text{FTAD0}}$ $\overline{\text{FTAD1}}$	Transport Address	Addresses up to 4 transports per formatter.
$\overline{\text{FGO}}$	Initiate Command	This signal is used to strobe the following command lines on the trailing edge: 1. $\overline{\text{FREV}}$ 2. $\overline{\text{FWRT}}$ 3. $\overline{\text{FWFM}}$ 4. $\overline{\text{FERASE}}$ 5. $\overline{\text{FLGAP}}$ 6. $\overline{\text{FSMC}}$
$\overline{\text{FREV}}$	Reverse/Forward	This signal specifies the direction of tape motion as follows: 1. False = Forward 2. True = Reverse
$\overline{\text{FWRT}}$	Write/Read	This signal specifies the read or write mode as follows: 1. False = Read 2. True = Write
$\overline{\text{FWFM}}$	Write File Mark	
$\overline{\text{FERASE}}$	Erase Tape	If $\overline{\text{FERASE}}$ and $\overline{\text{FWRT}}$ are low, the transport is positioned to execute a Dummy-Write command. The transport will go through all of the operations of a normal Write command except that no data is recorded. A length of tape will be erased equivalent to the length of the Dummy-Record (as defined by $\overline{\text{FLWD}}$). Alternatively, if $\overline{\text{FERASE}}$, $\overline{\text{FWRT}}$, and $\overline{\text{FWFM}}$ command lines are all low, the transport is conditioned to execute a Dummy-Write File Mark command. A fixed length of tape of approximately 3.6 inches will be erased.
FLGAP	Long Gap	When true, this line causes the transport to be set up for 1.2 inch gap. When false, will select the normal 0.6 inch gap.

Table 4-2 Tape Adapter To Formatter Signals

SIGNAL	DEFINITION	DESCRIPTION
$\overline{\text{FSMC}}$	Speed Mode Change	This signal causes selected transports to change the mode of operation (12.5 ips/ 100 ips).
$\overline{\text{FREW}}$	Rewind	This signal (minimum 1.0 microsecond pulse) causes the selected transport to rewind to BOT. The $\overline{\text{FRWD}}$ signal is asserted during the rewind operation. Formatter Busy is not set during a Rewind.
$\overline{\text{FOFL}}$	Off-line and Rewind	This line must be held true for a minimum of 1.0 microsecond. It causes the transport to rewind and unload the tape. Formatter Busy is not set.
$\overline{\text{FWDO-7}}$ $\overline{\text{FWDP}}$	Write Data	These lines transmit data to the transport. $\overline{\text{FWDO}}$ is the most significant.
$\overline{\text{FFEN}}$	Formatter Enable	This signal, when false, causes the transport to be reset to initialized state. It is independent to $\overline{\text{FFAD}}$. This is a level signal that will hold the transport reset while false.
$\overline{\text{FLWD}}$	Last Word	During Write and Controlled Erase, this line, when true with $\overline{\text{FWDO-7}}$, $\overline{\text{FWDP}}$ indicates that the character being strobed into the formatter is the last of the record.

Table 4-2 Tape Adapter To Formatter Signals (Continued)

COMMAND	LOOP	SNSR	REV	WRT	WFM	ERASE
Read Forward*	L	L	L	L	L	L
Read Reverse*	L	L	H	L	L	L
Write*	L	L	L	H	L	L
Write File Mark	L	L	L	H	H	L
Space Forward	L	L	L	L	L	H
Space Reverse	L	L	H	L	L	H

L = Low = False

H = High = True

* $\overline{\text{FLGAP}}$ is also strobed during these command transfers indicating the setting of a long or normal gap length (1.2 inch IBG or 0.6 inch IBG nominal, respectively). $\overline{\text{FSMC}}$ is also strobed by $\overline{\text{FGO}}$. However, $\overline{\text{FSMC}}$ is not issued during data operations.

Table 4-3 Formatter Interface Commands

SIGNAL	DEFINITION	DESCRIPTION
$\overline{\text{FFBY}}$	Formatter Busy	Only goes true when $\overline{\text{FGO}}$ command is received. Remains true until completion of command execution.
$\overline{\text{FDBY}}$	Data Busy	Only goes true when the transport has reached operating speed/traversed the IBG, and the transport is about to write data on the tape or read data from the tape. Data Busy remains low until the data transfer is finished. A new command may be given when Data Busy goes false for an "on-the-fly" operation. "On-the-fly" commands must be the same read/write mode and same tape direction.
$\overline{\text{FID}}$	PE Identification Burst Detected	Set when writing first record from load point or reading first record from load point if tape is PE.
$\overline{\text{FHER}}$	Hard Error	This line is set low if any error has been detected. This line will be set low as soon as an error occurs and stays low until the next $\overline{\text{FGO}}$ signal is transmitted, or the $\overline{\text{FFEN}}$ signal is set high. All error information will be reportec to the controller before $\overline{\text{FDBY}}$ signal goes false.
$\overline{\text{FCER}}$	Corrected Error	This line is set low whenever a single track error occurs during a read or read-after-write operation. The signal will stay true until the next $\overline{\text{FGO}}$ signal is transmitted or $\overline{\text{FFEN}}$ signal is set high. If the $\overline{\text{FCER}}$ signal is set low during the read-after-write operation, the record should be rewritten.
$\overline{\text{FFMK}}$	File Mark Detected	
$\overline{\text{FRDY}}$	Selected Transport Ready	
$\overline{\text{FONL}}$	Selected Transport On-Line	
$\overline{\text{FRWD}}$	Rewind	
$\overline{\text{FEOT}}$	End of Tape	

Table 4-4 Formatter To Tape Adapter Signals

SIGNAL	DEFINITION	DESCRIPTION
$\overline{\text{FFPT}}$	File Protect	
$\overline{\text{FLDP}}$	Load Point	
$\overline{\text{FDWDS}}$	Demand Write Data Strobe	This line consists of a pulse for each data character to be written onto tape. The pulse width of signal $\overline{\text{FDWDS}}$ is 1 microsecond. The first data character should be available on the write data input lines within one character period after the $\overline{\text{FDBY}}$ signal has been set true, and remain true until the trailing edge of the first $\overline{\text{FDWDS}}$ signal. Succeeding characters must then be placed on these lines within one-half of a character period after the trailing edge of each FDWDS signal. During a Write File Mark command, the required file mark pattern is generated internally by the formatter and the $\overline{\text{FDWDS}}$ signal is not used. During erase operation (variable length), this line will also be used. However, no data are transferred or written onto tape. The controller may use this line to determine the length of tape which has been erased.
$\overline{\text{FRSTR}}$	Read Data Strobe	This line consists of a pulse for each character of read information to be transmitted to the customer controller interface and should be used to sample the read data lines $\overline{\text{FRDP}}$, $\overline{\text{FRD0-7}}$. The pulse width of this signal is 1.2 microseconds. The average time between pulses on the $\overline{\text{FRSTR}}$ line is given by: $\frac{1}{S \times D}$ Where S = tape speed (ips) and D = 1600 bpi The customer controller interface must be able to accept the whole block of data at the specified data rate. Due to bit crowding, tape speed variation, and signal drop-out correction (PE), the customer controller interface must be able to receive characters at a rate which can

Table 4-4 Formatter To Tape Adapter Signals (Continued)

SIGNAL	DEFINITION	DESCRIPTION
$\overline{\text{FRSTR}}$	Read Data Strobe (Cont'd)	vary between twice the nominal rate and half the nominal rate.
$\overline{\text{FRD0-7}}$ $\overline{\text{FRDP}}$	Read Data	These nine lines transmit read data from the formatter to the customer controller. Each character read from tape is available to sampling these lines in parallel with the $\overline{\text{FRSTR}}$. Data will be placed on the read data lines at least 0.5 microseconds prior to the leading edge of the $\overline{\text{FRSTR}}$ pulse. The data remains on the read data lines for at least 0.5 microseconds after the trailing edge of the $\overline{\text{FRSTR}}$ pulse. Sense data is also transmitted on this bus analogous to the read data at 160K byte/second rate.

Table 4-4 Formatter To Tape Adapter Signals (Continued)

SECTION V

TAPE FORMAT

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SECTION V - TAPE FORMAT

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SECTION V

TAPE FORMAT

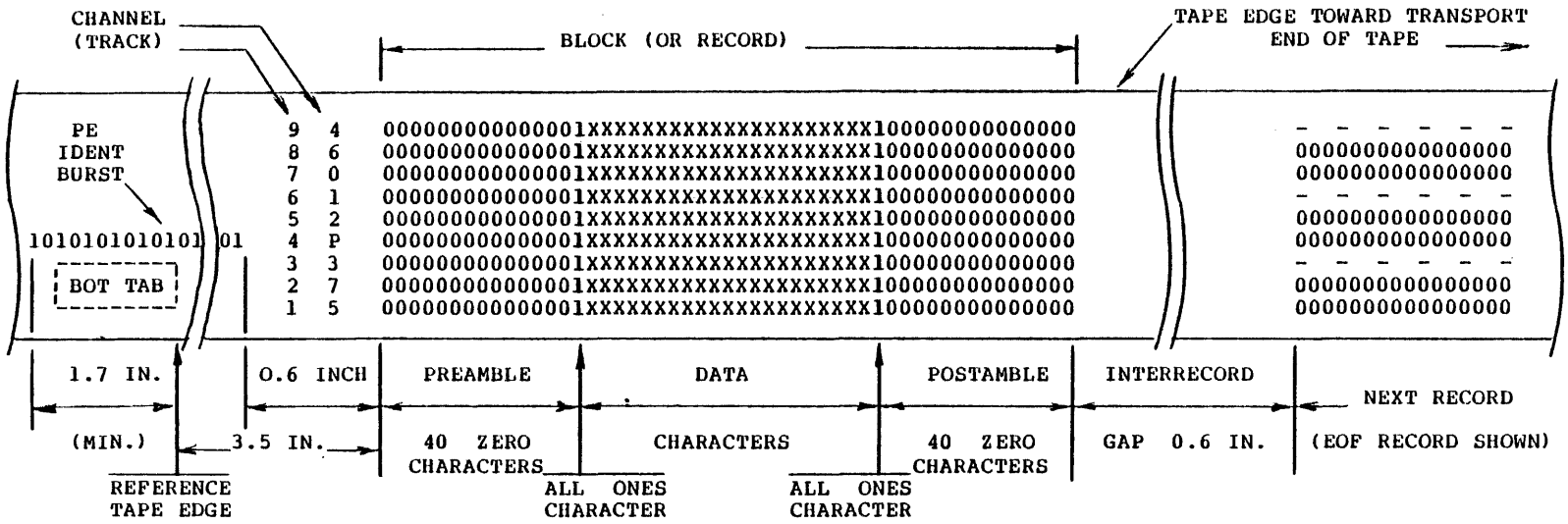
INTRODUCTION

The TC-30 Tape Adapter interfaces to industry standard formatted tape drives which write nine bit characters laterally across the tape. While the formatter in the drive is responsible for actually writing the data, this section provides an insight into how the data is formatted on tape. The density of the characters written on the tape is determined by the type of tape unit and (in some cases) the density selection made at the drive and/or the command issued by the CPU. A data block (record) written on the tape consists of data characters and error checking characters (or a preamble and postamble). Every data character consists of the data byte plus an odd parity bit that is generated by the formatter to conform with odd parity as specified by the format. A record (or block) of data on tape represents the data transferred to or from a block of memory in response to one read or write command. Adjacent records are separated by automatically erasing a 0.6 inch segment of tape to form an interrecord gap (IRG).

NINE TRACK PE FORMAT

The tape adapter uses the standard nine track Phase Encoded (PE) 1600 bits per inch tape format. Each tape block contains a preamble, a variable length data field, and a postamble. The 41 character preamble consists of 40 tape characters with all-zero bits followed by one character of all-one bits. The preamble is followed by the data field which also contains an odd vertical parity bit for each data character. Following the last character of the data field is the postamble which contains an all-ones character followed by 40 all-zero characters (the reverse-image of the preamble).

When the tape is at load point (beginning of tape) and the first data block is to be written, it is preceded by an identification burst consisting of alternating one and zero bits in the track for the parity (P) channel. with all other tracks erased. The file mark consists of 40 all-zero characters similar to those in the preamble or postamble, except that the tracks for channels 1, 3 and 4 are erased.



NOTES:

1. Tape shown oxide side up.
2. Channels 0 thrtough 7 contain data in decending order of significance.
3. Parity channel (P) always contains odd data character parity.
4. The PE Identification Burst contains alternating one and zero bits.
5. Data is recorded at 1600 characters per inch.
6. A File Mark is a 40 character burst, with "0" bits in channels P. 0, 2, 5, 6 and 7. Channels 1, 3, and 4 are erased and indicate dead tracks when read back. The EOF is preceded by a normal 0.6 inch gap, and is also separated by any following data record by a 0.6 inch inch gap.

Figure 5-1 1600 BPI PE Tape Format

NINE TRACK NRZI FORMAT

In the nine-track NRZI format, characters are written on the tape in 800 bits per inch density. Each data character contains eight data bits and one odd vertical parity bit. Following the last data character, the End of Record (EOR) gap (three blank characters) is written, followed by a Cyclic Redundancy Check (CRC) character, followed by three more blank characters, concluded by a Longitudinal Redundancy Check (LRC) character. The LRC character produces an even longitudinal parity in each of the tracks along the length of the tape. Reading or Writing, the tape adapter checks to ascertain that the lateral parity of every data character is odd, that the CRC character is correct, and that every track has even longitudinal parity.

The nine-track NRZI file mark consists of a single character record with a one-bit in channels 3, 6 and 7; the remaining channels contain zeros. The CRC character is left blank, but an LRC character is written which is identical to the file mark character.

RECORDING METHODS

NRZI and Phase Encoded formats are recorded on tape, using different recording techniques. In Figure 5-3, NRZI and PE waveforms are compared. The NRZI waveform shows a change in flux polarity for each binary one bit. A binary zero is represented by the absence of a flux change.

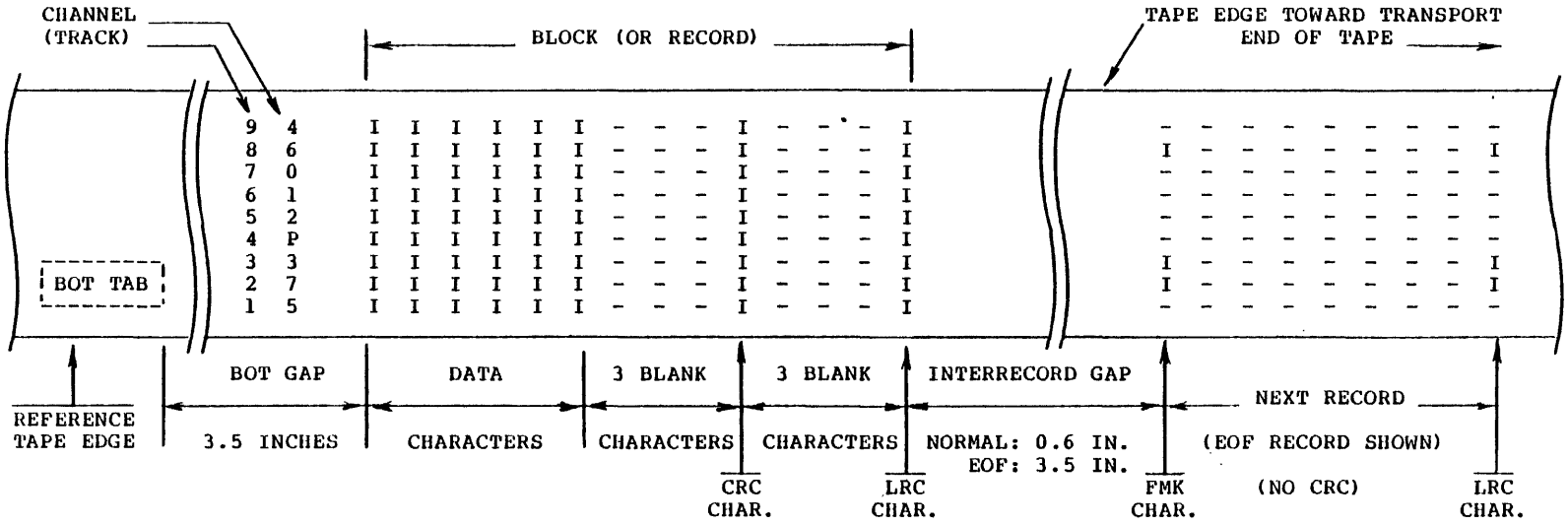
Phase encoded recording requires at least one flux change per bit cell. A binary zero leaves the flux polarized opposite to that of the interrecord gap.

DATA BLOCK SIZE

The maximum data block size is only limited by the Byte/Record Counter to a full 64K byte block. The minimum recommended data block size can vary with the application, depending upon the system where the generated tapes will be used.

END-OF-FILE MARKS

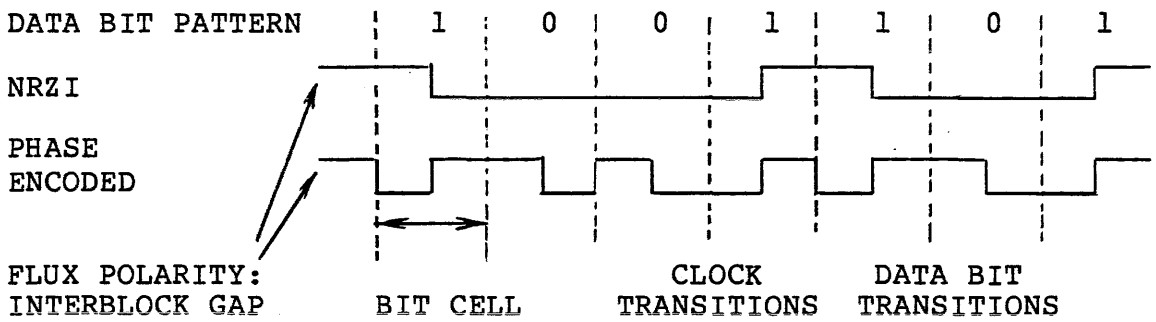
The program can group sets of data records into files. The end of a file is indicated by an End Of File (EOF) mark. The PE File Mark consists of 40 all-zero characters in a special combination of active and dead tracks. The NRZI File Mark is a special record containing only one special data character and its corresponding LRC character. Each EOF in the NRZI format is preceded by an extended record gap.



NOTES:

1. Tape shown oxide side up.
2. Channels 0 thrtough 7 contain data in decending order of significance.
3. Parity channel (P) always contains odd data character parity.
4. Each bit of the LRC ensures even parity for that track, including total of all data and CRC bits. The LRC is never all zero bits.
5. It is possible for the CRC to be all zeros.
6. A File Mark is a single character record, with "1" bits in channels 3, 6 and 7 for both the data character and the LRC. The CRC contains all zeros. The EOF is preceded by a 3.5 inch gap, and is separated by any following data record by a normal 0.6 inch gap.
7. Data is recorded at 800 characters per inch.

Figure 5-2 800 BPI NRZI Tape Format



NOTES:

NRZI: Any change in polarity is a "1" bit. No change in polarity is "0" bit.

PE: Data bit transition in direction of gap polarity is a "1" bit, opposite direction is a "0" bit.

Last transition (LRC) returns flux to gap polarity.

Figure 5-3 PE and NRZI Recording Comparison

TRANSFERS

When writing, the controller divides each computer word into two eight-bit bytes. In reading, the bytes from the tape are reassembled into a full sixteen-bit word for the computer bus.

TAPE-END MARKERS

The ends of the tape contain reflective strips that are detected by photo cells in the tape drive. The Load Point marker identifies the logical Beginning of Tape (BOT) and is positioned to allow at least ten feet of leader at the front of the tape. A Space Reverse or Rewind command automatically stops at this marker. At least three inches of tape are erased between the BOT marker and the first record.

The End of Tape (EOT) marker is located at least 14 feet from the physical end of the tape. The program should not record more than a few feet beyond the EOT marker, allowing at least ten feet of tape for a trailer. A status bit is set and any Space Reverse operations are terminated when the tape passes beyond the EOT marker.

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SECTION VI

COMPUTER INTERFACE

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SECTION VI - CONPUTER INTERFACE

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SECTION VI

CONPUTER INTERFACE

DEC PDP-11 UNIBUS

The tape adapter interfaces to the Unibus of the DEC PDP-11 computer system. The Unibus is an asynchronous I/O bus with separate 18-bit (or optionally 22-bit) address lines and 16 bit data bus lines. In addition to address and data information, the bus contains signal lines for NPR (DMA) Operations, Bus Requests (Interrupts), data transfer handshaking, initialization of devices and other control signals.

BUS INTERFACE SIGNALS

The interface signals used by the tape adapter to communicate with the bus, along with the connector and pin assignments, are shown in Table 6-1. The functions of these signals, as illustrated in Figure 6-1, are:

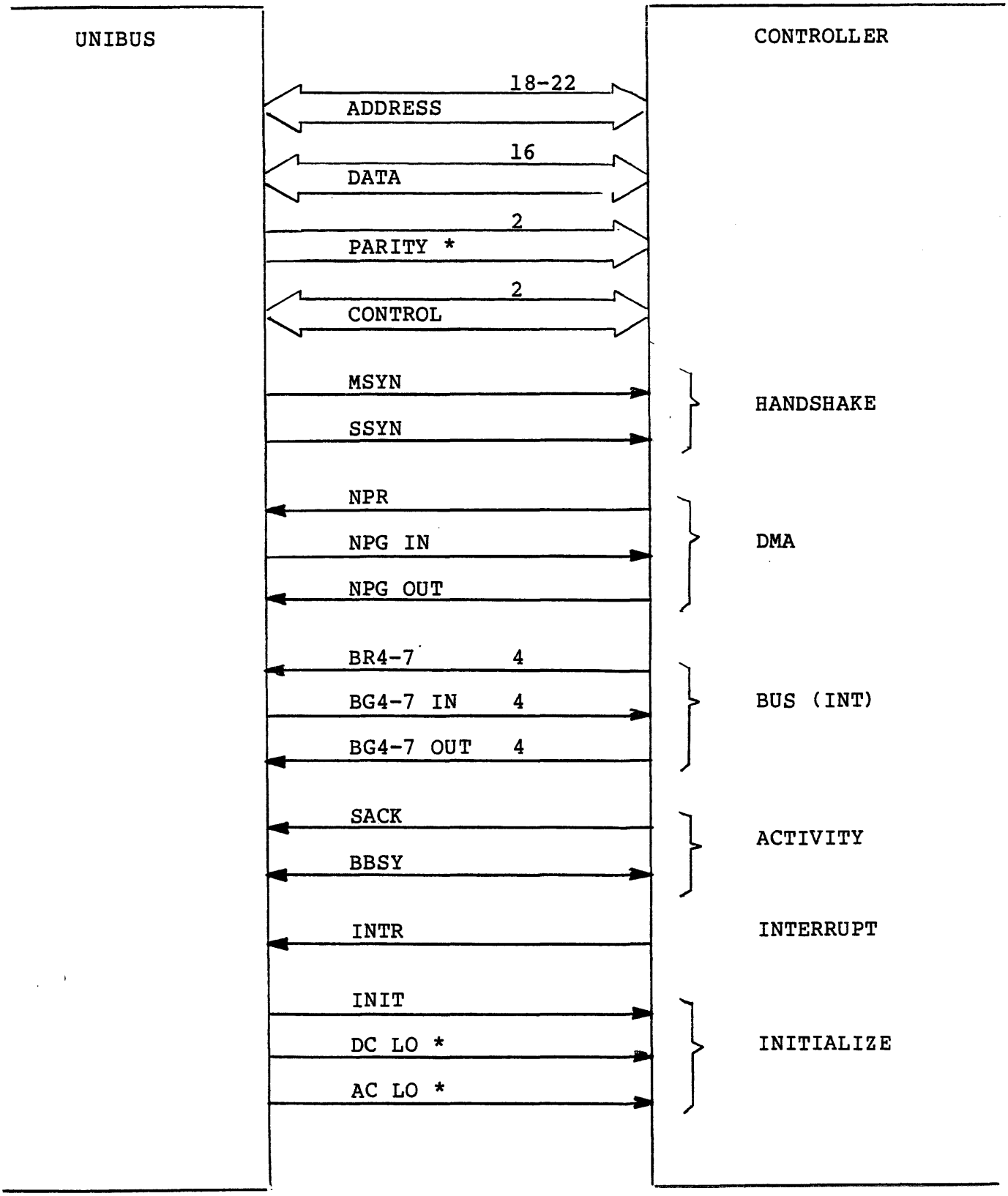
1. A0-A17/-A21 (ADDRESS LINES) - These lines are the 18-bit (or optionally 22-bit) address bus over which memory address and peripheral register address information is communicated. Address information is placed on the bus by the bus master device and is received and decoded by the selected slave device. The master device then either receives input data from, or outputs data to the addressed slave device (or memory) over the data bus lines.

2. D0-D15 (DATA LINES) - These 16 lines are used to transfer data and register control/status information to and from the tape adapter.

3. PA,PB (PARITY) - These lines are used by certain devices to indicate parity errors. (Not used in this device.)

4. C0, C1 (CONTROL LINES) - These two lines are coded by the master device to describe the type of transfer, as follows:

C1	C0	OPERATION
0	0	DATI - Data In (to master)
1	0	DATO - Data Out (from master)
1	1	DATOB - Data Out, Byte (from master)



* Not used in this device

Figure 6-1 Bus Interface

5. MSYN (MASTER SYNC) - This control signal is issued by the master device to indicate that Address and Control information is present on the bus.

6. SSYN (SLAVE SYNC) - This control signal is issued by the slave device in response to the signals MSYN or INTR generated by the master device.

7. NPR (NON-PROCESSOR REQUEST) - This signal is asserted by the tape adapter to request control of the bus for the purpose of transferring drive data directly to or from memory.

8. NPG (NON-PROCESSOR GRANT) - This signal is generated at the processor in response to the NPR, at the end of the bus cycle in progress. Since NPG is daisy-chained through the devices connected to the bus, it is received and regenerated by each device until it reaches the requesting device.

9. BR4-BR7 (BUS REQUEST LINES) - One of these lines will be asserted by the conrtroller to request control of the bus for the purpose of interrupting the processor.

10. BG4-BG7 (BUS GRANT LINES) - One of these signals is generated at the processor in response to the corresponding Bus Request signal, after completing the instruction in progress. Since the Bus Grant lines are daisy-chained through the devices connected to the bus, it is received and regenerated by each device until it reaches the requesting device.

11. SACK (SELECTION ACKNOWLEDGE) - This signal is asserted by the tape adapter in response to the processor's NPG or Bus Grant signal, indicating that control of the bus will pass to the tape adapter when the current bus master completes its operation.

12. BBSY (BUS BUSY) - This signal is asserted by the bus master to indicate that the bus is in use. When BBSY goes false, control of the bus is passed to the new bus master.

13. INTR (INTERRUPT REQUEST) - The tape adapter asserts this signal after becoming bus master to indicate that the desired Interrupt Vector information is present on the bus.

14. INIT (INITIALIZE) - This signal is asserted by the processor to initialize or clear all devices connected to the bus.

15. DC LO (DC POWER LOW) - This signal from the power supply initiates power-on sequencing in the computer and some devices. (Not used in this device.)

16. AC LO (AC POWER LOW) - This signal from the power supply initiates power-fail sequencing in the computer and some devices. (Not used in this device.)

BUS OPERATIONS

The tape adapter receives commands from and provides status information to the processor, with the tape adapter being the slave device. After the tape adapter receives the proper commands to transfer data, the tape adapter becomes a bus master device, handling the data transfers directly with memory (a process which requires no processor intervention). When the tape adapter has completed all data transfers, it alerts the processor by issuing an interrupt request. Bus operations are illustrated in Figures 6-2, 6-3 and 6-4 and are described in the following paragraphs.

The tape adapter requests a data transfer on the bus by asserting NPR. After completing the current bus cycle, the processor inhibits initiation of a new bus cycle and responds by asserting NPG. The tape adapter then asserts SACK and removes NPR, causing the processor to terminate NPG. When BBSY goes false, the tape adapter becomes bus master, asserting BBSY, and executing the required data transfer of one or more data words to or from memory. When the data transfer is completed, the tape adapter relinquishes the bus to the processor by terminating the BBSY signal. The processor then returns to its programmed operations.

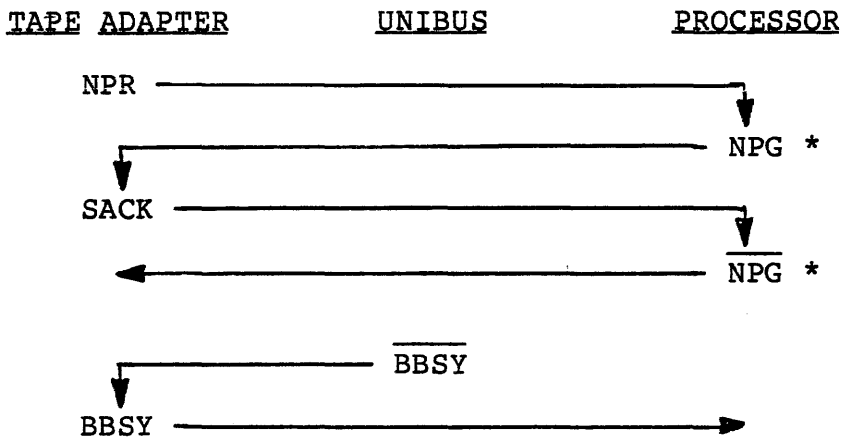
INPUT AND OUTPUT OPERATIONS

Input operations are used by the processor to receive status information from the tape adapter and are used by the tape adapter to obtain data from memory to be written onto tape. Output operations are used by the processor to provide the tape adapter with command information and are ased by the tape adapter when transferring information read from tape to the desired location in memory.

To begin an input transfer, address, control and MSYN are placed on the bus. The slave device responds by placing data and SSYN on the bus. The master device then receives the data, terminating MSYN, which causes the slave device to remove both SSYN and the data from the bus lines. The BBSY signal is then removed by the master device, terminating the input transfer. For an output transfer, data is placed on the bus by the master device together with MSYN. The slave device accepts the data and acknowledges by asserting the SSYN signal, which causes the master device to remove the data and terminate the MSYN signal. This action by the master device causes the slave to remove the SSYN signal which in turn causes the master to remove the BBSY signal, terminating the output transfer.

INTERRUPTS

Interrupts are used in the system so that the processor is not burdened with the responsibility of determining when the



* NOTE: Daisy-chained signal

Figure 6-2 DMA Request/Grant Sequences

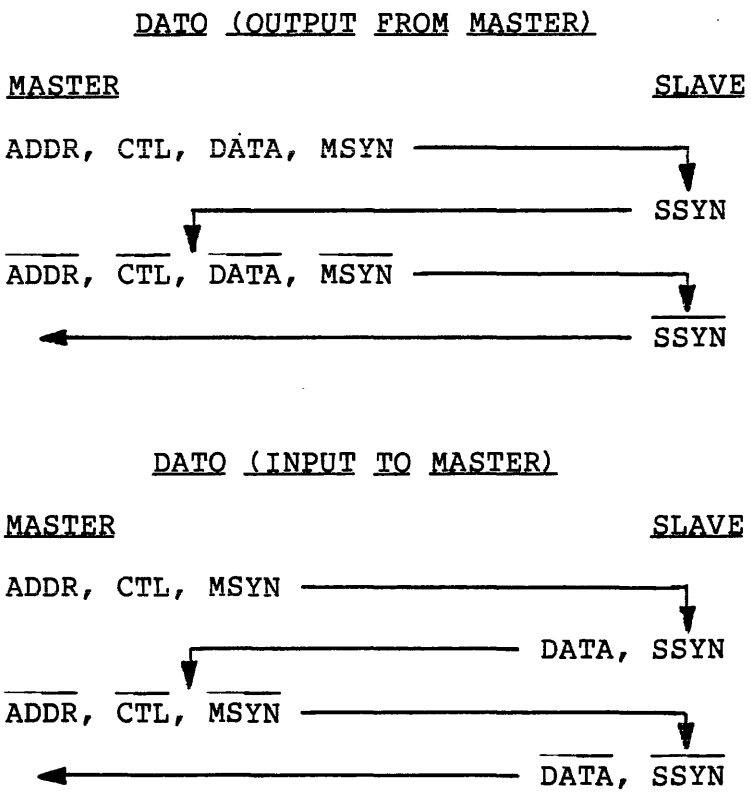
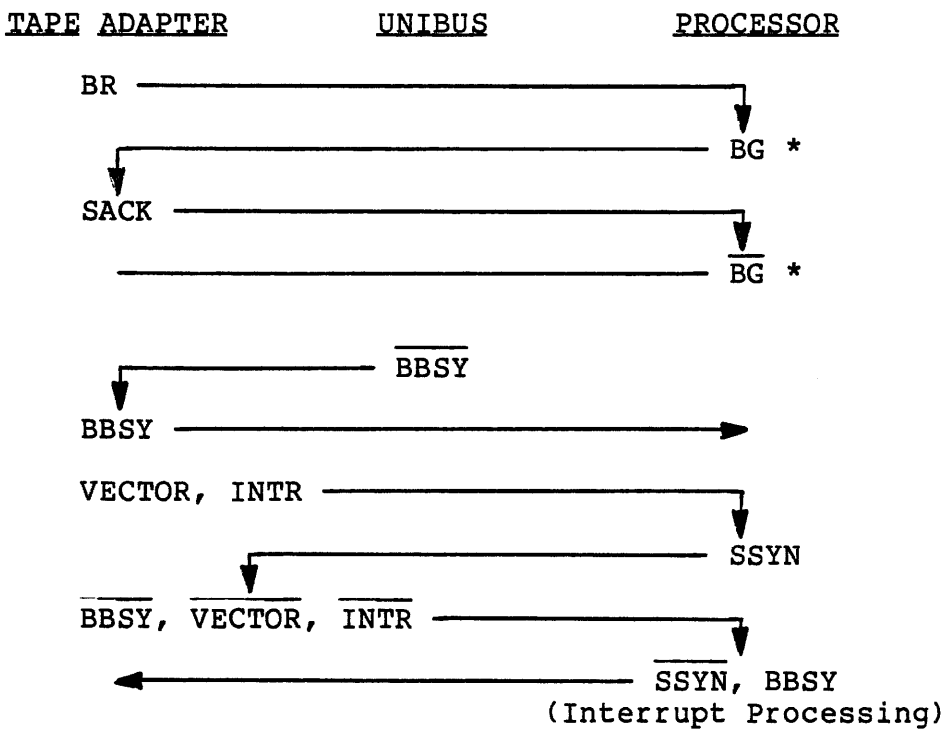


Figure 6-3 Bus Transfer Sequences

tape adapter has completed an operation. Interrupt processing allows the processor to continue with its programmed tasks until alerted by the tape adapter. When enabled in the tape adapter, the Bus Request is issued by the tape adapter to the processor upon completion of an operation. If the processor currently is accepting Bus Requests at that priority level, the daisy-chained Bus Grant signal is issued as a response. The Bus Grant signal is passed along by each device until captured by the requesting tape adapter. The interrupting tape adapter will then remove the Bus Request and assert SACK. When the instruction in progress has been completed, further program execution is suspended and the BBSY signal is released, allowing the tape adapter to become bus master. It asserts BBSY and INTR and places its hardwired vector address onto the bus. The vector points to memory locations containing a new processor status word (psw) and the program counter address (pc) of the interrupt handling routine. The processor saves its current processor status word and program counter address, receives the vector, and then terminates the SSYN signal. This causes the tape adapter to terminate the BBSY and INTR signals and remove the vector from the bus. The processor will then enter the tape adapter's interrupt service routine to handle the interrupt.



* NOTE: Daisy-chained signal

Figure 6-4 Bus Request/Interrupt Sequence

CONNECTOR F

PIN	SIDE 1	SIDE 2
A		+5V
B		-15V
C		GND
D	BBSYL	
E		
F		
H		
J	NPRL	
K		
L		
M	INTRL	
N		
P		
R		
S		
T	GND	SACKL
U		
V		

CONNECTOR E

PIN	SIDE 1	SIDE 2
A		+5V
B		
C	A12L	GND
D	A17L	A15L
E	MSYNCL	A16L
F	A07L	C1L
H	A01L	A00L
J	SSYNCL	C0L
K	A14L	A13L
L	A11L	
M		
N		A08L
P	A10L	A07L
R	A09L	
S		
T	GND	
U	A06L	A04L
V	A05L	A03L

CONNECTOR D

PIN	SIDE 1	SIDE 2
A		+5V
B		
C		GND
D		BR7L
E		BR6L
F		BR5L
H		BR4L
J		
K		BGIN7H
L	INITL	BGOUT7
M		BGIN6H
N		BGOUT6
P		BGIN5H
R		BGOUT5
S		BGIN4H
T	GND	BGOUT4
U		
V		

CONNECTOR C

PIN	SIDE 1	SIDE 2
A	NPGH	+5V
B	GOUTH	
C		GND
D		D15N
E		D14N
F		D13N
H	D11N	D12N
J		D10N
K		D09N
L		D08N
M		D07N
N	DCLOL	D04N
P		D05N
R		D01N
S	PBL	D00N
T	GND	D03N
U		D02N
V		D06N

* Connectors A and B use only ground connections (T1, C2)

Table 6-1 Unibus Signals

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APPENDIX A

SIGNAL GLOSSARY

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MNEMONIC	ORIGIN	TERM	COMMENTS
BCØ-15	10	Byte Count Ø-15	Register that counts the number of bytes in a record for control of DMA transfer. Also used to count number of records spaced in space operation
BCCL	15	Byte Count Clock Lower Byte	Used to load byte count register during I/O operation and count bytes during DMA operation and count records in space
BCCU	15	Byte Counter Clock Upper Byte	Used to load byte count register during I/O operation and count bytes during DMA operations and count records during space operation
BGL	9	Bus Grant Late	Status indicating that the data transfer rate the computer DMA transfer would allow was less than the adapter required
BGTN	2	Bus Grant In	Unibus priority bus grant from previous device for interrupt operation
BGTT	4	Bus Grant Out	Unibus priority bus grant to next device if this device is not requesting interrupt
BOT	13	Beginning of Tape	Status from tape system indicating the tape is positioned over the load point marker
BRX	4	Bus Request 4,5,6, or 7	This devices request for interrupt to unibus's "BR" line
BTG	15	Bad Tape Generate	Not used by adapter
BXFR	9	Byte Transfer	Indicates when an odd byte of information must be transferred by DMA at the beginning or end of a record

MNEMONIC	ORIGIN	TERM	COMMENTS
BXFR*	9	Byte Transfer Gated	Control to unibus to DMA transfer a byte of information to memory instead of a word (Read Mode Only)
CØ	2	Control Ø	Unibus control line buffered that determines whether transfer is word or byte. Word = Ø, Byte = 1
C1	2	Control 1	Unibus control line buffered that determines direction of data transfer. To Master = Ø, From Master = 1
CAØ-15	10	Current Address Bits Ø-15	DMA address register
CA16-21	15	Current Address Bits 16-21	Extended DMA address register
CACE	15	Current Address Clock Extended	Clock for loading and incrementing extended address bits 16 and 17
CACL	15	Current Address Clock Lower	Clock for loading and incrementing address bits Ø-7
CACU	15	Current Address Clock Upper	Clock for loading and incrementing address bits 8-15
CACX	15	Current Address Clock Extended	Clock for loading and incrementing address bits 18-21
CACY	10	Current Address Carry	Carry from current address register bits Ø-15 to extended address bits
CLK	15	System Clock	
CPE	13	Corrected Parity Error	Status from formatter indicating the record read has a single track dropout that was successfully corrected
CRS	15	CRC,LRC Select	Not used by adapter

MNEMONIC	ORIGIN	TERM	COMMENTS
CUR	14	Control Unit Ready	Status indicating when adapter will accept new command
CUR*	14	Control Unit Ready Special	Special control unit ready for command porcessing FPLA
DBDD	12	Data Busy Delayed Delayed	"DBYS" delayed by two "CLK" periods
DBY	13	Data Busy	Status from formatter indicating when it is in its data transfer phase
DBYD	12	Data Busy Delayed	"DBYS" delayed by one "CLK" period
DBYS	12	Data Busy Synchronized	"DBY" resynchronized to "CLK"
DEN5,8	6	Density 5, 8	Control register bits - DEN5 OFF causes extended gaps on streamer drives DEN8 OFF selects streaming mode
DNBY	14	Data Not Busy	Detects end of data busy phase of formatter to enable executing of next command if its same class as previous
EADØ	9	Exclusive OR'ed Address Data Bit Ø	Non-inverts CAØ for DEC mode. Inverts CAØ for IBM mode
EDIT	15	Edit Mode	Used to control formatter when editing tape and executing special commands
EIN	6	Enable Interrupt	Command register bit that controls enabling of interrupts
EIS	4	Enable Interrupts Special	Used to detect if interrupts were already enabled before present enable command
EOT	14	End of Tape	Status indicating that the selected drive is positioned at or past the end of tape marker

MNEMONIC	ORIGIN	TERM	COMMENTS
EOTS	14	End of Tape Sense	Detects position of end of tape marker when tape is in motion
ERASE	6	Erase	Control term to formatter that selects erase command or space command
ERR	14	Error Status	Summation of error status's of TM11 status register ready on bit 15 of TM11 command register
EVEN	6	Even	Control from command register to write even parity
FDBØ-7,P	13	Formatter Data Bus Bits Ø-7,P	Buffered read data from formatter
FEOT	13	Formatter End of Tape	Buffered status from formatter indication detection of end of tape sensor
FFCL	9	FIFO Clock	FIFO Clock from formatter "WSTR" during write operation, "RSTR" during read operation
FFM	13	Formatter File Mark	Buffered file mark status from formatter
FFRY	9	FIFO Ready	Indicates FIFO ready for output in write operation and ready for input in read operation
FICL	9	FIFO Input Clock	Clock that transfers data into FIFO buffer
FIDØ-7	11,13	FIFO Input Data Bits Ø-7	Multiplexed input to FIFO Unibus data in write operation, formatter read data in read operation
FIR1-3	12	FIFO Input Ready 1-3	Individual status from each FIFO indicating that it is ready for new data to be input to it

MNEMONIC	ORIGIN	TERM	COMMENTS
FIRY	12	FIFO Input Ready	Status indicating that all FIFO's are available for input of new data
FIRY*	9	FIFO Input Ready Gated	"FIRY" gated with WRT to control DMA transfers
FLPT	13	File Protect	Buffered status from formatter indicating that tape does not have a write ring installed
FM	14	File Mark	Stored status from formatter indicating that the last record read was a file mark
FMBY	13	Formatter Busy	Buffered status from formatter indicating that it is busy doing a tape motion command
FNC1-3	6	Function Bits 1-3	Command register bits that determine type of operation to be executed when GO bit set
FOCL	9	FIFO Output Clock	Clock that transfers new data to output of data buffer FIFO's
FODØ-7	12	FIFO Output Data Bits Ø-7	Data output of FIFO Buffer
FOR1-3	12	FIFO Output Ready 1-3	Individual status from each FIFO indicating that it is ready with data on its outputs
FORY	12	FIFO Output Ready	Status indicating that all FIFO's have valid data on their outputs
GAPC	14	Gap Control	Used to issue write command after erase 3" gap command when executing a write with extended gap operation
GO	6	Go	Signal that initiates command to formatter

MNEMONIC	ORIGIN	TERM	COMMENTS
GO*	12	Go Gated	"GO" or'ed with rewind command and off line command for generating Go reset
GORS	12	Go Reset	Used to reset "GO" logic
GORS*	6	Go Reset Gated	"GORS" gated with reset and illegal command
GOST	6	Go Strat	Raw go command from control register bit Ø
IBM	15	IBM Mode	When true DMA transfer start with most significant byte of word
ICAY	10	Immediate Current Address Carry	Increment carry for lower byte of current address
IDEN	13	Idenfitication Status	Active when formatter detects ID burst at beginning of PE tape
ILC	6	Illegal Command	Set when computer software does illegal function
ILCS	6	Illegal Command Set	Active when condition exists that would be illegal if command issued
INCL	4	Interrupt Clock	Sets interrupt request at completion of operation
INIT	2	Initialize	Buffered unibus initialize line
INT	4	Interrupt	Signal to unibus defining this unibus transfer is an interrupt
IWCC	10	Intermediate Word Count Carry	Increment carry for lower byte of byte count register
MDBØ-7 MDB8-15	7 8	Multiplexed Data Bus Ø-15	Data bus for transferring I/O and DMA address and data to unibus

MNEMONIC	ORIGIN	TERM	COMMENTS
MOEX	14	Multiple Operation Execute	Issues additional "GO" commands to formatter for operations requiring multiple commands. Spacing, write ex gap, etc.
NPBN	4	Nonprocessor Busy & Interrupt Busy	Busy signal to unibus for both DMA and interrupt operations
NPBY	5	Nonprocessor Busy	Sets busy on unibus during DMA operation
NPBY*	5	Nonprocessor Busy Extended	"NPBY" extended by 160 ns to conform to unibus protocol
NPGN	2	Nonprocessor Grant In	Unibus "NPG" from previous device
NPGT	5	Nonprocessor Grant Out	Unibus "NPG" to next device if this device not requesting bus
NPMS	5	Nonprocessor Master Sync	MSYN to unibus during DMA transfer
NPR	5	Nonprocessor Request	"NPR" to unibus when this device is requesting DMA operation
NSCK	5	Nonprocessor Selection Acknowledge	Unibus sack for DMA operation request
NXB	9	Non-existent Memory or Bus Grant Late	Or of "BGL" and "NXM"
NXM	12	Non-existent Memory	Status indicating attempted DMA transfer to address containing no memory
NXMS	4	Non-existent Memory Set	Time out counter that detects lack of replay at non-existent memory address
ONLN	13	On Line	Buffered formatter signal indicating that tape drive is on line

MNEMONIC	ORIGIN	TERM	COMMENTS
PER	13	Parity Error	Buffered status from formatter indicating improper completion of operation
REDY	13	Ready	Buffered formatter "READY" signal
REV	6	Reverse	Signal to formatter instructing the tape to move in the reverse direction (space reverse)
RFCL	9	Register Fill Clock	Used to unload output of FIFO data buffer when data loaded into "QDR" during read operation
RLE	9	Record Length Error	Status indicating that the record read contains more data than DMA requested to transfer
RLLØ-7	3	Register Load Lower Byte Ø-7	Clocks to load lower bytes of TM11 registers during I/O operation
RLMØ-7	3	Register Load Upper Byte Ø-7	Clocks to load upper bytes of TM11 registers during I/O operation
RNSC	5	Ready for Nonprocessor SACK	Enables DMA protocol to respond with a "SACK" to Unibus
RST	3	Reset	System Reset
RSTR	13	Read Strobe	Buffered formatter read strobe
RSTS	3	Reset Start	Reset or'ed with start operation
RWC	6	Rewind Command	Clock to formatter to initiate rewind of tape
RWC*	12	Rewind Command Gated	"RWC" or'ed with "UNC"

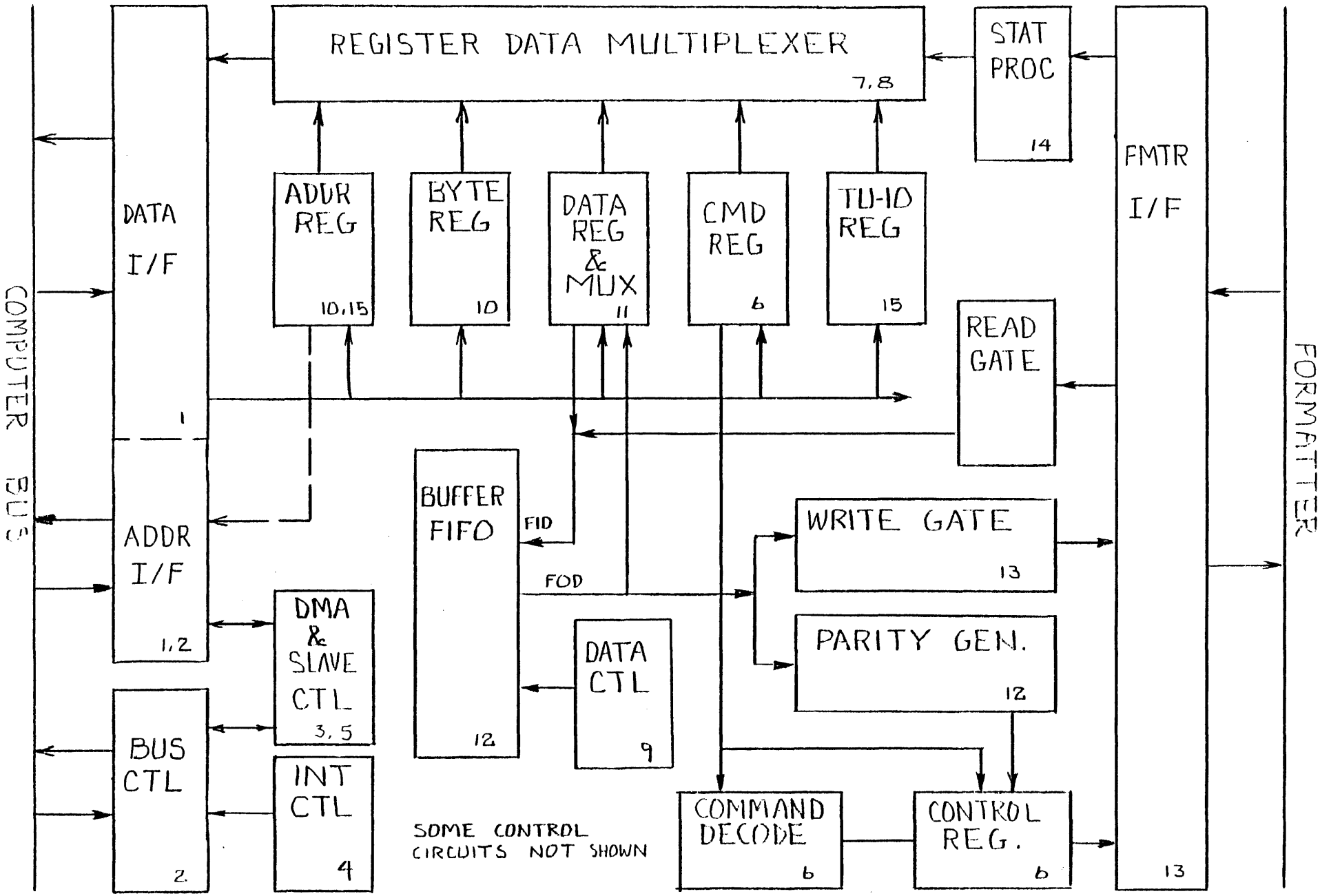
MNEMONIC	ORIGIN	TERM	COMMENTS
RWDG	13	Rewinding	Buffered formatter status indicating that drive is rewinding tape
RWDG*	3	Rewinding Gated	"RWDG" or'ed with logic that detects when new command is not same as previous when tape is stopping
RWGS	12	Rewinding Synchronized	"RWDG" status synchronized with clock
SAC	3	Selection Address Compare	Active when unibus address compares with one of the TM11 register assignments
SACK	4	Selection Acknowledge	Sack to unibus for acknowledging DMA or interrupt grant
SADØ-3	3	Stored Address Bits Ø-3	Lower order address bits stored for register selection during I/O operation
SADØ-3*	5	Stored Address Bits Ø-3 Stored	SAD1-3 modified to include addressing of address and data in DMA operating and interrupt vector during interrupt operation
SIDN	14	Stored Identification Status	"IDEN" stored for status to TM11 TU10 register
SPCM	6	Space Command	Decoded space command function
SPER	14	Stored Parity Error	"PER" stored for status to TM11 status register
SSY	2	Slave Sync	SSYN" to unibus acknowledge I/O transfer
STDN	15	Settle Down	Status to TM11 status register indicating that tape is stopping
STRD	12	Start Delayed	"STRT" delayed by a "CLK" period to make "GO" 1 micro-second wide

MNEMONIC	ORIGIN	TERM	COMMENTS
STRT	12	Start	"GO" synchronized with clock "CCK"
TUR	14	Tape Unit Ready	Tape unit ready and controller not busy
UAC	9	Unibus Address Clock	Increments the DMA address at the completion of each DMA transfer
UADØ-15	1	Unibus Address Bits Ø-15	Buffered unibus address bus
UAD16-21	2	Unibus Address Bits 16-21	Buffered extended unibus address
UAD5*-8*	3	Unibus Address Bits 5-8 Modified	Modifiable address bits used for selection of optional TM11 register addresses
UAUD	9	Unibus Address Update Done	Stops the incrementing of the DMA address after two clocks for word transfer and after one clock for byte transfer
UAUP	9	Unibus Address Update	Increments DMA address register when true
UAWC	9	Unibus Address Word Count Clock	Increments the DMA byte count register after each DMA transfer and at the detection of each record in space operation
UBAV	2	Unibus Available	Indicates both "BSY" and "SSYN" on unibus are inactive
UBDØ-15	1	Unibus Data Bus Bits Ø-15	Buffered unibus data bus
UBRX	2	Unibus Bus Request 4,5,6 or 7	Buffered unibus bus request
UBSY	2	Unibus Busy	Buffered unibus "BUSY" line

MNEMONIC	ORIGIN	TERM	COMMENTS
UDBE	5	Unibus Data Bus Enable	Enables this devices unibus data bus drivers for both I/O, DMA, and interrupt transfers
UDRØ-15	11	Unibus Data Register Bits Ø-15	TM11 data register used for DMA operations
UMSN	2	Unibus Master Sync	Buffered unibus master sync line
UMSN*	2	Unibus Master Sync Special	Enables loading of TM11 registers during I/O transfer to adapter
UNC	6	Unload Command	Command to formatter that rewinds tape and places drive off-line
UNPR	2	Unibus Non-processor Request	Buffered unibus nonprocessor request line
URCL	9	Unibus Register Clock Lower Byte	Loads the lower byte of the TM11 data register for either DMA transfer or I/O transfers
URCU	9	Unibus Register Clock Upper Byte	Loads the upper byte of the TM11 data register for either DMA transfers or I/O transfers
URFL	9	Unibus Register Full	Indicates that the unibus data register is ready for DMA transfer (Read Only)
URLC	9	Unibus Register Load Control	Used to count the load of two bytes of data to the unibus data register for DMA word transfers (Read Only)
URLD	9	Unibus Register Load	Controls the loading of the unibus data register with data for DMA transfer (Read Only)

MNEMONIC	ORIGIN	TERM	COMMENTS
USCK	2	Unibus Selection Acknowledge	Buffered unibus "SACK" line
USLØ-2	6	Unit Select Ø-2	TM11 control register unit select bits (most significant bit is formatter select)
USOK	4	Unit Select OK	Inhibits the detection of rewind completion until several microseconds after selection of new drive
USS	2	Unibus Slave Sync	Buffered unibus "SSYN" line
USSN		Unibus Slave Sync	Slave sync to unibus during I/O operation
WCC	10	Word Count	Carry from byte count register that causes termination of DMA transfers or record spacing
WCZ	9	Word Count Zero	Indicates when byte count register has reached zero terminating DMA transfers or spacing operation
WDP	12	Write Data Parity	Write data parity to formatter
WFM	6	Write File Mark	Control to formatter instructing it to write a file mark on tape
WRT	6	Write Mode	Control to formatter indicating that operation is writing on tape
WRTR	14	Write Ready	"WRT" gated with "CUR" for controlling multiplex of data into unibus data register
WST	13	Write Strobe	Buffered raw write strobe from formatter
WSTD	14	Write Strobe Detect	Used to store write strobe until resynchronized with "CLK"

MNEMONIC	ORIGIN	TERM	COMMENTS
WSTR	12	Write Strobe	Write strobe synchronized with "CLK" for controlling FIFO unload control
XFR	5	Transfer	Indicates the completion of a DMA transfer
XFRG	9	Transfer Gated	Indicates completion of DMA transfer and removal of "XFR" signal
XFRS	9	Transfer Stored	Used to remember "XFR" until "UAUP" is set
10K	15	10KC Clock	Used as "10KC" if crystal frequency is 2.56 MHz
10KC	15	10KC Clock	10KC clock for TM11 TU10 register bit 15



STREAMER TAPE ADAPTER · SIMPLIFIED BLOCK DIAGRAM

NOTES

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STANDARD DOCUMENTATION PACKAGE

MODEL TC-30 TAPE ADAPTER

Part No. P91000935

* * *

This package contains:

Hardware Manual, Publication Number 91000943

Logic Manual, Publication Number 91000950

Diagnostic Manual, Publication Number 91000448

CAUTION:

PLEASE REFER TO THE INSTALLATION SECTION OF THE HARDWARE MANUAL BEFORE INSTALLING THE SYSTEM.

Rev/ Suppl. Date _____ Production Run Date 10-31-83

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Before signing for your shipment which has arrived, use the delivery receipt to check off each package, accounting for all packages listed. Inspect the shipping containers immediately for evidence of mishandling during transit and note the damage on all copies of the delivery receipt before signing it. If a container is damaged, request that the carrier's agent be present when the package is opened.

Compare the packing list attached to the shipping container against your purchase order to verify that the shipment is correct. Notify the department issuing the requisition and the Purchasing department that the shipment has arrived.

Unpack the shipping containers and inspect each item for external or concealed damage such as broken controls and connectors, dented corners, bent panels, scratches, loose or damaged components, damaged subassemblies, etc. If any damage is found while unpacking, notify your supplier and the delivering carrier immediately and request inspection.

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