Tape Dimension III
Tape Controller
User's Manual

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PREFACE

This User's Manual provides information necessary for the installation and operation of the Western Peripherals TAPE DIMENSION III Tape Adapter, used with the DEC PDP-11 and VAX-11 family of Unibus-equipped computer systems.

The manual is divided into the following sections:

Section I	General Description
Section II	Installation
Section III	Programming
Section IV	Computer Interface
Section V	Pertec-Compatible Formatter Interface
Section VI	STC & Telex Formatter Interfaces
Section VII	NRZI and PE Tape Formats
Section VIII	GCR Tape Format

RELATED DOCUMENTS

ANSI X3.22	American National Standard: Recorded Magnetic Tape for Information Interchange (800 CPI, NRZI)
ANSI X30.39-1973	American National Standard: Recorded Magnetic Tape for Information Interchange (1600 CPI, Phase Encoded)
ANSI X3.40-1973	American National Standard: Unrecorded Magnetic Tape for Information Interchange (9-track 200 and 800 CPI, NRZI; and 1600 CPI, PE)
ANSI X3.54-1976	American National Standard: Recorded Magnetic Tape for Information Interchange (6250 CPI, GCR)
DEC	Unibus Protocol
DEC EK-OTS11-UG-001	TS-11 Subsystem User's Guide

SECTION I

GENERAL DESCRIPTION

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SECTION I - GENERAL DESCRIPTION

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SECTION I

GENERAL DESCRIPTION

INTRODUCTION

The Western Peripherals TAPE DIMENSION III Tape Controller emulates Digital Equipment Corporation (DEC) Model TS-11 Tape Subsystems. This Group Code Recording tape controller/coupler, containing 64K bytes of on-board data buffering, is compatible with the DEC PDP-11 and VAX-11 family of computer systems. Contained on a single standard-sized hex-wide printed circuit board, the Tape Dimension-III interfaces with these processors via a standard Unibus slot.

The Tape Dimension III provides the interface for a tape subsystem using industry-compatible formatted start/stop drives with dual density (NRZI/PE) or tri-density capability tape drives, which includes the 6250 bit per inch (bpi) Group Code Recording (GCR) format. The on-board data buffer allows the TD-III to take advantage of bus speeds without concern for data late conditions, even at fast data rates on a highly populated peripheral bus, while remaining transparent to standard DEC software.

EMULATION - SOFTWARE COMPATIBILITY

The Tape Dimension III is compatible with DEC operating systems that can support TS-11 tape subsystems. The controller uses these standard TS-11 registers and vector to simplify the system interface, and since the controller is fully buffered, it is immune to data late conditions, even when operating with high speed disk drives. Alternate TS-11 register addresses and vectors are also available via simple switch selection.

HARDWARE COMPATIBILITY

The Tape Dimension III interfaces the DEC PDP-11 or VAX-11 system processor via the Unibus. The hex-wide TD-III board mounts inside the cabinet of the host computer and plugs directly into an available SPC slot in its Unibus.

TAPE UNIT OPERATION AND INTERFACE

The Tape Dimension III supports the industry-standard tape drive interface as well as the special interfaces and other requirements to run GCR and other formats on STC and Telex tape drives.

Standard 50-conductor "A" and "B" formatter interface cables are used to connect Pertec-compatible tape drives to the controller through two connectors at the top edge of the controller board. Two additional connectors are also available for the STC/Telex interface. Various drive types are supported, including drives operating in the PE, NRZI and/or GCR format. Contact your Western Peripherals representative or the Western Peripherals Marketing department for a list of drives which are compatible with the TD-III.

TAPE FORMATS

Group Code Recording (GCR) is featured by the TD-III, allowing the user to take advantage of this modern high density recording technology. All data and control characters are recorded in groups and subgroups. Data groups contain error correcting characters for high data reliability. Each tape block contains preamble and postamble groups as well as ending data, control, and CRC groups. Resynchronization groups are also provided if the data block is longer than 1112 bytes.

The controller also uses the standard nine track 1600 bit per inch (bpi) phase encoded and 800 bpi NRZI tape formats. In PE, each tape block contains a 41 character preamble of 40 tape characters with all-zero bits followed by one character of all-one bits. The preamble is followed by the data field which also contains an odd parity bit for each data character. Following the data field is the postamble, which is the mirror-image of the preamble.

Like PE, the data field of the NRZI format contains an odd parity bit for each data character. Following the data field are the Cyclic Redundancy Check (CRC) and Longitudinal Redundancy Check (LRC) characters to ensure data integrity.

DATA BLOCK SIZE

Although the recommended maximum is 2K to 4K, the maximum data block size is only limited by the Byte/Record Count word to a full 64K byte block. While the controller can handle a single-byte tape block, the minimum recommended data block size can vary from system to system where the generated tapes will be used.

SPECIFICATIONS

COMPUTER INTERFACE - SOFTWARE

PDP-11 Interface Protocol -

DEC TS-11

Emulation -

One DEC TS-11 subsystem

Unibus Register Addressing Assignments -

Standard = 772520_8, 772522_8 (TSDB/TSBA, TSSR)

Optional= 770000_8-777760_8 (TSDB/TSBA register, in modulo 40_8 increments, via option switches).

Unibus Interrupt Vector -

Standard = 224 (octal)

Optional = 0 - 377 (via option switches).

PDP-11 Bus Level -

Bus level 4, 5, 6, or 7; (level 5 is standard).

COMPUTER INTERFACE - HARDWARE

Unibus interface -

(fits in a standard Unibus SPC slot).

Bus Loading -

One standard Unibus load.

DMA Addressing -

18 bits

Buffering -

64 Kbytes (read and write)

DMA Unibus Transfer Time (bus efficiency) -

Averages 1 us/word Read and Write (BBSY time).

TAPE DRIVE INTERFACE

Formatter Interface (Start-Stop or Streaming operation) -

Pertec-compatible NRZI/PE/GCR Formatter (Pertec, CDC, Kennedy, Cipher, Ampex, etc.) or STC/Telex-compatible formatter.

Formatted Tape Drive Protocol -

Industry (Pertec) Standard for formatted drive. STC/Telex drives have a different interface, described later.)

Number Of Drives -

One tape drive

Tape Interface Cabling -

Two 50 cond. 3M-type ribbon cables (Pertec-compatible)

Two 60 conductor 3M-type ribbon cables (STC/Telex)

Telex drives require a special cable adapter board

Recording Formats -

6250 BPI per ANSI X3.54
1600 BPI per ANSI X3.39
800 BPI per ANSI X3.22

Tape Transfer Rate -

Over 1 mb/sec. with single-record buffering.

SELF-TEST FEATURE

Provides a full basic test of controller's internal processor and storage to assure reliable operation every time power is applied to the system.

SIZE One Standard PDP-11 Hex-wide PC Board

POWER +5 volts (5% tolerance) @ 7.0 amps power consumption (maximum).

ENVIRONMENT

Operating temperature	0 to 55 degrees Celsius
Storage temperature	-10 to 70 degrees Celsius
Relative humidity	10% to 90% (without condensation)

SECTION II

INSTALLATION

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SECTION II - INSTALLATION

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SECTION II

INSTALLATION

INTRODUCTION

This section provides information required to configure and install the Western Peripherals TAPE DIMENSION III Magnetic Tape Controller in a DEC VAX/PDP-11 computer system. The TD-III consists of one standard hex-wide printed circuit board which plugs into a standard SPC backplane in the computer mainframe or expansion chassis. One cable set is provided for interconnecting the controller to the drive's formatter. (An adapter is provided to interface the Telex formatter.) An optional diagnostic tape is available (P/N P68000280) and a A User's Manual is included with each controller.

The installation information in this section applies to standard TAPE DIMENSION III assembly number P60001450, Revision 'X' or 'A'. If your board has a different part number, contact Western Peripherals for information concerning the proper installation of your controller board.

UNPACKING AND INSPECTION

After removal of the controller board and associated components from the shipping container, visually inspect them for physical damage. Check off each item on the enclosed packing list. In case of damage, retain all packaging material and notify the carrier to make a report. Always ensure all minor parts and small items are accounted for before discarding any shipping material.

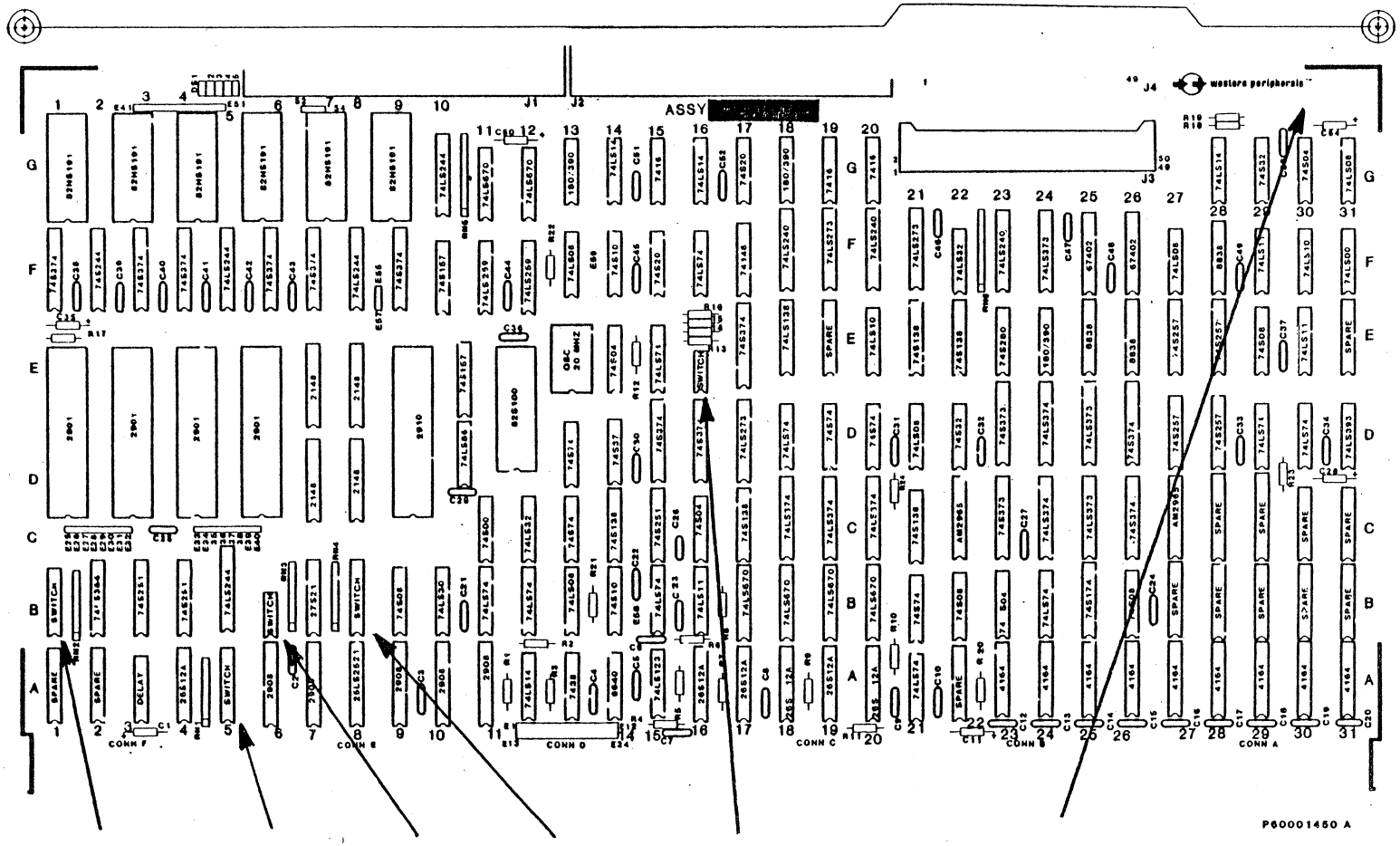
PREPARATION

Determine the position in the computer where the controller is to be installed. Remember that its physical location in the system determines its bus priority within the specified bus level. You may subsequently want to adjust the position of the devices on the bus to take advantage of the priority structure of the bus to minimize or eliminate bus grant late errors in the other various devices in the system. The TD-III remains immune to data late errors.

Refer to the appropriate tape drive manual to install the tape drive. The drive must be prepared and the processor checked out before the controller can be expected to operate properly.

Figure 2-1 Tape Dimension III Board Illustration

Assembly Number P60001450 Layout



BOARD REV. I.D. -

P76001296
PWM-X/PWB-X = BOARD REV. 'X'

P76001296
PWM-A/PWB-A = BOARD REV. 'A'

CONFIGURATION SELECTIONS

Unibus Address Selection

Unibus address bits 4 through 11 for the controller registers are switch selectable. These bits are controlled by switch toggles 1 through 8 of the switch module at location 8B on the controller board. Placing a switch toggle in the ON position selects a binary 0 while placing it in the OFF position, selects a binary 1 in its respective bit position.

The switch settings required to set up the standard Unibus addresses (772520 and 772522) are illustrated in Table 2-1. The switches are arranged differently for board revisions 'X' and 'A', so check your board revision (upper right-hand corner of board). The table has instructions for both versions.

OCTAL	7			7			2			5			2			0-2		
BIT	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BINARY	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	X	0
SWITCH # REV. A	FIXED VALUES						5	4	6	3	7	2	8	1	UNIT SELECT **	*		
SWITCH # REV. X							1	8	2	7	3	6	4	5				
"ON"							X		X		X		X					
"OFF"								X		X		X		X				

* Register-determined Values ** See Table 2-5

Table 2-1 Standard Unibus Address Selection (8B)

Vector Address Selection

The interrupt vector address for the drive is selected by positioning the switch toggles of the switch module at location 1B on the controller board. Switch toggles 1 through 6 control bits 02 through 07. (Bits 00 & 01 are allways 0) Placing a switch toggle in the ON position selects a binary 1 while placing it in the OFF position selects a binary 0 in its respective bit position.

The switch settings required to set up the standard drive interrupt vector address (224) are illustrated in Table 2-2.

OCTAL	2		2			4		
BINARY	1	0	0	1	0	1	0	0
SWITCH #	6	3	2	1	4	5		
ON	X			X		X		
OFF		X	X		X			

Table 2-2 Standard Interrupt Vector Selection (1B)

Bus Level Selection

By placement of jumpers in accordance with Table 2-3, any of bus levels 4, 5, 6 or 7 can be selected. Level 5 is standard. These jumpers are located at the bottom of the board near Connector D.

JUMPER CONNECTIONS	BUS LEVEL			
	4	5	6	7
E01-E13	**INSTALL**	REMOVE	REMOVE	REMOVE
E02-E14	**INSTALL**	REMOVE	REMOVE	REMOVE
E03-E15	REMOVE	**INSTALL**	REMOVE	REMOVE
E04-E16	REMOVE	**INSTALL**	REMOVE	REMOVE
E05-E17	REMOVE	REMOVE	**INSTALL**	REMOVE
E06-E18	REMOVE	REMOVE	**INSTALL**	REMOVE
E07-E19	REMOVE	REMOVE	REMOVE	**INSTALL**
E08-E20	REMOVE	REMOVE	REMOVE	**INSTALL**
E09-E21	**INSTALL**	REMOVE	REMOVE	REMOVE
E10-E22	REMOVE	**INSTALL**	REMOVE	REMOVE
E11-E23	REMOVE	REMOVE	**INSTALL**	REMOVE
E12-E24	REMOVE	REMOVE	REMOVE	**INSTALL**
E13-E14	REMOVE	**INSTALL**	**INSTALL**	**INSTALL**
E15-E16	**INSTALL**	REMOVE	**INSTALL**	**INSTALL**
E17-E18	**INSTALL**	**INSTALL**	REMOVE	**INSTALL**
E19-E20	**INSTALL**	**INSTALL**	**INSTALL**	REMOVE

Table 2-3 Bus level Selection

Drive-Type Switch Settings

The switch module on the controller at location 16E must be set according to the type of drive connected to the controller and the mode of operation. Table 2-4 identifies the correct switch settings for each drive-type.

	Switch Pack 16E Switch Toggle Number:			
Drive/Interface Type:	1	2	3	4
STC Drive	On	Off	Off	Off
Telex Drive	On	On	Off	Off
Pertec-type Start/Stop Drive	Off	Off	Off	On
Pertec-type Streaming Drive	Off	Off	Off	Off

Table 2-4 Drive-Type Switch Settings (16E)

Multiple Subsystems

When more than one TS-11 subsystem must be installed in the computer system, the TD-III can be addressed as UNIT-0, UNIT-1, UNIT-2, or UNIT-3 by switch settings, via a 4 position switch labeled 6B. See Table 2-5; (only one unit may be selected).

	Switch Pack 6B Switch Position:			
Unit #	4	3	2	1
0	ON	OFF	OFF	OFF
1	OFF	ON	OFF	OFF
2	OFF	OFF	ON	OFF
3	OFF	OFF	OFF	ON

Table 2-5 Unit Select (6B)

TAPE DIMENSION III BOARD INSTALLATION

The DMA Non-Processor Grant and Bus Grant lines are daisy-chained from one backplane connector to the next. To maintain continuity, unused backplane connector slots are usually jumpered with a jumper card and/or a jumper wire.

The Bus Grant jumper card is installed in the D connector of unused slots. Western Peripherals supplies part number P01310093 for this purpose. The DMA Non-Processor Grant jumper is connected between pins A1 and B1 on the backside of the "C" connectors of unused slots.

Any open slots between the controller and the processor must have these jumpers installed. Be sure to check for (by continuity test) and remove the DMA Non-Processor Grant jumper wire from the backplane connector of the slot selected for controller installation.

Place the controller board into the selected slot in the backplane, being careful to insure that it seats properly. Check that the computer Unibus is properly terminated.

INTERCONNECTIONS

Connections between the TD-III and the formatter are completed via two cables supplied with the controller. When connecting the cables, be sure pin 1 (the triangle or arrow) on each plug is oriented to the triangle on the socket. You should check the manual for the tape drive to ensure proper connection at the drive.

For the Pertec-compatible formatter interface, these cables plug into 50-pin socket connector J3 and 50-pin edge connector J4 on the controller board. The pin assignments for these two connectors are listed in Tables 2-6 and 2-7. When connecting the cable to J3, be sure pin 1 (the triangle or arrow) on the plug is oriented to the triangle on the socket. When connecting the cable to edge-connector J4, be sure the red stripe on the cable is oriented to pin 1 (printed on the board next to the connector).

For an STC or Telex formatter interface, the ribbon cables plug into two 60-pin socket connectors, J1 and J2 on the controller board. The pin assignments for the two connectors J1 and J2 on the controller are listed in Tables 2-8 and 2-9. These tables also list the the pin assignments for the Telex formatter I/O connectors.

For an STC drive, the cable from J1 connects to connector B4 on the drive and the cable from J2 connects to connector A4 on the drive.

Telex Adapter Installation Instructions

For a Telex formatter interface, a Telex/TD-III Cable Adapter (assembly P60001245) is also supplied. The ribbon cables from J1 and J2 on the TD-III plug into two 60-pin connectors on the Cable Adapter assembly and the connectors of the three 50-pin cables coming from the Cable Adapter assembly plug into three I/O connectors at the Telex formatter.

Installation of the Telex cable adapter is not difficult if you follow these simple steps. Be sure that the stripe on the cable and the arrow on the plugs match the pin 1 arrow on the board connectors. The cables to the Telex electronics are self-orienting and cannot be connected backwards.

1. Open the back door of the tape drive unit.

2. Mount the Telex Adapter Board on the cabinet rails using the hardware provided.

3. Connect the cables:

TAPE DIMENSION III	TELEX CABLE ADAPTER BOARD
CABLE P1	CONNECTOR J1
CABLE P2	CONNECTOR J2

TELEX CABLE ADAPTER BOARD	TELEX DRIVE ELECTRONICS
CABLE P101	CONNECTOR I.O.-1
CABLE P102	CONNECTOR I.O.-2
CABLE P103	CONNECTOR I.O.-3

Table 2-6 Pin Assignments for Pertec-compatible Formatter Interface (Connector J3)

Signal Pin	Ground Pin	TD-III Mnemonic	Formatter Mnemonic
2	1	FBSY	FBY
4	2	LBYT	LWD
6	5	WRD03	W4
8	7	CMDCLK	GO
10	9	WRD07	W0
12	11	WRD06	W1
18	17	CMD1	REV
20	19	REW	REW
22	21	WRDP	WP
24	23	WRD00	W7
26	25	WRD04	W3
27	26	WRD01	W6
30	29	WRD05	W2
32	31	WRD02	W5
34	33	CMD2	WRT
36	35	DS0	LGP
38	37	DS1	EDIT
40	39	CMD4	ERASE
42	41	CMD3	WFM
46	45	TA0	TAD0
48	47	RD05	R2
50	49	RD04	R3

NOTE: All interface signals are low-true.

Table 2-7 Pin Assignments for Pertec-compatible Formatter Interface (Connector J4)

Signal Pin	Ground Pin	TD-III Mnemonic	Formatter Mnemonic
1	5	DP	RP
2	5	RD07	R0
3	5	RD06	R1
4	5	LP	LDP
6	5	RD03	R4
8	7	RD00	R7
10	9	RD01	R6
12	11	ERR	HER
14	13	FM	FMK
16	15	IDB	IDENT
18	17	FEN	FEN
20	19	RD02	R5
22	21	EOT	EOT
24	23	ESC1	UNL
28	27	RDY	RDY
30	29	RW	RWD
32	31	FP	FPT
34	33	RSTR	RSTR
36	35	WSTR	WSTR
38	37	DBSY	DBY
40	39	ER1	SPD
42	41	CERR	CER
44	43	ONL	ONL
46	45	TA1	TAD1
48	47	TA2	TAD2
50	49	CMD0	HISP

NOTE: All interface signals are low-true.

Table 2-8 Pin Assignments for STC/Telex Interface (Connector J1)

TD-III CONNECTOR J1				TELEX I/O CONNECTORS		
SIGNAL PIN	GROUND PIN	TD-III MNEMONIC	STC MNEMONIC	TELEX MNEMONIC	TELEX ADAPTER	TELEX CONNECTOR
A1	B1	-	-	-	-	-
A2	B2	ER0	ERMX-0	ERROR 0	PIO3-3	IO3-2
A3	B3	ER1	ERMX-1	ERROR 1	PIO3-5	IO3-3
A4	B4	ER2	ERMX-2	ERROR 2	PIO3-7	IO3-4
A5	B5	ER3	ERMX-3	ERROR 3	PIO3-9	IO3-5
A6	B6	ER4	ERMX-4	ERROR 4	PIO3-11	IO3-6
A7	B7	ER5	ERMX-5	ERROR 5	PIO3-13	IO3-7
A8	B8	ER6	ERMX-6	ERROR 6	PIO3-15	IO3-8
A9	B9	ER7	ERMX-7	ERROR 7	PIO3-17	IO3-9
A10	B10	FBSY	BUSY	BSY	PIO1-23	IO1-12
A11	B11	DREQ	TREQ	DRQ	PIO2-23	IO2-12
A12	B12	-	-	-	-	-
A13	B13	IDB	ID BURST	IDS	PIO2-37	IO2-19
A14	B14	OPI	OPINC	REV	PIO1-41	IO1-21
A15	B15	DBSY	ENDATP	DBZ	PIO2-21	IO2-11
A16	B16	FMT	TMS	FMK	PIO2-43	IO2-22
A17	B17	RJS	REJECT	REJ	PIO1-27	IO1-14
A18	B18	OVR	OVRNS	OVR	PIO2-31	IO2-16
A19	B19	EM	DATA CHK	EM	PIO1-49	IO1-25
A20	B20	RPE	ROMPS	RPE	PIO1-39	IO1-20
A21	B21	CERR	CRERR	COR	PIO2-35	IO2-18
A22	B22	BLK	BLOCK	IBEN	PIO2-19	IO2-10
A23	B23	DD0	NRZI	DDS0	PIO2-39	IO2-20
A24	B24	DPE	BUPER	DPE	PIO2-47	IO2-24
A25	B25	ONL	ONLS	ONL	PIO1-33	IO1-17
A26	B26	DD1	HDENS	DDS1	PIO2-41	IO2-21
A27	B27	RDY	RDYS	RDY	PIO1-35	IO1-18
A28	B28	-	-	-	-	-
A29	B29	CMD0	-	CMD0	PIO1-7	IO1-4
A30	B30	TA2	-	TA2	PIO1-5	IO1-3

NOTE: All interface signals are low-true.

Table 2-9 Pin Assignments for STC/Telex Interface (Connector J2)

TD-III CONNECTOR J2				TELEX I/O CONNECTORS		
SIGNAL PIN	GROUND PIN	TD-III MNEMONIC	STC MNEMONIC	TELEX MNEMONIC	TELEX ADAPTER	TELEX CONNECTOR
A1	B1	TA0	AD0	TA0	PIO1-1	IO1-1
A2	B2	TA1	AD1	TA1	PIO1-3	IO1-2
A3	B3	CMD1	CMD0	CMD1	PIO1-9	IO1-5
A4	B4	CMD2	CMD1	CMD2	PIO1-11	IO1-6
A5	B5	CMD3	CMD2	CMD3	PIO1-13	IO1-7
A6	B6	CMD4	CMD3	CMD4	PIO1-15	IO1-8
A7	B7	DS0	DS0	-	GROUND	IO1-9
A8	B8	CMDCLK	START	CMD.CLK	PIO1-25	IO1-13
A9	B9	LBYT	STOP	LBY	PIO2-27	IO2-14
A10	B10	DACK	TRAK	DAK	PIO2-25	IO2-13
A11	B11	WRDP	DATA-P	DP	PIO2-17	IO2-9
A12	B12	WRD07	DATA-0	D0	PIO2-1	IO2-1
A13	B13	WRD06	DATA-1	D1	PIO2-3	IO2-2
A14	B14	WRD05	DATA-2	D2	PIO2-5	IO2-3
A15	B15	WRD04	DATA-3	D3	PIO2-7	IO2-4
A16	B16	WRD03	DATA-4	D4	PIO2-9	IO2-5
A17	B17	WRD02	DATA-5	D5	PIO2-11	IO2-6
A18	B18	WRD01	DATA-6	D6	PIO2-13	IO2-7
A19	B19	WRD00	DATA-7	D7	PIO2-15	IO2-8
A20	B20	SRST	RESET	SYSRST	PIO2-45	IO2-23
A21	B21	ESC1	SLX1	ESC1	PIO3-21	IO3-11
A22	B22	ESC0	SLX0	ESC0	PIO3-19	IO3-10
A23	B23	DS1	DS1	DS1	GROUND	IO1-10
A24	B24	ESC2	SLX2	-	-	-
A25	B25	ERR	SSC	ERR	PIO2-33	IO2-17
A26	B26	OSC	OSC	OB	PIO2-49	IO2-25
A27	B27	EOT	EOTS	EOT	PIO1-31	IO1-16
A28	B28	LP	BOTS	BOT	PIO1-29	IO1-15
A29	B29	FP	FPTS	FPT	PIO1-37	IO1-19
A30	B30	RW0	REWS	RWG	PIO1-47	IO1-24

NOTE: All interface signals are low-true.

SELF-TEST

The TAPE DIMENSION III uses its internal self-test firmware to verify the controller every time power is applied to the system. If no problem is detected, the LED indicators on the top edge of the board will be OFF. Table 2-10 lists other indications which define specific failures.

LED NUMBER: 5	4	3	2	1	HEX	TEST RESULT
OFF	OFF	OFF	OFF	OFF	0	Self Test OK
OFF	OFF	OFF	OFF	ON	1	Sequencer Failure
OFF	OFF	OFF	ON	OFF	2	ALU Test Condition Failure
OFF	OFF	OFF	ON	ON	3	DBUS Test Condition Failure
OFF	OFF	ON	OFF	OFF	4	Static Memory Failure
OFF	OFF	ON	ON	OFF	6	ALU Address Failure
OFF	OFF	ON	ON	ON	7	FIFO Failure
ON	X	X	X	X		Dynamic Memory Failure (See Table 2-11)

Table 2-10 Self-Test Indications

LED NUMBER: 5	4	3	2	1	HEX	LOCATION
ON	OFF	OFF	OFF	OFF	10	30A
ON	OFF	OFF	OFF	ON	11	29A
ON	OFF	OFF	ON	OFF	12	28A
ON	OFF	OFF	ON	ON	13	27A
ON	OFF	ON	OFF	OFF	14	26A
ON	OFF	ON	OFF	ON	15	25A
ON	OFF	ON	ON	OFF	16	24A
ON	OFF	ON	ON	ON	17	23A

Table 2-11 Failing Memory Chip Look-Up Table

CHECKOUT

With your tape system installed, you may now power-up the system and test the installation. To check the controller installation and the connection of the cables to the drive, examine the Control/Status Register of the controller. The Off-Line status bit (bit 6) should change when the drive is placed on-line.

You may then run the ZTSHC0 test program contained in the diagnostic tape supplied with the controller. An operational test should also be performed, such as performing a tape back-up from disk.

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SECTION III

PROGRAMMING

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SECTION III - PROGRAMMING

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SECTION III

PROGRAMMING

INTRODUCTION

This section contains machine-level programming reference information which describes the registers of the TAPE DIMENSION III. Also contained in this section is information on the operation of the controller including register transfers, packet transfers, data transfers, and interrupts.

GENERAL

Communication between the PDP-11 program and the controller involves program-addressable registers in the controller and various classes of buffer space in PDP-11 main memory.

Two switch-selectable register addresses are assigned to the controller. The first address is shared by the write-only TSDB register and the read-only TSBA register. The second address is assigned to the read/write TSSR register.

To implement any transport command, two packet buffers in PDP-11 memory must be assigned to that transport. These packet buffers include the Command Packet Buffer in which the PDP-11 program writes command information and the Message Buffer in which the controller writes transport status information.

After writing a command packet in a command buffer, the PDP-11 program then writes the command buffer address in the TSDB register associated with the transport to which the command is addressed. This causes the controller to read the command packet and, if possible, execute the command. Upon completion or rejection of the command, the controller writes the appropriate transport status information in the TSSR register and in the message packet buffer. If the interrupt-enable bit is set in the command packet, it also interrupts the PDP-11 program to inform it of the ending status.

A separate command, the Set Characteristics command, points to a characteristics data buffer in PDP-11 main memory. The PDP-11 program writes the address and length of the message buffer to be assigned to the transport in the characteristics data buffer and also writes a characteristics mode byte. The write characteristics command causes the controller to access the characteristics data buffer and obtain this information. Once a

message buffer address has been obtained, the message buffer continues to be assigned to the transport until initialization occurs. Since a message packet buffer is required to complete each command transaction, it follows that the first command to a transport following initialization must be a write Characteristics command.

The controller uses non-processor direct memory accesses to obtain information from the command buffer and the characteristics data buffer and to write status information in the message buffer. During a tape read or write operation, the controller uses non-processor direct memory transfers to access a tape data buffer in PDP-11 memory.

The TSBA register holds the 16 least significant bits of the PDP-11 memory address for each direct memory access. The two most significant bits of the PDP-11 memory address are held in the TSSR register.

The two least significant bits of each command packet buffer address are always 0s. Thus, the PDP-11 can specify the command packet buffer address by means of a single 16-bit transfer to the TSDB register. Bits 0 and 1 of the word transferred to the TSDB are the two most significant bits of the command packet buffer address. Bits 2 through 15 represent bits 2 through 15 of the command packet buffer address.

In addition to holding the two most significant bits of PDP-11 memory addresses, the TSSR register hold 13 bits of transport status. Although the TSSR register is defined as a read/write register, a DATO operation addressed to the TSSR register has the effect of resetting five of the status bits held in it rather than transferring information to it. Such an operation also results in transport initialization during which a load sequence returns the tape to the BOT position if the transport is on line.

PACKET BUFFER PROTOCOL

There is a specific protocol for accessing packet buffers and this protocol is defined in terms of buffer ownership. In general, ownership of both buffers belongs to the PDP-11 program at the time that a command transaction begins and passes to the controller when the PDP-11 program writes the command packet buffer address in the TSDB register with the Acknowledge bit set in the Command Packet header word. Ownership of the two buffers then passes back to the PDP-11 program after the command has been completed when the controller updates status and (if the Interrupt-Enable bit in the command packet is set) interrupts the PDP-11 program.

Since only the current owner is allowed to access a buffer, the controller cannot report a change of status occurring during an idle period after it has returned ownership to the PDP-11

program. If a change between on-line and off-line status occurs when the controller does not own the message buffer, it waits until the next command is received. This gives it the message buffer ownership required to update the message buffer so as to reflect the change in status. In this case, it does not accept ownership of the command buffer. If the attention-interrupt bit was set in the characteristics mode byte obtained during the most recent write-characteristics command transaction, then an attention interrupt occurs following the status update. This interrupt is independent of the state of the interrupt-enable bit of the command which returns message buffer ownership to the controller allowing the status update.

Because the controller has not accepted command buffer ownership, the transaction (which would normally have resulted in the processing of a command) in this case has resulted only in the reporting of a change in on-line/off-line status. If the command is still appropriate after this status change, the PDP-11 must restart the transaction by writing the command buffer address in the TSDB register in order to obtain command execution.

There is a message-buffer-release command whose only purpose is to leave ownership of the message buffer to the controller so that a subsequent change of on-line/off-line status can be reported immediately under transport-idle conditions. The controller updates the TSSR but not the message buffer during the message-buffer-release command transaction. If the release-interrupt-enable bit was set in the characteristics mode byte obtained during the most recent write-characteristics command transaction, then an interrupt is generated at the end of the message-buffer-release command transaction. This occurs independently of the state of the interrupt-enable bit of the message-buffer-release command.

If a change of on-line/off-line status occurs following the execution of the message-buffer-release command, then the message buffer is updated immediately to report this change of status. This update returns ownership of the message buffer to the PDP-11 program. If the attention-interrupt-enable bit was set in the characteristics mode byte obtained during the most recent write-characteristics command transaction, then an interrupt is generated at the time of the message buffer update. (This interrupt is also independent of the state of the interrupt-enable bit of the message-buffer-release command.)

PDP-11 PROGRAM-CONTROLLED INPUT/OUTPUT OPERATIONS

Two consecutive word addresses are assigned to the transport interfacing with the controller. The address assignments are established by setting toggle switches on the controller board. Standard addresses are as follows:

Unit #	Registers	Address (Octal)
1	TSDB/TSBA	772520
	TSSR	772522
2	TSDB/TSBA	772524
	TSSR	772526
3	TSDB/TSBA	772530
	TSSR	772532
4	TSDB/TSBA	772534
	TSSR	772536

Table 3-1 summarizes the PDP-11 program-controlled input and output transfer operations associated with each register.

The format of the TSDB and TSBA register is defined in the description of the input and output operations. The format of the TSSR is summarized in Table 3-2.

Table 3-1
PDP-11 Program-Controlled Input/Output Operations

Transfer Class and Register	Description
DATO, TSDB	Sixteen bits of command buffer address information from Unibus are accepted by the controller. Bits 15 through 02 from Unibus are stored in corresponding bit positions of TSBA and bits 01 and 00 from Unibus (MSBs of command buffer address) are stored in bit positions 09 and 08 of TSSR. SSR bit in TSSR is reset. Controller fetches command information from buffer and processes command without further program intervention if the ACK bit is set.
DATOB, TSDB, Upper Byte	Upper byte from Unibus is loaded into both bytes of TSBA and bits 09 and 08 from Unibus are loaded into corresponding bit positions in TSSR. Used to test integrity of controller Unibus addressing function for transport n. After this operation, DATO to TSSR must be performed to provide necessary initialization before command for transport n can be accepted.
DATOB, TSDB, Lower Byte	Lower byte from Unibus is loaded into lower byte of TSBA and lower byte of TSSR. Used for diagnostic purposes. After this operation, DATO to TSSR must be performed to provide necessary initialization before command for transport n can be accepted.
DATI, TSBA	Sixteen least significant bits of current Unibus address pointer for transport n are placed on Unibus.
DATO or DATOB, TSSR	SPE, UPE, RMR, NXM, and SSR bits of TSSR are reset. Any transport n operation currently in progress is aborted. If transport n is on-line, a rewind-to-loadpoint operation is executed. SSR bit of TSSR is then set to indicate that transport n is ready to accept a command.
DATI TSSR	Contents of TSSR are placed on Unibus.

Table 3-2 TSSR Format

Bit(s)	Mnemonic	Meaning When Set
15	SC	A special condition was detected during execution of last command. More information is contained in the termination class code (bits 04-01)
14	UPE	Unibus parity error
13	SPE	Not used by the controller. Always 0.
12	RMR	Register modification refused. The PDP-11 program has loaded a command packet address into the TSDB when SSR (bit 07) is reset. This can occur if the last command was a message buffer release command and the controller is updating the message buffer to report a change in on-line/off-line status at the time that the PDP-11 program loads the TSDB.
11	NXM	The controller has attempted to access a non-existent memory location. The attempted access may involve a command, message, or data buffer.
10	NBA	The controller needs a message buffer address. A write characteristics command has not been executed since the last TSSR initialization.
09, 08	A17, A16	Bits 17 and 16 of the Unibus address for non-processor direct memory access
07	SSR	The transport is not busy and another command addressed to it can be accepted.
06	OFL	The transport is off line.
05, 04	FC1, FC0	Fatal termination class code. Not supported.
03-01	TC2-TC0	Termination class code. See Table 3-3.
00		Not used.

Table 3-3 Termination Class Codes

Code Value TC2,1,0	Class	Description
0 0 0	Normal	No special condition detected.
0 0 1	Attention	Transport has gone off line or come on line.
0 1 0	Tape Status Alert	Tape status having program significance detected. Further information in TMK, RLS, RLL, EOT, or BOT bit of XSTAT0 word of message packet.
0 1 1	Function Reject	Command has been rejected. Further information in VCK, BOT, WLE, LLC, or ILA bit of XSTAT0 word of message packet or in OFL bit of TSSR.
1 0 0	Recoverable error, tape moved	An uncorrected error has been detected, and tape has moved one record position. Recommended procedure is to log error and issue retry command.
1 0 1	Recoverable error, tape not moved	Not used by the controller.
1 1 0	Unrecoverable error	Tape position has been lost. No valid recovery procedure is available.
1 1 1	Fatal error	Not used by the controller.

COMMAND PACKET

Figure 3-1 illustrates command packet formats. Every packet contains a command packet header word. For some commands, additional information is required. Packets for commands which require access to a data buffer in main memory have two address words and a count word. The first address word contains the 16 least significant bits of the address. The second address contains the two most significant address bits, right justified. The count word specifies the data buffer length in positive byte count format. Packets for position commands contain a count word which specifies the number of records or file marks to be spaced over. For other commands, the header word contains all the required information.

Table 3-4 summarizes the information contained in the command packet header word. Two fields of the header word, the command mode field and the command code field, specify the operation to be performed. The decoding of these fields is summarized in Table 3-5.

HEADER WORD																
A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	*
0	0	0	0	0	0	0	0	0	0	0	0	0	0	A17	A16	*
COUNT WORD																

* Address Words

A. Read, Write, Write Characteristics Command Packet Format

HEADER WORD
COUNT WORD

B. Position Command Packet Format

HEADER WORD
NOT USED

C. Control or Format Command Packet Format

Figure 3-1 Command Packet Formats

Table 3-4 Command Packet Header Word Format

Bit(s)	Mnemonic/ Name	Meaning When Set
15	ACK	Indicates the PDP-11 program has read message buffer. Is normally set for all commands except those occurring when the controller owns message buffer due to execution of a message-buffer-release command.
14-12	Device-Depend. Field	(Individual bits described below)
14	CVC	Clears volume check bit of XSTAT0 word.
13	OPP	Alters read retry commands so that the read occurs in the opposite direction (Reread previous record is executed by reading in reverse and then spacing forward. Reread next record is executed by reading forward and then backspacing.)
12	SWB	When this bit is reset, the order of data buffer byte addresses is the same as the order in which the characters appear on tape with the character associated with the lowest byte address being closest to the BOT. Setting this bit swaps the positions of the two bytes of each word so that the upper byte appears closer to the BOT on the tape. (See paragraph: "TAPE DATA BUFFERS")
11-8	Command Mode	In conjunction with command code (bits 4-0) these bits specify the operation to be performed as summarized in Table 3-5.
7-5	Packet Format:	(Individual bits described below)
7	IE	Interrupt enable
6,5	-	These bits always have value 00, specifying one word header.
4-0	Command Code	In conjunction with command note bits (11-8), these bits specify the operation to be performed as summarized in Table 3-5.

Table 3-5 Command Summary

Command Code Value	Command	Command Mode Value	Operation
00001	Read	0000	Read one record forward.
		0001	Read one record reverse.
		0010	Reread previous record (backspace over record and then read forward).
		0011	Reread next record (Space forward one record and then read reverse).
00100	Write characteristics	0000	Get message buffer address and characteristics byte from characteristics data buffer.
00101	Write	0000	Write one data record.
		0010	Retry to write one data record (Backspace over record and the erase and write record).
00110	Write Subsystem Memory	0000	Not supported.
01000	Position	0000	Space forward n records, where n is specified by count word.
		0001	Space reverse n records, where n is specified by count word.
		0010	Skip n tape marks forward, where n is specified by count word.
		0011	Space reverse n tape marks, where n is specified by count word.
		0100	Rewind tape to loadpoint.
01001	Format	0000	Write tape mark.
		0001	Erase forward 3 inches of tape.
		0010	Retry to write tape mark (Space reverse, erase, and write tape mark).
01010	Control	0000	This constitutes a message buffer release command. It leaves ownership of the message buffer with the controller so as to allow immediate reporting of transport on-line/off-line status change.
		0001	Rewind tape completely onto supply reel (unload).
		0010	Clean tape (not supported).
01111	Get status immediate	0000	Update message buffer.

CHARACTERISTICS DATA BUFFER

The information contained in the characteristics data buffer includes the message buffer address and the characteristics mode byte. The location and length of the characteristics data buffer are specified in the address and count words of the write characteristics command packet. The controlleruses non-processor direct memory accesses to obtain the information from the characteristics data buffer.

Figure 3-2 illustrates the characteristics data buffer format. Table 3-6 summarizes the information contained in the characteristics mode byte.

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	A17	A16	*
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	**
CHARACTERISTICS MODE BYTE																

* Message Buffer Address
** Message Buffer Length

Figure 3-2 Characteristics Data Buffer

TAPE DATA BUFFERS

Data to be written on tape or data read from tape is stored in a data buffer in PDP-11 main memory. This buffer is specified by the address and count words of the write or read command packet. Data transfers between the data buffer and the controller are implemented by means of non-processor direct memory accesses.

Figure 3-3A illustrates the standard relationship between the order in which characters are stored in the data buffer in main memory and the order in which they appear on tape. This relationship is independent of the direction in which characters are being transferred and, for tape read operations, is independent of the direction in which the tape is being read.

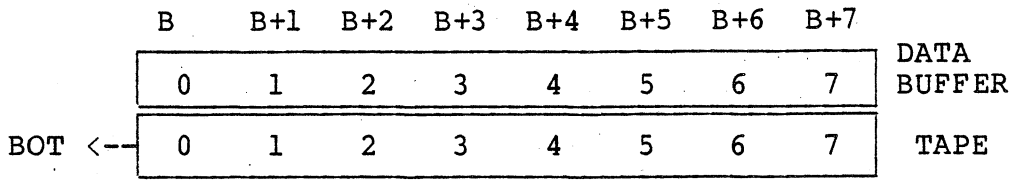
If swap-byte bit SWB is set in the header of the command packet, then character positions within each word are reversed with respect to the standard relationship. To illustrate this in terms of the data buffer address (B) two cases must be shown.

Figure 3-3B, illustrates the case of an even buffer address, BE. For this case, character 0 (the character that appears closest to the BOT) is stored at (B_E + 1) and character 1 is stored at B_E. Character 2 is stored at (B_E + 3) and character 3 is stored at (B_E + 2). And so on.

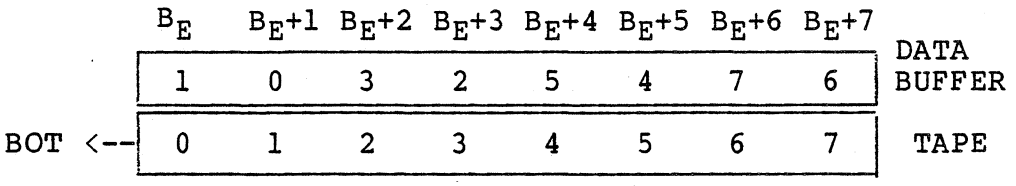
For an odd buffer address, B_O, character 0 is stored at B_O - 1); character 1 is stored at (B_O + 2); character 2 is stored at (B_O + 1), and so on. This case is illustrated in Figure 3-3C.

Table 3-6 Characteristics Mode Byte Format

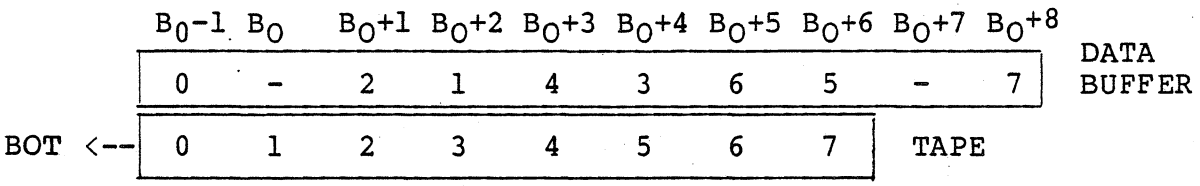
Bit	Mnemonic	Meaning
07	ESS	Instructs the tape transport to stop on a double tape mark during a Skip Tape Marks Position Command.
06	ENB	If the tape is at BOT and if ESS is set, instructs the tape transport to stop on a tape mark if it is the first tape block record encountered during a Skip Tape Marks Position Command. (LET status will be indicated.)
05	EAI	Enables ATTN interrupts when reporting on-line/off-line status change provided that interrupt-enable bit is set in command which passes message buffer ownership to controller, allowing status update to occur.
04	ERI	Enables interrupt in response to message buffer release command if IE is set in command packet header word.



A. Standard (DEC) Relationship (SWB=0)



B. Swapped Bytes (IBM), Even Buffer Address (SWB=1)



C. Swapped Bytes (IBM), Odd Buffer Address (SWB=1)

NOTE: 0 - 7 denote particular characters

Figure 3-3 Order of Characters

MESSAGE PACKET

Figure 3-4 illustrates the overall format of the message packet. The first word is the header word. The information in this word is summarized in Table 3-7. The second word is the data length word which always contains the value 10 (decimal) corresponding to the number of data bytes in the packet. The remaining words are extended status words RBPCR, XSTAT0, XSTAT1, XSTAT2, and XSTAT3. The information contained in these words is summarized in Table 3-8.

Figure 3-4 Message Packet Format

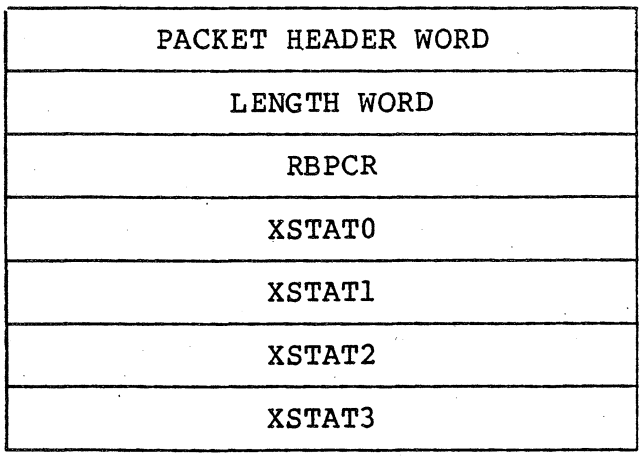


Table 3-7 Message Packet Header Word Format

Bit(s)	Mnemonic/ Name	Meaning
15	ACK	Indicates that controller has accessed the command packet buffer. In an ATTN message reporting an on-line status change, this bit is false.
14-12	-	Not used
11-8	Class Code Field	In a FAIL or ATTN message (see bits 4-0), this code defines the type of event. The controller ATTN messages are always type 0000 (indicating a change of on-line/off-line status). For a FAIL message, 0010 indicates a write-lock error or non-executible function and 0001 indicates other types of failures.
7-5	Packet Format Field	Always 000 indicating one word header.
4-0	Message Code	Code Value / Name / Associated Termination Class Codes in TSSR: 10000 End 0, 2 10001 Fail 3 10010 Error 4, 5, 6 10011 Attention 1

Table 3-8
Extended Status Word Formats

Bit(s)	Mnemonic	Meaning
RBPCR REGISTER		
15-0	C15-C0	Residual byte, record, or tape mark count for Read, Space Record, or Skip Tape Mark commands, respectively.
XSTAT0		
15	TMK	Tape mark detected during Read, Space, Skip, or Write Tape Mark command. Causes termination class code 2 if set during a Read or Space command.
14	RLS	For a Read operation, indicates that record length was less than byte count. For a Space Record operation, indicates that tape mark was encountered before specified number of records were spaced over. For Skip Tape Mark operation, indicates BOT was encountered before specified number of tape marks were spaced over. Causes termination class code 2.
13	LET	Logical End of Tape - Indicates a stop has occurred during a Skip Tape Marks Position command as a result of ESS or ENB bit of Characteristics Mode Byte being set and double tape mark or tape mark immediately following BOT being encountered.
12	RLL	Record read contained more bytes than specified by byte count. Causes termination class code 2.
11	WLE	Indicates attempt to write on or erase write protected tape. Causes termination class code 3: write-enable ring not installed. Causes termination class code 6 if WRITE LOCK switch is activated during operation.
10	NEF	The command could not be executed. Causes termination class code 3. (A command requiring reverse motion cannot be executed if the tape is at the BOT position. A write command cannot be executed if the write-enable ring is not installed on the tape. A motion command cannot be executed if VCK (bit 4) is set and the CVC bit in the command header is not set or if the unit is off-line.)

Table 3-8 (Continued)
Extended Status Word Formats

Bit(s)	Mnemonic	Meaning
09	ILC	Command code/command mode value does not correspond to operation supported by transport. Causes termination class code 3.
07	MOT	Capstan is moving.
06	ONL	Tape transport is On-Line. When tape switches on-line, termination class code 1 is presented with ATTN interrupt. If motion command is received when tape is off-line, termination class code 3 is presented.
05	IE	Interrupt Enable bit from most recent command.
04	VCK	Volume Check bit set after initialization and when transport switches between on-line and off-line status. Reset in response to CVC bit in command header. Causes termination class code 3 if it remains set.
03	PED	Indicates transport is capable of phase-encoded mode operation only.
02	WLK	Mounted tape reel does not have write-enable ring installed.
01	BOT	Beginning-of-tape reflective strip is being detected. Causes termination class code 3 if set when command requiring reverse motion is received. Causes termination class code 2 if set during command execution.
00	EOT	Indicates tape position is beyond reflective end-of-tape marker. Causes termination class code 2 if set during a write operation.
XSTAT1		
15	DLT	Indicates that data transfers between controller and PDP-11 memory have not been accomplished at rate required by tape read or write rate. Causes termination class code 4.
14	-	Not assigned.
13	COR	Indicates that a correctible error has been encountered during a read command.
12	CRS	Not supported.

Table 3-8 (Continued)
Extended Status Word Formats

Bit(s)	Mnemonic	Meaning
11	TIG	Not supported.
10	DBF	Not supported.
09	SCK	Not supported.
08	-	Not used.
07	IPR	Not supported.
06	SYN	Not supported.
05	IPO	Not supported.
04	IED	Not supported.
03	POS	Not supported.
02	POL	Not supported.
01	UNC	Indicates that an uncorrectable parity error has occurred during a read operation or that any parity error has occurred during a write operation. Causes termination class code 4.
00	MTE	Indicates that a multitrack dropout has been detected.
XSTAT2		
15	OPM	Indicates tape has moved in response to most recent command.
14	SIP	Not supported.
13	BPE	Not supported.
12	CAF	Not supported.
11	-	Not used.
10	WCF	Not supported.
09	-	Not used.
08	DTP	Not supported.
07-00	DT7-DT0	Not supported.

Table 3-8 (Continued)
Extended Status Word Formats

Bit(s)	Mnemonic	Meaning
XSTAT3		
15-08	-	Not supported.
07	LMX	Not supported.
06	OPI	Indicates a Read, Space or Skip operation moved 25 feet of tape without encountering data. Also set in a Write operation if the read head doesn't encounter data after moving four feet of tape.
05	REV	Indicates that reverse motion was required to execute most recent motion command. (This includes all retry commands.)
04	CRF	Not supported.
03	DCK	Indicates that an identification burst error has been detected. If set when a write command is executed, causes termination class code 6.
02	NOI	Not supported.
01	LXS	Not supported.
00	RIB	Indicates that the BOT marker was encountered after the start of reverse tape motion during a Read, Space, or Skip command. Causes termination class code 2. Tape motion is halted at the BOT position.

SECTION IV

COMPUTER INTERFACE

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SECTION IV - CONPUTER INTERFACE

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SECTION IV

CONPUTER INTERFACE

DEC PDP-11 UNIBUS

The tape controller interfaces to the Unibus of the DEC PDP-11 computer system. The Unibus is an asynchronous I/O bus with separate 18-bit address lines and 16 bit data bus lines. In addition to address and data information, the bus contains signal lines for NPR (DMA) Operations, Bus Requests (Interrupts), data transfer handshaking, initialization of devices and other control signals.

BUS INTERFACE SIGNALS

The interface signals used by the tape controller to communicate with the bus, along with the connector and pin assignments, are shown in Table 4-1. The functions of these signals, as illustrated in Figure 4-1, are:

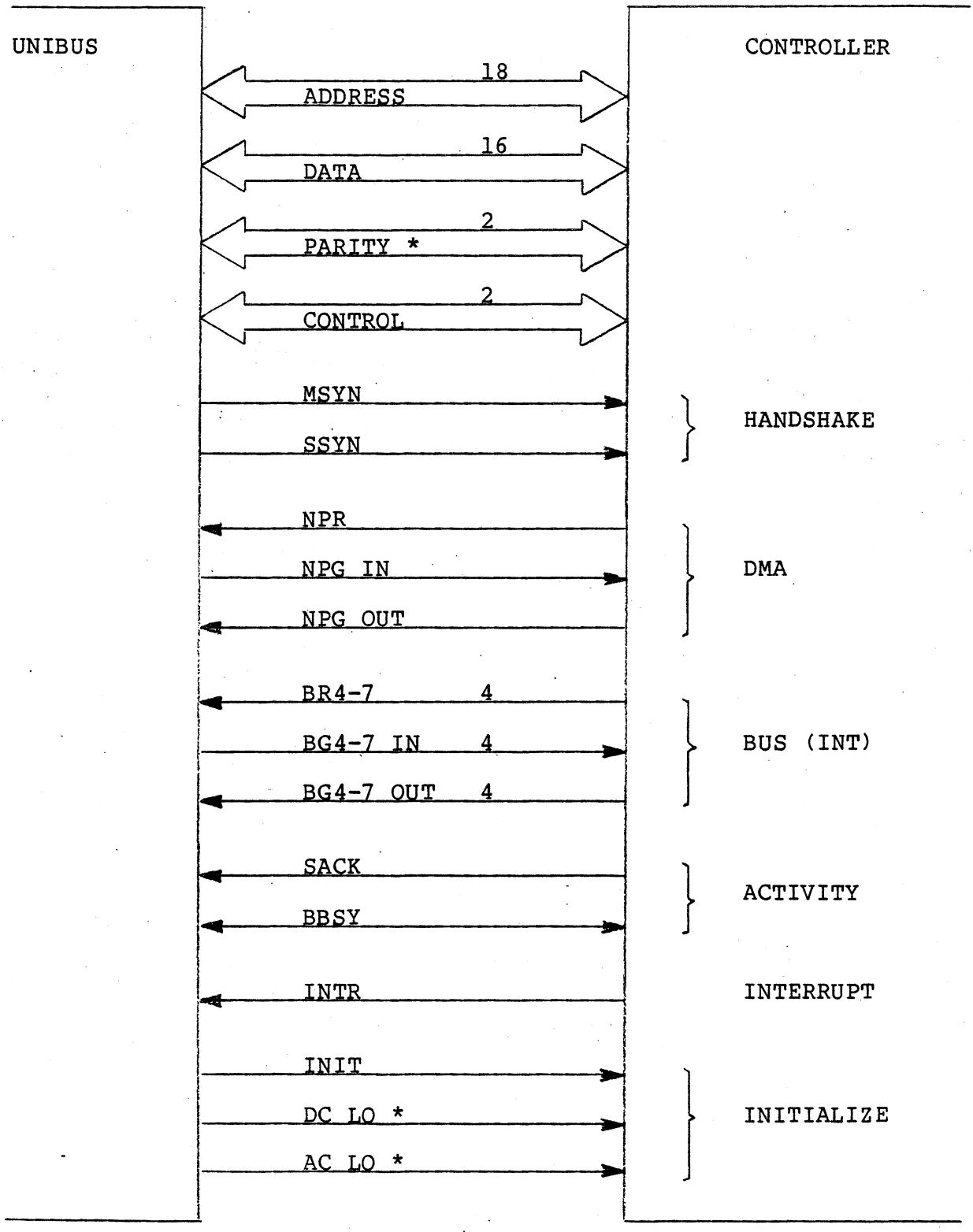
1. A0-A17/-A21 (ADDRESS LINES) - These lines are the 18-bit address bus over which memory address and peripheral register address information is communicated. Address information is placed on the bus by the bus master device and is received and decoded by the selected slave device. The master device then either receives input data from, or outputs data to the addressed slave device (or memory) over the data bus lines.

2. D0-D15 (DATA LINES) - These 16 lines are used to transfer data and register control/status information to and from the tape controller.

3. PA,PB (PARITY) - These lines are used by certain devices to indicate parity errors. (Not used in this device.)

4. C0, C1 (CONTROL LINES) - These two lines are coded by the master device to describe the type of transfer, as follows:

C1	C0	OPERATION
0	0	DATI - Data In (to master)
1	0	DATO - Data Out (from master)
1	1	DATOB - Data Out, Byte (from master)



* Not used in this device

Figure 4-1 Bus Interface

5. MSYN (MASTER SYNC) - This control signal is issued by the master device to indicate that Address and Control information is present on the bus.

6. SSYN (SLAVE SYNC) - This control signal is issued by the slave device in response to the signals MSYN or INTR generated by the master device.

7. NPR (NON-PROCESSOR REQUEST) - This signal is asserted by the tape controller to request control of the bus for the purpose of transferring drive data directly to or from memory.

8. NPG (NON-PROCESSOR GRANT) - This signal is generated at the processor in response to the NPR, at the end of the bus cycle in progress. Since NPG is daisy-chained through the devices connected to the bus, it is received and regenerated by each device until it reaches the requesting device.

9. BR4-BR7 (BUS REQUEST LINES) - One of these lines will be asserted by the conrtroller to request control of the bus for the purpose of interrupting the processor.

10. BG4-BG7 (BUS GRANT LINES) - One of these signals is generated at the processor in response to the corresponding Bus Request signal, after completing the instruction in progress. Since the Bus Grant lines are daisy-chained through the devices connected to the bus, it is received and regenerated by each device until it reaches the requesting device.

11. SACK (SELECTION ACKNOWLEDGE) - This signal is asserted by the tape controller in response to the processor's NPG or Bus Grant signal, indicating that control of the bus will pass to the tape controller when the current bus master completes its operation.

12. BBSY (BUS BUSY) - This signal is asserted by the bus master to indicate that the bus is in use. When BBSY goes false, control of the bus is passed to the new bus master.

13. INTR (INTERRUPT REQUEST) - The tape controller asserts this signal after becoming bus master to indicate that the desired Interrupt Vector information is present on the bus.

14. INIT (INITIALIZE) - This signal is asserted by the processor to initialize or clear all devices connected to the bus.

15. DC LO (DC POWER LOW) - This signal from the power supply initiates power-on sequencing in the computer and some devices.

16. AC LO (AC POWER LOW) - This signal from the power supply initiates power-fail sequencing in the computer and some devices. (Not used in this device.)

BUS OPERATIONS

The tape controller receives commands from and provides status information to the processor, with the tape controller being the slave device. After the tape controller receives the proper commands to transfer data, the tape controller becomes a bus master device, handling the data transfers directly with memory (a process which requires no processor intervention). When the tape controller has completed all data transfers, it alerts the processor by issuing an interrupt request. Bus operations are illustrated in Figures 4-2, 4-3 and 4-4 and are described in the following paragraphs.

The tape controller requests a data transfer on the bus by asserting NPR. After completing the current bus cycle, the processor inhibits initiation of a new bus cycle and responds by asserting NPG. The tape controller then asserts SACK and removes NPR, causing the processor to terminate NPG. When BBSY goes false, the tape controller becomes bus master, asserting BBSY, and executing the required data transfer of one or more data words to or from memory. When the data transfer is completed, the tape controller relinquishes the bus to the processor by terminating the BBSY signal. The processor then returns to its programmed operations.

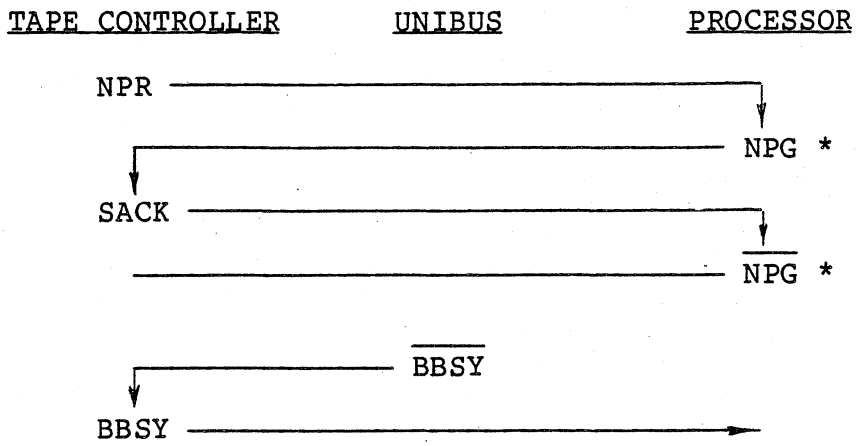
INPUT AND OUTPUT OPERATIONS

Input operations are used by the processor to receive status information from the tape controller and are used by the tape controller to obtain data from memory to be written onto tape. Output operations are used by the processor to provide the tape controller with command information and are used by the tape controller when transferring information read from tape to the desired location in memory.

To begin an input transfer, address, control and MSYN are placed on the bus. The slave device responds by placing data and SSYN on the bus. The master device then receives the data, terminating MSYN, which causes the slave device to remove both SSYN and the data from the bus lines. The BBSY signal is then removed by the master device, terminating the input transfer. For an output transfer, data is placed on the bus by the master device together with MSYN. The slave device accepts the data and acknowledges by asserting the SSYN signal, which causes the master device to remove the data and terminate the MSYN signal. This action by the master device causes the slave to remove the SSYN signal which in turn causes the master to remove the BBSY signal, terminating the output transfer.

INTERRUPTS

Interrupts are used in the system so that the processor is not burdened with the responsibility of determining when the



* NOTE: Daisy-chained signal

Figure 4-2 DMA Request/Grant Sequences

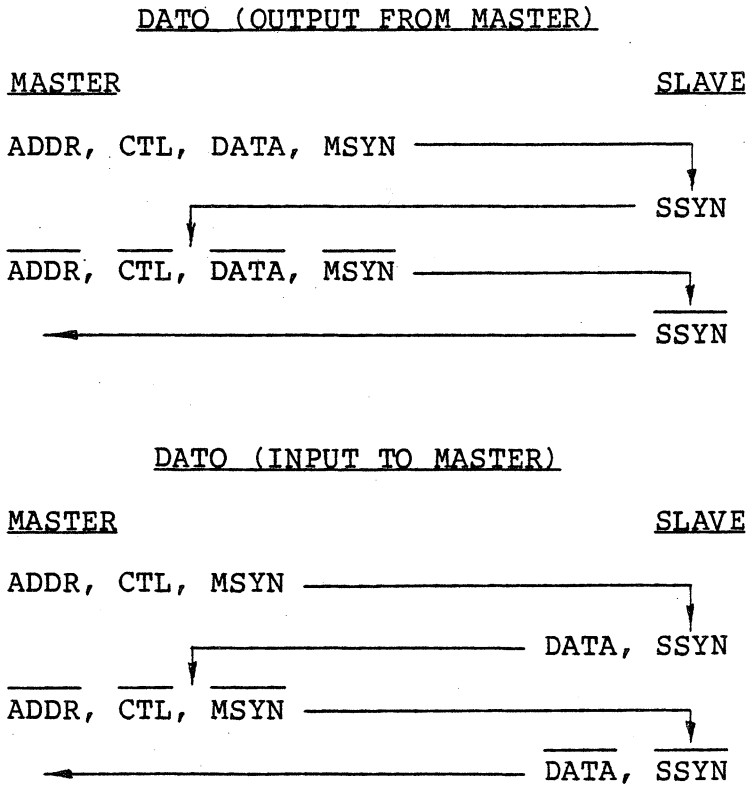
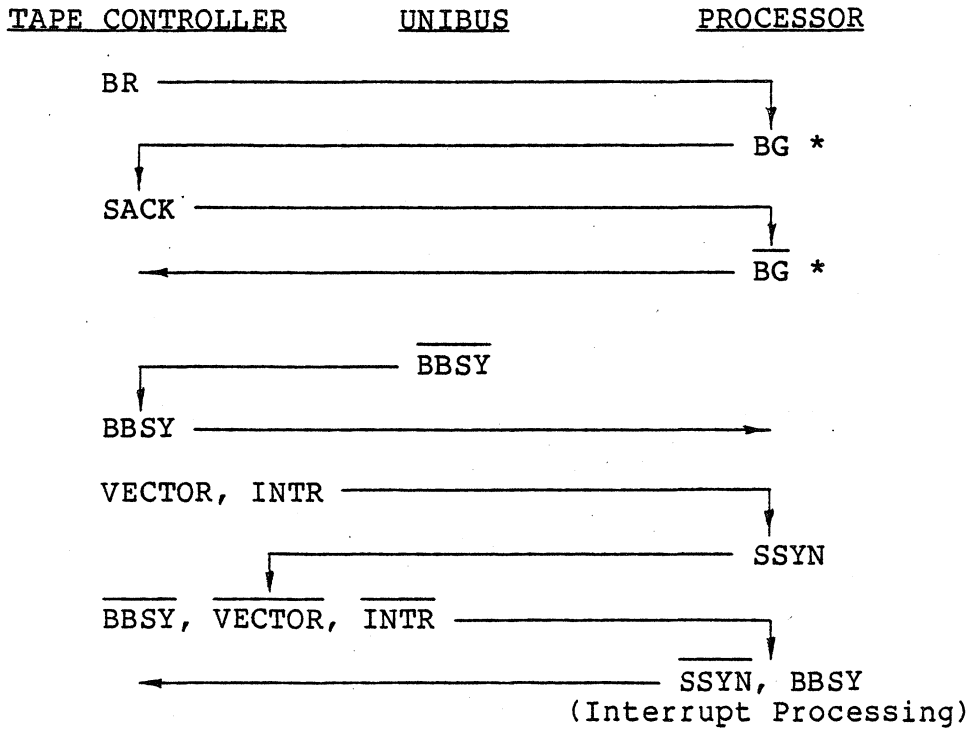


Figure 4-3 Bus Transfer Sequences

tape controller has completed an operation. Interrupt processing allows the processor to continue with its programmed tasks until alerted by the tape controller. When enabled in the tape controller, the Bus Request is issued by the tape controller to the processor upon completion of an operation. If the processor currently is accepting Bus Requests at that priority level, the daisy-chained Bus Grant signal is issued as a response. The Bus Grant signal is passed along by each device until captured by the requesting tape controller. The interrupting tape controller will then remove the Bus Request and assert SACK. When the instruction in progress has been completed, further program execution is suspended and the BBSY signal is released, allowing the tape controller to become bus master. It asserts BBSY and INTR and places its hardwired vector address onto the bus. The vector points to memory locations containing a new processor status word (psw) and the program counter address (pc) of the interrupt handling routine. The processor saves its current processor status word and program counter address, receives the vector, and then terminates the SSYN signal. This causes the tape controller to terminate the BBSY and INTR signals and remove the vector from the bus. The processor will then enter the tape controller's interrupt service routine to handle the interrupt.



* NOTE: Daisy-chained signal

Figure 4-4 Bus Request/Interrupt Sequence

CONNECTOR F

PIN	SIDE 1	SIDE 2
A		+5V
B		-15V
C		GND
D	BBSYL	
E		
F		
H		
J	NPRL	
K		
L		
M	INTRL	
N		
P		
R		
S		
T	GND	SACKL
U		
V		

CONNECTOR E

PIN	SIDE 1	SIDE 2
A		+5V
B		
C	A12L	GND
D	A17L	A15L
E	MSYNCL	A16L
F	A07L	C1L
H	A01L	A00L
J	SSYNCL	C0L
K	A14L	A13L
L	A11L	
M		
N		A08L
P	A10L	A07L
R	A09L	
S		
T	GND	
U	A06L	A04L
V	A05L	A03L

CONNECTOR D

PIN	SIDE 1	SIDE 2
A		+5V
B		
C		GND
D		BR7L
E		BR6L
F		BR5L
H		BR4L
J		
K		BGIN7H
L	INITL	BGOUT7
M		BGIN6H
N		BGOUT6
P		BGIN5H
R		BGOUT5
S		BGIN4H
T	GND	BGOUT4
U		
V		

CONNECTOR C

PIN	SIDE 1	SIDE 2
A	NPGH	+5V
B	GOUTH	
C		GND
D		D15N
E		D14N
F		D13N
H	D11N	D12N
J		D10N
K		D09N
L		D08N
M		D07N
N	DCLOL	D04N
P		D05N
R		D01N
S	PBL	D00N
T	GND	D03N
U		D02N
V		D06N

* Connectors A and B use only ground connections (T1, C2)

Table 4-1 Unibus Signals

SECTION V

PERTEC-COMPATIBLE FORMATTER INTERFACE

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SECTION V - PERTEC-COMPATIBLE FORMATTER INTERFACE

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SECTION V

PERTEC-COMPATIBLE FORMATTER INTERFACE

FORMATTED TAPE DRIVE INTERFACE

This section defines the interface to the tape formatter for the streaming or non-streaming tape units controlled by the tape controller. This interface is based on the industry standard interface for 1/2 inch formatted tape units, The basic industry conventions such as cabling, electrical characteristics, data and command transfer characteristics, and timing have been maintained.

Two 50-conductor 3M-type ribbon cables are used for interconnection between the standard or streaming transport formatter and the tape controller. These cables are connected between the card connectors on the tape controller and the formatter PC board. Cable length can be a maximum of 6.0 meters (20 feet).

The formatter input circuits are designed such that either a disconnected wire or removal of power at the transmitter results in a false signal being interpreted at the receiver end. All lines between the tape controller and the drive's formatter are low-true and driven by tri-state devices,

The following tables provide a list of pins and a definition of terms as used on the interface between the tape controller and the formatter.

INTERFACE				INTERFACE			
CON-NECTOR	SIGNAL PIN	RETURN PIN	LO-TRUE SIGNAL	CON-NECTOR	SIGNAL PIN	RETURN PIN	LO-TRUE SIGNAL
J3	2	1	FFBY	J4	1	5	FRDP
J3	4	3	FLWD	J4	2	5	FRDO
J3	6	5	FWD4	J4	3	5	FRD1
J3	8	7	FGO	J4	4	5	FLDP
J3	10	9	FWD0	J4	6	5	FRD4
J3	11	12	FWD1	J4	8	7	FRD7
J3	14	13	SPARE	J4	10	9	FRD6
J3	16	15	NOT USED	J4	12	11	FHER
J3	18	17	FREV	J4	14	13	FFMK
J3	20	19	FREW	J4	16	14	FID
J3	22	21	FWDP	J4	18	17	FFEN
J3	24	23	FWD7	J4	20	19	FRD5
J3	26	25	FWD3	J4	22	21	FEOT
J3	28	27	FWD6	J4	24	23	FOFL
J3	30	29	FWD2	J4	26	25	NOT USED
J3	32	31	FWD5	J4	28	27	FRDY
J3	34	33	FWRT	J4	30	29	FRWD
J3	36	35	NOT USED	J4	32	31	FFPT
J3	38	37	FLGAP	J4	34	33	FRSTR
J3	40	39	FERASE	J4	36	35	FDWDS
J3	42	41	FWFM	J4	38	37	FDBY
J3	44	43	NOT USED	J4	40	39	NOT USED
J3	46	45	FTADO	J4	42	41	FCER
J3	48	47	FRD2	J4	44	43	FONL
J3	50	49	FRD3	J4	46	45	FTAD1
				J4	48	47	FFAD
				J4	50	49	FSMC

Table 5-1 I/O Cable Pin Assignments

Table 5-2 Tape Controller To Formatter Signals

LO-TRUE SIGNAL	DEFINITION	DESCRIPTION
FFAD	Formatter Address	This signal level selects one of two possible transports attached to to transport interface: 1. FFAD False = Address 0 2. FFAD True = Address 1 The transport's address is predetermined by a strap on the formatter PWA.
FTADO,1	Transport Address	Addresses up to 4 transports per formatter.
FGO	Initiate Command	This signal is used to strobe the following command lines on the trailing edge: 1. FREV 4. FERASE 2. FWRT 5. FLGAP 3. FWFM 6. FSMC
FREV	Reverse/Forward	This signal specifies the direction of tape motion as follows: 1. False = Forward 2. True = Reverse
FWFM	Write File Mark	
FERASE	Erase Tape	If FERASE and FWRT are low, the transport is positioned to execute a Dummy-Write command. The transport will go through all of the operations of a normal Write command except that data is recorded. A length of tape will be erased equivalent to the length of the Dummy-Record (as defined by FLWD). Alternatively, if FERASE, FWRT, and FWFM command lines are all low, the transport is conditioned to execute a Dummy-Write File Mark command. A fixed length of tape of approximately 3.6 inches will be erased.

Table 5-2 Tape Controller To Formatter Signals (Continued)

LO-TRUE SIGNAL	DEFINITION	DESCRIPTION
FLGAP	Long Gap	When true, this line causes the transport to be set up for 1.2 inch gap. When false, will select the normal 0.6 inch gap.
FSMC	Speed Mode change	This signal causes selected transports to change the mode of operation (12.5 ips/100 ips).
FREW	Rewind	This signal (minimum 1.0 microsecond pulse) causes the selected transport to rewind to BOT. The FRWD signal is asserted during the rewind operation. Formatter Busy is not set during a Rewind.
FOFL	Off-line & Rewind	This line must be held true for a minimum of 1.0 microsecond. It causes the transpoert to rewind and unload the tape. Formatter Busy is not set.
FWDO-7,P	Write Data	These lines transmit data to the transport. FWDO represents the most significant bit.
FFEN	Formatter Enable	This signal, when false, causes the transport to be reset to initialized state. It is independent to FFAD. This is a level signal that will hold the transport reset while false.
FLWED	Last Word	During Write and Controlled Erase, this line, when true with FWDO-7, FWDP indicates that the character being strobed into the formatter is the last of the record.

Table 5-3 Formatter Interface Commands

COMMAND	LOOP	SNSR	REV	WRT	WFM	ERASE
Read Forward*	Low	Low	Low	Low	Low	Low
Read Reverse*	Low	Low	High	Low	Low	Low
Write*	Low	Low	Low	High	Low	Low
Write File Mark	Low	Low	Low	High	High	Low
Space Forward	Low	Low	Low	Low	Low	High
Space Reverse	Low	Low	High	Low	Low	High

Low = False
High = True

* FLGAP is also strobed during these command transfers indicating the setting of a long or normal gap length (2.2 inch IBG or 0.6 inch IBG nominal, respectively). FSMC is also strobed by FGO. However, FSMC is not issued during data operations. (FLGAP, FSMC and FGO are low-true signals.)

Table 5-4 Formatter To Tape Controller Signals

LO-TRUE SIGNAL	DEFINITION	DESCRIPTION
FFBY	Formatter Busy	Only goes true when FGO command is received. Remains true until completion of command execution.
FDBY	Data Busy	Only goes true when the transport has reached operating speed, traversed the IBG, and the transport is about to write data on the tape or read data from the tape. Data Busy remains low until the data transfer is finished. A new command may be given when Data Busy goes false for an "on-the -fly" operation. "On-the-fly" commands must be the same read/write mode and same tape direction.
FID	PE Identification	Set when writing first record from load point or reading first record from load point if tape is PE.
FHER	Hard Error	This line is set low if any error has been detected. This line will be set low as soon as an error occurs and stays low until the next FGO signal is transmitted, or the FFEN signal is set high. all error information will be reported to the controller before FDBY signal goes false.
FCER	Corrected Error	This line is set low whenever a single track error occurs during a read or read-after-write operation. The signal will stay true until the next FGO signal is transmitted or FFEN signal is set high. If the FCER signal is set low during the read-after-write operation, the record should be rewritten.
FFMK	File Detected	
FRDY	Selected Transport On-Line	
FRWD	Rewind	
FEOT	End of Tape	

Table 5-4 Formatter To Tape Controller Signals (Continued)

LO-TRUE SIGNAL	DEFINITION	DESCRIPTION
FFPT	File Protect	
FLDP	Load Point	
FDWDS	Demand Write Data Strobe	
FDWDS	Demand Write Data Strobe	This line consists of a pulse for each data character to be written onto tape. The pulse width of signal FWDS is 1 microsecond. The first data character should be available on the write data input lines within one character period after the FDBY signal has been set true, and remain true until the trailing edge of the first FDWDS signal. Succeeding characters must then be placed on these lines within one-half of a character period after the trailing edge of each FDWDS signal. During a Write File Mark command, the required file mark pattern is generated internally by the formatter and the FDWDS signal is not used. During erase operation (variable length), this line will also be used. However, no data are transferred or written onto tape. The controller may use this line to determine the length of tape which has been erased.

Table 5-4 Formatter To Tape Controller Signals (Continued)

LO-TRUE SIGNAL	DEFINITION	DESCRIPTION
FRSTR	Read Data Strobe	This line consists of a pulse for each character of read information to be transmitted to the customer controller interface and should be used to sample the read data lines FRDP, FRDO-7. The pulse width of this signal is 1.2 microseconds. The average time between pulses on the FRSTR line is given by: $\frac{1}{S \times D}$ Where D = 1600 bpi and S = tape speed (ips) The customer controller interface must be able to accept the whole block of data at the specified data rate. Due to bit crowding, tape speed variation, and signal drop-out correction (PE), the customer controller interface must be able to receive characters at a rate which can vary twice the nominal rate and half the nominal rate.
FRD0-7, P	Read Data	These nine lines transmit read data from the formatter to the customer controller. Each character read from tape is available to sampling these lines in parallel with the FRSTR. Data will be placed on the read to the leading edge of the FRSTR pulse. The data remans on the read datsa 1;ines for at least 0.5 microseconds after the trailing edge of the FRSTR pulse. Sense data is also transmitted on this bus analogous to the read data at 160K byte/second rate.

SECTION VI

STC/TELEX TAPE INTERFACE

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SECTION VI - STC/TELEX TAPE INTERFACE

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SECTION VI

STC/TELEX TAPE INTERFACE

GCR FORMATTED TAPE DRIVE INTERFACE

This section defines the interface to the STC or Telex tape formatter for tape units with GCR tape format capability controlled by the TAPE DIMENSION III. This interface is based on the manufacturers' specifications for their interface for 1/2 inch GCR-formatted tape.

Two 60-pin cables are used for the connection between the tape formatter and the tape controller. These cables are connected between the card connectors on the tape controller and the tape formatter. Cable length can be a maximum of 6.0 meters (20 feet). The Telex interface requires an adapter (available from Western Peripherals) that breaks out the signals into three 50-pin cables for connection to the Telex formatter.

Formatter input circuits are typically designed such that either a disconnected wire or removal of power at the transmitter results in a false signal being interpreted at the receiver end. All lines between the tape adapter and the drive's formatter are low-true and driven by tri-state devices.

The following paragraphs and tables provide a list of pins and a definition of terms as used on the interface between the controller and the formatter. Signals in parentheses are for the STC interface while those in square brackets are for the Telex formatter interface.

CONTROLLER-TO-FORMATTER SIGNALS

Initiate Command (Start)/[Command Clock] - This line clocks the command, address and density into the formatter and initiates the command. The controller asserts this signal until the formatter goes Busy.

Tape Unit Address (AD0,1)/[TA1,2] - Tape unit address lines are available at the interface for selection of a specific tape unit connected to the formatter.

Density Select (DS0,1) - During a read operation, tape density is automatically set according to the ID Burst. For a write operation (with the drive positioned at load point and set for remote software density selection) these lines select the density as follows:

DS0	DS1	Density Selected
0	0	Phase Encoded
1	0	Group Code Recording
0	1	NRZI
1	1	(NRZI) [Selected by drive]

Command Select (CMD0-3) [CMD0-4] - The commands to the formatter are specified by the code present on these lines when the Command Clock line is asserted.

STC CMD0-3	TELEX CMD0-4	Function
0 0 0 0	0 0 0 0 0	No Operation
0 0 0 1	1 0 0 1 1	Drive Clear
0 0 1 0	0 1 0 1 1	Diagnostic Mode
0 0 1 1	1 0 1 0 0	Sense Drive Status
0 1 0 0	0 0 0 1 0	Read One Block
0 1 0 1	0 1 1 0 0	Read Reverse One Block
0 1 1 0	0 0 0 0 1	Write One Data Block
0 1 1 1	0 1 X 1 1	Loop Write-to-Read
1 0 0 0	0 0 1 1 0	Backspace One File
1 0 0 1	0 0 1 0 1	Backspace One Block
1 0 1 0	0 1 0 0 0	Forward Space One File
1 0 1 1	0 0 1 0 0	Forward Space One Block
1 1 0 0	1 1 1 1 1	Write Tape Mark
1 1 0 1	1 0 1 1 1	Erase 3.5 Inch Gap
1 1 1 0	0 0 1 1 1	Rewind Tape
1 1 1 1	0 1 1 1 1	Rewind and Unload
- - - -	1 0 1 1 0	Erase Variable Gap (Ignores Write Data)
- - - -	0 1 0 1 0	Track In-Error (for NRZI error correction)
- - - -	0 0 0 1 1	Set Reject Status
- - - -	1 0 1 0 1	Tape Unit Sense (transfers 5 status bytes)

Data Transfer Acknowledge (TRAK)/[DAK] - The controller responds to the Data Transfer Request signal from the formatter with this signal. These handshaking signals are used to transfer all write and read data with the following meanings:

	Handshaking Signals	
Function	Data Req.	Data Ack.
Write	Data Req'd.	Data Avail.
Read	Data Avail.	Data Stored

Last Byte (STOP)/[LBY] - This signal indicates to the formatter that the last write data byte has been placed on the formatter bus. This signal (asserted in response to Data Transfer Request or Block Sensed) also terminates read transfers and spacing operations.

Tape Subsystem Reset (SRS)/[STSRST] - This signal resets the formatter and tape drive, discontinuing any operations in progress and resetting all command, data and status conditions. (Reset during tape motion could result in incorrect positioning or incomplete blocks.)

Multiplexed Error Status Select Code (ESC0,1)/[SLX0,1,2] - The code on these lines select the information to be placed on the Multiplexed Error Status Bus, as follows:

STC		MULTIPLEXED ERROR BIT								
SLX2-0	DESCRIPTION	P	7	6	5	4	3	2	1	0
0 0 0	Dead Tracks	DTP	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
0 0 1	Read/Write Errors	CRC ERR	WTM CHK	UCE	PART REC	MTE	NOT USED	END DATA CHK	VEL ERR	DIAG MODE LTCH
0 1 0	Diag. Aids	TACH	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0 1 1	Drive Sense Byte	WRT STAT	EOT STAT	BOT STAT	WRT INHB	FILE PROT	BKWD STAT	HIGH DENS	RDY STAT	ON-LINE
1 0 0	CRC-F	P	7	6	5	4	3	2	1	0
1 0 1	Reserved									
1 1 0	Reserved									
1 1 1	Reserved									

TELEX		MULTIPLEXED ERROR BIT							
ESC1,0	DESCRIPTION	7	6	5	4	3	2	1	0
0 0	Byte 0	NOT CMPT	VRC	MULT TRK	SAGC CHK	FMK ERR	NOIS	FMTR FAIL	DRV FAIL
0 1	Byte 1	LRC CHK	ENV CHK	PRE ERR	POST ERR	PART REC	LOST BOB	SKEW	CRC CHK
1 0	Byte 2	BRST CHK	VEL CHK	TACH FAIL	WRT CURR	LOOP OUT	NO DATA	IBG OVR	TRK P
1 1	TK IN ERR/DEAD TK	7	6	5	4	3	2	1	0

Bidirectional Data Bus (DATA 0-7,P)/[D0-7,P] - These nine data lines transmit data between the controller and the tape drive.

FORMATTER-TO-CONTROLLER SIGNALS

Data Transfer Request (TREQ)/[DRQ] - This handshaking signal requests a transfer of read or write data between the controller and the formatter. (See Data Transfer Acknowledge)

Block Sensed (BLOCK) - This signal indicates that the formatter has detected a data or tape mark block.

Input Bus Enable [IBEN] - This signal conditions the bidirectional data bus for transfers from the controller to the formatter.

Oscillator (OSC) - This signal line is derived from the internal crystal oscillator in the formatter, as follows:

GCR 50-75 ips	2.72 MHz
GCR 125 ips	2.27 MHz
NRZI and PE	1.40 MHz

Odd Byte [OBY] - This line toggles to the opposite state for each character to allow 16-bit computer word packing and unpacking.

End of Data Pulse (ENDATP) - This signal is asserted to indicate the last data byte has been read and (implied) transferred to the controller.

Data Busy [DBZ] - This signal indicates that write or read data is being transferred on the formatter bus.

Formatter Busy (BUSY)/[BSY] - This signal is true from the time the command is initiated until it is rejected or completed.

Identification Burst (ID BRST)/[IDB] - This signal indicates an Identification Burst (6250 or 1600) has been read or is being written.

Tape/File Mark Status (TMS)/[FMK] - This signal indicates a File/Tape Mark has been read or is beiing written.

Command Reject (REJECT)/[REJ] - This signal indicates the previous command is inappropriate to formatter/drive status.

Operation Incomplete (OP INC) - This signal is set to indicate the command was initiated but was not completed by the formatter.

Reverse Operation [REV] - This status signal indicates the previous command was a reverse command.

Overrun Status (OVRNS)/[OVR] - This signal indicates the data rate of the formatter has exceeded the transfer rate of the controller/bus and data has been lost.

ROM Parity Error Status (ROMPS)/[RPE] - This signal indicates an internal microcode failure in the formatter.

Slave Status Change (SSC) - This line indicates a drive has gone Ready, On-Line or Off-Line.

Error Status [ERR] - This line is set for the following error status: DPE, OVR, LWR, Multiplexed Error Bytes 0 and 2 (exc. bit 7) and Byte 1 (bits 0, 4-7 and bits 2 & 3 in the write mode).

Data Check (DATA CHK) - This signal indicates one or more of the following conditions has occurred: Any bit (exc. bit 1) of Multiplexed Error Status Byte 1, (CRC Error, Write Tape Mark Check, Uncorrectable Error, Partial Record, Multiple Track Error, End of Data Check, Velocity Error), Overrun, VRC Error, LRC Error, TIE Cannot be Found, Write Skew Error, BOT Detected, PE Postamble Error, Single Track Error.

Erase Mode [EM] - This status line indicates the previous command accepted was an erase operation.

Read Mode [RM] - This status line indicates the previous command accepted was a reading operation.

Write Mode [WM] - This status line indicates the previous command accepted was a writing operation.

Multiplexed Error Status Bus (ERRMX 0-7,P)/[ERROR 0-7,P] - These nine lines provide the Error Status Bytes previously described.

Corrected Error (CRERR)/[COR] - This signal is set to indicate the follwing errors have been corrected:
1 - PE single track read or read-after-write error.
2 - GCR single or double track read or read-after-write error.
(3) - NRZI tape error - resulting in a reread.

Data Bus Parity Error (BUPER)/[DPE] - (STC - This line indicates incorrect data parity was detected on the formatter data bus.) [Telex - This line indicates a VRC, CRC or LRC error occurred.]

On Line Status (ONLS)/[ONL] - This status line indicates the tape drive is On Line.

Ready Status (RDYS)/[RDY] - This status line indicates the tape drive is On Line with tape loaded and not rewinding.

Beginning of Tape Status (BOTS)/[BOT] - This status line indicates the tape is positioned at the BOT marker.

End of Tape Status (EOTS)/[EOT] - This status line indicates the tape is positioned at or beyond the EOT marker.

File Protect Status (FPTS)/[FPT] - This status line indicates the tape was loaded on the drive without a write-enable ring in the supply reel.

Rewinding Status (REWS)/[RWG] - This status line indicates the tape is rewinding to BOT.

High Density Status (HDENS)/[DDS0] - This status line indicates the GCR format is selected.

NRZI Status (NRZI)/[DDS1] - Unless High Density Status is selected, this status line indicates the NRZI format is selected.

Table 6-1 Pin Assignments for STC/Telex Interface (Connector J1)

CONTROLLER CONNECTOR J1				TELEX I/O CONNECTORS			
SIGNAL PIN	GROUND PIN	CONTROLLER SCHEM. MNEMONIC	STC MNEMONIC	TELEX MNEMONIC	CONN NO.	SIGNAL PIN	GND. PIN
A2	B2	ER0	ERMX-0	ERROR 0	3	2	27
A3	B3	ER1	ERMX-1	ERROR 1	3	3	28
A4	B4	ER2	ERMX-2	ERROR 2	3	4	29
A5	B5	ER3	ERMX-3	ERROR 3	3	5	30
A6	B6	ER4	ERMX-4	ERROR 4	3	6	31
A7	B7	ER5	ERMX-5	ERROR 5	3	7	32
A8	B8	ER6	ERMX-6	ERROR 6	3	8	33
A9	B9	ER7	ERMX-7	ERROR 7	3	9	34
A10	B10	FBSY	BUSY	BSY	1	12	37
A11	B11	DREQ	TREQ	DRQ	2	12	37
A12	B12			RM	1	22	47
A13	B13	IDB	ID BURST	IDS	2	19	44
A14	B14	OPI	OPINC	REV	1	21	46
A15	B15	DBSY	ENDATP	DBZ			
A16	B16	FMT	TMS	FMK	2	22	47
A17	B17	RJS	REJECT	REJ	1	14	39
A18	B18	OVR	OVRNS	OVR	2	16	41
A19	B19	EM	DATA CHK	EM	1	25	50
A20	B20	RPE	ROMPS	RPE	1	20	45
A21	B21	CERR	CRERR	COR	2	18	43
A22	B22	BLK	BLOCK	IBEN	2	10	35
A23	B23	DD0	NRZI	DDS0	2	20	45
A24	B24	DPE	BUPER	DPE	2	24	49
A25	B25	ONL	ONLS	ONL	1	17	42
A26	B26	DD1	HDENS	DDS1	2	21	46
A27	B27	RDY	RDYS	RDY	1	18	43
A28	B28			WM	1	23	48
A29	B29	CMD0	RESERVED	CMD0	2	11	36
A30	B30	TA0	RESERVED				

NOTE: All interface signals are low-true.

Table 6-2 Pin Assignments for STC/Telex Interface (Connector J2)

CONTROLLER CONNECTOR J2				TELEX I/O CONNECTORS			
SIGNAL PIN	GROUND PIN	CONTROLLER SCHEM. MNEMONIC	STC MNEMONIC	TELEX MNEMONIC	CONN NO.	SIGNAL PIN	GND. PIN
A1	B1	TA0	AD0	TA1	1	2	27
A2	B2	TA1	AD1	TA2	1	3	28
A3	B3	CMD1	CMD0	CMD1	1	5	30
A4	B4	CMD2	CMD1	CMD2	1	6	31
A5	B5	CMD3	CMD2	CMD3	1	7	32
A6	B6	CMD4	CMD3	CMD4	1	8	33
A7	B7	DS0	DS0	DS0	1	9	34
A8	B8	CMDCLK	START	CMD. CLK	1	13	38
A9	B9	LBYT	STOP	LBY	2	14	39
A10	B10	DACK	TRAK	DAK	2	13	38
A11	B11	(NO NAME)	DATA-P	DP	2	9	34
A12	B12	(NO NAME)	DATA-0	D0	2	1	26
A13	B13	(NO NAME)	DATA-1	D1	2	2	27
A14	B14	(NO NAME)	DATA-2	D2	2	3	28
A15	B15	(NO NAME)	DATA-3	D3	2	4	29
A16	B16	(NO NAME)	DATA-4	D4	2	5	30
A17	B17	(NO NAME)	DATA-5	D5	2	6	31
A18	B18	(NO NAME)	DATA-6	D6	2	7	32
A19	B19	(NO NAME)	DATA-7	D7	2	8	33
A20	B20	SRST	RESET	SYSRST	2	23	48
A21	B21	ESC1	SLX1	ESC1	3	11	36
A22	B22	ESC0	SLX0	ESC0	3	10	35
A23	B23	DS1	DS1	DS1	1	10	35
A24	B24	ESC2	SLX2	NOT USED			
A25	B25	ERR	SSC	ERR	2	17	42
A26	B26	OSC	OSC	OB	2	25	50
A27	B27	EOT	EOTS	EOT	1	16	41
A28	B28	LP	BOTS	BOT	1	15	40
A29	B29	FP	FPTS	FPT	1	19	44
A30	B30	RW0	REWS	RWG	1	24	49

NOTE: All interface signals are low-true.

SECTION VII

NRZI AND PE TAPE FORMAT

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SECTION VII - NRZI AND PE TAPE FORMAT

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SECTION VII

NRZI AND PE TAPE FORMAT

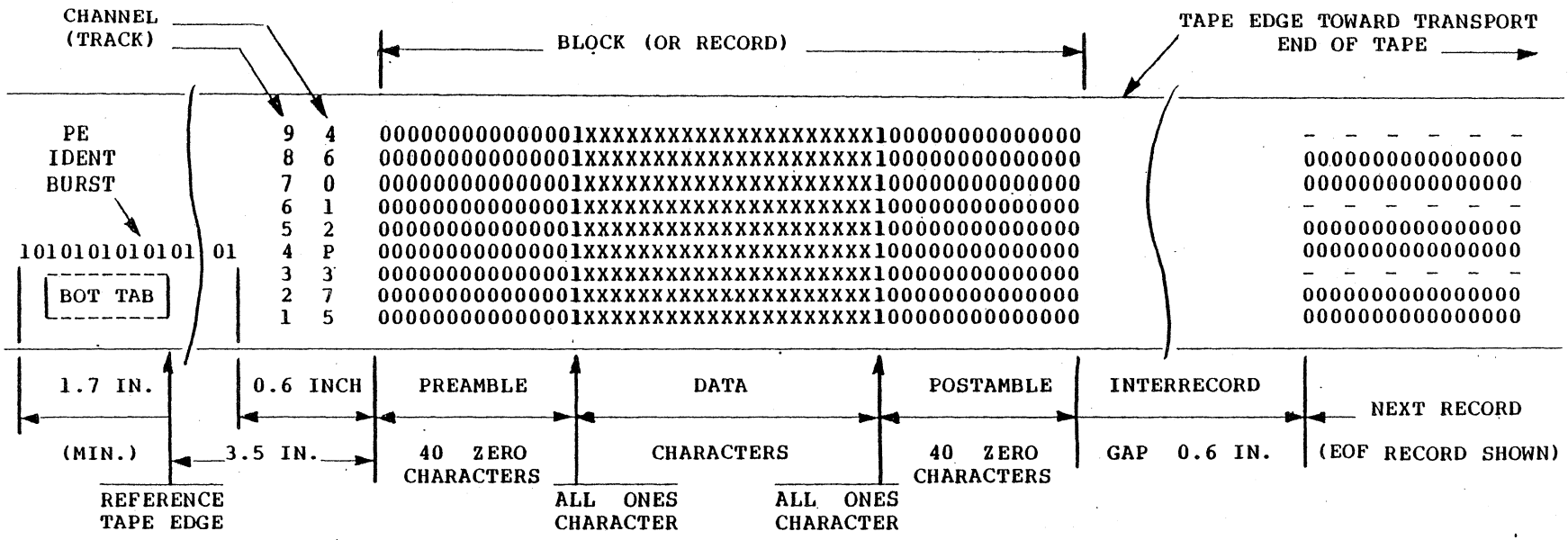
INTRODUCTION

The TAPE DIMENSION III Tape Controller interfaces to industry standard formatted tape drives which write nine bit characters laterally across the tape. While the formatter in the drive is responsible for actually writing the data, this section provides an insight into how the data is formatted on tape. The density of the characters written on the tape is determined by the type of tape unit and (in some cases) the density selection made at the drive and/or the command issued by the CPU. A data block (record) written on the tape consists of data characters and error checking characters (or a preamble and postamble). Every data character consists of the data byte plus an odd parity bit that is generated by the formatter to conform with odd parity as specified by the format. A record (or block) of data on tape represents the data transferred to or from a block of memory in response to one read or write command. Adjacent records are separated by automatically erasing a 0.6 inch segment of tape to form an interrecord gap (IRG).

NINE-TRACK PE FORMAT

The tape controller uses the standard nine track Phase Encoded (PE) 1600 bits per inch tape format. Each tape block contains a preamble, a variable length data field, and a postamble. The 41 character preamble consists of 40 tape characters with all-zero bits followed by one character of all-one bits. The preamble is followed by the data field which also contains an odd vertical parity bit for each data character. Following the last character of the data field is the postamble which contains an all-ones character followed by 40 all-zero characters (the reverse-image of the preamble).

When the tape is at load point (beginning of tape) and the first data block is to be written, it is preceded by an identification burst consisting of alternating one and zero bits in the track for the parity (P) channel. with all other tracks erased. The file mark consists of 40 all-zero characters similar to those in the preamble or postamble, except that the tracks for channels 1, 3 and 4 are erased.



NOTES:

1. Tape shown oxide side up.
2. Channels 0 thrtough 7 contain data in decending order of significance.
3. Parity channel (P) always contains odd data character parity.
4. The PE Identification Burst contains alternating one and zero bits.
5. Data is recorded at 1600 characters per inch.
6. A File Mark is a 40 character burst, with "0" bits in channels P. 0, 2, 5, 6 and 7. Channels 1, 3, and 4 are erased and indicate dead tracks when read back. The EOF is preceded by a normal 0.6 inch gap, and is also separated by any following data record by a 0.6 inch inch gap.

Figure 7-1 1600 BPI PE Tape Format

NINE-TRACK NRZI FORMAT

In the nine-track NRZI format, characters are written on the tape in 800 bits per inch density. Each data character contains eight data bits and one odd vertical parity bit. Following the last data character, the End of Record (EOR) gap (three blank characters) is written, followed by a Cyclic Redundancy Check (CRC) character, followed by three more blank characters, concluded by a Longitudinal Redundancy Check (LRC) character. The LRC character produces an even longitudinal parity in each of the tracks along the length of the tape. Reading or Writing, the tape controller checks to ascertain that the lateral parity of every data character is odd, that the CRC character is correct, and that every track has even longitudinal parity.

The nine-track NRZI file mark consists of a single character record with a one-bit in channels 3, 6 and 7; the remaining channels contain zeros. The CRC character is left blank, but an LRC character is written which is identical to the file mark character.

RECORDING METHODS

NRZI and Phase Encoded formats are recorded on tape, using different recording techniques. In Figure 7-3, NRZI and PE waveforms are compared. The NRZI waveform shows a change in flux polarity for each binary one bit. A binary zero is represented by the absence of a flux change.

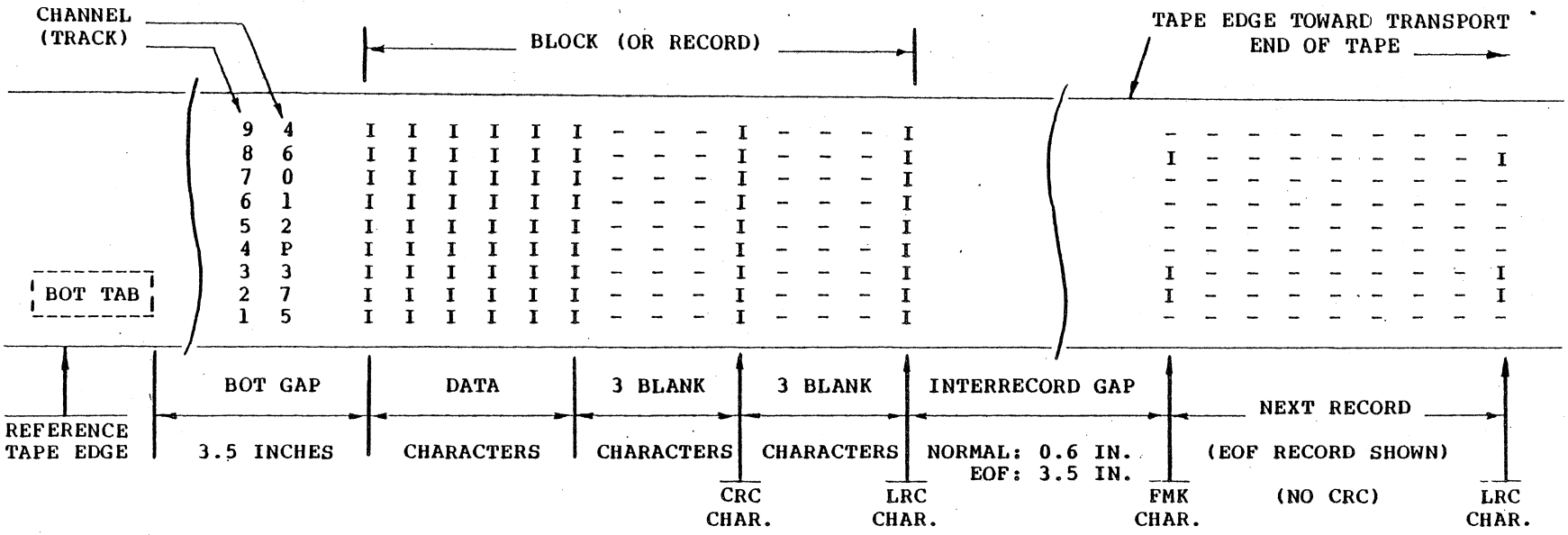
Phase encoded recording requires at least one flux change per bit cell. A binary zero leaves the flux polarized opposite to that of the interrecord gap.

DATA BLOCK SIZE

The maximum data block size is only limited by the Byte/Record Counter to a full 64K byte block. The minimum recommended data block size can vary with the application, depending upon the system where the generated tapes will be used.

END-OF-FILE MARKS

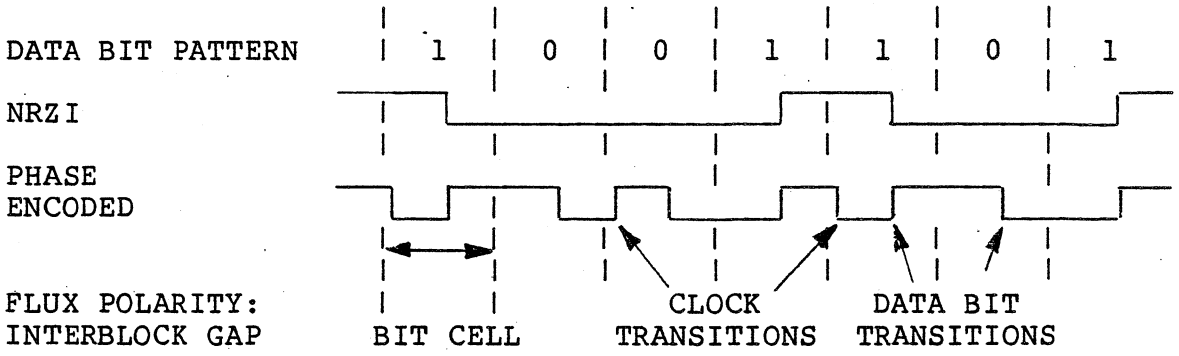
The program can group sets of data records into files. The end of a file is indicated by an End Of File (EOF) mark. The PE File Mark consists of 40 all-zero characters in a special combination of active and dead tracks. The NRZI File Mark is a special record containing only one special data character and its corresponding LRC character. Each EOF in the NRZI format is preceded by an extended record gap.



NOTES:

1. Tape shown oxide side up.
2. Channels 0 thrtough 7 contain data in decending order of significance.
3. Parity channel (P) always contains odd data character parity.
4. Each bit of the LRC ensures even parity for that track, including total of all data and CRC bits. The LRC is never all zero bits.
5. It is possible for the CRC to be all zeros.
6. A File Mark is a single character record, with "1" bits in channels 3, 6 and 7 for both the data character and the LRC. The CRC contains all zeros. The EOF is preceded by a 3.5 inch gap, and is separated by any following data record by a normal 0.6 inch gap.
7. Data is recorded at 800 characters per inch.

Figure 7-2 800 BPI NRZI Tape Format



NOTES:

NRZI: Any change in polarity is a "1" bit. No change in polarity is "0" bit.

PE: Data bit transition in direction of gap polarity is a "1" bit, opposite direction is a "0" bit.

Last transition (LRC) returns flux to gap polarity.

Figure 7-3 PE and NRZI Recording Comparison

TRANSFERS

When writing, the controller divides each computer word into two eight-bit bytes. In reading, the bytes from the tape are reassembled into a full sixteen-bit word for the computer bus.

TAPE-END MARKERS

The ends of the tape contain reflective strips that are detected by photo cells in the tape drive. The Load Point marker identifies the logical Beginning of Tape (BOT) and is positioned to allow at least ten feet of leader at the front of the tape. A Space Reverse or Rewind command automatically stops at this marker. At least three inches of tape are erased between the BOT marker and the first record.

The End of Tape (EOT) marker is located at least 14 feet from the physical end of the tape. The program should not record more than a few feet beyond the EOT marker, allowing at least ten feet of tape for a trailer. A status bit is set and any Space Reverse operations are terminated when the tape passes beyond the EOT marker.

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SECTION VIII

GCR TAPE FORMAT

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GCR TAPE FORMAT

INTRODUCTION

The Group Code Recording method, known as the GCR Format, allows writing and reading magnetic tapes at high density. The higher tape error rate generated by the high density is virtually eliminated by elaborate error detecting and correcting methods inherent in this format.

ANSI COMPATIBILITY

The controller will write and read magnetic tapes as specified by ANSI X3.54-1976. The interface signals required to write and read ANSI compatible tapes must be as specified in Section 7 "GCR Tape Interfaces" and Section 3 "Programming". The following paragraphs clarify certain aspects of GCR operation and format compatibility.

DENSITY

The density of recording is 6250 data characters per inch, nominal.

BLOCK LENGTH

The controller does not control or limit the number of data characters per tape block (within the limits of the byte count) except to disallow the writing of data blocks containing no data characters. The formatter will format the input data, independent of total number of data characters, into the data group and/or residual data group in the ANSI specified format. The controller may generate data blocks outside the ANSI specified minimum length or maximum length, if desired.

MAXIMUM INTERBLOCK GAP (IBG)

The user may generate extended length IBG's by repeated Erase Gap (ERG) commands to the formatter. The user may thus exceed the ANSI specified 15 foot maximum. Upon detecting a 15 foot IBG during read operations, the formatter will halt tape motion and set REJECT status according to Section 6.

END OF RECORDING AREA

The controller reports EOT status, but does not control or limit operations past EOT (in the End of Recording Area).

RECORDING FORMAT

The GCR recorded format is described by the diagrams and text in the remainder of this section.

Identification Burst - The GCR recording method is identified by a burst of PE recording on track 6 with all other tracks erased. The ID Burst starts at least 1.7 inches before the trailing edge of the BOT marker and continues past the BOT marker.

ARA Burst - The Automatic Read Amplification Burst is used by some drives to initialize their Dynamic Amplitude Control. The burst begins at least 1.5 inches but not farther than 4.3 inches from the leading edge of the BOT marker. The ARA Burst is written at 9042 fci and consists of the ARA ones-burst and the ARA ID burst.

ARA Ones-Burst - An undefined gap separates the ID Burst from the ARA ones-burst (all-ones in all tracks). The length of this burst is approximately 5 to 10 inches.

ARA ID Burst - The all-ones pattern continues with tracks 1,4, and 7 erased during the ID Burst. The ID Burst is approximately 2 inches long. A normal IBG follows.

IBG - The interblock gap is 0.3 inches, nominal. The IBG immediately preceeding the tape mark is 3.3 inches, nominal.

Tape Mark - The Tape Mark consists of 250 to 400 flux changes recorded at 9042 fci, with tracks 3, 6, and 9 erased.

Data Blocks - (Described in detail below.)

Preamble - Sixteen subgroups of five bytes each. The subgroups initiate the Read Circuits and synchronize them to the data coming from tape

Terminator Control Subgroup - The data pattern in this subgroup provides for long wave length inputs into the read circuits at the beginning of a Read operation. These inputs in turn ensure that the Read Detectors are turned on before they are synchronized.

The Terminator Control subgroup consists of a set of nine parallel 5-bit serial values of 10101 in all tracks located at the BOT end of each block, and 1010L at the EOT end of each block where L represents the resetting of the last character (which restores the Write Triggers to the erase state).

Second Control Subgroup - This subgroup is an important part of the synchronization process. The Second Control Subgroup consists of five bit serial values of 01111 in all tracks for the BOT end of the block and 11110 for the EOT end of the block.

Sync Control Subgroups - these are fourteen five-byte subgroups which synchronize the Read Reference Oscillator. Each subgroup consists of five-bit serial values of all ones in all tracks.

Mark 1 - This subgroup marks the coming of data. It ensures that the buffer counters are properly initiated so the data being read is formatted into the correct five-byte groups. This is necessary for correct decoding (translation from five to four bit codes) of the data which is being read. The Mark 1 control Subgroup is a set of five-bit serial values of 00111 on all tracks. During Backward operations, the Mark 1 looks like the Mark 2 Subgroup.

Data - The Data section of the tape has only data and the ECC recorded on it (no Control Subgroups). The data is divided into groups and the groups are divided into subgroups. These data subgroups are identified as data subgroup A and data subgroup B.

Data subgroup A consists of four data bytes before translation into the storage group. The same is true for data subgroup B except that it is made up of three data bytes and one ECC (Error Correction Character) before translation. The ECC is used for data correction within the eight-byte data groups (byte 8 is the ECC).

Data Values/Record Values - After the ECC is mathematically generated from the group of seven data bytes, the parity bits are also added and the resulting eight characters are divided into two groups of four characters each. During GCR recording, The four-bit pattern for each tape channel is translated into a five-bit pattern for storage on tape. These storage patterns assure that there are no more than two successive zeros in any track, a feature that provides more reliable synchronism of the read circuits. During a Read operation, the five-bit code is converted to the original four bits. Thus, the data sent to the CPU is in its original form.

Resync Burst - There may be no more than 158 contiguous data groups (1106 data bytes) in a recorded data block. Then, if there are more than six data bytes (before translation) remaining in an incoming record, a Resync Burst must be added before more data groups can be recorded. This burst is used to resynchronize the data of failing tracks when a data record is longer than 1112 bytes of data (before translation).

Mark 2 - This subgroup marks the end of data and the coming of non-data information. The Mark 2 Control Subgroup consists of a set of five-bit serial values of 11100 on all tracks. On Backward operations, the Mark 2 looks like the Mark 1 Subgroup.

End Mark - This control subgroup warns of the approach of the Residual Data Group, which is defined below. The End Mark Control Subgroup consists of one set of five-bit serial values of 11111 on all tracks.

Residual Data Group - This group is formed when there are six or fewer data bytes remaining in a data record. If six data bytes remain, the seventh byte of the Residual Data Group is the Auxiliary CRC Character (a data validity check character) and byte eight is the normal ECC. If there are fewer than six residual data bytes, pad characters of all zeros (with correct parity) are added to the data group to pad it to six bytes. (All data groups must have eight bytes total in GCR mode.) Thus, the Residual Data Group consists of remaining data bytes and/or the pad characters (H), the Auxiliary CRC Character (N) and the ECC character (E).

CRC Data Group - The CRC character has odd parity if there was an odd number of data groups and would normally have even parity if there was an even number of data groups. Since an even parity byte is not allowed in a GCR Data Group, the CRC Character must be made odd. To accomplish this, an additional pad byte consisting of all zeros and a parity bit (B) is added to the record. The addition of this byte changes the number of bytes in the CRC generation and provides an odd parity CRC Character.

The next five bytes of the CRC Data Group are identical CRC Characters. The additional CRC Characters serve to fill the CRC Data Group, since no more data will be written.

Next in the CRC Data Group is the Residual Character (X). This character is defined and used as a record data counter. (Bits 3-7 are a modulo 32 count.) These bits are used by some drives in a proprietary manner (pointers for internal data buffering in the subsystem). Bits 0-2 are used as a Modulo 7 counter to indicate how many of the Residual Data Group bytes are data bytes. The modulo 7 count of the Residual Character indicates how many data bytes are to be retrieved from the Residual Data Group.

The ECC in this data group (E), as in all other data groups, is used to verify the correctness of data in the group and to isolate any error, and to correct bad data during read operation.

Postamble - The Postamble is essentially the mirror image of the Preamble In Read Backward operations, the Postamble is used the same way the Preamble is used in Read Forward operations. (Refer to the description of the Preamble above.)

Check Characters - Three Check Characters are used in the GCR tape format: CRC (B), Auxiliary CRC (N), and ECC (E).

The CRC Characters are used to verify data validity during writing and reading operations. The ECC is used to to verify data validity and for Data Error Identification and Correction.

TAPE MARK BLOCK

The Tape Mark written is 250 to 400 flux changes (all "ones") at 9042 fci in zones 1 and 2 (physical tracks 1/4/7 and 2/5/8, respectively) and no recording in zone 3 (physical tracks 3/6/9).

A tape mark will be detected on reading if sufficient contiguous characters in either zone 1 or zone 2, in conjunction with zone 3, contain their appropriate format.

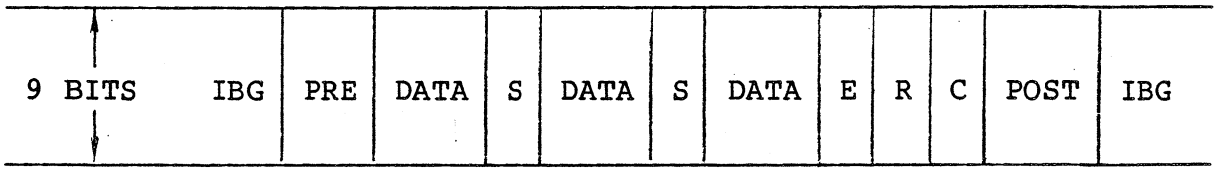
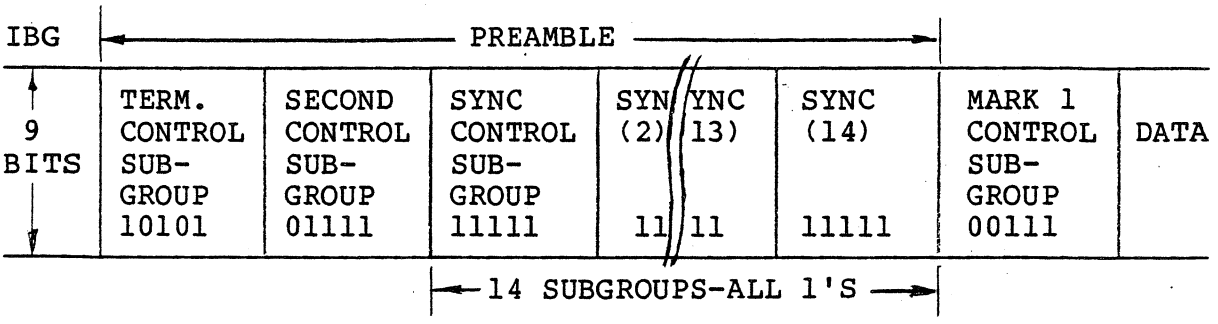


Figure 8-2 GCR Data Block Format



Mark 2 + Postamble (POST) is reverse image of Preamble + Mark 1

Figure 8-3 GCR Preamble and Mark 1 (PRE)

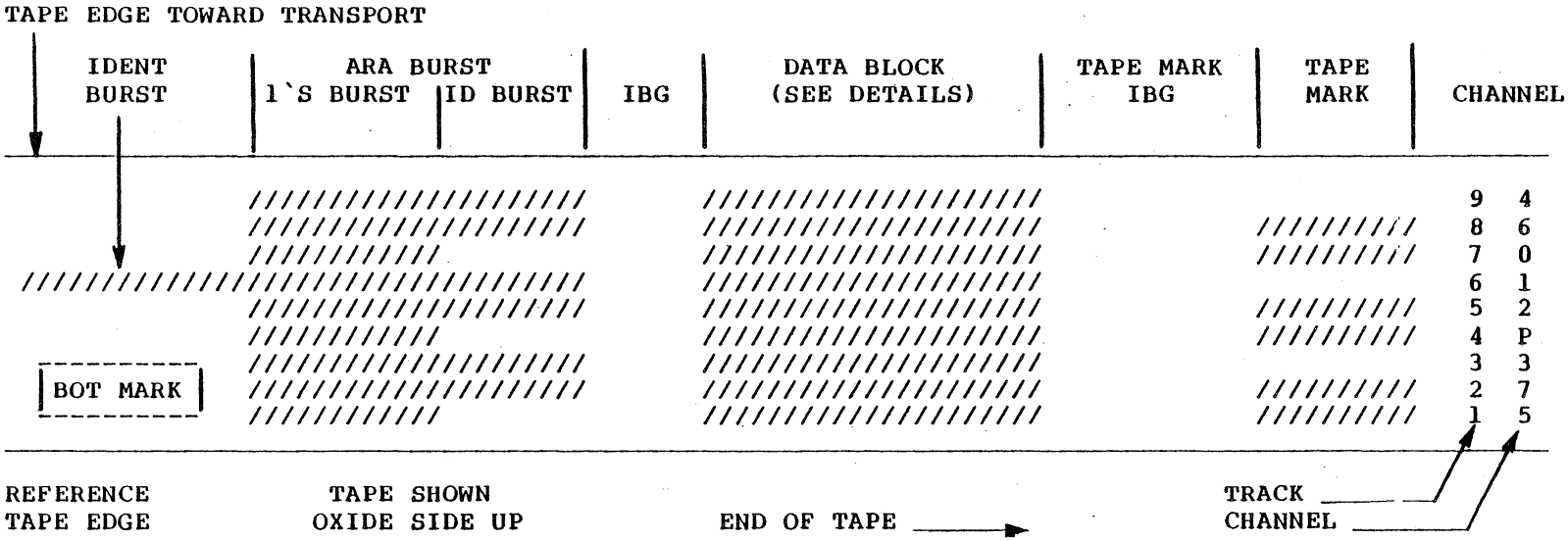


Figure 8-1 6250 BPI GCR Tape Format

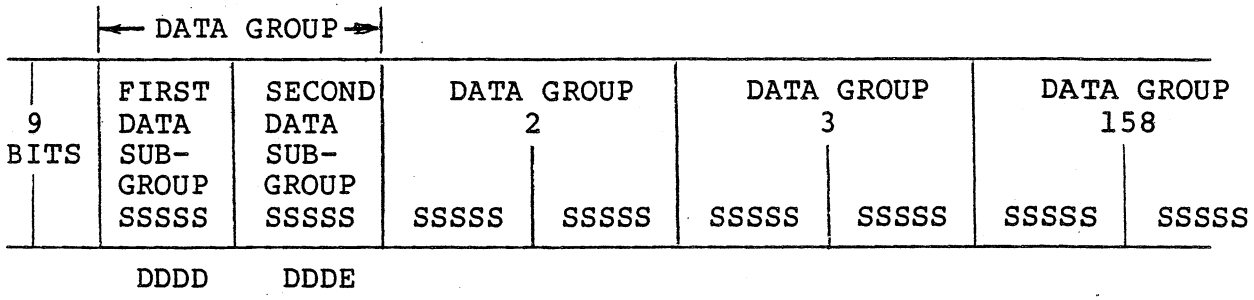


Figure 8-4 GCR Data Groups (DATA)

DATA VALUES	STORAGE VALUES
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111

Figure 8-5 Stored Data Translation

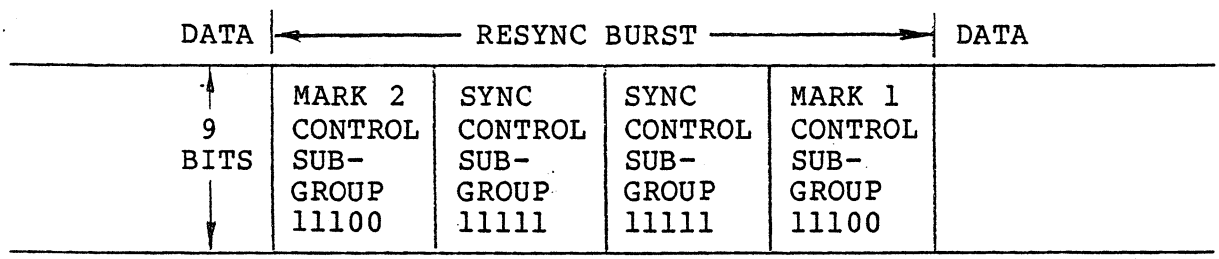


Figure 8-6 Resync Burst (S)

DATA	(E)	(R)		(C)		
↑ 9 BITS ↓	END MARK SUB-GROUP 11111	RESIDUAL DATA SSSSS	RESIDUAL GROUP SSSSS	CRC DATA SSSSS	CRC GROUP SSSSS	POST
		HHHH	HHNE	BCCC	CCXE	

H - RESIDUAL DATA OR PAD CHARACTER (ZEROS)
N - AUXILIARY CRC CHARACTER
E - ERROR CORRECTION CODE (ECC) CHARACTER
B - CRC OR PAD CHARACTER
C - CYCLIC REDUNDANCY CHECK (CRC) CHARACTER
X - RESIDUAL CHARACTER

Data/Pad/CRC/ECC are encoded into two data groups of ten stored bytes each.

Figure 8-7 End Mark/Residual Group/CRC Group

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WARRANTY

WESTERN PERIPHERALS warrants articles of equipment manufactured by it to be free from defects in materials and workmanship under normal use and service, its obligation under this warranty being limited to making good at its factory any article of equipment which shall within one year after delivery of such article of equipment to the original purchaser be returned intact to it, or to one of its authorized service stations, with transportation charges prepaid, and which its examination shall disclose to its satisfaction to have been thus defective. This warranty is expressly in lieu of all other warranties expressed or implied and of all other obligations or liabilities on its part, and **WESTERN PERIPHERALS** neither assumes, nor authorizes any other persons to assume for it, any other liability in connection with the sale of its products.

This warranty shall not apply to any article of equipment which shall have been repaired or altered outside the **WESTERN PERIPHERALS** factory or authorized service stations, nor which has been subject to misuse, negligence or accident, incorrect wiring by others, or installation or use not in accordance with instructions furnished by the manufacturer.