

LAL	Rev.	Description	Chk	Date	Approved
	A	ENGRG RELEASE	RF	3-4-76	RF
	B	REVISED	BN	6-16-76	RF
	C	M/L ITEM 45 WAS 10K P/N 116447-103. SH 9 R1 WAS 10K.	BN	9-28-76	RF
X	D	M/L ITEM 20 P/N 74S86 WAS 7486, ITEM 37 2200 pF P/N DC-222K WAS 820 pF, P/N DC821. ADDED ITEM 45,50, & 51. ITEM 57 P/N 514-AG11D WAS 514-AG10D, ITEM 58 P/N 516-AG11D WAS 516-AG10D. SH 9 REVISED LOGIC DIAGRAM. SH 2 ADDED NOTE 3.	BN	3-8-77	RF
X	E	DELETED NOTE 1 & NOTE 3	BN	5-16-78	RF

ENGINEERING  
RELEASE

THIS DOCUMENT CONTAINS 23 SHEETS.

Dist Code SPG

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	1. Tolerances .XX ±.03      Angular ±½° .XXX ±.010 2. Break All Sharp Edges .010 Approx. 3. Mach. Surfaces <input checked="" type="checkbox"/> 4. All Dim. in Inches	Check <i>[Signature]</i> 3-3-76	Title <b>ALTO II</b>		
		Appr. <i>[Signature]</i> 3-3-76	ASSEMBLY, PRINTED WIRING- ETHERNET		
		Material			
Model No. First Use <b>ALTO II EWO7YF92</b>	Finish	Code Ident. <b>18338</b>	Size <b>A</b>	Dwg. No. <b>216323</b>	Change Letter <b>E</b>
Next Assy. First Use <b>216302</b>		Scale -	Do Not Scale Drawing	Sheet <b>I</b>	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ~~THE FOLLOWING MODIFICATIONS HAVE TO BE MADE TO THIS ASSEMBLY USING "B" REVISION PRINTED WIRING BOARDS:~~

- ~~CUT ETCH BETWEEN~~
- ~~1) A47-12 AND A50-2~~
  - ~~2) A50-2 AND A60-5~~
  - ~~3) A50-13 AND A54-6~~

- ~~ADD WIRE FROM~~
- ~~1) A47-4 TO A60-5~~
  - ~~2) A54-6 TO A60-5~~
  - ~~3) A50-2 TO A64-6~~
  - ~~4) A64-4 TO A77-7~~
  - ~~5) A64-5 TO A75-6~~
  - ~~6) A50-13 TO EC PIN 76~~

2. ASSEMBLE PER ALTO II MODULE ASSEMBLY SPECIFICATION, DWG NO. 216207.

3. ~~THE FOLLOWING MODIFICATIONS ARE REQUIRED ON THIS ASSEMBLY USING "B" REVISION PRINTED WIRING BOARDS:~~

- ~~1) CUT ETCH BETWEEN C104 AND FEED THRU (COMPONENT SIDE) (CONNECTS TO A67-3).~~
- ~~2) ADD 10<sub>Ω</sub> RESISTOR (R18) FROM C104 TO FEED THRU (CONNECTS TO A67-3).~~
- ~~3) ADD 470<sub>Ω</sub> RESISTOR (R19) FROM C104 TO END OF R13.~~

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Title  
**ASSY, PRINTED WIRING  
 ETHERNET**

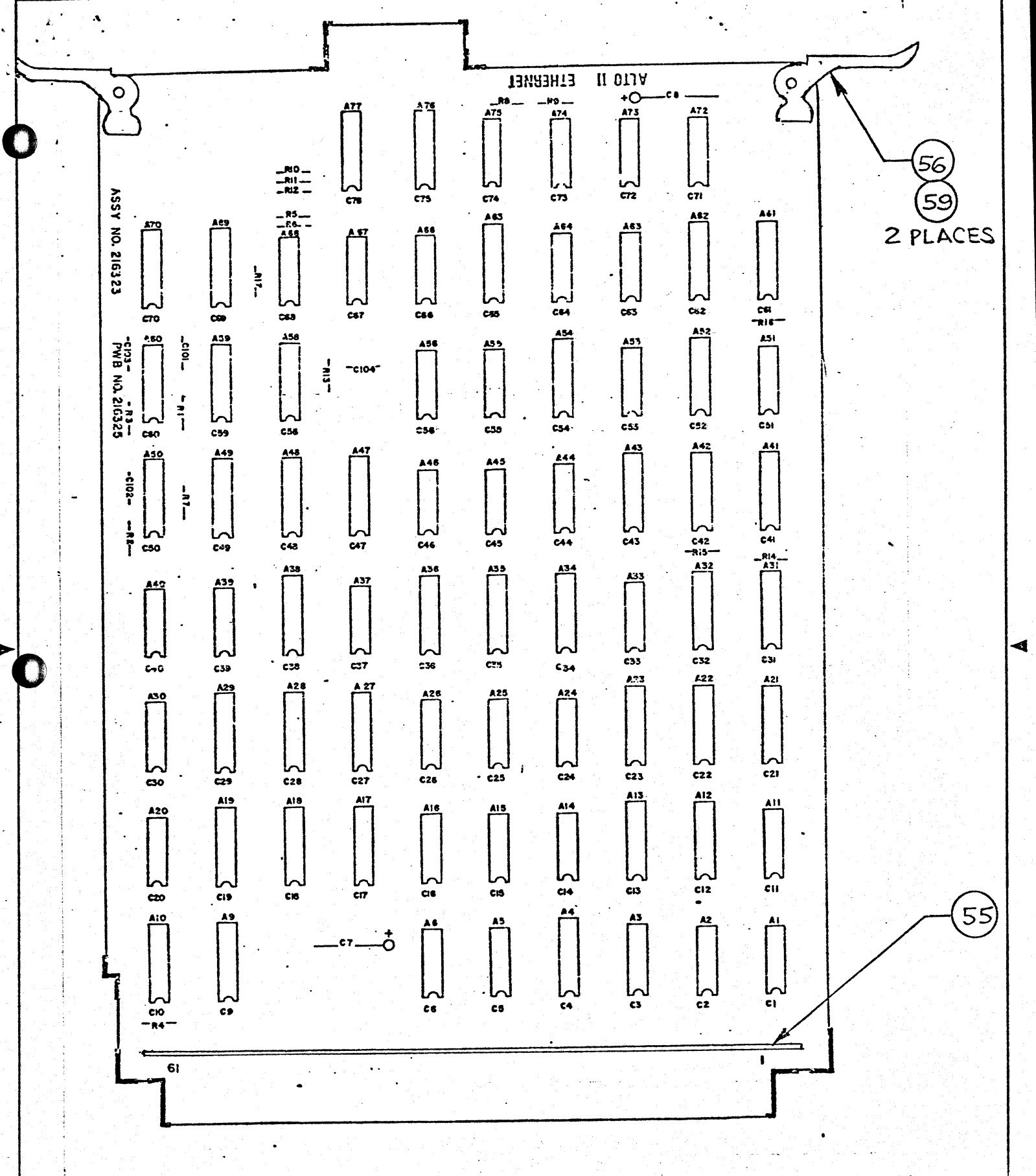
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 ETHERNET**

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216323		
Sheet	3	Of
		E

**Material List**

<b>ML</b>	Drawing No. <b>216323</b>	Rev. <b>E</b>
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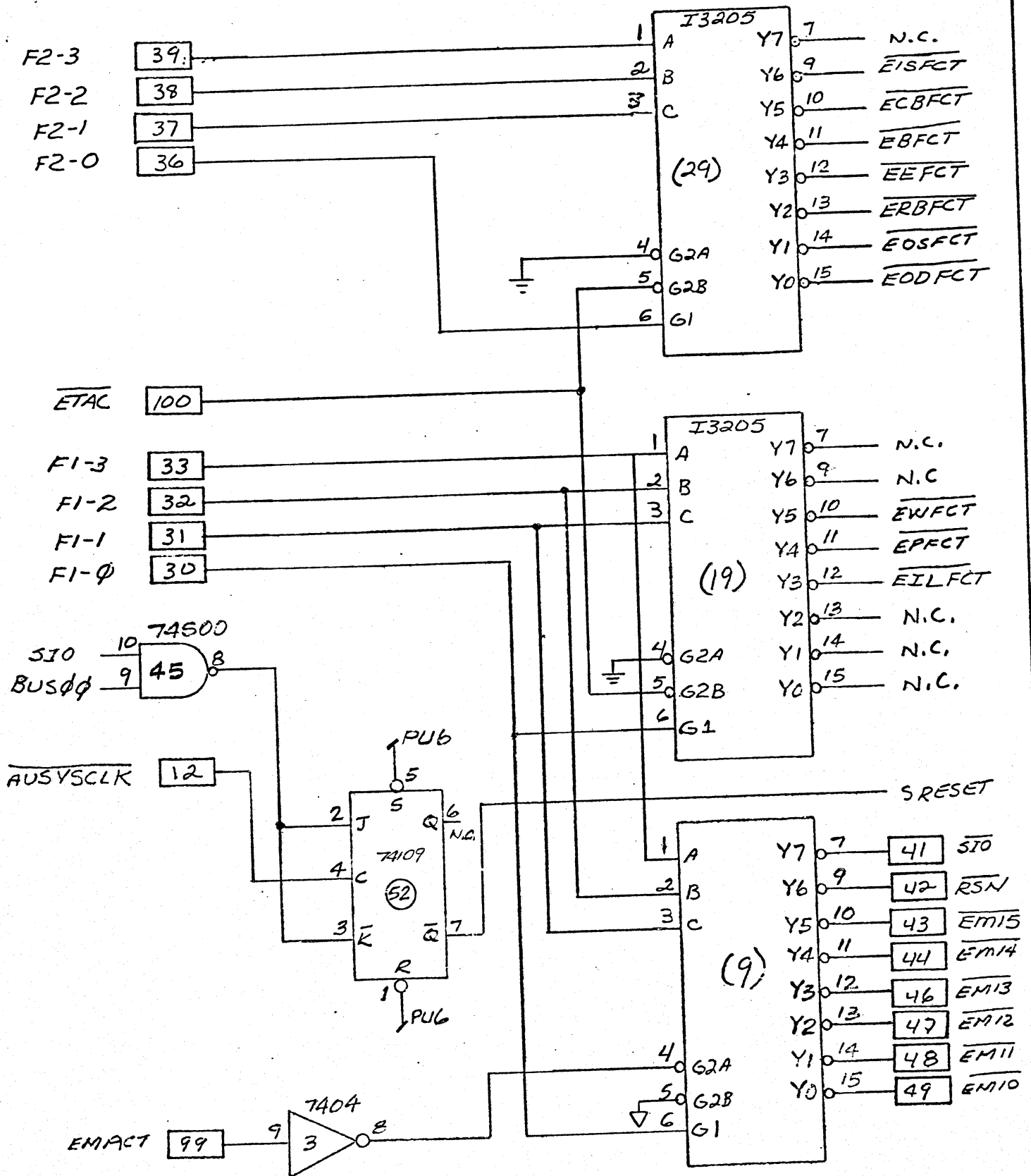
Rev.	Drawing Title <b>ALTO II</b>
Drawing No. <b>216323</b>	<b>ASSEMBLY, PRINTED WIRING- ETHERNET</b>

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Model No. <b>EWO 7YF92</b>	Date <b>3-3-76</b>	Sheet <b>4 of</b>
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Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
1	Board, P.W. Ethernet	216325	1	
2	Procedure, Test	216324	REF	
3	Spec, Module Assembly	216207	REF	
4	Microcircuit, 74H21		2	A1, 39
5	7408		3	A63,64,68
6	7404		3	A3, 44, 55
7	74H01		1	A30
8				
9	7437		1	A73
10	74LS298		4	A13,17,23,27
11	7400		2	A20,46
12	74164		2	A33,37
13	74165		2	A34,36
14	7402		2	A40,72
15	74174		1	A43
16	74157		2	A48,54
17	74123		2	A50,60
18	7410		2	A56,74
19	74161		2	A58,59
20	74S86		1	A67
21	74S08		1	A2
22	7438		8	A5,6,14,15,16,24,25, <sup>26</sup>
23	74S37		1	A11
24	74S00		3	A45,75,66
25	74S157		1	A76
26	898-1-R1.OK Beckman		3	A4,32,38
27	I3205 Intel		3	A9,19,29
28	I3101A Intel		4	A12,18,22,28
29	P3601 M.I.L. OR TN473		3	A41,42,49
30	Microcircuit, 9401 Fairchild		1	A53
31	Microcircuit, 74109		13	A10,21,31,35,47,51, 52,61,62,65,69,70,77





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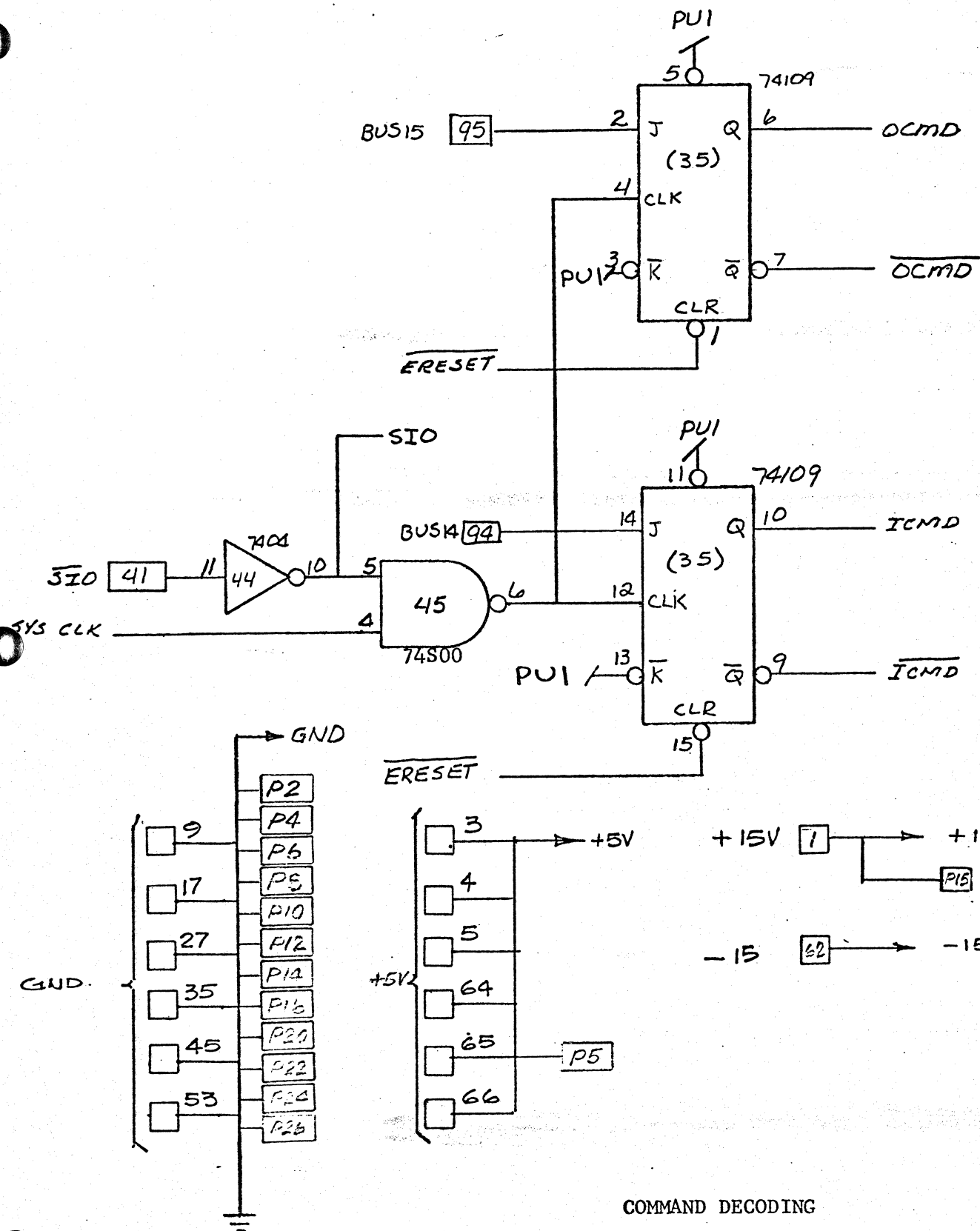
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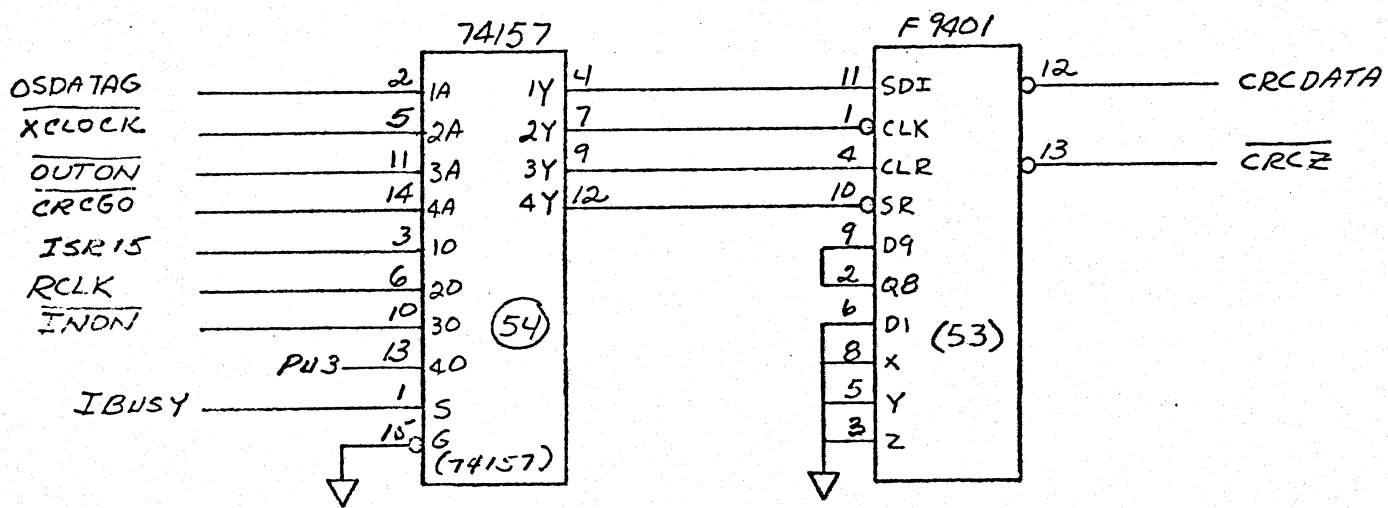
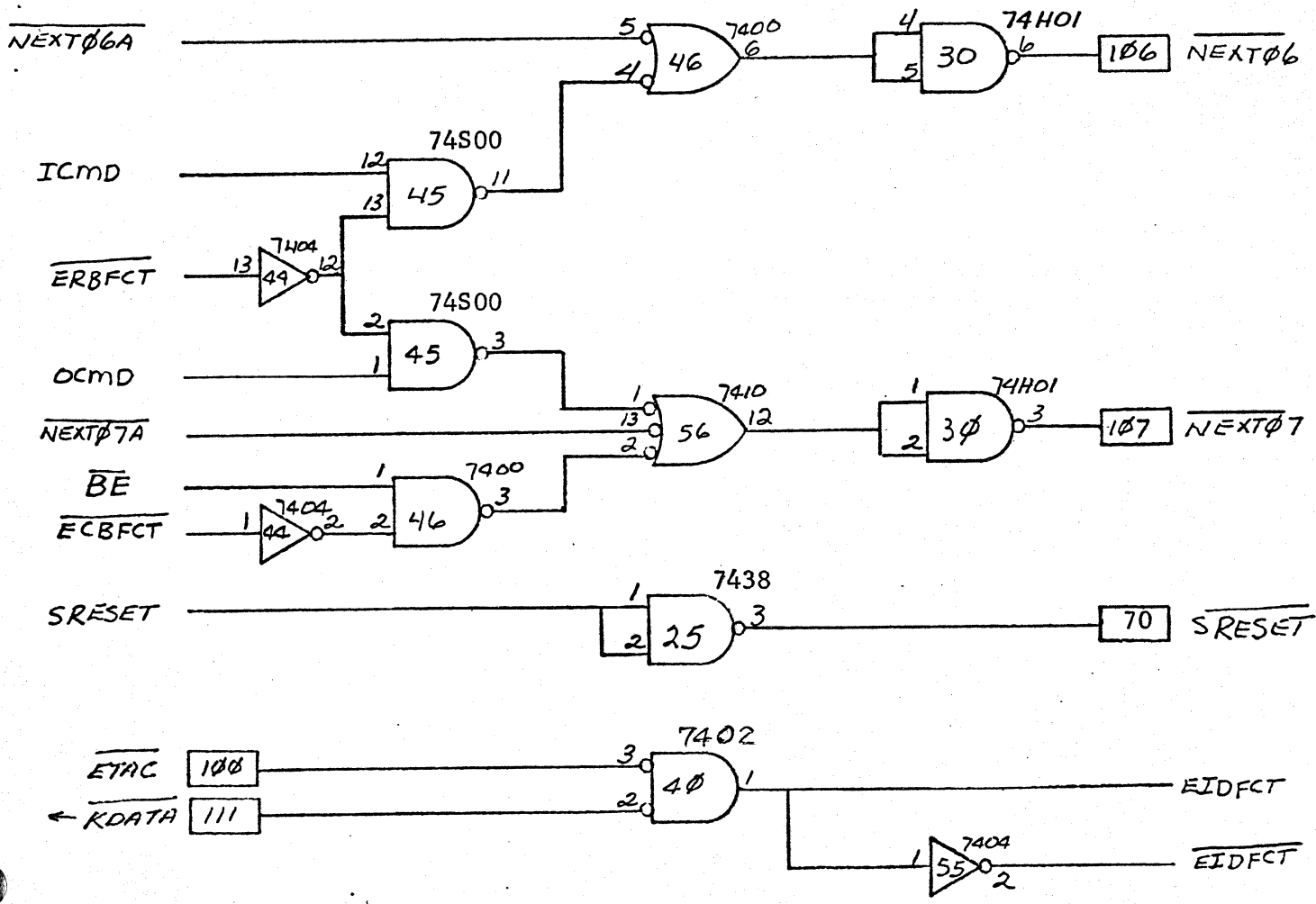


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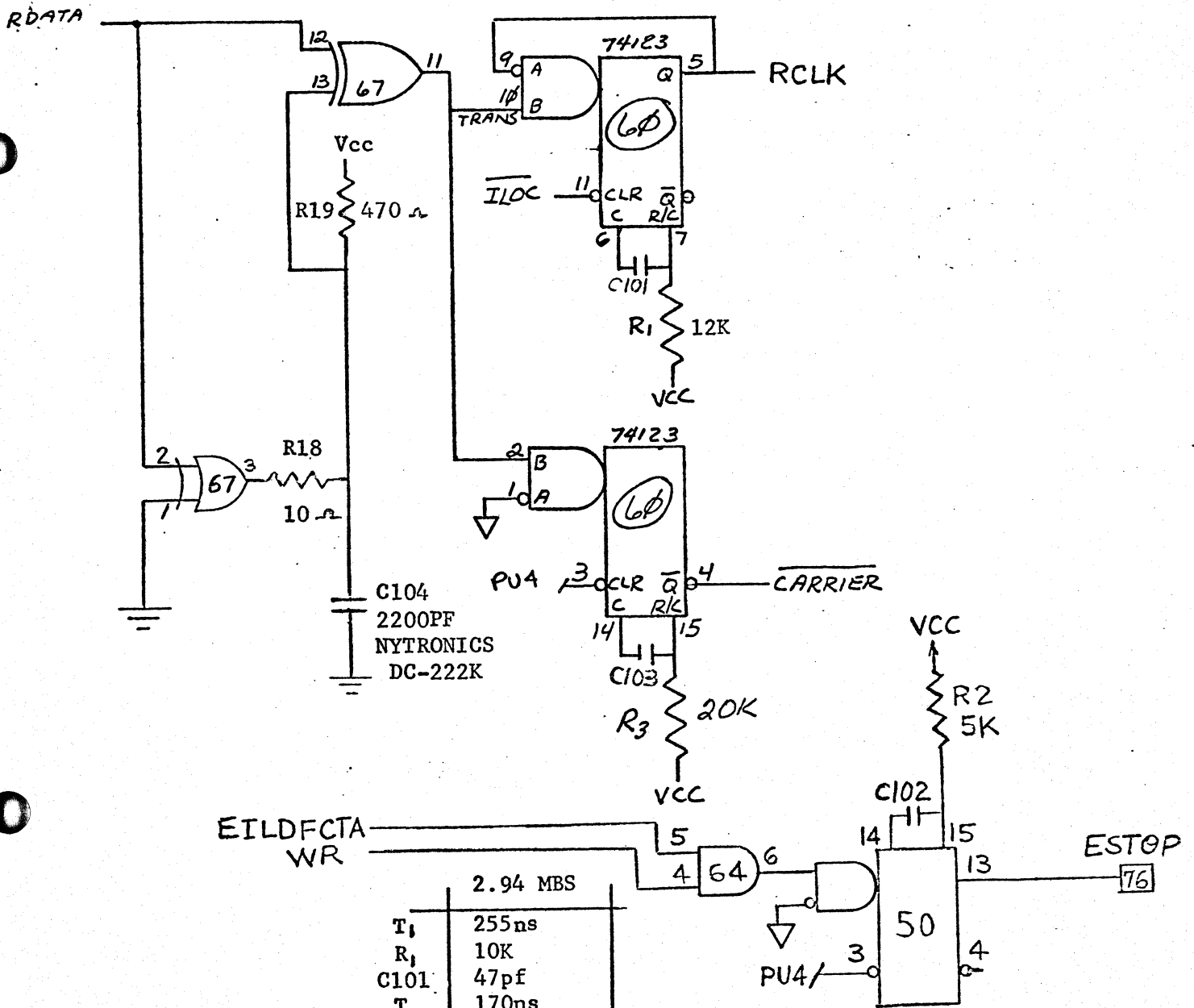
BRANCH LOGIC

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EILDFCTA  
WR

	2.94 MBS
T <sub>1</sub>	255ns
R <sub>1</sub>	10K
C101	47pf
T <sub>2</sub>	170ns
R <sub>2</sub>	5K
C102	68pf
T <sub>3</sub>	425ns
R <sub>3</sub>	20K
C103	39pf
C104	2200Pf
R18	10 Ω
R19	470 Ω

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ASSEMBLY, PRINTED WIRING  
ETHERNET

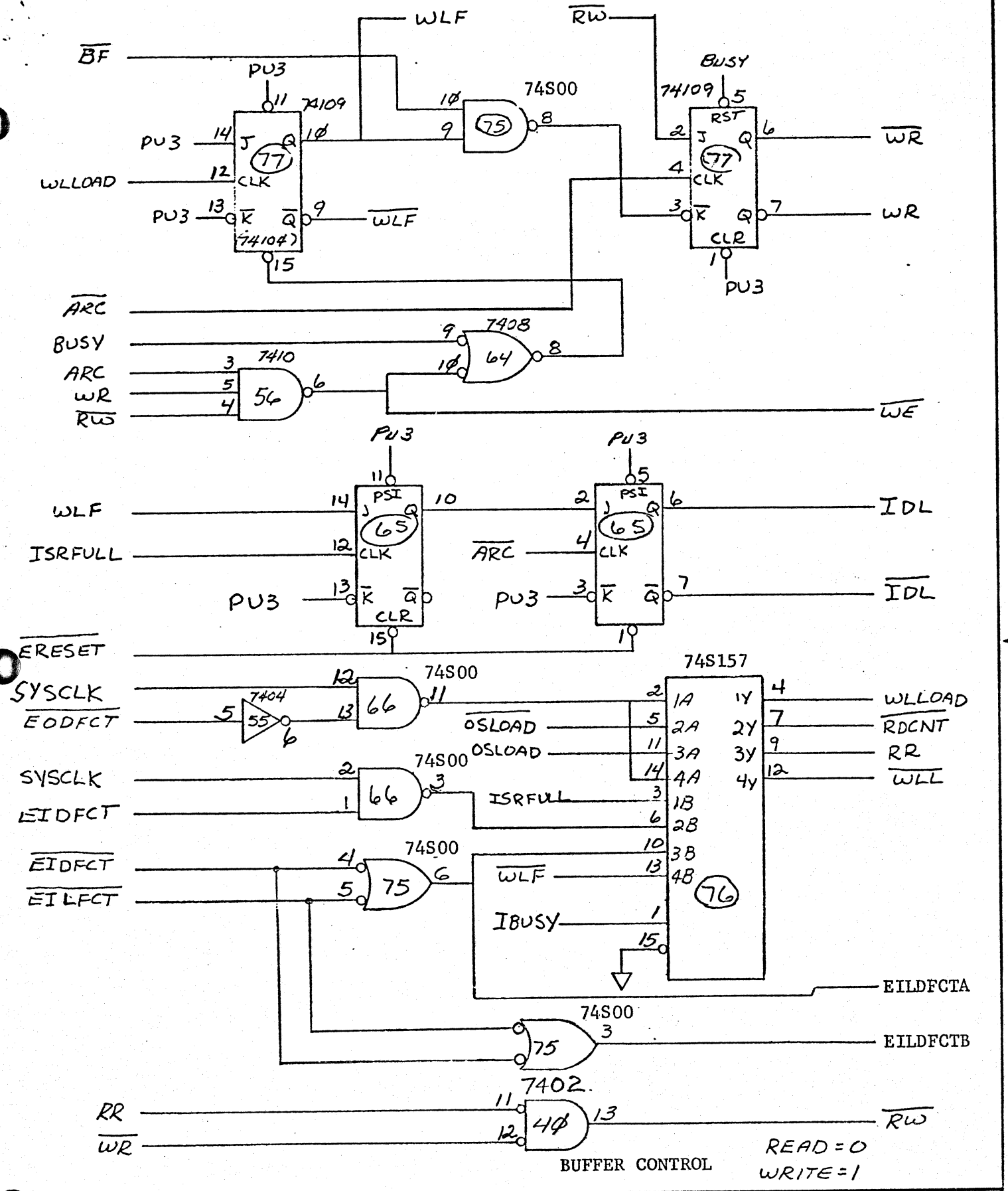
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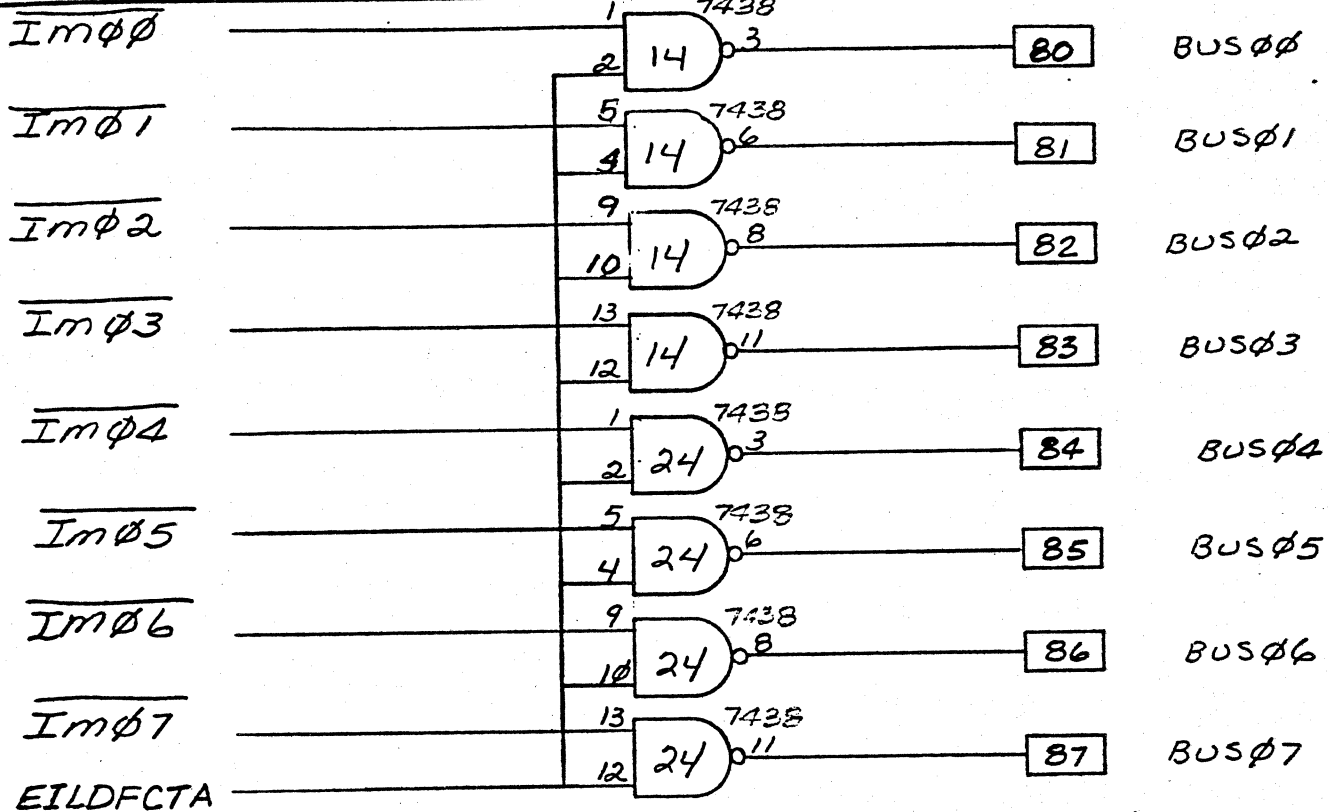


BUFFER CONTROL  
 READ = 0  
 WRITE = 1

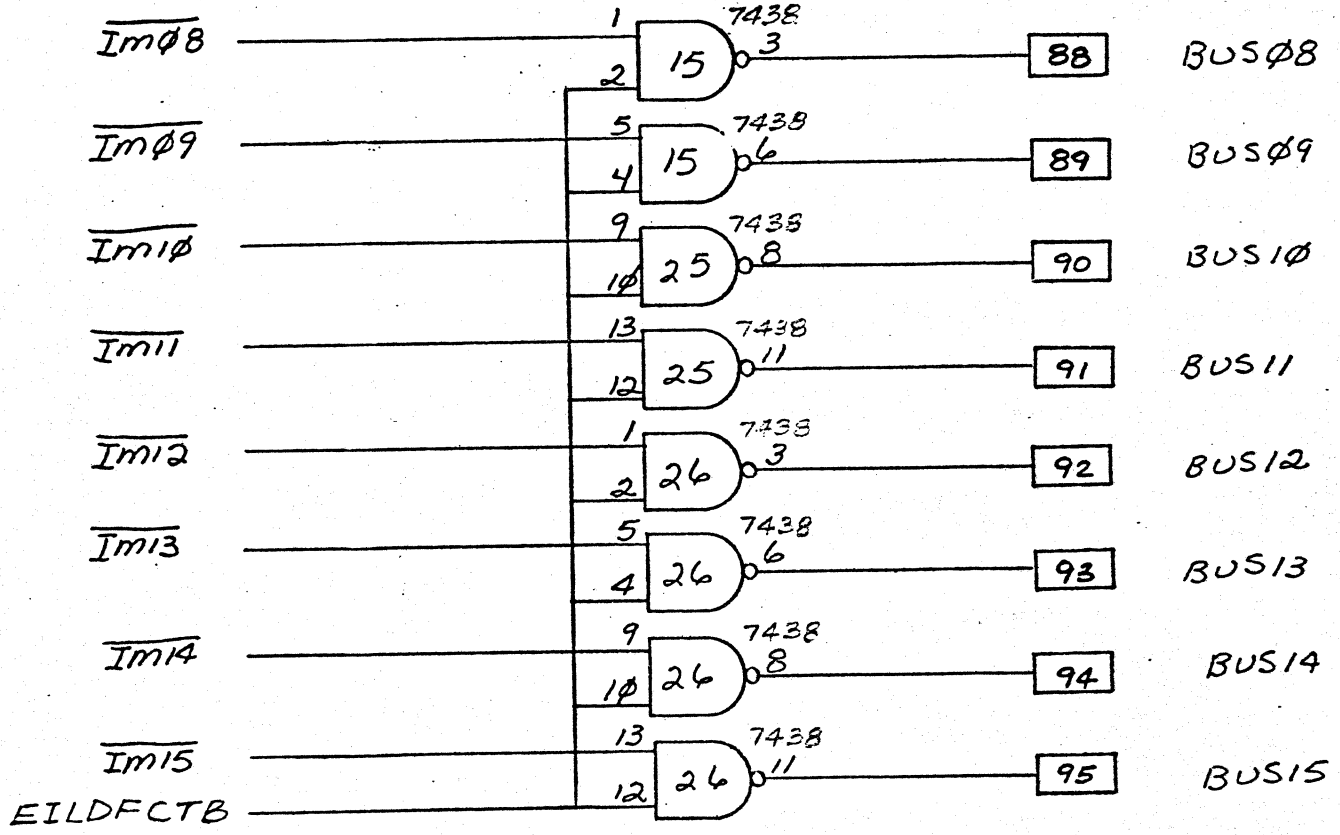
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74H01

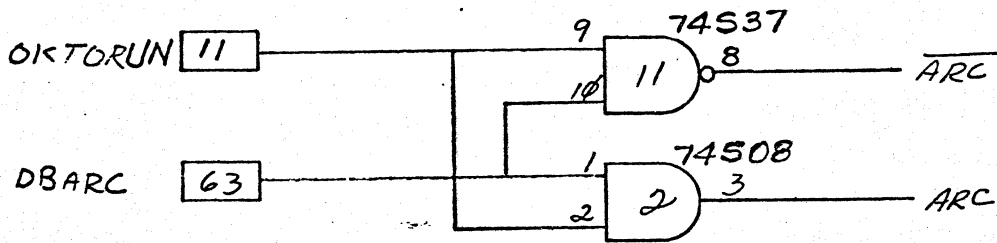
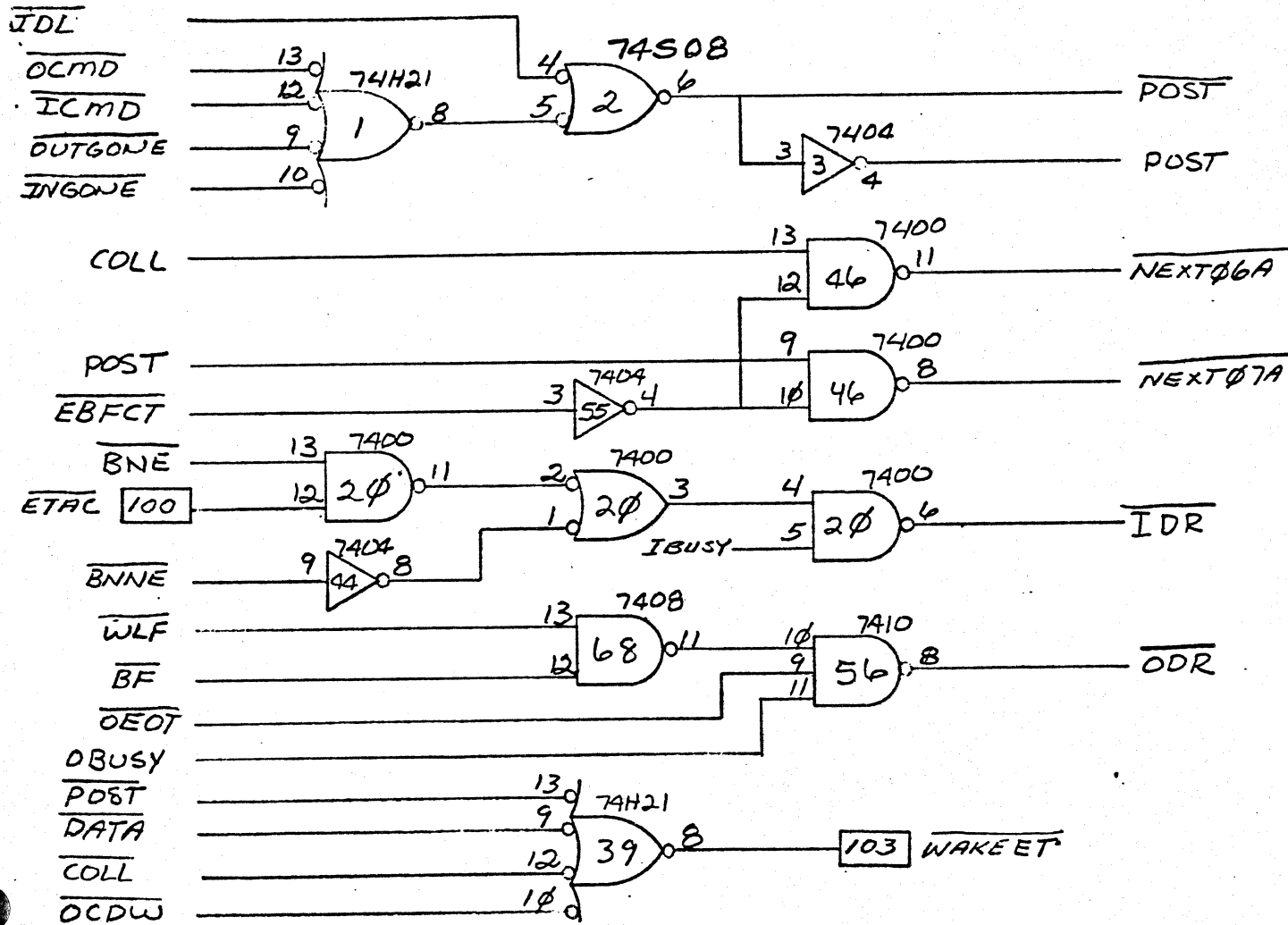


PROCESSOR BUS DRIVERS

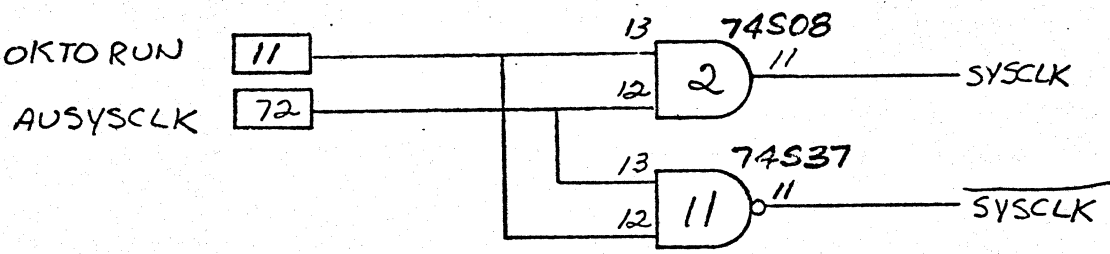
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NEXT 67	WAKEUP TYPE
00	DATA (CDW)
01	POST
10	COLL
11	POST

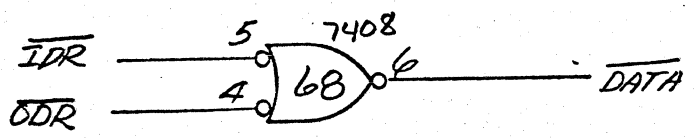
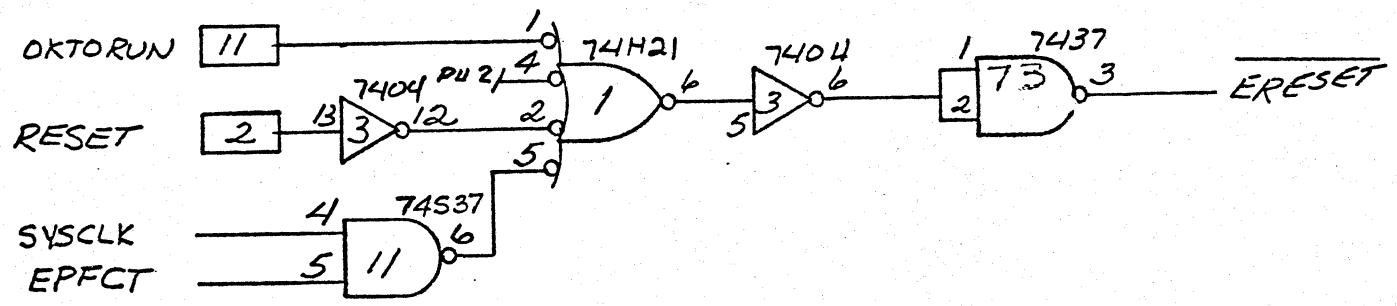
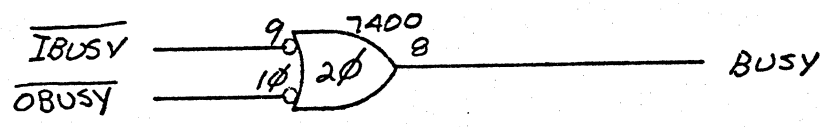
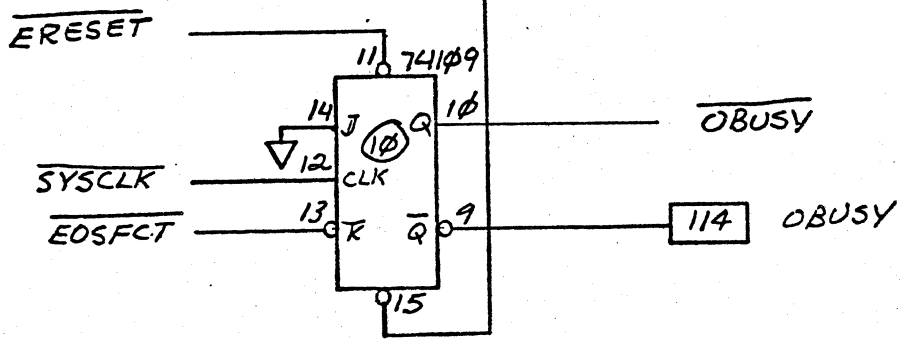
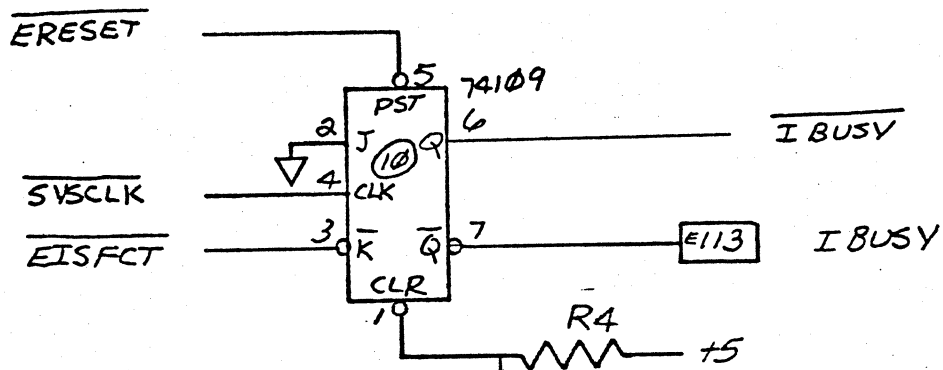


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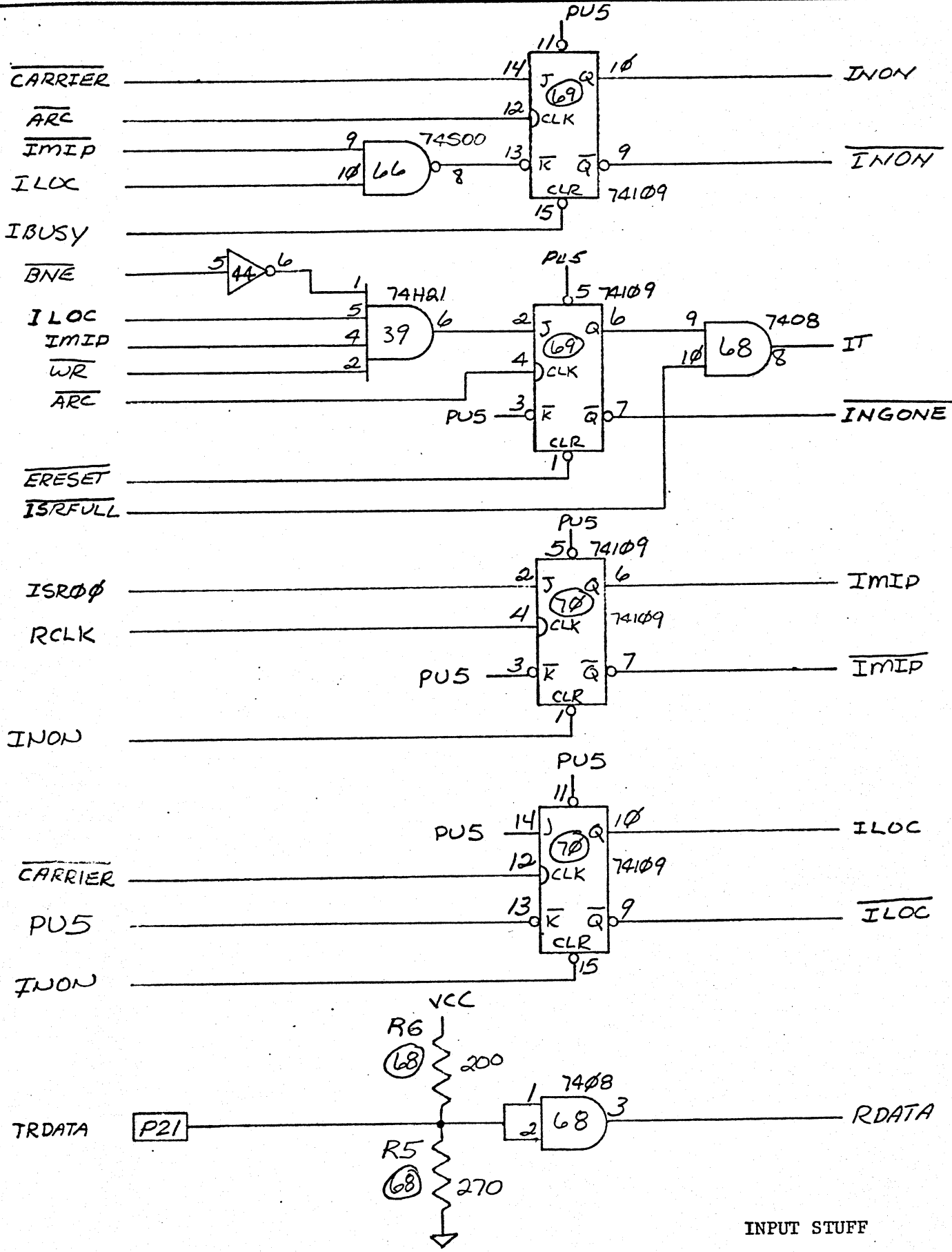


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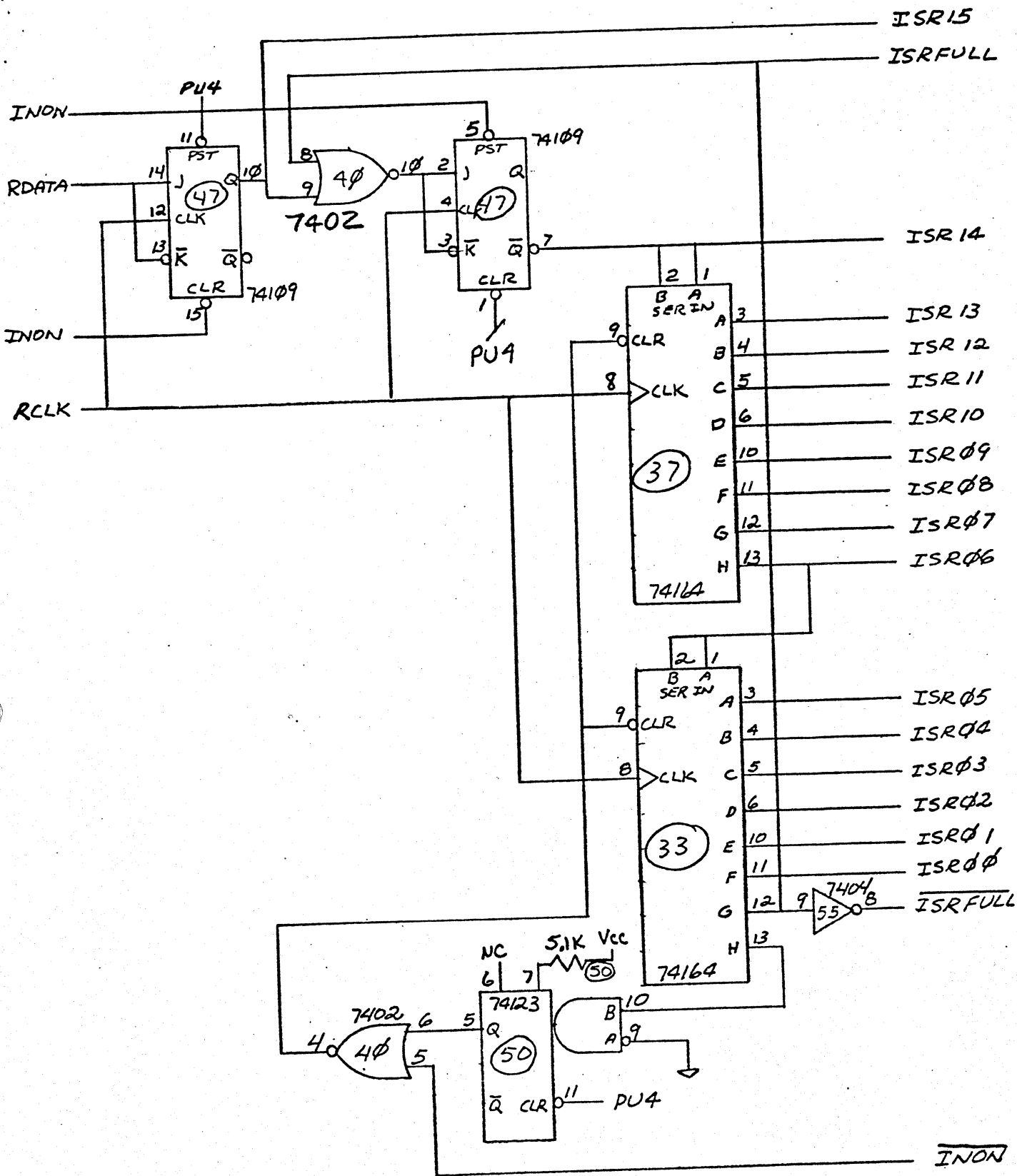
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INPUT SHIFT REGISTER

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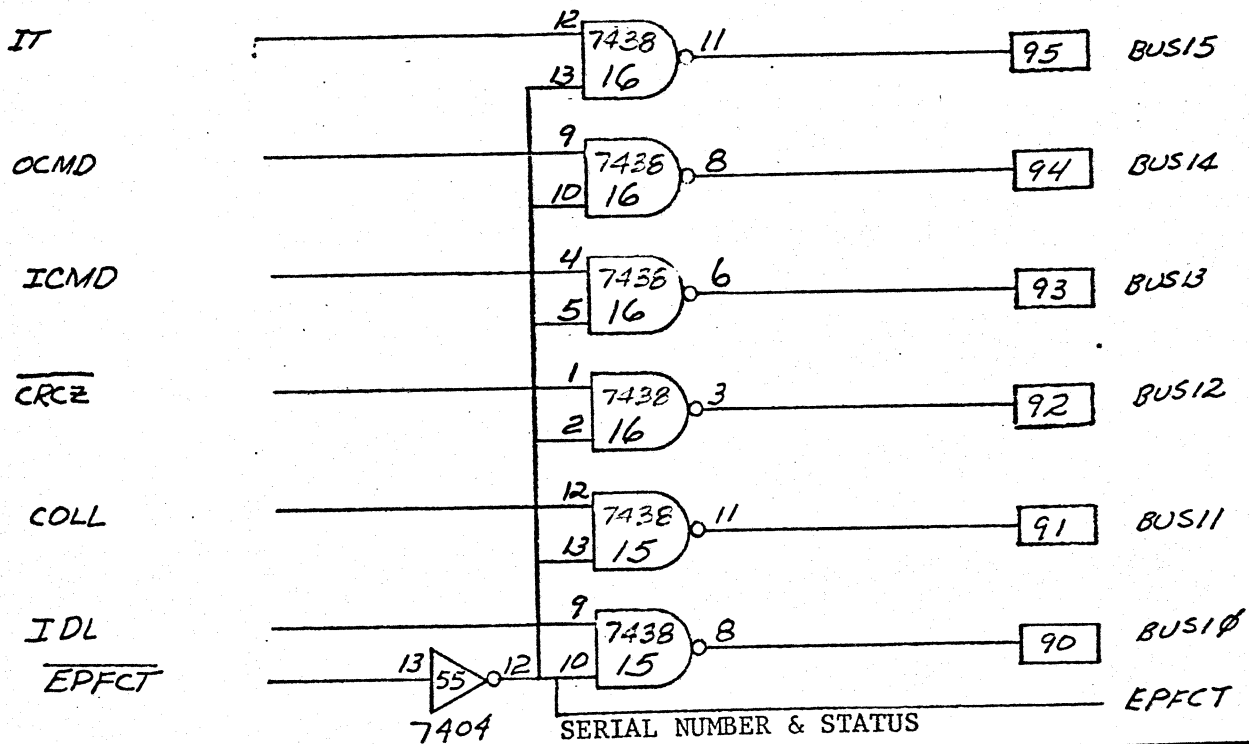
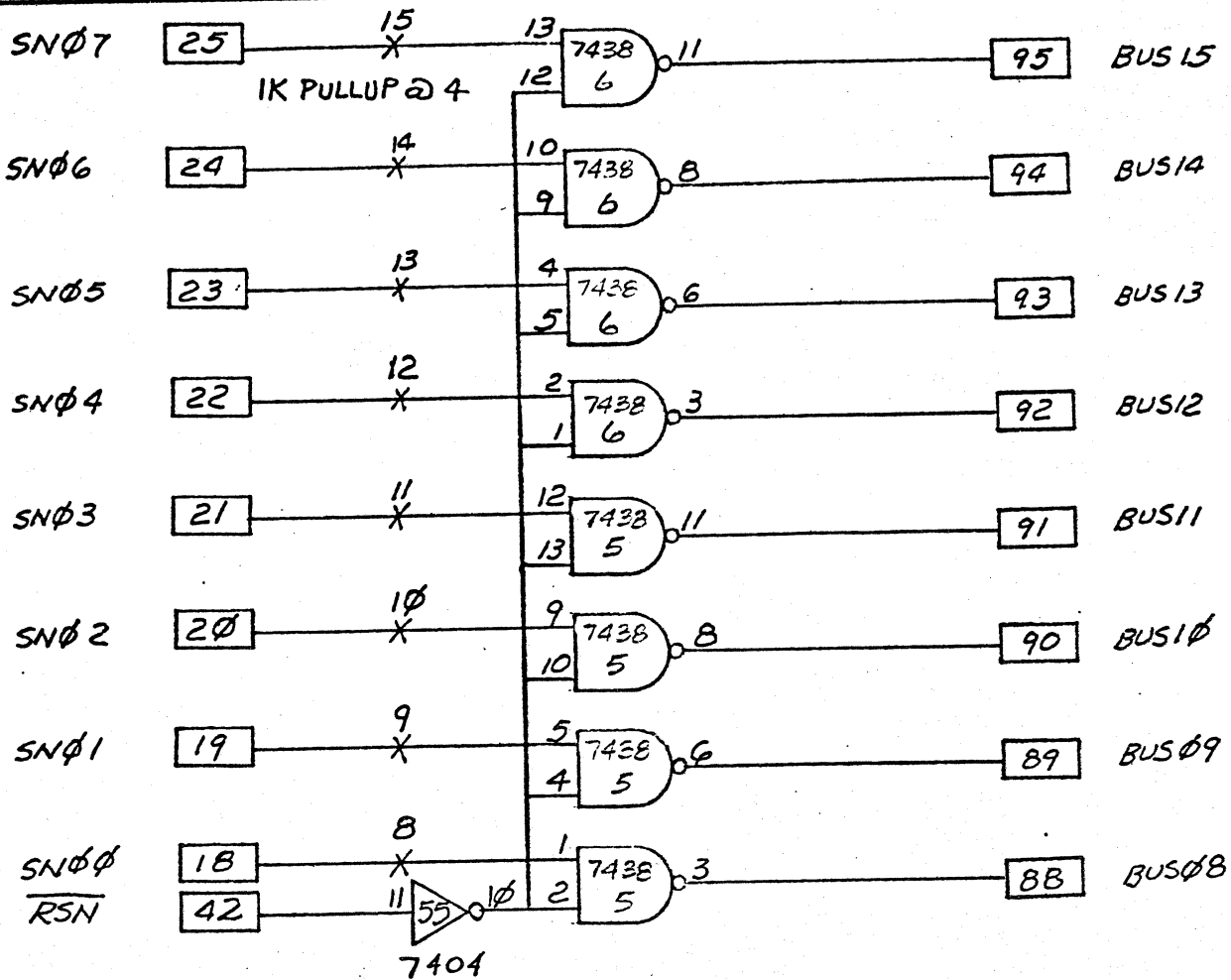
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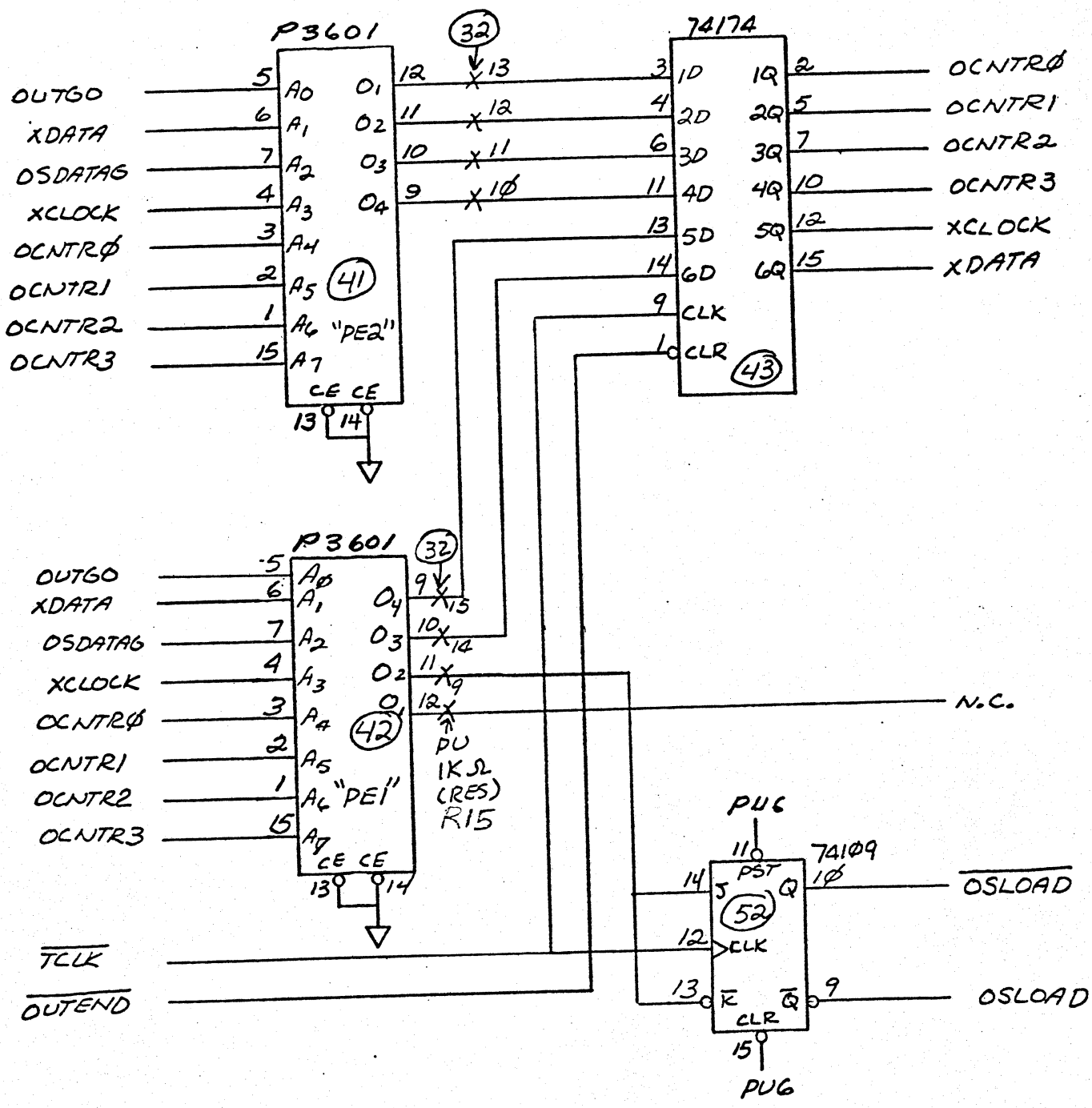


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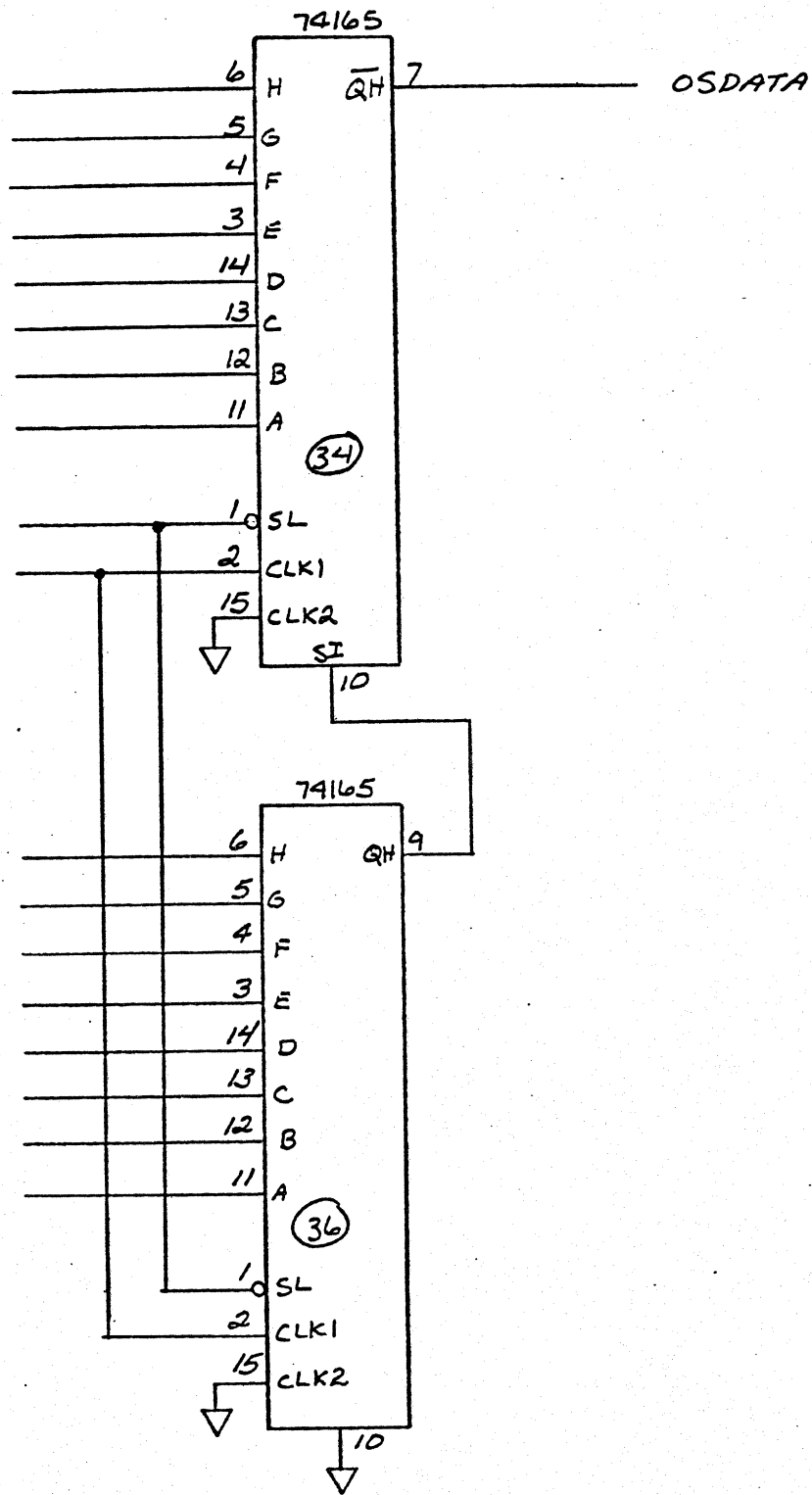
Title  
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IM00  
IM01  
IM02  
IM03  
IM04  
IM05  
IM06  
IM07

OSLOAD  
XCLOCK

IM08  
IM09  
IM10  
IM11  
IM12  
IM13  
IM14  
IM15



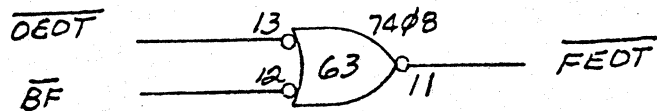
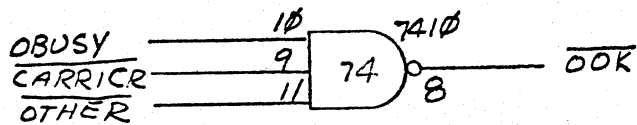
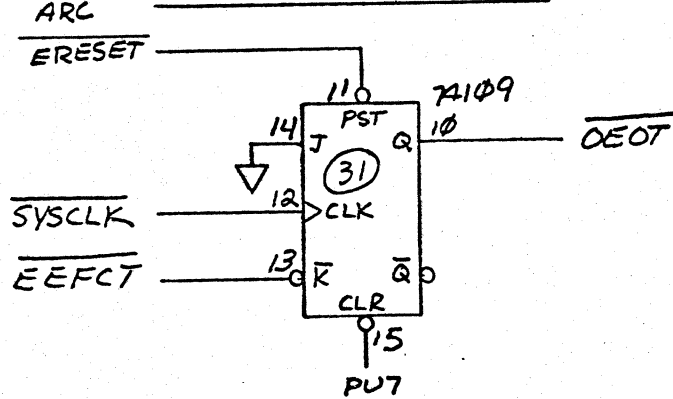
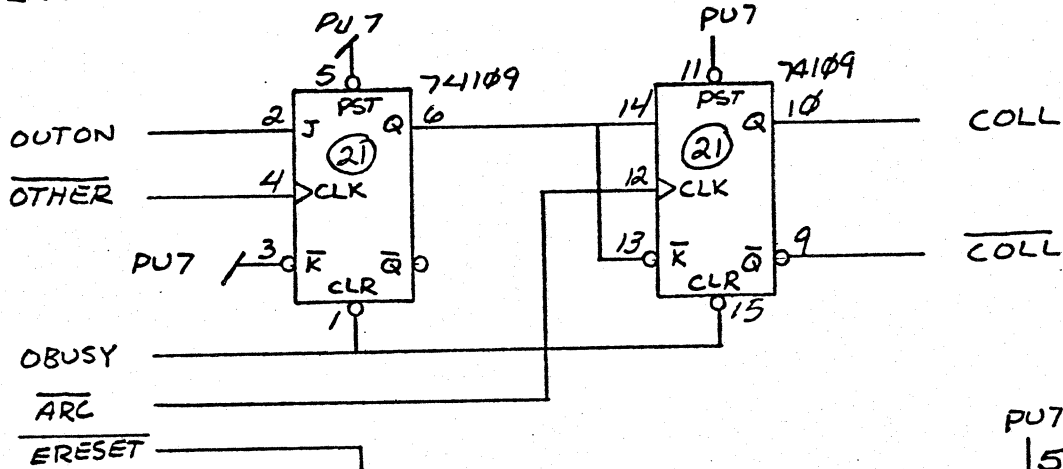
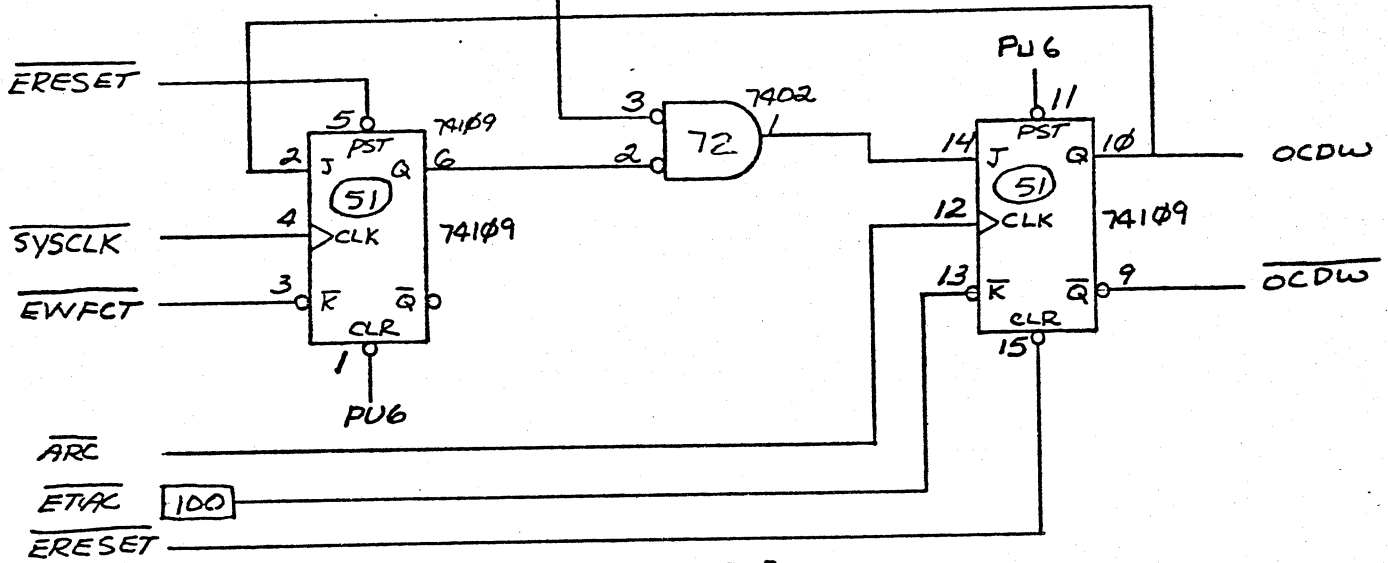
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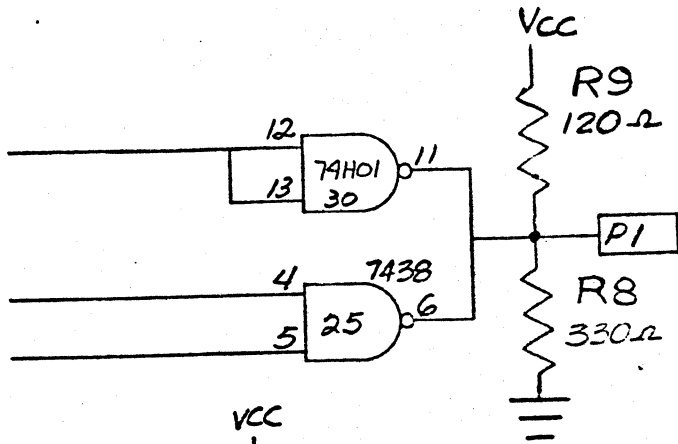
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COLL

XDATA

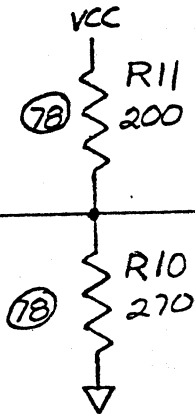
COLL



XDATA

TROTHER

P11



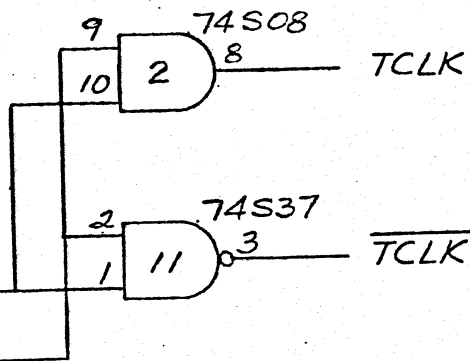
OTHER

DBARC

63

OKTORUN

11

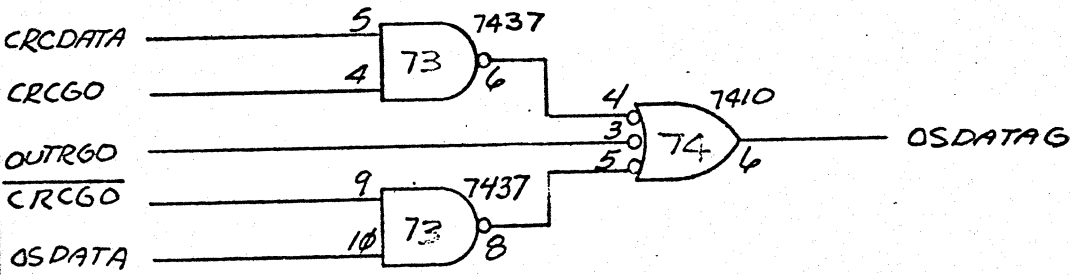
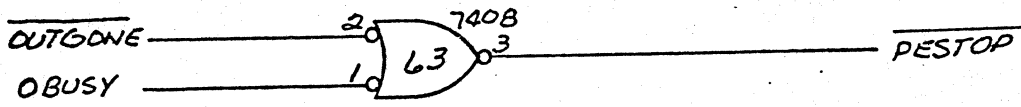
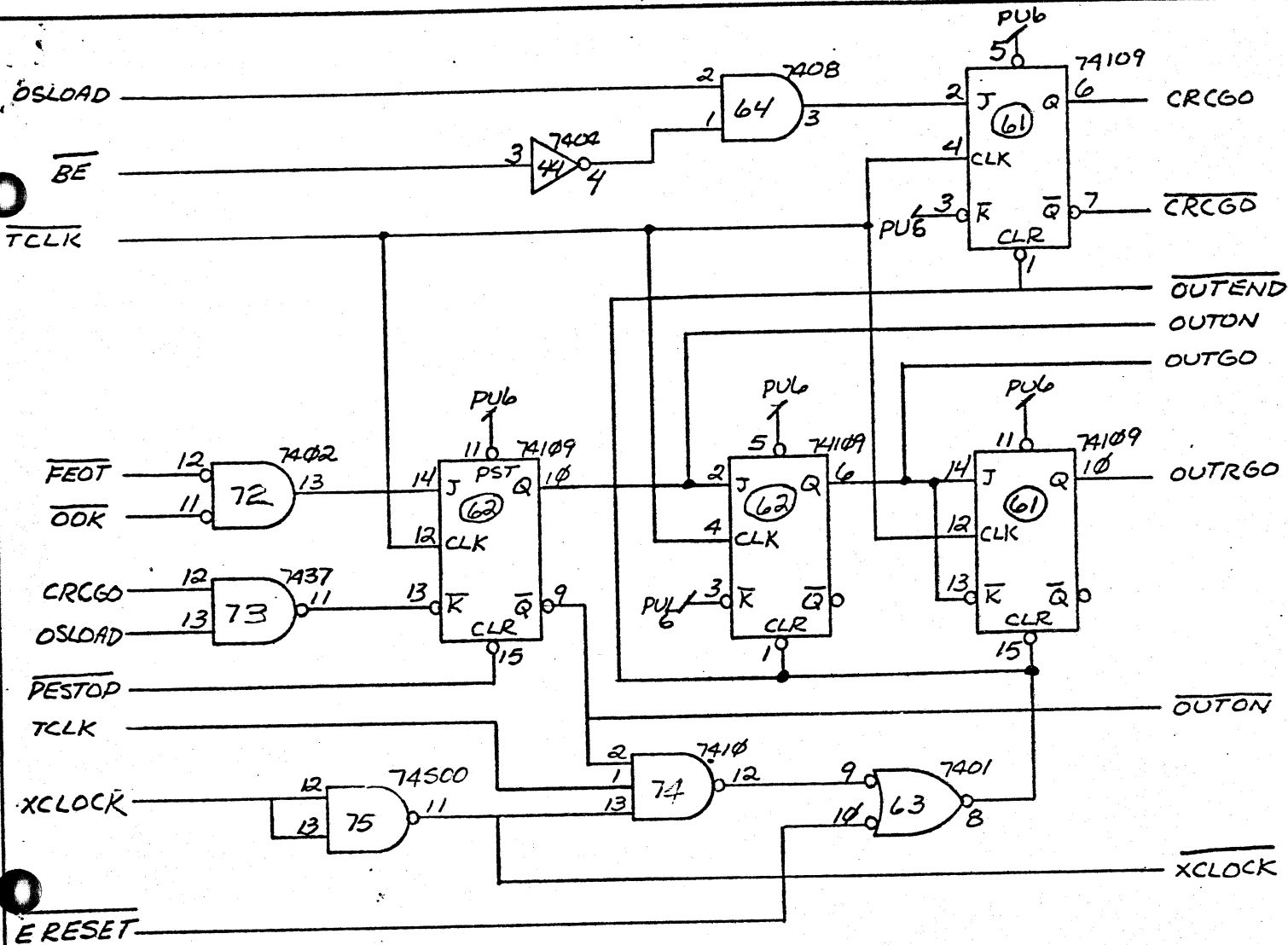


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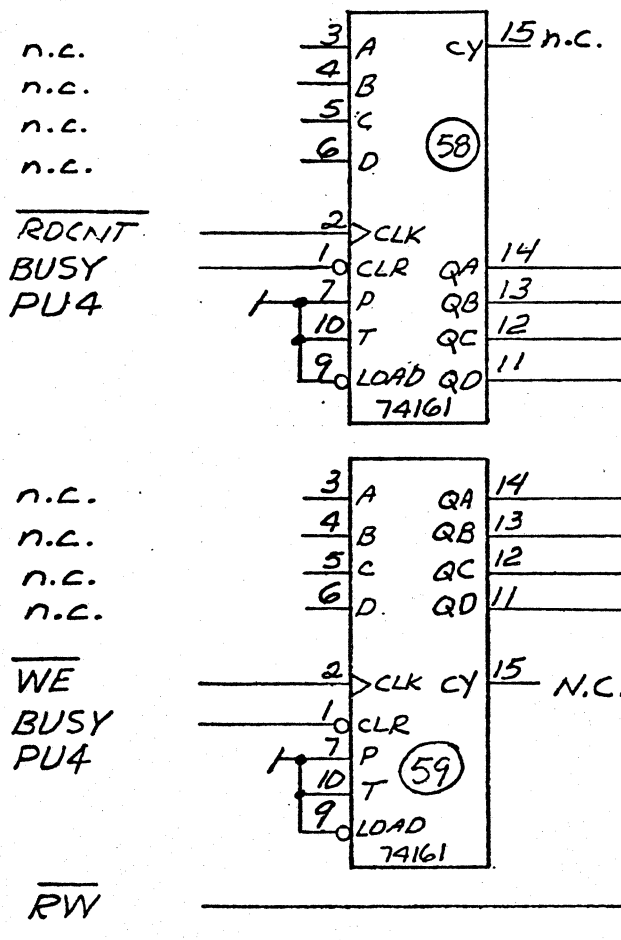


PHASE ENCODER CONTROL

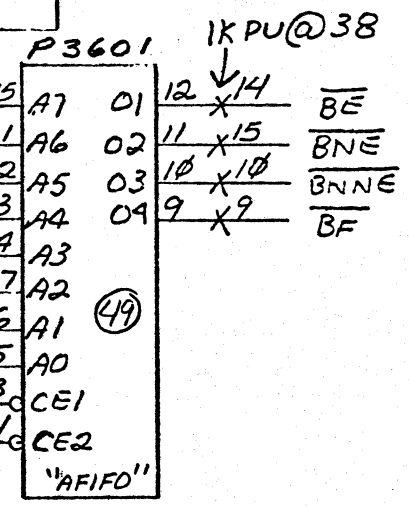
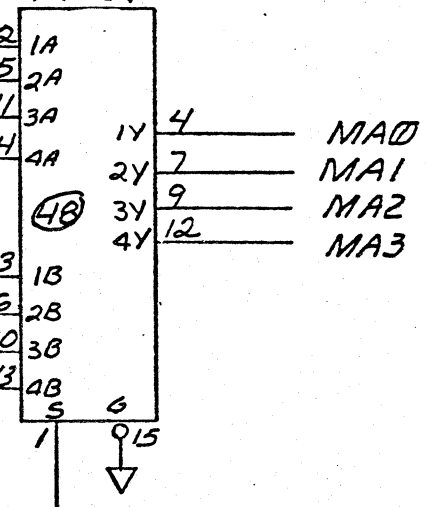
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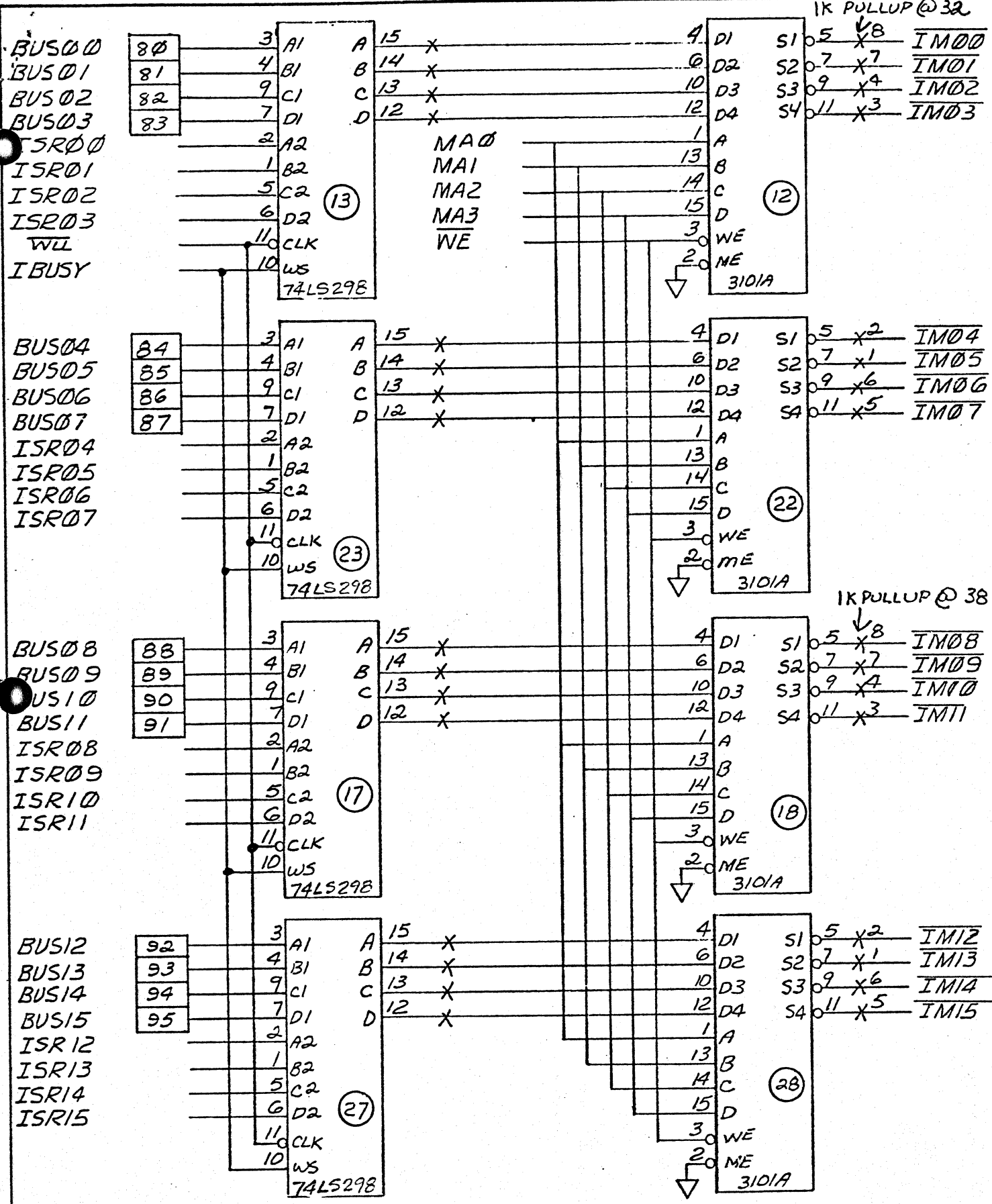
HALF DUPLEX BUFFER

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HALF DUPLEX BUFFER

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