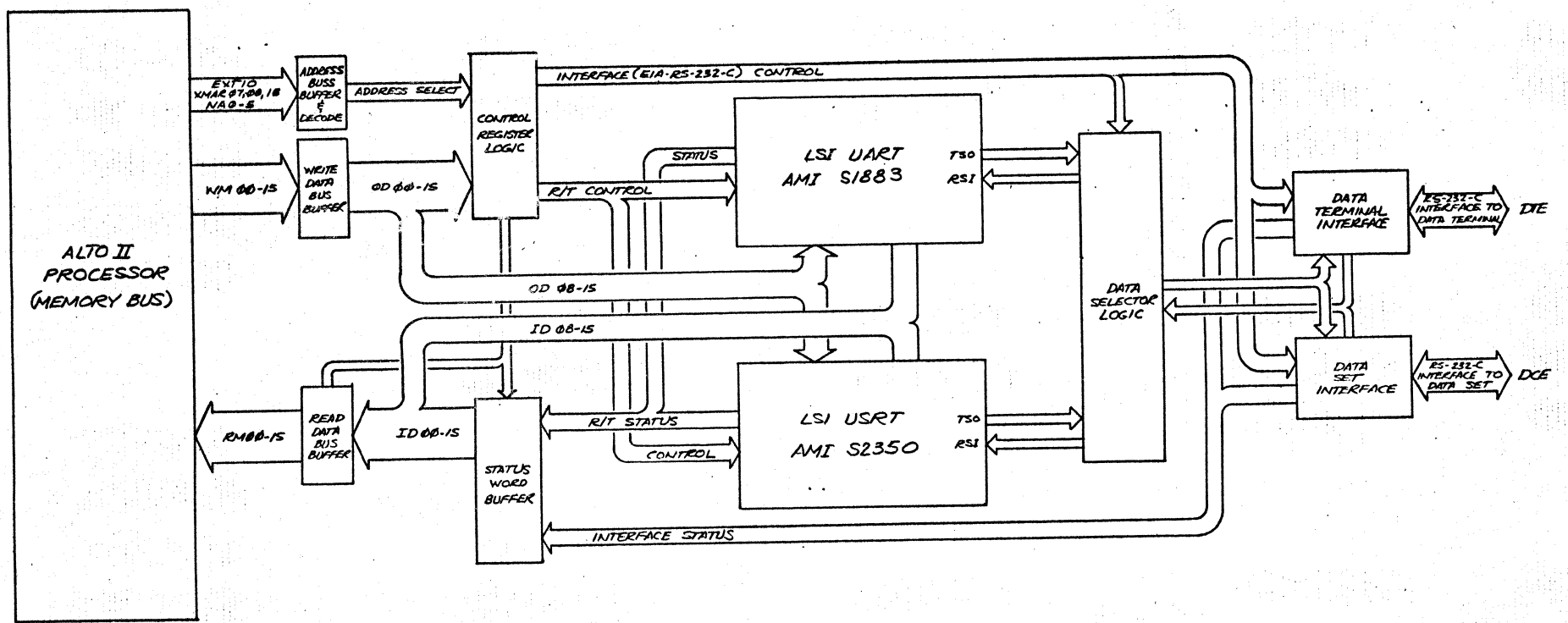


ML Drawing No. 596P61520 Rev. B

Material List

Rev.	Drawing Title	Model No.	Date	Sheet	
	ALTO II SERIAL COMMUNICATION CONTROL		2/9/78	3 of 14	
Drawing No.	Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
ML	1	BOARD, GENERAL PURPOSE, WIRE-WRAP	596P61506A	1	
	2	MICROCIRCUIT 8T98N		15	A1, A9, A12, B1, C1, C2, C4, C9, C12, E1, E12, F1, F9, G1, G12
	3	74LS75N		2	A5, B5
	4	7485N		1	A6
	5	74LS02N		3	A8, B9, C6
	6	74LS174N		1	A10
	7	7438N		1	A11
	8	1489PC		3	A13, B13, G13
	9	74LS138N		2	B6, F10
	10	S2350P		1	B7
	11	74LS00N		5	B8, B11, F8, G9, G11
	12	7493AN		1	B10
	13	8T97N		10	B12, C3, C5, C8, E2, E3, E5, F5, F12, G5
	14	74LS30N		1	C6
	15	F4702PC		1	C10
	16	74221N		2	C11, A8
	17	1488PC		3	C13, E13, F13
	18	74LS175N		4	D2, D4, E10, G10
	19	7404N		1	D5
	20	74LS10N		2	E4, F11
	21	7425N		1	E9
	22	CD4011BE		1	E11
	23	7474N		3	F6, G6, G8
	24	MICROCIRCUIT S1883P		1	F7
	25	RESISTOR PAK, MONOLITHIC 316B272		6	A2, A4, B4, F4, G2, G4
	26	RESISTOR PAK, MONOLITHIC 316B242		6	A3, B2, B3, F2, F3, G3

Revisions					
LAL	Rev.	Description	Chk	Date	Approved



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	1. Tolerances XX 2.03 Dimensioned & XXX 2.010 ± 1/2°	Check: <i>B. J. J.</i> 8/31/77	300 NORTH HALSTEAD ST., WEST PARADISE, CALIFORNIA 94597	
	2. Break All Sharp Ed. .010 Approx.	Appr: <i>Stall</i> 8-1-77	Title: ALTO II SERIAL COMMUNICATION CONTROL BLOCK DIAGRAM	
	3. Mach. Surfaces ✓	Material:	Code Ident. 12705 Size Dwg. No. 596P61520 Change Letter N/C	
	4. All Dim. in Inches 5. All True Position Tolerances Apply at MMC	Model No. First Use	Finish:	Scale Do Not Scale Drawing Sheet 5 of 14

CONTROL WORD FORMATS

STATUS WORD FORMAT

• MNEMONIC **INITIF** - INITIALIZE INTERFACE CIRCUITS

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
1	0	0	0	LINE	DS	HD	S	STD	X	BAUD RATE					

LINE - ADDRESSES CONTROL WORD TO SELECTED LINE CONTROL; UP TO 8 FULLY PROGRAMMABLE, FULL DUPLEX LINE CONTROLS MAY BE ACCOMMODATED IN ONE ALTO II PROCESSOR.
 DS - WHEN SET, SELECTED CONTROL WILL COMMUNICATE WITH A DATA SET; DEFAULT TO DATA TERMINAL.
 HD - WHEN SET, SELECTED CONTROL WILL OPERATE HALF-DUPLEX; DEFAULT TO FULL-DUPLEX.
 S - INDICATES ALTO SENDING WHEN SET (1) IN HALF-DUPLEX.
 STD - SETS SECONDARY REQ. TO SEND (ZSCA) TO ON WHEN SET AND INTERFACE IS TO DATA SET, SETS SECONDARY CARR. DET. TO ON WHEN SET AND INTERFACE IS TO DATA TERM.
 BAUD RATE - SELECTS BAUD RATE AT WHICH LINE WILL OPERATE.

B12	B13	B14	B15	B2	B3	B4	B15	B12	B13	B14	B15
0	0	1	0	0	1	1	1	1	1	0	0
0	0	1	1	1	0	0	0	1	1	0	1
0	1	0	1	1	0	0	1	1	1	0	1
0	1	0	1	1	0	1	1	1	1	0	1
0	1	1	0	1	1	0	0	1	1	1	0

• MNEMONIC **INITRT** - INITIALIZE RECEIVER/TRANSMITTER

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
1	0	0	1	LINE	NDB	NPB	A/S	POE	NSB	X	X	X	X	X	X

NDB - SELECTS NO. OF DATA BITS PER CHARACTER
 NPB - NO PARITY BIT WHEN SET
 A/S - SELECTS ASYNCHRONOUS (UART) OPERATION WHEN SET OR SYNCHRONOUS (USRT) WHEN NOT SET.
 POE - SELECTS EVEN PARITY WHEN SET, ODD PARITY WHEN NOT SET.
 NSB - SELECTS NO. OF STOP BITS PER CHARACTER WHEN ASYNC OPERATION IS SELECTED; SELECTS 1 STOP BIT WHEN SET; 2 STOP BITS WHEN NOT SET (EXCEPTION: SELECTS 1.5 STOP BITS WHEN NOT SET AND 5 DATA BITS ARE SELECTED).

• MNEMONIC **INITRG** - INITIALIZE REGISTERS

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
1	0	1	0	LINE	F/S	DATA FIELD									

F/S - WHEN SET CAUSES DATA FIELD TO BE LOADED INTO USRT TRANSMITTER FILL CHARACTER REGISTER; WHEN NOT SET DATA FIELD WILL BE LOADED INTO USRT RECEIVER SYNC CHARACTER REGISTER.

• MNEMONIC **RESET** - GENERATE CONTROLLER RESETS

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
1	0	1	1	LINE	D	RRT	RR	X	X	X	X	X	X	X	X

D - GENERATES A LINE DISCONNECT/MASTER CLEAR OF THE SELECTED LINE WHEN SET.
 RRT - CLEARS THE RECEIVER/TRANSMITTER (UART/USRT) WHEN SET.
 RR - RESETS SYNCHRONOUS RECEIVER, CLEARS STATUS REGISTER, RESTARTS SYNCHRONOUS RECEIVER IN THE BIT TRANSPARENT MODE FOR SYNC SEARCH.

• MNEMONIC **SWI** - FORCE THE SELECTED CONTROL TO REQUEST AN INTERRUPT

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
1	1	0	0	LINE	X	X	X	X	X	X	X	X	X	X	X

• MNEMONIC **INTA** INTERRUPT ACKNOWLEDGE TO THE SELECTED LINE.

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
1	1	0	1	LINE	X	X	X	X	X	X	X	X	X	X	X

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
D	CD	RI	SI	LINE	SRD	RDA	BMT	SCR	FCR	RPE	ROR	RFE	INTP		

• INTERFACE STATUS (HIGH ORDER BYTE)
 D - DISCONNECT FLAG: WHEN SET THIS BIT INDICATES LOSS OF RS-232 LINE; DATA SET RDY IF DATA SET INTERFACE IS SELECTED, DATA TERM. RDY IF DATA TERM INTERFACE IS SELECTED.
 CD - CARRIER DETECT FLAG.
 RI - RING INDICATOR FLAG.
 SI - SEND INDICATOR FLAG: WHEN BIT IS SET, INDICATES PRESENCE OF CLEAR TO SEND IF DATA SET INTERFACE IS SELECTED; REQUEST TO SEND IF DATA TERMINAL INTERFACE IS SELECTED.
 SRD - REMOTE HALF-DUPLEX BREAK: IN HALF DUPLEX THIS BIT GOING TO A ZERO SIGNALS A BREAK BY THE REMOTE RECEIVING STATION.
 • RECEIVER/TRANSMITTER STATUS (LOW ORDER BYTE)
 RDA - RECEIVE DATA AVAILABLE.
 TBMT - TRANSMIT BUFFER EMPTY.
 SCR - SYNC CHARACTER RECEIVED (USRT).
 FCT - FILL CHARACTER TRANSMITTED (USRT).
 RPE - RECEIVE PARITY ERROR
 ROR - RECEIVE OVERFLOW ERROR
 RFE - RECEIVE FRAMING ERROR (UART)
 • INTERRUPT FLAG (B15)
 INTP - INTP = D + CD + RI + SI + RDA + TBMT + SCR + (SRD * SEND * HDUP)

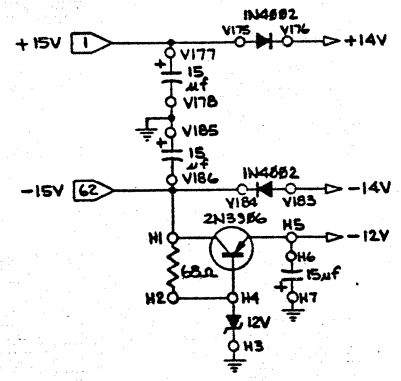
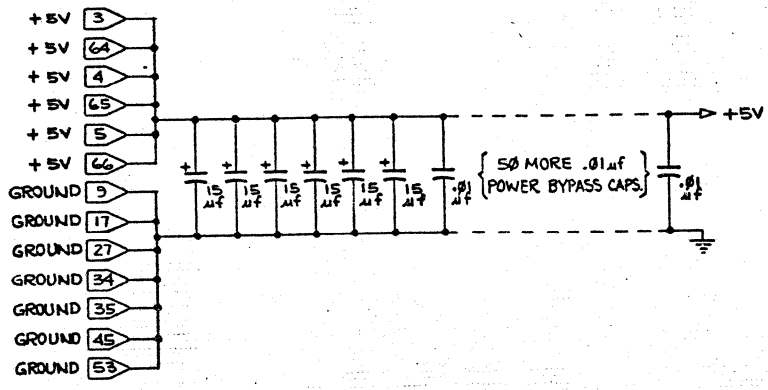
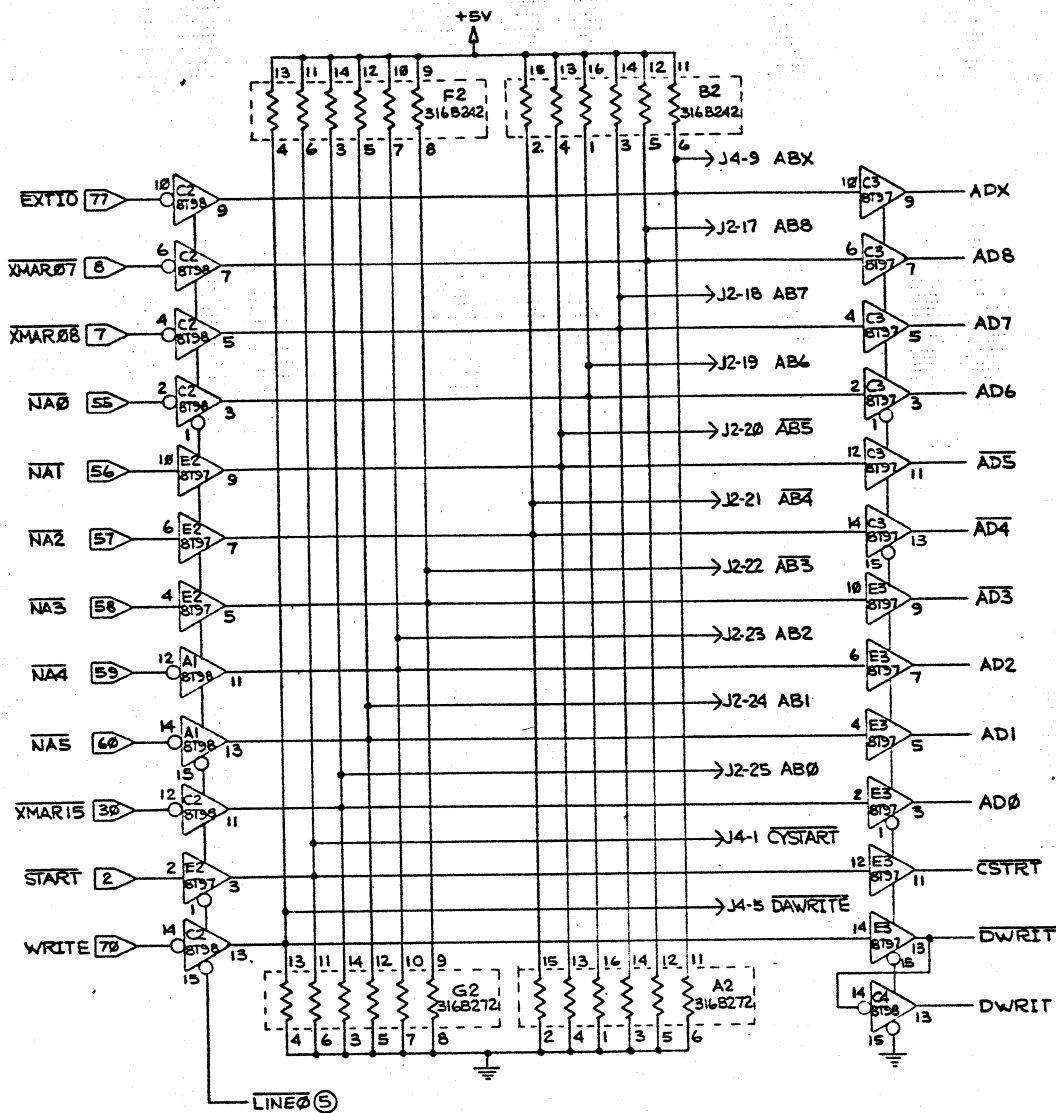
DATA WORD FORMAT (RECEIVE OR TRANSMIT)

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
0	X	X	X	LINE	X	DATA FIELD									

backwards (see BOP stream package)
 To set fill and sync char registers

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		FINISH-XEROX SPEC NO.	ANGLES	CHK. 1/1	
		DO NOT SCALE DRAWING	DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS, ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	M.E. APPD. 1/1	NAME ALTO II SERIAL COMM. CONTROL - SCHEMATIC DIAGRAM
				E.E. APPD. <i>26</i> 2/16/78	DWG A 596P61520 REV. B
				APPD. 1/1	SIZE SH 6 OF 14
				SURFACE QUALITY ON MACHINED SURFACES UNLESS OTHERWISE SPECIFIED	

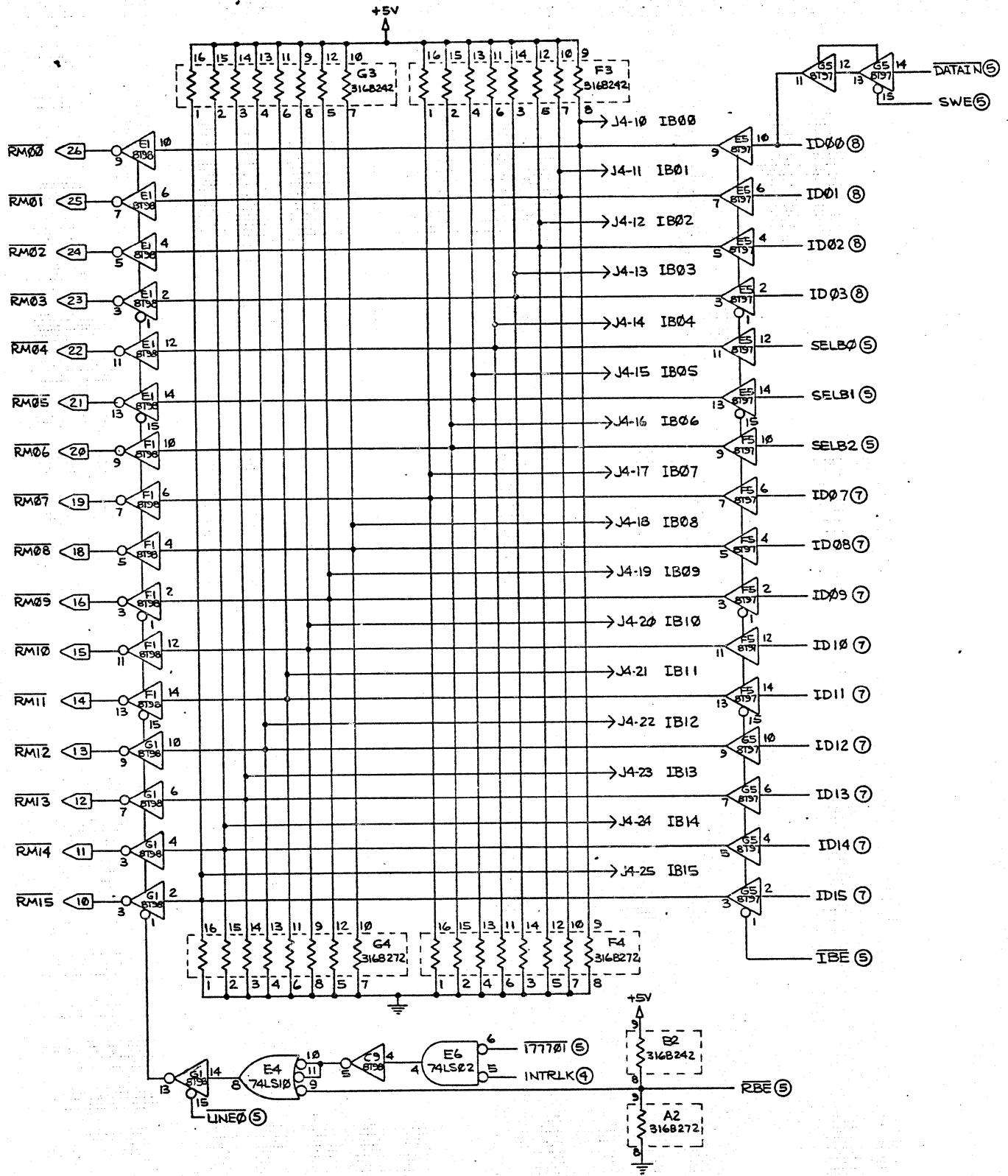
E D C B A



- NOTES: 1. CIRCLED N^o (Ⓢ) APPENDED TO SIGNAL NAMES INDICATE SHEET N^o WHEREON SIGNAL ORIGINATES.
2. SYMBOL \square INDICATES J1 CARDEDGE CONNECTOR PIN CONNECTION TO MOTHERBOARD BACKPLANE.
3. UNLESS OTHERWISE INDICATED, +5V TO PIN 14 FOR 14-PIN DIP AND PIN 16 FOR 16-PIN DIP, AND GROUND TO PIN 7 FOR 14-PIN DIP AND PIN 8 FOR 16-PIN DIP I.C.s.

MEMORY ADDRESS & CONTROL BUS BUFFER LOGIC

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		FINISH-XEROX SPEC NO.	ANGLES	CHK. <i>1/1</i>	
		DO NOT SCALE DRAWING	DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS, ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	APPD. <i>2/6/78</i>	NAME ALTO II SERIAL COMM. CONTROL-SCHEMATIC DIAGRAM
				SURFACE QUALITY ON MACHINED SURFACES UNLESS OTHERWISE SPECIFIED	DWG A 596P61520
					REV. B
					SIZE SH 7 OF 14



MEMORY READ BUS BUFFER LOGIC

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		FINISH-XEROX SPEC NO.	ANGLES	M.E. APPD. //							
		DO NOT SCALE DRAWING	DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS, ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	E.E. APPD. <i>[Signature]</i>		APPD. //					
			SURFACE QUALITY ON MACHINED SURFACES UNLESS OTHERWISE SPECIFIED	APPD. //		NAME ALTO II SERIAL COMM. CONTROL-SCHEMATIC DIAGRAM					
					<table border="1"> <tr> <td>DWG A</td> <td>596P61520</td> <td>REV. B</td> </tr> <tr> <td>SIZE</td> <td>SH 9 of 14</td> <td></td> </tr> </table>	DWG A	596P61520	REV. B	SIZE	SH 9 of 14	
DWG A	596P61520	REV. B									
SIZE	SH 9 of 14										

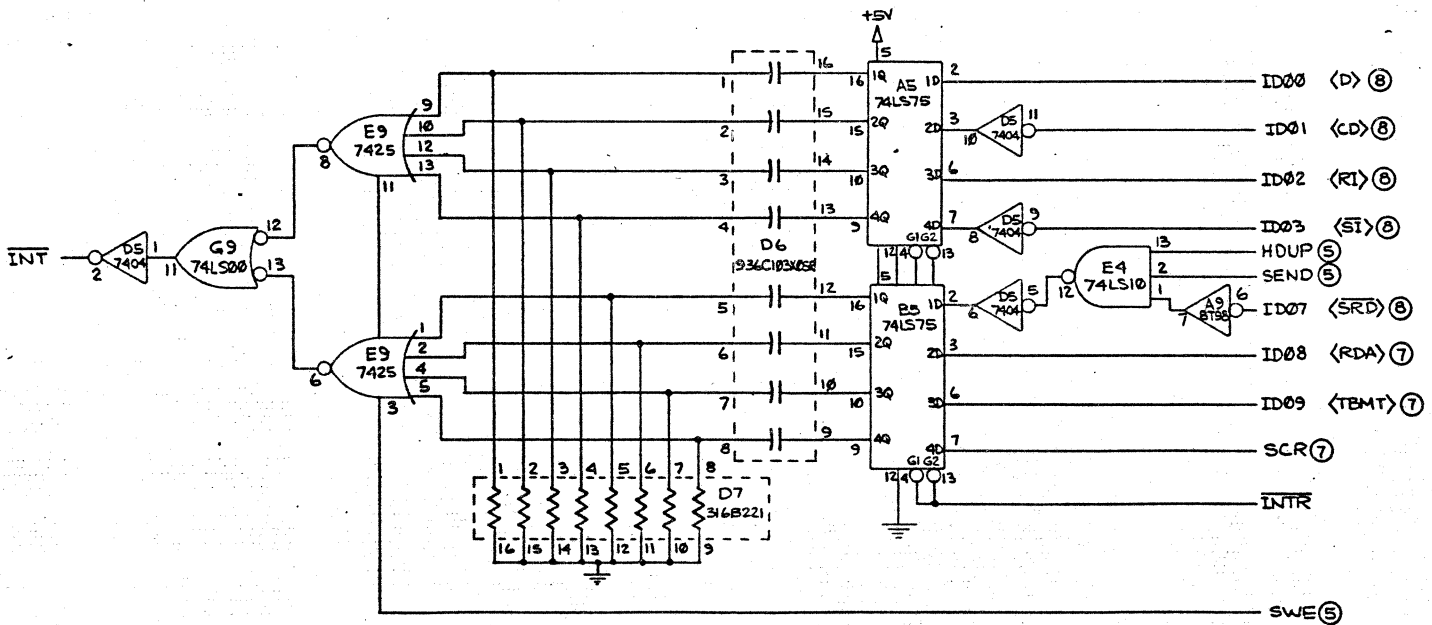
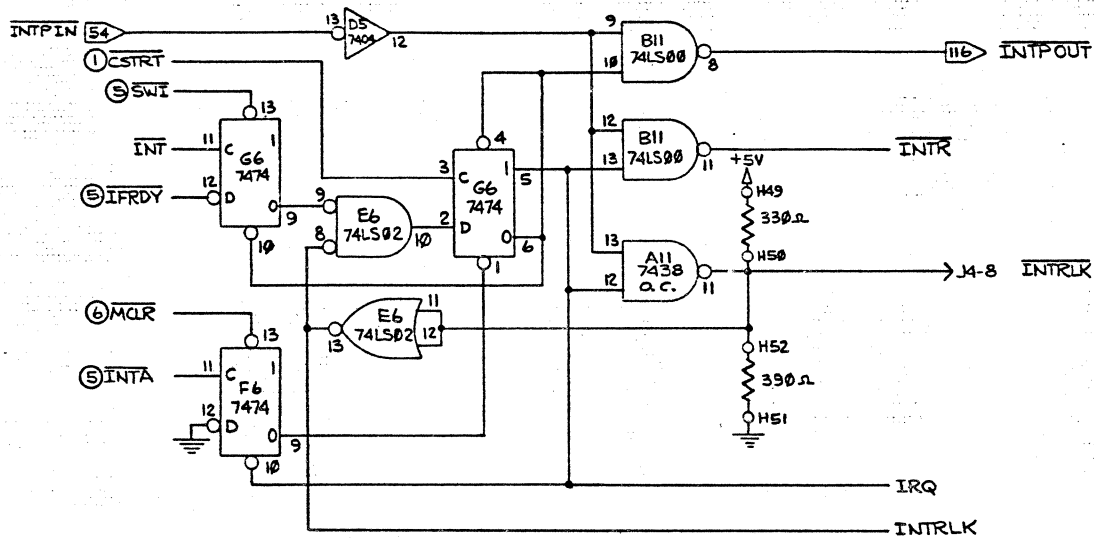
E

D

C

B

A



INTERRUPT LOGIC

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				CHK. <i>1/1</i>	
	FINISH-XEROX SPEC NO.	DO NOT SCALE DRAWING	ANGLES	M.E. APPD. <i>1/1</i>	NAME ALTO II SERIAL COMM. CONTROL-SCHEMATIC DIAGRAM
			DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS, ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	E.E. APPD. <i>2/1/78</i>	
			SURFACE QUALITY ON MACHINED SURFACES UNLESS OTHERWISE SPECIFIED	APPD. <i>1/1</i>	DWG A
					SIZE SH 10 OF 14
					REV. B

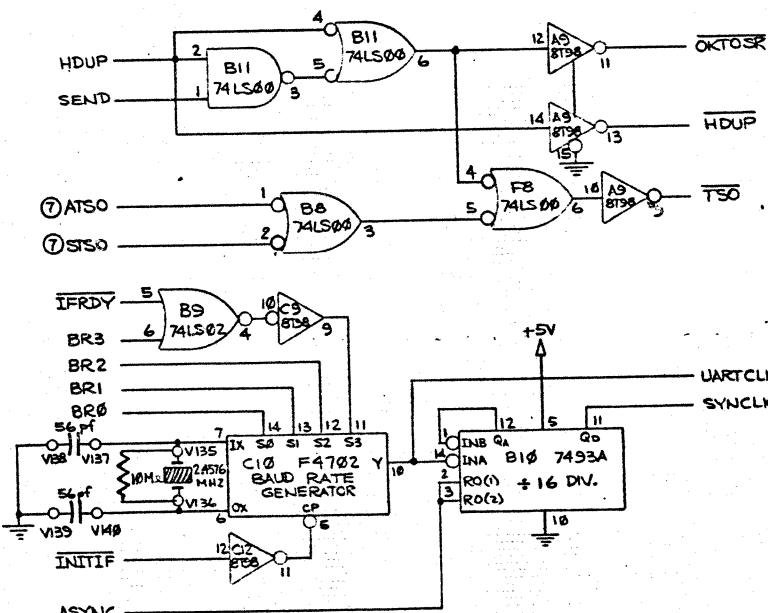
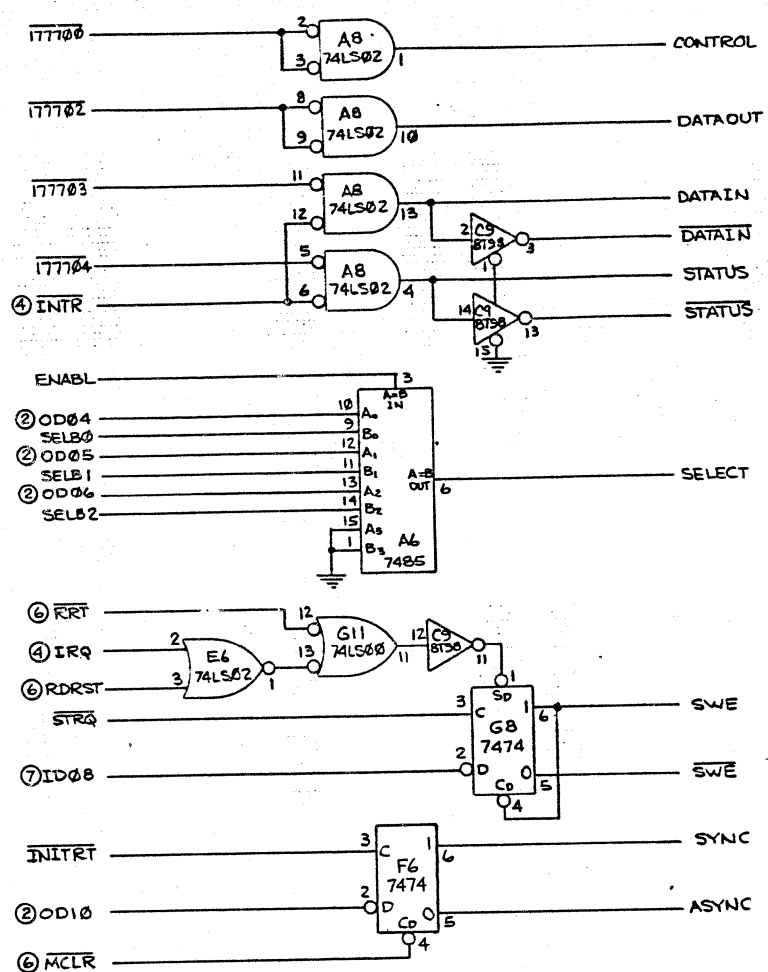
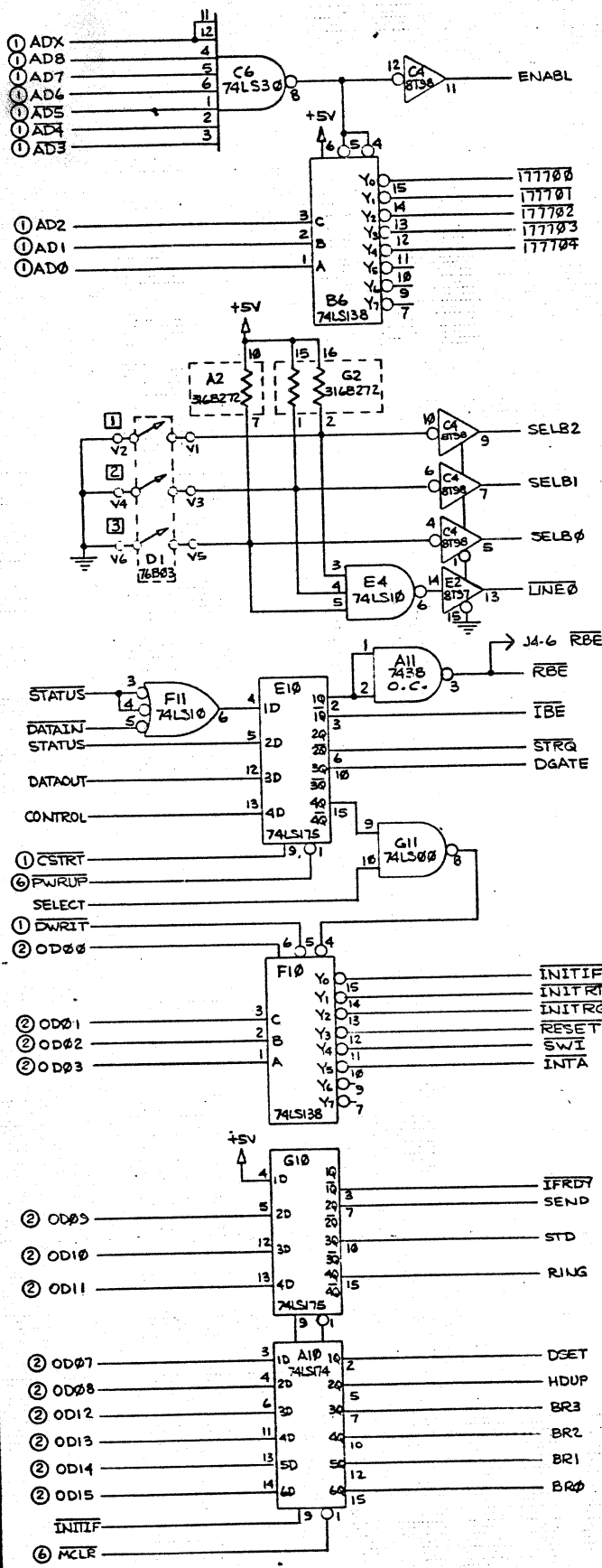
E

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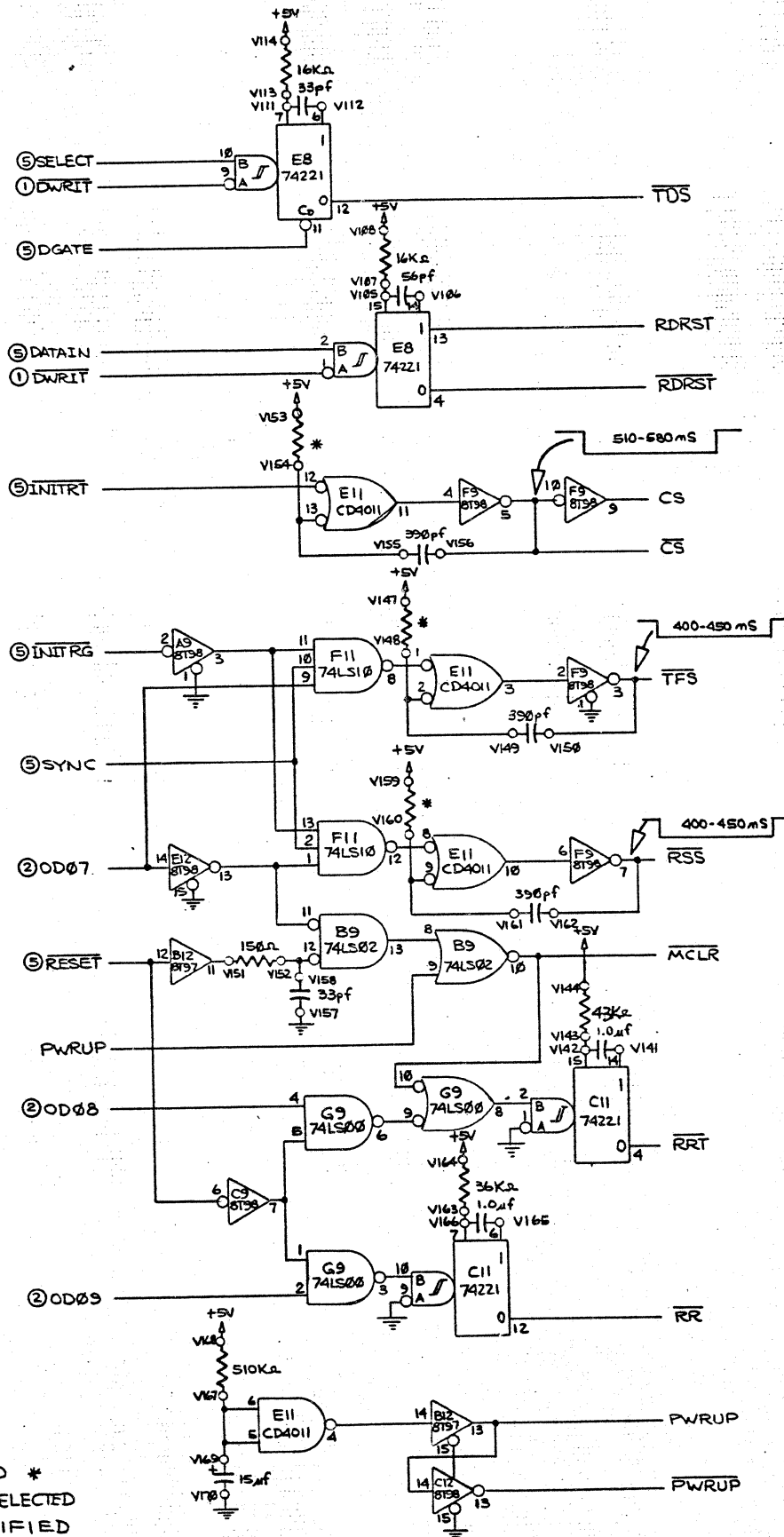
A



ADDRESS DECODING AND CONTROL LOGIC

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		FINISH-XEROX SPEC NO.	ANGLES	CHK. <i>11</i>	
			DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS, ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	M.E. APPD. <i>11</i>	NAME ALTO-II SERIAL COMM. CONTROL SCHEMATIC DIAGRAM
		DO NOT SCALE DRAWING		E.E. APPD. <i>2-16-78</i>	
				APPD. <i>11</i>	DWG 596P61520
				SURFACE QUALITY ON MACHINED SURFACES UNLESS OTHERWISE SPECIFIED <input checked="" type="checkbox"/>	REV. B
					SIZE SH 11 OF 14

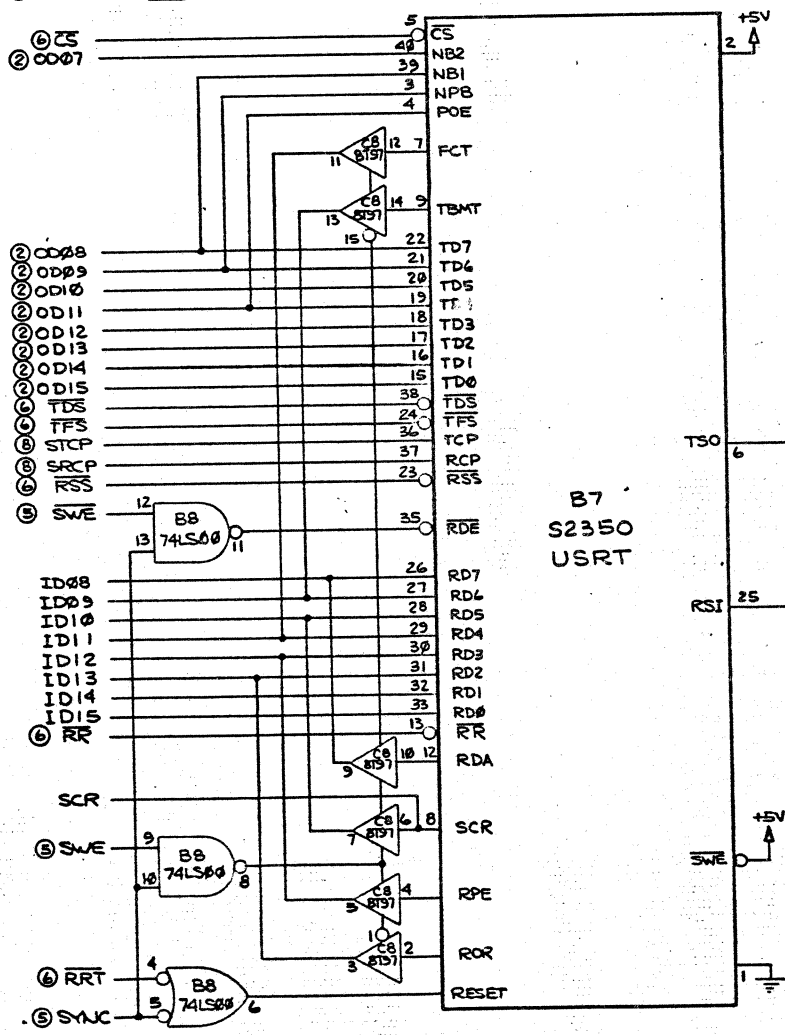
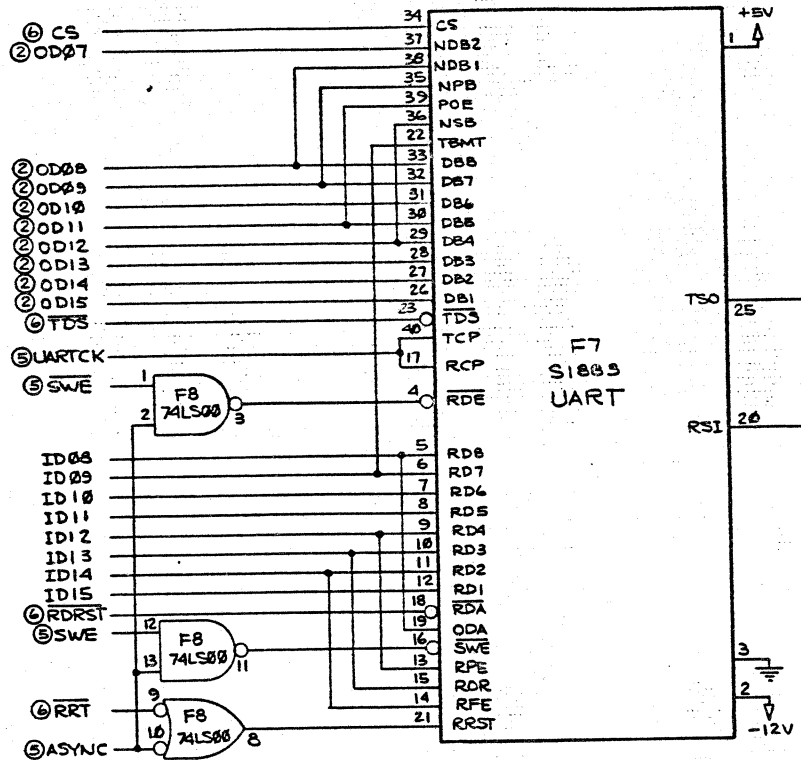
E D C B A



NOTE: COMPONENTS MARKED *
ARE INDIVIDUALLY SELECTED
TO PRODUCE SPECIFIED
PULSE WIDTHS.

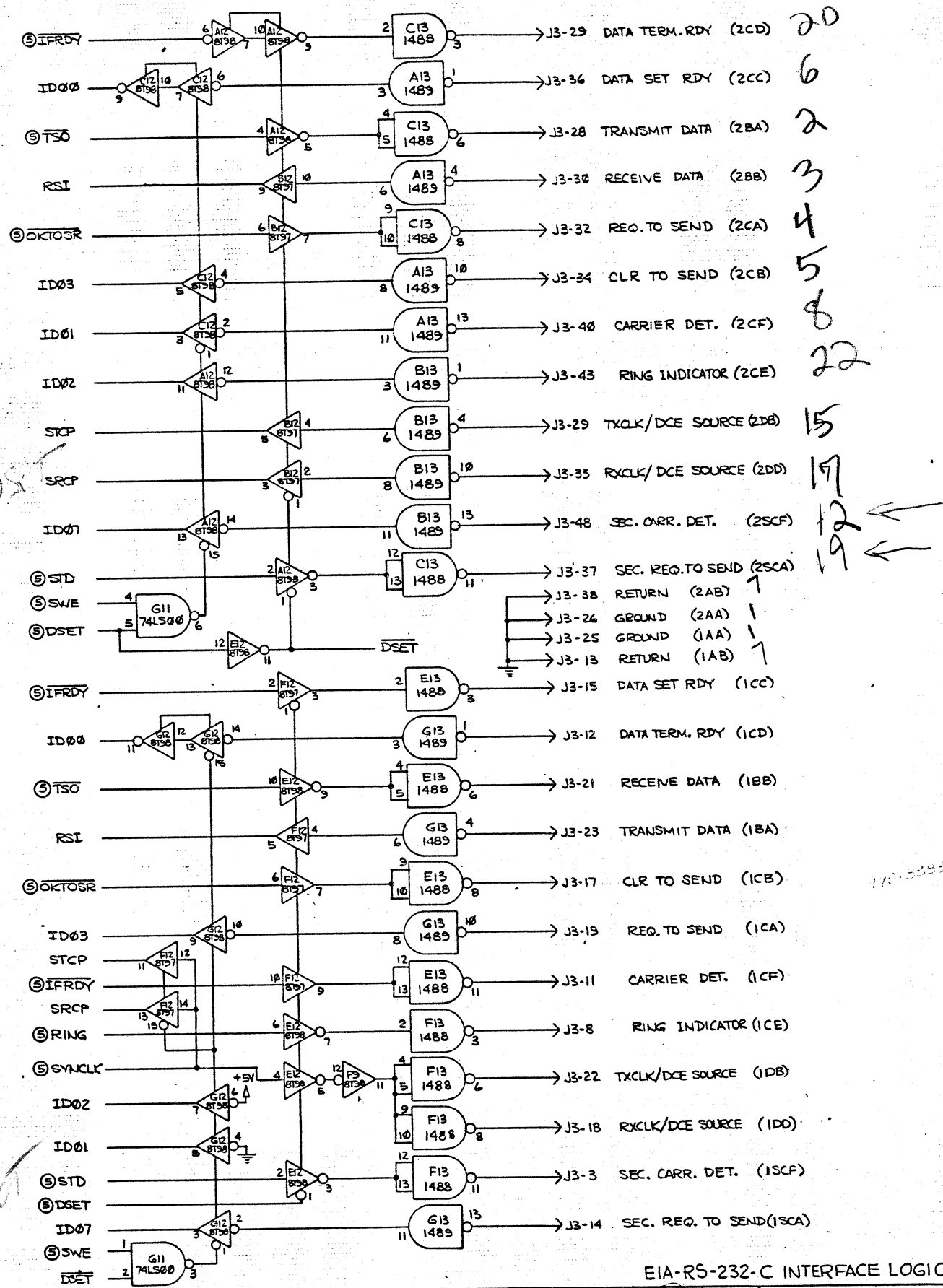
POWER UP, RESET & STROBE GENERATOR LOGIC

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		FINISH-XEROX SPEC NO.	ANGLES	CHK. //	
		DO NOT SCALE DRAWING	DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS, ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	M.E. APPD. // E.E. APPD. 2-16-78 APPD. //	NAME ALTO II SERIAL COMM. CONTROL SCHEMATIC DIAGRAM
				SURFACE QUALITY ON MACHINED SURFACES UNLESS OTHERWISE SPECIFIED ✓	DWG A 596P61520 REV. B SIZE SH 12 of 14



TRANSMIT-RECEIVE LOGIC

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		FINISH-XEROX SPEC NO.	ANGLES	CHK. <i>[Signature]</i> 1/1		
		DO NOT SCALE DRAWING	DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS, ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	M.E. APPD. <i>[Signature]</i> 1/1		NAME ALTO II SERIAL COMM.
				E.E. APPD. <i>[Signature]</i> 2/6/78		CONTROL SCHEMATIC DIAGRAM
				APPD. <i>[Signature]</i> 1/1	DWG A	
				SURFACE QUALITY ON MACHINED SURFACES UNLESS OTHERWISE SPECIFIED	SIZE SH 13 of 14	
					REV. B	



*DSET true
ie. talk
with a DSET*

*DSET false
ie. talk
as a DSET*

20
6
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17
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EIA-RS-232-C INTERFACE LOGIC

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		FINISH-XEROX SPEC NO.	ANGLES	CHK. //	
		DO NOT SCALE DRAWING	DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS, ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	M.E. APPD. //	
				E.E. APPD. 2/6/78	
			APPD. //	APPD. //	