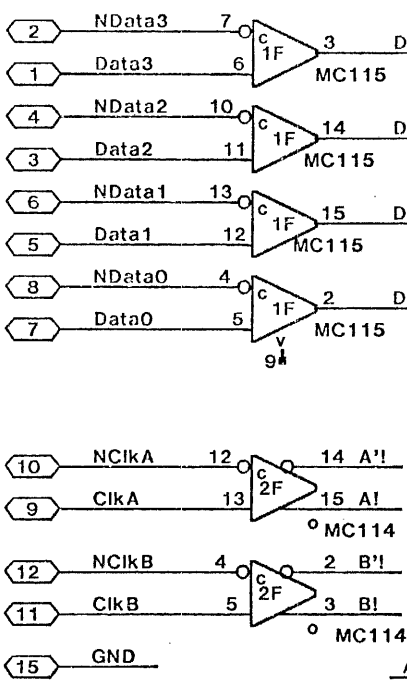


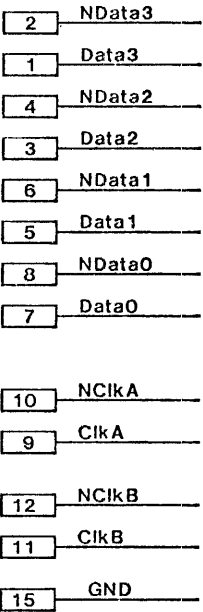
J1

DA15S Connector



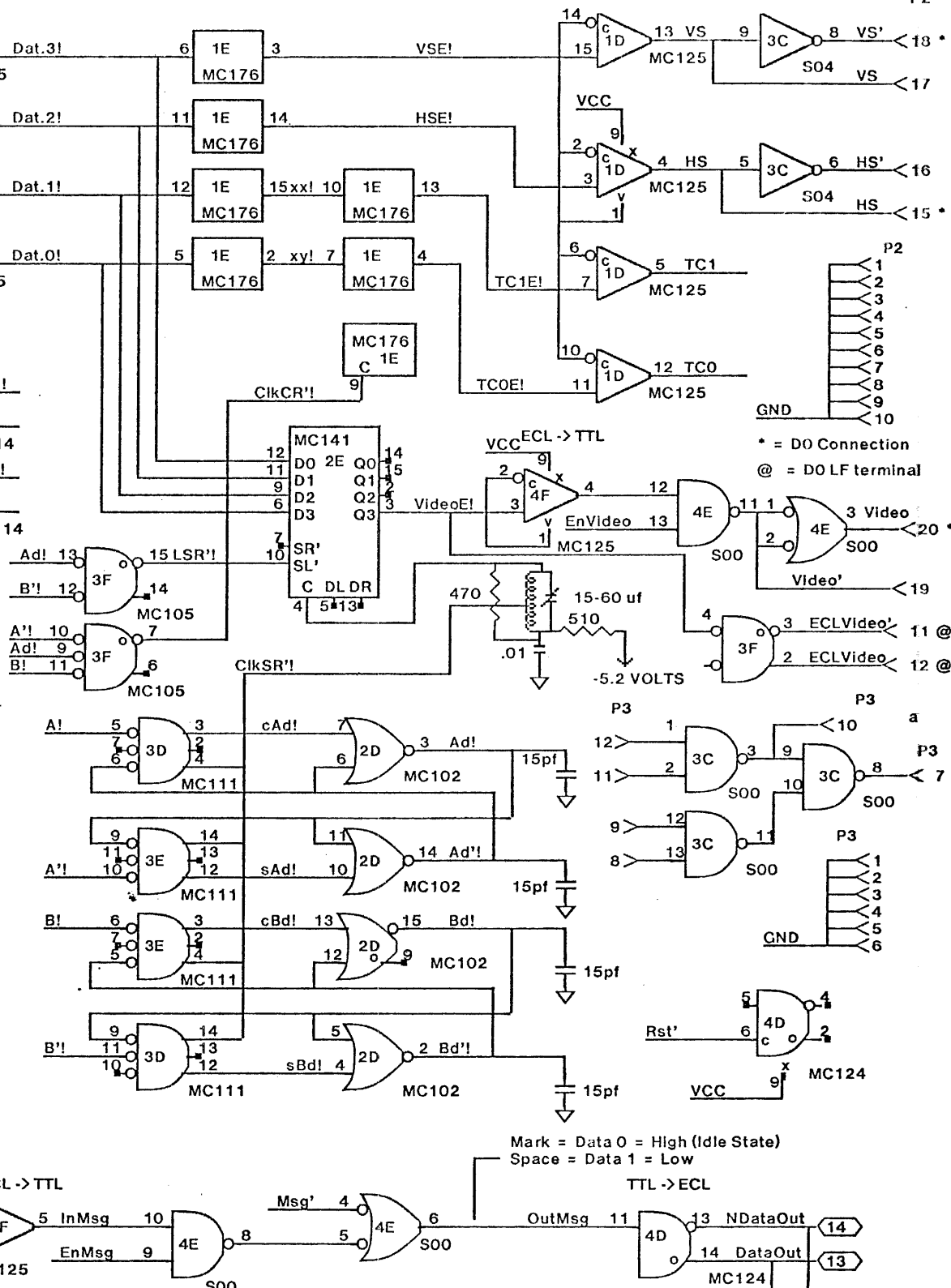
P1

DA15P Connector



ECL -> TTL

P2



\* = D0 Connection  
@ = D0 LF terminal

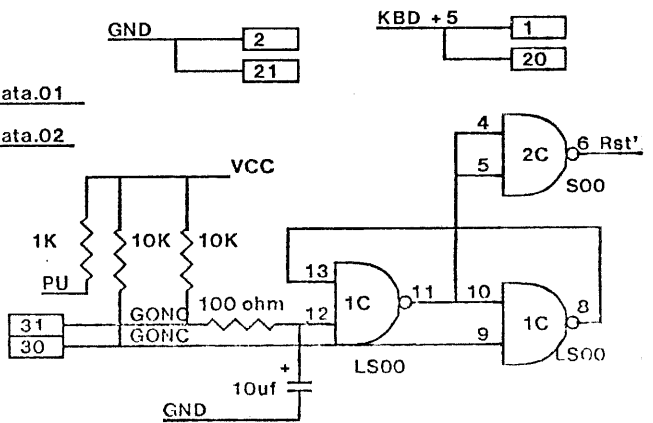
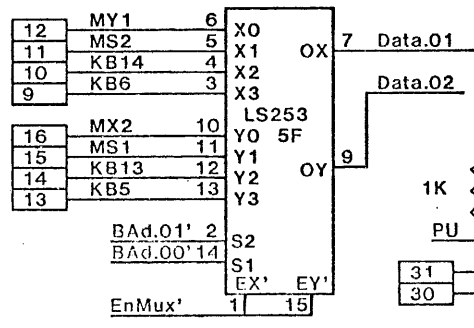
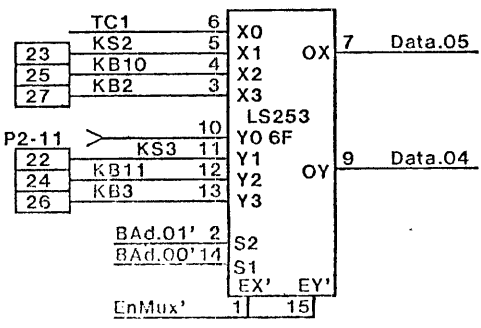
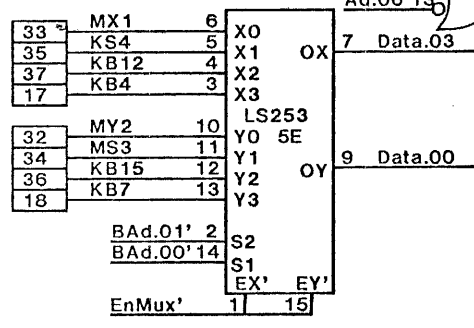
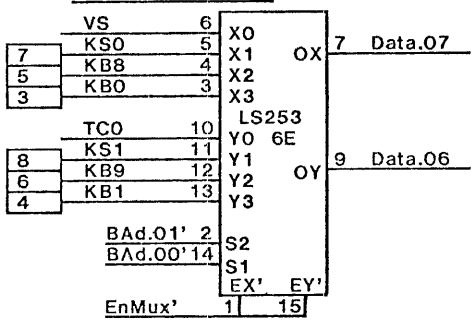
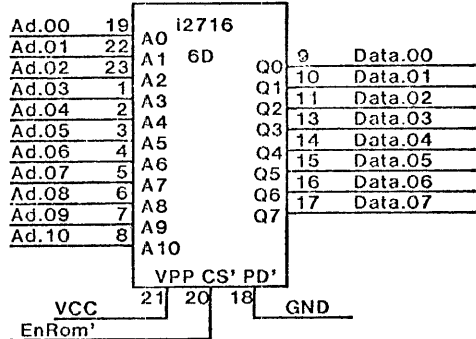
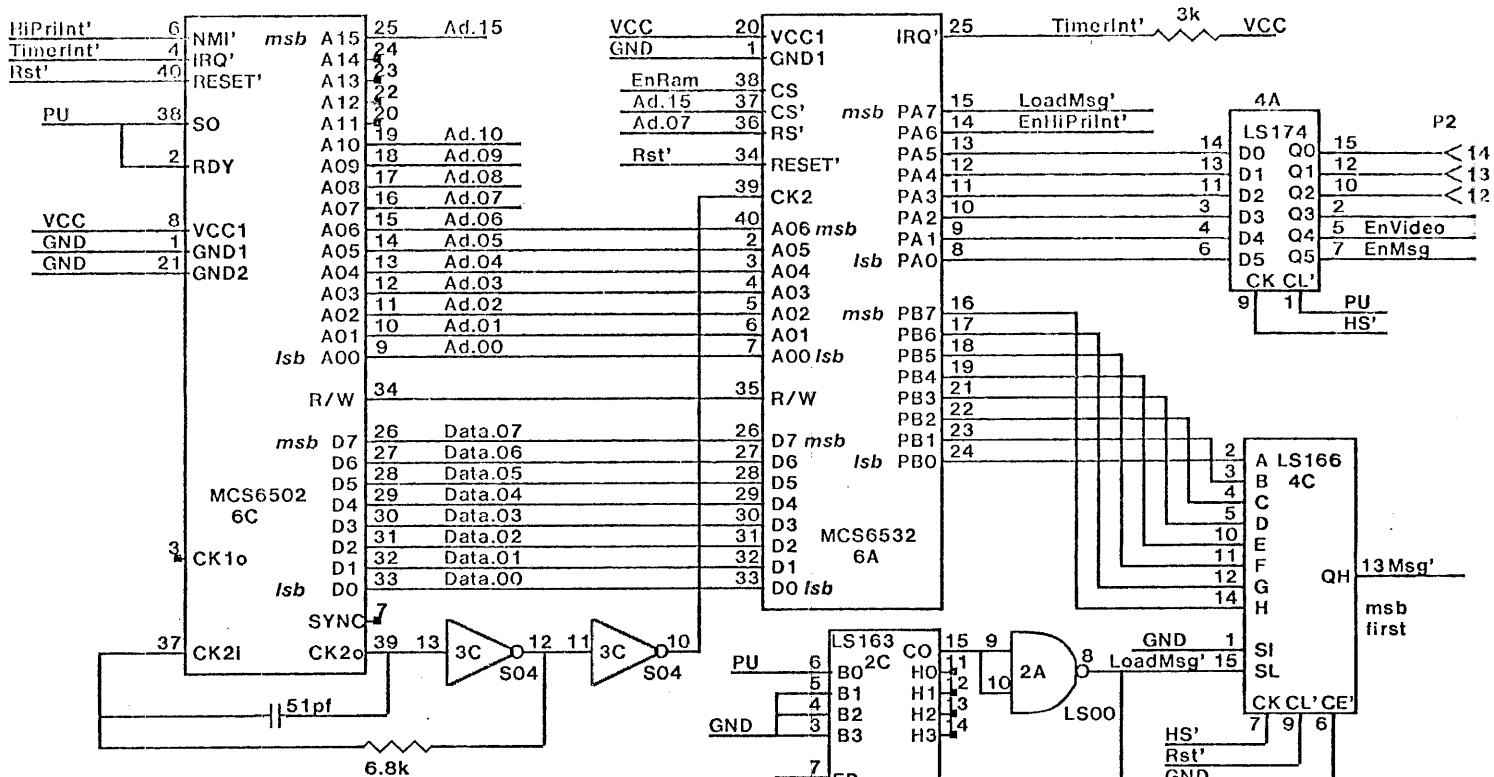
Mark = Data 0 = High (Idle State)  
Space = Data 1 = Low

TTL -> ECL

NOTES:

- 1) All signals with names of the form xxx! have 510ohm pulldown resistors to VEE (-5.2) (26 places)
- 2) P2 consists of wire-wrap posts on .100 centers
- 3) Ground, VCC, and VEE pins for ECL chips are as shown:

	GND	VEE	VCC
MC102, MC105, MC114, MC115	1,16	8	-
MC141			
MC111	1,15,16	8	-
MC124, MC125	16	8	9
MC173, 176	16	8	-



Pin connections on this page are to J2, a DA37S connector