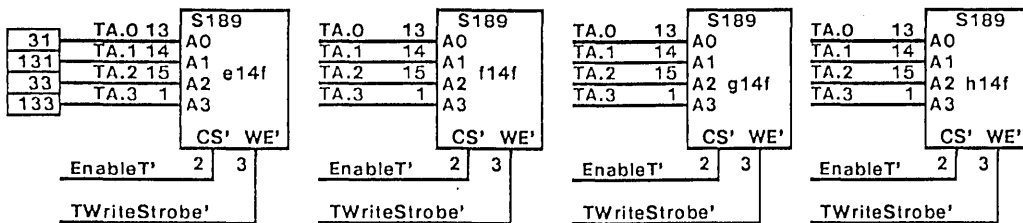
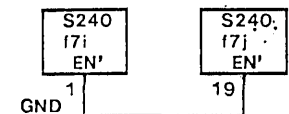
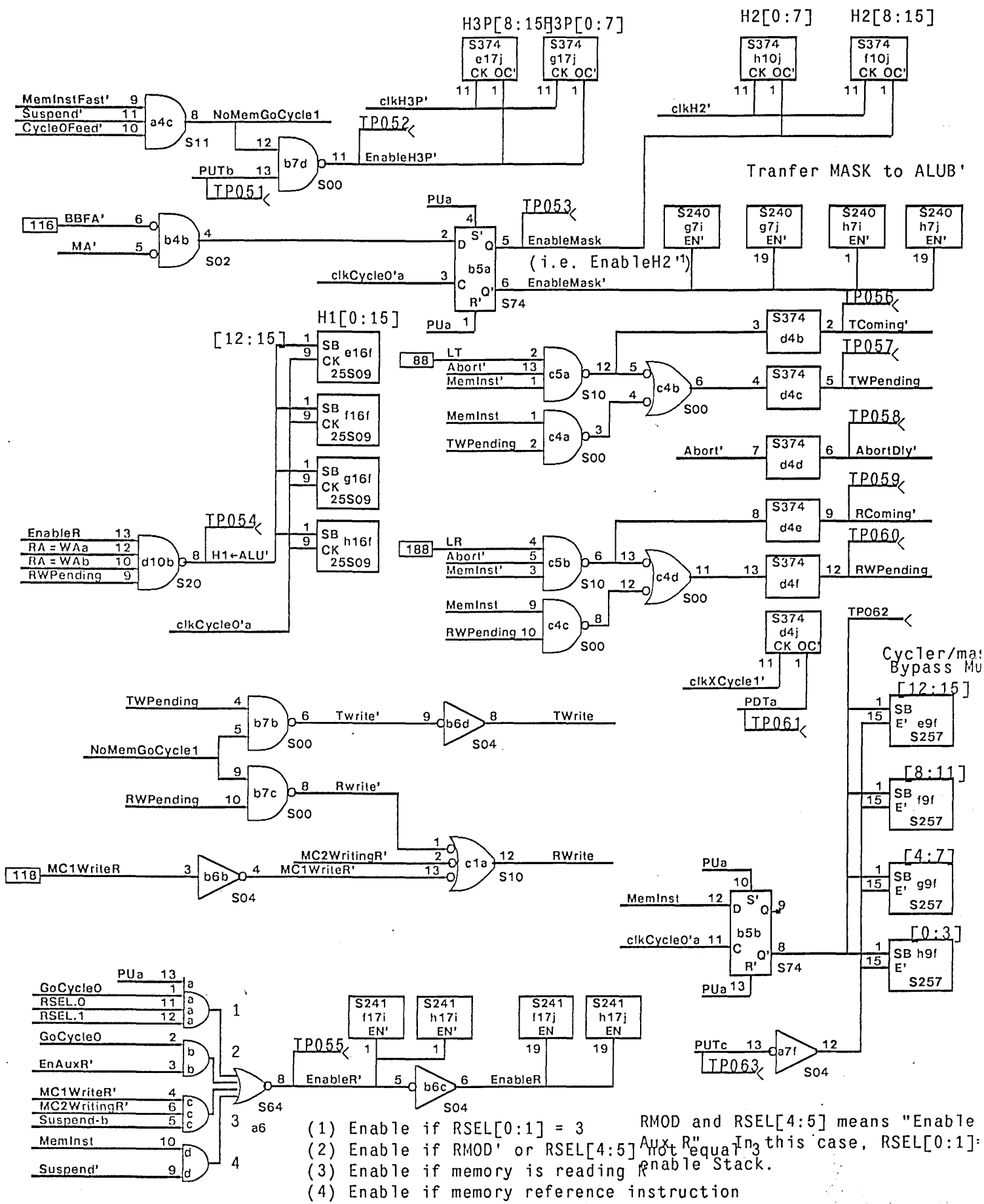


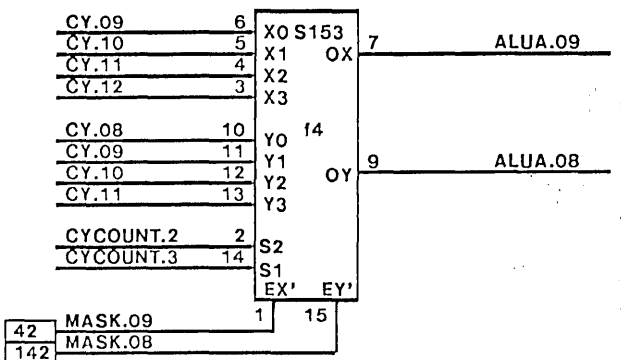
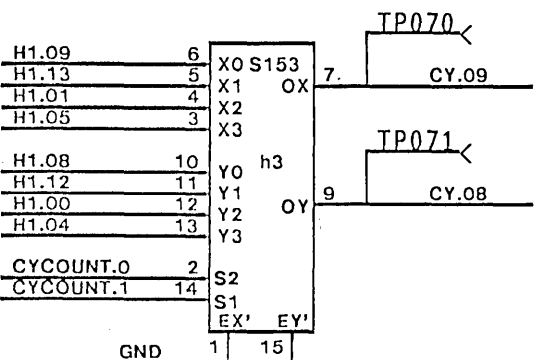
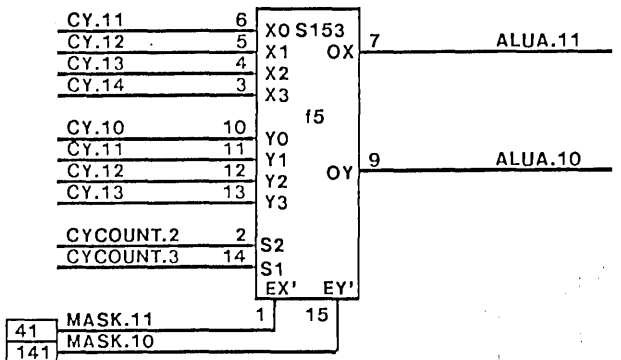
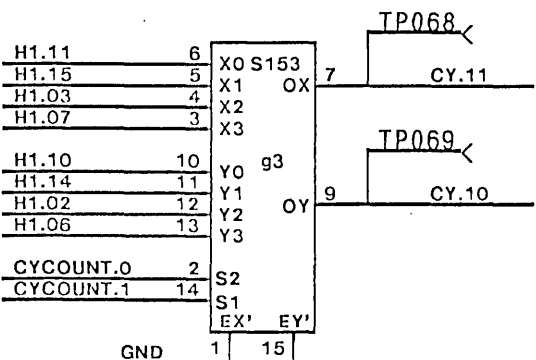
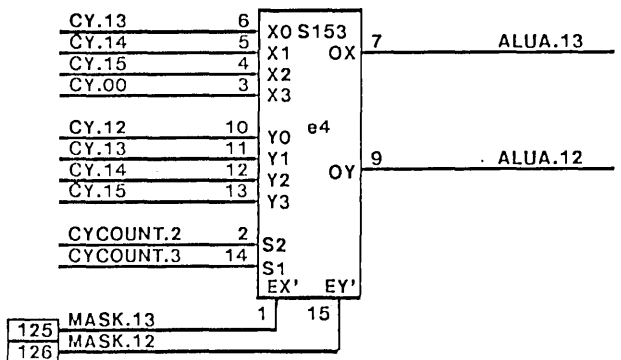
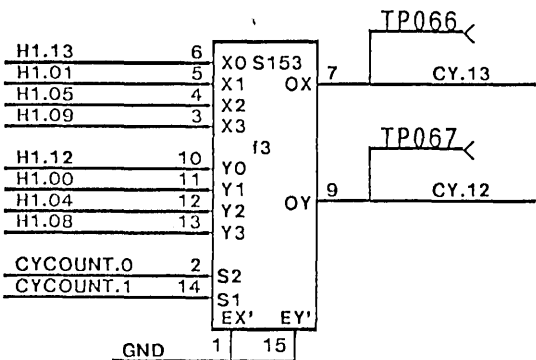
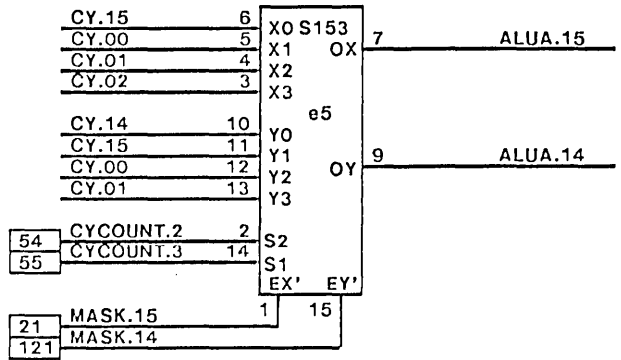
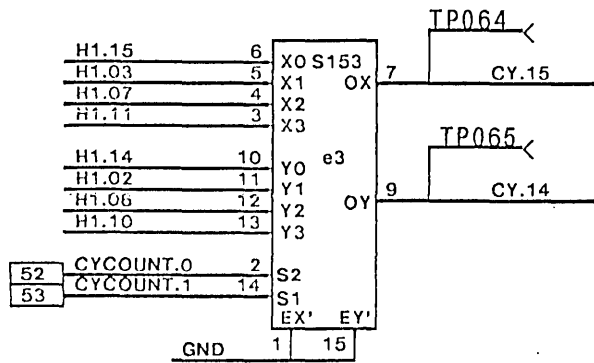
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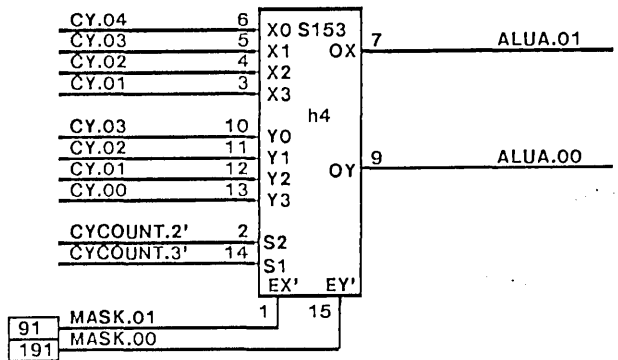
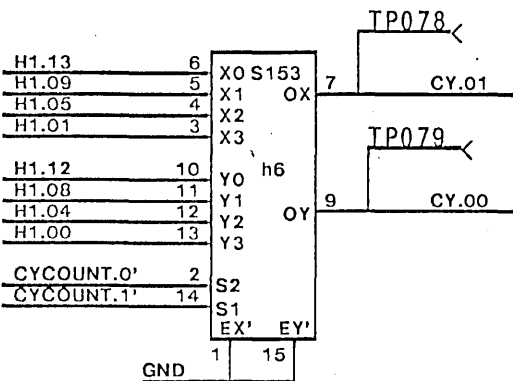
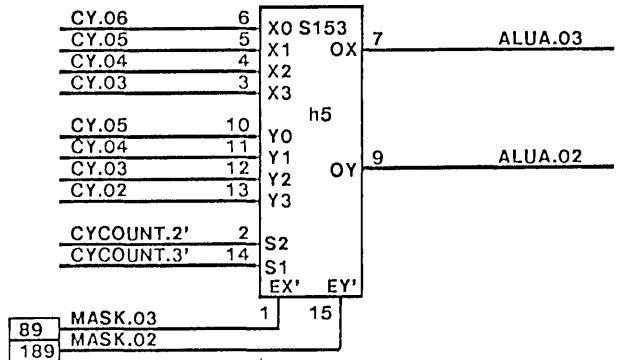
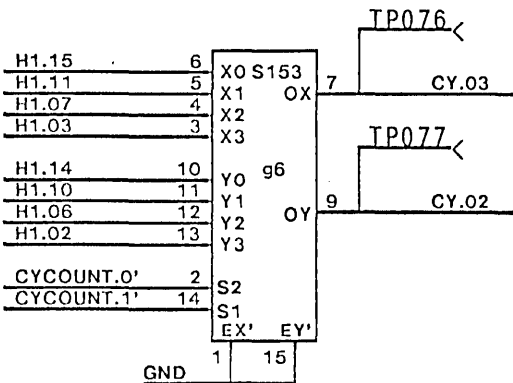
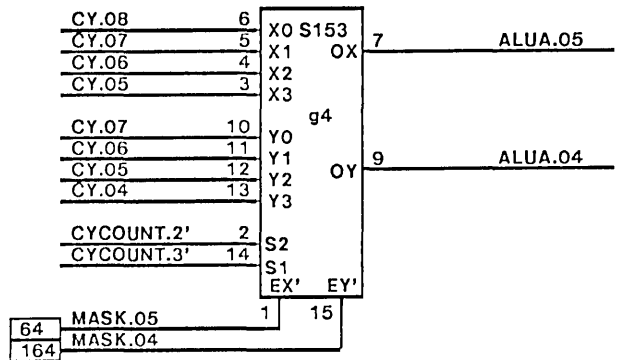
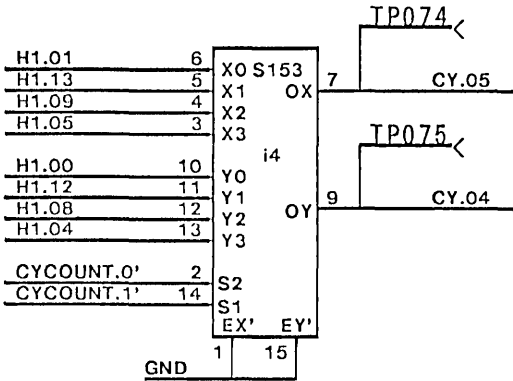
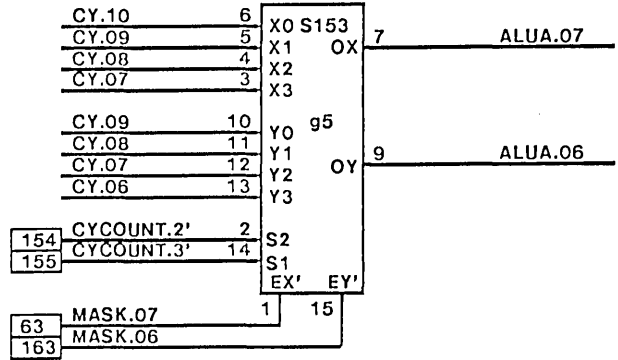
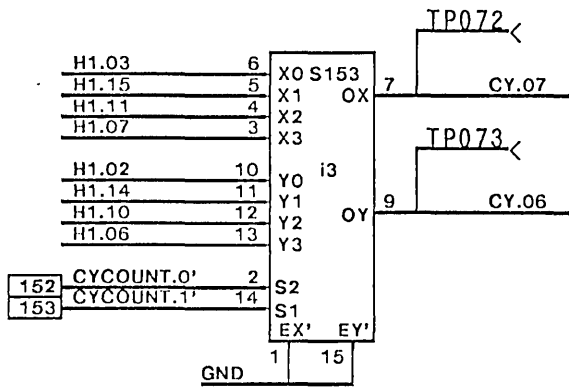


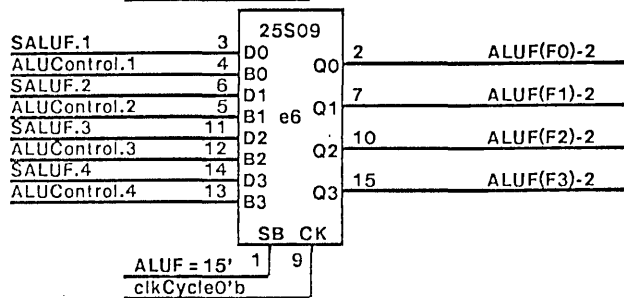
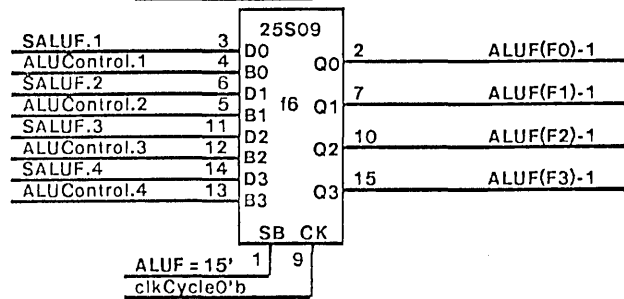
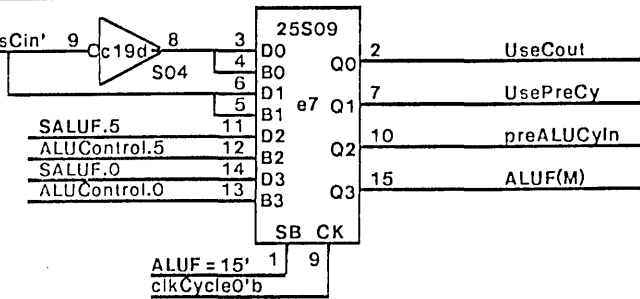
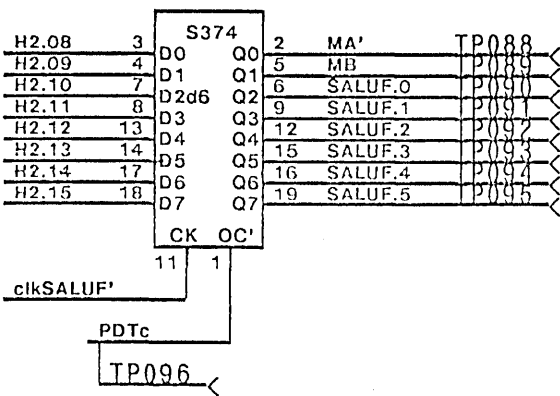
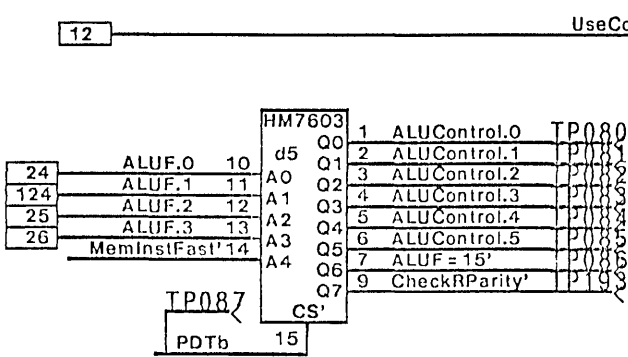
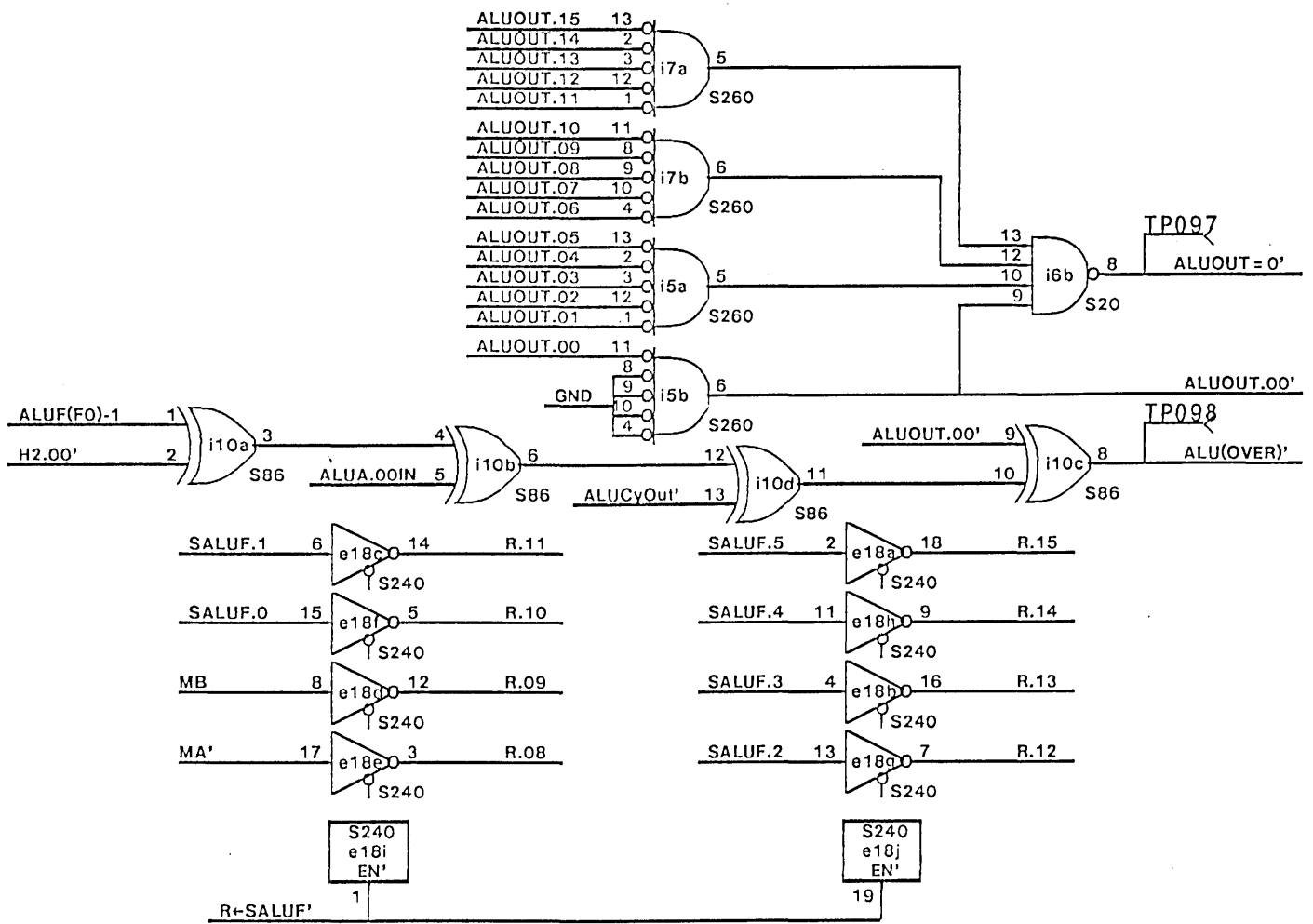
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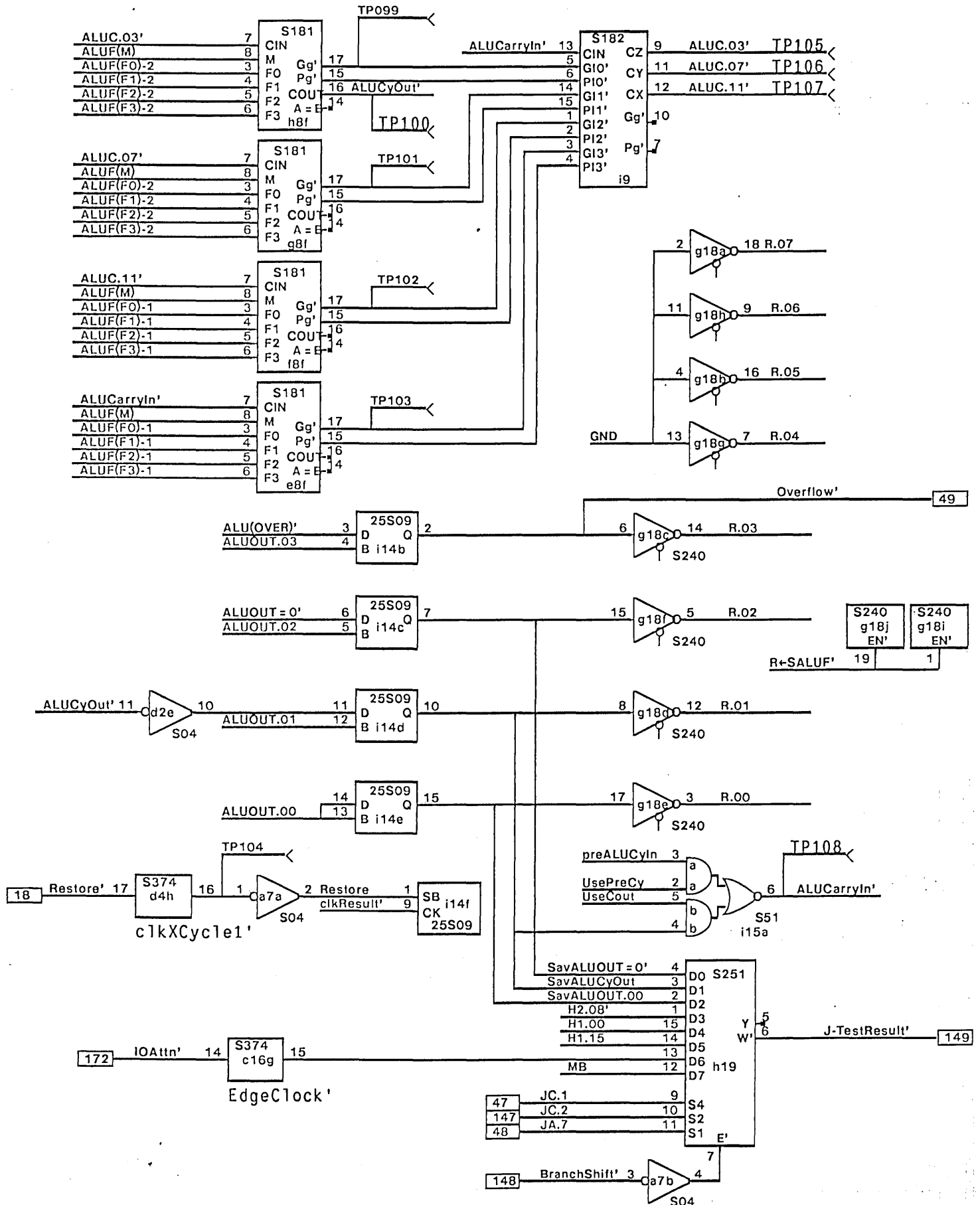




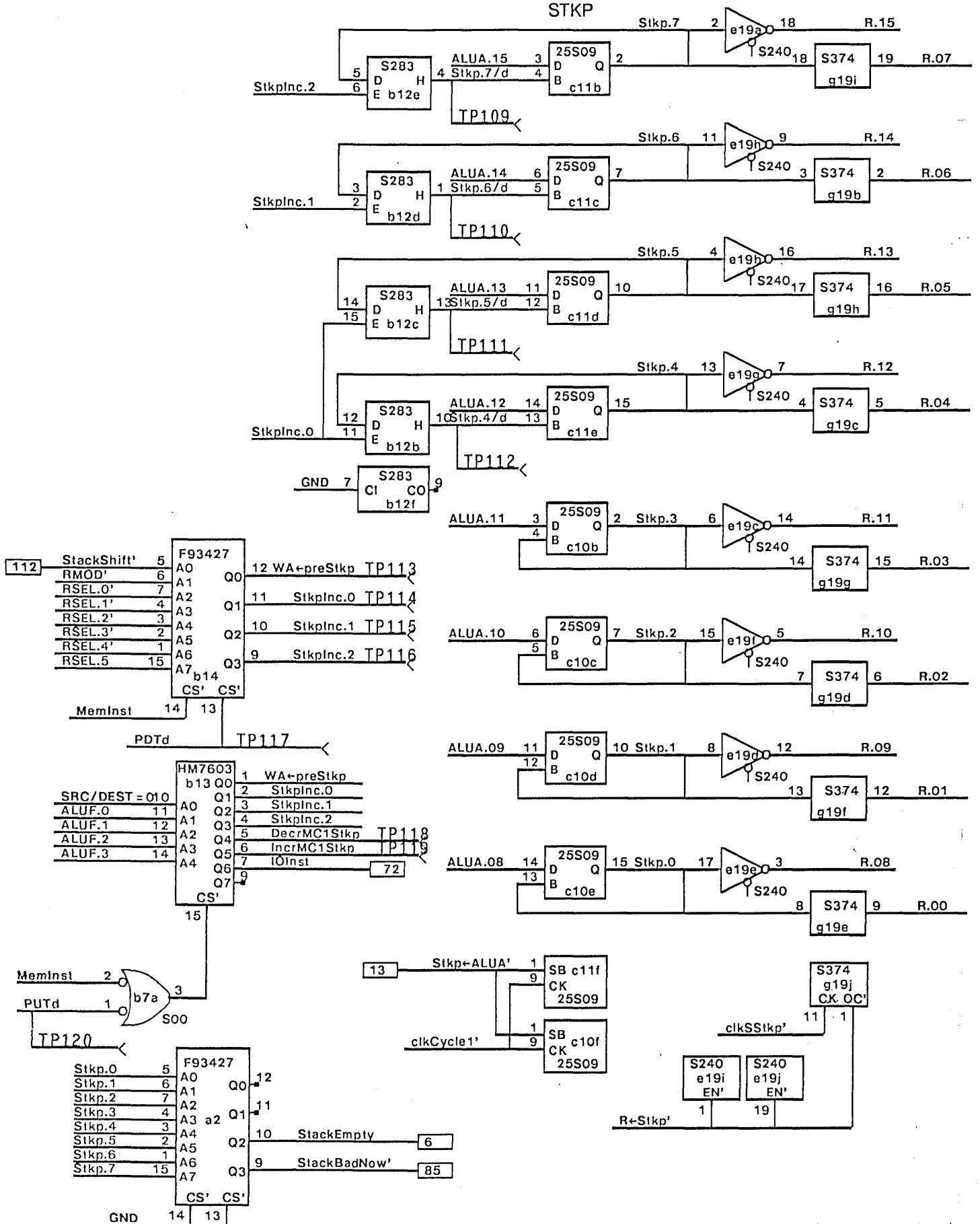


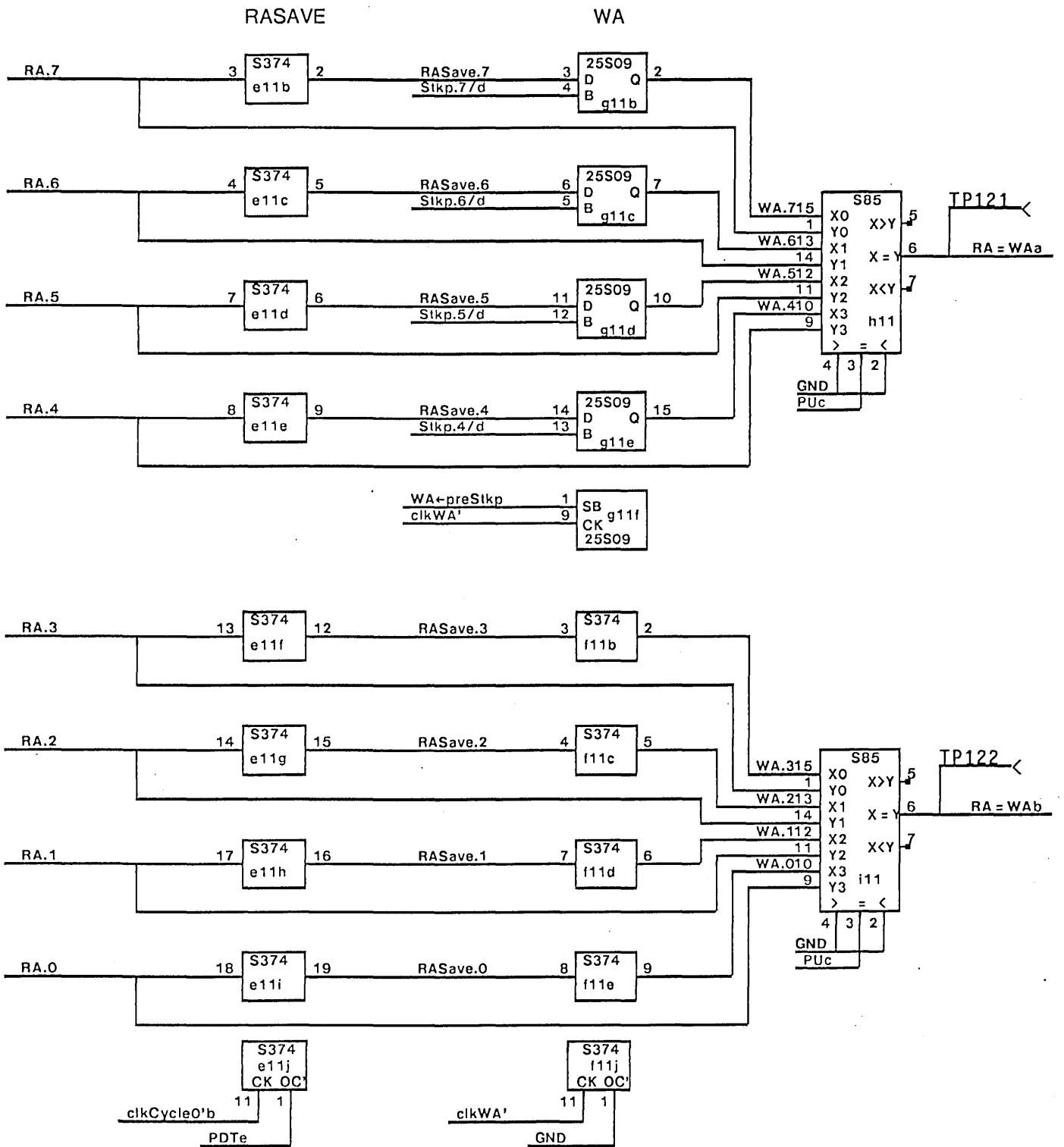


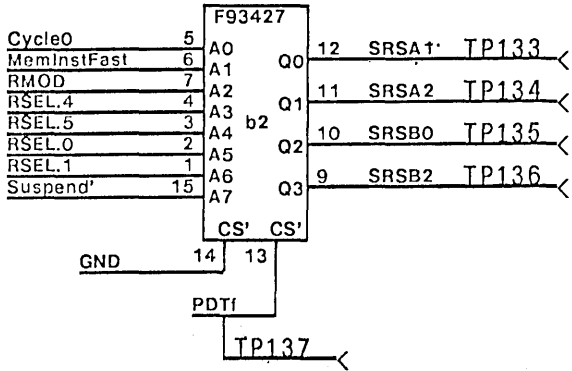
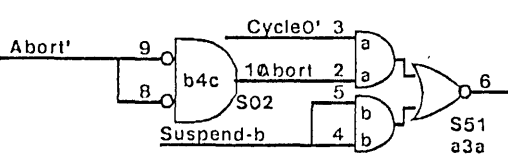
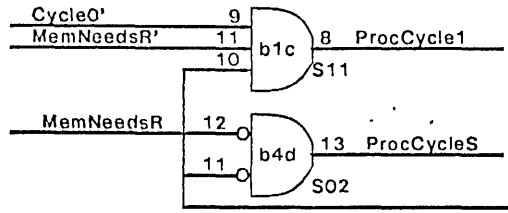
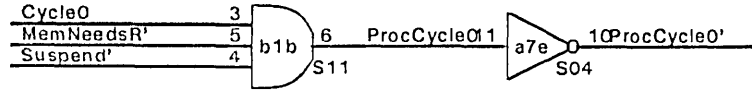
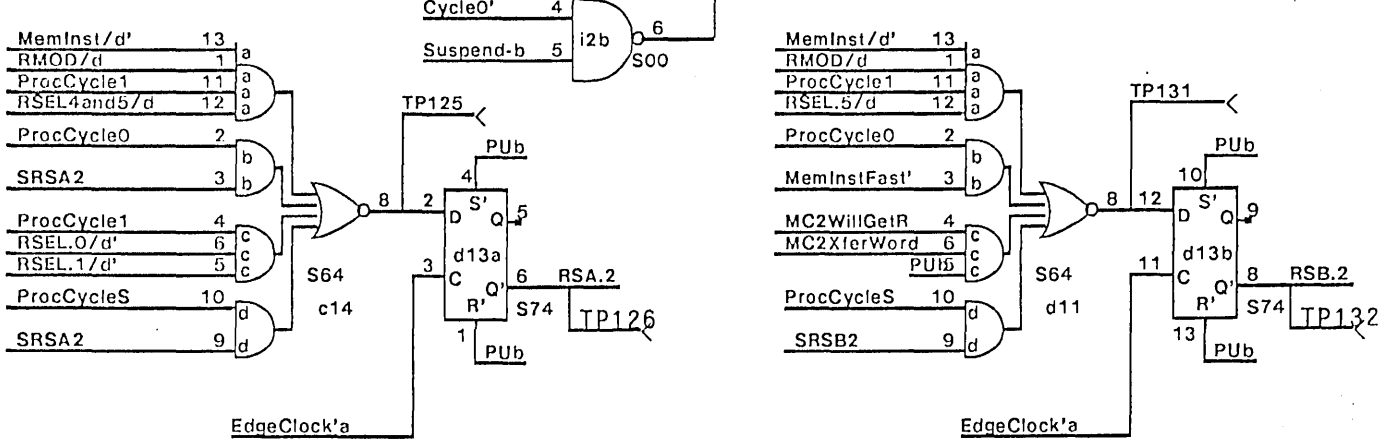
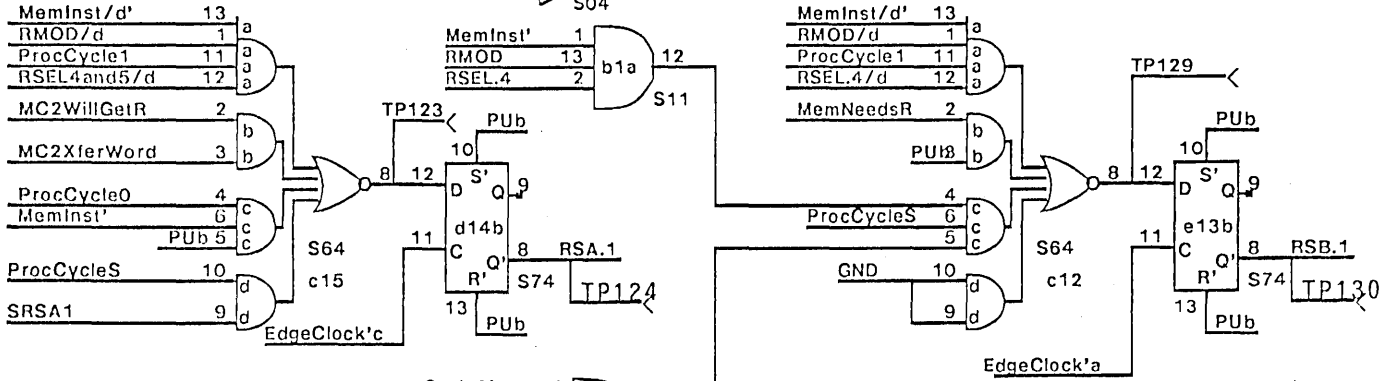
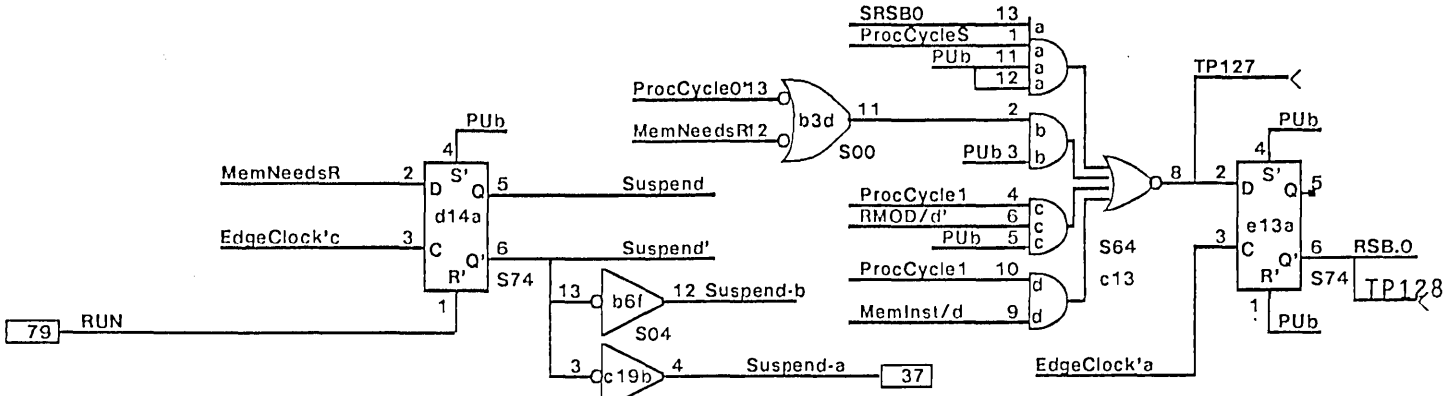


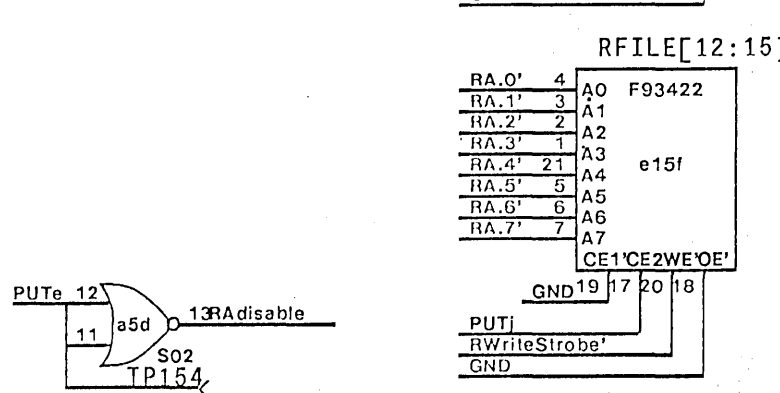
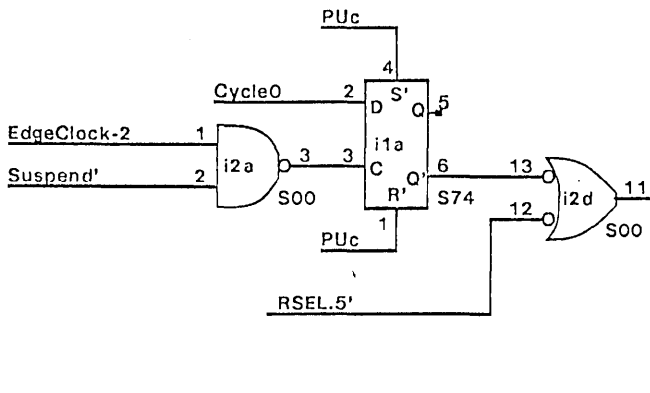
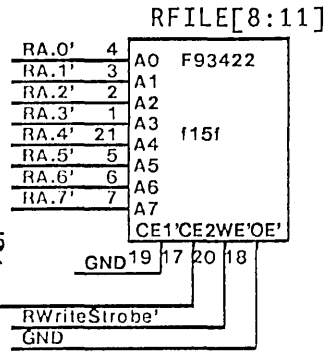
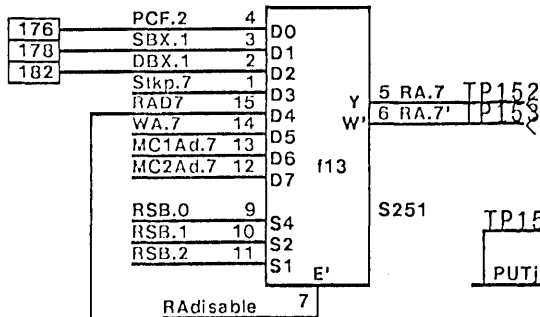
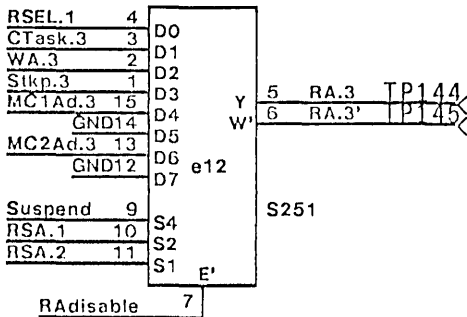
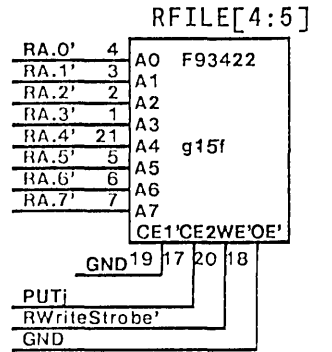
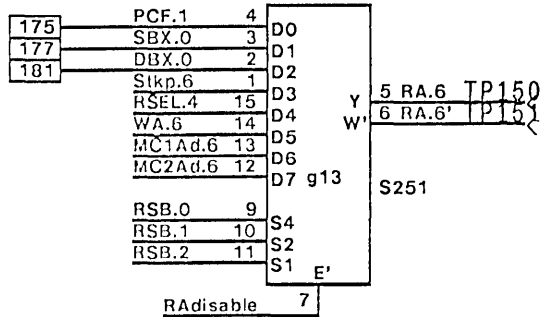
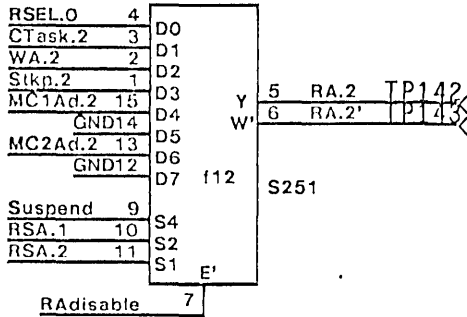
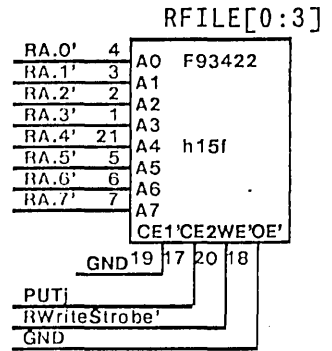
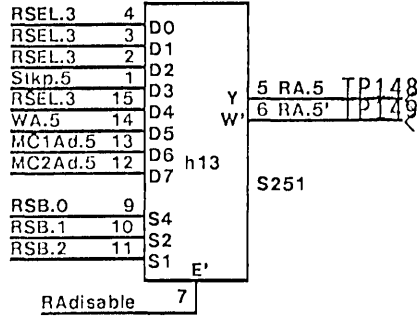
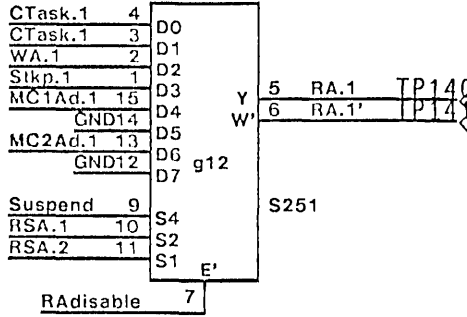
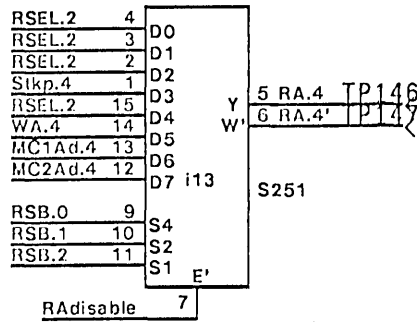
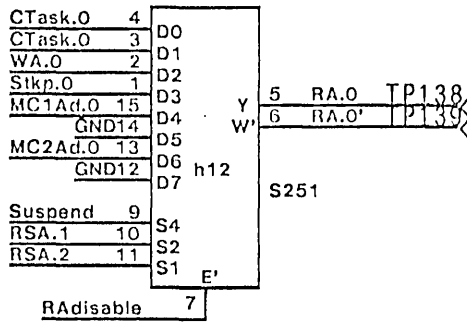


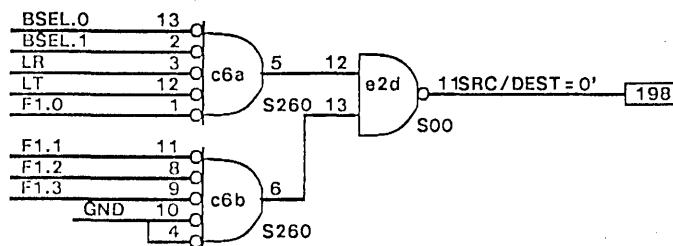
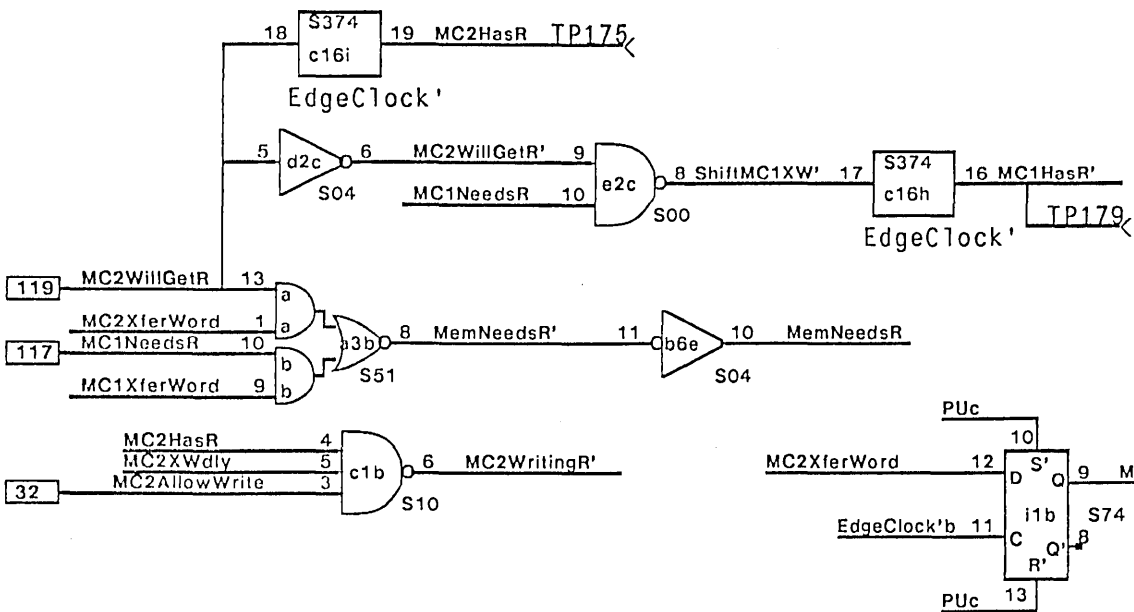
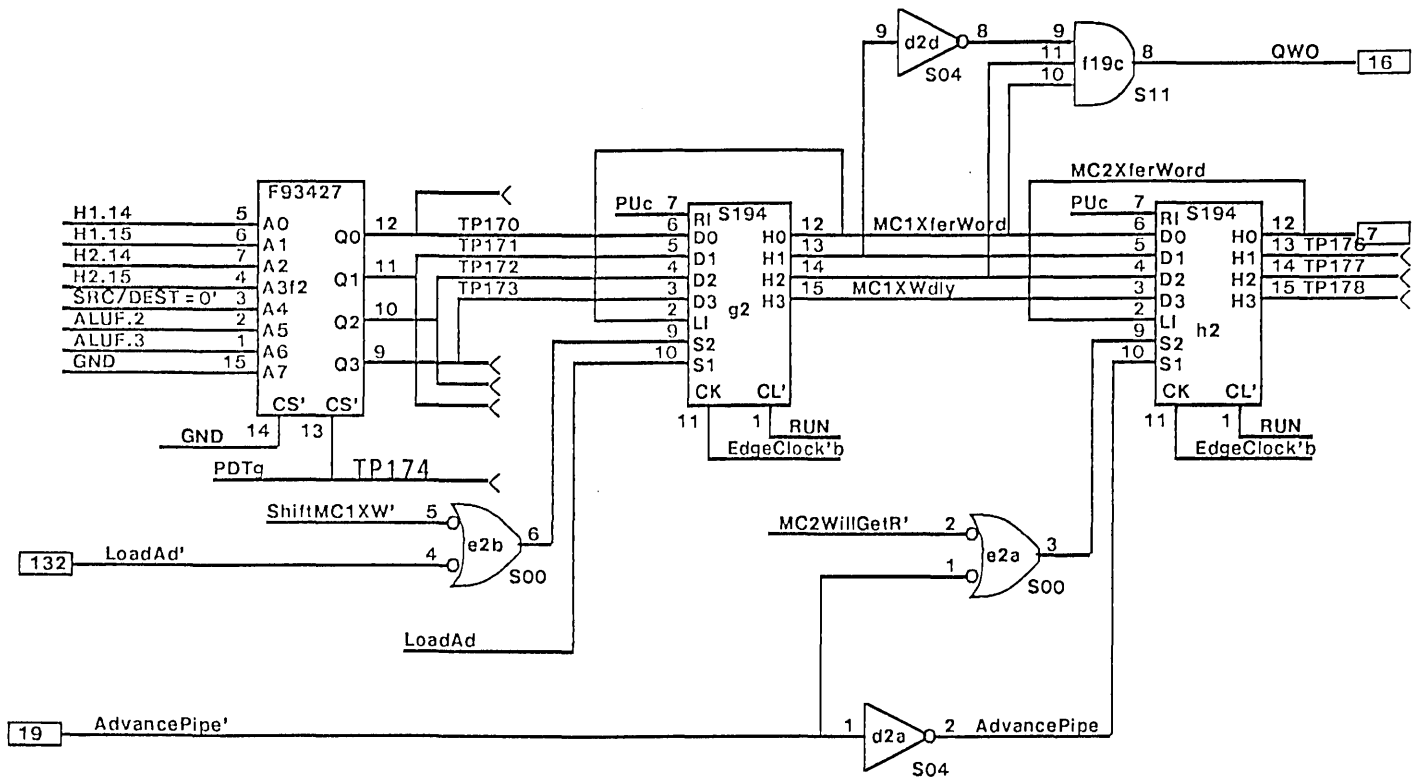
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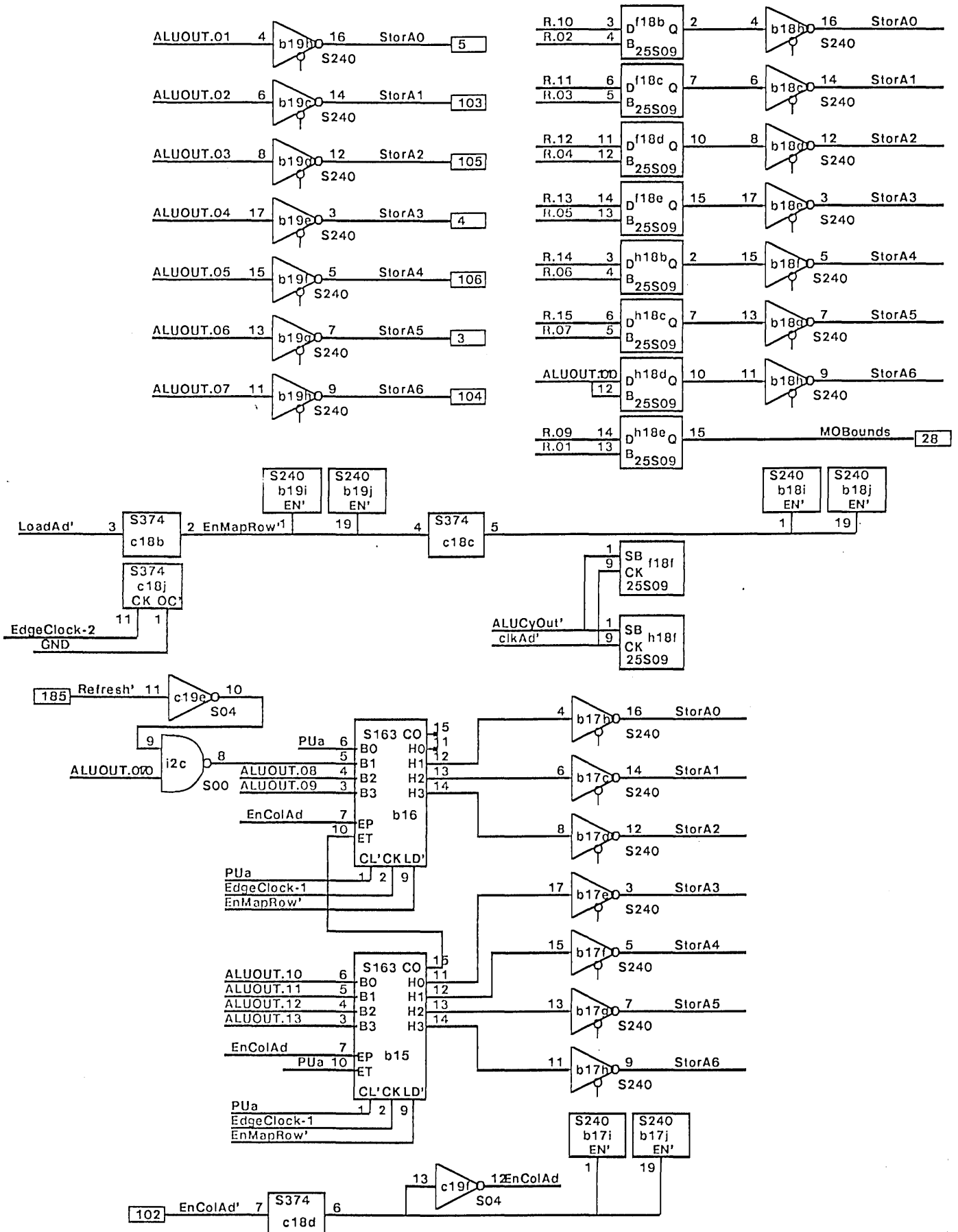


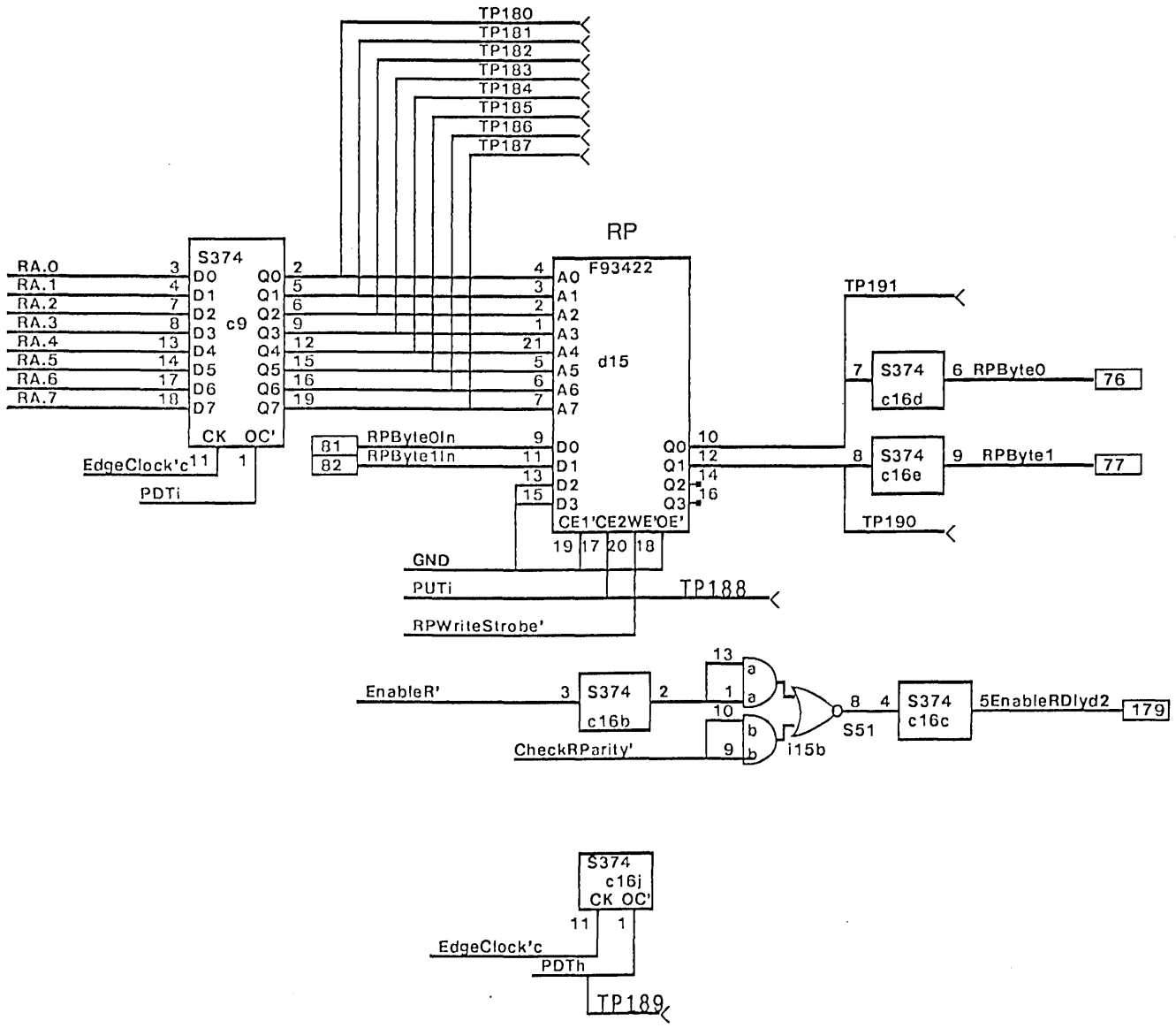


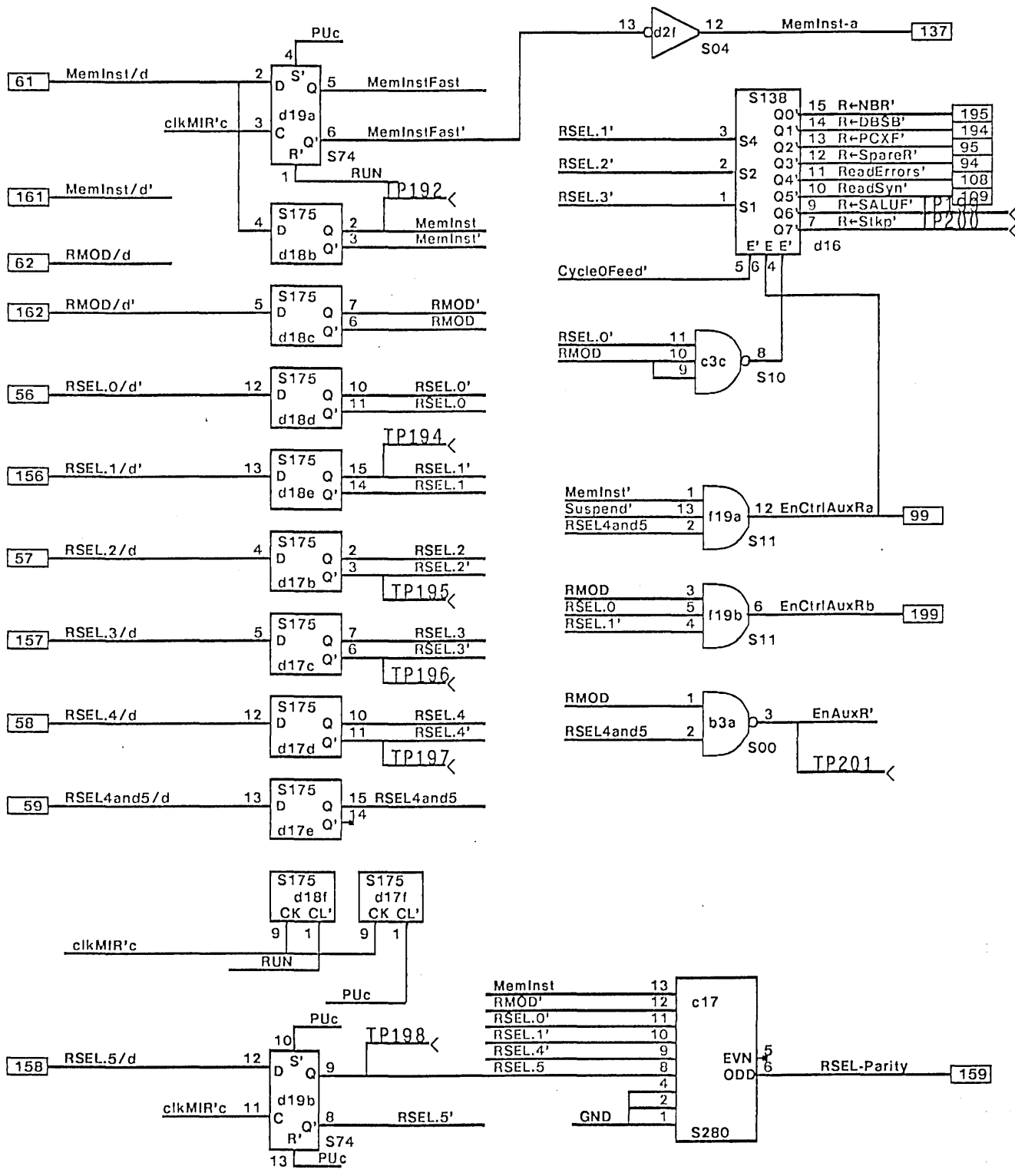


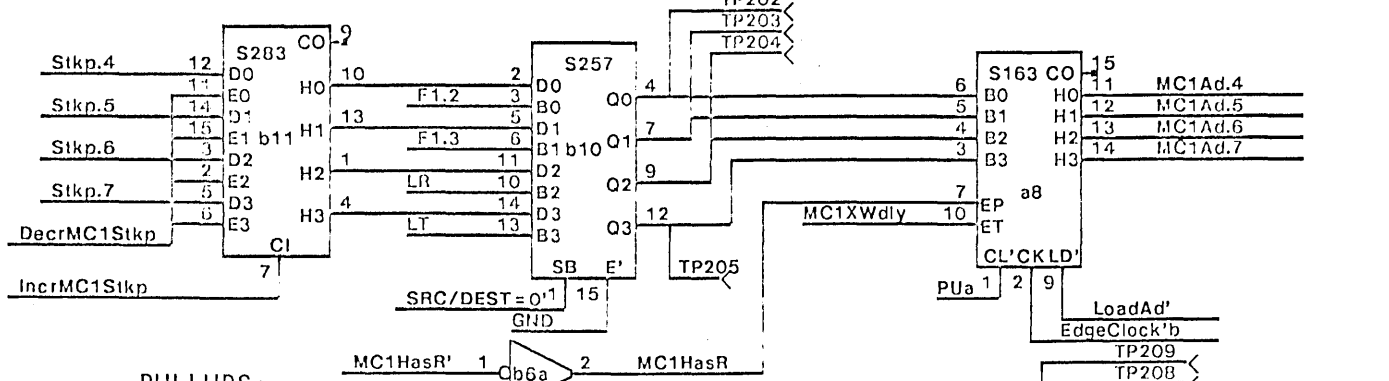
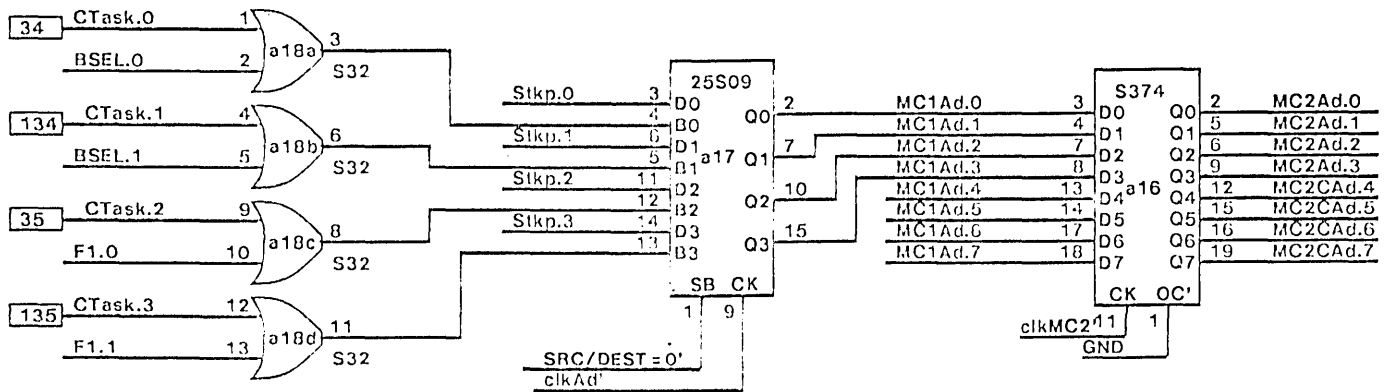








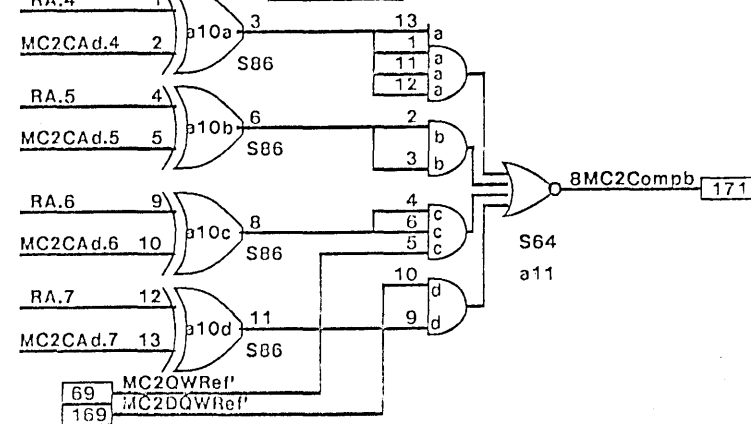
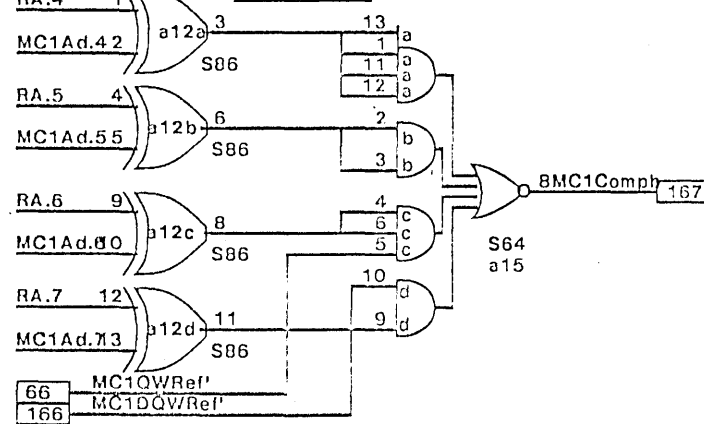
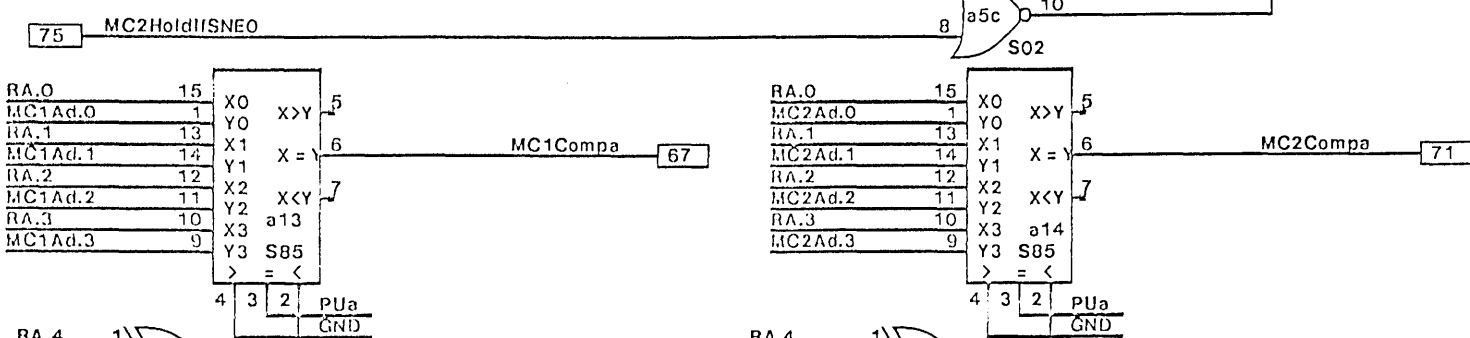
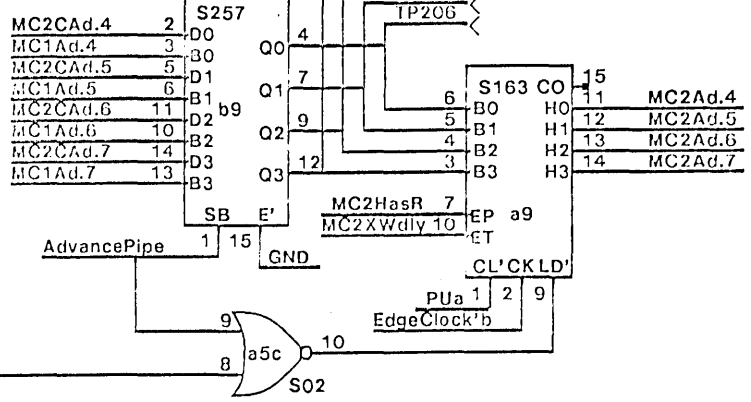


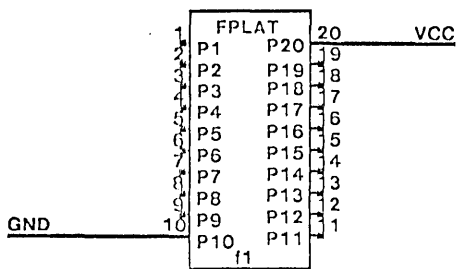
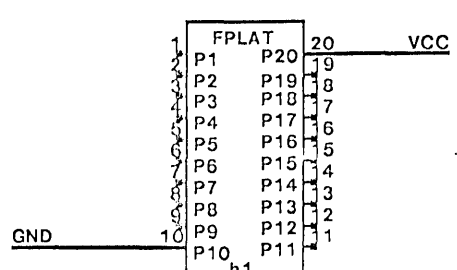
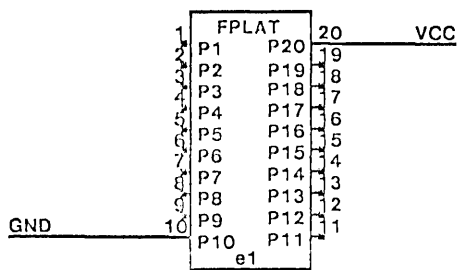
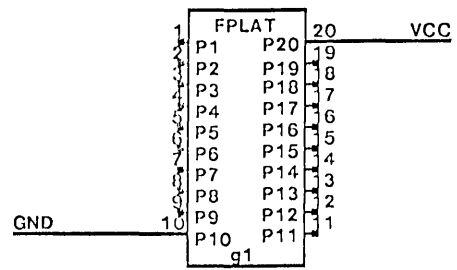
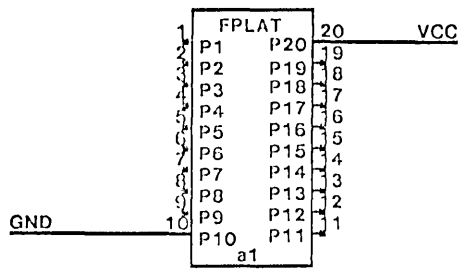


PULLUPS:
B898-1-R1K
(centered in 20pin package)

PULLDOWNS:
B898-1-R1K

FPLAT 20 VCC			FPLAT 20VCC		
PUa	1	P1	PDTa	1	P1
PUb	2	P2	PDTb	2	P2
PUc	3	P3	PDTc	3	P3
PUTa	4	P4	PDTd	4	P4
PUTb	5	P5	PDTe	5	P5
PUTc	6	P6	PDTf	6	P6
PUTd	7	P7	PDTg	7	P7
PUTe	8	P8	PDTg	8	P8
GND	9	P9	PDTg	9	P9
	10	P10	PDTg	10	P10
		P11	PDTg	11	P11





Changes for revision G to H:

- 1) Added clkH2' (pg 6,15).
- 2) Added output CheckRParity' to prom d5 (pg 9) and S51 i15b (pg 18) to check parity only when R is read.
- 3) Added (pg 6) gates i2b, a3a, and b4c to correct deficiencies in R address calculation.
- 4) Added signal PUTj (pg 14, 20) for test.
- 5) Added signal PUTk and gate b3c (pg 15,20) for test.
- 6) Added signal PDTi (pg 18,20) for test.

Changes for revision H to I:

- 1) Changed signal named HighByte←F1F2 to HighByte←F1F2' and changed dwg. of gate c3a (pg5).
- 2) Removed sign extension feature for constants in arithmetic operations. Changed signals SignExtendF1F2 to GND (pg 3,4) and removed gate a4a (pg 5).
- 3) Changed clear input of d18 from PUC to RUN (pg 19).
- 4) Eliminated (redundant) signal LoadMC1 (p16). This signal is now LoadAd. Changed gate at c3b (S10) to S00 (e2b).
- 5) f2.15 is now GND, was MemInst' (pg 16).
- 7) Changed ALUA.08In-ALUA.15IN to ALUA.08-ALUA.15 (stkp input, pg 11).
- 8) Added S240's to force R[04:07] to ONE during R←SALUF (pg 10).
- 9) Added test points. If signal was named, t.p is added in italics. If not, signal name is now TPxxx.

Changes for revision I to J (6/26/78)

- 1) Replaced signal Cycle0' with Cycle0Feed' at a4.10 (pg 6)
- 2) Changed PUB to MC2XferWord at c15.3 (pg 13)
- 3) Changed PUB to MC2XferWord at d11.6 (pg 13)
- 4) Generated MC1XWdly at g2.15 - added feedback from g2.12 to g2.2, removed PUC from g2.2 (pg 16)
- 5) Renamed MC1WillGetR' to ShiftMC1XW' (pg 16)
- 6) Generated MemNeedsR' in S51 at a3b rather than in S02 at b4a (pg 16)
- 7) Generated MC2XWdly in S74 at i1b (pg 16)
- 8) a8.10 is now connected to MC1XWdly (was MC1HasR) (pg 20)

Changes for revision J to K (8/29/78)

- 1) Shuffled inputs to decoder d16 and gate c3c, connected d16.5 to Cycle0Feed' (pg 19).
- 2) Changed gate c8a to S10 at c3b to form clkSS1kp' (pg 15).
- 3) Changed a4.2,5,10,13 from MC2Ad.x to MC2CA.x to make Raddress interlocking during single errors work properly (pg20).

Changes for revision K to revision L (10/7/78)

- 1) Changed inputs of c14 section b (pg13) from GND to ProcCycle0 and SRSA2. This requires revision E for Prom b2.
- 2) Connected clear inputs of g2 and h2 (pg16) to RUN rather than Puc. (required to initialize XferWord regs. at boot).
- 3) Reversed order of test points TP206-TP209 (pg 20).

Changes for revision L to revision M (12/9/78).

- 1) Changed h19.1 from QWO to H2.08' (pg 10). Branch on QWO is now done on Control Store.
- 2) Added flip-flop c18d in line EnColAd' (pg 17). Memory Control rev M is required with this change.
- 3) Added PROM a2 (at revision F) to check Stack overflow (pg 11).
- 4) Removed signal MC1XferWord from E006 to make room for new signal StackEmpty (pg 16).

Note: Revision M = Revision Ga

Current Prom Revisions:

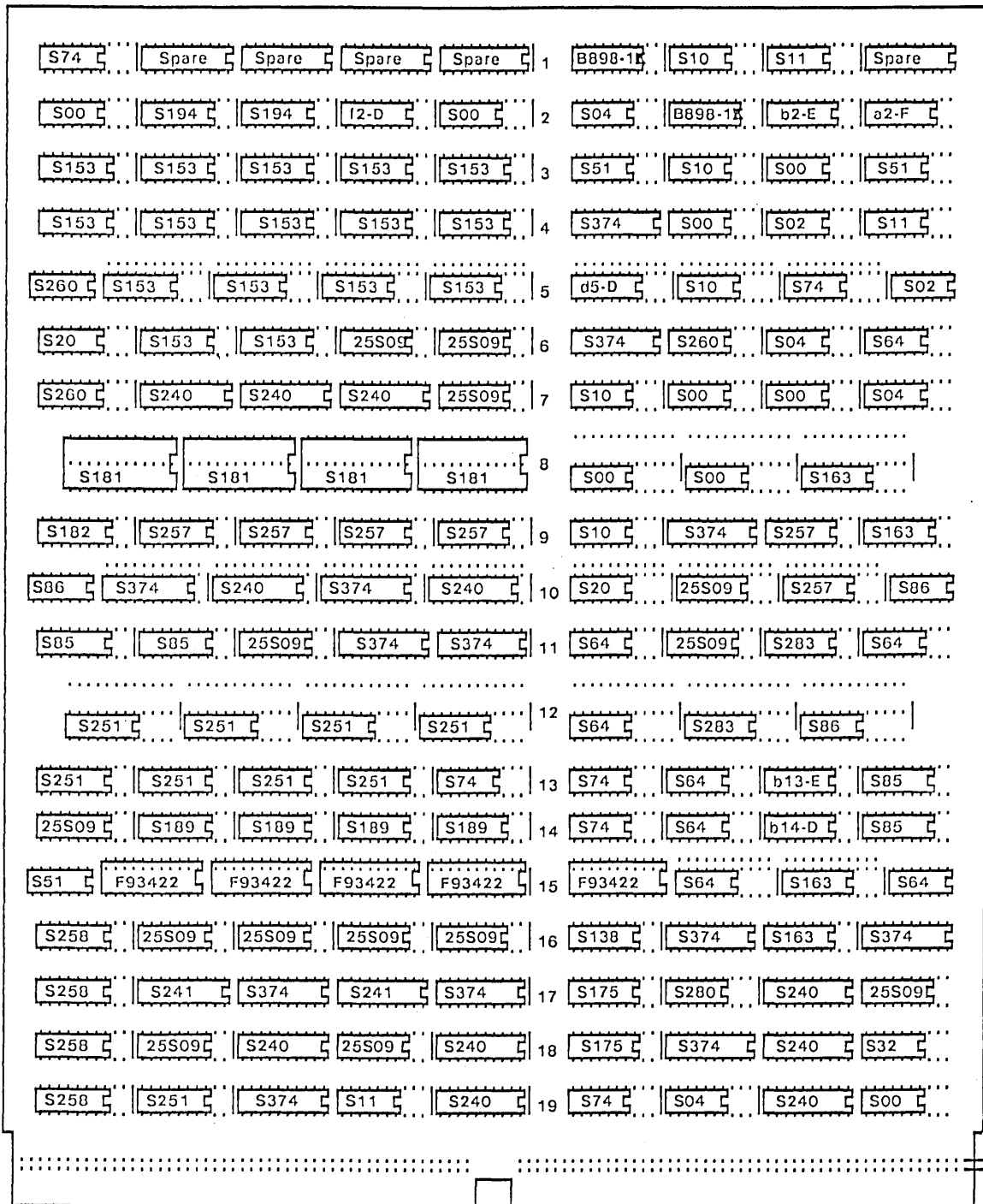
- a2: F
- d5: D
- b14: D
- b13: E
- f2: D
- b2: E

Note: This board contains no platforms. The "Plats" at positions c2 and d1 are Beckman B898-1-R1K resistor networks (15 1K resistors with pin 16 common).

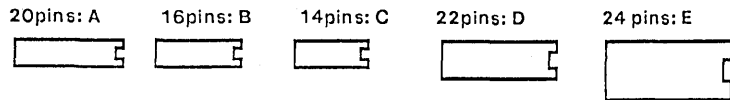
Equivalent networks from other manufacturers may be substituted.

XEROX F00	Project D0	ALU Card CHANGES	File D0aluCHANGES.sil	Designer Thacker	Rev Ga	Date 2/19/79
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I H G F E D C B A



101-200
1-100



Note: The short vertical lines indicate filter capacitor locations.
(119 Total)