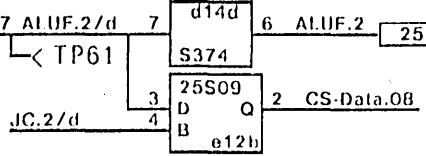
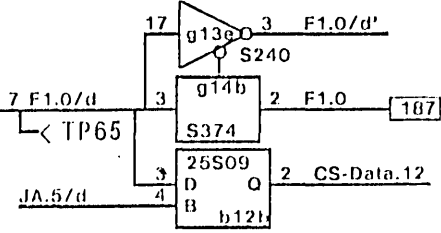


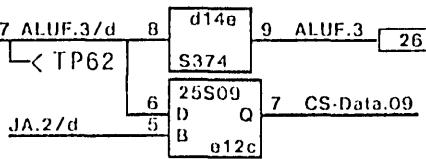
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TrmCS-A.02'a	3	A1
TrmCS-A.03'a	4	A2
TrmCS-A.04'a	5	A3
TrmCS-A.05'a	6	A4
TrmCS-A.06'a	17	A5
TrmCS-A.07'a	16	A6
TrmCS-A.08'a	15	A7
TrmCS-A.09'a	14	A8
TrmCS-A.10'a	13	A9
TrmCS-A.11a	12	A10
CSIn.08	11	A11
WE-CS-High'b	8	DIN
CsChipSel'a	10	WE'
		CS' e11



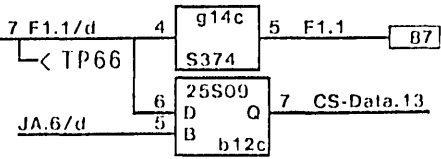
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TrmCS-A.03'a	4	A2
TrmCS-A.04'a	5	A3
TrmCS-A.05'a	6	A4
TrmCS-A.06'a	17	A5
TrmCS-A.07'a	16	A6
TrmCS-A.08'a	15	A7
TrmCS-A.09'a	14	A8
TrmCS-A.10'a	13	A9
TrmCS-A.11a	12	A10
CSIn.12	11	A11
WE-CS-High'b	8	DIN
CsChipSel'b	10	WE'
		CS' d10



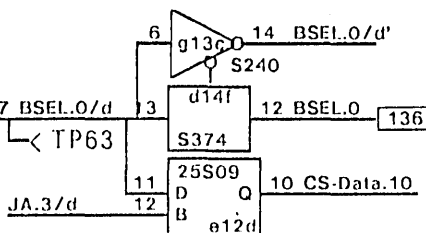
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TrmCS-A.04'a	5	A3
TrmCS-A.05'a	6	A4
TrmCS-A.06'a	17	A5
TrmCS-A.07'a	16	A6
TrmCS-A.08'a	15	A7
TrmCS-A.09'a	14	A8
TrmCS-A.10'a	13	A9
TrmCS-A.11a	12	A10
CSIn.09	11	A11
WE-CS-High'b	8	DIN
CsChipSel'a	10	WE'
		CS' d11



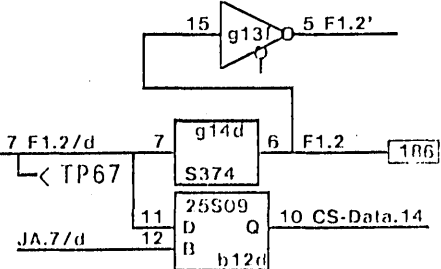
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TrmCS-A.03'a	4	A2
TrmCS-A.04'a	5	A3
TrmCS-A.05'a	6	A4
TrmCS-A.06'a	17	A5
TrmCS-A.07'a	16	A6
TrmCS-A.08'a	15	A7
TrmCS-A.09'a	14	A8
TrmCS-A.10'a	13	A9
TrmCS-A.11a	12	A10
CSIn.13	11	A11
WE-CS-High'b	8	DIN
CsChipSel'b	10	WE'
		CS' c10



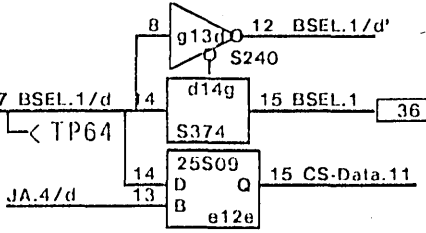
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TrmCS-A.03'a	4	A2
TrmCS-A.04'a	5	A3
TrmCS-A.05'a	6	A4
TrmCS-A.06'a	17	A5
TrmCS-A.07'a	16	A6
TrmCS-A.08'a	15	A7
TrmCS-A.09'a	14	A8
TrmCS-A.10'a	13	A9
TrmCS-A.11a	12	A10
CSIn.10	11	A11
WE-CS-High'b	8	DIN
CsChipSel'a	10	WE'
		CS' c11



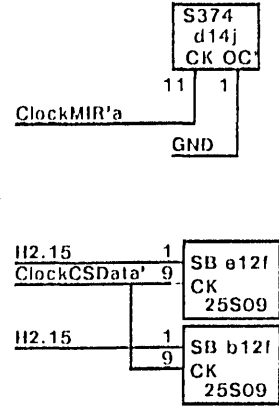
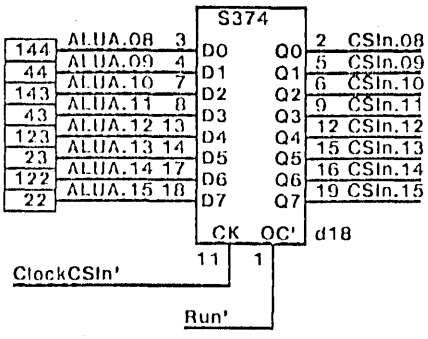
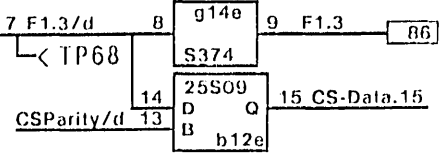
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TrmCS-A.03'a	4	A2
TrmCS-A.04'a	5	A3
TrmCS-A.05'a	6	A4
TrmCS-A.06'a	17	A5
TrmCS-A.07'a	16	A6
TrmCS-A.08'a	15	A7
TrmCS-A.09'a	14	A8
TrmCS-A.10'a	13	A9
TrmCS-A.11a	12	A10
CSIn.14	11	A11
WE-CS-High'b	8	DIN
CsChipSel'b	10	WE'
		CS' b10



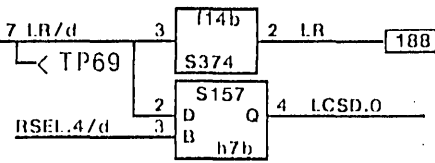
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TrmCS-A.03'a	4	A2
TrmCS-A.04'a	5	A3
TrmCS-A.05'a	6	A4
TrmCS-A.06'a	17	A5
TrmCS-A.07'a	16	A6
TrmCS-A.08'a	15	A7
TrmCS-A.09'a	14	A8
TrmCS-A.10'a	13	A9
TrmCS-A.11a	12	A10
CSIn.11	11	A11
WE-CS-High'b	8	DIN
CsChipSel'a	10	WE'
		CS' b11



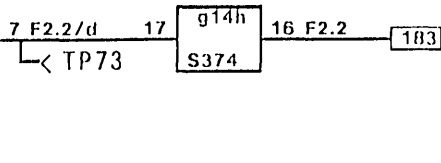
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TrmCS-A.03'a	4	A2
TrmCS-A.04'a	5	A3
TrmCS-A.05'a	6	A4
TrmCS-A.06'a	17	A5
TrmCS-A.07'a	16	A6
TrmCS-A.08'a	15	A7
TrmCS-A.09'a	14	A8
TrmCS-A.10'a	13	A9
TrmCS-A.11a	12	A10
CSIn.15	11	A11
WE-CS-High'b	8	DIN
CsChipSel'b	10	WE'
		CS' b9



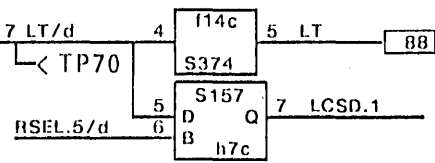
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.00	11	A11
WE-CS-Low'a	8	DIN
CsChipSel'b	10	WE'
		CS'



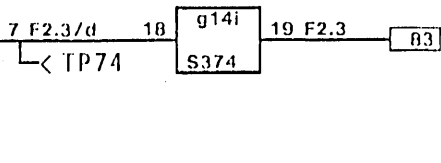
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.04	11	A11
WE-CS-Low'a	8	DIN
CsChipSel'b	10	WE'
		CS'



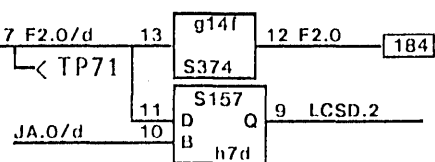
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.01	11	A11
WE-CS-Low'a	8	DIN
CsChipSel'b	10	WE'
		CS'



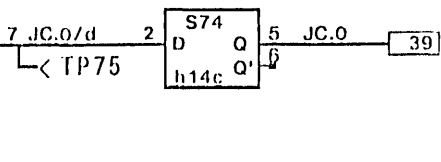
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.05	11	A11
WE-CS-Low'a	8	DIN
CsChipSel'b	10	WE'
		CS'



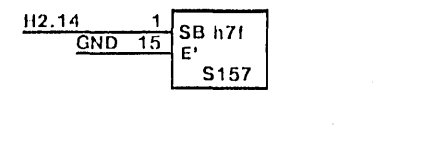
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.02	11	A11
WE-CS-Low'a	8	DIN
CsChipSel'b	10	WE'
		CS'



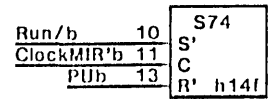
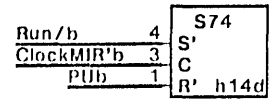
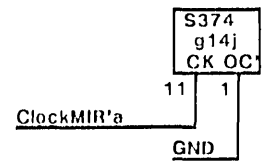
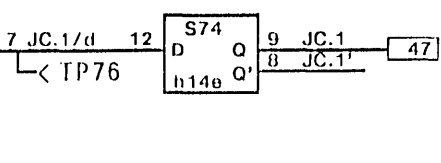
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.06	11	A11
WE-CS-Low'a	8	DIN
CsChipSel'b	10	WE'
		CS'



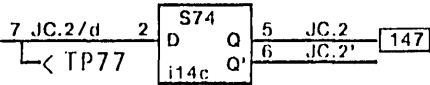
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.03	11	A11
WE-CS-Low'a	8	DIN
CsChipSel'b	10	WE'
		CS'



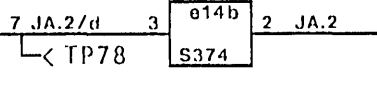
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.07	11	A11
WE-CS-Low'a	8	DIN
CsChipSel'b	10	WE'
		CS'



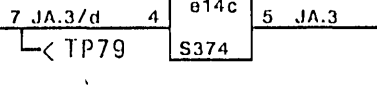
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.08	11	A11
WE-CS-Low'b	8	DIN
WE'		WE'
CsChipSel'c	10	CS' e9



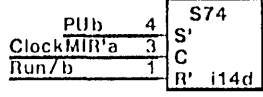
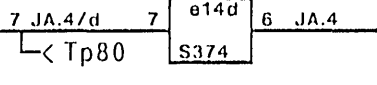
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TrmCS-A.03'b	4	A2
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TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.09	11	A11
WE-CS-Low'b	8	DIN
WE'		WE'
CsChipSel'c	10	CS' d9



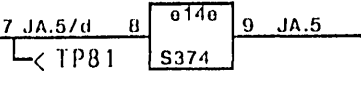
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TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.10	11	A11
WE-CS-Low'b	8	DIN
WE'		WE'
CsChipSel'c	10	CS' c9



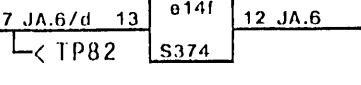
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TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.11	11	A11
WE-CS-Low'b	8	DIN
WE'		WE'
CsChipSel'c	10	CS' a8



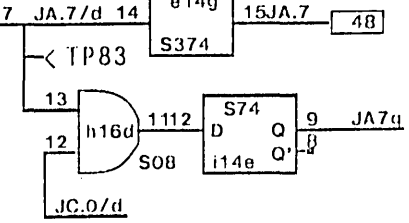
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.12	11	A11
WE-CS-Low'b	8	DIN
WE'		WE'
CsChipSel'c	10	CS' c8



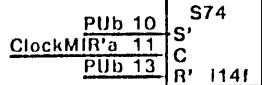
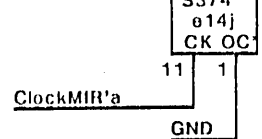
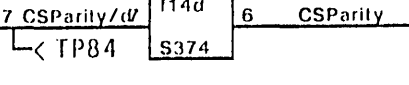
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TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.13	11	A11
WE-CS-Low'b	8	DIN
WE'		WE'
CsChipSel'c	10	CS' b8

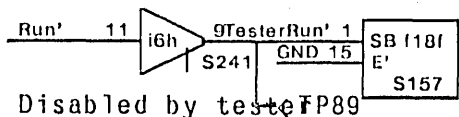
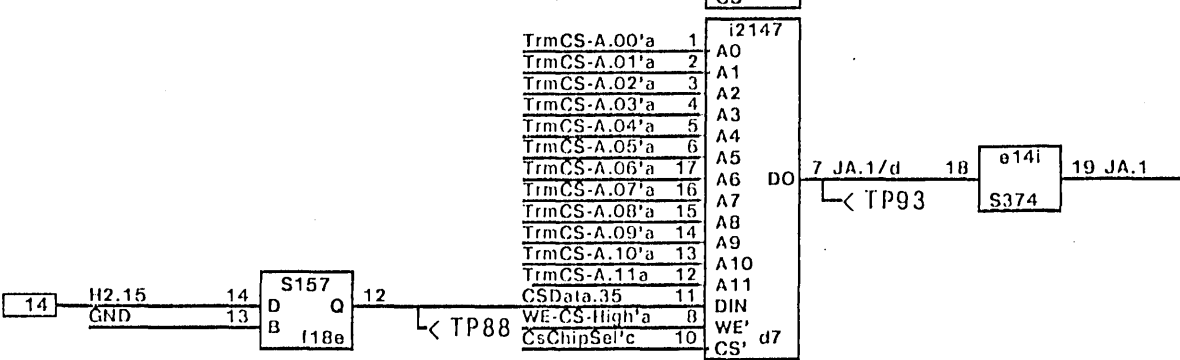
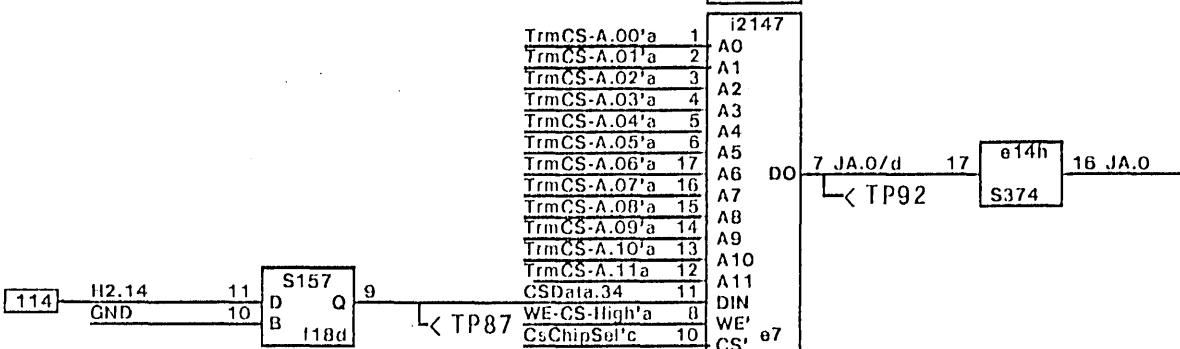
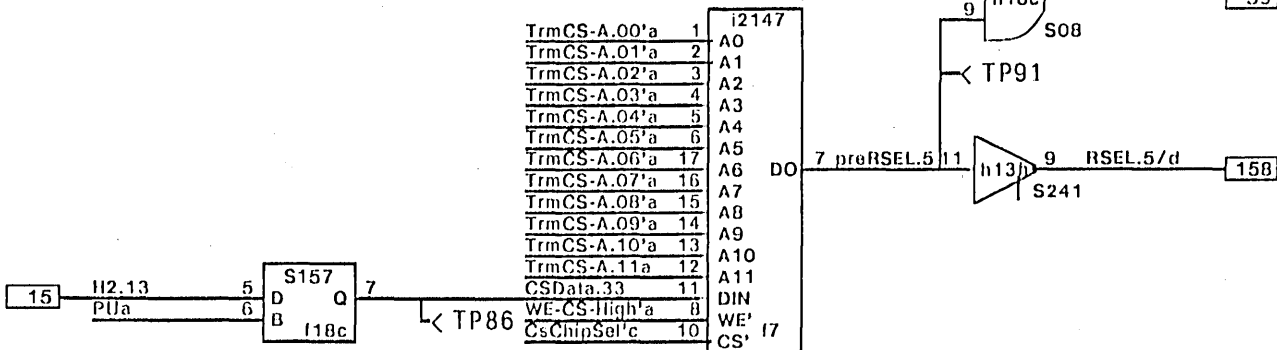
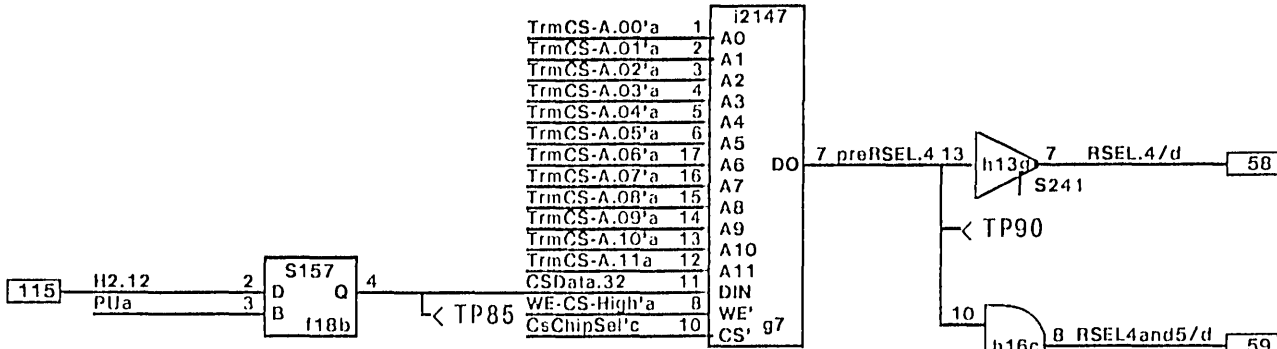


TrmCS-A.00'b	1	i2147
TrmCS-A.01'b	2	A0
TrmCS-A.02'b	3	A1
TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.14	11	A11
WE-CS-Low'b	8	DIN
WE'		WE'
CsChipSel'c	10	CS' c7



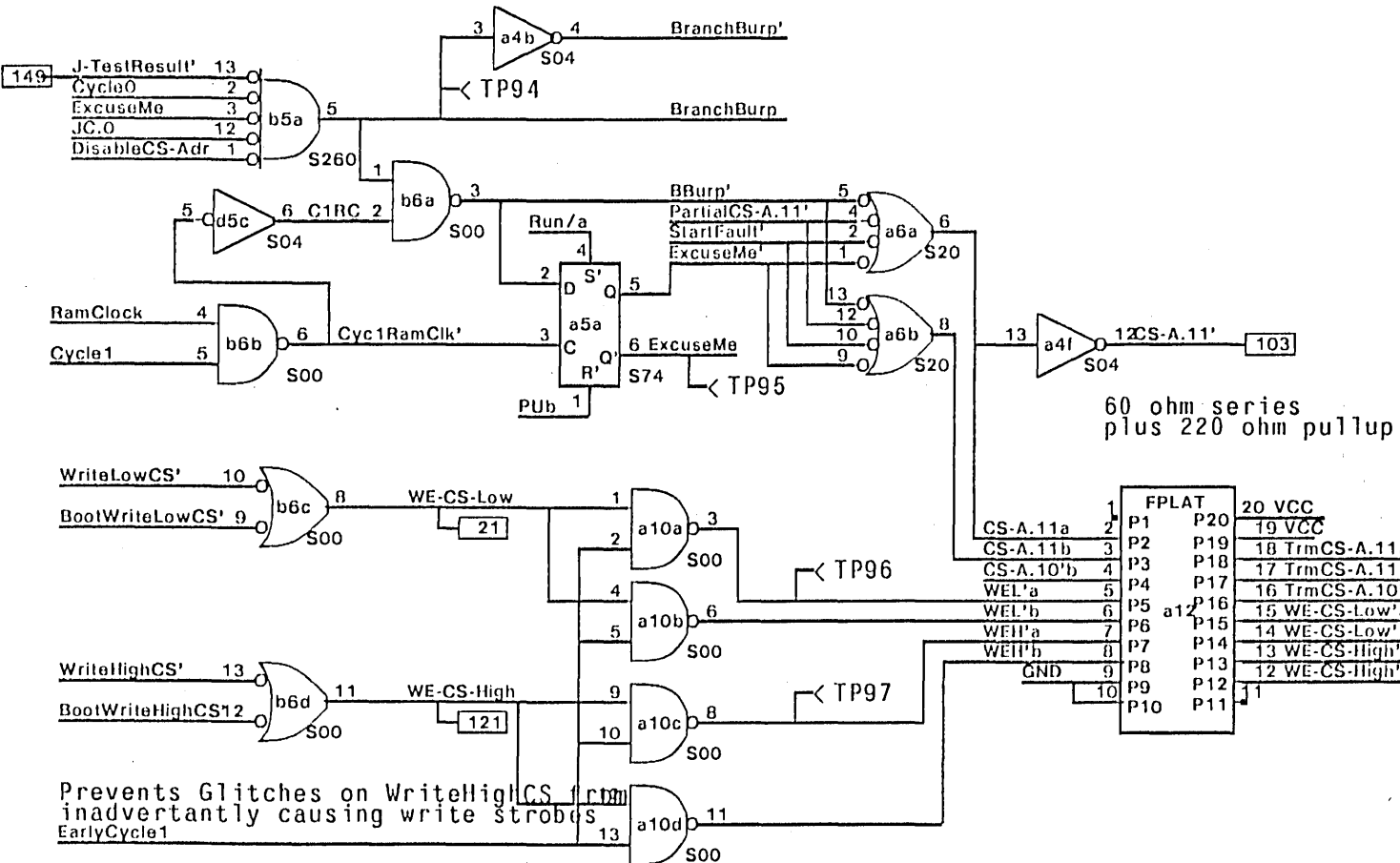
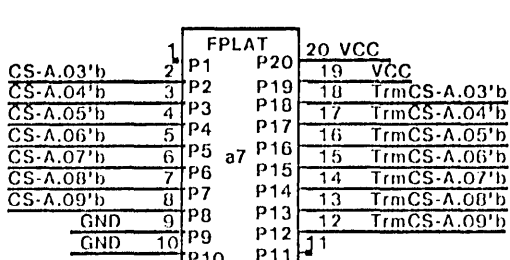
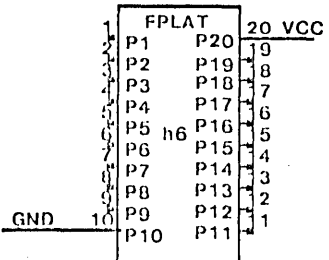
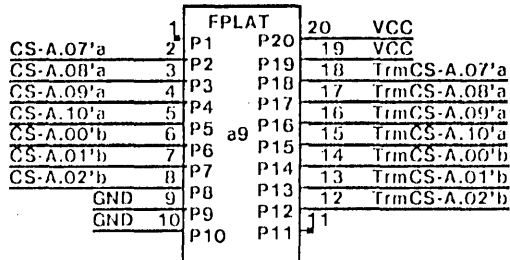
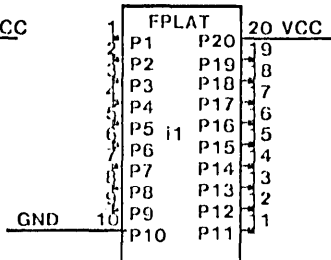
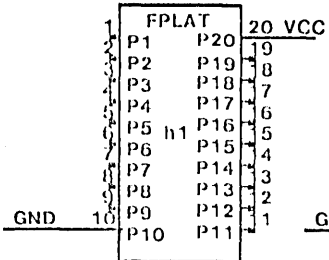
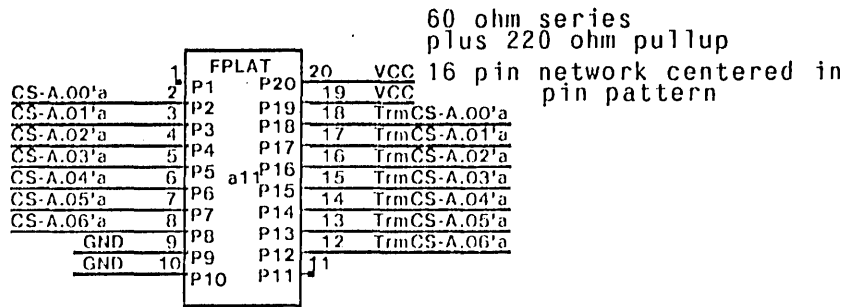
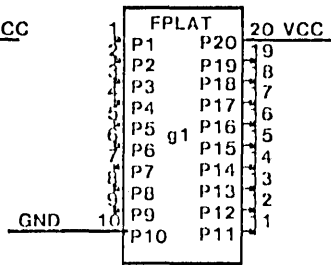
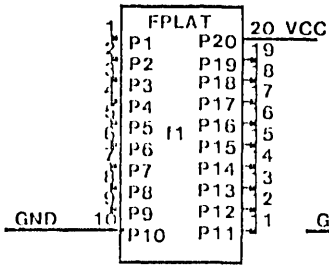
TrmCS-A.00'b	1	i2147
TrmCS-A.01'b	2	A0
TrmCS-A.02'b	3	A1
TrmCS-A.03'b	4	A2
TrmCS-A.04'b	5	A3
TrmCS-A.05'b	6	A4
TrmCS-A.06'b	17	A5
TrmCS-A.07'b	16	A6
TrmCS-A.08'b	15	A7
TrmCS-A.09'b	14	A8
TrmCS-A.10'b	13	A9
TrmCS-A.11b	12	A10
CSIn.15	11	A11
WE-CS-Low'b	8	DIN
WE'		WE'
CsChipSel'c	10	CS' b7



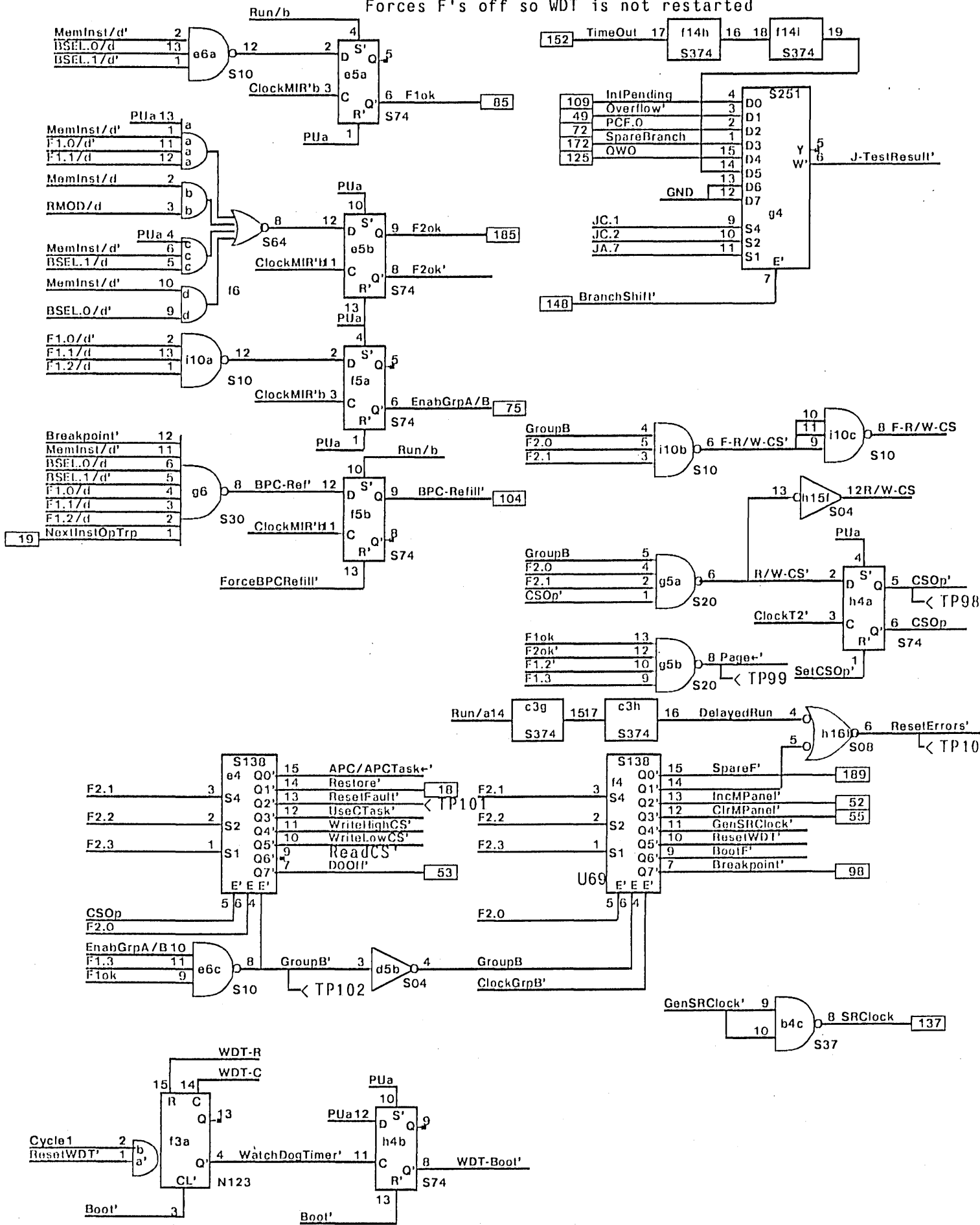


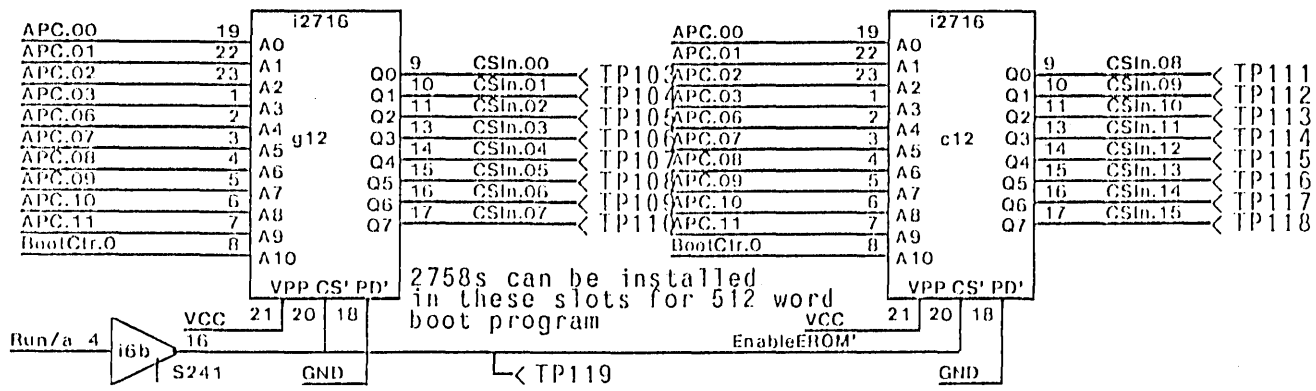
Disabled by test

Spare positions

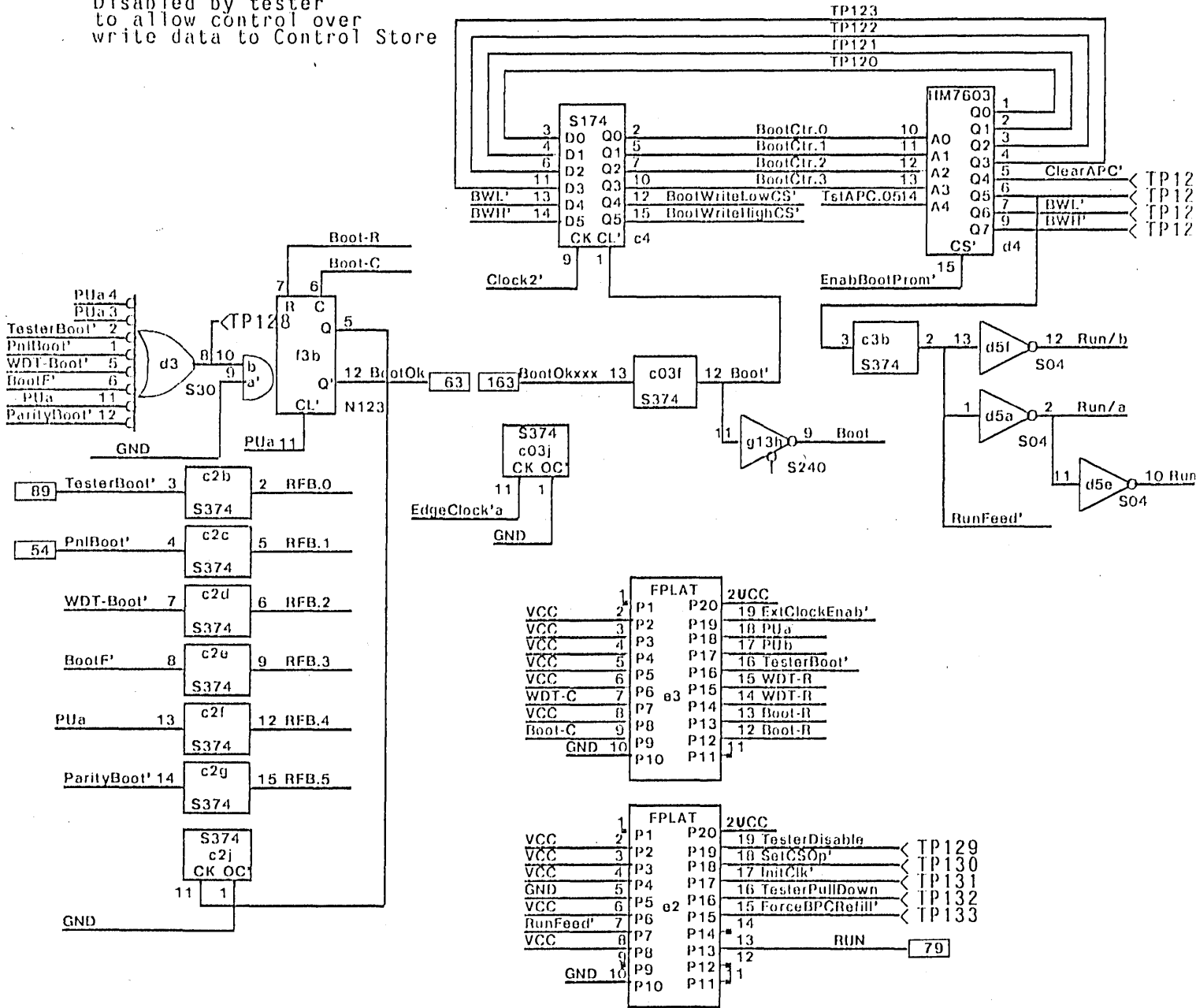


Forces F's off so WDT is not restarted

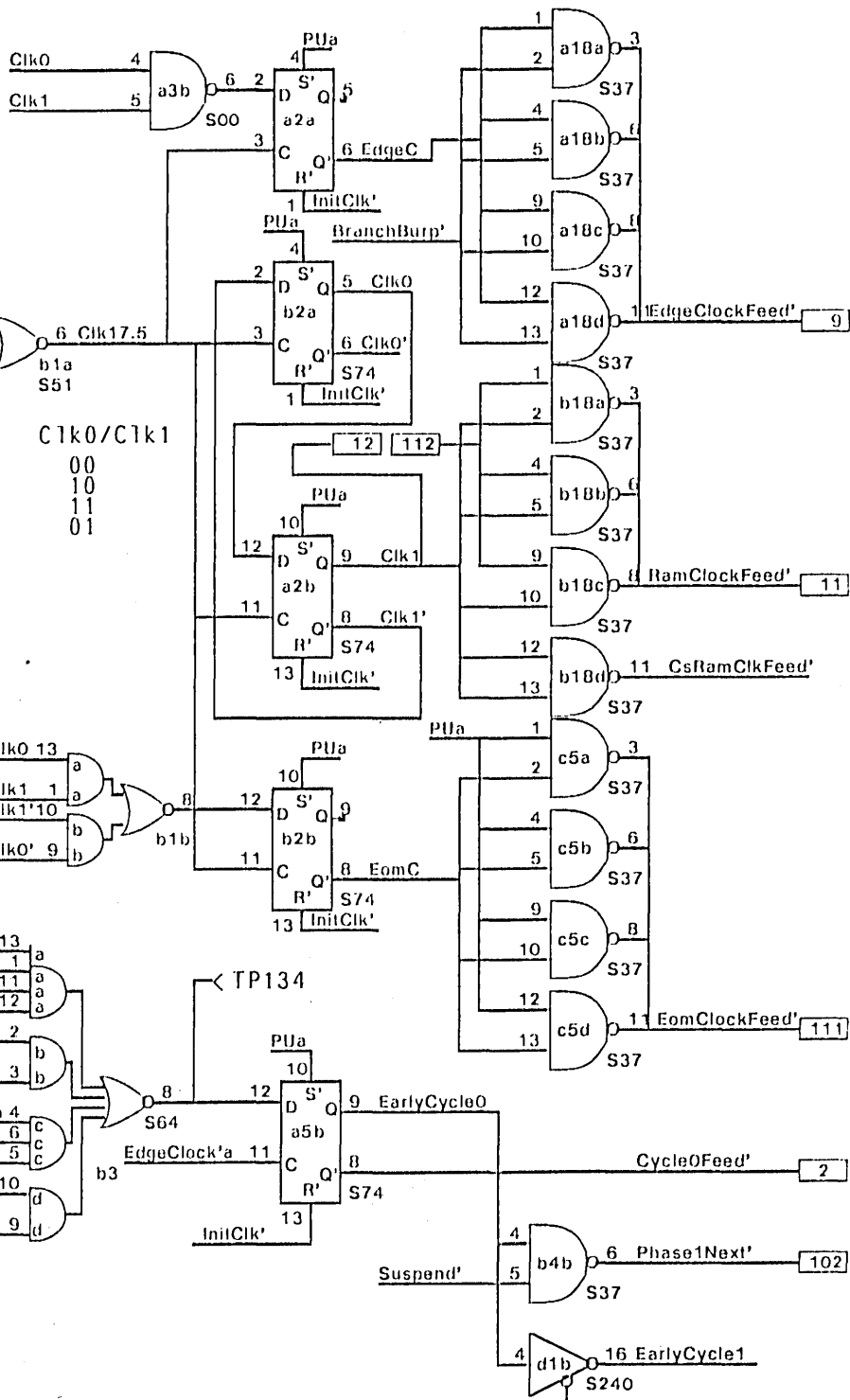
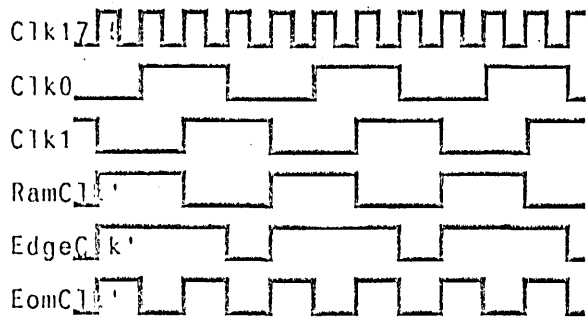
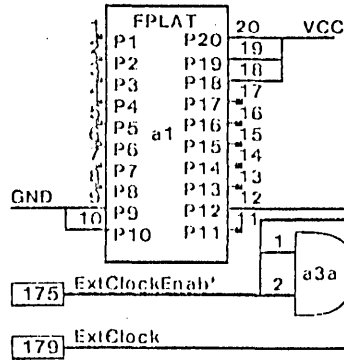




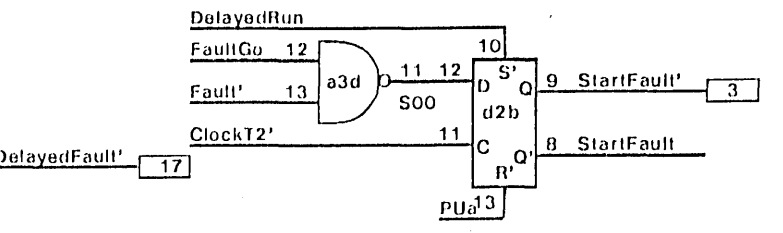
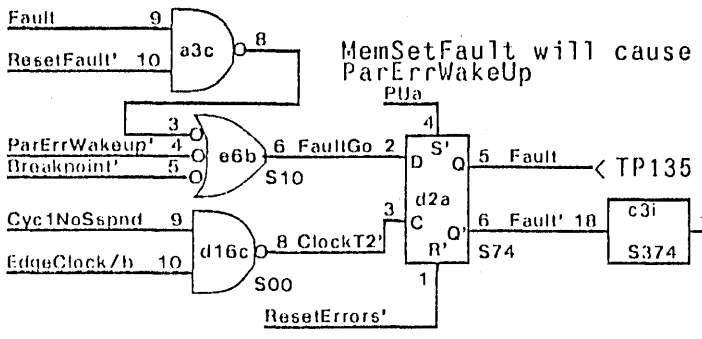
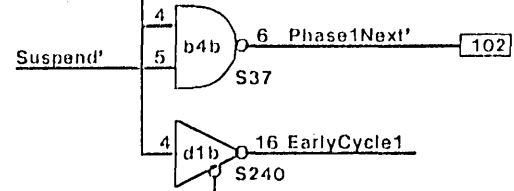
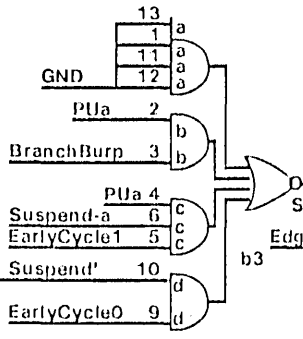
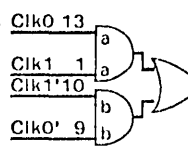
Disabled by tester to allow control over write data to Control Store

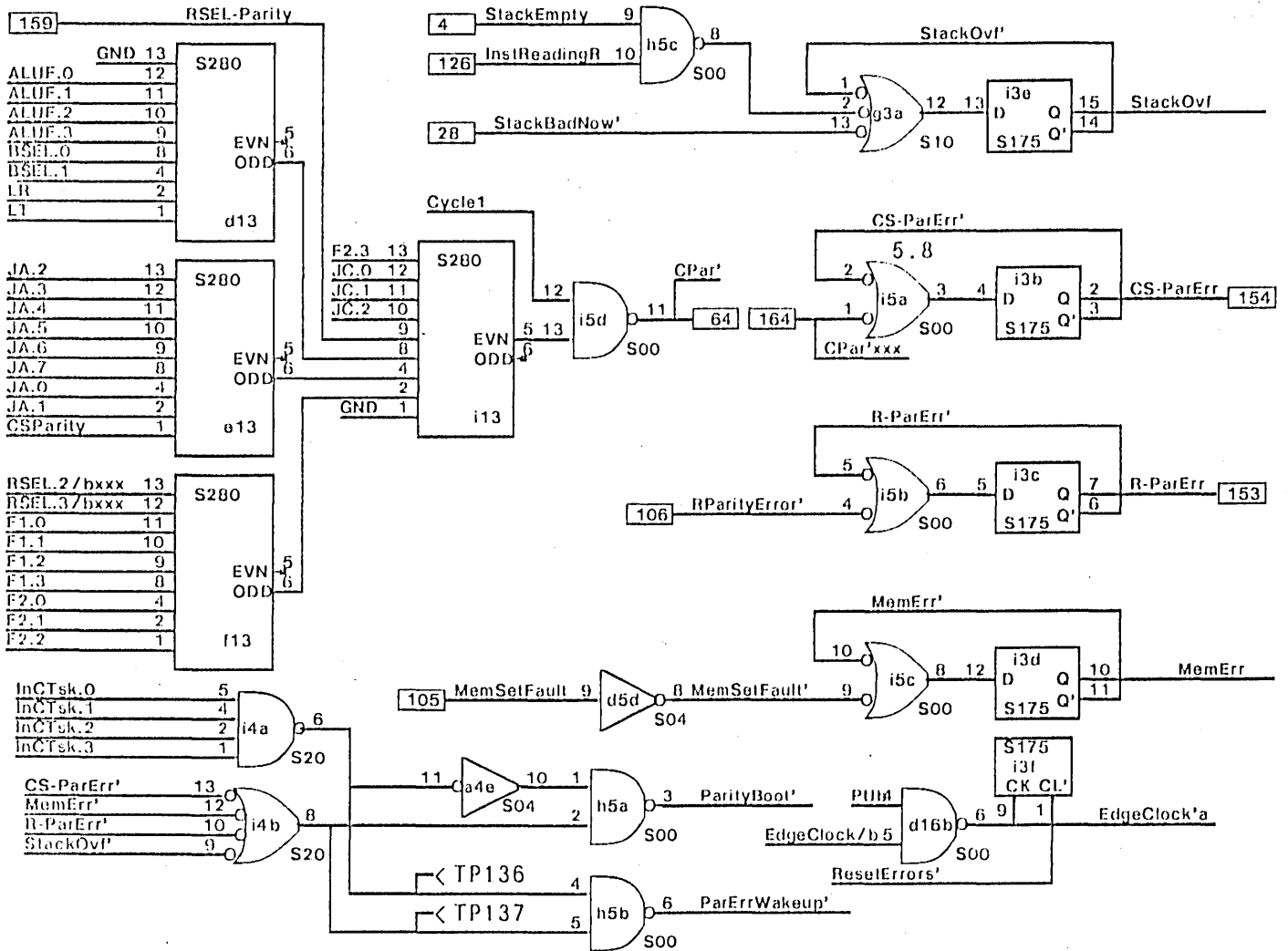
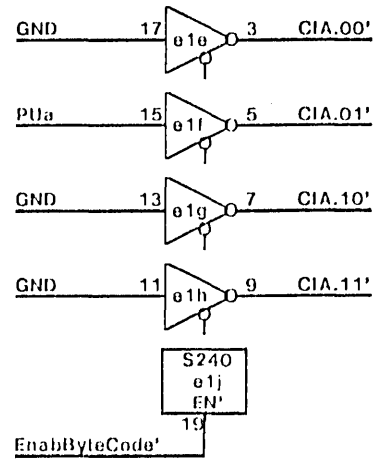
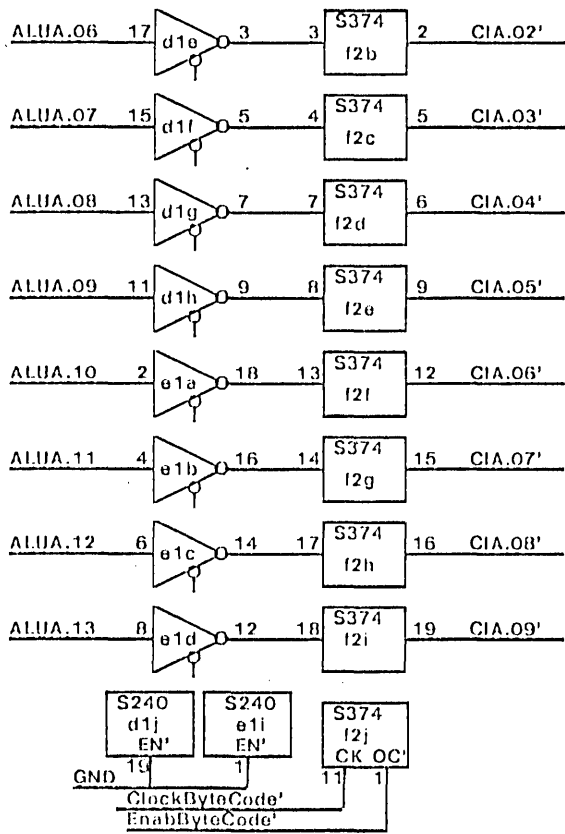


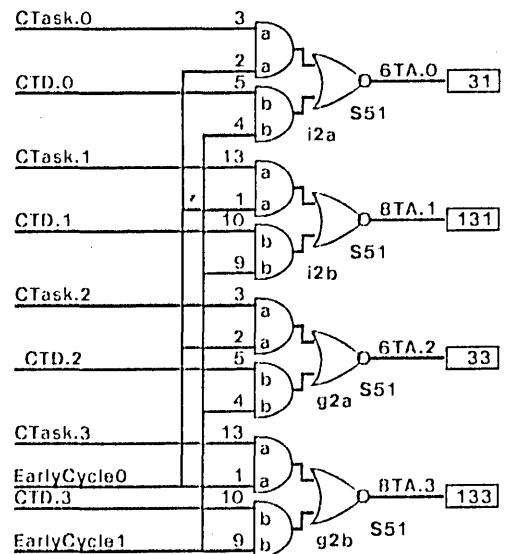
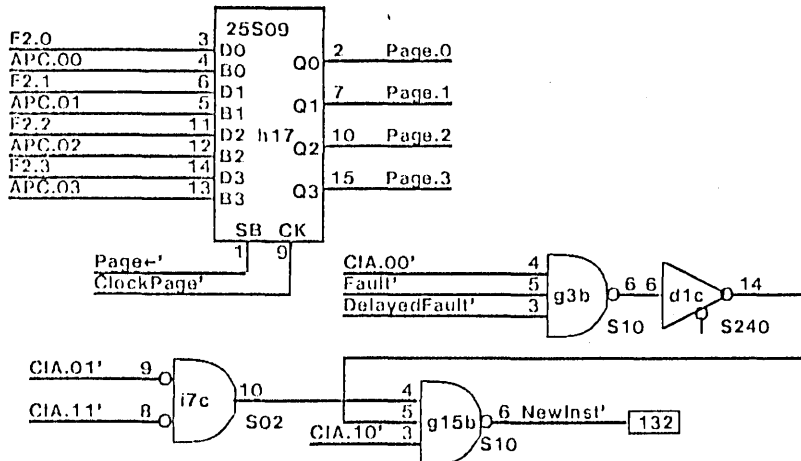
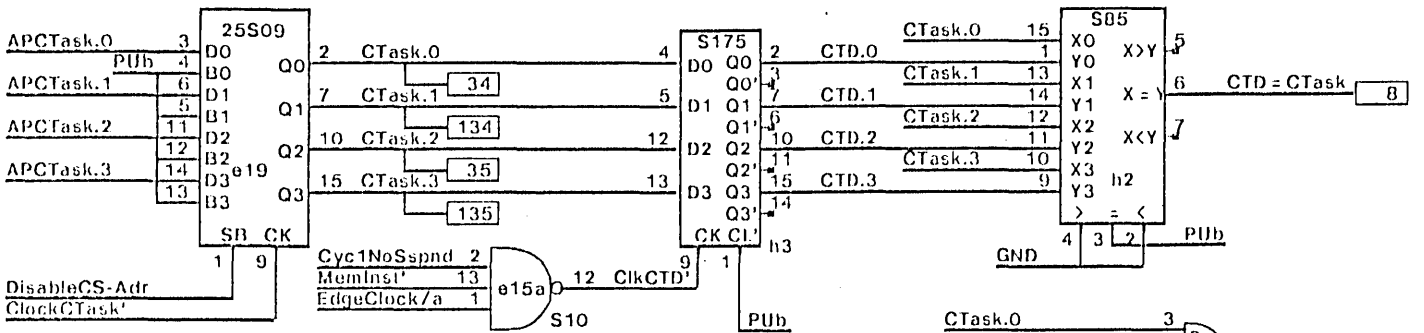
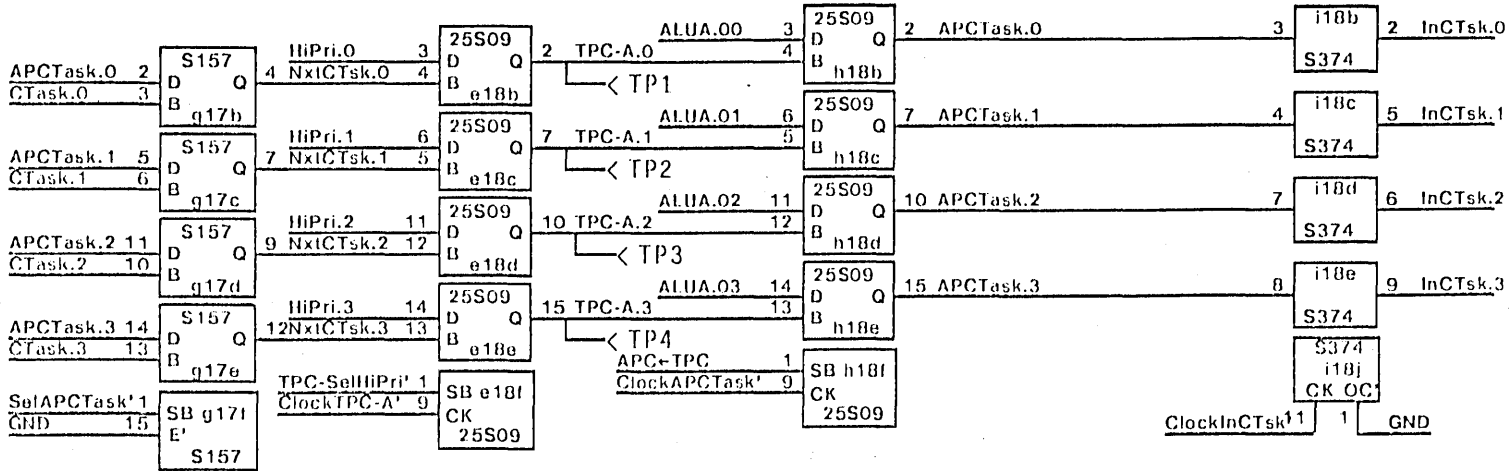
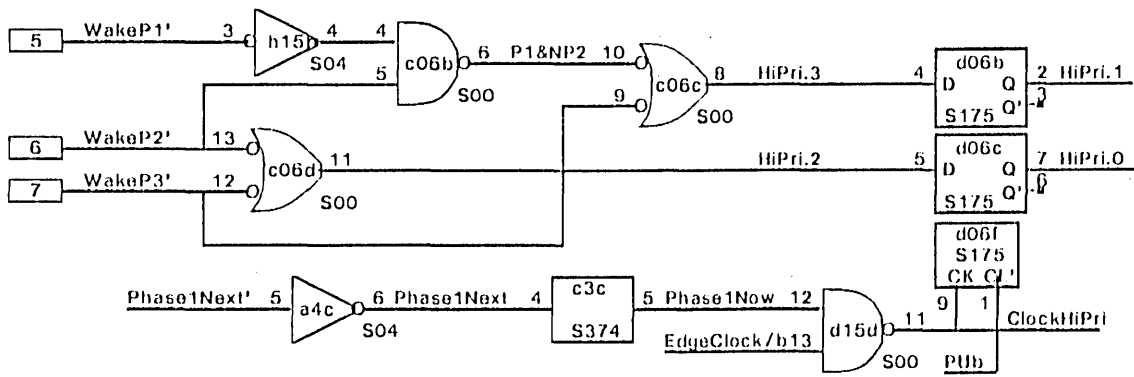
Xtal Oscillator



Clk0/Clk1
 00
 10
 11
 01







Rev E to Rev F 3/8/78 Brian Rosen

- 1) The Clock Drivers on page 12 were moved from c1/d1 to a18/b18 to eliminate waveform distortions due to reflections at the connector that caused false clocking on some boards. This necessitated moving the TPC-A multiplexer (page 1) from b18 to g17, and the Wake-up encoder S00 from a18 to c06. The wake-up lines now have long stubs on this board. The HiPri register was also moved up next to the S00 encoder (from e01 to d06).
- 2) The S30 at g6 that makes BPC-Rel' (page 10) had Breakpoint' added to it. This prevents the BPC-Refill trap from occurring when the successor of a breakpointed instruction points to an instruction which has NextInst or Nextop specified.
- 3) The trap location for Fault and BPC refill were reversed by changing the term on CS-A:11 from BPC-Refill' to StartFault' (S20 at a6 on page 9). Faults trap to 1, BPC refill traps to 0. This forces a nextinst/nextop which both BPC refills and Faults to hit the fault handler rather than the BCP handler.
- 4) The EPROM sockets were changed to allow 2716s or 2750s to be plugged in. This removes all dependency on the +12/-5 supplies for booting, and allows a 1k boot program. This change also affected the bit tested to determine end of boot load (from APC.00 to APC.05, thus affecting TstAPC.00 on page 3 and page 11)
- 5) A new Clock was added for the EOM board (ROS printer). This clock, EomClock, is a 35ns (nominal) squarewave, with a clock driver. See page 12.
- 6) Final testability changes were made, they include: a) A new signal, TesterDisable which is an independent pullup resistor on a new plat at e2 (page 11). This signal enables the S241 on page 3 which allows tester control of TstAPC.05, Enable BootProm, EnabCIA. b) another new signal, also an independent pullup (page 11) which allows tester to force CSOp to set. c) an S51 at b1 now lets the tester turn off the oscillator with a new signal-ExtClockEnab'. This signal is pulled up on the e3 plat instead of ExtClock'. c) the clock generator flip flops can be initialized by the InitClk' signal, which is pulled up on the e2 plat.
- 7) a minor improvement was achieved by eliminating the S32 at d6. Only one section was used (SRData, page 10) and an unused S32 section was available in the e16 S32. d6 is now empty

Rev F to Rev G 4/17/78 Brian Rosen

- 1) The chip enables for the TPC rams (control sections on pages 1 and 2) were run through an S241 controlled by DisableTester to allow tester control of APC inputs
- 2) The Run/a signal was run through another tester controlled S241 gate to allow tester control of the EPROMs (page 11)
- 3) The select input of the data in mux for bits 32:35 of the control store (page 8) was modified to run through another S241 gate to allow tester control of the data input to these 4 RAMs.
- 4) A new pull down resistor was added to the e2 plat (page 11) creating the signal TesterPullDown. This is the control input to the tester S241 (page 3)
- 5) The signal ChipSelect' (an input to all 2147 RAM chips, pages 4:8) was broken up into 3 separate nets, each fed from an S410 gate at i6 (page 3, nets CsChipSel'a, CsChipSel'b, and CsChipSel'c)
- 6) An adder, S283 was added between CIA and the TPC ram inputs (page 1) to make the return address CIA + 1 (carries propagate through 4 bits only). New chip is at c1.
- 7) The clock term for CTD (page 13) needed to have MemInst' as an input. Added a new gate (e15a) to make this term.

Rev G to Rev H 9/8/78 Brian Rosen

- 1) The Abort' term on ClockTPC-A' (g15.11) page 2 is erroneous, it was removed.
- 2) The Cycle1 term on RunningT2 came very late for some qualifier terms. It was changed to Cycle0Feed' thus cutting two gate delays
- 3) The Complement of the actual BranchBurp signal is needed for new clock driver scheme (see note 4 below). Added an inverter to BranchBurp using a4.3 and a4.4 creating BranchBurp'. The signal from b6.3 (page 9) had its name changed to BBurp'
- 4) Clock Drivers (page 12) were changed from S32s to S37s. This changed all inputs on a18, b18 and c5.
- 5) Cycle0Feed' is too late. The S37 that created this signal (page 12) was deleted. Cycle0Feed' now come from a5.8 this affected the name of the signal at b3.5 (was EarlyCycle1, now Cycle0Feed') This EarlyCycle0 is also used on a10 (page 9) and i2/g2 (page 13). The next revision (I) will remove some of these loads For now, they are all Cycle0Feed'

Rev H to Rev I - 11/18/78, C. Thacker

- 1) The register ByteCode is added (f2,d1,e1, pg13). This register holds ALUA[6:13]' for one cycle following NextInst, so that the bytecode can be written into TPC by the subsequent RETURN. This allows task switches between bytecodes.
- 2) The signal SRData (buffered H2.15) has been deleted. This requires a backplane change (pg 4,5,10).
- 3) The branch logic on pg 10 is changed to add IntPending (in place of Disp999), QWO, and a SpareBranch.
- 4) The signal NxtInNoTsk' is generated in c6a (pg2). This signal is true if a task switch will NOT occur in the RETURN following a NextInst. This signal determines the source of APC data during NextInst.
- 5) The signal NxtInstRTN' is generated in i7c (pg2). This signal will be asserted by all RETURNS following NextInsts, and will cause ByteCode + 1 rather than CIA + 1 to be written into TPC.
- 6) The function decoder on pg 10 is changed to bring out SpareF', and rename DispCnt' and DispClr' to be IncMPanel' and ClrMPanel'
- 7) The generation of RUN (pg11) is different. The feed signal from d4.6 is latched, RUN is generated on platform e2. (NOTE: e2 is changed to 18pins). PwrBoot' is generated in e16d.
- 8) CSOP (pg10) is clocked by clockT2' (used to be called ClkFault', pg 12).
- 9) EarlyCycle1 (pg 12) was added to reduce loading on Cycle0Feed'.
- 10) Clk1 is brought to the backplane (E12 -> E112) so that a delay can be inserted to reduce the width of RamClock.
- 11) a5.13 (pg 12) is connected to InitClk' rather than to PUa.
- 12) Stack overflow logic is added on pg 13.
- 13) NewInst (used to be an F) is generated on pg14.
- 14) Added TimeOut branch condition (pg10) and brought R-ParErr and CS-ParErr to the edge connector (pg 13).

Changes to revision Ga (2/18/79 - CT)

- 1) Changed all plats to 20 pins on logic diagrams to cause ROUTE to do no trace cuts.
- 2) Added synchronizer on TimeOut (pg 10)
- 3) Changed DOOff' to E53, ClrMPanel' to E55 (pg 10).
- 4) Added spare IC's in positions f1, g1, h1, i1, h6.

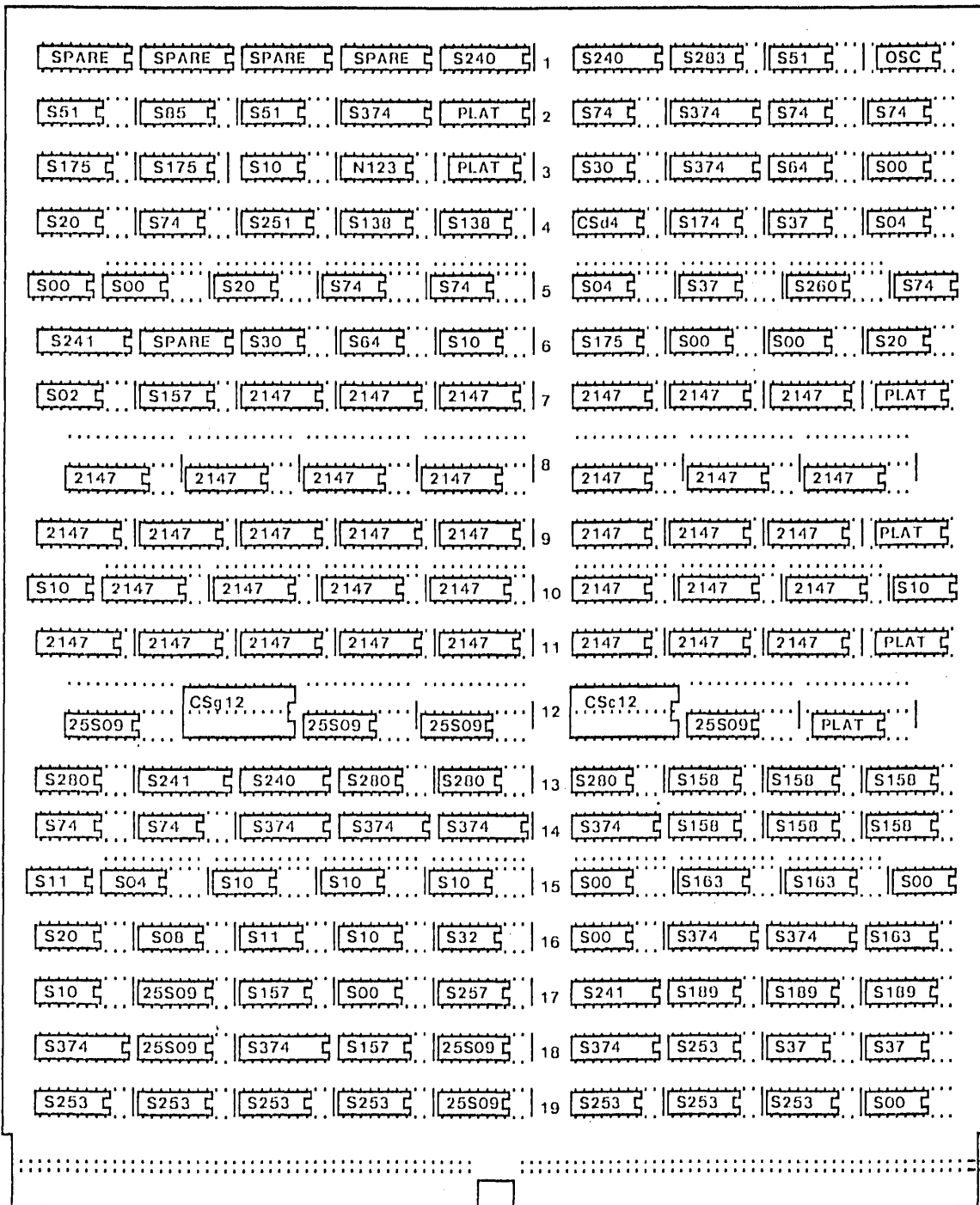
Rev Ga to rev Gb (3/8/79 - CT)

- 1) Added g3b, d1c on pg 14. This change keeps NewInst from occurring when the first microinstruction of a bytecode is aborted.

Rev Gb to rev Gc (7/17/80 - CT) Eliminated signal PwrBoot', changed RFB register clocking (pg 11).

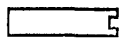
XEROX EOD	Project D0	Control Board Change History	File D0csChanges.sit	Designer Rosen	Rev Gc	Date 7/18/80	Page 15
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I H G F E D C B A



101-200
1-100

20pins: A



16pins: B



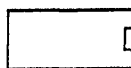
14pins: C



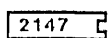
22pins: D



24 pins: E

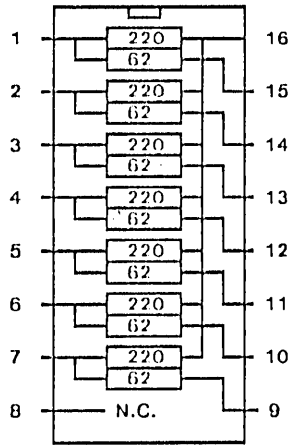


18 pins: F



Note: The short vertical lines indicate filter capacitor locations. (123 Total)

Plats in locations: a7, a9, a11, a12



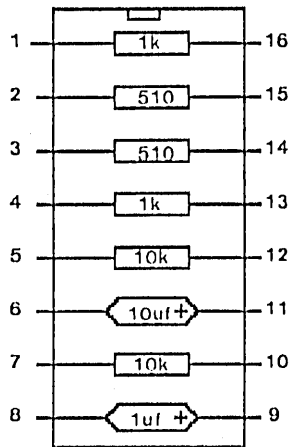
all resistors 1/8 watt

Note: Bourns has made a custom network for this platform.

16 pin platforms plugged into the middle
of the 20 pin pattern

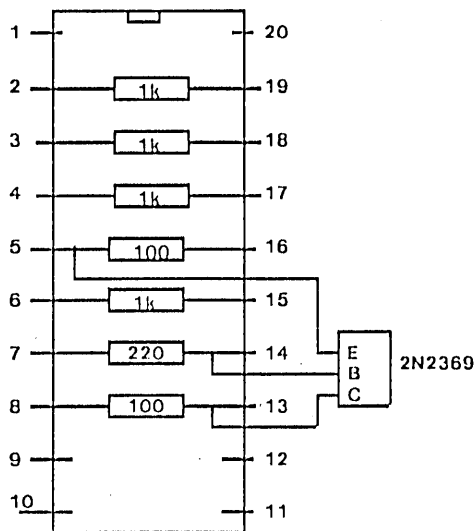
Pin 1 of plat goes in pin 2 of pattern

Plat in location e3



all resistors 1/4 watt
all capacitors Tantalum

Plat in location e2



all resistors 1/4 watt