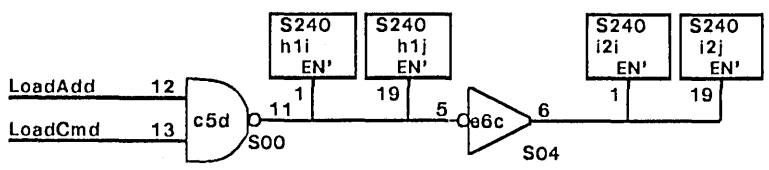
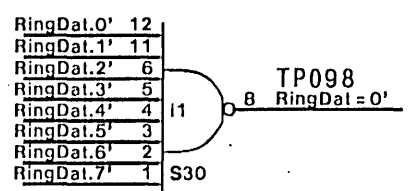
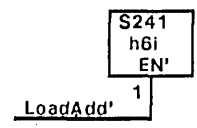
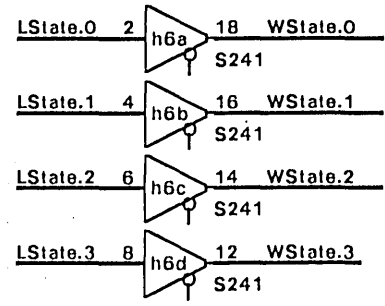
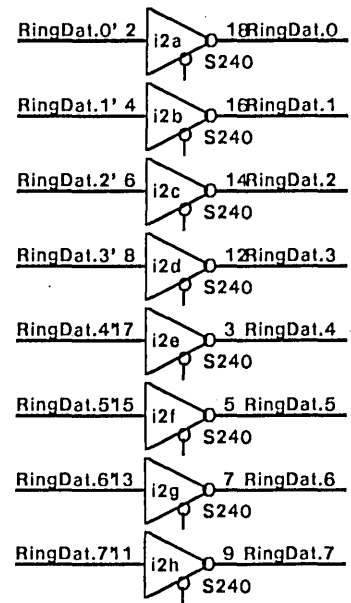
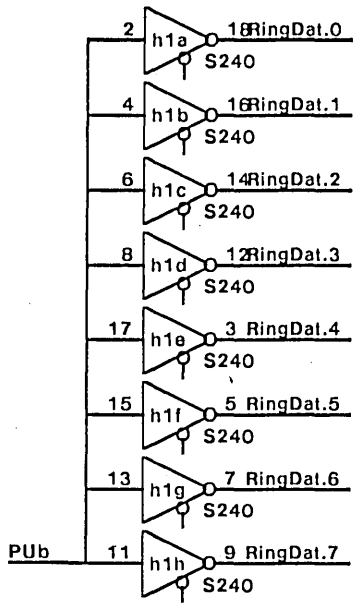
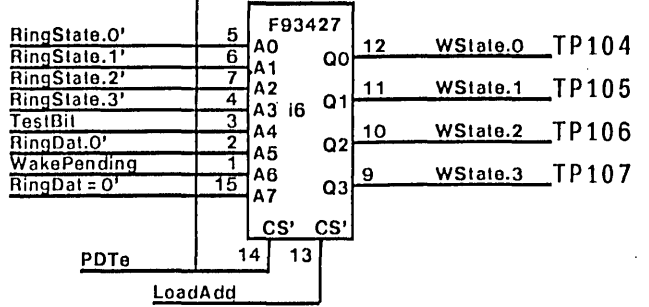
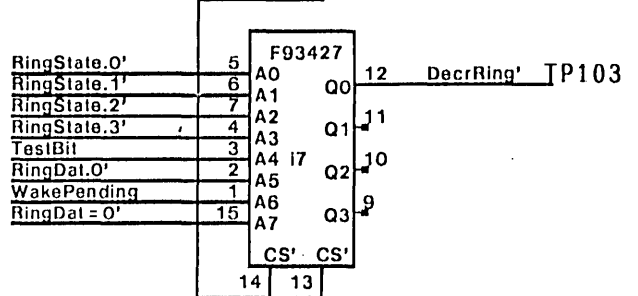
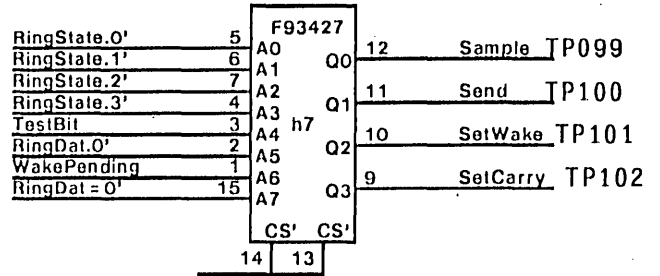
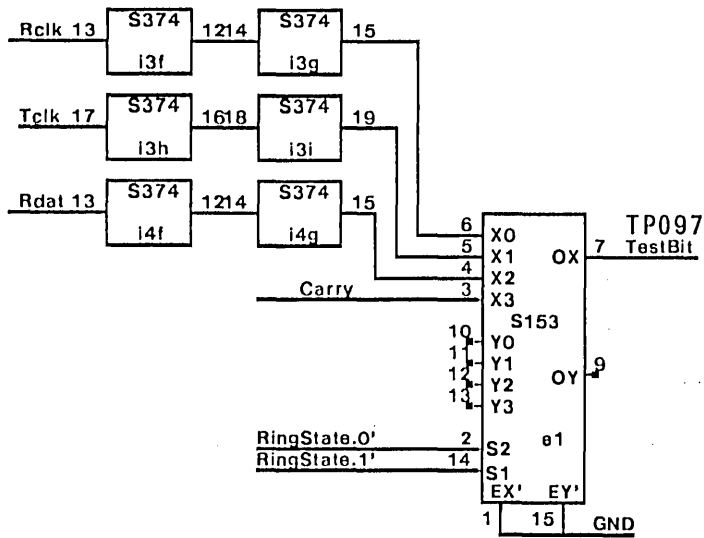
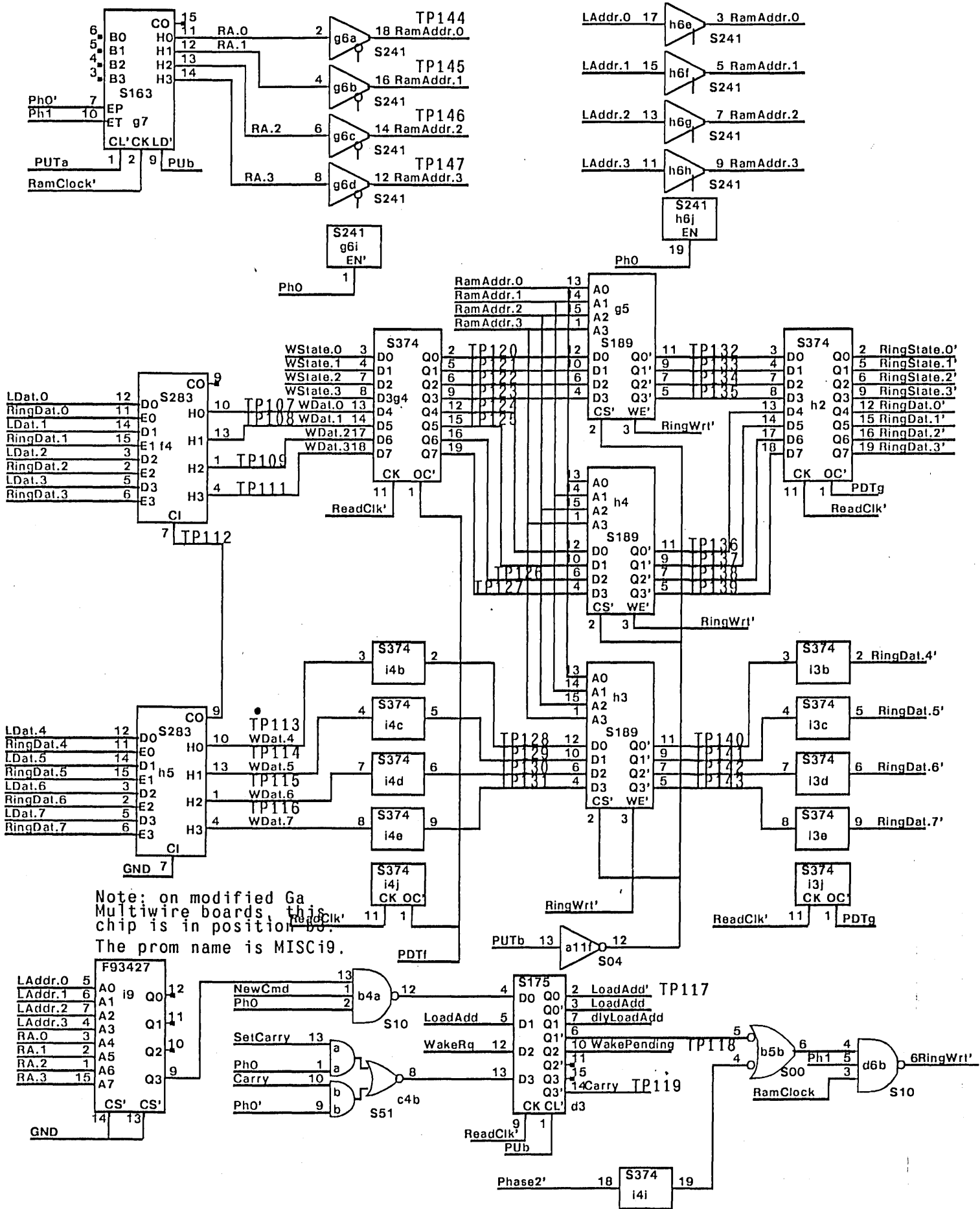
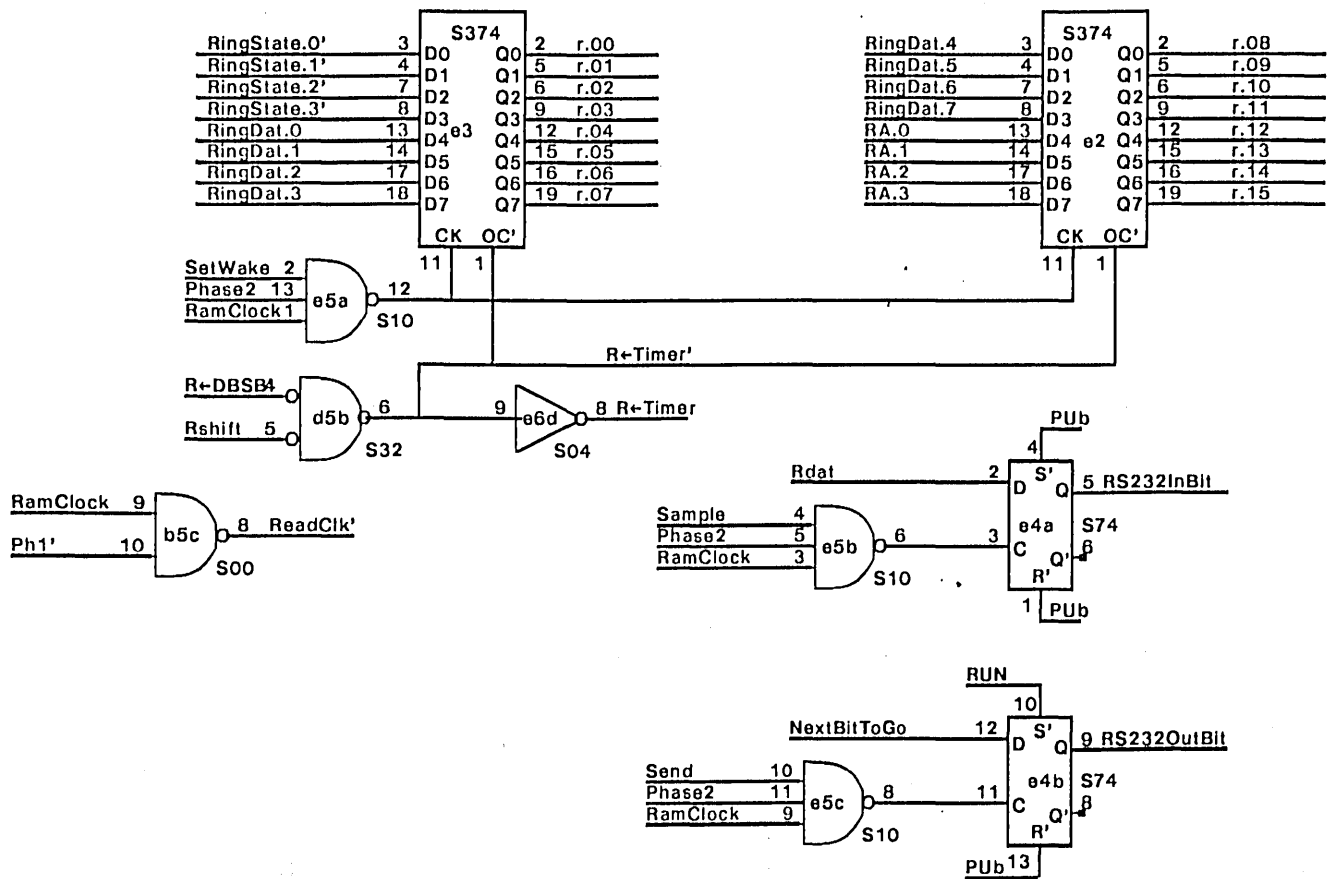


Possible that branch during R+Timer must be disallowed due to BranchBurp

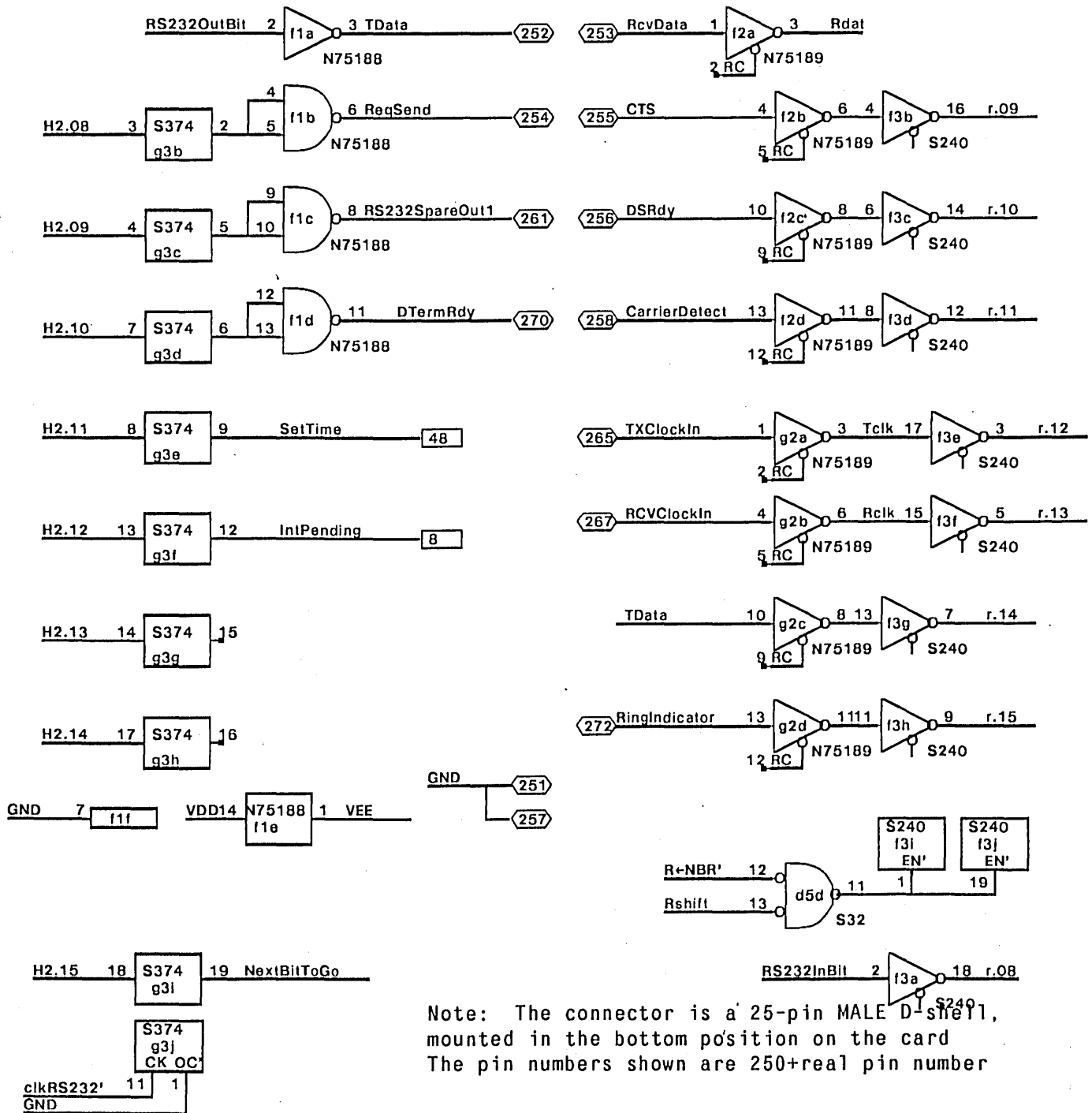




Note: on modified Ga  
Multiwire boards, this  
chip is in position B9.  
The prom name is MISCi9.

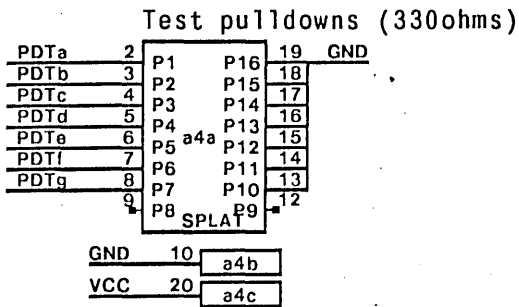
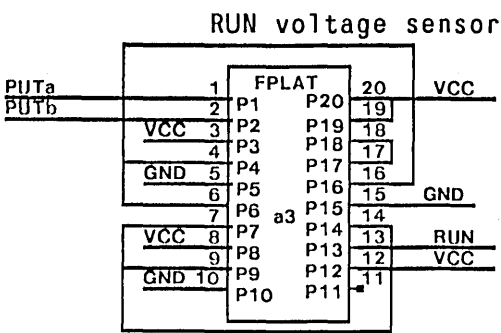


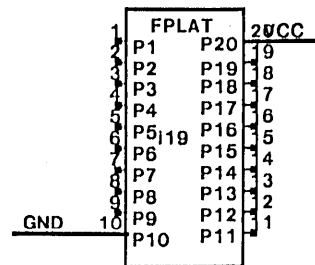
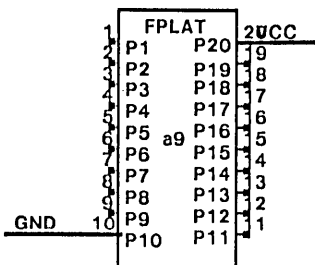
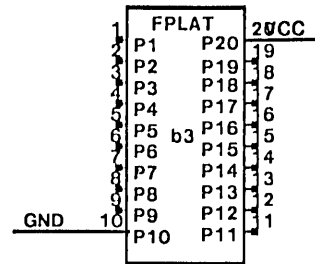
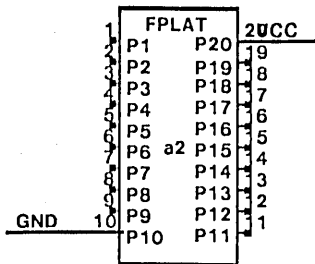
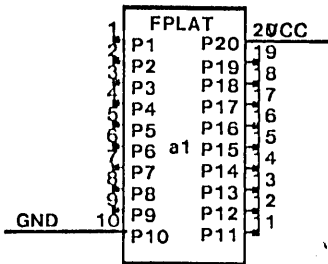
Note: Timers are device 14  
It is known that task 15 never competes for wakeups.



Note: The connector is a 25-pin MALE D-shell, mounted in the bottom position on the card. The pin numbers shown are 250+real pin number.

Note for PC Layout: PUTx and PDTx all have independent test points.







- 1) Added signal GateALUParity and inverter to receive it (Pg 1).
- 2) Deleted signal MC2EnableRP' (Pg 1).

**Changes for rev F to rev G (10/17/78 - C. Thacker)**

- 1) Reduced number of outbound RS232 lines to 4. Looped RS232 data back on R.14. Added SetTime as bit 11 in the output register (goes to E4B). Added IntPending as bit 10 of the register. All changes on pg 15.
- 2) Terminated PI.O - PI.4. Used R bus drivers PI.5-7 for voltage monitors.
- 3) Added a11e, b6d, b6c, e6f on pg 3 to cause IntPending to dispatch to Opcode0 on interrupt.
- 4) Added test pullups and pulldowns.
- 5) Added +5 monitor at a3 (pg 15) to control RUN.

**Changes for rev G to rev H (1/4/79 - C. Thacker)**

- 1) Brought signal InstReadingR to E018 (pg 2).
- 2) h17 pin 7 was NewInst', is now SpareF2, connected to E105
- 3) NewInst' is now connected to E005 rather than to h17.7.  
Note: Control boards with revision <I must have E005 jumpered to E105 on the backplane.
- 4) Removed the time-to-task counter (a9) and freed inverter a12d (pg8).
- 5) Terminated PD.O-7 with splat (R-pack) at b2
- 6) Added InterfacePower signal (short-circuit protected +12V) to Printer Interface connector

**Changes for rev H to rev I (1/18/79 - C.T)**

- 1) Changed layout - g1 is S241, not 75188
- 2) Modified platforms b1, a3.
- 3) (pg 1) b17.1 is GND, not PDTf.
- 4) (pg 10) b1.9 is VCC, not GND
- 5) (pg 10) Added S241 driver for PD.O-PD.7. (note - early etch boards will NOT have this change)
- 6) (pg 12) i6.14 is PDTa, not LoadAdd
- 7) (pg 13) i4.1 is PDTf, not GND

**Changes for rev I to rev J (1/31/79 - CT)**

- 1) Changed E18 from InstReadingR to InstReadingStack (pg2). Corrects a bug in overflow checking

Note: Revision J = Revision Ga

**Changes for revision Ga to revision Gb (10/14/79 by CT). Fixes interval timer inaccuracy.**

Note: This change comes in two flavors: Revision Ga multiwire boards have 2 extra IC's mounted in spare positions b3 (93427) and b4 (74S10). In the Multiwire Gb version, the S10 is in position b4, but the 93427 replaces the S85 in position i9. The logic diagrams show the revision Gb multiwire version of the change. To modify a revision Ga multiwire board, proceed as follows:

In the steps below, pin numbers are those of the chips, not those of the 20 pin sockets used to hold the chips. Chip b4 is mounted with pin 7 in pin 10 of the 20 pin pattern, b3 is mounted with pin 8 in pin 10 of the 20 pin pattern.

All wiring is to be done on the back (non-component) side of the board.

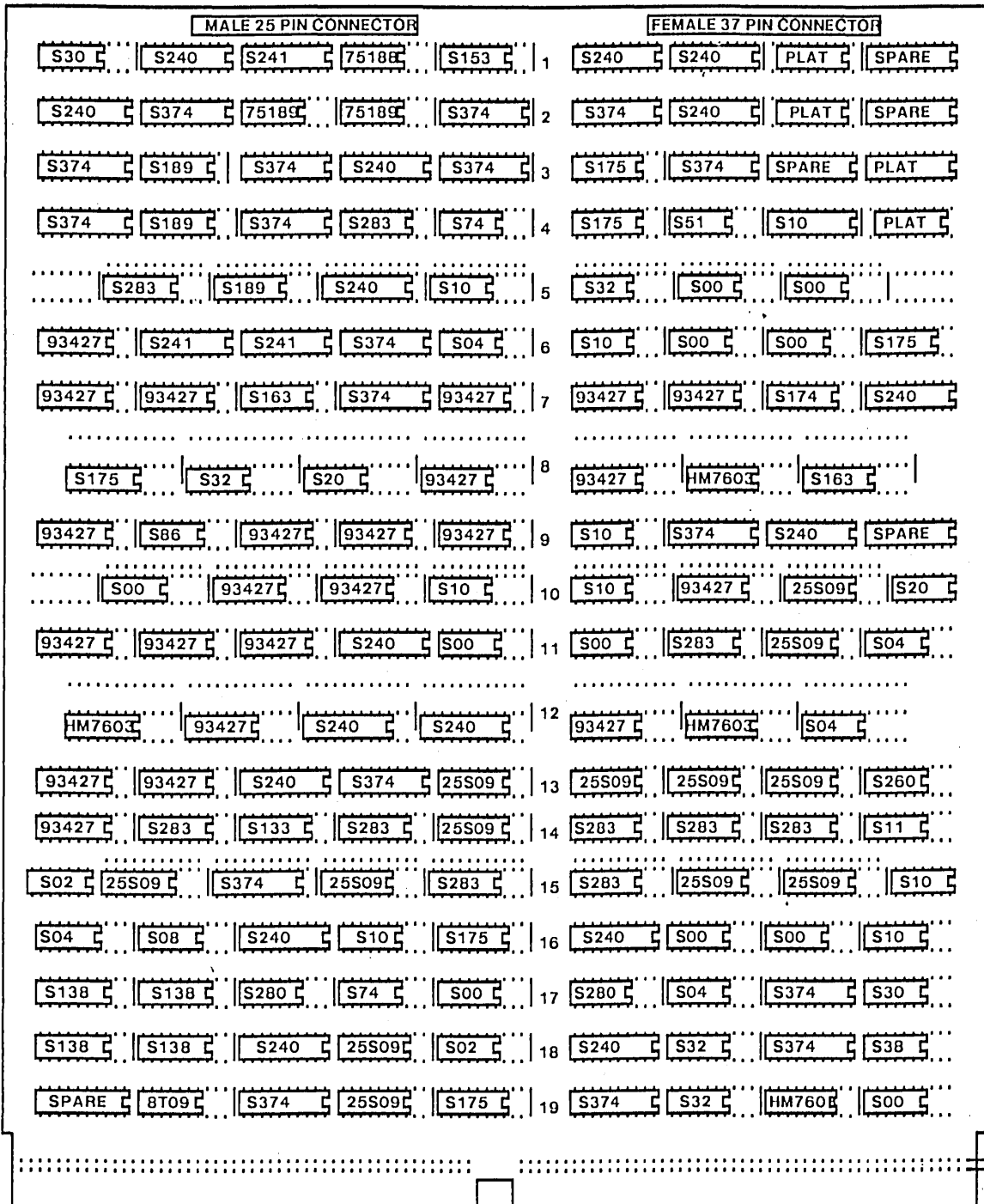
- 1) Add an S10 in position b4 and wire b4.14 to pin 20 of the pattern (Vcc).
- 2) Add a 93427 (programmed) in position b3, and wire b3.16 to pin 20 of the pattern (Vcc).
- 3) Lift pins b5.1, b5.2, and b5.3.
- 4) Remove chip i9 and jumper i9.6 to i9.8
- 5) Add b5.1 to b4.1
- 6) add b5.2 to b4.2
- 7) add b5.3 to b4.12
- 8) add b3.14 to b3.13 to b3.8
- 9) add b3.5 to f6.12
- 10) add b3.6 to f6.15
- 11) add b3.7 to f6.16
- 12) add b3.4 to f6.19
- 13) add b3.3 to e2.13
- 14) add b3.2 to e2.14
- 15) add b3.1 to e2.17
- 16) add b3.15 to e2.18

**Changes for revision Gb to Gc (7/17/80 - CPT)**

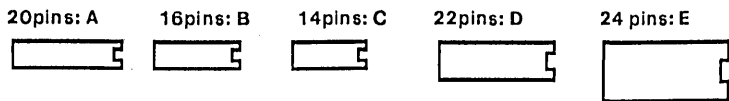
- 1) e18.5 + gnd (pg. 2) This causes memory reference instructions to interlock when referencing base registers

- 17) add b3.9 to b4.13

XEROX PARC/C.S.	Project DO	Title DO MISC board Changes	File DOMISCChanges	Designer CPT	Rev Gc	Date 7/17/80
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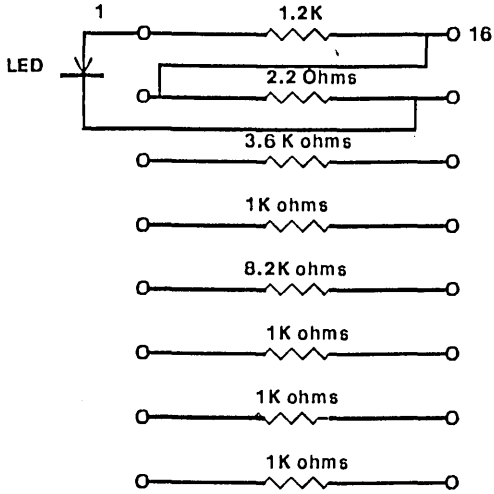


101-200  
1-100



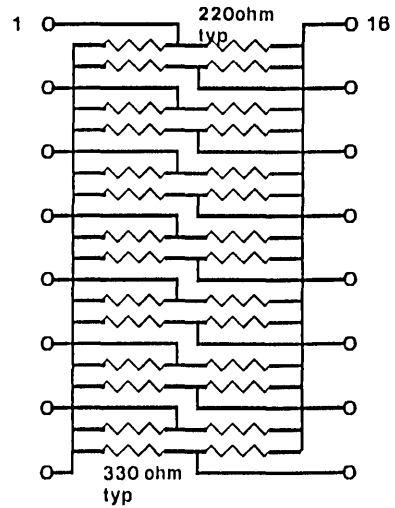
Note: The short vertical lines indicate filter capacitor locations.

SPLAT at b1



(Page 10)

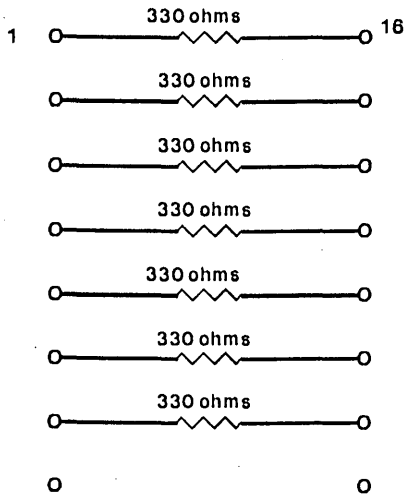
SPLAT b2,



Beckman P/N 898-5-R220/330  
Xerox P/N (?) 703W30491

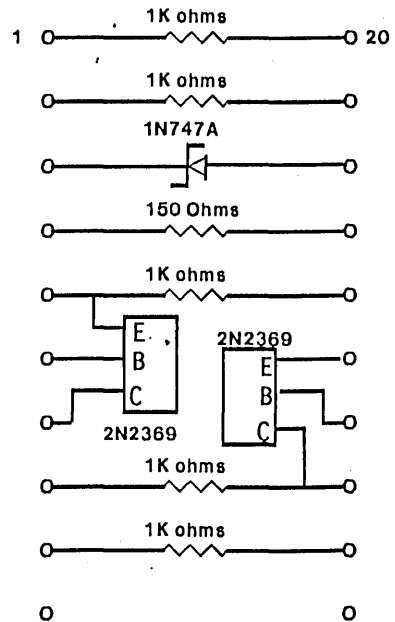
(Page 10)

SPLAT at a4



(Page 15)

FPLAT a3



(Page 15)