Xylogics®

MODEL 450

Users' Manual

Xylogics®

MODEL 450

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SECTION 1 SPECIFICATIONS

1.0 GENERAL

The Xylogics Model 450 Disk Controller can interface up to 4 SMD interface disk drives to IEEE P796 Multibus systems. Data transfers are implemented via DMA, which allows maximum throughput. Control is implemented via I/O Parameter Blocks (IOPBs) and byte I/O registers. The 450 circuitry is comprised of two sequencers and a microprocessor for control.

1.1 USING THIS MANUAL

Two program reference cards are provided in the front of this manual. The margins in this manual are large enabling you to jot down notes in appropriate places. If you will be installing the 450 read Section 3. If you wish to program it, read sections 2.1 and 2.6. This will give a good overview of the programming aspect. Section 2.3 describes the registers, section 2.4 describes the IOPB, and section 2.5 describes the commands.

1.1.1 Abbreviations

In many places in this manual several letters are used as mnemonics to encode various verbose functions. The following table can be utilized to decode these codes into useful information.

CDC	Control Data Corporation
CMD	Cartridge Module Drive
CPU	Central processor Unit and/or computer
CSR	Control and Status Register
DMA	Direct Memory Access
ECC	Error Correction Code
FIFO	First In First Out buffer
H	Notation for numerical values being in Hex.
(H)	A high level active signal
IOPB	Input / Output Parameter Block
I/O	Input / Output
(L)	A low level active signal
LED	Light Emitting Diode
LMD	Lark Module Drive
MB	Mega Bytes
PCB	Printed Circuit Board
RAM	Random Access Memory
SMD	Storage Module Drive

1.2 DESIGN RELIABILITY

XYLOGICS' design minimizes the likelihood (and the expense) of failure by the following:

- low parts-count, through microprogramming;
- low-power Schottky Integrated Circuits;
- low-stress design on all components;
- all components burned-in;
- one card, resident in backplane or expansion chassis;
- controller is power-cycled under thermal stress during test.

1.3 PHYSICAL

Packaging -- The 450 is completely resident on one printed circuit board that plugs into any 16-, 20- or 24-bit Intel Multibus or IEEE P796 card cage.

Dimensions -- 12-inch length x 6.75-inch height (30.48 cm X 17.15 cm); the 450 is identical in form-factor to the standard Intel Multibus, and IEEE P796 Printed Circuit Board (PCB).

Shipping Weight -- 3 pounds (1.4 kg).

1.4 ENVIRONMENTAL

The Model 450 Disk Controller environmental requirements are similar to the Intel 86/12 SBC or equivalent Multibus processors. (Typically 0-55°C and up to 90% relative humidity without condensation.) The 450 requires sufficient air circulation for cooling.

1.5 ELECTRICAL

Power -- The 450 requires 6.8 Amperes at +5 Volts DC and 1.0 Ampere at -5 Volts DC.

Tolerance -- Voltages must be within plus or minus five percent. (4.75 to 5.25).

Grounding -- Common earth ground must be established between the disk drives and the CPU chassis, backplane, and expansion cabinets.

1.6 SYSTEM-RELATED SPECIFICATIONS

Transfer Control -- Direct Memory Access (DMA).

DMA Throttle Control -- Programmable throttle value supports any Multibus throughput speed.

Interrupt Priority -- INT5/ standard, others jumper selectable.

Interrupts -- Non-Bus-Vectored.

Control Technique -- Channel Driven Control -- Programmable microprocessor.

Addressing Capability -- 16, 20, and 24 bit.

Controller I/O Parameter Block (IOPB) Length -- 24 bytes.

Controller Registers -- Six 8-bit I/O Registers, byte addressable only.

I/O Addressing Capability -- The 450 decodes byte addresses for its on-board registers. It will respond to either 8 or 16 bit I/O addresses.

Data Transfer Modes -- Data is transferred in bytes or words

Data Buffering -- On-board FIFO memory accomodates 2K bytes in word mode and 1K bytes in byte mode. Optional buffer accomodates 8K bytes.

Data Transfer Limit -- Data transfer length, from 1 to 65,535 sectors

1.6 SYSTEM RELATED SPECIFICATIONS (continued)

Software Support -- Standard software driver supplied for use in CP/M-80*, UNIX**, or RMX-86*** based systems (source included).

Error Detection and Correction -- A 32-bit ECC is used by the 450. Automatic detection and correction is under software control.

Status LEDs -- two status LEDs are implemented. One LED indicates successful completion of on-board diagnostics. The second LED indicates that the controller is active.

DMA Data Transfer Rate -- The 450 adds less than 500 ns overhead on each word transferred. Assuming 500 ns memory, total transfer time is 1000 ns for a DMA rate of 2.0 MB/sec. With 300 ns memory the 450 can DMA at 2.5 MB/sec.

1.7 DISK DRIVE RELATED SPECIFICATIONS

Disk Interface -- Storage Module Drive (SMD) Interface compatible and SMD+ (up to 1.9MB/sec.)

Maximum Disk Capacity -- More than 2.4 Gigabytes of on-line storage (drive limitation).

Number of Disk Drives -- The Model 450 supports up to four disk drives, including any mix of capacities.

Disk Sector Format -- The 450 sector format includes a header field separated from a data field by a splice area.

Header Format -- Header contains sector, head, cylinder address, drive type and header ECC. Headers are written only once during formatting of the media.

Data Verification -- Built-in 32-bit ECC are each on the header and data portions of the sector. The ECC detects and corrects error bursts up to 11 bits long, to assure data integrity.

Implied Seek Capability -- Data transfer instructions contain an implied-seek command. Data transfers cross sector, head, and cylinder boundaries as required (spiral read/write).

Overlapped Seek Capability -- When requests for more than one drive are in chained IOPBs, implicit overlapped seeking may be initiated by the controller.

Bit Cell Time -- 55 nanoseconds, minimum.

Disk Data Transfer Rate -- Continuous transfers at disk speeds of 1.9 megabytes per second.

Cabling -- Standard SMD flat cabling.

Dual Port -- Dual port drives are supported.

Defective Sectors -- Defective sectors may be slipped to spare sectors on each track.

* CP/M - Trademark of Digital Research
** UNIX - Trademark of Western Electric
*** RMX-86 - Trademark of Intel Corporation

1.8 PROGRAMMABLE FEATURES

- Software Controlled 16- or 20/24-bit Address Bus Support
- Jumper Selectable 20- or 24-bit Extended Address Bus Support
- Software Controlled 8- or 16-bit Data Transfers
- Software Controlled Interrupt or Software Polled Operation
- Software Programmable DMA Throttle
- Software Programmable Drive Size Parameters
- Sector Interleaving -- Standard 1:1, software programmable.

1.8.1 450 Internal Registers

The use of specific bits within the 450 I/O Registers is described in Section 2.3. The 450's internal registers (which can be loaded and read by the software driver to establish commands) are listed in Table 2-1.

1.8.2 Command Technique

The 450 command technique allows command-chaining and concurrent host and Disk Controller operations. Channel control allows a software driver to establish a disk command and parameters in an I/O Parameter Block (IOPB) in system memory. The use of specific bits within the IOPBs is described in Section 2.4. IOPB formats are listed in Table 2-2.

The software driver initiates commands or command chains by loading the memory address of the first IOPB in the chain into the 450 Relocation and Address Registers. It then sets the 450 Status Register Bit 7 (GBSY), which stays set until (chained) command completion or an error is detected.

The 450 reads the command IOPB from system memory by Direct Memory Access (DMA) and performs the required function. On detecting an error, the 450 writes a completion code into bytes 2 and 3 of the IOPB related to the operation which caused the error. To reset the 450 at any time, the operating system reads the Controller Reset Register.

1.8.3 Chained Commands

The 450 provides inherent command-chaining capability for complex operations. The software driver can set up a string of commands (e.g., disk-to-disk copy) to allow executing a series of disk operations without operating system intervention. At any time, the operating system can add new IOPBs or remove completed IOPBs from the chain using the attention request protocol. Chained commands may provide overlap seek operations on Multi-drive subsystems.

SECTION 2 PROGRAMMING REFERENCE

2.0 GENERAL

This section contains the information needed to program the XYLOGICS Model 450 Disk Controller. The 450 was designed to easily interface many different processors with a wide variety of disk drives.

2.1 PROGRAMMING TECHNIQUES

Commands for the 450 are set up by the preparation of an I/O Parameter Block (IOPB) in system memory. The command is initiated by loading the address of the IOPB into registers on the 450 controller and setting GBSY of the Controller Status Register. GBSY stays set until all commands in the IOPB chain are completed or a hard error is detected. Upon completion, the 450 writes the corresponding completion codes into bytes 2 and 3 of the completed IOPB. Table 2-2 lists the bytes in an IOPB.

The IOPB is an area in system memory used for passing command level information between the 450 and the CPU. The CPU writes and reads the IOPB by using normal byte or word instructions. The 450 reads and writes the IOPB by using byte mode Direct Memory Access (DMA).

The CPU builds the IOPB in system memory with the appropriate information and then passes the address of the IOPB by loading the first four I/O registers. The CPU then sets GBSY in the CSR. The 450 transfers the IOPB from memory into the 450 at the start of a command. It will then process the command and reset GBSY of the CSR on completion. While processing the command, the 450 may access the IOPB again and it may also DMA data to or from memory. IOPBs may be chained together. When chained, the 450 may perform overlap seeks on multiple drives and execute data transfers without CPU intervention.

Each byte in the IOPB has an address relative to the command byte. In order to maintain IOPB integrity, all 24 bytes of allowable IOPB space must be reserved.

2.2 MULTIBUS ADDRESS RELOCATION

When accessing Multibus memory the 450 uses a technique called Address Relocation. Address Relocation is the addition of two addresses to form a larger physical address. Two types of Address Relocation are supported by the 450: 20-bit relocation and 24-bit relocation. Either type of relocation may be used when specifying 16 bits of memory address. For 16-bit memory addressing the relocation register should be loaded with zero. A staple on the 450 board selects either 20-bit relocation or 24-bit relocation. The positon of the 20- or 24-bit mode staple can be determined by examining bit 3 of the CSR.

NOTE

This manual refers to both IOPB relocation and data relocation. Do not get them confused. IOPB relocation refers to the address at which the IOPB resides in memory. Data relocation refers to the address at which the data buffer exists. Data relocation may be affected by RELO (bit 6 of Command byte 0), but IOPB relocation will not. The jumper for 20/24 bit address selection affects address relocation for both Data and IOPBs.

2.2.1 20-Bit Address Relocation

The 450 forms a 20-bit physical address by adding a 16-bit address word to a shifted 16-bit relocation word. The relocation word is shifted by 4 bits as shown in Figure 2-1A.

2.2.2 24-Bit Address Relocation

For 24-bit Address Relocation the 450 calculates a 32-bit physical address. The Address word comprises the least significant 16-bits, and the Relocation word becomes the most significant 16 bits. When addressing memory, only the lower 24 bits of the physical address are used. See Figure 2-1B.

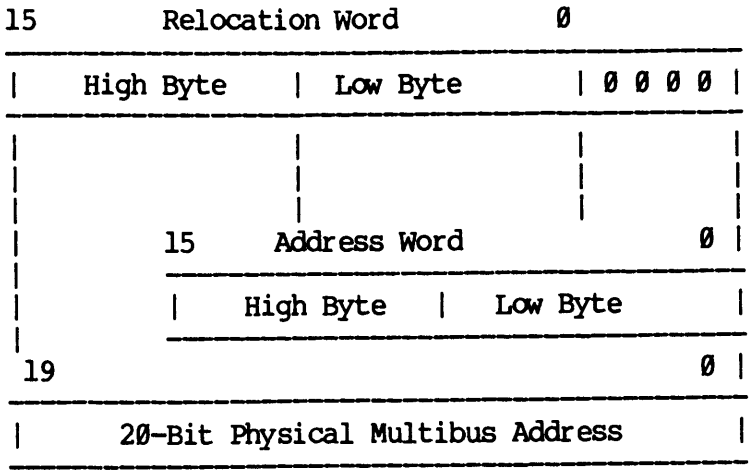


Figure 2-1A 20-Bit Multibus Address Relocation

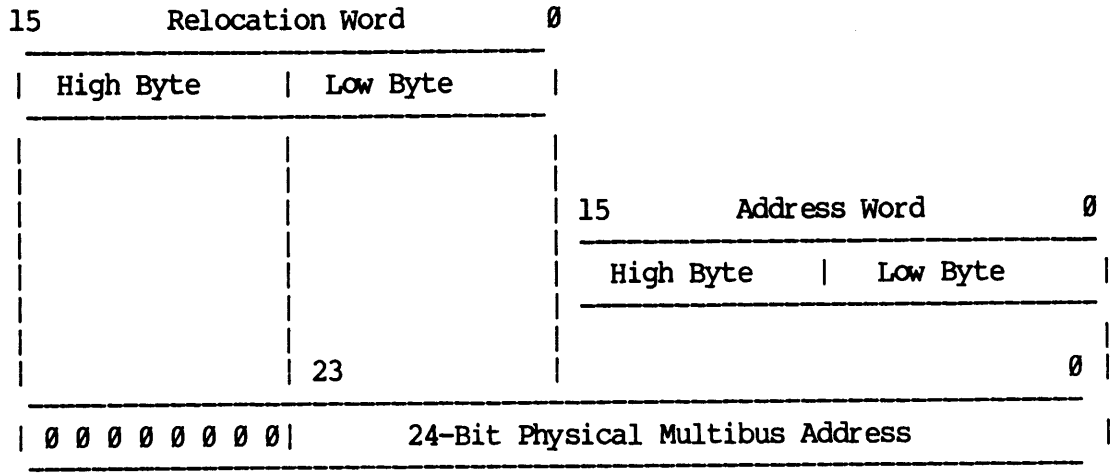


Figure 2-1B 24-Bit Multibus Address Relocation

Figure 2-1 Multibus Address Relocation

2.2.3 IOPB Address Relocation

IOPB Relocation occurs whenever a value is loaded into the IOPB Relocation registers. The IOPB Address registers and IOPB Relocation registers are combined to form either a 20-bit or 24-bit physical memory address as shown in Figure 2-1.

2.2.3 IOPB Address Relocation (continued)

When chaining IOPB's the Relocation registers are used in conjunction with the Next IOPB Address bytes to form a new 20-bit or 24-bit physical Multibus address. This address points to the next IOPB in the chain. All IOPBs in a chain must reside in the same 64K byte segment whose base address is in the Relocation Registers. The base address is computed by shifting the Relocation Registers 4 or 16 bits to the left depending on the relocation mode. See Figure 2-1.

2.2.4 Data Transfer Address Relocation

The starting memory address for a data transfer operation is specified by IOPB bytes C, D, E, and F. If RELO is clear, the Data Address bytes (IOPB bytes D & C) specify the physical Multibus address for the transfer. If RELO is set, the 450 uses Bytes F and E as the Data Relocation bytes and bytes D and C as the Data Address bytes. Data relocation occurs in the same manner as IOPB relocation. Figure 2-1 shows how data relocation addresses are formed.

2.3 450 I/O REGISTERS

	STANDARD I/O ADDRESSES (HEX)	
USAGE	8-Bit	16-Bit
IOPB Relocation Register Low Byte	40	EE40
IOPB Relocation Register High Byte	41	EE41
IOPB Address Register Low Byte	42	EE42
IOPB Address Register High Byte	43	EE43
Controller Status Register (CSR)	44	EE44
Controller Reset/Update Register	45	EE45

TABLE 2-1. 450 INPUT/OUTPUT REGISTERS

2.3.1 450 I/O Register Addressing

The 450 Input/Output Registers are addressed as input-output byte ports on the Multibus. The I/O Registers use a standard base address of 40H or EE40H. Table 2-1 summarizes usage and addressing of the 450 I/O Registers. See section 3.2.1 for alternate base addresses.

2.3.2 450 I/O Register Definitions

2.3.2.1 Relocation Registers

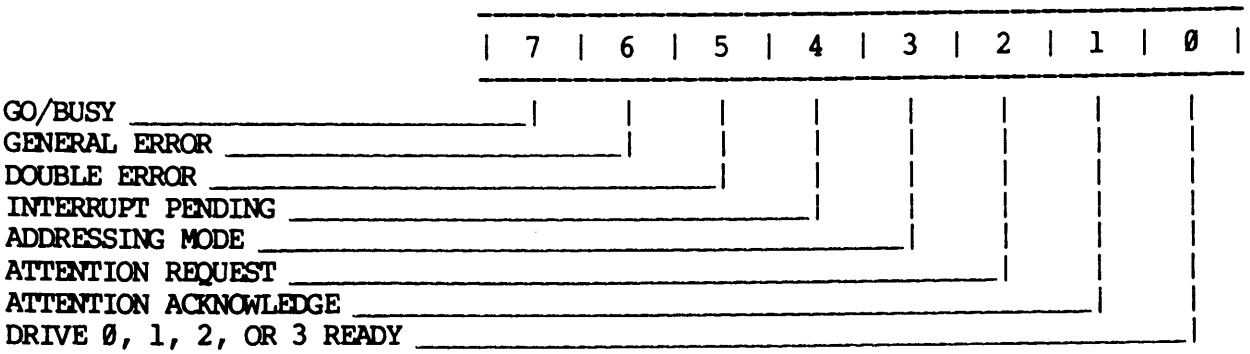
The Relocation Register is comprised of two bytes. The Relocation Register is the most significant portion of the IOPB memory address. On power-up this register is cleared by the 450. When using 16 bit addresses, this register should be zero. Writing anything except zero to this register causes IOPB relocation. See Figure 2-1 for an example of how 20- or 24-bit addresses are determined.

2.3.2.2 Address Registers

The Address Register is comprised of two bytes. This register is the least significant portion of the IOPB memory address. On power-up this register is cleared by the 450.

2.3.2.3 Controller Status Register

Controller Status Register -- I/O Address 44 or EE44



BIT	MNEMONIC	ACCESS	MEANING
7	GBSY	R/W	Go/Busy Bit - set it to start a transfer. GBSY remains set until the 450 completes the current IOPB command or command-chain. The 450 then clears GBSY to show readiness for another IOPB operation. While the 450 is busy, only GBSY, IPND, and AACK are valid.
6	ERR	R/W	General Error Bit - indicates that a hard error has been encountered. This bit must be cleared by either an Error Reset or a Controller Reset before another command can be executed. Set only on fatal errors. An Error Reset consists of writing a "1" to ERR.
5	DERR	R	Double Error - When set, it indicates a Double Error. A Double Error indicates that an error occured and a previous error condition has not been cleared. This usually means that the 450 cannot properly DMA the Status bytes to memory as a result of an error. A single or double error is cleared by an Error Reset or a Controller Reset.

NOTE:

It is more efficient to clear an error on the 450 by an Error Reset (writing a one to this bit) than by Controller Reset. Clearing by a Controller Reset is for 440 compatibility.

4	IPND	R/W	Interrupt Pending Bit - indicates that an IOPB is complete, the 450 has interrupted, and the interrupt has not been serviced. The interrupt service routine must clear this condition by either writing a 1 to this bit or a Controller Reset before another command (except IOPB update) can be executed. This and AREQ are the only 2 bits that can be written into the CSR while the 450 is busy.

2.3.2.3 Controller Status Register (continued)

NOTE:

It is more efficient to acknowledge an interrupt by an Interrupt Reset (writing a one to this bit) than by a Controller Reset. Acknowledging an interrupt by resetting the controller is for 440 compatibility.

BIT	MNEMONIC	ACCESS	MEANING
3	ADRM	R	Addressing Mode - when zero, indicates that the 450 is stapled for 20-bit addressing mode. When this bit is set it indicates the 450 is in 24-bit addressing mode. The addressing mode is selected by a hardware jumper on the 450 Board (see section 3.2.2) and is not software selectable.
2	AREQ	R/W	Attention Request - is used to gain the attention of the 450 when it is busy processing commands. It is used in conjunction with AACK, Attention Acknowledge. Software sets AREQ and waits until the 450 acknowledges the attention request with AACK. When AACK is set, system software may remove completed IOPBs and add new IOPBs. When work on the IOPB chain is complete, AREQ must be cleared by software, the 450 will then clear AACK and resume operation.
1	AACK	R	Attention Acknowledge - is set by the 450 to acknowledge an AREQ by the system software. It is cleared after AREQ is cleared. If Interrupt on Each IOPB is enabled, an interrupt occurs when the controller sets this bit.
0	DRDY	R	Drive Ready - Indicates the Ready-On Cylinder status of the last drive selected. After a Controller Reset the 450 updates this status.

NOTE

While the controller is busy the only allowed write access to the controller registers is bits 4 & 2 of the CSR.

2.3.2.4 Controller Reset/Update Register - I/O Address 45 or EE45

This is a special register whose functions are:

1. When the Controller Reset/Update IOPB Register is read, the 450 performs a Controller Reset, i.e., the registers will be cleared and IPND, ERR, and DERR will be cleared. The last drive selected (if none, Drive 0) will be reselected, the ready status latched, and then the drive will be released. A Controller Reset will not release all dual port drives previously reserved. Reading this register will cause GBSY to set while it executes the reset function.

2. When the Controller Reset/Update IOPB Register is written (actual data written is insignificant), the 450 updates the IOPB whose address is currently stored in the Address and Relocation Registers. The Update IOPB command writes the information contained in the 450 internal registers back to the current IOPB. Writing this register will cause GBSY to set until the update is complete.

2.3.2.4 Controller Reset/Update Register (continued)

An Update will update the IOPB to reflect the disk and data address at the termination of IOPB execution. The Update will also reflect any ECC error and the final sector count. On a normal termination, the sector count will be 0, and the completion code will also be 0.

2.3.3 Register Response

The time required to read or write registers has been improved to about 400 nsec. After any write to a register, the on-board microprocessor must update the information in its own RAM. A read or write to a 450 register immediately after a write to a register or read from the Reset register, will cause the 450 to delay in responding to the second transfer.

This delay, which is necessary for the microprocessor, will be less than 20 usec. Writing the CSR and reading or writing the Reset/update register will require more delay than the address registers. This delay starts after a write to any register or a read from the Reset/update register, and does not use any bus time unless another register is accessed before the delay is over. The second access will be held off only until the microprocessor has finished with the first.

2.4 IOPB DESCRIPTION

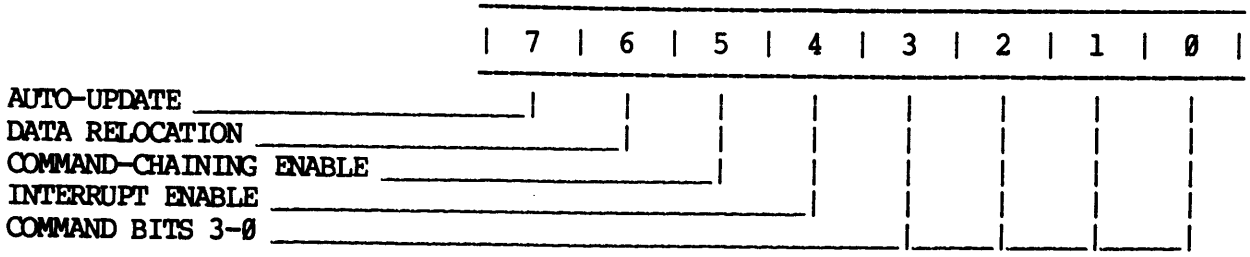
BYTE ADDRESS (HEX)	DESCRIPTION	MNEMONIC
0	Disk Command	COMM
1	Interrupt Mode	IMODE
2	Status Byte 1	STAT1
3	Status Byte 2	STAT2
4	Throttle	THROT
5	Drive Type, Unit Select	DRIVE
6	Head Address	HEAD
7	Sector Address	SECT
8	Cylinder Address Low	CYLL
9	Cylinder Address High	CYLH
A	Sector Count Low	SCNTL
B	Sector Count High	SCNTH
C	Data Address Low	DATAL
D	Data Address High	DATAH
E	Data Relocation Low	DATARL
F	Data Relocation High	DATARH
10	Head Offset	HDOFST
11	Reserved	RES
12	Next IOPB Address Low	NIOPL*
13	Next IOPB Address High	NIOPH*
14	ECC Mask Pattern High	ECCMH
15	ECC Mask Pattern Low	ECCML
16	ECC Bit Address Low	ECCAL
17	ECC Bit Address High	ECCAH

TABLE 2-2. 450 IOPB BYTE UTILIZATION

* All IOPBs in a chain must exist in the same 64K byte segment whose base address is specified by the 450 IOPB Relocation Registers.

2.4.1 Command Byte (IOPB Byte 0)

Command Byte -- (COMM)

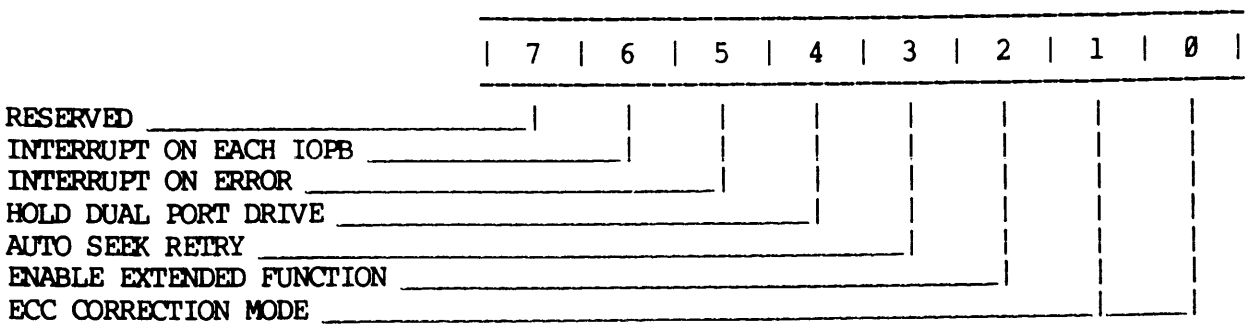


BIT	MNEMONIC	MEANING
7	AUD	Auto-Update - when set causes the current IOPB to be updated upon its completion. The Sector, Head, Cylinder, Sector Count and Data Address bytes will reflect the result of IOPB execution.
6	RELO	Relocation - if clear, Multibus data addresses are generated as 16-bit values, bits 16 through 23 are set to zero, and the Data Relocation Address bytes are ignored. If set, physical Multibus addresses are formed as shown in Figure 2-1. This bit enables only data relocation. IOPB relocation occurs whenever the IOPB Relocation register is non-zero.
5	CHEN	Chaining Enable bit - if clear, the 450 executes the current IOPB and clears GBSY upon completion. If CHEN is set, the 450 starts processing the next IOPB. The new IOPB's address is specified in the Next IOPB Address bytes. The 450 may examine all chained IOPB's in order to optimize transfers by performing any possible overlap seek operations.
4	IEN	Interrupt Enable - if clear, the 450 will not generate interrupts. If set, the 450 generates appropriate interrupts as defined by the Interrupt Mode byte.
3-0	COM	Command - interpreted as follows: See Section 2.5

Hex Value	Command
0	No Operation (NOP)
1	Write
2	Read
3	Write Track Headers
4	Read Track Headers
5	Seek
6	Drive Reset
7	Write Format
8	Read Header, Data and ECC
9	Read Drive Status
A	Write Header, Data and ECC
B	Set Drive Size
C	Self Test
D	Reserved
E	Maintenance Buffer Load
F	Maintenance Buffer Dump

2.4.2 Interrupt Mode/Function Modification (IOPB Byte 1)

Interrupt Mode/Function Modification (IMODE)



BIT	MNEMONIC	MEANING
7	-	This bit is reserved.
6	IEI	Interrupt On Each IOPB - when interrupts are enabled, and IEI is set, the 450 will interrupt each time an IOPB is completed or when AACK is set in the CSR.
5	IERR	Interrupt On Error - This is provided to maintain 440 compatability and has no effect on operation of the 450.
4	HDP	Hold Dual Port Drive - on a dual port drive, setting this bit will prevent the 450 from releasing the drive after the completion of the IOPB. When clear, the drive is released after each IOPB.
3	ASR	Auto Seek Retry - enables the 450 to recalibrate the drive once on either a cylinder/head header error, a drive fault, or a Hard Seek error, and to retry the transfer. If an auto retry was succesful, a completion code of 13H is provided.
2	EEF	Enable Extended Function - EEF enables commands 3 and 4, slip sector, and overlapped seeking. This is reset to prevent the 450 from scanning IOPBs to implement overlapped seeks.
1,0	ECM	ECC Correction Mode

Mode	Action on Error
0	o Provides an ECC pattern and offset. o Stops a chained transfer (fatal error). o Reports an ECC error (1EH or 06H) o Loses at least one Revolution.
1	o Does not correct or flag an error. o Continues a command chain. o Does not lose a Revolution.

2.4.2 Interrupt Mode/Function Modification (continued)

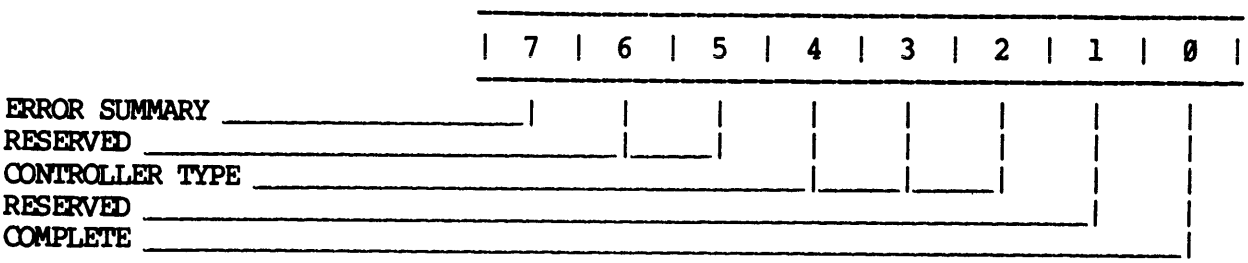
Mode	Action on Error
2*	o Corrects error. o Updates IOPB with soft ECC recovered error status 1FH. o Continues a command chain on soft error only. o Loses one Revolution
3*	o Does not correct an error. o Flags that an error occurred (hard ECC error). o Continues a chained command. o Does not lose a Revolution.

NOTE

Errors that do not stop the transfer at the occurance of the error can be masked by another error. For example in a multisector transfer, the second sector has an ECC recovered error, the transfer resumes and the fifth sector has a header not found error. In this case the Header Not Found status will be written over the ECC recovered status.

2.4.3 Status Byte 1 (IOPB Byte 2)

Status Byte 1 (STAT1)



BIT	MNEMONIC	MEANING
7	ERRS	Error Summary - when set indicates an error occured during IOPB processing. Clear indicates successful completion.
6-5	-	Reserved
4-2	CTYP	Controller Type - Each Xylogics Multibus controller has been assigned a controller type code as follows:

Code Bit 4	Code Bit 3	Code Bit 2	Controller
0	0	0	440
0	0	1	450
0	1	0	472

1	-	Reserved
0	DONE	Done - when set, Status Byte 2 holds the Completion Code for the IOPB.

2.4.3 Status Byte 1 (continued)

NOTE

Status bytes 1 and 2 must be zeroed by software before giving the IOPB to the 450. If DONE and EEF are set, the 450 will consider it complete.

2.4.4 Status Byte 2 (IOPB Byte 3)

When the IOPB has been executed, Status Byte 2 contains its Completion Code. Completion Codes are summarized in Table 2-3, and described with any required corrective action in the sections that follow. Unless otherwise noted, either writing a 1 into ERR or a Controller Reset will clear a hard error. Soft errors do not stop IOPB execution.

CODE	TYPE	DEFINITION
00	-	Successful Completion - No Errors
01	Hard	Interrupt Pending
02	-	Reserved
03	Hard	Busy Conflict
04	Soft	Operation Time Out
05	Hard	Header not Found
06	Hard	Hard ECC Error
07	Hard	Illegal Cylinder Address Error
08	-	Reserved
09	Soft	Sector Slip Command Error
0A	Hard	Illegal Sector Address
0B,0C	-	Reserved
0D	Hard	Last Sector Too Small
0E	Hard	Slave ACK Error (Non-Existent Memory)
0F,10,11	-	Reserved
12	Hard	Cylinder & Head Header Error
13	Soft	Seek Retry Required
14	Hard	Write Protect Error
15	Hard	Unimplemented Command
16	Hard	Drive Not Ready
17	Hard	Sector Count Zero
18	Hard	Drive Faulted
19	Hard	Illegal Sector Size
1A	Hard	Self Test A
1B	Hard	Self Test B
1C	Hard	Self Test C
1D	-	Reserved
1E	Hard	Soft ECC Error
1F	Soft	Soft ECC Error Recovered
20	Hard	Illegal Head Error
21	Hard	Disk Sequencer Error
22,23,24	-	Reserved
25	Hard	Seek Error

TABLE 2-3. SUMMARY OF COMPLETION CODES (IOPB BYTE 3)

2.4.4.1 Completion Code Descriptions

00 Successful Completion - Not an error, it indicates that the command is complete and the packet may be removed from the queue.

01 Interrupt Pending Error — This error occurs when an operation is attempted with an interrupt pending. Only Interrupt Reset, Update IOPB, Controller Reset or Error Reset operations are allowed while an interrupt is pending.

02 Reserved

03 Busy Conflict -- This error occurs if a register write is tried while GBSY is set. Bits 2 & 4 of the CSR are the only bits that can be written while the 450 is busy.

04 Operation Timeout - The IOPB was not completed within 2 seconds. Most common problems associated with this error are:

o Dual port access was not available.
o The drive failed to complete a seek.

05 Header Not Found Error -- This error occurs if the 450 does not find the requested sector. Other headers were read, and it was determined that the head and cylinder were correct. Some possible causes are:

- o The user specified drive type and the drive type in the header do not compare. Verify and correct the drive type.
- o The header was found, but the header ECC failed to compare.
- o If the drive type was correct and the error still occurs, try reformatting. If the error still occurs after reformatting, then a media defect in the header area must be assumed. The operating system should slip the sector or log the sector bad and discontinue its use.
- o There are more than 5 sectors more than specified in the Set Drive Size command. The 450 looks for headers for the specified number of sectors per track plus five. Readjust either the drive or Drive Type number of sectors per track.

06 Hard ECC Error -- This error occurs only on a Read command when the 450 has detected a data error longer than eleven bits in the data field or ECC correction is disabled (ECC Mode 3). Retry the previous Read operation. If the error still occurs, attempt to rewrite the data onto the sector in question. If the error persists, the operating system should slip the sector or log the sector bad and discontinue its use.

07 Illegal Cylinder Address -- The Cylinder Address specified was greater than the maximum cylinder number allowed. Check the cylinder address and the drive parameters, then retry the operation.

08,09 Reserved

0A Illegal Sector Address -- The Sector Address specified was greater than the maximum sector number allowed. Check the sector address and the maximum sector parameter for that drive type, then retry the IOPB operation.

2.4.4.1 Completion Code Descriptions (continued)

0B,0C Reserved

0D Last Sector too Small -- The very last sector (phantom or runt) sector is too small to write a complete header. Check the drive sector switches.

0E Slave ACK Error (Non-Existent Memory) -- This error occurs if the memory addressed by the 450 fails to respond within one millisecond. Validate the memory address or memory itself and retry the command.

0F,10 Reserved

11 Reserved

12 Cylinder and Head Header Error -- This error occurs if the cylinder or head address read from the disk fails to compare with the IOPB Cylinder and Head Address Bytes. The conditions that cause this error are:

- o The disk drive failed to seek to the correct cylinder. Issue a Drive Reset and retry the Read operation.
- o The disk format is corrupt. Reformat the sector in question, rewrite the data for the sector, and retry the Read operation. If the error persists, the operating system should slip the sector or log the sector bad and discontinue its use.
- o The head byte written on the disk does not compare with the Head Address selected. This may be due to a bad format or a hardware problem.

13 Seek Retry Required - A disk drive recalibrate was issued during the execution of this command to clear an error. See ASR in section 2.4.2.

14 Write Protect Error -- This error occurs when attempting a Write operation on a drive which is write-protected. Turn off write-protect and retry the Write operation.

15 Unimplemented Command -- This error occurs on all reserved commands.

16 Drive Not Ready -- This error occurs if the selected drive is not ready or is faulted. Issue Drive Reset to the drive in question. If the drive does not become ready, check these possible causes:

- o drive not up-to-speed, or hardware error,
- o bad or improperly connected "A" cable,
- o no drive of the specified Unit Number connected to the 450,
- o Signal "ACLO" on Multibus backplane connector P2 is low.

17 Sector Count Zero -- This error is caused by issuing the 450 an IOPB with a sector count of zero. All data transfer operations require a positive sector count. Correct the program in error and start the transfer again.

18 Drive Faulted -- This error code is returned when something has caused a fault in the selected disk drive. Issue Drive Reset. If the Fault still exists, operator intervention is needed to correct the drive fault.

2.4.4.1 Completion Code Descriptions (continued)

19 Illegal Sector Size -- The drive sectoring does not allow sufficient room for the header and data fields to be written.

- o The drive has more sector pulses than five more that the number of specified data sectors.
- o The last sector is too small to be a data sector, but has been included in the specified sector count. Adjust the drive to more sectors, or the drive type to fewer sectors.

1A Self Test A Failure - Either the microprocessor or its internal RAM failed diagnostics.

1B Self Test B Failure - Either the microprocessor or header shift register has failed.

1C Self Test C Failure - The buffer RAM failed diagnostics.

1D Reserved

1E Soft ECC Error -- This error occurs only on a Read operation when the 450 detects a correctable 11-bit-or-less error in the data field of the current sector and the ECC Mode is 0.

1F Soft ECC Recovered Error -- This error indicates that the ECC mode is 2 and one or more ECC errors were corrected during the transfer.

20 Illegal Head Address -- This error occurs if the Head Address specified is greater than the maximum Head Address allowed. The maximum Head Address varies with the Drive Type specified. Correct the Drive Type and the Head Address for the drive in use, and retry the operation.

21 Disk Sequencer Error -- This error indicates that the disk sequencer did not finish its operation within the alloted time. Several things can cause this problem:

- o The 450 does not receive the Servo Clock signal from the selected disk drive. A possible cause is the "B" cable may not be properly connected. Try a different "B" cable port on the 450.
- o The 450 isn't receiving any read data from the selected drive. Check the "B" cable.

22,23,24 Reserved

25 Seek Error --The drive has reported a seek error. This can be caused by selecting a cylinder higher than the drive maximum, or selecting a head beyond that supported by the drive. Check the drive parameters for the drive type you are using.

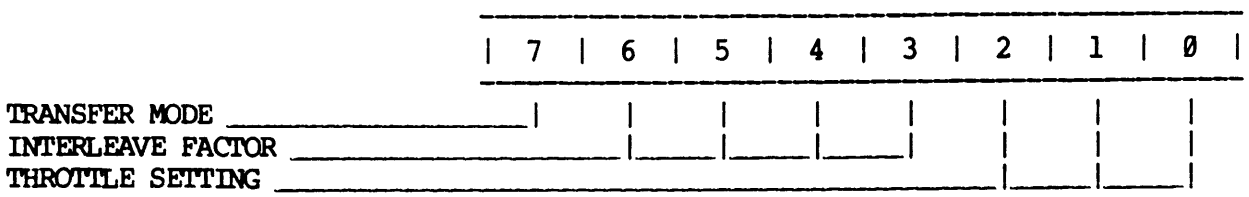
2.4.5 Throttle (IOPB Byte 4)

2.4.5.1 Throttle Byte Description

The Throttle byte selects the number of DMA cycles in a DMA burst, word or byte mode transfers, and the Interleave Factor.

2.4.5.1 Throttle Byte Description (continued)

Throttle -- IOPB Byte 4



BIT	MNEMONIC	MEANING
7	B/W	Transfer Mode - selects either word or byte DMA transfers between the 450 and system memory allowing the 450 to operate with word- and byte-oriented memory mixtures. B/W should be clear when reading or writing 16-bit words in memory, or should be set when reading or writing 8-bit bytes in memory.
6-3	-	Interleave Factor - used during format and Read/Write Header Data and ECCs. For 1:1 interleaving, the interleave factor is 0. For others the interleaving ratio is (n+1):1 where n is the interleave factor, i.e.,

Interleave Factor Bit 6-3	Ratio
0	1:1
1	2:1
2	3:1
:	:
F	16:1

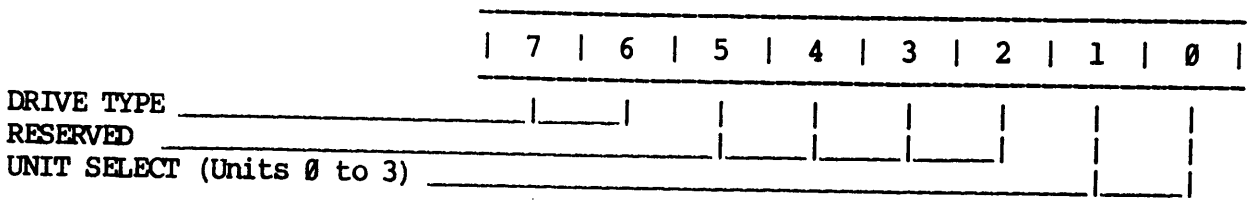
2-0	THRO	Throttle Setting - selects the maximum number of DMA cycles the 450 executes each time it assumes bus mastership as shown in Table 2-4. During one DMA cycle, one word or one byte (depending on B/W) is transferred. This throttle value determines the DMA burst length for both data and IOPB DMA transfers.

Value of Bits 0-2	DMA Cycles
0	2
1	4
2	8
3	16
4	32
5	64
6	128
7	128

TABLE 2-4 450 THROTTLE SETTING

2.4.6 Drive Type, Unit Select (IOPB Byte 5)

Drive Type, Unit Select



BIT	MNEMONIC	MEANING
7-6	DT	Drive Type - These bits select a specific size of drive. The Drive Type bits give the software control of drives of mixed capacities, without regard to either the 450 "B" cable port they are connected to or the logical unit number of the drive. The specific characteristics of a drive such as head offset, max head, max sector and max cylinder are specified and defined for a specific Drive Type by a Set Drive Size command. See section 2.5.12
5-2		These bits are reserved.
1-0	UNIT	The Unit Select bits contain the physical unit number of the disk unit to be accessed.

2.4.6.1 Drives with Fixed and Removable Media

Any physical drive with fixed and removable media, like the CDC CMD or LMD, uses two drive types, but is accessed as one logical unit. (i.e. the removable media of unit 0 is drive type 2, and the fixed media of unit 0 is drive type 3.) The head offset refers to the bit(s) that must be set during head tag to the drive to select between the fixed and removable portions of the drive. Both the fixed and removable media are referred to by the same physical unit number. Please see Section 2.5.13.

2.4.6.2 Controller Usage of Drive Type

The software must specify the Drive Type so the 450 will know how to address the disk drive. The Drive Type is written into the header on the disk to prevent accidental addressing of a drive with the wrong Drive Type. It may be retrieved from a formatted disk by using a Read Header - Data - ECC command on sector zero of cylinder zero. This allows software to poll all disks to determine drive type. Consult Section 2.5.11.3.1 to locate the Drive Type field in the header information.

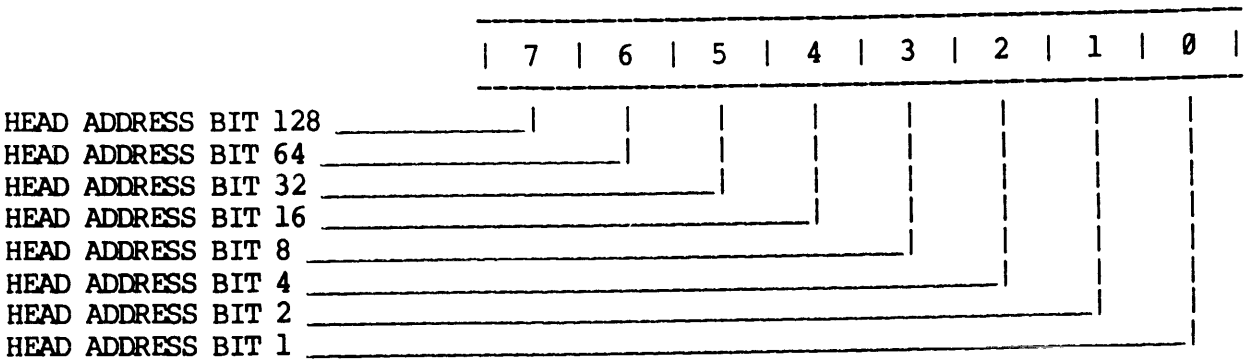
Accessing a drive with an incorrect Drive Type results in a Header Not Found Error. It is important that the correct Drive Type be specified for the disk drive being used.

2.4.7 Head Byte (IOPB Byte 6)

The Head Byte specifies the head number a transfer starts on. Heads are numbered starting with head 0. Attempting to access a head number larger than max-head will cause an Illegal Head Address error.

2.4.7 Head Byte (IOPB Byte 6) (continued)

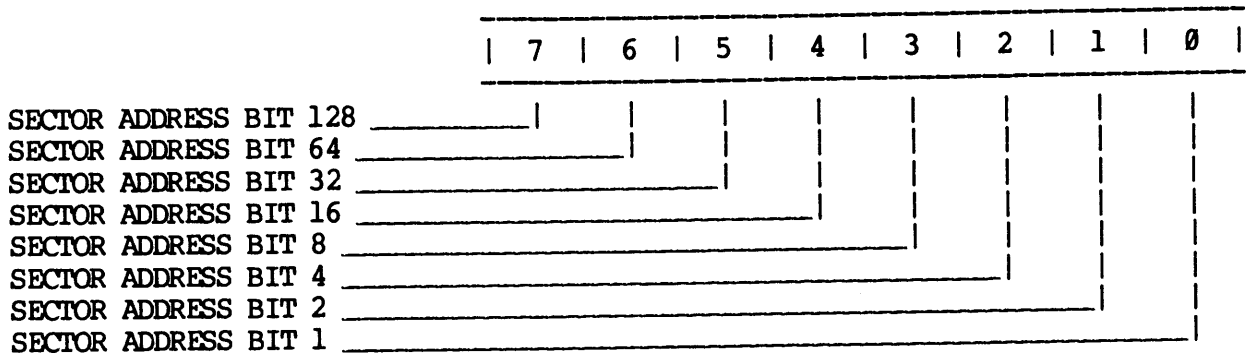
Head Byte -- IOPB Byte 6



2.4.8 Sector Byte (IOPB Byte 7)

The Sector byte specifies the starting sector number for a transfer. The sector number is used in all commands where the disk is read or written.

Sector Byte -- IOPB Byte 7



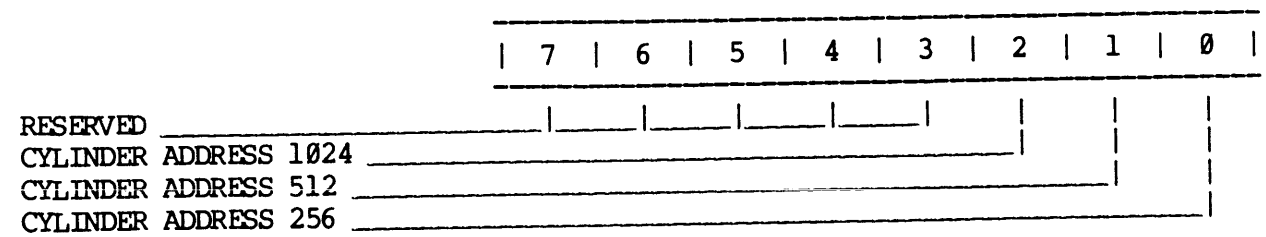
2.4.9 Cylinder Address (IOPB Bytes 8 and 9)

The Cylinder Address is specified in IOPB bytes 8 and 9. As illustrated below, IOPB byte 8 is the least significant portion of the Cylinder Address and IOPB byte 9 is the most significant portion of the Cylinder Address.

The cylinder address must be specified for all operations where data is moved to or from the disk.

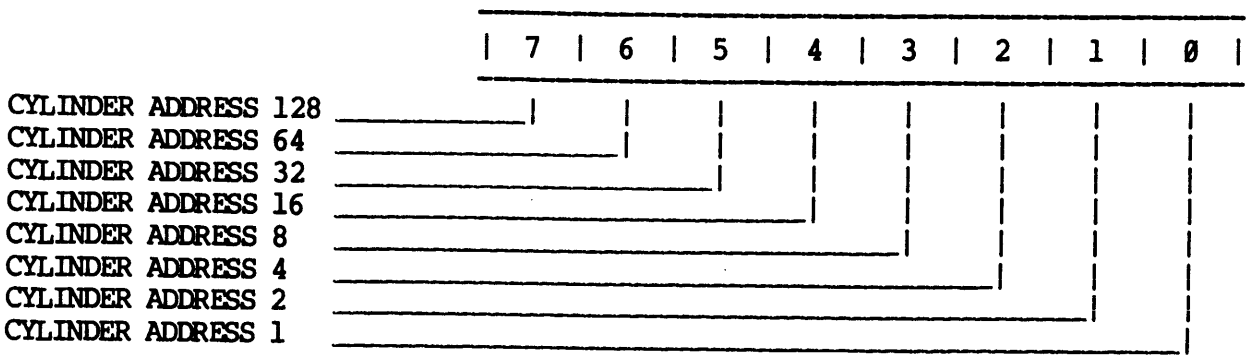
As shown in the following figures, the Cylinder Address is an 11-bit binary number. The lowest cylinder address is zero while the largest cylinder address is the number of cylinders minus 1.

Cylinder Address -- IOPB Byte 9



2.4.9 Cylinder Address (IOPB Bytes 8 and 9) (continued)

Cylinder Address -- IOPB Byte 8



2.4.10 Sector Count (IOPB Bytes A and B)

The 450 disk controller transfers information in whole sectors. The sector count, a 16-bit number stored as 2 bytes in the IOPB, is the number of sectors to be transferred. Byte A of the IOPB is the least significant half of the sector count while byte B is the most significant half. With a 16-bit sector count you can execute a continuous transfer of up to 65,535 sectors with one IOPB (memory permitting).

The 450 can support standard sector sizes of 256, 512 and 1024 bytes per sector. Custom sector sizes, ranging in even byte sizes from 256 to 4096 bytes per sector, may be handled with special firmware.

2.4.10.1 Sector Count (IOPB Byte A) for Read Drive Status Command

On a Read Drive Status command, Byte A is filled with status information from the selected drive. This is a special case in which this byte is used to return drive status information.

Read Drive Status Command -- IOPB Byte A

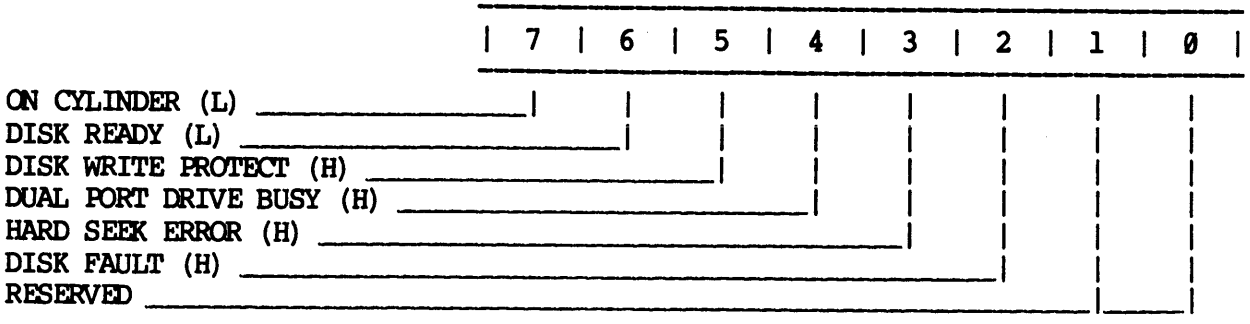


TABLE 2-6. DEFINITION OF IOPB "BYTE A" ON READ DRIVE STATUS

BIT	MNEMONIC	MEANING
7	ONCL	ON CYLINDER(L) - represents the On-Cylinder status of the selected drive. If the drive is ready and this bit is zero, this drive is not seeking. If this bit is a one, then the heads of the selected drive are not positioned over a cylinder.

2.4.10.1 Sector Count (IOPB Byte A) for Read Drive Status Command (continued)

BIT	MNEMONIC	MEANING
6	DRDY	DRIVE READY(L) - will be zero if there is a drive selected and ready at this Unit Number.
5	WRPT	DISK WRITE PROTECT(H) - is set when the selected disk is write protected.
4	DPB	DUAL PORT BUSY(H) - if set, indicates that the drive is dual ported and is selected by the other controller.
3	SKER	HARD SEEK ERROR(H) - will be set if the selected drive is reporting a Hard Seek Error.
2	DFLT	DISK FAULT(H) - will be set if the selected drive is reporting any type of fault.
0,1	-	RESERVED

2.4.11 Data Address (IOPB Bytes C and D)

The Data Address is composed of two bytes. Byte C is the Data Address low byte, and byte D is the Data Address high byte. The Data Address is the memory address to or from which a data transfer will start.

The 16-bit Data Address is added to a shifted Data Relocation word to form the physical starting address of a data transfer. Please see Figure 2-1.

2.4.12 Data Relocation Pointer (IOPB Bytes E and F)

The Data Relocation Pointer is composed of two bytes in the IOPB. Byte E is the low byte and Byte F is the high byte. When forming a physical address, the Data Relocation bytes and Data Address bytes are used to create Multibus addresses, as shown in Figure 2-1. However, the Data Relocation bytes are ignored if RELO is clear in the IOPB Command Byte.

2.4.13 Head Offset (IOPB Byte 10)

IOPB Byte 10 -- Head Offset - this byte is used by the Set Drive Size and Read Drive Status commands. It determines the offset required to access a fixed or removable section of a fixed/removable drive such as the CDC CMD or LMD. This byte contains the bits which must be added to the head value sent to the drive to select either the fixed or removable portion of the drive. In the case of the CMD, the Head Offset must equal 10H when defining the fixed portion of the drive, and 0 for the removable portion. In both cases the drive unit number will be 0 for Drive 0.

2.4.14 Reserved (IOPB Byte 11)

2.4.15 Next IOPB Address (IOPB Bytes 12 and 13)

When using command chaining, the starting address of the next IOPB must be specified. These two bytes (bytes 12 and 13) are combined with the IOPB Relocation registers to determine the next IOPB address. They are the missing link in the IOPB chain.

2.4.15 Next IOPB Address (IOPB Bytes 12 and 13) (continued)

Byte 12 is the low byte and byte 13 is the high byte of the Next IOPB Address. These two bytes make up a 16-bit address similar to the IOPB Address Register. The Next IOPB Address is added to the IOPB Relocation Register to form a physical address (Figure 2-1). This physical address is 20- or 24-bits in length, depending on the addressing mode selected and is used as the pointer to the next IOPB in the chain. All IOPBs in a chain are relative to the same relocation address and thus must be within a 64K byte block of memory.

To enable command chaining, set CHEN in the Command byte of the IOPB. If command chaining is not enabled, bytes 12 and 13 are ignored.

2.4.16 ECC Pattern Word (IOPB Bytes 14 and 15)

The ECC Pattern or Mask Word is a 11-bit word used in the soft ECC correction procedure. The ECC Pattern Word is stored in IOPB Bytes 14 and 15. A Soft ECC Error is defined as any single error of 11 bits or less. The error is still considered soft if there are bits wrong at each end of an 11-bit word, but the bits in the center are correct. This word provides a pattern to correct data in memory.

The ECC Pattern Word is calculated by the 450 and left in reverse order, in IOPB Bytes 14 and 15 as illustrated below. Before using the ECC Pattern Word a bit-reversal process must be executed to correct the direction of this mask, in relation to the data stream it will correct. After the reversal process, the equivalent word will have Pattern Bit 0 in Bit 16, Pattern Bit 1 in Bit 15, and so on. The five least-significant bits will be zero. See section 2.6.3.7

ECC Pattern Byte 14

	7	6	5	4	3	2	1	0
PATTERN BIT 11								
PATTERN BIT 10								
PATTERN BIT 9								
ZERO BITS								

ECC Pattern Byte 15

	7	6	5	4	3	2	1	0
PATTERN BIT 8								
PATTERN BIT 7								
PATTERN BIT 6								
PATTERN BIT 5								
PATTERN BIT 4								
PATTERN BIT 3								
PATTERN BIT 2								
PATTERN BIT 1								

2.4.17 ECC Address Word (IOPB Bytes 16 and 17)

When a Soft ECC Error occurs the 450 also calculates an ECC Address Word. Two bytes are used to store the ECC Address Word. IOPB byte 17 is the most significant, and IOPB byte 16 is the least significant. This address word points to the bit within a sector where the data in error starts. By exclusive ORing the ECC mask with this bit string the error may be corrected.

2.5 COMMANDS

The four least-significant bits of the Command byte are the IOPB Command bits. These four bits allow up to sixteen possible commands, one of which is reserved. Each command will start at the beginning of a page, will have a short description, and a reference IOPB. The IOPBs are encoded to show which bytes are used for, and which are returned after execution. The bytes indicated are returned with or without an update.

The commands are transferred to the 450 via a 24 byte long IOPB. Each 450 command requires different IOPB bytes. In general all commands use bytes 0 through 0FH, with bytes 10H through 17H being dependant on the command executed. Only the Read command uses ECC bytes 14H through 17H although all bytes must be reserved.

2.5.1 NOP Command (Command Code 0)

2.5.1.1 General

The No Operation (NOP) command causes the controller to select a disk drive, save DRDY (bit 0 of CSR) and release the drive.

2.5.1.2 IOPB

NOP

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EBF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type		0	DONE	
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	Head Offset							
11 - RES	0							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High			0				
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required for execution. Returned Value

2.5.2 Write Command (Command Code 1)

2.5.2.1 General

The Write command is the standard command used to transfer data to the disk. It will start at the disk and memory addresses specified in the IOPB and transfer as many sectors as requested. The 450 will cross cylinder, head and sector boundaries as required.

2.5.2.2 IOPB

WRITE

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type	0					Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	Head Offset							
11 - RES	0							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High	0						
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required for execution. Returned Value

2.5.2.3 Detailed Description

2.5.2.3.1 Implied Seeks

The 450 will issue an implied seek on a Write command. This seek will be issued as the first operation after reading the IOPB from system memory. If chained operations are implemented and EEF is set, the 450 will scan the remainder of the chain for the possibility of overlap seeks.

2.5.2.3.2 Filling Buffer

When the seek is complete the 450 will access the IOPB to determine the command parameters, and begin to fill the FIFO buffer. After sufficient data (minimum one sector) is in the buffer the controller will begin to look for sector coincidence. This process insures that sufficient data is available in the buffer at the start of the write.

2.5.2.3.3 Sector Coincidence

The 450 selects the proper head and tests the write protect status of the drive. The 450 will then read each sector header and compare it to the requested disk address. When a match is found, the data transfer begins. If a match is not found within one revolution plus five sectors, an error 5 or 12 will be generated.

2.5.2.3.4 Write Data

After a valid header has been found, the sequencer will count the appropriate number of bytes and then write the sync bits. It will then take words out of the FIFO, serialize them, generate a new ECC value, and write them to the disk. As data is removed from the FIFO, it is replaced by appropriate DMAs from system memory.

2.5.2.3.4 Throttle

The throttle is the maximum number of transfers that will be allowed each time the 450 becomes bus master. On a write operation the first DMA bursts will be at the programmed throttle value until the buffer is full. After data starts moving to the disk, the typical burst will be less than the throttle value. Words will continue to be transferred into the controller as required until the sector count goes to zero.

2.5.2.3.5 ECC

After the data field of a sector has been written, the ECC value generated from the data field is written.

2.5.2.3.6 Incrementing Disk Address

The sector address will be incremented by 1 as each sector is written. If the sector address is greater than max sector, it will be reset to zero and the head address will be incremented. If the resultant head address is greater than maximum head, then the head address will be reset to zero and the cylinder address will be incremented by one. If the cylinder address is greater than maximum cylinder when the implied seek is issued, an error will be generated.

2.5.2.3.7 Completing a Transfer

The sector count will be decremented by 1 for each sector transferred. At the end of the sector, the sector count is tested to determine if the transfer is complete. If the transfer is not complete, the next sector is transferred. If the cylinder address has just been incremented to a legal address, an implied seek will be issued.

When the transfer is complete, the two status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. If AUD of the IOPB command byte was set, the IOPB will be updated.

If the transfer ends in a hard error, the transfer is stopped, the two status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. Any chained operations will be halted. The IOPB address and relocation registers will be pointing to the IOPB which caused

2.5.2.3.7 Completing a Transfer (continued)

the error. If AUD was set, the IOPB will be updated.

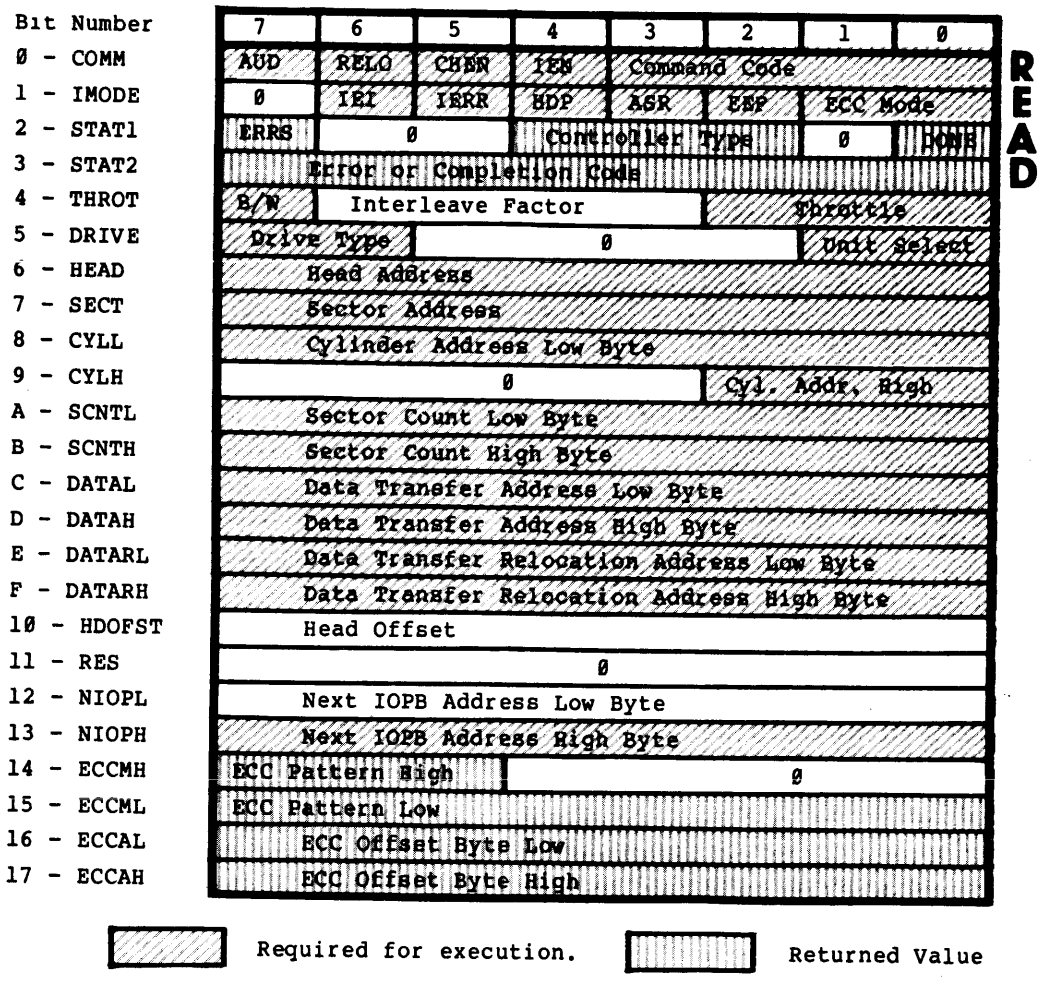
If the transfer ends with a soft error, the two status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. Any chained operations will be continued. If AUD was set, the IOPB will be updated. The ERR bit of the CSR will not be set since this is a soft error.

2.5.3 Read Command (Command Code 2)

2.5.3.1 General

The Read Command transfers data from the disk to memory. The command will transfer data from the disk to memory, starting at the disk and memory addresses specified in the IOPB, and cross sector, head, and cylinder boundaries as required.

2.5.3.2 IOPB



2.5.3.3 Detailed Read Description

2.5.3.3.1 Implied Seeks

The 450 will issue an implied seek on a Read command. This seek will be issued as the first operation after reading the IOPB from system memory. If chained operations are implemented and EEF is set, the 450 will scan the remainder of the chain for the possibility of overlap seeks.

2.5.3.3.2 Seek End

The 450 will scan the drives to determine when the drive has completed its seek.

2.5.3.3.3 Sector Coincidence

The 450 will read each sector header and compare it to the requested disk address. When a comparison is true, the transfer process will be initiated. If a comparison is not true within one revolution plus five sectors, an appropriate error will be generated.

2.5.3.3.4 Read Data

After a valid header match the sequencer will wait for the sync bits for the data field. As data is read in from the disk it is de-serialized and placed into the FIFO buffer. When data becomes available at the other end of the FIFO, the 450 requests the bus and transfers the data to memory via DMA. The serial stream of data is also used to generate an ECC.

2.5.3.3.5 Throttle

The throttle is the maximum number of transfers that will be allowed each time the 450 becomes bus master. On a read operation the first DMA bursts will be at minimum value since the limiting factor of the DMA burst length is the number of words available from the FIFO. After the initial few DMA bursts, the typical burst length will increase, possibly approaching the throttle limit. Words will continue to be transferred from the controller as required until the sector count goes to zero and the buffer is empty.

2.5.3.3.6 ECC

When the data field of a sector has been read, the ECC value generated by the 450 during the read is compared to the ECC written on the disk during the original write.

2.5.3.3.7 Incrementing Disk Address

The sector address will be incremented by 1 as each sector is read. If the sector address is greater than max sector, it will be reset to zero and the head address will be incremented. If the resultant head address is greater than maximum head, then the head address will be reset to zero and the cylinder address will be incremented by one. If the cylinder address is greater than maximum cylinder when the implied seek is issued, an error will be generated.

2.5.3.3.8 Completing a Transfer

At the end of the sector, the sector count is tested to determine if the transfer is complete. If the transfer is not complete, the next sector is transferred. If the cylinder address has just been incremented to a legal value, an implied seek will be issued.

When the transfer is complete, the two status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. If AUD of the IOPB command byte was set, the IOPB will be updated.

If the transfer ends in a hard error, the transfer is stopped, the two status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. Any chained operations will be halted. The IOPB address and relocation registers will be pointing to the IOPB which caused the error. If AUD was set, the IOPB will be updated.

2.5.3.3.8 Completing a Transfer (continued)

If the transfer ends with a soft error, the two status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. Any chained operations will be continued. If AUD was set, the IOPB will be updated. The ERR bit in the CSR will not be set since this is a soft error.

2.5.3.3.9 Read Command Encounters an ECC Error in ECC Mode 0

When the ECC value calculated from a Read does not compare with the ECC value written on the disk, the 450 stops reading. All data for that sector is written to memory and an ECC calculation begins. Through a shifting and counting process, the 450 determines where and how much of an error occurred.

If it finds an error larger than 11 bits, it is a hard error and Error Code 06 is written into the Completion Code Byte.

If the error is 11 bits or less, it is a soft error and the ECC Pattern and Address Words are written to their IOPB bytes and Error Code 1E is reported. This mode is supported for compatibility with the Model 440 Controller.

When an ECC Error has been encountered the internal registers will be in the following state: the disk address will point to the sector containing the error, the Data Address and Relocation address will point to the first byte of data from the sector following the sector in error, and the sector count will be equal to the number of sectors remaining, plus 1. To retrieve this information either the command must be in Auto-Update mode or a write of the Update IOPB register must be issued. This will identify the offending sector and its related Data Address.

To continue the transfer after a soft error, update the sector count (Subtract 1) and update the disk address then restart the IOPB.

2.5.3.3.10 Read Command Encounters an ECC Error in Mode 1

ECC errors are not detected in this mode. The data transfer continues since no error was encountered.

2.5.3.3.11 Read Command Encounters an ECC Error in Mode 2

If an ECC correctable error is encountered in Mode 2, the 450 will stop the transfer, correct the data in memory and resume transferring data on the next revolution of the disk. A soft ECC recovered error will be reported in the IOPB, and if chain mode is enabled, the chain will be continued.

2.5.3.3.12 Read Command Encounters an ECC Error in Mode 3

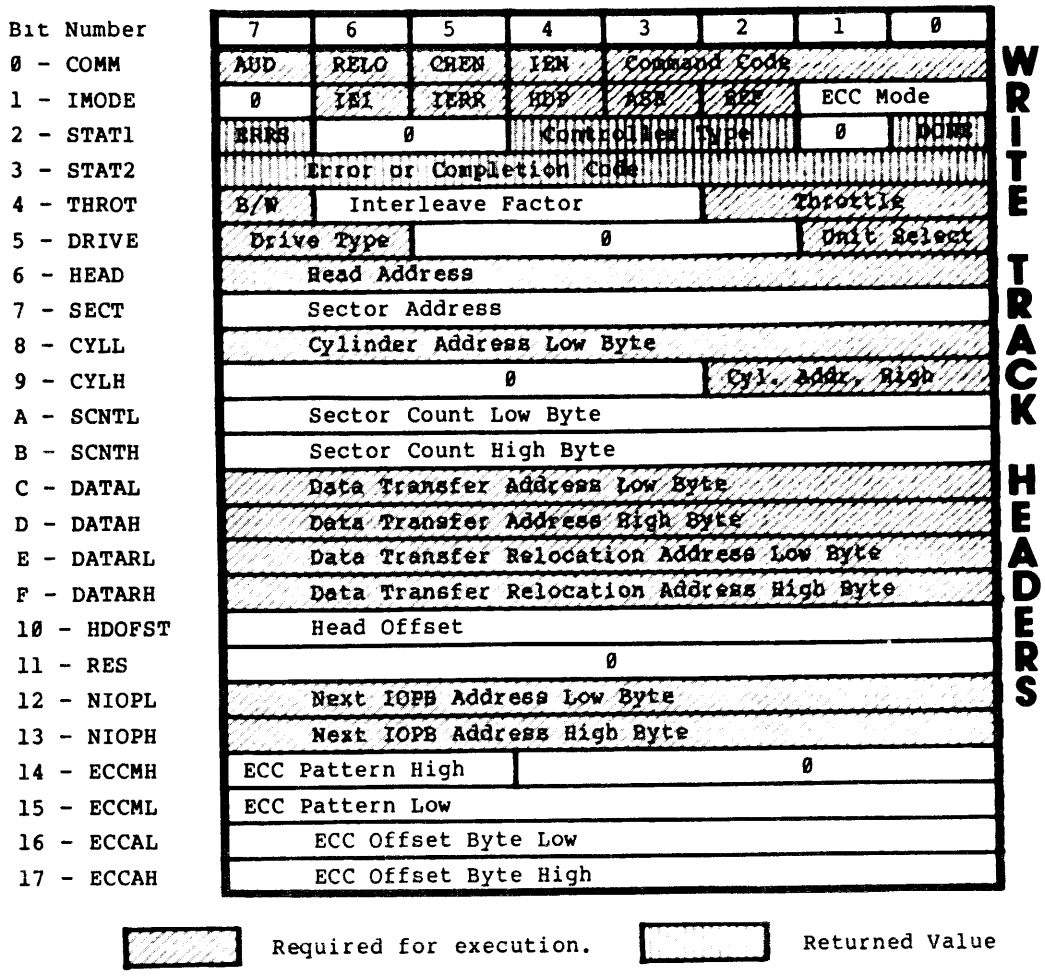
If an ECC error is detected the data transfer continues as if no error was detected. When the transfer completes, the error status code in the IOPB will indicate that it encountered one or more uncorrected ECC errors with a Hard ECC error, 06H.

2.5.4 Write Track Headers (Command Code 3)

2.5.4.1 General

This command and Read Track Headers will provide the ability to avoid media defects by slipping sectors. The Write Track Headers command will format a track with header data which is resident in system memory. The header data can be transferred to system memory by the Read Track Headers command. This data is the actual header for each sector on the track starting at psuedo index, including bad and spare sectors. Since this is a format type command, all data on that track will be overwritten. Please see section 2.6.4. This command will only function when enabled by EEF being set.

2.5.4.2 IOPB



2.5.4.3 Detailed Description

2.5.4.3.1 Data Buffer

A data buffer must be constructed in system memory prior to issuing a Write Track Headers command. The Read Track Headers command will construct a proper buffer in host memory. This buffer will consist of four bytes of data for each sector, therefore the total buffer length will be four bytes times the total number of sectors on the track including spare and bad sectors. The 450 counts the actual number of sectors on the drive. This count is used as the number of sectors for the Write Track Headers command. The first four bytes will be the header data for sector zero, the first sector after psuedo index. The next four bytes will be for the next sector, etc.

2.5.4.3.2 Implied Seeks

The 450 will issue an implied seek on a Write Track Headers command. The seek will be issued as the first operation after reading the IOPB from system memory. If chained operations are implemented, and EEF is set, the 450 will scan the remainder of the chain for the possibility of overlap seeks.

2.5.4.3.3 Seek End

The 450 will scan the drives to determine when the drive has completed its seek. When the requested drive has completed its seek, the 450 will access the IOPB to determine the command parameters, and then begin to fill its buffer. When sufficient data is in the buffer, the search for psuedo index will begin.

2.5.4.3.4 Throttle

The throttle is the maximum number of DMA transfers that can occur each time the 450 becomes bus master. On a Write Track Headers operation the DMA bursts will be at the specified throttle. The DMA transfers will continue until enough data is available to format an entire track.

2.5.4.3.5 Psuedo Index

The 450 has two different format schemes, 440 compatible and 450 standard. Psuedo index and physical index are the same in 440 compatible format. Psuedo index is delayed from physical index by one sector per track in the 450 standard format. When index has arrived under the head, the first four bytes of data are used to format that sector. The 450 automatically calculates and appends the ECC to the header.

2.5.4.3.6 Format the Track

As each successive sector arrives under the head, four bytes are taken from the buffer and used as the header for that sector. The data field portion of the sector is not written by a Write Track Headers command. Therefore the data will be invalid after this operation. This operation will continue for each sector on the requested track.

2.5.4.3.7 Incrementing Disk Address

The sector address will be incremented by 1 for each sector written. At the end of a successful command the head address will be incremented by 1. If the resultant head address is greater that maximum head, it will be cleared and the cylinder address will be incremented.

2.5.4.3.8 Completing a Transfer

The 450 will format an entire track if errors are not encountered. When the format is complete the two status bytes will be updated. If AUD is set, the IOPB will be updated and if interrupts are enabled, an interrupt will be generated.

If the transfer ends in a hard error the transfer is stopped and any chained operations are also terminated. The two status bytes will be updated. If AUD is set, the IOPB will be updated and if interrupts are enabled, an interrupt will be generated.

2.5.4.3.8 Completing a Transfer (continued)

If the transfer ends in a soft error, the transfer has completed, and chained operations will not be terminated. The two status bytes will be updated, if AUD is set the IOPB will be updated, and if interrupts are enabled an interrupt will be generated.

2.5.5 Read Track Headers (Command Code 4)

2.5.5.1 General

This command and Write Track Headers will provide the ability to avoid media defects by slipping sectors. The Read Track Headers command will read the header from each physical sector starting at psuedo index and transfer the data in order to system memory. The headers may not be in sequential order due to interleaving and sector slip. The headers are written back to the track by the Write Track Headers command. The buffer will contain the actual header data from each sector on the track starting at psuedo index, including bad and spare sectors. This command will only function if enabled by setting EEF.

2.5.5.2 IOPB

READ TRACK HEADERS

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	ADD	RELO	CHEN	IAM	Command Code			
1 - IMODE	0	IAI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type	0				Unit Select		
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	Head Offset							
11 - RES	0							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High				0			
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required for execution. Returned Value

2.5.5.3 Detailed Description

2.5.5.3.1 Data Buffer

A data buffer must be allocated in system memory prior to issuing a Read Track Headers command. The total buffer length should be four bytes times the total number of sectors on the track including spare and bad sectors. The 450 counts the actual number of sectors on the drive. This count is used as the number of sectors for the Read Track Headers command.

2.5.5.3.2 Implied Seeks

The 450 will issue an implied seek on a Read Track Headers command. The seek will be issued as the first operation after reading the IOPB from system memory. If chained operations are implemented, and EEF is set, the 450 will scan the remainder of the chain for the possibility of overlap seeks.

2.5.5.3.3 Seek End

The 450 will scan the drives to determine when the drive has completed its seek. When the requested drive has completed its seek, the 450 will access the IOPB to determine the command parameters and initiate a search for psuedo index.

2.5.5.3.4 Psuedo Index

The 450 has two different format schemes, 440 compatible and 450 standard. Psuedo index and physical index are the same in 440 compatible format. Psuedo index is delayed from physical index by one sector per track in the 450 standard format. When index has arrived under the head, the 450 will read the header from that sector, and transfer the data to the buffer.

2.5.5.3.5 Read the Track

As each sector arrives under the head, four bytes are read from the header and transfered to the buffer. This operation will continue for each sector on the requested track.

2.5.5.3.6 Empty Buffer

When a complete track has been read the 450 DMAs the header data to system memory.

2.5.5.3.7 Throttle

The throttle is the maximum number of DMA transfers that can occur each time the 450 becomes bus master. On a Read Track Headers operation the DMA bursts will be at the specified throttle. The DMA transfers will continue until all data has been transfered to system memory.

2.5.5.3.7 Incrementing Disk Address

The sector address will be incremented by 1 for each sector read. At the end of a successful command the head address will be incremented by 1. If the resultant head address is greater that maximum head, it will be cleared and the cylinder address will be incremented.

2.5.5.3.8 Completing a Transfer

The 450 will format an entire track if no errors are encountered. When the format is complete the two status bytes will be updated. If AUD is set, the IOPB will be updated and if interrupts are enabled, an interrupt will be generated.

If the transfer ends in a hard error the transfer is stopped, and any chained operations are also terminated. The two status bytes will be updated. If AUD is set, the IOPB will be updated and if interrupts are enabled, an interrupt will be generated.

2.5.5.3.8 Completing a Transfer (continued)

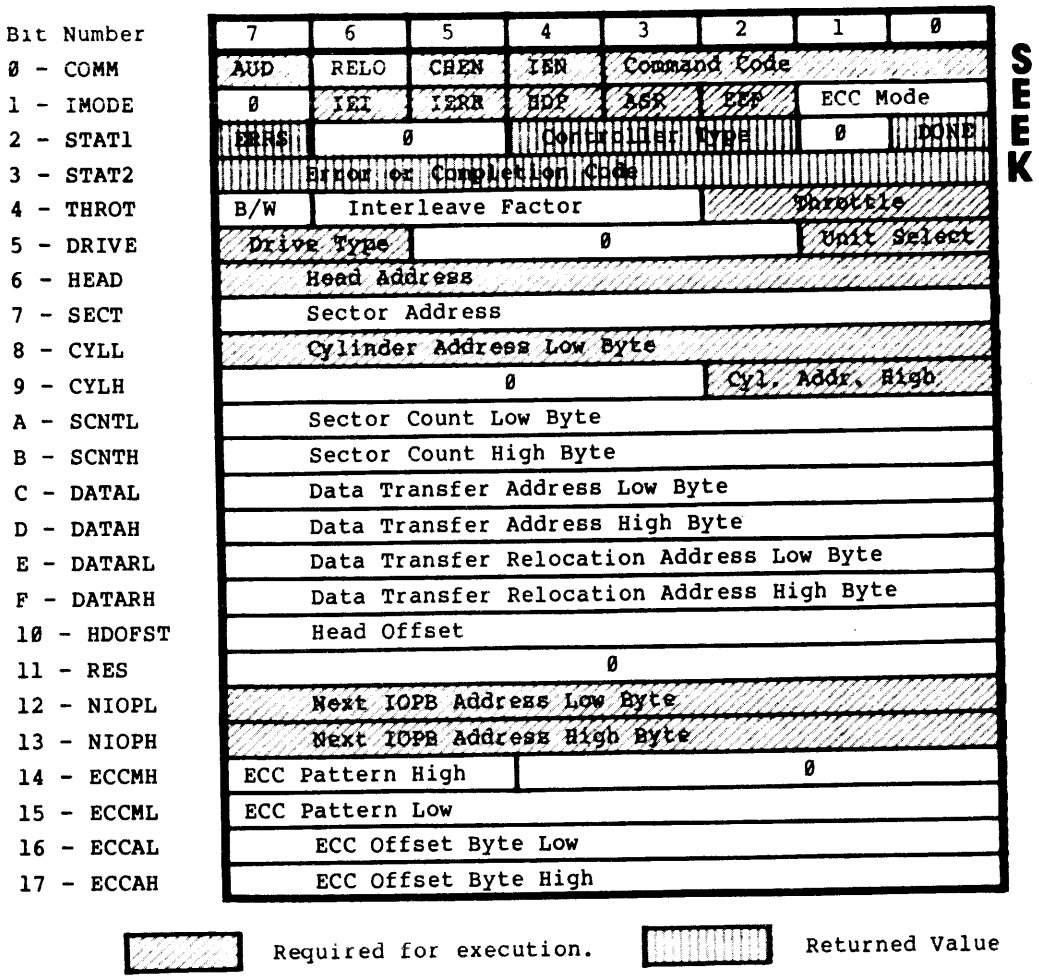
If the transfer ends in a soft error, the transfer has completed, and chained operations will not be terminated. The two status bytes will be updated. If AUD is set, the IOPB will be updated and if interrupts are enabled, an interrupt will be generated.

2.5.6 Seek (Command Code 5)

2.5.6.1 General

The Seek command is used to move the heads of the selected disk drive to the address specified in the IOPB Cylinder Address. This command is used mainly for diagnostic purposes since an implied-seek is inherent in data transfer commands. When IOPBs for different drives are all chained together, overlapped seeking may be initiated.

2.5.6.2 IOPB



2.5.6.3 Detailed Description

A Seek command starts the appropriate seek by sending the cylinder address to the disk drive. The 450 scans the drives to determine when one has completed its seek. After the Seek completes, the associated IOPB is marked as complete. Explicit seek commands will be overlapped like implied seeks if EEF is set.

2.5.7 Drive Clear (Command Code 6)

2.5.7.1 General

A Drive Clear command is used to clear a Drive Fault and return the drive to Cylinder Zero (Return to Zero or Recalibrate).

2.5.7.2 IOPB

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type	0					Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	Head Offset							
11 - RES	0							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High				0			
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

DRIVE RESET

Required for execution. Returned Value

2.5.7.3 Detailed Description

The drive clear command will issue a fault clear command to the disk drive and then issue a recalibrate command. The recalibrate command is a form of seek, therefore the IOPB will complete only when the drive has completed its seek.

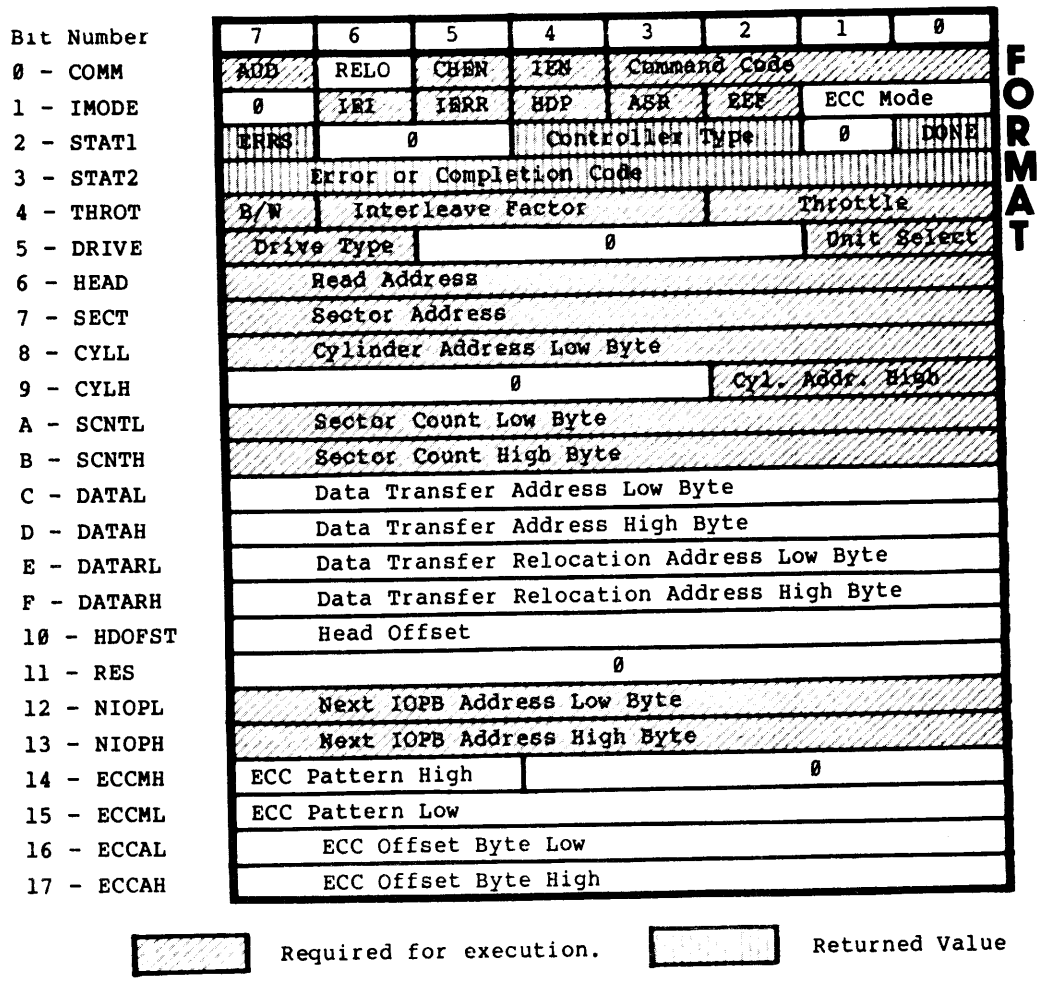
2.5.8 Write Format (Command Code 7)

2.5.8.1 General

The Write Format command is used to format a disk with header information. The 450 writes header information on the disk, crossing sector, head, and cylinder boundaries as required. When the sector count reaches zero, the IOPB is posted as complete.

In order to be able to use the sector slip function, the drive must be configured properly and a Set Drive Size command must have been issued to the 450. (See section 2.5.8.3.1)

2.5.8.2 IOPB



2.5.8.3 Detailed Description

2.5.8.3.1 Allocating Spare Sectors

Determine both the maximum number of sectors per track available on the drive and the number of sectors per track you wish to allocate to be spares. The drive switches should be specified to the maximum number of sectors per track. The drive size set by the Set Drive Size command should be the total number of sectors per track minus the number of sectors allocated as spares.

2.5.8.3.1 Allocating Spare Sectors (continued)

For example if the disk drive will support 34 sectors per track, set the drive sector switches to 34. If you are allocating 2 sectors per track as spares, set the drive size to 32 sectors per track. This automatically allocates 2 sectors as spares.

2.5.8.3.2 Implied Seeks

The 450 will issue an implied seek on a Format command. This seek will be issued as the first operation after reading the IOPB from system memory. If chained operations are implemented and EEF is set, the 450 will scan the remainder of the chain for the possibility of overlap seeks.

2.5.8.3.3 Filling Buffer

When the seek completes, the 450 will access the IOPB to determine the command parameters and begin to fill the buffer. The 450 will fill its own internal buffer for use by the format command. The only DMA activity during a Format command will be that of reading and updating IOPBs.

2.5.8.3.4 Test Track Size

The 450 will determine if the sector count and size is within limits. It does this by timing a track: counting sector pulses and checking the size of the last sector. The 450 performs this as part of the format function once per drive per unit select. The 450 determines if there are spare sectors on each track, and formats them accordingly.

2.5.8.3.5 Sector Coincidence

The 450 will wait for index pulse and then count the appropriate number of sector pulses until the sector to be formatted arrives under the heads. If the disk is to be interleaved, the interleave factor must be specified at format time so that the 450 will format the sectors in the proper sequence.

2.5.8.3.6 Write Header and ECC

After the sector pulse for the requested sector is sensed, the sequencer will count the appropriate number of bytes and then write the sync bits. It then takes the header words out of the FIFO, serializes them, generates a new ECC value, and writes the header to the disk. The ECC value generated for the header words becomes part of the header on the disk.

2.5.8.3.7 Sector Data

The data field portion of the sector will be wriiten by the 450.

2.5.8.3.8 Incrementing Disk Address

The sector address will be incremented by 1. If the sector address is greater than max sector, it will be reset to zero and the head address will be incremented. If the resultant head address is greater than maximum head, then the head address will be reset to zero and the cylinder address will be incremented by one. If the cylinder is greater than max cylinder when the implied seek is issued, an error will be generated.

2.5.8.3.9 Completing a Transfer

The sector count will be decremented by 1 each time the disk passes over a sector boundary while formatting. At the end of the sector, the sector count is tested to determine if the transfer is complete. If the transfer is not complete, the next sector is formatted. If the cylinder address has just been incremented, an implied seek will be issued.

When the transfer is complete, the two status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. If the AUD of the IOPB command byte was set, the IOPB will be updated.

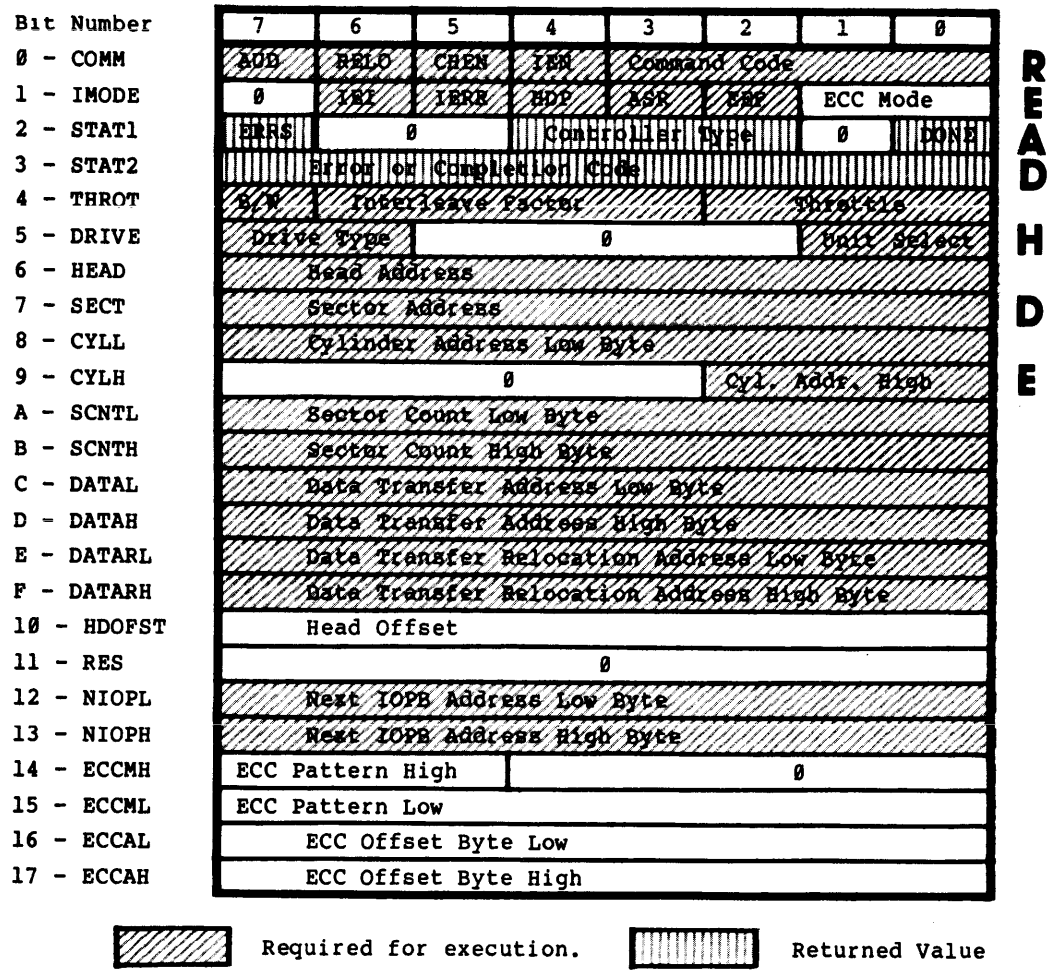
If the transfer ends in a hard error, the transfer is stopped and marked as complete with error. Any chained operations will be halted. The IOPB address and relocation registers will be pointing to the IOPB which caused the error. If the transfer ends with a soft error any chained operations will be continued.

2.5.9 Read Header, Data and ECC (Command Code 8)

2.5.9.1 General

The Read Header, Data and ECC command reads sectors from the disk into the memory locations specified by the Data Address. An additional 8 bytes are read for each sector (see Table 2-7). The interleave factor must be specified in order to read the sectors in the correct sequence from the drive.

2.5.9.2 IOPB



NOTE

The sector address specified in the IOPB is an absolute number, and does not take into consideration any sectors that may have been slipped.

2.5.9.3 Detailed Description

2.5.9.3.1 Implied Seeks

The 450 will issue an implied seek on a Read Header, Data, ECC command. The seek will be issued as the first operation after reading the IOPB from system memory. If chained operations are implemented and EEF is set, the 450 will scan the remainder of the chain for the possibility of overlap seeks.

2.5.9.3.2 Seek End

The 450 will scan the drives to determine when the drive has completed its seek.

2.5.9.3.3 Sector Coincidence

The 450 will wait for index pulse from the drive, count the appropriate number of sector pulses, and read the sector. The interleave factor will have to be specified in the IOPB.

2.5.9.3.4 Read Data

The sequencer will wait for the sync bits for the header field. As the header is read in from the disk it is de-serialized and placed into the FIFO buffer. After 2 header words are read into the FIFO, the sequencer waits for the sync bits for the data field. After synchronizing with the data field, data is read in, deserialized, and put into the FIFO buffer. The last 2 words read are the ECC words from the end of the data field. When data becomes available at the other end of the FIFO, the 450 requests the bus and transfers the data to memory. The 450 will transfer an additional 8 bytes per sector which are the header and ECC fields.

2.5.9.3.5 Throttle

The throttle is the maximum number of transfer that can occur each time the 450 becomes bus master. On a read operation the first DMA requests will be at minimum value since the limiting factor of the burst length is the number of words available from the FIFO. After the initial few DMA bursts, the typical burst length will increase, possibly approaching the throttle limit. Words will continue to be transferred from the controller as required until the sector count overflows and the buffer is empty.

2.5.9.3.6 ECC

ECC is not supported in this command.

2.5.9.3.7 Incrementing Disk Address

The sector address will be incremented by 1 as each sector is read. If the sector address is greater than max sector, it will be reset to zero and the head address will be incremented. If the resultant head address is greater than maximum head, then the head address will be reset to zero and the cylinder address will be incremented by one. If the cylinder is greater than maximum cylinder when the implied seek is issued, an error will be generated.

2.5.9.3.8 Completing a Transfer

At the end of each sector, the sector count is decremented and tested to determine if the transfer is complete. If the transfer is not complete, the next sector is transferred. If the cylinder address has been incremented, an implied seek will be issued.

When the transfer is complete, the status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. If the AUD of the IOPB command byte was set, the IOPB will be updated.

If the transfer ends in a hard error, it is stopped, the two status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. Any chained operations will be halted. The IOPB address and relocation registers will be pointing to the IOPB which caused the error. If AUD was set, the IOPB will be updated.

If the transfer ends with a soft error, the two status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. Any chained operations will be continued. If AUD was set, the IOPB will be updated. The ERR bit in the CSR will not be set since it is a soft error.

Sector Size and Byte Number Within Sector			Description
256 Byte	512 Byte	N Byte	Sector Size
1	1	1	Cylinder Address Low
2	2	2	Cylinder Address High & Sector Address 64/128
3	3	3	Head Number
4	4	4	Sector & Drive Type
5-260	5-517	5-N+4	Sector Data
261-264	517-520	(N+5)-(N+8)	Data ECC

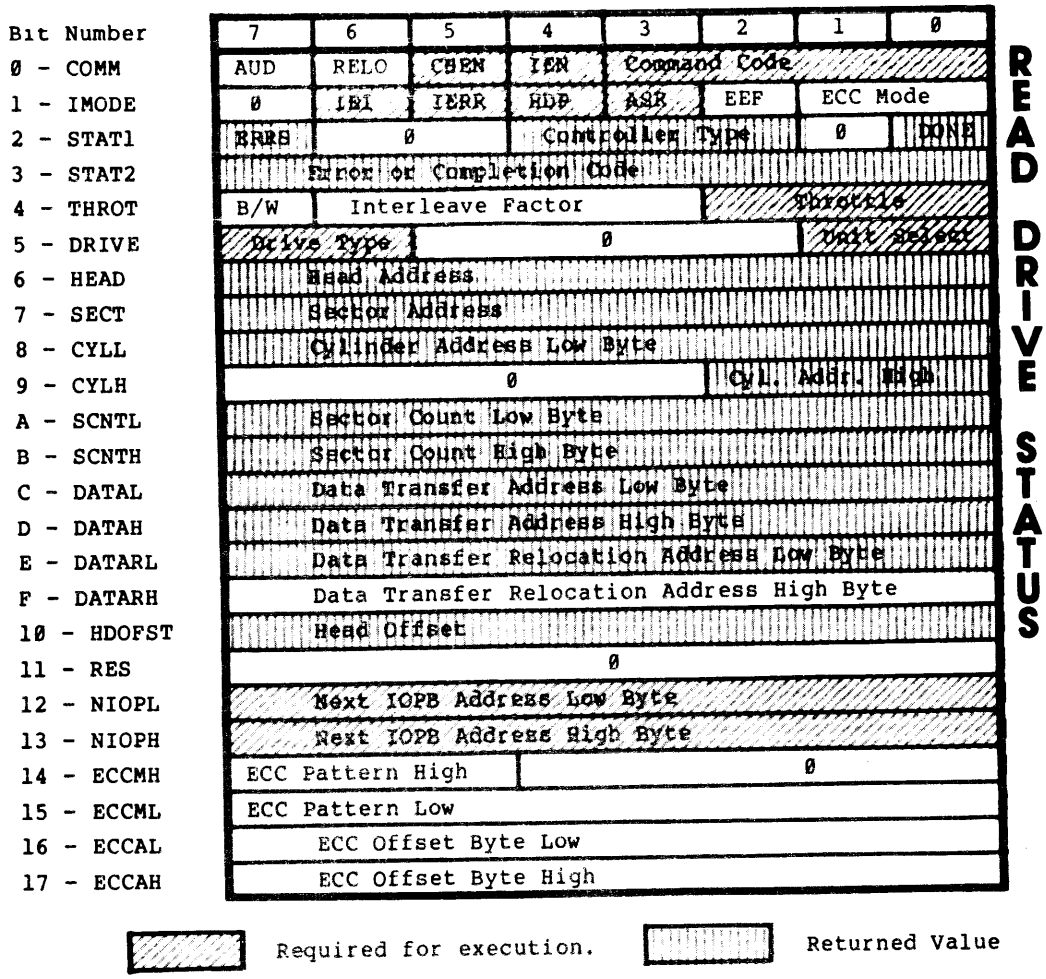
TABLE 2-7. HEADER, DATA, AND ECC BYTES

2.5.10 Read Drive Status (Command Code 9)

2.5.10.1 General

The Read Drive Status command causes the hardware status of the selected drive and drive type to be written to the IOPB.

2.5.10.2 IOPB



2.5.10.3 Detailed Description

This command has 2 purposes: it will show the current size of the drive type specified, and the status of the drive unit specified. The IOPB must contain the drive type and unit number. The returned values will be in bytes 6 through E and 10 of the resultant IOPB. The drive type does not have to correspond to the unit number for the purposes of this command.

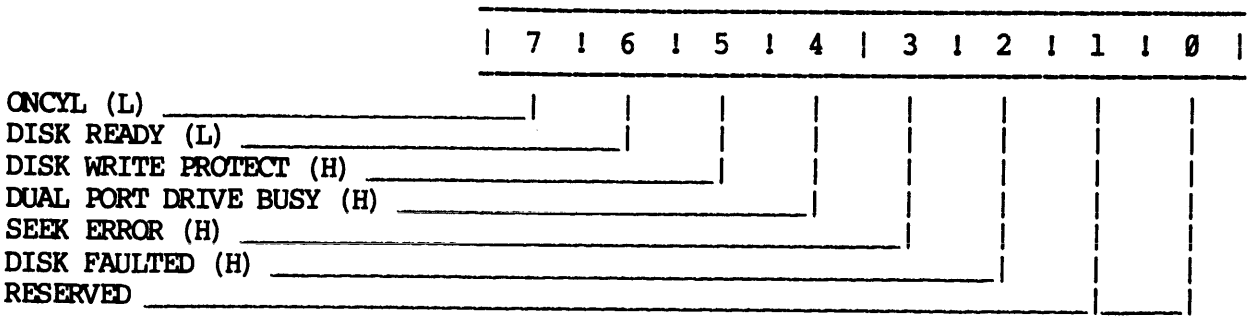
2.5.10.3.1 Returned Values

The following information is returned by executing this command:

Drive Type Specified	450	Selected Drive
Maximum Sector	Code Revision	Drive Status
Maximum Head	Sector Size	Number of Sectors/Track
Maximum Cylinder		
Head Offset		

2.5.10.3.2 Drive Status

The drive is selected, the following information is latched, and the drive is released.



BIT	MNEMONIC	MEANING
7	ONCL	ON CYLINDER(L) - represents the On-Cylinder status of the drive whose drive number is in the Drive byte of this IOPB. If the drive is ready and this bit is zero, this drive is not seeking. If this bit is a one, then the heads of the selected drive are not positioned over the desired cylinder.
6	DRDY	DISK READY(L) - will be zero if there is a drive selected and ready for selected unit.
5	WRPT	DISK WRITE PROTECT(H) - is set when the selected disk is write protected.
4	DPB	DUAL PORT BUSY(H)- if set, indicates that the drive is dual ported and is selected by the other controller. If reset the selected drive is not busy or not ready.
3	SKER	HARD SEEK ERROR(H) - will be set (1) if the selected drive is reporting a Hard Seek Error in its logic.
2	DFLT	DISK FAULT(H) - will be set to a one if the selected drive is reporting any type of Fault in its logic.
Ø,1	-	RESERVED

2.5.10.3.3 Drive Type Parameters

- Maximum Sector
- Maximum Head
- Maximum Cylinder
- Head Offset

The parameters of the drive size will be loaded into bytes 6 through 9 and 10H. The maximum sector value will be in byte 7, the maximum head value will be in byte 6; and the maximum cylinder value will be in bytes 8 and 9. The value for head offset will be in byte 10H. It will normally be Ø for a drive that does not have fixed and removable media.

2.5.10.3.4 450 Parameters

The sector size in bytes per sector, and firmware revision are also available. Byte B contains a revision code where 1=A, 2=B, etc. Bytes C and D contain the number of bytes per sector.

2.5.10.3.5 Drive Parameters

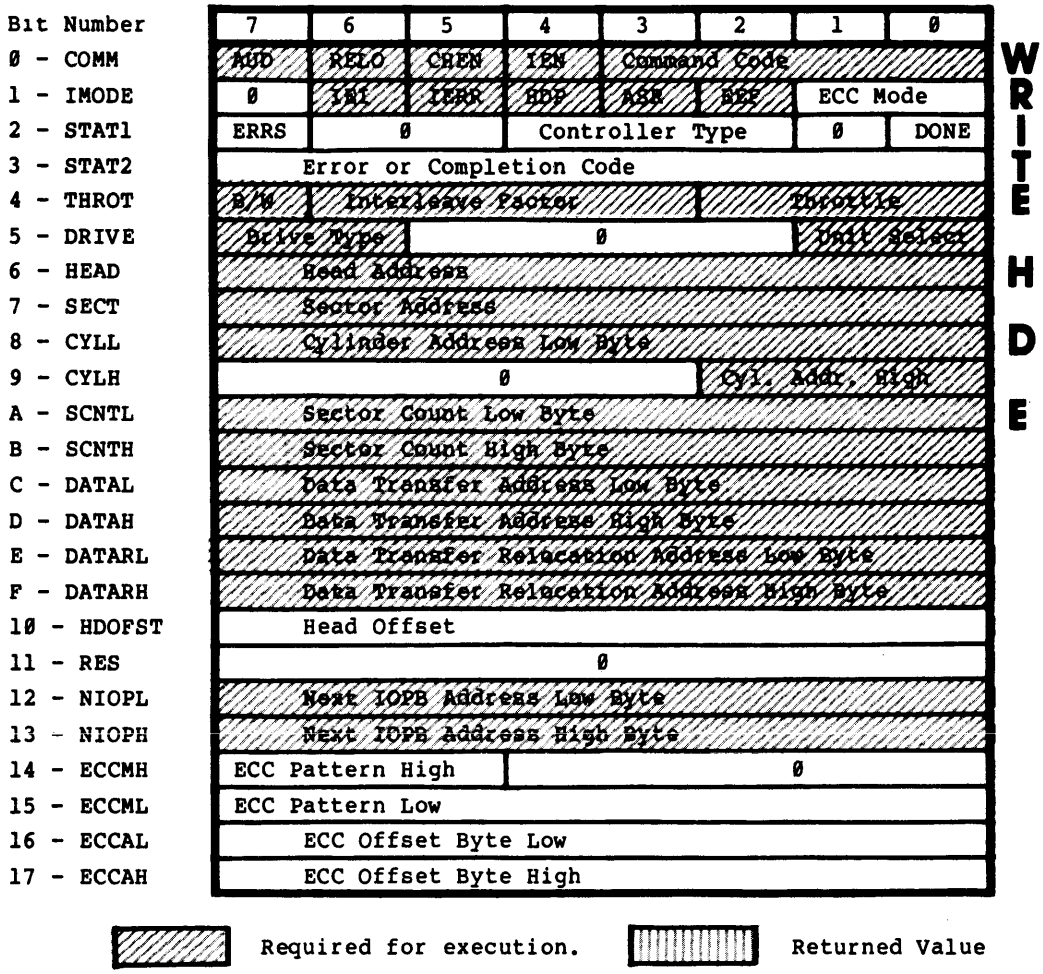
The 450 counts the total number of sectors per track. This number will include all sectors even if one of the sectors is too small (runt sector) to be a data sector. This count will be returned in byte E.

2.5.11 Write Header, Data and ECC (Command Code A)

2.5.11.1 General

This command writes the header, data, and ECC for one or more sectors. The header, data, and ECC are taken from memory as specified by the Data Transfer Address. Eight additional bytes per sector are written on the disk and are in the same order as in Table 2-7. The interleave factor must be specified in order to write sectors in the correct order on the disk.

2.5.11.2 IOPB



NOTE

The sector address specified in the IOPB is an absolute number and does not take into consideration any sectors that have been previously slipped.

2.5.11.3 Detailed Description

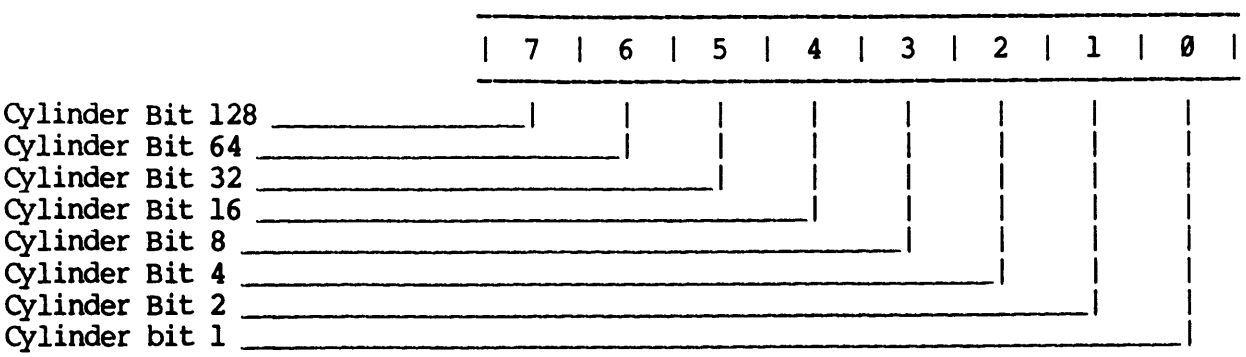
2.5.11.3.1 Data Buffer

Prior to issuing the IOPB for a Write Header, Data, and ECC, a data buffer must be set up in system memory. The first four bytes in the

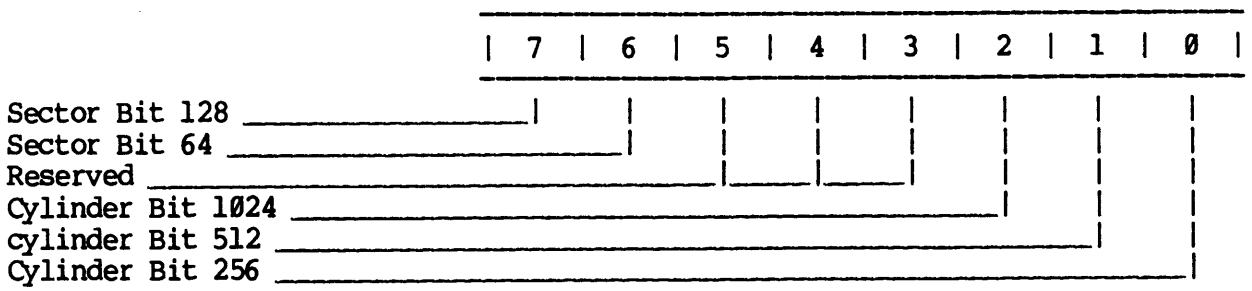
2.5.11.3.1 Data Buffer (continued)

buffer are the header bytes. The following diagrams show the proper layout for these bytes. The next 512 bytes (for 512 byte sectors) are the data to be written on the sector. The last four bytes are the ECC that will be written on the sector.

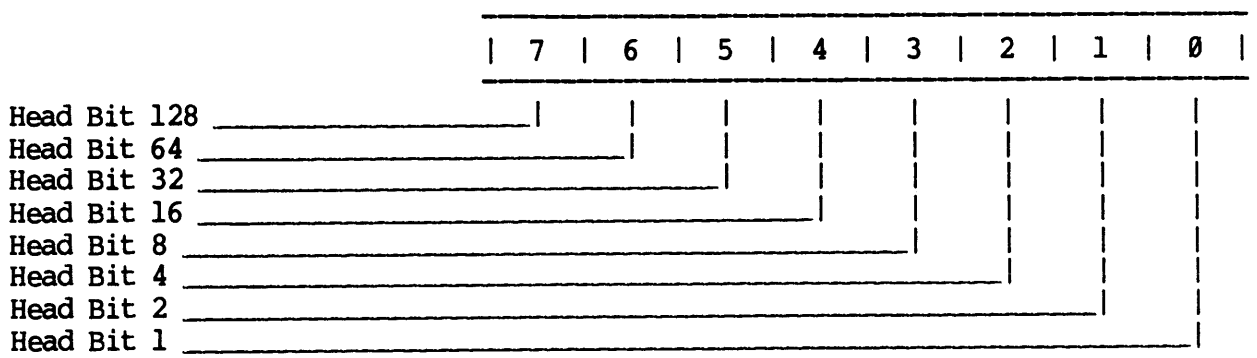
Buffer Byte 0



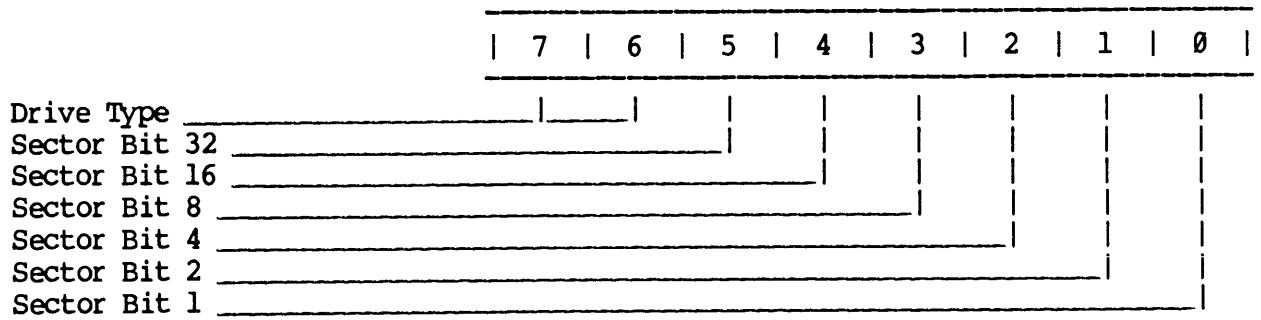
Buffer Byte 1



Buffer Byte 2



Buffer Byte 3



2.5.11.3.2 Implied Seeks

The 450 will issue an implied seek on a Write Header, Data and ECC command. The seek will be issued as the first operation after reading the IOPB from system memory. If chained operations are implemented and EFF is set, the 450 will scan the remainder of the chain for the possibility of overlap seeks.

2.5.11.3.3 Filling Buffer

When the seek is complete, the 450 will access the IOPB to determine the command parameters and begin to fill the buffer. When one sectors worth of data is in the buffer a search for the requested sector will be made. This is done to insure sufficient data is available in the buffer at the start of the write.

2.5.11.3.4 Sector Coincidence

The 450 will wait for index pulse from the drive, count the appropriate number of sector pulses, and write that sector. The interleave factor must be specified in the IOPB.

2.5.11.3.5 Write Data

The sequencer will count the appropriate number of bytes after sector coincidence and then write the sync bits. It will take two words out of the FIFO, serialize them, generate a new ECC value, and write them and the ECC to the disk as the new header. The sequencer will count an appropriate number of bytes and then write the data sync bits. It will take the data from the FIFO, serialize it, and write the data to the disk. As data is removed from the FIFO, it is replaced by the appropriate DMAs from system memory.

2.5.11.3.6 Throttle

The throttle is the maximum number of DMA transfers that can occur each time the 450 becomes bus master. On a write operation the first DMA bursts will be at maximum value until the buffer is full. After words start moving to the disk, the typical burst will be less than the throttle value. Data will continue to be transferred into the controller as required until the sector count overflows.

2.5.11.3.7 ECC

After the data field has been written, the ECC words are taken from the buffer and written to the disk.

2.5.11.3.8 Incrementing Disk Address

The sector address will be incremented by 1. If the sector address is greater than max sector, it will be reset to zero and the head address will be incremented. If the resultant head address is greater than maximum head, the head address will be reset to zero and the cylinder address will be incremented by one. If the cylinder is already at maximum cylinder when the implied seek is issued, an error will be generated.

2.5.11.3.9 Completing a Transfer

The sector count will be decremented by 1 each time the DMA address increments over a sector boundary. At the end of the sector the sector count is tested to determine if the transfer is complete. If the transfer is not complete, the

2.5.11.3.9 Completing a Transfer (continued)

next sector is transferred. If the cylinder address has been incremented, an implied seek will be issued.

If the transfer is complete, the two status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. If AUD of the IOPB command byte was set, the IOPB will be updated.

If the transfer ends in a hard error, the transfer is stopped, the two status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. Any chained operations will be halted. The IOPB address and relocation registers will be pointing to the IOPB which caused the error. If AUD was set, the IOPB will be updated.

If the transfer ends with a soft error, the two status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. Any chained operations will be continued. If AUD was set, the IOPB will be updated.

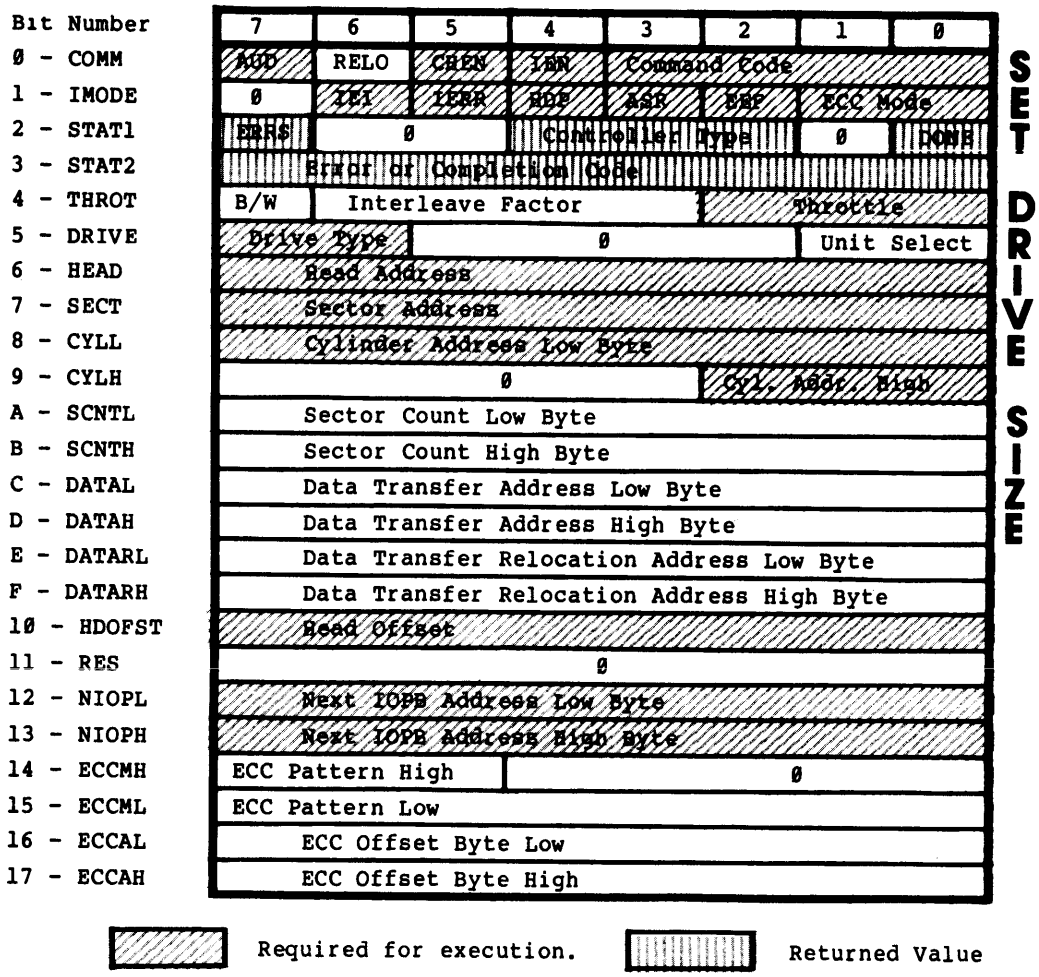
2.5.12 Set Drive Size (Command Code B)

2.5.12.1 General

This command will allow the drive size parameters to be reconfigured. The parameters for the drive type specified in Byte 5 will be modified. The max sector value should be in byte 7, the new max head value should be in byte 6, the new max cylinder value should be in bytes 8 and 9, with 9 being the most significant and the head offset value should be in byte 10H.

Any size parameters modified by this command will be reset to the default values in EPROM by bus init, power-up or the self test command.

2.5.12.2 IOPB



2.5.12.3 Detailed Description

This command allows customizing the 450 to operate with drives of any numbers of sectors, heads and cylinders.

2.5.12.3.1 Disk Sectors Per Track

The IOPB must contain the maximum value minus one of the number of sectors per track. If the disk you are using has 32 sectors per track, the controller will refer to them as sectors 0-31. The number to be entered in byte 7 is 1FH (the hex equivalent of 31).

2.5.12.3.2 Disk Heads per Cylinder

The IOPB must contain the maximum value minus one of the number of heads. If the disk you are using has 19 heads, the controller will refer to them as heads 0-18. The number to be entered in byte 7 is 12H.

If the drive type being specified is for a fixed/removable disk the maximum head value must be set appropriately for the fixed or removable sections. For example, when specifing the CDC 96 MB CMD the drive type that specifies the removable portion of the drive will have a maximum head address of 0, since it only has one head; the drive type that specifies the fixed portion of the disk will have a maximum head address of 4.

2.5.12.3.3 Disk Cylinders

The IOPB must contain the maximum value minus one of the number of cylinders. If the disk you are using has 823 cylinders, the controller will refer to them as cylinders 0-822. The number to be entered in byte 8 is 36H and byte 9 is 3 (336H is the hex equivalent of 822).

2.5.12.3.4 Head Offset

A value for head offset must be specified for fixed/removable drives such as the CMD and Lark. These drives will be specified by having two drive types describe them: one drive type will specify the removable protion of the drive, and the other will specify the fixed portion. The offset value will be a hex number which will be added to the head number in order to select either the fixed or removable portion of the disk. The head offset value for the removable portion of a CMD will be 0, while the head offset value for the fixed portion will be 10H. Refer to the appropriate vendor's manuals to determine the head offset values for the fixed and removable portions of the disk.

2.5.12.3.6 Default Parameters

Upon bus init, power-up, or self test, the size parameters are reset to the default parameters in EPROM. The defaults are described in the following table:

Drive Type	MB	Heads	Cylinder	Sector	Drive
00	300	19	823	32	CDC 9766
01	80	5	823	32	CDC 9762
02	474	20	842	46	Fujitsu 2351
03	*	255	2047	128	(Maximum Config.)

2.5.13 Self Test (Command Code C)

2.5.13.1 General

This command will start the same self test that is run automatically on power-up. If successfully completed, a success status will be reported. If not, the appropriate error status will be reported. This can only be utilized in non-chained mode.

2.5.13.2 IOPB

SELF TEST

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	ATN	RELO	CHEN	GO	Command Code			
1 - IMODE	0	LEI	IMRK	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERR	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	Head Offset							
11 - RES	0							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High			0				
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required for execution. Returned Value

2.5.13.3 Detailed description

This test is the same test performed during the power-up sequence. If the board is not functioning properly the self test LED will not extinquish and possibly the error status will not be returned.

2.5.13.3.1 Processor RAM Test

This test verifies that the RAM internal to the microprocessor and the microprocessor itself are functioning properly. If the RAM fails the memory test, error code 1A (hex) will be returned.

2.5.13.3.2 Header Shift Register Test

This test verifies that the header shift register and the microprocessor serial communication are functioning properly. If this test fails an error code of 1BH is returned.

2.5.13.3.3 Buffer Test

The on-board buffer is tested for faulty memory. A 1CH will be returned on error.

2.5.14 Reserved (Command Code D)

Use of this command will result in an unimplemented command error.

2.5.15 Maintenance Buffer Load (Command E)

2.5.15.1 General

This command is for diagnostic purposes only. It sets an address in the 450 which may later be used during the Maintainance Buffer Dump command. This command will not function properly in chained mode unless only chained to one Buffer Dump IOPB.

2.5.15.2 IOPB

BUFFER LOAD

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	MOD	SFTO	CHN	IEN	Command Code			
1 - IMODE	0	IBI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRS	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	S/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	Head Offset							
11 - RES	0							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High			0				
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required for execution. Returned Value

2.5.16 Maintenance Buffer Dump (Command F)

2.5.16.1 General

This command is for diagnostic purposes only. When issued it will DMA one sector of data from the address specified in The Maintainence Buffer Load command into the FIFO buffer. After the DMA is complete, it will DMA the data from the buffer to the address specified in the IOPB. This command will not function properly in chained mode unless it immediately follows a Buffer Load IOPB and EFF is reset.

2.5.16.2 IOPB

BUFFER DUMP

Bit Number	7	6	5	4	3	2	1	0
0 - COMM	AUD	RELO	CHEN	IEN	Command Code			
1 - IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 - STAT1	ERRB	0		Controller Type			0	DONE
3 - STAT2	Error or Completion Code							
4 - THROT	B/W	Interleave Factor				Throttle		
5 - DRIVE	Drive Type		0				Unit Select	
6 - HEAD	Head Address							
7 - SECT	Sector Address							
8 - CYLL	Cylinder Address Low Byte							
9 - CYLH	0					Cyl. Addr. High		
A - SCNTL	Sector Count Low Byte							
B - SCNTH	Sector Count High Byte							
C - DATAL	Data Transfer Address Low Byte							
D - DATAH	Data Transfer Address High Byte							
E - DATARL	Data Transfer Relocation Address Low Byte							
F - DATARH	Data Transfer Relocation Address High Byte							
10 - HDOFST	Head Offset							
11 - RES	0							
12 - NIOPL	Next IOPB Address Low Byte							
13 - NIOPH	Next IOPB Address High Byte							
14 - ECCMH	ECC Pattern High				0			
15 - ECCML	ECC Pattern Low							
16 - ECCAL	ECC Offset Byte Low							
17 - ECCAH	ECC Offset Byte High							

Required for execution. Returned Value

2.6 HOW TO PROGRAM THE 450

This section of the manual deals with preferred methods of programming the 450 Disk Controller. In the following, it is assumed that interrupts are enabled. If they are not, obviously the 450 will not interrupt. Thus ignore the sentences about interrupting if they are not enabled in your situation.

2.6.1 IOPB Processing With No Command Chaining

- o Set up IOPB

  Allocate a 24 byte long segment of memory to build an IOPB. Set the various bytes in this IOPB as required to perform a function. See Section 2.4

- o Point 450 to IOPB

  Write the address of this IOPB into the 450 IOPB address registers.

- o Set Go

  Write an 80H which is GBSY into the CSR register. This effectively starts the operation. The host processor should either poll the CSR for done, or wait for the interrupt.

- o The 450 Processing

  The 450 starts to process the IOPB after it detects that GBSY has been written into its Control and Status Register. It uses the Address and Relocation Registers to address Multibus memory and read the IOPB. It executes the function and when complete will update the status bytes of the IOPB, reset GBSY, and interrupt.

- o Check for Errors

  You should read both the CSR, and status byte 1 to determine if the command completed without error. You must test the CSR to determine if the DERR is set, since this may mean that status byte 1 was not updated. If DERR isn't set, check status byte 1 and determine if the general error bit (bit 7) is set, if not the command completed succesfully.

  The completion code of a command will appear in status byte 2. A code of 0 indicates successful completion, while anything else indicates an error. Error codes are fully explained in section 2.4.4. Depending upon the error, you may want to try to recover from the error and retry the command. See Section 2.6.3

2.6.2 IOPB Processing with Command Chaining Enabled

The 450 supports IOPB chaining so that many IOPBs may be queued and executed as fast as possible. The chain starts with the IOPB pointed to by the IOPB Address Registers and follows the address pointers in each IOPB to the next IOPB. The 450 will complete all IOPBs or stop the chain when a hard error is detected. If EEF is set the 450 scans the chain to try to do as much in parallel as possible, the commands may not be executed in the order in which they were chained.

2.6.2.1 The Chain

Each IOPB has a field which points to the next IOPB in the chain. The 450 does not look at the chain pointer unless CHEN in the command byte is set. The Next IOPB address bytes are relocated using the IOPB relocation registers, therefore all IOPBs in a chain must be located within the 64KB memory block starting at the base address in the IOPB relocation register.

2.6.2.2 Executing the Chain

Each time the 450 is started or after each Attention Request, the controller will scan the IOPB list for incomplete IOPB requests for disks which are not busy. The first unprocessed request for a non-busy disk will be analysed and if it is a seek, read, or write command, a seek will be initiated to move the heads to the correct cylinder. This will happen for as many drives as possible.

When each drive reaches the desired cylinder the requested data transfer for that drive will be initiated. Seek commands will be complete at this point. If EEF is set, IOPBs are completed in the order in which their seeks completed.

2.6.2.3 Completing IOPBs

As each IOPB is completed, the status bytes in the IOPB are updated to indicate DONE with the completion code. If the IEI is set, the 450 will interrupt as it completes each IOPB. An interrupt is acknowledged by writing a "1" into the Interrupt Pending Bit in the CSR. The Interrupt Pending and/or Error bits must not be reset with a Controller Reset, as this may cause drive faults and misposition errors upon continuing the chain.

The 450 will remain busy until either the chain is complete, or a hard error occurs. If the 450 completes all IOPBs while there is an active attention acknowledge, reseting AREQ will cause GBSY to set.

2.6.2.4 Modifying the Chain During Execution

There are two bits in the 450 Controller Status Register, Attention Request and Attention Request Acknowledge, used in the 450's Attention Request Protocol. System software should set the Attention Request bit (AREQ) to notify the 450 that it wishes to add or remove IOPBs from the queue. When the 450 has noticed this request it will set Attention Request Acknowledge (AACK) in the Controller Status Register and if IEI is set, an interrupt will occur.

System software may now remove IOPBs which have been marked as complete and may add new IOPBs to the queue. IOPBs which were queued previously but are not marked complete may <u>not</u> be touched except to modify CHEN and Next IOPB address. The 450 will continue to process commands which were given to it even though it has had its chain interrupted.

When system software has completed adding or removing IOPBs, it should clear (AREQ) and the 450 will clear (AACK). The 450 will rescan the entire queue at this time to look for additional IOPBs.

2.6.2.5 Chain Interrupts

The 450 supports a mode of interrupting that will provide an interrupt at the end of each IOPB. An interrupt may occur due to one IOPB being complete, or that several may be complete and AACK has been granted. One interrupt will occur and it is up to the software to determine why the interrupt occurred, and if it occurred for multiple interrupt requests. If 3 IOPBs complete at the same time only one interrupt will be provided. The 450 assumes that any complete IOPB at the time of setting GBSY or IPND or the time of resetting AREQ has ben taken care of by the software.

2.6.2.6 Completing a Chain

When all IOPBs in a chain have been completed, the Chain is complete. If one IOPB had a hard error, the chain completes with an error. If interrupts are enabled, an interrupt will occur.

2.6.3 Error Recovery

Some errors may be recovered by appropriate procedures. The procedures will vary depending upon the type of errror encountered. The errors are shown below and are grouped according to the recommended recovery procedure.

2.6.3.1 Errors 01,03,07,0A,15,17,19,1A,1B,1C, and 20

01	Interrupt Pending
03	Busy Conflict
07	Illegal Cylinder Address
0A	Illegal Sector Address
15	Unimplemented Command
17	Sector Count Zero
19	Illegal Sector Size
1A	Self Test A
1B	Self Test B
1C	Self Test C
20	Illegal Head Address

These errors are either programming errors or hard failures and should not be retried in a normal software driver. For further explanation see Section 2.4 of this manual.

2.6.3.2 Errors 04,05,06,16 and 19

04	Operation time Out
05	Header Not Found
06	Hard ECC Error
16	Drive Not Ready

These errors may be recovered by retrying the operation. Two retries should be executed and if the error persists the error is unrecoverable.

2.6.3.3 Errors 12,18, and 25

12	Cylinder & Head Header Error
18	Drive Faulted
25	Hard Seek Error

2.6.3.3 Errors 05, 18, and 25 (continued)

These errors indicate that the drive may have gone off cylinder. The retry proceedure is to issue a Drive Clear and then retry the transfer. This can be accomplished automatically be setting the ASR bit in byte 1.

2.6.3.4 Errors 09 and 0E

09	Sector Slip Command Error
0E	Slave ACK Error

Check the parameters issued, correct them, and try again. You have either run out of spare sectors on the track or have accessed non-existant memory.

2.6.3.5 Errors 0D and 13

0D	Last Sector Too Small
13	Illegal Sector Size

These errors occur during format and indicate that the drive may be configured for an improper number of sectors. Verify the sector switches on the drive and the drive size for this drive type.

2.6.3.6 Errors 14 and 1F

14	Write Protect Error
1F	Soft ECC Recovered Error

These errors are for information purposes only and may be logged by the operating system.

2.6.3.7 Error 1E

1E	Soft ECC Error

This error indicates that an ECC recoverable error has occured the software may correct this as follows:

For a byte-oriented system, e.g., 8080 or 8085, the following procedure is used.

1. Reserve 24 bits of storage for the ECC mask (3 bytes). Initialize to zero.

2. Take the mask word from IOPB, reverse the bit order of the word, and save the result in the least significant 16 bits of the storage allocated in step 1.

3. Get the bit address word from the IOPB and subtract 1. Since the bit address always starts at 1, this will cause the start to be at bit 0.

4. Shift the stored mask left using the least significant 3 bits of the adjusted bit address from step 3 as a count. These 3 bits are the starting bit number within the byte.

2.6.3.8 Error 1E (continued)

5. Divide the bit address by 8 by performing 3 logical shifts to the right. The result is the byte offset into the data where the stored mask is to be XOR ed with the data. Add this to the address of the start of the BAD sector to create a pointer to the first data byte to be corrected.

6. Exclusive or the data bytes in ascending order with the 3 mask bytes using the least significant mask byte first.

For word-oriented systems the procedure differs:

1. Reserve 32-bits of storage for the ECC mask (2 words). Initialize to zero.

2. Reverse the bit order of the ECC mask word and save the result in the least significant word of the two-word mask storage allocated in step 1.

3. Get the ECC bit address from the IOPB and subtract 1 to cause the bit count to start at 0 rather than at 1.

4. Shift the stored address mask bits left using the four low order bits of the adjusted ECC address of Step 3 as a count.

5. Divide the bit address by 16 by performing 4 logical shifts to the right. The result is the word offset into the BAD sector. Adding this offset to the start of sector memory address creates a pointer to the first word to be corrected.

6. Exclusive or two consecutive words in the data with the mask.

2.6.4 Formatting and Sector Slip

The following is a brief description of the steps to perform when formatting a disk.

2.6.4.1 Set Drive Size Parameters

Set the number of sectors per track in the drive size parameters equal to the number of sectors in an entire track. Do not subtract the number of sectors to use as spares for sector slip later on.

2.6.4.2 Format

Format the disk and verify the data. You may want to use several different patterns to be sure you have found all the media defects. As the disk is being verified, build a table in the program of all the media defects encountered.

2.6.4.3 Media Defects

Disk drives can produce a soft error in about 1 out of every 10^{10} transfers. A sector is not bad if it fails with a soft error once. Rewrite the pattern and read the sector up to ten times or until a second error occurs. If only one error occurs, it is not defective and there is no need to slip it. If a second error occurs, add the sector to the bad sector table and indicate if the error was a bad header, hard ECC, or soft ECC.

2.6.4.4 Reset Drive Size Parameters

Set the drive size parameters equal to the number of data sectors desired. The number should be the number of physical sectors the drive can hold minus the number of spare (slip) sectors desired and the runt sector if it exists.

2.6.4.5 Reformat the Disk

Use the format command to reformat the entire disk. This proceedure will format all spare sectors to have a header of DDDDH, DDDDH. If the runt sector exists, it will be formatted with a header of EEEEH, EEEEH.

2.6.4.6 Slip Defective Sectors

Using the procedure in section 2.6.5 slip the defective sectors and mark all defective sectors as bad.

2.6.5 Slip a Sector

This section contains the simple procedure used to slip sectors.

2.6.5.1 Read Track Headers

A buffer in system memory must be allocated to store the sector header information during this procedure. The buffer length in bytes must be four times the total number of sectors. Issue a Read Track Headers command for the track that contains the sector(s) to be slipped.

2.6.5.2 Record Bad and Spare Sectors

Determine which sectors have been allocated as spares, and which are bad. Build a table in memory with two variables, one being the physical sector number from psuedo index, and the other being the status of that sector (good - bad - spare). The following example shows the data buffer contents after a Read Track Headers.

Data	Physical Sector	Logical Sector	Status
36H,03H,04H,40H	1	0	good
36H,03H,04H,41H	2	1	good
36H,03H,04H,42H	3	2	good
36H,03H,04H,43H	4	3	good
EEH,EEH,EEH,EEH	5	-	bad
36H,03H,04H,44H	6	4	good
: : : :	:	:	good
: : : :	:	:	good
36H,03H,04H,5FH	33	31	good
DDH,DDH,DDH,DDH	34	-	spare

A table constructed for the example above would consist of sectors 1-4 good, 5 bad, 6-33 good, and 34 as a spare.

2.6.5.3 Spare Sector Available

Determine if enough spare sectors are available. For every sector to be slipped, there must be a spare available.

2.6.5.4 Determine sector to be slipped

Determine which sector will be slipped. First determine the absolute sector number in relation to psuedo index. Add it to the number of bad sectors that exist between psuedo index and the sector to be slipped. The absolute sector number will equal the logical sector number if the interleaving is 1:1 and there are no defective sectors.

The absolute sector number must be adjusted by the interleaving factor if the sectors are not contiguous. The interleaving can be determined by the following BASIC program. It will provide a vector of interleaved sector numbers such that A(physical)=interleaved.

```
10 REM INTERLEAVING PROGRAM FOR 450 CONTROLLER
20 DIM A(200)
30 REM N = TOTAL NUMBER OF SECTORS PER TRACK
40 N = 32
50 REM I = INTERLEAVING FACTOR I:1
60 I = 2
70 I9 = ((N-1)/I)+1 \ REM I9 = INTERVAL
80 I9 = INT(I9)
90 R = N - ((I9-1)*I) \ REM R = REMAINDER
100 P = 0 \ REM P = PHYSICAL SECTOR
110 I8 = I9 \ REM I8 = INTERVAL COUNT
120 R8 = R \ REM R8 = REMAINDER COUNT
130 B = 0 \ REM STARTING VALUE OF LAST SECTION
140 L = 0 \ REM LAST SECTOR NUMBER
150 A(0) = 0 \ REM FIRST SECTOR MAPPED TO 0
160 P = P + 1
170 IF P > (N-1) THEN 290 \ REM END OF TRACK EXIT
180 L = L + I8
190 R8 = R8 - 1
200 IF R8 <> 0 THEN 220
210 I8 = I8 - 1
220 IF L <= (N-1) THEN 280
230 B = B + 1
240 L = B
250 R8 = R
260 I8 = I9
270 A(P) = L
280 GOTO 160
290 STOP
```

For example upon reading a track interleaved 2:1, the sectors are arranged as follows:

```
0, 16, 1, 17, EEEE, 2, 18, 3, 19, 4, 20, 5, 21, 6, 22, 7, 23, 8,
24, 9, 25, 10, 26, 11, 27, 12, 28, 13, 29, 14, 30, 15, 31, DDDD
```

The table described in section 2.6.5.2 should list sectors 1-4 good, 5 bad, 6-33 good, and 34 as a spare sector. Logical sector 4 has been determined to be defective. The absolute sector number as determined from the algorithym is 9. There is 1 defective sector between psuedo index and the sector to be slipped, therefore the physical sector to be slipped is sector 10. The table with its new entry should be: 1-4 good, 5 bad, 6-9 good, 10 bad, 11-33 good, and 34 as spare.

2.6.5.4 Slip Sectors

Using the table updated in section 2.6.5.3 and the vector generated in 2.6.5.4 modify the buffer in preparation for the Write Track Headers. Start at the beginning of the buffer to set up the header for the first sector. The following procedure will outline the steps used to modify the buffer.

1. Get physical sector number to be modified.

2. Multiply this number by four bytes, add it to the buffer start address to determine where that sector's header begins.

3. Determine if this sector is to be good, bad, or a spare sector. If bad the four header bytes should be EEH, EEH, EEH, EEH. If spare the header bytes should be DDH, DDH, DDH, DDH. If this sector is to be usable the first byte should be the LSB cylinder, the next byte the MSB cylinder, the next byte the head, and the last byte the new sector number ORed with the Drive Type code. See section 2.5.11.3.1.

4. Determine the new sector number using the interleave algorithym, the physical sector number, and the number of bad sectors encountered so far. Take the physical sector number and subtract the number of bad sectors found between it and index. Use this number to determine the new sector number which will be ORed with the Drive Type and placed into the buffer.

5. Continue setting up the buffer for each physical sector on that track. Use the procedure outlined above to determine how to set up each sector.

NOTE

The physical locations of bad sectors must not be moved with relation to psuedo index. The media defects do not move when slipping sectors, and therefore any physical sector marked bad must remain bad.

2.6.5.5 Write Track Headers

The modified header can now be written to the disk to reformat the track with slipped sectors. Once reformated the defective sectors are invisible to the operating system through normal Read and Write commands. When using Read or Write Header - Data - ECC, defective sectors as well as good sectors can be accessed.

2.6.5.6 Sector Slip With Live Data

If the disk has live data, the following procedure should allow you to slip a sector and not lose the data on the disk. This procedure will require a full track buffer, and therefore it is recommended that this be accomplished using a stand-alone program.

1. Allocate a full track buffer in memory and read a track into memory. Use ECC mode 2 which corrects the bad data if possible.

   - OR -

   If a full track buffer is not available in memory, allocate disk space, and store the data in that space.

2.6.5.6 Sector Slip with Live Data (continued)

2. Using the Sector Slip procedure, slip the sector with the error in it.

3. Now use a normal write command to write the data from the buffer back onto the disk. The 450 will take care of the fact that a sector has been slipped.

2.6.6 Dual Port Drive Operation

Dual ported drives require the operating system to be more careful in its use of disk space. Other considerations include the possibility that one of the controllers will not release the drive, preventing the other controller gaining access.

2.6.6.1 Drive Space Allocation

Dual ported drives can be written on by two different controllers. When an operating system is allocating space on the disk it is unaware that the other controller may be allocating the same sectors. This can cause two files to trash each other. When using dual ported drives it is a good idea to allow only one controller to ever write on the disk. If this is impractical then only allow one controller to allocate the space on the disk and the other to write into only the allocated space.

2.6.6.2 Failure to Gain Access

Occasionally a controller will fail to gain access to a dual ported drive. In this case the operation will time out after waiting 2 seconds after the other IOPBs are complete. The error will cause the chain to terminate and the operating system can remove any IOPBs for that drive.

2.7 PERFORMANCE CONSIDERATIONS

This section deals with how to get the most from the 450. It discusses the various tradeoffs and their advantages and disadvantages. Using the following information, you should be able to get the best performance possible for YOUR application.

2.7.1 Throttle Considerations

From the 450 disk controller's viewpoint, the throttle value should be as high as possible so that the controller will never have to skip revolutions or get data lates. However, you may have some other real time application that must get to the bus periodically.

In these applications:

- determine the maximum time that the 450 can be bus master (less time then another unit can be without the bus);
- determine the response time of your memory, add 500 nsec. and divide into the allowable 450 bus master time. The number you come up with is the maximum throttle value;
- pick the closest number from the 450 throttle values without going over the actual amount.

2.7.1.1 High Throttle Advantages

- o Maximum disk throughput with minimum missed revolutions.
- o Maximum bus throughput with minimum bus overhead.

2.7.1.2 High Throttle Disadvantages

- o Tendency to "hog" the bus - time critical devices fail.
- o Other DMA units may not get enough bus time.

2.7.2 Word or Byte Mode

Word mode is definitely more efficient on the bus. It takes the same length of time to transfer a word in word mode as it does a byte in byte mode. Using word mode therefore effectivly doubles the throughput of the 450.

2.7.2.1 Word Mode Advantages

- o Increased throughput with less bus utilization.
- o Helps DMA keep up with disk.

2.7.2.2 Word Mode Diasadvantages

- o Works only on word oriented memory.

2.7.3 Transfers on Address Boundaries

The 450 will react differently to transfers on various address boundaries. Word mode transfers on odd addresses obviously must compensate for the odd address. The internal architecture of the 450 dictates how transfers across page boundaries are handled.

2.7.3.1 Word Mode on Odd Boundary

If a word mode transfer begins on an odd address, the 450 compensates by mixing word and byte mode. It will do the first transfer in byte mode, the remaining transfers in word mode, and complete the transfer with the final byte in byte mode. The disadvantage is that the on-board microprocessor must get involved with the transfers more often when starting a word mode transfer on an odd byte. This added involvement requires more time during a transfer and reduces the margin for keeping up with the disk. The extra time involved by the microprocessor does not result in any extra bus time except for one extra bus cycle for the last byte.

2.7.3.2 Transfers to Page Addresses

Each time the 450 crosses a 256 byte address boundary, the onboard microprocessor must update the upper address bits and restart the DMA sequencer. It is more efficient to align transfers on address boundaries so that this occurs the minimum number of times. It is only advantageous if you require the absolute maximum throughput from the 450.

2.7.4 Interleaving

Interleaving can be used to increase throughput on either a fully loaded system or one where the operating system response time is slow. It does so by effectivly cutting the disk speed in half for 2:1, or a third for 3:1 interleaving etc.

2.7.4.1 Advantages of Interleaving

- Maximum throughput on fully loaded systems.

  Fully loaded systems usually have many DMA devices contending for bus time. In this environment the 450 may fall behind the disk, and will stop the transfer and wait a revolution until the next sector arrives under the head. This will really slow the disk subsystem. If the disk was interleaved, the data rate is much slower, and therefore the 450s bus requirements are much lower.

- Maximum throughput on slow software systems.

  Slow software systems cannot turn around interrupts in a reasonable amount of time, and usually transfer one sector at a time. In this environment interleaving can allow the system to catch many sectors per revolution instead of just one on a non-interleaved disk.

- Less chance of missing revolutions.

2.7.4.2 Disadvantages of interleaving

Slows data throughput from the disk by the interleave factor.

2.7.5 Chaining Operations

Chaining will have an effect on the performance of your system and will result in several performance advantages:

The 450 will automatically perform overlap seeking, which will have a dramatic performance throughput increase for multidrive systems.

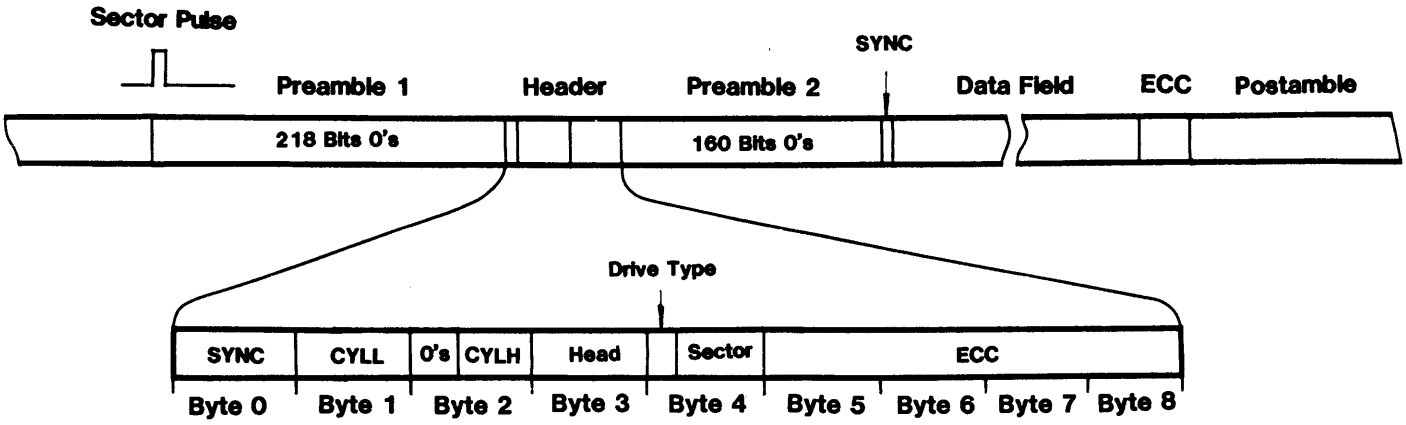
The operating system does not have to respond as rapidly at the end of a command; the 450 will continue to the next command without any operating system intervention. The 450 will allow interrupts at the end of each IOPB and notify the system that the IOPB is complete.

2.8 MEDIA FORMAT

The 450 has two different meadia formats which it supports. 440 Compatible format is used for media compatiblity with the 440 disk controller. The 450 standard format is more efficient in its use of disk space, and is required for use with the new faster SMD+ drives.

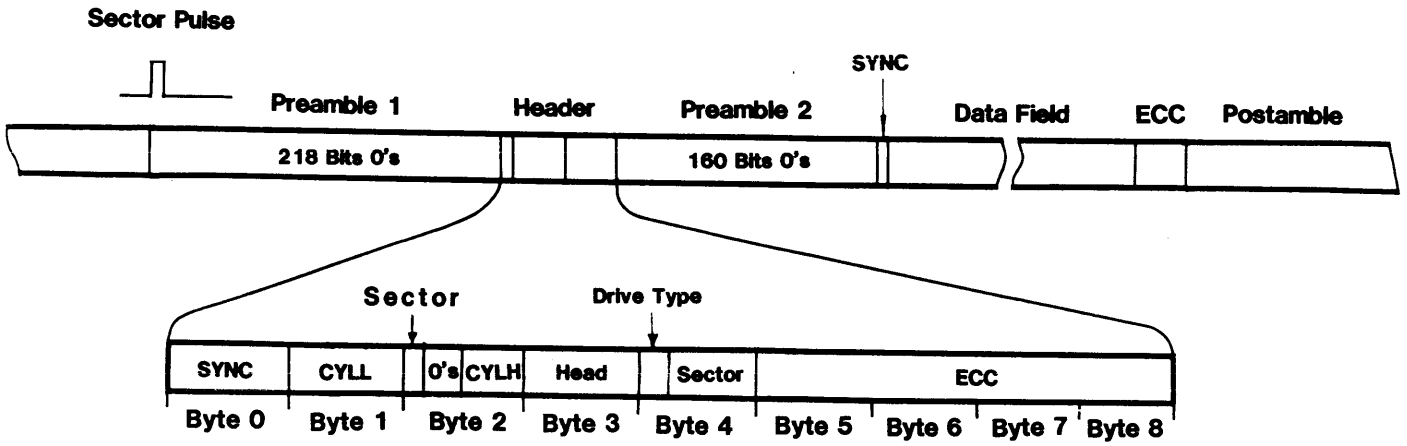
2.8.1 440 Compatible Format

This format is 440 compatible. The figures below show the actual format on the media, and an enlarged view of the header area.



440 Format

Figure 2-2 440 Compatible Format



450 Format

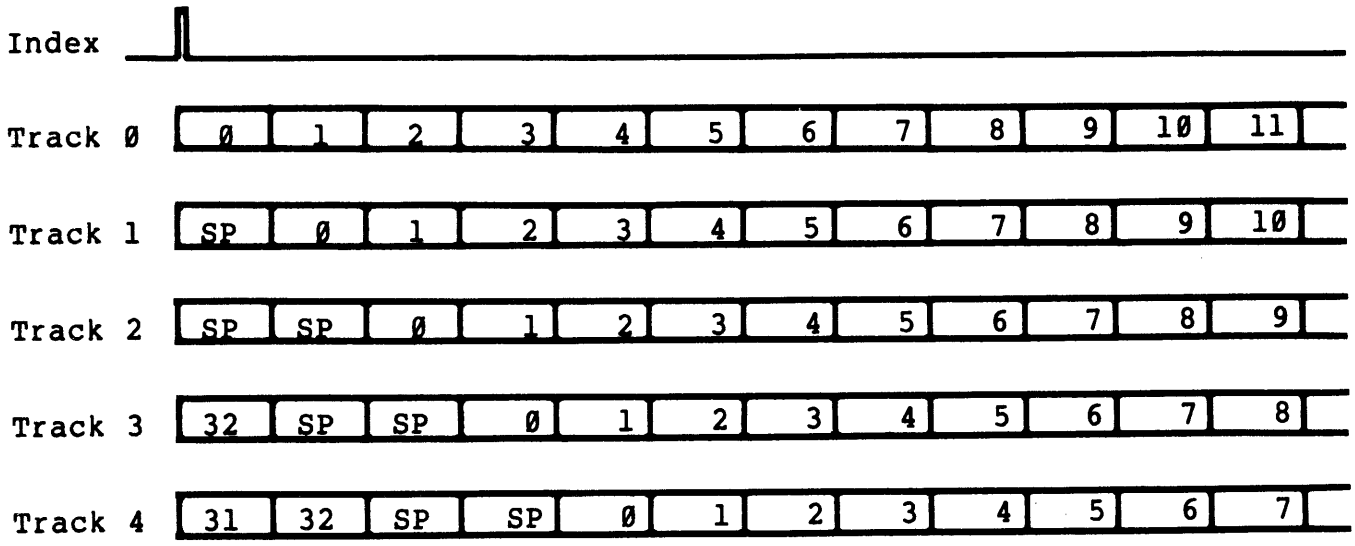
Figure 2-3 450 Standard Format

2.8.2 450 Standard Format

This format is more efficient in it's use of disk space, therefore allowing more sectors per track than the compatible format. Figures 2.3 descibes its actual format and layout of the header bytes.

2.8.3 Adaptive Format

The 450 format mode uses adaptive format. The adaptive format causes logical sector zero to slip one sector from physical index for each track. The logical to physical relationship is reset to 1:1 on track 0 of each cylinder. This feature allows the 450 to store more data per track since the head switching time is masked by the adaptive slip. The following figure shows the relationship between Index and the logical sector mapping. This figure is of a 32 sectored disk with 2 spare sectors.



2.9 SAMPLE PROGRAMS

2.9.1 Sample Listing for 8080 Processors

The following program will give the address of the IOPB at 120H to the controller, set GBSY, wait for done, and halt.

```
100   AF                XRA    A       ;Clear Accumulator
101   D3 40             OUT    IRELL   ;Clear Relocation Register
103   D3 41             OUT    IRELH
105   3E 20             MVI    A,20H   ;Low byte of IOPB address
107   D3 42             OUT    IADRL   ;send to IOPB address register
109   3E 01             MVI    A,01H   ;High byte of IOPB address
10B   D3 43             OUT    IADRH
10D   3E 80             MVI    A,GBSY  ;Set GBSY
10F   D3 44             OUT    CSR     ;Tell controller to GO
111   DB 44       LOOP: IN     CSR     ;Get status
113   E6 80             ANI    GBSY    ;Test for done
115   C2 11 01          JNZ    LOOP    ;No - Wait
118   76                HLT            ;Yes - Stop
```

2.9.1 Sample Listing for 8080 Processors (continued)

```
                        ORG     120H    ;IOPB

120   82                DB      AUD!READ        ;Read with auto update
121   0A                DB      ASR!EMOD2       ;Auto seek retry and ECC mode 2
122   00 00             DB      0,0             ;Not done
124   05                DB      THRT5!WRD       ;Word mode and throttle of 64
125   40                DB      DT1!UN0         :Drive Type and Unit Sel.
126   00 00 00 00       DB      0,0,0,0         ;Disk address 0
12A   01 00             DW      1               ;Sector count
12C   00 00             DW      0               :Data relocation
12E   00 10             DW      1000H           ;Data address
```

SECTION 3 INSTALLATION AND CHECKOUT

3.0 GENERAL

The following section describes the procedures used to unpack, configure, install, and checkout your 450.

3.1 UNPACKING AND INSPECTION

3.1.1 Inspect Shipping Carton

Inspect the shipping carton for possible shipping damage. Carefully unpack the 450 from its carton and save the carton and other shipping material for possible later use.

If you determine that there has been shipping damage, do not unpack the unit. Notify Xylogics and the freight carrier immediately.

3.1.2 Contents

There is a 450, single printed circuit board. Optional items which may be included are drive cables, a manual and/or software on a floppy diskette.

If any items are missing or damaged please contact Xylogics at one of the following telephone numbers:

United States 617-272-8140 International 44-753-78921
United Kingdom Slough 78921 West Germany 49-6196-47004

3.1.3 Inspect the 450

Inspect the 450 for socketed parts that may have become loosened during shipment. Assure that all parts are firmly seated in their sockets. If any parts must be reinserted, observe proper orientation.

3.2 CONFIGURING THE 450

The 450 has several jumper options which can be configured by the customer. These options are described in the following paragraphs. Refer to figure 3-1 for a board layout.

3.2.1 Base Address Selection

There are two separate parts to selecting the base address. The first is selecting response to 8 or 16 bit register addresses. This is controlled by the jumper JA10-JB10.

JA10-JB10 installed = 8 bit address
removed = 16 bit address

The actual base address is controlled by jumpers JA/JB 2-9, JE4-JE5, and JC/JD/JR 1-4. If 8 bit addressing is selected, the jumpers for address bits 0-7 are the only valid jumpers, and jumpers for bits 8-F are ignored. Table 3-1 shows how to set the staples for commonly used base addresses.

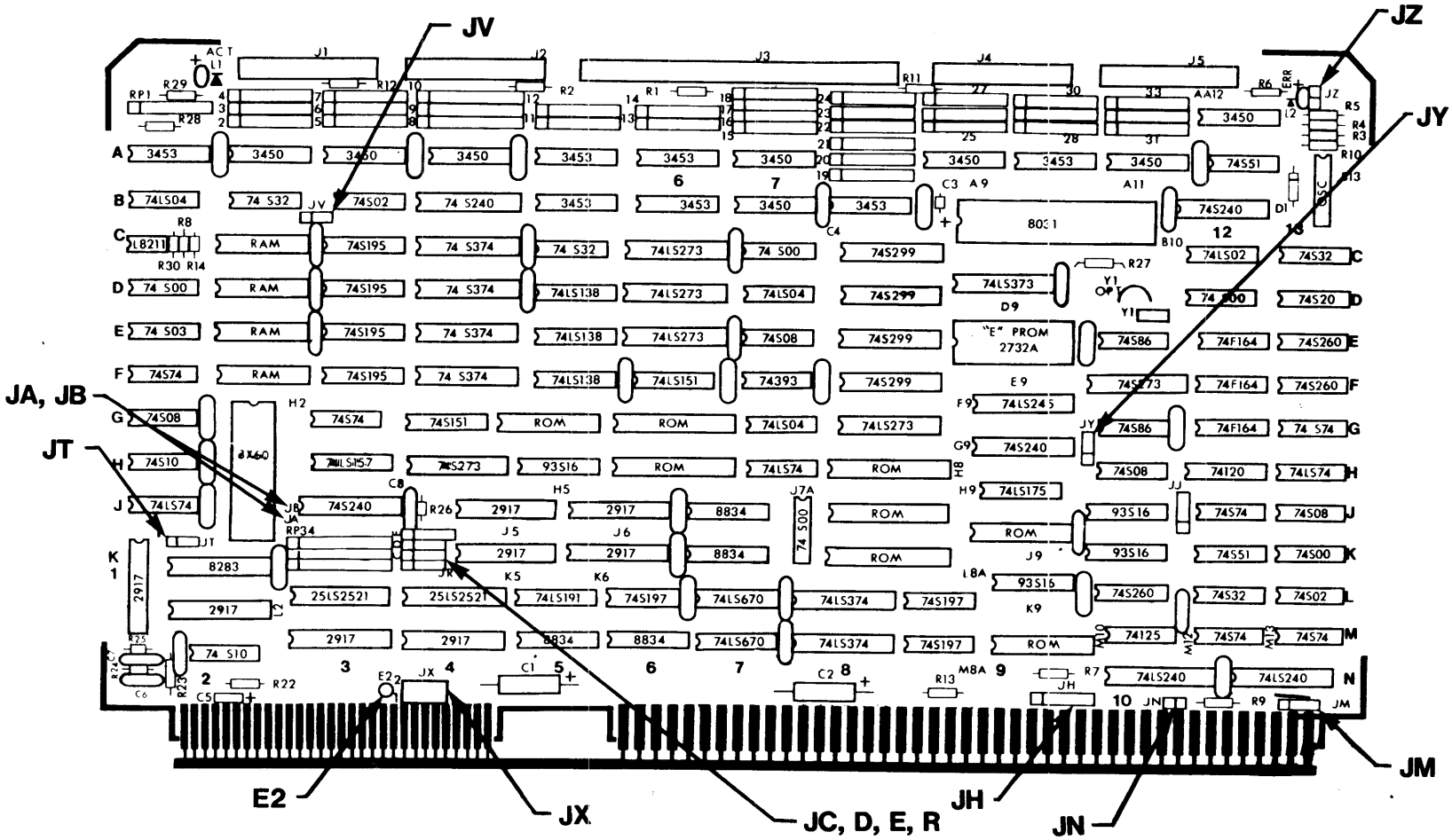


Figure 3-1 The 450 Controller

Figure 3-1 The 450 Controller

3.2.1 Base Address Selection (continued)

Figure 3-2 and Table 3-1 are to be used in configuring the base address to your needs. The jumpers are divied into three groups, jumper blocks JA and JB control address bits 8 - F, jumper blocks JR, JC, and JD control address bits 3 - 6, and jumper JE4-JE5 controls address bit 7.

Address bits 8 - F are controlled by inserting or removing a jumper between jumper blocks JA and JB. A jumper present relates to a Ø on that address line, and conversely no jumper relates to a 1. The jumper would be installed between similar pin numbers of each block, for example if address bit D is to be a Ø, then a jumper must connect JA pin 6 to JB pin 6.

Address bit 7 is treated the same as bits 8 - F, except that the jumper connection involved is JE pin 4 to JE pin 5.

Address bits 3 - 6 are controlled by three jumper blocks JC, JR, and JD. A Ø on the address line is determined by connecting between block JR and JC. A 1 on the address line is determined by connecting between block JC and JD. If address bit 3 were to be a Ø then a jumper must be installed between JR pin 4 and JC pin 4. If address bit 4 were to be a 1, then a jumper must be installed between JC pin 3 and JD pin 3.

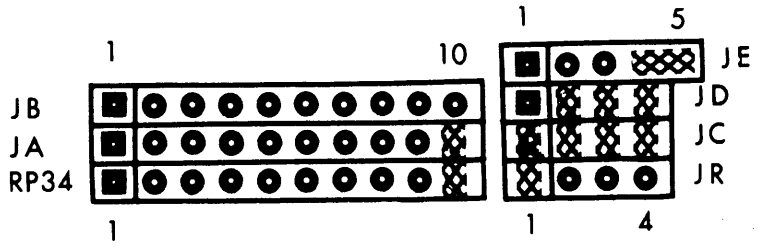


Figure 3-2

Address Bit:	F	E	D	C	B	A	9	8	7	6	5	4	3	8/16
Pin Numbers:														
Jumper JR/JC/JD										1	2	3	4	
Jumper JE4-JE5									X					
Jumper JA/JB	2	4	6	8	9	7	5	3						10
Address:														
40 - 8 bit	X	X	X	X	X	X	X	X	I	RC	CD	CD	CD	I
EE40 - 16 bit	0	0	0	I	0	0	0	I	I	RC	CD	CD	CD	0
50 - 8 bit	X	X	X	X	X	X	X	X	I	RC	CD	RC	CD	I
0050 - 16 bit	I	I	I	I	I	I	I	I	I	RC	CD	RC	CD	0

Where O = out, I = in, and X = don't care, RC = Jumper from JR to JC, and CD = Jumper from JC to JD.

Table 3-1

3.2.2 20/24 Bit Address Relocation

The 450 can function in backplanes of 16, 20, and 24 bit addresses. The 20 bit or 24 bit mode must be selected via jumpers. The 16 bit mode is software selectable. The status of the jumper can be determined by reading bit 3 of the CSR, if set this indicates that the board is jumpered for 24 bit address mode. Both 20 and 24 bit modes support 16 bit addressing.

Mode	JM1-JM2	JM3-JM4
16/20	Out	In
16/24	In	Out

3.2.3 Interrupt Request Levels

Any one of 8 interrupt request levels can be chosen. The 450 is supplied from the factory jumpered INT5/. The selection is performed by connecting a jumper per table 3-2.

Interrupt Request Level	Pin to	Pin
INT0/	E2	JX2
INT1/	E2	JX7
INT2/	E2	JX4
INT3/	E2	JX5
INT4/	E2	JX8
INT5/	E2	JX3
INT6/	E2	JX6
INT7/	E2	JX1

Table 3-2

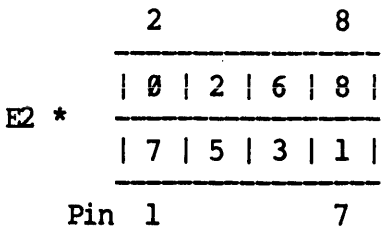


Figure 3-3
Interrupt Level vs. Location on JX Connector

3.2.4 Disable BPRO/

If the 450 is to be used in parallel DMA arbitration (see Section 3.3.2.2) the BPRO/ signal must be isolated from the multibus. This can be accomplished by removing the jumper from JE1-JE2.

3.2.5 Power Fail Protection

Some multibus systems require power fail protection. This is implemented by installing jumper JH1-JH2 and providing an appropriate power fail signal on pin

18 of the P2 connector. This signal should go to ground when the AC powersource has failed. Using an AC power fail indicator versus DC will allow the 450 more time to protect the drive from accidental spiral writes.

3.2.6 Remote Activity Indicator

An LED is provided on-board to indicate when the controller is busy. An activity indicator signal can also be provided to the backplane; install jumper JN1-JN2 and wire the remote LED between +5 volts and pin 42 of connector P2.

3.2.7 Factory Use

There are several jumpers on the 450 which should not be changed since they are for factory use only. Most of these jumpers are hard wired, and not jumper strips.

Jumper	Status	and description
JY2-JY3	In	Closes ECC feedback loop
JY1-JY2	Out	
JJ1-JJ2	Out	Selects Clock for disk sequencer
JJ3-JJ4	In	
JH5-JH6	In	Selects clock for DMA sequencer
JH3-JH4	Out	
JZ1-JZ2	In	Enables crystal clock

	Standard (2KB)	Optional (8KB)
JT1-JT2	Out	In
JT2-JT3	In	Out
JV2-JV3	In	Out
JV1-JV2	Out	In

3.2.8 Firmware and Sector Size

The sector size and format type are controlled by parameters contained in PROM. The following information is provided to ensure that your 450 was properly configured at the factory.

PROMS for Various Configurations

Order Number	Part Number 180-001-xxx Loc. J8	Loc. J9	Bytes/Sector	Buffer Size	Format
900-450-904	954	956	512	2 KB	450
900-450-900	961	962	512	2 KB	440
900-450-905	963	964	512	8 KB	450
900-450-901	965	966	512	8 KB	440
900-450-908	975	976	1024	2 KB	450
900-450-909	977	978	1024	8 KB	450

3.2.8 Firmware and Sector Size (continued)

PROMS / PALS Not Modified

Location	Part Number	
M9	181-001-003	PAL
H8	180-001-953	Disk Sequencer
K8	180-001-955	
E9	180-001-952	EPROM
G5	180-001-949	DMA Sequencer
G6	180-001-950	
H6	180-001-951	

3.3 PREPARING THE COMPUTER SYSTEM

Several steps must be followed in preparing your computer system to accept the 450 controller. A multibus slot must be provided in the backplane for the 450, the slot must be capable of handling a bus master, and the power source must handle the power consumption of the entire system, including the 450.

3.3.1 Card Cage Slot

The card cage must have a slot available for the 450. Placement of the 450 in the DMA priority chain may be critical and thus may affect which slot is chosen.

3.3.2 DMA Bus Arbitration

The 450 can use either serial or parallel DMA arbitration. Serial arbitration is much easier to implement but has restrictions on the number of bus masters it can arbitrate. Parallel bus arbitration is more difficult to implement but is more versitile and can handle more bus masters.

3.3.2.1 Serial DMA Priority

Serial priority is implemented by connecting the BPR0/ and BPRN/ lines in a serial fashion as shown in figure 3-4. The highest priority is the first slot must have its BPRN/ line grounded. The next highest priority is the next slot. To become bus master a unit must have its BPRN/ line asserted. If a unit is not currently a bus master, it passes the state of the BPRN/ to the BPRO/. If the unit is bus master, it de-asserts its BPRO/ so that the following units will not have BPRN/ asserted and therefore cannot become bus master.

3.3.2.2 Parallel DMA Priority

Parallel priority uses the same connections to each board, and connects them to a circuit similar to that of figure 3-5. This external circuit does the bus arbitration. Since BPRN/ of one board is usually connected to BPRN/ of the next the circuit shown in figure 3-4 will have two output tied together. This can be corrected by disabling BPRO/ from each board. Please see section 3.2.4. In the parallel scheme BREQ/ is utilized to request the bus.

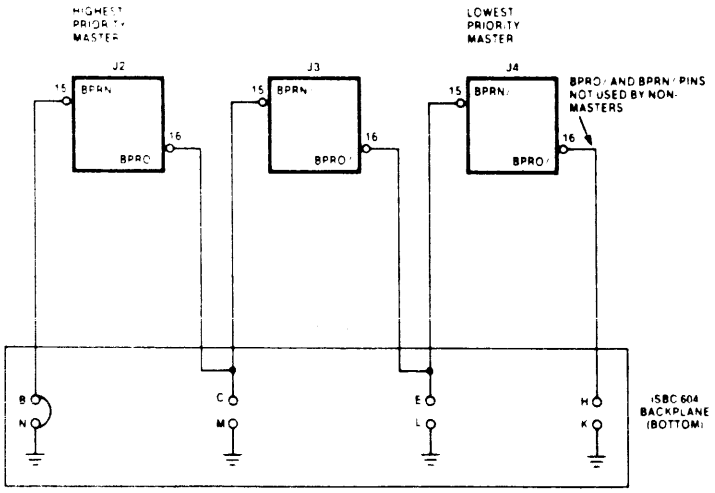


Figure 3-4

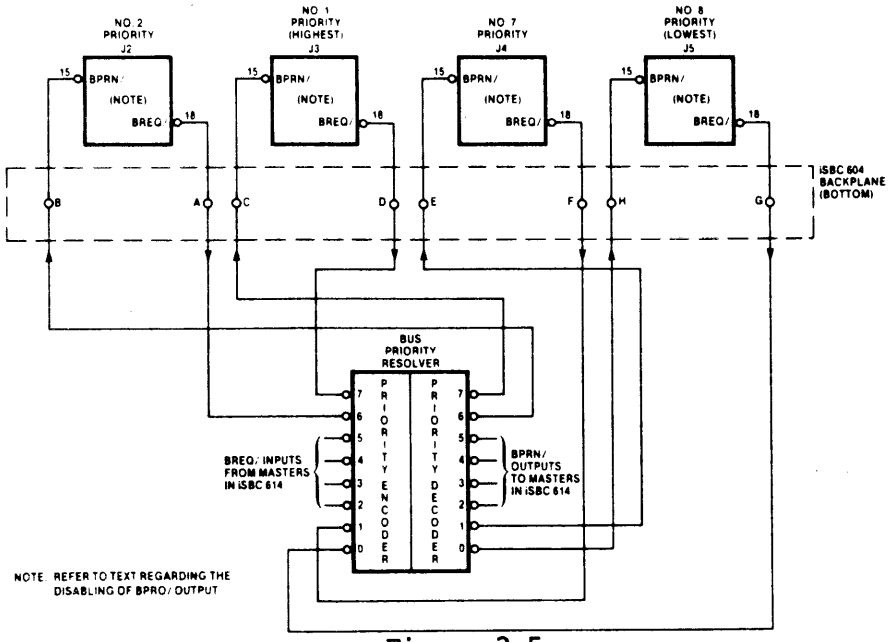


Figure 3-5

3.3.3 Power Considerations

The 450 uses -5 volts to power the differential drivers/receivers for the SMD interface, this helps keep heat producing components off the controller board and allows the user to put them in a more appropriate location.

The 450 will affect the power consumption of the entire computer system. Be sure that the power supplies are adequate to handle the entire power load and readjust the voltages AFTER the 450 has been plugged in. A power supply that is just adequate may cause intermittant and unusual problems due to noise generated by occasionally going into overcurrent protection.

Limits: 5 volts 4.75 to 5.25 volts, -5 volts -4.75 to 5.25 volts.

3.4 DISK DRIVE PREPARATION

The disk drive must be unpacked and prepared to use with the 450. Inspect the shipping container of the disk for any shipping damage and if any, notify the carrier immediately. Unpack the drive and remove any shipping constraints.

Configure the drive for use by the 450. This will entail setting up several parameters such as unit select, number of sectors, and ensuring that sector and index are provided on the A cable. Consult the drive manual for the exact method of configuring your drive.

3.4.1 Drive Unit Select

Unit select is usually set by either a plug on the front of the drive or switches on one of the circuit cards. The 450 can access drives addressed in the 0 to 3 range. The first drive connected should be set to Unit 0. This will satisfy the requirements of the test portion of this section.

3.4.2 Number of Sectors per Track

The number of sectors per track can usually be selected by switches on one of the circuit cards internal to the disk drive. The number of sectors per track can be determined by Table 3-3.

The 450 supports two different disk formats: one is 440 compatible and one is the 450 standard format. The 440 compatible format uses 67 bytes of overhead plus 30 microseconds which it needs for head switching time. The 450 standard format uses 67 bytes of overhead only and is more efficient since it does not require the head switching time. Table 3-4 indicates the switch settings for popularly used sectoring on the Control Data Corporation 9762 disk drive.

NOTE

> Caution must be used when selecting the number of sectors per track in the 450 standard mode. The drive specification for write gate deasserting to read gate asserting must be met. This specification is 12 microseconds for the Fujitsu 2351 and typically 10us for standard SMD drives. Read gate is asserted by the 450 eight bytes after a sector pulse. Write gate is deasserted by the 450 7 bytes after the ECC word.

If the sector slip feature is being used, the number of sectors available to the program is the number of allocated sectors less the spares. See section 2.5.5 for more information on the sector slip command.

The actual setting of the drive switches may be different than the number of data sectors required. Most disk drives will have a runt sector, that is a very small sector at the end of the disk. The 450 must have all sectors formatted, and somtimes the runt sector is too small to format. This will result in error 19H and can be remedied by resetting the sector switches in the drive. If the last sector is too small to be a data sector, but you have included it in the max sector value, then you will also get error 19H. For example hte Fujitsu 2351 can have 46 data sectors per track. Setting the drive switches to 46 results in the last sector having 575 bytes which is too small to be a data sector. If the drive is set to 47 sectors, all sectors are large enough to be formatted, and 46 sectors are large enough to be data sectors.

3.4.2 Number of Sectors per Track (continued)

Data Bytes Per sector	256	512	256	512	1024
Media Compatiblity	440	440	450	450	450
Minimum Bytes / Sector*			323	579	1091
Bytes/track - Bit Cell					
13,440 - 155 nsec.	N/A	22	41	23	12
20,160 - 103 nsec.	60	32	60	33	18
20,480 - 102 nsec.	60	32	60	34	18
20,480 - 123 nsec.	60	33	63	35	18
28,160 - 66 nsec.	N/A	N/A	86	46	25

Table 3-3
Maximum Number of Sectors per Track

* Not including the write gate to read gate delay required

Switch Setting for CDC 976X sector Switches

Switch		0	1	2	3	4	5	6	7	8	9	10	11
Sectors	32	O	O	+	+	+	O	+	O	O	+	+	+
	33	+	O	O	+	O	+	+	O	O	+	+	+
	60	O	O	O	O	O	+	O	O	+	+	+	+
	64	O	+	+	+	O	+	O	O	+	+	+	+

Where O = Closed and + = Open

Table 3-4

3.4.3 Sector and Index Pulses

Sector and index pulses can be provided on either the "A" (Control) cable or the "B" (radial) cable. Drives are usually provided from the disk vendor with sector and index on the A cable. The 450 requires that sector and index to be on the A cable.

3.4.4 Disable Tag 4 and Tag 5

Some disk drives use the spare interface lines for maintenance functions. Other disk drives use the spare interface lines for extended cylinder bits. The 450 was designed to utilize the extra lines as cylinder address. Therefore the disk drive must be configured to disable Tag 4 and 5.

3.5 INSTALL AND CABLE THE 450

In sections 3.1 through 3.4, we configured the controller and drive in preparation for the installation. In this section the controller will be installed and cabled.

3.5.1 Install the 450

Place the 450 into the computer cardcage being sure that it is facing in the proper direction and that it is firmly seated. Be careful not to dislodge any socketed ICs.

3.5.2.3 Mechanical Restraint

At this time be sure that both the A and B cable are mechanically restrained at both ends to prevent the cables from accidentally disconnecting

3.5.2.4 Disk Drive Grounds

Install a ground braid wire between the ground terminal on the disk drive(s) and the computer system ground. This will complete the cabling. Refer to figure 3-6.

3.6 INITIAL TESTS

This section relys upon the operator's familiarity with the monitor of the computer system.

3.6.1 Power up and Self Test

The initial test is the self test indicated by the LED upon power up. This LED should go on for a brief period and then go off. If it remains on, the board is not functioning properly and Xylogics Product Support should be contacted for further help.

NOTE

Check the power supply voltages to insure that they are within limits. (4.75 to 5.25 volts)

3.6.2 Drive Ready

Spin the drive up and wait until you get a ready status from the drive. Read the Reset Register. This will reset the controller, select drive Ø and test the drive ready status. Then read the CSR which will show the results of the drive ready test. The CSR should contain ØlH.

If bit Ø is not set, re-check the drive cable connections and try again. If you still are unable to get the proper status, check the -5V supply on the Multibus. If the problem still occurs check the disk drive for functionality with an offline tester.

3.7 DIAGNOSTICS

Now you should run the diagnostics. Section 4 describes how to use the diagnostics while this section gives a brief description of the recommended order.

- First format the disk. This can be accomplished with either the diagnostic or a formatter program.
- After the disk is formatted, run a full pass of the diagnostics.
- Cable any additional drives and test them. See section 3.8.

3.8 CABLING MULTIPLE DRIVES

If multiple drives are to be used, the A cables and B cables must be properly connected.

3.8.1 Terminator

The terminator must be removed from the drive currently connected to the controller. The terminator must be installed in the last drive in the chain. Refer to figure 3-6.

3.8.2 A (Daisy Chain Cable)

An A cable must be inserted into the "out" connector of one drive to the "in" connector on the next drive. The total length of the A cable is limited to a maximum of 100 feet. Thus if the cable from the controller to the first drive is 30' and the cables between the first and second drive and second and third drive are 30' each, then the total length is 90' which is just under the maximum allowable. Refer to Figure 3-6.

3.8.3 B Cable (Radial Cable)

The B cables will be connected directly from each drive to a B cable port on the 450. A "B" cable may be up to 50 feet long. Refer to section 3.5.2.2.

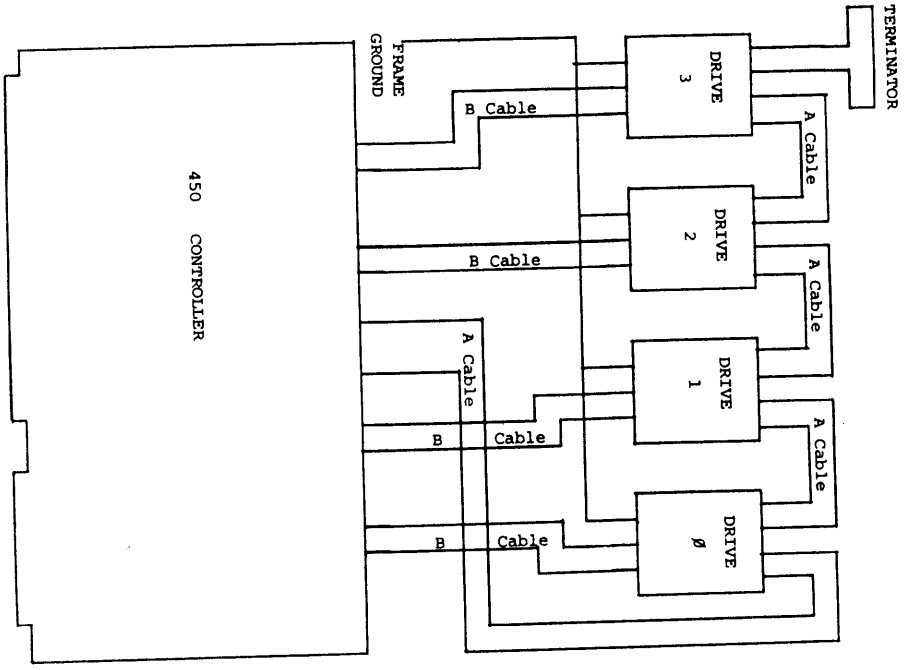


Figure 3-6

3.8.3 Unit Select

When multiple drives are connected, be sure to change the unit select numbers for each drive so that they are unique and no drive has a unit number greater than 3.

3.9 IMPLEMENT OPERATING SYSTEM

The subsystem has been completely tested at this point. Consult your operating system manuals on how to incorporate it into your system.

TO BE SUPPLIED

SECTION 5 MAINTAINENCE AIDS

5.0 GENERAL

The following information is provided for use in installing and maintaining your 450.

5.1 MULTIBUS INTERFACE SIGNALS

Mnemonic	Conn.	Pin	Used by 450	Description
ADR0/	P1	57	Y	
ADR1/	P1	58	Y	
ADR2/	P1	55	Y	
ADR3/	P1	56	Y	
ADR4/	P1	53	Y	
ADR5/	P1	54	Y	
ADR6/	P1	51	Y	
ADR7/	P1	52	Y	
ADR8/	P1	49	Y	
ADR9/	P1	50	Y	
ADRA/	P1	47	Y	
ADRB/	P1	48	Y	
ADRC/	P1	45	Y	
ADRD/	P1	46	Y	Address Bus
ADRE/	P1	43	Y	
ADRF/	P1	44	Y	
ADR10/	P1	28	Y	
ADR11/	P1	30	Y	
ADR12/	P1	32	Y	
ADR13/	P1	34	Y	
ADR14/	P2	57	Y	
ADR15/	P2	58	Y	
ADR16/	P2	55	Y	
ADR17/	P2	56	Y	
DAT0/	P1	73	Y	
DAT1/	P1	74	Y	
DAT2/	P1	71	Y	
DAT3/	P1	72	Y	
DAT4/	P1	69	Y	
DAT5/	P1	70	Y	
DAT6/	P1	67	Y	
DAT7/	P1	68	Y	
DAT8/	P1	65	Y	Data Bus
DAT9/	P1	66	Y	
DATA/	P1	63	Y	
DATB/	P1	64	Y	
DATC/	P1	61	Y	
DATD/	P1	62	Y	
DATE/	P1	59	Y	
DATF/	P1	60	Y	

Mnemonic	Conn.	Pin	Used by 450	Description
STROBE				
IORC/	P1	21	Y	I/O Read Cmd
IOWC/	P1	22	Y	I/O Write Cmd
MRDC/	P1	19	Y	Mem Read Cmd
MWTC/	P1	20	Y	Mem Write Cmd
XACK/	P1	23	Y	XFER Acknowledge
CLOCKS				
BCLK/	P1	13	Y	Bus Clock
CCLK/	P1	31		Constant Clk
PLC/	P2	31	N	Power Line Clock
INTERRUPTS				
INT0/	P1	41	P	
INT1/	P1	42	P	
INT2/	P1	39	P	
INT3/	P1	40	P	
INT4/	P1	37	P	Interrupt Request Levels
INT5/	P1	38	P	
INT6/	P1	35	P	
INT7/	P1	36	P	
INTA/	P1	33	Y	Intr Acknowledge
DMA				
BPRN/	P1	15	Y	Bus Pri. In
BPRO/	P1	16	Y	Bus Pri. Out
BREQ/	P1	18	P	Bus Request
BUSY/	P1	17	Y	Busy Ready
CBRQ/	P1	29	P	Common Bus Request
MISCELLEANEOUS CONTROL				
BHEN/	P1	27	Y	Byte High Enable
BD RESET/	P2	36	N	Board Reset
HALT/	P2	28	N	Bus Master Wait State
INH1/	P1	24	N	Inhib. 1 disable RAM
INIT/	P1	14	Y	Initialize
MISCELLEANEOUS				
ACLO/	P2	18	P	AC Low
ALE/	P2	32	N	Bus Master ALE
AUX RESET/	P2	38	N	Reset Switch Reserved
LOCK/	P1	25	N	Inhib. 2 dis. PROM or ROM
MPRO/	P2	20	N	Memory Protect
PAR1/	P2	27	N	Parity 1
PAR2/	P2	29	N	Parity 2
WAIT/	P2	30	N	Bus Master Wait State

Mnemonic	Conn.	Pin	Used by 450	Description
POWER				
12VB	P2	11,12	N	+12V Battery
5VB	P2	3	N	+5V Battery
GVB	P2	4	N	Return
-5VB	P2	7,8	N	-5V Battery
-12VB	P2	15,16	N	-12V Battery
+5V	P1	3,4,5,6,81,82,83,84	Y	+5Vdc
+12V	P1	7,8	N	+12Vdc
+15V	P2	23,24	N	+15V
-5V	P1	9,10	Y	-5 volt supply
-12V	P1	79,80	N	-12Vdc
-15V	P2	25,26	N	-15V
EEVPP	P2	6	N	E^2 PROM Power
GND	P1	1,2,11,12,75,76,85,86	Y	Signal GND
GND	P2	1,2,21,22	N	Signal GND

Y = Yes; N = No; P = Possibly

5.2 STORAGE MODULE DRIVE INTERFACE

Name	Cable	Pin+/- CDC	Pin+/- Stnd.	Description
UNIT SELECT				
Unit Select Tag	A	52/22	44/43	Works with Unit Select Bits to initiate a unit select sequence.
Unit Sel. Bit 0	A	53/23	46/45	Binary weighted signals to determine one of 16 drives to be selected.
Unit Sel. Bit 1	A	54/24	48/47	
Unit Sel. Bit 2	A	56/26	52/51	
Unit Sel. Bit 3	A	57/27	54/53	
Open Cable Det.	A	44/14	28/27	A signal the controller can use to deselect the drive in event of power failure.
Unit Selected	B	09/22	17/18	A "B" cable signal indicating drive has been selected.
Unit Ready	A	49/19	38/37	The selected drive is up to speed and the heads are loaded, and not faulted.

Name	Cable	Pin+/- CDC	Pin+/- Stnd	Description
CONTROL				
Tag 1	A	31/01	02/01	Cylinder select tag causes the drive to seek to the cylinder selected by bus bits 0-10.
Tag 2	A	32/02	04/03	Head Select Tag causes the drive to select the head specified by Bus Bits 0-9.
Tag 3	A	33/03	06/05	Control Tag commands the drive to perform the function defined by Bus Bits 0-9.
Pwr. Seq. Hold	A	59	58	Used for power sequencing with Remote/Local
Sequence Pick In	A	29	57	Used for power sequencing with Remote/Local
Bus Bit 0	A	34/04	08/07	Write Gate Enable or bit 0 of head or cyl.
Bus Bit 1	A	35/05	10/09	Read Gate Enable or bit 1 of Head or cyl.
Bus Bit 2	A	36/06	12/11	Servo Offset + or bit 2 of head or cyl.
Bus Bit 3	A	37/07	14/13	Servo Offset - or bit 3 of head or cyl.
Bus Bit 4	A	38/08	16/15	Fault Clear or bit 4 of head or cyl.
Bus Bit 5	A	39/09	18/17	Address mark Enable or bit 5 of head or cyl.
Bus Bit 6	A	40/10	20/19	Recalibrate or bit 6 of head or cyl.
Bus bit 7	A	41/11	22/21	Data Strobe Early or bit 7 of head or cyl.
Bus Bit 8	A	42/12	24/23	Data Strobe Late or bit 8 of head or cyl.
Bus Bit 9	A	43/13	26/25	Release or bit 9 of head or cyl.
Bus Bit 10	A	60/30	60/59	Bit 10 of cylinder address
CLOCKS and DATA				
Index	A	48/18	36/35	A pulse for every index mark.
Read Clock	B	17/05	08/09	Clock to syncronize Read Data
Read Data	B	16/03	06/05	Read data from drive.
Sector	A	55/25	50/49	Pulse for every sector except during index.
Servo Clock	B	14/02	02/03	Clock to syncronize write data to.
Write Clock	B	19/06	12/11	Clock sent to drive with syncronized write data.
Write Data	B	20/08	14/15	Write Data sent to drive.

Name	Cable	Pin+/- CDC	Pin+/- Stnd	Description
STATUS				
Address Mark	A	50/20	39/40	Signal indicates if drive has found a sector mark. This is not used by the 450.
Busy	A	51/21	42/41	Indicates that a dual ported drive is busy to the other port.
Fault	A	45/15	30/29	Signal indicates if drive is faulted.
On Cylinder	A	47/17	34/33	Signal indicates if drive is on cylinder
Seek End	B	23/10	20/19	Signal indicate that the drive has completed its commanded seek or the ehads have just loaded.
Seek Error	A	46/16	32/31	Signal indicates if drive had a seek error.
Write Protect	A	58/28	56/55	Signal indicates if drive is write protected.

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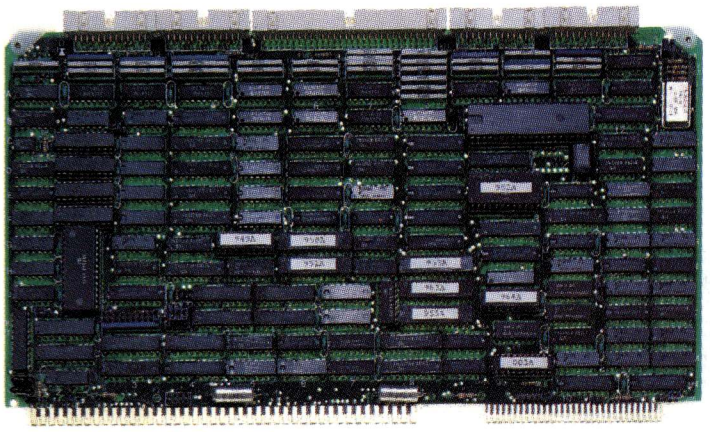
XYLOGICS 450 SMD DISK CONTROLLER.



The Xylogics 450 is a high performance disk controller for SMD compatible disk drives that sets the standard for price, performance, and size for IEEE-796 Multibus. Residing on one single-height Multibus printed circuit board, the 450 can address up to 16 MB of memory and control up to four SMD disk drives at data transfer rates up to 1.9 MB/sec. When attached to four drives, the 450 can access disk storage limited only by the capacity of existing drives.

The 450 uses the advanced technique of channel control for an optimal match to the multi-processing environment of the IEEE-796 bus and 16/32 bit microprocessors such as the 8086, 68000, 16032 and Z8000. A command is issued from an operating system by creating an I/O parameter block (IOPB) in memory and pointing the 450 at the IOPB. Multiple IOPBs can be linked together for optimal throughput. By using multiple IOPBs, implicit overlapped seeks and scatter-read and gather-write may be implemented.

Bad block handling is implemented by a sector slip method. Under system software control, a bad sector may be retired during system operation by use of special commands.

FEATURES	BENEFITS
• Fast DMA (up to 3.0 MB/sec.)	• Low Bus Utilization Overhead
• Overlap Seek Operation	• Access Time Reduced
• Bad Block Remapping	• Handles up to 4 Defective Sectors per Track
• High Speed Design	• Disk Data Rates up to 1.9 MB/sec. non-interleaved
• Programmable Drive Configuration	• Easy Configuration of System
• Single Board Design	• Requires Less Backplane Space
• IEEE-796 Bus Compatible	• Industry Standard Bus
• 16, 20 or 24 Bit Addressing	• Compatible with all Multibusses
• 2 or 8 KB FIFO Buffer	• Eliminates Lost Revolutions

FEATURES	BENEFITS
• SMD Interface	• Large Selection of Drives
• Up to 4 Drives per Board	• Growth Capability Built-In
• Mixed Capacity Drives	• Drive/Size Mix User Defined
• Standard Sector Sizes of 256, 512, & 1024 Bytes	• Optimized for User's Needs
• Programmable Throttle	• Support any Multibus Speed
• Selectable Device Address	• Matches System Requirements
• Programmable Interleave Factor (Standard 1:1)	• Customize System Throughput
• On-Board Diagnostic with Status LED	• Power Up Self Test
• Burned-in Components/Power Cycled	• Built-In Reliability

Xylogics®

The Peripheral Performance Leader.

MULTIBOOST

PRODUCT SPECIFICATIONS

Command Technique: The 450 uses the technique of channel control which allows the operating system to create a disk drive command in an I/O parameter block (IOPB) in memory. The command is initiated by loading the address of the IOPB into the IOPB address registers and setting the Go-bit in the command and status register. The 450 will execute the command and when complete, set a completion status and clear the Go-bit in the command status register. If interrupts are enabled, an interrupt will be generated when the Go-bit is cleared. If an error is detected, an error code is returned in the IOPB for examination by the operating system. A channel program may be created by linking IOPBs together in a chain to execute many functions sequentially with little or no host processor intervention, provided that the operating system driver can support and monitor this function. In addition, if IOPBs for different drives are queued at the same time, the 450 will initiate overlapped seeks.

I/O Parameter Block Format

Byte Offset	Description	Byte Offset	Description
0	Command	C	Data Address Low
1	Interrupt Mode	D	Data Address High
2	Status Byte 1	E	Data Relocation Low
3	Status Byte 2	F	Data Relocation High
4	Throttle		
5	Drive Select	10	Head Offset
6	Head Select	11	Reserved
7	Sector Select	12	Next IOPB Address Low
8	Cylinder Select Low	13	Next IOPB Address High
9	Cylinder Select High	14	ECC Mask High
A	Sector Count Low	15	ECC Mask Low
B	Sector Count High	16	ECC Bit Position Low
		17	ECC Bit Position High

Programmer Visible Registers: The 450 has six 8-bit programmer visible registers addressable as IEEE-796 byte I/O ports.

Byte 0 IOPB Relocation Low
Byte 1 IOPB Relocation High
Byte 2 IOPB Address Low
Byte 3 IOPB Address High
Byte 4 Controller Command and Status
Byte 5 Controller Reset/Update IOPB

Commands: The 450 supports the following commands:

Controller reset
Read with or without automatic ECC correction
Write
Seek
Drive Reset
Write Format
Read Header, Data and ECC
Write Header, Data and ECC
Read Drive Status
Set Drive Size
Self Test
Read Track Headers
Write Track Headers
Maintenance Buffer Load
Maintenance Buffer Dump

SPECIFICATION SUMMARY

Position Verification: Header preamble used with full sector, head and cylinder positioning data. Headers are written during format operation, and read for position verification on all subsequent seeks, reads and writes.

Data Verification: 32 bit ECC with 11 bit correction.

Disk Diagnostics: Comprehensive diagnostic is available for most 16/32 bit microprocessors written in C.

Customer Acceptance Tool: Xylogics Customer Acceptance Tool (XYCAT) is a Multibus-based single board processor with Xylogics 400 series diagnostics in ROM. It is used by Xylogics as a final acceptance test before shipping, and is available to customers for use in incoming tests. XYCAT contains the identical diagnostics that are available in C source code.

Software Support: Support for RMX[2]-86, XENIX[3], and Berkeley UNIX[4] 4.2 is available.

Sector Sizes: 256, 512 and 1024 standard. Others optional.

Data Transfers: From one to 65535 sectors. Transfers will cross sector, head and cylinder boundaries automatically (spiral read/write).

Transfer Mode: Throttle controlled, direct memory access (DMA). Throttle value specified in IOPB.

Transfer Rate: Disk data rates up to 1.9 MB/sec. are supported; however, the aggregate data rate depends on bus utilization and memory response time. With appropriate memory, the 450 can transfer a full cylinder to memory without losing a revolution of the disk. The 450 is capable of DMA speeds of up to 3.0 MB/sec. assuming XACK from memory of 300 ns.

Drive Compatibility: The 450 is compatible with fixed and removable SMD (1.2 MB/sec.) and modified SMD (1.9 MB/sec.) disk drives manufactured by the following companies: Ampex, Applied Peripherals, Century Data, Control Data, Fujitsu, Kennedy, Megavault, Memorex, Mitsubishi, NEC, Northern Telecom, Priam, Storage Technology, Tecstor and others.

Registers: Six

Dual Port Support: Standard

Status LEDs: Two LEDs indicate status. One goes on during power-up self-test and goes off after successful completion. If it stays on, an error has been detected. The other LED goes on to indicate that the 450 is active executing a command.

I/O Parameter Block Length: 24 bytes.

Command Chaining: Inherent in IOPB.

Address Capability: Up to 16 MB supported by the IEEE-796.

Packaging: One IEEE-796 Multibus standard size printed circuit card. Requires 6 Amps @ +5 and .6 Amps @ −5 VDC power from the backplane.

Sector Interleaving: 1:1 is standard. For slower Multibus configurations, interleave factor is programmable.

Environment: Meets IEEE-796 specifications.

IEEE-796 Compliance: Master D16 M24 V0L and Slave D8 I16.

FOOTNOTES
[1]Multibus is a trademark of Intel Corp.
[2]RMX is a trademark of Intel Corp.
[3]XENIX is a trademark of Microsoft Corp.
[4]UNIX is a trademark of Western Electric Corp.

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July 19, 1984

In response to your recent telephone conversation with Mark Lindholm, I am enclosing copies of Field Change Notices, # 12, 13, 13A and 450-20.

If you have any further questions after reviewing these, please don't hesitate to contact us.

Sincerely,

Kindra Alaimo

Kindra B. Alaimo
Manager,
Sales Administration

KA/tbm

Encl.

cc: M. Lindholm
J. Dean

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FIELD CHANGE NOTICE

FCN No. 450-20

PAGE 1 OF 1

DATE:		PRODUCT TYPE	
July 2, 1984		450	
FCN CLASS:	**ECO No.**	**DOC PKG NO.**	**REV**
E	1116	See Below	
TITLE: Correct Signal Short to GND		**PRODUCT SUPPORT APPROVAL** DATE: 7/9/84 BY: Joseph A Gontarell GSE 7/9/84	

REASON FOR CHANGE: This change corrects an artwork error. The error shorted a signal to ground. With this short the 450 will not function.

Effectivity:

No boards were shipped to the field with this mod. This change causes the documentation package revision level to change as shown below:

	From Rev	To Rev
900-450-900	J	K
900-450-901	J	K
900-450-902	E	F
900-450-903	E	F
900-450-904	J	K
900-450-905	J	K
900-450-906	E	F
900-450-907	E	F
900-450-908	F	G
900-450-909	F	G
900-450-910	D	E
900-450-911	B	C
900-450-912	B	C

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FIELD CHANGE NOTICE

FCN No. 13-Rev. A

PAGE 1 OF 1

DATE:		PRODUCT TYPE
July 9, 1984		450
FCN CLASS: C	**ECO No.** 1110	**DOC PKG NO.** 900-450-900, 901, 904, 905 Rev. J; 900-450-902, 903, 906, 907 Rev. E; 900-450-908, 909 Rev. F; 900-450-910 Rev. D
TITLE: XACK DRIVE PROBLEM		**PRODUCT SUPPORT APPROVAL** **DATE:** 7/9/84 **BY:** Approved ENG APPROVAL SEC 7/9/84

REASON FOR CHANGE:

Typographical error made on original FCN No. 13 dated 4/25/84. Revision letter "I" on tabs 900, 901, 904 and 905 shown in Doc. pkg. No. is incorrect. The correct revision letter is "J". Xylogics does not use the letters "I" and "O" to indicate a revision level.

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FIELD CHANGE NOTICE

FCN No. 13

DATE: 4/25/84		PRODUCT TYPE 450
FCN CLASS: C	ECO No. 1110	DOC PKG NO. 900-450-900, 901, 904, 905 Rev. I; 900-450-902, 903, 906, 907 Rev. E; 900-450-908, 909 Rev. F; 900-450-910 Rev. D
TITLE: XACK DRIVE PROBLEM		PRODUCT SUPPORT APPROVAL DATE: 4/27/84 BY: Richard L. Norton

REASON FOR CHANGE: The 74125 used to drive the Multibus signal XACK does not provide the proper sink current. This change provides the necessary sink current.

Effectivity:

Only those systems using more than 4 Multibus loads.

Implementation (See attached drawing): Remove the 74125 in location M10.

Etch cuts:

IC location	-	Pin
M10		5
M10		11
M10		13*
B4		18

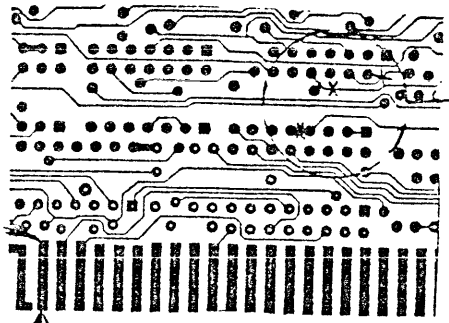
* Important - Two etch cuts are necessary - one on the etch side of the board - the other on the component side.

Add wire jumpers:

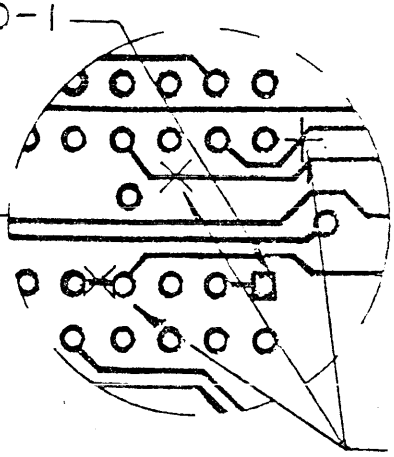
From	To
M10-5	M10-7
M10-7	M10-12
M10-4	M10-13
M10-6	M10-11
D5-10	N12-1

Install a new 74125 back into location M10.

NONCOMPONENT SIDE

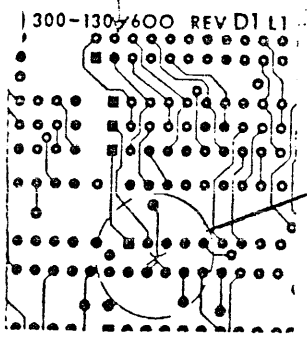


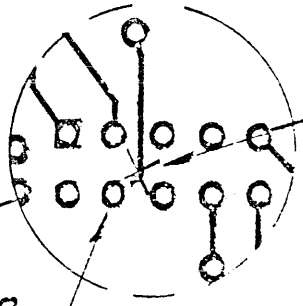
P2-60

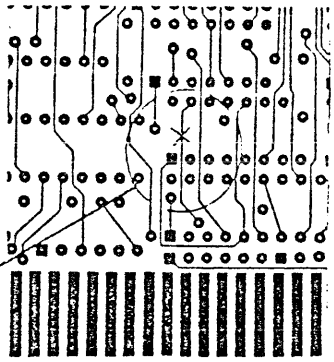


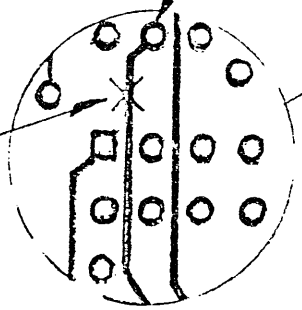
COMPONENT SIDE

CONNECTOR J1









SIZE	DRAWING NO.	REV
A		
SCALE	SHEET OF	LEVEL

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FIELD CHANGE NOTICE

FCN No. 12

DATE: 4/5/84		PRODUCT TYPE: 450
FCN CLASS: C	ECO No. 1109	DOC PKG NO. 900-450-9XX REV 900, 901, 904. 905-Rev. H; 911-Rev. A 902, 903, 906, 907-Rev.D; 908, 909-Rev. E
TITLE: 450 Microcode Enhancements/Fixes		PRODUCT SUPPORT APPROVAL DATE: 4-5-84 BY: Richard L. Horton

REASON FOR CHANGE:

The microcode on the 450 has been revised along with the disk sequencer configuration proms. The enhancements/fixes made along with a description of each of the changes are listed below.

ENHANCEMENTS:

1. End of Sector Fix: The 450 is now capable of running up to 47 data sectors on the Fujitsu Eagle (2351) and 34 sectors on CDC 80mb SMD type drives. This is an added feature and does not effect current configurations. This feature requires the latest revision disk sequencer proms. See below for for tab configuration revision level upgrade:

TAB	DESCRIPTION	PROM P/N	NEW REVISION
900	2KB/440/512BYT	961	B
901	8KB/440/512BYT	965	B
902	2KB/440/256BYT	967	B
903	8KB/440/265BYT	969	B
904	2KB/450/512BYT	954	B
905	8KB/450/512BYT	963	B
906	2KB/450/256BYT	971	B
907	8KB/450/256BYT	973	B
908	2KB/450/1024BYT	975	B
909	8KB/450/1024BYT	977	B
911	8KB/450/2048BYT	991,992	A

Both the CDC and Fujitsu require sector switch settings not specified in their respective manuals. The settings are as follows:

CDC Sector Switch Setting*: 1 2 3 4 5 6 — 0 0 0 1 0 0 — 1 2 3 4 5 6 — 0 1 1 0 0 0

*NOTE: 1= closed 0= open

Fujitsu Setting: (jumper installed)
BC7: 3-4, 5-6, 10-11, 13-14
BD7: 2-3, 6-7, 9-10, 13-14
BE7: 3-4, 5-6, 10-11, 13-14
BF7: 3-4, 6-7, 10-11, spare

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2. Adaptive Format Status Bit (AFE): A status bit has been added to IOPB byte 5 bit 4. This enables diagnostic software to determine if a controller is configured for adaptive format. Adaptive format is selected by all 450's which are '450 format' compatible and is not selected by 450's which are '440 format compatible. This bit is only set on a Read Drive Status command.

3. Embedded Servo Change: A bit was added to the Set Drive Parameters Command to enable a seek after a head change option. This bit now allows the user to select a seek after every head change which is required for embedded servo disk drives. The embedded servo bit is bit 7 of the head offset byte in the Set Drive Parameters command. Set bit 7 in the head offset byte to enable a seek after every head change. This change effects such drives as the CDC Lark 9755 and 9757, and the Northern Telecom 8210.

4. As part of the new microcode release Xylogics has added a new sector size. The 450 now supports 2048 bytes per sector which can be ordered as Tab 911. The disk sequencer proms will be labeled 992A and 993A. This configuration will only run with boards utilizing 8KB buffers which is due to the size of the sectors. The CDC SMD 9762 was set up for 9 sectors per track and requires special sector switch settings (see below). The Fujitsu Eagle was set up for 13 sectors and the settings were taken out of the Eagle manual.

CDC Sector Switch Setting:	1 2 3 4 5 6	1 2 3 4 5 6
	1 0 1 0 1 1	1 0 0 1 0 1

NOTE: 1=closed 0=open

FIXES:

1. Problem: Attention Request Protocol did not allow the addition of IOPB's into a chain already in progress.

   Customer Effect: Only those customers using chaining with Attention Protocol.

   Solution: Microcode has been updated to properly handle Attention Protocol. Inhouse diagnostics have been updated to handle the latest changes.

2. Problem: The 450 did not properly release a dual ported drive to allow access by the controller to another drive port.

   Customer Effect: Any customer using the dual ported drives.

   Solution: Microcode updated to properly release a dual ported drive.

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3. Problem: Memories with XACK response times greater than 20 micro seconds would cause the 450 to update the bus address incorrectly.

   Customer Effect: Only those customers using slow memories.

   Solution: The 450 now properly updates the bus address when slower memory is used.

4. Problem: Accessing non-existant memory for IOPB DMA would not timeout and would hang the Multibus.

   Solution: A DMA timeout has been added for IOPB DMA.

5. Problem: The 450 will report the wrong sector number in error when reporting a hard ECC error. The sector reported is one greater than the actual sector in error.

   Solution: Microcode has been updated to report the correct sector in error.

6. Problem: SMD class disk drives with slow data transfer rates may fault when a hard ECC error occurs. This was caused by deselecting the drive on an ECC correction without dropping Control Tag.

   Customer Effect: Any customer using disk drives with transfer rates below SMD standard. This problem was experienced with an older CDC SMD 9762 and a Fujitsu 2284 (168MB - 1.0MB/SEC).

   Solution: Microcode has been updated to handle slower SMD data rates.

7. Problem: The 450 was unable to interleave greater than 7:1.

   Customer Effect: Only those customers using interleave factors greater than 7:1.

   Solution: The 450 interleaves 16:1 as documented in the 450 manual.

8. Problem: Read Track Headers Command will go to drive pseudo instead of drive index.

   Customer Effect: Read and Write Track Headers commands are typically used during format time and for remapping defective sectors.

   Solution: Now both Read Track Header and Write Track Header Commands work from physical drive index.

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9. Problem: Read Header Data ECC and Write Header Data ECC commands currently work from pseudo index and not drive index.

   Customer Effect: Both these commands are typically used for diagnostic purposes and do not effect normal software driver operation.

   Solution: Both commands now work from drive index. These commands no longer check for a sector address greater than max, which means you can now read absolute sector addresses greater than the max sector. This also means that the implied seek to cross head boundries does not happen. Also remember that reading a runt sector will cause disk sequencer errors because we attempt to transfer full sectors of data.

10. Problem: If the 450 reads an IOPB from its internal ram and then does not get an XACK from system memory during an IOPB update the 450 will hang the Multibus.

    Solution: Microcode has been updated to timeout during an update when XACK does not respond. This condition will result in a double error.

11. Problem: ECC errors on the header were being picked up as header not found errors on the next data transfer command and the previous data transfer was not being completed.

    Customer Effect: ECC errors on the header are an uncommon occurance.

    Solution: Header ECC errors are now being found as header not found errors. Software should retry the IOPB which found this error.

12. Problem: When using the Set Drive Parameters command to change drive types the 450 returns zero sectors instead of the actual max sector for the drive.

    Solution: The 450 now returns the correct sector count for the drive selected. NOTE: If the drive is not ready this command will return a sector count of zero.

13. Problem: The 450 address and relocation bytes are not being properly updated upon completion of the command as indicated in the manual.

    Customer Effect: Only cause a problem if the updated addresses are being used.

    Solution: Upon IOPB completion addresses are now being updated correctly.

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14. Problem: Executing a Read Drive Status command with the drive write protected will report a hard error condition.

    Solution: After execution of a Read Drive Status command no errors are returned to IOPB status bytes 1 and 2. The actual drive status is returned in Drive Status byte A.

15. Problem: Attempting to format a write protected disk will hang the controller.

    Solution: The 450 now reports write protected error in the completion code and reports a hard error condition.

16. Problem: Auto update command would update the command byte and the interrupt mode byte which could clear out any newly added chain bit of an Attention Request Acknowledge sequence.

    Customer Effect: Only those customers using the auto-update feature and chaining IOPBs.

    Solution: Auto update no longer updates these bytes enabling chaining to continue if chain bit has been added to an IOPB.

17. Problem: If chained operations are being used and the EEF bit is set the 450 ignore the done in an already completed IOPB and will attempt to re-execute that IOPB. This error will cause overlap seeks to work improperly.

    Customer Effect: Only those customers using the EEF bit or implementing overlap seeks.

    Solution: Microcode has been updated and the overlap seek feature has been fully tested. NOTE: It is now necessary to clear the done bit before passing the 450 an IOPB.

18. Problem: When formatting completes the sector address is off by one sector. This does not result in the format being bad only the returned count is off.

    Solution: The sector address reported is the last sector formatted.

IMPLEMENTATION:

Remove 952B EPROM from location E9 and install 952C EPROM. Remove 9XXA prom (XX = tab dependant) from location J8 and install 9XXB prom.

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