10 Block Checking

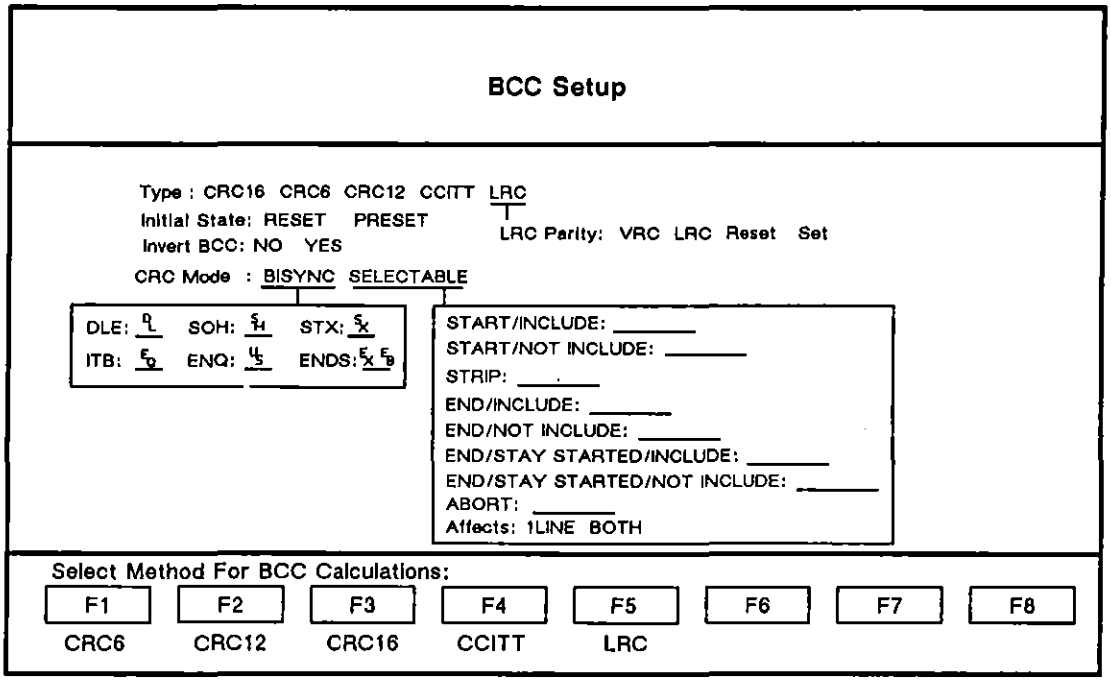


Figure 10-1 Fields and selections on BCC Setup screen.

10 Block Checking

The INTERVIEW is capable of a variety of standard and nonstandard block-check calculations (BCCs). These calculations can be appended to the INTERVIEW's own transmissions and they also can be used for comparison with BCCs in the line data. The results of the comparison are displayed on the unit's monitor as special symbols representing good and bad BCCs. (A "good" BCC in the line data is one that agrees with the INTERVIEW's own internal calculation.) The result of a BCC evaluation can also be used to satisfy a trigger condition.

10.1 BCC Symbols

The internal BCC that the INTERVIEW compares with a BCC in the line data and then displays as a special symbol on the data screen is enabled in a field on the Line Setup menu. This field is named **Rcv Blk Chk** and is shown in Figure 10-2. When **Rcv Blk Chk:** ON is selected, the unit evaluates as "good" or "bad" the BCCs in all properly framed data blocks. The last byte in the data BCC is then overwritten on the INTERVIEW monitor with G or B. Figure 10-3 shows a BCC symbol written over the second character of a line BCC that has been judged bad.

Figure 10-2 A field on the Line Setup menu enables block checking on all data "received" to screen and triggers.

It should be noted that the BCC-appending function and the BCC-evaluating function are separate, and that the **Rcv Blk Chk** field enables BCC *evaluation* in all data, including the INTERVIEW's own transmissions. The data block in Figure 10-3 was transmitted by the INTERVIEW. It is simply a fox message framed by ETX and ETX and preceded by sync characters. The transmit trigger that generated the message specified "no BCC" to be appended to the data (see Section 10.3), so ETX is followed by idle ▨ (pad) characters. But since **Rcv Blk Chk** is enabled, the unit treats the first two idle characters as BCC and evaluates them accordingly.

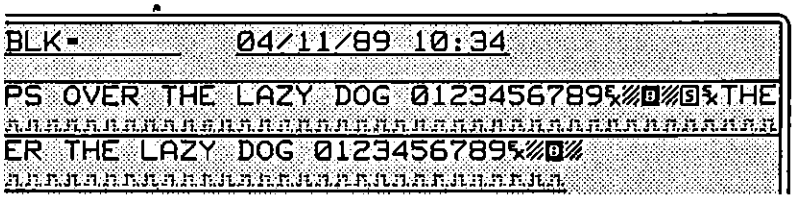


Figure 10-3 A special symbol overlays the final character in a bad BCC.

For non-BOP data, there are two ways to look underneath the G or B overlay to get a glimpse of the concealed final block-check character. One way is to select **Rcv Blk Chk: OFF**. Then the complete block-check calculation monitored by the INTERVIEW is displayed on the screen, with no special symbol overlaying the final BCC character.

The second way to uncover the hidden block-check character is to look at the binary expansion of the character in Freeze mode. In Figure 10-4, the operator has pressed FREEZE and then moved the cursor over the good-BCC symbol. In Freeze mode, the binary expansion of any character that comes under the cursor (including a concealed block-check character) is given at the top right of the screen.

When you look at the binary expansion of a BOP BCC-overlay, disregard the two least-significant (rightmost) bits. The third bit from the right is the real least-significant bit in the second BCC byte. The two high-order bits of the frame-check sequence simply are not made available for viewing by the BOP hardware.

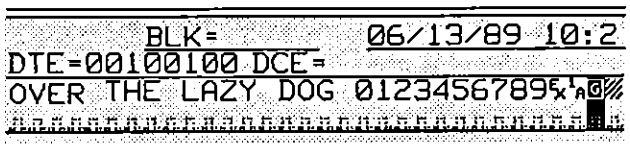


Figure 10-4 From the Freeze-mode binary expansion of the cursor character, it is easy to tell that the the good-BCC overlay is covering a hexadecimal *24*.

For BOP formats, **Rcv Blk Chk** does not appear on the Line Setup menu. Block-check evaluation is automatically *on* for BOP.

In BOP format only, block-check evaluation includes an abort symbol, A. Bisync devices signal an abort by sending ␆ in the middle of a text block, but BOP devices send no such control character—they merely idle mark for seven bit-times to indicate an aborted frame. The INTERVIEW uses the A symbol to stamp these seven consecutive 1-bits clearly as an abort.

Control over the type of block check and the many parameters associated with the type is afforded on the BCC Setup screen. The selections on this screen are laid out in Figure 10-1.

The BCC Setup screen does not operate for BOP. This format has a well-defined block-check sequence that is not alterable in the INTERVIEW.

10.2 BCC Conditions

Good and bad BCCs (and aborts in BOP format) can be used as trigger conditions. Figure 10-5 shows a GD BCC condition on a trigger menu. And here is an example of a BDBCC condition in a Protocol Spreadsheet test for Layer 1:

```
LAYER: 1
  TEST: bcc
    STATE: bad_bcc
        CONDITIONS: RECEIVE BAD_BCC
        ACTIONS: COUNTER bad_bcc INC
```

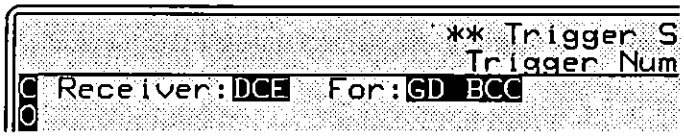


Figure 10-5 Good and bad BCCs can be used as trigger conditions.

Figure 10-6 is a string condition with a further condition added: Wait for E(nd) O(f) F(rame), the literal meaning of which is "wait for a good BCC." None of the triggers in these examples can come true unless block-check evaluations are enabled on the Line Setup menu. This enabling is automatic in BOP format. In other formats, Rcv Blk Chk: ON must be selected as a line-setup parameter.

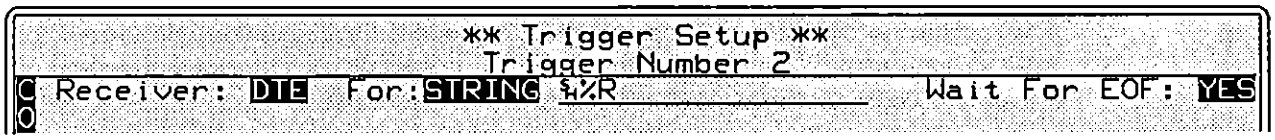


Figure 10-6 *Wait For EOF* following a *Receiver* condition means "wait for a good BCC."

10.3 Transmitted BCC

Block-check calculations that the INTERVIEW appends to messages and transmits out onto the line are enabled in the BCC field on trigger menus and in similar entries on the spreadsheet. BCC is a subfield under Xmit on trigger-action menus (see Figure 10-7). On the spreadsheet, transmitted BCC is a subselection under SEND: every time you transmit ("send") a message you have a choice of appending a good BCC, a bad one, an abort (BOP only), or nothing (not applicable to BOP).

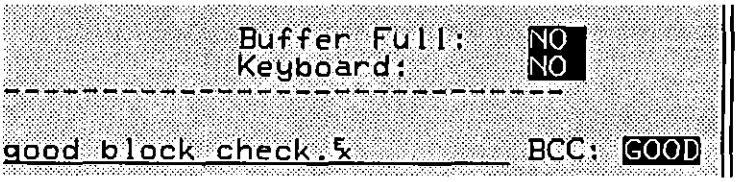


Figure 10-7 A transmitted BCC may be selected on the *actions* half of a trigger menu.

Please note that **BCC:** GOOD or BAD following a transmit string does not mean that a BCC will always follow. In bisync, the INTERVIEW will append BCCs only to text strings that are *properly framed*—as, for example, by STX and ETX (or ETB). If you are sending a bisync poll or ACK or ENQ or some other nontext message, your selection in the **BCC** field will have no significance.

BCC: NONE means that the INTERVIEW will go directly from transmitting the transmit string to idling mark, even if the string begins with STX and ends with ETX or ETB. The unit's receivers, if they are enabled for block checking and if they stay in sync for the requisite number of BCC characters, will interpret this no-BCC as a bad BCC (Figure 10-3).

In BOP format, the sudden shift from data to mark idle is an abort. The third BCC selection in BOP triggers therefore is called ABORT instead of NONE. The receivers put up the appropriate ◘ symbol when they see the seventh mark bit.

Good BCCs are transmitted in accordance with the parameters in effect on the BCC Setup menu. See Section 10.5.

10.4 Standard BCC Parameters

A specific set of block-check parameters is standard for each code selected on the Line Setup menu. Table 10-1 summarizes the correct BCC settings for the various standard codes and formats supported by the INTERVIEW.

The actual equations used by the INTERVIEW in block-check calculations are defined in Table 10-2.

Changes to the BCC Setup menu remain on the menu when you change line-setup formats.

Table 10-1
Standard Block-Check Parameters for Sync or Async/Isoc Formats

Code	Type	BCC starts following	BCC aborts/resets on	BCC ends with
EBCDIC	CRC-16	$^{5}_{H}$ or $^{5}_{X}$	$^{5}_{0}$ or next bit after BCC	$^{5}_{B}$, $^{5}_{X}$
ASCII	LRC	$^{5}_{H}$ or $^{5}_{X}$	$^{5}_{0}$ or next bit after BCC	$^{5}_{B}$, $^{5}_{X}$
IPARS	CRC-6	SY2 ($^{3}_{E}$)	SY1 ($^{3}_{F}$) or next bit after CRC	EOM-PB ($^{3}_{D}$) EOM-1 ($^{0}_{D}$) EOM-C ($^{1}_{D}$) EOM-U ($^{2}_{D}$)
BAUDOT	LRC	--	--	--
EBCD/ SELECTRIC	LRC; *Xmit:* LRC parity=LRC *Recv:* Ignores parity bit	*Xmit:* sync *Recv:* bid (#)	$^{5}_{F}$ on either side resets BCC for both sides	$^{5}_{B}$
XS-3	LRC	$^{4}_{0}$	--	$^{5}_{S}$ (not included in BCC)

Table 10-2
Block Check Polynomials

BCC Type	Block Check Polynomial
CRC-16	$X^{16} + X^{15} + X^2 + 1$
CRC-CCITT	$X^{16} + X^{12} + X^5 + 1$
CRC-12	$X^{12} + X^{11} + X^3 + X^2 + X + 1$
CRC-6	$X^6 + X^5 + 1$

(A) BOP Format

For Bit-Oriented Protocols, the INTERVIEW defaults to the BCC calculations standard for BOP. The parameters for these calculations cannot be changed on the BCC Setup screen. Any changes to this screen while the unit is set up for BOP will not be executed until another format (such as ASYNC) is selected. The changes will remain on the BCC Setup menu when you change formats.

(B) Sync and Start-Stop Formats

When a format other than BOP is selected on the Line Setup menu, the unit must be set up for BISYNC or SELECTABLE **CRC Mode** depending on the code selected on the Line Setup menu. The various correct configurations for SYNC or start-stop formats (ASYNC and ISOC) are detailed below.

1. *EBCDIC or ASCII code.* Both EBCDIC and ASCII require **CRC Mode:** BISYNC, but EBCDIC uses a sixteen-bit CRC-16 calculation while ASCII uses an eight-bit LRC check. You may redefine the values of the BCC control characters using alternate control characters, standard alphanumerics, or hexadecimal characters. You may also indicate that the control character does not exist by leaving the field blank. See Section 10.6 on bisync CRC-mode operation.

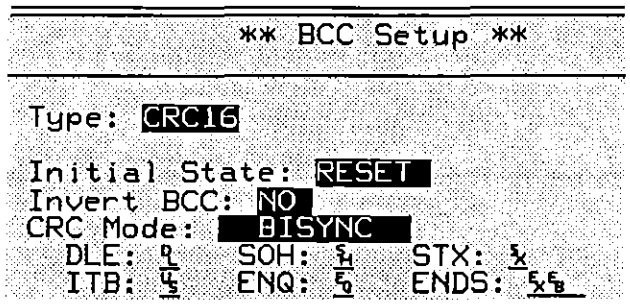


Figure 10-8 BCC setup for EBCDIC.

2. *IPARS.* Selecting **Code:** IPARS in sync or async (or isoc) format requires the BCC parameters shown in Figure 10-10. IPARS requires **CRC Mode:** SELECTABLE and uses CRCB to calculate BCCs. Any of the BCC parameters may be changed to meet specific applications.

3. *BAUDOT.* Since Baudot does not normally support block checking, there are no standard settings.

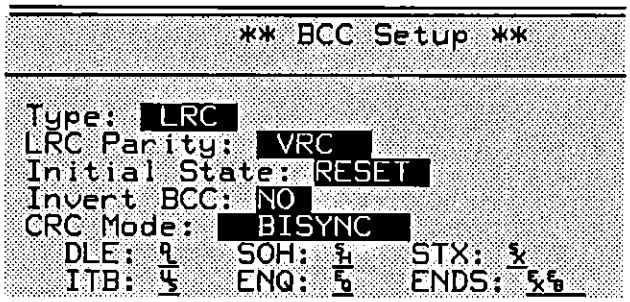


Figure 10-9 BCC setup for ASCII.

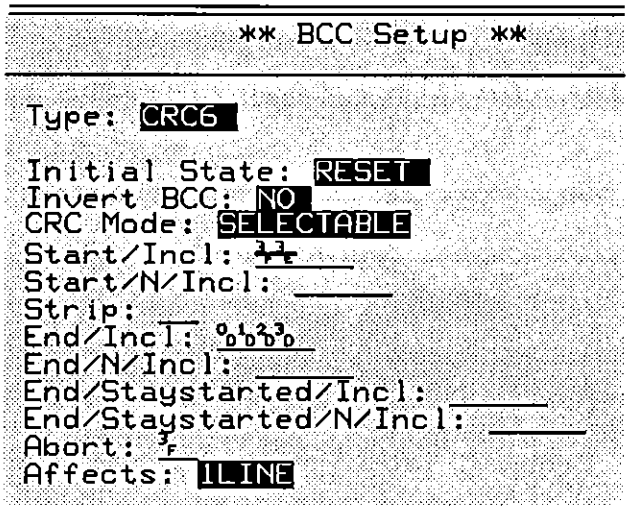


Figure 10-10 BCC setup for IPARS.

4. *EBCD, XS-3, or SELECTRIC.* Selecting EBCD or SELECTRIC code for SYNC or for either of the start-stop formats will require the BCC parameters shown in Figure 10-11. The XS_3 parameters are shown in Figure 10-12. All three codes require SELECTABLE CRC mode and use an LRC check to determine BCCs. Any of the BCC parameters may be changed to meet specific applications.

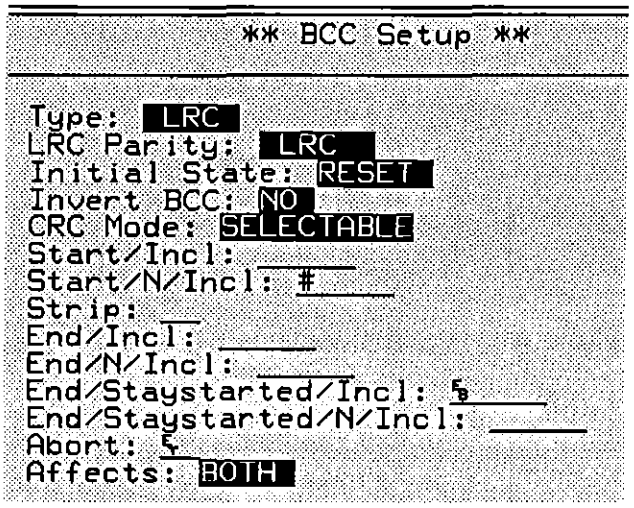


Figure 10-11 BCC setup for EBCD or SELECTRIC.

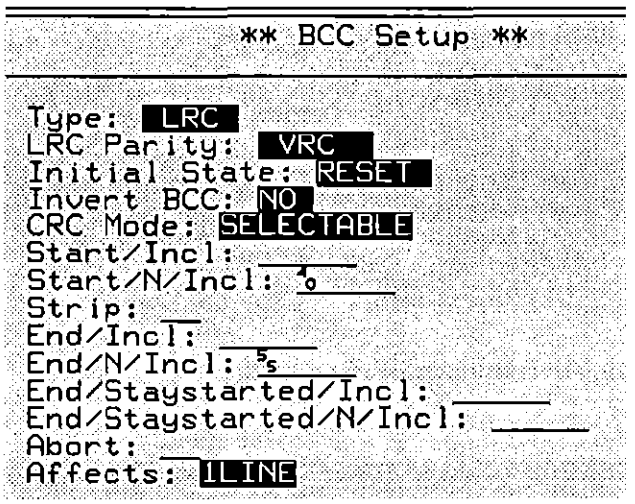


Figure 10-12 BCC setup for XS-3.

10.5 BCC Setup Menu Fields

The BCC Setup Menu controls and displays the values of the INTERVIEW's block check parameters. The full set of parameters is shown in Figure 10-1. The meanings of the BCC Setup parameter fields are found in Table 10-3.

Entries on the menu may be made in either alphanumerics, control characters, or hexadecimals. In the **START/INCL** field only, characters may also be entered in the not-equal format. See, for example, the IPARS setup in Figure 10-10.

Use control characters instead of hexadecimals where possible, since hexadecimals commit you to a particular parity that may change later on. An ASCII ENQ, for example, is hex 0_2 or 8_2 depending on the parity selected on the Line Setup menu. If you enter 0_2 in the **STX** or **START/N/INCL** field on the BCC Setup screen, the software will recognize ENQ only in odd-parity ASCII data. An entry of ENQ, on the other hand, will adjust for whatever parity is enabled on the Line Setup menu.

Table 10-3
BCC Setup Menu Fields

Type	Indicates method of BCC calculation selected. Polynomial expansions of each CRC type are listed in Table 10-2.
LRC Parity	Displayed when *Type: LRC* is selected. Identifies how the parity bit in the BCC character is calculated. *LRC* = parity bit in BCC character the result of an LRC on the parity bits within the message *VRC* = parity bit the result of a VRC on the BCC character *RESET* = parity bit always 0 *SET* = parity bit always 1
Initial State	Sets initial state of block check character. *RESET* = all 0's. When *Type* is *LRC*, this selection yields an *even* longitudinal check. *PRESET* = all 1's. When *Type* is *LRC*, this selection yields an *odd* longitudinal check.
Invert BCC	*YES* produces an inverted BCC by changing 1's to 0 and 0's to 1.
CRC Mode	Allows choice between *BISYNC* and *SELECTABLE* CRC modes.
BISYNC control character fields	Data-entry fields displayed for *BISYNC* CRC mode only. Allow you to select the characters that control block-checking. Default is standard set of bisync control characters. Alphanumeric, hexadecimal, and control characters are legal.
START/INCL	Displayed when *SELECTABLE* is chosen. Identifies the character(s) on which the INTERVIEW initiates BCC accumulation, and includes the character(s) in the accumulation. For this field only, characters may be entered in either normal or not-equal format.

Table 10-3 (continued)

START/N/INCL	Displayed when *SELECTABLE* is chosen. Identifies the character(s) on which the INTERVIEW initiates BCC accumulation, and does not include the character(s) in the accumulation.
STRIP	Displayed when *SELECTABLE* is chosen. Identifies character(s) to be stripped from BCC accumulation.
END/INCL	Displayed when *SELECTABLE* is chosen. Identifies the character(s) on which the INTERVIEW ends BCC accumulation, and includes the character(s) in the accumulation. Initiates processing of BCC. Returns to START state when processing is complete (see Figure 10-14).
END/N/INCL	Displayed when *SELECTABLE* is chosen. Identifies the character(s) on which the INTERVIEW ends BCC accumulation, and does not include the character(s) in the accumulation. Initiates processing of BCC. Returns to START state when processing is complete (see Figure 10-14).
END/STAYSTARTED/INCL	Displayed when *SELECTABLE* is chosen. Identifies the character(s) on which the INTERVIEW ends BCC accumulation, and includes the character(s) in the accumulation. Initiates processing of BCC. Returns to ACCUMULATE state when processing is complete (see Figure 10-14). This function is performed by the ↳ (Intermediate Block-check or ITB) character in bisync.
END/STAYSTARTED/N/INCL	Displayed when *SELECTABLE* is chosen. Identifies the character(s) on which the INTERVIEW ends BCC accumulation, but does not include the character(s) in the accumulation. Initiates processing of BCC. Returns to ACCUMULATE state when processing is complete (see Figure 10-14).
ABORT	Displayed when *SELECTABLE* is chosen. Identifies character(s) on which the INTERVIEW aborts BCC accumulation and returns to START state (See Figure 10-14). This function is performed by E_B in bisync. Note that the abort *function* does not generate an abort *overlay* on the screen. The user may enhance the abort character in the *Enhance* field on the Display Setup menu. See Section 6.3(D).
Affects	This field pertains to the *ABORT* character on the preceding line. The choices are *1LINE* or *BOTH*. The abort character may cause only the side of the line sending the character to reset its BCC; or it may have this affect on both sides. E_T in EBCD/SELECTRIC is an example of a character that resets BCC on both sides.

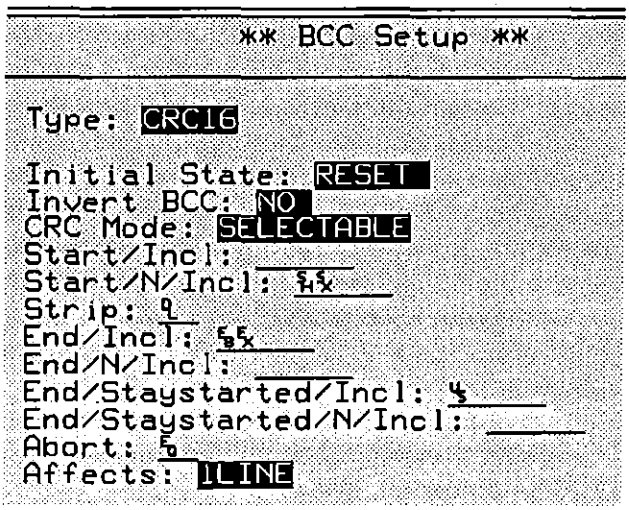


Figure 10-13 A valid BCC for nontransparent bisync can be configured "manually" using *SELECTABLE* parameters.

10.6 BISYNC vs. Selectable CRC Mode

The INTERVIEW supports an expanded subset of IBM's "Binary Synchronous Control Procedures" (BISYNC) that covers a wide variety of BISYNC-type applications including Burroughs, Honeywell, Univac, ISO-1175, and others.

Figure 10-8 shows the menu subfields under **CRC Mode:** BISYNC. In these subfields you may specify the values of the six BISYNC control characters (DLE, ITB, SOH, ENQ, STX, and ENDS) which appear on the BCC Setup menu with default character values already assigned (see Figure 10-8).

The BISYNC configuration has one important advantage, however, in that it implements full ^L transparency. When **CRC Mode:** BISYNC is employed, the appearance of ^L^X will enable a transparent mode in which all control characters except ^L are accumulated as data characters while their control functions are ignored. SELECTABLE mode offers no similar mechanism for treating control characters as data. The SELECTABLE setup in Figure 10-13 will work, therefore, only as long as the bisync data is not transparent.

Most of the bisync control characters have counterparts on the *other* set of BCC parameters, accessed under **CRC Mode:** SELECTABLE. Figure 10-13 shows how a standard bisync BCC would look if it were configured using the SELECTABLE subfields on the BCC Setup screen. Compare this screen with the bisync screen in Figure 10-8. Note that the names of the fields in Figure 10-13 are functionally descriptive. Start-Of-Header and Start-of-TeXt characters, for example, are really START/Not/INCLuded characters. This indicates that they activate block-check accumulation but they are not themselves included in the calculation. $^{E}_{B}$ and $^{E}_{X}$, on the other hand, which end the BCC accumulation, *are* included in the block-check calculation. Note also that the set of SELECTABLE parameters is more complete, and that thirty-four distinct characters may be designated as control characters compared to eight in the BISYNC fields.

A state diagram of SELECTABLE parameters is presented in Figure 10-14. In this diagram, process-BCC state does the following:

- Calculates and displays BCC result.
- Reinitializes BCC remainder.
- If end character was a STAYSTARTED character, returns to accumulate state.
- Otherwise, returns to start state.

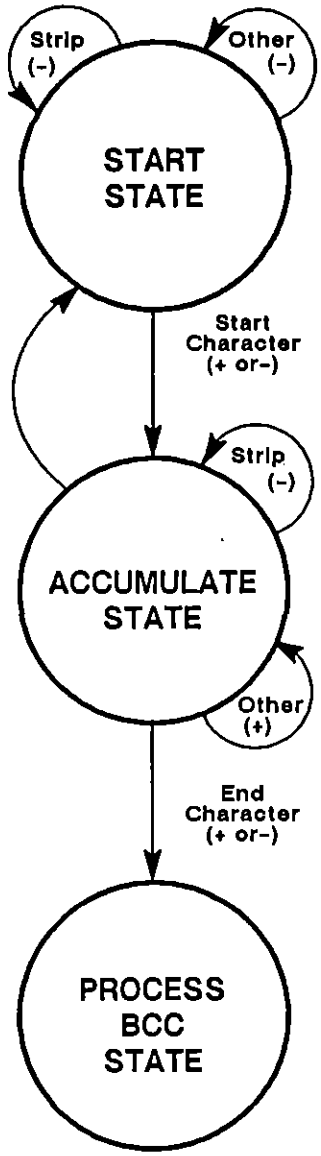


Figure 10-14 State diagram for CRC Mode: *selectable*. (+) means the character is included in BCC calculation; (-) means the character is not included.

11 Bit Error Rate Testing

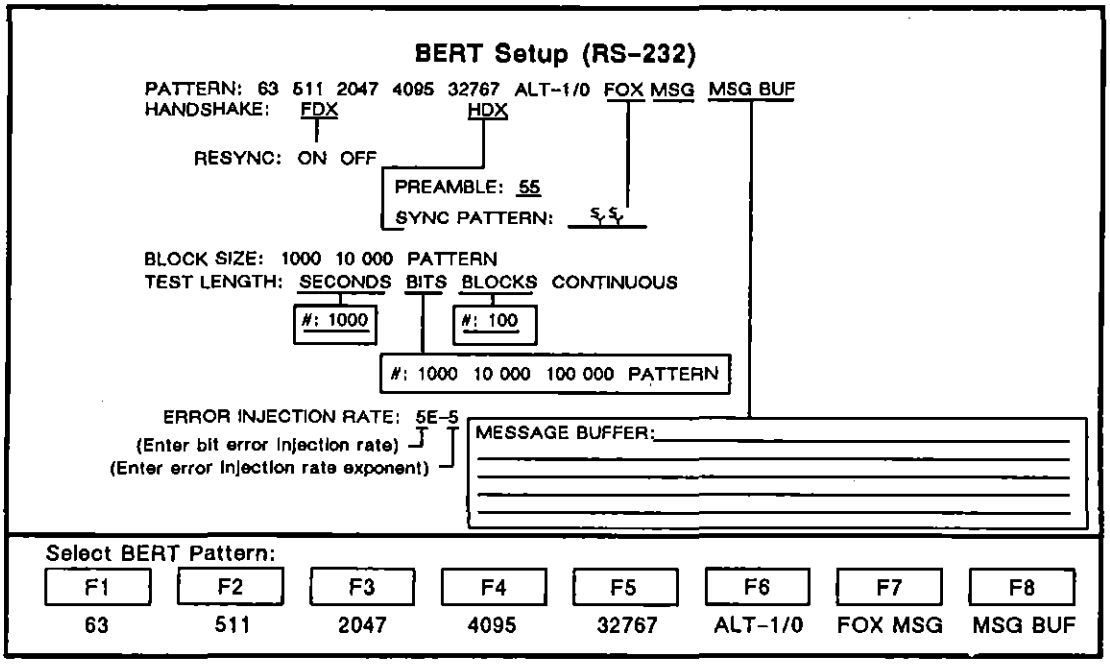


Figure 11-1 Menu selections on the BERT Setup screen.

11 Bit Error Rate Testing

The INTERVIEW can transmit and analyze Bit Error Rate Tests consisting of five different pseudorandom bit patterns, a series of alternating 1's and 0's, a canned fox message, and a user-assigned message of up to 259 characters. The INTERVIEW can send and analyze BERT patterns in synchronous or asynchronous format over transmission facilities that are full duplex or half duplex.

11.1 Pseudorandom Bit Patterns

BERT data may be transmitted and analyzed in pseudorandom patterns of 63, 511, 2047, 4095, or 32767 bits. The algorithm for each pattern is diagrammed in Figure 11-2.

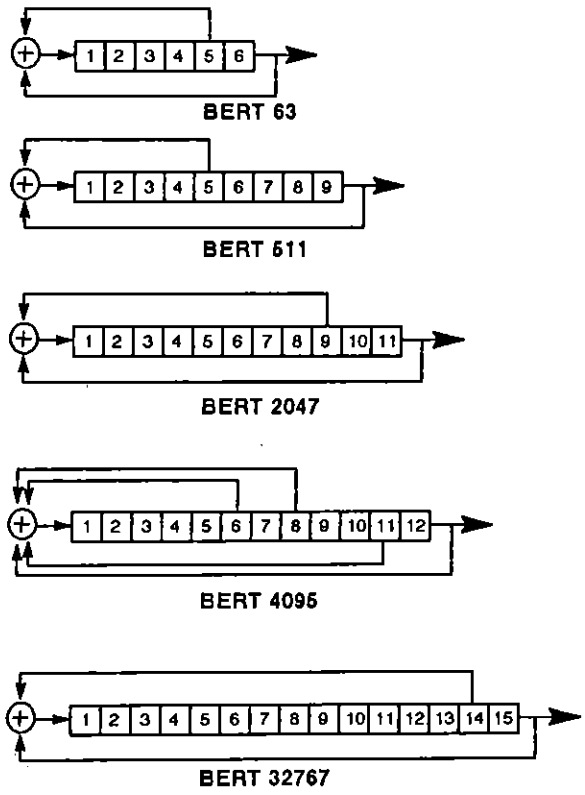


Figure 11-2 BERT algorithms.

11.2 Test Configurations

Tests can be configured for one tester or two.

A standard one-tester configuration places the remote modem (remote from the INTERVIEW) in a loopback condition. See Figure 11-3. The INTERVIEW generates the BERT data and analyzes the data upon its return over the transmission line. This is the easiest test to configure, since the INTERVIEW's BERT analyzer automatically looks for the same pattern of data that the unit generated.

When another BERT generator is used at the remote site, each tester analyzes the data generated by the other. See bottom of Figure 11-3. There is no looping of data. Both testers must generate data that matches bit for bit. Selections on the Line Setup and BERT Setup screens let the user control the pattern of information bits, the number of information bits allotted to a character, the stop bits used along with a start bit to frame each character (async only), and the sync characters necessary for locating (and relocating) the beginning of a fox or user-defined pattern.

The two-tester configuration can be thought of as two separate one-way tests. From the point of view of each tester, the transmitted BERT data is superfluous. The data that is received and analyzed is the test data.

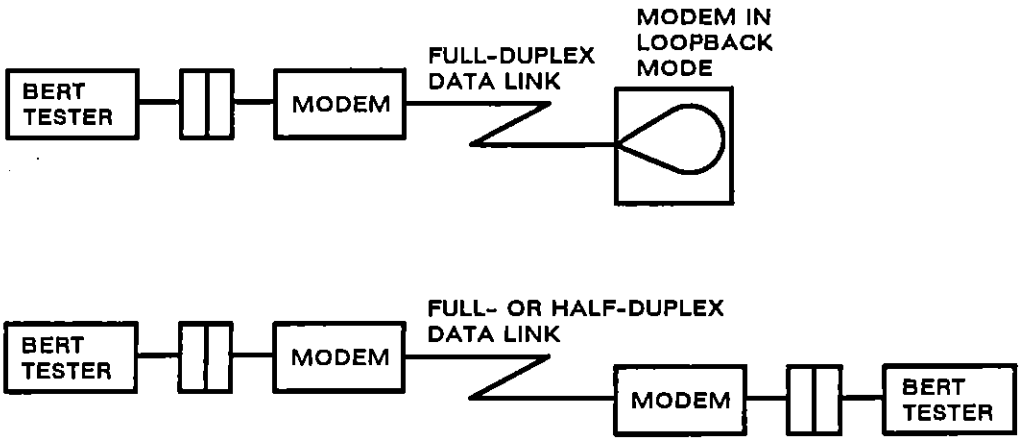


Figure 11-3 Two test configurations: loopback and two-tester.

11.3 BERT Operation: Full Duplex

When the test-interface module (TIM) for RS-232/V.24 is locked in place in the slot at the rear of the unit (see Section 1), the RS-232 subset of parameters on the BERT Setup screen is enabled automatically. On the RS-232 Interface Control menu, RTS, CTS, and CD all should be set to ON for full-duplex operation.

In the **Mode** field on the Line Setup menu, select either BERT DTE or BERT DCE. BERT is used most commonly to test modems and transmission links, so the normal attitude of the INTERVIEW will be **Mode:** BERT DTE. See Figure 11-4.

> *CAUTION: As soon as the INTERVIEW is run in either of its BERT modes, it will interfere with any active communications on the interface. Be sure that it is all right to break the line and transmit test data on it.*

Note on synchronous and BOP operation: The INTERVIEW can transmit using internal clock (SCTE) when it is emulating a DTE; but in order to display its own transmit data as well as receive data, it must be connected to a modem or other DCE device that is providing SCT and SCR clock.

If you have selected **Mode:** BERT DTE and external clock is not available for synchronous or BOP operation, choose **Clock Source:** INTERNAL and patch SCTE to SCT.

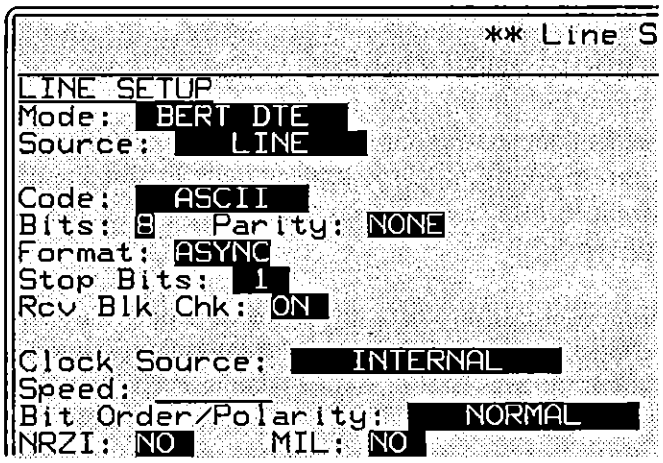


Figure 11-4 The fields on this Line Setup menu—except for *Source*, *Rcv Blk Chk*, and *NRZI*—also are BERT parameters.

Once you have selected the BERT mode, press PROGRAM, F1, F5, to enter the BERT Setup parameters menu (Figure 11-5). Select **Handshake:** FULL DUPLEX in the second field on this menu. When you have completed your other selections in these parameter fields (see Section 11.5), press RUN. In full-duplex testing, whenever you execute a run the INTERVIEW will begin to operate both as a BERT generator and analyzer.

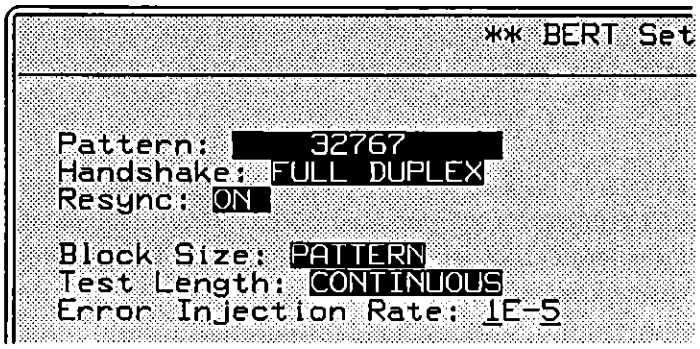


Figure 11-5 BERT Setup screen.

The unit will begin transmitting immediately. The transmission will consist of the bit pattern chosen on the BERT Setup menu according to the format entered on the Line Setup menu.

The INTERVIEW also begins immediately to perform a BERT statistical analysis on all received data. If you press [F3], RESET, while the pattern is being transmitted, the pattern will not be interrupted but the statistical counters will clear. See Section 11.7(E).

11.4 BERT Operation: Half Duplex

To operate over half-duplex transmission lines, go to the RS-232/V.24 Interface Control screen (press [PROGRAM], [F1], [F2]) and change the handshaking control leads (**RTS**, **CTS**, and **CD**) from ON to SWITCH. On the BERT Setup menu, select **Handshake:** HALF DUPLEX.

During the test you will transmit data one block at a time. (See Section 11.5(F) for a definition of "block.") After every block of information that it transmits, the INTERVIEW will drop its control lead and relinquish the data link while the remote tester transmits a block.

On the Line Setup menu, select **Mode:** BERT DTE. Then press [PROGRAM], [F1], [F5], to enter the BERT Setup screen. When you have made your selections in these BERT-menu fields (see Section 11.5), press [RUN].

CAUTION: As soon as the INTERVIEW begins running in either of its BERT modes, it will interfere with any active communications on the interface. Be sure that it is all right to break the line and transmit test data on it.

When the INTERVIEW operates in half duplex, it does not transmit and receive BERT data at the same time. When you send the Run command to start the test, the unit is in the "receive and analyze" mode. Once it has received a complete block of data, it will shift to "generate" mode and transmit *one* block automatically.

In this situation, both ends are waiting; press [F5], START, to initiate the sending-receiving cycle with a transmission.

11.5 BERT Setup Screen

(A) Pattern

With the cursor in the **Pattern** field, press [Roll Up] and [Roll Dn] to rotate between a series of alternating 1's and 0's, a canned fox message, a user-assigned message of up to 259 characters, and five different pseudorandom bit patterns. The INTERVIEW both transmits and expects to receive this pattern while it is in BERT Mode.

When MESSAGE BUFFER is selected in this field, the pattern will consist of the contents of the 259-byte message buffer represented by five data-entry lines toward the bottom of the BERT Setup menu.

Do not run the 1010 pattern if you have selected ASYNChronous (or ISOChronous) start-stop framing on the Line Setup menu.

(B) Handshake

In this field, select **Handshake:** FULL DUPLEX or HALF DUPLEX. The selection will determine whether preamble and sync characters can be appended to the data (half duplex) and whether the resync function can be enabled (full duplex only). In Run mode, the full-duplex pattern will run continuously for the duration of the test, while the half-duplex test will be transmitted one block at a time before turnaround. This field configures the test sequence, not the interface. The interface must be configured on the Interface Control screen in accordance with Table 11-1.

Table 11-1
Full- or Half-Duplex BERT
(RS-232/V.24 Interface Control screen)

	RTS	CTS	CD
Full duplex:	on	on	on
Half duplex:	switch	switch	switch

(C) Resync

Use the resync function to prevent one missed bit-time from skewing an entire test. **Resync:** ON is valid only when the screen is configured for full duplex. This selection allows you to go out of test-sync after a fault has been detected (see Section 11.9(G), Number Of Faults) and back into synchronization after a short interruption. When out of sync, the receiver stops analyzing bits and counting errors and waits for synchronization to turn the analyzer on again.

Resync: ON avoids a bit-error rate approaching fifty per cent for pseudorandom patterns over a long error count. (The analyzer will "guess" right fifty per cent of the time even if it is out of sync with the incoming test data.)

Table 11-2
BERT Pattern (BERT Setup screen)

PATTERN:	BERT ALGORITHM (63, 511, 2047, 4095, 32767)	ALT-1/0 (synchronous only)	FOX/MSG BUF
Handshake:	Full or half duplex	Full or half duplex	Full or half duplex
Resync on:	Algorithm (full duplex) or sync chars (switched)	1010 (full duplex) or sync chars	one or two sync chars
Preamble char:	selectable (switched line-use only)	selectable (switched line-use only)	selectable (switched line-use only)
Sync chars:	1st pattern-byte selectable, switched line-use (half duplex) only	selectable, switched line-use (half duplex) only	selectable
Block size:	1 Kbit, 10Kbit, or pattern	1 Kbit or 10 Kbit	1 Kbit, 10 Kbit, or pattern
Test length:	selectable # of seconds or blocks; 1 K, 10 K, 100 K, or pattern # of bits; or continuous	selectable # of seconds or blocks; 1 K, 10 K, 100 K, or pattern # of bits; or continuous	selectable # of seconds or blocks; 1 K, 10 K, 100 K, or pattern # of bits; or continuous
Error Injection Rate:	selectable	selectable	selectable

For a pseudorandom pattern, resync means going out of sync and performing the algorithm on two bytes of data in order to predict the third byte. Since the algorithm may be performed at any point in the cycle, there are no sync characters.

For the fox pattern or the user-defined message buffer, resync means going out of sync when a fault occurs and looking bit by bit for the sync pattern entered in the **Sync Pattern** field on the BERT Setup (not the Line Setup) menu.

In half-duplex BERT testing, **Resync:** ON is not available. The analyzer goes out of synchronization at the end of each block when the line turns around, but never in the middle of a block.

A fault in half duplex means that synchronization was missed entirely for a block. The analyzer stays out of sync until the next line turnaround.

On a noisy circuit, a fault may not imply that the analyzer has lost synchronization with the incoming BERT pattern. In spite of a high error rate, the test should remain in sync. Select **Resync:** OFF to prevent the analyzer from going out of sync and suspending its error count while waiting to resynchronize.

(D) Preamble

This selection is enabled when the BERT Setup menu is configured for half duplex only. One or two bytes selectable by the user can be prefixed to the sync pattern in half duplex tests. The default entry in this field is two bytes of ^{5}s, a character with an alternating pattern of 0 and 1 bits. After line turnaround, a modem can use this pattern from a remote DTE to put its bit clock into phase with the new carrier.

Since preamble characters always follow carrier turnaround and precede synchronization, they are not checked by the BERT analyzer for error.

Pressing CLEAR to blank this field will prevent the preamble pattern from being transmitted.

(E) Sync Pattern

Sync characters have a special role in BERT testing. Because they provide message synchronization as well as character sync, BERT analysis requires sync characters in line setups where they would not normally occur—in asynchronous fox-pattern testing, for example. To cover these special applications, the BERT Setup screen is provided with its own **Sync Pattern** field. The **Sync Char** field on the Line Setup menu is inoperative during BERT tests.

1. *Sync characters in fox or user-defined tests.* Default is $^{5}s^{5}s$ in the four-character **Sync Pattern** data-entry field. Alphanumerics, control

characters, and hexadecimals are legal. Entry of one, two, three, or four characters is legal. A blank field is treated as default: %%.

In full-duplex BERT tests, sync characters precede each fox message or user-defined message. In normal synchronous data transmission, sync characters help the receivers locate character boundaries. In BERT tests they do more: they help the analyzer find message boundaries. For this reason, sync characters precede fox and user messages in asynchronous tests as well as synchronous.

In a full-duplex fox or user test with few errors, the sync pattern is transmitted repeatedly but used only once by the analyzer. After initial synchronization, the analyzer stays in sync and does not look for the sync pattern. The sync characters that precede each successive message in the test are treated as data and checked for bit errors.

In half-duplex BERT, the sync characters precede every transmission in fox and user tests. They are not repeated in mid-transmission. They never are treated as data.

BERT testing can be tricky when two different brands of tester are being used, especially when a data pattern is being tested. Even fox messages will vary with different testers. Some use STX-ETX, some say "JUMPED . . . DOGS" instead of "JUMPS . . . DOG," and so on. Design a MESSAGE BUFFER test to mirror the fox message of the other tester. Use the **Sync Pattern** field for the first character (or more) of the fox message ("%," for example, or "T") in cases where the other tester does not send %%. Then continue the message on the first line of the **Message Buffer**. Figure 11-6 shows how the **Sync Pattern** field is used in conjunction with the message buffer to design a customized fox pattern.

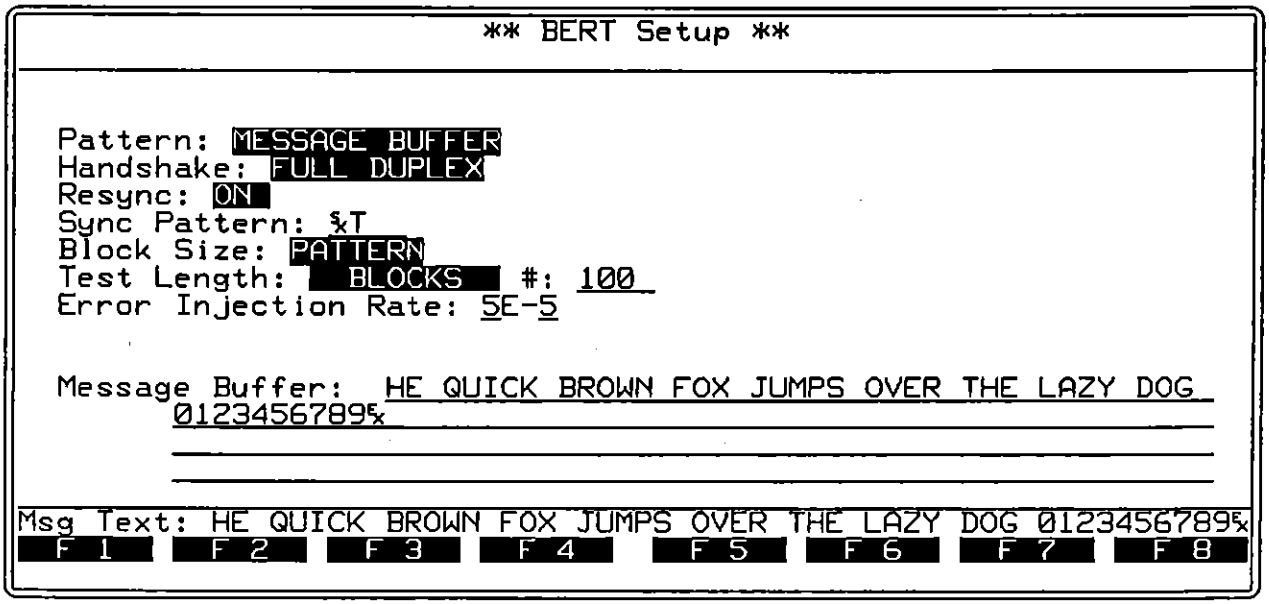


Figure 11-6 If the other tester does not send *sy sy*, synchronize on the first two characters he does send.

2. *Pattern-synchronization in pseudorandom tests.* For a pseudorandom pattern in full duplex, the **Sync Pattern** field does not apply. Since the algorithm may be performed at any point in the cycle, there are no sync characters.

   Synchronization for half-duplex pseudorandom tests is more complicated. The first few bits received after the line turns around are important bits to be tested. Both the transmitting and receiving testers must agree in advance on the point in the algorithmic series where the half-duplex test will begin.

   Here the **Sync Pattern** field is used not for standard sync characters but rather to identify the point in the pseudorandom pattern where the test will begin after each line turnaround. This special use of the **Sync Pattern** field allows the operator to program the INTERVIEW for compatibility with half-duplex testers from other manufacturers.

   To program a synchronization point into a half-duplex test, the user must know the eight bits that precede the point and the eight bits that follow. For example, suppose that the eight bits preceding a sync point in a 2047-bit test are 10100001.

   NOTE: In the notation above, the first bit transmitted is the rightmost. This is consistent with the presentation of binary patterns in all INTERVIEW screen-displays and documents. This

right-to-left ordering of bits is well suited to binary-to-hexadecimal and binary-to-ASCII/EBCDIC conversions; but the usual presentation of bits in the BERT literature is left to right.

Since this binary pattern corresponds to the hexadecimal number $^{A}_{1}$, the user would move the cursor to the **Sync Pattern** field and enter $^{A}_{1}$ in the first data-entry position. Suppose also that the eight bits following the sync point (and therefore the first eight bits transmitted after line-turnaround) are 01001000 (hex $^{4}_{8}$). The user enters $^{4}_{8}$ in the second position of the **Sync Pattern** field. Figure 11-7 shows the full pattern-sync entry.

$^{4}_{8}$ will be the first character transmitted in the half-duplex 2047-bit test. Since some algorithms are based on strings longer than eight bits (see Figure 11-2), the preceding character ($^{A}_{1}$) was included in the **Sync Pattern** field; but this character is not transmitted.

When it is receiving and analyzing, the test synchronizes on the character in the second position in the **Sync Pattern** field ($^{4}_{8}$ in our example). If there is an error in one of these first eight bits, synchronization will be missed and the test will record a "fault." See Number Of Faults, Section 11.9(G). Following the sync character, erroneous bits are recorded as BIT ERRORS.

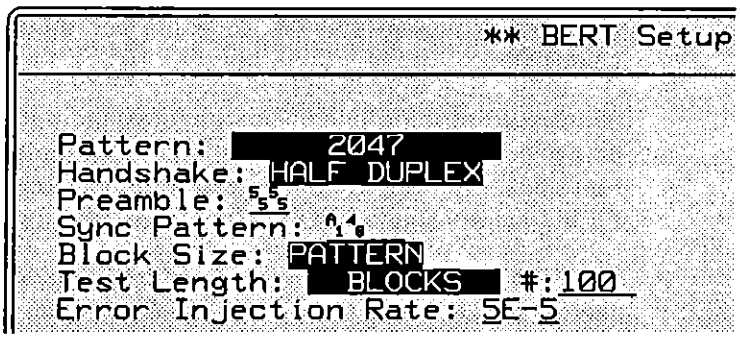


Figure 11-7 Pseudorandom tests in half duplex require pattern-synching.

In certain cases, two bytes of sync may be insufficient to begin a half-duplex pseudorandom test. The 32767 pattern, for example, requires fifteen bits to calculate the sixteenth bit and succeeding bits. If **Bits:** 8 is selected on the Line Setup screen, a two-byte entry in the **Sync Pattern** field is sufficient. But if a smaller bit-number is selected, two hex characters in the **Sync Pattern** field will not represent the number of bits that the algorithm requires to continue.

In such cases, use the four places in the **Sync Pattern** field (in conjunction with the bit number in the Line Setup) to construct a pattern that is at least

as long as the algorithmic series (see Figure 11-2). The last character in the pattern will be the first byte transmitted and analyzed.

3. *Default pattern–sync.* There are two default sets of half–duplex sync points in the INTERVIEW. These are outlined in Table 11-3. BERT testers that use set #1 include the TREND *Data Tester 100* series. NAVTEL's *Datatest II Plus* uses default set #2.

   To operate with sync-point set #1, enter $^{S}Y^{S}Y$ in the **Sync Pattern** field. To operate with set #2, clear the field (press CLEAR). If fewer than two characters are entered in the **Sync Pattern** field, the unit will default to set #2. Remember that the default sets are enabled only when **Handshake:** HALF DUPLEX is selected.

Table 11-3
Half-Duplex BERT: Default Synchronization Points

Pattern	1st 8 Data Bits Transmitted	Preceding 8 Bits In Pattern	Entry In Sync Chars Field
Set #1			
63	$^{A}3$	$^{0}0$	$^{S}Y\ ^{S}Y$ or $^{0}0\ ^{A}3$
511	$^{9}6$	$^{A}1$	$^{S}Y\ ^{S}Y$ or $^{A}1\ ^{9}6$
2047	$^{9}6$	^{B}D	$^{S}Y\ ^{S}Y$ or $^{B}D\ ^{9}6$
4095	$^{5}7$	$^{A}1$	$^{S}Y\ ^{S}Y$ or $^{A}1\ ^{5}7$
32767	$^{9}6$	^{F}F	$^{S}Y\ ^{S}Y$ or $^{F}F\ ^{9}6$
Set #2			
63	^{B}C	$^{A}3$	no chars or $^{A}3\ ^{B}C$
511	$^{9}6$	$^{A}1$	no chars or $^{A}1\ ^{9}6$
2047	$^{4}0$	$^{A}1$	no chars or $^{A}1\ ^{4}0$
4095	$^{5}7$	$^{A}1$	no chars or $^{A}1\ ^{5}7$
32767	$^{9}6$	^{F}F	no chars or $^{F}F\ ^{9}6$

(F) Block Size

A block can be the length of a cycle or message (PATTERN), or 1000 or 10000 bits rounded to the nearest byte. A block is a component of a test: complete tests often are measured in blocks.

CAUTION: The definition of a block varies from standard to standard and from BERT tester to BERT tester. Some standards

define a block as the pattern length while others specify 1,000 bits. The user must ascertain and then select the proper definition.

When a FOX MESSAGE or MESSAGE BUFFER pattern is chosen, PATTERN means one fox message or one message buffer. The PATTERN selection is not valid for the ALT 1010 pattern: a block in this pattern always is a set number of bits.

When a pseudorandom pattern is chosen, the message is one cycle of the pattern. The shortest pseudorandom block is 63 bits, while the longest block is 32,767 bits.

In half-duplex BERT, each transmission is one block. The line turns around following each block. After turnaround, the test continues.

(G) Test Length

Tests are measured in blocks, bits, or seconds. They can also be CONTINUOUS.

The **Test Length:** BLOCKS selection brings up a four-digit # field that accepts entries from 1 to 9999. The shortest pseudorandom block is 63 bits, so the shortest pseudorandom test that is one block long is also 63 bits. The longest test measured in blocks will be 9999 times the longest pattern (32,767), or 327,637,233 bits.

The **Test Length:** SECONDS field also brings with it a # field, with five places for numbers from 1 to 99,999. The maximum number of seconds comes to slightly more than twenty-seven and three-quarter hours.

If **Test Length:** BITS is selected, a # field appears with these rotating selections: 1000, 10000, 100000, and PATTERN.

(H) Automatic Error Injection

Errors can be injected in a bit pattern automatically at a preselected rate. (They may also be injected manually from the keyboard: see Section 11.7 below.) The **Error Injection Rate** field defaults to 5E-5, equivalent to 5 errors per 100,000 bits. The two fives are variables in this formula. The first five is the error rate and can be overwritten with numbers in the range of 0-9. The second five is the **negative exponent** and can be changed to any number in the range of 2-9.

Read the "E-" in the formula as *per 10-to-the-exponent bits*. For example, 1E-2 means $1/10^2$ or 1 error per 100 bits. 0E-6 means $0/10^6$ or no errors per 1,000,000 bits, equivalent to zero. Using 0 as the first variable is equivalent to injecting *no* errors and, in effect, disabling the field.

The highest automatic-error rate selectable would be 9E-2 or $9/10^2$ or 9 errored bits per 100 bits. The lowest rate of injected errors would be 1E-9 or $1/10^9$ or 1 error per 1 billion bits.

11.6 Transmission Format: Line Setup Menu

Certain selections on the Line Setup menu will affect the pattern of bits transmitted during a BERT test. The screen is illustrated in Figure 11-4.

(A) Code

If your BERT pattern is a fox message or a user-defined message that contains alphanumerics, the **Code** that you select on the Line Setup menu will affect the pattern of bits in your test. If your test involves sync characters, remember that the bit pattern for %% is different for ASCII and EBCDIC.

Testers on either side of a transmission link should be configured for the same code.

(B) Bits

Select the number of information bits. This field is invalid for pseudorandom and alternating 1/0 BERT patterns in SYNC format. In all other BERT configurations, characters are formed according to the bit-number specified here.

(C) Parity

For 5, 6, or 7 information bits in async or isoc format, you may select the type of parity. (For 8 information bits, even, odd, or no parity is available in async or isoc format. Eight bits plus mark or space parity is not available in any format.) The parity bit is additional to the information bits.

The BERT test transmits and checks parity. It calculates parity on the data bits it *expects* to receive, not the actual data bits. This is to prevent an errored data bit from causing a parity error and being counted twice as a result.

(D) Format

Choose **Format:** SYNC, BOP, ASYNC, or ISOC.

1. *Sync.* If **Format:** SYNC is selected on the Line Setup menu and a pseudorandom (or alternating 1/0) pattern is the BERT Setup selection, the pattern will be transmitted bit for bit without synchronization or character-framing. The Line Setup selection fields from **Code** down to (but not including) **Bit Order/Polarity** are invalid.

   If a character-oriented (fox or message-buffer) pattern is selected on the BERT Setup screen, the precise bit pattern will be determined partly by the

Code, Bits, and **Parity** selections on Line Setup. The fields from **Format:** SYNC down to **Bit Order/Polarity** are invalid for BERT, however. Sync characters are entered on the BERT Setup screen. See Section 11.5(E).

2. *BOP.* This softkey is nonfunctional. The selections default to the same as if **Format:** SYNC were selected.

3. *Async.* If **Format:** ASYNC is selected on the Line Setup menu, stop bits (ones) and a start bit (zero) will be added after every fifth, sixth, seventh, eighth, or ninth bit in the BERT pattern, depending on the **Bits** and **Parity** selections on Line Setup. This start/stop-bit framing applies to pseudorandom patterns as well as to character-oriented patterns.

   Do not run the alternating 1/0 pattern if you have selected asynchronous (or isochronous) start/stop-bit framing on Line Setup.

4. *Isoc.* This is a cross between async and sync. It uses asynchronous start/stop-bit framing; but unlike async, internal clock (if selected) will transmit clock pulses on the clock lead(s) for use by the other device on the interface.

(E) Clock

If clock is to be supplied by a modem during the test, you can select **Clock:** EXTERNAL. If no external clock is to be supplied, select INTERNAL or INTERNAL SPLIT and the correct speed or speeds.

> **Note on synchronous and BOP operation:** The INTERVIEW can transmit using internal clock (SCTE) when it is emulating a DTE; but in order to display its own transmit data as well as receive data, it must be connected to a modem or other DCE device that is providing SCT and SCR clock.
>
> If you are have selected **Mode:** BERT DTE and external clock is not available for synchronous or BOP operation, choose **Clock Source:** INTERNAL and patch SCTE to SCT.

(F) Bit Order/Polarity

The pattern of bits in sync and async tests will be affected by the selection in the **Bit Order/Polarity** field only if a character-oriented (fox or message-buffer) pattern is selected on the BERT Setup screen.

Table 11-4
Sync or Async BERT (Line Setup screen)

FORMAT:	SYNC	ASYNC	ISOC
Mode:	BERT DTE or BERT DCE	BERT DTE or BERT DCE	BERT DTE or BERT DCE
Code:	EBCDIC, ASCII, EBCD, XS-3, IPARS, SELECTRIC	EBCDIC, ASCII, EBCD, XS-3, IPARS, SELECTRIC	EBCDIC, ASCII, EBCD, XS-3, IPARS, SELECTRIC
Bits:	8, 7, 6, or 5	8, 7, 6, or 5	8, 7, 6, or 5
Parity:	none	none, even, or odd; mark or space (except 8 bits)	none, even, or odd; mark or space (except 8 bits)
Stop bits:	N/A	1 or 2	1 or 2
Clock source:	external, internal, or internal split	internal or internal split	external, internal, or internal split
Speed:	selectable (except external)	selectable	selectable (except external)
Bit order/polarity:	normal, rev-nor, nor-inv, rev-inv	normal, rev-nor, nor-inv, rev-inv	normal, rev-nor, nor-inv, rev-inv

11.7 Run Mode: Keyboard Control

Whenever you press [RUN], the INTERVIEW will begin to operate as both a BERT generator and analyzer.

It will begin immediately to transmit the bit pattern chosen on the BERT Setup menu according to the format entered on the Line Setup menu. The pattern will repeat until the test ends: see Test Length, Section 11.5(G).

(A) Freezing the Test

The pattern can be interrupted from the keyboard. Pressing [PROGRAM] or [FREEZE] will drive the analyzer out of sync and stop the counters. Freeze mode retains the latest results display on the screen (Figure 11-8). Hitting [FREEZE] a second time will unfreeze the analyzer and resume the count from the frozen readings.

(B) Restarting the Test

The [FREEZE] key restarts a frozen test.

To restart a test while it is running, use the F4 softkey, labeled RESTART. This restart also reinitializes the synching process. To clear and restart the counters, press F3, RESET. Softkey selections in Run mode are illustrated in Figure 11-8.

Hitting PROGRAM and RUN will also restart everything—test, synching process, and counters.

(C) Manual Errors

You may introduce errors into the BERT transmission one at a time via softkey. One errored bit will be sent each time the operator presses F1 (INJ1ERR).

(D) Automatic Error Injection

Automatic error-injection can be turned on and off by softkey. Press F2, ERR INJ, to toggle this function. See Section 11.5(H), for an explanation of error rates.

(E) Clearing the Results Screen

To clear the counters without losing sync, press F3, RESET.

(F) Restarting the Test Function

The test function length was determined on the BERT Setup screen to be measured in blocks, bits, or seconds, or to run continuously. Pressing F4, RESTART, restarts the test and reinitializes the synching process.

(G) Disabling Transmission

You may prevent the BERT pattern from being transmitted while the INTERVIEW analyzes a received pattern. If the unit is in BERT DTE mode, move the breakout switch for pin 2 on the test-interface module (TIM) to the open position. If the unit is in BERT DCE mode, open pin 3 instead.

11.8 Run Mode: Status Line

The status line of the Run-mode BERT display, shown in Figure 11-8, identifies the BERT test and the parameters chosen on the Line Setup menu. The INTERVIEW is using these parameters both to transmit and to analyze. Figure 11-8 shows a BERT 511 test in EBCDIC code; with 8 information bits, no parity, and full duplex pattern; and in synchronous mode.

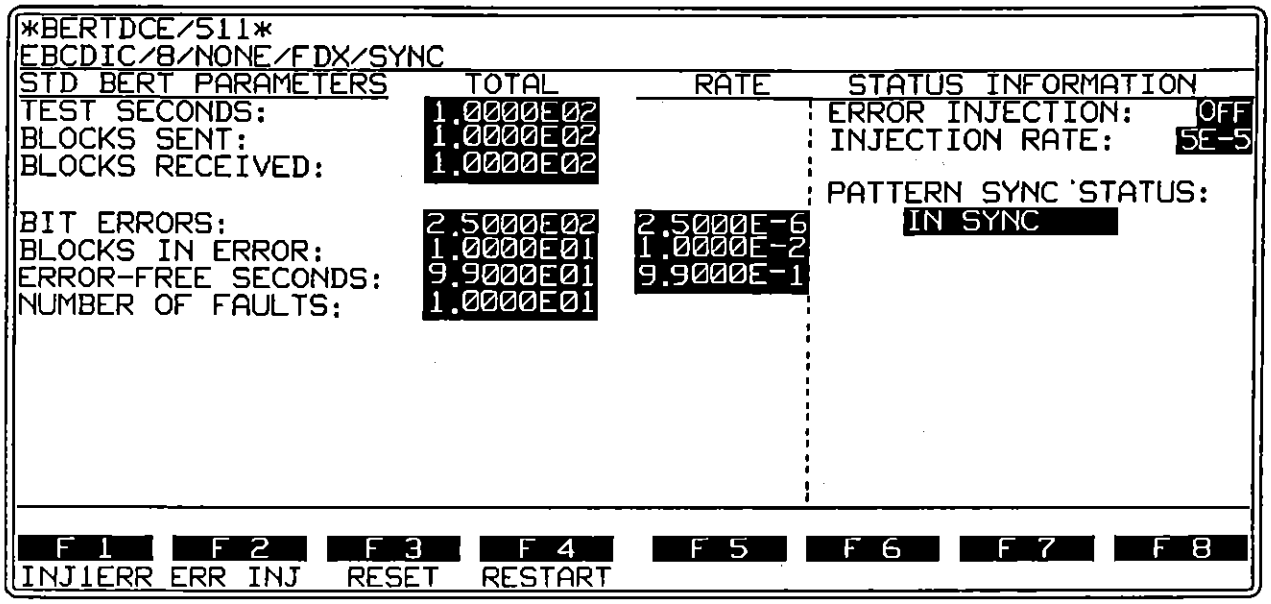


Figure 11-8 The BERT Results screen displays setup status, receiver-sync status, error injection rate, seven counters, and three rate calculations.

11.9 Run Mode: Statistical Display

BERT counters increment to $2^{64}-1$, or approximately 1.8 times 10^{19}. For practical purposes these counters are unlimited.

Each counter enters Run mode at 0.0000E00. The top of Figure 11-9 shows the block counter on the verge of rolling over to a new exponential value. The bottom of the figure shows the effect of the next block received: the exponent has incremented so that the counter is being updated on every tenth count instead of every one. The counter will be updated next when ten new blocks have been received.

Figure 11-9 This is a before-and-after illustration of the block counter receiving its 100,000th block.

Three of the counters have Rate displays adjacent to them. See Figure 11-8. These rates are to be read in the same way you would read an entry in the **Injection Rate** field on the BERT Setup menu (see Section 11.5(H)): 9.0000E-3 means 9 times

$1/10^3$ or 9 errors per 1,000 bits. Rates are displayed in real time. They enter Run mode at 0.0000E-0 and remain at zero until a bit error or block error or errored second occurs. Once an error rate is posted, the displays will behave like decrementing counters: while the number of bits, blocks, or seconds increases steadily, the rate of error will decrease. The top of Figure 11-10 shows a Rate display for bit errors that stands at 1.0000E-4 or 1 error per 10,000 bits. When the next bit arrives, unless it is an error the rate will decrease. The bottom of the figure shows the action of the display as the rate of error decreased: 1 per 10,000 became 9.9999 per 100,000 (9.9999E-05).

Figure 11-10 As the rate of error decreases, the minus-exponent grows larger.

(A) Test Seconds

This counter is incremented once for every second the test runs.

(B) Blocks Sent

The current number of blocks sent is recorded here. A block is defined in Section 11.5(F).

(C) Blocks Received

This shows the current number of blocks received. If this count is not incrementing, the INTERVIEW is not synching on a pattern and the PATTERN SYNC STATUS field on the lower right of the BERT statistical display screen should say OUT OF SYNC.

(D) Bit Errors

The bit sequence received is compared with that expected in accordance with the parameters chosen on the Line Setup menu and the BERT Setup screen. The count of received bits that do not match the expected pattern is displayed here. This counter value in relation to total bits is given in the Rate column at the right of the counter, expressed in errors per exponent of 10.

(E) Blocks In Error

The number of blocks in which one or more bit errors have occurred is recorded. A rate calculation of this value to total blocks received is given to the right of the counter in real time.

> NOTE: If two testers are being used, verify that both are defining block size in the same way. See Section 11.5(F).

(F) Error-Free Seconds

This counter will increment when the Test Seconds counter increments until one or more errors have been found during the last second. The rate of this counter value compared to total seconds is given to the right of the counter in real time.

(G) Number Of Faults

"Fault" has different meanings for full and half duplex. In full duplex, a fault is recorded whenever an error is detected in more than 25 percent of the bits received over a certain period of time (approximately 16 bits in 64 contiguous bits). This percentage is considered sufficient to indicate that a bit time has been missed.

In full duplex, if **Resync:** ON has been selected on the Transmit Mode menu the INTERVIEW's receiver will resynchronize every time a fault is found.

In half duplex, a fault occurs when the analyzer sees bit transitions that indicate a new block of BERT data but fails to recognize the sync pattern or the sync character.

(H) Error Injection

The status of Error Injection may be ON or OFF; it is toggled manually by the ERR INJ softkey. In Run mode it is turned on and off by the F2 softkey.

(I) Injection Rate

This status field simply reports the error-injection rate that the user has entered on the BERT Setup menu.

(J) Receiver

BERT analysis begins when the receiver synchronizes on incoming data. The PATTERN SYNC STATUS line on the results screen reports on receiver status. At all times during a BERT run, the line displays one of two messages, IN SYNC or OUT OF SYNC.

Once synchronization is established, the receiver can go out of sync only if **Resync:** ON is selected. During the out-of-sync condition, data is not analyzed for error.

When the resync function is turned off, the IN SYNC condition, once established, will remain in effect until the test ends. This setup is appropriate for relatively brief tests on noisy circuits.

11.10 Loopback at the Transmitting INTERVIEW

The INTERVIEW can analyze its own BERT transmission without being connected to the data interface. This is a good way for you to become familiar with the BERT test procedure before you apply it to a system.

With the interface disconnected, power up the unit and select **Mode:** BERT DCE on the Line Setup menu. Then select a configuration compatible with the specifications in Table 11-2 and Table 11-3. Select internal clock.

Press [RUN]. You will see only the first two counters, Test Seconds and Blocks Sent, incrementing. This is the way the Run-mode display will appear when you are sending the BERT pattern to another BERT analyzer. No statistical analysis is being done because the BERT analyzer is not seeing the transmitted pattern. The report on Receiver status is OUT OF SYNC.

Press [PROGRAM]. On the breakout box on the test-interface module (TIM), patch TD to RD. Press [RUN]. This time you will see the first three counters incrementing: Test Seconds, Blocks Sent, and Blocks Received. The receiver is now IN SYNC. The INTERVIEW's BERT analyzer can see its own transmission but it is unlikely that it will find any errors in its own data.

Use the [F1] key to introduce errors into the transmission. Observe the next three counters and the rate measurements alongside them. The [F1] key will not introduce a fault.

Run another test into which you have injected automatic errors. An **Error Injection Rate** entry of 1E-5 on the BERT Setup screen will produce one errored bit for every 100,000 bits and a bit-error rate of 1.0000E-5.

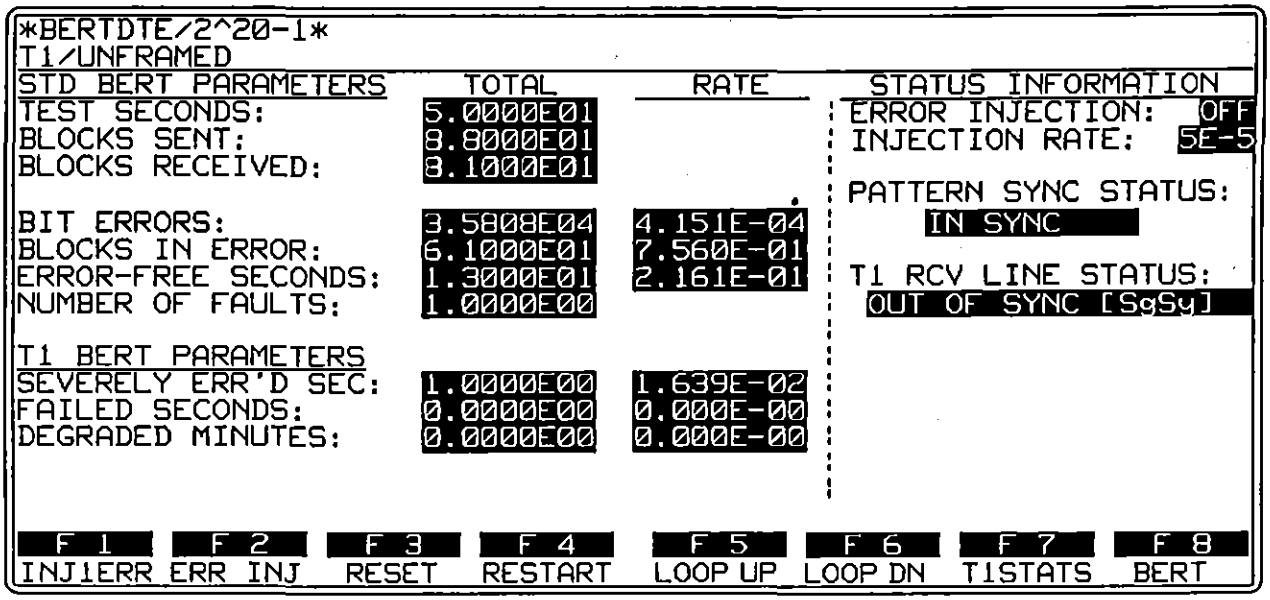


Figure 11-11 T1 BERT Statistics screen.

11.11 T1 BERT

The INTERVIEW can perform both framed and unframed BERT tests on T1 transmissions. An individual channel may also be BERT tested. Tests may be performed in a simple loopback configuration or in conjunction with another INTERVIEW or BERT tester. For further discussion of test configurations, refer to Section 11.2.

A T1 BERT display (see Figure 11-11) tracks test results in Run mode. In addition to T1 BERT testing, statistics are gathered on the quality of the T1 circuit whenever the T1 TIM is installed. These statistics are displayed and constantly updated on a separate screen, which is accessible from the BERT statistics screen during run time. Regular T1 statistics and modifiable selections that pertain to these statistics are described in Section 52.

(A) The T1 BERT Option

T1 BERT capabilities are available as part of the overall T1 option, which consists of a factory-installed multiplexer board and a removable Test Interface Module. If you have T1 BERT installed, Option 11-1 will be displayed on the start-up screen of the INTERVIEW when you turn it on. The TIM posted on the same screen must be T1 (see example in Figure 11-12).

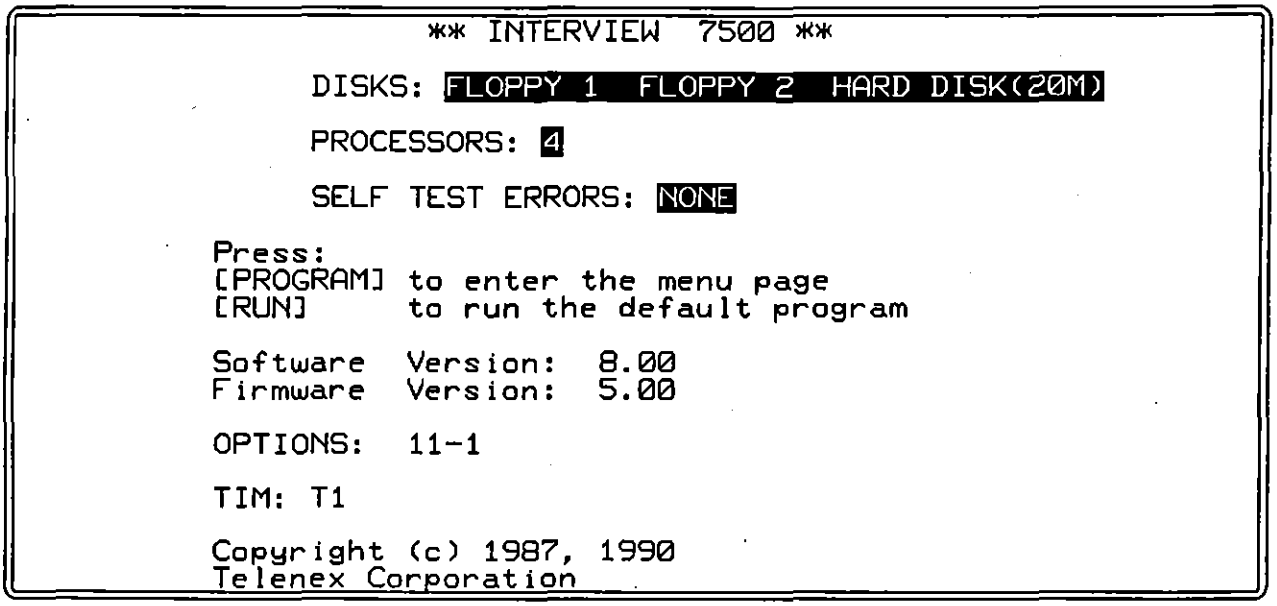


Figure 11-12 Power-up screen, INTERVIEW 7500.

(B) Preparing for T1 BERT Testing

Setting up for T1 BERT requires installation of the correct Test Interface Module, proper cabling, and making menu selections. In addition to the selections made on the BERT Setup screen, certain selections must be checked on the Line Setup screen and the T1 FEB Setup screen.

1. *Install the T1 TIM.* T1 testing can be done only when the T1 TIM, described in Section 52.2, is in place. Before powering up the INTERVIEW, install the T1 TIM as described in Section 1.10.

2. *Cable the T1 TIM.* With the power switch still OFF, connect to a data source as described in Section 52.2(A). When the TIM is in place and cabling is complete, power on the unit.

   Several types of cable may be used for T1 testing. The cable type and its length must be specified on the Line Setup screen, along with other items discussed in the next paragraph.

3. *Configure the Line Setup screen.* Before you run a T1 test, you must configure the Line Setup screen for the type of testing you wish to do. Select **Mode:** BERT DTE if you are operating as a DTE and testing a remote Channel Service Unit (CSU) or a transmission link. Select **Mode:** BERT DCE to test a CSU in local loopback mode.

CAUTION: When the INTERVIEW operates in broadband or normal channel transmit mode, it interrupts the regular exchange of data on the circuit for the duration of the test. Be certain you have permission to test the circuit before you proceed.

NOTE: Clocking of T1 data is not provided by the standard data clock. As a result, the **Clock** selection on the Line Setup screen is overridden. An applicable clock selection is provided on the T1 Interface Control screen and is described in Section 52.5.

NOTE: Channel BERT selections pertaining to half duplex operation are not applicable to T1 BERT.

Make other Line Setup selections as described in Section 11.3.

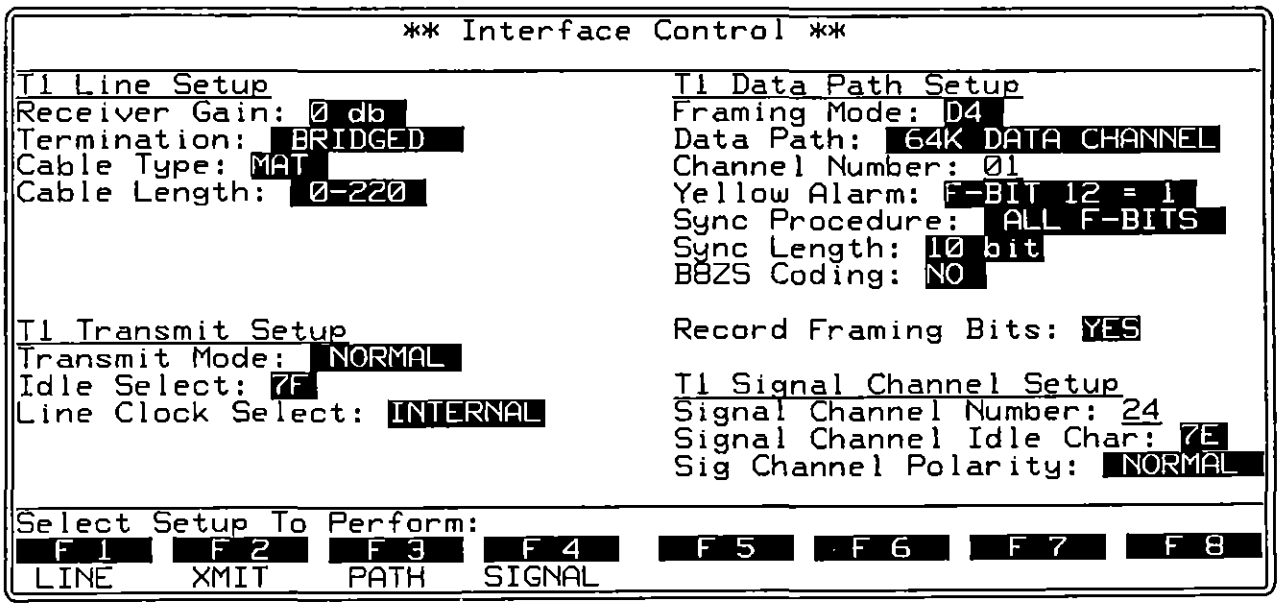


Figure 11-13 Interface Control Screen for T1 Protocol.

4. *Configure the T1 Interface Control screen.* Select the channel to be tested as the **Data Path** and **Channel Number** on the Interface Control screen (see Figure 11-13). T1 framing, syncing, code format, alarm procedures, and cable length are also controlled on the Interface Control screen. The **T1 Signal Channel Setup** fields pertain only to dual-channel T1 Primary Rate ISDN.

Transmit Mode in the T1 Transmit Setup selections pertains only to Channel BERT testing. Only one of the 24 available T1 channels is BERT-tested at one time. This selection determines what will be transmitted to the other channels which are not under test. The choices are NORMAL and DROP-AND-INSERT.

In NORMAL transmit mode, the standard milliwatts pattern of all 1's is transmitted on the 23 remaining channels.

In DROP-AND-INSERT transmit mode, all received channels pass through the INTERVIEW unchanged, with the exception of the channel under test. The specified channel BERT pattern is inserted into this channel in place of the original data.

Use drop-and-insert transmit mode when the INTERVIEW is operating in BERT DCE mode in order to test a T1 mux (using another INTERVIEW to emulate the user DTE).

Use drop-and-insert transmit mode when the INTERVIEW is operating in BERT DTE mode to test Channel Service Units and phone lines.

For more information on normal or drop-and-insert transmit mode, refer to Section 52.5(E).

Make selections on the T1 Interface Control screen as described in Section 52.5.

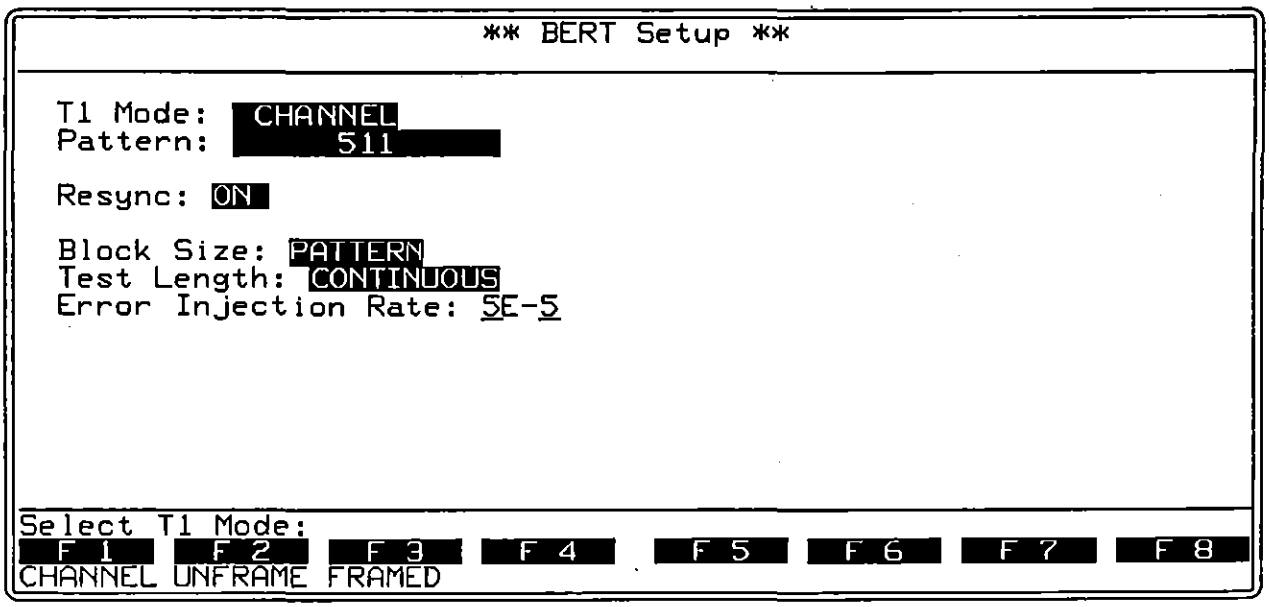


Figure 11-14 The T1 BERT Setup screen.

(C) T1 BERT Setup Screen

The default T1 BERT Setup screen is shown in Figure 11-14. For a full set of options available on this screen, refer to Figure 11-15. As illustrated in Figure 11-15, there are three modes available for T1 BERT testing. These are CHANNEL, UNFRAMED, and FRAMED.

Channel mode is used for single channel testing and may be done transparently (when drop-and-insert mode is used) so that transmissions on other channels experience minimal interruption.

> NOTE: At the instant that you begin running a test which employs the INTERVIEW in drop-and-insert transmit mode, on-going transmissions on all T1 channels on the circuit will be momentarily disrupted. This is true even though the INTERVIEW is already connected into the circuit. The interruption is minimal, however, and is not likely to produce a framing error or resynchronization.

Unframed and framed modes, on the other hand, are "broadband" BERT tests; that is, all channels on the T1 circuit are involved in the test.

1. *Channel mode.* T1 channel mode is similar to *full-duplex* RS-232 BERT testing, with the exception that **Block Size** selections are much larger. For a

full explanation of full duplex BERT operation and for **Pattern, Handshake, Sync Pattern,** and **Resync** selections, refer to Sections 11.3 and 11.5(A) through 11.5(F). T1 block sizes are described later in this section.

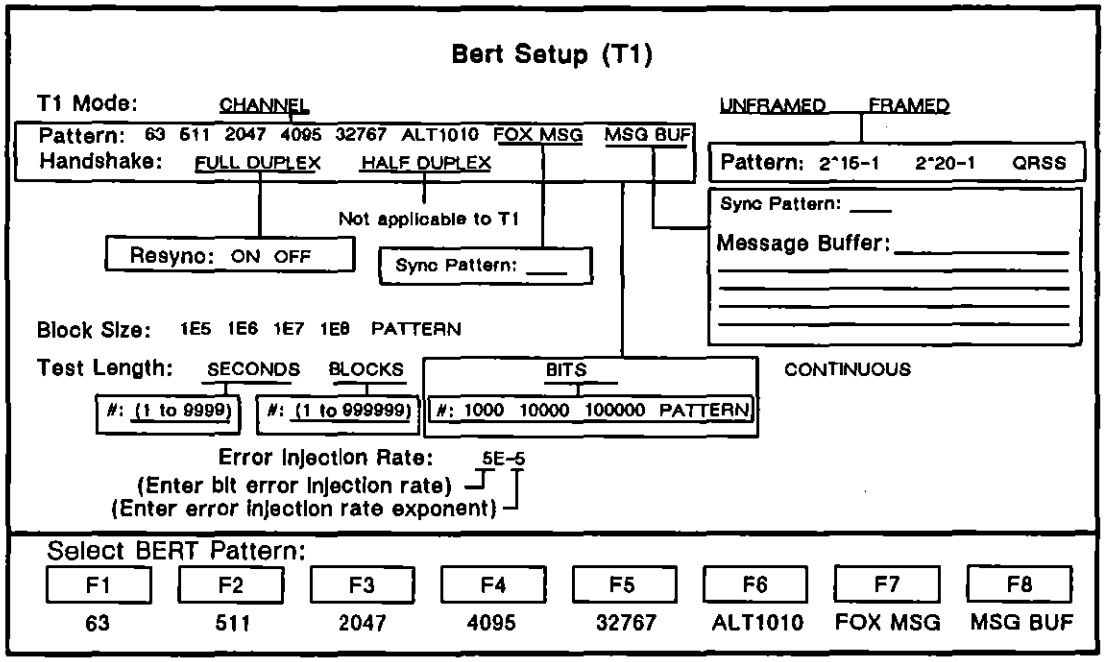


Figure 11-15 T1 BERT menu options.

2. *Unframed T1 BERT mode.* This mode sends the BERT pattern in every T1 bit position. Channel and framing conventions are ignored. When unframed BERT is the T1 mode, three **Pattern** selections are available. These selections are discussed in subsequent paragraphs.

3. *Framed T1 BERT mode.* This mode provides framing bits according to the convention chosen by the user (i.e., D4 or ESF; see discussion in Section 52). These bits are inserted in between (not written over) the BERT pattern during transmission, which means that error injection during the BERT test will never cause a framing error. When framed BERT is the T1 mode, the same three patterns available with unframed T1 BERT may be used (see the discussion in the next paragraph).

4. *Pattern.* The patterns shared by framed and unframed BERT differ from the patterns available with channel BERT. Channel BERT patterns are described in Section 11.5(A).

   For framed and unframed T1 BERT, the three selections in the **Pattern** field are $2^{15}-1$ (which is equivalent to the 32767 pattern and simulates the output

of a 15-bit shift register); $2^{20}-1$ (which simulates the output of a 20-bit shift register); and QRSS (or Quasi-Random Signal Source, which is similar to the $2^{20}-1$ pattern but observes the 1's density prescribed for transmission by suppressing any string of 15 or more 0's.)

5. *Block size.* A block is a component of a test: complete tests may be measured in blocks. In T1 channel BERT, **Block Size:** PATTERN selections are the same as for RS-232 BERT (see Section 11.5(F)); otherwise, the **Block Size** selection is a certain number of bits. Blocks measured in bits (as described in the next paragraphs) are larger for T1 channel BERT than are RS-232 blocks.

   For framed or unframed T1 BERT, a block can be the length of a cycle as indicated by one of the three **Pattern** selections or a certain number of bits.

   T1 block sizes measured in bits are 100,000 (1E5); 1,000,000 (1E6); 10,000,000 (1E7); and 100,000,000 (1E8).

   CAUTION: The definition of a block varies from standard to standard and from BERT tester to BERT tester. Some standards define a block as the pattern length while others specify 1,000 bits. The user must ascertain and then select the proper definition.

6. *Test length.* Tests are measured in blocks or seconds; or they may be CONTINUOUS. In Channel BERT, they may also be measured in bits.

   The **Test Length:** BLOCKS selection brings up a four-digit # field that accepts entries from 1 to 9999. If PATTERN has been selected in the **Block Size** field, the length of the test may be determined by multiplying this figure by the number of bits in the selected test pattern.

   The **Test Length:** SECONDS field also brings with it a # field, with five places for numbers from 1 to 99,999. The maximum number of seconds comes to slightly more than twenty-seven and three-quarter hours.

   The **Test Length:** BITS selection brings up a field that accepts entries of 1000, 10,000, 100,000 or a pattern. If PATTERN has been selected in the **Block Size** field, the length of the test is the number of bits in the selected test pattern.

7. *Error injection rate.* Errors can be injected in a bit pattern automatically at a preselected rate. Refer to Section 11.5(H) for more information on the pre-determined injection rate. Errors may also be injected manually, one-at-a-time, from the keyboard as explained in Section 11.11(E).

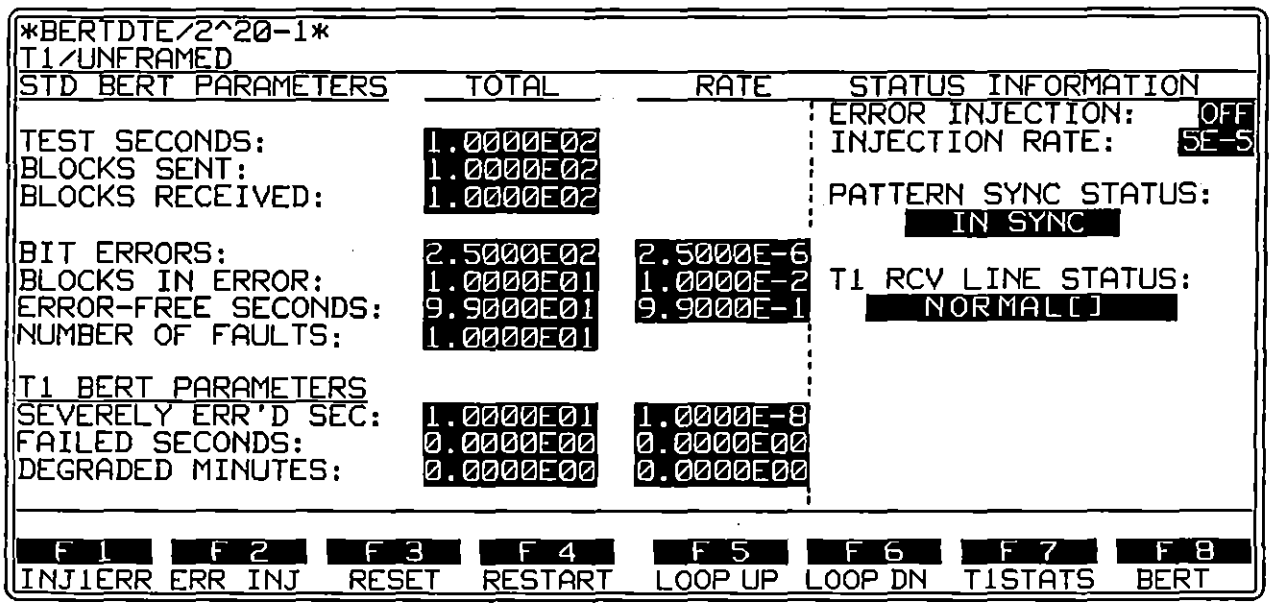


Figure 11-16 Sample T1 BERT Statistics screen in Run mode.

(D) T1 BERT Statistics Screen

As long as a BERT emulation mode has been selected on the Line Setup screen and the T1 hardware options are installed, the T1 BERT Statistics display appears on the screen. An example of the display is shown in Figure 11-16.

The top of the screen shows which side of the line the INTERVIEW is emulating, indicates whether channel, unframed, or framed testing is being done, and gives additional information on test selections.

Certain test status information is tracked at the far right of the screen. The **ERROR INJECTION** field indicates whether or not the operator has turned on automatic injection rate by pressing the appropriate function key during run-time. The **INJECTION RATE** field indicates the programmer's entry for automatic error injection on the T1 BERT Setup screen (see Section 11.5(H)). The **PATTERN SYNC STATUS** (as opposed to the line syncing status) field indicates whether the BERT pattern is in or out of sync (see discussion in Section 11.9(J)). The **T1 RCV LINE STATUS** field reflects the **T1 LINE CONDITIONS** information given on the regular T1 Statistics screen (see Section 52.6(O)).

The remainder of the screen provides constantly updated test statistics. Values for BERT parameters (far left of screen) are posted in highlighted boxes in the center of the screen. In addition to total values, rates (that is, total occurrences

divided by TEST SECONDS) are given in a highlighted box to the right of the totals. All values are measured starting from the last time [RUN], RESET, or RESTART was pressed.

1. *Test seconds.* This indicates the time elapsed since [RUN], RESET, or RESTART was pressed.

2. *Blocks sent.* This value represents the number of blocks which the INTERVIEW has transmitted. Blocks are recognized according to the block size (in terms of bits) or the pattern (one block per complete pattern) as selected in the **Block Size** and **Pattern** fields on the T1 BERT screen.

3. *Blocks received.* This is the number of blocks received from the remote end. These blocks are measured according to the same criteria as the number of blocks sent.

4. *Bit errors.* This value represents the number of individual bits received in error. The number of bits in error divided by the total bits received is posted in the RATE column.

5. *Blocks in error.* This value indicates the number of blocks received in which one or more bits were found to be in error. The rate which appears to the right is the total blocks in error divided by total blocks received.

6. *Error-free seconds.* This value is the number of TEST SECONDS during which no bit error, framing error, CRC error, or bipolar violation was recorded. The rate given to the right is total error-free seconds divided by total TEST SECONDS.

7. *Number of faults.* This is the number of times that the number of bits in error has exceeded 25% for at least 1/50th of a second.

8. *Severely errored seconds.* This is the number of individual seconds during which any of the following occurred: 320 or more Out of Frame conditions or CRC errors (see description in Section 52.6(H) and 52.6(I)); or the bit error rate was worse than 1E-3; that is, 1 X 10^{-3} power. (Ten or more consecutive Severely Errored Seconds constitute a Failed Signal State.)

9. *Failed seconds.* This is the duration of a Failed Signal State in seconds. The tenth consecutive Severely Errored Second is the first Failed Second. A failed signal state lasts until 10 consecutive seconds are *not* Severely Errored Seconds. Thus, there will always be at least 10 failed seconds recorded at one time.

10. *Degraded minutes.* This is the number of minutes during which the bit error rate exceeds 1E-6.

(E) Run-time Function Keys for T1 BERT

The function keys shown in Figure 11-17 appear at the bottom of the T1 BERT Statistics display when the INTERVIEW is running a T1 BERT test. You may access the T1 Statistics screen and the regular BERT screen, both of which are active while a T1 BERT test is in progress, by pressing the appropriate function key. Alternate screens have the same rack of function keys and so allow you to return to the original display.

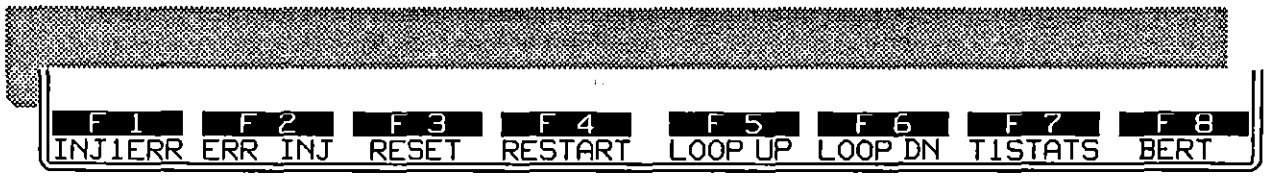


Figure 11-17 Run-time function keys available when performing a T1 BERT test.

1. *Inject one error.* The function key labeled INJ1ERR injects a single bit error into the INTERVIEW's T1 BERT transmission. If this key is used when error injection is on (see next paragraph), the single error is simply added to the automatic error rate.

2. *Error injection at pre-determined rate.* The function key labeled ERR INJ is an alternate-action function key which turns off the automatic error injection; or turns it back on and inserts errors into the T1 BERT transmission at the rate selected on the T1 BERT Setup screen. (See Section 11.5(H) for a description of the selection.) Error injection is off when the INTERVIEW enters Run mode. The **ERROR INJECTION** field at the far right of the screen tells you whether automatic error injection is currently on or off.

3. *Reset.* The function key labeled RESET sets the value of all timers and counters, including T1 counters, to zero. The BERT test continues, however.

4. *Restart.* The function key labeled RESTART is used to initiate T1 BERT testing again, once it has stopped at the point determined by the Test Length selection on the T1 BERT Setup screen. All counters and timers, including T1 counters, and elapsed time (TEST SECONDS) continue from wherever they stopped.

5. *Loop up.* The function key labeled LOOP UP sends a Loop-up command (for a duration of 5.5 seconds) to the remote CSU. This command allows

any pattern of data to be transmitted to the remote CSU for any length of time desired. Assuming that the remote CSU is functioning properly, all data will be looped back on the corresponding return lead thereafter.

NOTE: It is not necessary to send the Loop-up command, however, when the INTERVIEW is troubleshooting the line while remotely connected to another BERT tester.

CAUTION: Do not activate the Make lead on the T1 TIM when a T1 BERT test is in progress. Since the Loop-up signal has already been sent, generating a second Loop-up signal risks locking up all equipment under test and the INTERVIEW in a continuous data loop.

CAUTION: Do not activate the Break lead on the T1 TIM when a T1 BERT test is in progress, since this will interrupt the test in progress. The Loop-down signal can be generated from the T1 BERT screen as explained in the next paragraph.

6. *Loop down.* The function key labeled LOOP DN sends a Loop-down command to the remote CSU (for a duration of 5.5 seconds). This command takes the remote end out of loopback, so that it is capable of responding normally to received data rather than echoing it back without interpretation.

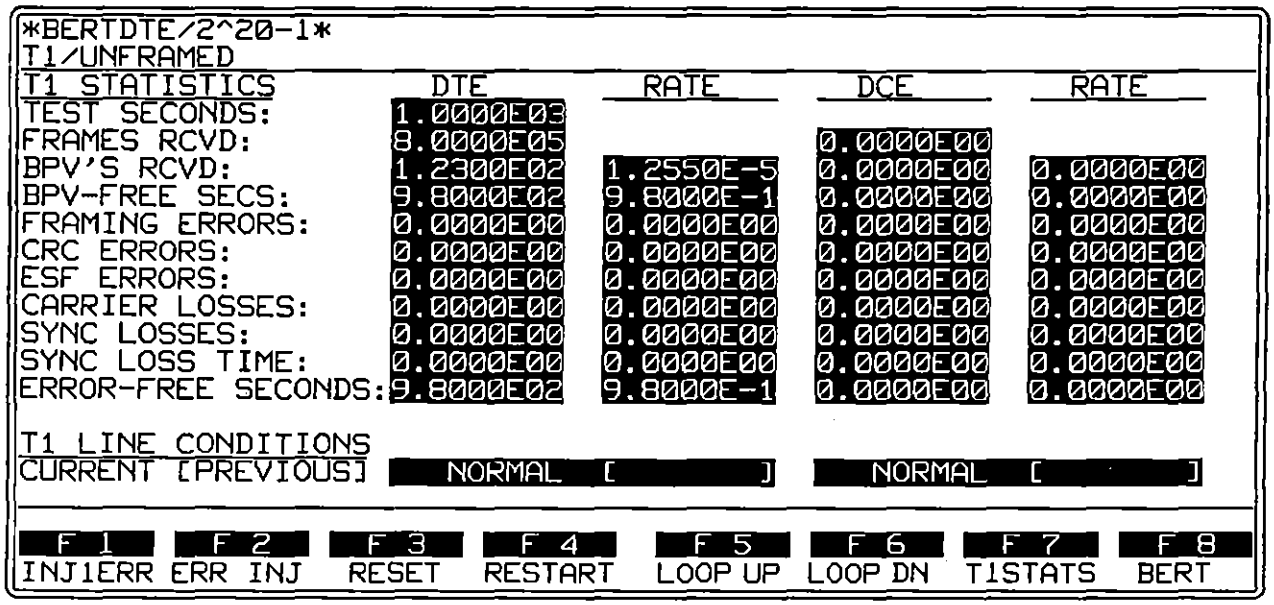


Figure 11-18 The T1 Statistics screen is an alternate run-time screen during T1 BERT testing.

7. *T1 statistics display.* The function key labeled T1STATS changes the INTERVIEW screen to the regular T1 statistics display (see example in Figure 11-18). The contents of this display are described in Section 52.

8. *Regular BERT display.* The function key labeled BERT changes the INTERVIEW screen to the regular BERT statistics display (see example in Figure 11-8). The contents of the regular BERT display are described in Section 11.9. Press the function key labeled BERT again to return to the T1 BERT statistics screen.

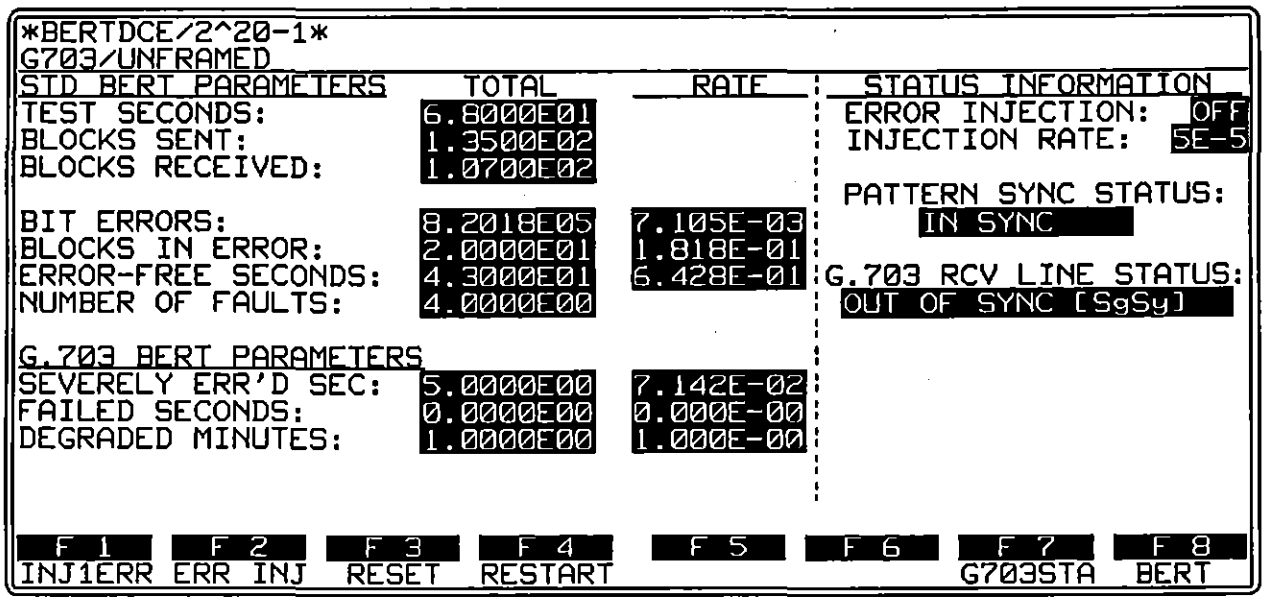


Figure 11-19 G.703 BERT Statistics screen.

11.12 G.703 BERT

The INTERVIEW can perform both framed and unframed BERT tests on G.703 transmissions. An individual channel may also be BERT tested. Tests may be performed in a simple loopback configuration or in conjunction with another INTERVIEW or BERT tester. For further discussion of test configurations, refer to Section 11.2.

A G.703 BERT display (see Figure 11-19) tracks test results in Run mode. In addition to G.703 BERT testing, statistics are gathered on the quality of the G.703 circuit whenever the G.703 TIM is installed. These statistics are displayed and constantly updated on a separate screen, which is accessible from the BERT statistics screen during run time. Regular G.703 statistics and modifiable selections that pertain to these statistics are described in Section 53.

(A) The G.703 BERT Option

G.703 BERT capabilities are available as part of the overall G.703 option, which consists of a multiplexer board and a removable Test Interface Module. If you have G.703 BERT installed, Option 24-1 will be displayed on the start-up screen of the INTERVIEW when you turn it on. The TIM posted on the same screen must be G.703 (see example in Figure 11-20).

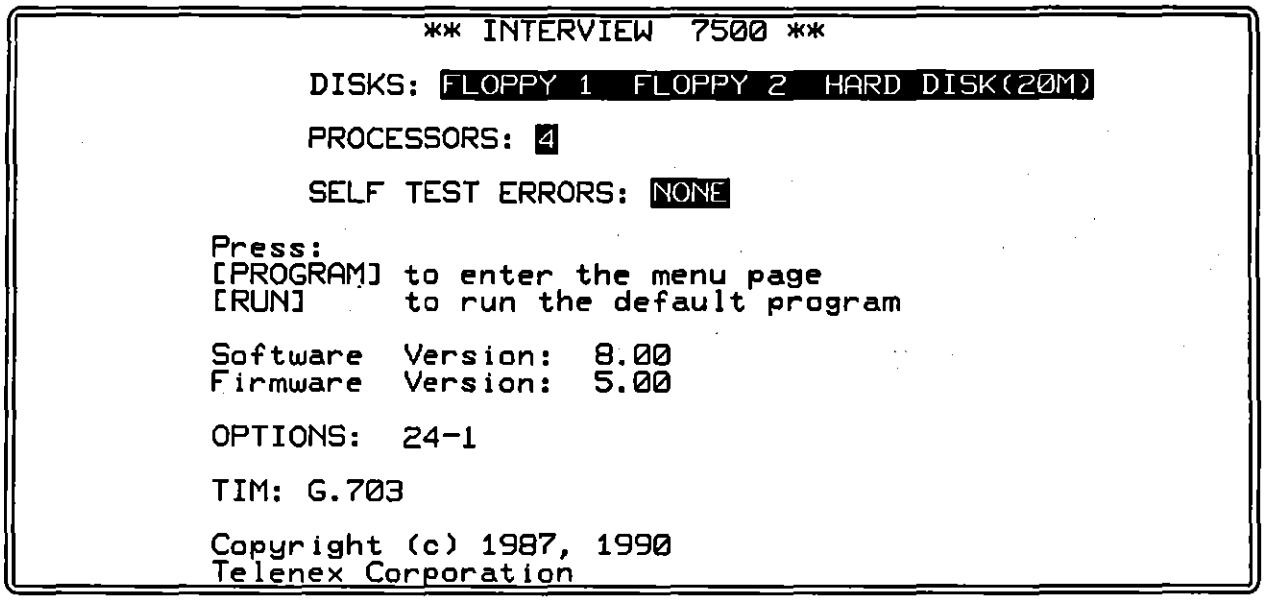


Figure 11-20 Power-up screen, INTERVIEW 7500.

(B) Preparing for G.703 BERT Testing

Setting up for G.703 BERT requires installation of the correct Test Interface Module, proper cabling, and making menu selections. In addition to the selections made on the BERT Setup screen, certain selections must be checked on the Line Setup screen and the G.703 Interface Control screen.

1. *Install the G.703 TIM.* G.703 testing can be done only when the G.703 TIM, described in Section 53.2, is in place. Before powering up the INTERVIEW, install the G.703 TIM as described in Section 1.10.

2. *Cable the G.703 TIM.* With the power switch still OFF, connect to a data source as described in Section 53.2(A). When the TIM is in place and cabling is complete, power on the unit.

   Depending upon the connector used on the TIM, two types of cable may be used for G.703 testing and the **Line Impedance** field selections must match the ohm-value indicated on the TIM. For DE-9 connectors with twisted pair cabling, select 120 ohms line impedance; for BNC connectors with standard coax cabling, select 75 ohms line impedance.

3. *Configure the Line Setup screen.* Before you run a G.703 test, you must configure the Line Setup screen for the type of testing you wish to do. Select **Mode:** BERT DTE if you are operating as a DTE and testing a transmission link or testing toward the network. Select **Mode:** BERT DCE to test toward the multiplexer.

CAUTION: When the INTERVIEW operates in broadband or normal channel transmit mode, it interrupts the regular exchange of data on the circuit for the duration of the test. Be certain you have permission to test the circuit before you proceed.

NOTE: Clocking of G.703 data is not provided by the standard data clock. As a result, the **Clock** selection on the Line Setup screen is overridden. An applicable clock selection is provided on the G.703 Interface Control screen and is described in Section 53.5.

NOTE: Channel BERT setup selections pertaining to half duplex operation are not applicable to G.703 BERT.

Make other Line Setup selections as described in Section 11.3.

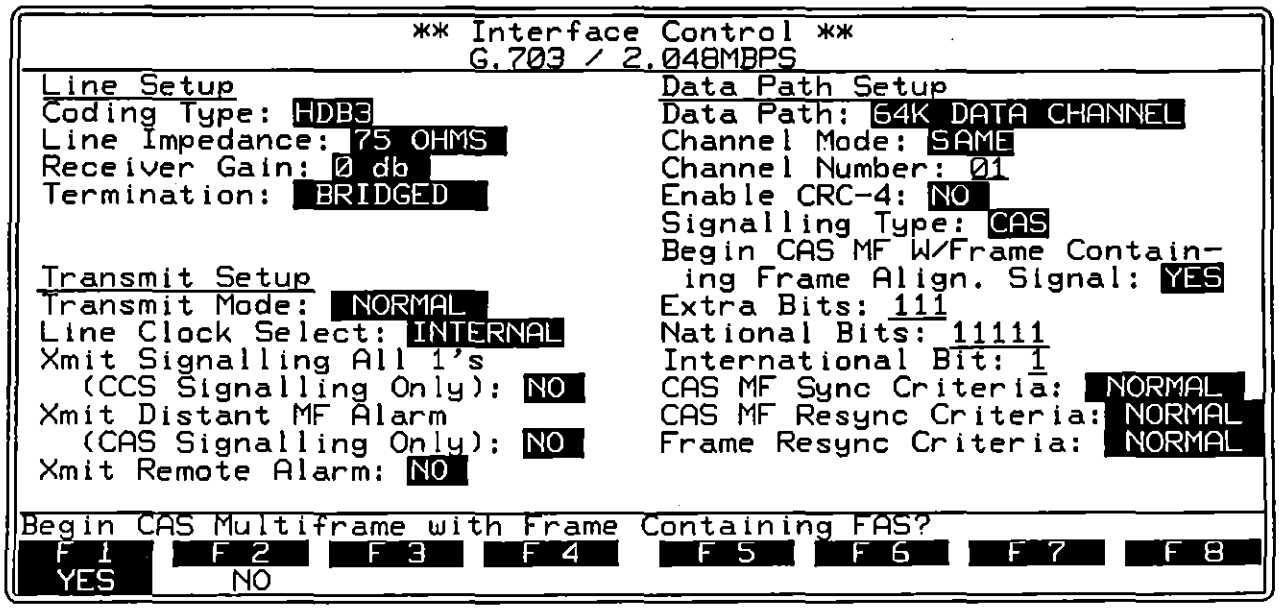


Figure 11-21 Interface Control Screen for G.703 Protocol in Emulate mode.

4. *Configure the G.703 Interface Control screen.* There are different selections on the Interface Control screen pertinent to each type of BERT mode: unframed, framed, or channel BERT.

a. *Unframed BERT.* The Line Setup selections on the G.703 Interface Control screen should be specific to the line to be tested. The rest of the fields on the Interface Control screen are not used in unframed BERT.

b. *Framed BERT.* The Line Setup selections on the G.703 Interface Control screen should be specific to the line to be tested. Those selections specific to the type of signalling selected (CAS or CCS) as well as those specific to CRC-4 errors and channel 0 should also match the line parameters. Other selections are not pertinent. When CAS is the signalling type, the user must not transmit BERT on channel 16 as it is used for signalling information. (Select **Include Ch16:** NO on the BERT Setup screen.)

c. *Channel BERT.* For Channel BERT, select the channel(s) to be tested via the **Data Path, Channel Mode,** and **Channel Number** fields on the Interface Control screen (see Figure 11-21). G.703 framing, syncing, code format, and alarm procedures are also controlled on the Interface Control screen.

Transmit Mode in the G.703 Transmit Setup selections pertains only to Channel BERT testing. One (or two, if **Channel Mode:** SPLIT is selected) of the 31 G.703 data-channels in CCS mode or 30 G.703 data-channels in CAS mode are available for BERT testing at one time. This selection determines what will be transmitted to the other channels which are not under test. The choices are NORMAL and DROP-AND-INSERT.

In NORMAL transmit mode, the standard idle pattern, 0s (hex D5), is transmitted on the remaining data channels. Channel 0, however, always sends framing bits and, if in CAS mode, channel 16 will send signalling information.

NOTE: Do not select **Include Ch16:** YES on the BERT Setup screen.

In DROP-AND-INSERT transmit mode, all received channels pass through the INTERVIEW unchanged, with the exception of the channel under test. The specified channel BERT pattern is inserted into this channel in place of the original data. If **Mode:** BERT DCE is selected, the INTERVIEW transmits the BERT pattern on RD and receives (verifies) on TD; if **Mode:** BERT DTE is selected, the INTERVIEW transmits the BERT pattern on TD and receives (verifies) on RD. If **Channel Mode:** SPLIT is selected, TD and RD are on different channels.

Use drop-and-insert transmit mode when the INTERVIEW is operating in BERT DCE mode in order to test a G.703 mux (using another INTERVIEW to emulate the user DTE).

Use drop-and-insert transmit mode when the INTERVIEW is operating in BERT DTE mode to test phone lines on the network.

For more information on normal or drop-and-insert transmit mode, refer to Section 53.5(E).

Make selections on the G.703 Interface Control screen as described in Section 53.5.

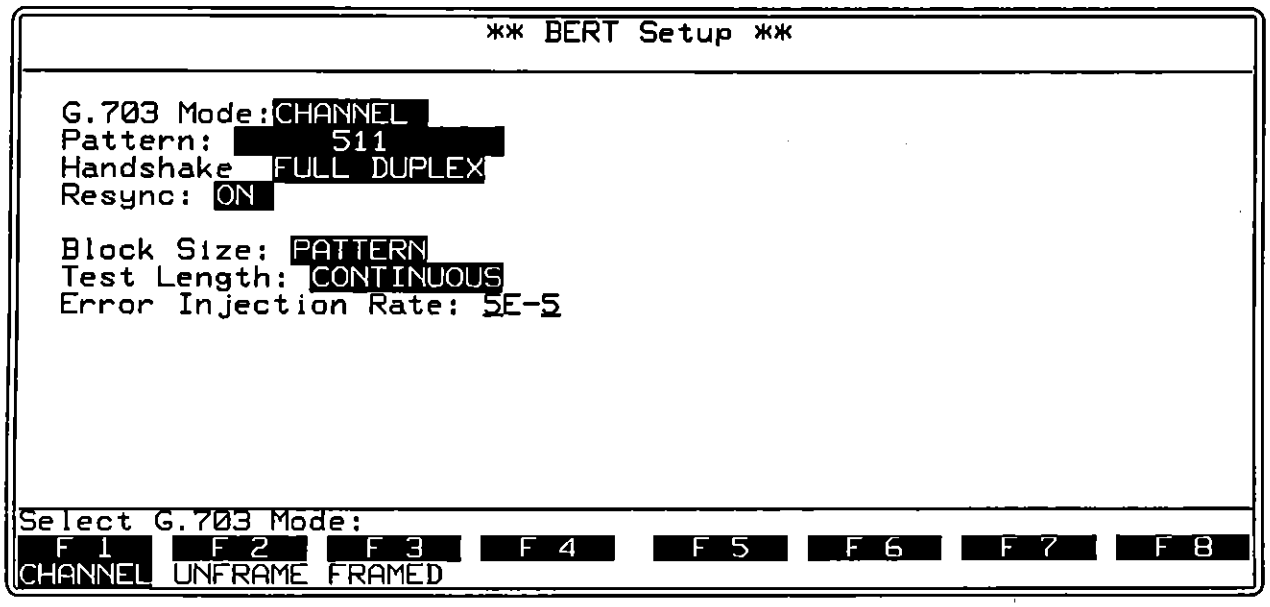


Figure 11-22 The G.703 BERT Setup screen.

(C) G.703 BERT Setup Screen

The default G.703 BERT Setup screen is shown in Figure 11-22. For a full set of options available on this screen, refer to Figure 11-23. As illustrated in Figure 11-23, there are three modes available for G.703 BERT testing. These are CHANNEL, UNFRAMED, and FRAMED.

Channel mode is used for single channel testing and may be done transparently (when drop-and-insert mode is used) so that transmissions on other channels experience minimal interruption.

> NOTE: At the instant that you begin running a test which employs the INTERVIEW in drop-and-insert transmit mode, on-going transmissions on all G.703 channels on the circuit will be momentarily disrupted. This is true even though the INTERVIEW is already connected into the circuit. The interruption is minimal, however, and is not likely to produce a framing error or resynchronization.

Unframed mode, on the other hand, is a "broadband" BERT test; that is, all channels on the G.703 circuit are involved in the test. In Framed mode, all channels except the framing channels (0 and, if selected, 16) are included in the testing.

1. *Channel mode.* G.703 channel mode is similar to *full-duplex* RS-232 BERT testing, with the exception that **Block Size** selections are much larger. For a full explanation of full duplex BERT operation and for **Pattern** and **Resync** selections, refer to Sections 11.3 and 11.5(A) through 11.5(F). G.703 block sizes are described later in this section.

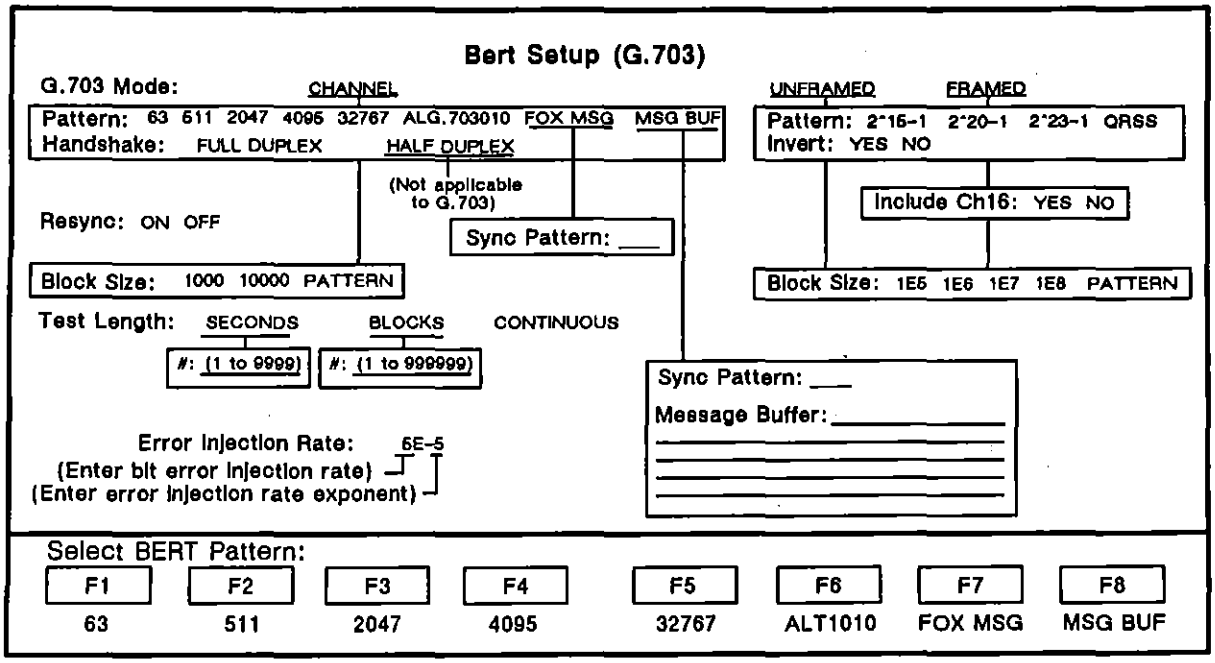


Figure 11-23 G.703 BERT menu options.

2. *Unframed G.703 BERT mode.* This mode sends the BERT pattern in every G.703 bit position, including channel 0. Channel and framing conventions are ignored. When unframed BERT is the G.703 mode, four **Pattern** selections are available. These selections are discussed in subsequent paragraphs.

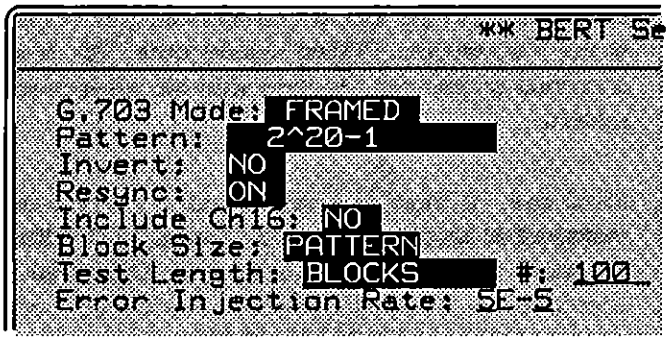


Figure 11-24 When in *FRAMED* G.703 BERT mode, the *Include Ch16* field appears.

3. *Framed G.703 BERT mode.* This mode provides framing bits according to the convention chosen by the user (i.e., CAS or CCS; see discussion in Section 53 and especially paragraph 6. below). These bits are carried on channel 0 and also on channel 16 in CAS mode; they are inserted in between (not written over) the BERT pattern during transmission, which means that error injection during the BERT test will never cause a framing error. When framed BERT is the G.703 mode, the same four patterns available with unframed G.703 BERT may be used (see the discussion in the next paragraph).

4. *Pattern.* The patterns shared by framed and unframed BERT differ from the patterns available with channel BERT. Channel BERT patterns are described in Section 11.5(A).

   For framed and unframed G.703 BERT, the four selections in the **Pattern** field are $2^{15}-1$ (which is equivalent to the 32767 pattern and simulates the output of a 15-bit shift register); $2^{20}-1$ (which simulates the output of a 20-bit shift register); $2^{23}-1$ (which simulates the output of a 23-bit shift register); and QRSS (or Quasi-Random Signal Source, which is similar to the $2^{20}-1$ pattern but observes the 1's density prescribed for transmission by suppressing any string of 15 or more 0's.)

5. *Invert.* This field appears when in either framed or unframed G.703 BERT mode. When **Invert:** YES is selected, a logical inversion of the BERT pattern occurs: 1's become 0's and 0's become 1's. Note that channel 0 is *not* inverted when in framed G.703 BERT mode; and if in CAS mode, channel 16 is not inverted as it contains the signalling bits for that mode.

6. *Include channel 16.* This field appears when in framed G.703 BERT mode. Do not select **Include Ch16:** YES when in CAS mode or else both the signalling bits and the BERT pattern will be sent on this same channel, resulting in a garbled BERT pattern. The signalling bits (which are carried

on channel 16) are inserted in between (not written over) the BERT pattern during transmission. When **Include Ch16:** YES is selected, the BERT pattern is carried on channel 16 along with the other channels and included in the pattern.

7. *Block size.* A block is a component of a test: complete tests may be measured in blocks. In G.703 channel BERT, **Block Size:** PATTERN selections are the same as for RS-232 BERT (see Section 11.5(F)); otherwise, the **Block Size** selection is a certain number of bits. Blocks are measured in bits of 1,000 or 10,000.

   For framed or unframed G.703 BERT, a block can be the length of a cycle as indicated by one of the four **Pattern** selections or a certain number of bits. G.703 block sizes measured in bits are 100,000 (1E5); 1,000,000 (1E6); 10,000,000 (1E7); and 100,000,000 (1E8).

   CAUTION: The definition of a block varies from standard to standard and from BERT tester to BERT tester. Some standards define a block as the pattern length while others specify 1,000 bits. The user must ascertain and then select the proper definition.

8. *Test length.* Tests are measured in blocks or seconds; or they may be CONTINUOUS.

   The **Test Length:** BLOCKS selection brings up a four-digit # field that accepts entries from 1 to 9999. If PATTERN has been selected in the **Block Size** field, the length of the test may be determined by multiplying this figure by the number of bits in the selected test pattern.

   The **Test Length:** SECONDS field also brings with it a # field, with six places for numbers from 1 to 999,999 (a maximum of over 11 days).

   The **Test Length:** BITS selection brings up a field that accepts entries of 1000, 10,000, 100,000 or a pattern. If PATTERN has been selected in the **Block Size** field, the length of the test is the number of bits in the selected test pattern.

9. *Error injection rate.* Errors can be injected in a bit pattern automatically at a preselected rate. Refer to Section 11.5(H) for more information on the pre-determined injection rate. Errors may also be injected manually, one-at-a-time, from the keyboard as explained in Section 11.12(E).

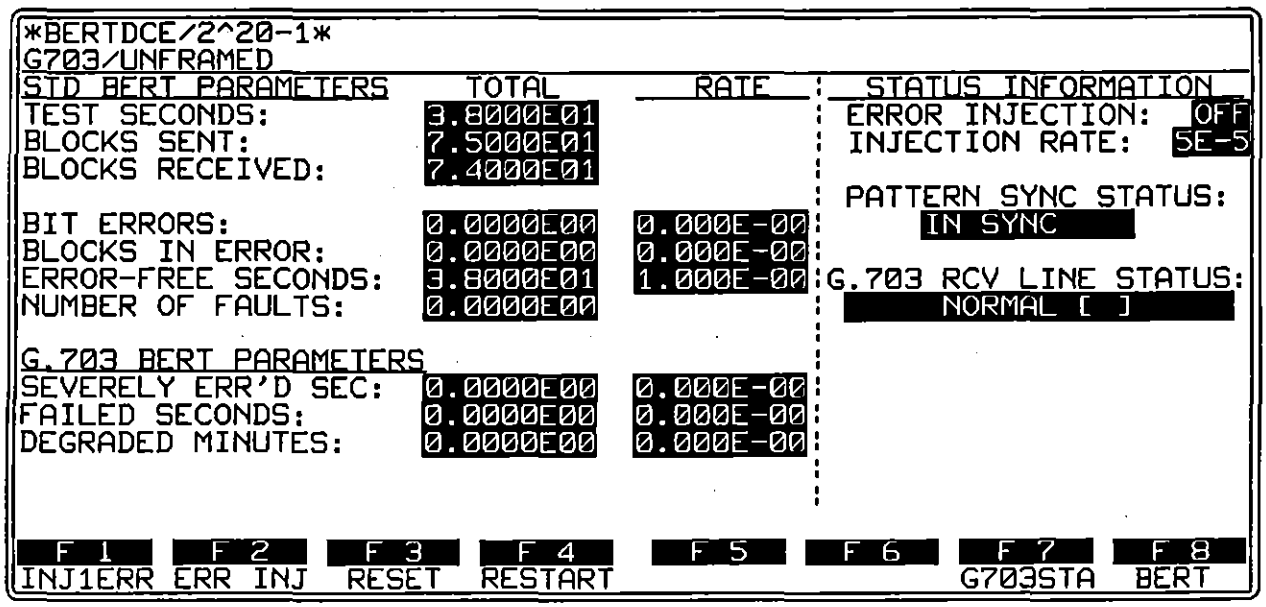


Figure 11-25 Sample G.703 BERT Statistics screen in Run mode.

(D) G.703 BERT Statistics Screen

As long as a BERT emulation mode has been selected on the Line Setup screen and the G.703 hardware options are installed, the G.703 BERT Statistics display appears on the screen. An example of the display is shown in Figure 11-25.

The top of the screen shows which side of the line the INTERVIEW is emulating, indicates whether channel, unframed, or framed testing is being done, and gives additional information on test selections.

Certain test status information is tracked at the far right of the screen. The **ERROR INJECTION** field indicates whether or not the operator has turned on automatic injection rate by pressing the appropriate function key during run-time. The **INJECTION RATE** field indicates the programmer's entry for automatic error injection on the G.703 BERT Setup screen (see Section 11.5(H)). The **PATTERN SYNC STATUS** (as opposed to the line status) field indicates whether the BERT pattern is in or out of sync (see discussion in Section 11.9(J)). The **G.703 RCV LINE STATUS** field reflects the **G.703 LINE CONDITIONS** information given on the regular G.703 Statistics screen (see Section 53.6(K)).

The remainder of the screen provides constantly updated test statistics. Values for BERT parameters (far left of screen) are posted in highlighted boxes in the center of the screen. In addition to total values, rates are given in a highlighted box to the right of the totals. All values are measured starting from the last time [RUN], RESET, or RESTART was pressed.

1. *Test seconds.* This indicates the time elapsed since [RUN] or **RESET** was pressed.

2. *Blocks sent.* This value represents the number of blocks which the INTERVIEW has transmitted. Blocks are recognized according to the block size (in terms of bits) or the pattern (one block per complete pattern) as selected in the **Block Size** and **Pattern** fields on the G.703 BERT screen.

3. *Blocks received.* This is the number of blocks received from the remote end. These blocks are measured according to the same criteria as the number of blocks sent.

4. *Bit errors.* This value represents the number of individual bits received in error. The number of bits in error divided by the total bits received is posted in the **RATE** column.

5. *Blocks in error.* This value indicates the number of blocks received in which one or more bits were found to be in error. The rate which appears to the right is the total blocks in error divided by total blocks received.

6. *Error-free seconds.* This value is the number of **TEST SECONDS** during which no bit error, framing error, CRC error, or bipolar violation was recorded. The rate given to the right is total error-free seconds divided by total **TEST SECONDS**.

7. *Number of faults.* This is the number of times that the number of bits in error has exceeded 25% for at least 1/50th of a second.

8. *Severely errored seconds.* This is the number of individual seconds during which the bit error rate was worse than 1E-3; that is, more than one errored-bit per 1,000 bits. (Ten or more consecutive Severely Errored Seconds constitute a Failed Signal State.)

9. *Failed seconds.* This is the duration of a Failed Signal State in seconds. The tenth consecutive Severely Errored Second is the first Failed Second. A failed signal state lasts until 10 consecutive seconds are *not* Severely Errored Seconds. Thus, there will always be at least 10 failed seconds recorded at one time.

10. *Degraded minutes.* This is the number of minutes during which the bit error rate exceeds 1E-6; that is, more than one errored-bit per 1,000,000 bits.

(E) Run-time Function Keys for G.703 BERT

The function keys shown in Figure 11-26 appear at the bottom of the G.703 BERT Statistics display when the INTERVIEW is running a G.703 BERT test. You may access the G.703 Statistics screen and the regular BERT screen, both of which are active while a G.703 BERT test is in progress, by pressing the appropriate function key. Alternate screens have the same rack of function keys and so allow you to return to the original display.

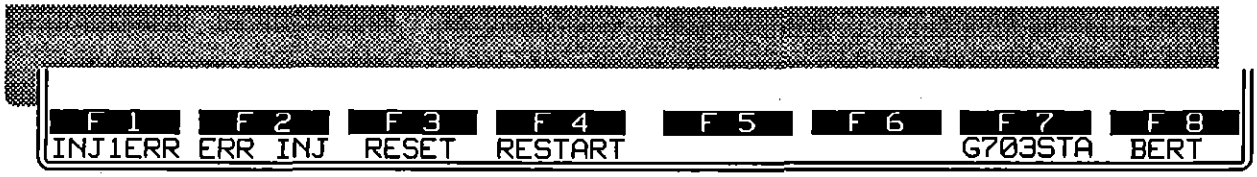


Figure 11-26 Run-time function keys available when performing a G.703 BERT test.

1. *Inject one error.* The function key labeled INJ1ERR injects a single bit error into the INTERVIEW's G.703 BERT transmission. If this key is used when error injection is on (see next paragraph), the single error is simply added to the automatic error rate.

2. *Error injection at pre-determined rate.* The function key labeled ERR INJ is an alternate-action function key which turns off the automatic error injection; or turns it back on and inserts errors into the G.703 BERT transmission at the rate selected on the G.703 BERT Setup screen. (See Section 11.5(H) for a description of the selection.) Error injection is off when the INTERVIEW enters Run mode. The **ERROR INJECTION** field at the far right of the screen tells you whether automatic error injection is currently on or off.

3. *Reset.* The function key labeled RESET sets the value of all timers and counters, including G.703 counters, to zero. The BERT test continues, however.

4. *Restart.* The function key labeled RESTART is used to initiate G.703 BERT testing again, once it has stopped at the point determined by the Test Length selection on the G.703 BERT Setup screen. All BERT counters, timers, and elapsed time (**TEST SECONDS**) continue from wherever they stopped.

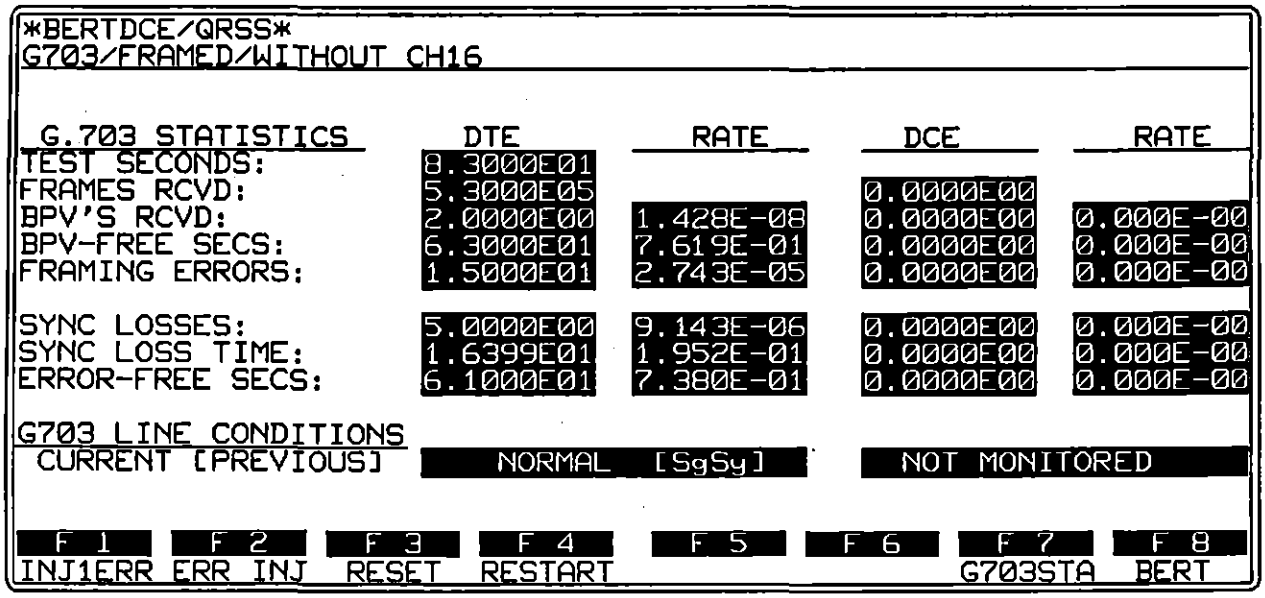


Figure 11-27 The G.703 Statistics screen is an alternate run-time screen during G.703 BERT testing.

5. *G.703 statistics display.* The function key labeled G703STA changes the INTERVIEW screen to the regular G.703 statistics display (see example in Figure 11-27). The contents of this display are described in Section 53.

6. *Regular BERT display.* The function key labeled BERT changes the INTERVIEW screen to the regular BERT statistics display (see example in Figure 11-8). The contents of the regular BERT display are described in Section 11.9. Press the function key labeled BERT again to return to the G.703 BERT statistics screen.

12 Standard Interface: RS-232

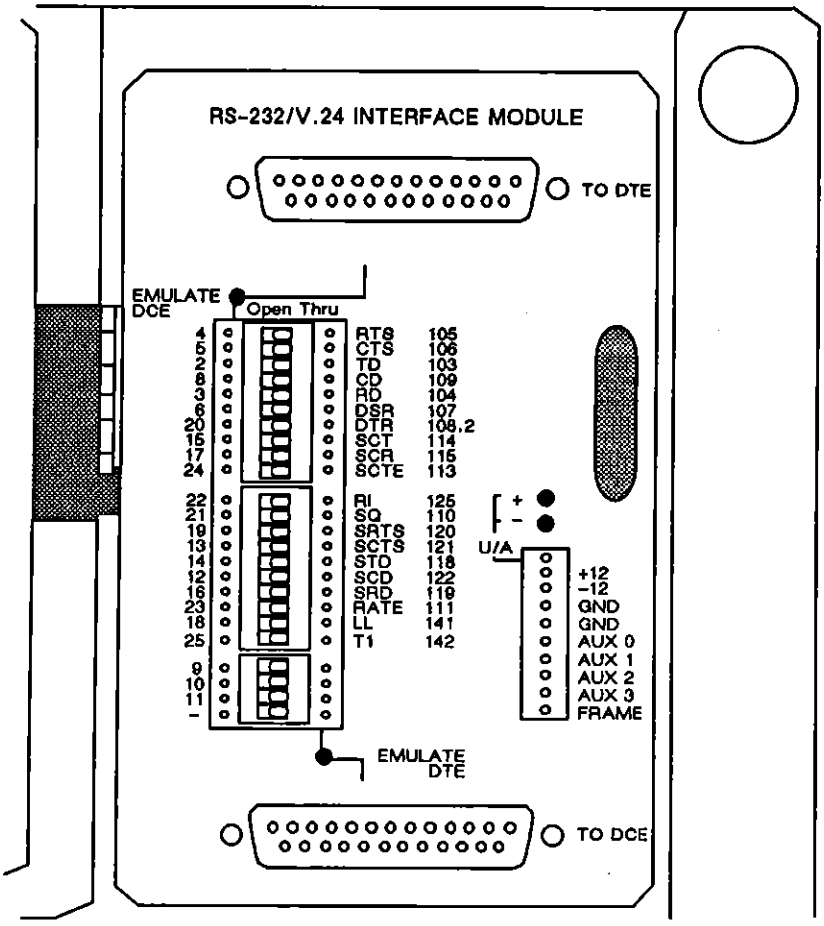


Figure 12-1 Breakout panel on RS-232/V.24 Test Interface Module (TIM).

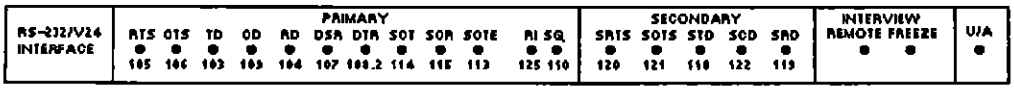


Figure 12-2 RS-232/V.24 Green-Red LED Overlay.

12 Standard Interface: RS-232

The INTERVIEW contains a universal logic interface that supports data rates into the megabits-per-second range. Physical interfaces that are adapted to the various data rates are provided in the form of test-interface modules (or TIMs).

TIMs currently available include RS-232/V.24, V.35, X.21, RS-449, RC-8245 (RS-485), T1, G.703, and ISDN. Each interface module provides *breakout* patching and switching for each lead.

TIMs are modular and simple to install. There are two steps to installing an interface module: 1) **With the unit powered off,** insert the TIM into the module slot at the rear of the unit and press until it latches; 2) apply the proper LED overlay in position on the front of the unit above the screen. The overlay is a flexible plastic strip with small tips on either end that fit into notches in the front panel. The overlay covers the front-panel green-red LEDs and gives them connector-specific identification.

Note that the test-interface module locks into place and a small blue release bar must be pressed to unlock it. The rear of the unit is illustrated in Section 1 of this manual.

Figure 12-1 and Figure 12-2 show the TIM and the LED overlay for the standard interface, RS-232. Once the RS-232 module is installed, the following EIA functions are enabled: seventeen leads can be monitored on the front-panel green-red LEDs; twenty-three RS-232 leads can be switched, patched, and tested on the breakout box on the module; up to five control leads can be selected for real-time screen display; seven leads can be monitored by menu and spreadsheet triggers; and five RS-232 leads and four auxiliary leads come under spreadsheet control in emulate modes. Also in emulate modes, five control leads, four auxiliary leads, six handshake timers, and two transmit delays can be regulated via an Interface Control menu screen.

12.1 Connectors

When you break a data line for testing, you may connect one end of the line to the TO DTE connector on the TIM (see top of Figure 12-1). Connect the other end of the line to the TO DCE connector on the TIM. Even when the INTERVIEW is powered off, this provides a through connection for the data line.

When **Mode:** MONITOR or AUTOMONITOR is the program selection, the INTERVIEW monitors data passively through either (or both) TO connectors on the TIM.

When the INTERVIEW is operating in EMULATE DCE mode (selected on the Line Setup menu), the EMULATE DCE indicator is red. This indicates that the TO DTE connector is active. The INTERVIEW is transmitting and receiving data through the TO DTE connector. When Mode: EMULATE DTE is the program selection, the INTERVIEW transmits and receives data through the TO DCE connector. The EMULATE DTE indicator is red, and the EMULATE DCE indicator is off.

CAUTION: To connect the data line, you must interrupt the flow of data on the line. Be sure you have permission to break the line before doing so.

12.2 Green-Red LEDs

The RS-232 LED overlay (Figure 12-2) identifies twenty LEDs. Seventeen of these represent RS-232 leads monitored at either of the line interfaces (TO DTE, TO DCE) on the test-interface module. An LED is dark when the unit is off, green when the unit is powered on but the lead is off or unterminated (off for EIA receivers being defined as less positive than +3 V relative to signal ground) and red when the lead is at or above the *on* threshold (+3 V).

Data and clock leads often transition quite rapidly. As a result, their LEDs typically show an orange color that is intermediate between red and green. Data-lead LEDs will vary in color with the type of data. $^{r}_{F}$-idle, for example, has no *on* transitions and appears as bright green. $^{r}_{E}$-idle is *on* 25 percent of the time (that is, two bits out of every eight bits are *zero)* and glows with its own distinctive light-orange mixture.

Two of the LEDs switch to red when the unit is in a special mode, Remote mode or Freeze mode. Remote means that the unit is *under* remote control via the REMOTE port. (The remote-control feature is not implemented at this time.)

The final LED label on the right end of the overlay is UA (user assigned). This LED monitors any signal that is patched to the UA-input jack on the module. See Figure 12-5. Any of the eight RS-232 leads that are not accounted for on the front overlay can be assigned to this LED by the user.

It is important to note that the front-panel LED indicators always reflect TIM activity. If the LEDs are active while data is being played back from disk, the activity is on the line, not in the data stored on the disk. Playback data may activate triggers that monitor interface leads, and it may generate a data-plus-leads display; but playback data never drives the green-red LEDs.

12.3 Breakout Box

The INTERVIEW is tied to the digital communications line by two cable-connections on the interface module, one cable going to the DTE and one to the DCE. Refer to Section 12.1. In between the two cables are the INTERVIEW's drivers and receivers and, on the face of the module, a breakout area. The breakout area has a column of switches that allows any RS-232 circuit to be opened, and two columns of patch jacks that allow circuits to be rerouted by patch cords.

The lefthand column of patch jacks may be thought of as belonging to the DTE, in that signals applied to those pins are *always* visible to the receiver and the front-panel green-red LEDs when the unit is emulating DTE, whatever the condition of the breakout switches.

The righthand column of patch jacks pertains to the DCE: signals applied to these leads are always visible to the receiver and the front-panel LEDs when the unit is emulating DCE, whatever the condition of the breakout switches.

> NOTE: Patching or switching the leads on the front panel can affect not only the received data but also the actual data on the line, *even when the INTERVIEW is in Monitor mode.*

(A) Paths Through the Breakout Switches

Figure 12-3 illustrates the position of the INTERVIEW's receivers and high-impedance monitors relative to the breakout and patching area when signals are moving across the interface module under two different emulate conditions (driving and receiving) and in Monitor mode. Note that an opened switch will have a different effect on the screen display and LED display of signals depending on the test mode.

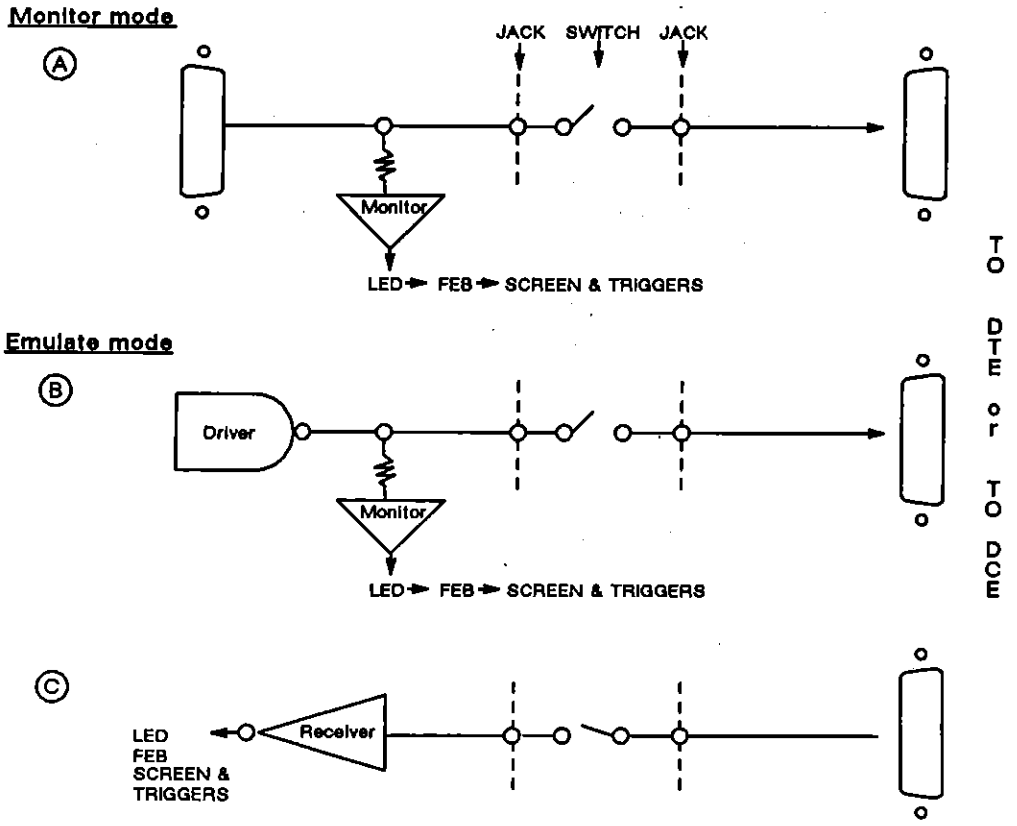


Figure 12-3 Position of patch jacks and breakout switches relative to monitors/receivers when unit is passively monitoring (A), driving signal in emulate mode (B), or receiving signal in emulate mode (C).

Monitor mode is shown at the top of the illustration. In this mode (example A), a signal is being transmitted left to right across the interface module while the INTERVIEW is monitoring passively. The breakout switch is open and the signal is prevented from reaching its destination, but the INTERVIEW monitor sees it. *In Monitor mode the INTERVIEW sees everything*, regardless of the position of the breakout switches.

The signal in the middle of the illustration in Figure 12-3 is being driven by the INTERVIEW. The breakout switch is open and the *on* signal is not reaching the cable connection to DCE or to DTE; but because the monitor is on the driver side of the switch, the front-panel LED is red and an *on* voltage level is shown on the data-plus-leads screen display.

The bottom signal in Figure 12-3 (example C) is being driven by the DTE or DCE at the cable interface. The signal is intended for an INTERVIEW receiver in an Emulate mode, but the breakout switch is open. Since the INTERVIEW's

receiver for incoming signals always is "downstream" of the switch, the front-panel LED is green and neither the screen nor the program detect the *on* status.

Note also in connection with Figure 12-3 that there is a selection on the Front End Buffer (FEB) Setup menu that inhibits reception and display of all EIA activity except data (see Section 9). Figure 12-3 indicates the point at which EIA status is passed to the FEB in Emulate and Monitor modes. (Refer also to the functional block diagram in Figure 2-5.) Green-red LED display is *not* affected by FEB suppression of EIA leads, since, as the figure suggests, the path of the signals is through the receivers/monitors to the LEDs first, to the FEB next, and finally to the triggers and screen.

(B) Patching Example: Modem Eliminator

Figure 12-4 is an example of patching. Six patch cords have configured the breakout area into a modem-eliminator that allows two DTEs to converse across the interface module. Note that switches next to rerouted leads have been opened.

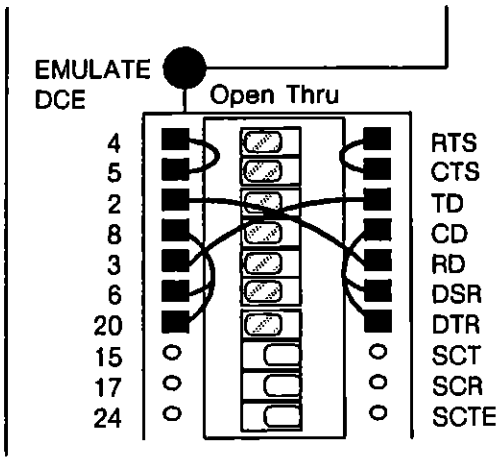


Figure 12-4 Patch cords reroute data and control leads to allow two DTEs to communicate.

(C) Special Input and Output Pins

Off to the right of the breakout area are two LEDs and another column of patch pins. The LEDs indicate the voltage patched to the uppermost pin (Figure 12-5). This is the UA (user-assigned) input jack. If a signal patched to this input is +3 V (nominal) or more positive, the red + LED will go on. If the signal is -3 V (nominal) or more negative, the green - LED will light. Any signal patched to this input can be monitored by the INTERVIEW's triggers.

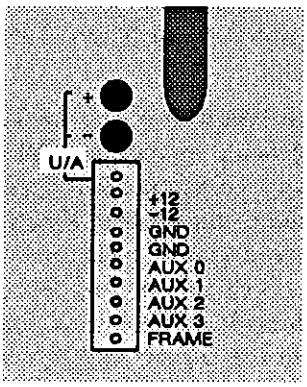


Figure 12-5 A separate column of patch jacks provides UA input and nine special output pins.

There are four kinds of lead-status indicators in the INTERVIEW: front-panel LEDs, lead-level graphic display on the data-plus-leads screen, triggers that test EIA status, and UA-input LEDs. Of these, *only the UA-input minus (-) LED indicates negative voltage*. The other indicators recognize two states only: more positive than +3 V and less positive than +3 V (with a slight allowance for hysteresis).

There is a glitch catcher on the UA input. Whenever the voltage is more positive or less positive than +3 V for at least one microsecond, it will be latched until the trigger logic checks it. Thus the UA trigger condition can be used to detect glitches on any interface lead.

Below the UA input are nine more patch jacks. See Figure 12-5. All are output jacks. Two of the outputs are test points that supply +12 V and -12 V, respectively, through 1-kohm resistors. The third and fourth pins are at signal ground.

The next four jacks allow you to patch the output of four auxiliary RS-232/V.24 drivers that are controlled by trigger actions on the Protocol Spreadsheet and by selections on the Interface Control menu (see Sections 12.5 and 12.6 below). These AUX outputs are useful if at some point in a program you want to turn on a signal that you don't actually control. You might be raising RTS, for example, and the modem is not giving you Clear to Send. Simply patch AUX0 to CTS on the TO DCE (right) side of the breakout switches; open the switch for CTS; and drive AUX0 via trigger. (The AUX pins on the test-interface module have nothing to do with the 25-pin TTL AUXILIARY connector on the rear of the unit.)

12.4 Screen Display of Lead Status

Five RS-232/V.24 control leads can be selected for a data-plus-leads display, in which the control leads are represented by two-state timing lines drawn beneath TX and RX data. See Section 6.3(B).

12.5 Program Control of Lead Activity

The status of seven RS-232/V.24 leads can be tested by triggers. The leads are RTS, CTS, CD, DTR, DSR, RI, and a lead of the user's choosing patched to the UA-input jack (see 12.3(C), above). The status of the lead may be made a trigger-menu condition (Figure 12-6) or a Spreadsheet condition (Figure 12-7).

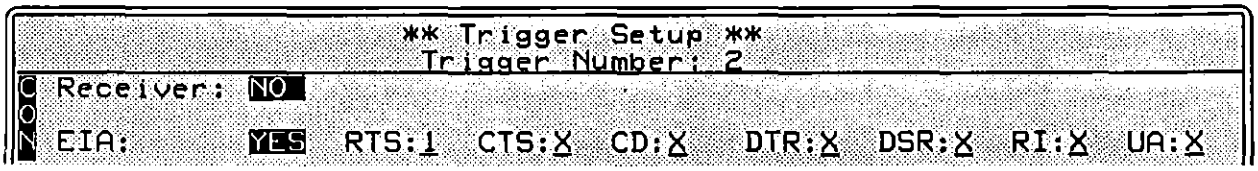


Figure 12-6 The status of seven RS-232 leads may be tested by triggers.

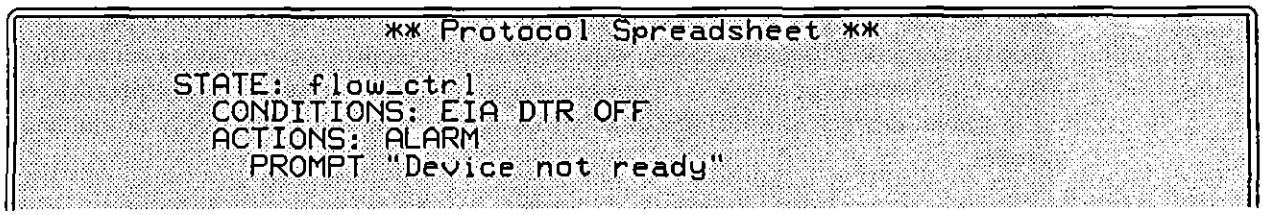


Figure 12-7 EIA status also may be made a spreadsheet condition.

On trigger menus, lead states are described as 1 or 0. For the receiver logic, 1 as an EIA trigger condition means +3 V (nominal) or more positive. 0 means less positive than +3 V. 0 on a trigger menu does not mean -3 V or more negative, even in the case of the UA lead.

Five RS-232 leads (RTS, CTS, DTR, DSR, and CD) can be driven on or off as a trigger action. This action is available on the spreadsheet for Layer 1 (see Figure 12-8) but not on trigger menus. Four auxiliary pins on the breakout panel likewise are under spreadsheet control.

An ON action by the spreadsheet program will drive an EIA lead into a plus range (+5 V to +15 V) defined by the standard. An OFF action by the spreadsheet program will drive a lead into a minus range (-5 V to -15 V) defined by the standard. The difference between a 0 condition and an OFF action (0 in a condition

only meant a voltage less positive than +3, not a minus range) is explained by the fact that drivers are allowed three states—on, off, and *inactive*—whereas receivers must decide between on and off.

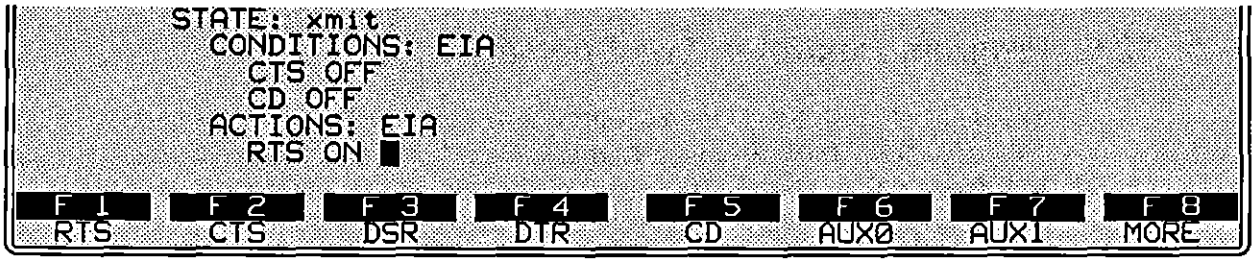


Figure 12-8 The spreadsheet program can control five RS-232 leads plus four auxiliary leads.

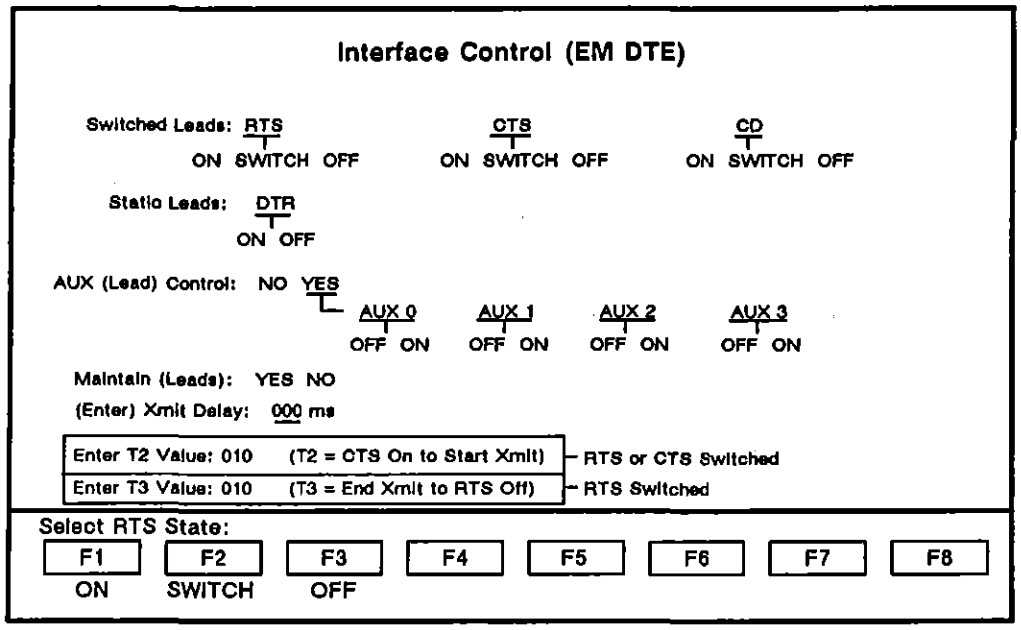
12.6 Interface Control Menu Screen

Figure 12-9 shows the programming selections on the Interface Control menu screen for RS-232/V.24. The menu differs slightly according to whether EMULATE DTE is the **Mode** selection on the Line Setup menu (top half of Figure 12-9) or whether EMULATE DCE is the selection (bottom half of figure). The menu simplifies the programming of EIA lead activity, especially in half-duplex environments where the RTS-CTS handshake would be cumbersome to program correctly on the spreadsheet. The screen controls the INTERVIEW's EIA drivers and is operative only in emulate modes.

On the Interface Control menu screen, ON and OFF imply that a lead is driven to *on* or *off* voltage in accordance with the RS-232/V.24 standard, which says that a signal is driven *off* within a range of −5 to −15 volts with respect to signal ground, and *on* within a range of +5 to +15 volts with respect to signal ground.

(A) Switched Leads: RTS, CTS, CD

The **RTS**, **CTS**, and **CD** fields enable the INTERVIEW to turn these three leads on and off, if it is controlling them. The **Mode** selection on the Line Setup menu determines which leads are controlled: RTS when the unit is in Emulate DTE mode and CTS and CD when it is in Emulate DCE mode.



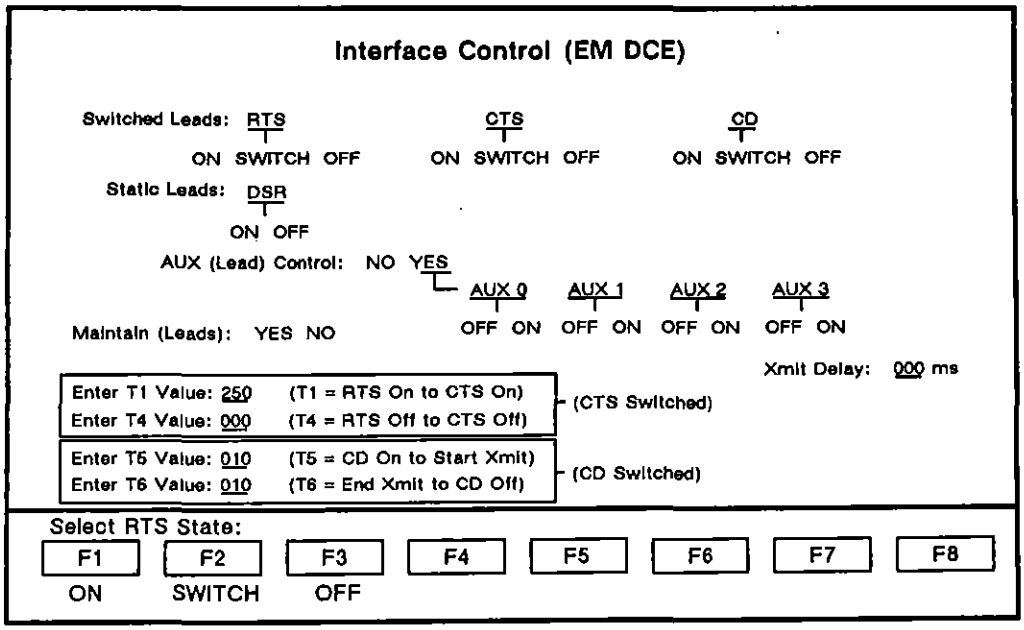


Figure 12-9 Menu fields on the Interface Control menu screen.

1. *Emulate DTE*

   a. Full-duplex systems. If the system is full duplex and the INTERVIEW is in Emulate DTE mode, turn **RTS:** ON. The unit will turn RTS on *when entering Run mode.*

   In Emulate DTE mode, the device under test should control CTS and CD. Your selections for these leads do make a difference, however. They tell the INTERVIEW what signals to expect from the other side of the interface, and the unit performs accordingly.

   CTS: ON means, for example, that the INTERVIEW will behave as if CTS always were on. Use this selection when you want to transmit as a DTE but for some reason you are not receiving Clear To Send. The unit will transmit as soon as the test conditions are satisfied.

   If **CTS:** SWITCH is selected, the INTERVIEW *will wait for CTS* before transmitting. See Table 12-1 for the significance of each control-lead selection in both Emulate DTE and Emulate DCE modes.

   b. Half-duplex or multidrop systems. In half-duplex operation, select SWITCH for RTS, CTS, and CD. The unit will turn on RTS before it transmits and turn it off after each transmission. The unit will wait for CTS to go off before it raises RTS for a new transmission.

   When you have selected SWITCH for RTS, you may enter a delay in the **Xmit Delay** field. See Figure 12-10. Use this field to enter a delay from the time that the test conditions are satisfied to the bringing up of the RTS lead to request permission to send. This field enables you to use characters near the beginning of a received block as the condition for transmission but delay the start of transmission until after the entire block has been received. It may also be used to simulate a response delay.

Table 12-1
Significance of On/Switch Selections on Interface Control Menu

Lead	On/Switch	Meaning
Mode: Emulate DTE		
RTS	ON	Turn RTS ON entering Run Mode.
	SWITCH	Turn RTS ON before each xmit. Turn RTS OFF after each xmit.
	OFF	Turn RTS OFF entering Run Mode.
CTS	ON/OFF	Xmit without respect to CTS ON.
	SWITCH	Wait for CTS ON before each xmit.
CD	ON/OFF	Raise RTS for new xmit without respect to CTS OFF.
	SWITCH	Wait for CTS OFF before raising RTS for new xmit.
Mode: Emulate DCE		
RTS	ON/OFF	Raise CD to xmit without waiting for CTS OFF.
	SWITCH	If CTS and CD switched, wait for CTS OFF before raising CD to xmit.
CTS	ON	Turn CTS ON entering Run Mode. Raise CD to xmit without waiting for CTS OFF.
	SWITCH	CTS follows RTS during Run Mode.
	OFF	Turn CTS OFF entering Run Mode.
CD	ON	Turn CD ON entering Run Mode.
	SWITCH	Turn CD ON before each xmit. Turn CD OFF after each xmit.
	OFF	Turn CD OFF entering Run Mode.

Figure 12-10 In Emulate DTE mode, *Xmit Delay* delays the raising of RTS to begin transmission, with a range of delay of zero to 999 ms.

Apart from the transmit delay, there are two other programmable delays in Emulate DTE Mode. In default, the unit will send data 10 msecs after it sees CTS come on. This delay can be set at zero to 999 msecs in the **T2** field at the bottom of the menu. See Figure 12-11. The same range of delay (and the same default setting of 010) is available for **T3**, the time the unit will wait before turning RTS off after it has transmitted the message.

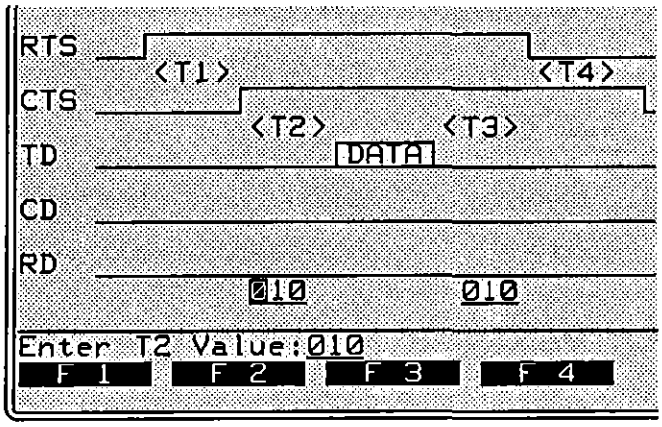


Figure 12-11 T2 and T3 delays also are selectable in Emulate DTE mode.

If **CTS:** ON is selected, the INTERVIEW will transmit after raising RTS but before it sees CTS. (Normally in half duplex, characters that arrive at the modem before CTS is granted are discarded.)

If **CD:** ON is selected, the INTERVIEW will raise RTS and start a new transmission before CTS has gone off to complete the handshake for the last transmission.

In multidrop systems, the selections depend on which side of the link you are on. If you are emulating the host (emulating DTE), select **RTS:** ON, **CTS:** ON, **CD:** SWITCH. If you are emulating DTE from the drop side of the line, select **RTS:** SWITCH, **CTS:** SWITCH, **CD:** ON.

Table 12-2 shows a group of typical switched-lead configurations in Emulate DTE (and Emulate DCE) mode.

Table 12-2
Standard Switched-Lead Configurations

Mode: EMULATE DTE			
RTS: ON	CTS: ON	CD: ON	full duplex
RTS: SWITCH	CTS: SWITCH	CD: SWITCH	half duplex
RTS: ON	CTS: ON	CD: SWITCH	multidrop, emulate host at host site
RTS: SWITCH	CTS: SWITCH	CD: ON	multidrop, emulate drop at drop site
Mode: EMULATE DCE			
RTS: ON	CTS: ON	CD: ON	full duplex
RTS: SWITCH	CTS: SWITCH	CD: SWITCH	half duplex
RTS: ON	CTS: ON	CD: SWITCH	multidrop, emulate drop at host site
RTS: SWITCH	CTS: SWITCH	CD: ON	multidrop, emulate host at drop site

2. *Emulate DCE*

   a. Full-duplex systems. If the system is full duplex and the INTERVIEW is in Emulate DCE mode, turn **CTS** and **CD** ON. The unit will turn both leads on when it enters Run mode. You do not control RTS in this mode, and the **RTS** field has no significance with CTS and CD on.

   If **CTS:** SWITCH is selected, this lead will follow RTS during Run mode.

   b. Half-duplex or multidrop systems. In half-duplex operation, select SWITCH for **RTS**, **CTS**, and **CD**.

   When you have selected SWITCH for **CTS**, you may enter a delay time of from 0 to 999 msec in the **T1** field at the bottom of the screen. See Figure 12-12. **T1** is a decimal field with a default value of 250 msec. When the INTERVIEW (in Emulate DCE mode) sees RTS go on, it will wait this delay before turning CTS on. After it sees RTS go off, it will wait the preset **T4** delay (zero msecs in default) to turn CTS off.

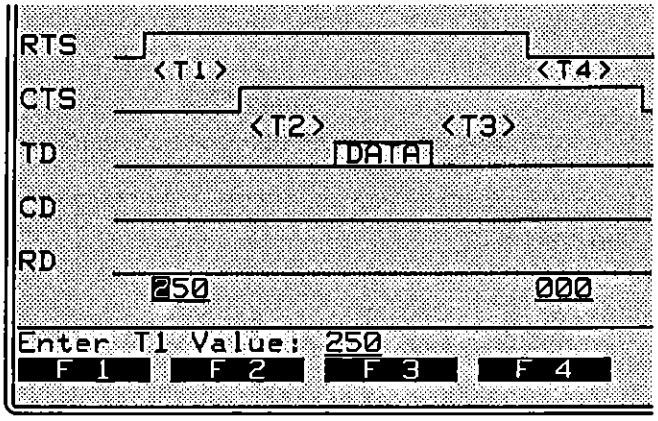


Figure 12-12 In Emulate DCE mode, T1 and T4 delay the raising and lowering of CTS.

When you have selected **CD:** SWITCH, the INTERVIEW (in Emulate DCE mode) will wait any delay time that might have been entered in the **Xmit Delay** field, and then try to raise CD. See Figure 12-13. If CTS is on (in response to RTS), the unit will not raise CD until CTS goes off. It will send data 10 msecs (or any other preset **T5** delay) after it has turned CD on, and turn CD off after the preset **T6** delay, subsequent to the block check characters or the end of transmission.

In multidrop systems, the selections depend upon which side of the link you are on. If you are emulating the modem (DCE) at the host site (that is, testing the host), select **RTS:** ON, **CTS:** ON, **CD:** SWITCH. If you are emulating a DCE at the drop site (testing a drop DTE), select **RTS:** SWITCH, **CTS:** SWITCH, **CD:** ON.

Table 12-2 shows a group of representative switched-lead configurations in Emulate DCE mode.

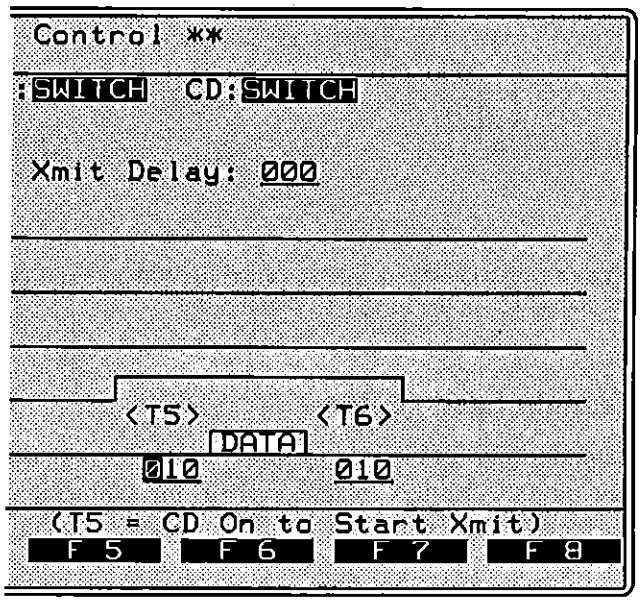


Figure 12-13 In Emulate DCE mode, Xmit Delay pertains to the raising of CD.

(B) Static Leads: DTR, DSR

Use the **Static Leads** field to instruct the INTERVIEW to drive either DTR or DSR—depending on the test mode—constantly on or off.

(C) Auxiliary Leads

These are four pins on the TIM breakout panel whose output is programmable on the Interface Control menu (and also in spreadsheet trigger actions). Four subfields appear to the right of **AUX Control:** YES on the Interface Control menu, one for each AUX driver from zero to three. See Figure 12-14. When one of these AUX fields is turned on, the output on that pin will be standard RS-232/V.24 space (+) voltage at the start of Run mode and will remain at that level until a spreadsheet trigger turns the signal to standard EIA mark (–) voltage. The output driver is a 1488, which can sink up to 10 mA.

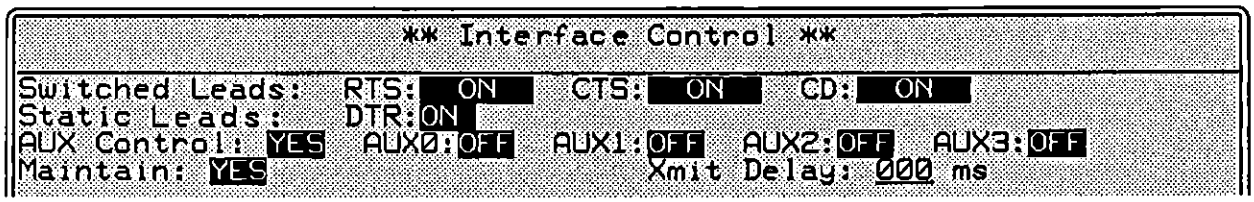


Figure 12-14 Auxiliary signals can be patched to EIA leads on the breakout box and then turned on and off on the Interface Control menu.

(D) Maintain Lead Status

Maintain: YES allows you to preserve the current lead status even after exiting Run mode. Use this selection when, for example, you are testing a remote device and dropping DTR would cause your modem to hang up.

If you select **Maintain:** NO, all interface leads will be reset to the *off* voltage each time the unit leaves Run mode.