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K450 LOGIC ANALYZER

SERVICE MANUAL

BIOMATION
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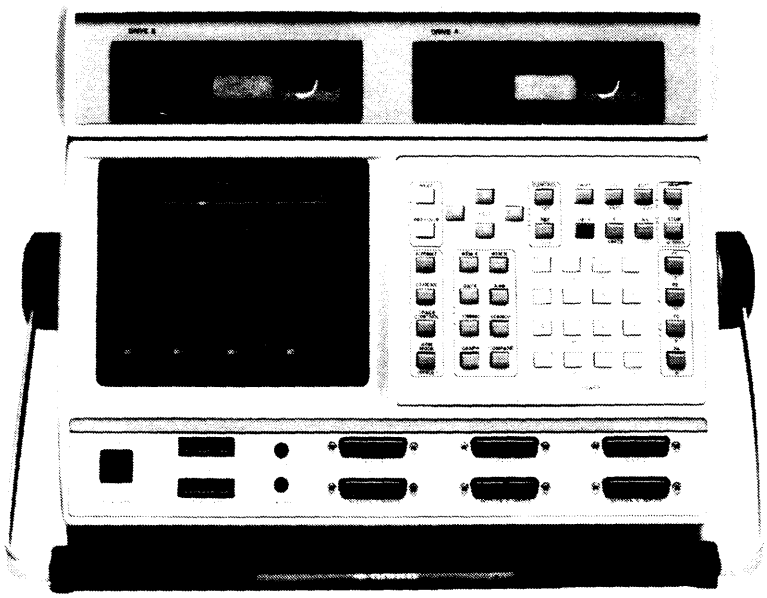
4/86



K450 Logic Analyzer

WARNING

This equipment has not been tested to show compliance with new FCC Rules (47 CFR Part 15) designed to limit interference to radio and TV reception. Operation of this equipment in a residential area is likely to cause unacceptable interference to radio communication requiring the operator to take whatever steps are necessary to correct the interference.

The following procedures may help to alleviate the Radio or Television Interference Problems:

1. Reorient the antenna of the receiver receiving the interference.

2. Relocate the equipment causing the interference with respect to the receiver (move or change relative position).

3. Reconnect the equipment causing the interference into a different outlet so the receiver and the equipment are connected to different branch circuits.

4. Remove the equipment from the power source.

Note: The user may find the following booklet prepared by the FCC helpful: "How to Identify and Resolve Radio-TV Interference Problems". This booklet is available from the U.S. Printing Office, Washington, D.C. 20402. Stock No. 004-000-00345-4.

PREFACE

This manual contains information for servicing and maintaining the Gould K450 Logic Analyzer. Procedures are provided for making adjustments and calibrating the control circuits for various functions. These procedures include the use of diagnostic tests to troubleshoot and isolate a malfunction to a circuit component. Theory of operation is presented for the printed circuit board functions. Service aids in the form of schematic diagrams, wiring diagrams, assembly drawings, cable connection diagrams and parts lists are included for user reference.

The material in this manual reflects the Control Firmware level valid on March 17, 1986 and is up-to-date at the time of publication. but is subject to change without notice.

Copies of this publication and other Gould Inc., Design and Test Systems Division Publications may be obtained from the Gould Inc., Design and Test Systems Division sales office or distributor serving your locality.

RELATED PUBLICATIONS

The following support documentation may be used with this manual:

- K450 User's Manual, Publication Number 0121-0004-10, Describes the capabilities, functions, and operation of the K450 Logic Analyzer.
- K450 Disk Storage System User's Manual Addendum, Publication Number 0121-0084-10, Describes the capabilities, function and operation of the K450 DSS option.

ASSISTANCE

If you require assistance on this product, please call Gould Inc., Design and Test Systems Division Customer Service on the toll-free, hot-line numbers listed below.

Nationwide (800) 538-9320/9321

California (800) 662-9231

WARRANTY

The Gould Inc., Design and Test Systems Division K450 is warranted against defects in materials and workmanship for a period of one year from date of shipment. Any floppy disk or hard disk drives attached to or contained within this equipment are warranted for 90 days from date of shipment. Gould Inc., Design and Test Systems Division will repair or replace products that prove to be defective during the warranty period.

Warranty service must be performed at a Gould Inc., Design and Test Systems Division authorized service facility. **The customer must call Gould's Customer Service department at the toll-free numbers listed in the front of this manual and obtain a Return Authorization number prior to returning the unit for service.** If a unit fails within 30 days of shipment date, Gould Inc. will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the 30-day period, should be sent to Gould Inc. prepaid, and Gould Inc. will return the unit prepaid. The customer must pay all shipping charges for units out of warranty.

Misuse of, abuse of, or tampering with this unit will, at the discretion of Gould Incorporated, cause this warranty to be null and void.

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Figure Page

Chapter 1

GENERAL DESCRIPTION

INTRODUCTION

Overview of K450 Features

The Gould/Biomation K450 Logic Analyzer (Figure 1-1) is a test and development instrument, that monitors and records signals from the user's target system.

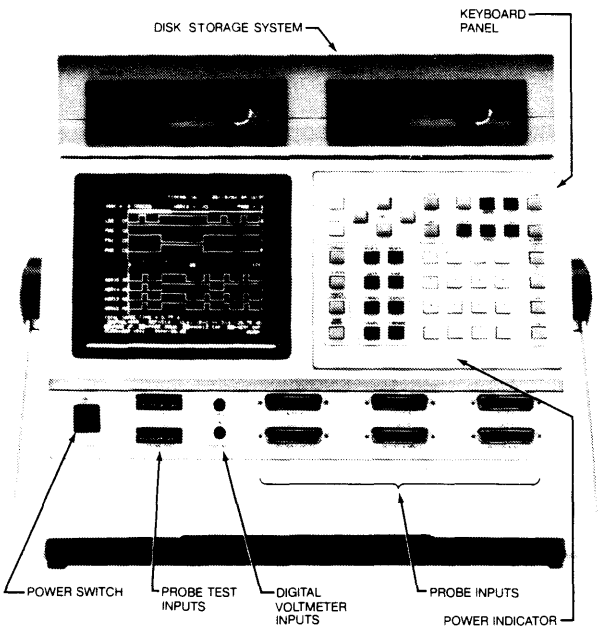


Figure 1-1. K450-D Logic Analyzer, General Arrangement

The K450 may be configured to accept the following data inputs:

- o 16, 32, or 48 Inputs @ 100 MHz Sections A, B and C.
- o 8, 16, or 24 Inputs @ 200 MHz Sections A, B and C.

The K450 also accepts the following external clock inputs:

- o 2 Sample and 2 Latch clocks, Section A only.
- o 6 Sample and 2 Latch clocks, Section A and B.
- o 6 Sample and 6 Latch clocks, Sections A, B and C.

The K450 control logic measures input signals to correlate data and timing characteristics. The K450 captures and compares data samples. The results are then recorded in memory. The features are menu-driven by resident firmware which is controlled by the Keyboard Panel. The menus allow the user to set up test conditions, capture the results of binary logic states through trace control for data-domain analysis. The pulse train waveforms are displayed for time domain analysis. The display screen presents the results of analysis for examination and/or modification by the user.

Major features of the K450 operation are:

- The K450 equipment functions are menu-driven under the control of a 16-bit, 8086 microprocessor.
- The operating system accommodates up to 512K bytes of RAM and 256K bytes of ROM.
- Three input sections, A, B and C, accept user inputs through probe circuits. Each section is subdivided into two input groups. Each input group accepts 8 data and 2 clock signals to provide 48 data inputs and 12 external clocks.
- Data inputs are capable of being sampled internally at frequency rates up to 200 MHz. Data may be displayed in 40-column Binary, Hexadecimal, Octal, ASCII, EBCDIC, or user defined formats.
- Sample, Glitch, and Latch/Demultiplex input modes are selected in groups of 8 or 16 channels.
- Independent threshold-level selection is provided for each logic probe and group of clocks.
- Up to 16 different state levels for trace control are selected by using the display menus and front panel keys.
- The K450 tracks a 50MHz state machine, while comparing the machine state to four search patterns per level, every 20 ns.
- The trace is recorded in a 48-bit wide x 2051-word length memory.
- A 24-hour Real-Time clock with battery backup feature allows the K450 to log the current time of day and date of each recording.
- The battery backup feature also drives the CMOS memory which preserves the current set up for recording parameters if power is interrupted.
- A built-in Digital Voltmeter (DVM) with input jacks on the front panel provides a 4-digit readout for user convenience.
- A self-contained frequency counter provides automatic measurement of external clock frequency and status.
- The K450 may be operated as a stand-alone unit or linked with the user's system through a RS-232-C or IEEE-488 interface.

- o An optional Disk Storage System (DSS) stores set up information and data on a floppy disk for later analysis. The DSS option also loads and executes disk-based diagnostic routines.

Overview of Manual Contents

The manual is arranged as follows:

Chapter 1. GENERAL INFORMATION - Presents an overview of the K450 operating features, organization of manual contents, service plan, maintenance features, and equipment specifications.

Chapter 2. SYSTEM COMPONENTS AND INTERCONNECTIONS - Describes the interconnection of printed circuit boards, power distribution, external I/O interface, and special tools and test equipment.

Chapter 3. CALIBRATION AND POWER UP DIAGNOSTICS - Describes the power up Boot PROM check, Probe Test, calibration of the Data Display Board, Clock Board, and Threshold/GPIB/RS-232 Board, and measurement of the power supply voltages.

Chapter 4. THEORY OF OPERATION - Presents theory of operation for each printed circuit board and associated circuitry.

Chapter 5. DSS DIAGNOSTICS - Describes each diagnostic module and its associated subtests.

Chapter 6. OPTIONS INSTALLATION Provides procedures for installing the Expansion Option for the B and C section inputs and the Disk Storage System (DSS) Option equipment.

Chapter 7. SCHEMATIC DIAGRAMS AND PARTS LISTS - Provides reference material such as schematic diagrams, assembly drawings, and parts lists.

SERVICE PLAN

The service plan for the K450 involves the use of diagnostic routines to isolate a defective circuit function. The K450 has diagnostic routines that perform a check of major circuit functions whenever the unit is reset or powered up from a cold start. Malfunctions detected by the diagnostics may be tested further by using the DSS routines to isolate the cause of failure.

The resident firmware also generates special displays which permit the user to conduct input Probe Tests and perform CRT alignment. The diagnostic should be rerun after a repair is completed to verify the problem is resolved before the unit is placed into operation.

Power Up Diagnostic Routines

The Power Up Diagnostic routines indicate system operational status. Messages are displayed on the screen to identify the type of error condition and the failed function. Since several components may be associated with the malfunction, boardswapping and rerunning the diagnostic may fix the problem. To avoid possible damage to equipment, do not remove or install a printed circuit board while ac or dc power is applied to the unit.

The following circuits are tested by the Power Up Diagnostic routines:

- o MPU Board RAM Test
- o MPU Board ROM Test
- o Keyboard Matrix Test For Stuck Keys
- o System Voltage Tolerance Test
- o Display Board CMOS RAM Test
- o Threshold/GPIB/RS-232 Board Check
- o DSS Recognition Check
- o Data Board Recognition Check
- o Clock Board Recognition Check
- o Control Board Recognition Check

DSS Diagnostic Routines

The K450 Disk Storage System (DSS) option loads diagnostic routines from the disk to further isolate the cause of failure to a specific circuit or component. The DSS diagnostic provides flexibility for the user to set up test parameters that halt on error, loop on error and perform repetitive tests for a specified pass count. The DSS diagnostic is described in Chapter 5.

A separate diagnostic routine is provided for each component. The diagnostic does not assume any part of the system is functional until it has passed its associated subtests. If a failure is detected, the diagnostic generates an error message identifying the cause of failure. A Self Test menu is displayed when the DSS diagnostic is invoked.

The following software is contained on the diagnostic disk:

- o Diagnostic Storage System (K450)
- o Keyboard/Display Diagnostic Module (KDDIAG)
- o Threshold/GPIB/RS-232 Diagnostic Module (THDIAG)
- o Control Board Diagnostic Module (CBDIAG)
- o Clock Board Diagnostic Module (CKDIAG)
- o Data Board Diagnostic Module (DBDIAG)
- o Storage System Controller Diagnostic Module (SCDIAG)

When the user selects a test for execution, the diagnostic test monitor generates detailed sub-menus that direct the user in running the test procedure.

MAINTENANCE FEATURES

The K450 contains additional built-in features that aid in maintaining the equipment. These features allow the user to test the sample and clock in-puts at each probe and to align the CRT display characteristics.

Probe Test

Two Probe Test connectors allow the user to verify that two clock inputs and eight data inputs supplied from each probe, operate within acceptable limits. A test pattern generated by the K450 firmware is supplied to the probe under test. Procedures for conducting the Probe Test are described in Chapter 3.

Display Calibration Pattern

Procedures for calibrating the CRT are described in Chapter 3. The Display Calibration Pattern, is used by holding the SHIFT key while powering up the unit. This pattern allows the user to make adjustments on the Display printed circuit board for calibrating the following display items:

- Vertical Height
- Vertical Hold
- Horizontal Width
- Horizontal Linearity
- Vertical Linearity
- Focus
- Brightness

SPECIFICATIONS

The following is a summary of the physical, environmental, and operating characteristics of the K450.

K450 Unit Configurations

016 Unit:	Provides inputs for 16 data signals @ 100 MHz (8 data signals @ 200 MHz) and 4 clocks via input Section A.
032 Unit:	Provides inputs for 32 data signals @ 100 MHz (16 data signals @ 200 MHz) and 8 clocks via input Sections A and B.
048 Unit:	Provides inputs for 48 data signals @ 100 MHz (24 data signals at 200 MHz) and 12 clocks via Input Sections A, B, and C.
Expansion Option:	Each data board provides probe inputs for 16 add-on data signals at 100 MHz (8 data signals @ 200 MHz) and 4 additional clocks through input Section B or C.
DSS Option:	Disk Storage System provides two 5 1/4" floppy disk drives mounted in an add-on assembly unit which provides 312K bytes of storage per disk.

Power Requirements

Input Frequency:	50 or 60 Hz
Input Voltage:	90 to 135 Vac or 180 to 270 Vac
Input Power:	500 Watts without DSS option or 550 Watts with DSS option

Fuses For Rated Voltage:

Voltage Range	Fuse
90 Vac to 135 Vac	3AG, 8 Amp
180 Vac to 270 Vac	3AG, 4 Amp

Physical Dimensions and Weight

Height:	8.6 inches (21.8 CM) without DSS, 12 inches (30.1 Cm) with DSS
Width:	17.5 inches (44.5 CM)
Depth:	24.7 inches (62.7 CM) including handle
Weight:	45 lbs. (20 kg) without probes or DSS
	55 lbs. (25 kg) without probes

Environmental Limits

Ambient Temp:	39 to 115 Deg.F (4 to 46 Deg.C) OPERATING
	-8 to 117 Deg.F (-20 to 50 Deg.C) STORAGE
Relative Humidity:	20% to 80% OPERATING
	1% to 95% STORAGE
Max Wet Bulb:	78 Deg.F (25 Deg.C) OPERATING
	No condensation STORAGE

Probes

Loading Characteristics:

Signal Inputs

Input Resistance: 1 megohm referenced to threshold

Input Capacitance: <= 6pF (<= 15 pF with flying leads)

NOTE: Input resistance may approach 500K ohms at voltages exceeding ±15 volts from threshold.

Maximum Input Without Damage:	±50 volts, peak
Common Mode Range:	±0.5 volt max between probe and unit probed
Ground Input:	Input resistance is 91K ohms referenced to chassis
Probe Transfer Characteristics:	Bandwidth to 90% volts out: = >100 MHz
Minimum Swing For Output:	Threshold ±0.20 V maximum
Threshold Variance:	±15 mV maximum, between input signals;
	±30 mV maximum, any two probes
Input Compensation:	Even to 20% overcompensated
Thresholds:	Thresholds are independently selectable for each probe:

TTL, +1.4 volts

ECL, -1.3 volts

VAR A and VAR B

NOTE: Variable thresholds may be set from -9.99 to +9.99 volts in 0.01 volt increments. Accuracy of all threshold voltages is 30mV.

Polarity: + or - is selectable for each signal

Data Inputs

16, 32, or 48 (@100 MHz); or 8, 16, 24 (@ 200 MHz) data inputs configured in one two or three input sections, A, B and C. Each section contains two input groups that accept 16 signals. One group for lower Bits 7-0 at 100 or 200 MHz, the other group for upper Bits F-8 at 100 MHz.

Input Modes: Sample Mode

Latch and Demultiplex Mode

Glitch Mode

Input Frequency: dc to 100 MHz (data)

dc to 50 MHz (clocks)

Clocks

The 16-input configuration provides 2 Sample (edge-sensitive) clocks and 2 Latch Enable (level sensitive) clocks for a total of 4 external clocks.

The 32-input configuration provides 6 Sample (edge-sensitive) clocks and 2 Latch Enable (level-sensitive) clocks for a total of 8 external clocks.

The 48-input configuration provides 6 Sample (edge-sensitive) clocks and 6 Latch Enable (level-sensitive) clocks for a total of 12 external clocks.

Internal: Internal clock is selectable from 20 ns (50 MHz) to 100 ms (10 Hz) in decades of time which is divided by units of 1 to 10 (100 ns, 1 us, 10 us and 1 us, 2 us, 3 us,... 10 us). One internal clock may be programmed per recording. This clock is edge sensitive. A 10 ns (100 MHz) or 5 ns (200 MHz) clock is available to the sample/store sections in addition to the external clock. This clock is edge sensitive.

External: Six external clock inputs which may be combined to form three Sample clocks, three Latch Enable clocks, and one Master (M) clock.

Sample Clock: One sample clock may be specified for each input section (A B, or C) to hold data for the master clock, or move trace data into memory (effective for internal, external, 200 MHz, and 100 MHz clocks). This clock is edge sensitive.

Latch Clock: A special case of Sample Mode which is used to temporarily hold (by latch) the first byte of multiplexed data. When the latch clock goes false, data are held in the input latched until the latch clock returns true.

The master clock then moves the sample into the pipeline (effective for external clocks only). This clock is edge sensitive.

M-Clock: The master clock is used to shift samples into memory and the trace control logic (effective for internal or external clocks). This clock is edge sensitive.

External Clock Specification

Frequency: dc to 50 MHz

Pulse Width: 8 ns Minimum

Clock Skew: 7 ns Maximum between any two clock combinations

Latch Clocks Setup: 13 ns Minimum before Sample Clocks

Clock Frequency: The K450 automatically measures the external clock frequency from 100 Hz to 50 MHz with 0.1% accuracy.

Data Setup and Hold Time

Data must be present 12 ns (maximum) before, and stable until, the clock active edge. Typical setup time is 8 ns.

Data may change zero ns after the clock active edge "0 Hold Time."

Minimum detectable pulse width is one clock period +5 ns.

DVM Input

Range: ±20 Vdc Maximum

Resolution: 20 mv

Input Impedance: 20k ohms

Accuracy: ±0.5%

Signal Outputs

VIDEO, BNC Connector: 1 Vp-p into 75 ohms composite video output is compatible with RS-170

CLOCK, BNC Connector: ECL active low corresponds to the internal clock

GET, BNC Connector: Group execute trigger pulse output for the IEEE-488 Command - TTL

TRACE BNC Connector: TTL high output when trace is enabled

Two LEMO Connectors:	+5V and -5.2V @ 300 mA

Memory

The K450 contains main memory M, storage memory A, and reference memory B. Memory M is organized as 2,048 by 20, 36 or 52 bits. Four bits of each word are used to store the level at which data were recorded. The CPU reads data from M into A or from A into B. Both A and B are a part of the CPU memory.

The operating system accommodates up to 512K bytes of RAM and 256K bytes of ROM under the control of the 16-bit, 8086 CPU.

Trace Control

Trace control employs 16 trace levels defined by user inputs through the display screen and keyboard. Four commands are decoded for each of the sixteen levels. The four commands are TRACE, STOP, JUMP, and ADVANCE. Control begins at level zero.

A delay counter may be programmed from 1 to 65,535 clocks or events to begin tracing after a specified condition occurs. The rear panel BNC output for TRACE is at a TTL level that goes high while the K450 is tracing.

Interface

One RS-232-C Serial I/O Port configured as Data Terminal Equipment (DTE) six wire system.

One Auxiliary Serial I/O Port for RS-232-C (reserved for K450 options).

One IEEE-488 Bus Interface, Parallel Port with Talker/Listener configuration selectable by the user through software control.

Timer:	A 24-hour, time and date clock is backed up by a 2.9 V battery
Backup Memory:	A 2k x 16 CMOS memory with battery backup saves the last setup of recording parameters if power is interrupted or when the unit is turned off.

Keystroke Tone Signal

A beeper indicates keystroke errors and is enabled by the user through a menu display.

Chapter 2

SYSTEM COMPONENTS AND INTERCONNECTIONS

INTRODUCTION

This chapter describes individual printed circuit boards and components that comprise the K450 Logic Analyzer. Information is also included for the interconnection of these boards and recommended equipment. Front and rear views of the K450 chassis are shown in Figures 2-1 and 2-2.

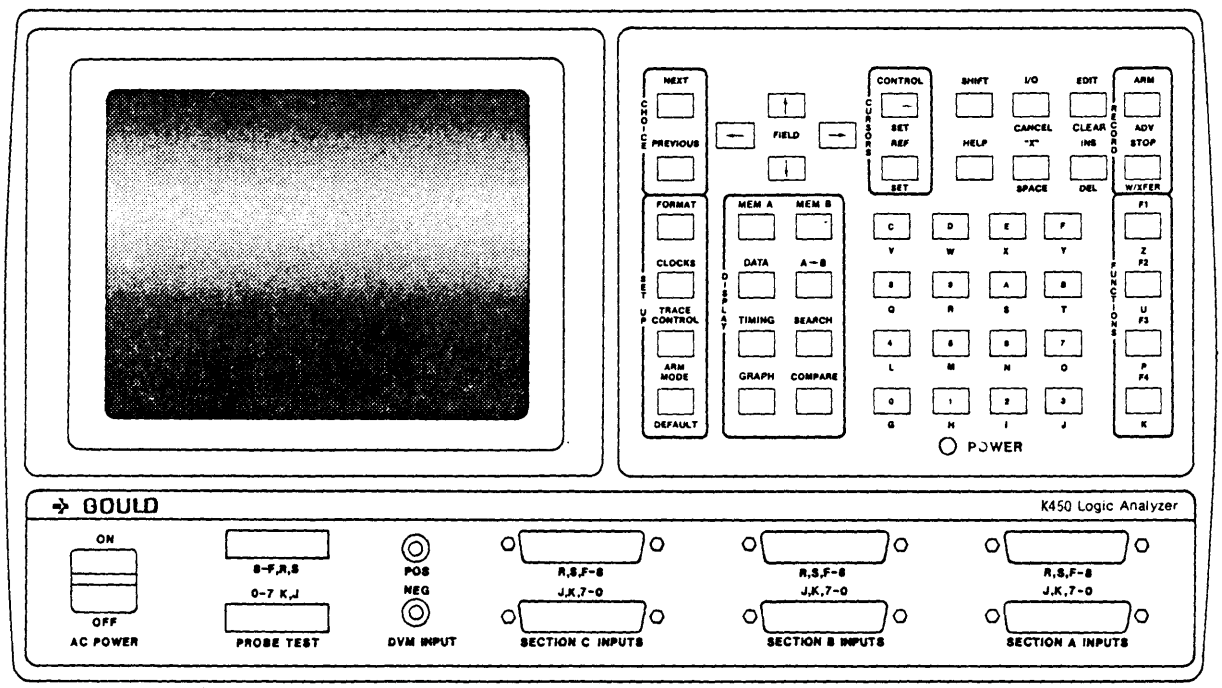


Figure 2-1. K450 Front Panel Arrangement

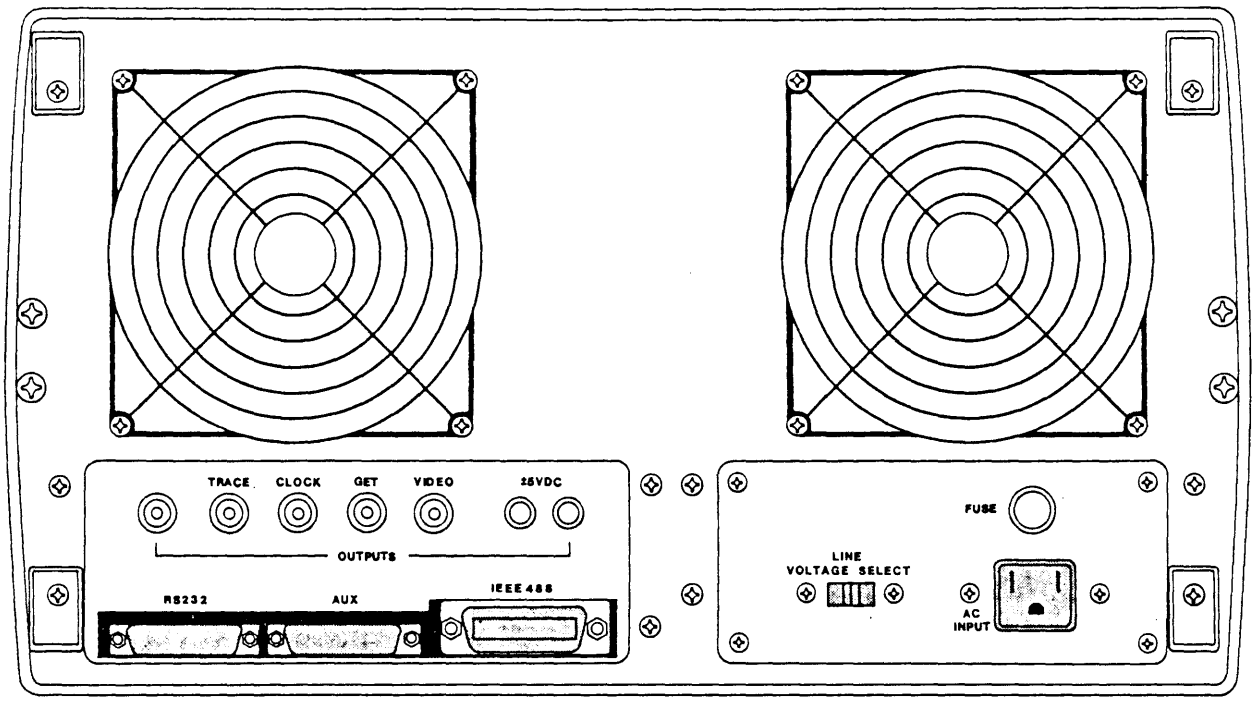


Figure 2-2. K450 Rear Panel Arrangement

BOARDS AND COMPONENTS

The following boards and components are used for K450 hardware configurations:

- o Keyboard:

  The keyboard has 48 keys, several can be shifted to perform a second function. Because of the shift capability, 20 keys can perform as a full alpha-numeric keyboard.

- o Front Connector Panel:

  The front connector panel has the following components:

  - Six DB-25 female connectors for external data/clock input
  - Two jacks for DVM (POS and NEG) input
  - Two card-edge female connectors for PROBE TEST output
  - Power LED indicator
  - ac power switch

- The data/clock input connectors available for 16, 32 or 48 input configuration are established by the number of Data Boards installed. The unit may be configured with one, two or three Data Boards. These Data Boards have 16, 32 or 48 inputs. The Configuration Display screen indicates the number of active connectors present for a given instrument.

- Illumination of the Power LED indicator also indicates the presence of +5 Vdc when ac power is applied.

o Display Assembly:

The display assembly has a 8-inch, P39 CRT and a CRT deflection yoke with cable harness. The mounting bracket for the assembly is an integral part of the CRT glass envelope.

o Rear Connector Panel:

The rear connector panel provides external interface for signal I/O and power through the following circuit components:

- Signal output is provided for VIDEO, CLOCK, TRACE, and GET through four BNC connectors.

- The + 5V and - 5V output is provided by each of two LEMO connectors

- Signal I/O is provided by one IEEE-488 connector and two RS-232 connectors. One RS-232 connector is labeled AUX and is intended for future options.

- Power Interface is provided by the 120/240Vac line voltage input socket and the line voltage select switch (for 120/240 Vac). The power fuse is rated at 8 Amp, 3AG for 120 Vac or 4 Amp, 3AG for 240 Vac power input.

o Power Supply:

The power supply provides the following outputs:

+ 5Vdc at 11 Amps

- 5.2Vdc at 36 Amps

+15Vdc at 3.0 Amps

-15Vdc at 0.2 Amp

-2Vdc at 17 Amps

o Data Board:

The Data Board Assembly interfaces the ECL devices of the probes to the TTL devices of the board. The Data Board processes 16 inputs. Either one, two or three Data Boards will be installed in a given system configuration as determined by the 16, 32 or 48 input capability.

- The Data Board main memory (M) is 2,048 bits deep by 48 bits wide and gathers data at 200 MHz in store mode input.

o MPU Board:

The MPU Board Assembly contains the 8086 microprocessor and operates as the controller for K450 operations. The firmware resides in ROM located on the MPU Board.

o Control Board:

The Control Board Assembly provides the user with a menu driven display that allows 16 trace levels to be programmed by the user. A selection of qualifiers enables the user to pick and choose the information that will be recorded. The Control Board also provides an output signal to the rear panel TRACE BNC connector.

o Threshold/GPIB/RS-232 Board:

The Threshold/GPIB/RS-232 Board Assembly provides fixed and variable threshold voltages for the probe pods. This board provides two RS-232 ports and one IEEE-488 Talker/Listener port. This board also has control circuits for DVM input and provides an output signal to the rear panel GET BNC connector.

o Data Display Board:

The Data Display Board Assembly contains the keyboard scanning circuitry and the horizontal and vertical and high-voltage circuitry for the CRT. In addition this board contains the interface for two 5 1/4 -inch floppy disk drives and the Keyboard Assembly. This board provides a video composite signal (8 MHz dot clock frequency) to the rear panel VIDEO BNC connector.

o Clock Board:

The Clock Board Assembly processes the external clocks from the probes and provides a range of internal clocks for the system. This board also provides an output signal to the rear panel CLOCK BNC connector and test pattern signal to the two front panel PROBE TEST sockets.

BOARD AND COMPONENT INTERCONNECTIONS

Boards

The K450 printed circuit boards are contained in an eight-slot card cage, and are interconnected through a mother board. Interconnection of the printed circuit boards to the front and rear connector panels is provided by flat cables that mate to connectors located along the upper edges of the board. See Figure 2-3 for the system interface.

Components

Because the K450 is a compact unit, the cable harnesses to the mother board, and to the Data Display Board are short. The mother board is connected to the keyboard by a short, flat cable.

The optional Disk Storage System (DSS) has two disk drives and a disk controller interface board. The DSS I/O signal interface is provided by a flat cable that mates to a connector (P4) located on the Data Display Board. The power supply harness interfaces to a harness connector located on the base of the chassis. All interface cables required for the DSS installation are included with the DSS kit.

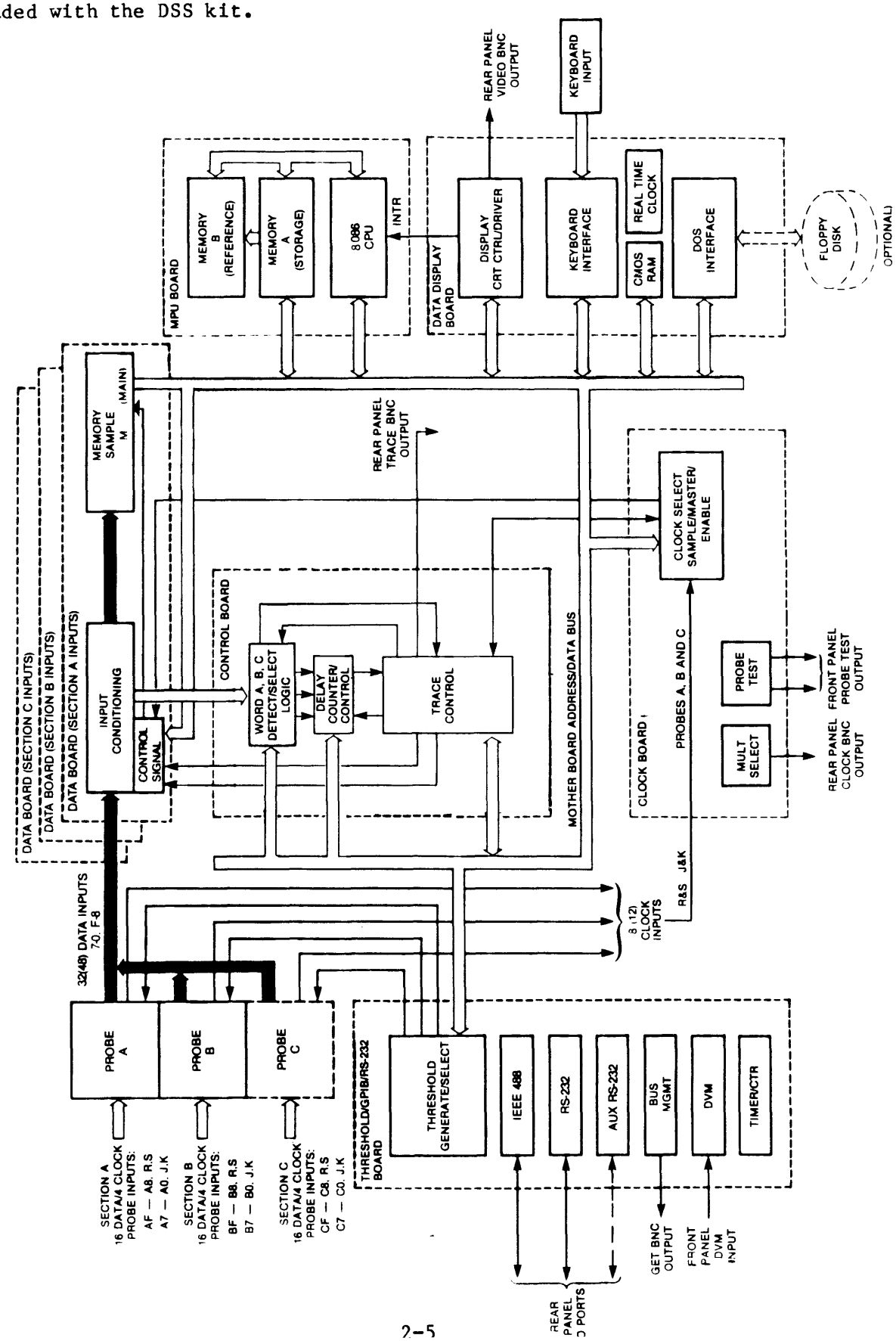


Figure 2-3. K450 System Interface of Components to Mother Board

CARD CAGE ARRANGEMENT

The K450 card cage arrangement is shown in Figure 2-4. The board ejector tabs on each printed circuit board are numbered to correspond to the assigned slot location in the card cage. The assigned board is dedicated to reside in its slot, except where noted below for the three Data Boards.

Data Board Configurations

Three Data Boards reside in slot locations A2, A3, and A4. The ejector tabs are not numbered on these boards, because each board is identical and is interchangeable for these slots. Each slot location has a specific SECTION INPUT, as shown in Figure 2-4.

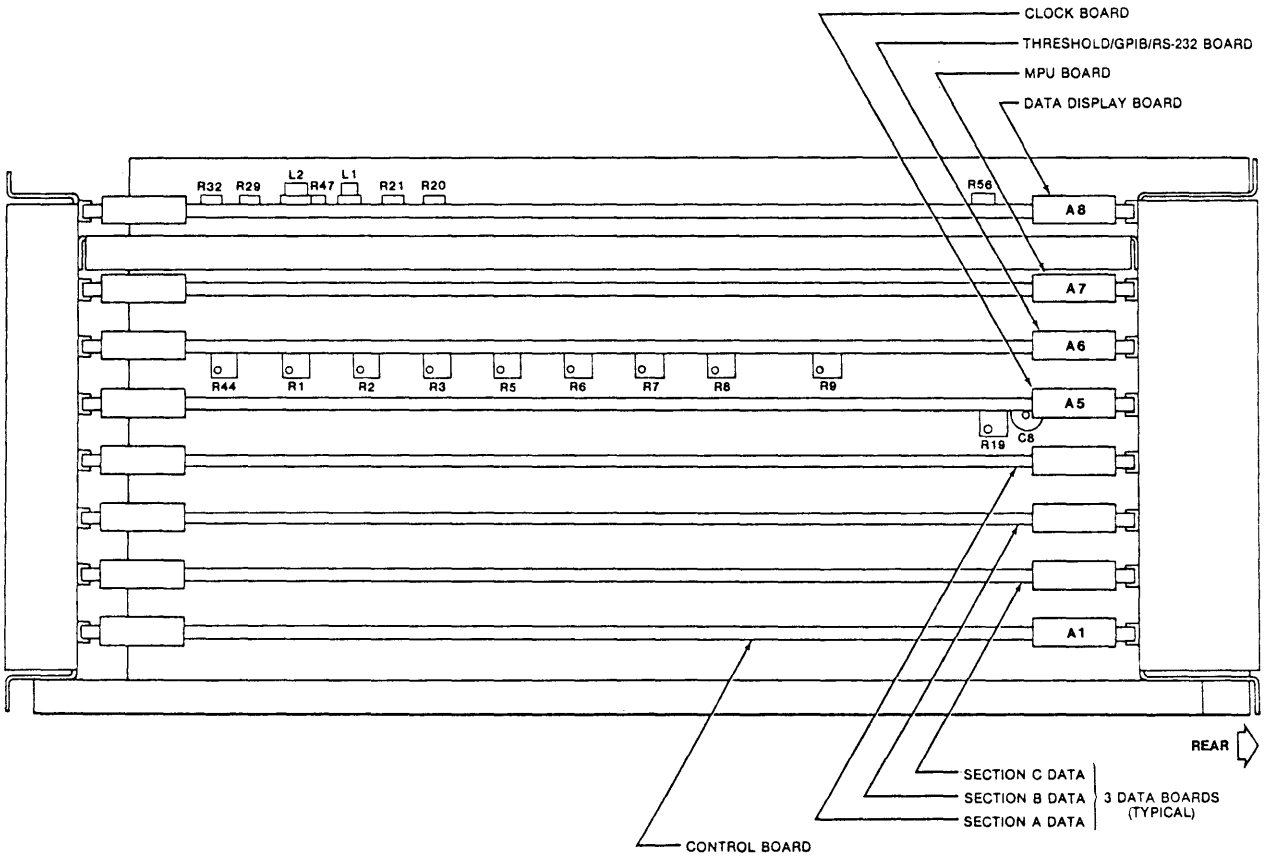


Figure 2-4. K450 Card Cage Arrangement

The K450 configured for 16 inputs (Section A) uses one data board installed in slot A. An instrument configured for 32 data inputs (Sections A and B) uses two Data Boards installed in slot locations A4 and A3. Instruments configured for extended 48 data inputs (Sections A, B and C) use an additional Data Board installed in slot location A2.

Board Calibration Controls

The Data Display, Threshold/GPIB/RS-232 and Clock boards have controls for calibrating circuit functions. The location of these controls is shown in Figure 2-4. The procedure for performing the calibration adjustments is described in Chapter 3. The following circuit functions are adjusted by these controls:

CARD CAGE LOCATION	BOARD NAME	CIRCUIT FUNCTION ADJUSTMENT
A8	Data Display	R20, CRT Vertical Height R21, CRT Vertical Hold R29, CRT Focus R32, CRT Brightness R47, CRT Vertical Linearity R56, Audio Alarm Volume L1, CRT Horizontal Width L2, CRT Horizontal Linearity
A6	Threshold/GPIB/RS-232	R1, R2, Variable B Threshold R3, R5, DVM Voltage R6, R9, Variable A Threshold R7, ECL Threshold R8, TTL Threshold R44, Reference Voltage (+ 10V)
A5	Clock	R19, C8 100 MHz Clock (Oscillator Circuit)

SUGGESTED TEST EQUIPMENT

The following is a list of the suggested test equipment for servicing the K450 Logic Analyzer:

ITEM	DESCRIPTION
Extender Board	Gould Part Number 0117-0195-01
Digital Multi-meter	4 1/2 Digits, dc Accuracy of +/- (0.03% of reading + 2 digits)
Frequency Counter	Capable of 0.01% accuracy on ECL at 100MHz
Oscilloscope	350 MHz band width, Horizontal Resolution to 1 ns/DIV
Logic Analyzer	Any current Gould production model
20-Pin, 0.3" IC Clip	Standard
3 Mini Clips/Grabbers	Standard
4.7K-Ohm, 1/4 W, 5% Resister	Standard

Chapter 3

CALIBRATION AND POWER UP DIAGNOSTICS

GENERAL

This chapter describes the K450 Power Up diagnostic test routines and procedures for calibrating system components. This information is organized as follows:

- Power Up Diagnostics
- Probe Test
- Display Calibration
- Power Supply Voltage Measurements
- Threshold Voltage Calibration
- DVM Circuit Calibration
- Internal Clock Adjustment

POWER UP DIAGNOSTICS

The Power Up Diagnostic test verifies the readiness of hardware components whenever the K450 is powered up from a cold start or restarted. The power up diagnostic is implemented by software in the EPROM firmware located on the MPU printed circuit board.

Diagnostic Operation

As soon as the AC POWER switch is turned ON, the K450 beeps and executes the diagnostic test routines. As each test is completed, the next test is run. When all tests are successfully completed, the Configuration screen displays the current hardware configuration. The K450 is ready to accept user inputs.

The power up diagnostic is also initiated when the SHIFT and DEFAULT keys are pressed to reset system operations. The power up diagnostic runs for approximately ten seconds to check certain components and perform a series of tests. The following tests and checks are performed by the power up diagnostics:

- Microprocessor RAM Test
- Microprocessor ROM Checksum Test
- Keyboard Stuck Key Test
- System Voltage Test
- Display Board CMOS RAM Test
- Threshold/GPIB/RS-232 Board Check

- o DOS Recognition Check
- o Data Board Recognition Check
- o Clock Board Recognition Check
- o Control Board Recognition Check

User Interaction

If an error is detected in any of the tests, the name of the failed test is displayed and testing is stopped. To run the remaining power up tests, or to attempt operation of the instrument despite the error condition, press the NEXT key to resume testing. Press the PREVIOUS key to repeat the test. After the last test is executed, the Configuration screen is displayed. Since an error was detected, the disk-based diagnostic test is used to further isolate the cause of the error.

As each power up diagnostic test is executed, the name of the test is displayed on the CRT. If the test is run successfully, PASSED is printed after the test name. The first failure in a test is indicated by FAILED, which is printed after the test name. A test-results header is then printed on the next line and the results of the test are printed on subsequent lines. Any more failures causes the results to be printed on successive lines. A description of the diagnostic tests is given in in this chapter.

Microprocessor RAM Test Description

The Microprocessor RAM Test is executed by writing and reading bits in a test pattern as follows:

1. Write 0000 to address locations 0000-FFFF.
2. Read 0000 from address locations FFFF-0000 and write FFFF at each location.
3. Read FFFF from address locations 0000-FFFF and write 0000 at each location.
4. Read 0000 from address locations 0000-FFFF and write FFFF at each location.
5. Read FFFF from address location FFFF-0000 and write 0000 at each location.

This test is repeated, changing the segment registers so that RAM address locations 0:0000 to 7000:FFFF are all tested. If all test patterns are read back successfully, the following is displayed:

MICROPROCESSOR RAM TEST - PASSED

If any bits fail, the following is displayed:

MICROPROCESSOR RAM TEST - FAILED

MPU MEMORY FAILURE

```
MAP OF RAMS ON MPU BOARD (G = GOOD,  X = BAD)

COL--->      4      6
ROW
  |    A     G      X
  V    B     G      G
       C     G      G
       D     G      G
       E     G      X
       F     G      G
       G     G      G
       H     G      G

Please press NEXT to continue.  PREV to repeat.
```

Where: COL and ROW positions correspond to the RAM socket locations on MPU board.

Microprocessor ROM Checksum Test Description

The ROM Checksum Test computes 16-bit checksums for each of the ROMs which are numbered from 1 to 10. The computed checksum values are then compared with the expected values which are stored in the top of ROMs 1 and 2. If the values match, the test is successful and the system proceeds to the next test.

If the values do not match, the error display indicates the ROM number, the expected checksum value, and the actual checksum value. Note that a missing ROM generates the following:

```
ROM CHECKSUM TEST      FAILED

 ROM          EXPECTED      ACTUAL
NUMBER       CHECKSUM      CHECKSUM

  2            463B        ALL "FF"
```

Keyboard Stuck Key Test Description

This test performs a check of the keyboard matrix for stuck keys.

If one or more keys are stuck, the affected key(s) is displayed below the test failed message, in a matrix that is continuously updated.

If all keys were stuck, the following is displayed on the CRT screen:

```
KEYBOARD STUCK KEY TEST -     FAILED

NE  ^  >  CN SH IO ED AR
PR  <  v  RF HL SP IN ST
FO  MA MB C  D  E  F  F1
CL  DA AB 8  9  A  B  F2
TR  TI SE 4  5  6  7  F3
AM  GR CM 0  1  2  3  F4
```

When all keys are unstuck, the test is successful and the system goes to the next test.

Voltage Test Description

The following voltages are checked by the power up diagnostic:

+15.00 Vdc

-15.00 Vdc

-10.00 Vdc

+5.04 Vdc

-5.28 Vdc

-2.08 Vdc

V BATT

Tolerance for the +15V test is +0.5 Vdc. The tolerances for remaining voltages have been set to +/- 10%. The testing sequence is as follows:

1. The +15V test is repeated up to 100 times. If the voltage returned is not within the tolerance limit on or before test 100 occurs, the test has failed.

2. If the +15V test is successful, remaining voltages are tested. A failed condition occurs if any of the voltages are not within acceptable limits.

3. For each voltage that fails, the following is displayed on the CRT:

   - Name of voltage being tested

   - The minimum voltage limit

   - The maximum voltage limit

   - Measured voltage value (average and peak-to-peak) which was read.

Display Board CMOS RAM Test Description

The CMOS RAM is backed up by batteries to store setup parameters for recording information. This test compares stored data with a stored checksum value. A failure displays an error message:

CMOS RAM TEST FAILED

An error indicates the K450 will not restore the recording setup parameters nor correctly save new parameters. The error does not always indicate a component has failed. The source of failure could be a soft error. Pressing the NEXT key resumes the diagnostic. If the original error was not caused by a component failure, the CMOS RAM TEST ERROR should not appear on the next power up and the CMOS memory should operate correctly.

PROBE TEST

Two front panel connectors, labeled PROBE TEST, are used to check the probe circuitry. The test is performed on eight ample data input signals of each probe and J and K clock input using the external clock set-up.

NOTE: The clocks are not checked by this test.

Probe Test Pattern Generator

The Probe Test Pattern Generator is always enabled. The pattern generator circuits send an output signal to the PROBE TEST sockets consisting of a known ring-counter loop and clocking sequence. The pattern generator outputs two clock signals and eight data signals for each PROBE TEST socket. These signals are supplied as input to the probe tip. The clock and data signals output from the PROBE TEST sockets have a voltage swing from 0 to -5 volts.

Trace Control Setup

To setup the trace control, perform the following:

1. Press the TRACE CONTROL key.

2. Press the DOWN CURSOR key once. Press the RIGHT CURSOR key twice.

3. Press the 2, 0, 5 and 0 numeric keys.

Record/Review Test Results

1. Press the ARM key to start a recording.

2. Watch the message located in the lower right of the screen. This status indicates a recording has occurred with the following condition:

   - READY Ready for an ARM signal

   - BUSY Setup internally for a recording

   - EOR End of recording activity

   NOTE: The actual recording occurs quickly. Press the ARM key again to view the display. Press the F1 key to scroll through the input displays until the input signals are shown on the screen.

3. Press the TIMING key and watch the display pattern. A staircase pattern of pulses (shown in Figure 3-1) appears on the screen. This pattern begins at any point on the screen as determined by the Default Setup. Memory is filled with samples starting at Location 0 in the data stream.

4. Use the Control and Reference cursors to measure the total trace time of 10 microseconds and pulse width of 0.9 microsecond. These conditions indicates the probes under test are properly accepting inputs for recording.

Verify a pulse for each channel. If no pulse, reverse the upper and lower probes and repeat the test. A generator malfunction is isolated by swapping the probes. A probe malfunction is isolated by swapping the probe at the input connector. A failure means a problem with cabling or the Data Boards.

5. Repeat the Probe Test for Section B and C Inputs. Verify if these probes are accepting inputs for recording.

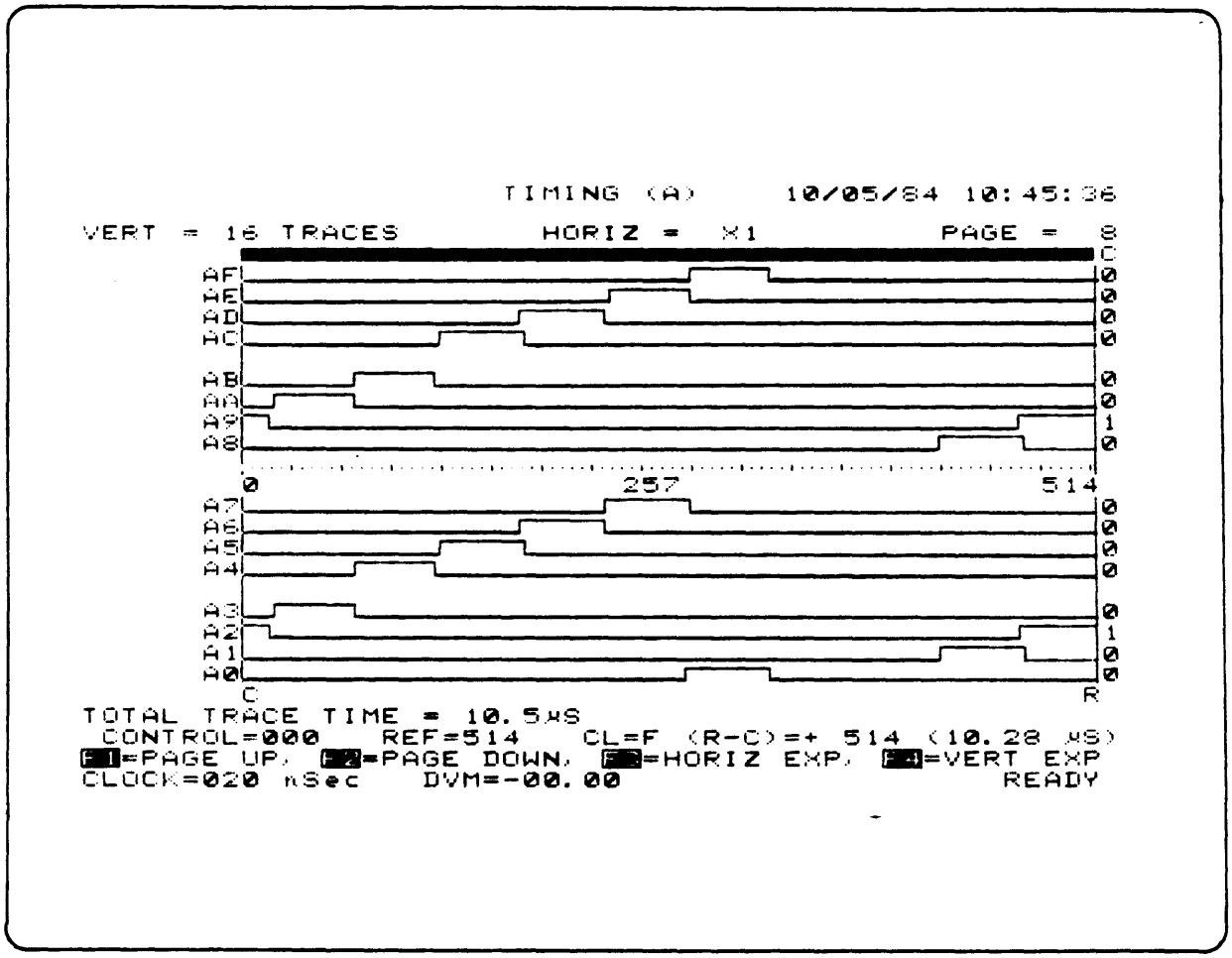


Figure 3-1. Typical Probe Test Recording Using Internal Clock

Probe Connections

The two PROBE TEST sockets allows the low order (bits 7-0) probe and high order (bits F-8) probe of each input section to be tested concurrently. To avoid noise pulses at the other input sections, connect the probe cables to these input sections while conducting the probe test. Use the following procedure to connect the probe cables:

1. Connect the low order bit probe cable to lower front panel socket labeled SECTION A INPUTS (J, K, 7-0). See Figure 3-2 for AJ external clock.

2. Connect the high order bit probe cable to upper front panel socket labeled SECTION A INPUTS (R, S, F-8).

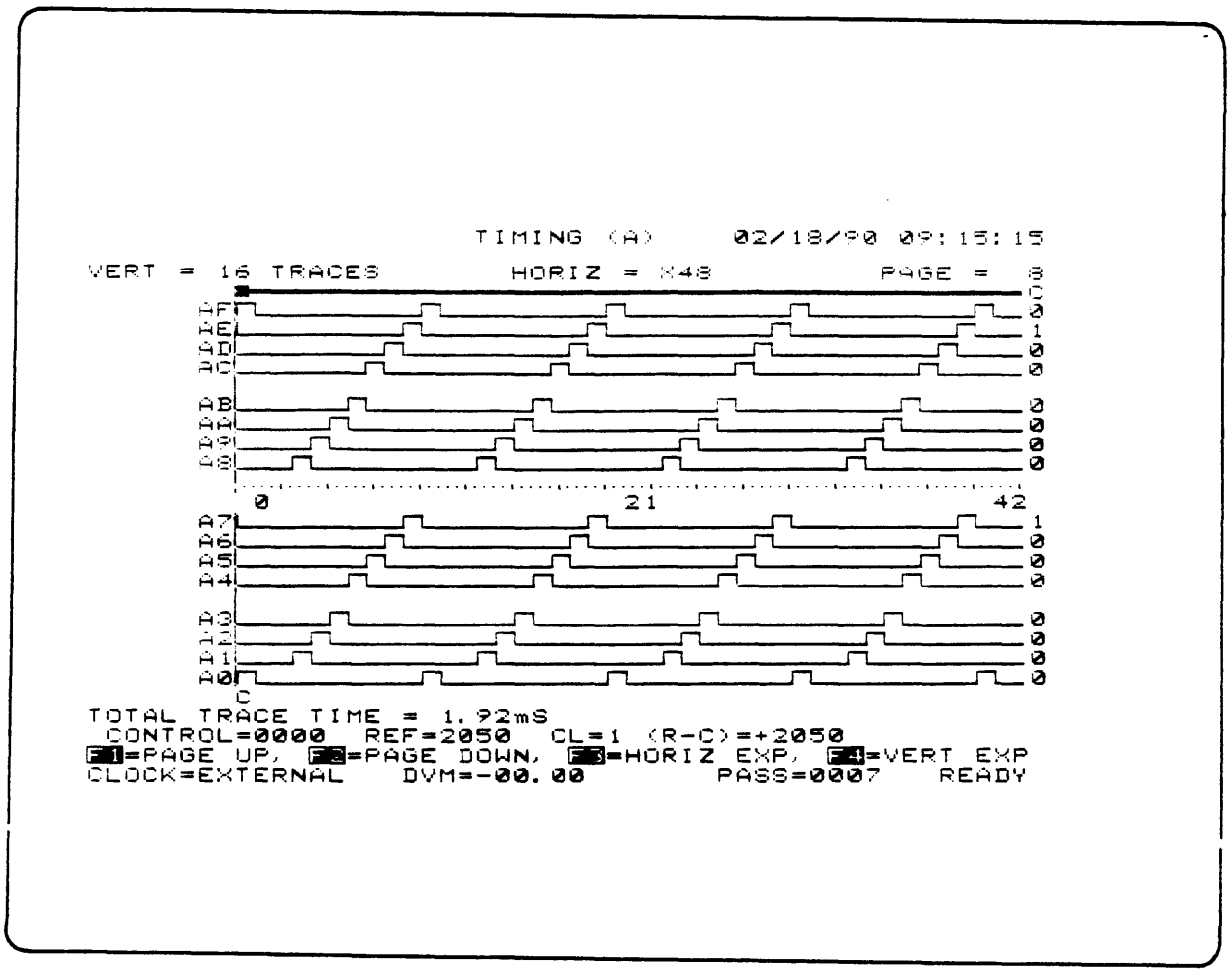


Figure 3-2. Typical Probe Test Recording Using An External Clock

3. Repeat Steps 1 and 2 to connect probe cables to front panel sockets at Section Inputs B and C.

4. Plug the lower order bit probe tip of SECTION A INPUT cable into the lower PROBE TEST socket. Ensure the label faces upward.

5. Plug the high order bit probe tip of SECTION A INPUT cable into the upper PROBE TEST socket. Ensure the label faces upward.

Default Setup

The K450 has CMOS memory backed up by battery to keep the previous set-up parameters. Whenever the unit is powered up from a cold start, the previous set-up parameters are restored. It is necessary to initialize all set-up parameters to their default value as follows:

1. Press the SHIFT and ARM MODE/DEFAULT keys to select the Configuration Screen.

2. Press the F1 Function key to select the Default Setup Parameters.

3. Watch for the following message at the top of the screen:

   Default Setup M and Display values locked in . . .

Fixed ECL Threshold Setup

1. Press the FORMAT key. Verify that the Format Display shows Data Inputs for AF through A0 and Threshold at TTL level.

2. Change the threshold for inputs AF through A0 to ECL by moving the blinking cursor to the AF-A8 line of the Data Inputs display and change TTL to ECL as follows:

   a) Press the F1 Function key to select top of threshold.

   b) Press the FIELD down-arrow key four times to move cursor downward to the AF-A8 line.

   c) Press 1 (numeric) key twice to change the entries to ECL level at lines AF-A8 and A7-A0.

DISPLAY CALIBRATION

The Display Board circuitry does the following:

- Signals that drive the CRT
- Reads the front panel Keyboard
- Controls priorities for interrupt levels
- Controls the Real Time Clock
- Drives the Audio Error Alarm.

```
* * * * * * * * * * * * * * * * * * * * * *
*                  WARNING                  *
*                                           *
*  Hazardous voltages dangerous to life     *
*  are present on the Data Display board    *
*  and CRT. Avoid body contact in these     *
*  areas which could result in injury.      *
* * * * * * * * * * * * * * * * * * * * * *
```

Calibration Requirements

A display calibration pattern is provided by the K450 firmware. This pattern is accessed by pressing and holding the SHIFT key while powering up the unit. Raster adjustments are made with the Data Display board fully installed in the chassis. Use nonmetallic tools when making raster adjustments.

Display Adjustment Points

Center the calibration pattern before making any height, width or linearity adjustments. Use the intersection point of the "X" traces as a reference point and locate the point to the center of the screen by moving the rings on the CRT yoke. See Figure 3-3.

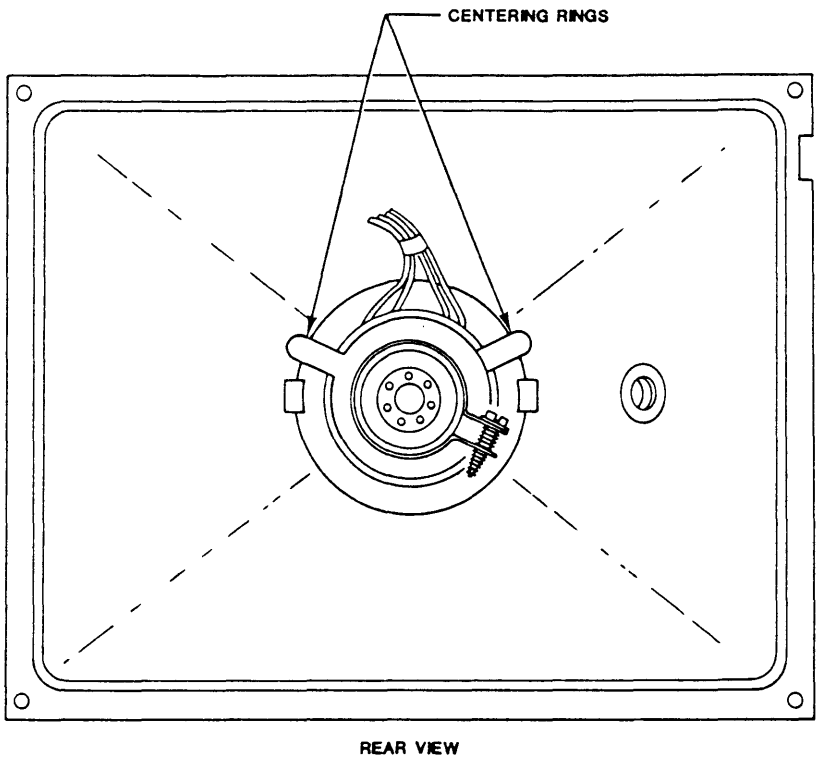


Figure 3-3. CRT Centering Rings

Since all raster adjustments are interactive, recentering the calibration pattern might be required as height, width and linearity adjustments are made. See Figure 3-4 for the location of adjustment controls for VOLUME (R56), VERTICAL (R20, R21 and R47), HORIZONTAL (L1 and L2), FOCUS (R29), and BRIGHTNESS (R32).

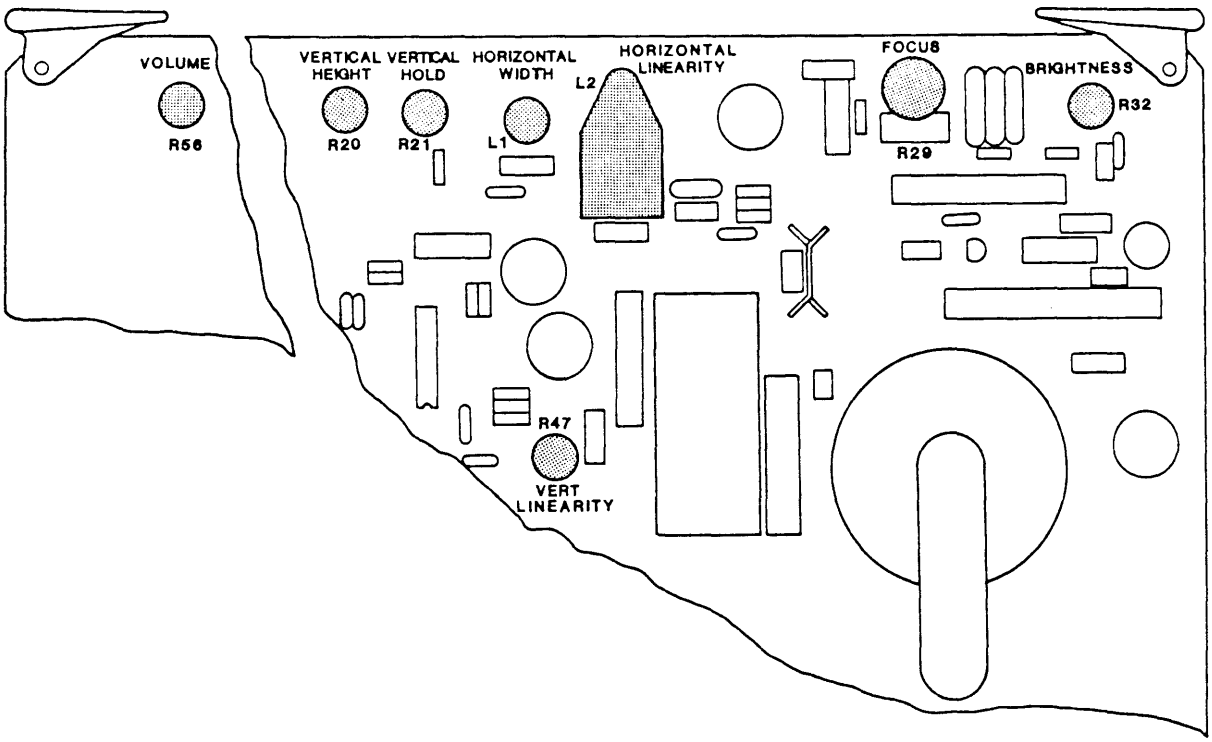


Figure 3-4. Data Display Board Adjustment Points

Adjust the Display board as follows:

1. Turn the power on and verify unit passes the power-up diagnostic test by displaying the Configuration Screen.

2. During power-up test, adjust VOLUME (R56) for good sound. Pressing an illegal Key with the Error Beep on sounds a brief tone. The Error Beep is turned on and off by accessing the Date screen and pressing the FIELD right arrow and NEXT keys to select the Beep parameter.

3. Adjust the VERTICAL HOLD (R21) until the picture locks in on screen.

   NOTE: In further screen adjustments, keep 0.25 inch margins on all four borders.

4. Adjust the VERTICAL HEIGHT (R20), verify that change occurs in the height. Set for the best picture.

5. Adjust the VERTICAL LINEARITY (R47), verify that change occurs in vertical linearity. Set for the best picture.

6. Adjust the FOCUS (R29), verify that change occurs in focus. Set for the best picture.

7. Adjust the BRIGHTNESS (R32), verify that change occurs in brightness. Set for the best picture brightness.

8. Adjust the HORIZONTAL WIDTH (L1), verify that change occurs in width. Set for the best picture.

9. Adjust the HORIZONTAL LINEARITY (L2), verify that change occurs in horizontal linearity. Set for the best picture. Turn the power off.

10. Hold down the SHIFT key and turn the power on. A grid appears on the screen, as shown in Figure 3-5.

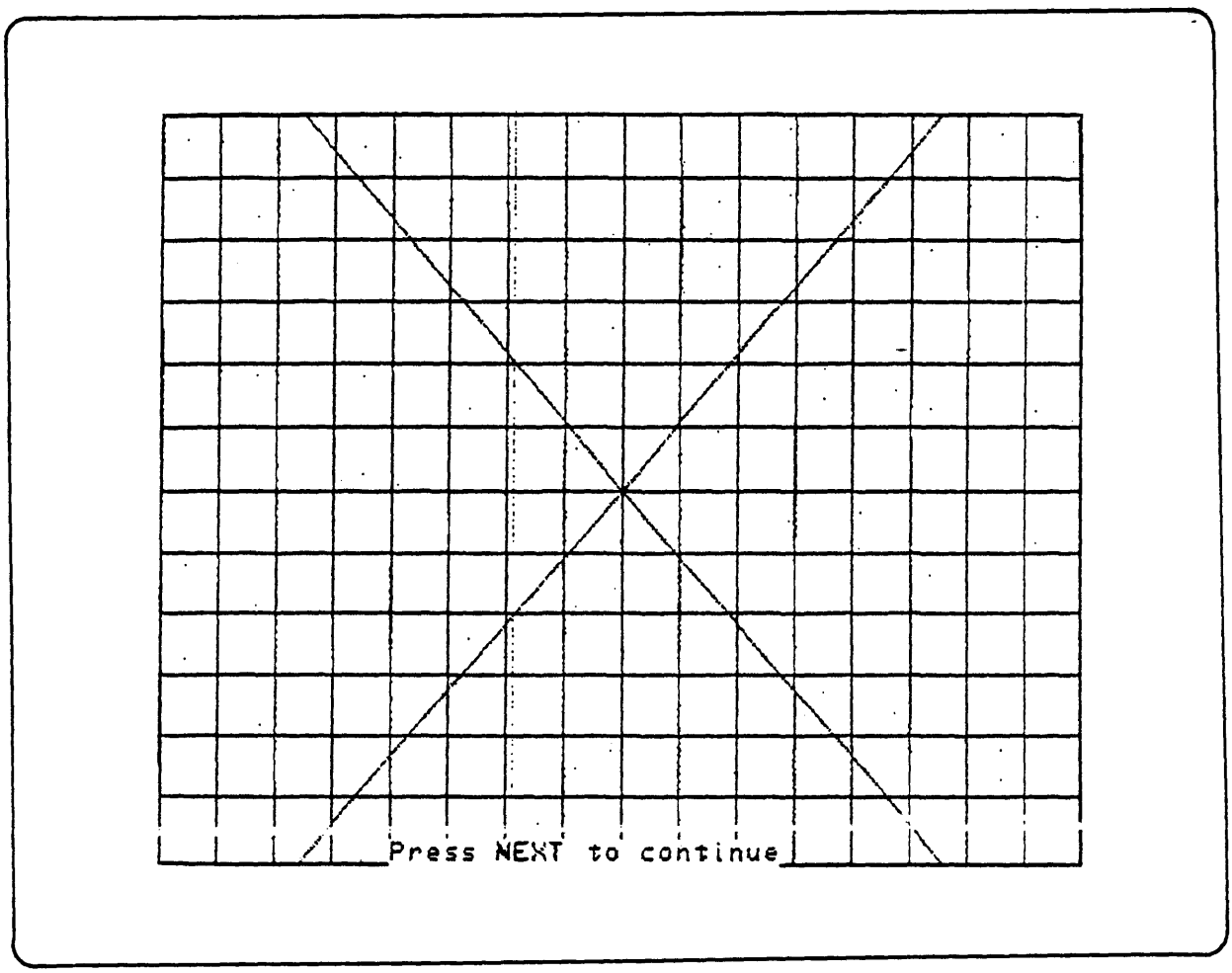


Figure 3-5. CRT Grid Pattern

11. Good linearity and picture is shown by the grid pattern. Repeat the adjustments to get a uniform picture in the display.

12. Verify if the VIDEO output signal at the rear panel BNC connector is present as follows:

    a. Connect a 50-ohm coaxial cable from the Composite Video Out BNC connector of K450 to one input of scope.

    b. Use a 1-Megohm input scope termination.

    c. Set the scope for 1 volt/division and ground.

    d. Verify that a 1.6V pp pulse occurs every 64 usec.

POWER SUPPLY VOLTAGE MEASUREMENTS

The user cannot adjust the K450 Power Supply. A voltage measurement check determines if the power supply is functioning properly. If the measured voltages are not within the specified limits, the power supply must be replaced. Voltages are measured at the power supply terminal board locations, as shown in Figure 3-6. The measurement is taken between the specified voltage signal and its respective return.

NOTE: The power supply should warm up for at least 10 minutes before checking the supply voltages.

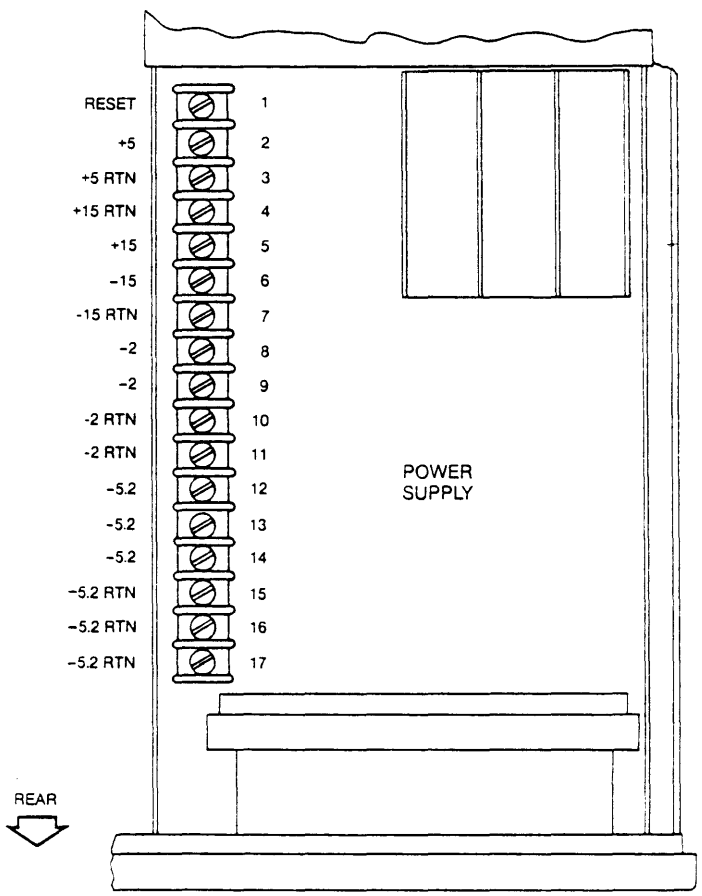


Figure 3-6. Power Supply Voltage Measurements

The measured voltages must be within the following ranges:

NOMINAL VOLTAGE	RANGE MINIMUM		MAXIMUM
+15V	+14.4	to	+15.6V
+ 5V	+ 4.8	to	+ 5.2V
- 2V	- 2.2	to	- 2.0V
- 5.3V	- 5.5	to	- 5.1V
-15V	-15.6	to	-14.4V

THRESHOLD VOLTAGE AND DVM CALIBRATION

The following adjustments are made on the Threshold/GPIB/RS-232 Board:

- o 10V Reference Voltage Adjustment
- o TTL Threshold Adjustment
- o ECL Threshold Adjustment
- o Variable A Threshold Adjustment
- o Variable B Threshold Adjustment
- o DVM Adjustment

The location of potentiometers is shown in Figure 3-7. The following tools and test equipment is required:

- o Extender Board: Gould Part Number 0117-0195-01
- o Digital Multimeter: 4 1/2 Digits, DC accuracy of +/- (0.03% of Reading plus 2 Digits)
- o 4.7K-Ohm, 1/4 W, 5% Resistor: Standard
- o External voltage source of +/- 20.000 Vdc +/- 3mV

Use the following procedures to make the adjustments:

NOTE: To set for Threshold adjustments, turn the power off. Turn the power on to get the Configuration screen. Pressing the F1 key moves the cursor to the top Threshold location on the screen.

10V Reference Voltage Adjustment

1. Turn the power off, remove the Threshold/GPIB/RS-232 Board from the card cage and install on an extender board.
2. Turn the power on and verify unit passes power-up diagnostic test by displaying the configuration screen.

3. Connect the external DVM reference (-) to the board A GND test point. Connect the DVM (+) input to the right side of resistor R38. See Figure 3-6.

4. Adjust R44 for a DVM reading of +10.00 +/- 0.01V.

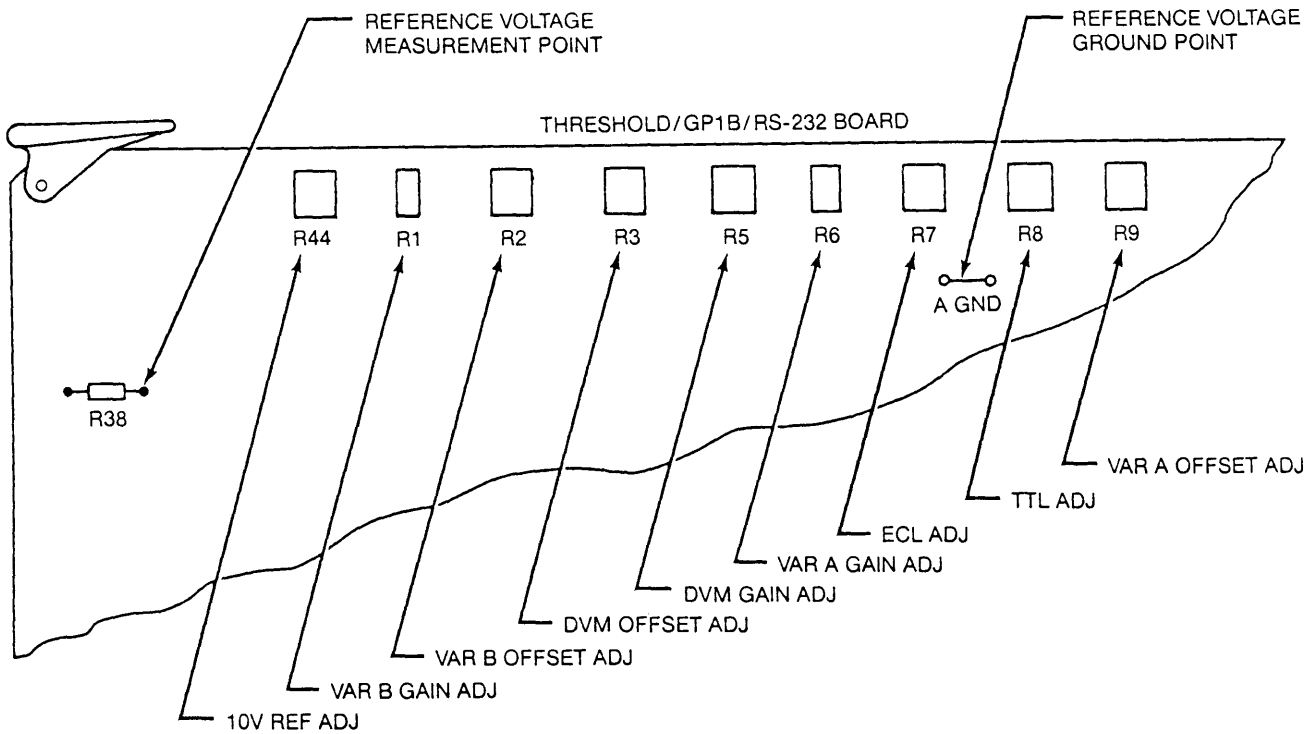


Figure 3-7. Threshold/GPIB/RS-232 Board Adjustments

TTL Threshold Adjustment

Remove all input cables from the unit. This procedure uses a 4.7K-Ohm resistor which serves as a load for adjustment of threshold voltages. All voltages are measured accross the resistor. The TTL adjustment procedure also verifies that no shorts are present between High and Low inputs, and between Data and Clock inputs. The TTL adjustment is performed on each front panel input connector as follows:

1. Configure the K450 unit with three Data Boards to provide 16 inputs at each SECTION Input (A, B, and C).

2. Install the 4.7K-Ohm resistor between sockets 2 (ground) and 14 (Clock Threshold input) at SECTION A (bits 7-0). Connect the DVM positive (+) lead to socket 2 and the DVM negative (-) lead to socket 14 so that the voltage measurement is taken across the resistor. See Figure 3-8.

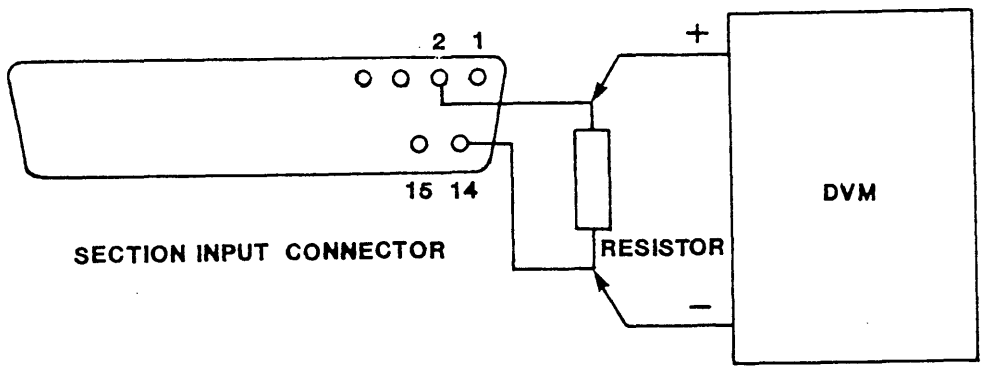


Figure 3-8. Test Connections for Threshold Voltage Adjustment

3. Press the FORMAT Key verify that all Thresholds are set to TTL.

4. Press the ARM key on keyboard

5. Adjust the TTL THRESHOLD (R8) for a DVM reading of +1.400 +/- 25mV.

6. Relocate the resistor to SECTION A Inputs (bits F-8) connector and verify the TTL Threshold of +1.400 +/- 5mV is present.

7. Check the TTL level of other inputs by moving the load resistor to input connectors at SECTIONs B and C. Verify the TTL Threshold of +1.400 +/- 5mV is present at sockets 2 and 14 of each low-byte (bits 7-0) and high-byte (bits F-8) connector.

8. Install the 4.7K Ohm resistor between sockets 2 and 15 (Data Threshold). Repeat steps 3 through 7.

9. Ensure no shorts are present between Low and High inputs, as well as between Data and Clock inputs by performing the following test:

   a. Press the FORMAT key to select the Format M screen. Press the F1 key to move cursor to top Threshold location. Press quick key 1, to change TTL level to ECL.

   b. Move the cursor down by pressing the FIELD down-arrow key once and press quick key 1 to change TTL level to ECL.

   c. Press the ARM key.

   d. Install the 4.7K-Ohm resistor between sockets 2 (ground) and 15 (Data Threshold) of SECTION C upper INPUT Connector.

Connect external DVM positive (+) lead to pin 2 and negative (-) lead to pin 15. Verify that the ECL Threshold of -1.300V +/- 25mV is present.

e. Install the 4.7K-Ohm resistor between pin 2 and 14 of the same connector. Connect the DVM leads and verify that the TTL Threshold of +1.400V +/- 25mV is present. If the DVM reads ECL Threshold instead of TTL Threshold, this indicates a short is present between Data Input and Clock Input lines.

f. Install the resistor between pin 2 (ground) and 15 (Data Threshold) of SECTION C lower input connector. Connect the DVM leads and verify ECL Threshold of ~~+1.400V~~ -1.300V +/- 25mV is present. If the DVM reads ECL instead of TTL, this indicates a short is present between High and Low Data Input lines.

g. Repeat substep e for this connector.

h. Repeat substeps d through f for SECTION B and SECTION A.

ECL Threshold Adjustment

The ECL Threshold adjustment is performed for each front panel input connector as follows:

1. Install the 4.7K-Ohm resistor at sockets 2 and 14 of SECTION A input connector (bits 7-0). Connect the DVM positive (+) lead to socket 2 and the DVM negative(-) lead to socket 14 so that the measurement is taken across the resistor.

2. Make the following keyboard entries to change all thresholds from TTL to ECL:

   a. Press the FORMAT key to access the Format screen.

   b. Press the F1 FUNCTION key, to move the cursor to the Top Threshold location.

   c. Press and hold quick Key 1 until ECL is selected for all threshold voltages.

   d. Press the ARM key to change DVM reading to ECL level. Select ECL levels for all inputs.

3. Adjust the ECL THRESHOLD (R7) for DVM reading of +1.300 +/- 25mV.

4. Relocate the resistor to SECTION A (bits F-8) input connector and verify the ECL Threshold of +1.300 +/- 5mV is present.

5. Check the ECL level of other inputs by moving the load resistor to input connectors at SECTION B and SECTION C. Verify the ECL Threshold of +1.300 +/- 5mV is present at sockets 2 and 14 of each low byte (bits 7-0) and high byte (bits F-8) input connector.

Variable A Threshold Adjustment

The Variable A Threshold adjustment is performed for each front panel input connector as follows:

1. Install the 4.7K-Ohm resistor at sockets 2 and 14 of the SECTION A Input connector (bits 7-0). Connect the DVM positive (+) lead to socket 2. Connect the DVM negative (-) lead to socket 14 so the measurement is taken across the resistor. See Figure 3-8.

2. Make the following keyboard entries:

   a. Press the FORMAT key to access the Format screen.

   b. Press the FUNCTION key, F1, to move cursor to the top threshold location.

   c. Press and hold quick Key 2 until VARA is selected for all threshold voltages.

   d. Press the ARM key to change DVM reading to VARA level. All inputs should read VARA = 9.99V.

3. Adjust the VARA GAIN (R6) for DVM reading of 9.990 +/- 5mV.

4. Make the following keyboard entries:

   a. Press the FIELD right-arrow key to move the cursor to 9.99.

   b. Press and hold Quick Key 0 until 9.99 inputs are set at 0.00

   c. Press the ARM key. All inputs should read VARA = 0.00V.

5. Adjust the VARA OFFSET (R9) for DVM reading of 0.000 +/- 5mV.

6. Make the following keyboard entries:

   a. Press and hold Quick Key 9 until 0.00 inputs are set at 9.99.

   b. Press the ARM key.

7. Adjust the VARA GAIN (R6) for DVM reading of +9.990 +/- 5mV.

8. Make the following keyboard entries:

   a. Press the FIELD left-arrow key to move cursor to the + position.

   b. Press the NEXT key to change positive (+) to negative (-) value.

   c. Press the ARM key.

9. Read the DVM and adjust the VARA GAIN (R6) for -9.990V + 1/2 the difference of actual reading and -9.990V. (For example, if the actual DVM reading is -9.98V, subtract this value from -9.990V. The difference of -0.01V is divided by 2 to obtain -0.005V and R6 would be adjusted for -9.995V.)

10. Repeat steps 6 through 9 until the offset is the same for both positive and negative voltages +/- 30mV.

Variable B Threshold Adjustment

The Variable B Threshold adjustment is performed for each front panel input connector. The procedures are the same as steps 1 through 10 for the Variable A adjustment, except as follows:

1. Install the 4.7K-Ohm resistor at SECTION A input connector as described in Variable A Threshold adjustment procedure.

2. Make the following keyboard entries:

   a. Press the FORMAT key to access the Format screen.

   b. Press the F1 FUNCTION key, to move the cursor to top of threshold.

   c. Press and hold quick Key 3 until VARB is selected for all threshold voltages.

   d. Press the ARM key to change the DVM reading to the VARB level. All inputs should read VARB = 9.99.

3. Adjust the VARB GAIN (R1) for a DVM reading of 9.990 +/- 5mV.

4. Make the following keyboard entries:

   a. Press the FIELD right-arrow key twice to move the cursor to position 9.99.

   b. Press and hold quick Key 0 until 9.99 inputs are set at 0.00.

   c. Press the ARM key. All inputs should read VARB = +0.00V.

5. Adjust the VARB OFFSET (R2) for a DVM reading of 0.000 +/- 5mV.

6. Make the following keyboard entries:

   a. Press and hold Quick Key 9 until 0.00 inputs are set at 9.99.

   b. Press the ARM key.

7. Adjust the VARB GAIN (R1) for a DVM reading of +9.990 +/- 5mV.

8. Make the following keyboard entries:

   a. Press the FIELD left-arrow key to move the cursor left to the (+) position.

   b. Press the NEXT key to change from a positive (+) to a negative (-) value.

   c. Press the ARM key.

9. Note the value of the DVM reading and adjust the VARB GAIN (R1) for - 9.990V + 1/2 the difference of actual reading and -9.990V.

10. Repeat steps 6 through 9 until the offset is the same for both positive and negative voltages, +/- 30mV.

DVM Circuit Adjustment

The user must provide an external voltage source of +20.000 +/- 3mV dc that is used to calibrate the K450 Digital Voltmeter (DVM) circuit. The adjustment controls for DVM GAIN (R5) and DVM OFFSET (R3) are located on the Threshold/GPIB/RS-232 Board shown in Figure 3-7.

The Configuration screen provides a DVM readout for making the adjustments. Note that any display screen reads the DVM voltage except those displays for Memory A or B.

Use the following procedure to calibrate the DVM circuit:

1. Turn the power on and verify if the unit passes the power-up diagnostic test.

2. Connect the DVM POS (+) lead to external dc voltage source positive output. Connect the DVM NEG (-) lead to an external dc negative output.

3. Set the external dc voltage source for a DVM reading of +20.000 +/- 3mV.

4. Connect the positive lead of an external voltage source to the POS DVM INPUT jack located on the K450 front panel. Connect the negative lead of an external voltage source to the NEG DVM INPUT jack on K450 front panel.

5. Check the voltage indication at the external voltage source to verify if the adjusted value of +20.000 +/- 3mV is still present. Readjust the voltage if necessary.

6. Watch the DVM value on the screen. Adjust the DVM GAIN (R5) for a DVM value of +20.00V.

7. Set the external DC voltage source to indicate 0.000 +/- 3mV and watch the DVM value on the screen.

8. Adjust the DVM OFFSET (R3) for a DVM value of 0.00V.

9. Set the external dc voltage source to -20.00V +/- 3mV. Watch the DVM value on the screen.

10. Verify if the DVM value is -20.00V. Adjust the DVM GAIN (R5) to get this reading.

11. Repeat steps 3 through 10 until the DVM values of +/- 20.00V and 0.00V are +/- 3mV.

INTERNAL CLOCK ADJUSTMENT

This adjustment is performed on the Clock Board. This board selects internal and external clocks, and enable circuits.

The following tools and test equipment are required to make the clock adjustments:

- o Frequency Counter: Capable of 0.01% accuracy on ECL at 100 MHz
- o Oscilloscope: 350 MHz Band Width, Horizontal Resolution to 1 ns/Div
- o Extender Board: Gould Part Number 0117-0195-01

Adjustment is as follows:

1. Turn the power off and remove the Clock Board from the card cage. Install on the Extender Board.
2. Connect six cables and probes to front panel connectors at SECTION A, B, and C.
3. Turn the power on and verify the power up diagnostic test by seeing the Configuration screen.
4. Set the oscilloscope to .05V/div. Use a Tektronix P6106 X10, 1 megohm probe. Set the time base to 2 ns/div. Set the trace base line at +1.30 V above the center line so that the ECL threshold (- 1.30V) is at the center line of the screen.
5. Connect the oscilloscope probe tip input to pin 12 (output) on the 100102 IC device at board location 12C. Connect the probe ground lead to the ground lug at board location 11B. See Figure 3-9 for clock board component locations.
6. Adjust pot R19 for approximately 50% duty cycle, symmetrical about the ECL threshold.
7. While probing IC 12C, pin 12, adjust trimmer cap C8 for maximum peak-to-peak amplitude.
8. Re-adjust symmetry pot R19 for a 50% +/- 2% duty cycle about the ECL threshold. Monitor IC 12C pin 12 or 13 with an oscilloscope. Verify that the rising and falling edges are sharp, not fuzzy.
9. Connect a frequency counter (use non-metalic adjustment tool) with a 1 megaohm input to IC 12C, pin 12 or 13. Verify for a frequency of 100 MHz +/- .1% (99.9 MHz to 100.1 MHz).
10. Turn off the unit.
11. Turn on the unit and should see a frequency of 100 MHz on the scope. If the frequency is not stable, repeat steps 1 through 11.
12. Turn off the unit and remove the clock board from the extender board. Install the clock board inside the K450 chassis. Turn on the unit.

13. Check for the proper frequency and duty cycle (symmetry) at IC 12C, pin 13. Re-adjust if necessary. Use the scope probe tip with insulated ground. Use the same ground lug location with short ground lead attached.

14. Turn the unit on and off. Re-check the frequency.

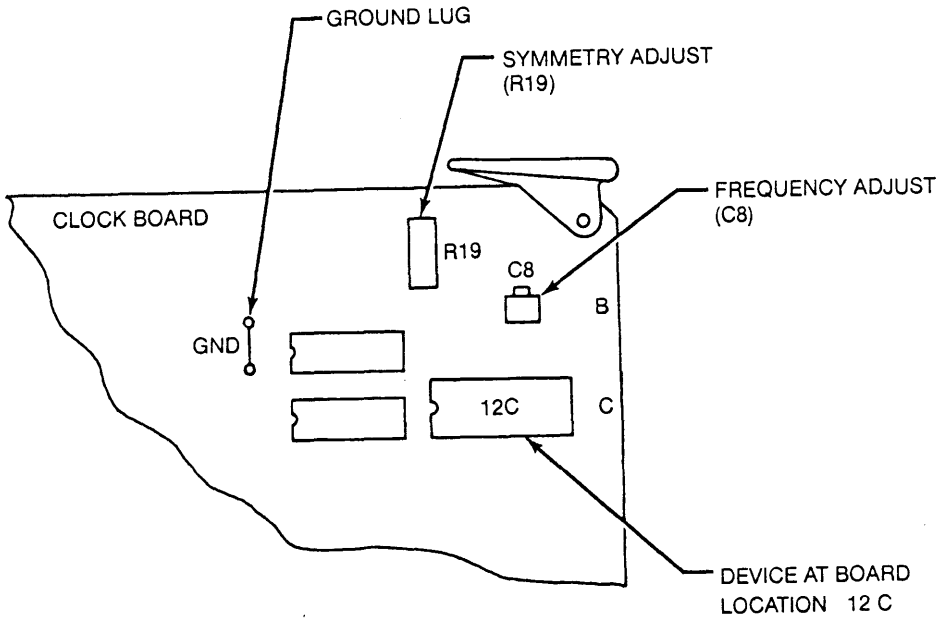


Figure 3-9. Clock Board Internal Clock Adjustment

Chapter 4

THEORY OF OPERATION

GENERAL

This chapter describes the theory of operation for the K450 Logic Analyzer. An overview of the operation is presented to show the relationship of the various circuit functions. The overview is followed by a description of internal circuit functions for each printed circuit board. These descriptions are referenced to specific board components and circuit functions found in chapter 7. A block diagram is provided to support these descriptions. Theory of operation is provided for the following printed circuit boards:

- Data Display Board
- MPU Board
- Threshold/GPIB/RS-232 Board
- Clock Board
- Data Board
- Control Board

OVERVIEW OF K450 UNIT OPERATION

The block diagram of Figure 4-1 presents the overall K450 system data flow and control operations. This diagram also shows the K450 system architecture and interaction of board circuit functions.

MPU Board Interaction

The K450 Logic Analyzer employs a 16-bit, 8086 microprocessor for controlling system operations. The 8086 CPU is located on the Master Processor Unit (MPU) board. The MPU Board addresses all other boards in the system as I/O devices. The MPU Board communicates with the circuit boards through the multiplexed address/data bus interface on the motherboard. The operating system uses up to 256K bytes of ROM and 512K bytes of RAM on the MPU board.

The K450 operating system and power-up diagnostic routines are firmware stored in the ten EPROM chips located on the MPU board. This firmware executes the K450 operations that perform digital circuit analysis and processing of external data and clock signals supplied by the user's equipment.

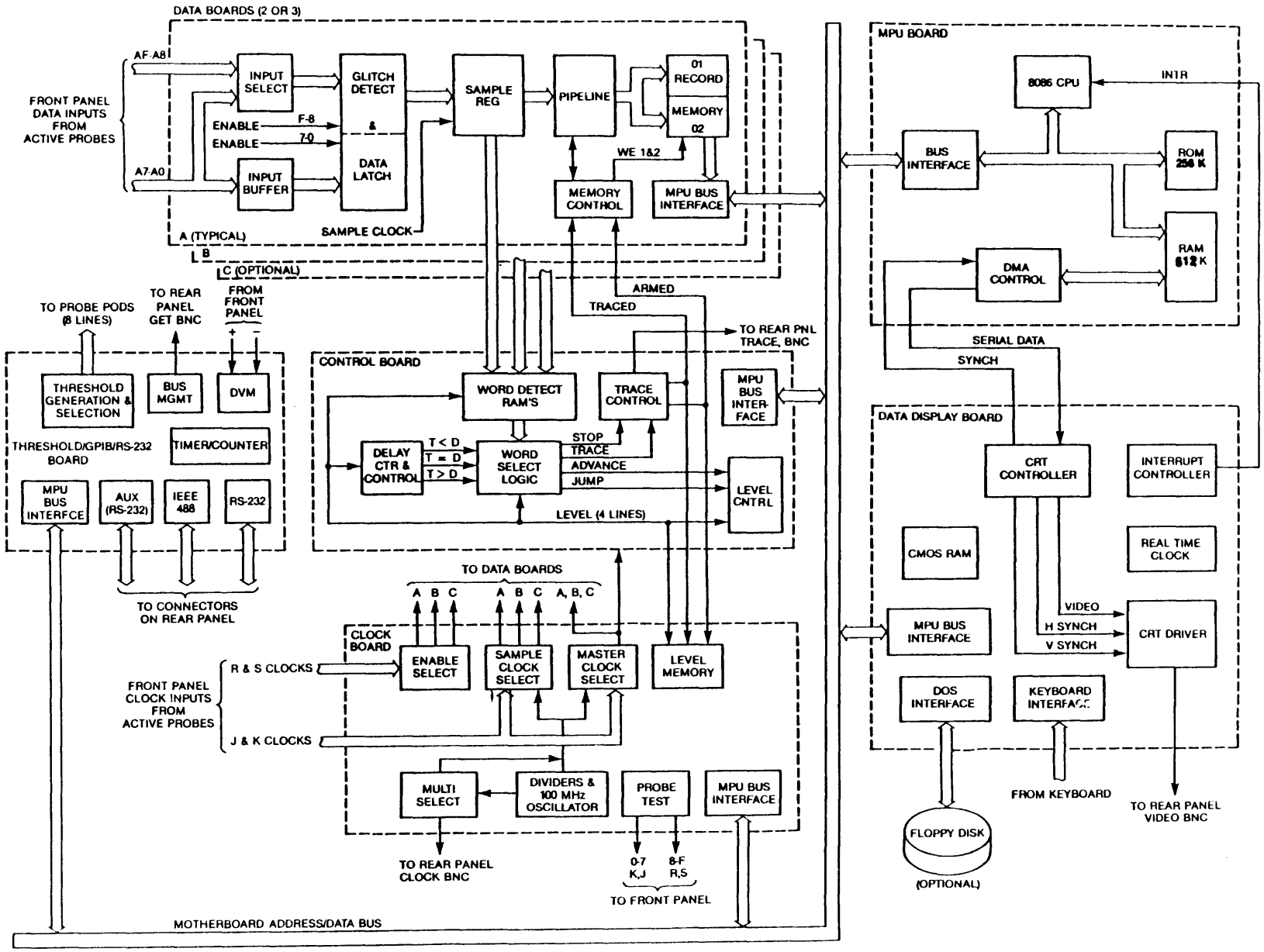


Figure 4-1. K450 System Block Diagram

Information collected and analyzed by the system is recorded in main memory. The results are selectively accessed by the user and displayed on demand. The MPU Board provides the control functions for display, display setups, memory transfer, memory control, memory compares and keyboard input.

Data Board Interaction

The external data and clock input signals collected by the probes are supplied to the input panel. The data input signals (7-0 and F-8) are directed to the Data Board. The clock input signals (J & K and R & S) are sent to the Clock Board. The Data Board functions have circuits that buffer the input data signals, select high/low bytes and detect glitches. These functions define the sample content through pipeline control circuits to main memory and word detection RAM on the Control Board. Control signals from MPU holding registers select the data source that is passed through the sampling circuitry. Input signals from the Control Board initiate the ARMED and TRACED condition so that the sample is recorded in Memory.

Clock Board Interaction

The Clock Board combines and selects clock signals to generate Latch, Sample and Master clocks. The J & K clock inputs and R & S latch inputs are combined in user defined AND/OR Boolean expressions. The internal clock is generated on this board. It is always available at the CLOCK output BNC connector on the rear panel.

The 100MHz internal clock is also generated on this board. The user selected clocks and combined clocks are routed to the Data Boards and the trace Control Board. The PROBE TEST output signal at the front panel connector is generated by the pattern generator on the Clock Board.

Control Board Interaction

The Control Board contains decision making logic for control of the trace and recording process. This includes word recognition circuits that detect the sample data supplied from the Data Boards. Delay counter logic combines delay conditions with detected words to set up sequencing for Stop Recording, Jump or advance to another recording level with different parameters. Delay counter logic also enables or disables input sample data recordings. The trace control logic resolves these conditions to initiate the ARMED and TRACE signals. These signals are sent to the Data Board to enable recording of the traced information. The Control Board also generates the TRACE output signal supplied to the BNC connector on the back panel.

Threshold/GPIB/RS-232 Board Interaction

The Threshold/GPIB/RS-232 Board generates two variable, and two fixed threshold voltage sources that are supplied to the probes. The variable voltages are VAR A and VAR B. The fixed voltages are TTL and ECL. Threshold control circuits enable each probe to select one of these voltage sources. The VAR A and VAR B threshold levels are driven by software-controlled, digital-to-analog converter (Dac) circuits. A comparator circuit performs the analog-to -digital conversion (ADC) that is used by the power-up diagnostic to measure power supply voltage levels.

The TTL and ECL Threshold sources use a voltage divider network and +/- 10V reference voltage for generating the fixed levels. Both the RS-232 and AUX serial communication links are driven by a Universal Synchronous/Asynchronous Receiver/Transmit (USART) chip. The GPIB (IEEE-488) parallel interface for Talker/Listen modes transfer data under control of an Interrupt line. The GPIB control circuits generate the interrupt signal supplied to the Data Display Board. The GPIB control circuits generate the GET (Group Execute Trigger) output signal supplied to the BNC connector on the rear panel. The DVM input supplied from the front panel is buffered to the Threshold/GPIB/RS-232 Board where the analog-to-digital conversion takes place.

Data Display Board Interaction

The Data Display Board presents a display pattern that is derived by the MPU processing and stored in the RAM as a complete dot map. Each dot location of the CRT is represented by a bit in the RAM (where 1 = white, 0 = black). Each dot is supplied to video control circuits on the Data Display Board. The video control circuits accept CRT address clocking information and serial input data supplied by the MPU. The circuits generates the video control signals that drive the horizontal, vertical, and synchronization for the CRT. The CRT controller circuits continuously interact with processor circuits to generate direct memory access cycles from the RAM. This data is translated to the CRT. A 16-bit word is read from the RAM every 2 us and converted into a string of 16 dots on the CRT. The Data Display Board also accepts interrupt signals generated by other board circuits. The interrupt signals are used by the Data Display Board interrupt processor to send an interrupt to the MPU.

The Data Display Board provides the Keyboard interface and DOS interface. The Real Time Clock and CMOS Memory Save circuits are backed up by battery power. These batteries drive the circuits when facility power is interrupted or removed from the K450 unit. The Audio Error Alarm circuit is also contained on the Data Display Board.

DATA DISPLAY BOARD OPERATIONS

Overview

This section describes Theory of Operation for the K450 Data Display Board assembly, Part Number 0114-2010-60 or 0114-3010-60. The board assembly drawing, schematic diagrams and list of material are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions of circuit functions. The Data Display Board block diagram is shown in Figure 4-2. The following board circuit functions are described:

- CRT Controller (Schematic sheets 1, 2 and 3)
- Interrupt Processor (Schematic Sheet 4)
- Keyboard and Front Panel Interface Circuit (Schematic Sheet 4)
- CMOS RAM Save Circuit (Schematic Sheet 5)
- Audio Error Alarm Circuit (Schematic Sheet 4)
- Real Time Clock (Schematic Sheet 6)
- DOS Interface Circuit (Schematic Sheet 6)

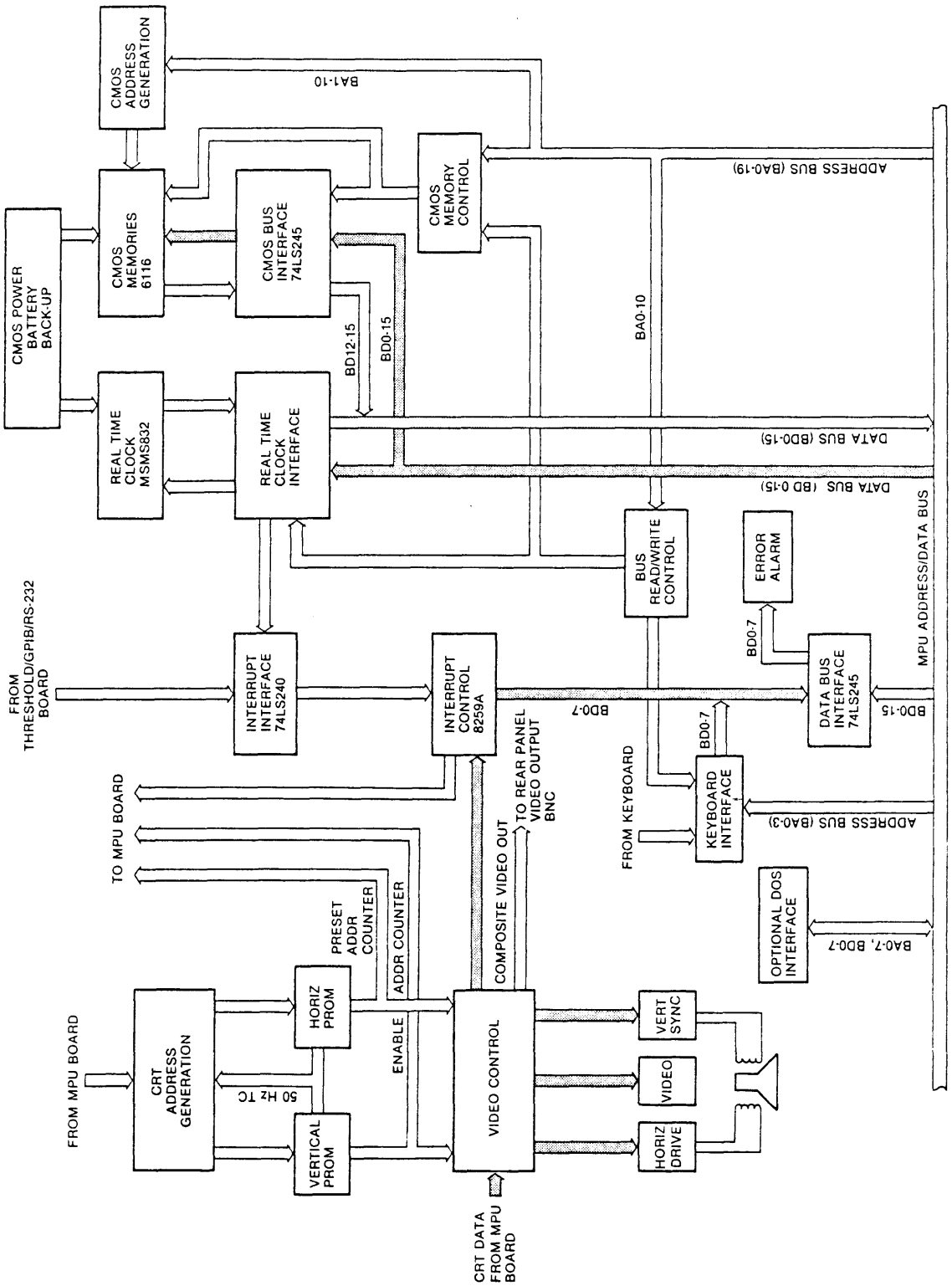


Figure 4-2. K450 Data Display Board Block Diagram

CRT Controller

The CRT Controller circuit (sheet 3 of schematic diagrams) generates a standard raster scan display format with data presented as a series of horizontally scanned lines. Each line starts at the left of the screen and goes to the right. The first line is at the top of the screen and the last is at the bottom. Standard sync and blanking signals are generated. The K450 operate at a 50Hz scan rate at all times.

Horizontal Timing: Each horizontal scan line is 64 usec long. Each scan line has 52 usec of video with 12 usec blanked and a 6-usec sync pulse during the blank time. The LS161 Horizontal Counter at location 9A and 10A runs continuously at a 500 KHz rate generating the five address lines for the horizontal ROM at 10B. The Horizontal ROM decodes the address to produce the blanking, sync and top count (end-of-line) pulses (74LS175 location 9B). The horizontal blanking interval occurs for the first 12 usec after the counter rolls over, states 0 through 5 (pin 7 of 9B). The sync pulse at pin 3 of 9B starts 2 usec after the blanking and lasts for 6 usec. In addition to addressing the ROM, the fifth address line is used by the horizontal drive for the deflection (pin 10, location 10C).

Vertical Timing: The vertical timing cycle begins with counters preset to 7200 Hex. The horizontal and vertical PROMs decode top count after counting 290 lines, and reset the counter to 7200 Hex. Simultaneously with the vertical top count, the vertical PROM generates the PRESET ADDRESS COUNTER signal which synchronizes the tracking address counter on the MPU board. The The vertical sync pulse is decoded to occur at line 35 Hex.

Horizontal Deflection and High Voltage: The horizontal drive signal from the CRT controller synchronizes the horizontal scanning with the retrace blanking by controlling the horizontal drive transistor, Q5 (sheet 1 of schematic diagrams). The horizontal drive transistor (Q5) provides energy to the flyback transformer and it draws current from the horizontal deflection coil to generate the scan from left to right. The Flyback Transformer (T2), provides the energy for rapid retrace from right to left. It serves as an ac to dc converter for generating the operating voltages for the CRT. The following voltages are supplied to the CRT:

+10KV	CRT Anode
+200V	Focus
+30V	Cathode
-40V	CRT Grid

The horizontal deflection and high voltage circuit allows adjustment of the Focus (R29) and Brightness (R32) which are located near the top of the board. The Horizontal Width adjustment (L1) and Linearity adjustment (L2) are also present.

Vertical Deflection: The vertical processor (sheet 2 of schematic diagrams) generates and synchronizes the vertical scanning. The vertical processor drives the vertical deflection coil directly, and senses current through the coil through a sense resistor.

The TDA 1270 processor (11B) contains an oscillator that is synchronized to the vertical sync pulse, an adjustable constant current source ramp generator, an emitter follower, and a power amplifier to drive the coil. The vertical processor circuitry allows adjustment of Vertical Hold (R21) Vertical Height (R20) and Vertical Linearity (R47).

Video: The CRT brightness is controlled by combining the digital data with the horizontal and vertical blanking signals and switching the cathode voltage between zero volts (white) and +30V (black). The video is modulated by an 8MHz clock signal to provide a sharper display presentation. A composite video signal is also generated at the rear panel BNC connector for use with another video monitor.

Video Operation: Transistor Q3 operates as the video amplifier and applies the video signal to the cathode of the CRT. R28 is the load resistor connecting Q3 to the 30 Vdc supply. The 30 Vdc supply is composed of CR6 and C38. The -40 Vdc grid bias supply for the CRT consists of CR3 and C35. CR4 and C37 comprise the 200 Vdc focus electrode supply.

The source voltage for these supplies is the high-voltage transformer, T2. Note also that T2 supplies the 10 KV for the second-anode of the CRT. The rectifier for the high-voltage is an integral part of the second-anode lead. The filter capacitor for the high-voltage is the 600pF capacitance of the CRT aquedag coatings.

Transformer T1 and transistors Q4 and Q5 drive transformer T2. When Q5 is conducting, energy is stored in the primary of T2. When Q5 is switched off, the energy stored in the T2 primary is transferred to the secondary.

When Q5 switches off, the voltage at its collector rises to approximately 120 Vdc and is impressed upon the horizontal deflection coil through L1 and L2. This voltage causes a current to flow in the deflection coil, which in turn causes the electron to deflect to the left side of the CRT. The positive current flow decays in a linear manner, being zero at center screen. Because of the resonant circuit, C53 and the deflection coil, the current increases in the negative direction for the right side of the screen. At center screen Q5 again switches on and remains on until the beam is deflected to the right side of the screen. At this time, Q5 again switches off, and the process begins again.

Vertical deflection is accomplished using a TDA1270 IC, U11B. This IC contains an oscillator, a preamp and a power amp. The oscillator frequency is controlled by R21, R22 and C49. The waveform is shaped by R20, R37, R42, R44, R47, C45 and C46. The waveform is amplified by the preamp and power amplifier and impressed upon the vertical deflection coil through C51. The current is sensed across R45 and returned to the preamp through feedback resistor R46.

Interrupt Processor

The Interrupt Processor circuit (sheet 4 of schematic diagrams) accommodates up to eight levels of interrupts (INT0 - INT7) using a 8259A Interrupt Processor chip (2E).

Seven levels of interrupts are used with the following assignments:

INTERRUPT LEVEL	ASSIGNMENT
INT7	Floppy Disk Controller
INT6	1 Second (Time of Day Clock)
INT5	(Not used)
INT4	Timer #0
INT3	Auxiliary, RS-232 (USART#2)(RXRDY+TXRDY)
INT2	RS-232 (USART #1) (RXRDY+TXRDY)
INT1	GPIB
INT0	50Hz (CRT Interrupt)

Keyboard and Front Panel Interface Circuit

The Keyboard and Front Panel Interface (sheet 4 of schematic diagrams) are addressed simultaneously by the microprocessor. The interface circuit decodes eight addresses out of the I/O map. Each row is read as a byte at a 50Hz rate. Any key contact that is closed is stored as a zero within the selected byte. Each bit of the byte corresponds to a column on the keyboard.

CMOS RAM Save Circuit

The CMOS RAM Save circuit (sheet 5 of schematic diagrams) provides 2K x 16 memory storage. If the K450 unit is powered down, the save circuit stores the last parameters displayed on the screen. A 2.9V battery (location B1) provides power to the two 6116 CMOS RAMs and the Real Time Clock when the unit is powered down. Data to and from the 6116 RAMs is transferred over a bi-directional data bus through the two 74LS245 Three-State Transceivers at locations 3C and 4C.

Real Time Clock

The Real Time Clock circuit (sheet 6 of schematic diagrams) is controlled by the MSM5832 IC module (location 2D) which drives the real time clock. A 32.768 KHz crystal (location Y1) is used to generate the clock frequency. The variable capacitor (C10) provides for adjustment of the frequency. The adjustment of C10 is set by the factory and is not available to the user. The clock is set by the software through the Date and Time Set-up display.

Audio Error Alarm Circuit

The Audio Error Alarm circuit (sheet 4 of schematic diagram) produces a low level beep tone when improper keyboard entries are made. The tone volume is controlled by R56. Enabling and disabling the tone is controlled by software selection through the Date and Time setup display.

DOS Interface Circuit

The optional DOS Assembly contains the Floppy Disk Controller board which communicates with the K450 through a signal cable link. The connector P4 on the Data Display Board (sheet 6 of schematic diagrams) provides the I/O link for the DOS Assembly. Information for Address (BA0-BA7) and Data (BD0-BD7) is supplied from P4 to the MPU Address/Data Bus on the motherboard through the P15 and P16 edge connectors. The Interrupt control (INTR 7) signal is supplied to the 8259A Interrupt Processor (location 2E, sheet 4 of schematic diagram) where it is then directed to the MPU through the control bus.

MPU BOARD OPERATIONS

Overview

This section describes theory of operation for the K450 MPU Board, Part Number 0117-0540-10. The circuits on the MPU Board consist of an 8086 microprocessor, address registers, data transceivers, random access memory (RAM), read only memory (ROM), memory controller and I/O decoder. This board provides control functions for display, display setups, memory transfer, memory functions, memory compares and keyboard.

The MPU Board block diagram is shown in Figure 4-3. The associated assembly drawing, schematic diagrams and list of materials are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Microprocessor (schematic sheet 2)
- Address Registers (schematic sheets 3 and 4)
- Memory (schematic sheets 3, 4 and 7)
- Memory Controller (schematic sheet 5)
- I/O Decoding (schematic sheet 6)

Microprocessor

The 8086 microprocessor (schematic sheet 2, location 10J) is used on the MPU Board to operate at a 4 MHz clock rate in the minimum mode configuration. The 8086 microprocessor outputs a 20-bit memory address. Data is accessed as 16-bit words, subdivided into a low-order byte and a high-order byte. The low-order 16 address bus lines (AD0 to AD15) are multiplexed with the 16-bit data bus. The Byte High Enable signal (BHE) is used to identify the high-order byte, while A0 identifies the low-order byte.

Initialization is accomplished with activation (HIGH) of the MPU RESET pin (location 8B) for more than four clock cycles. The 8086 microprocessor terminates operations on the high-going edge of the MPU RESET and remains dormant as long as MPU RESET is HIGH. The low-going edge of MPU RESET triggers an internal reset sequence of approximately 10 clock cycles, during which time no other operations should occur.

Non-maskable interrupt request (NMI) is initiated when external logic inputs a low-to-high transition at the NMI pin by power-up signal (PUP) at locations 11H and 11B.

A non-maskable interrupt has higher priority than the maskable interrupt. A maskable interrupt is generated when external logic inputs a HIGH level at the INTR pin. The 8086 CPU responds by generating INTA for the interrupt acknowledge cycle.

HOLD and HLDA are standard hold request/acknowledge signals. When external logic inputs HOLD high, the 8086 microprocessor enters a hold state upon completing the current instruction's execution. The 8086 microprocessor acknowledges the hold state by outputting HLDA high. Location 11H is the buffer for the INTR, INTA, and HLDA signals.

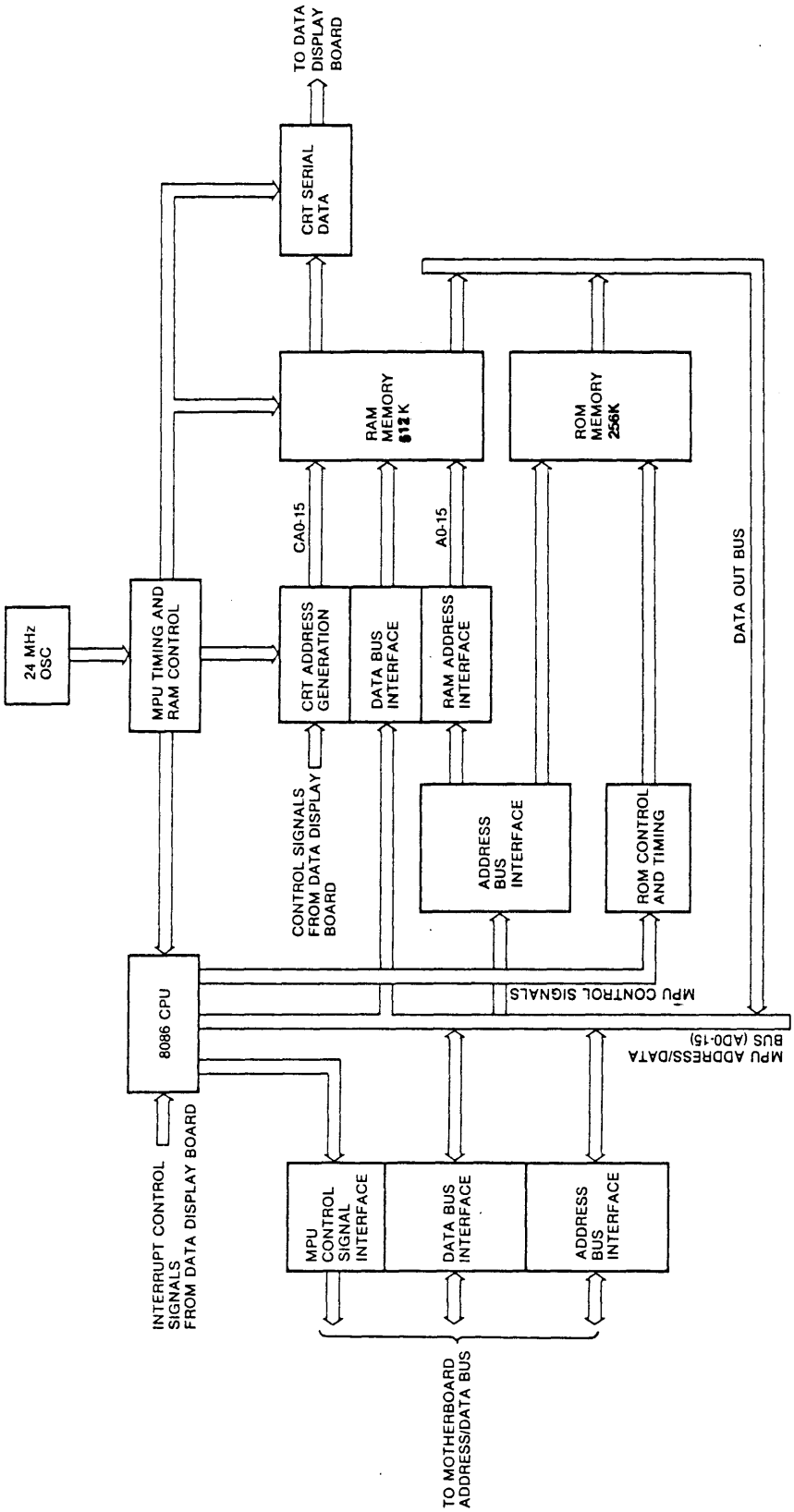


Figure 4-3. MPU Board Block Diagram

Address Registers and Data Transceivers

The 8086 microprocessor uses a multiplexed bus for address and data transfers (sheet 2 of schematic diagrams). The MPU Board demultiplexes the 8086 bus into two buses. One bus controls all information to the ROM and the RAM which is contained on locations 1A to 1E, 2A to 2E, 4A to 4H and 6A to 6H. The other bus interfaces with other boards in the K450. Locations 9H, 10H and 11J are buffers for 20 memory address lines (A0 to A19) and BHE. Locations 9K, 10K and 11K are buffers for 20 address lines and BHE to boards other than the MPU. The transceivers for the data lines are located at locations 7K and 8K. Locations 7J, 7H, 8J and 8H are wired for PROM's and buffers for temporary test only. The 8086 loads addresses into the address registers by using the Address Latch Enable signal (ALE) and then transmits (WR) the data to, or receives (RD) the data from, the address in the register.

Memory

The 8086 memory space is organized into 16 segments of 64K bytes of external memory space (sheets 2 and 5 of schematic diagrams). Segments C, D, E and F (Hex) are the 256K bytes of ROM which contains the operating software. Segment 0 - 7 (Hex) contain the 512K bytes of dynamic RAM.

The ROM segment (schematic sheet 7), locations 1A to 1E and 2A to 2E, uses sixteen 16K X 8 memories arranged into eight sections of 16K words each. Locations 3L and 3M (schematic sheet 6) are ROM chip select decoders. Data output is read from ROM through a buffer at location 3J for high-byte data and at location 3K for low byte data.

The RAM segment (schematic sheets 3 and 4), locations, 4A to 4H and 6A to 6H, is made up of sixteen 256K X 1 dynamic memories providing 256K words (512K bytes). Data is input into the RAM, through the buffer at location 4J for high-byte data and at location 6J for low-byte data through RAM WRITE DATA EN. Data output is read from RAM through the latch buffer at location 4K for high-byte data and at location 6K for low-byte data through MPU LATCH ENABLE and EN RAM READ. CRT Data is read out into buffer registers at locations 6L and 4L and then shifted out at an 8 MHz clock rate to the Data Display Board by shift registers at locations 6M and 4M.

Memory Controller

The memory timing and the clock for the 8086 microprocessor (sheet 5 of schematic diagrams) are derived from a 24 MHz oscillator (location Y1). Locations 10E, 10D, 12J, 12C, 11C, 11D, 11E and 12B are used to divide to an 8 MHz clock to the CRT and a 4 MHz clock to the 8086 clock pin. Locations 11E, 12E and 12F divide the 24 MHz clock into timing signals used to generate Row Address Strobe (RAS) at locations 10C and 8B. Additionally, column Address Strobe (CAS0 and CAS1) are also generated at locations 8A, 9A and 12D. Write Enable signals for high-byte and low-byte of both RAM segments are generated at locations 7A, 8A, 8B, 10A and 10B. Row Select, Column Select and Latch Enable for both the MPU and CRT are generated at locations 9A and 9B.

The CRT port of the memory requests a word from memory every 2 us (500 KHz). The CRT page select addresses are generated at locations 7C, 7D, 8C and 8E (sheet 6 of the schematics) by the 500 KHz clock rate from location 7B.

If the 8086 requests a memory cycle during the CRT cycle, the memory controller uses the READY line on the 8086 microprocessor to generate wait states until the CRT cycle is finished. The memory then completes the requested 8086 memory cycle. The CRT Read cycle of one word every 2 usec also provides sequential operation required for the RAM refreshing.

I/O Decoding

The MPU Board addresses other boards in the system as I/O. The PROM (schematic sheet 4) at location 10F is used to decode addresses A11 to A19. When I/O is addressed, M/IO goes LOW, causing the PROM's outputs to be HIGH. The conditions in which S.A EN is normally HIGH and DEN (Data Enable) becomes active and causes the EN OFFBOARD DATA signal at location 9C to go LOW, placing data on the bus. Read commands for RAM, ROM and S.A are generated by RD, RAM ADRS, ROM ADRS and S.A at locations 9D and 9E. Control signals RD, WR, DEN, DT/R and M/IO are also buffered out to other boards through buffers at location 9G.

THRESHOLD/GPIB/RS-232 BOARD OPERATIONS

Overview

This section describes the theory of operation for the Threshold/GPIB/RS-232 Board assembly, Part Number 0114-0170-30. The circuits on this board generate threshold voltage levels, convert analog voltages to digital equivalents, control the GPIB Talker/Listener interface, control the RS-232 Interface and process digital readout of external voltage input.

The Threshold/GPIB/RS-232 Board block diagram is shown in Figure 4-4. The board assembly drawing, schematic diagrams and list-of-materials are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Threshold Circuit (Schematic Sheet 1)
- DVM Circuit (Schematic Sheet 2)
- GPIB Interface Circuit (Schematic Sheet 3)
- RS-232 Interface Circuit (Schematic Sheet 4)
- MPU Interface (Schematic Sheet 5)

Threshold Circuit

The Threshold Circuit (sheet 1 of schematic diagram) generates voltage sources, (VAR A, VAR B, TTL and ECL) that may be selected for each probe.

The VAR A and VAR B thresholds are defined by the four 74LS273 Flip-Flop holding registers. Locations 9B and 12B for VAR A, and locations 4B and 6D for VAR B. The holding registers buffer the MPU data bus to the two AD7533LN Digital-to-Analog Converters (Dac) at location 9A for VAR A and location 4A for VAR B. Separate calibration adjustments are provided for VAR A and VAR B Voltage levels. The VAR A Gain is adjusted by R6; Offset is adjusted by R9. The VAR B Gain is adjusted by R1. The Offset is adjusted by R2. Both Dacs have a resolution of 10 bits.

The TTL and ECL thresholds are generated by using a voltage divider network and +/- 10V reference voltage level. The calibration adjustment for TTL is R8, ECL is adjusted by R7. The +/- 10V reference adjustment is controlled by R44.

The threshold voltages are supplied as input to eight analog multiplexers (sheet 2 of schematic diagrams). The selection of a particular threshold voltage (VAR A, VAR B, TTL or ECL) used by each probe is accomplished by a set of eight analog multiplexers and eight buffer amplifiers. Six of the multiplexers, at locations 1A, 1D, 1B, 1C, 2A and 2D are tied to high and low data bytes at input sections A, B and C. Two of the multiplexers are tied to R & S latch clocks (location 2B) and J & K sample clocks (location 2C). This allows the software to select one of the four voltages as the threshold. The outputs of the analog multiplexers are buffered by the operational amplifiers (locations 1E and 2E) which provide a gain of two that increases the range of the Dac output.

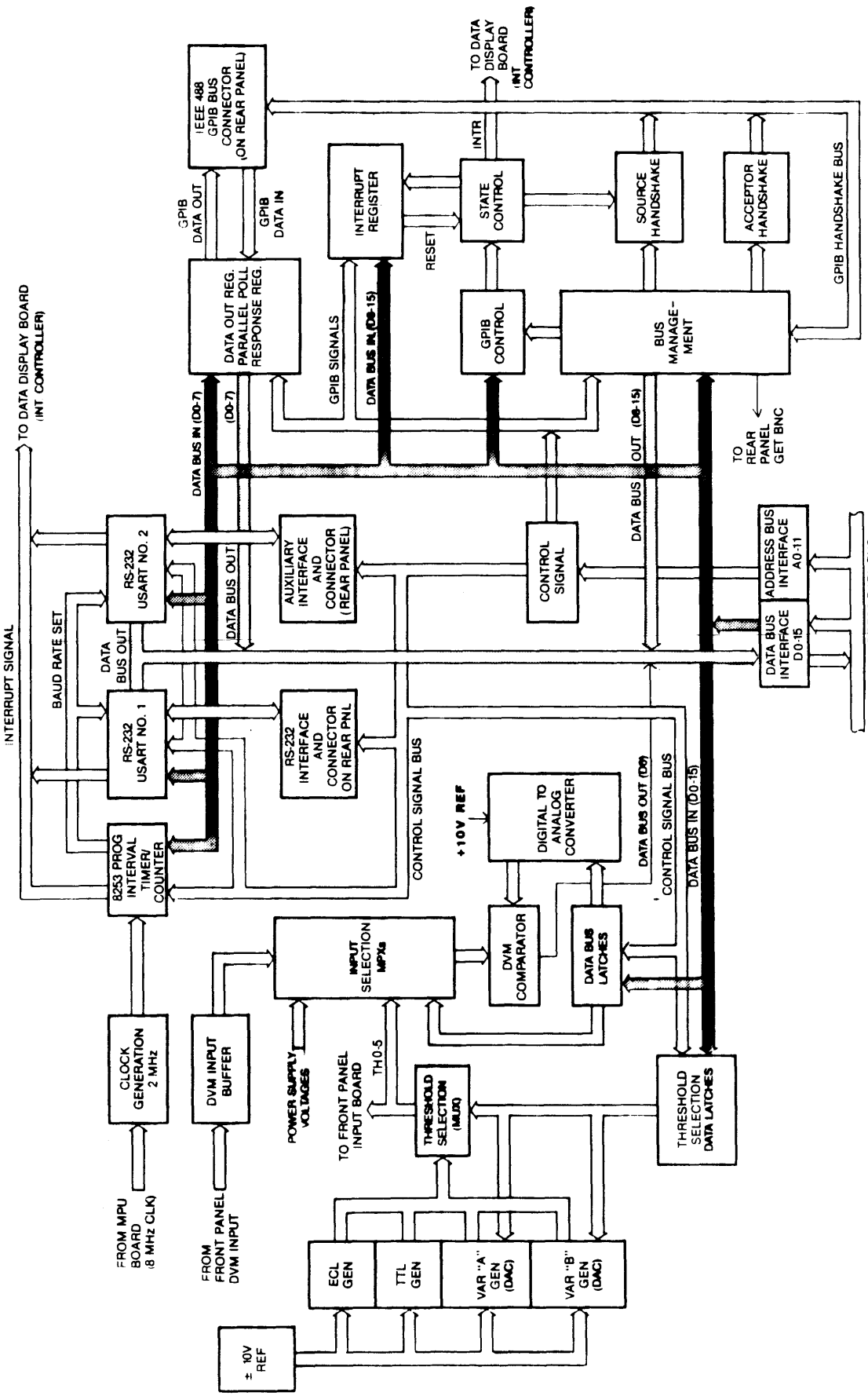


Figure 4-4. K450 Threshold/GPIB/RS-232 Board Block Diagram

One of the functions contained on the Threshold/GPIB/RS-232 Board is a software controlled Digital-to-Analog Converter and a comparator that performs Analog-to-Digital Conversions. This is used by the software to check the power supply and reference voltages during power up. Three multiplexers (sheet 2 of schematic diagrams) at locations 5F, 6F and 7F are used to select any one of the power supply voltages used in the K450. The selected voltage is then scanned by the software using the 12-bit Dac at location 8A. When the Dac value exceeds the voltage being tested, the comparator (location 7A) becomes switched. The MPU compares the resulting value with a table of voltages and their tolerances to determine the pass/fail condition of the test result.

DVM Circuit

The front panel DVM input signal (sheet 2 of schematic diagrams) is buffered onto the Threshold/GPIB/RS-232 Board by the operational amplifier at location 7A and is supplied to the multiplexer at 6F. The multiplexer selects the input voltage range that is supplied to the 12-bit Dac at location 8A and the comparator. The comparator (location 7A) generates the digital value that is used by the software to specify the DVM readout.

GPIB Interface Circuit

The GPIB Interface Circuit (sheet 3 of schematic diagram) is partitioned so that the handshake required to transmit individual bytes of information (for data or control) is performed by the hardware. All message generation or interpretation is done in the software. The GPIB address and mode for Talk Only, Talk/Listen and Listen Only, are determined by the interactive display for I/O setup. Once the Mode is determined, the GPIB control register is loaded with the specified mode information and the interrupt is enabled. All I/O data transfers occur under control of the interrupt line. With Listen mode selected, the receipt of a data byte or a command at the K450 will generate the interrupt. With Talker mode selected, the interrupt is generated when the byte has been accepted by the listener I/O device.

RS-232 Interface Circuit

The RS-232 Interface Circuit (sheet 4 of schematic diagram) causes information to be entered onto the Threshold/GPIB/RS-232 Board through two 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) at locations 12D and 12E. USART #1 interfaces with the K450 back panel RS-232 port. USART #2 interfaces with the AUX port. The Baud rate is set by the 8253B programmable interval timer/counter at location 8E. The internal timer uses a 2 MHz clock input derived from the CPU oscillator to measure the external master clock period. The bit rate clock output supplied to the USARTS is set at 16 times the actual rate at which data is being transmitted. Plus and minus 15-volt line drivers are used to send the signals to external devices.

MPU Interface

The MPU Interface circuit (sheet 5 of schematic diagram) buffers MPU data and address lines sent to the Threshold/GPIB/RS-232 Board through the motherboard interface. The MPU data bus (BD0-BD15) is buffered onto the board by two 74LS245 bus transceivers, locations 14F and 12F which control the two-way direction of data transfers to and from the MPU Address/Data Bus.

The buffered data bytes, D0-D7 and D8-DF are transferred to, and received from on board circuits for Threshold Selection Data Latch (schematic sheet 1), DVM Data Bus Latch (schematic sheet 2), Bus Management and GET BNC output connector (schematic sheet 3), Programmable Interval Timer and RS-232 USARTs (schematic sheet 4), and GPIB Parallel Poll Register and Interrupt Register (schematic sheet 3).

The MPU address bus (BA1-BA11) is buffered onto the board by the 74LS244 Buffer/Line Drivers at locations 10F and 11F (schematic sheet 5). The jumper connector for M/IO input signal supplied to line receiver at 11F must be connected across E13 and E14 to disable the memory mapped I/O and enable the I/O mapped I/O function. The 74LS244 buffers generate three state outputs that are supplied to five 74LS138, 1 of 8 decoders, locations 9D, 10B, 10D, 11B and 11D. These decoders accept three binary inputs and output one active-low control signal (from eight possibilities) for Write Hi Byte, Write Lo Byte, Read High Byte, Read Lo Byte. The control signals are supplied to on-board circuits that control the Threshold Selection Data Latch, DVM Data Bus Latch, Bus Management circuits and rear panel GET BNC output connector, Programmable Interval Timer and RS-232 USARTS and GPIB Parallel Poll Register.

CLOCK BOARD OPERATIONS

Overview

This section describes theory of operation for the K450 Clock Board assembly, Part Number 0121-0010-10. The circuits on this board provide all internal clock periods and programmable logic functions. These logic functions decode external clock inputs in accordance with the Master Clock, Sample Clock and Enable Boolean Expressions selected by the instrument operator. Also, circuits for the Level Memory, which store the level at which each sample was recorded, is located on the clock board.

The Clock Board block diagram is shown in Figure 4-5. The board assembly drawing, schematic diagrams and list-of-material are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Internal Clocks and Probe Test (Schematic Sheets 1 and 3)
- External Clocks (Schematic Sheets 2 and 3)
- AND Master Clocks (Schematic Sheet 3)
- OR Clock Selection (Schematic Sheet 3)
- Level Memory Circuit (Schematic Sheet 4)
- MPU Interface (Schematic Sheet 5)

Internal Clocks

All Internal Clocks (sheet 1 of schematic diagram) are derived from the 100 MHz oscillator circuit containing crystal Y1. The potentiometer, R19 allows adjustment of the average value of the 100 MHz signal on the emitter of Q2 so that symmetry of the clock output at location 12C, pin 12 can be set. The variable capacitor, C8 allows adjustment of oscillator frequency.

The two 10137 BCD counters, locations 9E and 10E are connected as decade dividers to provide the 10 MHz and 1 MHz decades. The 1 MHz output of 10E goes to Q1 which shifts the level, making it compatible with the input requirements of the counter at location 9C.

The two 14518 CMOS Dual BCD Counters at locations 9C and 9D operate between -5V and ground for compatibility with the ECL level. The outputs of all six decade dividers, are supplied to inputs of the eight-to-one, 10164 multiplexer at location 10C. The MPU can select any decade as the output of 10C. For clock frequencies greater than 10 MHz, the select lines to 10C, and the 10109 OR gate at location 10D, is set to all zeros by the MPU. This enables the 100102 OR gates at location 12C to output the 100 MHz (10nsec) clock. The selected decade feeds the input to the 10016 Programmable Binary Counter at location 11B.

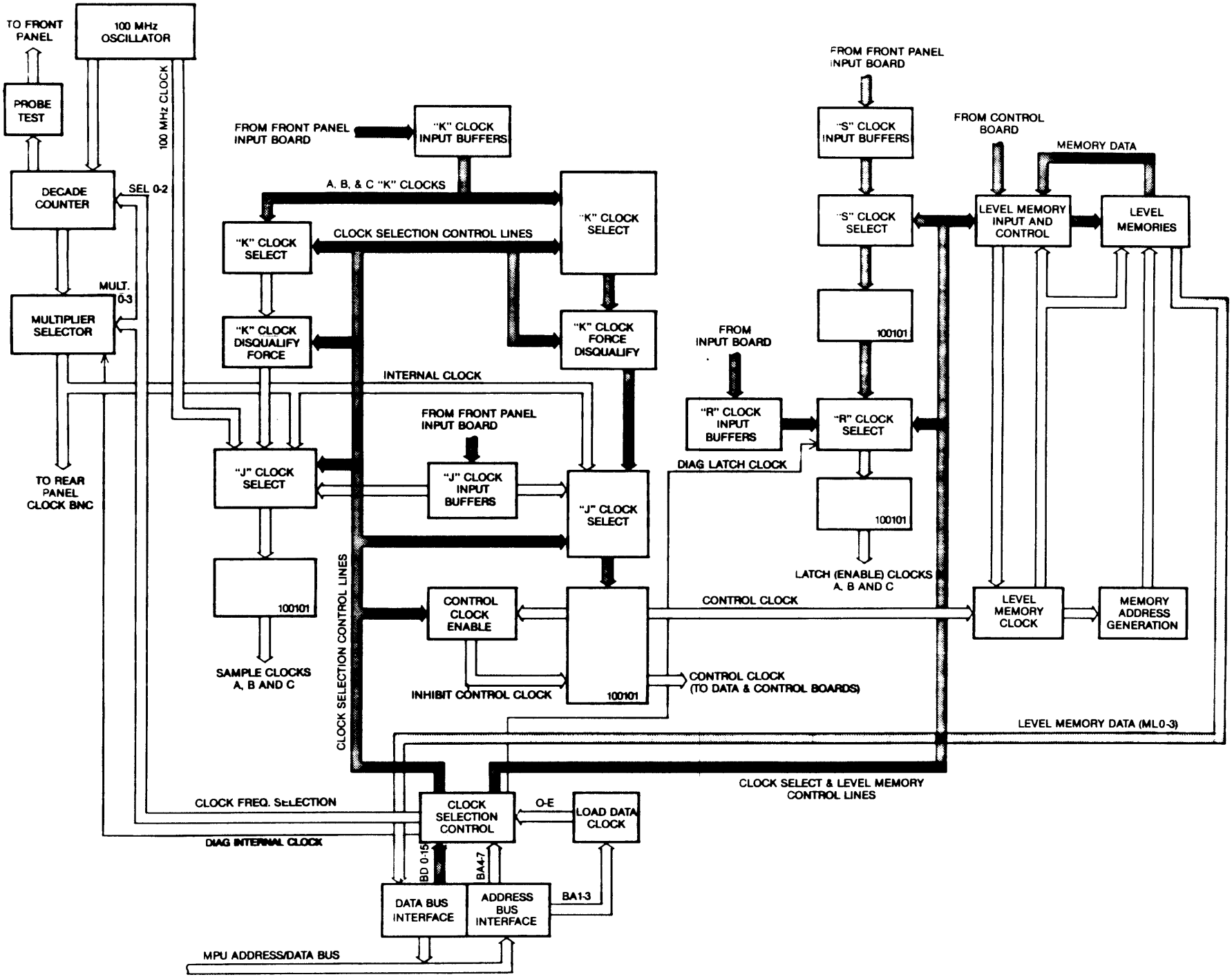


Figure 4-5. K450 Clock Board Block Diagram

The decade dividers with the programmable counter allows the selection of clock periods from 20 ns to 160 Ms in a 1 through 16 sequence. The software, however, limits the user capability to clock periods from 20 ns to 100 Ms in a 1 through 10 sequence. The BCD outputs of the 100 KHz decade counter also drives the select lines of the 4028 CMOS Demultiplexer at location 9B. The outputs of 9B provide a 1 of 8 pulse pattern to the front panel PROBE TEST connector as test data.

The 1 MHz clock and the least significant bit of BCD counter at location 9C are also supplied to the front panel PROBE TEST connector as test clocks. When an internal clock mode is selected, all external clocks are de-selected by the MPU (schematic sheet 3). The gate at location 3H, pin 21 is pulled low, enabling Internal clocks to pass through to the OR gate at location 4J, pin 9.

External Clocks

The External Clocks (sheets 2 and 3 of schematic diagram) consist of seven clock circuits as follows:

- Three Latch Enable Clocks (schematic sheet 2)
- Three Sample Clocks (schematic sheet 3)
- 1 Control (Master) Clock (schematic sheet 3)

Basically, all seven clock circuits are the same. Only the Control Clock selection, which is the most complex is described in subsequent paragraphs. The Control Clock selection gates have 13 inputs as follows:

- One Internal Clock
- Three $\overline{\text{AND}}$ Clocks ($\overline{\text{AJ}}$, $\overline{\text{BJ}}$ and $\overline{\text{CJ}}$)
- Three AND Clocks (AJ, BJ and CJ)
- Three OR Clocks (AK, BK and CK)
- Three $\overline{\text{OR}}$ Clocks ($\overline{\text{AK}}$, $\overline{\text{BK}}$ and $\overline{\text{CK}}$)

The major difference between Control Clock selection and the Latch Enable selection is the absence of Internal clocks for Latch Enable and the existence of Internal MPU Diagnostic Latch Enable.

AND Master Clocks Selection

The AND (Master) Clocks (sheet 3 of schematic diagram) are selected by the eight 100102 gates at locations 3H and 5H. Each of these gates has three inputs. Pin 19 is common to all gates and is driven by the output of the OR Clock selection gate at 4D. One pin of each of the 3H and 5H gates is driven by one of the J Clock inputs or their complements. The MPU controls the third input by placing a low on those gates whose J Clock input goes high when the selected clock is true. Only when all selected AND Clocks, or the OR Clock is true, will all of the outputs of 3H and 5H be low. This allows the control clock at location 4J, pin 9 to go high. Synchronous start-up of the control clock is provided by the 10H131 dual flip flops at location 5J. This prevents "sliver" clocks from being passed at the beginning of a record cycle.

OR Clock Selection

The OR Clocks (sheet 3 of schematic diagram) are selected by the five 100102 gates at location 5D and parts of the two gates at 4A and 4D. The MPU places a low on one input of each gate whose other input will be low when one of the selected OR Clocks is true. The OR clocks are the K Clock inputs.

Jumper selection for external clocks (schematic sheet 2, section A8) shows the jumper configuration table. With all jumpers positioned on the left two pins, the board is configured for all twelve clocks. With jumpers positioned on the right two pins, the C K Clock comes from the B S probe and the C J Clock from the B R probe.

NOTE: The software cannot read these jumpers, but counts the number of Data Boards in the system.

Level Memory Circuit

The Level Memory circuit (sheet 4 of schematic diagram) records which level of trace control is used for each word recorded on the Data Boards. Level data enters the clock board through the 20-pin header, J1.

The two 10176 registers at locations 11E and 11F and single 10173 register at location 11J operate as a pipeline which holds the level data temporarily while the decision is made to either record or not record the data. This decision is made on the Control Board which generates the Armed and Traced signals along with the level data that is sent to the pipeline. When the Traced signal is high, its complement is clocked into register 11F along with the level data. This action allows the OR gate, 12E to produce a write enable pulse on the next control clock transition. If the Traced signal is false, OR gate 12E is disabled and the level data in register 11F is written over at the next sample without being recorded. If the Armed signal goes false, the level memory becomes locked up.

The three 10016 address counters at locations 11G, 12J and 12H are used for the 10474 memories at locations 12F and 12G. The level memory is multiplexed in two ways. First through the 10H131 latch, pins 14 and 15 at location 11D which select the memory phase that is written to on each sample. Second through the 11D 10H131 latch at pin 3 which provides uniform 10nsec pulses when recording is in process regardless of the sample rate.

In read mode, the OR gate at location 12D, pin 3 is disabled thereby causing the output of latch 11D, pin 3 to become 1/2 the frequency of the input. When the Armed signal goes false, the pin D input goes true thereby stopping the pulse.

MPU Interface

The MPU Interface circuit (sheet 5 of schematic diagram) interfaces the Clock Board circuits to the motherboard through edge connector P2. The 74LS85 comparator at 12J decodes four address inputs A4 through A7 from the MPU to provide the My Address signal when the Clock Board is addressed. The My Address signal enables the five 10124 TTL-to-ECL level translators at locations 6J, 7J, 8J, 9K and 10K which buffer the MPU data bus content onto the Clock Board.

The 10161 de-multiplexer at location 9J decodes address lines A1, A2 and A3 along with the MPU BWR control signal to create load pulses for the 20 10176 holding registers at locations 7A through 7H, 8A through 8H, 9G and 9H, 10J and 10H.

The 10173 multiplexer latch at location 10G multiplexes 8 bits of read data into two 4-bit nibbles which are translated from ECL to TTL levels by the 10125 translator at location 10F. The 74368 tri-state buffer at location 9F is enabled by the BRD signal sent from the MPU and the My Address signal generated by the comparator at location 12L.

The clock Board is configured with eight jumpers located at the lower left corner of the board. These jumpers select clock signals for 32-input or 48-input capability as determined by the number of Data Boards installed in the unit. The jumpers are identically configured for 16 and 32 input systems. When the C Data Board is added to an existing 32-input unit to provide 48 inputs, it is necessary to rearrange the jumper connections to enable the SECTION C clock inputs. It is also necessary to route the BR, BS clocks into the user specified Latch Clock equation. The jumpers must be relocated from the eight center/lower-row pins to the center/upper-row pins.

NOTE: The K450 software will not recognize the SECTION C clock inputs unless these jumper connections are completed.

DATA BOARD OPERATIONS

Overview

This section describes theory of operation for the K450 Data Board assembly, part number 0121-0015-10. Each data board provides 16 inputs and one, two or three identical boards may be installed in the K450 unit to provide a 16, 32 or 48 data input configuration. The circuits on this board buffer input data signals supplied from the user's equipment, select operating modes, generate the pipeline processing functions, record traced information in main memory, decode the MPU address/data bus, and present status to the CPU.

The Data Board block diagram is shown in Figure 4-6. The board assembly drawing, schematic diagrams, and list of material are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Data Input Control (Schematic Sheets 3 and 7)
- Operating Modes (Schematic Sheet 3)
- Sampling Circuit Operation (Schematic Sheet 3)
- Data Pipeline Control (Schematic Sheets 2 and 3)
- Memory Control (Schematic Sheet 2)
- MPU Interface (Schematic Sheet 7)

Data Input Control

In the circuit descriptions which follow, all references are made to data input signals for AF, BF and CF which are used as an example.

Circuits for the 15 remaining signals at each Input Section are identical except as noted.

The differential input signal from the probe (schematic sheet 3) is buffered onto the Data Board by the 10216 Line Receiver Buffer at location 2B (upper left corner of schematic). Output of the buffer is presented to the 10121 gates at location 2D.

Control signals from the MPU Holding Registers (schematic sheet 7) select which of the four data sources, Memory, Probe, Multiplex, or Diagnostic, will be passed through to the sampling circuitry. A description of each data source type follows:

Memory Data: This data source is a recirculation of the channel memory output which is used only for self-diagnostic purposes (Memory Select).

Probe Data: This data source is used in normal input mode (Normal Select).

Multiplex Data: This data source obtained from the low order channels is also routed to the high order channels (F-8). In this case, channel F is paired with channel 7, allowing single probing when demultiplex is selected (Demux Select).

Diagnostic Data: This data source is supplied by the MPU for self-diagnostic purposes.

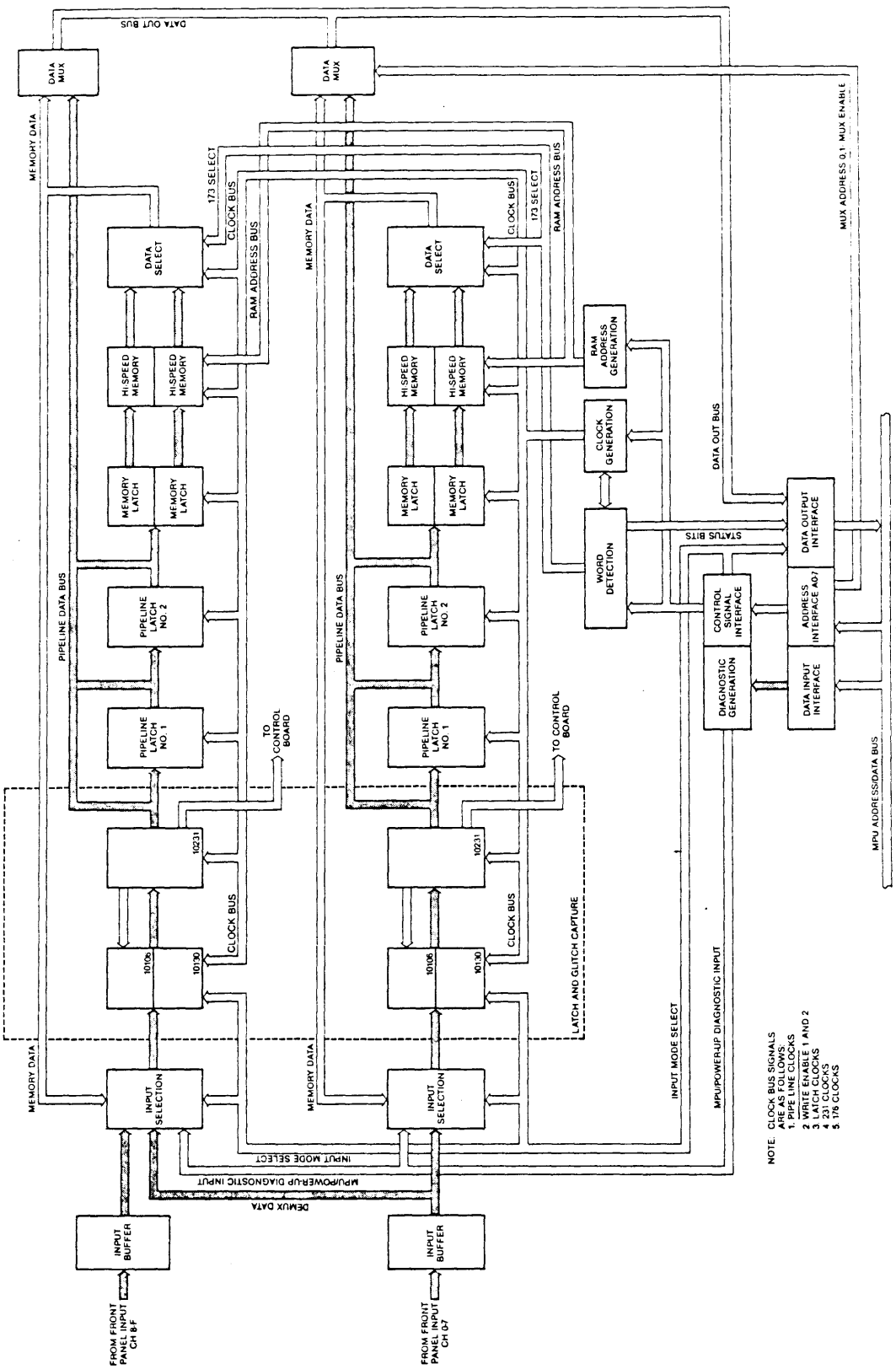


Figure 4-6. K450 Data Board, Block Diagram

Operating Modes

The output of the 10121 gate at location 2D (schematic sheet 3) is presented to the mode selection circuit consisting of two 10H106 gates at location 2E, the two 10H130 latches at location 2H and 10H131 latches at location 2J. This circuit has three different modes of operation, Sample Mode, Latch Mode, and Glitch Mode which are described in subsequent paragraphs.

Sample Mode: Pins 6 and 12 of the 10H106 gates, location 2E are held high by the MPU, causing these gates to become disabled in sample mode. Pins 6 and 9 at the 10H130 latch, location 2H are held low by the MPU which causes the latch output to follow the input asynchronously. The 10H131 latch at location 2J is the sample register. The input data is transferred to the output and held at the rising edge of the sample clock on pin 9.

Latch Mode: The gate, 2E is disabled as described in Sample Mode. Pin 6 of the 10H130 latch at location 2H is held low allowing the Latch Enable Clock at 2H, pin 9 to control the latch. When the latch clock is low, 2H is transparent as in sample mode. When the latch clock goes high, the data that was true at the clock transition is held at the output. The 10H131 sample register at location 2J functions the same as sample mode conditions.

Glitch Mode: The MPU signal Glitch Disable, is low in this mode allowing outputs of the 10H106, location 2E to be controlled by the input data and the data in the sample register. The MPU signal, Glitch Enable, is high in this mode, thereby disabling the D input pin of the 10H130 latch at location 2E. The state of the 2H latch output is then controlled by the outputs of 2E through the asynchronous set and reset pins.

Sampling Circuit Operation

The sampling circuit (sheet 3 of schematic diagram) operates as follows:

Assume that pins 2 and 15 of the 10H130 and 10H131 latches, at locations 2H and 2J respectively, are high at the start of operation. The input pin 5 of gate 2E is high thereby disabling the upper gate that goes to pin 5 of latch 2H. The input at pin 13 of gate 2E is low which allows any low input signal to reset 2H, pin 2 by placing a high on the direct reset, pin 4. Pin 2 of latch 2H remains in this new state regardless of any activity on the input signal.

At the next sample clock, the output of pin 15 at latch 2J goes low which enables the upper gate of 2E to respond to a high input signal only. If the input signal goes high at anytime, the signal at pin 3 of gate 2D goes low causing pin 3 of gate 2E to go high which sets the output of latch 2H to a high condition for the next sample clock.

In addition to going to the Glitch Feedback Comparison Gates, outputs of the register are also supplied to:

1. The 10174 multiplexer at location 2L for MPU diagnostic access.

2. The pipeline register 10176, location 2K.

3. Inverted data from pin 14 of latch 10H131 goes to the Control Board word recognition circuits.

5 ns Sampling (200 MHz Operation)

The DEMUX SELECT signal is active low at 2D, pin 9 and 2C pin 12. This allows data from the same channel (channel 7 in this example) to be sampled by IC's 1H and 2H. A rising edge of the LATCH CLK 0-7 signal, latches the data at 1H, pin 7. Then 5 ns later a rising edge of the LATCH CLK 8-F signal, latches the data at 2H, pin 7. Since the data going to these two pins are from the same channel, data is sampled every 5 ns. The outputs of 1H and 2H are then sampled by 1J and 2J every 10 ns.

Data Pipeline Control

The Data Pipeline (sheet 3 of schematic diagram) consists of two stages of D registers contained in the 10176 latch at location 2K. The source of the pipeline clock depends on either of two clock modes selected. In most modes, the pipe clock is the same as the Master (Control) Clock. In Store mode, the pipe clock is the same as the sample clock. Note that the data in both stages of the pipeline is also present at the 10174 multiplexers, locations 1L and 2L for diagnostic access.

Pipeline data is also presented to the inputs of both 10176 registers at locations 6D and 6E which begin two-way memory multiplexing. The registers at locations 6D and 6E act as pre-memories and are clocked by the rising edge of signals $\overline{WE}$01 and $\overline{WE}$02. They are outputed from the OR gates, location 6J or schematic sheet 2. The $\overline{WE}$01 and $\overline{WE}$02 signals are 180 degrees out of phase, which causes samples to be stored alternately in the two 10474 (2051), 512x4 RAMs at locations 5B and 5C. The 10173 demultiplexer at location 5D demultiplexes the memory. The data out of 5D goes back to the 10121 input selectors at location 2D for diagnostic recirculation and to the multiplexers at location 1L and 2L for MPU access.

Memory Control

The Memory Control logic (sheet 2 of schematic diagram) is implemented by the 100155 Mux Latch at location 6H which keeps track of control signals from the MPU and Control Board. This Mux Latch also controls which phase of memory will be written to, or read from, next through the 01 and 02 signals which alternately enable the two 100101 gates at location 5J.

When Internal Clock is used, the OLD TRACED signal, output from pin 2 of 6H combines with the $\overline{\text{ASYNCH MODE}}$ signal from the MPU to form the $\overline{\text{MEMORY ALIVE}}$ signal which enables pins 5 and 9 of the 100101 gates at location 5J.

When External Sample Clocks are selected, the $\overline{\text{MEMORY ALIVE}}$ signal is derived from the $\overline{\text{SYNC MODE MPU}}$ control signal and the $\overline{\text{TRACED}}$ signal from the Control Board. The outputs of pins 5 and 9 at location 5J are the $\overline{WE}$ pulses for the record memories.

The HALTED output signal from Mux Latch at location 6H disables the OR gates at location 5K. These gates pass the sample clock and select the source of the pipe clock. The OR gates at location 6J distribute all clocks and the WE signals. Note that the width of 173 clocks at gate 6J, pin 13 is set by a difference in propogation delay when the same signal feeds both inputs through two different paths.

MPU Interface

The MPU Interface circuits (sheet 7 of schematic diagram) decode the MPU Address Bus through the 10124 TTL to ECL Translator at location 8K, the 74S85 four-bit comparator at location 9M and the associated circuits. The 10124 translators at locations 6M, 7L, 10L and 9K are also used as TTL to ECL level translators for the data bus. These translators feed the inputs of the 10176 Hex D Latches which hold control information from the MPU.

The 10173 Multiplexers at locations 12M and 13M multiplex the lower 8 bits of Read data to the MPU. The 10125 TTL to ECL level translators at locations 1M, 2M, 3M and 11M translate TTL logic levels received from the bus to ECL logic level for data board interface.

CONTROL BOARD OPERATIONS

Overview

This section describes theory of operation for the K450 Control Board assembly, part number 0114-0120-10. The Control Board contains all decision making logic for controlling the recording process.

This includes word recognition circuits, delay counters, and the logic to combine delay conditions with detected words. These circuit functions cause the K450 to stop recording, jump or advance to another level with different record parameters and selectively enable or disable the recording operation.

The Control Board block diagram is shown in Figure 4-7. The board assembly drawing, schematic diagrams, and list of material are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Word Recognition Circuits (Schematic Sheets 1, 2, and 3)
- Word Selection Circuits (Schematic Sheets 4 and 5)
- Level Switching Circuit (Schematic Sheet 6)
- Delay Counter (Schematic Sheet 8)
- Recording Control Circuits (Schematic Sheet 7)
- MPU Interface (Schematic Sheet 9)

Word Recognition Circuits

The Word Recognition Circuits are contained on sheets 1, 2 and 3 of schematic diagrams. Word recognition is accomplished separately for each Input Section, A, B, and C with the separate words being combined in the word selection circuits described in subsequent paragraphs. In the circuit descriptions all references are made to the Section C Input (schematic sheet 3) which is used as an example. Sections A and B operate identically to Section C.

The DATA signal supplied from the Q output of the sample registers on the C Data Board enters the Control Board through the motherboard. It is synchronized with the control clock in the 10176 registers at locations 1H, 2H, and 3H.

The data output from these registers is presented to four of the eight address inputs, and to each of the four 10474 (2051), 256x4 Static RAMs at locations 1G, 1F, 3G and 3F. The other four address lines of the RAMs are driven by the LEVEL X signal, where X is the 4-bit number representing the level of trace control. The four data outputs of the 10474 RAMs correspond to the four combinational functions of the K450 for STOP, JUMP, ADVANCE and TRACE signals generated by the 100101 OR gates at locations 1D and 3D.

The MPU initializes the RAMs to contain zeros only at those address locations and bit positions that correspond to the combinations selected by the user for STOP, JUMP, ADVANCE and TRACE at each level.

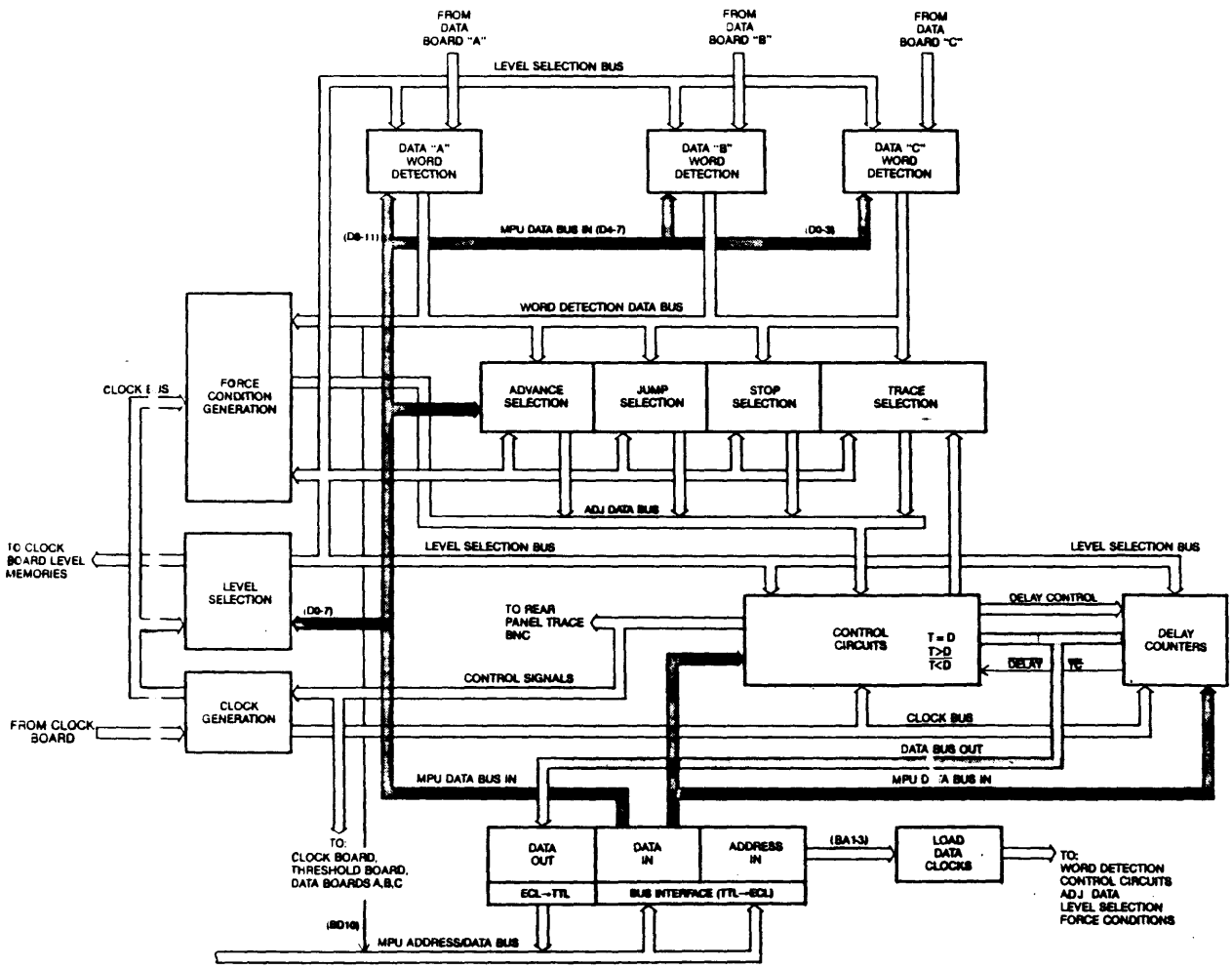


Figure 4-7. K450 Control Board Block Diagram

The RAMs function as programmable logic arrays. They respond to different STOP, JUMP, ADVANCE and TRACE combinations at each of 16 levels for a total of 48 combinations. The 100101 OR gate at 3D combines the outputs from four RAMs into the signals for STOP C, JUMP C, ADVANCE C and TRACE C (where C = Section C Inputs). The 10176 Holding Register at location 2J stores MPU control signals that are used during initialization. The 10164 Multiplexer at location 4C gives the MPU access to section outputs for diagnostic purposes.

Word Selection Circuits

The Word Selection Circuits are found on Sheets 4 and 5 of the schematic diagrams. The signals for STOP A, B, and C; JUMP A,B,and C; ADVANCE A, B, and C, and TRACE A, B, and C are combined with the delay condition signals $\overline{T<D}$, $\overline{T=D}$ and $\overline{T>D}$ in these circuits. In this example, only the ADVANCE select circuit is considered. The STOP, JUMP and TRACE circuits generally operate in the same manner as the ADVANCE circuit.

The signals for ADVANCE A, B, and C, and their complements along with the delay condition signals $\overline{T<D}$, $\overline{T=D}$, and $\overline{T>D}$ are presented to the inputs of the 100102 gates at locations 5C and 5D. Each of these gates is also supplied with one of the outputs of the 10145A High Speed, 4x16 RAMs at location 4B, 5B and 6B. The outputs of gates 5C and 5D are NORed together in the 100101 gate at location 5F whose input must be low for the ADVANCE signal to go high. The ADVANCE signal will be low if any of the gates at location 5C or 5D have lows on all three inputs. Pin 19 of gates at locations 5C and 5D is common to all gates. It is low at all times except during Diagnostic Tests or when the Arm Initialization condition is present. The MPU can pull it high for the FORCE ADVANCE condition, as in the following example:

1. Assume the user has selected conditions for:
   Advance if Data=A and T=D

2. For this selection, the MPU would initialize the 10145A High Speed RAMs to place a low state at pins 1 and 17 of gate 5C. Signals at the appropriate level would be applied to pins 17 and 24 of gate 5D.

3. The controlling input signals to these gates become: ADVANCE B, $\overline{T<D}$, $\overline{T>D}$, ADVANCE C, and ADVANCE A.

4. If any one of these signals is low, indicating the selected equation is false, the output of the gate it controls will be high, causing $\overline{\text{ADVANCE}}$ to be true and ADVANCE to be false.

The address inputs to the 10145A High Speed RAMs is the 4-bit LEVEL number (e.g., LEVEL 3C, LEVEL 2C, LEVEL 1C and LEVEL 0C). It is therefore possible to select a different Advance equation for each of the 16 levels of trace.

The inputs to the 100101 OR Gate at location 7D parallel the inputs supplied to OR Gate at location 5F which are controlled by the Word Recognition Logic, disregarding the delay conditions. The outputs of 7D are called EVENT and $\overline{\text{EVENT}}$ which are used to control the delay counter in Events Delay Mode.

The 10176 Registers at locations 6A and 7A are used to hold MPU control signals which can force the signals for $\overline{\text{STOP}}$, STOP, $\overline{\text{JUMP}}$, JUMP, ADVANCE, $\overline{\text{ADVANCE}}$, TRACE, $\overline{\text{TRACE}}$, EVENT, and $\overline{\text{EVENT}}$ to a desired logical state by overriding the normal input conditions. These signals are used during the Diagnostic Checks and the Arm Initialization Sequence.

The register at 6A also enables the 10H131 Latch at location 5A to FORCE ADVANCE for one clock period. This is used for manual advance and to begin the armed cycle when the unit advances from Level F into Level 0 on the first control clock.

Level Switching Circuit

The Level Switching Circuit is contained on sheet 6 of the schematic diagrams. The 100155 IC at location 5G is a Quad Multiplex Latch. The two sets of inputs to the latch come from the two 10145A RAMs at locations 5H and 5J. The address input to 5H and 5J is the 4-bit number level. The 5H and 5J RAMs are initialized by the MPU so that for any given level address, 5H contains the number of the user selected Jump To Level.

The 100155 has two Enable inputs, both of which must be in a low state for the selected input to be transferred to the output as the next level. One of the Enables is driven with the $\overline{\text{JUMP OR ADVANCE}}$ control signal, allowing the level to change only when a JUMP or ADVANCE condition is detected. The other Enable is a 3nsec pulse derived from the control (master) clock. The new level then becomes the new address for the Level RAMs 5H and 5J. The propagation delays around the loops are that much greater than the 3nsec Latch Enable pulse that allows glitch-free operation to occur. The $\overline{\text{JUMP}}$ condition present at pins 16 and 17 of 5G selects which set of inputs becomes latched. The decision to jump or advance gives priority to jumping even when the advance condition is true at the same time.

Delay Counter

The Delay Counter circuit is shown on sheet 8 of the schematic diagrams. The 10016 at location 13C and 13E form a simple Programmable Synchronous Counter. The 10145 RAMs at location 14C and 14F are addressed by the Level. Each address is initialized by the MPU with the two's complement plus 1 of the delay number for the corresponding Level.

Recording Control Circuits

The Recording Control circuits are shown on sheet 7 of schematic diagrams. The ICs at location 12A, 12B and 14B store the status of the Control Board that was present prior to the most recent transition of the control clock. Note that all output signal names are expressed in past tense. The input conditions that caused the outputs to become true may not always remain true after being latched. These remembered state signals are decoded by gate circuits located at 11D, 11C, 11B, 11A, 11F and 9B along with the DELAY TOP COUNT (TC) signal (supplied from location 11D on sheet 8 of schematic). The TC signal controls the delay status bits, T=D, T<D, and T>D to stop recording at the correct time and to control the process of selective trace recording.

The 100155 Mux Latch at location 12B has three inputs, $\overline{\text{EVENT ADVANCE}}$ and JUMP. Two of these inputs $\overline{\text{ADVANCE}}$ and JUMP are connected to both the A and B Mux inputs and are clocked to the output regardless of the state of the Mux Selection Control on pins 16 and 17 of 12B.

The two output signals ADVANCED and JUMPED are ORed together at location 11C, to form the $\overline{\text{DELAY PE}}$ signal. This allows the delay counter to become loaded on the next clock transition and Advanced or Jumped which is used to control the states of the delay condition signals.

The Mux Select control signal for 12B is the EVENT MODE signal which is output of the 10145A RAM at location 13A. This bit is high at those levels in which the user has selected Events Delay Mode. If EVENT MODE is low, the A Mux inputs of 12B are selected causing output pin 9 of 12B to become latched low only when $\overline{\text{EVENT}}$ is low.

The output signal at pin 9 of 12B is called $\overline{\text{EVENTED}}$ and is combined with the $\overline{\text{OLD T=D}}$ signal (which is at a low state if T was less than D prior to the last clock) to form the $\overline{\text{DELAY CE}}$ signal. Operation in Events Delay Mode only allows the Delay Counter to increment once for each sample on which the selected event combination was true.

The 10055 Mux Latch at location 14B also has three inputs, ADVANCE, STOP and TRACE. The STOP and TRACE inputs are connected to both the A and B Mux inputs. The STOP input signal becomes STOPPED after being clocked through 14B and causes the ARMED signal to become false thereby ending the recording process. The TRACE input signal becomes TRACED and $\overline{\text{TRACED}}$ after being clocked. The TRACED signal is combined with ARMED and is fed to a BNC connector on the rear of the K450 chassis as the TRACE signal. The $\overline{\text{TRACED}}$ signal is routed to the Data Boards where it is combined with the ARMED signal to allow the sample that caused the trace condition to be recorded.

The third input to Mux Latch at location 14B is the ADVANCE signal which is connected only to the B Mux input at pin 15. The Mux control input which determines whether ADVANCE will be latched in 14B is the END LEVEL signal which is one of the outputs supplied from the 10145A RAMs at location 13A. The END LEVEL signal will be high only at Level F.

The output signal at pin 9 of 14B is called ADVANCED and ENDED. As the name implies, the signal will be true only if Advance and End Level are both true when 14B is clocked. The Advanced and Ended condition causes the ARMED signal to go false thereby ending the recording process.

The 10176 Mux Latch at location 12A has six inputs: $\overline{\text{D=1 IF JUMP}}$, $\overline{\text{D=1 IF ADVANCE}}$, CYCLE RESET, $\overline{\text{T<D}}$, $\overline{\text{T=D}}$, AND $\overline{\text{T>D}}$. The CYCLE RESET signal is used only by the MPU during the Arm Initialization cycle or during Self Diagnosis. The other five inputs to 12A coordinate the switching of the delay status bits. The signals for $\overline{\text{D=1 IF JUMP}}$ and $\overline{\text{D=1 IF ADVANCE}}$ are supplied from the 10145A RAM at location 13A. These signals provide a look ahead function to provide delays of one which the 10016 Delay Counter cannot provide. The signals for $\overline{\text{D=1 IF JUMP}}$ and $\overline{\text{D=1 IF ADVANCE}}$ will be low only if the next level (either the JUMP-TO or ADVANCE-TO level, or both) has a delay of one selected.

The outputs of 12A for $\overline{\text{D=1 IF JUMPED}}$ and $\overline{\text{D=1 IF ADVANCED}}$ are combined with the $\overline{\text{JUMPED}}$ and $\overline{\text{ADVANCED}}$ signals respectively at location 11C and 11D to cause the T=D signal to become true immediately upon entering a level with a delay of one selected.

The signals for $\overline{\text{T<D}}$, $\overline{\text{T=D}}$ and $\overline{\text{T>D}}$ are clocked through 12A to become $\overline{\text{OLD T<D}}$, $\overline{\text{OLD T=D}}$ and $\overline{\text{OLD T>D}}$. These three signals also must be present at 11B, 11C, and 11D to ensure proper cycling of the delay condition bits. The 10164 Multiplexers at locations 12C and 12F provide access for the MPU to determine record control status for self-diagnostics.

MPU Interface

The MPU Interface is shown on sheet 9 of the schematic diagram. The 74LS85 Comparator at location 13H decodes the address bus to enable the interface only when the Control Board is addressed. The 10124 Translators at locations 11H, 8J, 7J, 3J and 10H provide TTL to ECL level translation for the 16 line address/data bus. The read data from the Control Board is multiplexed down to only four lines. These lines are translated from ECL to TTL levels by the 74368A Three-State Inverter Buffer at location 12H. The 10161 Demultiplexer at location 13G decodes Address Lines A1, A2 and A3 along with the $\overline{WR}$ signal from the MPU to provide LOAD signals for the MPU programmable holding registers, word detection RAMs and control RAMs.

Chapter 5

DISK DIAGNOSTICS

INTRODUCTION

This chapter provides the technician with descriptions of, and instructions for executing diagnostic test routines contained on the K450 Master Diagnostic Disk, Gould part number 0120-0290-10. Separate test routines are provided for each printed circuit board and associated circuits, excepting the MPU Board. The MPU Board is tested by the K450 Power-Up diagnostic firmware which verifies the operational status of the MPU Board whenever the K450 unit is initialized. The MPU Board must therefore be functional to load and execute the K450 Disk Diagnostic Routines.

The K450 Diagnostic Operating System (DIAG) software is organized as shown in Figure 5-1. The operating system is a monitor control program designed to checkout hardware/software functions for K450 printed circuit boards and components. The K450 DIAG is driven by the 8086 CPU on the MPU Board. The diagnostic routines are executed by using keys on the keyboard to select and set up a specific test module and control the testing operating.

Major features of DAIG are as follows:

- o DIAG provides a menu for the operator to enter options and parameters. The individual Diagnostic modules use these options to determine program flow and operation.

  These options specify which boards in the system are to be tested, the number of times to repeat each test, halt diagnostic execution upon error, loop diagnostic execution upon error, test floppy disk Drive A or B, test Drive Side 0 or Side 1, display or suppress error messages and allow operator interaction while running the Diagnostics. These options and parameters are explained in a later section.

- o DIAG loads Diagnostic modules from Disk and executes them. The Diagnostic modules consist of six programs on the K450-D disk and are loaded in one at a time, and executed. Due to the size of the modules, (up to 40k in length), and the limited RAM space available, (64k), it would be impossible for all of the code required to test the K450 to be resident in memory at once.

  So when DIAG is testing a particular board, the appropriate Diagnostic module is then loaded in from the Disk as an overlay and executed. These Diagnostic modules are discussed in a later section.

- o DIAG provides Pass/Fail History information. DIAG keeps a tabulation of each time a test is executed, and whether it Passed or Failed. This information is accumulative, so if the Diagnostic is run for a long period of time, the Pass/Error information is a total representation of all Passes and Errors.

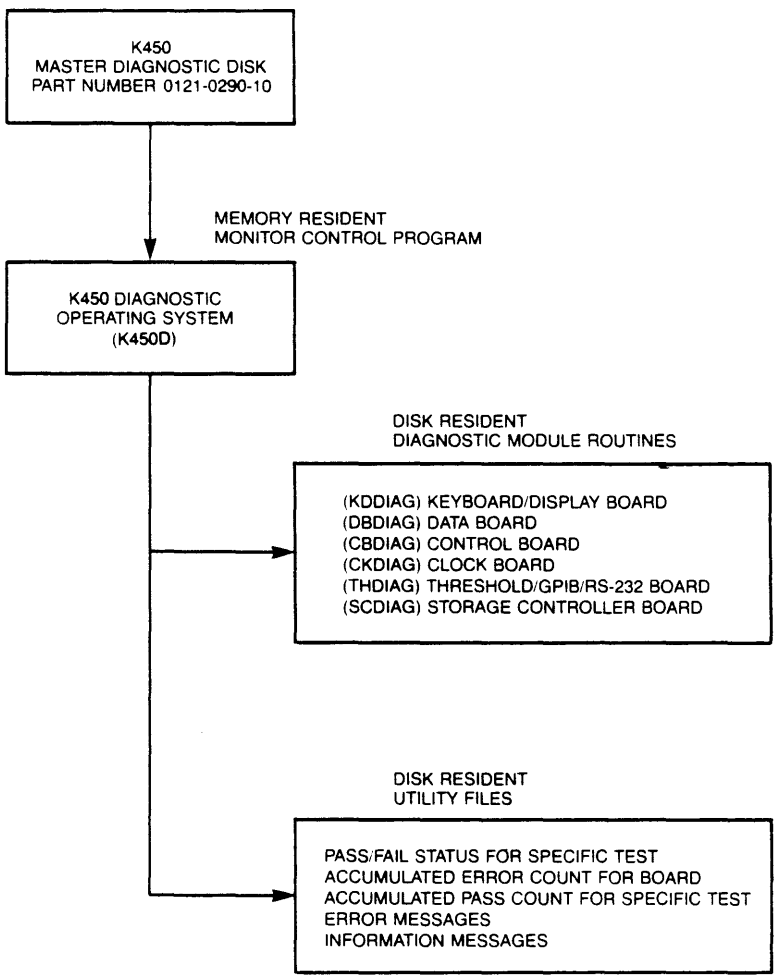


Figure 5-1. Organization of K450 Diagnostic Software

NOTE: The maximum number of Passes and Errors DIAG can log is 65,535. If the error count reaches this limit, it will not wrap around to 0, rather DIAG stops incrementing this count.

STARTING UP THE K450 DIAGNOSTICS

```
* * * * * * * * * * * *CAUTION* * * * * * * * * * * * *
*                                                       *
*    Prior to using the K450 Master Diagnostic          *
*    Disk, it is recommended that the user format       *
*    and copy the master disk as described in the       *
*    K450 Disk Storage System User's Manual Addendum.   *
*    Store the master disk and use the duplicate as     *
*    a backup to avoid possible damage to the original. *
*    Ensure the duplicate disk is write protected to    *
*    prevent inadvertent writing that could destroy     *
*    data.                                              *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * *
```

When The K450 Logic Analyzer is powered on, it performs its power on self-test Diagnostics. Assuming these have Passed, the Logic Analyzers's default menu is displayed. To boot up the Disk Operating System, insert the mini Floppy Diskette into Disk Drive A with the Write protect tab nearest to the activity light, and close the door on the Drive. Press the I/O key, then press the 1 key. This boots up the Disk Operating System and the screen display should change to show the directory contents of the Diskette. The following files should be in the display:

450D -01.EXE (K450 Diagnostic Operating System)

KDDIAG-00.EXE (Keyboard/Display Diagnostic Module)

DBDIAG-00.EXE (Data Board Diagnostic Module)

CBDIAG-00.EXE (Control Board Diagnostic Module)

CKDIAG-00.EXE (Clock Board Diagnostic Module)

THDIAG-00.EXE (Threshold/GPIB Board Diagnostic Module)

SCDIAG-00.EXE (Storage Controller Diagnostic Module)

Other files may be listed, but they are irrelevant to the Diagnostics.

The diagnostic modules for KDDIAG, DBDIAG, CBDIAG, CKDIAG, THDIAG and SCDIAG are not executable as stand alone programs. They are loaded in and executed by K450D-01.EXE. If a RECALL is done on one of these modules, the K450 locks up, and the power is turned off, and restored to reset system operations.

To load the K450 Diagnostic, press the NEXT key until the DOS RECALL selection appears. Press the RIGHT ARROW key to enter the filename field. Press the DOWN ARROW key until K450D-01.EXE is highlighted. Press the F4 key. This loads DIAG from the Disk and executes it. The K450 Diagnostic Main Menu is displayed.

DIAG MENUS AND DISPLAYS

Main Menu

The main menu is displayed upon booting up DIAG. This menu has three main fields.

The top of the screen has a list of the keys, and a description of the function for each key. Throughout the Diagnostic execution, the top of the screen has a list of keys. The keys listed and the functions of these keys vary, depending on the particular state or menu the Diagnostic is in.

The lower-right side of the screen has a list of the Active boards in the system. When DIAG began executing, it determined which boards were installed in the K450 chassis. The boards that it found are designated as Active, and these are the boards that are tested.

The lower-left side of the screen has a list of the Inactive boards, or the boards that are not present in the system. Some boards are optional, and since DIAG was written to test all possible components of a K450 system, boards that are not present are displayed as Inactive, indicating that these boards are not tested.

NOTE: The Active and Inactive status can be forced or overridden. If, a board is actually present in the system, but do not want to test it, force it to become Inactive by positioning the cursor with the UP or DOWN arrow keys, next to the name of the board, and press the LEFT ARROWkey. This action places the board into Inactive status. This is done for any or all boards.

Boards that are flagged as Inactive can be forced to become Active by positioning the cursor using the UP or DOWN ARROW key, next to the name of the board and pressing the RIGHT ARROW key. This would be useful if a board is actually in the system but is faulty, and caused it to appear in the Inactive status when DIAG started up. The board can be forced Active and tested.

Of course if a board is not in the system, and it is forced to be Active and the Diagnostic is run, it fails and gives non relevant information.

System Testing (All Active Boards)

When DIAG is started and the Main Menu is displayed, the Active/Inactive/Test >>> cursor is pointing to All Active Boards. If the NEXT Key is pressed, all of the tests for all of the boards in the Active list are automatically tested sequentially.

Before each test is executed it is loaded in by DIAG and the message Loading Diagnostic File, is displayed. The name of the current Diagnostic module is displayed at the top and the test names and test steps are updated.

During this automatic testing DIAG displays the number of Passes and Errors at the bottom of the screen. If there are any Errors, an Error message is displayed at the center of the screen, and the Error count at the bottom of the screen is incremented. The Pass counter at the bottom of the screen is not incremented until all tests for all Active boards are performed. Pressing the STOP key aborts the current test and returns to the Main Menu.

System Testing is normally performed if an overall picture of the unit's integrity is desired. Since all Subtests for all Active boards is performed, this test is long.

Single Board Testing

If a single board is to be tested, the Test >>> cursor is positioned next to the name of the board and the NEXT key pressed. This method is different from testing All Active Boards in several ways.

First, the testing is performed only on the chosen board.

Second, the testing is not started automatically. The Subtest Menu list for that particular Board is displayed, and either all Subtests are executed, or a single Subtest can be executed.

Third, the Pass and Error count is not displayed at the bottom of the screen.

Single Board testing is done when the integrity of a single board or boards is unknown, and a direct test on the board in question is performed. This method provides information at a quicker rate than if all the previous boards in the Active list are tested.

Pressing the STOP key aborts the current Subtest and returns to the Subtest Menu.

Conducting All Subtests or Individual Subtests

When a single board is selected for testing, the Subtest Menu is displayed. A single Subtest is performed by positioning the highlighting cursor, using the UP or DOWN ARROW keys, over the desired test and pressing the NEXT key. The single Subtest runs, and then returns to the Subtest Menu. If the parameter selection for NUMBER TO REPEAT TESTS is greater than 1, the particular Subtest is repeated that number of times.

Selecting ALL SUBTESTS executes all of the tests in the Menu sequentially, and returns to the Subtest Menu when complete.

Pressing the STOP key aborts the current subtest and returns to the Subtest menu. Pressing the PREVIOUS key restores the Main Menu.

DIAGNOSTIC PARAMETERS (EDIT KEY)

General

There are a number of options or parameters available for execution of the Diagnostic modules. These parameters control the program flow of execution. The parameters are displayed and/or changed at any time by pressing the EDIT key. This displays the list of parameters, and the current selections. Once the parameter options are selected, pressing the PREVIOUS key return to the previous Menu Display or program execution. The parameters are changed by positioning the highlighting cursor next to the desired parameter and pressing the NEXT key. This selects the opposite of the currently displayed option, (YES changes to NO). This method is valid for all parameters except the Times to Repeat Test.

The parameters are as follows:

	Parameter	Options	
1.	Halt on Error	No, Yes	(default is No)
2.	Loop on Error	No, Yes	(default is No)
3.	Display Error Messages	Yes, No	(default is Yes)
4.	Times to Repeat Test(s)	1 - 65535	(default is 1)
5.	Test Floppy Disk Drive A	No, Yes	(default is No)
6.	Test Floppy Disk Drive B	Yes, No	(default is Yes)
7.	Test Side 0 of Drive(s)	Yes, No	(default is Yes)
8.	Test Side 1 of Drive(s)	Yes, No	(default is Yes)
9.	Run Operator Action Tests	No, Yes	(default is No)

Halt on Error

The first parameter, Halt on Error, specifies that if an Error occurs during execution of the Diagnostic, the Diagnostic temporarily halts and the Error message remains on the screen. A HALTED ON ERROR message blinks on the screen to verify that the Diagnostic is halted. Diagnostic execution is resumed by pressing the NEXT key. If another error occurs, DIAG halts until the NEXT key is pressed.

Normally when there is an Error, and the Halt on Error parameter is not selected, the Error message is displayed on the screen for about a second. This does not allow adequate time to read all of the information displayed, so Halt on Error is useful for single stepping through the Errors that occur.

The disadvantage of Halt on Error is that when an Error occurs, all testing is suspended, and the NEXT key must be entered to resume. In the case where you want a unit to run the Diagnostics for a period of time without the need of operator actions, and then later check on the number of Passes and Errors, Halt on Error should be disabled by setting the option to NO.

Loop on Error

Loop on Error specifies that if during the execution of the Diagnostic an Error occurs, the Diagnostic loops on the test step that found an Error. This test step is repeated continuously even if it occasionally Passes.

The Loop on Error option is useful for debugging a board. For example, a board is intermittently failing, the continuous looping allows the operator to trigger on a Write pulse, a Read pulse or a Clock.

The looping continues until either the CONTROL key is pressed, or the Loop on Error option is disabled by pressing the EDIT key, and changing the selection to NO.

NOTE: The CONTROL key is used during the process of Looping on Error. Pressing the CONTROL key skips out of the current Test Step and proceeds to the next Test Step. It provides a means to quickly abort a Test Step without changing the Loop on Error Parameter.

NOTE: The Loop on Error option has one characteristic that is confusing. For example, the option is enabled and an Error occurs, the Error message is displayed as usual, and the test is repeated. But, the Error message is only displayed for about a second, so if the test starts Passing, the Diagnostic may appear to hang since no messages are displayed and the Test Step number remains constant. The Diagnostic is not hung up, it is in fact repeating the same Test Step without Error. Pressing the CONTROL key, or disabling the Loop on Error Parameter allows the Diagnostic execution to proceed.

Display Error Messages

This parameter controls whether or not the Error messages are displayed when Errors occur.

Normally when an Error occurs, and this option is set to YES, a message describing the Error is displayed for about a second, then the message is cleared. For most testing situations this is the desired response.

If a test is running that is rather lengthy, such as a RAM addressing test, and there are many Errors, the screen displays many Error messages. Each time a message is displayed the Diagnostic is paused, and this increases the Total Test Time. If the Display Error Messages is set to NO, this decreases the Total Test Time.

If the unit is to be run unattended (it is not necessary to view every Error message and the maximum number of test cycles desired), this parameter should be set to NO. The total number of Errors can be displayed at a later time by pressing the DATA key.

NOTE: When the Display Error Messages is set to NO, the Diagnostic module that is currently executing still calls the Error tabulation routine, so every Error is counted and tabulated.

Number of Times to Repeat Test(s)

This parameter controls the number of times a test is performed. The default is 1. This means when the test or tests are started by pressing the NEXT key, testing is executed one time and the Diagnostic will pause.

If several test repeats or continuous testing is desired, any number from 1 to 65,535 is selected. Enter this parameter by positioning the cursor, pressing the NEXT key, entering a number with 1 to 5 digits, and again pressing the NEXT key. (If 5 digits are entered, the terminating NEXT key need not be pressed.) For example, if the count desired is 158, press NEXT, 1, 5, 8, NEXT. If a number larger than 65,535 is entered, the program will requests to re-enter the number.

NOTE: If the repeat count is more than one, DIAG cycles through all Subtests of all Active boards and then repeat the cycle until the repeat count is reached.

At any time during this execution, the DATA key is pressed to view the Pass/Error history then the PREVIOUS key resumes execution. The EDIT key may also be pressed to change any of the parameters. The PREVIOUS key resumes execution.

Test Drive A, Test Drive B

This parameter refers to the Floppy Disk Drive tests for Disk Drives A and B. If a Drive is selected, a Disk Write/Read test is performed on that Drive, and a scratch Disk must be used since all data on that Disk is destroyed.

The default selections are Drive A = NO, Drive B = YES. The Diagnostic Disk is residing in Disk Drive A, and a scratch Disk should be residing in Disk Drive B. With the default selections, no operator actions are required. Drive B is tested, and Drive A is not tested.

If both Disk Drives are to be tested, the parameter options must be changed to Drive A = YES, and Drive B = YES. Each time DIAG is ready to test Disk Drive A, the Diagnostic Disk must be removed, and a scratch Disk placed in the Drive. When the test is complete, the scratch Disk is removed from Drive A, and the Diagnostic Disk re-inserted.

This procedure requires actions to be performed by the operator, and the RUN OPERATOR ACTIONS parameter must be enabled.

NOTE: A scratch Disk is defined as a new or fairly new Floppy Diskette, that is formatted using the K450 Disk Operating System Format command. The Write Protect slot must not be covered. The Disk used should not contain any important data or programs, since the process of Formatting and the Disk Drive testing destroys all data on the Diskette.

Test Side 0, Test Side 1

This parameter also refers to the Floppy Disk Drives testing. Each Disk Drive has two sides, Side 0 and Side 1. Normally parameters 7 and 8 are YES, and both sides are tested during the Floppy Disk testing.

For example, Disk Drive B is having Errors on Side 1, and no Errors on Side 0, setting the TEST SIDE 0 option to NO allows for more frequent testing of Side 1 of the Disk Drive, and give more Pass/Fail information at a quicker rate.

Run Operator Action Tests

Some of the tests in the Diagnostic modules require the operator to perform certain actions. One example is the testing of Disk Drive A requires the operator to remove the Diagnostic Disk and insert a scratch Disk, allows the test to run, then re-inserts the Diagnostic Disk.

Other actions might be the installation of RS-232 wrap-back connectors, the testing of the Keys on the K450 Keyboard, GPIB Testing, etc. If a unit is to run the Diagnostics unattended, this parameter should be set to NO, and the specific tests that require operator actions are not performed.

PASS/ERROR TABLUATION (DATA KEY)

At anytime during the Diagnostic Execution the number of Passes and Errors can be displayed by pressing the DATA key.

Pressing the PREVIOUS key returns to the previous Menu or executions. A list of the boards in the system is displayed, as well as the total number of Errors as follows:

Number of Errors Cycle Through All Tests	
Keybd/Display	0
Data Board A	0
Data Board B	0
Data Board C	0
Control Board	0
Clock Board	0
Threshold Board	0
Storage Controller Board	0

There are two fields that are highlighted by the cursor, they are Errors and Cycle Through All Tests. If the cursor is over Errors, pressing the NEXT key changes the display to the number of Passes, (changing Errors to Passes). Pressing the NEXT key again changes back to the Error display.

This Errors/Passes display shows the total accumulative Errors and Passes for each board in the K450 System. If a board is not in the system, or it was forced Inactive, the Pass and Error count is 0 for that board. Otherwise, the number of times DIAG tested the board is displayed for the Passes, and the total number, (if any), of Errors is displayed.

If the DOWN ARROW key is entered, this moves the cursor into the Cycle Through All Tests field. Pressing the NEXT key displays the total Errors/Passes for each Subtest of the Keyboard/Display Board. Pressing the NEXT key displays the total Errors/Passes for each Subtest of Data Board A.

Pressing the NEXT key displays the Data Board B, Data Board C, Control Board, Clock Board, Threshold Board, Storage Controller Board, and then finally back to the Board Level Error/Pass Display.

To view information about Data Board A, do the following steps:

1. Press the DATA key to display the Board list and total Error count.

2. Press the NEXT key to display the Board list and total Pass count.

3. Press the DOWN ARROW key. Press the NEXT key twice to display the Data Board A Subtest Pass count.

4. Press the UP ARROW key and then the NEXT key to display the Data Board A Subtest Error count.

5. Press the PREVIOUS key to return to the previous Menu.

DIAGNOSTIC RE-INITIALIZATION AND DIAGNOSTIC EXIT TO SYSTEM

General

When the Diagnostic Modules are executed, the Pass/Fail information is accumulated. Pressing the DATA key displays this information.

If a fresh start of the Diagnostic is desired, with the Pass/Error information set to 0, press the PREVIOUS key twice. This sets up the default Parameters, and sets all Pass/Error information to 0.

NOTE: Be careful using the PREVIOUS key while in Main Menu, it iseasy to re-initialize the Diagnostic by accident, and lose all the Pass/Error information that was accumulated.

Exiting the Diagnostic

When the K450 Logic Analyzer is powered on, it goes through its power on Diagnostics and comes up in the Default Menu. While in this menu, press the F2 key, the power on diagnostics are repeated.

While the K450 Diagnostic Operating System is under Execution, it is possible to exit back to the Default Menu of the Logic Analyzer. This is done by pressing the F2 key three times. This causes any Diagnostic execution to be aborted, and the K450 goes through the power on diagnostics and come up in the Default Menu.

Pressing the F2 key three times has the same effect as powering off the K450, and then powering it back on, without the need to remove the Floppy Diskettes.

NOTE: The F2 key must be pressed three times to avoid an accidental exit from the Diagnostic Operating System. Any other keys pressed between the three F2 keys voids out the exit.

SUMMARY OF K450 DIAGNOSTIC OPERATING SYSTEM KEYS

The K450 Diagnostic recognizes the following keys:

Key	Menu or Execution	Function
NEXT	Main Menu	Execute Diagnostic.
	Subtest Menu	Execute Diagnostic.
	HALTED ON ERROR	Resume Diagnostic execution.
	Parameter Menu	Change selected option.
	Pass/Error Display	Change Error display to Pass display, Cycle through Subtest lists.
PREVIOUS	Main Menu	Re-initialize Diagnostic.
	Subtest Menu	Return to Main Menu.
	Parameter Menu	Return to previous Menu/execution.
	Pass/Error Display	Return to previous Menu/execution.
EDIT	Any Menu or execution	Display the Parameter options.
DATA	Any Menu or execution	Display the Pass/Error data.
STOP	Any execution	Abort current test.

	HALTED ON ERROR	Abort current test.
ARROWS	Main Menu	Activate/Inactivate a Board, or Select a Board for testing.
	Subtest Menu	Select a Single Test or all Tests.
	Parameter Menu	Select a parameter.
	Pass/Error Display	Change fields for Errors/Passes, or cycle through Subtest lists.
CONTROL	Looping on Error	Skip out of current Subtest and proceed to the next Subtest.
F2	Any Menu or execution	Three consecutive key-strokes causes an EXIT from the Diagnostics and cold starts the K450 Logic Analyzer.

K450 KEYBOARD/DISPLAY BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes subtests that are executed on the K450 keyboard/ display board, how error reporting is done, and the concept behind each subtest program.

There are eight subtests written for the keyboard/ display board. Each of the subtests are described individually on the pages which follow. Loop on error, error count, and pass count update are incorporated into each subtest. Details for selecting the various test options and parameters for controlling the diagnostic monitor are described in the Introduction for Chapter 5.

All Error Messages are preceded by a "*". All Information Messages use the ">" prefix.

Early exit of each subtest is accomplished by pressing the "STOP" key.

ASSUMPTIONS

This series of tests assumes that the following boards are installed and are operational:

1. MPU
2. Threshold/GPIB/RS-232
3. Clock
4. Control

SUBTEST CATEGORIES

1. Keyboard Test
2. Interrupt Controller (8259) Test
3. Clock/Calendar (5832) Test
4. Video RAM Data Test
5. Video RAM Address Test
6. 6116 RAM Data Test
7. 6116 RAM Address Test
8. Beeper Exercise

ERROR COUNT CATEGORIES

1. Subtest 1 Error Count
2. Subtest 2 Error Count
3. Subtest 3 Error Count
4. Subtest 4 Error Count
5. Subtest 5 Error Count
6. Subtest 6 Error Count
7. Subtest 7 Error Count
8. Subtest 8 Error Count

Keyboard/Display Diagnostic Subtest 1

TITLE: KEYBOARD TEST

TARGET LOGIC: 8E, 14E, 13E, 10E and keyboard interface matrix

PURPOSE: The keyboard logic is functionally tested by pressing a specified key on the front panel, reading the corresponding I/O port from buffer (10E), and then verifying the key data to the expected data.

TEST DESCRIPTION: There are 48 keys on the front panel; the corresponding I/O Port, 1xh are arranged as follows:

a. x=0 if key is located at column 1 in the front panel
b. x=2 if key is located at column 2 in the front panel
c. x=4 if key is located at column 3 in the front panel
d. x=6 if key is located at column 4 in the front panel
e. x=8 if key is located at column 5 in the front panel
f. x=a if key is located at column 6 in the front panel
h. x=c if key is located at column 7 in the front panel
i. x=e if key is located at column 8 in the front panel.

There are 6 key data read from the buffer (10e),they are arranged as follows:

a. the key data read=feh if the key is located at row 1 in the front panel
b. the key data read=fdh if the key is located at row 2 in the front panel
c. the key data read=fbh if the key is located at row 3 in the front panel
d. the key data read=f7h if the key is located at row 4 in the front panel
e. the key data read=efh if the key is located at row 5 in the front panel
f. the key data read=dfh if the key is located at row 6 in the front panel

The following information message is displayed before each key is tested:

>Press key labeled: ?????????????

Where ????????????? could be 1 character, for example, "0" through "9", a" through "f", or up to 13 characters, for example, "TRACE CONTROL" in the domain of 48 defined keys.

TEST STEP INFORMATION:

Test Step	Key Tested
1	NEXT
2	PREVIOUS
3	FORMAT
4	CLOCKS
5	TRACE CONTROL
6	ARM MODE
7	UP ARROW
8	LEFT ARROW
9	MEM A
10	DATA
11	TIMING

Test Step	Key Tested (cont'd)
12	GRAPH
13	RIGHT ARROW
14	DOWN ARROW
15	MEM B
16	A->B
17	SEARCH
18	COMPARE
19	CONTROL
20	REF
21	C
22	8
23	4
24	0
25	SHIFT
26	HELP
27	D
28	9
29	5
30	1
31	I/O
32	"X"
33	E
34	A
35	6
36	2
37	EDIT
38	INS
39	F
40	B
41	7
42	3
43	ARM
44	STOP
45	F1
46	F2
47	F3
48	F4

ERROR MESSAGE:

If a key data error occurs, the following message is displayed:

```
*Test FAILED--Test Step    ss
 Keyboard Error
 Expected Keycode   = eeh
 Keycode Found      = ddh
 Key Data Code Read = "?????????????"
```

where ss should be 1 through 48
ee should be 1 through 48
dd should be be 1 through 48

Keyboard/Display Diagnostic Subtest 2

TITLE: INTERRUPT CONTROLLER TEST

PURPOSE: The interrupt logic is functionally tested by selecting each interrupt on the 8259 controller and causing each interrupt to occur. As each interrupt is generated, the 8259 receives the interrupt then outputs a vector for the 8086 processor. At these vectors are routines which set diagnostic flags. These flags are examined to determine if the interrupt actually took place. The source of the interrupts are then turned off, and the flags are cleared. After a small amount of time the flags are re-examined to determine if the source of the interrupt has actually been disabled. If a flag is found to be set then an error message is displayed.

TARGET LOGIC: 4E, 2E, 8E, 10E, 9D, and 10D

TEST DESCRIPTION: The following table indicates the interrupt source and line for the diagnostic test step:

TEST STEP INFORMATION:

Test Step	Interrupt from	On Board	Interrupt Line
1	GPIB	Threshold	intr 1
2	RS-232	Threshold	intr 2
3	AUX	Threshold	intr 3
4	Total trace time clock (timer #0)	Clock	intr 4
5	(Simulated from software)		not currently assigned
6	Time of day	Display	intr 6 -
7	Disk	Storage Controller	intr 7

ERROR MESSAGE:

If an error occurs, the following messages are displayed:

```
*Test FAILED--Test Step   z
Intr 0z Not Generated.
```

where z = 1 - 7

```
*Test FAILED--Test Step   z
Unexpected Interrupt 0z Generated.
```

where z = 1 - 7

Keyboard/Display Diagnostic Subtest 3

TITLE: CLOCK/CALENDAR TEST

PURPOSE: This subtest verifies operation of the 5832 clock/calendar by saving the current time, then exercising the component by setting the time. The time is then read back and verified. If test is successful, it indicates the 5832 is operating properly.

The time is set so the next second time interval causes a rollover. An example of a rollover is if the minutes counter was set to 59. When minutes are advanced then the minutes counter becomes zero and the hours count is incremented by one. This rollover process continues until the years counter rolls over to 00 (from 99).

TARGET LOGIC: 2D, 2E, 3D, 4D, 5D and 7D

TEST DESCRIPTION: Operations are exercised on the clock calendar components according to the following table:

TEST STEP INFORMATION:

Test Step	Operation
1	Read current time, save for last step
2	Set clock to: Jan. 1, 1900 @00:00:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 1, 1900 @00:01:00
3	Set clock to: Jan. 1, 1900 @00:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 1, 1900 @01:00:00
4	Set clock to: Jan. 1, 1900 @23:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 2, 1900 @00:00:00

Test Step	Operation (cont'd)
5	Set clock to: Jan. 31, 1900 @23:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Feb. 1, 1900 @00:00:00
6	Set clock to: Dec. 31, 1900 @23:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 1, 1901 @00:00:00
7	Set clock to: Dec. 31, 1999 @23:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 1, 1900 @00:00:00

NOTE: Exiting this test via the STOP key restores the time saved in step 1. If power is removed during steps 2 - 7, the time is lost.

ERROR MESSAGE:

If the time read does not match the time expected, the following error message is displayed:

```
*Test FAILED--Test Step          x
Clock/Calendar Error
          year month  day hour  minute  second
Expected: aaa  bbb    ccc ddd   eee     fff
    Read: ggg  hhh    iii jjj   kkk     lll
```

where aaa, ggg = 000 - 999
bbb, hhh = 001 - 012
ccc, iii = 001 - 031
ddd, jjj = 000 - 023
eee, kkk = 000 - 059
fff, lll = 000 - 059

Keyboard/Display Diagnostic Subtest 4

TITLE: VIDEO RAM DATA TEST

PURPOSE: This subtest verifies that the Keyboard/Display Board does not prevent normal operation of the MPU RAM dedicated to video display.

TARGET LOGIC: 7A, 7B, 7C, 8A, 8B, 8C, 9A, 9B, 9C, 10A and 10B dedicated RAM on MPU Board used for video

TEST DESCRIPTION: Although the RAM under test is on the MPU Board, the Display Board uses this memory to create an image sent to the screen. Various data patterns are written to the MPU memory and read back. The data written is compared to the data read and if a miscompare is detected an error message is displayed. This continues until all the data patterns listed below have been tried.

TEST STEP INFORMATION:

Test Step	Value Written
1	00H
2	AAH
3	55H
4	CCH
5	33H
6	01H
7	02H
8	04H
9	08H
10	10H
11	20H
12	40H
13	80H

NOTE: This memory physically starts at location 0100h

ERROR MESSAGE:

If an error occurs during this subtest the following message is displayed:

```
* Test FAILED--Test step   xx
RAM Data Error
Value Written = aaH
Value Read    = bbH
Address Count = ccccH
```

where **aa** = 00 - FF
bb = 00 - FF
cccc = 0000 - 3FFF

Keyboard/Display Diagnostic Subtest 5

TITLE: VIDEO RAM ADDRESS TEST

PURPOSE: This subtest verifies that the Keyboard/Display Board does not prevent normal operation of the MPU RAM dedicated to video display.

TARGET LOGIC: 7A, 7B, 7C, 8A, 8B, 8C, 9A, 9B, 9C, 10A and 10B
RAM located on MPU Board used for video,

TEST DESCRIPTION: All of the RAM in this test is preset to zero then the indicated address is written with the value 0aah. All of the RAM is then read to verify that the indicated address is the only data element that was set to 0aah.

TEST STEP INFORMATION:

Test Step	Indicated Address
1	0000H
2	0001H
3	0002H
4	0004H
5	0008H
6	0010H
7	0020H
8	0040H
9	0080H
10	0100H
11	0200H
12	0400H

NOTE: This memory physically starts at location 0100h

ERROR MESSAGE:

If an error occurs during this subtest, the following message is displayed:

```
* Test FAILED--Test Step     xx
RAM Data Error
Value Written = aah
Value Read    = bbh
Address Count = cccch
```

where aa = 00 - ff
bb = 00 - ff
cccc = 0000 - 3fff

Keyboard/Display Diagnostic Subtest 6

TITLE: 6116 RAM DATA TEST

PURPOSE: This subtest verifies operation and integrity of the 6116 RAMs on the keyboard/display board by writing to the memory several different data patterns. This memory is then read back and compared to the value written. If a miscompare occurs then an error message is displayed. This process is repeated for all of the 6116 memory until all the patterns listed below have been tried.

TARGET LOGIC: 1B, 3B, 3C, 4C, 5B, 6B, 5E, 6E, 5C and 6D

TEST DESCRIPTION: The following is a summary of the data written to RAM during each test step:

TEST STEP INFORMATION:

Test Step	Value Written
1	00H
2	AAH
3	55H
4	CCH
5	33H
6	01H
7	02H
8	04H
9	08H
10	10H
11	20H
12	40H
13	80H

NOTE: This memory physically starts at location 040000h

ERROR MESSAGE:

If an error occurs during this subtest, the following message is displayed:

```
* Test FAILED--Test Step   xx
RAM Data Error
Value Written = aaH
Value Read    = bbH
Address Count = ccccH
```

where aa = 00 - FF
bb = 00 - FF
cccc = 0000 - 3FFF

Keyboard/Display Diagnostic Subtest 7

TITLE: 6116 RAM ADDRESS TEST

PURPOSE: This subtest verfies the operation and integrity of the 6116 RAMs on the keyboard/display board. All of the RAM in this test is preset to zero then the indicated address is written with the value 0aah. All of RAM is then read to verify that the indicated address is the only data element that was set to 0aah.

TARGET LOGIC: 1B, 3B, 3C, 4C, 5B, 6B, 5E, 6E, 5C and 6D

TEST DESCRIPTION: All RAM is preset to zero, then the indicated address is written with the value 0aah. All of RAM is read to verify the written data.

TEST STEP INFORMATION:

Test Step	Indicated Address
1	0000H
2	0001H
3	0002H
4	0004H
5	0008H
6	0010H
7	0020H
8	0040H
9	0080H
10	0100H
11	0200H
12	0400H

NOTE: This memory physically starts at location 040000h

ERROR MESSAGE:

If an error occurs during this subtest, the following message is displayed:

```
* Test FAILED--Test step    xx
RAM Data Error
Value Written = aaH
Value Read    = bbH
Address Count = ccccH
```

where aa = 00 - FF
bb = 00 - FF
cccc = 0000 - 3FFF

Keyboard/Display Diagnostic Subtest 8

TITLE: BEEPER EXERCISE TEST

PURPOSE: This subtest exercises the beeper circuitry. There are no error messages generated by this routine as there is no way to verify operation except via audio monitoring.

TARGET LOGIC: 15E, 16E, 17E and 18E

TEST DESCRIPTION: The beeper is activated by loading p0-p3 on IC with the duration value, then the line labeled cp is pulsed. The beeper is set to various durations as given in the following table:

TEST STEP INFORMATION:

Test Step	Duration
1	.1 sec
25	1.5 sec

ERROR MESSAGE:

There are no error messages for this subtest. Also note that since no errors are possible, "loop on error" and "halt on error" do not function.

K450 DATA BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes subtests that are performed by the K450 Data Board Diagnostic. The target hardware is presented, as well as a general description of each subtest, a list of information for each test step, and a description of Error Messages that may be printed for the subtest results.

The K450 Data Board Diagnostic is a board level test of the board operations that run under the K450 Diagnostic Operating System. The diagnostic can test from 1 to 3 Data Boards in the system. These correspond to Data Boards A, B and C. In order for the Diagnostic to run properly, the board under test must be installed on the Mother Board, (not on an extender card). The internal probe input cables must be connected to J1 and J2, and the external probes installed. All of the channels of all probes must be free from connection to anything (they must be allowed to float). Also, all of the other boards must be installed in the K450 system.

NOTE: The internal probe input cables are too short for the board to be installed on an extender card. If extension cables are used, then an extender card may be used.

Several of the subtests use a sequence of 24 Data patterns to write, read and verify an I/O port or Memory Address. These Data patterns verify that all 16 Data Bits are functional and completely independent of each other. These 24 Data patterns are as follows:

0000H, 5555H, AAAAH, CCCCH, 3333H, 6666H, 9999H, FFFFH,
0001H, 0002H, 0004H, 0008H, 0010H, 0020H, 0040H, 0080H,
0100H, 0200H, 0400H, 0800H, 1000H, 2000H, 4000H, 8000H.

When writing these Data patterns to an I/O port such as the Sample Register or the Pipeline Registers, the Data value can be randomly accessed. The ECL RAM Memory is a 2048 byte FIFO. All 2048 locations are accessed at the same I/O address, (0C6H for writes, and 0C0H for reads). The RAM's addressing is accomplished by sequential reads from, or writes to the RAM. Address counters on the board are incremented each time a RAM access (a Sample Clock) occurs.

The RAM actually requires 2051 Sample clocks to get 2048 words of data to the RAM. The three extra clocks are required to get the Data through the pipeline. After the 2048th clock, the 2048th Data value resides in the Sample Register. One more clock shifts it to the New Pipe Register. An additional clock shifts it to the Old Pipe Register, and the last clock writes it to RAM.

NOTE: When an I/O address is specified for explanation, the addresses for Data Board A are used. These addresses would only apply if Data Board A was being tested. Data Board B addresses are 0DxH, and Data Board C are 0ExH.

SUBTEST CATAGORIES

There are thirteen Subtests that are performed by the Data Board Diagnostic. These are categorized as follows:

1. Force Conditions Test
2. Data Path Test
3. Clocking Disable Test
4. Latch Bits 0-7 Test
5. Latch Bits 8-F Test
6. Glitch Bits 0-7 Test
7. Glitch Bits 8-F Test
8. Multiplex Select Test
9. Pipeline Shift Test
10. RAM Data Integrity
11. RAM Addr Integrity
12. Trace Conditions Test
13. Recirculate RAM Test

ERROR COUNT CATEGORIES

The Error Count Display information is a one for one match with the Subtest list above. The K450 Diagnostic Operating System will display the "Subtest n" instead of the actual test name.

Subtest 1 (Force Conditions Test)
Subtest 2 (Data Path Test)
Subtest 3 (Clocking Disable Test)
Subtest 4 (Latch Bits 0-7 Test)
Subtest 5 (Latch Bits 8-F Test)
Subtest 6 (Glitch Bits 0-7 Test)
Subtest 7 (Glitch Bits 8-F Test)
Subtest 8 (Multiplex Select Test)
Subtest 9 (Pipeline Shift Test)
Subtest 10 (RAM Data Integrity)
Subtest 11 (RAM Addr Integrity)
Subtest 12 (Trace Conditions Test)
Subtest 13 (Recirculate RAM Test)

Data Board Diagnostic Subtest 1

TITLE: FORCE CONDITIONS TEST

TARGET LOGIC:

6H
6M 7L 10L 9K 7F 5F 8F 9H 6L
8K 7K 9M 8L 12M 13M
1M 2M 3M 11M 8K
7K 9M 8L 8M 10M

TEST DESCRIPTION:

This subtest writes various commands to the Data Board and expects certain status values to exist. The commands are written to ports 0C2H and 0C4H. The status is read back from port 0C8H.

This test does not require any boards other than the MPU to be installed in the system. Specifically, it requires no clocking from the Clock Board.

TEST STEP INFORMATION:

Step	Status Expected
1	45H
2	65H
3	75H
4	F5H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:
ssss is the test step number in the range of 1 to 4.

hmsg is the Error heading message:

Not Halt, Mem full, ExpWrlow 02 Error
Multiphase Mode Clear Error
Async Mode Clear Error
Freeze Memory Clear Error

aaaa is the I/O address of the Data Board:

0C8H for Data Board A Status Register,
0D8H for Data Board B Status Register,
0E8H for Data Board C Status Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 2

TITLE: DATA PATH TEST

TARGET LOGIC:

6M 7L 10L 9K 6F 5H 9F
2D 1D 2C 1C 4D 3C 4C 3D
11D 10D 11C 10C 13D 12C 13C 12D
2H 1H 4H 3H 11H 10H 13H 12H
2J 1J 4J 3J 11J 10J 13J 12J
8K 7K 9M 8L 5K 6J
10K 11L 12L 13L
13M 12M 1M 2M 3M 11M 8M 10M

TEST DESCRIPTION:

This subtest checks the Data Bus path of the Data Board for functionality and Data Bit uniqueness. Data is transferred by sending output to the Diagnostic Latch at I/O address 0C6H, issuing a Sample Clock, receiving input from the Sample Register at I/O address 0C6H, and comparing Data. Since the Glitch Mode and Latch Mode are both disabled, the Data will slip through to the Sample Registers without the need for a Latch Clock.

The Clock Board is required to run this test. The "Sample Clock", P1-42 is used to clock the data to the Sample Register. This is achieved by doing a "KICK$CLOCK", which writes a "1" to Data bit D0 of Write Register 8, (0B8H), of the Clock Board. The majority of the subsequent subtests use this Data Path to exercise various features and functions of the Data Board. So if there are any errors in this test, there are bound to be many failures that follow.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	0C6H, Diagnostic Latch	0C6H, Sample Register
2	5555H	0C6H, Diagnostic Latch	0C6H, Sample Register
3	AAAAH	0C6H, Diagnostic Latch	0C6H, Sample Register
4	CCCCH	0C6H, Diagnostic Latch	0C6H, Sample Register
5	3333H	0C6H, Diagnostic Latch	0C6H, Sample Register
6	6666H	0C6H, Diagnostic Latch	0C6H, Sample Register
7	9999H	0C6H, Diagnostic Latch	0C6H, Sample Register
8	FFFFH	0C6H, Diagnostic Latch	0C6H, Sample Register
9	0001H	0C6H, Diagnostic Latch	0C6H, Sample Register
10	0002H	0C6H, Diagnostic Latch	0C6H, Sample Register
11	0004H	0C6H, Diagnostic Latch	0C6H, Sample Register
12	0008H	0C6H, Diagnostic Latch	0C6H, Sample Register
13	0010H	0C6H, Diagnostic Latch	0C6H, Sample Register
14	0020H	0C6H, Diagnostic Latch	0C6H, Sample Register
15	0040H	0C6H, Diagnostic Latch	0C6H, Sample Register
16	0080H	0C6H, Diagnostic Latch	0C6H, Sample Register
17	0100H	0C6H, Diagnostic Latch	0C6H, Sample Register
18	0200H	0C6H, Diagnostic Latch	0C6H, Sample Register
19	0400H	0C6H, Diagnostic Latch	0C6H, Sample Register
20	0800H	0C6H, Diagnostic Latch	0C6H, Sample Register
21	1000H	0C6H, Diagnostic Latch	0C6H, Sample Register
22	2000H	0C6H, Diagnostic Latch	0C6H, Sample Register
23	4000H	0C6H, Diagnostic Latch	0C6H, Sample Register
24	8000H	0C6H, Diagnostic Latch	0C6H, Sample Register

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Data Path Diag to Sample Reg Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the I/O address of the Data Board:

0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 3

TITLE: CLOCK DISABLE TEST

TARGET LOGIC: 5K 8J 6J 5L
6H 5A 6A 8A 9A
All Logic listed in Subtest 2

TEST DESCRIPTION:

This subtest checks the different ways of clocking the Data Board, and the different ways of disabling the clocking.

In Single Phase Mode the Sample Clock, P1-42 is used for all clocking on the Data Board. If the Multiphase Mode is selected, the Sample Clock, P1-42 is used for the Sample Register, and the Control Clock, P1-46 is used for the RAM, Pipelines and Address Counters.

A Condition called Force Clocks causes all Sample Clocks and all Control Clocks to be ignored. Also a condition called Halted disables these clocks.

This test also checks the Address Reset-Memory Full function. The address counters are reset by toggling W4B12. The Memory is filled by clocking the address counters 2048 times.

TEST STEP INFORMATION:

Step	Mode of Phase	Force Clocks	Data Expected
1	Single Phase	inactive	5555H
2	Multi Phase	inactive	AAAAH
3	Single Phase	active	0000H
4	Multi Phase	active	0000H

Step	"HALTED/"	MEMORYFULL	Status
5	high	low	0001H
6	low	high	0004H

Step	Mode of Phase	Force Clocks	Halt When Full	Data Expected
7	Single Phase	inactive	active	0000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 7.

hmsg is the Error heading message:

Force Clocks Enable Data move Error,
Force Clocks Disable Data move Error,
155 En2 Memory Not Full Status Error,
155 En2 Mem-Full/Halt Status Error,
Halt Freeze Sample Register Error.

aaaa is the I/O address of the Data Board:

0C6H for Data Board A Sample Register,
0C8H for Data Board A Status Register,
0D6H for Data Board B Sample Register,
0D8H for Data Board B Status Register,
0E6H for Data Board C Sample Register,
0E8H for Data Board C Status Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 4

TITLE: LATCH DATA BITS 0-7 TEST

TARGET LOGIC:

5F
5L
2H 1H 4H 3H 11H 10H 13H 12H

Diagnostic Latch Clock P1-44 (From Clock Board)

All hardware used in Data Path Test.

TEST DESCRIPTION:

This tests the latch mode of 10130 latches of the lower 8 bits, with the upper eight bits in transparent mode. The Latch Clock 0-7 feeds the common Enable input to the 10130's. This input is held high, and pulsed low to latch the current data from the "D" to the "Q". The Glitch is disabled so the other Enable input is held low. The upper bits 8-F are not latched, the Data slips through the "D" to the "Q".

If there are any errors in this test, but the Data Path Test passed, the failure is probably in the Latch Clock or the 10130's.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	0C6H, Diagnostic Latch	0C6H, Sample Register
2	5555H	0C6H, Diagnostic Latch	0C6H, Sample Register
3	AAAAH	0C6H, Diagnostic Latch	0C6H, Sample Register
4	CCCCH	0C6H, Diagnostic Latch	0C6H, Sample Register
5	3333H	0C6H, Diagnostic Latch	0C6H, Sample Register
6	6666H	0C6H, Diagnostic Latch	0C6H, Sample Register
7	9999H	0C6H, Diagnostic Latch	0C6H, Sample Register
8	FFFFH	0C6H, Diagnostic Latch	0C6H, Sample Register
9	0001H	0C6H, Diagnostic Latch	0C6H, Sample Register
10	0002H	0C6H, Diagnostic Latch	0C6H, Sample Register
11	0004H	0C6H, Diagnostic Latch	0C6H, Sample Register
12	0008H	0C6H, Diagnostic Latch	0C6H, Sample Register
13	0010H	0C6H, Diagnostic Latch	0C6H, Sample Register
14	0020H	0C6H, Diagnostic Latch	0C6H, Sample Register
15	0040H	0C6H, Diagnostic Latch	0C6H, Sample Register
16	0080H	0C6H, Diagnostic Latch	0C6H, Sample Register
17	0100H	0C6H, Diagnostic Latch	0C6H, Sample Register
18	0200H	0C6H, Diagnostic Latch	0C6H, Sample Register
19	0400H	0C6H, Diagnostic Latch	0C6H, Sample Register
20	0800H	0C6H, Diagnostic Latch	0C6H, Sample Register
21	1000H	0C6H, Diagnostic Latch	0C6H, Sample Register
22	2000H	0C6H, Diagnostic Latch	0C6H, Sample Register
23	4000H	0C6H, Diagnostic Latch	0C6H, Sample Register
24	8000H	0C6H, Diagnostic Latch	0C6H, Sample Register

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Latch Data bits 0-7 Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the I/O address of the Data Board:

0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 5

TITLE: LATCH DATA BITS 8-F TEST

TARGET LOGIC:

5F
5L
2H 1H 4H 3H 11H 10H 13H 12H

Diagnostic Latch Clock P1-44 (From Clock Board)

All hardware used in Data Path Test.

TEST DESCRIPTION:

This subtest is identical to the previous test except that the upper Data bits 8-F are tested instead of the lower bits 0-7.

The test verifies the latch mode of 10130 latches the upper 8 bits, with the lower eight bits in transparent mode. The Latch Clock 8-F feeds the common Enable input to the 10130's. This input is held high, and pulsed low to latch the current data from the "D" to the "Q". The Glitch is disabled so the other Enable input is held low. The lower bits 0-7 are not latched, the Data slips through the "D" to the "Q".

If there are any errors in this test, but the Data Path Test passed, the failure is probably in the Latch Clock or the 10130's.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	0C6H, Diagnostic Latch	0C6H, Sample Register
2	5555H	0C6H, Diagnostic Latch	0C6H, Sample Register
3	AAAAH	0C6H, Diagnostic Latch	0C6H, Sample Register
4	CCCCH	0C6H, Diagnostic Latch	0C6H, Sample Register
5	3333H	0C6H, Diagnostic Latch	0C6H, Sample Register
6	6666H	0C6H, Diagnostic Latch	0C6H, Sample Register
7	9999H	0C6H, Diagnostic Latch	0C6H, Sample Register
8	FFFFH	0C6H, Diagnostic Latch	0C6H, Sample Register
9	0001H	0C6H, Diagnostic Latch	0C6H, Sample Register
10	0002H	0C6H, Diagnostic Latch	0C6H, Sample Register
11	0004H	0C6H, Diagnostic Latch	0C6H, Sample Register
12	0008H	0C6H, Diagnostic Latch	0C6H, Sample Register
13	0010H	0C6H, Diagnostic Latch	0C6H, Sample Register
14	0020H	0C6H, Diagnostic Latch	0C6H, Sample Register
15	0040H	0C6H, Diagnostic Latch	0C6H, Sample Register
16	0080H	0C6H, Diagnostic Latch	0C6H, Sample Register
17	0100H	0C6H, Diagnostic Latch	0C6H, Sample Register
18	0200H	0C6H, Diagnostic Latch	0C6H, Sample Register
19	0400H	0C6H, Diagnostic Latch	0C6H, Sample Register
20	0800H	0C6H, Diagnostic Latch	0C6H, Sample Register
21	1000H	0C6H, Diagnostic Latch	0C6H, Sample Register
22	2000H	0C6H, Diagnostic Latch	0C6H, Sample Register
23	4000H	0C6H, Diagnostic Latch	0C6H, Sample Register
24	8000H	0C6H, Diagnostic Latch	0C6H, Sample Register

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Latch Data bits 8-F Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the I/O address of the Data Board:

0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 6

TITLE: GLITCH DATA BITS 0-7 TEST

TARGET LOGIC:

2E 1E 2F 1F
4E 3F 4F 3E
11E 10E 11F 10F
13E 12F 13F 12E
2H 1H 4H 3H
11H 10H 13H 12H

All hardware in the Data Path Test.

TEST DESCRIPTION:

This subtest tests the Glitch capture feature of the Data boards by enabling the Glitch circuitry which uses the Set and Reset pins on the 10130's, instead of the D inputs to send the Data from the 10121 Multiplexers to the Q output. The individual Enable pins on the 10130's are held high so that any clocking from the Diagnostic Latch Clock is disabled.

Each output instruction to the Diagnostic bits port 0C6H, latches the Data in the Glitch latches. A Sample Clock is required to send the Data through to the Sample Register. A maximum of two Data values may be output to the Diagnostic bits port before data overrun occurs.

The way that this circuitry is tested, is two consecutive Output instructions are performed with different Data. The first Data is checked at the Sample register after issuing a single Sample Clock. Another Sample Clock presents the Second Data to the Sample Register.

In this test, only Data bits 0-7 are in the Glitch Mode. The upper bits 8-F slip through the 10130's because both of the enable pins are low, so Q follows D.

TEST STEP INFORMATION:

Step	1st Data	2nd Data
1	0000H	------
2	0000H	0000H
3	0055H	0000H
4	00AAH	0000H
5	00CCH	0000H
6	0033H	0000H
7	0066H	0000H
8	0099H	0000H
9	00FFH	0000H
10	0001H	0000H
11	0002H	0000H

Step	1st Data	2nd Data (cont'd)
12	0004H	0000H
13	0008H	0000H
14	0010H	0000H
15	0020H	0000H
16	0040H	0000H
17	0080H	0000H
18	0000H	0000H
19	0000H	0000H
20	0000H	0000H
21	0000H	0000H
22	0000H	0000H
23	0000H	0000H
24	0000H	0000H
25	0000H	0000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Glitch Data Bits 0-7 Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 25.

aaaa is the I/O address of the Data Board:

0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a 1. Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 7

TITLE: GLITCH DATA BITS 8-F TEST

TARGET LOGIC:

2E 1E 2F 1F
4E 3F 4F 3E
11E 10E 11F 10F
13E 12F 13F 12E
2H 1H 4H 3H
11H 10H 13H 12H

All hardware in the Data Path Test.

TEST DESCRIPTION:

This subtest is similar to the Glitch Data Bits 0-7 except the upper bits are being tested. This subtest checks the Glitch capture feature of the Data boards by enabling the Glitch circuitry which uses the "Set" and "Reset" pins on the 10130's, instead of the "D" inputs to send the Data from the 10121 Multiplexers to the "Q" output. The individual Enable pins on the 10130's are held high so that any "clocking" from the Diagnostic Latch Clock is disabled.

Each output instruction to the Diagnostic bits port 0C6H, latches the Data in the Glitch latches. A Sample Clock is required to send the Data through to the Sample Register. A maximum of two Data values may be output to the Diagnostic bits port before data overrun occurs.

The way that this circuitry is tested, is two consecutive Output instructions are performed with different Data. The first Data is checked at the Sample register after issuing a single Sample Clock. Another Sample Clock presents the Second Data to the Sample Register.

In this test, only Data bits 8-F are in the Glitch Mode. The lower bits 0-7 slip through the 10130's because both of the enable pins are low, so Q follows D.

TEST STEP INFORMATION:

Step	1st Data	2nd Data
1	0000H	------
2	0000H	0000H
3	5500H	0000H
4	AA00H	0000H
5	CC00H	0000H
6	3300H	0000H
7	6600H	0000H
8	9900H	0000H
9	FF00H	0000H

Step	1st Data	2nd Data (Cont'd)
10	0000H	0000H
11	0000H	0000H
12	0000H	0000H
13	0000H	0000H
14	0000H	0000H
15	0000H	0000H
16	0000H	0000H
17	0000H	0000H
18	0100H	0000H
19	0200H	0000H
20	0400H	0000H
21	0800H	0000H
22	1000H	0000H
23	2000H	0000H
24	4000H	0000H
25	8000H	0000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Glitch Data Bits 8-F Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 25.

aaaa is the I/O address of the Data Board:

0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 8

TITLE: PROBES/MULTIPLEX TEST

TARGET LOGIC:

8F
2B 1B 4B 3B 11B 10B 13B 12B
2D 1D 2C 1C 4D 3C 4C 3D
11D 10D 11C 10C 13D 12C 13C 12D

J1, J2, Internal Probe Cables, External Probe Cables

All of the hardware in the Data Path Test.

TEST DESCRIPTION:

This subtest checks the five Multiplexing Select Modes of the Data Board. The five modes are:

1. NORMAL mode. This samples the logic state at the inputs of J1 and J2. This logic state is set high or low by the external probes.

2. DEMUX mode. This is similar to the Normal Mode except the lower eight bits are mirrored into the upper eight bits.

3. DIAGNOSTIC select. This reads the Diagnostic bits Register.

4. MEMORY select. This reads the data that is currently residing in the ECL Memory, (Manual Recirculate).

5. NOTHING SELECTED. With all four select lines disabled, the Data lines should be pulled up to read OFFFFH.

This subtest requires the use of a known good Threshold Board and the installation of the external probes. The Normal Mode and the Demux Mode use the Threshold board to set different thresholds at the hybrid circuit in the probes.

TEST STEP INFORMATION:

Step	Data Expected	Multiplex	Lower Threshold	Upper Threshold
1	FFFFH	Normal	ECL	ECL
2	0000H	Normal	VARIABLE A	VARIABLE A
3	00FFH	Normal	ECL	VARIABLE A
4	FFFFH	Demux	ECL	ECL
5	0000H	Demux	VARIABLE A	VARIABLE A
6	FFFFH	Demux	ECL	VARIABLE A
7	F069H	Diagnostic	----------	----------
8	5AC3H	Memory	----------	----------
9	FFFFH	Floating	----------	----------

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 9.

hmsg is the Error heading message:

Normal ECL Threshold Mux Error,
Normal VARA F Threshold Mux Error,
Normal ECLVARA Threshold Mux Error,
Demux ECL Threshold Mux Error,
Demux VARA F Threshold Mux Error,
Demux ECLVARA Threshold Mux Error,
Diagnostic Select Mux Error,
Memory Select Mux Error,
Multiplexer Disable-Float Error.

aaaa is the I/O address of the Data Board:

0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 9

TITLE: PIPELINES SHIFT TEST

TARGET LOGIC:

2K 1K 3K 11K 12K 13K
2L 1L 3L 4L 10K 11L 12L 13L
5K

Sample Clock P1-42,

Control Clock P1-46, (from Clock Board).

All hardware in Data Path Test.

TEST DESCRIPTION:

This test checks the Data Board Pipeline. The Pipeline consists of a three step FILO, (first in last out), with D latches at each step that can be read. The steps are called the Sample Register, the New Pipe Register, and the Old Pipe Register.

With each Pipeline Clock transition, the Old Pipeline Register Data is lost and receives its new data from the New Pipeline Register. The New Pipeline Register receives its new data from the Sample Register. The Sample Register receives its data from the 10130 Glitch Latches.

The Pipeline can receive it's clocking from either the Sample Clock if Single Phase Mode is selected, or from the Control Clock if Multi Phase Mode is selected. Test Steps 1 - 24 will use the Sample Clock, and Test Steps 25 - 48 will use the Control Clock.

TEST STEP INFORMATION:

Step	Sample Data	New Pipe Data	Old Pipe Data	Mode of Phase
1	0000H	0000H	0000H	Single Phase
2	5555H	0000H	0000H	Single Phase
3	AAAAH	5555H	0000H	Single Phase
4	CCCCH	AAAAH	5555H	Single Phase
5	3333H	CCCCH	AAAAH	Single Phase
6	6666H	3333H	CCCCH	Single Phase
7	9999H	6666H	3333H	Single Phase
8	FFFFH	9999H	6666H	Single Phase
9	0001H	FFFFH	9999H	Single Phase
10	0002H	0001H	FFFFH	Single Phase
11	0004H	0002H	0001H	Single Phase
12	0008H	0004H	0002H	Single Phase
13	0010H	0008H	0004H	Single Phase
14	0020H	0010H	0008H	Single Phase
15	0040H	0020H	0010H	Single Phase
16	0080H	0040H	0020H	Single Phase

Step	Sample Data	New Pipe Data	Old Pipe Data	Mode of Phase(Cont'd)
17	0100H	0080H	0040H	Single Phase
18	0200H	0100H	0080H	Single Phase
19	0400H	0200H	0100H	Single Phase
20	0800H	0400H	0200H	Single Phase
21	1000H	0800H	0400H	Single Phase
22	2000H	1000H	0800H	Single Phase
23	4000H	2000H	1000H	Single Phase
24	8000H	4000H	2000H	Single Phase
25	0000H	0000H	0000H	Multi Phase
26	5555H	0000H	0000H	Multi Phase
27	AAAAH	5555H	0000H	Multi Phase
28	CCCCH	AAAAH	5555H	Multi Phase
29	3333H	CCCCH	AAAAH	Multi Phase
30	6666H	3333H	CCCCH	Multi Phase
31	9999H	6666H	3333H	Multi Phase
32	FFFFH	9999H	6666H	Multi Phase
33	0001H	FFFFH	9999H	Multi Phase
34	0002H	0001H	FFFFH	Multi Phase
35	0004H	0002H	0001H	Multi Phase
36	0008H	0004H	0002H	Multi Phase
37	0010H	0008H	0004H	Multi Phase
38	0020H	0010H	0008H	Multi Phase
39	0040H	0020H	0010H	Multi Phase
40	0080H	0040H	0020H	Multi Phase
41	0100H	0080H	0040H	Multi Phase
42	0200H	0100H	0080H	Multi Phase
43	0400H	0200H	0100H	Multi Phase
44	0800H	0400H	0200H	Multi Phase
45	1000H	0800H	0400H	Multi Phase
46	2000H	1000H	0800H	Multi Phase
47	4000H	2000H	1000H	Multi Phase
48	8000H	4000H	2000H	Multi Phase

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 48.

hmsg is the Error heading message:

Sample Clock: Old Pipe Register Error
Sample Clock: New Pipe Register Error
Sample Clock: Sample Register Error
Control Clock: Old Pipe Register Error
Control Clock: New Pipe Register Error
Control Clock: Sample Register Error

aaaa is the I/O address of the Data Board:

0C2H for Data Board A Old Pipe Register,
0C4H for Data Board A New Pipe Register,
0C6H for Data Board A Sample Register,
0D2H for Data Board B Old Pipe Register,
0D4H for Data Board B New Pipe Register,
0D6H for Data Board B Sample Register,
0E2H for Data Board C Old Pipe Register,
0E4H for Data Board C New Pipe Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a 1. Bits that show up as a 0 passed the compare.

Data Board Diagnostic Subtest 10

TITLE: RAM DATA INTEGRITY TEST

TARGET LOGIC:
6E 6D 7E 7D 8E 8D
5B 5C 6B 6C 8B 8C 9B 9C
5D 5E 9E 9D
5A 6A 8A 9A
6J 5J 5L 8J 4K
6H
All hardware in Data Path Test.

TEST DESCRIPTION:

This test performs a static test of the RAM on the Data boards. This is done using the 24 Data patterns. All 2048 Memory locations are written to with the same data to the same I/O port 0C6H. Since The address counters should be advancing on each Sample Clock, all locations should be written to. This test does not check the addressing uniqueness of each location. It does verify that all Data bits are functional and totally independent of each other.

Prior to this test, the Data path up to the Old Pipe Register has been checked. There are two 10176 "D" latches between the Old Pipe Register and the RAM chip. These latches receive their clock from either WE01/ or WE02/, depending on the current Phase of the clock. The signals WE01/ and WE02 also are the write enables to the RAM chips. So The RAM chips are alternately written to on each Sample Clock.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
2	5555H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
3	AAAAH	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
4	CCCCH	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
5	3333H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
6	6666H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
7	9999H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
8	FFFFH	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
9	0001H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
10	0002H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
11	0004H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
12	0008H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
13	0010H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
14	0020H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
15	0040H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
16	0080H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
17	0100H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
18	0200H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
19	0400H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
20	0800H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
21	1000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
22	2000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
23	4000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
24	8000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
RAM Data Integrity Verify Error
Byte Count      = aaaaH
Data Read       = rrrrH
Data Expected   = eeeeH
Error Bit Map   = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the Address offset for the RAM, in the range of 0 to 1FFH.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is a exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a 1. Bits that show up as a 0 passed the compare.

Data Board Diagnostic Subtest 11

TITLE: RAM ADDRESSING INTEGRITY TEST

TARGET LOGIC:

6E 6D 7E 7D 8E 8D
5B 5C 6B 6C 8B 8C 9B 9C
5D 5E 9E 9D
5A 6A 8A 9A
6J 5J 5L 8J 4K
6H

All hardware in Data Path Test.

TEST DESCRIPTION:

This test writes a unique Data value to each of the 2048 Memory locations. Each memory location should contain unique Data from each other location. The Memory is read back and each location is verified to see if each address is uniquely addressable.

The Data that is written is an incrementing pattern. The first test step starts with a value of 0001H for the first location, and the sequential locations are written to with a 0002H, 0003H, etc.

The second Test step is similar to the first, except the starting Data value is a 0002H. Subsequent test steps shift this Data value left, so that the starting Data values for the 16 test steps are:

TEST STEP INFORMATION:

Step	Start Data	Data Written to	Data Verified at
1	0001H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
2	0002H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
3	0004H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
4	0008H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
5	0010H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
6	0020H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
7	0040H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
8	0080H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
9	0100H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
10	0200H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
11	0400H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
12	0800H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
13	1000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
14	2000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
15	4000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
16	8000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
RAM Address Unique Error
Byte Count       = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 16.

aaaa is the Address offset for the RAM, in the range of 0 to 1FFH.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a 1. Bits that show up as a 0 passed the compare.

Data Board Diagnostic Subtest 12

TITLE: TRACE CONDITIONS TEST

TARGET LOGIC:

8J 8H
6H 6L 9H
12M 13M 3M 11M 10M

TRACED/ Signal P2-56 from Control Board
ARMED Signal P2-58 from Control Board

TEST DESCRIPTION:

This test uses the Control Board to provide Trace Conditions that exist on the Data Board. These are mainly ARMED and TRACED/. This test is similar to the Force Conditions Test.

TEST STEP INFORMATION:

Step	Status Expected
1	45H
2	C5H
3	72H
4	71H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Trace Conditions Error
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 4.

aaaa is the I/O address of the Data Board:

0C8H for Data Board A Status Register,
0D8H for Data Board B Status Register,
0E8H for Data Board C Status Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a 1. Bits that show up as a 0 passed the compare.

Data Board Diagnostic Subtest 13

TITLE: RECIRCULATE RAM TEST

TARGET LOGIC:

The main hardware being tested is the feed back loop of the 10173 Multiplexers 5D, 5E, 9E and 9D, to the 10121 Multiplexers with Memory Select Enabled.

The entire Data Path and most of the Control Logic must be fuctional for this test to pass.

TEST DESCRIPTION:

The contents of the ECL RAM is recirculated out of the RAM through the Multiplexers, through the Glitch Latches, through the Sample Register, through the New Pipe Register, through the Old Pipe Register, through the RAM latch and back into the ECL RAM. All of the clocking is done by the Clock board and the Control Board.

There is a time-out counter on the recirculation, and after the recirculation is completed, the Data in the ECL RAM should be the same as before.

TEST STEP INFORMATION:

Step	Status Expected	Clock Time Out
1	8000H	10 usec
3	8000H	20 usec
5	8000H	30 usec

Step	Data Expected
2	0000H - 01FFH (incrementing pattern)
4	0000H - 01FFH (incrementing pattern)
6	0000H - 01FFH (incrementing pattern)

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

ERROR MESSAGES: (Cont'd)

Where:

ssss is the test step number in the range of 1 to 6.

hmsg is the Error heading message:

Recirculation Time out-10us clock,
Recirculation Error-10us clock,
Recirculation Time out-20us clock,
Recirculation Error-20us clock,
Recirculation Time out-30us clock,
Recirculation Error-30us clock.

aaaa is the I/O address of the Data Board:

0C0H for Data Board A RAM,
0D0H for Data Board B RAM,
0E0H for Data Board C RAM,
0F0H for Control Board Status.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a 1. Bits that show up as a 0 passed the compare.

K450 CONTROL BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes the subtests that are performed by the K450 Control Board Diagnostic. The target hardware is presented, as well as a general description of each subtest, a list of information for each test step, and a description of Error Messages that may be printed for the subtest results. The Control Board Diagnostic is divided into 12 subtests, each of which is described individually on the following pages.

Subtest 1 is a Force Conditions test, subtest 2 is an Advance RAM Forward and Jump RAM backward test, subtest 3 and 4 are Detection RAMs Data and Address integrity test, subtest 5 and 6 are Delay Control RAM Data and Address integrity test, subtest 7 and 8 are Delay RAMs Data and Address integrity test, subtest 9 is Delay Counter test, subtest 10 is Relation Logic test, subtest 11 and 12 are Selection RAMs data and Address integrity test. Subtests 1, 2, and 3 require Data Boards A, B, and C installed in the system.

The external signals through mother board to the Data Boards are checked by subtest 1, the external signals through connector J1 to the Clock Board are checked by subtest 2.

NOTE: The TARGET LOGIC listed in each subtest description does not necessarily include all of the logic which could affect the operation of the subtest.

SUBTEST CATEGORY

1. Force Condition Test
2. Advance and Jump RAM Test
3. Detection RAMs Data Integrity Test
4. Detection RAMs Address Integrity Test
5. Delay Control RAM Data Integrity Test
6. Delay Control Ram Address Integrity Test
7. Delay RAMs Data Integrity Test
8. Delay RAMs Address Integrity Test
9. Delay Counter Test
10. Relation Logic Test
11. Selection RAMss Data Integrity Test
12. Selection RAMs Address Integrity Test

ERROR COUNT CATEGORY

1. Subtest 1 Error Count
2. Subtest 2 Error Count
3. Subtest 3 Error Count
4. Subtest 4 Error Count
5. Subtest 5 Error Count
6. Subtest 6 Error Count
7. Subtest 7 Error Count
8. Subtest 8 Error Count
9. Subtest 9 Error Count
10. Subtest 10 Error Count
11. Subtest 11 Error Count
12. Subtest 12 Error Count

Control Board Diagnostic Subtest 1

TITLE: FORCE CONDITION TEST

TARGET LOGIC: 6A, 7A, 5A, 4A, 11A, 5F, 7D, 5C, 5D, 7C, 4D, 8D, 1C, 3C, 8C, 9C, 5G, 11G, 4J, 12C, 14B, 12A, 12F, and 5K, 8J, 8H, 6H of DATA BOARD A, B, and C

TEST DESCRIPTION:

The force condition is functionally tested by forcing the desired condition true. The condition is then verified by reading back the corresponding status bit.

There are seven force condition tests included. Condition 0 is force level 0. Condition 1 is force jump and jump not. Condition 2 is force trace and trace not. Condition 3 is force stop and stop not. Condition 4 is force event and advance. Condition 5 is force stopped and armed. Condition 6 is force manual advance.

Condition 2 also verifies the TRACED signal can propagate through the mother board to data boards A, B, and C. Condition 5 also verifies the MEM. ARMED signal can propagate through the mother board to data boards A, B, and C.

TEST STEP INFORMATION:

Test Step	Condition Tested	Signals in schematics
1	force level 0	'FORCE LEVEL=0'
2	force jump and jump not	'FORCE JUMP','FORCE JUMP/'
3	force trace and trace not	'FORCE TRACE','FORCE TRACE/'
4.	force stop and stop not	'FORCE STOP','FORCE STOP/'
5.	force event and advance	'FORCE EVENT AND ADVANCE'
6.	force stopped and armed	'CYCLE RESET'
7.	force manual advance	'ENABLE MANUAL ADVANCE'

ERROR MESSAGES:

1. If error condition 0 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force Level 0
Level Expected = eeH
Level Read     = rrH

Where zz should be 01

ee should be 00 through 0F

rr should be 00 through 0F
```

2. If error condition 1 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force JUMP & JUMP NOT
Jump Expected = e
Jump Read     = r

Where zz should be 02

e should be 0 or 1

r should be 0 or 1
```

3. If error condition 2 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force TRACE & TRACE NOT
Trace Expected        = e
Trace Read            = r
Old Traced A Expected = a
Old Traced A Read     = t
Old Traced B Expected = b
Old Traced B Read     = u
Old Traced C Expected = c
Old Traced C Read     = v

Where zz should be 03

e, r, a, t, b, u, c, v should be 0 or 1
```

4. If error condition 3 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force STOP & STOP NOT
Stop Expected = e
Stop Read     = r

Where zz should be 04

e should be 0 or 1

r should be 0 or 1
```

5. If error condition 4 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force EVENT & ADVANCE
Event Expected   = e
Event Read       = r
Advance Expected = p
Advance Read     = d
```

Where zz should be 05

e, r, p, d should be 0 or 1

6. If error condition 5 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force STOPPED & ARMED
Stopped Expected      = e
Stopped/ Read         = r
Armed Expected        = p
Armed/ Read           = d
Mem. Armed A Expected = a
Mem. Armed A Read     = t
Mem. Armed B Expected = b
Mem. Armed B Read     = u
Mem. Armed C Expected = c
Mem. Armed C Read     = v
```

Where zz should be 06

e, r, p, d, a, t, b, u, c, v should be 0 or 1

7. If error condition 6 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force MANUAL ADVANCE
Advance Expected        = e
AdvancE Read            = r
Manual Advance Expected = p
Man. Advance Read       = d
```

Where zz should be 07

e, r, p, d should be 0 or 1

Control Board Diagnostic Subtest 2

TITLE: ADVANCE AND JUMP RAM TEST

TARGET LOGIC: 5H, 5J, 5G, 11G, 12F, 11F, and level memory logic in the clock board, connector J1 included.

TEST DESCRIPTION:

The advance and jump RAMs are functionally tested by advancing the Advance RAM to the next level and restoring the jump RAM backward to a previous level. The RAM data is then verified by reading back the level and comparing the result to the expected level.

TEST STEP INFORMATION:

Test Step	RAM Tested	Level Tested	Expected Level
1 through 16	advance	00H through 0FH	Level tested + 1
17 through 32	jump	00H through 0FH	Level tested - 1

ERROR MESSAGE:

1. If an error of Advance RAM occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Adv. RAM Advancing Test
Adv. RAM Level at       = llH
Adv. RAM Data Expected = eeH
Adv. RAM Data Read      = rrH
Error Bit Map           = xxxxxxxxB
Ext. Level Expected     = ppH
Ext. Level Read         = qqH
Error Bit Map           = yyyyyyyyB
```

Where zz should be 01 through 16

ll should be 00 through 0F

ee should be 00 through 0F

rr should be 00 through 0F

pp should be 00 through 0F

qq should be 00 through 0F

xxxxxxxx should be 00000000 through 00001111

yyyyyyyy should be 00000000 through 00001111

ERROR MESSAGE (Cont'd)

2. If an error of Jump RAM occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Jump RAM Advancing Test
Jump RAM Level at = llH
Jump RAM Data Expected = eeH
Jump RAM Data Read = rrH
```

Where zz should be 17 through 32

ll should be 00 through 0F

ee should be 00 through 0F

rr should be 00 through 0F

Control Board Diagnostic Subtest 3

TITLE: DETECTION RAM DATA INTEGRITY TEST

TARGET LOGIC:

8G, 8F, 9G, 9F, 8D, 9D
4G, 4F, 7G, 7F, 3D, 4D, 7D
1G, 1F, 3G, 3F, 1D, 3D
2J, 6B, 5B, 4B, 7B, 8B, 1B, 2B, 3B, 8A, 9A
5D, 5C, 7C, 4D, 5F, 3C, 1C, 8C, 9C, 9B
12C, 12G, 12H

TEST DESCRIPTION:

The detection RAMs data integrity is functionally tested by writing a four bits nibble into each RAM, the RAM data is then verified by reading the (ADVANCE,JUMP,STOP,TRACE) nibble and comparing the result to the expected nibble.

The nibble patterns tested are:

1010B, 0101B, 1100B, 0011B, 0001B, 0010B, 0100B, 1000B.

The detection RAMs tested are:

8G, 8F, 9G, 9F, 4G, 4F, 7G, 7F, 1G, 1F, 3G, 3F.

TEST STEP INFORMATION:

Test Step	RAM Chip Location	Nibble Patterns
01 through 08	8G(00)	1010,0101,1100,0011,0001,0010,0100,1000
09 through 16	8F(01)	1010,0101,1100,0011,0001,0010,0100,1000
17 through 24	9G(02)	1010,0101,1100,0011,0001,0010,0100,1000
25 through 32	9F(03)	1010,0101,1100,0011,0001,0010,0100,1000
33 through 40	4G(04)	1010,0101,1100,0011,0001,0010,0100,1000
41 through 48	4F(05)	1010,0101,1100,0011,0001,0010,0100,1000
49 through 56	7G(06)	1010,0101,1100,0011,0001,0010,0100,1000
57 through 64	7F(07)	1010,0101,1100,0011,0001,0010,0100,1000
65 through 72	1G(08)	1010,0101,1100,0011,0001,0010,0100,1000
73 through 80	1F(09)	1010,0101,1100,0011,0001,0010,0100,1000
81 through 88	3G(10)	1010,0101,1100,0011,0001,0010,0100,1000
89 through 96	3F(11)	1010,0101,1100,0011,0001,0010,0100,1000

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Detection RAMs Data Integrity Test
RAM chip location      = cc
Detect Address         = ddH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read      = rrH
Error Bit Map          = xxxxxxxxB
```

Where cc should be 00 through 11

dd should be 00 through FF

nn should be 0A,05,0C,03,01,02,04,08

rr should be 00 through FF

xxxxxxxx should be 00000000 through 00001111

NOTE: AJST is the abbreviation of ADVANCE, JUMP, STOP, TRACE nibble.

Control Board Diagnostic Subtest 4

TITLE: DETECTION RAM ADDRESS INTEGRITY TEST

TARGET LOGIC: 1H, 2H, 3H, 4H, 6H, 7H, 8H, 9H,
8G, 8F, 9G, 9F,
4G, 4F, 7G, 7F,
1G, 1F, 3G, 3F,

TEST DESCRIPTION:

The detection RAMs address integrity is functionally tested by clearing all locations of each RAM, then writing a 4 bits nibble (1010B) into the asserted address. The RAM address is then verified by reading the (ADVANCE, JUMP, STOP, TRACE) nibble from all locations and comparing the result to the nibble 0AH.

The detection RAMs tested are:

8G, 8F, 9G, 9F, 4G, 4F, 7G, 7F, 1G, 1F, 3G and 3F.

There are 8 address bits for each detection RAM, consisting of low nibble from levels and high nibble from sample registers of Data Boards.

TEST STEP INFORMATION:

Test Step	RAM Chip Location	Asserted Address Bit
1 through 8	8G(00)	01H,02H,04H,08H,10H,20H,40H,80H
9 through 16	8F(01)	01H,02H,04H,08H,10H,20H,40H,80H
17 through 24	9G(02)	01H,02H,04H,08H,10H,20H,40H,80H
25 through 32	9F(03)	01H,02H,04H,08H,10H,20H,40H,80H
33 through 40	4G(04)	01H,02H,04H,08H,10H,20H,40H,80H
41 through 48	4F(05)	01H,02H,04H,08H,10H,20H,40H,80H
49 through 56	7G(06)	01H,02H,04H,08H,10H,20H,40H,80H
57 through 64	7F(07)	01H,02H,04H,08H,10H,20H,40H,80H
65 through 72	1G(08)	01H,02H,04H,08H,10H,20H,40H,80H
73 through 80	1F(09)	01H,02H,04H,08H,10H,20H,40H,80H
81 through 88	3G(10)	01H,02H,04H,08H,10H,20H,40H,80H
89 through 96	3F(11)	01H,02H,04H,08H,10H,20H,40H,80H

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Detection RAMs Address Integrity Test
RAM Chip Location      = cc
High Nibble Related to Data Board B
Address Expected       = ddH
Address Found          = ffH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read      = rrH

Where cc should be 00 through 11

b should be A,B,C

dd should be 00 through FF

ff should be 00 through FF

nn should be 0A,05,0C,03,01,02,04,08

rr should be 00 through FF
```

NOTE: AJST is the abbreviation of ADVANCE, JUMP, STOP, TRACE nibble.

Control Board Diagnostic Subtest 5

TITLE: DELAY CONTROL RAM DATA INTEGRITY TEST

TARGET LOGIC: 13A, 12C, 12G, 12H

TEST DESCRIPTION:

The Delay Control RAM data integrity is functionally tested by writing a four bits nibble into the delay control RAM, the RAM data is then verified by reading the (EVENT MODE, END LEVEL, (D=1 IF JUMP)/, (D=1 IF ADVANCE)/) nibble from bit 14 of port 0FEH, 0FCH, 0FAH, 0F8H and compare the result to the nibble written.

There are 8 nibble patterns as follows:

1010B, 0101B, 1100B, 0011B, 0001B, 0010B, 0100B, 1000B

TEST STEP INFORMATION:

Test Step	Nibble Pattern	Levels
1	1010B	0 through 0FH
2	0101B	0 through 0FH
3	1100B	0 through 0FH
4	0011B	0 through 0FH
5	0001B	0 through 0FH
6	0010B	0 through 0FH
7	0100B	0 through 0FH
8	1000B	0 through 0FH

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED -- Test Step  zz
Delay control RAM Data Integrity Test
RAM Address      = aaH
Nibble Expected = eeH
Nibble Read      = rrH
Error Bit Map    = xxxxxxxxB

Where aa should be 00 through 0F

ee should be 0A,05,0C,03,01,02,04,08

rr should be 00 through 0F

xxxxxxxx should be 00000000 through 00001111
```

Control Board Diagnostic Subtest 6

TITLE: DELAY CONTROL RAM ADDRESS INTEGRITY TEST

TARGET LOGIC: 13A, 12C, 12G, 12H

TEST DESCRIPTION:

The Delay Control RAM address integrity is functionally tested by writing a four bits nibble (1010B) into the asserted address. The address is then verified by reading nibble data from all 16 locations,and comparing the result to the nibble expected (1010B).

TEST STEP INFORMATION:

Test Step	Nibble Pattern	Asserted Address
1	1010B	0001B
2	1010B	0010B
3	1010B	0100B
4	1010B	1000B

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay control RAM Address Integrity test
Address Expected = eeH
Address Found    = ffH
Nibble Expected  = nnH
Nibble Read      = rrH
```

Where zz should be 1 through 4

ee should be 01,02,04,08

ff should be 00 through FF

nn should be 0A.

rr should be 00 through 0F

Control Board Diagnostic Subtest 7

TITLE: DELAY RAMS DATA INTEGRITY TEST

TARGET LOGIC: 14C, 14D, 14E, 14F, 13C, 13D, 13E, 13F
11C, 11B, 12D, 12E, 12G, 12H

TEST DESCRIPTION:

The Delay RAMs data integrity is functionally tested by writing a word pattern into the delay RAMs. The word data of RAMs is then loaded into the delay counter. The data integrity is then verified by reading the word data and comparing the result to the word expected.

There are 8 delay word patterns tested as follows:

AAAAH, 5555H, CCCCH, 3333H, 1111H, 2222H, 4444H, 8888H.

TEST STEP INFORMATION:

Test Step	Word Pattern Tested
1	AAAAH
2	5555H
3	CCCCH
4	3333H
5	1111H
6	2222H
7	4444H
8	8888H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay RAM Data Integrity Test
RAM Address    = aaH
Word Expected = eeeeH
Word Read      = rrrrH
Error Bit Map = xxxxxxxxxxxxxxxxB
```

Where zz should be 1 through 8.

aa should be 00 through 0F

eeee should be AAAA,5555,CCCC,3333,1111,2222,4444,8888

rrrr should be 0000 through FFFF

xxxxxxxxxxxxxxxx should be 0000000000000000 through 1111111111111111

Control Board Diagnostic Subtest 8

TITLE: DELAY RAMS ADDRESS INTEGRITY TEST

TARGET LOGIC: 14C, 14D, 14E, 14F, 13C, 13D, 13E, 13F
11C, 11B, 12D, 12E, 12G, 12H

TEST DESCRIPTION:

The Delay RAMs address integrity is functionally tested by writing a word (0AAAAH) into the asserted level address. The delay RAM is then loaded into the delay counter, and the address integrity is verified by reading the delay count from all level addresses and comparing the result to the word 0AAAAH.

There are 4 address bits tested are:

0001B, 0010B, 0100B, 1000B

TEST STEP INFORMATION:

Test Step	Word Pattern Tested	Asserted Level Address
1	AAAAH	0001B
2	AAAAH	0010B
3	AAAAH	0100B
4	AAAAH	1000B

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay RAM Address Integrity Test
Address Expected = aaH
Address Found    = ffH
Word Expected    = eeeeH
Word Read        = rrrrH
```

Where zz should be 1 through 4.

aa should be 01,02,04,08

ff should be 00 through 0F

eeee should be AAAA.

rrrr should be 0000 through FFFF

Control Board Diagnostic Subtest 9

TITLE: DELAY COUNTER TEST

TARGET LOGIC: 14C, 14D, 14E, 14F, 13C, 13D, 13E, 13F
11C, 11B, 12D, 12E, 12G, 12H

TEST DESCRIPTION:

The Delay Counter is functionally tested by writing a delay word into the delay RAMs and loading it into the delay counter. The counting operation is then verified by kicking clocks, reading the delay count and comparing the result to the word expected.

The counting operation is verified by the following two methods:

1. Kick clocks until delay count is equal to 0.

2. Kick a clock to increment only one count.

The delay count word patterns being tested are as follows:

8000H, 4000H, 2000H, 1000H, 0800H, 0400H, 0200H, 0100H,

0080H, 0040H, 0020H, 0010H, 0008H, 0004H, 0002H, 0001H.

TEST STEP INFORMATION:

Test Step	Word Pattern Tested	Clocks to Kick	Expected Count
1	8000H	8000H	0
2	8000H	1	8001H
3	4000H	C000H	0
4	4000H	1	4001H
5	2000H	E000H	0
6	2000H	1	2001H
7	1000H	F000H	0
8	1000H	1	1001H
9	0800H	F800H	0
10	0800H	1	0801H
11	0400H	FC00H	0
12	0400H	1	0401H
13	0200H	FE00H	0
14	0200H	1	0201H
15	0100H	FF00H	0
16	0100H	1	0101H
17	0080H	FF80H	0
18	0080H	1	0081H
19	0040H	FFC0H	0
02	0040H	1	0041H
21	0020H	FFE0H	0
22	0020H	1	0021H
23	0010H	FFF0H	0
24	0010H	1	0011H

Test Step (Cont'd)	Word Pattern Tested	Clocks to Kick	Expected Count
25	0008H	FFF8H	0
26	0008H	1	0009H
27	0004H	FFFCH	0
28	0004H	1	0005H
29	0002H	FFFEH	0
30	0002H	1	0003H
31	0001H	FFFFH	0
32	0001H	1	0002H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay Counting Operation Test
Count Pattern  = ccccH
Count Expected = eeeeH
Count Read     = rrrrH
Error Bit Map  = xxxxxxxxxxxxxxxxB
```

Where zz should be 1 through 32

cccc should be 8000, 4000, 2000, 1000, 0800, 0400
0200, 0100, 0080, 0040, 0020, 0010
0008, 0004, 0002, 0001

eeee should be 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100
0080, 0040, 0020, 0010, 0008, 0004, 0002, 0001, 0

rrrr should be 0000 through FFFF

xxxxxxxxxxxxxxxx should be 0000000000000000 through 1111111111111111

Control Board Diagnostic Subtest 10

TITLE: RELATION LOGIC TEST

TARGET LOGIC: 12B, 14B, 12A, 13A, 11A, 11F, 11C, 11B, 11D, 9B, 12F

TEST DESCRIPTION:

The Relation Logic is functionally tested by making one of the logic paths true. The relation is then verified by reading the desired relation bit and comparing the result to the expected logic state.

The Boolean function of each logic path is:

```
Path 1 : P1 = (old T < D)*(advanced + jumped)*(evented)*(TC)
Path 2 : P2 = (jumped)*(D = 1 If Jumped)
Path 3 : P3 = (advanced)*(D = 1 If advanced)*(jumped /)
Path 4 : P4 = (old T = D)*(evented /)*((advanced + jumped) /)
Path 5 : P5 = (old T = D)*(evented)*((advanced + jumped) /)
Path 6 : P6 = (old T > D)*((advanced + jumped) /)
(T < D) = NOT (P1 + P2 + P3 + P4 + P5)
(T = D) = P1 + P2 + P3 + P4
(T > D) = P5 + P6
Path 0 logic means T < D true.
```

TEST STEP INFORMATION

Test Step	Logic Path	Relation True
1	0, 1	T < D then T = D
2	2	T = D
3	3	T = D
4	4, 5, 6	T = D then T > D

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
Relation Logic Path p Failed
"T < D" Expected = a
"T < D" Read     = b
"T = D" Expected = c
"T = D" Read     = d
"T > D" Expected = e
"T > D" Read     = f
```

Where zz should be 1 through 4.

a, b, c, d, e, f should be 0 or 1.

Control Board Diagnostic Subtest 11

TITLE: SELECTION RAM DATA INTEGRITY TEST

TARGET LOGIC: 6B, 5B, 4B, 7B, 8B, 1B, 2B, 3B, 8A, 9A, 5C, 5D, 7C, 4D, 8D, 5F, 7D, 1C, 3C, 8C, 9C, 3D, 9B

TEST DESCRIPTION:

The Selection RAMs data integrity is functionally tested by separating all RAMs into 4 subgroups (ADVANCE, JUMP, STOP, TRACE), writing the specified data into the RAMS of each subgroup, and verifying the data integrity by reading the (ADVANCE, JUMP, STOP, TRACE) bits and comparing the result to the nibble expected.

There are 4 subgroups as follows, being tested:

Subgroup A : bit 0 -- selection bit for ADVANCE A
bit 1 -- selection bit for ADVANCE B
bit 2 -- selection bit for ADVANCE C
bit 3 -- selection bit for (ADVANCE C.B.A)/
bit 4 -- selection bit for ADVANCE if T > D
bit 5 -- selection bit for ADVANCE if T = D
bit 6 -- selection bit for ADVANCE if T < D
bit 7 -- selection bit for ADVANCE if 'x'

Subgroup J : bit 0 -- selection bit for JUMP A
bit 1 -- selection bit for JUMP B
bit 2 -- selection bit for JUMP C
bit 3 -- selection bit for (JUMP C.B.A)/
bit 4 -- selection bit for JUMP if T > D
bit 5 -- selection bit for JUMP if T = D
bit 6 -- selection bit for JUMP if T < D

Subgroup S : bit 0 -- selection bit for STOP A
bit 1 -- selection bit for STOP B
bit 2 -- selection bit for STOP C
bit 3 -- selection bit for (STOP C.B.A)/
bit 4 -- selection bit for STOP if T > D
bit 5 -- selection bit for STOP if T = D
bit 6 -- selection bit for STOP if T < D
bit 7 -- selection bit for STOP if 'x'

Subgroup T : bit 0 -- selection bit for TRACE A
bit 1 -- selection bit for TRACE B
bit 2 -- selection bit for TRACE C
bit 3 -- selection bit for (TRACE C.B.A)/
bit 4 -- selection bit for TRACE if T > D
bit 5 -- selection bit for TRACE if T = D
bit 6 -- selection bit for TRACE if T < D
bit 7 -- selection bit for TRACE if 'x'

Each bit has logic 0 and logic 1 to be tested.

TEST STEP INFORMATION:

Test Step	Subgroup	Bit	Mnemonic	Logic State	Related Chip
1	Advance	0	ADVANCE A	0	4B-D3
2	Advance	0	ADVANCE A	1	4B-D3
3	Advance	1	ADVANCE B	0	5B-D2
4	Advance	1	ADVANCE B	1	5B-D2
5	Advance	2	ADVANCE C	0	5B-D3
6	Advance	2	ADVANCE C	1	5B-D3
7	Advance	3	(ADVANCE C.B.A)/	0	5B-D1
8	Advance	3	(ADVANCE C.B.A)/	1	5B-D1
9	Advance	4	ADVANCE if T > D	0	6B-D2
10	Advance	4	ADVANCE if T > D	1	6B-D2
11	Advance	5	ADVANCE if T = D	0	6B-D0
12	Advance	5	ADVANCE if T = D	1	6B-D0
13	Advance	6	ADVANCE if T < D	0	6B-D3
14	Advance	6	ADVANCE if T < D	1	6B-D3
15	Advance	7	ADVANCE if 'x'	0	6B-D1
16	Advance	7	ADVANCE if 'x'	1	6B-D1
17	Jump	0	Jump A	0	8B-D2
18	Jump	0	Jump A	1	8B-D2
19	Jump	1	Jump B	0	8B-D3
20	Jump	1	Jump B	1	8B-D3
21	Jump	2	Jump C	0	4B-D0
22	Jump	2	Jump C	1	4B-D0
23	Jump	3	(Jump C.B.A)/	0	4B-D2
24	Jump	3	(Jump C.B.A)/	1	4B-D2
25	Jump	4	Jump if T > D	0	7B-D3
26	Jump	4	Jump if T > D	1	7B-D3
27	Jump	5	Jump if T = D	0	7B-D1
28	Jump	5	Jump if T = D	1	7B-D1
29	Jump	6	Jump if T < D	0	7B-D2
30	Jump	6	Jump if T < D	1	7B-D2
31	Jump	7	None	x -	None
32	Jump	7	None	x	None
33	Stop	0	Stop A	0	3B-D2
34	Stop	0	Stop A	1	3B-D2
35	Stop	1	Stop B	0	2B-D0
36	Stop	1	Stop B	1	2B-D0
37	Stop	2	Stop C	0	2B-D2
38	Stop	2	Stop C	1	2B-D2
39	Stop	3	(Stop C.B.A)/	0	1B-D1
40	Stop	3	(Stop C.B.A)/	1	1B-D1
41	Stop	4	Stop if T > D	0	1B-D0
42	Stop	4	Stop if T > D	1	1B-D0
43	Stop	5	Stop if T = D	0	1B-D3
44	Stop	5	Stop if T = D	1	1B-D3
45	Stop	6	Stop if T < D	0	1B-D2
46	Stop	6	Stop if T < D	1	1B-D2
47	Stop	7	Stop if 'x'	0	2B-D3
48	Stop	7	Stop if 'x'	1	2B-D3
49	Trace	0	Trace A	0	9A-D0
50	Trace	0	Trace A	1	9A-D0
51	Trace	1	Trace B	0	8A-D2
52	Trace	1	Trace B	1	8A-D2

53	Trace	2	Trace C	0	8A-D0
54	Trace	2	Trace C	1	8A-D0
55	Trace	3	(Trace C.B.A)/	0	8A-D1
56	Trace	3	(Trace C.B.A)/	1	8A-D1
57	Trace	4	Trace if T > D	0	9A-D2
58	Trace	4	Trace if T > D	1	9A-D2
59	Trace	5	Trace if T = D	0	9A-D3
60	Trace	5	Trace if T = D	1	9A-D3
61	Trace	6	Trace if T < D	0	3B-D0
62	Trace	6	Trace if T < D	1	3B-D0
63	Trace	7	Trace if'x'	0	3B-D1
64	Trace	7	Trace if'x'	1	3B-D1

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Selection RAMs Data Integrity
Subgroup g Bit b Testing
RAM Address = aaH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read = rrH
Error Bit Map = xxxxxxxxB
```

Where zz should be 1 through 64

g should be A, J, S, T.

b should be 0 or 1.

aa should be 00 through 0F.

nn should be 08, 04, 02, 01, 0

rr should be 00 through 0F

xxxxxxxx should be 00000000 through 00001111

Control Board Diagnostic Subtest 12

TITLE: SELECTION RAM ADDRESS INTEGRITY TEST

TARGET LOGIC: 6B, 5B, 4B, 7B, 8B, 1B, 2B, 3B, 8A, 9A, 5C, 5D, 7C, 4D, 8D, 5F, 7D, 1C, 3C, 8C, 9C, 3D, 9B

TEST DESCRIPTION:

The Selection RAMs address integrity is functionally tested by separating all RAMs into 4 subgroups (ADVANCE, JUMP, STOP, TRACE), clearing all locations of selection RAMs, going to the asserted level address, and writing bit 0 into the RAMS of each subgroup. The address integrity is then verified by reading the (ADVANCE, JUMP, STOP, TRACE) bits from all locations.

There are 4 subgroups as follows, being tested:

Subgroup A : bit 0 -- selection bit for ADVANCE A
Subgroup J : bit 0 -- selection bit for JUMP A
Subgroup S : bit 0 -- selection bit for STOP A
Subgroup T : bit 0 -- selection bit for TRACE A

Each bit only test logic 0.

TEST STEP INFORMATION:

Test Step	Subgroup	Bit	Mnemonic	Logic State	Level Address
1	Advance	0	ADVANCE A	0	01H
2	Advance	0	ADVANCE A	0	02H
3	Advance	0	ADVANCE A	0	04H
4	Advance	0	ADVANCE A	0	08H
5	Jump	0	JUMP A	0	01H
6	Jump	0	JUMP A	0	02H
7	Jump	0	JUMP A	0	04H
8	Jump	0	JUMP A	0	08H
9	Stop	0	STOP A	0	01H
10	Stop	0	STOP A	0	02H
11	Stop	0	STOP A	0	04H
12	Stop	0	STOP A	0	08H
13	TRACE	0	TRACE A	0	01H
14	TRACE	0	TRACE A	0	02H
15	TRACE	0	TRACE A	0	04H
16	TRACE	0	TRACE A	0	08H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Selection RAMs Address Integrity
Subgroup g Testing
Address Expected       = eeH
Address Found          = ffH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read      = rrH
```

Where zz should be 1 through 16

g should be A, J, S, T.

ee should be 01, 02, 04, 08

ff should be 00 through 0F

nn should be 08, 04, 02, 01

rr should be 00 through 0F

K450 CLOCK BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes subtests that are performed by the K450 Clock Board Diagnostic. The target hardware is presented, as well as a general description of each Subtest, a list of information for each Test Step, and Error Messages that may be printed.

The K450 Clock Board Diagnostic is a board level Diagnostic which runs under the K450 Diagnostic Operating System. The Diagnostic verifies all functions of the Clock Board except for J2, which presents clocks to the front panel. The hardware that is not tested is a 4028 Multiplexer/Driver at 9B, two drivers at 10B, and the cable going to the front panel.

The Diagnostic Tests that are performed can be divided into five sections as described below.

The first is the Force Conditions Test. This test is a series of simple I/O operations that are performed on the Clock Board.

The second is the Sample and Control Clock testing. These clocks move data on the Data Boards. Specifically, the Sample Clock clocks the Data Board's Sample Registers, and the Control Clock clocks the Data Board's Pipeline.

The third is the Latch Clock testing. The Latch Clocks also clock data on the Data Boards, but in a special latch mode where data is latched before it reaches the Data Board's Sample Registers.

The fourth is the Frequency testing. All seven decades from the 100Mhz Clock, down to the 100 Hz Clock are tested. The Clock Board Multiplier is tested to see if it can actually perform a divide by function, thus slowing down the clock rate.

The fifth and final is the testing of the Level RAM. The RAM is tested for Data integrity, Addressing integrity, and control logic functionality.

The Diagnostic uses Data Boards A, B and C extensively to check out the clocking features. The Diagnostic also requires the use of the Control Board and the Threshold Board. All of these boards must be functional for any realistic pinpointing of possible failures. All six of the external probes must be installed, with floating inputs (no connection).

If Data Board C is not installed, (unit contains 32 input channels), the C section clocks of the Clock Board is not tested, and the following message is displayed:

>Testing sections A & B, cannot test section C.

This message informs the operator that the A and B sections are being tested, but there is insufficient hardware in the system to diagnose section C. All six probes must still be installed to properly test sections A and B.

The type of tests that are performed on the Clock Board are static type tests.

The tests verify the functionality and individuality of multiplexers and gates but do not perform real time testing on the board. Therefore, if racing conditions exist, or if problems occur with propagation delays, the Diagnostic will probably not detect them.

Also, the frequency test that is performed on the Clock Decades is a ballpark test, and does not verify that the 100 Mhz source clock is exactly 100.00 Mhz. This must be adjusted/verified with a scope or frequency counter.

The Clock Board provides very little status information to monitor the Modes or selections. Of the 133 Command Output Bits, the Clock board only provides 4 Status Input Bits.

If multiple failures exist on a board under test, the problem might originate in the I/O port decoding and data latching. This portion of the board is initially assumed to be functional. If it is not funtional, very few if any tests will pass.

DESCRIPTION OF DATA BOARD REGISTERS USED TO TEST CLOCK BOARD

The Sample Clocks, Latch Clocks and Control Clocks are tested using the K450 Data Boards. The Data Boards are also used for the Frequency tests.

A simple outline of the registers on the Data Boards is as follows:

1. Data Boards Diagnostic Latch Register.

   Data Board A - Write Port 0C0H. (cannot read this port back)
   Data Board B - Write Port 0D0H. (cannot read this port back)
   Data Board C - Write Port 0E0H. (cannot read this port back)

   This Latch is the "Front End" to the Data Board's Data Path. Data is placed in this register by simply performing an OUTWORD instruction.

2. Data Boards Sample Registers.

   Data Board A - Read Port 0C6H. (cannot write directly to this port)
   Data Board B - Read Port 0D6H. (cannot write directly to this port)
   Data Board C - Read Port 0E6H. (cannot write directly to this port)

   Data is transfered from the Data Board's Diagnostic Latch Registers to the Data Board's Sample Register when a Sample Clock is issued. Sample Register A requires Sample Clock A, Sample Register B requires Sample Clock B, and Sample Register C requires Sample Clock C. This transfer takes place assuming the Data Board is not in Latch mode.

3. Data Boards New Pipe Registers.

   Data Board A - Read Port 0C4H. (cannot write directly to this port)
   Data Board B - Read Port 0D4H. (cannot write directly to this port)
   Data Board C - Read Port 0D4H. (cannot write directly to this port)

   Data is transferred from the Data Boards Sample Registers to the Data Boards New Pipe Registers when a Control Clock is issued.

Data Boards A, B and C all use a single Control Clock for transfer.

4. Latch Mode on the Data Boards.

   When the Data Boards are in Latch Mode, an extra Data latch is present between the Diagnostic Latch Registers and the Sample Registers. A Latch Clock is required to transfer Data.

   In Latch Mode, the following sequence is required to place Data into the Data Board's Sample Registers.

   Output the desired Data to the Diagnostic Latch Registers. This presents the Data to the input of the "Latch" mode Registers. Issuing a Latch Clock presents this Data to the input of the Sample Registers. Issuing a Sample Clock latches this Data in the Sample Registers. Data Board A requires Latch Clock A, Data Board B requires Latch Clock B, and Data Board C requires Latch Clock C.

SUBTEST CATEGORIES

There are fourteen subtests performed by the Clock Board Diagnostic. These tests are as follows:

1. Force Conditions Test
2. Sample and Control Clocks, Diagnostic Internal Clock Test
3. Sample and Control Clocks, OR-only Enables Test
4. Sample Clocks, 10ns Clock Test
5. Sample and Control Clocks, AJ, BJ and CJ Clocks Test
6. Sample and Control Clocks, AK, BK and CK Clocks Test
7. Latch Clocks, Diagnostic Internal Clock Test
8. Latch Clocks, Diagnostic OR-only Enables Test
9. Latch Clocks, AR, BR and CR Clocks Test
10. Latch Clocks, AS, BS and CS Clocks Test
11. Decade Frequency and Multiplier Divide by Test
12. Level RAMs Data Integrity Test
13. Level RAMs Address Integrity Test
14. Level RAMs Control Test

ERROR COUNT CATEGORIES

The Error Count Display information is a one for one match with the subtest above. The K450 Diagnostic Operating System displays the message Subtest n instead of the actual test name (where n = Subtest Number).

Subtest	1	(Force Conditions)
Subtest	2	(Sample and Control Clocks, Diagnostic Internal)
Subtest	3	(Sample and Control Clocks, OR-only Enables)
Subtest	4	(Sample Clocks, 10ns Clock Test
Subtest	5	(Sample and Control Clocks, AJ, BJ and CJ)
Subtest	6	(Sample and Control Clocks, AK, BK and CK)
Subtest	7	(Latch Clocks, Diagnostic Internal)
Subtest	8	(Latch Clocks, Diagnostic OR-only Enables)
Subtest	9	(Latch Clocks, AR, BR and CR)

Subtest 10	(Latch Clocks, AS, BS and CS)
Subtest 11	(Decade Frequency and Multiplier)
Subtest 12	(Level RAMs Data Integrity)
Subtest 13	(Level RAMs Address Integrity)
Subtest 14	(Level RAMs Control)

Clock Board Diagnostic Subtest 1

TITLE: FORCE CONDITIONS TEST

TARGET LOGIC: 7J, 6J, 8J, 10K,
11K, 12J, 6K, 9K, 9J, 11H
10H
10G, 10F, 9F, 11K,
5J

TEST DESCRIPTION:

This test issues commands to the Clock Board and expects to see certain status conditions existing. Commands are issued by writing to port 0BEH, and the Status is read back from port 0B2H.

Since the Clock Board only provides 4 status bits for all of the 113 command bits, only a fraction of the I/O read/write/control logic is actually tested. If there are errors in this test, the I/O decode logic and/or data latches may be faulty, and the succeeding tests probably has multiple errors.

TEST STEP INFORMATION:

Step	Expected Status
1	A000H
2	2000H
3	0000H
4	6000H, 7000H
5	7000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Force Conditions/Status Error
No Clocking used
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range of 1 to 5.

aaaa is the address of the Clock Board Status Register, 00B2H.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Status Register.

NOTE: With the limited amount of status bits on the Clock Board, it is difficult to pin point the cause of an error. Whether the fault lies with an address decoder, a Data Bit Driver or Latch, the fault can be determined by using a Logic Analyzer or Scope, and setting the Loop On Error Option.

Clock Board Diagnostic Subtest 2

TITLE: SAMPLE AND CONTROL CLOCKS, DIAGNOSTIC INTERNAL CLOCK TEST

TARGET LOGIC:

7A, 8A, 10H, 7B, 8B, 9G
7D, 8D, 10J, 7E, 8E, 9H
7F, 8F, 7G, 8G, 7H, 8H
11H, 10D, 12C, 11C
10C
11B
3E, 3F, 3G, 3H, 4H, 4J, 4C, 4D

TEST DESCRIPTION:

The Diagnostic Internal Sample Clocks A, B and C, and the Diagnostic Internal Control Clock tests for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable, and the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing a Diagnostic Internal Sample Clock, and checking the Sample Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing a Diagnostic Internal Control Clock, and checking the New Pipe Registers to see if a Data transfer took place.

NOTE: The Diagnostic Internal Clock is kicked by outputing a 1 to bit D0 of Write Registers 0B8H of the Clock Board. This produces a clock pulse the width of the 8086's Write pulse. Consecutive kicks are achieved by consecutive outputs to this port. It is never necessary to set this bit low.

TEST STEP INFORMATION:

Step	Data	Clock Tested	Data Verified at
1	0000H	Sample A, B, C	Sample Registers A, B, C
2	5555H	Sample A, B, C	Sample Registers A, B, C
3	AAAAH	Sample A, B, C	Sample Registers A, B, C
4	CCCCH	Sample A, B, C	Sample Registers A, B, C
5	3333H	Sample A, B, C	Sample Registers A, B, C
6	6666H	Sample A, B, C	Sample Registers A, B, C
7	9999H	Sample A, B, C	Sample Registers A, B, C
8	FFFFH	Sample A, B, C	Sample Registers A, B, C
9	0000H	Control	New Pipe Registers A, B, C
10	5555H	Control	New Pipe Registers A, B, C
11	AAAAH	Control	New Pipe Registers A, B, C
12	CCCCH	Control	New Pipe Registers A, B, C
13	3333H	Control	New Pipe Registers A, B, C
14	6666H	Control	New Pipe Registers A, B, C
15	9999H	Control	New Pipe Registers A, B, C
16	FFFFH	Control	New Pipe Registers A, B, C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
17	AAAAH	0000H	0000H	Sample A	Sample Registers A, B, C
18	0000H	BBBBH	0000H	Sample B	Sample Registers A, B, C
19	0000H	0000H	CCCCH	Sample C	Sample Registers A, B, C
20	AAAAH	BBBBH	CCCCH	Control	Sample Registers A, B, C
21	AAAAH	BBBBH	CCCCH	Control	Sample Registers A, B, C
22	AAAAH	BBBBH	CCCCH	Control	Sample Registers A, B, C
23	AAAAH	BBBBH	CCCCH	Control	New Pipe Registers A, B, C
24	AAAAH	BBBBH	CCCCH	Control	New Pipe Registers A, B, C
25	AAAAH	BBBBH	CCCCH	Control	New Pipe Registers A, B, C

NOTE: Test Steps 20 - 22 verify the Control Clock does not change the contents of the Sample Registers.

Test Steps 23 - 25 verify the Control Clock can latch Data into the New Pipe Pipe Registers with all Sample Clocks disabled.

Disable Test

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
26	AAAAH	-----	-----	Sample A	Sample Register A
27	-----	BBBBH	-----	Sample B	Sample Register B
28	-----	-----	CCCCH	Sample C	Sample Register C
29	0000H	-----	-----	Control	New Pipe Register A
30	-----	0000H	-----	Control	New Pipe Register B
31	-----	-----	0000H	Control	New Pipe Register C

Force Disqualify Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
32	AAAAH	-----	-----	Sample A	Sample Register A
33	-----	BBBBH	-----	Sample B	Sample Register B
34	-----	-----	CCCCH	Sample C	Sample Register C
35	0000H	-----	-----	Control	New Pipe Register A
36	-----	0000H	-----	Control	New Pipe Register B
37	-----	-----	0000H	Control	New Pipe Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
Diagnostic Internal Clock
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 37.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control.

tttt is the test type: Functional,
Uniqueness,
Disable,
Force Disqualify

aaaa is the address of a Data Board Sample Register:

0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

or a Data Board New Pipe Register:

0C4H for Data Board A,
0D4H for Data Board B,
0E4H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:

0000H,
5555H,
AAAAH,
CCCCH,
3333H,
6666H,
9999H,
FFFFH.

NOTE: 0000H is the expected Data Word for Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 3

TITLE: SAMPLE AND CONTROL CLOCKS OR-ONLY ENABLES TEST

TARGET LOGIC: 5E, 5F, 5G, 5H, 4H, 4J, 4C, 4D

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Sample Clocks A, B and C, and Control Clock's OR-Only Enable bits are tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Force Disqualify Disable test.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing a Sample Clock by toggling the OR-Only Enable bit, and checking the Sample Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing a Control Clock by toggling the OR-Only Enable bit, and checking the New Pipe Registers to see if a Data transfer took place.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A	Sample Register A
2	BBBBH	Sample B	Sample Register B
3	CCCCH	Sample C	Sample Register C
4	AAAAH	Control	New Pipe Register A
5	BBBBH	Control	New Pipe Register B
6	CCCCH	Control	New Pipe Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	0000H	0000H	Sample A	Sample Registers A, B, C
8	0000H	BBBBH	0000H	Sample B	Sample Registers A, B, C
9	0000H	0000H	CCCCH	Sample C	Sample Registers A, B, C
10	AAAAH	BBBBH	CCCCH	Control	New Pipe Registers A, B, C
11	AAAAH	BBBBH	CCCCH	Control	New Pipe Registers A, B, C

Force Disqualify Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
12	AAAAH	-----	-----	Sample A	Sample Register A
13	-----	BBBBH	-----	Sample B	Sample Register B
14	-----	-----	CCCCH	Sample C	Sample Register C
15	0000H	-----	-----	Control	New Pipe Register A
16	-----	0000H	-----	Control	New Pipe Register B
17	-----	-----	0000H	Control	New Pipe Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
OR Only Enables
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 17.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control.

tttt is the test type: Functional,
Uniqueness,
Force Disqualify.

aaaa is the address of a Data Board Sample Register:

0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

or a Data Board New Pipe Register:

0C4H for Data Board A,
0D4H for Data Board B,
0E4H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:

AAAAH for Data Board A, (0C6H, 0C4H).
BBBBH for Data Board B, (0D6H, 0D4H).
CCCCH for Data Board C, (0E6H, 0E4H).

NOTE: 0000H **is the expected data word for all Data Boards during Uniqueness Testing.**

Clock Board Diagnostic Subtest 4

TITLE: SAMPLE CLOCKS, 10ns CLOCK TEST

TARGET LOGIC: 5E, 5F, 5G, 4H, 4J, 4C, 4D

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Sample Clocks A, B, C, and 10ns Clock Enable bit are tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, toggling the 10ns Enable bit, and then checking the Sample Registers to see if a Data transfer took place.

NOTE: The 10ns Enable bit is toggled active then inactive with two consecutive output instructions by the 8086 CPU. Since the 100Mhz Clock is so fast compared to the execution speed of the 8086, many Sample Clocks occur during the short period that the 10ns Enable is active. This does not cause a problem, since the Sample Register cannot overflow.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A	Sample Register A
2	BBBBH	Sample B	Sample Register B
3	CCCCH	Sample C	Sample Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
4	AAAAH	0000H	0000H	Sample A	Sample Registers A, B, C
5	0000H	BBBBH	0000H	Sample B	Sample Registers A, B, C
6	0000H	0000H	CCCCH	Sample C	Sample Registers A, B, C

Force Disqualify Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	-----	-----	Sample A	Sample Register A
8	-----	BBBBH	-----	Sample B	Sample Register B
9	-----	-----	CCCCH	Sample C	Sample Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
10 ns Clock
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 9.

cccc is the tested Clock: Sample A,
Sample B,
Sample C.

tttt is the test type: Functional,
Uniqueness,
Force Disqualify.

aaaa is the address of a Data Board Sample Register:

0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:

AAAAH for Data Board A.
BBBBH for Data Board B.
CCCCH for Data Board C.

NOTE: 0000H is the expected Data Word for all Data Boards during Testing.

Clock Board Diagnostic Subtest 5

TITLE: SAMPLE AND CONTROL CLOCKS AJ, BJ, and CJ CLOCKS TEST

TARGET LOGIC: 3E, 5E, 3F, 5F, 3G, 5G, 3H, 5H
4H, 4J, 4C, 4D
4E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AJ, AJ/, BJ, BJ/, CJ and CJ/ clock enables for the Sample Clocks A, B, C and the Control Clock are tested for functionality and uniqueness as well as the ability to disable these Clocks using the Threshold Disable, and the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing a Sample Clock by toggling one of the AJ, BJ, CJ Enables, and checking the Sample Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing a Control Clock by toggling one of the AJ, BJ, CJ Enables, and checking the New Pipe Registers to see if a Data transfer took place.

NOTE: The Logic states of AJ, AJ/, BJ, BJ/, CJ and CJ/ are determined by the current threshold at the probes. An ECL Threshold, and a VARAIABLE A Threshold are used to provide the High and Low logic states. This test requires the use of the Threshold Board and the probes.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A - AJ/, BJ/, CJ/	Sample Register A
2	BBBBH	Sample B - AJ/, BJ/, CJ/	Sample Register B
3	CCCCH	Sample C - AJ/, BJ/, CJ/	Sample Register C
4	AAAAH	Control - AJ/, BJ/, CJ/	New Pipe Register A
5	BBBBH	Control - AJ/, BJ/, CJ/	New Pipe Register B
6	CCCCH	Control - AJ/, BJ/, CJ/	New Pipe Register C
7	AAAAH	Sample A - AJ, BJ, CJ	Sample Register A
8	BBBBH	Sample B - AJ, BJ, CJ	Sample Register B
9	CCCCH	Sample C - AJ, BJ, CJ	Sample Register C
10	AAAAH	Control - AJ, BJ, CJ	New Pipe Register A
11	BBBBH	Control - AJ, BJ, CJ	New Pipe Register B
12	CCCCH	Control - AJ, BJ, CJ	New Pipe Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
13	AAAAH	0000H	0000H	Sample A - AJ/	Sample Registers A, B, C
14	AAAAH	0000H	0000H	Sample A - BJ/	Sample Registers A, B, C
15	AAAAH	0000H	0000H	Sample A - CJ/	Sample Registers A, B, C
16	0000H	BBBBH	0000H	Sample B - AJ/	Sample Registers A, B, C
17	0000H	BBBBH	0000H	Sample B - BJ/	Sample Registers A, B, C
18	0000H	BBBBH	0000H	Sample B - CJ/	Sample Registers A, B, C
19	0000H	0000H	CCCCH	Sample C - AJ/	Sample Registers A, B, C
20	0000H	0000H	CCCCH	Sample C - BJ/	Sample Registers A, B, C
21	0000H	0000H	CCCCH	Sample C - CJ/	Sample Registers A, B, C
22	AAAAH	BBBBH	CCCCH	Control - AJ/	New Pipe Registers A, B, C
23	AAAAH	BBBBH	CCCCH	Control - BJ/	New Pipe Registers A, B, C
24	AAAAH	BBBBH	CCCCH	Control - CJ/	New Pipe Registers A, B, C
25	AAAAH	0000H	0000H	Sample A - AJ	Sample Registers A, B, C
26	AAAAH	0000H	0000H	Sample A - BJ	Sample Registers A, B, C
27	AAAAH	0000H	0000H	Sample A - CJ	Sample Registers A, B, C
28	0000H	BBBBH	0000H	Sample B - AJ	Sample Registers A, B, C
29	0000H	BBBBH	0000H	Sample B - BJ	Sample Registers A, B, C
30	0000H	BBBBH	0000H	Sample B - CJ	Sample Registers A, B, C
31	0000H	0000H	CCCCH	Sample C - AJ	Sample Registers A, B, C
32	0000H	0000H	CCCCH	Sample C - BJ	Sample Registers A, B, C
33	0000H	0000H	CCCCH	Sample C - CJ	Sample Registers A, B, C
34	AAAAH	BBBBH	CCCCH	Control - AJ	New Pipe Registers A, B, C
35	AAAAH	BBBBH	CCCCH	Control - BJ	New Pipe Registers A, B, C
36	AAAAH	BBBBH	CCCCH	Control - CJ	New Pipe Registers A, B, C

Threshold Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
37	AAAAH	BBBBH	CCCCH	Sample A - AJ/	Sample Registers A, B, C
38	AAAAH	BBBBH	CCCCH	Sample A - BJ/	Sample Registers A, B, C
39	AAAAH	BBBBH	CCCCH	Sample A - CJ/	Sample Registers A, B, C
40	AAAAH	BBBBH	CCCCH	Sample B - AJ/	Sample Registers A, B, C
41	AAAAH	BBBBH	CCCCH	Sample B - BJ/	Sample Registers A, B, C
42	AAAAH	BBBBH	CCCCH	Sample B - CJ/	Sample Registers A, B, C
43	AAAAH	BBBBH	CCCCH	Sample C - AJ/	Sample Registers A, B, C
44	AAAAH	BBBBH	CCCCH	Sample C - BJ/	Sample Registers A, B, C
45	AAAAH	BBBBH	CCCCH	Sample C - CJ/	Sample Registers A, B, C
46	0000H	0000H	0000H	Control - AJ/	New Pipe Registers A, B, C
47	0000H	0000H	0000H	Control - BJ/	New Pipe Registers A, B, C
48	0000H	0000H	0000H	Control - CJ/	New Pipe Registers A, B, C
49	AAAAH	BBBBH	CCCCH	Sample A - AJ	Sample Registers A, B, C
50	AAAAH	BBBBH	CCCCH	Sample A - BJ	Sample Registers A, B, C
51	AAAAH	BBBBH	CCCCH	Sample A - CJ	Sample Registers A, B, C
52	AAAAH	BBBBH	CCCCH	Sample B - AJ	Sample Registers A, B, C
53	AAAAH	BBBBH	CCCCH	Sample B - BJ	Sample Registers A, B, C
54	AAAAH	BBBBH	CCCCH	Sample B - CJ	Sample Registers A, B, C
55	AAAAH	BBBBH	CCCCH	Sample C - AJ	Sample Registers A, B, C
56	AAAAH	BBBBH	CCCCH	Sample C - BJ	Sample Registers A, B, C
57	AAAAH	BBBBH	CCCCH	Sample C - CJ	Sample Registers A, B, C
58	0000H	0000H	0000H	Control - AJ	New Pipe Registers A, B, C
59	0000H	0000H	0000H	Control - BJ	New Pipe Registers A, B, C
60	0000H	0000H	0000H	Control - CJ	New Pipe Registers A,B,C

Force Disqualify Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
61	AAAAH	BBBBH	CCCCH	Sample A - AJ/	Sample Registers A, B, C
62	AAAAH	BBBBH	CCCCH	Sample A - BJ/	Sample Registers A, B, C
63	AAAAH	BBBBH	CCCCH	Sample A - CJ/	Sample Registers A, B, C
64	AAAAH	BBBBH	CCCCH	Sample B - AJ/	Sample Registers A, B, C
65	AAAAH	BBBBH	CCCCH	Sample B - BJ/	Sample Registers A, B, C
66	AAAAH	BBBBH	CCCCH	Sample B - CJ/	Sample Registers A, B, C
67	AAAAH	BBBBH	CCCCH	Sample C - AJ/	Sample Registers A, B, C
68	AAAAH	BBBBH	CCCCH	Sample C - BJ/	Sample Registers A, B, C
69	AAAAH	BBBBH	CCCCH	Sample C - CJ/	Sample Registers A, B, C
70	0000H	0000H	0000H	Control - AJ/	New Pipe Registers A, B, C
71	0000H	0000H	0000H	Control - BJ/	New Pipe Registers A, B, C
72	0000H	0000H	0000H	Control - CJ/	New Pipe Registers A, B, C
73	AAAAH	BBBBH	CCCCH	Sample A - AJ	Sample Registers A, B, C
74	AAAAH	BBBBH	CCCCH	Sample A - BJ	Sample Registers A, B, C
75	AAAAH	BBBBH	CCCCH	Sample A - CJ	Sample Registers A, B, C
76	AAAAH	BBBBH	CCCCH	Sample B - AJ	Sample Registers A, B, C
77	AAAAH	BBBBH	CCCCH	Sample B - BJ	Sample Registers A, B, C
78	AAAAH	BBBBH	CCCCH	Sample B - CJ	Sample Registers A, B, C
79	AAAAH	BBBBH	CCCCH	Sample C - AJ	Sample Registers A, B, C
80	AAAAH	BBBBH	CCCCH	Sample C - BJ	Sample Registers A, B, C
81	AAAAH	BBBBH	CCCCH	Sample C - CJ	Sample Registers A, B, C
82	0000H	0000H	0000H	Control - AJ	New Pipe Registers A, B, C
83	0000H	0000H	0000H	Control - BJ	New Pipe Registers A, B, C
84	0000H	0000H	0000H	Control - CJ	New Pipe Registers A, B, C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enables
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 84.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control.

tttt is the test type: Functional,
Uniqueness,
Disable,
Force Disqualify.

qqqq is the tested Clock Enable: AJ/ BJ/ CJ/,
AJ BJ CJ,
AJ/,
BJ/,
CJ/,
AJ,
BJ,
CJ.

aaaa is the address of a Data Board Sample Register:

0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.
or a Data Board New Pipe Register:
0C4H for Data Board A,
0D4H for Data Board B,
0E4H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:

AAAAH for Data Board A, (0C6H, 0C4H).
BBBBH for Data Board B, (0D6H, 0D4H).
CCCCH for Data Board C, (0E6H, 0E4H).

NOTE: 0000H is the expected Data Word for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 6

TITLE: SAMPLE AND CONTROL CLOCKS AK, BK AND CK CLOCKS TEST

TARGET LOGIC: 5A, 4A, 5B, 5C, 5D, 4C, 4D,
5E, 5F, 5G, 5H, 4H, 4J,
6A

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AK, AK/, BK, BK/, CK and CK/ clock enables for the Sample Clocks A, B, C, and the Control Clock is tested for functionality and uniqueness, as well as well as the ability to disable these Clocks using the Threshold Disable, and the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing a Sample Clock by toggling one of the AK, BK, CK Enables, and checking the Sample Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing a Control Clock by toggling one of the AK, BK, CK Enables, and checking the New Pipe Registers to see if a Data transfer took place.

NOTE: The Logic states of AK, AK/, BK, BK/, CK and CK/ are determined by the current threshold at the probes. An ECL Threshold, and a VARAIABLE A Threshold is used to provide the High and Low logic states.

This test requires the use of the Threshold Board, and the probes.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A - AK/, BK/, CK/	Sample Register A
2	BBBBH	Sample B - AK/, BK/, CK/	Sample Register B
3	CCCCH	Sample C - AK/, BK/, CK/	Sample Register C
4	AAAAH	Control - AK/, BK/, CK/	New Pipe Register A
5	BBBBH	Control - AK/, BK/, CK/	New Pipe Register B
6	CCCCH	Control - AK/, BK/, CK/	New Pipe Register C
7	AAAAH	Sample A - AK, BK, CK	Sample Register A
8	BBBBH	Sample B - AK, BK, CK	Sample Register B
9	CCCCH	Sample C - AK, BK, CK	Sample Register C
10	AAAAH	Control - AK, BK, CK	New Pipe Register A
11	BBBBH	Control - AK, BK, CK	New Pipe Register B
12	CCCCH	Control - AK, BK, CK	New Pipe Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
13	AAAAH	0000H	0000H	Sample A - AK/	Sample Registers A, B, C
14	AAAAH	0000H	0000H	Sample A - BK/	Sample Registers A, B, C
15	AAAAH	0000H	0000H	Sample A - CK/	Sample Registers A, B, C
16	0000H	BBBBH	0000H	Sample B - AK/	Sample Registers A, B, C
17	0000H	BBBBH	0000H	Sample B - BK/	Sample Registers A, B, C
18	0000H	BBBBH	0000H	Sample B - CK/	Sample Registers A, B, C
19	0000H	0000H	CCCCH	Sample C - AK/	Sample Registers A, B, C
20	0000H	0000H	CCCCH	Sample C - BK/	Sample Registers A, B, C
21	0000H	0000H	CCCCH	Sample C - CK/	Sample Registers A, B, C
22	AAAAH	BBBBH	CCCCH	Control - AK/	New Pipe Registers A, B, C
23	AAAAH	BBBBH	CCCCH	Control - BK/	New Pipe Registers A, B, C
24	AAAAH	BBBBH	CCCCH	Control - CK/	New Pipe Registers A, B, C
25	AAAAH	0000H	0000H	Sample A - AK	Sample Registers A, B, C
26	AAAAH	0000H	0000H	Sample A - BK	Sample Registers A, B, C
27	AAAAH	0000H	0000H	Sample A - CK	Sample Registers A, B, C
28	0000H	BBBBH	0000H	Sample B - AK	Sample Registers A, B, C
29	0000H	BBBBH	0000H	Sample B - BK	Sample Registers A, B, C
30	0000H	BBBBH	0000H	Sample B - CK	Sample Registers A, B, C
31	0000H	0000H	CCCCH	Sample C - AK	Sample Registers A, B, C
32	0000H	0000H	CCCCH	Sample C - BK	Sample Registers A, B, C
33	0000H	0000H	CCCCH	Sample C - CK	Sample Registers A, B, C
34	AAAAH	BBBBH	CCCCH	Control - AK	New Pipe Registers A, B, C
35	AAAAH	BBBBH	CCCCH	Control - BK	New Pipe Registers A, B, C
36	AAAAH	BBBBH	CCCCH	Control - CK	New Pipe Registers A, B, C

Threshold Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
37	AAAAH	BBBBH	CCCCH	Sample A - AK/	Sample Registers A, B, C
38	AAAAH	BBBBH	CCCCH	Sample A - BK/	Sample Registers A, B, C
39	AAAAH	BBBBH	CCCCH	Sample A - CK/	Sample Registers A, B, C
40	AAAAH	BBBBH	CCCCH	Sample B - AK/	Sample Registers A, B, C
41	AAAAH	BBBBH	CCCCH	Sample B - BK/	Sample Registers A, B, C
42	AAAAH	BBBBH	CCCCH	Sample B - CK/	Sample Registers A, B, C
43	AAAAH	BBBBH	CCCCH	Sample C - AK/	Sample Registers A, B, C
44	AAAAH	BBBBH	CCCCH	Sample C - BK/	Sample Registers A, B, C
45	AAAAH	BBBBH	CCCCH	Sample C - CK/	Sample Registers A, B, C
46	0000H	0000H	0000H	Control - AK/	New Pipe Registers A, B, C
47	0000H	0000H	0000H	Control - BK/	New Pipe Registers A, B, C
48	0000H	0000H	0000H	Control - CK/	New Pipe Registers A, B, C
49	AAAAH	BBBBH	CCCCH	Sample A - AK	Sample Registers A, B, C
50	AAAAH	BBBBH	CCCCH	Sample A - BK	Sample Registers A, B, C
51	AAAAH	BBBBH	CCCCH	Sample A - CK	Sample Registers A, B, C
52	AAAAH	BBBBH	CCCCH	Sample B - AK	Sample Registers A, B, C
53	AAAAH	BBBBH	CCCCH	Sample B - BK	Sample Registers A, B, C
54	AAAAH	BBBBH	CCCCH	Sample B - CK	Sample Registers A, B, C
55	AAAAH	BBBBH	CCCCH	Sample C - AK	Sample Registers A, B, C
56	AAAAH	BBBBH	CCCCH	Sample C - BK	Sample Registers A, B, C
57	AAAAH	BBBBH	CCCCH	Sample C - CK	Sample Registers A, B, C
58	0000H	0000H	0000H	Control - AK	New Pipe Registers A, B, C
59	0000H	0000H	0000H	Control - BK	New Pipe Registers A, B, C
60	0000H	0000H	0000H	Control - CK	New Pipe Registers A, B, C

Force Disqualify Test

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
61	AAAAH	BBBBH	CCCCH	Sample A - AK/	Sample Registers A, B, C
62	AAAAH	BBBBH	CCCCH	Sample A - BK/	Sample Registers A, B, C
63	AAAAH	BBBBH	CCCCH	Sample A - CK/	Sample Registers A, B, C
64	AAAAH	BBBBH	CCCCH	Sample B - AK/	Sample Registers A, B, C
65	AAAAH	BBBBH	CCCCH	Sample B - BK/	Sample Registers A, B, C
66	AAAAH	BBBBH	CCCCH	Sample B - CK/	Sample Registers A, B, C
67	AAAAH	BBBBH	CCCCH	Sample C - AK/	Sample Registers A, B, C
68	AAAAH	BBBBH	CCCCH	Sample C - BK/	Sample Registers A, B, C
69	AAAAH	BBBBH	CCCCH	Sample C - CK/	Sample Registers A, B, C
70	0000H	0000H	0000H	Control - AK/	New Pipe Registers A, B, C
71	0000H	0000H	0000H	Control - BK/	New Pipe Registers A, B, C
72	0000H	0000H	0000H	Control - CK/	New Pipe Registers A, B, C
73	AAAAH	BBBBH	CCCCH	Sample A - AK	Sample Registers A, B, C
74	AAAAH	BBBBH	CCCCH	Sample A - BK	Sample Registers A, B, C
75	AAAAH	BBBBH	CCCCH	Sample A - CK	Sample Registers A, B, C
76	AAAAH	BBBBH	CCCCH	Sample B - AK	Sample Registers A, B, C
77	AAAAH	BBBBH	CCCCH	Sample B - BK	Sample Registers A, B, C
78	AAAAH	BBBBH	CCCCH	Sample B - CK	Sample Registers A, B, C
79	AAAAH	BBBBH	CCCCH	Sample C - AK	Sample Registers A, B, C
80	AAAAH	BBBBH	CCCCH	Sample C - BK	Sample Registers A, B, C
81	AAAAH	BBBBH	CCCCH	Sample C - CK	Sample Registers A, B, C
82	0000H	0000H	0000H	Control - AK	New Pipe Registers A, B, C
83	0000H	0000H	0000H	Control - BK	New Pipe Registers A, B, C
84	0000H	0000H	0000H	Control - CK	New Pipe Registers A, B, C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enables
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 84.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control

tttt is the test type: Functional,
Uniqueness,
Disable,
Force Disqualify

qqqq is the tested Clock Enable: AK/ BK/ CK/,
AK BK CK,
AK/,
BK/,
CK/,
AK,
BK,
CK

aaaa is the address of a Data Board Sample Register:

0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

or a Data Board New Pipe Register:
0C4H for Data Board A,
0D4H for Data Board B,
0E4H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:

AAAAH for Data Board A, (0C6H, 0C4H).
BBBBH for Data Board B, (0D6H, 0D4H).
CCCCH for Data Board C, (0E6H, 0E4H).

NOTE: 0000H is the expected Data Word for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 7

TITLE: LATCH CLOCKS, DIAGNOSTIC INTERNAL CLOCK TEST

TARGET LOGIC: 11H, 1F, 1G, 1H, 2H
1D, 2B, 2A, 2C, 2D
6A

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Diagnostic Internal Latch Clocks A, B and C are tested for functionality as well as the ability to disable these Clocks using the Normal Disable and the Latch Disqualify Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board, issuing a Diagnostic Latch Clock, issuing a Diagnostic Sample Clock, and checking the Sample Registers to see if a Data transfer took place.

NOTE: The Diagnostic Latch Clock is kicked by outputing a 1 to bit D1 of Write Register 0B8H of the Clock Board. This produces a clock pulse the width of the 8086's Write pulse. Consecutive kicks is achieved by consecutive outputs to this port. It is never necessary to set this bit low.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	0000H	Latch A, B, C	Sample Registers A, B, C
2	5555H	Latch A, B, C	Sample Registers A, B, C
3	AAAAH	Latch A, B, C	Sample Registers A, B, C
4	CCCCH	Latch A, B, C	Sample Registers A, B, C
5	3333H	Latch A, B, C	Sample Registers A, B, C
6	6666H	Latch A, B, C	Sample Registers A, B, C
7	9999H	Latch A, B, C	Sample Registers A, B, C
8	FFFFH	Latch A, B, C	Sample Registers A, B, C

Threshold Disable Test:

Step	Data	Clock Tested	Data Verified at
9	AAAAH	Latch A	Sample Register A
10	BBBBH	Latch B	Sample Register B
11	CCCCH	Latch C	Sample Register C

Latch Disqualify Disable Test:

Step	Data	Clock Tested	Data Verified at
12	AAAAH	Latch A	Sample Register A
13	BBBBH	Latch B	Sample Register B
14	CCCCH	Latch C	Sample Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
Diagnostic Latch Clock
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 14.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Threshold Disable,
Disqualify Disable.

aaaa is the address of a Data Board Sample Register:

0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:

Data for Functional Testing:

0000H,
5555H,
AAAAH,
CCCCH,
3333H,
6666H,
9999H,
FFFFH.

Data for Threshold Disable and Disqualify Disable Testing:

AAAAH for Data Board A.
BBBBH for Data Board B.
CCCCH for Data Board C.

Clock Board Diagnostic Subtest 8

TITLE: LATCH CLOCKS, OR-ONLY ENABLES TEST

TARGET LOGIC: 2E, 2F, 2G, 2H
1D, 2B, 2A, 2C, 2D

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Latch Clocks A, B and C OR-Only Enables are tested for functionality, and the ability to disable these Clocks using the the Latch Disqualify Disable. The Latch Clocks are tested by placing Data at the Front End of the Data Board, issuing a Diagnostic Latch Clock, issuing a Diagnostic Sample Clock, and checking the Sample Registers to see if a Data transfer took place.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Latch A	Sample Register A
2	BBBBH	Latch B	Sample Register B
3	CCCCH	Latch C	Sample Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
4	AAAAH	0000H	0000H	Latch A	Sample Registers A, B, C
5	0000H	BBBBH	0000H	Latch B	Sample Registers A, B, C
6	0000H	0000H	CCCCH	Latch C	Sample Registers A, B, C

Latch Disqualify Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	BBBBH	CCCCH	Latch A	Sample Registers A, B, C
8	AAAAH	BBBBH	CCCCH	Latch B	Sample Registers A, B, C
9	AAAAH	BBBBH	CCCCH	Latch C	Sample Registers A, B, C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
OR Only Enables
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 9.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Uniqueness,
Latch Disqualify Disable.

aaaa is the address of a Data Board Sample Register:

0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:

AAAAH for Data Board A.
BBBBH for Data Board B.
CCCCH for Data Board C.

NOTE: 0000H is the expected data word for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 9

TITLE: LATCH CLOCKS, AR, BR AND CR CLOCKS TEST

TARGET LOGIC: 1F, 2E, 1G, 2F, 1H, 2G, 2H
1D, 2B, 2A, 2C, 2D
1E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AR, AR/, BR, BR/, CR and CR/ Clock Enables for Latch Clocks A, B, and C are tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable, and the Latch Disqualify Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board, issuing a Latch Clock by toggling one of the AR, BR, CR Enables, and issuing a Diagnostic Internal Sample Clock and checking the Sample Registers to see if a Data transfer took place.

NOTE: The Logic states of AR, AR/, BR, BR/, CR and CR/ are determined by the current threshold at the probes. An ECL Threshold, and a VARIABLE A Threshold is used to provide the High and Low logic states.

This test requires the use of the Threshold Board, and the probes.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Latch A - AR/, BR/, CR/	Sample Register A
2	BBBBH	Latch B - AR/, BR/, CR/	Sample Register B
3	CCCCH	Latch C - AR/, BR/, CR/	Sample Register C
4	AAAAH	Latch A - AR, BR, CR	Sample Register A
5	BBBBH	Latch B - AR, BR, CR	Sample Register B
6	CCCCH	Latch C - AR, BR, CR	Sample Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	0000H	0000H	Latch A - AR/	Sample Registers A, B, C
8	AAAAH	0000H	0000H	Latch A - BR/	Sample Registers A, B, C
9	AAAAH	0000H	0000H	Latch A - CR/	Sample Registers A, B, C
10	0000H	BBBBH	0000H	Latch B - AR/	Sample Registers A, B, C
11	0000H	BBBBH	0000H	Latch B - BR/	Sample Registers A, B, C
12	0000H	BBBBH	0000H	Latch B - CR/	Sample Registers A, B, C
13	0000H	0000H	CCCCH	Latch C - AR/	Sample Registers A, B, C

14	0000H	0000H	CCCCH	Latch C - BR/	Sample Registers A, B, C
15	0000H	0000H	CCCCH	Latch C - CR/	Sample Registers A, B, C
16	AAAAH	0000H	0000H	Latch A - AR	Sample Registers A, B, C
17	AAAAH	0000H	0000H	Latch A - BR	Sample Registers A, B, C
18	AAAAH	0000H	0000H	Latch A - CR	Sample Registers A, B, C
19	0000H	BBBBH	0000H	Latch B - AR	Sample Registers A, B, C
20	0000H	BBBBH	0000H	Latch B - BR	Sample Registers A, B, C
21	0000H	BBBBH	0000H	Latch B - CR	Sample Registers A, B, C
22	0000H	0000H	CCCCH	Latch C - AR	Sample Registers A, B, C
23	0000H	0000H	CCCCH	Latch C - BR	Sample Registers A, B, C
24	0000H	0000H	CCCCH	Latch C - CR	Sample Registers A, B, C

Threshold Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
25	AAAAH	BBBBH	CCCCH	Latch A - AR/	Sample Registers A, B, C
26	AAAAH	BBBBH	CCCCH	Latch A - BR/	Sample Registers A, B, C
27	AAAAH	BBBBH	CCCCH	Latch A - CR/	Sample Registers A, B, C
28	AAAAH	BBBBH	CCCCH	Latch B - AR/	Sample Registers A, B, C
29	AAAAH	BBBBH	CCCCH	Latch B - BR/	Sample Registers A, B, C
30	AAAAH	BBBBH	CCCCH	Latch B - CR/	Sample Registers A, B, C
31	AAAAH	BBBBH	CCCCH	Latch C - AR/	Sample Registers A, B, C
32	AAAAH	BBBBH	CCCCH	Latch C - BR/	Sample Registers A, B, C
33	AAAAH	BBBBH	CCCCH	Latch C - CR/	Sample Registers A, B, C
34	AAAAH	BBBBH	CCCCH	Latch A - AR	Sample Registers A, B, C
35	AAAAH	BBBBH	CCCCH	Latch A - BR	Sample Registers A, B, C
36	AAAAH	BBBBH	CCCCH	Latch A - CR	Sample Registers A, B, C
37	AAAAH	BBBBH	CCCCH	Latch B - AR	Sample Registers A, B, C
38	AAAAH	BBBBH	CCCCH	Latch B - BR	Sample Registers A, B, C
39	AAAAH	BBBBH	CCCCH	Latch B - CR	Sample Registers A, B, C
40	AAAAH	BBBBH	CCCCH	Latch C - AR	Sample Registers A, B, C
41	AAAAH	BBBBH	CCCCH	Latch C - BR	Sample Registers A, B, C
42	AAAAH	BBBBH	CCCCH	Latch C - CR	Sample Registers A, B, C

Latch Disqualify Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
43	AAAAH	BBBBH	CCCCH	Latch A - AR/	Sample Registers A, B, C
44	AAAAH	BBBBH	CCCCH	Latch A - BR/	Sample Registers A, B, C
45	AAAAH	BBBBH	CCCCH	Latch A - CR/	Sample Registers A, B, C
46	AAAAH	BBBBH	CCCCH	Latch B - AR/	Sample Registers A, B, C
47	AAAAH	BBBBH	CCCCH	Latch B - BR/	Sample Registers A, B, C
48	AAAAH	BBBBH	CCCCH	Latch B - CR/	Sample Registers A, B, C
49	AAAAH	BBBBH	CCCCH	Latch C - AR/	Sample Registers A, B, C
50	AAAAH	BBBBH	CCCCH	Latch C - BR/	Sample Registers A, B, C
51	AAAAH	BBBBH	CCCCH	Latch C - CR/	Sample Registers A, B, C
52	AAAAH	BBBBH	CCCCH	Latch A - AR	Sample Registers A, B, C
53	AAAAH	BBBBH	CCCCH	Latch A - BR	Sample Registers A, B, C
54	AAAAH	BBBBH	CCCCH	Latch A - CR	Sample Registers A, B, C
55	AAAAH	BBBBH	CCCCH	Latch B - AR	Sample Registers A, B, C
56	AAAAH	BBBBH	CCCCH	Latch B - BR	Sample Registers A, B, C
57	AAAAH	BBBBH	CCCCH	Latch B - CR	Sample Registers A, B, C
58	AAAAH	BBBBH	CCCCH	Latch C - AR	Sample Registers A, B, C
59	AAAAH	BBBBH	CCCCH	Latch C - BR	Sample Registers A, B, C
60	AAAAH	BBBBH	CCCCH	Latch C - CR	Sample Registers A, B, C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enable
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 60.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Uniqueness,
Threshold Disable,
Latch Disqualify Disable.

qqqq is the tested Clock Enable: AR/ BR/ CR/,
AR BR CR,
AR/,
BR/,
CR/,
AR,
BR,
CR.

aaaa is the address of a Data Board Sample Register:

0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:

AAAAH for Data Board A.
BBBBH for Data Board B.
CCCCH for Data Board C.

NOTE: 0000H is the expected data word for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 10

TITLE: LATCH CLOCKS AS, BS AND CS CLOCKS TEST

TARGET LOGIC: 2B, 2A, 2C, 2D, 1D, 2E, 2F, 2G, 2H
3A

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AS, AS/, BS, BS/, CS and CS/ Clock Enables for Latch Clocks A, B and C are tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board, asserting the appropriate AS, BS, CS Enables, issuing a Diagnostic Latch Clock, and issuing a Diagnostic Internal Sample Clock and checking the Sample Registers to see if a Data transfer took place.

This test is different than the rest due to the transparent mode of the 10130 Latches on the Data Boards. When the Latch Clock is held in a low state, the 10130 Latches on the Data Board are transparent, the Q output follows the D input. When the Latch Clock goes high, this latches the Data into the 10130's and the D input then becomes a don't care.

In this test, instead of toggling the enable to the AS, BS or CS, it is held active and a Diagnostic Int Clock issued. This causes the Data Board to be in Latch Mode, instead of being transparent.

The Logic states of AR, AR/, BR, BR/, CR and CR/ are determined by the current threshold at the probes. An ECL Threshold, and a VARIABLE A Threshold are used to provide the High and Low logic states.

This test requires the use of the Threshold Board, and the probes.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Latch A - AS/, BS/, CS/	Sample Register A
2	BBBBH	Latch B - AS/, BS/, CS/	Sample Register B
3	CCCCH	Latch C - AS/, BS/, CS/	Sample Register C
4	AAAAH	Latch A - AS, BS, CS	Sample Register A
5	BBBBH	Latch B - AS, BS, CS	Sample Register B
6	CCCCH	Latch C - AS, BS, CS	Sample Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	0000H	0000H	Latch A - AS/	Sample Registers A, B, C
8	AAAAH	0000H	0000H	Latch A - BS/	Sample Registers A, B, C
9	AAAAH	0000H	0000H	Latch A - CS/	Sample Registers A, B, C
10	0000H	BBBBH	0000H	Latch B - AS/	Sample Registers A, B, C
11	0000H	BBBBH	0000H	Latch B - BS/	Sample Registers A, B, C
12	0000H	BBBBH	0000H	Latch B - CS/	Sample Registers A, B, C
13	0000H	0000H	CCCCH	Latch C - AS/	Sample Registers A, B, C
14	0000H	0000H	CCCCH	Latch C - BS/	Sample Registers A, B, C
15	0000H	0000H	CCCCH	Latch C - CS/	Sample Registers A, B, C
16	AAAAH	0000H	0000H	Latch A - AS	Sample Registers A, B, C
17	AAAAH	0000H	0000H	Latch A - BS	Sample Registers A, B, C
18	AAAAH	0000H	0000H	Latch A - CS	Sample Registers A, B, C
19	0000H	BBBBH	0000H	Latch B - AS	Sample Registers A, B, C
20	0000H	BBBBH	0000H	Latch B - BS	Sample Registers A, B, C
21	0000H	BBBBH	0000H	Latch B - CS	Sample Registers A, B, C
22	0000H	0000H	CCCCH	Latch C - AS	Sample Registers A, B, C
23	0000H	0000H	CCCCH	Latch C - BS	Sample Registers A, B, C
24	0000H	0000H	CCCCH	Latch C - CS	Sample Registers A, B, C

Threshold Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
25	AAAAH	BBBBH	CCCCH	Latch A - AS/	Sample Registers A, B, C
26	AAAAH	BBBBH	CCCCH	Latch A - BS/	Sample Registers A, B, C
27	AAAAH	BBBBH	CCCCH	Latch A - CS/	Sample Registers A, B, C
28	AAAAH	BBBBH	CCCCH	Latch B - AS/	Sample Registers A, B, C
29	AAAAH	BBBBH	CCCCH	Latch B - BS/	Sample Registers A, B, C
30	AAAAH	BBBBH	CCCCH	Latch B - CS/	Sample Registers A, B, C
31	AAAAH	BBBBH	CCCCH	Latch C - AS/	Sample Registers A, B, C
32	AAAAH	BBBBH	CCCCH	Latch C - BS/	Sample Registers A, B, C
33	AAAAH	BBBBH	CCCCH	Latch C - CS/	Sample Registers A, B, C
34	AAAAH	BBBBH	CCCCH	Latch A - AS	Sample Registers A, B, C
35	AAAAH	BBBBH	CCCCH	Latch A - BS	Sample Registers A, B, C
36	AAAAH	BBBBH	CCCCH	Latch A - CS	Sample Registers A, B, C
37	AAAAH	BBBBH	CCCCH	Latch B - AS	Sample Registers A, B, C
38	AAAAH	BBBBH	CCCCH	Latch B - BS	Sample Registers A, B, C
39	AAAAH	BBBBH	CCCCH	Latch B - CS	Sample Registers A, B, C
40	AAAAH	BBBBH	CCCCH	Latch C - AS	Sample Registers A, B, C
41	AAAAH	BBBBH	CCCCH	Latch C - BS	Sample Registers A, B, C
42	AAAAH	BBBBH	CCCCH	Latch C - CS	Sample Registers A, B, C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enable
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 42.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Uniqueness,
Threshold Disable.

qqqq is the tested Clock Enable: AS/ BS/ CS/,
AS BS CS,
AS/,
BS/,
CS/,
AS,
BS,
CS.

aaaa is the address of a Data Board Sample Register:

0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:

AAAAH for Data Board A.
BBBBH for Data Board B.
CCCCH for Data Board C.

NOTE: 0000H is the expected data word for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 11

TITLE: DECADE FREQUENCY AND MULTIPLIER DIVIDE BY TEST

TARGET LOGIC:
10D, 12C, 11C
10C
11B
9E, 10E, 9C, 9D

Setup Latches in Subtest 2

100Mhz Oscilator Descrete Componets (Grid 8B-6B)

TEST DESCRIPTION:

This test checks the Clock Decade multiplexer, (Decade), and the divide by counter, (Multiplier).

The 100Mhz, 10Mhz, 1Mhz, 100Khz, 10Khz, 1Khz and 100hz Clocks are tested with various Multipliers. The Clock frequencies are verified within a ballpark range, but this verifies that the multiplexer is selecting different Decades. A frequency counter is required to adjust/verify the Time Period of the 100Mhz Clock.

When the faster Clock frequencies are being tested, the testing time is very quick, and the following message is displayed:

>Counting Clock Pulses...

During the 1Khz test, the following message is displayed:

>Counting Clock Pulses... 4 seconds

During the 100hz test, the following message is displayed:

>Counting Clock Pulses...20 seconds

During the testing of the Multiplier Divide by counter, the following message is displayed:

>Checking the Multiplier Divide by...

TEST STEP INFORMATION:

Decade Frequency Test:

Step	Decade	Mult	Clks Expected	Clks Minimum	Clks Maximum
1	0	8	256	128	384
2	1	8	256	128	384
3	2	8	256	128	384
4	3	8	256	128	384
5	4	8	256	128	384
6	5	8	256	128	384
7	6	8	256	128	384

Multiplier Divide by Test:

Step	Decade	Mult	Clks Expected	Clks Minimum	Clks Maximum
8	3	0	~83	0	2048
9	3	1	~89	Step 8 Clock Count	2048
10	3	2	~95	Step 9 Clock Count	2048
11	3	3	~97	Step 10 Clock Count	2048
12	3	4	~111	Step 11 Clock Count	2048
13	3	5	~122	Step 12 Clock Count	2048
14	3	6	~134	Step 13 Clock Count	2048
15	3	7	~148	Step 14 Clock Count	2048
16	3	8	~167	Step 15 Clock Count	2048
17	3	9	~191	Step 16 Clock Count	2048
18	3	10	~224	Step 17 Clock Count	2048
19	3	11	~270	Step 18 Clock Count	2048
20	3	12	~336	Step 19 Clock Count	2048
21	3	13	~450	Step 20 Clock Count	2048
22 *	3	14	256	0	2048
23 *	3	15	256	0	2048

The values above preceeded by ~ are approximate values. They were selected by running the test a single time on a single K450. This value varies from System to System due to minor differences in the CPU's Clock frequency, and other hardware propagation times. The precise values are not important as long as Clock count increments while the Multiplier increments.

Test Steps 22 and 23 are different from the rest. When the Multiplier goes from 13 to 14, and from 14 to 15, the Clock count no longer follows the slow-linear increase that it followed with the Multiplier range of 0 to 12. The Clock count approximately doubles, so a ballparking method of 256 clocks inside the 0 to 2048 range is used.

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg Error
Decade x:  ffff Clock
Multiplier      = mmmmD
Clocks counted  = ccccD
Min Clock count = 1111D
Max Clock count = hhhhD
```

Where:

ssss is the Test Step in the range: 1 to 23.

hmsg is "Clock Frequency Counting",
"Multiplier Clock Divide by".

x is the selected Decade: 0, 1, 2, 3, 4, 5, 6.

ffff is the Clock frequency:

100	Mhz,
10	Mhz,
1	Mhz,
100	Khz,
10	Khz,
1	Khz,
100	hz.

mmmm is the current Multiplier value, range is 0 to 15.

cccc is the Number of clocks counted, range is 0 to 2048.

1111 is the Minimum number of clocks that could be counted for frequency.

hhhh is the Maximum number of clocks that could be counted for frequency.

Clock Board Diagnostic Subtest 12

TITLE: LEVEL RAMs DATA INTEGRITY TEST

TARGET LOGIC:
11E, 11F
11J
12F, 12G
12D, 10D, 12E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Level RAMs on the Clock Board are organized as 2048 x 4. They are written to by the Control Board, and read into the highest nibble of the word from port B0H of the Clock Board. The Level RAM's Data Integrity is checked by writing all 16 possible values to the RAM, and reading it back to verify that each Data Bit is functional and unique.

TEST STEP INFORMATION:

Data Integrity Test:

Step	Data	Address Locations
1	0000H	000 - 2047
2	0001H	000 - 2047
3	0002H	000 - 2047
4	0003H	000 - 2047
5	0004H	000 - 2047
6	0005H	000 - 2047
7	0006H	000 - 2047
8	0007H	000 - 2047
9	0008H	000 - 2047
10	0009H	000 - 2047
11	000AH	000 - 2047
12	000BH	000 - 2047
13	000CH	000 - 2047
14	000DH	000 - 2047
15	000EH	000 - 2047
16	000FH	000 - 2047

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Level RAM Data Integrity Error
Diagnostic Internal Clock
Byte Count     = ccccD
Data Read      = rrrrH
Data Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 16.

cccc is RAM byte count, (address) in the range of 0 to 2047.

rrrr is the Data Word read from the Level RAMS.

eeee is the Data Word expected from the Level RAMS which should be:

0000H,
0001H,
0002H,
0003H,
0004H,
0005H,
0006H,
0007H,
0008H,
0009H,
000AH,
000BH,
000CH,
000DH,
000EH,
000FH.

Clock Board Diagnostic Subtest 13

TITLE: LEVEL RAMs ADDRESS INTEGRITY TEST

TARGET LOGIC:

11D
11G, 12H
11E, 11F
11J
12F, 12G
12D, 10D, 12E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Level RAMs address is provided by thru counters which provide ten address lines which can address 1024 locations. An additional flip flop toggles back and forth between the two 10474 RAM Chips on each Write/Read, to allow the access of 2048 RAM locations.

The Level RAMs are tested for addressing uniqueness. This verifies that each of 2048 locations can be written to independently of all other locations.

TEST STEP INFORMATION:

Step 1. An incrementing Data pattern from 00H to 0FH is written to RAM, which repeats after each 16 locations. This verifies address lines A0, A1, A2 and A3.

Step 2. A Block Incrementing Data pattern from 00H to 0FH is written to RAM, which repeats after each 1024 locations. This verifies address lines A4, A5, A8 and A9.

Step 3. A Block Data pattern of 05H and 0AH is written to RAM, which covers all 2048 locations. This verifies that both of the 10474 RAM chips are written to.

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Level RAM Address Uniqueness Error
Diagnostic Internal Clock
Byte Count     = ccccD
Data Read      = rrrrH
Data Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 3.

cccc is RAM byte count, (address) in the range of 0 to 2047.

rrrr is the Data Word read from the Level RAMS.

eeee is the Data Word expected from the Level RAMS which should be:

0000H,
0001H,
0002H,
0003H,
0004H,
0005H,
0006H,
0007H,
0008H,
0009H,
000AH,
000BH,
000CH,
000DH,
000EH,
000FH.

Clock Board Diagnostic Subtest 14

TITLE: LEVEL RAMs CONTROL TEST

TARGET LOGIC:
11D
11G, 12H
11E, 11F
11J
12F, 12G
12D, 10D, 12E

Setup Latches in Subtest 2

TEST DESCRIPTION:

This Subtest verifies the functionality of the Control Logic associated with the Level RAM. The First Test Step checks the odd/even toggling of the level ram. Each Consecutive write operation to the RAM should toggle back and forth between the Even 10422 RAM chip, and the ODD 10422 RAM chip. A D latch is acting as a flip flop, and providing a write enable signal to only one RAM chip. An 0AH is written to all Even addresses and a 05H to all Odd.

The Second Test Step checks the Level RAM Write Enable/Disable function. The Level RAM is Write enabled when the signals ARMED and TRACED from the Control Board are both active.

This test does seven writes with the following conditions:

LEVEL	ARMED	TRACED	RESULT
0	1	1	0
1	1	1	1
2	1	0	not recorded
3	1	0	not recorded
4	1	1	4
5	1	1	5
5	0	1	not recorded

The Third Test Step checks the Recirculation feature of the Level RAM. The Data is read out of the 10422 RAM chips, looped back, and written back in. This is checked by writing an incrementing pattern into the RAM, and then reading it back, verifying the Data Integrity. The Data is then read back a second time and verified. On the second read, the Data is shifted by one Address location from the Recirculation.

The Fourth Test Step checks the Level RAM reset persistence by first filling the RAM with a value of 00H, then holding the reset line to the RAM address counters active, and hammering address location 0 by performing 2048 consecutive write operations. This should modify the Data Value at location 0, but the other 2047 locations should be unchanged. All 2048 locations are read back and verified.

TEST STEP INFORMATION:

Step	Data Even Locations	Data Odd Locations
1	000AH	0005H

Step	Data	Address	
2	0000H	000	
	0001H	001	
	0004H	002	
	0005H	003	
4	0005H	000	(0005H in Location 000 Only)
	0000H	001	
	0000H	002	
	•	•	
	•	•	
	0000H	2046	
	0000H	2047	

ERROR MESSAGES:

If an error occurs, the following message is displayed:-

```
* Test FAILED--Test Step   ssss
hmsg Error
Diagnostic Internal Clock
Byte Count     = ccccD
Data Read      = rrrrH
Data Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 4.

hmsg is Level RAM odd/even Toggle,
Level RAM Write enable/disable,
Level RAM Recirculation,
Level RAM Hammer/Addr Reset.

cccc is RAM byte count, (address) in the range of 0 to 2047.

rrrr is the Data Word read from the Level RAMS.

eeee is the Data Word expected from the Level RAMS which should be:

Odd/Even Test:

0005H,
000AH.

Write Disable/Enable Test:

0000H,
0001H,
0004H,
0005H.

Recirculation Test:

0000H,
0001H,
0002H,
0003H,
0004H,
0005H,
0006H,
0007H,
0008H,
0009H,
000AH,
000BH,
000CH,
000DH,
000EH,
000FH.

Hammer/Address Reset Test:

0005H,
0000H.

K450 LOGIC ANALYZER THRESHOLD/GPIB/RS-232 BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes the subtests executed on the K450 Threshold/GPIB/RS-232 Board, how Error Reporting is accomplished, and the concept behind each subtest program.

The Threshold/GPIB/RS-232 board diagnostics is divided into nine subtests, each of which is described individually on the following pages.

Subtest 1 is a DAC 7541 linearity test; subtest 2 is a DAC 7533 linearity test; subtest 3 is a Multiplexer/threshold test, subtest 4 is a serial I/O #1 test; subtest 5 is a serial I/O #2 test, subtest 6 is a 8253 counter mode 1 test; subtest 7 through subtest 9 are GPIB internal logic tests (the GPIB cable and operator intervene flag should not be set); subtest 7 is GPIB control status test; subtest 8 is GPIB MPU interrupt logic test; subtest 9 is GPIB data out register and parallel poll response register test.

Subtests 4 and 5 require a RS-232 wrap back connector installed to perform the test.

Only a part of the GPIB logic is checked in the GPIB internal test (subtests 7 through 9 check internal logic only). The external handshake logic is not tested.

NOTE: The TARGET LOGIC listed in each subtest description does not necessarily include all of the logic which could affect the operation of the subtest.

SUBTEST CATEGORY

1. DAC 7541 LINEARITY TEST
2. DAC 7533 LINEARITY TEST
3. MUX/THRESHOLD LOGIC TEST
4. SERIAL I/O #1 TEST
5. SERIAL I/O #2 TEST
6. TIMER 8253 COUNTER 0 TEST
7. GPIB INTERNAL CONTROL LINE TEST
8. GPIB INTERNAL MPU INTERRUPT LOGIC TEST
9. GPIB INTERNAL DATA REGISTER TEST

ERROR COUNT CATEGORY

1. SUBTEST 1 ERROR COUNT.
2. SUBTEST 2 ERROR COUNT.
3. SUBTEST 3 ERROR COUNT.
4. SUBTEST 4 ERROR COUNT.
5. SUBTEST 5 ERROR COUNT.
6. SUBTEST 6 ERROR COUNT.
7. SUBTEST 7 ERROR COUNT.
8. SUBTEST 8 ERROR COUNT.
9. SUBTEST 9 ERROR COUNT.

TITLE: DAC 7541 LINEARITY TEST

TARGET LOGIC: 5E, 6E, 8B, 7F, 8F, 8A
7A, 7E, Q2
and power supply +5.0V, -5.2V,-2.0V, AGND, -10.0V, +10.0V, VBB(+3.0V), +15V(divided as +7.5V), -15V(divided as -7.5V)

TEST DESCRIPTION:

The DAC 7541 linearity is tested by using the +10.0V, -10.0V, AGND, -2.0V, -5.2V, +5.0V, +3.0V, +7.5V, -7.5V, +0.00V, +1.30V and -1.40V as reference voltage, multiplexed through 7F as noninverting input, and writing data into 8A as inverting input until Q2 toggles its state. The ADC status is then verified by reading port 04H bit 0.

When the reference voltage is +10.0V, the DAC 7541 is initially programmed to -10.0V, so Q2 is turned on. The ADC status bit is equal to 0 which increments the DAC 7541 output voltage until the ADC status bit toggles its state.

When the reference voltages are -10.0V, AGND, -2.0V, -5.2V, +5.0V, +3.0V, +7.50V, -7.50V, DVM input, +1.30V, and -1.40V, the DAC 7541 is initially programmed to +10.0V, so Q2 is turned off. The ADC status bit is equal to 1, decrementing the DAC 7541 output voltage until the ADC status bit toggles its state.

TEST STEP INFORMATION:

Step	Reference Voltage	Initial 7541 Data Voltage	Initial ADC Status
1	+10.0V	0FFFH (-10.0V)	0
2	-10.0V	0000H (+10.0V)	1
3	AGND	0000H (+10.0V)	1
4	-2.0V	0000H (+10.0V)	1
5	-5.2V	0000H (+10.0V)	1
6	+5.0V	0000H (+10.0V)	1
7	VBB(+3.0V)	0000H (+10.0V)	1
8	+15V/2	0000H (+10.0V)	1
9	-15V/2	0000H (+10.0V)	1
10	DVM	0000H (+10.0V)	1
11	-ECL	0000H (+10.0V)	1
12	+TTL	0000H (+10.0V)	1

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
DAC 7541 Linearity Test
Voltage Expected    = see.eee
Voltage Lower Limit = suu.uuu
Voltage Upper Limit = s11.111
Actual Voltage Read = saa.aaa
ADC Status Expected = x
ADC Status Expected = y

Where zz should be in the range of 1 through 12

s should be + or -

ee.eee should be in the range of 00.000 through 10.000

uu.uuu should be 9.940, 10.235, 0.300, 2.350, 5.625, 4.820
                 2.700,  7.380, 7.980, 0.300, 1.000, 1.700

11.111 should be 10.240, 9.935, 0.300, 1.750, 5.025, 5.420
                 3.300, 7.980, 7.380, 0.300, 1.600, 1.100

aa.aaa should be in the range of 00.000 through 10.000

x,y should be 0 or 1
```

Threshold Diagnostic Subtest 2

TITLE: DAC 7533 LINEARITY TEST

TARGET LOGIC: 6D, 4B, 12B, 9B, 9A, 4A, 5A, 10A, 6F, 7A, 8A, Q2, 8F, 5E, 6E, 8B

TEST DESCRIPTION:

The DAC 7533 linearity is tested by using the DAC 7541 as reference voltage. VAR A and VAR B are multiplexed through 6F as the noninverting input of 7A, and continues incrementing or decrementing the VAR A or VAR B voltage by writing to port 08H or 0AH until the ADC output bit toggles its state.

When the DAC 7541 reference voltage is +10.0V, the DAC 7533 is initially programmed to -10.0V, so Q2 is turned off and the ADC status bit is equal to 1. When the DAC 7541 reference voltages are -9.980V, -5.0V, 0.00V, and +5.0V, DAC 7533 is initialized to +10.0V, so Q2 is turned on, and the ADC is equal to 0.

When VAR A and VAR B are tested, each DAC 7533 contains five voltage levels, -9.980V, -5.0V, 0.00V, +5.00V, and +10.00V.

TEST STEP INFORMATION:

Step	Reference Voltage	Initial 7533 Data Voltage	Initial ADC Status
1	-9.980V (7541)	0000H (VAR A +10.0V)	0
2	-5.0V (7541)	0000H (VAR A +10.0V)	0
3	-0.000V (7541)	0000H (VAR A +10.0V)	0
4	+5.0V (7541)	0000H (VAR A +10.0V)	0
5	+10.00V (7541)	0FFFH (VAR A -10.0V)	1
6	-9.980V (7541)	0000H (VAR B +10.0V)	0
7	-5.0V (7541)	0000H (VAR B +10.0V)	0
8	-0.000V (7541)	0000H (VAR B +10.0V)	0
9	+5.0V (7541)	0000H (VAR B +10.0V)	0
10	+10.00V (7541)	0FFFH (VAR B -10.0V)	1

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
DAC 7533 Linearity Test
Voltage Expected     = see.eee
Voltage Lower Limit = suu.uuu
Voltage Upper Limit = s11.111
Actual Voltage Read = saa.aaa
ADC Status Expected = x
ADC Status Expected = y
```

Where zz should be in the range of 1 through 10

s should be + or -

ee.eee should be in the range of 00.000 through 10.000

uu.uuu should be 10.220, 5.620, 0.500, 4.620, 9.740

11.111 should be 9.740, 4.620, 0.500, 5.620, 10.240

aa.aaa should be in the range of 00.000 through 10.000

x,y should be 0 or 1

Threshold Diagnostic Subtest 3

TITLE: THRESHOLD/MUX. LOGIC TEST

TARGET LOGIC: 4D, 5B, 1A, 1D, 1B, 1C, 2A, 2D
5F, 7A, 7E, 5E, 6E, 8B, 8A, 8F
and Q2.

TEST DESCRIPTION:

The Threshold/mux's logic is tested by using the TH0 through TH5 as reference voltages. These voltages are multiplexed through 5F and supplied as the noninverting input to 7A. The DAC 7541 is initially programmed to +10.0V and decrements the output voltages until the ADC output status bit toggles its state.

Reference voltages for -ECL, -TTL, -VAR A, and -VAR B are present for each threshold channel. The -ECL is +1.300V, -TTL is -1.400V, -VAR A is +5.0V, and -VAR B is -5.0V.

Testing occurs for threshold channels TH0 through TH5. The original ADC status bit should be 1 when the DAC 7541 is initialized to +10.0V.

TEST STEP INFORMATION:

Step	Logic	TH Channel	Initialized 7541 Voltage	Initial ADC Status
1	-ECL	0	+10.0V	1
2	-ECL	1	+10.0V	1
3	-ECL	2	+10.0V	1
4	-ECL	3	+10.0V	1
5	-ECL	4	+10.0V	1
6	-ECL	5	+10.0V	1
7	-VAR A	0	+10.0V	1
8	-VAR A	1	+10.0V	1
9	-VAR A	2	+10.0V	1
10	-VAR A	3	+10.0V	1
11	-VAR A	4	+10.0V	1
12	-VAR A	5	+10.0V	1
13	-TTL	0	+10.0V	1
14	-TTL	1	+10.0V	1
15	-TTL	2	+10.0V	1
16	-TTL	3	+10.0V	1
17	-TTL	4	+10.0V	1
18	-TTL	5	+10.0V	1
19	-VAR B	0	+10.0V	1
20	-VAR B	1	+10.0V	1
21	-VAR B	2	+10.0V	1
22	-VAR B	3	+10.0V	1
24	-VAR B	4	+10.0V	1
24	-VAR B	5	+10.0V	1

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Threshold/Mux. Logic Test
?????? Threshold Testing
TH Channel n Testing
Voltage Expected     = see.eee
Voltage Lower Limit = suu.uuu
Voltage Upper Limit = s11.111
Actual Voltage Read = saa.aaa
ADC Status Expected = x
ADC Status Expected = y
```

Where zz should be in the range of 1 through 24

?????? should be -ECL, -VAR A, -TTL, -VAR B

n should be in the range of 0 through 5

s should be + or -

ee.eee should be 1.300, 5.000, 1.400, 5.000

uu.uuu should be 0.980, 4.800, 1.720, 5.440

11.111 should be 1.620, 5.400, 1.080, 4.800

aa.aaa should be in the range of 00.000 through 10.000

x,y should be 0 or 1

Threshold Diagnostic Subtest 4

TITLE: SERIAL I/O PORT #1 TEST

TARGET LOGIC: 12D, 14A, 13A, 8E

TEST DESCRIPTION:

Serial I/O port #1 is tested by using USART #1 as a transmitter/receiver to transmit an 8 bit data pattern and receive the transmitted bytes through the wrap back, RS-232 connector within a specified time window (95% through 105%).

The RS-232 wrap back connector is configured as follows:

Pin 2, CTS (clear to send); short to Pin 3, RTS (request to send),

Pin 4, DSR (data set ready); short to Pin5, DTR (data terminal ready),

Pin 6, RxD (received data); short to Pin 20, TxD (transmitted data).

The following patterns are transmitted:

0AAH, 055H, 0CCH, 033H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

The following baud rates are tested:

110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

TEST STEP INFORMATION:

Test Step	Baud Rate	Data Pattern
1 through 12	110	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
13 through 24	150	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
25 through 36	300	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
37 through 48	600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
49 through 60	1200	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
61 through 72	1800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
73 through 84	2400	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
85 through 96	4800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
97 through 108	9600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H

ERROR MESSAGE:

1. If an error for transmitter buffer not empty occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Transmitter Buffer Not Empty
Testing Baud Rate     = bbbb
Status Byte Read      = rrH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

2. If an error for no character received occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
No Character Received
Testing Baud Rate     = bbbb
Status Byte Read      = rrH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

3. If an error for character received early occurs,the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Character Received Early
Testing Baud Rate       = bbbb
Minimum Expected Count  = eeeee
Actual Software Count   = ccccc
Received Data           = rrH
Transmitted Data        = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 1777, 1296, 641, 320, 156, 118, 79, 40, 20

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

4. If an error for character received late occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Character Received Late
Testing Baud Rate       = bbbb
Maximum Expected Count  = eeeee
Actual Software Count   = ccccc
Received Data           = rrH
Transmitted Data        = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 2303, 1701, 859, 417, 204, 155, 99, 53, 28

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

5. If an error for bad character occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Bad character Received
Testing Baud Rate       = bbbb
Received Data           = rrH
Transmitted Data        = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

Threshold Diagnostic Subtest 5

TITLE: SERIAL I/O PORT #2 TEST

TARGET LOGIC: 12E, 15B, 13B, 8E, 8D

TEST DESCRIPTION:

Serial I/O port #2 is tested by using USART #2 as a transmitter/receiver to transmit an 8-bit data pattern and receive the transmitted bytes through the wrap back RS-232 connector within a specified time window (95% through 105%)

The RS-232 wrap back connector is configured as follows:

Pin 2, CTS (clear to send); short to Pin 3, RTS (request to send),

Pin 4, DSR (data set ready); short to Pin 5, DTR (data terminal ready),

Pin 6, RxD (received data); short to Pin 20, TxD (transmitted data).

The following patterns are transmitted:

0AAH, 055H, 0CCH, 033H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

The following baud rates are tested:

110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

TEST STEP INFORMATION:

Test Step	Baud Rate	Data Pattern
1 through 12	110	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
13 through 24	150	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
25 through 36	300	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
37 through 48	600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
49 through 60	1200	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
61 through 72	1800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
73 through 84	2400	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
85 through 96	4800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
97 through 108	9600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H

ERROR MESSAGE:

1. If an error for transmitter buffer not empty occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Transmitter Buffer Not Empty
Testing Baud Rate     = bbbb
Status Byte Read      = rrH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

2. If an error for no character received occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
No Character Received
Tesing Baud Rate      = bbbb
Status Byte Read      = rrH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

3. If an error for character received early occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Character Received Early
Tesing Baud Rate         = bbbb
Minimum Expected Count   = eeeee
Actual Software Count    = ccccc
Received Data            = rrH
Transmitted Data         = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 1777, 1296, 641, 320, 156, 118, 79, 40, 20

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

4. If an error for character received late occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Character Received Late
Tesing Baud Rate        = bbbb
Maximum Expected Count  = eeeee
Actual Software Count   = ccccc
Received Data           = rrH
Transmitted Data        = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 2303, 1701, 859, 417, 204, 155, 99, 53, 28

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

5. If an error for bad character occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Bad character Received
Testing Baud Rate       = bbbb
Received Data           = rrH
Transmitted Data        = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

Threshold Diagnostic Subtest 6

TITLE: TIMER 8253 COUNTER 0 TEST

TARGET LOGIC: 13F, 8D, 8E and GATE/ logic from control board

TEST DESCRIPTION:

The timer 8253 counter 0 is tested by programming counter 0 to to mode 1 (programmable one shot mode), and triggering GATE0 from control board GATE/ logic. The counter 0 is then verified by reading the latched count after GATE0 been triggered.

The terminal count patterns tested are :

8000H, 4000H, 2000H, 1000H, 0800H, 0400H, 0200H, 0100H,
0080H, 0040H, 0020H, 0010H, 0008H, 0004H, 0002H, 0001H.

There are two methods for testing counter 0 in mode 1:

1. After loading terminal count, trigger GATE0 from low to high.

2. After loading terminal count, trigger GATE0 from low to high two times. The second trigger should cause the counter to reset to the terminal count value.

TEST STEP INFORMATION:

Test Step	Terminal Count Programmed	Rising Edge Trigger Pulses
1	8000H	1
2	4000H	1
3	2000H	1
4	1000H	1
5	0800H	1
6	0400H	1
7	0200H	1
8	0100H	1
9	0080H	1
10	0040H	1
11	0020H	1
12	0010H	1
13	0008H	1
14	0004H	1
15	0002H	1
16	0001H	1
17	8000H	2
18	4000H	2
19	2000H	2
20	1000H	2
21	0800H	2
22	0400H	2

23	0200H	2
24	0100H	2
25	0080H	2
26	0040H	2
27	0020H	2
28	0010H	2
29	0008H	2
30	0004H	2
31	0002H	2
32	0001H	2

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Timer 8253 Counter 0 Test
Programmable One Shot Mode
Testing Terminal count = ccccH
Expected High Count    = eeeeH
Expected Low Count     = 1111H
Actually Read Count    = rrrrH
```

where zz should be in the range of 1 through 32

cccc should be 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100,
0080, 0040, 0020, 0010, 0008, 0004, 0002, 0001.

eeee should be 7EC8, 3EC8, 1EC8, 0EC8, 06C8, 02C8, 00C8, FFC8,
FF48, FF08, FEE8, FED8, FED0, FECC, FECA, FEC9.

or 7FDD, 3FDD, 1FDD, 0FDD, 07DD, 03DD, 01DD, 00DD,
005D, 001D, FFFD, FFED, FFE5, FFE1, FEDF, FFDE.

1111 should be 7EB8, 3EB8, 1EB8, 0EB8, 06B8, 02B8, 00B8, FFB8,
FF38, FEF8, FED8, FEC8, FEC0, FEBC, FEBA, FEB9.

or 7FCD, 3FCD, 1FCD, 0FCD, 07CD, 03CD, 01CD, 00CD,
004D, 000D, FFED, FFDD, FFD5, FFD1, FFCF, FFCE.

rrrr should be in the range of 0000 through FFFF

TITLE: GPIB INTERNAL CONTROL LINES TEST

TARGET LOGIC: 15F, 17F, 16F, 16D

TEST DESCRIPTION:

The GPIB internal control lines are tested by writing the local control bit true. The control bit is then verified by reading back the control status bit.

There are 5 control lines being tested as follows:

'catn', 'cifc', 'cren', 'srq', 'end'.

NOTE: If the 'cacs' line is not true, the lines for 'catn', 'cifc', 'cren' and 'srq' are also not true.

TEST STEP INFORMATION:

Test Step	Control Bit
1	'catn'
2	'cifc'
3	'cren'
4	'srq'
5	'end'

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Internal Control Lines
Status Port Address 01H
Bit 7 through Bit 3 is :
atn  srq  ifc  ren  eoi
"????" and "cacs" Logic Test
"????" Status Expected = ssssssssB
"????" Status Read     = rrrrrrrrB
Falling Time Constant  = ttttt
"????" Status Expected = eeeeeeeeB
"????" Status Read     = vvvvvvvvB
Rising Time Constant   = ccccc
```

where: zz should be in the range of 1 to 5

???? should be catn, cifc, cren, srq, end.

ssssssss should be 10000000, 00100000, 00010000, 01000000, 00001000.

rrrrrrrr should be 00000000 through 11111111.

ttttt should be in the range of 00000 through 65535.

eeeeeeee should be 00000000.

vvvvvvvv should be 00000000 through 11111111.

ccccc should be in the range of 00000 through 65535.

NOTE: Falling and rising time constants are for diagnostic reference only.

TITLE: GPIB INTERNAL MPU INTERRUPT TEST

TARGET LOGIC: 15F, 17F, 16F, 15D, 17D, 21D, 17B,

18B, 19B, 20A, 20B, 21A, 19A, 20A, 16B, 21F

TEST DESCRIPTION:

The GPIB internal MPU interrupt is tested by writing local control bit true and local command bits true. The interrupt status bit is then verified by reading the interrupt status.

There are four MPU interrupt logic conditions being tested: 'tint', 'srint', 'nrint' and 'cint'. The 'lint' logic condition is associated with the GPIB external handshake function which is not tested.

The 'INTR1/' test is associated with the 'tint',' srint', 'nrint' and 'cint' interrupt logic conditions.

TEST STEP INFORMATION:

Test Step	MPU Interrupt Logic
1	'tint' and 'INTR1/'
2	'srint' and 'INTR1/'
3	'nrint' and 'INTR1/'
4	'cint' and 'INTR1/'

ERROR MESSAGE:

1. If an INTR1/ error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Internal Interrupt Line
gint/ lint tint cint nrint srint get/ nins/
"?????" Interrupt Line Test
GPIB INTR1/ Not Generated
```

where zz should be in the range of 1 through 4

????? should be tint, srint, nrint, cint.

2. If an interrupt status error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Internal Interrupt Line
gint/ lint tint cint nrint srint get/ nins/
"?????" Interrupt Line Test
Status 1 Expected   = aaaaaaaaB
Status 1 Read       = bbbbbbbbB
Status 2 Expected   = cccccccB
Status 2 Read       = ddddddddB
Status 3 Expected   = eeeeeeeeB
Status 3 Read       = ffffffffB
Status 4 Expected   = gggggggB
Status 4 Read       = hhhhhhhhB
```

where zz should be 1 through 4

????? should be tint, srint, nrint, cint

aaaaaaaa should be 10000010.

cccccccc should be 11111111, 10000010.

eeeeeeee should be 00100010, 00000110, 00001010, 00010010.

gggggggg should be 10000010.

bbbbbbbb should be in the range of 00000000 through 11111111

dddddddd should be in the range of 00000000 through 11111111

ffffffff should be in the range of 00000000 through 11111111

hhhhhhhh should be in the range of 00000000 through 11111111

Threshold Diagnostic Subtest 9

TITLE: GPIB INTERNAL DATA REGISTER TEST

TARGET LOGIC: 18E, 19E, 18D, 19D, 20E, 21E, 20F

TEST DESCRIPTION:

The GPIB internal data register is functionally tested by writing a data byte pattern to the data register or parallel poll response register. The data is then verified by reading the data from the input register.

There are 12 data patterns tb be tested :

0AAH, 55H, 0CCH, 33H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

There are two output registers to be tested :

1. Data output register (18E)

2. Parallel poll response register (19E).

TEST STEP INFORMATION:

Test Step	Register Under Test	Data Pattern
1	data output register	0AAH
2	data output register	55H
3	data output register	0CCH
4	data output register	33H
5	data output register	01H
6	data output register	02H
7	data output register	04H
8	data output register	08H
9	data output register	10H
10	data output register	20H
11	data output register	40H
12	data output register	80H
13	parallel poll response	0AAH
14	parallel poll response	55H
15	parallel poll response	0CCH
16	parallel poll response	33H
17	parallel poll response	01H
18	parallel poll response	02H
19	parallel poll response	04H
20	parallel poll response	08H
21	parallel poll response	10H
22	parallel poll response	20H
23	parallel poll response	40H
24	parallel poll response	80H

ERROR MESSAGE:

1. If an error occurs in the data output register, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Data Register Test
Data Out Register Testing
Data Register Expected = eeH
Data Register Read     = rrH
```

where zz should be in the range of 1 through 24

ee should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

rr should be 00 through FF

2. If an error occurs in the parallel poll response register, the following displayed:

```
* Test FAILED -- Test Step zz
GPIB Data Register Test
Parallel Poll Response
Data Register Expected = eeH
Data Register Read     = rrH
```

where zz should be in the range of 1 through 24

ee should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

rr should be 00 through FF

K450 STORAGE CONTROLLER BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes subtests executed on the K450 Storage Controller Board, how error reporting is done, and the concept behind each subtest program.

The K450 Storage Controller Board has future provisions for installing a UART. This Diagnostic does not test any of the UART components.

There are six subtests written for the Storage Controller Board. Each of these subtests is described individually on the following pages. Parameters for Loop on Error, Error Count, and Pass Count Update are incorporated into each subtest.

All error messages are preceded by a "*". The information messages use the ">" prefix.

Early exit of each subtest is accomplished by pressing the STOP key.

ASSUMPTIONS

This series of tests assumes that two other boards are installed in the K450 and are functional, an operational MPU Board as well as the Keyboard/Display Board must be present.

SUBTEST CATEGORIES

1. 6116 Data Integrity Test
2. 6116 Address Integrity Test
3. FDC Seek Test
4. Fixed FDC Write/Read Test
5. Random FDC Write/Read Test
6. FDC/DMA Address Logic Test

ERROR COUNT CATEGORIES

1. Subtest 1
2. Subtest 2
3. Subtest 3
4. Subtest 4
5. Subtest 5
6. Subtest 6
7. Seek Command Error Count
8. Recalibrate Command Error Count
9. Write Command Error Count
10. Read Command Error Count
11. Drive A Error Count
12. Drive B Error Count
13. Side 0 Error Count
14. Side 1 Error Count
15. Soft Error Count
16. Hard Error Count
17. Not Ready Error Count
18. Head Address Error Count
19. Ready Changed State Error Count
20. Missing Address Mark Error Count
21. Write Protected Error Count
22. Sector Not Found Error Count
23. FDC Overrun Error Count
24. FDC Int Timout Error Count
25. Access beyond End of Track Error Count
26. Missing Data Address Mark Error Count
27. Bad Track Error Count
28. Wrong Cylinder Error Count
29. Data Error CRC Error Count
30. Control Mark : Deleted Data Encountered Error Count
31. Unformatted Diskette Error Count
32. Diagnostic Program Error Count

TITLE: 6116 DATA INTEGRITY TEST

PURPOSE:

This subtest confirms the ability of the DMA hardware to sucessfully write data into the 4K area of 6116 RAM. The integrity of the RAM is checked by running several patterns through the Memory.

The RAM is not directly addressable, all access is through the DMA controller.

TARGET HARDWARE: 5D, 5E, 5F, 5H, 6E, 6F, 7E

TEST DESCRIPTION:

It is not possible to Write directly to the 6116 RAMs. All access is through the DMA controller. Data is written to the DMA controller and the controller passes it on to the RAM. Reading is accomplished through the same type of cycle. Various Data patterns are written to the RAM then Read back. If a miscompare occurs, an Error message is printed.

TEST STEP INFORMATION:

Test Step	Value Written
1	0
2	AAH
3	55H
4	CCH
5	33H
6	01H
7	02H
8	04H
9	08H
10	10H
11	20H
12	40H
13	80H

ERROR MESSAGE:

If any errors are detected, this subtest displays the following message:

```
* Test FAILED--Test Step    xx
RAM Data Error
Value Written  = aaH
Value Read     = bbH
Address Count  = ccccH
DMA Status     = ddH
```

where xx = test step number
aa = 00 - FF
bb = 00 - FF
cccc = 0000 - 0FFF
dd = 00 - FF

TITLE: 6116 ADDRESS INTEGRITY TEST

PURPOSE:

The purpose of this test is to selectivly write 1 byte of Data into the 4K of RAM on the storage controller board which has been preset to zero. Verification is then made to confirm the only place the RAM is written to is the indicated Address.

TARGET HARDWARE: 5D, 5E, 5F, 5H, 6E, 6F, 7E

TEST DESCRIPTION:

It is not possible to Write directly to the 6116 RAMs. All access is through the DMA controller. Data is written to the DMA controller and the controller passes it on to the RAM. Reading is accomplished through the same type of cycle. Various Data patterns are written to the RAM then Read back. If a miscompare occurs, an error message is printed.

All of the RAM in this test is preset to zero then the indicated Address is written with the value 0aah. All of RAM is then Read to verify the written Data. If a miscompare is detected then an error message is displayed.

TEST STEP INFORMATION:

Test Step	Indicated Address
1	0000H
2	0001H
3	0002H
4	0004H
5	0008H
6	0010H
7	0020H
8	0040H
9	0080H
10	0100H
11	0200H
12	0400H

ERROR MESSAGES:

If any errors are detected, this subtest displays the following message:

```
* Test FAILED--Test Step    xx
All Storage Controller RAM Set to Zero.
Wrote aaH to Address bbbbH
Read  ccH at Address ddddH
```

where xx = test step number
aa = 00 - FF
bbbb = 0000 - 0FFF
cc = 00 - FF
dddd = 0000 - 0FFF

Storage System Controller Subtest 3

TITLE: FDC SEEK TEST

PURPOSE:

The purpose of this subtest is to verify operation of the seek process on one or both Disk Drives.

TARGET HARDWARE: 2H, 3D, 3E, 3F, 3H, 4C, 4D, 4E, 4F, 7D, 7F

TEST DESCRIPTION:

The FDC is commanded to perform seeks to the given Track as outlined below. Tracks are accessed from Track 0 to 39, and 39 to 0. Finally, an alternating pattern of seeks spiraling from outermost to innermost Tracks is performed.

As these operations are sent to the FDC controller, the status of the controller is monitored. If an error is detected, an error message is displayed.

This operation is repeated for all selected Drive and Side options selected.

TEST STEP INFORMATION:

Test Step Number	Drive/Side	Disk Action
1 - 40	A / 0	seek 0-39
41- 80	A / 0	seek 39-0
81- 120	A / 0	spiral inward
121-160	A / 1	seek 0-39
161-200	A / 1	seek 39-0
201-240	A / 1	spiral inward
241-280	B / 0	seek 0-39
281-320	B / 0	seek 39-0
321-360	B / 0	spiral inward
361-400	B / 1	seek 0-39
401-440	B / 1	seek 39-0
441-480	B / 1	spiral inward

ERROR MESSAGES:

If any errors are detected, this subtest displays the error messages found in Appendix 1.

Storage System Controller Subtest 4

TITLE: FDC WRITE/READ TEST

PURPOSE:

The purpose of this subtest is to verify the Storage Controller Board's capability to Write and Read back information on all Tracks of the Disk Drive.

TARGET HARDWARE: 2H, 3D, 3E, 3F, 3H, 4C, 4D, 4E, 4F, 7D, 7F

2A, 2B, 2C, 3A, 3B

TEST DESCRIPTION:

The FDC is Commanded to Write Data to all Tracks on a given Disk surface on a sector by sector basis. If the Track written to is either Track 0 or Track 39 then all sectors are written to. On other Tracks, only sector 1 is actually tested. The Data is then Read back and compared to the pattern written. If a miscompare occurs, an error message is displayed.

As these operations are sent to the FDC controller, the status of the controller is monitored and if an error is detected an error message is displayed. This operation is repeated for all selected Drive and Side options selected.

TEST STEP INFORMATION:

Test Step Number	Drive/Side	Disk Action
1 - 40	a/0	Write/Read/compare
41 - 80	a/1	Write/Read/compare
81 - 120	b/0	Write/Read/compare
121 - 160	b/1	Write/Read/compare

ERROR MESSAGES:

If any errors are detected, this subtest will display the following message:

```
* Test FAILED--Test Step    xxx
Sector Compare Error
Track Number          = 0aa
Sector Number         = 00b
Address Within Sector = 0ccch
Wrote ddh
Read  eeh
```

where xxx = test step number
aa = 0 - 39
bb = 0 - 8
ccc = 000 - FFF
dd = 00 - FF
ee = 00 - FF

NOTE: Also see Appendix 1.

Storage System Controller Subtest 5

TITLE: RANDOM FDC WRITE/READ

PURPOSE:

The purpose of this subtest is to verify the Storage Controller Board's capability to Write and Read back information on 63 random locations of the Disk Drive.

TARGET HARDWARE: 2H, 3D, 3E, 3F, 3H, 4C, 4D, 4E, 4F, 7D, 7F

2A, 2B, 2C, 3A, 3B

TEST DESCRIPTION:

This subtest generates random Data and performs 63 random Read/Write cycles. As Data is written it is then Read back and compared. If a miscompare of data occurs, it is reported via an error message. As these operations are sent to the FDC controller, the status of the controller is monitored and if an error is detected an error message is displayed. This operation is repeated for all selected Drive and Side options selected.

TEST STEP INFORMATION:

Test Step Number	Drive/Side	Disk Action
1- 64	a/0	Write/Read/compare
65- 126	a/1	Write/Read/compare
127- 190	b/0	Write/Read/compare
191- 254	b/1	Write/Read/compare

ERROR MESSAGES:

If any errors are detected, this subtest will display the following message:

```
* Test FAILED--Test Step    xx
Sector Compare Error
Track Number          = 0aa
Sector Number         = 00b
Address Within Sector = cccH
Wrote ddH
Read  eeH

where     xx = test step number
          aa = 0 - 39
          bb = 0 - 8
          ccc = 000 - FFF
          dd = 00 - FF
          ee = 00 - FF
```

NOTE: Also see Appendix 1.

Storage System Controller Subtest 6

TITLE: FDC/DMA ADDRESS LOGIC

PURPOSE:

The purpose of this subtest is to verify integrity of the Address Counters logic between the DMA controller and the floppy Disk controller.

TARGET HARDWARE: 2H, 3D, 3E, 3F, 3H, 4C, 4D, 4E, 4F, 7D, 7F

2A, 2B, 2C, 3A, 3B

TEST DESCRIPTION:

The Data pattern, 0aah, is written to the indicated Addresses on the Storage Controller Board. The entire RAM contents are written to Track 22 on the first available Drive. The RAM is zeroed out then a Read sector Command is issued. The RAM is then analyzed to determine if the DMA controller has placed Data in the original locations.

As these operations are sent to the FDC controller, the status of the controller is monitored and if an error is detected an error message is displayed.

This operation is repeated for all selected Drive and Side options selected.

TEST STEP INFORMATION:

Test Step	Address Range
1	0000H - 01FFH
2	0001H - 0200H
3	0002H - 0201H
4	0004H - 0203H
5	0008H - 0207H
6	0010H - 020FH
7	0020H - 021FH
8	0040H - 023FH
9	0080H - 027FH
10	0100H - 02FFH
11	0200H - 03FFH
12	0400H - 05FFH
13	0800H - 09FFH
14	1000H - 11FFH

ERROR MESSAGES:

If any errors are detected this subtest will display the following message:

```
* Test FAILED--Test Step    xx
All storage Controller RAM set to Zero.
Unique Testing Address Range = llllH to hhhhH
Data in Address Range = ddH
Checking Data at Address = aaaaH
Data Expected            = eeH
Data Read                = rrH


where     xx = test step number
          llll = 0000 - 0FFF
          hhhh = 0000 - 0FFF
          dd = AAH
          aaaa = 0000 - 0FFF
          ee = 00 - FF
          rr = 00 - FF
```

NOTE: Also see Appendix 1.

Error Messages Common to all Disk Activity:

Subtests 3-6 all use a common routine for Disk operations which generate the following error message:

```
* Test FAILED--Test Step    aa
Retrying Disk Command
Retry Count = b
Disk Command: c
Drive  = d
Head   = e
Track  = 0ff
Sector = g
msg
```

where aa = test step number
b = number of times Disk Command has been attempted
c = seek Command,
Read id Command,
recalibrate Command,
Write Track Command,
Write sector Command,
Read Track Command,
Read sector Command.
d = a or b
e = 0 or 1
ff = 0 to 39
g = 1 to 8

msg = Disk Drive Not Ready.
Head Address Error.
During Command, Ready Changed State.
Missing Address Mark.
Write Protected.
Sector Not Found.
FDC Over-run Error.
Data Error (CRC).
FDC Interrupt Timeout Error.
Access Beyond End of Track.
Missing Data Address Mark.
Bad Track.
Wrong Cylinder.
Data Error (crc).
Control Mark: Deleted Data Encountered.
Not a Formatted Disk.

Chapter 6

OPTIONS INSTALLATION

GENERAL

This chapter describes procedures for installing the K450 Input Expansion Option and K450 Disk Storage System (DSS) Option equipment at the user's site. This optional equipment is provided in kit form for users who desire to expand the operating capabilities of their existing equipment. Once installed, the K450 automatically recognizes the new hardware configuration when powered up. The Configuration Screen indicates which optional features are available for the user. The the system responds when the new features are accessed. The following kits are available:

- o K450 Input Expansion Option Kit, Part Number 0121-0030-10
- o K450 Disk Storage System Option Kit, Part Number 0114-0468-20

Each kit contains installation instructions for the equipment option. The internal wiring harness assemblies that interface with optional printed circuit board edge connectors are installed in the K450 chassis by the factory to facilitate the addition of options by the user. These harness assemblies are located at the upper right-hand side of the card cage. Individual cables contained within the harness are labeled for identification. The entire bundle of cables is exposed when the top cover is removed from the K450 chassis.

The K450 Input Expansion Option kit contains a Data printed circuit board assembly and a set of input cables, probes and grabbers which provide 16 additional inputs to the K450. A separate kit is required for Input Sections B and C.

The DSS Option Kit contains the dual disk drive assembly and mounting hardware which includes a power cable assembly and signal cable assembly that must be installed by the user. The associated diagrams and wiring details are described in the installation procedure. The DSS functional description and operation are described in a separate K450 User's Manual Addendum, Publication Number 0121-0084-10, which is included in the kit.

Card Cage Arrangement

The board ejector tabs on each printed circuit board are numbered to correspond to the assigned slot location in the card cage. For the most part, the assigned board is dedicated to reside in its assigned slot location except where specified below for the three Data Boards. The installed boards are secured in the card cage by a slotted retainer bar, which is fastened to the top of the card cage by two screws.

Data Board Input Configurations

Three Data Boards reside in slot locations A2, A3 and A4. The ejector tabs are not numbered because each board is identical and interchangeable for these slots. Each slot location has a particular Input Section as described in the installation procedure.

The K450 unit configured for 16 Inputs (Section A) uses one Data Board installed in slot location A4. Units configured for 32 inputs (Sections A and B) use two Data Boards installed in slot locations A4 and A3.

Units configured for 48 inputs (Sections A, B, C) use another Data Board installed in slot location A2. The expansion for Input Section C requires jumper connections on the Clock Board to be repositioned to convert the BR and BS Sample Clocks into Latch Clocks as described in the installation procedure.

INSTALLATION OF K450 INPUT EXPANSION OPTION

Unpacking and Inspection

The Data Board and probes supplied for the Expansion Option provide 16 additional channels for Input Sections B or C. A separate kit is required to install the option at each Input Section. All hardware items required to install and operate this option at the user's site are contained in the kit. The components provided for each kit are described in Table 6-1.

Table 6-1. Expansion Option Components

QUANTITY	PART NUMBER	DESCRIPTION
1	0121-0015-10	Data Board, Printed Circuit Board Assembly
2	0117-0294-30/-50	Input Cable Set
22	7100-0116-10	Grabbers
2	0117-0099-10	Probe Subassembly
1	0121-0031-10	Instruction Sheet
1	0117-0740-10	Label, Active Probe Pod
1	0117-0208-01	Label, Output Cable

All equipment was thoroughly inspected and checked out at the factory prior to packaging for shipment. After removing the equipment from its shipping container, inspect for damage that might have occurred during shipping. Refer to the shipping papers to verify all items were received.

If equipment received from the carrier is incomplete or damaged, do not install the equipment. File a claim with the shipping firm immediately, and notify Gould Inc., Design and Test Systems Division Customer Service department at once. Gould Inc., DTD will arrange for replacement of the equipment without waiting for settlement of the claim against the carrier.

Installation Procedure

Prior to beginning the option installation, position the carrying handle of the K450 to the front of the machine so that the unit rests flat on the work surface.

```
* * * * * * * * * * * * * * * * * * * * *
*                                       *
*              WARNING                  *
*                                       *
*  Disconnect the 115/240 Vac source    *
*  to the K450 prior to installing      *
*  any options. Otherwise, a shock      *
*  hazard exists. Also, high voltage    *
*  is present on the CRT and Display    *
*  Board.                               *
*                                       *
* * * * * * * * * * * * * * * * * * * * *
```

The following steps outline the procedure necessary to install the Data Board for Input Section B or C on K450 units that do not contain the DSS option. If the DSS Option is present in lieu of the top chassis cover, refer to the DSS Option Removal Procedure at the end of this section.

1. Remove the six Phillips-head screws securing the top cover to the chassis, and carefully lift cover from the unit.

2. Remove the two screws that secure the card retainer bar to the top of the card cage and lift it from the chassis. The card cage arrangement is shown in Figure 6-1.

3. Carefully disconnect the cable harnesses from board sockets at card cage locations A3, A4 and A5, noting which sockets are associated with each cable.

4. Position the Expansion Option Data Board with the solder side toward the power supply of the unit. Carefully insert the Data Board into the designated card slot, A2 for Section C Inputs or A3 for Section B Inputs (refer to Figure 6-1). Ensure the Data Board is seated firmly in the motherboard sockets.

5. If the Input Section C Data Board is being installed, remove the Clock Board from the card cage to change the jumper connections.

   Rearranging the jumper connections enables the Input Section C clock inputs and routes the BR and BS clocks into the user specified Latch Clock equation. The K450 software will not recognize clock inputs at Section C unless these jumper connections are completed.

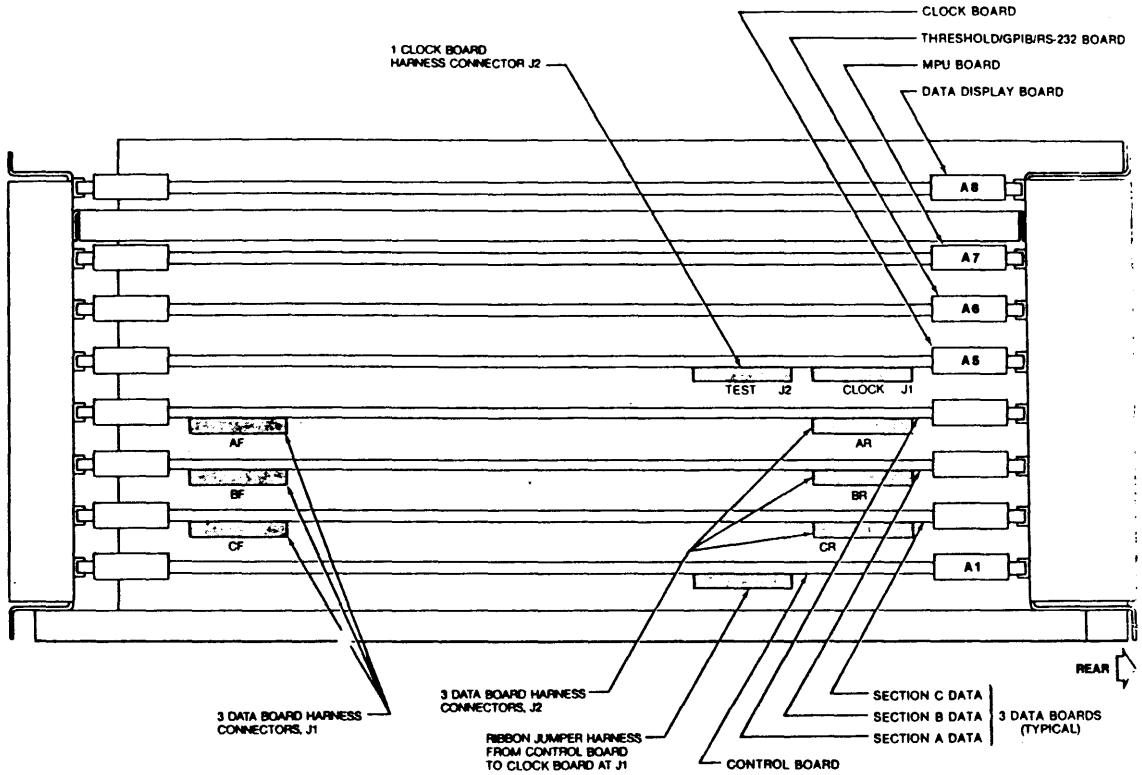


Figure 6-1. K450 Card Cage Arrangement, Top View

The eight jumpers are contained at board location column 3, row K. These jumpers are to be relocated to pins from the common/lower row to pins at the common/upper row, to provide the following connection points:

T1-T2, T4-T5, T7-T8, T10-T11

T13-T14, T16-T17, T19-T20, T22-T23

6. Replace the card cage retainer bar and secure with the two screws.

7. Locate the unattached ribbon cables BF and BR (for Section B Data Board) or CF and CR (for Section C Data Board). See Figure 6-2. Install the ribbon cable connector on J1 near the front of the machine. The dark-brown wire braid on the connector should be located to the front of the machine.

NOTE: If J1 is installed backwards, the equipment is not damaged. The data at D0 is displayed on channel D7. Reversing the connector corrects this condition.

Install the ribbon cable connector on J2 near the rear end of the machine. See Figure 6-2.

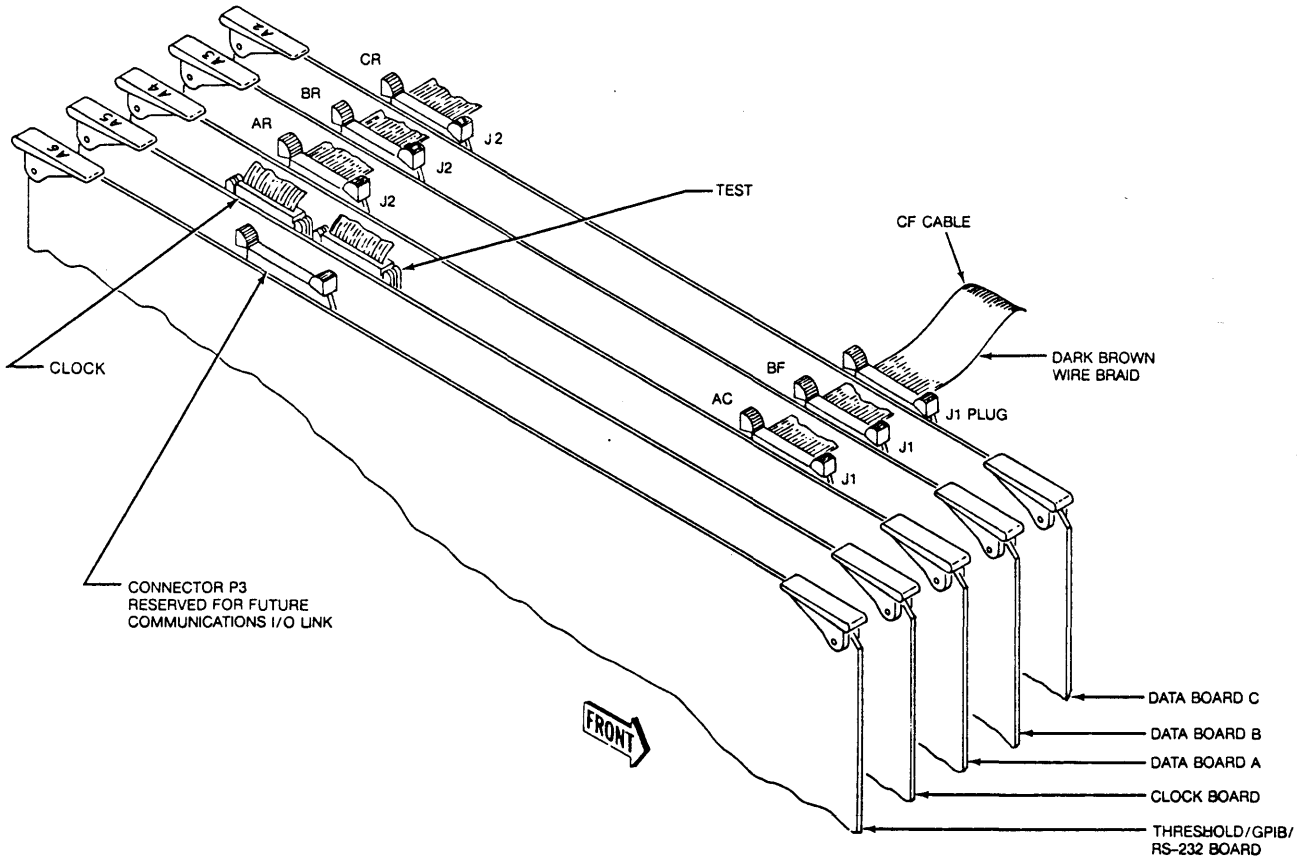


Figure 6-2. K450 Ribbon Cable Connections at Card Cage

8. Replace the harness connectors removed in Step 3. Ensure each harness is connected to its socket. See Figure 6-2.

9. Ensure the harness cables are properly positioned and do not interfere with reinstallation of the top cover. Reinstall the top cover.

10. Reinstall the six retaining screws.

11. Reconnect the 115/240 Vac source to the K450. Operation of the K450 with 32 or 48 expanded inputs is described in the K450 User's Manual.

Removal of DSS Option Assembley

The DSS assembly must be removed from the K450 chassis to gain access to the card cage or other components. Use the following procedure to accomplish removal:

1. Remove the four Phillips-Head screws securing the top cover to the DSS assembly, and carefully lift the top cover from the DOS housing.

2. Remove the two screws that secure the DSS base and ground connection lug to the top of the K450 chassis.

3. Remove the four screws (2 on each side) that secure the DSS assembly to the K450 chassis.

NOTE: Disconnect the power harness and I/O ribbon cable at the DSS assembly to remove it from the K450 chassis.

4. Lift the DSS assembly from the K450 chassis. Hold the DSS assembly suspended and disconnect the power harness plug. Disconnect the I/O ribbon cable from the interface connector, J3, on the Controller Board in the DSS assembly. Pull the I/O cable through the access slot under the printed circuit board so that the DSS assembly is separated from the K450 chassis.

5. Position the DSS assembly on its side to the left of the K450 chassis. The front of the DSS assembly should be located at the front of the K450 chassis.

6. Reinstall the DSS assembly by reversing the removal procedure. Ensure that the I/O signal cable is routed through the access slot under the printed circuit board. Ensure it is properly folded at the Controller Board connector (J3). Ensure it does not bind, nor interfere with other internal components, when the DSS assembly is positioned on top of the K450 chassis.

INSTALLATION OF DSS OPTION

Unpacking and Inspection

The Disk Storage System Option allows the user to store K450 set up parameters, trace information and data for later retrieval, and to load and execute the disk-based diagnostic routines. All hardware items required to install and operate the Disk Storage System (DSS) option at the user's site are shipped in packaged units. External interface cables are included for connecting all components in the system. Components supplied for the DSS Option are described in Table 6-2.

Table 6-2. DSS Option Components

QUANTITY	PART NUMBER	DESCRIPTION
1	0114-0468-20	DSS Option Assembly
1	0121-0084-10	K450 Disk Operating System User'S Manual Addendum
1	0121-0065-10	K450 Storage Operating System Diskettes (Set of 2)
1	0121-0094-20	K450 DSS Option Instruction Sheet

All equipment was thoroughly inspected and checked out at the factory prior to packaging for shipment. After removing the equipment from its shipping container, inspect for scratches, dents or other damage that might have occurred during shipping. Refer to the shipping papers to verify that all items were received.

If equipment received from the carrier is incomplete or damaged, do not install the equipment. File a claim with the shipping firm immediately, and notify Gould Inc., Design and Test Systems Division Customer Service department at once. Gould Inc., DTD will arrange for repair or replacement of the equipment without waiting for a settlement of the claim against the carrier.

Installation Procedure

Prior to beginning the option installation, position the carrying handle of the K450 to the front of the machine so that the unit rests flat on the work surface.

```
* * * * * * * * * * * * * * * * * * * * *
*                                         *
*              WARNING                    *
*                                         *
* Disconnect the 115/240 Vac source       *
* to the K450 prior to installing         *
* any options. Otherwise, a shock         *
* hazard exists. Also, high voltage       *
* is present on the CRT and Display       *
* Board.                                  *
*                                         *
* * * * * * * * * * * * * * * * * * * * *
```

The following steps outline the procedure necessary to install the DSS option on the K450 chassis:

1. Remove the six Phillips-head screws securing the top cover to the K450 chassis, and carefully lift the cover from the unit.

2. Remove the four Phillips-head screws securing the top cover to the DSS assembly, and carefully remove the top cover. Note the position of the ribbon cable connectors to the disk drives (see Figures 6-3 and 6-4). Disconnect the I/O ribbon cable connectors from the Disk Controller Board and remove the cable from the DSS assembly. (This helps to position and fold the I/O cable after the DSS assembly is placed on the K450 chassis.)

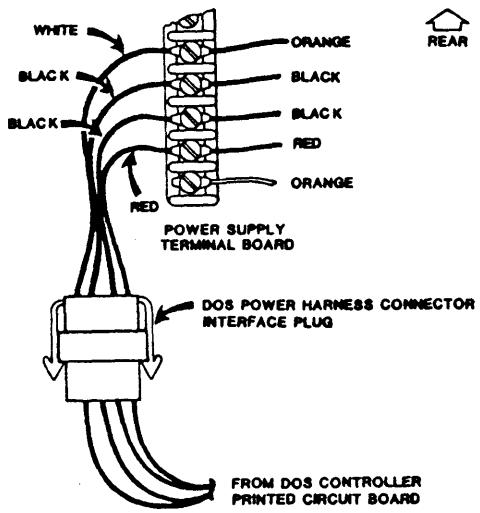


Figure 6-3. DSS Power Supply Harness Connection, Top View

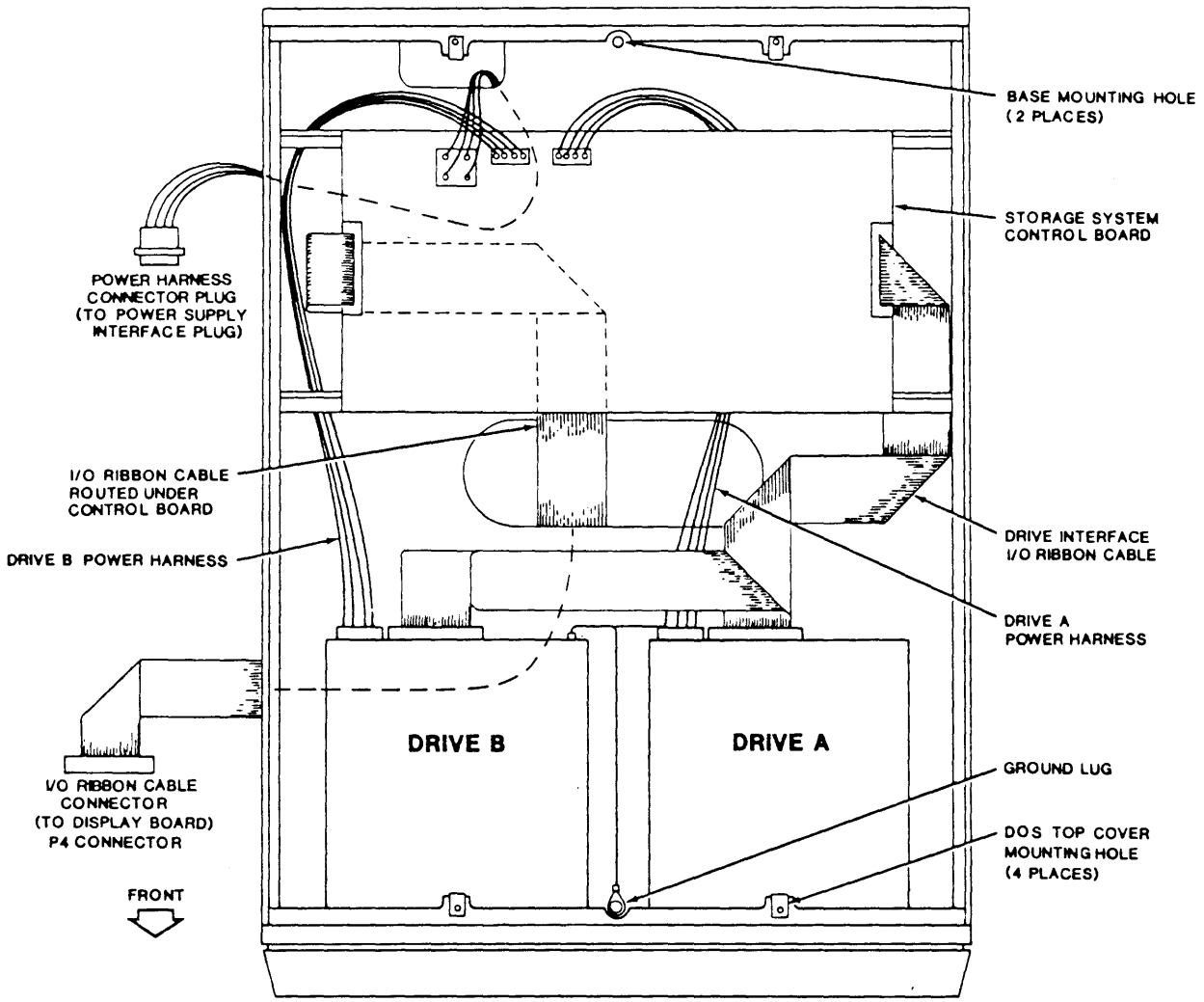


Figure 6-4. K450 DSS Assembly, Top View With Cover Removed

3. Connect the single ribbon connector to the Data Display Board connector P4, located near the center of the unit. See Figure 6-5. Remove the card cage retainer bar and raise the Data Display Board approximately 2 inches in the card cage to gain access to the P4 connector. Pin 1 is at the top of connector P4.

4. Position the DSS assembly on the K450 chassis and route the I/O ribbon cable through the access slot in the base of the DSS assembly. Do not connect the I/O ribbon cable at this time.

5. Locate the DSS power harness connector cable near the power supply which is installed by the manufacturer for interfacing the DSS option (See Figure 6-3). Connect the power harness connector plug from the DSS unit to the power supply harness connector through the rear access slot.

6. Fold the I/O ribbon cable under the Disk Controller Board so that it is routed to the left Controller Board connector, J3. See Figure 6-4. Pin 1 is at the front of connector J3. Connect the I/O ribbon cable to the Controller Board connector. Ensure that no cables interfere with the final positioning of the DSS assembly, and seat the assembly on the top of the K450 chassis.

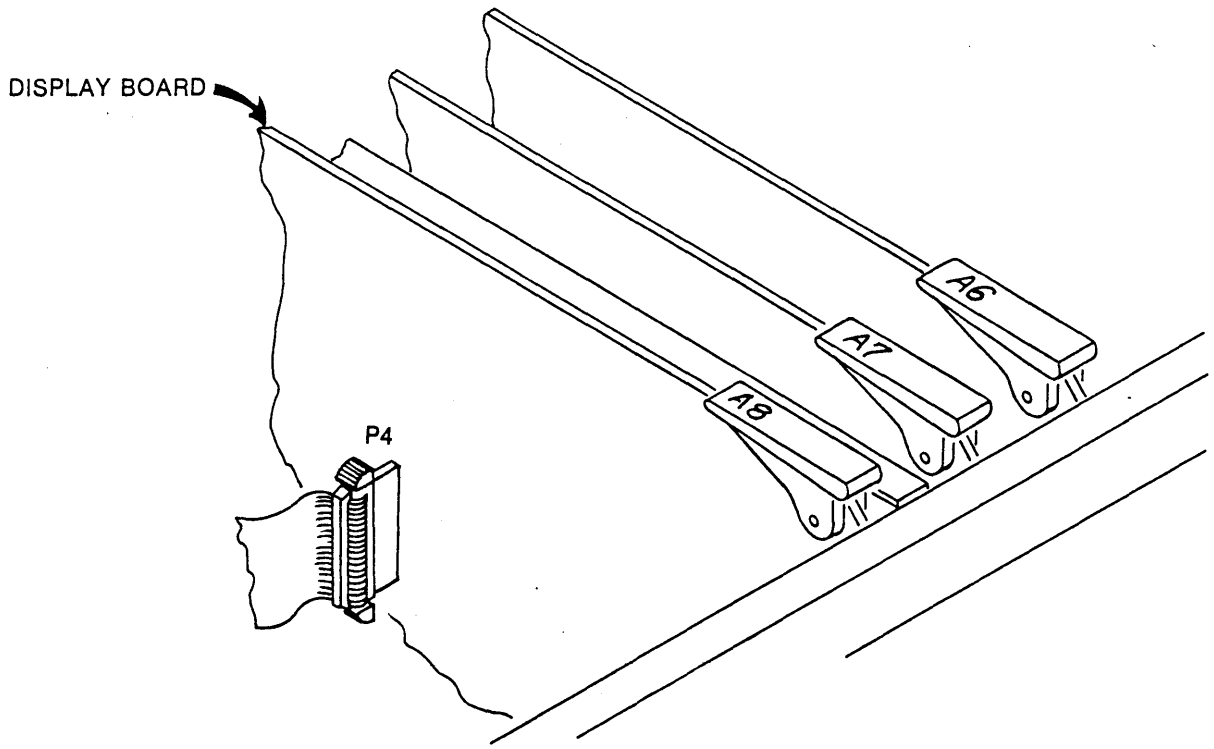


Figure 6-5. Disk Drive I/O Ribbon Cable Connection

7. Install the six retaining screws, the two screws that secure the DSS Base and ground lug to the top of the K450 chassis. Install the four screws that secure the sides of DSS unit to the K450 chassis.

8. Reinstall the DSS top cover with the four retaining screws.

9. Reconnect the 115/240 Vac source to the K450 unit.

Chapter 7

SCHEMATICS AND DRAWINGS

GENERAL

This chapter contains Schematic Diagrams, Assembly Drawings, Parts Lists and Wire Lists for the K450 Logic Analyzer. The drawings are arranged sequentially by drawing number.

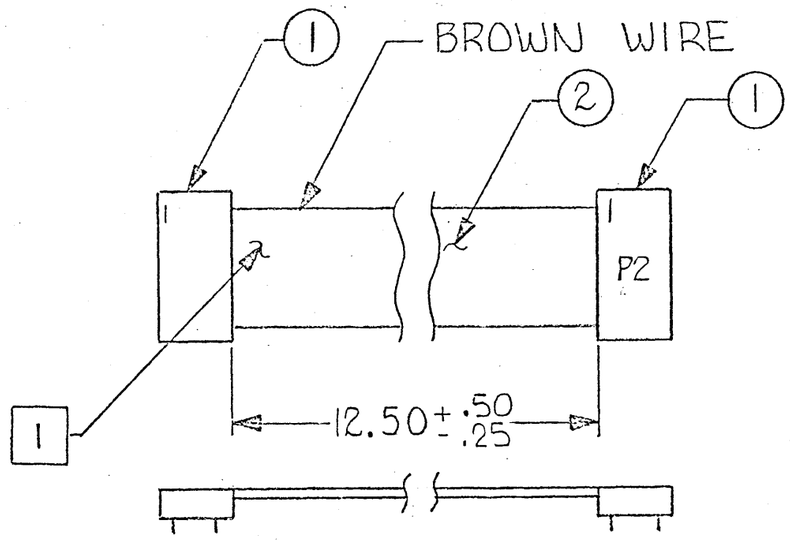
LIST OF DRAWINGS

The following drawings are provided in this chapter:

DRAWING NUMBER	DESCRIPTION
0112-0204-10	Keyboard Cable Assembly
0114-0120-10	Control Board Assembly
0114-0121	Control Board Schematic
0114-0170-30	Threshold/GPIB/RS-232 Board Assembly
0114-0171	Threshold/GPIB/RS-232 Board Schematic
0114-0468-20	DOS Option Assembly
0114-0475-10	DOS Controller Board Assembly
0114-0476	DOS Controller Board Schematic
0114-2010-60	Display Board Assembly
0114-2011	Display Board Schematic
0114-2024-10	Mother Board/Power Supply Cable Assembly
0114-3010-60	Display Board Assembly
0117-0021-10	Crt Cable Assembly
0117-0040-30	Keyboard P.C.B. Assembly
0117-0099-10	Probe Subassembly
0117-0117-10	Power Switch Cable Assembly
0117-0123-10	CRT Assembly
0117-0133-10	Chassis Ground Cable Assembly
0117-0294-30, -50	Input Cable Set
0117-0540-10	MPU Board Assembly
0117-0541	MPU Board Schematic
0120-0025-01	Input Board Assembly
0120-0026	Input Board Schematic
0120-0042-01	Input Board Cable Assembly
0120-0043-01	Probe Test Cable Assembly
0120-0044-01	Data Input Cable Assembly
0120-0080-10	Mother Board Assembly
0120-0081	Mother Board Schematic
0120-0145-10	DOS Power Harness Assembly
0121-0006-10	Chassis Top Assembly
0121-0010-10	Clock Board Assembly
0121-0011	Clock Board Schematic
0121-0015-10	Data Board Assembly
0121-0016	Data Board Schematic

DWG. NO. 0112-0204 | SH 1 | REV. F

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
F	3871	REV'D & REDRAWN PER ECO#	STM	DGW	6-13-83



1. MARK PART NO. 0112-0204 DASH NO. REV LEVEL AND VENDOR LOGO ON CABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

COM TECH 57062

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
10	0117-0040	1
10	0112-0120	1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES .XX ± .020 ± 1° .XXX ± .010

HOLE SIZE: .0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

ENG. SERV. | DATE

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DRAWN	G.GASSMAN	3-28-77
CHECKED	T. McCANN	3-28-77
PROJ. ENG.	?	
MANUFACTURING	?	
QUALITY ASSUR		

GOULD biomation

TITLE: KB TO FP CABLE ASSY

SCALE	SIZE	PART NUMBER	REV
	B	0112-0204	F

CODE K100 / K105 | SHEET 1 OF 1

KLINGLER K-VEL H

ITEM	QUANTITY PER ASSEMBLY									PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	VAR
	-90	-80	-70	-60	-50	-40	-30	-20	-10				
1									2	6000-0114-10	CONN. DIP 16 CONTACT	3M 3416-0000	
2									125	7100-0095-10	CABLE FLAT 16 COND. 28 AWG	3M 3302/16	

REV	DESCRIPTION	DATE	DWN	CKD
F	REV'D PER E.O. 3671	6-10-80	STM	RGW

DASH NO.	NEXT ASSEMBLY NUMBER	QTY
10	0117-0040	1
10	0112-0170	1

DWN	G. GASSMAN	3-28-77
CHK	T. McCANN	3-28-77
ENGR		
MFG.		
Q.A.		

LIST OF MATERIAL

KB TO FP CABLE ASSY

GOULD biomation

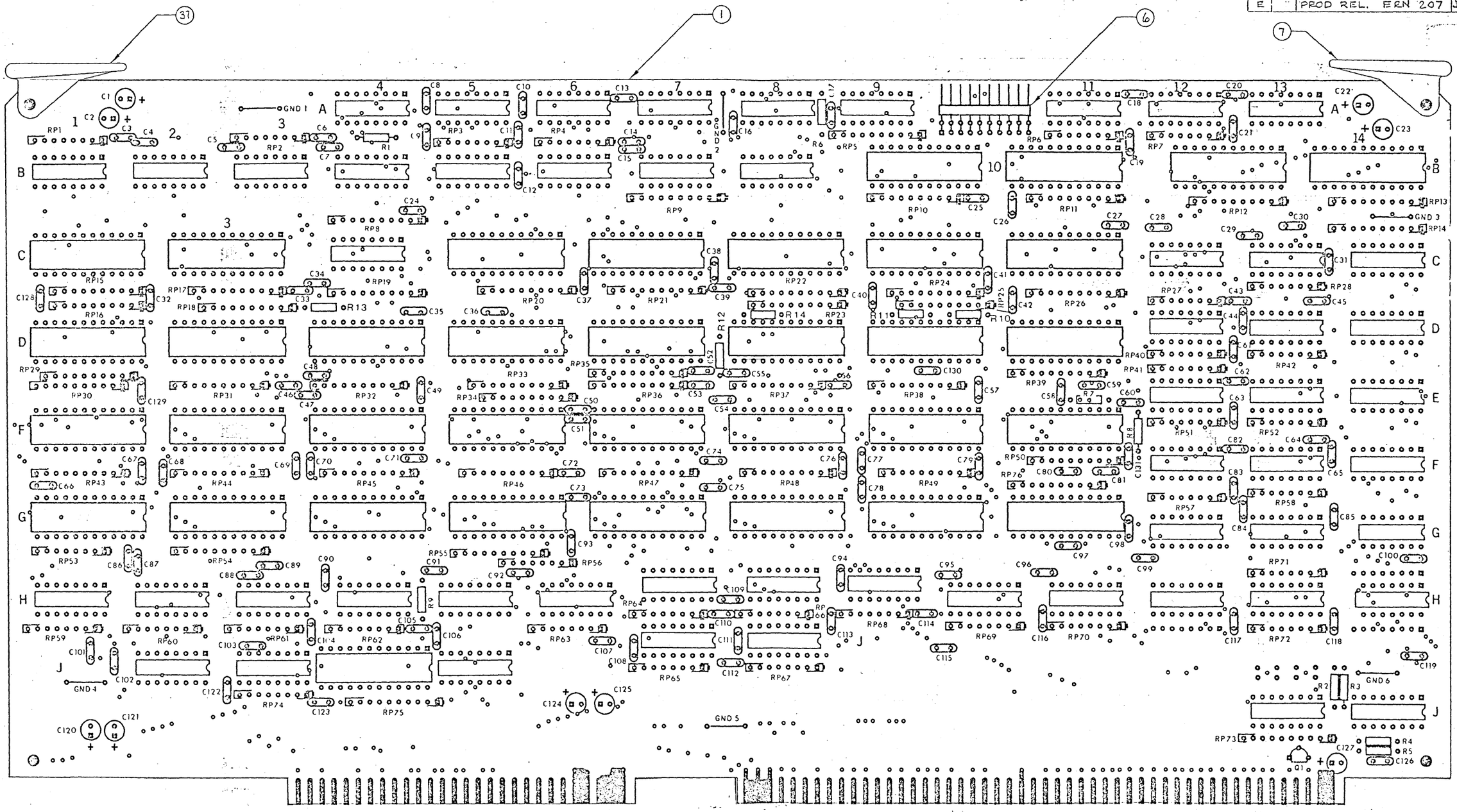
B | 0112-0204 | REV F

MODEL K10/105 | SHEET 1 OF 1

DWG. NO.	SH	REV.
0114-0120	1	J

F	2453	REVISED PER ECO	JWL	9-18-83
G	2512	REVISED PER ECO	JWL	11-8-83
H	4123	REVISED PER ECO N°	JWL	12-83
J	4235	REVISED PER ECO #	JWL	1-25-84

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	B		PILOT RELEASE ERN N° 0130	DB		
	C	1125	REVISED PER ECO	SR	DL	5-1-81
	D	1126	REVISED PER ECO	SR	DL	5-1-81
	D	—	——REDRAWN——	SR	DL	5-1-81
	E	1891	REVISED PER ECO.	MB	RD	5-13-81
	E		PROD REL. ERN 207	JWL	RG	7-8-81



NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.	NUMBER	QTY
-20	0114-1002	1
-10	0114-0002	1
	NEXT ASSEMBLY	

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = ±1° ANGLES, XX = .010 = 1°, XXX = .010

HOLE SIZE: 0-.599 = .003, .600-.999 = .004, 1.000-1.499 = .005

DRAWN	S. Riddell	DATE 5-1-81
CHECKED		
PROJ ENG		
MANUFACTURING		1/7/82
QUALITY ASSUR		
ENG. SERV.		DATE 1/7/82

GOULD biomation

TITLE: ASSEMBLY, CONTROL BOARD

SCALE	SIZE	PART NUMBER	REV
2:1	D	0114-0120	J

CODE K101-D

KLINGLER KVEL H

BILL OF MATERIAL

AS OF 02/12/86

0114-0120-10 ASSY,PCB,CONTROL,K101
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0114-0120	DWG,ASSY,CONTROL BD	0	EA	REF
0	00114-0121	DWG,SCHEM,CONTROL BD	0	EA	REF
1	0114-0122-10	FAB,PCB,CONTROL,K101	1	EA	
2	3700-0057-10	RPAK,2.2K,0.18W,2%,8/7	1	EA	RP71
3	1800-0105-10	IC 74LS00N 2-IN NAND LOW	1	EA	14G
4	1800-0254-10	IC 74LS85N 4-BIT MAG	1	EA	13H
5	1800-0349-10	IC 74368AN HEX BUS DR	1	EA	12H
6	6000-0307-10	CONN 20 PIN HDR. RT. ANGL	1	EA	
7	7000-0120-10	CARD EJECTOR NYLON 6/6	1	EA	
8	1850-0103-10	IC MC10125L QUAD ECL-TT	2	EA	12G,14J
9	1850-0097-10	IC MC10231L DUAL D F/F	1	EA	5A
10	1850-0104-10	IC MC10124L QUAD TTL	5	EA	10H,11H 3J,7J,8J
11	1850-0099-10	IC MC10164L 8-INPUT MULT	6	EA	12E,12F, 13J 4C,12C,12D
12	1850-0106-10	IC MC10117L DUAL 2 WIDE	1	EA	4A
13	1850-0111-10	IC MC10103L QUAD 2-IN	1	EA	11A
14	1850-0114-10	IC F10016DC 4-BIT BIN	4	EA	13C,13D, 13E,13F
15	1850-0098-10	IC MC10176L HEX D F/F	12	EA	1H,2H,2J, 3H,4H,6H, 6A,7A,12A 7H,8H,9H,
16	1850-0077-10	IC F100101DC TPL 5OR/NOR	9	EA	1D,3D,4D, 5F,7D,8D, 9B,9D,11D
17	1850-0078-10	IC F100102DC 2IN OR/NOR	11	EA	11C, 11F 1C,3C,4J, 5C,5D,7C, 8C,9C,11B
18	1850-0079-10	IC F100112DC QUAD DRIVER	1	EA	11G
19	1850-0088-10	IC HM10422 RAM 256 X 4 7NS	12	EA	1F,1G,3F, 3G,4F,4G, 7F,7G,8F, 8G,9F,9G
20	1850-0089-10	IC F10145ADC 16 X 4 RAM	10	EA	1B-8B 8A,9A
21	1850-0089-20	IC HD10145 HITACHI/FAIRCHILD	7	EA	14C-14F 5H,5J,13A
22	1850-0091-10	IC F100155DC QUAD MUX	3	EA	12B,14B,5G
23	1850-0100-10	IC MC10161L 1 OF 8 DEC	1	EA	13G
24	4010-0103-10	CAP,0.01UF,50V,10%,CER	122	EA	122,123, 126 128-131

BILL OF MATERIAL
AS OF 02/12/86

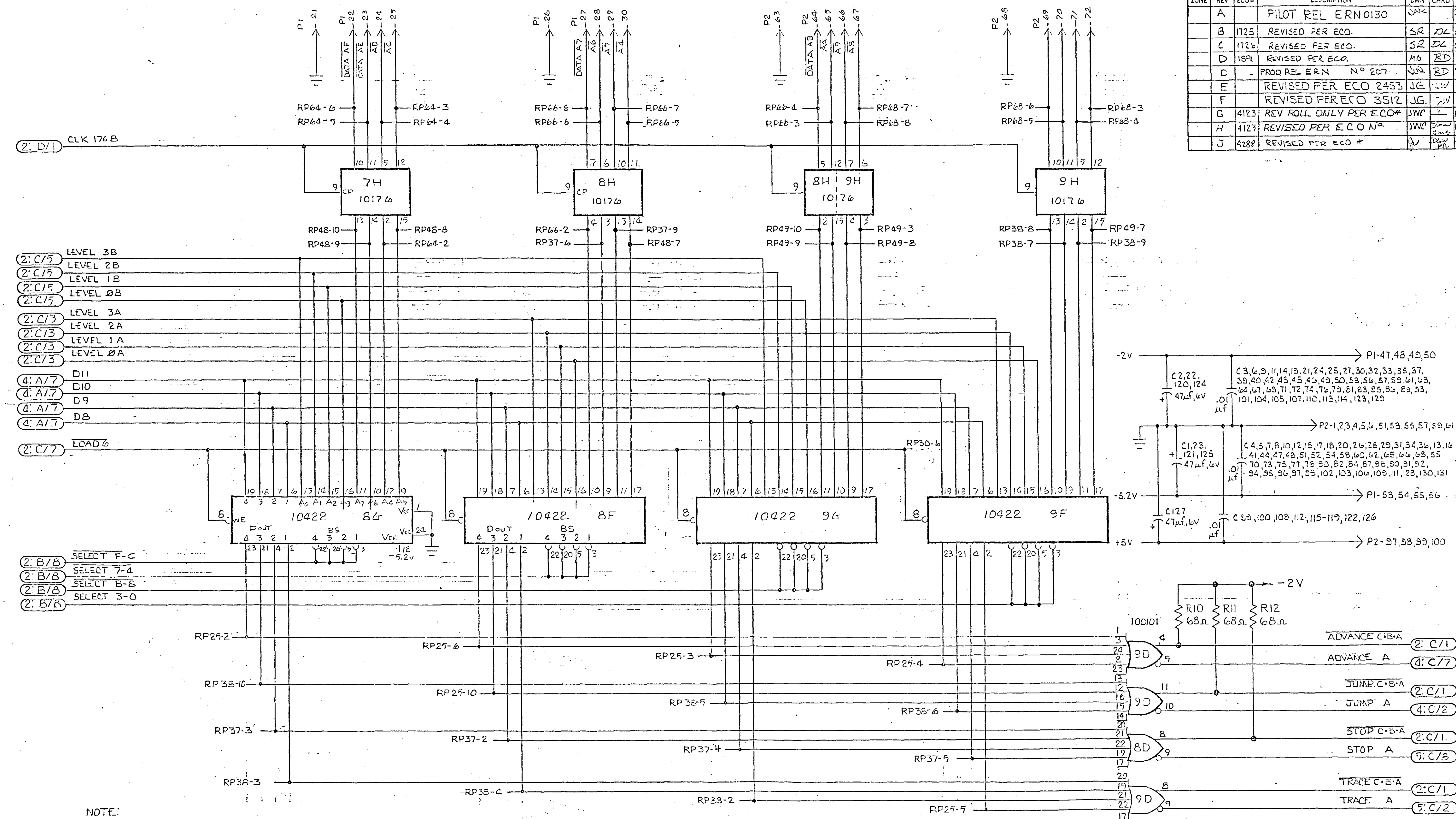
0114-0120-10 ASSY,PCB,CONTROL,K101
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
24	4010-0103-10	CAP,0.01UF,50V,10%,CER	122	EA	24-119 C3-21
25	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	9	EA	121,124, 125,127 23,120 C1,2,22
26	1400-0019-10	TRAN 2N3906	1	EA	Q1
28	3700-0088-10	RPAK,3K/6.2K,0.17W,2%,8/12	6	EA	69,70,72 74 RP65,67
29	3700-0091-10	RPAK,68,0.2W,2%,8/7	25	EA	27,28 40-42, 51-53, 56-64,66 68 RP1-4,6,7
30	3700-0092-10	RPAK,68,0.2W,2%,10/9	44	EA	29-39,76 43-50,54, 55,73,75 RP5,8-26
31	3000-2001-10	RES,2K,5%,1/4W,C	1	EA	R1
32	3000-2006-10	RES,20,5%,1/4W,C	1	EA	R2
33	3000-1800-10	RES,180,5%,1/4W,C	1	EA	R3
34	3000-3300-10	RES,330,5%,1/4W,C	1	EA	R4
35	3000-5106-10	RES,51,5%,1/4W,C	1	EA	R5
36	6100-0137-10	SKT 24 PIN DIP LOW PRO	12	EA	ALL 10422
37	0112-0228-01	CARD EJECTOR-HOT STAMPED (A1)	1	EA	
38	6100-0120-10	SKT 16 PIN DIP LO-PROFIL	17	EA	ALL 10145
39	9000-0054-10	BUSS WIRE, FORMED	6	EA	GND 1-6
41	6100-0119-10	SKT 14 PIN DIP LO-PROFIL	1	EA	X14H
42	3000-1002-10	RES,10K,5%,1/4W,C	1	EA	R14
43	1800-0280-10	IC 74S37N BUFFER/CLK DR.	1	EA	14H
45	3000-6806-10	RES,68,5%,1/4W,C	6	EA	13 R6,9 TO
46	3000-6800-10	RES,680,5%,1/4W,C	2	EA	R7,8

DWG. NO.	SH	REV
0114-0121	1	J

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL ERN0130	[illegible]		2-17-81
	B	1725	REVISED PER ECO.	SR	DL	5-4-81
	C	1726	REVISED PER ECO.	SR	DL	[illegible]
	D	1891	REVISED PER ECO.	MD	RD	8-13-[illegible]
	D	-	PROD REL ERN N° 207	[illegible]	RD	[illegible]
	E		REVISED PER ECO 2453	JG.	[illegible]	[illegible]
	F		REVISED PER ECO 3512	JG.	[illegible]	[illegible]
	G	4123	REV ROLL ONLY PER ECO#	JWC	[illegible]	12-1-83
	H	4123	REVISED PER ECO N°	JWC	[illegible]	12-2-83
	J	4288	REVISED PER ECO #	[illegible]	[illegible]	[illegible]



NOTE:

1. ALL RESISTOR PAKS TIED TO (-2V) EXCEPT FOR RP 59,69,70,72,73,75,76,77 TIED TO (+5V).
2. MAY USE HD10145 IC'S IN PLACE OF 10145A IC'S; ONLY IN LOCATIONS 5H, 5J, 13A, 14C-14F.

[3] R6 IS USED AS A TEST POINT AT TOP OF BOARD, SHT 6.

[4] RP34-4 AND RP34-2 WERE CONNECTED ON ETCH B.

[5] RP17-7 WAS CONNECTED ON ETCH B.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = ± .1, XX = ± .020, XXX = ± .010; ANGLES ± 1°

HOLE SIZE: 0-.599 = .003; .600-.999 = .004; 1.000-1.499 = .005

	Signature	DATE
DRAWN	[illegible]	[illegible]
CHECKED	[illegible]	4-16-81
PROJ. ENG.	[illegible]	1/18/82
MANUFACTURING	[illegible]	1/17/82
QUALITY ASSUR	[illegible]	[illegible]
ENG. SERV.	[illegible]	1/7/82

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

GOULD biomation

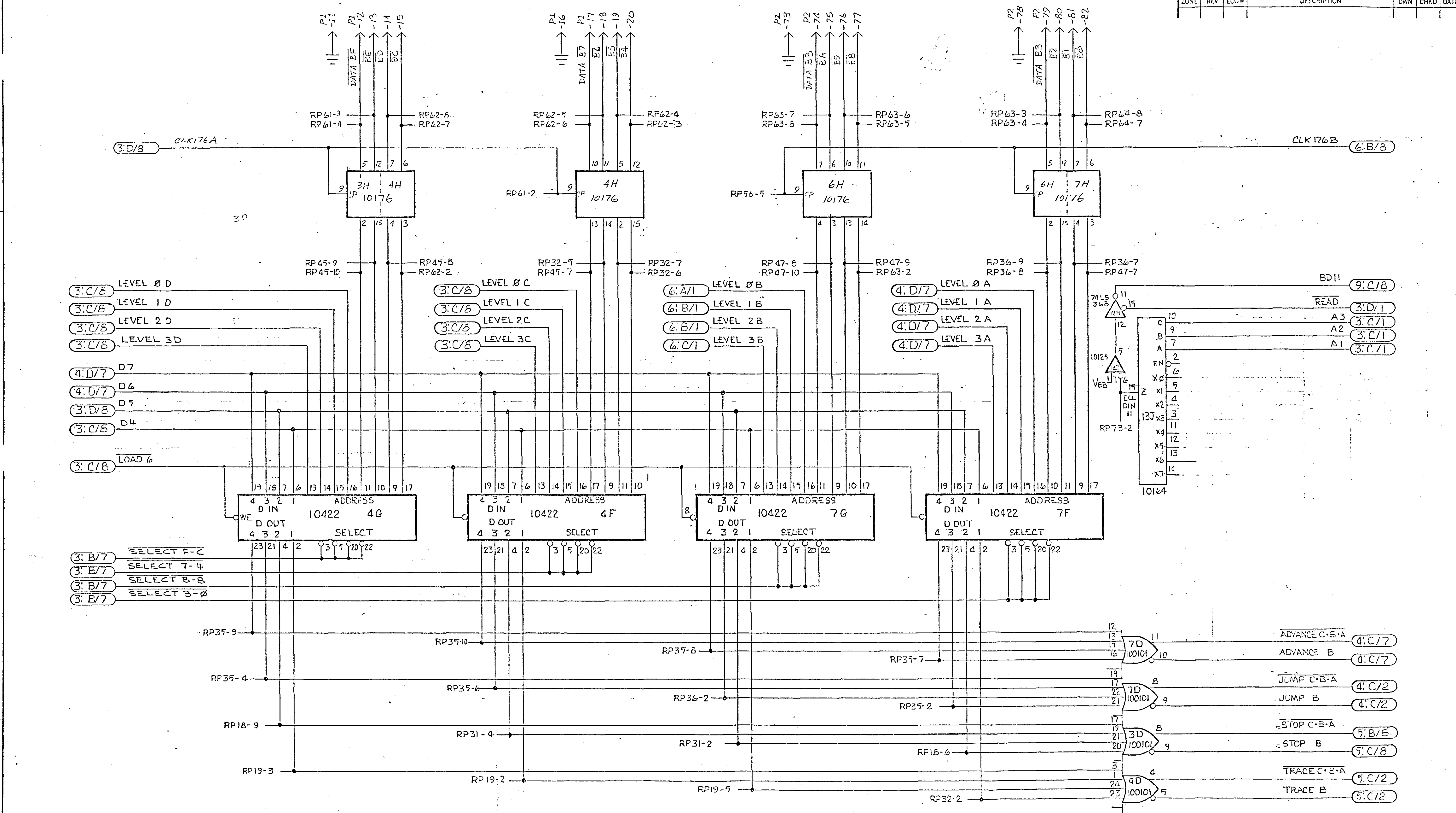
TITLE: SCHEMATIC CONTROL BOARD

SCALE	SIZE	PART NUMBER	REV
~	D	0114-0121	J

CODE [illegible] SHEET 1 OF 9

DWG. NO. 0114-0121 SH 2 REV. J

REVISIONS					
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM 1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = .1 ANGLES ± 1° XX = .020 XXX = .010 — HOLE SIZE: 0-.599 = .003, .600-.999 = .004, 1.000-1.499 = .005

DRAWN / DATE / CHECKED / PROJ. ENG. / MANUFACTURING / ENG. SERV. / DATE / QUALITY ASSUR

DASH NO. / NUMBER / NEXT ASSEMBLY / QTY

GOULD biomation

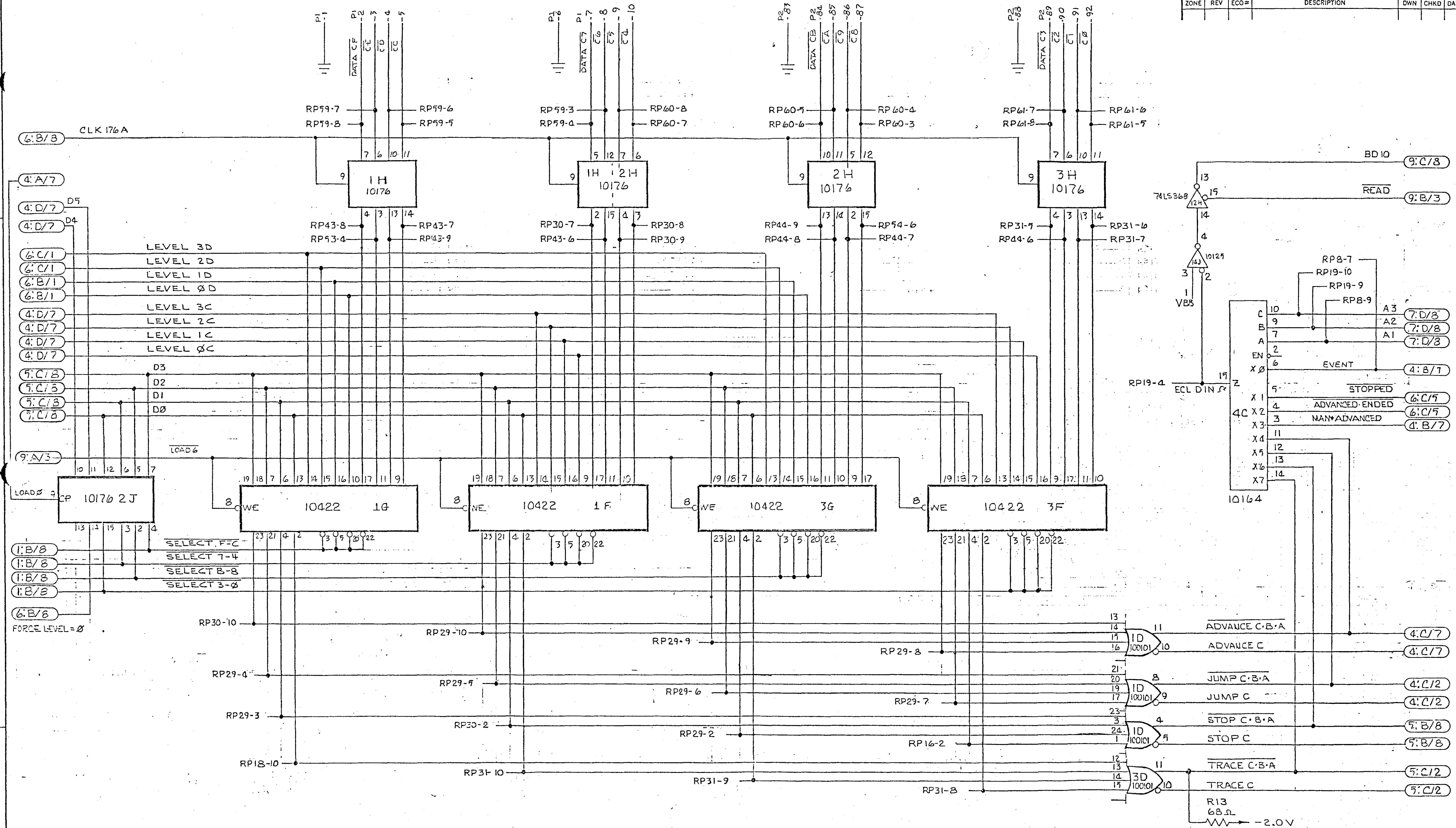
TITLE SCHEMATIC CONTROL BOARD (10422)

SCALE — SIZE D PART NUMBER 0114-0121 REV J

CODE K101-D SHEET 2 OF 9

DWG. NO. 0114-0121 SH 3 REV. J

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X = .1 .XX = .020 .XXX = .010 ANGLES = 1°

HOLE SIZE: 0-.599 = .003 .600-.999 = .004 1.000-1.499 = .005

DRAWN | DATE
CHECKED
PROJ. ENG.
MANUFACTURING
ENG. SERV. | DATE
QUALITY ASSUR

DASH NO. | NUMBER | QTY
NEXT ASSEMBLY

GOULD biomation

TITLE SCHEMATIC (10422) CONTROL BOARD

SCALE | SIZE D | PART NUMBER 0114-0121 | REV J

CODE K101 D | SHEET 3 OF 9

KLINGLER K-VEL H

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

LOAD E
LOAD C
LOAD A
LOAD B
LEVEL 3A
LEVEL 2A
LEVEL 1A
LEVEL ØA
LEVEL 3C
LEVEL 2C
LEVEL 1C
LEVEL ØC
D11
D10
D9
D8
D7
D6
D5
D4

6B 10145A
5B 10145A
4B 10145A
7B 10145A
8B 10145A

RP9-5
RP9-4
RP9-7
RP9-6
RP9-8

ADVANCE A
LOOP COUNT
ADVANCE B
ADVANCE C·B·A
T > 0
T = 0
T < 0

JUMP A
JUMP B
JUMP C
JUMP C·B·A

R14
10K

EVENT
MAN ADVANCED
R1
2K
CLK 10231
LOAD 2
LOAD Ø
FORCE JUMP
FORCE ADVANCE (-)
10117
EVENT
ADVANCE
JUMP
JUMP + ADVANCE
OLD CYCLE RESET
CYCLE RESET
FORCE STOP
FORCE TRACE

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
									1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER PLATED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: X = ± .1, ANGLES ± 1°, XX = ± .020, XXX = ± .010
HOLE SIZE: 0-.599 = .003, .600-.999 = .004, 1.000-1.499 = .005

DRAWN	J.W.CARROLL	DATE 4-10-81
CHECKED		
PROJ. ENG.		
MANUFACTURING		
QUALITY ASSUR		
ENG. SERV.		DATE

GOULD biomation

TITLE: SCHEMATIC CONTROL BOARD

SCALE	SIZE	PART NUMBER	REV
	D	0114-0121	J

CODE | SHEET 4 OF 9

DWG. NO. 0114-0121 SH 5 REV J

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

6:C/1 LEVEL 3A
6:B/1 LEVEL 2A
6:B/1 LEVEL 1A
6:A/1 LEVEL ØA
6:C/1 LEVEL 3C
6:B/1 LEVEL 2C
6:B/1 LEVEL 1C
6:A/1 LEVEL ØC

8:C/8 LOAD E
8:C/8 LOAD C
8:B/8 LOAD A

7:B/8 D11
7:B/8 D10
7:B/8 D9
7:B/8 D8

6:C/8 D3
6:C/8 D2
6:C/8 D1
6:C/8 DØ

RP1-2
RP2-8
RP2-3
RP5-4
RP5-6
RP5-5
RP5-7
RP1-4
RP1-6
RP1-5
RP1-7

1B 10145A
2B 10145A
3B 10145A
8A 10145A
9A 10145A

RP15-9 RP16-3 RP15-7 RP17-10 RP15-6 RP17-6 RP17-9 RP6-6 RP17-4 RP22-2 RP24-10 RP22-5 RP22-4 RP22-9 RP22-7 RP24-8 RP24-4 RP24-3 RP24-6

1:A/1 STOP A
2:A/1 STOP B
3:A/1 STOP C
3:A/1 STOP C·B·A
7:C/1 T>D
7:D/1 T=D
7:C/1 T<D
4:A/1 FORCE STOP
6:D/8 LOOP COUNT

RP17-3 RP17-8 RP15-5 RP8-3 RP25-8 RP22-3 RP22-8 RP25-9

TRACE A 1:A/1
TRACE B 2:A/1
TRACE C 3:A/1
TRACE C·B·A 5:A/1

RP16-8 RP19-10 RP19-2

3C 100102 1C 100102 1C 1C 1C 100102 1C 100102 3C 3C 100102 3C 3C 100102 8C 100102 9C 100102 9C 100102 9C 100102 8C 100102 8C 100102 8C 100102 8C 100102 8C 100102 9C 100102 9C 100102

RP17-5 RP18-4 RP18-3 RP18-2 RP10-8 RP10-7 RP10-6 RP10-9

4:A/2 FORCE STOP

3D 100101 STOP N.C.

7:B/8 STOP
4:A/2 FORCE TRACE
FORCE TRACE RP10-10

9B 100101 TRACE 7:B/8 N.C.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X = 1 ANGLES; XX = .020 ±1°; XXX = .010
HOLE SIZE: .0-.599 = .003; .600-.999 = .004; 1.000-1.499 = .005

DRAWN JWCARROLL DATE 4-2-81
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV. DATE

DASH NO. NUMBER NEXT ASSEMBLY QTY

GOULD biomation

TITLE SCHEMATIC CONTROL BOARD

SCALE SIZE D PART NUMBER 0114-0121 REV J

CODE K101D SHEET 5 OF 9

DWG. NO. 0114-0121 SH 6 REV J

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

TRACE D
ARMED
LOOP COUNT
LOAD 4
JUMP
JUMP + ADVANCE
FORCE LEVEL=Ø
CLK 176 B
CLK 176A
CLK TEST
CONTROL
ARMED
CLK 100116 (END OF LINE)
CLK 10231 (END OF LINE)
CLK 176
RP16-4
RP49-4
RP76-9
RP76-2
RP49-5
L3
L2
L1
LØ
R6 68Ω
-2V
N.C.
R9 68Ω
RP55-9
RP55-7
RP56-4
RP56-3
RP55-6
RP55-10
RP55-8
RP55-2
RP56-2
RP56-7
RP75-8
RP75-5
RP75-7
RP55-5
RP97-3
RP13-a
RP75-3
RP75-2
RP75-4
RP75-9
RP75-10
24 NSEC ~18" ± 1"
2 NSEC ~14" ± 1"
5H
5J
5G
10145A
100155 (DIP)
ADVANCE
JUMP
OUT PUT
~4. NSEC
3 NSEC
3 NSEC
LEVELS + CONTROL
DELAY COUNTERS
1 NSEC

LEVEL 3E 7:B/8
LEVEL 2E 7:B/8
LEVEL 1E 7:B/8
LEVELØE 7:B/8
LEVEL 3D 2:C/8
LEVEL 3C 2:C/16
LEVEL 3B 1:C/8
LEVEL 3A 1:C/8
LEVEL 2D 2:C/8
LEVEL 2C 2:C/16
LEVEL 2B 1:C/8
LEVEL 2A 1:C/8
LEVEL 1D 2:C/8
LEVEL 1C 2:C/16
LEVEL 1B 1:C/8
LEVEL 1A 1:C/8
LEVEL ØD 2:C/8
LEVEL ØC 2:C/16
LEVEL ØB 1:C/8
LEVEL ØA 1:C/8

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: X = 1 XX = .020 = 1° XXX = .010 ANGLES
HOLE SIZE: 0-.399 = .003 .400-.999 = .004 1.000-1.499 = .005
ENG. SERV. DATE

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DRAWN CHECKED PROJ. ENG. MANUFACTURING QUALITY ASSUR DATE

GOULD biomation

TITLE SCHEMATIC CONTROL BOARD

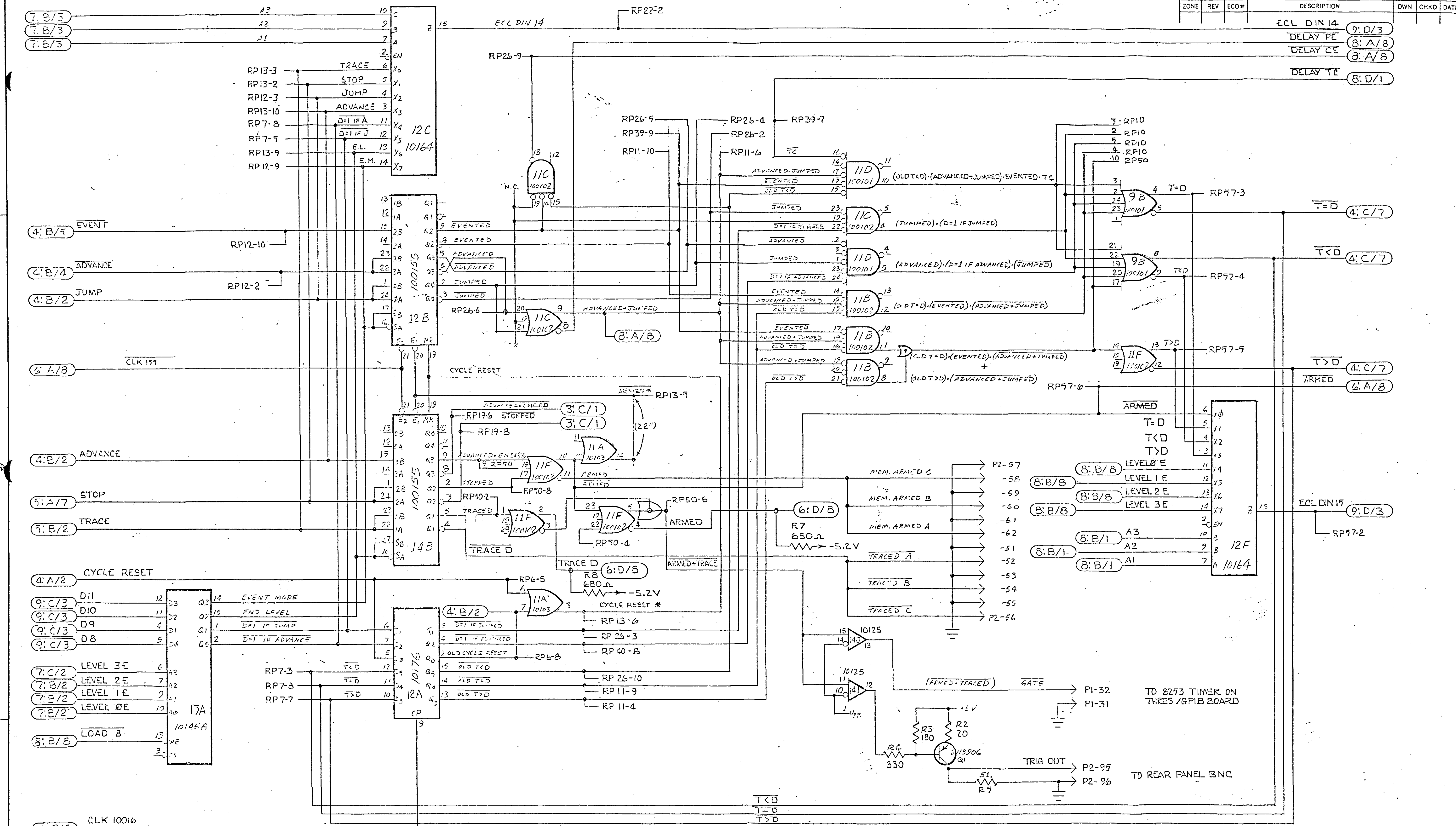
SCALE | SIZE D | PART NUMBER 0114-0121 | REV J

CODE K101-D | SHEET 6 OF 9

KLINGLER KVEL M

DWG. NO. 0114-0121 SH 7 REV. J

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
REVISIONS						



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = .1 ANGLES .XX = .020 ± 1° .XXX = .010

HOLE SIZE: 0-.599 = .003 .600-.999 = .004 1.000-1.499 = .005

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN J W CARROLL DATE 2-2-81

CHECKED

PROJ. ENG.

MANUFACTURING

ENG. SERV. DATE

QUALITY ASSUR

GOULD biomation

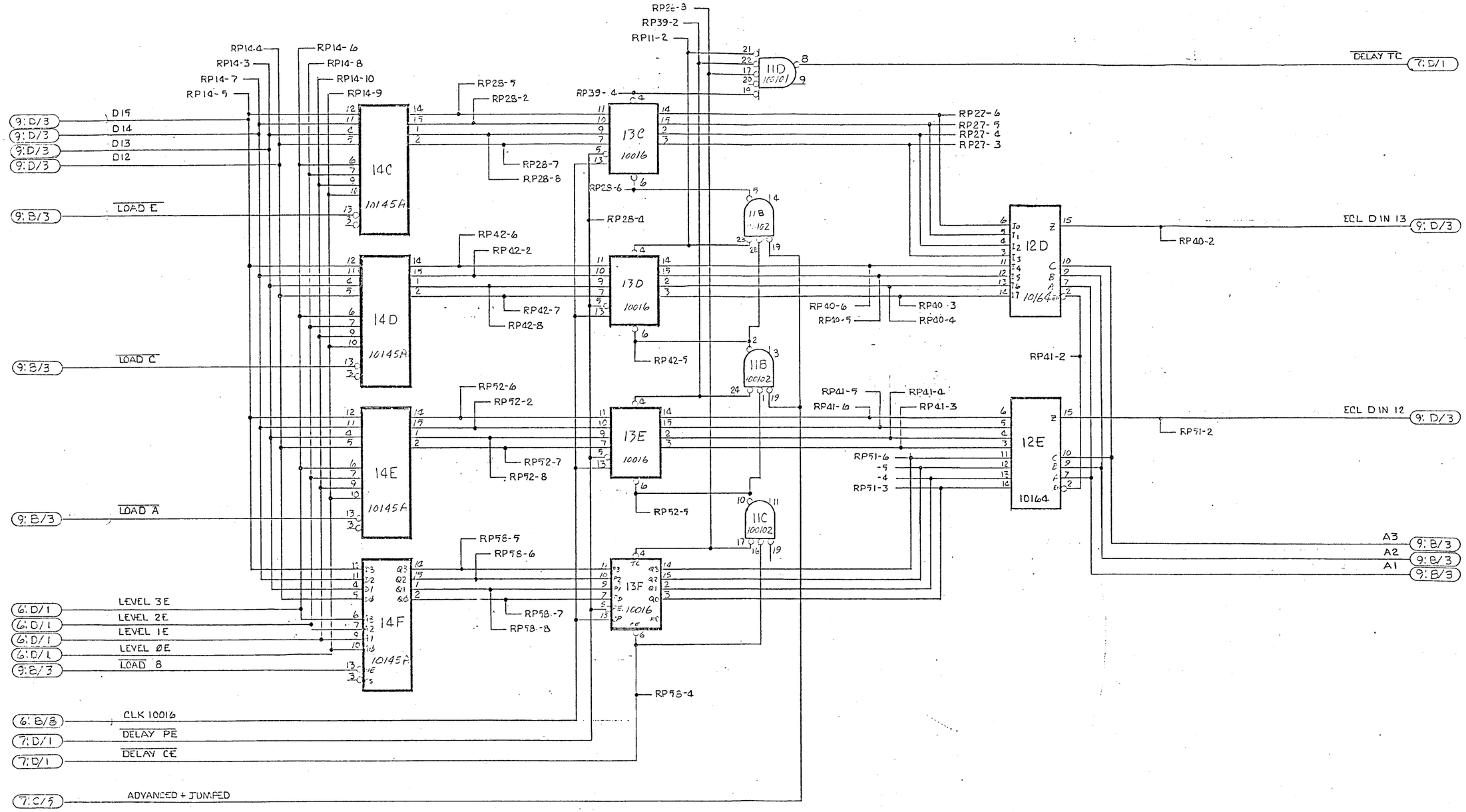
TITLE SCHEMATIC (10422 TYPE) CONTROL BOARD

SIZE PART NUMBER 0114-0121 REV J

SHEET 7 OF 9

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE



DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES, XX ± .020 = 1°, XXX ± .010
HOLE SIZE: 0-.599 = .003, .600-.999 = .004, 1.000-1.499 = .005

ENG. SERV. | DATE

DRAWN W.CARROLL | DATE
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR

GOULD biomation

TITLE SCHEMATIC CONTROL BOARD

SCALE ~ | SIZE D | PART NUMBER 0114-0121 | REV J

CODE K101-D | SHEET 8 OF 9

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

74368A 12H

74368A 12G

10124 11H

10124 8J

10124 7J

10124 3J

10124 10H

14G LS00

14H $37

10161 13G

74LS85 13H

RP70 3K/6.2K

RP67 3K/6.2K

RP66 3K/6.2K

RP74 3K/6.2K

RP69 3K/6.2K

RP72

RP71

RP70-3

RP70-2

RP58-2

ECL DIN 15 (7: B/1)
ECL DIN 14 (7: D/1)
ECL DIN 13 (8: C/1)
ECL DIN 12 (8: C/1)

P2-33 GND
P2-32 BD15
-31 BD14
-30 BD13
-29 BD12
-28 BD11 (2: C/1)
BD10 (3: D/1)
-25 BD9
-26 BD8
-24 BD7
-23 BD6
-22 BD5
-21 BD4
-20 BD3
-19 BD2
-18 BD1
P2-17 BD0
-16 EW2
-9 BA3
-38 BA2
-37 BA1
-36 RP70-3
-15 GND
-8 GND
-7 BRD
P2
P2-47,48 GND
P2-42 BA7
41 BA6
P2-40 BA5
39 BA4
M1/I0
P2-12
MY ADRS
WR
READ

D15 (8: D/8)
D14 (8: D/8)
D13 (4: A/7)
D12 (4: A/7)
D11 (1: C/8)
D10 (1: C/8)
D9 (1: C/8)
D8 (1: C/8)
D7 (2: C/8)
D6 (2: C/8)
D5 (2: C/8)
D4 (2: C/8)
D3 (3: C/8)
D2 (3: C/8)
D1 (3: C/8)
D0 (3: C/8)

A3 (2: C/1)
A2 (2: C/1)
A1 (2: C/1)
READ (2: C/1)

LOAD E (4: D/7)
LOAD C (4: D/7)
LOAD A (4: D/7)
LOAD 8 (4: D/7)
LOAD 6 (1: C/8)
LOAD 4 (6: C/8)
LOAD 2 (4: A/7)
LOAD 0 (3: E/8)

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
-50 -40 -30 -20 -10			1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY AFTER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X = 1 ANGLES; .XX = .020 = 1°; .XXX = .010
HOLE SIZE: 0.599 = .003; 600-999 = .004; 1.000-1.499 = .005

DRAWN	DATE
CURT & J.T.W.C	2-24-81
CHECKED	
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR	
ENG. SERV.	DATE

DASH NO. | NUMBER | QTY | NEXT ASSEMBLY

GOULD biomation

TITLE (10422 TYPE)
SCHEMATIC
CONTROL BOARD

SCALE	SIZE	PART NUMBER	REV
NONE	D	0114-0121	J

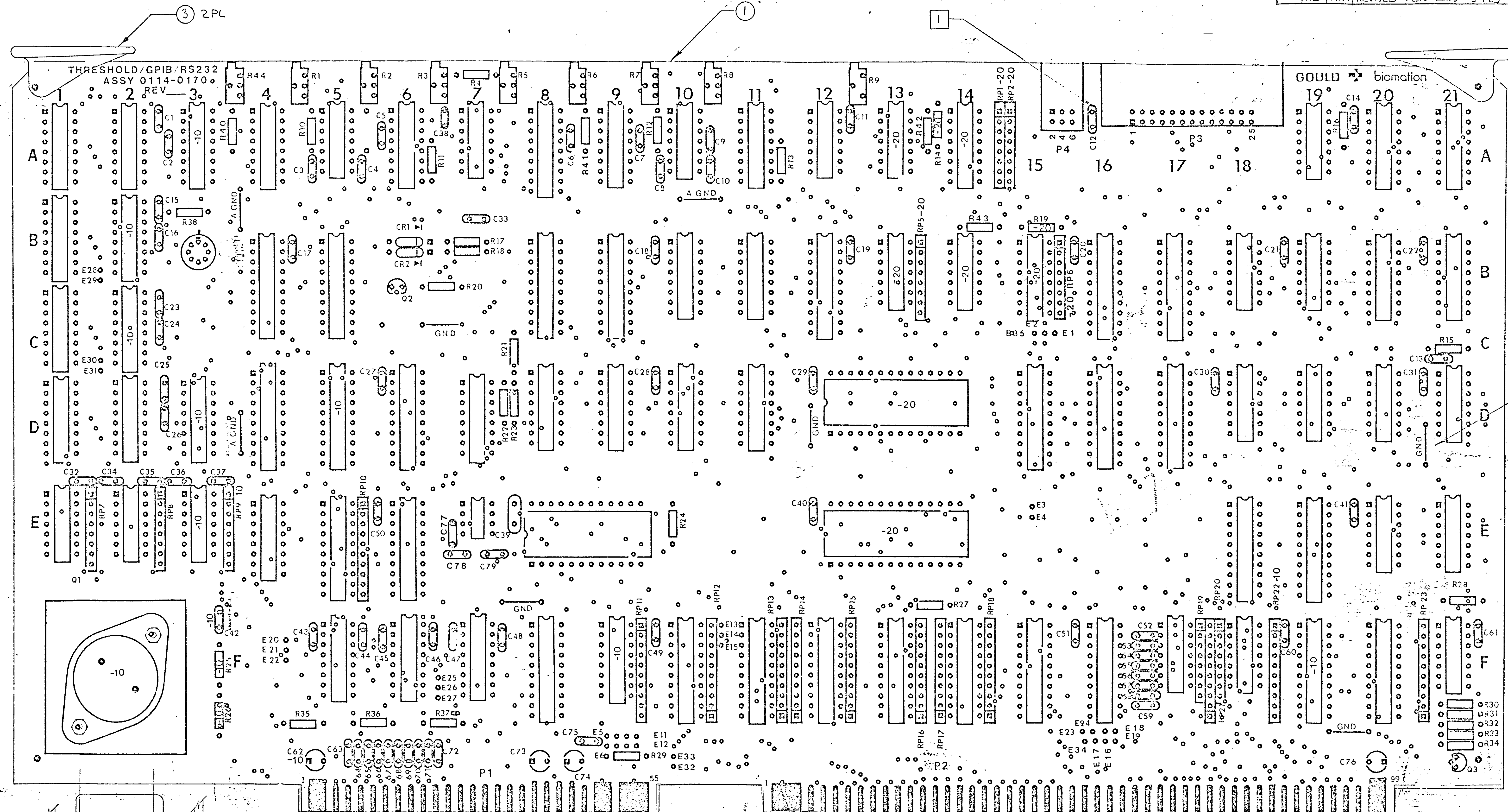
CODE K1010 SHEET 9 OF 9

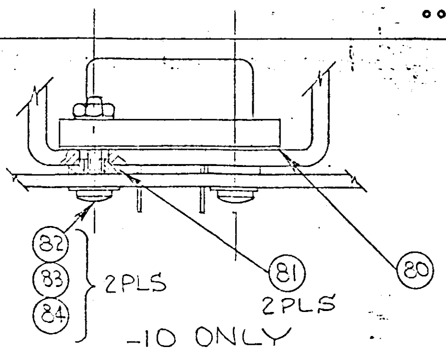
KLINGLER KVEL H

DWG. NO. 0114-0170 SH 1 REV. AC

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE HISTORY.			
	Z	4051	REVISED PER ECO			
	AA	4277	REVISED PER ECO			
	AB	4384	REVISED PER ECO			
	AC	4909	REVISED PER ECO 5-7-85	SAR	DW	

[1] C12 NOT LOADED





JUMPER LIST																	
DESCRIPTION	REF DES	AS ETCH	K500 -10	K101 -20	K205 -30	DESCRIPTION	REF DES	AS ETCH	-10	-20	-30	DESCRIPTION	REF DES	AS ETCH	-10	-20	-30
RS 449 RC	E1-E2	IN				SELECT M/$\overline{IO}$	E13-E14	IN	CUT				E25-E26	IN	CUT		
$\overline{INTR\ 3}$	E3-E4	IN				SELECT $\overline{IO}$ PAGE	E14-E15	OUT	JUMPER				E26-E27	OUT	JUMPER		
SELECT A11	E5-E6	IN				RS449 SG	E16-E17	OUT		JMP			E28-E29	OUT		JUMPER	
SELECT A10	E7-E8	OUT				RS449 SC	E18-E19	IN	CUT				E30-E31	OUT		JUMPER	
SELECT A9	E9-E10	OUT				SELECT +11V MONITOR	E20-E21	OUT	JUMPER			INTA	E32-E33	IN	CUT		
SELECT A8	E11-E12	IN				SELECT VBB MONITOR	E21-E22	IN	CUT				E17-E34	IN	CUT	CUT	
$\overline{INTR\ 2}$	E23-E24	IN											E2-E35	IN	CUT	CUT	

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X = .1 .XX = .020 .XXX = .010 ANGLES ± 1°

HOLE SIZE: 0-.599 = .003 .600-.999 = .004 1.000-1.499 = .005

DRAWN J. WELDON DATE 4-30-8

CHECKED

PROJ. ENG.

MANUFACTURING

ENG. SERV. DATE

QUALITY ASSUR

GOULD biomation

TITLE ASSEMBLY THRESHOLD/GPIB/RS232

SCALE 2:1 SIZE D PART NUMBER 0114-0170 REV AC

CODE K101/K500/K205 SHEET 1 OF 1

BILL OF MATERIAL

AS OF 02/12/86

0114-0170-30 ASSY,PCB,THRESHOLD,GPIB,RS232
MODEL:

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0114-0170	DWG,ASSY,THRESHOLD/GPIB/RS232	0	EA	REF
0	D0114-0171	DWG,SCHEM,THRESHOLD/GPIB/RS232	0	EA	REF
1	0114-0172-10	FAB,PCB,THRESHOLD/GPIB,RS232	1	EA	
3	7000-0120-10	CARD EJECTOR NYLON 6/6	2	EA	
5	1700-0086-10	IC LM324AN QUAD OP AMP	4	EA	10A 1E,2E,5A
6	1700-0063-20	IC REF-01EJ VOLT REF	1	EA	3B
8	1820-0077-10	IC MP7533CD MULT DAC	2	EA	4A,9A
9	1820-0076-10	IC MP7508DIJN ANA MULT	11	EA	1A-1D,2A 2D,5F,6F 7F,2B,2C
10	1820-0075-10	IC AD7541 12BIT MONO MLT DAC	1	EA	8A
11	1800-0343-10	IC P8251A PROG COMM	2	EA	12D,12E
12	1800-0344-10	IC P8253-5 PROG INTER	1	EA	8E
13	1700-0101-10	IC DS1488N DR RS232	2	EA	13A,13B
14	1700-0102-10	IC AM26LS32PC QUAD DIFF	2	EA	14A,15B
15	1800-0200-10	IC 7433N QUAD 2-IN	1	EA	14B
16	1800-0125-10	IC 74LS161N 20CNTR, SYN, BIN	1	EA	8D
17	1800-0231-10	IC 74LS273N 20 FF, D, X8	13	EA	15D,5E,6E 15F,12B 18E,19E 4B,5B,8B 9B,4D,6D
19	1800-0267-10	IC 74LS240N OCTAL LINE	5	EA	13F,16F 17B 20F,16B
20	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	5	EA	16D,17D 8F,10F,11F
21	1800-0268-10	IC 74LS245N BUS TRANS	2	EA	12F,14F
22	1800-0193-10	IC 74LS138N 16 DCDR, 3TO8	5	EA	10B,9D-11D 11B
24	1800-0311-10	IC 7438N QUAD 2-INPUT	7	EA	17F,18F 19D,20E 21E 21F,18D
25	1800-0110-10	IC 74LS10N TRIPLE NAND	1	EA	18B
26	1800-0105-10	IC 74LS00N 2-IN NAND LOW	3	EA	20D 21Q,19B
27	1800-0068-10	IC 74LS112N DUAL J-K FF	4	EA	20A,21A 20B,21B
28	1800-0111-10	IC 74LS20N DUAL 4-IN	1	EA	12A
29	1800-0309-10	IC 74LS260PC DUAL 5 INPUT	1	EA	19A
31	1700-0071-10	IC LF356AN MONO OP AMP	1	EA	7E
32	1700-0106-10	IC OP-11EP OP AMP	1	EA	7A
33	3000-3300-10	RES,330,5%,1/4W,C	3	EA	R15,23,33
34	3000-2201-10	RES,2.2K,5%,1/4W,C	6	EA	30,14,19

BILL OF MATERIAL
AS OF 02/12/86

0114-0170-30 ASSY,PCB,THRESHOLD,GPIB,RS232
MODEL:

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
34	3000-2201-10	RES,2.2K,5%,1/4W,C	6	EA	R20,24,28
35	3000-1001-10	RES,1K,5%,1/4W,C	4	EA	R35-38
36	3000-2200-10	RES,220,5%,1/4W,C	3	EA	R16,22,32
37	3000-1004-10	RES,1M,5%,1/4W,C	2	EA	R40,41
38	3000-2006-10	RES,20,5%,1/4W,C	1	EA	R31
39	3000-5106-10	RES,51,5%,1/4W,C	1	EA	R34
40	3000-2701-10	RES,2.7K,5%,1/4W,C	1	EA	R21
41	3000-2002-10	RES,2K,5%,1/4W,C	3	EA	R18,42,43
45	3100-1003-10	RES,100K,1%,1/8W,MF	1	EA	R4
46	3100-4990-10	RES,499,1%,1/8W,MF	1	EA	R17
47	3000-3302-10	RES,33K,5%,1/4W,C	2	EA	R11,13
48	3300-0070-10	POT,10K,0.5W,10% 20T,PC,RTANG	3	EA	R7,8,44
49	3300-0060-10	POT,500,0.5W,10% 25T,PC,RTANG	4	EA	R2,3,5,9
50	3300-0012-10	POT,1K,0.5W,10% 20T,PC,RTANG	2	EA	R1,6
51	3700-0048-10	RPAK,10K,0.1W,16/8	4	EA	6A,11A,4E 7D
52	3700-0083-10	RPAK,2.2K,0.18W,2%,10/9	2	EA	RP10,11
53	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	9	EA	23 RP12-18,20
54	3700-0084-10	RPAK,2.7K,0.2W,2%,8/4	2	EA	RP2,6
55	3700-0056-10	RPAK,180,0.2W,2%,8/4	4	EA	5 RP19,21,1
56	3700-0076-10	RPAK,47,.2W,2%,8/4	2	EA	RP7,8
57	3000-7500-10	RES,750,5%,1/4W,C	2	EA	R10,12
58	1000-0003-10	DIO,5082-2811	2	EA	CR1,2
59	1300-0028-10	TRAN 2N3904	1	EA	Q2
60	1400-0019-10	TRAN 2N3906	1	EA	Q3
61	3000-2001-10	RES,2K,5%,1/4W,C	1	EA	R27
62	3000-3001-10	RES,3K,5%,1/4W,C	1	EA	R29
63	4010-0103-10	CAP,0.01UF,50V,10%,CER	46	EA	14-32 34-37 39-41 43-51 75,78,79 9,11,60,61 C1,2,6,7
65	4010-0470-10	CAP,47PF,50/100V,5%/10%,CER	14	EA	13,33,38 53-57,59 C3-5,8,10
66	4010-0471-10	CAP,470PF,50/100V,5%,CER	1	EA	C77
67	4010-0104-10	CAP,0.1UF,50V,10%,CER	12	EA	58 C63-72,52
68	4400-0045-10	CAP,33UF,25V,ELCTLT	2	EA	C73,74
69	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	1	EA	C76
71	6000-0417-10	CONN 6 PIN HDR RT ANGLE	1	EA	P4
72	6000-0388-20	CONN 26 PIN RT ANGLE HDR	1	EA	P3

BILL OF MATERIAL
AS OF 02/12/86

0114-0170-30 ASSY,PCB,THRESHOLD,GPIB,RS232
MODEL:

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
74	6100-0119-10	SKT 14 PIN DIP LO-PROFIL	2	EA	X7A,X14B
75	6100-0120-10	SKT 16 PIN DIP LO-PROFIL	2	EA	X4A,9A
76	6100-0156-10	SKT 18 PIN	1	EA	X8A
77	6100-0122-10	SKT 24 PIN DIP	1	EA	X8E
78	6100-0151-10	SKT 28 PIN DIP LO PROFIL	2	EA	X12D,X12E
86	9000-0054-10	BUSS WIRE, FORMED	8	EA	

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	—	PROTOTYPE	CS		
	B	—	RELEASE TO PILOT, SER #0092	MR		
	B	—	PROD REL ERN #1129	MR	RG	4/81
	C	1701	REVISED PER ECO	JWC	JL	
	D	1805	REVISED PER ECO	B.H.	DW	11/82
	E	1954	REVISED PER ECO	B.H.	DW	1/5/83
	F	2202	REVISED PER ECO	[illegible]	JW	4/8/83
	G	2240	REVISED PER ECO	[illegible]	DW	5/3/83
	H	2342	REVISED PER ECO	[illegible]	DW	7/5/83
	J	2483	REVISED PER ECO	[illegible]	[illegible]	10/83
	K	2501	REV'D PER ECO	[illegible]	[illegible]	10/83
	L	2614	REV'D PER ECO	JWC	T.J.	2/26/84
	M	2703	REVISED PER ECO	SR	DW	11/1/84
			REVISIONS N-T NOT USED	MW	DW	5-1-85
	U	3589	REV'D PER ECO	MW	DW	5-1-85
	V	3605	REV'D PER ECO	MW	DW	5-1-85
	W	3706	REV'D PER ECO	MW	DW	9/4/85
	X	4068	REVISED PER ECO#	[illegible]	DW [illegible]	9/19/85
	Y	4111	REVISED PER ECO#	JR	DW	11/21/85
	Z	4087	REVISED PER ECO	[illegible]	DW [illegible]	12/11/85
	AA	4277	REVISED PER ECO	[illegible]	DW [illegible]	2/26/86
	AB	4384	REVISED PER ECO#	[illegible]	[illegible]	4/28/87
	AC	4809	REVISED PER ECO	S-9-88	SAR	DW

D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 — from sht. 5

WR VAR A HI
WR VAR A LO
WR VAR B HI
B RESET
WR VAR B LO

6D 74LS273 — MR CP D0 D1 D2 D3 D4 D5 D6 D7 — Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7

4B 74LS273

12B 74LS273

9B 74LS273

+5 — C76 47µf 6V — C11,14,17-22,27-31,39-41,49-51,60,61 .01µf — P2-97,98,99,100 +5V — +5V

P2-1,2,3,4,5,6 GND — GND

C75 .01µf

P1-47,48,49,50 -2.0V — to sht. 2

P1-51,52,53,54,55,56 -5.2V — to sht. 2

9A* AD7538LN — LSB MSB RFB V_{DD} I_O $\overline{I_O}$ AGND GND VREF

4A* AD7533 LN

+15V — R12 6 — C8 47pf — 11A 10K ±1% 10K — 10A LM324A — -VAR A — to sht. 2

R13 5 — 11A 10K, 1% — A GAIN R6 500 CW — A OFST R9 500 CW — R41 1M 5% 4 — C10 47pf — LM324A 10A

R10 6 — C5 47pf — 6A 10K ±1% 10K — 5A LM324A — -VAR B — to sht. 2

R11 5 — 10K, 1% 6A — B GAIN R1 500 CW — B OFST R2 500 CW — R40 1M 5% 4 — C4 47pf — LM324A 5A

A GND

+15V — R38 1K — 6A 10K ±1% 10K — LM324A 5A — -10V

3B REF01E — R44 10K — +10V

+10V — +10V to sht. 2

11A 10K — R7 10K CW CCW — 10A LM324A — -ECL (±3. V) — to sht. 2

11A 10K — R8 10K CW CCW — 10A LM324A — -TTL (±3. V) — to sht. 2

+15V to pin 4 of all LM324A

3 Heat Sink — Q1 LM317K — TO SHT. 2

P1-41,42 +15V — C74 33µfd 25V — C1,6,7,9,15,23,25,32,35,37,44,45,48. .01µfd — R25 3. 124Ω, 1% — R26 3. 976Ω, 1% — C42 3. .01µfd — C62 3. 33µf/25.V — +11V — P1 -1,2,3,4

P1-37,38,43,44 AGND — C73 33µfd 25V — C2,16,24,26,34,36,43,45,47,78 .01µfd — AGND

P1-39,40 -15V — -15V — to pin 11 of all LM324A

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, ¼W, 5%
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS

3 USED ON K500 ONLY (-10)

4 USED ON VERSIONS (-20), -30 ONLY

5 R11,13 (-10 VER = 100K, 1/8 W, 1%, -20 VER = 33K, -30 VER = 33K

6 FOR -10 RESISTOR IS 360Ω
FOR -20/-30 RESISTOR IS 750Ω, 1/8W, 1%

7 FOR -10 RESISTOR IS 500Ω
FOR -20/-30 RESISTOR IS 1KΩ.

8 USED ON K500 (-10) AND K205 (-30) ONLY.

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
							THRESHOLD DAC'S	1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X = 1 ANGLES; XX = .020 = 1°; XXX = .010
HOLE SIZE: 0.599 = .003; 600-999 = .004; 1.000-1.499 = .005

DRAWN	Curt	DATE 11-4-85
CHECKED	R. Dean	4/19/86
PROJ. ENG.		
MANUFACTURING		
QUALITY ASSUR		
ENG. SERV.		DATE

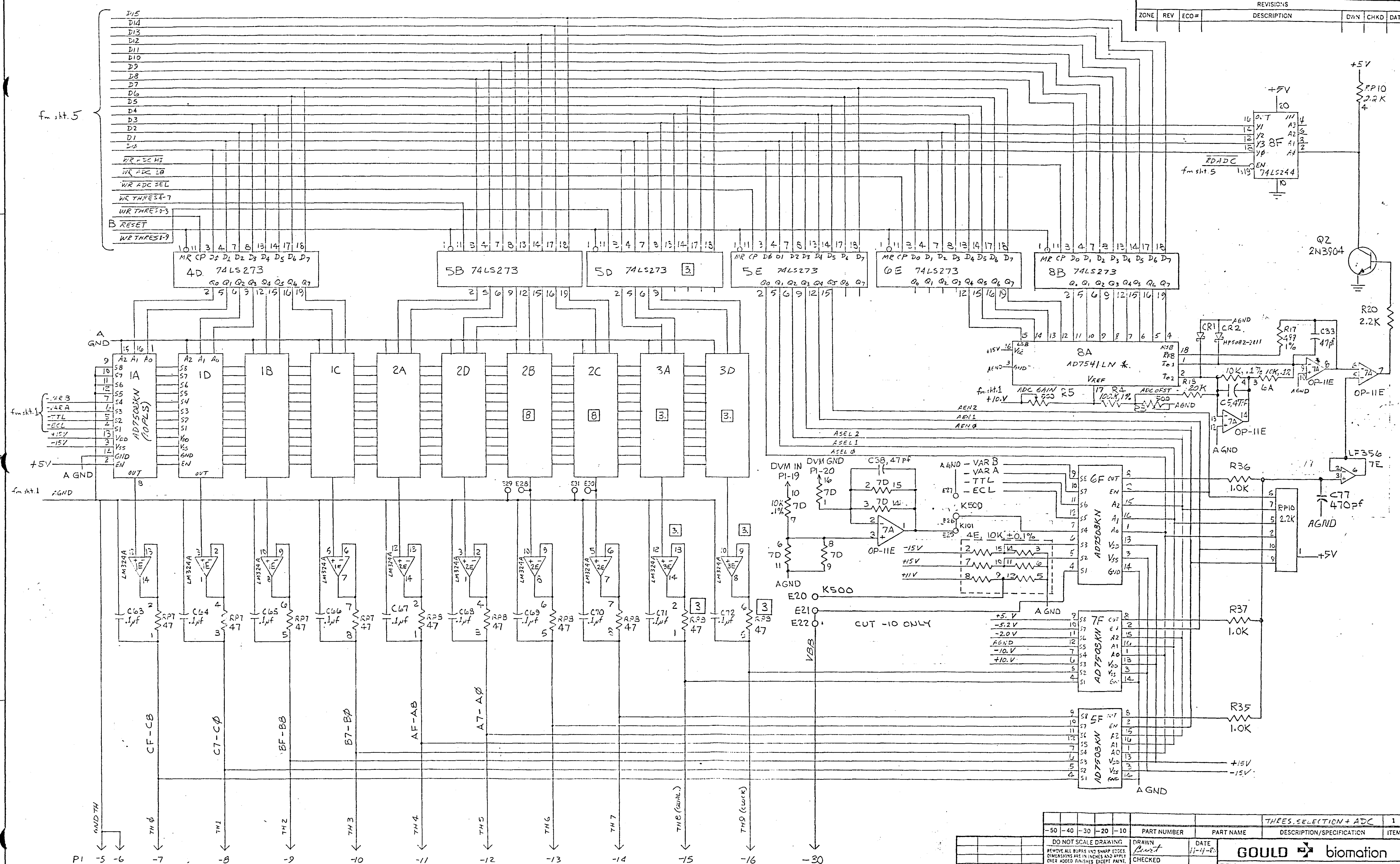
GOULD biomation

TITLE SCHEMATIC
THRESHOLD/GP/3/RS232

SCALE	SIZE	PART NUMBER	REV
—	D	0114-0171	AC

CODE K101/K501/K205 | SHEET 1 OF 3

KLINGLER KVEL H



DWG. NO. 0114-0171 SH 2 REV. AC

REVISIONS

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
							THRES. SELECTION + ADC	1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X = .1 .XX = .020 .XXX = .010 ANGLES = 1° HOLE SIZE: .0-.599 = .003 .500-.999 = .004 1.000-1.499 = .005

DASH NO. | NUMBER NEXT ASSEMBLY | QTY

DRAWN Curt DATE 11-4-8

CHECKED

PROJ. ENG.

MANUFACTURING

ENG. SERV. DATE

QUALITY ASSUR

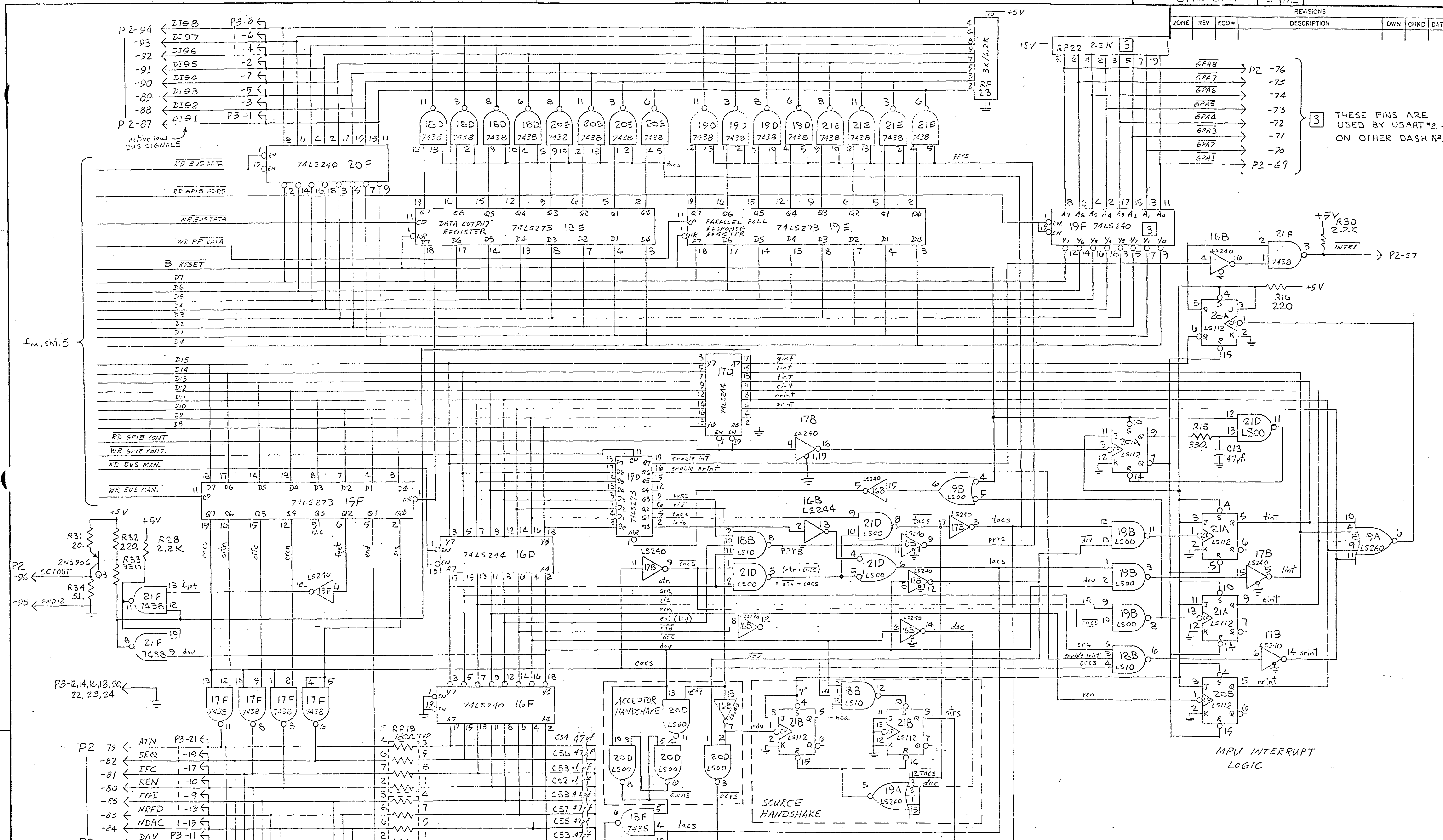
GOULD biomation

TITLE SCHEMATIC THRESHOLD/GPIB/RS232

SCALE | SIZE D | PART NUMBER 0114-0171 | REV AC

CODE K101/K500/K205 SHEET 2 OF 5

DWG. NO. 0114-0171 SH 3 REV AC



					GPIB (488) INTERFACE	1
-50 -40 -30 -20 -10	PART NUMBER	PART NAME			DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING. REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE — DIMENSIONAL: .X ± .1 ANGLES ± 1°, .XX ± .020, .XXX ± .010; HOLE SIZE: 0-.599 ± .003, .600-.999 ± .004, 1.000-1.499 ± .005

DRAWN Curt — DATE 11-4-83
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV. — DATE

DASH NO. | NUMBER NEXT ASSEMBLY | QTY

GOULD biomation

TITLE SCHEMATIC THRESHOLD /GPIB/RS232

SCALE — | SIZE D | PART NUMBER 0114-0171 | REV AC

CODE K101/K500/K205 | SHEET 3 OF 5

DWG. NO.	SH	REV
0114-0171	4	AC

REVISIONS

ZONE	REV	ECO=	DESCRIPTION	DWN	CHKD	DATE

fm sht 5: D7 D6 D5 D4 D3 D2 D1 D0 · A2 · A1 · B WR · B RD · USART #2 EN · USART #1 EN · TIMER EN

8E 8253-B PROG. INTERVAL TIMER/COUNTER — +5V, GND; CS RD WR A1 A0 D7 D6 D5 D4 D3 D2 D1 D0; CLK0 GATE0 OUT0 CLK1 GATE1 OUT1 CLK2 GATE2 OUT2

12D 8251A USART #1 UNIV. SYNCH/ASYNC RECEIVER/TRANSMITTER — +5V, GND; C/D RD WR CS D7 D6 D5 D4 D3 D2 D1 D0; RESET CLK; RECEIVE: R×RDY SYNDET CTS DSR R×D R×C; TRANSMIT: T×C T×D DTR RTS T×EMPTY T×RDY

12E 8251A USART #2 — +5V, GND; C/D RD WR CS D7 D6 D5 D4 D3 D2 D1 D0; RESET CLK; RECEIVE: R×RDY SYNDET CTS DSR R×D R×C; TRANSMIT: T×C T×D DTR RTS T×EMPTY T×RDY

BAUD x16 (#1) · BAUD x16 (#2) · 2MHz · RESET

14B 7433 — INTR 3 → P2-59 (E3, E4); INTR 2 → P2-53 (E23, E24); INTR 4 → 60

R24 2.2K · R27 2K · R29 3K · LS240 13F · GATE → -23 · P1-24

R21 2.7K · R22 220 (8MHz CLK) · R23 330 · 74LS161 8D (P3 P2 P1 P0 PE CP MR CEP CET; Q3 Q2 Q1 Q0; 2MHz) · P2-78 · -77

21F 7438 · LS240 · B RESET fm sht 5

R14 2.2K · 14A 26LS32 · 13A 1488 · R42 20K · RP2 2.7K · RP1 180. · P2 CTS DSR R×D T,DATA DTR RTS → G1 G2 G3 G4 G5 G7 G6 G5

J20 (on K101 motherboard) RS232 conn (pin 5) (pin 6) (pin 3) (pin 7) (pin 2) (pin 20) (pin 4) — 25 pins

R19 2.2K · 15B 26LS32 · 13B 1488 · R43 20K · RP6 2.7K · RP5 180. · P2 (SCS) CTS (SRR) DSR E,D (SRD) (RC) RC (SSD) T,D (SRS) RTS → G9 G0 G1 G2 G6 G5 G4 G3

J19 (on K101 motherboard) RS449 conn (pin 8) (pin 2) (pin 4) (pin 6) (pin 9) (pin 3) (pin 5) (pin 7) — 9 pins

449 names · 232 names

4 THESE PINS ARE USED BY GPIB (19F) ON -10 VERSION.

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
							RS232 INTERFACE	1

DO NOT SCALE DRAWING — REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER PLATED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE — DIMENSIONAL: X ± .1 ANGLES, .XX ± .020 = 1°, .XXX ± .010; HOLE SIZE: 0-.599 = .003, .600-.999 = .004, 1.000-1.499 = .005

	DRAWN	DATE
ENG. SERV.	CHECKED	
	PROJ. ENG.	
	MANUFACTURING	
	QUALITY ASSUR	

GOULD biomation

TITLE SCHEMATIC THRESHOLD/GPIB/RS232

SCALE	SIZE	PART NUMBER	REV
—	D	0114-0171	AC

CODE K101/K500/K205 — SHEET 4 OF 5

KLINGLER KV2L H

DWG. NO. 0114-0171 | SH 5 | REV AC

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

P2 -46 EA11 -45 EA10 -44 EA9 -43 EA8 → 74LS244 10F → RP11 2.2K, +5V; 74LS685 3/4 → E6 E5 E8 E7 E10 E9 E12 E11

P2 -14 DT/R → LS244 11F → DT/R

P2 -13 DEN, -56 INTA → LS240 12F → DEN; CUT -10; E32 E33

P2 -11 IOPAGE, -12 M/IO → LS244 11F → K500 E15 ONLY; J1 E14 K101/K102 E13 ONLY

P2 -42 BA7 -41 BA6 -40 BA5 -39 BA4 → 74LS244 11F

74LS138 11B: G2 ← GND; G1B ← GND; G1A ← IOPAGE; C ← BA7; B ← BA6; A ← BA5

74LS138 11B		
Y7	7	N.C.
Y6	9	UART #2 EN
Y5	10	TIMER EN
Y4	11	UART #1 EN
Y3	12	N.C. (SMT)
Y2	13	N.C. (CLOCK)
Y1	14	N.C. (KEYBOARD)
Y0	15	THIGPIB EN

12A LS20: 12, 10, 13 → 8; 2, 1 → 6 → DATA ENABLE

DATA ENABLE → to sht. 4

P2 -38 EA3 -37 EA2 -36 EA1 → 74LS244 10F

74LS138 C9D: G2 ← GND; G1B ← GND; G1A ← BHE; C ← BA3; B ← BA2; A ← BA1

74LS138 C9D			
Y7	7	(F)	WR THRES4-7 → to sht. 2
Y6	9	(D)	N.C.
Y5	10	(B)	WR VAR B HI → To SHT 1
Y4	11	(9)	WR VAR A HI → to sht. 1
Y3	12	(7)	N.C.
Y2	13	(5)	WR ADC HI (8 MSB's) → to sht 2
Y1	14	(3)	WR GPIB CONT. → to sht. 3
Y0	15	(1)	WR BUS MAN. → to sht. 3

RP13 +5 → 74LS244 10F → WR, GND2, RD, GND1 → LS244 11F → BWR, BRD

A2, A1, RD, BWR → To SHT 4

74LS138 10D: G2 ← GND; G1B ← GND; G1A ← BLE; C ← BA3; B ← BA2; A ← BA1

74LS138 10D			
Y7	7	(E)	WR THRES0-3 → to sht. 2
Y6	9	(C)	WR THRES1,9 → to sht. 2
Y5	10	(A)	WR VAR B LO → to sht 1
Y4	11	(8)	WR VAR A LO → to sht. 1
Y3	12	(6)	WR ADC SEL → to sht 2
Y2	13	(4)	WR ADC LO (4-554) → to sht. 2
Y1	14	(2)	WR PP DATA → to sht. 3
Y0	15	(0)	WR BUS DATA → to sht. 3

RP16 +5 → GND4, BHE, BA0 → LS240 11F → BHE, BLE (A0)

RD → 74LS138 11D

74LS138 11D			
Y7	7		
Y6	9		
Y5	10		
Y4	11		
Y3	12		
Y2	13		
Y1	14	(3)	RD GPIB CONT. → to sht. 3
Y0	15	(1)	RD BUS MAN. → to sht. 3

RESET → LS244 11F → BRESET → to shts 1, 2, 3, 4

P2 -16 GND3

74LS138 10B: G2 ← GND; G1B ← GND; G1A ← RD; C ← BA3; B ← BA2; A ← BA1

74LS138 10B			
Y7	7	(E)	
Y6	9	(C)	
Y5	10	(A)	
Y4	11	(8)	
Y3	12	(6)	
Y2	13	(4)	RD ADC → to sht. 2
Y1	14	(2)	RD GPIB ADDS → to sht. 3
Y0	15	(0)	RD BUS DATA → to sht. 3

P2 -32 BD15 -31 BD14 -30 BD13 -29 BD12 -28 BD11 -27 BD10 -26 BD9 -25 BD8 → 74LS245 14F: DIR ← +5; EN ← GND; A7..A0 → BD15..BD8; B7..B0 → D15..D8

P2 -24 BD7 -23 BD6 -22 BD5 -21 BD4 -20 BD3 -19 BD2 -18 BD1 -17 BD0 → 74LS245 12F: DIR ← +5; EN ← GND; A7..A0 → BD7..BD0; B7..B0 → D7..D0

RP17, RP18, RP14, RP15: 3K/6.2K → +5

D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 → to shts. 1,2,3,4

								MPU INTERFACE	1
-50	-40	-30	-20	-10	PART NUMBER		PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING. REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE: DIMENSIONAL: X = .1 ANGLES; XX = .020 = 1°; XXX = .010; HOLE SIZE: 0.598 = 003, 600.598 = 004, 1.000-1.499 = 005

DRAWN Kent DATE 11-4-82; CHECKED; PROJ. ENG.; MANUFACTURING; QUALITY ASSUR

DASH NO. | NUMBER NEXT ASSEMBLY | QTY | ENG. SERV. | DATE

GOULD biomation

TITLE SCHEMATIC
THRESHOLD/GPIB/RS232

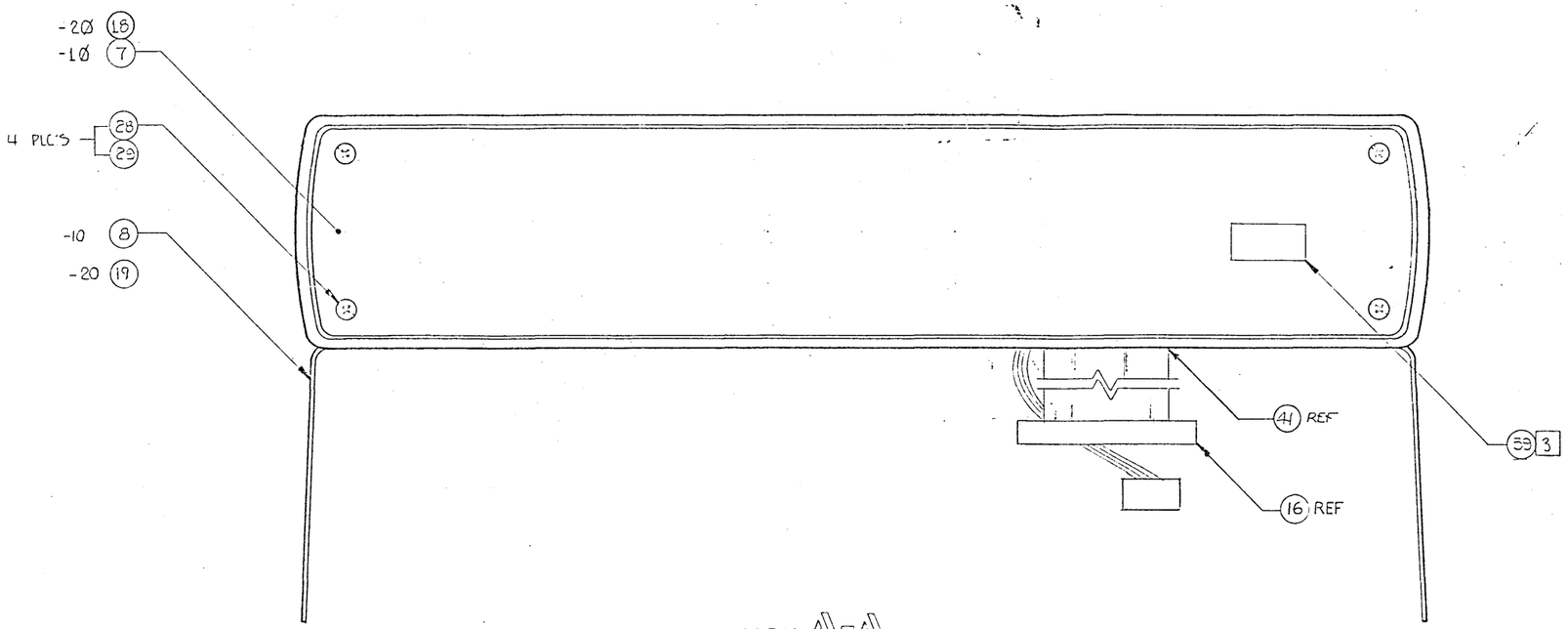
SCALE	SIZE	PART NUMBER	REV
—	D	0114-0171	AC

CODE IDENT K500/K505 | SHEET 5 OF 5

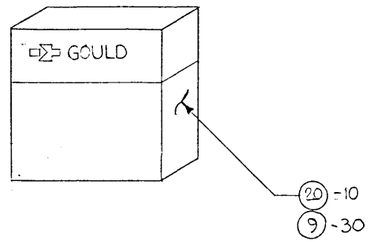
KLINGLER KVEL H

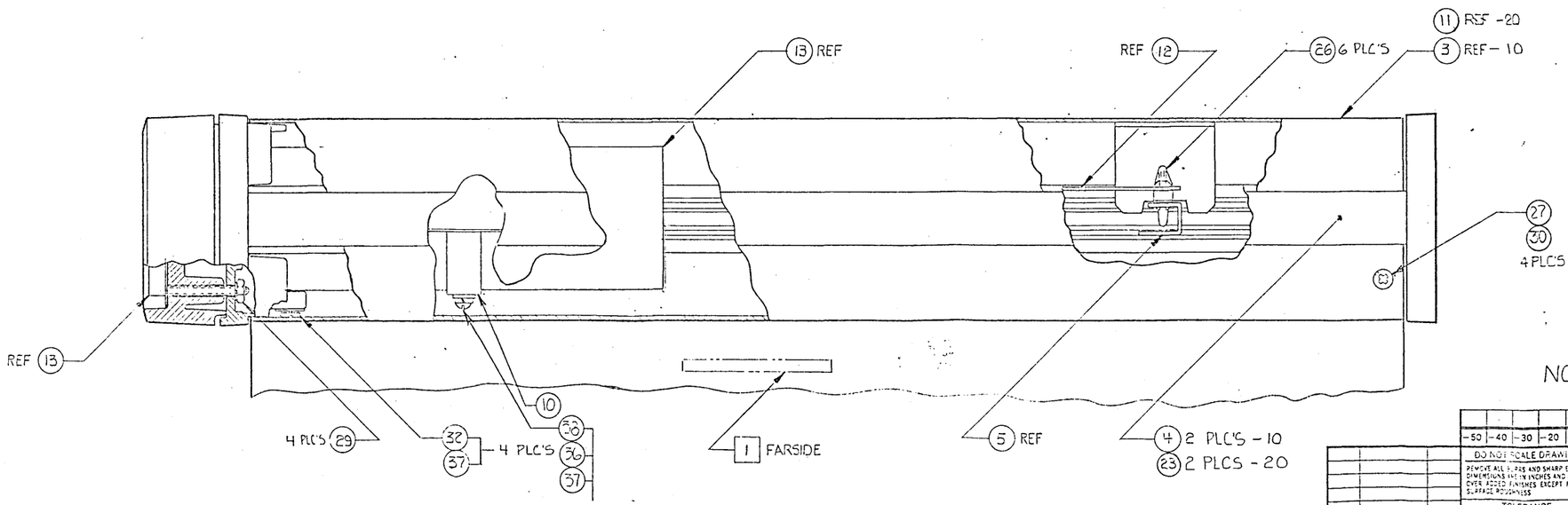
DWG. NO. 0114-0033 | SH 1 | REV U

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		REL PER ERN # 272	[illegible]	[illegible]	[illegible]
	B		PER ECO # 2718	[illegible]	[illegible]	[illegible]
	C	2728	REVISED PER ECO N°	[illegible]	[illegible]	[illegible]
	C		PROD REL ERN # 287	[illegible]	[illegible]	[illegible]
	D	2766	REVISED PER ECO #	[illegible]	[illegible]	[illegible]
	E	3795	REVISED PER ECO N°	[illegible]	[illegible]	[illegible]
	F	3767	REV'D PER ECO #	[illegible]	[illegible]	[illegible]
	G	3980	REV'D PER ECO#	[illegible]	[illegible]	[illegible]
	H	4015	REVISED PER ECO N°	[illegible]	[illegible]	[illegible]
	J	4097	REVISED PER ECO N°	[illegible]	[illegible]	[illegible]
	K	4125	REVISED PER ECO N°	[illegible]	[illegible]	[illegible]
	L	4149	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	M	4202	PER ECO 4202	[illegible]	[illegible]	[illegible]
	N	4481	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	P	4664	PER ECO 7-3-84	[illegible]	[illegible]	[illegible]
	Q	4792	REVISED PER ECO 11-21-84	SAR	[illegible]	[illegible]
	R	4987	REV L/M PER ECO 4-3-85	SAR	[illegible]	[illegible]
	S	5098	REV PER ECO 11/13/85	[illegible]	[illegible]	[illegible]
	T	5144	REV. L/M PER ECO 11/01/85	[illegible]	[illegible]	[illegible]
	U	5172	REV'D BOM ONLY 2/6/86	[illegible]	[illegible]	[illegible]



VIEW A-A
ROTATED CLOCKWISE 90°





VIEW B-B
ROTATED COUNTER CLOCKWISE 90°

[3] TYPE ASSY NO. 0114-0468 APPROPRIATE DASH NO, CURRENT REV LEVEL, AND SERIAL NO.

[2] VIEW B-B SHOWS TEAC DRIVES. OTHER APPROVED DRIVES MAY BE USED. BOTH DRIVES MUST BE MFG'D BY THE SAME VENDOR.

[1] TYPE ASSY NO. 0114-0468 APPROPRIATE DASH NO, CURRENT REVISION LETTER AND SERIAL NO.

NOTES: UNLESS OTHERWISE SPECIFIED.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: X = 1 ANGLES; .XX = .020 = 1°; .XXX = .010
HOLE SIZE: 0.599 = .003; 600-999 = .004; 1.000-1.499 = .005

DASH NO.	NUMBER	QTY
-20	0120-0002	1
	NEXT ASSEMBLY	

DRAWN [illegible] DATE [illegible]
CHECKED R. Gleason 11/12/82
PROJ. ENG. Curt 12/5/82
MANUFACTURING [illegible] 11/12/82
QUALITY ASSUR [illegible]
ENG. SERV. R. Gleason DATE 11/12/82

GOULD biomation

TITLE TOP ASSY, FLOPPY DISK HOUSING.

SCALE	SIZE	PART NUMBER	REV
1/1	D	0114-0466	U

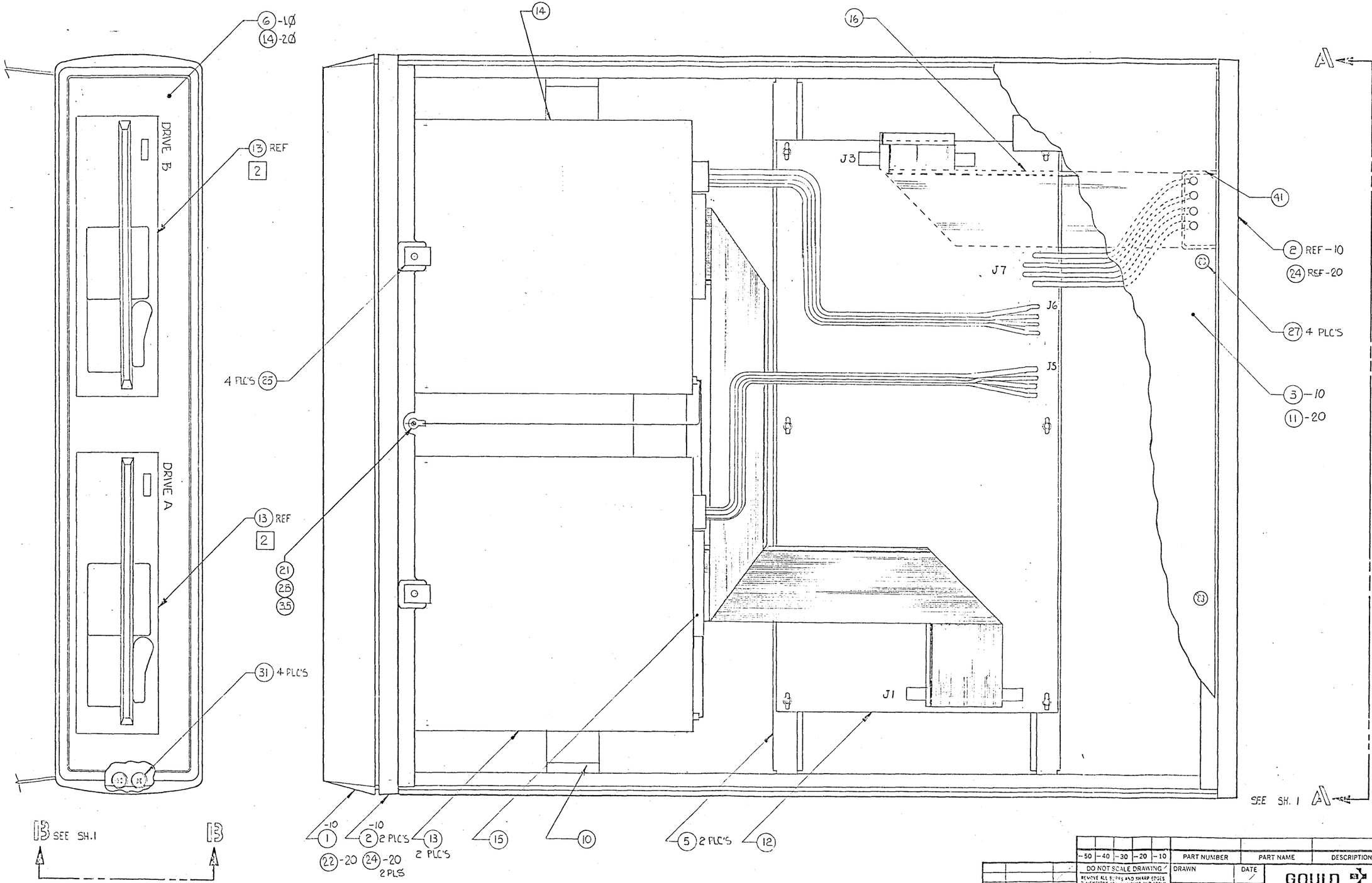
CODE | SHEET 1 OF 2

KLINGLER K-VEL M

DWG. NO.	SH	REV
0114-0468	2	U

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
—	—	—	SEE SH 1	—	—	—



ITEM	DESCRIPTION/SPECIFICATION	PART NAME	PART NUMBER	-10	-20	-30	-40	-50
1								

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = .1, XX = .020 = 1°, XXX = .010

HOLE SIZE: 0 .599 = .003; .500-.598 = .004; 1.000-1.499 = .005

DASH NO.	NUMBER NEXT ASSEMELY	QTY

		DATE
DRAWN		
CHECKED		
PROJ. ENG.		
MANUFACTURING		
ENG. SERV.		
QUALITY ASSUR		

GOULD biomation

TITLE: TOP ASSY, FLOPPY DISK HOUSING.

SCALE	SIZE	PART NUMBER	REV
1/1	D	0114-0468	U

CODE | SHEET 2 OF 2

KLINGLER KVEL H

BILL OF MATERIAL

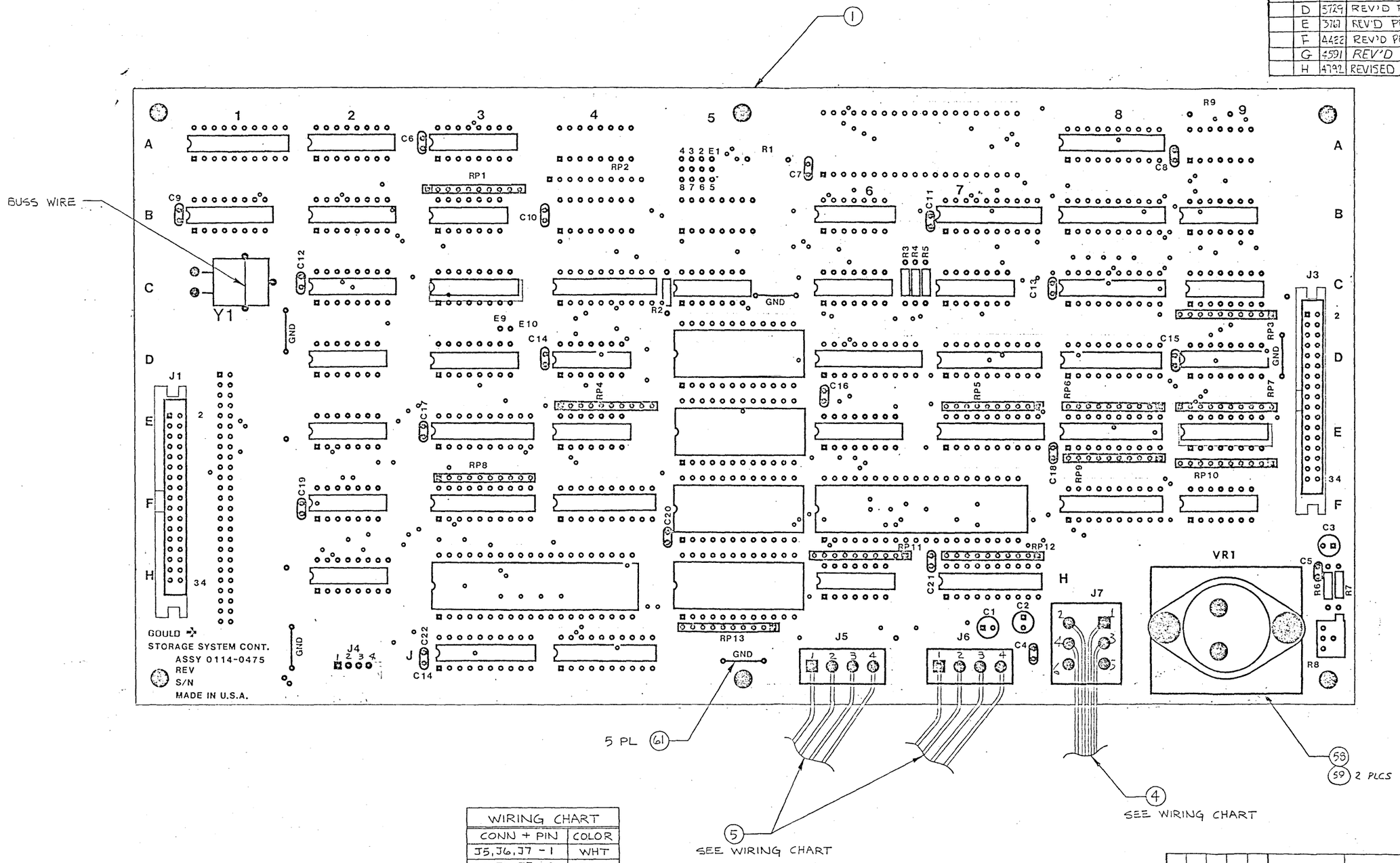
AS OF 02/12/86

0114-0468-20 ASSY,TOP,FLPY DSK HOUSING,K205
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0114-0468	DWG,ASSY,FLOPPY DISK HOUSING	0	EA	REF
5	0114-0469-10	BRCKT,PCB SUPP,K101/102/205	2	EA	
10	0114-0441-10	BRACKET,SUPPORT,FLOPPY DISK	1	EA	
11	0114-0466-30	COVER,TOP,K205	1	EA	
12	0114-0475-10	ASSY,PCB,STR SYS CTRL,K101/102	1	EA	
13	7500-0003-10	FLOPPY DISK DR 5" 1/2 HT	2	EA	
14	0114-0470-40	PANEL,FRONT,K205	1	EA	
15	0117-0164-10	ASSY,CABLE,I/O TO FLOPPY,K105	1	EA	
16	0114-0482-10	ASSY,CBL,K101 TO FDC SIGNALS	1	EA	
18	0117-0169-30	PANEL,REAR,DOS,K101,K102,K105	1	EA	
19	0114-0467-30	COVER,K205	1	EA	
21	0114-0485-10	ASSY,GROUND HARNESS,K101,K102	1	EA	
22	0114-0462-30	BEZEL,FRONT,K205	1	EA	
23	0114-0465-30	SIDE RAIL,K205	2	EA	
24	0114-0463-30	BEZEL,REAR,K205	2	EA	
25	7000-0334-10	HDWR "U" SPEED NUT FSTNR	4	EA	
26	7000-0461-10	HDWR PCB PLASTIC SPRT	6	EA	
27	7021-2632-12	SCR,X,FH 100,6-32 X 3/8,SS	8	EA	
28	7011-1632-16	SCR,X,PH,6-32 X 1/2,STZN	5	EA	
29	7071-1632-00	NUT,S-LOCK,6-32,STD,STZN	8	EA	
30	7072-1632-00	HEX NUT,NYLON LCKING #6	4	EA	
31	7012-1600-20	SCREW,X,PH,6-32 X .625	8	EA	
32	7000-0463-14	SCR,X,PH,3 X 14MM STZN	4	EA	
35	7086-1006-00	WSHR,EXT TOOTH LOCK,#6,STZN	1	EA	
36	7000-0463-08	SCREW 3MM X 8MM	4	EA	
37	7082-1004-00	WSHR,FLAT,#4,LP,STZN	8	EA	
38	7085-1004-00	WSHR,INT TOOTH LOCK,#4,STZN	4	EA	
40	7200-0044-10	GROMMET,FLEX,SPGS-2,ROLL	0	FT	

DWG. NO. 0114-0475 SH 1 REV H

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	—	PROTOTYPE	TMH		
	B	—	REVISED 7-19-82	TMH		
	B	—	REL PER ERN # 275			11/12/82
	C	2704	REVISED PER ECO	HA		
	C		PROD REL ERN 287	HA		
	D	3729	REV'D PER ECO	NW		8/4/83
	E	3761	REV'D PER ECO	SHR		11/30/83
	F	4422	REV'D PER ECO	NW		4/3/84
	G	4591	REV'D PER ECO	SHR		6/19/84
	H	4792	REVISED PER ECO 11-21-84	SHR		12/4/84



WIRING CHART	
CONN + PIN	COLOR
J5,J6,J7 - 1	WHT
J5,J6,J7 - 2	BLK
J5,J6,J7 - 3	BLK
J5,J6,J7 - 4	RED

DASH NO.	NUMBER	QTY
-10	0114-0463	1
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: X = 1 ANGLES: XX = .020 = 1° XXX = .010
HOLE SIZE: 0.599 = 003 .650 .959 = 004 1.000 1.499 = 005

ENG. SERV. DATE
DRAWN TMH 7/7/82
CHECKED Curt 11/12/82
PROJ. ENG. Curt 11/12/82
MANUFACTURING 11/12/82
QUALITY ASSUR. 11/12/82

GOULD biomation

TITLE ASSEMBLY - STORAGE SYSTEM CONTROLLER

SCALE	SIZE	PART NUMBER	REV
2/1	D	0114-0475	H

CODE SHEET 1 OF 1

ITEM	DESCRIPTION/SPECIFICATION	PART NAME	PART NUMBER
1			

KLINGLER KVEL H

BILL OF MATERIAL

AS OF 02/12/86

0114-0475-10 ASSY,PCB,STR SYS CTRL,K101/102
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0114-0475	DWG,ASSY,STOR SYS CONTROL,PWB	0	EA	REF
0	D0114-0476	DWG,SCHEM,S.S. CONTROLLER	0	EA	REF
1	0114-0477-10	PCB FAB STOR. SYS. CONT	1	EA	
2	0114-0474-10	PROM 32X8 DGTL PHASE LKD LOOP	1	EA	3C
3	0114-0479-10	PROM, I/O ADRS DECOD STOR SYS	1	EA	9E
4	0114-0429-10	ASSY,CBL,FDC PWR IN	1	EA	J7
5	0114-0481-10	ASSY,CBL,PWR,FDC TO FLOPPY	2	EA	J5,6
6	1700-0109-10	IC LM350K VOLT REG 3AMP	1	EA	VR1
7	1800-0085-10	IC 7407N HEX BUFFER/DR	2	EA	2E,2F
8	1800-0097-10	IC 7406N HEX INV BUF/DR	1	EA	2D
10	1800-0106-10	IC 74LS02N, 14, NOR, X4	1	EA	5C
11	1800-0109-10	IC 74LS08N 14, AND, X4	2	EA	7C,6B
12	1800-0110-10	IC 74LS10N TRIPLE NAND	1	EA	9F
13	1800-0115-10	IC 74LS74N, 14, FF, D, X2	4	EA	3B 6C,4E,4D
14	1800-0125-10	IC 74LS161N 20CNTR, SYN, BIN	2	EA	3A,2C
15	1800-0181-10	IC 74LS151N 16DATA SEL, 1/8	1	EA	3D
16	1800-0193-10	IC 74LS138N 16 DCDR, 3TO8	3	EA	6E,9C,9D
17	1800-0216-10	IC 74LS32N QUAD 2-INPUT	1	EA	6H
18	1800-0217-10	IC 74LS153N DUAL 4 TO 1	2	EA	2A,2B
19	1800-0231-10	IC 74LS273N 20 FF, D, X8	4	EA	4C 8D,8C,3E
20	1800-0237-10	IC 74LS139N DUAL 2 TO 4	1	EA	2H
21	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	3	EA	6D,8A,8B
22	1800-0267-10	IC 74LS240N OCTAL LINE	3	EA	7B,3F,4F
23	1800-0268-10	IC 74LS245N BUS TRANS	3	EA	8F,8E,7D
24	1800-0293-10	IC 74LS374N D F/F 3 STA	1	EA	7H
25	1800-0298-10	IC 74LS373N OCTAL D TYP	1	EA	7E
26	1800-0311-10	IC 7438N QUAD 2-INPUT	1	EA	9B
28	1800-0342-10	IC 8272 FLOP DISK CONT	1	EA	3H
29	1800-0357-10	IC 74LS629N VOLT CONT	1	EA	1B
30	1800-0358-10	IC P8257-5 DMA CONTROLLER	1	EA	6F
34	1820-0080-10	IC HM6116LP-3 2KX8 ST RAM CMOS	2	EA	5F,5H
37	3000-1001-10	RES,1K,5%,1/4W,C	1	EA	R7
38	3000-2201-10	RES,2.2K,5%,1/4W,C	4	EA	R2-5
39	3000-6806-10	RES,68,5%,1/4W,C	1	EA	R6
40	3300-0092-10	POT,100,0.25W,10% 12T,PC,STR	1	EA	R8
41	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	8	EA	9-13 RP3,5,6
42	3700-0083-10	RPAK,2.2K,0.18W,2%,10/9	3	EA	RP1,4,7
43	3700-0100-10	RPAK 150 OHM .18W 2% 10/9	1	EA	RP8
45	4010-0103-10	CAP,0.01UF,50V,10%,CER	19	EA	C4-22
46	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	1	EA	C1
47	4400-0045-10	CAP,33UF,25V,ELCTLT	2	EA	C2,3
49	5100-0021-10	XTAL 16.00 MHZ	1	EA	Y1
52	6000-0574-10	CONN HEADER 34 PIN	2	EA	J1,3

BILL OF MATERIAL
AS OF 02/12/86

0114-0475-10 ASSY,PCB,STR SYS CTRL,K101/102
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
54	6100-0122-10	SKT 24 PIN DIP	4	EA	X5D,X5E X5F,X5H
55	6100-0123-10	SKT 40 PIN DIP	2	EA	6F,3H
56	6100-0120-10	SKT 16 PIN DIP LO-PROFIL	2	EA	3C,9E
58	7000-0460-20	HEATSINK TO-3 BASE ONLY	1	EA	FOR VR1
59	7071-0632-00	#6 KEP NUT SM. PATT	2	EA	
60	7200-0016-10	INSULATOR TO-3	2	EA	HEATSINK VR1;
61	9000-0054-10	BUSS WIRE, FORMED	5	EA	
62	7011-0632-12	SCR,X,PH,6-32 X 3/8,STCD	2	EA	
63	7081-1006-00	WSHR,FLAT,#6,STZN	2	EA	

DWG. NO. 0114-0476 | SH 1 | REV. H

REVISIONS					
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
-	A	—	Eng. prototype	CB		6-3-82
-	B	—	REL PER ECN # 275			
—	C	—	REVISED PER # 2704	RC		
	C		P200 REL ECN 287	HA		
	D	3729	REVISED PER ECO #	DGW	DGW	5/31/83
	E	3767	REV'D PER ECO #	SM	DGW	7/13/83
	F	AA22	REVISED PER ECO	KW		9/2/84
	G	4591	REVISED PER ECO	RTM		6-27-84
	H	4792	REVISED PER ECO 11/21/84	SHR	DGW	11/21/84

NOTES:
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITORS ARE IN UF, 50V, 10%

3 COMPONENTS NOT LOADED

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING — REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ASSED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE: DIMENSIONAL: X = .1 ANGLES; XX = .020 = 1°; XXX = .010; HOLE SIZE: 0.593 = .003, 600.999 = .004, 1.000-1.499 = .005

DRAWN	Cust	DATE	4/19/82
CHECKED	Cust		4/25/82
PROJ. ENG.	Cust		6/29/82
MANUFACTURING			11/12/82
QUALITY ASSUR			11/12/82
ENG. SERV.	R. Gibson	DATE	11/12/82

DASH NO. | NUMBER | QTY | NEXT ASSEMBLY

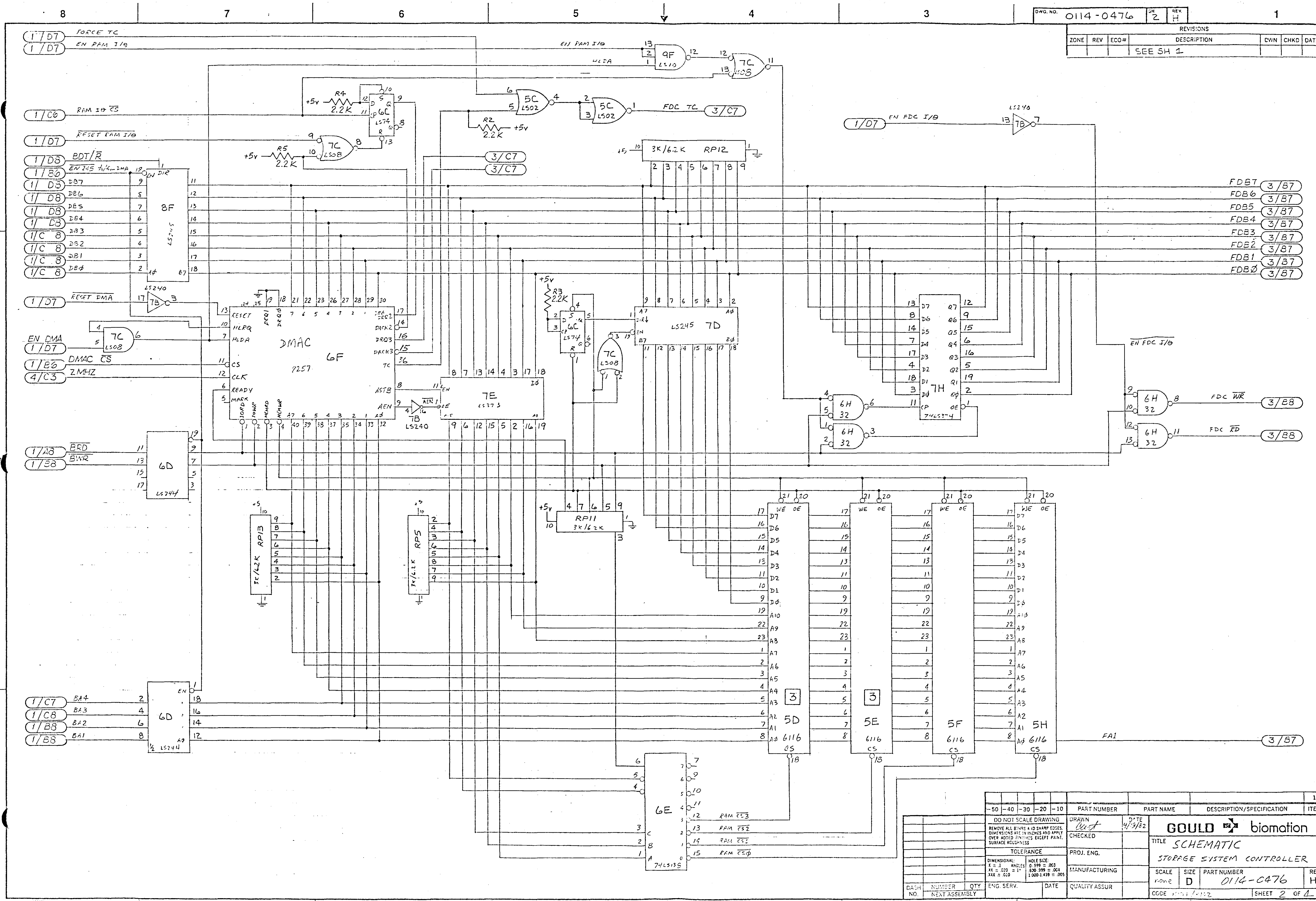
GOULD biomation

TITLE: SCHEMATIC - STORAGE SYSTEM CONTROLLER

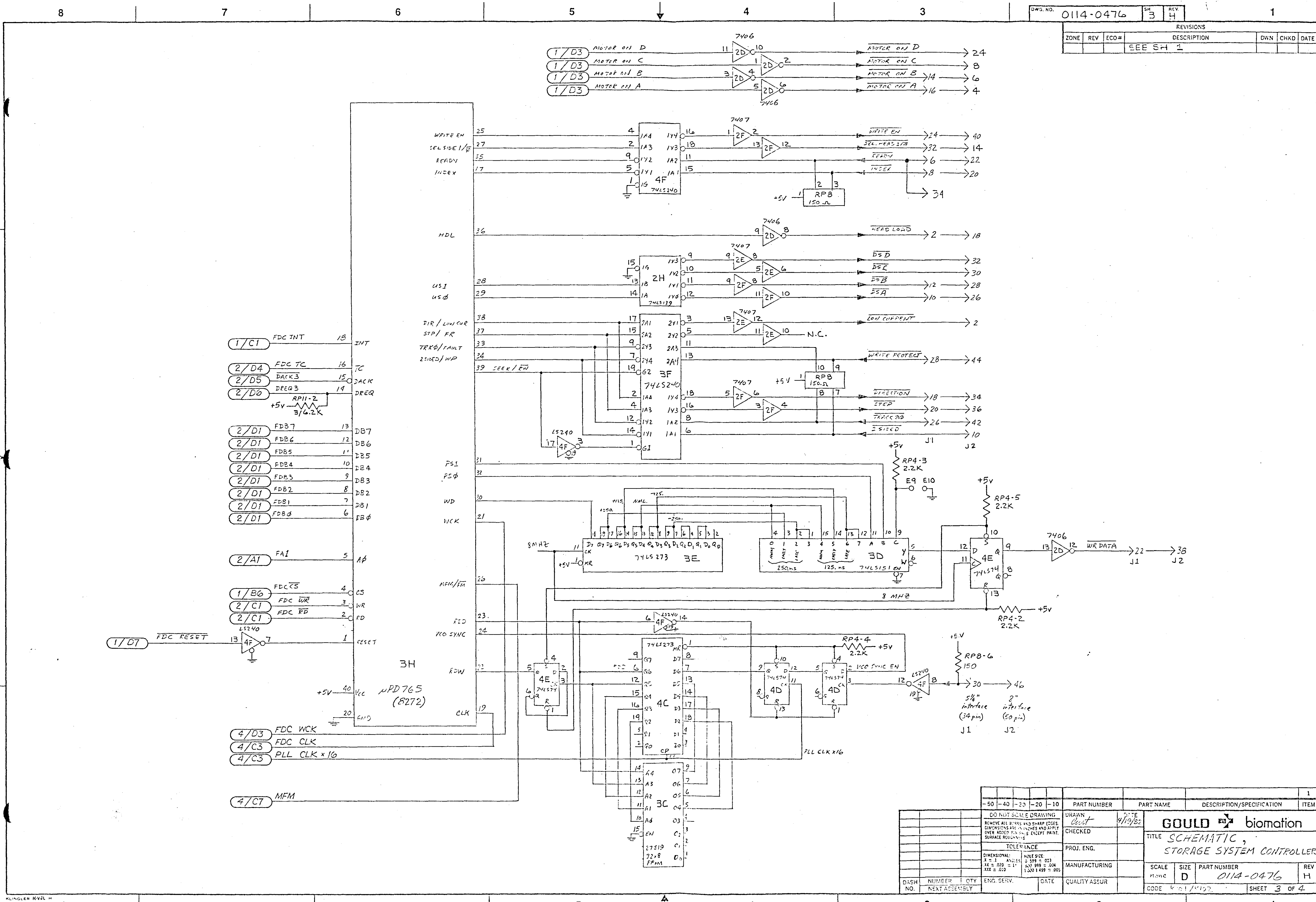
SCALE	SIZE	PART NUMBER	REV
—	D	0114-0476	H

CODE | SHEET 1 OF 4

KLINGLER K-VEL H



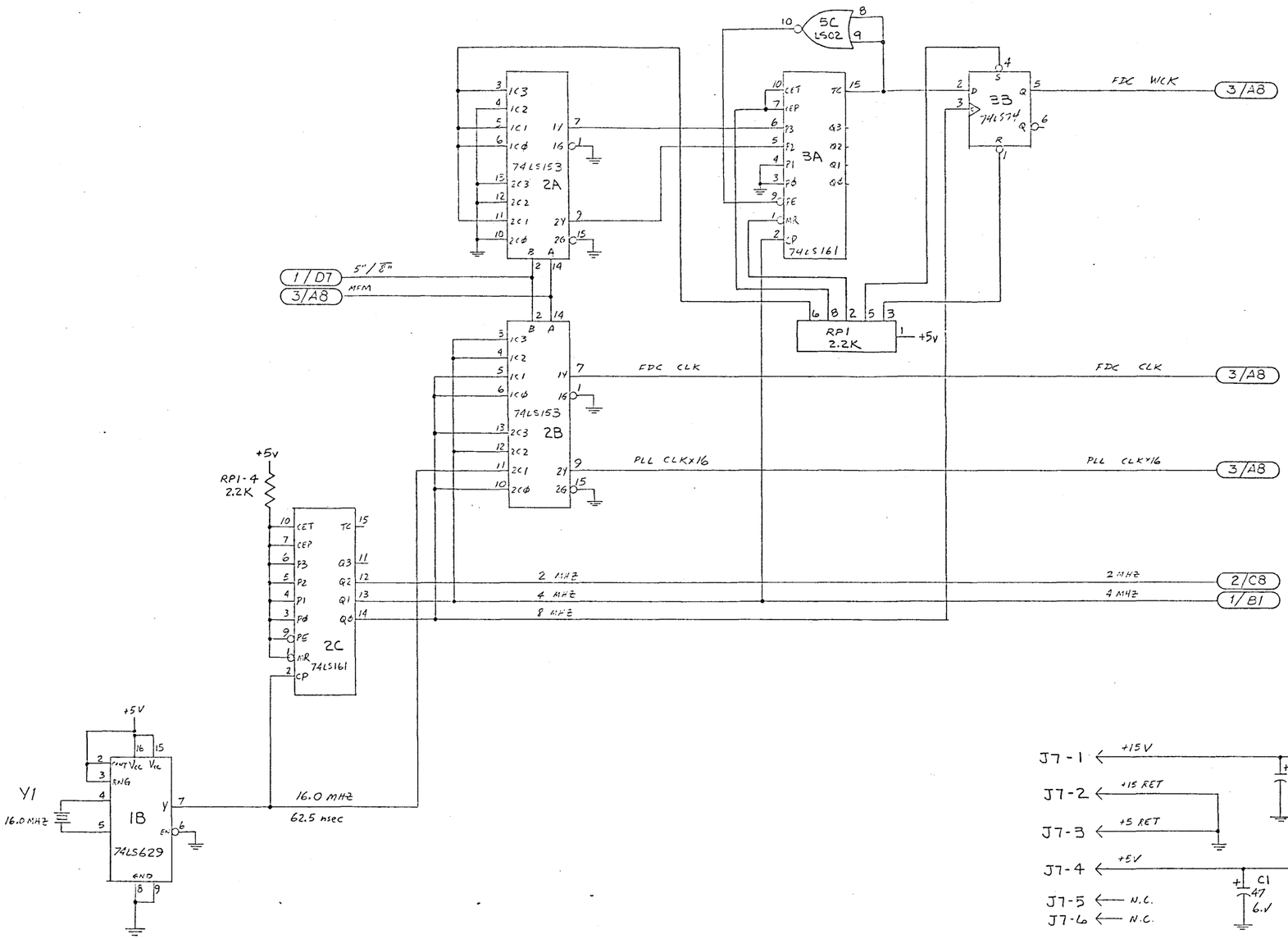
DWG. NO. 0114-0476 SH 2 REV. H
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
SEE SH 1
FORCE TC
EN RAM I/O
RAM I/O CS
RESET RAM I/O
BDT/R
EN 245 to/from DMA
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
8F
LS245
RESET DMA
LS240
7B
EN DMA
7C
LS08
DMAC CS
2MHZ
DMAC
6F
8257
RESET
HLRQ
HLDA
CS
CLK
READY
MARK
IORD
IOWR
MEMRD
MEMWR
DRQ2
DACK2
DRQ3
DACK3
TC
ASTB
AEN
R4
R5
R2
R3
2.2K
+5v
6C
LS74
9F
LS10
5C
LS02
HLDA
EN RAM I/O
FDC TC
3/C7
RP12
3K/6.2K
7E
LS373
7D
LS245
EN FDC I/O
LS240
FDB7
FDB6
FDB5
FDB4
FDB3
FDB2
FDB1
FDBØ
3/B7
7H
74LS374
6H
32
FDC WR
FDC RD
3/B8
BRD
BWR
6D
LS244
RP13
RP5
3K/6.2K
RP11
BA4
BA3
BA2
BA1
1/2 LS244
5D
5E
5F
5H
6116
WE
OE
CS
FA1
3/B7
6E
74LS138
RAM CS3
RAM CS2
RAM CS1
RAM CSØ
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: X = .1 ANGLES .XX = .020 ± 1° .XXX = .010
HOLE SIZE: 0-.599 = .003 .600-.999 = .004 1.000-1.499 = .005
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
DATE 4/19/82
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV.
DASH NO.
NUMBER
NEXT ASSEMBLY
QTY
GOULD biomation
TITLE SCHEMATIC
STORAGE SYSTEM CONTROLLER
SCALE none
SIZE D
PART NUMBER 0114-0476
REV H
SHEET 2 OF 4
KLINGLER K-VEL H

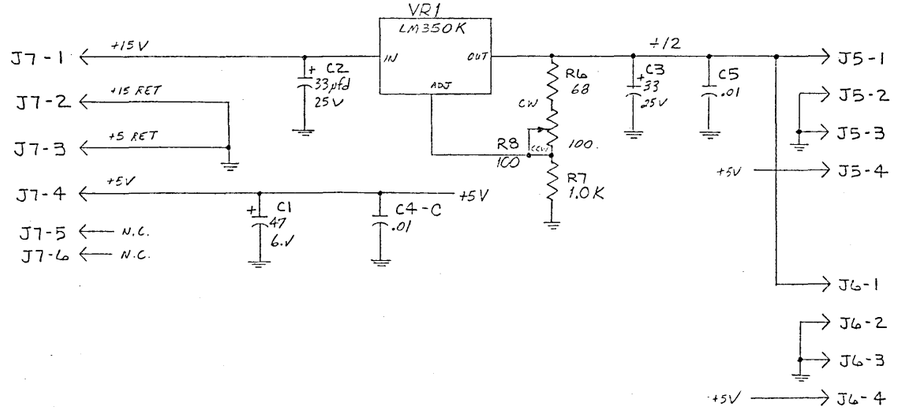

DWG. NO. 0114-0476 SH 3 REV. H
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SH 1
1/D3 MOTOR ON D
1/D3 MOTOR ON C
1/D3 MOTOR ON B
1/D3 MOTOR ON A
7406 2D
MOTOR ON D 24
MOTOR ON C 8
MOTOR ON B 14 6
MOTOR ON A 16 4
WRITE EN
SEL SIDE 1/Ø
READY
INDEX
4F 74LS240
7407 2F
WRITE EN 24 40
SEL. HEAD 1/Ø 32 14
READY 6 22
INDEX 8 20
34
RP8 150 Ω
+5V
HDL
HEAD LOAD 2 18
2H 74LS139
US1
USØ
DS D 32
DS C 30
DS B 12 28
DS A 10 26
DIR / LOW CUR
STP / FR
TRKØ / FAULT
2SIDED / WP
SEEK / RW
3F 74LS240
LOW CURRENT 2
N.C.
WRITE PROTECT 28 44
DIRECTION 18 34
STEP 20 36
TRACK ØØ 26 42
2 SIDED 10
J1 J2
1/C1 FDC INT INT
2/D4 FDC TC TC
2/D5 DACK3 DACK
2/D6 DREQ3 DREQ
+5V RP11-2 3/6.2K
2/D1 FDB7 DB7
2/D1 FDB6 DB6
2/D1 FDB5 DB5
2/D1 FDB4 DB4
2/D1 FDB3 DB3
2/D1 FDB2 DB2
2/D1 FDB1 DB1
2/D1 FDBØ DBØ
2/A1 FA1 AØ
1/B6 FDC CS CS
2/C1 FDC WR WR
2/C1 FDC RD RD
1/D7 FDC RESET
LS240 4F
RESET
3H
µPD765 (8272)
+5V VCC
GND
4/D3 FDC WCK
4/C3 FDC CLK
4/C3 PLL CLK x16
4/C7 MFM
PS1
PSØ
WD
WCK
MFM/FM
RDD
VCO SYNC
RDW
CLK
+5V RP4-3 2.2K E9 E10
8MHZ
74LS273 3E
+250. +125. NML. -125. -250.
NORM EARLY LATE 250ns
NORM EARLY LATE 125. ns
3D 74LS151 EN
+5V RP4-5 2.2K
4E 74LS74
7406 2D
WR DATA 22 38
J1 J2
8 MHZ
RP4-2 2.2K +5V
LS240 4F
74LS273 4C MR
RP4-4 2.2K +5V
4D 74LS74
VCO SYNC EN
+5V RP8-6 150
LS240 4F
30 46
5¼" interface (34 pin) J1
8" interface (50 pin) J2
PLL CLK x16
3C 27S19 32x8 PROM
-50 -40 -30 -20 -10
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: .X ± .1 .XX ± .020 .XXX ± .010 ANGLES ± 1°
HOLE SIZE: 0 .599 ± .003 .600 .999 ± .004 1.000 1.499 ± .005
DRAWN DATE 4/19/82
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV. DATE
DASH NO. NUMBER NEXT ASSEMBLY QTY
GOULD biomation
TITLE SCHEMATIC, STORAGE SYSTEM CONTROLLER
SCALE none SIZE D PART NUMBER 0114-0476 REV H
SHEET 3 OF 4
KLINGLER K-VEL H

DWG. NO.	REV
0114-0476	H

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SH 1			





5"	MFM	DESCRIPTION	FDC CLK	PLL CLKx16	FDC WCK	Preset Hex	Preset Binary
0	0	8" SINGLE DENSITY	8 MHZ	8 MHZ	500 KHZ	8	1000
0	1	8" DOUBLE DENSITY	8 MHZ	16 MHZ	1 MHZ	C	1100
1	0	5" SINGLE DENSITY	4 MHZ	4 MHZ	250 KHZ	0	0000
1	1	5" DOUBLE DENSITY	4 MHZ	8 MHZ	500 KHZ	8	1000

ITEM	DESCRIPTION/SPECIFICATION	PART NAME	PART NUMBER
1			

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = .1 ANGLES; XX = .020 = 1°; XXX = .010

HOLE SIZE: 0-.599 = .003; .600-.999 = .004; 1.000-1.499 = .005

CASH NO. | NUMBER | QTY | NEXT ASSEMBLY

ENG. SERV. | DATE

DRAWN Cust | DATE 4/19/82

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE SCHEMATIC
STORAGE SYSTEM CONTROLLER

SCALE	SIZE	PART NUMBER	REV
—	D	0114-0476	H

CODE | SHEET 4 OF 4

KINGLER KVEL H

DWG NO	0114-2010	REV	N

REVISIONS

ZONE	REV.	ECO#	DESCRIPTION	DWN	CHKD	APPD
			SEE HISTORY			
	K	4730	REVISED PER ECO "	SAR	[illegible]	[illegible]
	L	5100	REVISED PER ECO	DAW		
	M	5121	REVISED PER ECO " 11-2-95	DAW	[illegible]	
	N	5139A	REVISED PER ECO 2/26/96	[illegible]		

JUMPER	AS STUFFED	-10 K500	-20 K1012	-30 K105	-40 K205	-50 K115	-60 K450	DESCRIPTION
E1 TO E2	OUT	JMP						SET SCAN RATE IN=2MS, OUT=1ONE
E3 TO E4	OUT							NOT USED
E5 TO E6	OUT							NOT USED
E7 TO E8	OUT	JMP						IN=K500 HOR Z SCAN OUT=K101
E9 TO E10	OUT						JMP	A18
E11 TO E12	IN							A17
E13 TO E14	IN							A16
E15 TO E16	IN							A15 } K101 CMOS RAM
E17 TO E18	IN							A14 } ADRESS SELECTION
E19 TO E20	IN							A13
E21 TO E22	IN							A12
E23 TO E24	IN						CUT	A13
E25 TO E26	IN							A8 } K500 MEM MAPPED I/O
E27 TO E28	IN							A7 } ADRESS DECODE
E29 TO E30	IN	CUT						IN SELECTS I/O MAPPED I/O K101
E30 TO E31	OUT	JMP						IN SELECTS MEM MAPPED I/O K500
E32 TO E33	IN	CUT						IN FOR K101
E33 TO E34	OUT	JMP						IN FOR K500
20-6 TO 20-14	IN		CUT					TEST FIX FOR K101
20-14 TO GND	OUT		JMP					TEST FIX FOR K101
E35 TO E36	OUT							
E37 TO E39	IN							
E38 TO E40	OUT							
E138 TO E139	IN					CUT		
E139 TO E140	OUT					JMP		

NOTES:

1. REMOVE MOUNTING HARDWARE SUPPLIED WITH T1, USE ITEM (100) TO SECURE TO BOARD.
2. IC'S 7E 9E RP2 & S1 ARE -10; IC 9E & RP2 ARE -20.
3. COMPONETS IN THIS AREA PLUS R57 ARE -20, -40 & -50 ONLY EXCEPT FOR R26 & R27.
4. SECURE BATTERY, B1, TO BOARD WITH ITEM (39) 2 PLS, BEFORE SOLDERING LEADS.
5. JUMPER E1 TO E2 AND E3 TO E4 ON SOLDER SIDE OF BOARD. USE 18AWG 19 STRAND WIRE. MAKE JUMPERS AS SHORT AS POSSIBLE.

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

-50	K115-XXX	
-40	0120-0004	
-10	0850-0002	
DASH NO.	NEXT ASSY	USED ON
FIRST APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN SG WRIGHT	5/14/86
CHECKED	
PROJ ENG	

GOULD Electronics

TITLE: ASSEMBLY DATA DISPLAY BOARD

SIZE D | DWG NO. 0114-2010 | REV N

SCALE | MODEL K705 K750 | SHEET 1 OF 2

DWG NO 0114-2010	SH 2	REV N

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD

-50 -10 -30 (124)
-20 -40 (115)

-20 -40 -50 ONLY (127) NEAR SIDE
(129) 2PL 4
-20 -40 -50 FAR SIDE (123)
(104)
(112)
(1)
5
(27)
(33) -10 -20 ORIENTATION ONLY
(120) 1
1.75
-30 -40 -50 ONLY (133) (134) (96) (92) (92)
-30 -40 -50 ORIENTATION ONLY (28)
3
-20/-40
-20 ASSY SHOWN
(115)

VOLUME
VERTICAL HEIGHT
VERTICAL HOLD
HORIZONTAL WIDTH
HORIZONTAL LINEARITY
FOCUS
BRIGHTNESS
VERT LINEARITY
SPARE
SPARE

P1 P2 P3 P4 P15 P16

-03	-02	-01	QTY PER ASSY	PART NUMBER	DESCRIPTION	ITEM NO.

PARTS LIST

DASH NO.	NEXT ASSY	USED ON
FIRST APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS ± ANGLES ±
.XX ± .01
.XXX ± .005

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN D. WRIGHT	5/10/82
CHECKED	
PROJ ENG	

GOULD Electronics

TITLE: ASSEMBLY DATA DISPLAY BOARD

SIZE	DWG NO.	REV
D	0114-2010	N

SCALE | MODEL | SHEET 2 OF 2

DATAPOINT CORP. SAN ANTONIO, TEXAS

BILL OF MATERIAL

AS OF 02/12/86

0114-2010-60 ASSY,PCB,DATA DISPLAY,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0114-2010	DWG,ASSY,DATA DISPLAY	0	EA	REF
0	D0114-2011	DWG,SCHEM,DATA DISPLAY	0	EA	REF
1	0114-2012-10	FAB,PCB,DATA DISPLAY	1	EA	
2	3000-2000-10	RES,200,5%,1/4W,C	3	EA	R35,36,64
3	3000-3307-10	RES,3.3,5%,1/4W,C	1	EA	R38
4	3050-4700-10	RES,470,5%,1/2W,C	2	EA	R8,9
5	3000-8206-10	RES,82,5%,1/4W,C	1	EA	R12
6	3000-4700-10	RES,470,5%,1/4W,C	2	EA	R5,34
7	3000-2201-10	RES,2.2K,5%,1/4W,C	12	EA	3,4,60,62 53-55,58 65 R19,1,2
8	3000-1002-10	RES,10K,5%,1/4W,C	4	EA	R17,18,52 R63
9	3000-5601-10	RES,5.6K,5%,1/4W,C	1	EA	R46
10	3000-8201-10	RES,8.2K,5%,1/4W,C	2	EA	R39,40
11	3000-4702-10	RES,47K,5%,1/4W,C	2	EA	R43,44
12	3000-1203-10	RES,120K,5%,1/4W	1	EA	R22
13	3000-2203-10	RES,220K,5%,1/4W,C	2	EA	R37,41
14	3000-2703-10	RES,270K,5%,1/4W,C	1	EA	R42
15	3000-5103-10	RES,510K,5%,1/4W,C	1	EA	R31
17	3000-1004-10	RES,1M,5%,1/4W,C	2	EA	R30,49
18	3050-2200-10	RES,220,5%,1/2W,C	1	EA	R24
19	3050-1007-10	RES,1,5%,1/2W,C	1	EA	R45
20	3050-3906-10	RES,39,5%,1/2W,C	2	EA	R25,57
21	3050-1000-10	RES,100,5%,1/2W,C	1	EA	R33
23	3000-2202-10	RES,22K,5%,1/4W,C	2	EA	R67,68
24	3200-0008-10	RES,1,3%,1W,WW	1	EA	R48
25	3070-1501-10	RES,1.5K,5%,1W,C	1	EA	R28
26	3100-7506-10	RES,75,1%,1/8W,MF	1	EA	R13
27	3100-6040-10	RES,604,1%,1/8W,MF	1	EA	R14
28	3100-8250-10	RES,825,1%,1/8W,MF	1	EA	R15
29	3100-9090-10	RES,909,1%,1/8W,MF	1	EA	R16
30	3300-0084-10	POT,50K,0.5W,20% 1T,PC,STR	1	EA	R47
31	3300-0085-10	POT,100K,0.5W,20% 1T,PC,STR	3	EA	R20,21,32
32	3300-0088-10	POT,1M,0.25W,30% 1T,PC,STR	1	EA	R29
33	4100-0024-10	CAP,68PF,500V,5%,MICA	1	EA	C43
34	4100-0002-10	CAP,470PF,500V,5%,MICA	1	EA	C39
35	4000-0009-10	CAP,0.1UF,100V,10%,CER	8	EA	44-46,C5,6 C33,35,42
36	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	5	EA	C1,4,24,27 C19
37	4000-0042-10	CAP,0.15UF,100V,5%,POLYTEST	2	EA	C36,49
39	4000-0043-10	CAP,0.01UF,500V,10%,CER	3	EA	C32,34,37
40	4010-0103-10	CAP,0.01UF,50V,10%,CER	26	EA	18,20,56 21-23,25

BILL OF MATERIAL
AS OF 02/12/86

0114-2010-60 ASSY,PCB,DATA DISPLAY,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
40	4010-0103-10	CAP,0.01UF,50V,10%,CER	26	EA	26,28,29 48,7,12,17 57,58,59 8 9,13,14,16 C40,41,2,3
41	4010-0100-10	CAP,10PF,50/100V,5%,CER	1	EA	C11
42	4400-0036-10	CAP,1000UF,16V,10%,ELCTLT	1	EA	C51
43	4400-0037-10	CAP,470UF,25V,10%,ELCTLT	2	EA	C47,54
44	4400-0047-10	CAP,220UF,40V,-10% +50%,ELCTLT	1	EA	C50
45	4200-0036-10	CAP,6MF,200V,10%,POLYCARB	1	EA	C52
46	4400-0038-10	CAP,100UF,100V,-10%+100%,ELCTL	1	EA	C38
47	7000-0451-10	BATTERY, N.I.C.D. 2.4V	1	EA	B1
48	1200-0033-10	RECT 3SF4 3 AMP	1	EA	CR5
49	1200-0031-10	RECT 1N4937 1 AMP	3	EA	CR3,4,6
50	4300-0041-10	CAP,0.056UF,400V,10%,TNTLM	1	EA	C53
51	3000-3900-10	RES,390,5%,1/4W,C	1	EA	R66
52	6100-0151-10	SKT 28 PIN DIP LO PROFIL	3	EA	X2E,X1B X3B
54	4600-0010-10	CAP,7-40PF,100V,CER	1	EA	C10
55	1300-0028-10	TRAN 2N3904	2	EA	Q2,6
56	1400-0019-10	TRAN 2N3906	1	EA	Q1
57	1300-0049-10	TRAN BU407	1	EA	Q5
58	1300-0048-10	TRAN 2N4921	1	EA	Q4
59	6100-0120-10	SKT 16 PIN DIP LO-PROFIL	2	EA	X8B,X10B
60	3000-6800-10	RES,680,5%,1/4W,C	1	EA	R51
62	3700-0083-10	RPAK,2.2K,0.18W,2%,10/9	8	EA	12,15,20 14 RP1,5,6,9
63	3700-0085-10	RPAK,22K,0.3W,2%,10/9	5	EA	21 RP3,7,8,11
64	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	7	EA	4,13 RP10,16-19
65	1500-0018-10	TRAN VN10KM	1	EA	Q3
66	1800-0105-10	IC 74LS00N 2-IN NAND LOW	1	EA	7C
67	1800-0123-10	IC 74LS14N HEX SCHMITT	1	EA	6C
68	1800-0110-10	IC 74LS10N TRIPLE NAND	2	EA	9D,5D
69	1800-0111-10	IC 74LS20N DUAL 4-IN	1	EA	8D
70	1800-0115-10	IC 74LS74N, 14, FF, D, X2	2	EA	7B,17E
71	1800-0254-10	IC 74LS85N 4-BIT MAG	2	EA	5E,6E
72	1800-0404-10	IC 74LS136N 14 XOR X4	1	EA	9C
73	1800-0301-10	IC 74LS156N 16	1	EA	14E
74	1800-0125-10	IC 74LS161N 20CNTR, SYN, BIN	6	EA	15E,16E 7A-10A
75	1800-0121-10	IC 74LS175N QUAD D F/F	1	EA	9B
76	1800-0267-10	IC 74LS240N OCTAL LINE	3	EA	10D,4E,6B

BILL OF MATERIAL
AS OF 02/12/86

0114-2010-60 ASSY,PCB,DATA DISPLAY,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
77	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	3	EA	13E,5B,1D
78	1800-0268-10	IC 74LS245N BUS TRANS	3	EA	10E,3C,4C
79	1800-0231-10	IC 74LS273N 20 FF, D, X8	3	EA	12E,3D,4D
80	1800-0193-10	IC 74LS138N 16 DCDR, 3TO8	1	EA	8E
81	1800-0097-10	IC 7406N HEX INV BUF/DR	2	EA	10C,18E
82	1800-0038-10	IC 74S20N 14 NAND X2	1	EA	8C
84	1820-0080-10	IC HM6116LP-3 2KX8 ST RAM CMOS	2	EA	1B,3B
85	1800-0319-10	IC D8259A PROG INTR CNT	1	EA	2E
87	1700-0082-10	IC TDA1170/S TV VERT DEF	1	EA	11B
88	1800-0341-10	IC MSM5832 MICRO-PROC	1	EA	2D
89	1800-0311-10	IC 7438N QUAD 2-INPUT	1	EA	7D
91	9000-0049-10	WIDTH COIL	1	EA	L1
92	0113-0011-10	ASSY,HORIZONTAL COIL	1	EA	L2
93	5100-0018-10	XTAL 32.768KHZ,	1	EA	Y1
94	0113-0014-10	ASSY,XFMR,HORIZ DRIVE	1	EA	T1
95	9000-0082-10	ASSY,FLYBACK TRANSFORMER,FINIS	1	EA	T2
96	7000-0365-10	HTSK TO-202	1	EA	@ Q5
97	7000-0366-10	HTSK	1	EA	@ 11B
98	7000-0221-10	WSHR SHLDR INS R	1	EA	@ Q5
99	7200-0017-10	INSULATOR TO 220	1	EA	@ Q5
101	6000-0359-06	CONN 6 PIN HDR	1	EA	P1
102	6000-0359-08	CONN 8 PIN HDR	1	EA	P2
103	6000-0359-10	CONN 10 PIN HDR	1	EA	P3
104	7000-0120-10	CARD EJECTOR NYLON 6/6	1	EA	
105	9000-0054-10	BUSS WIRE, FORMED	1	EA	GND
106	7200-0032-10	MOUSETAIL, 4" LONG	2	EA	
108	3000-1001-10	RES,1K,5%,1/4W,C	2	EA	R10,69
109	3000-2200-10	RES,220,5%,1/4W,C	1	EA	R26
110	3000-3300-10	RES,330,5%,1/4W,C	1	EA	R27
111	3300-0096-10	POT,1K,0.5W,20% 1T,PC,STR	1	EA	R56
112	7400-0002-10	BUZZER/ALARM	1	EA	
113	1700-0071-10	IC LF356AN MONO OP AMP	1	EA	11C
114	4400-0045-10	CAP,33UF,25V,ELCTLT	1	EA	C55
115	0112-0228-08	CARD EJECTOR-HOT STAMPED (A8)	1	EA	
116	1800-0351-10	IC 74LS12N 3-IN NAND	1	EA	5C
117	1800-0352-10	IC 74LS22N 4-IN NAND OPE	1	EA	6D
118	3000-5106-10	RES,51,5%,1/4W,C	1	EA	R61
119	1000-0002-10	DIO,1N4152	1	EA	CR7
120	8300-0027-10	TAPE,FOAM,1X1X1/8"	0	FT	SS OF 3A
121	4000-0011-10	CAP,2.2UF,50V,20%,0.2LS,CER	1	EA	C61
122	6000-0389-10	CONN 34 PIN ST HDR	1	EA	P4
123	6100-0146-10	SKT 18 PIN TERM CARRIER	1	EA	2D
125	3000-2700-10	RES,270,5%,1/4W,C	1	EA	R7
126	3000-3301-10	RES,3.3K,5%,1/4W,C	1	EA	R50
127	0114-0432-10	LABEL, CAUTION "NICD ONLY"	1	EA	
128	7011-1440-10	SCR,X,PH,4-40 X 5/16,STZN	2	EA	

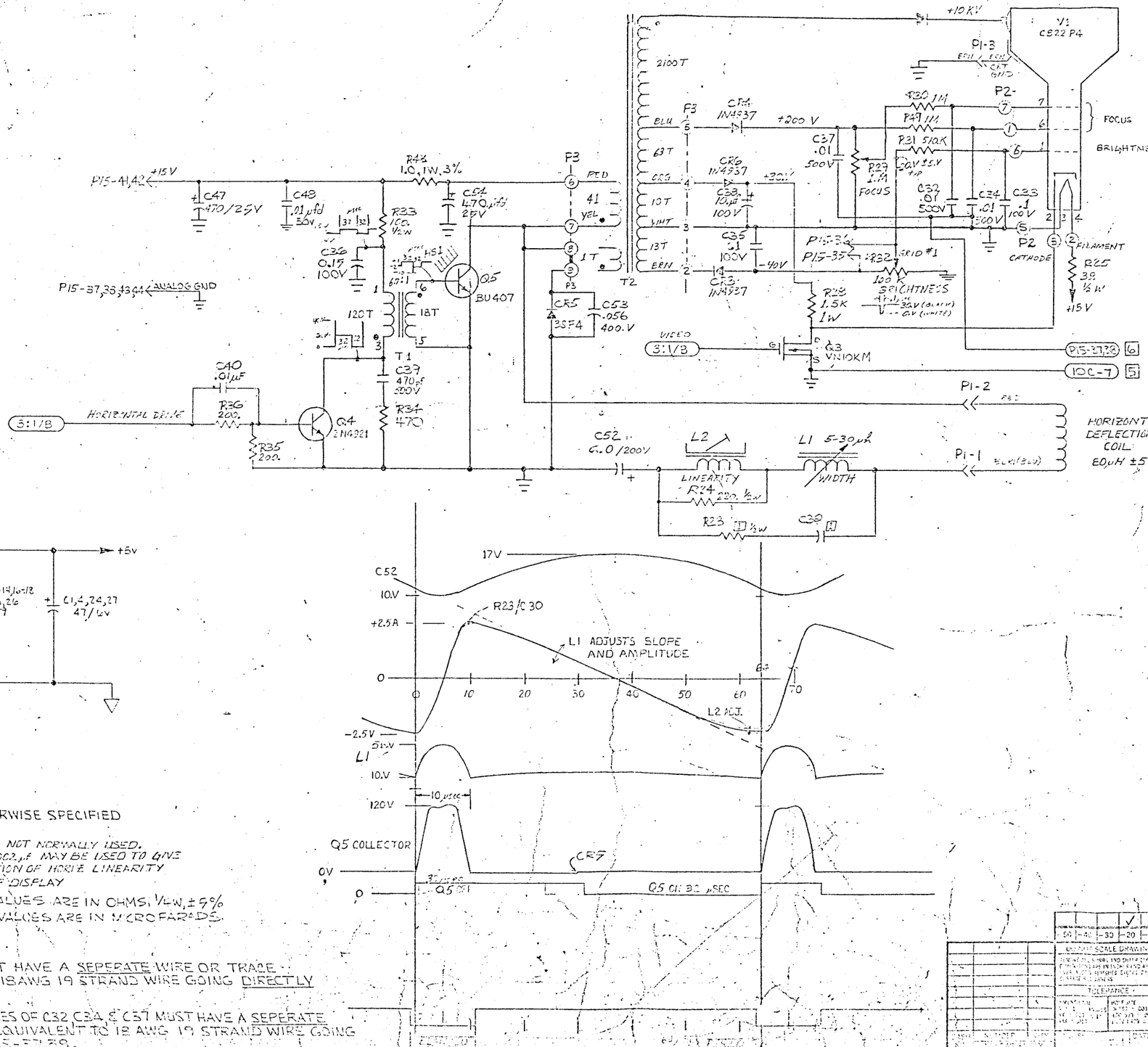
BILL OF MATERIAL
AS OF 02/12/86

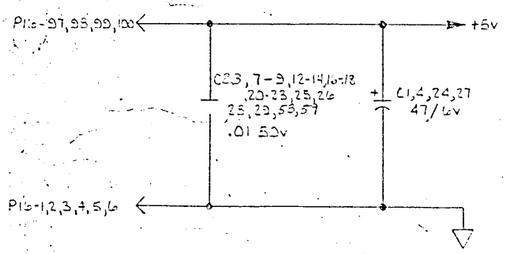
0114-2010-60 ASSY,PCB,DATA DISPLAY,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
129	0117-0149-10	ASSY,PROM,VERT,K105	1	EA	8B
130	0117-0150-10	ASSY,PROM,HORIZ,K105	1	EA	10B
132	0117-0139-10	SHIELD, DEFLECTION,K105	1	EA	
133	7085-1004-00	WSHR,INT TOOTH LOCK,#4,STZN	2	EA	
134	7080-1004-00	WSHR,FLAT,#4,SP,STZN	2	EA	
136	7150-0018-09	WIRE,PVC,18 AWG,WHT	1	FT	SEE NOTE 5

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PRODUCTION RELEASE			
	B		PRODUCTION RELEASE			
	C	3484	REVD PER ECO			
	D	3535	REVISED PER ECO			
	E	3900	REVISED PER ECO			
	F	4147	REVISED PER ECO			
	G	4426	REVISED PER ECO			
	H	4526	REVISED PER ECO H-D			
	J	4629	PER ECO			
	K	4730	REVISED PER ECO 11/20/84			
	K RC	4871	RECORD CHANGE ONLY 4/6/85			
	L	5103	REVISED PER ECO 11-2-85			
	M	5121	" " " 11-2-85			
	N	5139A	REVD PER ECO 2/25/86			





NOTES: UNLESS OTHERWISE SPECIFIED

1. SELECTED AT TEST. NOT NORMALLY USED. R23 = 100Ω, C30 = .002µF MAY BE USED TO GIVE A SMALL CORRECTION OF HORIZ LINEARITY AT LEFT SIDE OF DISPLAY
2. ALL RESISTOR VALUES ARE IN OHMS, ¼W, ±5%
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. -10 ONLY
5. Q3 SOURCE MUST HAVE A SEPERATE WIRE OR TRACE EQUIVALENT TO 18AWG 19 STRAND WIRE GOING DIRECTLY TO 10C-7.
6. THE GROUNDED SIDES OF C32 C34 & C37 MUST HAVE A SEPERATE WIRE OF TRACE EQUIVALENT TO 18 AWG 19 STRAND WIRE GOING DIRECTLY TO P15-37,38.

PART NUMBER	PART NAME	DESCRIPTION, SPECIFICATION	ITEM
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES ON FRACTIONS ± 1/64, ANGLES ± 1°, TOLERANCE ON TWO PLACE DECIMALS ± .01, THREE PLACE DECIMALS ± .005	DRAWN CWT 2-25-86	GOULD biomation	
	CHECKED	TITLE SCHEMATIC DATA DISPLAY PWB	
	ENGR APPR	SCALE	SIZE D
	MFG APPR	PART NUMBER 0114-2011	REV N
	DO NOT SCALE DRAWING		SHT 1 OF 6

ZONE	REV	ECO#	DESCRIPTION	DWN	CHK'D	DATE
			SEE SHT 1			

11B TDA 1270

+15V

C43 68 pf/500V

C44 0.1/100V

R41 220K

POWER-AMP

PRE-AMP

VREF +2.3V

C51 1000 /16V

R40 8.2K

C42 0.1 100V

C50 220/35V (K105) (K102) (K101) 10/16V (K500)

R38 3.3

R39 8.2K

R46 5.6K

R43 47K

R45 1.0 1/2 W

P1-5 WHT (BRN)

P1-4 YEL

VERTICAL DEFLECTION 10. mh I 5% 6.Ω ± 10%

± 250. mA

±.25V

6V

1V

2.3V

OSCILLATOR

RAMP GEN

BUFFER

D2*

Z1*

Q1* Q2* Q3* Q4* Q5* Q6* Q7* Q8* Q9* Q10* Q11* Q12* Q13* Q14* Q15* Q16* Q17* Q18*

R1* R2* R3* R4* R5* R6* R7* R8*

CR1*

11B-3 VERT SYNC

C41 .01μF

TAB 6

4.5V

R22 120

R21 10K VERT HOLD

C49 .15 100V

VERT HEIGHT R20 100K

R37 220K

R42 (K500) (K101) (K102) K1K-2.2K

C45 0.1 100V

C46 0.1 100V

R47 50.K VERT LINEARITY

R44 47.K

11B-4

.4 msec

1 msec

15 KHZ CROSSTALK FROM HORIZ

10.V

6. V

+.25V

0

-.25V

$\frac{\Delta I}{\Delta t} = \frac{.5A}{15\,msec} = .033\,A/msec$

$V = L\frac{dI}{dt} = .35V$

C51

5.4 V

.15V

5.7V

EFFECT OF R42

EFFECT OF R47 + R44

adj. R47 (CHANGES CURVATURE)

adj. R20 (CHANGES AMPLITUDE)

FINAL SLOPE = $\frac{12\mu A}{1f} + \frac{26\mu A}{1f} = .38\,V/msec$

11B-1

2.3V

1.V

INITIAL SLOPE = $.2V/msec = \frac{20\mu A}{1\mu F}$

VERT SYNC INPUT +2.V +.2V

183 μsec

16.7 msec

RAMP OUT 1 — RAMP GEN 12
Vcc 2 — COMPENSATION 11
OPEN 3 — AMP. INPUT 10
GROUND — GROUND
AMP OUT PUT 4 — OSCILLATOR 9
AMP Vcc 5 — SYNC. INPUT 8
REG VOLTAGE 6 — HEIGHT ADJ 7

TDA 1270
TOP VIEW

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	VEN

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ACTIVE FINISHES UNLESS OTHERWISE SPECIFIED
TOLERANCE
DIMENSIONAL X = ± .1 FRACTIONS ± 1/64 ANGULAR ± 2°
HOLE SIZE .093 = .062 .125 = .094 .250 = .125 .500 = .005

ITEM NO.	NUMBER REQ'D	NEXT ASSY	QTY

DRAWN	DATE
CHECKED	
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR.	

DWG. CONTR. | DATE

BOULD biomation

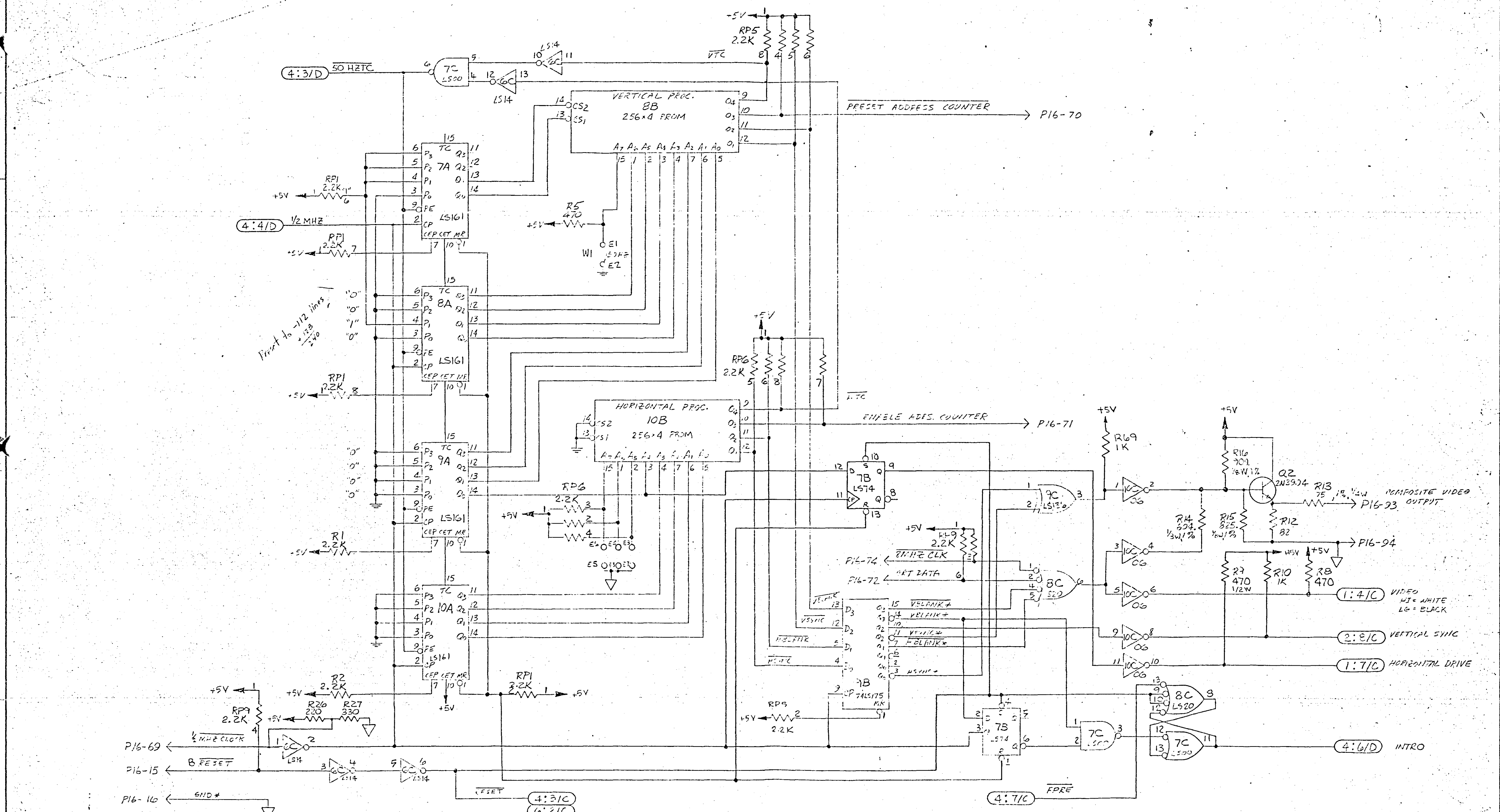
TITLE SCHEMATIC DATA DISPLAY PWB

SCALE	SIZE	PART NUMBER	REV
	D	0114-2011	M

SHEET 2 OF 6

DWG. NO. 0114-2011 SH 3 REV N

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			✓	✓				1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = .1 XX = .020 XXX = .010 ANGLES = 1° HOLE SIZE: 0-.599 = .003 .600-.999 = .004 1.000-1.499 = .005

DASH NO. | NUMBER NEXT ASSEMBLY | QTY

ENG. SERV. | DATE

DRAWN Cook DATE 5-5-80

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD .biomation

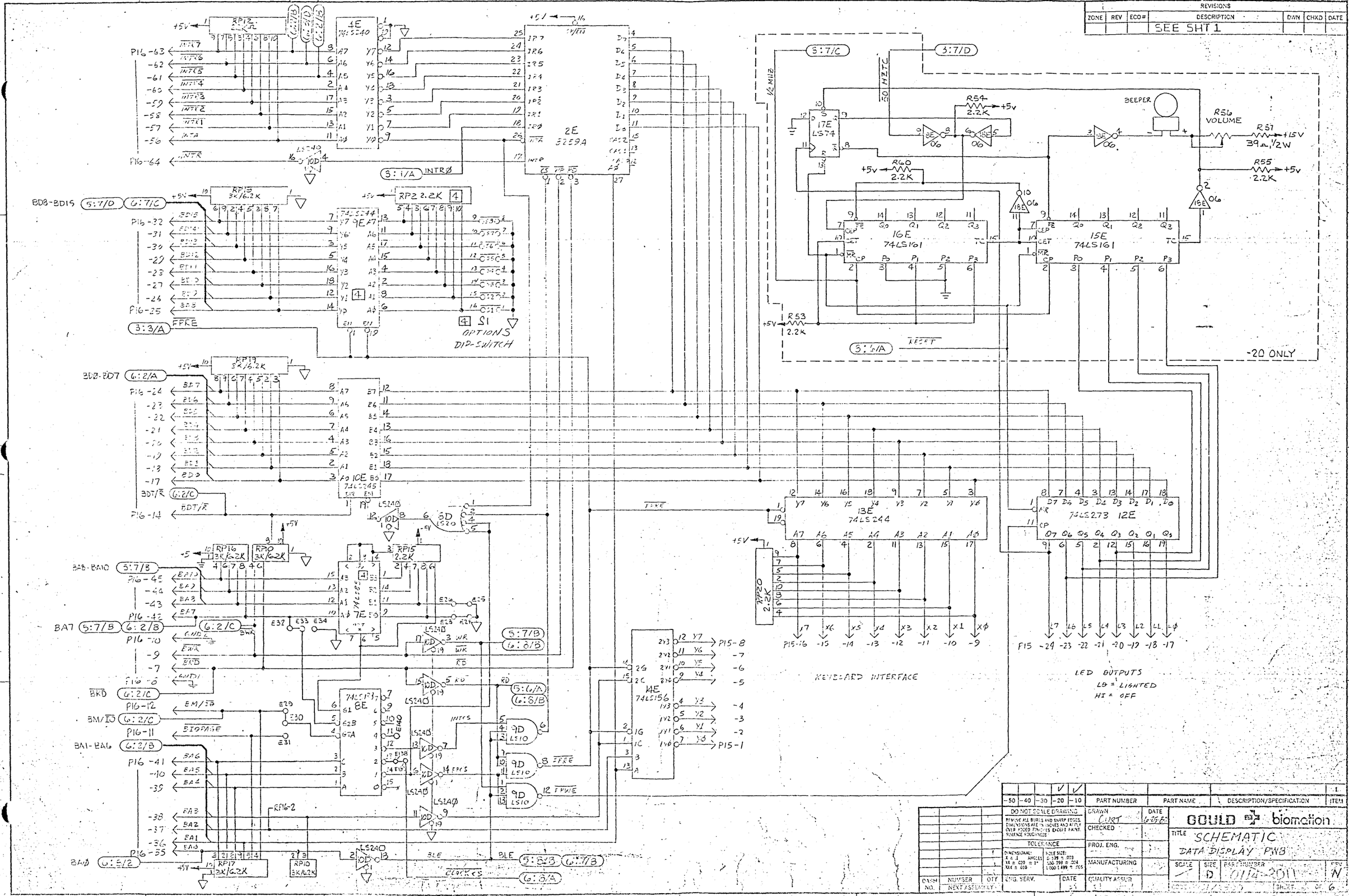
TITLE SCHEMATIC - DATA DISPLAY PWB

SCALE NONE SIZE D PART NUMBER 0114-2011 REV N

CODE

SHEET 3 OF 6

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			V	V				1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER PLATED FINISH. EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, XX ± .020 = 1°, XXX ± .010

HOLE SIZE: 0-.199 ± .003; .200-.999 ± .004; 1.000-1.499 ± .005

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

ENG. SERV.	DATE	
QUALITY ASSUR		

DRAWN	CURT 6-05-85
CHECKED	
PROJ. ENG.	
MANUFACTURING	

GOULD biomation

TITLE SCHEMATIC DATA DISPLAY PWB

SCALE	SIZE	PART NUMBER	REV
-	D	0114-2011	N

NEXT ASSY | SHEET 4 OF 6

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHK'D	DATE
			SEE SHT 1			

THIS SHEET -20 ONLY

6116 1B (TC5516A)

6116 3B (TC5516A)

CMOS RAM ADRS

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING — REMOVE ALL BURRS AND SHARP EDGES 0.010 MAX R. UNLESS OTHERWISE SPECIFIED — DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING AND FINISH EXCEPT PAINT. SURFACE FINISH

TOLERANCE — DIMENSIONAL: X ± 1, .XX ± 0.03, .XXX ± 0.01 — ANGULAR: ± 1° — FILLET SIZE: .125 = .093, .093 .999 = .062, 1.000 1.499 = .093

DRAWN — DATE — CHECKED — PROJ. ENG. — MANUFACTURING — ENG. SERV. — DATE — QUALITY ASSUR

GOULD biomation

TITLE: SCHEMATIC DATA DISPLAY, PW8

SCALE — SIZE D — PART NUMBER 0114-2011 — REV N

CODE — SHEET 5 OF 12

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			

22.K RP11 1 — 5:3/B VBATT

5 6 8 9

74LS244 (3D) — Y3 Y2 Y1 Y0 — A3 A2 A1 A0 — 17 15 13 11 — EN 19 — CLOCK DE

74LS244 (1D) — A7 A6 A5 A4 — Y7 Y6 Y5 Y4 — 18 16 14 12

R18 10K — R52 10K — R17 10K

7D 38 — 10 8 — INTR 6 → 4:7/D

7D 38 — 1 2 3

7D 38 — 12 13 11

7D 38 — 5 4 6

BD8-BD15 (4:8/D)

BD15 BD14 BD13 BD12 BD11 BD10 BD9 BD8

74LS373 MR CP — D7 D6 D5 D4 D3 D2 D1 D0 — Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 — 18 17 16 15 14 13 12 11 — 1 9

5:5/A PWR (DELAYED)

CUT AND JUMPER TO GROUND FOR -20 OPTION ONLY

2D MCM5832

BD0-BD7 (6:2/A)

BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0

74LS273 MR — D7 D6 D5 D4 D3 D2 D1 D0 — Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 — 18 17 16 15 14 13 12 11 — 1 11

4D

4:5/A BLE — 5D LS10 — CLOCK WEL

4:5/A WR

5:6/B BHE — 5D LS10 — BLOCK WEH

4:5/A RD — 5D LS10 — CLOCK RE

4:5/A CLOCK RE — LS240 — F1

HOLD — 30 ADJ — WRITE — TEST — XTAL — VBB — GND — Vcc

CK 7-40PF

Y1 32.768 KHZ

C11 10pf

0.1 μfd C17

5:3/B V BATT

P4-1 RESET ← 5:6/A

2 3

4 BRD ← 4:7/B

5

6 BWR ← 4:7/E

7

8 BDEN ← 5:1/E

9

P4-10 BDT/R ← 4:8/B 5:5/C

11

12 BM/IO ← 4:7/A

13

14 INTR5 ← 4:7/D

15

16 INTR7 ← 4:7/D

17

18 BA7 ← 4:7/B

19 BA6

P4-20 BA5

21 BA4

22 BA3

23 BA2

24 BA1

25 BA0 ← 4:7/B

26 BD7

27 BD6

28 BD5

29 BD4

30 BD3

31 BD2

32 BD1

33 BD0

P4-34

4:8/A 5:8/B BA1-BA6

4:7/C 5:7/C 6:7/C BD0-BD7

THIS SHEET -20 AND -40 ONLY

ITEM	DESCRIPTION/SPECIFICATION	PART NAME	PART NUMBER

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, ANGLES ± 1°, .XX ± .030, .XXX ± .010

MAX SIZE: 0 TO 6 = .003, AND 999 TO 1000 = .005

DRAWN — DATE

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR.

ENG SERV

DATE

NEXT ASSEMBLY — NUMBER — QTY

GOULD biomation

TITLE: SCHEMATIC - DATA BUFFER PWB

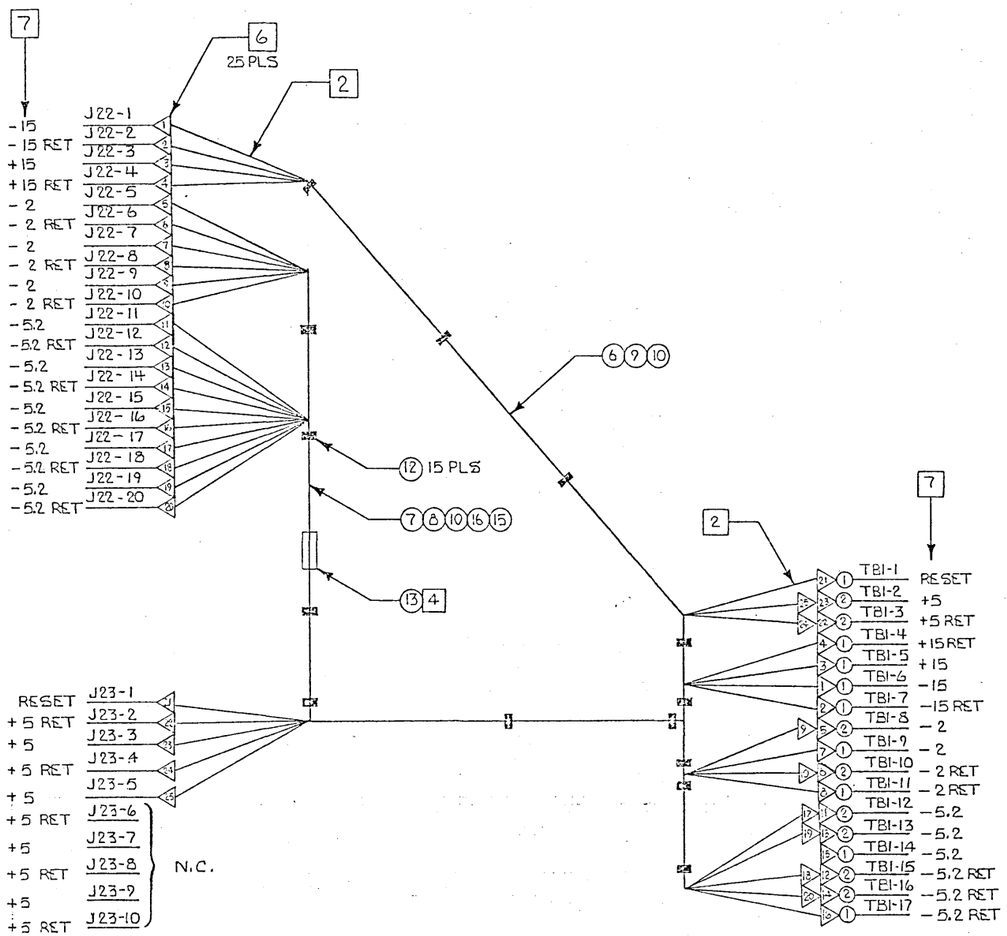
SCALE — SIZE D — PART NUMBER 0114-2011 — DEV N

CODE — SHEET 6 OF 6

DWG. NO.	SH.	REV.
0114-2024	1	D

REVISIONS

ZONE	REV.	ECO#	DESCRIPTION	DWN	CHKD	APPD
	C	4549	PER ECO	GG		
	D	4723	REDRAWN 9-10-84	JWC	DGW 10-5-84	JS 10-15-84



WIRE NO	FROM	TO	AWG	LNG ±.25	COLOR
1	J22-1	TB1-6	16	13.5	VIO
2	J22-2	TB1-7	16		BLK
3	J22-3	TB1-5	16		ORN
4	J22-4	TB1-4	16	13.5	BLK
5	J22-5	TB1-8	16	16.5	GRY
6	J22-4	TB1-10	16		BLK
7	J22-7	TB1-9	16		GRY
8	J22-8	TB1-11	16		BLK
9	J22-9	TB1-8	16		GRY
10	J22-10	TB1-10	16		BLK
11	J22-11	TB1-12	16		VIO
12	J22-12	TB1-15	16		BLK
13	J22-13	TB1-13	16		VIO
14	J22-14	TB1-16	16		BLK
15	J22-15	TB1-14	16		VIO
16	J22-16	TB1-17	16		BLK
17	J22-17	TB1-12	16		VIO
18	J22-18	TB1-15	16		BLK
19	J22-19	TB1-13	16		VIO
20	J22-20	TB1-16	16	16.5	BLK
21	J23-1	TB1-1	16	12.5	YEL
22	J23-2	TB1-3	16		BLK
23	J23-3	TB1-2	16		GRY
24	J23-4	TB1-3	16		BLK
25	J23-5	TB1-2	16	12.5	GRY

7

-15
-15 RET
+15
+15 RET
-2
-2 RET
-2
-2 RET
-2
-2 RET
-5.2
-5.2 RET
-5.2
-5.2 RET
-5.2
-5.2 RET
-5.2
-5.2 RET
RESET
+5 RET
+5
+5 RET
+5

NOTES: UNLESS OTHERWISE SPECIFIED

1. DRAWING IS TO SCALE AND MAY BE USED AS A TEMPLATE.
2. IDENTIFY LUGS AND ENDS OF WIRES WITH DESTINATION AS SHOWN.
3. TIP OF TERMINATION TRIANGLE DENOTES END OF CUT WIRE BEFORE LUGGING.
4. TAG HARNESS WITH ASSY NO., DASH NO. AND REV. LEVEL.
5. ▽ TERMINATION TRIANGLE INDICATES WIRE NO.
   ◯ CIRCLE INDICATES ITEM NO. ON PARTS LIST.
6. ENDS OF WIRES STRIPPED AND TINNED 1/4"
7. SIGNAL NAMES SHOW FOR REF. ONLY.
8. N.C. MEANS "NO CONNECTION".

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

DASH NO.	NEXT ASSY	USED ON
10	0950-0220	K500
10	0120-0080	K205
10	0114-0210	K101
FIRST APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

GOULD PART NO.

APPROVALS	DATE
DRAWN J.W. CARROLL	9-10-84
CHECKED DGW	6-4-84
PROJ ENG J.S.	6-15-84

GOULD Electronics

TITLE: CABLE ASSEMBLY POWER SUPPLY

SIZE	DWG. NO.	REV.
D	0114-2024	D.

SCALE 1/1 | MODEL | SHEET 1 OF 1

ELECTRONIC POST PROCESSOR NO

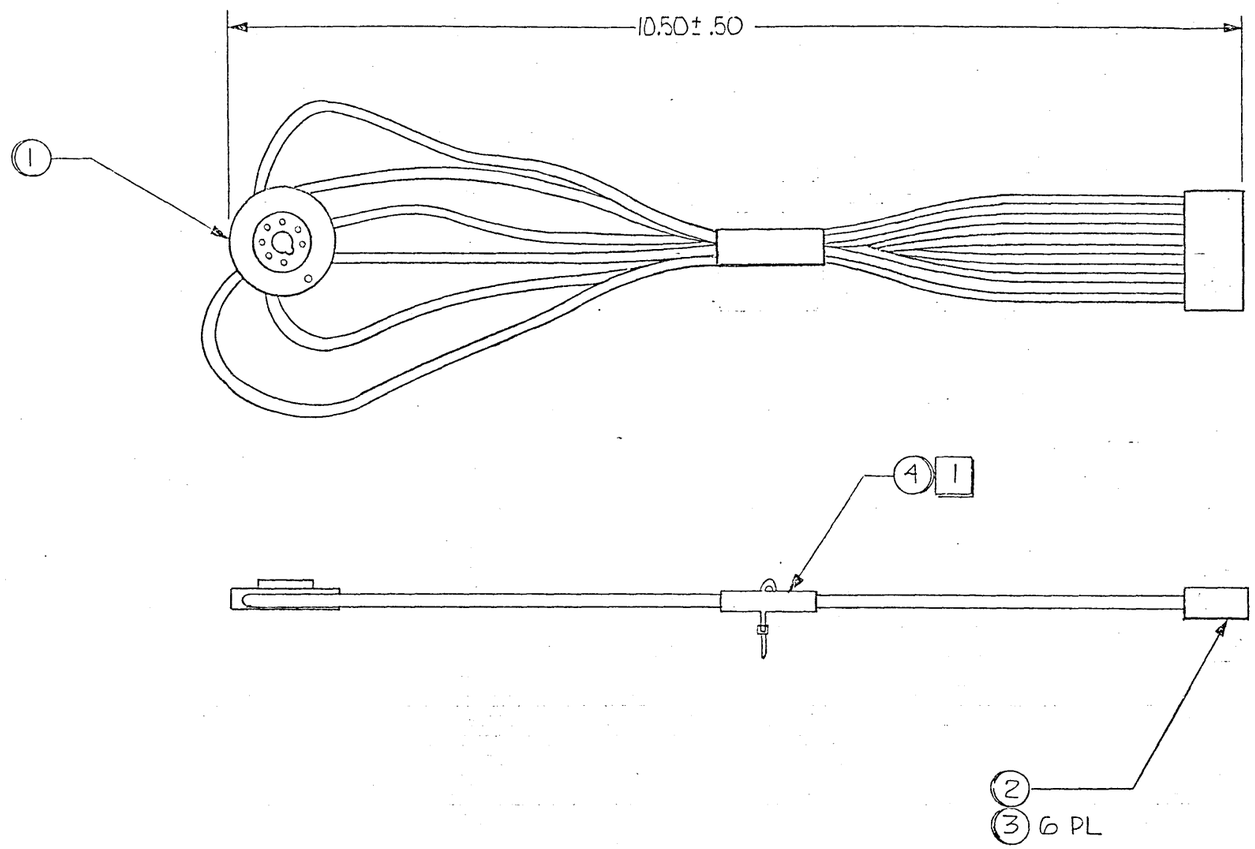
BILL OF MATERIAL

AS OF 02/12/86

0114-2024-10 ASSY,CABLE,PWR SPLY
MODEL: K101

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0114-2024	DWG,ASSY,PWR SUPPLY CBL	0	EA	REF
1	6200-0069-10	TERM LUG SNAP SPADE 22G INSLT	9	EA	
2	6200-0055-10	TERM LUG SPADE 10-12 #6	8	EA	
5	7150-0016-08	WIRE,PVC,16 AWG,GRY	7	FT	
6	7150-0016-03	WIRE,PVC,16 AWG,ORN	1	FT	
9	7150-0016-07	WIRE,PVC,16 AWG,VIO	8	FT	
10	7150-0016-10	WIRE,PVC,16 AWG,BLK	16	FT	
12	7200-0008-10	TIE,CBL,4"	15	EA	
13	7200-0039-10	TIE,MARKER,4"	1	EA	
15	7150-0016-04	WIRE,PVC,16 AWG,YEL	1	FT	

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 309	SM	GW	7/2/83
	A	3957	PROD REL PER ECO #	SM	GW	9/16/83



WIRING CODE	
PIN	COLOR
1	ORG
2	BRN
3	VIO
4	N/C
5	BLK
6	GRN
7	BLU
8	N/C

1 MARK PART WITH PART NO. 0117-0021 DASH NO. & REV LEVEL USING 1/8" CHARACTERS.

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
10	0117-0183	1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± .1 ANGLES, XX ± .020 ± 1°, XXX ± .010
HOLE SIZE: .0-.599 ± .003, .600-.999 ± .004, 1.000-1.499 ± .005

		DATE
DRAWN	SM	12-1-82
CHECKED		
PROJ. ENG.		2/3/83
MANUFACTURING		2-3-83
QUALITY ASSUR		2-3-83
ENG. SERV.	R. Hinman	2/3/83

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

GOULD biomation

TITLE CRT CABLE ASSEMBLY

SCALE	SIZE	PART NUMBER	REV
NONE	C	0117-0021	A

CODE K105 SHEET 1 OF 1

DWG. NO. 0117-0021 SH 1 REV A

0117-0021

SINGLER LEVEL H

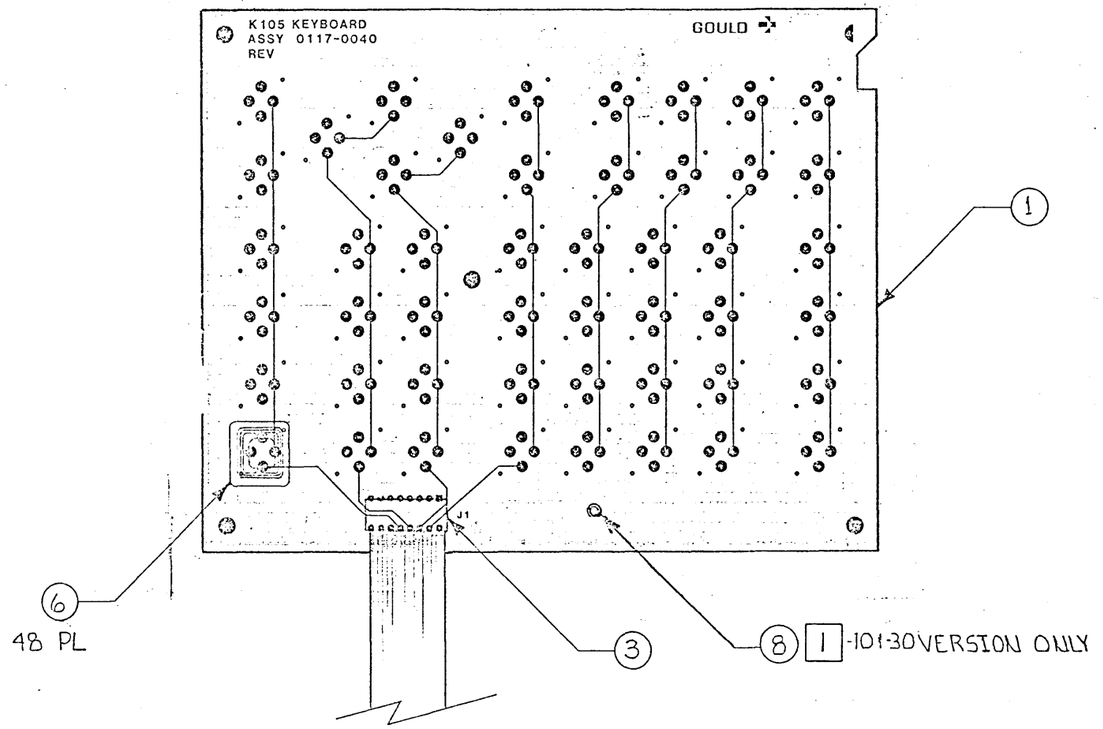
BILL OF MATERIAL

AS OF 02/12/86

0117-0021-10 ASSY,CABLE,CRT,K105
MODEL: K105

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	C0117-0021	DWG,ASSY,CRT CABLE	0	EA	REF
1	6100-0130-10	SKT CRT	1	EA	
2	6000-0358-08	CONN 8 POS PIN HOUSING	1	EA	
3	6000-0357-10	CONN PIN 24-18AG	6	EA	
4	7200-0039-10	TIE,MARKER,4"	1	EA	

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 316	SJM		7-3-80
	51	3695	REV'D PER ECO #	MW	DGW	4/6/83
	52	3739	REV'D PER. ECO #	MW	DGW	5/2/83
	A	3957	PROD REL PER ECO	JGS	DGW	7/6/83
	B	4220	PER ECO	K.R	DGW JMS	11/7/84
	C	4896	ROLL REV PER ECO 2-22-85	SAR	DGW ERM	3/4/85
	D	5109	REVISE PER ECO # 11-2-85	DGW	ERM	11/7/85



FLAT SIDE (CATHODE) OF ITEM 8 GOES TO SQUARE PAD ON CIRCUIT BOARD, -101-30 VERSION ONLY.

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
-30	0117-0003	1
-20	0120-0009	1
-10	0117-0006	1

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, .XX ± .020, .XXX ± .010; ANGLES ± 1°; HOLE SIZE: .0-.599 ± .003, .600-.999 ± .004, 1.000-1.499 ± .005

DRAWN	J.W.CARROLL	6-4-82
CHECKED	R. Wood	2/13/83
ENG. SERV.	R. Swan	2/18/83
PROJ. ENG.		2-18-83
MANUFACTURING		2-18-83
QUALITY ASSUR		

GOULD biomation

TITLE ASSY — KEYBOARD

SCALE	SIZE	PART NUMBER	REV
1:1	C	0117-0040	D

CODE K105 SHEET 1 OF 2

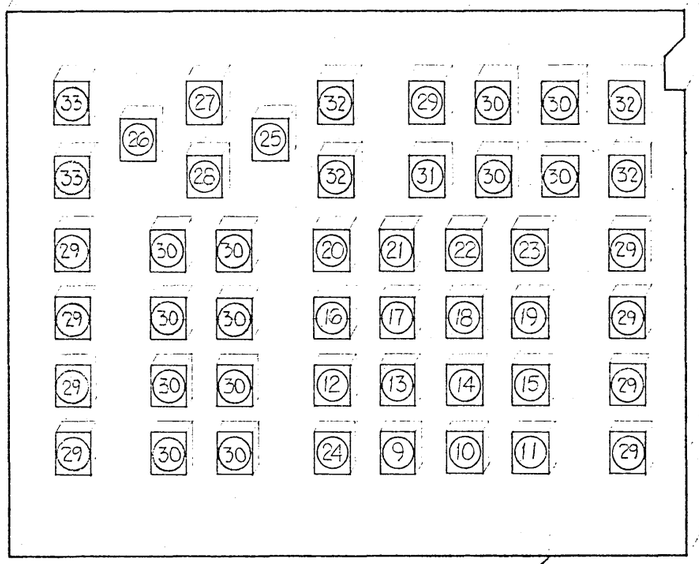
DWG. NO. 0117-0040 SH 1 REV D

0117-0040 182

KLINGLER K-VEL H

REVISIONS						
ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	-		SEE SH. 1			

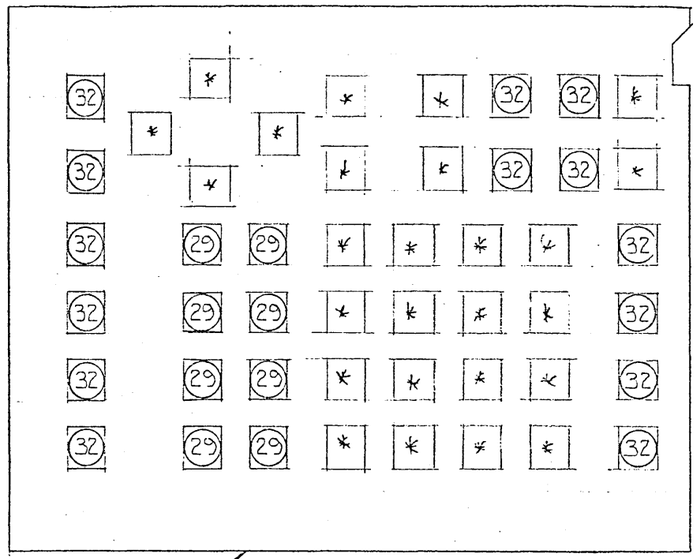
-10 & -20



(1) REF.

-30

*(ALL REF. DESG. NOT SHOWN SAME AS -10 & -20)



(1) REF.

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: .0-.599 ± .003; .600-.999 ± .004; 1.000-1.499 ± .005

ENG. SERV. R. Dixon DATE 2/18/83

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DRAWN [illegible] DATE 12-7-82

CHECKED R. Wood 2-15-83

PROJ. ENG. [signature] 2-18-83

MANUFACTURING [signature] 2-18-83

QUALITY ASSUR

GOULD biomation

TITLE ASSEMBLY KEYBOARD

SCALE	SIZE	PART NUMBER	REV
	C	0117-0040	D

CODE K105 SHEET 2 OF 2

DWG. NO. 0117-0040 SH 2 REV D

0117-0040 282

KEUFFEL & ESSER CO. KEUFFEL & ESSER CO. KEUFFEL & ESSER CO. KEUFFEL & ESSER CO.

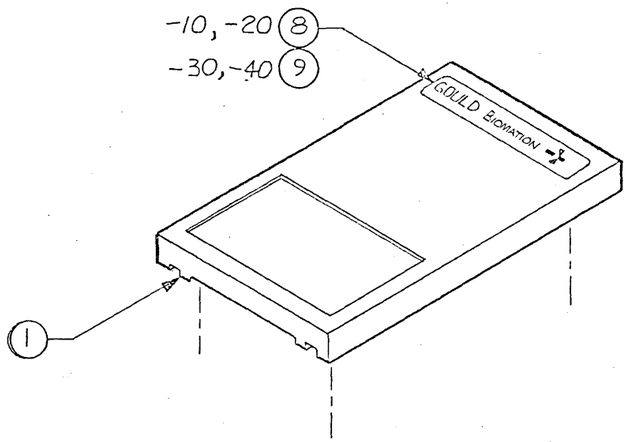
BILL OF MATERIAL

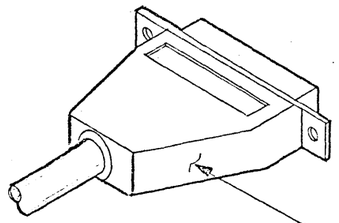
AS OF 02/12/86

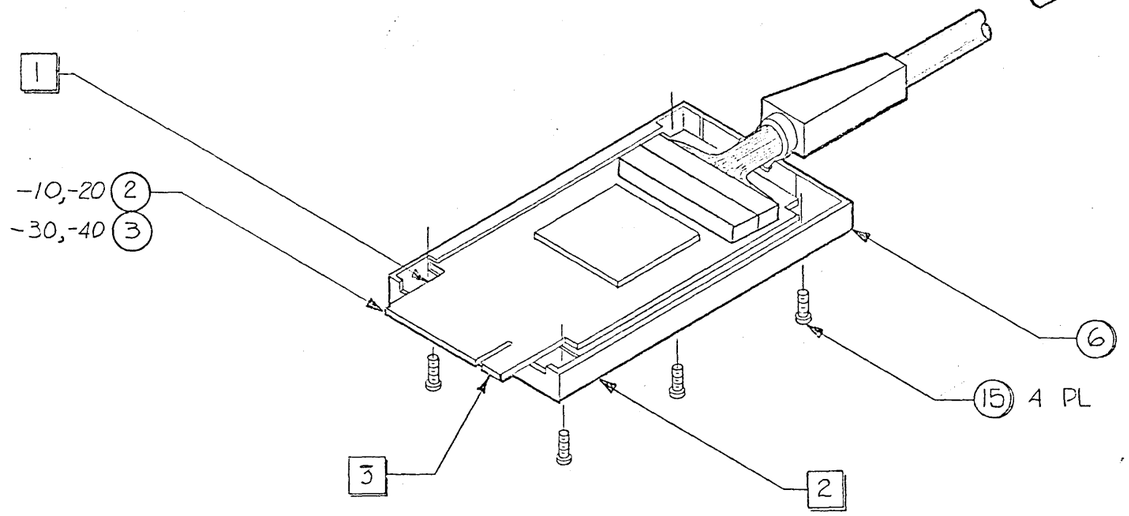
0117-0040-30 ASSY,KEYBOARD,K115
MODEL: K105

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	C0117-0040	DWG,ASSY,KEYBOARD	0	EA	REF
0	C0117-0041	DWG,SCHEM,KEYBOARD	0	EA	REF
1	0117-0042-10	FAB, KEYBOARD	1	EA	
3	0112-0204-10	ASSY,CBL,KB TO FP	1	EA	
6	6600-0118-10	SW KYBD. LO-PROFILE	48	EA	
8	6400-0039-10	LED 1 AMP RED	1	EA	CR1
9	0112-0079-01	KEYTOP,WHITE,'1',K100D	1	EA	"1"
10	0112-0079-02	KEYTOP,WHITE,'2',K100D	1	EA	"2"
11	0112-0079-03	KEYTOP,WHITE,'3',K100D	1	EA	"3"
12	0112-0079-04	KEYTOP,WHITE,'4',K100D	1	EA	"4"
13	0112-0079-05	KEYTOP,WHITE,'5',K100D	1	EA	"5"
14	0112-0079-06	KEYTOP,WHITE,'6',K100D	1	EA	"6"
15	0112-0079-07	KEYTOP,WHITE,'7',K100D	1	EA	"7"
16	0112-0079-08	KEYTOP,WHITE,'8',K100D	1	EA	"8"
17	0112-0079-09	KEYTOP,WHITE,'9',K100D	1	EA	"9"
18	0112-0079-10	KEYTOP,WHITE,'A',K100D	1	EA	"A"
19	0112-0079-11	KEYTOP,WHITE,'B',K100D	1	EA	"B"
20	0112-0079-12	KEYTOP,WHITE,'C',K100D	1	EA	"C"
21	0112-0079-13	KEYTOP,WHITE,'D',K100D	1	EA	"D"
22	0112-0079-14	KEYTOP,WHITE,'E',K100D	1	EA	"E"
23	0112-0079-15	KEYTOP,WHITE,'F',K100D	1	EA	"F"
24	0112-0079-16	KEYTOP,WHITE,'0',K100D	1	EA	"0"
25	0112-0059-23	KEYTOP,BLUE,K100D	1	EA	">"
26	0112-0059-24	KEYTOP,K100D	1	EA	"<"
27	0112-0059-25	KEYTOP,BLUE,K100D	1	EA	"^"
28	0112-0059-26	KEYTOP,BLUE,K100D	1	EA	"v"
29	0112-0049-10	KEYTOP, (BLUE PLAIN) BUTTON	9	EA	
31	0112-0049-50	KEYTOP, (RED) BUTTON	1	EA	
32	0112-0049-40	KEYTOP, (GREY) BUTTON	18	EA	

REVISIONS						
ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	01		PROTOTYPE	STM		1-8-83
	50		PILOT REL PER ERN 335	STM		4-18-83
	51	3960	REVISED PER ECO #	JWC	DGW	3-27-85
	52	3749	REV'D PER ECO 3749	RTM	DGW	2/14/14







USAGE CHART		
DASH	MODEL	LENGTH
10	K105	6'
20	K105	9'
30	K101	6'
40	K101	9'

[3] MARK BOTTOM OF CASE LARGE RECTANGULAR RECESS WITH THE FOLLOWING: XXX, XX, XX, XXXXX
MFG N° YEAR WEEK SERIAL N°
0117-0099-XX REV. X
DASH CURRENT REV. LEVEL

[2] BAG AND TAG WITH P/N 0117-0099, DASH NO. AND REV. LEVEL.

[1] PIN 1 (FARSIDE).

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.	NUMBER	QTY
40	0114-1092	1
40	0114-1091	1
30	0114-1062	1
30	0114-1061	1
20	0117-0174	1
10	0117-0173	1

NEXT ASSEMBLY

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°
HOLE SIZE: .0-.599 ± .003, .600-.999 ± .004, 1.000-1.499 ± .005

DRAWN	STM	DATE 1-8-83
CHECKED	R. Wood	4/19/83
PROJ. ENG.		5/13/83
MANUFACTURING		5-13-83
QUALITY ASSUR		5/13/83
ENG. SERV.	R. Simon	DATE 4/25/83

GOULD biomation

TITLE: PROBE SUB ASSY

SCALE	SIZE	PART NUMBER	REV
NONE	C	0117-0099	52

CODE K105/K101 SHEET 1 OF 1

DWG NO 6600-0110 SH 1 REV 52

0117-0099

55

SCRIBER LEVEL H

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	LAST
1						1	1	1	1	0114-0255-10	CASE, PROBE, TOP		
2						/	/	1	1	0117-0213-10	PROBE PWB ASSY, K105		
3						1	1	/	/	0117-0213-20	PROBE PWB ASSY, K101/K102		
4						/	1	/	1	0117-0022-10	POD TO UNIT CABLE 6'		
5						1	/	1	/	0117-0022-20	POD TO UNIT CABLE 9'		
6						1	1	1	1	0114-0255-20	CASE, PROBE, BOTTOM		
7													
8						/	/	1	1	0117-0171-10	LABEL, PROBE POD, K105		
9						1	1	/	/	0114-0264-10	LABEL, PROBE POD, K101/K102		
10													
11													
12													
13													
14													
15						4	4	4	4	7000-0429-20	SCREW 2 x 3/8 LG PH. HD.		

REV	DESCRIPTION	DATE	DWN	CKD
52	REV'D PER ECO 3749	1-30-84	RTM	DWN STM
51	REV'D PER ECO 3760	9-25-83	JWC	DGW
50	PILOT RELEASED PER ECN 335	4-15-83	STM	
01	PROTOTYPE	1-8-83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
40	0114-1092	1
40	0114-1091	1
30	0114-1062	1
30	0114-1061	1
20	0117-0174	1
10	0117-0173	1

		DATE
DWN	STM	1-8-83
CHK	R. Wood	4/29/83
ENGR		5/3/83
MFG		5/3/83
Q.A.		5/4/83

LIST OF MATERIAL

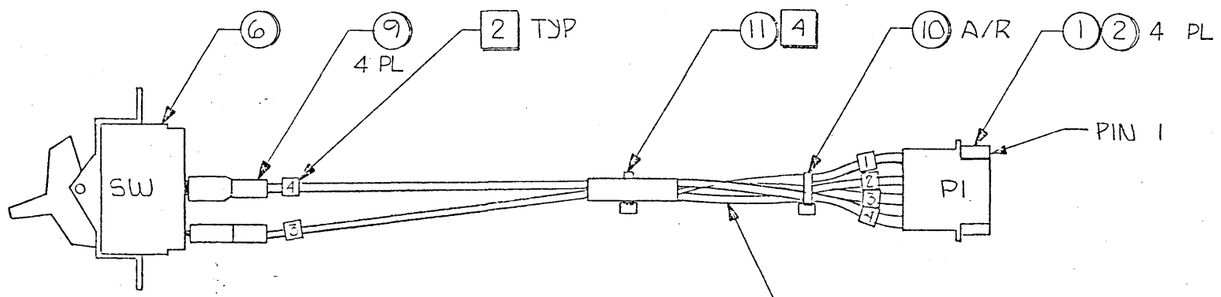
PROBE SUB ASSEMBLY

GOULD biomation

B 0117-0099 REV 52

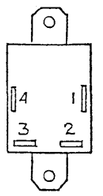
MODEL K105-K101 SHEET 1 OF 1

REVISIONS						
ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 316	STM		1-31-83
	A	3957	PROD REL PER ECO#	STM	DAW	9-16-83



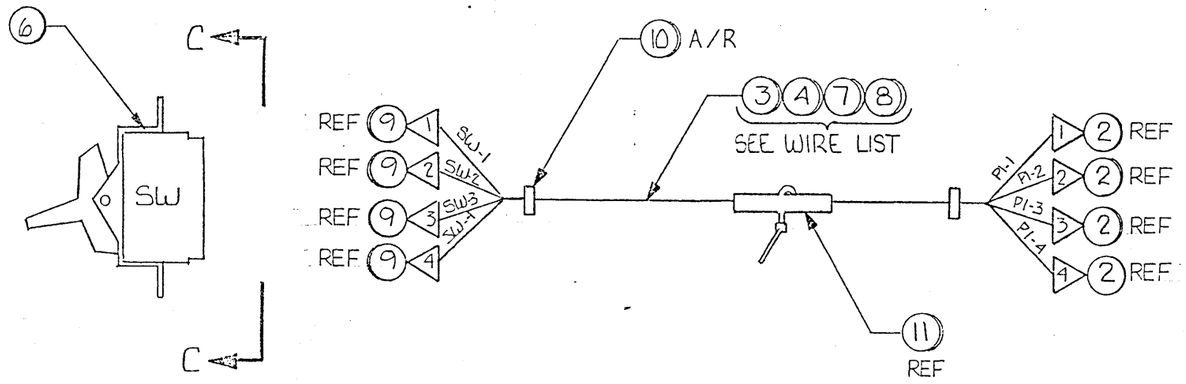
DETAIL A
COMPLETED CABLE

3 4 7 8
SEE WIRE LIST



VIEW C-C

WIRE LIST						
WIRE NO.	ITEM NO	FROM	TO	COLOR	AWG	LENGTH
1	8	P1-1	SW-1	WHT/VIO	18	7"
2	3	P1-2	SW-2	WHT/BRN	18	7"
3	4	P1-3	SW-3	BLU/BLK	18	7"
4	7	P1-4	SW-4	WHT/ORN	18	7"



DETAIL B
CABLE SCHEMATIC

5. ◁ TERMINATION TRIANGLE INDICATES WIRE NO.

4 TAG HARNESS WITH ASSY NO 0117-0117-10 AND REV LEVEL AS SHOWN

IDENTIFY END OF WIRES WITH DESTINATION AS SHOWN

1. DWG IS TO SCALE + MAY BE USED AS A TEMPLATE

NOTES: UNLESS OTHERWISE SPECIFIED

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

10	0117-0005	1
DASH NO.	NUMBER NEXT ASSEMBLY	QTY

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°
HOLE SIZE: .0-.599 ± .003, .600-.999 ± .004, 1.000-1.499 ± .005

DRAWN	STM	DATE 1-15-83
CHECKED	R. Wood	2-15-83
PROJ ENG.		2-18-83
MANUFACTURING		2-18-83
QUALITY ASSUR		
ENG. SERV.	R. Lyman	DATE 2/18/83

GOULD biomation

TITLE CABLE ASSEMBLY POWER SWITCH

SCALE	SIZE	PART NUMBER	REV
	C	0117-0117	A

CODE K105 SHEET 1 OF 1

DWG. NO. 0117-0117 SH 1 REV A

0117-0110

KLINGLER K-VEL H

BILL OF MATERIAL

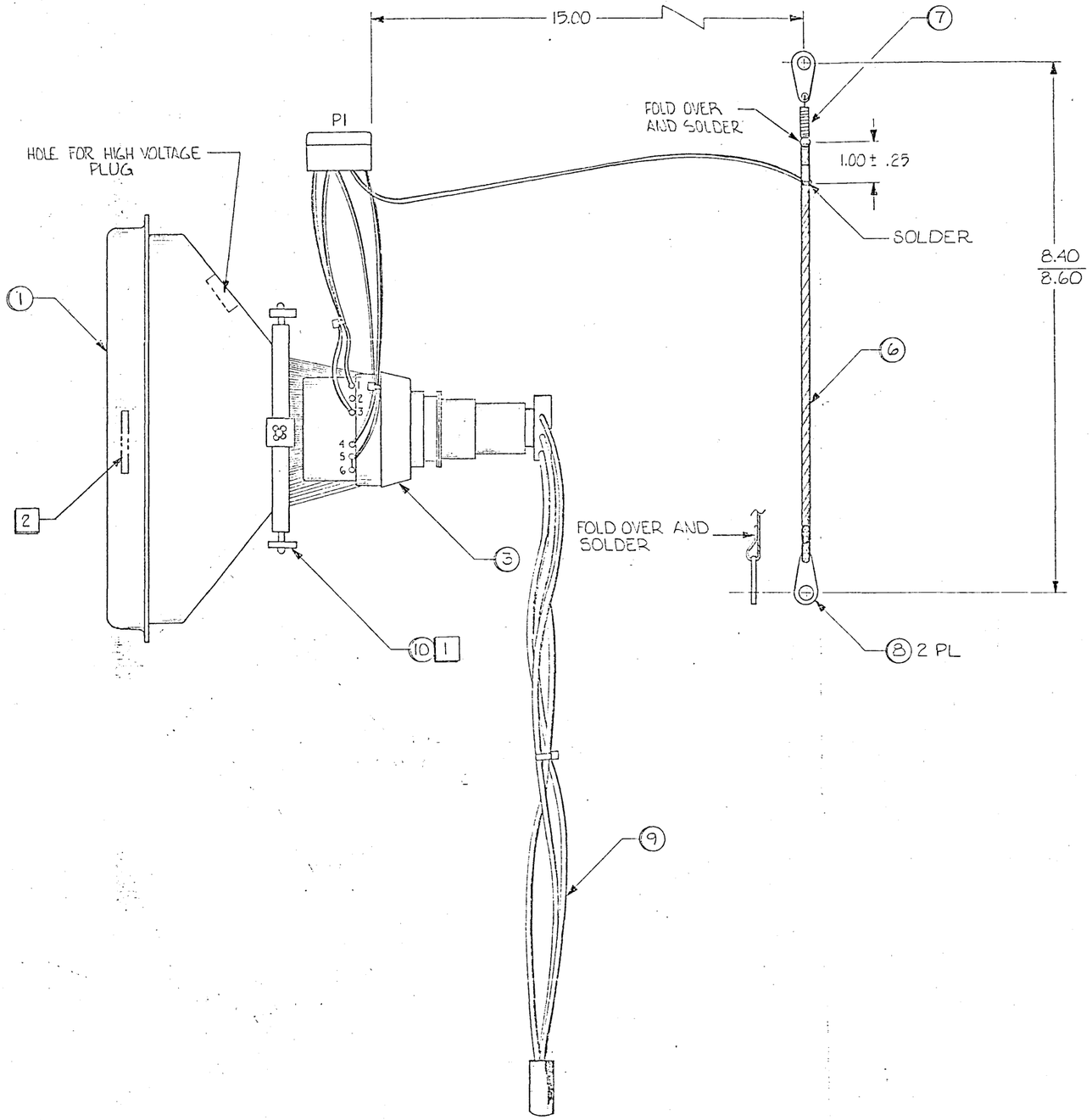
AS OF 02/12/86

0117-0117-10 ASSY,CABLE,POWER SWITCH,K105
MODEL: K105

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	C0117-0117	DWG,ASSY,POWER SWITCH CABLE	0	EA	REF
1	6000-0024-10	CONN 4 PIN HOUSING	1	EA	
2	6000-0157-10	CONN PIN 24-18 AWG	4	EA	
3	7150-0018-19	WIRE,PVC,18 AWG,WHT/BRN	1	FT	
4	7150-0018-37	WIRE,PVC,18 AWG,BLU/BLK	1	FT	
6	9000-0093-10	POWER SWITCH	1	EA	
7	7150-0018-20	WIRE,PVC,18 AWG,WHT/ORN	1	FT	
8	7150-0018-22	WIRE,PVC,18 AWG,WHT VIO	1	FT	
9	6200-0036-10	TERM FEMALE DISCONNECT	4	EA	
10	7200-0008-10	TIE,CBL,4"	2	EA	
11	7200-0039-10	TIE,MARKER,4"	1	EA	

DWG. NO. 0117-0123 SH 1 REV A

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DAN	CHKD	DATE
	50		PILOT REL PER ERN 309	SM	RW	7/1/82
	51	3773	REVISED PER ECO	RWJ	RWJ	8/24/82
	A	3957	PROD. REL PER ECO #	SM	RWJ	9/9/82



1. MAGNETS ITEM (10) TO BE INSTALLED AT TEST

2. IDENTIFY WITH ASSY NO. 0117-0123 DASH NO. & REV LEVEL WITH 1/8" BLK CHARACTERS

NOTES: UNLESS OTHERWISE SPECIFIED

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ROLLED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010
HOLE SIZE: 0 .599 ± .002; 600 .999 ± .004; 1.000 1.499 ± .005

DRAWN SM DATE 9-9-82
CHECKED
PROJ. ENG. [signature] 7/3/83
MANUFACTURING [signature] 9-23-83
ENG. SERV. R. Simpson DATE 9/3/83
QUALITY ASSUR. [signature] 9-23-83

GOULD Instruments Division Santa Clara Operations

TITLE C.R.T. ASSEMBLY

DASH NO.	NUMBER	QTY
10	0117-0005	1
	NEXT ASSEMBLY	

SCALE | SIZE D | PART NUMBER 0117-0123 | REV A

MODEL 405 | SHEET 1 OF 1

BILL OF MATERIAL

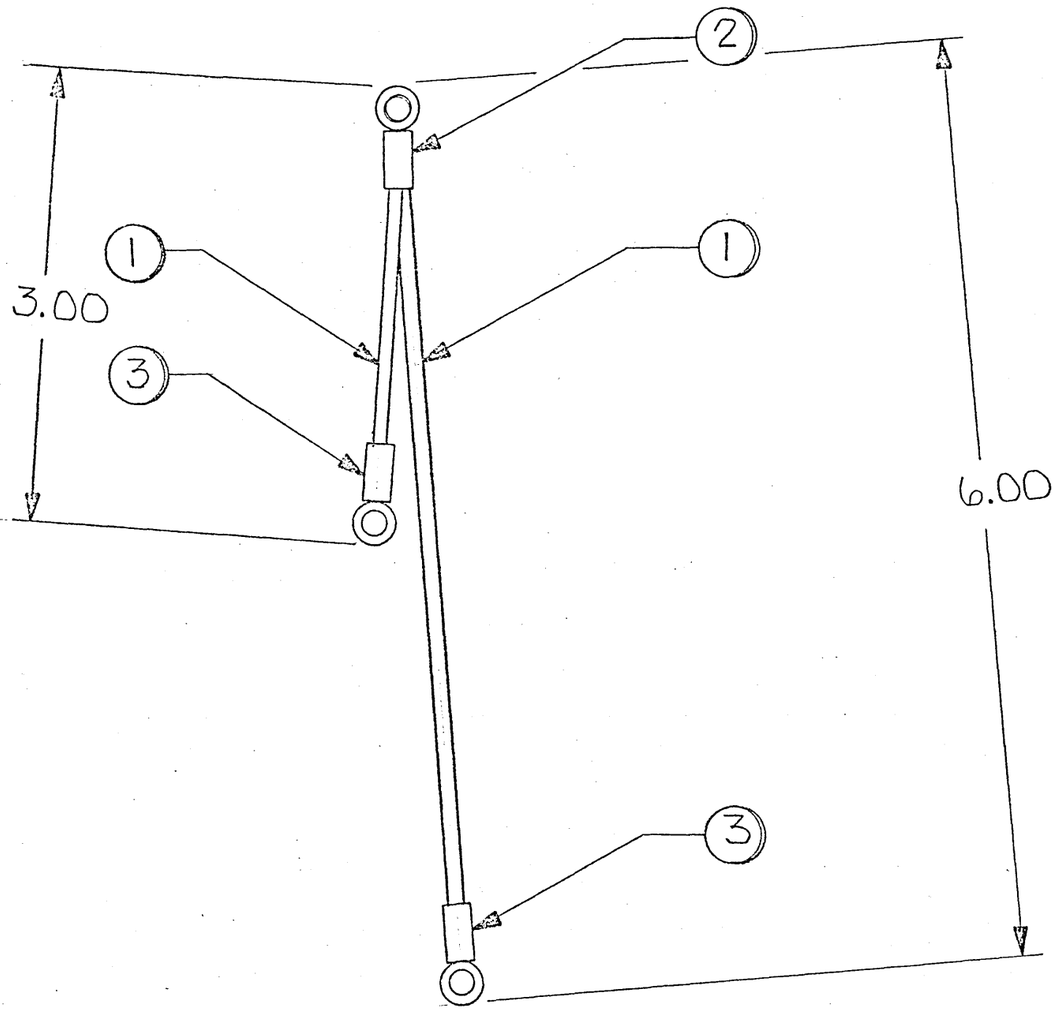
AS OF 02/12/86

0117-0123-10 ASSY,CRT,K105
MODEL: K105

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0117-0123	DWG,ASSY,CRT	0	EA	REF
1	9000-0029-30	CRT,SPEC.	1	EA	
3	9000-0047-30	SPEC. DEFLECTION COIL	1	EA	
6	7100-0067-10	CBL,TUBULAR BRAIDED,1/16"	1	FT	
7	7000-0375-10	HDWR EXT SPRING 1-1/4	1	EA	
8	7090-2006-00	LUG,LOCK,#6	2	EA	
9	0117-0021-10	ASSY,CABLE,CRT,K105	1	EA	
10	2000-0006-10	IND 3122-104-95000 MAG	5	EA	

DWG. NO. 0117-0133 | SH 1 | REV. A

REVISIONS					
REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
01		PROTOTYPE	STM		2-4-83
50		PILOT REL. PER ERN 322	[illegible]		2/3/83
51	3872	REVISED PER ECO Nº	SWC	DGW	7-7-83
A	3957	PROD. REL PER ECO #	STM	DGW	9-16-83



															1
					−50	−40	−30	−20	−10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION			ITEM
10	0117-0003	1													
DASH NO.	NUMBER	QTY													
	NEXT ASSEMBLY														

2. BAG & TAG WITH P/N 0117-0133 DASH NO AND REV LEVEL.
1. DRAWING IS TO SCALE & MAY BE USED AS TEMPLATE

NOTES: UNLESS OTHERWISE SPECIFIED

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES .XX ± .020 ± 1° .XXX ± .010

HOLE SIZE: .0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

ENG. SERV. R. Kiraan DATE 3/2/83

DRAWN STM	DATE 2-4-83	
CHECKED [illegible]	2/28/83	
PROJ. ENG. [illegible]	3/23/83	
MANUFACTURING [illegible]	3-25-83	
QUALITY ASSUR [illegible]	3-25-83	

GOULD biomation

TITLE
CHASSIS GND CABLE

SCALE	SIZE	PART NUMBER	REV
1:1	B	0117-0133	A

CODE K105 SHEET 1 OF 1

KLINGLER K-VEL H

BILL OF MATERIAL

AS OF 02/12/86

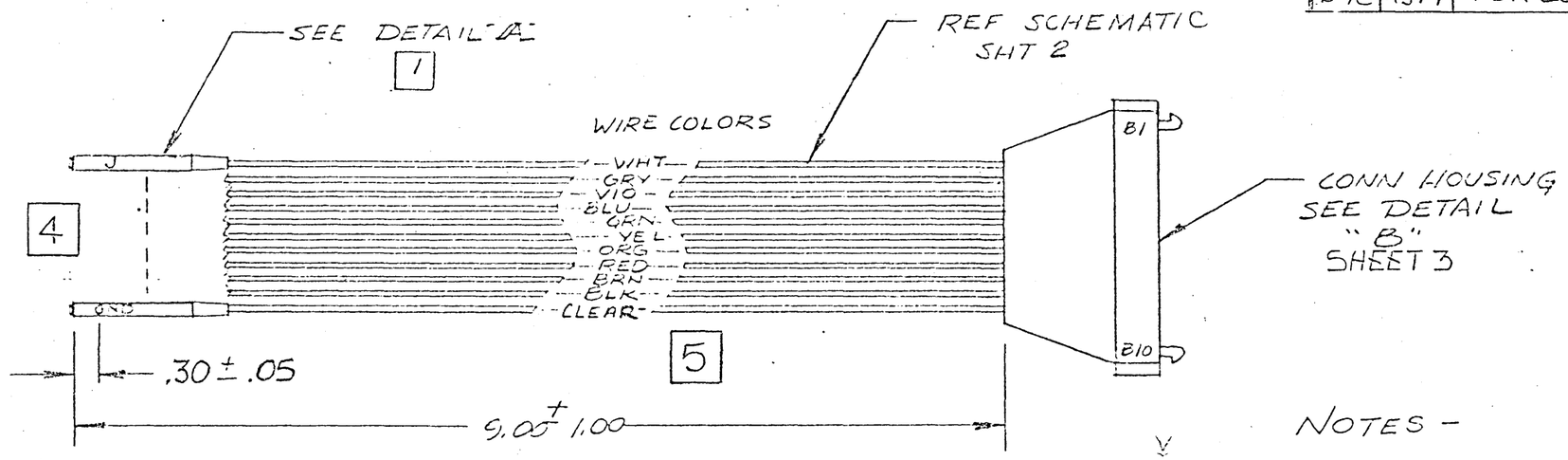
0117-0133-10 CABLE,CHASSIS GROUND,K105
MODEL: K105

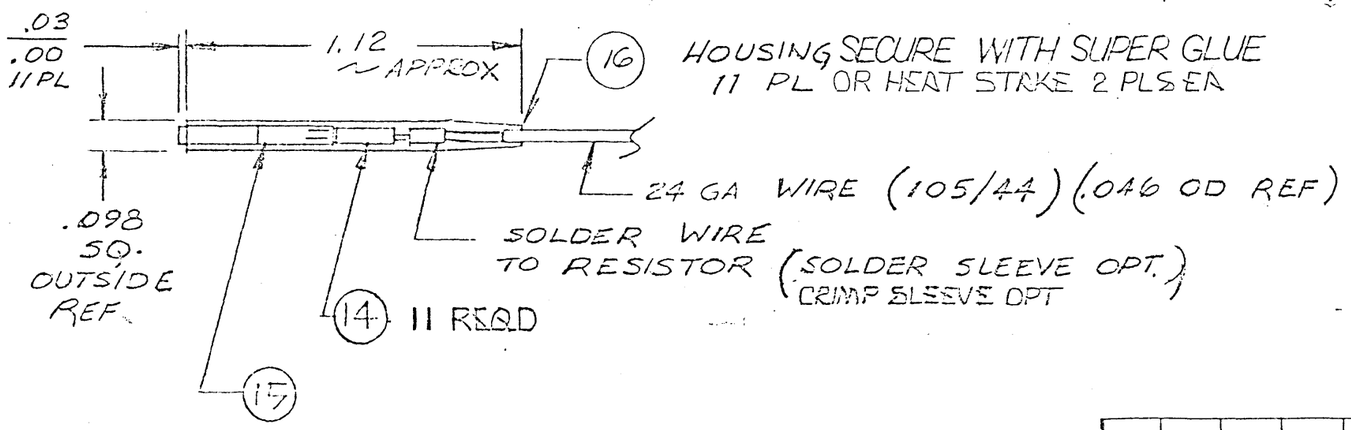
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0117-0133	DWG,ASSY,CHASSIS GND CABLE	0	EA	REF
1	7150-0020-10	WIRE,PVC,20 AWG,BLK	1	FT	
2	6200-0030-10	TERM RING TONGUE BLUE	1	EA	
3	6200-0025-10	TERM LUG RING #6 16-22AWG RED	2	EA	

DWG. NO 0117-0294 SH 1 REV B

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50		PILOT REL PER ECN	SAR		
51	3938	PER ECO	DW	DW	9/16/83
A	3957	PROD REL PER ECO NO	JWC	DW	9/4/83
B	4229	PER ECO 4229	KAREN	DW PM	1/22/84
B 1/2	4379	PER ECO 4379	DK.	DW	2/27/84

- 10 SHOWN





DETAIL A

SCALE : 2/1

NOTES -

1. NOMENCLATURE : CHARACTERS TO BE 8PT, WHITE CAPS 1 PLACE EACH CONTACT HOUSING (TYPICAL -10,-20,-30 -40 -50 VERSIONS
2. ALL RESISTORS ARE 100Ω 1/8W 5% CARBON COMP.
3. BAG & TAG WITH PART Nº 0117-0294 , DASH NO AND REV LEVEL.
4. CENTER LEADS IN HOUSING
5. MAX VARIATION OF INDIVIDUAL LEADS(11) SHALL BE .20.

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
50	0120-0057	1
30	0120-0057	1
50	0120-0038	2
30	0120-0038	2
40	0515-0057	1
30	0117-3200	4
20		
10		

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES, .XX ± .03 ± 1°, XXX ± .010
HOLE SIZE: .0-.599 +.003, .600-.999 +.004, 1.000-1.499 .005

ENG. SERV | DATE

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DRAWN S.RICO 5/4/83
CHECKED R. Wood 5/13/83
PROJ ENG [illegible] 5/13/83
MANUFACTURING [illegible] 5-13-83
QUALITY ASSUR [illegible] 5/13/83

GOULD biomation

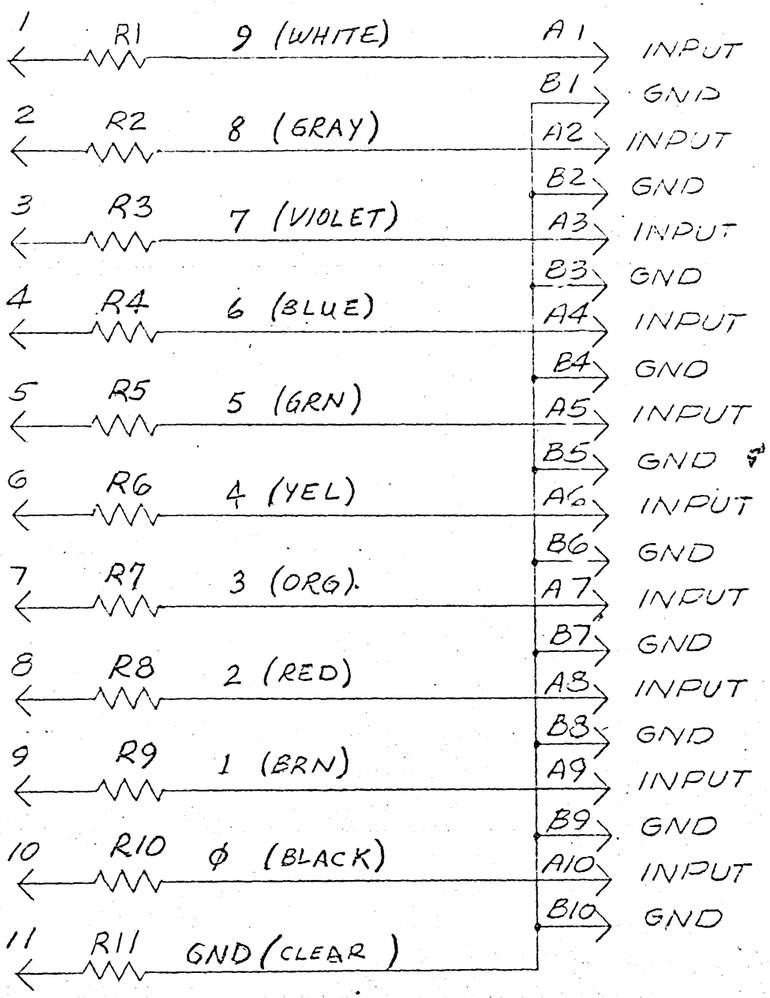
TITLE ASSY, INPUT CABLE, 11 LEADS, K105

SCALE	SIZE	PART NUMBER	REV
1/1	B	0117-0294	B

CODE K105 SHEET 1 OF 3

DWG. NO 0117-0294 SH 2 REV B

REVISIONS					
REV	ECO=	DESCRIPTION	DWN	CHKD	DATE
		SEE SH 1			



DASH	-10	-20	-30	-40	-50
1	J	R	J	C	R
	—	—	—	—	—
	K	S	K	Q	S
	—	—	—	—	—
	F	7	7	7	F
	—	—	—	—	—
	E	6	6	6	E
	—	—	—	—	—
	D	5	5	5	D
	—	—	—	—	—
	C	4	4	4	C
	—	—	—	—	—
	B	3	3	3	B
	—	—	—	—	—
	A	2	2	2	A
	—	—	—	—	—
	9	1	1	1	9
	—	—	—	—	—
	8	0	0	0	8
	GND	GND	GND	GND	GND

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES .XX ± .020 ± 1° .XXX ± .010

HOLE SIZE: .0-.599 + .003 .600-.999 ± .004 1.000-1.499 ± .005

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

DRAWN	S. RICO	DATE 5/4/83
CHECKED	R. Wood	5/13/83
PROJ. ENG.		5/13/83
MANUFACTURING		5/13/83
ENG. SERV.	R. Simon	DATE 1/11/82
QUALITY ASSUR		5/13/83

GOULD biomation

TITLE ASSY, INPUT CABLE, 11 LEAD, K105

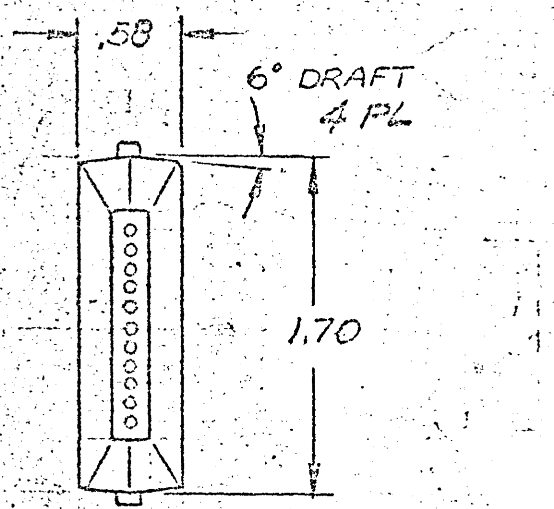
SCALE	SIZE	PART NUMBER	REV
NONE	B	0117-0294	B

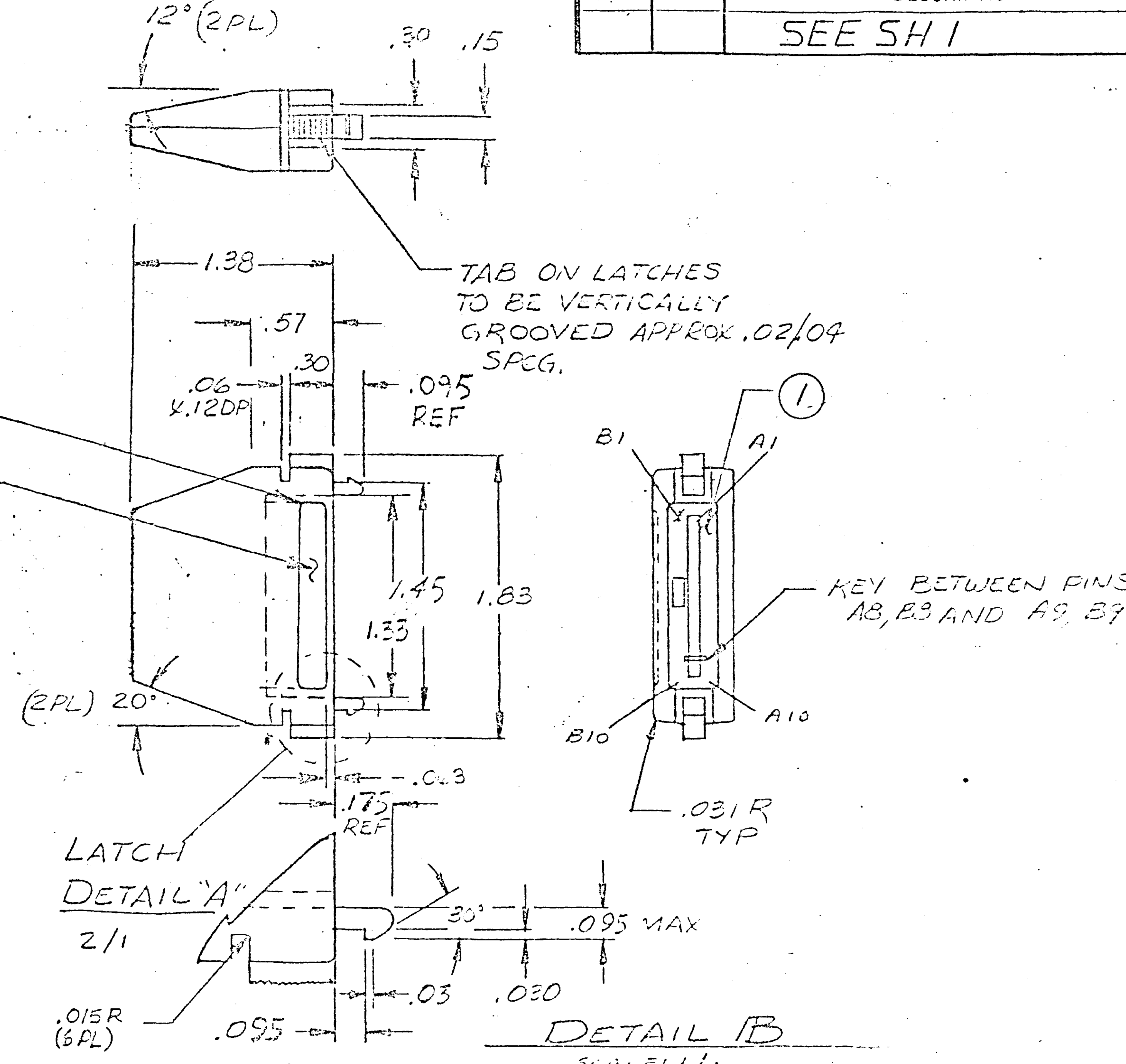
CODE K105. SHEET 2 OF 3

DWG. NO. 0117-0294 SH 3 B

REVISIONS

REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
		SEE SH 1	SAR		





1 MAT'L: HOUSING TO BE BLACK POLYPROPYLENE. BLOCK COPOLYMERS FLAME RETARDANT OR EQUIVALENT

2 FINISH: MATT TEXTURE PER MT 1013

								1
-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL:	ANGLES	HOLE SIZE
X ± .1	± 1°	0-.599 ± .003
.XX ± .020		.600-.999 ± .004
.XXX ± .010		1.000-1.499 ± .005

ENG. SERV. | DATE

		DATE
DRAWN	S. RICO	5/4/83
CHECKED	R. Wood	5/13/83
PROJ. ENG.	[illegible]	5/13/83
MANUFACTURING	[illegible]	5-13-83
QUALITY ASSUR	[illegible]	5/13/83

GOULD biomation

TITLE ASSY, INPUT CABLE 11 LEADS, K105

SCALE	SIZE	PART NUMBER	REV
1/1	B	0117-0294	B

CODE K105D SHEET 3 OF 3

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	LIST
1					1	1	1	1	1	6000-0396-30	CONNECTOR, 10 PIN DUAL		
2													
3					A/R	A/R	A/R	A/R	A/R	7100-0121-01	WIRE, WHT, 24 AWG, 105/44		
4					↑	↑	↑	↑	↑	-09	GRY		
5										-10	VIO		
6										-06	BLUE		
7										-04	GRN		
8										-05	YEL		
9										-08	ORG		
10										-03	RED		
11										-07	BRN		
12					↓	↓	↓	↓	↓	-02	BLK		
13					A/R	A/R	A/R	A/R	A/R	7100-0121-11	WIRE, CLEAR, 24 AWG, 105/44		
14					11	11	11	11	11	2950-1000-10	RESISTOR 100Ω, 1/8W, 5%, CAB		
15					11	11	11	11	11	6100-0131-10	SOCKET		
16					11	11	11	11	11	0112-0323-02	CONTACT HSG, BLK NYLON		

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL 5957	5/6/83	DAL	DWJ KR
B	PER ECO 4229	11084	KR	
B½	PER ECO 4379	8-31-84	D.C	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-50	C120-0057	1
-50	0120-0036	2
-40	0515-0057	1
-30	0117-0200	4
-20		
-10		

		DATE
DWN	S. RICO	5/4/83
CHK	R. Wood	6/6/83
ENGR		5/13/83
MFG.		5/13/83
QA		5/13/83

LIST OF MATERIAL

ASSY, INPUT CABLE
11 LEAD, K105

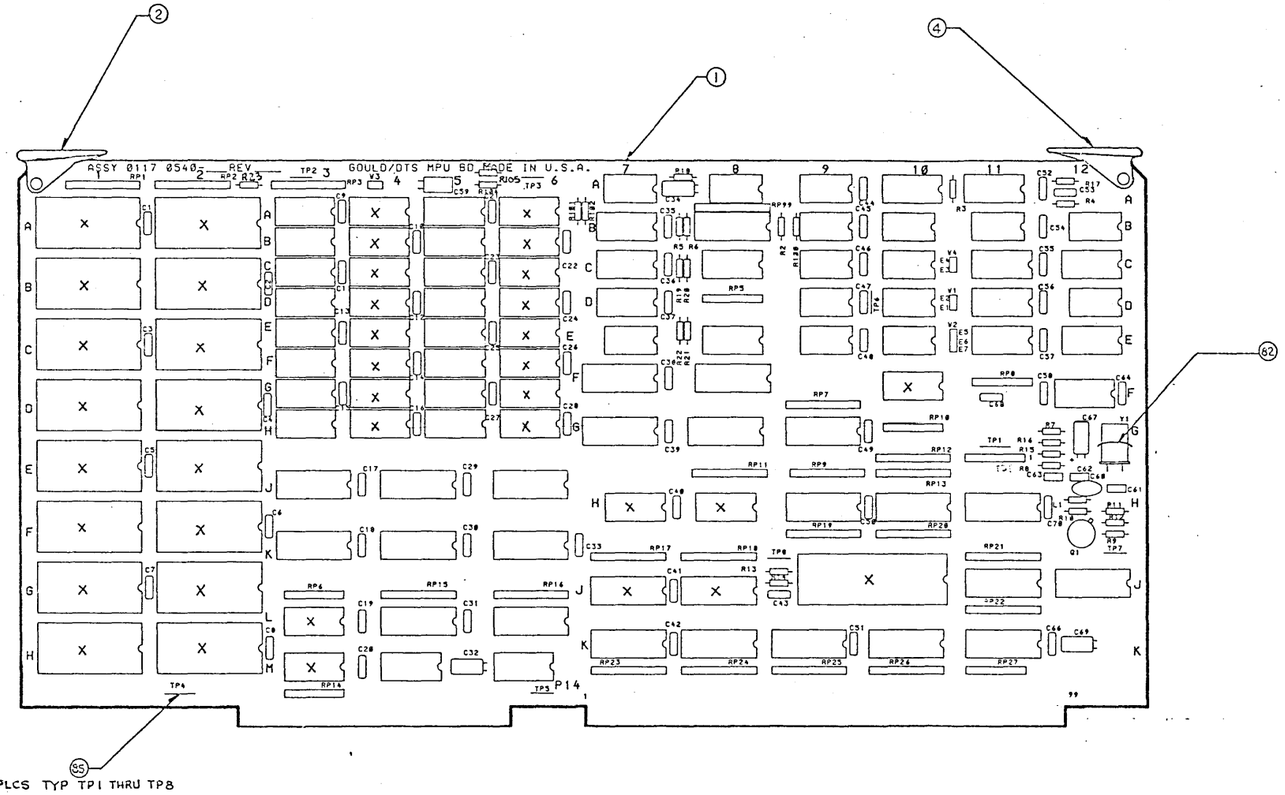
GOULD biomation

B	0117-0294	REV B

MODEL K105 SHEET 1 OF 1

0117-0540-10

REVISIONS						
ZONE	REV.	ECO#	DESCRIPTION	DWN	CHKD	APPD
	50	5124	NEW RELEASE	GS		
	51	5149	REL PER ECO 3/14/86	DW		



-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN	10/25/85
CHECKED	10/28/85
PROJ ENG	

GOULD Electronics

TITLE: ASSY-PCB, MPU BOARD

DASH NO.	NEXT ASSY	USED ON
	K450-XXX	

FIRST APPLICATION

SIZE D | DWG. NO. 0117-0540-10 | REV. 51

SCALE | MODEL 450 | SHEET 1 OF 1

DIETRICH PORST RECORDER NO.

BILL OF MATERIAL

AS OF 02/12/86

0117-0540-10 ASSY,PCB,MPU,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0117-0540	DWG,ASSY,MPU BOARD,K450	0	EA	
0	D0117-0541	DWG,SCHEM,MPU BOARD,K450	0	EA	
1	0117-0542-10	FAB,PCB,MPU,K450	1	EA	
2	7000-0120-10	CARD EJECTOR NYLON 6/6	1	EA	
4	0112-0228-07	CARD EJECTOR-HOT STAMPED (A7)	1	EA	
11	0121-0050-10	SPEC,PROM,512X4,K450 MAP	1	EA	10F
12	0121-0055-10	SPEC,PROM,256X4 ROM SELEC (HI)	1	EA	3L
13	0121-0060-10	SPEC,PROM 256X4 ROM SELEC (LO)	1	EA	3M
15	1800-0321-10	IC D8086 16 BIT HMOS	1	EA	10J
20	1800-0581-10	IC DRAM 256KX1	16	EA	4A,4B,4C 4D,4E,4F 4G,4H,6A 6B,6C,6D 6E,6F,6G 6H
21	6100-0120-10	SKT 16 PIN DIP LO-PROFIL	21	EA	X10F X3L,X3M, X4A-X4H, X6A-X6H, X8H,X7H
23	1400-0019-10	TRAN 2N3906	1	EA	Q1
25	1800-0031-10	IC 74S00N 14 NAND X4	3	EA	10C,12B,9B
26	1800-0038-10	IC 74S20N 14 NAND X2	1	EA	9C
27	1800-0039-10	IC 74S112N DUAL J-K F/F	8	EA	10A,11A 11C,11D 11E,12C 12E,12F
28	1800-0060-10	IC 74S10N 14 NAND X3	4	EA	12D 7A 8A 9D
29	1800-0092-10	IC 74S04N, 14, INV, X6	1	EA	10E
30	1800-0107-10	IC 74LS04N HEX INV	1	EA	9E
31	1800-0125-10	IC 74LS161N 20CNTR, SYN, BIN	4	EA	7C,7D,8C 8E
32	1800-0133-10	IC 74S11N 3-INPUT AND G	1	EA	10B
33	1800-0136-10	IC 74S51N DUAL 2-WIDE	1	EA	10D
34	1800-0208-10	IC 74S161N 4BIT BIN CNTR	1	EA	7B
35	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	9	EA	3J,3K,4J 6J,7F,7G 8F,8G,9G
36	1800-0243-10	IC 74S08N 14 AND X4	2	EA	11B,9A
37	1800-0268-10	IC 74LS245N BUS TRANS	2	EA	7K,8K
38	1800-0298-10	IC 74LS373N OCTAL D TYP	10	EA	10H,10K 11J,11K 4K,4L,6K 6L,9H,9K
40	1800-0335-10	IC 74LS166N 8-BIT SHIFT	2	EA	4M,6M

BILL OF MATERIAL
AS OF 02/12/86

0117-0540-10 ASSY,PCB,MPU,K450
MODEL: K450

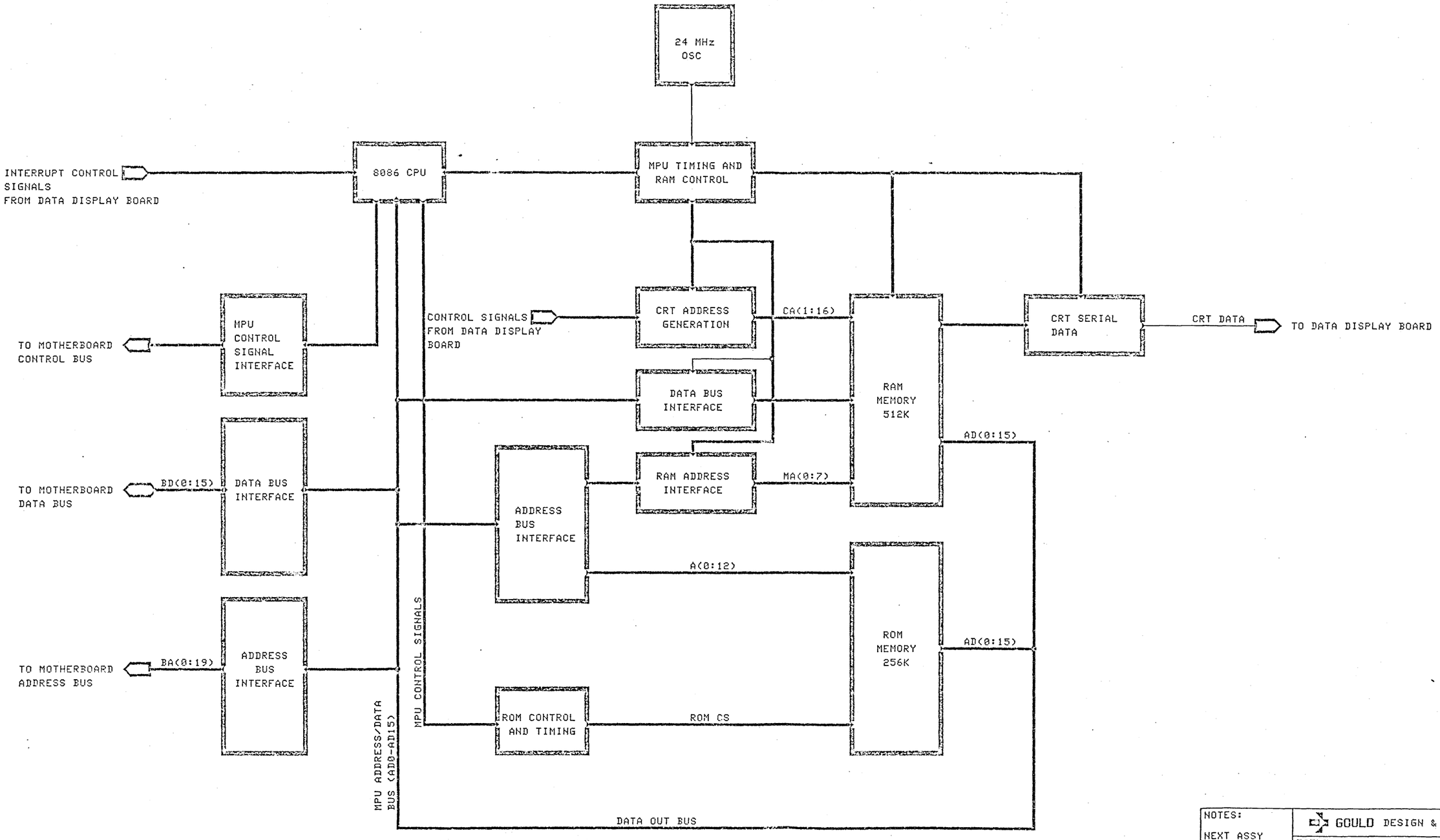
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
42	1800-0261-10	IC 74S240N 20 BFR,INV,X8	3	EA	8B,11H,12J
43	2100-0009-10	IND 1025-24 FERRITE CORE	1	EA	L1
46	3000-1000-10	RES,100,5%,1/4W,C	1	EA	R11
47	3000-1300-10	RES,130,5%,1/4W,C	1	EA	R9
48	3000-1601-10	RES,1.6K,5%,1/4W,C	2	EA	R6,R10
49	3000-2006-10	RES,20,5%,1/4W,C	1	EA	R4
50	3000-2200-10	RES,220,5%,1/4W,C	4	EA	R104 R7,R19,R21
51	3000-2201-10	RES,2.2K,5%,1/4W,C	7	EA	R15,R17 R18,R23 R2,R3,R5,
52	3000-2700-10	RES,270,5%,1/4W,C	1	EA	R13
53	3000-3300-10	RES,330,5%,1/4W,C	3	EA	R105 R8,20,22
54	3000-3301-10	RES,3.3K,5%,1/4W,C	1	EA	R12
55	3000-5100-10	RES,510,5%,1/4W,C	1	EA	R16
56	3000-9106-10	RES,91,5%,1/4W,C	1	EA	R14
57	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	13	EA	RP1,2,7,9 RP15,16,17 RP18,22,23 RP24,25,26
58	3700-0057-10	RPAK,2.2K,0.18W,2%,8/7	6	EA	RP14,27 RP5,6,8,10
59	3700-0065-10	RPAK,220/330,1/8W,5%,10/16	5	EA	RP11,12,13 RP3
60	3700-0066-10	RPAK,10K,0.18W,2%,10/9	3	EA	RP19,20,21
63	4000-0040-10	CAP,470PF,50V,10%,CER	1	EA	C43
64	4000-0044-10	CAP,0.01UF,100V,20%,CER	61	EA	C1-31,C33 C35-42,C68 C44-52, C54-58, C61-66
67	4100-0019-10	CAP,50PF,500V,5%,MICA	1	EA	C53
68	4100-0029-10	CAP,30PF,500V,5%,MICA	1	EA	C60
70	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	5	EA	67,69 C32,34,59,
72	5100-0016-10	XTAL 24.0MHZ,.015%	1	EA	Y1
74	6000-0190-10	CONN 8 PIN HDR ST SGL ROW	1	EA	TC1
78	6100-0123-10	SKT 40 PIN DIP	1	EA	X10J
79	6100-0151-10	SKT 28 PIN DIP LO PROFIL	16	EA	X1A-X1H X2A-X2H
82	7100-0017-10	WIRE,BUS,22 GA,TINNED	0	FT	
85	9000-0054-10	BUSS WIRE, FORMED	8	EA	TP1-8
88	0121-0045-10	ASSY,PROM SET,K450 MAIN CODE	1	ST	1A,1B,1C, 1D,1E,2A, 2B,2C,2D,

BILL OF MATERIAL
AS OF 02/12/86

0117-0540-10 ASSY,PCB,MPU,K450
MODEL: K450

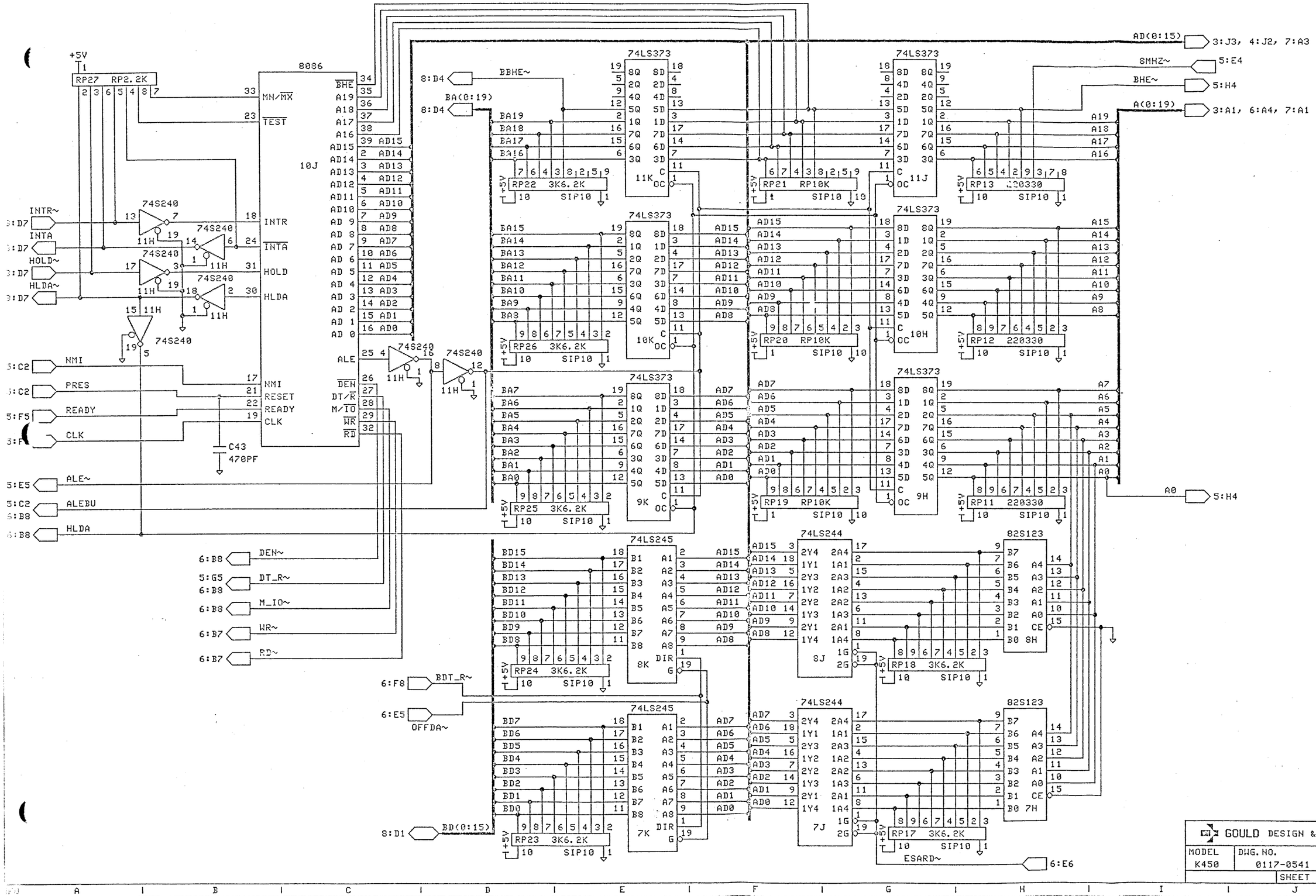
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
88	0121-0045-10	ASSY,PROM SET,K450 MAIN CODE	1	ST	2E
89	3000-3306-10	RES,33,5%,1/4W,C	3	EA	102 R100,101,
90	3700-0139-10	RPAK 33 OHM 10SIP	1	EA	RP99
95	1800-0324-10	IC 74LS125PC QUAD BUS BUF	1	EA	7E

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	51	5149	REVISED PER ECO 3/13/86	DW		



NOTES:	GOULD DESIGN & TEST	
NEXT ASSY	TITLE: SCHEMATIC MPU BOARD	
	PART NUMBER: 0117-0541	
0117-0003-70	SHEET 1 OF 8	REV 5J
0117-0003-60		

04 NOV 85 11:45 /USER/VLSI86C87/MPU_BLOCK.DRAW

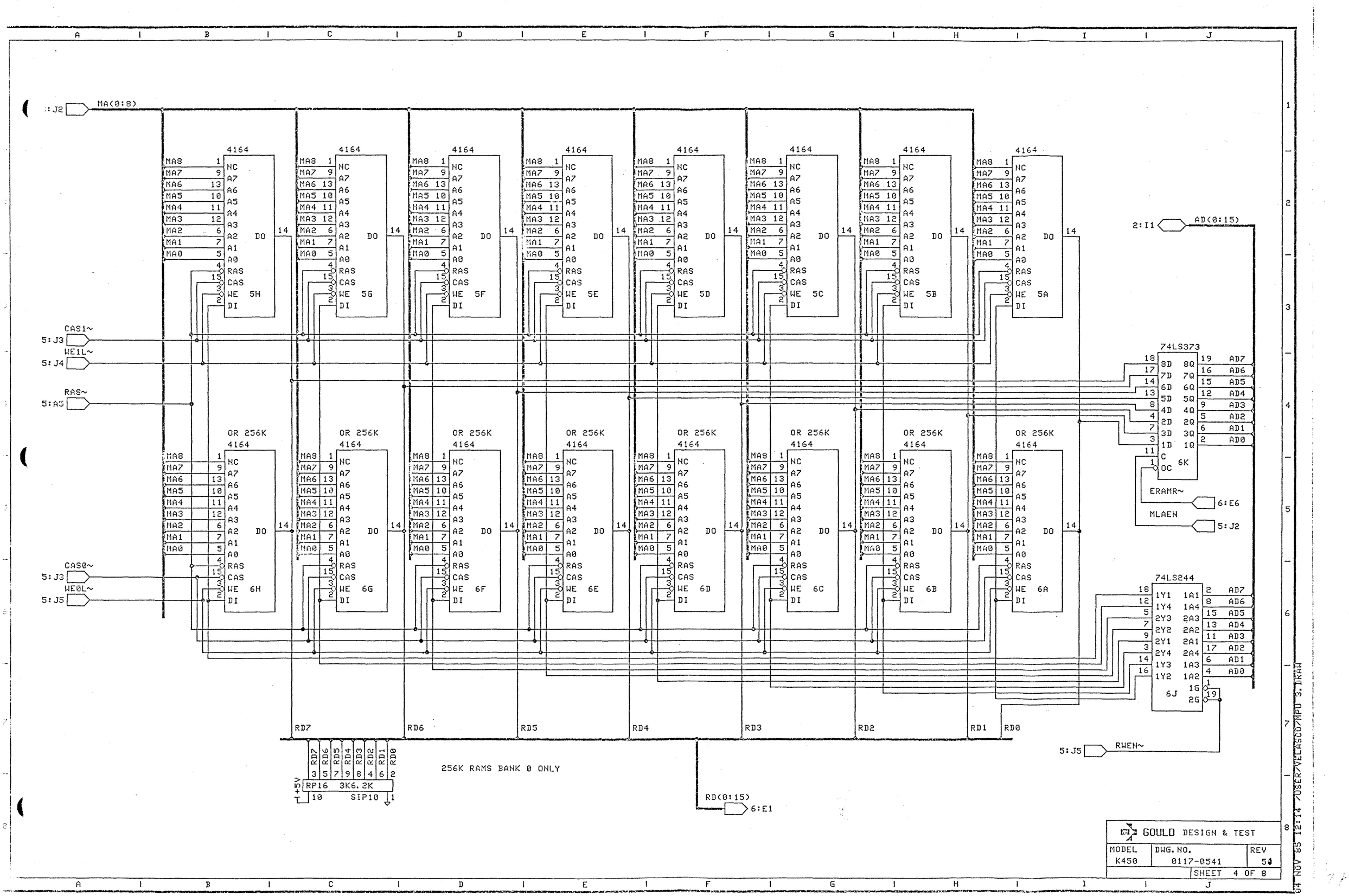

8086
74LS373
74S240
74LS245
74LS244
82S123
RP27 RP2.2K
RP22 3K6.2K
RP21 RP10K
RP13 220330
RP26 3K6.2K
RP20 RP10K
RP12 220330
RP25 3K6.2K
RP19 RP10K
RP11 220330
RP24 3K6.2K
RP18 3K6.2K
RP23 3K6.2K
RP17 3K6.2K
C43
470PF
+5V
SIP10
INTR~
INTA
HOLD~
HLDA~
NMI
PRES
READY
CLK
ALE~
ALEBU
HLDA
DEN~
DT_R~
M_IO~
WR~
RD~
BDT_R~
OFFDA~
BD(0:15)
BBHE~
BA(0:19)
AD(0:15)
8MHZ~
BHE~
A(0:19)
A0
ESARD~
3:J3, 4:J2, 7:A3
5:E4
5:H4
3:A1, 6:A4, 7:A1
5:H4
6:E6
GOULD DESIGN & TEST
MODEL K450
DWG. NO. 0117-0541
REV 5
SHEET 2 OF 8
04 NOV 85 11:52 /USER/VELASCO/MPU_1.DRAW

A(0:19)
5:J2
A18
A17
74LS244
74LS125
7E
220
220 R104
330
330 R105
MA8
MA(0:8)
4:A1
MCOLS~
5:J1
MROWS~
5:J2
CAS1~
5:J3
WE1H~
5:J4
RAS~
5:A5
CCOLS~
5:J1
CAS0~
5:J3
WE0H~
5:A4
CROWS~
5:J1
CA(1:16)
6:J1
4164
OR 256K
7F
7G
8F
8G
3H
3G
3F
3E
3D
3C
3B
3A
4H
4G
4F
4E
4D
4C
4B
4A
AD(0:15)
2:I1
74LS373
4J
4K
ERAMR~
6:E6
MLAEN
5:J2
RWEN~
5:J5
74LS125
MA8
RP3 220330
RP15 3K6.2K
+5V
SIP10
RD15
RD14
RD13
RD12
RD11
RD10
RD9
RD8
256K RAMS BANK 0 ONLY
RD(0:15)
6:E1

GOULD DESIGN & TEST

MODEL	DWG. NO.	REV
K450	0117-0541	50
	SHEET 3 OF 8	

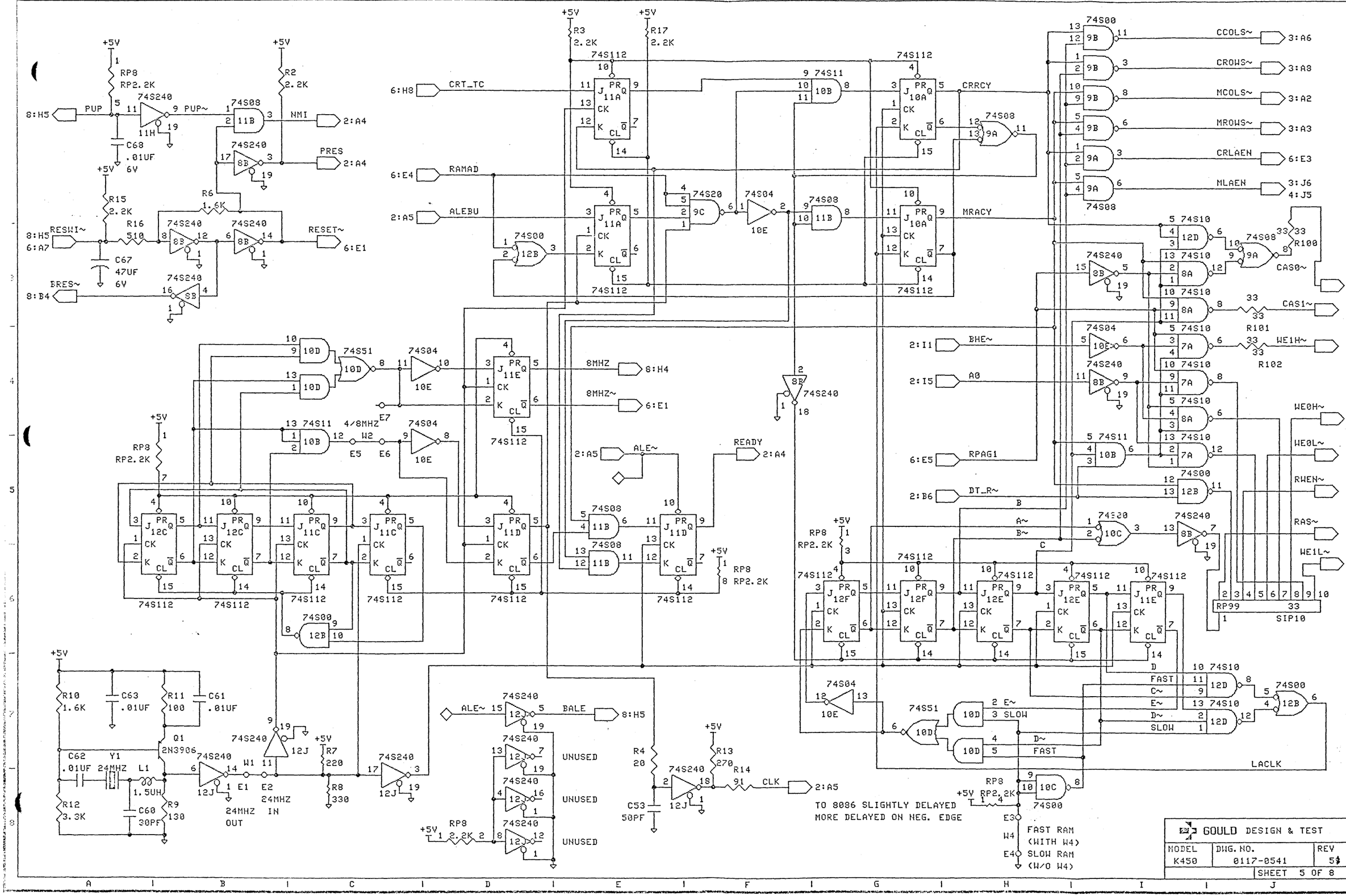
04 NOV 85 12:11 /USER2/VELASCO/MPU 2.DRAW



GOULD DESIGN & TEST

MODEL	DWG. NO.	REV
K450	0117-0541	5
	SHEET 4 OF 8	

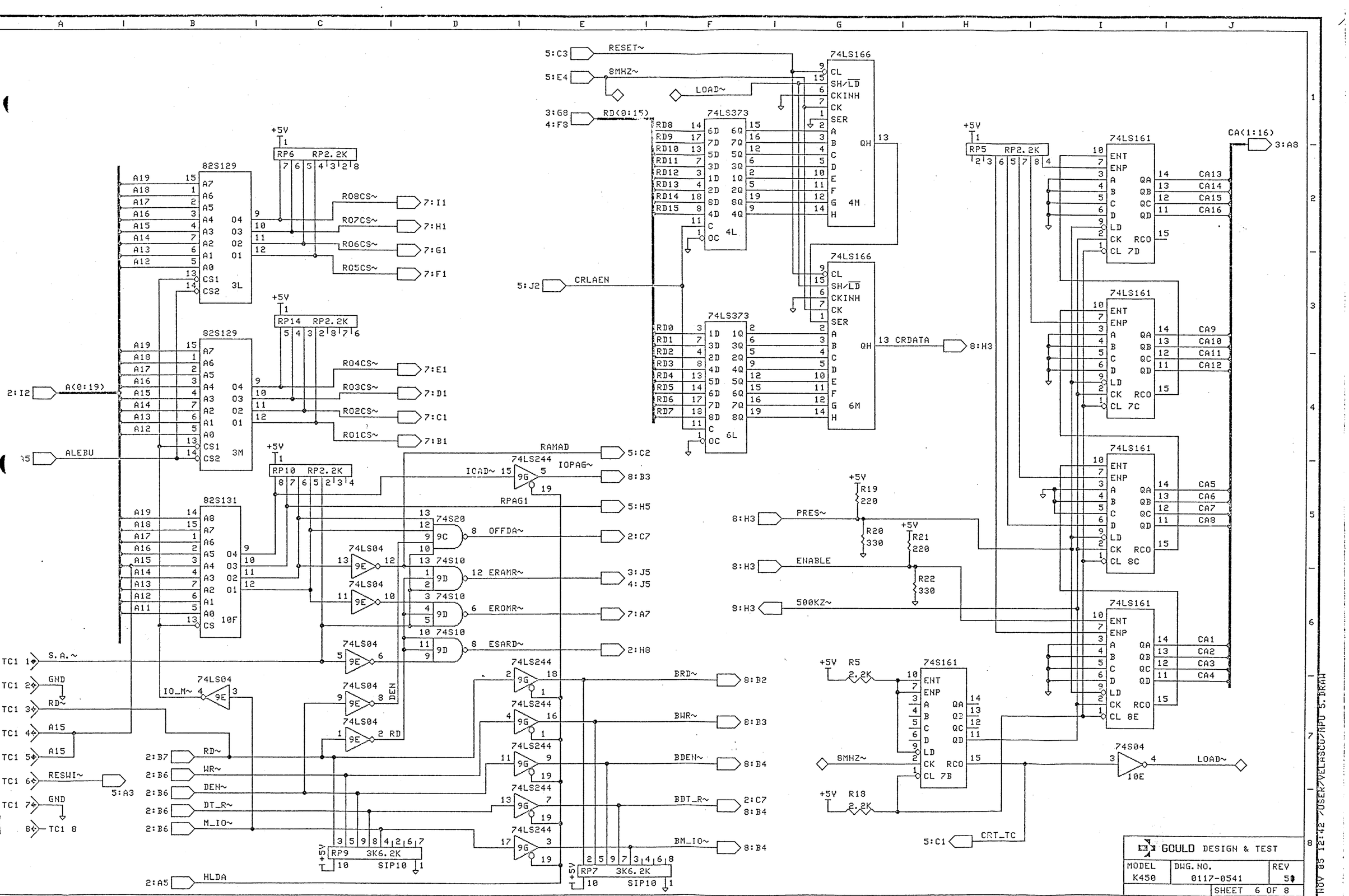
04 NOV 85 12:14 /USER/VELASCO/MPU 3.DRAW



GOULD DESIGN & TEST

MODEL	DWG. NO.	REV
K450	0117-8541	5$
	SHEET 5 OF 8	

04 NOV 85 12:39 /USER7/RELEASC07/MPU 4.DRAW


5:C3 RESET~
5:E4 8MHZ~
LOAD~
3:G8 4:F8 RD(0:15)
74LS166
74LS373
5:J2 CRLAEN
13 CRDATA
8:H3
+5V
RP6 RP2.2K
RP14 RP2.2K
RP10 RP2.2K
RP5 RP2.2K
82S129
82S131
R08CS~ 7:I1
R07CS~ 7:H1
R06CS~ 7:G1
R05CS~ 7:F1
R04CS~ 7:E1
R03CS~ 7:D1
R02CS~ 7:C1
R01CS~ 7:B1
2:I2 A(0:19)
5 ALEBU
RAMAD 5:C2
IOPAG~ 8:B3
RPAG1 5:H5
74S20 OFFDA~ 2:C7
74LS04
74S10 12 ERAMR~ 3:J5 4:J5
EROMR~ 7:A7
ESARD~ 2:H8
74LS244
BRD~ 8:B2
BWR~ 8:B3
BDEN~ 8:B4
BDT_R~ 2:C7 8:B4
BM_IO~ 8:B4
DEN
TC1 1 S.A.~
TC1 2 GND
TC1 3 RD~
TC1 4 A15
TC1 5 A15
TC1 6 RESWI~ 5:A3
TC1 7 GND
TC1 8
2:B7 RD~
2:B6 WR~
2:B6 DEN~
2:B6 DT_R~
2:B6 M_IO~
2:A5 HLDA
RP9 3K6.2K SIP10
RP7 3K6.2K SIP10
R19 220
R20 330
R21 220
R22 330
8:H3 PRES~
8:H3 ENABLE
8:H3 500KZ~
R5 2.2K
R18 2.2K
74LS161
CA(1:16) 3:A8
CA13 CA14 CA15 CA16
CA9 CA10 CA11 CA12
CA5 CA6 CA7 CA8
CA1 CA2 CA3 CA4
5:C1 CRT_TC
GOULD DESIGN & TEST
MODEL K450
DWG. NO. 0117-0541
REV 5
SHEET 6 OF 8
04 NOV 85 12:42 /USER/VELASCO/MPU 5.DRAW

NOTE: W3 FOR 27256 EPROM ONLY

+5V

R23 2.2K

W3 E8 E9

A15

2:I2 A(0:19)

6:D4 RO1CS~ 6:D4 RO2CS~ 6:D4 RO3CS~ 6:D4 RO4CS~ 6:D3 RO5CS~ 6:D2 RO6CS~ 6:D2 RO7CS~ 6:D2 RO8CS~

2764 (1H, 1G, 1F, 1E, 1D, 1C, 1B, 1A)

D(0:7)

RP1 3K6.2K SIP10

D0 D1 D2 D3 D4 D5 D6 D7

4 6 8 9 7 5 3 2

2:I1 AD(0:15)

74LS244 (3J)

AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8

2Y4 2Y3 2Y2 2Y1 1Y4 1Y3 1Y2 1Y1

2A4 2A3 2A2 2A1 1A4 1A3 1A2 1A1

1G 2G

2764 (2H, 2G, 2F, 2E, 2D, 2C, 2B, 2A)

C(0:7)

RP2 3K6.2K SIP10

C0 C1 C2 C3 C4 C5 C6 C7

4 6 8 9 7 5 3 2

74LS244 (3K)

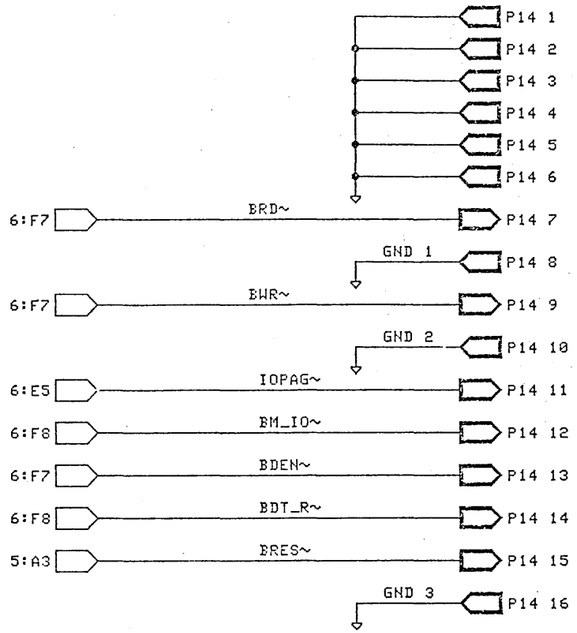
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

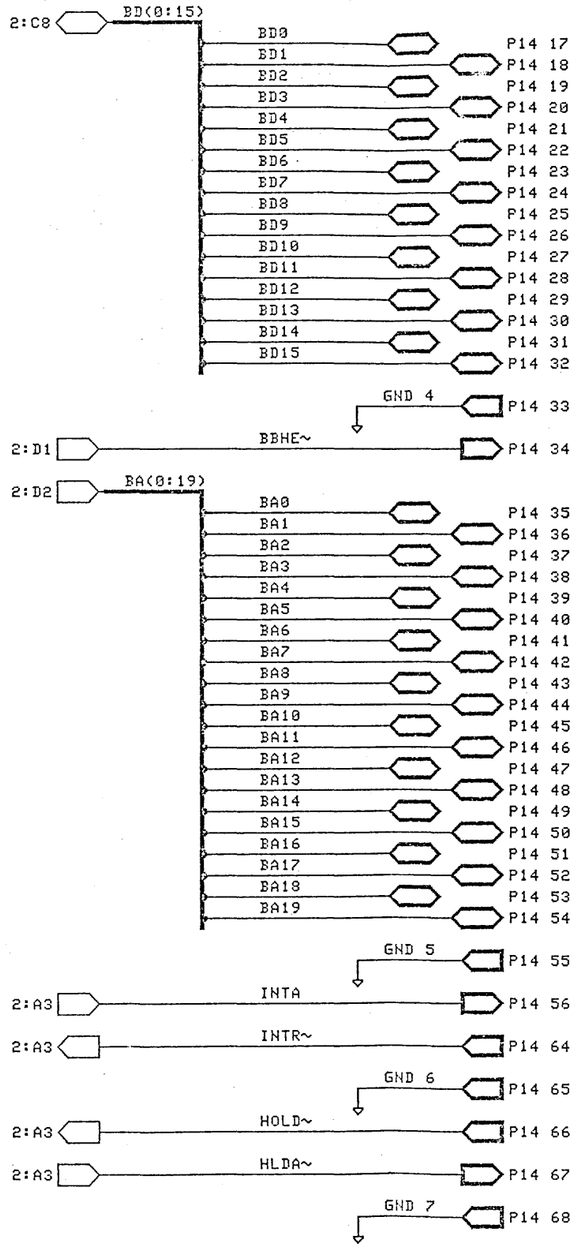
6:E6 EROMR~

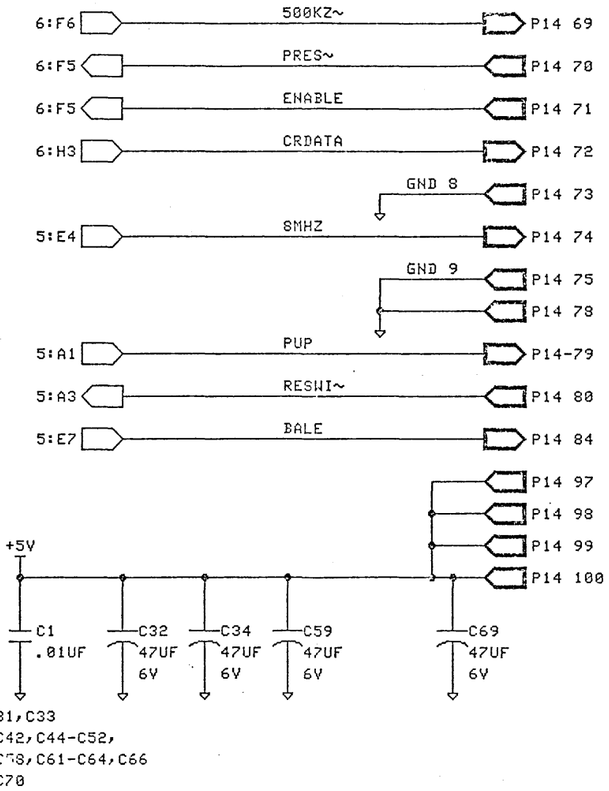
GOULD DESIGN & TEST

MODEL	DWG. NO.	REV
K450	0117-0541	5@
	SHEET 7 OF 8	

04 NOV 85 12:44 /USER/VELASCO/MPU 6.DRAW







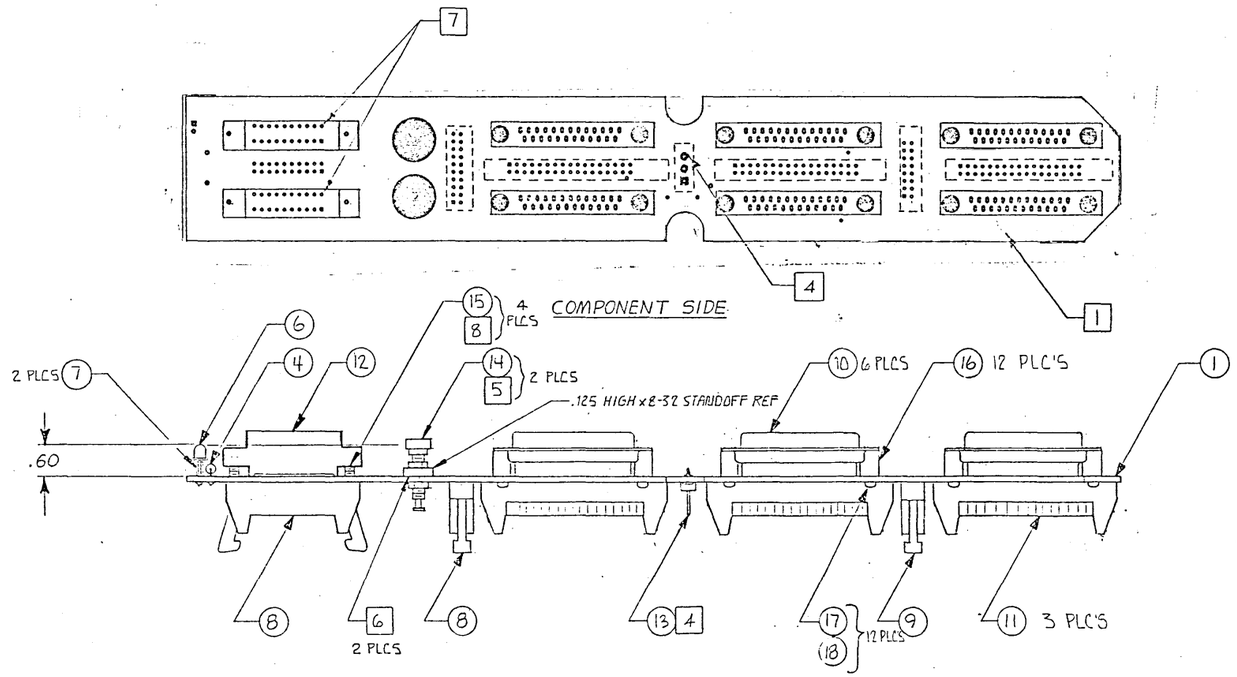
GOULD DESIGN & TEST

MODEL	DWG. NO.	REV
K450	0117-0541	5
	SHEET 8 OF 8	

04 NOV 85 15:04 /USER/VELASCO/MPU 2.DRAW

DWG. NO. 0120-0025 REV B

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHK'D	DATE
	01		PROTOTYPE			
	02		PROTOTYPE			
	03		REVISED			12-12-82
	50	4393	PILOT REL PER ECO#			12-23-83
	51	4442	REVISED PER ECO Nº			3/16/84
	52	4638	REVISED PER ECO			7/23/84
	A	4791	REVISED PER ECO 11-29-84			12/5/84
	B	5130	REV'D PER ECO 2-10-86			2/10/86



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK ASSEMBLY DASH NO., REVISION LEVEL AND SERIAL NO. APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK.
2. ASSEMBLY REFLECTS SCHEMATIC DRAWING 0120-0026 AND FABRICATION DRAWING 0120-0027
3. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.

4 CUT OFF PIN 3.

5 USE NUT AND LOCK WASHER SUPPLIED WITH CONNECTOR ITEM 14. DISCARD PLASTIC SPACER..

6 SOLDER SWAGED SIDE OF .125 HIGH x 8-32 STANDOFF TO PAD ON BOARD.

7 FOR ASSEMBLY-ITEM 12 PIN 1 IS ABOVE THE SQUARE PAD.

8 TEMPORARILY SECURE ITEM 15 WITH 4-40 SCREWS & NUTS.

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± .1, ANGLES ± 1°, XX ± .020, XXX ± .010
HOLE SIZE: 0.039 ± .003, 500 .999 ± .004, 1.000-1.499 ± .005

DASH NO.	NUMBER	QTY
	0120-0026	1
	NEXT ASSEMBLY	

DRAWN D.C 3-22-83
CHECKED 4/26/84
PROJ. ENG. 4/26/84
MANUFACTURING 4/24/84
QUALITY ASSUR 4/24/84
ENG. SERV. DATE

GOULD Instruments Division Santa Clara Operations

TITLE ASSEMBLY, K205 INPUT BD.

SCALE 1/1 | SIZE D | PART NUMBER 0120-0025 | REV B

MODEL K205 | SHEET 1 OF 1

SIGNATURE & TAYLOR REQUIRED PER MD 40-107-10

BILL OF MATERIAL

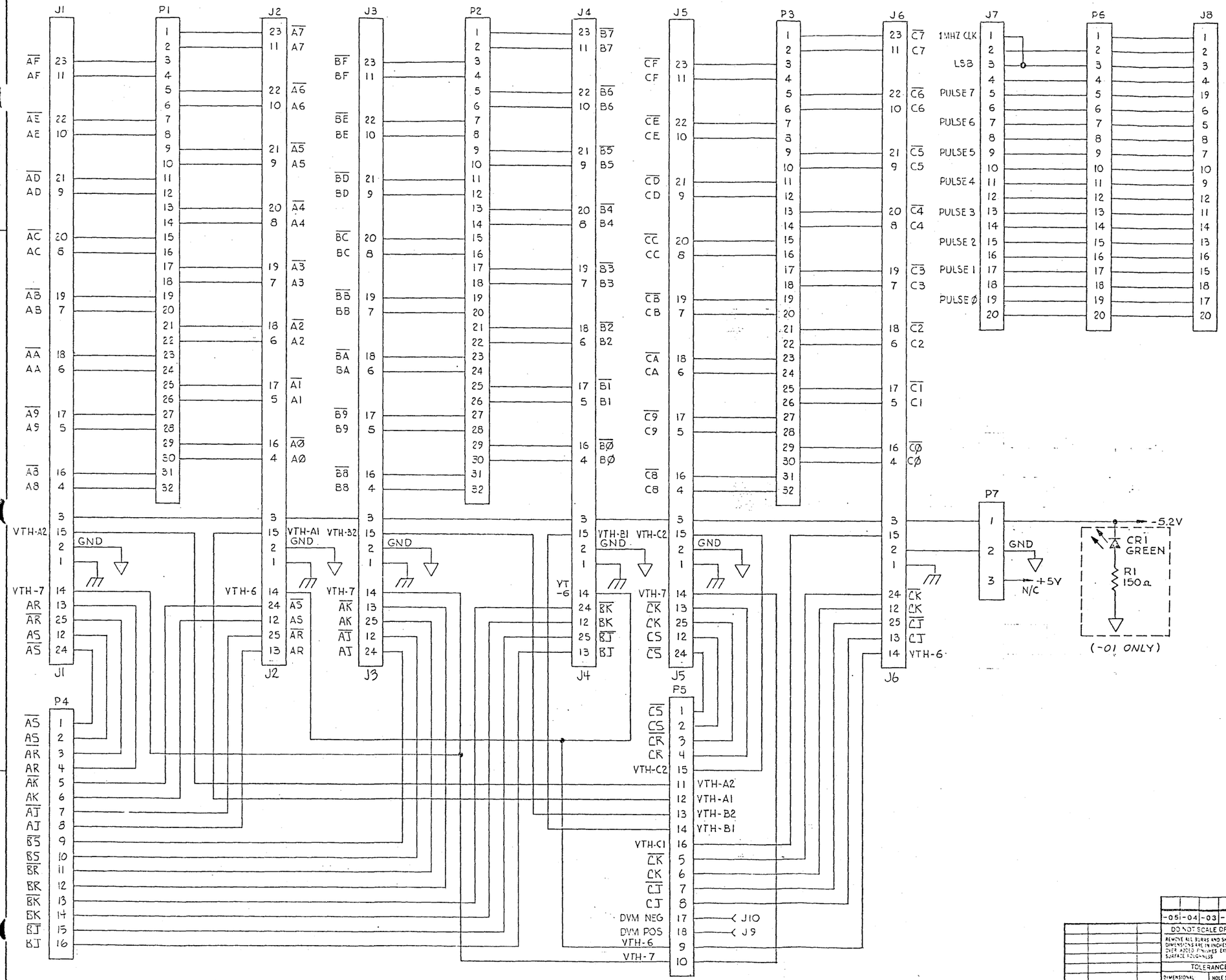
AS OF 02/12/86

0120-0025-01 ASSY,PCB,INPUT,K205
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0120-0025	DWG,ASSY,PCB INPUT	0	EA	REF
0	D0120-0026	DWG,SCHEM,INPUT BD,K205	0	EA	REF
1	0120-0027-01	FAB,PCB,INPUT,K205	1	EA	
4	3000-1500-10	RES,150K,5%,1/4W,C	1	EA	R1
6	6400-0041-10	LED, GRN, 20MA	1	EA	CR1
7	7200-0050-10	TUBING,SHRINK,3/16	0	FT	
8	6000-0271-10	CONN 20 PIN,HDR,ST,DBL,W/E	2	EA	P5,P6
9	6000-0271-20	CONN,16PIN,HDR ST DBL W/E	1	EA	P4
10	6000-0367-10	CONN 25 PIN, D-SUB	6	EA	J1-6
11	6000-0585-10	CONN 34PIN HDR STR S/EAR	3	EA	P1-3
12	6000-0396-10	CONN 10/20 C-EDGE	2	EA	J2,8
13	6000-0335-03	CONN 3 PIN HDR	1	EA	P7
14	6000-0041-10	CONN PIN JACK .080 DIA	2	EA	J9,J10
15	7000-0253-10	SPACER,RND 3/16 #6,LG	4	EA	
16	7000-0426-10	STDF RND 7/16X440 A F	12	EA	
17	7011-1440-08	SCR,X,PH,4-40 X 1/4,STZN	12	EA	
18	7080-1004-00	WSHR,FLAT,#4,SP,STZN	12	EA	

DWG. NO. 0120-0026 | SH. 1 | REV. B

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	01		PROTOTYPE			
	02		PROTOTYPE	DC		
	50	4343	PILOT REL PER ECO #	SAH	JL	11-83
	51	4442	REVISED PER ECO N°	LNC	TS	3/4/84
	52	4638	REVISED PER ECO	RTM	RJ	7/23/84
	A	4771	REVISED PER ECO 11-27-84	SAR	DCW	4/2/85
	B	5130	REV'D PER ECO 2-10-86	RTM	DWJ	3/10/86



NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS 5%, 1/4 W.

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X = 1 ANGLES; XX = .020 = 1°; XXX = .010
HOLE SIZE: 0.599 = .003; 600-999 = .004; 1.000-1.499 = .005

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

ENG. SERV. | DATE

DRAWN	D.C	DATE 3-22-83
CHECKED	R. Wood	3/25/85
PROJ. ENG.	[illegible]	11/21/84
MANUFACTURING	[illegible]	11/21/84
QUALITY ASSUR	[illegible]	11/21/84

GOULD Instruments Division Santa Clara Operations

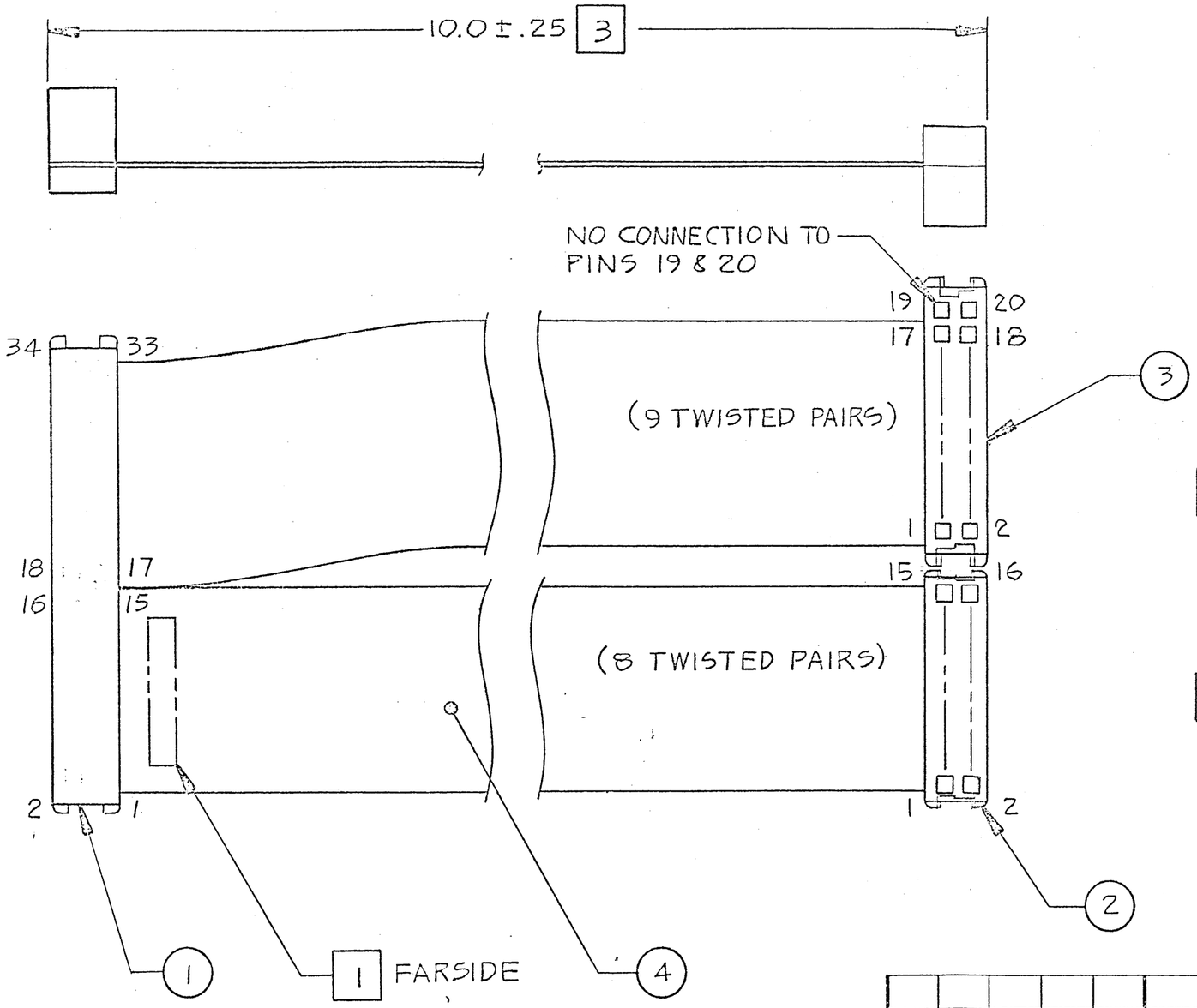
TITLE: SCHEMATIC, K205 INPUT BD.

SCALE	SIZE	PART NUMBER	REV
NONE	D	0120-0026	B

MODEL K205 | SHEET 1 OF 1

DWG. NO. 0120-0042-01 | SH 1 | REV. 51

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50	4293	PILOT REL. PER ECO	RM	DJW	1/2/84
51	4638	REVISED PER ECO	RTM	DGW JMC	3/13/84



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK CABLE WITH ASSY. NO., DASH NO. & REVISION LEVEL APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK. ALSO STAMP WITH VENDOR I.D.
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.
3. CONNECTORS MUST BE INSTALLED ON FLAT PORTIONS OF CABLE.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO.	NUMBER	QTY
01	0120-0004A	1
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES .XX ± .020 ± 1° .XXX ± .010

HOLE SIZE: .0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

		DATE
DRAWN	R Mercer	1/5/84
CHECKED	D G Weikart	1-12-84
PROJ. ENG.	A Hagen	1/10/84
MANUFACTURING	Ed Rees	1/10/84
QUALITY ASSUR.	K Crispin	1/13/84
ENG. SERV.		DATE

GOULD biomation

TITLE: ASSEMBLY, CABLE INPUT BD. TO MOTHERBOARD

SCALE	SIZE	PART NUMBER	REV
	B	0120-0042-01	51

CODE K205 SHEET 1 OF 1

KLINGLER K-VEL H

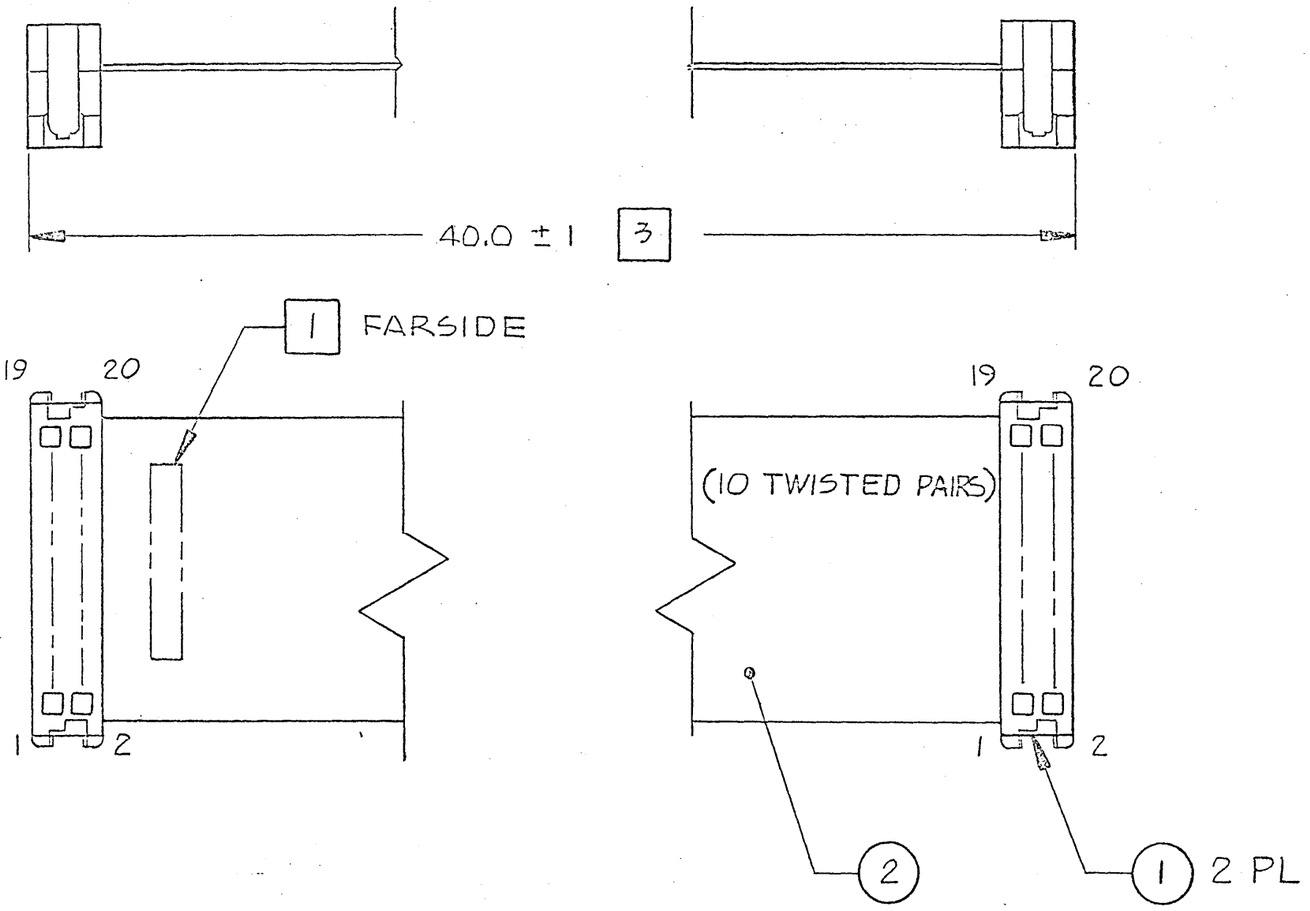
BILL OF MATERIAL

AS OF 02/12/86

0120-0042-01 ASSY,CBL,INPUT BD TO MB,K205
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0120-0042	DWG,ASSY,CABLE INPUT BD	0	EA	REF
1	6000-0391-20	CONN 34PIN W/O STRAIN REL	1	EA	
2	6000-0352-20	CONN SKT 16 CONTACT	1	EA	
3	6000-0273-10	CONN 20 PIN SKT	1	EA	
4	7100-0122-10	CBL,FLAT,28 AWG,TW,34 COND	1	FT	

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50	4293	PILOT REL. PER ECO	RM	DLW	1/12/84
51	4468	REVISED PER ECO N°	JWC	DGW	4/2/84



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK CABLE WITH ASSY. NO., DASH NO. AND REVISION LEVEL APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK. ALSO STAMP WITH VENDOR I.D.
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.
3. CONNECTORS MUST BE INSTALLED ON FLAT PORTIONS OF CABLE.

												1
-50	-40	-30	-20	-10	PART NUMBER		PART NAME		DESCRIPTION/SPECIFICATION			ITEM

DASH NO.	NUMBER	QTY
01	0120-0004	1
NEXT ASSEMBLY		

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES .XX ± .020 ± 1° .XXX ± .010

HOLE SIZE: .0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

ENG. SERV.		DATE
DRAWN	EMCRAY	1/4/83
CHECKED	DG WRIGHT	1-12-84
PROJ. ENG.		1/10/84
MANUFACTURING		1/10/84
QUALITY ASSUR		1/10/84

GOULD biomation

TITLE ASSY., CABLE, PROBE TEST TO CLOCK BD.

SCALE	SIZE	PART NUMBER	REV
NONE	B	0120-0043-01	51

CODE K205 SHEET 1 OF 1

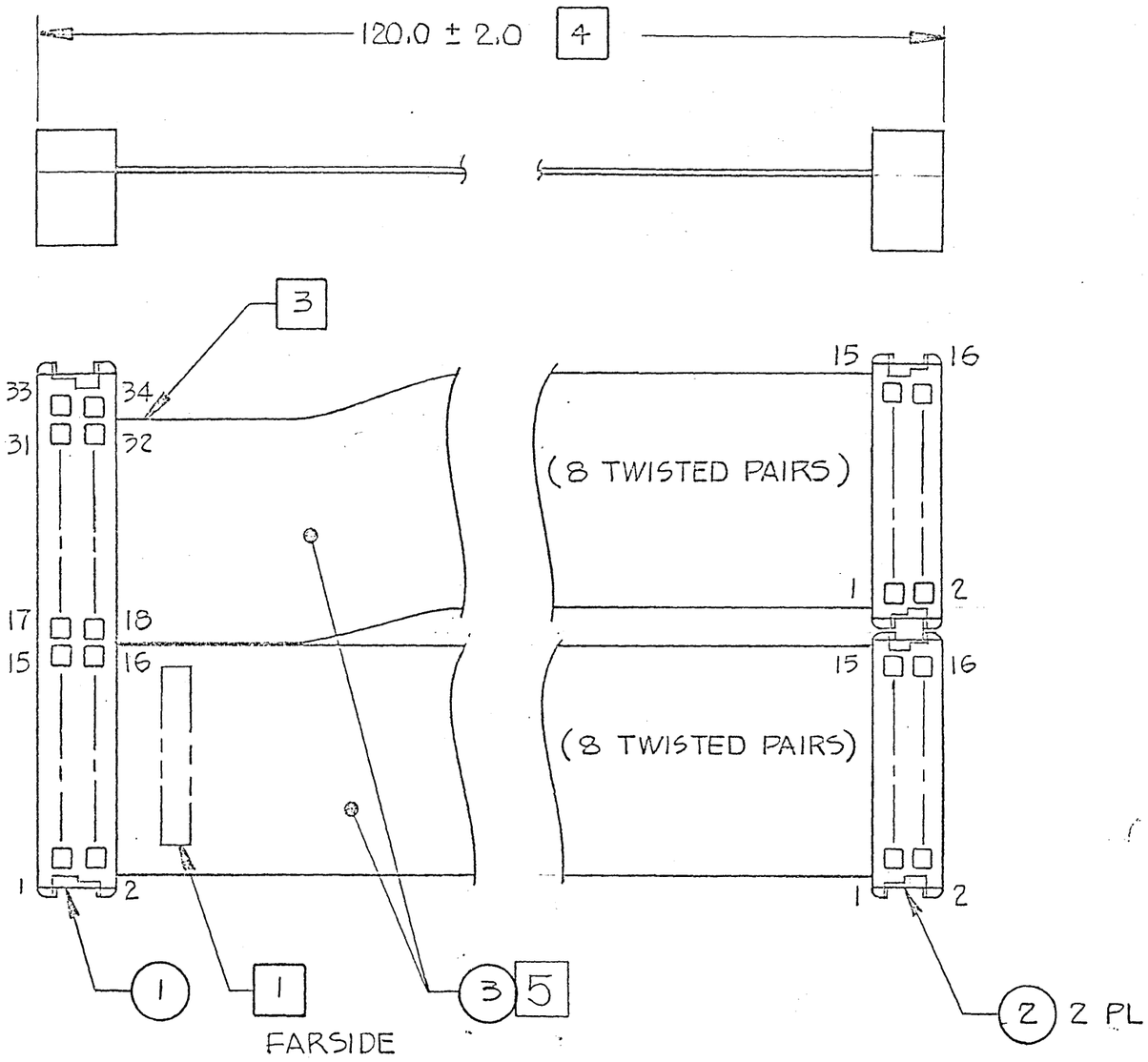
BILL OF MATERIAL

AS OF 02/12/86

0120-0043-01 ASY CBL PROBE TEST TO CLK,K205
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0120-0043	DWG,ASSY,CBL,PRB TST TO CLK BD	0	EA	REF
1	6000-0273-10	CONN 20 PIN SKT	2	EA	
2	7100-0068-10	CBL,FLAT,28 AWG,10PR,TW	3	FT	

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50	4293	PILOT REL PER ECO	RM	DLW	11/21/84
51	4457	REVISED PER ECO Nº	JWC	DLW	12/4/84



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK CABLE WITH ASSY. NO., DASH NO. AND REVISION LEVEL APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK. ALSO STAMP WITH VENDOR I.D.
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.
3. NO CONNECTION TO HEADER ITEM (1) PINS 33 & 34.
4. CONNECTORS MUST BE INSTALLED ON FLAT PORTIONS OF CABLE.
5. CUT CABLE (ITEM 3) INTO TWO TEN FOOT SECTIONS

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

01	0120-0004	3
DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES .XX ± .020 ± 1° .XXX ± .010

HOLE SIZE: .0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

ENG. SERV. | DATE

DRAWN	R Mercer	1/5/84
CHECKED	D L Wright	1/12/84
PROJ. ENG.		
MANUFACTURING		1/10/84
QUALITY ASSUR		1/10/84

GOULD biomation

TITLE ASSEMBLY, CABLE INPUT TO DATA BD.

SCALE	SIZE	PART NUMBER	REV
NONE	B	0120-0044-01	51

CODE K205 SHEET 1 OF 1

BILL OF MATERIAL

AS OF 02/12/86

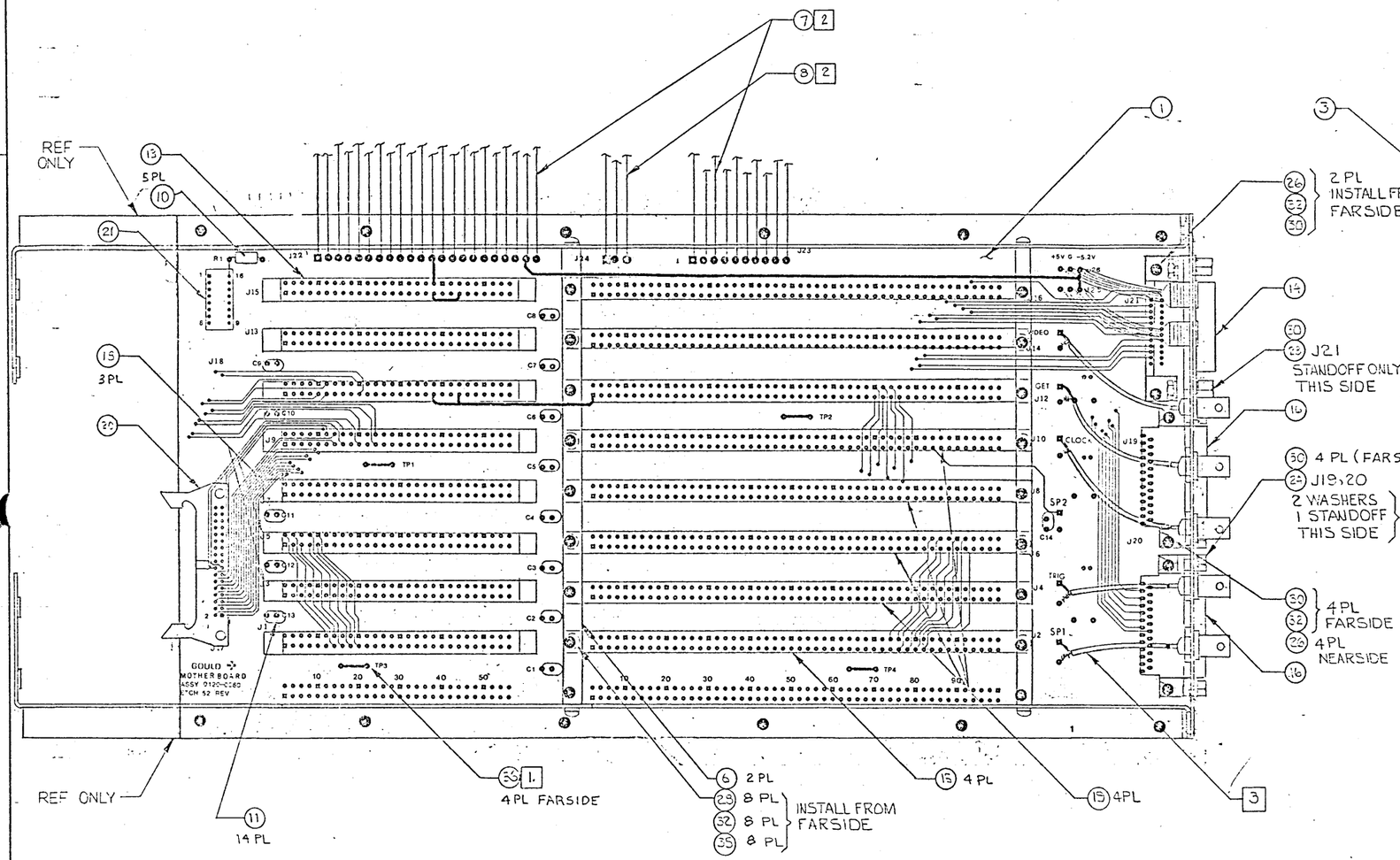
0120-0044-01 ASY CBL INPUT TO DATA BD,K205
MODEL: K205

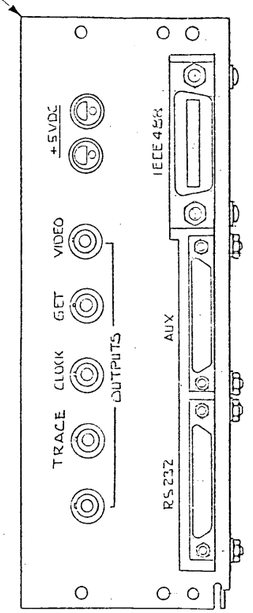
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0120-0044	DWG,ASSY,CBL,INPUT TO DATA BD	0	EA	REF
1	6000-0391-20	CONN 34PIN W/O STRAIN REL	1	EA	
2	6000-0352-20	CONN SKT 16 CONTACT	2	EA	
3	7100-0068-08	SPECTRASTRIP 455-248-16	20	FT	

DWG. NO. 0120-0080	SH 1	REV D

REVISIONS

ZONE	REV.	ECO#	DESCRIPTION	DWN	CHKD	APPD
53		4557		[illegible]	[illegible]	[illegible]
A		4825	REVISED PER ECO #2 12-5-84	SAR	DGW 12-5-84	[illegible]
B		5097	REV'D PER ECO 11/13/85	KTM	DWJ	11/13/85
C		5122	REVISED PER ECO # 2/10/86	DWJ	RTM	2/10/86
D		5221	REVISED PER ECO 3/5/86	RTM	DWJ	3/4/86





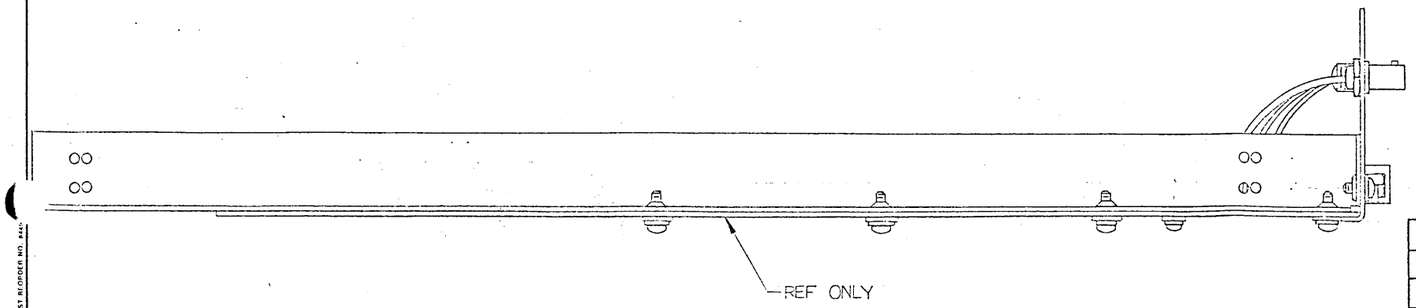
3 TABLE 1

PANEL WIRING

PANEL		MOTHER BD	
(SPARE)	BNC	SP1	3
	SHIELD	SP1	9
TRACE	BNC	TRIG	8
	SHIELD	TRIG	9
CLOCK	BNC	CLOCK	3
	SHIELD	CLOCK	9
GET	BNC	GET	3
	SHIELD	GET	9
VIDEO	BNC	VIDEO	8
	SHIELD	VIDEO	9
LEFT LEMO	GREEN	J25	-5.2V
	BLACK	J25	G
	RED	J25	+5V
RIGHT LEMO	GREEN	J26	-5.2V
	BLACK	J26	G
	RED	J26	+5V

NOTES: UNLESS OTHERWISE SPECIFIED

1. INSTALL GND BUSS WIRE, ITEM 36, ON FARSIDE AT TP1 - 4
2. INSTALL CABLE ON NEARSIDE OF BOARD & SOLDER WIRE TO J22, J23 & J24 PADS.
3. INSTALL LEADS PER TABLE 1.
4. LEFT AND RIGHT RAIL SUPPORTS ARE SHOWN FOR CLARITY AND REPORT TO 0120-0022.



-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					
				PARTS LIST	
10	0120-0022	K205			
DASH NO.	NEXT ASSY	USED ON			
FIRST APPLICATION					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN	1-5-84
CHECKED	3/4/84
PROJ ENG	1-11-85

GOULD Electronics

TITLE: ASSEMBLY — MOTHER BOARD PWB K205

SIZE D | DWG. NO. 0120-0080 | REV. D

SCALE 1/1 | MODEL K205 | SHEET 1 OF 1

DILITRON POST REORDER NO. 8440

BILL OF MATERIAL

AS OF 02/12/86

0120-0080-10 ASSY,PCB,MOTHER,K205
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0120-0080	DWG,ASSY,MOTHER BD,K205	0	EA	REF
0	D0120-0081	DWG,SCHEM,MOTHER PWB,K205	0	EA	REF
1	0120-0082-10	FAB,PCB,MOTHER,K205	1	EA	
3	0120-0092-10	ASSY PNL REAR MTHRBD K205	1	EA	
6	0114-0038-10	SUPPORT BAR MOTHER BOARD	2	EA	
7	0114-2024-10	ASSY,CABLE,PWR SPLY	1	EA	
8	0114-0055-20	ASSY,CBL,INPUT BD PWR	1	EA	
10	3000-1500-10	RES,150K,5%,1/4W,C	1	EA	R1
11	4000-0025-10	CAP,0.1UF,50V,20%,CER	14	EA	C1-14
13	6000-0198-10	CONN DUAL 28 PC	5	EA	15 J1,9,11,13
14	6000-0315-10	CONN 24 PIN RECEPT	1	EA	J21
15	6000-0333-10	CONN 50 PIN DUAL PC	4	EA	16 J2,12,14
16	6000-0353-10	CONN 25 POS. PCB	2	EA	J19,20
18	6000-0369-10	CONN DUAL 28 PIN SEL LOAD	3	EA	J3,5,7
19	6000-0370-10	CONN DUAL 50 PIN SEL LOAD	4	EA	J4,6,8,10
20	6000-0373-10	CONN 34 POS. HDR. RT. ANG	1	EA	J17
21	6100-0120-10	SKT 16 PIN DIP LO-PROFIL	1	EA	J18
23	7000-0399-10	HDWR MTG HDWR FOR GPIB	1	EA	J21
24	7000-0425-10	HDWR KIT, 2 FEMALE SCREWLOCKS	2	EA	J19,20
26	7011-1440-14	SCR,X,PH,4-40 X 7-16,STZN	6	EA	
28	7011-1440-16	SCR,X,PH,4-40 X 1/2,STZN	8	EA	
30	7071-1440-00	NUT,S-LOCK,4-40,STD,STZN	8	EA	
32	7081-1004-00	WSHR,FLAT,#4,STD PAT,STZN	14	EA	
35	7085-1004-00	WSHR,INT TOOTH LOCK,#4,STZN	12	EA	
36	9000-0054-10	BUSS WIRE, FORMED	4	EA	TPI-4

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
C	5122		REVISED PER ECO #	DJW	[illegible]	3/16/84

REVISIONS

DASH NO.	NUMBER	QTY	NEXT ASSEMBLY
	0120-0081		

	DATE
DRAWN	
CHECKED	3/16/84
PROJ. ENG.	1-17-84
MANUFACTURING	
QUALITY ASSUR	
ENG. SERV.	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. MAXIMUM RADIUS OF 0.010 IN. UNLESS OTHERWISE SPECIFIED. COVER AGOLD FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = ±1 XX = ±.05 XXX = ±.010 ANGLES ± .5°

HOLE SIZE: .000-.599 = .003 .600-.999 = .004 1.000-1.499 = .005

ITEM	DESCRIPTION/SPECIFICATION	PART NAME	PART NUMBER
1			

GOULD biomation

TITLE: SCHEMATIC DIAGRAM MOTHERBOARD- K205

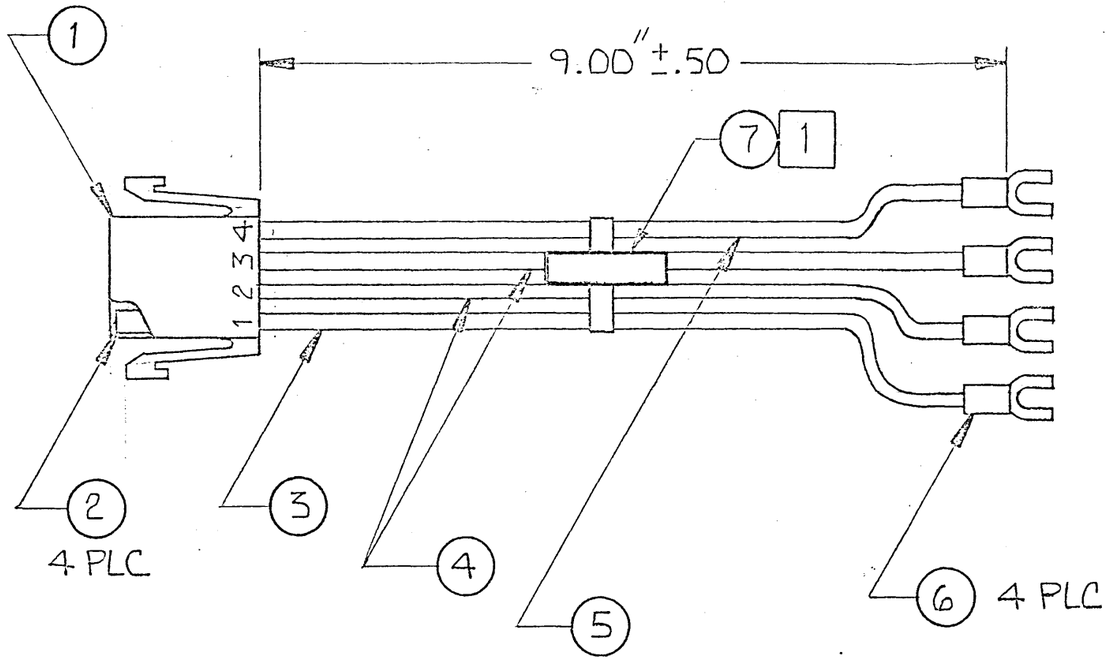
SCALE	SIZE	PART NUMBER	REV
~	D	0120-0081	C D

CODE | SHEET 1 OF 1

NOTES:
1. AGND IS CONNECTED TO GND AT PINSJ22-2,12.
2. ASHIELD IS CONNECTED TO GND AT P/N 7721-14
3. SHIELD IS CONNECTED TO GND BY TRACE TO E2(488), E4(449), E6(232)
4. 488 GND IS CONNECTED TO GND AT J12-95

DWG. NO. 0120-0145 SH 1 REV 51

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50	4604	PROTOTYPE REL	SAR	DGW JMS	7/24/84
51	4800	REVISED PER ECO 12-5-84	SAR	DGW JMS	12/5/24



1 MARK PART NUMBER, DASH NUMBER REV LEVEL AND VENDOR LOGO (IF APPLICABLE)

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-10	0120-0004	1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES .XX ± .020 ± 1° .XXX ± .010

HOLE SIZE: .0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

DRAWN S. Ross	DATE 4-23-84	GOULD
CHECKED [illegible]	7/24/84	TITLE ASSEMBLY, DOS-PWR HARNESS
PROJ. ENG. [illegible]	7/24/84	
MANUFACTURING		SCALE NONE / SIZE B / PART NUMBER 0120-0145 / REV 51
QUALITY ASSUR		CODE / SHEET 1 OF 1
ENG. SERV.	DATE	

KLINGLER K-VEL H

BILL OF MATERIAL

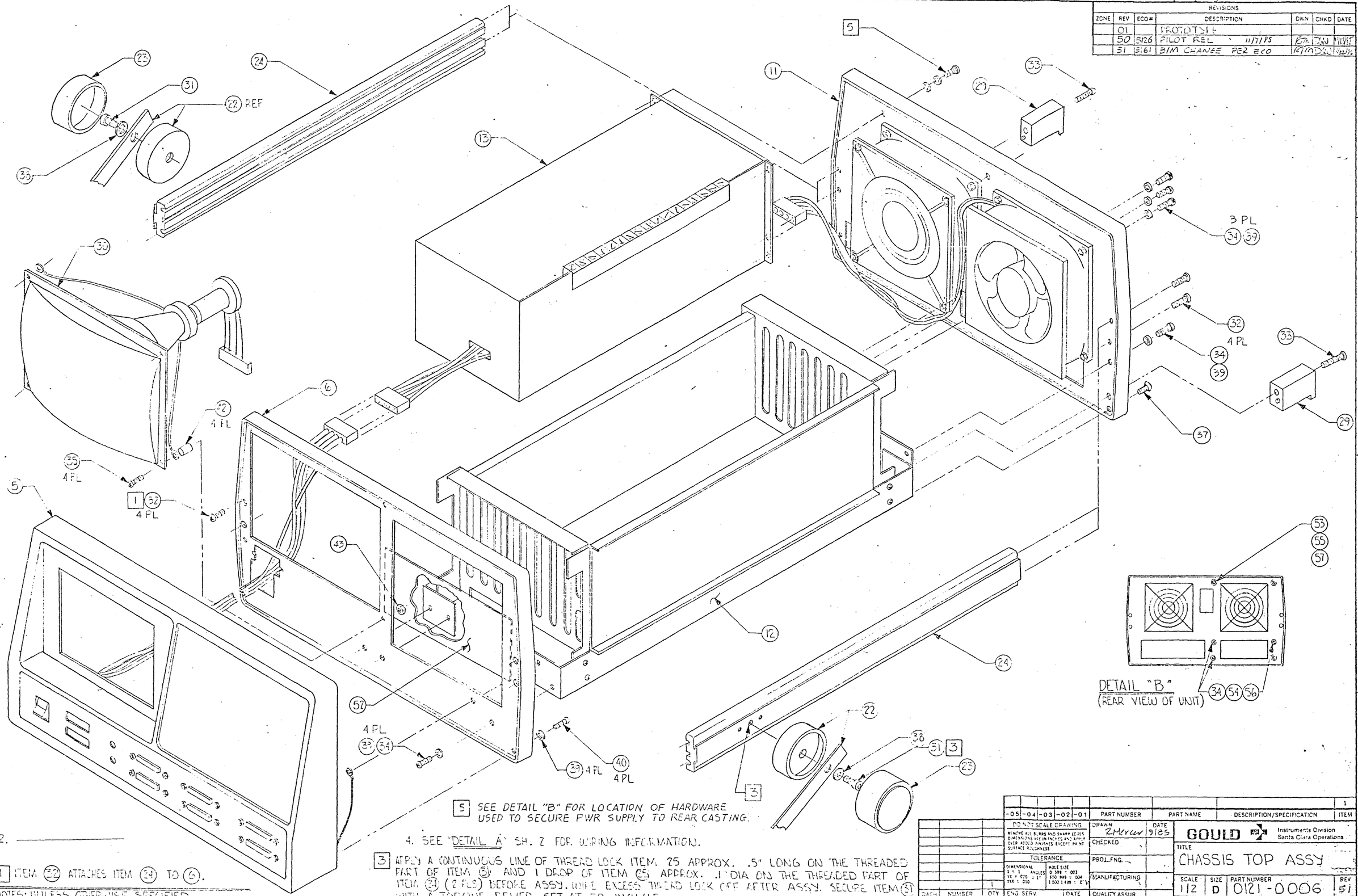
AS OF 02/12/86

0120-0145-10 ASSY,HARNESS,DOS-PWR,K205
MODEL:

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0120-0145	DWG,ASSY,DOS,PWR HARNESS	0	EA	REF
1	6000-0023-10	CONN 4 PIN SKT HOUSING	1	EA	
2	6000-0185-10	CONN SKT 22-18 AWG	4	EA	
3	7150-0018-09	WIRE,PVC,18 AWG,WHT	1	FT	
4	7150-0018-10	WIRE,PVC,18 AWG,BLK	2	FT	
5	7150-0018-02	WIRE,PVC,18 AWG,RED	1	FT	
6	6200-0069-10	TERM LUG SNAP SPADE 22G INSLT	4	EA	
7	7200-0039-10	TIE,MARKER,4"	1	EA	

DWG. NO. 0121-0006 | SH 1 | REV 51

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	01		PROTOTYPE			
	50	5126	PILOT REL 11/7/85	KTA	DJW	11/7/85
	51	5161	B/M CHANGE PER ECO	KTA	DJW	12/2/85



5 SEE DETAIL "B" FOR LOCATION OF HARDWARE USED TO SECURE PWR SUPPLY TO REAR CASTING.

4. SEE "DETAIL A" SH. 2 FOR WIRING INFORMATION.

3 APPLY A CONTINUOUS LINE OF THREAD LOCK ITEM 25 APPROX. .5" LONG ON THE THREADED PART OF ITEM 31 AND 1 DROP OF ITEM 25 APPROX. .1" DIA ON THE THREADED PART OF ITEM 34 (2 PLS) BEFORE ASSY. WIPE EXCESS THREAD LOCK OFF AFTER ASSY. SECURE ITEM 31 WITH A TORQUE DRIVER SET AT 70 INCH/LBS.

2. _____

1 ITEM 32 ATTACHES ITEM 34 TO 6.

NOTES: UNLESS OTHERWISE SPECIFIED

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER MOLD FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± .1 ANGLES ±1°; XX ± .020; XXX ± .010
HOLE SIZE: 0 599 + .003; 600 999 + .004; 1.000 1.499 + .005

DRAWN: Z Mercer DATE: 9/85
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV DATE

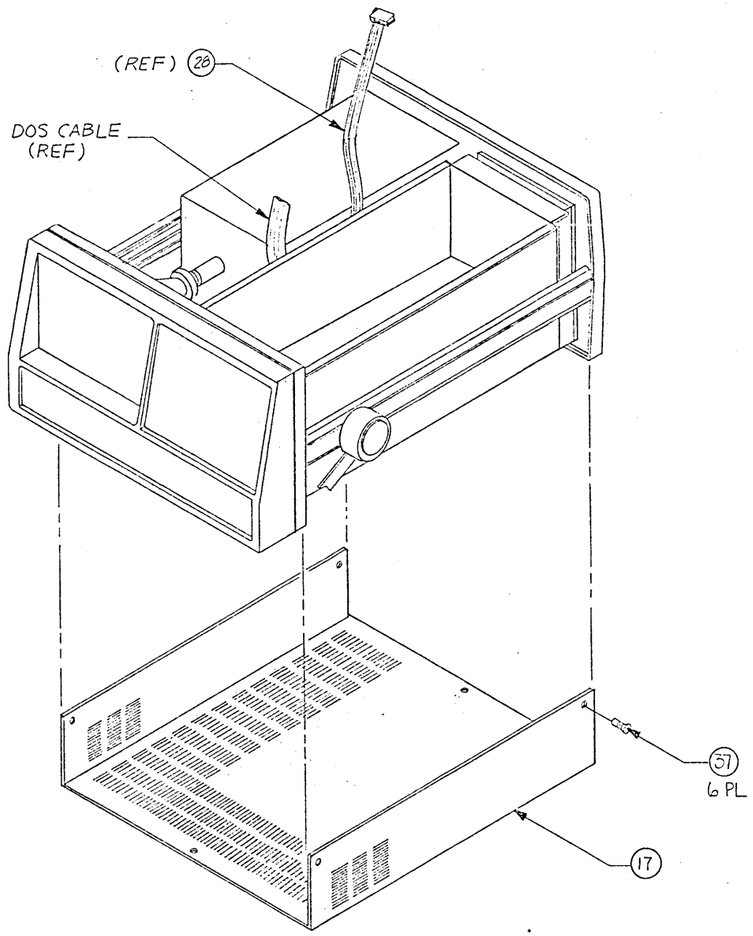
DASH NO | NUMBER | QTY | NEXT ASSEMBLY

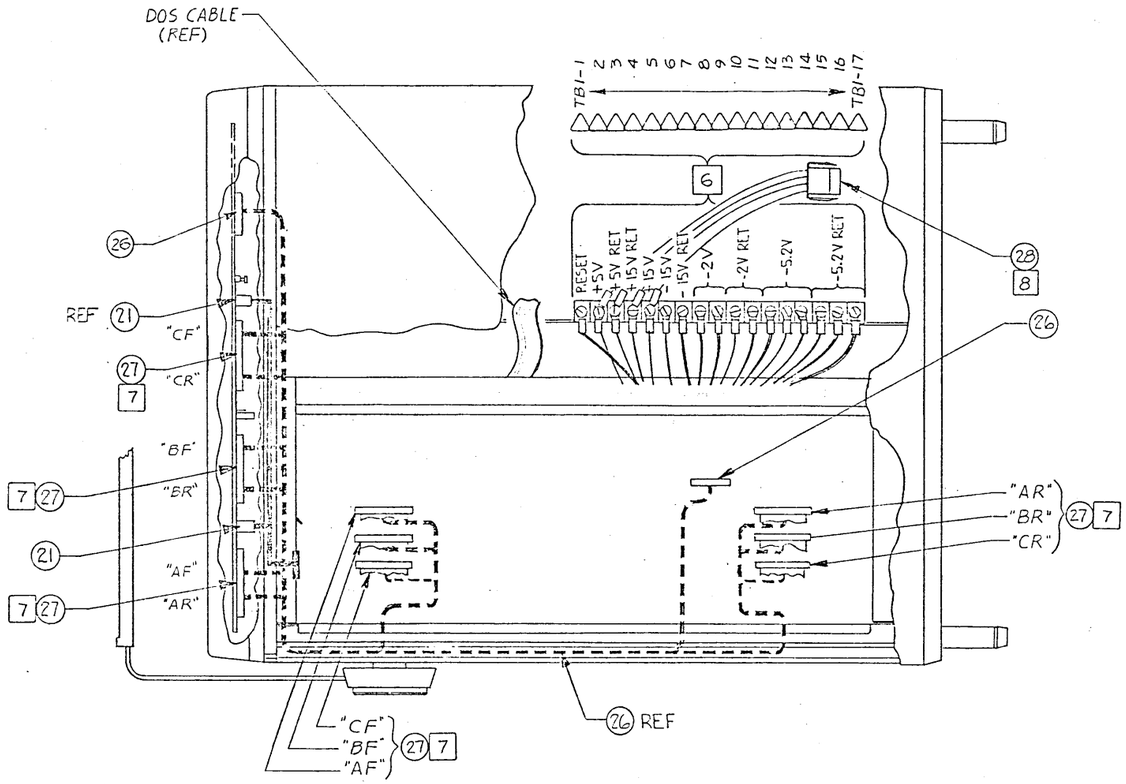
GOULD Instruments Division Santa Clara Operations

TITLE: CHASSIS TOP ASSY

SCALE	SIZE	PART NUMBER	REV
1/2	D	0121-0006	51

MODEL K450 SHEET 1 OF 2





DETAIL "A" WIRING INFORMATION

NOTES: (CONTINUED FROM SHT. 1)

6 NUMBER BESIDE "▷" INDICATES WIRE NO. FROM HARNESS 0114-2024-10 WHICH IS SOLDERED INTO CARD CAGE ITEM (12).

7 NOTATION TO BE USED ON LABELS FOR CABLE ROUTING.

8 WIRING CHART:

ITEM 28	
PIN NO.	TP-
1	5
2	4
3	3
4	2

SIZE D | GOULD | DWG. NO. 0121-0006 | REV. 51 | SHEET 2 OF 2

BILL OF MATERIAL

AS OF 02/12/86

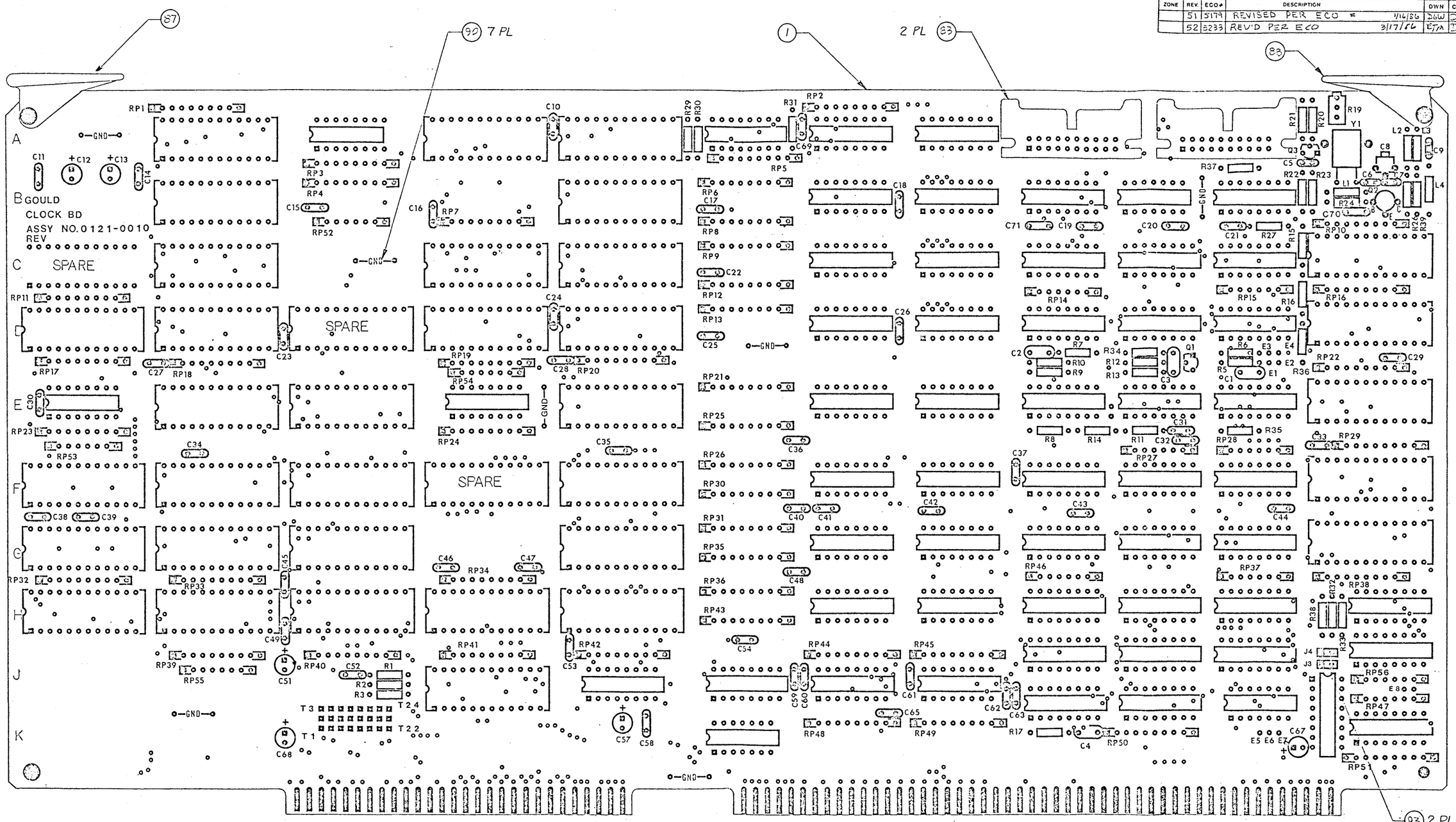
0121-0006-10 ASSY,CHASSIS,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	0114-0039-60	COVER,BOTTOM,4550	1	EA	
0	D0120-0004	DWG,ASSY,CHASSIS,K205	0	EA	REF
4	7000-0334-10	HDWR "U" SPEED NUT FSTNR	6	EA	
5	0121-0007-10	ASSY,FRT BEZEL,K450	1	EA	
6	0120-0023-10	BEZEL FRT,PUNCHED,K205	1	EA	
11	0114-0005-20	ASSY,REAR,CASTING	1	EA	
12	0120-0022-10	ASSY,CARD CAGE,K205	1	EA	
13	9000-0138-10	SPEC. PWR SPLY K101/02/05	1	EA	
21	0120-0042-01	ASSY,CBL,INPUT BD TO MB,K205	1	EA	
22	0111-0016-10	ASSY,HANDLE	1	EA	
24	0285-0117-30	SIDE RAIL,WHT,4500	2	EA	
25	8200-0032-10	ADHESIVE,THREAD LOCK 262	0	EA	
26	0120-0043-01	ASY CBL PROBE TEST TO CLK,K205	1	EA	
27	0120-0044-01	ASY CBL INPUT TO DATA BD,K205	3	EA	
28	0120-0145-10	ASSY,HARNESS,DOS-PWR,K205	1	EA	
29	0950-0099-10	REAR FOOT,K500	4	EA	
30	0117-0123-10	ASSY,CRT,K105	1	EA	
31	7000-0376-10	SCR,HD,CAP,3/4 X 1/4-20	2	EA	
32	7000-0328-10	SCR,PHH,8-32 X 5/8	8	EA	
33	7011-1832-60	SCR,X,PH,8-32 X 1-7/8,STZN	4	EA	
34	7011-1632-16	SCR,X,PH,6-32 X 1/2,STZN	4	EA	
36	7071-1008-00	NUT,KEP,#8,STD,STZN	2	EA	
37	7021-2632-12	SCR,X,FH 100,6-32 X 3/8,SS	6	EA	
38	7094-0001-10	WSHR,SPRG,1/4	2	EA	
39	7085-1006-00	WSHR,INT TOOTH LOCK,#6,STZN	16	EA	
40	7011-1632-12	SCR,X,PH,6-32 X 3/8,STZN	15	EA	
41	7011-1632-24	SCR,X,PH,6-32 X 3/4,STZN	4	EA	
42	7000-0320-10	SPCR,1/8 B,RND	4	EA	
43	7071-1632-00	NUT,S-LOCK,6-32,STD,STZN	5	EA	
52	0112-0308-10	INSULATOR, KEYBOARD	1	EA	
53	7011-1832-12	SCR,X,PH,8-32 X 3/8,STZN	1	EA	
57	7085-1008-00	LOCKWASHER INT. #8	1	EA	

DWG. NO. 0121-0010	SH 1	REV. 52

REVISIONS

ZONE	REV.	ECO#	DESCRIPTION	DWN	CHK'D	APP'D
	51	5179	REVISED PER ECO = 1/16/86	DGW	DGW	[illegible]
	52	3233	REV'D PER ECO 3/17/86	EJM	DGW	[illegible]



-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

GOULD PART NO.

APPROVALS	DATE
DRAWN LTM	6-4-85
CHECKED DG WRIGHT	11/16/86
PROJ ENG	

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD Electronics

TITLE: ASSEMBLY, CLOCK PCB

SIZE	DWG. NO.	REV.
D	0121-0010	52

SCALE 2/1 | MODEL K450 | SHEET 1 OF 1

10		
DASH NO.	NEXT ASSY	USED ON

FIRST APPLICATION

DIETRICH POST REORDER NO.

BILL OF MATERIAL

AS OF 02/12/86

0121-0010-10 ASSY,PCB,CLOCK,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	00121-0010	DWG,ASSY,CLOCK BD. K450	0	EA	
0	D0121-0011	DWG,SCHEM,CLOCK BD. K450	0	EA	
1	0121-0012-10	FAB,PWB,CLOCK BD. K450	1	EA	
3	1400-0019-10	TRAN 2N3906	2	EA	Q1,3
4	3000-1200-10	RES,120,5%,1/4W,C	5	EA	R1-3,34,37
5	1300-0038-10	TRAN BFR-91	1	EA	Q2
7	1800-0105-10	IC 74LS00N 2-IN NAND LOW	1	EA	11K
8	1800-0254-10	IC 74LS85N 4-BIT MAG	1	EA	12L
9	1800-0349-10	IC 74368AN HEX BUS DR	1	EA	9F
10	1800-0280-10	IC 74S37N BUFFER/CLK DR.	1	EA	6K
11	1820-0028-10	IC 4028 1 OF 10 DEC	1	EA	9B
12	1820-0065-10	IC F4069B HEX INVERTER	1	EA	10B
13	1820-0063-10	IC MC14518B DUAL UP CNT	2	EA	9C,9D
15	1850-0077-10	IC F100101DC TPL 5OR/NOR	7	EA	12E 1D,2H,4C 4D,4H,4J
17	6100-0119-10	SKT 14 PIN DIP LO-PROFIL	1	EA	X6K
19	1850-0078-10	IC F100102DC 2IN OR/NOR	25	EA	12D,4A,1F 1G,1H 2A-2G,12C 3E-3H 5A-5H
21	1850-0147-10	IC 10474	2	EA	12F,12G
22	1850-0125-10	IC MC10H116P TPL LINE RCVR	4	EA	1E,4E,3A 6A
23	1850-0097-10	IC MC10231L DUAL D F/F	2	EA	5J,11D
24	1850-0098-10	IC MC10176L HEX D F/F	22	EA	11E,9H,10J 11F 7A-7H,9G 8A-8H,10H
26	1850-0105-10	IC MC10173L QUAD 2-IN	2	EA	10G,11J
27	1850-0099-10	IC MC10164L 8-INPUT MULT	1	EA	10C
28	1850-0100-10	IC MC10161L 1 OF 8 DEC	1	EA	9J
29	1850-0101-10	IC MC10137L DECADE CNTR	2	EA	9E,10E
30	1850-0103-10	IC MC10125L QUAD ECL-TT	1	EA	10F
31	1850-0104-10	IC MC10124L QUAD TTL	5	EA	6J,7J,8J 9K,10K
32	1850-0108-10	IC F10109DC DUAL 4-5 INP	1	EA	10D
33	1850-0113-10	IC MC10101L QUAD OR/GAT	2	EA	11H,11C
34	1850-0114-10	IC F10016DC 4-BIT BIN	1	EA	11B
35	6100-0137-10	SKT 24 PIN DIP LOW PRO	2	EA	X12F,X12G
36	2100-0014-10	IND 1025-94 MOLDED CHOKE	2	EA	L2,L3
37	2100-0012-10	IND 1025-12 FERRITE CORE	1	EA	L1
38	2100-0036-10	IND 2743002121 SHLD BEAD	1	EA	L4
40	2950-5106-10	RES,51,5%,1/8W,C	1	EA	R24
41	3000-1000-10	RES,100,5%,1/4W,C	2	EA	R35,36

BILL OF MATERIAL
AS OF 02/12/86

0121-0010-10 ASSY,PCB,CLOCK,K450
MODEL: K450

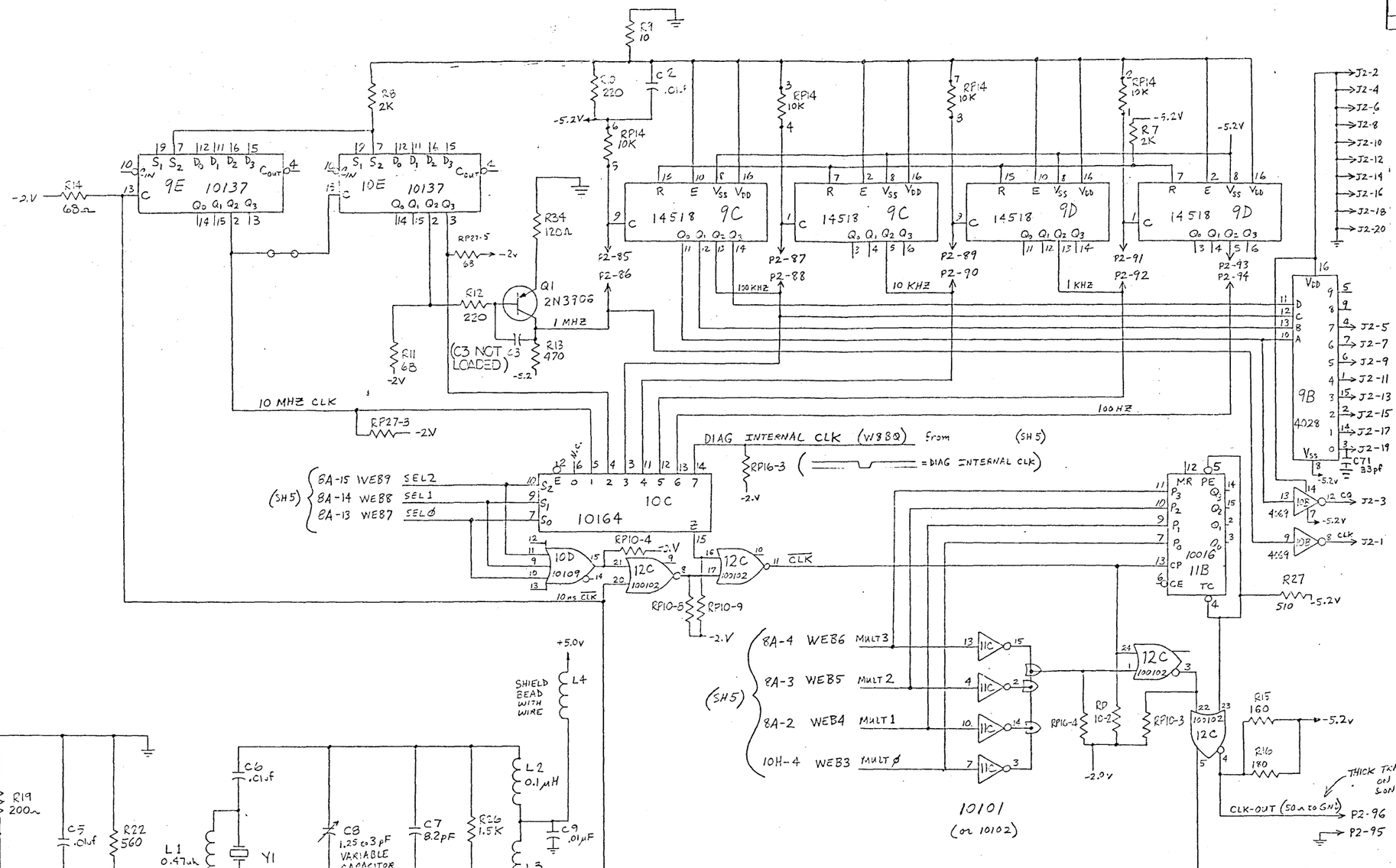
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
42	3000-8200-10	RES,820,5%,1/4W,C	1	EA	R21
43	3000-1006-10	RES,10,5%,1/4W,C	1	EA	R9
44	3000-1501-10	RES,1.5K,5%,1/4W,C	1	EA	R26
45	3000-1600-10	RES,160,5%,1/4W,C	1	EA	R15
46	3000-1800-10	RES,180,5%,1/4W,C	1	EA	R16
48	3000-2001-10	RES,2K,5%,1/4W,C	3	EA	R8,7,32
49	3000-2200-10	RES,220,5%,1/4W,C	4	EA	23 R10,12,20,
51	3000-3006-10	RES,30,5%,1/4W,C	1	EA	R5
52	3000-4700-10	RES,470,5%,1/4W,C	1	EA	R13
53	3000-5100-10	RES,510,5%,1/4W,C	1	EA	R27
54	3000-5600-10	RES,560,5%,1/4W,C	1	EA	R22
55	3000-3001-10	RES,3K,5%,1/4W,C	1	EA	R33
56	3000-6800-10	RES,680,5%,1/4W,C	1	EA	R6
57	3000-6806-10	RES,68,5%,1/4W,C	4	EA	R11,14,17 R38
58	3000-2201-10	RES,2.2K,5%,1/4W,C	3	EA	R29,30,31
59	3300-0067-10	POT,200,0.5W,10% 20T,PC,RTANG	1	EA	R19
60	3700-0051-10	RPAK,10K,0.2W,2%,8/4	1	EA	RP14
61	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	4	EA	RP48-51
62	3700-0057-10	RPAK,2.2K,0.18W,2%,8/7	4	EA	54 RP47,52,53
63	3700-0039-10	RPAK,56,0.18W,2%,10/9	4	EA	24 RP3,5,23
64	3700-0091-10	RPAK,68,0.2W,2%,8/7	6	EA	37,46,56 RP15,27,28
66	3700-0092-10	RPAK,68,0.2W,2%,10/9	36	EA	16-22,26 29-36 38-45 6-13,25 RP1,2,4
68	5100-0004-10	XTAL 100MHZ .39UH	1	EA	Y1
69	3700-0096-10	RPAK,100,0.2W,2%,8/7	1	EA	RP55
70	4010-0330-10	CAP,33PF,50/100V,5%,CER	2	EA	C70,71
71	4010-0680-10	CAP 68PF,50/100V /10% .1	1	EA	C1
73	4010-5606-10	CAP,5.6PF,100V,5%,CER	1	EA	C7
76	4010-0103-10	CAP,0.01UF,50V,10%,CER	54	EA	52-54 58-63,65 69 9-11,14-49 C2,4-6
79	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	6	EA	57,67,68 C12,13,51
80	4600-0009-10	CAP 1.2-3PF,100V	1	EA	C8
81	6000-0571-10	CONN SHORTING PLUG	10	EA	T1-T2 T10-T11

BILL OF MATERIAL
AS OF 02/12/86

0121-0010-10 ASSY,PCB,CLOCK,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
81	6000-0571-10	CONN SHORTING PLUG	10	EA	T13-T14 T16-T17 T19-T20 T22-T23 T4-T5 T7-T8 XJ3,XJ4
83	6000-0384-10	CONN 20 POS RT ANGLE HDR	2	EA	J1,2
84	6000-0293-08	CONN 8 POS HDR ST SGL ROW	3	EA	3K(3)
87	0112-0228-05	CARD EJECTOR-HOT STAMPED (A5)	1	EA	A5
88	7000-0120-10	CARD EJECTOR NYLON 6/6	1	EA	
90	9000-0054-10	BUSS WIRE, FORMED	7	EA	
91	1850-0131-10	IC MC10H016L B/N COUNTER	3	EA	11G,12H 12J
92	1850-0124-10	IC 10H105 TRIPLE 2-3-2 OR/NOR	1	EA	12K
93	6000-0293-02	CONN 2 POS HDR ST SGL ROW	2	EA	J3,J4

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	51	5179	REVISED PER ECO #	DLW	DLW	1/14/86
	52	5233	ADD R39 PER ECO 3/14/86	RTM	DLW	3/31/86



NOTES:

2. ALL DISCRETE RESISTORS 1/4 W, 5% UNLESS OTHERWISE NOTED.

1. MPU GENERATED DIAGNOSTIC INTERNAL CLOCK PRODUCES A SHORT LOW PERIOD CLK PULSE, OF THE SAME DURATION AS $\overline{WR}$ BUS PULSE. THE SAME IS TRUE OF THE DIAGNOSTIC LATCH CLOCK.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X = .1 ANGLES; .XX = .020 = 1°; .XXX = .010
HOLE SIZE: .0-.599 = .003; .600-.999 = .004; 1.000-1.499 = .005

DRAWN | DATE | CHECKED | PROJ. ENG. | MANUFACTURING | QUALITY ASSUR | ENG. SERV. | DATE

DASH NO. | NUMBER | QTY | NEXT ASSEMELY

GOULD biomation

TITLE: SCHEMATIC, CLOCK (WITH. LEVEL MEMORY)

SCALE	SIZE	PART NUMBER	REV
	D	0121-0011	52

CODE K4507 SHEET 1 OF 5

REVISIONS						
ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE

-2.1 RP3 5.6Ω 10H116 -5.2V RP52- 2.2K

P1-18 CS
P1-17 CS
BS
T5 EB
T11 EB
P1-2 AB
P1-1 AB

(SH 5)
EB-15 WC39
EB-14 WC38
EB-13 WC37
EB-4 WC36
EB-3 WC35
EB-2 WC34

100102 2B 2B 2B 2B 2B 2A

100101 1D

RP11- -2.V

LATCH CLK DISQUALIFY RP17-5 -2.V
MID-SOURCED RP18-5 -2.V

(SH 5)
EC-15 WAB9
EC-14 WAB8
EC-13 WAB7
EC-4 WAB6
EC-3 WAB5
EC-2 WAB4

100102 2C 2C 2C 2C 2C 2A

100101 1D

RP11- -2.V

MID-SOURCED RP32-5 -2.V
RP39-7 -2.V

(SH 5)
ED-15 WRB9
ED-14 WRB8
ED-13 WRB7
ED-4 WRB6
ED-3 WRB5
ED-2 WRB4

100102 2D 2D 2D 2D 2D 2A

100101 1D

RP17- -2.V
RP11-2 -2.V -2.V

MID-SOURCED RP32-6 -2.V
RP33-6 -2.V

RP18- 68Ω -2.V
RF1-1 -2.V

P1-22 CR
P1-21 CR
SH2 T17 BR
T25 BR
-6 AR
-5 AR

RP23 5.6Ω 10H116 -5.2V RP53- 2.2K

RP32-2 RP32-3 -2.V
RP32-8 RP32-10 68Ω
RP33-3 RP33-4 -2.V
RP32-4 -2.V

(SH 5) DIAG LATCH CLK (W381)
EE-15 W689
EE-14 W688
EE-13 W687
EE-4 W686
EE-3 W685
EE-2 W684
EH-14 (SH 5) W658

(SH 5)
EF-15 W489
EF-14 W488
EF-13 W487
EF-4 W486
EF-3 W485
EF-2 W484

(SH 5)
EG-15 W289
EG-14 W288
EG-13 W287
EG-4 W286
EG-3 W285
EG-2 W284

RP18-9 W631 9H-4 (SH 5) -2.V
RP23-9 W632 9H-3 (SH 5) -2.V
W653 9H-13 (SH 5) RP32-9 -2.V

100102 1F 1F 1F 1F 1F 2E 2E 2E
100102 1G 1G 1G 1G 1G 2F 2F 2F
100102 1H 1H 1H 1H 1H 2G 2G 2G

100101 2H 2H 2H

RP33 RP39-10 -2.V
RP39 RP55-6* RP33-5 -2.V
RP39-3 RP33-1 RP55-2* RP39-8 RP33-2 -2.V

RP55-8* -2.V
RP55-7* -2.V
RP55-4* -2.V

LATCH ENABLE A (+2") → P1-44, P1-43
LATCH ENABLE B (+1") → P1-38, P1-37
LATCH ENABLE C (+0") → P1-32, P1-31

NOTE: LATCH ENABLE = $\overline{\text{LATCH CLOCK}}$

*NOTE: RP55 IS 100Ω R-PAK

3
P1-20 T1 T2 T3 CK 6A-5 (SH 3)
P1-10 T4 T5 T6 BS 3A-10 (SH 2)
P1-19 T7 T8 T9 $\overline{CK}$ 6A-4 (SH 3)
P1-9 T10 T11 T12 $\overline{BS}$ 3A-9 (SH 2)
P1-24 T13 T14 T15 CJ 4E-5 (SH 3)
P1-14 T16 T17 T18 BR 1E-10 (SH 2)
P1-23 T19 T20 T21 $\overline{CJ}$ 4E-4 (SH 3)
P1-13 T22 T23 T24 $\overline{BR}$ 1E-9 (SH 2)

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X = .1, XX = .020, XXX = .010
HOLE SIZE: 0-.599 = .003; .600-.999 = .004; 1.000-1.499 = .005

ENGR. SERV. DATE

DRAWN	Chris Fitzhenry	DATE 4-13-81
CHECKED		
PROJ. ENG.		
MANUFACTURING		
QUALITY ASSUR		

GOULD biomation

TITLE SCHEMATIC CLOCK (WITH LEVEL MEMORY)

SCALE	SIZE	PART NUMBER	REV
	D	0121-0011	52

CODE SHEET 2 OF 5

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

-2.V 56Ω RP3 10H116 R31, 2.2K -5.2V R30, 2.2K R29, 2.2K

SH2 T2 CK, T8 CK; -12 BK, -11 BK; P1-4 AK, P1-3 AK

(SH5) 7A-15 WEB15, 7A-14 WEB14, 7A-13 WEB13, 7A-4 WEB12, 7A-3 WEB11, 7A-2 WEB10

(SH5) 7B-15 WCB15, 7B-14 WCB14, 7B-13 WCB13, 7B-4 WCB12, 7B-3 WCB11, 7B-2 WCB10

(SH5) 7C-15 WAB15, 7C-14 WAB14, 7C-13 WAB13, 7C-4 WAB12, 7C-3 WAB11, 7C-2 WAB10

(SH5) 7D-15 WBB15, 7D-14 WBB14, 7D-13 WBB13, 7D-4 WBB12, 7D-3 WBB11, 7D-2 WBB10

100102 5A 5A 5A 5A 5A 4A; 100102 5B 5B 5B 5B 5B 4A; 100102 5C 5C 5C 5C 5C 4A; 100102 5D 5D 5D 5D 5D 4A

RP7- -2.0V; RP7- -2.0V; RP19- -2.0V; RP19- -2.V

100101 4C; 4C; 4D; 4D

RP10-5 -2.0V, RP15-9 -2V; RP42-4 -2.0V, RP40-7 -2V; RP42-5 -2.0V, RP40-6 -2V; RP42-6 -2.V, RP10-5 -2V

MID-SOURCED STRING

FORCE DISQUALIFY WEB2 10H-14 (SH 5)

-2.V 56Ω RP24 10H116 RP54- 2.2K -5.2V

SH2 T14 CJ, T20 CJ; P1-16 BJ, P1-15 BJ; P1-8 AJ, P1-7 AJ

12C-13 (SH 1) 100 MHZ CLK

12C-5 (SH 1) INT CLK

RP20- -2.V; RP7-6 -2.V

(SH 5) 9G-4 WCB1, 7E-15 WG815, 7E-14 WG814, 7E-13 WG813, 7E-4 WG812, 7E-3 WG811, 7E-2 WG810, 8H-13 WØB7

(SH5) 9G-3 WCB2, 7F-15 WA815, 7F-14 WA814, 7F-13 WA813, 7F-4 WA812, 7F-3 WA811, 7F-2 WA810, 34-4 WØB6, 10J-13 WAB1

(SH5) 9G-13 WCB3, 7G-15 WB815, 7G-14 WB814, 7G-13 WB813, 7G-4 WB812, 7G-3 WB811, 7G-2 WB810, 8H-3 WØB5, 10J-14 WAB2

(SH5) 7H-15 WØ815, 7H-14 WØ814, 7H-13 WØ813, 7H-4 WØ812, 7H-3 WØ811, 7H-2 WØ810, 8H-2 WØB4, 10J-4 WAB3

WABØ 10J-2

3E 3E 3E 3E 3E; 5E 5E 5E 5E; 3F 3F 3F 3F 3F; 5F 5F 5F 5F; 3G 3G 3G 3G 3G; 5G 5G 5G 5G; 3H 3H 3H 3H 3H; 5H 5H 5H

RP41- -2V; RP43-4 -2V; RP40-9 -2V

4H; 4H; 4J; 4J

RP41-2, RP54-9, RP54-10, RP54-5, RP54-7

RP54-6, RP54-4, RP54-5, RP54-3, RP54-2

RP43-3, RP41-9, RP41-10, RP41-8, RP41-7

R2 120 -2V; R1 120 -2V; R3 120 -2

SAMPLE CLOCK A (+3") → P1-42, P1-41

SAMPLE CLOCK B (+2") → P1-36, P1-35

SAMPLE CLOCK C (+1") → P1-30, P1-29

CONTROL CLK A → P1-46, P1-45

CONTROL CLK B → P1-40, P1-39

CONTROL CLK C → P1-34, P1-33

ASYNCH FORCE ENABLE CONTROL CLK WEB1 (SH 5)

SYNCH INHIBIT CONTROL CLK WEB0 (SH 5)

INHIBIT CONTROL CLK

CONTROL CLK (SH 4)

CONTROL CLK → P1-28, P1-27 (to CONTROL BOARD)

CONTROL CLK EN STATUS 10A-10 (SH 5)

RP43-2 -2.V; RP42-9 -2.V; RP41-3 -2.V

CP C D 10231 R 5J S Q Q; CP C D 10231 R 5J S Q Q

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

GO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = .1, XX = .020 = 1°, XXX = .010

HOLE SIZE: 0-.599 +.003; .600-.999 +.004; 1.000-1.499 +.005

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

ENG. APPV. | DATE

DRAWN Curt Fothman DATE 4-10-91

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE SCHEMATIC CLOCK (WITH LEVEL MEMORY)

SCALE	SIZE	PART NUMBER	REV
	D	0121-0011	52

CODE SHEET 3 OF 5

DWG. NO. 0121-0011 | SH 4 | REV 52

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

J1-19 LEVEL LØ — RP22-2
J1-17 LEVEL L1 — RP22-4
J1-15 LEVEL L2 — RP22-5
J1-13 LEVEL L3 — RP22-7
J1-9 ARMED — R35 100 → -2
J1-11 -2V — 120 R37
J1-7
J1-3 TRACED — RP16-7
(SH 5) 2H-15 MIX FORCE READ RAMS WØB9

10176 11E — 10176 11F — 11J 10173
RP28-5 RP28-7 RP28-8 RP28-6 — RP56-4
RP56-7 RP56-5 RP56-8 RP56-6
RP38-6 RP38-4 RP38-5 RP38-7
RP22-10
SELECT

12D 100102 — RP28-4
12E 100101 — RP28-3 — 3½" ≈ 0.5ns OR MORE
12E 100101 — RP38-10 — RP16-8
12E 100101 — RP38-8 — RP16-9
RP28-2 -2

10109 10D
10231 11D — RP29-2 — RP38-3
12D 100102 — RP22-6
2" ≈ 0.3 ns OR MORE (LAST ON TRACE)

12F 10474 A — MLØ ML1 ML2 ML3
12G 10474 A — MLØ ML1 ML2 ML3 — TO 10G (10173) (SH 5)

(SH 5) CONTROL CLK — RP16-5
J1-5
J1-1 CABLE CONTROL CLOCK — RP22-8 — E2 E4 E1 E3 — RP16-2 — RP22-9
J1-2 -4 -6 -8 -10 -12 -14 -16 -18 J1-20
RP10-7 -2
12D 100102 — 10231 11D — R36 100 -2 — R5 30 — R6 680 -5.2V — C1 68 pf — RP22-3
≈10ns HIGH PULSE WIDTH WHEN "FORCE READ RAMS" BIT IS LOW.

11G 10H016 — RP29-8 RP29-7 RP29-5 RP29-6
12K 10H105 — RP38 -2 -2V
R32 2K
RP38-9
12H 10H016 — RP29-3 RP29-10 RP29-4 RP29-9
R33 3K -2V
R38 68 -2V
J3 J4

12J 10H016 — RP56-2 RP56-3

5:C/2 WC8Ø LEVEL MEMORY ADDRESS RESET

$\approx \frac{4v}{\approx 700\Omega} \approx 6ma$

$I = C\frac{dv}{dt}$ $\Delta V = \frac{1}{2}V$, $\Delta T = 6ns$ @ $V_{DD} = V_{TH}$

$6\times10^{-3} = (X\cdot10^{-12})\cdot(1/2)\div(3\times10^{-9})$

$X(pF) = 6\times10^{3}\times10^{+12}\times6\times10^{-9}\times2$

$X(pF) = 72$ {for 6ns} ⇒ USE 68pF

NOTE: WHEN READING RAMS WITH "FORCE READ RAMS" HIGH, TWO CLOCKS ARE REQUIRED FOR EACH READ.

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

ENG. SERV. | DATE | QUALITY ASSUR

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING — REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE — DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010 — HOLE SIZE: 0-.339 ± .003; .500-.999 ± .004; 1.000-1.499 ± .005

DRAWN Thomas E. DATE 4-10-91
CHECKED
PROJ. ENG.
MANUFACTURING

GOULD biomation

TITLE SCHEMATIC CLOCK (WITH LEVEL MEMORY)

SCALE | SIZE D | PART NUMBER 0121-0011 | 52

CODE K-150 | SHEET 4 OF 5

KLINGLER REVEL H

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

REVISIONS

DIAG LATCH CLK (WE8:) TO 1F-20 (SH 2: 7/E)

DIAG INTERNAL CLK (WE8:) (SH 1: 5/C)

(---- LATCH CLK IS LOW MOST OF THE TIME, TO PASS INFORMATION TRANSPARENTLY)

RP37-4

RP37-7

RP43-6

RP43-4

MID-SOURCED

MY ADDRESS → 2D 3/B

BWR

BA3

BA2

BA1

ERD → TO 3/B

BA1 → TO 3/D

M/IO

TO PAGE

LD-8 = WB-BWR

R17 68 -2V

C4 .01uf

+5V

-5V

-2V

RP2 RP15 RP4 RP9 RP8 RP13 RP12 RP21 RP25 RP6 RP26 RP50 RP31 RP35 RP43 RP45 RP44 RP47 2.2K

RP48 RP49 RP50 RP51 3K/6.2K

7J 6J 8J 10K 9K 9J 10161 11K 74LS22 12L 74LS05 6K $37

7A 8A 7B 8B 7C 8C 7D 8D 7E 8E 7F 8F 7G 8G 7H 8H 10176

10H 10G 9G 10J 9H 9F 74368A 10F 10125

MID-SOURCED

CONTROL CLK EN STATUS

MY ADDRESS

TO 6/C

TO 6/A

TO 5/B

TO 7/D

DWG. NO.	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
				1

DO NOT SCALE DRAWING — REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE — DIMENSIONAL: X ± .1 ANGLES; XX ± .020 = 1°; XXX ± .010; HOLE SIZE: .0-.599 = .003, .600-.999 = .004, 1.000-1.499 = .006

DRAWN Chatham 7-15-91 | CHECKED | PROJ. ENG. | MANUFACTURING | QUALITY ASSUR | ENG. SERV. | DATE

DASH NO. | NUMBER | NEXT ASSEMBLY | QTY

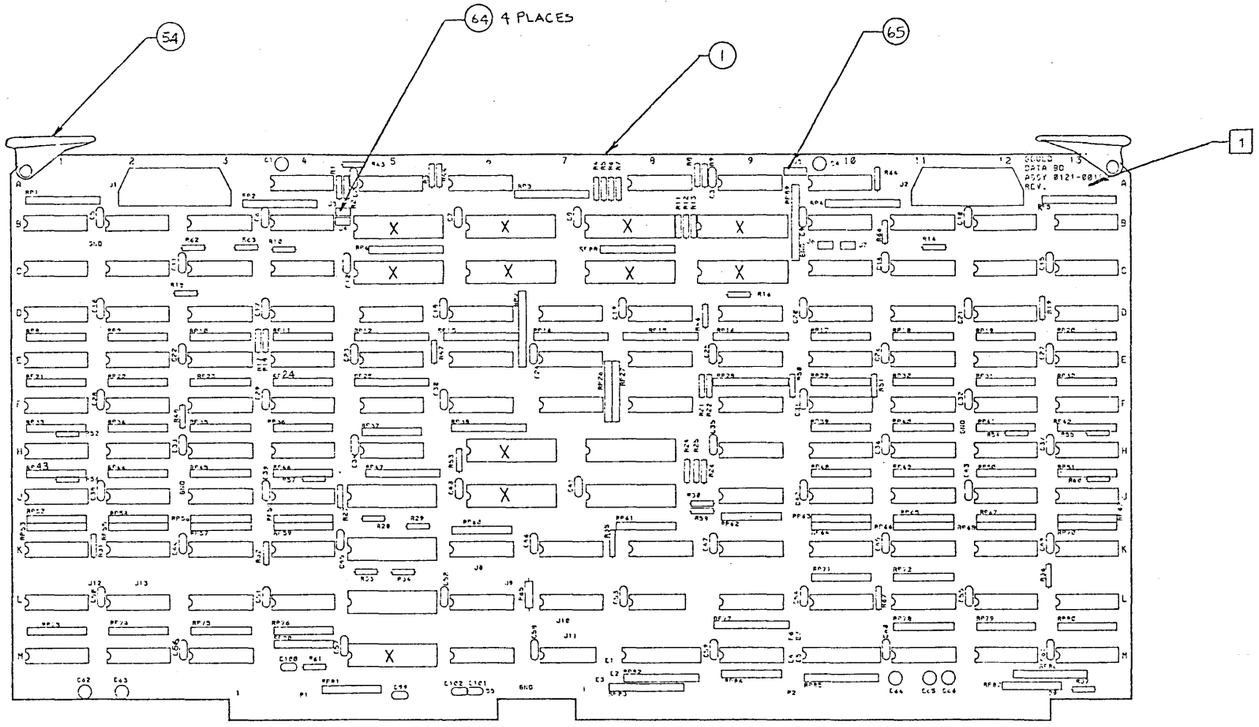
GOULD biomation

TITLE SCHEMATIC CLOCK WITH LEVEL MEMORY

SCALE | SIZE D | PART NUMBER 0121-0011. | REV 52

CODE | SHEET 5 OF 5

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	51	51781	REVISED PER ECO N2 1/30/86	AppCad	DLW	4/3/86



NOTES: UNLESS OTHERWISE SPECIFIED
1. MASK ASSY.DASH NO. REV. LEVEL & SERIAL NO. APPROX. WHERE SHOWN USING CONTRASTING INDELIBLE INK.
2. ASSY.REFLECTS SCHEM DWG 0121-0016 & FAB DWG 0121-0017.
3. MANUFACTURE PER GOULD WORKMANSHIP STD. 87000012.

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

-10	K450-XXX	K450
DASH NO.	NEXT ASSY	USED ON
FIRST APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL N/A

FINISH N/A

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN APPLICAD	1/30/86
CHECKED DLWeigart	2/3/86
PROJ ENG	

GOULD Electronics

TITLE: ASSY, DATA PCB

SIZE D | DWG. NO. 0121-0015 | REV. 51

SCALE | MODEL K450 | SHEET 1 OF 1

EXTERNAL POST INFORMATION NO. 4

BILL OF MATERIAL

AS OF 02/12/86

0121-0015-10 ASSY,PCB,DATA,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0121-0015	DWG,ASSY,PCB,DATA,K450	0	EA	
0	D0121-0016	DWG,SCHEM,DATA,BD.K450	0	EA	
1	0121-0017-10	FAB,PCB,DATA,K450	1	EA	
4	1800-0280-10	IC 74S37N BUFFER/CLK DR.	1	EA	8L
5	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	2	EA	8M,10M
6	1800-0123-10	IC 74LS14N HEX SCHMITT	1	EA	7M
7	1800-0290-10	IC 74S85N 4-BIT MAG COMP	1	EA	9M
10	1850-0131-10	IC MC10H016L B/N COUNTER	6	EA	4A,5A,6A 8A,9A,10A
11	1850-0140-10	IC 10H106 TPL 4-3-3 INP	16	EA	10E-13E 10F-13F 1E-4E 1F-4F
13	1850-0022-10	IC MC10107L TPL 2-IN EXC	1	EA	4K
14	1850-0030-10	IC MC10121P/L 4-W OR AND	16	EA	10C-13C 10D-13D 1C-4C 1D-4D
14	1850-0133-10	IC MC10H121P/L	16	EA	10C-13C 10D-13D 1C-4C 1D-4D
16	1850-0104-10	IC MC10124L QUAD TTL	5	EA	10L,6M 8K,9K,7L
18	1850-0103-10	IC MC10125L QUAD ECL-TT	4	EA	1M-3M,11M
19	1850-0146-10	IC 10H130 DUAL D LATCH	8	EA	10H-13H 1H-4H
20	1850-0100-10	IC MC10161L 1 OF 8 DEC	1	EA	7K
21	1850-0105-10	IC MC10173L QUAD 2-IN	6	EA	12M,13M,9D 5D,5E,9E
23	1850-0090-10	IC MC10174L DUAL 4 TO 1	8	EA	11L,12L 13L 1L-4L,10K
24	1850-0098-10	IC MC10176L HEX D F/F	20	EA	11K,12K,5F 13K 5H,9F,6F 6E,6D,7E 7D,1K-3K 7F,8E,8F 9H,9L,8D
27	1850-0119-10	IC MC10H131P/L DUAL D F/F	8	EA	10J-13J 1J-4J
28	1850-0094-10	IC MC10216L TPL DIFF	8	EA	10B-13B 1B-4B
28	1850-0125-10	IC MC10H116P TPL LINE RCVR	8	EA	10B-13B 1B-4B

BILL OF MATERIAL
AS OF 02/12/86

0121-0015-10 ASSY,PCB,DATA,K450
MODEL: K450

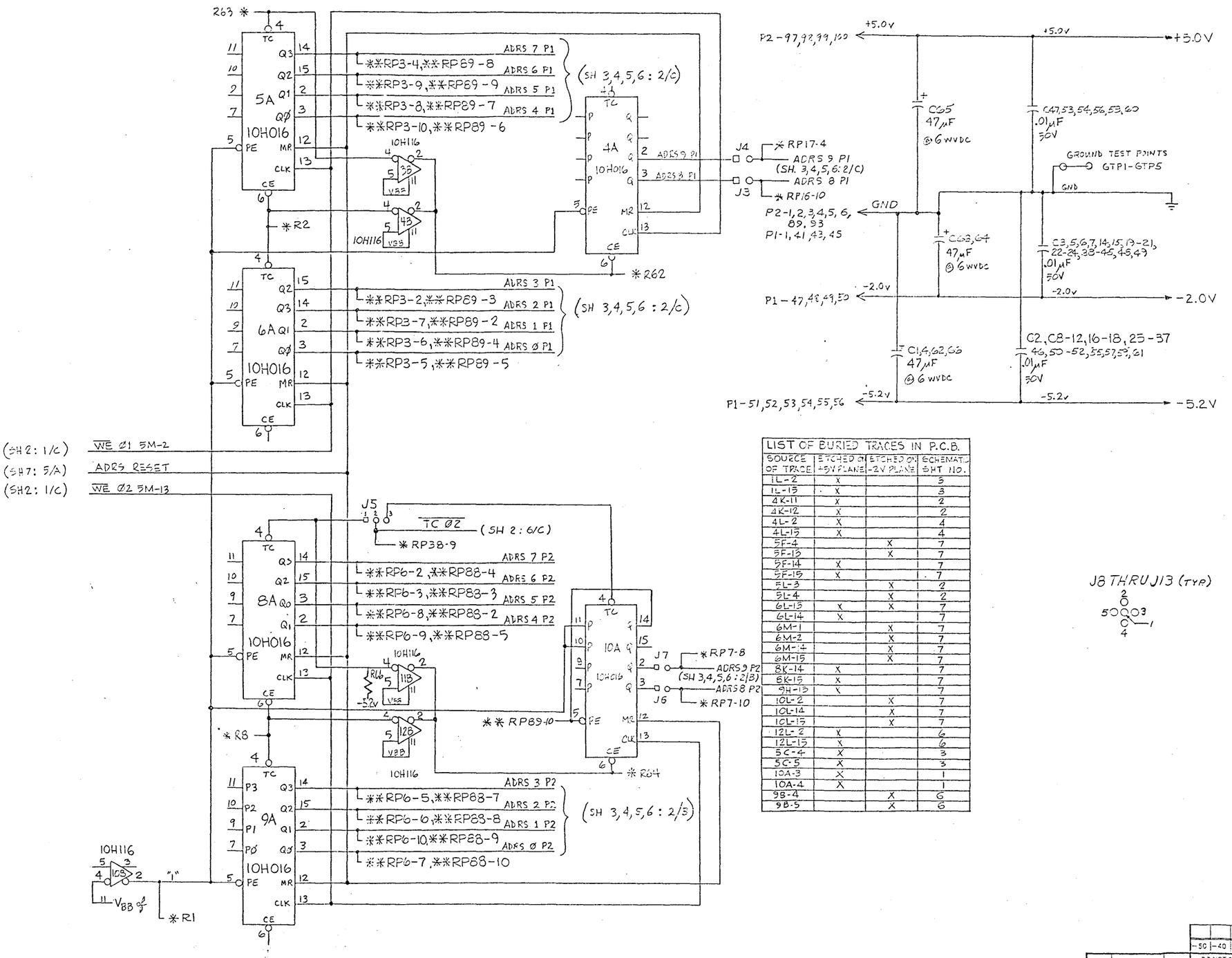
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
29	1850-0145-10	IC 10H210 3-IN 3-OUT OR	1	EA	6L
30	1850-0124-10	IC 10H105 TRIPLE 2-3-2 OR/NOR	1	EA	6K
31	1850-0077-10	IC F100101DC TPL 5OR/NOR	3	EA	8H,5J,5K
32	1850-0078-10	IC F100102DC 2IN OR/NOR	4	EA	5M 6J,8J,5L
33	1850-0091-10	IC F100155DC QUAD MUX	1	EA	6H
35	1850-0147-10	IC 10474	8	EA	5B,6B,8B 8C,9C 9B,5C,6C
37	3700-0060-10	RPAK 50 OHM, .18W, 2% 10P	4	EA	RP1,2,4,5
39	3700-0094-10	RPAK 75 OHM .18W 2% 10 P	11	EA	25,28,38 47,86 RP7,12-16
41	3700-0080-10	RPAK,100,0.3W,2%,10/9	4	EA	RP6 RP88,89,3
42	3700-0044-10	RPAK 220 OHM,0.3W,2% 8 P	8	EA	58,63,65 67,69 RP52,54,56
43	3700-0016-10	RPAK,1K,1/8W,2%,8/7	8	EA	59,64,66 68,70 RP53,55,57
44	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	4	EA	RP77,82,83 RP85
45	3700-0057-10	RPAK,2.2K,0.18W,2%,8/7	1	EA	RP84
46	3700-0047-10	RPAK 75OHM,.18W,2% 8 P	50	EA	17-24,27 29-37,87 39-46 48-51 60-62 71-76 78-81 90 RP8-11,26
48	4010-0103-10	CAP,0.01UF,50V,10%,CER	58	EA	14-61 C2,3,5-12
49	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	7	EA	C1,4,62-66
50	6000-0374-10	CONN 16 PIN HDR RT ANGLE	2	EA	J1,J2
51	6100-0137-10	SKT 24 PIN DIP LOW PRO	11	EA	X5B,X5C X5M X6B,X6C X6J,X6H X8B,X8C X9B,X9C
53	9000-0054-10	BUSS WIRE, FORMED	5	EA	GTP1-GTP5
54	7000-0120-10	CARD EJECTOR NYLON 6/6	2	EA	
56	3000-7506-10	RES,75,5%,1/4W,C	51	EA	21-31,61

BILL OF MATERIAL
AS OF 02/12/86

0121-0015-10 ASSY,PCB,DATA,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
56	3000-7506-10	RES,75,5%,1/4W,C	51	EA	33-37,58 43-50 52-56 R1-19 R1-19,60 R21,22 R24-26 R28-31 R33-37,R43 R44,R46,47 R50,52-54 R56,58 R60-64
59	3000-5106-10	RES,51,5%,1/4W,C	6	EA	R32,27,51 R48,55,65
60	3000-6806-10	RES,68,5%,1/4W,C	1	EA	R57
63	4010-0100-10	CAP,10PF,50/100V,5%,CER	4	EA	C99-102
64	6000-0293-02	CONN 2 POS HDR ST SGL ROW	4	EA	J3,4,6,7
65	6000-0293-03	CONN 3 POS HDR ST SGL ROW	1	EA	J5
66	6000-0571-10	CONN SHORTING PLUG	5	EA	XJ3,XJ4 XJ5,XJ6 XJ7
69	3000-3001-10	RES,3K,5%,1/4W,C	2	EA	R66,R67

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	01		PROTO TYPE	EM		
	02		ADD J8-J13 7/11/85	EM		
	03		REVISED FOR RELEASE			
	50	5123	PILOT REL 11/5/85	EM		
	51	5178	REVISED PER ECO# 12/4/85	DW	DW	12/9/85



LIST OF BURIED TRACES IN P.C.B.			
SOURCE OF TRACE	ETCHED ON +5V PLANE	ETCHED ON -2V PLANE	SCHEMAT. SHT NO.
1L-2	X		5
1L-13	X		5
4K-11	X		2
4K-12	X		2
4L-2	X		4
4L-13	X		4
5F-4		X	7
5F-13		X	7
5F-14	X		7
5F-15	X		7
5L-3		X	2
5L-4		X	2
6L-13	X	X	7
6L-14	X		7
6M-1		X	7
6M-2		X	7
6M-14		X	7
6M-15		X	7
8K-14	X		7
8K-15	X		7
9H-13	X		7
10L-2		X	7
10L-14		X	7
10L-15		X	7
12L-2	X		6
12L-13	X		6
5C-4	X		3
5C-5	X		3
10A-3	X		1
10A-4	X		1
9B-4		X	6
9B-5		X	6

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS.
2. ALL CAPACITANCE VALUES ARE IN MFDS.
3. SHT 8 IS WAVEFORMS
4. *** = 51Ω RESISTOR PACK TO -2V.
5. ** = 100Ω RESISTOR PACK TO -2V.
6. * = 75Ω RESISTOR PACK OR 1/4W RES TO -2V.

J8 THRU J13 (TYP)

REFERENCE DESIGNATIONS

LAST USED	NOT USED

ITEM	DESCRIPTION/SPECIFICATION	PART NAME	PART NUMBER
1			

DO NOT SCALE DRAWING. REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER PLATED FINISHES EXCEPT PAINT. 125 RMS FINISH.

TOLERANCE: DIMENSIONAL X = 1 ANGLES; XX = .030 ±1°; XXX = .010. NOTE SIZE: 0.599 = .003, 600.999 = .001, 1.000 1.499 = .005

DASH NO.	NUMBER	QTY
-10	0114-0130	—
	NEXT ASSEMBLY	

ENG. SERV. | DATE

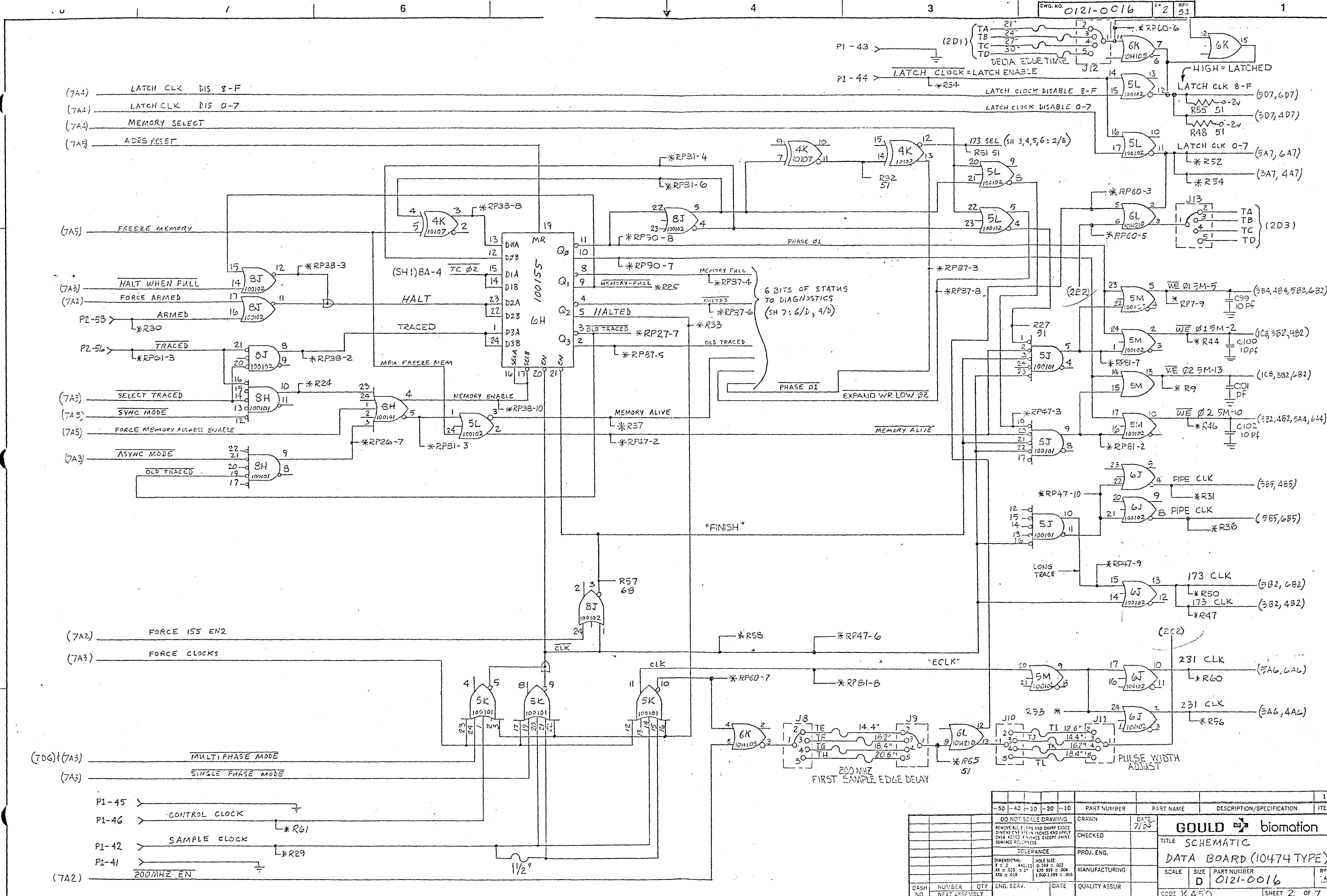
DRAWN EM 7/85 | CHECKED | PROJ. ENG. | MANUFACTURING | QUALITY ASSUR

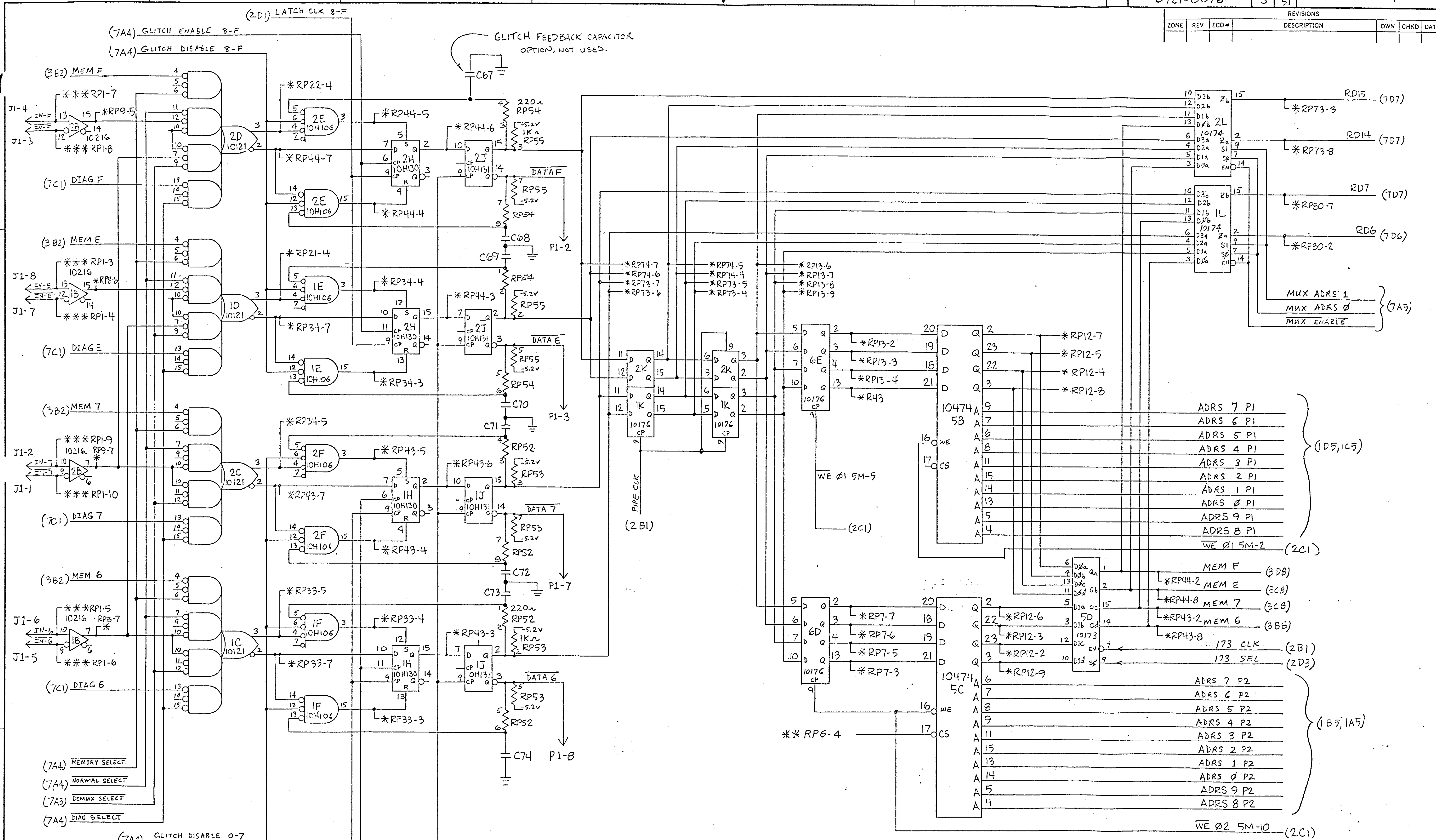
GOULD biomation

TITLE SCHEMATIC DATA BOARD (10474 TYPE)

SCALE	SIZE	PART NUMBER	REV
	D	0121-0016	5.1

CODE K450 | SHEET 1 OF 7


DWG. NO. 0121-0016 SH 2 REV 51
(2D1) TA 21" TB 24" TC 27" TD 30" DELTA EDGE TIME J12
P1-43
P1-44 LATCH CLOCK = LATCH ENABLE *R34
6K 10H105
6K
HIGH = LATCHED
LATCH CLOCK DISABLE 8-F
LATCH CLOCK DISABLE 0-7
5L 100102
LATCH CLK 8-F (5D7, 6D7)
R55 51 -2v
(3D7, 4D7)
R48 51 -2v
LATCH CLK 0-7 (5A7, 6A7)
*R52
(3A7, 4A7)
*R54
(7A4) LATCH CLK DIS 8-F
(7A4) LATCH CLK DIS 0-7
(7A4) MEMORY SELECT
(7A5) ADRS RESET
4K 10107
173 SEL (SH 3,4,5,6: 2/8)
R51 51
R32 51
*RP31-4
*RP31-6
*RP60-6
*RP60-3
*RP60-5
6L 10H210
J13 TA TB TC TD (2D3)
(7A5) FREEZE MEMORY
*RP38-8
MR
100155 6H
D0A D0B D1A D1B D2A D2B D3A D3B SELA SELB EN EN
Q0 Q1 Q2 Q3
8J 100102
*RP90-8
*RP90-7
PHASE Ø1
MEMORY FULL
*RP37-4
MEMORY-FULL *R25
HALTED
*RP37-6
5 HALTED
*R33
3 OLD TRACED *RP27-7
OLD TRACED
*RP87-5
6 BITS OF STATUS TO DIAGNOSTICS (SH 7: 6/D, 4/D)
PHASE Ø1
EXPAND WR LOW Ø2
*RP37-3
*RP37-8
(SH1) 8A-4 TC Ø2
(7A3) HALT WHEN FULL
(7A2) FORCE ARMED
P2-53 ARMED *R230
*RP38-3
HALT
TRACED
P2-56 TRACED *RPG1-3
*RP38-2
MPU FREEZE MEM
(7A3) SELECT TRACED
(7A3) SYNC MODE
(7A5) FORCE MEMORY ADDRESS ENABLE
8H 100101
*R24
MEMORY ENABLE
*RP38-10
*RP26-7
*RP31-3
MEMORY ALIVE
*R37
*RP47-2
MEMORY ALIVE
(7A3) ASYNC MODE
OLD TRACED
(2E2)
R27 51
5J 100101
*RP47-3
5M 100102
WE Ø1 5M-5 (3B4, 4B4, 5B2, 6B2)
*RP7-9
C99 10 pf
WE Ø1 5M-2 (1C8, 3B2, 4B2)
*R44
C100 10pf
*RP81-7
WE Ø2 5M-13 (1C8, 3B2, 6B2)
*R9
C101 pf
WE Ø2 5M-10 (3B2, 4B2, 5A4, 6A4)
*R46
C102 10 pf
*RP81-2
6J 100102
PIPE CLK (3B5, 4B5)
*R31
*RP47-10
PIPE CLK (5B5, 6B5)
*R36
LONG TRACE
*RP47-9
173 CLK (5B2, 6B2)
*R50
173 CLK (3B2, 4B2)
*R47
"FINISH"
R57 68
(7A2) FORCE 155 EN2
(7A3) FORCE CLOCKS
CLK
*R58
*RP47-6
"ECLK"
(2C2)
231 CLK (5A6, 6A6)
*R60
231 CLK (3A6, 4A6)
*R56
R53 *
CLK
*RP60-7
*RP81-8
5K 100101
6K 10H105
J8 TE TF TG TH 14.4" 16.2" 18.4" 20.6" J9
200 MHZ FIRST SAMPLE EDGE DELAY
6L 10H210
*R65 51
J10 TI TJ TK TL 12.6" 14.4" 16.2" 18.4" J11
PULSE WIDTH ADJUST
(7D6) & (7A3) MULTIPHASE MODE
(7A3) SINGLE PHASE MODE
P1-45
P1-46 CONTROL CLOCK *R61
P1-42 SAMPLE CLOCK *R29
P1-41
1 1/2"
(7A2) 200MHZ EN
-50 -40 -30 -20 -10 PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM 1
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: X = .1 .XX = .020 .XXX = .010 ANGLES = 1° HOLE SIZE: 0-.599 = .003 .600-.999 = .004 1.000-1.499 = .005
DRAWN DATE 7/85
CHECKED
PROJ. ENG.
MANUFACTURING
ENG. SERV. DATE
QUALITY ASSUR
DASH NO. NUMBER QTY NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC DATA BOARD (10474 TYPE)
SCALE SIZE D PART NUMBER 0121-0016 REV 51
CODE K450 SHEET 2 OF 7
KLINGLER K-VEL H



DWG. NO. 0121-0016 SH 3 REV. 51

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE: DIMENSIONAL: .X = .1 ANGLES = 1° .XX = .020 .XXX = .010; HOLE SIZE: .0-.599 = .003 .600-.999 = .004 1.000-1.499 = .005

DRAWN — DATE 7/85; CHECKED; PROJ. ENG.; MANUFACTURING; ENG. SERV.; QUALITY ASSUR

GOULD biomation

TITLE SCHEMATIC DATA BOARD (10474 TYPE)

SCALE | SIZE D | PART NUMBER 0121-0016 | REV 51

CODE K450 | SHEET 3 OF 7

REVISIONS					
ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE

(2D1) LATCH CLK 8-F
(7A4) GLITCH ENABLE 8-F
(7A4) GLITCH DISABLE 8-F

GLITCH FEEDBACK CAPACITOR OPTION, NOT USED.

C75

(4B2) MEM D
(7C1) DIAG D
(4B2) MEM C
(7C1) DIAG C
(4B2) MEM 5
(7B1) DIAG 5
(4B2) MEM 4
(7C1) DIAG 4

J1-11 J1-15 J1-10 J1-14 J1-13

10216 RP11-6, RP11-8, RP10-8, RP10-7
10216 RP2-8, RP2-7, RP2-4, RP2-3, RP2-10, RP2-9, RP2-6, RP2-5

4P 10121, 3C 10121, 4C 10121, 3D 10121

4E 10H106, 3F 10H106, 4F 10H106, 3E 10H106

4H, 4J, 3H, 3J 10H130 / 10H131

220Ω RP58, 1KΩ RP59, RP57, RP56, -5.2V

C76, C77, C78, C79, C80, C81, C82

DATA D, DATA C, DATA 5, DATA 4 → P1-4, P1-5, P1-9, P1-10

*RP24-4, *RP46-5, *RP46-2, *RP46-7, *RP46-4
*RP35-6, *RP36-6, *RP46-3, *RP36-7, *RP36-4
*RP36-5, *RP35-5, *RP45-3, *RP35-7, *RP35-4
*RP23-5, *RP45-5, *RP45-6, *RP45-7, *RP45-4

(7A4) MEMORY SELECT
(7A4) NORMAL SELECT
(7A3) ICMAX SELECT
(7A4) DIAG SELECT
(7A4) GLITCH DISABLE 0-7
(2D1) LATCH CLK 0-7
(7A4) GLITCH ENABLE 0-7
(2B1) 231. CLK

PIPE CLK (2B1)

*RP75-6, *RP75-7, *RP76-8, *RP76-7
*RP75-5, *RP75-4, *RP76-6, *RP76-4
*RP13-10, *RP27-2, *RP14-6, *RP14-7

3K, 2K 10176 CP

6E, 7E 10176 CP

*RP26-8, *RP14-8, *RP14-4, *RP14-5

6D, 7D 10176 CP

*RP7-2, *RP12-10, *RP14-9, *RP14-10

6B, 6C 10474

*RP25-8, *RP25-5, *RP25-4, *RP25-9
*RP25-7, *RP25-3, *RP25-6, *RP25-10

WE, CS

3L, 4L 10174

RD-13 (7D7) *RP74-2
RD-12 (7D7) *RP73-2
RD-5 (7D7) *RP79-8
RD-4 (7D6) *RP80-8

MUX ADRS 1
MUX ADRS Ø
MUX ENABLE
(7A5)

ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
ADRS 9 P1
ADRS 8
WE Ø1 5M-2
(1D5, 1C5)

5E 10173

MEM D (4D8)
*RP45-2 MEM C (4C8)
*RP45-8 MEM 5 (4C8)
*RP76-5 MEM 4 (4B8)
*RP76-3
173 CLK (2B1)
173 SEL (2D3)

ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
ADRS 9 P2
ADRS 8 P2
(1B5, 1A5)

WE Ø2 5M-10 (2C1)

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ASSIGNED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± .1, ANGLES, XX ± .020 = 1°, XXX ± .010
HOLE SIZE: 0 .199 ± .003; .200 .999 ± .004; 1.000 1.499 ± .005

DRAWN — DATE 7/85
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV. — DATE

DASH NO. | NUMBER | NEXT ASSEMBLY | QTY.

GOULD biomation

TITLE SCHEMATIC
DATA BOARD (10474 TYPE)

SCALE	SIZE	PART NUMBER	REV
	D	0121-0016	51

CODE K450 SHEET 4 OF 7

DWG. NO. 0121-0016 | SH 5 | REV 51

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

(2D1) LATCH CLK 8-F
(7A4) GLITCH ENABLE 8-F
(7A4) GLITCH DISABLE 8-F
GLITCH FEEDBACK CAPACITOR OPTION, NOT USED.
C83
(5B2) MEM B
(7C1) DIAG B
(5B2) MEM A
(7C1) DIAG A
(5B2) MEM 3
(7B1) DIAG 3
(5B2) MEM 2
(7B2) DIAG 2
J2-4 IN-B, J2-3 IN-B
J2-8 IN-A, J2-7 IN-A
J2-2 IN-3, J2-1 IN-3
J2-6 IN-2, J2-5 IN-2
11B 10216 RP4-7 RP18-7 RP4-8
10B 10216 RP4-2 RP17-7 RP4-3
11B 10216 RP4-9 RP18-8 RP4-10
10B 10216 RP4-5 RP17-5 RP4-6
11D 10121
10D 10121
11C 10121
10C 10121
11E 10H106
10E 10H106
11F 10H106
10F 10H106
11H 10H130
10H 10H130
11J 10H131
10J 10H131
RP30-4 RP49-7 RP49-8 RP49-6
RP17-3 RP40-4 RP40-7 RP40-3
RP40-5 RP48-6 RP48-8 RP48-5
RP39-5 RP39-4 RP39-7 RP39-3
RP49-4 RP49-5 RP48-3 RP48-4
220Ω RP65 5.2V 1K Ω RP60
RP66 RP65 C84 C85
RP65 RP66 C86 C87
RP63 RP64 C88 C89
220Ω RP63 1K Ω RP64 C90
DATA B DATA A DATA 3 DATA 2
P2-84 P2-85 P2-89 P2-90
(2B1) PIPE CLK
(7A4) MEMORY SELECT
(7A4) NORMAL SELECT
(7A3) LEMUX SELECT
(7A4) DIAG SELECT
(7A4) GLITCH DISABLE 0-7
(2D1) LATCH CLK 0-7
(7A4) GLITCH ENABLE 0-7
(2B1) 231 CLK
RP71-5 RP71-6 RP78-5 RP78-6
RP72-5 RP71-4 RP72-4 RP78-4
RP26-2 RP27-6 RP26-3 RP7-4
11K 12K 7E 8B 8C 9E 10K 11L 10174 10176 10173
R6 R5 RP15-2 R7
R4 RP15-7 RP14-3 RP14-2
RP28-3 RP28-5 RP28-2 RP28-8
RP28-6 RP28-4 RP28-7 RP28-9
WE 02 SM-10 (2C1)
RD11 (7D7) *RP74-3
RD10 (7D7) *RP74-8
RD3 (7D7) *RP79-3
RD2 (7D6) *RP79-2
MUX ADRS 1
MUX ADRS Ø
MUX ENABLE
(7A5)
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
ADRS 9 P1
ADRS 8 P1
(1D5, 1C5)
WE Ø1 SM-5 (2C1)
MEM B (5D8)
*RP48-2 MEM A (5C8)
*RP48-7 MEM 3 (5C8)
*RP49-3 MEM 2 (5B8)
*RP49-2
173 CLK (2B1)
173 SEL (2D3)
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
ADRS 9 P2
ADRS 8 P2
(1B5, 1A5)
WE Ø2 SM-13 (2C1)

ITEM	DESCRIPTION/SPECIFICATION	PART NAME	PART NUMBER
1			

DO NOT SCALE DRAWING
BREAK ALL R.015 AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND ARE AFTER FINISHES EXCEPT PAINT
SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: X = ±1, XX = ±.02, XXX = ±.010
ANGLES ±1°
HOLE SIZE: .000 - .003 = .005, .004 - .006 = .010

DRAWN | DATE 7/85
CHECKED
PROJ. ENG.
MANUFACTURING
ENG SERV. | DATE
QUALITY ASSUR

DASH NO. | NUMBER | QTY
NEXT ASSEMBLY

GOULD biomation

TITLE SCHEMATIC
DATA BOARD (10474 TYPE)

SCALE	SIZE	PART NUMBER	REV
	D	0121-0016	51

CODE K450 | SHEET 5 OF 7

RUNNER'S REVEL M

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

(2D1) LATCH CLK 8-F
(7A4) GLITCH ENABLE 8-F
(7A4) GLITCH DISABLE 8-F
GLITCH FEEDBACK CAPACITOR OPTION, NOT USED.
C91
(6B2) MEM 9
(6B2) MEM 8
(6B2) MEM 1
(6B2) MEM Ø
(7C1) DIAG 9
(7C1) DIAG 8
(7B1) DIAG 1
(7C1) DIAG Ø
13D 10121
12C 10121
13C 10121
12D 10121
13E 10H106
12F 10H106
13F 10H106
12E 10H106
13H 10H130
12H 10H130
13J 10H131
12J 10H131
220Ω RP69
1K Ω RP70
RP68
DATA 9
DATA 8
DATA 1
DATA Ø
P2-86
P2-87
P2-91
P2-92
C92
C93
C94
C95
C96
C97
C98
13K 10176
12K 10176
8E 10176
8D 10176
PIPE CLK
(2B1)
WE Ø2S M-10 (2C1)
10474 98
10474 9C
10173 9D
10174 12L
10174 13L
RD9 (7D7)
RD8 (7D7)
RD1 (7D7)
RD Ø (7D6)
MUX ADRS 1
MUX ADRS Ø
MUX ENABLE
(7A5)
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
ADRS 9 P1
ADRS 8 P1
(1D5, 1C5)
WE Ø1 5M-5 (2C1)
MEM 9 (6D8)
MEM 8 (6C8)
MEM 1 (6C8)
MEM Ø (6B8)
173 CLK (2B1)
173 SEL (2D3)
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
ADRS 9 P2
ADRS 8 P2
(1B5, 1A5)
WE Ø2 5M-13 (2C1)
231 CLK (2B1)
(7A4) MEMORY SELECT
(7A4) NORMAL SELECT
(7A3) LEMAX SELECT
(7A4) DIAG SELECT
(7A4) GLITCH DISABLE 0-7
(2D1) LATCH CLK 0-7
(7A4) GLITCH ENABLE 0-7

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: X = 1, XX = .020 = 1°, XXX = .010
HOLE SIZE: 0 .599 = .003; .600 .999 = .004; 1.000 1.499 = .005

DRAWN	DATE 7/83
CHECKED	
PROJ. ENG.	
MANUFACTURING	
ENG. SERV.	DATE
QUALITY ASSUR	

GOULD biomation

TITLE SCHEMATIC
DATA BOARD (10474 TYPE)

SCALE	SIZE	PART NUMBER	REV
	D	0121-0016	51

CODE K450 SHEET 6 OF 7

DWG. NO. 0121-0016 | SH 7 | REV 51

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

MPU READING FROM AND WRITING TO THIS BOARD

READ RESULT	ADDRESS BA3	BA2	BA1	WORD SELECTED	WRITE RESULTS
MEMORY CONTENTS	0	0	0	WØ Bn	NOT USED
OLD PIPELINE	0	0	1	W2 Bn	MODE SELECT
NEW PIPELINE	0	1	0	W4 Bn	INPUT & CLOCKS
DATA IN SAMPLE REG.	0	1	1	W6 Bn	DIAG DATA
STATUS	1	X	X	W8, WA, WC, WE	NOT USED

note: BA4 & BA5 DECODE IS A FUNCTION OF CARD SLOT ON MOTHER BOARD

MPU READING FROM THIS BOARD

(MY ADDRESS)·(RD) ENABLES TRISTATE ONTO BUS.
(MY ADDRESS)·(BA3, BA2, BA1) SELECTS READ DATA.

note: OLD DATA BOARD (7077): ZERO = STATUS!

EXPAND WR LOW Ø2 (2C4)
MULTIPHASE MODE (7A3)
ASYNC MODE (7A3)
MEMORY ALIVE (2C4)
PHASE Ø1 (2C4)
MEMORY FAIL (2C4)
OLD TRACED (2C4)
HALTED (2C4)
MUX ENABLE (7A5)

8M 74LS244 | 10M 74LS244

10173 13M | 10173 12M

10125 1M | 10125 2M | 10125 3M

10124 6M | 10124 7L | 10124 10L | 10124 9K | 10124 8K

10176 7F | 10176 5F | 10176 8F | 10176 9H | 10176 9L | 10176 5H | 10176 9F

74S85 9M | 74S37 8L | 74LS14 7M | 74S37 8L

3K/6.2K RP32 | 3K/6.2K RP35 | 3K/6.2K RP77 | 3K/6.2K RP33 | 3/6.2K RP83 | 2.2K RP84

+5.V | -5.2v

(WRITE)·(MY ADDRESS)
(READ)·(MY ADDRESS)
(READ FROM ME ONTO BUS)
WRITE TO ME
MUX ENABLE (7D4, 3C1, 4C1, 5C1, 6C1)
MUX ADRS 1
MUX ADRS Ø
} (3C1, 4C1, 5C1, 6C1)

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X = 1 ANGLES | XX = .020 = 1° | XXX = .010
HOLE SIZE: 0.188 = .003 | 500-999 = .004 | 1.000-1.499 = .005

		DATE
DRAWN		7/85
CHECKED		
PROJ. ENG.		
MANUFACTURING		
QUALITY ASSUR		
ENG. SERV.		DATE

GOULD biomation

TITLE SCHEMATIC
DATA BOARD (10474 TYPE)

SCALE	SIZE	PART NUMBER	REV
	D	0121-0016	51

CODE K450 | SHEET 7 OF 7

KLINGLER KVEL M