

HP 16510B

Logic Analyzer Module

for the HP 16500A Logic Analysis System

Getting Started Guide



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Getting Started Guide

HP 16510B Logic Analyzer Module for the HP 16500A Logic Analysis System



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How To Use This Guide

This guide teaches you the basic operation of the HP 16510B Logic Analyzer Module for the HP 16500A Logic Analysis System. It is organized in a task-oriented format that guides you through the touch-screen menus and basic measurements that you will use to solve digital system problems.

You should read this guide and perform the learning tasks once you have become familiar with the operation of the HP 16500A mainframe.

If you are an experienced HP logic analyzer user but new to this family of logic analyzers, you may want to go directly to the *HP 16510B Front-Panel Reference*, but we would like to suggest that you read chapters 1 through 4 of this guide first. These chapters describe the basics of the user interface and will only take a few minutes to go through. The user interfaces of the HP 16500A Logic Analysis System and its modules are very friendly and easy to learn.

This guide is formatted to help you through setups and measurements in the shortest time possible. To that end, you will occasionally see illustrations interspersed with or alongside the text showing a menu with a hand pointing to the field we are talking about. If you are going through a sequence for the first time, you may want to refer to the illustrations while reading the text to aid your understanding. If you know the basic operation and just need to refresh your memory about the sequence, you can follow the same steps without reading the text by just referring to the illustrations.

Introduction

About this book...

Welcome to the new generation of HP logic analyzers! The HP 16500A Logic Analysis System has been designed to make it easier to use than any previous Hewlett-Packard logic analyzer. And because of its configurable architecture, it can easily be tailored to you specific logic design and debug needs.

The user interface of the HP 16500A was designed to be as easy to operate as possible. The use of "pop up" windows and color graphics help lead you through setups and measurements without having to memorize a lot of steps. As you read this and the other references about the mainframe and the acquisition modules, you will see just how easy to use the HP 16500A really is.

We do not, however, try to cover every feature and function of the HP 16510B Logic Analyzer Module in this guide. That's the job of your *HP 16510B Front-Panel Reference*.

If you're new to logic analysis or just need a refresher, we think you'll find *Feeling Comfortable With Logic Analyzers* valuable reading. It will help you sort out any confusion you may have about their application and show you how to get the most out of your new logic analyzer.

If you haven't already read "How to Use This Guide", you should do so now. It will help get you started in the right direction.

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What is the HP 16510B

The HP 16510B Logic Analyzer is a programmable logic analyzer module that is installed in the HP 16500A Logic Analysis System. It offers 80 data channels, thus allowing the HP 16500A to have up to 400 channels when configured with five HP 16510B cards. It is capable of 100 MHz timing and 35 MHz state analysis on all channels.

The key features of the HP 16510B are:

- Transitional or glitch timing modes
- Simultaneous state/state or state/timing modes
- 1k-deep memory on all channels
- Glitch detection on all channels
- Marker measurements
- Pattern, edge, and glitch triggering
- Overlapping of timing waveform
- Eight sequence levels
- Eight pattern recognizers
- One range recognizer
- Small, lightweight probing
- Time and number of state tagging
- Pre-store
- State Compare
- State Waveform
- State Chart

Not all of these features will be covered in this *Getting Started Guide*. However, you can find the details of these and all the features of the HP 16510B in the *HP 16510B Front-Panel Reference*.

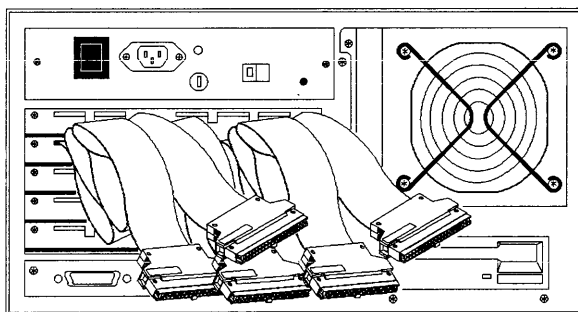
Cables and Probes

Introduction

This chapter describes the cables and probes that connect the HP 16510B module to your test system. If your system was ordered without the cards (PC boards) installed, or if you want to move the cards to another instrument, refer to the *HP 16510B Front-Panel Reference*.

What Cables and Probes Are Included?

The cables are already connected when you receive your instrument, exiting via the rear panel. Each card comes with five 1.4 m (4.5 ft.) 2 by 20, ribbon cables.



16510e07

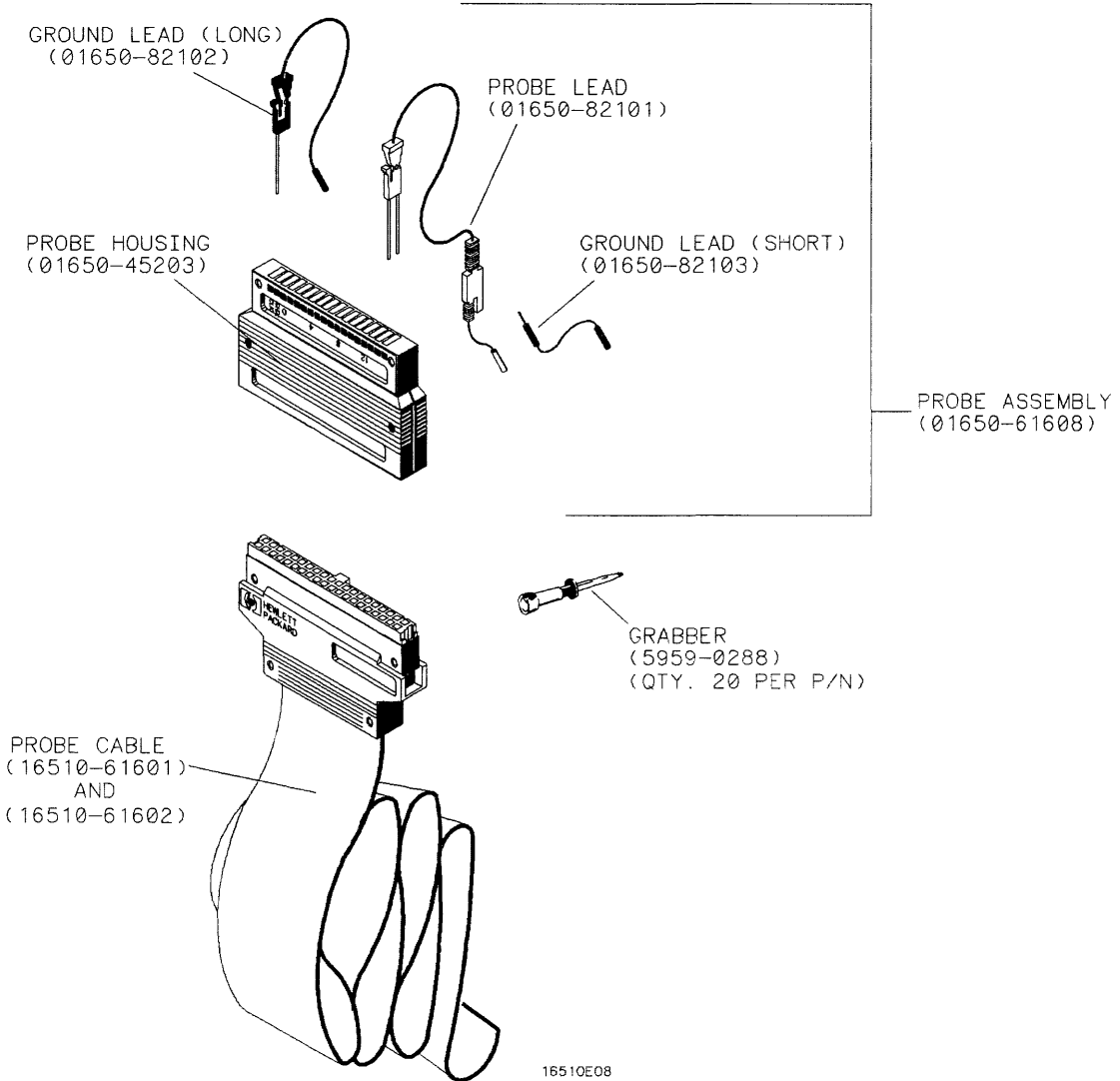
The cable for pod 1 is the far left cable (rear view). Cables 2 through 5 follow cable 1 consecutively from left to right.

It also comes with one bag of probes, leads and grabbers. This bag contains five sets of each of the following:

- 1 - probe pod
- 17 - acquisition probes
- 1 - pod ground
- 2 - probe grounds
- 20 - grabbers

Probe Assembly Identification

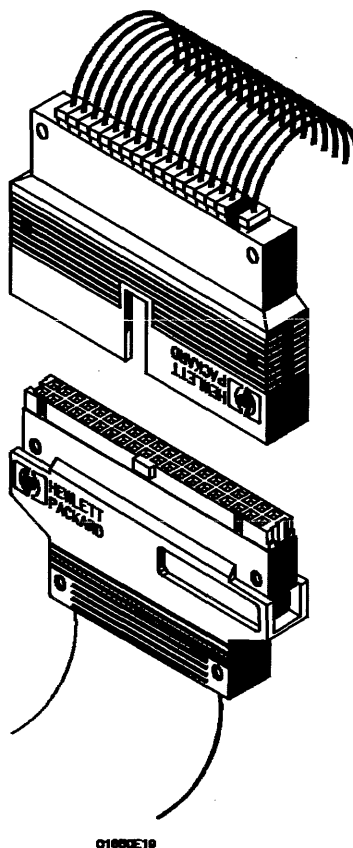
The illustration below identifies the different probes and assemblies used to connect to a test system.



16510E08

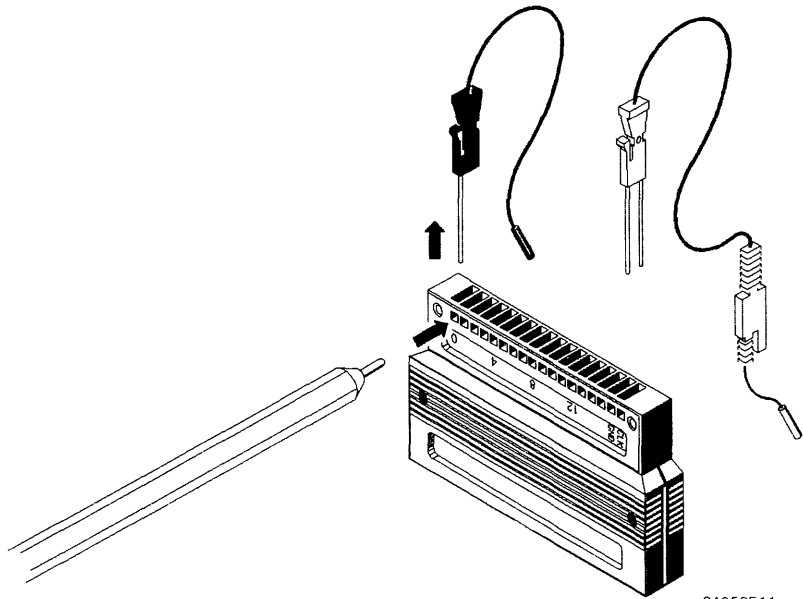
Connecting Pods to Probe Cables

The pods of the HP 16510B differ from those of other logic analyzers in that they are passive (have no active circuits at the outer end of the cable). The pods are the connector bodies in which the probes are installed when you receive your instrument. To connect the pod to the cable, align the key on the cable connector with the slot on the pod connector and push them together.



Disconnecting Probes from Pods

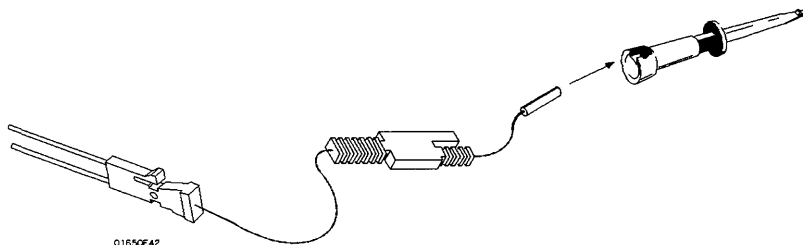
You can disconnect un-used probes from the pods to eliminate clutter. To disconnect a probe, insert the tip of a ball-point pen into the latch opening and push while gently pulling the probe out of the pod connector as shown below.



To reconnect a probe, insert the double-pin end of the probe into the pod. The probes and pod connector body are both keyed (chamfered) so that they will fit together in only one way.

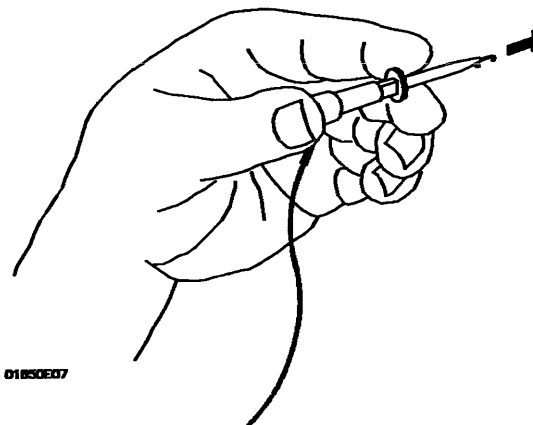
Connecting Grabbers to Probes

Connect the grabbers to the probes by slipping the connector at the end of the probe onto the recessed pin in the side of the grabber as shown below.



Connecting Grabbers to Test Points

The grabbers have a hook that fits around IC pins and component leads. You connect the grabber by pushing the rear of the grabber to expose the hook, hooking the lead, and releasing your thumb as shown below.



Pod Grounds

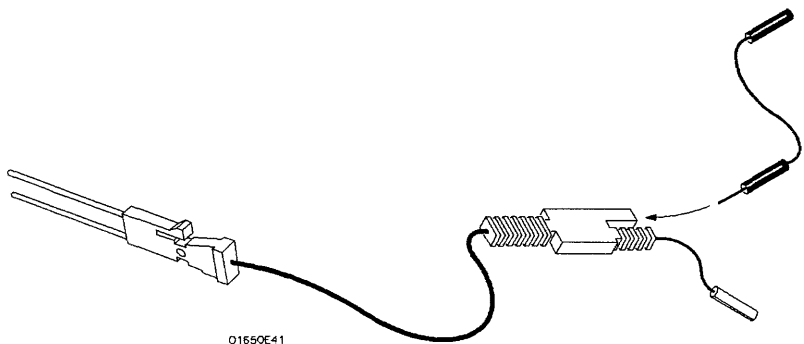
Each pod has a separate ground lead that allows you to connect the ground side of all the probes to a common ground. Connect it directly or with a grabber to a ground point on your test system. Connect the grabber to the ground lead by slipping the connector of the lead onto the recessed pin in the side of the grabber.

To connect the ground lead directly to the ground pins on the test system, the pins must be 0.63 mm (0.025 in.) square pins or round pins with a diameter from 0.66 mm (0.026 in.) to 0.84 mm (0.033 in.).

Probe Grounds

You can ground the probes in one of two ways. You can ground them with the pod ground only; however, the ground path won't be the same length as the signal path through the probe. If your probe ground path must be the same as your signal path, use the short ground lead (probe ground). The probe ground lead connects to the probe body via a pin and socket as shown below. A grabber can be used to connect the probe ground to the test system, or it can be connected directly to square 0.63 mm (0.025 in.) or round 0.66 mm (0.026 in.) pins on the test system.

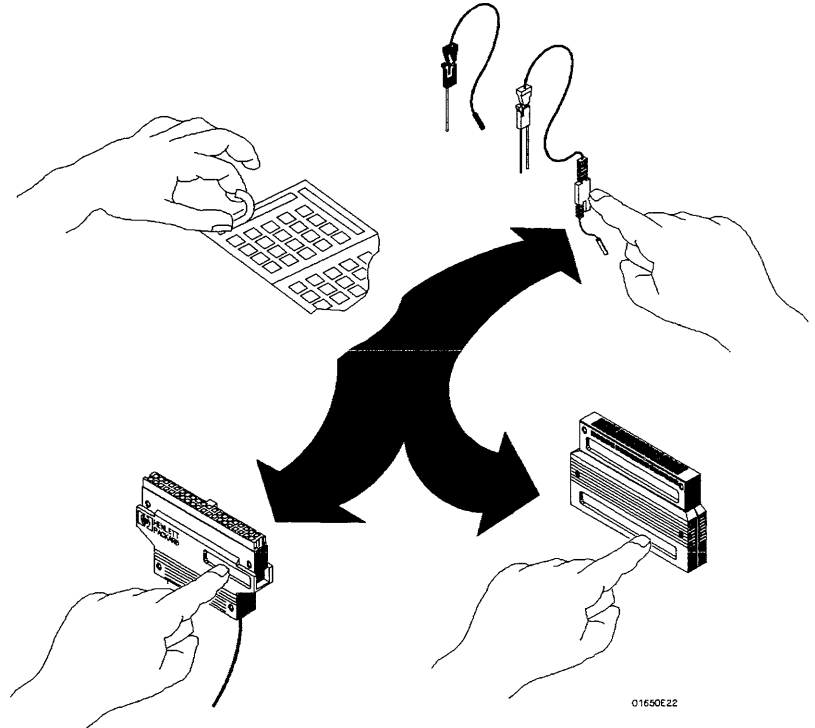
If you need additional probe ground leads, order HP part number 01650-82103 from your nearest Hewlett-Packard sales office.



Labeling Pods Probes and Cables

Included with your logic analyzer are self-adhesive labels you can attach to each pod, cable and probe. These provide a means of quickly locating and identifying the desired probes and pods for easy accurate connections.

The labels come in sets. Each set has a label for the pod connector body, a label for the clock probe, and 16 labels for each of the channels.



Signal Line Loading

Any signal line to be connected to a probe must be able to supply a minimum of 600 mV to the probe tip, which has an input impedance of 100 k Ω shunted by 8 pF. If the signal line can't supply this voltage, not only will you get an incorrect measurement, the system under test could malfunction.

Probe Interface

Instead of connecting the probe tips directly to the signal lines, you may use the HP 10269C Probe Interface (optional accessory). It allows you to connect the pod cables (without the probes) to connectors on the interface. When the appropriate preprocessor is installed in the interface, you will have a way to connect the interface directly to the microprocessor under test. A number of microprocessor-specific preprocessors are available as optional accessories. They are listed in the *HP 16510B Front-Panel Reference* along with additional details on how the probe interface and preprocessors work.

Summary

This chapter acquainted you with:

- what cables and probes are included with the module;
- how to identify the different probe assemblies;
- how to connect the pods to the cables;
- how to connect and disconnect the probes from the pods;
- how to connect and use the grabbers;
- the pod and probe grounds;
- labeling the probes, pods and cables;
- the minimum output for a signal line that you want to measure.

For more information on the probes and cables, refer to the *HP 16510B Front-Panel Reference*.

Getting to the Logic Analyzer Menus

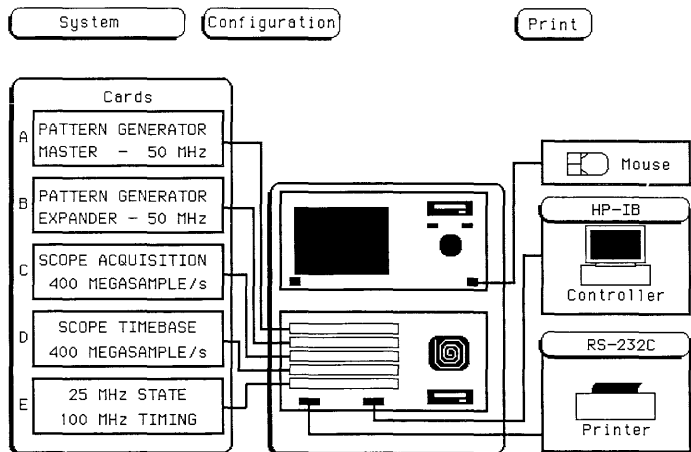
Touch or Mouse?

Before talking about the actual operation of the HP 16510B, we should mention that it has three user interface devices: the knob on the front panel, the touch-sensitive screen, and the optional mouse. If you are unfamiliar with their use, refer to the *Front-Panel Reference* for the HP 16500A mainframe.

"Touching" in this guide means touching the screen or using the mouse. For example, if the guide says to touch a specific field, it means you may touch that field on the screen (provided the touch screen is activated) or you may move the cursor to that field with the mouse and press the left button on the mouse.

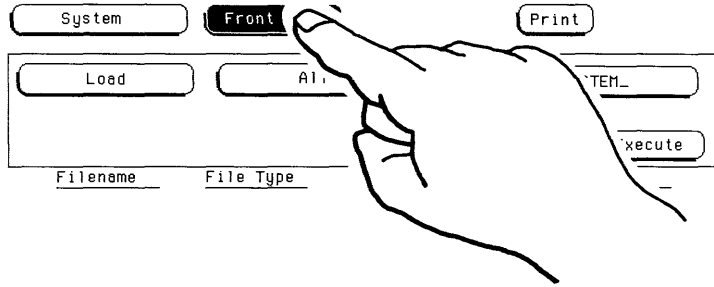
System Power Up

When the system is powered up, you should see a menu like the one below.

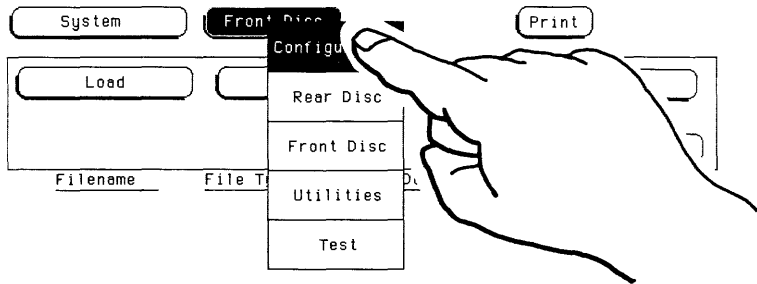


This is the System Configuration menu. If you have a different menu on the screen, you can get back to the Configuration menu with the following steps:

1. Touch the field second from the left at the top of the screen.
2. When the pop-up appears, touch the field labeled "Configuration."



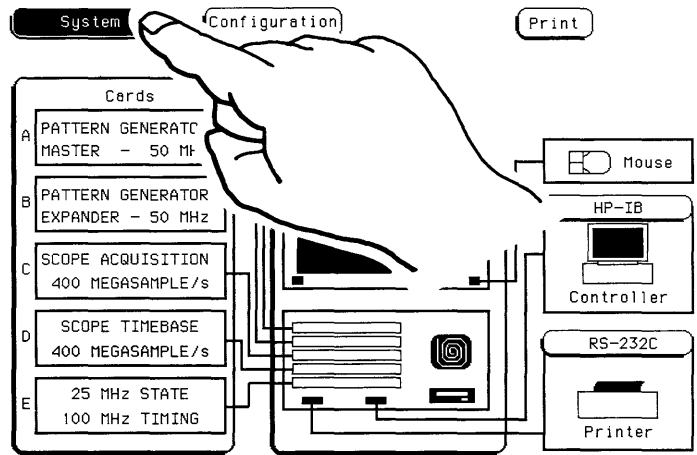
SYSTEM_	HP16500A	HP16500A System Software	V00.08
SYSTEM_001	001_system	1 GHz Timing Analyzer	V00.08
SYSTEM_011	011_system	400MSample/s Dig. Scope	V00.08
SYSTEM_021	021_system	50Mbit/s Pattern Gen.	V00.08
SYSTEM_031	031_system	25MHz State/100MHz Timing	V00.08



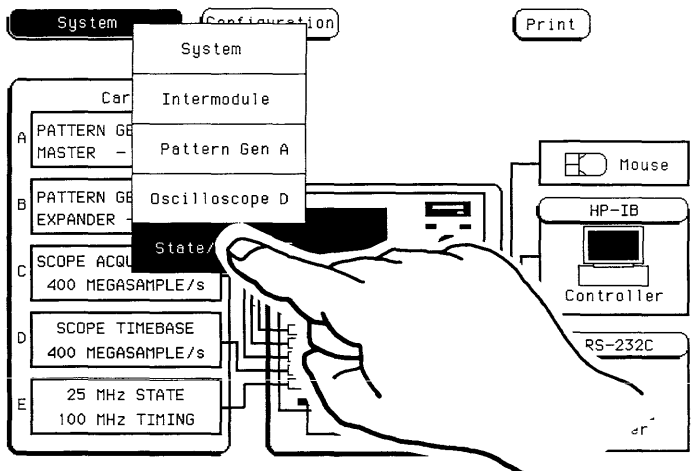
SYSTEM_	HP16500A	HP16500A System Software	V00.08
SYSTEM_001	001_system	1 GHz Timing Analyzer	V00.08
SYSTEM_011	011_system	400MSample/s Dig. Scope	V00.08
SYSTEM_021	021_system	50Mbit/s Pattern Gen.	V00.08
SYSTEM_031	031_system	25MHz State/100MHz Timing	V00.08

Moving to the Logic Analyzer

Now touch the field in the upper left of the screen labeled "System." A pop-up will appear displaying all the modules in the mainframe similar to that shown below.



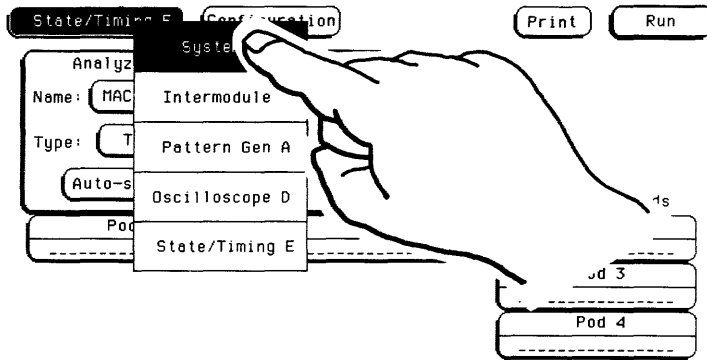
The actual order and content of the pop-up will depend on which modules you have installed and in which slots. In this example, to get to the logic analyzer menus, you should touch the "State/Timing E" field. This will bring up the logic analyzer configuration menu.



Getting Back to System Level

Depending on which module menu you are in, the name of the module will appear at the top left of the screen. This is the same field that previously said System. An important feature to remember about the HP 16500A menu structure is this: you are typically not more than three touches away from the system configuration menu. Why is this important? Because this makes it next to impossible to go so deep in menus that you can't find your way out.

To get back to the System Configuration menu, touch the field at the top left of the screen. When the pop-up appears, touch the field labeled "System."



Learning the Basic Logic Analyzer Menus

Introduction

In this chapter you will learn the most common pop-up menu types by doing some basic exercises. The pop-up menu types you will learn in this chapter are:

- Selector
- Alpha Entry
- Numeric Entry
- Assignment/Specification

To begin, move to the logic analyzer Configuration menu by following the method described in "Moving to the Logic Analyzer" in Chapter 3.

Selector Pop-up Menu

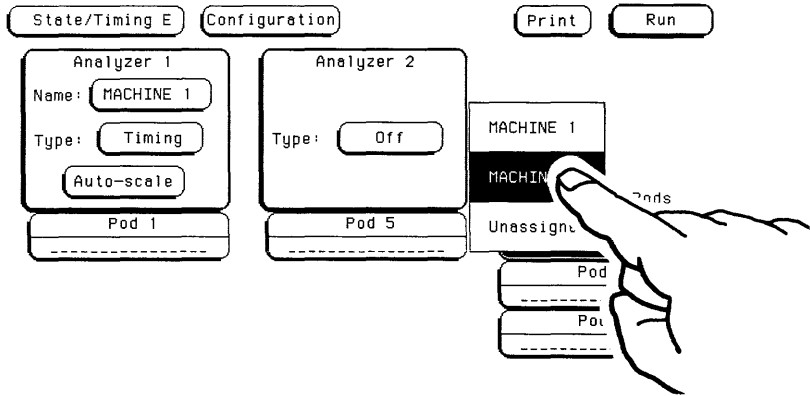
In the selector type of pop-up menu you do what the name implies: make a selection from two or more options. The best way to introduce the selector type of menu is to have you work with one right away.

Assigning Pods

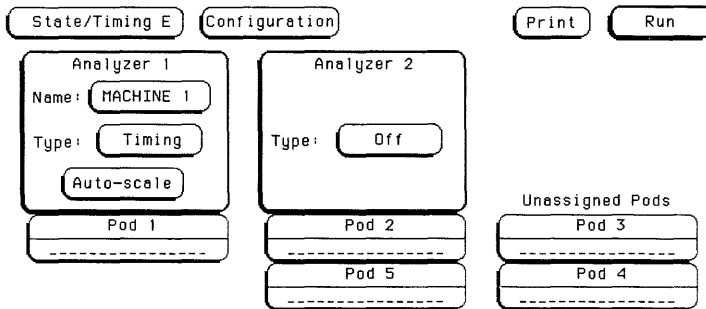
You will use a selector type of pop-up menu to assign pods to the analyzers. To assign pods:

1. Touch one of the pod fields in the Configuration menu on the right side of the display.

In the pop-up, touch the field labeled "Machine 2."



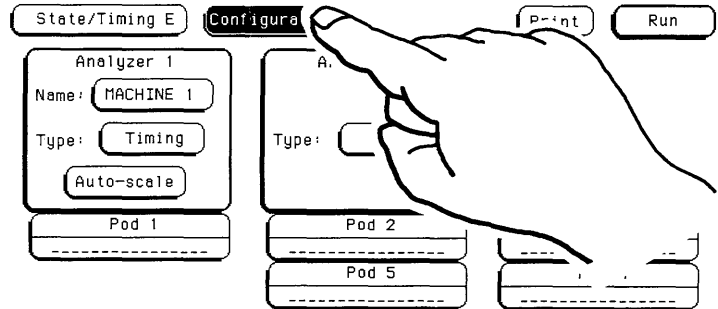
The pop-up closes and your desired pod is now assigned to Analyzer 2.



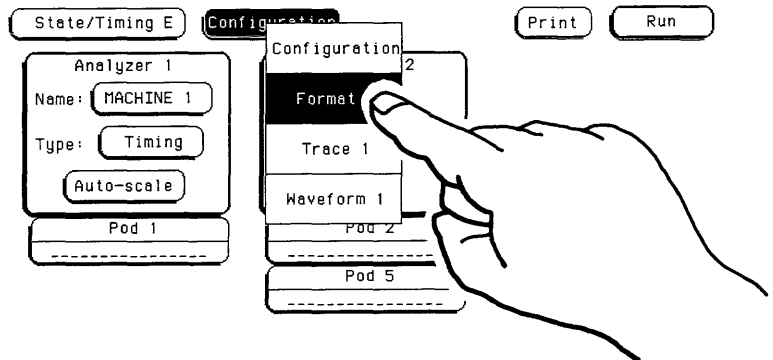
Choosing Specification Menus

Another selector menu type that you will use quite often allows you to switch between specification menus. To do this:

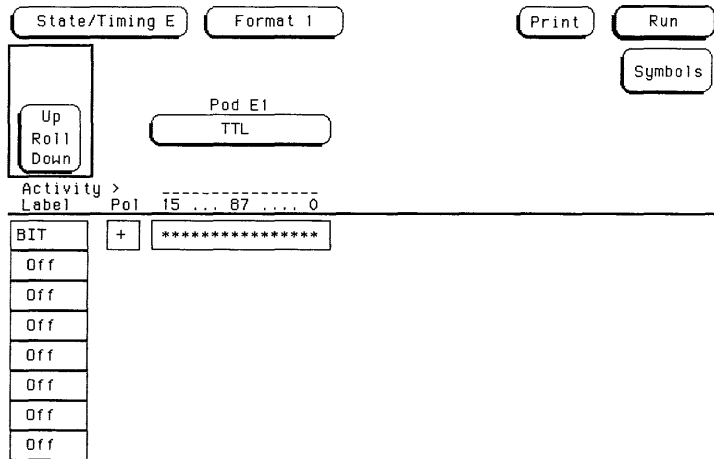
1. Touch the field second from the left at the top of the screen.



2. The pop-up that appears is shown below. Choose which specification menu you want and touch that field. For example to get to the timing Format specification menu, touch the field labeled Format 1.



This closes the pop-up and puts you in the timing Format menu.



Alpha Entry Pop-up Menu

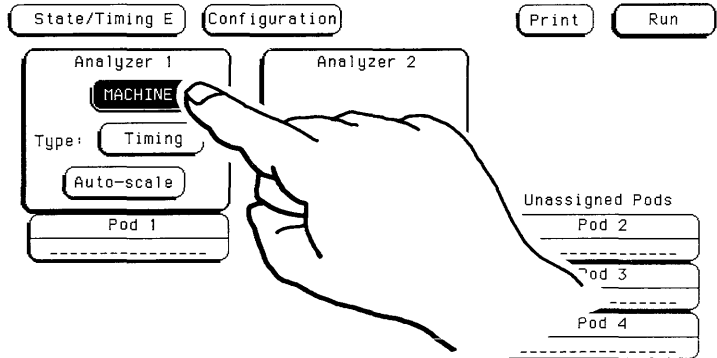
You can give specific names to several things. These names can represent your measurement specifically.

The two major examples of items that can be named are:

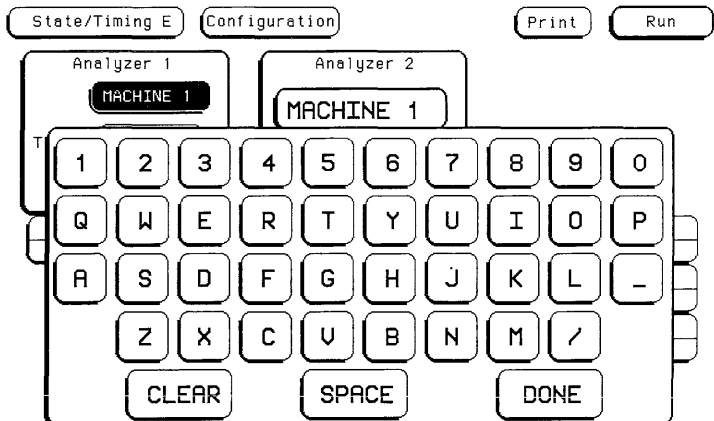
- Both analyzers
- Labels

To learn how this type of pop-up works, you will name Analyzer 1 LEARN. However, you will misspell it. You will then be shown how to correct it.

1. Get back to the logic analyzer Configuration menu by touching the field second from the left at the top of the screen. Then touch the field labeled Configuration in the pop-up.
2. In the Configuration menu, touch the field labeled Machine 1.



You will now see an alphanumeric keyboard similar to a typewriter keyboard, as shown below.

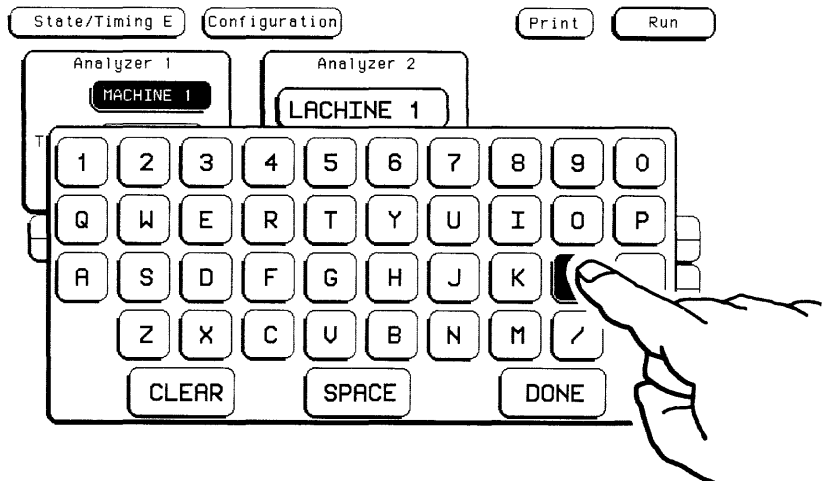


At the top of the keyboard you will see a space that contains the label "Machine 1." The cursor in this area will tell you where the next letter or number will appear when you touch it on the keyboard. The cursor can be moved within the display with the KNOB.

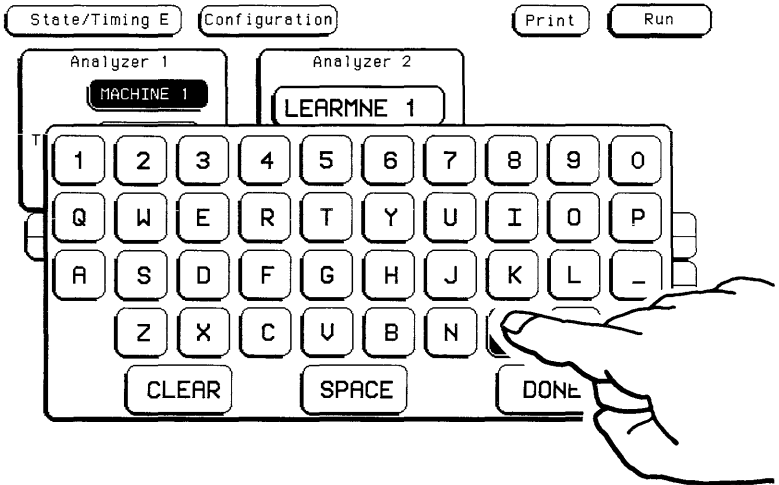
Note 

The cursor is not printed on a hardcopy printout therefore it is not printed in the illustrations in this guide.

3. Now that you are ready to name Analyzer 1, position the cursor over the M in Machine and touch the L key. Notice that "M" has been changed to "L."



4. Touch the E, A, R, and M keys.

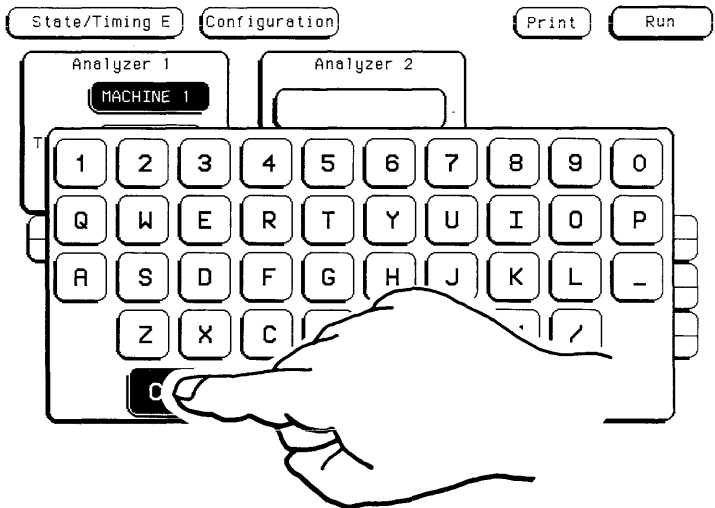


You should now see LEARMNE 1 in the display above the keyboard. Since this is not the name you wanted, change it.

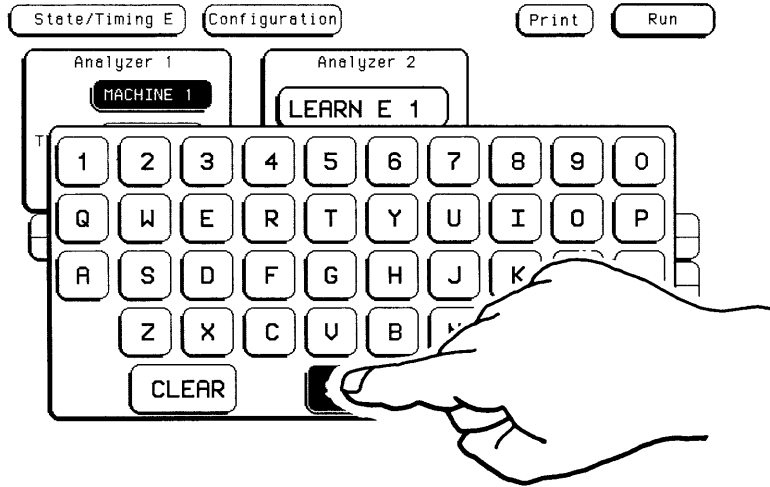
Changing Alpha Entries

To change the name, place the cursor on the character you wish to change and touch the new character.

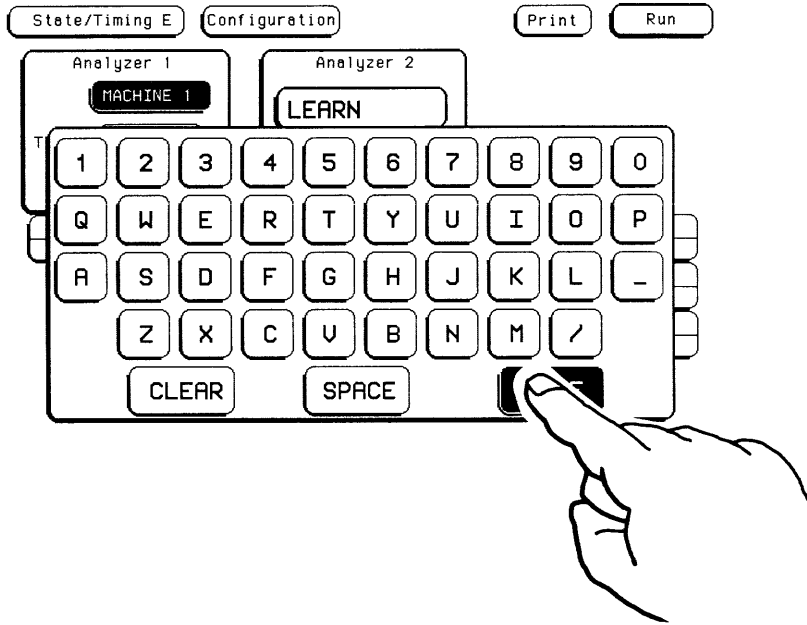
If you want to erase the entire entry and place the cursor at the beginning of the name box, touch the key labeled CLEAR.



If you want to replace a character with a space, place the cursor on that character and touch the key labeled SPACE.



Correct the name that we are working on from LEARMNE 1 to LEARN using the KNOB and the appropriate keys. After the name is correct, touch the field labeled DONE. This closes the pop-up and changes the name of analyzer 1 to LEARN.



Now that you have entered and edited a name, you will know how to use the Alpha Entry pop-up menu when it appears in other logic analyzer menus.

Numeric Entry Menus

There are many pop-up menus in which you enter numeric data. The two major types are:

- Numeric entry with fixed units
- Numeric entry with variable units (i.e. ms, ns, etc.)

There are several numeric entry menus where you enter only the value, the units being pre-determined. There are other numeric entry menus for which you will be required to specify the units. One such type of numeric entry pop-up is the POD Threshold pop-up menu.

Besides being able to set the pod thresholds to either of the preset values (TTL or ECL), you can set the thresholds to a specific voltage between -9.9 V and $+9.9\text{ V}$.

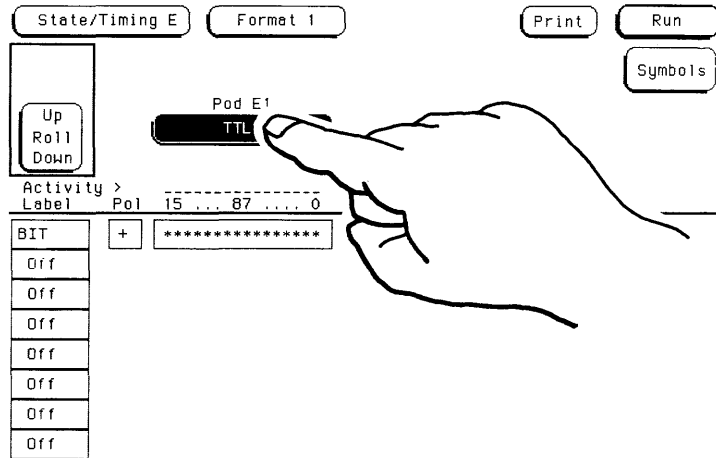
To set pod thresholds to a specific voltage, follow these steps:

1. Select either Format 1 or Format 2 to get to either the timing or state Format specification menu using the method described in "Choosing Specification Menus" earlier in this chapter. This displays either the state or timing Format specification. It does not matter whether you are in the timing or state Format specification menu.

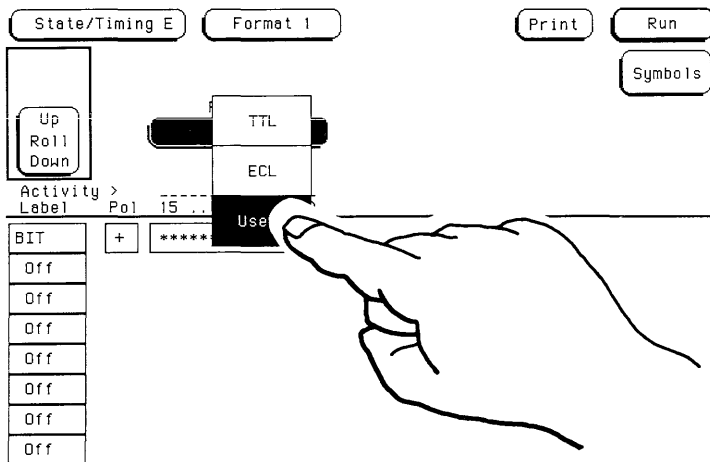
2. Touch the field of any pod displayed. You will now see a pop-up with the choices TTL, ECL, and User.

Note 

If you don't see any pods displayed, it simply means that you do not have any pods assigned to this analyzer. Either switch analyzers or assign a pod to the analyzer with which you are working.

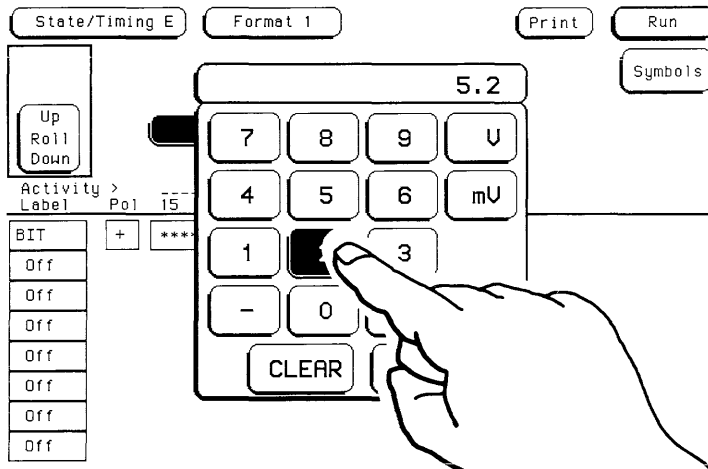


3. In the pop-up, touch the field labeled "User."

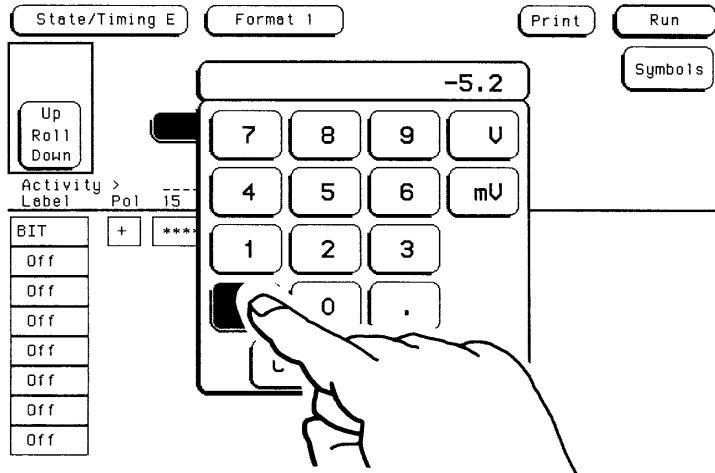


A numeric keypad will appear. You can use the keypad to enter your desired threshold. The space above the keypad will display the numbers as you touch them. To enter -5.2 V:

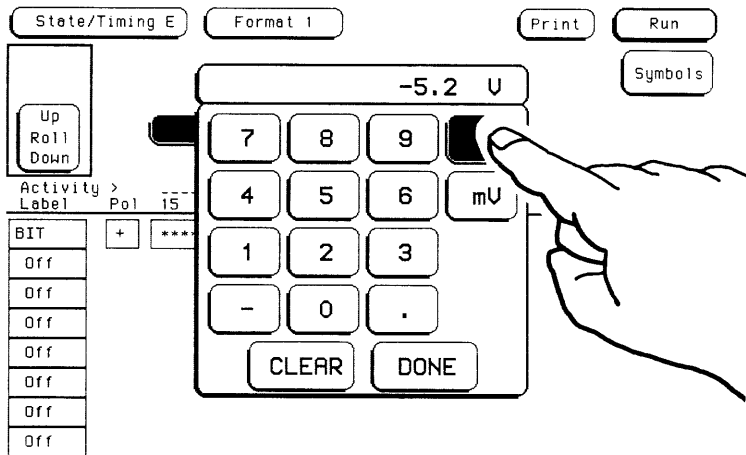
4. Touch the keys labeled "5", ".", and "2." Notice that 5.2 appears in the display above the keypad.



5. Touch the key with the – sign. Now you will see – 5.2 in the display.



6. Select your units by touching either of the keys on the right side of the keypad. For this example, touch the key labeled "V." The display now shows – 5.2 V.



7. Touch the DONE field to close the pop-up and place the new threshold in the Pod field.

The screenshot shows a logic analyzer interface with several menu items and a data table. At the top, there are buttons for 'State/Timing E', 'Format 1', 'Print', 'Run', and 'Symbols'. On the left, a vertical menu contains 'Up', 'Roll', and 'Down'. In the center, a 'Pod E1' field displays '-5.2V'. Below this, a table shows 'Activity >' and 'Label Pod' with values '15 ... 87 ... 0'. A horizontal line separates this from a table with columns 'BIT' and '+'. The 'BIT' column lists 'Off' seven times, and the '+' column contains a field with '*****'.

Activity >	Label	Pod
	15	... 87 ... 0

BIT	+
Off	*****
Off	
Off	
Off	
Off	
Off	
Off	
Off	

Assignment/ Specification Menus

There are a number of pop-up menus in which you assign or specify what you want the logic analyzer to do. The basic menus of this type consist of:

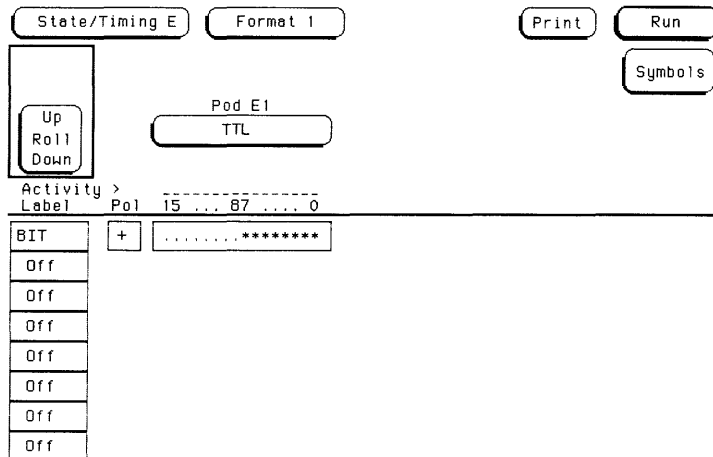
- Assigning bits to pods
- Specifying patterns
- Specifying edges

Assigning Bits to Pods

The bit assignment fields in both state and timing analyzers work identically. Before starting this exercise you need to know how the logic analyzer knows which bits are assigned and which ones are not assigned. The convention for bit assignment is:

- * (asterisk) indicates assigned bits
- . (period) indicates un-assigned bits

In the following menu example, bits 0 through 7 are assigned to the label BIT.

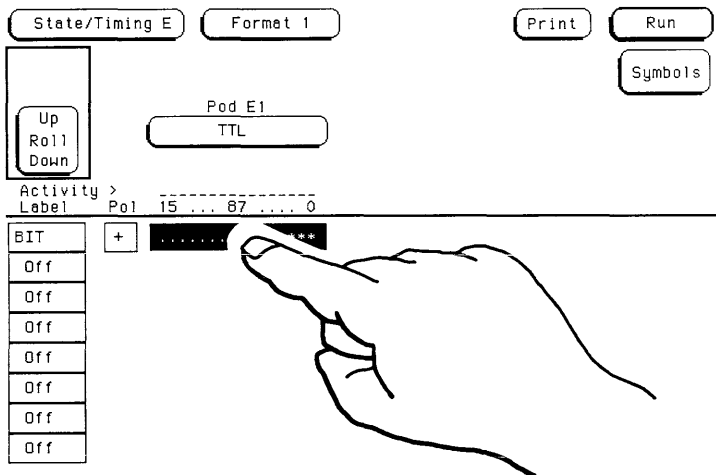


To assign bits:

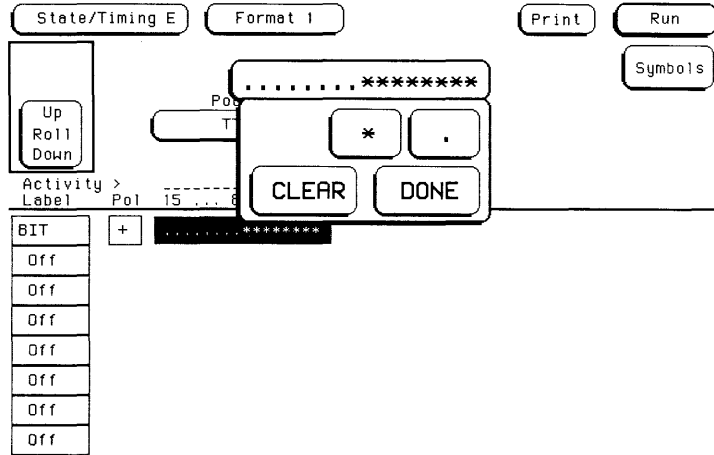
1. Get into either the timing or state Format specification menu using the method described in "Choosing Specification Menus" earlier in this chapter.
2. Touch one of the bit assignment fields.



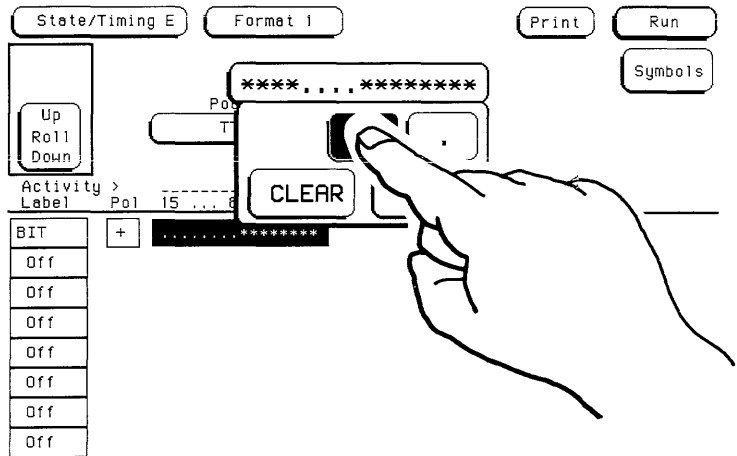
If you don't see any bit assignment fields, it simply means you don't have any pods assigned to this analyzer. Either switch analyzers or assign a pod to the analyzer with which you are working.



You will see the following pop-up menu.



3. Rotate the KNOB to place the cursor on any one of the asterisks or periods in the pop-up. To assign the bit, touch the field containing the asterisk. To un-assign the bit, touch the field with the period.



4. You close the pop-up by touching the DONE field.

Specifying Patterns

The Specify Pattern fields appear in several menus in both the timing and state analyzers. Patterns can be specified in one of several number bases. For now we'll use hexadecimal (HEX) since it is the default base.

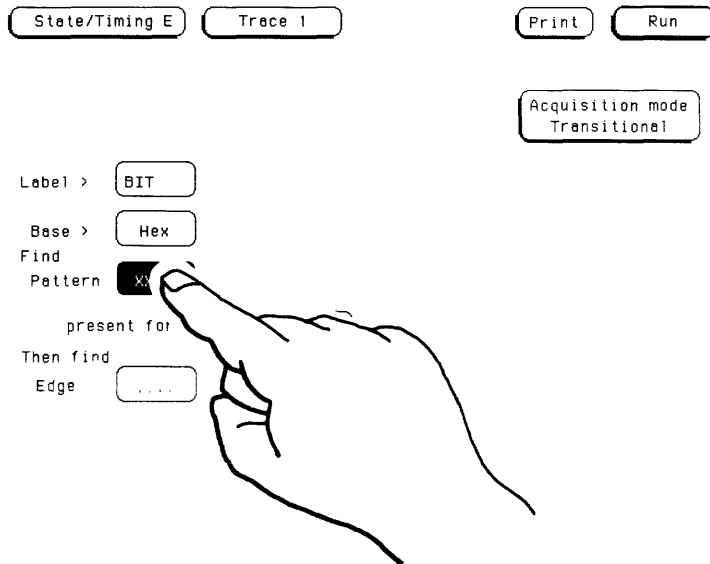
Before starting this exercise you need to know how the logic analyzer knows which patterns to ignore (doesn't care about). Whenever you see an "X" in this type of menu it indicates a "don't care."

To specify patterns:

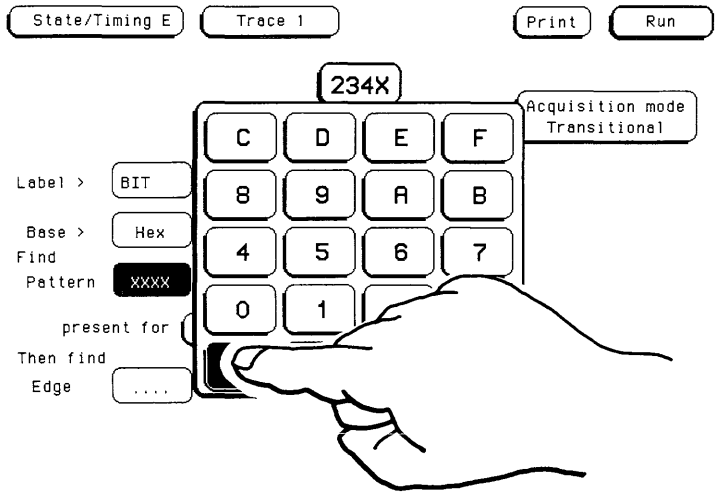
1. Get into the timing Trace specification menu.
2. Touch the field to the right of Find Pattern. A pop-up keyboard display will appear.



If the field does not contain four X's (representing don't cares) do not be alarmed. It simply means the number of bits in your label is different than the label in this example. Go to the timing Format specification menu and assign all the bits in the pod, using the method described in the previous section. Return to the timing Trace specification menu and continue.



3. On the pop-up keyboard, touch the keys 2, 3, 4, and X. You will see 234X in the display above. This will be the pattern in hexadecimal that you want the logic analyzer to recognize. If you make an error when entering a number, use the KNOB to position the cursor over the incorrect digit and touch the desired key.

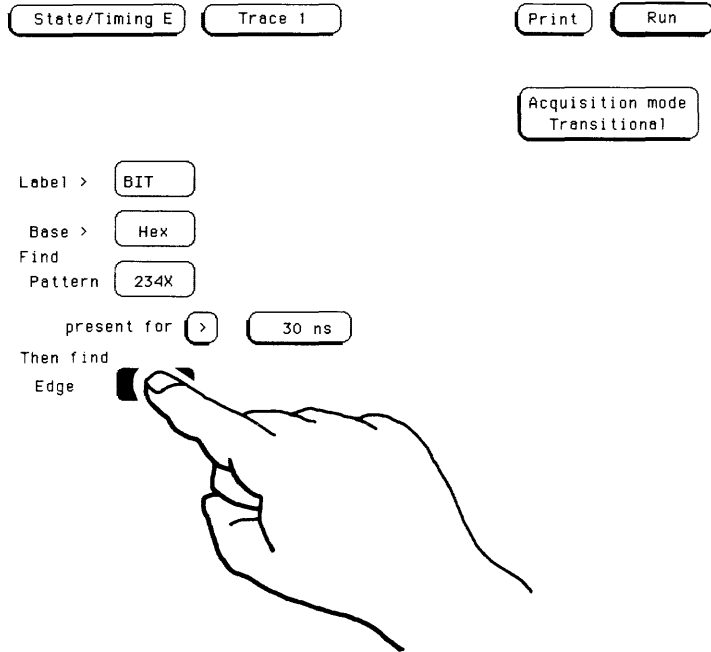


4. Close the pop-up keyboard display by touching the DONE field.

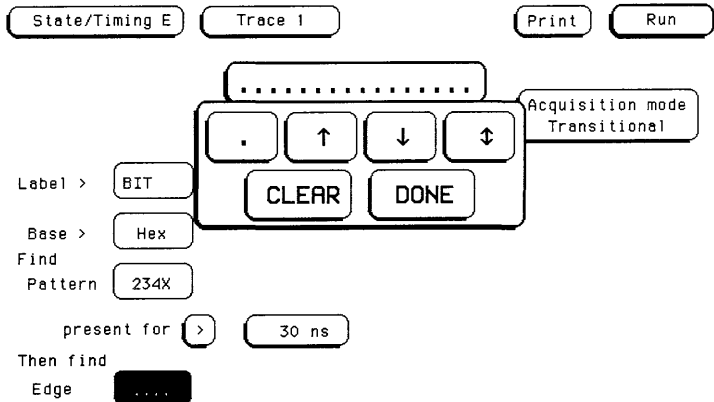
Specifying Edges

You specify edges in the timing Trace specification menu by following these steps:

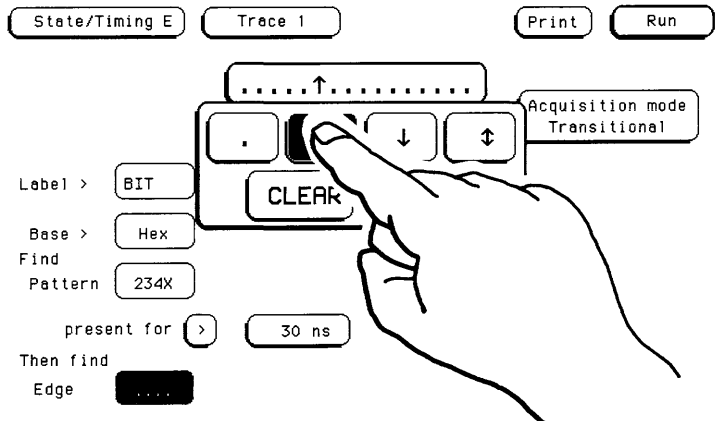
1. Get into the timing Trace specification menu.
2. Touch the field to the right of "Then Find Edge."



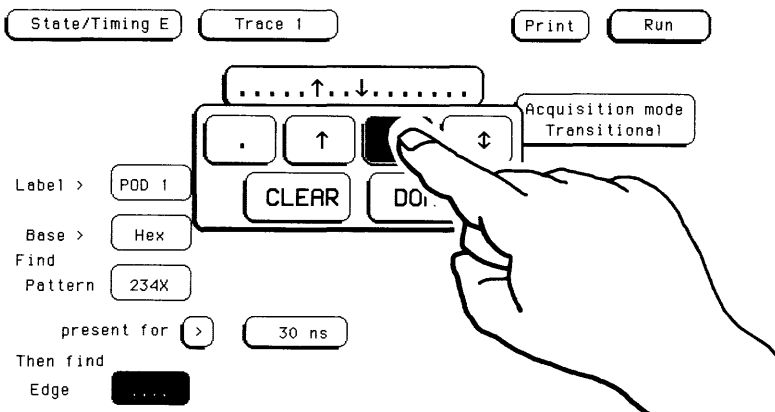
A pop-up menu will appear as shown below. You will notice 16 periods in the pop-up. Each period represents an unassigned edge for each bit assigned to the label. Don't be alarmed if you have a different number of unassigned edges; it simply means that the number of bits in your label is different than the label in this example.



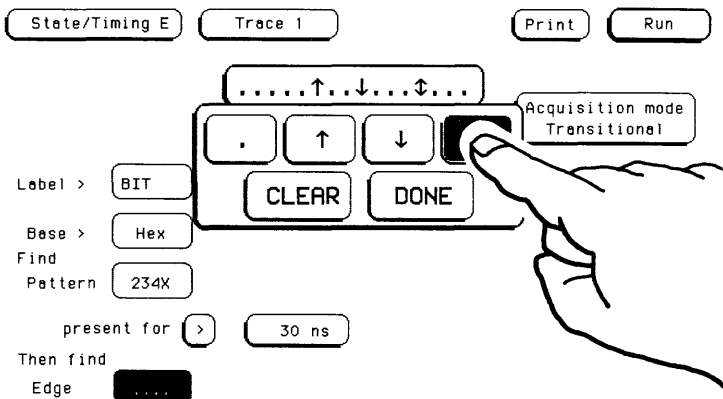
3. Use the KNOB to place the cursor on one of the unassigned edges. Touch the field with the arrow pointing up. The period is replaced with the arrow.



4. Move the cursor to another unassigned edge. Touch the field with the arrow pointing down. The period is replaced with the arrow.



5. Move the cursor to yet another unassigned edge. Touch the field with the arrow pointing both ways. The period is replaced with an arrow pointing both up and down.



You have just selected a positive-going (↑), negative-going (↓), and either edge (↑↓) for your edge parameter.

6. Touch the DONE field. The pop-up will close and you will see the following display.

State/Timing E Trace 1 Print Run

Acquisition mode
Transitional

Label > BIT

Base > Hex

Find
Pattern 234X

present for > 30 ns

Then find
Edge \$\$..



When you close the pop-up after specifying edges, you will see dollar signs (\$\$..) in the Then Find Edge field if the logic analyzer cannot display the data correctly in the number base you have selected.

Summary

In this chapter you have learned some of the most common pop-up menu types. You will use these pop-up menus as you set up the logic analyzer in the measurement example exercises in chapters 5 through 7.

If you are already familiar with logic analysis and feel you are comfortable enough with the HP 16500A interface, you may be ready for the *HP 16510B Front-Panel Reference*.

If you are not familiar with logic analyzers or logic analysis, you should continue with this guide.

Using the Timing Analyzer

Introduction

In this chapter you will learn how to use the timing analyzer by setting up the logic analyzer to make a simple measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized in a task format. The tasks are ordered in the same way you will most likely use them once you become an experienced user. The steps in this format are both numbered and lettered. The numbered steps state the step objective. The lettered steps explain how to accomplish each step objective. There is also an example of each menu after it has been properly set up.

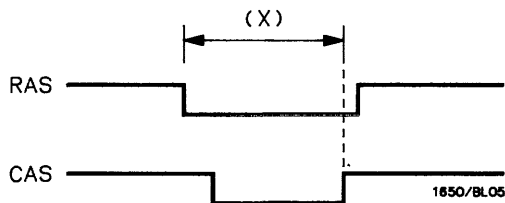
How you use the steps depends on how much you remember from chapters 3 and 4. If you can set up each menu by just looking at the menu picture, go ahead and do so. If you need a reminder of what steps you need to perform, follow the numbered steps. If you need still more information about "how," use the lettered steps.

Problem Solving with the Timing Analyzer

In this exercise, assume you are designing a dynamic RAM memory (DRAM) controller and you must verify the timing of the row address strobe (RAS) and the column address strobe (CAS). You are using a 4116 dynamic ram and the data book specifies that the minimum time from when LRAS is asserted (goes low) to when LCAS is no longer asserted (goes high) is 250 ns. You could use an oscilloscope but you have an HP 16500A with an HP 16510B module installed. Since the timing analyzer will do just fine when you don't need voltage parametrics, you decide to go ahead and use the logic analyzer.

What Am I Going to Measure?

After configuring the logic analyzer and hooking it up to your circuit under test, you will be measuring the time (x) from when the RAS goes low to when the CAS goes high, as shown below.

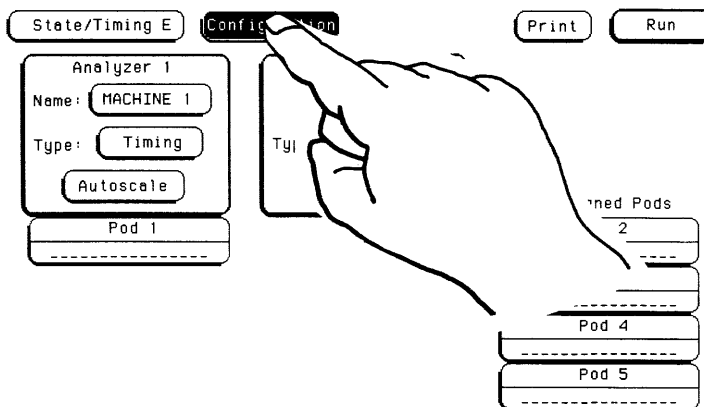


How Do I Configure the Logic Analyzer?

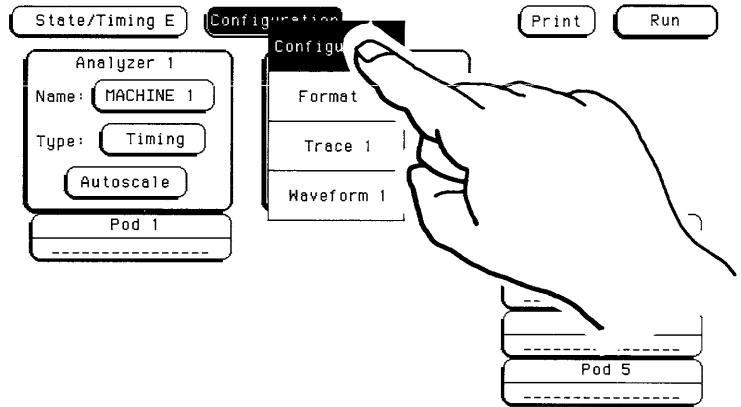
In order to make this timing measurement, you must configure the logic analyzer as a timing analyzer. By following these steps you will configure Analyzer 1 as the timing analyzer.

If you are in the analyzer Configuration menu, you are already in the right place and can start with step 2; otherwise, start with step 1.

1. Display the analyzer Configuration menu.
 - a. If you are in the State/Timing Analyzer module, go on to step b.
 - b. Touch the field in the top left corner. When the pop-up appears, touch the field labeled State/Timing E.
- b. Touch the field second from the left at the top of the screen.

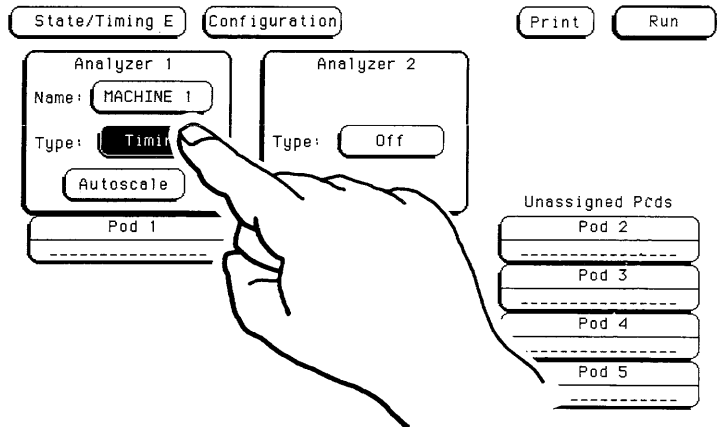


c. When the pop-up appears, touch the field labeled "Configuration."

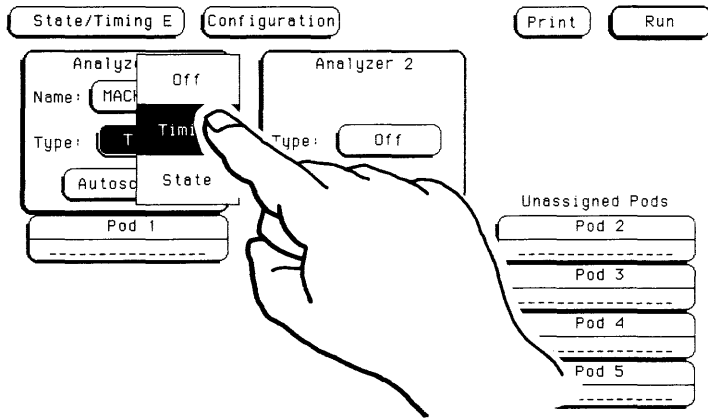


2. In the Configuration menu, change Analyzer 1 Type to Timing. If analyzer 1 is already a timing analyzer, go on to step 3.

a. Touch the field to the right of Type: _____.

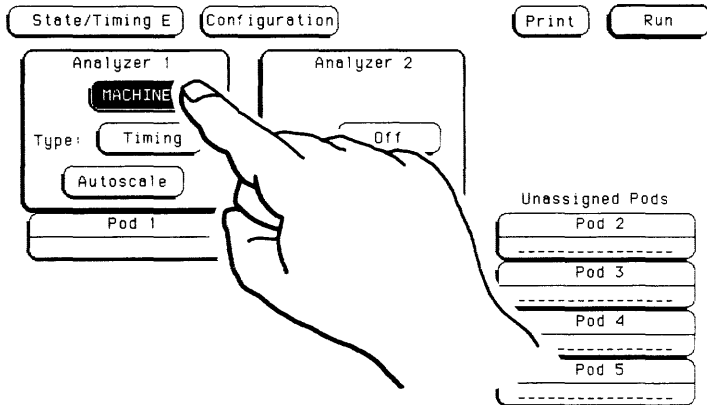


b. Touch the field labeled Timing.

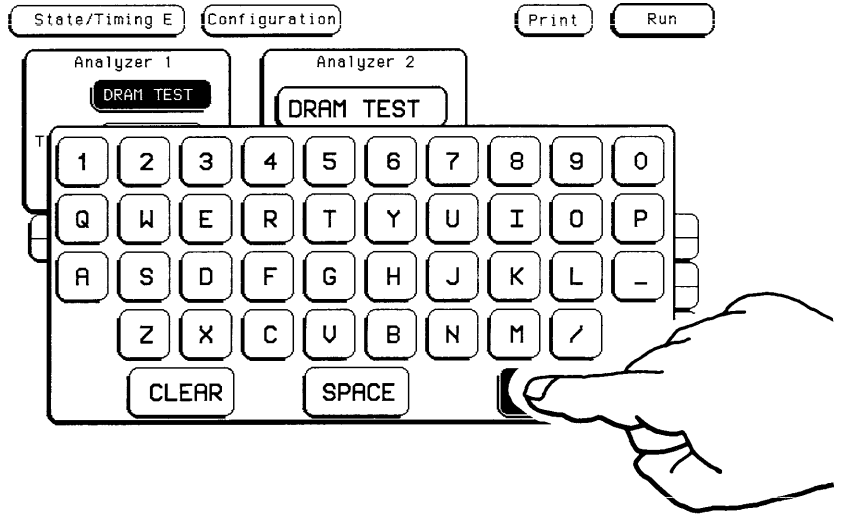


3. Name analyzer 1 "DRAM TEST" (optional)

a. Touch the field to the right of Name: _____ under Analyzer 1.

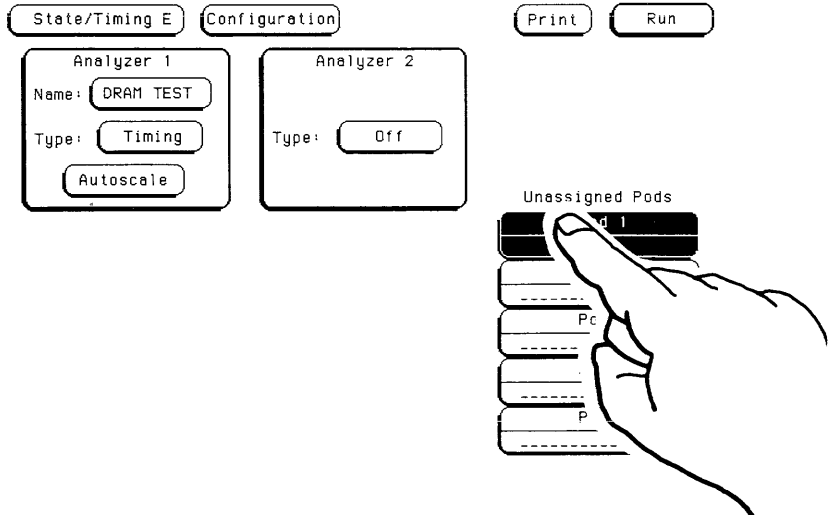


- b. When the alphanumeric keyboard pop-up appears, touch the appropriate keys to change the name to "DRAM TEST" (see "Alpha Entry Pop-up Menu" in Chapter 4 if you need a reminder).

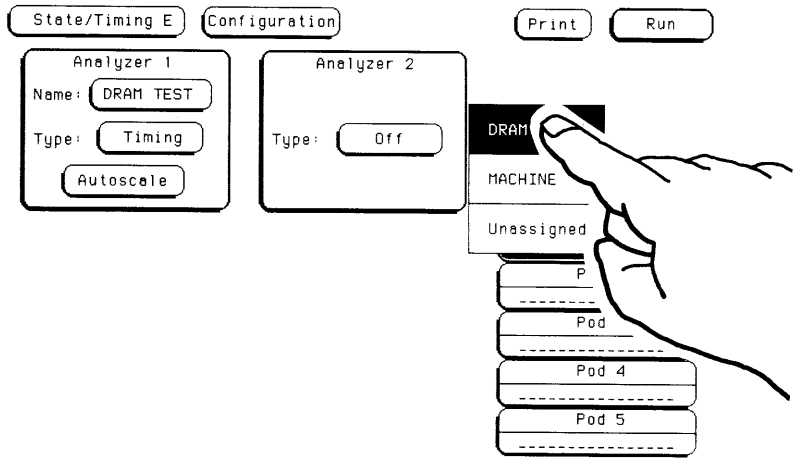


4. Assign pod 1 to the timing analyzer if it is not already assigned or if it is assigned to analyzer 2.

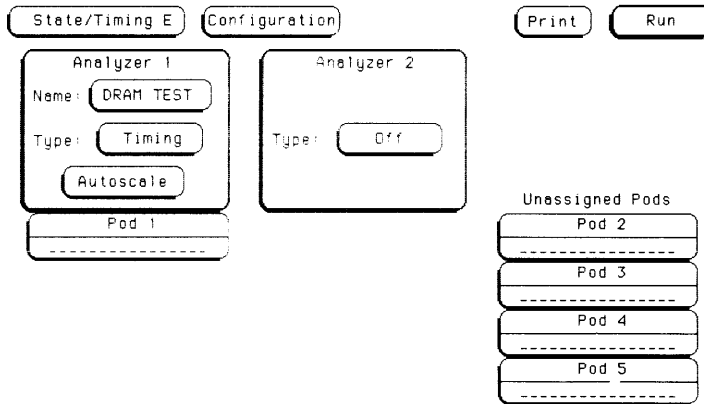
- a. Touch the Pod 1 field.



b. In the Pod 1 pop-up, touch the field labeled DRAM TEST (or Machine 1 if you didn't name the analyzer DRAM TEST).



The analyzer Configuration menu should look like that shown below.

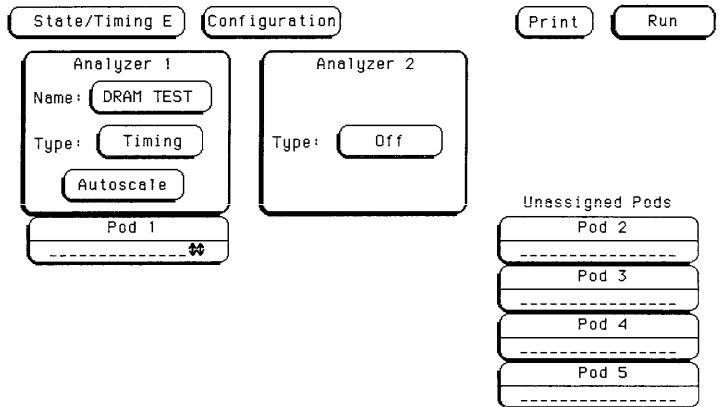


Connecting the Probes

At this point, if you had a target system with a 4116 DRAM memory IC, you would connect the logic analyzer to your system. Since you will be assigning Pod 1 bit 0 to the RAS label, you hook Pod 1 bit 0 to the memory IC pin connected to the RAS signal. You hook Pod 1 bit 1 to the IC pin connected to the CAS signal.

Activity Indicators

When the logic analyzer is connected and your target system is running, you will see two ↑ at the right-most end (least significant bits) of the Pod 1 field in the analyzer Configuration menu. This indicates that the RAS and CAS signals are transitioning.



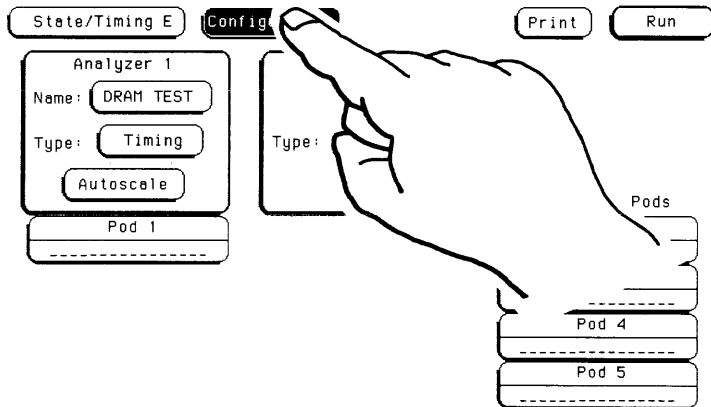
Configuring the Timing Analyzer

Now that you have configured the logic analyzer module, you are ready to configure the timing analyzer. You will:

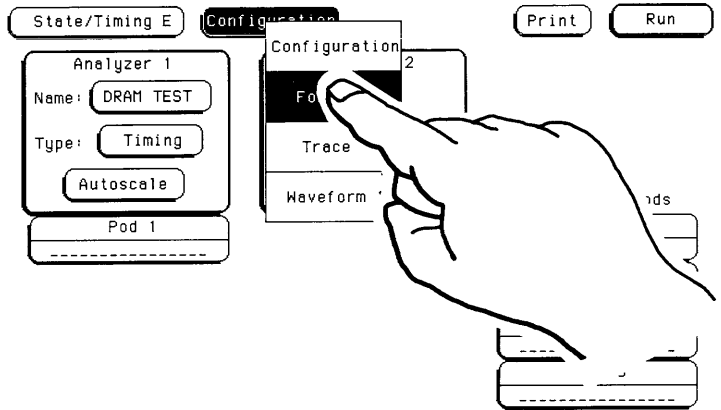
- Create two names (labels) for the input signals
- Assign the channels connected to the input signals
- Specify a trigger condition

1. Display the timing Format (Format 1) specification menu.

a. Touch the field second from the left at the top of the screen.

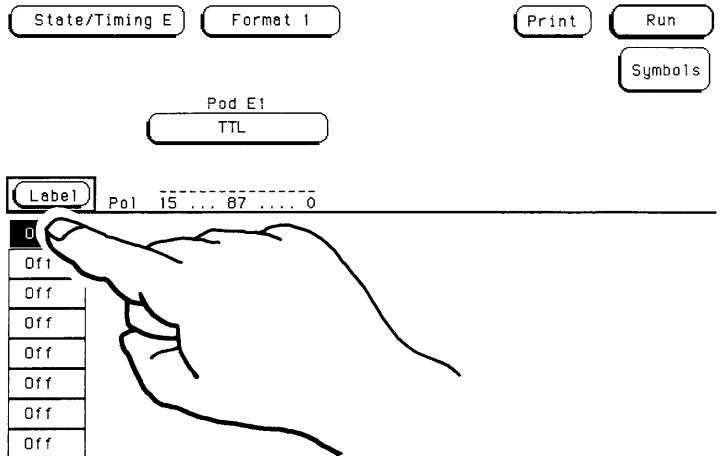


- b. Touch the field labeled Format 1. This gets you to the Format specification menu of analyzer 1, which you have configured as a timing analyzer.

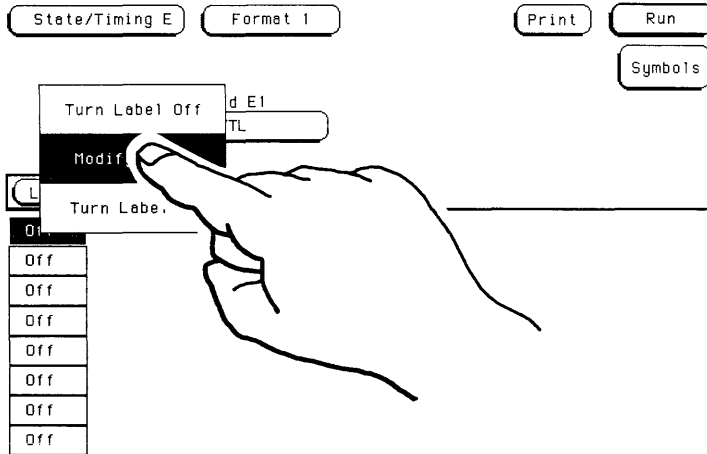


2. Name two labels, one RAS and one CAS.

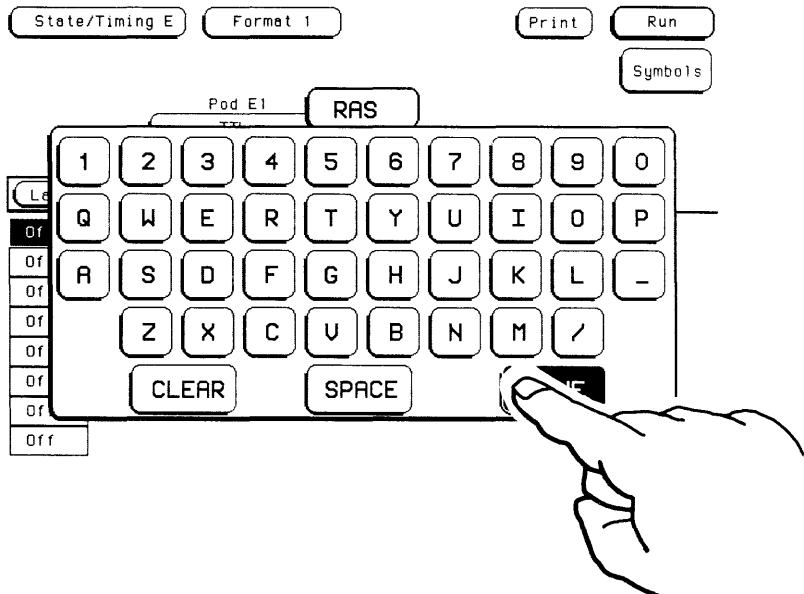
- a. Touch the top field in the label column.



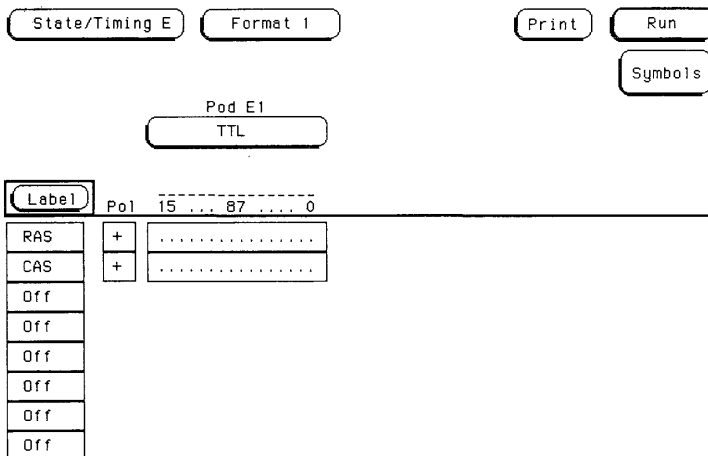
b. In the pop-up, touch the Modify Label field.



c. With the alphanumeric keyboard, change the name of the label to RAS (see "Alpha Entry Pop-up Menu" in Chapter 4 if you need a reminder).

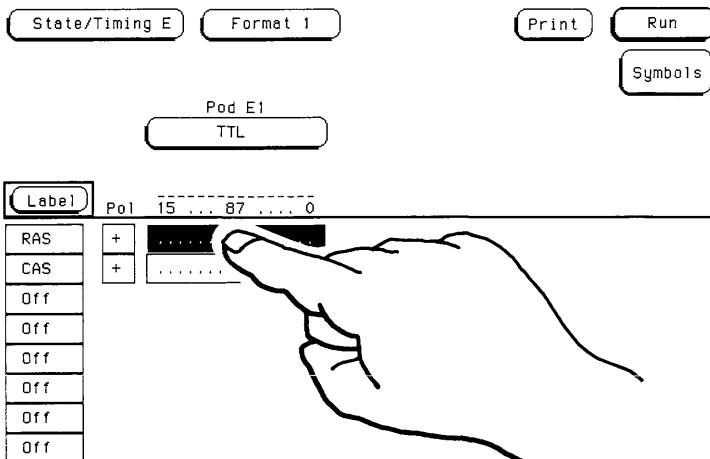


d. Name the second label CAS by touching the second field in the label column and then repeating steps b and c. The timing Format specification with the labels is shown below.

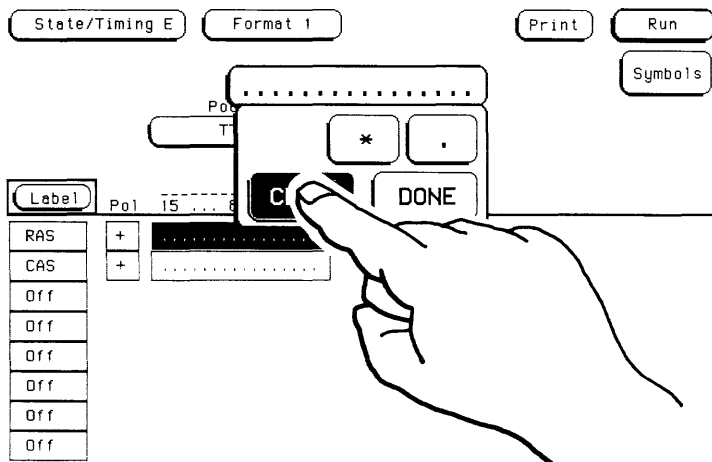


3. Assign the channels connected to the input signals (Pod 1 bits 0 and 1) to the labels RAS and CAS, respectively.

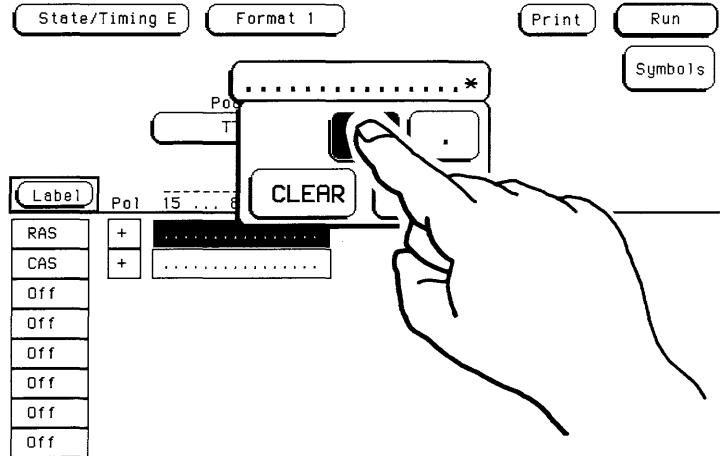
a. Touch the bit assignment field below Pod 1 and to the right of RAS.



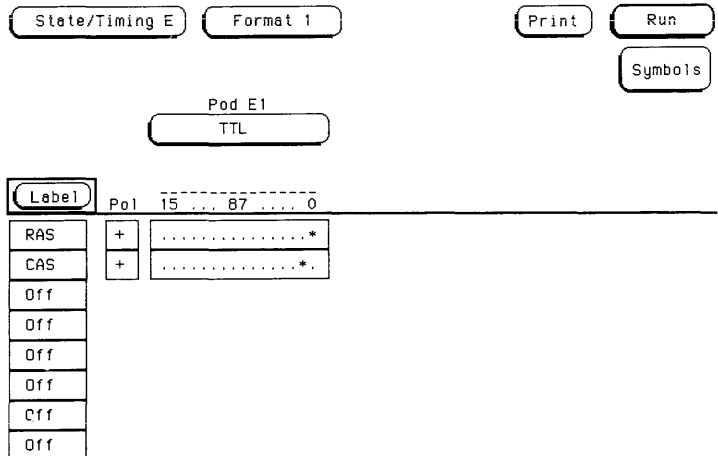
- b. Any combination of bits may be already assigned to this pod; however, you will want only bit 0 assigned to the RAS label. The easiest way to assign bits is to press the CLEAR field to unassign any assigned bits before you start.



- c. Use the KNOB to position the cursor on bit 0. This is the bit on the far right end of the bit assignment field. Touch the asterisk field. This places an asterisk in the pop-up for bit 0 indicating that Pod 1 bit 0 is now assigned to the RAS label. Touch the DONE field to close the pop-up.



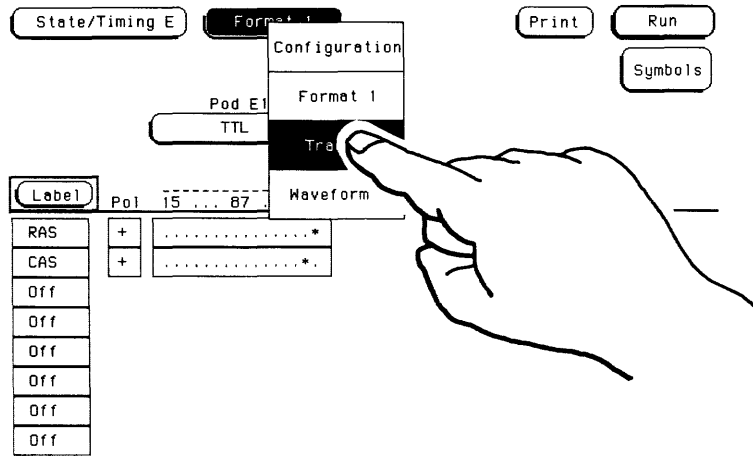
- d. Assign Pod 1 bit 1 to the CAS label by repeating steps a through c for bit 1. The resulting timing Format menu is shown below.



Specifying a Trigger Condition

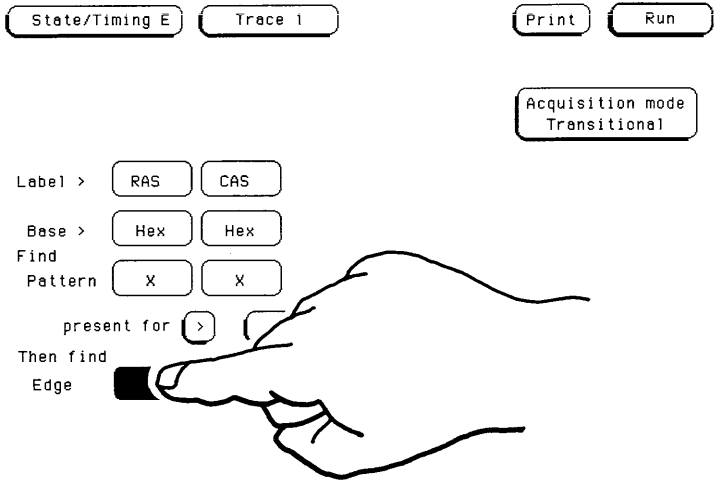
To capture and place the data of interest in the center of the Timing waveform menu display, you need to tell the logic analyzer when to trigger. Since the first event of interest is when the LRAS is asserted (negative-going edge of RAS), you need to tell the logic analyzer to trigger on a negative-going edge of the RAS signal.

1. Display the timing Trace specification menu.
 - a. Touch the field second from the left at the top of the screen.
 - b. When the pop-up appears, touch the field labeled "Trace 1."

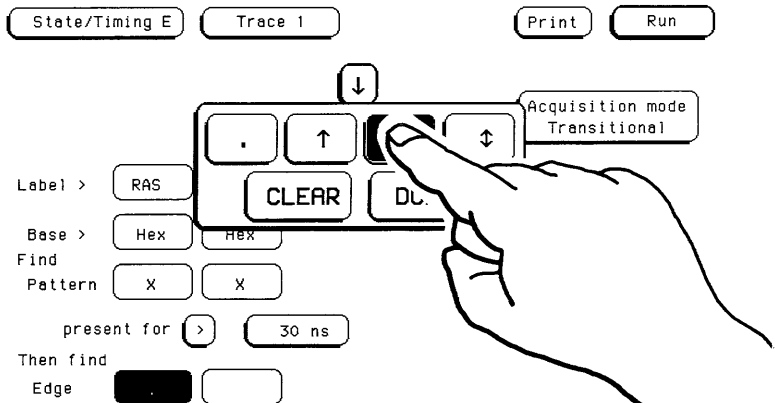


2. Set the trigger so that the logic analyzer triggers on the negative-going edge of the RAS signal.

a. Touch the field to the right of Then Find Edge and under the label "RAS."



b. In the pop-up, touch the field with the arrow pointing down. This replaces the period with the arrow, indicating a negative-going edge.



c. Touch the DONE field. The pop-up closes and a ↓ is located in the Then Find Edge field. The ↓ indicates that a negative-going edge has been specified.

State/Timing E Trace 1 Print Run

Acquisition mode
Transitional

Label > RAS CAS

Base > Hex Hex

Find
Pattern X X

present for > 30 ns

Then find
Edge ↓ .

Acquiring the Data

Now that you have configured and connected the logic analyzer, you can acquire the data for your measurement. To do so, first display the timing Waveform menu:

1. Touch the field second from the left at the top of the screen.
2. When the pop-up appears, touch the field labeled "Waveform 1."

State/Timing E Trace 1 Print Run

Acquisition mode
Transitional

Label > RAS CAS

Base > Hex Hex

Find
Pattern X X

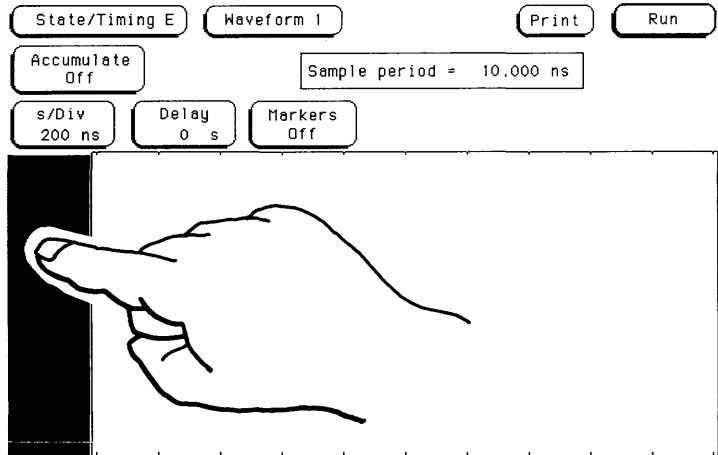
present for > 30 ns

Then find
Edge ↓ .

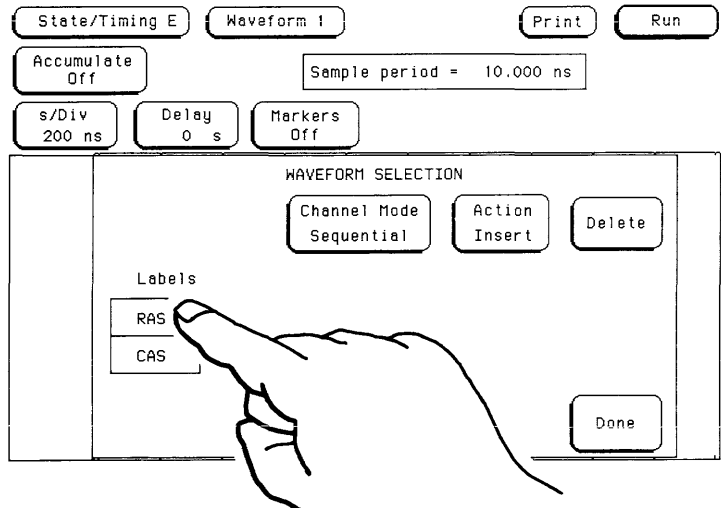
Configuration
Format 1
Trace 1
Waveform 1

If this is the first time you acquire data and you have not previously set up the timing Waveform menu, you will get a blank area at the bottom of the display. You need to turn on the RAS and CAS labels. To do so, follow these steps:

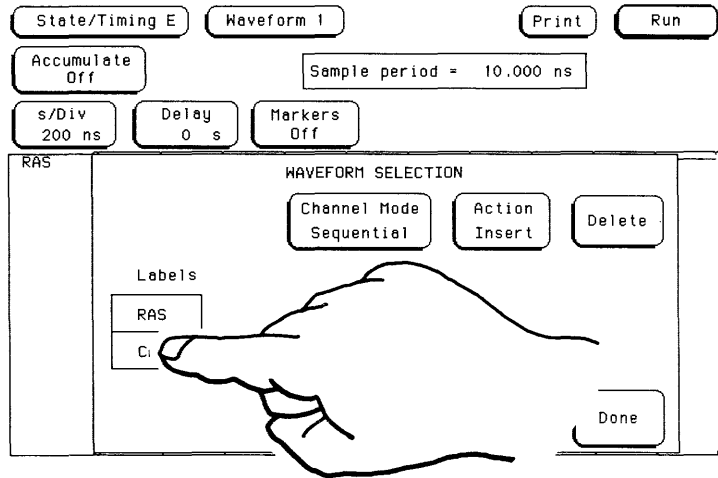
1. Touch the long blue field on the left side of the screen.



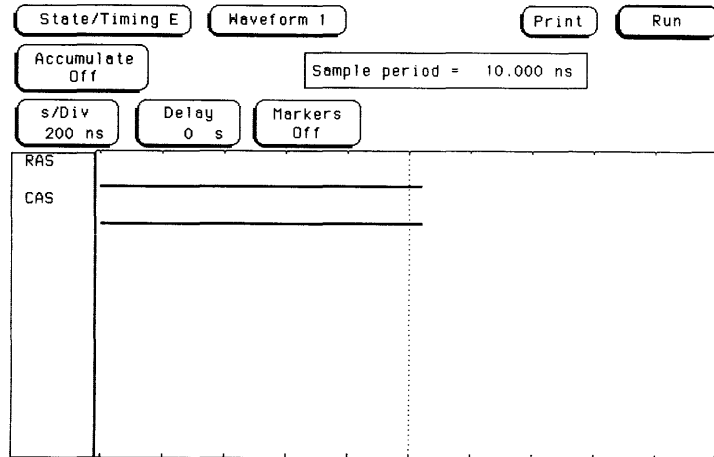
2. In the pop-up, touch the field labeled "RAS" located under Labels. The label RAS appears at the top of the long blue field.



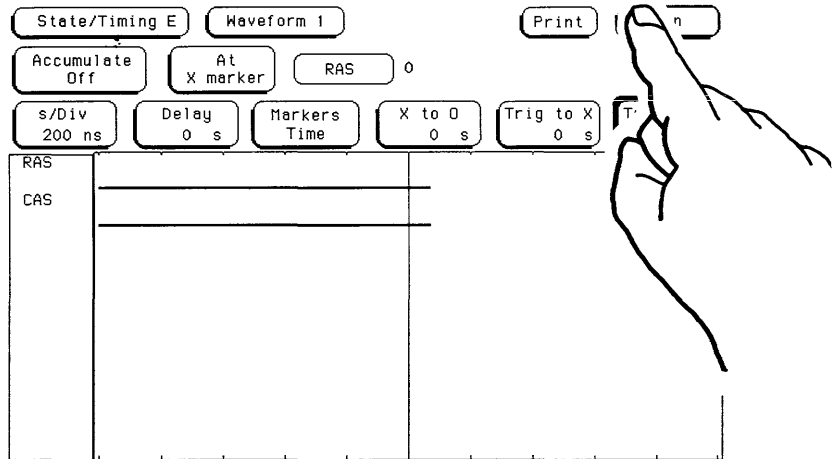
3. Touch the field labeled "CAS" located under Labels. The label CAS appears in the long blue field under RAS.



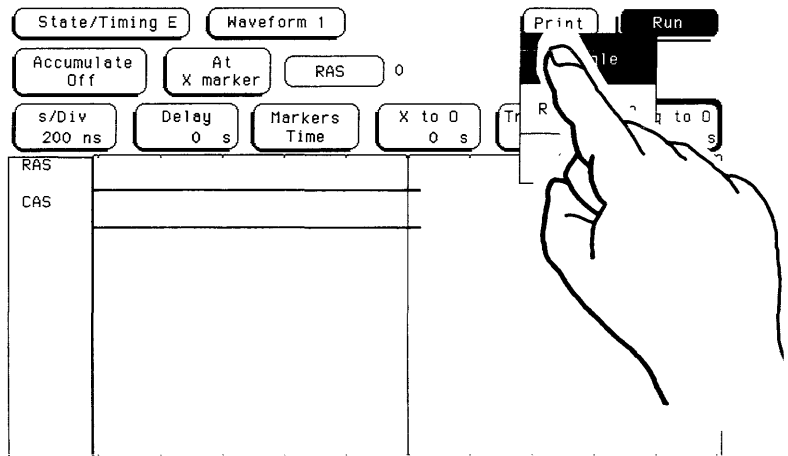
4. Touch the DONE field to close the pop-up.



To acquire the data, touch the green field in the upper right-hand corner labeled "Run." Do not lift your finger off the screen.



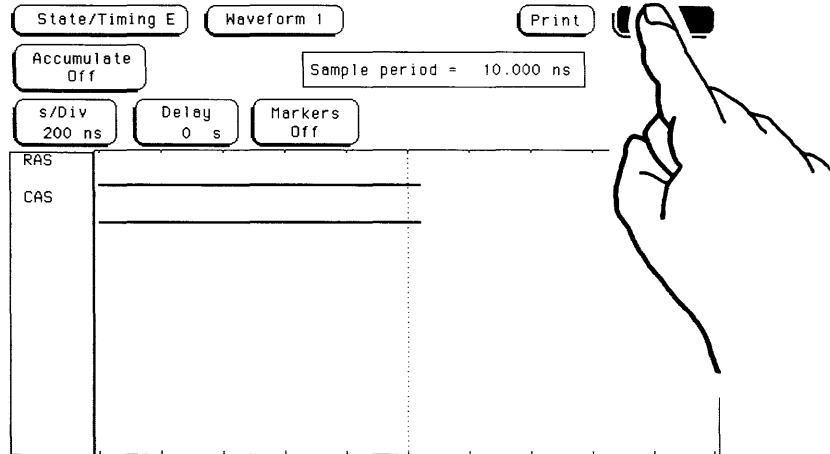
When you touch the Run field a pop-up appears next to it with the options Single, Repetitive and Cancel. With your finger still on the screen, move to the field labeled Single. It will turn white, indicating that it has been selected.



Note 

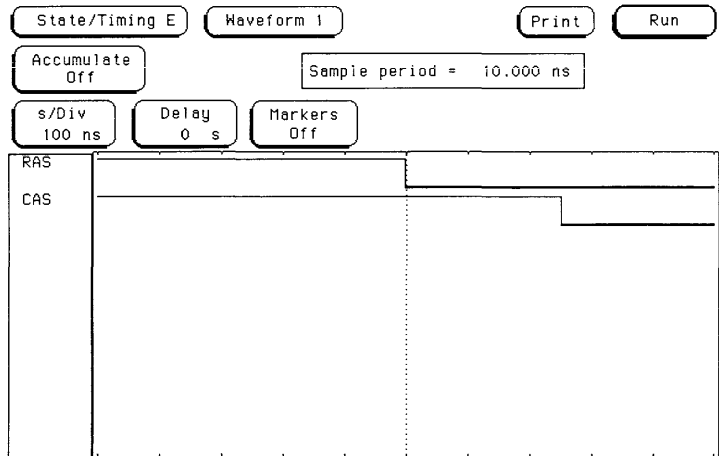
The Run field appears in, and can be activated from every specification menu. However, if the timing Waveform menu has not previously been set up, you need to display the Waveform menu as described above and get it ready. Thereafter, you can Run a test from any specification menu.

While the logic analyzer is acquiring data, the Run field changes color from green to red, and instead of Run it says Stop. This allows you to stop the data acquisition at any time just by touching this field.



If you select Cancel, the logic analyzer will return to the state it was in before the Run field was touched.

When you touch Run, the logic analyzer will look for a negative edge on the RAS signal and trigger if it sees one. When it triggers waveforms appear on the display.



The RAS label shows you the RAS signal and the CAS label shows you the CAS signal. Notice the RAS signal goes low at or near the center of the waveform display area (horizontal center).

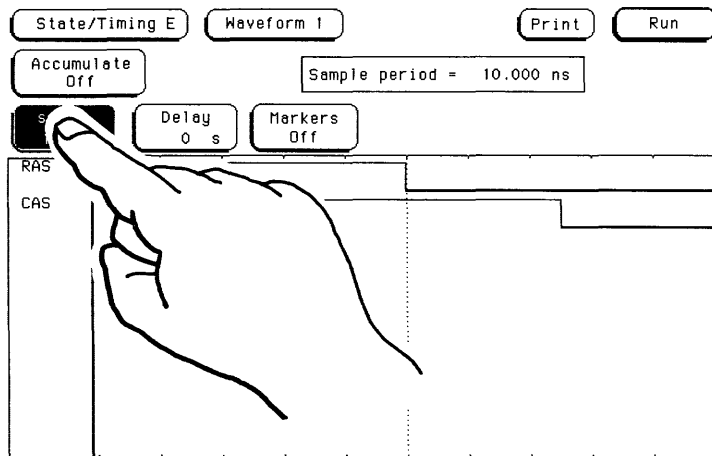
The Timing Waveform Menu

The timing Waveform menu differs from the other menus you have used so far in this exercise. Besides displaying the acquired data, it has menu fields that you can use to change the way the acquired data is displayed, such as *s/Div*, and fields that give you timing answers, such as the *Markers* field. These will now be discussed.

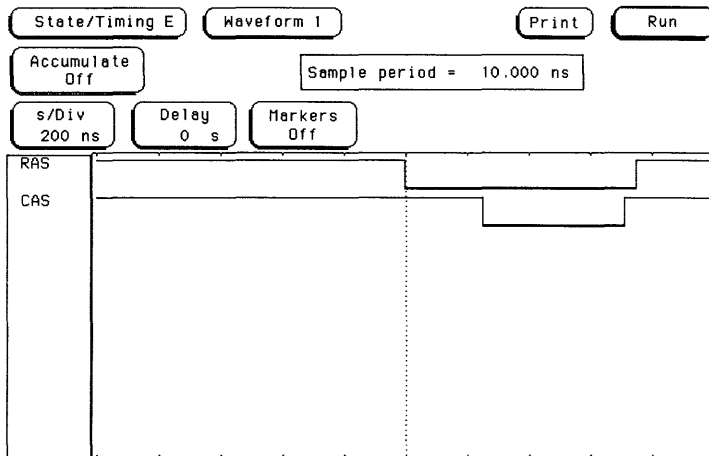
Display Resolution

You get the best resolution by changing the *s/Div* to a value that displays one negative-going and one positive-going edge of both the RAS and CAS waveforms. Set the *s/Div* by following these steps:

1. If the s/Div field is already light blue, go on to step 2. If it is not light blue, touch the field.



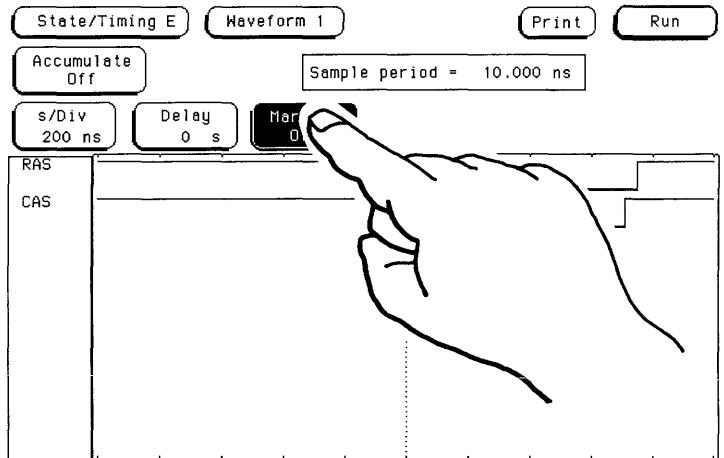
2. The light blue color of the field indicates that the value can be changed with the KNOB or by touching the field to get a pop-up keypad. For this exercise, rotate the KNOB until your waveform shows you only one negative-going edge of the RAS waveform and one positive-going edge of the CAS waveform. In this example 200 ns is best.



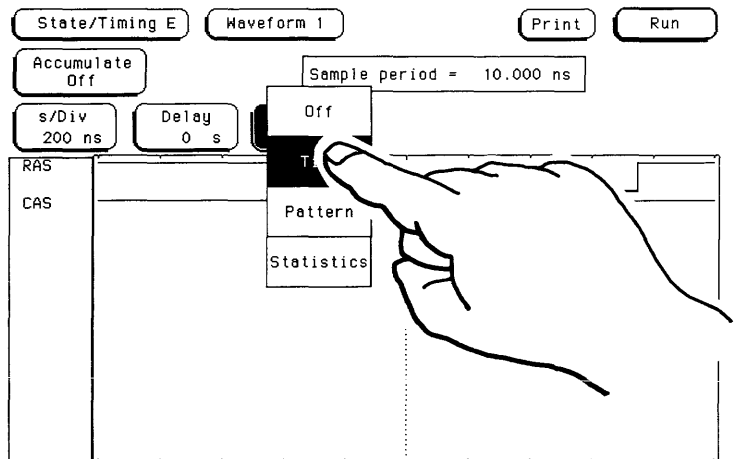
The Timing Markers

The logic analyzer supplies two markers that you can use to make timing measurements. One is called the X marker and the other is the O marker. You place them on the points of interest on your waveforms, and the logic analyzer displays the time between the markers. To turn the timing markers on:

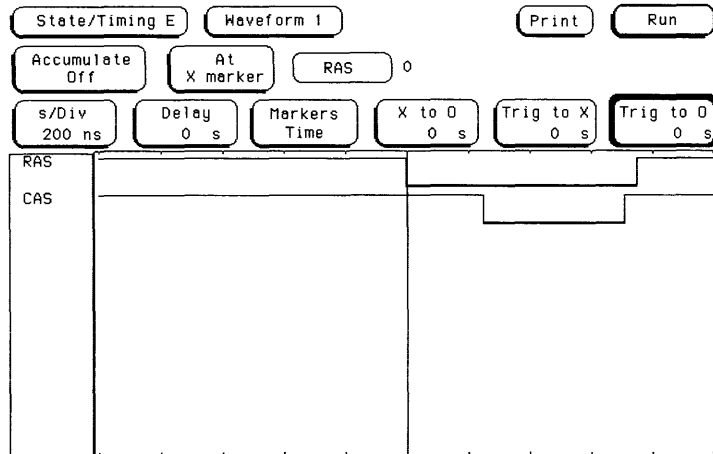
1. Touch the field third from the left, third row down from the top of the display. It should say "Markers Off."



2. In the pop-up, touch the field labeled "Time." This closes the pop-up and turns the timing markers on.



Three more fields will appear on the screen next to the Markers field. The first one tells you the time between the X and O markers. The second field, which is outlined in green, tells you the time from the X marker to the trigger point. The third field, which is outlined in yellow, tells you the time from the O marker to the trigger point.

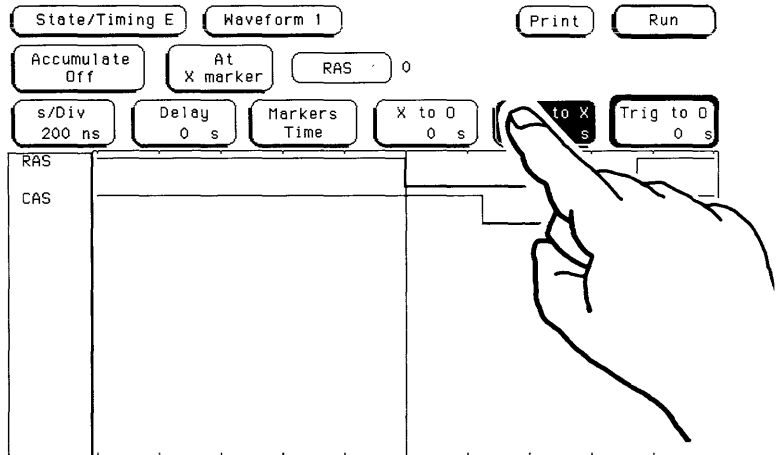


You will also see a multi-colored line down the center of the waveforms display area. This line is actually made up of three lines: a red line, a yellow line, and a green line. The green line is the X marker, and the yellow line is the O marker. The red line indicates the trigger point you specified in the timing Trace specification menu. Notice that it is superimposed on the negative-going edge of the RAS signal.

Making the Measurement

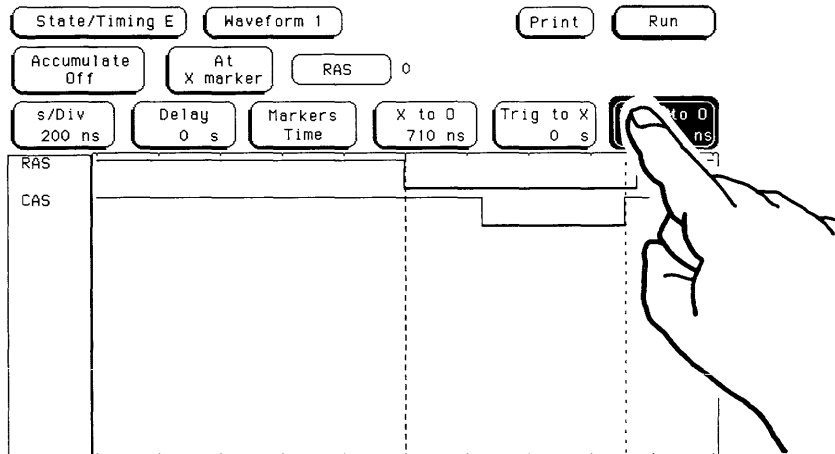
What you want to know is how much time elapses between the time RAS goes low and the time CAS goes high again. You will use the X and O markers to quickly find the answer. Remember that you specified the negative-going edge of the RAS to be your trigger point. Therefore, the X marker should be on this edge if Trig to X = 0. If not, follow steps 1 and 2.

1. Touch the field labeled "Trig to X." This turns the field light blue. Remember that a light blue field means that the value can be changed with the KNOB or by touching the field to get a pop-up keypad. For this exercise we'll use the KNOB.

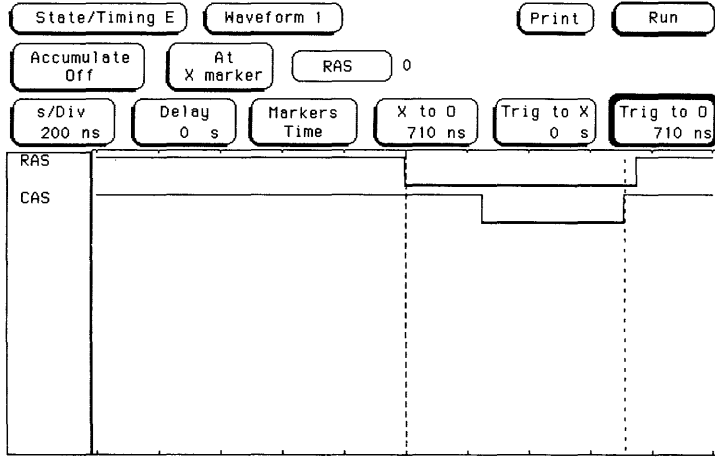


2. Rotate the KNOB to place the X marker (green line) on the negative-going edge of the RAS waveform. The field should read "Trig to X = 0 s."

3. Touch the field labeled "Trig to O." This field should now be light blue. Use the KNOB to place the O marker (yellow line) on the positive-going edge of the CAS waveform. The field should now read "Trig to O = 710 ns."



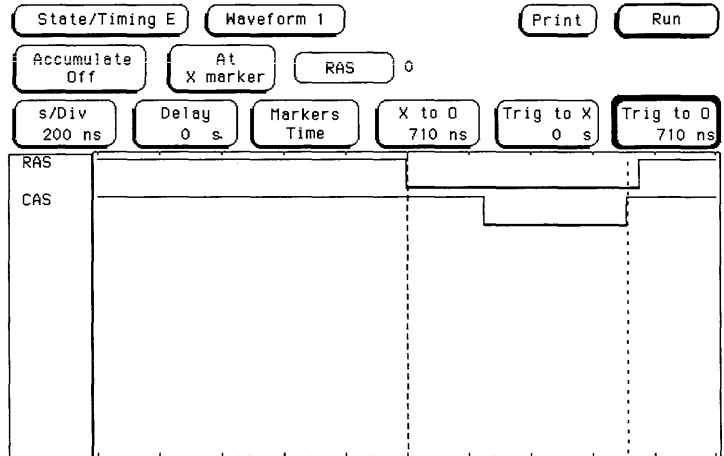
The timing Waveform menu should look like that shown below.



Finding the Answer

The time elapsed between the time RAS goes low and the time CAS goes high can be calculated by adding the Trig to X time and the Trig to O time, but there is no need. The logic analyzer has already calculated this answer and displays it in the X to O field on the display.

This example indicates that the time is 710 ns. Since the data book specifies a minimum of 250 ns, it appears your DRAM controller circuit is designed properly.



Summary

You have just learned how to make a simple timing measurement with the HP 16510B Logic Analyzer module in the HP 16500A. You have:

- specified a timing analyzer
- assigned pod 1
- assigned bits
- assigned labels
- specified a trigger condition
- learned which probes to connect
- acquired the data
- configured the display
- set the *s/Div* for best resolution
- positioned the markers for the measurement answer

You have seen how easy it is to use the timing analyzer to make timing measurements which you could have made with an oscilloscope. You can use the timing analyzer for any timing measurement that neither requires voltage parametrics nor surpasses the accuracy of the timing analyzer.

The next chapter teaches you how to use the state analyzer. You will go through a simple state measurement in the same way you did the timing measurement in this chapter.

Using the State Analyzer

Introduction

In this chapter you will learn how to use the state analyzer by setting up the logic analyzer to make a simple state measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized in a task format. The tasks are ordered in the same way you will most likely use them once you become an experienced user. The steps in this format are both numbered and lettered. The numbered steps state the step objective. The lettered steps explain how to accomplish each step objective. There is also an example of each menu after it has been properly set up.

How you use the steps depends on how much you remember from chapters 3 and 4. If you can set up each menu by just looking at the menu picture, go right ahead and do so. If you need a reminder of what steps you need to perform, follow the numbered steps. If you still need more information about "how," use the lettered steps.

Problem Solving with the State Analyzer

In this example assume you have designed a microprocessor controlled circuit. You have completed the hardware and the software designer has completed the software and programmed the ROM (read-only memory). When you turn your circuit on for the first time your circuit doesn't work properly. You have checked the power supply voltages and the system clock and they are working properly.

Since the circuit has never worked before, you and the software engineer aren't sure if it is a hardware or a software problem. The problem now requires some testing to find a solution.

What Am I Going to Measure?

You decide to start where the microprocessor starts when power is applied. We will describe a 68000 microprocessor; however, every processor has similar start-up routines.

When you power up a 68000 microprocessor it is held in reset for a specific length of time before it starts doing anything to stabilize the power supplies. This time during which the microprocessor is held in reset ensures stable levels (states) on all the devices and buses in your circuit. When this reset period has ended, the 68000 performs a specific routine called "fetching the reset vector."

The first thing you check is the time the microprocessor is held in reset. You find that the time is correct. The next thing to check is whether the microprocessor fetches the reset vector properly.

The steps of the 68000 reset vector fetch are:

1. Set the stack pointer to a location you specify which is in ROM at address locations 0 and 2.
2. Find the first address location in memory where the microprocessor fetches its first instruction. This is also specified by you and stored in ROM at address locations 4 and 6.

What you decide to find out is:

1. What ROM address does the microprocessor look at for the location of the stack pointer, and what is the stack pointer location stored in ROM?
2. What ROM address does the microprocessor look at for the address where its first instruction is stored in ROM, and is the instruction correct?
3. Does the microprocessor then go to the address where its first instruction is stored?
4. Is the executable instruction stored in the first instruction location correct?

Your measurement, then, requires verification of the sequential addresses the microprocessor looks at and of the data in ROM at these addresses. If the reset vector fetch is correct (in this example) you will see the following list of numbers in HEX (default base) when your measurement results are displayed:

0	000000	0000
1	000002	04FC
2	000004	0000
3	000006	8048
4	008048	3E7C

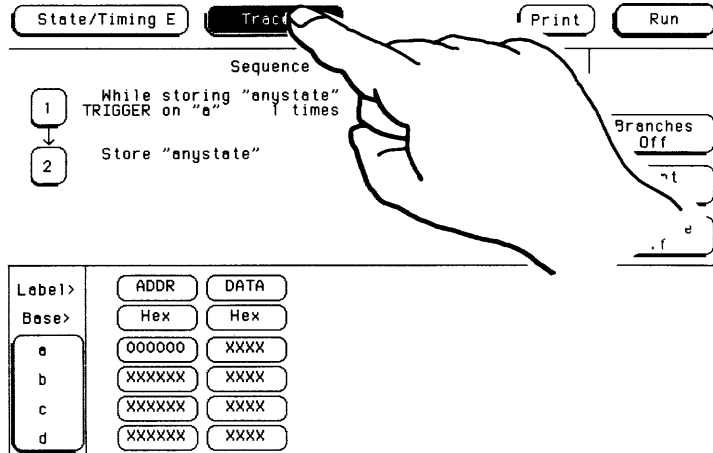
This list of numbers will be explained in detail later in this chapter in "The State Listing."

How Do I Configure the Logic Analyzer?

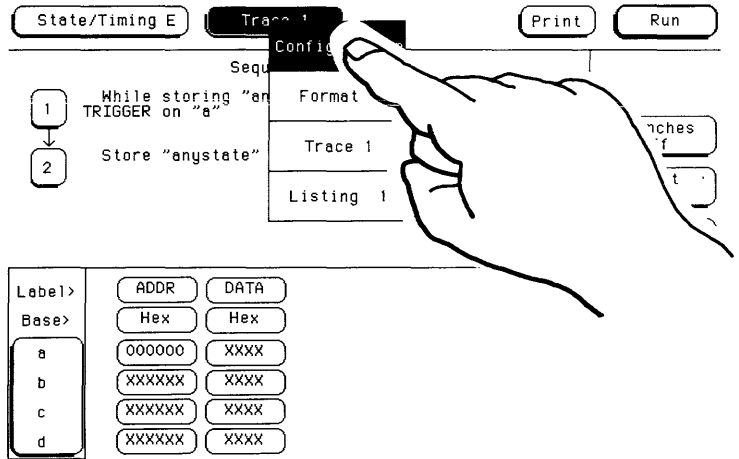
In order to make this state measurement, you must configure the logic analyzer as a state analyzer. By following these steps you will configure Analyzer 1 as the state analyzer.

If you are in the analyzer Configuration menu you are in the right place and can start with step 2; otherwise, start with step 1.

1. Display the analyzer Configuration menu.
 - a. If you are in the State/Timing Analyzer mode, go on to step b. If you are in another mode (i.e. operating from a different module), refer to "Moving to the Logic Analyzer" in Chapter 3 to see how to get to the analyzer mode.
 - b. Touch the field second from the left at the top of the screen.

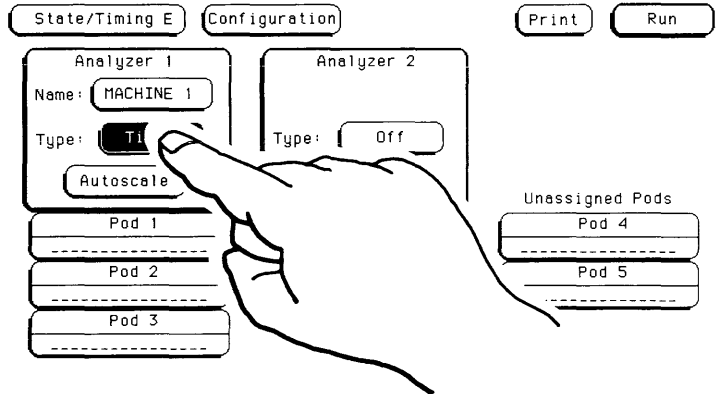


c. When the pop-up appears, touch the field labeled "Configuration".

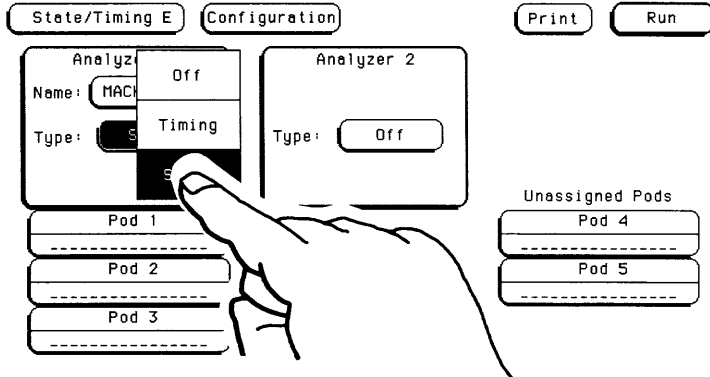


2. In the analyzer Configuration menu, change the Analyzer 1 type to State. If Analyzer 1 is already a state analyzer, go on to step 3.

a. Touch the field to the right of Type: ____.

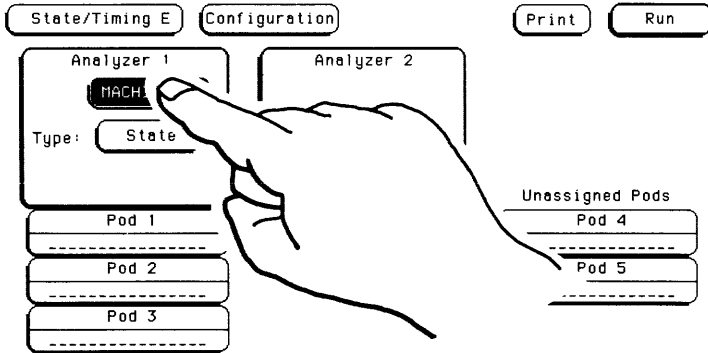


b. Touch the field labeled "State".

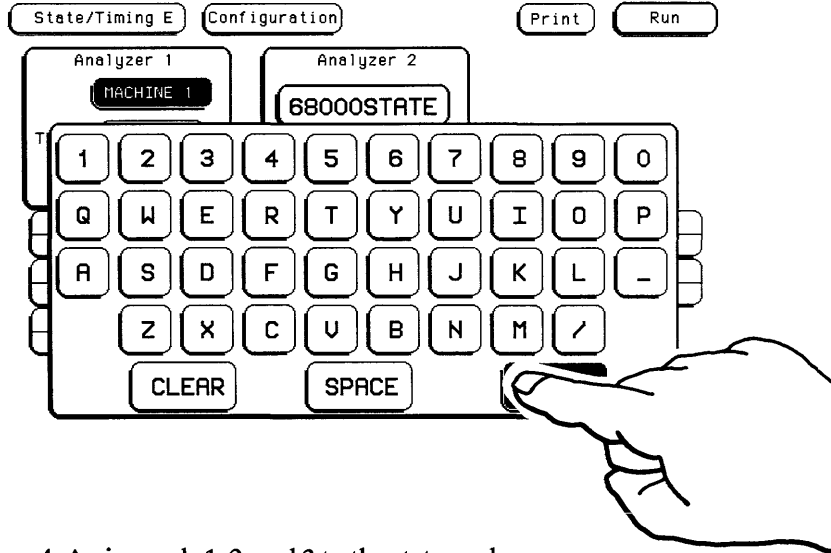


3. Name analyzer 1 68000STATE (optional).

a. Touch the field to the right of Name: _____.

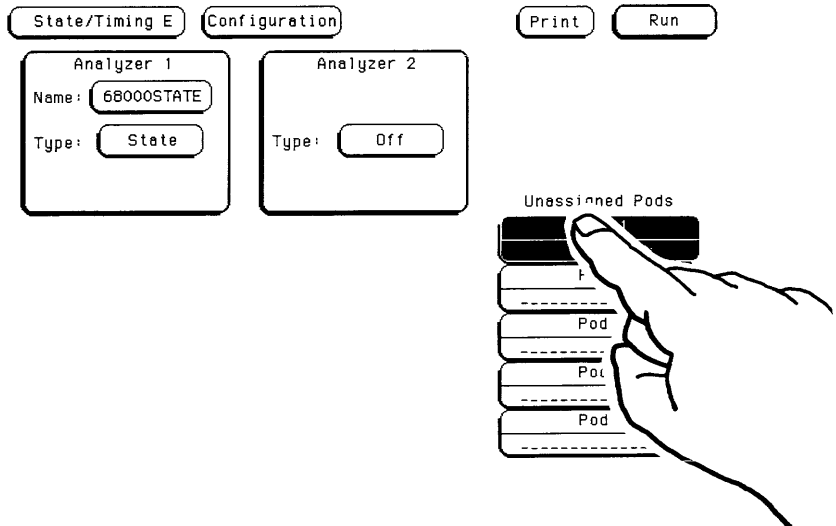


- b. When the alphanumeric keyboard pop-up appears, touch the appropriate keys to change the name to 68000STATE (see "Alpha Entry Pop-up Menu" in Chapter 4 if you need a reminder).

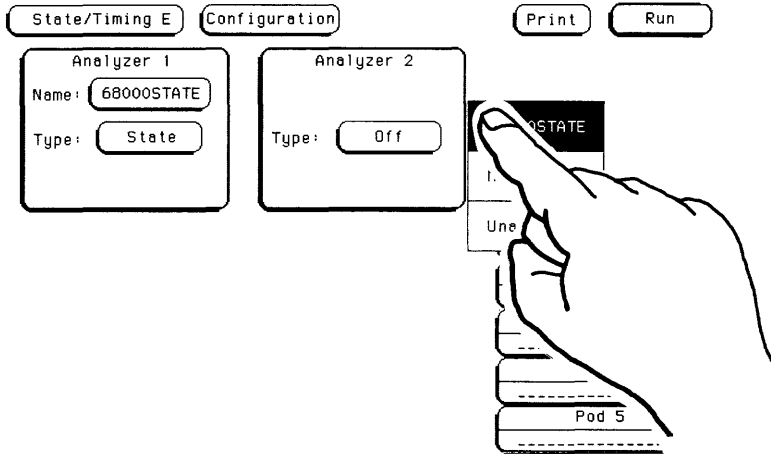


4. Assign pods 1, 2, and 3 to the state analyzer.

- a. Touch the Pod 1 field.

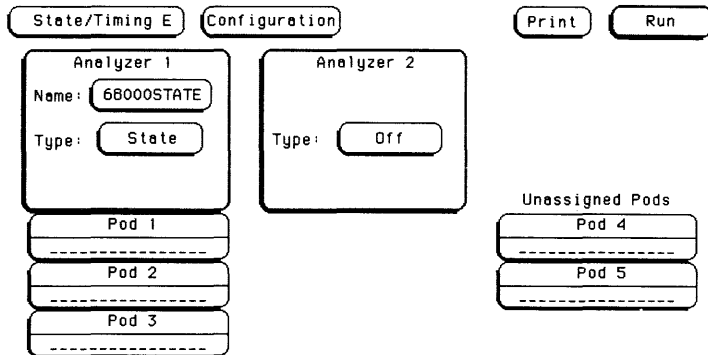


b. In the Pod 1 pop-up, touch the field labeled "68000STATE".



c. Repeat steps a and b for pods 2 and 3.

The analyzer Configuration menu should look similar to that shown below.



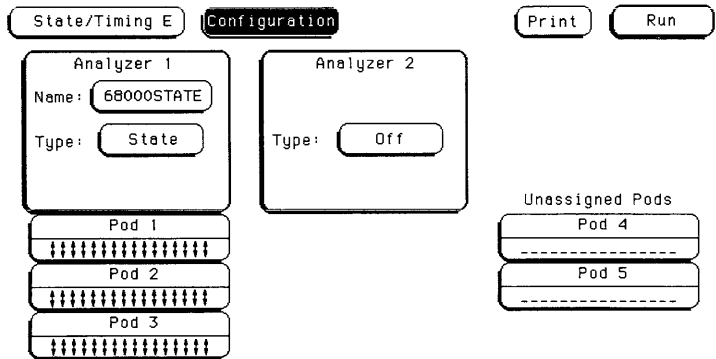
Connecting the Probes

At this point, if you had a target system with a 68000 microprocessor, you would connect the logic analyzer to your system. Since you will be assigning labels ADDR and DATA, you hook the probes to your system accordingly:

- Pod 1 probes 0 through 15 to the data bus lines D0 through D15.
- Pod 2 probes 0 through 15 to the address bus lines A0 through A15.
- Pod 3 probes 0 through 7 to the address bus lines A16 through A23.
- Pod 1, CLK (J clock) to the address strobe (LAS).

Activity Indicators

When the logic analyzer is connected and your target system is running, you will see (\uparrow) in the Pod 1, 2, and 3 fields of the analyzer Configuration menu. This indicates which signal lines are transitioning.



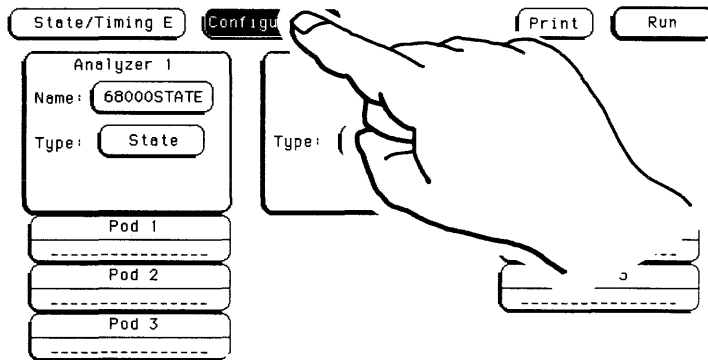
Configuring the State Analyzer

Now that you have configured the system, you are ready to configure the state analyzer. You will be:

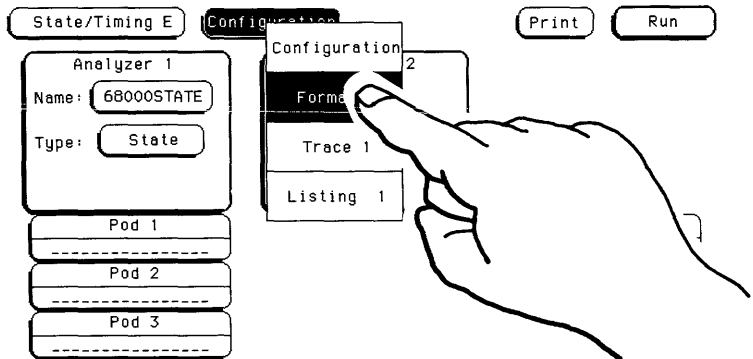
- Creating two names (labels) for the input signals
- Assigning the channels connected to the input signals
- Specifying the State (J) clock
- Specifying a trigger condition

1. Display the state Format specification menu.

a. Touch the field second from the left at the top of the screen.

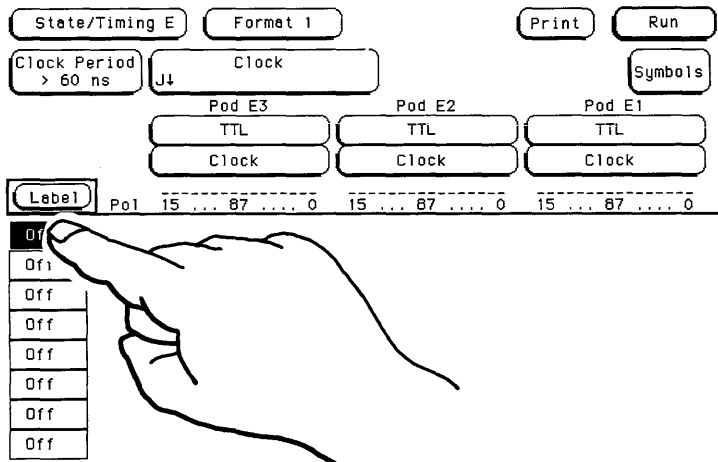


b. Touch the field labeled "Format 1".

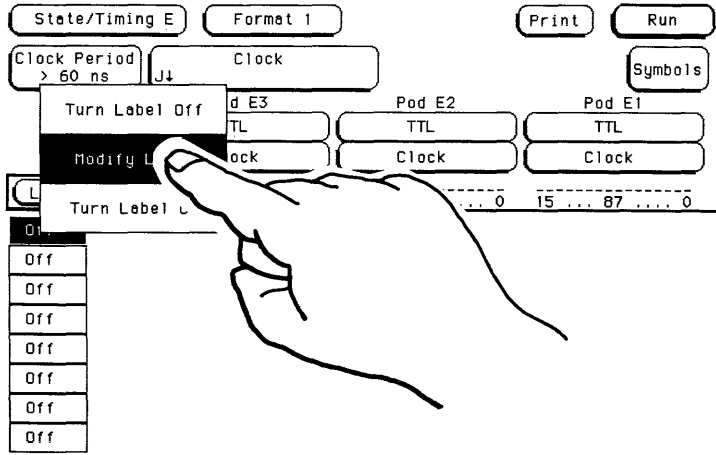


2. Name two labels, one ADDR and one DATA.

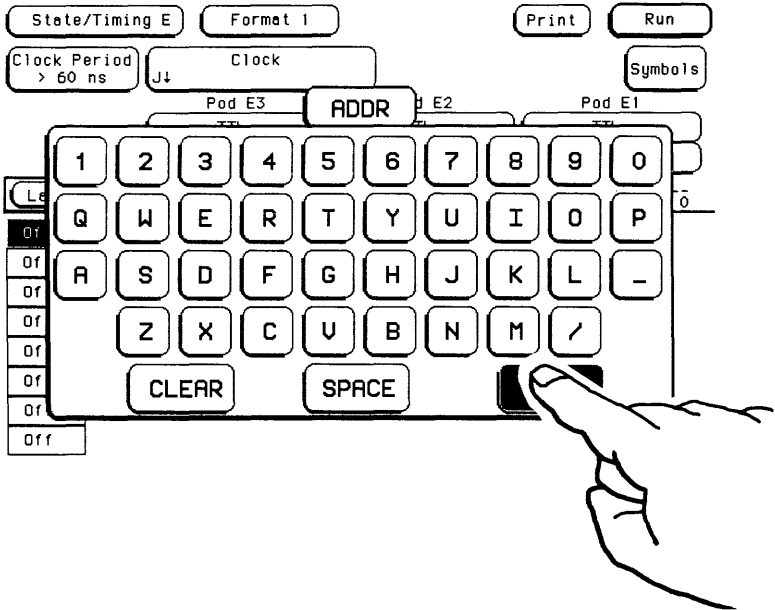
a. Touch the top field in the label column.



b. When the pop-up appears, touch the field labeled "Modify Label".



c. With the alphanumeric keypad pop-up, change the name of the label to ADDR (see "Alpha Entry Pop-up Menu" in Chapter 4 if you need a reminder).



d. Name the second label DATA by repeating steps a through c.

State/Timing E Format 1 Print Run

Clock Period > 60 ns J↓ Clock Symbols

Pod E3 Pod E2 Pod E1

TTL TTL TTL

Clock Clock Clock

Label

	Pod 1	15 ... 87 ... 0	15 ... 87 ... 0	15 ... 87 ... 0
ADDR	+
DATA	+
Off				
Off				
Off				
Off				
Off				
Off				

3. Assign Pod 1 bits 0 through 15 to the label DATA.

a. Touch the bit assignment field under Pod 1 and to the right of DATA.

State/Timing E Format 1 Print Run

Clock Period > 60 ns J↓ Clock Symbols

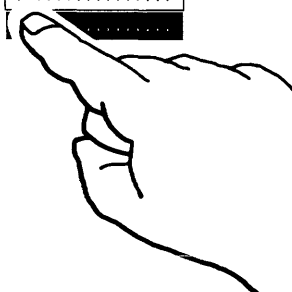
Pod E3 Pod E2 Pod E1

TTL TTL TTL

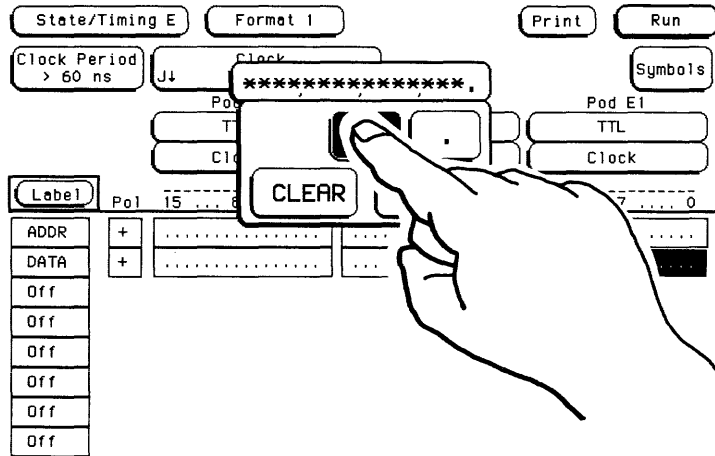
Clock Clock Clock

Label

	Pod 1	15 ... 87 ... 0	15 ... 87 ... 0	15 ... 87 ... 0
ADDR	+
DATA	+
Off				
Off				
Off				
Off				
Off				
Off				



- b. Any combination of bits may already be assigned to this pod; however, you will want all 16 bits assigned to the DATA label. Start at the left end and touch the asterisk field 16 times to assign all the bits. Touch Done to close the pop-up.



4. Assign Pod 2 bits 0 through 15 to the label ADDR by repeating step 3.

5. Assign Pod 3 bits 0 through 7 to the label ADDR.

If any other bit assignment field has bits assigned in it, clear that field so that the bits are all unassigned.

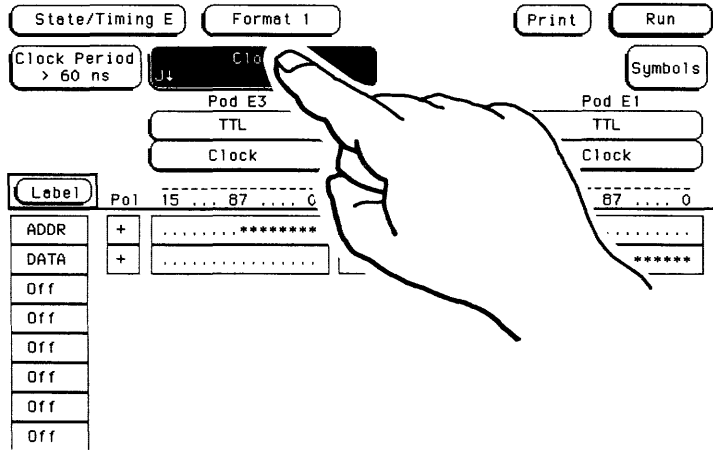
The state Format specification menu should now look like that below.

State/Timing E		Format 1		Print		Run	
Clock Period > 60 ns		Clock		J↓		Symbols	
		Pod E3		Pod E2		Pod E1	
		TTL		TTL		TTL	
		Clock		Clock		Clock	
Label	Po1	15 ... 87 ... 0	15 ... 87 ... 0	15 ... 87 ... 0	15 ... 87 ... 0	15 ... 87 ... 0	15 ... 87 ... 0
ADDR	+*****	*****
DATA	+
Off							
Off							
Off							
Off							
Off							
Off							
Off							

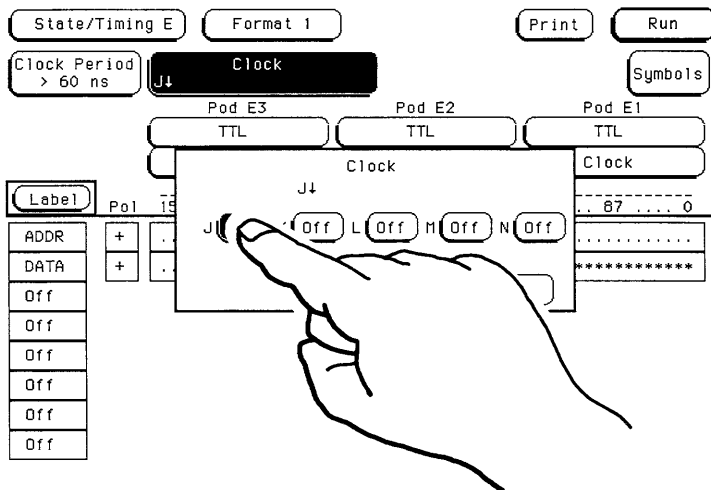
Specifying the J Clock

If you remember from "What's a State Analyzer" in *Feeling Comfortable With Logic Analyzers*, the state analyzer samples the data under the control of an external clock which is "synchronous" with your circuit under test. Therefore, you must specify which clock probe you will use for your measurement. In this exercise you will use the J clock, which is accessible through pod 1.

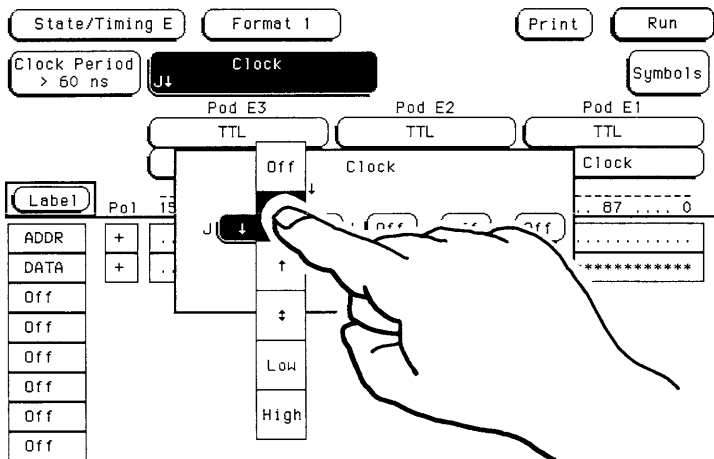
1. Display the state Format specification menu.
2. Set the J Clock to sample on a negative-going edge.
 - a. Touch the field labeled "Clock".



b. In the pop-up, touch the field to the right of J.

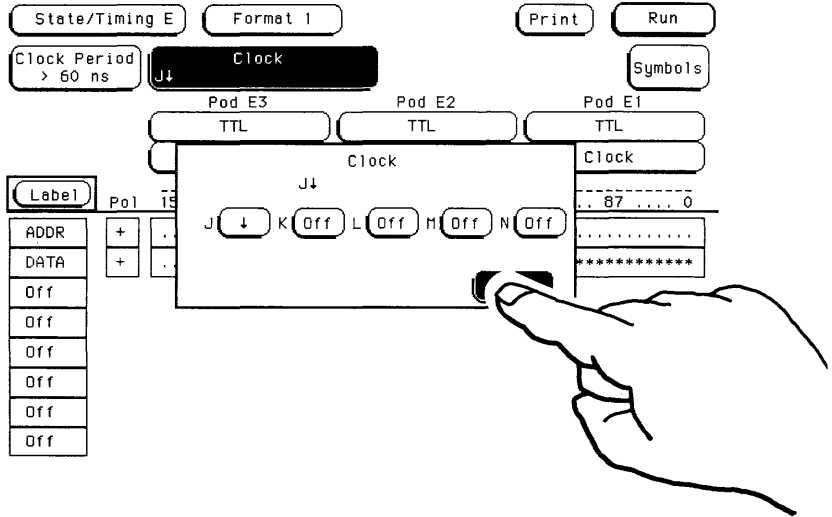


c. Touch the field with the arrow pointing down.

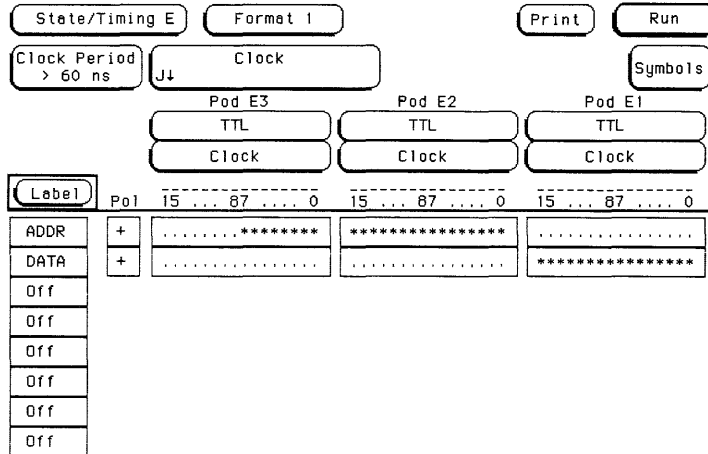


3. Turn off all other clocks (K-N) if any are on by repeating steps a through c above.

d. Touch the Done field to close the pop-up.



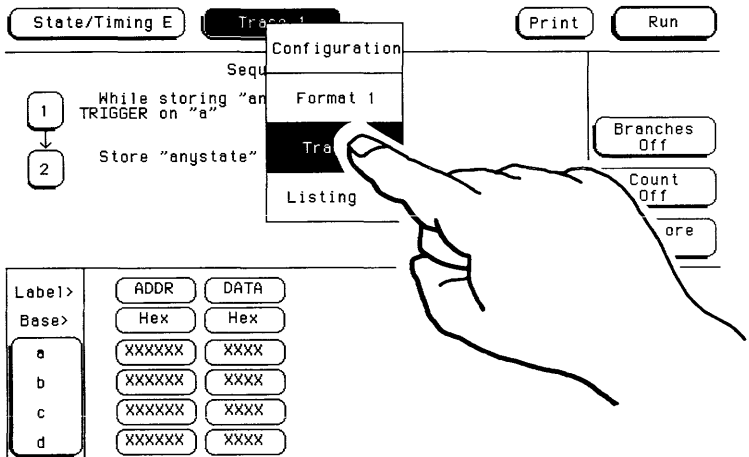
The state Format specification menu should look like that shown below.



Specifying a Trigger Condition

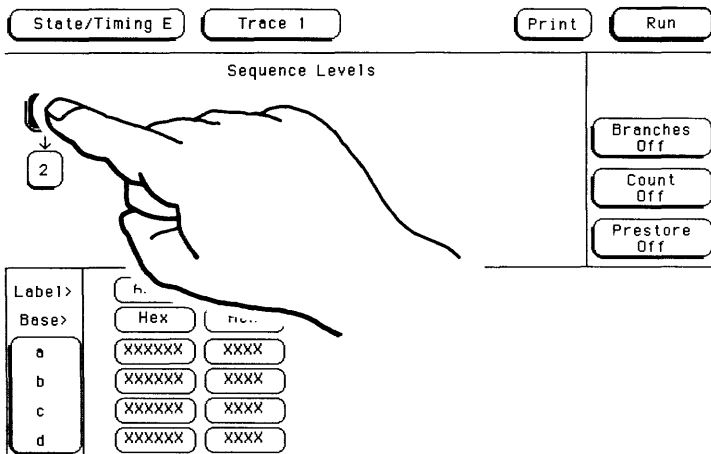
To capture the data and place the data of interest in the center of the display of the state Listing menu, you need to tell the state analyzer when to trigger. Since the first event of interest is address 0000, you need to tell the state analyzer to trigger when it detects address 0000 on the address bus.

1. Display the state Trace specification menu.
 - a. Touch the field second from the left at the top of the screen.
 - b. Touch the field labeled "Trace 1".

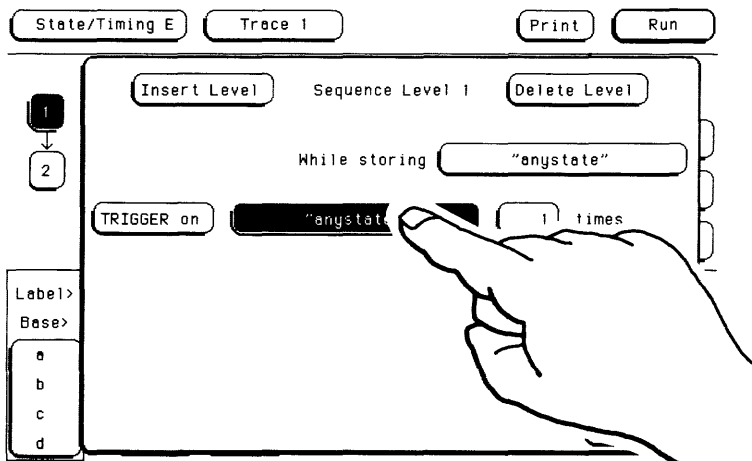


2. Set the trigger so that the state analyzer triggers on address 0000.

a. Touch the 1 in the Sequence Levels field of the menu.

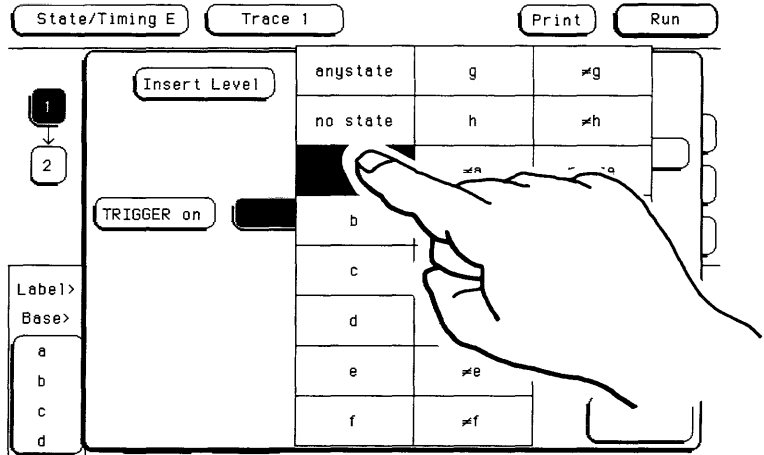


b. In the pop-up touch the field labeled "anystate" to the right of the TRIGGER on field.

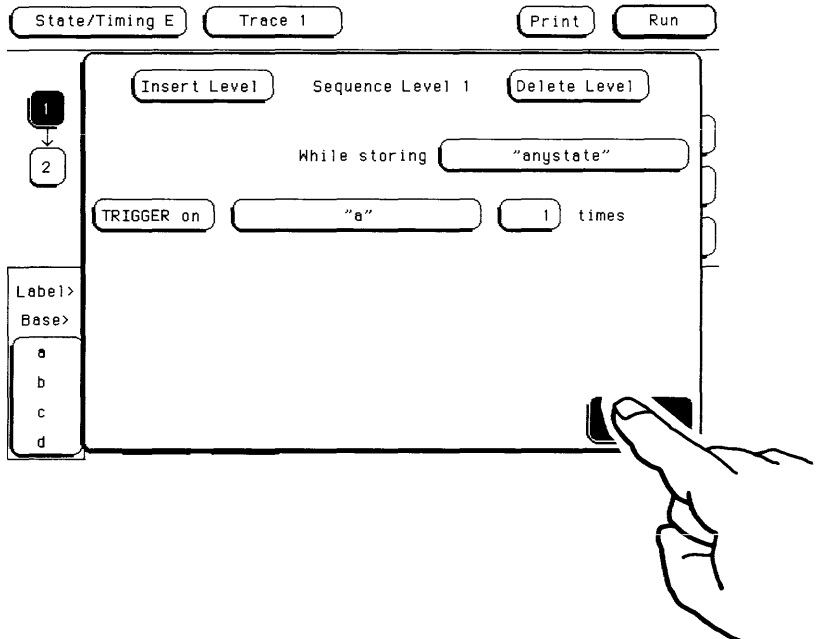


Another pop-up appears showing you a list of "trigger on" options. Options a through h are qualifiers that allow you to assign a pattern for the trigger specification.

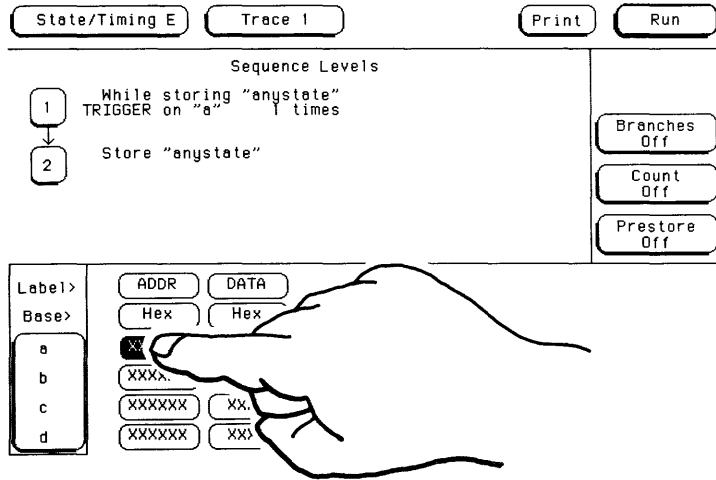
c. Touch the field with the "a" option.



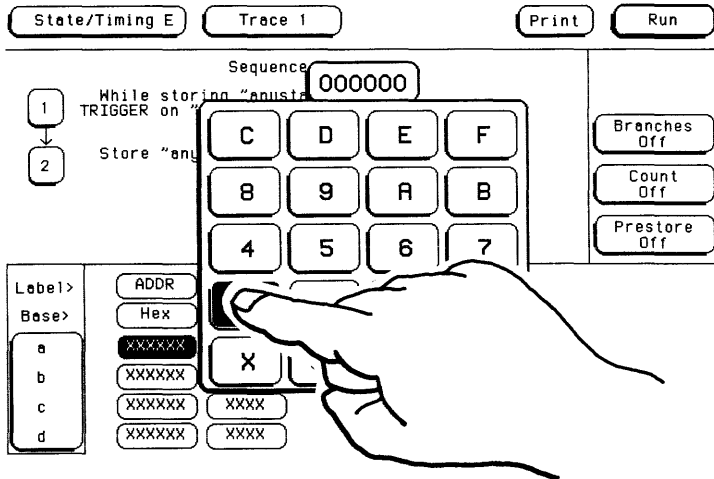
d. Touch the Done field in the Sequence Levels pop-up.



e. Touch the field to the right of "a" under the label ADDR.



f. With the pop-up keypad, touch the 0 (zero) key until all zeros appear in the display space above the keypad. Touch the Done field to close the pop-up.



Your trigger specification now states: "While storing anystate trigger on "a" once and then store anystate."

State/Timing E
Trace 1
Print
Run

Sequence Levels

```

1  While storing "anystate"
   | TRIGGER on "a" | times
   |
   v
2  Store "anystate"
        
```

Branches
Off

Count
Off

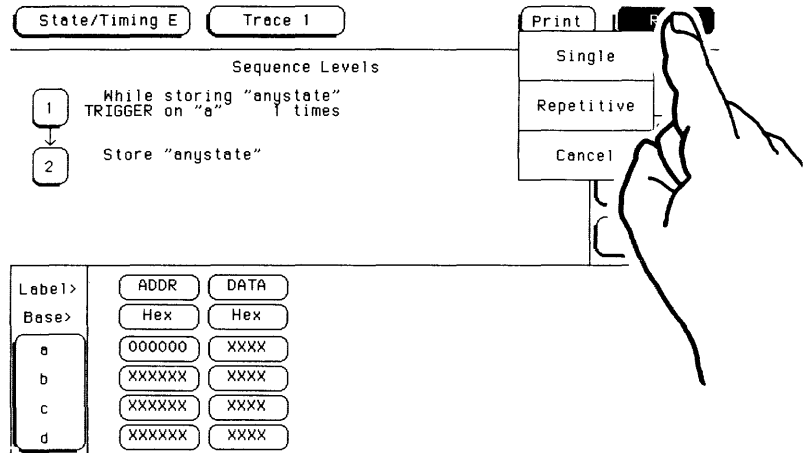
Prestore
Off

Label>	ADDR	DATA
Base>	Hex	Hex
a	000000	XXXX
b	XXXXXX	XXXX
c	XXXXXX	XXXX
d	XXXXXX	XXXX

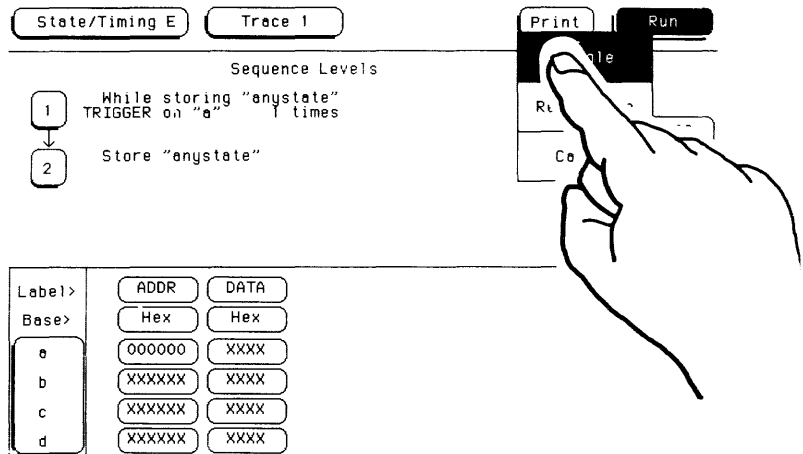
When the state analyzer is connected to your circuit and is acquiring data, it continuously stores until it sees 0000 on the address bus, at which time it begins to store anystate until the analyzer memory is filled.

Acquiring the Data

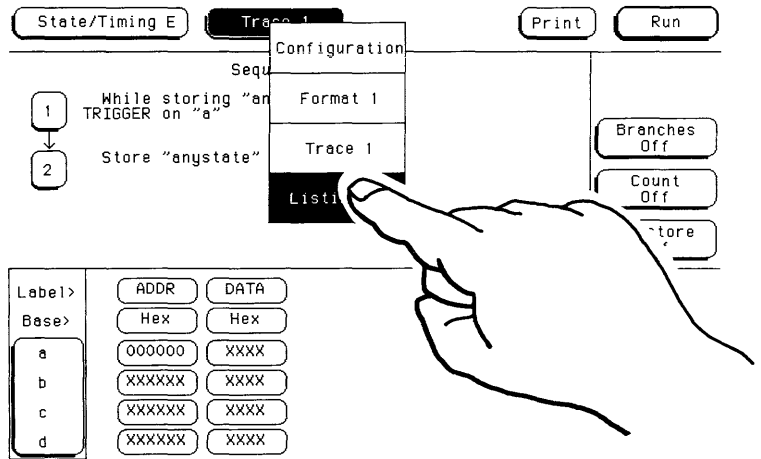
To acquire the data, you touch the green field in the upper right-hand corner of the screen labeled Run. Unlike the timing analyzer you do not have to go to the data display (state Listing) menu for the first run. You can simply touch the Run field while in any state specification menu. After touching the Run field, don't lift your finger off the screen.



When you touch the Run field a pop-up appears next to it with the options Single, Repetitive and Cancel. With your finger still on the screen, move it to the field labeled "Single". Single will turn white indicating that it has been selected.

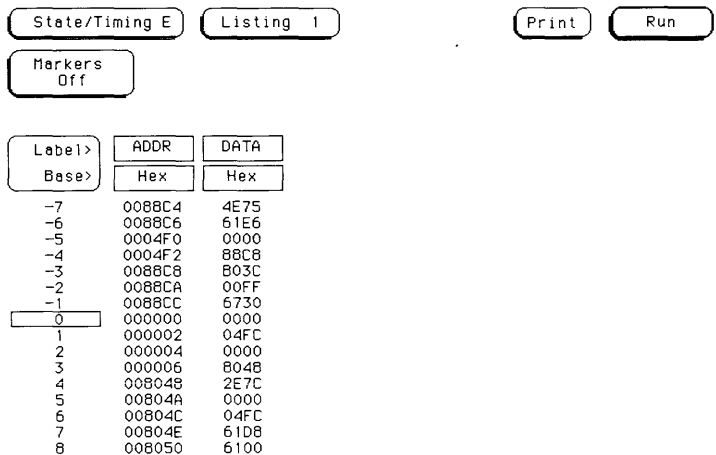


If you want to go to the state listing menu before taking a measurement, touch the field second from the left at the top of the screen. When the pop-up appears, touch the field labeled "Listing 1".



Since you want to capture the data when the microprocessor sends address 0000 on the bus after power-up, you touch the Run field to arm the state analyzer and then force a reset of your circuit. When the reset cycle ends, the microprocessor should send address 0000 trigger the state analyzer and switch the display to the state Listing menu.

We'll assume this is what happens in this example, since the odds of the microprocessor not sending address 0000 are very low.



The State Listing

The state listing displays three columns of numbers as shown:

State/Timing E	Listing 1	Print	Run
Markers Off			
Label>	ADDR	DATA	
Base>	Hex	Hex	
-7	0088C4	4E75	
-6	0088C6	61E6	
-5	0004F0	0000	
-4	0004F2	88C8	
-3	0088C8	803C	
-2	0088CA	00FF	
-1	0088CC	6730	
0	000000	0000	
1	000002	04FC	
2	000004	0000	
3	000006	8048	
4	008048	2E7C	
5	00804A	0000	
6	00804C	04FC	
7	00804E	61D8	
8	008050	6100	

The first column of numbers are the state line number locations as they relate to the trigger point. The trigger state is on the line 0 in the vertical center of the list area. The negative numbers indicate states occurring before the trigger and the positive numbers indicate the states occurring after the trigger.

The second column of numbers are the states (listed in HEX) the state analyzer sees on the address bus. This column is labeled ADDR.

The third column of numbers are the states (listed in HEX) the state analyzer sees on the data bus. This column is labeled DATA.

Finding the Answer

Your answer is now found in this listing of the states 0 through 4.

The 68000 always reads address locations 0, 2, 4, and 6 to find the stack pointer location and memory location for the instruction it fetches after power-up. The 68000 uses two words for each of the locations that it is looking for, a high word and a low word. When the software designer programs the ROM he must put the stack pointer location at address locations 0 and 2. 0 is the high word location and 2 is the low word location. Similarly, the high word of the instruction fetch location must be in address location 4 and the low word in location 6.

Since the software design calls for the reset vector to:

1. set the stack pointer to be set to 04FC
2. read memory address location 8048 for its first instruction fetch

you are interested in what is on both the address bus and the data bus in states 0 through 3.

You look at the following listing and see that states 0 and 1 do contain address locations 0 and 2 under the ADDR label, indicating that the microprocessor did look to the correct locations for the stack pointer data. You also see that the data contained in these ROM locations are 0000 and 04FC, which are correct.

You then look at states 2 and 3. You see that the next two address locations are 4 and 6, which is correct, and the data found at these locations is 0000 and 8048, which is also correct.

So far you have verified that the microprocessor has performed the correct reset vector search. The next thing you must verify is whether the microprocessor addresses the correct location in ROM that it was instructed to address in state 4 and whether the data is correct in this ROM location. From the listing you see that the address in state 4 is 008048, which is correct, but the instruction found in this location is 2E7C, which is not correct. You have found your problem: incorrect data stored in ROM for the microprocessor's first instruction.

- 0 000000 0000 (high word of stack pointer location)
- 1 000002 04FC (low word of stack pointer location)
- 2 000004 0000 (high word of instruction fetch location)
- 3 000006 8048 (low word of instruction fetch location)
- 4 008048 2E7C (first microprocessor instruction)

Label>	ADDR	DATA
Base>	Hex	Hex
-7	0088C4	4E75
-6	0088C6	61E6
-5	0004F0	0000
-4	0004F2	88C8
-3	0088C8	B03C
-2	0088CA	00FF
-1	0088CC	6730
0	000000	0000
1	000002	04FC
2	000004	0000
3	000006	8048
4	008048	2E7C
5	00804A	0000
6	00804C	04FC
7	00804E	61D8
8	008050	6100

Summary

You have just learned how to make a simple state measurement with the HP 16510B Logic Analyzer module in the HP 16500A. You have:

- specified a state analyzer
- learned which probes to connect
- assigned pods 1, 2, and 3
- assigned labels
- assigned bits
- specified the J clock
- specified a trigger condition
- acquired the data
- interpreted the state listing

You have seen how easy it is to use the state analyzer to capture the data on the address and data buses. You can use this same technique to capture and display related data on the microprocessor status control, and various strobe lines. You are not limited to using this technique on microprocessors. You can use this technique anytime you need to capture data on multiple lines and need to sample the data relative to a system clock.

The next chapter teaches you how to use the logic analyzer as an interactive timing and state analyzer. You will see a simple measurement that shows you both timing waveforms and state listings and how they are correlated.

Using the Timing/State Analyzer

Introduction

In this chapter you will learn how to use the timing and state analyzers interactively by setting up the logic analyzer to make a simple measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized differently than the two previous chapters. Since you have already set up both the timing and state analyzers, you should be ready to set them up for this measurement by looking at the menu pictures.

Any new set-ups in this exercise will be explained in task format steps as in the previous chapters.

How you use the steps depends on how much you remember from chapters 3 and 4. If you can set up each menu by just looking at the menu picture, go right ahead and do so. If you need a reminder of what steps to perform, follow the numbered steps. If you need still more information about "how", use the lettered steps.

Problem Solving with the Timing/State Analyzer

In this example assume you have designed a microprocessor-controlled circuit. You have completed the hardware, and the software designer has completed the software and programmed the ROM (read-only memory). When you turn your circuit on for the first time, it doesn't function as required. You have checked the power supply voltages and the system clock and they are working properly.

Since the circuit has never worked before, you and the software engineer aren't sure if it is a hardware or a software problem. Some testing will be required in order to find a solution.

You also notice the circuit fails intermittently. More specifically, it only fails when the microprocessor attempts to address a routine that starts at address 8930.

What Am I Going to Measure?

To see what might be causing the failure, you decide to start where the microprocessor goes to the routine that starts at address 8930.

The first thing you check is whether the microprocessor actually addresses address 8930. The next thing you check is whether the code is correct in all the steps in this routine.

Your measurement, then, requires verification of:

- whether the microprocessor addresses location 8930
- whether all the addresses within the routine are correct
- whether all the data at the addresses in the routine are correct

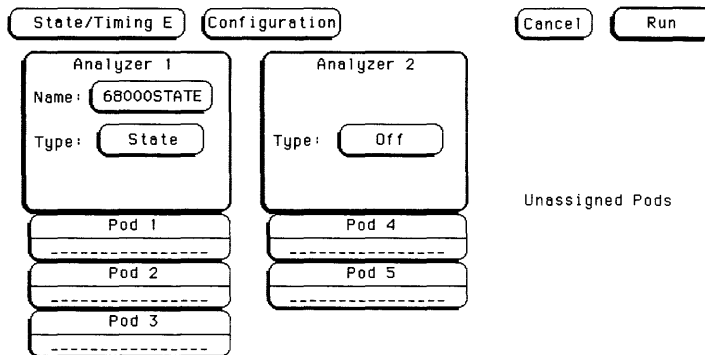
If the routine is correct, the state listing will display:

```
0 008930 B03C
1 008932 61FA
2 008934 67F8
3 008936 B03C
4 00892E 61FA
```

How Do I Configure the Logic Analyzer?

In order to make this measurement, you must configure the logic analyzer as a state analyzer because you want to trigger on a specific state (8930). You also want to verify that the addresses and data are correct in the states of this routine.

Configure the logic analyzer so that analyzer 1 is a state analyzer as shown:



Configuring the State Analyzer

Now that you have configured the system, you are ready to configure the state analyzer.

Configure the state Format specification as shown:

State/Timing E Format 1 Cancel Run

J↓ Clock Symbols

Pod E3 Pod E2 Pod E1

TTL TTL TTL

Clock Clock Clock

Label	Pod	15	8	7	0
ADDR	+	*****		
DATA	+	*****		
Off					
Off					
Off					
Off					
Off					
Off					

Configure the state Trace specification as shown:

State/Timing E Trace 1 Cancel Run

Sequence Levels

1 While storing "anystate"
TRIGGER on "a" 1 times

↓

2 Store "anystate"

Branches Off

Count Time

Prestore Off

Label>	ADDR	DATA
Base>	Hex	Hex
a	00B930	XXXX
b	XXXXXX	XXXX
c	XXXXXX	XXXX
d	XXXXXX	XXXX

Connecting The Probes

At this point, if you had a target system with a 68000 microprocessor, you would connect the logic analyzer to your system. Since you have assigned labels ADDR and DATA, you would hook the probes to your system accordingly:

- Pod 1 probes 0 through 15 to the data bus lines D0 through D15
- Pod 2 probes 0 through 15 to the address bus lines A0 through A15
- Pod 3 probes 0 through 7 to the address bus lines A16 through A23
- Pod 1, CLK (J clock) to the address strobe (LAS)

Acquiring the Data

Since you want to capture the data when the microprocessor sends address 8930 on the bus, you touch the Run field to arm the state analyzer. Remember, after you touch Run, a pop-up will appear. Touch the field labeled "Single" in the pop-up to get a single run. If the microprocessor sends address 8930, it will trigger the state analyzer and switch the display to the state Listing.

We'll assume this is what happens in this example.

Finding the Problem

You look at this listing to see what the data is in states 0 through 4. You know your routine is five states long.

The 68000 does address location 8930, so you know that the routine is addressed. Now you need to compare the state listing with the following correct addresses and data:

```
0 008930 B03C
1 008932 61FA
2 008934 67F8
3 008936 B03C
4 00892E 61FA
```

As you compare the state Listing (shown below), you notice the data at address 8932 is incorrect. Now you need to find out why.

State/Timing E Listing 1 Cancel Run

Markers Time Trig to X 0 s Trig to 0 0 s X to 0 0 s

Label>	ADDR	DATA
Base>	Hex	Hex
-6	0088CC	6730
-5	0088CE	48E7
-4	0088FE	4E75
-3	004480	1800
-2	0004F4	0000
-1	0004F6	8930
0	008930	B03C
1	008932	00FF
2	008934	67F8
3	0004F6	8930
4	00892E	61FA
5	008930	B03C
6	0004F4	0000
7	00027B	4498
8	008936	B03C
9	804496	7FCD

← INCORRECT DATA

Your first assumption is that incorrect data is stored into this memory location. Assume this routine is in ROM since it is part of the operating system for your circuit. Since the ROM is programmed by the software designer, you have the software designer verify if the data at address 8932 is correct. The software designer tells you that the data is correct. Now what do you do?

Now it's time to look at the hardware to see if it is causing incorrect data when the microprocessor reads this memory address. You decide you want to see what is happening on the address and data buses during this routine in the time domain.

In order to see the time domain, you need the timing analyzer.

What Additional Measurements Must I Make?

Since the problem arises during the routine that starts at address 8930, you decide you want to see the timing waveforms on the address and data bus when the routine is running. You also want to see the control signals that control the read cycle. You will then compare the waveforms with the timing diagrams in the 68000 data book.

Your measurement, then, requires verification of:

- correct timing of the control signals
- stable addresses and data during the memory read

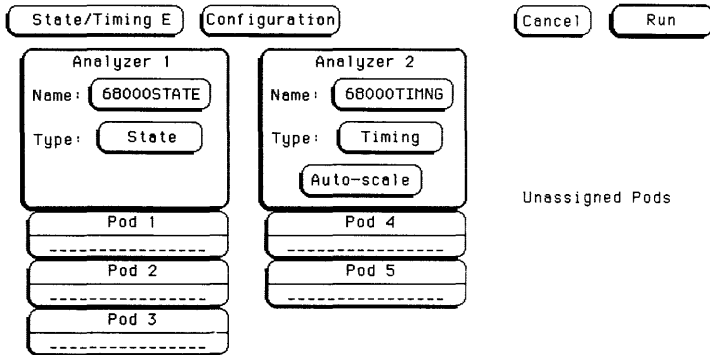
The control signals you must check are:

- system clock
- address strobe (AS)
- lower and upper data strobes (LDS and UDS)
- data transfer acknowledge (DTACK)
- read/write (R/W)

How Do I Re-configure the Logic Analyzer?

In order to make this measurement, you must re-configure the logic analyzer so that analyzer 2 is a timing analyzer. You leave analyzer 1 as a state analyzer since you will use the state analyzer to trigger on address 8930.

Configure the logic analyzer so analyzer 2 is a timing analyzer as shown:

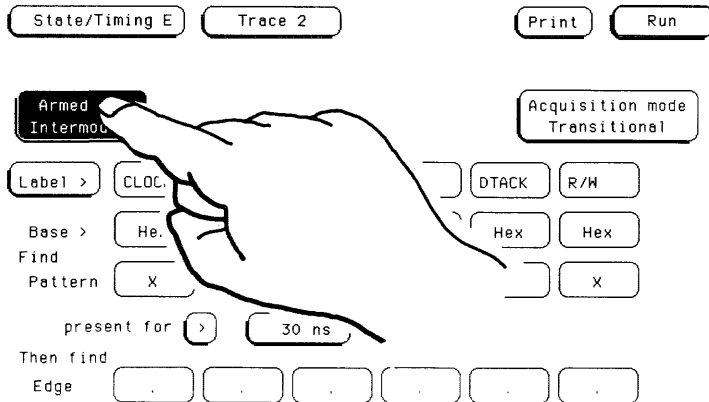


Setting the Timing Analyzer Trigger

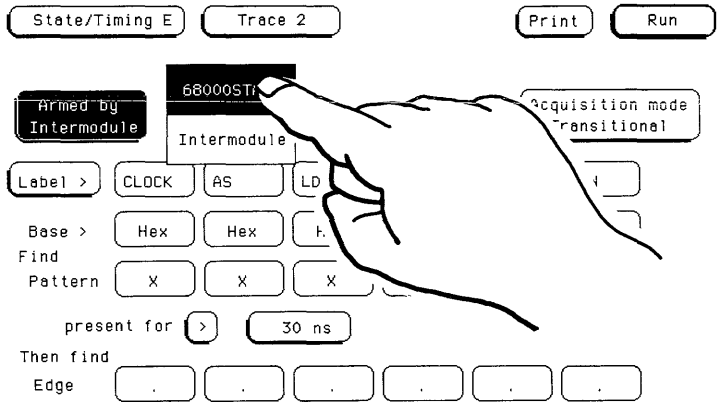
Your timing measurement requires the timing analyzer to display the timing waveforms present on the buses when the routine is running. Since you triggered the state analyzer on address 8930, you want to trigger the timing analyzer so the timing waveforms can be time-correlated with the state listing.

To set up the logic analyzer so that the state analyzer triggers the timing analyzer, perform these steps:

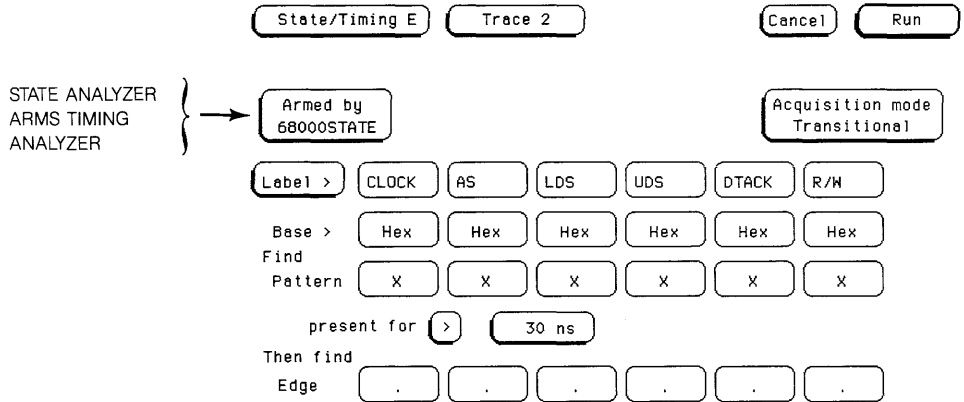
1. Display the timing Trace specification menu (Trace 2).
2. Touch the field labeled "Armed by Intermodule."



3. In the pop-up, touch the field labeled "68000STATE."



Your timing Trace specification should match the menu shown:

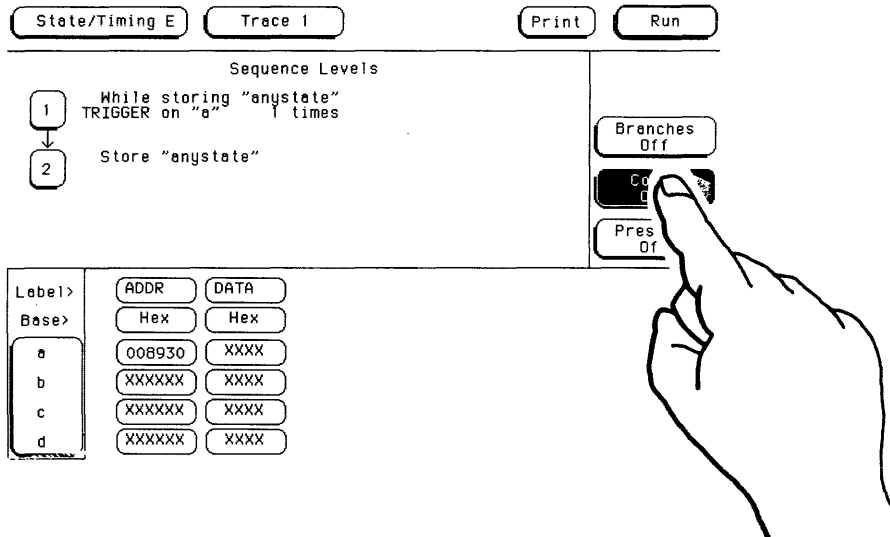


Time-Correlating the Data

In order to time-correlate the data, the logic analyzer must store the timing relationships between states. Since the timing analyzer samples asynchronously and the state analyzer samples synchronously, the logic analyzer must use the stored timing relationship of the data to reconstruct a time-correlated display.

To set up the logic analyzer to keep track of these timing relationships, turn on a counter in the state Trace specification menu. The following steps show you how:

1. Display the state Trace specification menu (Trace 1).
2. Touch the field labeled "Count Off."



3. In the pop-up, touch the field labeled "Time."

State/Timing E Trace 1 Print Run

Sequence Levels

1 While storing "anystate"
TRIGGER on "a" 1 times

2 Store "anystate"

Off Branches Off
Count Off

Stat...

Label> ADDR DATA
Base> Hex Hex
a 008930 XXXX
b XXXXXX XXXX
c XXXXXX XXXX
d XXXXXX XXXX

The counter will now be able to keep track of time for the time correlation.

State/Timing E Trace 1 Cancel Run

Sequence Levels

1 While storing "anystate"
TRIGGER on "a" 1 times

2 Store "anystate"

Branches Off
Count Time
Prestore Off

Label> ADDR DATA
Base> Hex Hex
a 008930 XXXX
b XXXXXX XXXX
c XXXXXX XXXX
d XXXXXX XXXX

Connecting the Timing Analyzer Probes

At this point you would connect the probes of pods 4 and 5 as follows:

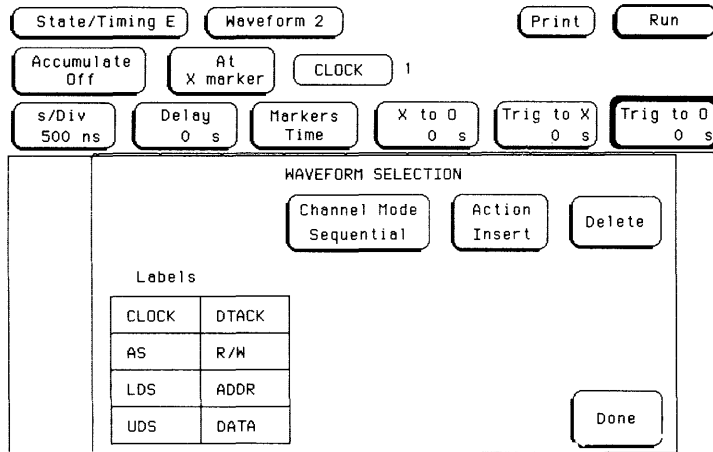
- Pod 4 bit 0 to address strobe (AS)
- Pod 4 bit 1 to the system clock
- Pod 4 bit 2 to low data strobe (LDS)
- Pod 4 bit 3 to upper data strobe (UDS)
- Pod 4 bit 4 to the read/write (R/W)
- Pod 4 bit 5 to data transfer acknowledge (DTACK)
- Pod 5 bits 0 through 7 to address lines A0 through A7
- Pod 5 bits 8 through 15 to data lines D0 through D7

The Timing Waveform Menu

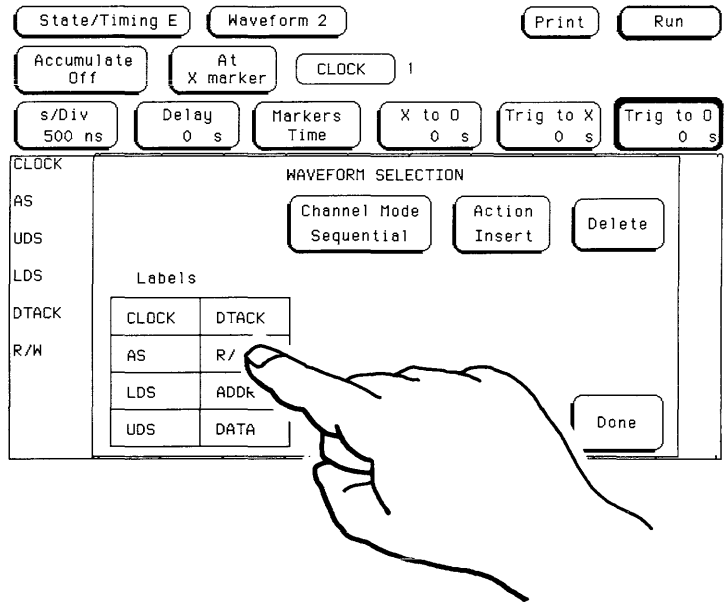
After the probes of pods 4 and 5 are connected, you can re-acquire the data. However, first you need to assign the labels in the timing Waveform menu. A few items in the timing Waveform menu were not discussed in Chapter 5, but they now need to be discussed.

Displaying the Waveforms

Display the timing Waveform menu. Touch the long blue field on the left side of the screen. The pop-up that appears should look like that below.

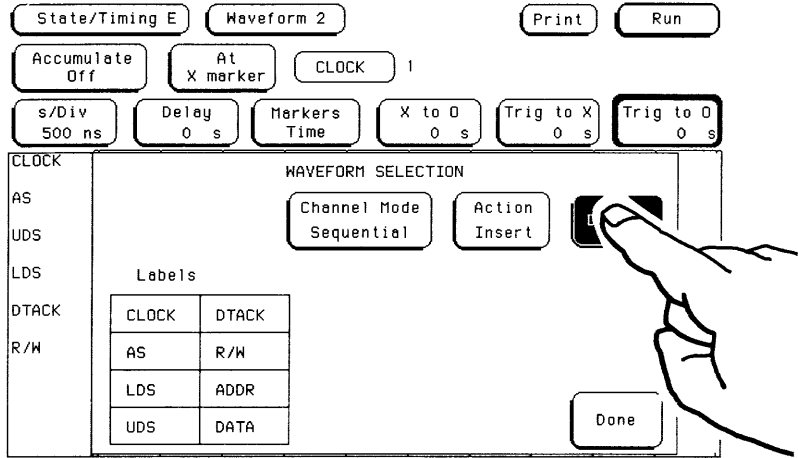


Touch the labels **CLOCK**, **AS**, **UDS**, **LDS**, **DTACK**, AND **R/W** in that order. They will appear in the blue label area.

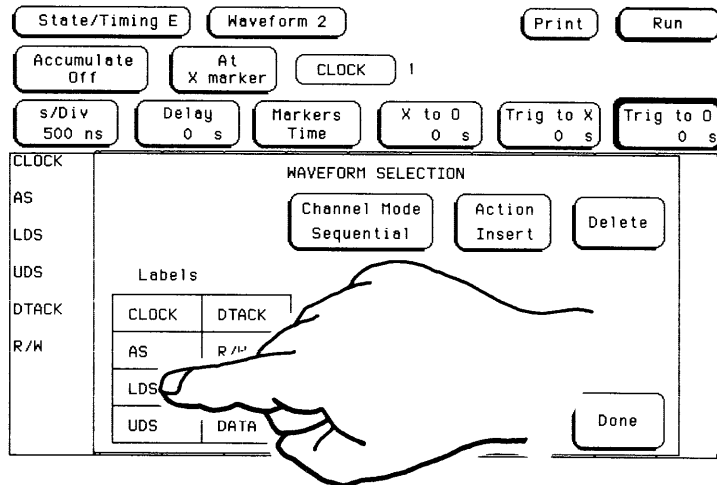


This is not the order we want them in. We want LDS before UDS. To correct this, follow these steps:

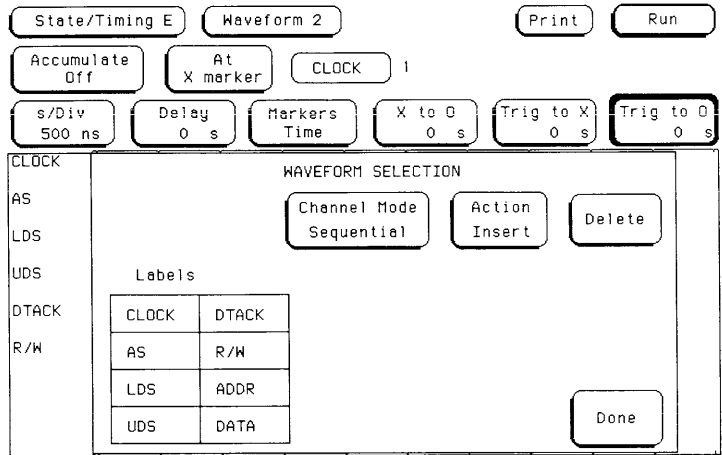
1. Use the KNOB to place the cursor on the label LDS in the long blue label field.
2. Touch the field labeled "Delete." This erases LDS.



3. Use the KNOB to place the cursor over the label AS. Touch the LDS field under Labels in the pop-up.

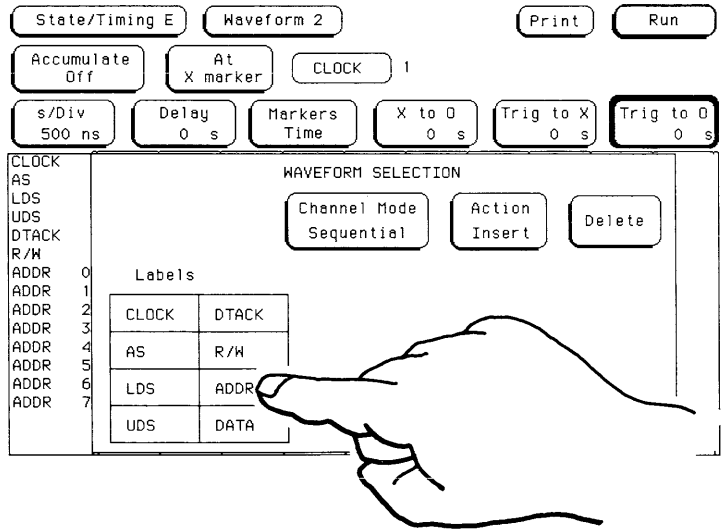


LDS appears in the blue label area in its correct position.

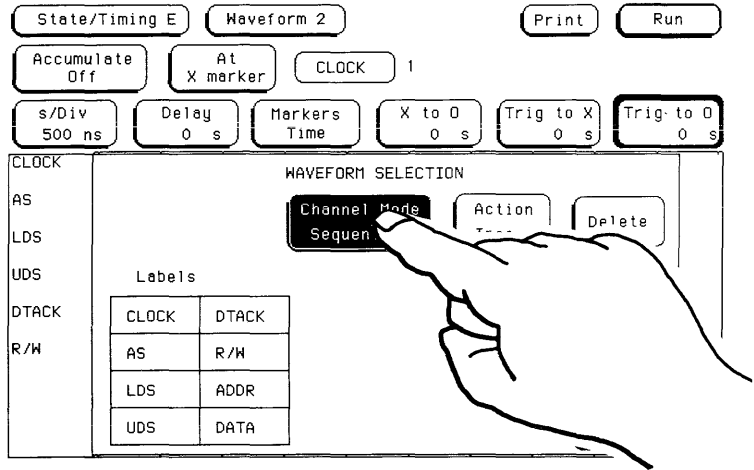


Now we want to put ADDR and DATA in the long blue label area.

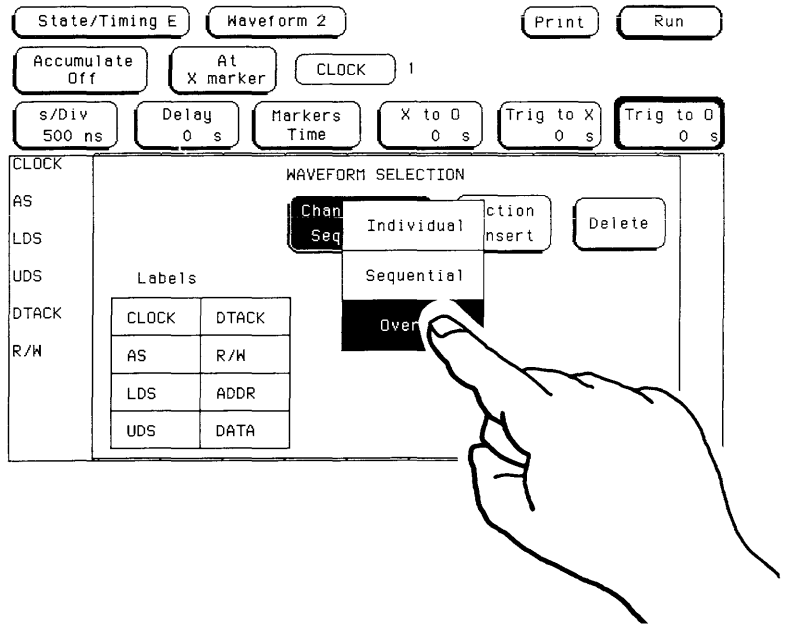
Position the cursor on R/W in the long blue label field. Touch ADDR under Labels in the pop-up. Since ADDR has eight bits assigned to it, eight labels appear in the label field, as shown:



2. Touch the field labeled "Channel Mode Sequential."

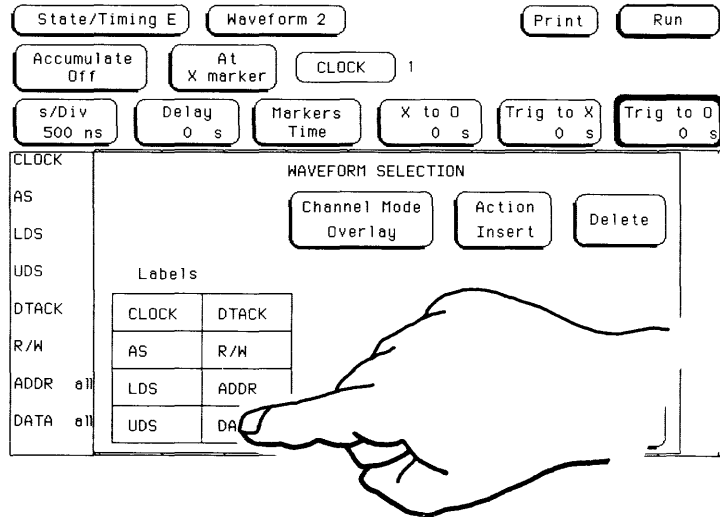


3. In the new pop-up, touch the field labeled "Overlay."



4. Touch the ADDR label field under Labels.

5. Touch the DATA label field under Labels. The screen should look like that shown below.



In the long blue label field ADDR and DATA have "all" next to them to show that the bits are overlapped. Touch the Done field to close the pop-up.

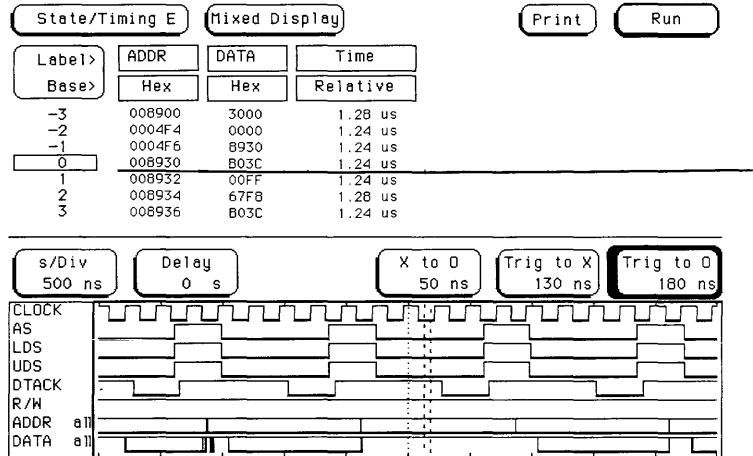
Re-acquiring the Data

Now you are ready to acquire the data. Touch Run. The logic analyzer will display the timing waveforms, unless you switched to one of the state analyzer menus, in which case the state listing will be displayed. Regardless of which menu is displayed, change the display to the Mixed Mode Display.

Mixed Mode Display

The Mixed Display shows you both the state Listing and timing Waveform menus simultaneously. To change to Mixed Display:

1. Touch the field second from the left at the top of the screen.
2. In the pop-up, touch the field labeled "Mixed Display." You will see the Mixed Display as shown:

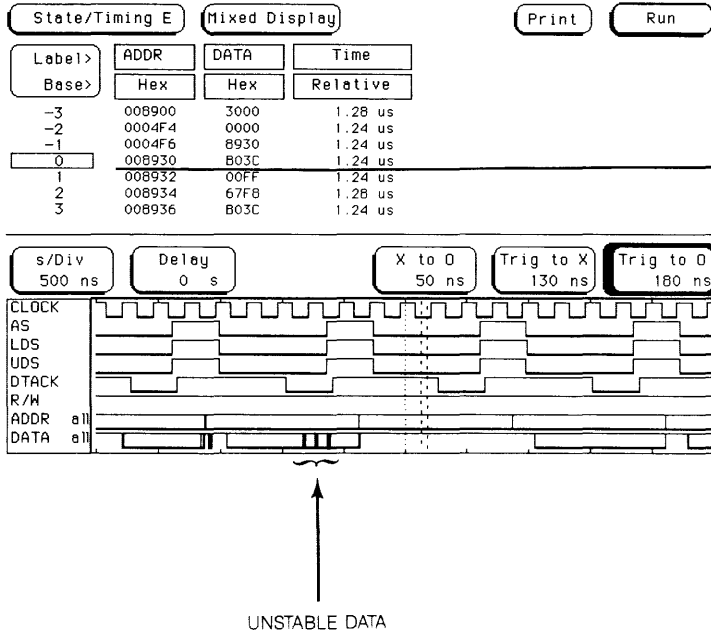


Finding the Answer

In the Mixed Mode Display the state Listing is in the top half of the screen and the timing waveforms are in the lower half. The important thing to remember is that you time-correlated this display so you could see what is happening in the time domain during the faulty routine.

Notice that the trigger points in both parts of the display are the same as they are when the displays are separate. The trigger in the state listing is in the box containing 0 and the trigger point of the timing waveform is the vertical red line.

As you look at the mixed display, you notice nothing wrong except the data at address 8932 is incorrect. However, as you look at the overlapping waveforms, you notice that there are transitions on the data lines during the read cycle, indicating that the data is unstable. You have found the probable cause of the problem in this routine. Additional troubleshooting of the hardware will lead you to the actual cause.



Summary

You have just learned how to use the timing and state analyzers interactively to find a problem that first appeared to be a software problem, but actually is a hardware problem.

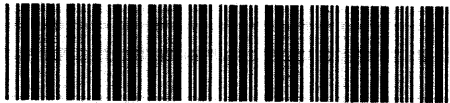
You have learned to:

- trigger one analyzer with the other
- time correlate measurement data
- overlap timing waveforms
- interpret the Mixed Mode Display

What Next?

Now that you are familiar with the logic analyzer module, you may want to try some of the basic measurements discussed in this book on your target system. Refer to the documentation for your microprocessor.

If you are comfortable with the basic measurements that you can perform with the HP 16510B Logic Analyzer Module, you are ready for the *HP 16510B Front-Panel Reference*. This reference explains all the capabilities and operations of the logic analyzer module.



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