64000

HP64000 Logic Development System

Model 64653A 8086/8088 Dedicated Interface Card

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

SERVICE MANUAL
MODEL 64653A
8086/8088 DEDICATED INTERFACE CARD

REPAIR NUMBERS

This manual applies directly to
8086/8088 Dedicated Interface Cards
with repair number prefixes 2310A.

Manual Part Number 64653-90904
Microfiche Part Number 64653-90804

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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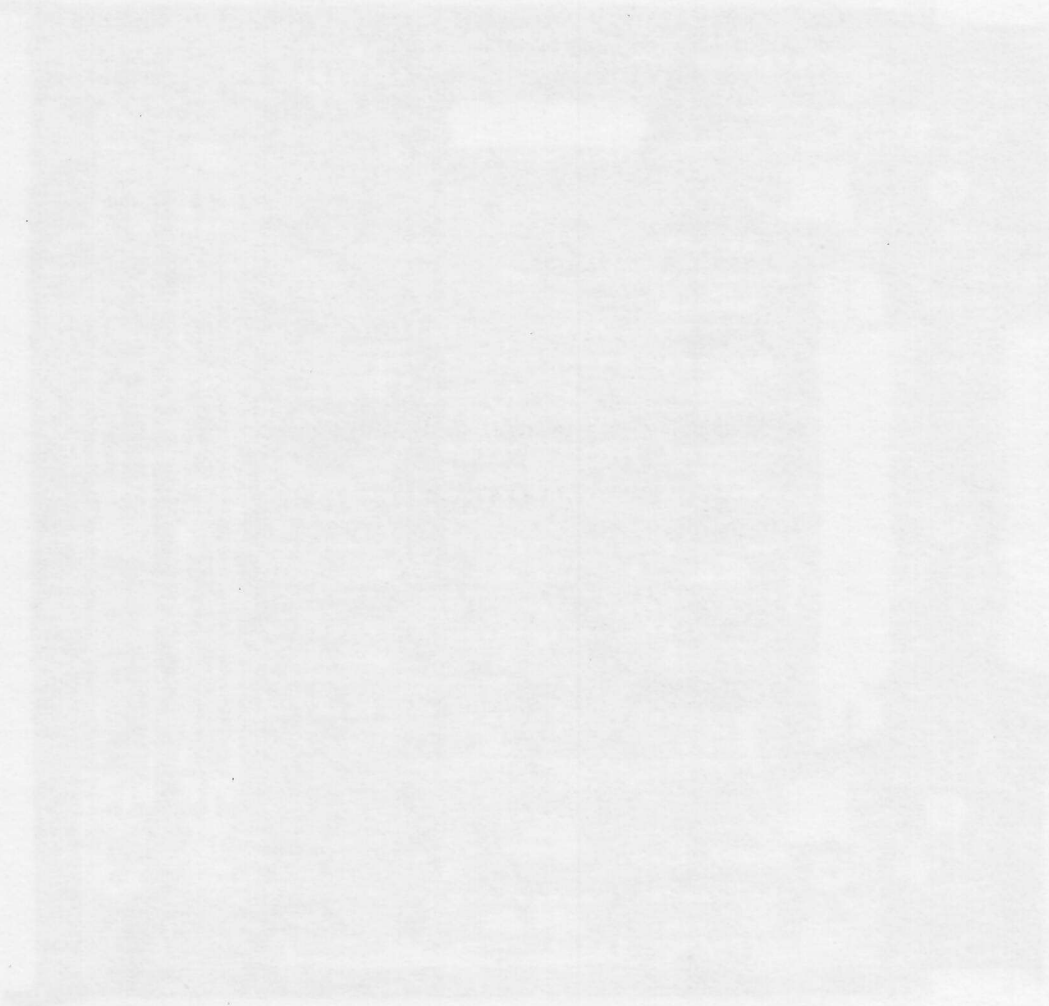


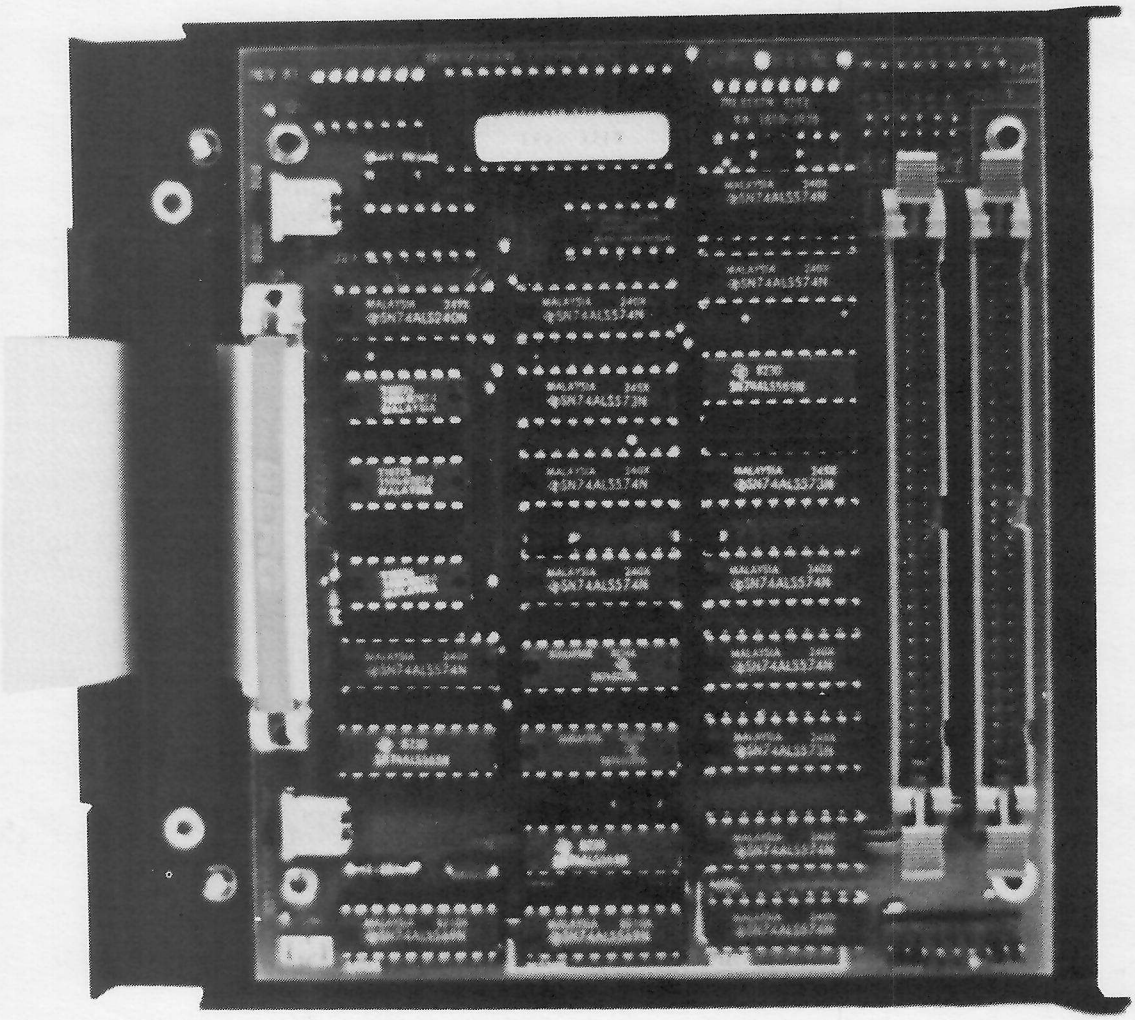


Figure 1-1. Model 64653A 8086/8088 Dedicated Interface Card

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual contains information required to install, test and service the Hewlett-Packard Model 64653A 8086/8088 Dedicated Interface Card.

1-3. Shown on the title page is a microfiche part number. This number can be used to order a 4 X 6-inch microfilm transparency of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. INSTRUMENTS COVERED BY THIS MANUAL.

1-5. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-6. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes Supplement. The supplement contains "change information" that explains how to adapt the manual for the newer instrument.

1-7. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes Supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-8. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes Supplement, call your nearest Hewlett-Packard office.

1-9.DESCRIPTION.

1-10. The 64653A 8086/8088 Dedicated Interface Card connects the 64620S Logic Analyzer or the 1630A/D Logic Analyzer to an 8086 or an 8088 microprocessor system. The Interface Card samples all necessary information about a bus transaction at the proper time, combines this information into a concise form, and then sends all information to the State Analyzer at one time. The CPU can be in either "min" or "max" mode of operation and operate at clock input rates of up to 10 MHz. If the CPU is in "max" mode the Interface Card can, at the user's option, completely dequeue the instruction stream and send only executed instructions to the analyzer.

1-11. ELECTRICAL CHARACTERISTICS.

Maximum clock speed:	10 MHz
Signal line loading:	Three LS TTL loads on the CLK line plus approximately 60 pF capacitance; one LS TTL load for all other monitored signal lines and approx 45 pF capacitance.
Outputs:	STIMULUS and HALT are LS TTL open collector active-low outputs; maximum current sinking, 6 mA.
Input:	ACK, acknowledge for STIMULUS line active low, TTL level.
Power Consumption:	up to 1 A at +5 Vdc maximum, supplied by Model 64620S Logic State/Software Analysis Subsystem or Model 1630A/D Logic Analyzer.

1-12. EQUIPMENT REQUIRED BUT NOT SUPPLIED.

1-13. For a complete 64000 State Analysis subsystem:

64621A State Analysis Control Board
64622A and/or 64623A State Analysis Acquisition Board
64650A General Purpose Preprocessor

For a complete 1630A/D system:

1630A/D
10269 Interface Module

1-14. RELATED MANUALS.

Service Manuals.

State Analysis Control Manual
State Analysis Acquisition Manual (40 Channel or 20 Channel)
State Data Probe Manual
General Purpose Preprocessor Manual
Logic Analyzer 1630A/D

Operating Manuals

State Analyzer Manual
General Purpose Preprocessor Manual
8086/8088 Interface Card Manual
Logic Analyzer 1630A/D

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the Model 64653A. Included are initial inspection procedures and instructions for repacking the instrument for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP's option without waiting for claim settlement.

2-5. INSTALLATION.

2-6. Installation in the 64650A General Purpose Preprocessor.

a. Remove power from the 64000 station.

b. Connect W6 from the small General Purpose Preprocessor card to J4 on the Interface Card.

c. Connect W3 from the Large General Purpose Preprocessor card to J3 on the Interface Card .

d. Lower the Interface Card into the Preprocessor so that the component side fits inside the pod.

e. Fit the Pod Cover hinges into hinge slots on the General Purpose Preprocessor pod. Lower the cover over the Interface Card and fasten down with screws.

CAUTION

To avoid possible damage from static discharge, always connect assembly (W4) from the Preprocessor endcap to J5 on the Interface Card.

2-7. Installation in Model 10269A Interface.

a. Connect W1 from J4 on the General Purpose Interface Card in the 10269A to J4 on the Dedicated Interface Module.

b. Connect W2 from J3 on the General Purpose Interface card in the 10269A to J3 on the Dedicated Interface Module.

c. Fit the Dedicated Interface Module assembly into hinge slots on the 10269A General Purpose Probe Interface Pod. Lower the cover and fasten down with screws.

2-8. OPERATING ENVIRONMENT.

2-9. The instrument may be operated in environments within the following limits:

Temperature	0°C to 55°C
Humidity	95%
Altitude	4572 metres (15 000 ft)

However, the instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-10. STORAGE AND SHIPMENT.

2-11. Environment.

2-12. The instrument may be stored or shipped in environments within the following limits:

Temperature	-40°C to +75°C
Humidity	up to 90%
Altitude	up to 15 300 metres (50 000 ft)

The instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-13. Packaging.

2-14. Original Packaging. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-15. Other Packaging. The following general instructions should be used for repacking with commercially available materials:

a. Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service center, attach tag indicating service required, return address, model number, and full serial number.)

b. Use strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3- to 4-inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

SECTION III

OPERATION

Operation of the Model 64653A is beyond the scope of this manual.

SECTION IV

PERFORMANCE VERIFICATION AND TROUBLESHOOTING

The Model 64653A does not have a performance verification test. If a problem becomes apparent, perform the following troubleshooting procedure:

a. If using the 64620S State Analyzer run the Performance Verification for the Model 64650A General Purpose Preprocessor. If using the 1630A/D Logic Analyzer run the Performance Verification for that instrument. Refer to the service manuals for the 64650A and 1630A/D for Performance Verification instructions.

b. If there are no failures, assume the problem is in the 64653A. Check the cable and connections for shorts and continuity.

c. Refer to the Illustrated Parts Breakdown (Figure 6-1) and replace the PC board assembly (HP P/N 64653-66502).

NOTE:

Section VIII describes the functions performed by the 64653A PC Board

SECTION V

ADJUSTMENTS

The Model 64653A Dedicated Interface Card requires no adjustments.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains names and addresses that correspond to the manufacturers' code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviations are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual , other abbreviation forms are used with both lower case and upper case letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Electrical assemblies and their components in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Miscellaneous parts.

d. Illustrated parts breakdowns, if appropriate.

The information given for each part consists of the following:

a. The Hewlett-Packard part number.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A typical manufacturer of the part in a five-digit code.

e. The manufacturer's number for the part.

The total quantity for each part is given only once--at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Office.

6-10. SPARE PARTS KIT.

6-11. At this time no Spare Parts Kit is available for this instrument

6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minumum on any mail order (there is a minimum order amount for parts ordered through a local HP office when orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices--to provide these advantages, a check or money order must accompany each order.

6-14. Mail order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2. Replaceable Parts List

REF DES	HP PART NUMBER	C D	Q TY	DESCRIPTION	MFR CODE	MFR PART NUMBER
MP1	64653-04101	9	1	POD COVER 8086/8088 INTERFACE CARD	28480	64653-04101
MP2	4320-0095	7	1	U CHANNEL NPRN .047-IN-WD-CHANNEL	28480	4320-0095
MP3	64651-01201	2	1	STRAIN RELIEF BRACKET	28480	64651-01201
MP4	5041-3163	5	1	PIN BASE 40 PIN	28480	5041-3163
MP5	1200-0682	1	2	SOCKET IC 40 COUNT DIP DIP SLDR	28480	1200-0682
MP6	64653-66502	4	1	BOARD ASSEMBLY 8086/8088	28480	64653-66502
W7	8120-3662	0	1	CABLE ASSEMBLY	28480	8120-3662
C1	0160-5246	6	7	CAPACITOR-FXD .1 UF +80-20% 50 VDC CER	28480	0160-5246
C2	0160-5246	6		CAPACITOR-FXD .1 UF +80-20% 50 VDC CER	28480	0160-5246
C3	0160-5246	6		CAPACITOR-FXD .1 UF +80-20% 50 VDC CER	28480	0160-5246
C4	0160-5246	6		CAPACITOR-FXD .1 UF +80-20% 50 VDC CER	28480	0160-5246
C5	0160-5246	6		CAPACITOR-FXD .1 UF +80-20% 50 VDC CER	28480	0160-5246
C6	0160-5246	6		CAPACITOR-FXD .1 UF +80-20% 50 VDC CER	28480	0160-5246
C7	0160-5246	6		CAPACITOR-FXD .1 UF +80-20% 50 VDC CER	28480	0160-5246
J1	1251-3004	4	1	CONNECTOR-POST TYPE 40 DPSLDR	28480	1251-3004
J3	1251-7575	2	2	HEADER 60 PIN	28480	1251-7575
J4	1251-7575	2		HEADER 60 PIN	28480	1251-7575
J5	1251-7613	9	1	CONN POST TYPE	28480	1251-7613
WT1	1251-7697	9	1	9 PIN POST SET	28480	1251-7697
WT2	1251-5835	3	2	6 PIN POST SET	28480	1251-5835
WT3	1251-5835	3		6 PIN POST SET	28480	1251-5835
R1	0757-0283	6	2	RESISTOR 2K 1% .125W F TC=0+-100	28480	0757-0283
R2	0757-0388	2	1	RESISTOR 30.1 1% .125 F TC=0+-100	28480	0757-0388
R3	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	28480	0757-0283
RP1	1810-0275	1	2	NETWORK-RES 10-SIP 1.0K OHMX9	28480	1810-0275
RP2	1810-0275	1		NETWORK-RES 10-SIP 1.0K OHMX9	28480	1810-0275
XU1B	1200-0567	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
UX4A	1200-0638	7	3	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
UX5A	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
UX6A	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
U1A	1820-2691	0	1	IC FF TTL F D-TYPE POS-EDGE-TRIG	07263	74F74PC
U1B	1820-3219	0	1	IC FIELD PROGRAMMABLE LOGIC SEQUENCER	28480	1820-3219
U1C	1820-1470	1	1	IC MUX/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	74LS157
U2A	1820-2690	9	1	IC GATE TTL F OR QUAD 2-INP	07263	74F32
U2B	1820-2685	2	1	IC GATE TTL F NOR QUAD 2-INP	07263	74F02
U2C	1820-2757	9	10	IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL	01295	74ALS574
U3A	1820-2951	5	1	IC INVERTED BUFFER OCTAL TRI-STATE	01295	74ALS240
U3B	1820-2757	9		IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL	01295	74ALS574
U3C	1820-2757	9		IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL	01295	74ALS574
U4A	1906-0202	7	3	DIODE ARRAY 40V 400MA	28480	1906-0202
U4B	1820-2724	0	3	IC TRANSPARENT LATCH OCTAL D-TYPE	01295	74ALS573
U4C	1820-3217	8	5	IC SYNCHRONOUS COUNTERS	01295	74ALS569
U5A	1906-0202	7		DIODE ARRAY 40V 400MA	28480	1906-0202
U5B	1820-2757	9		IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL	01295	74ALS574
U5C	1820-2724	0		IC TRANSPARENT LATCH OCTAL D-TYPE	01295	74ALS573
U6A	1906-0202	7		DIODE ARRAY 40V 400MA	28480	1906-0202
U6B	1820-2757	9		IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL	01295	74ALS574
U6C	1820-2757	9		IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL	01295	74ALS574

Table 6-2. Replaceable Parts List (Cont'd)

REF DES	HP PART NUMBER	C D	Q T Y	DESCRIPTION	MFR CODE	MFR PART NUMBER
U7A	1820-2757	9		IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL	01295	74ALS574
U7B	1820-2621	6	2	IC RGTR TTL S	01295	74S225
U7C	1820-2757	9		IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL	01295	74ALS574
U8A	1820-3217	8		IC SYNCHRONOUS COUNTERS	01295	74ALS569
U8B	1820-2621	6		IC RGTR TTL S	01295	74S225
U8C	1820-2724	0		IC TRANSPARENT LATCH OCTAL D-TYPE	01295	74ALS573
U9B	1820-3217	8		IC SYNCHRONOUS COUNTERS	01295	74ALS569
U9C	1820-2757	9		IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL	01295	74ALS574
U10A	1820-3217	8		IC SYNCHRONOUS COUNTERS	01295	74ALS569
U10B	1820-3217	8		IC SYNCHRONOUS COUNTERS	01295	74ALS569
U10C	1820-2757	9		IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL	01295	74ALS574
S1	3101-0459	2	2	SWITCH-SL SPDT SUBMIN .02A 20VDC	28480	3101-0459
S2	3101-0459	2		SWITCH-SL SPDT SUBMIN .02A 20VDC	28480	3101-0459

Table 6-3. List of Manufacturers' Codes

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	ANY SATISFACTORY SUPPLIER		
01295	TEXAS INSTRUMENTS	DALLAS TX	75222
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW CA	94042
18324	SIGNETICS CORP	SUNNYVALE CA	94086
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304

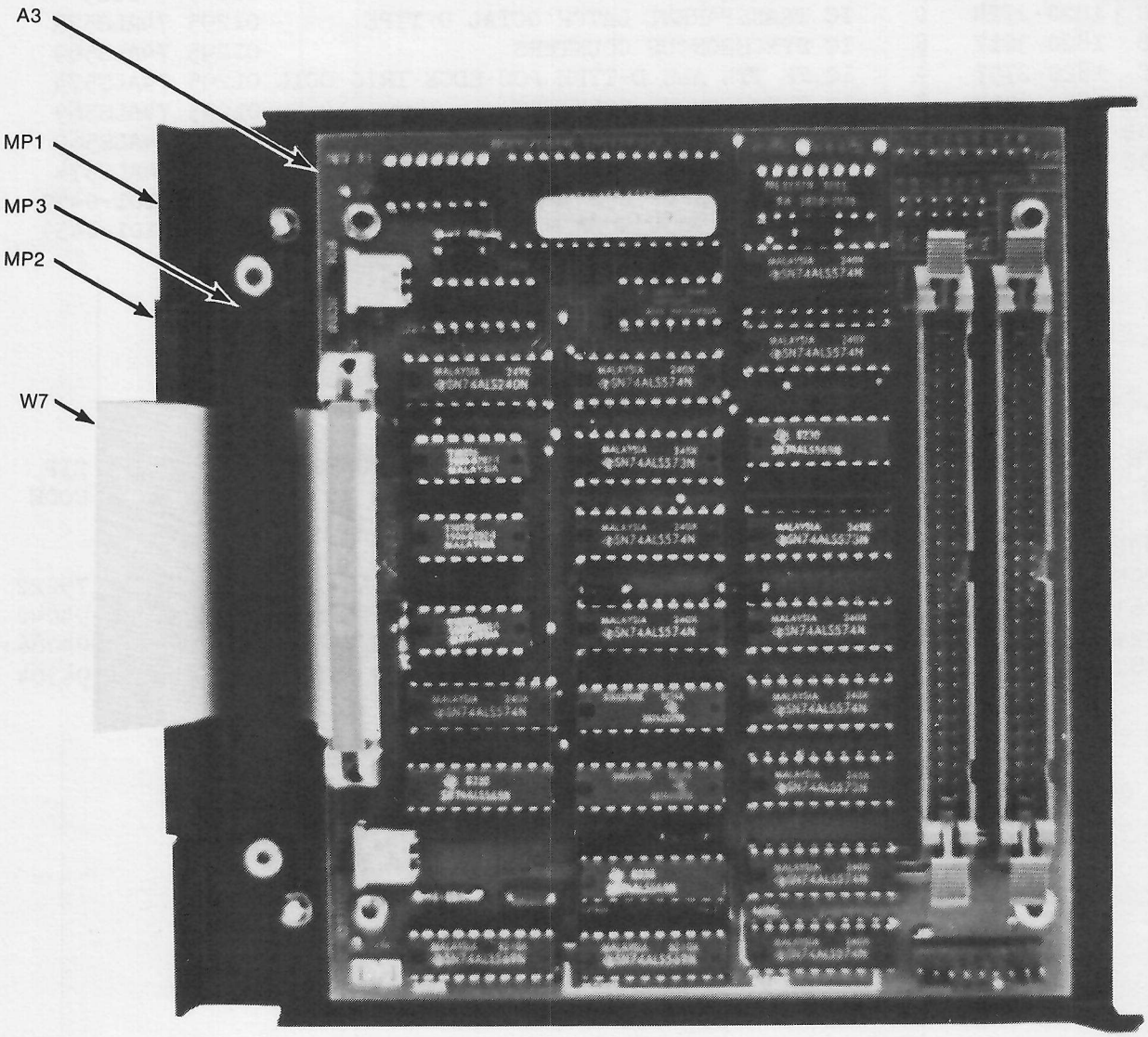


Figure 6-1. Replaceable Parts Locator

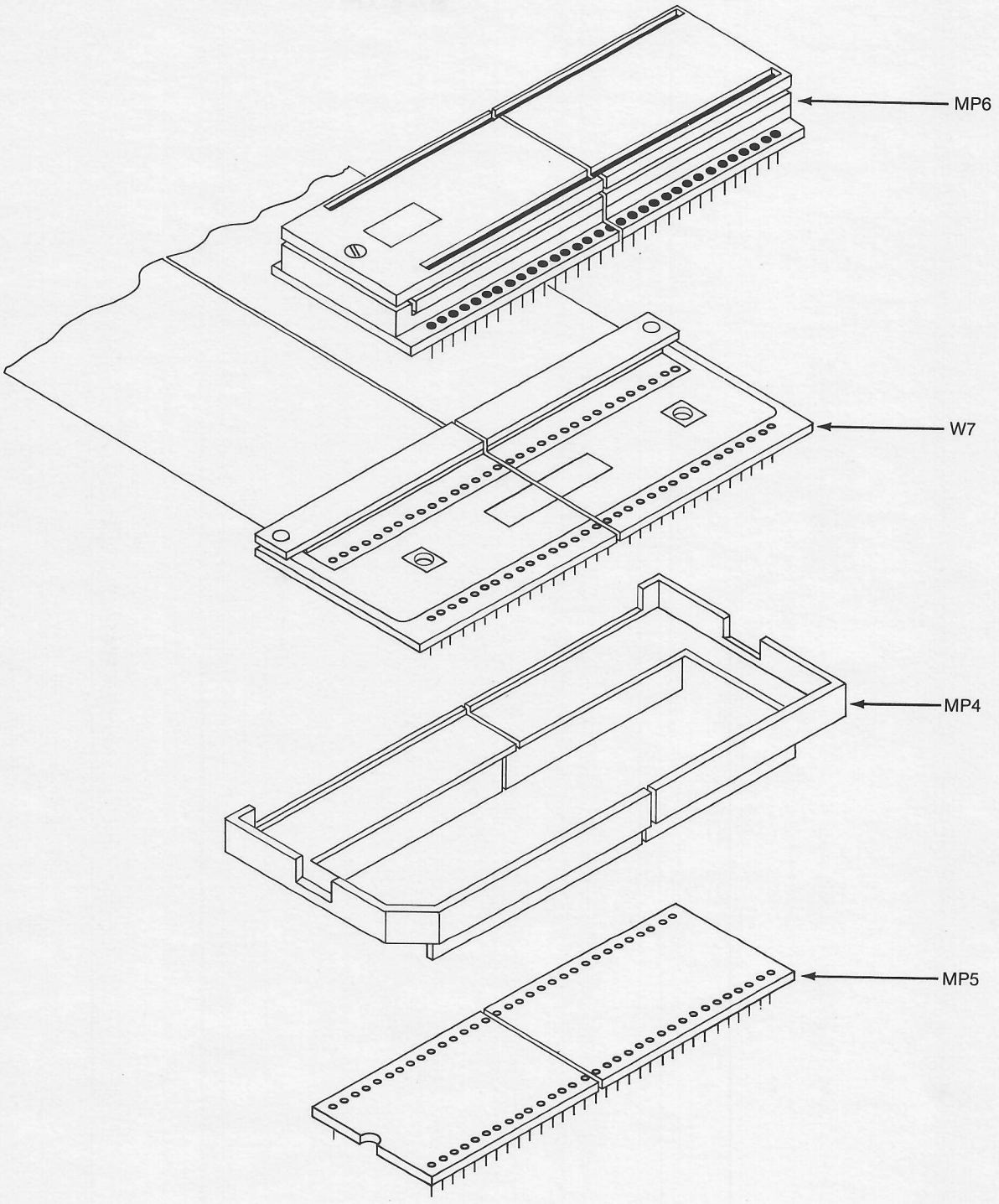


Figure 6-2. Exploded View User Probe

SECTION VII

MANUAL CHANGES

This section normally contains information for backdating this manual for models with repair numbers prior to the one shown on the title page. Because this edition includes the information for the first repair number there is no backdating material.

SECTION VIII

THEORY AND SCHEMATICS

8-1. INTRODUCTION.

8-2. This section contains block and component level theory and schematics for the 64653A Dedicated Interface Card.

8-3. LOGIC CONVENTIONS. The positive logic convention is used for logic variables and circuits within the 64653A. Positive logic defines a "1" as the more positive voltage (high) and a "0" as the move negative logic (low).

8-4. LOGIC LEVELS. TTL high--2.0 Vdc low--0.8 Vdc

8-5. POWER SUPPLIES. The mainframe supplies +5 volts to the Dedicated Interface Card.

8-6. The block diagram, schematic, component locator, and other service information are provided in foldout service sheets to help in servicing the Dedicated Interface Card.

8-7. THEORY.

8-8. OVERVIEW.

8-9. There are several functions that are unique to the 64653A 8086/8088 Interface Card. First, the multiplexed address/data bus must be separated so that all information can be sent to the logic analyzer in one state. Second, the status information from the two CPU's must be decoded. The definition of the status signals depends on two factors: which CPU is being monitored and whether the CPU is running in minimum or maximum mode. The circuitry of the interface module, illustrated in Figures 8-4 and 8-6, is described in the following paragraphs.

8-10. All information from the CPU is buffered and latched by the Bus Latch (U3B,U4B,U7A,U5B) on each CPU clock cycle. This latched information is then available to the other sections of the interface module. When the Bus Latch holds the address of a memory or I/O transfer this information is moved to the Address Latch (U3C,U9C,U10C). When the Bus Latch holds the data from that transfer, the Data Buffer allows that data to be sent to the logic analyzer along with the previously sampled address. The Controller (U1B) generates status to indicate what kind of transfer was made along with a clock signal (CLK 0) for the logic analyzer. The Controller also generates signals that tell the Address Latch when to accept an address and the Data Buffer when it should allow data to pass through. This process is performed for every bus operation, including instruction fetches, if the CPU is in minimum mode. It is also performed when the CPU is in maximum mode and the user has selected to not dequeue instructions. If the user desires to see executed instructions the BUS/EXECUTED switch is placed in the EXECUTED position and the operation is modified as follows.

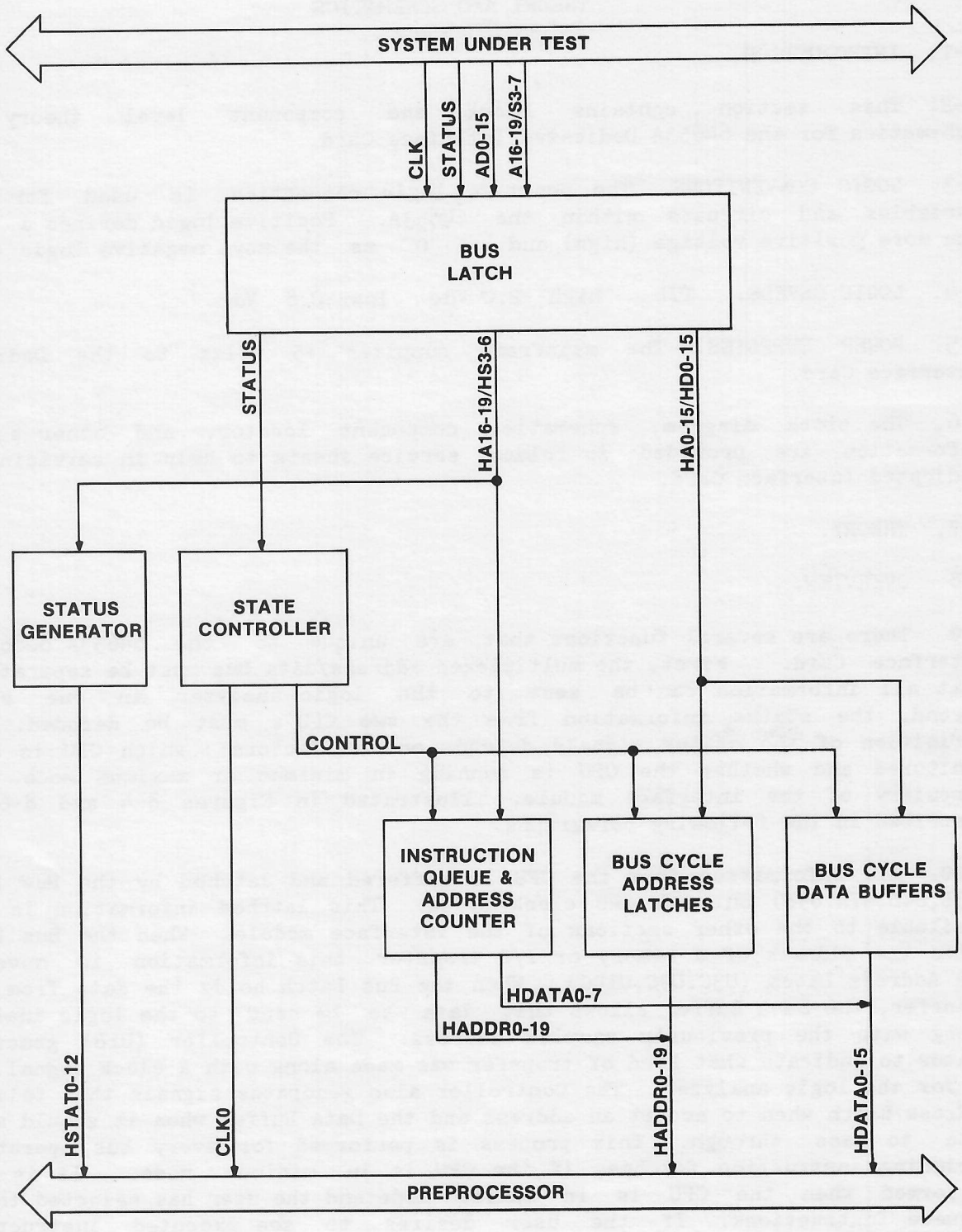


Figure 8-1. Model 64653A Block Diagram

8-11. In the EXECUTED mode, bus operations that fetch 8086/8088 instructions from memory are not immediately sent to the logic analyzer. Instead, the instructions are input into the Instruction Queue (U7B,U8B). This queue duplicates the function of the instruction queue that is inside the CPU. When the queue status lines from the CPU indicate that it is executing a byte from its queue the corresponding byte is pulled from the Instruction Queue on the interface module and sent to the analyzer along with an address from the Address Counter. The Controller is completely responsible for controlling the operation of the Instruction Queue and the Address Counter. The Controller identifies which bus operations are CPU instruction fetches and enters them into the Instruction Queue. It also monitors the CPU operation and sends instructions to the logic analyzer as they are executed. When the CPU executes a program transfer instruction, the Controller clears the Instruction Queue and loads a new value into the Address Counter.

8-12. While in the EXECUTED mode bus operations that are not CPU instruction fetches will immediately be sent to the logic analyzer. This includes all bus operations that are performed by a coprocessor that may be sharing the bus with the 8086/8088. One result of this instruction dequeueing is that for instructions that cause a bus operation, such as a memory or I/O read or write, the executed instruction will be immediately followed by the resulting bus operation. Priority is always given to executed instructions if an instruction and a bus operation need to be sent to the logic analyzer at the same time. If a conflict does occur the status will indicate that a bus operation has been lost. This conflict can occur only with a coprocessor and even then it is a rare event.

8-13. There are several resources that are available to the 64620S user in the form of a wire wrap area at the upper right corner of the interface module.

8-14. First, there are three signals labeled STM, ACK, and HLT. The STM and HLT lines are driven by the logic analyzer through the Preprocessor. These lines are available to the user to assert interrupt requests, halt requests, or other similar operations in the system under test. The ACK line is an acknowledge for the STM line when the Preprocessor has been programmed in the Preprocessor Specification to operate in the handshake mode of operation. For further information refer to the 64650A General Purpose Preprocessor Operation Manual. STM, ACK, and HALT are all active low signals. STM and HLT are open collector outputs from the Preprocessor.

8-15. Second, there are two pins labeled CK6 and CK7. These are the upper two of the eight analysis clock channels. They can be used as additional clock or clock qualifier lines.

8-16. Third, the upper six data channels of Data Pod 3 are available in the wirewrap area. These analysis channels might be used to monitor control signals or input/output ports in the target system.

8-17. BLOCK DESCRIPTION.

8-18. CPU Bus Latches. (Service Sheet 1, U3B,U4B,U7A,U5B)

8-19. The majority of the CPU information is sampled with the Bus latch driven by the inverted CPU clock (ICLKA, ICLKB or ICLK). This unqualified clock sampling allows the interface module to run with a CPU as fast as 10 MHz. When the bus flip flops hold valid information it is moved to other latches. Some of the CPU signals (S0, S1, S2, and READY) are sampled with U4B, a transparent latch driven by ICLKA. This means that these signals are sampled in the middle of a CPU state but the information is available during that state for the Controller, U1B.

8-20. The QS0/ALE signal is sampled by U1A on the rising edge of the CPU clock. This is when the min mode ALE signal is valid; the max mode QS0 is also valid at this time. It is then passed through a flip flop, U3B that is clocked by ICLKA so that it will be synchronous with the Controller, U1B.

8-21. State Controller. (Service Sheet 1, U1B)

8-22. The state controller, U1B, is the master of most of the functional blocks on the interface module. It has as inputs all the status information from the CPU plus the output of two manual switches. One switch selects between the 8086 or 8088 CPU and the other switch determines whether executed or fetched instructions are sent to the logic analyzer. The Controller operates synchronously with the CPU since it is driven by the inverted CPU clock.

8-23. The Controller provides several signals which control the operation of the instruction queue. LENLDQ is inverted and input to the 74S225 FIFO's (U7B,U8B) at pin 1. The CPU clock is inverted twice to produce IICLK and input to the FIFO's at pin 19. Pin 1 functions as an active high enable to the rising edge of the clock, pin 19. The PUNLDQ signal will pull one byte of code from the queue on each rising edge. The instruction queue is emptied when the controller issues the LCLRQ command. LENLOBYTE and LENHIBYTE are used to direct the low byte or the high byte into the queue, respectively.

8-24. The instruction queue address counter receives some of the same signals that control the queue. LEXBYTE enables the counter to count up on the next rising edge of ICLKA (U4A) or ICLKB (U8A,U9B,U10A, U10B). LCLRQ instructs the counter to parallel load a new value from the CPU bus. The counter outputs are enabled when LEXBYTE is low.

8-25. The Controller partially controls information flow to the logic analyzer. The Controller generates a signal, HSTAT7, which is high when there is a bus cycle that needs to be sent to the logic analyzer. This signal is Nored with HEXBYTE and then NORed with ICLKB to generate the analysis strobe CLK0. If the executed mode is selected, the controller gives first priority to the executed instructions. Other bus cycles will normally fit between the instructions with no conflict, but there may be a conflict if the CPU is running with a coprocessor. If such a conflict occurs the bus cycle information from the coprocessor is lost and the executed byte is sent to the analyzer, HSTAT7 will be high to indicate that a bus cycle should have been sent but the other status bits will indicate an executed byte.

8-26. Status Generator. (Service Sheet 1, U1C)

8-27. The purpose of the status generator is to generate status about the state that is being sent to the analyzer. Some status is valid with address and the rest with data at the end of the cycle. In addition, the kind of status that is available is different for min and max modes of the CPU. There are also some differences between the 8086 and the 8088. The status of an executed byte has to be generated entirely since it is not a bus cycle. Some of the status is generated by the Controller.

8-28. Instruction Queue and Address Counter. (Service Sheet 2, U7B,U8B, and U4C,U8A,U9B,U10A,U10B)

8-29. The Instruction Queue located on the interface module duplicates the primary function of the queue that is in the CPU. It is made of two 16 word X 5 bit FIFO's (functioning as 16 word X 4 bit FIFO's). When the CPU does a code fetch cycle the instructions are entered into the queue instead of being sent to the analyzer. When the queue status from the CPU indicates that it has executed a first byte or next byte the corresponding byte is pulled from the interface module queue. It is matched up with its address from the address counter and sent to the analyzer. When the CPU indicates through its queue status that it is doing a program transfer both queues are emptied of any prefetched but not executed instructions.

8-30. The addresses of the bytes that are in both queues are sequential. The CPU begins fetching code from some address and continues fetching from sequential addresses until a program transfer is executed. The CPU then empties its queue and begins fetching code from a new address. After each queue flush the address of the next code fetch is loaded into the address counter. As each executed byte is pulled from the queue the counter is incremented. Like the CPU's address counter the address counter on the Interface Card is 20 bits wide. The counter is made up of five 4-bit counters that are synchronous, can be parallel loaded, and have tri-state outputs.

8-31. Bus Cycle Address Latch and Data Buffer. (Service Sheet 2, U3C,U9C,U10C and U8C,U5C)

8-32. The bus cycle address latch is made up of U3C,U9C,and U10C. They get their information from the CPU bus latches on the rising edge of PLDBUSADDR. One of the extra bits of the address latch is used to capture BHE for the Status Generator. The data buffers allow data to get to the logic analyzer when a bus cycle is being sent.

8-33. MNEMONICS.

8-34. Signals in the 64653A have been assigned mnemonics which describe the active state and function of the signal line. A prefix letter (H,L,P, or N) indicates the active state of the signal and the remaining letters indicate its function. An H prefix indicates that the function is active in the high state; an L prefix indicates that it is active in the low state. For devices that are edge sensitive the prefix "P" indicates that the function is active on the positive going edge; the prefix "N" indicates that the device is active on the negative going edge.

Table 8-1. Mnemonics

TO/FROM SYSTEM UNDER TEST

AD0-15	ADDRESS/DATA 0-15. This is the multiplexed address data bus from the 8086/8088 system under test.
A16-19/S3-6	ADDRESS 16-19/STATUS 3-6. This is a multiplexed address/status bus from the system under test.
CLK	CLOCK. This is the CPU clock from the system under test.
LBHE/S7	LOW BYTE HIGH ENABLE/STATUS 7. This is a multiplexed control/status signal from the system under test.
MN/LMX	MINIMUM/LOW MAXIMUM. The CPU under test is in minimum mode if this signal is high; it is in maximum mode if this signal is low.
QS0/(ALE)	QUEUE STATUS LINE/ADDRESS LATCH ENABLE. This signal is a queue status line if the CPU under test is in maximum mode; it is an address latch enable if the CPU is in minimum mode.
QS1/(LINTA)	QUEUE STATUS LINE/LOW INTERRUPT ACKNOWLEDGE. This signal is a queue status line if the CPU under test is in maximum mode; it is an interrupt acknowledge data strobe if the CPU is in minimum mode.
LS0/(LDEN)	LOW STATUS 0/LOW DATA ENABLE. This signal is a status line if the CPU under test is in maximum mode; it is a data enable bus control line if the CPU is in minimum mode.
LS1(DT/LR)	LOW STATUS 1(DATA TRANSMIT/LOW RECEIVE). This signal is a status line if the CPU under test is in maximum mode; it is a data transmit/receive direction control line if the CPU is in minimum mode.
LS2(M/LIO)	LOW STATUS 2(MEMORY/INPUTOUTPUT). This signal is a low status 2 line if the CPU under test is in maximum mode; it is memory high/IO low if the CPU is an 8086 in minimum mode; if the CPU is an 8088 in minimum mode the signal is high for IO and low for memory.
READY	READY. This monitors the ready input to the CPU under test; it indicates that the data transfer can be completed.

Table 8-1. Mnemonics (Cont'd)

TO/FROM THE GP PREPROCESSOR

CLK0	CLOCK 0. This signal is the qualified clock for the analyzer generated on the Dedicated Interface Card.
HD0-7	High Data 0-7. This is the bus to the Preprocessor for the Dedicated Interface Card ID number.
HADDR0-19	HIGH ADDRESS 0-19. This is the address bus to the Logic Analyzer
HDATA0-15	HIGH DATA 0-15. This is the data bus to the Logic Analyzer.
HSTAT0-12	HIGH STATUS 0-12. This is the status bus to the Logic Analyzer.

INTRA-SCHEMATIC MNEMONICS

HA0-15/HD0-15	HIGH ADDRESS/HIGH DATA 0-15. This is the internal multiplexed address/data bus on the 8086/8088 Dedicated Interface Card.
HA16-19/HS3-6	HIGH ADDRESS 16-19/HIGH STATUS 3-6. This is the internal multiplexed address/status bus on the 8086/8088 Dedicated Interface Card.
HBUSMODE	HIGH BUS MODE. This signal generated by the MODE SELECT SWITCH is in BUS mode when high, in EXECUTED mode when low.
HENLDQ	HIGH ENABLE LOAD QUEUE. LENLDQ is inverted by U3A to HENLDQ and then enables the INSTRUCTION QUEUE (U7B, U8B) to load one byte.
HEXBYTE	HIGH EXECUTED BYTE. If this signal is high an executed byte will be sent to the logic analyzer during the current cycle.
HMIN	HIGH MINIMUM. The CPU is in minimum mode when this signal is high, in maximum mode when it is low.

Table 8-1. Mnemonics (Cont'd)

HQS0MX/HALEMN	HIGH QUEUE STATUS LINE0/HIGH ADDRESS LATCH ENABLE. This is a queue status line, QS0, if the CPU is in maximum mode; it is an address latch enable if the CPU is in minimum mode.
HQS1MX/LINTAMN	HIGH QUEUE STATUS 1/LOW INTERRUPT ACKNOWLEDGE . This is a queue status line QS1 if the CPU is in maximum mode; it is an interrupt acknowledge data strobe if the CPU is in minimum mode.
HREADY	HIGH READY. This monitors the ready input to the CPU; it indicates that data transfer can be completed.
HST0	HIGH STATUS 0. Status line produced by the CONTROLLER for bus cycles only which is used to generate HSTAT0.
H8088	HIGH 8088. The CPU being monitored is 8088 if high, 8086 if low.
ICLKA	INVERTED CLOCK A. The inverted CPU clock, A output.
ICLKB	INVERTED CLOCK B. The inverted CPU clock, B output.
ICLKC	INVERTED CLOCK C. The inverted CPU clock, C output.
IICLK	INVERTED INVERTED CLOCK. The ICLKC inverted by U3A, used to clock the INSTRUCTION QUEUE.
LBHE86/HSS088	LOW BYTE HIGH ENABLE 8086/HIGH SS0 8088. This signal is byte high enable if the CPU is an 8086; it is a status line SS0 if the CPU is an 8088.
LCLRQ	LOW CLEAR QUEUE. This signal clears the Instruction queue when it is low, and instructs the address counter to parallel load a new value from the CPU bus.
LENBUSADDR	LOW ENABLE BUS ADDRESS. This signal enables the BUS CYCLE ADDRESS LATCHES to be latched.
LENLDQ	LOW ENABLE LOAD QUEUE. This signal enables the INSTRUCTION QUEUE to load in one byte.
LENHIBYTE	LOW ENABLE HIGH BYTE. This signal enables the high byte of data to be presented to the INSTRUCTION QUEUE.
LENLOBYTE	LOW ENABLE LOW BYTE. This signal enables the low byte of data to be presented to the INSTRUCTION QUEUE.

Table 8-1. Mnemonics (Cont'd)

LEXBYTE	LOW EXECUTED BYTE. If this signal is low a executed byte will be sent to the logic analyzer during the current cycle.
LNEXTEX	LOW NEXT EXECUTED. During the next state an executed byte will be sent to the logic analyzer if this signal is low.
LQS0MX/LALEMN	LOW QUEUE STATUS 0/LOW ADDRESS LATCH ENABLE. This is the HQS0MX/HALEMN signal inverted.
LS0MX/LDENMN	LOW STATUS 0 MAX/LOW DATA ENABLE MIN. This signal is S0 if the CPU is in max mode; it is a data enable bus control line if the CPU is in min mode.
LS1MX/HDTMN	LOW STATUS 1/ HIGH DATA TRANSMIT. This is status line S1 if the CPU is in maximum mode; it is data transmit (high)/receive(low) direction control line if the CPU is in min mode.
LS2MX/HMEMMN	LOW STATUS 2/ HIGH MEMORY. This is status line S2 if the CPU is in max mode; it is memory (high/IO low) if the CPU is an 8086 in minimum mode. If the CPU is an 8088 in minimum mode the signal is high for IO and low for memory.
L8088	LOW 8088. If this line is low the CPU being monitored is an 8088; if it is high the CPU being monitored is an 8086.
PLDBUSADDR	POSITIVE LOAD BUS ADDRESS. The positive edge of this signal loads the BUS CYCLE ADDRESS LATCHES.
PUNLDQ	POSITIVE UNLOAD QUEUE. The positive edge of this signal enables the INSTRUCTION QUEUE to unload a byte.

Table 8-2. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

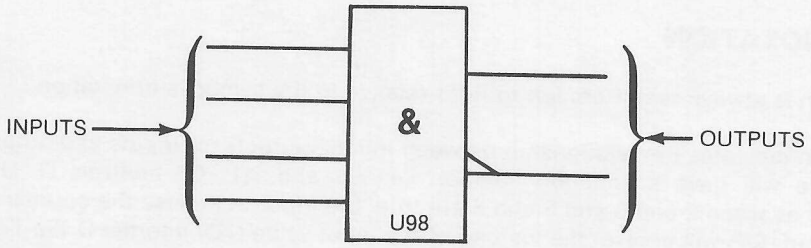
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

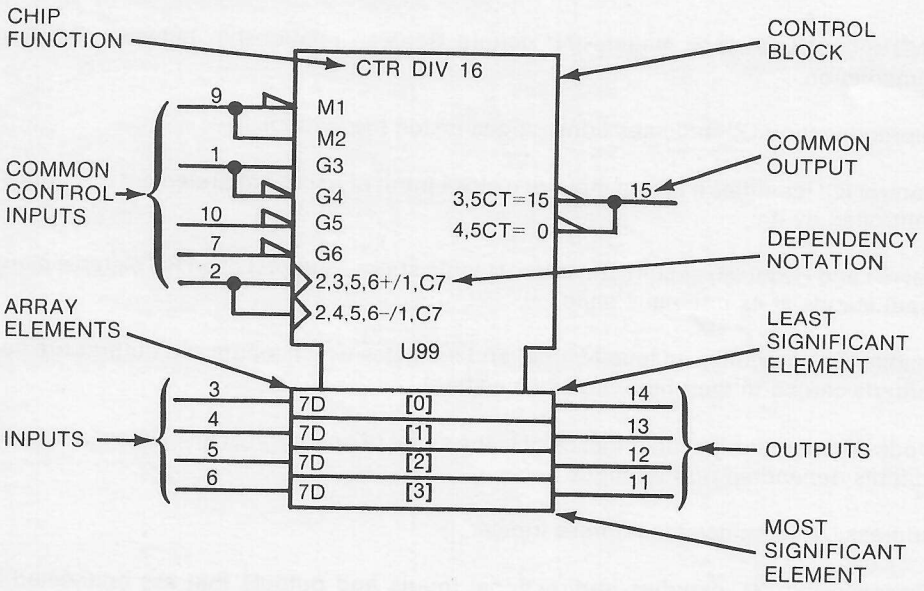
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in [ ]).

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Table 8-2. Logic Symbols (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-2. Logic Symbols (Cont'd)

OTHER SYMBOLS

∩ Analog Signal	◺◿ Inversion	→ Shift Right (or down)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
} { Bit Grouping	—x— Nonlogic Input/Output	▽ Tri-State
▷ Buffer	◇ Open Circuit (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	◇ Open Circuit (external resistor)	( ) Used for factoring terms using algebraic techniques.
▷ Dynamic	≥1 OR	[ ] Information not defined.
=1 Exclusive OR	▽ Passive Pull Down (internal resistor)	Φ Logic symbol not defined due to complexity.
⊓ Hysteresis	◇ Passive Pull Up (internal resistor)	
? Interrogation	⊓ Postponed	
— Internal Connection	← Shift Left (or up)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

⊓⊓	Astable
100 ns	Delay
1⊓	Nonretriggerable Monostable
NV	Nonvolatile
⊓⊓	Retriggerable Monostable

Table 8-3. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

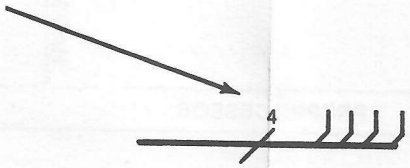
COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

1 3 NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION. LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

A CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS



(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

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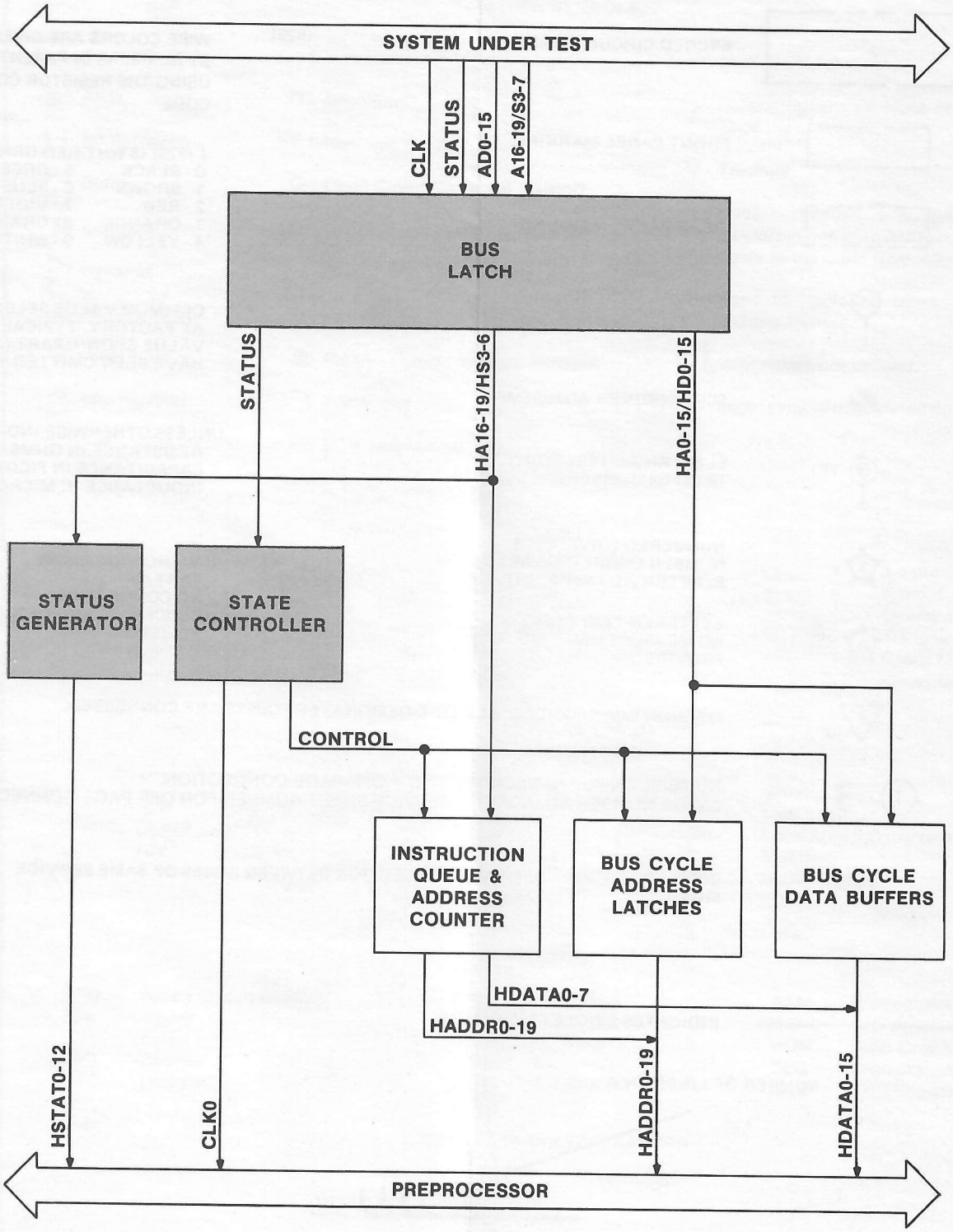
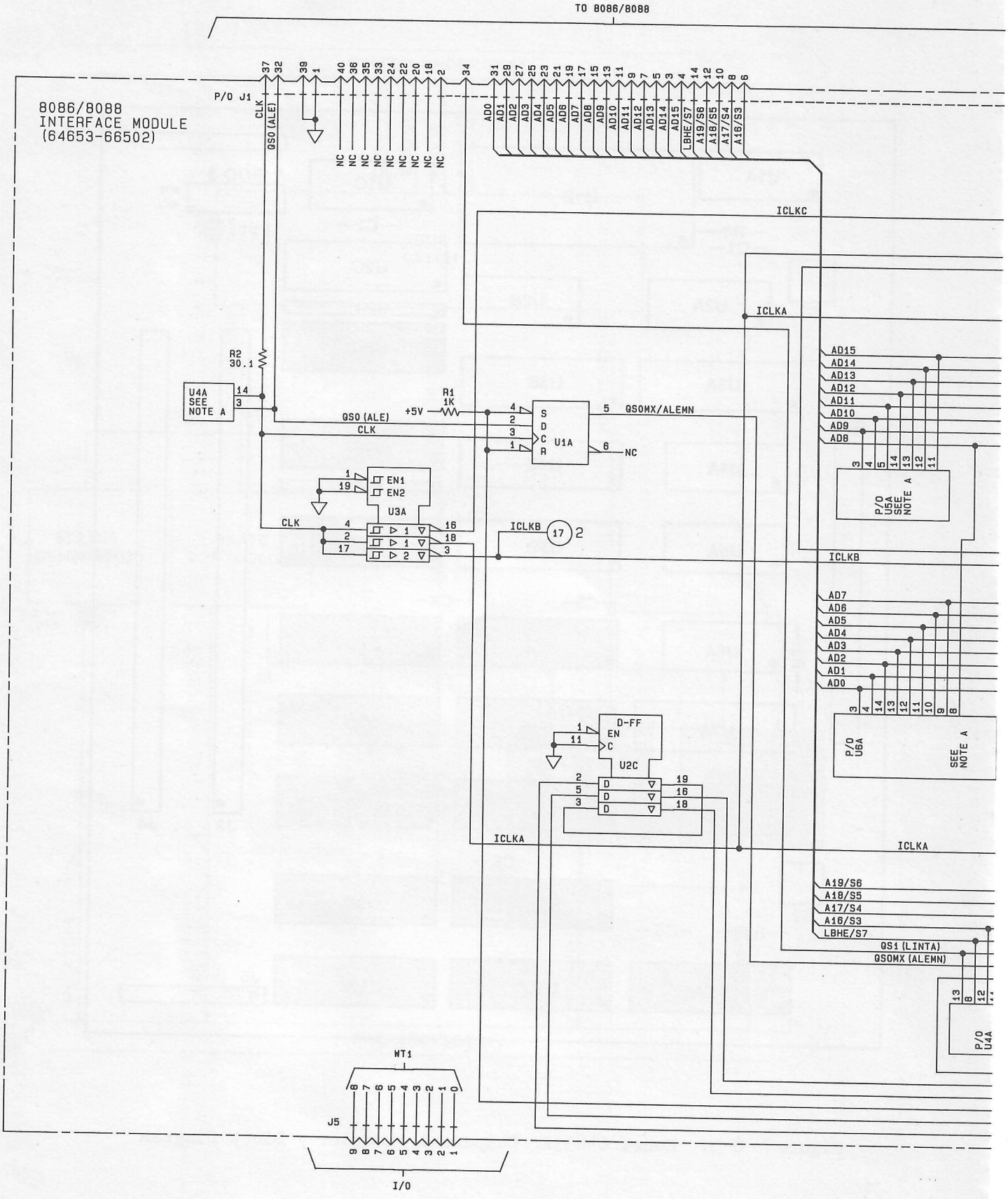
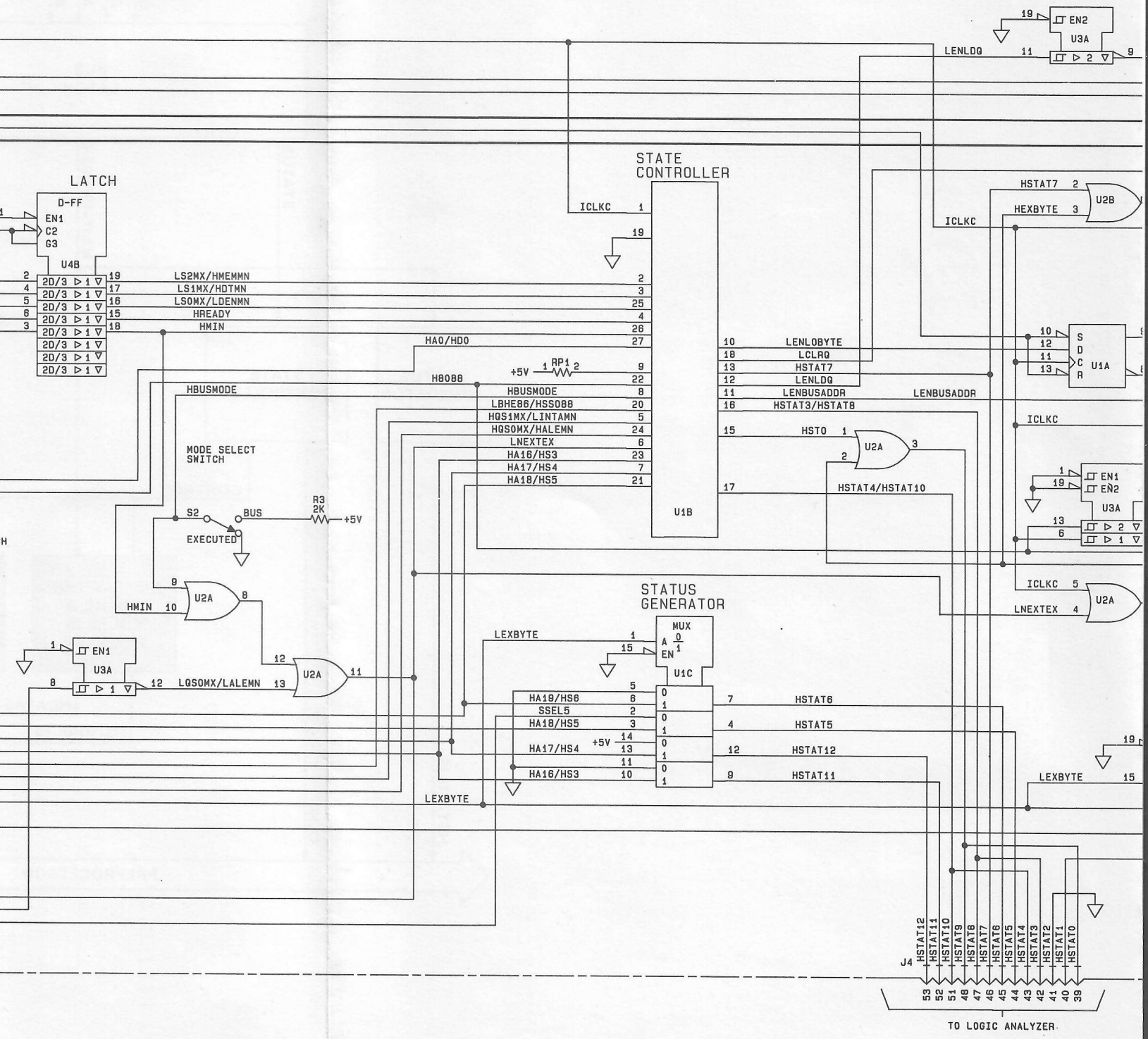
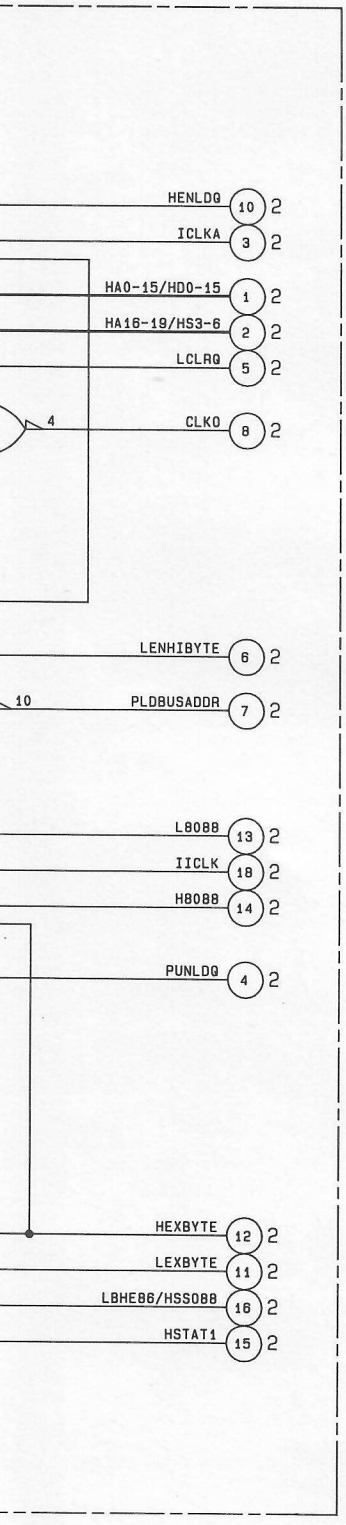

SYSTEM UNDER TEST
CLK
STATUS
AD0-15
A16-19/S3-7
BUS LATCH
STATUS
HA16-19/HS3-6
HA0-15/HD0-15
STATUS GENERATOR
STATE CONTROLLER
CONTROL
INSTRUCTION QUEUE & ADDRESS COUNTER
BUS CYCLE ADDRESS LATCHES
BUS CYCLE DATA BUFFERS
HDATA0-7
HADDR0-19
HSTAT0-12
CLK0
HADDR0-19
HDATA0-15
PREPROCESSOR


TO 8086/8088
8086/8088
INTERFACE MODULE
(64653-66502)
P/O J1
CLK
QS0 (ALE)
NC
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
LBHE/S7
A19/S6
A18/S5
A17/S4
A16/S3
ICLKC
ICLKA
R2
30.1
U4A
SEE
NOTE A
R1
1K
+5V
QS0 (ALE)
CLK
S
D
C
R
U1A
QSOMX/ALEMN
NC
EN1
EN2
U3A
ICLKB
P/O
U5A
SEE
NOTE A
D-FF
EN
C
U2C
P/O
U6A
SEE
NOTE A
QS1 (LINTA)
QSOMX (ALEMN)
P/O
U4A
WT1
J5
I/O


LATCH
D-FF
EN1
C2
G3
U4B
2D/3
LS2MX/HMEMMN
LS1MX/HDTMN
LSOMX/LDENMN
HREADY
HMIN
STATE CONTROLLER
ICLKC
U1B
HA0/HD0
H8088
+5V
RP1
HBUSMODE
LBHE86/HSS088
HQS1MX/LINTAMN
HQSOMX/HALEMN
LNEXTEX
HA16/HS3
HA17/HS4
HA18/HS5
MODE SELECT SWITCH
S2
BUS
EXECUTED
R3 2K
U2A
HMIN
EN1
U3A
LQSOMX/LALEMN
STATUS GENERATOR
LEXBYTE
MUX
U1C
HA19/HS6
SSEL5
HA18/HS5
HA17/HS4
HA16/HS3
HSTAT6
HSTAT5
HSTAT12
HSTAT11
LENLDQ
EN2
U3A
HSTAT7
HEXBYTE
U2B
ICLKC
LENLOBYTE
LCLRQ
HSTAT7
LENLDQ
LENBUSADDR
HSTAT3/HSTAT8
HSTO
U2A
HSTAT4/HSTAT10
S
D
C
R
U1A
ICLKC
EN1
EN2
U3A
ICLKC
LNEXTEX
U2A
LEXBYTE
J4
HSTAT12
HSTAT11
HSTAT10
HSTAT9
HSTAT8
HSTAT7
HSTAT6
HSTAT5
HSTAT4
HSTAT3
HSTAT2
HSTAT1
HSTAT0
TO LOGIC ANALYZER



IC'S ON THIS SCHEMATIC

REF MFR	HP PART NUMBER	MFR PART NUMBER	VCC	GND
U1A	1820-2691	74F74	14	7
U1B	1820-3219	1820-3219	28	14
U1C	1820-1470	74LS157	16	8
U2A	1820-2690	74F32	14	7
U2B	1820-2685	74F02	14	7
U2C	1820-2757	74ALS574	20	10
U3A	1820-2951	74ALS240	20	10
U3B	1820-2757	74ALS574	20	10
U4A	1906-0202			
U4B	1820-2724	74ALS573	20	10
U5A	1906-0202			
U5B	1820-2757	74ALS574	20	10
U6A	1906-0202			
U6B	1820-2757	74ALS574	20	10

PARTS ON THIS SCHEMATIC

R1,R2,R3

CONNECTORS ON THIS SCHEMATIC

J1,J4,J5

NOTE A

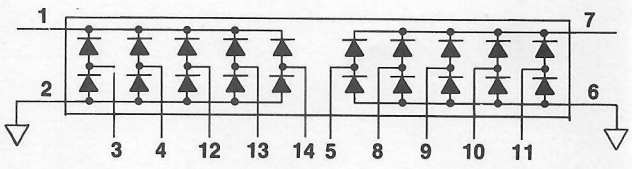
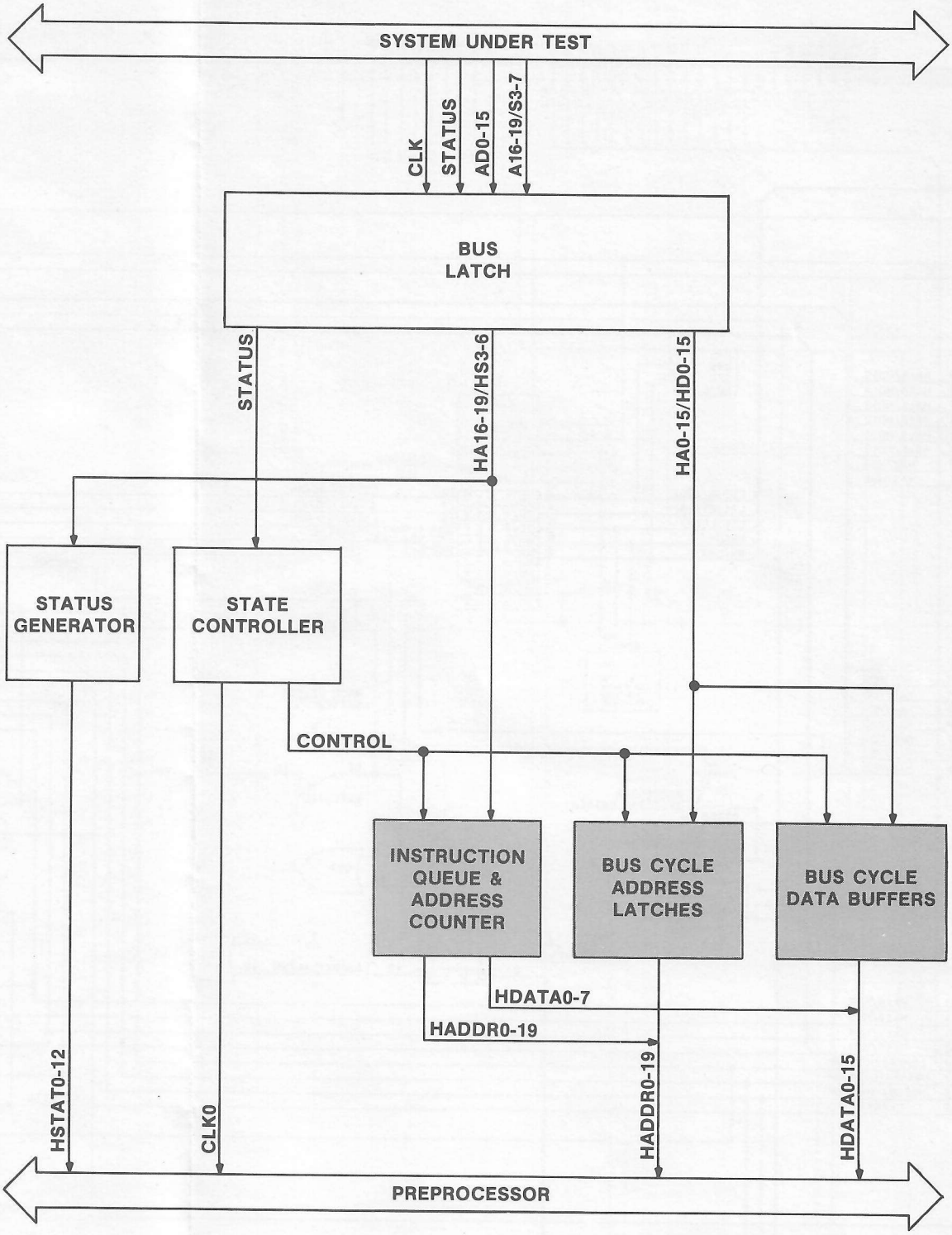


Figure 8-4. Service Sheet 1


SYSTEM UNDER TEST
CLK
STATUS
AD0-15
A16-19/S3-7
BUS LATCH
STATUS
HA16-19/HS3-6
HA0-15/HD0-15
STATUS GENERATOR
STATE CONTROLLER
CONTROL
INSTRUCTION QUEUE & ADDRESS COUNTER
BUS CYCLE ADDRESS LATCHES
BUS CYCLE DATA BUFFERS
HDATA0-7
HADDR0-19
HSTAT0-12
CLK0
HADDR0-19
HDATA0-15
PREPROCESSOR

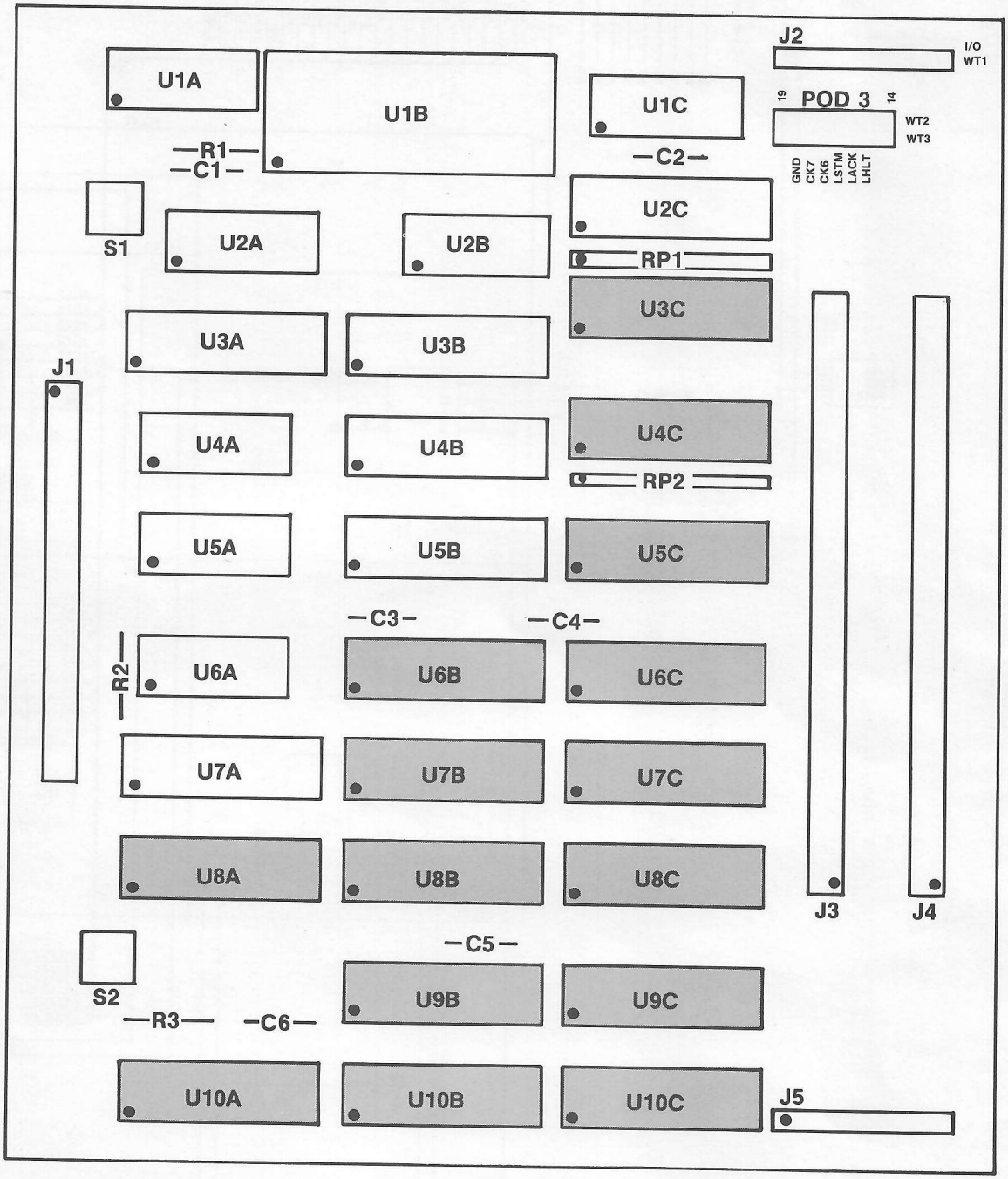
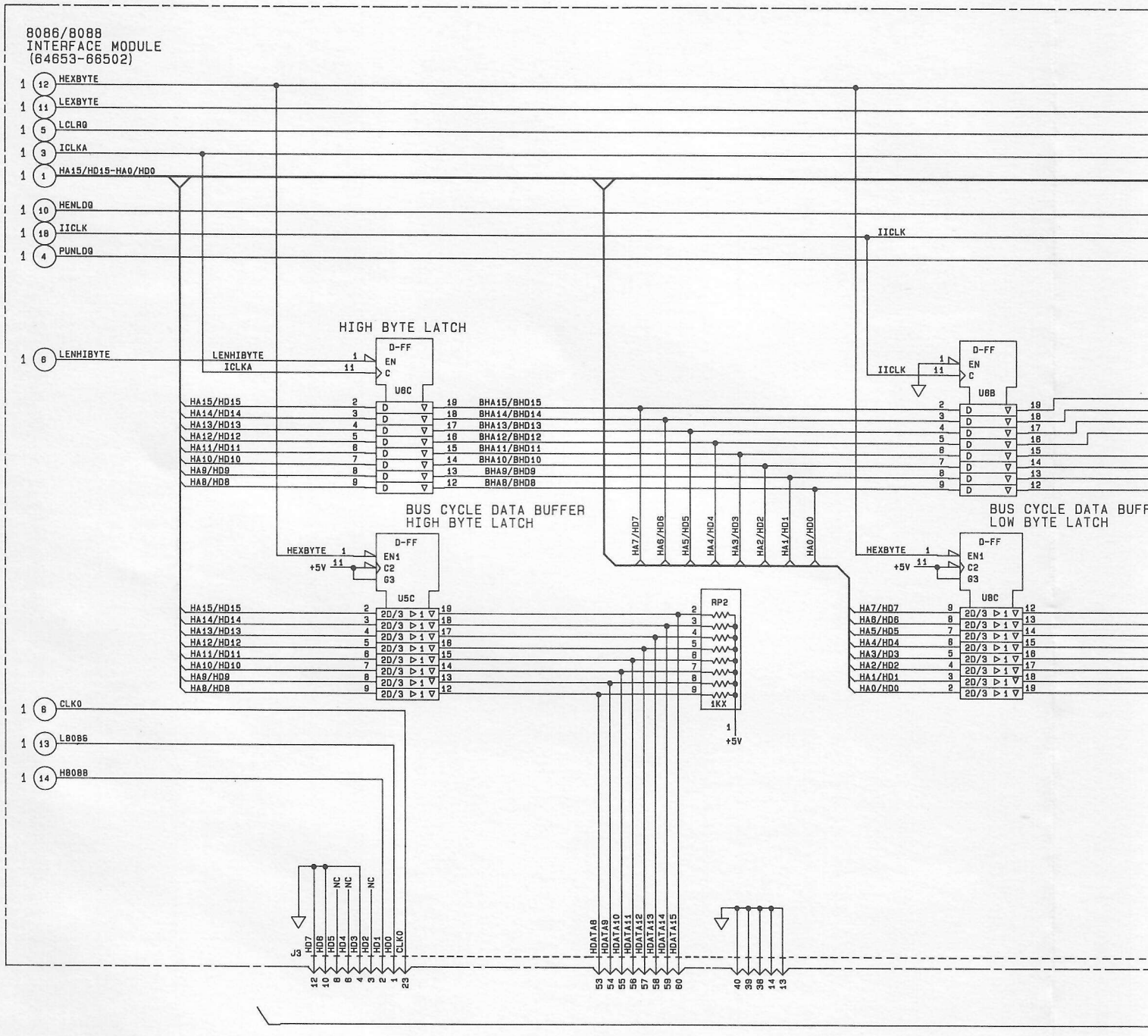
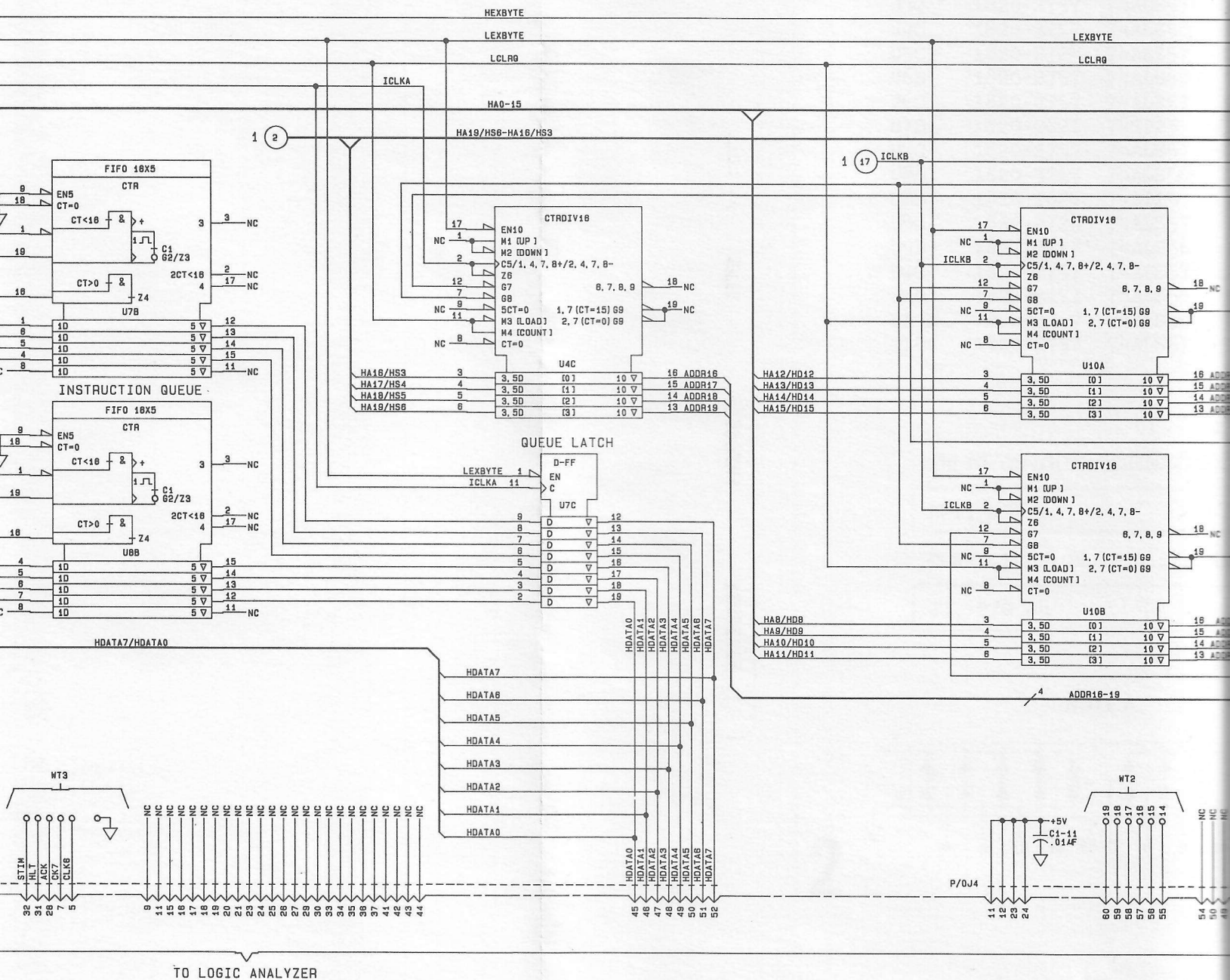
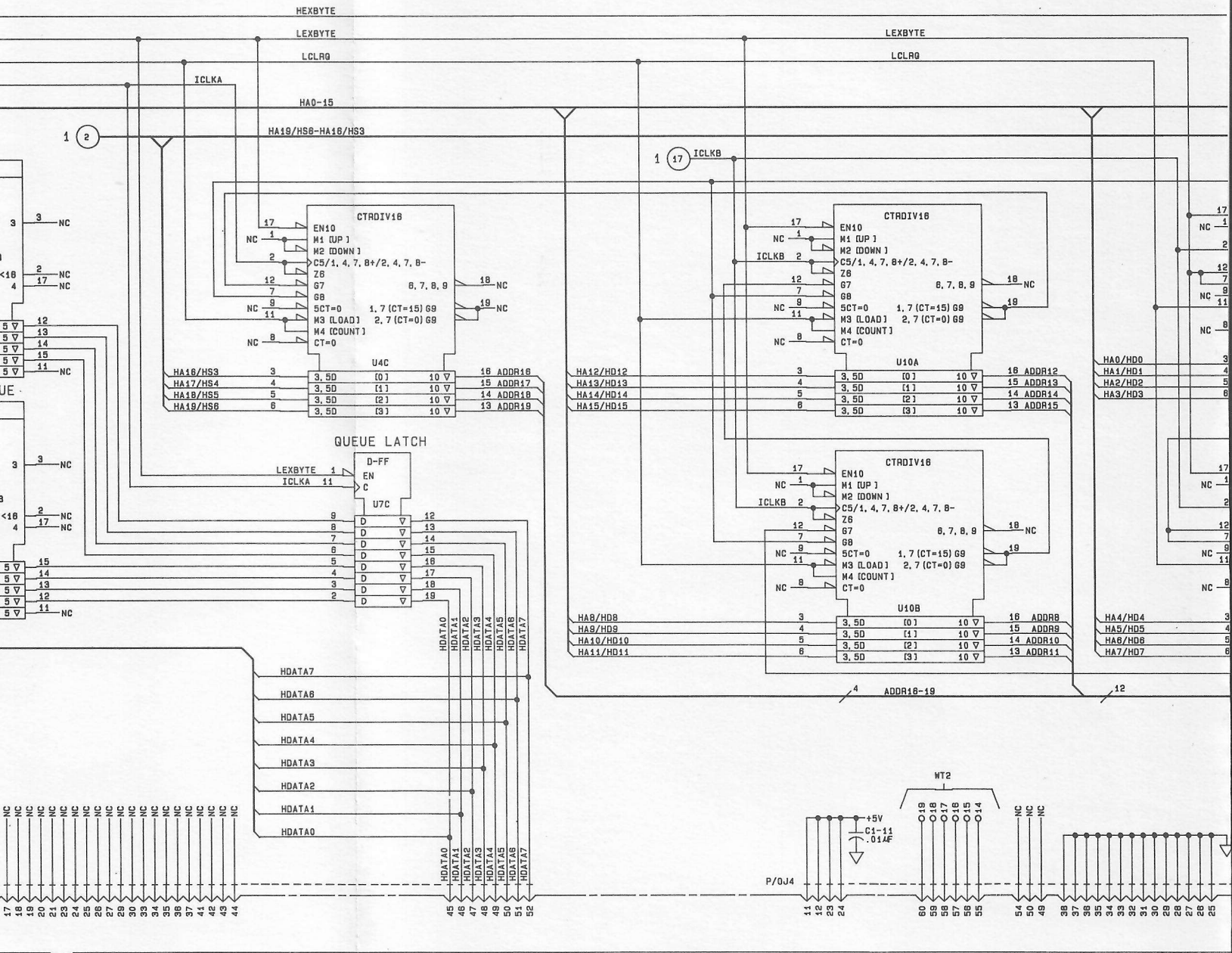


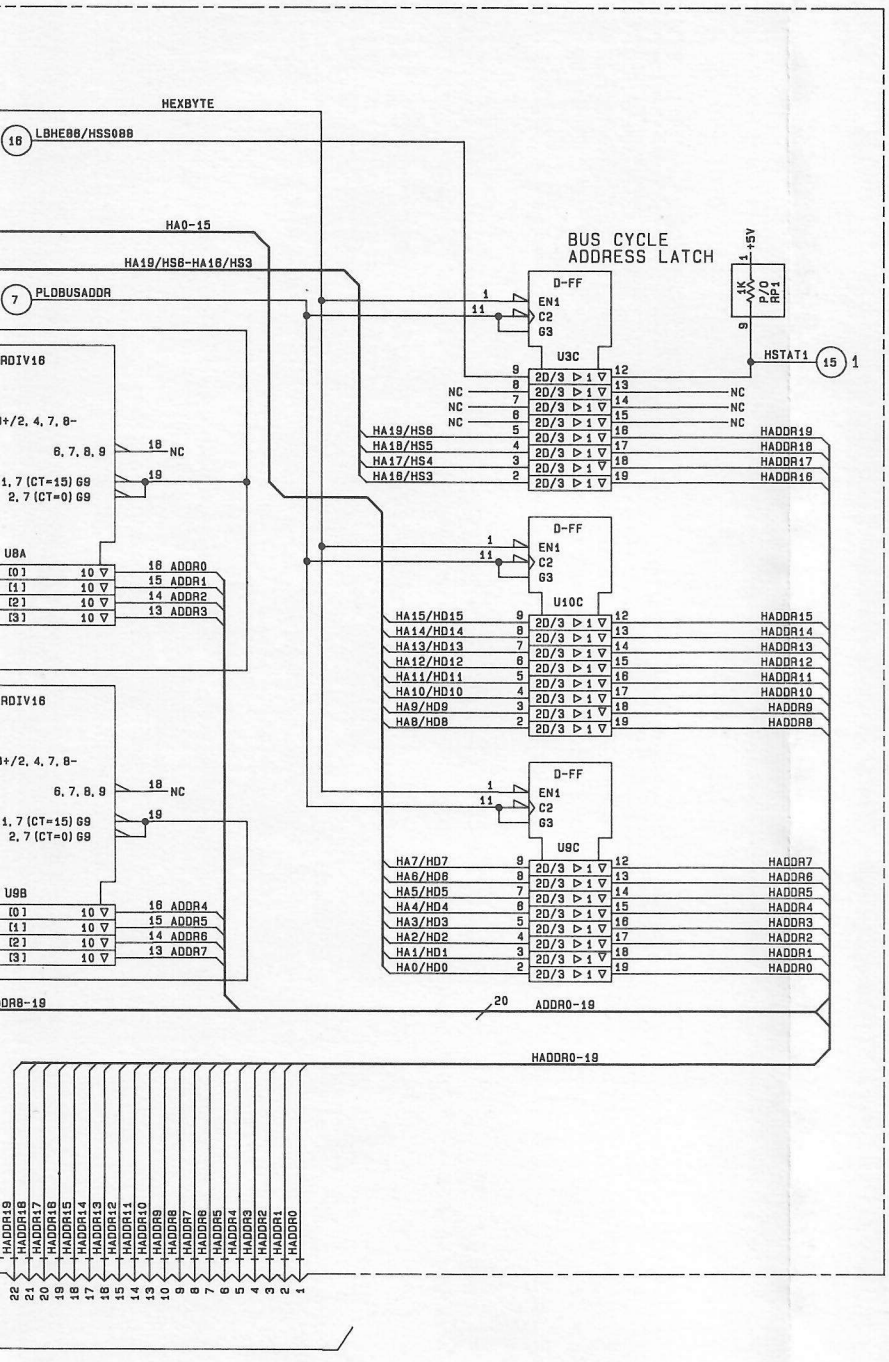
Figure 8-3. Model 64653A Component Locator / Block Diagram


8086/8088
INTERFACE MODULE
(64653-66502)
HEXBYTE
LEXBYTE
LCLRQ
ICLKA
HA15/HD15-HA0/HD0
HENLDQ
IICLK
PUNLDQ
HIGH BYTE LATCH
LENHIBYTE
D-FF
EN
C
U6C
U6B
BUS CYCLE DATA BUFFER
HIGH BYTE LATCH
BUS CYCLE DATA BUFF
LOW BYTE LATCH
EN1
C2
G3
U5C
U8C
2D/3
RP2
1KX
+5V
CLKO
L8086
H8088
J3
NC
HDATA8
HDATA9
HDATA10
HDATA11
HDATA12
HDATA13
HDATA14
HDATA15


HEXBYTE
LEXBYTE
LCLRQ
ICLKA
HA0-15
HA19/HS6-HA16/HS3
ICLKB
FIFO 16X5
CTR
EN5
CT=0
CT<16
CT>0
C1
G2/Z3
2CT<16
Z4
U7B
U8B
INSTRUCTION QUEUE
CTRDIV16
EN10
M1 (UP)
M2 (DOWN)
C5/1, 4, 7, 8+/2, 4, 7, 8-
Z6
G7
G8
5CT=0
1, 7 (CT=15) G9
M3 (LOAD)
2, 7 (CT=0) G9
M4 (COUNT)
CT=0
U4C
U10A
U10B
HA16/HS3
HA17/HS4
HA18/HS5
HA19/HS6
ADDR16
ADDR17
ADDR18
ADDR19
HA12/HD12
HA13/HD13
HA14/HD14
HA15/HD15
HA8/HD8
HA9/HD9
HA10/HD10
HA11/HD11
QUEUE LATCH
D-FF
EN
U7C
HDATA7/HDATA0
HDATA7
HDATA6
HDATA5
HDATA4
HDATA3
HDATA2
HDATA1
HDATA0
ADDR18-19
WT3
STIM
HLT
ACK
CK7
CLK8
WT2
+5V
C1-11
.01AF
P/OJ4
TO LOGIC ANALYZER



LOGIC ANALYZER



REF DES	HP PART NUMBER	MFR PART NUMBER	VCC	GND
U3C	1820-2757	74ALS574	20	10
U4C	1820-3217	74ALS569	20	10
U5C	1820-2724	74ALS573	20	10
U6B	1820-2757	74ALS574	20	10
U6C	1820-2757	74ALS574	20	10
U7B	1820-2621	74S225	20	10
U7C	1820-2757	74ALS574	20	10
U8A	1820-3217	74ALS569	20	10
U8B	1820-2621	74S225	20	10
U8C	1820-2724	74ALS573	20	10
U9B	1820-3217	74ALS569	20	10
U9C	1820-2757	74ALS574	20	10
U10A	1820-3217	74ALS569	20	10
U10B	1820-3217	74ALS569	20	10
U10C	1820-2757	74ALS574	20	10

PARTS ON THIS SCHEMATIC

RP1, RP2

CONNECTORS ON THIS SCHEMATIC

J3, P/O J4

NOTE A

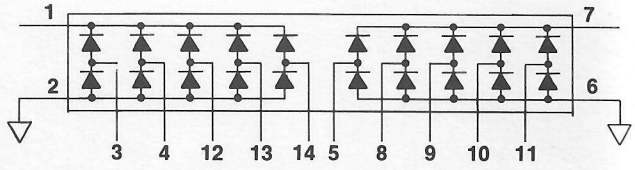


Figure 8-6. Service Sheet 2

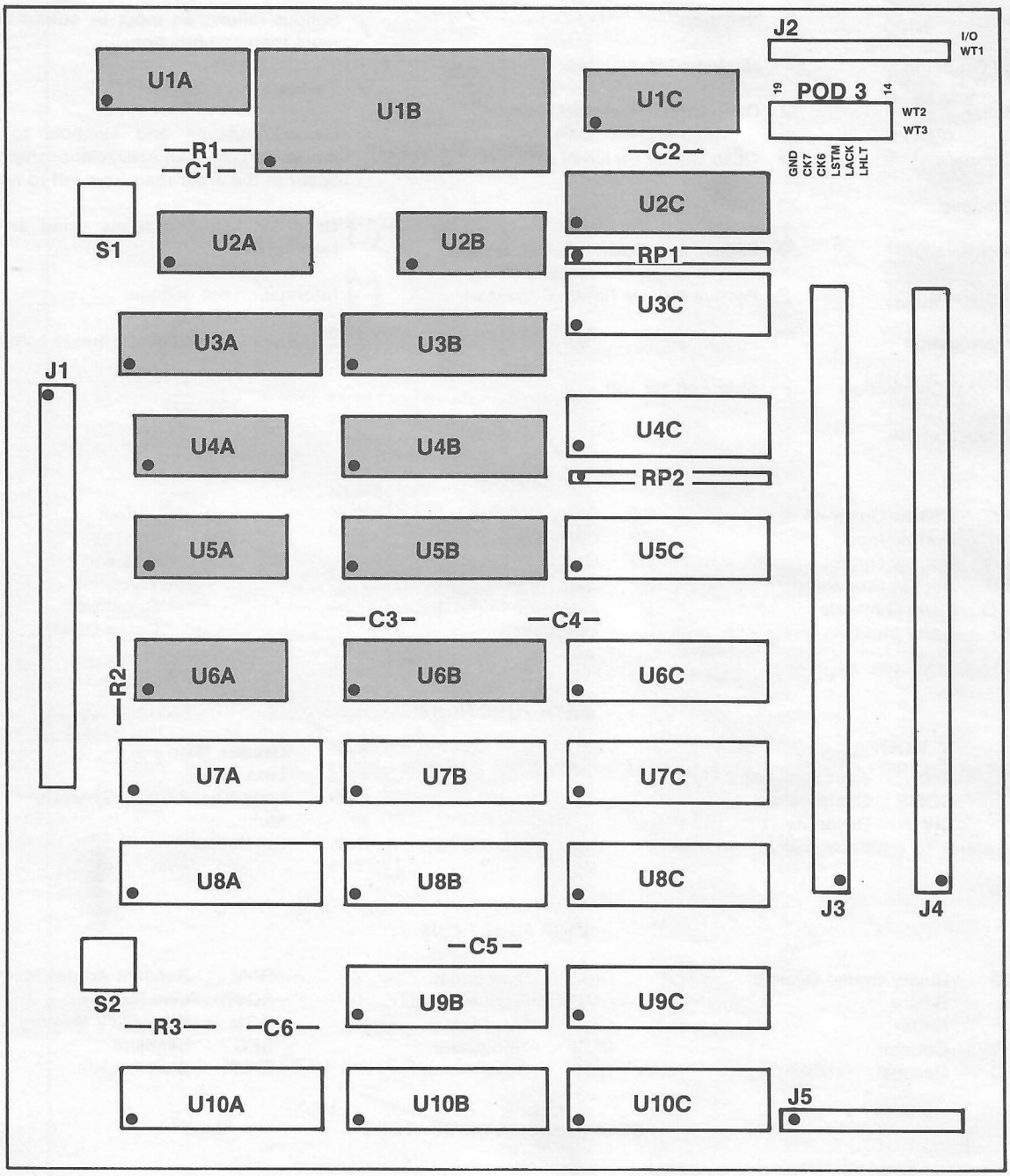


Figure 8-3. Model 64653A Component Locator / Block Diagram