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HP E2420A Motorola 68040 Preprocessor Interface User's Guide

HP E2420A Motorola 68040 Preprocessor Interface User's Guide

or the HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, IP 16511B, HP 16540/16541A,D, and HP 16550A Logic Analyzers

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Introduction

The HP E2420A Preprocessor Interface provides a complete interface between any 68040 target system and an HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, or HP 16550A Logic Analyzer.

The 68040 configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the 68040 microprocessor. The inverse assembler allows you to obtain displays of 68040 data in 68040 assembly language mnemonics.

HP 16500A Software Compatibility

The HP E2420A Preprocessor Interface requires HP 16500A system and module software version V04.01 or higher. If your software version is older than V04.01, load new HP 16500A system software with a version number of V04.01 or higher before loading the HP E2420A software. Only the Small inverse assembler can be used with the V03.01 or older HP 16500A system software.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2420A Preprocessor Interface:

HP 1650A (Limited Support)

This logic analyzer provides 1 k of memory depth with 80 channels of 25 MHz state analysis or 80 channels of 100 MHz timing analysis.

Due to the memory requirements for the inverse assemblers, the HP 1650A Logic Analyzer can only use the Small inverse assembler, so most floating point instructions are not decoded. The Burst, Generic, and Dequeing inverse assemblers can not be loaded into the HP 1650A Logic Analyzer. To increase the amount of memory in your HP 1650A so that it will be able to run the enhanced feature set of an HP 1650B, order the 10449A upgrade kit from your Hewlett-Packard Sales/Service Office.

HP 1650B, HP 16510A, HP 16510B, and HP 1652B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 16540A,D with Two HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with 112 channels of 100 MHz state or timing analysis.

HP 16550A (one or two cards)

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz of timing analysis. The logic analyzer will also support various combinations of mixed state/timing analysis.

The 80-channel logic analyzers do not provide all of the auxiliary status and control information available with the HP 16511B, HP 16550A, and HP 16540/16541A,D Logic Analyzers.

How to Use This Manual

This user's guide is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2420A Preprocessor Interface for state and timing analysis with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2420A software. It also provides information about the inverse assembler and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP E2420A.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

Table of Contents

Chapter 3: General Information

Appendix A: Troubleshooting

1

Setting Up the HP E2420A

Introduction

This chapter explains how to install and configure the HP E2420A Preprocessor Interface for state analysis with the supported logic analyzers.

Duplicating the Master Disk

Before you use the HP E2420A software, use the Duplicate Disk operation in the disk menu of your logic analyzer to make a duplicate copy of the HP E2420A master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidently deleted.

Equipment Supplied

The HP E2420A Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor circuit card and cables.
- The inverse assembly software on a 3.5-inch disk.
- Seven 100 kOhm Termination Modules (HP part number 01650-63204)
- Two jumpers (HP part number 1258-0261).
- This User's Guide.

Note

The preprocessor interface socket assembly pins are covered for shipment with either a conductive foam wafer or a conductive plastic pin protector. This is done to protect the circuitry in the preprocessor interface from electrostatic discharge (ESD), and to protect the delicate gold plated pins of the assembly from damage due to impact.

When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam or plastic pin protector.

Minimum Equipment Required

The minimum hardware for state analysis of a 68040 target system consists of the following equipment:

- An HP 1650A, HP 1650B, HP 16510A, HP 16510B, HP 1652B, HP 16511B, HP 16550A, or HP 16540/16541A,D Logic Analyzer.
- The 68040 Preprocessor Interface and Inverse Assembler (HP E2420A).

Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the HP E2420A Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

Caution

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. If they are not already connected, connect the 100 kOhm Termination Modules to the cables on the preprocessor interface (see page 1-4).
2. Set the jumpers on the HP E2420A preprocessor interface board (see page 1-5).
3. Install the preprocessor interface in the target system (see page 1-6).
4. Connect the logic analyzer probes to the termination modules on the cable connectors of the preprocessor interface board as shown in table 1-1 on page 1-9.

5. Load the logic analyzer configuration by loading one of the following configuration files:

   - For the HP 1650A, HP 1650B, HP 1652B, HP 16510A, and HP 16510B, load the configuration file C68040.
   - For the HP 16511B, load the configuration file D68040.
   - For the HP 16540/16541A,D, load the configuration file E68040.
   - For the HP 16550A (one or two cards, 4 k acquisition memory depth), load the configuration file F68040.
   - For the HP 16550A (two cards, 8 k acquisition memory depth), load the configuration file F68040D.

6. Load the appropriate inverse assembler file (see pages 1-11 through 1-13). Note that the HP 1650A logic analyzer only supports the Small inverse assembler, unless you have first installed the 10449A upgrade kit.

7. If you need to trace and disassemble code execution, disable the instruction cache to ensure proper disassembly (see page 1-7).

Note 

Do not disable the cache memory if burst transfers are to be monitored. Enabling the cache memory will allow you to view the data coming across the bus, but the code may not be properly disassembled.

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8. If you are using the 68040 Inverse Assembler, configure the MMU so that the physical addresses the preprocessor interface monitors are effectively the logical addresses (see page 1-7).

Note 

Enabling the MMU address translation may result in missing data for some applications. For more information, refer to the section "Interpreting Data" in chapter 2.

Connecting the Termination Module to the Preprocessor Interface

The 100 kOhm Termination Module (HP part number 01650-63204) properly terminates the probes of the logic analyzer. The following steps explain how to connect the termination module to the cables on the HP E2420A Preprocessor Interface:

1. Align the key on the male end of the termination module with the slot on the connector of one of the preprocessor interface cables.
2. Push the termination module into the connector.
3. Repeat steps 1 and 2 for each termination module.

For more information, refer to the user's guide for the 100 kOhm Termination Module.

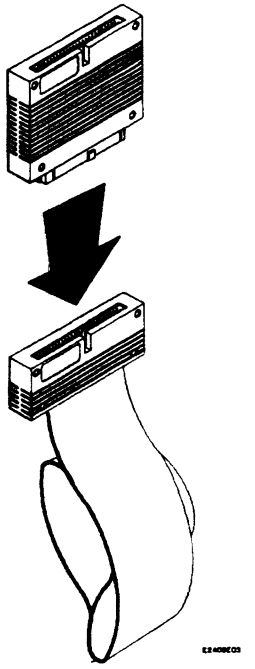


Figure 1-1. Connecting the Termination Module

Setting the Jumpers

By placing jumpers across the appropriate pins on the HP E2420A board, you can monitor the 68040 operating in the normal mode, Multiplexed Bus mode, or Data Latch Enabled (DLE) mode. The pins are labeled as shown in figure 1-2. Refer to figure 1-3 for the exact location of the pins.

- To monitor a 68040 operating in the normal mode, place both jumpers across pins A and B. The jumpers are connected across these pins when shipped from the factory.
- To monitor a 68040 operating in the multiplexed bus mode, place the first jumper across pins A and B. Then place the second jumper across pins B and C.
- To monitor a 68040 operating in the data latch enabled mode, place the first jumper across pins B and C. Then place the second jumper across pins A and B.

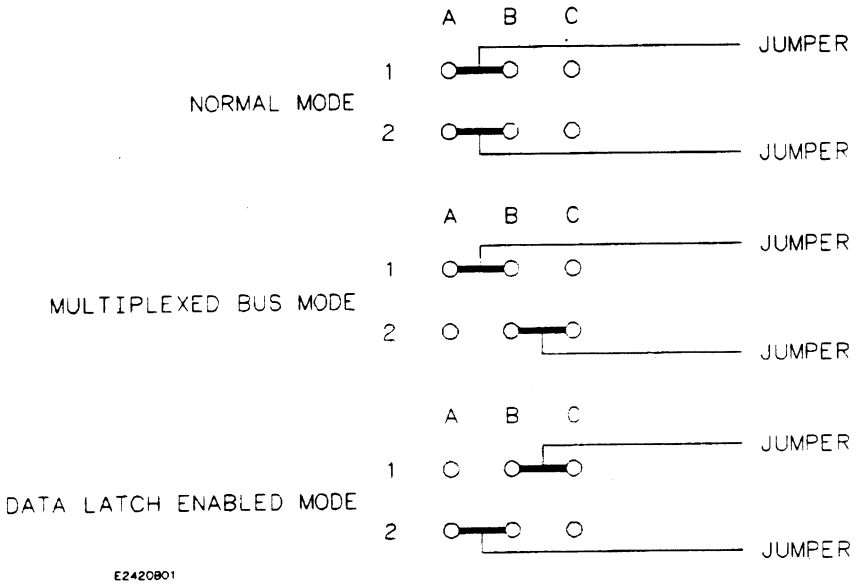


Figure 1-2. Jumpers Locations

Connecting to the Target System

The following steps explain how to connect the HP E2420A Preprocessor Interface to your target system:

Caution

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Remove the 68040 microprocessor from its socket on the target system and store it in a protected environment.

Caution

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin A1 (figure 1-3) on the preprocessor interface connector and the target system socket prior to inserting the connector in the socket. Also, take care to align the preprocessor interface connector with the socket on the target system so that all microprocessor pins are making contact.

2. Plug the preprocessor interface connector into the microprocessor socket on the target system.

Note

If the preprocessor interface connector interferes with components of the target system or if a higher profile is required, additional plastic pin guards can be added. Plastic pin guards can be ordered from Hewlett-Packard using the part number 1200-1597. However, any 179-pin PGA IC socket with a 68040 foot print and gold-plated pins can be used.

3. Plug the 68040 microprocessor into the socket of the preprocessor interface board. The socket on the preprocessor interface board is designed with low insertion force pins to allow you to install or remove the microprocessor with a minimum amount of force.

Caution 

Care must be used when removing a microprocessor or socket from the preprocessor interface board to prevent damaging the traces on the board.

4. If you need to trace and disassemble code execution, disable the instruction cache to force all instruction fetches to come in on the bus. This can be accomplished in various ways:

   - The target hardware asserts TCI (transfer cache inhibit).
   - The target hardware asserts TBI (transfer burst inhibit).
   - The target software disables the instruction cache by clearing bit 15 (instruction cache enable) in the cache control register. For example:

```
MOVE.L      #80000000,D0
MOVEC       D0,CACR
```

   - The instruction MMU is programmed to use non-cachable transparent translation for the code space.

   Refer to your 68040 user's manual for more information.

5. If you are using the 68040 Inverse Assembler, configure the MMU so that the physical addresses the preprocessor interface monitors are effectively the logical addresses. This can be done by setting bit 15 of the TC register to zero. For example:

```
MOVEQ       #0,D0
MOVEC       D0,TC
```

Note 

Enabling the MMU address translation may result in missing data for some applications. For more information, refer to the section "Interpreting Data" in chapter 2.

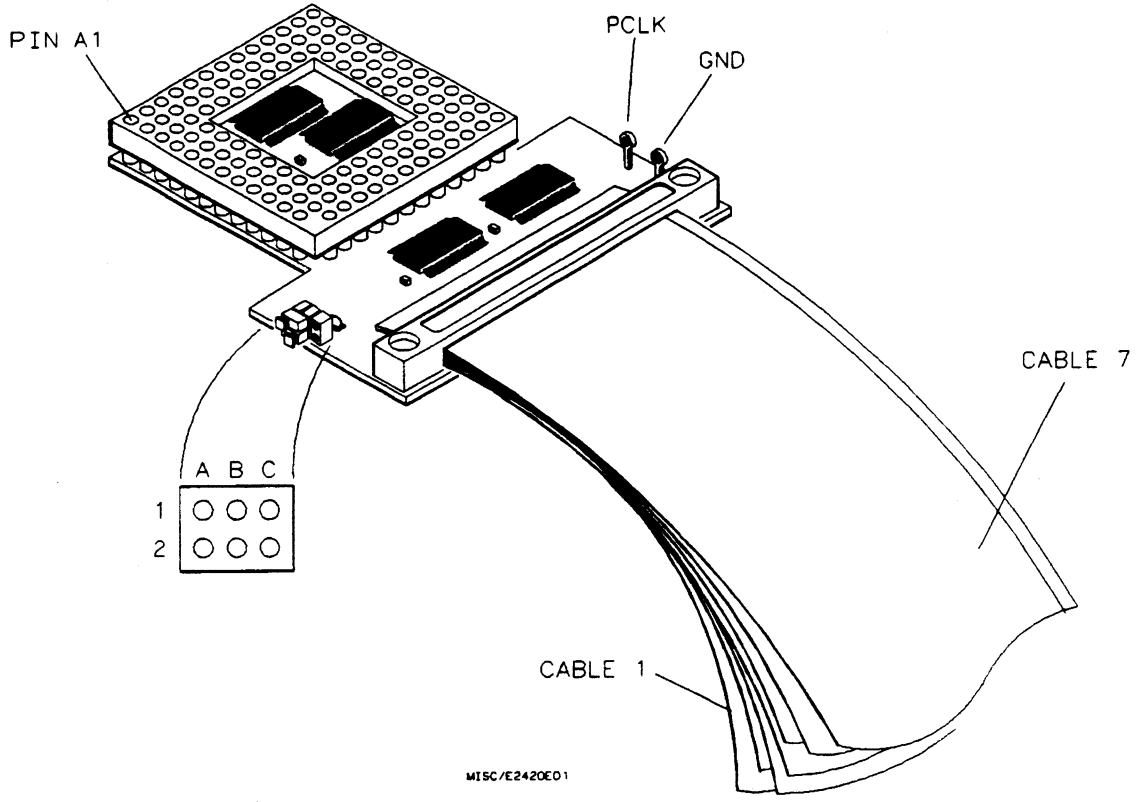


Figure 1-3. Preprocessor Interface Assembly

Note PCLK and GND test points are available on the HP E2420A Preprocessor Interface for the user's convenience.

Connecting to the Analyzer

Connect the logic analyzer probes to the termination modules on the cable connectors of the preprocessor interface board as shown in table 1-1. Figure 1-4 shows the logic analyzer card locations.

Table 1-1. Connections and Configuration Files

Logic Analyzer	Files	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A, HP 1650B, HP 16510A, HP 16510B, and HP 1652B	C68040	P5 (STAT)	P4 (DATA)	P3 (DATA)	P2 (ADDR)	P1 (ADDR)
HP 16511B Master (Upper Card)	D68040	--	P4 (DATA)	P3 (DATA)	P2 (ADDR)	P1 (ADDR)
HP 16511B Expander (Lower Card)		--	--	P7 (STAT C)	P6 (STAT B)	P5 (STAT)
HP 16540A,D Master Card	E68040	--	--	--	--	P5 (STAT)
HP 16541A,D Expander Card 1 *		--	--	P6 (STAT B)	P2 (ADDR)	P1 (ADDR)
HP 16541A,D Expander Card 2 *		--	--	P7 (STAT C)	P4 (DATA)	P3 (DATA)
HP 16550A Master **	F68040	P5 (STAT)	P4 (DATA)	P3 (DATA)	P2 (ADDR)	P1 (ADDR)
HP 16550A Exp. ** (optional)		--	--		P7 (STAT C)	P6 (STAT B)
HP 16550A Master** (8 k acquisition depth)	F68040D	P3 (DATA)		P2 (ADDR)		P1 (ADDR)
HP 16550A Exp.** (8 k acquisition depth)		P6 or P7 (optional)		P5 (STAT)		P4 (DATA)

* For the HP 16541A,D Expander Cards, Exp. Card 1 refers to the physically highest HP16541A,D card, and Exp. Card 2 refers to the next physically highest HP 16541A,D card (see figure 1-4).

** For the HP 16550A cards, the Expander Card is the higher card and the Master Card is the lower card.

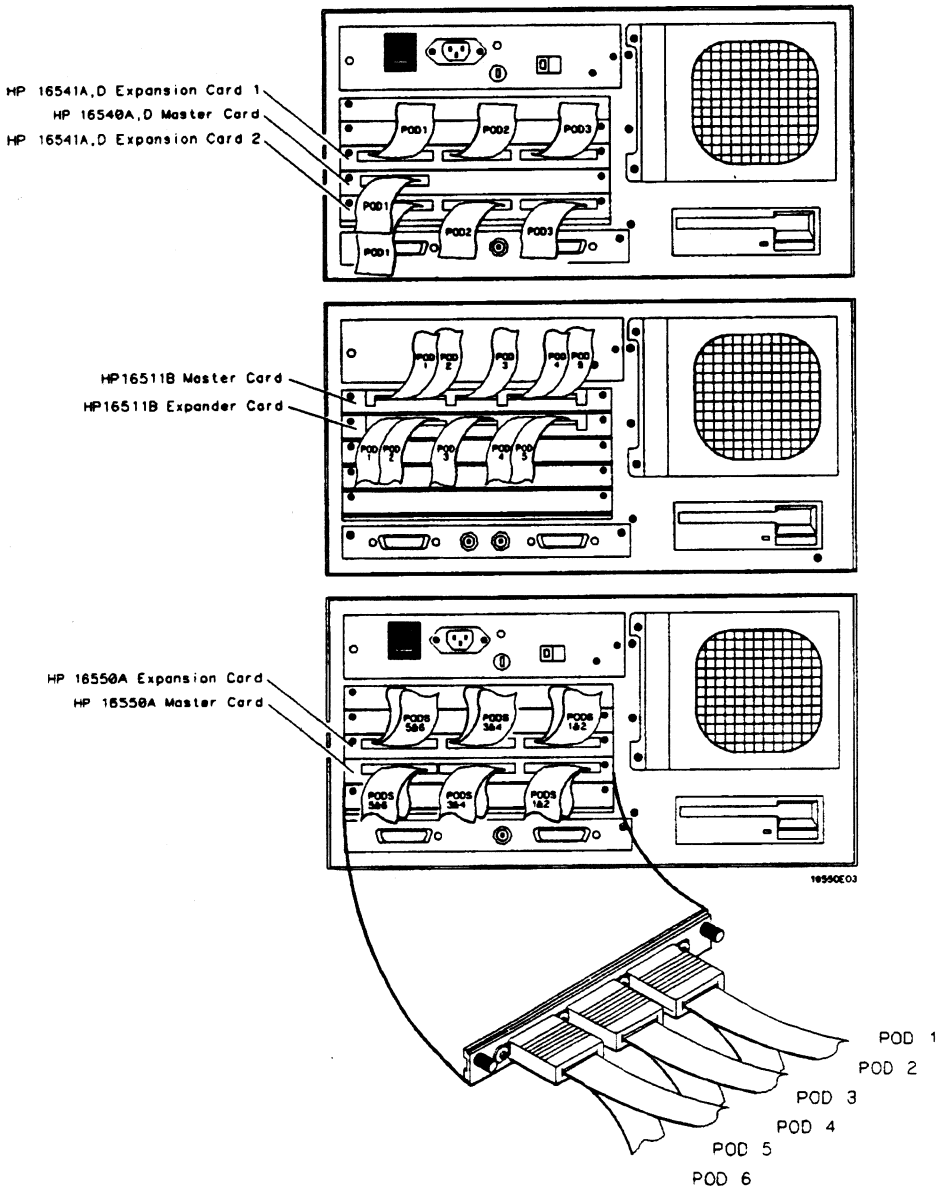


Figure 1-4. Logic Analyzer Card Locations (relative locations, actual slots used may vary)

Selecting an Inverse Assembler

The HP E2420A software contains four inverse assembler files. For the HP 1650A Logic Analyzer without the 10449A upgrade, or for HP 16500A Logic Analyzers with software version V03.01 or older, only the Small inverse assembler can be used. For the other supported logic analyzers any of the four inverse assemblers can be used. Each of these inverse assemblers are described in the following paragraphs.

I68040B - Burst Support

The I68040B inverse assembler should be used whenever the 68040 is operating with burst (line) accesses to instruction memory. During burst transfers, the 68040 holds the address lines constant, and the memory system internally increments address bits A3 and A2. The I68040B inverse assembler mimics this behavior, and displays the least significant hexadecimal digit of the instruction's memory address at the left-hand edge of the disassembled listing.

I68040G - Generic Disassembly

The I68040G inverse assembler may be used whenever the 68040 is not using burst accesses to instruction memory. The performance of this inverse assembler is faster than the I68040D inverse assembler.

I68040D - Dequeuing Disassembly

The I68040D inverse assembler can detect, in a number of circumstances, unused prefetches (instructions which were prefetched to keep the 68040's pipeline active, but were not executed). In order to get accurate results from this inverse assembler, you must take the following steps:

- Disable the 68040 instruction cache.
- Do not use storage qualification to filter out any program fetches.
- Configure the 68040 MMU so that the logical addresses used on the microprocessor correspond to the physical addresses used off the microprocessor. This means that the 68040 MMU is not performing any address translation.

On the I68040D inverse assembler, the prefix "–" is used to indicate that an instruction is not used. For example, the instruction following an RTS Instruction would not be executed, so it will be prefixed with "–" on the logic analyzer listing.

The prefix "~" (conditionally not used) indicates instructions that are not used following a conditional branch instruction.

The prefix "?" indicates that the record of bus activity is ambiguous and that the instruction may or may not have been executed.

For more information on these prefixes, see the section "Prefix Marking" in chapter 2.

I68040S - Small Disassembler

The I68040S inverse assembler does not decode most of the 68040 floating point instructions. This is the only inverse assembler that will run on an HP 1650A Logic Analyzer without the 10449A upgrade, or an HP 16500A mainframe using version V03.01 or older instrument software.

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for 68040 analysis by loading the 68040 configuration file. Loading this file does not automatically load the inverse assembler file. To load the configuration and inverse assembler:

1. Install the HP E2420A flexible disk in the front disk drive of the logic analyzer.
2. Select one of the following menus:
   - For the HP 1650 series logic analyzers, select the I/O Disk Operations menu;
   - For the HP 16500 series logic analyzers, select the System Front Disk menu.

3. Configure the menu to "Load" the one of the following configuration files:
   - For the HP 1650A, HP 1650B, HP 1652B, HP 16510A, and HP 16510B, load the configuration file C68040.
   - For the HP 16511B, load the configuration file D68040.
   - For the HP 16540/16541A,D, load the configuration file E68040.
   - For the HP 16550A (one or two cards, 4 k acquisition memory depth), load the configuration file F68040.
   - For the HP 16550A (two cards, 8 k acquisition memory depth), load the configuration file F68040D.
4. For HP 16500 series logic analyzers, select the configuration file with the knob, then touch "All" and select the correct module.
5. Execute the load operation to load the configuration file into the logic analyzer.
6. Configure the menu to "Load" one of the inverse assemblers (see the section "Selecting an Inverse Assembler" in this chapter).
7. For HP 16500 series logic analyzers, select the inverse assembler file with the knob, then touch "All" and select the correct module.
8. Execute the load operation to load the inverse assembler file into the logic analyzer.

Selecting the "Invasm" Field

Use the following steps to select the "Invasm" field for inverse assembly:

1. Select the Listing menu of the logic analyzer.
2. Select the "Base" field under the "DATA" label.
3. When the pop-up appears, select "Invasm."

Storing the Configuration File

At this point, if you store the configuration to the disk, the stored configuration will include the name of the inverse assembler you selected in step 6. When you subsequently load this configuration, it will automatically load the inverse assembler, as long as it is still present on the disk.

2

Analyzing the Motorola 68040

Introduction

This chapter provides reference information on the format specification and symbols configured by the HP E2420A software. It also provides information about the inverse assembler and status encoding.

Format Specification

When you use the HP E2420A Preprocessor Interface, the format specification set up by the software will be similar to figures 2-1 and 2-2. There may be some slight differences in the displays depending on which logic analyzer you are using. For example, some logic analyzers do not have a Clock Period field. Refer to your logic analyzer manual for more specific information on which fields and displays are available.

Table 3-2 in chapter 3 lists the 68040 signals for the HP E2420A Preprocessor Interface and their corresponding lines to the logic analyzer.

Note

For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field in figures 2-1 and 2-2 should remain in the current selection (< 60 ns) for proper HP E2420A operation. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

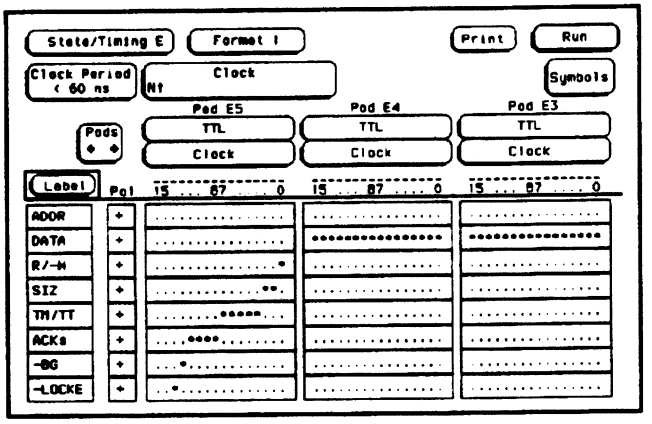


Figure 2-1. Format Specification (Pods 3 - 5)

Note In figures 2-1 and 2-2, additional labels are listed off screen. To view these signals on your logic analyzer, select the Label field and rotate the knob on the front panel clockwise.

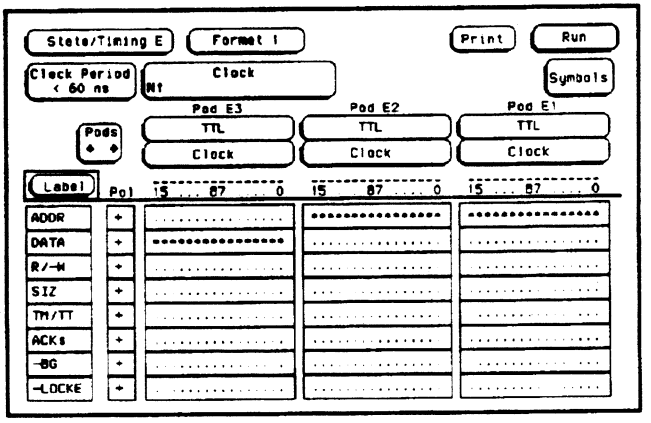


Figure 2-2. Format Specification (Pods 1 - 3)

Listing Menu

Captured data is displayed as shown in figures 2-3 and 2-4. These figures display the state listing for 32-bit bus cycles after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

The logic analyzer always probes the full 32-bit data bus of the 68040. There are some memory systems that occasionally use only 8 or 16 bits for memory transactions. The size of the bus cycle is indicated by the SIZ signals from the microprocessor to the memory. When fewer than the full 32 bits of the data bus are used by a memory cycle, the inverse assembler marks the bits not used by the microprocessor with an "x."

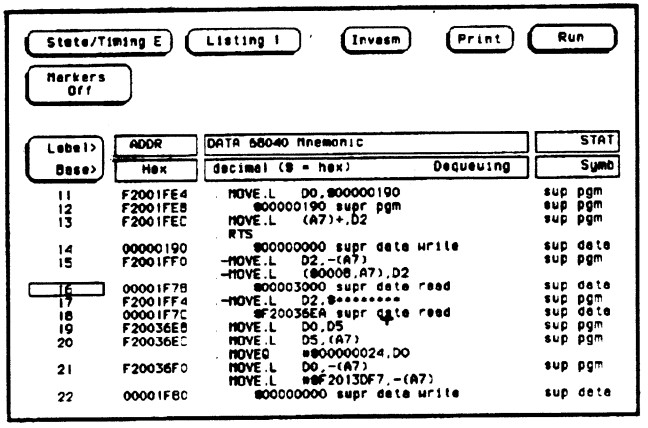


Figure 2-3. State Listing (Non-Burst)

Note

The "#" symbol in the state listing for the HP E2420A refers to an immediate operand.

Burst Data

During burst transfers the microprocessor holds the address constant during the entire burst.

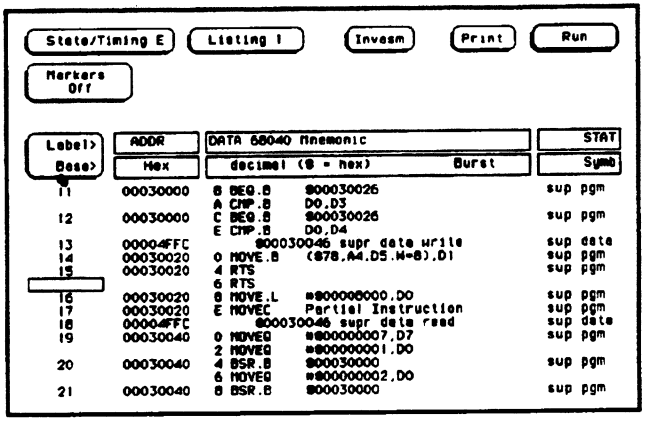


Figure 2-4. State Listing (Burst)

The 68040 Inverse Assembler

The 68040 microprocessor does not provide enough status information for the inverse assembler to pick out the first word of an opcode fetch from a series of program reads. To ensure correct disassembly, you may need to point to the 16-bit word that contains the first word of an opcode fetch. Once synchronized, the inverse assembler will disassemble from this point through the end of the screen. Use the following steps to point to the first word of an opcode fetch:

1. Select a line on the display that contains the first word of an opcode fetch.
2. Roll this line to the top of the display. Note that the cursor location is not the top of the display. In figure 2-4, line 11 is the top of the display.
3. Select the "Invasm" field at the top of the display and a pop-up will appear with the following choices:
   - High
   - Low
4. Select the choice that identifies which word of the 32-bit long word contains the first word of the instruction fetch. The listing will inverse assemble from the top line down. Any data before this display is left unchanged.

Rolling the display up will inverse assemble the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may need to re-synchronize the inverse assembler by repeating steps 1 through 4.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but activity between those blocks will not be inverse assembled.

Note 

The inverse assembler may lose synchronization due to jumps and branches to odd word addresses. When this occurs, re-synchronize the inverse assembler by repeating steps 1 through 4.

On the I68040D inverse assembler, the "Invasm" field also conveys to the disassembler that the selected word is not an unused prefetch.

Interpreting Data

In general, asterisks indicate that the expected operand fetches were not stored in the logic analyzer memory. The pair of asterisks (**) displayed in the operand field of an instruction indicates that a byte of an expected operand was not stored in the logic analyzer memory. Four asterisks (****) indicate that one word of an expected operand was missing, and eight asterisks signify a missing long word. Missing operands (or parts of operands) can result from 68040 instruction prefetch activity, storage qualification, instruction cache operation, or address translation by the MMU.

Examples:

ORI.B	#**,D2	(missing byte operand)
ORI.W	#****,D1	(missing word operand)
ORI.L	#234A****,D3	(missing "lower" word of the operand)
ORI.L	#********,D3	(missing both words of the operand)

The 68040 is capable of supporting byte, word, and long word (32-bit) operands. During operand reads and writes, entire 32-bit values appear on the microprocessor data bus. In the case of single-byte operands, the inverse assembler will display "xx" for the bytes of the input data that are ignored by the microprocessor. In this manner, it is possible to determine exactly which byte of data the microprocessor has used as an operand.

There is a chance that two instructions (16 bits each) will be fetched on one bus cycle. When this happens, the instructions will be displayed on separate lines.

The 68040 microprocessor is a prefetching microprocessor. That is, it will fetch subsequent instruction words while the last opcode is still being executed. When a program executes an instruction that causes a branch, the prefetched words are not used and will be discarded by the microprocessor.

The logic analyzer captures prefetches, even if they are not executed. Therefore, care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Prefetch Marking

The I68040D inverse assembler marks unused 68040 program fetches with the prefix "–" to indicate they were not used. Generally, the unused states were prefetched to keep the pipeline flowing before an instruction was executed that flushed the pipeline. Under some circumstances, the inverse assembler can determine which states are unused prefetches:

- When instruction execution is a subset of the bus activity captured by the logic analyzer; the 68040 program cache should be disabled and the logic analyzer should not be store-qualifying out any program fetches.
- When the logical addresses used on the microprocessor correspond to the physical addresses used off the microprocessor; the 68040 MMU should not be performing any address translation.

There are five categories of instructions which result in prefetch marking:

1. The following instructions flush and refill the pipeline, without upsetting the orderly flow of instruction execution:

move	ea , SR	
movec	Rn , Rc	
fmove	FPcr	(either way)
fmovem		(data or control)

2. The following instructions flush the pipeline and refill it from the target address:

bra	targ
bsr	targ
jmp	< eak >
jsr	< eak >

< eak > is one of the addressing modes where the target is known:

xxxx.W
xxxxxxxx.L
xxxx(PC)

3. The following instructions may be somewhat ambiguous. They may or may not behave like a branch.

bcc	targ
dbcc	targ

The notation "~" (conditionally not used) is used to indicate fetches that are most likely not executed, depending on whether a conditional branch is taken or not. In the following example, without detailed knowledge of the register contents or of the operation and state of the bus interface and instruction pipelines of the 68040, any of the BEQs could be taken:

```
7    0000303C       CMP.B     D0, D1
                    BEQ.B     0000305e
8    00004FFC       00003014  supr data write
9    00003040   ~   CMP.B     D0, D2
                ~   BEQ.B     0000305E
10   00003044   ~   CMP.B     D0, D3
                ~   BEQ.B     0000305E
11   00003048   ~   CMP.B     D0, D4
                ~   BEQ.B     0000305E
12   0000304C   ~   CMP.B     D0, D5
                ~   BEQ.B     0000305E
13   00003058   ~   MOVE.L    #12345678, D0
14   0000305C       RTS
```

The notation "?" is used for ambiguous cases in which the branch target is in its normal place in the instruction sequence:

```
45   00003050        CMP.B     D0, D6
                     BEQ.B     0000305E
46   00003054   ?    CMP.B     D0, D7
                ?    BEQ.B     0000305E
47   00003058   ?    MOVE.L    12345678, D0
48   0000305C        RTS
```

When it appears that a conditional branch target is fetched, but the branch is not taken, the target state is also marked ~:

```
57   00003040        CMP.B     D0, D2
                     BEQ.B     0000305E
58   00003044        CMP.B     D0, D3
                     BEQ.B     0000305E
59   00003048        CMP.B     D0,D4
                     BEQ.B     0000305E
60   0000304C        CMP.B     D0, D5
                     BEQ.B     0000305E
61   00003058   ~    MOVE.L    #12345678, D0
62   00003050        CMP.B     D0, D6
                     BEQ.B     0000305E
```

4. The following instructions flush the pipeline and refill it from a target address that is not known by the inverse assembler:

jsr	<eau>
jmp	<eau>
rtd	#xxxx
rte	
rtr	
stop	#xxxx
rts	
trap	#n

<eau> is any addressing mode other than <eak>.

The rts and trap instructions are similar to jmp <eau>, but the inverse assembler can only determine the branch address if data transactions on the bus are not filtered out by storage qualification.

5. The following instructions may act like a trap instruction:

   trapcc
   trapv

Error Messages

The following list of messages will help you identify operation errors.

Data Error Trace data collected by the logic analyzer cannot be retrieved from memory. This indicates a hardware error or inverse assembler software error.

Illegal Opcode Undefined opcode encountered. Microprocessor action cannot be determined.

Note

Do not modify the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Also note that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

On the HP 16511B, do not modify or turn off the ADDR_B or DATA_B labels. Changes to these labels will disable the inverse assembler.

Symbols

The HP E2420A software sets up Symbol Tables in the format specification with names to identify values from the 68040. The patterns for each symbol listed in table 2-1 are shown in the binary base. In the actual software, these patterns are listed in the hexadecimal base to conserve space. Each of the bits of the STAT label are described in table 2-2. Bit 0 is the least significant bit of the 16-bit field.

Table 2-1. HP E2420A Symbols

Label	Symbol	Pattern
R/-W	rd wr	1 0
SIZ	BYTE WORD LONG LINE	01 10 00 11
TM/TT	Ack Access Alt Access Cache Push MMU Data MMU Pgm User Data User Pgm User Super Data Super Pgm Super Pgm Data	xxx11 xxx10 00000 01100 10000 0010x 01000 0xx0x 1010x 11000 1xx0x xx100 xx00x
ACKs	idle retry wait TA TEA TS TIP	1xxx 0x00 0x11 xxx0 xx0x x0xx 0xxx

Table 2-1. HP E2420A Symbols (Continued)

Label	Symbol	Pattern
DATA_B	h Bxx	0110xxxx xxxxxxxx xxxxxxxx xxxxxxxx
	1 Bxx	xxxxxxxx xxxxxxxx 0110xxxx xxxxxxxx
	h Jxx	01001110 1xxxxxxx xxxxxxxx xxxxxxxx
	1 Jxx	xxxxxxxx xxxxxxxx 01001110 1xxxxxxx
	h RTx	01001110 01110xxx xxxxxxxx xxxxxxxx
	1 RTx	xxxxxxxx xxxxxxxx 01001110 01110xxx
	h BSR	01100001 xxxxxxxx xxxxxxxx xxxxxxxx
	1 BSR	xxxxxxxx xxxxxxxx 01100001 xxxxxxxx
	h BRA	01100000 xxxxxxxx xxxxxxxx xxxxxxxx
	1 BRA	xxxxxxxx xxxxxxxx 01100000 xxxxxxxx
	h JSR	01001110 10xxxxxx xxxxxxxx xxxxxxxx
	1 JSR	xxxxxxxx xxxxxxxx 01001110 10xxxxxx
	h JMP	01001110 11xxxxxx xxxxxxxx xxxxxxxx
	1 JMP	xxxxxxxx xxxxxxxx 01001110 11xxxxxx

Table 2-2. STAT Label Bits

Bit	Status Signals	Description
0	R/W	This signal is high for read cycles and low for write cycles.
1-2	SIZ0-SIZ1	These signals indicate the size of the bus transfer requested by the microprocessor.
3-4	TT0-TT1	These signals encode the transfer type.
5-7	TM0-TM2	These signals are the transfer modifier signals which encode supervisor/user state, code/data access, and cache/MMU access.
8	TA	Transfer Acknowledge (TA) is low whenever the memory system has responded to a transfer.
9	TEA	Transfer Error Acknowledge (TEA) is set low to indicate the memory system failed to respond to a transfer.
10	TS	Transfer Start (TS) is brought low for the first clock cycle of a transfer.
11	TIP	Transfer in Process (TIP) is set low to indicate a transfer is in process.

Table 2-2. STAT Label Bits (Continued)

Bit	Status Signals	Description
12	BG	This signal is set low to indicate the 68040 has been granted bus mastership.
13	LOCKE	This signal is brought low during the last transfer of a locked sequence of transfers.
14	IPEND	The 68040 brings this signal low when it has recognized an interrupt pending.
15	ACQUAL	This signal is generated on the preprocessor interface, and is set high to indicate that the logic analyzer should store the current state of the 68040 pins.

Timing Analysis

In most cases, the format specification loaded for state analysis may also be used for timing analysis. To configure the logic analyzer for timing analysis:

1. Load the appropriate state configuration from the disk.
2. Select the Configuration menu of the logic analyzer.
3. Select the Type field for the 68040 analyzer and select Timing (see figure 2-5).

For more information, refer to the reference manual for your logic analyzer.

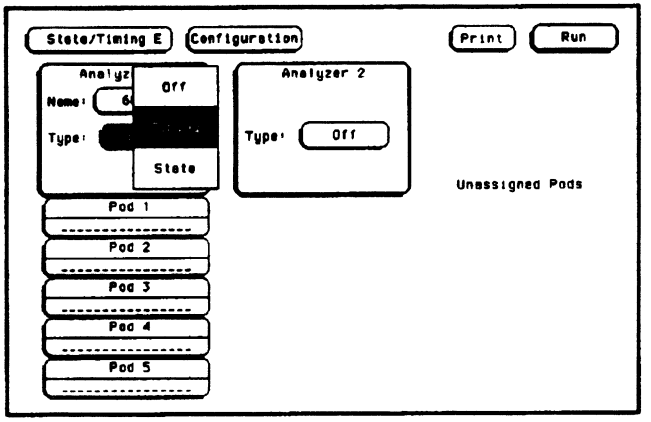


Figure 2-5. Setting Machine 1 to Timing

3

General Information

Introduction

This chapter contains additional reference information including the characteristics and signal mapping for the HP E2420A Preprocessor Interface.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2420A Preprocessor Interface. These characteristics are included as additional information for the user.

Microprocessor Compatibility: Motorola MC68040 and all microprocessors made by other manufacturers that comply with Motorola MC68040 specifications.

Microprocessor Package: 179-pin PGA.

Accessories Required: None.

Maximum Clock Speed: 50 MHz Clock Input using the HP 16540/16541A,D or HP 16550A.
35 MHz Clock Input using the HP 16510B, HP 16511B, HP 1650B, or HP 1652B.
25 MHz Clock Input using the HP 16510A or HP 1650A.

Signal Line Loading: One ACT load on all signals except TS, TIP, TA, and TEA.

Two ACT loads on TS, TIP, TA, and TEA.

Power Requirements: 300 mA at +5 Vdc maximum from the logic analyzer.

Logic Analyzer Required: HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, HP 16511B, HP 16550A, or HP 16540/16541A,D.

Number of Probes Used: Up to seven 16-channel probes.

Microprocessor Operations Displayed:	Burst Transfer User Data Read/Write User Program Read Supervisor Read/Write Supervisor Program Read Bus Grant CPU Space Accesses including: Breakpoint Acknowledge Interrupt Acknowledge	
Additional Capabilities:	The logic analyzer captures all bus cycles.	
Environmental Temperature:	Operating:	0 to +55 °C (+32 to +131 °F)
	Nonoperating:	-40 to +75 °C (-40 to +167 °F)
Altitude:	Operating:	4,600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)
Humidity:	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Target Signal Timing

All of the supported logic analyzers except the HP 16540/16541A,D and HP 16550A require a 10 ns setup time and 0 ns hold time relative to BCLK. The HP 16540/16541A,D and HP 16550A require a 4 ns setup time and 0 ns hold time relative to BCLK.

The buffers on the HP E2420A Preprocessor Interface will typically introduce less than 1 ns of skew between signals. Therefore, an 11 ns setup time (5 ns for the HP 16540/16541A,D and HP 16550A) and 1 ns hold time should be present at the preprocessor interface. Generally, this is compatible with the electrical specifications published for the 25 MHz 68040. The exceptions are:

- Data-In Valid to BCLK, which is specified as 5 ns setup and 4 ns hold time.
- Data-In Valid to DLE, which is specified at 2 ns setup and 8 ns hold time.
- Several of the control signals that are driven by alternate masters when the 68040 has granted the bus and is checking cache hits.

To determine whether or not your state analyzer will take valid samples, compare the 11 ns setup time (5 ns for the HP 16550A and HP 16540/16541A,D) and 1 ns hold time required by the preprocessor interface with setup and hold time available on your target system.

Clocking

Normally, the system BCLK is used to clock the logic analyzer. By configuring jumpers on the preprocessor interface, the DLE can also be configured to clock the logic analyzer. For specific jumper connections, refer to section "Setting the Jumpers" in chapter 1.

Interface Description

The primary function of a preprocessor interface is to connect the target microprocessor to the logic analyzer, and to perform any functions unique to that particular microprocessor. The HP E2420A Preprocessor Interface performs this primary function in the following ways:

- The address, status, and data bus of the 68040 microprocessor are buffered to control loading on the 68040 signal lines.
- The clock qualifier signal for the HP 16540A/16541A logic analyzer is generated from the appropriate 68040 microprocessor signals and bus conditions.

Table 3-1 lists the jumper connections for the HP E2420A Preprocessor Interface. Figure 3-1 shows the jumper connections for each mode of operation, and figure 3-2 shows the block diagram of the HP E2420A Preprocessor Interface.

Table 3-1. HP E2420A Jumper Pin Description

Jumper Pin	Description
A1	BCLK from the buffer on preprocessor interface.
B1	Analyzer clock to cables 1 and 5.
C1	DLE from the buffer on the preprocessor interface.
A2	Normal qualifier from the PAL on the preprocessor interface = -TIP and (-TA or -TEA) and not -TS.
B2	Analyzer qualifier to cable 5, bit 15 and to cable 5 auxiliary clock.
C2	MUX qualifier from the PAL on the preprocessor interface = -TIP and (-TA or -TEA or -TS).

Note

The minus sign "–" before the symbols in the equations in table 3-1 means that the signal is asserted low. For example, –TA means that TA is asserted low.

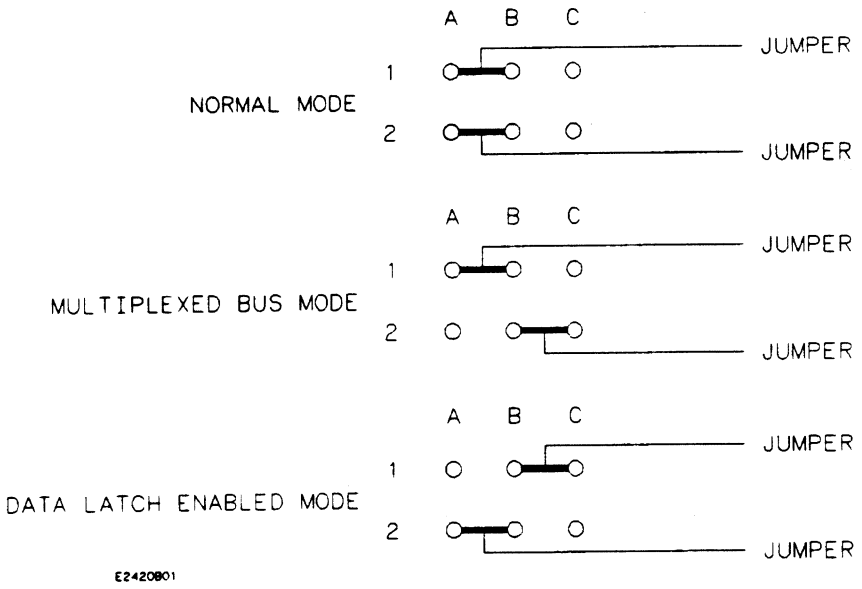


Figure 3-1. Jumper Connections

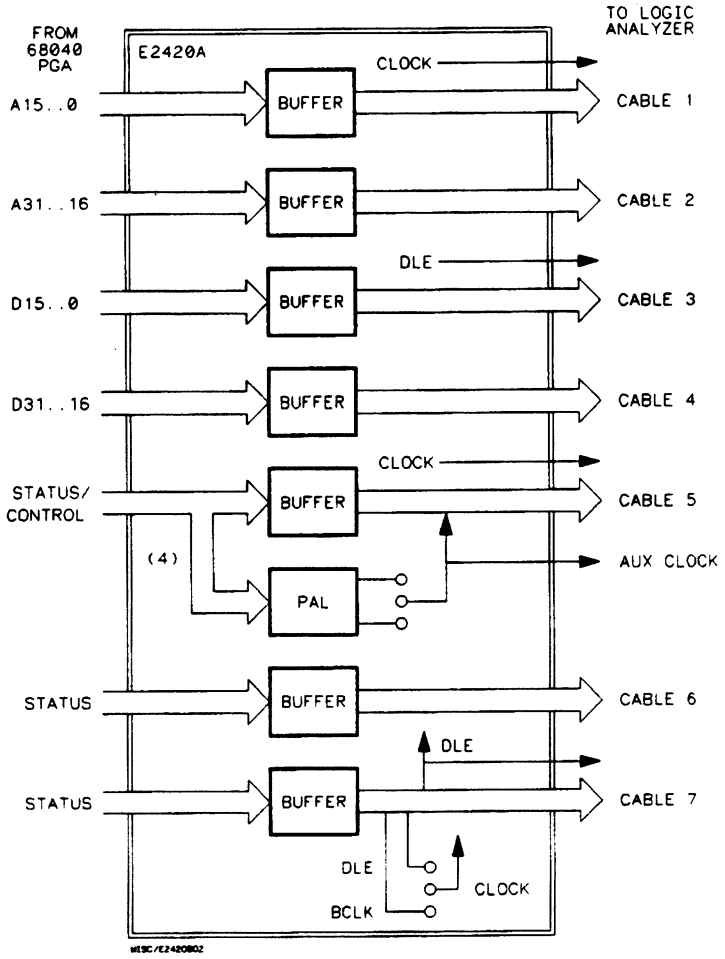


Figure 3-2. HP E2420A Block Diagram

68040 Signal to HP E2420A Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2420A Preprocessor Interface. The numbers in parenthesis refer you to notes that are listed directly after table 3-2 on page 3-15.

Note

The interconnections implemented with the HP E2420A are not direct interconnections. The HP E2420A Preprocessor Interface places digital circuitry between the microprocessor pins and the logic analyzer input.

Table 3-2. 68040 Signal List

68040 Pin	68040 Mnemonic	HP E2420A Cable	HP E2420A Pin	Logic Analyzer Bit	Label
L18	A0	1	37	0	ADDR
K18	A1	1	35	1	ADDR
J17	A2	1	33	2	ADDR
J18	A3	1	31	3	ADDR
H18	A4	1	29	4	ADDR
G18	A5	1	27	5	ADDR
G16	A6	1	25	6	ADDR
F18	A7	1	23	7	ADDR
E18	A8	1	21	8	ADDR
F16	A9	1	19	9	ADDR
P1	A10	1	17	10	ADDR
N3	A11	1	15	11	ADDR
N1	A12	1	13	12	ADDR
M1	A13	1	11	13	ADDR
L1	A14	1	9	14	ADDR
K1	A15	1	7	15	ADDR
R7	BCLK (1)	1	3	Clock (2)	

Table 3-2. 68040 Signal List (Continued)

68040 Pin	68040 Mnemonic	HP E2420A Cable	HP E2420A Pin	Logic Analyzer Bit	Label
K2	A16	2	37	0	ADDR
J1	A17	2	35	1	ADDR
H1	A18	2	33	2	ADDR
J2	A19	2	31	3	ADDR
G1	A20	2	29	4	ADDR
F1	A21	2	27	5	ADDR
E1	A22	2	25	6	ADDR
G3	A23	2	23	7	ADDR
D1	A24	2	21	8	ADDR
F3	A25	2	19	9	ADDR
E2	A26	2	17	10	ADDR
C1	A27	2	15	11	ADDR
E3	A28		13	12	ADDR
B1	A29	2	11	13	ADDR
D3	A30	2	9	14	ADDR
A1	A31	2	7	15	ADDR

Table 3-2. 68040 Signal List (Continued)

68040 Pin	68040 Mnemonic	HP E2420A Cable	HP E2420A Pin	Logic Analyzer Bit	Label
C3	D0	3	37	0	DATA
B3	D1	3	35	1	DATA
C4	D2	3	33	2	DATA
A2	D3	3	31	3	DATA
A3	D4	3	29	4	DATA
A4	D5	3	27	5	DATA
A5	D6	3	25	6	DATA
A6	D7	3	23	7	DATA
B7	D8	3	21	8	DATA
A7	D9	3	19	9	DATA
A8	D10	3	17	10	DATA
A9	D11	3	15	11	DATA
A10	D12	3	13	12	DATA
A11	D13	3	11	13	DATA
A12	D14	3	9	14	DATA
A13	D15	3	7	15	DATA
T9	DLE	3	3	Clock (2)	

Table 3-2. 68040 Signal List (Continued)

68040 Pin	68040 Mnemonic	HP E2420A Cable	HP E2420A Pin	Logic Analyzer Bit	Label
B11	D16	4	37	0	DATA
A14	D17	4	35	1	DATA
B12	D18	4	33	2	DATA
A15	D19	4	31	3	DATA
A16	D20	4	29	4	DATA
A17	D21	4	27	5	DATA
B16	D22	4	25	6	DATA
C15	D23	4	23	7	DATA
A18	D24	4	21	8	DATA
C16	D25	4	19	9	DATA
B18	D26	4	17	10	DATA
D16	D27	4	15	11	DATA
C18	D28	4	13	12	DATA
E16	D29	4	11	13	DATA
E17	D30	4	9	14	DATA
D18	D31	4	7	15	DATA

Table 3-2. 68040 Signal List (Continued)

68040 Pin	68040 Mnemonic	HP E2420A Cable	HP E2420A Pin	Logic Analyzer Bit	Label
N16	R/W	5	37	0	STAT
P17	SIZ0	5	35	1	STAT
P16	SIZ1	5	33	2	STAT
P3	TT0	5	31	3	STAT
P2	TT1	5	29	4	STAT
N18	TM0	5	27	5	STAT
M18	TM1	5	25	6	STAT
K17	TM2	5	23	7	STAT
T14	TA	5	21	8	STAT
S13	TEA	5	19	9	STAT
R16	TS	5	17	10	STAT
R15	TIP	5	15	11	STAT
T13	BG	5	13	12	STAT
R18	LOCKE	5	11	13	STAT
S1	IPEND	5	9	14	STAT
(3)	ACQUAL	5	7	15	STAT
(3)	ACQUAL	5	5	Clock (4)	
R7	BCLK (1)	5	3	Clock (2)	

Table 3-2. 68040 Signal List (Continued)

68040 Pin	68040 Mnemonic	HP E2420A Cable	HP E2420A Pin	Logic Analyzer Bit	Label
Q18	TLN0	6	37	0	STAT_B (5)
P18	TLN1	6	35	1	STAT_B
Q3	UPA0	6	33	2	STAT_B
Q1	UPA1	6	31	3	STAT_B
S18	LOCK	6	29	4	STAT_B
R1	CIOUT	6	27	5	STAT_B
S11	TBI	6	25	6	STAT_B
T10	TCI	6	23	7	STAT_B
T8	IPL0	6	21	8	STAT_B
T7	IPL1	6	19	9	STAT_B
T6	IPL2	6	17	10	STAT_B
T11	AVEC	6	15	11	STAT_B
T15	PST0	6	13	12	STAT_B
S14	PST1	6	11	13	STAT_B
R14	PST2	6	9	14	STAT_B
T16	PST3	6	7	15	STAT_B

Table 3-2. 68040 Signal List (Continued)

68040 Pin	68040 Mnemonic	HP E2420A Cable	HP E2420A Pin	Logic Analyzer Bit	Label
T18	BR	7	37	0	STAT_C (5)
T17	BB	7	35	1	STAT_C
T12	SC0	7	33	2	STAT_C
S12	SC1	7	31	3	STAT_C
Q16	MI	7	29	4	STAT_C
T5	CDIS	7	27	5	STAT_C
S6	MDIS	7	25	6	STAT_C
S7	RSTI	7	23	7	STAT_C
R3	RSTO	7	21	8	STAT_C
S4	TCK	7	19	9	STAT_C
S5	TMS	7	17	10	STAT_C
S3	TDI	7	15	11	STAT_C
T2	TDO	7	13	12	STAT_C
T3	TRST	7	11	13	STAT_C
T9	DLE	7	9	14	STAT_C
R7	BCLK	7	7	15	STAT_C
T9	DLE	7	3	Clock (2)	

Notes for Table 3-2

(1) With jumpers in the normal (state analysis) position. DLE may alternately drive the clocks to cables 1 and 5.

(2) The state analyzer clock is available on cables 1 and 5. The DLE clock is available on cables 3 and 7. This is necessary for clocking the HP 16511B when state information must be clocked to both boards.

(3) ACQUAL is one of two signals generated by a Pal on the preprocessor interface. It is selected by the QUAL jumper. In the normal position,

ACQUAL = -TIP and (-TA or -TEA) and not -TS.

In the multiplex bus mode,

ACQUAL = -TIP and (-TA or -TEA or -TS).

(4) The HP 16540/16541A,D is the only logic analyzer utilizing the second clock qualifier line in the preprocessor interface cable.

(5) Cables 6 and 7 are not available on the 80-channel logic analyzers (HP 1650A, HP 1650B, HP 1652B, HP 16510A, and HP 16510B).

Servicing

The repair strategy for the HP E2420A is board replacement. However, table 3-3 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

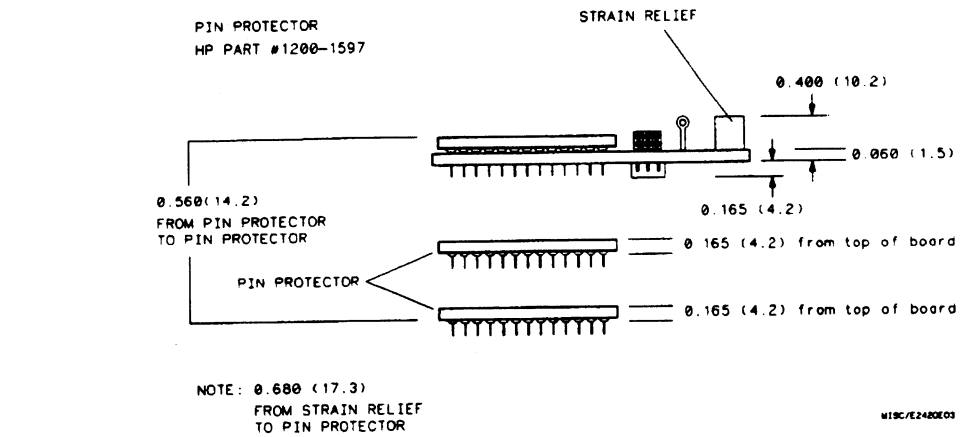
Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Table 3-3. Replaceable Parts

HP Part Number	Description
E2420-66501	Circuit Board Assembly
E2420-69501	Exchange Assembly
E2420-68702	Inverse Assembler Disk Pouch
E2420-44101	ESD Cover
1200-1597	Pin Protector IC Socket (179-pin 68040 footprint)
10449A	Memory upgrade for the HP 1650A Logic Analyzer
01650-63204	100 kOhm Termination Module
1258-0261	Jumper

Dimensions

Figure 3-3 lists the dimensions for the HP E2420A circuit board. The dimensions are listed in inches (millimeters).



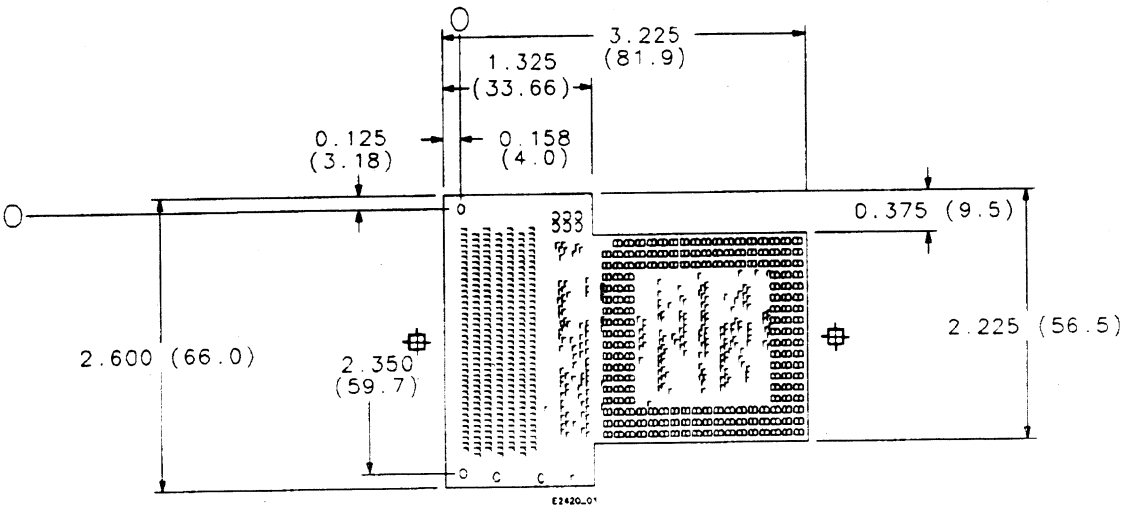


Figure 3-3. HP E2420A Dimensions - inches (mm)

A

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500/16501 frame. Ensure that the cards are firmly seated. If the error message persists, check the clock connections as follows:

HP 16540/16541A,D State:

The HP 16540/16541A,D Master Card is not receiving any clocks.

- Ensure that the target system is On.
- Ensure that connector P5 of the HP E2420A is connected to pod 1 of the Master Card.

HP 16511B State:

Neither of the HP 16511B cards is receiving state clocks.

- Ensure that the pod 1 cable from the master (upper) HP 16511B card is connected to connector P1.
- Ensure that the pod 1 cable from the expander (lower) HP 16511B card is connected to connector P5.

HP 1650A,B, HP 16510A,B, or HP 1652B State:

The logic analyzer is not receiving state clocks.

- Ensure that the pod 1 cable from the logic analyzer is connected to connector P1.
- Ensure that your target system is running properly.
- For HP 1650A and HP 16510A Logic Analyzers, check the preprocessor interface power fuse in the logic analyzer.

Slow Clock

If you have the preprocessor interface hooked up and running and observe a slow clock or no activity from the interface board, the +5 V supply coming from the analyzer may not be getting to the interface board.

To check the +5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the HP E2420A and measure across pins 1 and 2 or pins 39 and 40 (see figure A-1).

- If +5 V isn't observed across these pins, check the internal preprocessor fuse or current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the service manual for your logic analyzer.
- If +5 V is observed across these pins and you feel confident that the +5 V is getting to the preprocessor interface, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

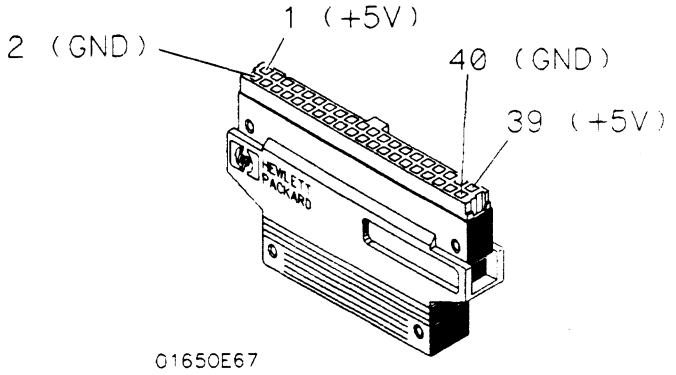


Figure A-1. Pinout of the Logic Analyzer Cable

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500 disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the cursor) and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that all microprocessor caches and memory managers have been disabled. In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the HP 1650A and HP 16510A Logic Analyzers if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. One technique to reduce the capacitive loading is to remove as many pin protectors, extenders, and adapters as possible.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, or with the HP 16540/16541A,D, Logic Analyzer, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates:

- For an HP 16511B Logic Analyzer, only one of the two cards is receiving its state clock. Refer to "Slow or Missing Clock."
- For an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded" (16540/16541A,D)

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D and HP 16541A,D cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.

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