HEWLETT PACKARD

User's Guide

HP E2449B PowerPC 403GA, 601, and 603 Interface Software

User's Guide

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For Safety information, Warranties, and Regulatory information, see the pages behind Appendix A

HP E2449B PowerPC 403GA, 601, and 603 Interface Software

The HP E2449B Interface Software — At a Glance

The HP E2449B Interface Software provides a complete interface for state or timing analysis between an appropriately-designed PowerPC target system and an HP logic analyzer. Table 1 shows the PowerPC microprocessors and logic analyzers supported by the inverse assembler.

Table 1. Logic Analyzer Support for PowerPC Microprocessors

	PowerPC 403GA	PowerPC 601	PowerPC 603
HP 1660A/AS	x	x	x
HP 1661A/AS	x	--	--
HP 16550A (one card)	x	--	--
HP 16550A (two card)	x	x	x
HP 16554A/55A (two or three cards)	x	x	x

The configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the microprocessors. It also loads the inverse assembler for obtaining displays of PowerPC data in PowerPC assembly language mnemonics.

In This Book

This book is the user's guide for the HP E2449B PowerPC Interface Software. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into three chapters and one appendix:

Chapter 1 explains how to install and configure the software for state or timing analysis with the supported logic analyzers.

Chapter 2 provides reference information on the format specification and symbols configured by the software and information about the inverse assemblers and status encoding.

Chapter 3 contains additional reference information including the signal mapping for the HP E2449B PowerPC Interface Software.

Appendix A contains information on troubleshooting problems or difficulties which may occur.

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manual for those products.

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1

Setting Up the PowerPC Interface Software

Setting Up the PowerPC Interface Software

This chapter explains how to install and configure the HP E2449B PowerPC Interface Software for state or timing analysis with the supported logic analyzers.

This section lists the logic analyzer supported by the HP E2449B, and provides other information about target system design and the inverse assembler.

Equipment Supplied

The HP E2449B Interface Software consists of the following equipment:

- The inverse assembler software and configuration files on a 3.5-inch disk.
- This User's Guide.

Minimum Equipment Required

The minimum hardware for analysis of a 403GA, 601, or 603 target system consists of the following equipment:

- The HP E2449B Interface Software.
- A method for connecting to the logic analyzer (see "Connecting to the Target System").
- One of the logic analyzers listed in the following table:

Table 2. Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16550A (one card) *	102	100 MHz	250 MHz	4 k states
16550A (two card)	204	100 MHz	250 MHz	4 k states
1660A/AS	136	100 MHz	250 MHz	4 k states
1661A/AS*	102	100 MHz	250 MHz	4 k states
16554A (two card)	136	70 MHz	125 MHz	512 k states
16555A (two card)	136	110 MHz	250 MHz	1 M states

* These logic analyzers do not support analysis of PowerPC 601 or 603.

Connecting to the Target System

The method for connecting the logic analyzer to the target system depends on the target system design. Broadly speaking, there are three possible approaches:

- Including logic analyzer connectors in the target system
- Probing the microprocessor with a PQFP (Plastic Quad Flat Pack) adapter; the pins on the PQFP adapter can then be probed with the GP (General Purpose) probes supplied with the logic analyzer
- Probing the target directly with GP probes

The following sections contain information on designing or using these three approaches. The signal-to-connector mapping, showing which signals must go to which logic analyzer connector, are shown in chapter 3.

Designing and using built-in connectors

For the logic analyzer user, the simplest method for connecting to the logic analyzer is to have analyzer-compatible connectors designed into the target. IBM's PowerPC 403GA Evaluation Board, for example, includes eight 2x10 connectors.

The primary concerns when using built-in connectors are the board real estate required by the connectors, ensuring that the logic analyzer is properly terminated, and ensuring that the microprocessor pins connect to the proper logic analyzer probes.

Four connector schemes are available. These schemes are described in detail on the following pages. A brief summary of these schemes is covered in the following table.

Table 3. Summary of Built-in Connectors

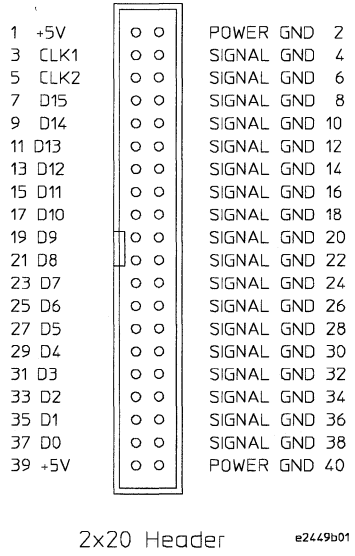
2x20 Connectors	low density requires on-board RC termination plugs directly into logic analyzer cables
2x25 Connectors	medium density (carries two pods) requires on-board RC termination requires special logic analyzer cable
2x10 Connectors	medium density requires termination adapter cable not recommended above 50 MHz
2x14 Connectors	high density requires on-board RC termination requires flexible cable adapter

Most of these schemes require an RC termination network on board for each probed signal. The terminations are available in SIP (single inline package), DIP (double inline package), and SMT (surface mount technology) packages. Additional information is available in HP Application Notes 1244-1 and 5962-8620E. A summary of the part numbers is located on page 1-10.

2x20 Headers

The 2x20 headers are low density connectors. Each connector plugs directly into a standard logic analyzer cable, and carries 16 microprocessor signals and a clock (CLK1). This connection scheme requires on-board RC termination. Figure 1 shows the pinout for a 2x20 header. Refer to chapter 3 for the tables showing the microprocessor signals for each pin. Note that the +5V pins (1 and 39) supply power from the logic analyzer to active devices on an interface board. In most instances, these pins should not be used.

Figure 1



Pinout for 2x20 header

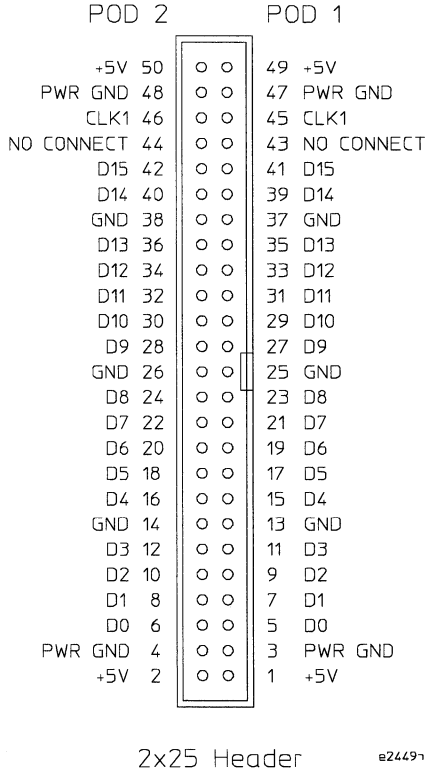
2x25 Headers

The 2x25 headers are medium density connectors. Each connector carries two logic analyzer pods of signals, consisting of 16 microprocessor signals and one clock per logic analyzer pod (CLK1). A special cable is required to connect to the logic analyzer (HP part number 16550-61605). This cable then plugs directly into the 2x25 header.

This connection scheme requires on-board RC termination. Figure 2 shows the pinout for a 2x25 header. Refer to chapter 3 for the tables showing the microprocessor signals for each pin. Note that the +5V pins (1, 2, 49, and 50) are used to supply power from the logic analyzer to any active devices on an interface board. In most instances, these pins should not be used.

For the 2x25 header, pod 2 is more significant than pod 1.

Figure 2



Pinout for 2x25 header

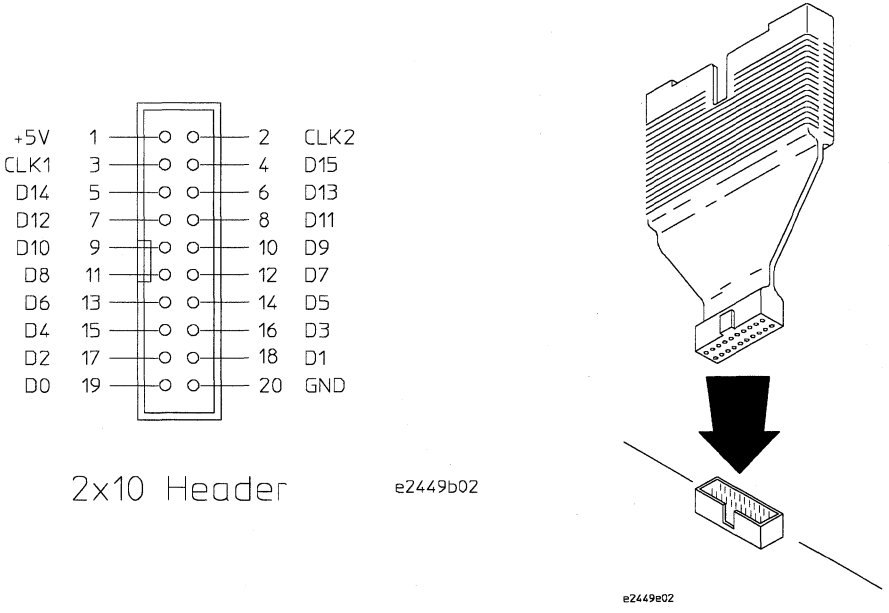
2x10 Headers

The 2x10 headers are medium density connectors. Each connector carries 16 microprocessor signals plus one clock (CLK1). This connection scheme requires one HP 100 kOhm Termination Adapter per connector (HP part number 01650-63203). On-board RC termination is not required.

Figure 3 shows the pinout for a 2x10 header. Refer to chapter 3 for the tables showing the microprocessor signals for each pin. Note that the +5V pin (pin 1) supplies power from the logic analyzer to active devices on an interface board. In most instances, this pin should not be used.

This connection scheme is not recommended for target systems operating above 50 MHz.

Figure 3



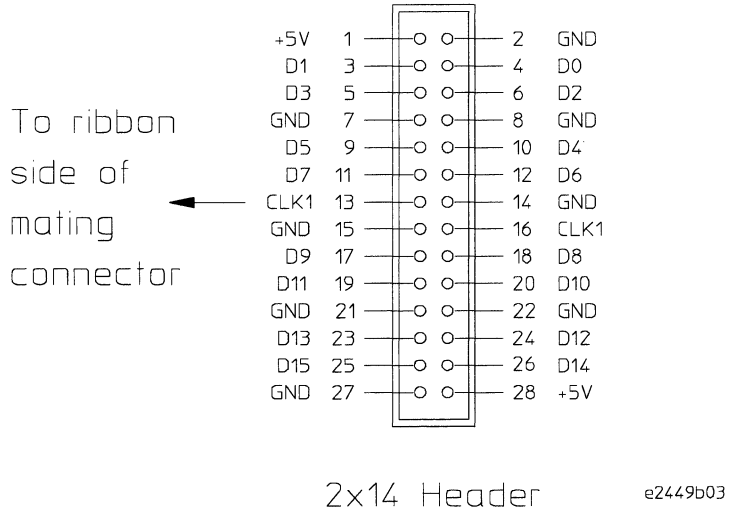
2x10 header pinouts and Termination Adapter

2x14 Headers

The 2x14 headers are high density connectors. Each connector carries 16 microprocessor signals plus one clock (CLK1). The clock signal can be located on pin 13 or 16. A special flexible cable adapter is required to connect the logic analyzer cable to to the connector (HP part number 16550-63201). One adapter is required for each pod.

This connection scheme requires on-board RC termination. Figure 4 shows the pinout for a 2x14 header. Refer to chapter 3 for the tables showing the microprocessor signals for each pin. Note that the +5V pins (1 and 28) are used to supply power from the logic analyzer to any active devices on an interface board. In most instances, these pins should not be used.

Figure 4



2x14 header pinouts

Part Numbers for Built-in Connectors

The following table contains part numbers for the components required for each connection scheme.

Table 4. Part Numbers for Built-in Connectors

	Header Part No.	On-board Termination Required	Adapter to Analyzer Cable
2x20	HP 1251-8828	DIP 1810-1278 (9 per part) SIP 1810-1588 (5 per part)	none
2x25	Fujitsu FCN-214Q050-G/0	DIP 1810-1278 (9 per part) SIP 1810-1588 (5 per part)	16550-61605 (replaces analyzer cable)
2x10	HP 1251-8106	none	01650-63203 Termination Adapter
2x14	HP 1252-6471	SIP 5062-7351 (5 per part) SMT 5062-7396 (6 per part)	16550-63201 flexible cable

Direct Probing with GP Probes

If you are using GP probes, connect the individual probes to the signals according to the tables in chapter 3. It is helpful to label the probe headers before installing the probes. You should connect the ground signal for the analyzer clock(s), and two to four signal grounds per pod.

Probing with a PQFP adapter

The PowerPC 403GA and 603 can be probed using HP PQFP adapters. These adapters require that the chip have 6 millimeters clearance on each side, and no heat sink mounted on top. The adapters use a locator base, permanently installed on the PC board, which precludes subsequent removal of the chip.

The product numbers for the probe adapters, and the part numbers for the locator kits, are as follows:

Table 5. PQFP Probe Adapters

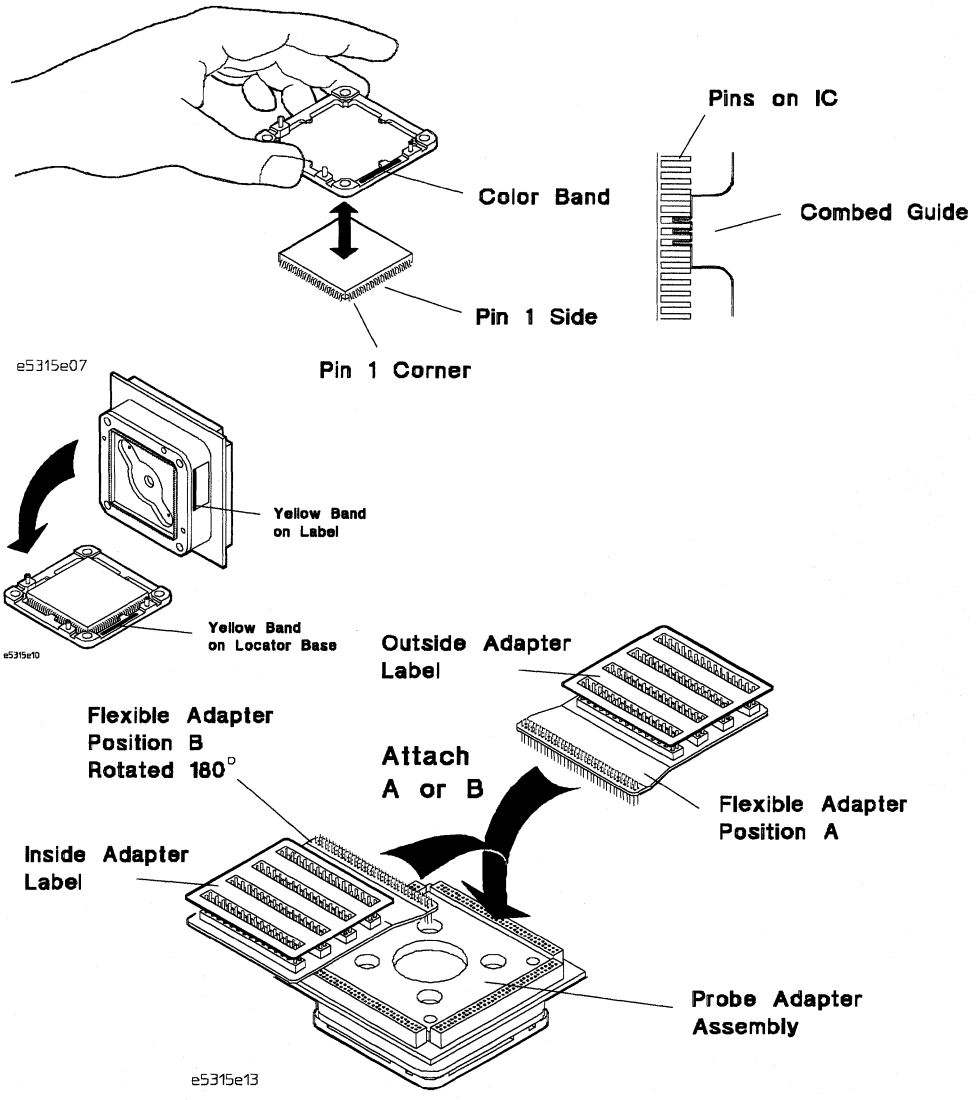
Microprocessor	Package	Probe Adapter	Locator Kit (no inserts)	Locator Kit (with inserts)
PowerPC 603	240-pin PQFP	HP E5315A	5041-9490	5041-9489
PowerPC 403GA	160-pin PQFP	HP E5319A	5042-1707	5042-1706

The locator kit with no inserts is used if the target board has mounting holes laid out to accept a locator base. The locator kit with inserts does not require mounting holes in the PC board.

In addition to a probe adapter and a locator kit, you will need four adapters as targets for the logic analyzer GP probes. These adapters come as Flexible Adapters (HP E5316A), or Rigid Adapters (HP E5330A). The Rigid Adapters require several inches clearance above the target microprocessor.

Additional information on these products is available in the "PQFP Adapter Installation Guide", HP part number E5315-92003. Figure 5 shows a typical mounting sequence using a PQFP adapter.

Figure 5



Connecting a PQFP Probe

Connecting to the Logic Analyzer

The following sections list the connection tables for connecting the logic analyzer pods to the target system connectors or signals. Note that there are different sections for the PowerPC 403GA, 603, and 604. The connection table used also depends on which logic analyzer is used. The configuration file for the specific logic analyzer and microprocessor is listed at the bottom of each table.

Connecting to the PowerPC 403GA

Table 6. Two-card HP 16555A Logic Analyzer Connections for 403GA

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card					J1 ADDR	J2 ADDR	J3 DATA	J4 DATA
Master Card					J5 STAT clk↑	J6 DMA	J7 DRAM	J8 JTAG

Use configuration file **C403M** or **CU403M**

Table 7. Three-card HP 16555A Logic Analyzer Connections for 403GA

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Upper Expander Card					J1 ADDR	J2 ADDR	J3 DATA	J4 DATA
Master Card					J5 STAT clk↑	J6 DMA		
Lower Expander Card							J7 DRAM	J8 JTAG

Use configuration file **C403M3** or **CU403M3**

Table 8. Two-card HP 16550A Logic Analyzer Connections for 403GA

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card			J6 DMA	J8 JTAG	J1 ADDR	J2 ADDR	J3 DATA	J4 DATA
Master Card				J5 STAT clk↑	J7 DRAM			

Use configuration file **C403F2** or **CU403F2**

Table 9. One-card HP 16550A Logic Analyzer and HP 1661A/AS Connections for 403GA

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Master Card/ HP 1661A			J1 ADDR	J2 ADDR	J3 DATA	J4 DATA	J5 STAT clk↑	*

Use configuration file **C403F** or **CU403F**
*This logic analyzer pod can be connected to J6, J7, or J8, depending on the analysis requirements

Table 10. HP 1660A/AS Connections for 403GA

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1660A	J1 ADDR	J2 ADDR	J6 DMA	J8 JTAG	J3 DATA	J4 DATA	J5 STAT clk↑	J7 DRAM
Use configuration file **C403J** or **CU403J**								

Connecting to the PowerPC 601

Table 11. Two-card HP 16555A Logic Analyzer Connections for 601

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card					P6 STAT	P7 STAT	P2 ADDR	P1 ADDR
Master Card					P6 DATA	P5 DATA	P4 DATA_B	P3 DATA_B clk↑
Use configuration file **C601M** or **CP601M**								

Table 12. Three-card HP 16555A Logic Analyzer Connections for 601

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Upper Expander Card					P8 STAT	P7 STAT	P2 ADDR	P1 ADDR
Master Card					P4 DATA_B	P3 DATA_B clk↑		
Lower Expander Card					P10 misc	P9 PARITY	P6 DATA	P5 DATA

Use configuration file **C601M3** or **CP601M3**

Table 13. Two-card HP 16550A Logic Analyzer Connections for 601

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card			P10 misc	P9 PARITY	P8 STAT	P7 STAT	P6 DATA	P5 DATA
Master Card			P4 DATA_B	P3 DATA_B clk↑	P2 ADDR	P1 ADDR		

Use configuration file **C601F** or **CP601F**

Table 14. HP 1660A/AS Logic Analyzer Connections for 601

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1660A	P8 STAT	P7 STAT	P6 DATA	P5 DATA	P4 DATA_B	P3 DATA_B clk↑	P2 ADDR	P1 ADDR

Use configuration file **C601J** or **CP601J**

Connecting to the PowerPC 603

Table 15. Two-card HP 16555A Logic Analyzer Connections for 603

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card					J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B
Master Card					J5 STAT	J2 STAT	J3 ADDR	J4 ADDR clk↑

Use configuration file **C603M** or **CP603M**

Table 16. Three-card HP 16555A Logic Analyzer Connections for 603

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Upper Expander Card					J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B
Master Card					J6 misc	J1 misc	J3 ADDR	J4 ADDR clk↑
Lower Expander Card							J5 STAT	J2 STAT

Use configuration file **C603M3** or **CP603M**

Table 17. Two-card HP 16550A Logic Analyzer Connections for 603

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expander Card			J5 STAT	J2 STAT	J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B
Master Card			J6 misc	J1 misc	J3 ADDR	J4 ADDR clk↑		

Use configuration file **C603F** or **CP603F**

Table 18. HP 1660A/AS Logic Analyzer Connections for 603

	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1660A	J5 STAT	J2 STAT	J9 DATA	J7 DATA	J10 DATA_B	J8 DATA_B	J3 ADDR	J4 ADDR clk↑

Use configuration file **C603J** or **CP603J**

Setting Up the Inverse Assembler Software

Setting up for the inverse assembler software consists of the following major steps:

1. **The first time you set up the inverse assembler, make a duplicate copy of the master disk.**

   For information on duplicating disks, refer to the reference manual for your logic analyzer.

2. **Insert the HP E2449B disk in the front disk drive of the logic analyzer.**

3. **Load the appropriate configuration file into the logic analyzer.**

   Once you have the hardware and software set up, you are ready to make measurements with the logic analyzer and inverse assembler. The rest of this section provides more detailed information on setting up the logic analyzer software.

To load the configuration and inverse assembler files

1 **Insert the HP E2449B disk in the front disk drive of the logic analyzer.**

2 **Depending on your logic analyzer, select one of the following menus:**

- For the HP 1660-series logic analyzers, select the "System Disk" menu
- For the HP 16500A mainframe, select the "System Front Disk" menu
- For the HP 16500B mainframe, select the "System Flexible Disk" menu

3 **Configure the menu to "Load" the analyzer configuration from disk.**

4 **Select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.**

5 **Use the knob to select the appropriate configuration file.**

Your configuration file choice depends on which analyzer you are using and the type of measurements you want to make. See the next section.

6 **Execute the load operation to load the file into the logic analyzer.**

The logic analyzer is configured for PowerPC analysis by loading the appropriate PowerPC configuration file. Loading this file also automatically loads the correct inverse assembler. The configuration file names are located at the bottom of the table showing the connections for your particular microprocessor and logic analyzer. The next section describes the differences between the configuration files.

To select the proper configuration file

There are two configuration files for each analyzer for each microprocessor.

For the PowerPC 601 and 603, there is one configuration file for AACK-before-TA (pipelined) systems, and one configuration file for AACK-delayed-until-last-TA (non-pipelined) systems. The only difference in the configuration files is the inverse assembler attached: one looks backwards from TA for AACK, the other looks forward.

For the PowerPC 403GA, there is one configuration file for systems that have IOTV (input/output transaction valid) enabled, and one for systems that have IOTV disabled. IOTV is used as a storage qualification term; in its absence, the logic analyzer uses state-per-clock capture, and the amount of information captured by the logic analyzer is reduced. The procedure for enabling IOTV is located on page 2-14.

Table 19 summarizes the configuration files:

Table 19. Configuration Files

analyzer	403 IOTV	403 st/clk	601 piped	601 non-pipe	603 piped	603 non-piped
2-card 16554/5/6	C403M	CU403M	CP601M	C601M	CP603M	C603M
3-card 16554/5/6	C403M3	CU403M3	CP601M3	C601M3	CP603M3	C603M3
2-card 16550	C403F2	CU403F2	CP601F	C601F	CP603F	C603F
1-card 16550	C403F	CU403F	--	--	--	--
1660	C403J	CU403J	CP601J	C601J	CP603J	C603J
1661	C403F	CU403F	--	--	--	--

To set up the analyzer for timing

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1 Select the Configuration menu of the logic analyzer.

2 Select the Type field for the analyzer and select Timing.

2

Analyzing the PowerPC

Analyzing the PowerPC

This chapter describes how to display configuration information, gives status information label and symbol encodings, and provides information about the available inverse assemblers.

Displaying Information

This section describes how to display analyzer configuration information, state and timing data captured by the preprocessor interface, and symbol information that has been set up by the preprocessor interface configuration software.

To display the format specification

- **Select the format specification menu for your logic analyzer.**

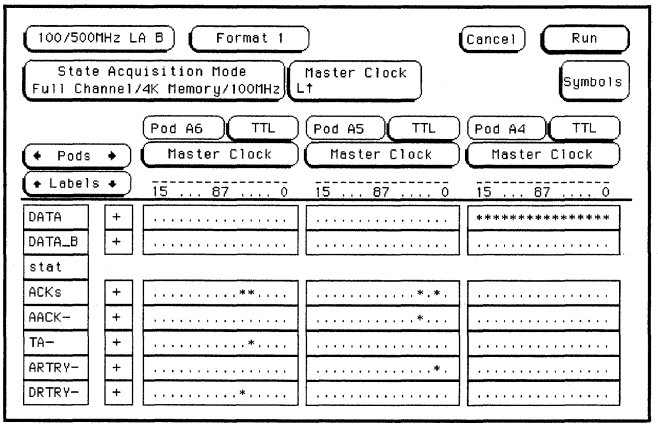
  The PowerPC configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microprocessor.

  Chapter 3 of this guide contains a table that lists the signals for the PowerPC microprocessors and on which pod and probe line the signal comes to the logic analyzer. Refer to this table and to the logic analyzer connection information for your analyzer in chapter 1 to determine where the microprocessor signals should be on the format specification screen.

Example

The format specification display shown in the following figure is from the PowerPC 603 HP 16550A logic analyzer configuration. Additional labels and pod assignments are listed off the screen. Select the "Labels" field and rotate the knob on the analyzer front panel to view additional signals. Select the "Pods" field and rotate the knob to view other pod-bit assignments. There may be some slight differences in the display shown by your particular analyzer.

Figure 3



Format Listing

To display the symbols

- **Select the "Symbols" field on the format specification menu and then choose a label name from the "Label" pop-up. The logic analyzer will display the symbols associated with the label.**

  The HP E2449B configuration software sets up symbol tables on the logic analyzers. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific PowerPC cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu.

  The following tables describe the PowerPC status signals and list the label and symbol encodings defined by the logic analyzer configuration software. There are separate tables for the 403GA, 601, and 603.

Table 20. PowerPC 403GA STAT Label Bits

Pod J1 STAT Bits (21 - 16)								
STAT Bit			21	20	19	18	17	16
Signal			BootW	BusErr	Error	Reset	WBE0	WBE1
Pod J5 STAT Bits (15 - 8)								
STAT Bit	15	14	13	12	11	10	9	8
Signal	INT0	INT1	INT2	INT3	INT4	CINT	WBE2	WBE3
Pod J5 STAT Bits (7 - 0)								
STAT Bit	7	6	5	4	3	2	1	0
Signal	R/W-	ES0	ES1	ES2	BTS	DMA-	I/D-	IOTV

Table 21. PowerPC 601 STAT Label Bits

							Pod P2	Pod P1
STAT Bit							Bit 29	Bit 28
Signal							TS	XATS
Pod P8 STAT Bits (27 - 20)								
STAT Bit	27	26	25		23	22		20
Signal	CI	WT	GBL		TC0	TC1		TBST
Pod P8 STAT Bits (19 - 12)								
STAT Bit	19	18	17	16	15	14	13	12
Signal	TT0	TT1	TT2	TT3	TT4	TSIZ0	TSIZ1	TSIZ2
(continued)								

Table 21. PowerPC 601 STAT Label Bits (continued)

Pod P7 STAT Bits (11 - 4)

STAT Bit	11	10	9	8	7	6	5	4
Signal	BR	BG	DBG	DBWO	ABB	DBB	TEA	INT

Pod P7 STAT Bits (3 - 0)

STAT Bit	3	2	1	0				
Signal	AACK	ARTRY	TA	DRTRY				

Table 22. PowerPC 603 STAT Label Bits

Pod J5 STAT Bits (31 - 24)

STAT Bit	31	30	29	28	27	26	25	24
Signal	TSIZ0	TSIZ1	TSIZ2	TBST	TT0	TT1	TT2	TT3

Pod J5 STAT Bits (23 - 16)

STAT Bit	23	22	21	20	19	18	17	16
Signal	SRESET	INT	DRTRY	TA	TEA	XATS	TS	DBB

Pod J2 STAT Bits (15 - 8)

STAT Bit	15	14	13	12	11	10	9	8
Signal	HRESET	CKSTP	CHECKSTOP	BR	TC0	TC1	WT	CI

Pod J2 STAT Bits (7 - 0)

STAT Bit	7	6	5	4	3	2	1	0
Signal	GBL	DBWO	DBG	BG	AACK	QREQ	ARTRY	ABB

Table 23. Symbol Description for PowerPC 403GA

Label	Symbol	403GA Encoding
STAT	pgm	xx xxxx xxxx xxxx 1xxx x111
	rd data	xx xxxx xxxx xxxx 1xxx x101
	wr data	xx xxxx xxxx xxxx 0xxx x111
	data	xx xxxx xxxx xxxx xxxx x111
	IOTV	xx xxxx xxxx xxxx xxxx xxx1
R/-W	rd	1
	wr	0
IOTV	(blank)	0
	valid transfer	1
ERROR	(blank)	0
	error	1
BusErr	bus error	0
	(blank)	1

Table 24. Symbol Description for PowerPC 601 and 603

Label	Symbol	601 Encoding	603 Encoding
ACKs	idle	1111	1111
	ARTRY	x0xx	xxx0
	DRTRY	xxx0	0xxx
	TA AACK	0x0x	x00x
	AACK	0xxx	xx0x
	TA	xx0x	x0xx
R/-W	rd	1	1
	wr	0	0

(continued)

Label	Symbol	601 Encoding	603 Encoding
TSIZ	burst	0xxx	xxx0
	8 byte	1000	0001
	1 byte	1001	0011
	2 byte	1010	0101
	3 byte	1011	0111
	4 byte	1100	1001
	5byte	1101	1011
	6byte	1110	1101
	7byte	1111	1111
TT	Kill Block	0110x	0110
	Wr Graphics	1010x	1010
	Rd Graphics	1110x	1110
	Clean Block	0000x	0000
	Write	0001x	0001
	Wr/Kill	0011x	0011
	Read	0101x	0101
	Rd/Flush	0111x	0111
	Wr/Atomic Flush	1001x	1001
	Read Atomic	1101x	1101
	Rd/Flush Atomic	1111x	1111
	Flush Block	0010x	0010
	DSYNC	0100x	0100
	eieio	1000x	1000
	reserved?	1011x	1011
	TLB Invalidate	1100x	1100

The TSIZ label includes the TBST- signal, which qualifies TSIZ.

Some transfer type (TT) and size (TSIZ) combinations are defined by the PowerPC architecture, but not asserted by the PowerPC 601 or 603 implementations. The symbols for these combinations include a "?".

The only symbol defined for the STAT label is "inst fetch". An instruction fetch is indicated by AACK asserted (address and qualifiers valid), R/-W (TT1) asserted for read, and TC0 asserted.

Trigger Menu

This section describes some PowerPC considerations in triggering the analyzer. The trigger menu determines what will be acquired by the analyzer and when it will be acquired. The HP E2449B software preconfigures a storage qualification term to exclude wait and idle states from the analyzer's memory.

To use the trigger menu for the PowerPC 403GA

The power-up default on the 403GA has the Real-Time Debug Mode(RDM) bits in the Input/Output Control Register (IOCR) cleared, so that Trace Status outputs (TS 0:6) are disabled. In this condition there are no status signals to indicate when the address and data busses are valid.

A state-per-clock configuration file is provided for this case, along with a state-per-clock inverse assembler, which infers valid states from changes in the address bus and Write Byte Enable signals. The following code sequence will configure the RDM bits in the IOCR to Bus Status mode (%01):

```
mfdcr   r10,IOCR
rlwinm  r10,r10,0,29,26          # clear bits 27 28
ori     r10,r10,8                # set bit 28
mtdcr   IOCR,r10
```

In this mode, the lower TS bits are assigned the following functions:

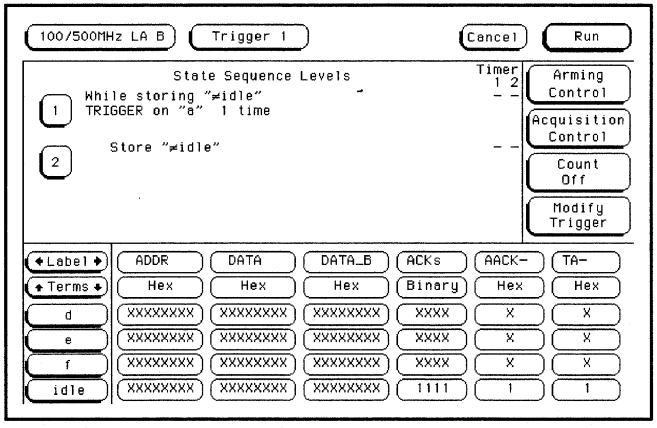
TS 0	IOTV	Input Output Transaction Valid
TS 1	I/-D	Instruction 1, Data 0
TS 2	-DMA	Processor Cycle 1, DMA Cycle 0
TS 3	BTS	Bus Transfer Start

An IOTV-aware configuration and disassembler are provided for this case. The trigger specification uses storage qualification to store only states in which IOTV is asserted.

To use the trigger menu for the PowerPC 601 and 603

The figure below shows the trigger menu for the PowerPC 601 and 603, as configured by the HP 16550A Logic Analyzer. The configuration software renames a pattern term to "idle" and assigns it a pattern with AACK, ARTRY, TA, and DRTRY, all high (de-asserted). The sequencer is programmed to store only states "≠ idle". That is, only states where one or more of these signals is asserted will be stored.

Figure 4



Trigger Menu for PowerPC 601 and 603

To configure the analyzer to store wait and idle states, change the storage qualification from "≠ idle" to "anystate". Doing so will capture all states (state-per-clock).

To accurately trigger on a specific address, enter the address in the ADDR field of a trigger term and also enter 0 in the AACK field of the term. This will ensure against false triggering on a floating address bus.

Since the PowerPC 601 and 603 enjoy an eight byte wide data bus, instruction address will always end in hex 0 or hex 8.

When bursting, the 601 will present a quadword aligned address, which will always end in hex 0. The 603 presents doubleword aligned addresses, which will end in hex 0 or hex 8. A burst consists of four double words, or 32 bytes. To accurately trigger on the fetch of a particular instruction address when bursting, the least significant five bits of the address should be "don't cares". You need to change the base of the ADDR label to binary to enter the five x's.

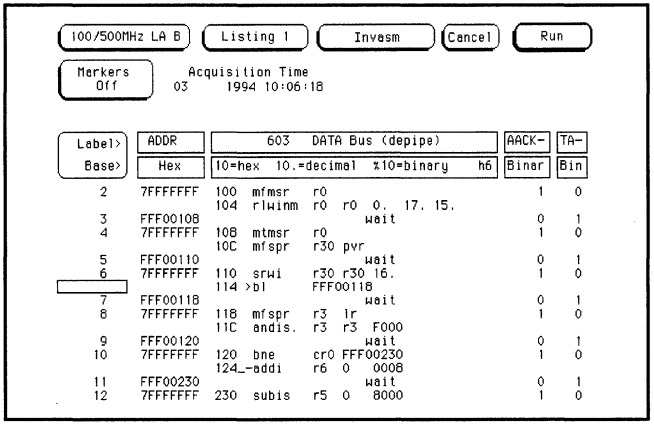
This section discusses the general output format of the inverse assemblers and microprocessor-specific information. Unless noted otherwise, the information covers all three supported microprocessors.

To display captured state data

- **Select the Listing Menu for your logic analyzer.**

  The logic analyzer displays captured data in the Listing Menu. The inverse assembler display is obtained by setting the base for the DATA label to Invasm. Figure 5 shows the Listing Menu as configured on the HP 16550A.

Figure 5



Listing Menu as configured on the HP 16550A

For the PowerPC 601 and 603, the three columns on the left of the inverse assembler display are the least significant hexadecimal digits of an instruction or burst address. These may be useful for matching an execution trace to an assembly listing. Because the PowerPC 60x present one address and then read two or eight instruction for each address, the low-order bits are synthesized by the disassembler. The actual address bits presented by the 60x may be observed under the ADDR label.

Since the 403GA presents an address for each instruction fetched from the bus, this information is not duplicated for the 403GA inverse assembler.

The fourth column may contain an underscore "_", which indicates a break in the sequential flow of instruction addresses.

The fifth column displays overfetch and branch-and-link indicators as described in the overfetch marking section on page 2-14. The remaining disassembly listing resembles an assembly listing.

Interpreting Data

General purpose registers are displayed as r0, r1, r2, ..., r31. Floating point registers are displayed as f0, f1, ..., f31. Condition registers are displayed as cr0, cr1, ..., cr7. Special purpose registers are displayed using their mnemonic.

Most numerical data is displayed in hexadecimal, e.g., "lwz r28 0044(r1)".

Bit numbers and shift counts are displayed in decimal with a dot suffix, e.g., "cror 31. 31. 31.".

A few instructions display their operands in binary with a % prefix, e.g., "mtcrf %001100000 r7".

Note **The inverse assemblers do not support little-endian encoding of data.**

The disassemblers decode the full PowerPC instruction set architecture, including 64-bit mode instructions and optional instructions not implemented on the various microprocessors. When these unimplemented opcodes are encountered, the instruction mnemonic has a "?" prefix. If a reserved bit is set in an instruction opcode field, a "?" is appended to the mnemonic, or in some cases to an operand.

An instruction word of 0000 0000 is decoded as "illegal". Otherwise, if an opcode is not valid, it is shown as "Undefined Opcode".

Branch instruction

If the address of a branch relative instruction is known, its target is presented as an absolute hex address (or as a symbol if it matches an ADDR pattern or range symbol). If the address of a branch relative instruction is not known, its target is displayed as a hexadecimal offset such as +00000C30 or -00000048.

If a branch hint is encoded, a "+" (for predicted taken) or a minus "-" (for predicted not taken) is appended to the conditional branch mnemonic.

Extended mnemonics

PowerPC assemblers support a number of extended mnemonics for some popular assembly language instructions. The HP E2449B disassembler supports the following dialect:

- Conditional traps and branches decode the condition mnemonically when possible. For some conditions which have no conventional mnemonics (for example, "signed less than or unsigned greater than"), the condition field is displayed in binary.
- The L bit is omitted as a compare operand. Instead, compares are decoded as "cmpw" (or "?cmpd").
- "Add immediate" instructions with a negative immediate operand are decoded as subtract immediate ("subi").
- "Subtract from" instructions "subf" and "subfc" are decoded as subtract instructions sub and subc with the source operands exchanged so that "sub r3 r4 r5" is mnemonically interpreted as "r3 = r4 - r5".
- ori r0 r0 0000 is decoded as "nop".

The following listing shows the extended mnemonics for the integer rotate instructions.

Mnemonic	Decoded As	
rlwimi (rotate left word immediate then mask insert)	inslwi	insert from left immediate
	insrwi	insert from right immediate
rlwinm (rotate left word immediate then AND with mask)	rotlwi	rotate left immediate
	rotrwi	rotate right immediate
	slwi	shift left immediate
	srwi	shift right immediate
	extlwi	extract and left justify immediate
	extrwi	extract and right justify immediate
	clrlwi	clear left immediate
	clrrwi	clear right immediate
	clrlslwi	clear left and shift left immediate
rlwnm (rotate left word then AND with mask)	rotlw	rotate left

Overfetch Marking

Overfetch refers to instructions that are are fetched but not executed by the microprocessor. They may arise from the following sources:

- When bursting, the 601 first fetches the critical quadword of an eight-word cache line; the 603 first fetches the critical doubleword; the 403GA fetches the critical word. The memory system then provides succeeding doublewords (single words for the 403GA). If the critical word was not the first quad- or double- or single word of the line, the memory system wraps at the line boundary to the first word. Fetches after the line wrap are not in the sequential execution path and are marked with an asterisk "*".
- When the microprocessors execute a branch instruction, the instructions between the branch and the branch target are not executed. These instructions are indicated with a hyphen "-". If the instruction cache is enabled, the branch target may already be in the cache and will not be fetched over the bus. The remaining cache line containing the branch will be marked as overfetch.

An exception to the above includes branches with the link bit set that record the next instruction address in the link register ("lr"). Frequently, these are subroutine branches which will return to the instructions following the branch. These branch-and-link instructions are indicated by a ">".

For conditional branches whose target addresses are not known or are known but not seen in the bus traffic, the inverse assembler cannot always determine if the branch was taken and will not mark ensuing states as overfetch.

Enabling IOTV (PowerPC 403GA)

To enable IOTV, the 403 microprocessor IOCR (configuration register) can be programmed with bits 27..28 set to b'01', i.e., Bus Status Mode. With supervisor access, the following code will accomplish this:

```
mfdcr    r10,iocr       # device control reg x'a0'
andi.    r11,r10,xFFE7  # clear bits 0..15 27 28
ori      r11,r11,8      # set bit 28
andis.   r12,r10,xFFFF  # copy bits 0..15
or       r12,r12,r11    # join bits 16..31
mtdcr    iocr,r12       # device control reg x'a0'
```

With Bus Status Mode disabled, there are no signals on the 403GA to distinguish an opcode fetch from an operand fetch.

To use the Invasm key

The disassembler may occasionally mispredict a conditional branch instruction as taken and incorrectly mark subsequent states as overfetch. The following steps may be taken to correct this:

- Roll the first incorrectly marked state to the top of the listing screen and select the Invasm key.
- Select High or Low as the first or second word of the double word that is incorrectly marked.

Note that the PowerPC 601 and 603 may branch to the second word of a doubleword without the disassembler detecting it. This could be a branch from cache, or via the lr, ctr, or srr0 registers. If the first word of the target doubleword is a branch, the inverse assembler may incorrectly mark the subsequent word(s) as overfetch.

Disabling the Instruction Cache

When the instruction cache is enabled, many PowerPC instructions may be executed from cache and will not appear on the external bus. To get an execution trace on the bus, the instruction cache can be disabled. This must be done in supervisor mode.

Disabling the Cache (403) The cacheability of areas of 403 memory space is controlled by bits in the Instruction Cache Control Register (ICCR)with a 128 megabyte granularity. For example, to disable the instruction cache for addresses 78000000 through 7FFFFFFF, the following code sequence could be used:

```
mfdcr   r1,ICCR
rlwinm  r1,r1,0,16,14 #   clear bit 15
mtdcr   ICCR,r1       #   disable i cache 78000000..7FFFFFFF
```

Disabling the Cache (601) On the 601, caching is inhibited by setting the I bit in the page table entries and Block Address Translation(BAT) registers. Refer to the 601 documentation for additional information.

Disabling the Cache (603) On the 603, a single bit in Hardware Implementation Dependent register 0 (HID0) globally controls instruction cacheability.

Disable the cache with the following code:

```
mfspr    r3    hid0
rlwinm   r3    r3 0 17 15 #clear bit 16(ICE)
mtspr    hid0  r3
```

- To also disable the data cache use:

```
mfspr    r3    hid0
rlwinm   r3    r3 0 18 15 #clear ICE and DCE
mtspr    hid0  r3
isync
```

- To invalidate and disable the cache use:

```
mfspr    r3    hid0
rlwinm   r3    r3 0 18 15 #clear ICE and DCE
ori      r3    0C00     # set ICFI and DCFI
mtspr    hid0  r3
sync
rlwinm   r3    r3 0 22 19 #clear ICFI and DCFI
mtspr    hid0  r3
isync
```

3

Preprocessor Interface Hardware Reference

Preprocessor Interface Hardware Reference

This chapter contains additional reference information including the signal mapping for the HP E2449B PowerPC Interface Software.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2449B PowerPC Interface Software.

Table 25. Operating Characteristics

Microprocessor Compatibility	PowerPC 403GA, PowerPC 601, and PowerPC 603
Microprocessor Clock Speed	70 MHz for the HP 16554 Logic Analyzer 100 MHz for the HP 16550, HP 16555, HP 1660, and HP 1661 Logic Analyzers
Probes Required	Eight 16-channel probes are required for disassembly of PowerPC 601 and 603. Two additional 16-channel pods are available for the 601 and 603. For the 403GA, five pods are required for disassembly and three additional pods are available.
Signal Line Loading	Typically 100 kOhm plus 10 pf.
Setup/Hold Requirement	Data must be valid for a 3.5 ns window with respect to the logic analyzer clock.

Signal-to-Connector Mapping

The following tables show the electrical signal-to-connector mapping required by the HP E2449B PowerPC Interface Software.

Table 26. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P1

2x20 pin	2x14 pin	2x10 pin	LA bit	403GA pin	signal name	analyzer labels		
3	13	3	clk1	22	SysClk			
7	25	4	15	11	BootW	BootW		STAT
9	26	5	14	12	BusErr	BusErr		STAT
11	23	6	13	136	Error	Error		STAT
13	24	7	12	134	Reset-	Reset-		STAT
15	19	8	11	122	WBE0 A4	WBE0	WBE0:3	STAT
17	20	9	10	123	WBE1 A5	WBE1	WBE0:3	STAT
19	17	10	9	92	A6			ADDR
21	18	11	8	93	A7			ADDR
23	11	12	7	94	A8			ADDR
25	12	13	6	95	A9			ADDR
27	9	14	5	96	A10			ADDR
29	10	15	4	97	A11			ADDR
31	5	16	3	98	A12			ADDR
33	6	17	2	99	A13			ADDR
35	3	18	1	103	A14			ADDR
37	4	19	0	104	A15			ADDR

Table 26. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P2

2x20 pin	2x14 pin	2x10 pin	LA bit	403GA pin	signal name	analyzer label
3	13	3	clk1	13	Ready	
7	25	4	15	105	A16	ADDR
9	26	5	14	106	A17	ADDR
11	23	6	13	107	A18	ADDR
13	24	7	12	108	A19	ADDR
15	19	8	11	109	A20	ADDR
17	20	9	10	110	A21	ADDR
19	17	10	9	112	A22	ADDR
21	18	11	8	113	A23	ADDR
23	11	12	7	114	A24	ADDR
25	12	13	6	115	A25	ADDR
27	9	14	5	116	A26	ADDR
29	10	15	4	117	A27	ADDR
31	5	16	3	118	A28	ADDR
33	6	17	2	119	A29	ADDR
35	3	18	1		gnd	ADDR
37	4	19	0		gnd	ADDR

Table 26. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P3

2x20 pin	2x14 pin	2x10 pin	LA bit	403GA pin	signal name	analyzer label
3	13	3	clk1	134	Reset-	
7	25	4	15	42	D0	DATA
9	26	5	14	43	D1	DATA
11	23	6	13	44	D2	DATA
13	24	7	12	45	D3	DATA
15	19	8	11	46	D4	DATA
17	20	9	10	47	D5	DATA
19	17	10	9	48	D6	DATA
21	18	11	8	51	D7	DATA
23	11	12	7	52	D8	DATA
25	12	13	6	53	D9	DATA
27	9	14	5	54	D10	DATA
29	10	15	4	55	D11	DATA
31	5	16	3	56	D12	DATA
33	6	17	2	57	D13	DATA
35	3	18	1	58	D14	DATA
37	4	19	0	62	D15	DATA

Table 26. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P4

2x20 pin	2x14 pin	2x10 pin	LA bit	403GA pin	signal name	analyzer label
3	13	3	clk1	6	TCK	
7	25	4	15	63	D16	DATA
9	26	5	14	64	D17	DATA
11	23	6	13	65	D18	DATA
13	24	7	12	66	D19	DATA
15	19	8	11	67	D20	DATA
17	20	9	10	68	D21	DATA
19	17	10	9	71	D22	DATA
21	18	11	8	72	D23	DATA
23	11	12	7	73	D24	DATA
25	12	13	6	74	D25	DATA
27	9	14	5	75	D26	DATA
29	10	15	4	76	D27	DATA
31	5	16	3	77	D28	DATA
33	6	17	2	78	D29	DATA
35	3	18	1	79	D30	DATA
37	4	19	0	82	D31	DATA

Table 26. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P5

2x20 pin	2x14 pin	2x10 pin	LA bit	403GA pin	signal name	analyzer labels		
3	13	3	clk1	22	SysCLK			
7	25	4	15	31	INT0	Intr 0	Intrpt	STAT
9	26	5	14	32	INT1	Intr 1	Intrpt	STAT
11	23	6	13	33	INT2	Intr 2	Intrpt	STAT
13	24	7	12	34	INT3	Intr 3	Intrpt	STAT
15	19	8	11	35	INT4	Intr 4	Intrpt	STAT
17	20	9	10	36	CINT	Crit In	Intrpt	STAT
19	17	10	9	124	WBE2 A30	WBE2	WBE0:3	STAT
21	18	11	8	125	WBE3 A31	WBE3	WBE0:3	STAT
23	11	12	7	127	R/W-	R/-W	TS0:6	STAT
25	12	13	6	17	ES0 TS0	ES0:2	TS0:6	STAT
27	9	14	5	18	ES1 TS1	ES0:2	TS0:6	STAT
29	10	15	4	19	ES2 TS2	ES0:2	TS0:6	STAT
31	5	16	3	86	BTS TS3	BTS	TS0:6	STAT
33	6	17	2	85	DMA- TS4	-DMA	TS0:6	STAT
35	3	18	1	84	I/D- TS5	I/D-	TS0:6	STAT
37	4	19	0	83	IOTV TS6	IOTV	TS0:6	STAT

Table 26. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P6

2x20 pin	2x14 pin	2x10 pin	LA bit	403GA pin	signal name	analyzer labels	
3	13	3	clk1	13	Ready		
7	25	4	15	14	HoldReq	Hold	
9	26	5	14	134	Reset-	Reset-	
11	23	6	13	135	BusReq	BusReq	
13	24	7	12	139	MuxSel	AmuxS	
15	19	8	11	2	Req0	-DMAR0	Req0:3
17	20	9	10	3	Req1	-DMAR1	Req0:3
19	17	10	9	4	Req2	-DMAR2	Req0:3
21	18	11	8	5	Req3	-DMAR3	Req0:3
23	11	12	7	156	Ack0	-DMAA0	Ack0:3
25	12	13	6	157	Ack1	-DMAA1	Ack0:3
27	9	14	5	158	Ack2	-DMAA2	Ack0:3
29	10	15	4	159	Ack3	-DMAA3	Ack0:3
31	5	16	3	128	EOT0	-EOT0	EOT0:3
33	6	17	2	131	EOT1	-EOT1	EOT0:3
35	3	18	1	132	EOT2	-EOT2	EOT0:3
37	4	19	0	133	EOT3	-EOT3	EOT0:3

Table 26. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P7

2x20 pin	2x14 pin	2x10 pin	LA bit	403GA pin	signal name	analyzer labels		
3	13	3	clk1	134	Reset-			
7	25	4	15	155	CS0	CS0:7		
9	26	5	14	154	CS1	CS0:7		
11	23	6	13	153	CS2	CS0:7		
13	24	7	12	152	CS3	CS0:7		
15	19	8	11	13	Ready	Ready		
17	20	9	10	126	OE	OE		
19	17	10	9	137	DramOE	DramOE		
21	18	11	8	138	DramWE	DramWE		
23	11	12	7	145	CAS3	CAS3	CAS3:0	
25	12	13	6	144	CAS2	CAS2	CAS3:0	
27	9	14	5	143	CAS1	CAS1	CAS3:0	
29	10	15	4	142	CAS0	CAS0	CAS3:0	
31	5	16	3	151	CS4/RAS3	CS4 RAS3	CAS0:7	RAS3:0
33	6	17	2	148	CS5/RAS2	CS5 RAS3	CAS0:7	RAS3:0
35	3	18	1	147	CS6/RAS1	CS6 RAS3	CAS0:7	RAS3:0
37	4	19	0	146	CS7/RAS0	CS7 RAS3	CAS0:7	RAS3:0

Table 26. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P8

2x20 pin	2x14 pin	2x10 pin	LA bit	403GA pin	signal name	analyzer label
3	13	3	clk1	6	TCK	TCLK
7	25	4	15	7	TMS	TMS
9	26	5	14	8	TDI	TDI
11	23	6	13	16	TDO	TDO
13	24	7	12	9	Halt-	Halt
15	19	8	11	26	SerClk	SerClk
17	20	9	10	27	RecvD	RecvD
19	17	10	9	87	XmitD	XmitD
21	18	11	8	88	DTR/RTS	-DTR -RTS
23	11	12	7	28	DSR/CTS	-DSR -CTS
25	12	13	6	25	Timer	TimClk
27	9	14	5	23	TestA	Test A
29	10	15	4	24	TestB	Test B
31	5	16	3	--	--	
33	6	17	2	--	--	
35	3	18	1	37	FrqR0	FreqR0
37	4	19	0	38	FrqR1	FreqR1

Table 27. PowerPC 601 Logic Analyzer Interface Signal List - Pod P1

2x20 pin	2x14 pin	2x10 pin	LA bit	601 pin	signal name	analyzer labels	
3	13	3	clk1	229	XATS	XATS-	STAT
7	25	4	15	43	A16		ADDR
9	26	5	14	45	A17		ADDR
11	23	6	13	46	A18		ADDR
13	24	7	12	47	A19		ADDR
15	19	8	11	49	A20		ADDR
17	20	9	10	50	A21		ADDR
19	17	10	9	51	A22		ADDR
21	18	11	8	54	A23		ADDR
23	11	12	7	55	A24		ADDR
25	12	13	6	56	A25		ADDR
27	9	14	5	58	A26		ADDR
29	10	15	4	59	A27		ADDR
31	5	16	3	60	A28		ADDR
33	6	17	2	62	A29		ADDR
35	3	18	1	63	A30		ADDR
37	4	19	0	64	A31		ADDR

Table 27. PowerPC 601 Logic Analyzer Interface Signal List - Pod P2

2x20 pin	2x14 pin	2x10 pin	LA bit	601 pin	signal name	analyzer labels
3	13	3	clk1	226	TS	TS-
7	25	4	15	18	A0	ADDR
9	26	5	14	19	A1	ADDR
11	23	6	13	21	A2	ADDR
13	24	7	12	22	A3	ADDR
15	19	8	11	23	A4	ADDR
17	20	9	10	26	A5	ADDR
19	17	10	9	27	A6	ADDR
21	18	11	8	28	A7	ADDR
23	11	12	7	30	A8	ADDR
25	12	13	6	31	A9	ADDR
27	9	14	5	32	A10	ADDR
29	10	15	4	34	A11	ADDR
31	5	16	3	35	A12	ADDR
33	6	17	2	36	A13	ADDR
35	3	18	1	41	A14	ADDR
37	4	19	0	42	A15	ADDR

Table 27. PowerPC 601 Logic Analyzer Interface Signal List - Pod P3

2x20 pin	2x14 pin	2x10 pin	LA bit	601 pin	signal name	analyzer labels
3	13	3	clk1	285	PCLK_EN	PCLKEN
7	25	4	15	151	DL16	DATA_B
9	26	5	14	149	DL15	DATA_B
11	23	6	13	148	DL14	DATA_B
13	24	7	12	147	DL13	DATA_B
15	19	8	11	145	DL12	DATA_B
17	20	9	10	144	DL11	DATA_B
19	17	10	9	143	DL10	DATA_B
21	18	11	8	140	DL9	DATA_B
23	11	12	7	139	DL8	DATA_B
25	12	13	6	138	DL7	DATA_B
27	9	14	5	136	DL6	DATA_B
29	10	15	4	135	DL5	DATA_B
31	5	16	3	134	DL4	DATA_B
33	6	17	2	132	DL3	DATA_B
35	3	18	1	131	DL2	DATA_B
37	4	19	0	130	DL1	DATA_B

Table 27. PowerPC 601 Logic Analyzer Interface Signal List - Pod P4

2x20 pin	2x14 pin	2x10 pin	LA bit	601 pin	signal name	analyzer labels
3	13	3	clk1	271	BCLK_EN	BCLKEN
7	25	4	15	188	DL0	DATA_B
9	26	5	14	185	DL1	DATA_B
11	23	6	13	182	DL2	DATA_B
13	24	7	12	181	DL3	DATA_B
15	19	8	11	180	DL4	DATA_B
17	20	9	10	178	DL5	DATA_B
19	17	10	9	173	DL6	DATA_B
21	18	11	8	172	DL7	DATA_B
23	11	12	7	169	DL8	DATA_B
25	12	13	6	168	DL9	DATA_B
27	9	14	5	167	DL10	DATA_B
29	10	15	4	165	DL11	DATA_B
31	5	16	3	161	DL12	DATA_B
33	6	17	2	159	DL13	DATA_B
35	3	18	1	157	DL14	DATA_B
37	4	19	0	155	DL15	DATA_B

Table 27. PowerPC 601 Logic Analyzer Interface Signal List - Pod P5

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer label
3	13	3	clk1	--	--	
7	25	4	15	99	DH16	DATA
9	26	5	14	98	DH17	DATA
11	23	6	13	97	DH18	DATA
13	24	7	12	95	DH19	DATA
15	19	8	11	94	DH20	DATA
17	20	9	10	93	DH21	DATA
19	17	10	9	91	DH22	DATA
21	18	11	8	90	DH23	DATA
23	11	12	7	86	DH24	DATA
25	12	13	6	85	DH25	DATA
27	9	14	5	84	DH26	DATA
29	10	15	4	83	DH27	DATA
31	5	16	3	82	DH28	DATA
33	6	17	2	81	DH29	DATA
35	3	18	1	80	DH30	DATA
37	4	19	0	75	DH31	DATA

Table 27. PowerPC 601 Logic Analyzer Interface Signal List - Pod P6

2x20 pin	2x14 pin	2x10 pin	LA bit	601 pin	signal name	analyzer label
3	13	3	clk1	--	--	
7	25	4	15	127	DH0	DATA
9	26	5	14	126	DH1	DATA
11	23	6	13	125	DH2	DATA
13	24	7	12	123	DH3	DATA
15	19	8	11	122	DH4	DATA
17	20	9	10	121	DH5	DATA
19	17	10	9	119	DH6	DATA
21	18	11	8	118	DH7	DATA
23	11	12	7	112	DH8	DATA
25	12	13	6	111	DH9	DATA
27	9	14	5	110	DH10	DATA
29	10	15	4	108	DH11	DATA
31	5	16	3	107	DH12	DATA
33	6	17	2	106	DH13	DATA
35	3	18	1	104	DH14	DATA
37	4	19	0	103	DH15	DATA

Table 27. PowerPC 601 Logic Analyzer Interface Signal List - Pod P7

2x20 pin	2x14 pin	2x10 pin	LA bit	601 pin	signal name	analyzer labels		
3	13	3	clk1	--	--			
7	25	4	15	219	BR	BR-		STAT
9	26	5	14	298	BG	BG-		STAT
11	23	6	13	300	DBG	DBG-		STAT
13	24	7	12	297	DBWO	DBWO-		STAT
15	19	8	11	224	ABB	ABB-		STAT
17	20	9	10	220	DBB	DBB-		STAT
19	17	10	9	291	TEA	TEA-		STAT
21	18	11	8	262	INT	INT-		STAT
23	11	12	7	295	AACK	AACK-	AACKs	STAT
25	12	13	6	221	ARTRY	ARTRY-	AACKs	STAT
27	9	14	5	290	TA	TA-	AACKs	STAT
29	10	15	4	292	DRTRY	DRTRY-	AACKs	STAT
31	5	16	3	279	HRESET	HRESET-		
33	6	17	2	264	SRESET	SRESET-		
35	3	18	1	258	CKSTP_IN	CHKIN-		
37	4	19	0	235	SHD	SHD-		

Table 27. PowerPC 601 Logic Analyzer Interface Signal List - Pod P8

2x20 pin	2x14 pin	2x10 pin	LA bit	601 pin	signal name	analyzer label		
3	13	3	clk1	--	--			
7	25	4	15	216	CI	CI-		STAT
9	26	5	14	214	WT	WT-		STAT
11	23	6	13	233	GBL	GBL-		STAT
13	24	7	12		--			STAT
15	19	8	11	243	TC0		TC	STAT
17	20	9	10	251	TC1		TC	STAT
19	17	10	9		--			STAT
21	18	11	8	236	TBST	TBST-	TSIZ	STAT
23	11	12	7	228	TT0	Atomic	TT	STAT
25	12	13	6	227	TT1	R/-W	TT	STAT
27	9	14	5	248	TT2	Invalid	TT	STAT
29	10	15	4	244	TT3	A Only	TT	STAT
31	5	16	3	238	TT4		TT	STAT
33	6	17	2	241	TSIZ0		TSIZ	STAT
35	3	18	1	232	TSIZ1		TSIZ	STAT
37	4	19	0	237	TSIZ2		TSIZ	STAT

Table 27. PowerPC 601 Logic Analyzer Interface Signal List - Pod P9

2x20 pin	2x14 pin	2x10 pin	LA bit	601 pin	signal name	analyzer label
3	13	3	clk1	282	2X_PCLK	2XPCLK
7	25	4	15		--	
9	26	5	14		--	
11	23	6	13	231	APE	APE-
13	24	7	12	222	DPE	DPE-
15	19	8	11	67	AP0	AP
17	20	9	10	68	AP1	AP
19	17	10	9	69	AP2	AP
21	18	11	8	71	AP3	AP
23	11	12	7	203	DP0	DP
25	12	13	6	202	DP1	DP
27	9	14	5	201	DP2	DP
29	10	15	4	199	DP3	DP
31	5	16	3	198	DP4	DP
33	6	17	2	197	DP5	DP
35	3	18	1	195	DP6	DP
37	4	19	0	194	DP7	DP

Table 27. PowerPC 601 Logic Analyzer Interface Signal List - Pod P10

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer labels	
3	13	3	clk1		--		
7	25	4	15		--		
9	26	5	14		--		
11	23	6	13		--		
13	24	7	12		--		
15	19	8	11		--		
17	20	9	10		--		
19	17	10	9		--		
21	18	11	8		--		
23	11	12	7	72	CKSTP_OUT	CHKOUT	
25	12	13	6		--		
27	9	14	5	215	CSE0		CSE
29	10	15	4	211	CSE1		CSE
31	5	16	3	212	CSE2		CSE
33	6	17	2	273	RTC	RTC	
35	3	18	1		--		
37	4	19	0	254	RSRV	RSRV-	

Table 28. PowerPC 603 Logic Analyzer Interface Signal List - Pod P1

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer labels	
3	13	3	clk1	221	CLKOUT		CLKOUT
7	25	4	15	231	AP0	AP	
9	26	5	14	230	AP1	AP	
11	23	6	13	227	AP2	AP	
13	24	7	12	226	AP3	AP	
15	19	8	11	186	MCP		MCP-
17	20	9	10	187	SMI		SMI-
19	17	10	9	198	TDO		TDO
21	18	11	8	200	TMS		TMS
23	11	12	7	199	TDI		TDI
25	12	13	6	202	TRST		TRST-
27	9	14	5	--	--		
29	10	15	4	205	LSSDMODE		LSSDMO
31	5	16	3	213	PLLCF0	PLLCFG	
33	6	17	2	211	PLLCF1	PLLCFG	
35	3	18	1	210	PLLCF2	PLLCFG	
37	4	19	0	208	PLLCF3	PLLCFG	

Table 28. PowerPC 603 Logic Analyzer Interface Signal List - Pod P2

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer labels		
3	13	3	clk1	235	QACK			QACK-
7	25	4	15	214	HRESET	STAT		HRESET-
9	26	5	14	215	CKSTP	STAT		CKSTP-
11	23	6	13	216	CHECK STOP	STAT		CKHOUT
13	24	7	12	219	BR	STAT		BR-
15	19	8	11	224	TC0	STAT	TC	TC0
17	20	9	10	223	TC1	STAT	TC	TC1
19	17	10	9	236	WT	STAT		WT-
21	18	11	8	237	CI	STAT		CI-
23	11	12	7	1	GBL	STAT		GBL-
25	12	13	6	25	DBW0	STAT		DBW0-
27	9	14	5	26	DBG	STAT		DBG-
29	10	15	4	27	BG	STAT		BG-
31	5	16	3	28	AACK	STAT	ACKs	AACK-
33	6	17	2	31	QREQ	STAT		QREQ-
35	3	18	1	32	ARTRY	STAT	ACKs	ARTRY-
37	4	19	0	36	ABB	STAT		ABB-

Table 28. PowerPC 603 Logic Analyzer Interface Signal List - Pod P3

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer label
3	13	3	clk1	--		
7	25	4	15	179	A0	ADDR
9	26	5	14	2	A1	ADDR
11	23	6	13	178	A2	ADDR
13	24	7	12	3	A3	ADDR
15	19	8	11	176	A4	ADDR
17	20	9	10	5	A5	ADDR
19	17	10	9	175	A6	ADDR
21	18	11	8	6	A7	ADDR
23	11	12	7	174	A8	ADDR
25	12	13	6	7	A9	ADDR
27	9	14	5	170	A10	ADDR
29	10	15	4	11	A11	ADDR
31	5	16	3	169	A12	ADDR
33	6	17	2	12	A13	ADDR
35	3	18	1	168	A14	ADDR
37	4	19	0	13	A15	ADDR

Table 28. PowerPC 603 Logic Analyzer Interface Signal List - Pod P4

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer label
3	13	3	clk1	212	SYSCLK	SYSCLK
7	25	4	15	166	A16	ADDR
9	26	5	14	15	A17	ADDR
11	23	6	13	169	A18	ADDR
13	24	7	12	16	A19	ADDR
15	19	8	11	164	A20	ADDR
17	20	9	10	17	A21	ADDR
19	17	10	9	160	A22	ADDR
21	18	11	8	21	A23	ADDR
23	11	12	7	157	A24	ADDR
25	12	13	6	22	A25	ADDR
27	9	14	5	158	A26	ADDR
29	10	15	4	23	A27	ADDR
31	5	16	3	151	A28	ADDR
33	6	17	2	30	A29	ADDR
35	3	18	1	144	A30	ADDR
37	4	19	0	37	A31	ADDR

Table 28. PowerPC 603 Logic Analyzer Interface Signal List - Pod P5

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer labels		
3	13	3	clk1	180	TT4			TT4
7	25	4	15	197	TSIZ0	STAT	TSIZ	
9	26	5	14	196	TSIZ1	STAT	TSIZ	
11	23	6	13	195	TSIZ2	STAT	TSIZ	
13	24	7	12	192	TBST	STAT	TSIZ	TBST-
15	19	8	11	191	TT0	STAT	TT	Atomic
17	20	9	10	190	TT1	STAT	TT	R/W-
19	17	10	9	185	TT2	STAT	TT	Invldt
21	18	11	8	184	TT3	STAT	TT	A Only
23	11	12	7	189	SRESET	STAT		SRESET-
25	12	13	6	188	INT	STAT		INT-
27	9	14	5	156	DRTRY	STAT	ACKs	DRTRY
29	10	15	4	155	TA	STAT	ACKs	TA-
31	5	16	3	154	TEA	STAT	ACKs	TEA-
33	6	17	2	150	XATS	STAT		XATS-
35	3	18	1	149	TS	STAT		TS-
37	4	19	0	145	DBB	STAT		DBB-

Table 28. PowerPC 603 Logic Analyzer Interface Signal List - Pod P6

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer labels
3	13	3	clk1	201	TCK	TCK
7	25	4	15	204	L1TSTCLK	L1Tclk
9	26	5	14	203	L2TSTCLK	L2Tclk
11	23	6	13	218	APE	APE
13	24	7	12	217	DPE	DPE
15	19	8	11	225	CSE	CSE
17	20	9	10	232	RSRV	RSRV-
19	17	10	9	234	TBEN	TBEN
21	18	11	8	233	TBLISYNC	TBLISY
23	11	12	7	38	DP0	DP
25	12	13	6	40	DP1	DP
27	9	14	5	41	DP2	DP
29	10	15	4	42	DP3	DP
31	5	16	3	46	DP4	DP
33	6	17	2	47	DP5	DP
35	3	18	1	48	DP6	DP
37	4	19	0	50	DP7	DP

Table 28. PowerPC 603 Logic Analyzer Interface Signal List - Pod P7

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer label
3	13	3	clk1			
7	25	4	15	85	DH16	DATA
9	26	5	14	84	DH17	DATA
11	23	6	13	83	DH18	DATA
13	24	7	12	82	DH19	DATA
15	19	8	11	81	DH20	DATA
17	20	9	10	80	DH21	DATA
19	17	10	9	78	DH22	DATA
21	18	11	8	76	DH23	DATA
23	11	12	7	75	DH24	DATA
25	12	13	6	74	DH25	DATA
27	9	14	5	73	DH26	DATA
29	10	15	4	72	DH27	DATA
31	5	16	3	71	DH28	DATA
33	6	17	2	68	DH29	DATA
35	3	18	1	67	DH30	DATA
37	4	19	0	66	DH31	DATA

Table 28. PowerPC 603 Logic Analyzer Interface Signal List - Pod P8

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer label
3	13	3	clk1	--		
7	25	4	15	117	DL16	DATA_B
9	26	5	14	107	DL17	DATA_B
11	23	6	13	106	DL18	DATA_B
13	24	7	12	105	DL19	DATA_B
15	19	8	11	102	DL20	DATA_B
17	20	9	10	101	DL21	DATA_B
19	17	10	9	100	DL22	DATA_B
21	18	11	8	51	DL23	DATA_B
23	11	12	7	52	DL24	DATA_B
25	12	13	6	55	DL25	DATA_B
27	9	14	5	56	DL26	DATA_B
29	10	15	4	57	DL27	DATA_B
31	5	16	3	58	DL28	DATA_B
33	6	17	2	62	DL29	DATA_B
35	3	18	1	63	DL30	DATA_B
37	4	19	0	64	DL31	DATA_B

Table 28. PowerPC 603 Logic Analyzer Interface Signal List - Pod P9

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer label
3	13	3	clk1	--		
7	25	4	15	115	DH0	DATA
9	26	5	14	114	DH1	DATA
11	23	6	13	113	DH2	DATA
13	24	7	12	110	DH3	DATA
15	19	8	11	109	DH4	DATA
17	20	9	10	108	DH5	DATA
19	17	10	9	99	DH6	DATA
21	18	11	8	98	DH7	DATA
23	11	12	7	97	DH8	DATA
25	12	13	6	94	DH9	DATA
27	9	14	5	93	DH10	DATA
29	10	15	4	92	DH11	DATA
31	5	16	3	91	DH12	DATA
33	6	17	2	90	DH13	DATA
35	3	18	1	89	DH14	DATA
37	4	19	0	87	DH15	DATA

Table 28. PowerPC 603 Logic Analyzer Interface Signal List - Pod P10

2x20 pin	2x14 pin	2x10 pin	LA bit	603 pin	signal name	analyzer label
3	13	3	clk1	153	DBDIS	DBDIS-
7	25	4	15	143	DL0	DATA_B
9	26	5	14	141	DL1	DATA_B
11	23	6	13	140	DL2	DATA_B
13	24	7	12	139	DL3	DATA_B
15	19	8	11	135	DL4	DATA_B
17	20	9	10	134	DL5	DATA_B
19	17	10	9	133	DL6	DATA_B
21	18	11	8	131	DL7	DATA_B
23	11	12	7	130	DL8	DATA_B
25	12	13	6	129	DL9	DATA_B
27	9	14	5	126	DL10	DATA_B
29	10	15	4	125	DL11	DATA_B
31	5	16	3	124	DL12	DATA_B
33	6	17	2	123	DL13	DATA_B
35	3	18	1	119	DL14	DATA_B
37	4	19	0	118	DL15	DATA_B

A

If You Have a Problem

If You Have a Problem

Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Hewlett-Packard service center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and preprocessors. Otherwise, you may damage circuitry in the analyzer, preprocessor, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reseat all cables and probes, ensuring that there are no bent pins on the preprocessor interface or poor probe connections.**
- ☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive Loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ☐ **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and preprocessor interface connections.
- ☐ Check for bent or damaged pins on the preprocessor probe.

No trace list display

If there is no trace list display, it may be that your analysis specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your analysis sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Target System Problems

This section lists problems that you might encounter with the target system. If the solutions suggested here do not correct the problem, you may have a damaged preprocessor. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the logic analyzer, the microprocessor (if socketed) or the cables may not be installed properly, or they may not be making electrical contact.

☐ **Ensure that you are following the correct power-on sequence for the logic analyzer and target system.**

1 Power up the analyzer.

2 Power up the target system.

If you power up the target system before you power up the logic analyzer, interface circuitry may latch up and prevent proper target system operation.

☐ **Verify that the microprocessor and the cables are securely inserted into their respective sockets.**

☐ **Verify that the logic analyzer cables are in the proper sockets of the target system and are firmly inserted.**

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ☐ **Do a full reset of the target system before beginning the measurement.**

  Some designs require a full reset to ensure correct configuration.

- ☐ **Ensure that your target system meets the timing requirements with the logic analyzer probe connected.**

  See "Capacitive Loading" in this chapter. While logic analyzer loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

  Microprocessors such as the i486, Pentium™, and MC68040 generate substantial heat. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the logic analyzer, or system lockup in the microprocessor. All interfaces add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ☐ **Remove as many pin protectors, extenders, and adapters as possible.**

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the preprocessor or in your target system. If you follow the suggestions in this section to ensure that you are using the preprocessor and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect synchronization, modified configuration, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- ☐ **Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the cursor position) and pressing the Invasm key.**

  The inverse assembler works from the first line of the trace *display.* If you jump to the middle of a trace and select Invasm, prior trace states may not be disassembled correctly. If you move to several random places in the trace list and synchronize the disassembly each time, the trace disassembly is only guaranteed to be correct for the portion of the trace list disassembled. See "To synchronize the inverse assembler" in Chapter 2 for more information.

- ☐ **Ensure that each logic analyzer pod is connected to the correct connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and connector numbers. Target systems must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each connector are often altered to support that need. Thus, one target system might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 1 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some preprocessors also require other data labels. See Chapter 2 for more information.

- ☐ **Verify that all microprocessor caches and memory managers have been disabled.**

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

- ☐ **Verify that storage qualification has not excluded storage of all the needed opcodes and operands.**

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **Ensure that the inverse assembler is on the same disk as the configuration files you are loading.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler or rename it, the configuration process will fail to load the disassembler.

  See Chapter 1 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- ☐ **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- ☐ **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

Messages

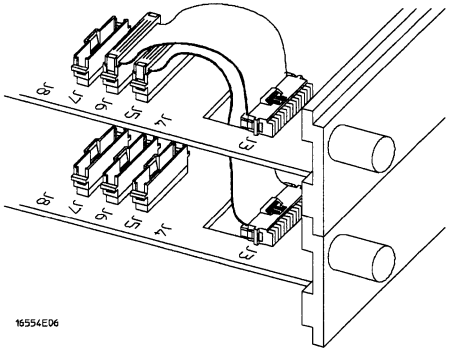
This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

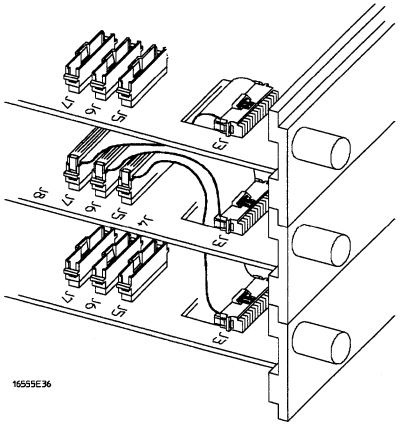
This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly for two or three HP 16550A logic analysis cards. The following diagrams show the correct cable connections for two-card and three-card installations. Ensure that your cable connections match the silk screening on the card. Then, repeat the measurement.



Cable Connections for Two-Card HP 16550A Installations



Cable Connections for Three-Card HP 16550A Installations

See Also

The *HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ **Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.**

See Also Chapter 1 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ **This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500A/B or HP 16501A frame. Ensure that the cards are firmly seated.**
- ☐ **This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.**
- ☐ **If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the preprocessor interface. See Chapter 1 to determine the proper connections.**

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- ☐ When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

Your Comments Please

HP E2449B

Your comments assist us in meeting your needs better. Please complete this questionnaire and return it to us. Feel free to add any additional comments that you might have. All comments and suggestions become the property of Hewlett-Packard. Omit any questions that you feel would be proprietary.

	Yes	No
1. Did you receive your product when expected?	[ ]	[ ]
2. Were you satisfied with the operation of the preprocessor interface at turn-on?	[ ]	[ ]

3. Were the proper accessories supplied with your product?

   If not, what was missing?

   Cables [ ] Manual(s) [ ] Other _____

4. What measurements will this preprocessor interface be used to make? _____

   _____

5. Which logic analyzer are you using?

   _____

6. What do you like most about the preprocessor interface? _____

   _____

7. What would you like to see changed or improved? _____

   _____

   _____

8. Which sections of the manual have you used?

   [ ] Installation Overview
   [ ] Step-By-Step Procedures
   [ ] Characteristics

9. Please rate the manuals on the following:

   4=Excellent 3=Good 2=Adequate 1=Poor

   [ ] Breadth and depth of information
   [ ] Ability to easily find information
   [ ] Ability to understand and apply the information provided in the manual

   Please explain: _____

   _____

   _____

10. What is your experience with logic analyzers and proprocessor interfaces?

    [ ] No previous experience
    [ ] Less than 1 year experience
    [ ] More than 1 year's experience on one model
    [ ] More than 1 year's experience on several models

Name _____ Company _____

Address _____

_____ Zip Code _____

Phone _____ Instrument Serial # _____

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New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by you. The dates on the title page change only when a new edition is published.

A software or firmware code may be printed before the date. This code indicates the version level of the software or firmware of this product at the time the manual or update was issued. Many product updates and fixes do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

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