

NPC-700
LOGIC ANALYSIS SYSTEM
OPERATOR'S MANUAL

**** WARNING ****

DO NOT REMOVE THE TOP COVER UNLESS THE AC LINE CORD IS FIRST UNPLUGGED.

BEFORE APPLYING POWER TO THE NPC-700, MAKE CERTAIN THAT THE PROGRAMMABLE AC VOLTAGE SELECTOR CARD, WHICH PLUGS INTO THE POWER MODULE AT THE REAR OF THE UNIT, IS INSERTED IN THE POSITION CORRESPONDING TO THE LINE VOLTAGE BEING USED; OTHERWISE, SERIOUS DAMAGE TO THE INTERNAL SWITCHING POWER SUPPLY MAY OCCUR. SEE SECTION 2.3.2

SERVICE OF THIS INSTRUMENT SHOULD ONLY BE PERFORMED BY SKILLED MAINTENANCE PERSONNEL.

APPLICABLE DOCUMENTS:

CP/M[®] SOFTWARE DOCUMENTATION

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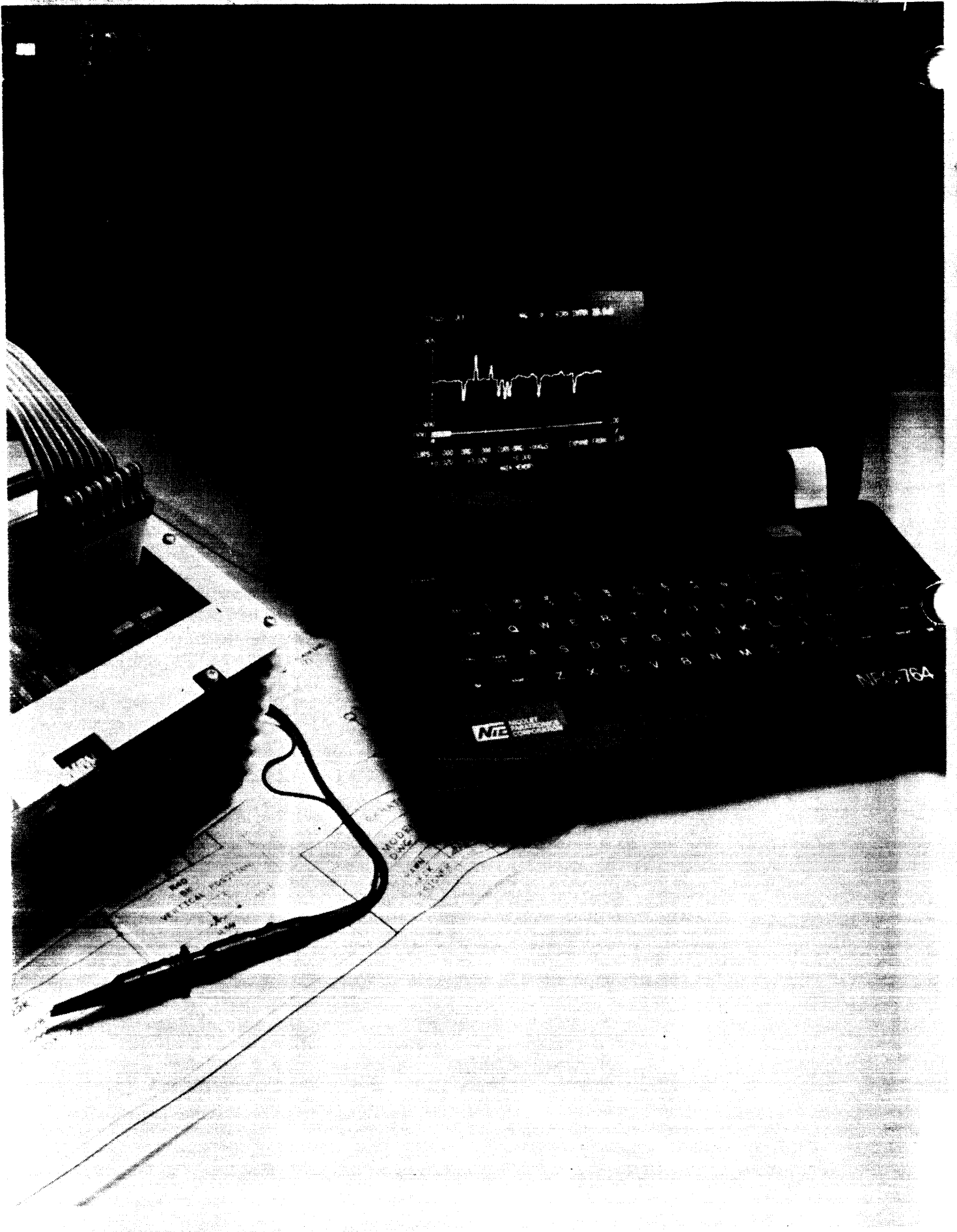
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A NOTE ABOUT THIS MANUAL...

This Operator's Manual describes the NPC-748 and the NPC-764 Logic Analysis Systems. These two systems are identical with two major exceptions: The NPC-748 has 16 fewer state channels and does not incorporate the floppy disk and the associated CP/M[®] Operating System found in the NPC-764. (However, the NPC-748 is upgradable to the NPC-764.)

Because of the similarities between the NPC-748 and NPC-764, the term "NPC-700" is used when describing common features. In all other cases, the appropriate model number is used.

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SECTION 1.0

INTRODUCTION

1.0 INTRODUCTION

The NPC-700 series are ASCII-keyboard instruments consisting of the NPC-748, a lower-cost, forty-eight-channel, logic analysis system ideal for general-purpose troubleshooting; and the top-of-the-line NPC-764, a sixty-four-channel, disk-based, analyzer/computer/controller which can be used in all phases of a product's life-cycle: design, development, production test, and service. The NPC-748 can be modularly upgraded to the NPC-764 at any time.

1.1 ELECTRONIC WORKBENCH

In order to simplify your overall engineering tasks, a comprehensive set of easy-to-use, ROM-based analysis tools are integrated in the NPC-700 series as shown below:

	State Analysis	Timing Analysis	Analog Waveform Recording	Counter-Timer	Signature Analysis	Serial Analysis	Computer/Controller
NPC-748	32 channels	16 channels	1 channel	Yes	Yes	Yes	No
NPC-764	48 channels	16 channels	1 channel	Yes	Yes	Yes	Yes

These test functions, powerful in their own right, can be used individually or linked together for analyzing problems that cross the hardware and software boundaries in your system.

Besides having 16 additional state channels, the NPC-764 incorporates 48K of user-RAM and a single-sided, double-density, 5 $\frac{1}{4}$ " floppy disk drive (expandable to 4 drives). This gives you full access to the instrument's internal CP/M[®]-based microcomputer for test storage, test automation, and general-purpose computational tasks which can include circuit analysis, simulation, and word processing. And since the NPC-764 operates as a powerful, IEEE-488 controller, you can add GPIB test equipment for a fully-automated test set-up. The architecture of the NPC-764 is shown in Figure 1-1.

® CP/M is a registered trademark of Digital Research.

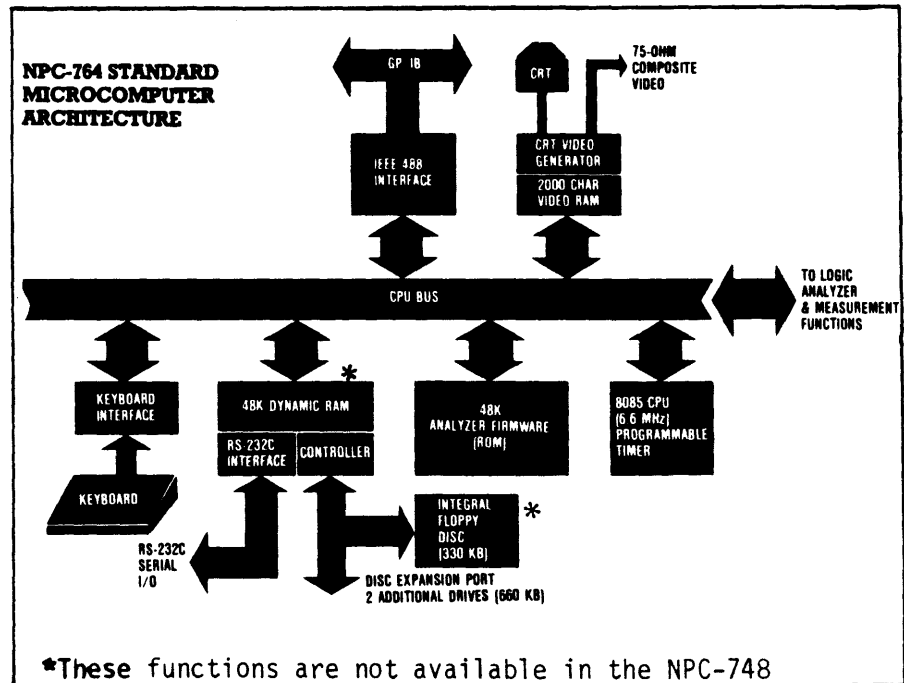


Figure 1-1. The architecture of the NPC-764.

1.2 USER-FRIENDLY

From start-up, both NPC-700 series instruments are easy-to-operate even for the occasional user. Menus are organized in a natural and comfortable manner that take you quickly and simply through the desired test. Prompting messages, soft keys and labels, minimize the need to reference this manual.

Simple problem-solving and meaningful data collections can be performed without any special set-ups because all menus default to the most commonly-used parameters. For example, when you're monitoring the operation of a microprocessor, all it takes is a single keystroke on the NPC-700 to see if your ADDRESS, DATA and STATUS signals are functioning properly.

1.3 RAPID SET-UP

When power is first applied to an NPC-700 series instrument, a Configuration List, containing twelve test and measurement modes, appears on a 9", 80-character by 25-line, CRT display. At the bottom of the display are labels for six software-directed (or "soft") keys which allow you to select the mode best suited to your application.

```

      NICOLET PARATRONICS

      NICOLET PARATRONICS 764 CONFIGURATION  VER 4.3

      1 - 48 CHNL STATE
      2 - 16 CHNL TIMING
      3 - 48 CHNL STATE/16 CHNL TIMING
      4 - 8 CHNL TIMING (100MHZ 2000 WORD)
      5 - 48 CHNL STATE/8 CHNL TIMING
      6 - 8 CHNL TIMING GLITCH
      7 - 48 CHNL STATE/8 CHNL GLITCH
      8 - WAVEFORM RECORDER
      9 - 48 CHNL STATE/WAVEFORM
     10 - COUNTER/TIMER
     11 - SIGNATURE ANALYZER
     12 - PI 70 SERIAL PROBE TRANSMIT

      ESC - DISK OPERATING SYSTEM

      BREAK - PROCESSOR SELF-TEST

      I - I/O CONFIGURATION MENU
  
```

Figure 1-2. Configuration Menu.

Once the desired mode is selected, the corresponding menu is displayed with its own set of soft-key labels. The soft keys allow you to access the menu fields so you can enter in test parameters from the ASCII keyboard. If an entry error occurs, a message appears on the CRT telling you which keys are valid for the current menu operation.

```

      NICOLET PARATRONICS

      48 CHANNEL STATE MENU

      FORMAT: AAAAAAAAAA AAAAAAAAAA BBBB BBBB CCCDDDD DDEEEEEE FFFFFFFF
              A HEX B BIN C BIN D DEC E OCT F ASC
      CLK SEL: A PRB: P B PRB: A C PRB: A QUALIFIERS: -AABBCC EL
      CLK QUAL: OFF
              OR OFF
      PRE-TRIG MEMORY (0-999): 010 WORDS
      RESTART: OFF

      TRIGGER:
      0      0040 XXXXXXXX XXX XX XX XX -XXXXXX XX
      1 THEN 0055 XXXXXXXX XXX XX XX XX -XXXXXX XX
              AFTER 0100 CLOCKS
      2 THEN 0062 XXXXXXXX XXX XX XX XX -XXXXXX XX
              BEFORE 0020 CLOCKS
  
```

Figure 1-3. State Menu. Three of sixteen levels of triggering are shown.

Menu fields controlling advanced triggering modes can be turned off at any time, reducing your triggering set-up to a simpler form. In this manner, you can check that basic triggering conditions can be satisfied before activating the advanced set-up. This illustrates the time-saving, "start simple and build" philosophy behind the NPC-700 series: Advanced features do not get in the way of simple problem-solving--but they're available and readily accessible when you need them.

1.4 THE NPC-764'S FLOPPY DISK FOR TEST STORAGE

The NPC-764's integral 5¼" floppy disk drive can further reduce your test time. Simple commands allow you to store menu set-ups and test results. Later, these tests can be recalled and executed. A blank diskette can accommodate up to 50 individual tests.

Each stored test can incorporate comments, instructions, and other pertinent information. For example, in an engineering lab application, test comments could include: date of test, name of engineer, test or probing procedures, and remarks. On the production line or in the field, step-by-step procedures can accompany stored tests to increase the productivity of test personnel.

```

A>ED AUTOTEST.SUB

NEW FILE

TO THE OPERATOR: YOU'RE GOING TO PERFORM 3 TESTS.
IT'S IMPORTANT THAT YOU FOLLOW THE INSTRUCTIONS CAREFULLY.

STATE TEST: AFTER READING THE INSTRUCTIONS BELOW, PRESS RETURN
WHEN THE CURSOR FLASHES. THIS WILL CALL THE STATE TEST.

A. CONNECT THE A STATE PROBE TO THE A SIDE OF THE TEST CARD.
B. WHEN THE CONFIGURATION LIST APPEARS, PRESS THE COLLECT KEY.
C. AFTER THE TEST IS COMPLETE, PRESS THE CONFIG KEY FOLLOWED BY THE
ESC KEY TO RECEIVE INSTRUCTIONS FOR THE NEXT TEST.

REMEMBER, PRESS RETURN WHEN THE CURSOR FLASHES.

PAUSE
LARECALL STATE

TIMING TEST

A. CONNECT THE B TIMING PROBE TO THE B SIDE OF THE TEST CARD.
B. WHEN THE CONFIGURATION LIST APPEARS, PRESS THE COLLECT KEY.
    
```

Figure 1-4. Simple automated test program with operator prompts.

1.5 THE NPC-764 FOR TEST AUTOMATION AND GENERAL-PURPOSE COMPUTING

The NPC-764 System Block Diagram is shown in Figure 1-5.

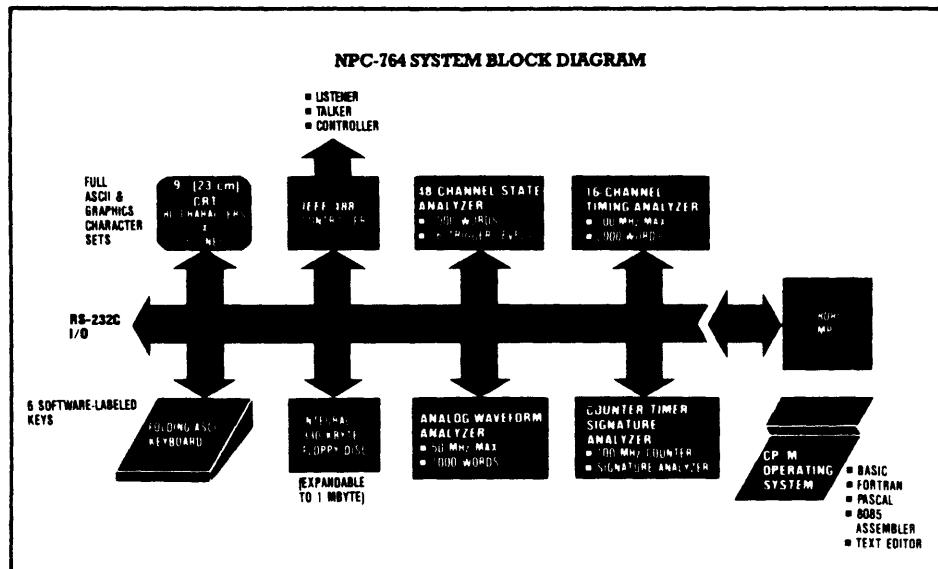


Figure 1-5. The bus structure of the NPC-764. (The NPC-748 is similar.)

In conjunction with its CP/M Operating System, the NPC-764's internal microcomputer allows you to:

- Automatically execute a series of stored tests using simple CP/M commands or the built-in GPIB CONTROLLER. Standard IEEE-488 commands in CBASIC permit the automation of internal test functions as well as the control of external GPIB instruments.
- Execute commercially-available* CP/M application programs for solving engineering equations, circuit simulation, and report generation--even before hardware and software have been developed.
- Generate programs in CBASIC, FORTRAN, PASCAL, and other high-level-languages to support your particular application. CBASIC is included at no cost with your NPC-764.
- Construct a low-cost, universal development system. Commercially-available compilers and assemblers, in-circuit emulators, and a disk expansion chassis, add software development capabilities to the NPC-764.

1.6 THE NPC-700'S LOGIC STATE ANALYZER

Each NPC-700 series analyzer incorporates a logic state section with some of the most powerful software debugging features available in the industry--features that are readily accessed through the ASCII keyboard. Upon initial selection, the state menu defaults to the most commonly-used parameters so you can collect meaningful data immediately.

When you need more debugging power, you can "build" on the basic state menu by calling up additional triggering levels, qualifiers, and other features. Operator prompts minimize your set-up time. A typical NPC-764 state menu is shown in Figure 1-6.

```

                                NICOLET PARATRONICS

                                48 CHANNEL STATE MENU

FORMAT:  AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA
          A HEX
CLK SEL:  A PRB: P  B PRB: A  C PRB: A  QUALIFIERS: -AABBCC EL
CLK QUAL: OFF
          OR OFF
PRE-TRIG MEMORY (0-999): 000 WORDS
RESTART:  OFF
TRIGGER:
O         XXXXXXXXXXXX -XXXXXX XX
END
```

Figure 1-6. The NPC-764 state menu. (The NPC-748 is similar.)

*Lifeboat Associates, 1641 Third Avenue, New York, NY 10028.
Telephone: 212/860-0300. TWX: 710/581-2524. Telex: 640693.
Specify format code SX when ordering applications software.

1.6.1 POWERFUL SOFTWARE ANALYSIS

The state analyzer section for each NPC-700 series instrument is summarized below.

	State Channels	Clock Qualifiers	Number of Clock Inputs	Main Memory Depth	Auxiliary Memory Depth	Trigger Levels	Pre-Triggering
NPC-748	32	Dual 37-Bit Wide	2	1000 Words	1000 Words	16	0-999 Words
NPC-764	48	Dual 55-Bit Wide	3	1000 Words	1000 Words	16	0-999 Words

These state analyzers allow you to collect ADDRESS, DATA, STATUS, or other synchronous occurrences from the digital portion of your system, at real-time rates up to 12.5 million events per second. And both instruments feature menu-controlled linkage to internal or external test and measurement functions.

1.6.2 COLLECTING CLOCK QUALIFIED DATA

The NPC-700's clock qualification mode extends the trace capabilities of each state analyzer's 1000-word memory by restricting the data collection to events of specific interest. The clock qualification field in the state menu is partitioned into two sections: an internal clock qualifier field and an external field. See Figure 1-7.

```

NICOLET PARATRONICS

48 CHANNEL STATE MENU

FORMAT: AAAAAAAAAA AAAAAAAAAA BBBCCDDDD DEEEEEEE XXXXXXXX XXXXXXXX
        A HEX B OCT C DEC D BIN E ASC
CLK SEL: A PRB: P B PRB: A C PRB: A QUALIFIERS: -AABCC EL
CLK QUAL: 004X X X XXXX XX, -XXXXXX X, External
          OR OFF Internal
PRE-TRIG MEMORY (0-999): 000 WORDS
RESTART: OFF
TRIGGER:
0
XXXXXXXXXXXX -XXXXX XX
END
    
```

Figure 1-7. The clock qualifier field. (NPC-764 shown.)

The internal field is used to "self-qualify" the data coming into the analyzer from the probes. If a match occurs between the pattern set into the internal field and an incoming data word, then that data word is clocked into the memory. Since the internal clock qualifier field can be as wide as the maximum number of channels of the state analyzer, one application of this function is to collect data over a certain range of addresses or data words. This is accomplished by specifying, in the internal field, only the most significant address or data bits and leaving the remaining bits unspecified (don't care).

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The external clock qualifier field uses separate lines (2 per 16-channel state probe plus 1 BNC input at the rear of the analyzer) to control the data collection. If one or more of the bits in the external field are set, the signals on the corresponding probe qualifier lines must match in order to clock data into the memory. A typical application is to use microprocessor status signals to restrict the data collection to memory, I/O or other operations of interest.

The clock qualifier fields for each NPC-700 state analyzer are partitioned as follows:

	Internal Field	External Field		Total State Clock Qualifier Field
	Data Probe Inputs	Data Probe Qualifiers	EXT BNC Connector	
NPC-748	32	4	1	37
NPC-764	48	6	1	55

6.3 MULTIPHASE CLOCKING

Multiphase clocking allows the data from the 16-channel state probes to be strobed into the analyzer at different times but displayed as if all incoming data were present simultaneously. For example, to simplify program tracing, a multiplexed ADDRESS/DATA bus can be deinterleaved so that address and corresponding data words are displayed side-by-side.

1.6.4 MULTI-LEVEL TRIGGERING

For branch and subroutine analysis, both NPC-700 state analyzers offer multi-level triggering with auto or manual restart capabilities. Using the state menu, you can build up to 16 levels of sequential triggering to trace deeply-nested sections of your code. Like the clock qualifier function, the NPC-700's state triggering levels are each divided into an internal field and an external field. See Figure 1-8.

```

NICOLET PARATRONICS
48 CHANNEL STATE MENU
FORMAT: AAAAAAAAAA AAAAAAAAAA BBCCDDDD DEEEEEEE XXXXXXXX XXXXXXXX
        A HEX B OCT C DEC D BIN E ASC
CLK SEL: A PRB: P B PRB: A C PRB: A QUALIFIERS: -AABCC EL
CLK QUAL: 004X X X XXXX XX -XXXXXX X
          OR OFF
PRE-TRIG MEMORY (0-999): 000 WORDS
RESTART: OFF
TRIGGER:
0        0040 X X XXXX XX -XXXXXX XX
1 THEN  0041 X X XXXX XX -XXXXXX XX           ON 2049 CLOCKS
2 THEN  0042 X X XXXX XX -XXXXXX XX           ON 3073 CLOCKS
3 THEN  005A X X XXXX XX -XXXXXX XX           AFTER 2000 CLOCKS
          |           |
          Internal   External
          Field      Field
    
```

Figure 1-8. The trigger qualifier field. (NPC-764 shown.)

For triggering to occur, the incoming data from the probes must match the pattern specified in the internal field at each trigger level.

The trigger fields for each NPC-700 state analyzer are partitioned as follows:

	Internal Field	External Field			Total State Trigger Field
	Data Probe Inputs	Data Probe Qualifiers	EXT BNC Connector	Linkage Bit	
NPC-748	32	4	1	1	38
NPC-764	48	6	1	1	56

The external **trigger qualifier** field utilizes the same probe and rear panel BNC control lines as the external **clock qualifier** field--plus 1 linkage bit. A typical application is to connect the microprocessor's branch status signal to a trigger qualifier line to enable triggering only when a jump instruction is executed. Another typical and powerful application is to use the linkage bit to trigger the state analyzer when commanded by the timing analyzer, the waveform analyzer, or any other test instrument--including another NPC logic analyzer model.

Further, at each trigger level, you can specify the time relationship of the current trigger word to the prior trigger word. For example, you can specify that the trigger word at the current level occur **precisely n clocks** after the word on the prior level. Other ways to characterize this time relationship include: **after n clocks**, **before n clocks**, **not on n clocks**. You can also specify that the current trigger word **occur n times** before the state analyzer will advance to the next level.

Each NPC-700 series state analyzer also incorporates an **AUTO-RESTART** feature which automatically resets the analyzer back to the first trigger level in the event that a user-specified triggering sequence is not completely satisfied. This situation can occur, for example, when an unexpected branch occurs during the sequence, so that subsequent triggering conditions are not satisfied. There is also a user-controlled **RESTART** function which allows you to specify a pattern in the state menu that will reset the analyzer's trigger stack when that pattern occurs in the incoming data.

In all, each NPC-700 state analyzer offers approximately 150 state triggering combinations which can handle virtually any software debugging requirement you're likely to encounter.

1.6.5 ADDITIONAL TIME-SAVING FEATURES

To further save analysis time, data can be specified in the state menu for display in any combination of hexadecimal, octal, decimal, binary, or ASCII characters. Displayed information can be grouped into as many as six different fields, with each field one or more bits wide. You can also blank one or more bits anywhere in the data field. Using optional disassembly software, microprocessor **ADDRESS**, **DATA**, and **STATUS** words are disassembled into an easy-to-read, mnemonic format.

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For additional time-savings, both NPC-700 analyzers display test codes that provide a quick, short-hand method of uniquely identifying your data collection. For each block of collected data, 16 bits wide by 1000 words deep, a 4-digit hexadecimal test code is computed by the analyzer using a CRC-type data compression algorithm. Thus, two data collections can be quickly compared.

To further save time, you can put your NPC-700 to work overnight to detect and isolate hard-to-find, intermittent failures. Using the state auxiliary memory and a special triggering mode called **HOLD #**, you can compare a known good reference collection to unknown, incoming data. If the two collections match, the test is automatically repeated. If a difference is detected, the NPC-700 will display the faulty collection with all differences highlighted, ready for inspection when you arrive at work the next morning. And if you need to record the failure, a single command saves the test set-up and results on a diskette.

1.6.6 STATE ANALYSIS—ONLY ONE PART OF THE ELECTRONIC WORKBENCH

The debugging power of the state analyzer is further enhanced when used with the other test and measurement functions. For example, the state analyzer can be linked to the timing and waveform sections for cross-domain analysis; with the counter-timer/signature analyzer for system performance measurements; with the serial analyzer for debugging RS-232 interfaces; and with other, external instruments as part of a completely automatic test system.

1.7 THE NPC-700's INDEPENDENT TIMING ANALYZER

For hardware debugging, each NPC-700 series analyzer incorporates an independent timing analyzer with advanced triggering, data collection, and display capabilities. Like the state analyzer section, these capabilities, when initially selected, default to the most commonly used parameters so you can collect meaningful data with a minimum of keystrokes. For more in-depth hardware analysis, simple ASCII keyboard commands--coupled with operator prompts--reduce the time you'll need to invest in setting up complex tests. A typical NPC-700 timing menu is shown in Figure 1-9.

NICOLET PARATRONICS			
16 CHNL TIMING/STATE MENU			
5us CLOCK			
TRIGGER WHEN: TRIG OCCURS > 0000 CLOCKS AFTER FIRST ARM			
CHNL NO.	A76543210	B76543210	FILTER LINKAGE
ARM (0,1,X):	XXXXXXXX	XXXXXXXX	OFF NONE
TRIG (0,1,X):	11111111	XXXXXXXX	OFF NONE
INPUT MODE (S,L):	SSSSLLS	SSSSSSS	
PRE-TRIGGER (0-9):	10%		
DISPLAY ORDER (0-7,X):	AAAAAAA	BBBBBBB	
DISPLAY POLARITY (+,-):	76543210	76543210	
THRESHOLD:	A PROBE	B PROBE	HYSTERESIS
(-6.4V - +6.35V)	+1.60	+1.60	ON

Figure 1-9. The NPC-700 timing menu.

1.7.1 POWERFUL HARDWARE ANALYSIS

The timing analyzer section for each NPC-700 series instrument is summarized below.

	Timing Channels	Max Sampling Rate	Main Memory Depth	Auxiliary Memory Depth	Separate Glitch Memory	External Clock Input	External Clock Qualifier
NPC-764 and NPC-748	16	50 MHz @ 16 ch; 100 MHz @ 8 ch;	1000 words @ 16 ch; 2000 words @ 8 ch;	1000 words @ 16 ch; 2000 words @ 8 ch;	YES	1	1

Like the state section, the NPC-700's timing analyzer can be linked to other internal or external test and measurement functions to trace hardware and software interactions in your system.

1.7.2 ADVANCED TRIGGERING

The optimum number of triggering levels for a timing analyzer is two: Only one level makes relatively routine timing measurements difficult; while more than two levels implies branch and subroutine tracing applications which are best performed by the state analyzer.

For this reason, the NPC-700's timing analyzer includes two levels of word recognition--ARM and TRIG.

When you use both trigger levels, three conditions must be satisfied before the timing analyzer will collect data: First, the ARM event must occur; second, the specified delay between ARM and TRIG must be satisfied; and finally, the TRIG event must occur.

Because of the large number of interactive signals in today's digital systems, it is necessary for a timing analyzer to provide the user flexibility in specifying the time relationship between the ARM and TRIG events. The NPC-700's timing analyzer accomplishes this through the following powerful delay modes:

- TRIG occurs **GREATER THAN** nnnn clocks **AFTER FIRST ARM**
- TRIG occurs **AFTER** nnnn ARMS
- Glitch in ARM when TRIG valid

In the above modes, **GREATER THAN** can be changed to **LESS THAN** or **ON**; **AFTER** can be changed to **BEFORE**; **FIRST** can be **LAST**; **ARM** can be substituted for **ARM**; and **TRIG** for **TRIG**. The bar symbol over the ARM and TRIG words identifies the nonoccurrence triggering mode as described in the state section.

Thus, for example, if an expected TRIG event was not occurring exactly nnnn clocks after the ARM event had ended, you would simply use the following triggering mode to see what was really happening:

TRIG occurs ON nnnn clocks AFTER LAST ARM

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In all, there are approximately 50 timing triggering combinations which can handle virtually any hardware debugging requirement you're likely to encounter.

If your problem is broader in nature, involving hardware-software or even digital-analog interactions, you can readily link the triggering of the timing analyzer to various combinations of state, waveform, or other, external measurement resources. For example, by linking the timing and state sections, you can observe and measure the performance of both the hardware interrupts and the associated software routines.

1.7.3 COMPLEX TIMING MEASUREMENTS MADE EASY

Because timing information is generally more difficult to analyze than state or analog information, a good timing analyzer should have extensive, yet easy-to-use, display measurement and manipulation capabilities. The display facilities of the NPC-700's timing analyzer have evolved through three generations of analysis instruments and provide one of the most useable presentations of timing information on the market.

For instance, when timing information is displayed, a moveable, inverse video graticule gives you an overview of the position and amount of data being displayed relative to the entire contents of the timing memory. See Figure 1-10.

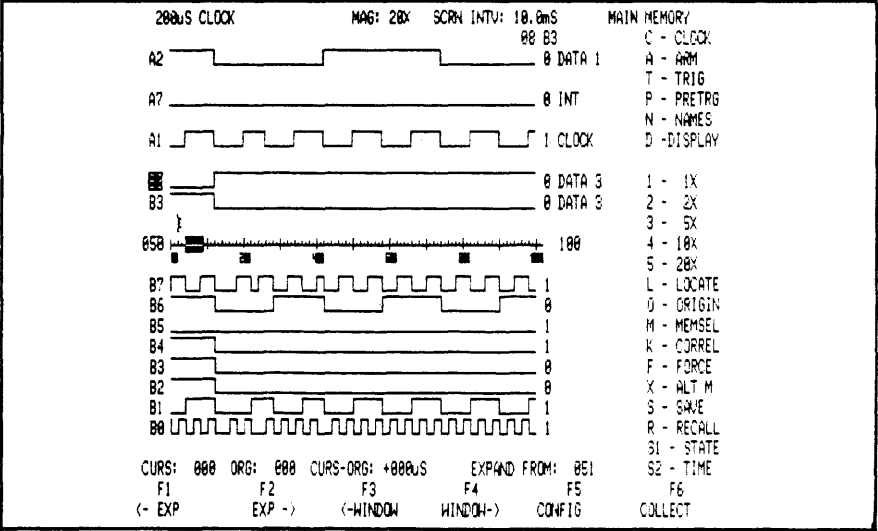


Figure 1-10. Typical NPC-700 timing display at 20X magnification.

Furthermore, all of the important timing parameters—sample rate, magnification factor (up to X20), screen interval, and the locations of the cursor and the origin—are all shown along with displayed data so you don't have to go back to the parameters in the menu to make sense of your timing measurements.

You can also name each channel with the 8-character label of your choice to make the display more meaningful.

If you need to rearrange the display order and polarity you don't have to adjust the probes; simply make the necessary changes in the timing menu. Probe thresholds and input comparator hysteresis are also ASCII keyboard selectable. A single keystroke gives you a state-equivalent display which can then be formatted in hexadecimal, octal, binary, decimal or ASCII.

1.7.4 COMPARISON TESTING

Like the state analyzer, the timing section has a separate, matching, auxiliary memory for comparing the current data collection with a known good reference. There is also a **CORRELATION** mode which tells you--on a channel-by-channel basis--how closely the main and auxiliary data collections match.

For example, if pulses are intermittently missing in a hardware sequencer, the data in the main and auxiliary memories will differ. Thus, the correlation factor for that particular channel will be low. A single keystroke selects a main/auxiliary memory comparison mode to automatically highlight those missing pulses.

If you'd like to have a permanent record of this and any other tests, along with the associated menu, simply save them on diskette.

1.7.5 RECONFIGURE THE TIMING MEMORY

For higher-speed work, you can select the **8-CHANNEL, 100 MHz** mode. In this mode, the 16-channel analyzer's 50 MHz sampling rate is doubled, as is its 1000-word memory. Thus, you can collect 2000 samples at 10 nS intervals, increasing the probability of capturing and viewing those high-speed problems.

Another mode, called the **8-CHANNEL GLITCH**, partitions the 16-channel timing memory into an 8-channel glitch memory and a corresponding 8-channel data memory. This mode is used to display glitches as they occur in relationship to actual data.

1.8 THE NPC-700's WAVEFORM ANALYZER

In spite of the proliferation of digital systems, it's still an analog world and you still have to run down problems caused by analog signals. That's why NPC offers a plug-in, waveform analyzer option for the NPC-700 series.

The waveform analyzer plug-in provides cost-effective, high-speed, waveform recording which you can use to uncover problems due to analog and digital interactions in your system. Using a 6-bit A/D converter, analog signals are sampled at rates to 50 MHz, providing an effective 3 dB bandwidth of 10 MHz.

Each time a data collection is initiated, 1000 samples are stored. Displayed sample points are software-smoothed for readability.

POWERFUL ANALOG ANALYSIS

The waveform analyzer section is summarized below:

	No. of Analog Channels	Max Sampling Rate	Main* Memory Depth	Auxiliary* Memory Depth	External Clock Input	Input Voltage Range	Pre-Triggering
NPC-764 and NPC-748	1	50 MHz	1000 Samples	1000 Samples	1	5 mV/DIV to 200 V/DIV	0-900 Samples

*The waveform analyzer uses the timing analyzer's main and auxiliary memories.

Like the state and timing analyzer sections, the waveform analyzer can be linked to other internal or external test and measurement functions.

1.8.1 SCOPE-TYPE MENU

The waveform menu is easy-to-use since it incorporates familiar, scope-like parameters. To record a waveform, select **PROBE TYPE, (X1/X10), INPUT COUPLING, ATTENUATOR, DC OFFSET, TRIGGER LEVEL, and TRIGGER SLOPE.** Next, select the free run or single shot mode and choose an appropriate sample rate, up to 50 MHz. See Figure 1-11.

```

                    NICOLET PARATRONICS

                    WAVEFORM ANALYZER MENU

                    PROBE TYPE: X1
                    INPUT COUPLING: DC
                    ATTENUATOR: 1 V /DIV
                    OFFSET (-1.00 TO +1.00): +0.00
                    (DYNAMIC RANGE -4.00V TO +4.00V )
                    TRIGGER LEVEL (0.00 TO 1.00): 1.00
                    TRIGGER SLOPE: c

                    USE TIMING MENU TO SELECT SAMPLE PERIOD,
                    TRIGGER MODE AND LINKAGE
                    SET ARM OR TRIGGER LINKAGE TO "W" FOR NON-AUTO-TRIGGER
    
```

Figure 1-11. Typical NPC-700 Waveform menu.

When an incoming analog signal meets the threshold and slope requirements you've set into the menu, the waveform analyzer will trigger and collect 1000 samples. These samples are stored in the timing analyzer's memory and can be displayed in one of the following four formats: software-smoothed, raw sample points, software interpolated, or binary.

1.8.2 EASY ANALOG MEASUREMENTS

The waveform display format is similar to that of the timing analyzer. A moveable, inverse video graticule at the bottom of the CRT indicates the position and the amount of the waveform being displayed relative to the entire 1000-sample data collection. For closer inspection, any section of the waveform can be magnified up

to 20 times. Also, any point on the waveform can be selected as the origin so you can directly read instantaneous voltage and time values as you sweep the cursor across the screen. See Figure 1-12.

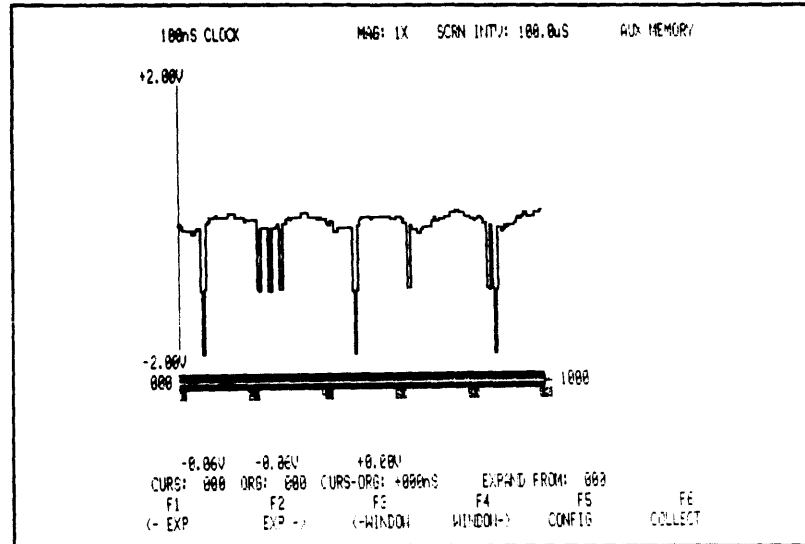


Figure 1-12. Typical Waveform display.

Like the state and timing analyzers, the waveform section allows you to store both the menu and a reference waveform for comparison testing. If you want permanent storage, the waveform and the associated menu can be transferred to diskette. You can even label the waveform for easy identification when the test is later recalled.

1.8.3 CROSS-DOMAIN ANALYSIS

Although the waveform analyzer is highly useful as a stand-alone tool, its enormous debugging power becomes apparent when you link it to the state or timing sections of the NPC-700. For example, when you need to closely examine the power-on characteristics of both the analog and digital portions of your system, you can set the waveform analyzer to trigger the state analyzer when the +5 volt power supply reaches a certain threshold. At this point, the NPC-700 will simultaneously collect both the +5 volt signal and the associated power-up subroutine.

As a second example, you can use the state analyzer to trigger the waveform analyzer upon the occurrence of an I/O address. The waveform analyzer could then be used to monitor the output signal at a serial port, while the state analyzer is collecting the associated I/O subroutine.

1.9 PERFORMANCE MONITORING USING THE COUNTER-TIMER PLUG-IN

As hardware and software become more complex, the time your system takes to complete a given task becomes an important consideration. That's why the NPC-700's plug-in, counter-timer option is a useful performance monitoring tool during system test and integration.

SECTION 1.0

INTRODUCTION

The counter-timer offers you a choice of 4 different modes of operation: **FREQUENCY**, **PERIOD**, **INTERVAL**, and **TOTAL**. For stand-alone operation, a single, scope-type probe allows you to make conventional counter-timer measurements at various points in your system. See Figure 1-13.

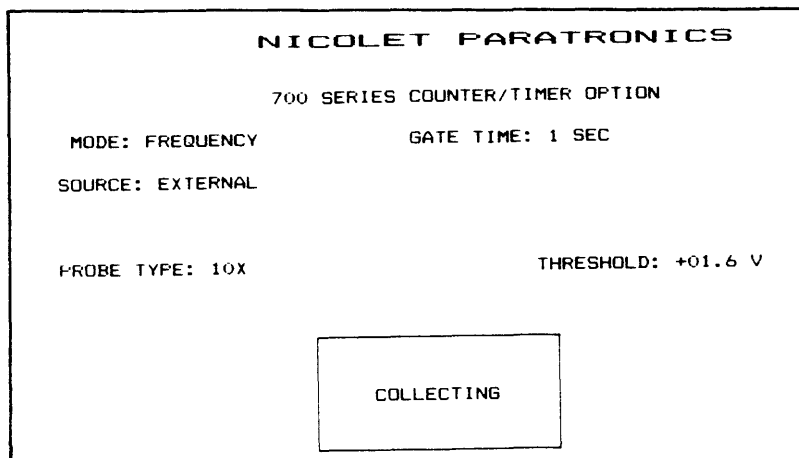


Figure 1-13. Typical Counter-Timer Menu.

However, for more complex measurements, particularly those involving performance monitoring, the counter-timer can be linked to the state analyzer's word recognizers, allowing measurements to be made on the data coming into the 16-channel state probes. See Figure 1-14.

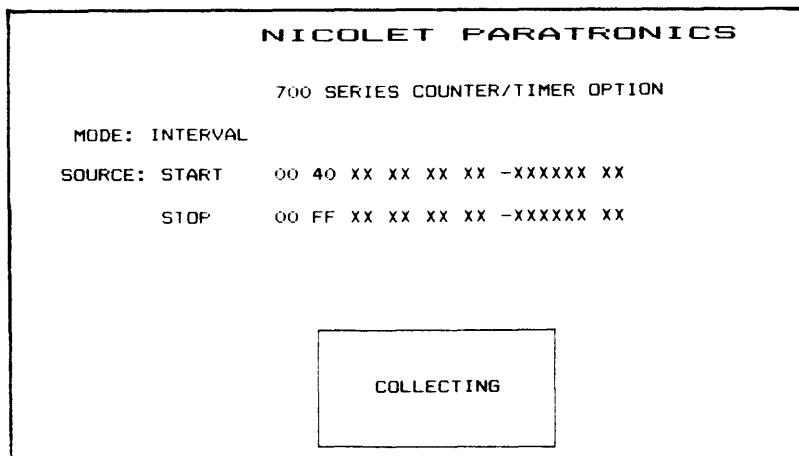


Figure 1-14. Measuring the interval between two state events.

**1.10 SIGNATURE ANALYSIS
FOR FAULT ISOLATION**

Using this internal linkage mode, performance monitoring examples include: measuring the frequency of occurrence or average period of a subroutine; counting the total number of times a particular address or data word occurs during a program; and determining the time elapsed during the execution of a particular segment of code.

The signature analyzer resides on the same plug-in board as the counter-timer. And like the counter timer, the signature analyzer can be linked to the state analyzer's word recognizers. This enables the start and stop signals to be a minimum of one bit wide, just like conventional signature analyzers, or equal to the channel width of the state data probes.

With a one-bit start and stop signal, a single scope-type probe is used to monitor the serial data stream associated with each node in the circuit-under-test. This serial data stream, gated by the start and stop signal, is used to develop the 4-digit signature. See Figure 1-15.

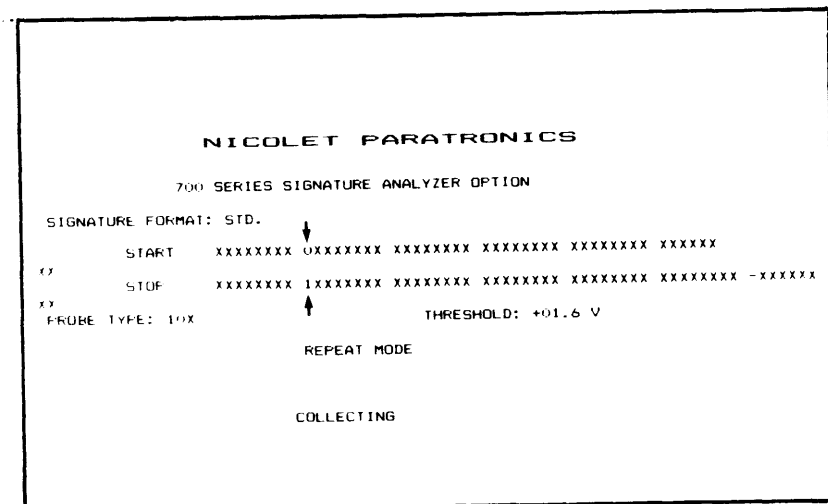


Figure 1-15. Simple 1-bit Signature Analyzer menu.

When the start and stop signal is more than one bit wide, you can develop signatures of more complex events. For example, if the start word were a subroutine call address and the stop word were a subroutine exit address, a unique signature of that subroutine would be developed by using the LSB of the address as the input serial data stream. In this manner, software bugs or revisions can be readily identified. See Figure 1-16.

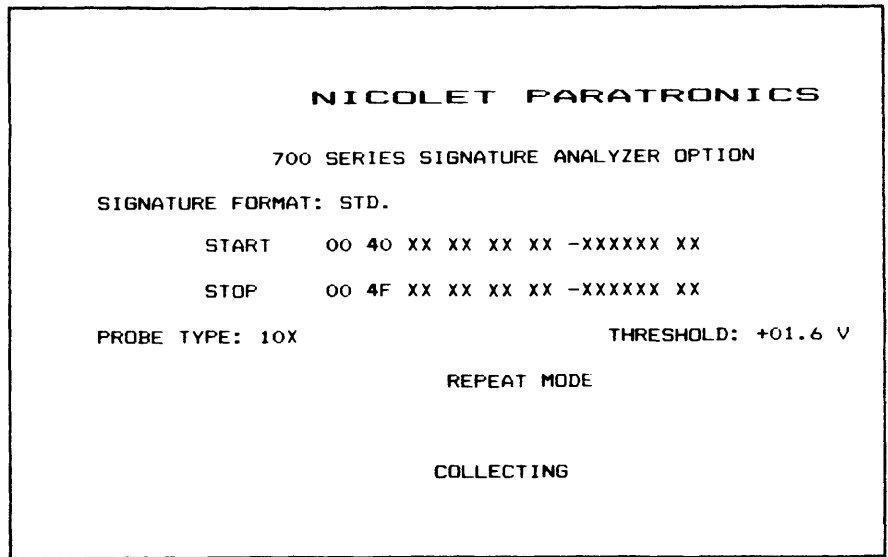


Figure 1-16. Signature Analyzer menu for developing software signatures.

In all cases, the algorithm used develops the same 4-digit signature as other industry-standard signature analyzers.

1.11 ACCESSORIES ENHANCE THE NPC-700

1.11.1 THE MODEL 70 FOR BIDIRECTIONAL SERIAL TESTING

In many applications, the ability to troubleshoot an RS-232 interface is an essential part of the system testing task. The Model 70 Serial Communications Probe offers you a cost-effective way of adding bidirectional serial testing capability to your NPC-700. Simply insert the Model 70's TEE connector between your computer and its peripheral and use the NPC-700's state analyzer and serial menu to capture, analyze, edit and transmit serial information. See Figure 1-17.

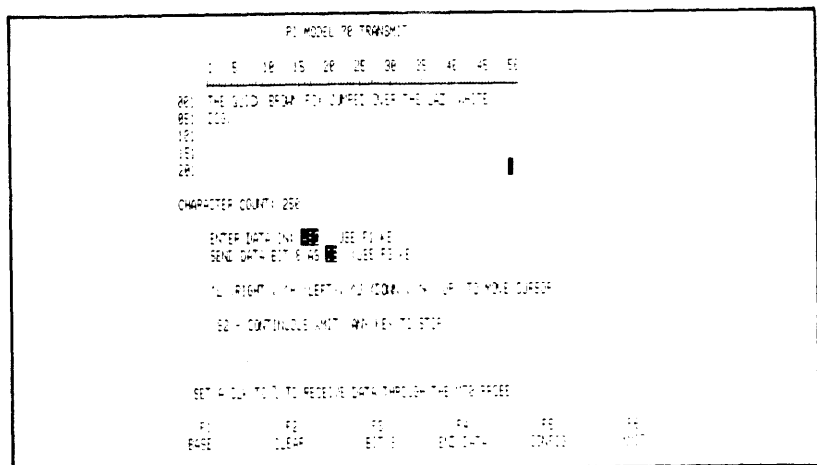


Figure 1-17. The Model 70 Serial Transmit Menu.

LED's on the Model 70 Serial Probe provide a real-time indication of the activity on the RECEIVE, TRANSMIT, and STATUS pins. Baud rates from 50 to 19.2 Kbaud are switch-selectable on the probe. Other switches allow you to define pins 2 and 3 as RECEIVE or TRANSMIT, as well as define the number of stop bits, parity, and word length. See Figure 1-18.

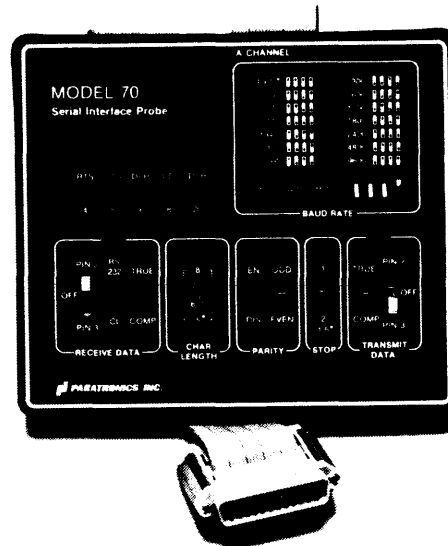


Figure 1-18. The Model 70 Serial Probe.

The Model 70 Serial Probe only requires 16 state channels. Depending on which NPC-700 you're using, there are as many as 32 extra state channels--plus 16 timing channels and the other internal test functions--all of which are available to support additional measurements in your system.

As an example, let's assume you have a peripheral device that is not functioning properly. Is the problem in the computer, in the device, or in the interface itself? With the NPC-700/Model 70 combination, you have all the resources you need to rapidly isolate the problem. Use the RECEIVE and TRANSMIT modes to identify the computer, the peripheral, or the interface as the culprit. Then use the additional state, timing or waveform resources to isolate the underlying hardware or software fault.

1.11.2 DEDICATED MICRO-PROCESSOR PROBES SPEED SOFTWARE DEBUG

8-BIT AND 16-BIT DEDICATED PROBES FOR POPULAR MICRO-PROCESSORS

As the software used in system design grows, a logic analyzer and a dedicated probe with real-time disassembly capabilities become invaluable tools for analysis and debug. Real-time disassembly gives the user the ability to look at software execution at full system speeds. The data collected are then displayed in easy-to-read assembly language mnemonics.

1.11.2.1 QUICK CONNECTION

Using a pre-wired IC clip, each dedicated probe offers quick, reliable connection to the microprocessor-under-test. A low-profile "piggy-back" socket is also available for applications where space is at a premium.

All necessary signals for clocking data into the NPC-700 are automatically generated by circuitry inside the probe. The data collection usually includes address, data, and control and status lines. One example of a dedicated probe is shown in Figure 1-19.

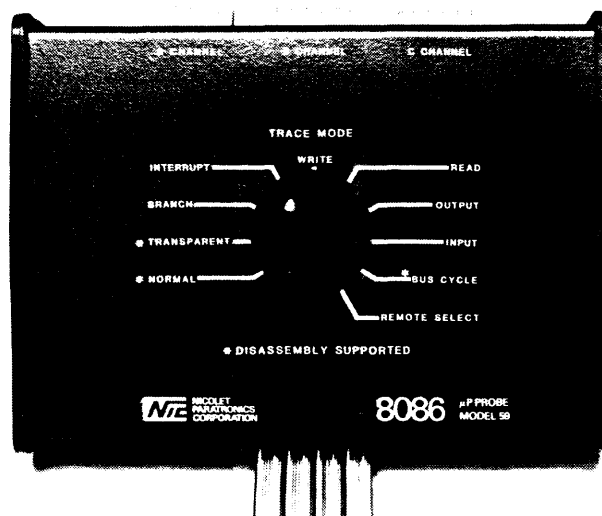


Figure 1-19. The dedicated probe for the 8086.

1.11.2.2 POWERFUL ANALYSIS CAPABILITIES

Used in conjunction with the dedicated probes, the NPC-700's powerful clock and trigger qualifiers can greatly simplify the analysis of your program's execution. With these qualifiers you can collect specific MPU operations or a combination of operations from among the following: MEMORY READ/WRITE, I/O, OPCODE FETCH, MPU STACK READ/WRITE, and BRANCHES. See Figure 1-20.

MAIN	TRIG	0000	F3	OPCODE FETCH(TAIL)
	+001	0000	FF	REFRESH
LDC: TRIG	+002	0001	JP	0040H
	+003	0001	FF	REFRESH
SIG: E3D7	+004	0002	40	OPERAND FETCH
36E5	+005	0003	00	OPERAND FETCH
DBD3	+006	0040	LD	SP,23FCH
	+007	0002	FF	REFRESH
	+008	0041	FC	OPERAND FETCH
	+009	0042	23	OPERAND FETCH
	+010	0043	LD	IY,00A0H
	+011	0003	FF	REFRESH
	+012	0044	21	OPCODE FETCH(TAIL)
	+013	0004	FF	REFRESH
	+014	0045	A0	OPERAND FETCH
	+015	0046	00	OPERAND FETCH
	+016	0047	SET	7, (IY+55H)
	+017	0005	FF	REFRESH
	+018	0048	CB	OPCODE FETCH(INCOMPLETE)
	+019	0006	FF	REFRESH
	+020	0049	55	OPERAND FETCH
	+021	004A	FE	OPCODE FETCH(TAIL)
	+022	00F5	21	DATA READ

Figure 1-20. Typical disassembly example.

Also, unwanted microprocessor activities, such as WAIT states and REFRESH cycles, can be purged from the data collection. Once set up, all modes are switch-selectable at the probe and require no further changes to the NPC-700's menu. Additional software analysis capabilities include triggering on one operation, such as a BRANCH, and collecting a different operation such as memory READS.

All of the NPC-700's 8-bit and 16-bit dedicated probes allow true, real-time disassembly of the instructions being executed in relationship to the actual operands and memory addresses being generated. Furthermore, NPC's dedicated probes do not interfere with the real-time operation of the target MPU.

1.11.2.3 ADVANCED ANALYSIS CAPABILITIES

NPC's dedicated probes require 32 to 48 state channels depending on the probe type. As shown below, this leaves the remaining channels and test functions for an in-depth analysis of events on or off the microprocessor bus:

Dedicated Probe Type*	Channels Required by Probe	Logic Analysis Channels Remaining	
		NPC-748	NPC-764
8080, 8085, Z80, 6809E, 6800, 6802	32 State	16 Timing	16 Timing plus 16 State
8086 68000	48 State	N/A	16 Timing

For example, let's say you're using the timing section to monitor a hardware interrupt subsystem and the state section to monitor the MPU. By linking the two sections, you can capture the interrupts while simultaneously disassembling the associated interrupt handling subroutine.

* Contact Nicolet Paratronics Corporation for the availability of dedicated probes not listed.

1.11.3 GENERAL PURPOSE PROBES SIMPLIFY INTERCONNECTION

Each NPC-700 is supplied with a complete set of probes and terminators. Three probe types are available: the Model 51A, the Model 80 and the Model 87. Each Model 51A accommodates 16 state channels, two qualifiers and an external clock. Each Model 80 probe accommodates 8 timing channels, 1 qualifier and a clock. The Model 87, which is actually a set of 5 dual-channel probes, is offered as an alternative to the Model 80. Whereas the Model 80 is perfectly suitable for monitoring signals that are physically in the same general area of your system, the Model 87 is ideal for the analysis of large systems where monitoring points can be as far as 8 feet apart. See Figures 1-21 and 1-22.

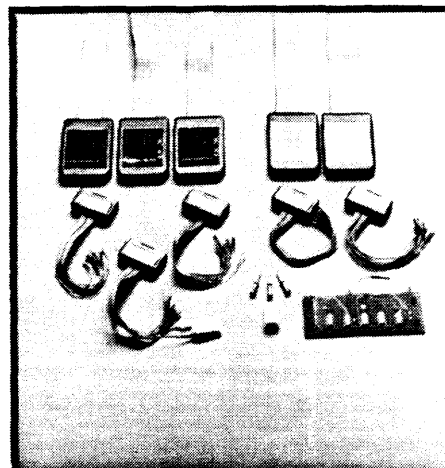


Figure 1-21. Standard probes and accessories.



Figure 1-22. Optional Model 87 probe set. (Replaces Model 80.)

When the optional test and measurement functions are installed, such as the waveform and counter timer/signature analyzers, a Model 90 X1/X10 probe is provided.

For all probes, compatible terminators are included which are color-coded and labeled for easy identification. The state and timing probe terminators interface with IC clips, wire-wrap pins, and spring-loaded miniature grabbers.

A summary of the general-purpose probes available with each NPC-700 analysis system is provided below:

	State Analyzer	Timing Analyzer	Waveform Analyzer	Counter-Timer/ Signature Analyzer
NPC-748	2 ea. Model 51A	2 ea. Model 80 or 2 ea. Model 87*	1 ea. Model 90	Same as Waveform Analyzer
NPC-764	3 ea. Model 51A	2 ea. Model 80 or 2 ea. Model 87*	1 ea. Model 90	Same as Waveform Analyzer

*The Model 87 is optional and consists of five, 5-foot long, dual-channel timing probes for the analysis of large systems.

**1.12 THE NPC-764 AS A
GENERAL-PURPOSE
COMPUTER**

The NPC-764 departs from conventional test equipment by giving you full access to its internal microcomputer for automatic control, test storage, post-processing, and general-purpose computing applications.

The NPC-764 uses an 8085 CPU and two operating systems: one operating system is in ROM and supports all test and measurement functions; the other operating system, CP/M, resides on disk and supports all computer-related activities. The two operating systems are designed to interact during automatic testing, test storage, and post-processing of collected data.

**1.12.1 THE NPC-764'S
ARCHITECTURE**

The NPC-764 incorporates a bus-oriented microcomputer architecture. The internal 8085 CPU, the CRT, the keyboard, the memory and I/O subsystems, as well as the logic analyzer and other measurement functions, all interface to the CPU bus as shown in Figure 1-1.

Since the analyzer's control programs are contained in 48K of ROM, all test and measurement functions are totally independent of the CP/M operating system and the disk drive.

On the other hand, all general-purpose computing tasks use the integral disk drive and the CP/M operating system as the primary interface. As shown in the figure, programs are downloaded into 48K of user RAM for execution. It's important to note that this user RAM is separate from the real-time data acquisition memories associated with the state and timing analyzers.

The integral floppy disk drive uses a 5¼", single-sided, double-density, soft-sectored, 100 TPI diskette, with 300 Kbytes of formatted capacity. There is a connector at the rear of the NPC-764 which allows you to expand the disk memory system to over 1 megabyte using an external, dual-drive expansion chassis.

The 9" CRT display is memory-mapped and uses an 80-character by 25-line format. A 256-character display generator provides full ASCII and graphics character sets.

1.12.2 CP/M ENHANCES THE NPC-764'S USEFULNESS

CP/M was chosen for the NPC-764 since it is the single most commonly used operating system. There are hundreds of reasonably priced applications programs on the market offering higher level languages, engineering and scientific packages--even word processing. Such programs can be ordered from Lifeboat Associates. (See Section 1.5.)

Through CP/M, the user can also generate his or her own programs. These programs can be written in assembly language; or using a high-level-language such as CBASIC*, FORTRAN, PASCAL, PL/1--to name a few.

A printer driver program is available that enables the NPC-764 to provide both text and graphics hardcopy on an Epson MX-80A printer. (Many of the illustrations in this Section 1.0 were derived using this program.)

1.12.3 POST-PROCESSING ANALYZER DATA

Prior to the NPC-764, the logic analyzer user had to be satisfied with whatever data manipulation and display modes the manufacturer provided. However, through CP/M, post-processing programs can be written to support special applications. These programs can be generated in assembly language, CBASIC, or other languages.

As a simple example, an applications program can be written to transfer previously collected data between the NPC-764's state and timing sections. In this manner, you can display data collected by the state analyzer in a timing diagram format; or you can display state and timing data side-by-side on the same screen in the state format of your choice. Other post-processing examples include: searching for certain patterns or sequences in the data collection, generating custom or non-standard data displays such as histograms, and implementing special algorithms such as computing the Fourier transform of a previously-digitized analog waveform.

The commands that allow the transferring of data between the various analyzer memories and the 48K of user RAM are an integral part of the standard, NPC-764 I/O software described in the following pages. Besides allowing the manipulation of data within the NPC-764, these commands also enable you to transfer normal or post-processed data to external GPIB or RS-232 devices.

*CBASIC is included with each NPC-764.

1.12.4 THE NPC-764 AS A LOW-COST DEVELOPMENT SYSTEM

During the hardware and software integration phase of a project, a logic analyzer can be indispensable for uncovering subtle bugs. If the bugs are hardware-related, they can generally be fixed on the spot. However, if they are software-related, you may have to save up (and work around) enough bugs to make it worthwhile to halt the integration process and go back to the main development system to generate corrected code.

By adding a stand-alone emulator and a PROM programmer to your NPC-764, software bugs, too, can be fixed as they occur. This can be a more efficient and effective way of performing software integration since the debugging process can proceed without the delays often associated with having to access the main development system. Both the emulator and the PROM programmer interface to the NPC-764's RS-232 port.

With the above set-up, software changes can be quickly implemented and tested in your system. When the changes are proved to be successful, new PROMs can be programmed.

Emulators for most of the common microprocessors are available from Applied Microsystems Corporation.* Each emulator is supplied with a diskette containing NPC-764-compatible software.

When using the NPC-764 as a low-cost MDS, it is recommended that you incorporate a single or dual-disk drive expansion chassis into the set-up. This will give you additional program storage and the ability to rapidly duplicate your diskettes.

1.12.5 AUTOMATED TESTING AND REMOTE CONTROL

A unique I/O software package allows the NPC-764 to be a central part of a powerful, IEEE-488 automated test system. This same software, which is standard on all NPC-764's, permits RS-232 MASTER/SLAVE operation in remote control applications. Additionally, the I/O software allows you to readily place the NPC-764 under the control of another computer.

1.12.5.1 SINGLE I/O MENU SPEEDS GPIB AND RS-232 SET-UPS

The I/O software is an integral part of the ROM-based test and measurement operating system and does not require the CP/M operating system during manual operation. The associated I/O CONFIGURATION MENU incorporates all of the fields necessary to manually set up the NPC-764 for GPIB and RS-232 operation. The menu consists of 4 quadrants: GPIB, RS-232, INPUTS, and OUTPUTS. See Figure 1-23.

* Applied Microsystems, 5020 148th Avenue N.E., P.O. Box 568, Redmond, WA 98052;
TELEX: 152471; PHONE: 800/426-3925 or 206/882-2000

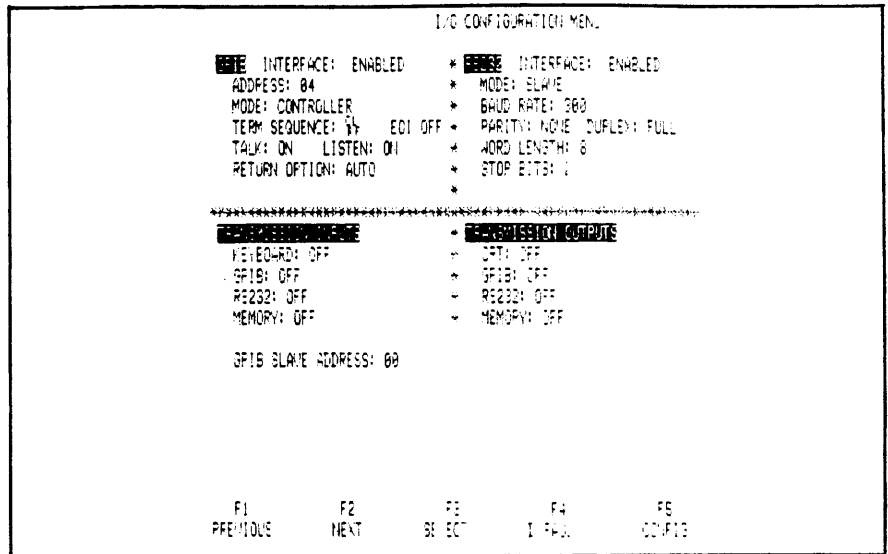


Figure 1-23. I/O CONFIGURATION MENU.

On the GPIB quadrant of the I/O CONFIGURATION MENU, the NPC-764 can be set up as a CONTROLLER or a LISTENER/TALKER. On the RS-232 quadrant the instrument can be a MASTER or a SLAVE. In the TRANSMISSION INPUTS quadrant, data can come from the keyboard, from the GPIB or RS-232 ports, or from various analyzer memories. Then, using the TRANSMISSION OUTPUTS quadrant, you can send data to the CRT, to the various analyzer data memories, or out the GPIB or RS-232 ports. As a simple example of the use of the I/O CONFIGURATION MENU, consider an automatic test application that first required the manual exercising of an RS-232 or a GPIB device before running it under program control. By defining the NPC-764's keyboard as the data input, and the NPC-764's CRT as the output from the device under test, you can rapidly verify the integrity of your set-up.

1.12.5.2 GPIB CONTROLLER/ DEVICE APPLICATIONS

When the NPC-764 is the central part of a GPIB-based, automated test system, the CP/M operating system, hosting CBASIC, is employed. Typical GPIB commands are:

ABORT	REQUEST	LOCAL LOCKOUT
GPIB	OUTPUT	CONFIGURE
RESET	ENTER	EOI STATUS
REMOTE	STATUS	SENDER BUS
LOCAL	SET TIMEOUT	TERM SEQ
TRIGGER		

When using these commands, it's important to note that the NPC-764's internal test and measurement functions respond as if they were external devices on the GPIB bus.

Thus, you can add a pattern generator, a DVM, a power supply, and other GPIB-compatible instruments to the NPC-764 and use the same command set for both internal and external functions.

If you already have an IEEE-488 controller, you can incorporate the NPC-764 into your GPIB test set-up as a powerful, LISTENER/TALKER. In this configuration, the NPC-764 will respond to standard GPIB commands from your controller, execute the required test, and transfer the results back.

1.12.5.3 RS-232 MASTER/SLAVE APPLICATIONS

One new application area that is showing considerable promise is remote diagnosis. Using an ordinary terminal and a telephone line, a factory specialist can remotely control the entire operation of an NPC-764. To avoid having to set up another communications link between the local and remote locations, any message typed at one location will appear on the CRT at the other location.

If the ordinary terminal is replaced by an intelligent terminal or a computer, then the NPC-764's functions can be fully automated. In this application, a test can be downloaded to the NPC-764 and the results sent back to the intelligent terminal or computer for processing.

A third possible I/O configuration involves using one NPC-764 as a MASTER and a second NPC-764 as a SLAVE. Here, the NPC-764 functioning as the MASTER can execute a test on System A while the SLAVE NPC-764, following the commands of the MASTER, is running a test on System B. The MASTER can then command the SLAVE to report its test results. (One of the example programs provided with your NPC-764 actually performs this MASTER/SLAVE application.)

SECTION 1.0

INTRODUCTION

1.13 SUMMARY: THE NPC-700 ELECTRONIC WORKBENCH

The table below summarizes how the NPC-700 performs test and measurement tasks previously requiring a bench full of sophisticated and expensive test gear.

Table 1-1. The NPC-700 Electronic Workbench.

		STATE ANALYZER	TIMING ANALYZER	SERIAL ANALYZER	WAVEFORM ANALYZER
INPUTS:	NPC-764:	48 DATA, 3 CLOCKS, 8 QUALIFIERS	16 DATA, CLOCK, QUALIFIER	8 DATA, 8 CONTROL	SINGLE CHANNEL (10 uV/DIV. to 20 V/DIV.)
	NPC-748:	32 DATA, 2 CLOCKS, 6 QUALIFIERS			
MAX. DATA RATES		12.5 MHz	100 MHz (8 CHANNELS)	19.2K BAUD RECEIVE/TRANSMIT	50 MHz (6 BIT A/D)
MAX. REAL-TIME MEMORY DEPTH		1000 WORDS	2000 WORDS	1000 CHARACTERS	1000 SAMPLES
MAX. AUX. MEMORY DEPTH		1000 WORDS	2000 WORDS	1000 CHARACTERS	1000 SAMPLES
TRIGGER LEVELS		16	2	16	0%-100%; POS. SLOPE, NEG. SLOPE
DELAYS		AFTER N CLOCKS, NOT ON N CLOCKS, BEFORE N CLOCKS, ON N CLOCKS, OCCURS N TIMES: 0 N 9,999			USES TIMING ANALYZER TRIGGERING/ DELAY CIRCUIT
MAX. PRETRIGGER		999 WORDS	1800 WORDS	999 CHARACTERS	900 SAMPLES
DISPLAY		HEX, OCT, DECIMAL, BINARY, ASCII IN ANY MIX	16 TIMING; HEX, OCT, DECIMAL, BINARY, ASCII	CHARACTERS--ASCII; CONTROL--BINARY, HEX, ETC.	ANALOG WAVEFORM, (SOFTWARE SMOOTHED OR UNSMOOTHED)
LINKAGES		STATE TO TIMING, WAVEFORM	TIMING TO STATE, SERIAL, WAVEFORM	SERIAL TO TIMING, WAVEFORM	WAVEFORM TO TIMING, SERIAL, STATE

COUNTER/TIMER	
MODES	FREQ., PERIOD, TOTAL, INTERVAL
MAX. INPUT FREQ.	100 MHz
INPUT SOURCES	SCOPE PROBE (1X/10X) OR STATE ANALYZER WORD RECOGNIZERS

SIGNATURE ANALYZER	
FORMATS	HP AND HEX
INPUT	SCOPE PROBE (1X/10X)
GATE	STATE ANALYZER WORD RECOGNIZERS

I/O AND COMPUTING FACILITIES*		
IEEE-488	DEVICE	CONTROLLER
RS-232	SLAVE	MASTER
CP/M	T&M PROCESSING	GENERAL-PURPOSE COMPUTER

*THE NPC-764 INCORPORATES FULL I/O AND COMPUTING FACILITIES; WHILE THE NPC-748 INCORPORATES IEEE-488 DEVICE FUNCTIONS ONLY.

The following pages provide the details associated with each test function. If you have any questions or comments please contact our Applications Engineering Department.

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2.0 PREPARATION FOR USE

2.1 INCOMING INSPECTION

Look for obvious shipping damage such as dents or punctures. Also, check for loose PC boards, IC's, or other components.

NOTE: If shipping damage has occurred, **SAVE THE ORIGINAL CONTAINER** and notify the shipper immediately.

2.1.1 BASIC EQUIPMENT

The following items form the basis of every shipment:

1. NPC-764 or NPC-748 Logic Analysis System:

Includes accessory case and handle.

2. Probes:

The following probes are standard:

(a) State Probes: For NPC-764--3 each Model 51A, 16-channel variable threshold state probes; for NPC-748--2 each Model 51A.

(b) Timing/State Probes: 2 each Model 80, 8-channel variable threshold timing probes.

3. Probe Terminators:

For connection to the system-under-test. The following probe terminators are standard:

(a) Model 52-1: 1 provided with each Model 51A probe.

(b) Model 82-1: 1 provided with each Model 80 probe.

NOTE: A package of 30 "ball clips" are included with the terminators.

4. Miscellaneous Items:

- 3-Wire Line Cord
- Logic Analyzer Test Card
- Operator's Manual
- CP/M Software Documentation (NPC-764 only)*
- CP/M Diskettes (2) (NPC-764 only)

2.1.2 OPTIONAL EQUIPMENT

1. Optional Probes:

(a) Model 87 High-Performance Timing Probe Set. High input impedance, high-speed hybrid probes useful for making timing measurements on circuit elements up to 8 feet apart.

*Includes CBASIC Reference Manual and Lifeboat Catalog.

(b) Model 70 Serial Interface Probe. For testing RS-232C/TTY interfaces.

(c) Dedicated Microprocessor Probes. One or more dedicated probes with disassembly for the 8080, 8085, 6800, 6802, 6809E, Z-80, 8086, and 68000 MPU's.

2. Waveform Analyzer Option:

For recording analog signals using high-speed (50 MHz) A/D conversion and software smoothing techniques. Includes one Model 90 (10X/1X) probe, if probe not otherwise provided with another option.

3. Counter-Timer/Signature Analyzer Option:

For performance monitoring and troubleshooting of the system-under-test. Includes one Model 90 (10X/1X) probe, if probe not otherwise provided with another option.

2.2 VERIFICATION OF ORDER

The original purchase order and the shipper should be checked against the equipment received. If an item which appears on the Purchase Order is missing and is not on the shipper as a back-ordered item, immediately notify Nicolet Paratronics or one of our local sales offices.

**2.3 BASIC ANALYZER
VERIFICATION TESTS**

2.3.1 EQUIPMENT HANDLING

The NPC-700 utilizes a modular construction in a rugged mechanical package. However, the operating environment temperature should be kept between 10° and 45°C (50° - 133°F). Also, avoid use or storage of the equipment in dusty, smokey, or high static electricity areas. For the NPC-764, as with other disk-based equipment, careful handling of disks and the disk drive is recommended.

**2.3.2 PROGRAMMABLE AC
VOLTAGE SELECTOR
CARD**

WARNING

BEFORE APPLYING POWER TO THE NPC-700, MAKE CERTAIN THAT THE PROGRAMMABLE AC VOLTAGE SELECTOR CARD, WHICH PLUGS INTO THE AC LINE CORD CONNECTOR/FUSE ASSEMBLY AT THE REAR OF THE NPC-700, IS INSERTED IN THE POSITION CORRESPONDING TO THE LINE VOLTAGE BEING USED; OTHERWISE, SERIOUS DAMAGE TO THE INTERNAL SWITCHING POWER SUPPLY MAY OCCUR.

The voltage selector card, shown in Figure 2-1, has three nominal voltage options: 100V, 115V, and 230V. The line voltage selected is visible without removing the card.

SECTION 2.0

PREPARATION FOR USE

If it is necessary to change the line voltage, carefully grasp the card edge with a pair of long-nose pliers and reorient it so that the proper voltage appears with the card fully inserted.

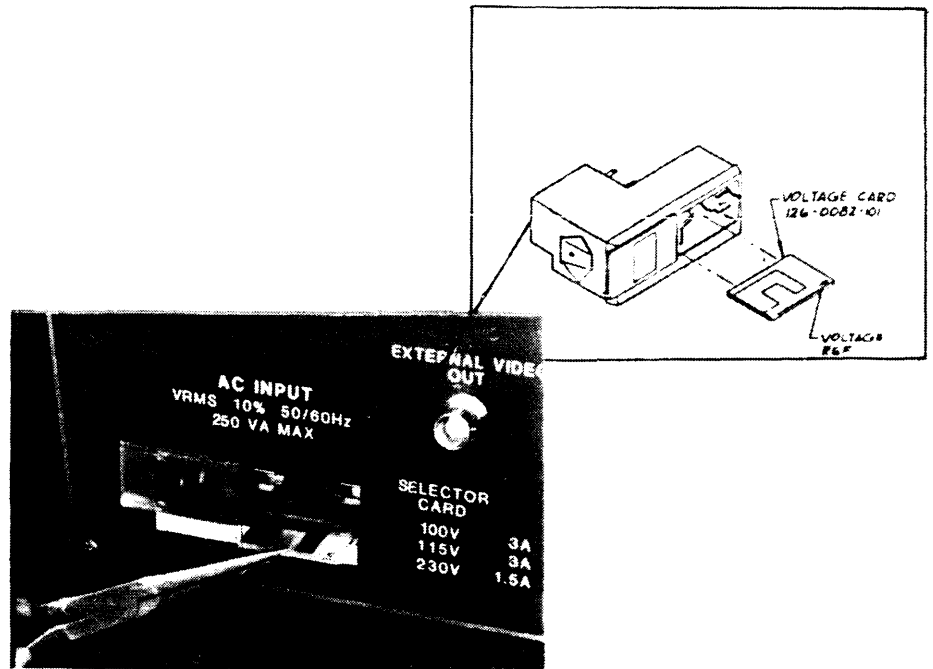


Figure 2-1. Programmable AC voltage selector.

2.3.3 BASIC STATE ANALYZER COLLECTION

1. Insert a Model 51A State Probe into the A (STATE) input on the left side of the NPC-700. Make sure the plastic key on the probe connector is facing up.
2. Plug the probe head into the A side of the Logic Analyzer Test Card. Make sure the probe switches are set to **TTL** and **TRUE**.
3. Turn power on using the power switch in the right rear side of the NPC-700.* If the unit is cold, wait up to 30 seconds for the CONFIGURATION LIST to appear. The half-intensity cursor should be located at the top of the list.
4. Press the F6 key, labeled **COLLECT** on the CRT, to take an arbitrary state data collection. The resulting display should contain twenty hexadecimal words whose four most significant digits contain values somewhere between 0000 and 00FF. The rest of the digits should be all F's. See Figure 2-2. See Section 6.2.1 for additional state data collection examples.

***NOTE:** The NPC-700 will emit a short beep upon power up or pressing **RESET**. This beep signifies that the NPC-700 has been reset.

MAIN	TRIG	00C0FFFFFFFF
	+001	00C1FFFFFFFF
LOC: TRIG	+002	00C2FFFFFFFF
	+003	00C3FFFFFFFF
SIG: 0B1F	+004	00C4FFFFFFFF
100F	+005	00C5FFFFFFFF
100F	+006	00C6FFFFFFFF
	+007	00C7FFFFFFFF
	+008	00C8FFFFFFFF
	+009	00C9FFFFFFFF
	+010	00CAFFFFFFFF
	+011	00CBFFFFFFFF
	+012	00CCFFFFFFFF
	+013	00CDFFFFFFFF
	+014	00CEFFFFFFFF
	+015	00CFFFFFFFFF
	+016	00D0FFFFFFFF
	+017	00D1FFFFFFFF
	+018	00D2FFFFFFFF
	+019	00D3FFFFFFFF

Figure 2-2. Arbitrary state data collection.
(Your data will probably differ.)

2.3.4 BASIC TIMING DATA COLLECTION

1. Turn power off or press **RESET** for approximately 2 seconds to reinitialize the NPC-700.
2. Insert a Model 80 Timing Probe into the A (TIMING) input on the left side of the NPC-700. Make sure the plastic key on the probe is facing up. (You can leave the state probe connected to the analyzer.)
3. Plug the probe head into the B side of the Logic Analyzer Test Card. (There are no switch settings on this probe.)
4. Turn power on. After the **CONFIGURATION LIST** appears, move the cursor down to the **16-CHANNEL TIMING** mode by pressing the **F4** key labeled **SEL DOWN**.
5. Press **F6**, the soft-key labeled **COLLECT**, to take an arbitrary timing data collection. This collection should contain sixteen high or low logic levels as shown in Figure 2-3. Note the momentary prompting message: **WARNING - PLUG IN B PROBE**. (Ignore this message for this basic check.) Note also that the 100 nS sampling rate of the NPC-700 at power on is much faster than the clock rate of the CMOS test card. Therefore, few--if any--logic transitions will be captured. See Section 6.2.2 for additional timing collection examples.

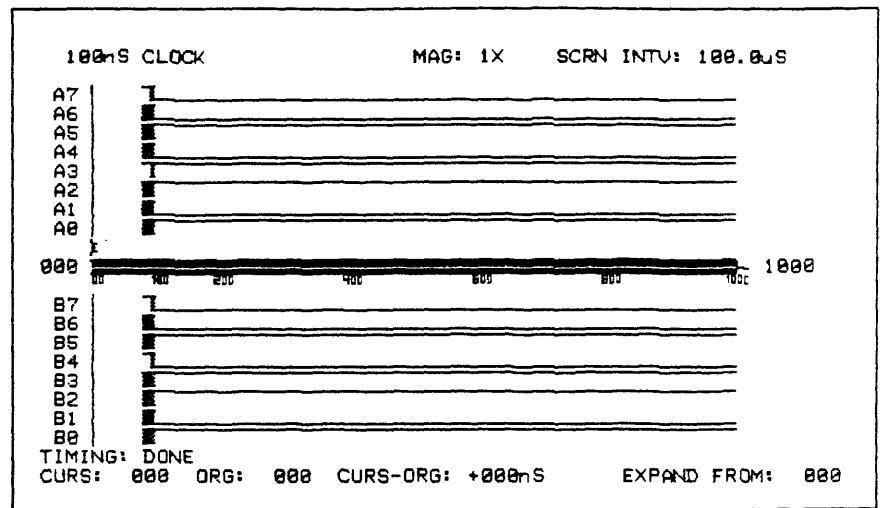


Figure 2-3. Arbitrary timing data collection.
(Your data will probably differ.)

2.3.5 BASIC WAVEFORM AND COUNTER-TIMER/SIGNA- TURE ANALYZER COLLECTIONS (Option Must Be Installed)

1. Press **F5**, the soft-key labeled **CONFIG**. The **CONFIGURATION LIST** should appear.
2. Using **F4**, the **SEL DOWN** key, step the cursor down to the **WAVEFORM** mode.
3. Press the **COLLECT** key. Since the Model 90 (10X/1X) scope probe is not connected and there is no input signal, the waveform display will contain only a baseline as shown in Figure 2-4. (If the Waveform Option is not installed, the display will not contain the baseline.) See Section 6.2.3 for additional waveform collection examples.
4. Repeat Steps 1 and 2 except step to the **COUNTER/TIMER** mode. Press the **F1** key. Since no input signal is present, the readout inside the display window should be all zeroes. (If this option is not installed, the display window will be blank.) See Section 6.2.4 for additional examples.
5. Repeat Step 4 except step down to the **SIGNATURE ANALYZER MODE**. Since no input or gating signals are present, there won't be any meaningful display. (This test verifies the presence of the menu only.) See Section 6.2.5 for additional examples.

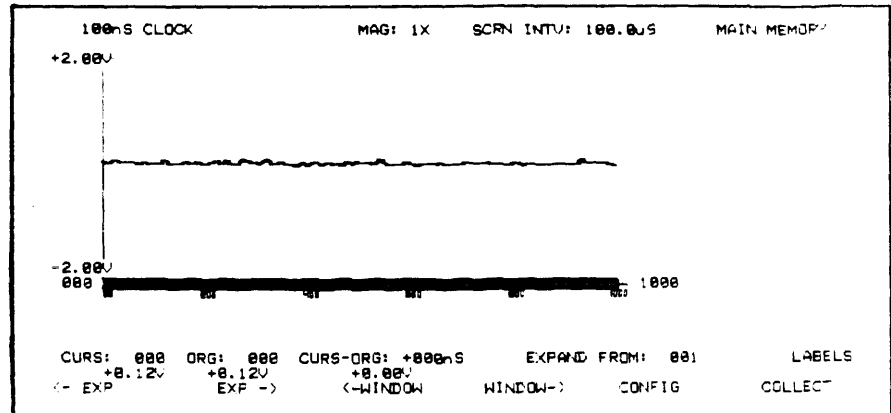


Figure 2-4. Waveform display without an input signal.

2.3.6 SCREEN ADJUSTMENT

If it is desired to adjust CRT screen brightness and contrast, use the following procedure:

1. Press the red **RESET** key for approximately two seconds as an alternate way to obtain the CONFIGURATION LIST. Then press the **F1** key labeled **STATE** to display the state menu.
2. Adjust the **BRIGHTNESS** and **CONTRAST** controls at the left of the CRT to accommodate ambient lighting conditions. Make sure the adjustments provide adequate contrast between the half-intensity and full-intensity characters.

2.3.7 50 Hz/60 Hz CRT FRAME RATE SELECTION

If the CRT display appears shifted up or down, it is probably because the setting of the **CRT FRAME RATE** switch on the Processor Board does not correspond to the line frequency being used. Figure 2-5 shows the location and settings of the **CRT FRAME RATE SELECT** switch.

SECTION 2.0

PREPARATION FOR USE

FRAME RATE SELECT SWITCH

The dip switch is accessed by first switching off the AC power and then removing the top cover by loosening the two quarter-turn fasteners on the rear of the cover. Note that the card cage hold-down strap may have to be removed to change the switch setting. Turn AC power on to check frame positioning and reverse the setting of S8, if necessary.

CRT Frame Rate Select

50 Hz
60 Hz

S8

OFF (Down)
ON (Up)

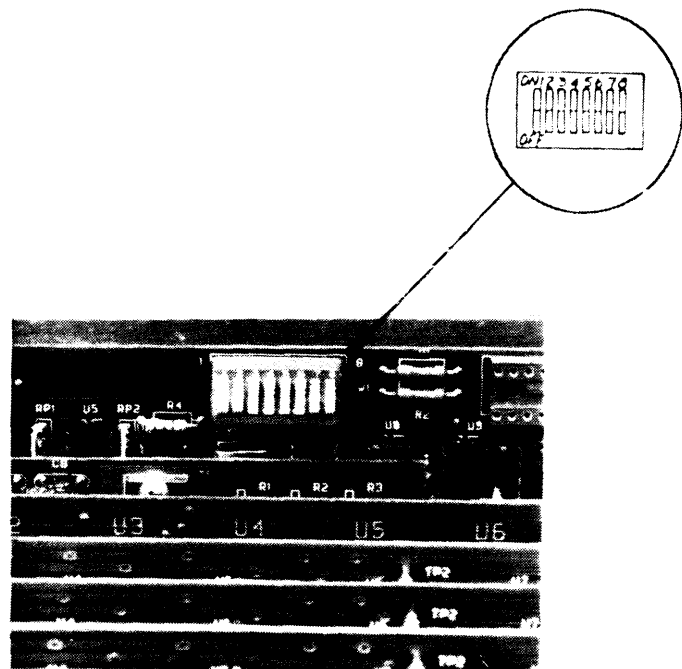


Figure 2-5. CRT FRAME RATE SELECT switch on Processor Board.

2.3.8 DISK SUBSYSTEM (NPC-764)

The diskette should be kept inside its paper protective envelope when not in use. Note that the recording medium of the diskette is contained within a sealed plastic jacket. **DO NOT ATTEMPT TO REMOVE THE PLASTIC JACKET.**

To insert the diskette into the disk drive, first remove the diskette from the paper envelope. Notice the large, circular opening in the center of the diskette, the long oval READ/WRITE head opening, and a square WRITE PROTECT notch along one edge of the diskette.

DISKETTE INSERTION

To insert the diskette, orient the plastic jacket so that the WRITE PROTECT notch is at the bottom and the label faces towards the CRT. See Figure 2-6.

Carefully slide the diskette into the vertical opening on the drive until no additional movement in the direction of insertion is possible. Now mount the diskette to the drive by pulling the drive door handle to the right until the handle latches, firmly clamping the diskette onto the drive motor spindle. An interlocking mechanism prevents the door from closing if the diskette is not properly loaded.

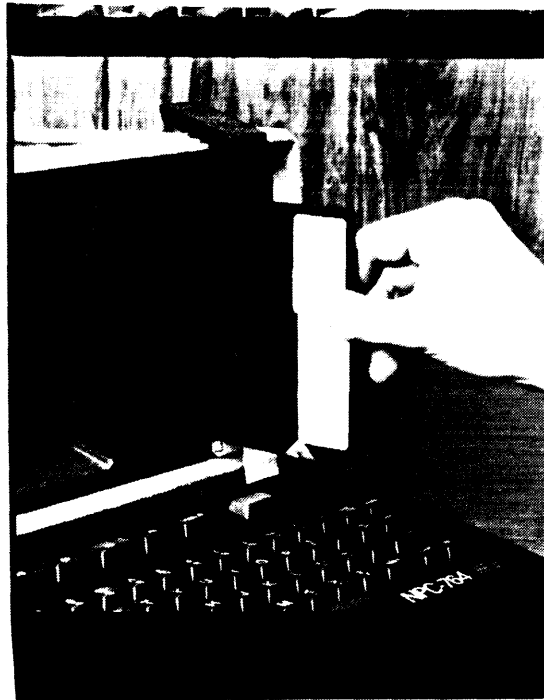


Figure 2-6. Diskette orientation for loading.

DISKETTE REMOVAL

Removal of the diskette requires a releasing of the latching mechanism. A partially ejected position is acceptable during power-up/down of the NPC-764.

WARNING

To protect the data on the diskette, it is good practice **NEVER** to interrupt power to the NPC-764 when a diskette is fully mounted on the drive.

2.3.8.1 WRITE PROTECT FEATURE AND ORIENTATION

The WRITE PROTECT notch, when covered, protects the contents of the diskette from accidental alteration. A microswitch detects the presence or absence of a notch in the side of the diskette. When the open notch is sensed, writing is allowed. When the notch is not sensed (covered with a tab), writing is inhibited and a status signal informs the disk controller that a WRITE PROTECT condition exists.

2.3.8.2 CONTAMINATION AND STORAGE OF DISKETTES

In order to protect the integrity of your data, menus, and programs, your diskettes should be handled with care. The following recommendations should be observed:

1. Always dismount the diskette from the drive before power-up/down of the NPC-764 to avoid possible loss of information on the diskette.
2. Return the diskette to its storage envelope whenever it is removed from the disk drive.
3. Keep diskettes away from magnetic fields since exposure to such fields can affect the data.
4. Do not write on the plastic jacket with a lead pencil or ball-point pen. Use a felt-tip pen or a stick-on label.
5. Smoke, heat and ashes from cigarettes can damage a disk.
6. Do not expose diskettes to heat or sunlight.
7. Never remove a diskette from its plastic jacket.
8. Do not touch or attempt to clean the diskette surface since abrasions may cause loss of magnetized oxide and data.
9. Replace the paper storage envelopes when they become worn, cracked, or distorted.

2.3.8.3 ADJUSTMENTS

The disk drive motor is part of a servo-controlled loop and is independent of changes in line voltage and line frequency; therefore, no speed adjustment is necessary.

2.3.8.4 OPERATIONAL CHECK OF THE DISK SUBSYSTEM

1. If power was off, turn power on and load a CP/M diskette as described in Section 2.3.8; otherwise, call the CONFIGURATION LIST.
2. When the CONFIGURATION LIST is displayed, press the **ESC** (escape) key to exit the analysis mode and enter the CP/M mode. (The red LED on the disk drive will illuminate.)
3. Wait until a header and the CP/M prompt: **A >** appears. Next type **DIR** (directory) and **RETURN** to see the programs resident on the disk. A typical directory is shown in Figure 2-7. See Sections 9.0, 10.0, and 11.0 for additional CP/M information and examples.

2.3.8.5 DISKETTE

The NPC-764 uses a 5/8 inch, single-sided, double-density flexible disk drive. When buying additional diskettes, specify that the diskettes be certified for double-density operation. Nicolet Paratronics' P/N 112-0503-0001 is Dyan's model 204/1D, DN800439 Soft-Sector, Single-Side, Double-Density, 96-100 tracks or an equivalent.

A few words of caution regarding diskettes: ALWAYS make a back-up copy. ALWAYS buy good quality diskettes. Many people have learned the hard way that these 2 rules are well worth the expense. Losing the only copy of a diskette, or losing a file due to accidental erasure, contamination, or poor quality media can be an expensive situation to correct.

```

A>DIR
A: CPM      COM : PIP      COM : XSUB     COM : ED       COM
A: ASM      COM : DDT      COM : LOAD     COM : STAT     COM
A: DUMP     COM : SUBMIT   COM : PRINT    COM : DSKTEST  COM
A: FORMATS  COM : LASAVE   COM : LARECALL COM : PAMTEST  COM
A: K/BDTEST COM : COPS      COM : LADISA   COM : LPRINT   COM
A: BIOS764  ASM : PROM764  ASM : CRUN2    COM : CFU1238  COM
A: CBAS2    COM : XREF      COM : D488     : D8888
A: D8885    : D8886     : DZ88        : D8888
A: D8883E   : D8888E     : GF18        BAS : LADTSC    EAS
A: LA      COM : RS232EX  INT : RS232E>  $$$ : RS232E>  882
A: RS232EX 881 : GP18E>     INT : GP18E>   BAS : RS232E>  EAS

```

**Figure 2-7. Typical CP/M diskette directory.
(Your listing may differ.)**

2.3.9 SELF-TEST

If you have difficulty operating the NPC-764 in the analysis or CP/M modes, built-in self-tests can help isolate the problem. Although these tests are not exhaustive, they can provide the NPC-764 operator with a high degree of confidence that various sub-systems are operating properly. See Appendix B for a description of these self-tests. (The NPC-748 can only perform the Processor Self-Test since the other tests are on diskette.)

**2.3.10 NOTES CONCERNING AIR
FILTER MAINTENANCE**

In order to assure proper internal cooling of your NPC-700, you should clean the air filter periodically. The frequency of the cleaning will depend on the operating environment; however the filter should be cleaned at least once every six months.

The filter is located on the upper-rear-corner of the analyzer and is held in place by three brackets attached with phillips drive screws. To remove the filter, loosen and remove the knurled thumbnut which holds the bottom bracket in place. Remove the bracket from the threaded stud. Slide the filter down and out to remove it.

Clean the filter with soap and water, a mild solvent or with air. Dry the filter and depress the inner surface gently so that the filter material bulges outward, away from the seam in the filter frame. Replace the filter in the two upper brackets, making certain that the seam in the frame is facing the back panel, and the bulge in the filter material is facing outward. Replace the lower bracket and tighten the thumbnut "finger-tight."

CAUTION: Failure to keep the filter clean could result in excessive heat generation and equipment malfunction which may void the warranty.

2.4 RETURN OF EQUIPMENT

If the unit must be sent back to the factory or an authorized service center for any reason, contact Nicolet Paratronics or your local sales office for instructions and a RETURN AUTHORIZATION NUMBER.

NOTE: EQUIPMENT RETURNED TO THE FACTORY OR SERVICE CENTER **WITHOUT PRIOR AUTHORIZATION** CANNOT BE ACCEPTED. (BY CONTACTING US FIRST, WE MIGHT BE ABLE TO SOLVE YOUR PROBLEM AND SAVE YOU A LOT OF TROUBLE.)

2.4.1 SUGGESTIONS CONCERNING RETURN OF EQUIPMENT

If you have authorization to return equipment, use the original shipping container and packing material, if possible. Also, it is always a good idea to insure any equipment shipped.

If the subassembly, board, PROM, diskette, or other component responsible for the problem can be identified (with or without the help of our application engineers), it is often more convenient, and certainly less costly, to return just the faulty item rather than the entire instrument.

IMPORTANT NOTE

U.S. CUSTOMERS SHOULD CONTACT OUR CUSTOMER SERVICE DEPARTMENT FOR ASSISTANCE AT:

(800) NICOLET (Toll-Free outside California)
(415) 490-8300 (California)

OUR CUSTOMER SERVICE ENGINEERS CAN ANSWER QUESTIONS AND AUTHORIZE RETURN OF EQUIPMENT.

INTERNATIONAL CUSTOMERS SHOULD DEAL DIRECTLY WITH THEIR LOCAL NICOLET PARATRONICS SALES AND SERVICE CENTER.

Regardless of how you proceed, please send a description of the problem along with the faulty item. If you return the entire instrument, be sure and **INCLUDE ALL PROBES**.

SECTION 3: KEYBOARD

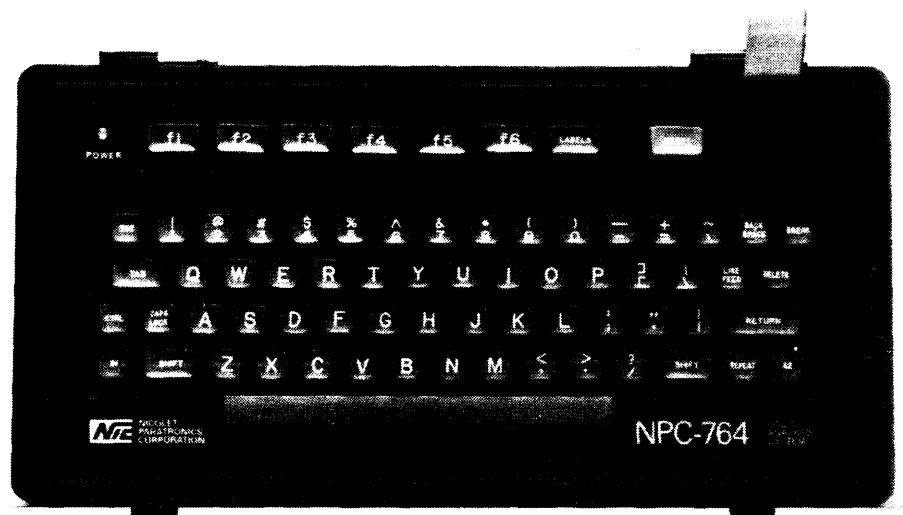
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3.0 KEYBOARD**3.1 KEYBOARD
ARRANGEMENT**

Figure 3-1 shows the keyboard of the NPC-700. This keyboard allows the operator to send data to the computer and to make data entries or menu changes in the logic analyzer and other analysis sections of the instrument. Most of the keys are the same as they are on an ordinary terminal or typewriter; i.e., they type the same alphanumeric characters. This familiar arrangement permits faster programming and menu set-ups without learning dedicated keys.

You cannot damage the computer or the logic analyzer by typing on the keys.

The keyboard assembly folds up conveniently over the CRT and floppy disk drive for their mutual protection during transport.



**Figure 3-1. The NPC-700's detachable, folding keyboard.
(NPC-764 shown.)**

Whenever you turn on the NPC-700, allow 5-30 seconds for the CRT to warm up. The NPC-700 is in the Analyzer Mode upon power up and the initial display is a list of analysis functions. For the NPC-764, in order to use the keyboard for computer operations, you must escape the Analyzer Mode by pressing the **ESC** key. Then you can load a CP/M diskette as described in Section 2.3.8.4. After the CP/M version number appears, you should then see a line and a blinking reverse video block cursor in the upper left-hand corner (the home position) of the screen.

The cursor identifies where the next character can be written. The screen contains 2000 normal character positions or 25 lines of 80 characters each. Only one character can occupy a character position at any given time and it will remain there until it is erased or replaced. Upon pressing the **ESC** key, the processor clears the screen by placing spaces in all character positions.

The keyboard consists of single-pole/single-throw switches in a matrix that is scanned by keyboard-encoding hardware located in the keyboard. The hardware is periodically polled by the software.

3.1.1 ALPHABETIC KEYS

The keyboard incorporates the standard 26 letters of the alphabet in lower-case or upper-case as determined by the **SHIFT** key. Use the **CAPS LOCK** key to obtain upper-case letters only.

3.1.2 NONALPHABETIC KEYS

The nonalphabetic keys are those with double markings. These include the numbers 0 through 9, punctuation marks, and special characters. The lower marking is generated when the **SHIFT** key is released, while the upper marking is generated with the **SHIFT** key down. The **CAPS LOCK** key will not shift these keys.

3.2 NONDISPLAYABLE KEYS

In addition to the standard typewriter keys, the following eleven function keys are included in the keyboard:

RETURN -- Moves the cursor to the first character position. If the cursor is already at the first character position, it remains there. **RETURN** is also called "carriage return" (CR). An automatic line feed is included in the **RETURN** function.

LINE FEED -- Moves the cursor down one line. If the cursor is at the bottom line, a **LINE FEED** causes it to remain there, but all of the data on the screen moves up one line. Data on the top line are lost as they are scrolled up and off the screen.

SPACE BAR -- Causes the cursor to move one character position to the right. If you depress the **SPACE BAR** when the cursor is at the right end of a line, the cursor will remain there since neither a carriage return nor a line feed is generated.

BACK SPACE -- Moves the cursor one space to the left. If the cursor is at the start (left end) of a line, it will not move when you depress the **BACK SPACE** key.

DELETE -- Causes the last character entered to be cancelled.

TAB -- Moves the cursor to the next tab stop (eight character spaces) to the right. Using columns numbered from 1 through 80, the tab stops are fixed at 9, 17, 25, 33, 41, 49, 57, 65, and 73. If the cursor is at a character position 73 through 79, it will only move one character position to the right each time you depress the **TAB** key. If the cursor is at character position 80, it will not move.

ESC (Escape) -- In a general sense, causes the software to enter and exit special modes. For the NPC-764, **ESC** accesses the CP/M mode. **ESC** can be used with other keys in the CP/M mode.

REPEAT -- When you hold this key down, along with another key, it will repeat the function of the other key as long as both keys are held down. The repeat rate is approximately 50-characters per second. (Note: Newer NPC-700's incorporate an **AUTOREPEAT** keyboard.)

BREAK -- When you select this key, it generates a continuous space and is generally used to tell the computer that you wish to interrupt program execution. With the Configuration List displayed, the **break** key initiates PROCESSOR SELF-TEST. See Appendix B.

S1, S2 -- These two keys are additional special keys that function according to prompts in the logic analyzer menus.

CTRL -- This key is held down while you push one of the other keys to send control codes to the processor. See Section 7.1.1 for ASCII control code definition.

3.3 SPECIAL KEYS (F1-F6, LABELS, RESET)

3.3.1 F1-F6

There are six software-directed ("soft") keys below the CRT that are automatically labeled on the screen by software.

3.3.2 LABELS

Depressing the **LABELS** key causes a prompting message to appear on the right-hand side of the CRT.

The prompting message is dependent on the analysis mode in use and lists the keys that can be selected to alter menus, change display formats, and save or recall data.

3.3.3 RESET

The red **RESET** key returns the NPC-700 to the initial power-on condition: processor RAM is cleared and the CONFIGURATION LIST appears on the CRT. A beep indicates completion of **RESET**.

NOTE: **RESET** will erase all menu parameters and auxiliary memory data.

In order to avoid causing an accidental **RESET**, the key must be held down for approximately two seconds.

3.4 SPECIAL COMMANDS

3.4.1 LASAVE (NPC-764) (LOGIC ANALYZER DATA SAVE)

This command is used to save on disk, all of the analyzer data in the NPC-764's state and timing/waveform auxiliary memories and the associated menu parameters. To use this command after making a data collection, return to the CONFIGURATION LIST with the **CONFIG** key and press the **ESC** key. The NPC-764 will exit to the CP/M operating system. Then type:

LASAVE FILENAME (RETURN)

A file will be created on the disk called **FILENAME** and will contain analyzer set-up information and associated data. (You can use any name for your file, 8 letters or less.) When file creation is complete, the NPC-764 will return to the analyzer configuration.

The following information is contained in a 12 Kbyte file saved on the diskette:

- Main State Menu
- Auxiliary State Menu
- Auxiliary State Data
- State Display Parameters
- Main Timing Menu
- Auxiliary Timing Menu
- Auxiliary Timing/Waveform Data
- Timing/Waveform Display Parameters
- Main Waveform Menu
- Counter-Timer Menu
- Signature Analyzer Menu
- Serial Transmit Menu
- I/O Menu
- Auxiliary Waveform Menu

NOTE: Main state data and main timing/waveform data are not automatically saved. Thus, if you want to save main memory data, it's necessary to first transfer it to the corresponding auxiliary memory by pressing the **S (SAVE)** key, prior to entering the CP/M operating system and executing the LASAVE command.

**3.4.2 LARECALL
(LOGIC ANALYZER (NPC-764)
DATA RECALL)**

This command is used to recall analyzer set-up and data from a file created previously with LASAVE. To use this command, return to the CONFIGURATION LIST and press ESC. Then type:

LARECALL FILENAME (RETURN)

The information in the selected file will be recalled back into the analyzer's auxiliary memory. At this point, the NPC-764 will be configured exactly the same as it was when the file was originally created, including all the menu parameters and the associated data, except for the main state data and the main timing/waveform data.

NOTE: See Section 6.3.1 for examples of disk storage and recall functions. See Section 11.12 for an example of how to use the CP/M SUBMIT utility together with LASAVE and LARECALL to automate tests.

Also, see Section 10.4 for a description of how to implement LASAVE and LARECALL from a CBASIC program.

3.4.3 AUTO COLLECT

Press **CTRL** and **C** simultaneously to activate an automatically repeating data collection mode. Press any ASCII key to stop.

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4.0 INTERCONNECTION

As described in this section, the NPC-700 can be interfaced to the system-under-test in a variety of ways. The probe and probe terminator the user chooses depends on his particular application and the mechanical configuration of the system-under-test. Figures 4-1 and 4-2 identify the standard probes and terminators. For special terminators, contact Nicolet Paratronics or your local sales office.

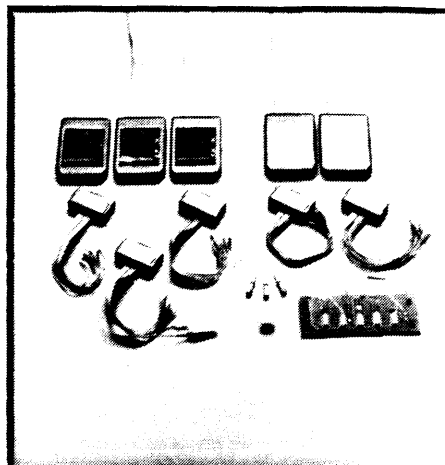


Figure 4-1. Standard Probes and terminators. (The NPC-748 has one less 16-channel state probe and terminator.)

CAUTION

ALWAYS CONNECT THE GROUND LEAD OF THE PROBE FIRST TO INSURE THAT THE ANALYZER AND SYSTEM-UNDER-TEST BOTH SHARE A COMMON GROUND POTENTIAL. THIS MINIMIZES THE POSSIBILITY OF DAMAGE DUE TO STATIC, FLOATING GROUND, OR AC COUPLING OF THE INPUT SIGNALS. ALSO, THE PROBE GROUND LINE SHOULD ALWAYS BE REMOVED LAST.

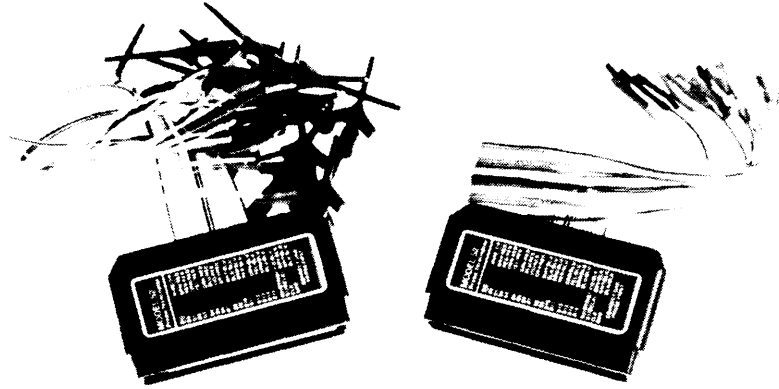


Figure 4-2. Terminator detail.

4.1 MECHANICALLY INTER-FACING THE MODEL 51A PROBES

The Model 51A State Probe interfaces to the system-under-test using a probe terminator, or a PC board edge connector (test port) incorporated into systems specifically designed to support troubleshooting with an NPC analyzer. See Figure 4-3 and Section 4.10.

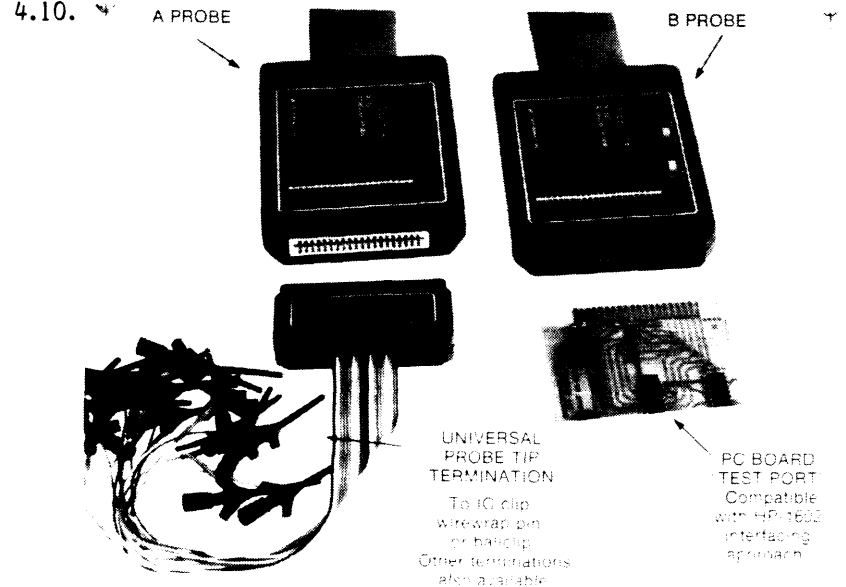


Figure 4-3. Probe interfacing methods.

4.1.1 THE MODEL 52 PROBE TERMINATOR

The Model 52 probe terminator is plugged into the Model 51A probe when it is desirable to take advantage of the flexible interconnection capability offered by the flying leads. Each terminator has color-coded leads providing the following functions: data inputs, qualifiers, external clock, and ground. Figure 4-4 is a reproduction of the color-code definitions provided on the Model 52 probe terminator label.

A photo of the Model 52 probe terminator leads is shown in Figure 4-5. Note that each flying lead is terminated in a gold-plated Berg connector, which readily mates with wirewrap pins, IC clips, and removable ball clips.


MODEL 52 Probe Terminator	
SIG	WIRE/TIP
D0	BRN/RED
D1	RED/RED
D2	ORN/RED
D3	YEL/RED
D4	GRN/RED
D5	BLU/RED
D6	VIO/RED
D7	GRY/RED
D8	WHT/BLU
D9	BLK/BLU
D10	BRN/BLU
D11	RED/BLU
D12	ORN/BLU
D13	YEL/BLU
D14	GRN/BLU
D15	BLU/BLU
Q _{TRIG}	VIO/BLK
Q _{CLK}	GRY/BLK
CLK	WHT/BLK
GND	BLK/BLK
CONNECT GND PROBE FIRST	
 PARATRONICS INC.	

Figure 4-4. The Model 52 color codes.

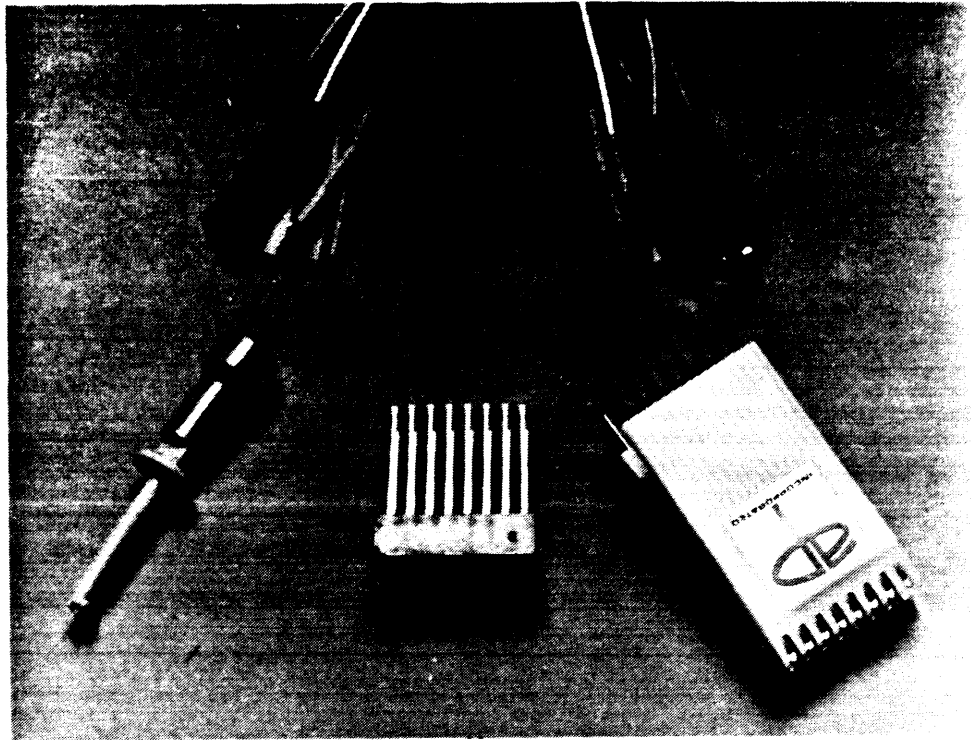


Figure 4-5. Using "Universal Pin Connectors" (Berg Connectors) for interfacing to system-under-test.

4.1.2 ELECTRICALLY INTERFACING THE MODEL 51A PROBE

CAUTION

IT IS IMPORTANT TO OBSERVE THE FOLLOWING MAXIMUM INPUT VOLTAGE RANGE TO AVOID DAMAGE TO THE PROBES:

MODEL 51A : $\pm 25V$

ALSO, ALWAYS CONNECT THE BLACK GROUND PROBE WIRE FIRST AND REMOVE IT LAST.

4.1.2.1 INPUT SIGNAL AND LOADING CHARACTERISTICS

In order to ensure reliable data collection, the user should be familiar with the input loading and threshold characteristics of the Model 51A as described in the following section.

SECTION 4.0

INTERCONNECTION

4.1.2.2 SIGNAL LEVELS FOR THE MODEL 51A STATE PROBE

The Model 51A state probe features a continuously variable threshold between $\pm 6V$. The threshold value is adjusted by setting a potentiometer (having a slotted shaft) accessible through a hole in the probe case. A voltage monitoring point (with respect to ground) is also provided next to the threshold potentiometer so that accurate threshold values can be established.

NOTE: THE VOLTAGE AT THE MODEL 51A'S MONITORING POINT IS 50% OF THE ACTUAL THRESHOLD VALUE. THUS, A MONITORING POINT VOLTAGE OF +1.0 VOLTS WILL YIELD AN ACTUAL THRESHOLD VALUE OF +2.0V.

The following table provides additional information about the input characteristics of the Model 51A:

<u>Characteristic</u>	<u>Value</u>
Minimum Signal Swing	500mV
Threshold Accuracy	$\pm 100mV$
Input Resistance	44Kohms
Input Capacitance	15pF

SPECIAL LOGIC FAMILIES

The Model 51A probe incorporates a resistance divider in front of the input sense amps so that resistor ratios can be tailored to accommodate different logic swings such as those associated with low-level logic or even 24V and 48V logic circuits. (Consult the factory about special threshold versions.)

TRUE/COMPLEMENT

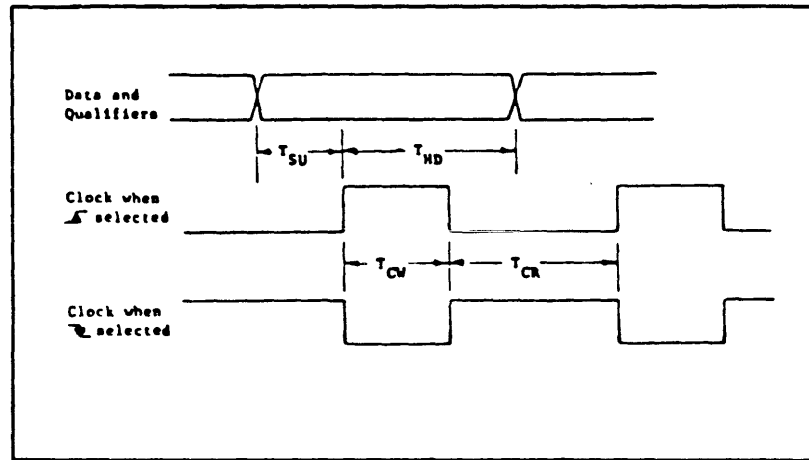
The Model 51A features a fixed threshold switch which permits the user to set the probe to a TTL threshold value of +1.6V $\pm 100mV$ without disturbing the variable setting.

The Model 51A also incorporates a **TRUE/COMPLEMENT** switch. With the **TRUE** position selected, all input data and qualifier signals at least 200mV below the threshold will be logic ZERO's. In the **COMPLEMENT** position, the logic sense is reversed. **NOTE THAT THE INPUT CLOCK IS NOT AFFECTED BY THIS SWITCH.**

Since the logic state portion of the analyzer is functionally split into 16-channel data input groups, various mixes of threshold settings and logic senses can be used to accommodate a variety of system requirements.

4.1.3 INPUT SIGNAL REQUIREMENTS FOR STATE DATA COLLECTIONS

Figure 4-6 illustrates the input signal timing requirements for the Model 51A probe. If the user is sure that the system-under-test meets or exceeds the minimum values specified, the NPC-700 will reliably collect data; otherwise, data collection errors can occur.



<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>MODEL 51A</u>
T_{SU}	Data and Qualifier Set-Up	20 nS
T_{HD}	Data and Qualifier Hold	0 nS
T_{CW}	Active Clock Pulse Width	20 nS (min)
T_{CR}	Recovery Pulse Width	30 nS (min)

(All times referred to threshold crossing)

MAXIMUM CLOCK FREQUENCY:

Model 51A: 15 MHz

Figure 4-6. Model 51A probe timing requirements.

4.2 MECHANICALLY INTER-FACING THE MODEL 80 PROBES

In a manner identical to the Model 51A, the Model 80 probe interfaces to the system-under-test using a probe terminator or a PC board edge connector (test port). See Figure 4-7 and Section 4.10.

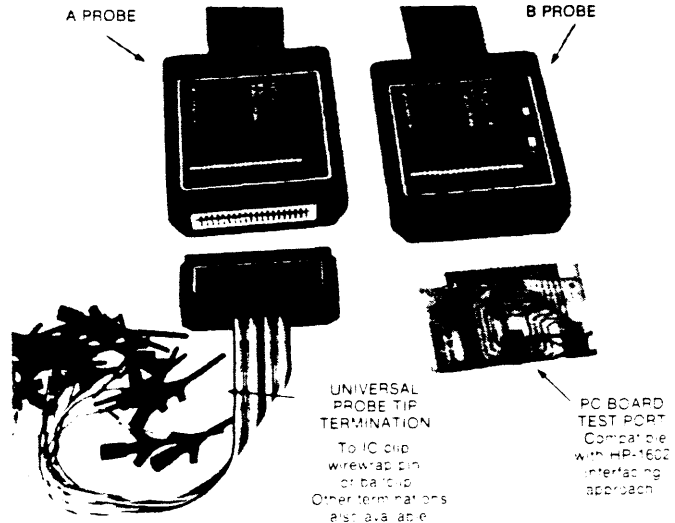


Figure 4-7. Probe interfacing methods.

4.2.1 THE MODEL 82 PROBE TERMINATOR

The Model 82 probe terminator is plugged into the Model 80 probe when it is desirable to take advantage of the flexible interconnection capability offered by the flying leads. Each terminator has color-coded leads providing the following functions: data inputs, qualifiers, external clock, and ground. Figure 4-8 is a reproduction of the color-code definitions provided on the Model 82 probe terminator label.


MODEL 82 Probe Terminator	
SIG	WIRE/TIP
D0	BRN/RED
D0-GND	RED/BLK
D1	ORN/RED
D1-GND	YEL/BLK
D2	GRN/RED
D2-GND	BLU/BLK
D3	VIO/RED
D3-GND	GRY/BLK
D4	WHT/RED
D4-GND	BLK/BLK
D5	BRN/BLU
D5-GND	RED/BLK
D6	ORN/BLU
D6-GND	YEL/BLK
D7	GRN/BLU
D7-GND	BLU/BLK
Clk	VIO/BLU
Clk-GND	GRY/BLK
CLK	WHT/BLU
CLK-GND	BLK/BLK
CONNECT GND PROBE FIRST	
	

Figure 4-8. The Model 82 color codes.

4.2.2 ELECTRICALLY INTERFACING THE MODEL 80 PROBE

CAUTION

IT IS IMPORTANT TO OBSERVE THE FOLLOWING MAXIMUM INPUT VOLTAGE RANGE TO AVOID DAMAGE TO THE PROBES:

MODEL 80 : $\pm 100V$

ALSO, ALWAYS CONNECT THE BLACK GROUND PROBE WIRE FIRST AND REMOVE IT LAST.

4.2.2.1 INPUT SIGNAL AND LOADING CHARACTERISTICS

In order to ensure reliable data collection, the user should be familiar with the input loading and threshold characteristics of the Model 80 as described below.

4.2.2.2 SIGNAL LEVELS FOR THE MODEL 80 PROBE

The Model 80 probe features a keyboard-selectable threshold between -6.4V and +6.35V in 50mV increments.

In the 16-channel mode, the threshold of each 8-channel Model 80 probe is individually adjustable.

In the 8-channel modes, separate thresholds can be set for channels 0-3, external clock and qualifier; and channels 4-7.

The following table provides additional information about the input characteristics of the Model 80:

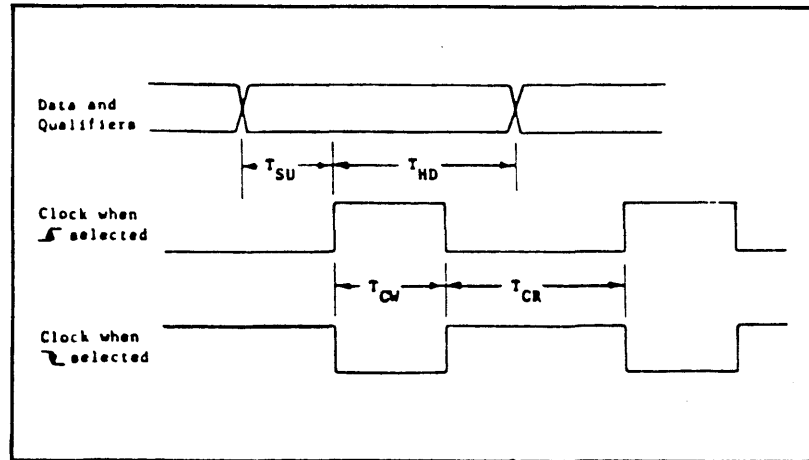
<u>Characteristic</u>	<u>Value</u>
Minimum Signal Swing	500mV
Threshold Accuracy	$\pm 50mV$
Input Resistance	1M
Input Capacitance	6pF
Hysteresis	200mV (menu selectable)

4.2.3 INPUT SIGNAL REQUIREMENTS FOR DATA COLLECTIONS

Figure 4-9 illustrates the input signal timing requirements for the Model 80 probe when using an external sampling clock. If the user is sure that the system-under-test meets or exceeds the minimum values specified, the NPC-700 will reliably collect data; otherwise, data collection errors can occur.

SECTION 4.0

INTERCONNECTION



<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>MODEL 80</u>
T_{SU}	Data and Qualifier Set-Up	5 nS
T_{HD}	Data and Qualifier Hold	10 nS
T_{CW}	Active Clock Pulse Width	10 nS (min)
T_{CR}	Clock Recovery Pulse Width	10 nS (min)

MAXIMUM CLOCK FREQUENCY:

Model 80: 40 MHz (external clock)

Figure 4-9. Model 80 probe timing requirements.

4.2.4 HIGH-PERFORMANCE TIMING PROBES, MODEL 87

The Model 87 High-Performance Timing Probe Set is designed for probing circuits on physically distant hardware such as large mainframe computers, computer peripherals, or a rack of equipment. The Model 87 features five timing probes with 5-foot cables to permit diagnostic probing with up to 8 feet between circuit test points.

The Model 87 consists of:

- One Model 84 High-Performance Timing Probe Expander. Each Model 84 will accept up to 5 Model 85 Timing Probes.
- Five Model 85 High-Performance Timing Probes. Each probe incorporates a hybrid technology FET circuit with input impedance of 1 Meg ohm and 5 pF.
- Five Model 86 Probe Terminators with Berg Connectors.

4.3 WAVEFORM PROBE, MODEL 90

The Model 90 (1X/10X) Waveform Probe interfaces to the system-under-test in the same manner as a scope probe. It is plugged into the rear panel BNC connector labeled **WAVEFORM**.

4.3.1 INPUT CHARACTERISTICS OF THE MODEL 90 WAVEFORM PROBE

The Model 90 Waveform Probe is identical to a scope probe with input impedance of 1M in parallel with 30pF.

4.4 COUNTER-TIMER/SIGNATURE ANALYZER PROBE, MODEL 90

The same probe is used for the Counter-Timer/Signature Analyzer (CTSA) as is used for the Waveform section of the NPC-700. It is, however, plugged into the rear panel BNC connector labeled CTSA.

4.5 SERIAL INTERFACE PROBE, MODEL 70

The Model 70 Serial Interface Probe, shown in Figure 4-10, is a dedicated probe which can be used with the PI-540, PI-648, PI-532, or NPC-700 Logic Analyzers. This probe can be used to record and analyze the operation of asynchronous RS-232, CCITT V.24, and 20 mA current loop interfaces. It can also be used to transmit RS-232 data to the system-under-test. The Model 70 offers the user front panel selection of stop bits, parity, word length, and baud rate. Baud rates are selectable from 50 baud to 19.2K baud. The Model 70 also includes a set of LED's for real-time monitoring of the status lines: CTS, DSR, RTS, DCD, and DTR.

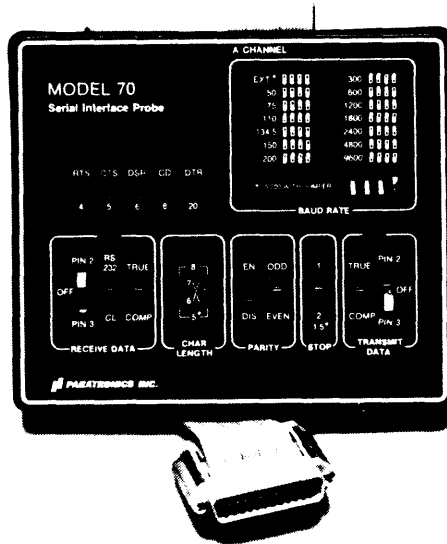


Figure 4-10. The Model 70 Serial Probe.

Connection to the analyzer is made by plugging the Model 70 into the 16 channel A probe port of the logic state analyzer. The remaining logic analyzer probe ports can then be used to monitor additional data channels. Detailed User's Instructions are provided with the Model 70.

4.6 DEDICATED MICRO-PROCESSOR PROBES

The powerful analysis capability of the NPC-700 can be further enhanced with a dedicated microprocessor probe. NPC offers a family of dedicated microprocessor probes that can be used with most NPC analyzers. A typical probe is shown in Figure 4-11.

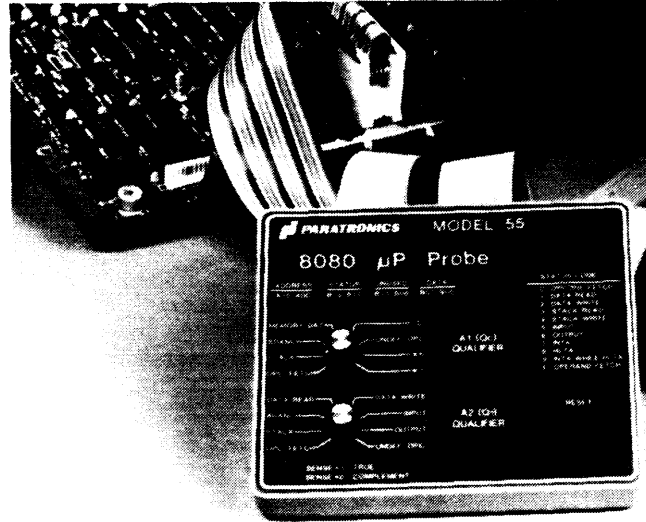


Figure 4-11. Typical Dedicated Probe.

Each dedicated probe offers quick, convenient connection to the microprocessor-under-test because it is terminated with a pre-wired DIP clip. The necessary signals for clocking data into the NPC-700 are automatically generated by the probe. Typically, the data collection includes 16 address lines, 8 data lines, and 8 cycle status lines--as well as user-defined signals. 16-bit microprocessor probes are also available for the NPC-764.

Each dedicated probe utilizes the flexible clock and trigger qualifiers of the NPC-700 to simplify the analysis of program execution. You can use these clock or trigger qualifiers to capture only the specific areas of program flow required to debug a particular software problem.

As shown in Figure 4-12, the disassembly software of the NPC-700 "comments" each line of recorded data with specific cycle status information such as MEMORY READ, MEMORY WRITE, ADD, MOV, I/O, OPERAND FETCH, etc.

MAIN	+049	EOF3	C7	STACK READ
	+050	EOF4	01	STACK READ
LOC: 004E	+051	01C7	F5	OPERAND FETCH
	+052	EOF4	FF	STACK WRITE
SIB: FC43	+053	EOF3	B4	STACK WRITE
D5AB	+054	01CB	3A	OPERAND FETCH
100F	+055	01C9		NOP
	+056	01CA	MOV	M,B
	+057	7000	FF	MEMORY READ
	+058	01CB	FE	OPERAND FETCH
	+059	01CC	IN	PORT: C2H
	+060	01CD	C2	OPERAND FETCH
	+061	01CE	RST	5
	+062	01CF	LXI	B, 16 bit data
	+063	01EF	F1	OPERAND FETCH
	+064	EOF3	B4	STACK READ

Figure 4-12. Disassembly example.

Detailed User's Instructions are provided with each dedicated probe. Contact NPC or your local sales office for the availability of specific microprocessor probes.*

4.7 INTERNAL LINKAGE OF NPC-700

Much of the power of the NPC-700 lies in its ability to trace system problems crossing between measurement domains. The basic concept is to give the user the ability to establish a triggering condition in one measurement domain that is linked to events in another domain. For example, you can set up a simple linkage such as arming the timing section upon the detection of a single address by the state section; or a complex linkage that enables **trigger stack level n** in the state section when the timing section simultaneously detects two events within **t nS** of one another.

4.8 RS-232C INTERFACE (NPC-764)

The serial RS-232C interface for the NPC-764 allows the analyzer to communicate with standard RS-232C and TTY peripherals, such as a teleprinter or keyboard/CRT. This is useful in applications where hardcopy printouts are necessary, or where a video terminal is the primary display medium (such as in a microprocessor development system application). Also, the RS-232C interface can be used to remotely control an NPC-764, or one NPC-764 can use it to control another NPC-764.

***NOTE:** For the NPC-764, the disassembly software for each dedicated probe is stored on a diskette using filenames such as D8085, D8086, DZ80, etc. To call a file, enter CP/M and type: **LADISA DXXXX**. Then display state data and type **1** to use the disassembled mnemonic format. See Section 6.5 for an example. For the NPC-748, disassembly software is in ROM. Type **1** to access this software.

4.9 IEEE-488 GENERAL-PURPOSE INTERFACE CONNECTOR

A GPIB system consists of one active controller and one or more instruments capable of listening or talking to the controller or to each other. The GPIB interface uses a 16-line cable to connect together devices which contain an interface circuit that enables each device to communicate with the rest of the system.

This communication technique is detailed in the IEEE STD 488-1975 specification (revised in 1978). Basically, the GPIB bus consists of 5 lines which perform general interface management, 3 lines for control of data transfers, and 8 data lines. Data and control information are communicated in 8-bit words. Each instrument can be addressed through individual commands. Also, there are universal commands to which all instruments respond. The commands to which a given instrument will respond are determined by the instrument manufacturer.

The NPC-764 can operate as a CONTROLLER, or as a DEVICE. The NPC-748 can only operate as a DEVICE. The commands utilized by the NPC-764 are discussed in Sections 13.0 and 14.0. The NPC-700 incorporates a standard IEEE-488 connector, which provides the interface to other instruments on the bus. The pin-outs for that connector are listed in Figure 4-13.

PIN-OUTS	<u>Contact</u>	<u>Signal Line</u>	<u>Contact</u>	<u>Signal Line</u>
	1	DIO1	13	DIO5
	2	DIO2	14	DIO6
	3	DIO3	15	DIO7
	4	DIO4	16	DIO8
	5	EOI	17	REN
	6	DAV	18	Gnd, (6)
	7	NRFD	19	Gnd, (7)
	8	NDAC	20	Gnd, (8)
	9	IFC	21	Gnd, (9)
	10	SRQ	22	Gnd, (10)
	11	ATN	23	Gnd, (11)
	12	SHIELD	24	Gnd, LOGIC

NOTE: Gnd, (n) refers to the signal ground return of the referenced contact.

Figure 4-13. IEEE-488 connector pin-out list.

4.10 SPECIAL-PURPOSE TEST PORTS AND REAR PANEL CONNECTIONS

4.10.1 DIRECT INTERFACING WITH A TEST PORT

In order to simplify system test, there is a growing trend towards incorporating "test ports" into new product designs. These ports bring out critical monitoring signals and allow analysis equipment, such as the NPC-700, easy access to system operation by directly plugging a Model 51A or Model 80 data probe into compatible PC board edge connectors. Figures 4-14 and 4-15 illustrate the concept and mechanical dimensions of the test port connectors. Note the offset arrangement of the PC board edge fingers which prevents the probes from being inserted incorrectly.

The Models 51A and 80 probes also offer a +5V output which can drive external circuit loads up to 200mA. Note that the +5V output is not brought out on the probe terminator's flying leads in order to avoid the accidental connection to sensitive circuitry in the system-under-test.

4.10.2 TEST PORT DESIGN GUIDELINES

The test port should be defined so that the most important test signals are available for monitoring by the NPC-700. Even though the NPC-700 allows you to monitor a large number of signals at any one time, the designer should consider implementing additional test port connectors if there are a greater number of critical signals in the system-under-test. Then, by moving the NPC-700's probes, the user can readily select signals to monitor from all those available at the test ports. Typical test port signals can include:

- Computer or microprocessor address busses
- Memory and I/O busses
- Output from system sensors
- Inputs to system activators
- Key points in a combinatorial logic network
- Control memory address bus (microprogrammed machine)
- Microcontrol word (microprogrammed machine)

SECTION 4.0

INTERCONNECTION

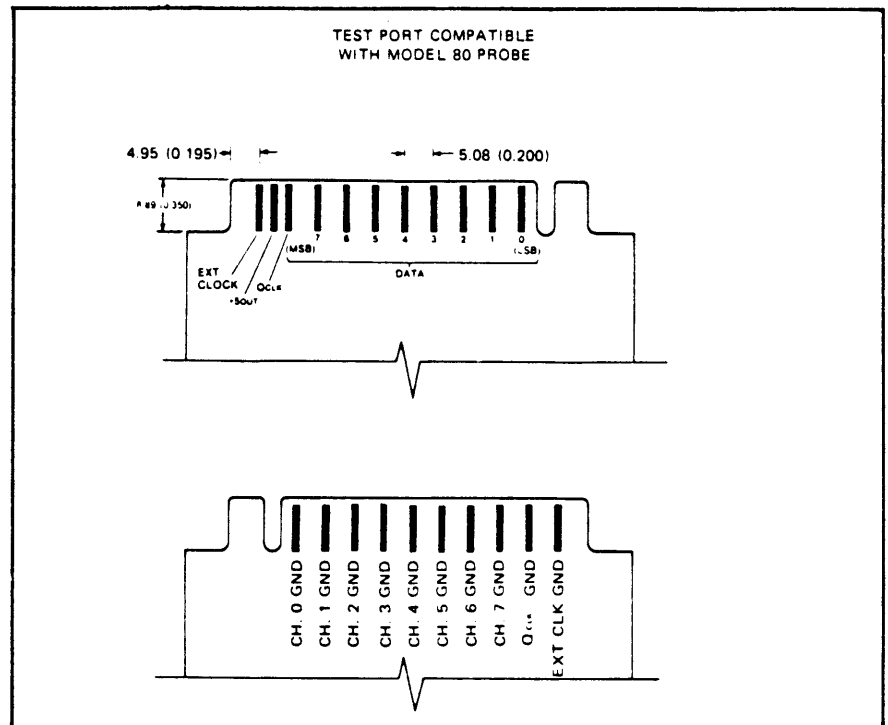


Figure 4-14. Model 80 test port electrical and mechanical definitions.

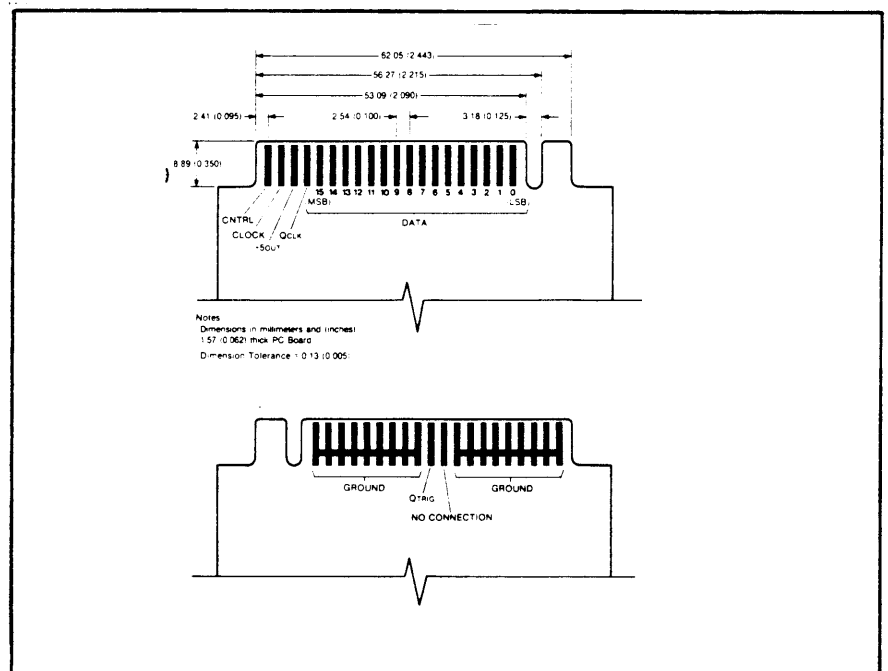


Figure 4-15. Model 51A test port electrical and mechanical definitions.

4.10.3 REAR PANEL CONNECTIONS

Various interconnections are available on the NPC-700's rear panel for interfacing internal test and measurement functions to the user's system-under-test or for triggering additional test equipment. These interconnections include both inputs and outputs and are described below:

4.10.3.1 COUNTER-TIMER/SIGNATURE ANALYZER INPUT

The BNC connector labeled **CTSA INPUT** is the common input for the Model 90 probe when using either the optional COUNTER-TIMER or SIGNATURE ANALYZER portions of the analyzer.

4.10.3.2 EXT VIDEO OUT

This BNC output connector provides a composite video signal to drive the 75-ohm video input of an optional monitor or to directly connect to a video printer.

4.10.3.3 SERIAL RS-232 (NPC-764)

The connector for this interface is used for bidirectional RS-232C serial port operation. RS-232 interface circuitry is located on the NPC-764's RAM/DISK board.

4.10.3.4 ARM AND TRIG OUTPUTS (BNC)

These rear panel BNC connectors provide a real-time, active-low, TTL level when the associated timing or state comparators are detecting valid (matched) input words. See Figure 4-16.

The **ARM** output is from the trigger word recognizer of the state analyzer. When the state analyzer is in the sample mode (collecting data) this output will go low approximately 70 nS following the sampling clock.

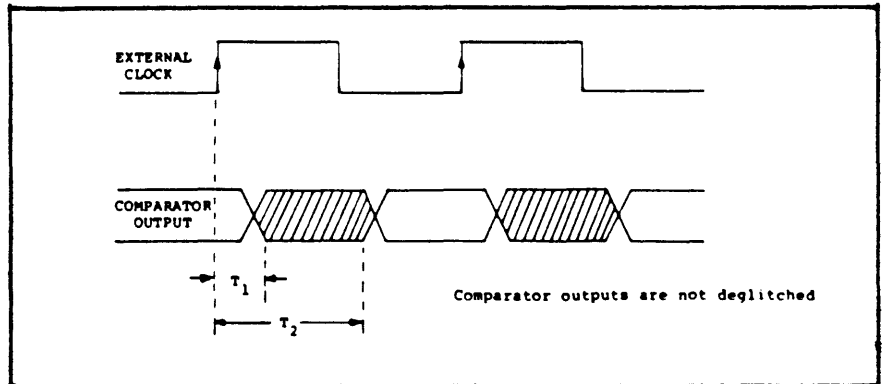
The **TRIG** output is from the trigger word recognizer of the timing analyzer. When the timing analyzer is in the sample mode (collecting data) this output will go low approximately 15 nS following the sampling clock.

EXTERNAL TRIGGERING

These outputs may be used to trigger a scope or another instrument. For continuous output from these BNC's it will be necessary to program menu conditions which will inhibit termination of the collection process. This can be done by specifying conditions which will never occur. (Set a trigger level in the state analyzer to XXX...X and the ARM word in the timing analyzer to XXX...X.)

SECTION 4.0

INTERCONNECTION



T_1 = DLY FROM ACTIVE CLOCK EDGE TO COMPARATOR LEVEL CHANGE

T_2 = DLY FROM ACTIVE CLOCK EDGE TO COMPARATOR STABLE

<u>COMPARATOR</u>	<u>T_1</u>	<u>T_2</u>
ARM OUTPUT (STATE)	20 nS min	150 nS max
TRIG OUTPUT (TIMING)	10 nS min	40 nS max

Figure 4-16. Timing and state comparator outputs.

4.10.3.5 EXT IN

This BNC input connector is used to accept a TTL active-high qualifying signal (clock or trigger) from an external source. (It takes a low-level signal to inhibit this input.) The external source can be linked, for the purpose of expanded triggering, to the internal analyzer sections. For example, this input can be used in combination with the trigger output from another manufacturer's analyzer to expand triggering.

For the **EXT IN** function, the NPC-700 requires a set-up time prior to the selected clock edge of 10 nS. Hold time after the selected clock edge is 20 nS.

4.10.3.6 LINK BNC

This BNC connector is bidirectional. It is normally used to link the NPC-700 to a PI-648 or PI-616 or other NPC-700's using a short BNC cable arrangement. For example, when the **RESTART** word or one of the trigger levels of the NPC-700 contains a "1" in an L bit position, that analyzer is considered the slave in the set-up and its **LINK BNC** connector becomes an input. The companion analyzer is considered the master and its **LINK BNC** connector becomes an output.

When the master analyzer's triggering conditions are completely satisfied, a TTL active-low level signal is output from the **LINK BNC** connector.

**LINK BIT
MASTER-SLAVE
SYNCHRONIZATION**

NOTE: This master/slave relationship is true whether or not the LINK cable is connected. Therefore, do not set the L bit unless the cable connection has been made.)

When the **COLLECT** key is pressed on the master unit, the analyzers perform the following sequence:

1. Set up all analyzer parameters.
2. Release the link control.
3. Enable data collection.

When the **COLLECT** key is pressed on the slave unit, the firmware in the slave unit performs the following sequence:

1. Set up all analyzer parameters.
2. Release the link control.
3. Monitor the link and wait until all linked analyzers have released control.
4. Enable data collection.

Therefore, this mechanism, along with the open collector implementation of the link signal, can synchronize all slaves to the **COLLECT** sequence of the master. For this operation to work correctly, the **COLLECT** keys must be pressed first on all connected slave units; then pressing the **COLLECT** key on the master unit will synchronize all slaves with the master. Because the firmware monitors the link signal only when a link bit is activated, any slave can acquire master status by simply returning any link bits in the trigger or restart words to "X."

Note, however, there can only be one master in the set-up. Also note that if the master/slave relationship is changed, it is not necessary to change the cable connection.

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SECTION 5.0

MENUS AND DISPLAYS

5.0 MENUS AND DISPLAYS

The power and ease-of-use of the NPC-700 Logic Analysis System results from the straight-forward interaction of each menu with the keyboard. In fact, much of this section of the Operator's Manual is contained in the software which directs the user to the proper keystroke sequence. **In general, keyboard entry of commands or data follows these basic guidelines:**

1. The information displayed is always the current state of the analyzer.
2. Parameters that can be modified by the user are identified on the video display screen by an inverse video field.
3. Keyboard entries are placed into the menu at the position identified by a blinking cursor.
4. To move the cursor from one field to the next, use the **PREVIOUS** and **NEXT** keys.
5. To move the cursor within a field, use the **SPACE BAR** and **BACK SPACE** keys.
6. When some menus are displayed, **F3** and **F4** are labeled at the bottom of the CRT as **SELECT** and **DEFAULT**, respectively. Pressing **SELECT** causes each of the available options for that field to be selected. This simplifies the specification of some parameters and allows the user to scroll through all options to select the one most appropriate. Depending on the field, **DEFAULT** returns the field to the power-on condition or moves the cursor to the beginning of the field.
7. For immediate movement of the cursor to a nonadjacent field of interest in the menu, the **DIRECT** keys, **C (CLK QUALIFIER)**, **P (PRETRIG)**, and **T (TRIG)**, can be used. In the menu mode, pressing the **S2** key followed by the **LABELS** key places a series of labels on the right side of the video display which define the function of each **DIRECT** key. Pressing one of the **DIRECT** keys calls the menu and steps the cursor directly to the corresponding field in the menu.
8. If an attempt is made to set up an illegal condition, an error message (in English) flashes on the CRT indicating which keys are appropriate for the current field.
9. In most data entry fields, pressing the **?** key displays a prompting message on the screen indicating the type of data or commands that can be entered into the current field.

HELP (?)

5.1 INITIALIZATION

When the NPC-700 is first switched on, a processor test series can be performed that checks the RAM, ROM, and other subsystems.* As indicated at the bottom of the **CONFIGURATION LIST**, pressing the **BREAK** key activates **PROCESSOR SELF-TEST**.

*It is possible to manually expand this self-test. (See Appendix B.)

5.1.1 CONFIGURATION OPTIONS

To call the CONFIGURATION LIST, after executing PROCESSOR SELF-TEST, press **RESET** for 2 seconds or cycle power. After several seconds, the CONFIGURATION LIST is displayed and the cursor appears at the top of the list. Twelve configurations are possible if the optional Counter-Timer/Signature Analyzer (CTSA) and Waveform boards are installed.

5.1.2 CONFIGURATION LIST DISPLAY

The parameters for each of the menus associated with the CONFIGURATION LIST are described in the remainder of this section. The user is encouraged to experiment with all test parameters, triggering modes, and display formats in order to gain more familiarity with the range and power of the instrument. See Section 6.0 for basic and advanced examples using the Logic Analyzer Test Card supplied with the NPC-700. See Sections 14.3 and 14.4 for I/O (RS-232 and IEEE-488) examples.

```

NR  NICOLET PARATRONICS 764 CONFIGURATION  UER 4.8
  1 - 48 CHNL STATE
  2 - 16 CHNL TIMING
  3 - 48 CHNL STATE/16 CHNL TIMING
  4 - 8 CHNL TIMING (100MHZ 2000 WORD)
  5 - 48 CHNL STATE/8 CHNL TIMING
  6 - 8 CHNL TIMING GLITCH
  7 - 48 CHNL STATE/8 CHNL GLITCH
  8 - WAVEFORM RECORDER
  9 - 48 CHNL STATE/WAVEFORM
 10 - COUNTER/TIMER
 11 - SIGNATURE ANALYZER
 12 - PI 70 SERIAL PROBE TRANSMIT

ESC - DISK OPERATING SYSTEM
BREAK - PROCESSOR SELF-TEST
I - I/O CONFIGURATION MENU

F1 STATE      F2      F3      F4      F5      F6
                SEL DOWN  SEL UP  COLLECT
  
```

Figure 5-1. Configuration List. (NPC-764 shown.)

In the above display, each line represents one possible configuration of the analyzer. Position the half-intensity cursor on the number of the configuration desired, using **SEL DOWN (F4)** or **SEL UP (F5)**. Then press **F1** to display the menu that will be used to establish the data collection parameters.

ESC/RESET

For the NPC-764, you can exit from the Analyzer Operating System and enter the CP/M Operating System by pressing **ESC**, the "escape key." The disk drive will turn on and load CP/M. Press **RESET** for at least 2 seconds to recall the Analyzer Operating System.

I/O

For the NPC-764, you can call the I/O configuration menu by pressing the **I** key. To return to the CONFIGURATION LIST, press the **CONFIG (F5)** key.

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5.2 48-CHANNEL STATE MENU* A. TO CALL MENU: (NPC-764)

1. Press the CONFIG or RESET key.
2. Using the SEL DOWN (F4) or SEL UP (F5) key, move the cursor to the 48 CHANNEL STATE mode (if necessary).
3. Press the STATE (F1) key.

```

                                     48 CHANNEL STATE MENU
1  FORMAT: AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA
2  A HEX
3  CLK SEL: A PRB: J B PRB: A C PRB: A QUALIFIERS: -AABBCC EL
4  CLK QUAL: OFF
5  OR OFF
6  PRE-TRIG MEMORY (0-999): 000 WORDS
7  RESTART: OFF
8  TRIGGER:
9  0 XXXXXXXXXXXX -XXXXXX XX
10 END
11
12
13
14
15
16
17
18
19
20
21 S1 - DATA DISPLAY
22 F1 PREVIOUS F2 NEXT F3 F4 F5 CONFIG F6 COLLECT
23
```

Figure 5-2. The NPC-764's 48-Channel State Menu. (Flashing prompting messages are not shown.)

B. EXPLANATION OF MENU:

FORMAT

Line 1: Using the labels A-F, this field allows the definition of a mixed-format state display consisting of any combination of HEX, OCT, BIN, DEC, and ASCII characters. The MSB of the A probe is at the far left of the field, the MSB of the B probe is the 17th bit from the left, the MSB of the C probe is the 33rd bit from the left. (Note that the labels A-F are completely general and have no relationship to the names "A probe," "B probe," and "C probe.")

When the menu is first called, the format field contains all A's. Use the A-F or X keys to insert other labels to establish the required groupings of the individual input data bits. Note that the label keys must be entered in order, i.e., AAAAAAAAA BCCCCCCC An X placed in any bit position will blank or mask that bit in the state display.

* The text in this section describes the NPC-764. In reading this text, note that the NPC-748 is identical except that the NPC-748 does not use the B probe and therefore has 16 fewer data channels than the NPC-764, 1 less clock input, and 2 fewer qualifiers.

LABELS A-F

Line 2: Press **NEXT (F2)** and use the **HEX, OCT, DEC, BIN,** or **ASC** keys (**H, O, Z, N,** or **Y**) respectively, to define these labels. (The default value is hex for all labels.)

CLOCK SELECT

Line 3: Selects the polarity of the A, B, and C clocks coming into the A, B, and C probes, respectively. If multiphase clocking is not required, the B and C probe clocks should be set to A (i.e., same as A probe clock); otherwise, use the appropriate clock edge, **(F3)** for positive, **(F4)** for negative.

QUALIFIERS: -AABBCC EL.

This is an identifying label only. The first A bit signifies the A probe's qualifier #1 (Q1 on the probe label); while the A probe's second A bit signifies the second qualifier #2 (Q2 on the probe label). The two B's and C's signify the same information for the B probe and C probe, respectively. Use of the E bit adds an EXTERNAL INPUT as a further qualifying condition while use of the L bit can LINK the internal State and Timing Analyzers or another, external NPC logic analyzer.

CLOCK QUALIFIER #1

Line 4: This is the first of two OR'ed clock qualification conditions that can be imposed on the data collection of the State Analyzer. This field normally defaults to OFF. With the OFF cursor flashing, pressing the **SELECT (F3)** key activates this field. The qualifier field consists of a 48-bit word (for data qualified clocking), followed by the six A, B, and C probe qualifier inputs (AABBCC), plus the E bit described above. This 55-bit word will automatically be grouped in accordance with the predefined display format. To set up the qualifier field, simply enter in the HEX, OCT, DEC, BIN, or ASCII digits as required. If a digit entered is out-of-range for the format used, the software will automatically "drop off" higher-order bits down to the number of bits allowed in the field. Also, values must be within the range of the selected base--such as 0-7 for an octal digit; otherwise an error message will appear.

Single formats can be used in this field independently of the format used for the RESTART word, TRIGGER word, or display. Simply press the **HEX, OCT,** etc., key for the single format of your choice. To recover the original display format used in Line 1, press the **USER** key, **U**. Note that to enter an ASCII character, the 2-digit HEX equivalent must be used. See Section 7.1.1 for a HEX-ASCII conversion table. The six probe qualifier bits can be entered only as 0, 1, or X; the E bit can only take on a 1 or X value.

CLOCK QUALIFIER #2

Line 5: This is the second OR'ed clock qualifier. It is set up in exactly the same way as the first qualifier. See Section 7.2 for additional information.

PRETRIG

Line 6: The PRETRIG field specifies the number of words that the analyzer will collect prior to the trigger word.

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RESTART*

Line 7: The RESTART field defaults to OFF. Pressing the **SELECT** key establishes a 48-bit word group in accordance with the specified display format, plus an 8-bit qualifier group. If this RESTART word is encountered, it will cause the trigger stack (described below) to return to level 0. See Section 8.1.3 for additional information.

Pressing the **SELECT** key again causes a bar (NOT indicator) to appear across the top of the RESTART word. This $\overline{\text{RESTART}}$ condition means that the analyzer will return to the top of the trigger stack (level 0) when anything other than the $\overline{\text{RESTART}}$ word is encountered.

TRIGGER STACK

Lines 8 to 12: These lines are used to set up 16 sequential triggering levels. Since only 4 levels can appear on the screen at one time, a scrolling technique is used to set up and display the remaining levels. The data keys are used to enter the 48-bit triggering conditions plus the 8 trigger qualifier conditions specified in the label: -AABBCC EL. (NOTE: If it is desired to set up a nonoccurrence triggering condition at any level, press the **SELECT** key, **F3**, to place a bar across the top of the TRIGGER word.)

DELAY

After level 0 is set up, the END field will flash. Pressing the **SELECT** key will access level 1 and display the associated delay mode. After level 1 data entry is complete, the cursor will move to the DELAY field. Use the **SELECT** key to choose the desired delay mode from the following choices:

AFTER nnnn CLOCKS
NOT ON nnnn CLOCKS
BEFORE nnnn CLOCKS
ON nnnn CLOCKS
OCCURS nnnn TIMES

Use the numeric keys to complete the DELAY field.

When level 3 is complete and level 4 is called, level 0 scrolls off the top of the stack display and is no longer displayed. This process can be continued until level 15 is completed. To roll the stack back and forth, use the **PREV** and **NEXT** keys, **F1** and **F2**.

LABELS

Lines 16 to 21: These fields are labels that indicate which key selects the format in which the data will be displayed. For example, press **H** to display all data in HEX. Press **U** to display data in the format specified in the menu.

* A RESTART word of all X's is not the same as OFF, and will cause the analyzer to continually reset the trigger stack to zero and **never collect data** (unless the TRIGGER words are also all X's).

- S1 Line 21: Press the S1 key to return to the data display without making a new data collection.
- F1 - F6 (FUNCTION KEYS) Line 22: Soft-key identifiers.
- PREVIOUS (F1) Line 23: Moves the cursor back to the previous field.
- NEXT (F2) Moves the cursor ahead to the next field.
- SELECT (F3) Used to display the options of the current field. Each time the SELECT key is pressed, a new option is displayed until the original option comes up again. If the cursor is moved with the PREV, NEXT or direct entry keys, the option displayed last becomes the operative parameter.
- DEFAULT (F4) Depending on the field, DEFAULT returns the field contents to the same value as that displayed upon initialization or moves the cursor to the first character position.
- CONFIG (F5) Returns to the CONFIGURATION LIST.
- COLLECT (F6) Initiates a new data collection.
- BACK SPACE Moves the cursor back one character position within the current field. (Field contents are unchanged.)
- SPACE BAR Moves the cursor ahead one character position within the current field. (Field contents are unchanged.)

5.2.1 48-CHANNEL STATE*
DATA DISPLAY
(NPC-764)

A. TO CALL DISPLAY:

1. Press the COLLECT key, F6, to perform the data collection. (One or more probes must be connected to the Logic Analyzer Test Card or a circuit-under-test; otherwise a WARNING-SLOW CLOCK message will appear and no data will be collected.)
2. If data has already been collected, press S1 to call the display.

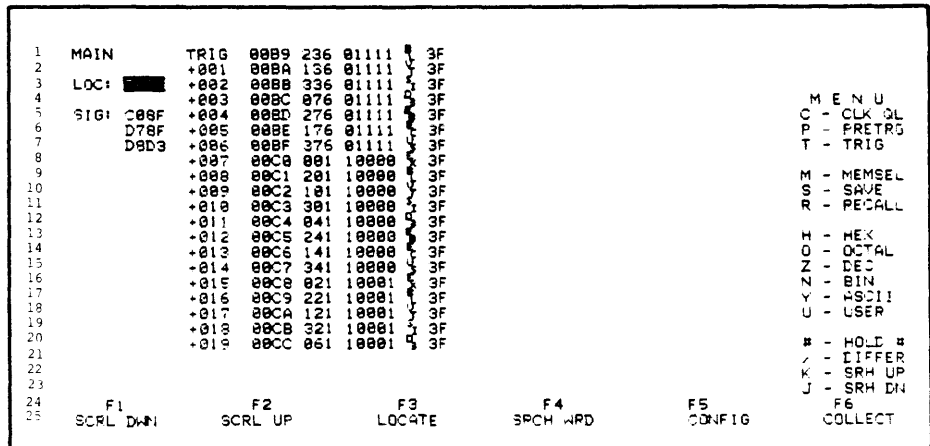


Figure 5-3. The NPC-764's 48-Channel State Data Display.

*The NPC-748 displays 16 fewer state channels.

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MENUS AND DISPLAYS

B. EXPLANATION OF 48-CHANNEL STATE DISPLAY:

MAIN (AUX)	Line 1: MAIN (AUX) memory identifier. Also, location of trigger word when the trigger word is at the top of the CRT.
TRIGGER/WORD LOCATOR	Line 3: Trigger and word locator field. Field accepts 3-digit word number plus sign. See LOCATE below.
TEST CODES	Lines 5 to 7: Test codes (SIG) of data collection. See Section 7.12.
DATA	Lines 1 to 20: Word number and associated data for 20 of the 1000 words collected. Note that the display is formatted in accordance with the FORMAT field previously set up.
LABELS	Lines 3 to 23: Menu for manipulating displayed data appears on right side of the CRT by pressing the LABELS key. Pressing the S1 key clears the menu.
DIRECT KEYS C-CLOCK QUAL P-PRETRG T-TRIG M-MEMSEL	C, P, or T will cause the state menu to be displayed, with the cursor in the field: CLOCK QUALIFIER, PRETRIGGER, or TRIGGER, respectively. M will select the AUX or MAIN memories for display.
S-SAVE*	S will write MAIN memory data into AUX memory.
R-RECALL*	R will return previous menu data into AUX memory.

***NOTE:** These commands provide temporary data storage/recall functions using the internal AUX RAM. The disk is not required for these functions.

DISPLAY FORMAT	H, O, Z, N, Y, or U will display all data in the single format selected.
-----------------------	---------------------------------------------------------------------------------

NOTE: The HEX, OCT, DEC, BIN, ASC, and USER formats serve two basic functions: When used within a menu, the bits in each data entry field are grouped into digits corresponding to the selected format; when used with data, they control the format displayed.

H - HEX	Causes state data or a data entry field to be displayed in a hexadecimal format.
O - OCT	Causes state data or a data entry field to be displayed in an octal format.

- Z - DEC** Causes state data or a data entry field to be displayed in a decimal format.
- N - BIN** Causes state data or a data entry field to be displayed in a binary format.
- Y - ASC** Causes state data to be displayed in 7-bit ASCII format. (Leading bits are ignored.)
- U - USER** Causes the mixed format defined in the menu by the user to replace the current display.
- I - MNEMONICS
(NOT SHOWN)** Displays collected data in assembly language using disassembler program selected from diskette. (See Section 6.5.)
- # - HOLD#** Pressing the # key calls the HOLD# mode. This mode is similar to COLLECT: It causes a data collection to be made according to the parameters specified in the menu. However, in the HOLD# mode, the data from the current data collection (main memory) is compared with the reference data in the auxiliary memory (previously stored using the SAVE key). If a difference is detected, the NPC-764 will stop the data collection process and display the data.

The differences in the data can be highlighted on the screen by using the DIFFERENCE function described below. If the data in the main memory are the same as the reference data, the collection process is automatically repeated until a difference is found. The message SAMPLING is displayed while collecting data and the message HOLDING is displayed when a difference between MAIN and AUX memories has been detected.

- / - DIFFERENCE** Pressing the / (DIFFERENCE) key once causes the information in the main memory to be compared to the reference data in the auxiliary memory. Data words that are identical are displayed at half-intensity; words exhibiting differences are displayed at full intensity. Pressing LOCATE and D finds the first difference. Alternating between AUX and MAIN memories (M + REPEAT) further highlights differences in data. The word DIFFERENCE on the screen indicates that the DIFFERENCE mode has been activated. Pressing the / key again deactivates the DIFFERENCE MODE.

- K - SEARCH UP,
J - SEARCH DOWN** K, SEARCH UP, and J, SEARCH DOWN are used in conjunction with SEARCH WORD mode described below.

- COLLECTION STATUS** Line 21: If triggering conditions are met, the message TRIGGERED is briefly displayed, followed by the message DONE when the 1K state data memory is full. If the sequential trigger stack is used and triggering conditions are not met at a particular trigger level, that level is identified and data are not displayed. If there is not enough incoming data to fill the 1K state memory, the amount of data words

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actually collected is also displayed. If no input clock is being detected or if the clock period is greater than approximately 1 second, the message WARNING-SLOW CLOCK will be displayed.

F1 - F6 (FUNCTION KEYS)

Line 24: Soft-Key identifiers.

SCROLL (F1, F2)

Line 25: The **SCRL DWN** and **SCRL UP** keys allow the viewing of different portions of the data collection. Note that **BACKSPACE** and **SPACEBAR** keys can also be used for scrolling the down and up, respectively.

LOCATE (F3)

The **LOCATE** key is used to position the cursor at the **LOC** field in the state display. After pressing the **LOCATE** key, the user enters a + or - followed by a three-digit number that represents the word location in memory relative to the trigger word. Pressing **LOCATE** and **T** places the trigger word at the top of the screen; pressing **LOCATE** and **B** places the beginning of the state collection (not necessarily the trigger word) at the top of the screen; pressing **LOCATE** and **E** places the end of the collection at the bottom. Pressing **LOCATE** and **D** when using the difference mode places the first full-intensity difference line at the top of the screen. Repeating **LOCATE** and **D** will move the next difference word to the top of the display. Pressing **LOCATE** and **S** places the first half-intensity same word at the top of the screen.

SEARCH WORD (F4)

Pressing the **SRCH WRD** key, **F4**, provides a rapid method of locating a particular word or bit pattern within a data collection. Pressing the **SRCH WRD** key activates the following menu:

```
FORMAT: AAAAAAAAA AAAAAAAAA BBBB BBBB CCDDDDDD DEEEEEEE EEEEEEE
        A HEX B OCT C BIN D ASC E HEX
SEARCH WORD:
          XXXX XXX XXX XX XXXX

S1 - DATA DISPLAY
F1  F2  F3  F4  F5  F6
PREVIOUS  NEXT  CONFIG  COLLECT

H - HEX
O - OCTAL
Z - DEC
N - BINARY
Y - ASCII
U - USER
```

Figure 5-4. Search Word Menu.

Pressing **PREVIOUS** or **NEXT** causes the display to return to the STATE menu to allow changes in the **FORMAT** field.

Once the desired word is entered in the SEARCH WORD field, return to the data display mode and then press the **K (SEARCH UP)** or **J (SEARCH DOWN)** key to initiate a search for that word in the data memory. When the SEARCH WORD is located, it is positioned at the top of the screen. Additional occurrences of the SEARCH WORD are found by again pressing the **K** or **J** key.

CONFIGURATION (F5)

The **CONFIG** key causes the CONFIGURATION LIST to be displayed again.

COLLECT (F6)

The **COLLECT** key initiates a new data collection.

5.3 16 CHANNEL TIMING MENU (1000 words, 50 MHz) A. TO CALL MENU:

1. Press the **CONFIG** or **RESET** key.
2. Press soft-key labeled **SEL DOWN** or **SEL UP** as appropriate to move the cursor to the 16 CHANNEL TIMING position.
3. Press **F1** to select the TIMING menu.
4. Place cursor in **CLOCK** field.

```

10 CHNL TIMING/STATE MENU
1 100ns CLOCK
2 TRIGGER WHEN: TRIG OCCURS > 0000 CLOCKS AFTER FIRST ARM
3 CHNL NO. A76543210 B76543210 FILTER LINKAGE
4 ARM (0.1.X): XXXXXXXX XXXXXXXX OFF NONE
5 TRIG (0.1.X): XXXXXXXX XXXXXXXX OFF NONE
6 INPUT MODE (S.L): SSSSSSSS SSSSSSSS
7 PRE-TRIGGER (0-9): 10%
8
9
10 DISPLAY ORDER (0-7.Y): AAAAAAAA BBBB8888
11 DISPLAY POLARITY (+.-): 76543210 76543210
12 THRESHOLD: A PROBE B PROBE HYSTERESIS
13 (-6.4V - +6.35V) +1.60 +1.60 ON

```

S1 - STATE DISPLAY F3 F4 F5 F6
 S2 - TIMING DISPLAY PREVIOUS NEXT CONFIG COLLECT

Figure 5-5. 16-Channel Timing Menu.

B. EXPLANATION OF MENU:

CLOCK SELECT

Line 1: Clock sampling interval (internal clock) or clock polarity and qualifier (external clock). Clock speed is selected using the **SLOWER (F3)** and **FASTER (F4)** keys. External clock polarity is selected by **P**, for positive edge, or **N**, for negative edge. If an external clock is selected, the **CLOCK QUALIFIER** field is displayed, allowing selection of 1, 0, or X for the external clock qualifier bit.

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TRIGGER MODE

Lines 2 and 3: Triggering modes. Use the **NEXT** or **PREVIOUS** keys to access the TRIGGER MODE field as indicated by the small, flashing cursor. Then use the **SELECT** key to call the desired mode. The possible modes are described in detail in Section 8.0.

Within each mode, use the **NEXT** and **SELECT** keys to change TRIG to TRIG,<to> to =, ARM to ARM, FIRST to LAST, and AFTER to BEFORE. In order to change the clock delay value, use the **NEXT** key to step to the DELAY field. Then use the numeric keys to set up the clock delay.

CHNL NO.

Line 4: Headers for the CHANNEL NUMBER, FILTER, and LINKAGE fields.

ARM, FILTER, LINKAGE

Line 5: In the ARM field, the combinatorial logic values (0,1,X) will arm (enable) the analyzer for triggering. FILTER sets the number of consecutive clock sample intervals (2-9) during which the ARM word must be stable before it is accepted. (NOTE: Use of 0 or 1 will turn the filter off which is equivalent to a default value of 1.) When in the LINKAGE field, press the **SELECT** key to set up the NPC-700 for linking to other analyzers, to the State (L) or Waveform (W) Sections, or to an external input (E).

TRIG, FILTER, LINKAGE

Line 6: Similar to Line 5 except that these parameters set up the conditions associated with the trigger word.

NOTE: In order for the analyzer to complete a data collection, the delay relationship between arm and trigger specified in Line 3 must be completely satisfied.

INPUT MODE (S,L)

Line 7: Sets each channel for sample or latch (glitch capture) operation.

PRETRIGGER (0-9)

Line 8: Specifies percentage (0-90%) of data to be collected prior to trigger point. 10% pretrigger is the default value. To ensure data collection, note that the NPC-700 does not require that the full amount of pretrigger data be collected before the trigger condition becomes satisfied, so that the amount of data actually preceding the trigger point can be less. However, the amount of data following the trigger point will always be constant for a given pretrigger value.

DISPLAY ORDER (0-7, X)

Lines 9 and 10: Specifies the order in which the collected timing channels appear in the display. The labels A and B correspond to 8-bit data groups coming through the A and B probes. An X blanks out a line, and the numbers 0-7, entered in any order (or even repeated), set up the display order within the probe group.

DISPLAY POLARITY (+,-)

Line 11: Use of the + or - keys here will display a TRUE or COMPLEMENTED timing diagram, respectively.

THRESHOLD (-6.4V to +6.35V)

Lines 12 and 13: These fields allow the keyboard selection of thresholds at the input to each 8-channel probe. Thresholds are settable in 50 mV increments anywhere in the specified range by pressing the appropriate numeric data entry keys. Note that the default value is +1.60V for TTL logic.

HYSTERESIS

If HYSTERESIS is ON, a preset hysteresis value of 200 mV is incorporated into the threshold for noise rejection.

5.3.1 16-CHANNEL TIMING DISPLAY
(1000 words, 50 MHz)

COLLECT (F6)

A. TO CALL DISPLAY:

1. Press the **COLLECT** key to perform a data collection. (One or more probes must be connected to the test card or a circuit-under-test to collect data.)
2. Press **S1** to display equivalent state data; press **S2** for equivalent timing data.

S1
S2

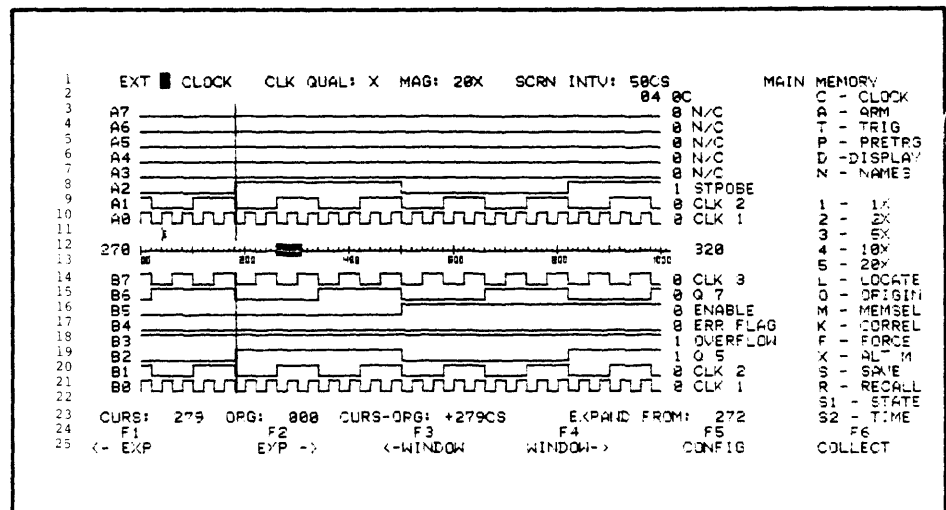


Figure 5-6. 16-Channel Timing Display using an external clock, 0% pretrigger, and 20X magnification. The Logic Analyzer Test Card is the source.

B. EXPLANATION OF THE 16-CHANNEL TIMING DISPLAY:

CLOCK, MAG, SCRN INTV,
MAIN/AUX

Line 1: Displays the clock sampling interval (internal clock) or clock polarity and qualifier (external clock), the magnification factor, and the screen interval. (FOR INTERNAL CLOCK OPERATION, THE SCREEN INTERVAL = CLK PERIOD X 1000 SAMPLES - BY MAGNIFICATION FACTOR; FOR EXTERNAL CLOCK OPERATION, THE SCREEN INTERVAL = NUMBER OF CLOCK SAMPLES.) Also displayed is the MAIN/AUX memory identifier.

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HEX VALUE	Line 2: Data in hexadecimal at current cursor location. The hexadecimal cursor value is affected by the display order.
TIMING DIAGRAMS	Lines 3-10 and 14-21: Displays all 16 channels of timing data in two groups of 8. The cursor is used to measure time between events. The value of the corresponding data in binary at the current cursor location is displayed at the right end of each timing trace. Note that the NPC-700 provides a unique "shaded" display for those timing diagrams whose transitions are occurring too close together to be resolved at lower screen magnifications. This feature reduces the possibility of making erroneous visual time measurements. Shaded areas are always resolved into discrete lines at X10 or X20 magnification factors.
EXPANSION INDICATOR (E)	Line 11: This indicator can be moved anywhere within the screen by pressing the EXPAND keys <-EXP or EXP-> . It is used to locate an area in the current screen that requires additional magnification. Expansion is always to the right of the indicator.
GRATICULE	Line 12: The graticule shows the range and position in inverse video (relative to the entire 1000-word data collection) of the current display. The trigger point is shown as an intensified numeric label on the graticule. The numbers at the left and right-hand sides of the graticule indicate the boundary values of the displayed data.
CURS, ORG, CURS-ORG, EXPAND FROM	Line 23: Displays the numeric values for the current location of the cursor, the current location of the origin, the difference in time or clock samples between the cursor and origin, and the expansion indicator location.
<-EXP, EXP-> (F1, F2)	Line 25: The <-EXP and EXP-> keys move the expansion cursor, E , back and forth on the screen. Note that the expansion cursor cannot be moved off the screen. The expansion cursor does not appear in the waveform display; however, the EXPAND functions are still valid.
<-WINDOW, WINDOW-> (F3, F4)	The <-WINDOW and WINDOW-> keys are used to select the portion of the data collection currently being displayed. This window, and its position in the data memory, are shown by the inverse video portion of the graticule below the waveforms on the screen. Note that at any expansion factor other than X1, all of the data memory cannot be displayed at one time. For these larger expansion factors, pressing either WINDOW key will step or sweep (using REPEAT) the window so that the entire data collection can be viewed. Moving the window to the left, for example, causes the displayed data to move from left to right.
CONFIG (F5)	Pressing the CONFIG key, F5 , causes the CONFIGURATION LIST to be displayed again.
COLLECT (F6)	Pressing the COLLECT key, F6 , initiates a new data collection.

LABELS

Lines 2 to 23: Prompting messages can be accessed (after a data collection is displayed) by pressing the **LABELS** key. It identifies all direct entry functions.

C-CLOCK
A-ARM
T-TRIG
P-PRETRG
D-DISPLAY

Lines 2 to 6: These keys call the **TIMING** menu, with the cursor located in the particular field selected by each key. For example, **T** will place the cursor in **TRIGGER** field of the menu. Other fields can then be accessed by using **PREVIOUS** or **NEXT**. Also, **S2** can be pressed to call the data again.

N-NAMES

Line 7: The **N** key places a cursor at the right of the timing diagram display for the generation of an 8-character alphanumeric label for each channel. These labels are defined by the user to identify and document displayed signals. Pressing the **ESC** key terminates the **NAME** mode.

1-1X
2-2X
3-5X
4-10X
5-20X

Lines 9 to 13: The numeric keys **1**, **2**, **3**, **4**, and **5** expand the timing (and waveform) displays by the indicated factor. Expansion occurs from the right of the current position of the expansion cursor, which is represented on the screen by the symbol \bar{E} . When expansion occurs, the expansion cursor will normally be positioned to the far left of the screen. The exact position of the expansion cursor is indicated on the screen in the **EXPAND FROM** field.

L-LOCATE (CURSOR)

Line 14: **L** is used rapidly to bring the timing cursor onto the left-hand edge of the screen. This is useful when the cursor's present location is away from the present window of data being viewed.

O-ORIGIN

Line 15: **O** is used to simplify time measurements with the cursor. Pressing this key causes the current position of the cursor to become the **ORIGIN**. In the waveform mode, the voltage at the current cursor position also becomes the **ORIGIN** value. Moving the cursor from this position then causes differences in time (and voltage) between cursor and origin values to be displayed.

M-MEMSEL

Line 16: **M**, **MEMSEL**, selects the **MAIN** or **AUXILIARY** memory for display.

K-CORREL

Line 17: The **K** key is used to calculate the correlation (figure of merit) between the current data collection in the main memory and the reference data in the auxiliary memory. The computation is performed independently for each active channel. Total bit-for-bit correspondence results in a correlation of 1.000 being displayed. A one-bit difference, for example, reduces the correlation to 0.999. For a correlation example, see Section 6.2.2.

NOTE: When the **K** key is pressed, the correlation values replace the timing diagram names. Press **S2** to return the names.

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F-FORCE

Line 18: If the **COLLECT** key has been pressed, but triggering conditions have not been met (or if the collection is only partially complete), **F**, the **FORCE DISPLAY** key, stops the data collection process and causes captured data to be displayed. The last data word collected is automatically defined as the trigger point. Pressing the **FORCE DISPLAY** key allows the prior 999 words to be viewed, regardless of the setting of the pretrigger field. (In the 8 CHANNEL TIMING mode, the prior 1999 words are displayed.)

X-ALT M

Line 19: The **X** key causes the display to automatically alternate between **MAIN** and **AUX**.

S-SAVE*

Line 20: After a data collection has been made, pressing the **S** key saves the contents of the main memory into the auxiliary memory. Included with the saved data is the set of menu parameters and test codes used to obtain the data collection.

R-RECALL*

Line 21: Pressing the **R** key recalls the menu information and data stored in the auxiliary memory with the **SAVE** key. This function allows a previous test to be repeated without having to re-enter parameters. Note: Pressing the **RECALL** key causes the current menu parameters to be lost.

S1-STATE

Line 22: The **S1** key allows the user to select the state equivalent of the timing diagram or analog waveform displays. Pressing **S1** will again call the timing display.

S2-TIME

Line 23: The **S2** key returns the timing display.

CURSOR RIGHT, CURSOR LEFT

The **SPACE BAR** and **BACK SPACE** keys step the timing cursor right or left, respectively, through the data collection.

As the cursor moves, its current position is indicated on the screen. The cursor measures the time between events in the data collection and can be used in conjunction with the **ORIGIN** function. Note that even if the cursor is off-screen, its position is still indicated correctly. Also note that the binary value corresponding to the state of each input line appears at the right-hand-side of the screen. The associated hexadecimal value corresponds to all channels in the memory, whether they are displayed or not. The binary and hexadecimal values will change when the display order is modified in the menu. (The general rule that applies here is: "What you see is what you get.") In the waveform mode, the voltage at the cursor position is also displayed.

***NOTE:** These commands provide temporary data storage/recall functions using the internal AUX RAM. The disk is not required for these functions.

5.3.2 16-CHANNEL STATE DISPLAY
(1000 words, 50 MHz)

A. TO CALL DISPLAY:

COLLECT
S1

1. Press the **COLLECT** key to perform the data collection.
2. If data have been collected and are displayed in the timing format, press **S1** to call the state display.
3. Press the **LABELS** key, then press one of the display format keys. (Hexadecimal is used in this example.)

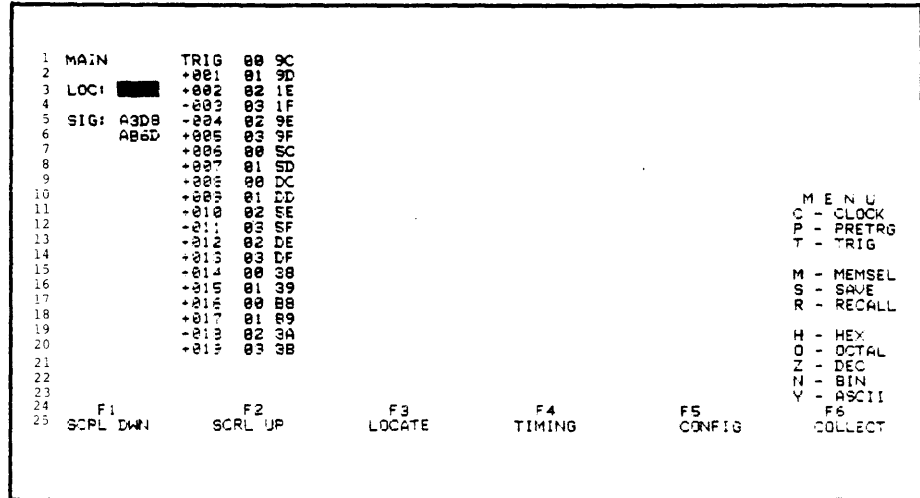


Figure 5-7. 16-Channel State Display.

B. EXPLANATION OF THE 16-CHANNEL STATE DISPLAY:

MAIN (AUX)

Line 1: **MAIN (AUX)** memory identifier, location of trigger word (this example).

LOC

Line 3: TRIGGER word locator field.

SIG

Lines 5 and 6: Test codes (SIG) of data collection.

DATA

Lines 1 to 20: Word number and associated data for 20 of the 1000 words (max) collected in this mode. Note that the display is formatted in accordance with the **H**, **O**, **Z**, **N**, or **Y** key used. The data order is A7-A0, B7-B0, and is fixed.

SCRL DWN (F1)
SCRL UP (F2)
LOCATE (F3)

Line 25: The **SCRL DWN (BACKSPACE)** and **SCRL UP (SPACEBAR)** keys, as described earlier, allow different segments of data to be viewed.

The **LOCATE** key is used to position the cursor at the LOC field in the state display. After pressing the LOC key, the user enters a + or - followed by a three-digit number that represents the word location in memory relative to the trigger word. Pressing **LOCATE** and **T** places the trigger word at the top of the screen; pressing **LOCATE** and **B** places the beginning of the state collection (not necessarily the trigger

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word) at the top of the screen; pressing **LOCATE** and **E** places the end of the collection at the bottom. Pressing **LOCATE** and **D** when using the **DIFFERENCE** mode places the first full-intensity difference line at the top of the screen. Repeating **LOCATE** and **D** will move the next difference word to the top of the display. Pressing **LOCATE** and **S** places the first half-intensity "same" word at the top of the screen.

TIMING (F4), S2

The **TIMING** key calls the timing display, as does **S2**.

LABELS

Lines 10 to 23: The menu for manipulating timing data is displayed by pressing the **LABELS** key.

DIRECT KEYS C-CLOCK QUAL P-PRETRG T-TRIG M-MEMSEL

C, P, or T will cause the menu to be displayed, with the cursor in the field: **CLOCK QUALIFIER**, **PRETRIGGER**, or **TRIGGER**.

M will alternate the display between the **AUX** and **MAIN** memories.

S-SAVE

S will write **MAIN** memory data into **AUX** memory.

R-RECALL

R will write **AUX** memory data into **MAIN** memory.

DISPLAY FORMAT

H, O, Z, N, Y, or U will display all data in the single format selected.

NOTE: The **HEX**, **OCT**, **DEC**, **BIN**, **ASC**, and **USER** formats serve two basic functions: When used within a menu, the bits in each data entry field are grouped into digits corresponding to the selected format; when used with displayed data, they control the format used.

H - HEX

Causes state data or a data entry field to be displayed in a hexadecimal format.

O - OCT

Causes state data or a data entry field to be displayed in an octal format.

Z - DEC

Causes state data or a data entry field to be displayed in a decimal format.

N - BIN

Causes state data or a data entry field to be displayed in a binary format.

Y - ASC

Causes state data to be displayed in a 7-bit ASCII format. (Leading bits are ignored.)

5.4 **8-CHANNEL TIMING MENU**
(2000 words, 100 MHz)

A. TO CALL MENU:

1. Press the **CONFIG** or **RESET** key.
2. Press the **SEL DOWN** or **SEL UP** key to move the cursor to the 8 channel timing position.
3. Press the **TIMING (F1)** key to call the **TIMING** menu.

```

      8 CHNL TIMING/STATE MENU

      10ns CLOCK
TRIGGER WHEN: TRIG OCCURS > 0000 CLOCKS AFTER FIRST ARM
              CHNL NO. A76543210 B76543210 FILTER LINKAGE
ARM (0.1.X):  XXXXXXXX OFF NONE
TRIG (0.1.X): XXXXXXXX OFF NONE
INPUT MODE (S.L): SSSSSSS
PPE-TRIGGER (0-9): 00%
DISPLAY ORDER (0-7.X): AAAAAAA 76543210
DISPLAY POLARITY (+.-): ++++++
THRESHOLD: CH 0-3,CLOCK CH 4-7 HYSTERESIS
(-6.4V - +6.35V) +1.60 +1.60 ON

      S1 - STATE DISPLAY
      S2 - TIMING DISPLAY
      F1 - PREVIOUS      F2 - NEXT      F3      F4      F5      F6
                                CONFIG      COLLECT
  
```

Figure 5-8. 8-Channel Timing Menu.

B. EXPLANATION OF THE MENU:

CLOCK SELECT

The 8-channel timing menu is virtually identical to the 16-channel menu described in Section 5.3 except that only the fields associated with the A timing probes are valid.

- NOTES:**
1. The B probe must be disconnected for this mode.
 2. When using an external clock, data words are recorded on both clock edges, independent of the edge selected.

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5.4.1 8-CHANNEL TIMING DISPLAY (2000 WORDS, 100 MHz)

COLLECT
S2

A. TO CALL DISPLAY:

1. Press the **COLLECT** key to perform a data collection.
2. If data have already been collected, but displayed in the state format, press the **S2** or the **TIMING (F4)** key.

NOTE: Although an internal sampling clock was used in this example, an external clock (rising or falling edge) and qualifier (0,1,X) could have been used as well.

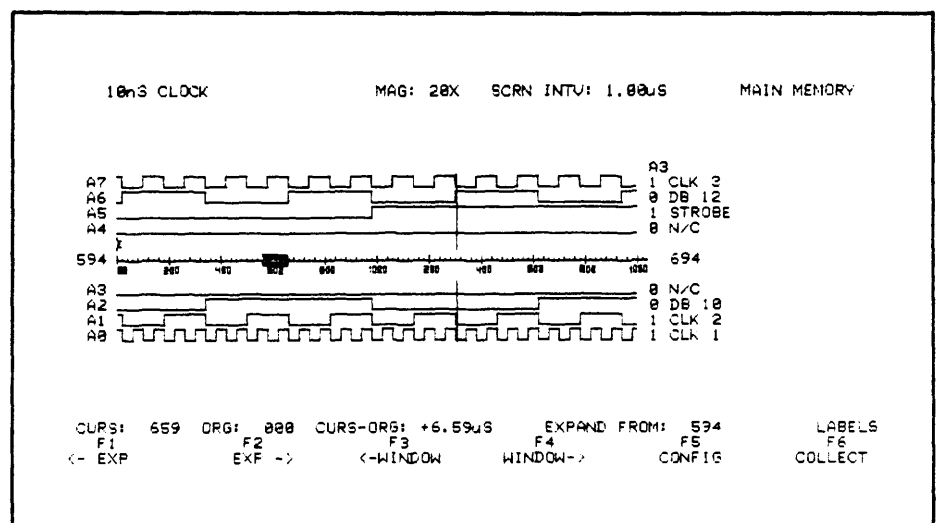


Figure 5-9. 8-Channel Timing Display.

B. EXPLANATION OF THE 8-CHANNEL TIMING DISPLAY:

The 8-channel timing display is similar to the 16-channel timing display described in Section 5.3.1 except that the left and right-hand graticule range numbers cover 0 to 2000 words. Also, data displayed corresponds only to the A probe.

5.4.2 8-CHANNEL STATE DISPLAY
(2000 WORDS, 100 MHz)

COLLECT
S1

A. TO CALL DISPLAY:

1. Press the COLLECT key to perform the data collection.
2. If data have been collected and are displayed in the timing format, press S1 to call the state display.
3. Press one of the display format keys. (Hexadecimal is used in this example.)

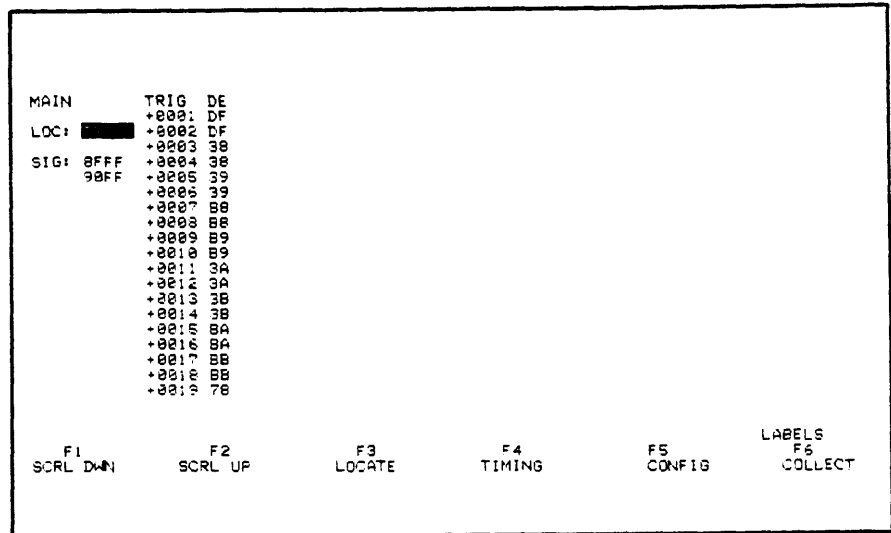


Figure 5-10. 8-Channel State Display.

B. EXPLANATION OF THE 8-CHANNEL STATE DISPLAY:

The 8-channel state display is similar to the 16-channel state display described in Section 5.3.2 except that only the 8 channels corresponding to the A probe are displayed.

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5.5 8-CHANNEL TIMING GLITCH MENU (1000 words, 50 MHz) A. TO CALL UP MENU:

1. Press the **CONFIG** or **RESET** key.
2. Press the **SEL DOWN** or **SEL UP** key to select the **8 CHNL TIMING GLITCH** mode.
3. Press the **TIMING (F1)** key to call the menu.

```

                                     8 CHNL TIMING/STATE MENU
1                                     100ns CLOCK
2 TRIGGER WHEN:
3 TRIG OCCURS > 0000 CLOCKS AFTER FIRST ARM
4 CHNL NO. A76543210 B76543210 FILTER LINKAGE
5 ARM (0-1,X): XXXXX
6 TRIG (0-1,X): XXXXX
7 INPUT MODE (S,L): SSSSSSSS OFF NONE
8 PRE-TRIGGER (0-9): 10X OFF NONE
9
10 DISPLAY ORDER (0-7,X): AAAAAAA
11 DISPLAY POLARITY (+,-): 76543210
12 THRESHOLD: CH 0-3,CLOCK CH 4-7 HYSTERESIS
13 (-5.4V - +6.35V) +1.60 +1.60 ON

```

S1 - STATE DISPLAY
S2 - TIMING DISPLAY

F1 PREVIOUS F2 NEXT F3 F4 F5 CONFIG F6 COLLECT

Figure 5-11. 8-Channel Timing Glitch Menu.

B. EXPLANATION OF MENU:

- Line 1: Clock sampling interval (internal clock) or external clock and qualifier.
- Lines 2 to 13: Same as 8-channel timing menu described in Section 5.4 except that the INPUT MODE field will default to all S's (sample mode) for proper operation. Also, the B probe must be disconnected from the analyzer.

NOTE: The triggering mode: **GLITCH IN ARM WHEN TRIG VALID** is not used here because it requires latch (L) bits to be set in the INPUT MODE field. As described above, the S bits (and not the L bits) are used in the 8-CHANNEL TIMING GLITCH mode. See Section 7.9 for a description of the sample (S) and Latch (L) modes of operation.

5.5.1 8-CHANNEL GLITCH TIMING
DISPLAY
(1000 words, 50 MHz)

COLLECT
S2

LABELS
X10, X20

A. TO CALL DISPLAY:

1. Press the **COLLECT** key to perform a data collection.
2. If data have been collected and displayed in the state format, press the **S2** key to call the timing display.
3. Press the **LABELS** key.
4. Press the **4 (X10)** or **5 (X20)** key to view glitches.

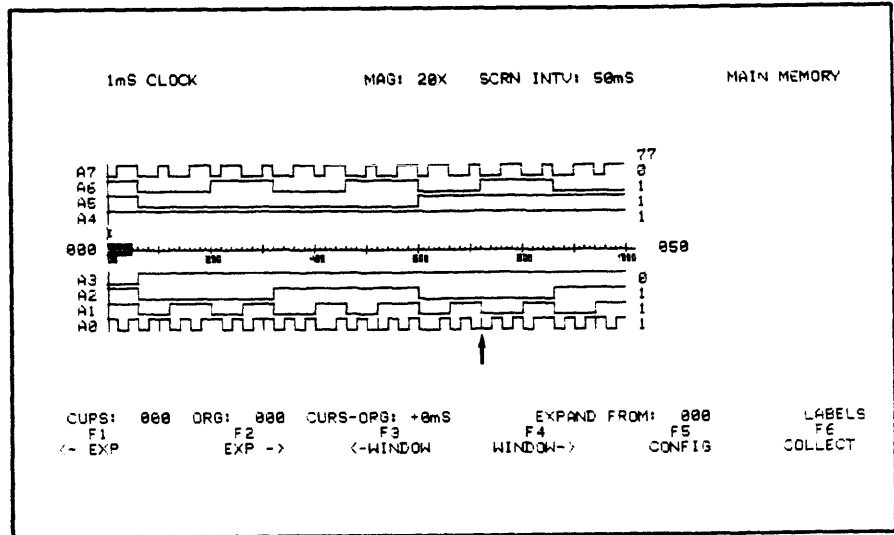


Figure 5-12. 8-Channel Timing Glitch Display using a 1 mS clock, 0% pretrigger, and 20X magnification. The Logic Analyzer Test Card is the source.

B. EXPLANATION OF THE 8-CHANNEL GLITCH TIMING DISPLAY:

The 8-channel glitch timing display is similar to the 16-channel timing display described in Section 5.3.1 except that vertical lines or "spikes" are displayed where glitches occur between clock transitions. Data and glitches correspond only to the A probe.

For additional information, see Section 7.9.

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5.5.2 8-CHANNEL GLITCH STATE MODE (1000 words, 50 MHz)

COLLECT
S1

BIN (N)

A. TO CALL DISPLAY:

1. Press the **COLLECT** key to perform a data collection.
2. If data have already been collected and displayed in the timing format, press **S1** to call the state display.
3. Press the **BIN (N)** key for a binary display format. (Binary is generally used in this mode for glitch identification.)

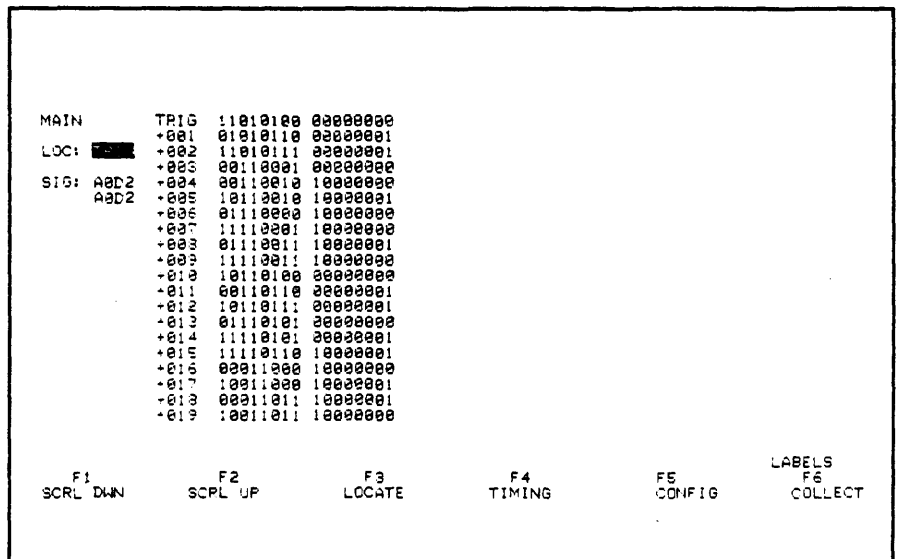


Figure 5-13. 8-Channel Glitch State Display.

B. EXPLANATION OF THE 8-CHANNEL GLITCH STATE DISPLAY:

The 8-channel glitch state display is similar to the 16-channel state display described in Section 5.3.2 except that the second (right-hand) set of 8-bit words represents the glitch memory while the left-hand set of 8-bit words represents the corresponding data memory. A logic 1 in the right-hand set of words indicates that a glitch has occurred in the corresponding word location and channel in the 8-bit data memory display. In this manner, glitches that are coincident with normal data transitions can be readily identified. (These coincident glitches are not apparent in the timing diagram display.)

5.6 WAVEFORM MENU
(1000 WORDS, 50 MHz)

A. TO CALL UP MENU:

1. Press the **CONFIG** or **RESET** key
2. Press the **SEL DOWN** or **SEL UP** to select the **WAVEFORM RECORDER** mode.
3. Press the **WAVEFORM (F1)** key to call the menu.

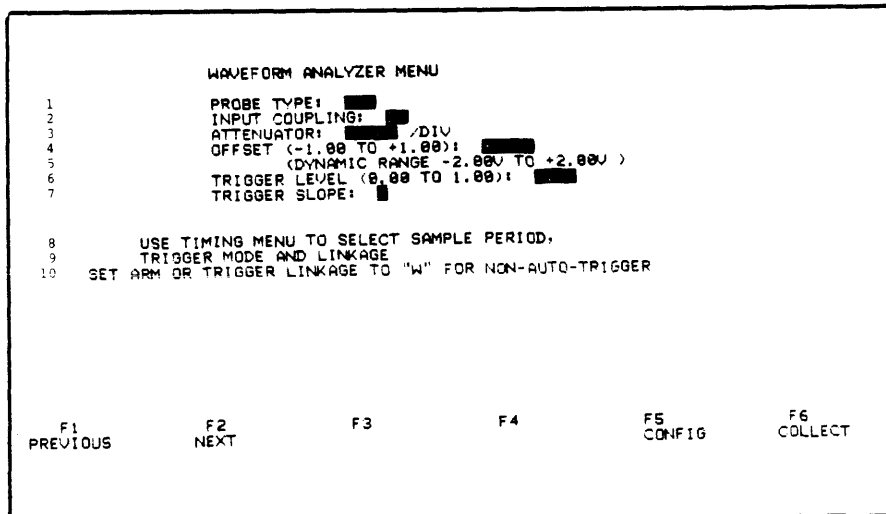


Figure 5-14. Waveform menu.

B. EXPLANATION OF MENU:

Line 1: PROBE TYPE (X10,X1). This field configures the waveform analyzer for the type of probe used.

Line 2: INPUT COUPLING. DC, AC, GND.

Line 3: ATTENUATOR. 5mV/DIV to 20V/DIV (X1 probe). 50mV/DIV to 200V/DIV (X10 probe).

Line 4: OFFSET. Waveform vertical position control. (± 1.00 full screen).

Line 5: DYNAMIC RANGE. Computed by waveform analyzer based on above parameters. Input waveforms within this range will be digitized by the A/D converter without saturation.

Line 6: TRIGGER LEVEL. Threshold level for incoming waveform to cause analyzer to trigger. (0.00-1.00; 0.00 = bottom of screen; 1.00 = top of screen.)

Line 7: TRIGGER SLOPE. Rising or falling. This is the slope of the waveform at the threshold crossing which is required for triggering.

Lines 8-10: Instructions to use timing menu to set up sample clock, trigger mode (including pretrigger), and linkage. For threshold and slope parameters of the waveform menu to be

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active, a **W** must be set into the linkage portion of the ARM or TRIG field; otherwise, the waveform analyzer operates in an auto-trigger (free-running) mode when **COLLECT** is pressed.

5.6.1 WAVEFORM DISPLAY (1000 words, 50 MHz)

A. TO CALL DISPLAY:

1. Press the **COLLECT** key to perform a data collection.
2. Press the **D** key once for raw sample points. Press the **D** key a second time for unconnected, software interpreted values. Press the **D** key a third time to return to a software-smoothed display.

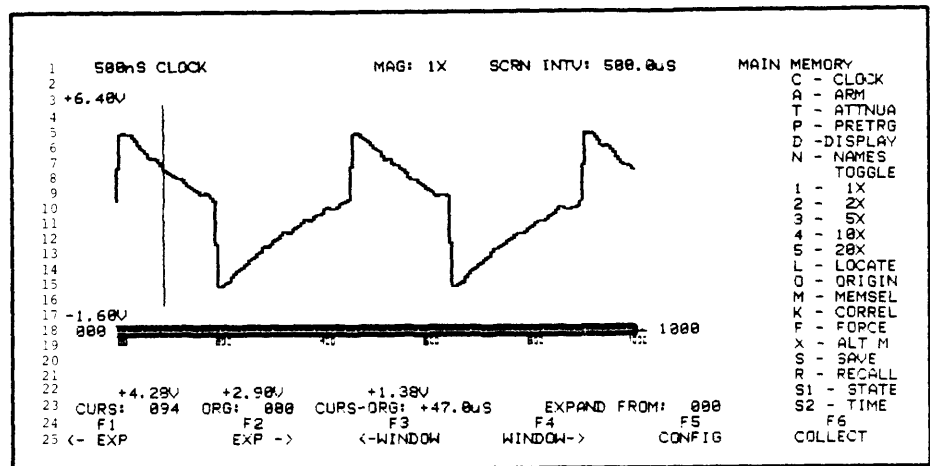


Figure 5-15. Waveform display.

B. EXPLANATION OF WAVEFORM DISPLAY:

Line 1: Displays the internal (or external) clock sampling interval, the magnification factor, the screen interval, and the MAIN/AUX memory.

Line 3: Displays the most positive voltage of the measurement window at the left.

Line 17: Displays the most negative voltage of the measurement window at the left.

Line 18: Displays the inverse video graticule which shows the range and position (relative to the entire 1000-sample data collection) of the current display. The trigger point is intensified.

Line 22: Displays the voltage at the cursor, the voltage at the origin, and the voltage difference between the cursor and the origin. (Measurement accuracy is $\pm 3\%$.)

Line 23: Displays the current location of the cursor, the current location of the origin, the difference in time between the cursor and origin values (for time measurement), and the expansion factor location.

NOTE: The expansion symbol, Ξ , used in the timing display is not available in the waveform display. However, the **EXPAND FROM:** indicator is still valid.

Lines 2-23: Direct entry and display manipulation keys.

Lines 24 and 25: Soft-key identifiers and labels.

5.6.2 STATE VERSION OF WAVEFORM DISPLAY

A. TO CALL DISPLAY:

1. Press the **COLLECT** key to perform the data collection.
2. Or if data have been collected, press the **S1** key.
3. Press the **BIN (N)** key.

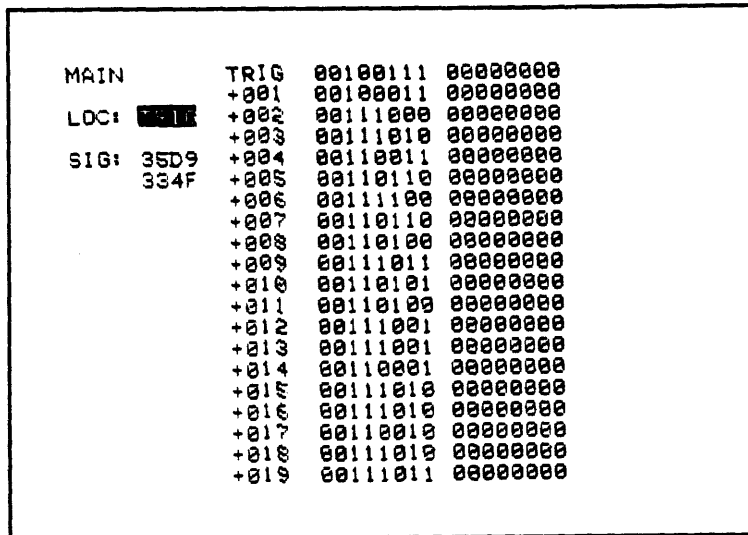


Figure 5-16. Binary values of waveform samples.

B. EXPLANATION OF THE STATE VERSION OF THE WAVEFORM DISPLAY:

The state version of the waveform display is similar to the 8-channel state display. However, for the waveform analyzer, the binary words represent the instantaneous voltage values at the sample points of the incoming analog signal. (Since the waveform analyzer uses a 6-bit A/D converter, the two MSB's in the 8-bit display are always 0.)

5.6.3 WAVEFORM DISPLAY MAGNIFICATION CONCEPTS

- X1** For this magnification factor, each point of the waveform display represents 5 samples of data in the timing memory. The software takes the first valid sample (i.e., the fourth sample), then scans subsequent sets of 5 samples each,

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choosing the sample with the largest deviation from the last point displayed. This procedure continues until 997 samples in memory are processed.

X2 For X2 magnification, the display process is similar to X1 magnification, except that only 500 samples of timing memory are scanned in alternating groups of 2 and 3 samples.

X5 Here, 200 samples of the timing memory are used to display 200 waveform points on the screen. A filtering algorithm is used to smooth the data at X5 and higher magnifications.

X10 Here, 100 samples of the timing memory are used to generate 200 waveform points on the display. The interpolated points are calculated by the linear interpolation algorithm. Furthermore, the filtering algorithm mentioned previously is also utilized.

X20 Here, 50 samples of the timing memory are used to generate 200 points of waveform data. Each bit of timing memory generates 4 points on the display. A linear interpolation method is used for the interpolated points; then it is smoothed by the filtering algorithm.

5.4 ALIASING

Aliasing occurs when a high frequency waveform appears on the display as a low frequency waveform due to an insufficient sample rate (i.e., below the Nyquist limit).

To avoid aliasing, as a **conservative** rule of thumb, always sample at 5 to 10 times faster than the highest frequency component of the incoming waveform.

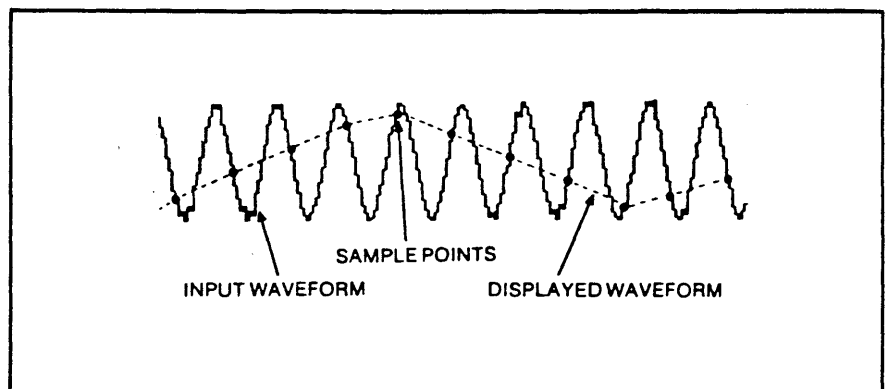


Figure 5-17. Example of aliasing. Notice that the high frequency waveform is displayed as a low frequency "alias."

5.7 COUNTER-TIMER
MENUS

Three illustrative counter-timer menus are shown below:

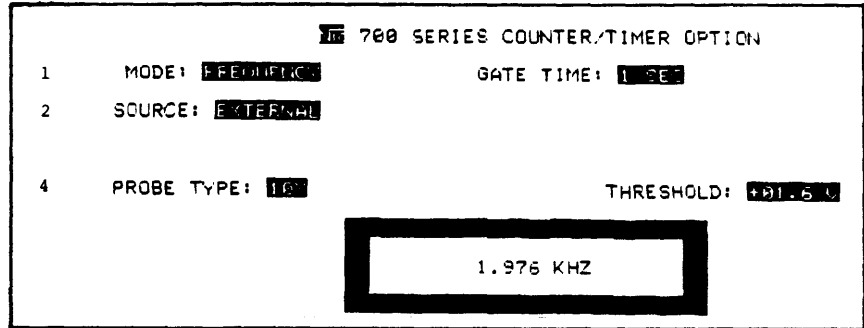


Figure 5-18. Frequency mode with external as source. (Using Model 90 probe.) (The total mode is similar.)

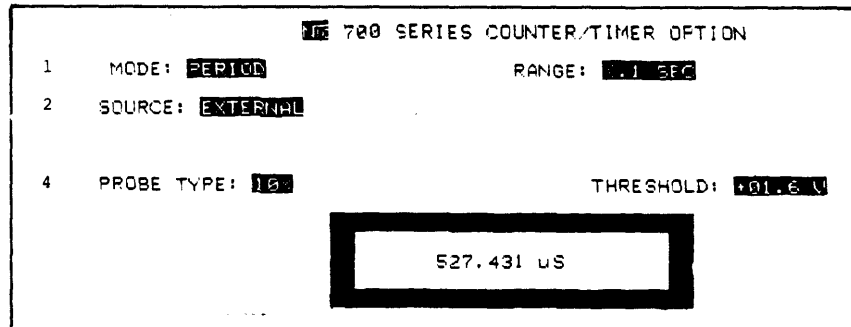


Figure 19. Period mode with data as source. (Using state probes.) (The total mode is similar.)

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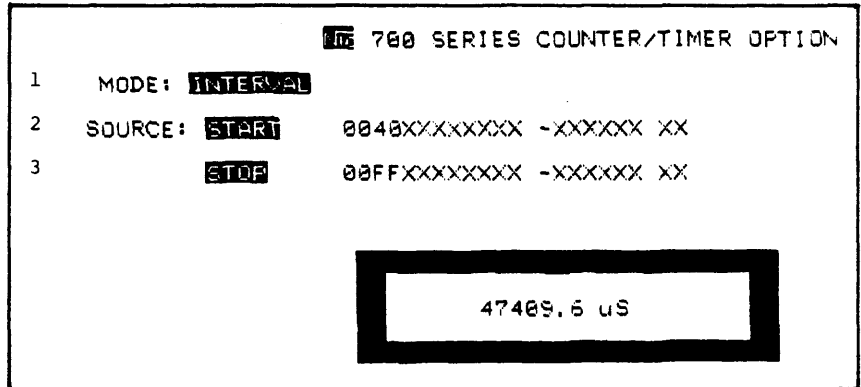


Figure 5-20. Interval mode with start and stop words as source. (NPC-764 shown.)

A. TO CALL UP MENU:

1. Press the **CONFIG** or **RESET** key.
2. Press the **SEL DOWN** or **SEL UP** key to select the **COUNTER-TIMER** mode.
3. Press the **SELECT (F1)** key to call the menu.

B. EXPLANATION OF MENU:

Line 1: **MODE.** The user can select from the following counter-timer modes: **FREQUENCY**, **PERIOD**, **INTERVAL**, and **TOTAL**. Measurements can be made of individual signals using the Model 90 scope probe or of state events using the analyzer's 16-channel state probes.

The **FREQUENCY** mode can measure individual signals up to 100 MHz using the Model 90 probe, or state events up to 10 MHz using the 16-channel state probes.

The **PERIOD** mode is the inverse of the **FREQUENCY** mode.

The **TOTAL** mode measures the total number of occurrences of single events monitored by the Model 90 probe, or state events monitored by the 16-channel state probes.

GATE TIME: Used in the **FREQUENCY** mode only. The **GATE TIME** is the time interval over which the frequency is measured and can be selected from 10 msec to 10 seconds.

RANGE: Used in the **PERIOD MODE** only. The **RANGE** is the maximum period which can be measured and can be selected from 10 msec to 10 seconds.

Lines 2 & 3: **SOURCE:** In the FREQUENCY, PERIOD, AND TOTAL modes, the SOURCE field can be selected as EXTERNAL (Model 90 probe), PRESCALE (EXTERNAL/10), or DATA (state probes). The PRESCALE mode must be selected for measurements above 10 MHz (100 MHz maximum). For the NPC-764, the DATA mode allows measurements to be made on state events up to 56 bits wide. (38 bits wide for the NPC-748.)

In the INTERVAL mode, the SOURCE field allows the specification of START and STOP words, each 38-56 bits wide.

Line 4: **PROBE TYPE:** This field is displayed only in the FREQUENCY, PERIOD, and TOTAL modes--and only when the SOURCE field is EXTERNAL or PRESCALE (EXT/10). The two options are 10X and 1X, according to the setting of the Model 90 probe.

THRESHOLD: This field is available only when the PROBE TYPE field is displayed. When a 10X probe type is selected, the threshold for an incoming signal can be set between -2.56V and +2.54V, in 0.2V increments. When a 1X probe type is selected, the threshold can be set between -2.56V and +2.54V, in 0.02V increments.

5.7.1 COUNTER-TIMER DISPLAY

The counter-timer display is incorporated into the menu. To take a measurement of a signal, simply connect the appropriate probe(s). The frequency, time, or count of input events will appear in the rectangle on the screen. Also, the message COLLECTING appears below the reading to indicate the real-time nature of the current measurement. To "freeze" the measurement, press the HOLD (F4) key; the message HOLDING will then appear below the reading.

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5.8 SIGNATURE MENU

A. TO CALL UP MENU:

1. Press the **CONFIG** or **RESET** key.
2. Press the **SEL DOWN** or **SEL UP** key to select the **SIGNATURE ANALYZER** mode.
3. Press the **SELECT (F1)** key to call the menu.

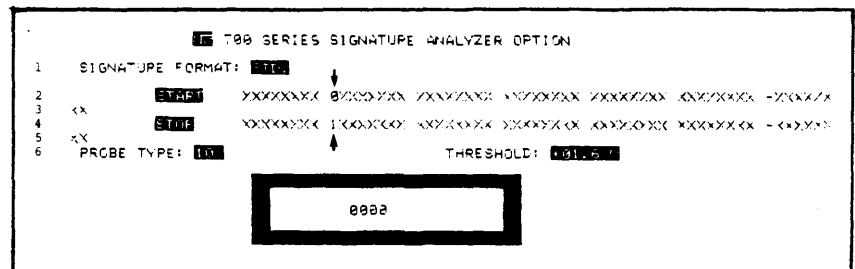


Figure 5-21. Use of single bit START and STOP words.

B. EXPLANATION OF MENU:

Line 1: **SIGNATURE FORMAT.** Two formats can be selected: STD or HEX. The STD format uses the 7-segment alphanumeric type of display of the HP-5004A Signature Analyzer (0-9, A, C, F, H, P, U). The HEX format displays the signatures in hexadecimal (0-9, A-F).

Lines 2-5: **START and STOP.** The START and STOP words gate the serial bit stream coming through the Model 90 probe. For the NPC-764, each word can be 1-56 bits wide. (38 bits wide for the NPC-748.) A logic zero in any bit position corresponds to (V) on the HP-5004A; while a logic one corresponds to (A).

The START and STOP words are automatically formatted in accordance with the user's display format in the 48-channel state menu. A single format can be selected using the HEX, OCT, BIN, DEC, or ASC keys.

Line 6: **PROBE TYPE:** The two options are 10X and 1X to match the corresponding setting of the Model 90 probe.

THRESHOLD: When a 10X probe type is selected, the threshold for an incoming signal can be set between -25.6V and +25.4V, in 0.2V increments. When a 1X probe type is selected, the threshold can be set between -2.56V and +2.54V, in 0.02V increments.

NOTE: In typical application, the clock used in conjunction with the serial bit stream being monitored should be derived from the A state probe. Set this clock for a rising or falling active edge in the state menu as appropriate. Make sure the B (and C) clock fields are set to A.

5.8.1 SIGNATURE DISPLAY

The signature display is incorporated into the menu. To take a signature of a serial bit stream being monitored by the Model 90 probe, simply touch the probe to the node and press the **COLLECT** key.

5.9 SERIAL ANALYZER

The NPC-700's serial testing capabilities require the use of the Model 70 Serial Probe. With this probe, **RECEIVE**, **EDIT** and **TRANSMIT** functions are possible. In the **RECEIVE** mode, the Model 70 converts incoming serial data to parallel words for collection by the state analyzer. Captured data can be displayed in ASCII or any other available format. In order to display received data in the menu in Figure 5-22, you must first transfer the collected data from the main state ASCII memory to the auxiliary memory. This is accomplished by pressing the **S (SAVE)** key after the data collection.

The **EDIT** and **TRANSMIT** modes operate on whatever ASCII characters are in the data field shown in Figure 5-22. The instructions for using these modes are contained in the menu itself. For additional details, consult the **Model 70 User's Instructions**, available from your nearest NPC sales office.

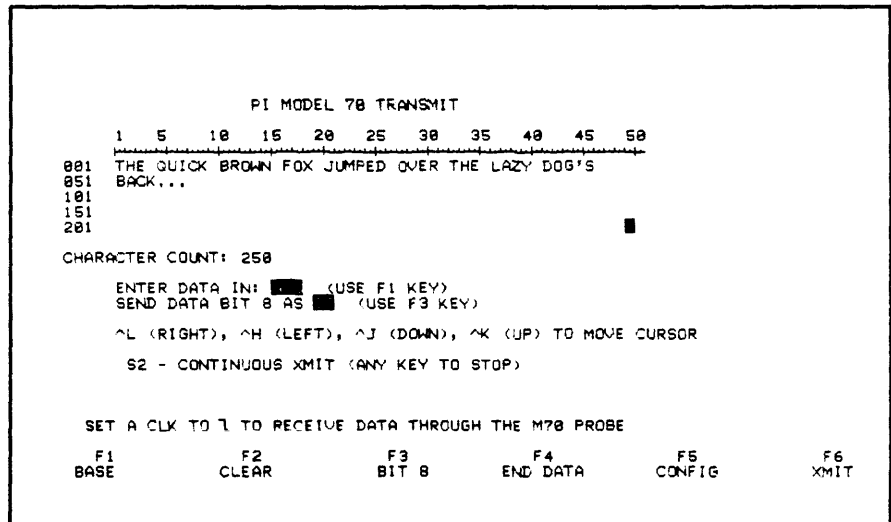


Figure 5-22. The Model 70 EDIT and TRANSMIT menu.

NOTE: The cursor commands shown in the menu: **CTRL L** (RIGHT) and **CTRL H** (LEFT), are used when the data entry base is hexadecimal or octal. When the data entry base is in ASCII, it's easier to use the **SPACEBAR** and **BACKSPACE** keys for simple editing.

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5.10 I/O CONFIGURATION MENU (NPC-764 ONLY)

A. TO CALL MENU:

1. Press the **CONFIG** or **RESET** key.
2. Press the **I** key.

```

                                     I/O CONFIGURATION MENU
1  INTERFACE: DISABLED * INTERFACE: ENABLED
2  ADDRESS: 04 * MODE: SLAVE
3  MODE: CONTROLLER * BAUD RATE: 1200
4  TERM SEQUENCE: 07 EOI OFF * PARITY: NONE DUPLEX: FULL
5  TALK: ON LISTEN: ON * WORD LENGTH: 8
6  RETURN OPTION: AUTO * STOP BITS: 1
*****
7  KEYBOARD: OFF * CRT: OFF
8  GPIB: OFF * GPIB: OFF
9  RS232: OFF * RS232: OFF
10 MEMORY: OFF * MEMORY: OFF
11
12 GPIB SLAVE ADDRESS: 00
13
14
15
16 F1 F2 F3 F4 F5 F6
17 PREVIOUS NEXT SELECT DEFAULT CONFIG TRANSMIT [ESC]
G - GPIB
R - RS232
I - INPUTS
O - OUTPUTS
D - DEFAULT ALL
```

Figure 5-23. I/O Menu.

B. EXPLANATION OF MENU:

GPIB Section

INTERFACE

Line 1: The **INTERFACE** field defaults to **ENABLED**. This allows the NPC-764 to be either a **CONTROLLER** or **DEVICE** on the GPIB bus. Pressing the **SELECT** key puts the interface into a **DISABLED** state in which the NPC-764 is effectively disconnected from the bus.

ADDRESS

Line 2: The **ADDRESS** field defines the address of the NPC-764 on the GPIB bus. Pressing the **SELECT** key increments the address of the device. Valid addresses are 00 through 30 (HEX). The default address is 04.

MODE

Line 3: The **MODE** field determines if the NPC-764 is a **DEVICE** or **CONTROLLER** on the GPIB bus. The default condition is set by switch 2 on the DIP switch located on the Processor Board. (See Figure 12-3.) The unit is a **CONTROLLER** if the switch is in the **OFF** position. (The switch is read during power up and when the **RESET** key is pressed. See Table 5-1.) Pressing the **SELECT** key changes the **MODE** to **DEVICE**.

Table 5-1. Power Up/Reset I/O Initialization.

RS-232		GPIB	
SWITCH 1		SWITCH 2	
ON	OFF	ON	OFF
SLAVE	MASTER	DEVICE	CONTROLLER

TERMINATION SEQUENCE

Line 4: The TERMINATION SEQUENCE field defines the end of data transmission. The flashing cursor will initially be placed in the ASCII character field. Pressing the **SELECT** key changes the sequence to C_RL_F (carriage return - line feed), C_R alone, L_F alone, or NULL (no ASCII characters). If NULL is selected, EOI ON will automatically be selected and cannot be changed. If NULL is not selected, pressing the **NEXT** key will move the flashing cursor to the EOI selection portion of the TERMINATION SEQUENCE. Pressing the **SELECT** key changes EOI to ON or OFF. If EOI ON is selected, EOI will be sent out with the last character of the termination sequence previously selected or with the last character of data if NULL was selected. The default states for the TERMINATION SEQUENCE field is C_RL_F and EOI OFF.

**TALK
LISTEN**

Line 5: These fields determine whether the NPC-764 is a TALKER, LISTENER, or both on the GPIB bus. These fields normally default to ON. With the ON cursor flashing, pressing the **SELECT** key disables the function and sets the field to OFF.

RETURN OPTION

Line 6: The RETURN OPTION field defines the way in which the NPC-764 returns to the CP/M calling program from the ANALYZER mode. The field defaults to AUTO. Pressing the **SELECT** key changes the field from AUTO to AUTO/MAN, to MANUAL. In the AUTO mode, the return to CP/M will take place immediately after the command string has been executed by the analyzer. In the MANUAL mode, the return to CP/M will take place when the R key is pressed. (The R key is not defined in this menu.) In the AUTO/MAN mode, the return to CP/M will take place immediately after the command string has been executed by the analyzer, except when a data collection is being initiated by the command string. After data collection is completed, the return to CP/M will be the same as described above for the MANUAL mode.

RS-232 Section

INTERFACE

Line 1: The INTERFACE field defaults to ENABLED which allows the NPC-764 to communicate with other devices via an RS-232 bus. After accessing this field, pressing the **SELECT** key puts the interface into a DISABLED state which effectively disconnects the device from the bus. If the ENABLED mode is selected, the NPC-764 can either be a MASTER or SLAVE on the bus.

SECTION 5.0

MENUS AND DISPLAYS

MODE

Line 2: The MODE field allows you to reconfigure the NPC-764 as the MASTER or SLAVE on an RS-232 bus. The default condition is set by switch 1 on the DIP switch located on the Processor Board. (See Figure 12-3.) The unit is a MASTER if the switch is in the OFF position. (The switch is read during power up and when the **RESET** key is pressed. See Table 5-1.) A third mode of operation, MASTER/ECHO, is also available. This mode is identical to MASTER, except that all commands executed by the NPC-764 are echoed from the RS-232 port (except when in the I/O configuration menu). This feature is useful when it is desired to set up the MASTER and SLAVE in the same configuration, or to simply see the SLAVE's menus when entering commands manually. The **SELECT** key changes the mode from SLAVE to MASTER to MASTER/ECHO.

Line 3: The BAUD RATE field defines the RS-232 transmission rate. The field defaults to 1200. Use the following keys to select the desired BAUD RATE:

Table 5-2. Baud Rate Select

<u>KEY</u>	<u>BAUD RATE</u>
1	110
2	150
3	300
4	600
5	1200
6	2400
7	4800
8	9600

NOTE: This information is displayed on the CRT when the BAUD RATE field is activated.

PARITY

Line 4: The PARITY field defaults to NONE. Pressing the **SELECT** key allows you to set the PARITY to NONE, ODD, EVEN, MARK, or SPACE.

DUPLEX

Line 4: The DUPLEX field defaults to FULL which enables the echo mode for the RS-232 interface. Pressing the **SELECT** key allows you to set the DUPLEX field to HALF or FULL.

WORD LENGTH

Line 5: The WORD LENGTH field defaults to 8. Pressing the **SELECT** key allows you to set the WORD LENGTH to 8, 7, 6, or 5 bits.

STOP BITS

Line 6: The STOP BITS field defaults to 1. Pressing the **SELECT** key allows you to set the number of STOP BITS to 1 or 2. Note that some combinations of parity and word length force the number of stop bits to a specific state. For example, if the word length is selected to be 8 and parity is selected, 1 stop bit is sent even though 2 stop bits may have been selected; if the word length is 5 and no parity is selected, 1.5 stop bits are sent if 2 stop bits are selected.

Transmission Inputs Section

This section defines the source(s) of data that will be sent to the interface or memory defined in the TRANSMISSION OUTPUTS section, described below.

KEYBOARD

Line 7: The KEYBOARD field normally defaults to OFF. The keyboard can only be used to configure and control the analyzer in the OFF state. With the OFF cursor flashing, pressing the **SELECT** key turns the KEYBOARD field ON to transmit data to the interface(s) selected in the TRANSMISSION OUTPUTS section.

GPIB

Line 8: The GPIB field normally defaults to OFF. If the INTERFACE field in the GPIB section of the menu is DISABLED, the GPIB field will be forced to OFF and cannot be changed. With the OFF cursor flashing, pressing the **SELECT** key turns this field ON and enables the NPC-764 to receive data from another device over the GPIB bus and send data to the destination(s) selected in the TRANSMISSION OUTPUTS section.

RS-232

Line 9: The RS-232 field normally defaults to OFF. If the INTERFACE field in the RS-232 section of the menu is DISABLED, the RS-232 field will be forced to OFF and cannot be changed. With the OFF cursor flashing, pressing the **SELECT** key turns this field ON and enables the NPC-764 to receive data from another device over the RS-232 interface and send data to the destination(s) selected in the TRANSMISSION OUTPUTS section.

MEMORY

Line 10: The MEMORY field normally defaults to OFF. If the MODE field in the GPIB section is set to DEVICE and the mode field in the RS-232 section is set to SLAVE, the field will be forced to OFF and cannot be changed. With the OFF cursor flashing, pressing the **SELECT** key will provide several combinations of memory data to be transmitted over the GPIB or RS-232 interfaces. With the field flashing, pressing the **SELECT** key allows you to select the TIMING or STATE memory to be transmitted. Pressing the **NEXT** key moves the flashing cursor to the SETUP field. With the SETUP field flashing, pressing the **SELECT** key allows you to select the memory type to be transmitted. The choices are SETUP, DATA, or AUX. Pressing the **DEFAULT** key when either field is flashing will set both fields to OFF.

Transmission Outputs Section

CRT

Line 7: The CRT field normally defaults to OFF. The CRT will display configuration menus and data collection displays in the OFF state. With the OFF cursor flashing, pressing the **SELECT** key turns the CRT ON to display data received on the interface(s) selected in the TRANSMISSION INPUTS section.

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MENUS AND DISPLAYS

GPIB

Line 8: The GPIB field normally defaults to OFF. If the INTERFACE field in the GPIB section of the menu is DISABLED, the GPIB field will be forced to OFF and cannot be changed. With the OFF cursor flashing, pressing the SELECT key turns this field ON and enables the NPC-764 to transmit data to another device over the GPIB bus. The data sent will be from the source(s) selected in the TRANSMISSION INPUTS section.

RS-232

Line 9: The RS-232 field normally defaults to OFF. If the INTERFACE field in the RS-232 section of the menu is DISABLED, the RS-232 field will be forced to OFF and cannot be changed. With the OFF cursor flashing, pressing the SELECT key turns this field ON and enables the NPC-764 to transmit data to another device over the RS-232 interface. The data sent will be from the source(s) selected in the TRANSMISSION INPUTS section.

MEMORY

Line 10: The MEMORY field normally defaults to OFF. If the MODE field in the GPIB section is set to DEVICE and the MODE field in the RS-232 section is set to SLAVE, the field will be forced to OFF and cannot be changed. With the OFF cursor flashing, pressing the SELECT key will provide several combinations of memory to receive data from another NPC-764 over the interface selected in the TRANSMISSION INPUTS section. With the field flashing, pressing the SELECT key allows you to select the TIMING OR STATE memory to receive the data. Pressing the NEXT key moves the flashing cursor to the SETUP field. With the SETUP field flashing, pressing the SELECT key allows you to select the memory type to receive data. The choices are SETUP, DATA, or AUX. Pressing the DEFAULT key when either field is flashing will set both fields to OFF.

GPIB SLAVE ADDRESS

Line 12: The GPIB SLAVE ADDRESS field will be displayed only if the MODE field in the GPIB section is set to CONTROLLER. Pressing the SELECT key increments the address. Valid addresses are 00 through 30 (HEX). The field defines the GPIB address of another NPC-764 (or other device*) to which the data or memory block will be sent as defined in the TRANSMISSION INPUTS or OUTPUTS section.

LABELS

Lines 11 to 15: These fields are labels to define the functions of direct entry keys. Pressing G, R, I, or O will move the flashing cursor to the associated section of the menu. Pressing D will set every field to its default state.

* The format of the transferred data is unique and only a NPC-700 can use it without translation.

If MEMORY input or MEMORY output is selected, the **TRANSMIT** key will initiate the data transmission. The field will show **TRANSMIT ON** during transmission and will change back to **TRANSMIT OFF** upon transmission completion.

NOTE: Only one MEMORY (input or output) is allowed to be selected. The other MEMORY will be forced to OFF.

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SECTION 6.0

ANALYSIS EXAMPLES

6.0 ANALYSIS EXAMPLES

The NPC-700 was designed for ease-of-use. Upon application of power, the Analyzer's ROM-based Operating System will display the CONFIGURATION LIST illustrated in Figure 6-1. This section of the manual provides the user with examples representing operational modes from this list.

```
NR  NICOLET PARATRONICS 764 CONFIGURATION  VER 4.0
    1 - 48 CHNL STATE
    2 - 16 CHNL TIMING
    3 - 48 CHNL STATE/16 CHNL TIMING
    4 - 8 CHNL TIMING (100MHZ 2000 WORD)
    5 - 48 CHNL STATE/8 CHNL TIMING
    6 - 8 CHNL TIMING GLITCH
    7 - 48 CHNL STATE/8 CHNL GLITCH
    8 - WAVEFORM RECORDER
    9 - 48 CHNL STATE/WAVEFORM
   10 - COUNTER/TIMER
   11 - SIGNATURE ANALYZER
   12 - PI 70 SERIAL PROBE TRANSMIT

ESC - DISK OPERATING SYSTEM
BREAK - PROCESSOR SELF-TEST
I - I/O CONFIGURATION MENU
```

Figure 6-1. Configuration List. (NPC-764 shown)

The analysis examples in this section, are structured for progressive self-study in that each step "builds" on the previous step. The Logic Analyzer Test Card, included with each NPC-700, provides a known stimulus to the analyzer so that a given test set-up will result in a predictable response.

If you have any questions, please feel free to call Nicolet Paratronics' Applications Engineers at:

(800) 642-6538 (Toll-free outside California)
(415) 490-8300 (California)
(910) 381-7030 (TWX)

6.1 TEST CARD DESCRIPTION

The Logic Analyzer Test Card is provided to allow you and your co-workers to rapidly familiarize yourselves with the basic and advanced features of the instrument.

The Logic Analyzer Test Card consists of two 8-bit CMOS counters (A and B), a clock, and simple decoding logic. See Figure 6-2. Each CMOS counter normally counts from (00)HEX to (FF)HEX. When the A counter reaches (40)HEX, the decode logic resets the B counter to (00)HEX.

The test card's A channel connector is wired so that the 8 least significant bits toggle in a sequential fashion; while the 8 most significant bits are tied to ground. Therefore, the A channel connector provides a 16-bit word which covers the range from (0000)HEX to (00FF)HEX.

The test card's B channel connector is wired so that its 16 output bits toggle nonsequentially. A typical binary count sequence at the B channel connector is:

COUNT	BINARY PATTERN*	HEX PATTERN
0	00000000 00000000	00 00
1	10000000 00000001	80 01
2	01000000 00000010	40 02
3	11000000 00000011	C0 03
.	.	..
.	.	..
.	.	..
15	11110000 00001111	F0 0F

Power to the test card is supplied by the +5V output at each probe connector.

The A counter is generally used as a signal source for the one state or timing probe while the B counter output feeds the second state or timing probe. For the NPC-764, the third 16-channel state probe is not normally connected to the test card.

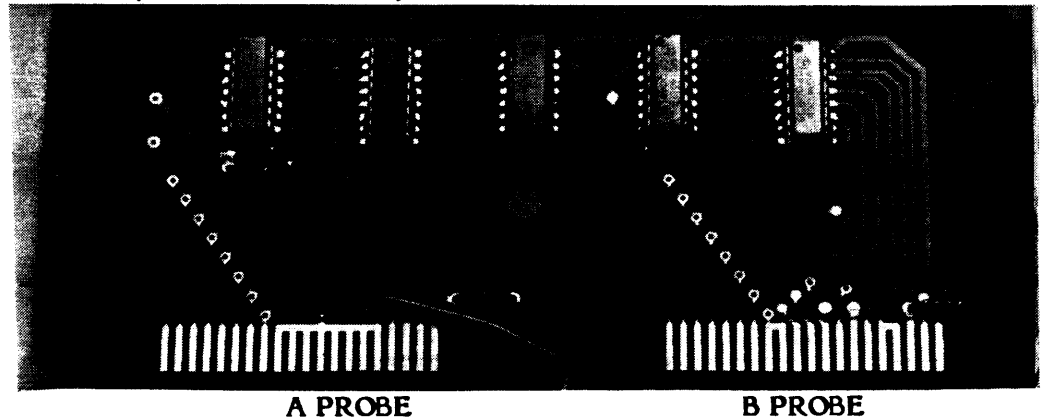


Figure 6-2. Test card layout.

***NOTE:** Due to the difference in pin-outs between the 16-channel state probes and the 8-channel timing probes, this exact pattern will only be displayed on the NPC-700 when using the state probe.

6.2 BASIC ANALYSIS EXAMPLES

The purpose of this basic test is to show how simple it is to set up the NPC-700 to collect STATE, TIMING, and other data.

The six "soft" function keys labeled F1 to F6, from left to right, are identified by labels on the bottom line of the CRT. These labels differ from menu to menu, as selected with the **SEL DOWN** or the **SEL UP** keys. Each menu defaults to the most commonly-used parameters so that a first-time user can immediately collect data. Also, a flashing error message indicates when an invalid key is pressed and tells the operator which keys are valid for the current operation.

6.2.1 BASIC STATE ANALYSIS

In order to illustrate the basic state analysis capabilities of the NPC-700, the user need only select the menu, enter in a trigger word, and press the **COLLECT (F6)** key. Captured data can then be formatted in a variety of ways.

SET-UP

Connect the two state probes to the NPC-700. Note that the A probe connector is located toward the rear of the analyzer. For the NPC-764, leave the C probe disconnected.

Connect the A probe to the left-hand connector of the test card and the second probe to the right-hand connector. Set both probes for **TRUE** and **TTL** operation.

Turn the NPC-700's power switch on to produce the **CONFIGURATION LIST** illustrated in Figure 6-1. Select the **STATE** menu by pressing the **STATE (F1)** key. See Figure 6-3.

TRIGGER (0040)

The state menu should be set up with the default values in all fields except the trigger word field. Advance the blinking cursor to the trigger stack field, level 0, with the **NEXT (F2)** key. Press the **H** key to format this field for a hexadecimal trigger word. Now type in the following trigger word: **0040**. Observe from the labels field at the lower right corner of the CRT that other formats can be selected using the indicated keys.

```

                                48 CHANNEL STATE MENU
FORMAT: AAAAAAAAAA AAAAAAAAAA AAAAAAAAAA AAAAAAAAAA AAAAAAAAAA AAAAAAAAAA
        A HEX
CLK SEL: A PRB: J B PRB: A C PRB: A QUALIFIERS: -AABBCC EL
CLK QUAL: OFF
        OR OFF
PRE-TRIG MEMORY (0-999): 000 WORDS
RESTART: OFF
TRIGGER:
0      00 40 XX XX XX XX -XXXXXX XX
END

```

H - HEX
 O - OCTAL
 Z - DEC
 N - BINAR
 Y - ASCII
 U - USER

S1 - DATA DISPLAY
 F1 PREVIOUS F2 NEXT F3 F4 F5 CONFIG F6 COLLECT

Figure 6-3. State menu with 0040 selected as the trigger word. (NPC-764 shown.)

COLLECT

Press the **COLLECT (F6)** key to take a data collection. With state data displayed, the word labeled TRIG at the top of the CRT should be **0040** for the 4 most significant digits. (Ignore the rest of the word for now.) Press the **LABELS** key. Then format the display in octal, decimal, binary, and ASCII by pressing the **O**, **Z**, **N**, and **Y** keys in turn. Press the **H** key for the hexadecimal format. See Figure 6-4.

AUTOCOLLECT

Press **CTRL** and **C** simultaneously to activate an automatically repeating data collection mode. Press any **ASCII** key to stop.

SCROLL

Scroll the display up and down by pressing the **SCRL UP (F2)** or **SPACEBAR** key and then the **SCRL DWN (F1)** or **BACKSPACE** key. Rapid scrolling is accomplished by pressing either scrolling key and the **REPEAT** key simultaneously.* Locate the end of the data collection by pressing the **LOCATE (F3)** key followed by the **E** key. Then locate word +101 by pressing **LOCATE** and typing **+101**. (Remember to **SHIFT** to access the **+** key or use the **SPACEBAR** to step through the **+** field.) Finish with the trigger word at the top of the CRT by pressing **LOCATE** and **T**.

HINT: If you press the wrong key and get an error message, you can use the **BACKSPACE** and **SPACEBAR** keys to edit the **LOCATE** field. Alternatively, you can press **S1** to clear the field.

***NOTE:** Newer NPC-700's have an **AUTOREPEAT** keyboard. Holding any single key depressed for more than approximately one second activates this function.

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ANALYSIS EXAMPLES

```

MAIN      TRIG 00 40 00 00 FF FF
          +001 00 41 80 01 FF FF
LOC: 1471 +002 00 42 40 02 FF FF
          +003 00 43 C0 03 FF FF
SIG: C1E7 +004 00 44 20 04 FF FF
      19E7 +005 00 45 A0 05 FF FF
      D3D3 +006 00 46 60 06 FF FF
          +007 00 47 E0 07 FF FF
          +008 00 48 10 08 FF FF
          +009 00 49 90 09 FF FF
          +010 00 4A 50 0A FF FF
          +011 00 4B D0 0B FF FF
          +012 00 4C 30 0C FF FF
          +013 00 4D B0 0D FF FF
          +014 00 4E 70 0E FF FF
          +015 00 4F F0 0F FF FF
          +016 00 50 00 10 FF FF
          +017 00 51 80 11 FF FF
          +018 00 52 40 12 FF FF
          +019 00 53 C0 13 FF FF

M E N U
PC - CLK CL
PT - PRETRG
T - TRIG

RAM - MEMSEL
      - SAVE
      - REDALL

H - HEX
      - OCTAL
      - DEC
      - BIN
      - ASCII
      - USER

# - HOLD#
      - DIFFER
      - SRCH UP
      - SRCH DN

F1  SCRL DOWN      F2  SCRL UP      F3  LOCATE      F4  SRCH WRD      F5  CONFIG      F6  COLLECT

```

Figure 6-4. State data in HEX format. (NPC-764 shown.)

SAVING DATA (S Key)

To illustrate the SAVE mode, press the LABELS key in the top row. Perform the SAVE function by pressing the S key. This action causes the entire data collection, the test codes (SIG), and the menu parameters to be stored in the NPC-700's auxiliary RAM memory. (Notice the flashing SAVED message.) Now press the M key (MEMSEL) to cause the auxiliary memory to be displayed. Press M again to return the main memory to the screen. Both memories should now contain identical signatures.

HOLD# MODE (# Key)

The HOLD# mode is used to detect and isolate intermittent faults. Press the # key (SHIFT and 3) to activate the HOLD# mode. Note the flashing status messages which indicate that the analyzer is automatically collecting 1000 words and comparing main and auxiliary data.

Hold the shorting wire on pad 5 on the right-hand side (B side) of the test card. Note that the flashing status message now reads HOLDING, and data are displayed. Remove the shorting wire from pad 5.

COMPARE (M Key)

Press the M key to compare main and auxiliary test codes. Notice that one of the main memory test codes differs from the corresponding auxiliary memory test code. This indicates that somewhere in the new data collection, there are one or more bits that differ between the main and auxiliary memories. Now return to the main memory.

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ANALYSIS EXAMPLES

```
MAIN      +681 00000000 11101001 10010101 10101001 11111111 11111111
+682 00000000 11101010 01010101 10101010 11111111 11111111
LOC:      +683 00000000 11101011 11010101 10101011 11111111 11111111
+684 00000000 11101100 00110101 10101100 11111111 11111111
SIG: DIET +685 00000000 11101101 10110101 10101101 11111111 11111111
      ERAT +686 00000000 11101110 01110101 10101110 11111111 11111111
      DSOS +687 00000000 11101111 11110101 10101111 11111111 11111111
+688 00000000 11110000 00001101 10110000 11111111 11111111
+689 00000000 11110001 10001101 10110001 11111111 11111111
+690 00000000 11110010 01001101 10110010 11111111 11111111
+691 00000000 11110011 11001101 10110011 11111111 11111111
DIFFERENCE +692 00000000 11110100 00101101 10110100 11111111 11111111
+693 00000000 11110101 10101101 10110101 11111111 11111111
+694 00000000 11110110 01101101 10110110 11111111 11111111
+695 00000000 11110111 11101101 10110111 11111111 11111111
+696 00000000 11111000 00011101 10111000 11111111 11111111
+697 00000000 11111001 10011101 10111001 11111111 11111111
+698 00000000 11111010 01011101 10111010 11111111 11111111
+699 00000000 11111011 11011101 10111011 11111111 11111111
+700 00000000 11111100 00111001 10011100 11111111 11111111
      ↑      ↑
```

Figure 6-6. Using the M (MEMSEL) key to identify which bits were affected by the short on pad 5. (NPC-764 shown.)

LOCATE DIFFERENCE (LOCATE + D)

Return to the main memory and press the H key. Press **LOCATE (F3)** followed by **D** to place the first difference word at the top of the screen. (This is an alternative and faster way of locating the first difference word.) Now press **LOCATE** followed by **S** to find the next group of half-intensified words that are the "same" (if any). Press the **SCRL DWN (F1)** key once to verify this. See Figure 6-7. (NPC-764 shown.)

Press **LOCATE** followed by **T** to place the trigger word at the top of the CRT. Then press the / key to disable the difference mode.

MAIN	+703	00	FF	F9	9F	FF	FF	←
	+704	00	00	03	00	FF	FF	
LOC:	+705	00	01	03	01	FF	FF	
	+706	00	02	43	02	FF	FF	
SIG: C1E7	+707	00	03	03	03	FF	FF	
79E7	+708	00	04	23	04	FF	FF	
D8D3	+709	00	05	A3	05	FF	FF	
	+710	00	06	63	06	FF	FF	
	+711	00	07	E3	07	FF	FF	
	+712	00	08	13	08	FF	FF	
	+713	00	09	53	09	FF	FF	
DIFFERENCE	+714	00	0A	93	0A	FF	FF	
	+715	00	0B	D3	0B	FF	FF	
	+716	00	0C	33	0C	FF	FF	
	+717	00	0D	73	0D	FF	FF	
	+718	00	0E	B3	0E	FF	FF	
	+719	00	0F	F3	0F	FF	FF	
	+720	00	10	00	D0	FF	FF	
	+721	00	11	30	D1	FF	FF	
	+722	00	12	40	D2	FF	FF	

Figure 6-7. In this particular example, word +704 is the first word in the next group of data words that are the "same." (Your example will probably turn out differently.)

SEARCH WORD

The SEARCH WORD mode allows you to locate any particular bit pattern within a data collection; you specify the word to search for and then the direction of search.

Press the **SRCH WRD (F4)** key to obtain the menu shown in Figure 6-8.

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ANALYSIS EXAMPLES

```
FORMAT:  AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA
          A HEX
SEARCH WORD:
          009EXXXXXXXX
```

Figure 6-8. SEARCH WORD menu with 009E as the search word. (NPC-764 shown.)

K, J

In the example, 009E is used as the word to be found in the data collection. Type in 0-0-9-E (the rest of the field are X's--DON'T CARE.) Press S1 to display the data again, then press K to search the data for 009E. See Figure 6-9. Press K again to search for additional occurrences of 009E further down in the memory. Press J to search in the opposite direction.

NOTE: This is a good stopping point if you wish to power down.

MAIN	00 9E 7A 5E FF FF
LOC: 009E	00 9F FA 5F FF FF
	00 A0 06 60 FF FF
	00 A1 86 61 FF FF
SIG: 081F	00 A2 46 62 FF FF
D1A6	00 A3 C6 63 FF FF
100F	00 A4 26 64 FF FF
	00 A5 A6 65 FF FF
	00 A6 66 66 FF FF
	00 A7 E6 67 FF FF
	00 A8 16 68 FF FF
	00 A9 96 69 FF FF
	00 AA 56 6A FF FF
	00 AB D6 6B FF FF
	00 AC 36 6C FF FF
	00 AD B6 6D FF FF
	00 AE 76 6E FF FF
	00 AF F6 6F FF FF
	00 B0 0E 70 FF FF
	00 B1 8E 71 FF FF

**Figure 6-9. SEARCH WORD 009E at the top of the display.
(NPC-764 shown.)**

6.2.2 BASIC TIMING ANALYSIS

In order to illustrate the basic timing analysis capabilities of the NPC-700, the user need only select the menu, choose a sampling clock and a trigger point, and press the **COLLECT (F6)** key.

SET UP

Before starting this test, connect the two A and B Model 80 Timing Probes to the NPC-700. Then connect these probes to the Test Card's A and B outputs, respectively. (You can leave the state probes plugged into the NPC-700.)

CLOCK AND TRIGGER

Press the **F5** key to return to the CONFIGURATION LIST. Now select the 16-CHANNEL TIMING mode by pressing the **SEL DOWN (F4)** key. Call the menu with the **TIMING (F1)** key; the cursor should be at the CLOCK field. Select an external clock with a rising (positive) edge by pressing **P**. Use the **NEXT (F2)** key to step to the TRIG field (above INPUT MODE) and specify a trigger word of **0-0-0-0-0-0-0 0-0-0-1-1-0-0-0** (i.e., **(0018)HEX**). Use the **NEXT** key to step down to the PRETRIGGER field. Set this field to **00%**. Leave all other menu parameters set at their default values as shown in Figure 6-10. Press the **COLLECT (F6)** key. Notice a brief status message TRIGGERED appearing in the lower left corner of the CRT screen. When a timing data collection is complete, the message "DONE" is displayed briefly in its place, and the screen fills with the timing diagram display. Press the **LABELS** key to call the DISPLAY menu. See Figure 6-11.

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```
16 CHNL TIMING/STATE MENU
EXT J CLOCK CLK QUAL: X
TRIGGER WHEN: TRIG OCCURS > 0000 CLOCKS AFTER FIRST ARM
              CHNL NO. A76543210 B76543210 FILTER LINKAGE
ARM (0.1.X):   XXXXXXXX XXXXXXXX OFF NONE
TRIG (0.1.X):  00000000 00011000 OFF NONE
INPUT MODE (S,L): SSSSSSSS SSSSSSSS
PRE-TRIGGER (0-9): 00%
DISPLAY ORDER (0-7.X): AAAAAAAAA BBBB8888
DISPLAY POLARITY (+,-): ++++++++ ++++++++
THRESHOLD:      A PROBE      B PROBE      HYSTERESIS
(-6.4V - +6.35V) +1.60      +1.60      ON
```

Figure 6-10 Timing menu with 00000000 00011000 as the trigger word and 00% pretrigger.

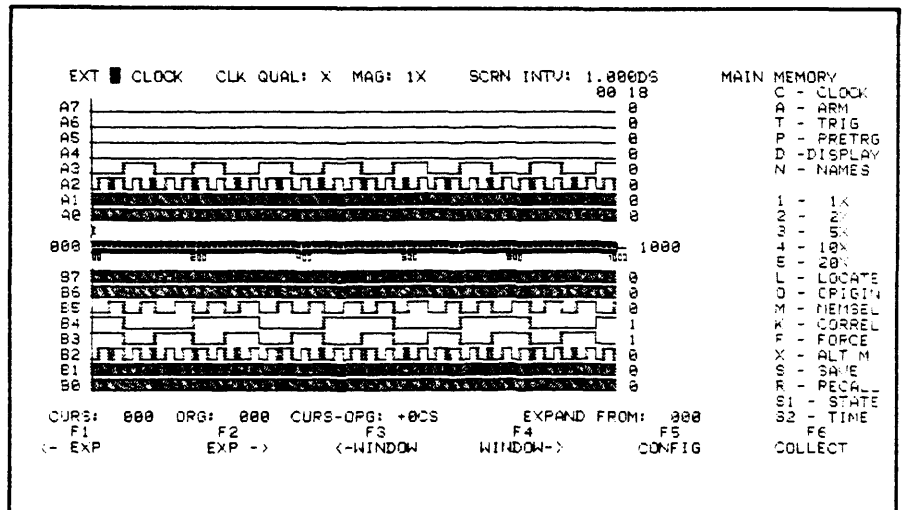


Figure 6-11. Timing diagram display at 1X magnification.

DISPLAY

The horizontal inverse video graticule at the middle of the display in Figure 6-11 represents the entire 1000 samples in the memory. Note that the small 00 indicator at the left end of the graticule is intensified, indicating the 00% pretrigger value set in previously. With 00% pretrigger, the first word in the data collection always is the trigger word. The cursor reads the binary and hexadecimal values of each location in the data memory where the cursor is placed. Thus, the trigger word at cursor location 000 should be (0018)HEX. In Figure 6-11, this trigger word appears at the upper right-hand-corner of the CRT.

Figure 6-11 also shows the sixteen timing channels and the corresponding binary values at cursor location 000. Note that the four most significant A channels (A7-A4) are at ground as described in Section 6.1. Also note that the cross-hatched areas on certain channels indicate that data in the memory are occurring too close together at the current X1 magnification factor to be resolved **visually**. (However, cursor values at the right of the CRT are always valid at **all** magnification factors.)

**EXPAND
(E)**

Sweep the expansion symbol, Ξ , towards the middle of the CRT by pressing F2. Stop the symbol at location 500 as indicated by the EXPAND FROM: readout in the lower right-hand portion of the CRT. (Use the F1 key to step back if you overshoot.) See Figure 6-12.

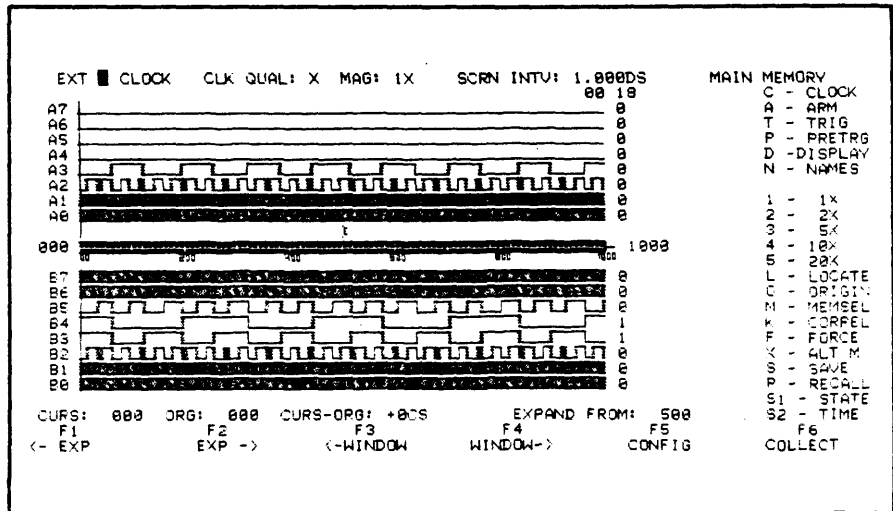


Figure 6-12. Timing display with the expansion symbol, Ξ , at location 500.

MAGNIFICATION

Try magnification factors between 2X to 20X using the 2 to 5 numeric keys as indicated in the DISPLAY MENU. After each higher magnification key is pressed, the inverse video indicator at the bottom of the screen reduces proportionately in size. This indicator shows the location and amount of timing data currently being displayed relative to the entire 1000-word data collection. At 20X magnification, note that the inverse video indicator is only 5% of its original (1X) size and that the screen is now displaying timing data between memory locations 500 and 550. See Figure 6-13.

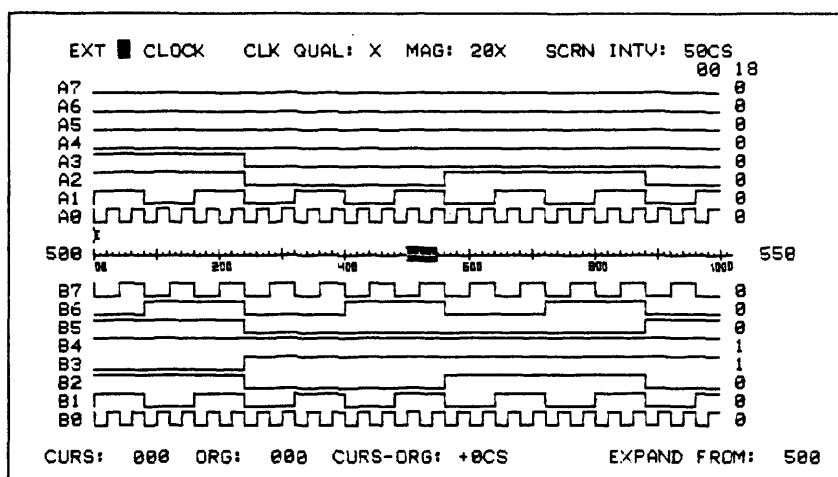


Figure 6-13. Timing display at 20X magnification.

WINDOW

View other segments of the memory by pressing the **<-WINDOW (F3)** or the **WINDOW-> (F4)** keys. Return to a data window of 500 to 550 as shown in Figure 6-13. Also return the expansion symbol to the left-hand side of the CRT.

CURSOR

To quickly set the cursor (which is currently at 000) to the left side of the screen, simply press the **L (LOCATE CURSOR)** key as indicated in the **LABELS** menu. Bring the cursor to the approximate center of the CRT by pressing the **SPACE BAR** key. (Overshooting can be remedied by pressing the **BACKSPACE** key.)

NAMES

Press the **N** key to activate the NAME cursor at the upper right-hand side of the screen. Experiment with naming each of the timing channels. You can use any alphanumeric name up to 8 characters. Use the **SPACEBAR** and **BACKSPACE** keys for editing. Press the **ESC** key to terminate name entry.

**TIME MEASUREMENTS
(O)**

In this step, you will measure the relative time between the edges in two channels. Visually select an edge (rising or falling) in channel A2 and another edge (later in time) in channel B6. Step the cursor so that it aligns with the selected edge in channel A2. Note the value of the cursor position indicator at the lower left of the screen. Now press the letter O to reset the origin from 000 to the current cursor location. The CURS-ORG indicator should now read +0CS, where CS stands for clock samples. (When an internal clock is being used, the indicator reads in units of time.) Next, step the cursor to the selected edge on channel B6. The CURS-ORG indicator will now directly read the time (in clock samples) between these two edges. Figure 6-14 shows one example of using this measurement procedure.

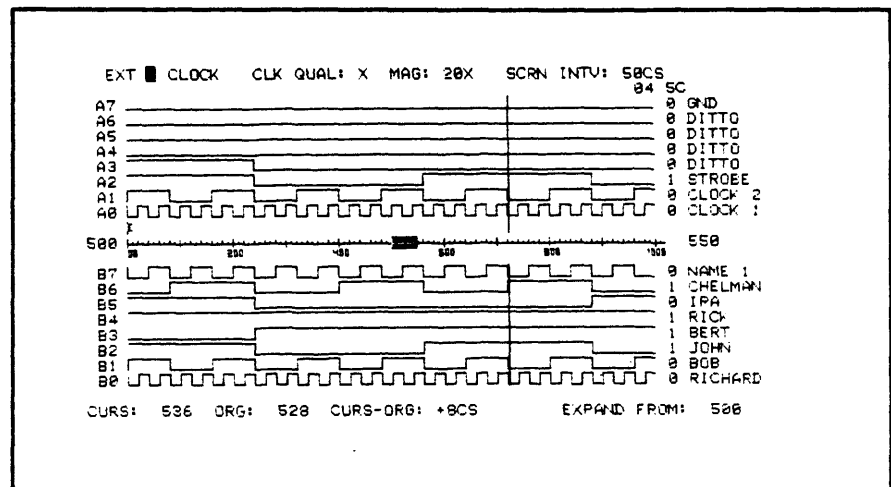


Figure 6-14. One example of measuring the relationship between timing data edges. (Your example may differ.)

**CORRELATION
(K)**

Press the **SAVE (S)** key and observe the flashing SAVED message. Press the **K (CORREL)** key to compare main and auxiliary data. Note that a correlation factor of 1.000 is displayed at the right of each channel. This factor means that all 1000 bits associated with each main memory channel compares with the 1000 bits in the corresponding auxiliary memory channel on a bit-for-bit basis. See Figure 6-15. Thus, if a correlation factor of .995 were displayed, it would indicate that 5 bits out of 1000 were different.

Note that when the **K** key is pressed, the correlation factors replace the NAMES. To restore the NAMES, press **S2**.

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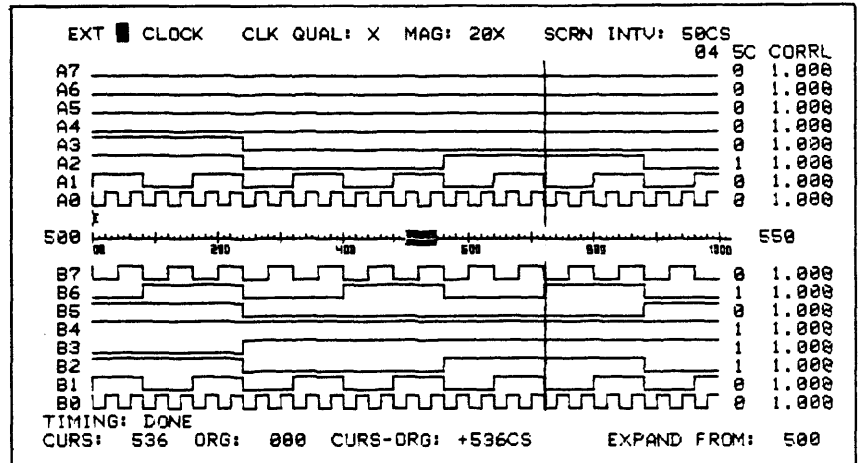


Figure 6-15. A correlation factor of 1.000 means that data in a main memory channel precisely matches the data in the corresponding auxiliary memory channel.

Now short out the pad labeled 5 on the B side of the demo card. While holding the short in place, press COLLECT. Now remove the short. To see which channel was affected by the short, again press K. Note that the correlation factor for channel B5 is significantly lower than 1.000. (The other channels still have correlation factors of 1.000 since an external, synchronous clock from the demo card was used in this example. If the internal, asynchronous clock were used, the correlation factors of the other channels would, in general, never be exactly 1.000 due to normal sampling uncertainties.)

MAIN/AUX MEMORY COMPARE (X)

In order to view the actual effect of the short on channel B5, press the X (ALT MEMORY) key. As shown in Figure 6-16, channel B5 should cycle between a 1 and a 0. Return to a X1 magnification by pressing the 1 key. (The main memory should be displayed.)

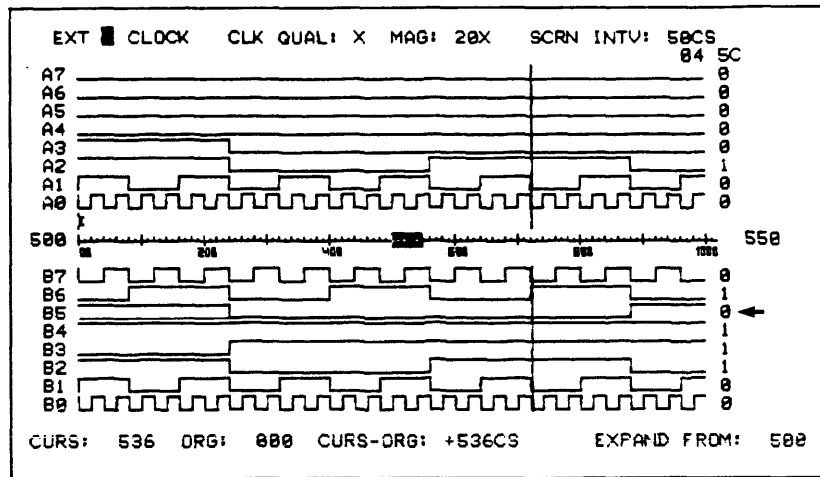


Figure 6-16. Using the MEMORY SELECT key to observe the effect of the short in channel B5.

STATE DISPLAY
S1
S2

To view the timing data in a state format, press S1. The state data can be displayed in HEX, OCTAL, DECIMAL, BINARY, or ASCII. Press the LABELS key to display the formats available in this mode. Return to the timing diagram display by pressing S2.

NOTE: This is a good stopping point if you wish to power down.

6.2.3 BASIC WAVEFORM ANALYSIS (OPTIONAL WAVEFORM ANALYZER MUST BE INSTALLED)*

To demonstrate the basic waveform recording features of the NPC-700, the user need only set the desired sample period, connect the scope probe to the waveform test point on the test card, and press COLLECT. After data collection, the captured waveform may be magnified, measured, and stored in a manner similar to the timing diagram display discussed above. In addition, voltage information is displayed.

WAVEFORM MODE

Press the CONFIG key and step down to the mode labeled WAVEFORM RECORDER. Press the WAVEFORM (F1) key to call the waveform menu. Connect the Model 90 scope probe to the WAVEFORM BNC at the rear of the NPC-700. Set the probe switch to the X10 position.

Note that the waveform menu contains typical oscilloscope-type parameters. Since the default values are not appropriate for this example, these values should be changed as shown in Figure 6-17.

***NOTE:** A baseline in the waveform display will not be present if the COLLECT key is pressed when this option is not installed.

AUTO-TRIGGER

In the above example, the waveform analyzer was in the auto-trigger mode. That is, the 1 μ S clock begins sampling the analog signal as soon as the **COLLECT** key is pressed without regard to the trigger level and slope of the signal. This free-running mode can be inhibited by setting the arm or trigger linkage field in the timing menu to **W**. In this manner, only incoming analog signals that meet the triggering conditions of the waveform menu will be collected. See Section 6.3.4, Advanced Waveform Examples, for additional information.

**6.2.4 BASIC COUNTER-TIMER/
SIGNATURE ANALYSIS
(OPTIONAL CT/SA BOARD
MUST BE INSTALLED)***

To demonstrate the basic features of the optional counter-timer and signature analysis functions of the NPC-700, the Model 90 probe is used to monitor signals on the test card. Connect the probe to the rear panel input connector labeled CTSA. Set the Model 90 probe for X10 operation.

**6.2.4.1 BASIC COUNTER/TIMER
EXAMPLE**

This section illustrates the use of the NPC-700 to make frequency (or period) measurements and totalize events using the Model 90 probe.

MENU

Press the **CONFIG** key and step down to the **COUNTER-TIMER** mode. Then press the **SELECT** key to display the **COUNTER-TIMER** menu. See Figure 6-19.

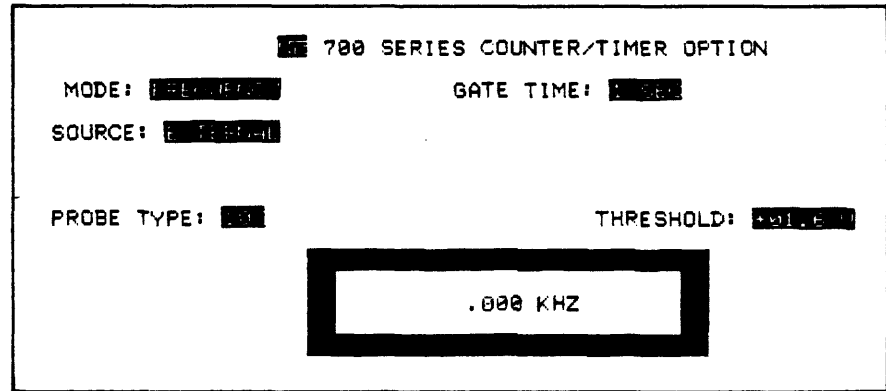


Figure 6-19. COUNTER-TIMER menu.

***NOTE:** The rectangular display window will be blank if the CT/SA option is not installed.

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FREQUENCY

When the counter-timer menu is first displayed, the cursor is automatically placed in the MODE field. Use the FREQUENCY mode for the next step.

You're now ready to make a frequency measurement. Take the probe and hold it on the data line DB0, on the test card (A channel side) and watch the NPC-700 as it displays the frequency. See Figure 6-20. Notice the message COLLECTING that appears under the counter-timer display, indicating that the NPC-700 is in a real-time measurement mode.

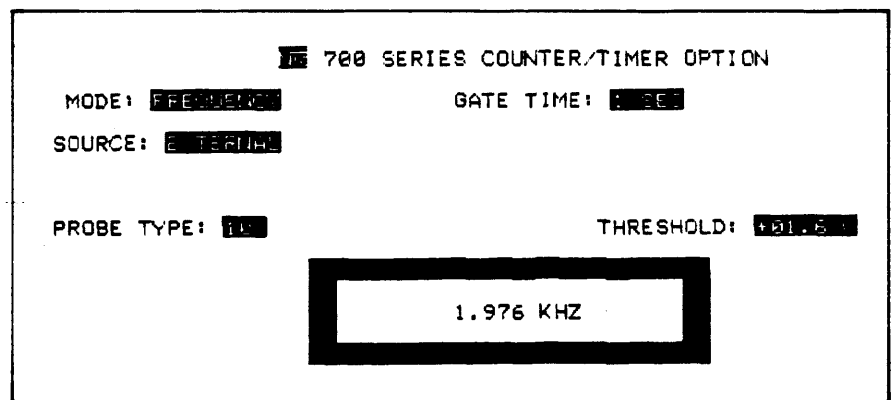


Figure 6-20. Frequency measurement using the counter-timer.

PERIOD

With the cursor in the MODE field and the probe still on DB0, use the SELECT key to change the mode to PERIOD. Notice that the display now measures in units of time (μsec) instead of frequency (KHz). Also, note that the GATE TIME field changes to RANGE when the mode is changed to PERIOD. The GATE TIME indicates the interval over which the frequency is measured and also the interval between display updates. The RANGE indicates the maximum period which can be measured. See Figure 6-21.

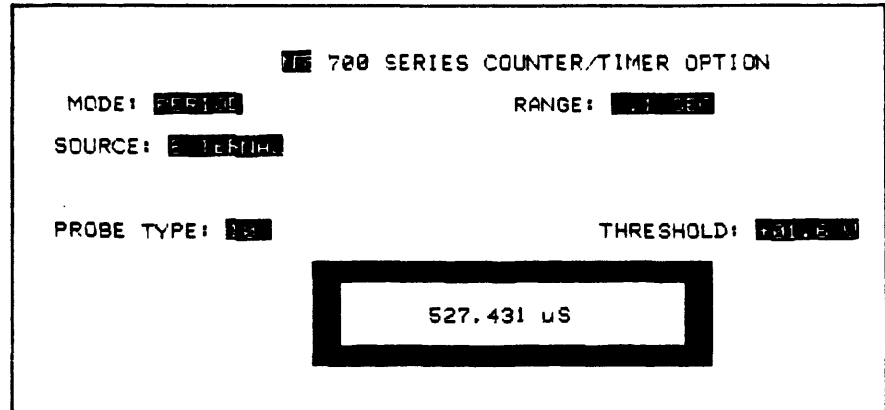


Figure 6-21. Period measurement using the counter-timer.

**FORCE DISPLAY
(F)**

Next, press the **HOLD** key (F4). This causes the display to hold the last measurement and displays the message **HOLDING** under the value. Press the **COLLECT** key to restart the counter-timer. The message **COLLECTING** will again appear under the counter-timer display.

PROBE AND THRESHOLD

The other two parameters which were used--**PROBE TYPE** and **THRESHOLD**--set the voltage range of the input signal. If the probe setting and menu are both set to 1X, the range of threshold settings which can be used is anywhere from -2.56V to +2.54V, in 0.02V increments. With a probe setting of 10X in the menu, and the Model 90 probe set to X10, the range of threshold voltages is from -25.6V to +25.4V, in .2V increments.

TOTAL

Another mode of operation for the counter-timer is the **TOTAL** mode. To activate the **TOTAL** mode, make sure the cursor is in the **MODE** field and press the **SELECT** key as required. The events monitored can be from the Model 90 probe, from the state probes, or from the external and linkage bits.

INTERVAL

Still another mode is the **INTERVAL** mode. This mode is used to measure the time between state events and is described in Section 6.3.5.

**6.2.4.2 BASIC SIGNATURE
ANALYSIS EXAMPLE**

This section illustrates the basic signature analyzer features of the optional Counter-Timer/Signature Analyzer board. The NPC-764 can be used to perform the function of a traditional signature analyzer (Hewlett Packard 5004A or equivalent) which uses individual lines for start, stop, and clock signals. See Section 6.3.5.2 and below for additional discussion of the **START** and **STOP** signals.

SECTION 6.0

ANALYSIS EXAMPLES

DISCUSSION

Briefly, signature analysis is a trouble-shooting technique which uses a data compression algorithm to reduce a complex, serial data stream to a unique 4-digit signature. To develop a signature, a START bit, STOP bit, CLOCK, and a serial data signal are required. In most signature analyzers, each of these signals requires a single line connected to the circuit board being tested.

By comparison, the NPC-700 allows the use of up to 56 bits to define the START and STOP signals. (See Section 6.3.5.2.) The CLOCK signal is specified in the state menu (A, B, and C clock edges and clock qualifiers) and the serial data signal is provided through the Model 90 probe connected to the rear panel input connector labeled CTSA.

The NPC-700's signature analyzer allows variable-threshold signal levels to be input to the serial data probe for testing logic other than TTL (i.e., ECL). It also allows a variable threshold implementation of start, STOP, and CLOCK signals using the adjustable threshold feature of the analyzer's probes.

SIGNATURE ANALYZER MODE

Press the **CONFIG** key and step down to the SIGNATURE ANALYZER mode. Press the **SELECT** key to display the SIGNATURE menu. See Figure 6-22. The fields of the SIGNATURE menu are SIGNATURE FORMAT, START and STOP words, PROBE TYPE and THRESHOLD.

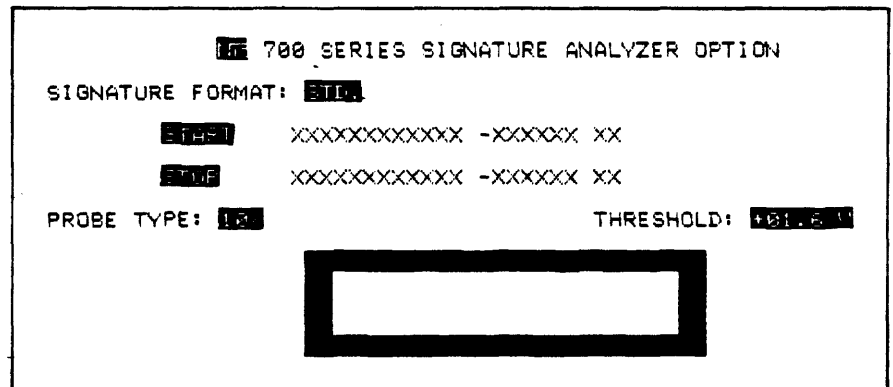


Figure 6-22. Signature analyzer menu and display. (NPC-764 shown.)

FORMAT

Notice that the first field displays the STD signature format. STD refers to the Hewlett Packard seven-segment format which displays characters 0-9, A, C, F, H, P, U. (The HEX display format, which can be selected in this field, displays the hexadecimal characters 0-9, and A-F.)

START/STOP

Move the cursor to the START field using the **NEXT** or **PREVIOUS** keys as required. The START word is always displayed in the format used in the state menu. Press the **N (Binary)** key to display the START word in a binary format. Next, enter the single-bit START word (**0**) in the ninth bit position from the left. Press the **NEXT** key to move to the STOP field. Then press the **N (Binary)** key and enter the single-bit STOP word (**1**) in the same bit position as before. See Figure 6-23.

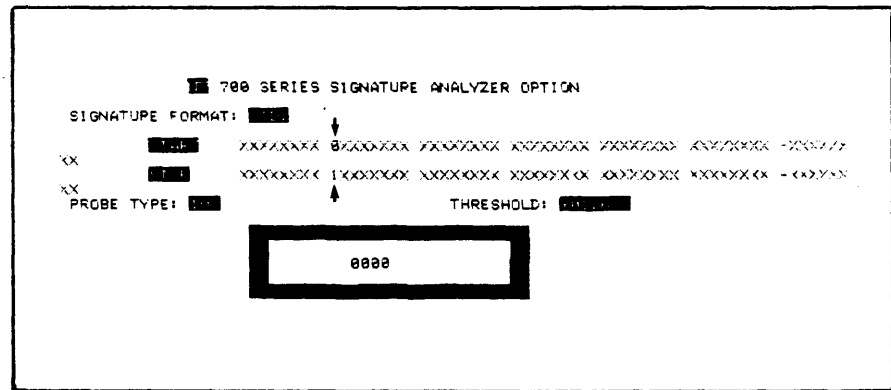


Figure 6-23. Use of single bit START and STOP words.
(NPC-764 shown.)

NOTE: The use of a ZERO in the menu display above is equivalent to a (✓) signal on the HP-5004A, while the use of a ONE is equivalent to a (⌘) signals

Connect the A and B state probes to the A and B outputs of the test card. Press the **COLLECT** key. A signature can now be taken for any serial stream on the test card in the interval between the single-bit START and STOP words.

SIGNATURES

When you want to take a signature of a test point, simply touch the circuit node of interest. For example, touch the Model 90 probe tip to the B channel data lines (labeled DB0-DB7), one at a time; the NPC-700 automatically displays the signature of the data line being tested. See Figure 6-24. (NPC-764 shown.)

Note that each time you take a serial collection resulting in a new signature, the display underneath the signature reads UNSTABLE (changing) for approximately a second, before switching to STABLE. However, if the signature collection is the same for successive measurements, only the message STABLE is displayed.

Also note that the signature window displays REPEAT MODE above the signature. This is the automatic mode mentioned above. Press the **HOLD (F4)** key to hold the displayed signature; press the **COLLECT** key to return to the automatic mode.

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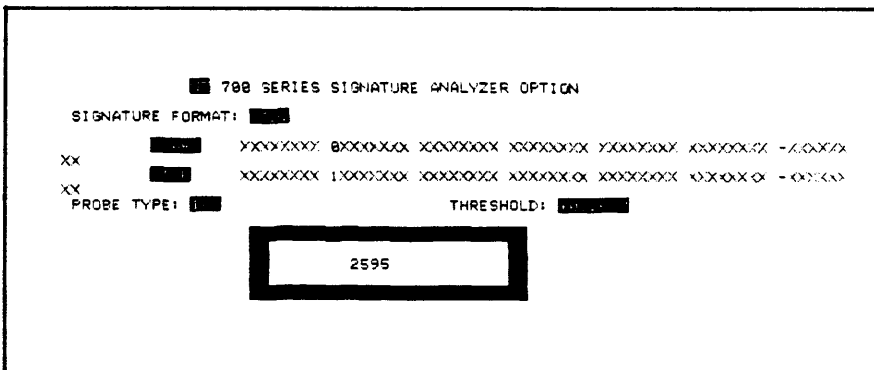


Figure 6-24. Display of signature for test point DB0 of the B channel. (Note: Your signature may differ since there are several versions of the test card in the field.)

FAULT-ISOLATION

Using the REPEAT mode, let's generate a fault. With the probe on DB0 on the B channel side of the test card, place the shorting wire on pin 2 of U3. U3 is located at the top center of the test card. This fault changes the counting sequence of the B counter. Press COLLECT to obtain a new signature for test point DB0. Note that the new signature shown in Figure 6-25 differs from the signature in Figure 6-24.

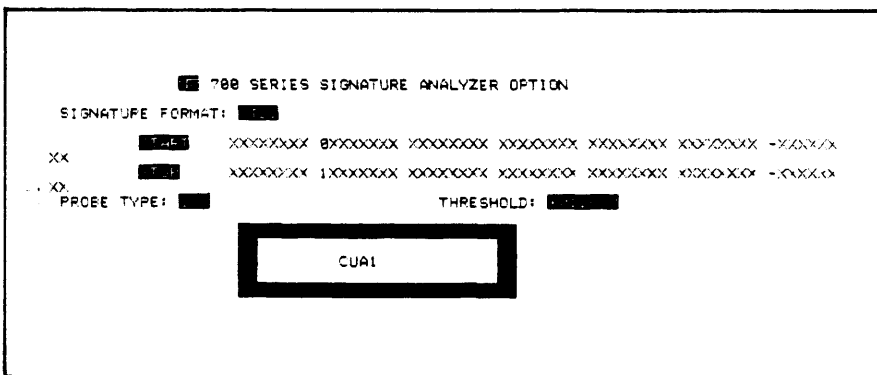


Figure 6-25. New signature for DB0 (B Counter).

**6.2.5 BASIC ANALYSIS
SUMMARY**

When using the NPC-700 to solve basic system problems, all that is required to collect meaningful data is the following steps:

1. Select the appropriate menu.
2. Select a clock.
3. Set in a trigger word.
4. Press the **COLLECT** key.

SECTION 6.0

ANALYSIS EXAMPLES

6.3 ADVANCED ANALYSIS EXAMPLES

At times, a problem may require more sophisticated analysis capabilities than those described in Section 6.2. When this is the case, the advanced state features of the NPC-700 such as 16 levels of sequential triggering, data qualified clocking, counter-timer and HP-type signature measurements, and linkage can all be employed. The advanced features of the timing analyzer, such as glitch memory, waveform recording, and linkage can prove indispensable. These features are designed to "build" on the basic capabilities described earlier so that a minimum amount of time is required to utilize even the most sophisticated features of the NPC-700.

6.3.1 ADVANCED STATE ANALYSIS EXAMPLES

SET-UP

With the two state probes connected to the test card as in the basic test of Section 6.2, initialize the NPC-700 by pressing the **RESET** key. (Or, turn power on if the NPC-700 has been off.) For the NPC-764, the C state probe should now be plugged into the analyzer and set to **TTL** and **COMP** so that the 16 least significant bits in the following steps are set to all zeroes. Check that the 48 (32) CHANNEL STATE mode is selected.

MIXED DISPLAY FORMAT

The NPC-700 allows the user to intermix up to five different display formats. Thus, for example, you can display the address of an I/O port in HEX, the characters being output in ASCII, and the associated handshaking signals in binary. Note that you can also blank out any channel by placing an X in the appropriate bit position.

Call the STATE menu and set the display format as follows:

```
AAAAAAAA AAAAAAAAA BBBCDDDD DEEEEEEE
```

```
A=HEX B=OCT C=DEC D=BIN E=ASC
```

```
(H) (O) (Z) (N) (Y)
```

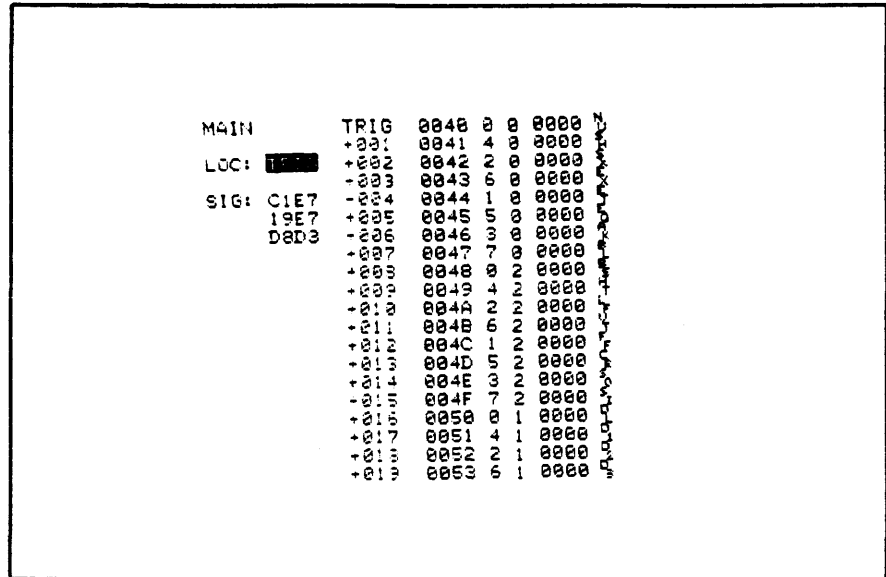
Set the A-channel trigger to **0040**. Leave the remaining bits in the trigger word as X ("don't care"). See Figure 6-26.

```
48 CHANNEL STATE MENU
FORMAT: AAAAAAAAA AAAAAAAAA BBBCDDDD DEEEEEEE XXXXXXXX XXXXXXXX
        A HEX B OCT C DEC D BIN E ASC
CLK SEL: A PRB: J B PRB: A C PRB: A QUALIFIERS: -AABBCC EL
CLK QUAL: OFF
        OR OFF
PRE-TRIG MEMORY (8-249): 000 WORDS
RESTART: OFF
TRIGGER:
0      0040 X X XXXX XX -XXXXXX XX
END
```

Figure 6-26. State menu for mixed format display. (NPC-764 shown.)

**SAVING DATA
IN AUX MEMORY**

Press **COLLECT** to obtain a data collection in the selected mixed format. See Figure 6-27.



**Figure 6-27. Mixed format display.
(NPC-764 shown.)**

**CLOCK QUALIFICATION*
(NPC-764)**

Press the **LABELS** key and note that the C key will step you to the first (top) **CLOCK QUAL** field, which is currently off. After pressing the C key, press the **SELECT** key to turn the first clock qualifier on.

The clock qualifier consists of two fields: a 48-bit field for internal clock qualification, and a 7-bit field (separated by a "-") for external clock qualification. The 48-bit field corresponds to the data coming into the 16-channel A, B, and C probes and is automatically formatted in accordance with the mixed format specified in Figure 6-26.

Press the **HEX**, **OCT**, **DEC**, **BIN** and **ASC** keys to change this field from one format to the other.

Return to the original mixed format by pressing the **U** key.

* For simplicity, this discussion on qualifiers pertains to the NPC-764. Since the NPC-748 does not use a third probe, it has 16 fewer internal qualifiers and 2 fewer external qualifiers.

EXTERNAL CLK QUAL (NPC-764)

The 7-bit external clock qualifier field corresponds to the header: -AABBCC EL, at the upper right of the CRT. (The eighth bit, L, is not used in the CLOCK QUAL field.) The two A bits correspond to a pair of external qualifier lines (Q₁ and Q₂) coming in through pins 33 and 20 in the A probe; likewise, the two B bits and C bits correspond to qualifier lines on the B and C probes. The E bit corresponds to an additional external qualifier line coming in through the EXTERNAL INPUT BNC connector at the rear of the analyzer.

INTERNAL CLK QUAL

The internal clock qualifier field is used to limit the collection of data to a certain range of address or data words. Without this qualifier, the NPC-700 would simply collect sequential counter data from the test card. Starting with the trigger word 0040, a nonqualified data collection would consist of 0041, 0042,... 0050, 0051, 0052...etc. But suppose you wished to exclude from the collection all address words that did not begin with 004. In other words, the data collection is to contain address words between 0040 and 004F only. To test this, set the clock qualifier word corresponding to A probe input data to 004X. (The rest of this field should remain all X's.) See Figure 6-28.

```

                                48 CHANNEL STATE MENU
FORMAT:  AAAAAAAAA AAAAAAAAA BBBCCDDD DEEEEEEE XXXXXXXX XXXXXXXX
          A HEX B OCT C DEC D BIN E ASC
CLK SEL:  A PRB: J B PRB: A C PRB: A QUALIFIERS: -AABBCC EL
CLK QUAL: 004 X X XXXX XX -XXXXX X
          OR OFF
PRE-TRIG MEMORY (0-249): 000 WORDS
RESTART:  OFF
TRIGGER:
0         0040 X X XXXX XX -XXXXX XX
END
    
```

Figure 6-28. Setting up the internal clock qualifier field. (NPC-764 shown.)

COLLECT

Press COLLECT to collect qualified data. Notice that the COLLECTION STATUS line reads STATE: TRIGGERED and provides a real-time count as the 1000-word state memory fills up. Also notice that word +016 is now 0040, instead of 0050. Scroll the data collection upward. Note that only addresses over the range 0040-004F are in the data collection. See Figure 6-29.

MAIN	TRIG	0040	0	0	0000	X
	+001	0041	4	0	0000	X
LOC: █	+002	0042	2	0	0000	X
	+003	0043	6	0	0000	X
SIG: C0E7	+004	0044	1	0	0000	X
42E7	+005	0045	5	0	0000	X
D8D3	+006	0046	3	0	0000	X
	+007	0047	7	0	0000	X
	+008	0048	0	2	0000	X
	+009	0049	4	2	0000	X
	+010	004A	2	2	0000	X
	+011	004B	6	2	0000	X
	+012	004C	1	2	0000	X
	+013	004D	5	2	0000	X
	+014	004E	3	2	0000	X
	+015	004F	7	2	0000	X
	+016	0040	0	0	0000	X
	+017	0041	4	0	0000	X
	+018	0042	2	0	0000	X
	+019	0043	6	0	0000	X

Figure 6-29. Example of qualified data collection containing addresses from 0040 through 004F only. (NPC-764 shown.)

COMPARE

Press **M** and compare the previously saved, nonqualified data with the current, qualified data collection. Return to the main memory. Then press the **LOCATE** and **T** keys to place the trigger word at the top of the display.

Press the **C** and **NEXT** keys to move to the second clock qualifier field. Activate this field by pressing the **SELECT** key or simply enter **005F** (rest **X**'s). Because this second clock qualifier is logically OR'ed with the first one, and the trigger word is **0040**, the NPC-700 will collect addresses over the range 0040-004F followed by the address word 005F. Press **COLLECT**. The resulting data collection is shown in Figure 6-30.

NOTE: Even if the trigger word is different than the qualified data, the NPC-700 will still trigger provided that the trigger word is valid (i.e., exists in the circuit-under-test). For example, try using **0032** in the TRIG field. Then press the **COLLECT** key. The resulting data collection contains the same qualified data as before; however, the trigger word: **0032** is not present. Return to a trigger word of **0040**.

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MAIN	TRIG	0040	0	0	0000
	+001	0041	4	0	0000
LOC: 0000	+002	0042	2	0	0000
	+003	0043	6	0	0000
SIG: BD4C	+004	0044	1	0	0000
0E4C	+005	0045	5	0	0000
D8D3	+006	0046	3	0	0000
	+007	0047	7	0	0000
	+008	0048	0	2	0000
	+009	0049	4	2	0000
	+010	004A	2	2	0000
	+011	004B	6	2	0000
	+012	004C	1	2	0000
	+013	004D	5	2	0000
	+014	004E	3	2	0000
	+015	004F	7	2	0000
	+016	005F	7	3	0000
	+017	0040	0	0	0000
	+018	0041	4	0	0000
	+019	0042	2	0	0000

Figure 6-30. The logical OR'ing of two clock qualifiers. (NPC-764 shown.)

Return to the STATE menu by pressing the C key. Use the SELECT key to turn each clock qualifier off. Note that this "deselect" feature allows you to set up qualifiers and use them only as needed.

PRETRIGGER

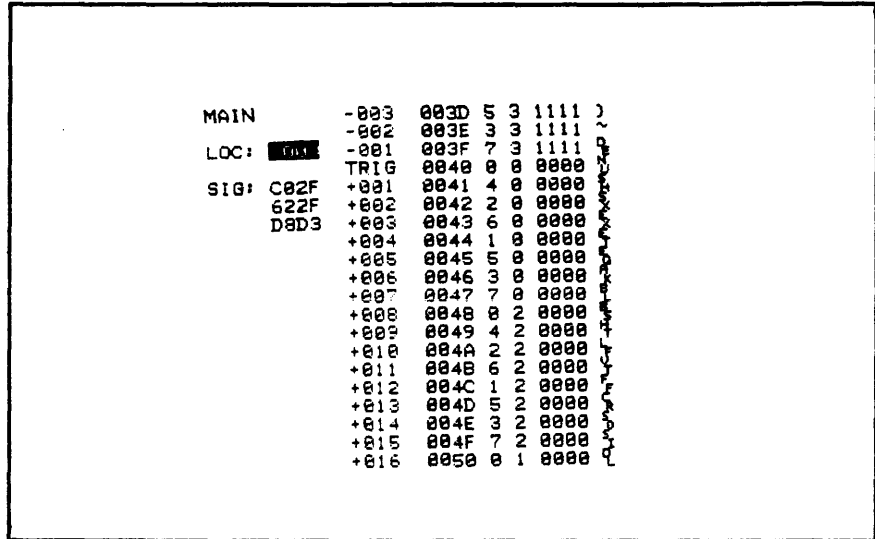
Use the NEXT key to access the pretrigger field. Enter 0-0-3 into this field. See Figure 6-31.

48 CHANNEL STATE MENU	
FORMAT:	AAAAAAAA AAAAAAAAA BBBCCDD DEEEEEEE XXXXXXXX XXXXXXXX
	A HEX B OCT C DEC D BIN E ASC
CLK SEL:	A PRB: J B PRB: A C PRB: A QUALIFIERS: -AABBC EL
CLK QUAL:	OFF
	OR OFF
PRE-TRIG MEMORY (0-249):	003 WORDS ←
RESTART:	OFF
TRIGGER:	
0	0040 X X XXXX XX -XXXXXX XX
END	

Figure 6-31. State menu set for pretrigger data collection. (NPC-764 shown.)

COLLECT

In order to view pretrigger data, press **COLLECT**. Then press the **LOCATE** and **B** keys. This will cause the first (or beginning) word in the data collection (-003) to be displayed at the top of the display. See Figure 6-32.



**Figure 6-32. Example of pretrigger data.
(NPC-764 shown.)**

**PRETRIGGER
MECHANISM**

The maximum pretrigger value is 999*. For the NPC-700, this means that as many as 999 words prior to the trigger word can be collected. However, it should be noted that the NPC-700's pre-triggering mechanism is specifically designed so that any given pretrigger value reflects the maximum number of data words that can be collected prior to the trigger. This means, for example, if a pretrigger value of 225 was used, the amount of data words collected prior to the trigger could be anywhere between 1 and 225. This type of pretrigger mechanism is employed so that the user doesn't have to be absolutely certain when he presses **COLLECT** that at least 225 events are going to occur prior to the trigger. If fewer events occur, the data collection will still be accomplished and the results displayed. (Other approaches cause the data collection to be inhibited if an internal pretrigger counter is not allowed to count down to zero.) Experiment with the NPC-700's pretrigger mechanism by setting in the maximum pretrigger value. Then press **COLLECT** followed by **LOCATE** and **B**. Repeat this several times and note that the beginning word in the data collection will vary, depending on where the trigger word happens to be in the test card's 256-step count loop when you press **COLLECT**.

* 249 was the maximum value in earlier production versions.

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Press **P** to return to the PRETRIGGER field and set this field to 000 (no pretriggering). Press **COLLECT**. Then press the **LOCATE** and **T** keys to return the trigger word to the top of the display.

SEQUENTIAL TRIGGERING

The NPC-700 incorporates 16 levels of sequential triggering. One application of this feature is in the tracing of deeply-nested subroutines. Use the **T** key to access the TRIGGER field at level 0. Press the **NEXT** key to access the END field. Then press the **SELECT** key to activate the trigger word and delay at level 1.* Set the level 1 trigger word to 0-0-4-1. Then press the **NEXT** key to access the DELAY field. Use the **SELECT** key to view the 5 possible delay modes: AFTER 0000 CLOCKS, NOT ON 0000 CLOCKS, BEFORE 0000 CLOCKS, ON 0000 CLOCKS, and OCCURS 0000 TIMES. Select **ON 0000 CLOCKS** and enter in a delay value of **2049**. Because the counter on the test card rolls over after 256 counts, any delay value (like 2049) that satisfies the equation:

$DELAY = (N \times 256) + 1$, where $N = \text{an integer}$, will work here.

Set up levels 2 and 3 as shown in Figure 6-33 so that the entire trigger word sequence is as follows:

<u>LEVEL</u>	<u>TRIGGER WORD</u>	<u>DELAY</u>
0	0040	---
1 THEN	0041	ON 2049 CLOCKS
2 THEN	0042	ON 3073 CLOCKS
3 THEN	005A	AFTER 2000 CLOCKS

```
48 CHANNEL STATE MENU
FORMAT: AAAAAAAAAA AAAAAAAAAA BBBCCDD DDDEEEEE XXXXXXXX XXXXXXXX
        A HEX B OCT C DEC D BIN E ASC
CLK SEL: A PRB: J B PRB: A C PRB: A QUALIFIERS: -AABBCC EL
CLK QUAL: OFF
        OR OFF
PRE-TRIG MEMORY (0-249): 000 WORDS
RESTART: OFF
TRIGGER:
0      0040 X X XXXX XX -XXXXXX XX
1 THEN 0041 X X XXXX XX -XXXXXX XX           ON 2049 CLOCKS
2 THEN 0042 X X XXXX XX -XXXXXX XX           ON 3073 CLOCKS
3 THEN 005A X X XXXX XX -XXXXXX XX           AFTER 2000 CLOCKS
```

Figure 6-33. Menu used for sequential triggering example. (NPC-764 shown.)

* An alternative to using the **SELECT** key is to simply start entering data and the field will activate itself.

COLLECT

Press **COLLECT**. Note that status messages on the display show the user how the NPC-700 is progressing through the triggering sequence. Also note how the use of a slow CMOS counter circuit in the test card and large delay values allow these messages to be readily viewed. Observe that the trigger word is **005A**, which is the last word specified in the trigger stack. See Figure 6-34.

MAIN	TRIG	005A	2	3	0000	!
	+001	005B	6	3	0000	"
LOC: 0077	+002	005C	1	3	0000	#
	+003	005D	5	3	0000	\$
SIG: C877	+004	005E	3	3	0000	%
5877	+005	005F	7	3	0000	&
D8D3	+006	0060	0	0	1000	'
	+007	0061	4	0	1000	(
	+008	0062	2	0	1000)
	+009	0063	6	0	1000	*
	+010	0064	1	0	1000	+
	+011	0065	5	0	1000	,
	+012	0066	3	0	1000	-
	+013	0067	7	0	1000	
	+014	0068	0	2	1000	
	+015	0069	4	2	1000	
	+016	006A	2	2	1000	*
	+017	006B	6	2	1000	+
	+018	006C	1	2	1000	,
	+019	006D	5	2	1000	-

Figure 6-34. Data collection corresponding to sequential triggering example. (NPC-764 shown.)

Press **COLLECT** again. Then, before level 3 is reached, hold the shorting wire at the junction of the resistor and capacitor (WF test point) located on the A side of the test card. This will short out the clock circuit driving the CMOS counters. Note that the NPC-700 indicates the current trigger level and the message "WARNING: SLOW CLOCK." Remove the short so that the triggering sequence can go to completion.

**SAVING STATE DATA*
IN THE AUX MEMORY AND
ON DISKETTE
(NPC-764 ONLY)**

For use with the NPC-764 in a later step, it's necessary to save the menu in Figure 6-33 and the associated data collection in Figure 6-34 on your diskette.

NOTE: In order to store main memory test data on the diskette, you must always transfer it first to the auxiliary memory by pressing the **S (SAVE)** key.

* For the NPC-748, press the **S (SAVE)** key to save the menu and test results in auxiliary memory for later use.

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NOTE: DO NOT PRESS RESET TO OBTAIN THE CONFIGURATION LIST OR YOU'LL ERASE ALL OF YOUR MENU PARAMETERS AND DATA.

When the prompt **A>** appears, type:

LASAVE

LASAVE SDATA (RETURN)

At this point, the menu parameters and data are stored in a file called **SDATA**. (You could have used any other file name up to 8 characters.)

NOTE: The **LASAVE** command actually saves both state and timing menus and auxiliary memory data. However, only the state information is pertinent at this time. As you will see later on, **SDATA** serves as an intermediate file for a state/timing linkage example.

DIR

Type **ESC** and **DIR** to verify that this file is now on the diskette.

FILE TEST

Press **RESET** to erase your menu parameters and data. To verify this, call the state menu when the **CONFIGURATION LIST** appears. Press **S1** and **M** to examine the main and auxiliary memory data which will be blank except for one or more "garbage" words.

LARECALL

Now, with the diskette loaded, call the **CONFIGURATION LIST** and press **ESC**. When the **A>** prompt again appears, type:

LARECALL SDATA (RETURN)

When the **CONFIGURATION LIST** is displayed, call the state menu and compare it with Figure 6-33. Press **S1** to call the state display and then press **M** to view the contents of the auxiliary memory. Compare the auxiliary memory data with Figure 6-34. Press **M** to return to the main memory.

NOTE: If you now want the same data in main memory as is in the auxiliary memory, simply press **COLLECT**. Then press the **M** key to compare signatures.

RESTART

When tracing program flow, there can be several paths leading to the same point in the program. The restart feature of the NPC-700 gives you control over which path will be actually traced by the analyzer to get to the desired trigger point. Figure 6-35 illustrates this concept.

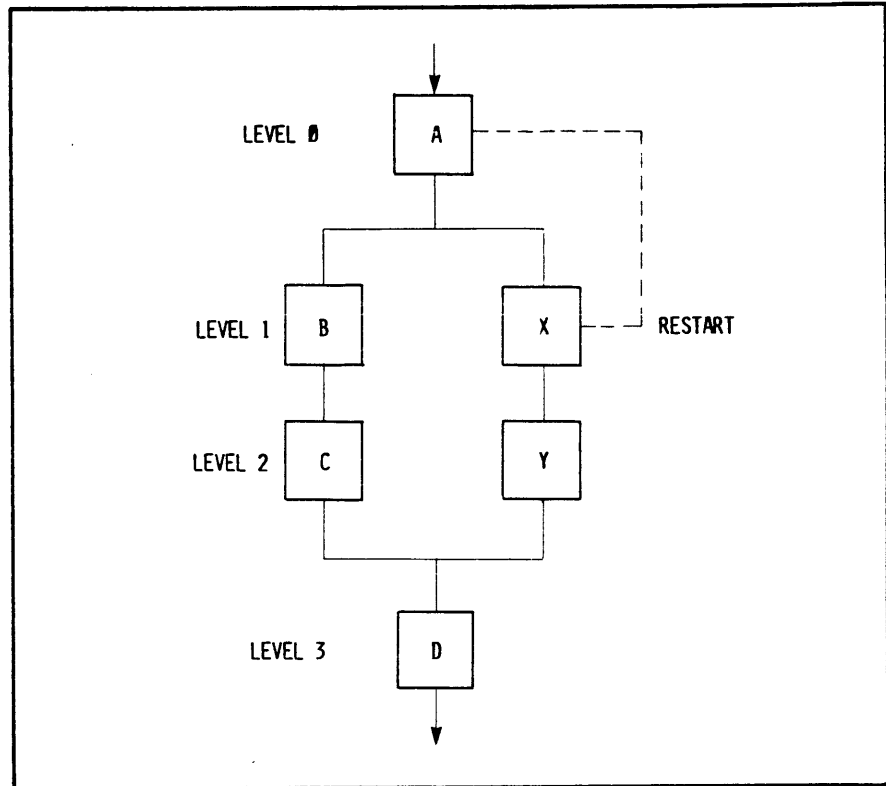


Figure 6-35. Using the RESTART feature to ensure that program path A-B-C-D is followed.

RESTART EXAMPLE

Suppose that to get to point D, the program in Figure 6-35 can follow either path A-B-C-D or path A-X-Y-D. If the trigger stack is set up to trace path A-B-C-D but path A-X-Y-D occurs, the analyzer will be "hung-up" at level 1 because event B never occurred. The restart feature is used to reset the stack back to level 0 whenever an event in the undesired path occurs. Thus, if RESTART = X, the occurrence of the undesired path (A-X-Y-D) will be detected and the trigger stack will automatically restart at level 0 as if a COLLECT had occurred. Then, when path A-B-C-D occurs, the analyzer will be ready and the triggering sequence will go to completion.

Access the RESTART field by pressing the T and PREVIOUS keys. Then press the SELECT key. (Notice that the RESTART word has the same mixed format as the clock qualifiers and trigger words.) Enter the value 0080 for the RESTART word. See Figure 6-36.

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```

48 CHANNEL STATE MENU
FORMAT: AAAAAAAAA AAAAAAAAA BBBCCDD DEEEEEEE XXXXXXXX XXXXXXXX
        A HEX B OCT C DEC D BIN E ASC
CLK SEL: A PRB: J B PRB: A C PRB: A QUALIFIERS: -AABBCC EL
CLK QUAL: OFF
        OR OFF
PRE-TRIG MEMORY (0-249): 000 WORDS
RESTART: 0080 X XXXX XX -XXXXXX XX
TRIGGER:
0      0040 X X XXXX XX -XXXXXX XX
1 THEN 0041 X X XXXX XX -XXXXXX XX           ON 2049 CLOCKS
2 THEN 0042 X X XXXX XX -XXXXXX XX           ON 3073 CLOCKS
3 THEN 005A X X XXXX XX -XXXXXX XX           AFTER 2000 CLOCKS

```

Figure 6-36. State menu with RESTART word 0080. (NPC-764 shown.)

COLLECT

In order to test the restart feature, we'll create an "apparent" branch in the test card's counter sequence. To do this, short out pad 7 (MSB) on the A side of the test counter. This causes the counter output sequence to consist of 128 counts (0000-007F) instead of 256 counts (0000-00FF). With pad 7 shorted, press **COLLECT**. Since the RESTART word 0080 never occurs, the trigger sequence goes to completion. Now press **COLLECT** again and remove the short **before** level 3 is reached. Note that the stack returns to level 0 (flashing) because the RESTART word 0080 is now permitted to occur. See Figure 6-37. Again short out pad 7 and watch the trigger sequence go to completion. Remove the short.

```

MAIN      TRIG  005A 2 3 0000
+031     005B 6 3 0000
LOC:  TRIG  +032 005C 1 3 0000
      +033 005D 5 3 0000
SIG: C177 +034 005E 3 3 0000
      5077 +035 005F 7 3 0000
      D8D3 +036 0060 0 0 1000
      +037 0061 4 0 1000
      +038 0062 2 0 1000
      +039 0063 6 0 1000
      +040 0064 1 0 1000
      +041 0065 5 0 1000
      +042 0066 3 0 1000
      +043 0067 7 0 1000
      +044 0068 0 2 1000
      +045 0069 4 2 1000
      +046 006A 2 2 1000
      +047 006B 6 2 1000
      +048 006C 1 2 1000
      +049 006D 5 2 1000
STATE:  STACK LEVEL 0

```

Figure 6-37. The occurrence of 0080 (RESTART) causes the trigger stack to reset to level 0. (NPC-764 shown.)

RESTART

Return to the RESTART field and press the **SELECT** key to activate the RESTART mode. Unlike the RESTART word which forces the stack back to level 0, the occurrence of any data pattern not matching the RESTART word forces the stack to leave level 0. Press the **SELECT** key to turn RESTART off.

TRIGGER QUALIFIERS*

Notice that each trigger level or RESTART word can also be set up to require the occurrence of the external trigger qualifier events: -AABBCC EL. The AABBCC and E signals are physically the same external input probe lines that were previously discussed in connection with the clock qualifier fields. However, in this case, they act as enabling signals to the incoming trigger words. Thus, if level 1 were set up as follows:

0041 X X XXXX XX -IXXXXX 1X, (NPC-764 shown)

then the A probe qualifier on pin 33 must be high (1) and the external BNC input on the rear panel must also be high (1) when 0041 occurs; otherwise, the analyzer will not advance to level 1 from level 0. (Do not actually change the trigger qualifier from all X's.)

The L bit is another trigger qualifier which links any stack level to the successful triggering of the timing or waveform analyzers or another analyzer connected to the LINK BNC on the back panel. (The use of the L bit is discussed in more detail later.) In microprocessor applications, for example, trigger qualifiers can control triggering using signals that are generally not on the address bus or data bus, or are not required in the data collection. As such, they can be considered as extra channels that are not displayed. Thus, for the NPC-764, a 56-bit-wide trigger word can be specified (48 data channels plus 8 trigger qualifiers).

NONOCCURRENCE TRIGGERING

Press the **NEXT** key and step to trigger level 1. Then use the **SELECT** key to choose the nonoccurrence triggering mode. The trigger word for level 1 will now be displayed as:

0041 X X XXXX XX -XXXXXX XX. (NPC-764 shown)

This mode can be used to trace program sequences when expected events are not occurring. In this example, the analyzer would pass through level 1 only if 0041 did not occur precisely 2049 clocks after 0040. Nonoccurrence triggering is available at each of the 16 levels. Note that the qualifiers do not change sense in the nonoccurrence triggering mode.

TURNING THE STACK OFF

With level 1 still accessed, press the **SELECT** key to turn level 1 and subsequent levels in the trigger stack off. This feature allows the user to store a desired triggering sequence in the stack for later use as required. Press the **SELECT** key once to again activate the entire stack.

*The NPC-748 has 2 fewer trigger qualifiers.

NOTE: For the NPC-748, this is **not** a good stopping point if you wish to power down. (The stored test previously saved in the auxiliary memory will be lost if the power is turned off.)

6.3.2 ADVANCED TIMING ANALYSIS EXAMPLES

SET-UP

With the A and B timing probes connected to the A and B outputs of the test card as in the basic timing example of Section 6.2.2, call the CONFIGURATION LIST by pressing the **CONFIG** key. Select the 16 CHANNEL TIMING configuration and call the menu.

CLOCK

With the 16-CHANNEL TIMING/STATE menu on the display and the cursor at the **CLOCK** field, select the **2 mS** clock by using the **SLOWER** key.

ARM AND TRIG

In this example, both levels of triggering will be used. Press **S2** and **A** as a quick way to enter the **ARM** field. Then enter: 0-0-0-0-0-0-0-0 plus 0-1-0-0-1-0-0-0, which is **(0048)HEX**. Use the **NEXT** key to step down to the **TRIG** field and enter: 0-0-0-0-0-0-0 plus 1-1-0-0-1-0-0-0, which is **(00C8)HEX**.

TRIGGERING MODES

Because we have now set up two levels of triggering (**ARM** and **TRIG**), we must use one of the triggering modes to specify the time delay between these levels. Use the **PREVIOUS** key to access the **TRIGGER MODE** field. Press the **SELECT** key to view the following major timing trigger mode options:

TRIG OCCURS > 0000 CLOCKS AFTER FIRST ARM

TRIG OCCURS BEFORE 0000 ARMS

GLITCH IN ARM WHEN TRIG VALID

Note that within the first two major trigger modes, the **NEXT** and **SELECT** keys can be used to change **TRIG** to TRIG, **>** to **<** or **=** (blank), **BEFORE** to **AFTER**, **FIRST** to **LAST**, and **ARM** to ARM.

Set the trigger mode to **TRIG OCCURS > 0000 CLOCKS AFTER FIRST ARM**. Then use the **NEXT** key to step to the **DELAY** field and set in a delay value of 1500. The trigger mode should now read:

TRIG OCCURS > 1500 CLOCKS AFTER FIRST ARM.

PRETRIGGER

Access the **PRETRIGGER** field by pressing the **S2** and **P** keys. Enter the value **5** into this field for 50% pretrigger. Figure 6-38 shows the timing menu up to this point.

```

                                16 CHNL TIMING/STATE MENU
                                2ms CLOCK
TRIGGER WHEN: TRIG OCCURS > 1500 CLOCKS AFTER FIRST ARM
                                CHNL NO. A76543210 B76543210 FILTER LINKAGE
ARM (0.1.X):      00000000 01001000 OFF NONE
TRIG (0.1.X):    00000000 11001000 OFF NONE
INPUT MODE (S,L): SSSSSSSS SSSSSSSS
PRE-TRIGGER (0-9): 50%
DISPLAY ORDER (0-7.X): AAAAAAAA BBBB8888
DISPLAY POLARITY (+,-): 76543210 76543210
THRESHOLD:        A PROBE B PROBE HYSTERESIS
(-6.4V - +6.35V) +1.60 +1.60 ON

```

Figure 6-38. Menu corresponding to this example thus far.

STATUS MESSAGES

Press **COLLECT** and wait several seconds. Notice the flashing status messages which indicate what the analyzer is doing as it transitions from **SAMPLING** to **ARMED** to **TRIGGERED** to **DONE**. (The relatively slow 2 mS clock allows these messages to be observed.)

LOCATING THE TRIGGER WORD

With the timing diagram displayed (at 1X magnification), the next step is to locate the trigger word, **00000000 11001000 (00C8)**. Notice that the 500 mark on the inverse video graticule at the bottom of the CRT is at full-intensity. This is the location of the trigger word with 50% pretrigger set in. When the **COLLECT** key was pressed, the following sequence of events occurred:

1. SAMPLE (COLLECT DATA AT 2 mS INTERVALS)
2. DETECT ARM WORD (0048)
3. COUNT AT LEAST 1500 CLOCKS (3 seconds +)
4. COLLECT PRETRIGGER DATA (500 WORDS PRIOR TO TRIGGER WORD)
5. DETECT TRIG WORD (00C8)
6. COLLECT TRIGGER WORD AND FILL REMAINING MEMORY (TRIGGER WORD PLUS 499 ADDITIONAL WORDS)
7. DISPLAY (MESSAGE DONE)

The display at 1X magnification is shown in Figure 6-39.

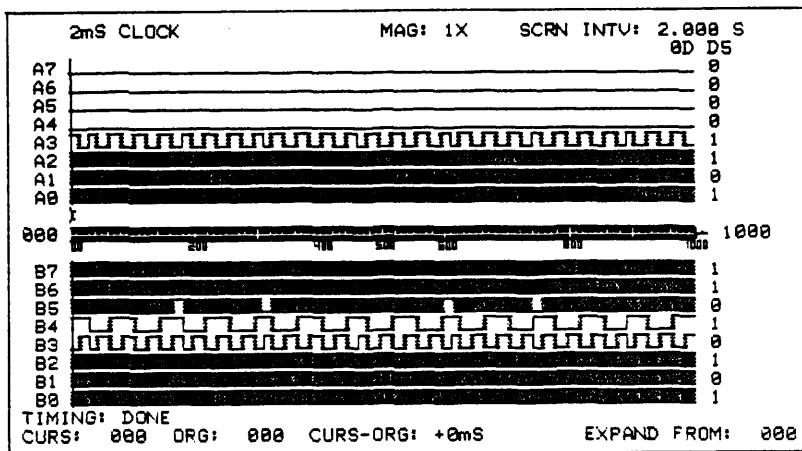


Figure 6-39. Timing display at 1X magnification.

SAVE (S)

Save the timing menu and data in the auxiliary memory for a later step by pressing the **S** key.

To locate the trigger word and examine data at the same time, step the expansion indicator **E** towards the middle of the screen using the **EXP->** key. Stop when the EXPAND FROM indicator readout at the lower right of the screen reads 500.

Press the **5** (20X magnification) key. Note that the display is now displaying data between memory locations 500 and 550. Bring the cursor to the left-hand edge of the CRT by pressing **L**. The cursor locator at the bottom left of the display should read **CURS: 500**. The trigger word, **(00C8)HEX**, will now appear at the right of the CRT. See Figure 6-40. Note that the binary value of the cursor corresponds only to the data at location 500.

SAVING TIMING DATA

NOTE: If a **RESET** or a power cycle has occurred between the advanced state example in the previous section and the current step, it will be necessary to restore the state menu shown in Figure 6-33. First, check to see if the state menu is intact by returning to the **CONFIGURATION LIST**, selecting the **48 (32) CHANNEL STATE** mode, and calling the state menu. If this menu is not identical to Figure 6-33, and you're using an NPC-764, then use the **LARECALL** command. This command will allow you to restore the state menu using the intermediate file, **SDATA**, as described toward the end of Section 6.3.1. For the NPC-748, the menu in Figure 6-33 must be restored manually. Once the required state menu is restored, do not press **RESET**. Also, if the **LARECALL SDATA** command is executed, it will be necessary to repeat the steps in this section to recover the timing menu and display up to this point. (This exercise illustrates the importance of using intermediate or back-up files.)

MAIN	TRIG	00	C8
	+001	02	CA
LOC: 512	+002	05	0D
	+003	06	0E
SIG: A850	+004	04	4C
AFC1	+005	05	CD
	+006	07	CF
	+007	00	A8
	+008	02	AA
	+009	01	69
	+010	02	6A
	+011	04	2C
	+012	05	AD
	+013	07	AF
	+014	04	EC
	+015	06	EE
	+016	09	11
	+017	0A	12
	+018	08	50
	+019	09	D1

Figure 6-41. Equivalent state display in hexadecimal. (Your data and signatures may differ since the triggering conditions specified are not unique).

LOCATING DATA IN MEMORY

With the state display selected, locate the beginning of the data collection by pressing the LOCATE and B keys. The data word at -500 should now be at the top of the display. Press S2 to recover the timing display. Note that the display is unchanged from Figure 6-40 since the software keeps track of each display independently. This feature can be useful when you need to examine one portion of the display in the state or timing domain, while leaving the other display unaffected as a point of reference. Now press S1 and the LOCATE (F3) and T keys to put the trigger at the top of the CRT.

L

Now find the beginning of the timing display by pressing the 1 (1X magnification) key and returning the cursor to location 000 by pressing the L key. The hexadecimal value at cursor location 000 in the timing display should match the value for word -500 in the state display. Verify this by using the S1 key to access the state mode. Press the S2 key to restore the timing display.

MISCELLANEOUS
FEATURES
OF THE 16-CHANNEL
TIMING/STATE MODE

TIMING DISPLAY
MANIPULATION

Access the DISPLAY ORDER field by pressing the D key. To illustrate the timing display flexibility of the NPC-700, set in the following display order for the 8 most significant channels: B4 - A0 - A6 - B7 - B0 - X - B4 - A2. Use the NEXT key to step down to the DISPLAY POLARITY field. Then set in the following display polarity: -+++---. See Figure 6-42.

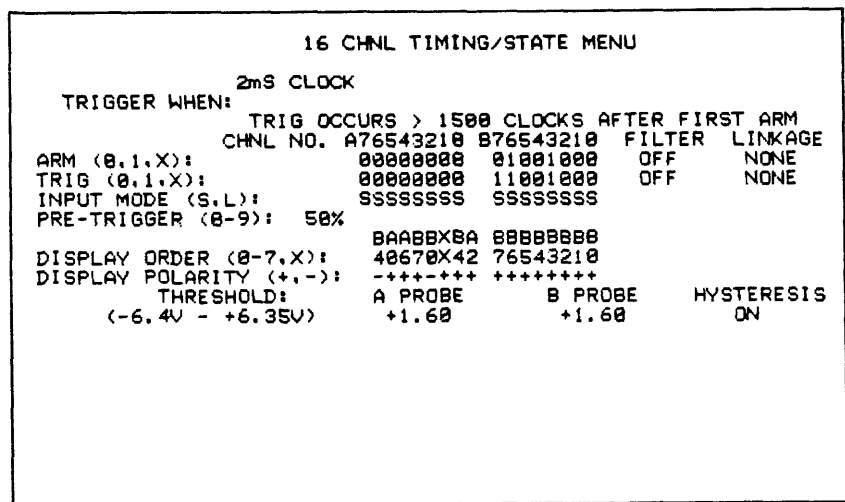


Figure 6-42. The menu used to illustrate the NPC-700's timing display flexibility.

S2
4 (10X)

Now press the S2 and 4 (10X) keys. At 10X magnification, the timing diagram will be similar to Figure 6-43. Note that the NPC-700 permits any mix of inverted and noninverted channels to be displayed. Also note that any channel can be blanked out and any channel can be repeated. In Figure 6-43, B4 is inverted at the top of the CRT and is adjacent to A0. Near the center of the display, B4 appears non-inverted and is adjacent to A2.

NOTE: If you're going to use the NAMES feature to label the timing signals, it's important to be aware that the position of these names are not changed when the timing display is reordered. Therefore, it is suggested that the NAMES feature be used **after** your display order is chosen.

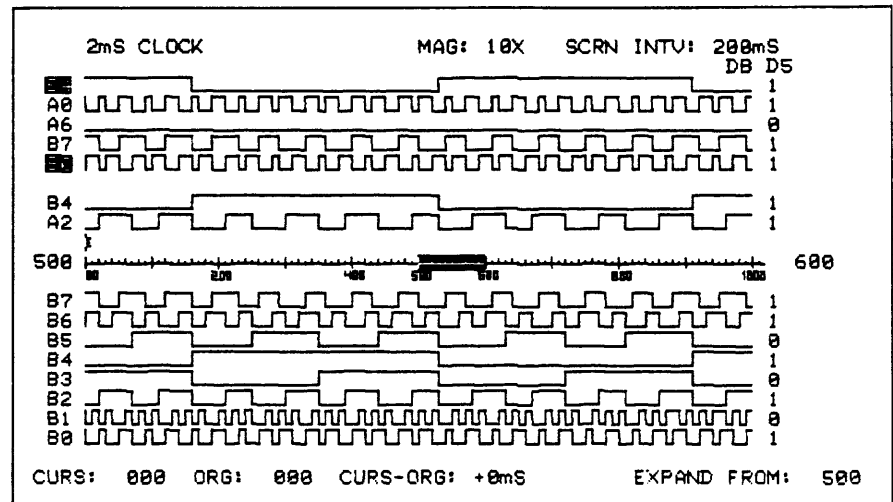


Figure 6-43. Demonstrating the NPC-700's timing diagram display flexibility.

FILTER

Access the ARM field by pressing the A key. Then step to the FILTER field associated with the ARM word using the NEXT key. The filter fields are used to make certain that the associated ARM or TRIG words are stable for 2 to 9 clock sample periods before they are considered valid. This feature avoids the generation of false ARM or TRIG words due to race conditions, propagation delays, or other transient events on the bus. (Note: the FILTER field ignores data entry values of 0 or 1.)

SAMPLE AND LATCH INPUT MODES

In the 16-channel/50 MHz mode (and the 8-channel/100MHz mode), the SAMPLE (S) mode is normally used for timing data acquisition. The LATCH (L) mode means that the corresponding channel is enabled to detect glitches (down to 5 nS) between sample clocks.

NOTE: In the conventional LATCH mode, a glitch whose width is at least 5 nS (but less than the sample clock period) is displayed as a pulse equal to one clock period wide. Refer to the 8 CHANNEL GLITCH MEMORY mode discussion later in this section which shows how glitches can be more readily identified on the CRT.

THRESHOLD

In the 16 CHANNEL TIMING mode, the threshold level for the 8 inputs to each Model 80 probe is keyboard settable in 50 mV increments between -6.40V and +6.35V. For the 8-channel modes, channels 0-3, Q, CLK, are adjustable independently of channels 4-7. These features are useful for monitoring ECL logic and mixed logic families.

HYSTERESIS

When enabled, this field provides 200 mV of hysteresis at each Model 80 probe. Hysteresis is useful for noise rejection and can improve the reliability of a data collection.

RECALL (R)

Next, set up the somewhat arbitrary menu parameters of Figure 6-44. The intent here is to illustrate how you can use the auxiliary memory to return to a previously stored menu after executing an unrelated test.

```

16 CHNL TIMING/STATE MENU
10uS CLOCK
TRIGGER WHEN: TRIG OCCURS > 0100 CLOCKS AFTER FIRST ARM
CHNL NO. A76543210 B76543210 FILTER LINKAGE
ARM (0.1.X): XXXXXXXX XXXXXXXX OFF NONE
TRIG (0.1.X): 00000011 01101111 OFF NONE
INPUT MODE (S,L): SSSSSSSS SSSSSSSS
PRE-TRIGGER (0-9): 50% BAABBXBA BBBBBBBB
DISPLAY ORDER (0-7.X): 40670X42 76543210
DISPLAY POLARITY (+,-): -+-+-+++ ++++++++
THRESHOLD: A PROBE B PROBE HYSTERESIS
(-6.4V - +6.35V) +1.60 +1.60 ON

```

Figure 6-44. Arbitrary menu.

COLLECT

Press **COLLECT** to take the data collection shown in Figure 6-45. Now, to recall the stored test, simply press **R**. Compare the recalled menu with Figure 6-38. Note that display parameters such as **DISPLAY ORDER** and **DISPLAY POLARITY** (which, in practice, would tend to remain the same in your test set-up) are not affected by the recall function. If **COLLECT** were pressed at this time, a data collection corresponding to the recalled menu would be displayed.

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ANALYSIS EXAMPLES

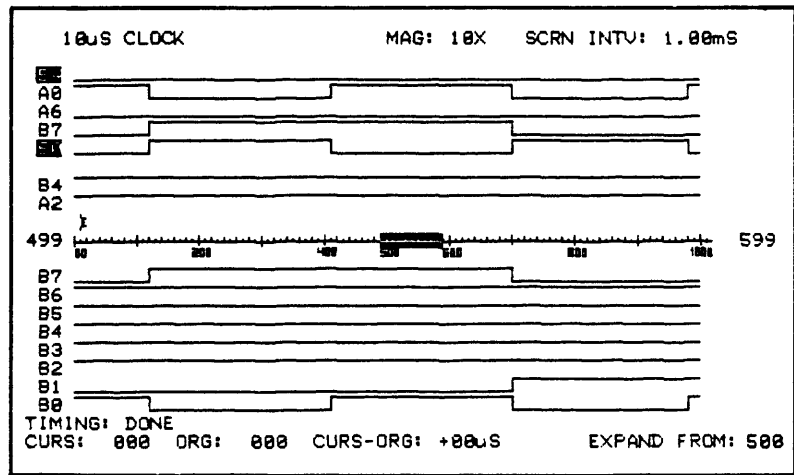


Figure 6-45. Timing display corresponding to the arbitrary menu of Figure 6-44.

8-CHANNEL/100 MHz MODE

For high-speed applications, the 8-CHANNEL/100MHz mode allows you to asynchronously sample your system using a 10 nS clock. In addition, this configuration increases the depth of the data memory to 2000 words. Thus, with this mode, you can achieve higher measurement resolution and double the number of samples at the same time.

Press **RESET** to reinitialize the NPC-700. (This is primarily done to quickly re-establish the default values of the DISPLAY ORDER and DISPLAY POLARITY fields.) Select the 8 CHANNEL TIMING (100 MHz) menu. See Figure 6-46. Notice that all channel-dependent fields are truncated to 8 bits.

```

      8 CHNL TIMING/STATE MENU
      10nS CLOCK
      TRIGGER WHEN:
      ■ TRIG OCCURS > 0000 CLOCKS AFTER FIRST ARM
      CHNL NO. A76543210 B76543210 FILTER LINKAGE
      ARM (0.1.X):          XXXXXXXX          OFF  NONE
      TRIG (0.1.X):          XXXXXXXX          OFF  NONE
      INPUT MODE (S.L):      SSSSSSSS
      PRE-TRIGGER (0-9):  10%
      DISPLAY ORDER (0-7.X):  AAAAAAAA
      DISPLAY POLARITY (+,-):  76543210
      THRESHOLD:             CH 0-3,Q,CK      CH 4-7      HYSTERESIS
      (-6.4V - +6.35V)      +1.60            +1.60      ON
  
```

Figure 6-46. 8 CHANNEL/100 MHz menu.

COLLECT

Set the clock to 10 nS. With both A and B probes plugged in, press **COLLECT**. Notice that the error message:

REMOVE B PROBE & PRESS COLLECT

appears on the display. This is because the removal of the B probe from the NPC-700 allows the hardware and software to multiplex the data coming from the A probe into both the A and B memories. Carefully remove the B probe from the NPC-700 (and the test card) and press **COLLECT**. This time a timing diagram display will appear. (However, it's doubtful you'll see any transitions of the slow CMOS counter due to the high sample rate.)

Access the pretrigger field by pressing the **P** key. Enter in a **0** for a pretrigger value of **00%**. Then press **COLLECT**. Next press the **S1** key to view the equivalent state display in hexadecimal. Locate the end of the data collection (word +1999) by pressing the **LOCATE** and **E** keys. See Figure 6-47. Return to the trigger word by pressing the **LOCATE** and **T** keys.

MAIN		+1980	00
		+1981	00
LOC:	0000	+1982	00
		+1983	00
SIG:	A314	+1984	00
	A314	+1985	00
		+1986	00
		+1987	00
		+1988	00
		+1989	00
		+1990	00
		+1991	00
		+1992	00
		+1993	00
		+1994	00
		+1995	00
		+1996	00
		+1997	00
		+1998	00
		+1999	00

Figure 6-47. State display of 8 CHANNEL/100 MHz mode. The last word in the data collection is at memory location +1999. (The data is meaningless due to the high sampling rate relative to the slow logic changes on the CMOS test card.)

8 CHANNEL GLITCH MEMORY MODE

The NPC-700's 8 CHANNEL GLITCH MEMORY mode allows you to capture 5 nS glitches and display them along with 8 channels of data. It is important to distinguish between this mode and the conventional 5 nS glitch latch capabilities of the previously described 8 and 16-channel timing/state configurations which do not incorporate a separate glitch memory. In the conventional 5 nS latch mode, the analyzer "remembers" the previous sample and arms a latch to capture any transitions occurring before the next sample clock edge. If a transition does occur, the latch is set and sampled at the next clock edge. In the case of a narrow glitch whose width is less than the clock sample period, the display will show the glitch as one clock period wide. See Figure 6-48.

LATCH MODE

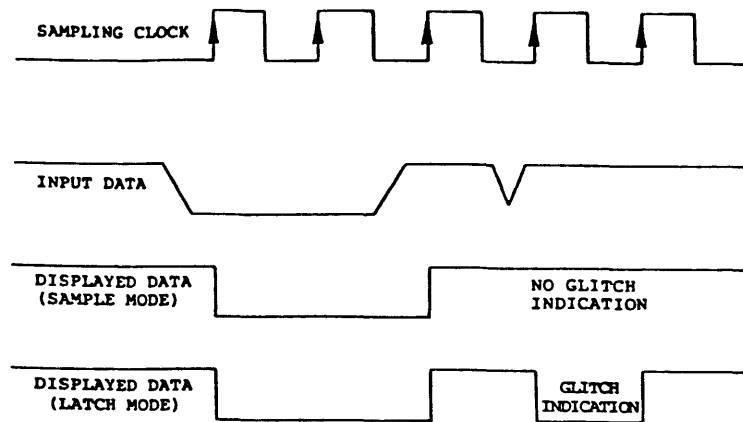


Figure 6-48. Sample and latch mode timing.

When using the NPC-700's 8-CHANNEL GLITCH MEMORY mode configuration, the analyzer splits its 1000-word, 16-channel memory into an 8-channel data memory plus an 8-channel glitch memory. Using the A timing probe only, glitches of 5 nS duration or longer that occur between sample clock edges are stored in the separate glitch memory. Upon display, a glitch is shown as a vertical line interspersed with the data. See Figure 6-49.

GLITCH MEMORY

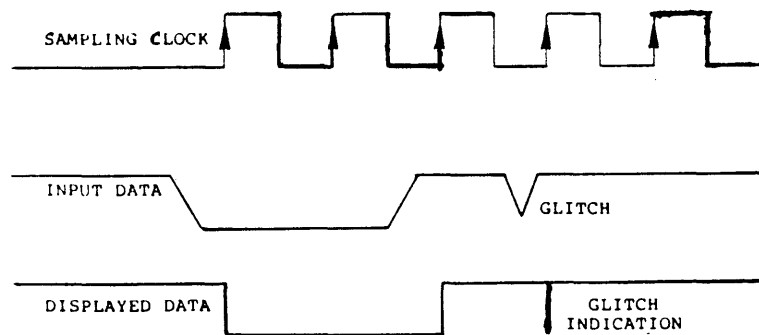


Figure 6-49. Glitch interspersed with data.

Press the CONFIG key. Select the 8 CHANNEL TIMING GLITCH mode from the CONFIGURATION LIST. Set in a clock of 1 mS and a pretrigger value of 00%.

COLLECT
S2

Press **COLLECT** to take a data collection. Press the **S2** key if necessary to display timing data. With the timing data displayed at X20, move the window (if necessary) to obtain a display similar to Figure 6-50. Notice the glitch indications on channel A0. The use of the relatively slow (1 mS) clock allows the "glitches" to be viewed since the definition of a glitch is any transition which occurs between sample clocks. (If you don't get at least 1 "glitch" on channel A0, press **COLLECT** again or use a 2 mS clock.)

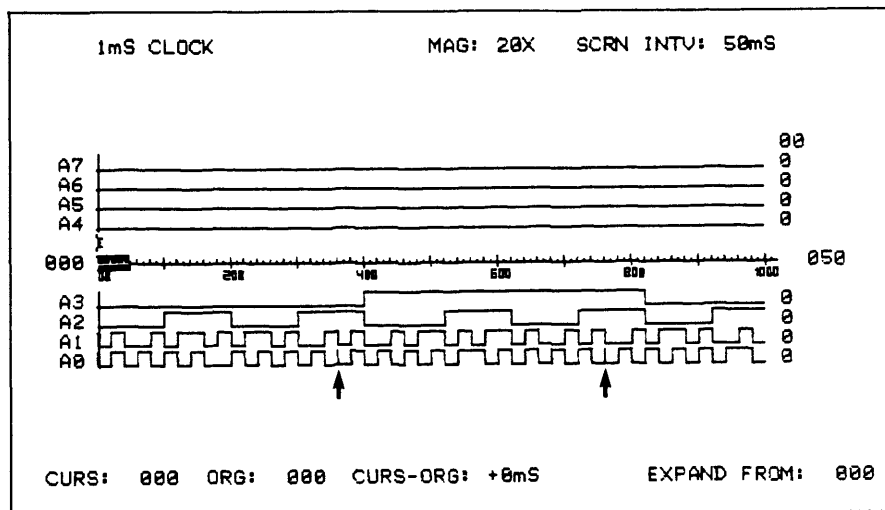


Figure 6-50. Timing display with glitches on channel A0. (Your display will differ since no trigger word was specified.)

NOTE: For the NPC-748, this is **not** a good stopping point if you wish to power down. (The stored test previously saved in the auxiliary memory will be lost if the power is turned off.)

6.3.3 LINKING OF STATE AND TIMING ANALYZERS

Linkage is used for tracing problems which cross between measurement domains. Up to this point, the state and timing analyzers have been operating totally independently. In the following steps, previously stored state and timing tests will be recalled so you can link the ARM word of the timing analyzer to the successful completion of the four levels of state triggering set up previously.

SETUP

Connect the **A STATE** probe to the A side of the test card and the **B TIMING** probe to the B side. All other probes should be connected to the analyzer without input signals.

LARECALL*
(NPC-764 ONLY)

Skip to the **LINKING STATE TO TIMING** paragraph if you're using the NPC-748.

Insert the diskette containing the **STATE** and **TIMING** files. Call the **CONFIGURATION LIST** and press **ESC**. When the **A** prompt appears, type:

LARECALL STDATA (RETURN)

At this point, the state data associated with the menu in Figure 6-33 and the timing data associated with Figure 6-38 have been recalled into their respective state and timing auxiliary memories. (Refer to Paragraphs 3.4.1 and 3.4.2 for details on LASAVE and LARECALL.)

**LINKING STATE TO
TIMING**

Select the 48 (32) **CHANNEL STATE/16 CHANNEL TIMING** mode (Configuration #3). Call the timing menu (**F2** key) and access the linkage field in the **ARM** word. Use the **SELECT** key to set this field to **L**. See Figure 6-51. The **ARM** word is now linked to the successful triggering of the state section.

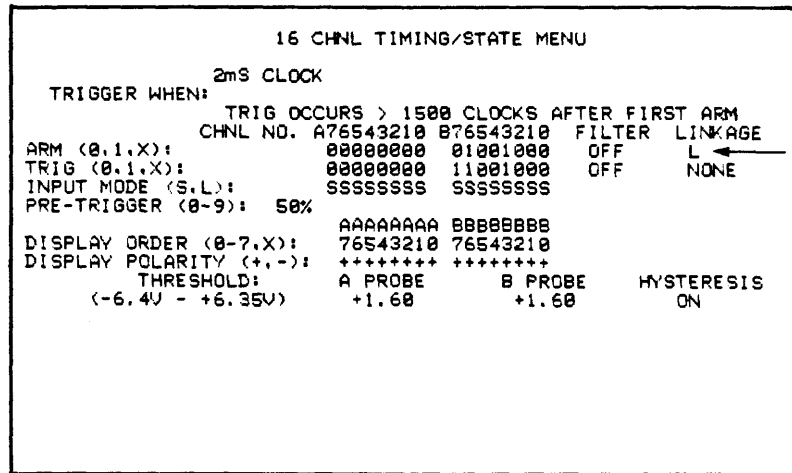


Figure 6-51. Linking the **ARM** word of the timing analyzer to the state analyzer.

STATE MENU

Return to the **CONFIGURATION LIST** and call the state menu (**F1** key). Verify that the 4-level trigger stack is again set-up as illustrated in Figure 6-33.

* For the NPC-748, the menus in Figures 6-33 and 6-38 must be manually restored if power has been cycled.

SECTION 6.0

ANALYSIS EXAMPLES

COLLECT

Press the **COLLECT** key and watch the status messages go through the following sequence:

STATE:	STACK LEVEL 0	TIMING:	SAMPLING
	STACK LEVEL 1		SAMPLING
	STACK LEVEL 2		SAMPLING
	STACK LEVEL 3		SAMPLING
	TRIGGERED	----->	ARMED
	DONE	(LINKAGE)	TRIGGERED
			DONE

LINKAGE

Notice how the timing analyzer continues sampling until the state section passes through stack level 3. At that instant, the timing analyzer's ARM word is enabled by the linkage bit so that when the ARM word actually occurs, the timing analyzer will be armed. (Meanwhile, the state analyzer is collecting data.) Then, after the 1500 clock delay is counted down, the timing analyzer "looks" for the timing trigger word. When it occurs, the analyzer triggers and begins collecting data. After 1000 samples are collected, the analyzer flashes the message DONE and displays the results. To switch displays between timing and state analyzers, press the **S2** and **S1** keys. (In the timing display, the A channels are all zeroes since the A timing probe is not connected.)

APPLICATION

As an example of linking the state analyzer to the timing analyzer, consider a process control application. Here, this type of linkage could be used to monitor the control signals generated as a result of a specific subroutine being executed.

DISABLING THE L BIT

With the timing display on the CRT, access the ARM field by pressing the **A** key. Step to the LINKAGE field and select **NONE**. (Once in the LINKAGE field, pressing the **DEFAULT** key is another way to do this.)

LINKING TIMING TO STATE

Return to the CONFIGURATION LIST and press the **F1** key to call the state menu. Using the L bit in the trigger qualifier field, any sequential trigger word in the state analyzer's 16-level trigger word stack can be linked to occurrences in the timing domain. Use the **NEXT** key to step down to level 1. Then use the **SPACE BAR** to access the L bit, which is the last bit in the trigger qualifier. Set this bit to 1 as shown in Figure 6-52.

```

                                48 CHANNEL STATE MENU
FORMAT:  AAAAAAAAA AAAAAAAAA BBBCCDDD DEEEEEEE XXXXXXXX XXXXXXXX
          A HEX  B OCT  C DEC  D BIN  E ASC
CLK SEL:  A PRB: J  B PRB: A  C PRB: A  QUALIFIERS: -AABBCC EL
CLK QUAL: OFF
          OR  OFF
PRE-TRIG MEMORY (0-249): 000 WORDS
RESTART:  OFF
TRIGGER:
0         0040 X X XXXX XX -XXXXXX XX
1 THEN   0041 X X XXXX XX -XXXXXX X1 ←      ON 2049 CLOCKS
2 THEN   0042 X X XXXX XX -XXXXXX XX      ON 3073 CLOCKS
3 THEN   005A X X XXXX XX -XXXXXX XX      AFTER 2000 CLOCKS

```

Figure 6-52. Linking the state analyzer's TRIGGER LEVEL 1 to the timing analyzer. (NPC-764 shown.)

COLLECT

Press the **COLLECT** key and watch the trigger status messages go through the following sequence:

TIMING: SAMPLING	STATE: LEVEL 0/1
	LEVEL 0/1
ARMED	
TRIGGERED	-----> LEVEL 1
	(LINKAGE)
DONE	LEVEL 2
	LEVEL 3
	TRIGGERED
	DONE

Notice how the state analyzer automatically restarts at level 0 until the timing analyzer completes its triggering sequence. When this happens, the state analyzer advances through the trigger stack.

Press the **S2** and **S1** keys to switch between state and timing displays. As an example, this type of linkage could be used to monitor the subroutine called by the occurrence of an interrupt. You are encouraged to experiment with other linkage set-ups.

NOTE: Linkage conditions should not be set in both analyzers simultaneously. (Neither analyzer will trigger.)

6.3.4 ADVANCED WAVEFORM EXAMPLES (OPTIONAL WAVEFORM BOARD MUST BE INSTALLED)*

In this section, the optional waveform analyzer will be used to monitor the composite video signal coming from the video BNC connector of the NPC-700. In addition, the LINKAGE field in the timing menu will be set to **W** to illustrate the "single-shot" storage capability of the waveform analyzer.

WAVEFORM MODE

Press **RESET** and select the **WAVEFORM RECORDER** mode when the **CONFIGURATION LIST** appears.

WAVEFORM MENU

Set up the waveform menu in accordance with Figure 6-53. (Set **ATTENUATOR** to **200 mV/DIV**, **OFFSET** to **+0.10V**, and the **TRIGGER LEVEL** to **0.95**.)

```
WAVEFORM ANALYZER MENU

PROBE TYPE: X10
INPUT COUPLING: DC
ATTENUATOR: 200mV /DIV
OFFSET (-1.00 TO +1.00): +0.10
(DYNAMIC RANGE -0.64V TO +0.96V )
TRIGGER LEVEL (0.00 TO 1.00): 0.95
TRIGGER SLOPE: c

USE TIMING MENU TO SELECT SAMPLE PERIOD,
TRIGGER MODE AND LINKAGE
SET ARM OR TRIGGER LINKAGE TO "W" FOR NON-AUTO-TRIGGER
```

Figure 6-53. Waveform menu for monitoring the NPC-700's video signal.

CLOCK (100 nS)

Press the **S2** key followed by the **C** key to call the timing menu with the cursor at the clock field. Use a **100 nS** sample clock.

***NOTE:** A baseline in the waveform display will not be present if the **COLLECT** key is pressed when the Waveform Option is not installed.

**SINGLE-SHOT MODE
(W)**

Use the **NEXT** key to step to the TRIG LINKAGE field. Then use the **SELECT** key to enter a **W** into this field. Use the **NEXT** key again to step down to the PRETRIGGER field. Enter in a **0** for a pretrigger value of **00%**. See Figure 6-54.

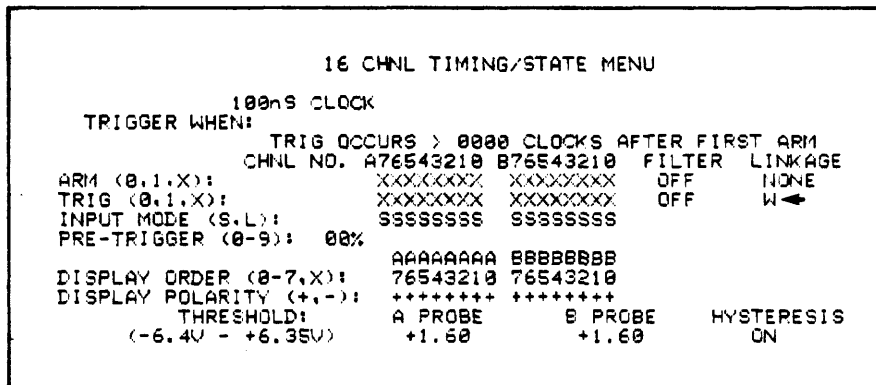


Figure 6-54. Timing menu set-up for waveform example.

NO INPUT SIGNAL

In the NPC-700, the timing menu is used to set up the waveform sample period and linkage. Setting a **W** into the LINKAGE field means that all triggering conditions associated with the waveform menu (such as threshold and slope) must be satisfied by the incoming analog signal in order to trigger the analyzer. Make certain that the Model 90 probe is set to X10 and plug it into the rear BNC connector labeled **WAVEFORM**. (In Section 6.2.4.2, the Model 90 probe was connected to the rear BNC connector labeled CTSA. It must now be moved to the **WAVEFORM** BNC.) With the ground clip attached to the body of any rear BNC connector, and the Model 90 probe tip unconnected, press **COLLECT**. Note that the waveform display is blank and the status message **ARMED** flashes on the CRT. This means that the **W** (or linkage) conditions are not being satisfied, so the waveform analyzer is inhibited from triggering.

VIDEO INPUT

Insert the probe tip into the rear BNC connector labeled **VIDEO**. Then press the **COLLECT** key to get a "clean" data collection. At 1X magnification, the display should look approximately as shown in Figure 6-55. The negative-going pulse after the video pulse group is the horizontal sync pulse. (Note: Since the video signal levels can vary from unit-to-unit, you may have to adjust the waveform menu settings slightly to match Figure 6-55.)

SECTION 6.0

ANALYSIS EXAMPLES

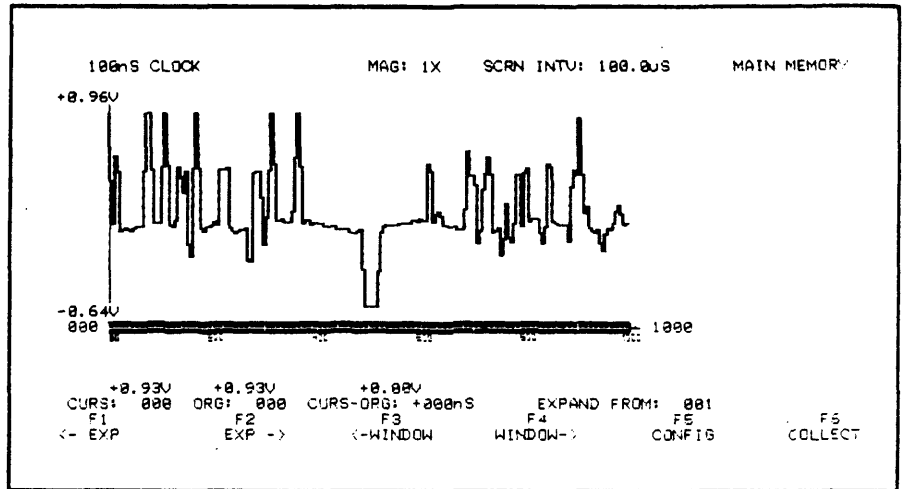


Figure 6-55. Video signal at 1X magnification.

EXPAND

Press the X2 (2), X5 (3), X10 (4), X20 (5) keys to view the video signal at different magnification factors. Return to X1 magnification and press the **EXPAND** \rightarrow key until the EXPAND FROM indicator at the lower-right-corner of the CRT corresponds to the approximate position in memory of the sync pulse. (No \bar{E} symbol is used in the waveform display.) Then press the X10 (4) key. Next press the **WINDOW** \leftarrow or \rightarrow keys as required to center the sync pulse. See Figure 6-56.

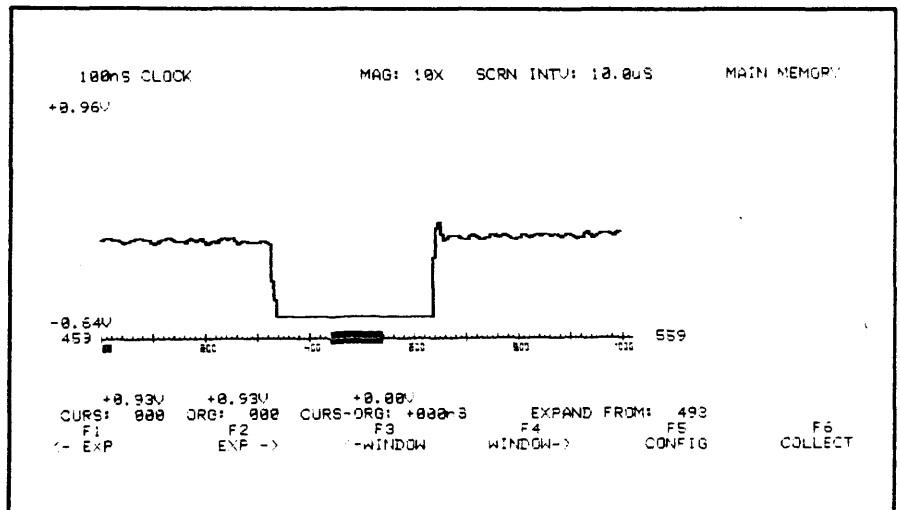


Figure 6-56. Examining the sync pulse at X10 magnification.

Return to 1X magnification and use the **EXPAND** key to return the **EXPAND FROM** indicator to 000. Then press the **X20** key to again view the video pulse group at X20 magnification.

SAVE (S)

Press the **SAVE (S)** key to store the waveform and menu in the auxiliary memory. Then press the **COMPARE (X)** key to compare main and auxiliary memories. Return to the main memory by pressing the **MEMSEL (M)** key as required. Next press **COLLECT** to take another data collection. Use the **X** key to compare the new collection with the reference collection. (There should be differences in both amplitude and time.) Return to the main memory.

MEASUREMENTS

Locate the cursor by pressing the **L** key. Experiment with making voltage and time measurements in the main and auxiliary memories using the cursor. The **ORIGIN (O)** key can be used here to relocate the origin from 000 to any cursor location.

6.3.5 ADVANCED COUNTER-TIMER/SIGNATURE ANALYSIS (OPTIONAL CT/SA BOARD MUST BE INSTALLED)*

6.3.5.1 ADVANCED COUNTER-TIMER EXAMPLE

In addition to the basic use of the counter-timer to measure simple events using the Model 90 probe, the NPC-700 can be used to make counter-timer measurements of bus or other state events as monitored by the three state probes.

STATE-RELATED MEASUREMENTS

Frequency, period, and count measurements can be made by specifying a cyclical or repeating data word or event; interval measurements can be made by specifying two data words or events. In both cases, the data word can be specified to be as wide as the total number of bits monitored by the state probes. For the NPC-764, for example, these include 48 bits of data from the A, B, and C channel probes and eight additional bits of clock qualifiers: six (two each) from the A, B, and C channel probes (AABBCC), one external trigger bit (E), and one linkage bit (L). The following procedure illustrates the use of the counter-timer for state-related measurements. As before, the A state probe should be plugged into the A side of the test card.

FREQUENCY

Press the **CONFIG** key and select the **COUNTER-TIMER** menu. In this example, the **FREQUENCY** mode with a 1 second gate time is used.

SOURCE: DATA

Next, step the cursor to the **SOURCE** field and select **DATA**. When **DATA** is the source, the field for the data word is automatically displayed in the format previously selected in the state menu. Then enter the data word: **0040** (rest X's). See Figure 6-57.

***NOTE:** The rectangular display window will be blank if the CT/SA option is not installed.

COLLECT

Press the **COLLECT** key to begin the counter-timer. Notice that the display indicates the frequency of occurrence of the specified data word being monitored by the A probe. (The remaining bits of the B and C channel probes are each set to DON'T CARE as are the clock qualifier bits AABBC EL.) Pressing the **HOLD (F4)** key will cause the last measurement to be held on the display. Pressing **COLLECT** again will cause the counter-timer to resume making measurements.

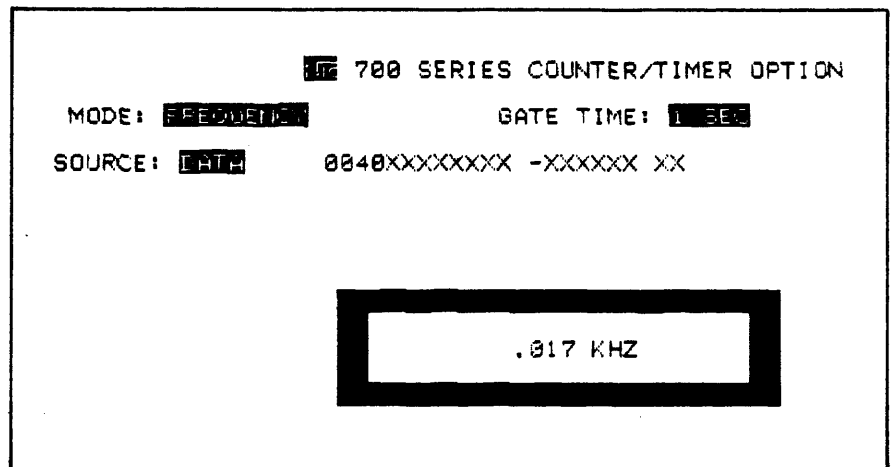


Figure 6-57. Counter-timer display indicating the frequency of occurrence of a specified data word. (NPC-764 shown.)

SELECT

Move the cursor through the menu and back to the **MODE** field. Note that the counter-timer remains functioning and collecting even while the cursor is moved within the menu. Press the **SELECT** key to change modes to **PERIOD**, **INTERVAL**, and **TOTAL** and watch the display reflect the mode selected.

As in the basic counter-timer example, pressing the **HOLD** key holds the measured data; while pressing the **COLLECT** key restarts the measurement.

INTERVAL MODE

All of the modes with the exception of **INTERVAL** require only a single event. As the name implies, **INTERVAL** refers to the time between two events and thus requires two data words: **START** and **STOP**. When the **INTERVAL** mode is entered, the fields for the two data words are displayed. The fields represent the word recognizers of the state analyzer.

COLLECT

Select the **INTERVAL** mode and step the cursor to the **SOURCE** field. Enter **0040** (rest X's) and **00FF** (rest X's) in the **START** and **STOP** fields, respectively. When finished, press the **COLLECT** key and watch the display indicate the interval (in μ s) between the two data words. See Figure 6-58. Note that the interval timer will continue making and displaying measurements until the **HOLD** key is pressed.

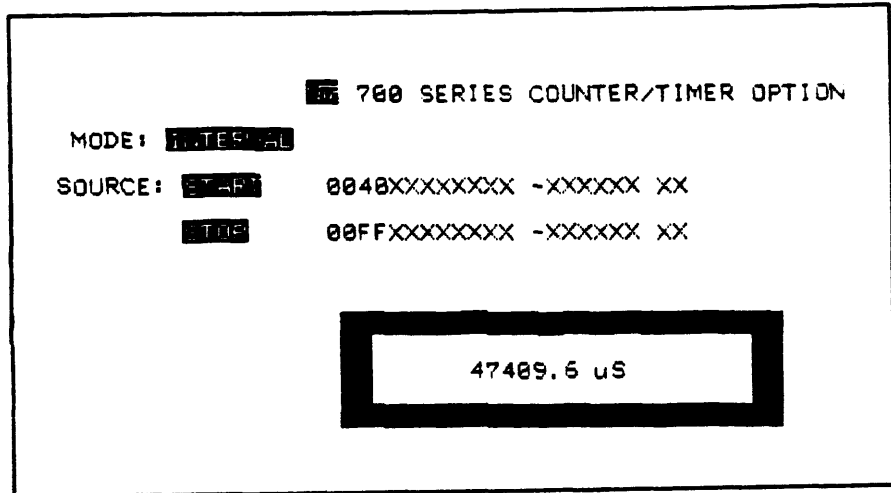


Figure 6-58. Counter-timer measurements of the interval between START and STOP data words. (NPC-764 shown.)

6.3.5.2 ADVANCED SIGNATURE ANALYSIS EXAMPLE

The NPC-700's signature analyzer provides additional capabilities which could be used to test complex state sequences. Often, digital systems do not contain separate on-board start and stop signals representing complex events. The NPC-700's word recognition circuitry can be used to supply the necessary signals. (In the basic example of Section 6.2.4.2, a single bit was used for both start and stop signals.) For advanced applications, the entire trigger word can be used to control the signature analyzer. The E bit provides a single bit qualification for independent synchronization from a signal anywhere in the circuitry you're testing. The L bit provides a powerful linkage capability to one or more additional logic analyzers.

SOFTWARE SIGNATURES

As a practical example, the beginning and ending addresses of a software routine could be used to gate the signature analyzer. By placing the Model 90 probe on the LSB of the address word during program execution, a unique signature of the executing code is obtained. In this manner, faulty software or "unannounced" revs can be rapidly uncovered.

6.4 RS-232/IEEE-488 EXAMPLES (NPC-764)

See Section 14.3, Transmission Examples

6.5 DISASSEMBLY EXAMPLE

In order to simplify the tracing of a microprocessor's program, NPC offers dedicated probes with disassembly software for most of the popular 8 and 16 bit microprocessors. (Dedicated probes are described in general in Section 4.6.)

"DISASSEMBLING" THE TEST CARD

Even if you do not currently have a dedicated probe, you can still "disassemble" data patterns from the test card.

0040

Connect the A and B state probes to corresponding connectors on the test card. Call the state menu and set the A-channel trigger to 0040.

COLLECT

For the NPC-764, press the COLLECT key and display the data in hexadecimal, or any other format desired.

CP/M*
DIR (NPC-764)

Press the CONFIG key and then press ESC to call the CP/M operating system. When the cursor appears, type DIR to see what disassembly programs are on your diskette.

LADISA
DZ80

Type LADISA DZ80 to load the disassembler for the Z80. When the CONFIGURATION LIST appears, press the S1 key to view the data previously collected from the test card. Then type 1 for a disassembled display. See Figure 6-59.

```

MAIN      TRIG 0040  NOP
          +001 0041  OPERAND FETCH
LOC:      +002 0042  HIGH READ
          +003 0043  HIGH
SIG: C1E7 +004 0044  INPUT
          19E7 +005 0045  INPUT
          C8BB +006 0046  INPUT
          +007 0047  INPUT
          +008 0048  DJNZ 005BH
          +009 0049  INPUT
          +00A 004A  INPUT
          +00B 004B  INPUT
          +00C 004C  INPUT
          +00D 004D  INPUT
          +00E 004E  INPUT
          +00F 004F  INPUT
          +010 0050  DJNZ 006BH
          +011 0051  INPUT
          +012 0052  INPUT
          +013 0053  INPUT
          +014 0054  INPUT
          +015 0055  INPUT
          +016 0056  INPUT
          +017 0057  INPUT
          +018 0058  INPUT
          +019 0059  INPUT
          +01A 005A  INPUT
          +01B 005B  INPUT
          +01C 005C  INPUT
          +01D 005D  INPUT
          +01E 005E  INPUT
          +01F 005F  INPUT
          +020 0060  INPUT
          +021 0061  INPUT
          +022 0062  INPUT
          +023 0063  INPUT
          +024 0064  INPUT
          +025 0065  INPUT
          +026 0066  INPUT
          +027 0067  INPUT
          +028 0068  INPUT
          +029 0069  INPUT
          +02A 006A  INPUT
          +02B 006B  INPUT
          +02C 006C  INPUT
          +02D 006D  INPUT
          +02E 006E  INPUT
          +02F 006F  INPUT
          +030 0070  INPUT
          +031 0071  INPUT
          +032 0072  INPUT
          +033 0073  INPUT
          +034 0074  INPUT
          +035 0075  INPUT
          +036 0076  INPUT
          +037 0077  INPUT
          +038 0078  INPUT
          +039 0079  INPUT
          +03A 007A  INPUT
          +03B 007B  INPUT
          +03C 007C  INPUT
          +03D 007D  INPUT
          +03E 007E  INPUT
          +03F 007F  INPUT
          +040 0080  INPUT
          +041 0081  INPUT
          +042 0082  INPUT
          +043 0083  INPUT
          +044 0084  INPUT
          +045 0085  INPUT
          +046 0086  INPUT
          +047 0087  INPUT
          +048 0088  INPUT
          +049 0089  INPUT
          +04A 008A  INPUT
          +04B 008B  INPUT
          +04C 008C  INPUT
          +04D 008D  INPUT
          +04E 008E  INPUT
          +04F 008F  INPUT
          +050 0090  INPUT
          +051 0091  INPUT
          +052 0092  INPUT
          +053 0093  INPUT
          +054 0094  INPUT
          +055 0095  INPUT
          +056 0096  INPUT
          +057 0097  INPUT
          +058 0098  INPUT
          +059 0099  INPUT
          +05A 009A  INPUT
          +05B 009B  INPUT
          +05C 009C  INPUT
          +05D 009D  INPUT
          +05E 009E  INPUT
          +05F 009F  INPUT
          +060 00A0  INPUT
          +061 00A1  INPUT
          +062 00A2  INPUT
          +063 00A3  INPUT
          +064 00A4  INPUT
          +065 00A5  INPUT
          +066 00A6  INPUT
          +067 00A7  INPUT
          +068 00A8  INPUT
          +069 00A9  INPUT
          +06A 00AA  INPUT
          +06B 00AB  INPUT
          +06C 00AC  INPUT
          +06D 00AD  INPUT
          +06E 00AE  INPUT
          +06F 00AF  INPUT
          +070 00B0  INPUT
          +071 00B1  INPUT
          +072 00B2  INPUT
          +073 00B3  INPUT
          +074 00B4  INPUT
          +075 00B5  INPUT
          +076 00B6  INPUT
          +077 00B7  INPUT
          +078 00B8  INPUT
          +079 00B9  INPUT
          +07A 00BA  INPUT
          +07B 00BB  INPUT
          +07C 00BC  INPUT
          +07D 00BD  INPUT
          +07E 00BE  INPUT
          +07F 00BF  INPUT
          +080 00C0  INPUT
          +081 00C1  INPUT
          +082 00C2  INPUT
          +083 00C3  INPUT
          +084 00C4  INPUT
          +085 00C5  INPUT
          +086 00C6  INPUT
          +087 00C7  INPUT
          +088 00C8  INPUT
          +089 00C9  INPUT
          +08A 00CA  INPUT
          +08B 00CB  INPUT
          +08C 00CC  INPUT
          +08D 00CD  INPUT
          +08E 00CE  INPUT
          +08F 00CF  INPUT
          +090 00D0  INPUT
          +091 00D1  INPUT
          +092 00D2  INPUT
          +093 00D3  INPUT
          +094 00D4  INPUT
          +095 00D5  INPUT
          +096 00D6  INPUT
          +097 00D7  INPUT
          +098 00D8  INPUT
          +099 00D9  INPUT
          +09A 00DA  INPUT
          +09B 00DB  INPUT
          +09C 00DC  INPUT
          +09D 00DD  INPUT
          +09E 00DE  INPUT
          +09F 00DF  INPUT
          +0A0 00E0  INPUT
          +0A1 00E1  INPUT
          +0A2 00E2  INPUT
          +0A3 00E3  INPUT
          +0A4 00E4  INPUT
          +0A5 00E5  INPUT
          +0A6 00E6  INPUT
          +0A7 00E7  INPUT
          +0A8 00E8  INPUT
          +0A9 00E9  INPUT
          +0AA 00EA  INPUT
          +0AB 00EB  INPUT
          +0AC 00EC  INPUT
          +0AD 00ED  INPUT
          +0AE 00EE  INPUT
          +0AF 00EF  INPUT
          +0B0 00F0  INPUT
          +0B1 00F1  INPUT
          +0B2 00F2  INPUT
          +0B3 00F3  INPUT
          +0B4 00F4  INPUT
          +0B5 00F5  INPUT
          +0B6 00F6  INPUT
          +0B7 00F7  INPUT
          +0B8 00F8  INPUT
          +0B9 00F9  INPUT
          +0BA 00FA  INPUT
          +0BB 00FB  INPUT
          +0BC 00FC  INPUT
          +0BD 00FD  INPUT
          +0BE 00FE  INPUT
          +0BF 00FF  INPUT
          +0C0 0100  INPUT
          +0C1 0101  INPUT
          +0C2 0102  INPUT
          +0C3 0103  INPUT
          +0C4 0104  INPUT
          +0C5 0105  INPUT
          +0C6 0106  INPUT
          +0C7 0107  INPUT
          +0C8 0108  INPUT
          +0C9 0109  INPUT
          +0CA 010A  INPUT
          +0CB 010B  INPUT
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```

**UNUSED STATE
CHANNELS**

USER FORMAT (U)

Since NPC's 8-bit dedicated probes require 32 channels (A & B), there are 16 additional state channels in the NPC-764 (and 16 additional timing channels in both the NPC-764 and NPC-748) available for monitoring other signals in your system. To view additional state channels in the NPC-764, simply type the key corresponding to the desired display format. (See the LABELS field.) For example, if you are using a mixed format, type U to call all 48 channels (A, B, and C) of state data in that format. Then type 1 to again disassemble the data associated with the A and B probe inputs.

Good luck, and remember, for additional information or assistance, contact our Applications Engineering department at:

(800) 642-6538 (Toll-free outside California)

(415) 490-8300 (California)

(910) 381-7030 (TWX)

**NICOLET PARATRONICS CORPORATION
201 Fourier Avenue
Fremont, California 94539**

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SECTION 7.0

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7.0 REFERENCE

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7.1.1 HEX-ASCII

ASCII & GPIB CODE CHART																							
B7 B6 B5 BITS		B B B		B B 1		B 1 B		B 1 1		1 B B		1 B 1		1 1 B		1 1 1							
CONTROL				NUMBERS SYMBOLS				UPPER CASE				LOWER CASE											
B4	B3	B2	B1	0	20	40	60	100	120	140	160	0	20	40	60								
B B B B	0	BREAK NUL	0	20	DLE	10	16	20	32	30	48	40	@	64	50	80	60	96	70	p	112		
B B B 1	1	GTL SOH	1	21	S1 DC1	11	17	21	33	31	49	41	A	65	51	81	61	a	97	71	q	113	
B B 1 B	2	STX	2	22	S2 DC2	12	18	22	34	32	50	42	B	66	52	82	62	b	98	72	r	114	
B B 1 1	3	ETX	3	23	F1 DC3	13	19	23	35	33	51	43	C	67	53	83	63	c	99	73	s	115	
B 1 B B	4	SDC EOT	4	24	F2 DC4	14	20	24	36	34	52	44	D	68	54	84	64	d	100	74	t	116	
B 1 B 1	5	PPC ENQ	5	25	F3 NAK	15	21	25	37	35	53	45	E	69	55	85	65	e	101	75	u	117	
B 1 1 B	6	F4 ACK	6	26	SYN	16	22	26	38	36	54	46	F	70	56	86	66	f	102	76	v	118	
B 1 1 1	7	TAB BEL	7	27	F5 ETB	17	23	27	39	37	55	47	G	71	57	87	67	g	103	77	w	119	
1 B B B	8	GET BS	8	30	F6 CAN	18	24	28	40	38	56	48	H	72	58	88	68	h	104	78	x	120	
1 B B 1	9	TCT HT	9	31	LABELS EM	19	25	29	41	39	57	49	I	73	59	89	69	i	105	79	y	121	
1 B 1 B	10	A LF	10	32	SUB	1A	26	2A	42	3A	58	4A	J	74	5A	90	6A	j	106	7A	z	122	
1 B 1 1	11	B VT	11	33	ESC	1B	27	2B	43	3B	59	4B	K	75	5B	91	6B	k	107	7B	{	123	
1 1 B B	12	C FF	12	34	FS	1C	28	2C	44	3C	60	4C	L	76	5C	92	6C	l	108	7C		124	
1 1 B 1	13	D CR	13	35	GS	1D	29	2D	45	3D	61	4D	M	77	5D	93	6D	m	109	7D	}	125	
1 1 1 B	14	E SO	14	36	RS	1E	30	2E	46	3E	62	4E	N	78	5E	94	6E	n	110	7E	~	126	
1 1 1 1	15	F SI	15	37	US	1F	31	2F	47	3F	63	4F	O	79	5F	95	6F	o	111	7F	DEL (RUBOUT)	127	
		ADDRESSED COMMANDS		UNIVERSAL COMMANDS		LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES OR COMMANDS													

KEY

octal	25	PPU	GPIB code
	NAK		ASCII character
hex	15	21	decimal

REF: ANSI STD X3. 4-1977
IEEE STD 488-1978

7.1.2 HEX-DECIMAL

F E D C		B A 9 8		7 6 5 4		3 2 1 0	
Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal
0	0	0	0	0	0	0	0
1	4,096	1	256	1	16	1	1
2	8,192	2	512	2	32	2	2
3	12,288	3	768	3	48	3	3
4	16,384	4	1,024	4	64	4	4
5	20,480	5	1,280	5	80	5	5
6	24,576	6	1,536	6	96	6	6
7	28,672	7	1,792	7	112	7	7
8	32,768	8	2,048	8	128	8	8
9	36,864	9	2,304	9	144	9	9
A	40,960	A	2,560	A	160	A	10
B	45,056	B	2,816	B	176	B	11
C	49,152	C	3,072	C	192	C	12
D	53,248	D	3,328	D	208	D	13
E	57,344	E	3,584	E	224	E	14
F	61,440	F	3,840	F	240	F	15

7.1.3 OCTAL-TO-BINARY-
TO-HEX

<u>OCTAL</u>	<u>BINARY</u>	<u>HEX</u>	<u>BINARY</u>
0	000	0	0000
1	001	1	0001
2	010	2	0010
3	011	3	0011
4	100	4	0100
5	101	5	0101
6	110	6	0110
7	111	7	0111
		8	1000
		9	1001
		A	1010
		B	1011
		C	1100
		D	1101
		E	1110
		F	1111

Example: Convert (7412) OCT to HEX equivalent

Procedure: $\frac{7}{111}$ $\frac{4}{100}$ $\frac{1}{001}$ $\frac{2}{010}$ OCTAL WORD
OCTAL BINARY
GROUPING

(Extra Zeroes 0000) 1111 0000 1010 HEX BINARY
GROUPING

0 F 0 A HEX WORD

Thus: (7412) OCT = (0F0A) HEX

7.1.4 HEX-DECIMAL-ASCII
EQUIVALENTS FOR
SOFT-KEYS

KEY	HEX	ASCII	DECIMAL
S1	11	CONTROL-Q	17
S2	12	CONTROL-R	18
F1	13	CONTROL-S	19
F2	14	CONTROL-T	20
F3	15	CONTROL-U	21
F4	16	CONTROL-V	22
F5	17	CONTROL-W	23
F6	18	CONTROL-X	24
LABELS	19	CONTROL-Y	25

7.2 CLOCKS AND QUALIFIERS

7.2.1 CLOCK

The clock is the signal that strobes each data word into the analyzer and initiates the recording of that data word into the analyzer's memory. In order to use the full capabilities of the NPC-700, it is important to understand the two different types of clocks and clock qualifiers.

EXTERNAL CLOCK

This is an input signal from the system-under-test which governs the **synchronous** collection of data by the analyzer. In order to ensure reliable data collection, the active (rising or falling) edge of this clock must occur when the data are stable. Data collected in this manner are usually considered to be **state** data.

INTERNAL CLOCK

This is a signal generated by the analyzer for **asynchronous** collection of data. The higher the sampling rate, the better the time resolution between events. As a conservative rule-of-thumb, the internal sampling clock should be approximately 5 to 10 times faster than the fastest signal in the system being analyzed. Data collected in this manner are usually considered to be **timing** data. The NPC-700's internal clock offers sampling times ranging from 10 nS to 10 mS.

CLOCK QUALIFIERS

Qualifiers are additional data collection control lines that come into the analyzer's probes from the system-under-test. Their fundamental use is to filter (i.e. qualify) the incoming data so that only specific information defined by the user is collected by the analyzer. In this manner, the analyzer's data memory is used more efficiently.

As described below, there are three types of qualifiers: external clock qualifier bits, internal clock qualifier words, and trigger qualifiers. In the NPC-700, qualifiers are used only in the state (synchronous) modes of operation.

EXTERNAL CLOCK QUALIFIER BIT

An external clock qualifier bit is a bit from the system-under-test that is ANDed with the incoming (external) clock. When this bit is TRUE (i.e., when it matches the logic level set in the clock qualifier field), the data present at the clock edge is collected. When this bit is false, the analyzer behaves as if no clock at all had occurred. The NPC-700 incorporates up to 7 external clock qualifier bits as described below.

INTERNAL CLOCK QUALIFIER WORD

The NPC-764's 48 CHANNEL STATE mode offers two logically ORed 48-bit-wide internal clock qualifier words. These clock qualifier words are termed "internal" since the normal, incoming, 48-bit data words from the state probes are tested against a pre-specified pattern to see if they "qualify" for collection. For the NPC-748, the internal clock qualifier word is 32 bits wide.

CLOCK QUALIFIER FIELD

For the NPC-764's 48 CHANNEL STATE mode, each of the two clock qualifier fields consists of the 48-bit-wide internal portion and a 7-bit-wide external portion made up of two input lines (Q1 and Q2) coming from each of the 3 state probes (A, B, C) plus external input line (E) from a rear BNC connector. Figure 7-1

shows the two clock qualifier fields. The NPC-748's two clock qualifier fields are identical except that the internal portion is 32 bits wide and the external portion is 5 bits wide.

The internal fields in Figure 7-1 are set to 004 and 005 (rest are set to X) while the external fields are all set to X (don't care). The external fields are preceded by a "-" and have the label: -AABBCCCEL as shown in the upper-right-hand portion of the menu. (The L bit is not used in the clock qualifier field.)

```

FORMAT: AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA
        A HEX
CLK SEL: A PRB: J B PRB: A C PRB: A QUALIFIERS: -AABBCC EL
CLK QUAL: 004XXXXXXXXX -XXXXXX X
          OR 005XXXXXXXXX -XXXXXX X
PRE-TRIG MEMORY (0-249): 000 WORDS
RESTART: OFF
TRIGGER: 0
          0040XXXXXXXXX -XXXXXX XX
        END

```

S2 - DATA DISPLAY

Figure 7-1. Clock qualifier fields with 004 and 005 as qualifier words. (NPC-764 shown.)

The incoming data is tested against both specified clock qualifier patterns (at the selected clock edge). If the incoming data matches **either** pattern, then the analyzer recognizes that a qualified clock has occurred and stores the associated data word. Note that either internal clock qualifier word must match incoming data words that are to be collected; while either external field provides the clock qualification function only and is not collected.

CLOCK QUALIFIER APPLICATIONS

A typical application of the internal qualifier field is to set up a clock qualifying condition (0's, 1's, and X's) to match the occurrence of a certain address word, A. Every time A occurs, the analyzer will collect both the address and the associated data. In this manner, you can obtain a list of all the data changes occurring at address A.

Another application is to qualify the clock over a range of addresses by "don't caring" part of the address word. Using this feature, you can collect a table of data words associated with the address range of interest. For example, for the NPC-764, let's say you're interested in the data between the HEX addresses 00F0 and 00FF. Assuming no other qualification is necessary, you'd set up the following clock qualifier:

```
00FX XXXX XXXX -XXXXXX X .
```

Note that the least significant hex digit of the address portion of the qualifier word is set to "don't care," as is the rest of the word. With this clock qualifier, the NPC-764 will collect addresses and data only over the range 00F0 to 00FF.

NOTE: A special feature of newer NPC-700's allows the trigger word to differ from the qualified data collection. Thus, in the above example, the NPC-764 would still trigger even if the trigger word was completely different from 00FX. However, this trigger word must be valid (i.e., exist in the system-under-test); otherwise the analyzer will not trigger.

Another common application of clock qualifiers is to purge undesired state events in your system using the external clock qualifier field. For example, if you want to collect data only when a certain control signal is high, you could connect a clock qualifier on the A probe to that signal and set the first A qualifier bit in either of the clock qualifier words to a logic one. Data will then be collected only when the specified signal is high.

7.3 TRIGGERS AND QUALIFIERS

7.3.1 TRIGGER WORD

This is a user-specified data pattern which identifies the beginning or end of a data collection. If the pretrigger condition is specified as 000, then the trigger word identifies the beginning of the collection.

TRIGGER

Each trigger word in the stack can be set individually for **nonoccurrence triggering**. This means that the analyzer will trigger on **anything but** a particular trigger word. This feature is extremely useful for tracing what happened in place of an expected event.

7.3.2 TRIGGER QUALIFIER BITS

For the NPC-764, there are up to 8 extra bits (2 each from the A, B, and C state probes plus an external (E) bit and a linkage (L) bit) which are ANDed with the trigger word. The extra bits impose additional conditions on triggering: Unless these qualifier bits are TRUE simultaneously with the trigger word, the analyzer will not trigger. Note that the extra trigger qualifier bits are not displayed. The NPC-748 is identical except that this trigger qualifier field is 6 bits wide.

7.3.3 TRIGGER QUALIFIER FIELDS, LINKAGE

The NPC-764's trigger qualifier field and associated header (-AABBCC EL) are shown in Figure 7-2. (The header for the NPC-748 is -AACC EL). When the last (L) bit is set to a logic one, the triggering of the state analyzer is conditioned on the occurrence of a logic low-level signal on the linkage bit open-collector bus. This linkage signal can be provided by the TIMING/WAVEFORM section or an external analyzer.


```

FORMAT: AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA AAAAAAAAA
        A HEX
CLK SEL: A PRB: J B PRB: A C PRB: A QUALIFIERS: -AABBCC EL
CLK QUAL: 004XXXXXXXXX -XXXXXX X
          OR 005XXXXXXXXX -XXXXXX X
PRE-TRIG MEMORY (0-249): 000 WORDS
RESTART: OFF
TRIGGER: 0040XXXXXXXX -001100 11 ←
        0
        END

```

Figure 7-2. Trigger qualifier field. (NPC-764 shown.)

7.3.4 RESTART

When this word is detected, it causes the stack to return to level 0 (the top of the stack). Note that the RESTART word has priority over all other triggering conditions. When the RESTART word is detected, the stack returns to level 0 and a search for a new trigger word at level 0 begins 2 clock pulses following the RESTART word. (This 2-clock delay is necessary to initialize the stack.) See Section 6.3.1 for additional information.

NOTE: The setting of the RESTART word to X's "don't care" is **not the same** as turning it off. A RESTART word of all X's will continually hold the stack at level 0, and triggering will never occur.

RESTART

Any word which **does not match** the restart word will force the trigger stack back to level 0.

7.4 TIMING ANALYSIS: ARM AND TRIGGER WORDS

7.4.1 ARM AND TRIG

The NPC-700's Timing Analyzer Section provides two word recognizers called ARM and TRIG. These word recognizers are used to test for the presence (or absence) of specific patterns in the incoming data.

The ARM and TRIG conditions each consist of a pattern recognizer, a filter field and a linkage field. The pattern recognizer tests for the existence of a specified pattern in the incoming data. The filter field is used to specify that the data be present (and stable) for up to 9 consecutive clocks before it is recognized. The linkage field is used to extend the power of the NPC-700 by linking the timing analyzer to the state or waveform sections, or to other instruments.

The ARM or TRIG word recognizer does not output a TRUE signal until **all** the conditions set into the three fields are satisfied. For an illustration of the use of the ARM and TRIG word recognizers, see the advanced timing examples in Section 6.3.2.

7.5 HOLD# (#)

The HOLD# mode is used when it is desirable to compare **synchronously-collected** reference data in the **auxiliary** memory with the **current synchronous** data collection in the **main** memory. Applications include intermittent testing of hardware and monitoring areas of software for expected or unexpected jumps.

When the HOLD# key, #, is pressed, the analyzer performs the normal data collection and test code (SIG) computation functions associated with the COLLECT mode. However, in the HOLD# mode, the current signature is compared with the signature in the AUX memory; if they are the same, another collection is automatically initiated; if they are different, data collection stops and data are displayed.

7.6 MULTIPHASE CLOCKING

The NPC-700's State Analyzer Section can be used to demultiplex the shared address and data bus arrangement of 8085, 8086, and similar microprocessor chips. This demultiplexing action is desirable in order to simplify the tracing of program flow when the NPC-700 is connected directly to these chips. Demultiplexing allows you to view addresses and associated data or instructions side-by-side as if they were collected from separate busses.

**7.6.1 HOW MULTIPHASE
CLOCKING WORKS**

Each of the NPC-700's state probes has its own clock input. If one probe is assigned to the collection of addresses, the associated clock would be connected to the microprocessor's **ADDRESS VALID** strobe. Similarly, if the second probe is assigned to the collection of status words, its clock would be connected to the **STATUS VALID** strobe. For the NPC-764, the third probe could be clocked from yet a third clock. As is the case for single-phase clocking, the proper active edge for each of the clocks being used must be set in the state menu.

In the NPC-764, the C clock is considered the master and must always occur **after** the A and B* clocks. In the above example, the following sequence of events occur during data collection:

1. The A clock causes its associated address information to be loaded into the input latches.
2. The B clock strobes in its associated status information.
3. The C clock then strobes in its associated data word.
4. If all three words then meet additional clock qualification conditions, if any, they are transferred from the input latches into the data collection RAM by the C clock. The C clock is also used to advance the RAM address pointer and clock the sequencing logic.

Note that using the state menu, the B probe clock can be synchronized to the A probe clock and that the C probe clock can be synchronized to either the A or B probe clocks.

If more than one A or B clock occurs before the next qualified C clock, the most recent address information is stored in RAM. If the A or B clock is missing between a set of C clocks, the data in the RAM at that location will be "garbage."

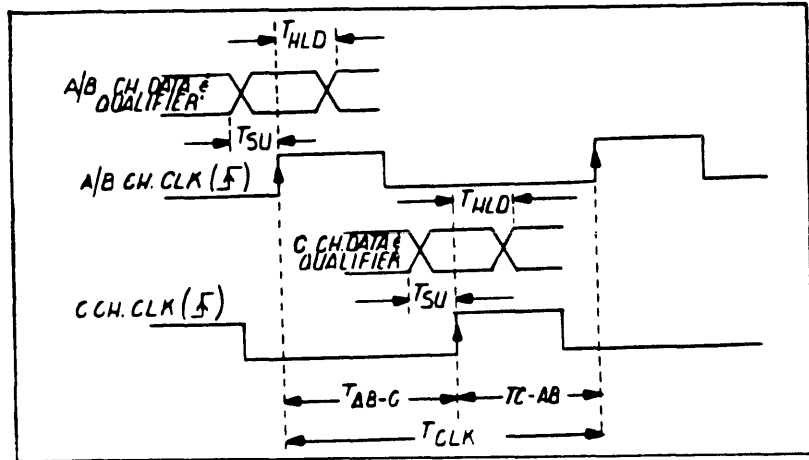
For the NPC-748, multiphase clocking works the same way except that there are only A and C clocks and the C clock is the master.

NOTE: Nicolet Paratronics' dedicated microprocessor probes automatically perform the multiphase clocking function for any microprocessors utilizing shared busses.

* The B probe and the associated clock is not used on the NPC-748.

**7.6.2 MULTIPHASE CLOCKING
TIMING RESTRICTIONS**

The diagram in Figure 7-3 illustrates the timing restrictions which apply when multiphase clocking is employed in the NPC-764. (For the NPC-748, delete the B clock.)



<u>PARAMETERS</u>	<u>DEFINITIONS</u>	<u>VALUE</u>
T_{HLD}	DATA HOLD TIME	0 nS MAX
T_{SU}	DATA SETUP TIME	20 nS MIN
T_{AB-C}	MIN A OR B TO C CLOCK DELAY	0 nS
T_{C-AB}	MIN C TO A OR B CLK DELAY	40 nS
T_{CLK}	MIN CLK PERIOD	70 nS

Figure 7-3. Multiphase clock timing.

7.7 PRETRIGGERING

Pretriggering is sometimes called Negative Triggering. Pretriggering means that the captured record consists of data which occurred before the trigger. Figure 7-4 shows a simple example of pretriggering.

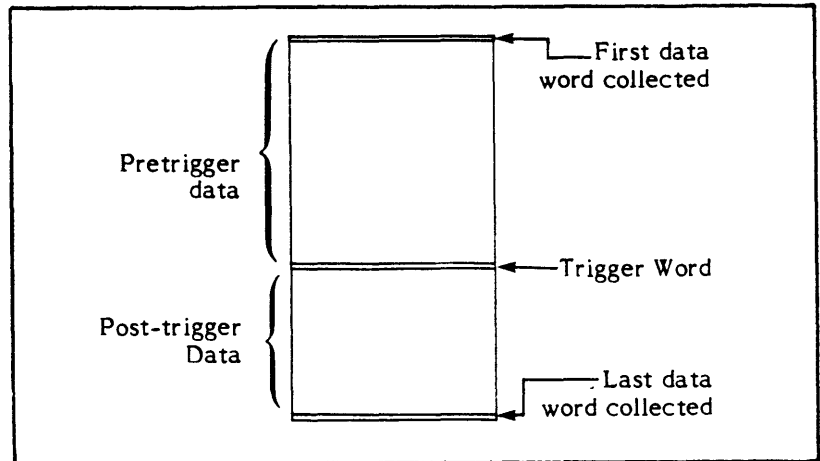


Figure 7-4. Pretriggering example.

7.7.1 PRETRIGGER IN THE TIMING ANALYZER

The NPC-700's Timing Analyzer has a maximum pretrigger value of 900 words in the 16 CHANNEL TIMING/STATE and 8 CHANNEL GLITCH modes; and 1800 words in the 8-channel 100 MHz mode. However, the pretriggering mechanism is designed so that any pretrigger value set in reflects the **maximum** number of data words that can be collected prior to the trigger. This means, for example, that if a pretrigger value of 200 (20%) was used, then the amount of data words collected prior to the trigger will be **between 1 and 200**. This type of pretrigger mechanism is employed so that the user doesn't have to be absolutely certain when he presses the **COLLECT** key that at least 200 events are going to occur prior to the trigger. If fewer events occur, the data collection will still be accomplished and the results displayed. (Other approaches cause the data collection to be inhibited if an internal pretrigger counter is not allowed to count down to zero, thereby losing the desired data collection.)

**7.7.2 PRETRIGGER IN THE
STATE ANALYZER**

The NPC-700's State Analyzer has a maximum pretrigger value of 999 words.* However, the pretriggering mechanism is designed so that any pretrigger value set in reflects the **maximum** number of data words that can be collected prior to the trigger. This means, for example, that if a pretrigger value of 225 was used, then the amount of data words collected prior to the trigger will be **anywhere** between 1 and 225. This type of pretrigger mechanism is employed so that the user doesn't have to be absolutely certain when he presses the **COLLECT** key that at least 225 events are going to occur prior to the trigger. If fewer events occur, the data collection will still be accomplished and the results displayed. (Other approaches cause the data collection to be inhibited if an internal pretrigger counter is not allowed to count down to zero, thereby losing the desired data collection.)

NOTE: Due to the uncertainty in the amount of pretrigger words in the data collection when pretriggering is employed, the use of test codes (SIG) for test identification is generally **not** recommended. Furthermore, since the HOLD \neq mode compares auxiliary and main memory test codes, use of the pretrigger mode with HOLD \neq is also **not** recommended.

7.8 DISPLAY FORMATS

The NPC-700 is capable of displaying data in HEXADECIMAL, OCTAL, DECIMAL, BINARY, ASCII and timing diagram formats.

**7.8.1 STATE ANALYZER
DISPLAY FORMATS**

In the state analysis mode, the data can be displayed entirely in one format, i.e. all HEX or all OCTAL, or the display can be mixed, to include any combination of the 5 formats available.

The NPC-700's state display formatting allows you flexibility in presenting captured information for rapid evaluation of system operation. Furthermore, once the data is displayed in a mixed format, you can elect to display it in any single format by pressing the desired **H** (HEX), **O** (OCT), **N** (BIN), **Z** (DEC), or **Y** (ASCII) keys. Then you can return to the mixed mode by pressing the **FORMAT** key. This feature allows you to use the NPC-700 for code conversions.

Once a mixed-format is selected, the clock qualifier group, the restart word, all 16 trigger levels, and the counter-timer/signature analyzer data entry fields, are formatted in exactly the same way. (Also note that when the cursor is in any of these fields, that field can be changed to any other format.)

***NOTE:** An early version of the NPC-700 incorporated a 250-word state memory with a pretrigger capability of 249 words.

7.8.2 MIXED FORMAT EXAMPLE

If you were using the NPC-700 to monitor an 8-bit microprocessor, you might select the 16-bit address bus and the 8-bit data bus for hexadecimal display, and 7 status bits for display in binary. The remaining bits might be unused. For these formats, the menu would be set up as follows:

```

                                48 CHANNEL STATE MENU
FORMAT:  AAAAAAAAA AAAAAAAAA BBBB BBBB CCCCCCX XXXXXXXX XXX.XXX.X
          A HEX B HEX C BIN
CLK SEL:  A PRB: J B PRB: A C PRB: A QUALIFIERS: -AABBCC EL
CLK QUAL: 004X XX XXXXXXXX -XXXXXX X
          OR OFF
PRE-TRIG MEMORY (0-249): 000 WORDS
RESTART:  0003 XX XXXXXXXX -XXXXXX XX
TRIGGER:
0
END

```

Figure 7-5. Mixed display format in state menu.
(NPC-764 shown.)

NOTE: The labels identifying bit groupings must be used in the sequence A-F, except that X's (blank) can be interspersed anywhere in the FORMAT field. (Label meanings are defined in the menu on the line below the FORMAT field.)

After pressing **COLLECT**, the resulting data display might look something like this:

MAIN	TRIG	0040	00	00000000
	+001	0041	30	00000000
LOC: 7820	+002	0042	40	00000001
	+003	0043	C0	00000001
SIG: 17BF	+004	0044	20	00000100
AD4B	+005	0045	A0	00000100
100F	+006	0046	60	00000111
	+007	0047	E0	00000111
	+008	0048	10	00001000
	+009	0049	90	00001000
	+010	004A	50	00001001
	+011	004B	D0	00001001
	+012	004C	30	00001100
	+013	004D	B0	00001100
	+014	004E	70	00001111
	+015	004F	F0	00001111
	+016	0040	00	00000000
	+017	0041	80	00000000
	+018	0042	40	00000001
	+019	0043	C0	00000001

Figure 7-6. Mixed format display for microprocessor example. (NPC-764 shown.)

7.8.3 TIMING ANALYZER STATE DISPLAY

The timing analyzer can display the data in only one state format at a time.

7.8.4 TIMING ANALYZER TIMING DISPLAY

The timing analyzer is commonly used to display asynchronous data in the timing diagram format, which gives a graphic representation of the sampled data and permits timing relationships to be readily measured.

7.9 GLITCH CAPTURING

The NPC-700 has up to 16 timing channels which can be individually set to the **SAMPLE** or **LATCH** mode by entering an **S** or **L** in the appropriate location in the menu's **INPUT MODE** field.

In the **8 CHANNEL GLITCH** mode, the 8 channels corresponding to the **B** probe (which is not used) are automatically set to **L** and are transparent to the user. The 8 channels corresponding to the **A** probe are set to **S**. In operation, both **A** and **B** 8-channel memories record simultaneously. A glitch is displayed in each bit location that differs between the two memories.

NOTE: When using the 8-channel glitch mode, it is not necessary to change the S settings of the INPUT MODE field.

**7.9.1 SAMPLE MODE
(16-CHANNEL TIMING
CONFIGURATION)**

In the SAMPLE mode, the NPC-700 will collect data at the occurrence of the sampling clock edge. This edge is selectable as rising or falling for external clock operation. However, for internal clock operation, data words are always sampled on the rising edge. For external clock operation, valid data are defined as those words which are stable for at least the 5 nS set-up time prior to the edge, and held for a 10 nS hold time after the edge. In the SAMPLE mode, transitions occurring between clock edges will be ignored.

**7.9.2 LATCH MODE
(16-CHANNEL TIMING
CONFIGURATION)**

In the LATCH mode, the analyzer "remembers" the previous sample and arms a latch to capture any transitions occurring before the next sample clock edge. If a transition does occur, the latch is set and sampled at the next clock edge. The latch circuit is sensitive to transitions of 5 nS duration or longer. In the case of a narrow glitch whose width is less than the clock sample period, the display will show the glitch as one clock period wide.

The LATCH mode is also useful for capturing normal system pulses that happen to be shorter than the sample period being used for data collection. For example, assume the timing analyzer is sampling using a 200 nS clock, and that this clock sample rate is appropriate for collecting data on 7 of the 8 channels. The 8th channel is connected to a signal that has a 50 nS pulse width and a 1 mS period. In the SAMPLE mode, this signal will often be missed. However, setting the LATCH mode for the 8th channel will ensure capturing every pulse.

NOTE: The SAMPLE and LATCH fields are generally used in the 16 CHANNEL TIMING mode only. As stated above, the 8 CHANNEL GLITCH mode automatically sets these fields for proper glitch memory operation.

**7.9.3 SAMPLE AND LATCH
MODE TIMING**

Figure 7-7 shows how the SAMPLE and LATCH modes respond to a glitch.

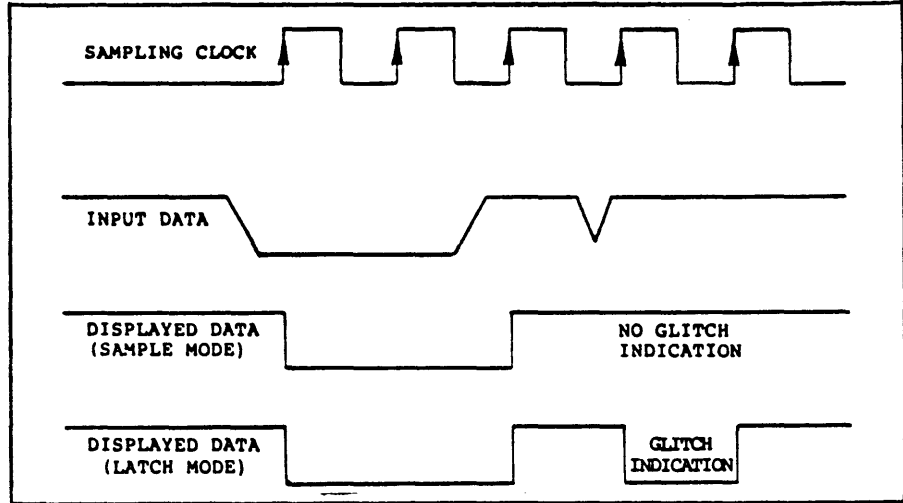


Figure 7-7. Sample and latch mode timing. (Glitch memory not used.)

**7.9.4 8-CHANNEL TIMING
GLITCH MODE**

When using the NPC-700's 8-CHANNEL TIMING GLITCH configuration, the analyzer splits its 1000-word, 16-channel memory into an 8-channel data memory plus an 8-channel glitch memory. Glitches of 5 nS duration or longer that occur between sample clock edges are stored in the separate glitch memory. Upon display, a glitch is shown as a vertical line interspersed with the data. See Figure 7-8.

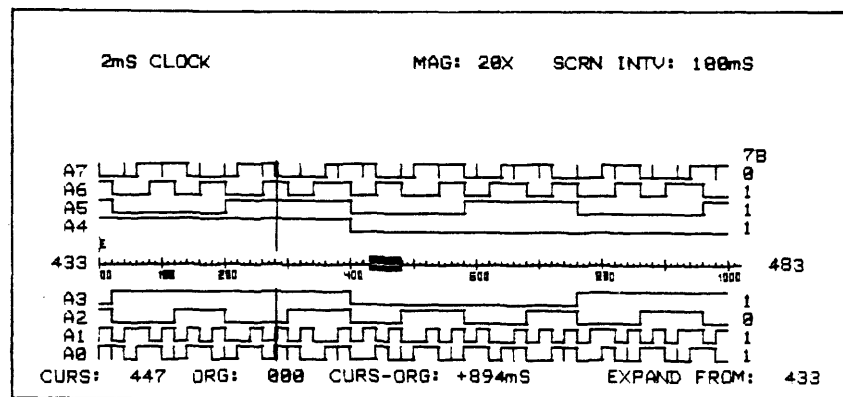


Figure 7-8. Glitches interspersed with data.

NOTE: The NPC-700 also allows you to view the state equivalent display of the data and glitch memories side-by-side. By pressing the S1 key and choosing a binary format, you can achieve an alternative and sometimes more complete way of locating glitches. Simply compare the binary glitch table (on the right) with the data word table. In each location where a logic 1 occurs in the glitch table, a glitch is present on the corresponding data channel. In this manner, glitches that are coincident with the rising or falling edges of valid data can be detected.

7.10 LINKING ANALYSIS* RESOURCES

Part of the power of the NPC-700 lies in its ability to trace problems crossing between measurement domains. For example, the waveform section can be triggered from the occurrence of a pattern (or sequence of patterns) recognized by the timing/state section. Conversely, the timing/state section can be triggered by a signal monitored by the waveform section. The NPC-700 can also be linked (through the rear-panel LINK connector) to other NPC analyzer instruments for additional cross-domain triggering. The signal associated with this connector is called the L bit.

7.10.1 TIMING LINKAGE

The ARM and TRIG fields can each be linked to other internal or external measurement resources by stepping the cursor to the associated LINKAGE field and pressing the SELECT key until the desired combination is viewed. The linkage possibilities are: (W,L,E); (W,L); (W,E); (W); (L,E); (L); (E); or (NONE). These possibilities are described below.

7.10.2 STATE LINKAGE

The state analyzer can be linked to other internal or external measurement resources by specifying a 1 in the L bit of the trigger qualifier field.

The rear-panel BNC connector, labeled **LINK**, consists of an open-collector-driven line with a pull-up. This line is normally at a low (TTL) level, until the COLLECT key is pressed. The NPC-700 then releases the line. When another analyzer connected to the LINK BNC releases the line, it will go high and synchronize both analyzers to initiate a data collection. This high-to-low transition is detected by hardware in the analyzer with the link (L) bit set to one. The state and timing analyzers are both connected to this BNC connector.

7.10.3 EXTERNAL INPUT (E)

An additional qualifying input, denoted by an E in the LINKAGE or QUALIFIER fields, corresponds to a signal coming into the rear-panel BNC labeled EXTERNAL INPUT. This signal is provided as an extra qualifier bit for the ARM, TRIGGER and/or CLOCK QUALIFIER fields; however, it is not recorded. If selected, the E bit enables the associated ARM or TRIGGER to be recognized when the signal coming into the EXTERNAL INPUT BNC is a TTL logic 1.

***NOTE:** See Section 6.3.3 for a linkage example.

7.10.4 WAVEFORM LINKAGE (W)

Waveform linkage, denoted by a W in the timing menu, represents a signal from the triggering section of the waveform analyzer which detects when an incoming analog signal passes a specified threshold in a specified (positive-or negative-going) direction. (When using the WAVEFORM mode for routine, single-shot recordings, the W bit must be selected in the corresponding timing menu to inhibit free-running.)

NOTE: The waveform front-end always operates when the timing analyzer is in its data collection mode; therefore, the W linkage bit can be used as an additional triggering condition even though the analyzer is collecting timing information. Thus, you can specify the threshold and slope of a certain analog signal as a precondition to collecting state or timing data.

7.11 50/60 Hz OPERATION

The 50/60 Hz switch on the Processor Board should be set to the local power line frequency. See Section 2.3.7.

NOTE: A precise 50 or 60 Hz frame rate requires the appropriate crystal on the Processor Board as follows:

60 Hz operation - 13.2192 MHz
50 Hz operation - 13.0560 MHz

7.12 TEST CODES (SIG)

Nicolet Paratronics' special type of software signature analysis (or test codes) is standard on all NPC logic analyzers. It utilizes a post-data collection algorithm which compresses the data in the memory into a set of 4-digit hexadecimal identification codes. The algorithm operates on each data word (8 bits wide for the timing analyzer, 16 bits wide for the state analyzer) to produce independent test codes for each data grouping. One part of the algorithm utilizes the internal 8085's ADD and CARRY instruction which processes all the data words in the memory until a residue is formed. The residue contains bit-oriented (horizontal) significance due to the left-shifting carry action of the algorithm.

Another part of the algorithm keeps track of the relative position of each data word in the memory. This calculation adds "vertical" significance to the test code. The effect is to minimize the possibility of achieving identical test codes when the data collection contains the same data--but in a different order.

7.12.1 TEST CODE APPLICATIONS

To ensure repeatability, test codes can only be used with synchronously-collected state data. Even a 1-bit difference between two data collections will yield totally different test codes.

Applications of test codes include:

SOFTWARE VERIFICATION

Compute the test codes of a program to verify correct execution and to keep track of revisions.

TEST IDENTIFICATION

Compute the test codes associated with the normal operation of a known good system for comparison with a suspect system.

PARAMETRIC TESTING

Compute the test codes of a system-under-test while supply voltage, temperature, or other parameters are being varied to determine when these variations are just beginning to affect system operation.

The NPC-700 also uses test codes for its HOLD \neq mode. In this mode, the test code associated with auxiliary memory reference data is compared with the test code of main memory data. If the two codes differ, data collection is halted and the differences in both test codes and individual data bits can be displayed.

7.13 COMMON ANALYSIS PROBLEMS

Experience shows that most of the problems associated with using any logic analyzer fall into the following categories:

1. Insufficient knowledge of operation of the system-under-test (SUT).
2. Improper connection of the analyzer to the SUT.
3. Lack of knowledge concerning the operation of the analyzer, particularly in the areas of clocks, qualifiers, and triggering modes.

Items 1 and 2 are under your direct control; item 3 is the responsibility of Nicolet Paratronics to make the necessary information available through a detailed Operator's Manual, application notes, and any other means possible. If you encounter problems or have any questions whose answers are not readily available, please contact our Applications Engineering Department at:

(800) 642-6538 (toll-free outside California)
(415) 490-8300 (California)
TWX: 910-338-0201

Before we discuss some of the problems associated with item 3, we'd like to give you one piece of advice that we think you'll find invaluable in using the NPC-700:

START SIMPLE AND BUILD

In other words, first collect data without trigger qualification. Ask yourself, "Does the collection make sense?" It's both frustrating and a waste of time to proceed with complex triggering conditions until you're reliably collecting data using simpler modes. It's also a good idea to keep a record of your interconnections and menus in order to easily repeat previous tests.

TABLE 7-1. TABLE OF COMMON ANALYSIS PROBLEMS

<u>PROBLEM/DESCRIPTION</u>	<u>POSSIBLE CAUSE/SOLUTION</u>
1. No data collection or SLOW CLOCK warning.	1. a) Improper or too restrictive clock qualification. b) External clock input not connected. c) Probe threshold set incorrectly. d) System clock halted--use FORCE DISPLAY.
2. Data does not make sense.	2. a) Data not valid at selected clock edge. See Sections 4.1.3 and 4.2.3 for setup and hold time requirements. b) Noise or glitches on clock input signal. c) Improper clock sequence in multiphase clocking. See Section 7.6.
3. Analyzer will not trigger.	3. a) Triggering conditions too restrictive. Reduce restriction by using "don't care's" or removing triggering levels until a collection is made; then analyze the results. Build triggering conditions back up, step-by-step. b) Insufficient system clocks to fill data memory. The FORCE DISPLAY key can be used to view pre-trigger data.
4. Unstable data collection and signatures.	4. a) Non-repetitive input data. b) Noise on input or marginal timing conditions.
5. Unpredictable or unstable operation of Counter-Timer.	5. a) Frequency exceeding input range. Prescaler must be used for inputs to Model 90 probe above 10 MHz.
6. Disk Errors	6. a) Disk READ errors can occur due to clamping the diskette in an "off-center" position, causing the READ/WRITE head to be misaligned with the data track. Opening and closing the drive door will normally correct this situation. b) Use the back-up diskette.

SECTION 8: ADVANCED TRIGGERING MODES

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8.0 ADVANCED TRIGGERING MODES

The NPC-700's ability to detect subtle hardware faults or uncover deeply-nested software problems results from its powerful triggering modes.

The purpose of any triggering mode is to enable certain events of interest occurring in the system-under-test to be captured by the analyzer's data collection memory. Since an analyzer cannot have a memory of infinite depth, the more versatile the triggering modes, the better the chances that the events of interest will be captured. This is particularly important when you are working on an intermittent problem.

Often, there are a number of different, but equally valid ways of triggering the NPC-700. The information provided in this section is intended to give you general guidance in selecting proper triggering modes. As you gain experience with the analyzer, you'll find it easier to select the proper triggering mode for the task-at-hand.

8.1 STATE ANALYSIS TRIGGER MODES

The triggering capabilities of the NPC-700's state section allow you to create up to 16 levels of sequential trigger patterns which are useful for debugging nested software or microcode routines.

8.1.1 TRIGGER STACK

The 16 levels of triggering are accomplished through the use of a trigger stack set up through the state menu. The top or beginning of the stack is always level 0; the bottom is always level 15. The triggering sequence progresses from top to bottom, leaving a particular level only after all trigger word, qualifiers, and delay conditions are satisfied.

The current level of the stack is displayed on the CRT during data collection to inform the user of triggering progress.

In most applications, the stack sequence occurs so rapidly that this message may not be visible. However, if conditions for a particular level fail to be satisfied, the level at which the analyzer is "stuck" is displayed. A complex multi-level stack may be temporarily reduced to simplify triggering by selecting the END option at a particular level. When END is deselected, the stack will return to the pre-set, multi-level condition.

NOTE: The trigger stack can impose very restrictive conditions on triggering and data collections. The user should "build" the stack up from simpler, proven triggering conditions. If an expected event does not occur at a particular trigger level, set that level to $\overline{\text{TRIG}}$ (nonoccurrence triggering) to see what actually did take place.

8.1.2 DELAY

At each stack level (except level 0), a delay parameter can be specified. This delay parameter indicates the relationship of the current stack level with the previous level. (This is the reason that there is no delay at level 0.) The delay options include the following formats:

<u>OPTION</u>	<u>DESCRIPTION</u>
AFTER nnnn CLOCKS	The trigger word must occur after nnnn clocks from the previous level, where $0000 \leq nnnn \leq 9999$.
NOT ON nnnn CLOCKS	The trigger word must occur some time other than nnnn clocks from the previous level, where $0001 \leq nnnn \leq 9999$.
BEFORE nnnn CLOCKS	The trigger word must occur some time before nnnn clocks from the previous level, where $0002 \leq nnnn \leq 9999$.
ON nnnn CLOCKS	The trigger word must occur exactly on the nth clock following the previous level, where $0001 \leq nnnn \leq 9999$.
OCCURS nnnn TIMES	The trigger word must occur nnnn times before advancing to the next level, where $0001 \leq nnnn \leq 9999$.

A typical trigger stack is shown in Figure 8-1.

```

RESTART: 0003 XX XXXXXXXX -XXXXXX XX
TRIGGER:
0        0048 XX XXXXXXXX -XXXXXX XX
1 THEN  0042 XX XXXXXXXX -XXXXXX XX
2 THEN  0048 XX XXXXXXXX -XXXXXX XX
3 THEN  006E XX XXXXXXXX -XXXXXX XX
                                ON 0002 CLOCKS
                                AFTEP 0084 CLOCKS
                                OCCURS 0020 TIMES
  
```

**Figure 8-1. Typical setup of trigger stack.
(NPC-764 shown.)**

SECTION 8.0

ADVANCED TRIGGER MODES

8.1.3 RESTART

The restart capability augments the trigger stack of the NPC-700. This feature is useful since an attempt to trigger can often progress through a number of levels before "failing" or "missing" a match condition. The restart mechanism provides a way to reinitiate the triggering sequence. This is accomplished by allowing the user to specify a data pattern called the RESTART word. When this word is detected, it causes the stack to return to level 0 (the top of the stack). Note that the RESTART word has priority over all other triggering conditions. When the RESTART word is detected, the stack returns to level 0 and a search for a new level 0 trigger word begins 2 clock pulses following the RESTART word. (This 2-clock delay is necessary to initialize the stack.)

NOTE: The setting of the RESTART word to X's "don't care" is **not the same** as turning it off. A RESTART word of all X's will continually hold the stack at level 0, and triggering will never occur.

When tracing program flow, there can be several paths leading to the same point in the program. The RESTART feature of the NPC-700 gives you control over which path will actually be traced by the analyzer to get to the desired trigger point. Figure 8-2 illustrates this concept.

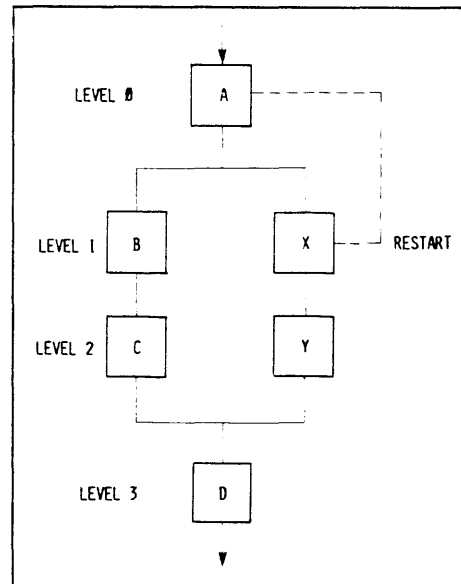


Figure 8-2. Illustration of the use of RESTART for branch analysis.

Suppose that to get to point D, the program in Figure 8-2 can follow either path A-B-C-D or path A-X-Y-D. If the trigger stack is set up to trace path A-B-C-D but path A-X-Y-D occurs, the analyzer will be "hung-up" at level 1 because event B never occurred. The restart feature is used to reset the stack back to level 0 whenever an event in the undesired path occurs. Thus, if X=RESTART, the occurrence of the undesired path (A-X-Y-D) will be detected and the trigger stack will automatically restart at level 0 as if the COLLECT key had been pressed. Then, when path A-B-C-D occurs, the analyzer will be ready and the triggering sequence will go to completion.

8.1.4 UNSPECIFIED RESTART

Even when a RESTART word is not specified, an automatic restart is initiated whenever the specified triggering conditions have become impossible to satisfy at a particular level. For example, if the DELAY mode: BEFORE nnnn CLOCKS cannot be satisfied because a trigger word has not occurred by the nth clock, the trigger stack will return to level 0.

8.2 TIMING ANALYSIS

As described in Section 7.4.1, the NPC-700's timing analyzer has two trigger word comparators, ARM and TRIG, and a number of triggering modes that define the relationship between these two words.

For simple, single-level triggering, the entire ARM word is set to X (don't care). For this case, a match between incoming data and the TRIG word is all that is required to trigger the analyzer.

However, when the capturing of more complex events requires the 2-level sequential triggering action of the ARM and TRIG words, the advanced modes described below can be used.

Note that data collection always begins relative to the occurrence of a TRIG word match; an ARM word match simply enables the analyzer to advance to the second triggering level.

8.2.1 TRIGGERING MODE 1: TRIG OCCURS nnnn CLOCKS AFTER FIRST ARM

Description:

1. The first match of the ARM word enables the analyzer.
2. The delay value nnn is counted down.
3. If the TRIG word is true, upon delay completion, the analyzer triggers; otherwise, LOCK OUT occurs and triggering is not possible.

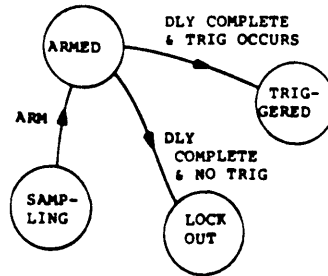
Options:

1. $\overline{\text{TRIG}}$ can be selected for TRIG.
2. $\overline{\text{ARM}}$ can be selected for ARM.

In the above options, any input pattern, **except the one selected**, would cause a match.

Typical Use:

Normally used with an external clock when searching for a particular 2-level sequence.



8.2.2 TRIGGERING MODE 2: TRIG OCCURS > nnnn CLOCKS AFTER FIRST ARM

Description:

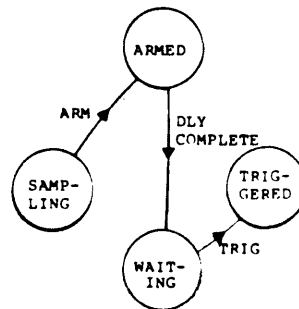
1. The first match of the ARM word enables the analyzer.
2. The delay value is counted down.
3. After countdown, the analyzer triggers on the first occurrence of a TRIG word match.

Options:

1. $\overline{\text{TRIG}}$ can be selected for TRIG.
2. $\overline{\text{ARM}}$ can be selected for ARM.

Typical Use:

ARM on a pattern but hold off triggering for a specific amount of time or clock samples. If ARM is used, it is possible to enable the analyzer when the system-under-test "leaves" a given pattern.



8.2.3 TRIGGERING MODE 3: TRIG OCCURS < nnnn CLOCKS AFTER FIRST ARM

Description:

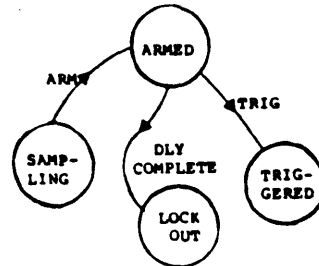
1. The first match of the ARM word enables the analyzer.
2. If a TRIG match occurs before the delay value is counted down, the analyzer will trigger.
3. Otherwise, the analyzer will LOCK OUT when the delay is complete and triggering will not be possible.

Options:

1. $\overline{\text{ARM}}$ can be selected for ARM.
2. $\overline{\text{TRIG}}$ can be selected for TRIG.

Typical Use:

1. Search for a specific pattern (TRIG) that occurs **within** a certain interval of time (or clocks) from another pattern (ARM).



**8.2.4 TRIGGERING MODE 4:
TRIG OCCURS > nnnn
CLOCKS AFTER LAST ARM**

Description:

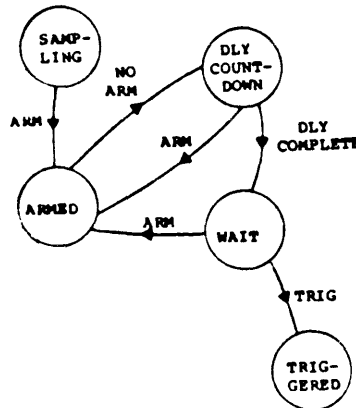
1. The first match of the ARM word enables the analyzer.
2. When the ARM word is no longer present, the delay value is counted down.
3. During this period, TRIG word matches are ignored, but an ARM word reoccurrence will restart the sequence.
4. If TRIG word occurs **after** an uninterrupted countdown, the analyzer triggers.

Options:

1. $\overline{\text{TRIG}}$ can be selected for TRIG.
2. $\overline{\text{ARM}}$ can be selected for ARM.

Typical Use:

After an ARM word has come and gone, hold off the search for a particular TRIG word until a certain time has passed (or clocks have occurred).



8.2.5 TRIGGERING MODE 5: TRIG OCCURS < nnnn CLOCKS AFTER LAST ARM

Description:

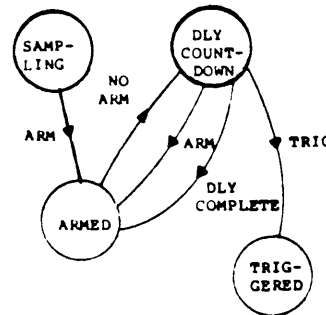
1. The first match of the ARM word enables the analyzer.
2. When the ARM word is no longer present, delay countdown is initiated.
3. If a TRIG match occurs before the delay is complete, the analyzer triggers.
4. If the delay completes or an ARM word reoccurs before a TRIG word is detected, the sequence restarts.

Options:

1. $\overline{\text{TRIG}}$ can be selected for TRIG.
2. ARM can be selected for ARM.

Typical Use:

Search for the occurrence of a TRIG word within a certain period of time (or clocks) after an ARM word has occurred and gone.



8.2.6 TRIGGERING MODE 6: TRIG OCCURS nnnn CLOCKS AFTER LAST ARM

Description:

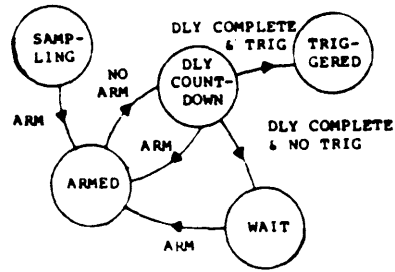
1. The first match of the ARM word enables the analyzer.
2. When the ARM word is no longer present, the delay countdown is initiated.
3. If the TRIG word is present at the end of the delay, the analyzer triggers.
4. If the TRIG word is not present at the end of the delay, wait for another ARM word to start sequence.

Options:

1. $\overline{\text{TRIG}}$ can be selected for TRIG.
2. ARM can be selected for ARM.

Typical Use:

Normally used with an external clock. Search for a specific pattern (TRIG), or the absence of a particular pattern (TRIG), at a fixed number of clocks after the ARM word has gone.



**8.2.7 TRIGGERING MODE 7:
TRIG OCCURS BEFORE
nnnn ARMS**

Description:

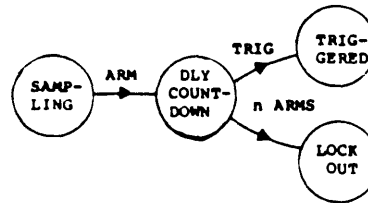
1. The delay count is initialized.
2. Each ARM word causes the delay to count down.
3. If a TRIG word occurs before the nth ARM, the analyzer triggers; otherwise, LOCK OUT occurs.

Options:

1. $\overline{\text{TRIG}}$ can be selected for TRIG.
2. $\overline{\text{ARM}}$ can be selected for ARM.

Typical Use:

Search for the occurrence of a TRIG word before a specified number of ARM words have occurred.



**8.2.8 TRIGGERING MODE 8:
TRIG OCCURS AFTER
nnnn ARMS**

Description:

1. The search for the TRIG word is held off until nnnn ARM words have been detected.

Options:

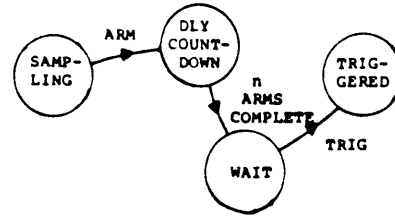
1. $\overline{\text{TRIG}}$ can be selected for TRIG.
2. $\overline{\text{ARM}}$ can be selected for ARM.

Typical Use:

Search for a TRIG word only after another ARM word has occurred a certain minimum number of times. This mode is primarily used with external (synchronous) clocking.

SECTION 8.0

ADVANCED TRIGGER MODES



8.2.9 TRIGGERING MODE 9: GLITCH IN ARM WHEN TRIG VALID

Description:

1. The channel designated by a "1" in the ARM word is examined for a glitch. The glitch is defined as a 0-1-0 or 1-0-1* transition over 3 consecutive clock sampling periods. (The channel being examined for a glitch should be in the latch input mode and the ARM filter must be off.)
2. If the TRIG word is present when the glitch is detected, the analyzer will trigger.

Options:

None

Typical Use:

This mode allows triggering on an unexpected glitch transition in a single channel. The mode can be expanded through the trigger linkage field.



NOTE: In the 8-channel glitch memory configuration, this triggering mode is not used.

*This means OCCURRENCE-NONOCURRENCE-OCCURRENCE, or NONOCURRENCE-OCCURRENCE-NONOCURRENCE of the pattern specified in the ARM word.

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SECTION 9.0

GENERAL-PURPOSE COMPUTER

9.0 GENERAL-PURPOSE COMPUTER

As described in the introduction, the NPC-764 is not only a very capable logic analysis system, it is also a general-purpose, desk-top microcomputer. Since the logic analyzer has been thoroughly described in previous sections of this manual, this section, as well as Sections 10.0 and 11.0, will deal only with the microcomputer aspects of the NPC-764.

All microcomputers are comprised of a hardware system and a software system. Unless used for a single, specific task, the software system is called an "operating system." The purpose of an operating system is to provide the interface between the hardware and the user.

9.1 HARDWARE

DISPLAY

There are three display techniques available to the user. The integral display is a 9-inch CRT with 25 lines of 80 character positions each. There is a BNC connector on the back panel which permits the information on the CRT to also be displayed on an external video monitor or printer. The RS-232C interface provides a means of transmitting information to an external terminal or printer for display. See Section 12.0 for details on these output ports.

KEYBOARD

The keyboard is a full ASCII keyboard, which will be familiar to most users. There are 7 special function keys at the top of the keyboard, plus a red **RESET** key. The **RESET** key calls the Logic Analyzer Operating System and must be held down for approximately 2 seconds to accomplish this function. This time delay is provided to prevent an accidental reset at an inopportune time. The other 6 special keys are predefined when operating the NPC-764 as a logic analyzer; or can be user-defined in the microcomputer mode.

MEMORY SUBSYSTEM

There are 48K bytes of RAM available to the user. Since the NPC-764's 8085 microprocessor cannot directly address this 48K of RAM plus the 40K of analyzer ROM, the memories are "bank switched," enabling only one memory bank at a time.

DISK DRIVE

The integral flexible disk drive is 5 $\frac{1}{4}$ ", single-sided, double-density, soft-sectored, 100 tracks per inch, 77 tracks, with 300K bytes of formatted capacity. Refer to Section 2.3.8.5 for the diskette specification. There is a connector provided to expand the disk memory to approximately 1M bytes, unformatted, by using an external dual-drive expansion chassis (Micropolis or equivalent). The RS-232C interface can also be used to extend the disk memory using a serial driven disk subsystem.

I/O

The RS-232C interface provides a "standard" interface to serial devices. This bidirectional interface is described in Section 12.0.

The NPC-764 also incorporates an intelligent controller for the IEEE-488 interface bus. The commands that permit the execution of user programs to control an IEEE-488 bus-based system are described in Section 13.0.

9.2 SOFTWARE

As stated previously, an "operating system" is a program designed to provide an interface between the user and the hardware. The NPC-764 actually has 2 operating systems, the logic analyzer operating system which is in ROM, and CP/M which is loaded from the disk into RAM. CP/M is a trademark of Digital Research, which created the "Control Program/Monitor."

The ROM-based operating system for the logic analyzer should require little explanation because the functions of this system are fixed and dedicated to the task of controlling the logic analyzer hardware.

On the other hand, the user interface to the microcomputer cannot be defined specifically because of the great diversity of application software available to be purchased or created by the user. Therefore, a description of CP/M is included in Section 10.0.

CP/M

CP/M is probably the single most commonly used operating system in the microcomputer world for the 8080, 8085, and the Z80 microprocessors. There are many reasonably priced programs available on the market that perform a wide variety of applications from word processing to scientific analysis of data.

Through CP/M, the user can also create his or her own programs. These programs can be machine-code-generated via assembly language by a resident assembler, or it can be generated using a high-level-language such as BASIC or FORTRAN. CP/M can also be used to set up and control the analyzer and then post-process the analyzer data. See Section 11.12 for an example of using CP/M to automate analyzer tests, including operator prompts.

9.2.1 OPTIONAL PRINTER PROGRAM

A printer driver program that enables the NPC-764 to generate text and graphics hardcopy using an Epson MX-80A printer is available. The printer must be equipped with "Grafrax" and a serial 2K buffer interface card. The driver software is provided on diskette and contains the following 3 files:

MX.80PRNT.COM	(The program itself)
MX.80PRNT.DOC	(Documentation concerning operation)
COPY1.COM	(Single file copy routine for 1-drive systems)

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SECTION 10.0

CP/M OPERATING SYSTEM

10.0 CP/M OPERATING SYSTEM

This Operator's Manual for the NPC-764 is intended to **guide** the user in the application of CP/M on the NPC-764, not to provide a tutorial, nor to make the user proficient in its use. This section provides an overview of CP/M, and Section 11.0 provides simple, basic examples of some of CP/M's features and commands. For more detailed knowledge of CP/M and its applications and/or modifications, refer to the CP/M Documentation Manual provided with the NPC-764.

The CP/M operating system is literally a system of interrelated programs. Rather than load all of CP/M into memory at once and unnecessarily consume RAM memory space, the hardware memory is partitioned such that one section will contain the core of the operating system (hereafter referred to simply as "the system"), while the remaining programs will reside in an area of memory designated as "transient program area." These transient programs will be loaded into the shared memory only when needed.

There are 2 kinds of commands available in CP/M: built-in and transient. Built-in commands are five of the most commonly used commands which are part of the core of the CP/M system and do not appear on the directory of the disk. Transient commands are so named because they are actually programs that generally appear in the disk directory. When called, they are loaded into the transient program area (TPA) of RAM. Each transient program has its own set of commands which can be executed after loading into RAM is complete.

10.1 BUILT-IN COMMANDS

DIR

DIR is the command used to display the directory of the disk.*

TYPE

TYPE is the command used to simply examine a disk file by displaying the file on the CRT, exactly as it is stored on the disk.

SAVE

SAVE is used to save a file onto the disk.

REN

REN is used to rename an existing file on the disk. It will not create a new copy of the old file, merely assign a new name to it.

ERA

ERA will erase an unwanted file from the disk.

10.2 TRANSIENT COMMANDS

SYSGEN

SYSGEN is a program that will not appear in the disk directory. It is used to generate a new system disk, to be used as a backup copy. Due to copyright restrictions, CP/M may not be copied.

***NOTE:** The file labeled: **READ ME** describes the other files on the diskette. To access this file, type:

TYPE READ.ME

Then press **CNTL S** to stop scrolling; and any key to start.

- STAT** STAT is a program which will display the remaining memory space on the disk or the size of a specific file.
- ED** ED and its associated commands perform a simple text editor function. It is not a word processor, but a tool to use in the creation and editing of files. These files can be simple text or high-level programs to be compiled later.
- PIP** PIP is a file handling and manipulation program. It is used to copy files, transmit and receive data on the RS-232C interface, and assign physical devices to logical device names used in PIP for file handling.
- SUBMIT** SUBMIT is a program used to specify a series of CP/M commands to be executed sequentially. This series can be stored as a file, then called any time the user wishes to perform that series of commands--without having to type them from the keyboard each time.
- XSUB** XSUB is an extended submit program which allows a series of commands to be linked into a file; and which also will stop and permit the user to insert variable information into specific elements of the command list.
- ASM** ASM is an assembler program for the 8080/8085. It allows the user to create 8080/8085 code using assembly language. This 8080/8085 code thus generated may be used in the NPC-764 or it can be transmitted, using PIP, to an external device such as a PROM programmer. There are similar programs for other microprocessors available from software suppliers such as Lifeboat Associates.*
- DDT** DDT is used to debug programs created with ASM. It will test the program, as well as permit editing.
- SAVE** SAVE is used to transfer the transient program area of RAM memory to the disk. Normally this program would be used to save the programs generated by ASM.
- LOAD** LOAD is used to convert a program from a ".HEX" file type created by ASM into an executable ".COM" file. As the conversion takes place, the program is loaded into executable memory space.
- DUMP** DUMP is used to display a file from the disk in HEX form, rather than ASCII.

10.3 NPC TRANSIENT COMMANDS

- FORMAT5** FORMAT5 is a program used to prepare a new diskette for use, or to erase an old diskette and prepare it for reuse.

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SECTION 10.0

CP/M OPERATING SYSTEM

COPY5

COPY5 is a program which allows the duplication of a diskette. Since PIP requires an external drive, COPY5 was designed to copy a diskette using only the single drive in the NPC-764. It repetitively transfers a portion of the source diskette into RAM memory, prompts the user to install the target diskette, then transfers the information from RAM to the target diskette.

LASAVE

LASAVE is a program which stores all analyzer set-ups and auxiliary memory data on disk.

LARECALL

LARECALL is a program which recalls all analyzer set-ups and auxiliary memory data which was previously stored on disk using LASAVE.

10.4 USE OF LASAVE AND LARECALL FROM A CBASIC PROGRAM

A file is provided on floppy disk (named LADISC.BAS) which provides the function definitions necessary to save or recall analyzer set-ups and data while executing a CBASIC program. This is useful in automated testing for recalling canned set-ups or "known-good" data and to save results for later analysis.

To make use of these functions it is necessary to compile a CBASIC test program with LADISC.BAS included prior to the first program access. This can be done with the CP/M editor or at compile time by using the following CBASIC statement:

```
%INCLUDE LADISC
```

To execute LASAVE, use the statement format:

```
RC% = FN.LASAVE% (<filename$>)
```

To execute LARECALL, use the statement format:

```
RC% = FN.LARECALL% (<filename $>)
```

<filename \$> is any valid CP/M file name.

RC% will contain a return code, as follows:

```
0 = normal execution  
1 = disc full (save only)  
2 = no such filename (recall only)  
3 = invalid filename
```


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SECTION 11.0

CP/M EXAMPLES

11.0 CP/M EXAMPLES

This section of the operating manual describes the steps needed to perform some of the more commonly-used commands that are available to the user. Although you will not receive an in-depth knowledge of CP/M and its facilities, the examples that follow will show you how to perform basic text file creation, limited file manipulation, 8080/8085 code generation and debug, and how to get a hardcopy of your files. You'll also be able to exercise control over the execution of logic analyzer tests saved on disk.

11.1 POWER ON

If the power is already on, it is not necessary to turn the power off and back on. Insert the CP/M diskette in accordance with Section 2.3.8, call the CONFIGURATION LIST, and press the ESC (ESCAPE) key. If the power is off, turn it on at the rear of the right side of the unit **BEFORE INSERTING THE DISKETTE**.

11.2 HEADER

The system will respond with a header identifying the current version of the CP/M operating system. The system will also display a prompt to signify that it is ready for operator input:

A>

11.3 DIR

DIR is used to display the disk directory. Simply type DIR and press RETURN:

A>DIR (RETURN)

The CRT should now display the contents of the disk:

```
A>DIR
A: CPM          COM : PIP          COM : XSUB          COM : ED          COM
A: ASM          COM : DDT          COM : LOAD          COM : STAT          COM
A: DUMP         COM : SUBMIT       COM : PRINT         COM : DSKSTEST     COM
A: FORMATS     COM : LSAVE        COM : LARECALL      COM : RAMTEST      COM
A: KYEDTEST    COM : COPYE        COM : LADISA        COM : LAPRINT      COM
A: BIOS764     ASM : PROM764      ASM : CRUN2        COM : CRUN238     COM
A: CBAS2       COM : XREF          COM : D486          : D8888          : D8888
A: D8885       : D8885            : DZ88             : D6888          :
A: D6889E     : D6889E           : GPIB             BAS : LADISC         BAS
A: LA         COM : RS232EX      INT : RS232EX     $$$ : RS232EX        002
A: RS232EX    001 : GPIBEX        INT : GPIBEX      BAS : RS232EX        BAS
```

(Sample Only -- Your Directory Will Probably Differ)

The A identifies the disk drive in use. If the dual-disk expansion capabilities are used, a B or C is displayed.

11.4 STAT

STAT is a transient command used primarily to determine how much DISK MEMORY is remaining, or the size of a particular file. Type:

STAT (RETURN)

The above command will display the remaining disk memory.

```
A>STAT
A: R/W, Space: 62k
```

Next, type:

STAT RAMTEST.COM \$\$ (RETURN)

```
A>STAT RAMTEST.COM$S
  Reqs  Bytes  Ext Acc
    7      2k   1 R/W A:RAMTEST.COM
Bytes Remaining On A: 164k
```

This command will display the size of any file using the format: STAT FILENAME.EXT \$\$S. Select another file from your directory and try this command again.

NOTE: You must enter all commands **exactly** as shown with all spaces and characters specified; otherwise the NPC-764 will respond with a **File Not Found** or other error message.

11.5 ED

ED is a simple implementation of a text editor, used for the creation of files. These files can be text, or they can be a high-level-language program that will later be compiled.

ED has its own set of commands that will only operate after **ED** has been executed. Those commands allow you to create the text, edit it, store it on disk, and retrieve it from disk.

For this example, only a small portion of those commands will be used. Therefore, it is **IMPERATIVE THAT YOU FOLLOW THIS EXAMPLE PRECISELY**. Otherwise, you may get into a situation in which this example will not help you recover.

- NOTES:**
1. If you get into trouble, press **RESET** and **ESC** and start again.
 2. Be certain that the **CAPS LOCK** key is locked in the down position.
-

Type:

ED TESTFILE.TXT (RETURN)

If this file does not already exist, **ED** will return with a prompt:

NEW FILE
:*

11.5.1 INSERT

Next, we must prepare to **INSERT** text into our file, using the **I** command. Type:

I (RETURN)

ED is now ready to accept text into line 1:

1:

Begin typing the following text, ending each line with the **RETURN** key. (It is suggested that each line be no more than 80 characters to maintain readability.) **ED** will provide a new line number each time you press **RETURN**.

- 1: **THE NPC-764 REPRESENTS A NEW TREND IN THE TEST AND MEASUREMENT INDUSTRY.**
- 2: **THE INTERNAL COMPUTING POWER OF THE MICROPROCESSOR IS NOW AVAILABLE TO THE USER.**
- 3: **TASKS SUCH AS AUTOMATIC TESTING, POST-PROCESSING, AND TEST FUNCTION EXPANSION ARE EASILY IMPLEMENTED.**

To end the text insertion mode, simply press **CTRL** and **Z** simultaneously. Then press **RETURN**.

To end this session with **ED**,

Type:

E (RETURN)

The system will now store this text file on the disk. When it returns with the system prompt, **A>**, you may use **DIR** to see your new file in the directory. Notice that the system also creates a backup file, **TESTFILE.BAK**. You can use **STAT** to examine the file size if desired.

11.6 TYPE

TYPE is a built-in command used for quick and easy examination of file contents. When executed, it will display the file exactly as it is stored on the disk.

Type:

TYPE TESTFILE.TXT (RETURN)

If you are examining a large file, you may want to stop the text before it scrolls off the **CRT**. Simultaneously press **CTRL** and **S** to stop scrolling; press any key to continue scrolling.

11.7 REN

REN will rename an existing file. It will not duplicate the file under a new name, merely change the old name to the new one:

Type:

REN NEWNAME.DOC=TESTFILE.TXT (RETURN)

S=LASAVE
R=LARECALL

As a practical example of **REN**, execute the following commands:

REN S.COM=LASAVE.COM
REN R.COM=LARECALL.COM

Therefore, when using the disk to save and recall logic analyzer tests, the **REN** command allows you to reduce your typing by replacing **LASAVE** with **S** and **LARECALL** with **R**.

DIR will allow you to verify that each file name has been changed.

11.8 ERA

ERA will erase the specified file, **FOREVER**. Be certain that you specify the correct file. There is no way to recover erased files.

Type:

ERA NEWNAME.DOC (RETURN)
ERA TESTFILE.BAK (RETURN)

11.9 FORMAT5

FORMAT5 is a special transient command supplied by Nicolet Paratronics. Since **SYSGEN** is not supplied with this system, **FORMAT5** is used to format a new diskette (or reformat a used one) in preparation for use.*

Type:

FORMAT5 (RETURN)

```
A>FORMAT5
INITIALIZATION PROGRAM FOR ALADDIN 5.25"
VERSION 2.0

FORMAT ON DRIVE A,B,C, OR D? A
WRITE ENABLED BLANK DISK READY TO FORMAT? (Y,N)
```

If desired, insert a "Write Enabled" blank diskette.

Type:

Y (RETURN)

The disk drive will turn on and begin formatting the diskette.

11.10 COPY5

COPY5 is another special transient command supplied by Nicolet Paratronics, which will copy an entire diskette, using the single built-in drive. The program prompts the operator to remove the source diskette and install the target diskette at the appropriate times.

***NOTE:** **FORMAT5** will erase **all** programs listed in the directory on your diskette.

To execute this command and create a copy of a diskette,

Type:

COPY5 (RETURN)

```
A>COPY5
COPYRIGHT (C) 1982, NICOLET-PARATRONICS CORP.

DISK COPY UTILITY, V1.0
COPY5 WILL COPY THE SYSTEM OR AN ENTIRE DISK
FROM A SOURCE DISKETTE TO A TARGET DISKETTE.
THE COPY REQUIRES ONLY A SINGLE DISK DRIVE, BUT
WILL USE MULTIPLE DRIVES IF AVAILABLE.

COPY (X=EXIT, S=SYSTEM, ELSE ALL)?
SOURCE DRIVE (A, B, C OR D) ? A
TARGET DRIVE (A, B, C OR D) ? A
READY SOURCE DISKETTE ON DRIVE A (RETURN)
READY TARGET DISKETTE ON DRIVE A (RETURN)
```

Simply answer the questions asked by the program, and switch the diskettes when instructed to do so.

11.11 ASM

ASM is the transient command which provides the ability to write an assembly language program for the 8080 or 8085. The following example illustrates the mechanics of writing a simple assembly language program using **ED**, assembling the program using **ASM**, converting the program to an executable file using **LOAD**, and finally, executing the program. For detailed explanation of this procedure, refer to the CP/M Software Documentation Manual.

The first step in writing a program is to define the task to be performed. This example will simply display a message on the NPC-764 CRT. The next step is to create a file, using **ED**, with **MSSGDISP** as the main file name and **.ASM** as the file name extender. A sample file is shown in Figure 11-1.

```
*****
;*****
;THIS IS A TEST PROGRAM TO ILLUSTRATE THE ASSEMBLER.
;*****
ORG 100H
RDBTEST: LXI B,DSTART ;LD START ADRS

LXI H,0F100H ;LD OUTPUT ADRS

START: LDAX B ;LD DATA TO ACCUM.
CPI '$' ;IS DATA BYTE END OF STRING ?
JZ EXIT ;YES JUMP TO END & EXIT PROG.
MOV M,A ;MOV DATA BYTE TO RAM MEMORY.
INX H ;INC DATA ADRS.
INX B ;INC OUTPUT ADRS.
JMP START ;GO BACK & LD NEXT DATA BYTE.
EXIT: RET ;FINISH.
DSTART: DB 'THIS IS AN EXAMPLE OF THE ASSEMBLER $'
END

A>█
```

Figure 11-1. Sample source file created by ED.

.PRN FILE

After the program is written and stored on the diskette, it must be assembled. Typing **ASM MSSGDISP** will cause the transient program **ASM** to be loaded. **ASM** will then load **MSSGDISP.ASM** and create two new files, **MSSGDISP.PRN** and **MSSGDISP.HEX**. The **.PRN** file is the one to be used when printing the source file. See Figure 11-2.

```

*****
*                                     *
* THIS IS A TEST PROGRAM TO ILLUSTRATE THE ASSEMBLER.                       *
*                                     *
*****
*
0100          ORG      100H
0100 011301  RDBTEST: LXI    B,DSTART      ;LD START ADRS
0103 2100F1          LXI    H,0F100H      ;LD OUTPUT ADRS
0106 0A          START: LDAX   B          ;LD DATA TO ACCUM.
0107 FE24          CPI     '0'          ;IS DATA BYTE END OF STRING ?
0109 CA1201          JZ     EXIT        ;YES JUMP TO END & EXIT PROG.
010C 77          MOV     M,A          ;MOV DATA BYTE TO RAM MEMORY.
010E 23          INX    H            ;INC DATA ADPS.
010F 03          INX    B            ;INC OUTPUT ADRE.
010F C30601          JMP     START      ;GO BACK & LD NEXT DATA BYTE.
0112 C9          EXIT:  RET          ;FINISH.
0113 644849E320DSTART: DB    'THIS IS AN EXAMPLE OF THE ASSEMBLER' ;'
013E          END

A>

```

Figure 11-2. Sample .PRN file created by ASM.

.HEX FILE

The **.HEX** file shown in Figure 11-3 will be used to create the executable file by using the transient program **LOAD**. Typing **LOAD MSSGDISP** will then load **MSSGDISP.HEX** and create the file **MSSGDISP.COM**.

```

A>TYPE MSSGDISP.HEX
:100100000113012100F10AFE24CA1201772303C35F
:100110000601C9544849E320495320414E204558AF
:10012000414D504C45204F462054484520415353A3
:0E013000454D424C4552202020202020202020406
:0000000000

A>

```

Figure 11-3. Sample .HEX file created by ASM

We now have the file **MSSGDISP.COM** available to be executed.

Type:

MSSGDISP (RETURN)

EXECUTE

The NPC-764 will now display the message "THIS IS AN EXAMPLE OF THE ASSEMBLER" near the top of the CRT.

Using **ED** and the steps illustrated above, you can change the original file **MSSGDISP.ASM**, or create your own new program.

11.12 SUBMIT

The **SUBMIT** utility is a program which allows the user to automatically--and sequentially--execute a series of CP/M common files.

To use this feature of CP/M, you simply create a file, using **ED**, that contains a sequential list of the CP/M common files to be executed. Then type:

A> SUBMIT FILENAME

CP/M will load **SUBMIT** which in turn causes all the lines from **FILENAME** to be sequentially read and executed. When finished, the prompt **A>** appears, indicating that the NPC-764 is ready for the next command from the keyboard.

EXECUTING CP/M COMMANDS

The following example demonstrates how to use **SUBMIT** to automatically execute several of the CP/M commands discussed previously. In this example, the filename will be **DEMOFILE**. Simply follow the listing in Figure 11-4. (Remember to type **CTRL Z** at line 7 to terminate command entry.)*

```
A>ED DEMOFILE.SUB
NEW FILE
: *I
1: DIR
2: ERA *.BAK
3: STAT *.COM $S
4: DIR
5: ;
6: ;THIS COMPLETES DEMOFILE.
7:
: *E
A>
```

Figure 11-4. Example of **SUBMIT** utility.

To execute, type:

A>SUBMIT DEMOFILE (RETURN)

At this point, CP/M will load the **SUBMIT** utility and sequentially execute the commands and text in **DEMOFILE** as follows:

1. **DIR** Display the directory of the diskette, including back-up files (if any).
2. **ERA *.BAK** Erase all backup files.

***NOTE:** If necessary, see the CP/M Software Documentation Manual for the editing procedures required to correct program entry errors.

3. **STAT *.COM\$\$** ... Display the statistics of all .COM files.
4. **DIR** Display the updated directory (without back-up files.).
5. **;** (Blank line for spacing.)
6. **;**THIS COMPLETES**** (Comment.)
DEMOFILE

EXECUTING ANALYZER TESTS

One of the most powerful advantages of combining logic analysis with CP/M is the simplicity in which multiple tests--including user prompts--can be automated. In the following example, three separate analyzer tests and corresponding test instructions are created, stored, and executed using **SUBMIT**.

STATE TEST

1. Press **RESET** to access the analyzer operating system. Call the 48 CHANNEL STATE menu and enter **0040** as the trigger word. (Leave all other menu parameters unchanged.)
2. Connect the **A** state probe to the **A** side of the Logic Analyzer Test Card supplied with the NPC-764. (See Section 6.1 for a description of the test card.) The state probe switches should be set to **TTL** and **TRUE**.
3. Press **COLLECT** to take and display a data collection.
4. Press the **CONFIG** followed by the **ESC** key to call the CP/M operating system. When the **A >** prompt appears, type:

LASAVE STATE (RETURN)

to save the first test under the arbitrary file name: **STATE.*** When the test is saved, the **CONFIGURATION LIST** will automatically appear.

TIMING TEST

1. Call the 16 CHANNEL TIMING menu. Enter in a sample clock of **100 μ S** and a trigger word of **XXXXXXXX 00000000**. (X=don't care.) Also set **PRETRIG** to **00%**.
2. Connect the **B** timing probe to the **B** side of the test card. Then press **COLLECT** to take and display a data collection. Use **X20** magnification.
3. Call the **CONFIGURATION LIST** and press **ESC** as before.

Type:

LASAVE TIMING (RETURN)

to save the second test under the arbitrary file name: **TIMING.**

***NOTE:** If you've renamed **LASAVE** as **S**, type **S STATE (RETURN)** to save data.

**WAVEFORM TEST
(OPTIONAL WAVEFORM
BOARD MUST BE
INSTALLED)***

1. Call the **WAVEFORM RECORDER** menu. Set the **ATTENUATOR** to 1V/DIV and the **OFFSET** to +0.30. (See Figure 6-17, if necessary.)
2. Press the **S2** key to access the display mode so you can press the **C** key to call the clock field in the timing menu. Set this clock to 1 μ S. Step down to the trigger **LINKAGE** field and select **W** for single-shot operation.
3. Connect the Model 90 probe to the **WAVEFORM BNC** at the rear of the NPC-764. (Make sure it is not connected to the **CTSA BNC**.) With **X10** selected, place the probe tip at the **WF** test point on the test card and press **COLLECT**. (It is not necessary to connect the probe ground wire.) Select **X1** magnification when the waveform is displayed.
4. Call the **CONFIGURATION LIST** and press **ESC** as before.

Type:

LASAVE WAVE (RETURN)

to save the third test under the arbitrary file name: **WAVE**.

DIRECTORY

Press **ESC** and type **DIR (RETURN)** to verify that you have **STATE**, **TIMING**, and **WAVE** files on the diskette.

OPERATOR PROMPTS

Using the **ED** utility, you can create a message that will prompt the user for each test. However, in order to keep the message on the screen until the user is ready to continue, a **PAUSE** program is required.

AUTOMATIC TESTING

The **SUBMIT** program for controlling the logic analyzer will be called **AUTOTEST**. To incorporate prompting messages prior to each test, follow the procedure described below:

PAUSE

The **PAUSE** program in Figure 11-5 is written in assembly language.

```

A>ED PAUSE.ASM
NEW FILE
: *I
1:          ORG     100H
2:          MUI     C,1
3:          CALL   5
4:          RET
5:
: *E
A>ASM PAUSE.AAX

```

Figure 11.5 **PAUSE** program.

***NOTE:** If your NPC-764 does not have this option, continue with the procedure and ignore all references to waveform.

When typing the program in Figure 11-5, press the **TAB** key to achieve the spacing shown. Also, don't forget to type **CTRL Z** at line 5 to exit program entry. The command **ASM PAUSE.AAX** initiates program assembly.

After program assembly,

type:

A> LOAD PAUSE

Check the directory to verify your **PAUSE** program.

AUTOTEST

The program in Figure 11-6 combines analyzer tests, prompting messages, and the **PAUSE** program.*

```

A)ED AUTOTEST.SUB
NEW FILE
: *I
1: |
2: | TO THE OPERATOR: YOU'RE GOING TO PERFORM 3 TESTS.
3: | IT'S IMPORTANT THAT YOU FOLLOW THE INSTRUCTIONS CAREFULLY.
4: |
5: | STATE TEST: AFTER READING THE INSTRUCTIONS BELOW, PRESS RETURN
6: | WHEN THE CURSOR FLASHES. THIS WILL CALL THE STATE TEST.
7: |
8: | A. CONNECT THE A STATE PROBE TO THE A SIDE OF THE TEST CARD.
9: | B. WHEN THE CONFIGURATION LIST APPEARS, PRESS THE COLLECT KEY.
10: | C. AFTER THE TEST IS COMPLETE, PRESS THE CONFIG KEY FOLLOWED BY THE
11: | ESC KEY TO RECEIVE INSTRUCTIONS FOR THE NEXT TEST.
12: |
13: | REMEMBER, PRESS RETURN WHEN THE CURSOR FLASHES.
14: PAUSE
15: LARECALL STATE
16: |
17: | TIMING TEST
18: |
19: | A. CONNECT THE B TIMING PROBE TO THE B SIDE OF THE TEST CARD.
20: | B. WHEN THE CONFIGURATION LIST APPEARS, PRESS THE COLLECT KEY.
21: | C. AFTER THE TEST IS COMPLETE, PRESS THE CONFIG KEY FOLLOWED BY THE
22: | ESC KEY TO RECEIVE INSTRUCTIONS FOR THE NEXT TEST.
23: |
24: PAUSE
25: LARECALL TIMING
26: |
27: | WAVEFORM TEST (OPTIONAL)
28: |
29: | A. CONNECT THE SCOPE PROBE TO THE WF TESTPOINT ON THE TEST CARD.
30: | B. AFTER THE CONFIGURATION LIST APPEARS, PRESS THE COLLECT KEY.
31: | C. THIS COMPLETES THE TEST SERIES.
32: PAUSE
33: LARECALL WAVE
34: |
: *E

```

Figure 11-6. AUTOTEST program.

***NOTE:** If necessary, see the CP/M Software Documentation Manual for the editing procedures required to correct program entry errors.

SECTION 11.0

CP/M EXAMPLES

Don't forget **CTRL Z** on line 34. Also, replace **LARECALL** by **R** if you've previously renamed this command.

After entering this program, you can execute it by typing:

SUBMIT AUTOTEST (RET)

and following the instructions. Note how the NPC-764 executes each line exactly as it was originally typed in. The user is encouraged to use this simple example as a model for more comprehensive automatic tests.

NOTE: If automatic tests **without** operator intervention are required, the GPIB controller capability of the NPC-764 can be used. See Section 13.0.

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12.0 INPUT/OUTPUT INTERFACE PORTS

12.1 PROBE CONNECTIONS

The primary inputs to the logic analysis functions of the NPC-700 are the probe connectors located on the left side of the instrument. See Figure 12-1. These ports are bidirectional, allowing the user to not only acquire data to be saved in the high-speed RAM of the analyzer, but also to output stimulus or data to his system under test via a user-supplied interface. (The probes themselves are not bidirectional.)

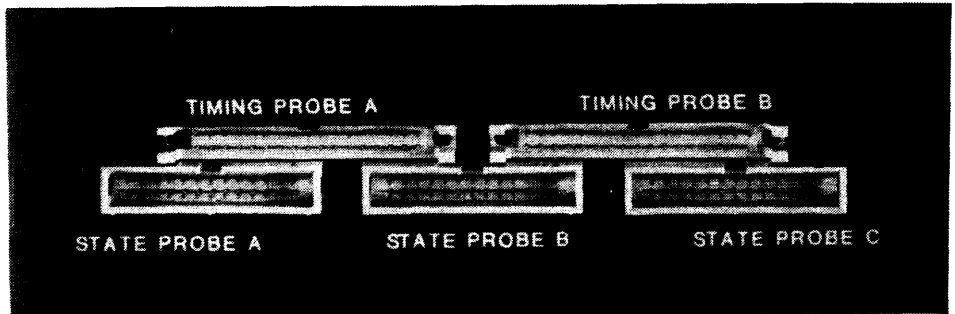


Figure 12-1. Probe connections. (NPC-764 shown. The B probe is not used on the NPC-748.)

12.2 EXTERNAL VIDEO OUT

This rear-panel BNC connector, shown in Figure 12-2, allows the NPC-700 user to display video information from the CRT on an external monitor. It can also be used to drive a video printer for hard copy documentation of menus and associated data. The output of this connector is standard composite video and its impedance is 75 ohms.

NOTE: The NPC-700 uses halflight reverse video in some menu fields. Some video printers cannot reproduce these fields. In order to use these printers, you must short out the 680-ohm voltage divider (R5) on the top left portion of the Processor Board (just below the video connector). Use a shorting wire with miniature ball clips on both ends, or install a SPST switch. Remove the short when printing displayed data.

12.3 RS-232C SERIAL* INTERFACE PORT (NPC-764 ONLY)

As shown in Figure 12-2, the NPC-764 uses a standard EIA 25-Pin connector to provide a bidirectional interface to RS-232C compatible devices such as printers, PROM programmers, emulators, etc. The interface connection and internal switch settings are described below.

NOTE: An optional RS-232C software package for outputting text and graphics to an Epson (or equivalent) printer is available. Contact your local NPC sales office or the factory for details.

*The NPC-748 does not include serial I/O.

12.3.1 INTERFACE CONNECTIONS

The connection utilizes standard EIA levels of ± 12 V amplitude (positive true logic) and are described in the following list. Unlisted pin numbers are not used by the NPC-764.

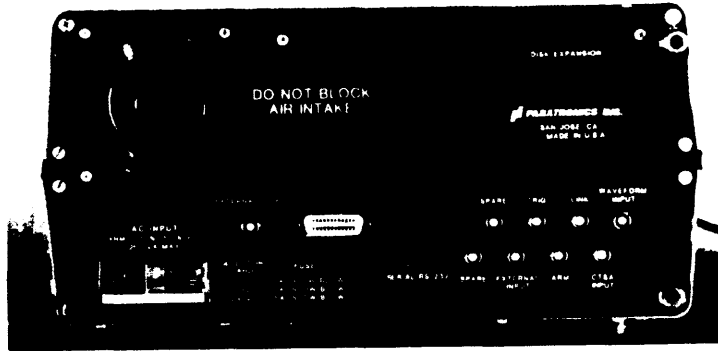


Figure 12-2. NPC-764 Rear Panel connectors.

**RS-232C
PIN DEFINITIONS**

- PIN 1 **Chassis and logic Ground.**
- PIN 2 **Serial In.** (Note: The Disk/RAM Controller (DRC) board can be "strapped" to configure this pin as **Serial Out.**)
- PIN 3 **Serial Out.** (Note: The Disk/RAM Controller (DRC) board can be "strapped" to configure this pin as **Serial In.**)
- PIN 4 **Return to Send (RTS).** Programmable. Upon power-on reset, RTS is normally "ON."
- PIN 5 **Clear to Send (CTS).** If data is transmitted to the NPC-764, this pin must be pulled up so that if disconnected, it is normally high (ON).
- PIN 6 **Data Set Ready (DSR).** Status bit DSR is readable, if desired, and is pulled up so it is normally high (ON).
- PIN 7 **Logic Ground.**
- PIN 8 **Data Carrier Detect (DCD).** Status bit DCD is readable, if desired, and is pulled up so it is normally high (ON).
- PIN 20 **Data Terminal Ready (DTR).** Programmable DTR is driven by software and is normally (ON).

All other pins are disconnected. "Pulled high" means the pin is tied to +15V through a resistor.

12.3.2 INTERFACE CONFIGURATION

The RS-232C interface is implemented using a Rockwell (Synertek) 6551A chip. This chip is user-programmable to suit desired interface conditions.

The NPC-764 has been designed to interface to other RS-232C compatible equipment. Reference to the 6551A chip manufacturer's data manual (Rockwell/Synertek) is recommended.

CONTROL REGISTER COMMAND REGISTER

The control register selects the mode of the chip with regard to word length, number of stop bits and clock controls. The command register is used to control specific transmit/receive functions. These are programmed automatically when power is initially applied, and are set up in accordance to the dip switch located on the Processor Board in the card cage inside the NPC-764 as shown in Figure 12-3. See Figure 12-4 for dip switch settings.

NOTE: The default condition for **CHARACTER LENGTH** is 8 bits with 1 **STOP** bit. Parity is disabled.

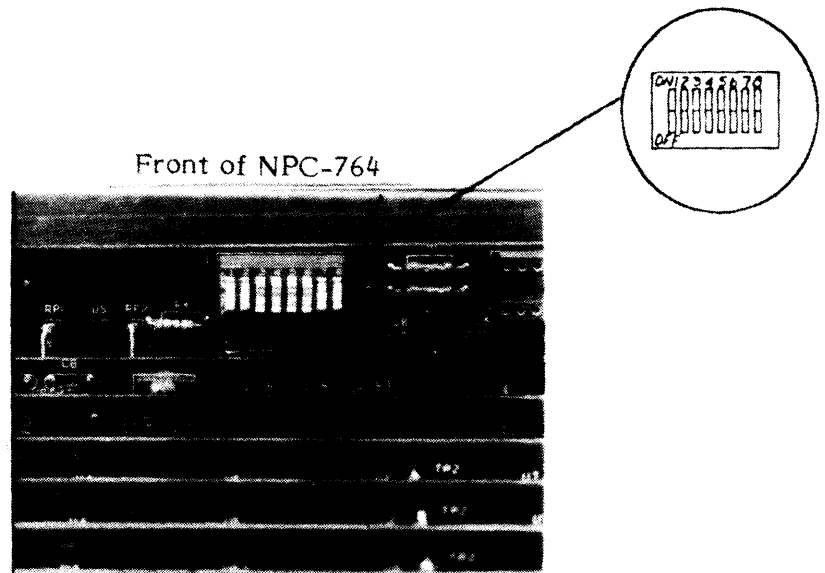


Figure 12-3. Dip Switch location on Processor Board.

RS-232C SET-UP

The RS-232C interface is set up using the I/O Configuration Menu. See Section 5.10.

12.4 SWITCH SETTINGS

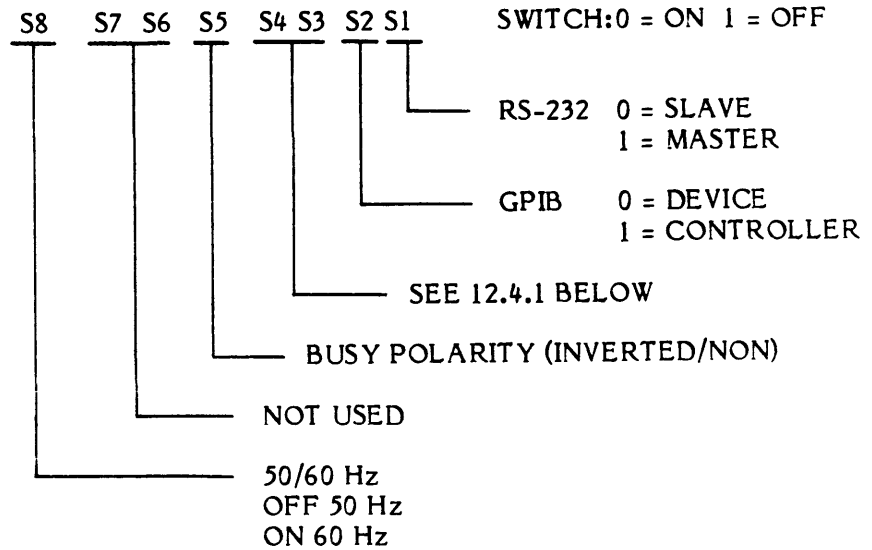


Figure 12-4. Processor Board DIP Switch Settings (NPC-764).

12.4.1 DEFAULT BAUD RATE

The DIP switch settings for the power-on default baud rate are as follows:

S4	S3	BAUD RATE
0	0	300
0	1	1200
1	0	4800
1	1	9600

12.5 IEEE-488 PARALLEL INTERFACE PORT

See Sections 13.0 and 14.0 for a description of the NPC-764 as a CONTROLLER and DEVICE, and Section 14.0 for a description of the NPC-748 as a DEVICE. The Processor Board DIP switch settings for NPC-748 LISTENER/TALKER operation are shown below:

<u>NPC-748 GPIB DEVICE ADDR</u>	<u>TERMINATION SEQUENCE:</u>
ON = 0 OFF = 1	ALWAYS ON EOI
(ADDR 31 DEFAULTS to 30)	<u>SW6</u> <u>SW7</u>
A0 = SWITCH 1	ON ON EOI ONLY
A1 = SWITCH 2	ON OFF CR
A2 = SWITCH 3	OFF ON LF
A3 = SWITCH 4	OFF OFF CR,LF
A4 = SWITCH 5	
<u>SWITCH 8</u>	
ON = 60 Hz	
OFF = 50 Hz	

SECTION 13: IEEE-488 CONTROLLER

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SECTION 13.0

IEEE-488 CONTROLLER

13.0 IEEE-488 INTERFACE CONTROLLER

The requirement for the automation of test and measurement equipment using the IEEE-488 bus has grown in recent years. IEEE-488 applications range from research projects, which require extremely complex measurements, to production test which requires that the same test be performed repetitively without deviation from the prescribed process.

The IEEE-488 General Purpose Interface Bus (or GPIB) offers the user the flexibility to configure a test system to include most types of test instruments. Due to the standardization of the interface, instruments from different manufacturers can readily be connected using a GPIB Controller.

The NPC-764 can be used as the CONTROLLER in a GPIB environment. It provides a set of commands which have been optimized for ease of use, but still retain a great deal of flexibility. The instrument can also function as a LISTENER/TALKER through resident software in its ROM-based, Analyzer Operating System.

The command set has been designed such that it can be accessed from any application program: It has not been restricted to a specific language, such as CBASIC. Therefore, GPIB control functions can be available from a number of CP/M-compatible higher-order languages. However, CBASIC is standard and a new software interface would have to be written to accommodate another language. See Section 13.7 and contact Nicolet Paratronics for further information.

13.1 COMMAND SET SUMMARY

ABORT GPIB

This command clears the interface. All transactions presently taking place on the bus will stop and the interface is initialized.

RESET

This command performs the reset function on each instrument--individually or universally.

REMOTE

This command enables one or all instruments to respond to the controller's commands.

LOCAL

This command is the opposite of **REMOTE**, returning one or all instruments to local, front-panel control.

TRIGGER

This command is used after an instrument has been set up to make a data collection. Typically, several instruments are set up in sequence; then all are TRIGGERED at the same time to make a data collection.

REQUEST

This command is used to assert the Request For Service line, SRQ. Normally, **REQUEST** will be used when the NPC-764 is acting as a LISTENER/TALKER on the bus.

OUTPUT

This is the command used to send data to each instrument. The data sent is usually a string of characters interpreted by the instrument as set-up instructions.

ENTER	This command is the opposite of OUTPUT . It instructs the instrument to send data to the controller. (The data is usually the result of a specific test.)
STATUS	This command is used to serially request the status of each instrument to determine whether it has completed the last instruction.
SET TIMEOUT	This command is used to change the maximum time to wait for a response on the bus.
LOCAL LOCKOUT	The LOCAL LOCKOUT command is used by the controller to lock all devices under remote control and disable front-panel input. The LOCAL ALL command is used to defeat LOCAL LOCKOUT .
CONFIGURE	This command is used by the NPC-764 to set up data transmission between devices other than the NPC-764.
EOI STATUS	This command is used to identify the end of a data transmission between devices. It is used after a CONFIGURE command.
SENBUS	This is a special command used to tailor controller output for custom applications.
TERM SEQ	This command gives the user flexibility in specifying data termination sequences when used with subsequent OUTPUT or ENTER commands.

The above command set provides the capability to perform most of the common functions required in a GPIB test system. The IEEE-488 standard interface connector, located on the back panel of the NPC-764, allows easy interface to the instruments being controlled. See Figure 12-2.

13.2 REFERENCE DOCUMENTS

The following documents should be referred to if necessary to elaborate on the discussions in the following sections:

CBASIC Language Manual
TMS9914 GPIB Adaptor Data Manual
ANSI/IEEE Std. 488-1978

13.3 ABBREVIATIONS

ATN	Attention
DAB	Data Byte
DCL	Device Clear
GET	Group Execute Trigger
GTL	Go to Local
IFC	Interface Clear
LA	Listen Address
LAG	Listen Address Group (See Note 1)
MA	My Address
MLA	My Listen Address
MTA	My Talk Address
SCG	Secondary Command Group
SDC	Selected Device Clear
SPD	Serial Poll Disable
SPE	Serial Poll Enable
SRQ	Service Request
STB	Status Byte
TA	Talk Address
TAG	Talk Address Group (See Note 2)
TLC	Talker/Listener/Controller
UNL	Unlisten
UNT	Untalk

Note 1: LAG is defined as LA SCG LA SCG

Note 2: TAG is defined as TA SCG

Where XXX indicates to duplicate "XXX" 0 or more times

13.4 GENERAL DISCUSSION

The GPIB command package allows the NPC-764 to be used as a GPIB system controller, or as a device on a bus with a different controller.

The NPC-764 utilizes an 8085 microprocessor with a CP/M operating system, and a TMS9914 GPIB adaptor chip. The GPIB command package uses the TMS9914 to control and interface to the bus. The commands can be used directly from an 8085 assembler program, or from a higher level language such as CBASIC. (The software interface to the commands is very flexible, allowing easy implementation from a variety of other languages.)

As a system controller, the NPC-764 can transfer data to and from devices, respond to a service request, and send these GPIB commands: Remote/Local Changes, Device Clear, Selected Device Clear, Group Execute Trigger and Serial Poll. Commands and data output can be sent to any combination of bus listeners. Complete secondary addressing capability is also available. As a bus device, the NPC-764 can request service, respond to a serial poll and transfer data across the bus when addressed by the controller. A bus status command can be executed at any time to get the complete NPC-764 interface and GPIB status.

13.5 DETAILED GPIB COMMAND DESCRIPTIONS

This section provides a description of each of the GPIB commands including command references.

The I/O Menu is used to enable the interface, set the bus address-- and optionally--to define the data termination sequence. See Section 5.10.

ABORT GPIB OR INIT GPIB

This command will **ABORT** any pending bus transactions, put all devices in remote and assert the NPC-764 as the active controller. Also, all necessary initialization for proper bus functioning is performed. If the TALKER/LISTENER/CONTROLLER (TLC) mask specifies that the NPC-764 is not the system controller, only initialization in the NPC-764 will be performed; the bus configuration remains unchanged.

Sequence

- 1) Reset the TMS9914 bus controller chip
- 2) Save MAX-TIMEOUT in parameter area
- *3) Set IFC
- *4) Wait $100 \mu\text{S}$
- *5) Set $\overline{\text{IFC}}$
- *6) Set REN

*Note: These steps are performed only if the TLC mask = XX1

RESET

The **RESET** command will place a device (or devices) into a known initial state. Two different **RESETS** are implemented. If an address list is specified, an SDC command is sent to each device in the list. Otherwise, a DCL command is sent to all devices. Whether a device implements a DCL or SDC, and the actual effects of the command, depends on the particular instrument used. Only the active controller can issue a **RESET**.

A. Sequence For No Address List

- 1) Set ATN
- 2) Send DCL

B. Sequence For Address Specified

- 1) Set ATN
- 2) Send MTA
- 3) Send UNL
- 4) Send LAG
- 5) Send SDC

REMOTE

The **REMOTE** command is sent by the active controller to place one or more devices under GPIB control. It can be issued to all devices or to any specified device or group of devices. Normally, the **REMOTE** to all devices is not necessary, as it is also executed during the **ABORT** GPIB command. A device (or devices) can be removed from the **REMOTE** state with the **LOCAL** command, then later toggled back to **REMOTE**.

A. Sequence For REMOTE-All Devices

- 1) Set REN

B. Sequence For REMOTE Device

- 1) Set REN
- 2) Set ATN
- 3) Send MTA
- 4) Send UNL
- 5) Send LAG

NOTE: The actual state of a device on the bus when in **REMOTE** is device dependent.

LOCAL

The **LOCAL** command is used to remove a device from GPIB control and return it to its "normal" front-panel operation. This command may be issued to all devices or to any subset of devices. The **LOCAL** command has no effect if a **LOCAL LOCKOUT** has been issued by a controller and not cleared.

Normally the **LOCAL** command is sent by the active controller. Two special cases are permitted when the NPC-764 is not the active controller. If no address is specified, the NPC-764 will be set to the **LOCAL** state independent of the active controller. If the NPC-764 is not the active controller and its own address is specified, it will "LOCK" itself in the **LOCAL** state, so that the active controller will have no access. Sending a **LOCAL** command again with no address will "UNLOCK" the NPC-764.

A. Sequence For All Devices

- 1) Set $\overline{\text{REN}}$

B. Sequence For A Device

- 1) Set ATN
- 2) Send MTA
- 3) Send UNL
- 4) Send LAG
- 5) Send GTL

TRIGGER

The **TRIGGER** command is sent by the active controller to initiate a device function (e.g., take DMM reading, send burst of pulses from pulse generator, etc.). The **TRIGGER** command is sent only to those addresses specified. Note that the **TRIGGER** command is sent to all devices simultaneously; however, internal device delays should be considered for proper operation.

Sequence For TRIGGER Device(s)

- 1) Set ATN
- 2) Send MTA
- 3) Send UNL
- 4) Send LAG
- 5) Send GET

REQUEST

The **REQUEST** command is used to set the status byte that the active controller will read from **MA** during a serial poll. If BIT 6 of the status byte is set, a service request will be sent to the controller. **REQUEST** has no function when in the active controller state, but the status will be set when this state is exited.

Sequence

- 1) Set STB
- *2) Set SRQ
- *3) After active controller executes A serial poll, set $\overline{\text{SRQ}}$.

*Only when BIT 6 = 1

OUTPUT

When in the active controller state, the **OUTPUT** command will transfer DATA to all devices specified in the address list. When in the TALKER-only state, data is transferred to any devices set to listen by the active controller. In this case, the NPC-764 is not the initiating device, and will only output the data after it is requested. Data string length is 0 to 65535 characters (0 to 255 from CBASIC).

A. Sequence

- 1) Set ATN
- 2) Send MTA
- 3) Send UNL
- 4) Send LAG
- 5) Set ATN
- 6) Send DAB
- 7) Repeat 6 for additional characters
- 8) Send TERMINATION SEQUENCE

B. Sequence For TALKER-Only

- 1) Send DAB
- 2) Repeat 1 for additional characters
- 3) Send TERMINATION SEQUENCE

ENTER

When in the active controller state, the **ENTER** command will transfer data from the device specified to the NPC-764. When in the LISTENER-only state, data is transferred from the TALKER to the NPC-764. Data string length is 0 to 65535 characters (0 to 255 from CBASIC).

Sequence

- *1) set ATN
- *2) Send UNL
- *3) Send MLA
- *4) Send TAG
- *5) Set ATN
- 6) Enter DAB
- 7) Repeat Step 6 until the TERMINATION SEQUENCE is satisfied.
- *8) Set ATN
- *9) Send UNT

Notes: *Used only in the active controller mode.

If in the LISTENER-only state, it is up to the user to first determine that data are being transferred to the NPC-764, using the **STATUS** command.

STATUS

There are three different functions of the **STATUS** command. The first can be executed at any time using the address = "B" (controller or noncontroller). This command will return MA for the NPC-764 and the TALKER/LISTENER/CONTROLLER status (i.e., active, idle, or not allowed for each function). Also, the occurrence of any of the following bus commands will be reported:

GET
DCL
SDC
MA
UNIDENTIFIED COMMAND
HANDSHAKE ERROR
IFC
SRQ

The second form of the **STATUS** command is implemented by specifying the address of one GPIB device. This will return the device **STATUS BYTE**, which occurs after a **SERIAL POLL**.

The third form of the **STATUS** command is implemented by not specifying an address. This will cause a serial poll of all bus addresses. The return data will be the status of each bus address (i.e., active, inactive, or service required).

A. Sequence For Address

- 1) Set ATN
- 2) Send UNL
- 3) Send MLA
- 4) Send TA
- 5) Send SPE
- 6) Set ATN
- 7) Receive STB
- 8) Set ATN
- 9) Send SPD
- 10) Send UNT

B. Sequence For "No" Addresses

- 1) Set ATN
- 2) Send UNL
- 3) Send MLA
- 4) Send SPE
- 5) Send TA(1)
- 6) Set ATN
- 7) Receive DAB
- 8) Set ATN
- 9) Repeat 5 thru 8 for TA (2) thru TA (30)
- 10) Send SPD
- 11) Send UNT

SET TIMEOUT

The **SET TIMEOUT** command can be issued at any time to change the maximum time (in msec) to wait for a response on the bus. The **ABORT GPIB** command will reset the max time to a default time specified in the primitives.

LOCAL LOCKOUT

LOCAL LOCKOUT (LLO) is a GPIB universal command, which can be issued by the active controller to lock all devices under GPIB remote control and disable front-panel local control (if any). A **LOCAL ALL** command must be used to defeat the **LOCAL LOCKOUT**.

Sequence

- 1) Set ATN
- 2) Send LLO

CONFIGURE

The **CONFIGURE** command can be used when the NPC-764 is the active controller to set up the GPIB for data transmission between devices other than the NPC-764. One TALKER and any number of LISTENERS can be specified. After the bus is configured, ATN is set false to allow the TALKER to begin transmitting data. The **EOI STATUS** command can be used to look for an occurrence of EOI, which signifies that the data transmission has been completed.

Sequence

- 1) Set ATN
- 2) Send UNL
- 3) Send LAG
- 4) Send TAG
- 5) Set ATN

EOI STATUS

The **EOI STATUS** command is a special-purpose command (designed to be used after a **CONFIGURE**) that indicates the end of data transmission between devices.

SEENBUS

The **SEENBUS** command allows the user to tailor controller output for a special application. Any sequence of universal commands, addressable commands, or data can be specified--up to a maximum of 65535 bytes (255 bytes for CBASIC).

TERM SEQ

The **TERM SEQ** command allows flexible data termination sequences to be used in any subsequent **OUTPUT** or **ENTER** command. Several options are available:

- 1) Terminate output and enter with CR-LF.
- 2) Output--Same as 1, but with EOI true for LF.
Enter--Terminate on EOI.
- 3) Output--Force EOI on last data byte.
Enter--Terminate on EOI.
- 4) Same as 1, but any termination sequence (up to 5 bytes) can be specified in place of CR-LF.
- 5) Same as 4, but EOI is forced on last byte of specified termination sequence.

13.6 GPIB COMMAND IMPLEMENTATION VIA CBASIC

This section describes how to use each GPIB command from a CBASIC PROGRAM. In order to use the GPIB from CBASIC, the file GPIB.BAS must be inserted ahead of any GPIB command references in a CBASIC PROGRAM before compilation. This can be done using the EDITOR or by using: % INCLUDE GPIB.

This CBASIC directive will include GPIB.BAS in the compilation directly following its placement. This file contains the CBASIC source code which defines the GPIB FUNCTION definitions. Any of these function definitions which are not needed by a user program can be deleted, if necessary, to conserve memory space.

In the heading of the GPIB function definitions are several variables the user may wish to change, they are:

- 1) Start address of GPIB commands in PROM
- 2) Start address of 32 byte RAM parameter & stack area

For each GPIB command, a CBASIC statement format is defined. This is the recommended format, and can be modified for a particular application. Any valid CBASIC statement can be used, so long as the function call is intact.

ABORT GPIB OR INIT GPIB

Statement Format (Type on one line):

[<STMT NUMBER>] GPIB.RET% = FN.ABORT.GPIB%
or GPIB.RET% = FN.INIT.GPIB%

Parameters: None

Options: None. (However, the effects of the command will depend on whether the NPC-764 is the system controller.)

Purpose:

- 1) Initialization
- 2) Abort pending bus transactions (only when system controller)
- 3) Take control of bus (only when system controller)

Return Code: GPIB.RET% = 0 NPC is active/system controller
GPIB.RET% = 1 NPC-764 is device

Notes: The **INIT GPIB** command must be used prior to any other GPIB command in a program to assure proper initialization.

SECTION 13.0

IEEE-488 CONTROLLER

RESET

Statement Format (Type on one line):

[<STMT NUMBER>] GPIB.RET% = FN.RESET%(<ADDRESS LIST>)

Parameters: ADDRESS LIST is an ASCII string which specifies which bus devices are to be RESET. (See Section 13.6.1 for Data Format.)

Options:

1. ADDRESS LIST = "valid Section 13.6.1 format" data
This will send a selected device CLEAR (SDC) to all bus devices specified.
2. ADDRESS LIST = NULL. This will send a DCL to all bus devices.

Purpose:

1. Send a SDC to each address specified in the ADDRESS LIST or
2. Send a DCL to all devices on GPIB

Return Code: GPIB.RET% will equal 0 if the command executed properly; otherwise one or more error bits will be set as follows:

BIT

- 0 NPC-764 is not the active controller
- 1 Not used
- 2 Timeout
- 3 Invalid ADDRESS LIST format

Notes: The **RESET** command does not reset the GPIB. The actual effect of the command (if any) depends on its implementation in bus devices.

REMOTE

Statement Format (Type on one line):

[<STMT NUMBER>] GPIB.RET% = FN.REMOTE%
(<ADDRESS LIST>)

Parameters: ADDRESS LIST is an ASCII string which specifies which bus devices are to be set to GPIB control. (See Section 13.6.1 for data format.)

Options:

1. ADDRESS LIST = "valid Section 13.6.1 format" data
Used when the NPC-764 is the active controller to set specific bus devices back to GPIB bus control after a **LOCAL** command with Option 1 has been executed.
2. ADDRESS LIST = NULL. Used when the NPC-764 is the active controller to re-assert the REN LINE, after a LOCAL (with Option 2) has been executed.

Purpose: To set the bus or bus devices back to GPIB control after a **LOCAL** command has been executed.

Return Code: GPIB.RET% will equal 0 if the command executed properly, otherwise, one or more error bits will be set, defined as follows:

BIT

- 0 NPC-764 is not the active controller
- 1 Not used
- 2 Timeout
- 3 Invalid ADDRESS LIST format

Notes: A **REMOTE** command with option 2 will not place devices in **REMOTE** if they have been set to **LOCAL** using option 1. They must be set back to remote using the option 1 format.

LOCAL

Statement Format (Type on one line):

[<STMT NUMBER>] GPIB.RET% = FN.LOCAL%
(<ADDRESS LIST>)

Parameters: ADDRESS LIST is an ASCII string which specifies which bus devices are to be set to **LOCAL** (front panel) operation. (See Section 13.6.1 for data format.)

Options:

1. ADDRESS LIST = "valid Section 13.6.1 format" data. Used when the NPC-764 is the active controller, command specifies devices to **LOCAL**.
2. ADDRESS LIST = NULL. When the NPC-764 is the active controller, a DCL is sent to all devices. If the NPC-764 is not the active controller, only the NPC-764 will be set to **LOCAL**.
3. ADDRESS LIST = "L" used when the NPC-764 is not the active controller. This option will lock the NPC-764 in local until a **LOCAL** command using option 2 is executed.

Purpose: Remove a device (or devices) from GPIB bus control and return it to "front panel" operation.

Return Code: GPIB.RET% will equal 0 if the command executed properly, otherwise one or more error bits will be set, defined as follows:

BIT

ERROR DEFINITION

- 0 Improper controller state
- 1 Not used
- 2 Timeout
- 3 Invalid ADDRESS LIST format

SECTION 13.0

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TRIGGER

Statement Format (Type on one line):

[<STMT NUMBER>] GPIB.RET% = FN.TRIGGER%
(<ADDRESS LIST>)

Parameters: ADDRESS LIST is an ASCII string specifying which bus devices are to receive the Group Execute Trigger (GET) command. (See Section 13.6.1 for data format.)

Options: None

Purpose: To send a **GET** command (simultaneously) to all devices specified in the address list.

Return Code: GPIB.RET% will equal \emptyset if the command executed properly; otherwise one or more error bits will be set as follows:

BIT

- | | |
|-------------|--------------------------------------|
| \emptyset | NPC-764 is not the active controller |
| 1 | Not used |
| 2 | Timeout |
| 3 | Invalid ADDRESS LIST format |

Notes: When using the **TRIGGER** command to trigger multiple devices simultaneously, it is important to consider response times of instruments as it can vary widely (from msec to sec).

REQUEST

Statement Format (Type on one line):

[<STMT NUMBER>] GPIB.RET% = FN.REQUEST%
(<STATUS>)

Parameters: STATUS is an **INTEGER** that will be sent (LSB only) on the GPIB as a response to a serial poll by the active controller.

Options: Bit 6 of STATUS is used to request service from the active controller. If it is set, an SRQ is generated. The remaining 7 bits can be defined by the user.

Purpose: 1) Load GPIB status byte
2) Optionally generate an SRQ

Return Code: Bit 2 Timeout

Notes: 1) **ABORT.GPIB** will clear the status byte.
2) **RESET** to MA will clear the status byte.
3) **REQUEST** can be executed when the NPC-764 is the active controller and the status byte will be loaded, but no other action will take place.

OUTPUT

Statement Format (Type on one line):

[<STMT NUMBER>] GPIB.RET% = FN.OUTPUT%
(<ADDRESS LIST>,<DATA>)

Parameters:

DATA is an ASCII string which is sent to all bus devices that are set to listen. It can be any valid CBASIC string expression (Ø to 255 characters).

ADDRESS LIST is an ASCII string which specifies the bus devices which are to listen to the data. (See Section 13.6.1 for data format.)

Options:

1. ADDRESS LIST = "valid Section 13.6.1 format" data is used when the NPC-764 is the active controller and specifies the bus LISTENERS.
2. ADDRESS LIST = NULL is used when the NPC-764 is not the active controller.

Purpose:

Transmit ASCII data from the NPC-764 to other bus devices

Return Code:

GPIB.RET% will equal Ø if the command executed properly, otherwise one or more error bits will be set, defined as follows:

<u>BIT</u>	<u>ERROR DEFINITION</u>
Ø	Improper controller state
1	In device mode and not addressed to talk
2	Timeout
3	Invalid ADDRESS LIST format
4	NPC-764 is not a TALKER

Notes:

- 1) The TERMINATION SEQUENCE will be transmitted immediately following data to signify end of transmission.

ENTER

Statement Format (Type on one line):

[<STMT NUMBER>] DATA\$ = FN.ENTER\$(<ADDRESS>)

Parameters:

DATA is a string variable which will contain the ASCII data entered from a device, after execution.

ADDRESS is an ASCII string which specifies the address of the device which is to talk on the bus. (See Section 13.6.1 for data format.)

Options:

1. ADDRESS LIST = "valid Section 13.6.1 format" data is used when the NPC-764 is the active controller.
2. ADDRESS LIST = NULL is used when the NPC-764 is not the active controller or for continuing the entering of long data strings.

SECTION 13.0

IEEE-488 CONTROLLER

Purpose: To transmit data from another device on the GPIB to the NPC-764.

Return Code: GPIB.RET% will equal 0 if the command executed properly; otherwise one or more error bits will be set as follows:

<u>BIT</u>	<u>ERROR DEFINITION</u>
0	Improper controller state
1	In device mode and not addressed to listen
2	Timeout
3	Invalid (address) format
4	NPC-764 is not a LISTENER
5	Input data has been truncated

- Notes:
- 1) Data will be entered from the TALKING device until the termination sequence is encountered. However, only the first 255 bytes will be saved in data.
 - 2) To continue entering data when truncated, use the ADDRESS = NULL mode repetitively until data transfer is complete (i.e., GPIB.RET%=0).

STATUS

Statement Format (Type on one line):

[<STMT NUMBER>] DATA\$ = FN.STATUS\$(<ADDRESS>)

Parameters: DATA is a string variable which will contain the status of the device (or devices) specified by ADDRESS
ADDRESS is an ASCII string which specifies the address of the device whose status is required. (See Section 13.6.1 for data format.)

Options: ADDRESS = "valid Section 13.6.1 format" data will return the STB for the device specified by address.
ADDRESS = NULL will return the status of all bus addressees (i.e., present, not present or service required).
ADDRESS = "B" will return the bus status (i.e., hardware status, NPC-764 bus address (MA), and TLC mask).

- Purpose:
- 1) Perform serial poll of specific device and return its status byte, or
 - 2) Get configuration status (i.e., what devices are present, who is requesting service) or
 - 3) Get all available NPC-764 GPIB status

Return Code: GPIB.RET% will equal 0 if the command executed properly; otherwise, one or more error bits will be set as follows:

<u>BIT</u>	<u>ERROR DEFINITION</u>
0	Not active controller
1	Not used
2	Timeout
3	Invalid address format
15-8	Device status byte

<u>BIT</u>	<u>DEFINITION FOR BUS STATUS</u>
0	REN is true
1	IFC is true
2	SRQ is true
3	EOI is true
4	NRFD is true
5	NDAC is true
6	DAV is true
7	ATN is true
8	IFC has occurred
9	SRQ has occurred
10	MA has occurred
11	DCL has occurred
12	Not used
13	Unidentified
14	Incomplete handshake has occurred
15	GET has occurred

SET TIMEOUT

Statement Format:

[<STMT NUMBER>] GPIB.RET%=FN.SET.TIMEOUT%(<TIME>)

Parameters: TIME is the desired maximum time (binary) to wait for all devices to respond to bus transactions (in msec).

Options: None

Purpose: Used to initially specify the max time in a program, or to temporarily change the time to allow for an extremely slow device response.

Return Code: Not used

Notes: The **ABORT.GPIB** (or **INIT.GPIB**) command will reset the maximum timeout to a default value which is specified in the primitives of 5 seconds.

LOCAL LOCKOUT

Statement Format:

[<STMT NUMBER>] GPIB.RET%=FN.LOCAL.LOCKOUT%

Parameters: None

Options: None

Purpose: To enable the local lockout feature of the GPIB (a universal command).

Return Code: GPIB.RET% will equal 0 if the command executed properly; otherwise one or more error bits will be set as follows:

BIT

0	NPC-764 is not the active controller
1	Not used
2	Timeout

Notes: 1. Setting REN false (i.e., LOCAL with null address list) will disable LOCAL LOCKOUT state.

CONFIGURE

Statement Format (Type on one line):

[<STMT NUMBER>] GPIB.RET%=FN.CONFIGURE(<TALK ADDRESS>,<LISTEN ADDRESS LIST>)

Parameters: TALK ADDRESS is an ASCII string which specifies the data output device. (See format for "ADDRESS" in Section 13.6.1)

LISTEN ADDRESS LIST is an ASCII string which specifies which bus devices are to receive data from the talking device. (See the format for ADDRESS LIST in Section 13.6.1.)

Options: None

Purpose: To configure the GPIB to transfer data between devices on the bus without having the controller handle the data, thus optimizing the transfer rate and freeing the controller for other duties.

Return Code: GPIB.RET% will equal 0 if the command executed properly; otherwise one or more error bits will be set as follows:

BIT

0	Not active controller
1	Not used
2	Timeout
3	Invalid ADDRESS format

- Notes:
1. After configuring the GPIB TALKER and LISTENERS, ATN is set false, which will initiate data transfer. The **EOI STATUS** command should then be used to detect the end of this data transfer (if necessary).

EOI STATUS

Statement Format (Type on one line):

[<STMT NUMBER>] GPIB.RET%=FN.EOI.STATUS%

Parameters: None

Options: None

Purpose: To detect end of data transmission between devices set-up by a **CONFIGURE** statement.

Return Code: GPIB.RET% will equal 0 if EOI has not occurred, and 8 if it has occurred.

- Notes:
1. This command should only be used after a **CONFIGURE** has been executed. The GPIB interface could possibly be left in an unknown state if executed at other times.

SENCBUS

Statement Format (Type on one line):

[<STMT NUMBER>] GPIB.RET%+FN.SEND.BUS%
(<COMMAND/DATA STRING>)

Parameters: COMMAND/DATA STRING contains the combined command and data to be output by the controller. Two characters are used to control output type (command or data). A colon signifies the switch to COMMAND output (ATN true) and a semicolon signifies the switch to DATA output (ATN false). For example; the string ":(;WAKE UP:6*;START" would have this effect:

```

: set ATN
? send UNL
( send LISTEN ADDRESS 8
; set ATN false
WAKE UP data sent to address 8
: set ATN
6* send listen address 22 and 10
; set ATN false
START data sent to address 8, 10 & 22

```

Options: None

Purpose: Generation of flexible command/data output structures when the NPC-764 is the bus controller.

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IEEE-488 CONTROLLER

Return Code: GPIB.RET% will equal 0 if the command executed correctly; otherwise one or more error bits will be set as follows:

BIT

0	Not active controller
1	Not used
2	Timeout
3	Not used
4	NPC-764 is not a TALKER

TERMINATION SEQUENCE

Statement Format:

[<STMT NUMBER>] GPIB.RET%=FN.TERM.SEQ%(<DATA>)

Parameters: DATA contains the desired ASCII sequence to signify end of data string on **OUTPUT** and **ENTER**.

Options:

1. DATA = NULL (CR/LF is used)
2. DATA = "E" (EOI is forced on the last data byte.)
3. 1st character of DATA = ":" will force EOI on last byte of termination sequence.

Purpose:

Definition of alternate data terminators for **OUTPUT** and **ENTER**

Return Code:

Not used

Notes:

1. **ABORT.GPIB** (or **INIT.GPIB**) will reset the termination sequence to CR/LF.

**13.6.1 ADDRESS/DATA FORMATS
FOR CBASIC**

<u>FUNCTION</u>	<u>C*</u>	<u>D*</u>	<u>Statement Format</u>
Initialize	X	X	GPIB.RET% = FN.ABORT.GPIB%
Abort/Take Control	X		GPIB.RET% = FN.ABORT.GPIB%
Device Clear	X		GPIB.RET% = FN.RESET%("")
Selected Device Clear	X		GPIB.RET% = FN.RESET%(ADDRESS.LIST\$)
Go To Local-All	X		GPIB.RET% = FN.LOCAL%("")
Go To Local-Device	X		GPIB.RET% = FN.LOCAL%(ADDRESS.LIST\$)
Set NPC-764 To Local		X	GPIB.RET% = FN.LOCAL%("")
Lock NPC-764 In Local		X	GPIB.RET% = FN.LOCAL%("L")
Remote Enable	X		GPIB.RET% = FN.REMOTE%("")
Set Device to Remote	X		GPIB.RET% = FN.REMOTE%(ADDRESS.LIST\$)
Device Status	X		DUMMY.VARIABLE\$ = FN.STATUS\$(ADDRESS)
Configuration Status	X		STATUS.VARIABLE\$ = FN.STATUS%("")
Bus Status	X	X	STATUS.VARIABLE\$ = FN.STATUS%("B")
Group Execute Trigger	X		GPIB.RET% = FN.TRIGGER%(ADDRESS.LIST\$)
Request Service		X	GPIB.RET% = FN.REQUEST%(STATUS.BYTE%)
Output Data	X		GPIB.RET% = FN.OUTPUT%(ADDRESS.LIST\$,DATA\$)
Output Data		X	GPIB.RET% = FN.OUTPUT%("",DATA\$)
Input Data	X		DATA.VARIABLE \$ = FN.ENTER%(ADDRESS\$)
Input Data	X	X	DATA.VARIABLE \$ = FN.ENTER%("")
Local Lockout	X		GPIB.RET% = FN.LOCAL.LOCKOUT%
Set Timeout	X	X	DUMMY% = FN.SET.TIMEOUT%(TIME%)
Configure	X		GPIB.RET% = FN.CONFIGURE%(ADDRESS\$, ADDRESS.LIST\$)
EOI Status	X		GPIB.RET% = FN.EOI.STATUS%
Sendbus	X		GPIB.RET% = FN.SEND.BUS%(COMMAND.DATA\$)
Termination Sequence	X	X	GPIB.RET% = FN.TERM.SEQ%(TERM\$)

***NOTE:** C - CONTROLLER mode
D - DEVICE mode

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IEEE-488 CONTROLLER

- ADDRESS\$** The primary GPIB bus address (range 00-30) of 1 bus device can be followed by any number of secondary commands (range 00-31). A "." is used to separate each address/command.
- Examples: 25
12.15
04.31.09
- ADDRESS.LIST\$** Up to 15 GPIB devices can be specified, using the format for address\$. Device addresses are separated by a ",".
- Examples: 12.15,04.31.09
23
10,15,20,25
- DATA\$** Output data string to device(s). Can be any valid ASCII expression.
- DATA.VARIABLE\$** Name of ASCII variable which will contain data after an **ENTER**.
- STATUS.BYTE%** A byte which is returned to the controller in response to a serial poll. Setting bit 6 will set SRQ to request service from the controller.
- STATUS.VARIABLES** For FN.Status\$("") this variable will be 31 characters long, each character corresponding to a bus address, 0-30, where:
- N=No device present
 - P=Device present
 - S=Device has requested service
- For FN.Status\$("B") the character positions are defined as follows:
1. My address (in binary)
 2. Address status (used primarily when NPC-764 is bus device)
 - BIT: 0-TADS or TACS (addressed to talk)
 - 1-LADS or LACS (addressed to listen)
 - 4-ATN is true
 - 5-LLO is on
 - 6-In remote state
 3. TALK/LISTEN/CONTROL Status
 - BIT: 0-Device mode
 - 1-Active/System controller
 - 2-Controller enabled
 - 3-Listen enabled
 - 4-Talk enabled

13.6.2 CBASIC RESERVED IDENTIFIERS

These identifiers should not be used in application programs as they are used in the GPIB software interface.

RESERVED VARIABLE IDENTIFIERS:

CMD.GPIB%
GPIB.RET%
T.GPIB%
T.GPIB\$

RESERVED FUNCTION IDENTIFIERS:

FN.ABORT.GPIB%
FN.CALL.GPIB%
FN.CONFIGURE%
FN.ENTER\$
FN.EOI.STATUS%
FN.GPIB.ASM%
FN.INIT.GPIB%
FN.LOCAL%
FN.LOCAL.LOCKOUT%
FN.MAXGPIB.TIME%
FN.OUTPUT%
FN.PARM.LOC%
FN.REMOTE%
FN.REQUEST%
FN.RESET%
FN.SEND.BUS%
FN.SET.TIMEOUT%
FN.STATUS\$
FN.TERM.SEQ%
FN.TRIGGER%

13.7 DIRECT USE OF GPIB PRIMITIVES

1. Before calling a command, these locations must first be loaded with the appropriate data:

E000 LSB of starting address of GPIB ADDRESS LIST
E001 MSB of starting address of GPIB ADDRESS LIST
E002 LSB of starting address of DATA string
E003 MSB of starting address of DATA string
E006 Command Branch Index
E007 Command Control Word

2. Execute a call to location F842 HEX.
3. After execution, the return code will be in locations E008 (LSB) and E009 (MSB).
4. Only the stack is preserved, registers are destroyed.

Notes: a) See Section 13.7.1 for data formats of each parameter in 1, above.

- b) For the **REQUEST** command, the binary data is passed in place of the DATA string address.

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IEEE-488 CONTROLLER

13.7.1 ADDRESS/DATA FORMATS FOR ASSEMBLER PRIMITIVES

ADDRESS: First location is length of ADDRESS LIST (1-255). Each subsequent location contains a TALK, LISTEN or secondary address.

BIT

4-0 Binary Device Address
6-5 Address Type: 01 = LISTEN
10 = TALK
11 = Secondary

All commands can use any combination of LISTEN and secondary addresses, except for **ENTER** and **STATUS**, which can have one TALK address and any number of secondary addresses.

DATA (OUTPUT/ENTER)

Two data string modes are available (bit 0 of the command control byte selects which mode): BYTE or WORD. In the BYTE mode, the first location is used as the string length. In the WORD mode, the first 2 locations are used to form a 16-bit-word length (LSB first), thus allowing a 0-65535 character string length. For the **ENTER** command, the string length before execution will be used as the maximum length.

DATA (BUS STATUS)

The first location contains the string length, which is always 3. The next location contains MA, in binary. The third location contains MA status.

BIT

0 Addressed to TALK (TADS or TACS)
1 Addressed to LISTEN (LADS or LACS)
4 ATN is true
5 LLO is active
6 In remote state

This location is primarily of interest when the NPC-764 is a bus device. The fourth location contains the system mode.

BIT

0 Device
1 Controller
4-2 TLC Mask

**COMMAND BRANCH
INDEX**

A binary number of the index of the command selected from the Branch Table

- 0 = Abort/Init
- 1 = Selected Device Clear (alternate command is Device Clear)
- 2 = Go To Local (alternate command sets REN false)
- 3 = Local-Lock
- 4 = Go To Remote (alternate command sets REN true)
- 5 = Device Status
- 6 = Bus Status
- 7 = Trigger
- 8 = Request
- 9 = Output
- 10 = Enter
- 11 = Local Lockout
- 12 = Configure
- 13 = Sendbus
- 14 = EOI Status
- 15 = Set Termination Sequence

**COMMAND CONTROL
BYTE**

BIT DEFINITION

- 0 0 = Byte Mode; 1 = Word Mode
- 1 0 = Listen Address; 1 = Talk Address
- 2 Address conversion required
- 3 Alternate command select (equivalent to NULL address mode of CBASIC command description)
- 5-4 Required controller status:
 - 00 = Don't Care
 - 01 = Must be device
 - 10 = Must be controller
 - 11 = Must be controller if alternate command is not selected
- 6 Must be LISTENER
- 7 Must be TALKER

RETURN CODE

BIT DEFINITION (See below for exceptions)

- 0 Incorrect controller status
- 1 NPC-764 is device and not addressed to TALK/LISTEN
- 2 Timeout
- 3 Not used
- 4 Not a TALKER/LISTENER
- 5 Input data has been truncated to length of data string

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BIT DEFINITION FOR BUS STATUS

0	REN is true
1	IFC is true
2	SRQ is true
3	EOI is true
4	NRFD is true
5	NDAC is true
6	DAV is true
7	ATN is true
8	IFC has occurred
9	SRW has occurred
10	MA has occurred
11	DCL has occurred
12	Not used
13	Unidentified command has occurred
14	Incomplete handshake has occurred
15	GET has occurred

FOR ABORT.GPIB: 0 = Controller
 1 = Device

FOR EOI STATUS: 0 = EOI has not occurred
 8 = EOI has occurred

FOR DEVICE STATUS: The device status byte (STB) will be in the MSB of the return code

13.8 **LEVEL OF GPIB IMPLEMENTATION**

The following table provides a summary of the level of implementation of those functions described in the document: ANSI/IEEE std. 488-1978.

<u>Identification</u>	<u>Description</u>	<u>Notes</u>
SH1	Source Handshake	
AH1	Acceptor Handshake	
T6	Talker	T0 when TALK is off
TE0	Extender Talker	
L4	Listener	L0 when LISTEN is off
LE0	Extender Listener	
SR1	Service Request	
RL1	Remote Local	
PP0	Parallel Poll	
DC0	Device Clear	
DT0	Device Trigger	
C1	Controller	C0 when DEVICE
C2	Controller	C0 when DEVICE
C3	Controller	C0 when DEVICE
C4	Controller	C0 when DEVICE
C27	Controller	C0 when DEVICE

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SECTION 14.0

EXTERNAL CONTROL

14.0 EXTERNAL CONTROL OF THE NPC-700

The NPC-764 can be controlled through three "ports:" RS-232, IEEE-488, or the internal CP/M operating system. The NPC-748 can only be controlled through its IEEE-488 port.

To the NPC-764's CP/M operating system, the internal analysis functions, as a group, look like a device on the IEEE-488 bus. This group of functions is accessed by simply using the correct port address in the CBASIC OUTPUT and ENTER functions. The same commands are used for all three ports.

14.1 COMMAND FORMATS

14.1.1 MENU COMMANDS

External commands to the NPC-700 follow the same format and sequence as used when commanding the NPC-700 from the keyboard. ASCII characters are used for all commands. The actual definition of each ASCII character depends on the menu that is currently being displayed. See Section 7.1.4 for soft-key definitions and Table 14-1 for command formats and field definitions.

14.1.2 BUS COMMANDS

In addition to the MENU COMMANDS, a set of BUS COMMANDS is available to enhance the external control features of the NPC-700. See Table 14-2 for a summary of these commands.

14.1.3 IEEE-488 (GPIB)

For GPIB operation, command strings are limited to 80 bytes. All command strings must end in the correct termination sequence (which is programmable in the NPC-700). Only one BUS COMMAND is allowed in a command string, and it must be the last one specified. For burst commands, the data must follow the command string termination sequence. There are no limits to the length of the data portion of a burst command.

14.1.4 RS-232 (NPC-764 ONLY)

There are no restrictions for command sequences when using the NPC-764's RS-232 interface. Commands are executed as they are input. The only requirements for RS-232 operation are that the electrical interface be set up in accordance with the pin definitions in Section 12.3.1 and that the Baud rate be matched between the NPC-764 and the terminal.

For non-ASCII control formats, use the conversion table in Section 7.1.1.

The following commands enable the NPC-764 to be controlled remotely from an RS-232 terminal:

<u>NPC-764 Key</u>	<u>Remote Command</u>
S1	CNTL Q
S2	CNTL R
F1	CNTL S
F2	CNTL T
F3	CNTL U
F4	CNTL V
F5	CNTL W
F6	CNTL X
SCREEN DUMP	>U or >Z

14.1.5 COMMANDS THAT RETURN DATA

Table 14-3 contains a summary of all commands which return data from the analyzer. Note that some commands are returned as several strings of ASCII characters on the IEEE-488 bus, each terminated with a Carriage Return/Line Feed. Data are ASCII-encoded HEX: therefore the number of characters transmitted will be twice the number of data bytes shown in Table 14-3.

Table 14-1. Command Formats and Field Definitions.

<u>Format Number</u>	<u>Format</u>	<u>Field Definitions</u>
1	A {CRLF}	Keyboard Commands
2	>A {CRLF}	Bus Commands
3	>A <u>HXHX</u> {CRLF}	Address
4	>A <u>HXHX</u> <u>DDDD</u> {CRLF}	Number of Hex Pairs Address
5	>A <u>HXHX</u> <u>HX</u> {CRLF}	Data Address
6	>A {CRLF}	
	<u>AAA...</u> {CRLF}	ASCII Data

NOTE: For the NPC-764, {CRLF} is the GPIB termination sequence and is not used on RS-232 commands. The termination sequence is transmitted automatically by the NPC-764 each time an FN.OUTPUT function is executed from CBASIC.

HX = Hexadecimal Pair (i.e., 0F)
D = Decimal Digit
A = ASCII Character

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Table 14-2. NPC-700 Command List (Other than Keyboard Commands)

<u>Command</u>	<u>Description</u>	<u>Format Number</u>
> 0	Initialize All	2
> 1	Initialize Logic Analyzer (excluding I/O menu)	2
> 2	Lock Keyboard	2
> 3	Unlock Keyboard	2
> 4	Clear CRT	2
> 5	CONFIGURATION LIST	2
> 6	CONFIGURATION LIST-SELECT 48 (32)	
	CHANNEL STATE	2
> 7	Not Used	2
> 8	Not Used	2
> 9	Collect	2
> A	Read State Setup	*6
> B	Read State Data to Aux Memory	*6
> C	Same as above.	*6
> D	Read Timing Setup	*6
> E	Read Timing Data to Aux Memory	*6
> F	Same as above.	*6
> G	Dump State Setup	2
> H	Dump State Data	2
> I	Dump State Aux	2
> J	Dump Timing Setup	2
> K	Dump Timing Data	2
> L	Dump Timing Aux	2
> M	Dump Collection Status	2
> N	Dump Signatures	2
> P	Dump Collection Variables	2
> Q	Dump State Probe A Data	4
> R	Dump State Probe B Data**	4
> S	Dump State Probe C Data	4
> T	Dump Timing Data	4
> U	Dump Screen to RS-232 Device**	
> V	Dump Byte from Memory to Output Device	3
> W	Write Byte to Memory from Input Device	5
> X	Set CRT Cursor Position	3
> Y	Write to CRT From Input Device	*6
> Z	Dump Screen to CRT of Remote NPC-764 over RS-232**	*6

* Burst Commands

** Not available in the NPC-748.

Table 14-3. Command Formats

NOTE: Each logic analyzer byte below (8 bits) is divided into two 4 bit nibbles. An ASCII equivalent byte is then sent for each nibble.

<u>Input Command</u>	<u>Output Command</u>	<u>String #</u>	<u>Length (Bytes)</u>	<u>Description</u>
> A	> G	1	713	State Setup and Configuration
> B	> H	1	413	State Setup
		2	12	State Display Parameters
		3	6144*	State Data
> C	> I	1	413	State Aux Setup
		2	12	State Aux Display Parameters
		3	6144*	State Aux Data
> D	> J	1	271	Timing Setup
> E	> K	1	30	Timing Display Parameters
		2	12	Timing Display Parameters
		3	2	Location of First Data Word
		4	1	Collection Status
		5	2048	Timing Data
> F	> L	1	30	Timing Aux Display Parameters
		2	12	Timing Aux Display Parameters
		3	3	Timing Aux Display Status
		4	2048	Timing Aux Data
	> M	1	2	Collection Status
	> N	1	20	Test Codes: 6 - State 4 - Timing 6 - Aux State 4 - Aux Timing
	> P	1	8	2 - State Trigger Displacement 2 - State Word Count 2 - Timing Trigger Displacement 2 - Timing Word Count
> Q	HXHXDDDD	1	DDDD	State Probe A MSB
		2	DDDD	State Probe A LSB
> R	HXHXDDDD	1	DDDD	State Probe B MSB**
		2	DDDD	State Probe B LSB**
> S	HXHXDDDD	1	DDDD	State Probe C MSB
		2	DDDD	State Probe C LSB
> T	HXHXDDDD	1	DDDD	Timing Probe A
		2	DDDD	Timing Probe B

*The NPC-748 has 2048 bytes less. **Not available in the NPC-748.

14.2 COMMAND DEFINITIONS

The following definitions apply to the NPC-764 commands you can execute from an external controller. The controller can be another NPC-764, a dedicated GPIB CONTROLLER, or an RS-232 terminal. If the controller is another NPC-764, the TRANSMIT field of the controller's I/O menu must be ON to avoid local response to commands. (See Table 14-1 for command formats.)

>0 - Initialize All of NPC-700

This command performs the same function as a power-up reset. All analysis parameters and data are reset, the CP/M operating system is reset, and the GPIB bus is also reset (Interface Clear is set).

>1 - Initialize Analyzer*

This command performs the same functions as the >0 command, except for the CP/M operating system and the GPIB bus. Thus, this command can be sent to the internal analyzer from a CP/M program to initialize only the analyzer and leave the rest of the system intact.

>2 - Lock Keyboard

This command will set a flag which prevents access to the NPC-700 by unauthorized users at the keyboard.

NOTE: The slave NPC-764 keyboard cannot be locked while in the I/O menu on the master. The user can only execute this function from CP/M or while in the analyzer proper (menu's or data display).

>3 - Unlock Keyboard

This command will reset the Lock Keyboard flag and restore keyboard access.

>4 - Clear CRT

This command will cause the NPC-700 to blank its CRT. It is normally used in conjunction with the >Y command to send messages to an operator when the NPC-700 is under automatic control.

>5 - CONFIGURATION LIST

This command provides a convenient method of calling the NPC-700's Configuration List.

>6 - CONFIGURATION LIST-SELECT 48 (32) CHANNEL STATE

This command calls the Configuration List and sets the cursor at the 48 (32)-CHANNEL STATE mode.

>7 - NOT USED

*Same as the >0 command for the NPC-748.

> 8 - NOT USED

> 9 - COLLECT

This command has the same function as the **COLLECT** key, but can be executed from any menu.

> A - READ STATE SETUP

This command is used to read data into the state menu.

> B,C - READ STATE DATA

These commands are used to read data into the State Aux Memory.

> D - READ TIMING SETUP

This command is used to read data into the timing menu.

> E,F - READ TIMING DATA

These commands are used to read data into the Timing Aux Memory.

> G - DUMP STATE SETUP

This command is used to dump the State Analyzer's setup.

> H - DUMP MAIN STATE DATA

This command is used to dump the State Analyzer's Main Memory Data.

> I - DUMP AUX STATE DATA

This command is used to dump the State Analyzer's Aux Memory Data.

> J - DUMP TIMING SETUP

This command is used to dump the Timing Analyzer's setup.

> K - DUMP MAIN TIMING DATA

This command is used to dump the Timing Analyzer's Main Memory Data.

> L - DUMP AUX TIMING DATA

This command is used to dump the Timing Analyzer's Aux Memory Data.

*NPC-748 does not have the B signature.

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> M - DUMP COLLECTION STATUS

This command is used to dump the Analyzer's Collection Status. If not collecting, then dump one byte for the State Analyzer and one byte for the Timing Analyzer.

> N - DUMP SIGNATURES*

Dump Signatures (20 bytes): A,B,C, Main State Memory; A,B, Main Timing Memory; A,B,C, Aux State Memory; and A,B, Aux Timing Memory Signatures.

> O - NOT USED

This command is not used.

> P - DUMP COLLECTION VARIABLES (16 bytes)

This command provides a State Word Count (4 bytes) and a Trigger Displacement (4 bytes); a Timing Word Count (4 bytes) and a Trigger Displacement (4 bytes).

> QXXXXYYYY - DUMP STATE A PROBE DATA

This command is used to dump the State A Probe data with most significant bytes followed by least significant bytes, where XXXX = start of dump displacement from first word collected and YYYY = word count to dump.

> RXXXXYYYY - DUMP STATE B PROBE DATA*

See Q command above.

> SXXXXYYYY - DUMP STATE C PROBE DATA

See Q command above.

> TXXXXYYYY - DUMP TIMING A & B PROBE DATA

This command dumps A Timing Probe data bytes followed by B Timing Probe data bytes. See Q command above.

> U - DUMP SCREEN TO RS-232 DEVICE*

> Vaaaa - SINGLE BYTE MEMORY DUMP

This command is used to dump the byte at HEX address to enabled output ports.

> Waaaabb - SINGLE BYTE MEMORY WRITE

This command writes byte bb to address aaaa.

*Not available in the NPC-748.

> Xpppp - SET SCREEN CURSOR POSITION

This command is used to set cursor position to relative value pppp in decimal (0-1999).

> Yddd..dd\$ - WRITE TO SCREEN

This command is used to write data ddd.. to the screen cursor location. Terminate data with \$. Screen RAM begins at F000(HEX) and ends at F7CF(HEX).

> Z - SCREEN DUMP TO REMOTE NPC-764

This command is used to dump a CR and a LF followed by the first 25 lines of the screen to the RS-232C port, if enabled.

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14.3 TRANSMISSION EXAMPLES (NPC-764 ONLY)

The purpose of these examples is to demonstrate the use of the I/O CONFIGURATION MENU of the NPC-764.

14.3.1 RS-232 INTERFACE

In this example, the NPC-764 will communicate with another device over the RS-232 interface. The device should be capable of displaying and transmitting ASCII data (such as a data terminal).

SET-UP

Connect the NPC-764 to the terminal using the RS-232 interface at the rear of the analyzer. Ensure the terminal is configured as follows:

BAUD RATE:	1200
PARITY:	NONE
DUPLEX:	HALF
WORD LENGTH:	8
STOP BITS:	1

NOTE: If settings on the terminal are not easily changed, the NPC-764's parameters can be changed instead using the RS-232 section of the I/O CONFIGURATION MENU.

Press the **RESET** key and hold it down for at least two seconds to call the CONFIGURATION LIST. Select the I/O CONFIGURATION MENU by pressing the **I** key. Make sure the RS-232 INTERFACE field is **ENABLED**. Advance the blinking cursor to the **KEYBOARD** field by pressing the **I (INPUTS)** key. Press the **SELECT** key to enable keyboard inputs to be transmitted when pressed. Use the **NEXT** and **SELECT** keys to turn the RS-232 INPUT field **ON** to enable the NPC-764 to receive data over the RS-232 interface. Advance the cursor to the **CRT** field by pressing the **O (OUTPUTS)** key. Press the **SELECT** key to turn this field **ON**, enabling the CRT to display input data. Move the blinking cursor to the **RS-232 OUTPUT** field by pressing the **NEXT** key. Press the **SELECT** key to turn this field **ON** to enable transmitting data over the RS-232 interface. See Figure 14-1.

```

                                     I/O CONFIGURATION MENU
-----
INTERFACE: ENABLED * INTERFACE: ENABLED
ADDRESS: 04 * MODE: SLAVE
MODE: CONTROLLER * BAUD RATE: 1200
TERM SEQUENCE: 54 EOI OFF * PARITY: NONE DUPLEX: FULL
TALK: ON LISTEN: ON * WORD LENGTH: 8
RETURN OPTION: AUTO * STOP BITS: 1
-----
KEYBOARD: ON * CRT: ON
 GPIB: OFF * GPIB: OFF
 RS232: ON * RS232: ON
 MEMORY: OFF * MEMORY: OFF
-----
GPIB SLAVE ADDRESS: 00
THE NPC-764 IS NOW SENDING DATA TO A TERMINAL...

  ^S      ^T      ^U      ^V      ^W      ^X
  F1      F2      F3      F4      F5      F6
PREVIOUS  NEXT   SELECT  DEFAULT  CONFIG  TRANSMIT
```

Figure 14-1. Using the I/O CONFIGURATION MENU to transmit keystrokes to another device such as a terminal.

TRANSMIT

Press the **TRANSMIT (F6)** key. The **TRANSMIT** key label will change to ON to indicate that transmission and reception are enabled. Type a few characters on the NPC-764 keyboard. Note that the characters appear on the CRT of the NPC-764, as shown in Figure 14-1, and on the printer or CRT. Now type a few characters on the terminal keyboard. Note that the characters appear on the CRT of the NPC-764.

Press the **TRANSMIT** key again. The key label will now change to OFF. Check the RS-232 MODE field. It should be set to SLAVE. (If not, use the **R**, **NEXT**, and **SELECT** keys to call the SLAVE mode.) Type **CTRL T** on the terminal's keyboard and note that the blinking cursor moves to the next field. (**CTRL S** moves the cursor to the previous field.) Type an **R** on the terminal keyboard and note that the cursor moves to the RS-232 INTERFACE field. In this mode, data or keystrokes from the terminal are executed by the NPC-764 as if the keys on its own keyboard were being pressed.

14.3.2 ANALYZER DATA TRANSMISSION

In this example, the transfer of blocks of analyzer data from one NPC-764 to another will be demonstrated. The example will use the GPIB bus, but the RS-232 bus may also be used.

SET-UP

Connect one NPC-764 to another NPC-764 using the GPIB bus connectors at the rear of each unit. (Disconnect the RS-232 cable to avoid possible noise problems.)

For both units, perform the following sequence: Turn the power switch on or press **RESET** to produce the CONFIGURATION LIST. Then press the **I** keys to call the I/O CONFIGURATION MENUS.

CONTROLLER (MASTER)

For the unit selected to be the CONTROLLER, the I/O menu will be set up in the following steps with the default values in all fields except GPIB INTERFACE (ENABLED), GPIB MODE (CONTROLLER), MEMORY INPUT (TIMING SETUP), and GPIB OUTPUT (ENABLED). After making sure that the GPIB INTERFACE field is enabled, advance the cursor to the GPIB mode field using the **NEXT** key. If the field is set to DEVICE, press the **SELECT** key to set it to CONTROLLER. Access the TRANSMISSION INPUT field by pressing the **I** key. Then advance the cursor to the MEMORY field by pressing the **NEXT** key. Press the **SELECT** key twice to set the memory to TIMING SETUP. Then use the **O** key and the **NEXT** key to access the GPIB OUTPUT field. Use the **SELECT** key to turn this field ON.

Press the **CONFIG** key to call the CONFIGURATION LIST. Select the 16-CHANNEL TIMING mode by pressing the **SEL DOWN** key. Call the menu with the **TIMING** key. Arbitrarily change two or three of the parameters in the menu.

Press the **CONFIG** key to call the CONFIGURATION LIST again. Select the I/O CONFIGURATION MENU by pressing the **I** key. At this point, the first NPC-764 (CONTROLLER) is ready to send the timing menu to the second NPC-764 (DEVICE) over the GPIB bus. See Figure 14-2.

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```

I/O CONFIGURATION MENU
*****
[ ] INTERFACE: ENABLED * [ ] INTERFACE: ENABLED
ADDRESS: 04 * MODE: SLAVE
MODE: CONTROLLER * BAUD RATE: 1200
TERM SEQUENCE: 54 EOI OFF * PARITY: NONE DUPLEX: FULL
TALK: ON LISTEN: ON * WORD LENGTH: 8
RETURN OPTION: AUTO * STOP BITS: 1
*****
[ ] * [ ]
KEYBOARD: OFF * CRT: OFF
GP1B: OFF * GP1B: ON
RS232: OFF * RS232: OFF
MEMORY: TIMING SETUP * MEMORY: OFF
GP1B SLAVE ADDRESS: 00
*****
G -GP1B
R -RS232
I -INPUTS
O -OUTPUTS
D -DEFAULT
ALL
F1 F2 F3 F4 F5 F6
PREVIOUS NEXT CONFIG TRANSMIT [ ]

```

Figure 14-2. I/O menu for transmitting the timing menu to an NPC-764, acting as a DEVICE on the GPIB bus.

DEVICE (SLAVE)

For the NPC-764 acting as a DEVICE, the I/O menu should be set up as shown in Figure 14-3. Note that DEVICE is selected, the DEVICE ADDRESS is set to 00* (using the SELECT key), and the GPIB INPUT field is ON. At this point, the second NPC-764 is ready to receive the timing menu over the GPIB bus.

```

I/O CONFIGURATION MENU
*****
[ ] INTERFACE: ENABLED * [ ] INTERFACE: ENABLED
ADDRESS: 00 * MODE: SLAVE
MODE: DEVICE * BAUD RATE: 1200
TERM SEQUENCE: 54 EOI OFF * PARITY: NONE DUPLEX: FULL
TALK: ON LISTEN: ON * WORD LENGTH: 8
RETURN OPTION: AUTO * STOP BITS: 1
*****
[ ] * [ ]
KEYBOARD: OFF * CRT: OFF
GP1B: ON * GP1B: OFF
RS232: OFF * RS232: OFF
MEMORY: OFF * MEMORY: OFF
*****
G -GP1B
P -RS232
I -INPUTS
O -OUTPUTS
D -DEFAULT
ALL
F1 F2 F3 F4 F5 F6
PREVIOUS NEXT CONFIG TRANSMIT [ ]

```

Figure 14-3 I/O menu for receiving the timing menu from another NPC-764.

*30 device addresses are available.

Now go back to the NPC-764 you have set up as a CONTROLLER and press the **TRANSMIT** key to turn the field ON. The message DONE will flash on the NPC-764 acting as a DEVICE when transmission is complete and the TIMING SETUP data has been transferred from the CONTROLLER.

Press the **CONFIG** key on the second NPC-764 (DEVICE) to get back to the CONFIGURATION LIST. Select the 16-CHANNEL TIMING mode by pressing the **SEL DOWN** key. Call the menu with the **TIMING** key. Note that those parameters that were changed in the CONTROLLER are also changed in the DEVICE.

14.4 MORE I/O EXAMPLES

Your NPC-764's diskette contains two CBASIC programs to further illustrate the instrument's GPIB CONTROLLER/DEVICE and RS-232 MASTER/SLAVE capabilities. These programs are called GPIBEX and RS232EX and do not require any programming to use. Through easy-to-use menus, you can control another instrument and transfer data.

SOURCE

The source listings for both programs are available on the diskette by typing: **TYPE GPIBEX.BAS** or **TYPE RS232EX.BAS**. These listings will be of interest to those of you who would like to modify these programs for your own application. (Type **CNTL S** to stop the screening from scrolling; type any key to start.)

14.4.1 GPIBEX

The GPIBEX program allows you to exercise an external GPIB-compatible instrument, or control your NPC-764's internal analysis functions. In the example that follows, the internal 48 CHANNEL STATE ANALYZER will be exercised by the CONTROLLER, just as if it were an independent instrument on the GPIB bus:

PROCEDURE

1. Insert the diskette and press **ESC** to call the CP/M operating system. Type **DIR** and **RETURN** to make certain the GPIBEX program is on your diskette. (Contact the factory or your nearest sales office if the program is not on your diskette.)

CRUN2 GPIBEX

2. Type **CRUN2 GPIBEX (RETURN)**. After a short delay, when the main menu is displayed, select the LOGIC ANALYZER COMMAND MENU (option 2) as shown in Figure 14-4.

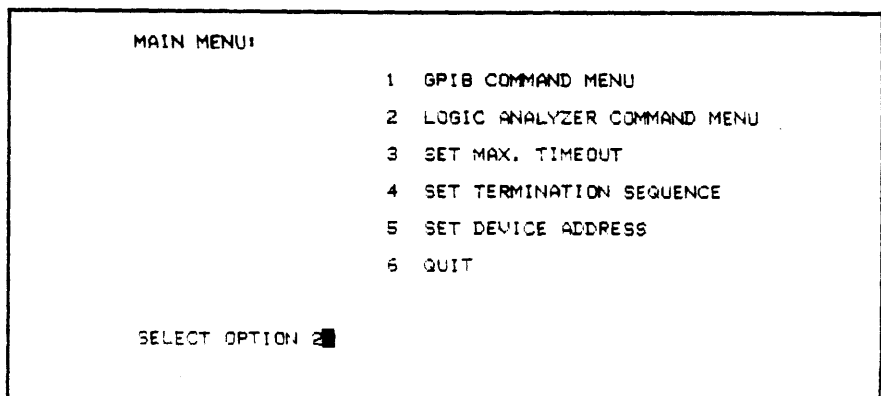


Figure 14-4. MAIN MENU.

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COMMAND MENU

3. After pressing **RETURN**, the LOGIC ANALYZER COMMAND MENU will be displayed. Select the option: SEND COMMAND TO LOGIC ANALYZER (option 1) as shown in Figure 14-5.

```
LOGIC ANALYZER COMMAND MENU:
      1 SEND COMMAND TO LOGIC ANALYZER
      2 SEND SOFT-KEY COMMAND TO LOGIC ANALYZER
      3 GO TO LOGIC ANALYZER
      4 LSAVE
      5 LARECALL
      6 GO TO MAIN MENU

SELECT OPTION 1
```

Figure 14-5. LOGIC ANALYZER COMMAND MENU.

NOTE: Selecting option 1 automatically sets the device address for the NPC-764's internal analysis functions.

4. Press **RETURN** to call the header: ENTER COMMAND STRING.

NOTE: In this program, you can only enter in one command or menu field set-up at a time. See Section 14.1 and 14.2 for command formats and definitions. Be careful to use correct formats; otherwise the software may return you to the analyzer operating system (or possibly crash) and you'll have to repeat the above procedure from step 1.

5. Type **>1 (RETURN)** to initialize the analyzer and display the CONFIGURATION LIST. Then press **RETURN** to call the command menu, as indicated by the message on the bottom of the CRT.

6. Select option 2 to send a soft-key command and press **RETURN**. When the header: SELECT SOFT-KEY (1-6) appears, type **1** to select the **F1 (STATE)** function which calls the state menu.

STATE MENU

- At this point, observe that the state menu is displayed with the cursor in the FORMAT field. Now call the command menu and type 1 and RETURN. When the command string header appears, type in 16 A's, 16 B's, and 16 X's. See Figure 14-6. Next, press RETURN.

```
ENTER COMMAND STRING AAAAAAAAAAAAAAAAAABBBBBBBBBBBBBBBBBBXXXXXXXXXXXXXXXXXX
```

Figure 14-6. Setting up the State Format Field.

TRIG

- Notice that the state menu carries out the format command as soon as RETURN is pressed. Suppose you wanted the A and B FORMAT fields to be set to hexadecimal and binary, respectively. To accomplish this, call the command menu, select option 1, and simply type: HN.
- Next, trigger word will be set up. (The rest of the menu will be unchanged.) To set down to the TRIGGER field, command the F2 (NEXT) key 5 times. (Call the command menu, type 2 (RETURN), and type 2 again (RETURN). Repeat until the cursor is in the TRIGGER field.)
- For this example, we will use the trigger word 0040. Call the command menu, type 1, and type 0040 (RETURN). See Figure 14-7.

```

                                48 CHANNEL STATE MENU
FORMAT:  AAAAAAAAAA AAAAAAAAAA BBBBBBBB BBBBBBBB XXXXXXXX XXXXXXXX
          A HEX B BIN
CLK SEL:  A PRB: J B PPB: A C PRB: A   QUALIFIERS: -AABBCC EL
CLK QUAL: OFF
          OR OFF
PRE-TRIG MEMORY (0-999): 000 WORDS
RESTART:  OFF
TRIGGER:
0         0040 XXXXXXXXXXXXXXXXXXXX -XXXXXX XX
END

```

H - HEX
O - OCTAL
N - DEC
Z - BINARY
Y - ASCII

PRESS RETURN TO CONTINUE

Figure 14-7. The State Menu Set-Up.

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COLLECT

11. To take a data collection, first make sure the A state probe is connected to the test card. Then return to the command menu, type 2, and then type 6 for **F(6) (COLLECT)**. The analyzer will respond initially with no data displayed. To display data, you must command the **F(6) (COLLECT)** key again or select any of the valid display commands. (For example, you can display data by sending a **U (USER format)** command to the analyzer.) See Figure 14-8.

```
MAIN      TRIG 0040 0000000000000000
+001     0041 1000000000000001
LOC:      +002     0042 010000000000010
+003     0043 110000000000011
SIG: C1E7 +004     0044 001000000000100
      19E7 +005     0045 101000000000101
      D8D3 +006     0046 011000000000110
+007     0047 111000000000111
+008     0048 000100000001000
+009     0049 100100000001001
+010     004A 010100000001010
+011     004B 110100000001011
+012     004C 001100000001100
+013     004D 101100000001101
+014     004E 011100000001110
+015     004F 111100000001111
+016     0050 000010000000000
+017     0051 100010000000001
+018     0052 010010000000010
+019     0053 110010000000011

STATE:  DONE

PRESS RETURN TO CONTINUE
```

Figure 14-8. Corresponding State Display.

DIRECT

12. Once data are displayed, you can rapidly access a desired field of the state menu by sending a direct entry command, such as **P (PRETRIGGER)**.

NOTE: The **S1** or **S2 (DATA DISPLAY)** function is not available in the GPIBEX program.

You are encouraged to experiment with other portions of the GPIBEX program using the state or other internal analyzer functions of the NPC-764. You will also find this program convenient for checking out the operation of external GPIB instruments.

14.4.2 RS232EX

The RS232EX program demonstrates the use of the NPC-764's MASTER/SLAVE capability. For this program you'll need two NPC-764's tied together via the RS-232C interface.

PROCEDURE

SET-UP

1. Define one NPC-764 as a MASTER and the other as SLAVE. See Section 12.4 so that the master defaults to "MASTER" and the slave to "SLAVE" upon power-on reset. See Section 12.4. Connect an RS-232 male-to-male cable between units. MAKE SURE THAT PINS 2 AND 3 ARE SWAPPED ON ONE END. (Use a break-out box or equivalent.)

**CRUN2
RS232EX**

2. Press **RESET** and type **I** for both units. On the unit defined as a **SLAVE**, make sure that the **GPIB INTERFACE** field is **DISABLED**, **RS-232 INTERFACE** field is **ENABLED**, and the **RS-232 MODE** field is set to **SLAVE**. On the unit defined as a **MASTER**, set up the **I/O CONFIGURATION MENU** the same as for the **SLAVE**, **except make sure the RS-232 MODE field is set to MASTER**. On both units call the **CONFIGURATION LIST**. Then, for the **MASTER**, press **ESC** and type **CRUN2 RS232EX**.

**COMPARE
UUT**

3. Connect each NPC-764's A state probe to the A input connector on each test card. Make sure both probes are set to **TRUE** and **TTL**.
4. When the **MAIN MENU** appears, select option **1**, **COMPARE UUT DATA WITH "GOLDEN UNIT,"** and when the **LOGIC ANALYZER SETUP MENU** appears, select: **SETUP DATA WITH SIMPLE TRIGGER**. At this point, follow the directions to execute a pre-stored test in both units simultaneously.* The program concludes by comparing test codes to see if the data collections match.

**OTHER LOGIC
ANALYZER SETUPS**

5. After the program displays the test codes, return to the **MAIN MENU**, select option **1** again and then experiment with the other logic analyzer setups. (Go back to Step 2 to set up the **I/O CONFIGURATION MENU** as before.) Option **2** is similar to option **1** except a more complex, multi-level trigger test is executed; option **3** allows you to recall your own, previously-saved file (using **LASAVE**); and option **4** allows you to use a manually set-up test.

**ADDITIONAL RS232EX
TESTS**

6. Other **RS232EX** options are: **VIEW/MODIFY LOGIC ANALYZER SETUP**, which allows you to manually edit or revise the **MASTER's** test setup;** **SAVE CURRENT SETUP & DATA**, allows you to store the revised test on diskette for execution by option **1** (**COMPARE UUT DATA WITH "GOLDEN UUT"**); and the last option, option **4**, which allows you to exit.

***NOTE:** The messages **TRANSMITTING** and **RECEIVING** will appear at the appropriate points in each step of the test. Note that it will take several seconds to several minutes, depending on the amount of data and the data rate used, to complete the data transfer between units.

****NOTE:** After editing the logic analyzer menus, call the **CONFIGURATION LIST** and type **R** to return to automatic control.

APPENDIX A — GLOSSARY

Acquisition	The process by which input logic signals are compared at a discrete instant to a threshold level and recorded.
Active Clock Edge	The clock transition on which all receivers (listeners) interpret the data on the bus. A logic analyzer must monitor the system using this same active edge as its clock.
Address Bus	That bus in the system used to address or define the memory or device location enabled.
Aliasing	The misleading display of a sampled analog waveform when the sample rate is less than twice the input frequency.
Arm	An input or condition that must occur prior to the analyzer trigger conditions being recognized. See Trigger Enable .
ASCII	American Standard Code for Information Interchange; a standard alphanumeric code defining a character set.
Assemble	To combine routines to form a program; to translate a source program into a machine language, usually producing one machine language instruction for each source language instruction.
Assembly Language	A language of mnemonics (resembling English more closely than 1's and 0's) that defines the machine instruction to be executed.
Asynchronous Clocking	Data is clocked into the logic analyzer at a rate unrelated to the system under test. See Timing Analyzer , Synchronous Data .
Asynchronous Data	Data that is not referenced to time. The completion of one operation signals the next operation.
Asynchronous Triggering	Triggering of timing analyzer by signals independent of the analyzer clock.
Automatic Test	A capability of some analyzers that allows the storage of a partial or complete test procedure, plus the expected results, in an auxiliary memory. Tests are then executed with minimal user intervention.
Auxiliary Memory	Space in memory in addition to the active recording memory. It may include RAM and PROM and is used in comparing data, halting on difference, automatic testing and other functions.
Baud Rate	The number of symbols per second that are transmitted (a symbol normally consists of one bit.)

Block Transfer	The movement of a group of fields from one group of addresses to another group of addresses.
Bootstrap	The instructions at the beginning of a program together with a few instructions entered from the control console used to load a program into RAM; a minimal-size loader program.
Branch	See Transfer Command .
Breakpoint	A point in a program in which a process(or) may be made to stop automatically for a check on the progress of the data handling. See Emulator .
Bus System	A network of paths or set of lines that facilitate data flow in a digital system. The common buses are the address, data, and control buses.
Call	To place the necessary initial values of variables in the required addresses and then to transfer control to a subroutine. See Transfer Command .
Clock	The pulses that control the timing of operations in a digital system; some systems having more than one clock. Both the system and any monitoring instrument must interpret the data on an active clock edge when all data are valid.
Clock Delay	The number of occurrences of a clock before an event.
Clock Qualifier	Additional logic analyzer inputs that may or may not be displayed that define conditions as to when data may be sampled or displayed. A sample is taken only on an active clock edge provided the clock qualifier conditions are satisfied. See Active Clock Edge, Sampling .
Clock Slope	The transition or active edge at which the analyzer samples data. See Edge Sensitive .
Combinational Trigger	The pattern of 0's, 1's, and "don't cares" set on all channels that, when matched by the sampled data, causes a trace to commence.
Comparator	A circuit that compares two or more signals and supplies an indication of their agreement or disagreement to initiate some other action.
Compare Data	Any form of display in which a captured data record is manipulated with the data set in an auxiliary memory in such a way as to make differences conspicuous. Two examples: the "exclusive-OR" display and rapid alternation of the display between recording and auxiliary memories.

APPENDIX A

GLOSSARY

Compiler	A routine by which a computer can translate a source program into an object program by assembling and copying from other programs stored in a library of routines.
Composite Video	An analog signal containing not only display information but also horizontal and vertical synchronizing pulses, all of standard polarity and size.
Concatenate	To connect or link elements in a series or chain to form a whole.
Conditional Transfer	An instruction that causes the processor either to continue with the next instruction in the original sequence or to change control to some other designated instruction, depending upon the result of some logic operation. See Transfer Command .
Contents	The word or field stored at a given address or in a given register.
Control Character	A character embedded in operand data that specifies an operation to be done, such as skip to a new page while printing output data.
Correlation	A comparison function; a figure of merit, indicating the number of similarities relative to the number of differences between two elements.
CR	Carriage Return; a control character used to end an input from a keyboard; refers to the mechanical carriage on a printer returning to begin another line, requiring a finite amount of time.
Cross Compiler	A special utility program allowing compiling of code for a processor which differs from the host.
Cross-Domain Linkage	Linkage between the state, timing, and analog domains. See State Analyzer , Timing Analyzer .
CT/SA	Counter-timer/signature analyzer. See Time Measurements .
Data Compression	Any display technique intended to reduce the time or effort required to examine an entire data record. The simplest form converts binary words into hexadecimal words. One of the more effective techniques is signature analysis. See Signature Analysis .
Data Domain	A domain concerned with the total amount of data that must be collected at every event/time in order to characterize synchronous system behavior. A logic analyzer is a data domain monitoring instrument.
Data Qualified Clocking	Specifying a data pattern that is logically ANDed with the clock, to exclude "non-qualified" clock occurrences.
Data Rate	The clock rate for synchronous systems; it must not exceed the specified maximum clock rate of the analyzer.

Debugger	A program used to facilitate testing of a microprocessor system.
Decision	In computer operations, the processes of detecting the existence of specified patterns of relationships in the data being handled, and of taking alternative courses of action based upon the differences detected. See Transfer Command .
Dedicated Probe (Personality Probe)	A probe used to examine a particular microprocessor chip used by clipping over the processor and passively monitoring its state transaction.
Delay	User set for an N-count of selected events. Delay is used to offset in time the position of the final data record with respect to the triggering event. See Clock Delay, Trigger Delay .
Demultiplexing (Demux)	The sorting of multiple signals which time-share a signal path into dedicated lines (channels).
Density	Referring to a memory diskette, how closely information is packed on a track.
Diagnostic Routine	A routine designed to locate either a malfunction in a computer system or a mistake in coding.
Disassembly	The reverse of assembly; to convert machine language code into user recognizable mnemonics, usually done with the help of a dedicated personality probe. See Assembly Language, Dedicated Probe .
Diskette	A flexible mylar oxide-coated storage device, commonly known as a floppy.
Display Polarity	If a logic one at the probe input is displayed as a logic zero on the CRT, the display polarity is said to be inverted (-). If a 1 at the probe inputs is displayed as such, the polarity is normal (+).
DMA	Direct Memory Access is the transfer of I/O information to memory by bypassing the processor.
Don't Care	A channel that may be in either state "0" or state "1," symbolized "X," thereby not restricting data qualification if used in a qualifier word.
Don't Care Triggering	A triggering condition where all of the trigger bits are don't care. The first data that comes along will be traced.

Edge Sensitive	Response of a system to rising (positive) or falling (negative or trailing) transitions as opposed to levels of the clock. See Active Clock Edge .
Edit	To arrange, rearrange, or arbitrarily alter information, especially in format.
Emulator	Hardware containing a microprocessor that replaces the target system's microprocessor and permits execution and interaction with the user's program.
External Trigger	An active signal or an external logic analyzer input that will start (trigger) the analyzer. See Trigger .
Field (in a menu)	One or more adjoining characters treated as a group.
File	A set of records on a common subject and usually organized or ordered on the basis of some combination of items of data uniformly found in all the records of the file, such as a date.
Filter	A circuit that ensures trigger conditions (i.e., Boolean combinations) are satisfied for a minimum time before actually triggering the analyzer.
Flow Chart (diagram)	An analysis technique providing a graphic presentation of a procedure. In programming, a chart setting forth the particular sequences of operations to be done in a computer to handle a particular application.
Format	An arrangement of information on a form, document, or in storage. Configuration of a logic analyzer, e.g., arbitrary labels given to input channels, clock and logic polarities, and display presentation.
Glitch Memory	An auxiliary memory that stores the presence of any glitches between sample periods.
Glitch Triggering	Triggering on a glitch on any specified channel. Usually combined with other logic level requirements on all lines.
Halt on Difference	The trigger caused by any detected difference, when incoming data is continually compared to the contents of an auxiliary memory. See Hold# .
Hold#	A trigger mode that causes a logic state analyzer to continually collect data until a difference is detected between main and auxiliary reference memories. The last collection is held for display with differences intensified.

Hold-Time	The time following the active clock edge where the analyzer may sample data. Since many systems do not hold the data past the active clock edge, a logic analyzer should have a zero hold time ideally.
Housekeeping	Computer operations which do not directly contribute to useful data handling--extracting of fields, verifying the identification of the input, etc.; in general, the setup (including initialization) and cleanup operations in a program.
In Circuit Emulation	See Emulator .
Independent CLK/TRIG Qualification	The concept of forced acceptance of an otherwise not qualified trigger word; occurring before or after (i.e., displaced from) the clock qualification. See Clock Qualifier , Trigger Qualifier .
Initialization	When first powered up, a processor will have a random program counter value so that setting variables and control indicators in a program to their starting values is necessary.
Instruction	A word or field that directs the automatic computer to take a certain action. The instruction usually consists of a command together with one or more operand addresses, which, taken together, cause the computer to act upon the indicated operands.
Intelligent Controller	Referring to GPIB instruments it is the director of any transactions on the bus equipped with a uP.
Interpretive Routine	An executive routine which, during the course of data-handling operations, translates a stored macrocoded program into a machine code and at once performs the indicated operations by means of subroutines.
Interrupt	An external control system used to suspend normal operations and possibly cause new sequences of instructions to be followed.
Inverse Video	A black on white display used to highlight trigger words; or in serial displays, the data received. In formatting an analyzer, it is used to indicate user-definable parameters.
Iterative Loop	A repeated group of instructions in a routine.
Jump	See Transfer Command .
Label	An identifier, in either human or machine language, e.g., a magnetic tape label identifying the tape or an address identifying a storage location, or an alphanumeric character representing an input channel.

Latch	A glitch latch detects narrow pulses and stretches them such that they are traced by the clock.
LF	Line Feed. See Carriage Return .
Library Routines	A collection of standard and fully debugged programs, routines, and subroutines by means of which many types of problems and parts of problems can be processed or handled.
List	A string with pointers (called links) added to each data element to enable their logical sequence to be different from their physical sequence.
Listener	A device in a digital system that is reading data from the bus.
Load Routine	A routine which causes a computer to transfer object code into RAM storage. See Bootstrap .
Lockout	The recognition by the processor of an illegal or impossible triggering requirement. Simplification of the restraining conditions is recommended.
Lookup Table	A memory structure, typically a ROM, where a specific address yields specific yet repetitive data. The process of finding a function in a table when provided with a key and arguments.
Loop	An iterative routine, usually subject to instruction modification in a progressive manner until an exit condition is reached.
Machine Language	Information represented in a form which an automatic computer can handle directly. For example, the result of assembling a symbolic source program is the machine language object code.
Macro, Macrocommand, Macroinstruction	A symbolic command or instruction that is translated into two or more machine language instructions (often an entire subroutine) by the translator program.
MDS	Microprocessor Development System; a system of hardware and software used to develop and help debug microprocessor-based products. See Emulator, State Analyzer, Timing Analyzer .
Microprocessor Analyzer	A special logic state analyzer that monitors microprocessor bus systems and displays the results in microprocessor mnemonics. See Dedicated Probe .
Microprogram	A basic command repertoire for an automatic computer that consists only of basic elemental operations which the programmer can combine into commands to suit his/her own convenience and in terms of which he/she would then program.

Mnemonic	A set of symbols that combine a series of 0's and 1's, as used by a machine, into symbols that suggest the instruction to a human; e.g., LDA is Load Accumulator.
Monitor	To execute a program under the control of an executive routine; an executive routine capable of controlling the execution of a number of different programs one immediately after the other, including the clean up and restart between each program, thus relieving the operating personnel of some control functions and reducing computer idle time. See Operating System .
Multiphase Clocking	Input data is organized as multiple words in width, each word with its own clock input. User may select positive or negative-going edges for each clock -- a necessary capability when the analyzer is used with a microprocessor that multiplexes data and address information on the same bus (for example, the Intel 8085).
Multiple Occurrences	Part of the trigger conditions that require the analyzer to find the trigger state a specified number of times in order to completely satisfy the trigger conditions. See Clock Delay , Trigger Delay .
Multiplexed	The process of transmitting more than one set of signals over one bus; e.g., address and data information could occur at different times on the one bus. Information on the bus is defined by the control signals.
Negative Logic	Refers to a logic "0" being true; a common misconception is that it refers to negative voltage levels.
Negative Time	Events that occur before the defined trigger conditions are satisfied are said to occur in negative time. See Pretrigger .
Nested Loop	A subroutine enclosed within a larger subroutine.
Nibble	Half of a byte.
Nonoccurrence Trigger	In the sequential triggering mode, means trigger, if any word other than B occurs N events after A. It can have meaning for parallel triggering, if the inputs are organized as two words. Then the term means trigger if one word and anything but the other word occur simultaneously. See NOT Trigger .
NOP	An instruction causing no change in the processor except a normal increment of the program counter, in other words, to go to the next instruction.
NOT Trigger	A trigger condition that initiates data acquisition any time a state other than the state specified occurs. Also known as non-occurrence triggering.

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GLOSSARY

Object Program	A program produced by some translation process, as by the use of a compiler routine, from a source program. An object program need not be in a machine language, but often is.
Op Code	The portion of a software instruction set that defines the next operation to be performed. Often extra information (the operand) will be required to define the data or location on which the op code will operate. See Dedicated Probe, Mnemonic .
Operand	The part of an instruction to a processor that defines the data or the location to which the op code refers; something acted upon.
Operating System	An executive routine and other supporting programs used to assist and control, in part, the operation of a computer. See Monitor .
Parallel Trigger	The event caused by the occurrence of a selected word (or simultaneous occurrence of two words, like address and data) at the inputs. One of the obvious advantages of logic analyzers over conventional analog oscilloscopes.
Parity Check	A type of redundant check in which the evenness or oddness of the number of 1 bits is verified.
Pass Count	See Clock Delay, Trigger Delay .
Patch	A correction made to a program and usually inserted into the control sequence by unconditional transfers of control.
Pointer	A means of designating the address or name of something. See Label .
Positive True Logic	Refers to a logic "1" being true.
Polling	A technique in which multiple I/O devices time-share an I/O channel without contention.
Post Processing	Processing of data after the collection is complete. For example, determining the number of occurrences of a specific data pattern.
Post-trigger	Positive Triggering. Post-trigger means the captured record consists of data, all or most of which occurred after the trigger.
Pretrigger	Negative Triggering. Pretrigger means that the captured record consists of data, all or part of which occurred before the trigger. It can never be greater than the memory capacity.

Probe	The pod on the logic analyzer that actually connects to the circuit under test. Important criteria are probe loading and speed capability. The mechanical interface to the system under test. A basic probe consists of a ribbon cable terminating in a pod with flying leads. The pod contains input buffers and sometimes other circuitry, which can, for example, set the logic threshold.
Program	A set of in-sequence, coded instructions for a digital computer, sometimes known as a routine or a subroutine.
Program Counter	An essential register in a CPU keeping track of where a program is.
Protocol	The sequence of events or the format of signals or lines that must occur for the correct operation of a system.
Qualifier	An additional input, not necessarily recorded as data, but used to enable the trigger or the analyzer's clock input.
Radix (base)	The fundamental number of a number system, e.g., 10 in the decimal system.
Restart	Used with sequential trigger to restart the trigger sequence should a given state occur; useful when a critical branch is encountered in program flow.
Resolution	The time interval over which a transition displayed by a timing analyzer may have occurred. For a single channel this will be 1 clock period. Between channels, the resolution is ± 1 clock period.
Routine	A program, or a part of a program.
Sample Window	The sample window consists of set-up and hold times and is the time about the sample instant when the analyzer registers data.
Sampling	Examining a voltage at discrete instances in time with the implied assumption that the waveform is constant until the next sample strobing.
Scroll	The rolling or shifting of the logic analyzer display window through the analyzer memory.
Sector	The subdivision of a track on a memory disk. On floppy diskettes two versions are available: hard and soft sectored.
Sector Access Hole	A small hole on the floppy diskette jacket through which the index hole can be sensed by the disc drive timing sensor.
Selective Trace	A data collection where the data sampled is selectively edited before being stored in memory; performed to conserve memory space.

Sequential Trigger	A trigger condition that must be satisfied by a series of states in the specified sequence. The event caused when and only when data word B follows data word A by N selected events. N is usually set by the delay function.
Serial Data Bus	A bus on which the data is all transferred bit-by-bit in a serial manner.
Set-Up Time	The time prior to the active clock edge during which data may be sampled by the analyzer. Therefore, the data must be valid for at least this interval.
Signature Analysis	A technique for data compression, in which the entire data record is compacted into one or more 4-character words through an algorithm that weights each bit equally. For all practical purposes, this signature is unique to the data and may be compared to a known, good signature.
Simulator	A program used in a host computer to test the correctness of machine code. See Emulator .
Single Step	To execute a program on a step-by-step basis.
Skew	The difference in the delays across channels as measured between the probe tip and the point when the data is interpreted by the analyzer.
Soft-Key	A key that serves different purposes at different times, as defined by software, and is labeled accordingly.
Source Program	A program that is to be translated to an object program; for example, a program written in a symbolic language.
Stack	A group of storage locations used to temporarily store data, in a modified sequence, according to the last location, unlike a program counter.
State Analyzer	State-sequences of a digital system are recorded for analysis with a logic state analyzer.
Storage Dump	A read-out or printout of the contents of a storage device. Usually only the contents of internal storage are dumped, and usually the read-out is onto magnetic tape or disks, and the printout onto paper via a line printer or typewriter.
Synchronous Analyzer	Traces data which are synchronized with the clock of the system under observation. See State Analyzer .
Synchronous Data	Data that coincides or is valid with a defined clock or control signal.

System Clock	Clock signal provided by the system under test.
Table	A listing. See State Analyzer .
Talker	A device in the system that is putting data onto the IEEE-488 bus.
Text Editor	A program used to develop and modify source programs, used before translation to an object program.
Threshold	A signal amplitude level that divides one state from a second. A facility that allows the threshold on a logic analyzer to be varied either for different logic families or to check marginal data transitions.
Threshold Adjust	An adjustment control on a logic analyzer used to vary the voltage level that defines what a logic analyzer will interpret as a logic "0" or logic "1." This can be software programmable or a hardware adjustment point. See Variable Threshold .
Threshold Range	Spread of threshold voltage to accommodate different logic families.
Time Out	If a trigger event does not occur within a preset time, a trigger event will be forced.
Time Measurements	Time measurements with logic analyzers that may be relative (between samples), absolute (from trigger word), or between states and trigger stack levels, or between edges of specific traces.
Timing Analyzer	A timing analyzer monitors the activity of a digital system and presents its observations as a state-time display or a pseudo-waveform of logic levels and transitions.
Trace Programming	To follow the control sequence instruction-by-instruction, usually producing a printout reporting the consequences of each instruction; a routine for doing tracing. A hardware trace is the video display of a logic waveform.
Track	The path on which data is recorded on a floppy diskette, lying directly beneath the read/write head.
Transfer Command	A signal that conditionally or unconditionally specifies the location of the next instruction and directs the CPU to that instruction. See Conditional Transfer .
Transfer Rate	The speed of data transmission, usually quoted in characters (baud) or bits per second.
Transient Triggering	Triggering of a timing analyzer on a state that only occurs as a transient. See Hold# .

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GLOSSARY

Trigger	A word, or sequence of words or events, that defines the point where a logic analyzer references its trace to the system activity, the start of a data collection process. To initiate the capture of a data record. Loosely, it may refer to the triggering event. See Parallel, Sequential, Non-occurrence, Pre and Post-trigger .
Trigger Delay	Delay added so that the Nth word past the trigger is recorded by the logic analyzer.
Trigger Disable	A condition or state that cancels the trigger enable. See Restart .
Trigger Enable	A state that must occur before the trigger word will be recognized. See Arm .
Trigger Output	A synchronizing signal out of a logic analyzer that signifies that trigger conditions are met. It may be used to synchronize external instruments such as oscilloscopes or to arm a second analyzer. See Comparator .
Trigger Qualifier	A combinatorial signal (word) that places constraints on satisfying trigger conditions; i.e., the analyzer is triggered only when the specified trigger state and the trigger qualifier conditions occur. See Data Qualified Clocking .
Utility Routine	A routine to perform functions auxiliary to the running of other programs. Examples are storage dump routines, bootstrap routines, tape label routines.
Variable Threshold	A type of probe that allows user-adjustment of the logic threshold voltage reference. User can adapt the analyzer to different logic families or to test noise immunity. See Threshold .
Waveform	A modified timing mode, with an A/D converter as the front-end of the analyzer which performs like a digitizing oscilloscope.

APPENDIX B — SELF-TEST

INTRODUCTION

Included on the disk that you receive with your NPC-764 are three programs which perform a self-test of the hardware and software. Although these tests are not exhaustive, they do provide the user with a measure of confidence that the NPC-764 is operating properly. These tests are KYBDTEST.COM, which tests the keyboard; DSK5TEST.COM, which tests the disk drive and the diskette; and RAMTEST.COM, which tests the 48k of dynamic RAM. The PROCESSOR SELF-TEST, which tests the processor's STACK, RAM, ROM, character generator, RS-232C interface IC, IEEE-488 interface IC, and the 8155 timer IC, is in analyzer ROM and can be accessed whenever the CONFIGURATION LIST is displayed.

With this extensive set of self-test programs, the user should be able to confirm whether the microcomputer portion of the NPC-764 is functioning properly. The analyzer portion can be further tested using Sections 2.0 and 6.0 of this manual. The results of those examples are predictable so the user should have no trouble confirming whether the analyzer is functioning properly.

To perform the disk-resident self-test functions, turn power on, load the diskette onto the drive, press **ESC** to exit to CP/M, press **CAPS LOCK** to its down position, and type the file name of the test that you want to execute.

KEYBOARD TEST

For example, to test the keyboard, type:

KYBDTEST (RETURN)

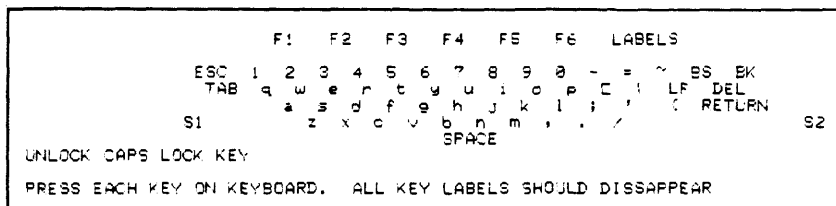


Figure B-1. KYBDTEST.

The program will be loaded into RAM and begin executing. As shown in Figure B-1, there should be a representation of the keyboard layout on the display. As you test each key, the associated key on the display will disappear. Press each key in turn until all keys have been recognized and removed from the display. If you press a key which does not have a duplicate on the display, the program will give you the opportunity to stop the test or to continue. (The program does not know whether you pressed the wrong key, or if the keyboard is defective.) The ASCII value (in HEX) of each key is displayed in the upper left corner of the CRT as each key is pressed.

DISK TEST

To perform the disk test, type:

DSK5TEST (RETURN)

```
NTE NICOLET-PARATRONICS 7000 48K CPM 2.2 OF 9-3-81
A>DSK5TEST
TARBELL DISK DIAGNOSTIC
STANDARD VERSION 1.8
77 TRACKS    16 SECTORS

SELECT DRIVE. (A/B/C/D) A
HOW MANY RETRYS? (0-9) 0
SELECT STEP RATE. (S/M/F)
FULL TRACK SEEK? (Y/N) Y
TO START TEST TYPE RETURN.

0000 READ ERRORS DETECTED.

REPEAT TEST? (Y/N/C=CONTINUOUS) █
```

Figure B-2. DSK5TEST.

Answer each question asked by the program as shown in Figure B-2. Unless you have external disk drives installed, your answer to the SELECT DRIVE statement will always be **A**. The number of retries to select (attempts to retest a specific block of the diskette upon encountering a failure) is up to you. Normally, that number should be 0. The drive will read each track in sequence. However, if you answer **"Y"** to FULL TRACK SEEK, drive will step back to track zero after reading each track and then proceed to the next track in the sequence. When the test is complete, you have the option to repeat the test once, continuously, or not at all.

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RAM TEST

To perform the test of the dynamic RAM (not the high speed analyzer RAM), type:

RAMTEST (RETURN)

```
48K DYNAMIC RAM TEST PROGRAM 08/17/81
SET RAM TO HIGH(ADDR).EOR.LOW(ADDR)

TESTING ADDRESS:      5283
LAST FAILED ADDRESS:  ----  EXPECTED: --  READ: --
TOTAL FAILURES:       0
PASSES COMPLETED:   0
```

Figure B-3. RAMTEST.

The program performs a fast READ and WRITE, then begins a "walking ones and zeroes" test. This portion of the test is quite long, so you might not want to monitor this test, merely check the results. See Figure B-3.

PROCESSOR SELF-TEST

Press **RESET** to call the CONFIGURATION LIST. Press the **BREAK** key to execute the PROCESSOR SELF-TEST as shown in Figure B-4.

```
Y$%&'()*+,-./:;<=>?@ABCDEFGHIJKLMN
PQRSTUVWXYZ[\]^_`abcde fgh: jk lmnopstuvwxyz{|}~
N/A 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
NORMAL HALFBLINK BLINK OVERLINE HALFBLINK REVERSE
RAM TEST: PASS
ROM CHECKSUM TEST: 6D2D 6438 C5F8 6866 D45C 65EE A24F 54CF
9155 TIMER TEST: PASS
RS-232 TEST: PASS
VERTICAL SYNC TEST: PASS
IEEE-488 (GPIB) TEST: TIMEOUT TMS9914
```

Figure B-4. Processor Self-Test.

The program will first print both character sets on the top of the display. It then prints each of the "attributes" used in the display: NORMAL video, HALFLIGHT video, BLINKING messages, full intensity REVERSE video, OVERLINE, and HALFLIGHT REVERSE video. Next it performs a test of the stack RAM and checksum of each of the ROMs. The first row of checksums is the reference data stored in ROM. The second row is the result of the current checksum calculation. Finally, the 8155 timer IC, the RS-232C* interface IC, and the IEEE-488 interface IC are tested. This test is repeated continuously, so press **RESET** to exit from this program.

***NOTE:** In order for the RS-232C test to pass, you must connect the TRANSMIT pin (3) to the RECEIVE pin (2).

THE ELECTRONIC WORKBENCH: APPLICATIONS IN RESEARCH AND DEVELOPMENT, PRODUCTION ENGINEERING AND FIELD SERVICE

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INTRODUCTION

In the days of vacuum tubes and transistors, hardware design engineers predominantly staffed design labs using a primary set of tools consisting of good scopes, spectrum analyzers and VTVM's. Each instrument had a learning curve and a set of idiosyncracies to be dealt with. Computers were used primarily for modeling and limited computation by a select few skilled in software techniques. As logic became integrated in small, medium and large scales (SSI, MSI and LSI) and the cost of memory plummeted, the rise in computing power enabled most design engineers to consider the use of microprocessors in new implementations.

Many products became "smart" and the instrument industry created a standard by which different test and measurement tools from different manufacturers could be addressed and controlled through a common interface. This standard is known by several names: GPIB, 488 bus, HPIB, IEEE bus to name a few, but officially, it is known as the IEEE-488-1978 Standard Digital Interface for Programmable Instrumentation.

The microprocessor and integrated logic market's rapid growth and the parallel increase in complexity of electronic products required new tools and techniques for product design engineers (both hardware and software) and production/support personnel.

This paper will attempt to explain and suggest how today's existing technology aids designers and technicians in reducing the cost and effort expended in creating, testing, and servicing microprocessor-based products. The man-machine interface to each element of a test setup has been successfully integrated and automated testing of traditionally hand checked systems is possible.

DESIGN OF DIGITAL SYSTEMS: THE PROCESS

Today, a typical new product design might well involve the following considerations:

- A microprocessor based design (8 or 16 bit processors like 8085, Z80, 6809, 68000, or NSC 16000 series MPU's)
- High speed hardware comprised of random logic (ECL logic family)
- Digital signal processing circuitry for error correction or Discrete Fourier Transform (DFT) computation

- An analog man-machine interface (voice actuated via ADC or digital speech synthesis prompting)
- Complex (perhaps real-time) software including built-in operational diagnostics in PROM
- Large RAM storage for data base
- Custom logic (LSI gate-arrays)

Hardware engineers today design typically from the gate level to systems level, where functional building blocks (of MSI and LSI technology) provided by integrated semiconductor manufacturers are combined into a desired functional unit with SSI "glue." Conventional analog troubleshooting skills, anticipation and analysis of problems such as noise, glitches, ground loops and cross-coupling are still required. Scopes fall into the background of importance as logic analyzers emerge as the "window" into the circuit under test (CUT), because of the large number of events happening in parallel, and complex triggering requirements to begin observation.

A software designer, with a totally new set of computer based tools, has emerged to design the algorithm under which the product will function. He writes the code (programs it), subsequently traces (debugs) its operation on a software simulator or other microprocessor development system (MDS), and finally assesses real-time execution efficiency.

Once the product specification is crystallized by management, the process begins. In order to minimize the total design time, the process proceeds in two parallel and similar iterative sequences. See Figure 1.

Hardware to Run the Software

The hardware designer still performs the circuit design as has been done traditionally, perhaps utilizing a general-purpose desk top computer to function as more than a fancy math problem solver. Servo-loop simulation, component value optimization, and/or circuit analysis (i.e., BODE, FFT or sensitivity plots) are selectable from off-the-shelf applications programs or from the home-grown variety, frequently found in trade journals.

After circuit design and timing diagram sketching, prototyping begins typically with a wire-wrapped breadboard. Testing proceeds with the help of a logic timing analyzer to pin-point timing races, decoding

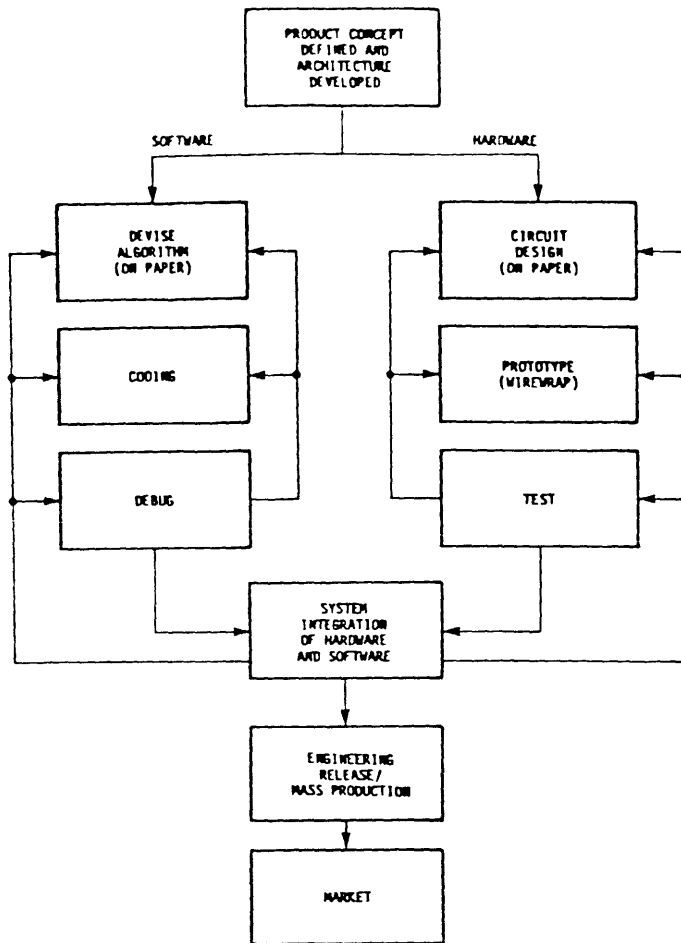


FIGURE 1.

errors, multiplexing errors, glitches, reduced noise margins, slow transitions or stuck bits, incorrect clock phasing or sequencing, etc. throughout the circuit. This ultimately leads to printed circuit board layout. The process is briefly repeated but accomplished much more quickly after the PCB layout is committed. This iterative debugging job, although far from trivial, is still well supported by test and measurement instrument manufacturers, as it has been in the past.

A little known and even lesser used piece of instrumentation that proves to be helpful during a limited portion of hardware development is the pattern generator. Available in nearly its present form for approximately the past decade, the parallel output or "word" generators perform the inverse of the logic state analyzers--instead of acquiring synchronous data they produce and output synchronous patterns per pre-programmed requirements. Pattern generators have found uses in hardware design checkout before the proper software development has produced "in-situ" testable code.

A typical application might be to imitate a limited amount of processor activity via address and data bus patterns, and to output these patterns to stimulate a particular bus component and facilitate testing.

Some instrument manufacturers have recently recognized this market need and have included small word generators in their logic analyzers. Word generators, however, are also available with an asynchronous internal clock producing a more realistic output as a "timing simulator." The greatly increased channel capacity and memory capability to generate greater lengths of microprocessor program "activity" is available in programmable standalone timing simulator/word generators from various manufacturers.

Software to Control the Hardware

The object of the software design task, often misjudged and subject to delays and cost overruns, is to design program code to drive the hardware which is concurrently under design. The tools for program development consist of:

- A typewriter-like console serving as the user interface to a timeshare system, mainframe, mini or microcomputer
- An editor to enter, modify and store program modules
- Assemblers (or cross-assemblers) and compilers (or cross-compilers) to enable programmers to write in a more English-like language than the basic executing machine language
- Linkers to allow modular program development without regard to absolute addresses but rather by functional name.

With the exception of the console itself, the "tools" consist of fairly specialized applications software. The edited, assembled and linked code can be executed and tested functionally on a simulator (a micro or minicomputer on which the preceding tasks were accomplished). However, some testing can only be accomplished in the target system into which the software is transported as firmware.

Transporting or downloading this executable code into reprogrammable read only memory (EPROM) requires a PROM programmer and a suitable communications interface between it and the simulator. Several manufacturers presently offer such equipment. This executable code, when inserted into the newly-developed prototype hardware environment and tested using logic analyzers, provide some of the initial steps of system integration. Here time dependent or I/O related problems can be best pinpointed, with logic timing or logic state analyzers or both working in conjunction with one another.

Again, an iterative process soon uncovers errors whereupon the user must return to the source code, modify it with an editor, assemble it, link it, and reload it into a new PROM resident in the target system.

SYSTEM INTEGRATION

There comes a time during product development when the hardware is sufficiently well developed that it necessitates a more stringent test than a small pattern generator could provide. When the software designer has successfully tested his program on an MDS or simulator, the next logical step for him would be to attempt to run it on prototype hardware (either a breadboard or a brass-board). This becomes a time of much fingerpointing called "systems integration." The tools used by the hardware and software development crew become increasingly overlapped and intertwined.

Emulators provide some answers to register activity within the microprocessor itself while logic analyzers, with their analog and digital (synchronous or asynchronous) examination capabilities provide a view of total hardware and software operation.

For Systems Engineers—Emulators

Some standalone microprocessor "in-circuit emulators" available today are truly transparent to the system. Behaving exactly like the microprocessor they are supposed to emulate, they assure the systems integration team of true systems conditions with respect to timing, circuit loading and software objects in the user's address space.

The emulator has significantly shortened the steps in which software designers correct code, as linked object code can be loaded into emulation RAM via a suitable communications interface. The aforementioned communications interface commonly in use for linking the microprocessor development system (MDS) with both PROM programmers or standalone in-circuit emulators is the serial EIA RS-232C interface. It performs adequately to enable communications between the MDS and the emulator or programmer. By replacing the target microprocessor and executing PROM resident programs with the emulator, the engineer has the ability to control the system much as the microprocessor itself had done.

Emulation may be accomplished in real-time and transparently with fast bipolar emulation memory (taking the place of PROM) and a "background" memory where the functions of in-circuit emulation are executed. The latter allows examination of the program and software "patching" while in the target system.

In-circuit emulation provides a "microscopic" view of the role of the microprocessor in the newly designed product enabling register-to-register activity to be monitored thereby helping eliminate register utilization conflicts.

For Systems Engineers—Logic Analyzers

A complimentary tool providing a much more "macroscopic" view of the entire system is the logic state analyzer which may be equipped with a passive microprocessor personality probe and mnemonic disassembly capability.

When used in conjunction with interactive in-circuit emulators, they further aid the software designer by allowing quick confirmation of properly performing initialization routines of the various system components (typically, LSI devices). Historically, these tools had a vast array of knobs and switches to befuddle even the most daring software designer. Recently, however, a standard and familiar typewriter-like keyboard has emerged as the primary user-interface to logic analyzers, thus virtually eliminating the need for any knobs and switches. Syntax driven soft function keys make the use of such keyboard controlled machines friendlier than ever before. A color display option is even available from one manufacturer.

Two is Better Than One

As was previously alluded to, the microprocessor based product could have a variety of signal types including synchronous digital ones (processor bus activity), asynchronous digital ones (interrupts or error correction feedback) and analog waveforms such as sinusoids or non-linear functions (voice). The ability to trigger on asynchronous (perhaps high-speed ECL) interrupts and also trace synchronous microprocessor activity looking before and after the interrupt (thus monitoring the microprocessor's reaction) necessitates two analyzers running concurrently. Each analyzer must be independently clocked and qualified yet they can be linked to function together.

Since the two independent sections can either trigger or enable the other, synchronous program activity can be related to asynchronous I/O events. This ability to cross boundaries of synchronous activity into the asynchronous circuit phenomena is particularly useful at system integration time.

It is then a relatively simple matter to determine whether some portion of the program is limping under some unique operating conditions or if a subsection of the hardware is marginal or failing intermittently.

The NPC-764 from Nicolet Paratronics (and its predecessor the PI-540) contains two such independent analyzers. These logic analyzers also employ optional fast A to D converters allowing analog phenomena to trigger either synchronous or asynchronous recording of digital activity thereby encompassing every kind of signal type found in modern day electronic circuitry. Logic analyzer performance measuring hardware options enable the software designer to measure his real-time software execution improvements quantitatively and allow memory utilization versus availability to be graphically charted over the entire program's execution.

After system integration has undergone several iterations from both hardware and software designers and the product generally performs its desired function, engineering releases it to be mass produced. Again this combined hardware/software capability can play an important part in testing, at any stage in the product's life.

PRODUCTION TEST OF THE NEW PRODUCT

As the first engineering release items appear on the production floor a new set of problems arises imposing the pressures and constraints of efficiency and speed. Fundamentally, they are communications problems--how to convey to the production test engineers and technicians information concerning the proper operation of the circuit, how to go about testing it for such and teaching them a procedure for effective troubleshooting of the board. This sometimes needs to be repeated at frequent intervals to accommodate the influx/outflow of technicians in production test. It is fairly uninteresting to the design engineer after about the third time around and most designers disdain sustaining engineering!

Test Procedure Generation and Documentation

Test routines are essentially defined during the latter stages of design and development of a product. The information accumulated during this phase can be passed on to production test, quality control and service personnel who otherwise might unnecessarily duplicate previous efforts, rediscovering facts already known.

Some instrument manufacturers have included mass storage devices such as disk or tape drives as standard equipment. This allows the user to "can" certain switch settings or complete instrument setups for future recall, be it the next day or in six months. The Nicolet Paratronics NPC-764 logic analysis system includes such a mass storage device. Since this logic analyzer already included a microprocessor, a standard typewriter-like keyboard and flexible disk drive storage system, (all of the essential ingredients of a small computer system) this manufacturer added the popular microcomputer operating system CP/M^R to pioneer the first T&M instrument with user-access to the microprocessor. See Figure 2. This operating

system provides a text editor to help document the test itself or the test results.

The transition into production has been eased by properly utilizing the disk/tape storage to save instrument setups, data collections and test descriptions to be used in production test. While system integration progresses, the documentation required for the production staff can be nearly completed by the time the prototype is finished.

An example of such a documented message for a test is illustrated in Figure 3.

Coupled with its ability to store measurement parameters as well as known-good reference data collections, the foundation for fully automated test execution with one single user interface (and learning curve) has been created, as will be discussed shortly.

Software Maintenance

In many companies the responsibility for sustaining engineering belongs to the production test engineers. Under those circumstances, minor software changes and, on some occasions, major software revisions need to be made. The need for production engineering to use a smaller-scale, easily reconfigurable microprocessor development system for these tasks has been recognized. The "kernel" of such a system must be able to read source diskettes, edit the code, assemble (or cross-assemble for different families of microprocessors), link and download to PROM programmers or emulators. This requirement is much like that of the engineering department MDS. The added ability of being able to monitor real-time program flow with personality probes dedicated to the specific processor type in use further enhances the power of such a system.

The NPC-764 is being applied to exactly such tasks by several large corporations nationwide.

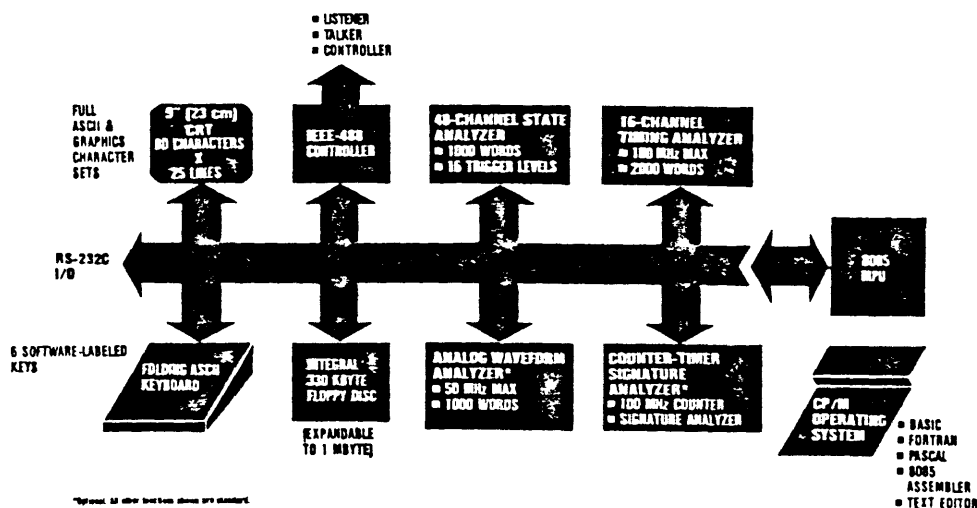


FIGURE 2.

```

A>TYPE TSTDSCP.TXT
THIS TEST WILL VERIFY THE CORRECT OPERATION OF:
- FIFO BUFFER ADDRESS COUNTER (U35 - 39)
- LOAD INHIBIT LOGIC (U19, 22, & U25 - 32)

IF THE TIMING CORRELATION MEASURES LESS THAN .75μ
THE CLOCK SYNCH FLIP FLOP (U36) SHOULD BE REPLACED.

IF NO ACTIVITY ON THE BUFFER OUTPUT IS SEEN THE HEAD
CLOCK IS OUT OF SYNC. REPLACE U23.

```

PRESS ANY KEY TO CONTINUE

FIGURE 3.

Quasi-Automatic Testing

Simple quasi-automatic (with minimal user intervention) test execution requires essentially no computer programming experience. A CP/M^R batch processing utility called "SUBMIT" allows concatenation of files to function as a unit to facilitate such test execution. An example is illustrated in Figure 4, and is called "AUTOTEST."

```

A>TYPE AUTOTEST.SUB
TYPE TSTDSCP.TXT ; TEST DESCRIPTION
PAUSE
TYPE PROBES.3RD ; PROBE PLACEMENT (3RD TEST)
PAUSE
LARECALL TEST3
LASAVE BADTEST3
TYPE TSTDSCP2.TXT ; 2ND HALF TEST DESCRIPTION
PAUSE
TYPE PROBES.4TH ; PROBE PLACEMENT (4TH TEST)
PAUSE
LARECALL TEST4

```

FIGURE 4.

"AUTOTEST" is a file composed of several standalone test and text files interspersed with an executable program to pause while the user performs various tasks. This composite file is a program that sequentially executes the previously created "test programs" in prescribed order. In this case it first types the circuit description, then the test description. These are interspersed with a user prompt to press any key on the keyboard when ready to proceed. The computer can then continue typing text after one CRT screen is filled--to obviate speed reading. See Figure 5 for an illustration of instructions for the test technician concerning at which test point to place his probe terminators.

```

A>TYPE PROBES.3RD
PLACE THE STATE PROBES AT THE FOLLOWING TEST PORTS:
A PROBE TEST PORT 12
B PROBE TEST PORT 13
C PROBE TEST PORT 5

PLACE THE TIMING PROBE TERMINATORS AT THE TEST POINTS
AS LISTED IN THE TABLE BELOW:
A PROBE CHANNEL TEST POINT #
D0 1
D1 2
D2 6
D3 8
D4 14
D5 16

PRESS ANY KEY TO CONTINUE!

```

FIGURE 5.

When all the probes are placed and the operator is ready, the NPC-764 will automatically recall a "canned" test. This is done with the "LARECALL TEST3" line of "AUTOTEST" (LA represents logic analyzer). The user need only press one syntax driven soft function key labelled "COLLECT" near the CRT to execute this test and acquire data. Saving suspicious looking data can be performed via the "LASAVE BAD TEST3" line.

Comparison of Results to Engineering References

Array Signatures as "Test Codes"

If the first test was a synchronous interface to some bus structured architecture, the NPC-764 facilitates quick comparison of results by calculating a "data collection signature." In principal this is the same as a nodal signature analysis but an array signature is computed in three groups of 16 inputs. Examination of this signature will reveal (with a probability of one) if the test result differed even by one bit out of the 48,000 bits collected, when compared to the reference (the disk-stored sample). With only one bit altered, a vastly different signature results in one of the three displayed signatures. See Figure 6.

AUX	TRIG	0000	DI	MAIN	TRIG	0000	DI
	+001	0000	FF		+001	0001	JP 004
LOC: TRIG	+002	0001	JP 004	LOC: FE	+002	0002	40
	+003	0001	FF		+003	0003	00
SIG: CDFD	+004	0002	40	SIG: FE00	+004	0040	LD SP,
CR12	+005	0003	00	8732	+005	0041	FC
100F	+006	0040	LD SP,	100F	+006	0042	23
	+007	0002	FF		+007	0043	LD IY,
	+008	0041	FC		+008	0044	21
	+009	0042	23		+009	0045	80

FIGURE 6.

Trace Correlation

If the first test was an asynchronous sampling of some random logic, a similar technique of comparing the results of all 16,000 data samples collected exists. Entitled "correlation" the number of similar vs. dissimilar samples on each trace is calculated between the main and reference memory and displayed beside the traces as illustrated in Figure 7.

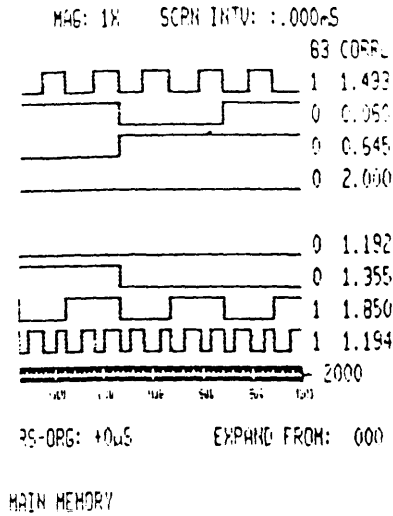


FIGURE 7.

Since, at a glance, a quantitative assessment of the likeness of data collections can be made, these two techniques greatly increase productivity and testing not only of first production run samples but also in field service, as will be examined shortly.

Timing Traces Labeled

To ease the record-keeping tasks of hardware design engineers some manufacturers have included in their logic analyzers the ability to use your own signal names in labeling the timing analyzer traces. This eliminates the need for a look-up table to identify that trace A2 and B6 really represent MREQ and RD respectively. The ability to reorder displayed traces after data collections have been made also facilitates making the timing diagram displayed look more like that tattered engineering sketch. See Figure 8.

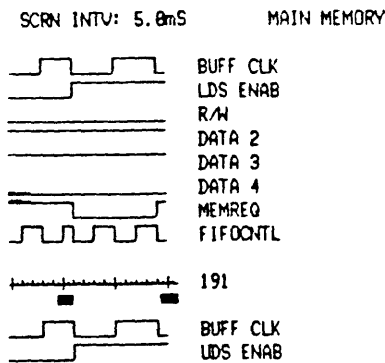


FIGURE 8.

Test Failures

If for some reason the test results differ from that expected, the technician can reposition his probes and alter the menu as needed to further track down the difference without interrupting the AUTOTEST sequence or he can simply continue making a note in his test log of the failure on that board.

Should he choose to continue with more quasi-automated testing, he can return to the logic analyzer's operational configuration menu and then escape to the CP/M^R disk operating system, each with individual keystrokes. The computer will recall the next prompting message concerning probe placement or a test description for another section of the board. This process continues until the tests are complete.

A total of 30 menu/setups and data collections can be stored on a single diskette enabling the test or design engineer to store an entire battery of tests for one card or module conveniently, with full prompting and test/circuit descriptions.

Automated Measurements

With the emergence of a microcomputer accessible by the instrument user in the form of a general-purpose desk-top computer, the logic analyzers of today have evolved into instrument controllers with more flexibility than ever before. Not only can such instruments execute their own functions under program control, they can also control other devices interfaced by way of the IEEE-488 standard parallel interface bus.

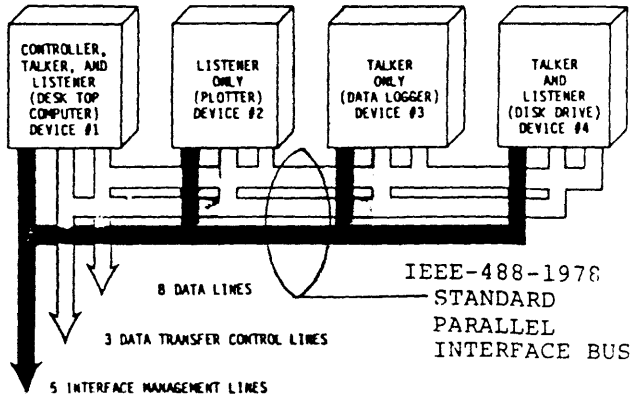


FIGURE 9.

The NPC-764 logic analysis system functions as a universal bus controller/data handler. The man-machine interface to different test instruments made by different manufacturers has hereby been significantly simplified. In the long run, using the NPC-764 for creating and storing tests with a logic analyzer as well as using it in conjunction with other standalone bus controllable instruments, will require less test engineering effort than is already being wasted employing traditional troubleshooting.

One example is testing an algorithmic error correction module used in a communications network. To sample over the long time intervals required to perform such tests necessitates tedious monitoring and periodic logging of data currently requires operator presence.

This process is now nicely automated from the nucleus of the same workbench that was used to debug the circuit itself. Furthermore, it can be run entirely in the absence of an operator.

Initial "noise" levels in the Bit Error Ratio (BER) test set are established via program control running in the IEEE-488 intelligent bus controller and the averaging interval started. At the end of the interval, the BER test set returns the results of the measurement to the controller which in turn logs it and then repeats the test or automatically readjusts the noise level via bus control pending the outcome of such a test. Results are then plotted on an IEEE bus controllable X-Y plotter and are ready upon return of the operator. To further increase productivity, several such Bit Error testers can be run in parallel with a single controller and printer/data logger to increase test throughput. Such a system is illustrated in block form in Figure 10.

FIELD SERVICE

Instrument manufacturers are attempting to solve the increasingly difficult problem of properly servicing the ever-growing complexity of microprocessor based equipment. Several approaches exist, but each with inherent limitations. Of the currently used approaches, the following will be discussed:

- o Built-in self-test
- o Replacement modules (board swap)
- o Signature analysis
- o Remote logic analysis

Built-In Self Test

This approach is viable depending upon product complexity and the production scale anticipated. In some cases it is better to accept the higher cost of after-sales service instead of spending large amounts of front-end money designing self diagnostics and in coping with the required additional memory installed in a product. Another approach is to include a special self-test mode during which an alternative operational command sequence is executed while certain man-machine interface points are exercised. This, however, requires that much of the system be operational.

Replacement of Modules (Board Swap)

One form of hardware service is assembly level substitution from a local inventory. This eliminates on-site repair and the disruption it causes customers. But the product manufacturer must maintain a service module inventory or "board float." See Figure 11 for an illustration of product flow for exchanged module repair.

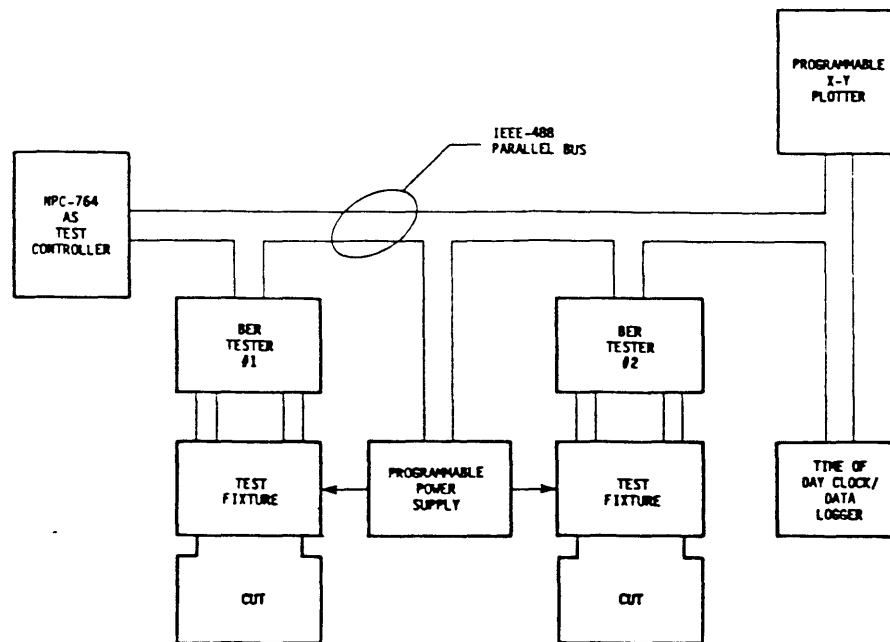


FIGURE 10.

Limitations include the fact that it is a synchronous technique and races generated by the board can cause unstable signatures. If not eliminated by design, a measurement window that excludes this uncertain data from entering the measurement cycle must be chosen. Another important factor to consider is program interrupts. The microprocessor in the resulting attempt to service an interrupt will break the stimulus program continuity and destroy signature repeatability. But solutions do exist and despite these potential drawbacks, free-running address cycling and software-driven signature analysis proves to be a useful tool in digital troubleshooting.

Remote Logic Analysis

There exists a huge network of telephone lines and facilities that can connect your location to almost any other place in the country, if not the world. Instrumentation manufacturers have designed EIA RS-232C serial interfaces into their microprocessor design/development/debugging equipment to permit easy interface through low data rate modems to capitalize on this vast network.

Nicolet Paratronics Corporation has recently equipped the NPC-764 with a standard software enhancement called the I/O communications package. This package allows the entire operation of the logic analyzer to be controlled from a standard video terminal or another similarly equipped NPC-764 via the RS-232C interface and telephone modems. See Figure 12.

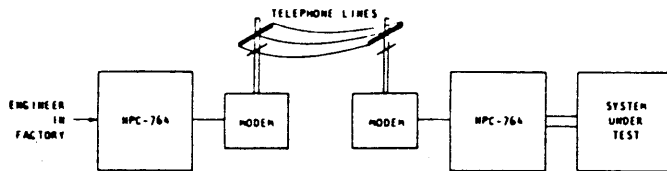


FIGURE 12.

Most any technically knowledgeable individual can now be sent into the field to setup the modem/NPC-764 combination and then "walked through" the troubleshooting/fault isolation exercise by factory-resident experts. These experts can give instructions displayed on the CRT screen of the NPC-764 in front of this individual in the field. See Figure 13 for an example of such instructions.

```
*****
TRANSMISSION=INPUT          * TRANSMISSION=OUTPUT
KEYCARD: ON                  * CRT: ON
GP16: OFF                    * GP16: OFF
FS232: ON                    * FS232: ON
MEMORY: OFF                  * MEMORY: OFF

GP16 SLAVE ADDRESS: 00
```

OKAY JOHN NOW PLACE YOUR PROBES AT THE OUTPUT OF U43(THE BUS BUFFER) AND LETS REDO THAT LAST TEST. WE'LL EXAMINE THE RESULTS FROM OUR END!

FIGURE 13.

A known-good reference data collection of critical test points throughout the circuit may be "canned" on disk for inclusion as a field service tool, much like for production test technician use previously described. If certain rudimentary tests fail, telephone assistance from the factory or depot level could be solicited. Additional test setups or reference data collections can be sent to the remote analyzer. Coupled with the NPC-764's ability to view nearly any electronic phenomenon in a microprocessor-based product's bowels, such remote troubleshooting would help obviate the need for good, expensive and hard-to-find field service engineers.

Conclusion

No matter in what test environment the engineer finds himself, certain fundamental considerations need to be made. The test and measurement instrumentation he selects for use must be cost-effective, increase his productivity, and maintain a high return-on-investment for his employer to assure higher revenues (for his employer and himself).

As a result of the closely related procedures followed by today's design engineers, many of their tools have a remarkably large common ground. Manufacturers of test and measurement instrumentation will be providing more multi-purpose tools that function flexibly for the benefit of the user, whatever his skill level. This can already be seen today in the applications of the NPC-764 serving as a nucleus of such an electronic workbench.

Construct your own universal development system

Design a flexible, expandable μ P development system that can serve as a stand-alone component or in a network.

Sandra Reynolds, Applied Microsystems Corp

You can build a universal microprocessor development system using standard off-the-shelf instrumentation and software. Features such as timing analysis, signature analysis, frequency measurement, built-in memory-test diagnostics and scope loop-synchronization signals become available when you combine components at hand in configurations that meet your immediate needs. And although procuring a complete universal development system from one source might seem less time consuming, the availability of logic-analysis systems, PROM programmers, stand-alone in-circuit emulators and other components has actually simplified the integration task.

Because these components must communicate freely, however, you must be certain to determine whether you must reformat data on the communications channel or whether the components provide the capability of changing baud rate, start and stop bits and parity bit. In some cases, for example, you might have to write a short dump routine or bit translator. Nevertheless, the integration task is relatively straightforward.

Putting together the parts

Where do you begin? If you have ever gone through the arduous task of selecting capital equipment for a new design project, you know first-hand the fear that the equipment you choose will soon be obsolete. To avoid that problem in this case, choose equipment that can be used in a project as system components, then broken out as stand-alone units, reintegrated and finally incorporated into larger test systems. You can combine these parts into new systems or enhance an existing system if the parts have built-in switch-selectable and/or software-selectable capabilities that facilitate rapid integration; examine your options.

If, for instance, you already have a software or

software/hardware μ P development system, using off-the-shelf instruments to share the workload could prove a better solution than purchasing a new system. Off-the-shelf hardware is particularly valuable in the integration phase of a project because it provides

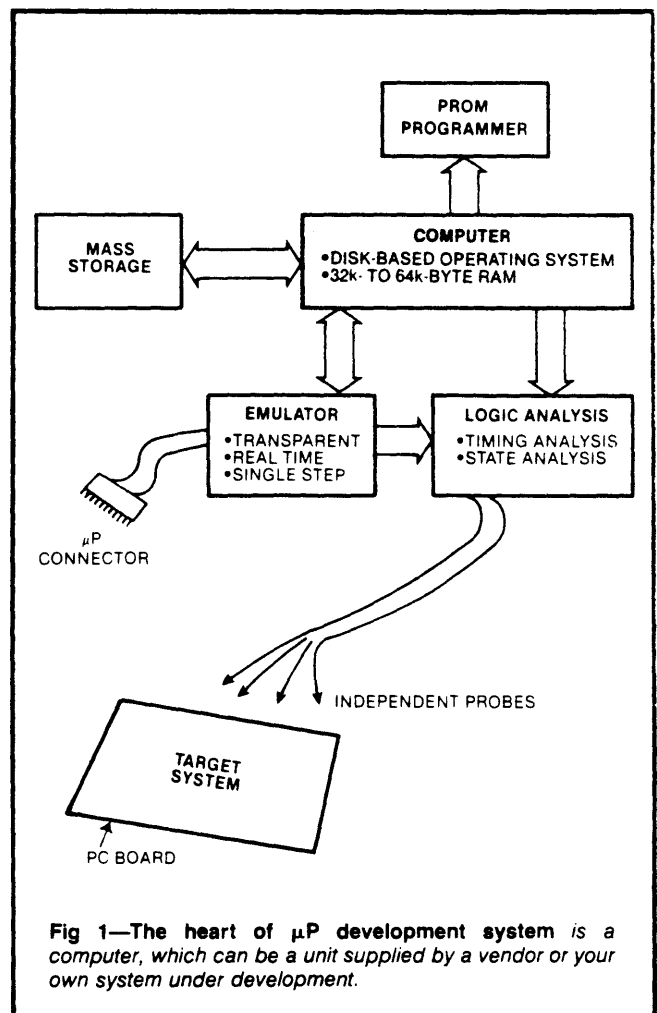


Fig 1—The heart of μ P development system is a computer, which can be a unit supplied by a vendor or your own system under development.

Independent hardware and software provide much flexibility

independent patching and debugging resources. If your current system has adequate software support, adding more powerful hardware/software-integration tools greatly enhances it.

The block diagram in Fig 1 shows that the heart of such a system is a computer—either vendor supplied or your own system under development. If you must finish a design as inexpensively as possible, use the system under development in conjunction with carefully selected tools such as a PROM programmer and a stand-alone in-circuit emulator and/or a logic analyzer. That is, when cost is a primary factor, consider how much you can spend on today's project and what cost can be ascribed to a future one.

Select standard software

Hardware represents only a portion of system-development cost, however; software is another factor. No longer do most companies wish to be burdened by

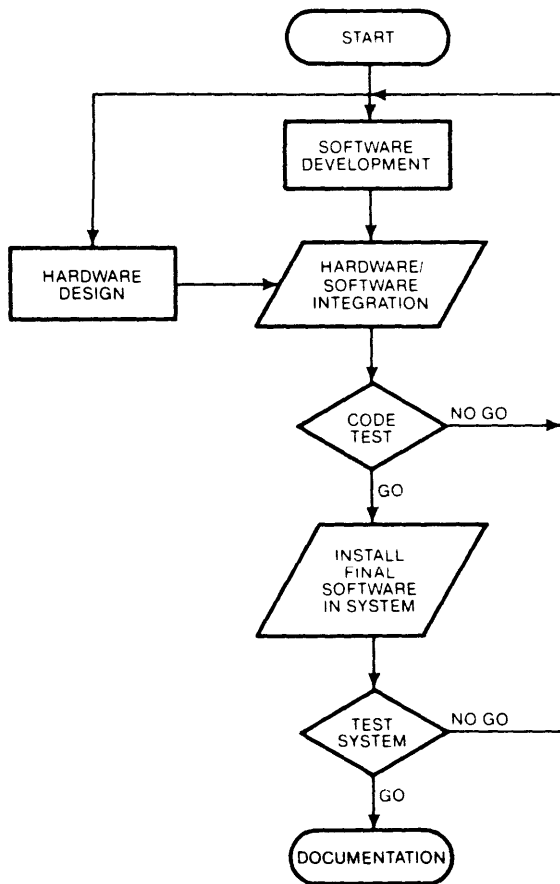


Fig 2—Follow these steps to complete the design of your own μP development system.

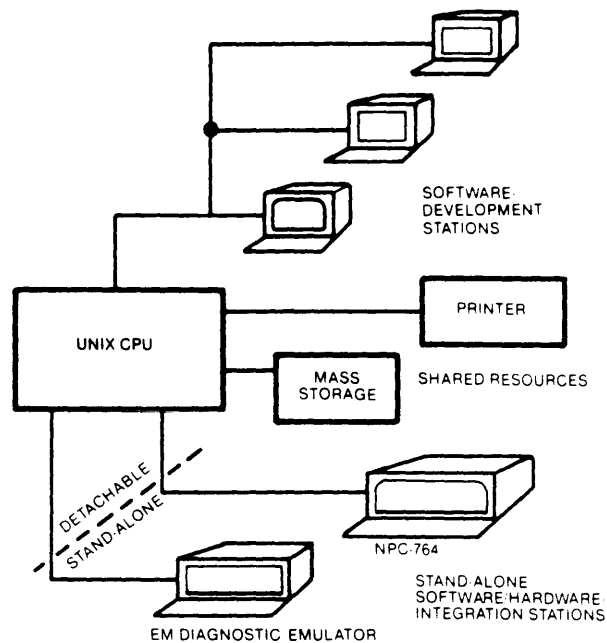


Fig 3—The system you design could later be integrated into a larger network. The example illustrated combines a CP/M-based logic-analysis system and diagnostic emulator in a UNIX-based network.

the cost of developing custom software—they understand the cost advantages of using a standard operating system. And although the high-level languages, software assemblers and cross assemblers used in standard operating systems are less efficient than code generated by assembly-language programs, the time they save can be significant. Note also that the additional memory costs of using high-level languages are important in a mass-produced product but not as crucial in one-of-a-kind systems. Hence, evaluating the desirability of a particular operating system becomes simpler when viewed as a tradeoff among memory cost, engineering cost and the number of products to be produced.

Another major development-system capability, in-circuit emulation, carries its own set of specifications. These include the types of μP s supported, satellite vs dedicated operation, real-time vs quasi-real-time program execution, transparent vs interrupt address-space constraints, diagnostic capabilities, disassembly and/or in-line-assembler features, real-time trace and overlay memory.

Two additional capabilities, logic-state and -timing analysis, significantly reduce the design and debugging time of system hardware and interactive software. Logic-analysis specifications include the ability to trigger and to resolve timing measurements, the

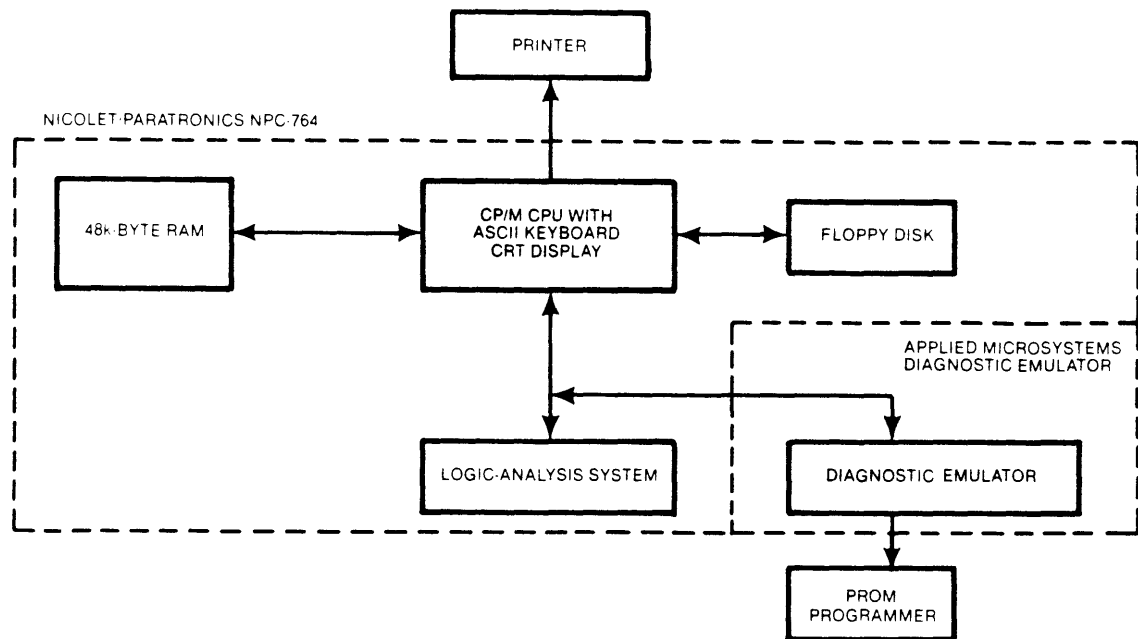


Fig 4—Built using off-the-shelf parts, this development system utilizes Applied Microsystems's EM Series Model 188 diagnostic emulator. That instrument operates in real time, allowing a user to exercise circuits via the μP bus while debugging the hardware with its built-in test routines.

number of signals that can be captured simultaneously, the length of the record-time-window frequency measurement and provision of signature analysis.

Finally, the mass storage, PROM programmer and number and type of communications ports a system needs are fairly straightforward parameters to select once you have determined which software, CPU and hardware/software tools to incorporate. These elements, combined with the design, manufacturing and service requirements, dictate the amount of peripheral support required.

You might benefit from making a detailed feature-availability grid with the foregoing parameters as row entries; designate the columns for dedicated development systems, universal development systems and systems built from individual components. Observe that systems assembled from off-the-shelf components provide many more powerful features than the individual parts of dedicated systems. And note that their cost varies widely compared with that of the dedicated systems. For instance, you can build an off-the-shelf system for less than \$8000 or as much as \$25,000; single-supplier base systems, on the other hand, vary in price from \$14,000 to \$35,000.

Ask the crucial questions

Look at the total cycle of a μP development project when evaluating system parameters. The flowchart in

Fig 2 illustrates the process necessary to complete a design. The relative importance of each project phase is unique to the design: It depends on the complexity of the hardware as well as the software.

Consider, for example, whether a design team or only one project engineer must complete the project and whether equipment will be shared for several projects or used only for one. Also determine whether the equipment will be used by the Manufacturing department or remain in the design lab. And find out where Manufacturing will obtain the test routines to check out the product after it goes into production.

Once you've dealt with these key considerations, the final selection and use of the equipment becomes straightforward because the new system is oriented specifically to a particular application.

Consider an example

Independent hardware and software can provide a development system with a high degree of flexibility—for future expansion or integration into other systems. A CP/M-based logic-analysis system and a diagnostic emulator can, for instance, combine with a larger system such as a UNIX-based network. **Fig 3** shows an example of such a network.

This combination of a CP/M-based logic-analysis system, a stand-alone in-circuit emulator and a low-cost system PROM programmer illustrates the process of

Define the problem your design project must solve

constructing your own development system as well as the results obtained in actual applications. Four factors influenced the choice of this automatic test equipment:

- The need for a universal, economical, well-supported operating system
- The need for high-speed logic-timing analysis to assist in the development and debugging of an automatic test system under design
- A transparent-emulation feature (the user did not want to build the ATE system around the constraints of the emulator)
- The ability to operate in manufacturing and service applications.

A Nicolet Paratronics NPC-764 logic-analysis system was chosen because it contains a suitable CP/M-based computer, a 48-channel logic-state analyzer with 16 trigger levels for software debugging and a separate 16-channel logic-timing analyzer with 100-MHz capability for hardware testing. It also provides a 50-MHz waveform recorder for capturing and viewing analog signals and a 100-MHz counter/timer for measuring system performance critical in the development and manufacturing of the ATE design.

To provide transparent emulation, the designers selected an Applied Microsystems EM Series Model 188 diagnostic emulator. This 8085- μ P-based unit accepts downloading of assembled code via an RS-232 port, allowing execution directly in a user's system. Because the emulator operates in real time with no Wait states inserted, the user can exercise circuits via the μ P bus while debugging the hardware with the diagnostic emulator's built-in test routines.

Test routines generated on the NPC-764 were also used to force conditions requiring timing analysis. The actual system program was then executed by the emulator in Single Step and Real Time modes to complete final testing of the entire system. The logic-analysis system and diagnostic emulator were configured as illustrated in Fig 4.

An 8085 assembler and CP/M editor served along with the hardware system. A simple software routine was written to provide downloading for the CP/M object-code files to the diagnostic emulator and uploading to retrieve the disassembler output from the emulator and display it on screen. The ATE system under development, an IEEE-488-compatible pc-board test instrument interfaced to a larger host computer, was an 8085-based system connected to an IEEE-488-interface chip and other hardware on the tester. No provisions were made for an RS-232 serial interface in the original design, but designers later found that the ability to go off line and operate the tester from a local terminal was necessary. The proposed solution was to develop a software UART, in which the 8085 manipulates an output of a spare I/O port to synthesize the

UART function in software. The solution required the development and debugging of an assembly program that could support various baud rates, word lengths and stop bits to permit the use of any of several available terminals. An 8155 I/O timer running off the processor clock was available to time the shifting of the data bits out of the I/O port.

The task of designing, debugging and documenting the RS-232 modification to the ATE system was accomplished rapidly using the NPC-764 and EM-188 system. A flowchart for the UART program was designed and a source file created, using the editor of the NPC-764's CP/M system. After assembly of the source file using the CP/M 8085 assembler, the object file was loaded into the diagnostic emulator and executed. After the code appeared to work, detailed timing measurements were made using the NPC-764's high-speed logic-analyzer section. Verification and calibration of bit times, start and stop times and word lengths were then made. Producing manufacturing documentation was easy, thanks to the program's listing, basic schematic and printouts of the analyzer setup and actual timing waveforms.

This off-the-shelf system served to complete software development, program debugging, software/hardware integration, hardware performance verification and calibration, and documentation. The system's various parts have since been used both independently and together to solve other problems. In the future, both instruments could find use, for example, as development workstations for a multiuser PDP-11-based system.

EDN

Author's biography

Sandra Reynolds is director of marketing at Applied Microsystems Corp (Kirkland, WA) and previously served as product group manager at Gould Inc's Biomation Div. She holds a BSEE degree from the University of Washington. Out of the test-and-measurement and computer markets, Sandra sees emerging microprocessor support-instrumentation systems. In her spare time, she enjoys skiing, hiking, scuba diving, painting and gardening.



Article Interest Quotient (Circle One)
High 479 Medium 480 Low 481

THE ROLE OF THE DEVELOPMENT SYSTEM, EMULATOR, AND LOGIC ANALYZER IN THE DEVELOPMENT CYCLE

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Fremont, California

Microprocessor Development Systems (MDS) coupled with Emulation Subsystems (EMS) are often thought to provide all necessary analysis functions needed during the development phase of a uP-based product. While both instruments are valuable tools, their claim to be the complete solution is inaccurate. The addition of a Logic Analyzer System (LAS), along with the traditional laboratory test instruments, results in a much more productive development environment. Each instrument, taken on its own, has identifiable uses; taken collectively, they create a productive, friendly environment in which the hardware and software engineer can develop and debug both the hardware and software.

Figure 1 illustrates a stylized uP based target product and illustrates possible analysis linkages to the collective instrumentation. Figure 2 provides a flow chart of the development process and identifies the instrument best used at each step. Figure 3 illustrates a stand-alone emulator (Applied Micro), Figure 4 shows a full MDS (Futuredata) and a logic analyzer (NPC-764) is presented in Figure 5. A specific example, Figure 6, is discussed to illustrate the techniques used at each development step.

The Instruments Described

What is an MDS? It is a computer system, Figure 4, combined with a collection of cross software designed to support the development of programs for the target uP product. It may be as big as an Amdahl mainframe or as small as a personal computer. It is primarily used for software development, including the editing, compilation, assembly and linkage of programs targeted at the system being developed. The MDS may be linked to a parallel or serial port of the target system and may have a download program capable of loading the target system's RAM for execution. It may likewise be linked to a PROM programmer with the ability to download programs for later insertion into the target system's memory. Finally, it may be linked to an Emulator—loosely via a serial port or tightly via an integrated bus or network. In this environment, it has the capability of loading the Emulation memory or through the Emulator, the target memory. It also has the capability of interaction with the Emulator to facilitate setup, data collection and display of related information.

The Emulator Subsystem, Figure 3, is generally a computer-based instrument specifically programmed to facilitate the setup and control of the emulation process. The EMS is plugged directly into the target system in place of the uP it is emulating. There is an identical uP in the EMS which assumes active control of the target system through its uP socket. The EMS also contains RAM capable of being mapped over all or portions of the target product's memory. It contains debug logic capable of breakpointing (halting) the program execution of the target system based on a simple to complex sequence of events which can be monitored at the target's uP socket. It has the ability to monitor, qualify and trace (i.e., record in an integral trace memory) events which occur at the target's internal bus. When the target uP is halted, the EMS provides a window into its memory and into the internal registers within the uP chip. It may be used to single step a target program, to multi-step at a controlled rate, or to execute at full speed.

The MDS/EMS combination adds software in the MDS to simplify the setup, data collection and data display for analysis of the target system's behavior. Software executing at the target's uP socket can stimulate the target. The EMS can monitor the local bus activity and can be setup to breakpoint on a given condition following which the MDS can recover the state of the uP's internal registers and display them for analysis; the program can be quickly changed and the process recycled. Likewise the EMS can monitor and collect activity at the target uP's pins--the local bus. This data may be qualified and saved in trace RAM and may later be displayed and analyzed from the MDS. During early program development, the EMS can execute programs even prior to the completion of the target system hardware; thus, programs may be partially debugged without a physical connection and in parallel with hardware development.

The Logic Analyzer System, Figure 5, is also a processor-based instrument programmed to monitor and collect digital signals over time. It contains internal logic to monitor sequences of events and to capture data in RAM for subsequent display and analysis. Unlike the EMS, the Logic Analyzer is a passive instrument. It does not modify the target system's behavior, but does enable observation of that behavior at virtually any set of points. The LAS usually has a wide collection and display capability: 16, 32 or 48 channels or more. It can monitor activity on the uP chip pins. With the addition of a dedicated probe and some special software, it can display the uP's behavior in a disassembled form, similar to the information collected and displayed by an MDS/EMS instrument. The LAS, however, can also monitor activity at points far removed from the local bus. It can capture data using the target system's timing clocks (synchronous to the uP operation) or it can capture data using an internal clock (asynchronous to the uP operation). The data can be displayed in a state format, logically grouped to simplify analysis, or in a timing diagram format. The collection can be set up to capture signal glitches (data transitions between clocks). To aid in identifying an intermittent problem, a collection can be made repetitively and compared to a stored reference until they differ--the differences can then be displayed to pinpoint the problem area.

As demonstrated above, each instrument has its logical place in the development cycle; the MDS for software development, the MDS/EMS combination for software development and hardware analysis, the LAS for software and hardware analysis and the combination of all three for complete product development and test analysis.

The Right Tool Yields Results

Figure 6 illustrates a target system which is packaged in two separate boxes; e.g., a disk subsystem coupled to a uP subsystem. For the purpose of this example, assume that the coupled system is the new product to be tested. The hardware problem is to develop the interface mechanism and cable used to couple the two boxes and to develop the control logic for the new target subsystem. The software problem is to develop the control algorithm to monitor the peripheral, to control its function and to pass data. This software must then be integrated into the larger system software environment so that the peripheral can be used as a system component.

During the specification and design phase, the hardware and software considerations can proceed in parallel. Both can be fabricated in parallel (program fabrication is generally called coding). Using the MDS, the software team member can develop clean code designed to accomplish the specified task. Using the MDS/EMS combination, the software team member can assure that the program is in fact outputting controls and data in the prescribed sequence. In a similar manner, the software's response to status and data inputs can be verified.

When the logic breadboard is fabricated, the hardware team member can begin to use the MDS/EMS/LAS to assure proper hardware behavior. This is typically begun by developing simple exercise loops using the MDS/EMS debugger capability. To stimulate the outputs, the hardware engineer must program a sequence of commands and data to exercise each mode of operation in the hardware. The resultant inputs can be monitored to assure correct response to each stimulus. To isolate faults in the design or fabrication phase, the engineer can use the LAS to assure that the outputs arrive at the target system as expected and that the various circuits respond and behave correctly and in the proper time sequence. Status and inputs can likewise be monitored to assure that they are presented to the uP subsystem correctly. The LAS closes the analysis loop by truly allowing the engineer to visualize and document the interaction of logic signals throughout the circuit. Timing problems, control sequence problems and race conditions can all be quickly detected using the LAS.

When the logic breadboard is working to the satisfaction of the hardware engineer, the software engineer joins the test activity to integrate the control software with the hardware. For the first time, the software will be executing in its target environment. The software and hardware engineers use the analysis tools to resolve their misunderstandings and to solve any new problems which may be detected in this environment.

The development process is completed when the control software and the prototype hardware are integrated into the operational system including the uP and its system software. It is typically at this point that an infrequent problem is detected. For example, once every day or two, the peripheral loses data or generates a ghost interrupt. Where is the real problem? Is it in the hardware or software? The answer of course is a qualified yes to both and the MDS/EMS/LAS combination are put to work to isolate the cause of the symptom. It is also not infrequent that the intermittent problem is first encountered by a customer, requiring that engineering must somehow contrive to duplicate the symptom prior to isolating the cause. The MDS/EMS tool is used to explore possibilities toward this goal. The LAS is then set up to capture data when the exception occurs. In combination, these tools help the engineering team isolate and solve the real problem regardless of its cause.

The LAS, supplemented by a graphics type printer, can be used to generate timing and state diagrams for engineering, production test and field service documentation. Instrumentation setups and collections can also be saved on disk so that consistent results can be observed either by engineering to qualify hardware and software changes or by production or field service test to qualify the system's behavior.

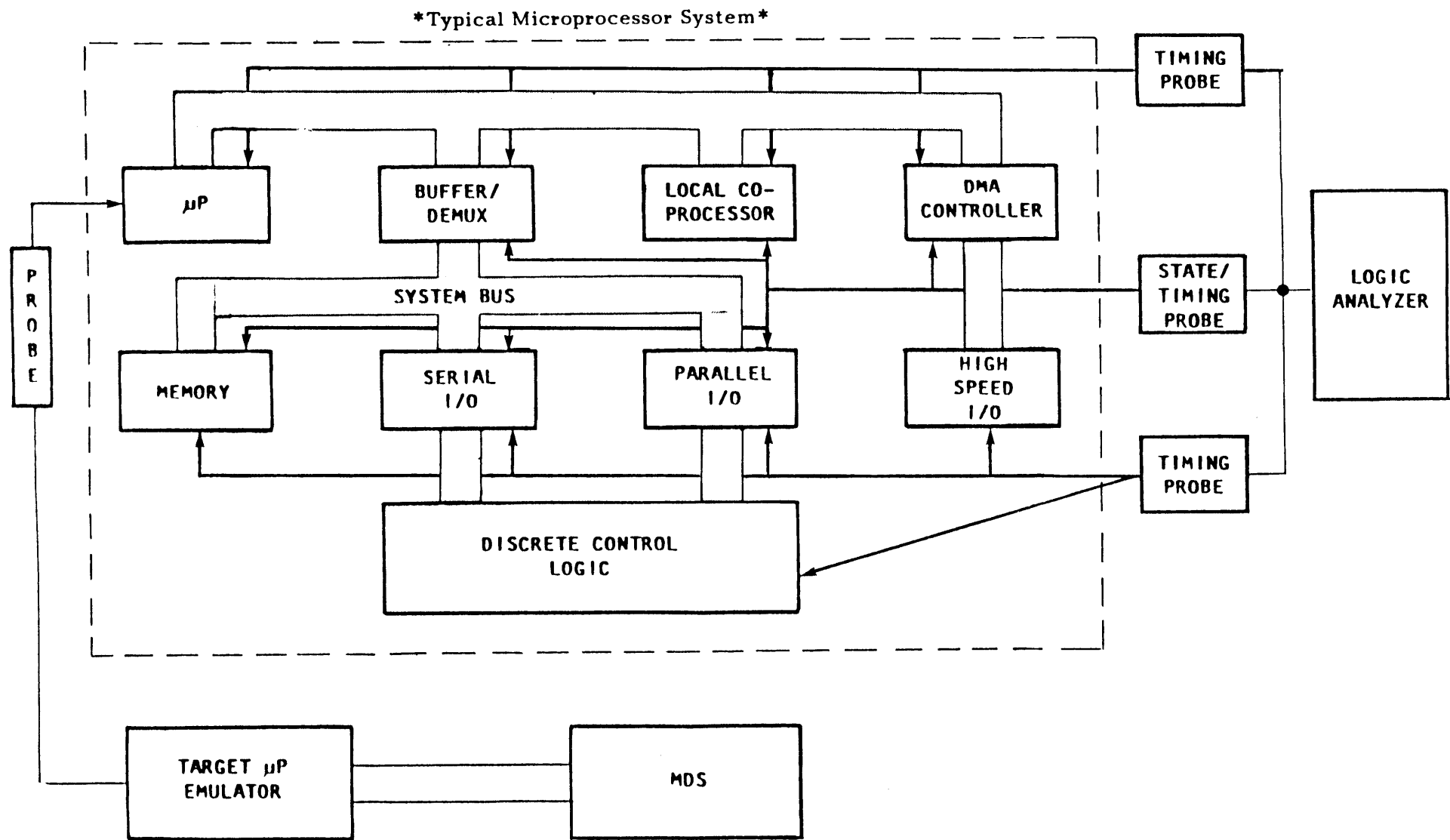


Figure 1. Typical uP System with MDS, Emulator and Logic Analyzer

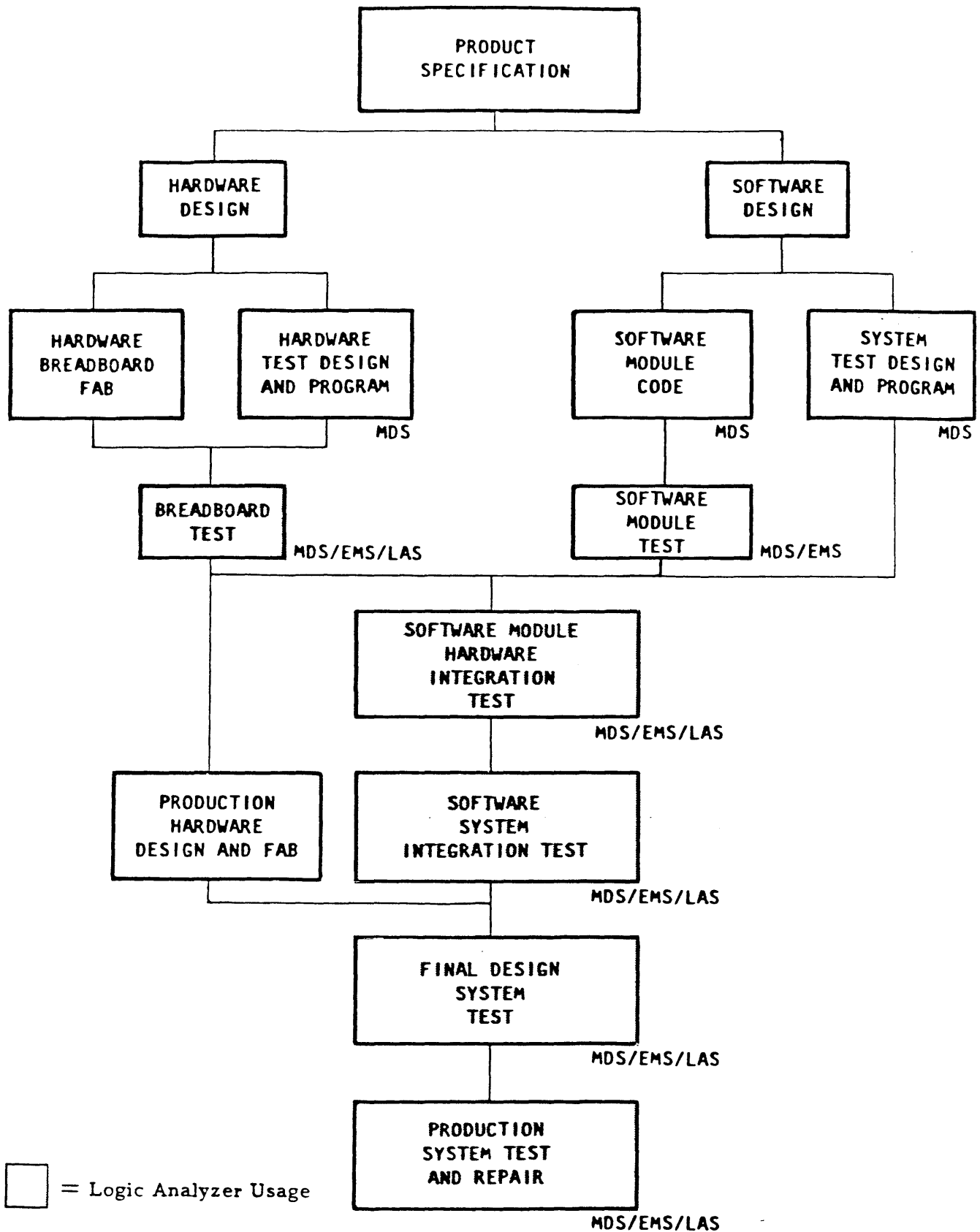


Figure 2. Product Development Cycle.

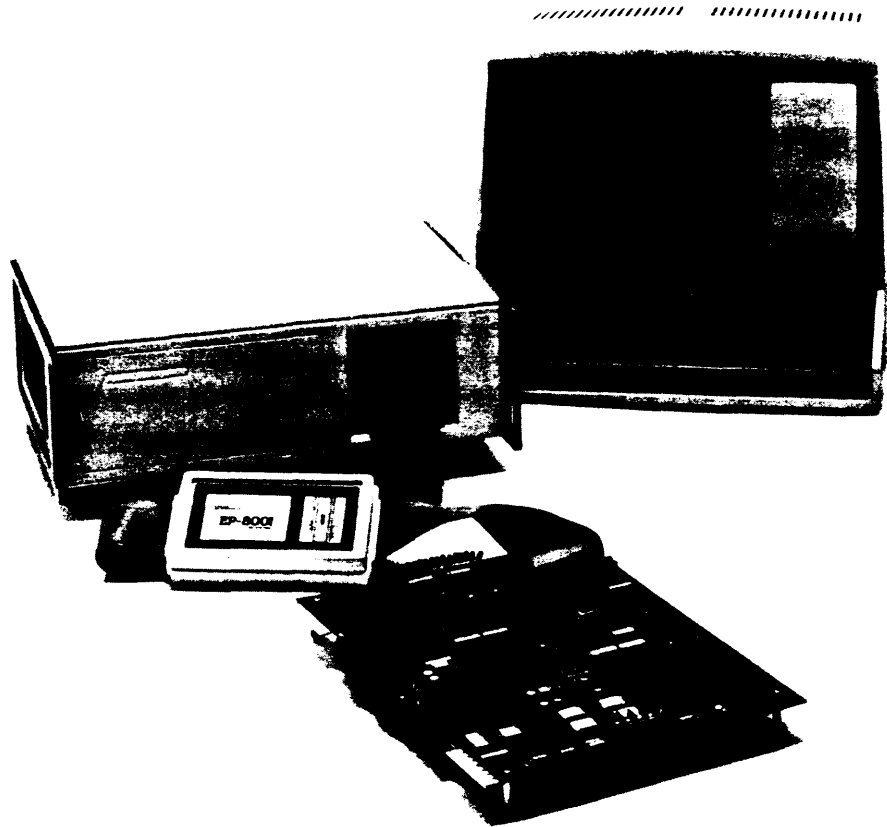


Figure 3. "Applied Microsystems' new Satellite Emulator upgrades existing development systems, enhances hardware/software integration for computer-developed software and operates as a standalone-debug-station when linked to a CRT Terminal."

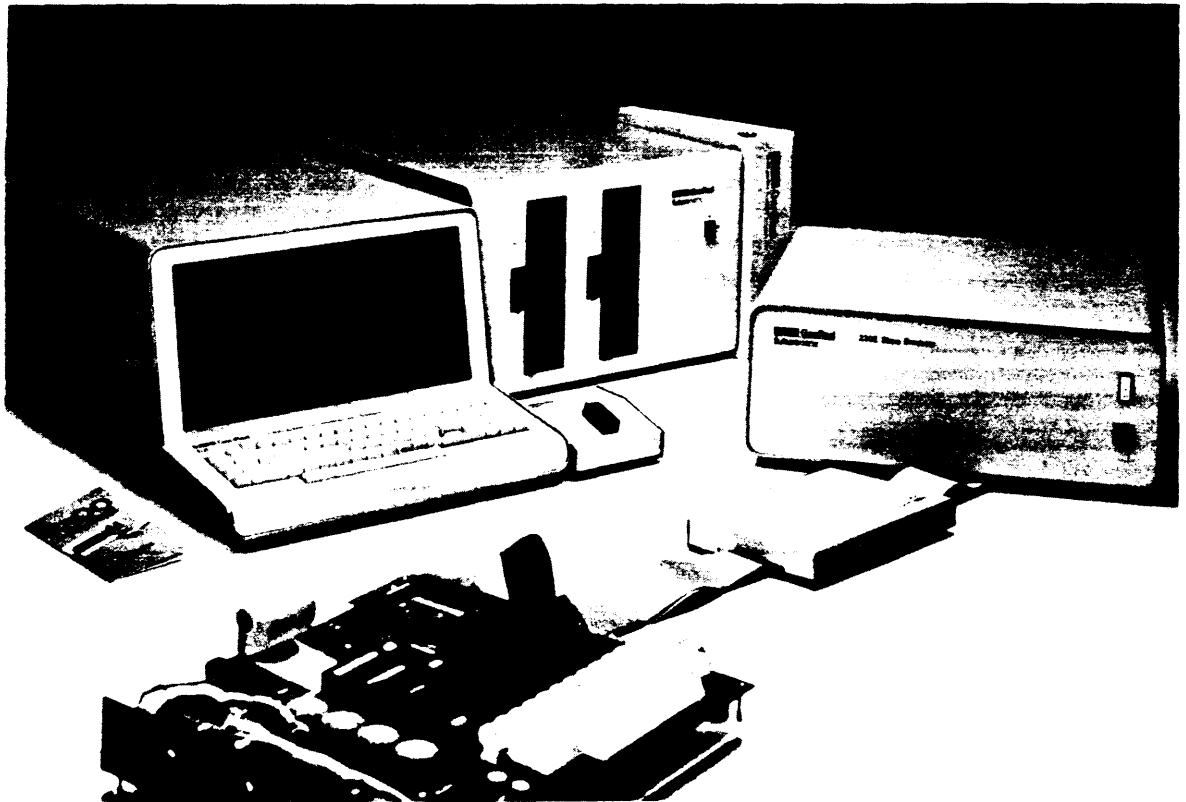


Figure 4. Futuredata Development System.



Figure 5. Nicolet-Paratronics (NPC-764).

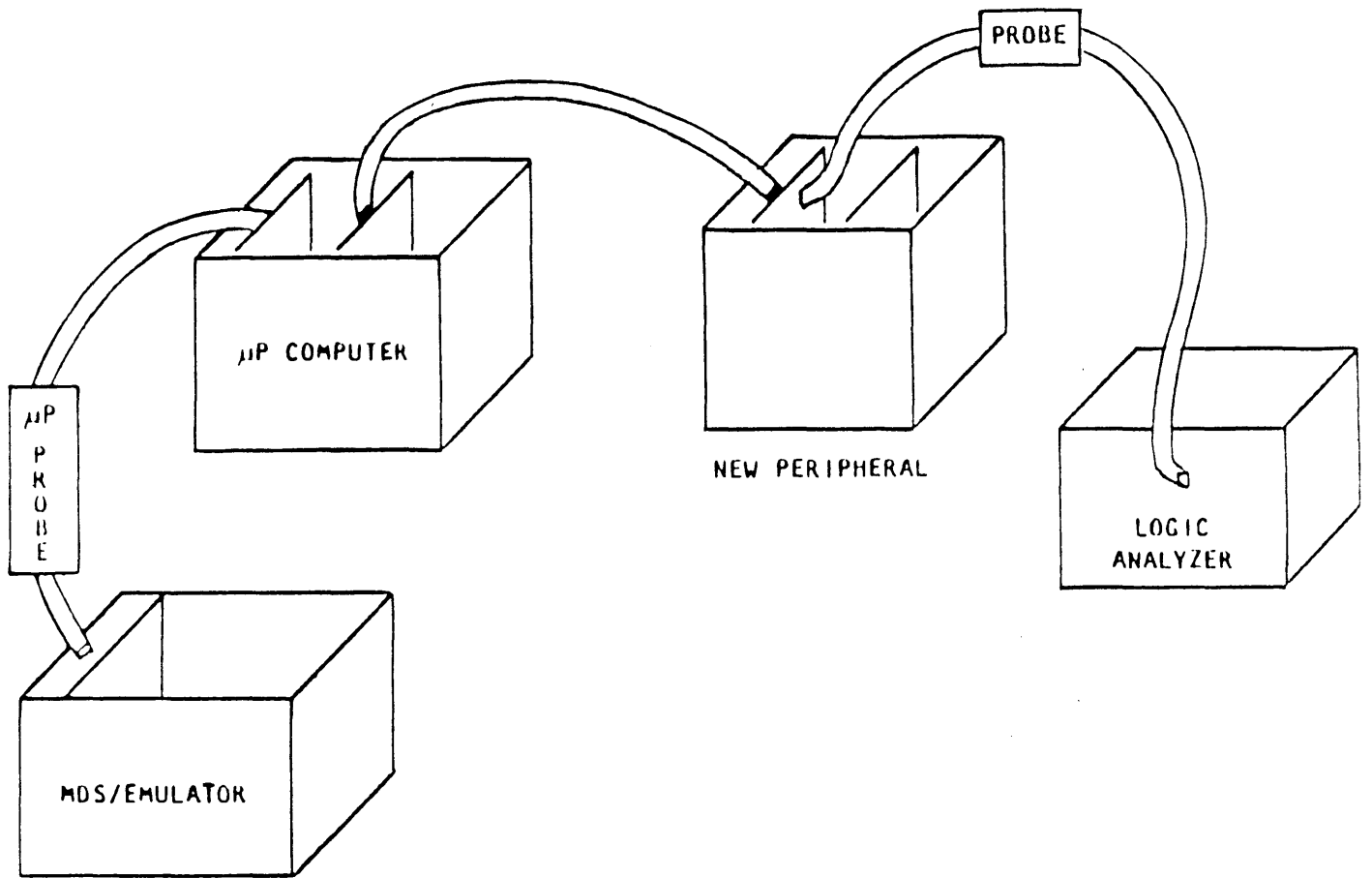


Figure 6. Engineer Test Setup - New Peripheral.