Digital Equipment Corporation
Maynard, Massachusetts

digital

decsystem10

Maintenance Manual

DF10
DATA CHANNEL

DEC-10-HDFC-D

decsystem10

DF10 DATA CHANNEL MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Printing July 1968
2nd Printing (Rev) February 1970
3rd Printing (Rev) September 1971

The following are trademarks of Digital Equipment Corporation, Maynard, Massachusetts:

DEC	PDP
FLIP CHIP	FOCAL
DIGITAL	COMPUTER LAB

CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

TABLES

CHAPTER 1
INTRODUCTION

This manual together with the referenced documents provides information relevant to the installation, operation, and maintenance of the DF10 Data Channel. The level of discussion assumes a general familiarity with the decsystem10. The DF10 is a high-speed transfer device (10^6 words per second) that accomplishes direct data transfers between I/O devices such as the disk, drum, disk pack, magnetic tape, and certain real-time devices, and the PDP-10 memory. Using the DF10, only a single device may communicate at one time. Communication is initiated by the I/O device on a first-come-first-serve basis. Once enabled, the DF10 functions as an I/O processor and transfers data independently of the program in progress, thereby releasing the central processor for other operations. The program establishes the initial link when it activates the I/O device which then requests access and conditions the data channel to allow data transfer when access is granted. Volume II of this manual contains the Engineering Drawing Set for the DF10 Data Channel.

1.1 GENERAL DESCRIPTION

The DF10 is housed in a standard DEC 19-in. cabinet (Type CAB-9B) of welded steel frame construction with sheet aluminum covering (Figure 1-1).

Access doors(mounted on the cabinet front and rear) are held closed by magnetic latches. The Type 844 Power Control and Type 728 dc Power Supplies are mounted inside the rear access door on a plenum door that is latched at the top by a spring loaded pin. Module mounting racks are located behind the front access door as are the switch panels. The rear plenum door is used to gain access to the modules for removal and replacement.

A fan at the bottom of the cabinet draws cooling air into the unit through a dust filter, and a fan assembly in the logic rack forces the filtered air over the modules. Exhaust takes place through the top of the cabinet.

Two Type 728 Power Supplies (60 Hz), or Type 728A (50 Hz), furnish dc power. Power is controlled by a Type 844 Power Control Unit which contains a 30A line circuit breaker to protect the channel from overloads.

If an MX10 Memory Data Multiplexor is included in the system, it may be housed within the DF10 cabinet. The multiplexor is furnished dc power by the DF10.

1.1.1 Specifications

Table 1-1 lists the specifications for the DF10. Cabling information is contained in Chapter 2.

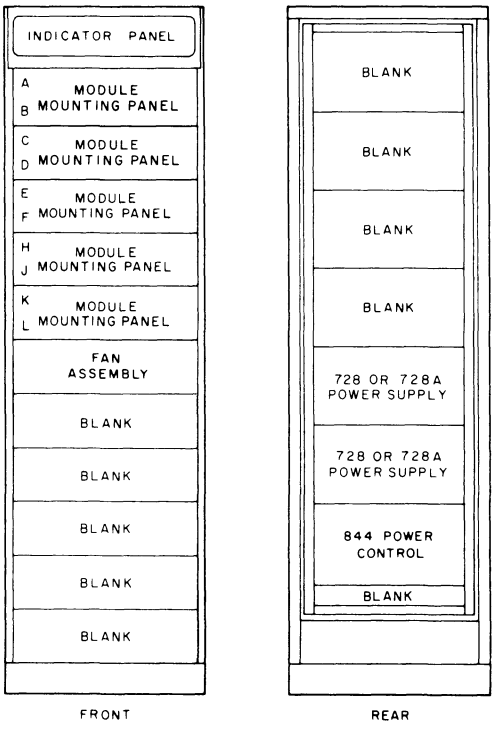


Figure 1-1 DF10 Data Channel, Assembly Locations

Table 1-1
Specifications

Characteristic	Specification
Input Power (ac)	115 Vac ± 10%, 60 Hz ±2 Hz, single phase 230 Vac ± 10%, 50 Hz ±2 Hz, single phase (The equipment will operate with either of the indicated combinations if appropriate Type 728 Power Supplies are installed and internal control connections made.)
Line Current (Steady State at 115 Vac)	5.0A (Surge: 12.0A)
Power Dissipation	550W
Power Interrupt	Up to 25 ms with no effect on operation
Internal Power Supply Potentials	+10 Vdc, -15 Vdc
Transfer Rate	10^6 words per second (maximum)
Thermal Dissipation	1900 Btu/Hr
Operating Temperature	15°C to 35°C 60°F to 95°F
Storage Temperature	5°C to 45°C 40°F to 110°F

Table 1-1 (Cont)
Specifications

Characteristic	Specification		
Relative Humidity	20% to 80%		
Dimensions	Height	Width	Depth
	69 in. 1.75m	22 in. 0.54m	29 in. 0.72m
Weight	450 lbs, 200 kg		

1.1.2 System Interface

Figure 1-2 and 1-3 illustrate the DF10 interface and a hypothetical system configuration respectively. Cable termination locations for the DF10 and other system components are discussed in Chapter 2.

The DF10 is connected to the core memory via the PDP-10 memory bus; or the multiplexor bus if an MX10 Memory Data Multiplexor is included in the system. Connection to the associated I/O device is effected over the channel bus. An MPX control cable is also required if the MX10 is used. These cables are described in Chapter 2.

1.1.3 Logic Sections

The DF10 Contains the following major logic sections:

Data Channel Control A (CCA)	Data Address Register (CDA)
Data Channel Control B (CCB)	Word Count Register (WCR)
Data Channel Control C (CCC)	Address Drivers (CAD)
Initial Address Register (CIA)	Memory Buffer Left (MBL)
Control Word Address Register (CCW)	Memory Buffer Right (MBR)

Data Channel Parity Generator (CPG)

The CCA, CCB, and CCC logic receives and transmits the control signals from and to the I/O device and the memory unit. The 8-bit address of the initial control word is stored in the CIA when the I/O device first gains access to the channel. The CCW is a 18-bit register which holds the memory address for the next transfer and is an up counter; however, no carry propogates beyond the most significant bit. The WCR is an 18-bit register which hold the two's complement of the high order 18 bits of the control word; this is also an up counter. Carries beyond bit zero are lost.

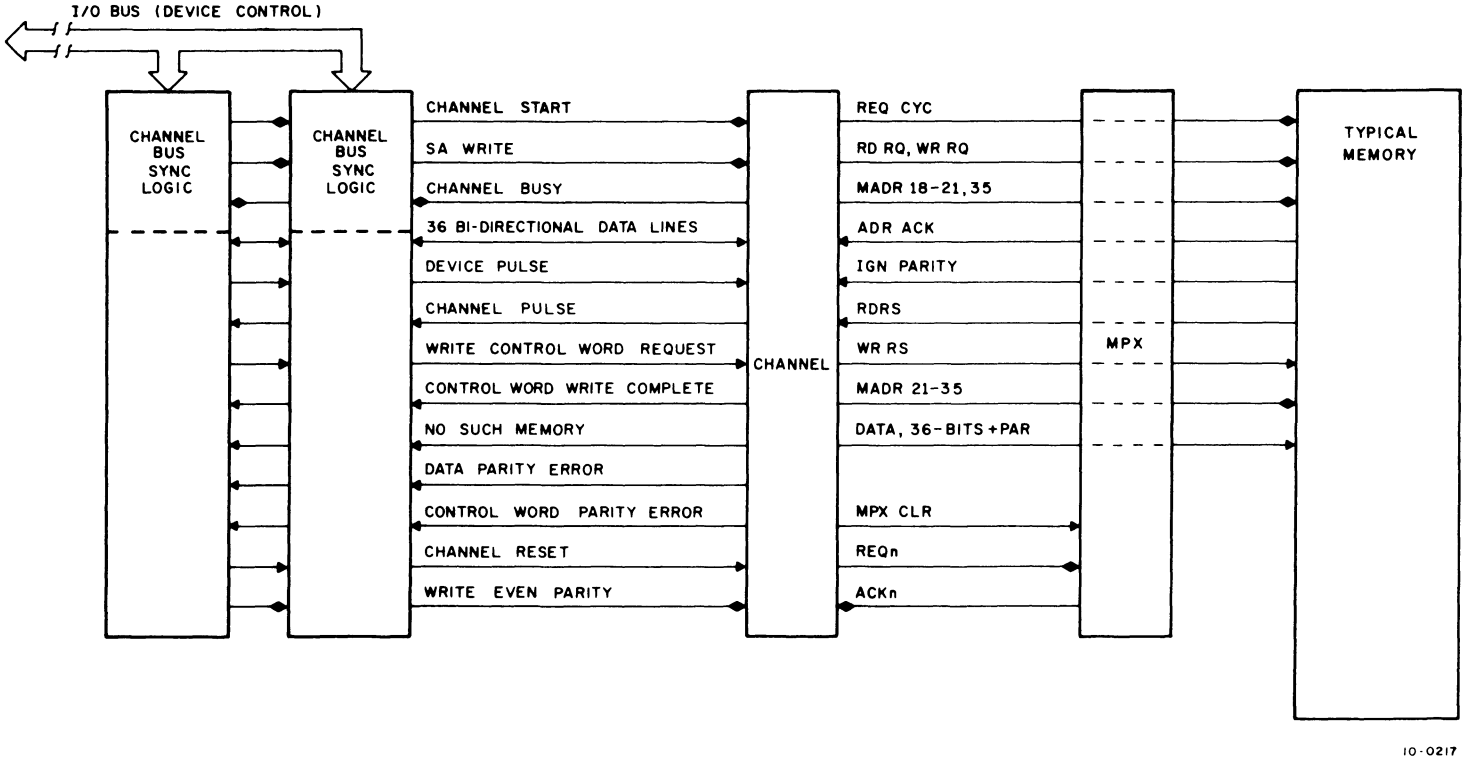


Figure 1-2 DF10 Interface

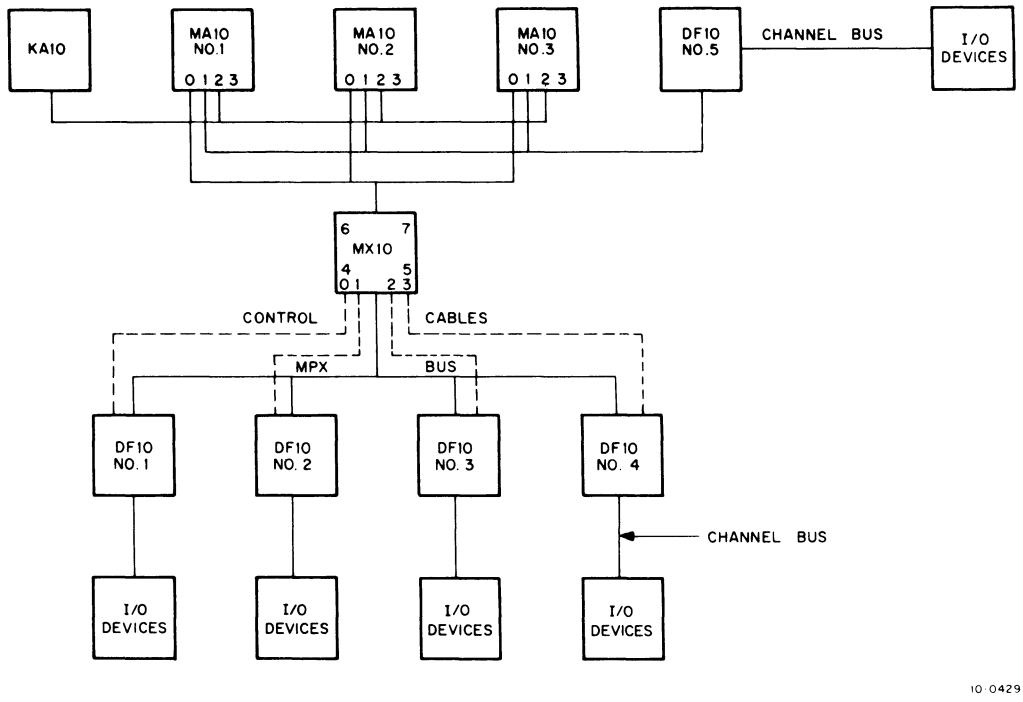


Figure 1-3 Hypothetical System Configuration

The address drivers transmit the memory address information to the memory over the MADR lines. Data read from core or to be written into core are stored in the MBL (bits 00 through 17) and MBR (bits 18 through 35). Odd parity for each data word is generated in the CPG logic. Even parity may be generated under program control but can be locked out by means of a DF10 switch setting.

1.1.4 Reference Documents

The following documents contain information which supplements that contained in this manual:

PDP-10 System Reference Manual
KA10 Central Processor Maintenance Manual
PDP-10 Site Preparation Manual
PDP-10 Interface Manual
MX10 Memory Data Multiplexor Maintenance Manual
MA10 Core Memory Maintenance Manual
MB10 Core Memory Maintenance Manual
ME10 Core Memory Maintenance Manual
DF10 Engineering Drawing Set

This material is available from the nearest DEC Field Office or from:

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

1.1.5 Engineering Drawings

Reduced size copies of pertinent DF10 Engineering Drawings are contained in Volume II of this manual.

CHAPTER 2
INSTALLATION

This section in conjunction with the PDP-10 System Site Preparation Guide and the applicable DF10 Engineering Drawings provides information relevant to DF10 installation. Installation information regarding other system components may be found in the individual equipment technical manuals.

2.1 INSTALLATION INSTRUCTIONS

2.1.1 Unpacking

Remove all crating and packing materials; being careful not to damage the equipment. Determine that all modules are correctly seated and repair any mechanical damage.

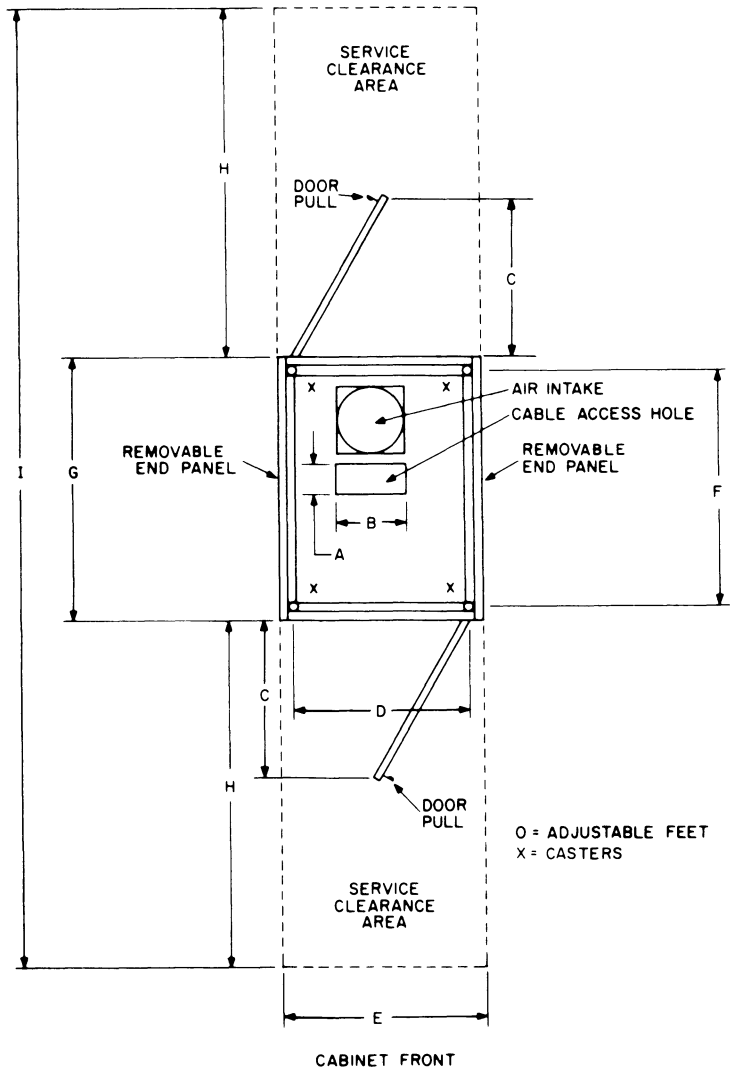
2.1.2 Site and Space Requirements

There are no special site requirements other than those dictated by environmental conditions (Table 1-1) and service clearances (Figure 2-1). Subflooring is not normally required. The units are free standing and may be bolted to the cabinet of an associated I/O device.

2.1.3 Cables

All cables entering or leaving the data channel cabinet do so through access cutouts under the bottom left and right sides, respectively. Figure 2-2 is a cable interconnection diagram illustrating the cable termination locations within the DF10 and the common system components. Figure 2-3 shows the channel interconnections.

2.1.3.1 Memory Bus - A DF10 connected directly to the memory bus (no MX10 Multiplexor) is associated with one particular memory port, normally that possessing the highest priority (P0). The connection is accomplished by two coaxial cable assemblies terminated in Type W851 connectors. The memory bus output connectors must be terminated through 100 Ω resistors using four Type G703 or eight G700 terminators. Maximum allowable physical length of the memory bus is approximately 100 ft (see the PDP-10 Interface Manual for detailed information) which includes wire runs through each memory unit. The memory bus is a part of the memory unit.



DIMENSIONS	A	B	C	D	E	F	G	H	I
INCHES	3.50	7.00	19.00	19.30	22.00	26.00	29.00	36.00	100
METERS	0.10	0.20	0.48	0.49	0.54	0.65	0.72	0.91	2.50

10-0147

Figure 2-1 Service Clearances for DF10

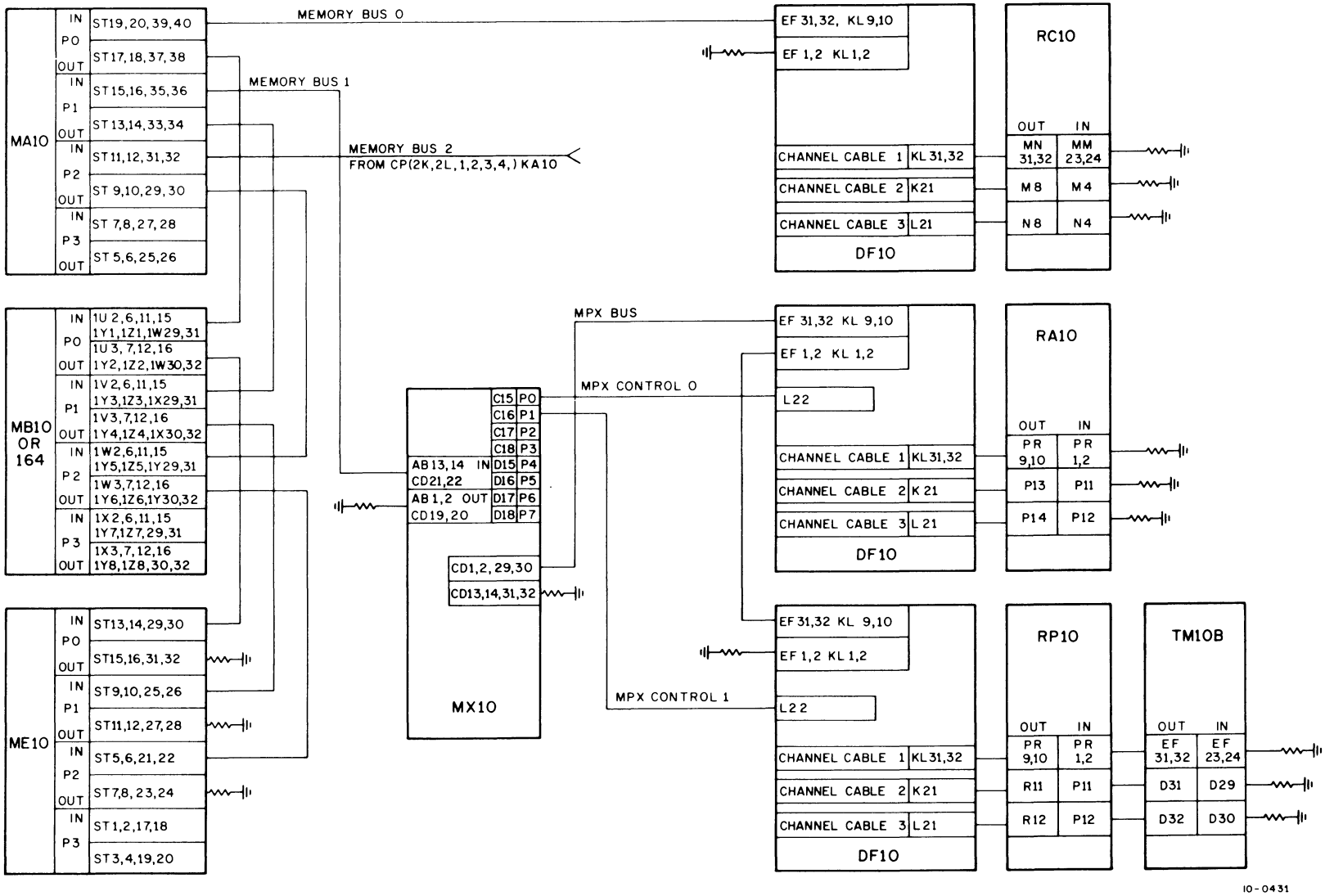


Figure 2-2 System Interconnections*

*The in-out designations for the Memory Bus, MPX Bus, and Channel Cable #1 are arbitrary, as these are bi-directional lines; connection may therefore be made through either the in or out connectors, whichever is more convenient. Also, the resistor terminations shown at the end of the Memory and MPX Busses and the channel cables are type G700 (single height) or TYPE G703 (double height) 100Ω terminator modules.

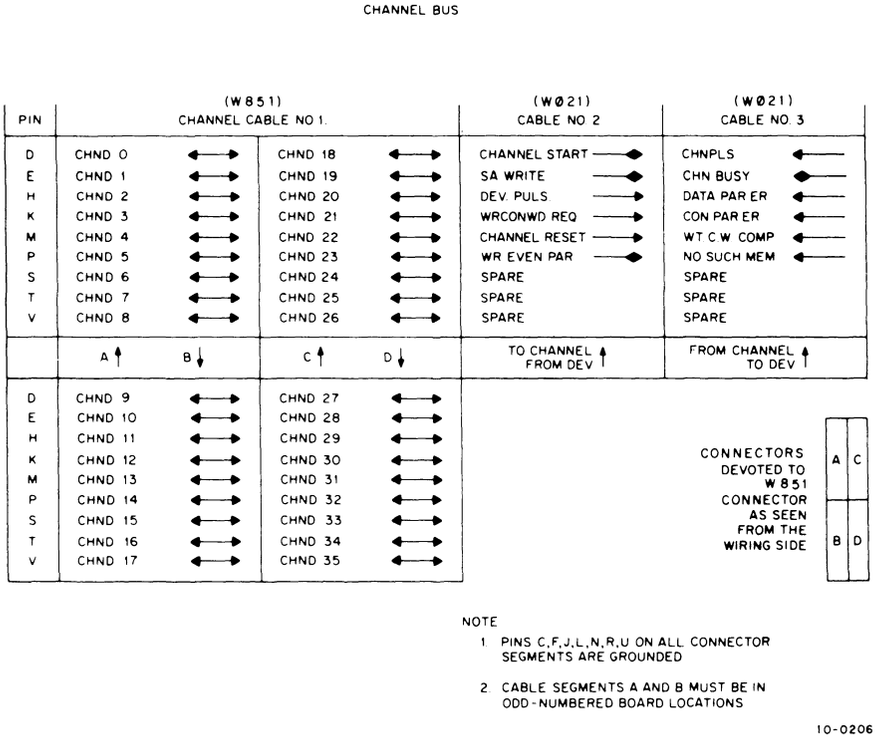


Figure 2-3 Channel Interconnections

If a DF10 is being added to a PDP-10 System containing MA10 and/or ME10 memory units, an MC10 option is required for activating an additional memory unit port in each memory unit in the system. The 187 option applies to Type 164 and MB10 memory units.

2.1.3.2 Multiplexor Bus - If the DF10 is associated with the MX10 Memory Data Multiplexor, the MPX bus is used to convey data between the DF10 and the MX10 (therefore, to the memory bus). An MPX control cable terminated in W021 connectors at both ends is also required between the MX10 and each DF10. The MPX bus is identical to the memory bus and consists of two coaxial cable sets. Each MPX control cable must be terminated through 100Ω ±10% resistors. The maximum length of the MPX bus and memory bus combined is nominally 100 ft which includes the lengths of wire runs through each DF10 and a 30 ns delay equivalent to 20 ft through the MX10. Actual length of the bus is dependent upon the MX10s location in the system with respect to the memory unit and MPX bus. For additional information refer to Chapter 7 of the PDP-10 Interface Manual.

2.1.3.3 Channel Cables - Three channel cables are required for connection between the DF10 and its associated I/O device system. Channel cable #1 is identical to the memory and MPX bus cables consisting of

two coaxial cable assemblies terminated in Type W851 connectors. Channel cables #2 and #3 have six conductors and are terminated at both ends in Type W021 connectors. Each channel cable must be terminated through 100Ω ±10% resistors connected to the last device on the channel bus.

CHAPTER 3

OPERATION

This chapter contains a general description of channel operation together with a listing of the switches and indicator functions.

3.1 INDICATORS AND SWITCHES

3.1.1 Indicator Panel

Table 3-1 lists the meanings of the various indicators when each is illuminated. Most of the indicators change state too rapidly to be meaningful when the channel is operating normally; however, they are extremely valuable as maintenance aids, especially while operating in the local mode.

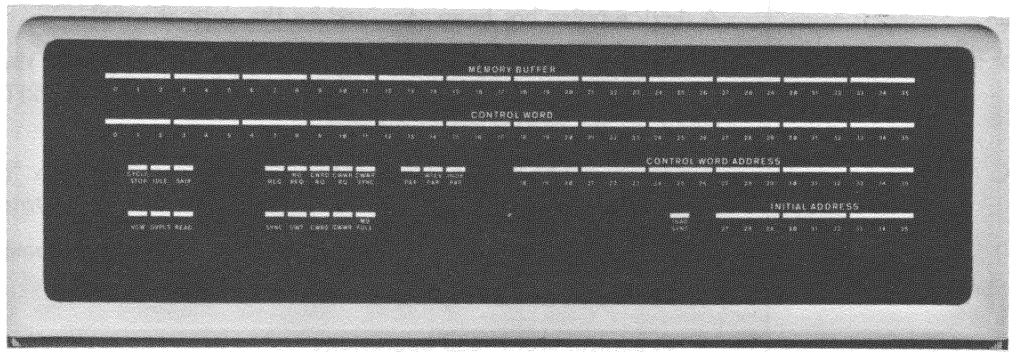


Figure 3-1 DF10 Indicator Panel

Table 3-1
DF10 Indicators

Indicator	Function
MEMORY BUFFER (Indicators 0-35)	Indicates the content of the Memory Buffer Register, bits 0 through 35.
CONTROL WORD (Indicators 0-35)	Indicates the content of the Control Word Register, bits 0 through 35.
CONTROL WORD ADDRESS (Indicators 18-35)	Indicates the content of the Control Word Address Register, bits 18 through 35.

Table 3-1 (Cont)
DF10 Indicators

Indicator	Function
INITIAL ADDRESS (Indicators 27-35)	Indicates the content of the Initial Address Register, bits 27 through 35.
CYCLE STOP	The data channel is ready to terminate operations.
IDLE	The data channel is in an idle state.
SKIP	The control word fetched has a zero data address field.
REQ	A request cycle signal has been sent to memory if the NO REQ indicator is off.
NO REQ	The request cycle signal is being suppressed.
CWRD RQ	A control word read request has been initiated.
CWWR RQ	A control word write request has been initiated.
CWWR SYNC	A control word write request is being held until required by the normal control sequence.
PAR	A parity bit has been received from memory.
WTEV PAR	Data transfers to memory have even parity.
INOR PAR	The channel is ignoring the parity bit (bit 37) of data words read from memory.
VCW	The control word is valid (non-zero word count).
DVPLS	A device pulse has been received by the data channel.
READ	The channel is performing a data transfer into memory and the device connected to the channel has not generated a SAWRITE signal at the beginning of the cycle.
SYNC	A memory cycle has been initiated. The indicator remains "on" until all memory control flip-flops return to their normal states.
	These lights indicate the processing of data to and from memory.
DWT	A data word memory transfer.
CWRD	A control word read operation.
CWWR	A control word write operation.
MB FULL	The memory buffer is loaded.
(INAD SYNC)	The INAD SYNC flip-flop is set locking the initial control word address into the Initial Address Register (INAD 27-34).

3.1.2 Power Control

The Type 844 Power Control is shown in Figure 3-2. Main power controls for the DF10 are situated on the DEC Type 844 Power Control Panel located on the lowest position of the plenum door and accessible with the rear door open. Provided are a 30A ganged toggle type circuit breaker, a LOCAL-OFF-REMOTE toggle switch, and a neon power ON indicator. The circuit breaker removes all power from the memory unit when placed in the OFF position or when tripped as a result of excessive line current. The LOCAL-OFF-REMOTE switch in the REMOTE position allows power to be turned on and off with the PDP-10 system from the central processor. In the OFF position the switch removes all power from the channel power supplies; and, in the LOCAL position applies power to the channel independent of the central processor.

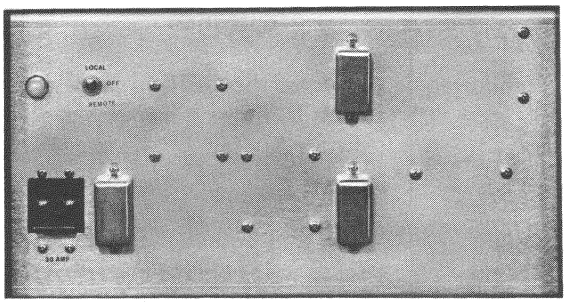


Figure 3-2 Type 844 Power Control

3.1.3 Switch Panels

Table 3-2 lists the DF10 switches with brief functional descriptions. These switches are shown in Figures 3-3 through 3-5.

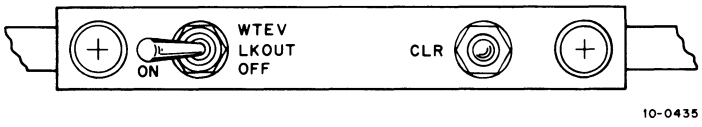


Figure 3-3 Switch Panel No. 1

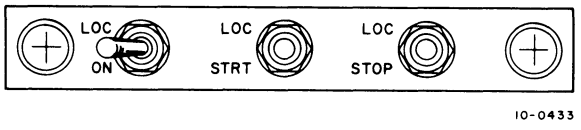


Figure 3-4 Switch Panel No. 2

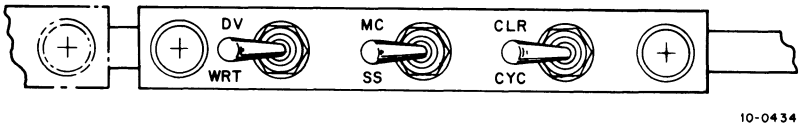


Figure 3-5 Switch Panel No. 3

Table 3-2
DF10 Switches

Switch	Type	Function
WTEV LKOUT	Toggle	When ON prevents even parity from being written into memory. When OFF allows even parity to be written into memory.
CLR	Pushbutton	Clears the channel control.
LOC	Toggle	When ON enables the Local mode circuitry and locks out channel bus signals which are then developed internally for test purposes. CAUTION This switch must be OFF for normal on-line operation.
LOC STRT	Pushbutton	Activates the DF10 in local mode. If single-stepping, this switch initiates a memory cycle.
LOC STOP	Pushbutton	In local mode, stops DF10 operation upon completion of the current cycle.
DV WRT	Toggle	When ON causes the local mode circuitry to simulate a device write operation; when OFF causes local mode simulation of a device read cycle.
MC SS	Toggle	When ON causes the DF10 to stop upon completion of a local mode memory cycle.
CLR CYC	Toggle	When ON enables a 300 μs delay when the channel is started in local mode. Upon timing out of the delay, the channel is automatically cleared. CAUTION This switch should be ON only when the channel is hanging up as the result of a malfunction and cannot be started normally without first clearing. If ON during other instances, the memory may hang or a normal operation may be suspended prematurely.

3.2 OPERATIONAL DESCRIPTION

This section contains an operational description of DF10 operation relating to the Block Diagram (Figure 3-6). Also included are descriptions of the control word and typical programming examples.

Initialization of the DF10 is accomplished by the controller (synchronizer/adapter) associated with the device requiring service on a first-come-first-served basis. Included in the control word transmitted to the channel from the requesting device is the address of the first command in memory to be executed. This command is fetched and executed.

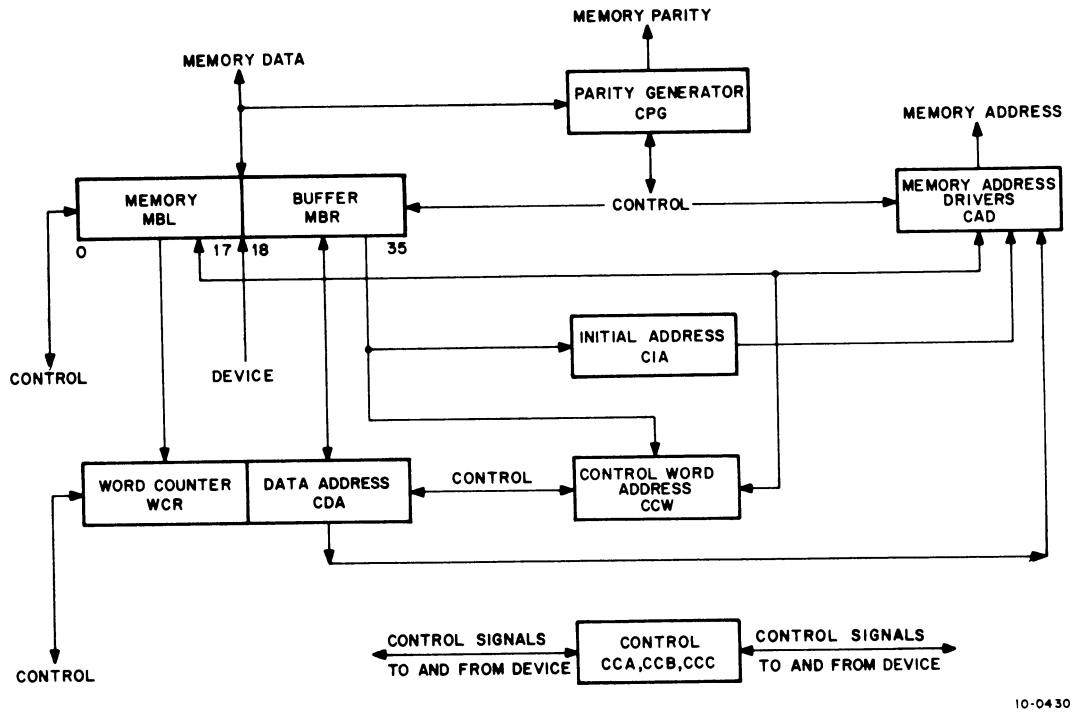


Figure 3-6 DF10 Block Diagram

If the left 18 bits of the command word contain a word count, and an address other than all 0s is continued in the right 18 bits, the number of words specified will be transferred by the channel to or from memory starting at the specified address. Upon completion of the transfer of each word, the word count register and the address register are incremented. When the word count register goes to all 1s, signifying the completion of the transfer, the next sequential command word is fetched from memory and executed.

A command word containing all 0s in the left half and an address in the right half is interpreted as a pointer to the next list of command words in memory. In this instance the next command word is fetched from that location. No data is transferred; this capability allows the chaining of noncontiguous command strings, in addition to the chaining of noncontiguous data blocks.

For a command word processed during a device read operation that contains a word count but has 0s in the address portion (an address equal to 0), the channel reads from the device the number of words specified by the word count. The data is not stored in memory. This feature is useful for skipping unwanted information on sequentially oriented data devices such as magnetic tape.

A command word containing all 0s is interpreted as a "stop" command. The controller which has access is signalled and it or another controller on the bus may re-initialize the channel and start a new data transfer sequence.

Once a device has gained access to the channel, no other device may interrupt until its entire string of command words is executed.

3.2.1 Control Word Format

During the initializing phase, the I/O device which has gained access to the data channel sends the initial control word address to the data channel. The control word is fetched from memory and evaluated to determine the ensuing operation. The format of the control word contains the data address (DA) and the word count (WC) of the data transfer as shown below. It is the WC and DA position of the control word that is evaluated. The format of the control word has the following meaning:

Table 3-3
Control Word Format

WC	DA	Function
= 0	= 0	Terminate the data channel operation with the I/O device. Set CHANNEL BUSY = 0 and IDLE = 1.
= 0	≠ 0	DA is set to the control word address register and a new control word is fetched from that location in memory.
≠ 0	= 0	If SAWRITE is not asserted (writing memory), the channel will receive the number of words specified by WC from the device, but will not put them into memory. This feature is useful for tape and disk applications (see examples).
		If SAWRITE is asserted (reading memory) the channel will receive the number of words specified by WC from memory commencing at address 0.
≠ 0	≠ 0	Transfer the number of words indicated by WC. Transfer the first word into or from the address specified by DA+1. After each transfer, increment the DA register by 1 and transfer the next word to or from the incremented address.

If the evaluation of the control word specifies a data transfer, the DA and WC are stored in their respective registers. The DA is incremented before the first transfer.

The initial control word address, B, an even number, is supplied by the device. Immediately upon receiving the CHANNEL BUSY signal from the channel, the device should send 8 bits of initial address (bits 27 through 34) and the DEVICE PULSE on the data bus. There is no latest-time for sending these signals, the channel will wait indefinitely to receive them. Bits 0 through 17 and 35 must be zero to insure proper operation.

If a control word with WC = 0 is stored in B, the channel will load DA into the control word address register and fetch another control word from the location specified in the DA.

The control word address register is incremented by 1 after each control word fetch. Thus, when the number of words specified by the word count of a particular control word has been transferred, a new control word is fetched from the next address.

3.2.2 Typical Program Examples

All numbers are in octal representation.

Memory Location	Contents	
	WC	DA
B	0	001000
1000	777700	001777
1001	0	0

If SAWRITE is not asserted by the device, the channel will accept up to 100 words from the device, and store them sequentially in memory locations 2000 through 2077. The channel will then reset the CHANNEL BUSY signal. Note that 1001 must contain zero to stop the channel.

Memory Location	Contents	
	WC	DA
B	776000	004777
B + 1	0	0

If SAWRITE is asserted, the channel will deliver up to 2000 words to the device. The first word will come from 5000 and the others sequentially. The channel user should understand that if the device sends a WRITE CONTROL WORD REQUEST pulse while the CHANNEL BUSY signal is asserted, the contents of B + 1 will change, and may cause undersirable consequences.

Memory Location	Contents	
	WC	DA
B	0	000500
500	777700	000777
501	777000	004777
502	777300	0
503	777000	005777
504	0	0

If SAWRITE is not asserted, and this program runs to completion, the first 100 words delivered by (or from) the device (for example a file header) will go to 1000 through 1077, the next 1000 words will go to 5000 through 5777, the next 500 words will be skipped and the next 1000 words will go to 6000 through 6777. In the case of disk or tape operations, skipping saves memory space, and allows this type of transfer without reinitiating the device.

If SAWRITE had been asserted, the first 100 words delivered to the device would have come from 1000 through 1077, the next 1000 words from 5000 through 5777, the next 500 from 0 through 477, and the next 1000 words from 6000 through 6777.

3.2.3 Write Control Word

The write control word facility permits the device using the data channel to initiate a control word write. The device accomplishes this by asserting the WRITE CONTROL REQUEST signal and the data channel responds immediately by writing the control word into memory. Furthermore when the data channel terminates for any reason, it automatically writes the control word into memory. The memory address for the control word write is the initial control word address + 1. The control word written into memory contains the contents of the control word address register in bits 0 through 17 and the contents of the data address register in bits 18 through 35.

3.2.4 Write Even Parity

Normally, the parity for data transfer between data channel and core memory is odd since the central processor and other devices using memory, check for odd parity. As a maintenance check of the parity circuits, even parity can be specified by the device, by asserting the WRITE EVEN PARITY signal. Data written into memory from the data channel now contains even parity. Any device accessing this data from memory would expect to find a parity error since the device checks for odd parity.

3.2.5 Local Mode

An invaluable servicing aid, the "Local" mode of operation, is provided to facilitate maintenance of the DF10.

Operation within the Local mode allows troubleshooting of a DF10 without the requirement of having to program a device on the channel bus. A device is simulated by: Providing a means of starting the channel, loading an initial control word address, and generating device pulses at the appropriate time. An initial control word of 100_8 is forced and any channel command list can therefore be deposited in memory commencing at location 100_8.

The channel is automatically restarted after each termination thereby providing automatic recycling of any operation for observation with an oscilloscope.

Channel operation may be closely inspected while single stepping one memory cycle at a time under control of a pushbutton switch.

In a local mode device write operation, normal data transfer operation is simulated in that data is transferred from memory to the channel memory buffer. For a device read, only 0s are written into memory from the DF10.

Included is a delayed clear circuit which unconditionally clears the DF10 and then restarts it an arbitrary time following the initial start to allow troubleshooting in instances where a channel hangs up and cannot be re-started normally.

CHAPTER 4
PRINCIPLES OF OPERATION

This chapter describes the principles of operation of the DF10 Data Channel. The detailed logic descriptions refer to engineering drawings contained in Volume II of this manual. Reference to logic drawings is by mnemonic signal names; all signal names reflect their logic drawing origination. For example, signal CCB CLEAR MB originates on Drawing D-BS-DF10-0-CCB.

Before describing the detailed logic of the data channel, a general description and a simplified flow diagram are presented.

4.1 DF10 DATA CHANNEL DESCRIPTION

Operation is first initiated by an I/O device that is connected to the data channel. The PDP-10 program initiates operation when it issues an I/O instruction to the device to start operation and provide the initial control word address. The control word address is stored by the I/O device until it gains access to the data channel.

When access is gained, the I/O device sends the initial control word address to the data channel where it is stored in the control word address register. The data channel then fetches the first control word which usually consists of a jump to another control word address (WC = 0, DA $\neq$ 0). The second control word is then fetched and normally contains the WC (word count) in the left half, and DA (data address) in the right half. The WC and DA are stored in their respective data channel registers. The WC register specifies the number of data words to be transferred and the DA specifies the first core memory location to be read from or written into. After a word transfer between core memory and the device, the WC is decremented (i.e., WC contains 2s complement and is incremented) and the DA is incremented. When the WC overflows, the number of words initially specified have been transferred and the next control word is fetched from core memory. If the control word contains all 0s, the end of communications is specified and the data channel terminates operation.

A number of devices can be connected to the data channel; however, the data channel communicates with only one device at a time. To establish, maintain, and terminate communications, the signals shown in Table 4-1 are exchanged between device and data channel.

Table 4-1
Channel/Device Signal Transfer

Signal	Description
Data	These 100 ns negative-going ground to -3V pulses are transmitted in both directions between the device and channel over 36 bi-directional pulse lines.
Channel Pulse	This 100 ns negative-going pulse originates in the channel and accompanies the data pulses when the channel is sending data to the device. It also signifies a readiness to receive data when the device is attempting to send data to memory.
Device Pulse	This signal is similar in function to the channel pulse signal. It accompanies the data when the device is sending, and signifies readiness to receive when data flow is toward the device.
Channel Start	This is a level (true when -3V) transmitted from the device to the channel where it initiates channel operation.
Sawrite	This signal controls the direction of data transfer. When true, the device is writing (reading memory). The timing is the same as that for CHANNEL START.
Channel Busy	This signal originates in the channel and is asserted (-3V) sometime after CHANNEL START. The device does not transmit data over the bus until this signal is asserted. When this signal goes false after having been true, the channel has terminated for one reason or another. CHANNEL START and CHANNEL BUSY must be false for at least 400 ns prior to reassertion of CHANNEL START.
Write Control Word Request	This negative 100 ns pulse from the device causes the channel to store the current contents of the data address register and the control word address register in memory location B + 1 where B (an even number) is the channel initial control word address. The contents of the control word address register are loaded into bits 0 through 17 and the contents of the data address into bits 18 through 35. Upon any channel termination, the control word as specified above, is written into memory location B + 1 (as above) automatically.
Write Control Word Complete	This pulse originating in the channel signals the completion of the operation requested above and is not generated on the automatic transfer.
Channel Reset	Forces the data channel to its clear state.
Write Even Parity	Causes data channel to write even parity into memory.

Table 4-1 (Cont)
Channel/Device Signal Transfer

Signal	Description
No Such Memory	This pulse is sent from the channel as CHANNEL BUSY goes false indicating that the addressed memory failed to respond.
Control Word Parity Error	If a parity error is detected in the control word fetched from the memory by the channel, CHANNEL BUSY is reset, and this pulse is transmitted to the device from the channel.
Data Word Parity Error	This pulse accompanies the data and the CHANNEL PULSE when a data word from memory contains a parity error, and is sent to the device.

The I/O devices attached to a data channel are arranged as shown in Figure 4-1 (only the pertinent signals are shown). In order for a device to gain access to the data channel, the device must transmit CHANNEL START to the channel and receive CHANNEL BUSY from the channel. If a device is not actively engaged with the data channel, it relays the CHANNEL START and CHANNEL BUSY. A device that is relaying CHANNEL START is prevented from generating its own CHANNEL START. A device that is busy with the data channel does not relay CHANNEL BUSY.

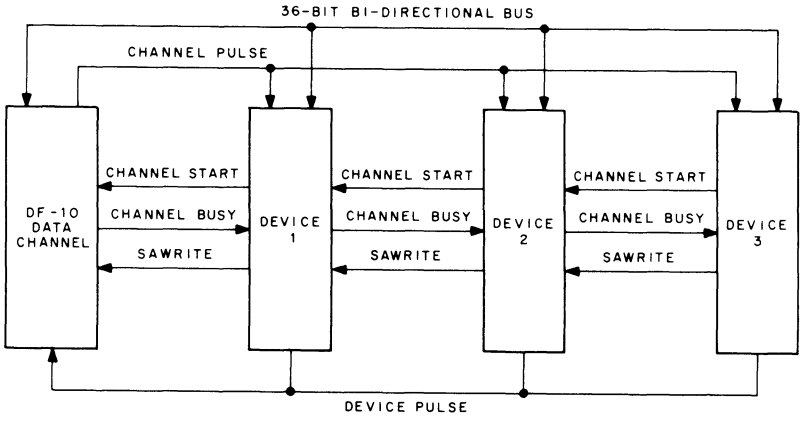


Figure 4-1 Data Channel Communication

Assume that devices 1 and 2 are not busy and device 3 initiates communication by asserting its CHANNEL START signal. The signal asserted is at device 2 and as device 2 is not busy, CHANNEL START is relayed. Similarly, device 1 relays CHANNEL START to the channel. The data channel acknowledges CHANNEL START by asserting CHANNEL BUSY. The information transfer has not specified to the channel which device is requesting access. The data channel responds only to the control signals by transferring data to and from the data bus or starting and stopping operation. It is the responsibility of the devices to determine which has access.

As devices 1 and 2 are not busy, they relay CHANNEL BUSY to device 3. Upon receipt of CHANNEL BUSY, device 3 has access to the data channel and can communicate over the data bus. The requirement for gaining access to the data channel therefore is dependent upon the assertion of CHANNEL START by the device and the receipt of CHANNEL BUSY from the channel.

To demonstrate this dual requirement, assume that device 2 is communicating with the data channel. It has asserted CHANNEL START and received CHANNEL BUSY. It does not relay CHANNEL BUSY to device 3. If now, device 3 attempts communication, it can assert its CHANNEL START as it is not relaying CHANNEL START. However, since device 2 is already generating a CHANNEL START, it essentially ignores the CHANNEL START from device 3. The CHANNEL BUSY is not relayed to device 3; therefore, device 3 does not gain access to the data channel because of the two requirements, assertion of CHANNEL START and receipt of CHANNEL BUSY. Device 3 now must wait until device 2 has finished with the data channel.

Either device 2 or the data channel can terminate operation. The data channel terminates operation by removing CHANNEL BUSY and the device responds by negating CHANNEL START. The device terminates operation by removing CHANNEL START and the data channel responds by negating CHANNEL BUSY. After termination, device 3 is free to communicate; however, the data channel requires at least 400 ns between the negation of CHANNEL BUSY and CHANNEL START and the reassertion of CHANNEL START. This 400 ns requirement is imposed upon device 2 (or any other device that is generating or relaying CHANNEL START and receives the on-to-off transition of CHANNEL BUSY). When termination occurs, the device must inhibit the generation or relaying of CHANNEL START for 400 ns.

4.2 FLOW DIAGRAM DESCRIPTION

Assuming initial operation, a device requests access to the data channel by generating CHANNEL START (refer to Figure 4-2). The data channel responds by resetting the IDLE flip-flop and asserting CHANNEL BUSY which is an acknowledgement to the device that it has access to the data channel. The data channel now prepares to receive the initial control word address.

The device responds to CHANNEL BUSY by generating the DEVICE PULSE and transferring the initial control word address to the data channel (into CWAD - Control Word ADdress register via MB, the Memory Buffer.) The data channel now fetches the control word from memory. The memory transfers the control word to the MB where it is evaluated. The left half of MB corresponds to the WC portion of the control word and the right half corresponds to the DA portion.

When both the WC and DA are not equal to 0, the data transfer starts. The direction of transfer is specified by SAWRITE. The address that the data is written into or read from is contained in the DA. The number of words

transferred is determined by the 2s complement number in the WC. On each data transfer, the WC and DA are incremented. When the WC overflows, a new control word is fetched (read) from memory.

When the WC $\neq 0$ and the DA = 0 and the SAWRITE signal indicates writing into memory, the channel receives the number of words specified by the WC from the device, but does not write them into memory. This allows the channel to skip certain data.

When the WC = 0 and the DA $\neq 0$, the address currently contained in the DA is transferred to CWAD. This becomes the address of the next control word (WC and DA) and a control word fetch cycle is initiated. This capability is similar to a jump instruction.

If both the WC and DA = 0, the data channel terminates operation by setting IDLE and removing CHANNEL BUSY.

During a data transfer cycle, CWAD is incremented after control word evaluation. For a write operation, a data word is obtained from memory at the earliest possible time. The data word is transferred to the data channel MB. The first data word obtained is immediately transferred to the device, as the device has signified readiness with the initial DEVICE PULSE. When the MB is empty a memory cycle is initiated to reload MB. When MB is full it waits for the DEVICE PULSE from the device. During each memory fetch, the DA and WC are incremented.

When the WC contains all 0s and the MB is empty a control word fetch is executed to obtain the next control word.

For a read operation, the device sends the data to the MB and generates DEVICE PULSE. The data channel transfers the data word to memory, increments the DA and WC and then generates the CHANNEL PULSE. This operation is repeated until the WC contains all 1s, at which time the next control word is fetched and evaluated.

4.3 DETAILED LOGIC DESCRIPTION

For the following description refer to the flow charts and logic diagram referenced in Chapter 6. The state of control circuits are assumed to be as shown in Flow Chart A, Drawing D-DF10-0-00A.

4.3.1 Initial Operation

For the initial operation, assume that a device is going to transfer data to memory via the data channel.

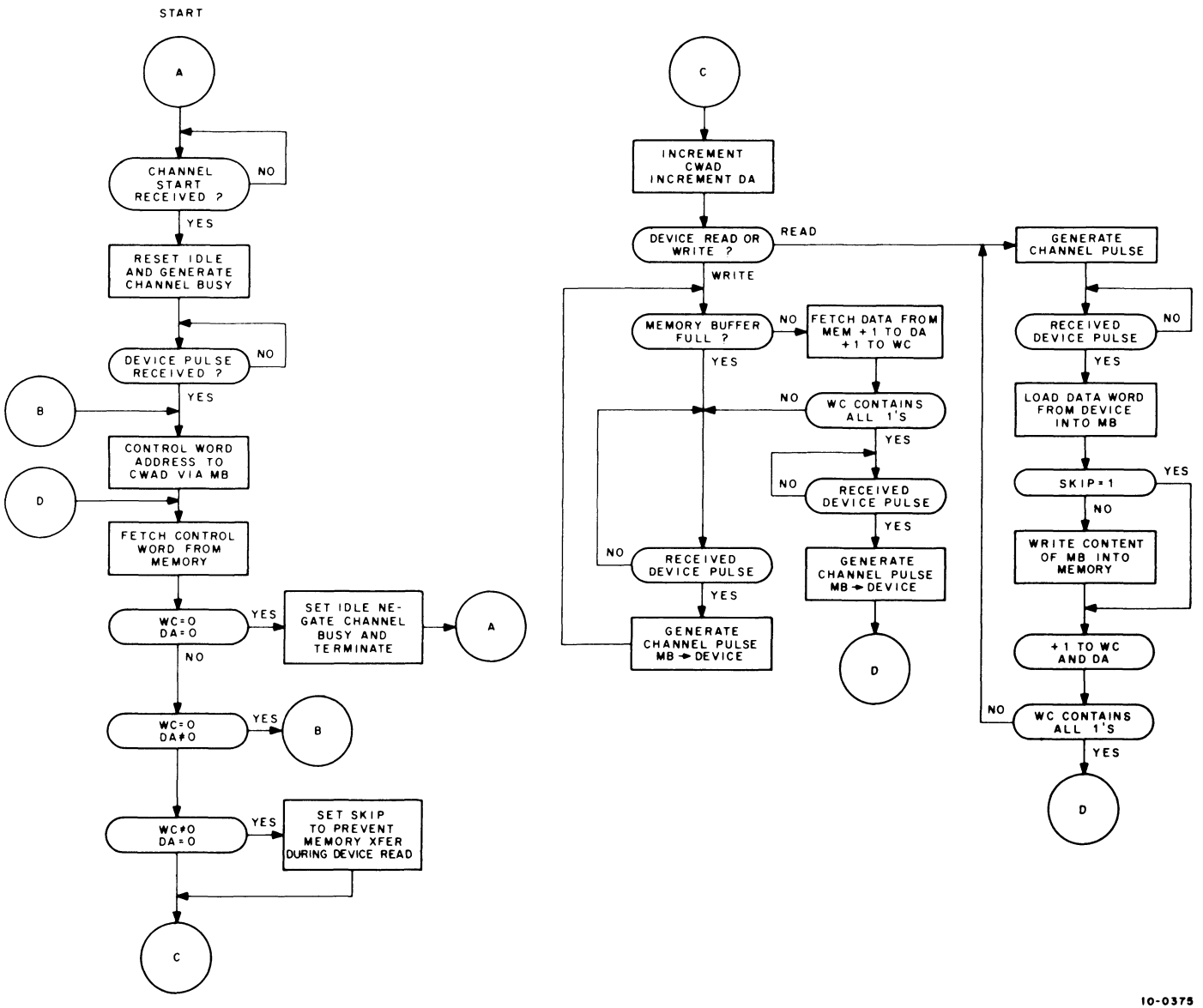


Figure 4-2 DF10 Flow Diagram

Operation starts when the device transmits CHANNEL START over channel cable #2 causing generation of CBC CHANNEL START in the channel. CBC CHANNEL START collector clears CYCLE STOP and generates CCA START. CCA START clears CCA IDLE after a 50 ns delay and generates CCB CLEAR MB which clears the MB in preparation for receiving the initial control word address from the device. The CCA IDLE (0) condition causes generation of CCC CHANNEL BUSY which is transmitted to the device over channel cable #3 acknowledging access to the channel.

The device also negates or asserts the SAWRITE signal over channel cable #2 to designate the read or write mode respectively, which either sets or resets CCA DEV READ; CIA INAD SYNC (0) is true at this time.

In response to CHANNEL BUSY, the device sends the control word initial address data pulses (via channel bus, CBC CHND 27 through 34 which loads the data into the MB). (The CC WRITE MEM GATE 1, 2, 3 signals are on at this time since CIA INAD SYNC (0) is true.) The device also generates CBC DEVICE PULSE which, after a delay, generates CCA XFER CW (transfer control word).

CCB DEVPULS is not generated because CIA INAD SYNC (1) is false and the DVPLS flip-flop remains clear. As the left half of MB is 0 (CCA MBL EQ ZERO true), CCA XFER CW generates CCA LOAD CWAD 1, 2, 3. (The device must insure that bits 0 through 18 are 0 when it transfers the initial control word address control word.) The right half of MB now contains the control word initial address. The CCA LOAD CWAD pulses jam transfer the right half of MB into the CWAD (Control Word ADdress) register (drawing CCW). Simultaneously, CCA LOAD CW generates CCB CLEAR MB to clear the memory buffer.

Up to this point, a device has requested access to the data channel via CHANNEL START; the data channel has acknowledged CHANNEL START by asserting CHANNEL BUSY, and the device has responded by sending the initial control word address which is now in the CWAD. The next operation is to fetch the control word from memory.

4.3.2 Control Word Fetch

The CCC CWRDRQ (Control Word ReaD ReQuest) flip-flop is set to obtain the initial control word from memory. CCA LOAD CWAD sets CCC CWRDRQ because CCA MBR EQ ZERO is false and CPG ODD PARITY is true. (Parity is forced odd by the CIA INAD SYNC false condition.) CCC CWRDRQ turns on CCC CWRD (Control Word ReaD). CCC CWRD (1) generates CCC CLCWR which clears the word count register and turns on CCC SYNC the memory cycle sync flip-flop.

CCC SYNC (1) generates CCC REQN thereby requesting access to the multiplexor which responds by generating CBC ACKN. This signal is generated by a W990 module in the data channel if it is connected directly to the memory bus (see the CBC print). CBC ACKN generates CAD ACKN 1, 2, 3 turning on the memory address gates

to the address bus. Since CCC CWRD is true, the control word address is gated to the memory address bus. CCC CWRD (1) generates CCC MCRD (Memory Cycle ReaD) to specify the direction of transfer to the memory.

CCC SYNC (1) ANDed with CBC ACKN and CC REQ (0) sets CCC REQ which generates CCC REQ CYC to request a memory cycle. CCC REQ PULSE sets the CIA INAD SYNC flip-flop which loads the initial control word address in CIA INAD 27 through 34.

The memory now responds with CBC ADDR ACK (ADDRess ACKnowledge) over memory cable 1A to acknowledge receipt of the address. CBC ADDR ACK generates CCB GTD ADDR ACK (GaTeD ADDRess ACKnowledge) which sets CCC NO REQ. CCC NO REQ (1) negates CCC REQ CYC.

The memory now sends the control word data and CBC RDRS (ReaD ReStart). CCC READ MEM GATE turns on the bus to the memory buffers thereby enabling the control word data to enter the memory buffer. CBC RDRS generates CCA END RD DY (END ReaD DelaY). This delay allows time for the parity and zero-detection circuits to settle. CCA END RD DY generates CCC END MC (END Memory Cycle) and CCA XFR CW since this is a control word transfer (-CCC RD DW being true). The CCC END MC signal strobes the delayed reset input of CCC CWRD and after a delay, turns off CCC SYNC. This delay insures that DWT, CWRD, and CWWT are all off when SYNC turns off, otherwise SYNC might retrigger.

4.3.3 Control Word Evaluation

In the event of a parity error, CCA LOAD CW ANDed with CPG ODD PARITY sets CCA IDLE terminating the cycle and generating CPG CON PAR ERR.

The newly fetched control word is examined in the CCA logic to determine the type of cycle to be performed. If all the word is 0, then a termination is specified. If WC = 0 (i.e., MBL = 0) and DA $\neq$ 0, then the DA data is transferred to the CWAD and another control word read is requested. If WC $\neq$ 0 and DA = 0, then the ensuing read cycle will perform all operations of reading the device; however, no data transfer to memory occurs. When WC $\neq$ 0 and DA $\neq$ 0, then the normal data transfer is requested.

When both the WC and the DA portion of the control word are 0, both the CCA MBL EQ ZERO and CCA MBR EQ ZERO signals are true and thus enable CCA LOAD CW to set the IDLE flip-flop to terminate operation.

When the WC portion is 0 (MBL EQ ZERO is true) and the DA portion not 0 (-MBR EQ ZERO is true), CCA LOAD CWAD 1, 2, and 3 is generated to load MB 18 through 35 into the CWAD. CCA LOAD CWAD3 then sets CWRDRQ and the next control word is fetched from memory as described previously.

When DA $\neq$ 0, CCA LOAD WCDA (1, 2, and 3) is generated and the content of MB is transferred to the control word register WCR WCT 0 through 17 and CDA 18 through 35; the control word register was cleared when CCC CWRD became true.

The DA portion determines if the ensuing read cycle is to transfer data to memory. If DA = 0, CCA SKIP is set to prevent a memory transfer. If DA $\neq$ 0, CCA SKIP is cleared to permit a normal transfer.

4.3.4 Data Transfer (READ)

To this point, the data channel has been initialized, and a control word has been obtained and evaluated. Assuming that the control word specifies a normal transfer (that is WC $\neq$ 0 and DA $\neq$ 0), the read operation continues.

The CCA LOAD WCDA 1 triggers a 450 ns delay which, upon timing out, generates CCB COUNT ADR1 and 2. (The delay allows time for the data address to settle before stepping it from DA-1 to DA.)

CCB SET VCW turns on CCB VCW (Valid Control Word) which signifies the readiness of the channel to transfer data. CCB VCW (1) generates CCB COUNT CWAD1 and 2 to increment the control word address register (drawing CCW). The MB has been cleared for some time; therefore the device may transmit the first word to the channel. VCW turning on, generates CCB INT CHN PLS (the INTernal CHaNnel PuLSe) which in turn generates CBC CHANNEL PULSE for the device.

Upon receiving CBC DEVICE PULSE from the device, the data channel generates CBC DEVPULS turning on CCB DVPLS (the device pulse flip-flop) and CCB MB FULL. With CCB DVPLS true, CCC DWT (Data Word Transfer) flip-flop is set, causing CCC SYNC to turn on a short time later. CCC SYNC generates CCC REQN, to request access to the multiplexor. As previously described, signal CBC ACKN (acknowledgement from either the jumper or multiplexor) generates CCC REQ CYCLE. This will start a memory write cycle (CCC MCWR asserted) since CCC WTDW (WriTe Data Word) is true. REQ and NO REQ behave as for control word fetch.

The memory responds with CCB GTD ADDR ACK which now does the following:

a. Turns off CCB DVPLS.

b. Generates CCB COUNT WC 1 and 2 and CCB COUNT ADR 1 and 2 to increment the control word.

c. Generates CCB WRIT MEM STROBE 1 and 2 to fire the data off to memory. CCB WRITE MEM STROBE 1 generates CC WRRS (the WRite ReStart to memory), CC END MC, and after a delay, CCB CLEAR MB which clears the CCB MB FULL flip-flop and the MB.

The CCB MB FULL (0) condition generates CCB INT CHN PLS (INTernal CHaNnel PuLSe) which generates CCC CHANNEL PULSE to complete one cycle.

When CCA SKIP is on, DVPLS will not turn on, thus preventing a memory cycle; however, the control word must still be counted, the channel pulse generated, and the MB cleared. This is accomplished by CCB SKIP PULSE.

If, when the CCC REQ PULSE is generated (when CCC REQ CYC is asserted to memory) the contents of the WC register is all 1s, WCR WCT OVFLO (word count overflow) will be true causing CCB VCW to turn off and CCC CWRDRQ to turn on. At the completion of the current write cycle, the channel fetches another control word as described previously. Note also that the CCB SKIP PULSE can cause the same action.

4.3.5 Data Transfer (Write)

The initial write cycle is identical to that of read except that CCB DVPLS is turned on by the device pulse that accompanies the initial address. This informs the channel that the device is ready to receive the first data word.

When CCB VCW is true, CCC DWT is true also, since CCB MB FULL is 0 and CCA READ is 0. A memory read cycle will now occur; however, CCB GTD ADDR ACK will only count the control word. CCA END RD DY will turn on CCB MB FULL and CCB AUX MB FULL. Since CCB DVPLS is on, CCB READ MEM STROBE 1 and 2 are now generated which:

a. Transmit the contents of MB to the device.

b. Generate CCB INT CHN PLS which in turn generates CCC CHANNEL PULSE for the device.

c. Through a delay, turn off CCB DVPLS.

d. Through a delay, generate CCB CLEAR MB turning off MB FULL and AUX MB FULL.

With MB FULL equal to 0, CCC DWT will turn on, generating another memory cycle and filling the memory buffer. When AUX MB FULL turns on, if the device pulse has not been received, the cycle will stop and not generate CCB READ MEM STROBE and CHANNEL PULSE. The data channel will wait until CCB DVPLS becomes true which occurs when the device is ready for the next word.

If WCR WCT OVFLO is true at CCC REQ PULSE time, CCB VCW turns off and CCC CWRDRQ turns on when the memory buffer is emptied, allowing a new control word to be fetched.

If there is a parity error in the data at the time READ MEM STROBE occurs, CPG DATA PAR ER is sent to the device to signal the error.

4.3.6 Write Control Word

The device may request the control word written into memory by asserting WT CONT WD RQ thereby generating CBC WRCON WD REQUEST which, if the channel is not IDLE, sets CCC CWWT SYNC. The next data transfer not calling for an immediate control word fetch sets CCC CWWTRQ. This condition sets CCC CWWT when the memory buffer is clear preventing CCB MB FULL from going off. (If READ = 1, CCB INT CHN PLS is inhibited and the device is not signalled that the MB is empty. If READ = 0, CCC DWT will not turn on to reload MB.) With CCC CWWT on, CCC START CW WRITE triggers and, after a delay to allow the MB to settle, CCC CW

to MB 1 and 2 are generated. These pulses load the MB, the contents of CCW CWAD 18 through 35 to MB 0 through 17 and CDA ADDR 18 through 35 to MB 18 through 35. CCC SYNC is now turned on to cause a memory cycle.

The address used for this transfer is the initial control word address + 1 which was initially stored in INAD 27 through 34. It is assumed that the initial address transferred was even. (If the initial address sent was odd, this transfer goes into that location by forcing memory address bit 35 equal to 1 for this transfer).

START CW WRITE turns off CCC CWWR SYNC and CCC CWWTRQ. Thus, when CCB WRIT MEM STROBE generates CCB CLEAR MB, MB FULL will go off allowing the normal cycle to resume.

CCB GTD ADDR ACK, in addition to generating CCB WRIT MEM STROBE, also generates CCC CONT WRD WRITE COMP to the device.

4.3.7 Cycle Termination

Normal termination occurs when CCA IDLE is set prior to CCA CYCLE STOP. With IDLE changing state, the device is obliged to remove CBC CHANNEL START which, after a delay, generates CCA CYCLE TERMINATE setting CCA CYCLE STOP and CC CWWR SYNC. With CWWR SYNC and IDLE on, CCC CWWT will set. After a delay, CCC START CW WRITE is generated, generating CCB CLEAR MB and after another delay CCC CW TO MB, loading MB and turning on SYNC thereby forcing a memory cycle to store information.

For an abnormal termination, the device removes CBC CHANNEL START prior to the channel going IDLE. This immediately inhibits the inputs to CCC SYNC, and after a delay, turns on CCA CYCLE STOP. (This delay allows SYNC to turn on if the inhibit arrived too late.) With CYCLE STOP on, as soon as the current memory cycle is completed (that is if SYNC was caught on) IDLE will come on. CCA CYCLE TERMINATE, the pulse which turned on CCA CYCLE STOP, has also turned on CCC CWWT SYNC. CCC CWWT SYNC (1) is ANDed with CCC SYNC (0) and CCA IDLE (1) to set CCC CWWT. Thus when IDLE goes on, CCC CWWT will go on also. This causes CCC START CW WRITE to fire after a delay (the delay to allow MB to settle) clearing MB.

4.3.8 Memory Hang-Up

When CCC SYNC turns on, it releases the retriggerable one-shot CCB NONEXMEM. If this one-shot times out indicating that the memory cycle has not been completed after 100 μs, it will generate CCB NO MEM. If SYNC turns off before it times out, the one-shot is caught in the one-state and held until next time.

This circuit presumes that the multiplexor, if used, can always service a channel in 100 μs. If this is not the case, and the multiplexor is servicing higher priority inputs and is not hung-up, a clear pulse is asserted which causes a disruption of the data transfer.

4.3.9 Local Mode

During the initialize phase; CCA POWER CLEAR clears CCC LOCAL START. Pressing the local start button causes generation of a direct set level to CCC RECYCLE DLY through a Schmidt trigger. CCC RECYCLE DLY is an integrating flip-flop processing a 25 μs delay. Upon release of the start button, the delay begins to time out. Upon timing out of the 25 μs delay, if the local switch is ON, CCC LOCAL START is set and CCC LOCAL START PLS is generated. CCC LOCAL START PLS clears CCC STOP MC.

The CCC LOCAL START (1) condition generates CBC CHANNEL START B. This simulates a start command from a device and thereby initiates channel operation in the local mode.

CBC CHANNEL START generates CCA START which, after 50 ns delay, clears CCA IDLE. CCA IDLE (0) ANDed with CCC LOCAL START (1) generates CCC LOCAL DVPLS simulating the initial DEVICE PULSE from an I/O device. CIA INAD SYNC B (asserted when CCA INAD SYNC (0) and CCA IDLE (0) are true) ANDed with CCC LOCAL DVPLS, sets MB29 thereby forcing 100_8 into the MB. This is the local mode initial control word address.

The channel now proceeds to execute the control word sequence beginning at 100_8. CCB INT CHN PLS fires CCB START DVPLS DLY (6 μs) to regenerate CCC LOCAL DVPLS thereby establishing the sequence of data word transfers which will progress until normal word count overflow.

Termination occurs if CCC LOCAL TERM is generated. The conditions for generation of CCC LOCAL TERM are CCB LOCAL and CCA IDLE (1). CCC LOCAL TERM clears CCC LOCAL START thereby dropping CBC CHANNEL START.

Since the STOP and SINGLE STEP switches are OFF, when CCC LOCAL START is reset, CCC RECYCLE DLY is retriggered, and the local mode channel cycle continues as previously described.

Placing the MC SS switch ON allows channel operation to be single-stepped, the DF10 performing one memory cycle each time the start button is depressed. This action is controlled by the CCC STOP MC flip-flop which is set at the completion of each memory cycle by CCC END MC. CCC END MC is also gated through a 50 ns delay to the direct clear input of CCC SYNC. When set, CCC STOP MC prevents CCC SYNC from being set by inhibiting those inputs to CCC SYNC which cause a data word transfer or a control word read. A control word write cycle cannot be inhibited and thus cannot be single stepped; therefore, in some instances when Start originated, two memory cycles occur, the last being a control word write. Since CCC SYNC must be set in order for the channel to perform a memory cycle, the DF10 stops after each cycle until CCC STOP MC is reset by CCC LOCAL START PLS (generated by pressing the start button), or by placing the local switch to OFF. Automatic setting of CCC RECYCLE DLY by CCC LOCAL START (0) is inhibited by assertion of CCC SINGLE STEP at CCC RECYCLE DLY's gated one input.

The CLEAR CYCLE switch, when ON, allows CCA CLR CYCLE DLY to be set by CCC LOCAL START (1). This one-shot has an associated 300 μs delay which, upon timing out, generates CCA LOCAL CLR. CCA LOCAL CLR generates CCC POWER CLEAR which performs the identical initializing functions as when powering up or pressing the clear switch. CCA POWER CLEAR resets CCC LOCAL START. Therefore, if the single step switch is not ON, CCC RECYCLE DLY retriggers and the operation repeats.

CHAPTER 5
MAINTENANCE

This chapter describes the preventive and corrective maintenance procedures which apply to the DF10. The operational characteristics of the DF10 are such (non-programmable) that no specific diagnostic program applies to the channel. Also, the margin tolerances exhibited by the channel are dependent upon the type of controller used and the program being run. On-line testing procedures therefore, relate to the diagnostic programs written for the devices which compose the system.

Off line-testing is facilitated by use of the "Local Mode" wherein a device is simulated by logic contained within the DF10 and blocks of data are actually transferred to and from memory through the channel.

5.1 PREVENTIVE MAINTENANCE

A preventive maintenance program consists of the performance of specific tasks at intervals determined by the usage and down-time tolerance of the system. The benefit to be realized from a good preventive maintenance program is the discovery of conditions which, if ignored, might result in failure of the system at a later time.

All pertinent action taken during the performance of either preventive or corrective maintenance procedures should be entered in the maintenance log book.

5.1.2 Test Equipment

Table 5-1 lists the test equipment required for performing the maintenance tasks.

Table 5-1
Required Test Equipment

Equipment	Function
Voltmeter	Capable of measuring positive or negative dc potentials over a range of 0V to 70V with 3% accuracy.
Oscilloscope	Tektronix 453, or equivalent, calibrated against frequency and voltage standards.

5.1.3 Daily Tasks

Make a general visual inspection of the interior and exterior of the equipment. Correct obvious deficiencies such as burned out indicator lamps and improperly seated modules and connectors. Determine that fans are running and that air filters are not clogged with dirt.

5.1.4 Monthly Tasks

Clean air filters.

5.1.5 Quarterly Tasks

Clean and inspect the interior and exterior of the equipment; repair all mechanical damage and replace any component or wiring which appears damaged or abnormal.

If the system contains an RC10 Controller, margin the DF10 while running MAINDEC 10 D5CC (part EX Float). Margins should agree with the specifications in Table 5-2. Correct faulty margin indications.

Table 5-2
DF10 Margin Specifications (RC10)

Rack	+10V		-15V	
A, B, C, E, J, K, L,	2.5V	17.5V	-18V	-12V
D	3.6V	17.5V	-18V	-12V
F, H	6V	17.5V	-18V	-12V

Consult the particular device maintenance manual for margins applying to other diagnostics.

5.1.6 Power Supply Measurements

The +10V and -15V potentials required for operation of the DF10 logic are provided by two Type 728 (60 Hz) or 728A (50 Hz) Power Supplies mounted above the Type 844 Power Control on the rear plenum door. Each potential should be read from the terminals on the logic end. If the amplitude or ripple content is not within the limits specified, the power supply must be either repaired or replaced.

Check the +10V outputs between the red (+) and black (-) leads. These should measure between 9.5V and 11V with less than 700 mV ripple. The -15V output is measured between the blue (-) and black (+) leads; these readings should fall between 14.5V and -16V with less than 700 mV ripple.

5.2 CORRECTIVE MAINTENANCE

The DF10 is constructed of highly reliable transistorized modules and standard circuits. The reliability of the equipment, combined with proper performance of the preventive maintenance tasks, ensures minimum down-time due to failure. If a malfunction occurs, analyze the fault and correct the condition as suggested in the following paragraphs.

5.2.1 Preliminary Investigation

The primary purpose of the preliminary investigation is to simplify and, if possible, isolate the fault. If the fault occurred while in the user program, determine from the user what is expected of the program and the particular error. Take full advantage of all built-in maintenance aids such as the lamps provided on the indicator panel and the local operation mode described in the following paragraphs. All failure possibilities cannot be discussed; however, two examples of the use of the local mode to diagnose a malfunction are presented and should demonstrate the value and use of the local mode to servicing personnel.

5.2.2 Local Mode Troubleshooting

The local mode switch functions and the indicator panel are discussed in Chapter 3.

5.2.2.1 Troubleshooting - Example 1 Problem: A DF10 Data Channel is connected to a device not manufactured by DEC therefore, service personnel have no device diagnostic. The user states that the channel will not write data to the buffer starting at location 2000 and is altering the program instead.

Procedure:

a. Throw the local switch ON and the device write switch OFF. Deposit the command list into memory.

100		1000
1000	777777	001777
1001	0	0

b. Enter ONES into 2000; press the Start button. The channel should continuously write ZEROS into this location; however, the location still contains ONES indicating a malfunction.

c. The control word written into 101 by the channel is examined and the address portion found to contain 6001 (110 000 000 001) rather than 2001 (010 000 000 001). This indicates that bit 24 of the DF10's data address register is failing.

d. Press the Stop button, then turn ON the single step switch and press the Start switch. The channel starts and reads the control word jump in 100. Press Start again, the channel reads the control word in 1000 into the word count and data address registers. Bit 24 is indeed on after reading the control word. The S202 module in location J07 is replaced and normal operation ensues.

5.2.2.2 Troubleshooting - Example 2 Problem: Once started, the DF10 hangs up with CWWT on. Due to this condition, the channel cannot be started by the program or cleared with the IOB reset switch. Field Service personnel, therefore, have no way to loop the channel for troubleshooting except in the local mode.

Procedure:

a. Turn ON Local and deposit the control word into memory

100 0 0

b. Press the Start switch; the channel hangs up with CWWT ON. Turn ON the CLR CYC switch and press Start again.

c. The channel now starts, clears after 300 μs and restarts. With the oscilloscope synchronized on CWWT going on, it is observed that there is no END MC pulse to clear CWWT; also NO MEM is missing. The absence of NO MEM is found to be due to a faulty B611 module in the location C24. The absence of END MC (due to no ADDR ACK) is isolated to the memory.

CHAPTER 6

RECOMMENDED SPARE PARTS LIST

This section contains a listing of all modules (Table 6-1), transistors (Table 6-2), and miscellaneous components (Table 6-3), together with recommended quantities of each to be stocked at the user's site.

Table 6-1
Modules

DEC Type No.	Description	No. in Use	Suggested Spares
B130	3-Bit Parity Circuit	18	2
B133	Diode Gate	22	3
B134	Diode Gate	2	1
B135	Diode Gate	11	2
B137	Diode Gate	3	1
B163	Diode Gate	22	3
B165	Inverter	12	2
B212	Dual R S Flip-Flop	5	1
B214	Flip-Flop	15	2
B311	Tapped Delay Line	11	2
B611	Pulse Amplifier	12	2
B683	Bus Driver	11	2
B685	Diode Gate Driver	3	1
G704	2 MA. Level Terminator	14	2
R001	Diode Network	3	1
R303	Integrating One-Shot	2	1
R613	Pulse Amplifier	2	1
S181	DC Carry Chain	9	1
S202	Flip-Flop (Quad)	27	3
S603	Pulse Amplifier	1	1
W012	Indicator Cable Connector	11	2
W102	Pulse Bus Transceiver	22	3

Table 6-1 (Cont)
Modules

DEC Type No.	Description	No. in Use	Suggested Spares
W250	Indicator Cable Connector	-	1
W301	Delay Line	1	1
W990	Blank Module	1	-

Table 6-2
Transistors

Type	DEC Part No.	Suggested Spares
DEC SDA-86718-1	15-02105	2
2894	15-03097	2
2N3605	15-02151	2
2N4258	15-05321	6
DEC 3009B-S	15-03100	2
2N2904	15-01742	2
DEC 3639-D	15-02762-02	8
DEC 2894-38-S	15-03099	2
DEC 3009A-S	15-01999	2
DEC 2894-2S	15-03098	2
DEC 6534	15-03409	2

Table 6-3
Miscellaneous

Description	DEC Part No.	Suggested Spares
D662 Diode	11-00113	10
D664 Diode	11-00114	10
D668 Diode	11-02161	6
Indicator Lamps	12-555	10
Trimpot	A-13-5395	1

Digital Equipment Corporation
Maynard, Massachusetts

digital

printed in U.S.A.