CHARACTER DISPLAY TERMINAL

VG-920

SERVICE MANUAL

CONTENTS

1. OUTLINE

1.1 General

Character display terminal VG-920 consists of display unit DP-920 and keyboard unit KB-920.

This is a conversational-mode equipment that enables data of up to 80 or 132 characters x 24 lines to be displayed on the non-glare 12" CRT and provided with the DEC VT220 function.

The logic configuration centering around micro CPU allows this terminal to provide a variety of functions and high flexibility in operation. This terminal employs the angle alignment feature for the screen and the low-profile keyboard so as to have high operationability.

Thus, it is said to be a high-performance and easy-to-use equipment that can meet a wide range of applications in various fields.

1.2 Features

1) The keyboard unit is separated from the main frame so as to be easily used and it is designed very compact.
2) The operation angle alignment feature allows the display unit to swing up/down and left/right. Moreover, the keyboard can be used at any of three tilt angles to allow convenient operation.

3) Employment of micro CPU and advanced LSIs enables a compact mounting design.

4) The Set Up function enables the optimum function to be selected in order to meet a wide range of applications. Further, the selected optimum function can be stored in nonvolatile memory (NVR).

5) To interface with the host computer, the MODEM interface conforming to RS232C/RS423 and the 20mA current loop interface are provided as the standard features. The data transfer rate ranging from 75 to 19200 bps can be selected.

6) To interface with the serial printer, the MODEM interface conforming to RS232C/RS423 is provided as the standard feature.

7) The parallel printer interface conforming to the CENTRONIX specifications is also provided as an option at factory shipment.

8) This terminal is fully compatible with the DEC VT220 function.

2. SPECIFICATIONS

2.1 Display Unit DP-920 Specifications

1) Display Function

(1) CRT: 12 inch non-glare screen (Green, Amber, and White)

(2) Active display size: 210 mm x 140 mm

(3) Screen capacity: 80 columns x 24 lines or
132 columns x 24 lines
(For single-height and single-width characters)

(4) Character format: 7 x 10 dot matrix (For single-height and single-width characters)
10 x 10 dot matrix (For 80 characters/line)
9 x 10 dot matrix (For 132 characters/line)

(5) Display system: Raster scan

(6) Refresh rate: 50 Hz/sec. or 60 Hz/sec.
(Selected in the Set Up mode)

(7) Cursor: Blinking block/block/blinking underline/underline non-display
(Selected in the Set Up mode)

(8) Character set: (94 characters each)
- ASCII character set
- UK national character set
- Special graphic character set
- Auxiliary character set
- Down Line Loadable character set

(9) Code: ANSI/ASCII

2) Operation mode

(1) Set Up mode

Sets the operation conditions with the keyboard unit. (Selected by the Set Up key)

(2) Online mode

Sends/receives data to/from the host computer (Selected in the Set Up mode)

(3) Local mode

Inhibits data from being transmitted to the host computer and stores the received data in the received data buffer. (Selected in the Set Up mode)

3) Control mode

(1) VT200 7-bit control mode

Supports the 7-bit control characters.

(2) VT200 8-bit control mode

Supports the 8-bit control characters.

(3) VT100 mode

This is the control mode compatible with the DEC VT100 terminal.

(4) VT52 mode

This is the control mode compatible with the DEC VT52 terminal.

4) Data transmitting/receiving (Line interface) function

(1) Communication mode: Conversational mode

(2) Transfer rate: 75/110/150/300/600/1200/2400/4800/9600/19200 bps. (Selected in the Set Up mode)

(3) Data format

Asynchronous mode, Bit serial

1 start-stop bit, 7 or 8 data bits, 0 or 1 parity bit, 1 or 2 stop bits. (Selected in the Set Up mode.)

(4) Interface: EIA RS232C/RS423 or 20mA current loop

5) Print (Printer interface) function

(1) Print mode: Normal print/Auto print/Controller mode

(2) Serial interface

(i) Transfer rate: 75/110/150/300/600/1200/

2400/4800/9600/19200 bps. (Selected in the Set Up mode.)

(ii) Data format:

1 start-stop bit, 7 or 8 data bits, 0 or 1 parity bit, 1 or 2 stop bits. (Selected in the Set Up mode.)

(iii) Interface: EIA RS232C/RS423

(3) Parallel interface (Option)

The handshake system (conforming to CENTRONIX, 36-pin connector) using 8-bit parallel data at the TTL level and acknowledge and busy signals is employed.

6) Audible alarm

(1) Key click: Operates when the effective key on the keyboard unit is pressed.

(2) Bell: Operates when keyed-in data causes the cursor to move to the right margin at occurrence of a RAM error during self-diagnosis, at reception of a BEL code, or at occurrence of a keyboard operation error.

7) Power supply: AC90 to 132V/AC180 to 264V
50/60 Hz
32W (including the keyboard unit)

8) Ambient temperature and humidity, dimensions, weight, and storage conditions

(1) Ambient temperature: 0 to 40°C

(2) Ambient humidity: 35 to 80% RH (non-condensing)

(3) Dimensions: 343 mm (H) x 353 mm (W) x 324 mm (D)

(4) Weight: About 10 kg

(5) Storage conditions: <Temperature>-10 to 50°C
<Humidity> 10 to 90% RH (non-condensing)

2.2 Keyboard Unit KB-920 Specifications

1) Key arrangement

(1) Keytop arrangement: The keytop consists of the main keypad, editing keypad, auxiliary keypad, and Top-Row function keys.

(2) Keytop inclination: Step sculpture

(3) Key movement: 4±0.5 mm

(4) Key row offset: 9.5 - 4.75 - 9.5 mm

2) Data output function

(1) Structure and output: Low-profile type, capacitive keyboard with serial

encoded output

(2) Roll over: N-key roll over

(3) Repeat function: Automatic repeat (when pressing a key for more than 0.5 second)

3) Ambient temperature and humidity, dimensions, weight, and storage conditions

(1) Ambient temperature: 0 to 40°C

(2) Ambient humidity: 35 to 80% RH (non-condensing)

(3) Dimensions: 30 mm (H) x 532 mm (W) x 197 mm (D)

(4) Weight: About 2.5 kg

(5) Strage conditions:

‹Temperature› -10 to 50°C ‹Humidity› 10 to 90% RH (non-condensing)

2.3 Standard Shipment Specifications

VG-920 is so set as to be powered by the AC power supply of your country at shipment. If the AC power supply voltage is 100 to 120V, VG-920 is provided with a 2-A fuse and the AC voltage changeover switch is set at 100V.
On the other hand, if the AC power supply voltage is 200 to 240 V, it is provided with an 1-A fuse and the AC voltage changeover switch is set to 200V.

CAUTION

When powering this terminal with other power supply voltage, be sure to use it after replacing the fuse according to the

AC voltage value and setting the AC voltage Select switch to the voltage to be supplied.

3. SERVICE INFORMATION

Be sure to follow the following instructions during the service and inspection of this equipment:

1) Be sure to follow the cautions.

For the points which require a special care when they are serviced, the cautions are indicated on the cabinet and the parts with labels, etc. Therefore, be sure to follow these cautions and the cautions described in the function and operation manuals, etc.

2) Beware of an electric shock.

(1) Be careful for handling this equipment when it is powered ON because it has the high-voltage portions inside.

(2) Be careful so as not to touch the heat sink on the board when this equipment is powered ON because the voltage may be impressed to the heat sink.

3) Be sure to use the specified parts.

The parts of this equipment have the safety characteristics such as incombustibility and voltage withstandingness . Therefore, be sure to use the specified parts for replacement.

Use of the part other than the specified one may cause the trouble to get worse or cause an electric

shock or fire.

4) Be sure to restore the parts mounting and wire leading after completion of the service or inspection.
Some parts employ insulation materials such as a tube and tape and are mounted being unseated on the printed-circuit board. Also, the internal wiring is so made as to keep away from the heat-generating and high-voltage parts with leading and clampers. Therefore, be sure to restore these.

5) Be careful for handling the CRT.
It is dangerous to shock the cone part of the CRT at removal of the CRT or maintenance performed from the back. Be sure to take a great care for handling the CRT.

6) Caution for X ray
The CRT, the high-voltage peripheral circuits, etc. are so designed as to secure the safety against X ray. Therefore, be sure to use the specified parts such as the CRT and do not change the circuit when servicing the high-voltage peripheral circuit.

7) Be sure to perform the safety inspection after completion of the service.
Check if the screws, parts, and wiring removed for

the service are restored and if the serviced points are deteriorated, in order to secure the safety.

8) Do not use any solvent such as thinner, benzine, or gasoline to clean up the exterior of the equipment. It may damages the plastic parts.
Be sure to clean up the equipment with the cloth soaked in a small amount of furniture or house cleaner.

4. INSTALLATION

4.1 Unpacking and Installation

For VG-920, display unit DP-920 and keyboard unit KB-920 are independently packaged.

Unpack these units in reference to Figures 4-1-1 and 4-1-2, and place them quietly on a stable and solid stand.

For installing VG-920, be sure to meet the power supply and environmental conditions specified in Section 2.1 "Display Unit DP-920 Specifications" and the environmental conditions specified in Section 2.2 "Keyboard Unit KB-920 Specifications, and take care the following points:

1) Do not install this equipment in the place with the direct sunlight.
2) Do not operate this equipment when enclosed with a cover or cloth. This prevents heat radiation effect thus may cause a failure.
3) Keep moisture, dust, oil, and smoke away from this equipment as far as possible.
4) Keep any magnetism generating article (such as a transformer) as far as possible.

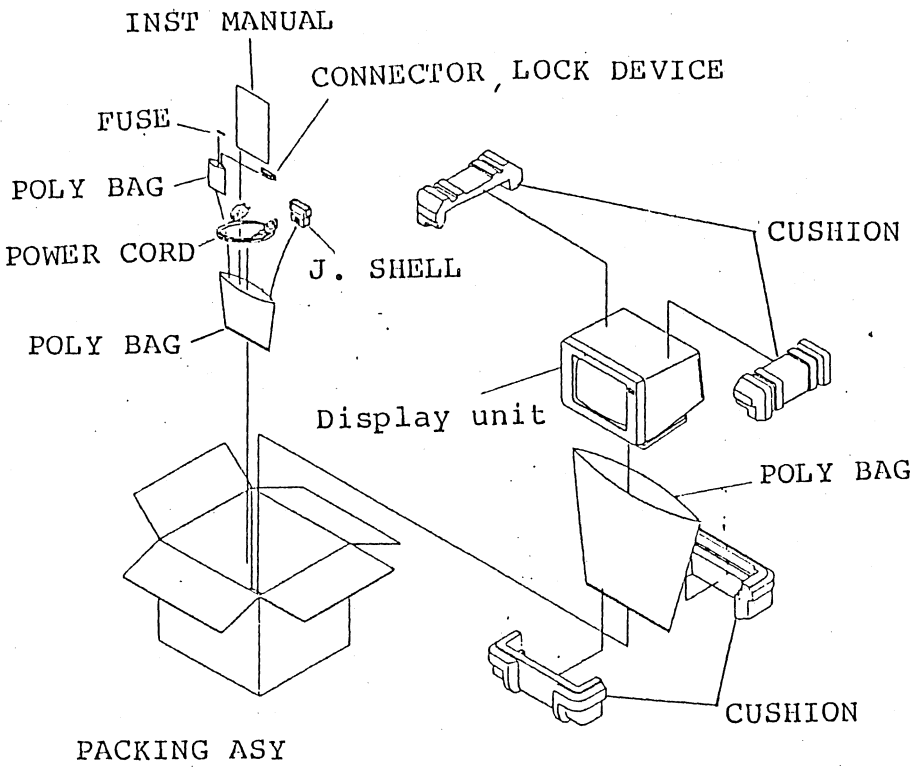


Fig. 4-1-1 Display Unit Packaging Diagram

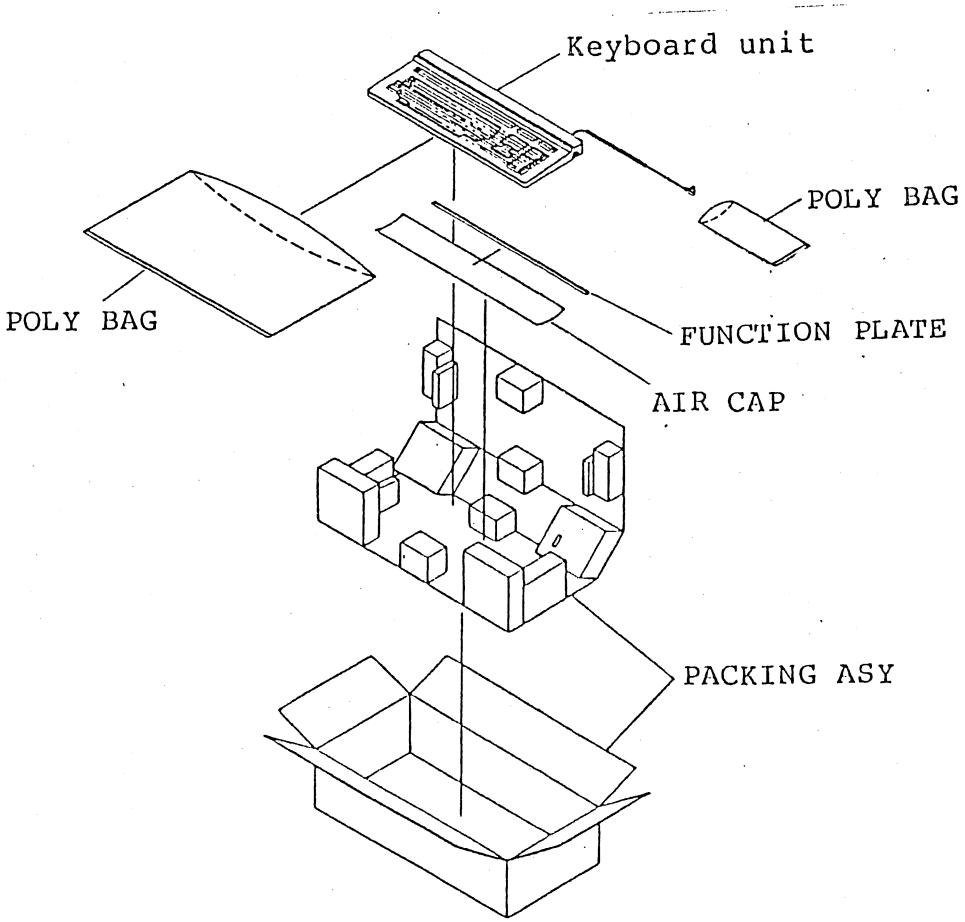


Fig. 4-1-2 Keyboard Unit Packaging Diagram

4.2 Appearance and Dimensions

Fig. 4-2-1 and Fig. 4-2-2 show the dimensions of display unit DP-920 and keyboard unit KB-920, respectively.

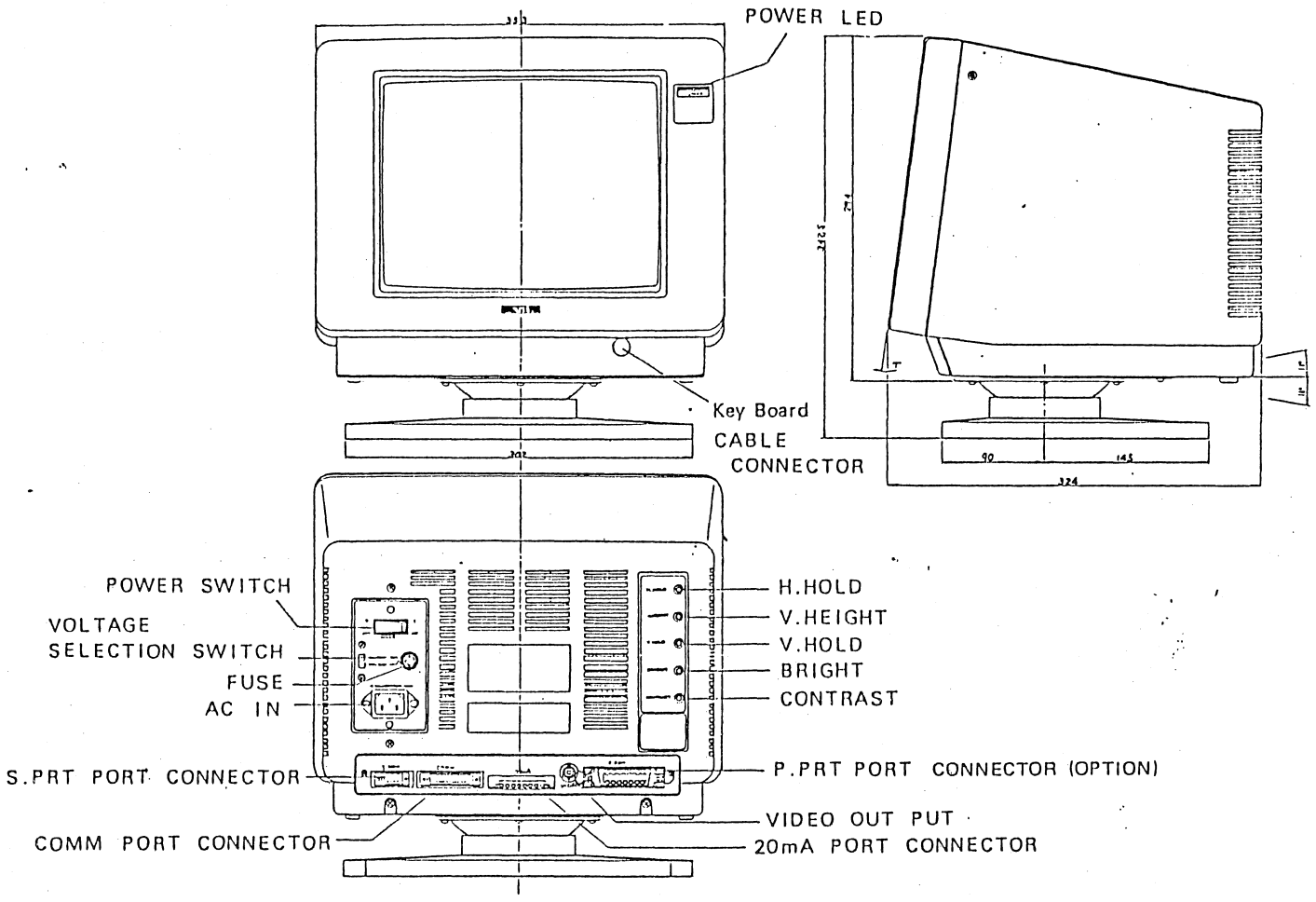


Fig. 4-2-1 Display Unit Dimensions Diagram

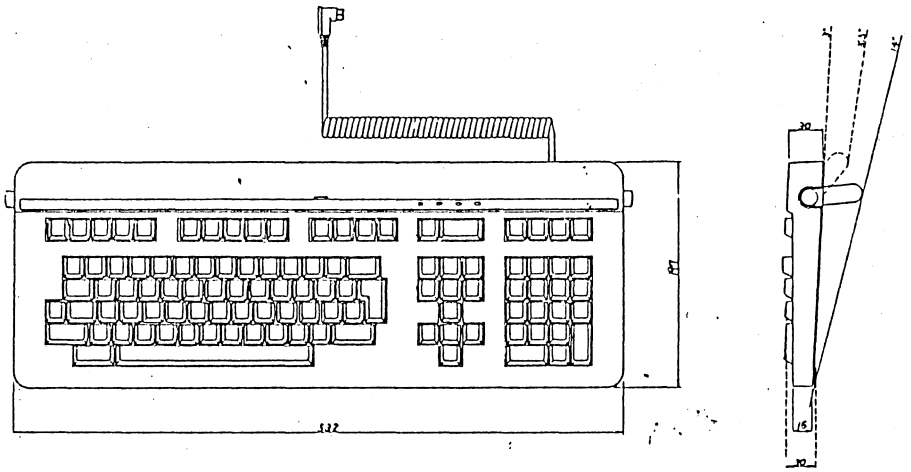


Fig. 4-2-2 Keyboard Unit Dimensions Diagram

4.3 Connections

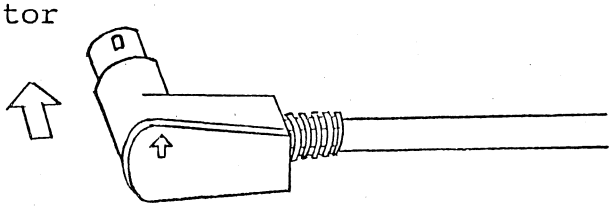
1) Connecting the keyboard unit (KB-920) and the display unit (DP-920)

Connect the DIN connector provided for the keyboard unit with the keyboard connector on the lower right side of the front panel of display unit.

Make sure to have the arrow pointing up when connecting the DIN connector.

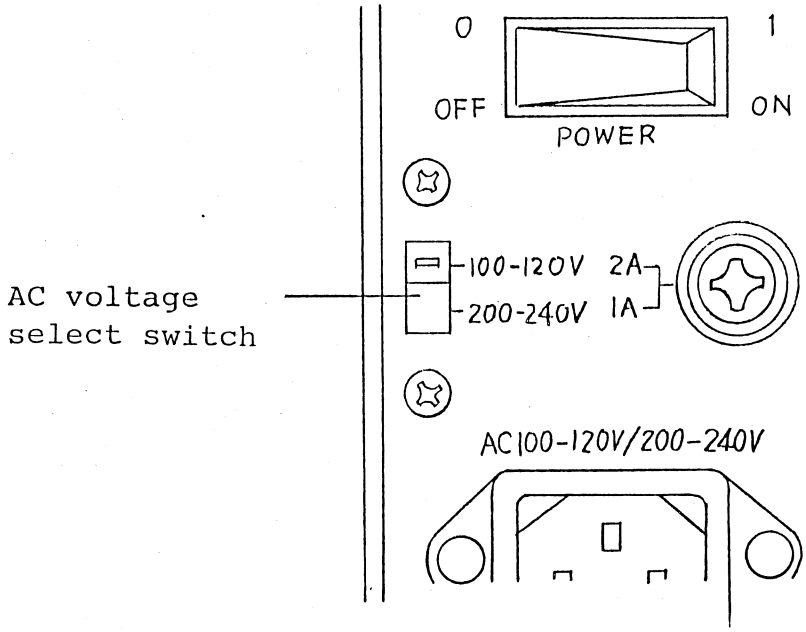
Be sure to turn OFF the POWER switch when plugging the keyboard connector in and out.

Keyboard connector

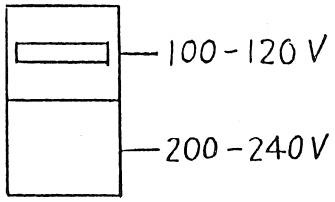


2) Connecting the power supply cord

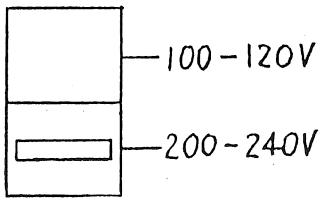
Be sure to check that the AC voltage select switch is set to the voltage to be supplied when connecting the power supply cord.



Be sure to check that the AC voltage Select switch is set as shown below when the power supply voltage is 100 to 120 V:



Be sure to check that the AC voltage Select switch is set as shown below when the power supply voltage is 200 to 240 V.



CAUTION

If the switch setting is wrong, be sure to set the switch correctly according to the following procedures. VG-920 may fail if operated with the wrong AC voltage.

(1) Set the AC voltage Select switch to the voltage to be supplied when the power cord is disconnected.

(2) Replace the fuse according to the voltage value to be supplied.

Setting the AC voltage to AC100V: 2A/250V fuse

The 2A/250V fuse is pre-set to the equipment to be shipped to the 100V area as a standard part; it is provided as an accessory for the equipment to be shipped to the 200V area.

Setting the AC voltage to AC200V: 1A/250V

The 1A/250V fuse is pre-set to the equipment to be shipped to the 200V area as a standard part; it is provided as an accessory for the equipment to be shipped to the 100V area.

(3) Connect the power cord with the equipment and

plug the cord into the AC plug receptacle.

3) Connecting the line interface connector

This equipment is provided with two kinds of line interface; the COMM port conforming to the EIA RS232C/RS423 standard and the 20mA port for the 20mA current loop interface.

Take care the following points for connection:

(1) When connecting the 25P D connector with the COMM port, be sure to tighten two screws on the connector cover to lock the connector plug onto the equipment.

(2) When connecting the Mate-N-Loc connector with the 20mA port, fix the connector to the equipment with the left and right lock mechanisms.

(3) Be sure to turn OFF the POWER switch when plugging the line interface connector in and out.

4) Printer interface connector

Either the S.PRT port (standard) conforming to the EIA RS232C/RS423 standard or the P.PRT (Option) for the TTL level (conforming to CENTRONIX) parallel data can be selected. For connection, take care the following points:

(1) When connecting the 9pin D connector with the S.PRT port, be sure to tighten two screws on the connector cover to lock the connector plug onto the equipment.

(2) When connecting the connector with the P.PRT port (option), lock the connector plug onto the equipment with two spring locks of the connector receptacle.

(3) Be sure to turn OFF the POWER switch when plugging the printer interface connector in and out.

4.4 Angle Alignment

1) Angle alignment for display unit DP-920

The tilt swivel feature enables up/down and right/left angle alignment on the CRT. (See Section 4.2 "Appearance and Dimensions.")

2) Angle alignment for keyboard unit KB-920

The tilt angle of the keyboard unit can be adjusted in 3 steps by operating the angle alignment Foots on both right and left sides of this unit.

(See Section 4.2 "Appearance and Dimensions.")

The Foots come out by pressing the button.

5. OPERATION PRINCIPLES

5.1 General

VG-920 consists of display unit DP-920 and keyboard unit KB-920, and DP-920 consists of the power supply, monitor, and controller.

Fig. 5-1-1 shows the VG-920 configuration.

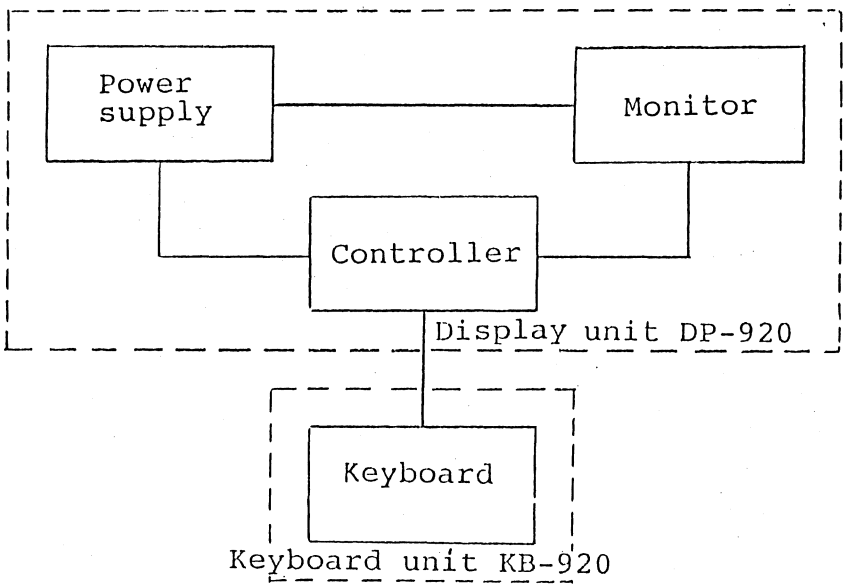


Fig. 5-1-1 VG-920 Configuration

5.2 Power supply

The power supply has the input of AC100 to 120V or AC200 to 240V, and supplies +12V to monitor, +5V and ±12V to controller, and +5V to keyboard unit, respectively.

The input voltage (AC100 to 120V or AC200 to 240V) is set by the AC voltage select switch. Fig. 5-1-2 shows the power supply system diagram.

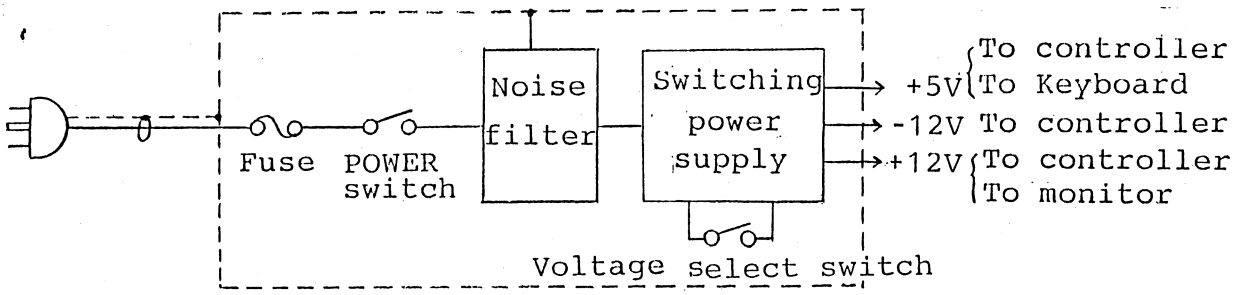


Fig. 5-1-2 Power Supply System Diagram

	Voltage select switch	Fuse
When setting AC100 to 120V	Close	2A/250V
When setting AC200 to 240V	Open	1A/250V

5.3 Monitor

The monitor consists of the non-glare 12" CRT and the monitor board, and display characters on the CRT screen with the TTL-level video signal (VIDEO), vertical synchronous signal (VSYHC), and horizontal synchronous signal (HSYNC) supplied from the controller.

1) Video signal amplifier circuit

The video signal supplied from the controller is amplified by the video amplifier transistors (X103 and X401) connected in cascade. The signal outputted from the video amplifier transistors is supplied to the cathode of CRT as the video signal with the corrected frequency characteristic.

The amplitude of the video signal is adjusted by the CONTRAST volume (R106). The brightness is controlled by changing the first grid voltage with the BRIGHT volume (R325).

2) Vertical deflection circuit

The vertical oscillation, waveform shape, and vertical output circuit consists of single-chip IC AN5763 (IC201) and its peripheral circuit.

The sawtooth wave is generated by R210, R211, R220, R221, C205, and C206 and amplified by IC201.

It is supplied to the vertical polarizing coil as the sawtooth current to deflect the CRT beam vertically. The oscillation frequency is controlled by adjusting the discharge time constant determined by C204, R203, and R204, and synchronized with the vertical synchronous signal. The vertical amplitude and the vertical linearity are adjusted by the V.HEIGHT volume (R210) and the V.LIN volume (R209), respectively.

3) Horizontal deflection circuit

The horizontal, phase detector,and horizontal drive circuit consists of a single chip IC AN5753 (IC301) and its peripheral circuits.

The horizontal output stage has the function to deflect the CRT beam left and right by impressing the sawtooth waveform deflection current to the horizontal deflection coil, and the function to generate the high screen voltage to be impressed to the CRT and the voltage to be impressed to the video circuit.

The horizontal synchronous signal is impressed to pin 1 of IC301 to synchronize the pulse generated by the fly-back transformer (T302) and the phase-detected oscillation frequency with the synchronous signal.

The output signal of IC301 pin 7 turns ON/OFF the output transistor (X303) via the drive transformer (T301). The damper diode (D302) and this transistor operate as a switch to flow the sawtooth waveform deflection current in the deflection coil.

The horizontal amplitude is adjusted by changing the deflection current with the WIDTH COIL (L302) serially connected with the deflection coil.

The high screen voltage required for the CRT is also supplied by stepping up and rectifying with T302 the fly-back pulse generated when transistor X303 is turned OFF.

5.4 Controller

In the controller, all the functions centering around the 8-bit CPU are controlled by the program control system and incorporated into one logic PWB.

Fig. 5-4-1 shows the controller block diagram.

The controller consists of the CPU, CRT controller, and interface to be explained as follows.

In the following, the explanation of each unit component (such as an IC) is omitted unless otherwise required. For the details, see each user's manual.

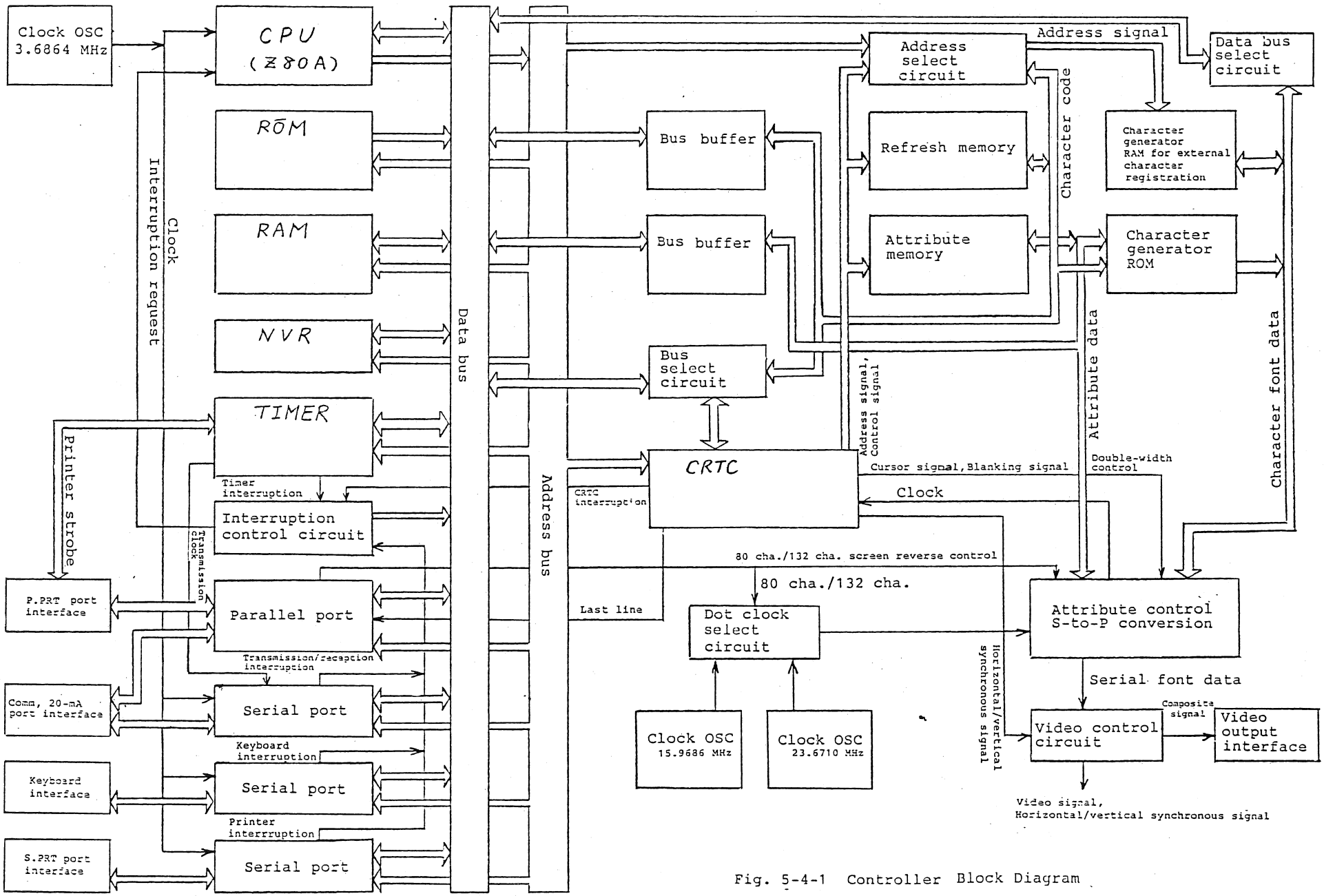


Fig. 5-4-1 Controller Block Diagram

1) CPU block

The CPU block consists of the data bus, the address bus, the bus control signal generator, EPROM, RAM, NVR (nonvolatile RAM), the memory chip select signal generator circuit, the I/O port chip select signal generator circuit, the timer, the CPU clock generator, the reset circuit, and the interruption control circuit centering around the 8-bit micro CPU (Z80A).

(1) CPU clock generator

The CPU clock generator oscillates the clock of 3.6864 MHz with the XTL1 OSC module. This clock is not only supplied to the CPU (Z80A) as the CPUCLK signal but also inputted to pin 11 of LS74A (Location 4B, The location is hereafter omitted.) and used to generate the $\overline{\text{WAIT}}$ signal for inserting an 1-clock WAIT into the M1 cycle of CPU. In addition, this is also used as the clock for the timer and that for the serial port.

(2) Reset circuit

The reset circuit consists of R34, C35, D3, LS14 (4F), and capacitors C33 and C34.

When the power supply is turned ON to supply +5V,

pin 11 of LS14 (4F) determined by R34 and C35 is changed from LOW to HIGH and the RES signal is outputted to pin 10 of LS14 (4F). Both the RES and $\overline{RES}$ signals are used to initialize the controller.

(3) Interruption control circuit

Z80A has two kinds of interruption, an $\overline{INT}$ interruption and an $\overline{NMI}$ interruption.

As the INT interruption, one of modes 0, 1, and 2 can be selected by the internal program. This equipment causes the $\overline{INT}$ interruption to control 5 kinds of interruption; the interface transmission/reception interruption (SRINT), CRTC interruption (CRTCINT), keyboard data transmission/reception interruption (KBINT), serial printer interface transmission/reception interruption (PRINT), and timer interruption (TINT).

The interruption control circuit consists of LS174 (3C), LS148 (3D), and LS244 (3B).

At the leading edge of $\overline{M1}$ signal inputted to pin 9 of LS174 (3C), the states of $\overline{TINT}$ (Timer interruption), $\overline{PRINT}$ (serial printer interface

transmission/reception interruption), $\overline{\text{KBINT}}$ (Keyboard data transmission/reception interruption), $\overline{\text{CRTCINT}}$ (CRTC interruption), and $\overline{\text{SPRINT}}$ (line-interface transmission/reception interruption) are latched and inputted to LS148 (3D).

If any of these interruption signals is active, interruption signals $\overline{\text{SRINT}}$, $\overline{\text{CRTCINT}}$, $\overline{\text{KBINT}}$, $\overline{\text{PRINT}}$, and $\overline{\text{TINT}}$ are encoded in 3 bits in this priority order and outputted to LS244 (3B).

At the same time, the $\overline{\text{INT}}$ signal (interruption request) is transmitted to the CPU.

When receiving the $\overline{\text{INT}}$ signal, the CPU outputs both the $\overline{\text{IORQ}}$ and $\overline{\text{M1}}$ signals simultaneously to make the $\overline{\text{INTA}}$ signal for pin 3 of LS32 (7M) active. As the result, pin 19 of LS244 (3B) becomes "L" and the interruption signals encoded by LS148 (3D) are outputted to CPU data buses D3 to D5 and read into the CPU to start a series of interruption processes.

Table 5-4-1 Interruption List

Interruption signal name		Program jump address	Interruption contents	Generation source	Interruption sense	Priority
$\overline{INT}$	$\overline{SRINT}$	08H	Line interface data transmission/ reception	Comm, 20mA port interface	"L" level sense	High ↑
	$\overline{CRTCINT}$	10H	Frame timer	CRTC		
	$\overline{KBINT}$	18H	Keyboard data transmission/ reception	Keyboard interface		
	$\overline{PRINT}$	20H	Serial printer data transmission/reception	S.PRT port interface		
	$\overline{TINT}$	28H	Programmable timer	TIMER		Low

(4) Bus control signal generator

The bus control signal generator controls the bus operation with the status control information from the CPU. For the relationship between the Z80A machine cycle and the state, see the Z80A User's Manual. The control signal generator generates the following control signals:

Signal name	Function
$\overline{IOR}$	Set to "L" when data is read from the I/O port.
$\overline{IOW}$	Set to "L" when data is outputted to the I/O port.
$\overline{RD}$	Set to "L" when data is read from memory or from I/O port.
$\overline{WR}$	Set to "L" when data is written to memory or outputted to the I/O port.
$\overline{IORQ}$	Set to "L" when the I/O port is accessed.
$\overline{MREQ}$	Set to "L" when memory is accessed.
$\overline{INTA}$	Set to "L" when the vector data for an interruption request is read.
$\overline{M1}$	Set to "L" when the machine cycle is the OP-code fetch cycle.

(5) EPROM

This is one 27256 EPROM(7H) and one 2764 EPROM(7F) of 40 K bytes. The VG-920 control program is written to this EPROM.

(6) RAM

This is a static RAM 6264 (7D) of 8 K bytes and used as the working area for the control program, the line interface received data buffer, the keyboard received data buffer, the print editing buffer, the stacking area, etc.

(7) NVR (Nonvolatile RAM)

NVR X2212 (7C) consists of a pair of a 256 x 4 bit RAM and a 256 x 4 bit EEPROM. When pin 9 ($\overline{\text{STORE}}$) is set to "L," the contents of the RAM are written to the EEPROM; when pin 10 ($\overline{\text{RECALL}}$) is set to "L," the contents of the EEPROM are read to the RAM.

NVR is used to store the Set Up information.

(8) Memory chip select signal generator circuit

This circuit consists of LS138 (3L), LS21 (2Ka), and LS08 (2Kb) and generates EPROM chip select signals $\overline{\text{ROMCS0}}$ to $\overline{\text{ROMCS1}}$, RAM chip select signal

$\overline{\text{RAMCS0}}$, NVR chip select signal $\overline{\text{RAMCS1}}$, and RAM chip select signal $\overline{\text{RAMCS2}}$ for external character registration.

Table 5-4-2 shows the VG-920 memory map.

(9) I/O port chip select signal generator circuit

This circuit causes LS154 (5C) to generate the chip select signal for the controller I/O port.

Table 5-4-3 shows the VG-920 I/O port address map.

(10) Timer

8253C-5 (5D) consists of three independent timers and operate with the CPU clock as the basic clock. It generates parallel printer strobe signal $\overline{\text{PRSTB}}$, Baud rate clock signal $\overline{\text{TSPEED}}$ for line-interface transmission data, and timer interruption signal $\overline{\text{TINT}}$ for software control, when accessed by the CPU.

2) CRT control block

The CRT control block consists of refresh memory, attribute memory, character generator, character generator for external character registration, dot clock generator, video control circuit, and their peripheral circuits, centering around CRTC (SCN2674BC4N

Table 5-4-2 VG-920 Memory Map

Address (Hexa-decimal code)	Size	Memory	Usage	Chip select signal	Area for use	Remarks
0000 ~ 7FFF	32K	ROM	Program	$\overline{\text{ROMCS0}}$	0000 ~ 7FFF	32K x 8 bits
8000 ~ 9FFF	8K	ROM	Program	$\overline{\text{ROMCS1}}$	8000 ~ 9FFF	8K x 8 bits
A000 ~ BFFF	8K	RAM	Working buffer or stacking area	$\overline{\text{RAMCS0}}$	A000 ~ BFFF	8K x 8 bits
C000 ~ DFFF	8K	NVR	Set Up information	$\overline{\text{RAMCS1}}$	C000 ~ C0FF	256 x 4 bits (4 low-order bits mounted)
E000 ~ FFFF	8K	RAM	Registration of external character patterns	$\overline{\text{RAMCS2}}$	E000 ~ E7FF	2K x 8 bits

Table 5-4-3 VG-920 I/O Port Address Map

Address (Hexa-decimal code)	Port select signal	Input/ Output	Usage	Data	Remarks
00 - 0F	$\overline{SCRTC}$	Input/ Output	Writing/reading data to/from the CRTC (SCN2674BC4N40: 1A) register	D0 - D7 (8 bits)	
10 - 1F	$\overline{STIM}$	Input/ Output	Writing/reading data to/from the timer (8253C-5: 5D) register	D0 - D7 (8 bits)	
20 - 2F	$\overline{STORE}$	Output	Writing the contents of the RAM for NVR (X2212: 7C) to the EEPROM	-	
30 - 3F	$\overline{RECALL}$	Output	Reading the contents of EEPROM for NVR to the RAM	-	
40 - 4F	$\overline{IOS}$	Input/ Output	Writing/reading data to/from the parallel port (8255A-5: 1M)	D0 - D7 (8 bits)	
50 - 5F	$\overline{GATE}$	Output	Transmitting the strobe signal to the parallel printer interface	-	
60 - 6F	Unused				
70 - 7F	Unused				
80 - 8F	$\overline{SCOM}$	Input/ Output	Writing/reading data to/from the line interface serial port register	D0 - D7 (8 bits)	
90 - 9F	$\overline{SPRT}$	Input/ Output	Writing/reading data to/from the serial printer interface serial port register	D0 - D7 (8 bits)	
A0 - AF	$\overline{SKB}$	Input/ Output	Writing/reading data to/from the keyboard interface serial port register	D0 - D7 (8 bits)	
BO - BF	Unused				
C0 - CF	Unused				
D0 - DF	$\overline{CDATA}$	Input/ Output	Writing/reading data to/from refresh memory	D0 - D7 (8 bits)	
E0 - EF	$\overline{ADATA}$	Input/ Output	Writing/reading data to/from attribute memory	D0 - D7 (8 bits)	
F0 - FF	Unused				

40: 1A) and attribute controller (SCB2675BC5N40: 1K). The CRT control block has the function to interface the CPU block and the CRT monitor of raster scan type. To display characters on the CRT screen, the CRT screen needs to be always scanned and refreshed. This equipment stores the character data codes to be displayed and the first memory address (line start address) for each display line in refresh memory (6264: 1E), and the contents to modify character data (reverse display, bold display, blink display, and underline display) and the character set select data in attribute memory (6264: 1C). It causes by CRTC to access both refresh memory and attribute memory simultaneously in order to refresh the CRT screen.

(1) Refresh memory

The 7-bit character data codes are written from the CPU to refresh memory via the bi-directional bus buffer (8X371: 2E). These codes cannot be displayed as characters on the screen as they are. Therefore, they need to be converted into the character patterns.

The character generator is used for this

conversion process. It generates a character pattern with the raster number and the character code as its address. The character pattern is read in parallel by dot patterns each for 1 character and 1 raster, converted into serial data by the attribute controller (SCB2675BC5N40: 1K), and displayed on the CRT screen.

(2) Attribute memory

Into attribute memory (6264: 1C), 4-bits attribute data (reverse display, bold display, blink display, and underline display) and 3-bit character set select data are read from the CPU via the bi-directional bus buffer (8X371: 2C). The 4-bit attribute data is sent to the attribute controller (SCB2675BC5N40: 1K) as ATT0 to ATT3 and used to modify the characters displayed on the screen.

ATT0: Specifies bold display.

ATT1: Specifies underline display.

ATT2: Specifies blink display.

ATT3: Specifies reverse display.

After being delayed for 1 character by LS273 (3A, 3E) as signals ATT5 to ATT7, the 3-bit character

set select data is sent to character generators 2764 (1F) and 6116 (2F) and used for select the display character set.

(3) CRTC

The major CRTC (SCN2674BC4N40:1A) function is to generate the timing signals required for the CRT monitor of raster scan type according to the specifications programmed by the CPU.

These timing signals generated by the CRTC are listed as follows:

- Address signals DADR0 to DADR12 to access both refresh memory and attribute memory
- Timing signals $\overline{\text{WDB}}$, $\overline{\text{RDB}}$, and $\overline{\text{BCE}}$ for data transmission/reception between refresh or attribute memory and the bi-directional bus buffer
- Raster addresses SL0 to SL3 transmitted to the character generators. (These are transmitted by time-dividing DADRs 4 to 7.)
- Horizontal and vertical synchronous signals (HSYNC nad VSYNC)
- Cursor control signal (CURS)
- Display time control signal (BLANK)

- Interruption request signal ($\overline{\text{CRTCINT}}$)
- Control signals (Double-width control, underline control, blink display control, and last line signals: These signals are transmitted by time-dividing DADRs 9 to 11 and DADR 13.)

Once these output signal functions are programmed by the CPU, they are automatically transmitted by the CRTC.

The CRTC consists of the following blocks:

1 Data bus driver block

This block is the interface between the external data bus and the internal CRTC bus.

2 Interface block

This block consists of the decoder for addresses A0 to A2 and the READ/WRITE circuit for the data to be transmitted/ received to/from the CPU.

3 Control block

This block decodes commands sent from the CPU and generates the signals to be sent to other blocks. It is also provided with the

initialization, command, interruption, and status registers to/from which data can be written/read from the CPU via the data bus driver and interface blocks.

4 Timing block

This block consists of the counter and the decoder circuit and generates the horizontal synchronous (HSYNC), vertical synchronous (VSYNC), and screen display time control (BLANK) signals.

5 Display block

This block consists of the circuit to generate address signals DADR0 to DADR12 to be outputted to both refresh memory and attribute memory, the circuit to generate raster address signals SL0 to SL3 to be outputted to the character generators, the scroll control circuit, the double-height control circuit, the cursor address register, the cursor control circuit, screen start registers 1 and 2, and the memory address control circuit.

6 Display handshake logic block

This block generates timing signals $\overline{\text{WDB}}$, $\overline{\text{RDB}}$,

and $\overline{BCE}$ required for data transmission/ reception between the CPU and refresh/attribute memory.

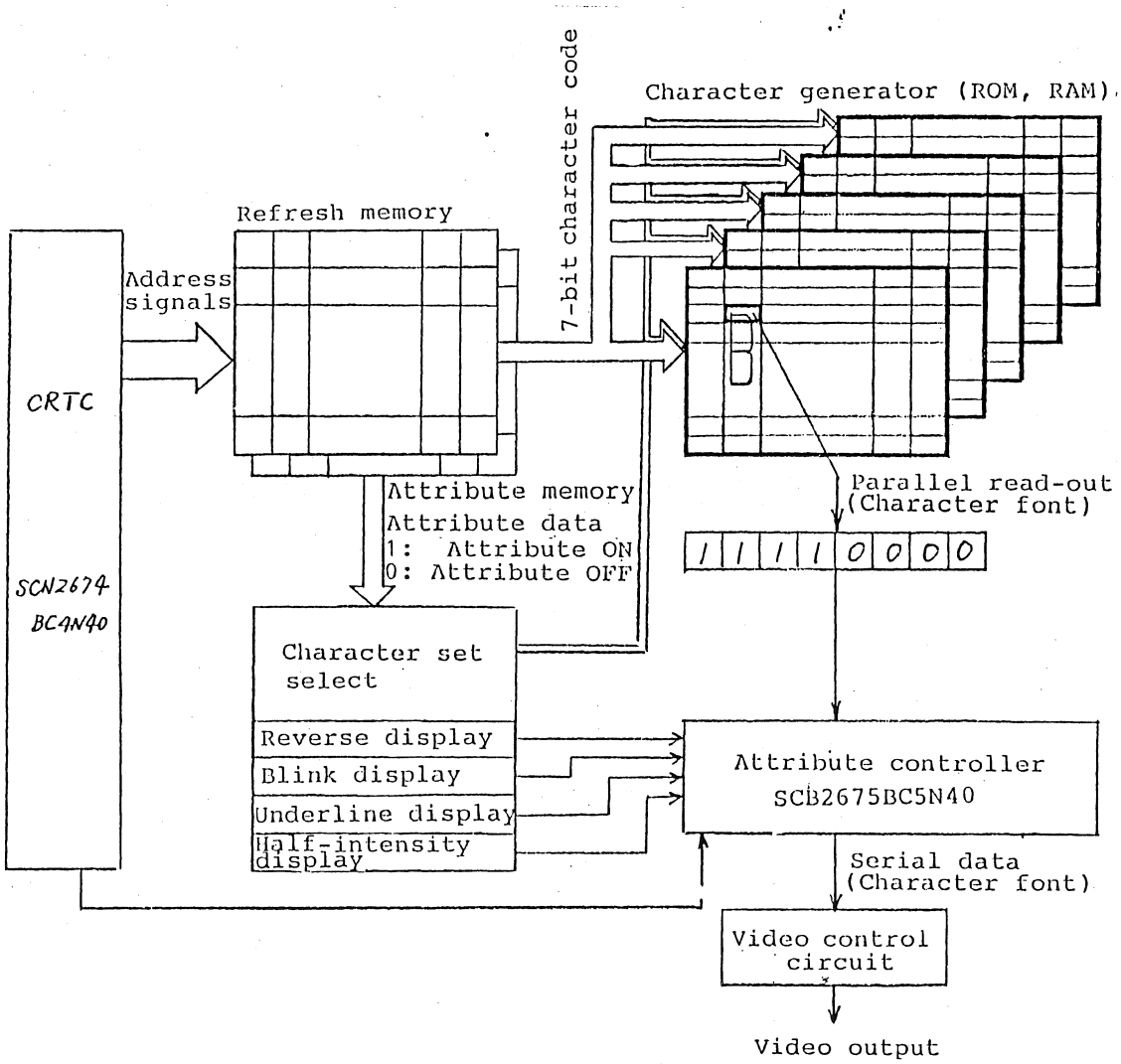


Fig. 5-4-2 Display Data Generation Processes

The display control of this equipment which employs this CRTC (SCN2674BC4N40) is shown as follows:

Scan mode: Non-interlace mode

Dot frequency: 15.9686 MHz (62.623 ns/dot) when operating at 80 characters/line
23.6710 MHz (42.246 ns/dot) when operating at 132 characters/line

Character font (Horizontal x Vertical):
7 x 10 dots (for single-height and single-width characters)
14 x 10 dots (for single-height and double-width characters)
14 x 20 dots (for double-height and double-width characters)

1-character block (Horizontal x Vertical):
10 x 10 dots (for 80 characters/line and single-height and single-width characters)
20 x 10 dots (for 80 characters/line and single-height and double-width characters)
20 x 20 dots (for 80 characters/

line and double-height and double-width characters)

9 x 10 dots (for 132 characters/line and single-height and single-width characters)

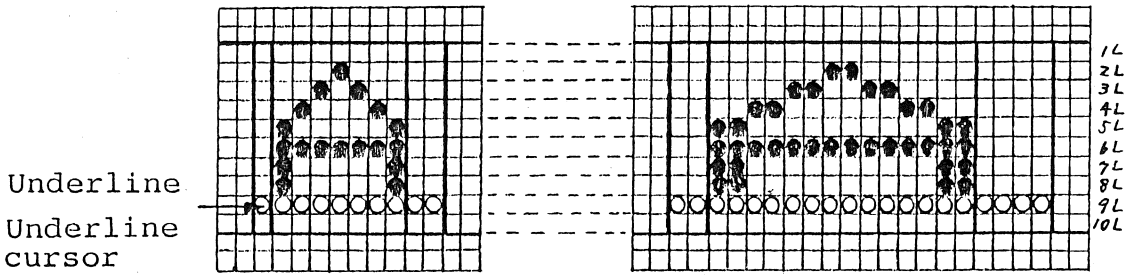
18 x 10 dots (for 132 characters/line and single-height and double-width characters)

18 x 20 dots (for 132 characters/line and double-height and double-width characters)

1-character frequency: 1.59686 MHz (626.23 ns/character) when operating at 80 characters/line

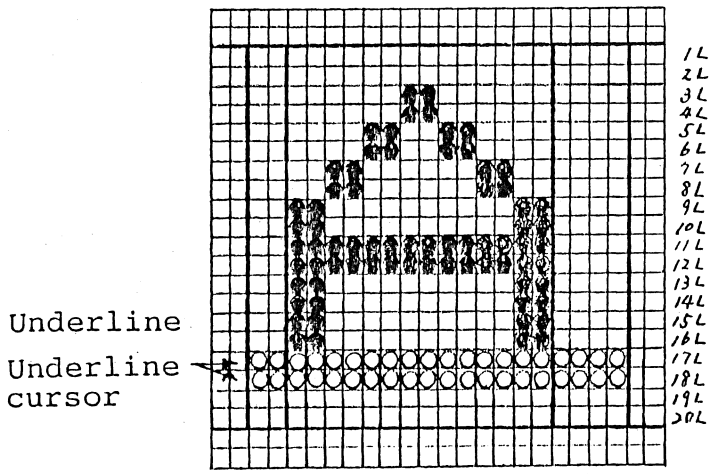
2.63011 MHz (380.21 ns/character) when operating at 132 characters/line

80 characters/line screen

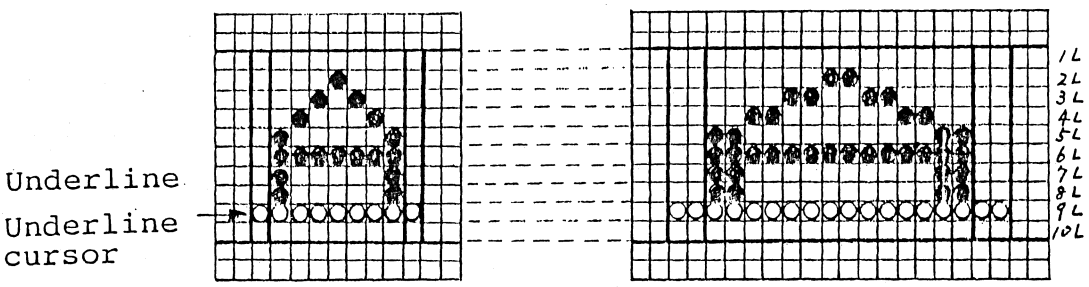


80 characters/line and single-height and single-width character

80 characters/line and single-height and double-width characters

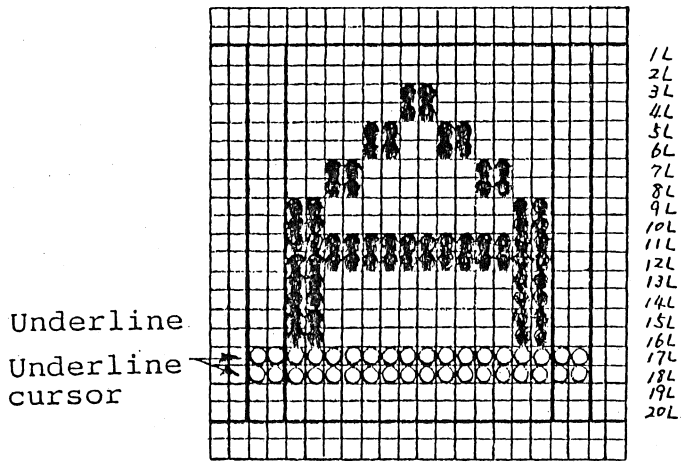


80 characters/line and double-height and double-width characters



132 characters/line and single-height and single-width character

132 characters/line and single-height and double-width character



132 characters/line and single-height and single-width character

Screen capacity: Max. 1920 characters (80 columns x 24 lines) when operating at 80 characters/line

Max. 3168 characters (132 columns x 24 lines) when operating at 132 characters/line

Deflection frequency

- At refresh rate 50 Hz
  - When operating at 80 characters/line

    Horizontal deflection frequency: 15.655 kHz (63.875 µs)

    Vertical deflection frequency: 50.018 Hz (19.993 ms)
  - When operating at 132 characters/line

    Horizontal deflection frequency: 15.655 kHz (63.876 µs)

    Vertical deflection frequency: 50.017 Hz (19.993 ms)
- At refresh rate 60 Hz
  - When operating at 80 characters/line

    Horizontal deflection frequency: 15.655 kHz (63.875 µs)

    Vertical deflection frequency: 59.983Hz

(16.671ms)

- When operating at 132 characters/line

  Horizontal deflection frequency: 15.655 kHz

  (63.876 μs)

  Vertical deflection frequency: 59.982 Hz

  (16.672 ms)

Horizontal synchronous signal pulse width:

When operating at 80 characters/line: 5.01 μs

When operating at 132 characters/line: 4.56 μs

Vertical synchronous signal pulse width:

When operating at 80 characters/line: 0.319 ms

When operating at 132 characters/line: 0.319 ms

Cursor blink cycle: 64-frame cycle

(4) Dot clock generation circuit

The dot clock generation circuit consists of the two kinds of clock generator for 80 characters/line and 132 characters/line screens.

The dot clock for the 80 characters/line screen oscillates at 15.9686 MHz with the XTL2 OSC module while the dot clock for 132 characters/line oscillates at 23.6710 MHz with the XTL3 OSC module.

(5) Dot clock select circuit

The output from the dot clock generation circuit is selected by the output from pin 39 of parallel port 8225A-5 (1M) at the S38 (4L) NAND gate. When the output from pin 39 is "H," the dot clock (23.6710 MHz) for 132 characters/line screen is selected; when it is "L," the clock for 80 characters/line (15.9686 MHz) is selected. Either of the above clocks is supplied to the attribute controller (SCB2675BC5N40: 1K).

(6) Character generators

The character generators are provided as the 8K byte EPROM (2764: 1F) and the 2K byte static RAM (6116: 2F).

The character fonts for the following hard character sets can be defined in the EPROM:

- ASCII character set
- U.K. National character set
- Special graphic character set
- Auxiliary character set

The character fonts for up to 94 characters can be defined by the user in the RAM as the Down Line Loadable character set.

From either of the above character generators,

the character font is read as 8-bit parallel data and supplied to the attribute controller (SCB2675BC5N40: 1K).

The character fonts defined in the EPROM corresponding to the character codes are listed in Tables 5-4-4 to 5-4-7.

Table 5-4-4 ASCII Character Set/CO Control

Character set select data b5:1 (ATT5:0)
b6:1 (ATT6:0)
b7:1 (ATT7:0)
CHAO to 6 CPU input/output data

Character Code data	b_6 b_5 b_4	1 1 1	1 1 0	1 0 1	1 0 0	0 1 1	0 1 0	0 0 1	0 0 0
b_3 b_2 b_1 b_0	CHA4 - 6 / CHAO - 3	0	1	2	3	4	5	6	7
1 1 1 1	0	N_U	D_L	(sp)	0	@	P	`	p
1 1 1 0	1	S_H	D_1	!	1	A	Q	a	q
1 1 0 1	2	S_X	D_2	"	2	B	R	b	r
1 1 0 0	3	E_X	D_3	#	3	C	S	c	s
1 0 1 1	4	E_T	D_4	$	4	D	T	d	t
1 0 1 0	5	E_Q	N_K	%	5	E	U	e	u
1 0 0 1	6	A_K	S_Y	&	6	F	V	f	v
1 0 0 0	7	B_L	E_B	'	7	G	W	g	w
0 1 1 1	8	B_S	C_N	(	8	H	X	h	x
0 1 1 0	9	H_T	E_M	)	9	I	Y	i	y
0 1 0 1	A	L_F	ς	*	:	J	Z	j	z
0 1 0 0	B	V_T	E_C	+	;	K	[	k	{
0 0 1 1	C	F_F	F_S	,	<	L	\	l	|
0 0 1 0	D	C_R	G_S	-	=	M	]	m	}
0 0 0 1	E	S_O	R_S	.	>	N	^	n	~
0 0 0 0	F	S_I	U_S	/	?	O	_	o	D_T

Table 5-4-5 Auxiliary Character Set/C1 Control Code

Character set select data b5:0 (ATT5:1)
b6:1 (ATT6:0)
b7:1 (ATT7:0)
CHAO to 6 CPU input/output data

Character Code data	b_6 b_5 b_4	1 1 1	1 1 0	1 0 1	1 0 0	0 1 1	0 1 0	0 0 1	0 0 0
b_3 b_2 b_1 b_0	CHA4 - 6 / CHAO - 3	0	1	2	3	4	5	6	7
1 1 1 1	0	8_0	9_0	A_0	°	À	D_0	à	F_0
1 1 1 0	1	8_1	9_1	¡	±	Á	Ñ	á	ñ
1 1 0 1	2	8_2	9_2	¢	²	Â	Ò	â	ò
1 1 0 0	3	8_3	9_3	£	³	Ã	Ó	ã	ó
1 0 1 1	4	8_4	9_4	A_4	B_4	Ä	Ô	ä	ô
1 0 1 0	5	8_5	9_5	¥	µ	Å	Õ	å	õ
1 0 0 1	6	8_6	9_6	A_6	¶	Æ	Ö	æ	ö
1 0 0 0	7	8_7	9_7	§	·	Ç	CE	ç	ce
0 1 1 1	8	8_8	9_8	¤	B_8	È	Ø	è	ø
0 1 1 0	9	8_9	9_9	©	¹	É	Ù	é	ù
0 1 0 1	A	8_A	9_A	ª	º	Ê	Ú	ê	ú
0 1 0 0	B	8_B	9_B	«	»	Ë	Û	ë	û
0 0 1 1	C	8_C	9_C	A_C	1/4	Ì	Ü	ì	ü
0 0 1 0	D	8_D	9_D	A_D	1/2	Í	Ý	í	ý
0 0 0 1	E	8_E	9_E	A_E	B_E	Î	D_E	î	F_E
0 0 0 0	F	8_F	9_F	A_F	¿	Ï	ß	ï	□

Table 5-4-6 Special Graphic Character Set

Character set select data b5:1 (ATT5:0)
b6:0 (ATT6:1)
b7:1 (ATT7:0)
CHAO to 6 CPU input/output data

Character Code data	b_6 b_5 b_4	1 1 1	1 1 0	1 0 1	1 0 0	0 1 1	0 1 0	0 0 1	0 0 0
b_3 b_2 b_1 b_0	CHA4 - 6 / CHAO - 3	0	1	2	3	4	5	6	7
1 1 1 1	0			(sp)	0	@	P	◆	—
1 1 1 0	1			!	1	A	Q	⁘	—
1 1 0 1	2			"	2	B	R	H_T	—
1 1 0 0	3			#	3	C	S	F_F	—
1 0 1 1	4			$	4	D	T	C_R	├
1 0 1 0	5			%	5	E	U	L_F	┤
1 0 0 1	6			&	6	F	V	°	┴
1 0 0 0	7			'	7	G	W	±	┬
0 1 1 1	8			(	8	H	X	N_L	│
0 1 1 0	9			)	9	I	Y	V_T	≤
0 1 0 1	A			*	:	J	Z	┘	≥
0 1 0 0	B			+	;	K	[	┐	π
0 0 1 1	C			,	<	L	, \	┌	≠
0 0 1 0	D			-	=	M	]	└	£
0 0 0 1	E			.	>	N	^	+	·
0 0 0 0	F			/	?	O	(sp)	—	

Table 5-4-7 Katakana Character Set

Character set select data b5:0 (ATT5:1)
b6:0 (ATT6:1)
b7:1 (ATT7:0)
CHAO to 6 CPU input/output data

Character Code data	b_6 b_5 b_4	1 1 1	1 1 0	1 0 1	1 0 0	0 1 1	0 1 0	0 0 1	0 0 0
b_3 b_2 b_1 b_0	CHA4 - 6 / CHAO - 3	0	1	2	3	4	5	6	7
1 1 1 1	0			(sp)	—	タ	ミ	E_0	F_0
1 1 1 0	1			。	ア	チ	ム	E_1	F_1
1 1 0 1	2	—		「	イ	ツ	メ	E_2	F_2
1 1 0 0	3			」	ウ	テ	モ	E_3	F_3
1 0 1 1	4			、	エ	ト	ヤ	E_4	F_4
1 0 1 0	5			・	オ	ナ	ユ	E_5	F_5
1 0 0 1	6			ヲ	カ	ニ	ヨ	E_6	F_6
1 0 0 0	7			ァ	キ	ヌ	ラ	E_7	F_7
0 1 1 1	8			ィ	ク	ネ	リ	E_8	F_8
0 1 1 0	9			ゥ	ケ	ノ	ル	E_9	F_9
0 1 0 1	A			ェ	コ	ハ	レ	E_A	F_A
0 1 0 0	B			ォ	サ	ヒ	ロ	E_B	F_B
0 0 1 1	C			ャ	シ	フ	ワ	E_C	F_C
0 0 1 0	D			ュ	ス	ヘ	ン	E_D	F_D
0 0 0 1	E			ョ	セ	ホ	゛	E_E	F_E
0 0 0 0	F			ッ	ソ	マ	゜	E_F	□

(7) Address select and data bus select circuits

The address select circuit consists of 3 LS157 chips 2J, 3J, and 3K and select the address signal to access the character generator RAM (6116: 2F) for external character registration. During the display period, the character generator RAM is accessed by the output from refresh memory (6264: 1E); on the other hand it is accessed by the address outputted from the CPU (Z80A: 6K).

During the display period, the BLANK signal outputted from the CRTC becomes "L" and inputted to pin 1 of LS157 (2J, 3J, and 3K) after delayed for 2 CRTCLK signal cycles. Delay signals DCHA0 to DCHA6 and raster addresses SL0 to SL3 are inputted to the RAM (6116:2F) addresses, and signal $\overline{\text{DATT7}}$ is inputted to $\overline{\text{OE}}$.

The character generator RAM (6116: 2F) becomes active when signal $\overline{\text{DATT7}}$ is "L" and outputs 8-bit font data in parallel to DOTs 0 to 7.

During blanking, the BLANK signal outputted from the CRTC becomes "H" and inputted to pin 1 of LS157 (2J, 3J, and 3K) after delayed for 2 CRTCLK

signal cycles. Address bus signals A0 to A10 outputted from the CPU are inputted to the character generator RAM (6116: 2F) addresses, signal $\overline{RD}$ is inputted to $\overline{OE}$.

At this time, if the CPU makes an access to memory area addresses E000 to FFFF, signal $\overline{RAMCS2}$ becomes active to start writing/reading data to/from the character generator RAM (6116: 2F).

The CPU's access to the character generator RAM is executed during blanking after waiting for the CRTC interruption caused by the $\overline{CRTCINT}$ signal.

The data bus select circuit consists of LS245 (3F) and connects the CPU data buses (D0 to D7) with the data signals (DOT0 to DOT7) outputted from the character generator RAM for selection of the data transmission/reception direction.

(8) Bus buffer

This equipment is provided with the two kinds of bus buffer; the bus buffer (8X371: 2E) for refresh memory and the bus buffer (8X371: 2C) for attribute memory. The bus buffer has the function to temporarily latch the data transferred between the CPU and refresh/attribute memory.

When the CPU makes an access to the I/O port, signal $\overline{\text{CDATA}}$ or $\overline{\text{ADATA}}$ becomes active and then the character codes are written to 8X371 (2E) or the attribute data and character set select data are written to 8X371 (2C).

Then, the CPU outputs the address data and the write command to the CRTC, and the CRTC makes both the address data and the $\overline{\text{WDB}}$ signal active to write the 8X371 (2E) latch data or the 8X371 (2C) latch data to refresh memory (1E) or attribute memory (1C).

To read the contents of refresh or attribute memory into the CPU, the CPU first outputs the address data and the read command to the CRTC. The CRTC waits for the timing for blanking and makes both the $\overline{\text{RDB}}$ and $\overline{\text{BCE}}$ signals active to write the contents of the specified memory address to 8X371 (2E, 2C). After confirming that the CRTC completes writing data to 8X371 with the contents of the CRTC register, the CPU makes an access to the I/O port to read the character data codes, attribute data, and character set select data.

(9) Bus select circuit

The CRTC reads the first memory address for the next display line from refresh memory during blanking immediately after displaying the last raster (scanning line 10 for each display line.) That is, the CRTC makes both the BLANK and CURS signals active simultaneously to supply refresh memory outputs CHA0 to CHA7 to the CRTC bus lines via LS244 (2B) and read these outputs. The bus select circuit controls the timing to supply CPU data bus signals (D0 to D7) and refresh memory outputs CHA0 to CHA7 to the CRTC data bus lines. This circuit consists of LS245 (2A) and LS244 (2B).

(10) Attribute controller

The main function of the attribute controller (SCB2675BC5N40: 1K) is to add attribute data to the character-font parallel data read from the character generator and output it as serial data. The attribute controller functions are listed as follows:

- The DOTCLK signal supplied from the dot clock select circuit causes the attribute controller to perform internal control and

at the same time, it is frequency-divided to generate the $\overline{\text{CRTCLK}}$ signal for CRTC control. It is frequency-divided by 10 (when the 132CHA signal is "L") when the equipment operates at 80 characters/line; by 9 (when the 132CHA signal is "H") when the equipment operates at 132 characters/line.

- Signals DOT0 to DOT7 outputted from the character generator are expanded into 9-bit data and supplied to pins D0 to D8 to output character-font serial data signals TTLV1 and TTLV2.

  If the DOT0 signal outputted from the character generator is "H," the contents of the DOT1 signal and those of the DOT7 signal are inputted to D8 and D0, respectively, in order to control the graphic patterns of the special graphic character set so as to link them horizontally. On the other hand, if the DOT0 signal is "L," the "L" level signals are supplied to D8 and D0 so that the graphic patterns are not linked horizontally.

- The DADR10 signal specifies the scan line to

display an underline; the ATT1 signal specifies the characters to be underlined.

- o The DADR11 signal specifies the blinking cycle; the ATT2 signal specifies the characters to be blinked.
- o The ATT3 signal specifies the characters to be displayed in reverse.
- o The CURS signal causes the cursor data to be added to character-font serial data signals TTLV1 and TTLV2.
- o The DOUBLE signal specifies the horizontally magnified character.
- o The REVSCN signal causes the entire display screen to be displayed in reverse.
- o The ATT0 signal specifies bold display.

(11) Video control circuit

Signals TTLV1 and TTLV2 outputted from the attribute controller and the HSYNC and VSYNC signals outputted from the CRTC generate composite VIDEO SIGNAL and TTL Level Separate Video signals.

3) Interface block

The interface block consists of the parallel printer interface, COMM interface, 20mA current loop interface, serial printer interface, keyboard interface, and video output interface, centering around the parallel port block (8255A-5) and the three serial ports (SCN2641CCIN24).

(1) Parallel port

The parallel port block (8255A-5: 1M) consists of three 8-bit parallel ports (ports A, B, and C). Ports A, B, and C are used to output the control signals, input the control signals, and output the parallel printer data, respectively.

Table 5-4-8 shows the function of each input/output terminal of the parallel port.

Table 5-4-8 Parallel Port Input/Output Terminal Functions

Port No.	Pin No.	Input/ Output	Signal Name	Function
PA0	4	Output	COMDR	Set the COMM interface DTR signal turn ON when "H".
PA1	3	Output	SPDS	Set the COMM interface SPDS signal turn ON when "H".
PA2	2	Output	(RREDY)	Stand-by.
PA3	1	Output	$\overline{\text{DCDCTL}}$	Controls the COMM interface RLSD signal.
PA4	40	Output	$\overline{\text{EIA}}$	Selects the COMM interface when "L"; the 20mA interface when "H".
PA5	39	Output	132CHA	Selects the 132 characters/line operation when "H"; the 80 characters/line operation when "L".
PA6	38	Output	REVSCN	Selects the reverse screen display when "H".
PA7	37	Output	N.C	Unused.
PB0	18	Input	DSR	Indicates that the COMM interface DSR signal is turned ON when "H."
PB1	19	Input	SPDI	Indicates that the COMM interface SPDI signal is turned ON when "H."
PB2	20	Input	COMCS	Indicates that the COMM interface CTS signal is turned ON when "H."
PB3	21	Input	N.C	Unused.
PB4	22	Input	(TP1)	For internal alignment.
PB5	23	Input	LL	Indicates that the last raster of each line (SCANNING line 10) is being displayed when "H".
PB6	24	Input	$\overline{\text{PBUSY}}$	The inverted parallel printer busy signal output is inputted.
PB7	25	Input	PACK	The latch signal for the parallel printer acknowledge signal is inputted.

Port No.	Pin No.	Input/ Output	Signal Name	Function
PC0	14	Output	(PD0)	These are buffered by LS244 (1N) and outputted to the parallel printer as data signals PD0 to PD7.
PC1	15	Output	(PD1)	
PC2	16	Output	(PD2)	
PC3	17	Output	(PD3)	
PC4	13	Output	(PD4)	
PC5	12	Output	(PD5)	
PC6	11	Output	(PD6)	
PC7	10	Output	(PD7)	

(2) COMM/20 mA port interface

Either the COMM port or the 20mA port is selected in the Communication Set Up.

It is selected by switching the signal line with LS32 (4K), S38 (4L), and LS02 (4J) by using the $\overline{\text{EIA}}$ signal outputted from parallel port (8255A-5: 1M) PA4, the $\overline{\text{DCDCTL}}$ signal outputted from parallel port PA3, and the $\overline{\text{CTSCTL}}$ signal outputted from the S.PRT port (SCN2641CCIN24: 5F).

The data signal (COMSD/COMRD) transmitted/received to/from this port connects with the CPU bus via the serial port (SCN2641CC1N24:5H) so that the CPU is able to set the data length and the parity and stop bits programmably for the serial port (SCN2641CC1N24: 5H). At this serial port, the data transmitting/receiving rate can be independently set. The data transmitting rate can be determined by supplying the $\overline{\text{TSPEED}}$ signal outputted from the timer (8253C-5: 5D); the data receiving rate can be determined by frequency-dividing the CPUCLK signal according to the internal resistor value in the serial port.

(3) S.PRT port interface

The data signal (PRTSD/PRTRD) transmitted/received to/from this port connects with the CPU bus via the serial port (SCN2641CC1N24: 5F), and the CPU is able to set the data length and the parity and stop bits programmably for the serial port (SCN2641CC1N24).

The data trasmitting/receiving rate can be determined by frequency-dividing the CPUCLK signal according to the internal register in the serial port.

(4) Keyboard interface

The data signal (KBSD/KBRD) transmitted/received to/from the keyboard connects with the CPU bus via the serial port (SCN2641CC1N24: 5E), and the CPU is able to set the data length and the parity and stop bits programmably for the serial port (SCN2641CC1N 24: 5E). The data trasmitting/receiving rate can be determined by frequency-dividing the CPUCLK signal according to the internal register value in the serial port.

(5) Video output interface

The TTL-level separate video signals (VIDEO, HSYNC, and VSYNC) are supplied to the monitor block via the J308 connector and displayed on the

CRT screen.

The composite video signal (COMPV) are supplied to the J305 connector and can be connected with the external UNIT.

5.5 Keyboard block

The keyboard block consists of the capacitive key switch, key switch scanning circuit, indicator LEDs, bell circuit, etc., centering around the single-chip CPU8749 or 8049 (Z4), and connects to the DP-920 display unit controller block with the curl cord.

The following commands are sent from the controller block to the keyboard block as the TTL-level serial data in the start-stop Asynchronous system:

- Auto repeat speed control command
- Initialize command
- LED control command
- Key-click/bell control command
- Keyboard status request command

The following codes are sent from the keyboard block to the controller block as the TTL-level serial data in the start-stop Asynchronous system:

- Key code
- Initialize sequence code
- Status code

The keyboard block has the following specifications:

- Keytop arrangement: Main keypad, editing keypad, auxiliary keypad, and Top-Row function keypad
- Number of keys: 106 keys
- Keytop inclination: Step sculpture
- Key movement: 4±0.5 mm
- Key row offset: 9.5 - 4.75 - 9.5 mm
- Key structure: : Low-profile type, capacitive keyboard
- Roll over: N-key roll over
- Repeat function: Auto repeat (when pressing a key for more than 0.5 second)
- Data format: Start-stop Asynchronous system
  1 start bit
  8 data bits
  1 stop bit
- Data transfer rate: 4800 bps

- Input/output signal

Input/output signal name		Cable logic	Signal direction KB block ↔ Controller block	DIN connector pin No.	Remarks
KBRD	Start bit	Positive logic	→	1	
	Data bit	Negative logic			
	Stop bit	Negative logic			
$\overline{\text{KBBSY}}$		Negative logic	→	5	
KBSD	Start bit	Positive logic	←	4	
	Data bit	Negative logic			
	Stop bit	Negative logic			
$\overline{\text{KBRTS}}$		Negative logic	←	2	

6. DISASSEMBLY AND REPLACEMENT

CAUTION: Be sure to turn OFF the POWER switch and pull out the power cable from the plug receptacle before disassembling or replacing this equipment.

6.1 Disassembly and Replacement of Display Unit

Fig. 6-1-1 shows the disassembly diagram of display unit DP-920.

1) Removal of the logic PWB (No. 1)

(1) Turn OFF the POWER switch and remove the power cord and the keyboard cable on the back and front of the display unit, respectively.

(2) Remove the two screws (Part E: No. 2) on the back of the display unit.

(3) Remove the two connectors (P307 and P308) on the logic PWB. (See Fig. 6-1-2.)

(4) Pull out the logic PWB by pushing it up.

2) Removal of the rear cabinet (No. 3)

(1) Remove the logic PWB according to the procedures described in 1).

(2) Cover the solid stand surface with a soft cloth and place the display unit quietly with the CRT surface down.

(3) Remove the two screws (Part C: No. 4) on the back of display unit.

(4) Remove the two screws (Part D: No. 5) on the back of display unit.

(5) Remove the two tapping screws (Part F: No. 6) on the side of display unit.

(6) Remove the two tapping screws (Part G: No. 7) on the bottom of display unit.

(7) Pull up the rear cabinet.

3) Removal of the power bracket (No. 8)

(1) Remove the logic PWB and the rear cabinet according to the procedures described in 1) and 2).

(2) Remove the J102 connector (10 P) of the switching power supply. (See Fig. 6-1-3.)

(3) Remove the cable from the two cable clamps on the power bracket. (See Fig. 6-1-3.)

(4) Remove the two tapping screws (Part A: No. 9). (See Fig. 6-1-1.)

(5) Remove the tapping screw (No. 10). (See Fig. 6-1-1.)

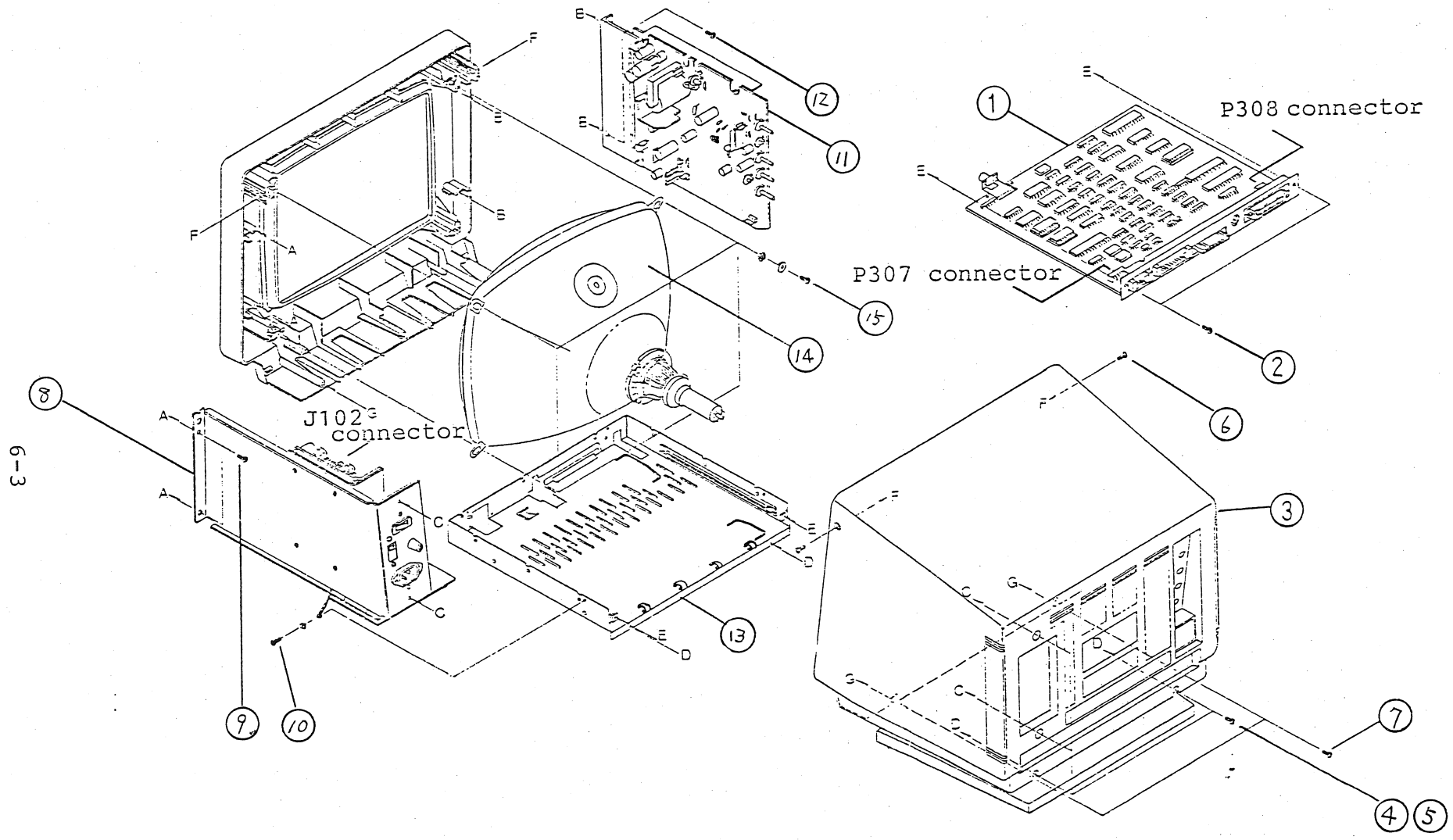


Fig. 6-1-1 Display Unit Disassembly Diagram

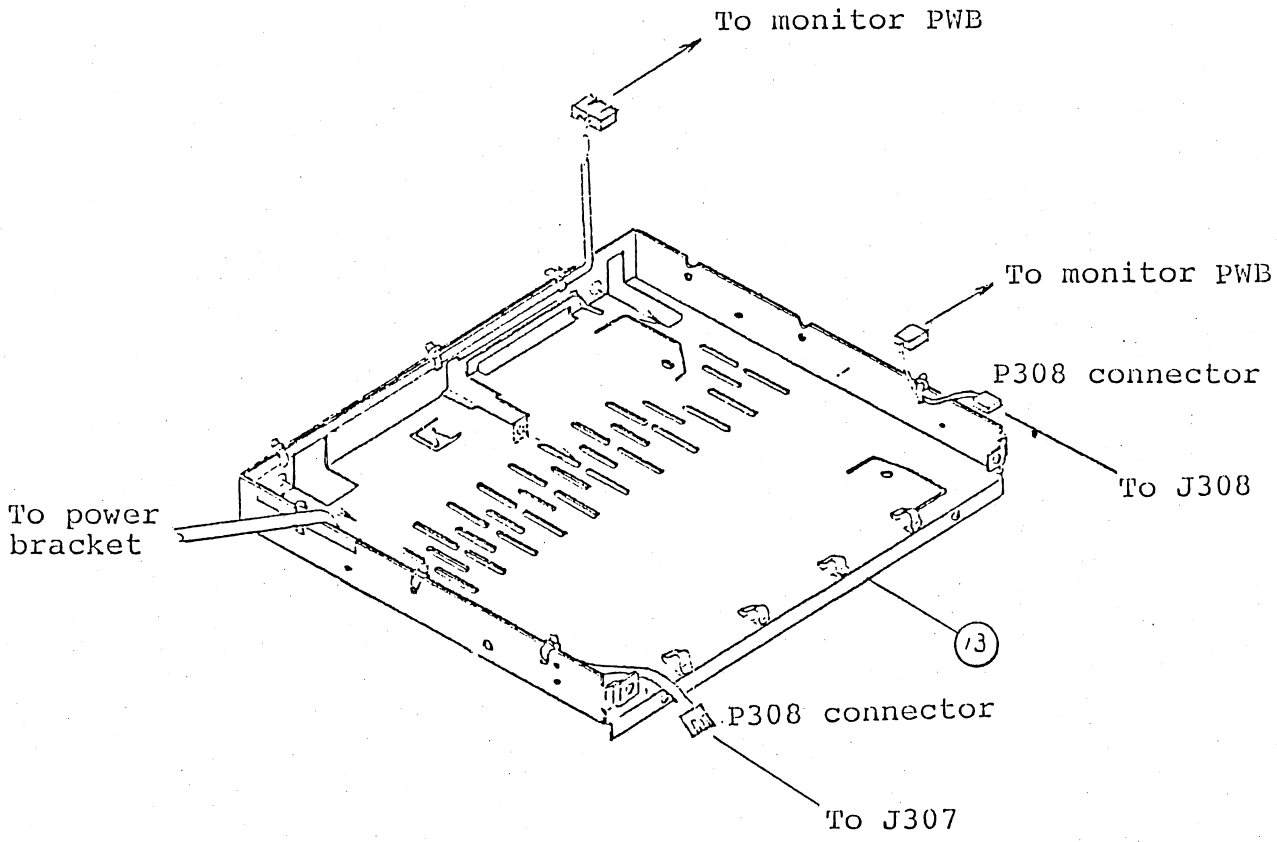


Fig. 6-1-2 Removal of Logic PWB

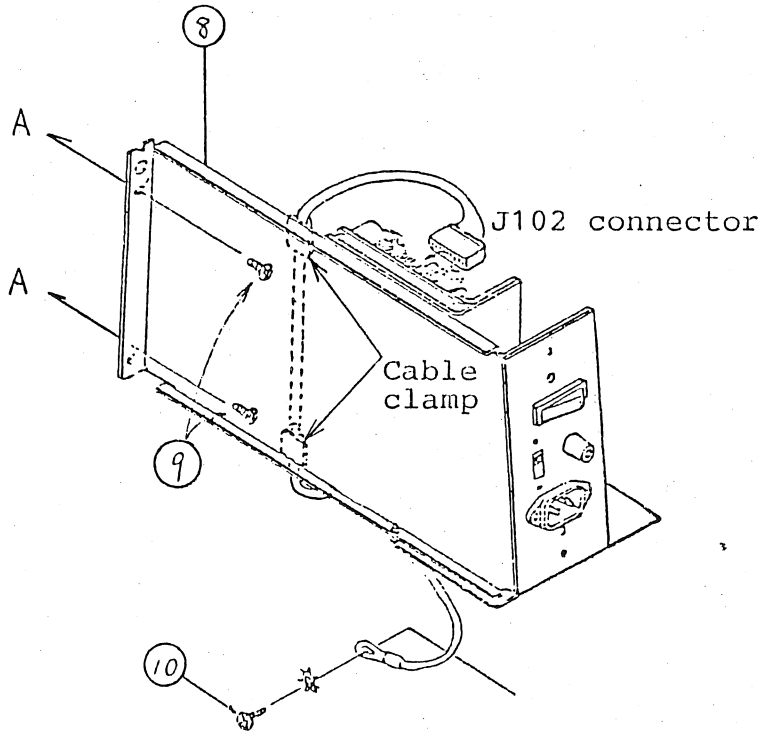


Fig. 6-1-3 Removal of Power Bracket

4) Removal of monitor PWB (No. 11)

(1) Remove the J6 connector (5P) on the monitor PWB. (See Fig. 6-1-5.)

(2) Remove the SG connector (3P) of the CRT SOCKET PWB. (SEE FIG. 6-1-5.)

(3) Pull out the CRT SOCKET PWB from the CRT neck.

(4) Remove the J1 connector (3P), J3 connector (5P), and J5 connector (2P) on the monitor PWB. (See Fig. 6-1-6.)

(5) Remove the anode cap from the CRT. (See Fig. 6-1-4.)

CAUTION

Remove the anode cap after discharging the high-voltage electricity from the CRT by shortcircuiting the CRT anode cavity and the CRT mounting lug with a clip wire.

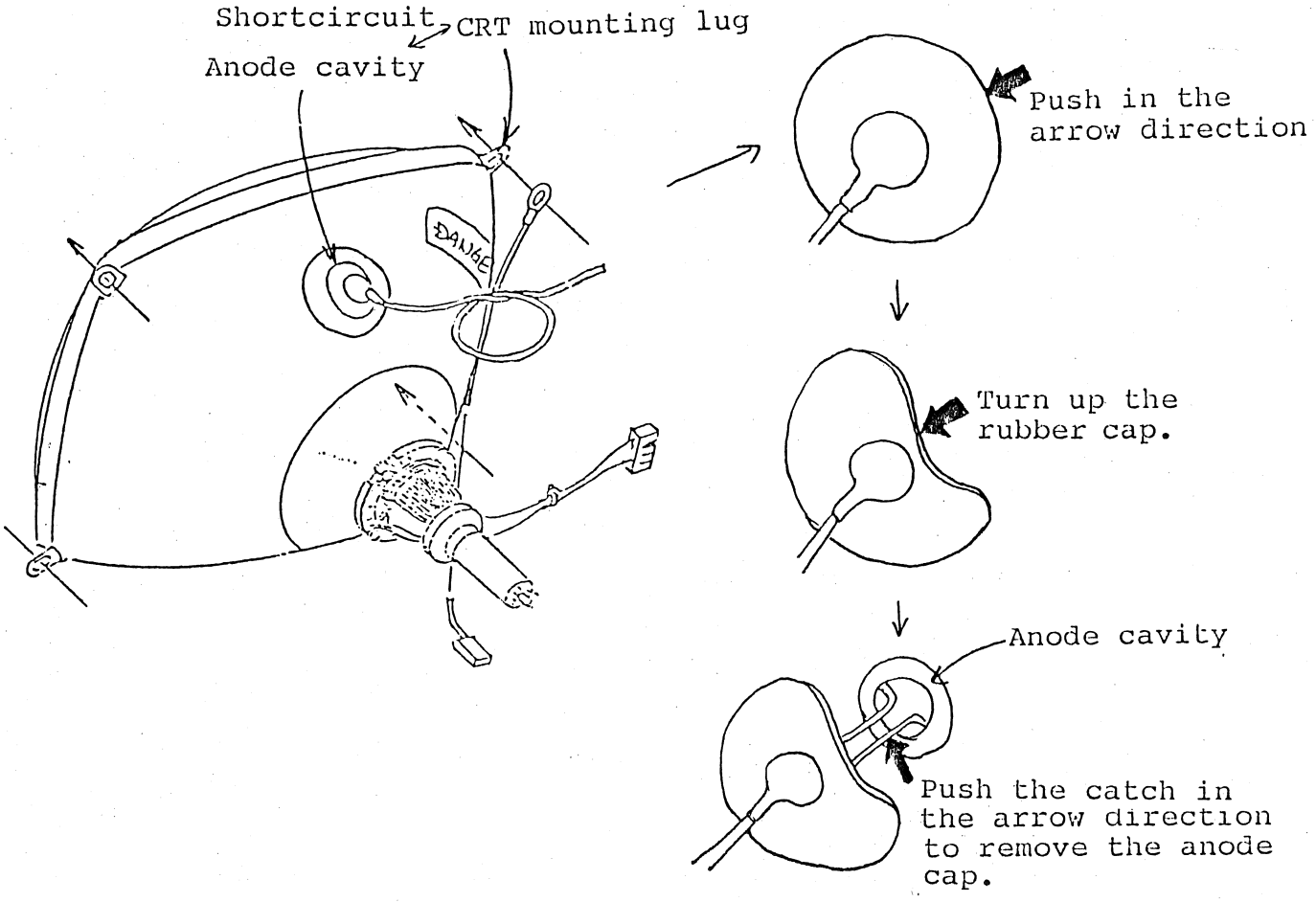


Fig. 6-1-4 Removal of Anode Cap

(6) Remove the two tapping screws (Part B: No. 12).

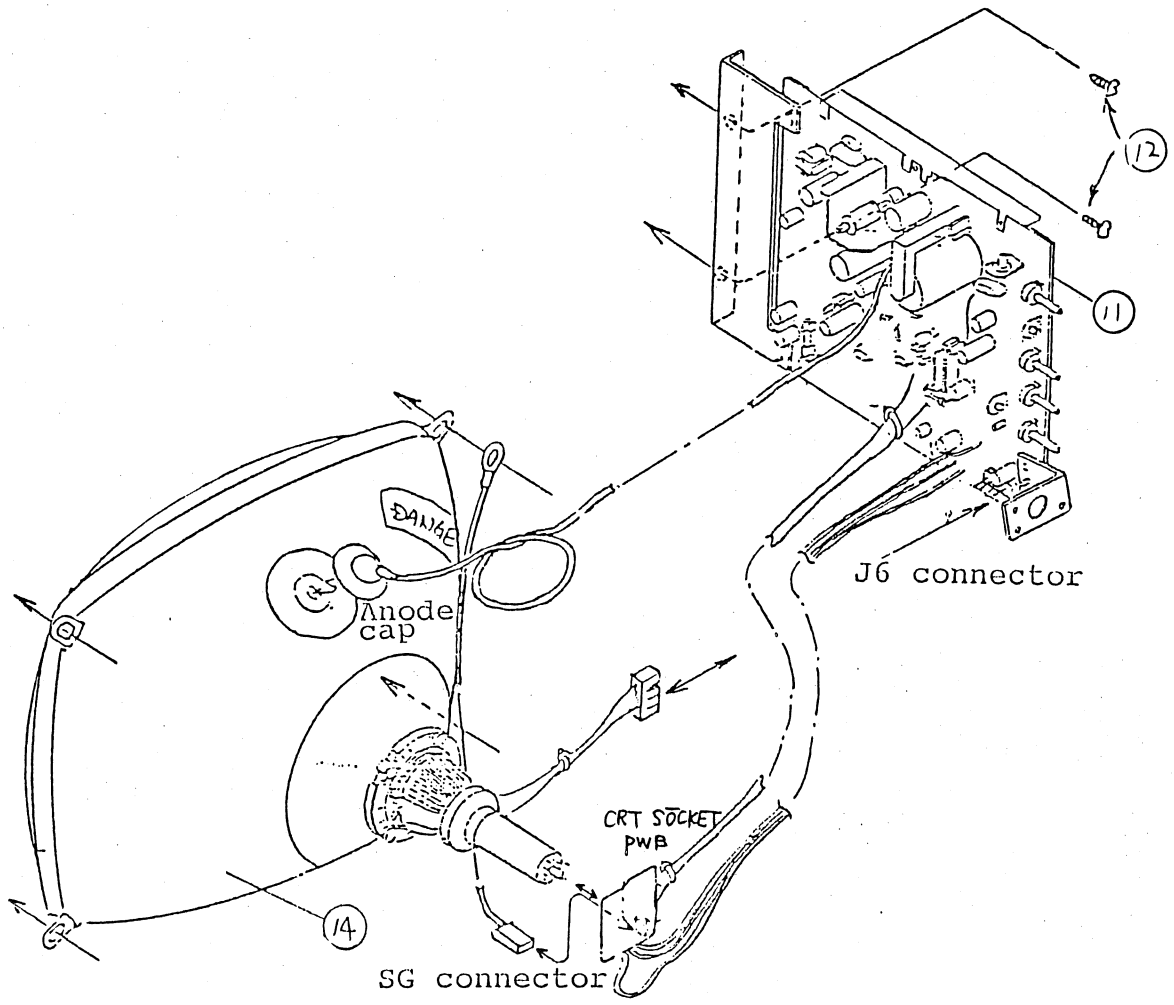


Fig. 6-1-5 Removal of Monitor PWB

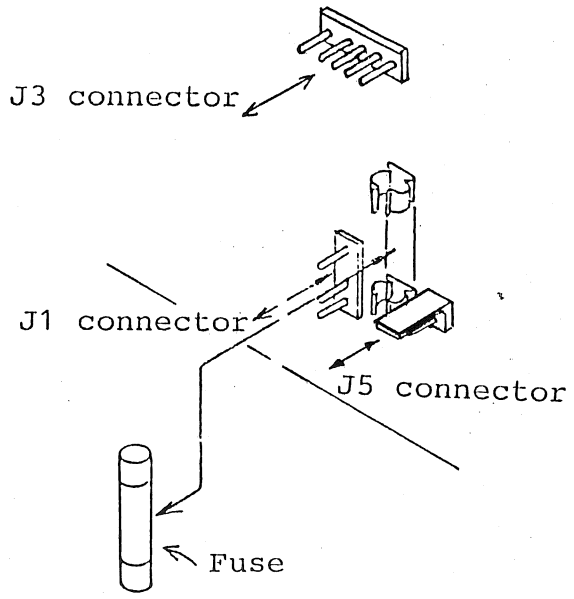


Fig. 6-1-6 Removal of Monitor PWB

5) Removal of PWB CASE ASY (No. 13)

(1) Remove the logic PWB and the rear cabinet according to the procedures described in 1) and 2).

(2) Remove the J102 connector according to the procedures described in (2) and (3) of 3) and remove the cable from the cable clamp.

(3) Remove the J6 connector (5P) according to the procedures described in (1) of 4).

(4) Remove the J1 connector (3P) according to the Procedures described in (4) of 4).

(5) Pull out the PWB CASE ASY toward the CRT neck.

6) Removal of the CRT ASY (No. 14)

(1) Remove the logic PWB, rear cabinet, power bracket, monitor PWB, and PWB CASE ASY according to the procedures described in 1) through 5).

(2) Remove the four tapping screws (No. 15).

(3) Remove the CRT ASY. Cover the solid stand surface with a soft cloth and place the CRT ASY quietly with the CRT surface down.

CAUTION

It is dangerous to shock the CRT corn part. Take care so as not shock the removed CRT ASY.

6.2 Disassembly and Replacement of Keyboard Unit

Fig. 6-2-1 shows the disassembly diagram of keyboard unit KB-920.

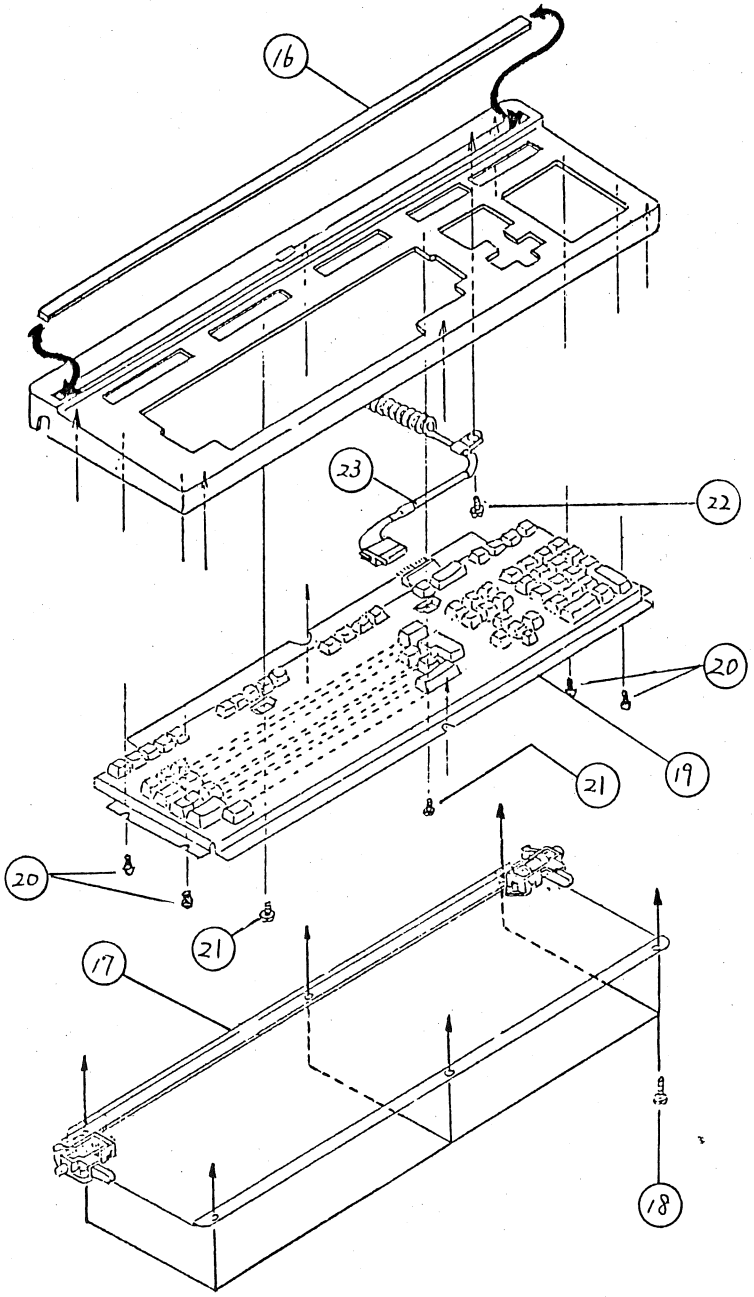


Fig. 6-2-1 Keyboard Unit Disassembly Diagram

1) Removal of the function plate (No. 16)

(1) Pull out the function plate so as to pull up its center.

2) Removal of the bottom panel (No. 17)

(1) Cover the solid stand surface with a soft cloth and place the keyboard unit quietly with the keytop surface down.

(2) Remove the six tapping screws (No. 18) on the keyboard bottom. (See Fig. 6-2-1.)

(3) Pull up the bottom panel.

3) Removal of the keyboard PWB (No. 19)

(1) Remove the bottom panel according to the procedures described in 2).

(2) Remove the four tapping screws (No. 20) from the keyboard soldered surface. (See Fig. 6-2-2.)

(3) Remove the two tapping screws (No. 21) from the keyboard soldered surface. (See Fig. 6-2-2.)

(4) Remove the tapping screw (No. 22) from the keyboard soldered surface. (See Fig. 6-2-2.)

(5) Pull up the keyboard PWB.

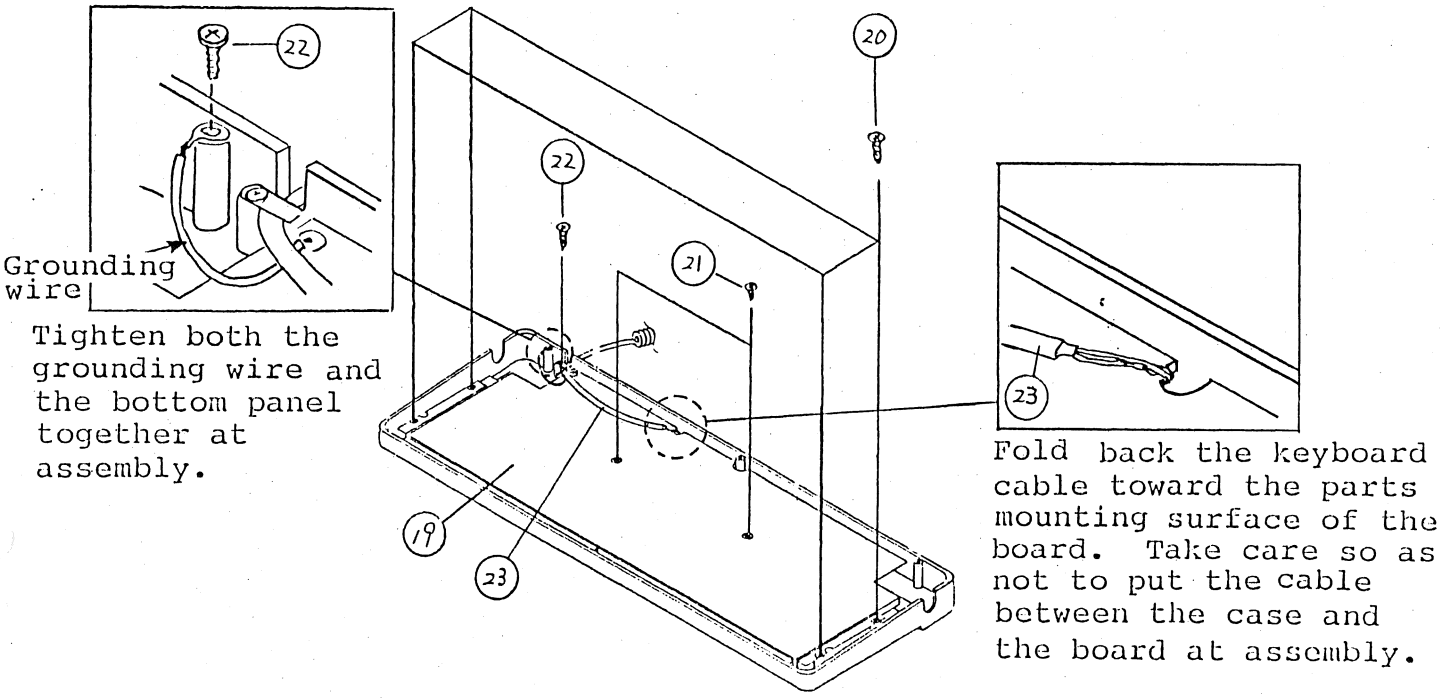


Fig. 6-2-2 Removal of Keyboard PWB

4) Removal of the keyboard cable (No. 23)

(1) Remove the keyboard PWB according to the procedures described in 2) and 3).

(2) Pull out the keyboard cable holding the housing of the 9-pin keyboard cable connector.

7. ADJUSTMENT

7.1 Adjustment Points

The display unit has the following two adjustment points:

(1) +5V power supply voltage

(2) Monitor screen

The above points have already been adjusted at the factory shipment. Therefore, do not touch any part other than the user control knob of the monitor unit unless otherwise required.

1) +5V power supply voltage adjustment

Item	Procedure (Condition)	Standard	Tool & Measuring instrument
+5V power supply voltage adjustment	1) Check that the keyboard is connected with the display unit. 2) Turn ON the power. 3) Adjust the +5V Adj volume (VR) on the power supply PWB so as to set the voltage between J307 connector pins 1 (+5V) and 4 (SG) on the logic PWB to the standard value.	+5.07~ +5.08V	Tester (DC voltage meter, Digital volt meter)

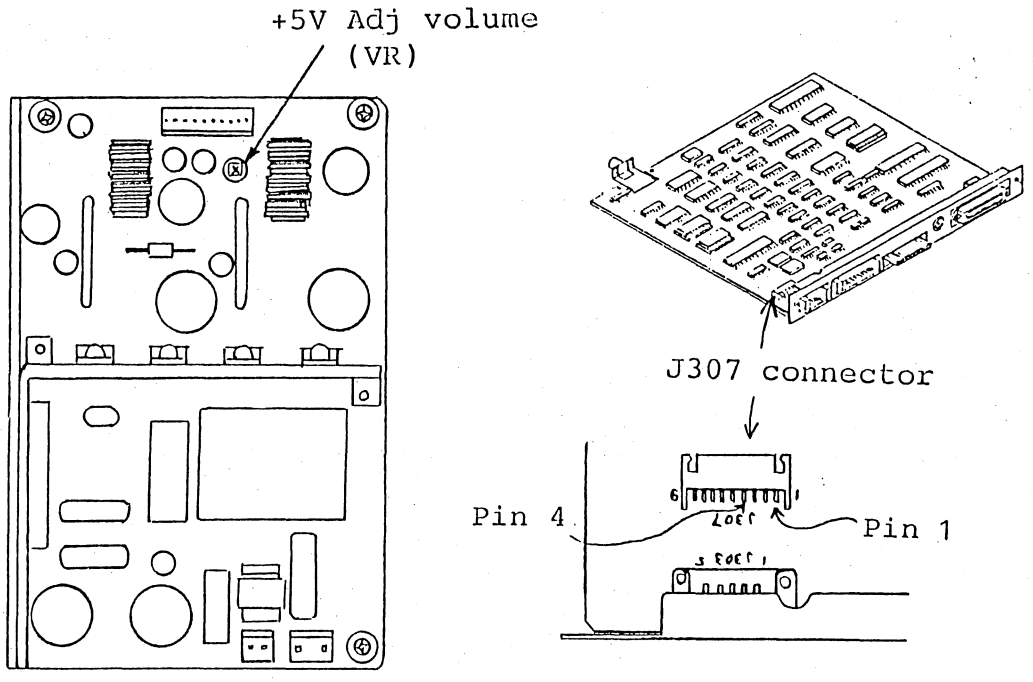


Fig. 7-1-1 +5V Power Supply Voltage Adjustment

2) Monitor screen adjustment

The monitor is adjusted with the user control knobs, service-man control knobs, centering magnet, etc.

Table 7-1-1 lists the adjusting instruments. The class column with an asterisk indicates user control; that without an asterisk indicates service-man control. Be sure to adjust these instruments accoording to the adjustment procedures.

Each adjusting instrument operates as described below when it is turned clockwise:

Table 7-1-1 Monitor Unit Adjustment

No.	Control class	Name	Wiring diagram symbol	Operation contents
1	*	BRIGHT	R326	Both the raster and picture become bright.
2	*	CONTRAST	R106	The picture becomes bright.
3	*	V. HOLD	R204	The picture distorts vertically
4	*	H. HOLD	R312	The picture distorts slantly to the right or left.
5		V. HEIGHT	R210	The picture expands vertically.
6		V. LIN	R209	The upper part of the picture extends; the lower part of the picture shrinks.
7		FOCUS	R321	The picture center is defocused and the picture corners are focused.
8		SUB.BRIGHT	R325	Both the raster and picture become bright.
9		WIDTH COIL	L302	The raster horizontally shrinks.
10		CENTERING MAGNET		Adjusts the raster so as to be positioned in the CRT center.
11		CORRECTION MAGNET		Adjusts the distortion of the picture

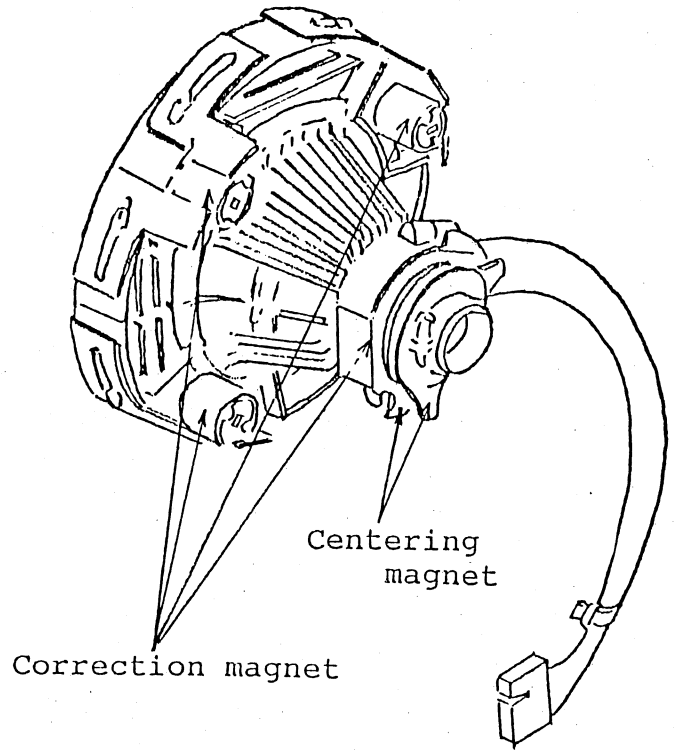


Fig. 7-1-2 Monitor Adjustment Points

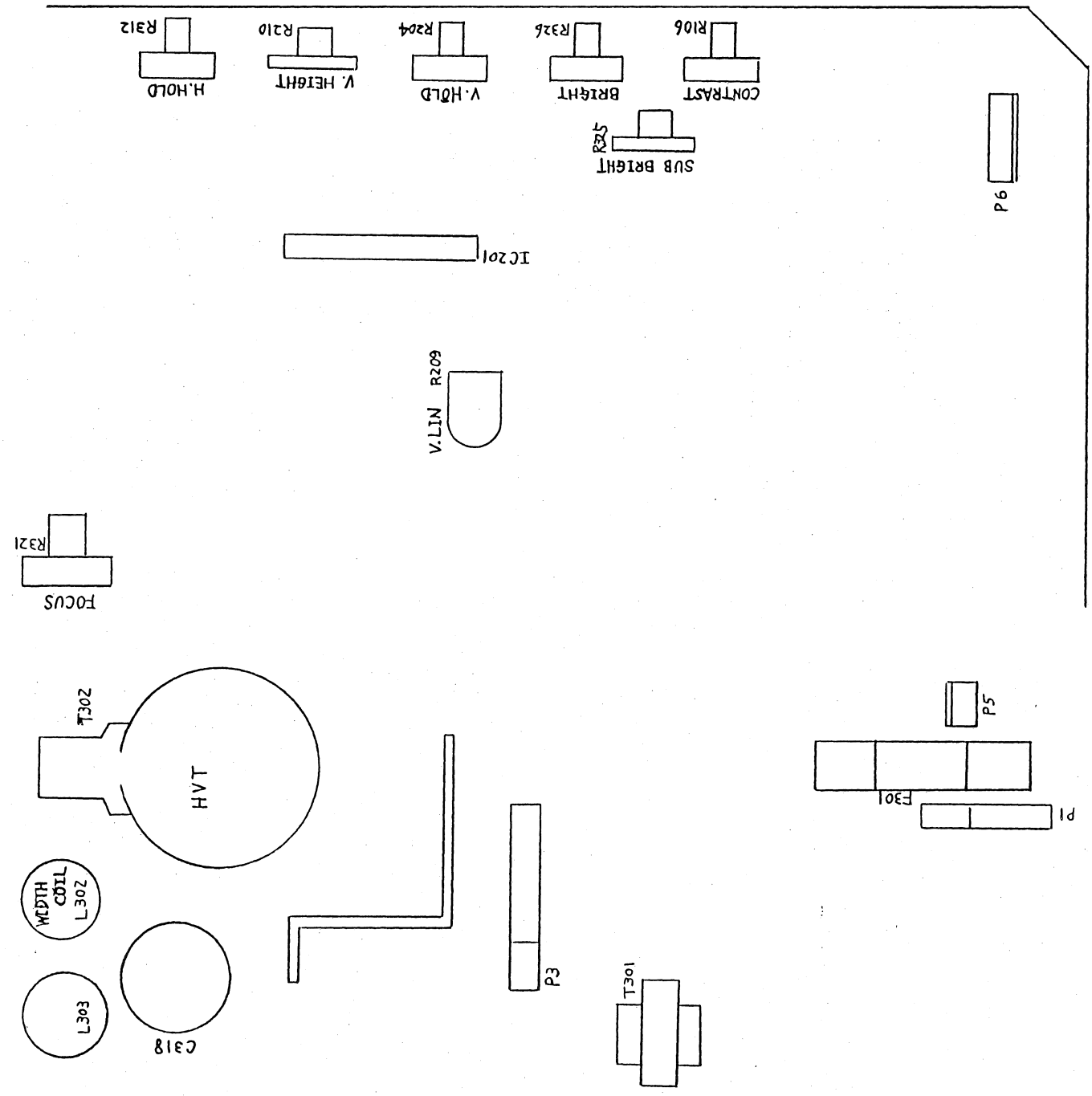


Fig. 7-1-3 Monitor Adjustment Points

(1) Adjustment conditions

Be sure to understand the position of each adjusting instrument and its operation contents with Table 7-1-1 and Figures 7-1-2 and 7-1-3.

For adjustment, "H" is keyed in from the keyboard unit and displayed on the entire screen.

The following shows how to display "H" on the entire screen:

① Turn ON the power when the display unit is connected with the keyboard unit.

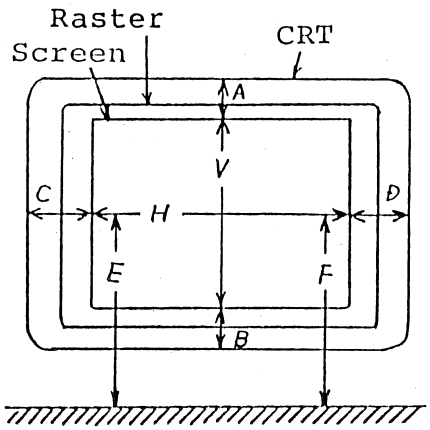
② Select the Set Up Directory (Setting guide) menu by inputting the [Set Up] key and select Local.

③ Next, select the Display Set Up menu and select Interpret Controls.

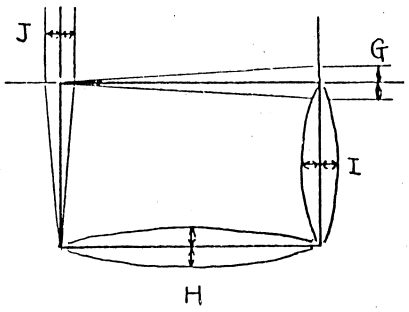
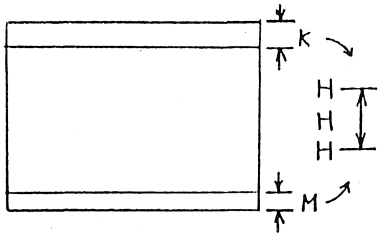
④ Input the [Set Up] key to cancel the Set Up mode.

⑤ Input [Ctrl] + [[], [Shift] + [#], and [8].

(2) Adjustment procedures

No.	Item	Procedure (Condition)	Wiring diagram symbol	Standard	Tool and measuring instrument
1		Set each knob to the center of the rotary angle temporarily.			
2	Horizontally synchronous adjustment	Turn H.HOLD and set picture at the raster center.	R312	Service-range center	
3	Vertically synchronous adjustment	Turn V.HOLD to set the picture at the center of the service range.	R204	Service-range center	
4	Screen inclination adjustment	(a) Adjustment diagram  1 Adjust the screen inclination by turning the DY, based on the straight line of the front panel. (measure both E and F.) 2 Tighten DY and lock it with paint.	DY	Less than 1.3mm (Difference between E and F) DY shall be in fully contact with the CRT so that there is no space between them.	Scale Paint lock

No.	Item	Procedure (Condition)	Wiring diagram symbol	Standard	Tool and measuring instrument
5	Picture position adjustment	1 Set the picture almost at the center of the CRT screen with the centering magnet. (Measure a pair of A and B and that of C and D.) 2 Lock the position with paint.	Centering magnet	Less than 3mm (Difference between A and B, C and D.)	Scale Paint lock
6	Sub.BRIGHT	1 Maximize BRIGHT and CONTRAST. 2 Turn SUB.BRIGHT and set the raster at the point where it is slightly visible near the cut-off point. 3 Turn CONTRAST counterclockwise about 30 to 45 from the maximum point. 4 Set BRIGHT at the point where the raster disappears.	R326 R106 R325	The raster shall be slightly visible.	
7	Screen size adjustment	1 Adjust H shown in the adjustment diagram with WIDTH COIL. 2 Adjust V shown in the adjustment diagram with V.HEIGHT.	L302 R210	H=210mm ±3mm V=140mm ±3mm	Scale

No.	Item	Procedure (Condition)	Wiring diagram symbol	Standard	Tool and measuring instrument
8	Screen distortion adjustment	 1 Adjust the screen distortion with correction magnets. (Measure G, H, I, and J.) 2 After screen distortion adjustment, check the screen size and tilt.	Correction magnet	Less than 1.8mm (Each of G,H,I, and J indicates the distance from the center line.)	Scale
9	V.LIN	(Character H)  (K and M indicate the distance between two lines.)	R209	Less then 0.5mm (Differences K and M)	Scale
10	FOCUS	Adjust the focus of each character with the FOCUS Knob so that the focus becomes even on the entire screen.			
11	V.HOLD	Turn ON after OFF the POWER switch.		It shall not be asynchronous.	

No.	Item	Procedure (Condition)	Wiring diagram symbol	Standard	Tool and measuring instrument
12	H.HOLD	Turn ON after OFF the POWER switch.		It shall not be asynchro-nous.	

8. REPAIR

8.1 Self-diagnostic Function

VG-920 is provided with the self-diagnostic function to check the equipment status. This function has two kinds; AUTO DIAG to be executed automatically at power ON and the self-diagnostic function to be executed by inputting commands from the keyboard unit or the host computer.

When the self-diagnosis starts, the data which has been displayed on the CRT is cleared. During execution of the self-diagnosis other than AUTO DIAG, "Testing" is displayed on the lowermost screen line blinking.

When an error is detected, the test is terminated, the error message is displayed, and "END" is displayed on the lowermost screen line.

At normal end of the self-diagnosis, VG-920 OK is displayed on the screen center.

After completion of the self-diagnosis, VG-920 starts operating according to the Set Up parameters set in NVR.

The message displayed at completion of the self-diagnosis is cleared when data is inputted from the keyboard or received from the host computer, and data starts being displayed with the first column on the first line.

(At completion of the self-diagnosis other than AUTO DIAG,

the error message displayed on the screen is not cleared by the data received from the host computer. It can be cleared only when data is inputted from the keyboard.)

8.2 Kinds of self-diagnostic Function

1) AUTO DIAG

At power ON, VG-920 automatically executes the self-diagnosis shown in Table 8-2-1 in sequence. At normal end of the self-diagnosis, VG-920 OK is displayed; at detection of an error, the error message is displayed on the screen.

Table 8-2-1 Kinds of AUTO DIAG

No.	Name	Operation Outline
1	RAMTST (RAM Test)	Writes/reads data to/from the RAM (6264: 7D) to perform comparison check.
2	RFMTST (Refresh Memory Test)	Writes/reads data to/from the refresh memory (6264: 1E), attribute memory (6264: 1C), and character generator RAM (6116: 2F) to perform comparison check.
3	ROMTST (ROM Test)	Compares the registered SUM check values for EPROM (27256: 7H.2764: 7F) with the calculated values for checking.
4	KBDTST (Keyboard Test)	Outputs both the LED and BELL control commands to the keyboard unit. Then, receives the status data from the keyboard unit to perform the validity check. Also, checks the timer (8253C-5: 5D).

2) Self-diagnosis performed by commands

The commands inputted from the keyboard unit or the host computer cause the self-diagnosis shown in Table 8-2-2 to be executed individually or in combination.

During the self-diagnosis, "Testing" is displayed on the lowermost screen line blinking.

At normal end of the self-diagnosis, VG-920 OK is displayed on the screen center.

At detection of an error, the test is terminated, the error message is displayed on the screen, and "END" is displayed on the lowermost screen line.

Table 8-2-2 Kinds of self-diagnosis Performed Commands

No.	Name	Operation Outline
1	RAMTST (RAM Test)	Writes/reads data to/from the RAM (6264: 7D) to perform comparison check.
2	RFMTST (Refresh Memory Test)	Writes/reads data to/from the refresh memory (6264: 1E), attribute memory (6264: 1C), and character generator RAM (6116: 2F) to perform comparison check.
3	ROMTST (ROM Test)	Compares the registered SUM check values for EPROM (27256: 7H, 2764: 7F) with the calculated values for checking.
4	KBDTST (Keyboard Test)	Outputs the LED and BELL control commands to the keyboard unit. Then, receives the status data from the keyboard to perform validity check. Also, checks for the timer (8253C-5: 5D) and CRTC (SCN2674BC4N40: 1A) interruptions.
5	EIATST (EIA Test)	Performs the data loop-back test for the COMM port by using the signal loop-back connector.
6	SPRTST (Serial Printer Test)	Performs the data loop-back test for the S.PRT port by using the signal loop-back connector.
7	PPRTST (Parallel Printer Test)	Outputs the fixed message to the printer when the parallel-interface printer (conforming to CENTRONIX) is connected with this equipment. Monitors the time out for the response with the acknowledge signal.
8	CLPTST (Current Loop Test)	Performs the data loop-back test for the 20mA port by using the signal loop-back connector.
9	SIGTST (EIA Port Signal Test)	Checks for the MODEM control signal for the EIA port by using the signal loop-back connector

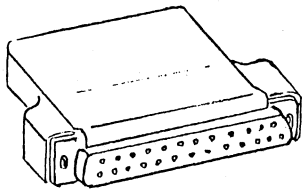
No.	Name	Operation Outline
10	NVRTST (NVR Test)	Writes/reads data to/from NVR (X2212: 7C) to perform comparison check.
11	DSPTST (Display Test)	On the screen, the character fonts (character generator 2764: 1F) for the hard character set, the display character attributes, and the line attributes (magnified display) are displayed.

8.3 Tools

The following tools are required for executing self-diagnoses EIATST, SPRTST, PPRTST, CLPTST, and SIGTST:

1) Signal loop-back connector for EIATST/SIGTST(JT8005)

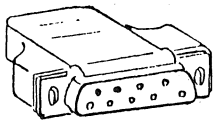
25P D-Sub connector



Pin connections	
From	To
2(SD)	3(RD)
4(RTS)	5(CTS), 8(RLSD)
20(DTR)	6(DSR)
23(SPDS)	12(SPDI)

2) Signal loop-back connector for SPRTST(JT8007)

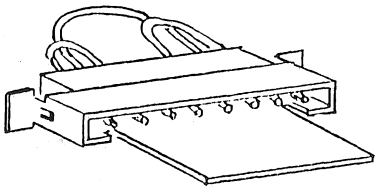
9P D-Sub connector



Pin connections	
From	To
2(SD)	3(RD)
5(DTR)	6(DSR)

3) Signal loop-back connector for CLPTST(JT8006)

Mate-N-Loc connector
(8P, Manufactured by AMP)



Pin connections	
From	To
1(-12v)	3(Receive -)
2(Transmit -)	7(Receive +)
5(Transmit +)	8(SG)

4) Parallel interface printer for PPRTST

Conforming to CENTRONIX, TTL-level 8-bit parallel interface printer and connection cable (36-pin connector)

P.PRT port connector pin list					
Pin NO.	Mnemonic	Signal name	Pin NO.	Mnemonic	Signal name
1	$\overline{\text{PRSTB}}$	Printer storobe	19	SGND	Signal ground
2	PD0	Data bit 0	20	SGND	Signal ground
3	PD1	Data bit 1	21	SGND	Signal ground
4	PD2	Data bit 2	22	SGND	Signal ground
5	PD3	Data bit 3	23	SGND	Signal ground
6	PD4	Data bit 4	24	SGND	Signal ground
7	PD5	Data bit 5	25	SGND	Signal ground
8	PD6	Data bit 6	26	SGND	Signal ground
9	PD7	Data bit 7	27	SGND	Signal ground
10	$\overline{\text{ACK}}$	Acknowledge	28	SGND	Signal ground
11	BUSY	Printer busy	29	SGND	Signal ground
12			30	SGND	Signal ground
13			31		
14			32		
15			33		
16			34		
17	PGND	Protective ground	35		
18			36		

8.4 Execution of Self-diagnostic Function

1) AUTO DIAG

VG-920 automatically executes AUTO DIAG when powered ON.

2) Self-diagnosis performed by commands

The self-diagnosis shown in Table 8-2-2 can be executed by receiving the following ESC sequence commands from the keyboard unit or the host computer:

1/11	5/11	3/4	3/11		3/11		7/9
ESC	[	4	;	Ps	;	Pn	y

Ps: Indicates the kind of the test to be executed. (See Table 8-4-1.)

Pn: Indicates the number of times for executing the test.

When Pn=0 or Pn is none, the test is excuted permanently.

The specified value greater than 256 is regarded as 255.

Table 8-4-1 Ps Values For Tests to be Executed

Ps value	Test to be executed	Ps value	Test to be executed	Ps value	Test to be executed
0	ROMTST	1	RFMTST	20	PPRTST
	KBDTST		ROMTST	21	KBDTST
	EIATST		KBDTST	22	ROMTST
	SPRTST	2	EIATST	23	RAMTST
	SIGTST	3	SPRTST	24	RFMTST
	PPRTST	6	SIGTST	25	NVRTST
	CLPTST	7	CLPTST	26	DSPTST

8.5 Error Messages

When an error is detected during execution of AUTO DIAG or a self-diagnosis by inputting a command, any of the error messages shown in Table 8-5-1 is displayed on the screen.

Table 8-5-1 Self-Diagnosis Error Message List

No.	NAME	DISPLAY LINE	ERROR MESSAGE	ERROR CONTENTS
1	RAMTST		None. (The bell rings at occurrence of an error.)	An error is detected during the comparison check for RAM (6264: 7D).
2	RFMTST	2	Refresh Memory Error 0	An error is detected during the comparison check for refresh memory (6264: 1E)
			Refresh Memory Error 1	An error is detected during the comparison check for attribute memory (6264: 1C)
			Refresh Memory Error 2	An error is detected during the comparison check for the character generator RAM (6116: 2F).
3	ROMTST	4	PROM Error	The registered SUM check values for EPROM (27256: 7H, 2764: 7F) do not match the calculated values. lated values.
4	KBDTST	6	KBD Error 0	An error is detected during the munication with the keyboard.
			KBD Error 1	An error is detected during the timer (8253C-5: 5D) or CRTC (SCN2674BC4N40: 1A).

No.	NAME	DISPLAY LINE	ERROR MESSAGE	ERROR CONTENTS
5	EIATST	8	EIA Port Error 0	Data cannot be sent to the Comm port.
			EIA Port Error 1	Data cannot be received from the Comm port.
			EIA Port Error 2	The data sent to the Comm port does not match the data received from the Comm port.
6	SPRTST	10	Serial Printer Port Error 0	Data cannot be sent to the S.PRT port.
			Serial Printer Port Error 1	Data cannot be received from the S.PRT port.
			Serial Printer Port Error 2	The data sent to the S.PRT port does not match the data receiv-ed from the S.PRT port.
			Serial Printer Port Error 3	The DSR input signal of S.PRT Port is turned OFF.
7	PPRTST	14	Parallel Printer Port Error	The ACK (Acknow-ledge) signal does not return from the parallel printer within the specified period of time (10 seconds) or the BUSY signal is not cancelled within the spe-cified period of time (60 seconds)
8	CLPTST	16	20mA Port Error 0	Data cannot be sent to the 20mA port.

No.	NAME	DISPLAY LINE	ERROR MESSAGE	ERROR CONTENTS
8	CLPTST	16	20mA Port Error 1	Data cannot be received from the 20mA ,port
			20mA Port Error 2	The data sent to the 20mA port does not match the data received from the 20mA port.
9	SIGTST	12	EIA Port Controls Error 0	The SPDI signal is turned OFF when the SPDS signal is turned ON.
			EIA Port Controls Error 1	The SPDI signal is turned ON when the SPDS signal is turned OFF.
			EIA Port Controls Error 2	The DSR signal is turned OFF when the DTR signal is turned ON.
			EIA Port Controls Error 3	The DSR signal is turned ON when the DTR signal is turned OFF.
			EIA Port Controls Error 4	The CTS signal is turned ON when the RTS signal is turned OFF.
			EIA Port Controls Error 5	The PLSD signal is turned ON when the RTS signal is turned OFF.
			EIA Port Controls Error 6	The CTS signal is turned OFF when the RTS signal is turned ON.
			EIA Port Controls Error 7	The RLSD Signal is turned OFF when the RTS signal is turned ON.

No.	NAME	DISPLAY LINE	ERROR MESSAGE	ERROR CONTENTS
10	NVRTST	2	NVR Error	An error is detected during the comparison check for NVR (X2212: 7C).
11	DSPTST		None. On the screen, the character fonts (2764: 1F) for the hard character set, the display character attributes, and the line attributes (magnified display) are displayed. However, neither the error message nor VG-920 OK at normal end is displayed.	

8.6 Troubleshooting

The cautions and the typical trouble and troubleshooting examples are described as follows:

1) Cautions

(1) Be sure to pull out the power cord before disassembling or replacing the part such as the connector, cabinet.

There are some high-voltage parts in the equipment so that it is dangerous to touch them.

(2) Be sure to visually check that there is no abnormal condition on the appearance and the internal parts.

2) Typical trouble and troubleshooting examples

(1) Troubles generated at power ON

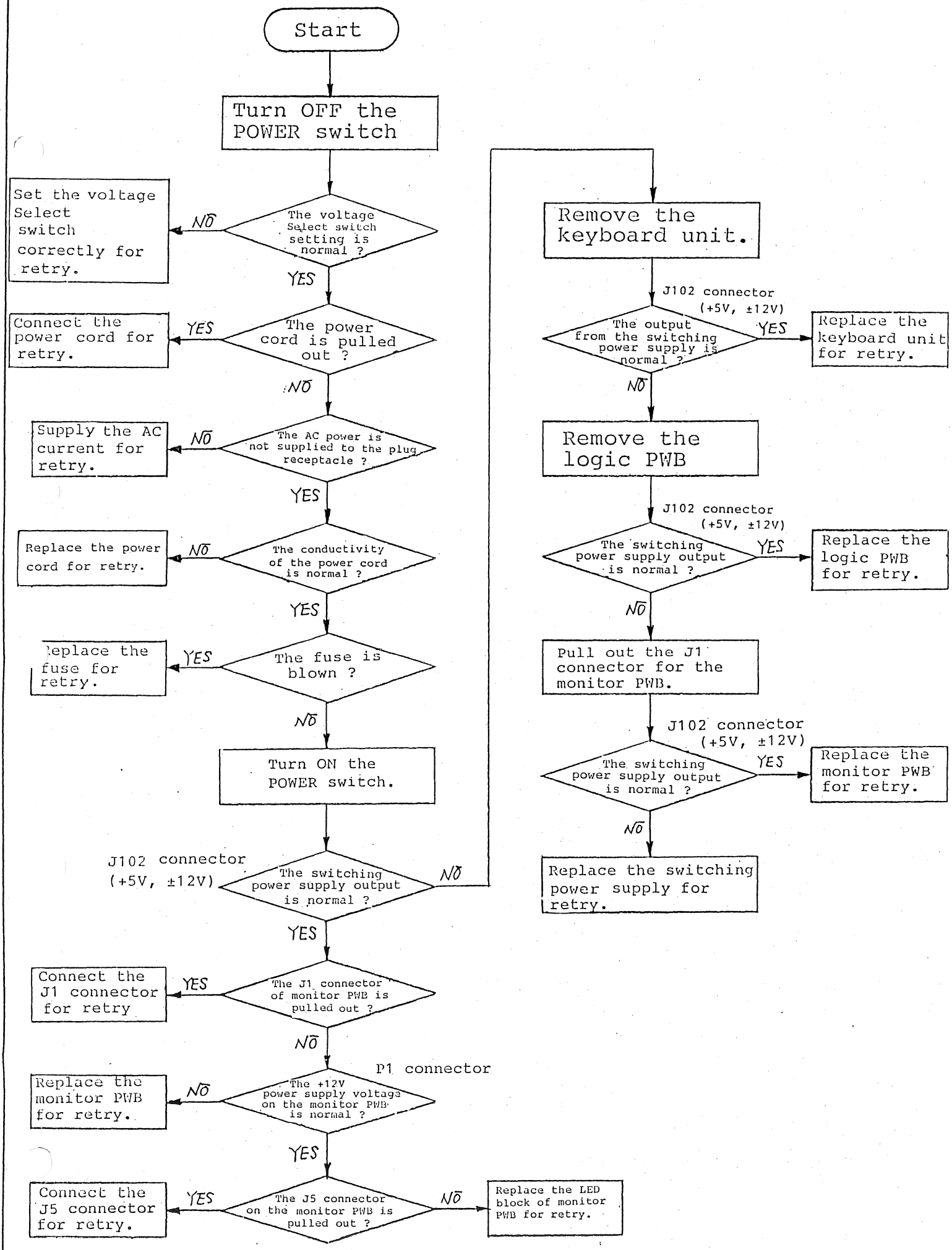
No.	Phenomenon	Troubleshooting example
1	The power LED does not light up when the POWER switch is turned ON.	See Fig. 8-6-1.
2	The power LED lights up but no data is displayed on the screen.	See Fig. 8-6-2
3	The screen display is abnormal.	See Fig. 8-6-3
4	An error is displayed during AUTO DIAG.	See Fig. 8-6-4
5	The Keyboard operates abnormally	See Fig. 8-6-5

(2) Troubles generated during operation

No.	Phenomenon	Troubleshooting example
1	The screen display is abnormal.	See Fig. 8-6-6
2	Data transfer with the external device is abnormal.	See Fig. 8-6-7
3	The keyboard operates abnormally.	See Fig. 8-6-5

(3) Others

No.	Phenomenon	Troubleshooting example
1	The abnormal noise is generated.	See Fig. 8-6-8


Start
Turn OFF the POWER switch
The voltage Select switch setting is normal ?
NO
Set the voltage Select switch correctly for retry.
YES
The power cord is pulled out ?
YES
Connect the power cord for retry.
NO
The AC power is not supplied to the plug receptacle ?
NO
Supply the AC current for retry.
YES
The conductivity of the power cord is normal ?
NO
Replace the power cord for retry.
YES
The fuse is blown ?
YES
Replace the fuse for retry.
NO
Turn ON the POWER switch.
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
NO
YES
The J1 connector of monitor PWB is pulled out ?
YES
Connect the J1 connector for retry
NO
P1 connector
The +12V power supply voltage on the monitor PWB is normal ?
NO
Replace the monitor PWB for retry.
YES
The J5 connector on the monitor PWB is pulled out ?
YES
Connect the J5 connector for retry.
NO
Replace the LED block of monitor PWB for retry.
Remove the keyboard unit.
J102 connector (+5V, ±12V)
The output from the switching power supply is normal ?
YES
Replace the keyboard unit for retry.
NO
Remove the logic PWB
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the logic PWB for retry.
NO
Pull out the J1 connector for the monitor PWB.
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the monitor PWB for retry.
NO
Replace the switching power supply for retry.

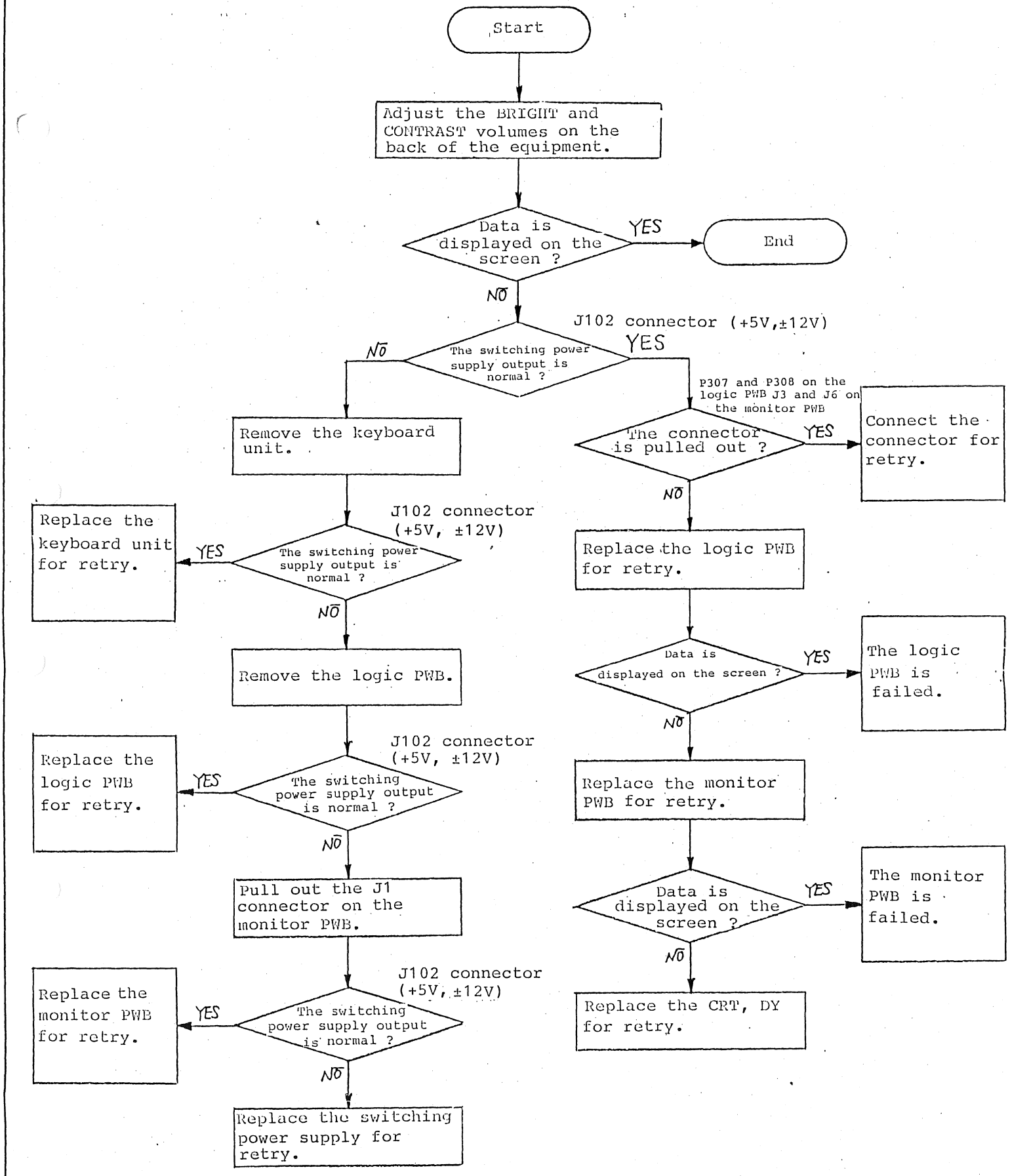

Start
Adjust the BRIGHT and CONTRAST volumes on the back of the equipment.
Data is displayed on the screen ?
YES
End
NO
J102 connector (+5V,±12V)
The switching power supply output is normal ?
NO
YES
P307 and P308 on the logic PWB J3 and J6 on the monitor PWB
The connector is pulled out ?
YES
Connect the connector for retry.
NO
Remove the keyboard unit.
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the keyboard unit for retry.
NO
Replace the logic PWB for retry.
Remove the logic PWB.
Data is displayed on the screen ?
YES
The logic PWB is failed.
NO
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the logic PWB for retry.
NO
Replace the monitor PWB for retry.
Pull out the J1 connector on the monitor PWB.
Data is displayed on the screen ?
YES
The monitor PWB is failed.
NO
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the monitor PWB for retry.
NO
Replace the CRT, DY for retry.
Replace the switching power supply for retry.

Fig. 8-6-2.

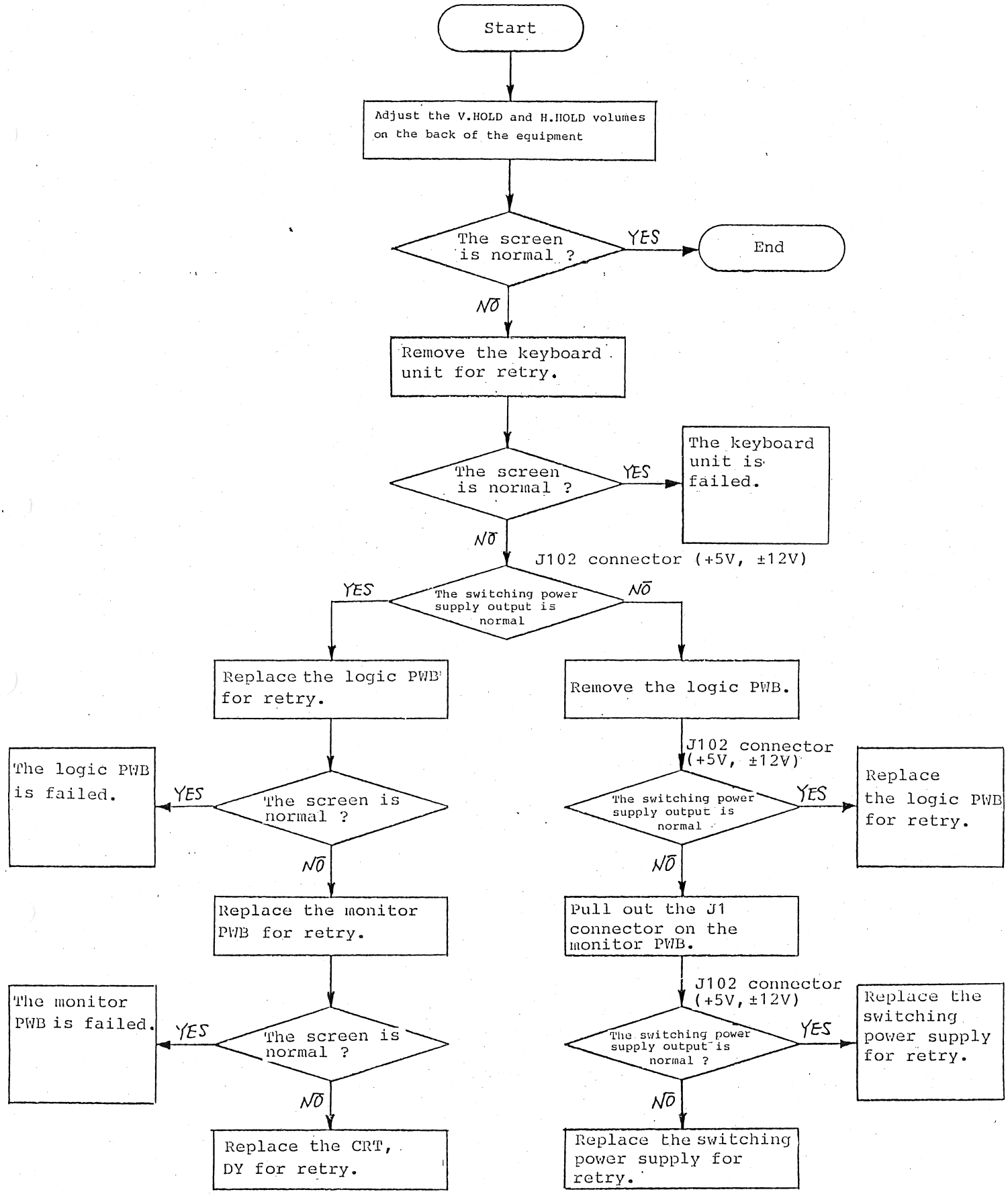

Start
Adjust the V.HOLD and H.HOLD volumes on the back of the equipment
The screen is normal ?
YES
End
NO
Remove the keyboard unit for retry.
The screen is normal ?
YES
The keyboard unit is failed.
NO
J102 connector (+5V, ±12V)
The switching power supply output is normal
YES
NO
Replace the logic PWB for retry.
Remove the logic PWB.
The logic PWB is failed.
YES
The screen is normal ?
NO
J102 connector (+5V, ±12V)
The switching power supply output is normal
YES
Replace the logic PWB for retry.
NO
Replace the monitor PWB for retry.
Pull out the J1 connector on the monitor PWB.
The monitor PWB is failed.
YES
The screen is normal ?
NO
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the switching power supply for retry.
NO
Replace the CRT, DY for retry.
Replace the switching power supply for retry.

Fig. 8-6-3

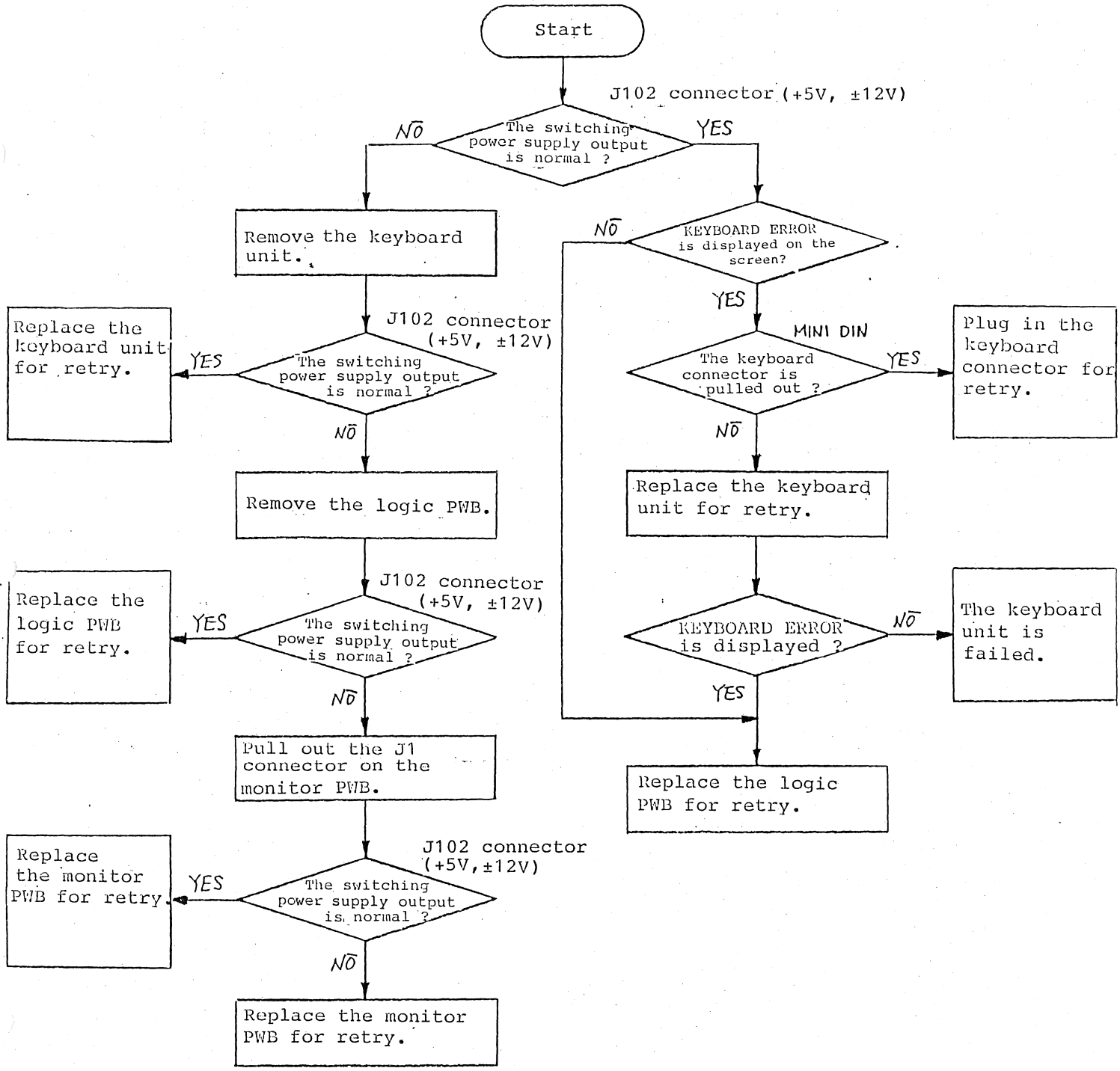

Start
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
NO
YES
Remove the keyboard unit.
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the keyboard unit for retry.
NO
Remove the logic PWB.
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the logic PWB for retry.
NO
Pull out the J1 connector on the monitor PWB.
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the monitor PWB for retry.
NO
Replace the monitor PWB for retry.
KEYBOARD ERROR is displayed on the screen?
NO
YES
MINI DIN
The keyboard connector is pulled out ?
YES
Plug in the keyboard connector for retry.
NO
Replace the keyboard unit for retry.
KEYBOARD ERROR is displayed ?
NO
The keyboard unit is failed.
YES
Replace the logic PWB for retry.

Fig. 8-6-4

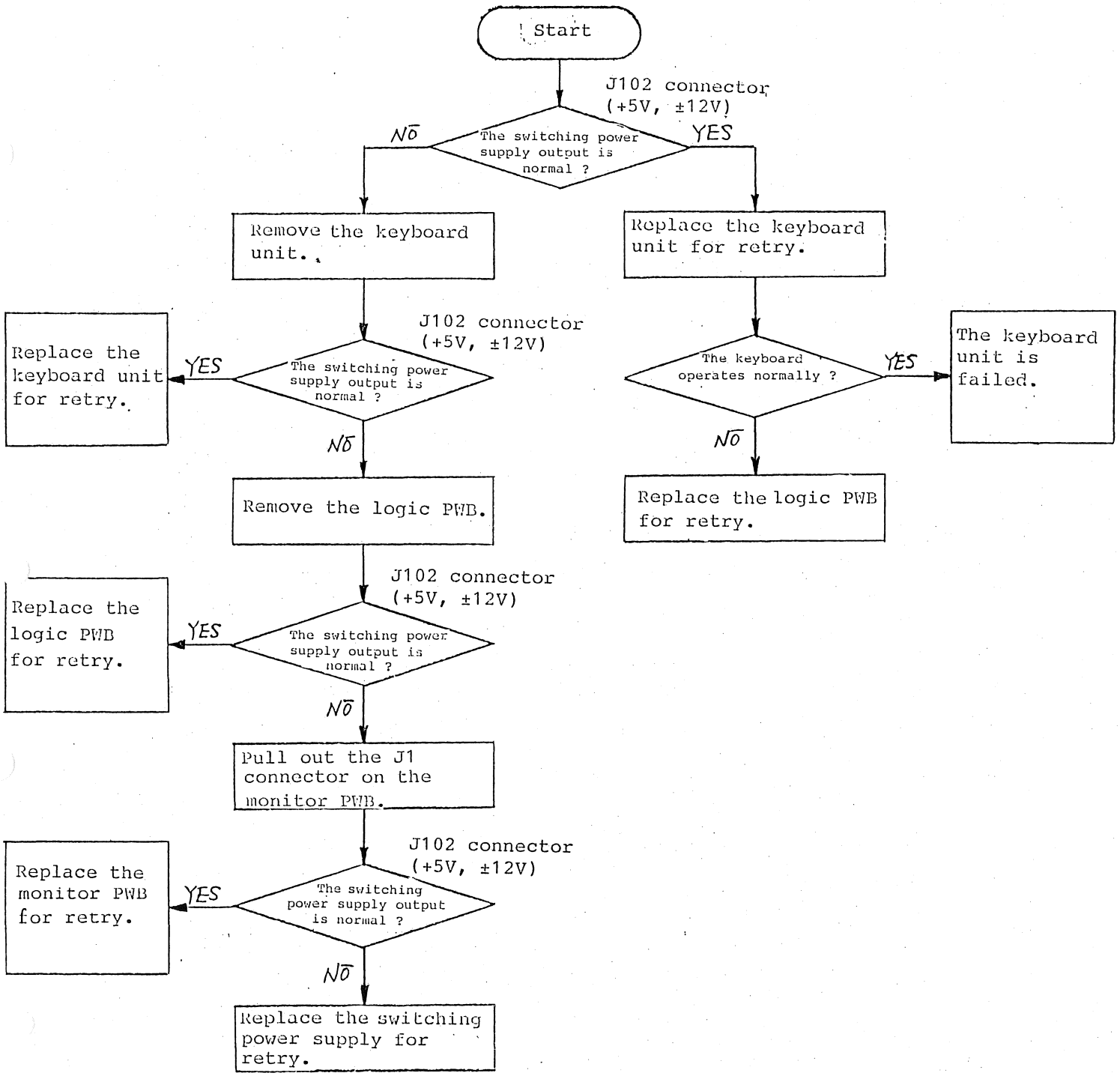

Start
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
NO
YES
Remove the keyboard unit.
Replace the keyboard unit for retry.
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the keyboard unit for retry.
NO
Remove the logic PWB.
The keyboard operates normally ?
YES
The keyboard unit is failed.
NO
Replace the logic PWB for retry.
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the logic PWB for retry.
NO
Pull out the J1 connector on the monitor PWB.
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
YES
Replace the monitor PWB for retry.
NO
Replace the switching power supply for retry.

Fig. 8-6-5

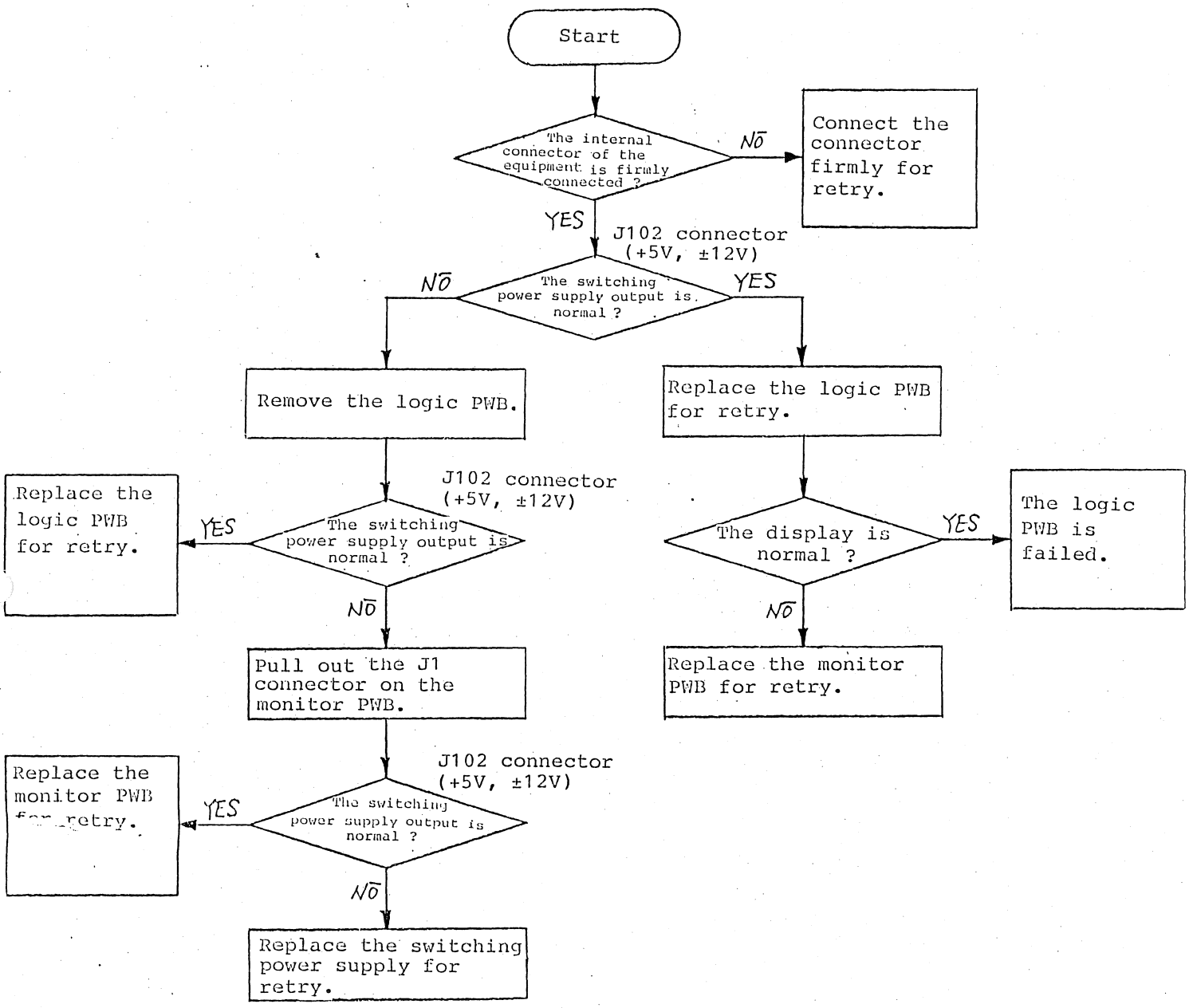

Start
The internal connector of the equipment is firmly connected ?
NO
Connect the connector firmly for retry.
YES
J102 connector (+5V, ±12V)
The switching power supply output is normal ?
NO
YES
Remove the logic PWB.
Replace the logic PWB for retry.
J102 connector (+5V, ±12V)
Replace the logic PWB for retry.
YES
The switching power supply output is normal ?
The display is normal ?
YES
The logic PWB is failed.
NO
NO
Pull out the J1 connector on the monitor PWB.
Replace the monitor PWB for retry.
J102 connector (+5V, ±12V)
Replace the monitor PWB for retry.
YES
The switching power supply output is normal ?
NO
Replace the switching power supply for retry.

Fig. 8-6-6

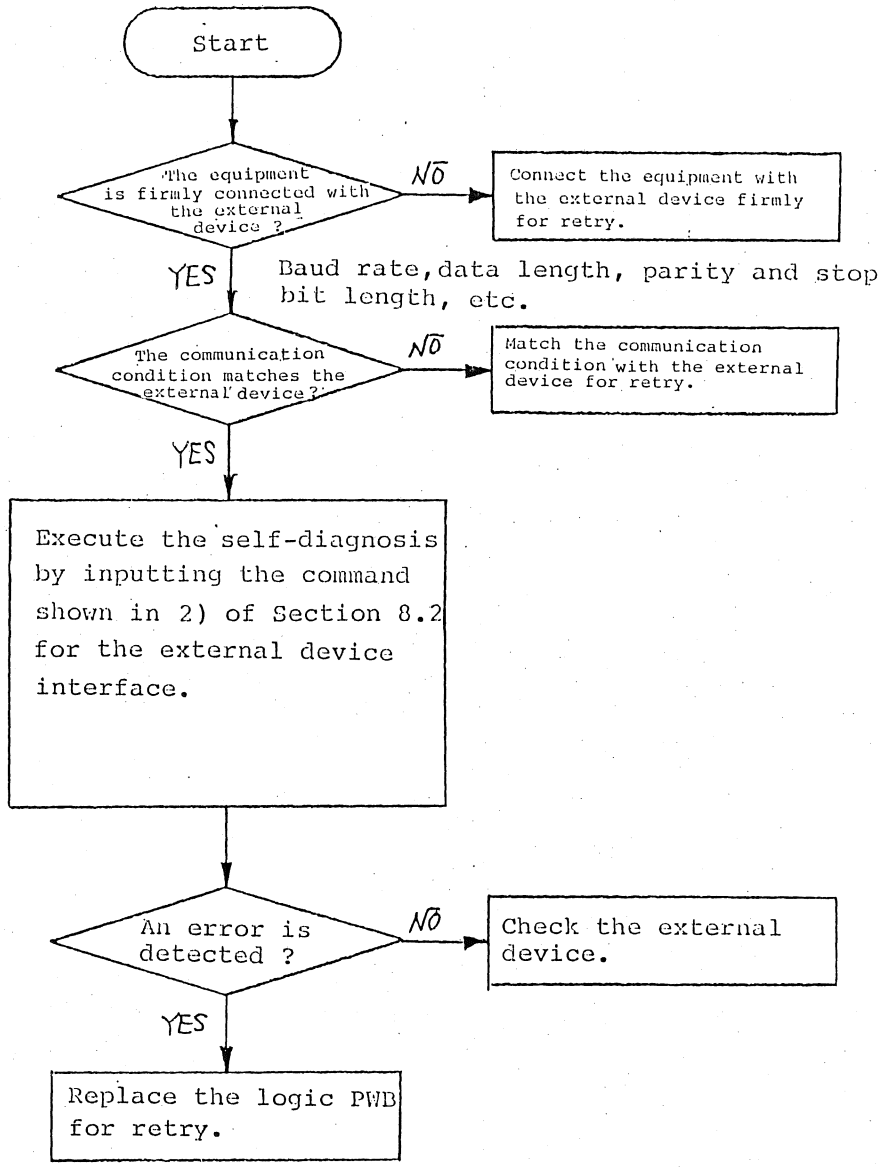
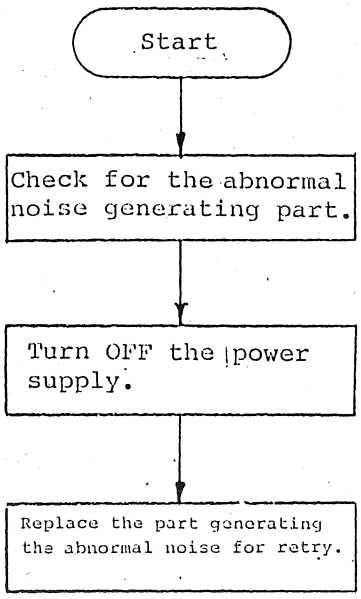

Start
The equipment is firmly connected with the external device ?
NO
Connect the equipment with the external device firmly for retry.
YES
Baud rate, data length, parity and stop bit length, etc.
The communication condition matches the external device ?
NO
Match the communication condition with the external device for retry.
YES
Execute the self-diagnosis by inputting the command shown in 2) of Section 8.2 for the external device interface.
An error is detected ?
NO
Check the external device.
YES
Replace the logic PWB for retry.

Fig. 8-6-7


Start
Check for the abnormal noise generating part.
Turn OFF the power supply.
Replace the part generating the abnormal noise for retry.

9. HOW TO REFERENCE CIRCUIT DIAGRAMS

* The circuit diagrams are the standard circuit diagrams so that they may be changed without any prior notice to improve the product such as the circuit and constant.

9.1 Safety

Be sure to use the specified part to secure safety when replacing the part marked with ⚠ on the circuit diagram. For other parts, be sure to use the specified ones for securing the safety and maintaining the performance.

9.2 Indications on Circuit Diagrams

1) Resistance

(1) Resistance value

No unit indication: [Ω]

K: [KΩ]

M: [MΩ]

(2) Rated allowable power

No unit indication: 1/4 W

Others: Indicated

2) Capacitor

(1) Capacity

P: pF μ: [μF] No indication: [μF]

(2) Dielectric voltage

No indication: 50V

Others: Indicated

3) Ground indications

⏚ : GROUND (SIGNAL) (GND)

⏚ : EARTH (FRAME) (FG)

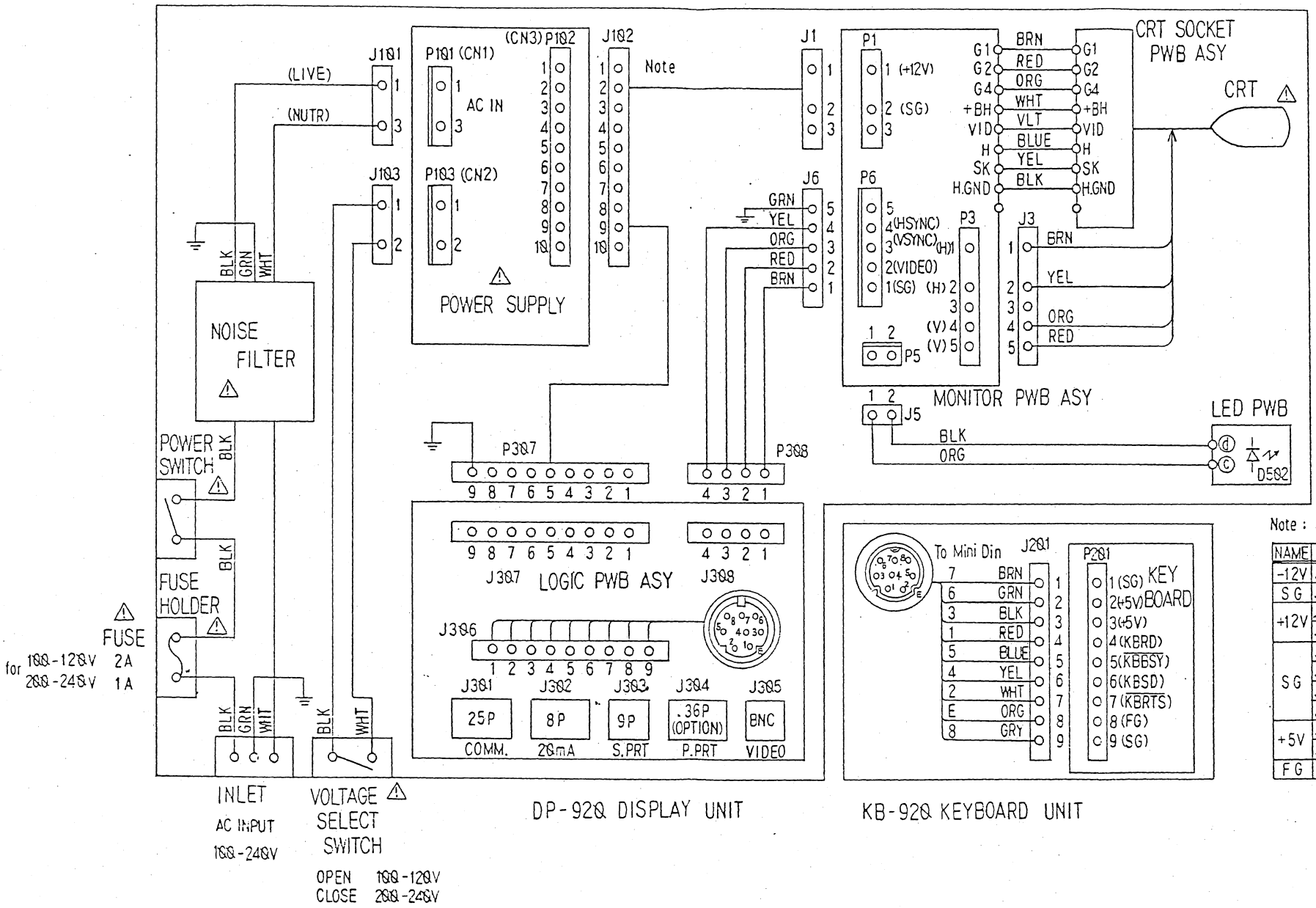
10. CIRCUIT DIAGRAMS

(1) VG-920 WIRING Fig. 10-1

(2) VG-920 LOGIC PWB Fig. 10-2 1/6 to 6/6

(3) VG-920 MONITOR PWB Fig. 10-3

(4) VG-920 LOGIC PWB CONNECTOR LIST Fig. 10-4



Note : J102 WIRING

NAME	From	Wire	To
-12V	J102- 1	BRN	P307
S G	J102- 2	RED	P307
+12V	J102- 3	ORG	P307
	J102- 4	YEL	J1-1
S G	J102- 5	GRN	J1-2
	J102- 6	BLUE	P307
	J102- 7	VLT	P307
	J102- 8	GRY	P307
+5V	J102- 9	WHT	P307
	J102-10	BLK	P307
F G	FG	GRN	P307

FIG. 10-1 VG-920 WIRING

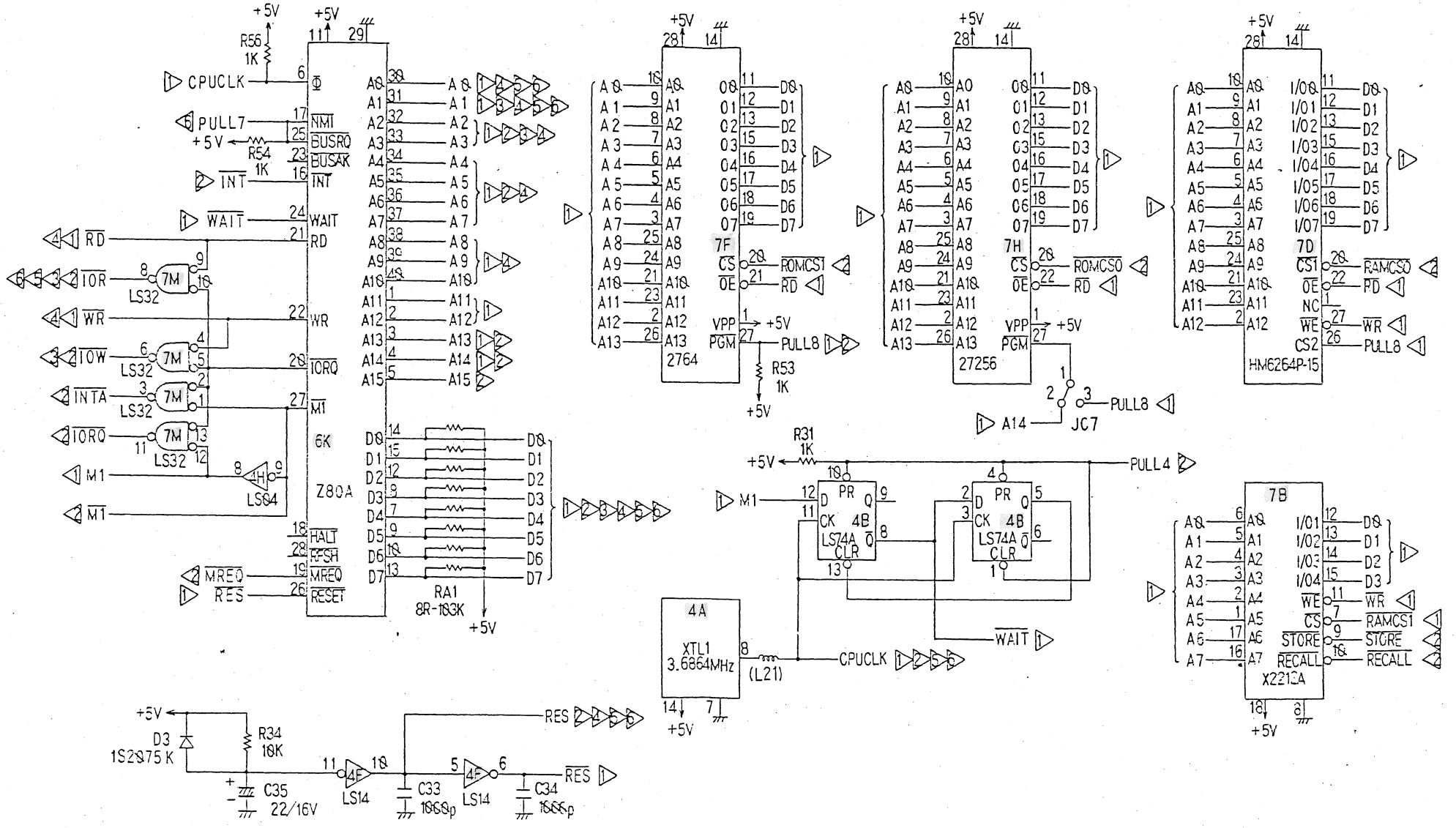


FIG. 10-2 VG-920 LOGIC PWB 1/6

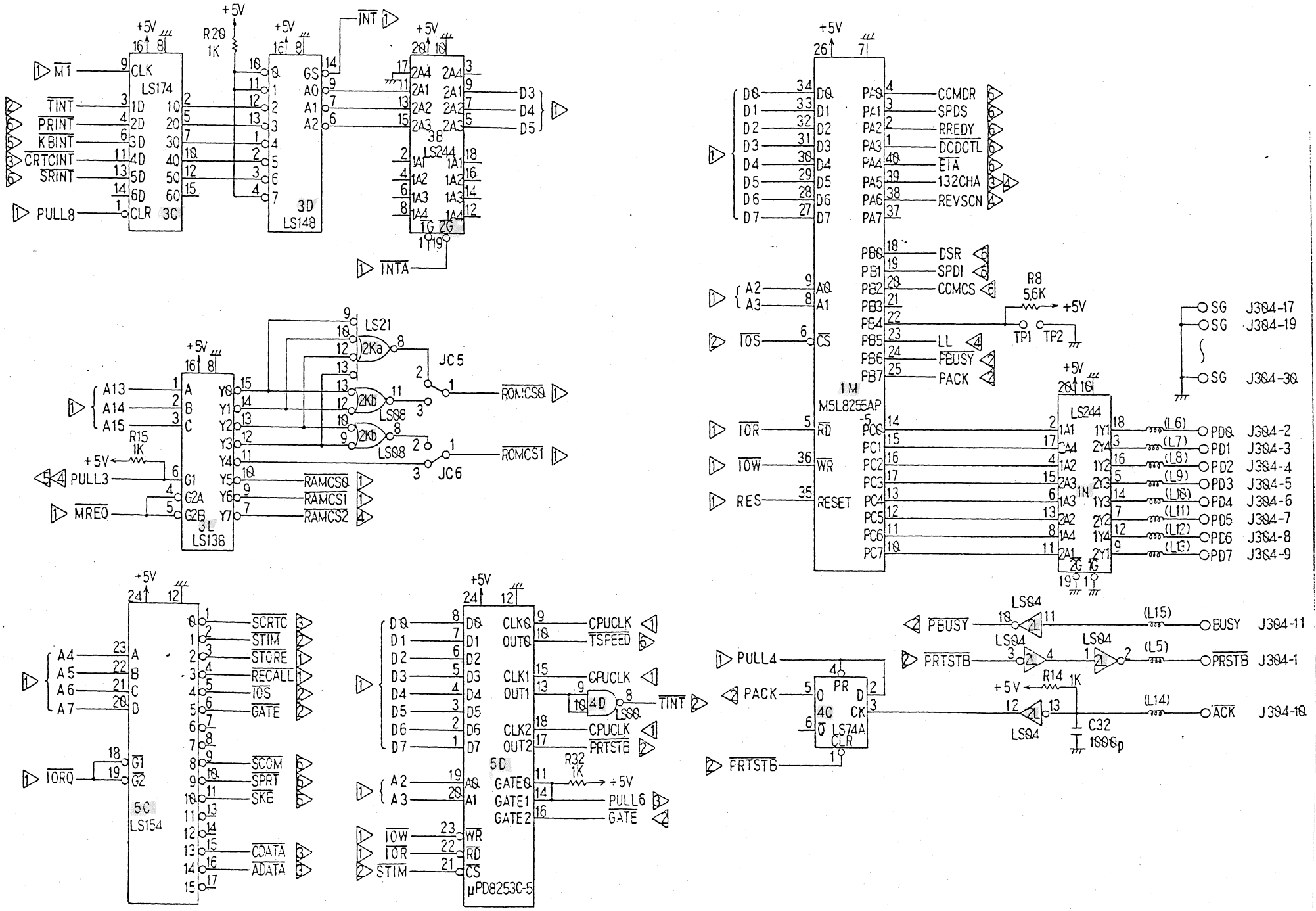


FIG. 10-2 VG-920 LOGIC PWB 2/6

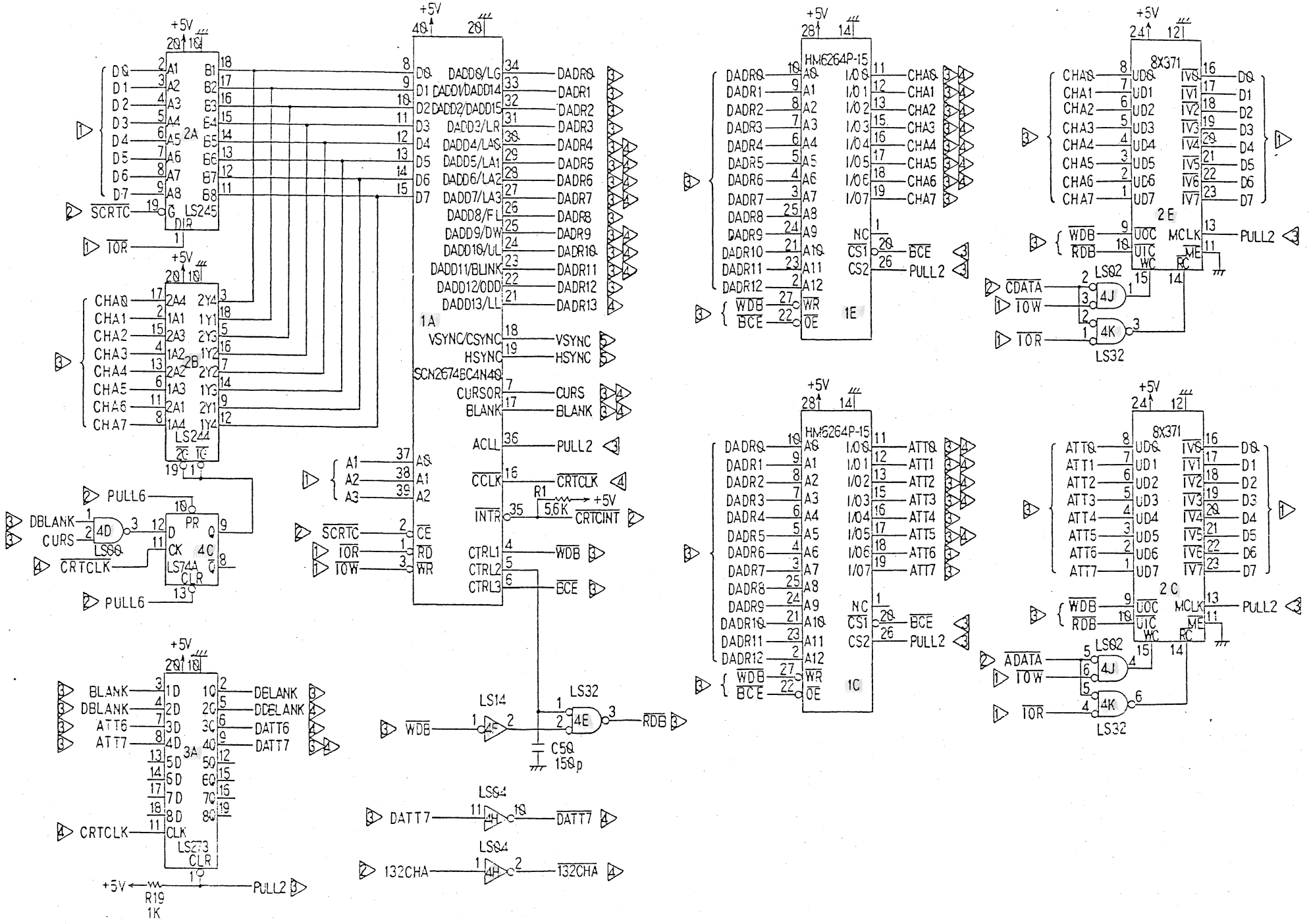


FIG. 10-2 VG-920 LOGIC PWB 3/6

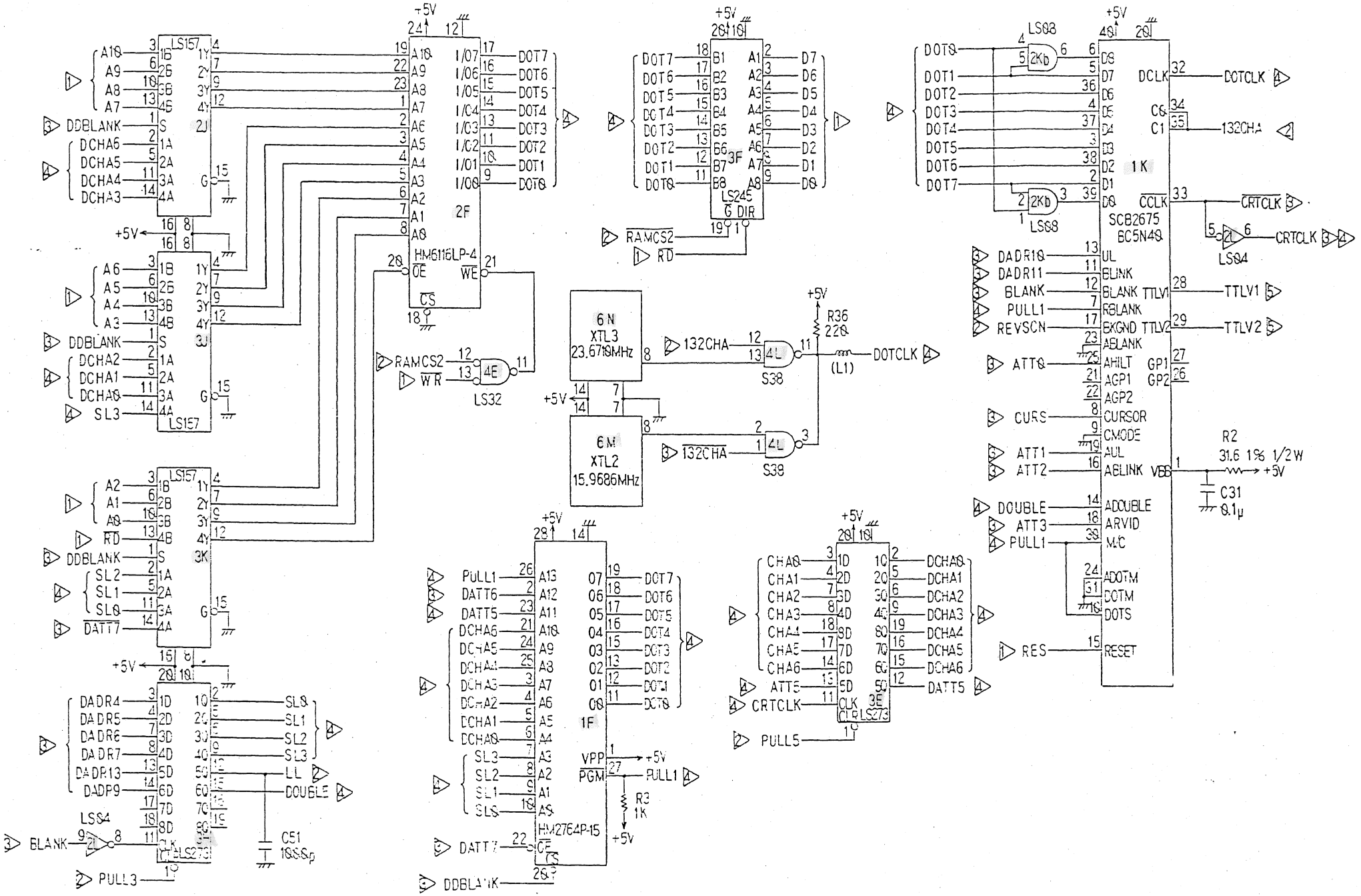


FIG. 10-2 VG-920 LOGIC PWB 4/6

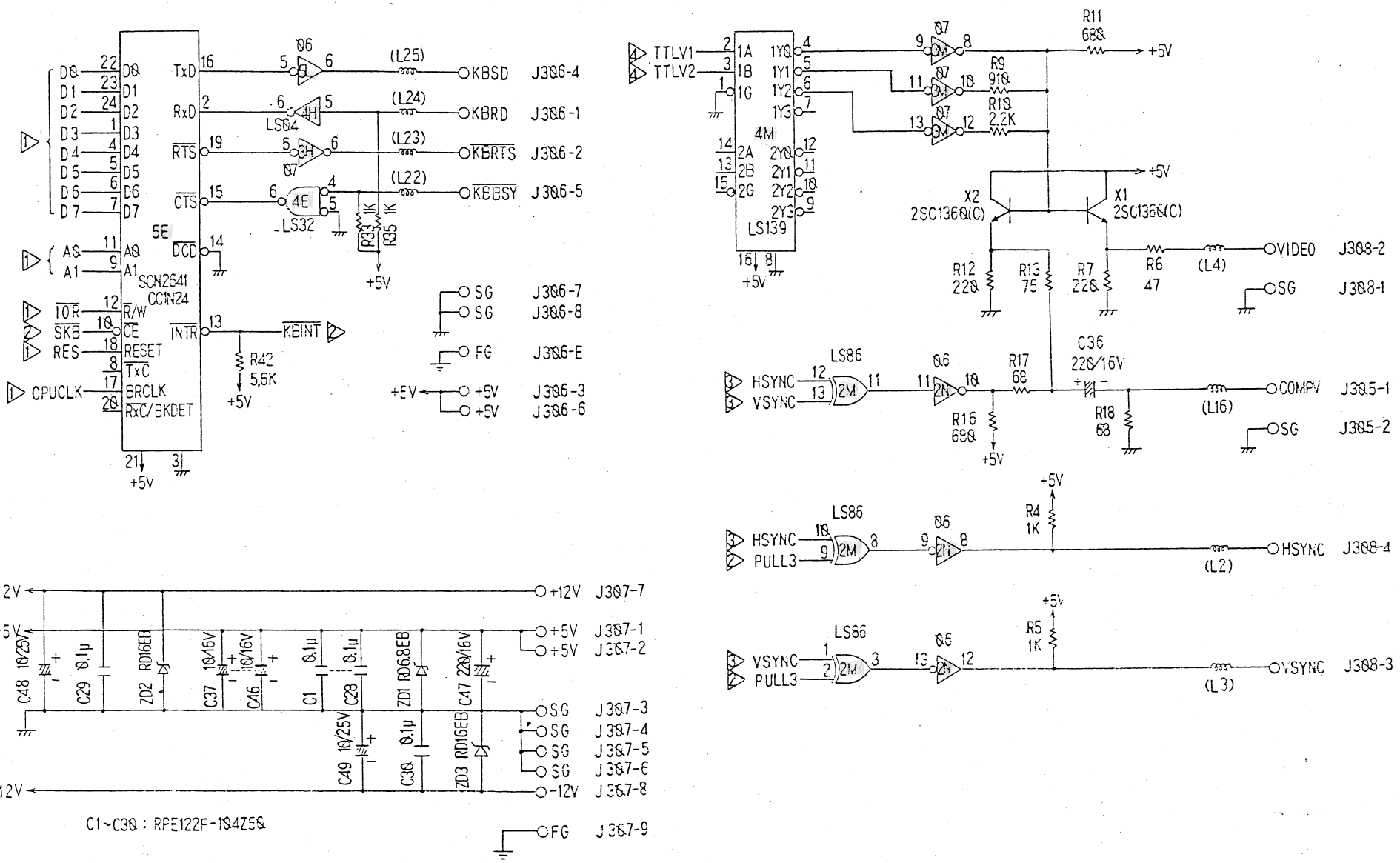


FIG. 10-2 VG-920 LOGIC PWB 5/6

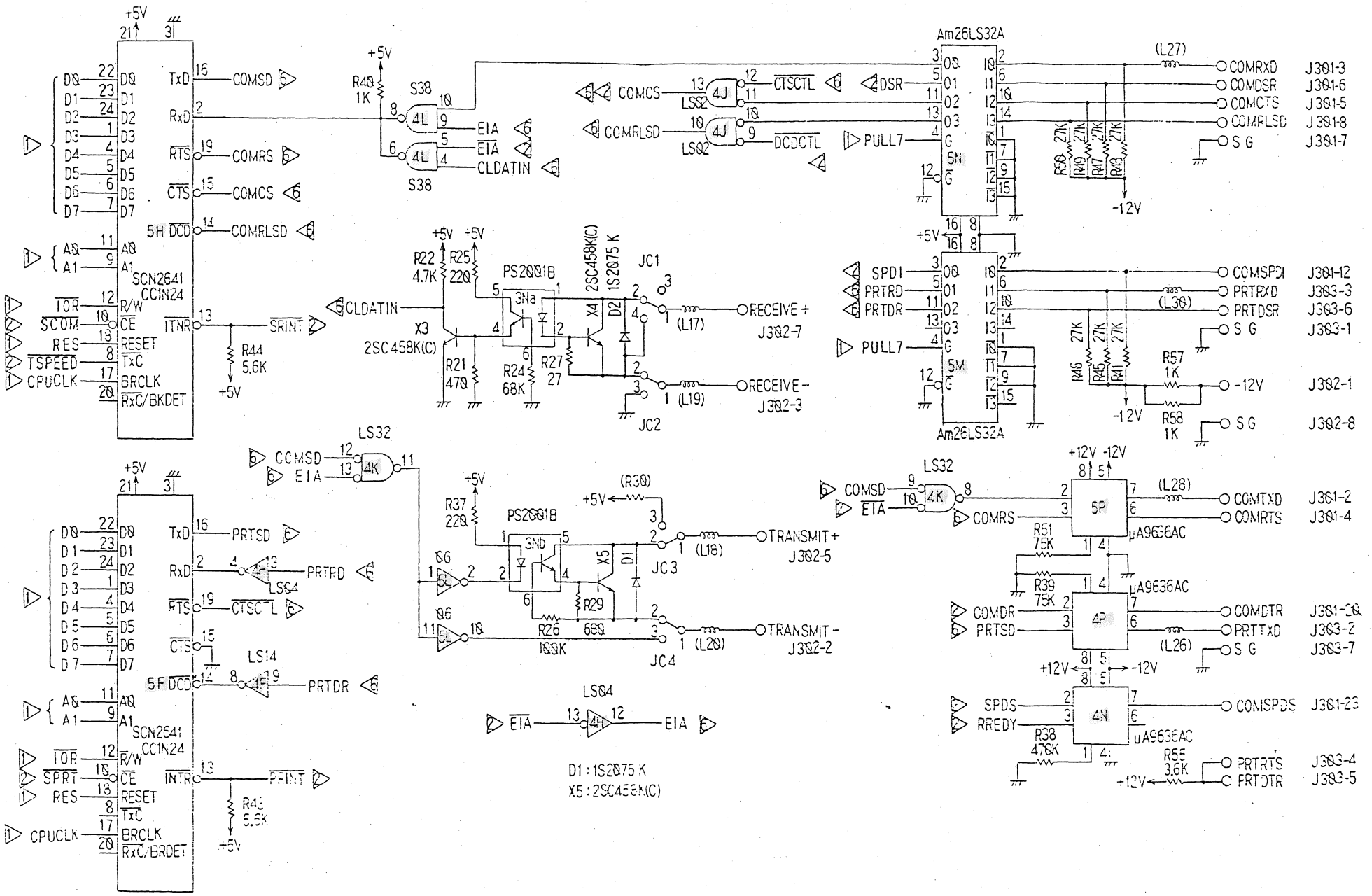


FIG. 10-2 VG-920 LOGIC PWB 6/6

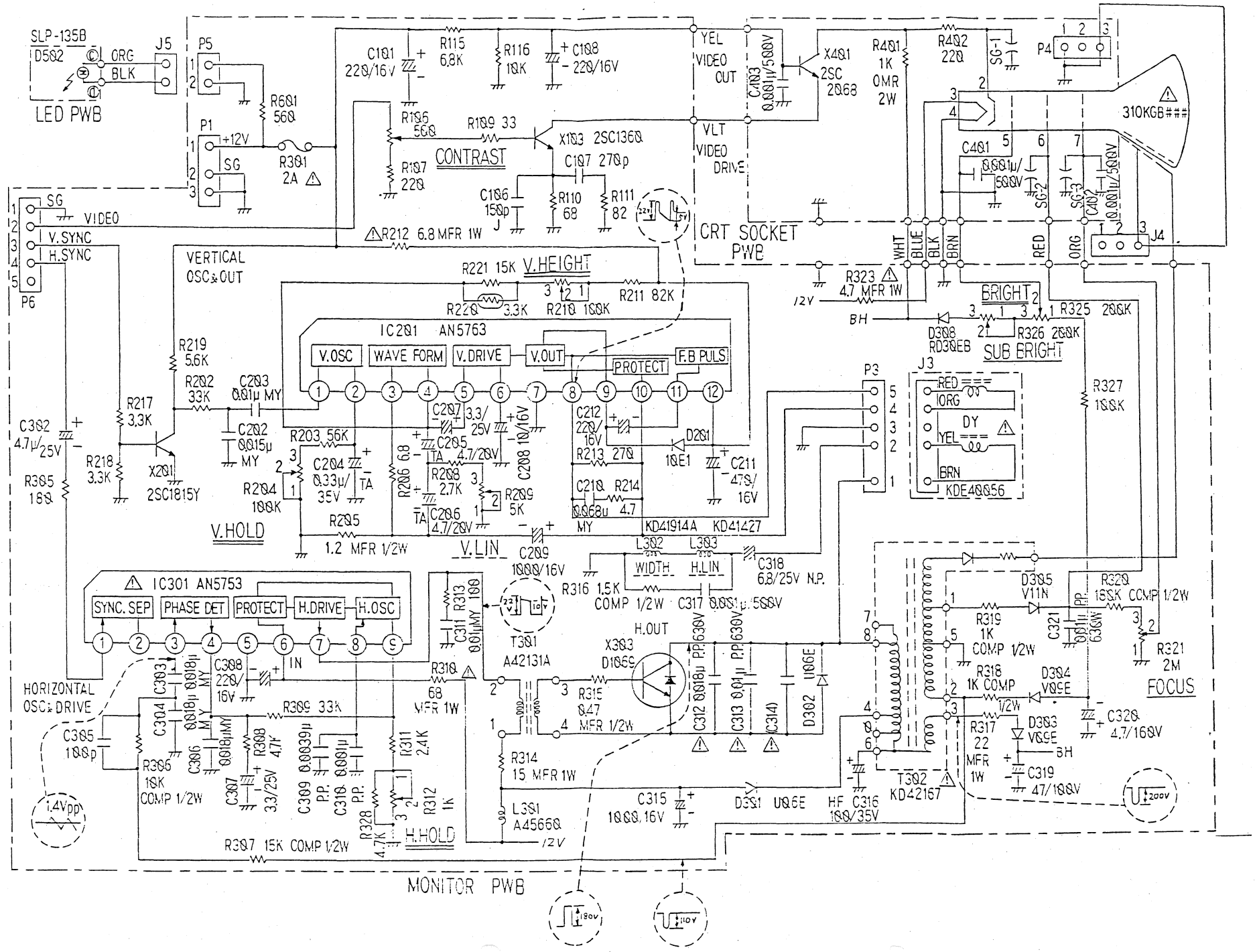


FIG. 10-3 VG-920 MONITOR PWB

J301
COMM

PIN NO.	SIGNAL NAME
1	
2	COMTXD
3	COMRXD
4	COMRTS
5	COMCTS
6	COMDSR
7	S G
8	COMRLSD
9	
10	
11	
12	COMSPDI
13	
14	
15	
16	
17	
18	
19	
20	COMDTR
21	
22	
23	COMSPDS
24	
25	

J302
20mA

PIN NO.	SIGNAL NAME
1	-12V
2	TRANSMIT-
3	RECEIVE-
4	
5	TRANSMIT+
6	
7	RECEIVE+
8	S G

J303
S.PRT

PIN NO.	SIGNAL NAME
1	S G
2	PRTTXD
3	PRTRXD
4	PRTRTS
5	PRTDTR
6	PRTDSR
7	S G
8	
9	

J304
P.PRT OPTION

PIN NO.	SIGNAL NAME
1	$\overline{\text{PRSTB}}$
2	PD0
3	PD1
4	PD2
5	PD3
6	PD4
7	PD5
8	PD6
9	PD7
10	$\overline{\text{ACK}}$
11	BUSY
12	
13	
14	
15	
16	
17	S G
18	
19	S G
20	S G
21	S G
22	S G
23	S G
24	S G
25	S G
26	S G
27	S G
28	S G
29	S G
30	S G
31	
32	
33	
34	
35	
36	

J305
VIDEO

PIN NO.	SIGNAL NAME
1	COMPV
2	S G

J306
KEYBOARD

PIN NO.	SIGNAL NAME
1	+5V
2	+5V
3	KBSD
4	KBRD
5	$\overline{\text{KBRTS}}$
6	$\overline{\text{KBBSY}}$
7	S G
8	S G
9	F G

Mini DIN CONNECTOR

PIN NO.	SIGNAL NAME
1	KBRD
2	$\overline{\text{KBRTS}}$
3	+5V
4	KBSD
5	$\overline{\text{KBBSY}}$
6	+5V
7	S G
8	S G
E	F G

J307
POWER

PIN NO.	SIGNAL NAME
1	+5V
2	+5V
3	S G
4	S G
5	S G
6	S G
7	+12V
8	-12V
9	F G

J308
VIDEO

PIN NO.	SIGNAL NAME
1	S G
2	VIDEO
3	VSYNC
4	HSYNC

FIG. 10-4 VG-920 LOGIC PWB CONNECTOR LIST

11. MAINTENANCE PARTS LIST

The parts marked with ⚠ are important. Therefore, be sure to use the specified parts for replacement to secure the safety and maintain the performance.

Display unit parts

Symbol	⚠	Part No.	Description	Remarks	
		DFS0003-005	FRONT PANEL ASY		
		KD10342-012*	REAR COVER		
		KD42100	MASK PLATE		
		KD42245	CAUTION LABEL	English indication	
		KD43073	SERIAL LABEL	English indication	
		KD31717-00A	STAND ASY		
		KD31623-002	BOTTOM PLATE		
		TFS0021	PWB CASE ASY		
	⚠	TSS0025	POWER BRACKET ASY	Set at 100V	
	⚠	TSS0038-001	POWER BRACKET ASY	Set at 200V	
	⚠	KD42530C*	SWITCHING REGULATOR UNIT		
	⚠	02-TFK-0114*	NOISE FILTER		
	⚠	FH033*	FUSE HOLDER		
	⚠	KDE40067*	POWER SWITCH		
	⚠	T-S12NB6X2-A*	VOLTAGE SELECT SWITCH		
	⚠	QMF51U2-2R0*	FUSE	For 100V	
	⚠	QMF51U2-1R0*	FUSE	For 200V	
	⚠	310KGB(QA)N*	CRT TUBE	AMBER	
	⚠	310KGB4N*	CRT TUBE	WHITE	
	⚠	310KGB31N*	CRT TUBE	GREEN	
	⚠	DPS0032-001	MONITOR PWB ASY		
R301	⚠	QMF51U1-2R0*	FUSE	For MONITOR PWB	
	⚠	KDE40056*	DY		
		TPS0024-001	LOGIC PWB ASY	D-SUB mm screw conforming to ASCII specifications	

Display unit parts

Symbol	⚠	Part No.	Description	Remarks	
		TPS0024-002	LOGIC PWB ASY	D-SUB inch screw conforming to ASCII specifications	
		TPS0024-003	LOGIC PWB ASY	D-SUB mm screw conforming to ASCII specifications	With P.PRT option
		TPS0024-006	LOGIC PWB ASY	D-SUB inch screw conforming to ASCII specifications	With P.PRT option

Keyboard unit parts

Symbol	⚠	Part No.	Description	Remarks	
		KDE40077-002	KEYBOARD PWB ASY	ASCII specifications	
		KD10410-002	KEYBOARD CASE	Upper cover	
		KD21211-002	FUNCTION PLATE	ASCII specifications	

Accessories

Symbol	⚠	Part No.	Description	Remarks	
	⚠	KDH40058*	POWER CORD		Note 1
	⚠	KDH40121*	POWER CORD		Note 2
	⚠	KD42532	POWER CORD		Note 3

Notes 1 through 3: See Notes 1 through 3 for Section 13 "PACKING

Tools

Symbol	⚠	Part No.	Description		
		JT8005	Signal loop-back Connector	For EIATST, SIGTST	D-Sub
		JT8007	Signal loop-back Connector	For SPRTST	D-Sub
		JT8006	Signal loop-back Connector	For CLPTST	Mate-N -Loc

LOGIC PWB

Symbol	⚠	Part No.	Description	Remarks	
6K		D780C-1	IC		
1C,1E,7D		HM6264P-15	IC		x3
1F, 7F		2764	IC	250ns	x2
2F		HM6116LP-4	IC		
1M		M5L8255AP-5	IC		
5D		μPD8253C-5	IC		
1A		SCN2674BC4N40	IC		
5E,5F,5H		SCN2641CC1N24	IC		x3
1K		SCB2675BC5N40	IC		
2C,2E		8X371	IC		x2
7C		X2212	IC		
4N,4P,5P		μA9636AC	IC		x3
5M,5N		Am26LS32A	IC		x2
7H		27256	IC	300ns	
4D		SN74LS00N	IC		
4J		SN74LS02N	IC		
2L,4H		SN74LS04N	IC		x2
2Kb		SN74LS08N	IC		
4F		SN74LS14N	IC		
4E,4K,7M		SN74LS32N	IC		x3
4B,4C		SN74LS74AN	IC		x2
2M		SN74LS86N	IC		
3L		SN74LS138N	IC		
4M		SN74LS139N	IC		

LOGIC PWB

Symbol	⚠	Part No.	Description	Remarks	
3D		SN74LS148N	IC		
5C		HD74LS154P	IC		
2J,3J,3K		SN74LS157N	IC		x3
2B,3C		SN74LS244N	IC		x2
1N		SN74LS244N	IC	For P.PRT OPTION	
2A,3F		SN74LS245N	IC		x2
3B,3E,3H		SN74LS273N	IC		x3
7A		SN74LS174N	IC		
2Ka		SN74LS21N	IC		
2N,5L		SN7406N	IC		x2
3M		SN7407N	IC		
4L		SN74S38N	IC		
3Na,3Nb		PS2001B	IC		x2
D1,D2,D3		1S2075K	DIODE		x3
ZD1		RD6.8EB	Z. DIODE		
ZD2,ZD3		RD16EB	Z. DIODE		x2
X1,X2		2SC1360(C)	TRANSISTOR		x2
X3,X4,X5		2SC458K(C)	TRANSISTOR		x3
R27		QRD141J-270S	C. RESISTOR	27Ω 1/4W	
R6		QRD141J-470S	C. RESISTOR	47Ω 1/4W	
R17, R18		QRD141J-680S	C. RESISTOR	68Ω 1/4W	x2
R13		QRD141J-750S	C. RESISTOR	75Ω 1/4W	
R7,R12,R25, R36,R37		QRD141J-221S	C. RESISTOR	220Ω 1/4W	x5
R21		QRD141J-471S	C. RESISTOR	470Ω 1/4W	
R11,R16,R29		QRD141J-681S	C. RESISTOR	680Ω 1/4W	x3
R9		QRD141J-911S	C. RESISTOR	910Ω 1/4W	
R3,R4,R5, R15,R19,R20, R31,R32,R33, R35,R40,R53, R54,R56,R57, R58		QRD141J-102S	C. RESISTOR	1KΩ 1/4W	x16
R14		QRD141J-102S	C. RESISTOR	1KΩ 1/4W For P.PRT OPTION	
R10		QRD141J-222S	C. RESISTOR	2.2KΩ 1/4W	
R55		QRD141J-362S	C. RESISTOR	3.6KΩ 1/4W	

LOGIC PWB

Symbol	⚠	Part No.	Description	Remarks	
R22		QRD141J-472S	C. RESISTOR	4.7KΩ 1/4W	
R1,R8,R42 R43,R44		QRD141J-562S	C. RESISTOR	5.6KΩ 1/4W	x5
R34		QRD141J-103S	C. RESISTOR	10KΩ 1/4W	
R41,R45,R46 R47,R48,R49, R50		QRD141J-273S	C. RESISTOR	27KΩ 1/4W	x7
R24		QRD141J-683S	C. RESISTOR	68KΩ 1/4W	
R39,R51		QRD141J-753S	C. RESISTOR	75KΩ 1/4W	x2
R26		QRD141J-104S	C. RESISTOR	100KΩ 1/4W	
R38		QRD141J-474S	C. RESISTOR	470KΩ 1/4W	
R2		QRX121F-31R6	M.F.R	31.6Ω 1/2W	
RA1		8R103K	SIL RESISTOR	10KΩ	
C33,C34,C51		QFN41HK-102	M. CAPACITOR	1000pF 50V	x3
C32		QFN41HK-102	M. CAPACITOR	1000pF 50V For P.PRT OPTION	
C31		QFN41HK-104	M. CAPACITOR	0.1μF 50V	
C35		QET21CR-226	E. CAPACITOR	22μF 16V	
C36,C47		QET21CR-227	E. CAPACITOR	220μF 16V	x2
C48,C49		QET21ER-106	E. CAPACITOR	10μF 25V	x2
C37,C38,C39, C40,C41,C42, C43,C44,C45, C46		QET21CR-106	E. CAPACITOR	10μF 16V	x10
C1,C2,C3 C4,C5,C6, C7,C8,C9, C10,C11,C12, C13,C14,C15, C16,C17,C18, C19,C20,C21, C22,C23,C24, C25,C26,C27, C28,C29,C30		RPE122F104Z50	C. CAPACITOR	0.1μF 50V	x30

LOGIC PWB

Symbol	⚠	Part No.	Description	Remarks	
C50		QCS21HJ-151	C. CAPACITOR	150pF 50V	
XTL1		KDE40069-001	X-TAL	3.6864MHz	
XTL2		KDE40069-007	X-TAL	15.9686MHz	
XTL3		KDE40069-008	X-TAL	23.6710MHz	
1F,7F,7H		DICF-28CS	IC SOCKET		x3
J306		TCF7680-01-201	CONNECTOR	Mini DIN	
J301		DB-25PA-N	CONNECTOR	D-SUB 25P	
J303		DE-9PA-N	CONNECTOR	D-SUB 9P	
J305		BNC-LR-PC-4	CONNECTOR	BNC	
J302		KDE40068	CONNECTOR		
J304		KDE40066	CONNECTOR	For P.PRT OPTION	
J307		S9B-XH-A	CONNECTOR		
J308		S4B-XH-A	CONNECTOR		
TP1,TP2		KD41377	TEST POINT		x2
		KDH40077	JUMP WIRE		

MONITOR PWB

Symbol	⚠	Part No.	Description	Remarks	
IC201		AN5763	IC		
IC301	⚠	AN5753	IC		
X103		2SC1360	TRANSISTOR		
X201		2SC1815Y	TRANSISTOR		
X303		2SD1069	TRANSISTOR		
X401		2SC2068	TRANSISTOR		
D201		10E1	DIODE		
D301,D302		U06E	DIODE		x2
D303,D304		V09E	DIODE		x2
D305		V11N	DIODE		
D502		SLP-135B-08	LED	RED	
D308		RD30EB	Z. DIODE		
T301		A42131A-1*	H. DRIVE TRANS		
T302	⚠	KD42167*	H.V TRANS		
L301		A45660-001	CHOKE COIL		
L302	⚠	KD41914A*	H. WIDTH COIL		
L303	⚠	KD41427	H. LIN COIL		
R106		KD42177-501	V. RESISTOR	500Ω CONTRAST	
R204		KD42177-104	V. RESISTOR	100KΩ V.HOLD	
R209		EVLS3AA00B53	V. RESISTOR	5KΩ V.LIN	
R210		EVLVOAA00B15	V. RESISTOR	100KΩ V.HEIGHT	
R312		KD42177-102	V. RESISTOR	1KΩ H.HOLD	
R321		VG151HB2M	V. RESISTOR	2MΩ FOCUS	
R325		EVLVOAA00B25	V. RESISTOR	200KΩ SUB BRIGHT	
R326		KD42177-204	V. RESISTOR	200KΩ BRIGHT	

MONITOR PWB

Symbol	⚠	Part No.	Description	Remarks	
R314		QRG019J-150	Oxidized metal film resistor	15Ω 1W	
R317		QRG019J-220	Oxidized metal film resistor	22Ω 1W	
R310	⚠	QRG019J-680	Oxidized metal film resistor	68Ω 1W	
R401		QRG029J-102	Oxidized metal film resistor	1KΩ 2W	
R315		QRX126K-R47	Metal film resistor	0.47Ω 1/2W	
R205		QRX126K-1R2	Metal film resistor	1.2Ω 1/2W	
R323	⚠	QRX019J-4R7	Metal film resistor	4.7Ω 1W	
R212	⚠	QRX019J-6R8	Metal film resistor	6.8Ω 1W	
R220		A04292-103	NEGATIVE THER-MISTOR	3.3KΩ	

MONITOR PWB

Symbol	⚠	Part No.	Description	Remarks	
R601		QRC122K-561	COMP RESISTOR	560Ω 1/2W	
R318,R319		QRC122K-102	COMP RESISTOR	1KΩ 1/2W	x2
R316		QRC122K-152	COMP RESISTOR	1.5KΩ 1/2W	
R306		QRC122K-103	COMP RESISTOR	10KΩ 1/2W	
R307		QRC122K-153	COMP RESISTOR	15KΩ 1/2W	
R320		QRC122K-184	COMP RESISTOR	180KΩ 1/2W	
R214		QRD148J-4R7S	C. RESISTOR	4.7Ω 1/4W	
R206		QRD148J-6R8S	C. RESISTOR	6.8Ω 1/4W	
R109		QRD148J-330S	C. RESISTOR	33Ω 1/4W	
R110		QRD148J-680S	C. RESISTOR	68Ω 1/4W	
R111		QRD148J-820S	C. RESISTOR	82Ω 1/4W	
R313		QRD148J-101S	C. RESISTOR	100Ω 1/4W	
R305		QRD148J-181S	C. RESISTOR	180Ω 1/4W	
R107,R402		QRD148J-221S	C. RESISTOR	220Ω 1/4W	x2
R213		QRD148J-271S	C. RESISTOR	270Ω 1/4W	
R311		QRD148J-242S	C. RESISTOR	2.4KΩ 1/4W	
R208		QRD148J-272S	C. RESISTOR	2.7KΩ 1/4W	
R217,R218		QRD148J-332S	C. RESISTOR	3.3KΩ 1/4W	x2
R308,R328		QRD148J-472S	C. RESISTOR	4.7KΩ 1/4W	x2
R219		QRD148J-562S	C. RESISTOR	5.6KΩ 1/4W	
R115		QRD148J-682S	C. RESISTOR	6.8KΩ 1/4W	
R116		QRD148J-103S	C. RESISTOR	10KΩ 1/4W	
R221		QRD148J-153S	C. RESISTOR	15KΩ 1/4W	
R202,R309		QRD148J-333S	C. RESISTOR	33KΩ 1/4W	x2
R203		QRD148J-563S	C. RESISTOR	56KΩ 1/4W	
R211		QRD148J-823S	C. RESISTOR	82KΩ 1/4W	
R327		QRD148J-104S	C. RESISTOR	100KΩ 1/4W	
C207,C307		QET51EM-335	E. CAPACITOR	3.3μF 25V	x2
C302		QET51EM-475	E. CAPACITOR	4.7μF 25V	
C320		QET52CM-475	E. CAPACITOR	4.7μF 160V	
C318	⚠	A03054-685	E. CAPACITOR	6.8μF 25V	
C208		QET51CM-106	E. CAPACITOR	10μF 16V	
C319		QET52AM-476	E. CAPACITOR	47μF 100V	
C316		ECEA1VF101R	E. CAPACITOR	100μF 35V	
C101,C108 C212,C308		QET51CM-227	E. CAPACITOR	220μF 16V	x4

MONITOR PWB

Symbol	⚠	Part No.	Description	Remarks	
C211		QET51CM-477	E. CAPACITOR	470μF 16V	
C209,C315		QET51CM-108	E. CAPACITOR	1000μF 16V	x2
C203,C311		QFM81HK-103	MYLAR CAPA-CITOR	0.01μF 50V	x2
C202		QFM81HK-153	MYLAR CAPA-CITOR	0.015μF 50V	
C303,C304 C306		QFM81HK-183	MYLAR CAPA-CITOR	0.018μF 50V	x3
C210		QFM81HK-683	MYLAR CAPA-CITOR	0.068μF 50V	
C310		QFP31HJ-102	PP CAPACITOR	0.001μF 50V	
C309		QFP31HJ-392	PP CAPACITOR	0.0039μF 50V	
C313,C321	⚠	QFP32XK-103	PP CAPACITOR	0.01μF 630V	x2
C312	⚠	QFP32XK-183	PP CAPACITOR	0.018μF 630V	
C305		QCS21HJ-101	C. CAPACITOR	100pF 50V	
C106		QCS21HJ-151	C. CAPACITOR	150pF 50V	
C107		QCS21HJ-271	C. CAPACITOR	270pF 50V	
C317,C401 C402,C403		QCY22HP-102	C. CAPACITOR	0.001μF 500V	x4
C204		CS15E1VR33MIS	TANTAL CAPA-CITOR	0.33μF 35V	
C205,C206		CS15E1D4R7MIS	TANTAL CAPA-CITOR	4.7 μF 20V	
		A75802-5	PLUG ASY	5P DY	
		A75802-3	PLUG ASY	3P 12V	
		171825-5	PLUG ASY	5P VIDEO IN	
		171825-3	PLUG ASY	3P CRT EARTH	
		171825-2	PLUG ASY	2P LED	
F301		PU51212	CONTACT CLIP		x2
X303		C40635-A	HEAT SINK		
SG-1		A04237-1	SPARK GAP		
SG-2,SG-3		SP10N	SPARK GAP		x2
		A44397-C*	CRT SOCKET		
		KD31698-00A	LED WIRE ASY		

12. PARTS MOUNTING DIAGRAMS

(1) VG-920 LOGIC PWB Parts Mounting Diagram Fig. 12-1

(2) VG-920 MONITOR PWB Parts Mounting Diagram Fig. 12-2

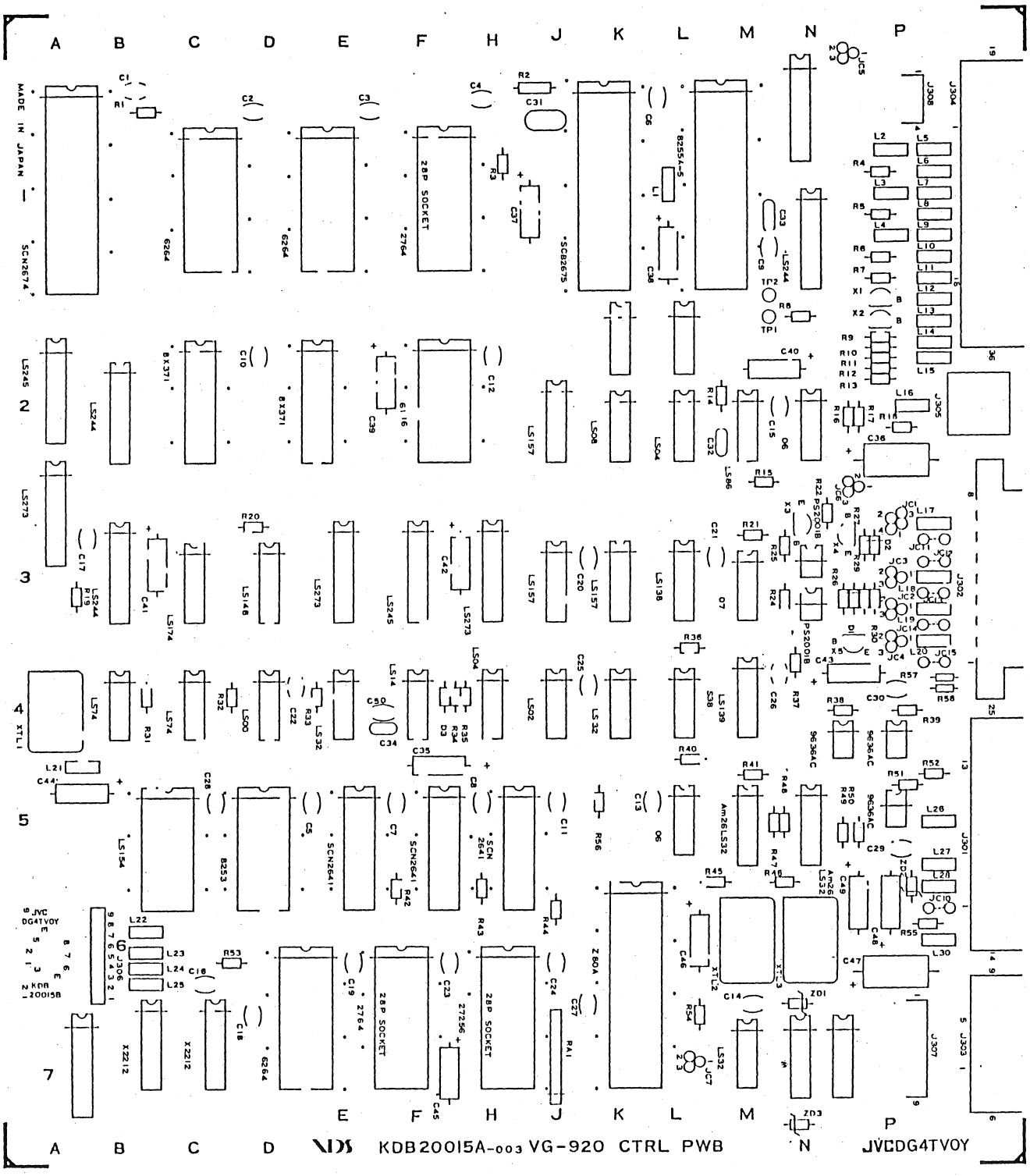
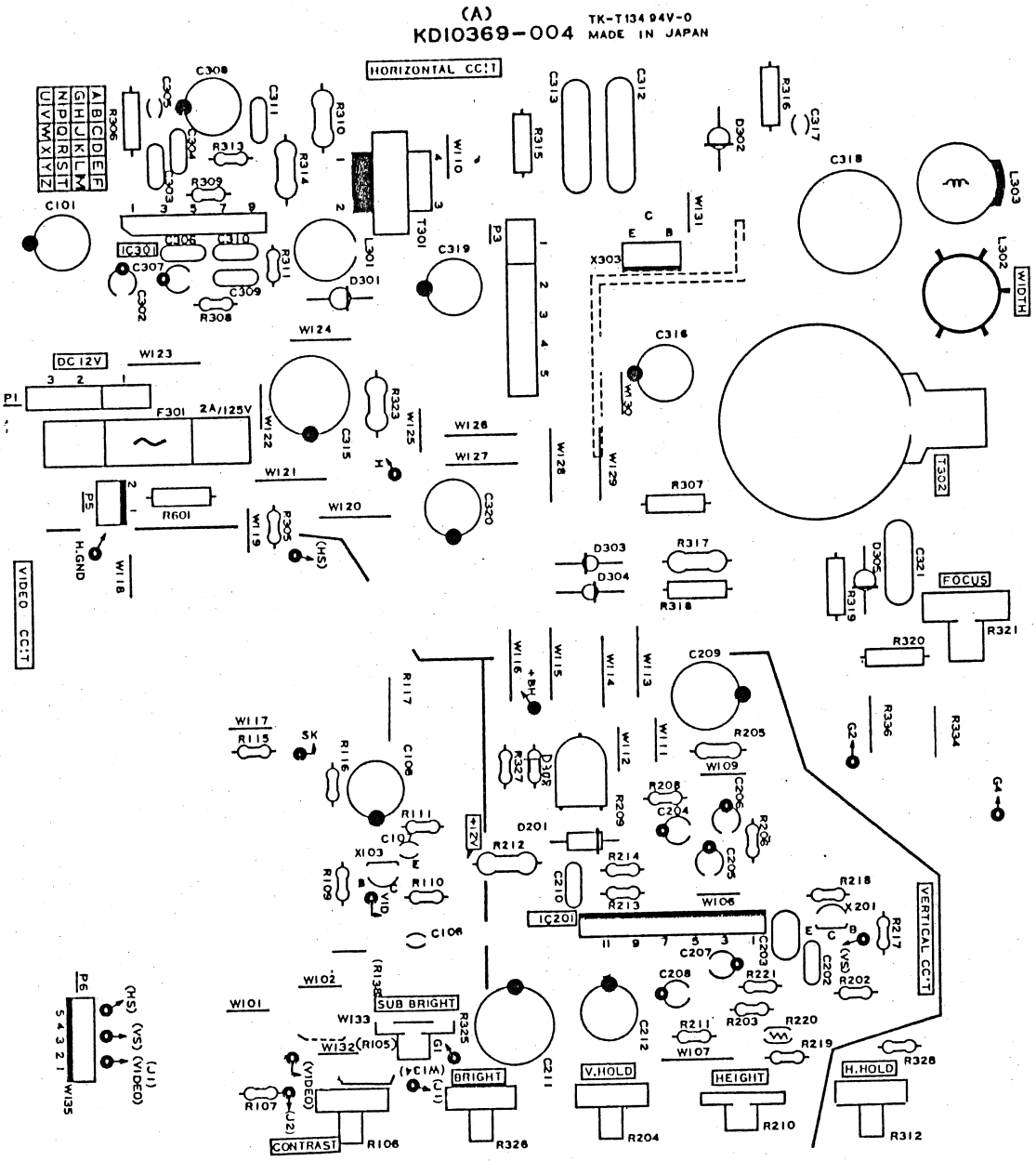


Fig. 12-1-1 Logic PWB Parts Mounting Diagram



Fig, 12-1-2 Monitor PWB Parts Mounting Diagram

13. PACKING PARTS AND ACCESSORIES

(1) Display unit packing parts

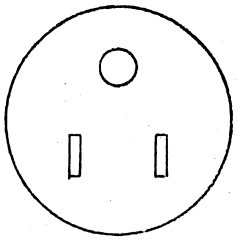
Description	Part No.	Remarks	
PACKING ASY	KD31735-01N		
CUSHION	KD10362		
CUSHION	KD21084		
POLY BAG	KD42182		
LABEL	KD43234-002		

(7) Keyboard unit

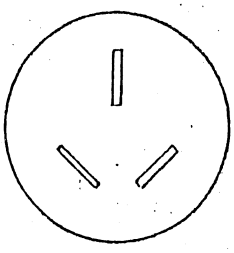
Description	Part No.	Remarks	
PACKING ASY	KD10415-00B		
POLY BAG	KD42272		
LABEL	KD43234-002		
POLY BAG	KD41811-008	FOR KEYBOARD CABLE	

(8) Display unit accessories

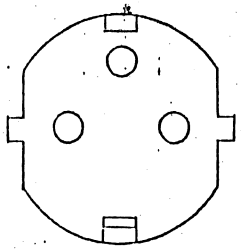
Description	Part No.	Remarks	
POWER CORD	KDH40058*		Note 1
POWER CORD	KDH40121*		Note 2
POWER CORD	KD42532		Note 3
CONNECTOR	DB-25S-N	D-SUB 25P	
J. SHELL	DB-C3-J10	For D-SUB inch screw	
LOCK DEVICE	D20419-21	For D-SUB inch screw	
INST MANUAL	KD43027	English	
FUSE	QMF51U2-2RO*	For 100V	
FUSE	QMF51U2-1RO*	For 200V	



Note 1



Note 2



Note 3