PowerPC™

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Changes in Long Trail from Pass 1 to Pass 2

Application Note AN-PPC-017

This document outlines the major changes between the Pass 1 release and the Pass 2 release of the Longtrail CHRP PowerPC Reference Design. The document does not attempt to describe every minor implementation difference. It is a bridge between the Pass 1 specification and the Pass 2 specification.

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1.1 Purpose and Organization

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1.2 Major Changes

The major changes are listed with a paragraph or two of rationale and explanation. Subordinate changes which were driven by the major change are listed in indented format under each major change. All changes are driven by the desire to make the board less expensive and one that OEMs can very quickly bring to market.

1.2.1 Processor Card Replaced With PGA Processor in ZIF Socket

Major customers indicated a strong preference for this mode of processor attachment in order to better fit their business model. IBM has announced availability of all 60x PowerPC processors in PGA. A common pinout has been designed so that the 603 family or 604 family processors may be interchanged in a common socket. The socket chosen is a 17x17 fully populated array similar to socket 3. Low cost fan sink and or passive heat sink solutions are available.

1.2.1.1 VRM Chosen for Regulator

The 40–pin VRM module used in Pentium–Pro designs was chosen because it is expected to be a readily available commodity and it meets requirements. OEMs may be able to make certain optimizations by setting the core voltage to values other than 3.3 or 2.5 volts.

1.2.1.2 Autoconfigure PAL Replaced with Jumpers or ”KEY” card

The processor card had seven presence detect bits which were used to drive a PAL which configured the bus speed, PLL ratio, and bus mode. The PGA socket does not contain these presence bits. Accordingly, jumpers are required to set these parameters for the particular type and speed of processor installed. Longtrail is designed to accept any 60x family processor except the original 603 which is near end of life.

A socket is defined for a ”KEY” card which may be used to set all configuration variables without the use of jumpers. OEMs may choose either option or both when assembling the board. IF the ”KEY” card option is chosen, a small 20 pin card must be provided with each system to customize the board to the mated processor. The card has only wires that replace jumper connections. A different ”KEY” would have to be provided to the customer in in order to upgrade. IBM does not supply ”KEY” cards. Jumpers are required:

- 4 – to program the VRM output voltage
- 3 – to set the cpu/pci bus frequencies to 50/25, 27.5/55, 60/30, or 66/33 MHz as best optimizes the CPU speed for the inserted processor
- 4 – to set the CPU PLL ratio
- 2 – to set the bus mode according to the family of the inserted processor.

1.2.1.3 Debug Support Modified

The Pass 1 offering included a 60x bus probe card set compatible with the processor card. This is not appropriate to the PGA processor. HP offers the HP E2465A PowerPC 604 PGA Preprocessor Interface product which may be adapted to probe the 60x bus at the PGA processor. Other vendors may have similar offerings. IBM will not offer a probe device.

1.2.2 Golden Gate Bridge Chip Set Upgraded to Pass2 Silicon

1.2.2.1 COASt L2 Cache Modules Supported

The GG designers chose to provide support for commodity L2 cache modules available for X86 systems. Cache modules supporting linear burst order are required. The 182–pin standard on Pass 1 has been abandoned. The chip set contains support for both burst and flow–though cache designs. Both the 8–bit tag and 11–bit tag versions are supported. The board utilizes the FX connector and can physically accept any version of the COASt module.

1.2.2.2 SDRAM Support Added

Support for SDRAM has been implemented in the Pass 2 design. The Pass 1 board supported it, but the function was not in the first silicon.

1.2.2.3 GG Refinements

Pass 2 silicon contains additional buffers and other refinements which speed the operation but do not affect function. Firmware has minor impacts due to register changes.

1.2.3 Design changed to Four–layer

Customers indicated that the design must be on a four–layer board in order to be cost competitive. Pass 1 was a six–layer design. This decision drove a decision to substantially change the pinout of the pass 2 GG chips.

1.2.4 I/O Cable Connector Scheme Changed

The Pass 1 board used connectors in order to provide egress for both the Apple–type connectors and the IBM compatible type connectors. The Pass 2 board uses less costly connectors and allows the OEM options to assemble the board in a way that cost–optimizes for Apple–type connectors or for compatible–type connectors. The OEM may also support both sets of connectors. The keyboard connector site has a dual footprint that may be populated with either an ADB connector or a stacked KB/MSE connector. The VGA connector space has been eliminated.

1.2.5 Clock Chip Replaced

IC works announced a clock chip which combines the processor, PCI, and SDRAM clocks into one low–cost clock chip. We adopted this chip. There is virtually no penalty in the cost of the board to support SDRAM.

1.2.6 308 Errata Embedded

There are minor hardware errata outstanding against the current version of the NS ’308 chip. These have been embedded. The schematic indicates how to reverse the changes when the chip is upgraded.

1.2.7 3.3V MACROM Standard Supported

A standard for 3.3v MACROM SIMMs has been worked out with Apple Computer. There are minor pinout changes but no functional differences. Our objective is to use standard 3.3V MACROM SIMMs to be offered by Apple Computer.

1.2.8 Tollgate ISA Bridge

Tollgate has been upgraded to pass 2 silicon. It is currently being tested on pass 2 boards. The plan is to build pass 2 boards with Tollgate. OF will be modified accordingly.

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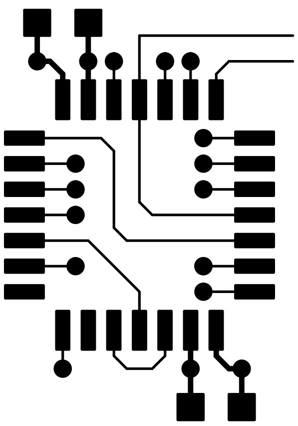

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