

# **OHCI Registers and Interrupts**

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L. Wilson, J. Bennett / 1394 OpenHCI Registers

## **Set/Clear Registers**

- Some registers have separate set and clear addresses
- This avoids the need to perform read/mask/write operations
  - A '1' in the set register sets the bit. A '1' in the clear register clears the bit
  - A '0' in either register leaves the bit unchanged
- These registers are marked as "set" and "clear" registers

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**HCI** 

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## **Interrupt Registers**

- Event (set and clear) and Mask (set and clear)
- Specific bits

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- DMA complete
  - Asynch request & response, isoch transmit & receive
- Asynch Context Progress
  - Receive Request Received, Receive Response Received
- Erroneous Behavior
  - *Posted write*: Asynch data received and acknowledged, but there was an error sending it to memory
  - Cycle Lost: A cycle start was expected, not received
  - Cycle Inconsistent: Cycle start number didn't match Cycle Timer Register
  - Unrecoverable: Some error causing all or some subunits to stop (such as master abort on a context program fetch)
  - *Cycle Too Long*: > 125 usec between cycle start and subaction gap

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### PEN Interrupt Registers

- Specific Bits (continued)
  - Self ID Complete
  - Bus Reset Encountered
  - Phy request through status transfer
  - Phy register received
  - New isoch cycle started
  - Cycle 64 Seconds
  - Vendor Specific

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#### **TIPEN Isoch Interrupt Registers**

- Additionally, the Isochronous registers have more specific interrupts, with interrupt masks
  - Isoch Transmit Event (set and clear)
  - Isoch Transmit Mask (set and clear)
  - Isoch Receive Event (set and clear)
  - Isoch Receive Mask (set and clear)
- All registers are 32 bits. Each bit represents an isochronous context number

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#### **Filter / Mask Registers**

#### Isoch Receive Channel Mask (set and clear)

- 64 bit register: Bit location indicates channel number
- When set, channel is masked. Packets are ignored
- Asynch Request Filter (set and Clear)
  - Used for requests that do not access first 1K of CSR Configuration ROM
  - 64 bit register: Bit location indicates channel number
  - When set, request is ignored.
- Physical Request Filter
  - Used for asynch requests when the offset is below 48'h0001\_0000\_0000
  - 64 bit register: Bit location indicates channel number
  - When set, request is ignored.

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#### **TOREN Compare/Swap Registers**

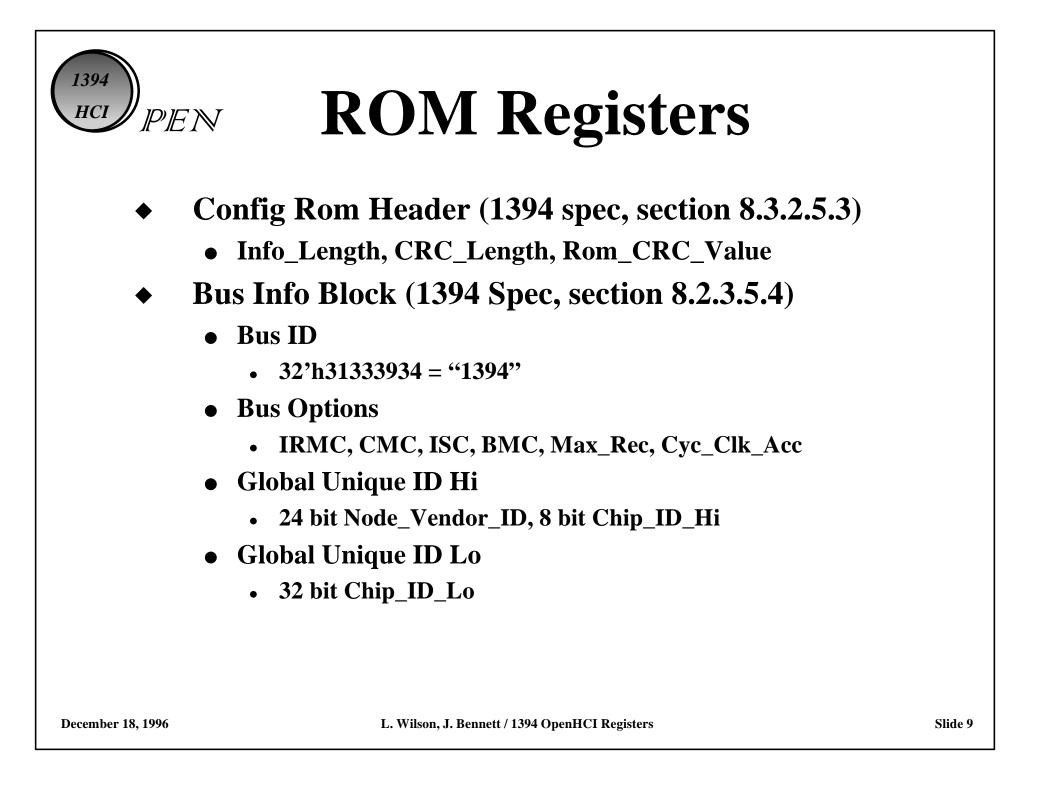
- **CSRReadData 32 bits**
- **CSRCompareData 32 bits**
- **CSRControl** 
  - Compare/swap done
  - Selection
    - 2'h0 = BUS\_MANAGER\_ID
    - 2'h1 = BANDWIDTH\_AVAILABLE
    - 2'h2 = CHANNELS\_AVAILABLE\_HI
    - 2'h3 = CHANNELS\_AVAILABLE\_LO

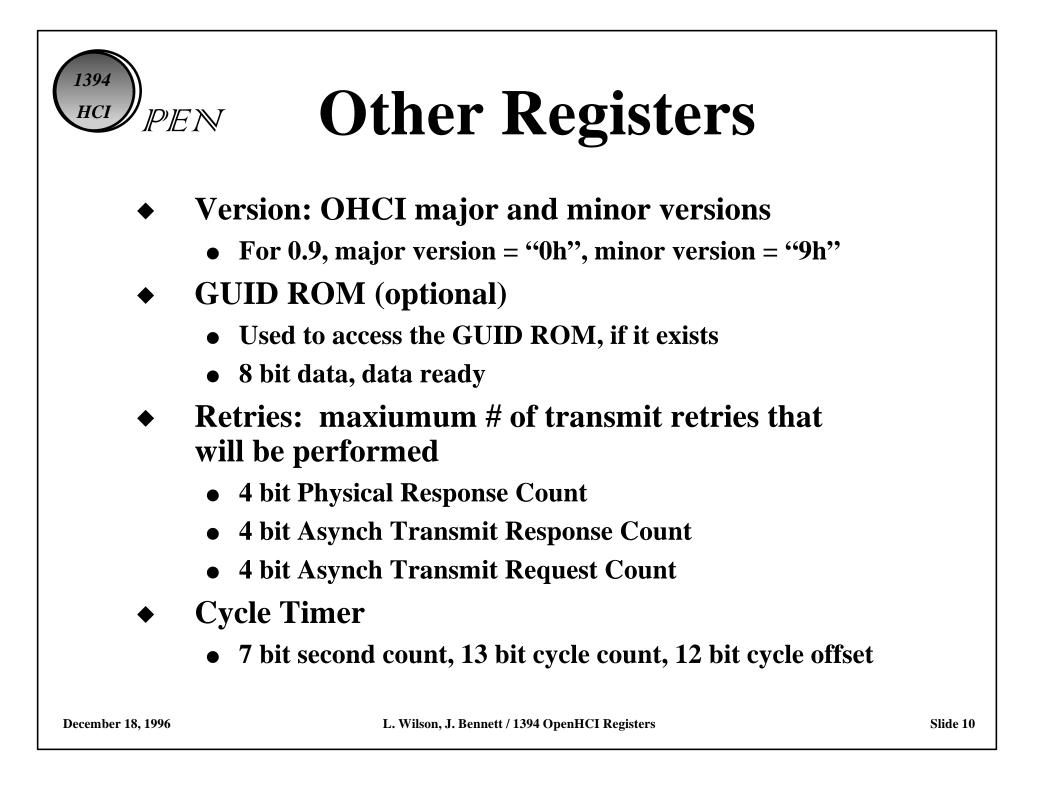
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### PEN Host / Link Registers

- Host Control
  - Link Enabled, Host Controller soft reset, PostedWriteEnable
- LinkControl: Specific bits
  - External/Internal cycle source
  - Enables OHCI as cycle master, enables cycle timer
  - Allows PHY packet and self ID reception
- NodeID
  - Valid ID, is root, cable power is OK
  - Bus Number, Node Number
- PhyControl: Register reads/writes
  - Register access done
  - 4 bit address, 8 bit read data, read/write direction, 8 bit write data

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#### <sup>1394</sup> PEN Other Registers cont.

- Configuration Rom Mapping Register
  - 1k Aligned 32 bit address
- Posted Write Address
  - 64 bit address
  - When a posted write error occur, 16 bit sourceID, 48 bit address stored, interrupt event is set
  - This is a Queue: When interrupt event cleared, next in queue appears at this address
- Vendor Company ID
  - registration number with IEEE
  - 8 bit vendor unique, 24 bit company ID

