z/OS V1R13

BCP supervisor: RMODE 64 stage 1

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Session objectives

- Describe RMODE 64 changes

Overview

- Problem
  - DB2® has code that “lives” with its data. It costs time to move that code from where the data is read in (above 2G) to where it can be run (below 2G)
- Solution:
  - Provide support for this sort of code to be above 2G. Among other restrictions, it must not call any system services
- Benefit / Value: Performance

Usage and invocation

- Today: z/OS® supports directed load of non-executable code above 2G.
- New: This support is now extended to allow there also to be executable code, as long as that code does not invoke system services. It may get external or I/O interrupts or retryable machine checks or resolvable program interrupts and will have its status properly saved and later restored.
- Diagnostics-wise: IPCS can already handle displaying data above 2G. SLIP can already handle ranges above 2G. GTF is extended to capture 16-byte PSW information. System trace is extended to capture 16-byte PSW information.

Key control structures

- Today: RBOPSW contains the 8-byte PSW for dispatch
- Tomorrow: RBOPSW still contains that value, but it is not relied upon
  - XSBOPSW16 contains the official (16-byte PSW)
  - XSB_Orig_RBOPSW contains the original value of RBOPSW
  - If a program (IBM or ISV or customer) modifies RBOPSW (as many do), the system detects that RBOPSW now differs from XSB_Orig_RBOPSW and makes the corresponding update to XSBOPSW16.
    - An update to bytes 0-3 is copied directly
    - A “delta” update to the address is applied as a delta to the 8-byte address (this is defined as a change of plus-or-minus 6)
    - A “replacement” of the address results in replacing the 8-byte address with the 4-byte replacement
- In macro CVT: new field CVTBSM0F is defined. A recovery routine that wants to retry to an address above 2G would set up 64-bit retry GPR 15 (such as by setting field SDWAG6415 and indicated RETREGS=64 on SETRP) with the pointer-defined address of the “real” retry point. At CVTBSM0F, BSM 0,15 is issued, so an address above 2G must have bit 63 on so that the target will get control in AMODE 64.
- In macro IHAEPIE: new field EPIEPS16 is added. This is the 16-byte error PSW

Usage and invocation (IEARBUP)

- IEARBUP service:
- Extension to PSWADDR parameter
  - The high 33 bits must be zero unless the result is to be AMODE 64.

Usage and invocation (changed messages)

- Message IEA995I is changed.
- When the error address is below 2G, there is no change. The PSW address line looks like

```
PSW AT TIME OF ERROR xxxxxxxx xxxxxxxx ILC x INTC xx
```

- When the error address is above 2G, that line is not presented; instead two lines are used:

```
PSW AT TIME OF ERROR xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
  ILC x INTC xx


  IEA995I SYMPTOM DUMP OUTPUT
  {SYSTEM|USER} COMPLETION CODE=cde [REASON CODE=reason-code]
  TIME=hh.mm.ss SEQ=ssssss CPU=cccc ASID=asid
  PSW AT TIME OF ERROR xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
  ILC x INTC xx
  ....
```

- Message IEE844W is changed. The current text and explanation shows the PSW line as
  PSW: cccccccc cccccccc
- This is incorrect in that PSW is left-aligned not indented, but in any case is changed to
  PSW: cccccccc cccccccc cccccccc cccccccc
- The current text shows the explanation for the first line in the PER case as “address is the address where the PER event occurred”. This changes to “address is the 8-byte address where the PER event occurred”.

```
IEE844W   SLIP TRAP xxxx MATCHED.  ACTION=WAIT TYPE=yy
  [REMOTE ACTION{S} NOT PERFORMED]
  PER INFO:  cccc aaaaaaaa_aaaaaaaa
  PSW:       cccccccc cccccccc cccccccc cccccccc
  CR 3-4:    dddddddd eeeeeeee
  AR/GR 0-1: aaaaaaaa/gggggggg_gggggggg   aaaaaaaa/gggggggg_gggggggg
  ....
```

- Messages BLW004A and IEA500A are changed: They both describe the PSW as “The program status word ...”. The description in both changes to “The 16-byte program status word ...”

```
  BLW004A   RESTART INTERRUPT DURING {jobname stepname | UNKNOWN JOBNAME}
  ASID=asid MODE=mode PSW=pppppppp pppppppp pppppppp pppppppp
  SYSTEM NON-DISPATCHABILITY INDICATOR IS {ON|OFF}
  [text]
  REPLY ABEND TO ABEND INTERRUPTED PROGRAM,
        RESUME TO RESUME INTERRUPTED PROGRAM,
        REPAIR TO PERFORM REPAIR ACTIONS.


  IEA500A   RESTART INTERRUPT DURING {jobname stepname|UNKNOWN JOBNAME}
  ASID=asid MODE=mode PSW=pppppppp pppppppp pppppppp pppppppp
  REPLY RESUME TO RESUME INTERRUPTED
  PROGRAM REPLY ABEND TO ABEND INTERRUPTED PROGRAM
  [PREVIOUS REPLY WAS INVALID, ENTER A VALID REPLY]
```

Message IEE854I is changed. Current lines

```
PSW AT TIME OF ERROR=070C0000 80000002 ILC=2 INT=01
  TRANSLATION EXCEPTION ADDR=7F1EF000
```

are changed. The first line is split into 2 and extended for a 16-byte PSW. The second is extended for an 8-byte address:

```
PSW AT TIME OF ERROR=07040000 8000000 00000000 0000002
  ILC=2 INT=01
  TRANSLATION EXCEPTION ADDR=00000000_7F1EF000
```

Usage and invocation (changed diagnostics)

- Some system Trace records are changed to contain 16-byte PSWs. The formatted data will be updated. The physical records will be changed (incompatibly) as well. This applies to the following trace entries: Dispatcher, I/O, External interrupt, SVC, SSRV, Program check, Machine Check, Restart, and SPER/SPR2. Dispatcher entries cover DSP, SRB, and SSRB. External interrupt entries cover CALL, CLKC, EMS, EXT, and SS. SVC entries cover SVC, SVCE, SVCR
- For the changed records, wherever the 8-byte current PSW is present (field header such as PSW----- ADDRESS-), the output will contain the 8-byte address on the first line, with the two 4-byte parts separated by an underscore, and bytes 0-7 of the PSW will be underneath, on the second line. <<Note, this format is used at the suggestion of Level 2>>
- GTF records and formatting are changed (incompatibly): 8-byte PSW fields are extended to 16 to contain the 16-byte PSW

Usage and invocation (changed System Trace examples)

```
PR ASID WU-ADDR- IDENT  CD/D PSW----- ADDRESS-  UNIQUE-1 ...
                                               UNIQUE-4 ...
00 0022 006E1BF8  SVC      1 00000000_082C21B0  00000000 ...
                               07141000 80000000
00 0022 006E1BF8  SVCR     1 00000000_082C21B0  806FF0C0 ...
                               07141000 80000000
00 000A 024E8F00  SRB        00000000_011ADA8E  0000000A ...
                               07040000 80000000  006F9758 ...
00 000A 006F9758  DSP        00000000_08119448  00000000 ...
                               07041000 80000000
00 000A 006FA0B0  EXT   1005 00000000_061EA096  00001005 ...
                               07040000 80000000
```

Usage and invocation (changed GTF examples)

```
SVC..... 001      ASCB.... 00FDBF00 CPU..... 0001     JOBNAME. *MASTER*                    OLD-PSW. 07041000 80000001 00000000
  0960DA98
                    TCB..... 005ED1A0 MODN.... IEFENFWT R15..... 00000000
                    R0...... 00000001 R1...... 00FDE2D4 PLIST... 00FDE2D4

SVCR.... 001      ASCB.... 00FDBF00 CPU..... 0001     JOBN.... *MASTER*
                    DSP-PSW. 07041000 80000001 00000000 0960DA32
                    TCB..... 005ED1A0 MODN.... IEFENFWT R15..... 805ED118
                    R0...... 00000001 R1...... 00FDE2D4
```

```
EXT..... 1202     ASCB.... 00FDBF00 CPU..... 0000     JOBN.... *MASTER*
                    OLD-PSW. 07060000 00001202 00000000 00000000
                    TCB..... 00000000 PARM.... 7FFFFBAD SIG-CPU. 0002

DSP               ASCB.... 00FDBF00 CPU..... 0002     JOBN.... *MASTER*
                    DSP-PSW. 07060000 00000000 00000000 00000000
                    TCB..... 00000000 MODN.... WAITTCB  R15..... 805E4130
                    R0...... 00000001 R1...... F660168C

SRB               ASCB.... 00FB8280 CPU..... 0002     JOBN.... XCFAS
                    SRB-PSW. 07040000 80000000 00000000 013AB406
                    SRB..... 0924D814 PARM.... 8924D7E8
                    TYPE.... INITIAL DISPATCH OF SRB
```

Usage and invocation (changed diagnostics)

- The data formatted by
  SYSTRACE PERFDATA(SHOWTRC SIGCPU(time))
  will change to show 8-byte addresses when needed. If the address is below 2G, the existing line format will be used (the PSW area shows ffffffff aaaaaaaa where ffffffff is bytes 0-3 of the PSW, and aaaaaaaa is the address. If the address is above 2G, that line will show aaaaaaaa_aaaaaaaa (the 8-byte address) and a second line will be added that contains ffffffff gggggggg (bytes 0-3 then 4-7 of the PSW) aligned with the 8-byte address.
- IPCS LIST PSW will return / display a 16-byte PSW
- The SDUMP 4K Buffer (which can be displayed in IPCS using LIST 0 DOMAIN(SDUMPBUFFER) LENGTH(4096) will have the 16-byte PSW added at the end (bytes x'FEC'-x'FEF' will have the EBCDIC characters “P16 “ to identify 16-byte PSW, and bytes X'FF0'-'xFFF' will have that 16-byte PSW). For PER cases, the variable portion will add the 8-byte PER address to the (current) PER interrupt code

Interactions and dependencies

- Software dependencies
  - None
- Hardware dependencies
  - None
- Exploiters
  - None

Migration and coexistence considerations

- No unique considerations

Installation

- No unique considerations

Session summary

- RMODE 64 support is provided for a limited set of programs, with the system handling status saving and restoring to accommodate such programs

Appendix - References

- Publications
  - MVS Authorized Assembler Services Reference (various volumes)
    - for example, SA22-7609
  - MVS Diagnostic Tools and Service Aids (GA22-7589)
  - MVS Initialization and Tuning Reference (SA22-7592)
  - MVS IPCS User's Guide (SA22-7596)
  - MVS System Messages (various volumes)
    - for example, SA22-7634
  - MVS Data Areas