IBM System z9

IBM System z9 109

Processor, Memory and System Structure

zSTSU, August 2, 2005
Harv Emery
Washington Systems Center

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Agenda

- **IBM System z9™ 109 (z9-109) Introduction**
- **System Structure**
- **Model Configurations and Memory**
- **Processor Unit Specifics**
- **"On Demand"**
- **Cryptography and Security**

IBM System z9 109 (z9-109) Introduction

z9-109 New Functions and Features

- Five New Hardware Models
- Faster Uni Processor
- Up to 54 CPs
- Up to 512GB Memory
- Up to 60 LPARs
- CBU for IFL, ICF and zAAP
- Separate PU Pool Management
- Redundant I/O Interconnect
- Enhanced Driver Maintenance
- Enhanced Book Availability
- Wild Branch PD Assist
- 54 additional hardware Instructions

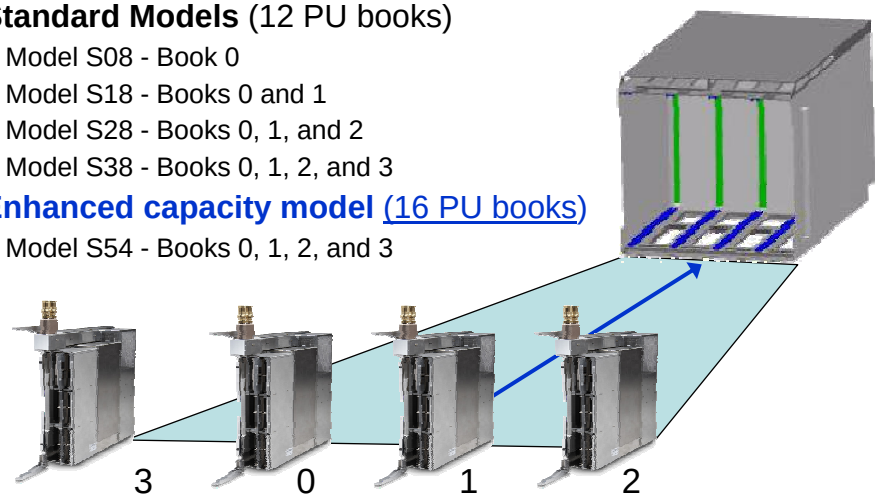
- Up to 16 2.7 GB STIs per book
- MIDAW facility
- Second Subchannel Set in each LCSS
- Subchannel set 0 increased to 63.75K Subchannels
- FICON Express2 supports 64 Open Exchanges
- Increased Number of FICON® Express2 features
- N_Port ID Virtualization
- IPv6 Support for HiperSockets™
- OSA-Express2 1000BASE-T
- OSA-Express2 OSN (OSA for NCP)
- Enhanced CPACF with AES, PRNG and SHA-256
- Configurable Crypto Express2

Preview*
Server Time Protocol

*This statement represents IBM's current intentions. IBM development plans are subject to change or withdrawal without further notice.

z9-109 Books and CEC Cage

- **Cage accepts one to four processor books**
- **Standard Models** (12 PU books)
  - Model S08 - Book 0
  - Model S18 - Books 0 and 1
  - Model S28 - Books 0, 1, and 2
  - Model S38 - Books 0, 1, 2, and 3
- **Enhanced capacity model** (16 PU books)
  - Model S54 - Books 0, 1, 2, and 3

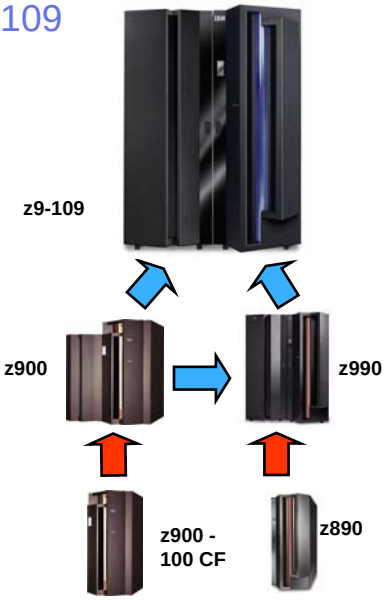


zSeries® upgrade paths to z9-109

- **To z9-109 from any model z990**
- **To z9-109 from any model z900 except CF Model 100**

- Upgrade to any z990 model from any model z900 except z900 CF model 100
- Upgrade to z990-A08 from z890-A04 170 (1-way), 250 (2-way), 330 (3-way), 430 (4-way) and larger only
- Upgrade to any z900 model from z900 CF model 100

Note: 2-step "upgrade" asset swap only



IBM System z9™ Key Dates

- **z9-109 Announce – July 26, 2005**
  - First Day Orders
  - Resource Link™ support available
  - SAPR Guide and SA Confirmation available
- **Availability dates**
  - z9-109 Models S08, S18, S28 and S38: September 16, 2005
  - Models S08, S18, S28, S38 CBU and On/Off CoD Activate: September 16, 2005
  - z990 upgrades to z9-109 Models S08, S18, S28 or S38: September 16, 2005
  - z900 upgrades to z9-109 Models S08, S18, S28 or S38: September 16, 2005
  - z9-109 Model S54: November 18, 2005
  - Model S54 CBU and On/Off CoD Activate: November 18, 2005
  - z990 upgrades to z9-109 Model S54: November 18, 2005
  - z900 upgrades to z9-109 Model S54: November 18, 2005
  - Models S08, S18, S28 and S38 MES feature upgrades: December 16, 2005
  - Model S54 MES feature upgrades: February 25, 2006
  - Model S08, S18, S28 or S38 upgrade to Model S54: February 25, 2006

z9-109 ITR Comparison

z9-109 CPs	z9-109 MCI*	z990 MCI*	ITR Ratio
1	701	301	1.35 ± ??
8	708	308	1.34 ± ??
18	718	318	1.34 ± ??
28	728	328	1.32 ± ??
38	738	332	1.51 ± ??

Ratios depend on workload and LPAR configuration!

Note: For MSU values, refer to:
http://www.ibm.com/servers/eserver/zseries/library/swpriceinfo/

* MCI = Model capacity Indicator refers to number of installed CPs. Reported by STSI instruction. MCI 700 means no CPs.

z9-109 ITR Comparison – Model S54

z9-109 CPs	z9-109 MCI*	z990 MCI*	ITR Ratio
1	701	301	1.35 ± ??
8	708	308	1.34 ± ??
18	718	318	1.34 ± ??
28	728	328	1.32 ± ??
38	738	332	1.51 ± ??
54	754	332	1.95 ± ??

Ratios depend on workload and LPAR configuration!

Note: For MSU values, refer to:
http://www.**ibm.com**/servers/eserver/zseries/library/swpriceinfo/

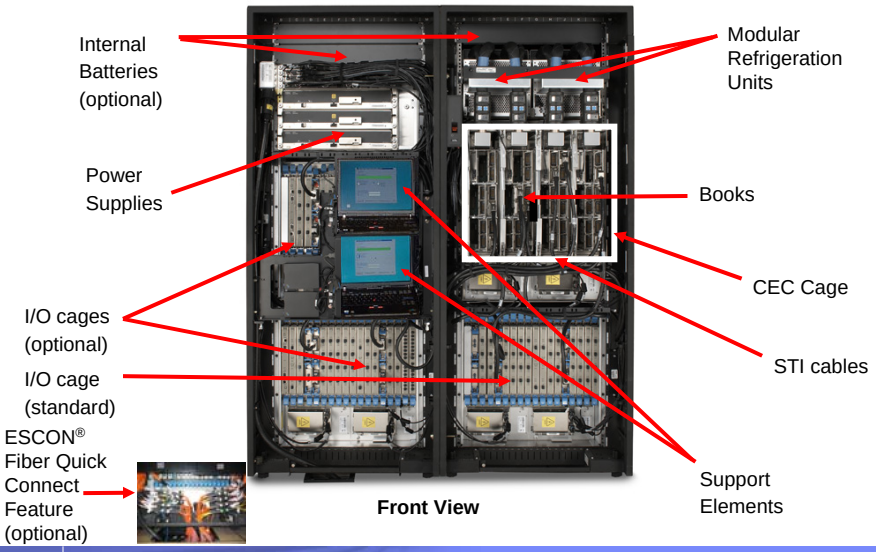
* MCI = Model capacity Indicator refers to number of installed CPs. Reported by STSI instruction. MCI 700 means no CPs.

z9-109 Capacity Planning in a nutshell

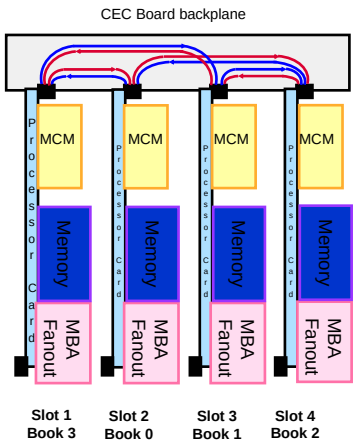
Don't use "one number" capacity comparisons!
Work with IBM technical support for capacity planning!

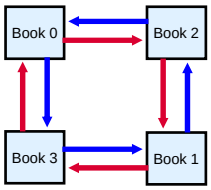
IBM System z9 109 System Structure

z9-109 – Under the covers (Model S38 or S54)



z9-109 Book Communication Ring Structure

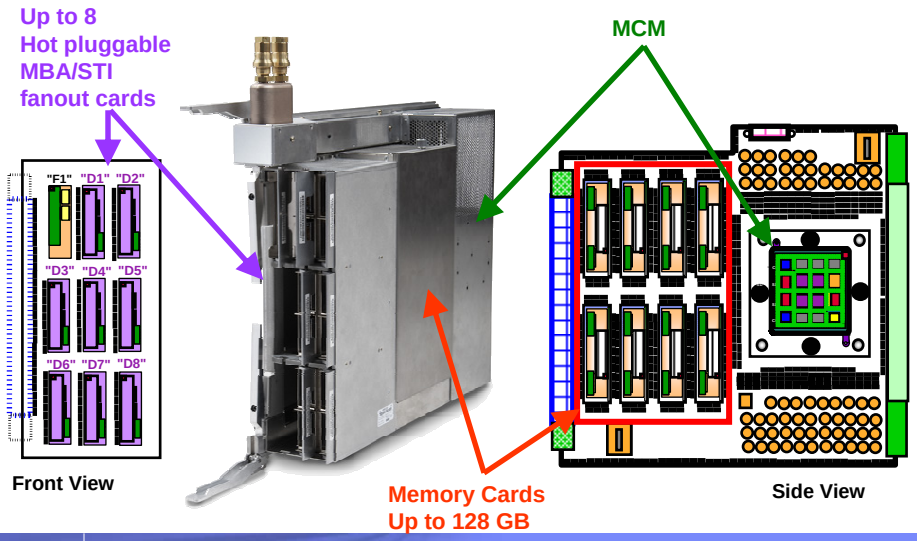




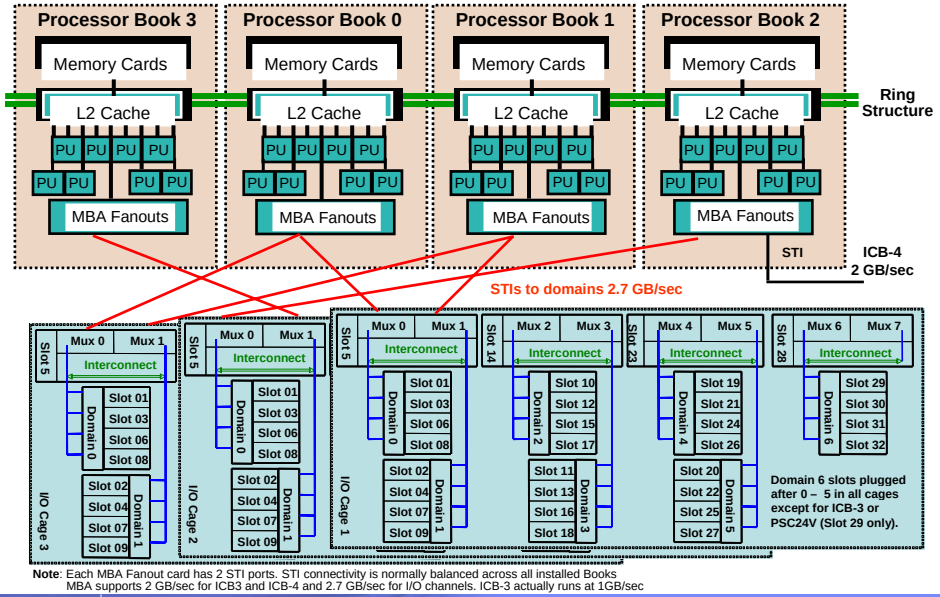
- The ring structure consists of two rings (one running clockwise, the other counterclockwise)
- In a two or three Book configuration, jumper Book(s) (installed in the CEC cage) complete the ring
  - Jumper Books are not needed for a single-Book configuration
- Designed to allow books to be inserted into or removed from the ring non-disruptively*
  - May allow **Concurrent Book Add** for model upgrade
  - May allow **Enhanced Book Availability** to remove and return a book for upgrade/repair or restart with a fenced book in the unlikely event of a book failure

* Customer pre-planning required, may require acquisition of additional hardware resources

z9-109 Processor Book Layout

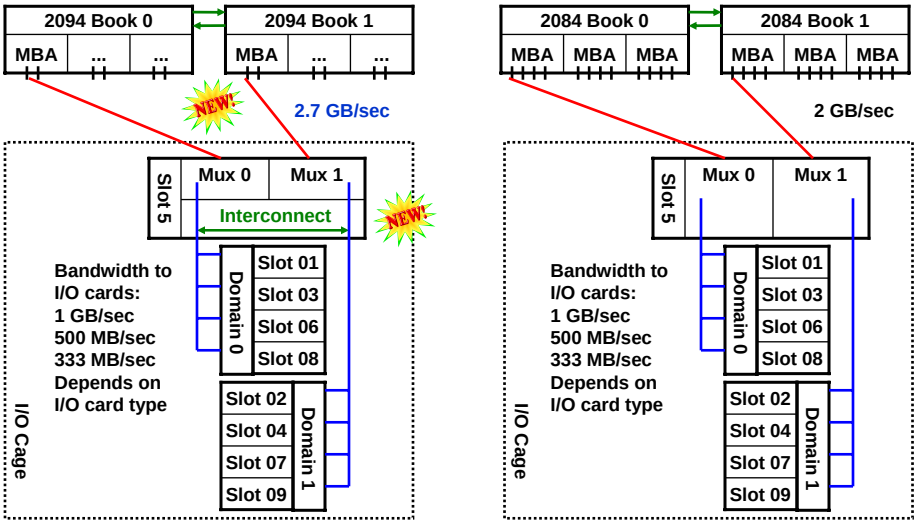


z9-109 Book, STI and I/O Cage Configuration



Note: Each MBA Fanout card has 2 STI ports. STI connectivity is normally balanced across all installed Books
MBA supports 2 GB/sec for ICB3 and ICB-4 and 2.7 GB/sec for I/O channels. ICB-3 actually runs at 1GB/sec

z9-109 Redundant I/O Interconnect compared to z990



IBM System z9 109 Model Configurations and Memory

z9-109 Model Configuration Overview

Model	S08	S18	S28	S38	S54
Books	1	2	3	4	4
Processor Units (PUs)	12	24	36	48	64
Spare PUs	2	2	2	2	2
Standard SAPs	2	4	6	8	8
Configurable PUs (Standard)	8	18	28	38	54
Configurable PUs (Enhanced Availability)	NA	8	18	28	40
GB Memory (Standard)	16 - 128	16 - 256	16 - 384	16 - 512	16 - 512
GB Memory (Flexible)	NA	32 - 128	32 - 256	32 - 384	32 - 384
Maximum Channels	960	1024	1024	1024	1024

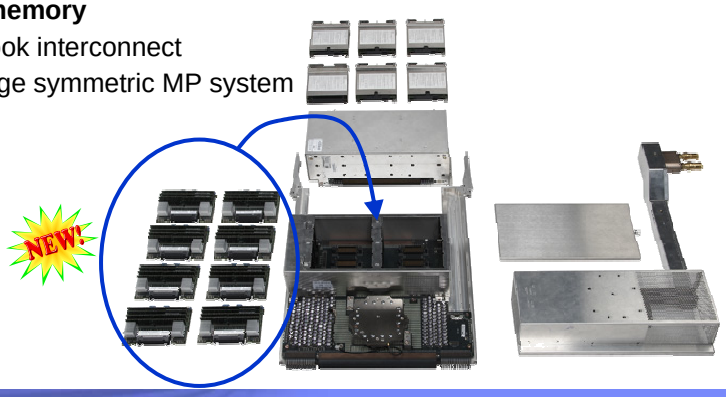
Notes: Books with 16 PUs are available only in the **Enhanced Capacity Model S54**
Shaded boxes represent improvements compared to z990.
"Enhanced Availability" and "Flexible" configurations best exploit **Enhanced Book Availability**, the capability to run with one book removed from the configuration.
Channel maximums vary by type. "Maximum Channels" assumes all ESCON.

z9-109 – Enhanced Availability Configurations

- **Design Concept: Configure enough physical memory and limit PUs configured so that all active purchased PUs and memory remain available with one book removed from the configuration with Enhanced Book Availability**
  - Book removed concurrently for physical upgrade or repair
  - Restart with a fenced book following the rare event of a book failure
- **How?**
  - **Select an S18, S28, S38, or S54 Model**
    - Configure no more than the following number of PUs
      - 8 active PUs on the S18
      - 18 active PUs on the S28
      - 28 active PUs on the S38
      - 40 active PUs on the S54
    - Requires no special feature codes for PU or model configuration.
  - **Select Flexible Memory configuration features**

System z9 Memory Cards

- **Memory cards 4, 8 or 16 GB**
- **Configurations of 4 or 8 cards per book**
- **Physical memory may be larger than purchased memory**
- **Purchased memory enabled by LIC-CC**
- **Unified memory**
  - Ring book interconnect
  - One large symmetric MP system



z9-109 Memory Configurations

- **Standard – Lower cost**: split memory as equally as possible among books, use smallest possible cards for purchased memory
- **Flexible – Supports Enhanced Book Availability**: split memory as equally as possible among books, use large enough cards to **ensure purchased memory remains available if any one book is removed**
- **Memory Purchase Increment – 16 GB** standard or flexible

Purchased	Model	S08	S18	S28	S38, S54
Standard Configuration	Minimum	16 GB	16 GB	16 GB	16 GB
	Maximum	128 GB	256 GB	384 GB	512 GB
Flexible Configuration	Minimum	NA	32 GB	32 GB	32 GB
	Maximum	NA	128 GB	256 GB	384 GB

Purchased memory: Model S08	16 GB	32 GB	48GB	64 GB	80 GB	96 GB	112 GB	128 GB
Memory Card Configuration	4 x 4	4 x 8	8 x 8	8 x 8	8 x 16	8 x 16	8 x 16	8 x 16

z9-109 Concurrent Memory Upgrades

- **LIC enable additional memory to the physical limit of the installed cards and memory configuration**
  - Designed to be possible and concurrent in many but not all configurations
- **Concurrent Book Add with additional memory**
  - Designed to be possible except for Models S38 and S54
- **Exploit Enhanced Book Availability to change memory card configuration in existing books**
  - Not possible on Model S08
  - Exploits capability for concurrent book remove, upgrade and return
  - Designed to be possible with flexible memory and PU configurations
  - May be possible with standard memory and PU configurations depending on LPAR configuration with appropriate planning and operator action

Note: Concurrent memory upgrades above are designed not to require CEC activation (POR). z/OS® with "reserved memory" configured in the LPAR profile can add memory to a running partition. Otherwise adding memory to a partition requires deactivation, profile change and activation of the partition, which is designed to be disruptive to that partition only.

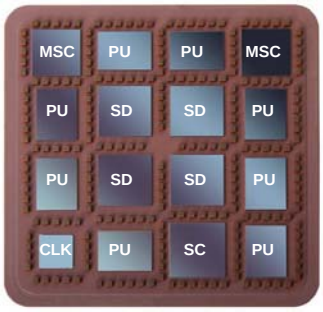
z9-109 Model and I/O MES Upgrades

- **Model upgrades**
  - **Designed to be concurrent to Model S18, S28, and S38** from any lower z9-109 model by exploiting **Concurrent Book Add**
  - **Disruptive upgrade to Model S54**
    - All four books must be replaced with 16 PU books
- **I/O cage add**
  - **Disruptive**
  - Avoid by using **"Plan Ahead"** on initial order to configure additional cages for later requirements
- **I/O and crypto feature adds**
  - **Designed to be concurrent**
    - I/O add requires z/OS or z/VM® exploitation of dynamic I/O to avoid disruption.
    - Concurrent exploitation of added cryptographic features requires "candidate" predefinition in the LPAR image profile.

IBM System z9 109 PU Specifics

z9-109 multi-chip module (MCM)

- **Advanced 95mm x 95mm MCM**
  - 104 Glass Ceramic layers
  - 16 chip sites, 217 capacitors
  - 0.476 km of internal wire

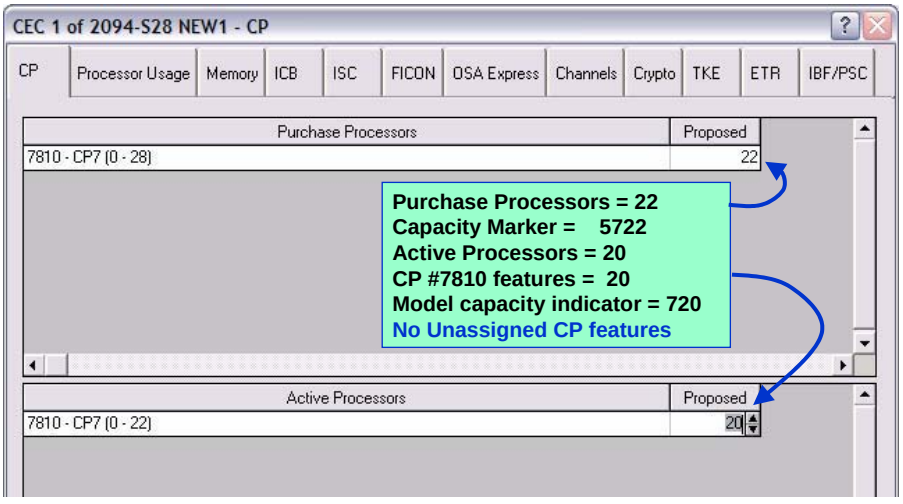


- **CMOS 10K chip Technology**
  - PU, SC, SD and MSC chips
  - Copper interconnections, 10 copper layers
  - 8 PU chips/MCM
    - 15.78 mm x 11.84 mm
    - 121 million transistors/chip
    - L1 cache/PU
      - 256 KB I-cache
      - 256 KB D-cache
    - 0.58 ns Cycle Time
  - 4 System Data (SD) cache chips/MCM
    - 15.66 mm x 15.40mm
    - 660 million transistors/chip
    - L2 cache per Book: 40 MB
  - One Storage Control (SC) chip
    - 16.41mm x 16.41mm
    - 162 million transistors
    - L2 cache crosspoint switch
    - L2 access rings to/from other MCMs
  - Two Memory Storage Control (MSC) chips
    - 14.31 mm x 14.31 mm
    - 24 million transistors/chip
    - Memory cards (L3) interface to L2
    - L2 access to/from MBAs (off MCM)
- **One Clock (CLK) chip - CMOS 8S**
  - Clock and ETR Receiver

z9-109 PU Types and Characterization Features

- **Central Processor (CP) – Feature 7810**
  - Provides processing capacity for z/Architecture™ and ESA/390 instruction sets
  - Can support **ANY** operating system, z/VM guest, or Coupling Facility
  - z9-109 has **Capacity Marker** features NOT **Unassigned CP** features
- **IBM System z9 Application Assist Processor (zAAP)** - **Feature 7814**
  - Under z/OS only and only the Java Virtual Machine (JVM)
  - Requires z/OS 1.6 or later
- **Integrated Facility for Linux™ (IFL) and Unassigned IFL – Feature 7811 and 7831**
  - Provides additional processing capacity exclusively for Linux on System z9 workloads
  - Runs Linux on System z9 or z/VM Version 4 or Version 5 for Linux guests
- **Internal Coupling Facility (ICF) – Feature 7812**
  - Provides additional processing capacity exclusively for the execution of Coupling Facility Control Code (CFCC) in a CF LPAR
- **System Assist Processors (SAPs)**
  - Standard and Optional SAPs (**Feature 7813**) do I/O processing in the channel subsystem
  - Two standard SAPs are provided per System z9 book
  - Optional SAPs are typically NOT needed except, sometimes for TPF
- **Spare PUs – Not orderable**
  - Two standard spares per z9-109 and all available (unassigned) PUs
  - Support "Transparent Sparing" for other PU types

eConfig Selection of Unassigned CP Capacity



z9-109 Concurrent PU Feature Conversions

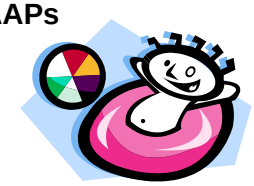
- **Flexibility to meet changing business environments**
- **Decreasing the number of CP or IFL features is designed to be concurrent.**
  - Can be ordered by MES or by CIU. (No RPQ needed.)
  - Like z990 and z890, z9-109 unassigned IFL capacity is recorded by **Unassigned IFL** features
  - Unlike z990, z9-109 does NOT have **Unassigned CP** features
  - Like z890, z9-109 unassigned CP capacity is recorded by a **Capacity Marker** feature
- **PU type conversions shown below with Yes are designed to be concurrent**
  - Can be ordered by MES or CIU (No RPQ needed)
  - **Example:** From z9-109 S08 with eight CPs, convert one CP to an IFL
  - **Note:** CP feature conversions also change (increase or decrease) the **Capacity Marker** feature

From \ To	CP	IFL	Unassigned IFL	ICF
CP	x	**Yes**	No	**Yes**
IFL	**Yes**	x	**Yes**	**Yes**
Unassigned IFL	No	**Yes**	x	No
ICF	**Yes**	**Yes**	No	x

Note: Customer planning and operator action are required to exploit.
Disruptive if ALL current PUs are converted to different types
May require individual LPAR disruption if dedicated PUs are converted.

PR/SM™ Hypervisor™ PU Dispatching "Pools"

- **PU Pool – Physical PUs to dispatch to online logical PUs**
- **z9-109 with 10 CPs, 1 ICF, 2 IFLs, and 3 zAAPs**
  - CP pool contains 10 CP engines
  - **ICF pool** contains 1 ICF
  - **IFL pool** contains 2 IFLs
  - **zAAP pool** contains 3 zAAPs
  - **z/OS LPAR can have different initial CP and zAAP weights**
- z990 with 10 CPs, 1 ICF, 2 IFLs, and 3 zAAPs
  - CP pool contains 10 CP engines
  - **Specialty pool** contains 6 engines – ICFs, IFLs, zAAPs
  - z/OS LPAR zAAP weight is set equal to the initial CP weight



PR/SM Hypervisor PU Pool Rules

- **Logical PUs dispatched from supporting pool only**
  - Logical CPs from CP pool only, for example
- **Pool "width"**
  - Width equals the number of physical PUs in the pool
  - Limits an LPAR's maximum number of shared logical PUs brought online
- **PUs placed in pools by**
  - Activate (POR)
  - Concurrent Upgrade – On/Off CoD, CBU, CIU, CUoD MES
  - Dedicated LPAR **deactivation**
  - Dedicated LPAR configure logical PU **OFF**
- **PUs removed from pools by**
  - Concurrent Downgrade - On/Off CoD, CBU, PU Conversion MES
  - Dedicated LPAR activation ("width" permitting)
  - Dedicated LPAR configure logical PU ON ("width" permitting)

z990 with 10 CPs, 1 ICF, 2 IFLs, and 3 zAAPs

- **LPAR Share = Pool PUs x (LPAR Pool Weight)/(Total Pool Weight)**
  - Can't exceed number of Online Logical Processors dispatched from the pool
  - z/OS LPAR – "Initial" weight applies to CPs and to zAAPs
- **Pool PUs (Physical) – CP =10, Specialty = 6 (ICF, IFL, zAAP)**
- **Total Pool Weights – CP = 1000, Specialty = 1500**

LPAR Name	LPAR Weight	Shared Logical PUs ON				PU Share	
		CP	zAAP	IFL	ICF	CP	Specialty
ZOS1	250c / 250z	10	2	NA	NA	2.5	1
ZOS2	750c / 750z	10	3	NA	NA	7.5	3
CF1	50	0	NA	NA	1	0	.2
CF2	50	0	NA	NA	1	0	.2
ZVM1	100	0	NA	2	NA	0	.4
LINUX1	300	0	NA	2	NA	0	1.2
Pool Weight >		1000	1500				
Total PUs (Physical) >						10	6

CP

Specialty

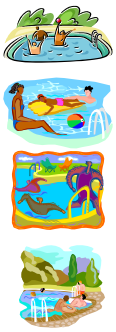
- **Interaction among specialty engine weights impact share**

z9-109 with 10 CPs, 1 ICF, 2 IFLs, and 3 zAAPs

NEW!

- **LPAR Share = Pool PUs x (LPAR Pool Weight)/(Total Pool Weight)**
  - Can't exceed number of Online Logical Processors dispatched from the pool
  - z/OS LPAR – Separate "Initial" weights for CPs and zAAPs
- **Pool PUs (Physical) – CP =10, zAAP = 3, IFL = 2, ICF =1**
- **Total Pool Weights – CP = 1000, zAAP = 200, IFL= 400, ICF= 100**

LPAR Name	LPAR Weight	Shared Logical PUs On				PU Share			
		CP	zAAP	IFL	ICF	CP	zAAP	IFL	ICF
ZOS1	250c / 100z	10	2	NA	NA	2.5	1.5	NA	NA
ZOS2	750c / 100z	10	3	NA	NA	7.5	1.5	NA	NA
CF1	50 - ICF	0	NA	NA	1	0	NA	NA	.5
CF2	50 - ICF	0	NA	NA	1	0	NA	NA	.5
ZVM1	100 - IFL	0	NA	2	NA	0	NA	.5	NA
LINUX1	300 - IFL	0	NA	2	NA	0	NA	1.5	NA
Pool Weight >		1000	200	400	100				
Total PUs (Physical) >						10	3	2	1



- **No interaction among specialty engine weights**

IBM System z9 109 "On Demand"

ON DEMAND BUSINESS™

ENABLING BUSINESS. A THROUGH Z.

z9-109 Capacity Upgrade on Demand

- **CUoD is designed to support addition of processors and/or memory or concurrent type conversion among CPs, IFLs, and ICFs without disruption to workloads running on the machine - no power-off, power-on. Includes**:
  - Addition of CP, ICF, IFL and zAAP includes turning on (assigning) "Unassigned" IFL features
  - LIC enabling additional 16 GB memory increments
  - Concurrent z9-109 model upgrade (Concurrent Book Add)
  - Concurrent z9-109 memory upgrade exploiting **Enhanced Book Availability**
- **CUoD capabilities can be exploited by IBM ordered/installed MES upgrade**
- **Some CUoD capabilities can be exploited by customer controlled upgrades:**
  - **Capacity Backup (CBU)** – temporary emergency upgrades
  - **Customer Initiated Upgrade (CIU)** – permanent upgrades
  - **On/Off Capacity on Demand (On/Off CoD)** – temporary on-demand upgrades
- Notes:
  1. CUoD is built on a base of concurrent "hot-plug" maintenance
  2. I/O feature adds and removes are also nondisruptive but not really "CUoD"
  3. Customer planning and operator action are required to take full advantage of CUoD. To avoid a planned outage, it may be necessary to predefine LPAR profiles with "reserved" resource specified. It may also be necessary to use z/OS or z/VM dynamic I/O capabilities. In some cases, disruption of certain LPARs is required following a concurrent hardware change.

Concurrent Upgrade - Customer Controlled

- **CBU – Capacity Backup - Temporary emergency capacity upgrade**
  - Non-disruptive temporary addition of **CPs, zAAPs, IFLs and ICFs** in an emergency situation
  - CBU contract required to order CBU features and CBU LIC CC
  - Customer (or IBM) activates upgrade for test or temporary emergency
  - Non-disruptive downgrade required after test or recovery completed
- **CIU – Customer Initiated Upgrade - Express - Permanent upgrade**
  - Customer capability to order and install permanent upgrade
  - CUoD capabilities NOT included:
    - Upgrades requiring parts (e.g. I/O feature card add)
    - Channel upgrades by LIC enable of existing ports
  - CIU feature - ordered to initiate contract and administrative setup
  - Customer orders and installs upgrade via Resource Link™ and IBM RSF
- **On/Off Capacity on Demand - Temporary upgrade**
  - Nondisruptive temporary addition of CPs, zAAPs, IFLs, and ICFs in any situation
    - Upgrades requiring parts (e.g. I/O feature card add) not supported
  - "Right to use" feature - ordered to initiate contract and administrative setup
  - Customer orders and installs upgrade via Resource Link and IBM RSF
  - Nondisruptive removal when capacity is no longer wanted

System z9 CBU Features

- **CBU features are ordered using eConfig**
  - Features are: CBU CP, CBU zAAP, CBU IFL and CBU ICF
  - Limitations:
    - **Active PUs plus CBU PUs cannot exceed configurable PUs**
      - Unassigned CP capacity and Unassigned IFL features do not limit CBU PUs
      - MES addition of active PU features to the base may require removal of CBU PU features
    - **After activation, the number of zAAPs cannot exceed the "number of CPs"**
      Note: **"Number of CPs"** includes base CPs, CBU CPs and unassigned CP capacity recorded by the system's Capacity Marker feature.
- **MES conversion among CBU PU types is concurrent**
  - Order using eConfig

From \ To	CBU CP	CBU zAAP	CBU IFL	CBU ICF
CBU CP	X	Yes	Yes	Yes
CBU zAAP	Yes	X	Yes	Yes
CBU IFL	Yes	Yes	X	Yes
CBU ICF	Yes	Yes	Yes	X

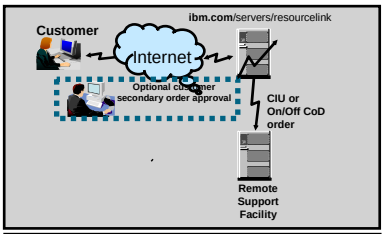
System z9 On/Off Capacity on Demand

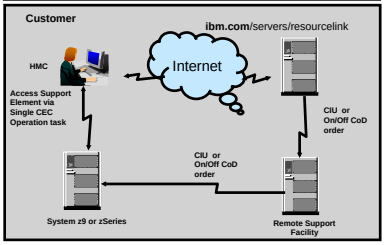
- **Prerequisite for use:**
  - **Customer Initiated Upgrade** (FC #9898) and **On/Off CoD** (FC #9896) "right-to-use feature"
  - Signed CIU contract with specific Ts & Cs governing temporary capacity
- **Order temporary capacity – Resource Link**
  - **Can at most add capacity equal to active permanent capacity of the same type**
    For example – Go from 2 CPs to 4, 1 IFL to 2, or do both in the same order
    (Note: CIU upgrades and CBU do NOT have the this restriction)
  - PUs that have never been characterized can be activated as CPs, zAAPs, IFLs or ICFs
  - Unassigned IFLs can be activated only as IFLs – **Price advantage on z9-109**
  - Unassigned CP capacity can be activated only as CPs – **Price advantage on z9-109**

- **Order is manufactured: A LIC record is established and staged to RETAIN**
  - Multiple orders to meet different customer requirements can be staged
  - Orders remain on RETAIN for an extended period until:
    - Downloaded and activated (Initiates billing except for the 24-hour test)
    - Customer cancels order
    - Machine is no longer under warranty or IBM Maintenance Service Agreement
    - Change to Permanent PU and/or memory configurations invalidates order
  - A record, once activated, has no expiration date
- **On/Off CoD activation and CBU can coexist**
  - Must deactivate one function to activate the other one.
  - CBU PUs configured do not reduce On/Off CoD temporary capacity orderable

System z9 and zSeries CIU and On/Off CoD

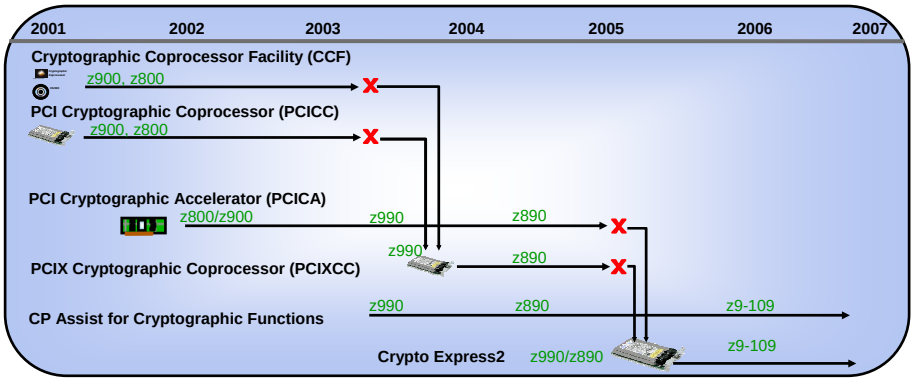
- **Order CIU and CoD "right to use" features**
  - Qualification, contracting, and pricing
  - Resource Link ID Authorization
- **Customer CIU or On/Off CoD order or On/Off CoD test order (up to 24 hours)**
  - Configure upgrade on Resource Link
  - Secondary Approval (Option)
  - Resource Link communicates with Remote Support Facility (RSF) to stage order and prepare download
  - Customer notified order ready
- **Access Support Element (SE) using Hardware Management Console (HMC)**
  - "Perform Model Upgrade"
  - Code obtained using RSF and installed on target machine





IBM System z9 Cryptography and Security

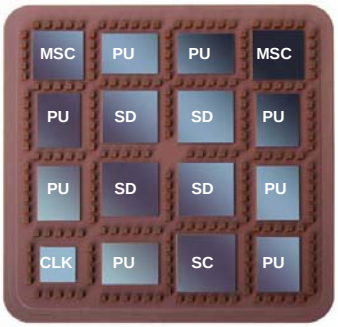
System z9 and zSeries Crypto Roadmap



- **z9-109, z990, and z890 include NO standard cryptographic coprocessor function**
- **CP Assist for Cryptographic Function (message security assist) Optional Feature #3863**
  - Provides instructions and access to cryptographic functions in every PU
  - Supports limited clear key processing **running on the PU** – Compute intensive!
  - **NOT equivalent to CCF on older machines in function or offload capability**
- **Migration to z9-109, z990 or z890 when CCF, PCICC, PCIXCC or PCICA is in use on an older machine almost always requires Crypto Express2.**

z9-109 CP Assist for Cryptographic Function (CPACF)

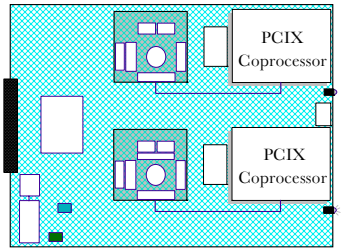
- **High performance cryptographic instructions in every PU but NOT an offload engine**
  - Clear key cryptographic processing, hashing and random number generation
  - Pseudo-optimized for low-latency SSL transactions
- **Five capabilities, three System z9 exclusive:**
  - **Advanced Encryption Standard (AES)**
    - **128 bit keys**
  - **Secure Hashing – 256 (SHA-256)**
  - **Pseudo-random Number Generation (PRNG)**
  - Data Encryption Standard (DES) and Triple DES
    - Up to 2**64 byte message, interruptible execution
  - Secure Hashing (SHA-1)
- **CPACF Enabler Feature FC #3863**
  - No additional charge export control feature
  - Required to enable AES, DES/TES, and PRNG (SHA-1 and SHA-256 are always enabled)
  - Required to order Crypto Express2
  - **Recommended on EVERY system if allowed by law**



System z9 Crypto Express2 Feature

- **Dual Integrated Cryptographic Coprocessors**
  - Individually configurable as:
    - **Secure Coprocessor** (default), designed to provide both "Secure key" and "Public key" function
    - **Accelerator**, designed to provide only "Public key" function with enhanced performance
  - Current applications expected to run without change
- **Secure Coprocessor mode is fully programmable and supports User Defined Extensions (UDX)**
- **Scalable (no CP affinity) –**
  - Supported Crypto Express2 configurations: 0, 2, 3, 4, 5, 6, 7, or 8 features (but NOT 1 feature)
  - Plugs into an I/O card slot (no external cables)
  - Up to 8 Crypto Express2 features can plug into a single I/O cage
- **Designed for FIPS 140-2 Level 4 Certification**
- **Trusted Key Entry (TKE) support (optional)**
  - If TKE configured, TKE 5 is required on z9-109
  - Updated user interface compared to TKE 4.x
  - Secure operational and master key loading
  - Smart Card Reader support

NEW!



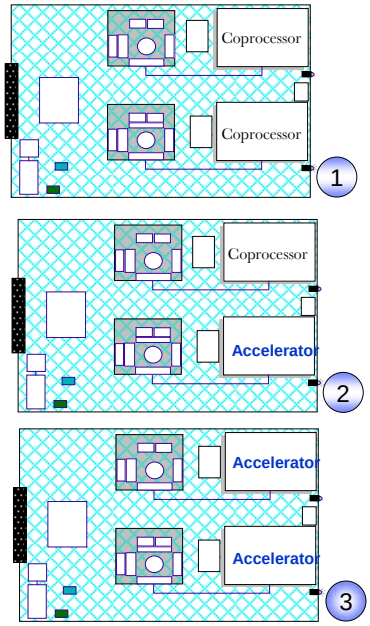
NEW!

z9-109 Crypto Express2 Configuration

- **Secure Coprocessor** (default)
  - Designed to provide both Secure key" and "Public key" function with performance equivalent to Crypto Express2 on z990
  - Designed to provide "Secure key" function with improved performance compared to PCIXCC on z990 (requires multitasking)
  - Designed to provide "Public key" function with performance equivalent to PCICA on z990
  - No configuration action required

NEW!

- **Accelerator**
  - Designed to provide only "Public key" function with enhanced performance compared to the Secure Coprocessor configuration
  - **Must be configured using the HMC**



System z9 and zSeries Cryptographic Technology

- Continues to provide flexible Secure Sockets Layer (SSL) acceleration
- Continues to provide competitive symmetric performance in a security-rich environment
- Provides integration of Crypto features via ICSF
- Focuses on required certifications and open standards
- Continues to improve performance
  - Each Crypto Express2 feature on a System z9, with both adapters configured as accelerators is designed to provide up to 6000* SSL handshakes per second

z900/z800 – Dec. 2000/ May 2002
2 SCMs on CEC Board -
CMOS7s+ PCICC/PCICA (10/01)

G6 – June 1999
2 Chips on Processor
MCM - CMOS5x +
PCICC (6/99)

G5 – Sept. 1998
2 Chips on Processor
MCM - CMOS5x +
PCICC (6/99)

G4 – Sept. 1997
SCMs on Planar
Board - CMOS5x

G3 – June, 1997
SCMs on Planar
Board - CMOS5x

z9-109 – Planned for Sept, 2005
Crypto Express2

z990/z890 – January 2005
Crypto Express2

z890 – May 2004
PCIXCC/PCICA

z990 - September 2003
PCIXCC

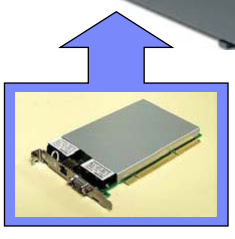
z990 - June 2003
CPACF/PCICA

z900/z800 – Dec. 2000/ May 2002
2 SCMs on CEC Board -
CMOS7s+ PCICC/PCICA (10/01)

*These measurements are examples of the maximum transactions/second achieved in a lab environment with no other processing occurring and do not represent actual field measurements. Details available upon request.

System z9 Trusted Key Entry (TKE) Workstation 5.0

- **Optional TKE Workstation:**
  - **The only TKE feature that supports z9-109**
  - Orderable on z9-109, z990, z890, z900 and z800
  - TKE 5.0 LIC: FC 0855
    - **Requires TKE 5.0 hardware**
  - TKE 5.0 hardware: FC 0859
    - **Requires TKE 5.0 LIC**
    - xSeries-based system unit, keyboard, flat panel, mouse
    - PCI-X Crypto Coprocessor
    - **Ethernet connectivity only**
  - Optional Smart Card Reader: FC 0887
  - Optional Additional Smart Cards: FC 0888
- **TKE 5.0 Hardware and LIC support to enter secure cryptographic keys for:**
  - z9-109: Crypto Express2
  - z990 and z890: PCIXCC and Crypto Express2
  - z900 and z800: CCF and PCICC



PCI-X Crypto Coprocessor

System z9 Security Certifications

- **Cryptographic Security Certification**
  - Crypto Express2 – Designed to meet FIPS 140-2 Level 4
  - Smart Cards – Certified to meet FIPS 140-2 Level 2
- **Common Criteria (ISO/IEC 15408) Evaluation Assurance Levels Reference: http://niap.nist.gov/cc-scheme/**
  - **z/OS 1.6 with RACF®** – Certified for Controlled Access Protection Profile (CAPP) EAL3+ and Labeled Security Protection Profile (LSPP) EAL3+
  - **SUSE LINUX SLES 8** – Certified for Controlled Access Protection Profile (CAPP) EAL3+
  - **z/VM V5.1 with RACF for z/VM** – IBM has applied for Controlled Access Protection Profile (CAPP) EAL3+ and the Labeled Security Protection Profile (LSPP) EAL3+
  - **SOD**: IBM intends to submit for evaluation z/VM V5.2 with the RACF® for z/VM for Controlled Access Protection Profile (CAPP) and the Labeled Security Protection Profile (LSPP) at EAL4
  - **z9-109 PR/SM –** Not certified (Probable future submission for EAL5)

zEnd