

## z/OS CPENABLE Settings IBM 9672 / zSeries Processor

**This Hints & Tips document replaces Flash 9634A**

### Recommended CPENABLE Setting

<b>Processor Family</b>	<b>Basic Mode</b>	<b>LPAR Dedicated</b>	<b>LPAR Shared</b>
zSeries 800/900 (2066/2064)	10, 30	10, 30	0, 0
9672 G5, G6	10, 30	10, 30	0, 0
9672 G1, G2, G3, G4	10, 30	10, 30	10, 30
MP3000 (1)	10, 30	10, 30	0, 0
MP2000 (2), ASP3000(3)	10, 30	10, 30	10, 30
ES/3090, ES9021	10, 30	10, 30	0, 0

(1) Model Type = 7060

(2) Model Type = 200

(3) Model Type = 3000

The use of CPENABLE to control the number of processors enabled to handle I/O processing involves a trade-off between response time and Internal Throughput Rate (ITR) efficiency. Measurements in a controlled environment, on an IBM 9672 n-way have shown ITR performance, in some situations, is degraded from 0% to 10% because of I/O interrupt handling effects. The additional CPU utilization is incurred when more than one processor is handling I/O interrupts at the same time.

SRM periodically monitors I/O interruptions to determine if a change should be made to the number of processors that are enabled. By comparing this value to threshold values, SRM determines if another processor should be enabled or if an enabled processor should be disabled for I/O interruptions. If the SRM computed value exceeds the upper threshold, I/O interruptions are being delayed, and another processor (if available) will be enabled for I/O interruptions. If the value is less than the lower threshold (and more than one processor is enabled), a processor will be disabled for I/O interruptions. The installation can change the threshold values using the CPENABLE parameter in the IEAOPTxx parmlib member.

A processor entering a wait state is always enabled for I/O interruptions, regardless of the specification of the CPENABLE keyword. An installation can use the CPENABLE keyword to specify low and high thresholds. For logical partitions using dedicated processors, IBM recommends a CPENABLE=(10,30) setting to minimize the number of CPs handling I/O interrupts on an logical CP.

Please refer to the table for recommended settings.