Processor Capacity Planning:

LSPR Workload Sensitivities

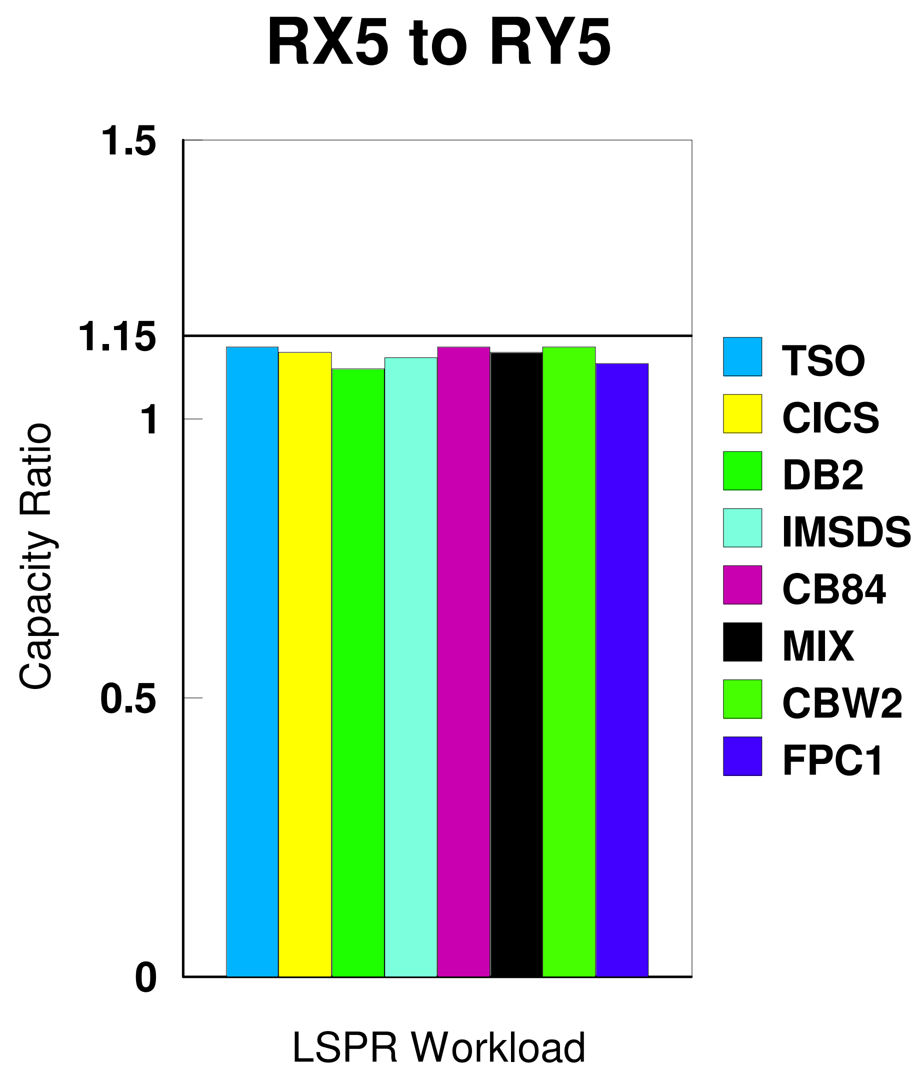
Processor Performance: Most Influential Factors

- Processor Design
  - Cycle time
  - Memory subsystem
    - high speed buffer (HSB)
    - latency
    - bandwidth
  - Logic
    - hardware vs. millicode
    - execution order
    - branch prediction
    - special features
  - Number of engines

- Workload Characteristics
  - Reference pattern
    - transaction size
    - I/O rate
    - multiprogramming level
  - Code
    - instruction mix
    - instruction sequence
    - branch characteristics
  - Common tasks/functions
  - LPAR Configuration

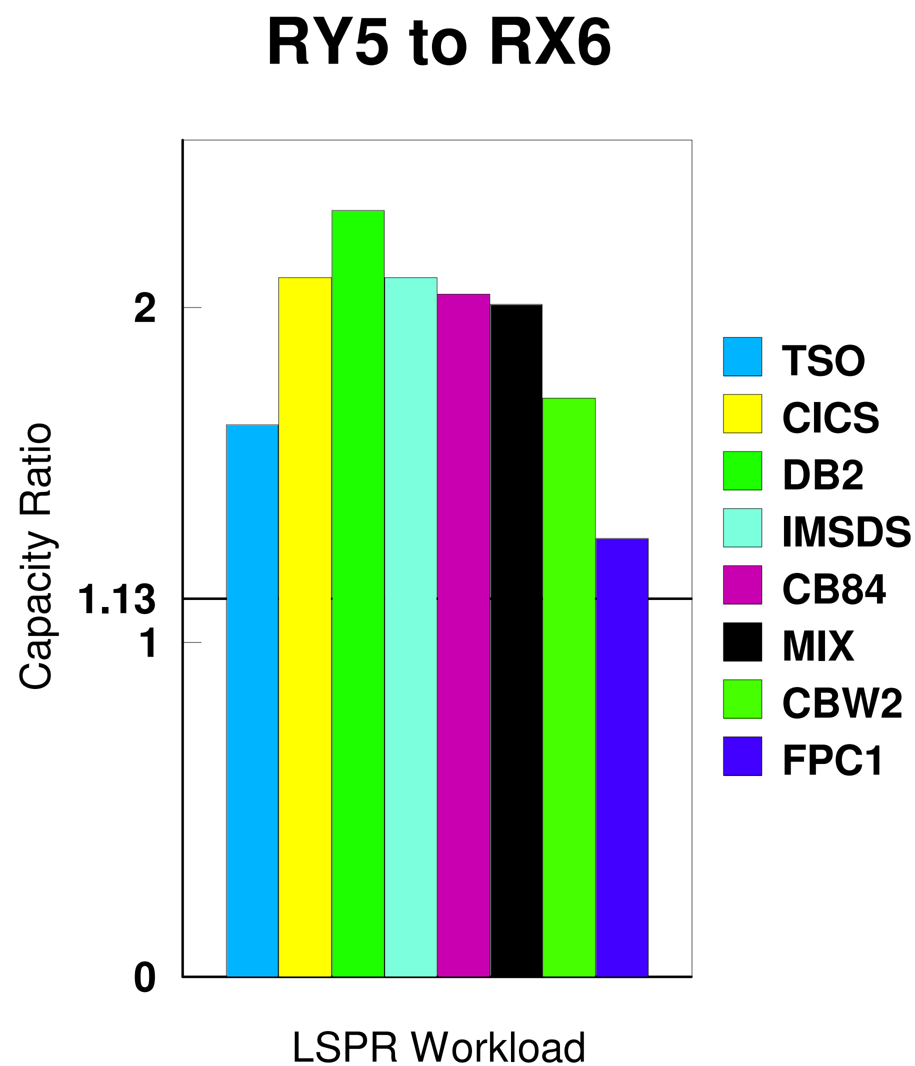
Processor Performance Example: Cycle Time Change

- RX5
  - Cycle time: 3.1 ns
  - Memory subsystem: same
  - Logic: same
  - Number of engines: same
- RY5
  - Cycle time: 2.7 ns
  - Memory subsystem: same
  - Logic: same
  - Number of engines: same



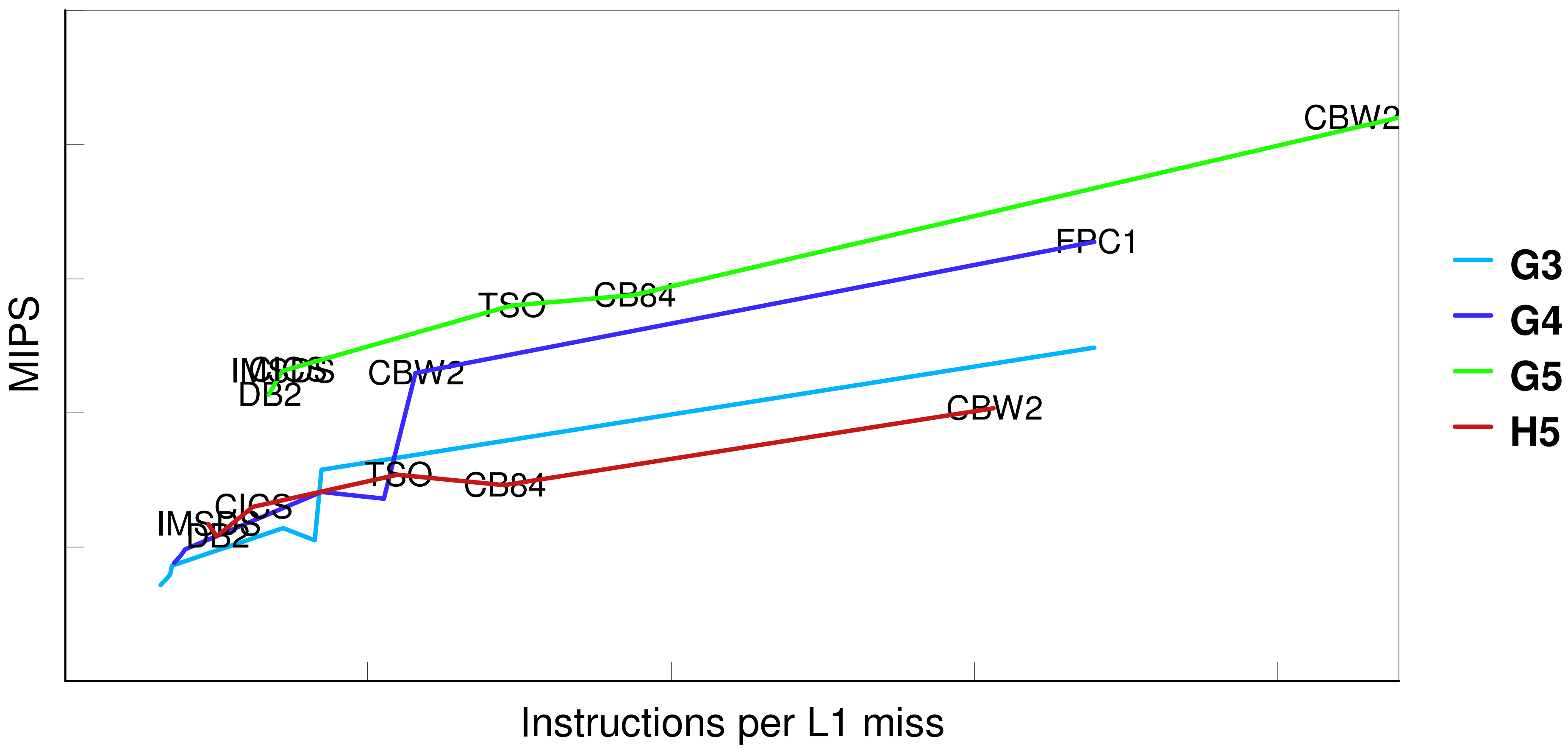
Processor Performance Example: Memory Subsystem Change

- RY5
  - Cycle time: 2.7 ns
  - L1: 64k
  - L2: 768k / 3CPs non-shared
  - L3: cross-point switch design
- RX6
  - Cycle time: 2.4 ns
  - L1: 256k
  - L2: 4mb / side non-shared
  - L3: storage controller design
  - Logic improvements
    - more hardware
    - branch history table



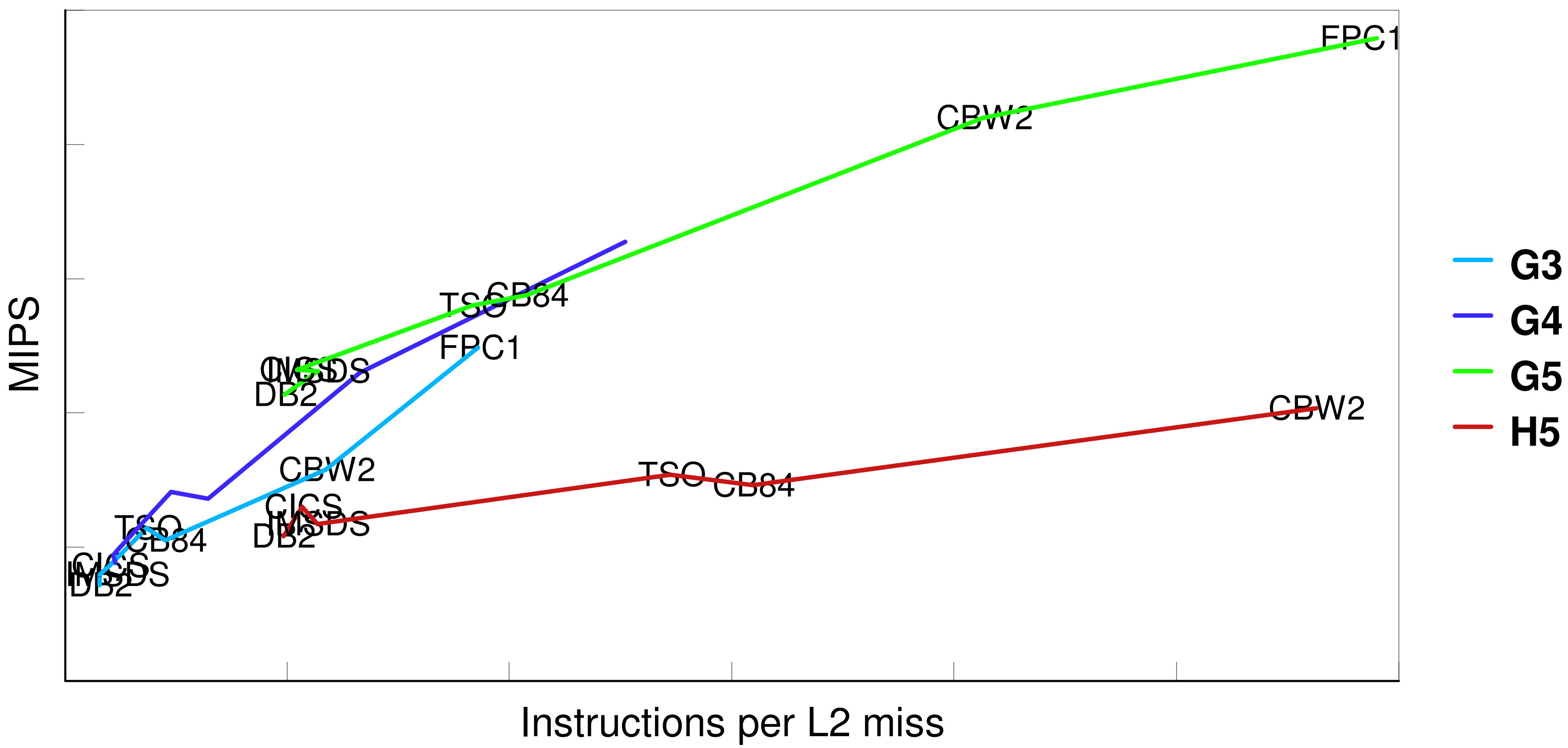
Workload<->Memory Subsystem Effects

MIPS versus i/L1 miss by LSPR workload
10way Processors



Workload<->Memory Subsystem Effects

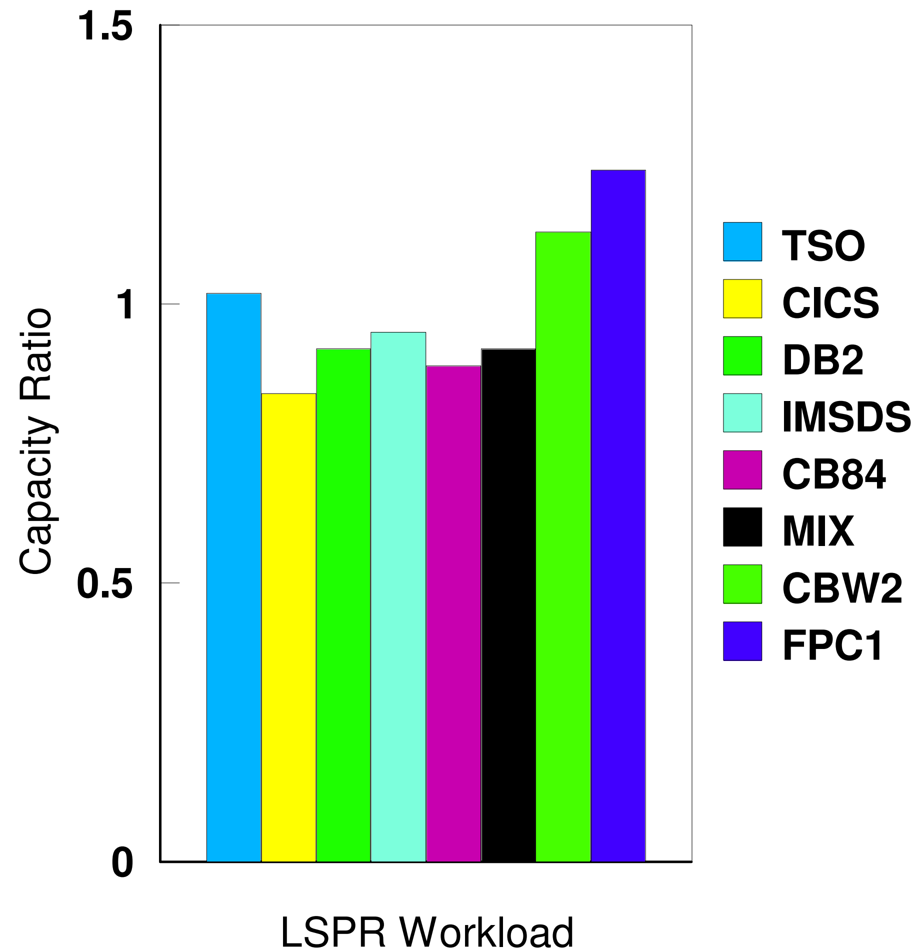
MIPS versus i/L2 miss by LSPR workload
10way Processors



Processor Performance Example: Logic Change

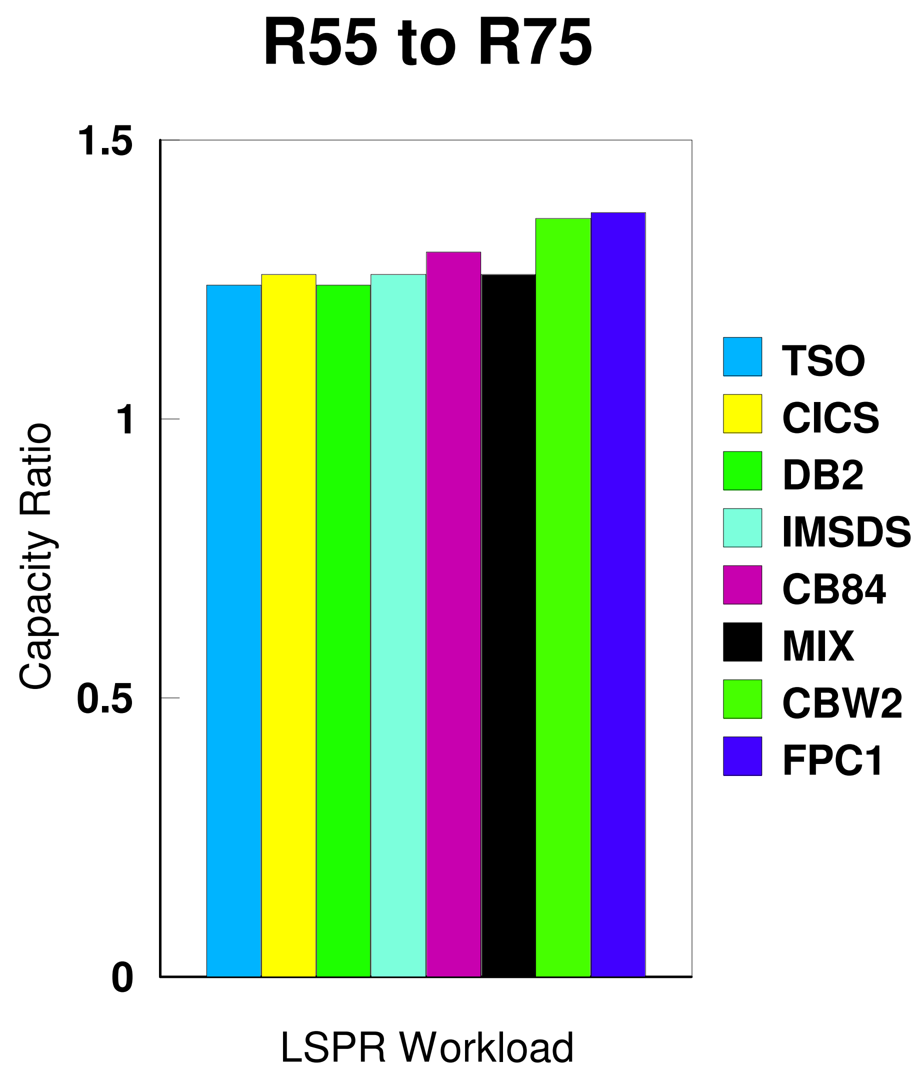
- 9X2
  - Cycle time: 7.1 ns
  - L1: 128k i and 128k d
  - L2: 4mb / side shared
  - L3: storage controller design
  - multiple decode, prefetch
  - sophisticated branch history
- RY5
  - Cycle time: 2.7 ns
  - L1: 64k
  - L2: 768k / 3 CPs non-shared
  - L3: cross-point switch design
  - sequential decode
  - millicode

9X2 to RY5



Processor Performance Example: Number of engines change

- R55
  - Cycle time: same
  - Memory subsystem: same
  - Logic: same
  - Number of engines: 5
- R75
  - Cycle time: same
  - Memory subsystem: same
  - Logic: same
  - Number of engines: 7

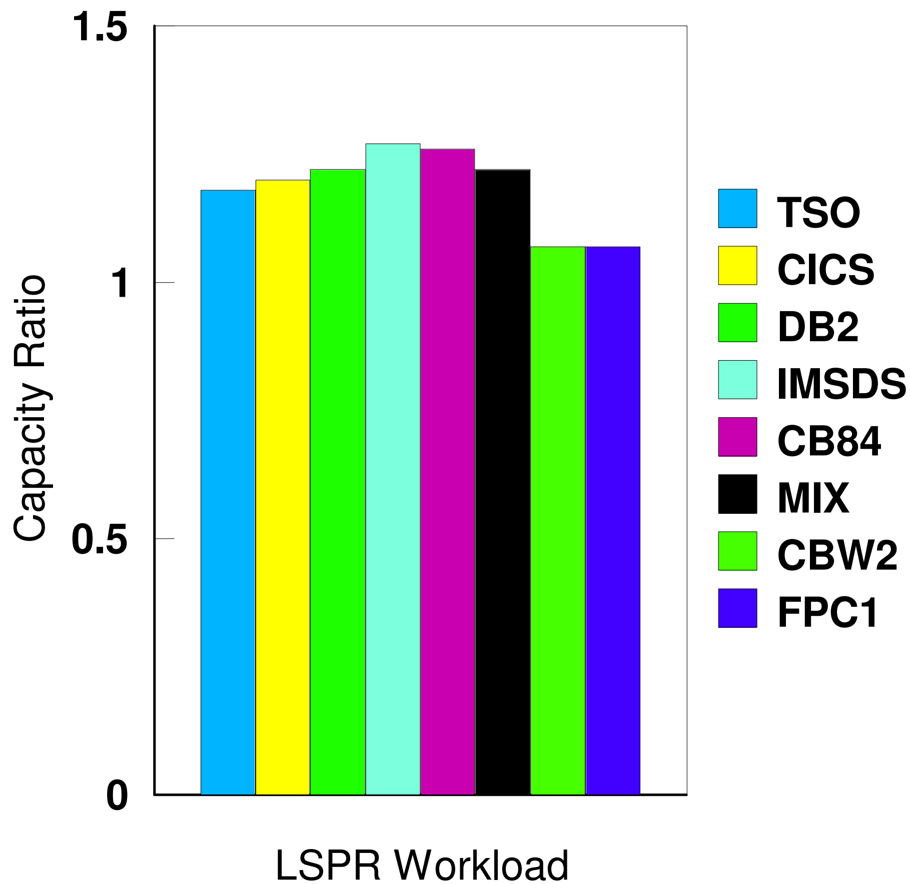


Processor Design Comparison

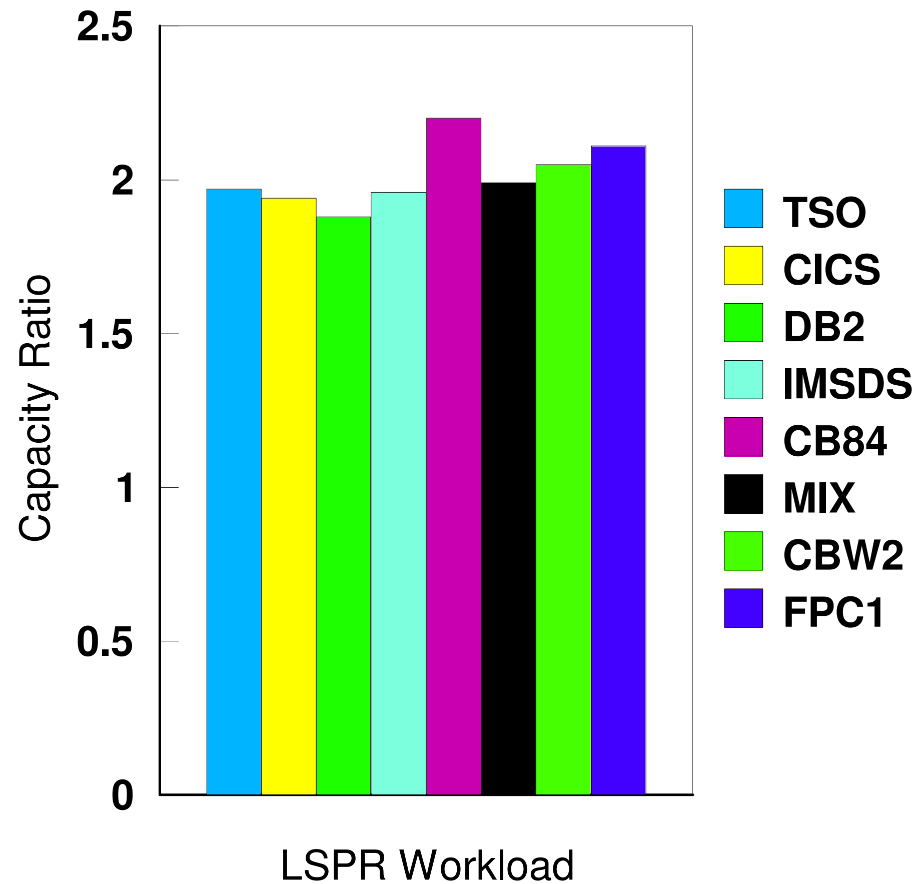
	Cycle Time	L1	L2	L2.5	L3 Access	Logic
G2	12	16k	384k/CP non-shr	-	xpt-switch	millicode + hardware
G3	6.5,5.9	32k	256k/CP non-shr	2mb	xpt-switch	millicode + hardware
G4	3.3,3.1,2.7	64k	768k/3CP non-shr	2mb	xpt-switch	millicode + hardware
G5	2.4,2.0	256k	4mb/side non-shr	-	stg-cntlr	more hdw brnch hst
H5	7.1	128k i 128k d	4mb/side shared	-	stg-cntlr	multi-decode ++ brnch hst

Upgrade to Next CMOS Generation

G2 to G3
RX3 to R54

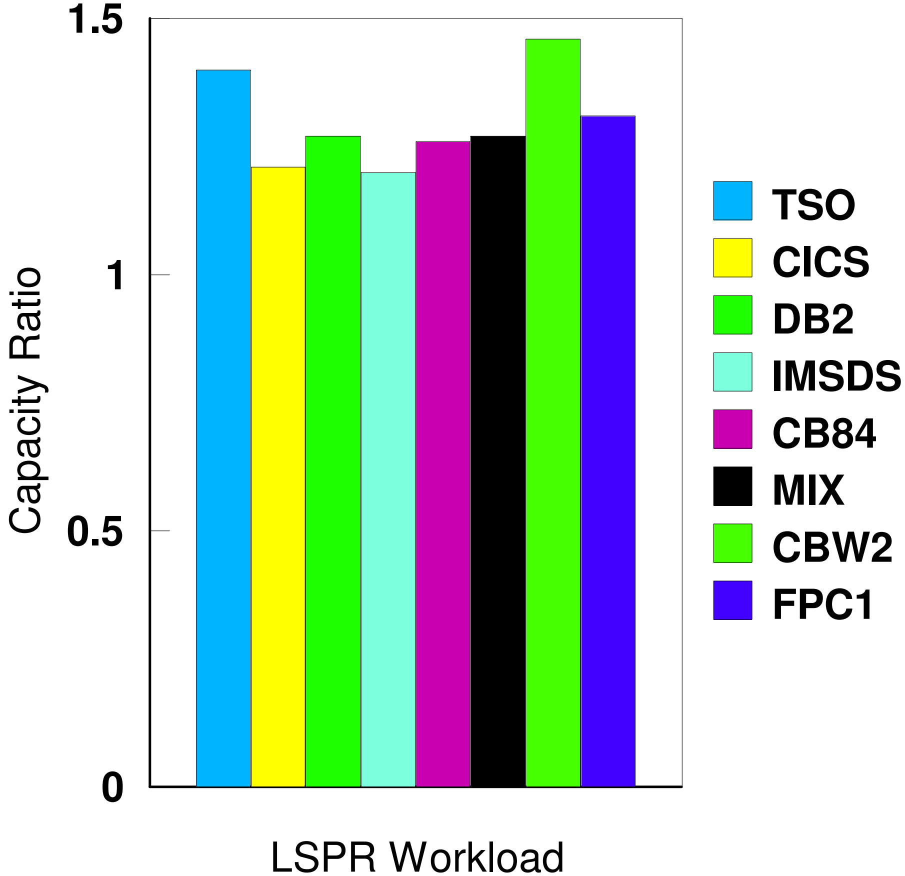


G2 to G3
RX3 to RX4

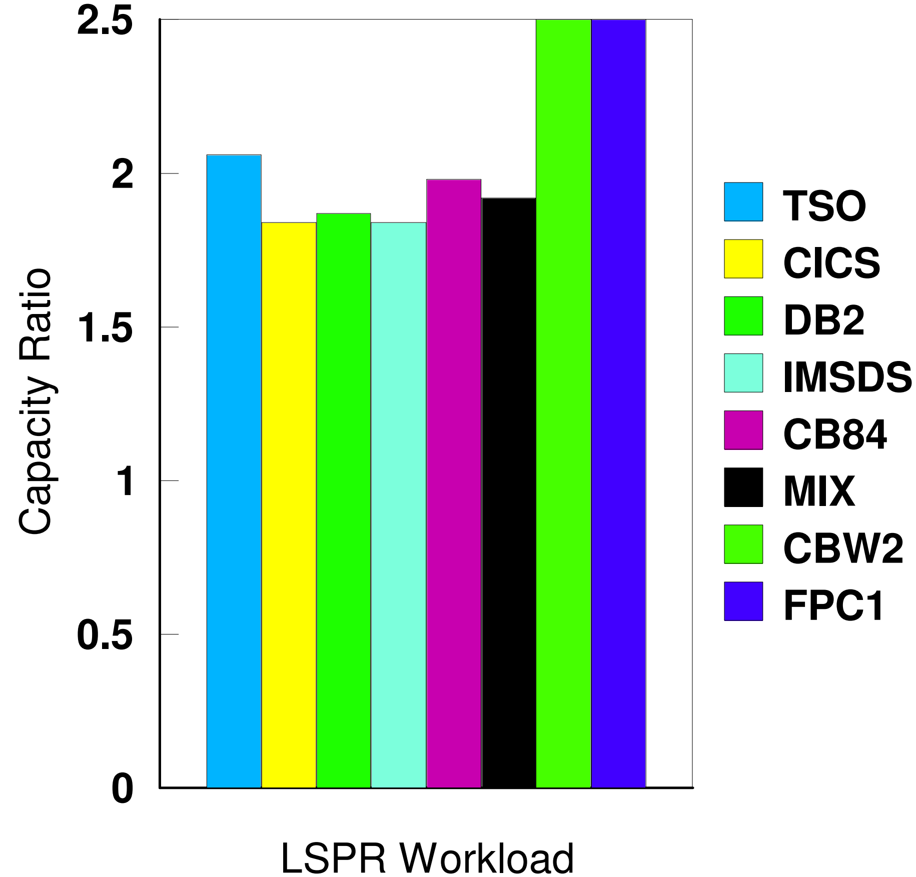


Upgrade to Next CMOS Generation

G3 to G4
R54 to R55

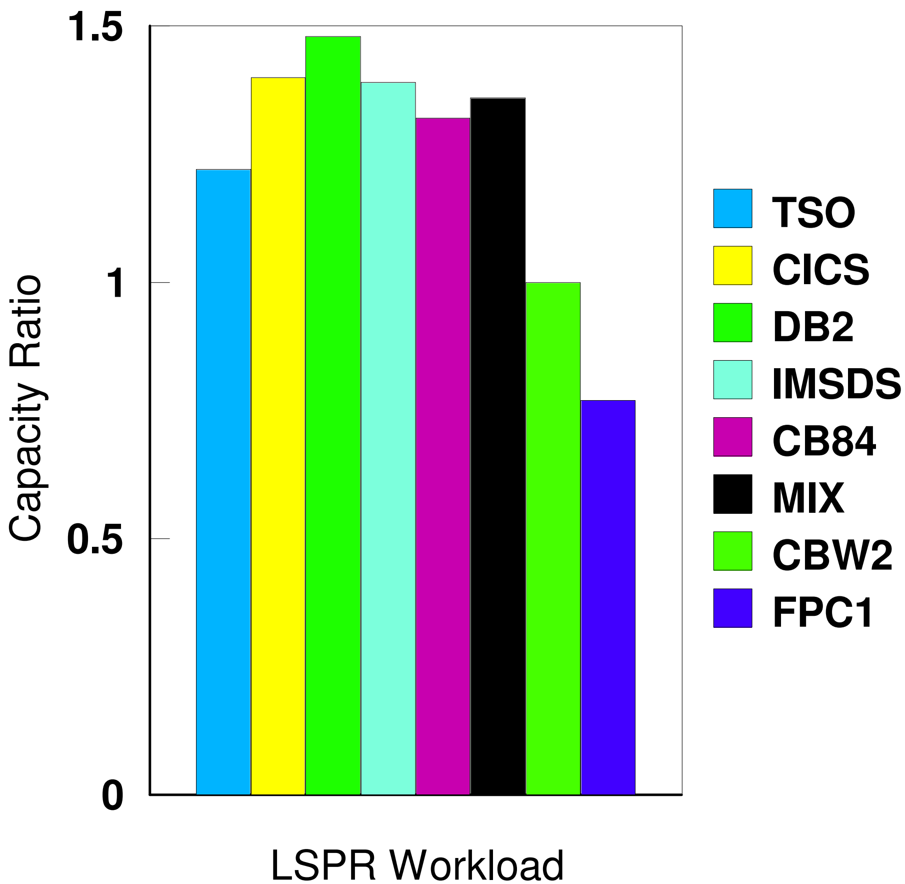


G3 to G4
R54 to RX5

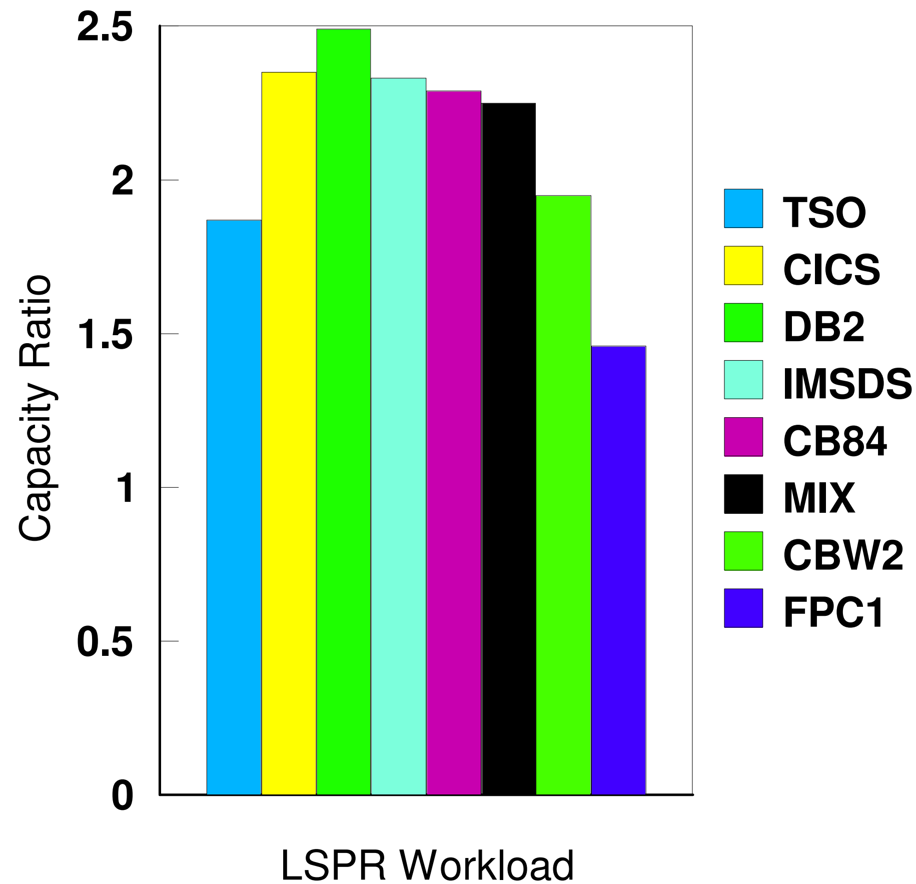


Upgrade to Next CMOS Generation

G4 to G5
RX5 to R56

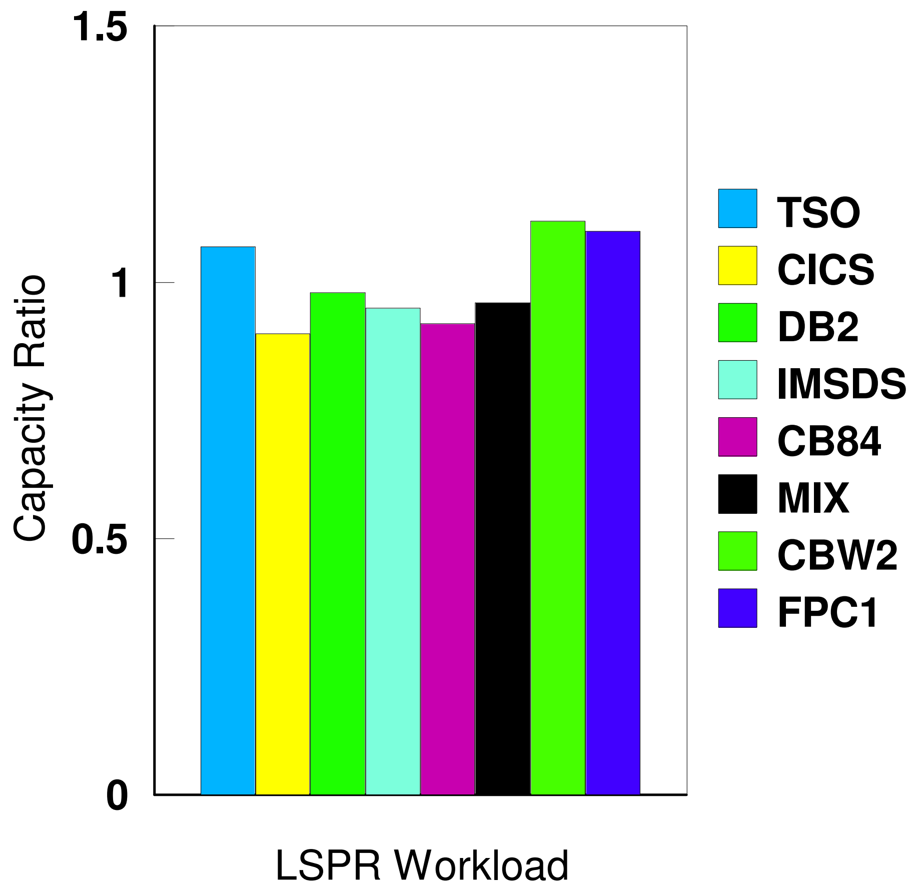


G4 to G5
RX5 to RX6

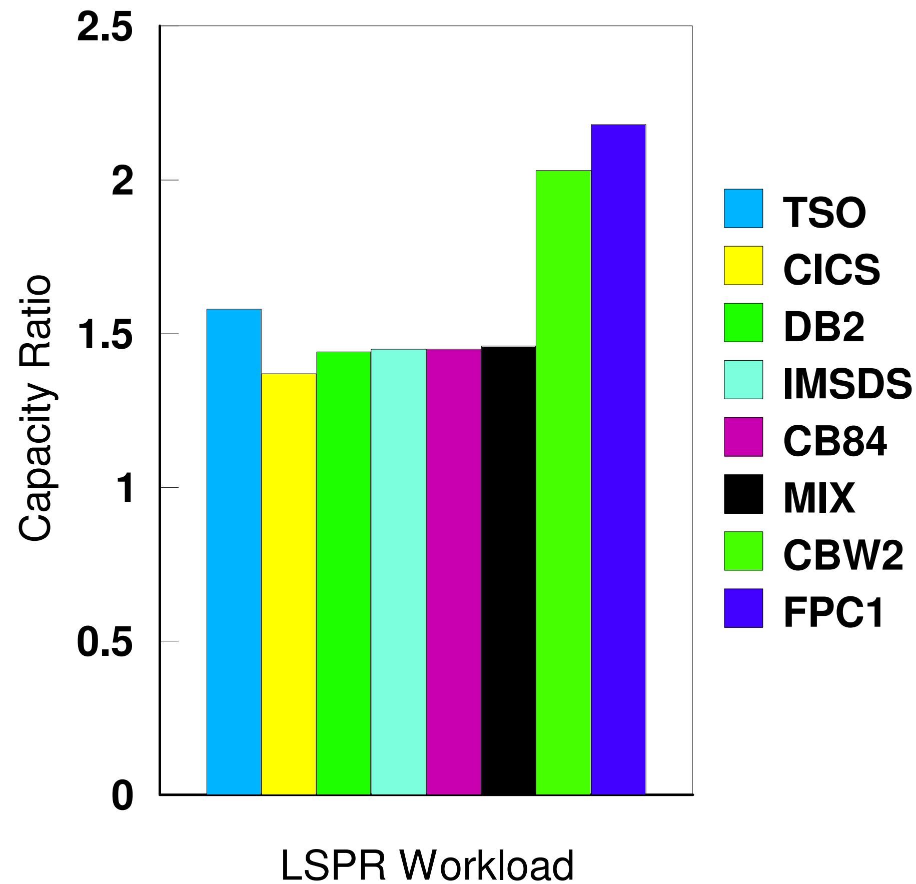


Upgrade Bipolar to CMOS

H5 to G4
952 to R55

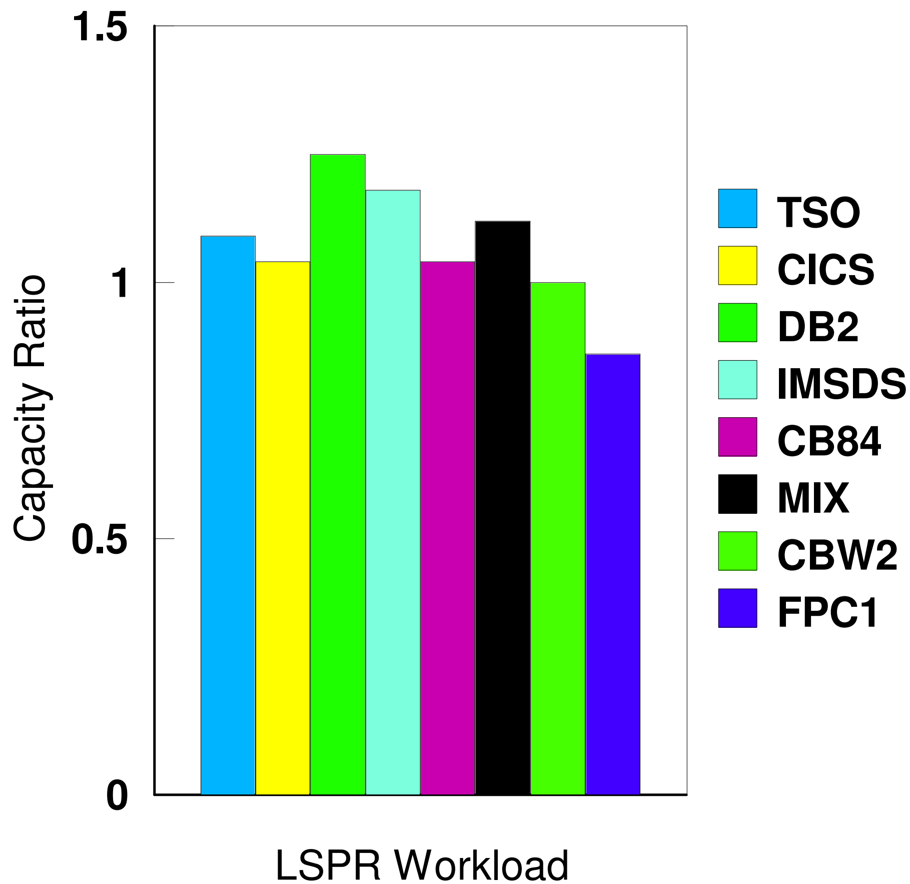


H5 to G4
952 to RX5

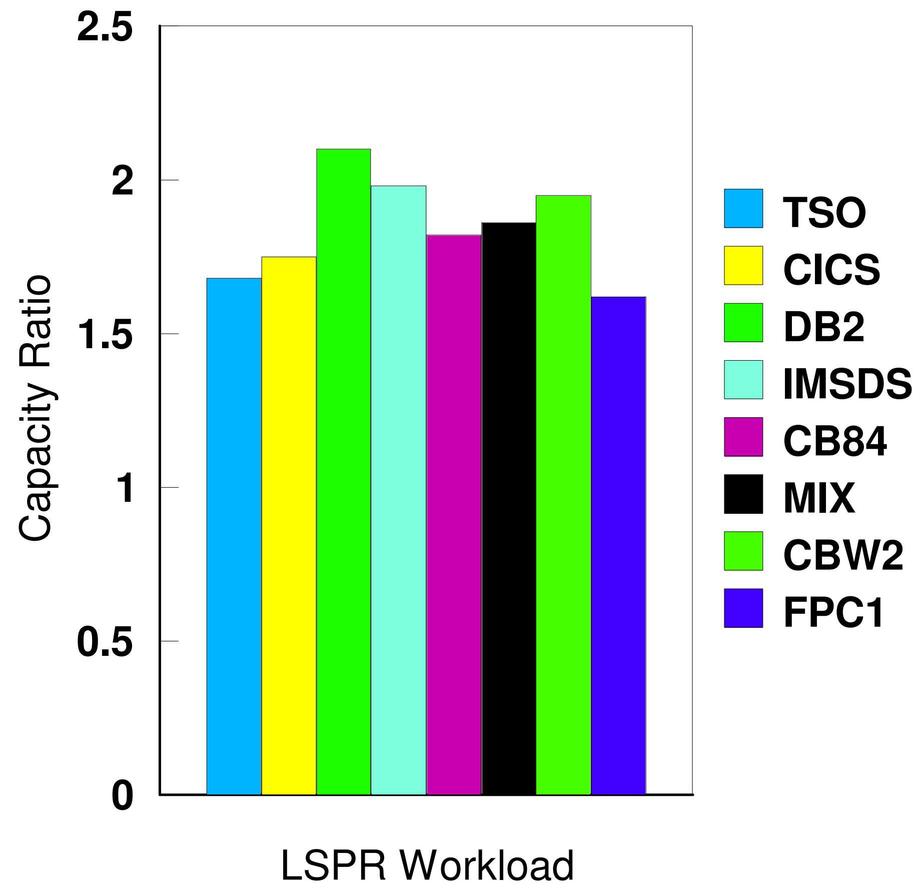


Upgrade Bipolar to CMOS

H5 to G5
9X2 to R56

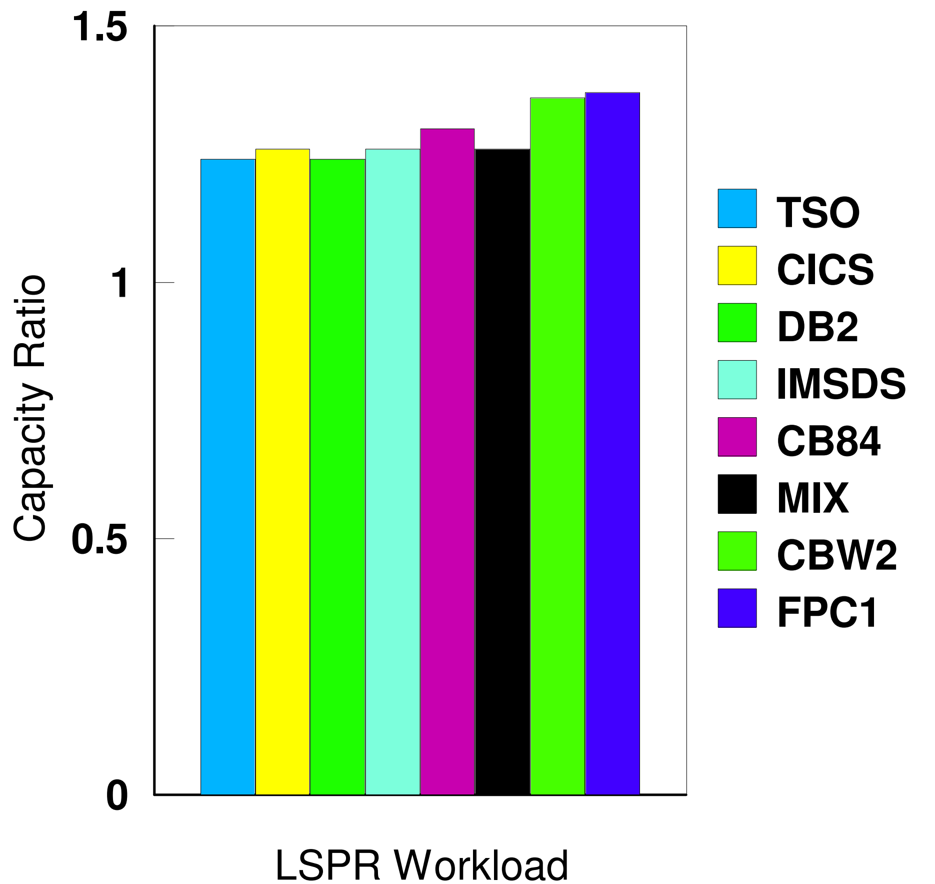


H5 to G5
9X2 to RX6

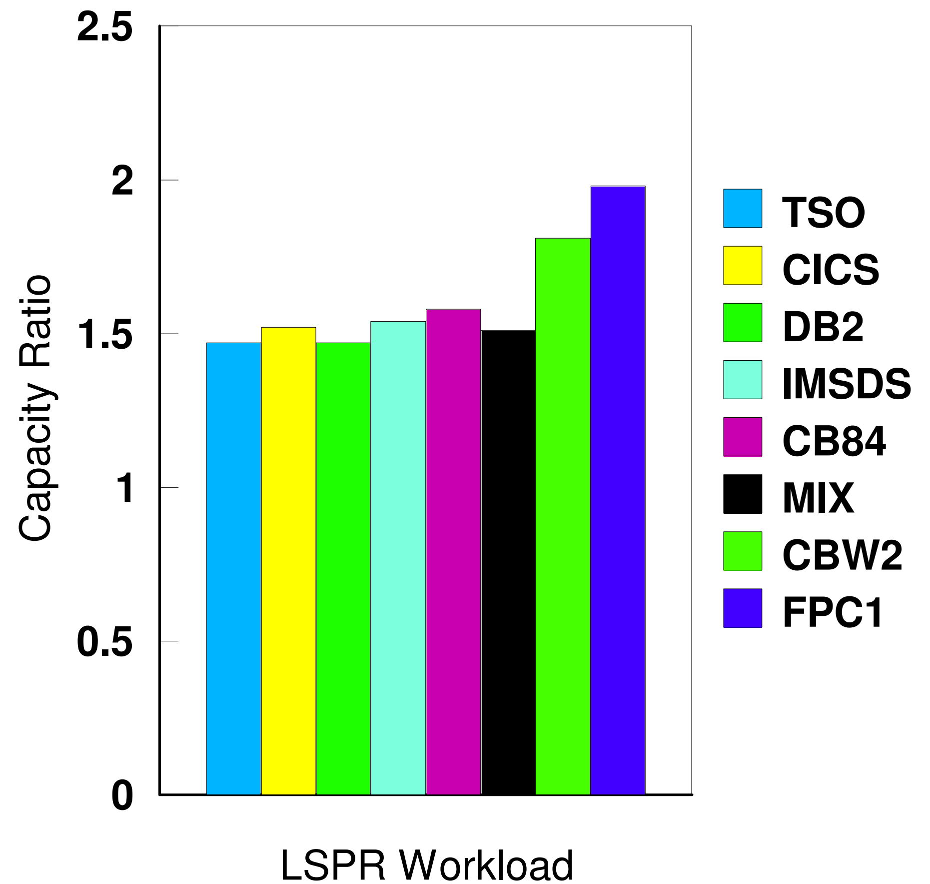


Upgrade Number of Engines

G4
R55 to R75

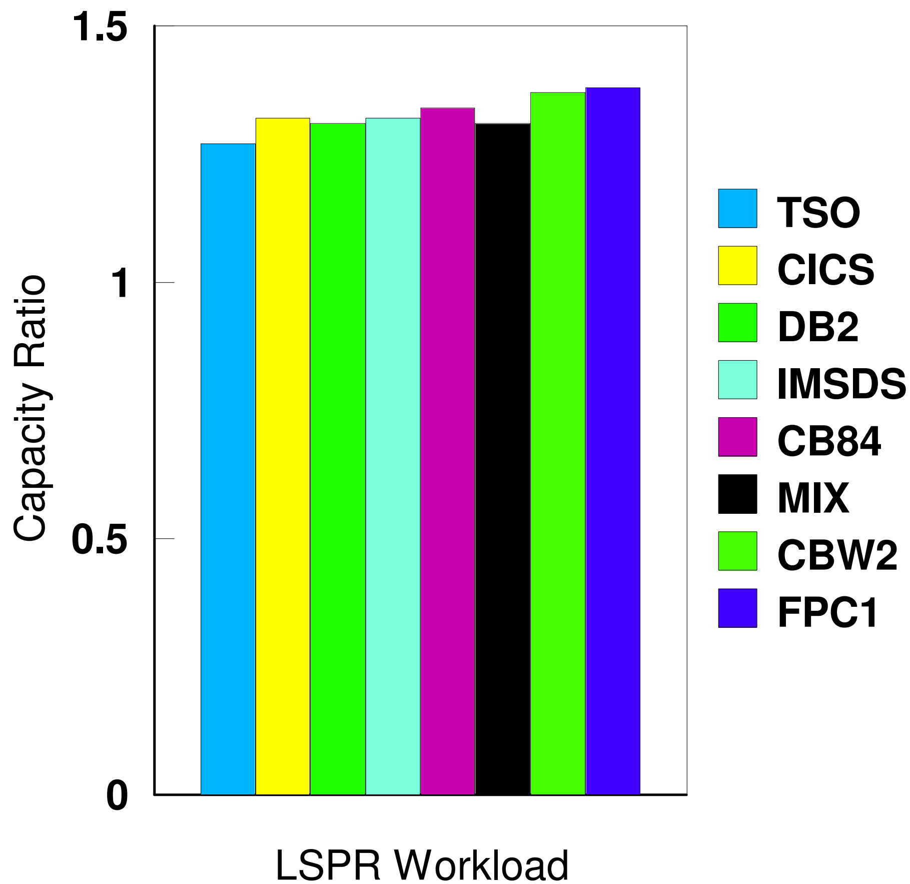


G4
R55 to RX5

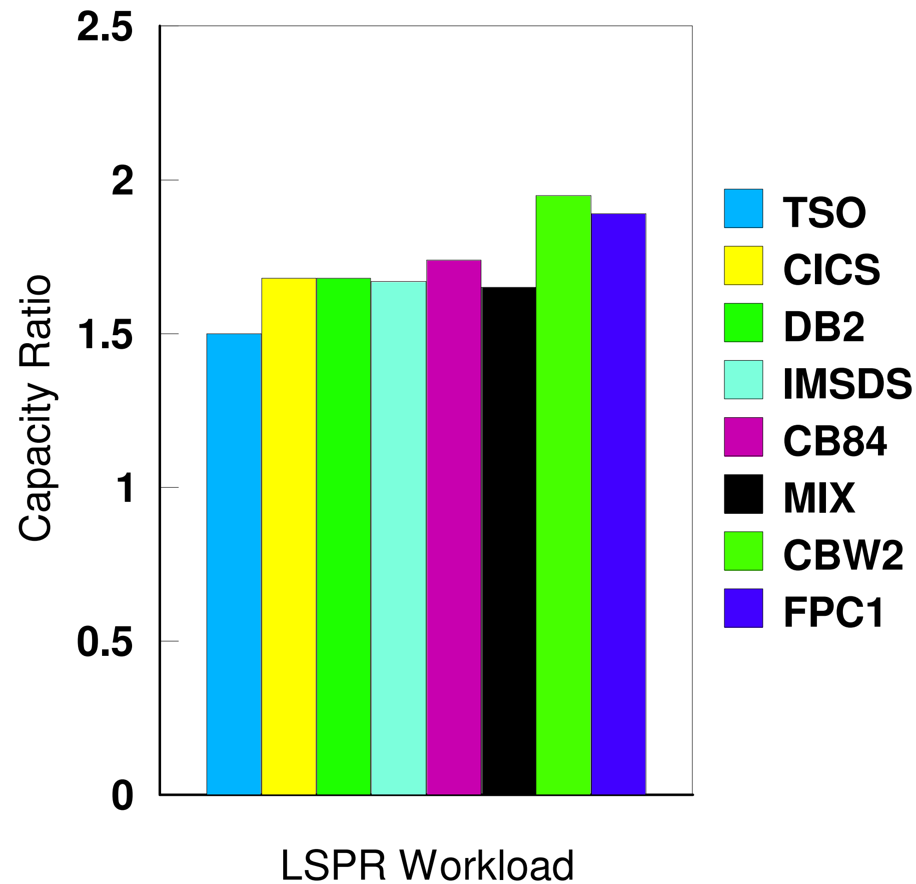


Upgrade Number of Engines

G5
R56 to R76



G5
R56 to RX6



LSPR Workload Capacity Ratios: Sensitive to type of upgrade

- Add engines within processor family
  - Generally similar ratios
  - Memory-subsystem-light workloads can have slightly higher ratios
- Majority of improvement from cycle time reduction
  - Generally similar ratios
  - Memory-subsystem-light workloads can have higher ratios
- Majority of improvement from enhanced memory subsystem
  - Wide range in ratios
  - Memory-subsystem-light workloads will have lower ratios
- Majority of improvement from logic enhancements
  - Likely to be somewhat variable
- Balanced improvements in all areas
  - Generally similar ratios

Current and Future Upgrade Sensitivities

From	To	Major Difference(s)
H5	G5,G6	cycle time, mem-subsys+, logic
G4	G5,...,G6,G7	memory-subsystem+++
G5	G6	cycle time
G6	G7	cycle time, mem-subsys, logic