```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                     2 ************************************************************************
                                                     3 *
                                                     4 *            CLC, CLCL, MVCIN and TRT instruction tests
                                                     5 *
                                                     6 ************************************************************************
                                                     7 *
                                                     8 *  This program tests proper functioning of the CLCL, MVCIN and TRT
                                                     9 *  instructions.  It also optionally times them.
                                                    10 *
                                                    11 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                    12 *  obvious coding errors.  None of the tests are thorough.  They are
                                                    13 *  NOT designed to test all aspects of any of the instructions.
                                                    14 *
                                                    15 ************************************************************************
                                                    16 *
                                                    17 *  Example Hercules Testcase:
                                                    18 *
                                                    19 *
                                                    20 *     *Testcase CLCL-et-al (Test CLCL, MVCIN and TRT instructions)
                                                    21 *
                                                    22 *     archlvl     390
                                                    23 *     mainsize    2
                                                    24 *     numcpu      1
                                                    25 *     sysclear
                                                    26 *
                                                    27 *     loadcore    "$(testpath)/CLCL-et-al.core"
                                                    28 *
                                                    29 *     ##r           21fd=ff   # (enable timing tests too!)
                                                    30 *     ##runtest     150       # (TIMING too test duration)
                                                    31 *     runtest     1         # (NON-timing test duration)
                                                    32 *
                                                    33 *     *Done
                                                    34 *
                                                    35 *
                                                    36 ************************************************************************
```

```
 LOC         OBJECT CODE        ADDR1     ADDR2     STMT

                                                       38           PRINT OFF
                                                     3419           PRINT ON

                                                     3421 ********************************************************************************
                                                     3422 *        SATK prolog stuff...
                                                     3423 ********************************************************************************

                                                     3425           ARCHLVL  ZARCH=NO,MNOTE=NO
                                                     3427+$AL       OPSYN AL
                                                     3428+$ALR      OPSYN ALR
                                                     3429+$B        OPSYN B
                                                     3430+$BAS      OPSYN BAS
                                                     3431+$BASR     OPSYN BASR
                                                     3432+$BC       OPSYN BC
                                                     3433+$BCTR     OPSYN BCTR
                                                     3434+$BE       OPSYN BE
                                                     3435+$BH       OPSYN BH
                                                     3436+$BL       OPSYN BL
                                                     3437+$BM       OPSYN BM
                                                     3438+$BNE      OPSYN BNE
                                                     3439+$BNH      OPSYN BNH
                                                     3440+$BNL      OPSYN BNL
                                                     3441+$BNM      OPSYN BNM
                                                     3442+$BNO      OPSYN BNO
                                                     3443+$BNP      OPSYN BNP
                                                     3444+$BNZ      OPSYN BNZ
                                                     3445+$BO       OPSYN BO
                                                     3446+$BP       OPSYN BP
                                                     3447+$BXLE     OPSYN BXLE
                                                     3448+$BZ       OPSYN BZ
                                                     3449+$CH       OPSYN CH
                                                     3450+$L        OPSYN L
                                                     3451+$LH       OPSYN LH
                                                     3452+$LM       OPSYN LM
                                                     3453+$LPSW     OPSYN LPSW
                                                     3454+$LR       OPSYN LR
                                                     3455+$LTR      OPSYN LTR
                                                     3456+$NR       OPSYN NR
                                                     3457+$SL       OPSYN SL
                                                     3458+$SLR      OPSYN SLR
                                                     3459+$SR       OPSYN SR
                                                     3460+$ST       OPSYN ST
                                                     3461+$STM      OPSYN STM
                                                     3462+$X        OPSYN X
                                                     3463+$AHI      OPSYN AHI
                                                     3464+$B        OPSYN J
                                                     3465+$BC       OPSYN BRC
                                                     3466+$BE       OPSYN JE
                                                     3467+$BH       OPSYN JH
                                                     3468+$BL       OPSYN JL
                                                     3469+$BM       OPSYN JM
                                                     3470+$BNE      OPSYN JNE
```

```
 LOC         OBJECT CODE        ADDR1     ADDR2     STMT

                                                   3471+$BNH     OPSYN JNH
                                                   3472+$BNL     OPSYN JNL
                                                   3473+$BNM     OPSYN JNM
                                                   3474+$BNO     OPSYN JNO
                                                   3475+$BNP     OPSYN JNP
                                                   3476+$BNZ     OPSYN JNZ
                                                   3477+$BO      OPSYN JO
                                                   3478+$BP      OPSYN JP
                                                   3479+$BXLE    OPSYN JXLE
                                                   3480+$BZ      OPSYN JZ
                                                   3481+$CHI     OPSYN CHI
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  3483 ********************************************************************
                                                  3484 *        Initiate the CLCLetal CSECT in the CODE region
                                                  3485 *        with the location counter at 0
                                                  3486 ********************************************************************

                                                  3488 CLCLetal ASALOAD  REGION=CODE
                                00000000  00003000  3489+CLCLetal START 0,CODE
00000000  000A0000 00000008                       3491+         PSW   0,0,2,0,X'008'      64-bit Restart ISR Trap New PSW
00000008                      00000008  00000058  3492+         ORG   CLCLetal+X'058'
00000058  000A0000 00000018                       3494+         PSW   0,0,2,0,X'018'      64-bit External ISR Trap New PSW
00000060  000A0000 00000020                       3495+         PSW   0,0,2,0,X'020'      64-bit Supervisor Call ISR Trap New PSW
00000068  000A0000 00000028                       3496+         PSW   0,0,2,0,X'028'      64-bit Program ISR Trap New PSW
00000070  000A0000 00000030                       3497+         PSW   0,0,2,0,X'030'      64-bit Machine Check Trap New PSW
00000078  000A0000 00000038                       3498+         PSW   0,0,2,0,X'038'      64-bit Input/Output Trap New PSW
00000080                      00000080  00000200  3499+         ORG   CLCLetal+512



                                                  3501 ********************************************************************
                                                  3502 *        Create IPL (restart) PSW
                                                  3503 ********************************************************************


                                                  3505          ASAIPL   IA=BEGIN
00000200                      00000200  00000000  3506+         ORG   CLCLetal
00000000  00080000 00000200                       3507+         PSW   0,0,0,0,BEGIN,24
00000008                      00000008  00000200  3508+         ORG   CLCLetal+512     Reset CSECT to end of assigned storage area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    3510 ********************************************************************************
                                                    3511 *                The actual "CLCLetal" program itself...
                                                    3512 ********************************************************************************
                                                    3513 *
                                                    3514 *  Architecture Mode: 390
                                                    3515 *  Addressing Mode:   31-bit
                                                    3516 *  Register Usage:
                                                    3517 *
                                                    3518 *   R0       (work)
                                                    3519 *   R1       I/O device used by ENADEV and RAWIO macros
                                                    3520 *   R2       First base register
                                                    3521 *   R3       IOCB pointer for ENADEV and RAWIO macros
                                                    3522 *   R4       IO work register used by ENADEV and RAWIO
                                                    3523 *   R5-R7    (work)
                                                    3524 *   R8       ORB pointer
                                                    3525 *   R9       Second base register
                                                    3526 *   R10-R13  (work)
                                                    3527 *   R14      Subroutine call
                                                    3528 *   R15      Secondary Subroutine call or work
                                                    3529 *
                                                    3530 ********************************************************************************

00000200                    00000000                3532          USING  ASA,R0          Low core addressability
00000200                    00000200                3533          USING  BEGIN,R2        FIRST Base Register
00000200                    00001200                3534          USING  BEGIN+4096,R9   SECOND Base Register
00000200                    00000000                3535          USING  IOCB,R3         SATK Device I/O Control Block
00000200                    00000000                3536          USING  ORB,R8          ESA/390 Operation Request Block

00000200  0520                                      3538 BEGIN    BALR   R2,0            Initalize FIRST base register
00000202  0620                                      3539          BCTR   R2,0            Initalize FIRST base register
00000204  0620                                      3540          BCTR   R2,0            Initalize FIRST base register

00000206  4190 2800                  00000800       3542          LA     R9,2048(,R2)    Initalize SECOND base register
0000020A  4190 9800                  00000800       3543          LA     R9,2048(,R9)    Initalize SECOND base register

0000020E  45E0 91E8                  000013E8       3545          BAL    R14,INIT        Initalize Program
                                                    3546 *
                                                    3547 **       Run the tests...
                                                    3548 *
00000212  45E0 2052                  00000252       3549          BAL    R14,TEST01      Test CLC   instruction
00000216  45E0 2108                  00000308       3550          BAL    R14,TEST02      Test CLCL  instruction
0000021A  45E0 21E2                  000003E2       3551          BAL    R14,TEST03      Test MVCIN instruction
0000021E  45E0 2228                  00000428       3552          BAL    R14,TEST04      Test TRT   instruction
                                                    3553 *
00000222  45E0 22D0                  000004D0       3554          BAL    R14,TEST91      Time CLC   instruction  (speed test)
00000226  45E0 25B2                  000007B2       3555          BAL    R14,TEST92      Time CLCL  instruction  (speed test)
0000022A  45E0 29E8                  00000BE8       3556          BAL    R14,TEST93      Time MVCIN instruction  (speed test)
0000022E  45E0 2C8E                  00000E8E       3557          BAL    R14,TEST94      Time TRT   instruction  (speed test)
                                                    3558 *
00000232  45E0 2F3E                  0000113E       3559          BAL    R14,TEST95      Test CLCL page fault handling
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                 3561 ********************************************************************************
                                                 3562 *         Test for normal or unexpected test completion...
                                                 3563 ********************************************************************************

00000236  9500 9FFD                    000021FD  3565          CLI   TIMEOPT,X'00'    Normal (non-timing) run?
0000023A  4770 9238                    00001438  3566          BNE   EOJ              No, timing run; just go end normally

0000023E  9595 9FFE                    000021FE  3568          CLI   TESTNUM,X'95'    Did we end on expected test?
00000242  4770 9268                    00001468  3569          BNE   FAILTEST         No?! Then FAIL the test!

00000246  9510 9FFF                    000021FF  3571          CLI   SUBTEST,X'10'    Did we end on expected SUB-test?
0000024A  4770 9268                    00001468  3572          BNE   FAILTEST         No?! Then FAIL the test!

0000024E  47F0 9238                    00001438  3574          B     EOJ              Yes, then normal completion!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                          3576 ********************************************************************************
                                          3577 *        TEST01                  Test CLC instruction
                                          3578 ********************************************************************************

00000252  9201 9FFE                     000021FE  3580 TEST01   MVI   TESTNUM,X'01'
                                          3581 *
                                          3582 **       Initialize test parameters...
                                          3583 *
00000256  5850 9458                     00001658  3584          L      R5,CLC4          Operand-1 address
0000025A  92FF 5003                     00000003  3585          MVI    3(R5),X'FF'      Force unequal compare (op1 high)
0000025E  5850 9468                     00001668  3586          L      R5,CLC256        (same thing for CLC256)
00000262  92FF 50FF                     000000FF  3587          MVI    255(R5),X'FF'    (same thing for CLC256)
00000266  5850 9470                     00001670  3588          L      R5,CLCOP1        (same thing for CLCOP1)
0000026A  92FF 50FF                     000000FF  3589          MVI    255(R5),X'FF'    (same thing for CLCOP1)
0000026E  5860 9464                     00001664  3590          L      R6,CLC8+4        OPERAND-2(!) address
00000272  92FF 6007                     00000007  3591          MVI    7(R6),X'FF'      Force OPERAND-2 to be high! (op1 LOW!)
                                          3592 *
                                          3593 **       Neither cross (one byte)
                                          3594 *
00000276  9201 9FFF                     000021FF  3595          MVI   SUBTEST,X'01'
0000027A  9856 9438                     00001638  3596          LM    R5,R6,CLC1
0000027E  D500 5000 6000      00000000  00000000  3597          CLC   0(1,R5),0(R6)
00000284  4770 9268                     00001468  3598          BNE   FAILTEST
                                          3599 *
                                          3600 **       Neither cross (two bytes)
                                          3601 *
00000288  9202 9FFF                     000021FF  3602          MVI   SUBTEST,X'02'
0000028C  9856 9440                     00001640  3603          LM    R5,R6,CLC2
00000290  D501 5000 6000      00000000  00000000  3604          CLC   0(2,R5),0(R6)
00000296  4770 9268                     00001468  3605          BNE   FAILTEST
                                          3606 *
                                          3607 **       Neither cross (four bytes)
                                          3608 *
0000029A  9204 9FFF                     000021FF  3609          MVI   SUBTEST,X'04'
0000029E  9856 9458                     00001658  3610          LM    R5,R6,CLC4
000002A2  D503 5000 6000      00000000  00000000  3611          CLC   0(4,R5),0(R6)
000002A8  47D0 9268                     00001468  3612          BNH   FAILTEST                 (see INIT; CLC4:    op1 > op2)
                                          3613 *
                                          3614 **       Neither cross (eight bytes)
                                          3615 *
000002AC  9208 9FFF                     000021FF  3616          MVI   SUBTEST,X'08'
000002B0  9856 9460                     00001660  3617          LM    R5,R6,CLC8
000002B4  D507 5000 6000      00000000  00000000  3618          CLC   0(8,R5),0(R6)
000002BA  47B0 9268                     00001468  3619          BNL   FAILTEST                 (see INIT; CLC8:    op1 < op2)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3621 *
                                                  3622 **       Neither cross (256 bytes)
                                                  3623 *
000002BE  92FF 9FFF                     000021FF  3624          MVI   SUBTEST,X'FF'
000002C2  9856 9468                     00001668  3625          LM    R5,R6,CLC256
000002C6  D5FF 5000 6000      00000000  00000000  3626          CLC   0(256,R5),0(R6)
000002CC  47D0 9268                     00001468  3627          BNH   FAILTEST                (see INIT; CLC256:  op1 > op2)
                                                  3628 *
                                                  3629 **       Both cross
                                                  3630 *
000002D0  9222 9FFF                     000021FF  3631          MVI   SUBTEST,X'22'
000002D4  9856 9448                     00001648  3632          LM    R5,R6,CLCBOTH
000002D8  D5FF 5000 6000      00000000  00000000  3633          CLC   0(256,R5),0(R6)
000002DE  4770 9268                     00001468  3634          BNE   FAILTEST
                                                  3635 *
                                                  3636 **       Only op1 crosses
                                                  3637 *
000002E2  9210 9FFF                     000021FF  3638          MVI   SUBTEST,X'10'
000002E6  9856 9470                     00001670  3639          LM    R5,R6,CLCOP1
000002EA  D5FF 5000 6000      00000000  00000000  3640          CLC   0(256,R5),0(R6)
000002F0  47D0 9268                     00001468  3641          BNH   FAILTEST                (see INIT; CLCOP1:  op1 > op2)
                                                  3642 *
                                                  3643 **       Only op2 crosses
                                                  3644 *
000002F4  9220 9FFF                     000021FF  3645          MVI   SUBTEST,X'20'
000002F8  9856 9450                     00001650  3646          LM    R5,R6,CLCOP2
000002FC  D5FF 5000 6000      00000000  00000000  3647          CLC   0(256,R5),0(R6)
00000302  4770 9268                     00001468  3648          BNE   FAILTEST
                                                  3649 *
00000306  07FE                                    3650          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  3652 ********************************************************************************
                                                  3653 *        TEST02                    Test CLCL instruction
                                                  3654 ********************************************************************************

00000308  9202 9FFE                     000021FE  3656 TEST02   MVI   TESTNUM,X'02'
                                                  3657 *
                                                  3658 **       Initialize test parameters...
                                                  3659 *
0000030C  9856 9E9C                     0000209C  3660          LM    R5,R6,CLCL4     CLCL4 test Op1 address and length
00000310  1E56                                    3661          ALR   R5,R6           Point past last byte
00000312  0650                                    3662          BCTR  R5,0            Backup to last byte
00000314  92FF 5000                     00000000  3663          MVI   0(R5),X'FF'     Force unequal compare (op1 high)
                                                  3664 *
00000318  9856 9EBC                     000020BC  3665          LM    R5,R6,CLCLOP1   (same thing for CLCLOP1 test)
0000031C  1E56                                    3666          ALR   R5,R6                    "
0000031E  0650                                    3667          BCTR  R5,0                     "
00000320  92FF 5000                     00000000  3668          MVI   0(R5),X'FF'              "
                                                  3669 *
00000324  9856 9EB4                     000020B4  3670          LM    R5,R6,CLCL8+8   CLCL8 test ===> OP2 <===
00000328  1E56                                    3671          ALR   R5,R6
0000032A  0650                                    3672          BCTR  R5,0
0000032C  92FF 5000                     00000000  3673          MVI   0(R5),X'FF'     ===> OPERAND-2 high (OP1 LOW) <===
                                                  3674 *
                                                  3675 **       Neither cross (one byte)
                                                  3676 *
00000330  9201 9FFF                     000021FF  3677          MVI   SUBTEST,X'01'
00000334  98AD 9E3C                     0000203C  3678          LM    R10,R13,CLCL1
00000338  0FAC                                    3679          CLCL  R10,R12
0000033A  4770 9268                     00001468  3680          BNE   FAILTEST
0000033E  4150 9EDC                     000020DC  3681          LA    R5,ECLCL1
00000342  45F0 91FA                     000013FA  3682          BAL   R15,ENDCLCL
                                                  3683 *
                                                  3684 **       Neither cross (two bytes)
                                                  3685 *
00000346  9202 9FFF                     000021FF  3686          MVI   SUBTEST,X'02'
0000034A  98AD 9E4C                     0000204C  3687          LM    R10,R13,CLCL2
0000034E  0FAC                                    3688          CLCL  R10,R12
00000350  4770 9268                     00001468  3689          BNE   FAILTEST
00000354  4150 9EEC                     000020EC  3690          LA    R5,ECLCL2
00000358  45F0 91FA                     000013FA  3691          BAL   R15,ENDCLCL
                                                  3692 *
                                                  3693 **       Neither cross (four bytes)
                                                  3694 **       (inequality on last byte of op1)
                                                  3695 *
0000035C  9204 9FFF                     000021FF  3696          MVI   SUBTEST,X'04'
00000360  98AD 9E9C                     0000209C  3697          LM    R10,R13,CLCL4
00000364  0FAC                                    3698          CLCL  R10,R12
00000366  47D0 9268                     00001468  3699          BNH   FAILTEST                (see INIT; CLCL4:   op1 > op2)
0000036A  4150 9F3C                     0000213C  3700          LA    R5,ECLCL4
0000036E  45F0 91FA                     000013FA  3701          BAL   R15,ENDCLCL
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   3703 *
                                                   3704 **       Neither cross (eight bytes)
                                                   3705 **       (inequality on last byte of op2)
                                                   3706 *
00000372  9208 9FFF                    000021FF   3707          MVI   SUBTEST,X'08'
00000376  98AD 9EAC                    000020AC   3708          LM    R10,R13,CLCL8
0000037A  0FAC                                    3709          CLCL  R10,R12
0000037C  47B0 9268                    00001468   3710          BNL   FAILTEST                  (see INIT; CLCL8:   op1 < op2)
00000380  4150 9F4C                    0000214C   3711          LA    R5,ECLCL8
00000384  45F0 91FA                    000013FA   3712          BAL   R15,ENDCLCL
                                                   3713 *
                                                   3714 **       Neither cross (1K bytes)
                                                   3715 *
00000388  9200 9FFF                    000021FF   3716          MVI   SUBTEST,X'00'
0000038C  98AD 9E6C                    0000206C   3717          LM    R10,R13,CLCL1K
00000390  0FAC                                    3718          CLCL  R10,R12
00000392  4770 9268                    00001468   3719          BNE   FAILTEST
00000396  4150 9F0C                    0000210C   3720          LA    R5,ECLCL1K
0000039A  45F0 91FA                    000013FA   3721          BAL   R15,ENDCLCL
                                                   3722 *
                                                   3723 **       Both cross
                                                   3724 *
0000039E  9222 9FFF                    000021FF   3725          MVI   SUBTEST,X'22'
000003A2  98AD 9E7C                    0000207C   3726          LM    R10,R13,CLCLBOTH
000003A6  0FAC                                    3727          CLCL  R10,R12
000003A8  4770 9268                    00001468   3728          BNE   FAILTEST
000003AC  4150 9F1C                    0000211C   3729          LA    R5,ECLCLBTH
000003B0  45F0 91FA                    000013FA   3730          BAL   R15,ENDCLCL
                                                   3731 *
                                                   3732 **       Only op1 crosses
                                                   3733 **       (inequality on last byte of op1)
                                                   3734 *
000003B4  9210 9FFF                    000021FF   3735          MVI   SUBTEST,X'10'
000003B8  98AD 9EBC                    000020BC   3736          LM    R10,R13,CLCLOP1
000003BC  0FAC                                    3737          CLCL  R10,R12
000003BE  47D0 9268                    00001468   3738          BNH   FAILTEST                  (see INIT; CLCLOP1: op1 > op2)
000003C2  4150 9F5C                    0000215C   3739          LA    R5,ECLCLOP1
000003C6  45F0 91FA                    000013FA   3740          BAL   R15,ENDCLCL
                                                   3741 *
                                                   3742 **       Only op2 crosses
                                                   3743 *
000003CA  9220 9FFF                    000021FF   3744          MVI   SUBTEST,X'20'
000003CE  98AD 9E8C                    0000208C   3745          LM    R10,R13,CLCLOP2
000003D2  0FAC                                    3746          CLCL  R10,R12
000003D4  4770 9268                    00001468   3747          BNE   FAILTEST
000003D8  4150 9F2C                    0000212C   3748          LA    R5,ECLCLOP2
000003DC  45F0 91FA                    000013FA   3749          BAL   R15,ENDCLCL
                                                   3750 *
000003E0  07FE                                    3751          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   3753 ********************************************************************************
                                                   3754 *        TEST03                    Test MVCIN instruction
                                                   3755 ********************************************************************************

000003E2  9203 9FFE                      000021FE  3757 TEST03   MVI   TESTNUM,X'03'
                                                   3758 *
                                                   3759 **       Neither cross (one byte)
                                                   3760 *
000003E6  4150 9478                      00001678  3761          LA    R5,INV1
000003EA  45F0 920A                      0000140A  3762          BAL   R15,MVCINTST
                                                   3763 *
                                                   3764 **       Neither cross (two bytes)
                                                   3765 *
000003EE  4150 9488                      00001688  3766          LA    R5,INV2
000003F2  45F0 920A                      0000140A  3767          BAL   R15,MVCINTST
                                                   3768 *
                                                   3769 **       Neither cross (four bytes)
                                                   3770 *
000003F6  4150 9498                      00001698  3771          LA    R5,INV4
000003FA  45F0 920A                      0000140A  3772          BAL   R15,MVCINTST
                                                   3773 *
                                                   3774 **       Neither cross (eight bytes)
                                                   3775 *
000003FE  4150 94A8                      000016A8  3776          LA    R5,INV8
00000402  45F0 920A                      0000140A  3777          BAL   R15,MVCINTST
                                                   3778 *
                                                   3779 **       Neither cross (256 bytes)
                                                   3780 *
00000406  4150 94B8                      000016B8  3781          LA    R5,INV256
0000040A  45F0 920A                      0000140A  3782          BAL   R15,MVCINTST
                                                   3783 *
                                                   3784 **       Both cross
                                                   3785 *
0000040E  4150 94C8                      000016C8  3786          LA    R5,INVBOTH
00000412  45F0 920A                      0000140A  3787          BAL   R15,MVCINTST
                                                   3788 *
                                                   3789 **       Only op1 crosses
                                                   3790 *
00000416  4150 94D8                      000016D8  3791          LA    R5,INVOP1
0000041A  45F0 920A                      0000140A  3792          BAL   R15,MVCINTST
                                                   3793 *
                                                   3794 **       Only op2 crosses
                                                   3795 *
0000041E  4150 94E8                      000016E8  3796          LA    R5,INVOP2
00000422  45F0 920A                      0000140A  3797          BAL   R15,MVCINTST
                                                   3798 *
00000426  07FE                                     3799          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3801 ********************************************************************************
                                                  3802 *        TEST04                    Test TRT instruction
                                                  3803 ********************************************************************************

00000428  9204 9FFE                      000021FE  3805 TEST04   MVI   TESTNUM,X'04'
                                                  3806
0000042C  5010 22C4                      000004C4  3807          ST    R1,SAVER1          Save register 1
00000430  18F2                                     3808          LR    R15,R2             Save first base register
                                                  3809
00000432                                          3810          DROP  R2                 Temporarily drop addressability
00000432                  00000200                3811          USING BEGIN,R15          Establish temporary addressability
                                                  3812
00000432  4150 96F8                      000018F8  3813          LA    R5,TRTCTL          Point R5 --> testing control table
00000436                  00000000                3814          USING TRTTEST,R5         What each table entry looks like
                                                  3815
                          00000436  00000001    3816 TST4LOOP EQU   *
                                                  3817 *
                                                  3818 **       Initialize operand data  (move data to testing address)
                                                  3819 *
00000436  58A0 5008                      00000008  3820          L     R10,OP1WHERE       Where to move operand-1 data to
0000043A  58C0 5014                      00000014  3821          L     R12,OP2WHERE       Where to move operand-2 data to
                                                  3822
0000043E  5860 5000                      00000000  3823          L     R6,OP1DATA         Where op1 data is right now
00000442  5870 5004                      00000004  3824          L     R7,OP1LEN          How much of it there is
00000446  4470 F2AE                      000004AE  3825          EX    R7,TRTMVC1         Move op1 data to testing location
                                                  3826
0000044A  5860 500C                      0000000C  3827          L     R6,OP2DATA         Where op1 data is right now
0000044E  5870 5010                      00000010  3828          L     R7,OP2LEN          How much of it there is
00000452  4470 F2B4                      000004B4  3829          EX    R7,TRTMVC2         Move op1 data to testing location
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  3831 *
                                                  3832 **       Initialize R1/R2...      (TRT non-zero CC updates R1/R2!)
                                                  3833 *
00000456  1F11                                    3834          SLR   R1,R1              (known value)
00000458  5820 9354                     00001554  3835          L     R2,=A(REG2PATT)    (known value)
                                                  3836 *
                                                  3837 **       Execute TRT instruction and check for expected condition code
                                                  3838 *
0000045C  5870 5018                     00000018  3839          L     R7,EXLEN           (len-1)
00000460  58B0 501C                     0000001C  3840          L     R11,FAILMASK       (failure CC)
00000464  89B0 0004                     00000004  3841          SLL   R11,4              (shift to BC instr CC position)
                                                  3842
00000468  9200 9FFF                     000021FF  3843          MVI   SUBTEST,X'00'      (primary TRT)
0000046C  4470 F2BA                     000004BA  3844          EX    R7,TRT             TRT...
00000470  9012 F2C8                     000004C8  3845          STM   R1,R2,SAVETRT      (save R1/R2 results)
00000474  44B0 F2C0                     000004C0  3846          EX    R11,TRTBC          fail if...
                                                  3847 *
                                                  3848 **       Verify R1/R2 now contain (or still contain!) expected values
                                                  3849 *
00000478  9867 5020                     00000020  3850          LM    R6,R7,ENDREGS
                                                  3851
0000047C  9201 9FFF                     000021FF  3852          MVI   SUBTEST,X'01'      (R1 result)
00000480  1516                                    3853          CLR   R1,R6              R1 correct?
00000482  4770 F2A2                     000004A2  3854          BNE   TRTFAIL            No, FAILTEST!
                                                  3855
00000486  9202 9FFF                     000021FF  3856          MVI   SUBTEST,X'02'      (R2 result)
0000048A  1527                                    3857          CLR   R2,R7              R2 correct?
0000048C  4770 F2A2                     000004A2  3858          BNE   TRTFAIL            No, FAILTEST!
                                                  3859
00000490  4150 5028                     00000028  3860          LA    R5,TRTNEXT         Go on to next table entry
00000494  D503 9358 5000      00001558  00000000  3861          CLC   =F'0',0(R5)        End of table?
0000049A  4770 F236                     00000436  3862          BNE   TST4LOOP           No, loop...
0000049E  47F0 F2A6                     000004A6  3863          B     TRTDONE            Done! (success!)
                                                  3864
000004A2  41E0 9268                     00001468  3865 TRTFAIL  LA    R14,FAILTEST       Unexpected results!
000004A6  5810 F2C4                     000004C4  3866 TRTDONE  L     R1,SAVER1          Restore register 1
000004AA  182F                                    3867          LR    R2,R15             Restore first base register
000004AC  07FE                                    3868          BR    R14                Return to caller or FAILTEST
                                                  3869
000004AE  D200 A000 6000      00000000  00000000  3870 TRTMVC1  MVC   0(0,R10),0(R6)     (move op1 to where it should be)
000004B4  D200 C000 6000      00000000  00000000  3871 TRTMVC2  MVC   0(0,R12),0(R6)     (move op2 to where it should be)
                                                  3872
000004BA  DD00 A000 C000      00000000  00000000  3873 TRT      TRT   0(0,R10),0(R12)    (TRT op1,op2)
000004C0  4700 F2A2                     000004A2  3874 TRTBC    BC    0,TRTFAIL          (fail if unexpected condition code)
                                                  3875
000004C4  00000000                                3876 SAVER1   DC    F'0'
000004C8  00000000 00000000                       3877 SAVETRT  DC    D'0'               (saved R1/R2 from TRT results)
                                                  3878
000004D0                                          3879          DROP  R5
000004D0                                          3880          DROP  R15
000004D0                      00000200            3881          USING BEGIN,R2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  3883 ********************************************************************************
                                                  3884 *        TEST91                  Time CLC instruction  (speed test)
                                                  3885 ********************************************************************************

000004D0  91FF 9FFD                     000021FD  3887 TEST91   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
000004D4  078E                                    3888           BZR   R14              No, skip timing tests

000004D6  9291 9FFE                     000021FE  3890           MVI   TESTNUM,X'91'
000004DA  9201 9FFF                     000021FF  3891           MVI   SUBTEST,X'01'
                                                  3892 *
                                                  3893 **       First, make sure we start clean!
                                                  3894 *
000004DE  98AD 9E5C                     0000205C  3895           LM    R10,R13,CLCL256        (Yes, "CLCL256", not "CLC256"!)
000004E2  D2FF A000 C000      00000000  00000000  3896           MVC   0(256,R10),0(R12)      (forces full equal comparison)
                                                  3897 *
                                                  3898 **       Next, time the overhead...
                                                  3899 *
000004E8  5850 93A0                     000015A0  3900           L     R5,NUMLOOPS
000004EC  B205 93A8                     000015A8  3901           STCK  BEGCLOCK
000004F0  0560                                    3902           BALR  R6,0
000004F2  0656                                    3903           BCTR  R5,R6
000004F4  B205 93B0                     000015B0  3904           STCK  ENDCLOCK
000004F8  45F0 915C                     0000135C  3905           BAL   R15,CALCDUR
000004FC  D207 93C0 93B8      000015C0  000015B8  3906           MVC   OVERHEAD,DURATION
                                                  3907 *
                                                  3908 **       Now do the actual timing run...
                                                  3909 *
00000502  5850 93A0                     000015A0  3910           L     R5,NUMLOOPS
00000506  B205 93A8                     000015A8  3911           STCK  BEGCLOCK
0000050A  0560                                    3912           BALR  R6,0
0000050C  D5FF A000 C000      00000000  00000000  3913           CLC   0(256,R10),0(R12)
00000512  D5FF A000 C000      00000000  00000000  3914           CLC   0(256,R10),0(R12)
                                                  3915 *         ..........ETC..........
                                                  3916           PRINT OFF
                                                  4022           PRINT ON
0000078E  D5FF A000 C000      00000000  00000000  4023           CLC   0(256,R10),0(R12)
00000794  D5FF A000 C000      00000000  00000000  4024           CLC   0(256,R10),0(R12)
0000079A  D5FF A000 C000      00000000  00000000  4025           CLC   0(256,R10),0(R12)
000007A0  0656                                    4026           BCTR  R5,R6
000007A2  B205 93B0                     000015B0  4027           STCK  ENDCLOCK
                                                  4028 *
000007A6  D204 9409 937C      00001609  0000157C  4029           MVC   PRTLINE+33(5),=CL5'CLC'
000007AC  45F0 9082                     00001282  4030           BAL   R15,RPTSPEED
000007B0  07FE                                    4031           BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4033 ********************************************************************************
                                                  4034 *        TEST92                  Time CLCL instruction  (speed test)
                                                  4035 ********************************************************************************

000007B2  91FF 9FFD                     000021FD  4037 TEST92   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
000007B6  078E                                    4038          BZR   R14              No, skip timing tests

000007B8  9292 9FFE                     000021FE  4040          MVI   TESTNUM,X'92'
000007BC  9201 9FFF                     000021FF  4041          MVI   SUBTEST,X'01'
                                                  4042 *
                                                  4043 **       First, make sure we start clean!
                                                  4044 *
000007C0  98AD 9E5C                     0000205C  4045          LM    R10,R13,CLCL256
000007C4  D2FF A000 C000      00000000  00000000  4046          MVC   0(256,R10),0(R12)          (forces full comparison)
                                                  4047 *
                                                  4048 **       Next, time the overhead...
                                                  4049 *
000007CA  5850 93A0                     000015A0  4050          L     R5,NUMLOOPS
000007CE  B205 93A8                     000015A8  4051          STCK  BEGCLOCK
000007D2  0560                                    4052          BALR  R6,0
000007D4  98AD 9E5C                     0000205C  4053          LM    R10,R13,CLCL256
000007D8  98AD 9E5C                     0000205C  4054          LM    R10,R13,CLCL256
                                                  4055 *        .........ETC.........
                                                  4056          PRINT OFF
                                                  4153          PRINT ON
0000095C  98AD 9E5C                     0000205C  4154          LM    R10,R13,CLCL256
00000960  98AD 9E5C                     0000205C  4155          LM    R10,R13,CLCL256
00000964  0656                                    4156          BCTR  R5,R6
00000966  B205 93B0                     000015B0  4157          STCK  ENDCLOCK
0000096A  45F0 915C                     0000135C  4158          BAL   R15,CALCDUR
0000096E  D207 93C0 93B8      000015C0  000015B8  4159          MVC   OVERHEAD,DURATION
                                                  4160 *
                                                  4161 **       Now do the actual timing run...
                                                  4162 *
00000974  5850 93A0                     000015A0  4163          L     R5,NUMLOOPS
00000978  B205 93A8                     000015A8  4164          STCK  BEGCLOCK
0000097C  0560                                    4165          BALR  R6,0
0000097E  98AD 9E5C                     0000205C  4166          LM    R10,R13,CLCL256
00000982  0FAC                                    4167          CLCL  R10,R12
00000984  98AD 9E5C                     0000205C  4168          LM    R10,R13,CLCL256
00000988  0FAC                                    4169          CLCL  R10,R12
                                                  4170 *        .........ETC.........
                                                  4171          PRINT OFF
                                                  4366          PRINT ON
00000BD0  98AD 9E5C                     0000205C  4367          LM    R10,R13,CLCL256
00000BD4  0FAC                                    4368          CLCL  R10,R12
00000BD6  0656                                    4369          BCTR  R5,R6
00000BD8  B205 93B0                     000015B0  4370          STCK  ENDCLOCK
                                                  4371 *
00000BDC  D204 9409 9381      00001609  00001581  4372          MVC   PRTLINE+33(5),=CL5'CLCL'
00000BE2  45F0 9082                     00001282  4373          BAL   R15,RPTSPEED
00000BE6  07FE                                    4374          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   4376 ********************************************************************************
                                                   4377 *        TEST93                  Time MVCIN instruction  (speed test)
                                                   4378 ********************************************************************************

00000BE8  91FF 9FFD                     000021FD  4380 TEST93   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
00000BEC  078E                                    4381          BZR   R14              No, skip timing tests

00000BEE  9293 9FFE                     000021FE  4383          MVI   TESTNUM,X'93'
00000BF2  9201 9FFF                     000021FF  4384          MVI   SUBTEST,X'01'
                                                   4385 *
                                                   4386 **       First, make sure we start clean!
                                                   4387 *
00000BF6  98AD 94B8                     000016B8  4388          LM    R10,R13,INV256
00000BFA  D2FF D000 94F8      00000000  000016F8  4389          MVC   0(256,R13),MVCININ     (doesn't really matter, but...)
                                                   4390 *
                                                   4391 **       Next, time the overhead...
                                                   4392 *
00000C00  5850 93A0                     000015A0  4393          L     R5,NUMLOOPS
00000C04  B205 93A8                     000015A8  4394          STCK  BEGCLOCK
00000C08  0560                                    4395          BALR  R6,0
00000C0A  0656                                    4396          BCTR  R5,R6
00000C0C  B205 93B0                     000015B0  4397          STCK  ENDCLOCK
00000C10  45F0 915C                     0000135C  4398          BAL   R15,CALCDUR
00000C14  D207 93C0 93B8      000015C0  000015B8  4399          MVC   OVERHEAD,DURATION
                                                   4400 *
                                                   4401 **       Now do the actual timing run...
                                                   4402 *
00000C1A  5850 93A0                     000015A0  4403          L     R5,NUMLOOPS
00000C1E  B205 93A8                     000015A8  4404          STCK  BEGCLOCK
00000C22  0560                                    4405          BALR  R6,0
00000C24  E8FF A000 B000      00000000  00000000  4406          MVCIN 0(256,R10),0(R11)
00000C2A  E8FF A000 B000      00000000  00000000  4407          MVCIN 0(256,R10),0(R11)
00000C30  E8FF A000 B000      00000000  00000000  4408          MVCIN 0(256,R10),0(R11)
                                                   4409 *        .........ETC.........
                                                   4410          PRINT OFF
                                                   4505          PRINT ON
00000E6A  E8FF A000 B000      00000000  00000000  4506          MVCIN 0(256,R10),0(R11)
00000E70  E8FF A000 B000      00000000  00000000  4507          MVCIN 0(256,R10),0(R11)
00000E76  E8FF A000 B000      00000000  00000000  4508          MVCIN 0(256,R10),0(R11)
00000E7C  0656                                    4509          BCTR  R5,R6
00000E7E  B205 93B0                     000015B0  4510          STCK  ENDCLOCK
                                                   4511 *
00000E82  D204 9409 9386      00001609  00001586  4512          MVC   PRTLINE+33(5),=CL5'MVCIN'
00000E88  45F0 9082                     00001282  4513          BAL   R15,RPTSPEED
00000E8C  07FE                                    4514          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4516 ********************************************************************************
                                                  4517 *        TEST94                  Time TRT instruction  (speed test)
                                                  4518 ********************************************************************************

00000E8E  91FF 9FFD                     000021FD  4520 TEST94   TM    TIMEOPT,X'FF'    Is timing tests option enabled?
00000E92  078E                                    4521          BZR   R14              No, skip timing tests

00000E94  9294 9FFE                     000021FE  4523          MVI   TESTNUM,X'94'
00000E98  9201 9FFF                     000021FF  4524          MVI   SUBTEST,X'01'
                                                  4525 *
                                                  4526 **       First, make sure we start clean!
                                                  4527 *
00000E9C  58A0 935C                     0000155C  4528          L     R10,=A(00+(5*K64))
00000EA0  D2FF A000 983C      00000000  00001A3C  4529          MVC   0(256,R10),TRTOP10
00000EA6  58C0 9360                     00001560  4530          L     R12,=A(MB+(5*K64))
00000EAA  D2FF C000 9B3C      00000000  00001D3C  4531          MVC   0(256,R12),TRTOP20     (no stop = full op1 processing)
                                                  4532 *
                                                  4533 **       Next, time the overhead...
                                                  4534 *
00000EB0  5850 93A0                     000015A0  4535          L     R5,NUMLOOPS
00000EB4  B205 93A8                     000015A8  4536          STCK  BEGCLOCK
00000EB8  0560                                    4537          BALR  R6,0
00000EBA  0656                                    4538          BCTR  R5,R6
00000EBC  B205 93B0                     000015B0  4539          STCK  ENDCLOCK
00000EC0  45F0 915C                     0000135C  4540          BAL   R15,CALCDUR
00000EC4  D207 93C0 93B8      000015C0  000015B8  4541          MVC   OVERHEAD,DURATION
                                                  4542 *
                                                  4543 **       Now do the actual timing run...
                                                  4544 *
00000ECA  5850 93A0                     000015A0  4545          L     R5,NUMLOOPS
00000ECE  B205 93A8                     000015A8  4546          STCK  BEGCLOCK
00000ED2  0560                                    4547          BALR  R6,0
00000ED4  DDFF A000 C000      00000000  00000000  4548          TRT   0(256,R10),0(R12)
00000EDA  DDFF A000 C000      00000000  00000000  4549          TRT   0(256,R10),0(R12)
00000EE0  DDFF A000 C000      00000000  00000000  4550          TRT   0(256,R10),0(R12)
                                                  4551 *        .........ETC.........
                                                  4552          PRINT OFF
                                                  4647          PRINT ON
0000111A  DDFF A000 C000      00000000  00000000  4648          TRT   0(256,R10),0(R12)
00001120  DDFF A000 C000      00000000  00000000  4649          TRT   0(256,R10),0(R12)
00001126  DDFF A000 C000      00000000  00000000  4650          TRT   0(256,R10),0(R12)
0000112C  0656                                    4651          BCTR  R5,R6
0000112E  B205 93B0                     000015B0  4652          STCK  ENDCLOCK
                                                  4653 *
00001132  D204 9409 938B      00001609  0000158B  4654          MVC   PRTLINE+33(5),=CL5'TRT'
00001138  45F0 9082                     00001282  4655          BAL   R15,RPTSPEED
0000113C  07FE                                    4656          BR    R14
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4658 ********************************************************************************
                                          4659 *        TEST95                    Test CLCL page fault handling
                                          4660 ********************************************************************************

0000113E  9295 9FFE                     000021FE  4662 TEST95   MVI   TESTNUM,X'95'
00001142  9200 9FFF                     000021FF  4663          MVI   SUBTEST,X'00'
                                          4664 *
                                          4665 **       First, make sure we start clean!
                                          4666 *
00001146  98AD 9ECC                     000020CC  4667          LM    R10,R13,CLCLPF     Retrieve CLCL PF test parameters
0000114A  0EAC                                    4668          MVCL  R10,R12            (forces full comparison)
                                          4669 *
                                          4670 **       Initialize Dynamic Address Translation tables...
                                          4671 *
0000114C  58A0 9364                     00001564  4672          L     R10,=A(SEGTABLS)   Segment Tables Origin
00001150  41B0 0020                     00000020  4673          LA    R11,NUMPGTBS       Number of Segment Table Entries
00001154  58C0 9368                     00001568  4674          L     R12,=A(PAGETABS)   Page Tables Origin
00001158  1F00                                    4675          SLR   R0,R0              First Page Frame Address
0000115A  4160 0004                     00000004  4676          LA    R6,4               Size of one table entry
0000115E  5870 936C                     0000156C  4677          L     R7,=A(PAGE)        Size of one Page Frame

00001162  50C0 A000                     00000000  4679 SEGLOOP  ST    R12,0(,R10)        Seg Table Entry <= Page Table Origin
00001166  960F A003                     00000003  4680          OI    3(R10),X'0F'       Seg Table Entry <= Page Table Length
0000116A  1EA6                                    4681          ALR   R10,R6             Bump to next Segment Table Entry

0000116C  41D0 0010                     00000010  4683          LA    R13,16             Page Table Entries per Page Table

00001170  5000 C000                     00000000  4684 PAGELOOP ST    R0,0(,R12)         Page Table Entry = Page Frame Address
00001174  1E07                                    4685          ALR   R0,R7              Increment to next Page Frame Address
00001176  1EC6                                    4686          ALR   R12,R6             Bump to next Page Table Entry
00001178  46D0 2F70                     00001170  4687          BCT   R13,PAGELOOP       Loop until Page table is complete

0000117C  46B0 2F62                     00001162  4689          BCT   R11,SEGLOOP        Loop until all Segment Table Entries built
                                          4690 *
                                          4691 **       Update desired page table entry to cause page fault
                                          4692 *
00001180  98AD 9ECC                     000020CC  4693          LM    R10,R13,CLCLPF     Retrieve CLCL PF test parameters
00001184  185A                                    4694          LR    R5,R10             R5 --> Operand-1
00001186  5E50 9370                     00001570  4695          AL    R5,=A(PFPGBYTS)    R5 --> Operand-1 Page Fault address
0000118A  1865                                    4696          LR    R6,R5              R6 --> Address where PF should occur
0000118C  8850 000C                     0000000C  4697          SRL   R5,12              R5 = Page Frame number
00001190  8950 0002                     00000002  4698          SLL   R5,2               R5 = Page Table Entry number

00001194  9204 9FFF                     000021FF  4700          MVI   SUBTEST,X'04'
00001198  5E50 9368                     00001568  4701          AL    R5,=A(PAGETABS)    R5 --> Page Table Entry
0000119C  9604 5002                     00000002  4702          OI    2(R5),X'04'        Mark this page invalid
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4704 *
                                                  4705 **       Install program check routine to catch the page fault
                                                  4706 *
000011A0  9202 9FFF                      000021FF  4707          MVI   SUBTEST,X'02'
000011A4  D207 2FE0 0068      000011E0   00000068  4708          MVC   SVPGMNEW,PGMNPSW   Save original Program New PSW
000011AA  4100 2FF0                      000011F0  4709          LA    R0,MYPGMNEW        Point to temporary Pgm New routine
000011AE  5000 006C                      0000006C  4710          ST    R0,PGMNPSW+4       Point Program New PSW to our routine
000011B2  9208 0069                      00000069  4711          MVI   PGMNPSW+1,X'08'    Make it a non-disabled-wait PSW!
                                                  4712 *
                                                  4713 **       Run the test: should cause a page fault
                                                  4714 *
000011B6  920F 9FFF                      000021FF  4715          MVI   SUBTEST,X'0F'
000011BA  B700 9398                      00001598  4716          LCTL  R0,R0,CRLREG0      Switch to DAT mode
000011BE  B711 939C                      0000159C  4717          LCTL  R1,R1,CTLREG1      Switch to DAT mode
000011C2  8200 2FE8                      000011E8  4718          LPSW  DATONPSW           Switch to DAT mode
000011C6  4700 2FC6                      000011C6  4719 BEGDATON NOP   *                (pad)
000011CA  4700 2FCA                      000011CA  4720          NOP   *                (pad)
000011CE  B20D 0000                      00000000  4721          PTLB  ,                  Purge Translation Lookaside Buffer
000011D2  0FAC                                     4722 PFINSADR CLCL  R10,R12            Page Fault should occur on this instr
000011D4  07000700                                 4723          CNOP  0,8                    (align to doubleword)
000011D8  00000000 00000000                        4724 LOGICERR DC    D'0'                 We should never reach here!
000011E0  00000000 00000000                        4725 SVPGMNEW DC    D'0'                 Original Program New PSW
000011E8  04080000 000011C6                        4726 DATONPSW DC    XL4'04080000',A(BEGDATON)  Enable DAT PSW
                                                  4727 *
                                                  4728 **       Temporary Program New routine:
                                                  4729 **       Restore original Program New PSW
                                                  4730 *
000011F0  D207 0068 2FE0      00000068   000011E0  4731 MYPGMNEW MVC   PGMNPSW,SVPGMNEW   Restore original Program New PSW
                                                  4732 *
                                                  4733 **       Verify Program Check occurred on expected instruction
                                                  4734 *
000011F6  9268 9FFF                      000021FF  4735          MVI   SUBTEST,X'68'
000011FA  D503 9374 002C      00001574   0000002C  4736          CLC   =A(PFINSADR),PGMOPSW+4   Program Check where expected?
00001200  4770 9268                      00001468  4737          BNE   FAILTEST                 No?! Something is VERY WRONG!
                                                  4738 *
                                                  4739 **       Verify Program Check was indeed a page fault
                                                  4740 *
00001204  9211 9FFF                      000021FF  4741          MVI   SUBTEST,X'11'
00001208  9511 008F                      0000008F  4742          CLI   PGMICODE+1,X'11'   Verify it's a Page Fault interrupt
0000120C  4770 9268                      00001468  4743          BNE   FAILTEST           If not then something is VERY WRONG!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4745 *
                                          4746 **       Verify Page Fault occurred on expected Page
                                          4747 *
00001210  9205 9FFF                 000021FF  4748          MVI   SUBTEST,X'05'
00001214  5800 0090                 00000090  4749          L     R0,PGMTRX           Get where Page Fault occurred
00001218  8800 000C                 0000000C  4750          SRL   R0,12
0000121C  8900 000C                 0000000C  4751          SLL   R0,12

00001220  8860 000C                 0000000C  4753          SRL   R6,12               Where Page Fault is expected
00001224  8960 000C                 0000000C  4754          SLL   R6,12

00001228  1506                              4756          CLR   R0,R6               Page Fault occur on expected Page?
0000122A  4770 9268                 00001468  4757          BNE   FAILTEST            No? Then something is very wrong!
                                          4758 *
                                          4759 **       Verify CLCL instruction registers were updated as expected
                                          4760 *
0000122E  9206 9FFF                 000021FF  4761          MVI   SUBTEST,X'06'
00001232  55A0 9ECC                 000020CC  4762          CL    R10,CLCLPF          (op1 greater than starting value?)
00001236  47D0 9268                 00001468  4763          BNH   FAILTEST
0000123A  55C0 9ED4                 000020D4  4764          CL    R12,CLCLPF+4+4      (op2 greater than starting value?)
0000123E  47D0 9268                 00001468  4765          BNH   FAILTEST

00001242  9207 9FFF                 000021FF  4767          MVI   SUBTEST,X'07'
00001246  15BD                              4768          CLR   R11,R13             (same remaining lengths?)
00001248  4770 9268                 00001468  4769          BNE   FAILTEST
0000124C  55B0 9ED0                 000020D0  4770          CL    R11,CLCLPF+4        (op1 len less than starting value?)
00001250  47B0 9268                 00001468  4771          BNL   FAILTEST
00001254  55D0 9ED8                 000020D8  4772          CL    R13,CLCLPF+4+4+4    (op2 len less than starting value?)
00001258  47B0 9268                 00001468  4773          BNL   FAILTEST

0000125C  9208 9FFF                 000021FF  4775          MVI   SUBTEST,X'08'
00001260  55A0 9F6C                 0000216C  4776          CL    R10,ECLCLPF         (stop before end?)
00001264  47B0 9268                 00001468  4777          BNL   FAILTEST

00001268  9209 9FFF                 000021FF  4779          MVI   SUBTEST,X'09'
0000126C  15A6                              4780          CLR   R10,R6              (stop at or before expected page?)
0000126E  4720 9268                 00001468  4781          BH    FAILTEST

00001272  9210 9FFF                 000021FF  4783          MVI   SUBTEST,X'10'
00001276  187A                              4784          LR    R7,R10              (op1 stopped address)
00001278  1E7B                              4785          ALR   R7,R11              (add remaining length)
0000127A  1576                              4786          CLR   R7,R6               (would remainder reach PF page?)
0000127C  47D0 9268                 00001468  4787          BNH   FAILTEST

00001280  07FE                              4789          BR    R14                 Success!
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          4791 ********************************************************************************
                                          4792 *        RPTSPEED                  Report instruction speed
                                          4793 ********************************************************************************

00001282  50F0 9158                  00001358  4795 RPTSPEED ST    R15,RPTSAVE        Save return address
00001286  45F0 915C                  0000135C  4796          BAL   R15,CALCDUR        Calculate duration
                                          4797 *
0000128A  4150 93C0                  000015C0  4798          LA    R5,OVERHEAD        Subtract overhead
0000128E  4160 93B8                  000015B8  4799          LA    R6,DURATION        From raw timing
00001292  4170 93B8                  000015B8  4800          LA    R7,DURATION        Yielding true instruction timing
00001296  45F0 91B0                  000013B0  4801          BAL   R15,SUBDWORD       Do it
                                          4802 *
0000129A  98CD 93B8                  000015B8  4803          LM    R12,R13,DURATION   Convert to...
0000129E  8CC0 000C                  0000000C  4804          SRDL  R12,12             ... microseconds
                                          4805 *
000012A2  4EC0 93C8                  000015C8  4806          CVD   R12,TICKSAAA       convert HIGH part to decimal
000012A6  4ED0 93D0                  000015D0  4807          CVD   R13,TICKSBBB       convert LOW  part to decimal
                                          4808 *
000012AA  F877 93D8 93C8      000015D8  000015C8  4809          ZAP   TICKSTOT,TICKSAAA            Calculate...
000012B0  FC75 93D8 9390      000015D8  00001590  4810          MP    TICKSTOT,=P'4294967296'      ...decimal...
000012B6  FA77 93D8 93D0      000015D8  000015D0  4811          AP    TICKSTOT,TICKSBBB            ...microseconds
                                          4812 *
000012BC  D20B 9413 942C      00001613  0000162C  4813          MVC   PRTLINE+43(L'EDIT),EDIT          (edit into...
000012C2  DE0B 9413 93DB      00001613  000015DB  4814          ED    PRTLINE+43(L'EDIT),TICKSTOT+3     ...print line)
```

```
                                          4816          RAWIO 4,FAIL=FAILIO      Print elapsed time on console
000012C8  9200 300E                  0000000E  4817+         MVI   IOCBSC,X'00'           Clear SC information
000012CC  D201 300A 3006      0000000A  00000006  4818+         MVC   IOCBST,IOCBZERO       Clear accumulated status
000012D2  5810 3000                  00000000  4819+         L     1,IOCBDID             Remember the device ID with which I am working
                                          4820+* Initiate Subchannel-based input/output operation
000012D6  5840 3018                  00000018  4821+         $L    4,IOCBORB             Locate the ORB for the channel subsystem
000012DA  B233 4000                  00000000  4822+         SSCH  0(4)                  Initiate the I/O operation
000012DE  A774 00BD                  00001458  4823+         $BC   B'0111',FAILIO        ..Start function failed, report/handle the error
000012E2  5840 3020                  00000020  4824+         $L    4,IOCBIRB             Locate the IRB storage area
000012E6                      00000000          4825+         USING IRB,4                 Make it addressable

                                          4827+* Wait for I/O operation to present status via an interruption
000012E6                                  4828+IOWT0007 DS    0H  Wait for I/O to complete
000012E6  D207 9108 0078      00001308  00000078  4830+         MVC   IOS0008(8),120(0)               Save Input/Output new PSW
000012EC  D207 0078 9100      00000078  00001300  4831+         MVC   120(8,0),ION0008              Establish Input/Ouput new PSW
000012F2  8200 90F8                  000012F8  4832+         $LPSW WPSW0008                      Wait for event
000012F8  020A0000 00000000                    4833+WPSW0008 PSW   2,0,2,0,0                     Wait for event
00001300  00082000 00001310                    4834+ION0008  PSW   0,0,0,32,IRST0008,24               I/O New PSW: cc==2
00001308  00000000 00000000                    4835+IOS0008  DC    XL8'00'
                                          4836+* Handle input/output interruption
00001310                                       4837+IRST0008 DS    0H
00001310  D207 0078 9108      00000078  00001308  4838+         MVC   120(8,0),IOS0008            Restore input/output new PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                         4839+* Process the interruption...
                                         4840+* Validate interruption is for the expected subchannel
00001316  5510 00B8                 000000B8  4841+         CL    1,IOSSID              Is this the device for which I am waiting?
0000131A  A774 FFE6                 000012E6  4842+         $BNE  IOWT0007              ..No, continue waiting for it
                                         4843+* Accumulate interruption information from IRB
0000131E  B235 4000                 00000000  4844+         TSCH  0(4)                  Retrive interrupt information
00001322  A744 FFE2                 000012E6  4845+         $BC   B'0100',IOWT0007      CC1 (not status pending), wait for it to arriv
00001326  A714 0099                 00001458  4846+         $BC   B'0001',FAILIO        CC3 (not operational), an error then
                                         4847+*                                       CC0 (status was pending), accumulate the status
0000132A  D600 300E 4003  0000000E  00000003  4848+         OC    IOCBSC,IRBSCSW+SCSW2  Accumulate status control
00001330  D601 300A 4008  0000000A  00000008  4849+         OC    IOCBST,IRBSCSW+SCSWUS Accumulate device and channel status
00001336  9104 300E                 0000000E  4850+         TM    IOCBSC,SCSWSPRI       Primary subchannel status?
0000133A  A7E4 FFD6                 000012E6  4851+         $BNO  IOWT0007              ..No, wait for primary status
0000133E  D203 3010 4004  00000010  00000004  4852+         MVC   IOCBSCCW,IRBSCSW+SCSWCCW  CCW address
00001344  D201 3016 400A  00000016  0000000A  4853+         MVC   IOCBRCNT,IRBSCSW+SCSWCNT  Residual count
                                         4854+* Test for errors as specified in the IOCB
0000134A  910C 300A                 0000000A  4855+         TM    IOCBUS,CSWCE+CSWDE    Channel end and device end both accumulated?
0000134E  A7E4 0085                 00001458  4856+         $BNO  FAILIO                Hunh? No CE and DE but do have primary status!
                                         4857+* Input/Output operation successful


00001352  58F0 9158                 00001358  4859          L     R15,RPTSAVE           Restore return address
00001356  07FF                               4860          BR    R15                   Return to caller

00001358  00000000                           4862 RPTSAVE  DC    F'0'                  R15 save area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                          4864 ********************************************************************************
                                          4865 *        CALCDUR                    Calculate DURATION
                                          4866 ********************************************************************************

0000135C  50F0 91A0                       000013A0  4868 CALCDUR  ST    R15,CALCRET        Save return address
00001360  9057 91A4                       000013A4  4869          STM   R5,R7,CALCWORK     Save work registers
                                          4870 *
00001364  9867 93A8                       000015A8  4871          LM    R6,R7,BEGCLOCK     Remove CPU number from clock value
00001368  8C60 0006                       00000006  4872          SRDL  R6,6                       "
0000136C  8D60 0006                       00000006  4873          SLDL  R6,6                       "
00001370  9067 93A8                       000015A8  4874          STM   R6,R7,BEGCLOCK             "
                                          4875 *
00001374  9867 93B0                       000015B0  4876          LM    R6,R7,ENDCLOCK     Remove CPU number from clock value
00001378  8C60 0006                       00000006  4877          SRDL  R6,6                       "
0000137C  8D60 0006                       00000006  4878          SLDL  R6,6                       "
00001380  9067 93B0                       000015B0  4879          STM   R6,R7,ENDCLOCK             "
                                          4880 *
00001384  4150 93A8                       000015A8  4881          LA    R5,BEGCLOCK        Starting time
00001388  4160 93B0                       000015B0  4882          LA    R6,ENDCLOCK        Ending time
0000138C  4170 93B8                       000015B8  4883          LA    R7,DURATION        Difference
00001390  45F0 91B0                       000013B0  4884          BAL   R15,SUBDWORD       Calculate duration
                                          4885 *
00001394  9857 91A4                       000013A4  4886          LM    R5,R7,CALCWORK     Restore work registers
00001398  58F0 91A0                       000013A0  4887          L     R15,CALCRET        Restore return address
0000139C  07FF                            4888          BR    R15                Return to caller

000013A0  00000000                        4890 CALCRET  DC    F'0'               R15 save area
000013A4  00000000 00000000               4891 CALCWORK DC    3F'0'              R5-R7 save area



                                          4893 ********************************************************************************
                                          4894 *        SUBDWORD                   Subtract two doublewords
                                          4895 *        R5 --> subtrahend, R6 --> minuend, R7 --> result
                                          4896 ********************************************************************************

000013B0  90AD 91D8                       000013D8  4898 SUBDWORD STM   R10,R13,SUBDWSAV   Save registers
                                          4899 *
000013B4  98AB 5000                       00000000  4900          LM    R10,R11,0(R5)      Subtrahend  (value to subtract)
000013B8  98CD 6000                       00000000  4901          LM    R12,R13,0(R6)      Minuend     (what to subtract FROM)
000013BC  1FDB                            4902          SLR   R13,R11            Subtract LOW part
000013BE  47B0 91C6                       000013C6  4903          BNM   *+4+4              (branch if no borrow)
000013C2  5FC0 9378                       00001578  4904          SL    R12,=F'1'          (otherwise do borrow)
000013C6  1FCA                            4905          SLR   R12,R10            Subtract HIGH part
000013C8  90CD 7000                       00000000  4906          STM   R12,R13,0(R7)      Store results
                                          4907 *
000013CC  98AD 91D8                       000013D8  4908          LM    R10,R13,SUBDWSAV   Restore registers
000013D0  07FF                            4909          BR    R15                Return to caller

000013D8  00000000 00000000               4911 SUBDWSAV DC    2D'0'              R10-R13 save area
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                    4913 ********************************************************************************
                                                    4914 *        Program Initialization
                                                    4915 ********************************************************************************

000013E8                                            4917 INIT     DS     0H               Program Initialization

000013E8  4130 92D8                    000014D8     4919          LA     R3,IOCB_009      Point to IOCB
000013EC  5880 3018                    00000018     4920          L      R8,IOCBORB       Point to ORB

000013F0  45F0 9278                    00001478     4922          BAL    R15,IOINIT       Initialize the CPU for I/O operations
000013F4  45F0 9286                    00001486     4923          BAL    R15,ENADEV       Enable our device making ready for use
000013F8  07FE                                      4924          BR     R14              Return to caller




                                                    4926 ********************************************************************************
                                                    4927 *        Verify CLCL ending register values
                                                    4928 * R10-R12 = actual ending values, R5 --> expected ending values
                                                    4929 ********************************************************************************

000013FA  90AD 9F7C                    0000217C     4931 ENDCLCL  STM    R10,R13,CLCLEND      Save actual ending register values
000013FE  D50F 5000 9F7C      00000000 0000217C     4932          CLC    0(4*4,R5),CLCLEND    Do they have the expected values?
00001404  4770 9268                    00001468     4933          BNE    FAILTEST             If not then the test has failed
00001408  07FF                                      4934          BR     R15                  Otherwise return to caller




                                                    4936 ********************************************************************************
                                                    4937 *        MVCINTST
                                                    4938 ********************************************************************************

0000140A  98AD 5000                    00000000     4940 MVCINTST LM     R10,R13,0(R5)        a(dst),a(src+(len-1)),a(len-1),a(src)
0000140E  4160 95F7                    000017F7     4941          LA     R6,MVCININ+256-1     Point to end of source
00001412  1F6C                                      4942          SLR    R6,R12               Backup by length amount
00001414  44C0 9226                    00001426     4943          EX     R12,MVCINSRC         Initialize source data
00001418  44C0 922C                    0000142C     4944          EX     R12,MVCINMVC         Do the Move Inverse
0000141C  44C0 9232                    00001432     4945          EX     R12,MVCINCLC         Compare with expected results
00001420  4770 9268                    00001468     4946          BNE    FAILTEST             FAIL if not the expected value
00001424  07FF                                      4947          BR     R15                  Otherwise return to caller


00001426  D200 D000 6000      00000000  00000000  4949 MVCINSRC MVC    0(0,R13),0(R6)       Executed Instruction
0000142C  E800 A000 B000      00000000  00000000  4950 MVCINMVC MVCIN  0(0,R10),0(R11)      Executed Instruction
00001432  D500 A000 95F8      00000000  000017F8  4951 MVCINCLC CLC    0(0,R10),MVCINOUT    Executed Instruction
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  4953 ********************************************************************************
                                                  4954 *        Normal completion or Abnormal termination PSWs
                                                  4955 ********************************************************************************
                                                  4957 EOJ      DWAITEND LOAD=YES          Normal completion
00001438                                          4959+EOJ      DS    0H
00001438  8200 9240                   00001440    4960+         LPSW  DWAT0010
00001440  000A0000 00000000                       4961+DWAT0010 PSW   0,0,2,0,X'000000'
                                                  4963 FAILDEV  DWAIT LOAD=YES,CODE=01     ENADEV failed
00001448                                          4964+FAILDEV  DS    0H
00001448  8200 9250                   00001450    4965+         LPSW  DWAT0011
00001450  000A0000 00010001                       4966+DWAT0011 PSW   0,0,2,0,X'010001'
                                                  4968 FAILIO   DWAIT LOAD=YES,CODE=02     RAWIO failed
00001458                                          4969+FAILIO   DS    0H
00001458  8200 9260                   00001460    4970+         LPSW  DWAT0012
00001460  000A0000 00010002                       4971+DWAT0012 PSW   0,0,2,0,X'010002'
                                                  4973 FAILTEST DWAIT LOAD=YES,CODE=BAD    Abnormal termination
00001468                                          4974+FAILTEST DS    0H
00001468  8200 9270                   00001470    4975+         LPSW  DWAT0013
00001470  000A0000 00010BAD                       4976+DWAT0013 PSW   0,0,2,0,X'010BAD'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    4978 ************************************************************************
                                                    4979 *        Initialize the CPU for I/O operations
                                                    4980 ************************************************************************

                                                    4982 IOINIT   IOINIT ,
00001478  B766 9280                       00001480  4983+IOINIT   LCTL  6,6,IOMK0014       Enable subchannel subclasses for interruptions
0000147C  47F0 9284                       00001484  4984+         B     IOMK0014+4
00001480                                            4985+IOMK0014 DS    0F
00001480  FF000000                                  4986+         DC    XL4'FF000000'         All subchannel subclasses enabled

00001484  07FF                                      4988          BR    R15                   Return to caller

                                                    4990 ************************************************************************
                                                    4991 *        Enable the device, making it ready for use
                                                    4992 ************************************************************************

                                                    4994 ENADEV   ENADEV ENAOKAY,FAILDEV,REG=4
00001486  5810 92CC                       000014CC  4995+ENADEV   L     1,FIND0015
0000148A  5840 3028                       00000028  4996+         $L    4,IOCBSIB             Locate where the SCHIB is to be stored
0000148E                        00000000            4997+         USING SCHIB,4
0000148E                                            4998+FINL0015 DS    0H   Retrieve Subchannel Information Block for desired device number
0000148E  B234 4000                       00000000  4999+         STSCH 0(4)                  Store the SCHIB for first subchannel
00001492  A774 FFDB                       00001448  5000+         $BC   B'0111',FAILDEV       Subchannel does not exist and device number not found
00001496  9101 4005                       00000005  5001+         TM    PMCW1_8,PMCWV         Is the subchannel device number valid?
0000149A  A784 0011                       000014BC  5002+         $BZ   FINN0015              ..No, check the next subchannel
0000149E  D501 4006 3004        00000006  00000004  5003+         CLC   PMCWDNUM,IOCBDEV      Is this the device number being sought?
000014A4  A774 000C                       000014BC  5004+         $BNE  FINN0015              ..No, check the next subchannel
                                                    5005+* Subchannel found!
000014A8  5010 3000                       00000000  5006+         ST    1,IOCBDID             Remember the subchannel so I/O can be done to it.
000014AC  9680 4005                       00000005  5007+         OI    PMCW1_8,PMCWE         Make sure it is enabled so I/O requests accepted
000014B0  B232 4000                       00000000  5008+         MSCH  0(4)                  Enable the subchannel to the channel sub-system
000014B4  A784 0010                       000014D4  5009+         $BC   B'1000',ENAOKAY       CC0 (SCHIB updated), device is ready.
000014B8  A7F4 FFC8                       00001448  5010+         $B    FAILDEV               CC1,CC2,CC3 (SCHIB update failed), quit
000014BC                                            5011+FINN0015 DS    0H  Advance to next subchannel
000014BC  4110 1001                       00000001  5012+         LA    1,1(0,1)              Advance to next subchannel
000014C0  5510 92D0                       000014D0  5013+         CL    1,FINM0015            Beyond maximum subchannel
000014C4  A7D4 FFE5                       0000148E  5014+         $BNH  FINL0015              ..No, examine the next subchannel
000014C8  A724 FFC0                       00001448  5015+         $BH   FAILDEV               ..Yes, failed to enable the device
000014CC                                            5016+         DROP  4                     Forget SCHIB addressing
000014CC  00010000                                  5017+FIND0015 DC    A(X'00010000')        First subchannel subsystem ID
000014D0  0001FFFF                                  5018+FINM0015 DC    A(X'0001FFFF')        Last subchannel subsystem ID

000014D4  07FF                                      5020 ENAOKAY  BR    R15                   Return to caller
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                  5022 ********************************************************************************
                                                  5023 *         Structure used by RAWIO identifying
                                                  5024 *         the device and operation being performed
                                                  5025 ********************************************************************************


                                                  5027 IOCB_009 IOCB  X'009',CCW=CONPGM
000014D8  00000000                                5028+IOCB_009 DC    A(0)            +0 Device Identifier (supplied by ENADEV macro)
000014DC  0009                                    5029+         DC    AL2(X'009')     +4 Device address or device number
000014DE  0000                                    5030+         DC    H'0'            +6 Must be zeros
000014E0  D3                                      5031+         DC    AL1(X'D3')      +8 Default detected unit errors
000014E1  3F                                      5032+         DC    AL1(X'3F')      +9 Default detected channel errors
000014E2  0000                                    5033+         DC    HL2'0'          +10 Accumulated unit and channel errors
000014E4  0000                                    5034+         DC    HL2'0'          +12 Tested unit and channel status
000014E6  00                                      5035+         DC    XL1'00'         +14 Accumulated subchannel status control from SCSW
000014E7  80                                      5036+         DC    XL1'80'         +15 Default unsoliticed wait condition
000014E8  00000000                                5037+         DC    F'0'            +16 I/O status CCW address
000014EC  00000000                                5038+         DC    F'0'            +20 residual count
000014F0  00001548                                5039+         DC    A(IORB0016)     +24  Address where ORB is located
000014F4  00000000                                5040+         DC    A(0)            +28  reserved
000014F8  00001508                                5041+         DC    A(IIRB0016)     +32 Address where IRB stored
000014FC  00000000                                5042+         DC    A(0)            +36 reserved
00001500  00001508                                5043+         DC    A(IIRB0016)     +40 Address where SCHIB stored
00001504  00000000                                5044+         DC    A(0)            +44 reserved
00001508  00000000 00000000                       5045+IIRB0016 DC    16F'0'              Embedded shared IRB and SCHIB area
00001548                                          5047+IORB0016 DS    0XL12
00001548  00000000                                5048+         DC    A(0)            Word 0 - Interruption Parameter
0000154C  00                                      5049+         DC    AL1((0)*16+B'0000')  Word 1, bits 0-7
0000154D  80                                      5050+         DC    BL1'10000000'   Word 1, bits 8-15
0000154E  FF                                      5051+         DC    AL1(255)        Word 1, bits 16-23
0000154F  00                                      5052+         DC    BL1'00000000'    Word 1, bits 24-31
00001550  000015E0                                5053+         DC    AL4(CONPGM)     Word 2 - CCW address
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5055 ********************************************************************************
                                                    5056 *        Working Storage
                                                    5057 ********************************************************************************


00001554                                            5059          LTORG ,                 Literals pool
00001554  AABBCCDD                                  5060                =A(REG2PATT)
00001558  00000000                                  5061                =F'0'
0000155C  00050000                                  5062                =A(00+(5*K64))
00001560  00150000                                  5063                =A(MB+(5*K64))
00001564  00003000                                  5064                =A(SEGTABLS)
00001568  00003080                                  5065                =A(PAGETABS)
0000156C  00001000                                  5066                =A(PAGE)
00001570  00005000                                  5067                =A(PFPGBYTS)
00001574  000011D2                                  5068                =A(PFINSADR)
00001578  00000001                                  5069                =F'1'
0000157C  C3D3C340 40                               5070                =CL5'CLC'
00001581  C3D3C3D3 40                               5071                =CL5'CLCL'
00001586  D4E5C3C9 D5                               5072                =CL5'MVCIN'
0000158B  E3D9E340 40                               5073                =CL5'TRT'
00001590  04294967 296C                             5074                =P'4294967296'

                            00000400  00000001  5076 K        EQU   1024              One KB
                            00001000  00000001  5077 PAGE     EQU   (4*K)             Size of one page
                            00010000  00000001  5078 K64      EQU   (64*K)            64 KB
                            00100000  00000001  5079 MB       EQU   (K*K)              1 MB

                            000021FE  00000001  5081 TESTADDR EQU   (2*PAGE+X'200'-2)  Where test/subtest numbers will go
                            000021FD  00000001  5082 TIMEADDR EQU   (TESTADDR-1)       Address of timing tests option flag

                            00200000  00000001  5084 MAINSIZE EQU   (2*MB)                    Minimum required storage size
                            00000020  00000001  5085 NUMPGTBS EQU   ((MAINSIZE+K64-1)/K64)   Number of Page Tables needed
                            00000002  00000001  5086 NUMSEGTB EQU   ((NUMPGTBS*4)/(16*4))    Number of Segment Tables
                            00003000  00000001  5087 SEGTABLS EQU   (3*PAGE)                  Segment Tables Origin
                            00003080  00000001  5088 PAGETABS EQU   (SEGTABLS+(NUMPGTBS*4))  Page Tables Origin
00001598  00B00060                                  5089 CRLREG0  DC    0A(0),XL4'00B00060'      Control Register 0
0000159C  00003002                                  5090 CTLREG1  DC    A(SEGTABLS+NUMSEGTB)     Control Register 1

000015A0  00002710                                  5092 NUMLOOPS DC    F'10000'         10,000 * 100 = 1,000,000

000015A8  BBBBBBBB BBBBBBBB                         5094 BEGCLOCK DC    0D'0',8X'BB'     Begin
000015B0  EEEEEEEE EEEEEEEE                         5095 ENDCLOCK DC    0D'0',8X'EE'     End
000015B8  DDDDDDDD DDDDDDDD                         5096 DURATION DC    0D'0',8X'DD'     Diff
000015C0  FFFFFFFF FFFFFFFF                         5097 OVERHEAD DC    0D'0',8X'FF'     Overhead

000015C8  00000000 0000000C                         5099 TICKSAAA DC    PL8'0'           Clock ticks high part
000015D0  00000000 0000000C                         5100 TICKSBBB DC    PL8'0'           Clock ticks low part
000015D8  00000000 0000000C                         5101 TICKSTOT DC    PL8'0'           Total clock ticks

000015E0  09000044 000015E8                         5103 CONPGM   CCW1  X'09',PRTLINE,0,L'PRTLINE
000015E8  40404040 40404040                         5104 PRTLINE  DC    C'         1,000,000 iterations of XXXXX took 999,999,999 microseconds'
0000162C  40202020 6B202020                         5105 EDIT     DC    X'402020206B2020206B202120'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   5107 ************************************************************************
                                                   5108 *        CLC Test Parameters:   A(operand-1),A(operand-2)
                                                   5109 ************************************************************************

00001638  00010000 00110000                        5111 CLC1     DC    A(1*K64),A(MB+(1*K64))                          both equal
00001640  00010000 00110000                        5112 CLC2     DC    A(1*K64),A(MB+(1*K64))                          both equal
00001648  0000FFF4 0010FFDE                        5113 CLCBOTH  DC    A(1*K64-12),A(MB+(1*K64)-34)                    both equal
00001650  00010000 0010FFDE                        5114 CLCOP2   DC    A(1*K64),A(MB+(1*K64)-34)                       both equal

00001658  00020000 00120000                        5116 CLC4     DC    A(2*K64),A(MB+(2*K64))                            op1 HIGH
00001660  00030000 00130000                        5117 CLC8     DC    A(3*K64),A(MB+(3*K64))                            op1 LOW!
00001668  00040000 00140000                        5118 CLC256   DC    A(4*K64),A(MB+(4*K64))                            op1 HIGH
00001670  0004FFF4 00150000                        5119 CLCOP1   DC    A(5*K64-12),A(MB+(5*K64))                         op1 HIGH


                                                   5121 ************************************************************************
                                                   5122 *        MVCIN Test Parameters
                                                   5123 ************************************************************************
                                                   5124          PRINT DATA
00001678  00010000 00110000                        5125 INV1     DC    A(1*K64),A(MB+(1*K64)+1-1),A(1-1),A(MB+(1*K64))
00001680  00000000 00110000
00001688  00020000 00120001                        5126 INV2     DC    A(2*K64),A(MB+(2*K64)+2-1),A(2-1),A(MB+(2*K64))
00001690  00000001 00120000
00001698  00030000 00130003                        5127 INV4     DC    A(3*K64),A(MB+(3*K64)+4-1),A(4-1),A(MB+(3*K64))
000016A0  00000003 00130000
000016A8  00040000 00140007                        5128 INV8     DC    A(4*K64),A(MB+(4*K64)+8-1),A(8-1),A(MB+(4*K64))
000016B0  00000007 00140000
000016B8  00050000 001500FF                        5129 INV256   DC    A(5*K64),A(MB+(5*K64)+256-1),A(256-1),A(MB+(5*K64))
000016C0  000000FF 00150000

000016C8  0005FFF4 001600DD                        5131 INVBOTH  DC    A(6*K64-12),A(MB+(6*K64)-34+256-1),A(256-1),A(MB+(6*K64)-34)
000016D0  000000FF 0015FFDE
000016D8  0006FFF4 001700FF                        5132 INVOP1   DC    A(7*K64-12),A(MB+(7*K64)+256-1),A(256-1),A(MB+(7*K64))
000016E0  000000FF 00170000
000016E8  00080000 001800DD                        5133 INVOP2   DC    A(8*K64),A(MB+(8*K64)-34+256-1),A(256-1),A(MB+(8*K64)-34)
000016F0  000000FF 0017FFDE
                                                   5134          PRINT NODATA
000016F8                                           5135 MVCININ  DC    0XL256'00'
000016F8  00010203 04050607                        5136          DC    XL16'000102030405060708090A0B0C0D0E0F'
00001708  10111213 14151617                        5137          DC    XL16'101112131415161718191A1B1C1D1E1F'
00001718  20212223 24252627                        5138          DC    XL16'202122232425262728292A2B2C2D2E2F'
00001728  30313233 34353637                        5139          DC    XL16'303132333435363738393A3B3C3D3E3F'
                                                   5140          PRINT OFF
                                                   5153          PRINT ON
000017F8                                           5154 MVCINOUT DC    0XL256'00'
000017F8  FFFEFDFC FBFAF9F8                        5155          DC    XL16'FFFEFDFCFBFAF9F8F7F6F5F4F3F2F1F0'
00001808  EFEEEDEC EBEAE9E8                        5156          DC    XL16'EFEEEDECEBEAE9E8E7E6E5E4E3E2E1E0'
00001818  DFDEDDDC DBDAD9D8                        5157          DC    XL16'DFDEDDDCDBDAD9D8D7D6D5D4D3D2D1D0'
00001828  CFCECDCC CBCAC9C8                        5158          DC    XL16'CFCECDCCCBCAC9C8C7C6C5C4C3C2C1C0'
                                                   5159          PRINT OFF
                                                   5172          PRINT ON
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    5174 ********************************************************************************
                                                    5175 *        TRTTEST DSECT
                                                    5176 ********************************************************************************


                                                    5178 TRTTEST  DSECT ,


00000000  00000000                                  5180 OP1DATA  DC    A(0)           Pointer to Operand-1 data
00000004  00000000                                  5181 OP1LEN   DC    F'0'           How much data is there - 1
00000008  00000000                                  5182 OP1WHERE DC    A(0)           Where Operand-1 data should be placed


0000000C  00000000                                  5184 OP2DATA  DC    A(0)           Pointer to Operand-2 data
00000010  00000000                                  5185 OP2LEN   DC    F'0'           How much data is there - 1
00000014  00000000                                  5186 OP2WHERE DC    A(0)           Where Operand-2 data should be placed


00000018  00000000                                  5188 EXLEN    DC    F'0'           Operand-1 test length (EX instruction)
0000001C  00000000                                  5189 FAILMASK DC    A(0)           Failure Branch on Condition mask


00000020  00000000 00000000                         5191 ENDREGS  DC    A(0),XL4'00'   Ending R1/R2 register values


                    00000028  00000001  5193 TRTNEXT  EQU   *              Start of next table entry...


                                                    5195 REG2PATT EQU   X'AABBCCDD'    Register 2 starting/ending CC0 value
                    000000DD  00000001  5196 REG2LOW  EQU         X'DD'    (last byte above)


                    00000000  00003000  5198 CLCLetal CSECT ,
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   5200 ********************************************************************************
                                                   5201 *        TRT Testing Control tables   (ref: TRTDSECT)
                                                   5202 ********************************************************************************
                                                   5203          PRINT DATA
000018F8                                           5204 TRTCTL   DC    0A(0)    start of table




000018F8  00001A3C 00000000                        5206 TRT1     DC    A(TRTOP10),A(001-1),A(00+(1*K64))
00001900  00010000
00001904  00001D3C 000000FF                        5207          DC    A(TRTOP20),A(256-1),A(MB+(1*K64))
0000190C  00110000
00001910  00000000 00000007                        5208          DC               A(001-1),A(7) CC0
00001918  00000000 AABBCCDD                        5209          DC                        A(0),A(REG2PATT)



00001920  00001A3C 00000000                        5211 TRT2     DC    A(TRTOP10),A(002-2),A(00+(2*K64))
00001928  00020000
0000192C  00001D3C 000000FF                        5212          DC    A(TRTOP20),A(256-1),A(MB+(2*K64))
00001934  00120000
00001938  00000001 00000007                        5213          DC               A(002-1),A(7) CC0
00001940  00000000 AABBCCDD                        5214          DC                        A(0),A(REG2PATT)



00001948  00001A3C 00000003                        5216 TRT4     DC    A(TRTOP10),A(004-1),A(00+(3*K64))
00001950  00030000
00001954  00001D3C 000000FF                        5217          DC    A(TRTOP20),A(256-1),A(MB+(3*K64))
0000195C  00130000
00001960  00000003 00000007                        5218          DC               A(004-1),A(7) CC0
00001968  00000000 AABBCCDD                        5219          DC                        A(0),A(REG2PATT)



00001970  00001A3C 00000007                        5221 TRT8     DC    A(TRTOP10),A(008-1),A(00+(4*K64))
00001978  00040000
0000197C  00001D3C 000000FF                        5222          DC    A(TRTOP20),A(256-1),A(MB+(4*K64))
00001984  00140000
00001988  00000007 00000007                        5223          DC               A(008-1),A(7) CC0
00001990  00000000 AABBCCDD                        5224          DC                        A(0),A(REG2PATT)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001998  00001A3C 000000FF                        5226 TRT256   DC    A(TRTOP10),A(256-1),A(00+(5*K64))
000019A0  00050000
000019A4  00001D3C 000000FF                        5227          DC    A(TRTOP20),A(256-1),A(MB+(5*K64))
000019AC  00150000
000019B0  000000FF 00000007                        5228          DC               A(256-1),A(7) CC0
000019B8  00000000 AABBCCDD                        5229          DC                    A(0),A(REG2PATT)



000019C0  00001B3C 000000FF                        5231 TRTBTH   DC    A(TRTOP111),A(256-1),A(00+(6*K64)-12)  both cross page
000019C8  0005FFF4
000019CC  00001E3C 000000FF                        5232          DC    A(TRTOP211),A(256-1),A(MB+(6*K64)-34)  both cross page
000019D4  0015FFDE
000019D8  000000FF 0000000B                        5233          DC                A(256-1),A(11) CC1 = stop, scan incomplete
000019E0  00060005 AABBCC11                        5234          DC                     A(00+(6*K64)-12+X'11'),A(REG2PATT-REG2LOW+X'11')



000019E8  00001C3C 000000FF                        5236 TRTOP1   DC    A(TRTOP1F0),A(256-1),A(00+(7*K64)-12)  only op1 crosses
000019F0  0006FFF4
000019F4  00001F3C 000000FF                        5237          DC    A(TRTOP2F0),A(256-1),A(MB+(7*K64))
000019FC  00170000
00001A00  000000FF 0000000D                        5238          DC                A(256-1),A(13) CC2 = stopped on last byte
00001A08  000700F3 AABBCCF0                        5239          DC                     A(00+(7*K64)-12+255),A(REG2PATT-REG2LOW+X'F0')



00001A10  00001B3C 000000FF                        5241 TRTOP2   DC    A(TRTOP111),A(256-1),A(00+(8*K64))
00001A18  00080000
00001A1C  00001E3C 000000FF                        5242          DC    A(TRTOP211),A(256-1),A(MB+(8*K64)-34)  only op2 crosses
00001A24  0017FFDE
00001A28  000000FF 0000000B                        5243          DC                A(256-1),A(11) CC1 = stop, scan incomplete
00001A30  00080011 AABBCC11                        5244          DC                     A(00+(8*K64)+X'11'),A(REG2PATT-REG2LOW+X'11')



00001A38  00000000                                 5246          DC    A(0)     end of table
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   5248 ********************************************************************************
                                                   5249 *        TRT op1 scan data...
                                                   5250 ********************************************************************************

00001A3C  78125634 78125634                        5252 TRTOP10  DC    64XL4'78125634'    (CC0)
00001A44  78125634 78125634
00001A4C  78125634 78125634
00001A54  78125634 78125634
00001A5C  78125634 78125634
00001A64  78125634 78125634
00001A6C  78125634 78125634
00001A74  78125634 78125634
00001A7C  78125634 78125634
00001A84  78125634 78125634
00001A8C  78125634 78125634
00001A94  78125634 78125634
00001A9C  78125634 78125634
00001AA4  78125634 78125634
00001AAC  78125634 78125634
00001AB4  78125634 78125634
00001ABC  78125634 78125634
00001AC4  78125634 78125634
00001ACC  78125634 78125634
00001AD4  78125634 78125634
00001ADC  78125634 78125634
00001AE4  78125634 78125634
00001AEC  78125634 78125634
00001AF4  78125634 78125634
00001AFC  78125634 78125634
00001B04  78125634 78125634
00001B0C  78125634 78125634
00001B14  78125634 78125634
00001B1C  78125634 78125634
00001B24  78125634 78125634
00001B2C  78125634 78125634
00001B34  78125634 78125634

00001B3C  78125634 78125634                        5254 TRTOP111 DC    04XL4'78125634',X'00110000',59XL4'78125634'    (CC1)
00001B44  78125634 78125634
00001B4C  00110000 78125634
00001B54  78125634 78125634
00001B5C  78125634 78125634
00001B64  78125634 78125634
00001B6C  78125634 78125634
00001B74  78125634 78125634
00001B7C  78125634 78125634
00001B84  78125634 78125634
00001B8C  78125634 78125634
00001B94  78125634 78125634
00001B9C  78125634 78125634
00001BA4  78125634 78125634
00001BAC  78125634 78125634
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001BB4  78125634 78125634
00001BBC  78125634 78125634
00001BC4  78125634 78125634
00001BCC  78125634 78125634
00001BD4  78125634 78125634
00001BDC  78125634 78125634
00001BE4  78125634 78125634
00001BEC  78125634 78125634
00001BF4  78125634 78125634
00001BFC  78125634 78125634
00001C04  78125634 78125634
00001C0C  78125634 78125634
00001C14  78125634 78125634
00001C1C  78125634 78125634
00001C24  78125634 78125634
00001C2C  78125634 78125634
00001C34  78125634 78125634

00001C3C  78125634 78125634                    5256 TRTOP1F0 DC    63XL4'78125634',X'000000F0'    (CC2)
00001C44  78125634 78125634
00001C4C  78125634 78125634
00001C54  78125634 78125634
00001C5C  78125634 78125634
00001C64  78125634 78125634
00001C6C  78125634 78125634
00001C74  78125634 78125634
00001C7C  78125634 78125634
00001C84  78125634 78125634
00001C8C  78125634 78125634
00001C94  78125634 78125634
00001C9C  78125634 78125634
00001CA4  78125634 78125634
00001CAC  78125634 78125634
00001CB4  78125634 78125634
00001CBC  78125634 78125634
00001CC4  78125634 78125634
00001CCC  78125634 78125634
00001CD4  78125634 78125634
00001CDC  78125634 78125634
00001CE4  78125634 78125634
00001CEC  78125634 78125634
00001CF4  78125634 78125634
00001CFC  78125634 78125634
00001D04  78125634 78125634
00001D0C  78125634 78125634
00001D14  78125634 78125634
00001D1C  78125634 78125634
00001D24  78125634 78125634
00001D2C  78125634 78125634
00001D34  78125634 000000F0
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   5258 ********************************************************************************
                                                   5259 *        TRT op2 stop tables...
                                                   5260 ********************************************************************************

00001D3C  00000000 00000000                        5262 TRTOP20  DC    256X'00'     no stop
00001D44  00000000 00000000
00001D4C  00000000 00000000
00001D54  00000000 00000000
00001D5C  00000000 00000000
00001D64  00000000 00000000
00001D6C  00000000 00000000
00001D74  00000000 00000000
00001D7C  00000000 00000000
00001D84  00000000 00000000
00001D8C  00000000 00000000
00001D94  00000000 00000000
00001D9C  00000000 00000000
00001DA4  00000000 00000000
00001DAC  00000000 00000000
00001DB4  00000000 00000000
00001DBC  00000000 00000000
00001DC4  00000000 00000000
00001DCC  00000000 00000000
00001DD4  00000000 00000000
00001DDC  00000000 00000000
00001DE4  00000000 00000000
00001DEC  00000000 00000000
00001DF4  00000000 00000000
00001DFC  00000000 00000000
00001E04  00000000 00000000
00001E0C  00000000 00000000
00001E14  00000000 00000000
00001E1C  00000000 00000000
00001E24  00000000 00000000
00001E2C  00000000 00000000
00001E34  00000000 00000000

00001E3C  00000000 00000000                        5264 TRTOP211 DC    17X'00',X'11',238X'00'     stop on X'11'
00001E44  00000000 00000000
00001E4C  00110000 00000000
00001E54  00000000 00000000
00001E5C  00000000 00000000
00001E64  00000000 00000000
00001E6C  00000000 00000000
00001E74  00000000 00000000
00001E7C  00000000 00000000
00001E84  00000000 00000000
00001E8C  00000000 00000000
00001E94  00000000 00000000
00001E9C  00000000 00000000
00001EA4  00000000 00000000
00001EAC  00000000 00000000
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00001EB4  00000000 00000000
00001EBC  00000000 00000000
00001EC4  00000000 00000000
00001ECC  00000000 00000000
00001ED4  00000000 00000000
00001EDC  00000000 00000000
00001EE4  00000000 00000000
00001EEC  00000000 00000000
00001EF4  00000000 00000000
00001EFC  00000000 00000000
00001F04  00000000 00000000
00001F0C  00000000 00000000
00001F14  00000000 00000000
00001F1C  00000000 00000000
00001F24  00000000 00000000
00001F2C  00000000 00000000
00001F34  00000000 00000000

00001F3C  00000000 00000000                    5266 TRTOP2F0 DC    240X'00',X'F0',15X'00'     stop on X'F0'
00001F44  00000000 00000000
00001F4C  00000000 00000000
00001F54  00000000 00000000
00001F5C  00000000 00000000
00001F64  00000000 00000000
00001F6C  00000000 00000000
00001F74  00000000 00000000
00001F7C  00000000 00000000
00001F84  00000000 00000000
00001F8C  00000000 00000000
00001F94  00000000 00000000
00001F9C  00000000 00000000
00001FA4  00000000 00000000
00001FAC  00000000 00000000
00001FB4  00000000 00000000
00001FBC  00000000 00000000
00001FC4  00000000 00000000
00001FCC  00000000 00000000
00001FD4  00000000 00000000
00001FDC  00000000 00000000
00001FE4  00000000 00000000
00001FEC  00000000 00000000
00001FF4  00000000 00000000
00001FFC  00000000 00000000
00002004  00000000 00000000
0000200C  00000000 00000000
00002014  00000000 00000000
0000201C  00000000 00000000
00002024  00000000 00000000
0000202C  F0000000 00000000
00002034  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   5268 ********************************************************************
                                                   5269 *        CLCL Test Parameters
                                                   5270 ********************************************************************

0000203C  00060000 00000001                        5272 CLCL1    DC    A(6*K64),A(1),A(MB+(6*K64)),A(1)             both equal
00002044  00160000 00000001

0000204C  00060000 00000002                        5274 CLCL2    DC    A(6*K64),A(2),A(MB+(6*K64)),A(2)             both equal
00002054  00160000 00000002

0000205C  00060000 00000100                        5276 CLCL256  DC    A(6*K64),A(256),A(MB+(6*K64)),A(256)         both equal
00002064  00160000 00000100

0000206C  00060000 00000400                        5278 CLCL1K   DC    A(6*K64),A(K),A(MB+(6*K64)),A(K)             both equal
00002074  00160000 00000400

0000207C  0005FFF4 00010000                        5280 CLCLBOTH DC    A(6*K64-12),A(K64),A(MB+(6*K64)-34),A(K64)   both equal
00002084  0015FFDE 00010000

0000208C  00060000 00001000                        5282 CLCLOP2  DC    A(6*K64),A(PAGE),A(MB+(6*K64)-34),A(K64)     both equal
00002094  0015FFDE 00010000

0000209C  00070000 00000004                        5284 CLCL4    DC    A(7*K64),A(4),A(MB+(7*K64)),A(4)              op1 HIGH
000020A4  00170000 00000004

000020AC  00080000 00000008                        5286 CLCL8    DC    A(8*K64),A(8),A(MB+(8*K64)),A(8)              op1 LOW!
000020B4  00180000 00000008

000020BC  0008FFF4 00010000                        5288 CLCLOP1  DC    A(9*K64-12),A(K64),A(MB+(9*K64)),A(PAGE)      op1 HIGH
000020C4  00190000 00001000

000020CC  000A0000 00010000                        5290 CLCLPF   DC    A(10*K64),A(K64),A(MB+(10*K64)),A(K64)      page fault
000020D4  001A0000 00010000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    5292 ************************************************************************
                                                    5293 *        CLCL Expected Ending Register Values
                                                    5294 ************************************************************************

000020DC  00060001 00000000                         5296 ECLCL1   DC    A(6*K64+1),A(0),A(MB+(6*K64)+1),A(0)         both equal
000020E4  00160001 00000000

000020EC  00060002 00000000                         5298 ECLCL2   DC    A(6*K64+2),A(0),A(MB+(6*K64)+2),A(0)         both equal
000020F4  00160002 00000000

000020FC  00060100 00000000                         5300 ECLCL256 DC    A(6*K64+256),A(0),A(MB+(6*K64)+256),A(0)     both equal
00002104  00160100 00000000

0000210C  00060400 00000000                         5302 ECLCL1K  DC    A(6*K64+K),A(0),A(MB+(6*K64)+K),A(0)         both equal
00002114  00160400 00000000

0000211C  0006FFF4 00000000                         5304 ECLCLBTH DC    A(6*K64-12+K64),A(0),A(MB+(6*K64)-34+K64),A(0) bth equl
00002124  0016FFDE 00000000

0000212C  00061000 00000000                         5306 ECLCLOP2 DC    A(6*K64+PAGE),A(0),A(MB+(6*K64)-34+K64),A(0) both equal
00002134  0016FFDE 00000000

0000213C  00070003 00000001                         5308 ECLCL4   DC    A(7*K64+4-1),A(1),A(MB+(7*K64)+4-1),A(1)       op1 HIGH
00002144  00170003 00000001

0000214C  00080007 00000001                         5310 ECLCL8   DC    A(8*K64+8-1),A(1),A(MB+(8*K64)+8-1),A(1)       op1 LOW!
00002154  00180007 00000001

0000215C  0009FFF3 00000001                         5312 ECLCLOP1 DC    A(9*K64-12+K64-1),A(1),A(MB+(9*K64)+PAGE),A(0) op1 HIGH
00002164  00191000 00000000

0000216C  000B0000 00000000                         5314 ECLCLPF  DC    A(10*K64+K64),A(0),A(MB+(10*K64)+K64),A(0)   page fault
00002174  001B0000 00000000

0000217C  00000000 00000000                         5316 CLCLEND  DC    4F'0'          (actual ending register values)
00002184  00000000 00000000
                            00000005  00000001    5317 PFPAGE   EQU   5              (page the Page Fault should occur on)
                            00005000  00000001    5318 PFPGBYTS EQU   (PFPAGE*PAGE)  (number of bytes into operand-1)
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                  5320 ********************************************************************************
                                                  5321 *        Fixed storage locations
                                                  5322 ********************************************************************************


0000218C                     0000218C  000021FD  5324          ORG   CLCLetal+TIMEADDR      (s/b @ X'21FD')

000021FD  00                                     5326 TIMEOPT  DC    X'00'      Set to non-zero to run timing tests




000021FE                     000021FE  000021FE  5328          ORG   CLCLetal+TESTADDR      (s/b @ X'21FE', X'21FF')

000021FE  00                                     5330 TESTNUM  DC    X'00'      Test number of active test
000021FF  00                                     5331 SUBTEST  DC    X'00'      Active test sub-test number


00002200                     00002200  00003000  5333          ORG   CLCLetal+SEGTABLS      (s/b @ X'3000')
00003000  00                                     5335 DATTABS  DC    X'00'      Segment and Page Tables will go here...
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    5337 ********************************************************************************
                                                    5338 *        IOCB DSECT
                                                    5339 ********************************************************************************

                                                    5341          DSECTS NAME=IOCB
                                                    5343+IOCB     DSECT
                                                    5344+*     Field usage by: CH SC Description (R->program read-only, X->program read/write)
00000000                                            5345+IOCBDID  DS    0F  +0     R  Device Identifier - Subsystem ID for channel subsystem
00000000  0000                                      5346+         DS    H   +0  R      reserved - must be zeros
00000002  0000                                      5347+IOCBDV   DS    H   +2  R      Channel Unit Device address of I/O operation
00000004  0000                                      5348+IOCBDEV  DS    H   +4  X  X   Device address or device number (R after ENADEV)
00000006  0000                                      5349+IOCBZERO DS    H   +6  R  R   Must be zeros
00000008  00                                        5350+IOCBUM   DS    X   +8  X  X   Unit status test mask
00000009  00                                        5351+IOCBCM   DS    X   +9  X  X   Channel status test mask
0000000A                                            5352+IOCBST   DS    0H  +10 X  X   Input/Output unit and channel status accumulation
0000000A  00                                        5353+IOCBUS   DS    X   +10 R  R   Accumulated unit status
0000000B  00                                        5354+IOCBCS   DS    X   +11 R  R   Accumulated channel status
0000000C  00                                        5355+IOCBUT   DS    X   +14 R  R   Used to test unit status
0000000D  00                                        5356+IOCBCT   DS    X   +13 R  R   Used to test channel status
0000000E  00                                        5357+IOCBSC   DS    X   +14    R   Accumulted subchanel status control
0000000F  00                                        5358+IOCBWAIT DS    X   +15 X  X   Recognized unsolicited interruption unit status events
00000010  00000000                                  5359+IOCBSCCW DS    A   +16 R  R   I/O status CCW address
00000014                                            5360+IOCBSCNT DS    0F  +20 R  R   I/O status residual count as a positive full word
00000014  0000                                      5361+         DS    H   +20 R      reserved must be zeros
00000016  0000                                      5362+IOCBRCNT DS    H   +22 R      I/O status residual count as an unsigned halfword
00000018                                            5363+IOCBCAW  DS    0A  +24 X      Channel Address word
00000018  00000000 00000000                         5364+IOCBORB  DS    AD  +24    X   Address of the ORB for channel subsystem I/O
00000020  00000000 00000000                         5365+IOCBIRB  DS    AD  +32    X   Channel subsystem IRB address
00000028  00000000 00000000                         5366+IOCBSIB  DS    AD  +40    X   Channel subsystem SCHIB address
                            00000030  00000001      5367+IOCBL    EQU   *-IOCB  Length of IOCB control block (48) without embedded structures
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  5369 ********************************************************************************
                                                  5370 *        ORB DSECT
                                                  5371 ********************************************************************************

                                                  5373          DSECTS NAME=ORB
                                                  5375+ORB      DSECT
00000000  00000000                                5376+ORBPARM  DC    F'0'     Word 0, bits 0-31

00000004  00                                      5378+ORB1_0   DC    X'00'    Word 1, bits 0-7
                            000000F0  00000001    5379+ORBKEYM  EQU   X'F0'    Word 1, bits 0-3   - Storage Key Mask
                            00000008  00000001    5380+ORBS     EQU   X'08'    Word 1, bit 4      - Suspend Control
                            00000004  00000001    5381+ORBC     EQU   X'04'    Word 1, bit 5      - Streaming Mode Control
                            00000002  00000001    5382+ORBM     EQU   X'02'    Word 1, bit 6      - Modification Control
                            00000001  00000001    5383+ORBY     EQU   X'01'    Word 1, bit 7      - Synchronization Control

00000005  00                                      5385+ORB1_8   DC    X'00'    Word 1, bits 8-15
                            00000080  00000001    5386+ORBF     EQU   X'80'    Word 1, bit 8      - CCW Format-Control
                            00000040  00000001    5387+ORBP     EQU   X'40'    Word 1, bit 9      - Pre-fetch control
                            00000020  00000001    5388+ORBI     EQU   X'20'    Word 1, bit 10     - Initial-status Interruption Control
                            00000010  00000001    5389+ORBA     EQU   X'10'    Word 1, bit 11     - Address Limit Checking Control
                            00000008  00000001    5390+ORBU     EQU   X'08'    Word 1, bit 12     - Suppress-suspended-interruption control
                            00000004  00000001    5391+ORBB     EQU   X'04'    Word 1, bit 13     - Channel-Program-Type Control
                            00000002  00000001    5392+ORBH     EQU   X'02'    Word 1, bit 14     - Format 2-IDAW Control
                            00000001  00000001    5393+ORBT     EQU   X'01'    Word 1, bit 15     - 2K-IDAW control
00000006  00                                      5394+ORBLPM   DC    X'00'    Word 1, bits 16-23 - Logical Path Mask
00000007  00                                      5395+ORRB1_24 DC    X'00'    Word 1, bits 24-31
                            00000080  00000001    5396+ORBL     EQU   X'80'    Word 1, bit 24     - Incorrect Length Suppression Mode
                            0000007F  00000001    5397+ORBRSV3  EQU   X'7F'    Word 1, bits 25-31 - reserved must be zeros
                            00000040  00000001    5398+ORBD     EQU   X'40'    Word 1, bit 25     - MIDAW Addressing Control
                            0000003E  00000001    5399+ORBRSV26 EQU   X'3E'    Word 1, bits 26-30 - reserved must be zeros
                            0000007E  00000001    5400+ORBRSV25 EQU   X'7E'    Word 1, bits 25-30 - reserved must be zeros
                            00000001  00000001    5401+ORBX     EQU   X'01'    Word 1, bit 31     - ORB-extension control

00000008  00000000                                5403+ORBCCW   DC    A(0)     Word 2, bits 1-31  - Channel Program Address
                            00000080  00000001    5404+ORBRSV4  EQU   X'80'    Word 2, bit 0      - reserved must be zero
                            0000000C  00000001    5405+ORBLEN   EQU   *-ORB Length of standard ORB
                                                  5406+* Extended ORB fields
0000000C  00                                      5407+ORBCSS   DC    X'00'    Word 3, bits 0-7   - Channel Subsystem Priority
0000000D  00                                      5408+ORBRSV5  DC    X'00'    Word 3, bits 8-15  - reserved must be zeros
0000000E                                          5409+ORBPGM   DC    0X'00'   Word 3, bits 16-23 - Transport mode reserves for program us
0000000E  00                                      5410+ORBCU    DC    X'00'    Word 3, bits 16-23 - Control Unit Priority
0000000F  00                                      5411+ORBRSV6  DC    X'00'    Word 3, bits 24-31 - reserved must be zeros
00000010  00000000 00000000                       5412+ORBRSV7  DC    XL16'00' Words 4-7          - reserved must be zeros
00000018  00000000 00000000
                            00000020  00000001    5413+ORBXLEN  EQU   *-ORB Length of extended ORB
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  5416 ********************************************************************************
                                                  5417 *        IRB DSECT
                                                  5418 ********************************************************************************

                                                  5420          DSECTS NAME=IRB
                                                  5422+IRB      DSECT Interruption          Response Block
00000000  00000000 00000000                       5423+IRBSCSW  DC    XL12'00' Words 0-2 - Subchannel Status Word (Defined by DSECT SCSW)
00000008  00000000
0000000C  00000000 00000000                       5424+IRBESW   DC    XL20'00' Words 3-7 - Extended Status Word
00000014  00000000 00000000
0000001C  00000000
00000020  00000000 00000000                       5425+IRBECW   DC    XL32'00' Words 8-15 - Extended Control Word
00000028  00000000 00000000
00000030  00000000 00000000
00000038  00000000 00000000
                             00000040  00000001  5426+IRBL     EQU   *-IRB    IRB Length
00000040  00000000 00000000                       5427+IRBEMW   DC    XL32'00' Words 16-23 - Extended Measurement Word
00000048  00000000 00000000
00000050  00000000 00000000
00000058  00000000 00000000
                             00000060  00000001  5428+IRBXL    EQU   *-IRB    Extended IRB Length
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  5431 ********************************************************************************
                                                  5432 *        SCSW DSECT
                                                  5433 ********************************************************************************

                                                  5435          DSECTS NAME=SCSW
                                                  5437+SCSW     DSECT Subchannel          Status Word
00000000  00                                      5438+SCSWFLAG DC    X'00'    Flags
                                 000000F0  00000001 5439+SCSWKEYM EQU   X'F0'    Storage Key Mask of subchannel storage key
                                 00000008  00000001 5440+SCSWSUSC EQU   X'08'    Suspend Control
                                 00000004  00000001 5441+SCSWESWF EQU   X'04'    Extended Status Word Format
                                 00000003  00000001 5442+SCSWDCCM EQU   X'03'    Deferred condiont code mask
                                 00000000  00000001 5443+SCSWDCC0 EQU   X'00'    Normal I/O interruption
                                 00000001  00000001 5444+SCSWDCC1 EQU   X'01'    Deferred condition code is 1
                                 00000003  00000001 5445+SCSWDCC3 EQU   X'03'    Deferred condition code is 3

00000001  00                                      5447+SCSWCTLS DC    X'00'    General Controls
                                 00000080  00000001 5448+SCSWCCWF EQU   X'80'    CCW Format control when ...
                                 00000040  00000001 5449+SCSWCCWP EQU   X'40'    CCW Prefetch Control
                                 00000020  00000001 5450+SCSWISIC EQU   X'20'    Initial-Status-Interruption Control
                                 00000010  00000001 5451+SCSWALKC EQU   X'10'    Address-Limit-Checking Control
                                 00000008  00000001 5452+SCSWSSIC EQU   X'08'    Suppress suspended interruption
                                 00000004  00000001 5453+SCSW0CC  EQU   X'04'    Zero-Condition Code
                                 00000002  00000001 5454+SCSWECWC EQU   X'02'    Extended Control Word control
                                 00000001  00000001 5455+SCSWPNOP EQU   X'01'    Path Not Operational

00000002  00                                      5457+SCSW1    DC    X'00'    Control Byte 1
                                 00000070  00000001 5458+SCSWFM   EQU   X'70'    Functional Control Mask
                                 00000040  00000001 5459+SCSWFS   EQU   X'40'    Function Control - Start Function
                                 00000020  00000001 5460+SCSWFH   EQU   X'20'    Function Control - Halt Function
                                 00000010  00000001 5461+SCSWFC   EQU   X'10'    Function Control - Clear Function
                                 00000008  00000001 5462+SCSWARP  EQU   X'08'    Activity Control - Resume pending
                                 00000004  00000001 5463+SCSWASP  EQU   X'04'    Activity Control - Start pending
                                 00000002  00000001 5464+SCSWAHP  EQU   X'02'    Activity Control - Halt pending
                                 00000001  00000001 5465+SCSWACP  EQU   X'01'    Activity Control - Clear pending
00000003  00                                      5466+SCSW2    DC    X'00'    Control Byte 2
                                 00000080  00000001 5467+SCSWASA  EQU   X'80'    Activity Control - Subchannel Active
                                 00000040  00000001 5468+SCSWADA  EQU   X'40'    Activity Control - Device Active
                                 00000020  00000001 5469+SCSWASUS EQU   X'20'    Activity Control - Suspended
                                 00000010  00000001 5470+SCSWSAS  EQU   X'10'    Status Control   - Alert Status
                                 00000008  00000001 5471+SCSWSINT EQU   X'08'    Status Control   - Intermediate Status
                                 00000004  00000001 5472+SCSWSPRI EQU   X'04'    Status Control   - Primary Status
                                 00000002  00000001 5473+SCSWSSEC EQU   X'02'    Status Control   - Secondary Status
                                 00000001  00000001 5474+SCSWSPEN EQU   X'01'    Status Control   - Status Pending

00000004  00000000                                5476+SCSWCCW  DC    A(0)     CCW Address

00000008  00                                      5478+SCSWUS   DC    X'00'    Unit Status
                                 00000080  00000001 5479+SCSWATTN EQU   X'80'    Attention
                                 00000040  00000001 5480+SCSWSM   EQU   X'40'    Status modifier
                                 00000020  00000001 5481+SCSWCUE  EQU   X'20'    Control-unit end
                                 00000010  00000001 5482+SCSWBUSY EQU   X'10'    Busy
                                 00000008  00000001 5483+SCSWCE   EQU   X'08'    Channel end
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                               00000004  00000001  5484+SCSWDE   EQU   X'04'    Device end
                               00000002  00000001  5485+SCSWUC   EQU   X'02'    Unit check
                               00000001  00000001  5486+SCSWUX   EQU   X'01'    Unit exception

00000009  00                                       5488+SCSWCS   DC    X'00'    Channel Status
                               00000080  00000001  5489+SCSWPCI  EQU   X'80'    Program-controlled interruption
                               00000040  00000001  5490+SCSWIL   EQU   X'40'    Incorrect length
                               00000020  00000001  5491+SCSWPRGM EQU   X'20'    Program check
                               00000010  00000001  5492+SCSWPROT EQU   X'10'    Protection Check
                               00000008  00000001  5493+SCSWCDAT EQU   X'08'    Channel-data check
                               00000004  00000001  5494+SCSWCCTL EQU   X'04'    Channel-control check
                               00000002  00000001  5495+SCSWICTL EQU   X'02'    Interface-control check
                               00000001  00000001  5496+SCSWCHNG EQU   X'01'    Chaining check

0000000A  0000                                     5498+SCSWCNT  DC    H'0'     Residual CCW count
                               0000000C  00000001  5499+SCSWL    EQU   *-SCSW
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  5502 ********************************************************************************
                                                  5503 *        (other DSECTS needed by SATK)
                                                  5504 ********************************************************************************

                                                  5506          DSECTS PRINT=OFF,NAME=(ASA,SCHIB,CCW0,CCW1,CSW)
```

```
                                                  5782          PRINT ON

                                                  5784 ********************************************************************************
                                                  5785 *        Register equates
                                                  5786 ********************************************************************************

                          00000000  00000001  5788 R0        EQU   0
                          00000001  00000001  5789 R1        EQU   1
                          00000002  00000001  5790 R2        EQU   2
                          00000003  00000001  5791 R3        EQU   3
                          00000004  00000001  5792 R4        EQU   4
                          00000005  00000001  5793 R5        EQU   5
                          00000006  00000001  5794 R6        EQU   6
                          00000007  00000001  5795 R7        EQU   7
                          00000008  00000001  5796 R8        EQU   8
                          00000009  00000001  5797 R9        EQU   9
                          0000000A  00000001  5798 R10       EQU   10
                          0000000B  00000001  5799 R11       EQU   11
                          0000000C  00000001  5800 R12       EQU   12
                          0000000D  00000001  5801 R13       EQU   13
                          0000000E  00000001  5802 R14       EQU   14
                          0000000F  00000001  5803 R15       EQU   15
```

```
                                  5805          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
ASA	4	00000000	512	5510	3532
ASBEGIN	U	00000000	1	5511	5516 5558 5594 5603 5621 5628 5634 5638 5642 5648 5665
ASEND	U	00000200	1	5664	5665
ASLENGTH	U	00000200	1	5665	
BCEXTCOD	H	0000001A	2	5528	
BCIOCOD	H	0000003A	2	5536	
BCMCKCOD	H	00000032	2	5534	
BCPGMCOD	H	0000002A	2	5532	
BCSVCCOD	H	00000022	2	5530	
BEGCLOCK	D	000015A8	8	5094	3901 3911 4051 4164 4394 4404 4536 4546 4871 4874 4881
BEGDATON	I	000011C6	4	4719	4726
BEGIN	I	00000200	2	3538	3507 3533 3534 3811 3881
CALCDUR	I	0000135C	4	4868	3905 4158 4398 4540 4796
CALCRET	F	000013A0	4	4890	4868 4887
CALCWORK	F	000013A4	4	4891	4869 4886
CAW	F	00000048	4	5540	
CAWADDR	R	00000049	3	5543	
CAWKEY	X	00000048	1	5541	
CAWSUSP	U	00000008	1	5542	
CCW0	4	00000000	8	5669	5675
CCW0ADDR	R	00000001	3	5671	
CCW0CNT	H	00000006	2	5674	
CCW0CODE	X	00000000	1	5670	
CCW0FLGS	X	00000004	1	5672	
CCW0L	U	00000008	1	5675	
CCW1	4	00000000	8	5687	5692
CCW1ADDR	A	00000004	4	5691	
CCW1CNT	H	00000002	2	5690	
CCW1CODE	X	00000000	1	5688	
CCW1FLGS	X	00000001	1	5689	
CCW1L	U	00000008	1	5692	
CCWCC	U	00000040	1	5679	
CCWCD	U	00000080	1	5678	
CCWIDA	U	00000004	1	5683	
CCWPCI	U	00000008	1	5682	
CCWSKIP	U	00000010	1	5681	
CCWSLI	U	00000020	1	5680	
CCWSUSP	U	00000002	1	5684	
CHANID	F	000000A8	4	5595	
CLC1	A	00001638	4	5111	3596
CLC2	A	00001640	4	5112	3603
CLC256	A	00001668	4	5118	3586 3625
CLC4	A	00001658	4	5116	3584 3610
CLC8	A	00001660	4	5117	3590 3617
CLCBOTH	A	00001648	4	5113	3632
CLCL1	A	0000203C	4	5272	3678
CLCL1K	A	0000206C	4	5278	3717
CLCL2	A	0000204C	4	5274	3687
CLCL256	A	0000205C	4	5276	3895 4045 4053 4054 4057 4058 4059 4060 4061 4062 4063 4064 4065 4066 4067 4068 4069 4070 4071 4072 4073 4074 4075 4076 4077 4078 4079 4080 4081 4082 4083 4084 4085 4086 4087 4088 4089 4090 4091 4092 4093 4094 4095 4096 4097 4098 4099 4100 4101 4102 4103 4104

```
     SYMBOL         TYPE    VALUE      LENGTH    DEFN  REFERENCES

                                                      4105  4106  4107  4108  4109  4110  4111  4112  4113  4114  4115  4116  4117
                                                      4118  4119  4120  4121  4122  4123  4124  4125  4126  4127  4128  4129  4130
                                                      4131  4132  4133  4134  4135  4136  4137  4138  4139  4140  4141  4142  4143
                                                      4144  4145  4146  4147  4148  4149  4150  4151  4152  4154  4155  4166  4168
                                                      4172  4174  4176  4178  4180  4182  4184  4186  4188  4190  4192  4194  4196
                                                      4198  4200  4202  4204  4206  4208  4210  4212  4214  4216  4218  4220  4222
                                                      4224  4226  4228  4230  4232  4234  4236  4238  4240  4242  4244  4246  4248
                                                      4250  4252  4254  4256  4258  4260  4262  4264  4266  4268  4270  4272  4274
                                                      4276  4278  4280  4282  4284  4286  4288  4290  4292  4294  4296  4298  4300
                                                      4302  4304  4306  4308  4310  4312  4314  4316  4318  4320  4322  4324  4326
                                                      4328  4330  4332  4334  4336  4338  4340  4342  4344  4346  4348  4350  4352
                                                      4354  4356  4358  4360  4362  4364  4367
CLCL4                A     0000209C           4  5284  3660  3697
CLCL8                A     000020AC           4  5286  3670  3708
CLCLBOTH             A     0000207C           4  5280  3726
CLCLEND              F     0000217C           4  5316  4931  4932
CLCLETAL             J     00000000       12289  3489  3492  3499  3506  3508  5324  5328  5333
CLCLOP1              A     000020BC           4  5288  3665  3736
CLCLOP2              A     0000208C           4  5282  3745
CLCLPF               A     000020CC           4  5290  4667  4693  4762  4764  4770  4772
CLCOP1               A     00001670           4  5119  3588  3639
CLCOP2               A     00001650           4  5114  3646
CODE                 2     00000000       12289  3489
CONPGM               W     000015E0           8  5103  5053
CPUID                U     0000031B           1  5667
CRLREG0              A     00001598           4  5089  4716
CSW                  F     00000040           8  5539
CSWATTN              U     00000080           1  5709
CSWBUSY              U     00000010           1  5712
CSWCCTL              U     00000004           1  5724
CSWCCW               R     00000001           3  5706
CSWCDAT              U     00000008           1  5723
CSWCE                U     00000008           1  5713  4855
CSWCHNG              U     00000001           1  5726
CSWCNT               H     00000006           2  5728
CSWCS                X     00000005           1  5718
CSWCUE               U     00000020           1  5711
CSWDCC0              U     00000000           1  5702
CSWDCC1              U     00000001           1  5703
CSWDCC3              U     00000003           1  5704
CSWDCCM              U     00000003           1  5701
CSWDE                U     00000004           1  5714  4855
CSWFLAG              X     00000000           1  5696
CSWFMT               4     00000000           8  5695  5729
CSWFMTL              U     00000008           1  5729
CSWICTL              U     00000002           1  5725
CSWIL                U     00000040           1  5720
CSWKEYM              U     000000F0           1  5697
CSWLOG               U     00000004           1  5700
CSWPCI               U     00000080           1  5719
CSWPRGM              U     00000020           1  5721
CSWPROT              U     00000010           1  5722
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
CSWSM	U	00000040	1	5710	
CSWSUSP	U	00000008	1	5699	
CSWUC	U	00000002	1	5715	
CSWUS	X	00000004	1	5708	
CSWUX	U	00000001	1	5716	
CTLREG1	A	0000159C	4	5090	4717
DATONPSW	X	000011E8	4	4726	4718
DATTABS	X	00003000	1	5335	
DURATION	D	000015B8	8	5096	3906 4159 4399 4541 4799 4800 4803 4883
DWAT0010	3	00001440	8	4961	4960
DWAT0011	3	00001450	8	4966	4965
DWAT0012	3	00001460	8	4971	4970
DWAT0013	3	00001470	8	4976	4975
ECLCL1	A	000020DC	4	5296	3681
ECLCL1K	A	0000210C	4	5302	3720
ECLCL2	A	000020EC	4	5298	3690
ECLCL256	A	000020FC	4	5300	
ECLCL4	A	0000213C	4	5308	3700
ECLCL8	A	0000214C	4	5310	3711
ECLCLBTH	A	0000211C	4	5304	3729
ECLCLOP1	A	0000215C	4	5312	3739
ECLCLOP2	A	0000212C	4	5306	3748
ECLCLPF	A	0000216C	4	5314	4776
EDIT	X	0000162C	12	5105	4813 4814
ENADEV	I	00001486	4	4995	4923
ENAOKAY	I	000014D4	2	5020	5009
ENDCLCL	I	000013FA	4	4931	3682 3691 3701 3712 3721 3730 3740 3749
ENDCLOCK	D	000015B0	8	5095	3904 4027 4157 4370 4397 4510 4539 4652 4876 4879 4882
ENDREGS	A	00000020	4	5191	3850
EOJ	H	00001438	2	4959	3566 3574
EXLEN	F	00000018	4	5188	3839
EXTCPUAD	H	00000084	2	5560	
EXTICODE	H	00000086	2	5561	
EXTIPARM	F	00000080	4	5559	
EXTNPSW	F	00000058	8	5549	
EXTOPSW	F	00000018	8	5521	5527
FAILDEV	H	00001448	2	4964	5000 5010 5015
FAILIO	H	00001458	2	4969	4823 4846 4856
FAILMASK	A	0000001C	4	5189	3840
FAILTEST	H	00001468	2	4974	3569 3572 3598 3605 3612 3619 3627 3634 3641 3648 3680 3689 3699
					3710 3719 3728 3738 3747 3865 4737 4743 4757 4763 4765 4769 4771
					4773 4777 4781 4787 4933 4946
FIND0015	A	000014CC	4	5017	4995
FINL0015	H	0000148E	2	4998	5014
FINM0015	A	000014D0	4	5018	5013
FINN0015	H	000014BC	2	5011	5002 5004
IIRB0016	F	00001508	4	5045	5041 5043
IMAGE	1	00000000	12289	0	
INIT	H	000013E8	2	4917	3545
INV1	A	00001678	4	5125	3761
INV2	A	00001688	4	5126	3766
INV256	A	000016B8	4	5129	3781 4388

```
     SYMBOL         TYPE    VALUE      LENGTH    DEFN  REFERENCES

INV4                 A     00001698          4  5127  3771
INV8                 A     000016A8          4  5128  3776
INVBOTH              A     000016C8          4  5131  3786
INVOP1               A     000016D8          4  5132  3791
INVOP2               A     000016E8          4  5133  3796
IOCB                 4     00000000         48  5343  5367  3535
IOCBCAW              A     00000018          4  5363
IOCBCM               X     00000009          1  5351
IOCBCS               X     0000000B          1  5354
IOCBCT               X     0000000D          1  5356
IOCBDEV              H     00000004          2  5348  5003
IOCBDID              F     00000000          4  5345  4819  5006
IOCBDV               H     00000002          2  5347
IOCBIRB              A     00000020          8  5365  4824
IOCBL                U     00000030          1  5367
IOCBORB              A     00000018          8  5364  4821  4920
IOCBRCNT             H     00000016          2  5362  4853
IOCBSC               X     0000000E          1  5357  4817  4848  4850
IOCBSCCW             A     00000010          4  5359  4852
IOCBSCNT             F     00000014          4  5360
IOCBSIB              A     00000028          8  5366  4996
IOCBST               H     0000000A          2  5352  4818  4849
IOCBUM               X     00000008          1  5350
IOCBUS               X     0000000A          1  5353  4855
IOCBUT               X     0000000C          1  5355
IOCBWAIT             X     0000000F          1  5358
IOCBZERO             H     00000006          2  5349  4818
IOCB_009             A     000014D8          4  5028  4919
IOELADDR             F     000000AC          4  5596
IOICODE              H     000000BA          2  5601
IOIID                F     000000C0          4  5606
IOINIT               I     00001478          4  4983  4922
IOIPARM              F     000000BC          4  5605
IOMK0014             F     00001480          4  4985  4983  4984
ION0008              3     00001300          8  4834  4831
IONPSW               F     00000078          8  5553
IOOPSW               F     00000038          8  5525  5535
IORB0016             X     00001548         12  5047  5039
IOS0008              X     00001308          8  4835  4830  4838
IOSSID               F     000000B8          4  5604  4841
IOWT0007             H     000012E6          2  4828  4842  4845  4851
IPLCCW1              F     00000008          8  5513
IPLCCW2              F     00000010          8  5514
IPLPSW               F     00000000          8  5512
IRB                  4     00000000         96  5422  5426  5428  4825
IRBECW               X     00000020         32  5425
IRBEMW               X     00000040         32  5427
IRBESW               X     0000000C         20  5424
IRBL                 U     00000040          1  5426
IRBSCSW              X     00000000         12  5423  4848  4849  4852  4853
IRBXL                U     00000060          1  5428
IRST0008             H     00001310          2  4837  4834
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     SYMBOL         TYPE    VALUE      LENGTH    DEFN  REFERENCES

K                    U     00000400          1  5076  5077  5078  5079  5278  5302
K64                  U     00010000          1  5078  5085  4528  4530  5111  5112  5113  5114  5116  5117  5118  5119  5125  5126
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                                                     5304  5306  5308  5310  5312  5314
LCHANLOG             F     000000B0          4  5597
LOGICERR             D     000011D8          8  4724
MAINSIZE             U     00200000          1  5084  5085
MB                   U     00100000          1  5079  5084  4530  5111  5112  5113  5114  5116  5117  5118  5119  5125  5126  5127
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                                                     5302  5304  5306  5308  5310  5312  5314
MCKLOG               F     00000100          4  5629
MCKNPSW              F     00000070          8  5552
MCKOPSW              F     00000030          8  5524  5533
MEASUREB             X     000000B9          1  5600
MKARCHMD             X     000000A3          1  5588
MKARS                F     00000120          4  5627
MKCLKCMP             F     000000E0          8  5613
MKCPUTIM             F     000000D8          8  5612
MKCRS                F     000001C0          4  5632
MKDMGCOD             F     000000F4          4  5616
MKFAILA              F     000000F8          4  5618
MKFPRS               D     00000160          8  5630
MKICODE              F     000000E8          4  5614
MKLOGOUT             F     00000100          4  5620
MKMODEL              F     000000FC          4  5619
MKXSAA               F     000000D4          4  5611
MONCLS               H     00000094          2  5576
MONCODE              F     0000009C          4  5583
MONNUMBR             X     00000095          1  5578
MPGACCID             X     000000A2          1  5586
MVCINCLC             I     00001432          6  4951  4945
MVCININ              X     000016F8        256  5135  4389  4941
MVCINMVC             I     0000142C          6  4950  4944
MVCINOUT             X     000017F8        256  5154  4951
MVCINSRC             I     00001426          6  4949  4943
MVCINTST             I     0000140A          4  4940  3762  3767  3772  3777  3782  3787  3792  3797
MYPGMNEW             I     000011F0          6  4731  4709
NKGRS                F     00000180          4  5631
NUMLOOPS             F     000015A0          4  5092  3900  3910  4050  4163  4393  4403  4535  4545
NUMPGTBS             U     00000020          1  5085  5086  5088  4673
NUMSEGTB             U     00000002          1  5086  5090
OP1DATA              A     00000000          4  5180  3823
OP1LEN               F     00000004          4  5181  3824
OP1WHERE             A     00000008          4  5182  3820
OP2DATA              A     0000000C          4  5184  3827
OP2LEN               F     00000010          4  5185  3828
OP2WHERE             A     00000014          4  5186  3821
ORB                  4     00000000         32  5375  5405  5413  3536
ORB1_0               X     00000004          1  5378
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
ORB1_8	X	00000005	1	5385	
ORBA	U	00000010	1	5389	
ORBB	U	00000004	1	5391	
ORBC	U	00000004	1	5381	
ORBCCW	A	00000008	4	5403	
ORBCSS	X	0000000C	1	5407	
ORBCU	X	0000000E	1	5410	
ORBD	U	00000040	1	5398	
ORBF	U	00000080	1	5386	
ORBH	U	00000002	1	5392	
ORBI	U	00000020	1	5388	
ORBKEYM	U	000000F0	1	5379	
ORBL	U	00000080	1	5396	
ORBLEN	U	0000000C	1	5405	
ORBLPM	X	00000006	1	5394	
ORBM	U	00000002	1	5382	
ORBP	U	00000040	1	5387	
ORBPARM	F	00000000	4	5376	
ORBPGM	X	0000000E	1	5409	
ORBRSV25	U	0000007E	1	5400	
ORBRSV26	U	0000003E	1	5399	
ORBRSV3	U	0000007F	1	5397	
ORBRSV4	U	00000080	1	5404	
ORBRSV5	X	0000000D	1	5408	
ORBRSV6	X	0000000F	1	5411	
ORBRSV7	X	00000010	16	5412	
ORBS	U	00000008	1	5380	
ORBT	U	00000001	1	5393	
ORBU	U	00000008	1	5390	
ORBX	U	00000001	1	5401	
ORBXLEN	U	00000020	1	5413	
ORBY	U	00000001	1	5383	
ORRB1_24	X	00000007	1	5395	
OVERHEAD	D	000015C0	8	5097	3906 4159 4399 4541 4798
PAGE	U	00001000	1	5077	5081 5087 5318 4677 5282 5288 5306 5312
PAGELOOP	I	00001170	4	4684	4687
PAGETABS	U	00003080	1	5088	4674
PCFETO	A	000000C4	4	5607	
PERACCID	X	000000A1	1	5585	
PERADDR	F	00000098	4	5582	
PERCODE	X	00000096	1	5579	
PERCODMK	U	000000F0	1	5580	
PFINSADR	I	000011D2	2	4722	4736
PFPAGE	U	00000005	1	5317	5318
PFPGBYTS	U	00005000	1	5318	4695
PGMACCID	X	000000A0	1	5584	
PGMDXC	F	00000090	4	5574	
PGMICODE	H	0000008E	2	5573	4742
PGMIID	F	0000008C	4	5569	
PGMIILC	X	0000008D	1	5571	
PGMIILCM	U	0000000C	1	5572	
PGMNPSW	F	00000068	8	5551	4708 4710 4711 4731

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
PGMOPSW	F	00000028	8	5523	5531 4736
PGMTRX	F	00000090	4	5575	4749
PMCW1_0	X	00000004	1	5736	
PMCW1_8	X	00000005	1	5739	5001 5007
PMCWB	U	00000004	1	5771	
PMCWCHP0	X	00000010	1	5760	
PMCWCHP1	X	00000011	1	5761	
PMCWCHP2	X	00000012	1	5762	
PMCWCHP3	X	00000013	1	5763	
PMCWCHP4	X	00000014	1	5764	
PMCWCHP5	X	00000015	1	5765	
PMCWCHP6	X	00000016	1	5766	
PMCWCHP7	X	00000017	1	5767	
PMCWDNUM	H	00000006	2	5751	5003
PMCWE	U	00000080	1	5740	5007
PMCWEXC	X	0000001B	1	5770	
PMCWIP	F	00000000	4	5735	
PMCWISCM	U	00000038	1	5737	
PMCWLM	U	00000060	1	5741	
PMCWLMG	U	00000020	1	5742	
PMCWLML	U	00000040	1	5743	
PMCWLPM	X	00000008	1	5753	
PMCWLPUM	X	0000000A	1	5755	
PMCWM	U	00000004	1	5747	
PMCWMBI	H	0000000C	2	5757	
PMCWMM	U	00000018	1	5744	
PMCWMMC	U	00000008	1	5746	
PMCWMME	U	00000010	1	5745	
PMCWPAM	X	0000000F	1	5759	
PMCWPIM	X	0000000B	1	5756	
PMCWPNOM	X	00000009	1	5754	
PMCWPOM	X	0000000E	1	5758	
PMCWRES1	X	00000018	4	5768	
PMCWRES2	X	00000018	3	5769	
PMCWS	U	00000001	1	5773	
PMCWT	U	00000002	1	5748	
PMCWV	U	00000001	1	5749	5001
PMCWX	U	00000002	1	5772	
PRTLINE	C	000015E8	68	5104	4029 4372 4512 4654 4813 4814 5103
R0	U	00000000	1	5788	3532 4675 4684 4685 4709 4710 4716 4749 4750 4751 4756
R1	U	00000001	1	5789	3807 3834 3845 3853 3866 4717
R10	U	0000000A	1	5798	3678 3679 3687 3688 3697 3698 3708 3709 3717 3718 3726 3727 3736
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
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R11	U	0000000B	1	5799	3840 3841 3846 4406 4407 4408 4411 4412 4413 4414 4415 4416 4417
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R12	U	0000000C	1	5800	3679 3688 3698 3709 3718 3727 3737 3746 3821 3871 3873 3896 3913
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     SYMBOL         TYPE    VALUE      LENGTH    DEFN  REFERENCES

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R14                    U    0000000E           1  5802  3545  3549  3550  3551  3552  3554  3555  3556  3557  3559  3650  3751  3799
                                                      3865  3868  3888  4031  4038  4374  4381  4514  4521  4656  4789  4924
R15                    U    0000000F           1  5803  3682  3691  3701  3712  3721  3730  3740  3749  3762  3767  3772  3777  3782
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R2                     U    00000002           1  5790  3533  3538  3539  3540  3542  3808  3810  3835  3845  3857  3867  3881
R3                     U    00000003           1  5791  3535  4919
R4                     U    00000004           1  5792
R5                     U    00000005           1  5793  3584  3585  3586  3587  3588  3589  3596  3597  3603  3604  3610  3611  3617
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SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
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					3665 3666 3667 3668 3670 3671 3672 3673 3681 3690 3700 3711 3720
					3729 3739 3748 3761 3766 3771 3776 3781 3786 3791 3796 3813 3814
					3860 3861 3879 3900 3903 3910 4026 4050 4156 4163 4369 4393 4396
					4403 4509 4535 4538 4545 4651 4694 4695 4696 4697 4698 4701 4702
					4798 4869 4881 4886 4900 4932 4940
R6	U	00000006	1	5794	3590 3591 3596 3597 3603 3604 3610 3611 3617 3618 3625 3626 3632
					3633 3639 3640 3646 3647 3660 3661 3665 3666 3670 3671 3823 3827
					3850 3853 3870 3871 3902 3903 3912 4026 4052 4156 4165 4369 4395
					4396 4405 4509 4537 4538 4547 4651 4676 4681 4686 4696 4753 4754
					4756 4780 4786 4799 4871 4872 4873 4874 4876 4877 4878 4879 4882
					4901 4941 4942 4949
R7	U	00000007	1	5795	3824 3825 3828 3829 3839 3844 3850 3857 4677 4685 4784 4785 4786
					4800 4869 4871 4874 4876 4879 4883 4886 4906
R8	U	00000008	1	5796	3536 4920
R9	U	00000009	1	5797	3534 3542 3543
REG2LOW	U	000000DD	1	5196	5234 5239 5244
REG2PATT	U	AABBCCDD	1	5195	3835 5209 5214 5219 5224 5229 5234 5239 5244
RPTSAVE	F	00001358	4	4862	4795 4859
RPTSPEED	I	00001282	4	4795	4030 4373 4513 4655
RSTNPSW	F	00000000	8	5517	
RSTOPSW	F	00000008	8	5518	
SAVER1	F	000004C4	4	3876	3807 3866
SAVETRT	D	000004C8	8	3877	3845
SCANOUT	X	00000080	1	5555	5556
SCANOUTL	U	00000000	1	5556	
SCHIB	4	00000000	52	5732	5779 4997
SCHIBL	U	00000034	1	5779	
SCHMBA	A	00000028	8	5777	
SCHMDA1	X	00000030	4	5778	
SCHMDA3	X	00000028	12	5776	
SCHPMCW	X	00000000	28	5734	
SCHSCSW	X	0000001C	12	5775	
SCSW	4	00000000	12	5437	5499
SCSW0CC	U	00000004	1	5453	
SCSW1	X	00000002	1	5457	
SCSW2	X	00000003	1	5466	4848
SCSWACP	U	00000001	1	5465	
SCSWADA	U	00000040	1	5468	
SCSWAHP	U	00000002	1	5464	
SCSWALKC	U	00000010	1	5451	
SCSWARP	U	00000008	1	5462	
SCSWASA	U	00000080	1	5467	
SCSWASP	U	00000004	1	5463	
SCSWASUS	U	00000020	1	5469	
SCSWATTN	U	00000080	1	5479	
SCSWBUSY	U	00000010	1	5482	
SCSWCCTL	U	00000004	1	5494	
SCSWCCW	A	00000004	4	5476	4852
SCSWCCWF	U	00000080	1	5448	
SCSWCCWP	U	00000040	1	5449	
SCSWCDAT	U	00000008	1	5493	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SCSWCE	U	00000008	1	5483	
SCSWCHNG	U	00000001	1	5496	
SCSWCNT	H	0000000A	2	5498	4853
SCSWCS	X	00000009	1	5488	
SCSWCTLS	X	00000001	1	5447	
SCSWCUE	U	00000020	1	5481	
SCSWDCC0	U	00000000	1	5443	
SCSWDCC1	U	00000001	1	5444	
SCSWDCC3	U	00000003	1	5445	
SCSWDCCM	U	00000003	1	5442	
SCSWDE	U	00000004	1	5484	
SCSWECWC	U	00000002	1	5454	
SCSWESWF	U	00000004	1	5441	
SCSWFC	U	00000010	1	5461	
SCSWFH	U	00000020	1	5460	
SCSWFLAG	X	00000000	1	5438	
SCSWFM	U	00000070	1	5458	
SCSWFS	U	00000040	1	5459	
SCSWICTL	U	00000002	1	5495	
SCSWIL	U	00000040	1	5490	
SCSWISIC	U	00000020	1	5450	
SCSWKEYM	U	000000F0	1	5439	
SCSWL	U	0000000C	1	5499	
SCSWPCI	U	00000080	1	5489	
SCSWPNOP	U	00000001	1	5455	
SCSWPRGM	U	00000020	1	5491	
SCSWPROT	U	00000010	1	5492	
SCSWSAS	U	00000010	1	5470	
SCSWSINT	U	00000008	1	5471	
SCSWSM	U	00000040	1	5480	
SCSWSPEN	U	00000001	1	5474	
SCSWSPRI	U	00000004	1	5472	4850
SCSWSSEC	U	00000002	1	5473	
SCSWSSIC	U	00000008	1	5452	
SCSWSUSC	U	00000008	1	5440	
SCSWUC	U	00000002	1	5485	
SCSWUS	X	00000008	1	5478	4849
SCSWUX	U	00000001	1	5486	
SEGLOOP	I	00001162	4	4679	4689
SEGTABLS	U	00003000	1	5087	5088 5333 4672 5090
SSARCHMD	X	000000A3	1	5587	
SSARS	F	00000120	4	5643	
SSCLKCMP	F	000000E0	8	5637	
SSCPUTIM	F	000000D8	8	5636	
SSCRS	F	000001C0	4	5646	
SSFPRS	D	00000160	8	5644	
SSGRS	F	00000180	4	5645	
SSMODEL	F	0000010C	4	5641	
SSPREFIX	F	00000108	4	5640	
SSPSW	F	00000100	8	5639	
SSXSAA	A	000000D4	4	5635	
STFLDATA	F	000000C8	4	5608	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SUBDWORD	I	000013B0	4	4898	4801 4884
SUBDWSAV	D	000013D8	8	4911	4898 4908
SUBTEST	X	000021FF	1	5331	3571 3595 3602 3609 3616 3624 3631 3638 3645 3677 3686 3696 3707 3716 3725 3735 3744 3843 3852 3856 3891 4041 4384 4524 4663 4700 4707 4715 4735 4741 4748 4761 4767 4775 4779 4783
SVCICODE	H	0000008A	2	5567	
SVCIID	F	00000088	4	5563	
SVCIILC	X	00000089	1	5565	
SVCIILCM	U	0000000C	1	5566	
SVCNPSW	F	00000060	8	5550	
SVCOPSW	F	00000020	8	5522	5529
SVPGMNEW	D	000011E0	8	4725	4708 4731
TEST01	I	00000252	4	3580	3549
TEST02	I	00000308	4	3656	3550
TEST03	I	000003E2	4	3757	3551
TEST04	I	00000428	4	3805	3552
TEST91	I	000004D0	4	3887	3554
TEST92	I	000007B2	4	4037	3555
TEST93	I	00000BE8	4	4380	3556
TEST94	I	00000E8E	4	4520	3557
TEST95	I	0000113E	4	4662	3559
TESTADDR	U	000021FE	1	5081	5082 5328
TESTNUM	X	000021FE	1	5330	3568 3580 3656 3757 3805 3890 4040 4383 4523 4662
TICKSAAA	P	000015C8	8	5099	4806 4809
TICKSBBB	P	000015D0	8	5100	4807 4811
TICKSTOT	P	000015D8	8	5101	4809 4810 4811 4814
TIMEADDR	U	000021FD	1	5082	5324
TIMEOPT	X	000021FD	1	5326	3565 3887 4037 4380 4520
TIMER	F	00000050	4	5546	
TRT	I	000004BA	6	3873	3844
TRT1	A	000018F8	4	5206	
TRT2	A	00001920	4	5211	
TRT256	A	00001998	4	5226	
TRT4	A	00001948	4	5216	
TRT8	A	00001970	4	5221	
TRTBC	I	000004C0	4	3874	3846
TRTBTH	A	000019C0	4	5231	
TRTCTL	A	000018F8	4	5204	3813
TRTDONE	I	000004A6	4	3866	3863
TRTFAIL	I	000004A2	4	3865	3854 3858 3874
TRTMVC1	I	000004AE	6	3870	3825
TRTMVC2	I	000004B4	6	3871	3829
TRTNEXT	U	00000028	1	5193	3860
TRTOP1	A	000019E8	4	5236	
TRTOP10	X	00001A3C	4	5252	4529 5206 5211 5216 5221 5226
TRTOP111	X	00001B3C	4	5254	5231 5241
TRTOP1F0	X	00001C3C	4	5256	5236
TRTOP2	A	00001A10	4	5241	
TRTOP20	X	00001D3C	1	5262	4531 5207 5212 5217 5222 5227
TRTOP211	X	00001E3C	1	5264	5232 5242
TRTOP2F0	X	00001F3C	1	5266	5237
TRTTEST	4	00000000	40	5178	3814

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
TST4LOOP	U	00000436	1	3816	3862
TTDES	F	00000054	4	5547	
UA0	F	00000010	8	5519	
UA1	F	0000004C	4	5544	
UA2	F	000000A4	4	5589	
UA3	F	000000B4	4	5598	
UA4	X	000000B8	1	5599	
UA5	X	000000CC	8	5609	
UA6	X	000000EC	8	5615	
UA7	F	00000118	8	5626	
UA8	X	00000180	32	5655	
WPSW0008	3	000012F8	8	4833	4832
ZBRKADDR	A	00000110	8	5625	
ZEMONCNT	F	0000010C	4	5624	
ZEMONCTR	A	00000100	8	5622	
ZEMONSIZ	F	00000108	4	5623	
ZEXTNPSW	X	000001B0	16	5658	
ZEXTOPSW	X	00000130	16	5650	
ZIONPSW	X	000001F0	16	5662	
ZIOOPSW	X	00000170	16	5654	
ZMCKNPSW	X	000001E0	16	5661	
ZMCKOPSW	X	00000160	16	5653	
ZMKFAILA	F	000000F8	8	5617	
ZMONCODE	F	000000B0	8	5592	
ZPGMNPSW	X	000001D0	16	5660	
ZPGMOPSW	X	00000150	16	5652	
ZPGMTRX	F	000000A8	8	5591	
ZRSTNPSW	X	000001A0	16	5657	
ZRSTOPSW	X	00000120	16	5649	
ZSASDISP	U	000011C0	1	5663	
ZSVCNPSW	X	000001C0	16	5659	
ZSVCOPSW	X	00000140	16	5651	
=A(00+(5*K64))	A	0000155C	4	5062	4528
=A(MB+(5*K64))	A	00001560	4	5063	4530
=A(PAGE)	A	0000156C	4	5066	4677
=A(PAGETABS)	A	00001568	4	5065	4674 4701
=A(PFINSADR)	A	00001574	4	5068	4736
=A(PFPGBYTS)	A	00001570	4	5067	4695
=A(REG2PATT)	A	00001554	4	5060	3835
=A(SEGTABLS)	A	00001564	4	5064	4672
=CL5'CLC'	C	0000157C	5	5070	4029
=CL5'CLCL'	C	00001581	5	5071	4372
=CL5'MVCIN'	C	00001586	5	5072	4512
=CL5'TRT'	C	0000158B	5	5073	4654
=F'0'	F	00001558	4	5061	3861
=F'1'	F	00001578	4	5069	4904
=P'4294967296'	P	00001590	6	5074	4810

MACRO	DEFN	REFERENCES					
ANTR	104						
APROB	236						
ARCHIND	396	3426					
ARCHLVL	537	3425					
ASAIPL	663	3505					
ASALOAD	743	3488					
ASAREA	798	5509					
ASAZAREA	983						
CPUWAIT	1066	4829					
DSECTS	1392	5341	5373	5420	5435	5506	
DWAIT	1595	4958	4963	4968	4973		
DWAITEND	1652	4957					
ENADEV	1660	4994					
ESA390	1760						
IOCB	1771	5027					
IOCBDS	1947	5342					
IOFMT	1981	5374	5421	5436	5668	5686	5694	5731
IOINIT	2319	4982					
IOTRFR	2360						
ORB	2408	5046					
POINTER	2597						
PSWFMT	2625						
RAWAIT	2759						
RAWIO	2855	4816					
SIGCPU	3013						
SMMGR	3071						
SMMGRB	3171						
TRAP128	3220						
TRAP64	3197	3490	3493				
TRAPS	3233						
ZARCH	3307						
ZEROH	3319						
ZEROL	3347						
ZEROLH	3375						
ZEROLL	3398						

```
   DESC     SYMBOL    SIZE     POS        ADDR

Entry: 0

Image      IMAGE     12289  0000-3000  0000-3000
  Region   CODE      12289  0000-3000  0000-3000
    CSECT  CLCLETAL  12289  0000-3000  0000-3000
```

```
   STMT                                          FILE NAME

1     c:\Users\Fish\Documents\Visual Studio 2008\Projects\MyProjects\ASMA-0\CLCL-et-al\CLCL-et-al.asm
2     C:\Users\Fish\Documents\Visual Studio 2008\Projects\Hercules\_Git\_Harold\SATK-0\srcasm\satk.mac


** NO ERRORS FOUND **
```