```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                      2 ************************************************************************
                                                      3 *
                                                      4 *Testcase IEEE LOAD ROUNDED
                                                      5 *  Test case capability includes IEEE exceptions, trappable and
                                                      6 *  otherwise.  Test result, FPCR flags, and DXC saved for all tests.
                                                      7 *  Load Rounded does not set the condition code.
                                                      8 *
                                                      9 *
                                                     10 *                        ********************
                                                     11 *                        **   IMPORTANT!   **
                                                     12 *                        ********************
                                                     13 *
                                                     14 *        This test uses the Hercules Diagnose X'008' interface
                                                     15 *        to display messages and thus your .tst runtest script
                                                     16 *        MUST contain a "DIAG8CMD ENABLE" statement within it!
                                                     17 *
                                                     18 *
                                                     19 ************************************************************************
                                                     20 ************************************************************************


                                                     22 ************************************************************************
                                                     23 *
                                                     24 *                           bfp-002-loadr.asm
                                                     25 *
                                                     26 *        This assembly-language source file is part of the
                                                     27 *                Hercules Binary Floating Point Validation Package
                                                     28 *                           by Stephen R. Orso
                                                     29 *
                                                     30 * Copyright 2016 by Stephen R Orso.
                                                     31 * Runtest *Compare dependency removed by Fish on 2022-03-08
                                                     32 * PADCSECT macro/usage removed by Fish on 2022-03-08
                                                     33 *
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                                                     36 * are met:
                                                     37 *
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                                                     39 *    notice, this list of conditions and the following disclaimer.
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                                                     41 * 2. Redistributions in binary form must reproduce the above copyright
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                                                     56 * PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                      57 * PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY
                                                      58 * OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT
                                                      59 * (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE
                                                      60 * OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.
                                                      61 *
                                                      62 ********************************************************************************



                                                      64 ********************************************************************************
                                                      65 *
                                                      66 *
                                                      67 *Testcase IEEE LOAD ROUNDED
                                                      68 *  Test case capability includes ieee exceptions trappable and
                                                      69 *  otherwise.  Test result, FPCR flags, and DXC saved for all tests.
                                                      70 *  Load Rounded does not set the condition code.
                                                      71 *
                                                      72 * Tests the following three conversion instructions
                                                      73 *   LOAD ROUNDED (long to short BFP, RRE)
                                                      74 *   LOAD ROUNDED (extended to short BFP, RRE)
                                                      75 *   LOAD ROUNDED (extended to long BFP, RRE)
                                                      76 *   LOAD ROUNDED (long short BFP, RRF-e)
                                                      77 *   LOAD ROUNDED (extended to long BFP, RRF-e)
                                                      78 *   LOAD ROUNDED (extended to short BFP, RRF-e)
                                                      79 *
                                                      80 * This routine exhaustively tests rounding in 32- and 64-bit binary
                                                      81 * floating point.  It is not possible to use Load Rounded to test
                                                      82 * rounding of 128-bit results.  There is no Load Rounded that returns
                                                      83 * a 128-bit result.
                                                      84 *
                                                      85 * Test data is compiled into this program.  The test script that runs
                                                      86 * this program can provide alternative test data through Hercules R
                                                      87 * commands.
                                                      88 *
                                                      89 * Test Case Order
                                                      90 * 1) Long to short BFP basic tests (exception traps and flags, NaNs)
                                                      91 * 2) Long to short BFP rounding mode tests
                                                      92 * 3) Extended to short BFP basic tests
                                                      93 * 4) Extended to short BFP rounding mode tests
                                                      94 * 5) Extended to long BFP basic tests.
                                                      95 * 6) Extended to long BFP rounding mode tests
                                                      96 * 7) Long to short BFP trappable underflow and overflow tests
                                                      97 * 8) Extended to short BFP trappable underflow and overflow tests
                                                      98 * 9) Extended to Long BFP trappable underflow and overflow tests
                                                      99 *
                                                     100 * Test data is 'white box,' meaning it is keyed to the internal
                                                     101 * characteristics of Softfloat 3a, while expecting results to conform
                                                     102 * to the z/Architecture Principles of Opeartion, SA22-7832-10.
                                                     103 *
                                                     104 * In the discussion below, "stored significand" does not include the
                                                     105 * implicit units digit that is always assumed to be one for a non-
                                                     106 * tiny Binary Floating Point value.
                                                     107 *
                                                     108 * Round long or extended to short: Softfloat uses the left-most 30
                                                     109 *   bits of the long or extended BFP stored significand for
                                                     110 *   rounding, which means 7 'extra' bits participate in the
                                                     111 *   rounding.  If any of the right-hand 22 bits are non-zero, the
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    112 *   30-bit pre-rounded value is or'd with 1 in the low-order bit
                                                    113 *   position.  Bit 30 is the "sticky bit."
                                                    114 *
                                                    115 * Round extended to long: Softfloat uses the left-most 62 bits of
                                                    116 *   the extended BFP stored significand for rounding, which means
                                                    117 *   10 'extra' bits participate in the rounding.  If any of the
                                                    118 *   remaining right-hand 50 bits are non-zero, the 62-bit pre-
                                                    119 *   rounded value is or'd with 1 in the low-order bit position.  Bit 62
                                                    120 *   is the "sticky bit."  At least one of the test cases will have one
                                                    121 *   bits in only the low-order 64 bits of the stored significand.
                                                    122 *
                                                    123 * The or'd 1 bit representing the bits not participating in the
                                                    124 *   rounding process prevents false exacts.  False exacts would
                                                    125 *   otherwise occur when the extra 7 or 10 bits that participate
                                                    126 *   in rounding are zero and bits to the right of them are not.
                                                    127 *
                                                    128 * Basic test cases are needed as follows:
                                                    129 *   0, +1.5, -1.5, QNaN, SNaN,
                                                    130 *
                                                    131 * Rounding test cases are needed as follows:
                                                    132 *   Exact results are represented (no rounding needed)
                                                    133 *   Ties are represented, both even (round down) and odd (round up)
                                                    134 *   False exacts are represented
                                                    135 *   Nearest value is toward zero
                                                    136 *   Nearest value is away from zero.
                                                    137 *   Each of the above must be represented in positive and negative.
                                                    138 *
                                                    139 * Because rounding decisions are based on the binary significand,
                                                    140 *   there is limited value to considering test case inputs in
                                                    141 *   decimal form.  The binary representations are all that is
                                                    142 *   important.
                                                    143 *
                                                    144 * If overflow/underflow occur and are trappable, the result should
                                                    145 *   be in the source format but scaled to the target precision.
                                                    146 *   These test cases are handled by both the basic tests to
                                                    147 *   ensure that the non-trap results are correct and again by
                                                    148 *   specific trappable overflow/underflow tests to ensure that the
                                                    149 *   scaled result rounded to target precision is returned in
                                                    150 *   the source format.
                                                    151 *
                                                    152 * Overflow/underflow behavior also means that result registers
                                                    153 *   must be sanitized and allocated in pairs for extended inputs;
                                                    154 *   results must store source format registers.  Basic tests
                                                    155 *   for overflow/underflow only store the target precision, so
                                                    156 *   *Want needs to be coded accordingly.  The trappable
                                                    157 *   overflow/underflow tests store the source format.
                                                    158 *
                                                    159 *   Overflow/underflow test cases include inputs that overflow
                                                    160 *   the target precision and that result in a tiny in the target.
                                                    161 *   Rounding mode for all overflow/underflow testing is Round
                                                    162 *   to Nearest, Ties to Even (RNTE).
                                                    163 *
                                                    164 * Rounding test cases are needed as follows:
                                                    165 *   Exact results are represented (no rounding needed)
                                                    166 *   Ties are represented, both even (round down) and odd (round up)
                                                    167 *   False exacts are represented
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    168 *   Nearest value is toward zero
                                                    169 *   Nearest value is away from zero.
                                                    170 *   Each of the above must be represented in positive and negative.
                                                    171 *
                                                    172 * Because rounding decisions are based on the binary significand,
                                                    173 *   there is limited value to considering test case inputs in
                                                    174 *   decimal form.  The binary representations are all that is
                                                    175 *   important.
                                                    176 *
                                                    177 * Three input test data sets are provided, one for long to short, one
                                                    178 *   for extended to short, and one for extended to long.  We cannot use
                                                    179 *   the same extended inputs for long and short results because the
                                                    180 *   rounding points differ for the two result precisions.
                                                    181 *
                                                    182 * Also tests the following floating point support instructions
                                                    183 *   LOAD  (Short)
                                                    184 *   LOAD  (Long)
                                                    185 *   LFPC  (Load Floating Point Control Register)
                                                    186 *   SRNMB (Set BFP Rounding Mode 3-bit)
                                                    187 *   STFPC (Store Floating Point Control Register)
                                                    188 *   STORE (Short)
                                                    189 *   STORE (Long)
                                                    190 *
                            00000000  0000A693      191 BFPLDRND START 0
                            00000000  00000001      192 R0       EQU   0
                            00000001  00000001      193 R1       EQU   1
                            00000002  00000001      194 R2       EQU   2
                            00000003  00000001      195 R3       EQU   3
                            00000004  00000001      196 R4       EQU   4
                            00000005  00000001      197 R5       EQU   5
                            00000006  00000001      198 R6       EQU   6
                            00000007  00000001      199 R7       EQU   7
                            00000008  00000001      200 R8       EQU   8
                            00000009  00000001      201 R9       EQU   9
                            0000000A  00000001      202 R10      EQU   10
                            0000000B  00000001      203 R11      EQU   11
                            0000000C  00000001      204 R12      EQU   12
                            0000000D  00000001      205 R13      EQU   13
                            0000000E  00000001      206 R14      EQU   14
                            0000000F  00000001      207 R15      EQU   15
                                                    208 *
                                                    209 * Floating Point Register equates to keep the cross reference clean
                                                    210 *
                            00000000  00000001      211 FPR0     EQU   0
                            00000001  00000001      212 FPR1     EQU   1
                            00000002  00000001      213 FPR2     EQU   2
                            00000003  00000001      214 FPR3     EQU   3
                            00000004  00000001      215 FPR4     EQU   4
                            00000005  00000001      216 FPR5     EQU   5
                            00000006  00000001      217 FPR6     EQU   6
                            00000007  00000001      218 FPR7     EQU   7
                            00000008  00000001      219 FPR8     EQU   8
                            00000009  00000001      220 FPR9     EQU   9
                            0000000A  00000001      221 FPR10    EQU   10
                            0000000B  00000001      222 FPR11    EQU   11
                            0000000C  00000001      223 FPR12    EQU   12
```

```
  LOC         OBJECT CODE        ADDR1     ADDR2     STMT
                                 0000000D  00000001   224 FPR13    EQU   13
                                 0000000E  00000001   225 FPR14    EQU   14
                                 0000000F  00000001   226 FPR15    EQU   15
                                                      227 *
00000000                         00000000             228          USING *,R15
00000000                         0000A280             229          USING HELPERS,R12
                                                      230 *
                                                      231 * Above works on real iron (R15=0 after sysclear)
                                                      232 * and in z/CMS (R15 points to start of load module)
                                                      233 *


                                                      235 ************************************************************************
                                                      236 *
                                                      237 * Low core definitions, Restart PSW, and Program Check Routine.
                                                      238 *
                                                      239 ************************************************************************


00000000                         00000000  0000008E   241          ORG   BFPLDRND+X'8E'      Program check interrution code
0000008E  0000                                       242 PCINTCD  DS    H
                                                      243 *
                                 00000150  00000000   244 PCOLDPSW EQU   BFPLDRND+X'150'     z/Arch Program check old PSW
                                                      245 *
00000090                         00000090  000001A0   246          ORG   BFPLDRND+X'1A0'     z/Arch Restart PSW
000001A0  00000001 80000000                          247          DC    X'0000000180000000',AD(START)
                                                      248 *
000001B0                         000001B0  000001D0   249          ORG   BFPLDRND+X'1D0'     z/Arch Program check NEW PSW
000001D0  00000000 00000000                          250          DC    X'0000000000000000',AD(PROGCHK)
                                                      251 *
                                                      252 * Program check routine.  If Data Exception, continue execution at
                                                      253 * the instruction following the program check.  Otherwise, hard wait.
                                                      254 * No need to collect data.  All interesting DXC stuff is captured
                                                      255 * in the FPCR.
                                                      256 *
000001E0                         000001E0  00000200   257          ORG   BFPLDRND+X'200'
00000200                                             258 PROGCHK  DS    0H              Program check occured...
00000200  9507 F08F                       0000008F   259          CLI   PCINTCD+1,X'07'  Data Exception?
00000204  A774 0004                       0000020C   260          JNE   PCNOTDTA        ..no, hardwait (not sure if R15 is ok)
00000208  B2B2 F150                       00000150   261          LPSWE PCOLDPSW        ..yes, resume program execution

0000020C  900F F23C                       0000023C   263 PCNOTDTA STM   R0,R15,SAVEREGS  Save registers
00000210  58C0 F27C                       0000027C   264          L     R12,AHELPERS     Get address of helper subroutines
00000214  4DD0 C000                       0000A280   265          BAS   R13,PGMCK        Report this unexpected program check
00000218  980F F23C                       0000023C   266          LM    R0,R15,SAVEREGS  Restore registers

0000021C  12EE                                       268          LTR   R14,R14         Return address provided?
0000021E  077E                                       269          BNZR  R14             Yes, return to z/CMS test rig.
00000220  B2B2 F228                       00000228   270          LPSWE PROGPSW         Not data exception, enter disabled wait
00000228  00020000 00000000                          271 PROGPSW  DC    0D'0',X'0002000000000000',XL6'00',X'DEAD' Abnormal end
00000238  B2B2 F2F8                       000002F8   272 FAIL     LPSWE FAILPSW         Not data exception, enter disabled wait
0000023C  00000000 00000000                          273 SAVEREGS DC    16F'0'           Registers save area
0000027C  0000A280                                   274 AHELPERS DC    A(HELPERS)       Address of helper subroutines
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    276 ********************************************************************************
                                                    277 *
                                                    278 *  Main program.  Enable Advanced Floating Point, process test cases.
                                                    279 *
00000280  B600 F308                        00000308  280 START    STCTL R0,R0,CTLR0    Store CR0 to enable AFP
00000284  9604 F309                        00000309  281          OI    CTLR0+1,X'04'  Turn on AFP bit
00000288  B700 F308                        00000308  282          LCTL  R0,R0,CTLR0    Reload updated CR0
                                                    283 *
                                                    284 * Long Load Rounded to short tests
                                                    285 *
0000028C  41A0 F314                        00000314  286          LA    R10,LTOSBAS    Long BFP test inputs
00000290  4DD0 F3A4                        000003A4  287          BAS   R13,LEDBR      Load rounded to short BFP
00000294  41A0 F344                        00000344  288          LA    R10,LTOSRM     Long BFP inputs for rounding tests
00000298  4DD0 F424                        00000424  289          BAS   R13,LEDBRA     Round to short BFP using rm options
                                                    290 *
                                                    291 * Extended Load Rounded to short tests
                                                    292 *
0000029C  41A0 F324                        00000324  293          LA    R10,XTOSBAS    Point to extended BFP test inputs
000002A0  4DD0 F4F6                        000004F6  294          BAS   R13,LEXBR      Load rounded to short BFP
000002A4  41A0 F354                        00000354  295          LA    R10,XTOSRM     Extended BFP inputs for rounding tests
000002A8  4DD0 F57A                        0000057A  296          BAS   R13,LEXBRA     Round to short BFP using rm options
                                                    297 *
                                                    298 * Extended Load Rounded to short tests
                                                    299 *
000002AC  41A0 F334                        00000334  300          LA    R10,XTOLBAS    Point to extended BFP test inputs
000002B0  4DD0 F64C                        0000064C  301          BAS   R13,LDXBR      Load rounded to long BFP
000002B4  41A0 F364                        00000364  302          LA    R10,XTOLRM     Extended BFP inputs for rounding tests
000002B8  4DD0 F6D0                        000006D0  303          BAS   R13,LDXBRA     Round to long BFP using rm options
                                                    304 *
                                                    305 * Trappable long to short tests
                                                    306 *
000002BC  41A0 F374                        00000374  307          LA    R10,LTOSOU     Long BFP over/underflow test inputs
000002C0  4DD0 F3EE                        000003EE  308          BAS   R13,LEDBROUT   Load rounded to short BFP, trappable
                                                    309 *
                                                    310 * Trappable extended to short tests
                                                    311 *
000002C4  41A0 F384                        00000384  312          LA    R10,XTOSOU     Extended BFP over/underflow test inputs
000002C8  4DD0 F540                        00000540  313          BAS   R13,LEXBROUT   Load rounded to short BFP, trappable
                                                    314 *
                                                    315 * Trappable extended to long tests
                                                    316 *
000002CC  41A0 F394                        00000394  317          LA    R10,XTOLOU     Extended BFP over/underflow test inputs
000002D0  4DD0 F696                        00000696  318          BAS   R13,LDXBROUT   Load rounded to long BFP, trappable
                                                    319 *
                                                    320 ********************************************************************************
                                                    321 *                    Verify test results...
                                                    322 ********************************************************************************
                                                    323 *
000002D4  58C0 F27C                        0000027C  324          L     R12,AHELPERS     Get address of helper subroutines
000002D8  4DD0 C0A0                        0000A320  325          BAS   R13,VERISUB      Go verify results
000002DC  12EE                                       326          LTR   R14,R14          Was return address provided?
000002DE  077E                                       327          BNZR  R14              Yes, return to z/CMS test rig.
000002E0  B2B2 F2E8                        000002E8  328          LPSWE GOODPSW          Load SUCCESS PSW
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

000002E8                                          330          DS    0D             Ensure correct alignment for PSW
000002E8  00020000 00000000                       331 GOODPSW  DC    X'0002000000000000',AD(0)  Normal end - disabled wait
000002F8  00020000 00000000                       332 FAILPSW  DC    X'0002000000000000',XL6'00',X'0BAD' Abnormal end
                                                  333 *
00000308  00000000                                334 CTLR0    DS    F
0000030C  00000000                                335 FPCREGNT DC    X'00000000'  FPCR, trap all IEEE exceptions, zero flags
00000310  F8000000                                336 FPCREGTR DC    X'F8000000'  FPCR, trap no IEEE exceptions, zero flags
                                                  337 *
                                                  338 * Input values parameter list, four fullwords:
                                                  339 *      1) Count,
                                                  340 *      2) Address of inputs,
                                                  341 *      3) Address to place results, and
                                                  342 *      4) Address to place DXC/Flags/cc values.
                                                  343 *
00000314                                          344 LTOSBAS  DS    0F           Inputs for long to short BFP tests
00000314  0000000D                                345          DC    A(LTOSCT/8)
00000318  000007A8                                346          DC    A(LTOSIN)
0000031C  00001000                                347          DC    A(LTOSOUT)
00000320  00001080                                348          DC    A(LTOSFLGS)
                                                  349 *
00000324                                          350 XTOSBAS  DS    0F           Inputs for extended to short BFP tests
00000324  0000000D                                351          DC    A(XTOSCT/16)
00000328  00000890                                352          DC    A(XTOSIN)
0000032C  00001900                                353          DC    A(XTOSOUT)
00000330  00001980                                354          DC    A(XTOSFLGS)
                                                  355 *
00000334                                          356 XTOLBAS  DS    0F           Inputs for extended to long BFP tests
00000334  0000000D                                357          DC    A(XTOLCT/16)
00000338  00000A60                                358          DC    A(XTOLIN)
0000033C  00002200                                359          DC    A(XTOLOUT)
00000340  00002300                                360          DC    A(XTOLFLGS)
                                                  361 *
00000344                                          362 LTOSRM   DS    0F       Inputs for long to short BFP rounding tests
00000344  00000010                                363          DC    A(LTOSRMCT/8)
00000348  00000810                                364          DC    A(LTOSINRM)
0000034C  00001100                                365          DC    A(LTOSRMO)
00000350  00001500                                366          DC    A(LTOSRMOF)
                                                  367 *
00000354                                          368 XTOSRM   DS    0F       Inputs for extended to short BFP rounding tests
00000354  00000010                                369          DC    A(XTOSRMCT/16)
00000358  00000960                                370          DC    A(XTOSINRM)
0000035C  00001A00                                371          DC    A(XTOSRMO)
00000360  00001E00                                372          DC    A(XTOSRMOF)
                                                  373 *
00000364                                          374 XTOLRM   DS    0F       Inputs for extended to long BFP rounding tests
00000364  00000010                                375          DC    A(XTOLRMCT/16)
00000368  00000B30                                376          DC    A(XTOLINRM)
0000036C  00002400                                377          DC    A(XTOLRMO)
00000370  00002B00                                378          DC    A(XTOLRMOF)
                                                  379 *
00000374                                          380 LTOSOU   DS    0F       Inputs for long to short BFP rounding tests
00000374  00000008                                381          DC    A(LTOSOUCT/8)
00000378  000007D0                                382          DC    A(LTOSINOU)
0000037C  00003000                                383          DC    A(LTOSOUO)
00000380  00003080                                384          DC    A(LTOSOUOF)
                                                  385 *
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00000384                                        386 XTOSOU   DS    0F       Inputs for extended to short BFP rounding tests
00000384  00000008                              387          DC    A(XTOSOUCT/16)
00000388  000008E0                              388          DC    A(XTOSINOU)
0000038C  00003100                              389          DC    A(XTOSOUO)
00000390  00003180                              390          DC    A(XTOSOUOF)
                                                391 *
00000394                                        392 XTOLOU   DS    0F       Inputs for extended to long BFP rounding tests
00000394  00000008                              393          DC    A(XTOLOUCT/16)
00000398  00000AB0                              394          DC    A(XTOLINOU)
0000039C  00003200                              395          DC    A(XTOLOUO)
000003A0  00003280                              396          DC    A(XTOLOUOF)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                    398 ************************************************************************
                                                    399 *
                                                    400 * Round long BFP to short BFP.  A pair of results is generated for each
                                                    401 * input: one with all exceptions non-trappable, and the second with all
                                                    402 * exceptions trappable.   The FPCR contents are stored for each result.
                                                    403 *
                                                    404 ************************************************************************


000003A4  9823 A000                 00000000   406 LEDBR    LM    R2,R3,0(R10)  Get count and address of test input values
000003A8  9878 A008                 00000008   407          LM    R7,R8,8(R10)  Get address of result area and flag area.
000003AC  1222                                 408          LTR   R2,R2         Any test cases?
000003AE  078D                                 409          BZR   R13           ..No, return to caller
000003B0  0DC0                                 410          BASR  R12,0         Set top of loop
                                               411 *
000003B2  B375 0010                            412          LZDR  FPR1          Zero FRP1 to clear any residual
000003B6  6800 3000                 00000000   413          LD    FPR0,0(,R3)   Get long BFP test value
000003BA  B29D F30C                 0000030C   414          LFPC  FPCREGNT      Set exceptions non-trappable
000003BE  B344 0010                            415          LEDBR FPR1,FPR0     Cvt long in FPR0 to short in FPR1
000003C2  7010 7000                 00000000   416          STE   FPR1,0(,R7)   Store short BFP result
000003C6  B29C 8000                 00000000   417          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                               418 *
000003CA  B375 0010                            419          LZDR  FPR1          Zero FRP1 to clear any residual
000003CE  B29D F310                 00000310   420          LFPC  FPCREGTR      Set exceptions trappable
000003D2  B344 0010                            421          LEDBR FPR1,FPR0     Cvt long in FPR0 to short in FPR1
000003D6  7010 7004                 00000004   422          STE   FPR1,4(,R7)   Store short BFP result
000003DA  B29C 8004                 00000004   423          STFPC 4(R8)         Store resulting FPCR flags and DXC
                                               424 *
000003DE  4130 3008                 00000008   425          LA    R3,8(,R3)     Point to next input value
000003E2  4170 7008                 00000008   426          LA    R7,8(,R7)     Point to next result pair
000003E6  4180 8008                 00000008   427          LA    R8,8(,R8)     Point to next FPCR result area
000003EA  062C                                 428          BCTR  R2,R12        Convert next input value.
000003EC  07FD                                 429          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                    431 ************************************************************************
                                                    432 *
                                                    433 * Round long BFP to short BFP.  Inputs are expected to generate
                                                    434 * overflow or underflow exceptions, all of which are trappable.  This
                                                    435 * means a scaled result should be generated rounded to the target
                                                    436 * precision but returned in the source precision.   The FPCR contents
                                                    437 * are stored for each result.
                                                    438 *
                                                    439 ************************************************************************


000003EE  9823 A000                 00000000   441 LEDBROUT LM    R2,R3,0(R10)  Get count and address of test input values
000003F2  9878 A008                 00000008   442          LM    R7,R8,8(R10)  Get address of result area and flag area.
000003F6  1222                                 443          LTR   R2,R2         Any test cases?
000003F8  078D                                 444          BZR   R13           ..No, return to caller
000003FA  0DC0                                 445          BASR  R12,0         Set top of loop
                                               446 *
000003FC  B375 0010                            447          LZDR  FPR1          Zero FRP1 to clear any residual
00000400  6800 3000                 00000000  448          LD    FPR0,0(,R3)   Get long BFP test value
00000404  B29D F310                 00000310  449          LFPC  FPCREGTR      Set exceptions trappable
00000408  B344 0010                            450          LEDBR FPR1,FPR0     Cvt long in FPR0 into short in FPR1
0000040C  6010 7000                 00000000  451          STD   FPR1,0(,R7)   Store long scaled BFP trapped result
00000410  B29C 8000                 00000000  452          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                               453 *
00000414  4130 3008                 00000008  454          LA    R3,8(,R3)     Point to next input value
00000418  4170 7008                 00000008  455          LA    R7,8(,R7)     Point to next long trapped result value
0000041C  4180 8004                 00000004  456          LA    R8,4(,R8)     Point to next FPCR result area
00000420  062C                                 457          BCTR  R2,R12        Convert next input value.
00000422  07FD                                 458          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    460 ************************************************************************
                                                    461 *
                                                    462 * Convert long BFP to rounded short BFP using each possible rounding
                                                    463 * mode.  Ten test results are generated for each input.  A 48-byte test
                                                    464 * result section is used to keep results sets aligned on a quad-double
                                                    465 * word.
                                                    466 *
                                                    467 * The first four tests use rounding modes specified in the FPCR with
                                                    468 * the IEEE Inexact exception supressed.  SRNM (2-bit) is used  for
                                                    469 * the first two FPCR-controlled tests and SRNMB (3-bit) is used for
                                                    470 * the last two To get full coverage of that instruction pair.
                                                    471 *
                                                    472 * The next six results use instruction-specified rounding modes.
                                                    473 *
                                                    474 * The default rounding mode (0 for RNTE) is not tested in this
                                                    475 * section; prior tests used the default rounding mode.  RNTE is tested
                                                    476 * explicitly as a rounding mode in this section.
                                                    477 *
                                                    478 ************************************************************************

00000424  9823 A000                 00000000   480 LEDBRA   LM    R2,R3,0(R10)  Get count and address of test input values
00000428  9878 A008                 00000008   481           LM    R7,R8,8(R10)  Get address of result area and flag area.
0000042C  1222                                 482           LTR   R2,R2         Any test cases?
0000042E  078D                                 483           BZR   R13           ..No, return to caller
00000430  0DC0                                 484           BASR  R12,0         Set top of loop
                                               485 *
00000432  6800 3000                 00000000   486           LD    FPR0,0(,R3)    Get long BFP test value
                                               487 *
                                               488 * Test cases using rounding mode specified in the FPCR
                                               489 *
00000436  B29D F30C                 0000030C   490           LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
0000043A  B299 0001                 00000001   491           SRNM  1             SET FPCR to RZ, Round towards zero.
0000043E  B344 0410                            492           LEDBRA FPR1,0,FPR0,B'0100'  FPCR ctl'd rounding, mask inexact
00000442  7010 7000                 00000000   493           STE   FPR1,0*4(,R7) Store shortened rounded BFP result
00000446  B29C 8000                 00000000   494           STFPC 0(R8)         Store resulting FPCRflags and DXC
                                               495 *
0000044A  B29D F30C                 0000030C   496           LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
0000044E  B299 0002                 00000002   497           SRNM  2             SET FPCR to RP, Round to +infinity
00000452  B344 0410                            498           LEDBRA FPR1,0,FPR0,B'0100'  FPCR ctl'd rounding, mask inexact
00000456  7010 7004                 00000004   499           STE   FPR1,1*4(,R7) Store shortened rounded BFP result
0000045A  B29C 8004                 00000004   500           STFPC 1*4(R8)       Store resulting FPCR flags and DXC
                                               501 *
0000045E  B29D F30C                 0000030C   502           LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000462  B2B8 0003                 00000003   503           SRNMB 3             SET FPCR to RM, Round to -infinity
00000466  B344 0410                            504           LEDBRA FPR1,0,FPR0,B'0100'  FPCR ctl'd rounding, mask inexact
0000046A  7010 7008                 00000008   505           STE   FPR1,2*4(,R7) Store shortened rounded BFP result
0000046E  B29C 8008                 00000008   506           STFPC 2*4(R8)       Store resulting FPCR flags and DXC
                                               507 *
00000472  B29D F30C                 0000030C   508           LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000476  B2B8 0007                 00000007   509           SRNMB 7             RFS, Round Prepare for Shorter Precision
0000047A  B344 0410                            510           LEDBRA FPR1,0,FPR0,B'0100'  FPCR ctl'd rounding, mask inexact
0000047E  7010 700C                 0000000C   511           STE   FPR1,3*4(,R7) Store shortened rounded BFP result
00000482  B29C 800C                 0000000C   512           STFPC 3*4(R8)       Store resulting FPCR flags and DXC
                                               513 *
                                               514 * Test cases using rounding mode specified in the instruction M3 field
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    515 *
00000486  B29D F30C                     0000030C   516          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
0000048A  B344 1010                                517          LEDBRA FPR1,1,FPR0,B'0000'  RNTA, to nearest, ties away
0000048E  7010 7010                     00000010   518          STE   FPR1,4*4(,R7) Store shortened rounded BFP result
00000492  B29C 8010                     00000010   519          STFPC 4*4(R8)       Store resulting FPCR flags and DXC
                                                    520 *
00000496  B29D F30C                     0000030C   521          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
0000049A  B344 3010                                522          LEDBRA FPR1,3,FPR0,B'0000'  RFS, prepare for shorter precision
0000049E  7010 7014                     00000014   523          STE   FPR1,5*4(,R7) Store shortened rounded BFP result
000004A2  B29C 8014                     00000014   524          STFPC 5*4(R8)       Store resulting FPCR flags and DXC
                                                    525 *
000004A6  B29D F30C                     0000030C   526          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000004AA  B344 4010                                527          LEDBRA FPR1,4,FPR0,B'0000'  RNTE, to nearest, ties to even
000004AE  7010 7018                     00000018   528          STE   FPR1,6*4(,R7) Store shortened rounded BFP result
000004B2  B29C 8018                     00000018   529          STFPC 6*4(R8)       Store resulting FPCR flags and DXC
                                                    530 *
000004B6  B29D F30C                     0000030C   531          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000004BA  B344 5010                                532          LEDBRA FPR1,5,FPR0,B'0000'  RZ, toward zero
000004BE  7010 701C                     0000001C   533          STE   FPR1,7*4(,R7) Store shortened rounded BFP result
000004C2  B29C 801C                     0000001C   534          STFPC 7*4(R8)       Store resulting FPCR flags and DXC
                                                    535 *
000004C6  B29D F30C                     0000030C   536          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000004CA  B344 6010                                537          LEDBRA FPR1,6,FPR0,B'0000' RP, to +inf
000004CE  7010 7020                     00000020   538          STE   FPR1,8*4(,R7) Store shortened rounded BFP result
000004D2  B29C 8020                     00000020   539          STFPC 8*4(R8)       Store resulting FPCR flags and DXC
                                                    540 *
000004D6  B29D F30C                     0000030C   541          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000004DA  B344 7010                                542          LEDBRA FPR1,7,FPR0,B'0000' RM, to -inf
000004DE  7010 7024                     00000024   543          STE   FPR1,9*4(,R7) Store shortened rounded BFP result
000004E2  B29C 8024                     00000024   544          STFPC 9*4(R8)       Store resulting FPCR flags and DXC
                                                    545 *
000004E6  4130 3008                     00000008   546          LA    R3,8(,R3)     Point to next input value
000004EA  4170 7030                     00000030   547          LA    R7,12*4(,R7)  Point to next short BFP result pair
000004EE  4180 8030                     00000030   548          LA    R8,12*4(,R8)  Point to next FPCR result area
000004F2  062C                                     549          BCTR  R2,R12        Convert next input value.
000004F4  07FD                                     550          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                    552 ************************************************************************
                                                    553 *
                                                    554 * Round extended BFP to short BFP.  A pair of results is genearted for
                                                    555 * each input: one with all exceptions non-trappable, and the second
                                                    556 * with all exceptions trappable.   The FPCR contents are stored for
                                                    557 * each result.
                                                    558 *
                                                    559 ************************************************************************


000004F6  9823 A000                 00000000    561 LEXBR    LM    R2,R3,0(R10)  Get count and address of test input values
000004FA  9878 A008                 00000008    562          LM    R7,R8,8(R10)  Get address of result area and flag area.
000004FE  1222                                  563          LTR   R2,R2         Any test cases?
00000500  078D                                  564          BZR   R13           ..No, return to caller
00000502  0DC0                                  565          BASR  R12,0         Set top of loop
                                                566 *
00000504  6800 3000                 00000000    567          LD    FPR0,0(,R3)   Get extended BFP test value part 1
00000508  6820 3008                 00000008    568          LD    R2,8(,R3)     Get extended BFP test value part 2
0000050C  B29D F30C                 0000030C    569          LFPC  FPCREGNT      Set exceptions non-trappable
00000510  B346 0010                             570          LEXBR FPR1,FPR0     Cvt extended in FPR0-2 to short in FPR1
00000514  7010 7000                 00000000    571          STE   R1,0(,R7)     Store short BFP result
00000518  B29C 8000                 00000000    572          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                573 *
0000051C  B29D F310                 00000310    574          LFPC  FPCREGTR      Set exceptions trappable
00000520  B375 0010                             575          LZDR  FPR1          Eliminate any residual results
00000524  B346 0010                             576          LEXBR FPR1,FPR0     Cvt extended in FPR0-2 to short in FPR1
00000528  7010 7004                 00000004    577          STE   FPR1,4(,R7)   Store short BFP result
0000052C  B29C 8004                 00000004    578          STFPC 4(R8)         Store resulting FPCR flags and DXC
                                                579 *
00000530  4130 3010                 00000010    580          LA    R3,16(,R3)    Point to next input value
00000534  4170 7008                 00000008    581          LA    R7,8(,R7)     Point to next long rounded value pair
00000538  4180 8008                 00000008    582          LA    R8,8(,R8)     Point to next FPCR result area
0000053C  062C                                  583          BCTR  R2,R12        Convert next input value.
0000053E  07FD                                  584          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    586 ************************************************************************
                                                    587 *
                                                    588 * Round extended BFP to short BFP.  Inputs are expected to generate
                                                    589 * overflow or underflow exceptions, all of which are trappable.  This
                                                    590 * means a scaled result should be generated rounded to the target
                                                    591 * precision but returned in the source precision.   The FPCR contents
                                                    592 * are stored for each result.
                                                    593 *
                                                    594 ************************************************************************


00000540  9823 A000                 00000000    596 LEXBROUT LM    R2,R3,0(R10)  Get count and address of test input values
00000544  9878 A008                 00000008    597          LM    R7,R8,8(R10)  Get address of result area and flag area.
00000548  1222                                  598          LTR   R2,R2         Any test cases?
0000054A  078D                                  599          BZR   R13           ..No, return to caller
0000054C  0DC0                                  600          BASR  R12,0         Set top of loop
                                                    601 *
0000054E  6800 3000                 00000000    602          LD    FPR0,0(,R3)   Get extended BFP test value part 1
00000552  6820 3008                 00000008    603          LD    R2,8(,R3)     Get extended BFP test value part 2
00000556  B29D F310                 00000310    604          LFPC  FPCREGTR      Set exceptions trappable
0000055A  B346 0010                             605          LEXBR FPR1,FPR0     Cvt float in FPR0-2 to scaled in FPR1-3
0000055E  6010 7000                 00000000    606          STD   FPR1,0(,R7)   Store scaled extended BFP result part 1
00000562  6030 7008                 00000008    607          STD   FPR3,8(,R7)   Store scaled extended BFP result part 2
00000566  B29C 8000                 00000000    608          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                    609 *
0000056A  4130 3010                 00000010    610          LA    R3,16(,R3)    Point to next input value
0000056E  4170 7010                 00000010    611          LA    R7,16(,R7)    Point to next extended trapped result
00000572  4180 8004                 00000004    612          LA    R8,4(,R8)     Point to next FPCR result area
00000576  062C                                  613          BCTR  R2,R12        Convert next input value.
00000578  07FD                                  614          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    616 ************************************************************************
                                                    617 *
                                                    618 * Convert long BFP to integers using each possible rounding mode.
                                                    619 * Ten test results are generated for each input.  A 48-byte test result
                                                    620 * section is used to keep results sets aligned on a quad-double word.
                                                    621 *
                                                    622 * The first four tests use rounding modes specified in the FPCR with
                                                    623 * the IEEE Inexact exception supressed.  SRNM (2-bit) is used  for
                                                    624 * the first two FPCR-controlled tests and SRNMB (3-bit) is used for
                                                    625 * the last two To get full coverage of that instruction pair.
                                                    626 *
                                                    627 * The next six results use instruction-specified rounding modes.
                                                    628 *
                                                    629 * The default rounding mode (0 for RNTE) is not tested in this
                                                    630 * section; prior tests used the default rounding mode.  RNTE is tested
                                                    631 * explicitly as a rounding mode in this section.
                                                    632 *
                                                    633 ************************************************************************

0000057A  9823 A000                 00000000    635 LEXBRA   LM    R2,R3,0(R10)  Get count and address of test input values
0000057E  9878 A008                 00000008    636          LM    R7,R8,8(R10)  Get address of result area and flag area.
00000582  1222                                  637          LTR   R2,R2         Any test cases?
00000584  078D                                  638          BZR   R13           ..No, return to caller
00000586  0DC0                                  639          BASR  R12,0         Set top of loop
                                                    640 *
00000588  6800 3000                 00000000    641          LD    FPR0,0(,R3)    Get long BFP test value
                                                    642 *
                                                    643 * Test cases using rounding mode specified in the FPCR
                                                    644 *
0000058C  B29D F30C                 0000030C    645          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000590  B299 0001                 00000001    646          SRNM  1             SET FPCR to RZ, Round towards zero.
00000594  B346 0410                             647          LEXBRA FPR1,0,FPR0,B'0100' FPCR ctl'd rounding, mask inexact
00000598  6010 7000                 00000000    648          STD   FPR1,0*4(,R7) Store shortened rounded BFP result
0000059C  B29C 8000                 00000000    649          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                    650 *
000005A0  B29D F30C                 0000030C    651          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000005A4  B299 0002                 00000002    652          SRNM  2             SET FPCR to RP, Round to +infinity
000005A8  B346 0410                             653          LEXBRA FPR1,0,FPR0,B'0100' FPCR ctl'd rounding, mask inexact
000005AC  6010 7004                 00000004    654          STD   FPR1,1*4(,R7) Store shortened rounded BFP result
000005B0  B29C 8004                 00000004    655          STFPC 1*4(R8)       Store resulting FPCR flags and DXC
                                                    656 *
000005B4  B29D F30C                 0000030C    657          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000005B8  B2B8 0003                 00000003    658          SRNMB 3             SET FPCR to RM, Round to -infinity
000005BC  B346 0410                             659          LEXBRA FPR1,0,FPR0,B'0100' FPCR ctl'd rounding, mask inexact
000005C0  6010 7008                 00000008    660          STD   FPR1,2*4(,R7) Store shortened rounded BFP result
000005C4  B29C 8008                 00000008    661          STFPC 2*4(R8)       Store resulting FPCR flags and DXC
                                                    662 *
000005C8  B29D F30C                 0000030C    663          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000005CC  B2B8 0007                 00000007    664          SRNMB 7             RFS, Round Prepare for Shorter Precision
000005D0  B346 0410                             665          LEXBRA FPR1,0,FPR0,B'0100' FPCR ctl'd rounding, mask inexact
000005D4  6010 700C                 0000000C    666          STD   FPR1,3*4(,R7) Store shortened rounded BFP result
000005D8  B29C 800C                 0000000C    667          STFPC 3*4(R8)       Store resulting FPCR flags and DXC
                                                    668 *
                                                    669 * Test cases using rounding mode specified in the instruction M3 field
                                                    670 *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000005DC  B29D F30C                    0000030C   671          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000005E0  B346 1010                               672          LEXBRA FPR1,1,FPR0,B'0000' RNTA, to nearest, ties away
000005E4  6010 7010                    00000010   673          STD   FPR1,4*4(,R7) Store shortened rounded BFP result
000005E8  B29C 8010                    00000010   674          STFPC 4*4(R8)       Store resulting FPCR flags and DXC
                                                  675 *
000005EC  B29D F30C                    0000030C   676          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000005F0  B346 3010                               677          LEXBRA FPR1,3,FPR0,B'0000' RFS, prepare for shorter precision
000005F4  6010 7014                    00000014   678          STD   FPR1,5*4(,R7) Store shortened rounded BFP result
000005F8  B29C 8014                    00000014   679          STFPC 5*4(R8)       Store resulting FPCR flags and DXC
                                                  680 *
000005FC  B29D F30C                    0000030C   681          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000600  B346 4010                               682          LEXBRA FPR1,4,FPR0,B'0000' RNTE, to nearest, ties to even
00000604  6010 7018                    00000018   683          STD   FPR1,6*4(,R7) Store shortened rounded BFP result
00000608  B29C 8018                    00000018   684          STFPC 6*4(R8)       Store resulting FPCR flags and DXC
                                                  685 *
0000060C  B29D F30C                    0000030C   686          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000610  B346 5010                               687          LEXBRA FPR1,5,FPR0,B'0000' RZ, toward zero
00000614  6010 701C                    0000001C   688          STD   FPR1,7*4(,R7) Store shortened rounded BFP result
00000618  B29C 801C                    0000001C   689          STFPC 7*4(R8)       Store resulting FPCR flags and DXC
                                                  690 *
0000061C  B29D F30C                    0000030C   691          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000620  B346 6010                               692          LEXBRA FPR1,6,FPR0,B'0000' RP, to +inf
00000624  6010 7020                    00000020   693          STD   FPR1,8*4(,R7) Store shortened rounded BFP result
00000628  B29C 8020                    00000020   694          STFPC 8*4(R8)       Store resulting FPCR flags and DXC
                                                  695 *
0000062C  B29D F30C                    0000030C   696          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000630  B346 7010                               697          LEXBRA FPR1,7,FPR0,B'0000' RM, to -inf
00000634  6010 7024                    00000024   698          STD   FPR1,9*4(,R7) Store shortened rounded BFP result
00000638  B29C 8024                    00000024   699          STFPC 9*4(R8)       Store resulting FPCR flags and DXC
                                                  700 *
0000063C  4130 3010                    00000010   701          LA    R3,16(,R3)    Point to next input value
00000640  4170 7030                    00000030   702          LA    R7,12*4(,R7)  Point to next long BFP converted values
00000644  4180 8030                    00000030   703          LA    R8,12*4(,R8)  Point to next FPCR/CC result area
00000648  062C                                    704          BCTR  R2,R12        Convert next input value.
0000064A  07FD                                    705          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   707 ************************************************************************
                                                   708 *
                                                   709 * Round extended BFP to long BFP.  A pair of results is generated for
                                                   710 * each input: one with all exceptions non-trappable, and the second
                                                   711 * with all exceptions trappable.   The FPCR contents are stored for
                                                   712 * each result.
                                                   713 *
                                                   714 ************************************************************************

0000064C  9823 A000                 00000000    716 LDXBR    LM    R2,R3,0(R10)  Get count and address of test input values
00000650  9878 A008                 00000008    717          LM    R7,R8,8(R10)  Get address of result area and flag area.
00000654  1222                                  718          LTR   R2,R2         Any test cases?
00000656  078D                                  719          BZR   R13           ..No, return to caller
00000658  0DC0                                  720          BASR  R12,0         Set top of loop
                                                721 *
0000065A  6800 3000                 00000000    722          LD    FPR0,0(,R3)   Get extended BFP test value part 1
0000065E  6820 3008                 00000008    723          LD    R2,8(,R3)     Get extended BFP test value part 1
00000662  B29D F30C                 0000030C    724          LFPC  FPCREGNT      Set exceptions non-trappable
00000666  B345 0010                             725          LDXBR FPR1,FPR0     Round extended in FPR0-2 to long in FPR1
0000066A  6010 7000                 00000000    726          STD   FPR1,0(,R7)   Store shortened rounded BFP result
0000066E  B29C 8000                 00000000    727          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                728 *
00000672  B29D F310                 00000310    729          LFPC  FPCREGTR      Set exceptions trappable
00000676  B376 0010                             730          LZXR  FPR1          Eliminate any residual results
0000067A  B345 0010                             731          LDXBR FPR1,FPR0     Round extended in FPR0-2 to long in FPR1
0000067E  6010 7008                 00000008    732          STD   FPR1,8(,R7)   Store shortened rounded BFP result
00000682  B29C 8004                 00000004    733          STFPC 4(R8)         Store resulting FPCR flags and DXC
                                                734 *
00000686  4130 3010                 00000010    735          LA    R3,16(,R3)    Point to next extended BFP input value
0000068A  4170 7010                 00000010    736          LA    R7,16(,R7)    Point to next long BFP rounded value pair
0000068E  4180 8008                 00000008    737          LA    R8,8(,R8)     Point to next FPCR result area
00000692  062C                                  738          BCTR  R2,R12        Convert next input value.
00000694  07FD                                  739          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    741 ************************************************************************
                                                    742 *
                                                    743 * Round extended BFP to long BFP.  Inputs are expected to generate
                                                    744 * overflow or underflow exceptions, all of which are trappable.  This
                                                    745 * means a scaled result should be generated rounded to the target
                                                    746 * precision but returned in the source precision.   The FPCR contents
                                                    747 * are stored for each result.
                                                    748 *
                                                    749 ************************************************************************

00000696  9823 A000                 00000000    751 LDXBROUT LM    R2,R3,0(R10)  Get count and address of test input values
0000069A  9878 A008                 00000008    752          LM    R7,R8,8(R10)  Get address of result area and flag area.
0000069E  1222                                  753          LTR   R2,R2         Any test cases?
000006A0  078D                                  754          BZR   R13           ..No, return to caller
000006A2  0DC0                                  755          BASR  R12,0         Set top of loop
                                                    756 *
000006A4  6800 3000                 00000000    757          LD    FPR0,0(,R3)   Get extended BFP test value part 1
000006A8  6820 3008                 00000008    758          LD    R2,8(,R3)     Get extended BFP test value part 1
000006AC  B29D F310                 00000310    759          LFPC  FPCREGTR      Set exceptions trappable
000006B0  B345 0010                             760          LDXBR FPR1,FPR0     Round ext'd in FPR0-2 to scaled in FPR1-3
000006B4  6010 7000                 00000000    761          STD   FPR1,0(,R7)   Store scaled extended BFP result part 1
000006B8  6030 7008                 00000008    762          STD   FPR3,8(,R7)   Store scaled extended BFP result part 2
000006BC  B29C 8000                 00000000    763          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                    764 *
000006C0  4130 3010                 00000010    765          LA    R3,16(,R3)    Point to next extended BFP input value
000006C4  4170 7010                 00000010    766          LA    R7,16(,R7)    Point to next long BFP rounded value pair
000006C8  4180 8004                 00000004    767          LA    R8,4(,R8)     Point to next FPCR result area
000006CC  062C                                  768          BCTR  R2,R12        Convert next input value.
000006CE  07FD                                  769          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                     771 ************************************************************************
                                                     772 *
                                                     773 * Convert extended BFP to integers using each possible rounding mode.
                                                     774 * Ten test results are generated for each input.  A 48-byte test result
                                                     775 * section is used to keep results sets aligned on a quad-double word.
                                                     776 *
                                                     777 * The first four tests use rounding modes specified in the FPCR with
                                                     778 * the IEEE Inexact exception supressed.  SRNM (2-bit) is used  for
                                                     779 * the first two FPCR-controlled tests and SRNMB (3-bit) is used for
                                                     780 * the last two To get full coverage of that instruction pair.
                                                     781 *
                                                     782 * The next six results use instruction-specified rounding modes.
                                                     783 *
                                                     784 * The default rounding mode (0 for RNTE) is not tested in this
                                                     785 * section; `prior tests used the default rounding mode.  RNTE is tested
                                                     786 * explicitly as a rounding mode in this section.
                                                     787 *
                                                     788 ************************************************************************

000006D0  9823 A000                 00000000    790 LDXBRA   LM    R2,R3,0(R10)  Get count and address of test input values
000006D4  9878 A008                 00000008    791          LM    R7,R8,8(R10)  Get address of result area and flag area.
000006D8  1222                                  792          LTR   R2,R2         Any test cases?
000006DA  078D                                  793          BZR   R13           ..No, return to caller
000006DC  0DC0                                  794          BASR  R12,0         Set top of loop
                                                795 *
000006DE  6800 3000                 00000000    796          LD    FPR0,0(,R3)    Get extended BFP test value part 1
000006E2  6820 3008                 00000008    797          LD    R2,8(,R3)    Get extended BFP test value part 2
                                                798 *
                                                799 * Test cases using rounding mode specified in the FPCR
                                                800 *
000006E6  B29D F30C                 0000030C    801          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000006EA  B299 0001                 00000001    802          SRNM  1             SET FPCR to RZ, Round towards zero.
000006EE  B345 0410                             803          LDXBRA FPR1,0,FPR0,B'0100' FPCR ctl'd rounding, mask inexact
000006F2  6010 7000                 00000000    804          STD   FPR1,0*8(,R7) Store shortened rounded BFP result
000006F6  B29C 8000                 00000000    805          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                806 *
000006FA  B29D F30C                 0000030C    807          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000006FE  B299 0002                 00000002    808          SRNM  2             SET FPCR to RP, Round to +infinity
00000702  B345 0410                             809          LDXBRA FPR1,0,FPR0,B'0100' FPCR ctl'd rounding, mask inexact
00000706  6010 7008                 00000008    810          STD   FPR1,1*8(,R7) Store shortened rounded BFP result
0000070A  B29C 8004                 00000004    811          STFPC 1*4(R8)       Store resulting FPCR flags and DXC
                                                812 *
0000070E  B29D F30C                 0000030C    813          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000712  B2B8 0003                 00000003    814          SRNMB 3             SET FPCR to RM, Round to -infinity
00000716  B345 0410                             815          LDXBRA FPR1,0,FPR0,B'0100' FPCR ctl'd rounding, mask inexact
0000071A  6010 7010                 00000010    816          STD   FPR1,2*8(,R7) Store shortened rounded BFP result
0000071E  B29C 8008                 00000008    817          STFPC 2*4(R8)       Store resulting FPCR flags and DXC
                                                818 *
00000722  B29D F30C                 0000030C    819          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000726  B2B8 0007                 00000007    820          SRNMB 7             RFS, Round Prepare for Shorter Precision
0000072A  B345 0410                             821          LDXBRA FPR1,0,FPR0,B'0100' FPCR ctl'd rounding, mask inexact
0000072E  6010 7018                 00000018    822          STD   FPR1,3*8(,R7) Store shortened rounded BFP result
00000732  B29C 800C                 0000000C    823          STFPC 3*4(R8)       Store resulting FPCR flags and DXC
                                                824 *
00000736  B29D F30C                 0000030C    825          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
0000073A  B345 1010                          826          LDXBRA FPR1,1,FPR0,B'0000' RNTA, to nearest, ties away
0000073E  6010 7020                 00000020 827          STD   FPR1,4*8(,R7) Store shortened rounded BFP result
00000742  B29C 8010                 00000010 828          STFPC 4*4(R8)       Store resulting FPCR flags and DXC
                                             829 *
00000746  B29D F30C                 0000030C 830          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
0000074A  B345 3010                          831          LDXBRA FPR1,3,FPR0,B'0000' RFS, prepare for shorter precision
0000074E  6010 7028                 00000028 832          STD   FPR1,5*8(,R7) Store shortened rounded BFP result
00000752  B29C 8014                 00000014 833          STFPC 5*4(R8)       Store resulting FPCR flags and DXC
                                             834 *
00000756  B29D F30C                 0000030C 835          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
0000075A  B345 4010                          836          LDXBRA FPR1,4,FPR0,B'0000' RNTE, to nearest, ties to even
0000075E  6010 7030                 00000030 837          STD   FPR1,6*8(,R7) Store shortened rounded BFP result
00000762  B29C 8018                 00000018 838          STFPC 6*4(R8)       Store resulting FPCR flags and DXC
                                             839 *
00000766  B29D F30C                 0000030C 840          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
0000076A  B345 5010                          841          LDXBRA FPR1,5,FPR0,B'0000' RZ, toward zero
0000076E  6010 7038                 00000038 842          STD   FPR1,7*8(,R7) Store shortened rounded BFP result
00000772  B29C 801C                 0000001C 843          STFPC 7*4(R8)       Store resulting FPCR flags and DXC
                                             844 *
00000776  B29D F30C                 0000030C 845          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
0000077A  B345 6010                          846          LDXBRA FPR1,6,FPR0,B'0000' RP, to +inf
0000077E  6010 7040                 00000040 847          STD   FPR1,8*8(,R7) Store shortened rounded BFP result
00000782  B29C 8020                 00000020 848          STFPC 8*4(R8)       Store resulting FPCR flags and DXC
                                             849 *
00000786  B29D F30C                 0000030C 850          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
0000078A  B345 7010                          851          LDXBRA FPR1,7,FPR0,B'0000' RM, to -inf
0000078E  6010 7048                 00000048 852          STD   FPR1,9*8(,R7) Store shortened rounded BFP result
00000792  B29C 8024                 00000024 853          STFPC 9*4(R8)       Store resulting FPCR flags and DXC
                                             854 *
00000796  4130 3010                 00000010 855          LA    R3,16(,R3)    Point to next input value
0000079A  4170 7050                 00000050 856          LA    R7,10*8(,R7)  Point to next long BFP rounded result
0000079E  4180 8030                 00000030 857          LA    R8,12*4(,R8)  Point to next FPCR result area
000007A2  062C                               858          BCTR  R2,R12        Convert next input value.
000007A4  07FD                               859          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    861 ********************************************************************************
                                                    862 *
                                                    863 * BFP inputs.  One set of longs and two sets of extendeds are included.
                                                    864 * Each set includes input values for basic exception testing and input
                                                    865 * values for exhaustive rounding mode testing.  One set of extended
                                                    866 * inputs is used to generate short results, and the other is used to
                                                    867 * generate long results.  The same set cannot be used for both long
                                                    868 * and short because the rounding points are different.
                                                    869 *
                                                    870 * We can cheat and use the same decimal values for long to short and
                                                    871 * and extended to short because the result has the same number of
                                                    872 * bits and the rounding uses the same number of bits in the pre-
                                                    873 * rounded result.
                                                    874 *
                                                    875 ********************************************************************************


                                                    877 *
                                                    878 * Long to short basic tests, which tests trappable results, NaN
                                                    879 * propagation, and basic functionality.  The second part of this list
                                                    880 * is used for testing trappable results.
                                                    881 *
000007A8                                            882 LTOSIN   DS    0D        Inputs for long to short BFP basic tests
000007A8  00000000 00000000                         883          DC    X'0000000000000000'         +0
000007B0  3FF80000 00000000                         884          DC    X'3FF8000000000000'         +1.5
000007B8  BFF80000 00000000                         885          DC    X'BFF8000000000000'         -1.5
000007C0  7FF01000 00000000                         886          DC    X'7FF0100000000000'         SNaN
000007C8  7FF81100 00000000                         887          DC    X'7FF8110000000000'         QNaN
                                                    888 * See rounding tests below for details on the following four
000007D0                                            889 LTOSINOU DS    0D             start of under/overflow tests
000007D0  47EFFFFF FFFFFFFF                         890          DC    X'47EFFFFFFFFFFFFF'    Positive oveflow test
000007D8  C7EFFFFF FFFFFFFF                         891          DC    X'C7EFFFFFFFFFFFFF'    Negative oveflow test
000007E0  47FFFFFF EFFFFFFF                         892          DC    X'47FFFFFFEFFFFFFF'    Positive oveflow prec. test
000007E8  C7FFFFFF EFFFFFFF                         893          DC    X'C7FFFFFFEFFFFFFF'    Negative oveflow prec. test
000007F0  36900000 00000000                         894          DC    X'3690000000000000'    Positive magnitude underflow
000007F8  B6900000 00000000                         895          DC    X'B690000000000000'    Negative magnitude underflow
00000800  47F00000 00000000                         896          DC    X'47F0000000000000'    Positive magnitude overflow
00000808  C7F00000 00000000                         897          DC    X'C7F0000000000000'    Negative magnitude overflow
                                                    898 *
                          00000068  00000001        899 LTOSCT   EQU   *-LTOSIN     Count of long BFP in list * 8
                          00000040  00000001        900 LTOSOUCT EQU   *-LTOSINOU   Ct * 8 of trappable over/underflow tests




                                                    902 *
                                                    903 * Test cases for exhaustive rounding mode tests of long to short
                                                    904 * Load Rounded.
                                                    905 *
00000810                                            906 LTOSINRM DS    0D        Inputs for long to short BFP rounding tests
                                                    907 *              x'8000000000000000'    sign bit
                                                    908 *              x'7FF0000000000000'    Biased Exponent
                                                    909 *              x'000FFFFFE0000000'    Significand used in short
                                                    910 *              x'000000001FC00000'    Significand used in rounding
                                                    911 *              x'00000000003FFFFF'    'extra' significand bits
                                                    912 *   Note: in the comments below, 'up' and 'down' mean 'toward
                                                    913 *   higher magnitude' and 'toward lower magnitude' respectively and
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      914 *   without regard to the sign, and rounding is to short BFP.
                                                      915 *
                                                      916 * Exact (fits in short BFP)   ..  1.999999880790710449218750
00000810  3FFFFFFF E0000000                           917          DC    X'3FFFFFFFE0000000'    Positive exact
00000818  BFFFFFFF E0000000                           918          DC    X'BFFFFFFFE0000000'    Negative exact
                                                      919 *
                                                      920 * Tie odd - rounds up    ..  1.999999940395355224609375
                                                      921 * rounds up to              ..  2.0
                                                      922 * rounds down to            ..  1.999999880790710449218750
00000820  3FFFFFFF F0000000                           923          DC    X'3FFFFFFFF0000000'    Positive tie odd
00000828  BFFFFFFF F0000000                           924          DC    X'BFFFFFFFF0000000'    Negative tie odd
                                                      925 *
                                                      926 * Tie even - rounds down ..  1.999999821186065673828125
                                                      927 * rounds up to              ..  1.999999880790710449218750
                                                      928 * rounds down to            ..  1.999999761581420898437500
00000830  3FFFFFFF D0000000                           929          DC    X'3FFFFFFFD0000000'    Positive tie even
00000838  BFFFFFFF D0000000                           930          DC    X'BFFFFFFFD0000000'    Negative tie even
                                                      931 *
                                                      932 * False exact 1.999999881722032801789623590593691915273666381835937500
                                                      933 * ..rounds up to       2.0
                                                      934 * ..rounds down to     1.999999880790710449218750
00000840  3FFFFFFF E03FFFFF                           935          DC    X'3FFFFFFFE03FFFFF'    Positive false exact
00000848  BFFFFFFF E03FFFFF                           936          DC    X'BFFFFFFFE03FFFFF'    Negative false exact
                                                      937 *
                                                      938 * Nearest is towards zero: 1.999999881256371736526489257812500
                                                      939 * ..rounds up to           2.0
                                                      940 * ..rounds down to         1.999999880790710449218750
00000850  3FFFFFFF E0200000                           941          DC    X'3FFFFFFFE0200000'    Positive zero closer
00000858  BFFFFFFF E0200000                           942          DC    X'BFFFFFFFE0200000'    Negative zero closer
                                                      943 *
                                                      944 * Nearest is away from zero: 1.999999999068677425384521484375
                                                      945 * ..rounds up to             2.0
                                                      946 * ..rounds down to           1.999999880790710449218750
00000860  3FFFFFFF FFC00000                           947          DC    X'3FFFFFFFFFC00000'    Positive zero further
00000868  BFFFFFFF FFC00000                           948          DC    X'BFFFFFFFFFC00000'    Negative zero further
                                                      949 *
                                                      950 * Overflow test: 3.402823669209384256844427444746065018888E38
                                                      951 * ..rounds up to    Overflow
                                                      952 * ..rounds down to  3.402823466385288598117041834845169254400E38
00000870  47EFFFFF FFFFFFFF                           953          DC    X'47EFFFFFFFFFFFFF'    Positive oveflow test
00000878  C7EFFFFF FFFFFFFF                           954          DC    X'C7EFFFFFFFFFFFFF'    Negative oveflow test
                                                      955 *
                                                      956 * Underflow test:  7.006492321624085354618647916449581...E-46
                                                      957 * ..rounds up to   1.401298464324817070923729583289910...E-45
                                                      958 *                     represented in short bfp as a tiny.
                                                      959 * ..rounds down to     underflow (but exact)
00000880  36900000 00000000                           960          DC    X'3690000000000000'    Positive magnitude underflow
00000888  B6900000 00000000                           961          DC    X'B690000000000000'    Negative magnitude underflow
                            00000080  00000001    962 LTOSRMCT EQU   *-LTOSINRM   Count of long BFP rounding tests * 8
                                                      964 *
                                                      965 * Extended to short basic tests, which tests trappable results, NaN
                                                      966 * propagation, and basic functionality.  The second part of this list
                                                      967 * is used for testing trappable results.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    968 *
00000890                                            969 XTOSIN   DS    0D        Inputs for extended to short BFP basic tests
00000890  00000000 00000000                         970          DC    X'00000000000000000000000000000000'         +0
000008A0  3FFF8000 00000000                         971          DC    X'3FFF8000000000000000000000000000'         +1.5
000008B0  BFFF8000 00000000                         972          DC    X'BFFF8000000000000000000000000000'         -1.5
000008C0  7FFF0100 00000000                         973          DC    X'7FFF0100000000000000000000000000'         SNaN
000008D0  7FFF8110 00000000                         974          DC    X'7FFF8110000000000000000000000000'         QNaN
                                                    975 * See rounding tests below for details on the following four
000008E0                                            976 XTOSINOU DS    0D            start of over/underflow test cases
000008E0  407EFFFF FFFFFFFF                         977          DC    X'407EFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    Pos. oveflow test
000008F0  C07EFFFF FFFFFFFF                         978          DC    X'C07EFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    Neg. oveflow test
00000900  407FFFFF FEFFFFFF                         979          DC    X'407FFFFFFEFFFFFFFFFFFFFFFFFFFFFF'    Pos. oveflow test
00000910  C07FFFFF FEFFFFFF                         980          DC    X'C07FFFFFFEFFFFFFFFFFFFFFFFFFFFFF'    Neg. oveflow test
00000920  3F690000 00000000                         981          DC    X'3F690000000000000000000000000000'    Pos. exact uflow
                                                    982 *                                                     ..result is tiny
00000930  BF690000 00000000                         983          DC    X'BF690000000000000000000000000000'    Neg. exact uflow
                                                    984 *                                                     ..result is tiny
00000940  407F0000 00000000                         985          DC    X'407F0000000000000000000000000000'    Pos. exact oflow
00000950  C07F0000 00000000                         986          DC    X'C07F0000000000000000000000000000'    Neg. exact oflow
                                                    987 *
                          000000D0  00000001        988 XTOSCT   EQU   *-XTOSIN     Count of extended BFP in list * 16
                          00000080  00000001        989 XTOSOUCT EQU   *-XTOSINOU   Ct * 16 of trappable over/underflow tests


                                                    991 *
                                                    992 * Test cases for exhaustive rounding mode tests of extended to short
                                                    993 * Load Rounded.
                                                    994 *
00000960                                            995 XTOSINRM DS    0D     Inputs for extended to short BFP rounding tests
                                                    996 *                x'80000000000000000000000000000000'  sign bit
                                                    997 *                x'7FFF0000000000000000000000000000'  Biased Exponent
                                                    998 *                x'0000FFFFFE0000000000000000000000'  Sig'd used in short
                                                    999 *                x'0000000001FC0000000000000000000'  Sig'd used in rndg
                                                   1000 *                x'000000000003FFFFFFFFFFFFFFFFFF'  'extra' sig'd bits
                                                   1001 *   Note: in the comments below, 'up' and 'down' mean 'toward
                                                   1002 *   higher magnitude' and 'toward lower magnitude' respectively and
                                                   1003 *   without regard to the sign, and rounding is to short BFP.
                                                   1004 *
                                                   1005 * Exact (fits in short BFP)   ..  1.99999988079071044921875
00000960  3FFFFFFF FE000000                        1006          DC    X'3FFFFFFFFE0000000000000000000000'    Pos. exact
00000970  BFFFFFFF FE000000                        1007          DC    X'BFFFFFFFFE0000000000000000000000'    Neg. exact
                                                   1008 *
                                                   1009 * Tie odd - rounds up    ..  1.99999994039535522460937 5
                                                   1010 * rounds up to              ..  2.0
                                                   1011 * rounds down to            ..  1.99999988079071044921875
00000980  3FFFFFFF FF000000                        1012          DC    X'3FFFFFFFFF0000000000000000000000'    Pos. tie odd
00000990  BFFFFFFF FF000000                        1013          DC    X'BFFFFFFFFF0000000000000000000000'    Neg. tie odd
                                                   1014 *
                                                   1015 * Tie even - rounds down ..  1.99999982118606567382812 5
                                                   1016 * rounds up to              ..  1.99999988079071044921875
                                                   1017 * rounds down to            ..  1.99999976158142089843 75
000009A0  3FFFFFFF FD000000                        1018          DC    X'3FFFFFFFFD0000000000000000000000'    Pos. tie even
000009B0  BFFFFFFF FD000000                        1019          DC    X'BFFFFFFFFD0000000000000000000000'    Neg. tie even
                                                   1020 *
                                                   1021 * False exact 1.99999988172203302383422851562499 98... (continues)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  1022 *               ..0740700556127641469440220574150 7... (continues)
                                                  1023 *               ..2681461898351784611804760061204433441162109375
                                                  1024 * ..rounds up to       2.0
                                                  1025 * ..rounds down to     1.99999988079071044921875
000009C0  3FFFFFFF FE03FFFF                       1026          DC    X'3FFFFFFFFE03FFFFFFFFFFFFFFFFFFFF'    Pos. false exact
000009D0  BFFFFFFF FE03FFFF                       1027          DC    X'BFFFFFFFFE03FFFFFFFFFFFFFFFFFFFF'    Neg. false exact
                                                  1028 *
                                                  1029 * Nearest is towards zero: 1.99999988125637173652648925781 25
                                                  1030 * ..rounds up to           2.0
                                                  1031 * ..rounds down to         1.99999988079071044921875
000009E0  3FFFFFFF FE020000                       1032          DC    X'3FFFFFFFFE020000000000000000000000'    Pos. zero closer
000009F0  BFFFFFFF FE020000                       1033          DC    X'BFFFFFFFFE020000000000000000000000'    Neg. zero closer
                                                  1034 *
                                                  1035 * Nearest is away from zero: 1.99999999906867742538452148437 5
                                                  1036 * ..rounds up to             2.0
                                                  1037 * ..rounds down to           1.99999988079071044921875
00000A00  3FFFFFFF FFFC0000                       1038          DC    X'3FFFFFFFFFFC0000000000000000000000'    Pos. zero further
00000A10  BFFFFFFF FFFC0000                       1039          DC    X'BFFFFFFFFFFC0000000000000000000000'    Neg. zero further
                                                  1040 *
                                                  1041 * Overflow test:    3.40282366920938463463374607431768178688E38
                                                  1042 * ..rounds up to    Overflow
                                                  1043 * ..rounds down to  3.40282346638528859811704183484516925440E38
00000A20  407EFFFF FFFFFFFF                       1044          DC    X'407EFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    Pos. oveflow test
00000A30  C07EFFFF FFFFFFFF                       1045          DC    X'C07EFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    Neg. oveflow test
                                                  1046 *
                                                  1047 * Underflow test:   7.0064923216240853546186479164495 8...E-46
                                                  1048 * ..rounds up to    1.4012984643248170709237295832899 1...E-45
                                                  1049 *                    represented in short bfp as a tiny.
                                                  1050 * ..rounds down to  Underflow (but exact)
00000A40  3F690000 00000000                       1051          DC    X'3F690000000000000000000000000000'    Pos. exact u-flow
                                                  1052 *                                                     ..result is tiny
00000A50  BF690000 00000000                       1053          DC    X'BF690000000000000000000000000000'    Neg. exact u-flow
                                                  1054 *                                                     ..result is tiny
                            00000100  00000001    1055 XTOSRMCT EQU   *-XTOSINRM   Count of extended BFP rounding tests * 16
                                                  1056 *
                                                  1057 * Extended to long basic tests, which tests trappable results, NaN
                                                  1058 * propagation, and basic functionality.  The second part of this list
                                                  1059 * is used for testing trappable results.
                                                  1060 *
00000A60                                          1061 XTOLIN   DS    0D        Inputs for extended to long BFP basic tests
00000A60  00000000 00000000                       1062          DC    X'00000000000000000000000000000000'        +0
00000A70  3FFF8000 00000000                       1063          DC    X'3FFF8000000000000000000000000000'        +1.5
00000A80  BFFF8000 00000000                       1064          DC    X'BFFF8000000000000000000000000000'        -1.5
00000A90  7FFF0100 00000000                       1065          DC    X'7FFF0100000000000000000000000000'        SNaN
00000AA0  7FFF8110 00000000                       1066          DC    X'7FFF8110000000000000000000000000'        QNaN
                                                  1067 * See rounding tests below for details on the following four
00000AB0                                          1068 XTOLINOU DS    0D       Start of trappable over/underflow test cases
00000AB0  43FEFFFF FFFFFFFF                       1069          DC    X'43FEFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    Pos. oveflow test
00000AC0  C3FEFFFF FFFFFFFF                       1070          DC    X'C3FEFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    Neg. oveflow test
00000AD0  43FFFFFF FFFFFFFF                       1071          DC    X'43FFFFFFFFFFFFFF7FFFFFFFFFFFFFFF'    Pos. oveflow test
00000AE0  C3FFFFFF FFFFFFFF                       1072          DC    X'C3FFFFFFFFFFFFFF7FFFFFFFFFFFFFFF'    Neg. oveflow test
00000AF0  3BCC0000 00000000                       1073          DC    X'3BCC0000000000000000000000000000'    Pos. underflow
                                                  1074 *                                                     ..result is tiny
00000B00  BBCC0000 00000000                       1075          DC    X'BBCC0000000000000000000000000000'    Neg. underflow
                                                  1076 *                                                     ..result is tiny
00000B10  43FF0000 00000000                       1077          DC    X'43FF0000000000000000000000000000'    Pos. exact o-flow
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
00000B20  C3FF0000 00000000                       1078          DC    X'C3FF0000000000000000000000000000'    Neg. exact o-flow
                             000000D0  00000001   1079 XTOLCT   EQU   *-XTOLIN     Count of extended BFP in list * 16
                             00000080  00000001   1080 XTOLOUCT EQU   *-XTOLINOU   Ct * 16 of trappable over/underflow tests
                                                  1081 *
                                                  1082 * Test cases for exhaustive rounding mode tests of long to short
                                                  1083 * Load Rounded.
                                                  1084 *
00000B30                                          1085 XTOLINRM DS    0D     Inputs for extended to short BFP rounding tests
                                                  1086 *              x'80000000000000000000000000000000'  sign bit
                                                  1087 *              x'7FFF0000000000000000000000000000'  Biased Exponent
                                                  1088 *              x'0000FFFFFFFFFFFF000000000000000'  Sig'd used in long
                                                  1089 *              x'00000000000000000FFC000000000000'  Sig'd used in rndg
                                                  1090 *              x'00000000000000000003FFFFFFFFFFFF'  'extra' sig'd bits
                                                  1091 *
                                                  1092 *   Note: in the comments below, 'up' and 'down' mean 'toward
                                                  1093 *   higher magnitude' and 'toward lower magnitude' respectively and
                                                  1094 *   without regard to the sign, and rounding is to short BFP.
                                                  1095 *
                                                  1096 *
                                                  1097 * Exact (fits in short BFP)
                                                  1098 * ..  1.99999999999999977795539507496869191527366638183593 75
                                                  1099 *
00000B30  3FFFFFFF FFFFFFFF                       1100          DC    X'3FFFFFFFFFFFFFFF000000000000000'    Pos. exact
00000B40  BFFFFFFF FFFFFFFF                       1101          DC    X'BFFFFFFFFFFFFFFF000000000000000'    Neg. exact
                                                  1102 *
                                                  1103 *
                                                  1104 * Tie odd - rounds up
                                                  1105 * ..  1.99999999999999988897769753748434595763683319091796875
                                                  1106 * rounds up to                ..  2.0
                                                  1107 * rounds down to
                                                  1108 * ..  1.99999999999999977795539507496869191527366638183593 75
                                                  1109 *
00000B50  3FFFFFFF FFFFFFFF                       1110          DC    X'3FFFFFFFFFFFFFFF800000000000000'    Pos. tie odd
00000B60  BFFFFFFF FFFFFFFF                       1111          DC    X'BFFFFFFFFFFFFFFF800000000000000'    Neg. tie odd
                                                  1112 *
                                                  1113 *
                                                  1114 * Tie even - rounds down
                                                  1115 * ..  1.99999999999999966693309261245303787291049957275390625
                                                  1116 * rounds up to
                                                  1117 * ..  1.99999999999999977795539507496869191527366638183593 75
                                                  1118 * rounds down to
                                                  1119 * ..  1.99999999999999955591079014993738383054733276367 1875
                                                  1120 *
00000B70  3FFFFFFF FFFFFFFF                       1121          DC    X'3FFFFFFFFFFFFFFE800000000000000'    Pos. tie even
00000B80  BFFFFFFF FFFFFFFF                       1122          DC    X'BFFFFFFFFFFFFFFE800000000000000'    Neg. tie even
                                                  1123 *
                                                  1124 *
                                                  1125 * False exact 1.99999988172203302383422851562499 98... (continues)
                                                  1126 *               ..07407005561276414694402205741507... (continues)
                                                  1127 *               ..26814618983517846118047600612044334411621093 75
                                                  1128 * ..rounds up to       2.0
                                                  1129 * ..rounds down to
                                                  1130 * ..  1.99999999999999977795539507496869191527366638183593 75
                                                  1131 *
00000B90  3FFFFFFF FFFFFFFF                       1132          DC    X'3FFFFFFFFFFFFFFF003FFFFFFFFFFF'    Pos. false exact
00000BA0  BFFFFFFF FFFFFFFF                       1133          DC    X'BFFFFFFFFFFFFFFF003FFFFFFFFFFF'    Neg. false exact
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  1134 *
                                                  1135 *
                                                  1136 * Nearest is towards zero:
                                                  1137 *  .  1.99999999999999977817223550946579280207515694200992584228515625
                                                  1138 * ..rounds up to           2.0
                                                  1139 * ..rounds down to
                                                  1140 *  .  1.99999999999999977795539507496869191527366638183593 75
                                                  1141 *
00000BB0  3FFFFFFF FFFFFFFF                       1142          DC    X'3FFFFFFFFFFFFFFF004000000000000'    Pos. zero closer
00000BC0  BFFFFFFF FFFFFFFF                       1143          DC    X'BFFFFFFFFFFFFFFF004000000000000'    Neg. zero closer
                                                  1144 *
                                                  1145 * Nearest is away from zero:
                                                  1146 *  .  1.99999999999999997224442438437108648940920829772949218 75
                                                  1147 * ..rounds up to             2.0
                                                  1148 * ..rounds down to
                                                  1149 *  .  1.99999999999999955591079014993738383054733276367187 5
                                                  1150 *
00000BD0  3FFFFFFF FFFFFFFF                       1151          DC    X'3FFFFFFFFFFFFFFFE00000000000000'    Pos. zero further
00000BE0  BFFFFFFF FFFFFFFF                       1152          DC    X'BFFFFFFFFFFFFFFFE00000000000000'    Neg. zero further
00000BF0                                          1153          DS    0D           required by asma for following EQU to work.
                                                  1154 *
                                                  1155 * Overflow test:    1.797693134862315708145274237317043...E308
                                                  1156 * ..rounds up to    Overflow
                                                  1157 * ..rounds down to  1.797693134862315907729305190789024...E308
00000BF0  43FEFFFF FFFFFFFF                       1158          DC    X'43FEFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    Pos. oveflow test
00000C00  C3FEFFFF FFFFFFFF                       1159          DC    X'C3FEFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    Neg. oveflow test
                                                  1160 *
                                                  1161 * Underflow test:   2.4703282292062327208828439643411 0...E-324
                                                  1162 * ..rounds up to    4.9406564584124654417656879286822 1...E-324
                                                  1163 * ..rounds down to  Underflow
00000C10  3BCC0000 00000000                       1164          DC    X'3BCC0000000000000000000000000000'    Pos. tie odd
                                                  1165 *                                                     ..result is tiny
00000C20  BBCC0000 00000000                       1166          DC    X'BBCC0000000000000000000000000000'    Neg. tie odd
                                                  1167 *                                                     ..result is tiny
                            00000100  00000001    1168 XTOLRMCT EQU   *-XTOLINRM   Count of extended BFP rounding tests * 16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          1170 ************************************************************************
                                          1171 *                   ACTUAL results saved here
                                          1172 ************************************************************************
                                          1173 *
                                          1174 *                Locations for ACTUAL results
                                          1175 *
                                          1176 *
                          00001000  00000000 1177 LTOSOUT  EQU   BFPLDRND+X'1000'    Short BFP rounded from long
                                          1178 *                                    ..9 pairs used, room for 16
                          00001080  00000000 1179 LTOSFLGS EQU   BFPLDRND+X'1080'    FPCR flags and DXC from above
                                          1180 *                                    ..9 pairs used, room for 16
                          00001100  00000000 1181 LTOSRMO  EQU   BFPLDRND+X'1100'    Short BFP result rounding tests
                                          1182 *                                    ..14 sets used, room for 21
                          00001500  00000000 1183 LTOSRMOF EQU   BFPLDRND+X'1500'    FPCR flags and DXC from above
                                          1184 *                                    ..14 sets used, room for 21
                                          1185 *
                          00001900  00000000 1186 XTOSOUT  EQU   BFPLDRND+X'1900'    Short BFP rounded from extended
                                          1187 *                                    ..5 pairs used, room for 16
                          00001980  00000000 1188 XTOSFLGS EQU   BFPLDRND+X'1980'    FPCR flags and DXC from above
                                          1189 *                                    ..5 pairs used, room for 16
                          00001A00  00000000 1190 XTOSRMO  EQU   BFPLDRND+X'1A00'    Short BFP rounding tests
                                          1191 *                                    ..14 sets used, room for 21
                          00001E00  00000000 1192 XTOSRMOF EQU   BFPLDRND+X'1E00'    FPCR flags and DXC from above
                                          1193 *                                    ..14 sets used, room for 21
                                          1194
                                          1195 *
                          00002200  00000000 1196 XTOLOUT  EQU   BFPLDRND+X'2200'    Long BFP rounded from extended
                                          1197 *                                    ..5 pairs used, room for 16
                          00002300  00000000 1198 XTOLFLGS EQU   BFPLDRND+X'2300'    FPCR flags and DXC from above
                                          1199 *                                    ..5 pairs used, room for 32
                          00002400  00000000 1200 XTOLRMO  EQU   BFPLDRND+X'2400'    Long BFP rounding tests
                                          1201 *                                    ..12 results used, room for 22
                          00002B00  00000000 1202 XTOLRMOF EQU   BFPLDRND+X'2B00'    FPCR flags and DXC from above
                                          1203 *                                    ..12 results used, room for 21
                                          1204 *
                          00003000  00000000 1205 LTOSOUO  EQU   BFPLDRND+X'3000'    Long BFP trappable o/uflow tests
                                          1206 *                                    ..4 results used, room for 16
                          00003080  00000000 1207 LTOSOUOF EQU   BFPLDRND+X'3080'    FPCR flags and DXC from above
                                          1208 *
                          00003100  00000000 1209 XTOSOUO  EQU   BFPLDRND+X'3100'    Extd BFP trappable o/uflow tests
                                          1210 *                                    ..4 results used, room for 8
                          00003180  00000000 1211 XTOSOUOF EQU   BFPLDRND+X'3180'    FPCR flags and DXC from above
                                          1212 *
                          00003200  00000000 1213 XTOLOUO  EQU   BFPLDRND+X'3200'    Extd BFP trappable o/uflow tests
                                          1214 *                                    ..4 results used, room for 8
                          00003280  00000000 1215 XTOLOUOF EQU   BFPLDRND+X'3280'    FPCR flags and DXC from above
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                  1217 ********************************************************************
                                                  1218 *                      EXPECTED results
                                                  1219 ********************************************************************
                                                  1220 *
00000C30                      00000C30  00004000  1221          ORG   BFPLDRND+X'4000'   (past end of actual results)
                                                  1222 *
                              00004000  00000001  1223 LTOSOUT_GOOD EQU *
00004000  D3C5C4C2 D9409985                       1224  DC CL48'LEDBR result pairs 1-2'
00004030  00000000 00000000                       1225  DC XL16'0000000000000003FC000003FC00000'
00004040  D3C5C4C2 D9409985                       1226  DC CL48'LEDBR result pairs 3-4'
00004070  BFC00000 BFC00000                       1227  DC XL16'BFC00000BFC000007FC0800000000000'
00004080  D3C5C4C2 D9409985                       1228  DC CL48'LEDBR result pairs 5-6'
000040B0  7FC08800 7FC08800                       1229  DC XL16'7FC088007FC088007F80000027F00000'
000040C0  D3C5C4C2 D9409985                       1230  DC CL48'LEDBR result pairs 7-8'
000040F0  FF800000 A7F00000                       1231  DC XL16'FF800000A7F000007F80000027FFFFFF'
00004100  D3C5C4C2 D9409985                       1232  DC CL48'LEDBR result pairs 9-10'
00004130  FF800000 A7FFFFFF                       1233  DC XL16'FF800000A7FFFFFF0000000056900000'
00004140  D3C5C4C2 D9409985                       1234  DC CL48'LEDBR result pairs 11-12'
00004170  80000000 D6900000                       1235  DC XL16'80000000D69000007F80000027F00000'
00004180  D3C5C4C2 D9409985                       1236  DC CL48'LEDBR result pair 13'
000041B0  FF800000 A7F00000                       1237  DC XL16'FF800000A7F00000000000000000000000'
                              00000007  00000001  1238 LTOSOUT_NUM EQU (*-LTOSOUT_GOOD)/64
                                                  1239 *
                                                  1240 *
                              000041C0  00000001  1241 LTOSFLGS_GOOD EQU *
000041C0  D3C5C4C2 D940C6D7                       1242  DC CL48'LEDBR FPCR pairs 1-2'
000041F0  00000000 F8000000                       1243  DC XL16'00000000F800000000000000F8000000'
00004200  D3C5C4C2 D940C6D7                       1244  DC CL48'LEDBR FPCR pairs 3-4'
00004230  00000000 F8000000                       1245  DC XL16'00000000F800000000800000F8008000'
00004240  D3C5C4C2 D940C6D7                       1246  DC CL48'LEDBR FPCR pairs 5-6'
00004270  00000000 F8000000                       1247  DC XL16'00000000F800000000280000F8002C00'
00004280  D3C5C4C2 D940C6D7                       1248  DC CL48'LEDBR FPCR pairs 7-8'
000042B0  00280000 F8002C00                       1249  DC XL16'00280000F8002C0000280000F8002800'
000042C0  D3C5C4C2 D940C6D7                       1250  DC CL48'LEDBR FPCR pairs 9-10'
000042F0  00280000 F8002800                       1251  DC XL16'00280000F8002800001800000F8001000'
00004300  D3C5E7C2 D940C6D7                       1252  DC CL48'LEXBR FPCR pairs 11-12'
00004330  00180000 F8001000                       1253  DC XL16'00180000F8001000002800000F8002000'
00004340  D3C5E7C2 D940C6D7                       1254  DC CL48'LEXBR FPCR pair 13'
00004370  00280000 F8002000                       1255  DC XL16'00280000F8002000000000000000000000'
                              00000007  00000001  1256 LTOSFLGS_NUM EQU (*-LTOSFLGS_GOOD)/64
                                                  1257 *
                                                  1258 *
                              00004380  00000001  1259 LTOSRMO_GOOD EQU *
00004380  D3C5C4C2 D9C1404E                       1260  DC CL48'LEDBRA +exact FPCR modes 1-3, 7'
000043B0  3FFFFFFF 3FFFFFFF                       1261  DC XL16'3FFFFFFF3FFFFFFF3FFFFFFF3FFFFFFF'
000043C0  D3C5C4C2 D9C1404E                       1262  DC CL48'LEDBRA +exact M3 modes 1, 3-5'
000043F0  3FFFFFFF 3FFFFFFF                       1263  DC XL16'3FFFFFFF3FFFFFFF3FFFFFFF3FFFFFFF'
00004400  D3C5C4C2 D9C1404E                       1264  DC CL48'LEDBRA +exact M3 modes 6, 7'
00004430  3FFFFFFF 3FFFFFFF                       1265  DC XL16'3FFFFFFF3FFFFFFF0000000000000000'
00004440  D3C5C4C2 D9C14060                       1266  DC CL48'LEDBRA -exact FPCR modes 1-3, 7'
00004470  BFFFFFFF BFFFFFFF                       1267  DC XL16'BFFFFFFFBFFFFFFFBFFFFFFFBFFFFFFF'
00004480  D3C5C4C2 D9C14060                       1268  DC CL48'LEDBRA -exact M3 modes 1, 3-5'
000044B0  BFFFFFFF BFFFFFFF                       1269  DC XL16'BFFFFFFFBFFFFFFFBFFFFFFFBFFFFFFF'
000044C0  D3C5C4C2 D9C14060                       1270  DC CL48'LEDBRA -exact M3 modes 6, 7'
000044F0  BFFFFFFF BFFFFFFF                       1271  DC XL16'BFFFFFFFBFFFFFFF0000000000000000'
00004500  D3C5C4C2 D9C1404E                       1272  DC CL48'LEDBRA +tie odd FPCR modes 1-3, 7'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00004530  3FFFFFFF 40000000                         1273  DC XL16'3FFFFFFF400000003FFFFFF3FFFFFF'
00004540  D3C5C4C2 D9C1404E                         1274  DC CL48'LEDBRA +tie odd M3 modes 1, 3-5'
00004570  40000000 3FFFFFFF                         1275  DC XL16'400000003FFFFFF400000003FFFFFF'
00004580  D3C5C4C2 D9C1404E                         1276  DC CL48'LEDBRA +tie odd M3 modes 6, 7'
000045B0  40000000 3FFFFFFF                         1277  DC XL16'400000003FFFFFF0000000000000000'
000045C0  D3C5C4C2 D9C14060                         1278  DC CL48'LEDBRA -tie odd FPCR modes 1-3, 7'
000045F0  BFFFFFFF BFFFFFFF                         1279  DC XL16'BFFFFFFFBFFFFFFFC0000000BFFFFFFF'
00004600  D3C5C4C2 D9C14060                         1280  DC CL48'LEDBRA -tie odd M3 modes 1, 3-5'
00004630  C0000000 BFFFFFFF                         1281  DC XL16'C0000000BFFFFFFFC0000000BFFFFFFF'
00004640  D3C5C4C2 D9C14060                         1282  DC CL48'LEDBRA -tie odd M3 modes 6, 7'
00004670  BFFFFFFF C0000000                         1283  DC XL16'BFFFFFFFC00000000000000000000000'
00004680  D3C5C4C2 D9C1404E                         1284  DC CL48'LEDBRA +tie even FPCR modes 1-3, 7'
000046B0  3FFFFFFE 3FFFFFFF                         1285  DC XL16'3FFFFFFE3FFFFFFF3FFFFFFE3FFFFFFF'
000046C0  D3C5C4C2 D9C1404E                         1286  DC CL48'LEDBRA +tie even M3 modes 1, 3-5'
000046F0  3FFFFFFF 3FFFFFFF                         1287  DC XL16'3FFFFFFF3FFFFFFF3FFFFFFE3FFFFFFE'
00004700  D3C5C4C2 D9C1404E                         1288  DC CL48'LEDBRA +tie even M3 modes 6, 7'
00004730  3FFFFFFF 3FFFFFFE                         1289  DC XL16'3FFFFFFF3FFFFFFE0000000000000000'
00004740  D3C5C4C2 D9C14060                         1290  DC CL48'LEDBRA -tie even FPCR modes 1-3, 7'
00004770  BFFFFFFE BFFFFFFE                         1291  DC XL16'BFFFFFFEBFFFFFFEBFFFFFFFBFFFFFFF'
00004780  D3C5C4C2 D9C14060                         1292  DC CL48'LEDBRA -tie even M3 modes 1, 3-5'
000047B0  BFFFFFFF BFFFFFFF                         1293  DC XL16'BFFFFFFFBFFFFFFFBFFFFFFEBFFFFFFE'
000047C0  D3C5C4C2 D9C14060                         1294  DC CL48'LEDBRA -tie even M3 modes 6, 7'
000047F0  BFFFFFFE BFFFFFFF                         1295  DC XL16'BFFFFFFEBFFFFFFF0000000000000000'
00004800  D3C5C4C2 D9C1404E                         1296  DC CL48'LEDBRA +false exact FPCR modes 1-3, 7'
00004830  3FFFFFFF 40000000                         1297  DC XL16'3FFFFFFF400000003FFFFFF3FFFFFF'
00004840  D3C5C4C2 D9C1404E                         1298  DC CL48'LEDBRA +false exact M3 modes 1, 3-5'
00004870  3FFFFFFF 3FFFFFFF                         1299  DC XL16'3FFFFFFF3FFFFFFF3FFFFFF3FFFFFFF'
00004880  D3C5C4C2 D9C1404E                         1300  DC CL48'LEDBRA +false exact M3 modes 6, 7'
000048B0  40000000 3FFFFFFF                         1301  DC XL16'400000003FFFFFF0000000000000000'
000048C0  D3C5C4C2 D9C14060                         1302  DC CL48'LEDBRA -false exact FPCR modes 1-3, 7'
000048F0  BFFFFFFF BFFFFFFF                         1303  DC XL16'BFFFFFFFBFFFFFFFC0000000BFFFFFFF'
00004900  D3C5C4C2 D9C14060                         1304  DC CL48'LEDBRA -false exact M3 modes 1, 3-5'
00004930  BFFFFFFF BFFFFFFF                         1305  DC XL16'BFFFFFFFBFFFFFFFBFFFFFFFBFFFFFFF'
00004940  D3C5C4C2 D9C14060                         1306  DC CL48'LEDBRA -false exact M3 modes 6, 7'
00004970  BFFFFFFF C0000000                         1307  DC XL16'BFFFFFFFC00000000000000000000000'
00004980  D3C5C4C2 D9C1404E                         1308  DC CL48'LEDBRA +near zero FPCR modes 1-3, 7'
000049B0  3FFFFFFF 40000000                         1309  DC XL16'3FFFFFFF400000003FFFFFF3FFFFFF'
000049C0  D3C5C4C2 D9C1404E                         1310  DC CL48'LEDBRA +near zero M3 modes 1, 3-5'
000049F0  3FFFFFFF 3FFFFFFF                         1311  DC XL16'3FFFFFFF3FFFFFFF3FFFFFFF3FFFFFFF'
00004A00  D3C5C4C2 D9C1404E                         1312  DC CL48'LEDBRA +near zero M3 modes 6, 7'
00004A30  40000000 3FFFFFFF                         1313  DC XL16'400000003FFFFFF0000000000000000'
00004A40  D3C5C4C2 D9C14060                         1314  DC CL48'LEDBRA -near zero FPCR modes 1-3, 7'
00004A70  BFFFFFFF BFFFFFFF                         1315  DC XL16'BFFFFFFFBFFFFFFFC0000000BFFFFFFF'
00004A80  D3C5C4C2 D9C14060                         1316  DC CL48'LEDBRA -near zero M3 modes 1, 3-5'
00004AB0  BFFFFFFF BFFFFFFF                         1317  DC XL16'BFFFFFFFBFFFFFFFBFFFFFFFBFFFFFFF'
00004AC0  D3C5C4C2 D9C14060                         1318  DC CL48'LEDBRA -near zero M3 modes 6, 7'
00004AF0  BFFFFFFF C0000000                         1319  DC XL16'BFFFFFFFC00000000000000000000000'
00004B00  D3C5C4C2 D9C1404E                         1320  DC CL48'LEDBRA +near +inf FPCR modes 1-3, 7'
00004B30  3FFFFFFF 40000000                         1321  DC XL16'3FFFFFFF400000003FFFFFF3FFFFFF'
00004B40  D3C5C4C2 D9C1404E                         1322  DC CL48'LEDBRA +near +inf M3 modes 1, 3-5'
00004B70  40000000 3FFFFFFF                         1323  DC XL16'400000003FFFFFF400000003FFFFFF'
00004B80  D3C5C4C2 D9C1404E                         1324  DC CL48'LEDBRA +near +inf M3 modes 6, 7'
00004BB0  40000000 3FFFFFFF                         1325  DC XL16'400000003FFFFFF0000000000000000'
00004BC0  D3C5C4C2 D9C14060                         1326  DC CL48'LEDBRA -near -inf FPCR modes 1-3, 7'
00004BF0  BFFFFFFF BFFFFFFF                         1327  DC XL16'BFFFFFFFBFFFFFFFC0000000BFFFFFFF'
00004C00  D3C5C4C2 D9C14060                         1328  DC CL48'LEDBRA -near -inf M3 modes 1, 3-5'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004C30  C0000000 BFFFFFFF                        1329  DC XL16'C0000000BFFFFFFFC0000000BFFFFFFF'
00004C40  D3C5C4C2 D9C14060                        1330  DC CL48'LEDBRA -near -inf M3 modes 6, 7'
00004C70  BFFFFFFF C0000000                        1331  DC XL16'BFFFFFFFC0000000000000000000000'
00004C80  D3C5C4C2 D9C1404E                        1332  DC CL48'LEDBRA +overflow FPCR modes 1-3, 7'
00004CB0  7F7FFFFF 7F800000                        1333  DC XL16'7F7FFFFF7F8000007F7FFFF7F7FFFFF'
00004CC0  D3C5C4C2 D9C1404E                        1334  DC CL48'LEDBRA +overflow M3 modes 1, 3-5'
00004CF0  7F800000 7F7FFFFF                        1335  DC XL16'7F8000007F7FFFF7F8000007F7FFFF'
00004D00  D3C5C4C2 D9C1404E                        1336  DC CL48'LEDBRA +overflow M3 modes 6, 7'
00004D30  7F800000 7F7FFFFF                        1337  DC XL16'7F8000007F7FFFF0000000000000000'
00004D40  D3C5C4C2 D9C14060                        1338  DC CL48'LEDBRA -overflow FPCR modes 1-3, 7'
00004D70  FF7FFFFF FF7FFFFF                        1339  DC XL16'FF7FFFFFF7FFFFFFF800000FF7FFFFF'
00004D80  D3C5C4C2 D9C14060                        1340  DC CL48'LEDBRA -overflow M3 modes 1, 3-5'
00004DB0  FF800000 FF7FFFFF                        1341  DC XL16'FF800000FF7FFFFFF800000FF7FFFFF'
00004DC0  D3C5C4C2 D9C14060                        1342  DC CL48'LEDBRA -overflow M3 modes 6, 7'
00004DF0  FF7FFFFF FF800000                        1343  DC XL16'FF7FFFFFF8000000000000000000000'
00004E00  D3C5C4C2 D9C1404E                        1344  DC CL48'LEDBRA +tiny tie odd FPCR modes 1-3, 7'
00004E30  00000000 00000001                        1345  DC XL16'00000000000000010000000000000001'
00004E40  D3C5C4C2 D9C1404E                        1346  DC CL48'LEDBRA +tiny tie odd M3 modes 1, 3-5'
00004E70  00000001 00000001                        1347  DC XL16'00000001000000010000000000000000'
00004E80  D3C5C4C2 D9C1404E                        1348  DC CL48'LEDBRA +tiny tie odd M3 modes 6, 7'
00004EB0  00000001 00000000                        1349  DC XL16'00000001000000000000000000000000'
00004EC0  D3C5C4C2 D9C14060                        1350  DC CL48'LEDBRA -tiny tie odd FPCR modes 1-3, 7'
00004EF0  80000000 80000000                        1351  DC XL16'80000000800000008000000180000001'
00004F00  D3C5C4C2 D9C14060                        1352  DC CL48'LEDBRA -tiny tie odd M3 modes 1, 3-5'
00004F30  80000001 80000001                        1353  DC XL16'80000001800000018000000080000000'
00004F40  D3C5C4C2 D9C14060                        1354  DC CL48'LEDBRA -tiny tie odd M3 modes 6, 7'
00004F70  80000000 80000001                        1355  DC XL16'80000000800000010000000000000000'
                             00000030  00000001   1356 LTOSRMO_NUM EQU (*-LTOSRMO_GOOD)/64
                                                1357 *
                                                1358 *
                             00004F80  00000001   1359 LTOSRMOF_GOOD EQU *
00004F80  D3C5C4C2 D9C1404E                        1360  DC CL48'LEDBRA +exact FPC modes 1-3, 7 FCPR'
00004FB0  00000001 00000002                        1361  DC XL16'00000001000000020000000300000007'
00004FC0  D3C5C4C2 D9C1404E                        1362  DC CL48'LEDBRA +exact M3 modes 1, 3-5 FPCR'
00004FF0  00000000 00000000                        1363  DC XL16'00000000000000000000000000000000'
00005000  D3C5C4C2 D9C1404E                        1364  DC CL48'LEDBRA +exact M3 modes 6, 7 FCPR'
00005030  00000000 00000000                        1365  DC XL16'00000000000000000000000000000000'
00005040  D3C5C4C2 D9C14060                        1366  DC CL48'LEDBRA -exact FPC modes 1-3, 7 FCPR'
00005070  00000001 00000002                        1367  DC XL16'00000001000000020000000300000007'
00005080  D3C5C4C2 D9C14060                        1368  DC CL48'LEDBRA -exact M3 modes 1, 3-5 FPCR'
000050B0  00000000 00000000                        1369  DC XL16'00000000000000000000000000000000'
000050C0  D3C5C4C2 D9C14060                        1370  DC CL48'LEDBRA -exact M3 modes 6, 7 FCPR'
000050F0  00000000 00000000                        1371  DC XL16'00000000000000000000000000000000'
00005100  D3C5C4C2 D9C1404E                        1372  DC CL48'LEDBRA +tie odd FPC modes 1-3, 7 FCPR'
00005130  00000001 00000002                        1373  DC XL16'00000001000000020000000300000007'
00005140  D3C5C4C2 D9C1404E                        1374  DC CL48'LEDBRA +tie odd M3 modes 1, 3-5 FPCR'
00005170  00080000 00080000                        1375  DC XL16'00080000000800000008000000080000'
00005180  D3C5C4C2 D9C1404E                        1376  DC CL48'LEDBRA +tie odd M3 modes 6, 7 FCPR'
000051B0  00080000 00080000                        1377  DC XL16'00080000000800000000000000000000'
000051C0  D3C5C4C2 D9C14060                        1378  DC CL48'LEDBRA -tie odd FPC modes 1-3, 7 FCPR'
000051F0  00000001 00000002                        1379  DC XL16'00000001000000020000000300000007'
00005200  D3C5C4C2 D9C14060                        1380  DC CL48'LEDBRA -tie odd M3 modes 1, 3-5 FPCR'
00005230  00080000 00080000                        1381  DC XL16'00080000000800000008000000080000'
00005240  D3C5C4C2 D9C14060                        1382  DC CL48'LEDBRA -tie odd M3 modes 6, 7 FCPR'
00005270  00080000 00080000                        1383  DC XL16'00080000000800000000000000000000'
00005280  D3C5C4C2 D9C1404E                        1384  DC CL48'LEDBRA +tie even FPC modes 1-3, 7 FCPR'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000052B0  00000001 00000002                      1385  DC XL16'00000001000000020000000300000007'
000052C0  D3C5C4C2 D9C1404E                      1386  DC CL48'LEDBRA +tie even M3 modes 1, 3-5 FPCR'
000052F0  00080000 00080000                      1387  DC XL16'00080000000800000008000000080000'
00005300  D3C5C4C2 D9C1404E                      1388  DC CL48'LEDBRA +tie even M3 modes 6, 7 FCPR'
00005330  00080000 00080000                      1389  DC XL16'00080000000800000000000000000000'
00005340  D3C5C4C2 D9C14060                      1390  DC CL48'LEDBRA -tie even FPC modes 1-3, 7 FCPR'
00005370  00000001 00000002                      1391  DC XL16'00000001000000020000000300000007'
00005380  D3C5C4C2 D9C14060                      1392  DC CL48'LEDBRA -tie even M3 modes 1, 3-5 FPCR'
000053B0  00080000 00080000                      1393  DC XL16'00080000000800000008000000080000'
000053C0  D3C5C4C2 D9C14060                      1394  DC CL48'LEDBRA -tie even M3 modes 6, 7 FCPR'
000053F0  00080000 00080000                      1395  DC XL16'00080000000800000000000000000000'
00005400  D3C5C4C2 D9C1404E                      1396  DC CL48'LEDBRA +false exact FPC modes 1-3, 7 FCPR'
00005430  00000001 00000002                      1397  DC XL16'00000001000000020000000300000007'
00005440  D3C5C4C2 D9C1404E                      1398  DC CL48'LEDBRA +false exact M3 modes 1, 3-5 FPCR'
00005470  00080000 00080000                      1399  DC XL16'00080000000800000008000000080000'
00005480  D3C5C4C2 D9C1404E                      1400  DC CL48'LEDBRA +false exact M3 modes 6, 7 FCPR'
000054B0  00080000 00080000                      1401  DC XL16'00080000000800000000000000000000'
000054C0  D3C5C4C2 D9C14060                      1402  DC CL48'LEDBRA -false exact FPC modes 1-3, 7 FCPR'
000054F0  00000001 00000002                      1403  DC XL16'00000001000000020000000300000007'
00005500  D3C5C4C2 D9C14060                      1404  DC CL48'LEDBRA -false exact M3 modes 1, 3-5 FPCR'
00005530  00080000 00080000                      1405  DC XL16'00080000000800000008000000080000'
00005540  D3C5C4C2 D9C14060                      1406  DC CL48'LEDBRA -false exact M3 modes 6, 7 FCPR'
00005570  00080000 00080000                      1407  DC XL16'00080000000800000000000000000000'
00005580  D3C5C4C2 D9C1404E                      1408  DC CL48'LEDBRA +near zero FPC modes 1-3, 7 FCPR'
000055B0  00000001 00000002                      1409  DC XL16'00000001000000020000000300000007'
000055C0  D3C5C4C2 D9C1404E                      1410  DC CL48'LEDBRA +near zero M3 modes 1, 3-5 FPCR'
000055F0  00080000 00080000                      1411  DC XL16'00080000000800000008000000080000'
00005600  D3C5C4C2 D9C1404E                      1412  DC CL48'LEDBRA +near zero M3 modes 6, 7 FCPR'
00005630  00080000 00080000                      1413  DC XL16'00080000000800000000000000000000'
00005640  D3C5C4C2 D9C14060                      1414  DC CL48'LEDBRA -near zero FPC modes 1-3, 7 FCPR'
00005670  00000001 00000002                      1415  DC XL16'00000001000000020000000300000007'
00005680  D3C5C4C2 D9C14060                      1416  DC CL48'LEDBRA -near zero M3 modes 1, 3-5 FPCR'
000056B0  00080000 00080000                      1417  DC XL16'00080000000800000008000000080000'
000056C0  D3C5C4C2 D9C14060                      1418  DC CL48'LEDBRA -near zero M3 modes 6, 7 FCPR'
000056F0  00080000 00080000                      1419  DC XL16'00080000000800000000000000000000'
00005700  D3C5C4C2 D9C1404E                      1420  DC CL48'LEDBRA +near +inf FPC modes 1-3, 7 FCPR'
00005730  00000001 00000002                      1421  DC XL16'00000001000000020000000300000007'
00005740  D3C5C4C2 D9C1404E                      1422  DC CL48'LEDBRA +near +inf M3 modes 1, 3-5 FPCR'
00005770  00080000 00080000                      1423  DC XL16'00080000000800000008000000080000'
00005780  D3C5C4C2 D9C1404E                      1424  DC CL48'LEDBRA +near +inf M3 modes 6, 7 FCPR'
000057B0  00080000 00080000                      1425  DC XL16'00080000000800000000000000000000'
000057C0  D3C5C4C2 D9C14060                      1426  DC CL48'LEDBRA -near -inf FPC modes 1-3, 7 FCPR'
000057F0  00000001 00000002                      1427  DC XL16'00000001000000020000000300000007'
00005800  D3C5C4C2 D9C14060                      1428  DC CL48'LEDBRA -near -inf M3 modes 1, 3-5 FPCR'
00005830  00080000 00080000                      1429  DC XL16'00080000000800000008000000080000'
00005840  D3C5C4C2 D9C14060                      1430  DC CL48'LEDBRA -near -inf M3 modes 6, 7 FCPR'
00005870  00080000 00080000                      1431  DC XL16'00080000000800000000000000000000'
00005880  D3C5C4C2 D9C1404E                      1432  DC CL48'LEDBRA +overflow FPCR modes 1-3, 7 FCPR'
000058B0  00000001 00200002                      1433  DC XL16'00000001002000020000000300000007'
000058C0  D3C5C4C2 D9C1404E                      1434  DC CL48'LEDBRA +overflow M3 modes 1, 3-5 FPCR'
000058F0  00280000 00080000                      1435  DC XL16'00280000000800000028000000080000'
00005900  D3C5C4C2 D9C1404E                      1436  DC CL48'LEDBRA +overflow M3 modes 6, 7 FCPR'
00005930  00280000 00080000                      1437  DC XL16'00280000000800000000000000000000'
00005940  D3C5C4C2 D9C14060                      1438  DC CL48'LEDBRA -overflow FPCR modes 1-3, 7 FCPR'
00005970  00000001 00000002                      1439  DC XL16'00000001000000020020000300000007'
00005980  D3C5C4C2 D9C14060                      1440  DC CL48'LEDBRA -overflow M3 modes 1, 3-5 FPCR'
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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000059B0  00280000 00080000                       1441  DC XL16'00280000000800000028000000080000'
000059C0  D3C5C4C2 D9C14060                       1442  DC CL48'LEDBRA -overflow M3 modes 6, 7 FPCR'
000059F0  00080000 00280000                       1443  DC XL16'00080000002800000000000000000000'
00005A00  D3C5C4C2 D9C1404E                       1444  DC CL48'LEDBRA +tiny tie odd FPCR modes 1-3, 7 FPCR'
00005A30  00100001 00100002                       1445  DC XL16'00100001001000020010000300100007'
00005A40  D3C5C4C2 D9C1404E                       1446  DC CL48'LEDBRA +tiny tie odd M3 modes 1, 3-5 FPCR'
00005A70  00180000 00180000                       1447  DC XL16'00180000018000000180000000180000'
00005A80  D3C5C4C2 D9C1404E                       1448  DC CL48'LEDBRA +tiny tie odd M3 modes 6, 7 FPCR'
00005AB0  00180000 00180000                       1449  DC XL16'00180000018000000000000000000000'
00005AC0  D3C5C4C2 D9C14060                       1450  DC CL48'LEDBRA -tiny tie odd FPCR modes 1-3, 7 FPCR'
00005AF0  00100001 00100002                       1451  DC XL16'00100001001000020010000300100007'
00005B00  D3C5C4C2 D9C14060                       1452  DC CL48'LEDBRA -tiny tie odd M3 modes 1, 3-5 FPCR'
00005B30  00180000 00180000                       1453  DC XL16'00180000018000000180000000180000'
00005B40  D3C5C4C2 D9C14060                       1454  DC CL48'LEDBRA -tiny tie odd M3 modes 6, 7 FPCR'
00005B70  00180000 00180000                       1455  DC XL16'00180000018000000000000000000000'
                           00000030  00000001   1456 LTOSRMOF_NUM EQU (*-LTOSRMOF_GOOD)/64
                                                1457 *
                                                1458 *
                           00005B80  00000001   1459 XTOSOUT_GOOD EQU *
00005B80  D3C5E7C2 D9409985                       1460  DC CL48'LEXBR result pairs 1-2'
00005BB0  00000000 00000000                       1461  DC XL16'0000000000000003FC000003FC00000'
00005BC0  D3C5E7C2 D9409985                       1462  DC CL48'LEXBR result pairs 3-4'
00005BF0  BFC00000 BFC00000                       1463  DC XL16'BFC00000BFC000007FC0800000000000'
00005C00  D3C5E7C2 D9409985                       1464  DC CL48'LEXBR result pairs 5-6'
00005C30  7FC08800 7FC08800                       1465  DC XL16'7FC088007FC088007F800000207F0000'
00005C40  D3C5E7C2 D9409985                       1466  DC CL48'LEXBR result pairs 7-8'
00005C70  FF800000 A07F0000                       1467  DC XL16'FF800000A07F00007F800000207FFFFF'
00005C80  D3C5E7C2 D9409985                       1468  DC CL48'LEXBR result pairs 9-10'
00005CB0  FF800000 A07FFFFF                       1469  DC XL16'FF800000A07FFFFF000000005F690000'
00005CC0  D3C5E7C2 D9409985                       1470  DC CL48'LEXBR result pair 11-12'
00005CF0  80000000 DF690000                       1471  DC XL16'80000000DF6900007F800000207F0000'
00005D00  D3C5E7C2 D9409985                       1472  DC CL48'LEXBR result pair 13'
00005D30  FF800000 A07F0000                       1473  DC XL16'FF800000A07F0000000000000000000'
                           00000007  00000001   1474 XTOSOUT_NUM EQU (*-XTOSOUT_GOOD)/64
                                                1475 *
                                                1476 *
                           00005D40  00000001   1477 XTOSFLGS_GOOD EQU *
00005D40  D3C5E7C2 D940C6D7                       1478  DC CL48'LEXBR FPCR pairs 1-2'
00005D70  00000000 F8000000                       1479  DC XL16'00000000F8000000000000000F8000000'
00005D80  D3C5E7C2 D940C6D7                       1480  DC CL48'LEXBR FPCR pairs 3-4'
00005DB0  00000000 F8000000                       1481  DC XL16'00000000F8000000000800000F8008000'
00005DC0  D3C5E7C2 D940C6D7                       1482  DC CL48'LEXBR FPCR pairs 5-6'
00005DF0  00000000 F8000000                       1483  DC XL16'00000000F8000000000280000F8002C00'
00005E00  D3C5E7C2 D940C6D7                       1484  DC CL48'LEXBR FPCR pairs 7-8'
00005E30  00280000 F8002C00                       1485  DC XL16'00280000F8002C0000280000F8002800'
00005E40  D3C5E7C2 D940C6D7                       1486  DC CL48'LEXBR FPCR pairs 9-10'
00005E70  00280000 F8002800                       1487  DC XL16'00280000F8002800001800000F8001000'
00005E80  D3C5E7C2 D940C6D7                       1488  DC CL48'LEXBR FPCR pairs 11-12'
00005EB0  00180000 F8001000                       1489  DC XL16'00180000F8001000002800000F8002000'
00005EC0  D3C5E7C2 D940C6D7                       1490  DC CL48'LEXBR FPCR pair 13'
00005EF0  00280000 F8002000                       1491  DC XL16'00280000F8002000000000000000000'
                           00000007  00000001   1492 XTOSFLGS_NUM EQU (*-XTOSFLGS_GOOD)/64
                                                1493 *
                                                1494 *
                           00005F00  00000001   1495 XTOSRMO_GOOD EQU *
00005F00  D3C5E7C2 D9C1404E                       1496  DC CL48'LEXBRA +exact FPCR modes 1-3, 7'
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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00005F30  3FFFFFFF 3FFFFFFF                         1497  DC XL16'3FFFFFFF3FFFFFFF3FFFFFFF3FFFFFFF'
00005F40  D3C5E7C2 D9C1404E                         1498  DC CL48'LEXBRA +exact M3 modes 1, 3-5'
00005F70  3FFFFFFF 3FFFFFFF                         1499  DC XL16'3FFFFFFF3FFFFFFF3FFFFFFF3FFFFFFF'
00005F80  D3C5E7C2 D9C1404E                         1500  DC CL48'LEXBRA +exact M3 modes 6, 7'
00005FB0  3FFFFFFF 3FFFFFFF                         1501  DC XL16'3FFFFFFF3FFFFFFF0000000000000000'
00005FC0  D3C5E7C2 D9C14060                         1502  DC CL48'LEXBRA -exact FPCR modes 1-3, 7'
00005FF0  BFFFFFFF BFFFFFFF                         1503  DC XL16'BFFFFFFFBFFFFFFFBFFFFFFFBFFFFFFF'
00006000  D3C5E7C2 D9C14060                         1504  DC CL48'LEXBRA -exact M3 modes 1, 3-5'
00006030  BFFFFFFF BFFFFFFF                         1505  DC XL16'BFFFFFFFBFFFFFFFBFFFFFFFBFFFFFFF'
00006040  D3C5E7C2 D9C14060                         1506  DC CL48'LEXBRA -exact M3 modes 6, 7'
00006070  BFFFFFFF BFFFFFFF                         1507  DC XL16'BFFFFFFFBFFFFFFF0000000000000000'
00006080  D3C5E7C2 D9C1404E                         1508  DC CL48'LEXBRA +tie odd FPCR modes 1-3, 7'
000060B0  3FFFFFFF 40000000                         1509  DC XL16'3FFFFFFF400000003FFFFFF3FFFFFFF'
000060C0  D3C5E7C2 D9C1404E                         1510  DC CL48'LEXBRA +tie odd M3 modes 1, 3-5'
000060F0  40000000 3FFFFFFF                         1511  DC XL16'400000003FFFFFFF400000003FFFFFFF'
00006100  D3C5E7C2 D9C1404E                         1512  DC CL48'LEXBRA +tie odd M3 modes 6, 7'
00006130  40000000 3FFFFFFF                         1513  DC XL16'400000003FFFFFFF0000000000000000'
00006140  D3C5E7C2 D9C14060                         1514  DC CL48'LEXBRA -tie odd FPCR modes 1-3, 7'
00006170  BFFFFFFF BFFFFFFF                         1515  DC XL16'BFFFFFFFBFFFFFFFC0000000BFFFFFFF'
00006180  D3C5E7C2 D9C14060                         1516  DC CL48'LEXBRA -tie odd M3 modes 1, 3-5'
000061B0  C0000000 BFFFFFFF                         1517  DC XL16'C0000000BFFFFFFFC0000000BFFFFFFF'
000061C0  D3C5E7C2 D9C14060                         1518  DC CL48'LEXBRA -tie odd M3 modes 6, 7'
000061F0  BFFFFFFF C0000000                         1519  DC XL16'BFFFFFFFC00000000000000000000000'
00006200  D3C5E7C2 D9C1404E                         1520  DC CL48'LEXBRA +tie even FPCR modes 1-3, 7'
00006230  3FFFFFFE 3FFFFFFF                         1521  DC XL16'3FFFFFFE3FFFFFF3FFFFFE3FFFFFFF'
00006240  D3C5E7C2 D9C1404E                         1522  DC CL48'LEXBRA +tie even M3 modes 1, 3-5'
00006270  3FFFFFFF 3FFFFFFF                         1523  DC XL16'3FFFFFFF3FFFFFF3FFFFFE3FFFFFFE'
00006280  D3C5E7C2 D9C1404E                         1524  DC CL48'LEXBRA +tie even M3 modes 6, 7'
000062B0  3FFFFFFF 3FFFFFFE                         1525  DC XL16'3FFFFFFF3FFFFFE0000000000000000'
000062C0  D3C5E7C2 D9C14060                         1526  DC CL48'LEXBRA -tie even FPCR modes 1-3, 7'
000062F0  BFFFFFFE BFFFFFFE                         1527  DC XL16'BFFFFFFEBFFFFFFEBFFFFFFFBFFFFFFF'
00006300  D3C5E7C2 D9C14060                         1528  DC CL48'LEXBRA -tie even M3 modes 1, 3-5'
00006330  BFFFFFFF BFFFFFFF                         1529  DC XL16'BFFFFFFFBFFFFFFFBFFFFFFEBFFFFFFE'
00006340  D3C5E7C2 D9C14060                         1530  DC CL48'LEXBRA -tie even M3 modes 6, 7'
00006370  BFFFFFFE BFFFFFFF                         1531  DC XL16'BFFFFFFEBFFFFFFF0000000000000000'
00006380  D3C5E7C2 D9C1404E                         1532  DC CL48'LEXBRA +false exact FPCR modes 1-3, 7'
000063B0  3FFFFFFF 40000000                         1533  DC XL16'3FFFFFFF400000003FFFFFF3FFFFFFF'
000063C0  D3C5E7C2 D9C1404E                         1534  DC CL48'LEXBRA +false exact M3 modes 1, 3-5'
000063F0  3FFFFFFF 3FFFFFFF                         1535  DC XL16'3FFFFFFF3FFFFFFF3FFFFFFF3FFFFFFF'
00006400  D3C5E7C2 D9C1404E                         1536  DC CL48'LEXBRA +false exact M3 modes 6, 7'
00006430  40000000 3FFFFFFF                         1537  DC XL16'400000003FFFFFFF0000000000000000'
00006440  D3C5E7C2 D9C14060                         1538  DC CL48'LEXBRA -false exact FPCR modes 1-3, 7'
00006470  BFFFFFFF BFFFFFFF                         1539  DC XL16'BFFFFFFFBFFFFFFFC0000000BFFFFFFF'
00006480  D3C5E7C2 D9C14060                         1540  DC CL48'LEXBRA -false exact M3 modes 1, 3-5'
000064B0  BFFFFFFF BFFFFFFF                         1541  DC XL16'BFFFFFFFBFFFFFFFBFFFFFFFBFFFFFFF'
000064C0  D3C5E7C2 D9C14060                         1542  DC CL48'LEXBRA -false exact M3 modes 6, 7'
000064F0  BFFFFFFF C0000000                         1543  DC XL16'BFFFFFFFC00000000000000000000000'
00006500  D3C5E7C2 D9C1404E                         1544  DC CL48'LEXBRA +near zero FPCR modes 1-3, 7'
00006530  3FFFFFFF 40000000                         1545  DC XL16'3FFFFFFF400000003FFFFFF3FFFFFFF'
00006540  D3C5E7C2 D9C1404E                         1546  DC CL48'LEXBRA +near zero M3 modes 1, 3-5'
00006570  3FFFFFFF 3FFFFFFF                         1547  DC XL16'3FFFFFFF3FFFFFF3FFFFFF3FFFFFFF'
00006580  D3C5E7C2 D9C1404E                         1548  DC CL48'LEXBRA +near zero M3 modes 6, 7'
000065B0  40000000 3FFFFFFF                         1549  DC XL16'400000003FFFFFFF0000000000000000'
000065C0  D3C5E7C2 D9C14060                         1550  DC CL48'LEXBRA -near zero FPCR modes 1-3, 7'
000065F0  BFFFFFFF BFFFFFFF                         1551  DC XL16'BFFFFFFFBFFFFFFFC0000000BFFFFFFF'
00006600  D3C5E7C2 D9C14060                         1552  DC CL48'LEXBRA -near zero M3 modes 1, 3-5'
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00006630  BFFFFFFF BFFFFFFF                          1553  DC XL16'BFFFFFFFBFFFFFFFBFFFFFFFBFFFFFFF'
00006640  D3C5E7C2 D9C14060                          1554  DC CL48'LEXBRA -near zero M3 modes 6, 7'
00006670  BFFFFFFF C0000000                          1555  DC XL16'BFFFFFFFC0000000000000000000000'
00006680  D3C5E7C2 D9C1404E                          1556  DC CL48'LEXBRA +near +inf FPCR modes 1-3, 7'
000066B0  3FFFFFFF 40000000                          1557  DC XL16'3FFFFFFF400000003FFFFFF3FFFFFF'
000066C0  D3C5E7C2 D9C1404E                          1558  DC CL48'LEXBRA +near +inf M3 modes 1, 3-5'
000066F0  40000000 3FFFFFFF                          1559  DC XL16'400000003FFFFFF400000003FFFFFF'
00006700  D3C5E7C2 D9C1404E                          1560  DC CL48'LEXBRA +near +inf M3 modes 6, 7'
00006730  40000000 3FFFFFFF                          1561  DC XL16'400000003FFFFFF0000000000000000'
00006740  D3C5E7C2 D9C14060                          1562  DC CL48'LEXBRA -near -inf FPCR modes 1-3, 7'
00006770  BFFFFFFF BFFFFFFF                          1563  DC XL16'BFFFFFFFBFFFFFFFC0000000BFFFFFFF'
00006780  D3C5E7C2 D9C14060                          1564  DC CL48'LEXBRA -near -inf M3 modes 1, 3-5'
000067B0  C0000000 BFFFFFFF                          1565  DC XL16'C0000000BFFFFFFFC0000000BFFFFFFF'
000067C0  D3C5E7C2 D9C14060                          1566  DC CL48'LEXBRA -near -inf M3 modes 6, 7'
000067F0  BFFFFFFF C0000000                          1567  DC XL16'BFFFFFFFC0000000000000000000000'
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00006830  7F7FFFFF 7F800000                          1569  DC XL16'7F7FFFFF7F8000007F7FFFF7F7FFFFF'
00006840  D3C5E7C2 D9C1404E                          1570  DC CL48'LEXBRA +overflow M3 modes 1, 3-5'
00006870  7F800000 7F7FFFFF                          1571  DC XL16'7F8000007F7FFFF7F8000007F7FFFF'
00006880  D3C5E7C2 D9C1404E                          1572  DC CL48'LEXBRA +overflow M3 modes 6, 7'
000068B0  7F800000 7F7FFFFF                          1573  DC XL16'7F8000007F7FFFF0000000000000000'
000068C0  D3C5E7C2 D9C14060                          1574  DC CL48'LEXBRA -overflow FPCR modes 1-3, 7'
000068F0  FF7FFFFF FF7FFFFF                          1575  DC XL16'FF7FFFFFFF7FFFFFFF800000FF7FFFFF'
00006900  D3C5E7C2 D9C14060                          1576  DC CL48'LEXBRA -overflow M3 modes 1, 3-5'
00006930  FF800000 FF7FFFFF                          1577  DC XL16'FF800000FF7FFFFFFF800000FF7FFFFF'
00006940  D3C5E7C2 D9C14060                          1578  DC CL48'LEXBRA -overflow M3 modes 6, 7'
00006970  FF7FFFFF FF800000                          1579  DC XL16'FF7FFFFFFF8000000000000000000000'
00006980  D3C5E7C2 D9C1404E                          1580  DC CL48'LEXBRA +tiny tie odd FPCR modes 1-3, 7'
000069B0  00000000 00000001                          1581  DC XL16'00000000000000010000000000000001'
000069C0  D3C5E7C2 D9C1404E                          1582  DC CL48'LEXBRA +tiny tie odd M3 modes 1, 3-5'
000069F0  00000001 00000001                          1583  DC XL16'00000001000000010000000000000000'
00006A00  D3C5E7C2 D9C1404E                          1584  DC CL48'LEXBRA +tiny tie odd M3 modes 6, 7'
00006A30  00000001 00000000                          1585  DC XL16'00000001000000000000000000000000'
00006A40  D3C5E7C2 D9C14060                          1586  DC CL48'LEXBRA -tiny tie odd FPCR modes 1-3, 7'
00006A70  80000000 80000000                          1587  DC XL16'80000000800000008000000180000001'
00006A80  D3C5E7C2 D9C14060                          1588  DC CL48'LEXBRA -tiny tie odd M3 modes 1, 3-5'
00006AB0  80000001 80000001                          1589  DC XL16'80000001800000018000000080000000'
00006AC0  D3C5E7C2 D9C14060                          1590  DC CL48'LEXBRA -tiny tie odd M3 modes 6, 7'
00006AF0  80000000 80000001                          1591  DC XL16'80000000800000010000000000000000'
                            00000030  00000001      1592 XTOSRMO_NUM EQU (*-XTOSRMO_GOOD)/64
                                                     1593 *
                                                     1594 *
                            00006B00  00000001      1595 XTOSRMOF_GOOD EQU *
00006B00  D3C5E7C2 D9C1404E                          1596  DC CL48'LEXBRA +exact FPC modes 1-3, 7 FCPR'
00006B30  00000001 00000002                          1597  DC XL16'00000001000000020000000300000007'
00006B40  D3C5E7C2 D9C1404E                          1598  DC CL48'LEXBRA +exact M3 modes 1, 3-5 FPCR'
00006B70  00000000 00000000                          1599  DC XL16'00000000000000000000000000000000'
00006B80  D3C5E7C2 D9C1404E                          1600  DC CL48'LEXBRA +exact M3 modes 6, 7 FCPR'
00006BB0  00000000 00000000                          1601  DC XL16'00000000000000000000000000000000'
00006BC0  D3C5E7C2 D9C14060                          1602  DC CL48'LEXBRA -exact FPC modes 1-3, 7 FCPR'
00006BF0  00000001 00000002                          1603  DC XL16'00000001000000020000000300000007'
00006C00  D3C5E7C2 D9C14060                          1604  DC CL48'LEXBRA -exact M3 modes 1, 3-5 FPCR'
00006C30  00000000 00000000                          1605  DC XL16'00000000000000000000000000000000'
00006C40  D3C5E7C2 D9C14060                          1606  DC CL48'LEXBRA -exact M3 modes 6, 7 FCPR'
00006C70  00000000 00000000                          1607  DC XL16'00000000000000000000000000000000'
00006C80  D3C5E7C2 D9C1404E                          1608  DC CL48'LEXBRA +tie odd FPC modes 1-3, 7 FCPR'
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00006CB0  00000001 00000002                       1609  DC XL16'00000001000000020000000300000007'
00006CC0  D3C5E7C2 D9C1404E                       1610  DC CL48'LEXBRA +tie odd M3 modes 1, 3-5 FPCR'
00006CF0  00080000 00080000                       1611  DC XL16'00080000000800000008000000080000'
00006D00  D3C5E7C2 D9C1404E                       1612  DC CL48'LEXBRA +tie odd M3 modes 6, 7 FCPR'
00006D30  00080000 00080000                       1613  DC XL16'00080000000800000000000000000000'
00006D40  D3C5E7C2 D9C14060                       1614  DC CL48'LEXBRA -tie odd FPC modes 1-3, 7 FCPR'
00006D70  00000001 00000002                       1615  DC XL16'00000001000000020000000300000007'
00006D80  D3C5E7C2 D9C14060                       1616  DC CL48'LEXBRA -tie odd M3 modes 1, 3-5 FPCR'
00006DB0  00080000 00080000                       1617  DC XL16'00080000000800000008000000080000'
00006DC0  D3C5E7C2 D9C14060                       1618  DC CL48'LEXBRA -tie odd M3 modes 6, 7 FCPR'
00006DF0  00080000 00080000                       1619  DC XL16'00080000000800000000000000000000'
00006E00  D3C5E7C2 D9C1404E                       1620  DC CL48'LEXBRA +tie even FPC modes 1-3, 7 FCPR'
00006E30  00000001 00000002                       1621  DC XL16'00000001000000020000000300000007'
00006E40  D3C5E7C2 D9C1404E                       1622  DC CL48'LEXBRA +tie even M3 modes 1, 3-5 FPCR'
00006E70  00080000 00080000                       1623  DC XL16'00080000000800000008000000080000'
00006E80  D3C5E7C2 D9C1404E                       1624  DC CL48'LEXBRA +tie even M3 modes 6, 7 FCPR'
00006EB0  00080000 00080000                       1625  DC XL16'00080000000800000000000000000000'
00006EC0  D3C5E7C2 D9C14060                       1626  DC CL48'LEXBRA -tie even FPC modes 1-3, 7 FCPR'
00006EF0  00000001 00000002                       1627  DC XL16'00000001000000020000000300000007'
00006F00  D3C5E7C2 D9C14060                       1628  DC CL48'LEXBRA -tie even M3 modes 1, 3-5 FPCR'
00006F30  00080000 00080000                       1629  DC XL16'00080000000800000008000000080000'
00006F40  D3C5E7C2 D9C14060                       1630  DC CL48'LEXBRA -tie even M3 modes 6, 7 FCPR'
00006F70  00080000 00080000                       1631  DC XL16'00080000000800000000000000000000'
00006F80  D3C5E7C2 D9C1404E                       1632  DC CL48'LEXBRA +false exact FPC modes 1-3, 7 FCPR'
00006FB0  00000001 00000002                       1633  DC XL16'00000001000000020000000300000007'
00006FC0  D3C5E7C2 D9C1404E                       1634  DC CL48'LEXBRA +false exact M3 modes 1, 3-5 FPCR'
00006FF0  00080000 00080000                       1635  DC XL16'00080000000800000008000000080000'
00007000  D3C5E7C2 D9C1404E                       1636  DC CL48'LEXBRA +false exact M3 modes 6, 7 FCPR'
00007030  00080000 00080000                       1637  DC XL16'00080000000800000000000000000000'
00007040  D3C5E7C2 D9C14060                       1638  DC CL48'LEXBRA -false exact FPC modes 1-3, 7 FCPR'
00007070  00000001 00000002                       1639  DC XL16'00000001000000020000000300000007'
00007080  D3C5E7C2 D9C14060                       1640  DC CL48'LEXBRA -false exact M3 modes 1, 3-5 FPCR'
000070B0  00080000 00080000                       1641  DC XL16'00080000000800000008000000080000'
000070C0  D3C5E7C2 D9C14060                       1642  DC CL48'LEXBRA -false exact M3 modes 6, 7 FCPR'
000070F0  00080000 00080000                       1643  DC XL16'00080000000800000000000000000000'
00007100  D3C5E7C2 D9C1404E                       1644  DC CL48'LEXBRA +near zero FPC modes 1-3, 7 FCPR'
00007130  00000001 00000002                       1645  DC XL16'00000001000000020000000300000007'
00007140  D3C5E7C2 D9C1404E                       1646  DC CL48'LEXBRA +near zero M3 modes 1, 3-5 FPCR'
00007170  00080000 00080000                       1647  DC XL16'00080000000800000008000000080000'
00007180  D3C5E7C2 D9C1404E                       1648  DC CL48'LEXBRA +near zero M3 modes 6, 7 FCPR'
000071B0  00080000 00080000                       1649  DC XL16'00080000000800000000000000000000'
000071C0  D3C5E7C2 D9C14060                       1650  DC CL48'LEXBRA -near zero FPC modes 1-3, 7 FCPR'
000071F0  00000001 00000002                       1651  DC XL16'00000001000000020000000300000007'
00007200  D3C5E7C2 D9C14060                       1652  DC CL48'LEXBRA -near zero M3 modes 1, 3-5 FPCR'
00007230  00080000 00080000                       1653  DC XL16'00080000000800000008000000080000'
00007240  D3C5E7C2 D9C14060                       1654  DC CL48'LEXBRA -near zero M3 modes 6, 7 FCPR'
00007270  00080000 00080000                       1655  DC XL16'00080000000800000000000000000000'
00007280  D3C5E7C2 D9C1404E                       1656  DC CL48'LEXBRA +near +inf FPC modes 1-3, 7 FCPR'
000072B0  00000001 00000002                       1657  DC XL16'00000001000000020000000300000007'
000072C0  D3C5E7C2 D9C1404E                       1658  DC CL48'LEXBRA +near +inf M3 modes 1, 3-5 FPCR'
000072F0  00080000 00080000                       1659  DC XL16'00080000000800000008000000080000'
00007300  D3C5E7C2 D9C1404E                       1660  DC CL48'LEXBRA +near +inf M3 modes 6, 7 FCPR'
00007330  00080000 00080000                       1661  DC XL16'00080000000800000000000000000000'
00007340  D3C5E7C2 D9C14060                       1662  DC CL48'LEXBRA -near -inf FPC modes 1-3, 7 FCPR'
00007370  00000001 00000002                       1663  DC XL16'00000001000000020000000300000007'
00007380  D3C5E7C2 D9C14060                       1664  DC CL48'LEXBRA -near -inf M3 modes 1, 3-5 FPCR'
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000073B0  00080000 00080000                       1665  DC XL16'00080000000800000008000000080000'
000073C0  D3C5E7C2 D9C14060                       1666  DC CL48'LEXBRA -near -inf M3 modes 6, 7 FCPR'
000073F0  00080000 00080000                       1667  DC XL16'00080000000800000000000000000000'
00007400  D3C5E7C2 D9C1404E                       1668  DC CL48'LEXBRA +overflow FPCR modes 1-3, 7 FPCR'
00007430  00000001 00200002                       1669  DC XL16'00000001002000020000000300000007'
00007440  D3C5E7C2 D9C1404E                       1670  DC CL48'LEXBRA +overflow M3 modes 1, 3-5 FPCR'
00007470  00280000 00080000                       1671  DC XL16'00280000000800000028000000080000'
00007480  D3C5E7C2 D9C1404E                       1672  DC CL48'LEXBRA +overflow M3 modes 6, 7 FPCR'
000074B0  00280000 00080000                       1673  DC XL16'00280000000800000000000000000000'
000074C0  D3C5E7C2 D9C14060                       1674  DC CL48'LEXBRA -overflow FPCR modes 1-3, 7 FPCR'
000074F0  00000001 00000002                       1675  DC XL16'00000001000000002002000300000007'
00007500  D3C5E7C2 D9C14060                       1676  DC CL48'LEXBRA -overflow M3 modes 1, 3-5 FPCR'
00007530  00280000 00080000                       1677  DC XL16'00280000000800000028000000080000'
00007540  D3C5E7C2 D9C14060                       1678  DC CL48'LEXBRA -overflow M3 modes 6, 7 FPCR'
00007570  00080000 00280000                       1679  DC XL16'00080000002800000000000000000000'
00007580  D3C5E7C2 D9C1404E                       1680  DC CL48'LEXBRA +tiny tie odd FPCR modes 1-3, 7 FPCR'
000075B0  00100001 00100002                       1681  DC XL16'00100001001000002001000300100007'
000075C0  D3C5E7C2 D9C1404E                       1682  DC CL48'LEXBRA +tiny tie odd M3 modes 1, 3-5 FPCR'
000075F0  00180000 00180000                       1683  DC XL16'00180000001800000018000000180000'
00007600  D3C5E7C2 D9C1404E                       1684  DC CL48'LEXBRA +tiny tie odd M3 modes 6, 7 FPCR'
00007630  00180000 00180000                       1685  DC XL16'00180000001800000000000000000000'
00007640  D3C5E7C2 D9C14060                       1686  DC CL48'LEXBRA -tiny tie odd FPCR modes 1-3, 7 FPCR'
00007670  00100001 00100002                       1687  DC XL16'00100001001000002001000300100007'
00007680  D3C5E7C2 D9C14060                       1688  DC CL48'LEXBRA -tiny tie odd M3 modes 1, 3-5 FPCR'
000076B0  00180000 00180000                       1689  DC XL16'00180000001800000018000000180000'
000076C0  D3C5E7C2 D9C14060                       1690  DC CL48'LEXBRA -tiny tie odd M3 modes 6, 7 FPCR'
000076F0  00180000 00180000                       1691  DC XL16'00180000001800000000000000000000'
                            00000030  00000001  1692 XTOSRMOF_NUM EQU (*-XTOSRMOF_GOOD)/64
                                                1693 *
                                                1694 *
                            00007700  00000001  1695 XTOLOUT_GOOD EQU *
00007700  D3C4E7C2 D9409985                       1696  DC CL48'LDXBR result pair 1'
00007730  00000000 00000000                       1697  DC XL16'00000000000000000000000000000000'
00007740  D3C4E7C2 D9409985                       1698  DC CL48'LDXBR result pair 2'
00007770  3FF80000 00000000                       1699  DC XL16'3FF80000000000003FF8000000000000'
00007780  D3C4E7C2 D9409985                       1700  DC CL48'LDXBR result pair 3'
000077B0  BFF80000 00000000                       1701  DC XL16'BFF8000000000000BFF8000000000000'
000077C0  D3C4E7C2 D9409985                       1702  DC CL48'LDXBR result pair 4'
000077F0  7FF81000 00000000                       1703  DC XL16'7FF81000000000000000000000000000'
00007800  D3C4E7C2 D9409985                       1704  DC CL48'LDXBR result pair 5'
00007830  7FF81100 00000000                       1705  DC XL16'7FF81100000000007FF8110000000000'
00007840  D3C4E7C2 D9409985                       1706  DC CL48'LDXBR result pair 6'
00007870  7FF00000 00000000                       1707  DC XL16'7FF000000000000023FF000000000000'
00007880  D3C4E7C2 D9409985                       1708  DC CL48'LDXBR result pair 7'
000078B0  FFF00000 00000000                       1709  DC XL16'FFF0000000000000A3FF000000000000'
000078C0  D3C4E7C2 D9409985                       1710  DC CL48'LDXBR result pair 8'
000078F0  7FF00000 00000000                       1711  DC XL16'7FF000000000000023FFFFFFFFFFFFFF'
00007900  D3C4E7C2 D9409985                       1712  DC CL48'LDXBR result pair 9'
00007930  FFF00000 00000000                       1713  DC XL16'FFF0000000000000A3FFFFFFFFFFFFFF'
00007940  D3C4E7C2 D9409985                       1714  DC CL48'LDXBR result pair 10'
00007970  00000000 00000000                       1715  DC XL16'00000000000000005BCC000000000000'
00007980  D3C4E7C2 D9409985                       1716  DC CL48'LDXBR result pair 11'
000079B0  80000000 00000000                       1717  DC XL16'80000000000000000DBCC000000000000'
000079C0  D3C4E7C2 D9409985                       1718  DC CL48'LDXBR result pair 12'
000079F0  7FF00000 00000000                       1719  DC XL16'7FF000000000000023FF000000000000'
00007A00  D3C4E7C2 D9409985                       1720  DC CL48'LDXBR result pair 13'
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00007A30  FFF00000 00000000                       1721  DC XL16'FFF0000000000000A3FF000000000000'
                             0000000D  00000001   1722 XTOLOUT_NUM EQU (*-XTOLOUT_GOOD)/64
                                                  1723 *
                                                  1724 *
                             00007A40  00000001   1725 XTOLFLGS_GOOD EQU *
00007A40  D3C4E7C2 D940C6D7                       1726  DC CL48'LDXBR FPCR pairs 1-2'
00007A70  00000000 F8000000                       1727  DC XL16'00000000F8000000000000000F8000000'
00007A80  D3C4E7C2 D940C6D7                       1728  DC CL48'LDXBR FPCR pairs 3-4'
00007AB0  00000000 F8000000                       1729  DC XL16'00000000F8000000000800000F8008000'
00007AC0  D3C4E7C2 D940C6D7                       1730  DC CL48'LDXBR FPCR pairs 5-6'
00007AF0  00000000 F8000000                       1731  DC XL16'00000000F8000000000280000F8002C00'
00007B00  D3C4E7C2 D940C6D7                       1732  DC CL48'LDXBR FPCR pairs 7-8'
00007B30  00280000 F8002C00                       1733  DC XL16'00280000F8002C0000280000F8002800'
00007B40  D3C4E7C2 D940C6D7                       1734  DC CL48'LDXBR FPCR pairs 9-10'
00007B70  00280000 F8002800                       1735  DC XL16'00280000F8002800001800000F8001000'
00007B80  D3C4E7C2 D940C6D7                       1736  DC CL48'LDXBR FPCR pairs 11-12'
00007BB0  00180000 F8001000                       1737  DC XL16'00180000F8001000002800000F8002000'
00007BC0  D3C4E7C2 D940C6D7                       1738  DC CL48'LDXBR FPCR pair 13'
00007BF0  00280000 F8002000                       1739  DC XL16'00280000F8002000000000000000000000'
                             00000007  00000001   1740 XTOLFLGS_NUM EQU (*-XTOLFLGS_GOOD)/64
                                                  1741 *
                                                  1742 *
                             00007C00  00000001   1743 XTOLRMO_GOOD EQU *
00007C00  D3C4E7C2 D9C1404E                       1744  DC CL48'LDXBRA +exact FPC modes 1, 2'
00007C30  3FFFFFFF FFFFFFFF                       1745  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00007C40  D3C4E7C2 D9C1404E                       1746  DC CL48'LDXBRA +exact FPC modes 3, 7'
00007C70  3FFFFFFF FFFFFFFF                       1747  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00007C80  D3C4E7C2 D9C1404E                       1748  DC CL48'LDXBRA +exact M3 modes 1, 3'
00007CB0  3FFFFFFF FFFFFFFF                       1749  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00007CC0  D3C4E7C2 D9C1404E                       1750  DC CL48'LDXBRA +exact M3 modes 4, 5'
00007CF0  3FFFFFFF FFFFFFFF                       1751  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00007D00  D3C4E7C2 D9C1404E                       1752  DC CL48'LDXBRA +exact M3 modes 6, 7'
00007D30  3FFFFFFF FFFFFFFF                       1753  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00007D40  D3C4E7C2 D9C14060                       1754  DC CL48'LDXBRA -exact FPC modes 1, 2'
00007D70  BFFFFFFF FFFFFFFF                       1755  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00007D80  D3C4E7C2 D9C14060                       1756  DC CL48'LDXBRA -exact FPC modes 3, 7'
00007DB0  BFFFFFFF FFFFFFFF                       1757  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00007DC0  D3C4E7C2 D9C14060                       1758  DC CL48'LDXBRA -exact M3 modes 1, 3'
00007DF0  BFFFFFFF FFFFFFFF                       1759  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00007E00  D3C4E7C2 D9C14060                       1760  DC CL48'LDXBRA -exact M3 modes 4, 5'
00007E30  BFFFFFFF FFFFFFFF                       1761  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00007E40  D3C4E7C2 D9C14060                       1762  DC CL48'LDXBRA -exact M3 modes 6, 7'
00007E70  BFFFFFFF FFFFFFFF                       1763  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00007E80  D3C4E7C2 D9C1404E                       1764  DC CL48'LDXBRA +tie odd FPC modes 1, 2'
00007EB0  3FFFFFFF FFFFFFFF                       1765  DC XL16'3FFFFFFFFFFFFFFF4000000000000000'
00007EC0  D3C4E7C2 D9C1404E                       1766  DC CL48'LDXBRA +tie odd FPC modes 3, 7'
00007EF0  3FFFFFFF FFFFFFFF                       1767  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00007F00  D3C4E7C2 D9C1404E                       1768  DC CL48'LDXBRA +tie odd M3 modes 1, 3'
00007F30  40000000 00000000                       1769  DC XL16'40000000000000003FFFFFFFFFFFFFFF'
00007F40  D3C4E7C2 D9C1404E                       1770  DC CL48'LDXBRA +tie odd M3 modes 4, 5'
00007F70  40000000 00000000                       1771  DC XL16'40000000000000003FFFFFFFFFFFFFFF'
00007F80  D3C4E7C2 D9C1404E                       1772  DC CL48'LDXBRA +tie odd M3 modes 6, 7'
00007FB0  40000000 00000000                       1773  DC XL16'40000000000000003FFFFFFFFFFFFFFF'
00007FC0  D3C4E7C2 D9C14060                       1774  DC CL48'LDXBRA -tie odd FPC modes 1, 2'
00007FF0  BFFFFFFF FFFFFFFF                       1775  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00008000  D3C4E7C2 D9C14060                       1776  DC CL48'LDXBRA -tie odd FPC modes 3, 7'
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00008030  C0000000 00000000                        1777  DC XL16'C000000000000000BFFFFFFFFFFFFFFF'
00008040  D3C4E7C2 D9C14060                        1778  DC CL48'LDXBRA -tie odd M3 modes 1, 3'
00008070  C0000000 00000000                        1779  DC XL16'C000000000000000BFFFFFFFFFFFFFFF'
00008080  D3C4E7C2 D9C14060                        1780  DC CL48'LDXBRA -tie odd M3 modes 4, 5'
000080B0  C0000000 00000000                        1781  DC XL16'C000000000000000BFFFFFFFFFFFFFFF'
000080C0  D3C4E7C2 D9C14060                        1782  DC CL48'LDXBRA -tie odd M3 modes 6, 7'
000080F0  BFFFFFFF FFFFFFFF                        1783  DC XL16'BFFFFFFFFFFFFFFFC000000000000000'
00008100  D3C4E7C2 D9C1404E                        1784  DC CL48'LDXBRA +tie even FPC modes 1, 2'
00008130  3FFFFFFF FFFFFFFE                        1785  DC XL16'3FFFFFFFFFFFFFFE3FFFFFFFFFFFFFFF'
00008140  D3C4E7C2 D9C1404E                        1786  DC CL48'LDXBRA +tie even FPC modes 3, 7'
00008170  3FFFFFFF FFFFFFFE                        1787  DC XL16'3FFFFFFFFFFFFFFE3FFFFFFFFFFFFFFF'
00008180  D3C4E7C2 D9C1404E                        1788  DC CL48'LDXBRA +tie even M3 modes 1, 3'
000081B0  3FFFFFFF FFFFFFFF                        1789  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
000081C0  D3C4E7C2 D9C1404E                        1790  DC CL48'LDXBRA +tie even M3 modes 4, 5'
000081F0  3FFFFFFF FFFFFFFE                        1791  DC XL16'3FFFFFFFFFFFFFFE3FFFFFFFFFFFFFFE'
00008200  D3C4E7C2 D9C1404E                        1792  DC CL48'LDXBRA +tie even M3 modes 6, 7'
00008230  3FFFFFFF FFFFFFFF                        1793  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFE'
00008240  D3C4E7C2 D9C14060                        1794  DC CL48'LDXBRA -tie even FPC modes 1, 2'
00008270  BFFFFFFF FFFFFFFE                        1795  DC XL16'BFFFFFFFFFFFFFFEBFFFFFFFFFFFFFFE'
00008280  D3C4E7C2 D9C14060                        1796  DC CL48'LDXBRA -tie even FPC modes 3, 7'
000082B0  BFFFFFFF FFFFFFFF                        1797  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
000082C0  D3C4E7C2 D9C14060                        1798  DC CL48'LDXBRA -tie even M3 modes 1, 3'
000082F0  BFFFFFFF FFFFFFFF                        1799  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00008300  D3C4E7C2 D9C14060                        1800  DC CL48'LDXBRA -tie even M3 modes 4, 5'
00008330  BFFFFFFF FFFFFFFE                        1801  DC XL16'BFFFFFFFFFFFFFFEBFFFFFFFFFFFFFFE'
00008340  D3C4E7C2 D9C14060                        1802  DC CL48'LDXBRA -tie even M3 modes 6, 7'
00008370  BFFFFFFF FFFFFFFE                        1803  DC XL16'BFFFFFFFFFFFFFFEBFFFFFFFFFFFFFFF'
00008380  D3C4E7C2 D9C1404E                        1804  DC CL48'LDXBRA +false exact FPC modes 1, 2'
000083B0  3FFFFFFF FFFFFFFF                        1805  DC XL16'3FFFFFFFFFFFFFFF4000000000000000'
000083C0  D3C4E7C2 D9C1404E                        1806  DC CL48'LDXBRA +false exact FPC modes 3, 7'
000083F0  3FFFFFFF FFFFFFFF                        1807  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00008400  D3C4E7C2 D9C1404E                        1808  DC CL48'LDXBRA +false exact M3 modes 1, 3'
00008430  3FFFFFFF FFFFFFFF                        1809  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00008440  D3C4E7C2 D9C1404E                        1810  DC CL48'LDXBRA +false exact M3 modes 4, 5'
00008470  3FFFFFFF FFFFFFFF                        1811  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00008480  D3C4E7C2 D9C1404E                        1812  DC CL48'LDXBRA +false exact M3 modes 6, 7'
000084B0  40000000 00000000                        1813  DC XL16'4000000000000003FFFFFFFFFFFFFFF'
000084C0  D3C4E7C2 D9C14060                        1814  DC CL48'LDXBRA -false exact FPC modes 1, 2'
000084F0  BFFFFFFF FFFFFFFF                        1815  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00008500  D3C4E7C2 D9C14060                        1816  DC CL48'LDXBRA -false exact FPC modes 3, 7'
00008530  C0000000 00000000                        1817  DC XL16'C000000000000000BFFFFFFFFFFFFFFF'
00008540  D3C4E7C2 D9C14060                        1818  DC CL48'LDXBRA -false exact M3 modes 1, 3'
00008570  BFFFFFFF FFFFFFFF                        1819  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00008580  D3C4E7C2 D9C14060                        1820  DC CL48'LDXBRA -false exact M3 modes 4, 5'
000085B0  BFFFFFFF FFFFFFFF                        1821  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
000085C0  D3C4E7C2 D9C14060                        1822  DC CL48'LDXBRA -false exact M3 modes 6, 7'
000085F0  BFFFFFFF FFFFFFFF                        1823  DC XL16'BFFFFFFFFFFFFFFFC000000000000000'
00008600  D3C4E7C2 D9C1404E                        1824  DC CL48'LDXBRA +near zero FPC modes 1, 2'
00008630  3FFFFFFF FFFFFFFF                        1825  DC XL16'3FFFFFFFFFFFFFFF4000000000000000'
00008640  D3C4E7C2 D9C1404E                        1826  DC CL48'LDXBRA +near zero FPC modes 3, 7'
00008670  3FFFFFFF FFFFFFFF                        1827  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00008680  D3C4E7C2 D9C1404E                        1828  DC CL48'LDXBRA +near zero M3 modes 1, 3'
000086B0  3FFFFFFF FFFFFFFF                        1829  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
000086C0  D3C4E7C2 D9C1404E                        1830  DC CL48'LDXBRA +near zero M3 modes 4, 5'
000086F0  3FFFFFFF FFFFFFFF                        1831  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00008700  D3C4E7C2 D9C1404E                        1832  DC CL48'LDXBRA +near zero M3 modes 6, 7'
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00008730  40000000 00000000                        1833  DC XL16'40000000000000003FFFFFFFFFFFFFFF'
00008740  D3C4E7C2 D9C14060                        1834  DC CL48'LDXBRA -near zero FPC modes 1, 2'
00008770  BFFFFFFF FFFFFFFF                        1835  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00008780  D3C4E7C2 D9C14060                        1836  DC CL48'LDXBRA -near zero FPC modes 3, 7'
000087B0  C0000000 00000000                        1837  DC XL16'C000000000000000BFFFFFFFFFFFFFFF'
000087C0  D3C4E7C2 D9C14060                        1838  DC CL48'LDXBRA -near zero M3 modes 1, 3'
000087F0  BFFFFFFF FFFFFFFF                        1839  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00008800  D3C4E7C2 D9C14060                        1840  DC CL48'LDXBRA -near zero M3 modes 4, 5'
00008830  BFFFFFFF FFFFFFFF                        1841  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00008840  D3C4E7C2 D9C14060                        1842  DC CL48'LDXBRA -near zero M3 modes 6, 7'
00008870  BFFFFFFF FFFFFFFF                        1843  DC XL16'BFFFFFFFFFFFFFFFC000000000000000'
00008880  D3C4E7C2 D9C1404E                        1844  DC CL48'LDXBRA +near +inf FPC modes 1, 2'
000088B0  3FFFFFFF FFFFFFFF                        1845  DC XL16'3FFFFFFFFFFFFFFF4000000000000000'
000088C0  D3C4E7C2 D9C1404E                        1846  DC CL48'LDXBRA +near +inf FPC modes 3, 7'
000088F0  3FFFFFFF FFFFFFFF                        1847  DC XL16'3FFFFFFFFFFFFFFF3FFFFFFFFFFFFFFF'
00008900  D3C4E7C2 D9C1404E                        1848  DC CL48'LDXBRA +near +inf M3 modes 1, 3'
00008930  40000000 00000000                        1849  DC XL16'40000000000000003FFFFFFFFFFFFFFF'
00008940  D3C4E7C2 D9C1404E                        1850  DC CL48'LDXBRA +near +inf M3 modes 4, 5'
00008970  40000000 00000000                        1851  DC XL16'40000000000000003FFFFFFFFFFFFFFF'
00008980  D3C4E7C2 D9C1404E                        1852  DC CL48'LDXBRA +near +inf M3 modes 6, 7'
000089B0  40000000 00000000                        1853  DC XL16'40000000000000003FFFFFFFFFFFFFFF'
000089C0  D3C4E7C2 D9C14060                        1854  DC CL48'LDXBRA -near -inf FPC modes 1, 2'
000089F0  BFFFFFFF FFFFFFFF                        1855  DC XL16'BFFFFFFFFFFFFFFFBFFFFFFFFFFFFFFF'
00008A00  D3C4E7C2 D9C14060                        1856  DC CL48'LDXBRA -near -inf FPC modes 3, 7'
00008A30  C0000000 00000000                        1857  DC XL16'C000000000000000BFFFFFFFFFFFFFFF'
00008A40  D3C4E7C2 D9C14060                        1858  DC CL48'LDXBRA -near -inf M3 modes 1, 3'
00008A70  C0000000 00000000                        1859  DC XL16'C000000000000000BFFFFFFFFFFFFFFF'
00008A80  D3C4E7C2 D9C14060                        1860  DC CL48'LDXBRA -near -inf M3 modes 4, 5'
00008AB0  C0000000 00000000                        1861  DC XL16'C000000000000000BFFFFFFFFFFFFFFF'
00008AC0  D3C4E7C2 D9C14060                        1862  DC CL48'LDXBRA -near -inf M3 modes 6, 7'
00008AF0  BFFFFFFF FFFFFFFF                        1863  DC XL16'BFFFFFFFFFFFFFFFC000000000000000'
00008B00  D3C4E7C2 D9C1404E                        1864  DC CL48'LDXBRA +overflow FPC modes 1, 2'
00008B30  7FEFFFFF FFFFFFFF                        1865  DC XL16'7FEFFFFFFFFFFFFF7FF0000000000000'
00008B40  D3C4E7C2 D9C1404E                        1866  DC CL48'LDXBRA +overflow FPC modes 3, 7'
00008B70  7FEFFFFF FFFFFFFF                        1867  DC XL16'7FEFFFFFFFFFFFFF7FEFFFFFFFFFFFFF'
00008B80  D3C4E7C2 D9C1404E                        1868  DC CL48'LDXBRA +overflow M3 modes 1, 3'
00008BB0  7FF00000 00000000                        1869  DC XL16'7FF00000000000007FEFFFFFFFFFFFFF'
00008BC0  D3C4E7C2 D9C1404E                        1870  DC CL48'LDXBRA +overflow M3 modes 4, 5'
00008BF0  7FF00000 00000000                        1871  DC XL16'7FF00000000000007FEFFFFFFFFFFFFF'
00008C00  D3C4E7C2 D9C1404E                        1872  DC CL48'LDXBRA +overflow M3 modes 6, 7'
00008C30  7FF00000 00000000                        1873  DC XL16'7FF00000000000007FEFFFFFFFFFFFFF'
00008C40  D3C4E7C2 D9C14060                        1874  DC CL48'LDXBRA -overflow FPC modes 1, 2'
00008C70  FFEFFFFF FFFFFFFF                        1875  DC XL16'FFEFFFFFFFFFFFFFFFEFFFFFFFFFFFFF'
00008C80  D3C4E7C2 D9C14060                        1876  DC CL48'LDXBRA -overflow FPC modes 3, 7'
00008CB0  FFF00000 00000000                        1877  DC XL16'FFF0000000000000FFEFFFFFFFFFFFFF'
00008CC0  D3C4E7C2 D9C14060                        1878  DC CL48'LDXBRA -overflow M3 modes 1, 3'
00008CF0  FFF00000 00000000                        1879  DC XL16'FFF0000000000000FFEFFFFFFFFFFFFF'
00008D00  D3C4E7C2 D9C14060                        1880  DC CL48'LDXBRA -overflow M3 modes 4, 5'
00008D30  FFF00000 00000000                        1881  DC XL16'FFF0000000000000FFEFFFFFFFFFFFFF'
00008D40  D3C4E7C2 D9C14060                        1882  DC CL48'LDXBRA -overflow M3 modes 6, 7'
00008D70  FFEFFFFF FFFFFFFF                        1883  DC XL16'FFEFFFFFFFFFFFFFFFF0000000000000'
00008D80  D3C4E7C2 D9C1404E                        1884  DC CL48'LDXBRA +tiny tie odd FPC modes 1, 2'
00008DB0  00000000 00000000                        1885  DC XL16'00000000000000000000000000000001'
00008DC0  D3C4E7C2 D9C1404E                        1886  DC CL48'LDXBRA +tiny tie odd FPC modes 3, 7'
00008DF0  00000000 00000000                        1887  DC XL16'00000000000000000000000000000001'
00008E00  D3C4E7C2 D9C1404E                        1888  DC CL48'LDXBRA +tiny tie odd M3 modes 1, 3'
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00008E30  00000000 00000001                       1889  DC XL16'00000000000000010000000000000001'
00008E40  D3C4E7C2 D9C1404E                       1890  DC CL48'LDXBRA +tiny tie odd M3 modes 4, 5'
00008E70  00000000 00000000                       1891  DC XL16'00000000000000000000000000000000'
00008E80  D3C4E7C2 D9C1404E                       1892  DC CL48'LDXBRA +tiny tie odd M3 modes 6, 7'
00008EB0  00000000 00000001                       1893  DC XL16'00000000000000010000000000000000'
00008EC0  D3C4E7C2 D9C14060                       1894  DC CL48'LDXBRA -tiny tie odd FPC modes 1, 2'
00008EF0  80000000 00000000                       1895  DC XL16'80000000000000008000000000000000'
00008F00  D3C4E7C2 D9C14060                       1896  DC CL48'LDXBRA -tiny tie odd FPC modes 3, 7'
00008F30  80000000 00000001                       1897  DC XL16'80000000000000018000000000000001'
00008F40  D3C4E7C2 D9C14060                       1898  DC CL48'LDXBRA -tiny tie odd M3 modes 1, 3'
00008F70  80000000 00000001                       1899  DC XL16'80000000000000018000000000000001'
00008F80  D3C4E7C2 D9C14060                       1900  DC CL48'LDXBRA -tiny tie odd M3 modes 4, 5'
00008FB0  80000000 00000000                       1901  DC XL16'80000000000000008000000000000000'
00008FC0  D3C4E7C2 D9C14060                       1902  DC CL48'LDXBRA -tiny tie odd M3 modes 6, 7'
00008FF0  80000000 00000000                       1903  DC XL16'80000000000000008000000000000001'
                            00000050  00000001   1904 XTOLRMO_NUM EQU (*-XTOLRMO_GOOD)/64
                                                 1905 *
                                                 1906 *
                            00009000  00000001   1907 XTOLRMOF_GOOD EQU *
00009000  D3C4E7C2 D9C1404E                       1908  DC CL48'LDXBRA +exact FPC modes 1-3, 7 FCPR'
00009030  00000001 00000002                       1909  DC XL16'00000001000000020000000300000007'
00009040  D3C4E7C2 D9C1404E                       1910  DC CL48'LDXBRA +exact M3 modes 1, 3-5 FPCR'
00009070  00000000 00000000                       1911  DC XL16'00000000000000000000000000000000'
00009080  D3C4E7C2 D9C1404E                       1912  DC CL48'LDXBRA +exact M3 modes 6, 7 FCPR'
000090B0  00000000 00000000                       1913  DC XL16'00000000000000000000000000000000'
000090C0  D3C4E7C2 D9C14060                       1914  DC CL48'LDXBRA -exact FPC modes 1-3, 7 FCPR'
000090F0  00000001 00000002                       1915  DC XL16'00000001000000020000000300000007'
00009100  D3C4E7C2 D9C14060                       1916  DC CL48'LDXBRA -exact M3 modes 1, 3-5 FPCR'
00009130  00000000 00000000                       1917  DC XL16'00000000000000000000000000000000'
00009140  D3C4E7C2 D9C14060                       1918  DC CL48'LDXBRA -exact M3 modes 6, 7 FCPR'
00009170  00000000 00000000                       1919  DC XL16'00000000000000000000000000000000'
00009180  D3C4E7C2 D9C1404E                       1920  DC CL48'LDXBRA +tie odd FPC modes 1-3, 7 FCPR'
000091B0  00000001 00000002                       1921  DC XL16'00000001000000020000000300000007'
000091C0  D3C4E7C2 D9C1404E                       1922  DC CL48'LDXBRA +tie odd M3 modes 1, 3-5 FPCR'
000091F0  00080000 00080000                       1923  DC XL16'00080000000800000008000000080000'
00009200  D3C4E7C2 D9C1404E                       1924  DC CL48'LDXBRA +tie odd M3 modes 6, 7 FCPR'
00009230  00080000 00080000                       1925  DC XL16'00080000000800000000000000000000'
00009240  D3C4E7C2 D9C14060                       1926  DC CL48'LDXBRA -tie odd FPC modes 1-3, 7 FCPR'
00009270  00000001 00000002                       1927  DC XL16'00000001000000020000000300000007'
00009280  D3C4E7C2 D9C14060                       1928  DC CL48'LDXBRA -tie odd M3 modes 1, 3-5 FPCR'
000092B0  00080000 00080000                       1929  DC XL16'00080000000800000008000000080000'
000092C0  D3C4E7C2 D9C14060                       1930  DC CL48'LDXBRA -tie odd M3 modes 6, 7 FCPR'
000092F0  00080000 00080000                       1931  DC XL16'00080000000800000000000000000000'
00009300  D3C4E7C2 D9C1404E                       1932  DC CL48'LDXBRA +tie even FPC modes 1-3, 7 FCPR'
00009330  00000001 00000002                       1933  DC XL16'00000001000000020000000300000007'
00009340  D3C4E7C2 D9C1404E                       1934  DC CL48'LDXBRA +tie even M3 modes 1, 3-5 FPCR'
00009370  00080000 00080000                       1935  DC XL16'00080000000800000008000000080000'
00009380  D3C4E7C2 D9C1404E                       1936  DC CL48'LDXBRA +tie even M3 modes 6, 7 FCPR'
000093B0  00080000 00080000                       1937  DC XL16'00080000000800000000000000000000'
000093C0  D3C4E7C2 D9C14060                       1938  DC CL48'LDXBRA -tie even FPC modes 1-3, 7 FCPR'
000093F0  00000001 00000002                       1939  DC XL16'00000001000000020000000300000007'
00009400  D3C4E7C2 D9C14060                       1940  DC CL48'LDXBRA -tie even M3 modes 1, 3-5 FPCR'
00009430  00080000 00080000                       1941  DC XL16'00080000000800000008000000080000'
00009440  D3C4E7C2 D9C14060                       1942  DC CL48'LDXBRA -tie even M3 modes 6, 7 FCPR'
00009470  00080000 00080000                       1943  DC XL16'00080000000800000000000000000000'
00009480  D3C4E7C2 D9C1404E                       1944  DC CL48'LDXBRA +false exact FPC modes 1-3, 7 FCPR'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000094B0  00000001 00000002                         1945  DC XL16'00000001000000020000000300000007'
000094C0  D3C4E7C2 D9C1404E                         1946  DC CL48'LDXBRA +false exact M3 modes 1, 3-5 FPCR'
000094F0  00080000 00080000                         1947  DC XL16'00080000000800000008000000080000'
00009500  D3C4E7C2 D9C1404E                         1948  DC CL48'LDXBRA +false exact M3 modes 6, 7 FCPR'
00009530  00080000 00080000                         1949  DC XL16'00080000000800000000000000000000'
00009540  D3C4E7C2 D9C14060                         1950  DC CL48'LDXBRA -false exact FPC modes 1-3, 7 FCPR'
00009570  00000001 00000002                         1951  DC XL16'00000001000000020000000300000007'
00009580  D3C4E7C2 D9C14060                         1952  DC CL48'LDXBRA -false exact M3 modes 1, 3-5 FPCR'
000095B0  00080000 00080000                         1953  DC XL16'00080000000800000008000000080000'
000095C0  D3C4E7C2 D9C14060                         1954  DC CL48'LDXBRA -false exact M3 modes 6, 7 FCPR'
000095F0  00080000 00080000                         1955  DC XL16'00080000000800000000000000000000'
00009600  D3C4E7C2 D9C1404E                         1956  DC CL48'LDXBRA +near zero FPC modes 1-3, 7 FCPR'
00009630  00000001 00000002                         1957  DC XL16'00000001000000020000000300000007'
00009640  D3C4E7C2 D9C1404E                         1958  DC CL48'LDXBRA +near zero M3 modes 1, 3-5 FPCR'
00009670  00080000 00080000                         1959  DC XL16'00080000000800000008000000080000'
00009680  D3C4E7C2 D9C1404E                         1960  DC CL48'LDXBRA +near zero M3 modes 6, 7 FCPR'
000096B0  00080000 00080000                         1961  DC XL16'00080000000800000000000000000000'
000096C0  D3C4E7C2 D9C14060                         1962  DC CL48'LDXBRA -near zero FPC modes 1-3, 7 FCPR'
000096F0  00000001 00000002                         1963  DC XL16'00000001000000020000000300000007'
00009700  D3C4E7C2 D9C14060                         1964  DC CL48'LDXBRA -near zero M3 modes 1, 3-5 FPCR'
00009730  00080000 00080000                         1965  DC XL16'00080000000800000008000000080000'
00009740  D3C4E7C2 D9C14060                         1966  DC CL48'LDXBRA -near zero M3 modes 6, 7 FCPR'
00009770  00080000 00080000                         1967  DC XL16'00080000000800000000000000000000'
00009780  D3C4E7C2 D9C1404E                         1968  DC CL48'LDXBRA +near +inf FPC modes 1-3, 7 FCPR'
000097B0  00000001 00000002                         1969  DC XL16'00000001000000020000000300000007'
000097C0  D3C4E7C2 D9C1404E                         1970  DC CL48'LDXBRA +near +inf M3 modes 1, 3-5 FPCR'
000097F0  00080000 00080000                         1971  DC XL16'00080000000800000008000000080000'
00009800  D3C4E7C2 D9C1404E                         1972  DC CL48'LDXBRA +near +inf M3 modes 6, 7 FCPR'
00009830  00080000 00080000                         1973  DC XL16'00080000000800000000000000000000'
00009840  D3C4E7C2 D9C14060                         1974  DC CL48'LDXBRA -near -inf FPC modes 1-3, 7 FCPR'
00009870  00000001 00000002                         1975  DC XL16'00000001000000020000000300000007'
00009880  D3C4E7C2 D9C14060                         1976  DC CL48'LDXBRA -near -inf M3 modes 1, 3-5 FPCR'
000098B0  00080000 00080000                         1977  DC XL16'00080000000800000008000000080000'
000098C0  D3C4E7C2 D9C14060                         1978  DC CL48'LDXBRA -near -inf M3 modes 6, 7 FCPR'
000098F0  00080000 00080000                         1979  DC XL16'00080000000800000000000000000000'
00009900  D3C4E7C2 D9C1404E                         1980  DC CL48'LDXBRA +overflow FPCR modes 1-3, 7 FPCR'
00009930  00000001 00200002                         1981  DC XL16'00000001002000020000000300000007'
00009940  D3C4E7C2 D9C1404E                         1982  DC CL48'LDXBRA +overflow M3 modes 1, 3-5 FPCR'
00009970  00280000 00080000                         1983  DC XL16'00280000000800000028000000080000'
00009980  D3C4E7C2 D9C1404E                         1984  DC CL48'LDXBRA +overflow M3 modes 6, 7 FPCR'
000099B0  00280000 00080000                         1985  DC XL16'00280000000800000000000000000000'
000099C0  D3C4E7C2 D9C14060                         1986  DC CL48'LDXBRA -overflow FPCR modes 1-3, 7 FPCR'
000099F0  00000001 00000002                         1987  DC XL16'00000001000000020020000300000007'
00009A00  D3C4E7C2 D9C14060                         1988  DC CL48'LDXBRA -overflow M3 modes 1, 3-5 FPCR'
00009A30  00280000 00080000                         1989  DC XL16'00280000000800000028000000080000'
00009A40  D3C4E7C2 D9C14060                         1990  DC CL48'LDXBRA -overflow M3 modes 6, 7 FPCR'
00009A70  00080000 00280000                         1991  DC XL16'00080000002800000000000000000000'
00009A80  D3C4E7C2 D9C1404E                         1992  DC CL48'LDXBRA +tiny tie odd FPCR modes 1-3, 7 FPCR'
00009AB0  00100001 00100002                         1993  DC XL16'00100001001000020010000300100007'
00009AC0  D3C4E7C2 D9C1404E                         1994  DC CL48'LDXBRA +tiny tie odd M3 modes 1, 3-5 FPCR'
00009AF0  00180000 00180000                         1995  DC XL16'00180000001800000018000000180000'
00009B00  D3C4E7C2 D9C1404E                         1996  DC CL48'LDXBRA +tiny tie odd M3 modes 6, 7 FPCR'
00009B30  00180000 00180000                         1997  DC XL16'00180000001800000000000000000000'
00009B40  D3C4E7C2 D9C14060                         1998  DC CL48'LDXBRA -tiny tie odd FPCR modes 1-3, 7 FPCR'
00009B70  00100001 00100002                         1999  DC XL16'00100001001000020010000300100007'
00009B80  D3C4E7C2 D9C14060                         2000  DC CL48'LDXBRA -tiny tie odd M3 modes 1, 3-5 FPCR'
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  LOC         OBJECT CODE       ADDR1     ADDR2    STMT
00009BB0  00180000 00180000                        2001  DC XL16'00180000001800000018000000180000'
00009BC0  D3C4E7C2 D9C14060                        2002  DC CL48'LDXBRA -tiny tie odd M3 modes 6, 7 FPCR'
00009BF0  00180000 00180000                        2003  DC XL16'00180000001800000000000000000000'
                            00000030  00000001   2004 XTOLRMOF_NUM EQU (*-XTOLRMOF_GOOD)/64
                                                 2005 *
                                                 2006 *
                            00009C00  00000001   2007 LTOSOUO_GOOD EQU *
00009C00  D3C5C4C2 D940A399                        2008  DC CL48'LEDBR trap results 1-2'
00009C30  27F00000 00000000                        2009  DC XL16'27F0000000000000A7F0000000000000'
00009C40  D3C5C4C2 D940A399                        2010  DC CL48'LEDBR trap results 3-4'
00009C70  27FFFFFF E0000000                        2011  DC XL16'27FFFFFFE0000000A7FFFFFFE0000000'
00009C80  D3C5C4C2 D940A399                        2012  DC CL48'LEDBR trap results 5-6'
00009CB0  56900000 00000000                        2013  DC XL16'569000000000000D690000000000000'
00009CC0  D3C5C4C2 D940A399                        2014  DC CL48'LEDBR trap results 7-8'
00009CF0  27F00000 00000000                        2015  DC XL16'27F0000000000000A7F0000000000000'
                            00000004  00000001   2016 LTOSOUO_NUM EQU (*-LTOSOUO_GOOD)/64
                                                 2017 *
                                                 2018 *
                            00009D00  00000001   2019 LTOSOUOF_GOOD EQU *
00009D00  D3C5C4C2 D940A399                        2020  DC CL48'LEDBR trap FPCR 1-4'
00009D30  F8002C00 F8002C00                        2021  DC XL16'F8002C00F8002C00F8002800F8002800'
00009D40  D3C5C4C2 D940A399                        2022  DC CL48'LEDBR trap FPCR 5-8'
00009D70  F8001000 F8001000                        2023  DC XL16'F8001000F8001000F8002000F8002000'
                            00000002  00000001   2024 LTOSOUOF_NUM EQU (*-LTOSOUOF_GOOD)/64
                                                 2025 *
                                                 2026 *
                            00009D80  00000001   2027 XTOSOUO_GOOD EQU *
00009D80  D3C5E7C2 D940A399                        2028  DC CL48'LEXBR trap results 1'
00009DB0  207F0000 00000000                        2029  DC XL16'207F00000000000000000000000000000'
00009DC0  D3C5E7C2 D940A399                        2030  DC CL48'LEXBR trap results 2'
00009DF0  A07F0000 00000000                        2031  DC XL16'A07F00000000000000000000000000000'
00009E00  D3C5E7C2 D940A399                        2032  DC CL48'LEXBR trap results 3'
00009E30  207FFFFF FE000000                        2033  DC XL16'207FFFFFFE0000000000000000000000'
00009E40  D3C5E7C2 D940A399                        2034  DC CL48'LEXBR trap results 4'
00009E70  A07FFFFF FE000000                        2035  DC XL16'A07FFFFFFE0000000000000000000000'
00009E80  D3C5E7C2 D940A399                        2036  DC CL48'LEXBR trap results 5'
00009EB0  5F690000 00000000                        2037  DC XL16'5F690000000000000000000000000000'
00009EC0  D3C5E7C2 D940A399                        2038  DC CL48'LEXBR trap results 6'
00009EF0  DF690000 00000000                        2039  DC XL16'DF690000000000000000000000000000'
00009F00  D3C5E7C2 D940A399                        2040  DC CL48'LEXBR trap results 7'
00009F30  207F0000 00000000                        2041  DC XL16'207F00000000000000000000000000000'
00009F40  D3C5E7C2 D940A399                        2042  DC CL48'LEXBR trap results 8'
00009F70  A07F0000 00000000                        2043  DC XL16'A07F00000000000000000000000000000'
                            00000008  00000001   2044 XTOSOUO_NUM EQU (*-XTOSOUO_GOOD)/64
                                                 2045 *
                                                 2046 *
                            00009F80  00000001   2047 XTOSOUOF_GOOD EQU *
00009F80  D3C5E7C2 D940A399                        2048  DC CL48'LEXBR trap FPCR 1-4'
00009FB0  F8002C00 F8002C00                        2049  DC XL16'F8002C00F8002C00F8002800F8002800'
00009FC0  D3C5E7C2 D940A399                        2050  DC CL48'LEXBR trap FPCR 5-8'
00009FF0  F8001000 F8001000                        2051  DC XL16'F8001000F8001000F8002000F8002000'
                            00000002  00000001   2052 XTOSOUOF_NUM EQU (*-XTOSOUOF_GOOD)/64
                                                 2053 *
                                                 2054 *
                            0000A000  00000001   2055 XTOLOUO_GOOD EQU *
0000A000  D3C4E7C2 D940A399                        2056  DC CL48'LDXBR trap result 1'
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  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

0000A030  23FF0000 00000000                         2057  DC XL16'23FF0000000000000000000000000000'
0000A040  D3C4E7C2 D940A399                         2058  DC CL48'LDXBR trap result 2'
0000A070  A3FF0000 00000000                         2059  DC XL16'A3FF0000000000000000000000000000'
0000A080  D3C4E7C2 D940A399                         2060  DC CL48'LDXBR trap result 3'
0000A0B0  23FFFFFF FFFFFFFF                         2061  DC XL16'23FFFFFFFFFFFFFF000000000000000'
0000A0C0  D3C4E7C2 D940A399                         2062  DC CL48'LDXBR trap result 4'
0000A0F0  A3FFFFFF FFFFFFFF                         2063  DC XL16'A3FFFFFFFFFFFFFF000000000000000'
0000A100  D3C4E7C2 D940A399                         2064  DC CL48'LDXBR trap result 5'
0000A130  5BCC0000 00000000                         2065  DC XL16'5BCC0000000000000000000000000000'
0000A140  D3C4E7C2 D940A399                         2066  DC CL48'LDXBR trap result 6'
0000A170  DBCC0000 00000000                         2067  DC XL16'DBCC0000000000000000000000000000'
0000A180  D3C4E7C2 D940A399                         2068  DC CL48'LDXBR trap result 7'
0000A1B0  23FF0000 00000000                         2069  DC XL16'23FF0000000000000000000000000000'
0000A1C0  D3C4E7C2 D940A399                         2070  DC CL48'LDXBR trap result 8'
0000A1F0  A3FF0000 00000000                         2071  DC XL16'A3FF0000000000000000000000000000'
                            00000008  00000001    2072 XTOLOUO_NUM EQU (*-XTOLOUO_GOOD)/64
                                                  2073 *
                                                  2074 *
                            0000A200  00000001    2075 XTOLOUOF_GOOD EQU *
0000A200  D3C4E7C2 D940A399                         2076  DC CL48'LDXBR trap FPCR 1-4'
0000A230  F8002C00 F8002C00                         2077  DC XL16'F8002C00F8002C00F8002800F8002800'
0000A240  D3C4E7C2 D940A399                         2078  DC CL48'LDXBR trap FPCR 5-8'
0000A270  F8001000 F8001000                         2079  DC XL16'F8001000F8001000F8002000F8002000'
                            00000002  00000001    2080 XTOLOUOF_NUM EQU (*-XTOLOUOF_GOOD)/64
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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000A280                                            2082 HELPERS  DS    0H       (R12 base of helper subroutines)

                                                    2084 ************************************************************
                                                    2085 *                 REPORT UNEXPECTED PROGRAM CHECK
                                                    2086 ************************************************************

0000A280                                            2088 PGMCK    DS    0H
0000A280  F342 C072 F08E      0000A2F2  0000008E    2089          UNPK  PROGCODE(L'PROGCODE+1),PCINTCD(L'PCINTCD+1)
0000A286  926B C076                     0000A2F6    2090          MVI   PGMCOMMA,C','
0000A28A  DC03 C072 C178      0000A2F2  0000A3F8    2091          TR    PROGCODE,HEXTRTAB

0000A290  F384 C07C F150      0000A2FC  00000150    2093          UNPK  PGMPSW+(0*9)(9),PCOLDPSW+(0*4)(5)
0000A296  9240 C084                     0000A304    2094          MVI   PGMPSW+(0*9)+8,C' '
0000A29A  DC07 C07C C178      0000A2FC  0000A3F8    2095          TR    PGMPSW+(0*9)(8),HEXTRTAB

0000A2A0  F384 C085 F154      0000A305  00000154    2097          UNPK  PGMPSW+(1*9)(9),PCOLDPSW+(1*4)(5)
0000A2A6  9240 C08D                     0000A30D    2098          MVI   PGMPSW+(1*9)+8,C' '
0000A2AA  DC07 C085 C178      0000A305  0000A3F8    2099          TR    PGMPSW+(1*9)(8),HEXTRTAB

0000A2B0  F384 C08E F158      0000A30E  00000158    2101          UNPK  PGMPSW+(2*9)(9),PCOLDPSW+(2*4)(5)
0000A2B6  9240 C096                     0000A316    2102          MVI   PGMPSW+(2*9)+8,C' '
0000A2BA  DC07 C08E C178      0000A30E  0000A3F8    2103          TR    PGMPSW+(2*9)(8),HEXTRTAB

0000A2C0  F384 C097 F15C      0000A317  0000015C    2105          UNPK  PGMPSW+(3*9)(9),PCOLDPSW+(3*4)(5)
0000A2C6  9240 C09F                     0000A31F    2106          MVI   PGMPSW+(3*9)+8,C' '
0000A2CA  DC07 C097 C178      0000A317  0000A3F8    2107          TR    PGMPSW+(3*9)(8),HEXTRTAB

0000A2D0  4100 0042                     00000042    2109          LA    R0,L'PROGMSG     R0 <== length of message
0000A2D4  4110 C05E                     0000A2DE    2110          LA    R1,PROGMSG       R1 --> the message text itself
0000A2D8  4520 C27A                     0000A4FA    2111          BAL   R2,MSG           Go display this message
                                                    2112
0000A2DC  07FD                                      2113          BR    R13              Return to caller




0000A2DE                                            2115 PROGMSG  DS   0CL66
0000A2DE  D7D9D6C7 D9C1D440                         2116          DC    CL20'PROGRAM CHECK! CODE '
0000A2F2  88888888                                  2117 PROGCODE DC    CL4'hhhh'
0000A2F6  6B                                        2118 PGMCOMMA DC    CL1','
0000A2F7  40D7E2E6 40                               2119          DC    CL5' PSW '
0000A2FC  88888888 88888888                         2120 PGMPSW   DC    CL36'hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh '
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                    2122 ************************************************************************
                                                    2123 *                        VERIFICATION ROUTINE
                                                    2124 ************************************************************************

0000A320                                            2126 VERISUB  DS    0H
                                                    2127 *
                                                    2128 **       Loop through the VERIFY TABLE...
                                                    2129 *

0000A320  4110 C32C                 0000A5AC        2131          LA    R1,VERIFTAB       R1 --> Verify table
0000A324  4120 0012                 00000012        2132          LA    R2,VERIFLEN       R2 <== Number of entries
0000A328  0D30                                      2133          BASR  R3,0              Set top of loop

0000A32A  9846 1000                 00000000        2135          LM    R4,R6,0(R1)       Load verify table values
0000A32E  4D70 C0C2                 0000A342        2136          BAS   R7,VERIFY          Verify results
0000A332  4110 100C                 0000000C        2137          LA    R1,12(,R1)        Next verify table entry
0000A336  0623                                      2138          BCTR  R2,R3             Loop through verify table

0000A338  9500 C278                 0000A4F8        2140          CLI   FAILFLAG,X'00'    Did all tests verify okay?
0000A33C  078D                                      2141          BER   R13               Yes, return to caller
0000A33E  47F0 F238                 00000238        2142          B     FAIL              No, load FAILURE disabled wait PSW


                                                    2144 *
                                                    2145 **       Loop through the ACTUAL / EXPECTED results...
                                                    2146 *

0000A342  0D80                                      2148 VERIFY   BASR  R8,0              Set top of loop

0000A344  D50F 4000 5030      00000000  00000030  2150          CLC   0(16,R4),48(R5)  Actual results == Expected results?
0000A34A  4770 C0DA                     0000A35A  2151          BNE   VERIFAIL          No, show failure
0000A34E  4140 4010                     00000010  2152 VERINEXT LA    R4,16(,R4)        Next actual result
0000A352  4150 5040                     00000040  2153          LA    R5,64(,R5)        Next expected result
0000A356  0668                                      2154          BCTR  R6,R8             Loop through results

0000A358  07F7                                      2156          BR    R7                Return to caller
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   2158 ************************************************************************
                                                   2159 *                      Report the failure...
                                                   2160 ************************************************************************

0000A35A  9005 C250                    0000A4D0   2162 VERIFAIL STM   R0,R5,SAVER0R5   Save registers
0000A35E  92FF C278                    0000A4F8   2163          MVI   FAILFLAG,X'FF'   Remember verification failure
                                                   2164 *
                                                   2165 **       First, show them the description...
                                                   2166 *
0000A362  D22F C1E0 5000      0000A460 00000000   2167          MVC   FAILDESC,0(R5)   Save results/test description
0000A368  4100 0044                    00000044   2168          LA    R0,L'FAILMSG1    R0 <== length of message
0000A36C  4110 C1CC                    0000A44C   2169          LA    R1,FAILMSG1      R1 --> the message text itself
0000A370  4520 C27A                    0000A4FA   2170          BAL   R2,MSG           Go display this message
                                                   2171 *
                                                   2172 **       Save address of actual and expected results
                                                   2173 *
0000A374  5040 C24C                    0000A4CC   2174          ST    R4,AACTUAL       Save A(actual results)
0000A378  4150 5030                    00000030   2175          LA    R5,48(,R5)       R5 ==> expected results
0000A37C  5050 C248                    0000A4C8   2176          ST    R5,AEXPECT       Save A(expected results)
                                                   2177 *
                                                   2178 **       Format and show them the EXPECTED ("Want") results...
                                                   2179 *
0000A380  D205 C210 C408      0000A490 0000A688   2180          MVC   WANTGOT,=CL6'Want: '
0000A386  F384 C216 C248      0000A496 0000A4C8   2181          UNPK  FAILADR(L'FAILADR+1),AEXPECT(L'AEXPECT+1)
0000A38C  9240 C21E                    0000A49E   2182          MVI   BLANKEQ,C' '
0000A390  DC07 C216 C178      0000A496 0000A3F8   2183          TR    FAILADR,HEXTRTAB

0000A396  F384 C221 5000      0000A4A1 00000000   2185          UNPK  FAILVALS+(0*9)(9),(0*4)(5,R5)
0000A39C  9240 C229                    0000A4A9   2186          MVI   FAILVALS+(0*9)+8,C' '
0000A3A0  DC07 C221 C178      0000A4A1 0000A3F8   2187          TR    FAILVALS+(0*9)(8),HEXTRTAB

0000A3A6  F384 C22A 5004      0000A4AA 00000004   2189          UNPK  FAILVALS+(1*9)(9),(1*4)(5,R5)
0000A3AC  9240 C232                    0000A4B2   2190          MVI   FAILVALS+(1*9)+8,C' '
0000A3B0  DC07 C22A C178      0000A4AA 0000A3F8   2191          TR    FAILVALS+(1*9)(8),HEXTRTAB

0000A3B6  F384 C233 5008      0000A4B3 00000008   2193          UNPK  FAILVALS+(2*9)(9),(2*4)(5,R5)
0000A3BC  9240 C23B                    0000A4BB   2194          MVI   FAILVALS+(2*9)+8,C' '
0000A3C0  DC07 C233 C178      0000A4B3 0000A3F8   2195          TR    FAILVALS+(2*9)(8),HEXTRTAB

0000A3C6  F384 C23C 500C      0000A4BC 0000000C   2197          UNPK  FAILVALS+(3*9)(9),(3*4)(5,R5)
0000A3CC  9240 C244                    0000A4C4   2198          MVI   FAILVALS+(3*9)+8,C' '
0000A3D0  DC07 C23C C178      0000A4BC 0000A3F8   2199          TR    FAILVALS+(3*9)(8),HEXTRTAB

0000A3D6  4100 0035                    00000035   2201          LA    R0,L'FAILMSG2    R0 <== length of message
0000A3DA  4110 C210                    0000A490   2202          LA    R1,FAILMSG2      R1 --> the message text itself
0000A3DE  4520 C27A                    0000A4FA   2203          BAL   R2,MSG           Go display this message
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                          2205 *
                                          2206 **       Format and show them the ACTUAL ("Got") results...
                                          2207 *
0000A3E2  D205 C210 C40E      0000A490  0000A68E  2208          MVC   WANTGOT,=CL6'Got:  '
0000A3E8  F384 C216 C24C      0000A496  0000A4CC  2209          UNPK  FAILADR(L'FAILADR+1),AACTUAL(L'AACTUAL+1)
0000A3EE  9240 C21E                     0000A49E  2210          MVI   BLANKEQ,C' '
0000A3F2  DC07 C216 C178      0000A496  0000A3F8  2211          TR    FAILADR,HEXTRTAB

0000A3F8  F384 C221 4000      0000A4A1  00000000  2213          UNPK  FAILVALS+(0*9)(9),(0*4)(5,R4)
0000A3FE  9240 C229                     0000A4A9  2214          MVI   FAILVALS+(0*9)+8,C' '
0000A402  DC07 C221 C178      0000A4A1  0000A3F8  2215          TR    FAILVALS+(0*9)(8),HEXTRTAB

0000A408  F384 C22A 4004      0000A4AA  00000004  2217          UNPK  FAILVALS+(1*9)(9),(1*4)(5,R4)
0000A40E  9240 C232                     0000A4B2  2218          MVI   FAILVALS+(1*9)+8,C' '
0000A412  DC07 C22A C178      0000A4AA  0000A3F8  2219          TR    FAILVALS+(1*9)(8),HEXTRTAB

0000A418  F384 C233 4008      0000A4B3  00000008  2221          UNPK  FAILVALS+(2*9)(9),(2*4)(5,R4)
0000A41E  9240 C23B                     0000A4BB  2222          MVI   FAILVALS+(2*9)+8,C' '
0000A422  DC07 C233 C178      0000A4B3  0000A3F8  2223          TR    FAILVALS+(2*9)(8),HEXTRTAB

0000A428  F384 C23C 400C      0000A4BC  0000000C  2225          UNPK  FAILVALS+(3*9)(9),(3*4)(5,R4)
0000A42E  9240 C244                     0000A4C4  2226          MVI   FAILVALS+(3*9)+8,C' '
0000A432  DC07 C23C C178      0000A4BC  0000A3F8  2227          TR    FAILVALS+(3*9)(8),HEXTRTAB

0000A438  4100 0035                     00000035  2229          LA    R0,L'FAILMSG2    R0 <== length of message
0000A43C  4110 C210                     0000A490  2230          LA    R1,FAILMSG2      R1 --> the message text itself
0000A440  4520 C27A                     0000A4FA  2231          BAL   R2,MSG           Go display this message

0000A444  9805 C250                     0000A4D0  2233          LM    R0,R5,SAVER0R5   Restore registers
0000A448  47F0 C0CE                     0000A34E  2234          B     VERINEXT         Continue with verification...



0000A44C                                          2236 FAILMSG1 DS    0CL68
0000A44C  C3D6D4D7 C1D9C9E2                       2237          DC    CL20'COMPARISON FAILURE! '
0000A460  4D8485A2 83998997                       2238 FAILDESC DC    CL48'(description)'


0000A490                                          2240 FAILMSG2 DS    0CL53
0000A490  40404040 4040                           2241 WANTGOT  DC    CL6' '           'Want: ' -or- 'Got:  '
0000A496  C1C1C1C1 C1C1C1C1                       2242 FAILADR  DC    CL8'AAAAAAAA'
0000A49E  407E40                                  2243 BLANKEQ  DC    CL3' = '
0000A4A1  88888888 88888888                       2244 FAILVALS DC    CL36'hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh '

0000A4C8  00000000                                2246 AEXPECT  DC    F'0'             ==> Expected ("Want") results
0000A4CC  00000000                                2247 AACTUAL  DC    F'0'             ==> Actual ("Got") results
0000A4D0  00000000 00000000                       2248 SAVER0R5 DC    6F'0'            Registers R0 - R5 save area
0000A4E8  F0F1F2F3 F4F5F6F7                       2249 CHARHEX  DC    CL16'0123456789ABCDEF'
                            0000A3F8  00000010    2250 HEXTRTAB EQU   CHARHEX-X'F0'    Hexadecimal translation table
0000A4F8  00                                      2251 FAILFLAG DC    X'00'            FF = Fail, 00 = Success
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                          2253 ********************************************************************
                                          2254 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                          2255 ********************************************************************

0000A4FA  4900 C404                 0000A684  2257 MSG      CH    R0,=H'0'               Do we even HAVE a message?
0000A4FE  07D2                              2258          BNHR  R2                     No, ignore

0000A500  9002 C2B0                 0000A530  2260          STM   R0,R2,MSGSAVE          Save registers

0000A504  4900 C406                 0000A686  2262          CH    R0,=AL2(L'MSGMSG)      Message length within limits?
0000A508  47D0 C290                 0000A510  2263          BNH   MSGOK                  Yes, continue
0000A50C  4100 005F                 0000005F  2264          LA    R0,L'MSGMSG            No, set to maximum

0000A510  1820                              2266 MSGOK    LR    R2,R0                  Copy length to work register
0000A512  0620                              2267          BCTR  R2,0                   Minus-1 for execute
0000A514  4420 C2BC                 0000A53C  2268          EX    R2,MSGMVC              Copy message to O/P buffer

0000A518  4120 200A                 0000000A  2270          LA    R2,1+L'MSGCMD(,R2)     Calculate true command length
0000A51C  4110 C2C2                 0000A542  2271          LA    R1,MSGCMD              Point to true command

0000A520  83120008                          2273          DC    X'83',X'12',X'0008'    Issue Hercules Diagnose X'008'
0000A524  4780 C2AA                 0000A52A  2274          BZ    MSGRET                 Return if successful
0000A528  0000                              2275          DC    H'0'                   CRASH for debugging purposes

0000A52A  9802 C2B0                 0000A530  2277 MSGRET   LM    R0,R2,MSGSAVE          Restore registers
0000A52E  07F2                              2278          BR    R2                     Return to caller
```

```
0000A530  00000000 00000000                 2280 MSGSAVE  DC    3F'0'                  Registers save area
0000A53C  D200 C2CB 1000      0000A54B  00000000  2281 MSGMVC   MVC   MSGMSG(0),0(R1)      Executed instruction

0000A542  D4E2C7D5 D6C8405C                 2283 MSGCMD   DC    C'MSGNOH * '           *** HERCULES MESSAGE COMMAND ***
0000A54B  40404040 40404040                 2284 MSGMSG   DC    CL95' '                The message text to be displayed
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                  2286 ********************************************************************************
                                                  2287 *                              VERIFY TABLE
                                                  2288 ********************************************************************************
                                                  2289 *
                                                  2290 *        A(actual results), A(expected results), A(#of results)
                                                  2291 *
                                                  2292 ********************************************************************************

0000A5AC                                          2294 VERIFTAB DC    0F'0'
0000A5AC  00001000                                2295          DC    A(LTOSOUT)
0000A5B0  00004000                                2296          DC    A(LTOSOUT_GOOD)
0000A5B4  00000007                                2297          DC    A(LTOSOUT_NUM)
                                                  2298 *
0000A5B8  00001080                                2299          DC    A(LTOSFLGS)
0000A5BC  000041C0                                2300          DC    A(LTOSFLGS_GOOD)
0000A5C0  00000007                                2301          DC    A(LTOSFLGS_NUM)
                                                  2302 *
0000A5C4  00001100                                2303          DC    A(LTOSRMO)
0000A5C8  00004380                                2304          DC    A(LTOSRMO_GOOD)
0000A5CC  00000030                                2305          DC    A(LTOSRMO_NUM)
                                                  2306 *
0000A5D0  00001500                                2307          DC    A(LTOSRMOF)
0000A5D4  00004F80                                2308          DC    A(LTOSRMOF_GOOD)
0000A5D8  00000030                                2309          DC    A(LTOSRMOF_NUM)
                                                  2310 *
0000A5DC  00001900                                2311          DC    A(XTOSOUT)
0000A5E0  00005B80                                2312          DC    A(XTOSOUT_GOOD)
0000A5E4  00000007                                2313          DC    A(XTOSOUT_NUM)
                                                  2314 *
0000A5E8  00001980                                2315          DC    A(XTOSFLGS)
0000A5EC  00005D40                                2316          DC    A(XTOSFLGS_GOOD)
0000A5F0  00000007                                2317          DC    A(XTOSFLGS_NUM)
                                                  2318 *
0000A5F4  00001A00                                2319          DC    A(XTOSRMO)
0000A5F8  00005F00                                2320          DC    A(XTOSRMO_GOOD)
0000A5FC  00000030                                2321          DC    A(XTOSRMO_NUM)
                                                  2322 *
0000A600  00001E00                                2323          DC    A(XTOSRMOF)
0000A604  00006B00                                2324          DC    A(XTOSRMOF_GOOD)
0000A608  00000030                                2325          DC    A(XTOSRMOF_NUM)
                                                  2326 *
0000A60C  00002200                                2327          DC    A(XTOLOUT)
0000A610  00007700                                2328          DC    A(XTOLOUT_GOOD)
0000A614  0000000D                                2329          DC    A(XTOLOUT_NUM)
                                                  2330 *
0000A618  00002300                                2331          DC    A(XTOLFLGS)
0000A61C  00007A40                                2332          DC    A(XTOLFLGS_GOOD)
0000A620  00000007                                2333          DC    A(XTOLFLGS_NUM)
                                                  2334 *
0000A624  00002400                                2335          DC    A(XTOLRMO)
0000A628  00007C00                                2336          DC    A(XTOLRMO_GOOD)
0000A62C  00000050                                2337          DC    A(XTOLRMO_NUM)
                                                  2338 *
0000A630  00002B00                                2339          DC    A(XTOLRMOF)
0000A634  00009000                                2340          DC    A(XTOLRMOF_GOOD)
0000A638  00000030                                2341          DC    A(XTOLRMOF_NUM)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    2342 *
0000A63C  00003000                                  2343          DC    A(LTOSOUO)
0000A640  00009C00                                  2344          DC    A(LTOSOUO_GOOD)
0000A644  00000004                                  2345          DC    A(LTOSOUO_NUM)
                                                    2346 *
0000A648  00003080                                  2347          DC    A(LTOSOUOF)
0000A64C  00009D00                                  2348          DC    A(LTOSOUOF_GOOD)
0000A650  00000002                                  2349          DC    A(LTOSOUOF_NUM)
                                                    2350 *
0000A654  00003100                                  2351          DC    A(XTOSOUO)
0000A658  00009D80                                  2352          DC    A(XTOSOUO_GOOD)
0000A65C  00000008                                  2353          DC    A(XTOSOUO_NUM)
                                                    2354 *
0000A660  00003180                                  2355          DC    A(XTOSOUOF)
0000A664  00009F80                                  2356          DC    A(XTOSOUOF_GOOD)
0000A668  00000002                                  2357          DC    A(XTOSOUOF_NUM)
                                                    2358 *
0000A66C  00003200                                  2359          DC    A(XTOLOUO)
0000A670  0000A000                                  2360          DC    A(XTOLOUO_GOOD)
0000A674  00000008                                  2361          DC    A(XTOLOUO_NUM)
                                                    2362 *
0000A678  00003280                                  2363          DC    A(XTOLOUOF)
0000A67C  0000A200                                  2364          DC    A(XTOLOUOF_GOOD)
0000A680  00000002                                  2365          DC    A(XTOLOUOF_NUM)
                                                    2366 *
                            00000012  00000001      2367 VERIFLEN EQU   (*-VERIFTAB)/12    #of entries in verify table
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000A684                                            2369          END
0000A684  0000                                      2370                =H'0'
0000A686  005F                                      2371                =AL2(L'MSGMSG)
0000A688  E68195A3 7A40                             2372                =CL6'Want: '
0000A68E  C796A37A 4040                             2373                =CL6'Got:  '
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
AACTUAL	F	00A4CC	4	2247	2174 2209
AEXPECT	F	00A4C8	4	2246	2176 2181
AHELPERS	A	00027C	4	274	264 324
BFPLDRND	J	000000	42644	191	241 244 246 249 257 1177 1179 1181 1183 1186 1188 1190 1192 1196 1198 1200 1202 1205 1207 1209 1211 1213 1215 1221
BLANKEQ	C	00A49E	3	2243	2182 2210
CHARHEX	C	00A4E8	16	2249	2250
CTLR0	F	000308	4	334	280 281 282
FAIL	I	000238	4	272	2142
FAILADR	C	00A496	8	2242	2181 2183 2209 2211
FAILDESC	C	00A460	48	2238	2167
FAILFLAG	X	00A4F8	1	2251	2140 2163
FAILMSG1	C	00A44C	68	2236	2168 2169
FAILMSG2	C	00A490	53	2240	2201 2202 2229 2230
FAILPSW	X	0002F8	8	332	272
FAILVALS	C	00A4A1	36	2244	2185 2186 2187 2189 2190 2191 2193 2194 2195 2197 2198 2199 2213 2214 2215 2217 2218 2219 2221 2222 2223 2225 2226 2227
FPCREGNT	X	00030C	4	335	414 490 496 502 508 516 521 526 531 536 541 569 645 651 657 663 671 676 681 686 691 696 724 801 807 813 819 825 830 835 840 845 850
FPCREGTR	X	000310	4	336	420 449 574 604 729 759
FPR0	U	000000	1	211	413 415 421 448 450 486 492 498 504 510 517 522 527 532 537 542 567 570 576 602 605 641 647 653 659 665 672 677 682 687 692 697 722 725 731 757 760 796 803 809 815 821 826 831 836 841 846 851
FPR1	U	000001	1	212	412 415 416 419 421 422 447 450 451 492 493 498 499 504 505 510 511 517 518 522 523 527 528 532 533 537 538 542 543 570 575 576 577 605 606 647 648 653 654 659 660 665 666 672 673 677 678 682 683 687 688 692 693 697 698 725 726 730 731 732 760 761 803 804 809 810 815 816 821 822 826 827 831 832 836 837 841 842 846 847 851 852
FPR10	U	00000A	1	221	
FPR11	U	00000B	1	222	
FPR12	U	00000C	1	223	
FPR13	U	00000D	1	224	
FPR14	U	00000E	1	225	
FPR15	U	00000F	1	226	
FPR2	U	000002	1	213	
FPR3	U	000003	1	214	607 762
FPR4	U	000004	1	215	
FPR5	U	000005	1	216	
FPR6	U	000006	1	217	
FPR7	U	000007	1	218	
FPR8	U	000008	1	219	
FPR9	U	000009	1	220	
GOODPSW	X	0002E8	8	331	328
HELPERS	H	00A280	2	2082	229 274
HEXTRTAB	U	00A3F8	16	2250	2091 2095 2099 2103 2107 2183 2187 2191 2195 2199 2211 2215 2219 2223 2227
IMAGE	1	000000	42644	0	
LDXBR	I	00064C	4	716	301
LDXBRA	I	0006D0	4	790	303
LDXBROUT	I	000696	4	751	318
LEDBR	I	0003A4	4	406	287
LEDBRA	I	000424	4	480	289
LEDBROUT	I	0003EE	4	441	308

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
LEXBR	I	0004F6	4	561	294
LEXBRA	I	00057A	4	635	296
LEXBROUT	I	000540	4	596	313
LTOSBAS	F	000314	4	344	286
LTOSCT	U	000068	1	899	345
LTOSFLGS	U	001080	0	1179	348 2299
LTOSFLGS_GOOD	U	0041C0	1	1241	1256 2300
LTOSFLGS_NUM	U	000007	1	1256	2301
LTOSIN	D	0007A8	8	882	899 346
LTOSINOU	D	0007D0	8	889	900 382
LTOSINRM	D	000810	8	906	962 364
LTOSOU	F	000374	4	380	307
LTOSOUCT	U	000040	1	900	381
LTOSOUO	U	003000	0	1205	383 2343
LTOSOUOF	U	003080	0	1207	384 2347
LTOSOUOF_GOOD	U	009D00	1	2019	2024 2348
LTOSOUOF_NUM	U	000002	1	2024	2349
LTOSOUO_GOOD	U	009C00	1	2007	2016 2344
LTOSOUO_NUM	U	000004	1	2016	2345
LTOSOUT	U	001000	0	1177	347 2295
LTOSOUT_GOOD	U	004000	1	1223	1238 2296
LTOSOUT_NUM	U	000007	1	1238	2297
LTOSRM	F	000344	4	362	288
LTOSRMCT	U	000080	1	962	363
LTOSRMO	U	001100	0	1181	365 2303
LTOSRMOF	U	001500	0	1183	366 2307
LTOSRMOF_GOOD	U	004F80	1	1359	1456 2308
LTOSRMOF_NUM	U	000030	1	1456	2309
LTOSRMO_GOOD	U	004380	1	1259	1356 2304
LTOSRMO_NUM	U	000030	1	1356	2305
MSG	I	00A4FA	4	2257	2111 2170 2203 2231
MSGCMD	C	00A542	9	2283	2270 2271
MSGMSG	C	00A54B	95	2284	2264 2281 2262
MSGMVC	I	00A53C	6	2281	2268
MSGOK	I	00A510	2	2266	2263
MSGRET	I	00A52A	4	2277	2274
MSGSAVE	F	00A530	4	2280	2260 2277
PCINTCD	H	00008E	2	242	259 2089
PCNOTDTA	I	00020C	4	263	260
PCOLDPSW	U	000150	0	244	261 2093 2097 2101 2105
PGMCK	H	00A280	2	2088	265
PGMCOMMA	C	00A2F6	1	2118	2090
PGMPSW	C	00A2FC	36	2120	2093 2094 2095 2097 2098 2099 2101 2102 2103 2105 2106 2107
PROGCHK	H	000200	2	258	250
PROGCODE	C	00A2F2	4	2117	2089 2091
PROGMSG	C	00A2DE	66	2115	2109 2110
PROGPSW	D	000228	8	271	270
R0	U	000000	1	192	263 266 280 282 2109 2162 2168 2201 2229 2233 2257 2260 2262 2264 2266 2277
R1	U	000001	1	193	571 2110 2131 2135 2137 2169 2202 2230 2271 2281
R10	U	00000A	1	202	286 288 293 295 300 302 307 312 317 406 407 441 442 480 481 561 562 596 597 635 636 716 717 751 752 790 791
R11	U	00000B	1	203	
R12	U	00000C	1	204	229 264 324 410 428 445 457 484 549 565 583 600 613 639 704 720 738 755 768 794 858
R13	U	00000D	1	205	265 287 289 294 296 301 303 308 313 318 325 409 429 444

```
     SYMBOL         TYPE  VALUE    LENGTH  DEFN  REFERENCES

                                                458   483   550   564   584   599   614   638   705   719   739   754   769   793
                                                859  2113  2141
R14                  U    00000E        1   206   268   269   326   327
R15                  U    00000F        1   207   228   263   266
R2                   U    000002        1   194   406   408   428   441   443   457   480   482   549   561   563   568   583   596
                                                598   603   613   635   637   704   716   718   723   738   751   753   758   768
                                                790   792   797   858  2111  2132  2138  2170  2203  2231  2258  2260  2266  2267
                                               2268  2270  2277  2278
R3                   U    000003        1   195   406   413   425   441   448   454   480   486   546   561   567   568   580   596
                                                602   603   610   635   641   701   716   722   723   735   751   757   758   765
                                                790   796   797   855  2133  2138
R4                   U    000004        1   196  2135  2150  2152  2174  2213  2217  2221  2225
R5                   U    000005        1   197  2150  2153  2162  2167  2175  2176  2185  2189  2193  2197  2233
R6                   U    000006        1   198  2135  2154
R7                   U    000007        1   199   407   416   422   426   442   451   455   481   493   499   505   511   518   523
                                                528   533   538   543   547   562   571   577   581   597   606   607   611   636
                                                648   654   660   666   673   678   683   688   693   698   702   717   726   732
                                                736   752   761   762   766   791   804   810   816   822   827   832   837   842
                                                847   852   856  2136  2156
R8                   U    000008        1   200   407   417   423   427   442   452   456   481   494   500   506   512   519   524
                                                529   534   539   544   548   562   572   578   582   597   608   612   636   649
                                                655   661   667   674   679   684   689   694   699   703   717   727   733   737
                                                752   763   767   791   805   811   817   823   828   833   838   843   848   853
                                                857  2148  2154
R9                   U    000009        1   201
SAVER0R5             F    00A4D0        4  2248  2162  2233
SAVEREGS             F    00023C        4   273   263   266
START                I    000280        4   280   247
VERIFAIL             I    00A35A        4  2162  2151
VERIFLEN             U    000012        1  2367  2132
VERIFTAB             F    00A5AC        4  2294  2367  2131
VERIFY               I    00A342        2  2148  2136
VERINEXT             I    00A34E        4  2152  2234
VERISUB              H    00A320        2  2126   325
WANTGOT              C    00A490        6  2241  2180  2208
XTOLBAS              F    000334        4   356   300
XTOLCT               U    0000D0        1  1079   357
XTOLFLGS             U    002300        0  1198   360  2331
XTOLFLGS_GOOD        U    007A40        1  1725  1740  2332
XTOLFLGS_NUM         U    000007        1  1740  2333
XTOLIN               D    000A60        8  1061  1079   358
XTOLINOU             D    000AB0        8  1068  1080   394
XTOLINRM             D    000B30        8  1085  1168   376
XTOLOU               F    000394        4   392   317
XTOLOUCT             U    000080        1  1080   393
XTOLOUO              U    003200        0  1213   395  2359
XTOLOUOF             U    003280        0  1215   396  2363
XTOLOUOF_GOOD        U    00A200        1  2075  2080  2364
XTOLOUOF_NUM         U    000002        1  2080  2365
XTOLOUO_GOOD         U    00A000        1  2055  2072  2360
XTOLOUO_NUM          U    000008        1  2072  2361
XTOLOUT              U    002200        0  1196   359  2327
XTOLOUT_GOOD         U    007700        1  1695  1722  2328
XTOLOUT_NUM          U    00000D        1  1722  2329
XTOLRM               F    000364        4   374   302
XTOLRMCT             U    000100        1  1168   375
```

```
     SYMBOL         TYPE  VALUE   LENGTH  DEFN  REFERENCES

XTOLRMO              U    002400       0  1200   377  2335
XTOLRMOF             U    002B00       0  1202   378  2339
XTOLRMOF_GOOD        U    009000       1  1907  2004  2340
XTOLRMOF_NUM         U    000030       1  2004  2341
XTOLRMO_GOOD         U    007C00       1  1743  1904  2336
XTOLRMO_NUM          U    000050       1  1904  2337
XTOSBAS              F    000324       4   350   293
XTOSCT               U    0000D0       1   988   351
XTOSFLGS             U    001980       0  1188   354  2315
XTOSFLGS_GOOD        U    005D40       1  1477  1492  2316
XTOSFLGS_NUM         U    000007       1  1492  2317
XTOSIN               D    000890       8   969   988   352
XTOSINOU             D    0008E0       8   976   989   388
XTOSINRM             D    000960       8   995  1055   370
XTOSOU               F    000384       4   386   312
XTOSOUCT             U    000080       1   989   387
XTOSOUO              U    003100       0  1209   389  2351
XTOSOUOF             U    003180       0  1211   390  2355
XTOSOUOF_GOOD        U    009F80       1  2047  2052  2356
XTOSOUOF_NUM         U    000002       1  2052  2357
XTOSOUO_GOOD         U    009D80       1  2027  2044  2352
XTOSOUO_NUM          U    000008       1  2044  2353
XTOSOUT              U    001900       0  1186   353  2311
XTOSOUT_GOOD         U    005B80       1  1459  1474  2312
XTOSOUT_NUM          U    000007       1  1474  2313
XTOSRM               F    000354       4   368   295
XTOSRMCT             U    000100       1  1055   369
XTOSRMO              U    001A00       0  1190   371  2319
XTOSRMOF             U    001E00       0  1192   372  2323
XTOSRMOF_GOOD        U    006B00       1  1595  1692  2324
XTOSRMOF_NUM         U    000030       1  1692  2325
XTOSRMO_GOOD         U    005F00       1  1495  1592  2320
XTOSRMO_NUM          U    000030       1  1592  2321
=AL2(L'MSGMSG)       R    00A686       2  2371  2262
=CL6'Got:  '         C    00A68E       6  2373  2208
=CL6'Want: '         C    00A688       6  2372  2180
=H'0'                H    00A684       2  2370  2257
```

MACRO DEFN REFERENCES

No defined macros

```
   DESC      SYMBOL     SIZE      POS         ADDR

Entry: 0

Image       IMAGE      42644  0000-A693  0000-A693
  Region                42644  0000-A693  0000-A693
    CSECT   BFPLDRND   42644  0000-A693  0000-A693
```

```
   STMT                                                FILE NAME
1     c:\Users\Fish\Documents\Visual Studio 2008\Projects\MyProjects\ASMA-0\bfp-002-loadr\bfp-002-loadr.asm

** NO ERRORS FOUND **
```