```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                        2 ********************************************************************************
                                                        3 *
                                                        4 *Testcase fix-page
                                                        5 *  A test case for "Simplified Execution Path" of the Fix
                                                        6 *  Page E502 Assist instruction.
                                                        7 *
                                                        8 ********************************************************************************
                                                        9 *
                                                       10 *                          fix-page.asm
                                                       11 *
                                                       12 * Created and placed into public domain 09 OCT 2020 by Bob Polmanter.
                                                       13 * Remove runtest *Compare dependency on 2022-03-08 by Fish
                                                       14 *
                                                       15 * The Fix Page E502 Assist instruction is tested against the definition
                                                       16 * of the Simplified Execution Path as described in the System/370
                                                       17 * Assists for MVS, publication GA22-7079-1.  The tests for the E502
                                                       18 * execution in the problem state are tested against the definition
                                                       19 * in GA22-7072-0 System/370 Extended Facility within the section titled
                                                       20 * Virtual-Machine Extended Facility Assist.
                                                       21 *
                                                       22 * Test data is assembled into this program, and some test data is
                                                       23 * generated by this program. The program itself verifies the resulting
                                                       24 * status of registers and condition codes via simple CLC comparison.
                                                       25 *
                                                       26 *
                                                       27 * Tests performed with Fix Page E502:
                                                       28 *
                                                       29 * TEST #1
                                                       30 * 1.  That GR14 contains the address of the next sequential instruction
                                                       31 *       following the E502 instruction.
                                                       32 * 2.  That GR15 contains the contents of the fullword field MPLPFAL.
                                                       33 * 3.  That the PSW next instruction address is loaded with the fullword
                                                       34 *     field MPLPFAL and that execution resumed at that location.
                                                       35 *
                                                       36 * TEST #2
                                                       37 * 4.  Repeating the essence of Test #1, except that the PSW is in the
                                                       38 *     problem state, and CR6 is set to indicate that a virtual machine
                                                       39 *     is in the virtual supervisor state (CR6 bit 1=0) and the VM
                                                       40 *     Extended Assist feature ("370E") is enabled (CR6 bit 29=1). When
                                                       41 *     CR6 is set with these bits, this is the only case where E502 (and
                                                       42 *     the other E5xx assists) are allowed to execute in real problem
                                                       43 *     state. The conditions 1, 2, and 3 of Test #1 above are reverified
                                                       44 *     for test #2.
                                                       45 *
                                                       46 * TEST #3
                                                       47 * 5.  Validates that when the PSW is in the problem state and CR6 bit
                                                       48 *     1=1 (Virtual problem state) while the 370E feature is enabled
                                                       49 *     (CR6 bit 29=1) that E502 execution results in a privileged
                                                       50 *     operation exception.
                                                       51 *
                                                       52 * TEST #4
                                                       53 * 6.  Validates that when the PSW is in the problem state and CR6 bit
                                                       54 *     29=0 (370E feature disabled) while CR6 also indicates bit 1=0
                                                       55 *     (virtual supervisor state) that E502 execution results in a
                                                       56 *     privileged operation exception.
                                                       57 *
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                       58 *
                                                       59 * NOTE: The other bits in CR6 are used by ECPS:VM and whether or not
                                                       60 *       the other VM assists are enabled, bits 1 and 29 of CR6 still
                                                       61 *       control the virtualization of the E5xx assists regardless of
                                                       62 *       the values of other other bits in CR6.
                                                       63 *
                                                       64 * NOTE: the MPLP is a control block normally maintained by some
                                                       65 *       versions of the S/370 MVS operating system in support of the
                                                       66 *       various Assists. The base address of the MPLP is defined by
                                                       67 *       the second operand of the E502 instruction.  The word MPLPFAL
                                                       68 *       is at offset 0x34 into the MPLP, as described in GA22-7079-1.
                                                       69 *
                                                       70 ************************************************************************
```

```
  LOC         OBJECT CODE        ADDR1     ADDR2     STMT
                                 00000000  0000075F    72 FPA001   START 0
                                 00000000  00000001    73 STRTLABL EQU   *
                                 00000000  00000001    74 R0       EQU   0
                                 00000001  00000001    75 R1       EQU   1
                                 00000002  00000001    76 R2       EQU   2
                                 00000003  00000001    77 R3       EQU   3
                                 00000004  00000001    78 R4       EQU   4
                                 00000005  00000001    79 R5       EQU   5
                                 00000006  00000001    80 R6       EQU   6
                                 00000007  00000001    81 R7       EQU   7
                                 00000008  00000001    82 R8       EQU   8
                                 00000009  00000001    83 R9       EQU   9
                                 0000000A  00000001    84 R10      EQU   10
                                 0000000B  00000001    85 R11      EQU   11
                                 0000000C  00000001    86 R12      EQU   12
                                 0000000D  00000001    87 R13      EQU   13
                                 0000000E  00000001    88 R14      EQU   14
                                 0000000F  00000001    89 R15      EQU   15
                                                       90 *
                                                       91 *
00000000                         00000000              92          USING *,R0
                                                       93 *
                                                       94 * Selected S/370 low core layout
                                                       95 *
                                                       96 *
00000000                         00000000  00000000    97          ORG   STRTLABL+X'00'      Restart PSW
00000000  000C0000 00000200                            98          DC    X'000C0000',A(START)
                                                       99 *
00000008                         00000008  00000020   100          ORG   STRTLABL+X'20'      SVC old PSW
00000020  00000000 00000000                           101 SVCOPSW  DC    X'00000000',A(0)
                                                      102 *
00000028                         00000028  00000028   103          ORG   STRTLABL+X'28'      Program check old PSW
00000028  00000000 00000000                           104 PGMOPSW  DC    X'00000000',A(0)
                                                      105 *
00000030                         00000030  00000060   106          ORG   STRTLABL+X'60'      SVC new PSW
00000060  000C0000 00000340                           107 SVCNPSW  DC    X'000C0000',A(SVCFLIH) SVC handler
                                                      108 *
00000068                         00000068  00000068   109          ORG   STRTLABL+X'68'      Program check new PSW
00000068  000C0000 00000320                           110 PGMNPSW  DC    X'000C0000',A(PGMFLIH) PGM Check handler
                                                      111 *
00000070                         00000070  00000088   112          ORG   STRTLABL+X'88'      interrupt code area EC mode
00000088  00000000                                    113 SVCINTC  DC    X'00000000'          SVC interrupt code area
0000008C  00000000                                    114 PGMINTC  DC    X'00000000'          Prog check interrupt code area
                                                      115 *
00000090                         00000090  000000A4   116          ORG   STRTLABL+X'A4'      Address of MPLP assist control block
000000A4  00000700                                    117 AMPLP    DC    A(MPLP)
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT
                                                     119 ********************************************************************************
                                                     120 *
                                                     121 *  Main program.
                                                     122 *
000000A8                        000000A8  00000200   123          ORG   STRTLABL+X'200'
00000200                                             124 START    DS    0H
00000200  4110 0001                      00000001   125          LA    R1,1                Init
00000204  5010 0600                      00000600   126          ST    R1,RESULTS1         Initialize results area
00000208  5010 0604                      00000604   127          ST    R1,RESULTS2         Initialize results area
0000020C  5010 0608                      00000608   128          ST    R1,RESULTS3         Initialize results area
00000210  5010 060C                      0000060C   129          ST    R1,RESULTS4         Initialize results area
                                                     130 *
                                                     131 ********** Execute Fix Page on simplified path return.
                                                     132 * TEST 1 * PSW in supervisor state
                                                     133 *        * CR6 all bits zero
                                                     134 ********** No program checks should occur
                                                     135 *
                                00000214  00000001   136 TEST1    EQU   *
00000214  4180 0001                      00000001   137          LA    R8,1                Test 1 in progress
00000218  B766 0750                      00000750   138          LCTL  6,6,C6ZERO          Init CR6: all bits off
0000021C  4110 023C                      0000023C   139          LA    R1,SUCCESS1         Value to place in MPLPFAL
00000220  5010 0734                      00000734   140          ST    R1,MPLPFAL          Init the field
                                                     141 *
00000224  9812 073C                      0000073C   142          LM    R1,R2,PGSTART       -> starting,ending page addresses
00000228  5800 0744                      00000744   143          L     R0,PGRADD           -> address within page to be fixed
0000022C  E5020000 00A4                              144          DC    X'E502',AL2(0),S(AMPLP) Fix Page; operand 1 not used
                                                     145 *
                                00000232  00000001   146 FAIL1    EQU   *
00000232  D203 0600 0748        00000600  00000748   147          MVC   RESULTS1,BADRC      Set bad result code
00000238  47F0 0250                      00000250   148          B     TEST2               Go to next test
                                                     149 *
                                0000023C  00000001   150 SUCCESS1 EQU   *
0000023C  4110 0232                      00000232   151          LA    R1,FAIL1            -> instruction after E502
00000240  151E                                       152          CLR   R1,R14              Does R14 contain correct addr?
00000242  0771                                       153          BNER  R1                  No, fail the test
00000244  55F0 0734                      00000734   154          CL    R15,MPLPFAL         Does R15 contain MPLPFAL?
00000248  0771                                       155          BNER  R1                  No, fail the test
0000024A  D203 0600 074C        00000600  0000074C   156          MVC   RESULTS1,GOODRC     Test was successful
                                                     157 *
                                                     158 *
                                                     159 ********** Execute Fix Page on simplified path return.
                                                     160 * TEST 2 * Real PSW in problem state
                                                     161 *        * CR6 = X'00000004'  (CR6 bit 1=0 (virtual supervisor state),
                                                     162 *                              bit 29=1 (370E enabled))
                                                     163 ********** No program checks should occur
                                                     164 *
                                00000250  00000001   165 TEST2    EQU   *
00000250  4180 0002                      00000002   166          LA    R8,2                Test 2 in progress
00000254  B766 0754                      00000754   167          LCTL  6,6,C6ALLOW         Init CR6: allow problem state
00000258  4110 027A                      0000027A   168          LA    R1,SUCCESS2         Value to place in MPLPFAL
0000025C  5010 0734                      00000734   169          ST    R1,MPLPFAL          Init the field
00000260  0A01                                       170          SVC   1                   Enter problem state
                                                     171 *
00000262  9812 073C                      0000073C   172          LM    R1,R2,PGSTART       -> starting,ending page addresses
00000266  5800 0744                      00000744   173          L     R0,PGRADD           -> address within page to be fixed
0000026A  E5020000 00A4                              174          DC    X'E502',AL2(0),S(AMPLP) Fix Page; operand 1 not used
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                     175 *
                                00000270  00000001   176 FAIL2    EQU   *
00000270  D203 0604 0748        00000604  00000748   177          MVC   RESULTS2,BADRC       Set bad result code
00000276  47F0 028E                       0000028E   178          B     TEST3               Go to next test
                                                     179 *
                                0000027A  00000001   180 SUCCESS2 EQU   *
0000027A  4110 0270                       00000270   181          LA    R1,FAIL2            -> instruction after E502
0000027E  151E                                       182          CLR   R1,R14              Does R14 contain correct addr?
00000280  0771                                       183          BNER  R1                  No, fail the test
00000282  55F0 0734                       00000734   184          CL    R15,MPLPFAL         Does R15 contain MPLPFAL?
00000286  0771                                       185          BNER  R1                  No, fail the test
00000288  D203 0604 074C        00000604  0000074C   186          MVC   RESULTS2,GOODRC     Test was successful
                                                     187 *
                                                     188 *
                                                     189 ********** Execute Fix Page on simplified path return.
                                                     190 * TEST 3 * Real PSW in problem state
                                                     191 *        * CR6 = X'40000004'  (CR6 bit 1=1 (virtual PROBLEM state),
                                                     192 *                              bit 29=1 (370E enabled))
                                                     193 ********** Program check 02 should occur
                                                     194 *
                                0000028E  00000001   195 TEST3    EQU   *
0000028E  0A00                                       196          SVC   0                   Back to supervisor state
00000290  4180 0003                       00000003   197          LA    R8,3                Test 3 in progress
00000294  B766 0758                       00000758   198          LCTL  6,6,C6VPROB         Init CR6: virt prob state, 370E
00000298  4110 02BA                       000002BA   199          LA    R1,FAIL3            Value to place in MPLPFAL
0000029C  5010 0734                       00000734   200          ST    R1,MPLPFAL          Init the field
000002A0  0A01                                       201          SVC   1                   Enter problem state
                                                     202 *
000002A2  9812 073C                       0000073C   203          LM    R1,R2,PGSTART       -> starting,ending page addresses
000002A6  5800 0744                       00000744   204          L     R0,PGRADD           -> address within page to be fixed
000002AA  E5020000 00A4                              205          DC    X'E502',AL2(0),S(AMPLP) Fix Page; operand 1 not used
                                                     206 *
                                000002B0  00000001   207 SUCCESS3 EQU   *
000002B0  D203 0608 074C        00000608  0000074C   208          MVC   RESULTS3,GOODRC     Good result (expected PIC occurred)
000002B6  47F0 02C0                       000002C0   209          B     TEST4               Go to next test
                                                     210 *
                                000002BA  00000001   211 FAIL3    EQU   *
000002BA  D203 0608 0748        00000608  00000748   212          MVC   RESULTS3,BADRC      FAIL (E502 ran when it should not)
                                                     213 *
                                                     214 *
                                                     215 *
                                                     216 ********** Execute Fix Page on simplified path return.
                                                     217 * TEST 4 * Real PSW in problem state
                                                     218 *        * CR6 = X'00000000'  (CR6 bit 1=0 (virtual Supv state),
                                                     219 *                              bit 29=0 (370E disabled))
                                                     220 ********** Program check 02 should occur
                                                     221 *
                                000002C0  00000001   222 TEST4    EQU   *
000002C0  0A00                                       223          SVC   0                   Back to supervisor state
000002C2  4180 0004                       00000004   224          LA    R8,4                Test 4 in progress
000002C6  B766 075C                       0000075C   225          LCTL  6,6,C6N370E         Init CR6: virt supv state, 370E OFF
000002CA  4110 02EC                       000002EC   226          LA    R1,FAIL4            Value to place in MPLPFAL
000002CE  5010 0734                       00000734   227          ST    R1,MPLPFAL          Init the field
000002D2  0A01                                       228          SVC   1                   Enter problem state
                                                     229 *
000002D4  9812 073C                       0000073C   230          LM    R1,R2,PGSTART       -> starting,ending page addresses
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT
000002D8  5800 0744                       00000744   231          L     R0,PGRADD            -> address within page to be fixed
000002DC  E5020000 00A4                               232          DC    X'E502',AL2(0),S(AMPLP) Fix Page; operand 1 not used
                                                      233 *
                            000002E2  00000001    234 SUCCESS4 EQU   *
000002E2  D203 060C 074C    0000060C  0000074C    235          MVC   RESULTS4,GOODRC      Good result (expected PIC occurred)
000002E8  47F0 02F2                       000002F2   236          B     EOJ                  All tests completed
                                                      237 *
                            000002EC  00000001    238 FAIL4    EQU   *
000002EC  D203 060C 0748    0000060C  00000748    239          MVC   RESULTS4,BADRC       FAIL (E502 ran when it should not)
                                                      240 *
                            000002F2  00000001    241 EOJ      EQU   *
000002F2  0A00                                    242          SVC   0                    Back to supervisor state
                                                      243 *
                                                      244 **      Verify test results...
                                                      245 *
000002F4  D503 0600 0380    00000600  00000380    246          CLC   RESULTS1,=F'0'
000002FA  4770 033C                       0000033C   247          BNE   FAIL
000002FE  D503 0604 0380    00000604  00000380    248          CLC   RESULTS2,=F'0'
00000304  4770 033C                       0000033C   249          BNE   FAIL
00000308  D503 0608 0380    00000608  00000380    250          CLC   RESULTS3,=F'0'
0000030E  4770 033C                       0000033C   251          BNE   FAIL
00000312  D503 060C 0380    0000060C  00000380    252          CLC   RESULTS4,=F'0'
00000318  4770 033C                       0000033C   253          BNE   FAIL
                                                      254 *
0000031C  8200 0368                       00000368   255          LPSW  GOODPSW              EOJ, load disabled wait PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    257 *
                                                    258 *
                                                    259 * HERE FOR PROGRAM CHECKS
                                                    260 *
00000320                                            261          DS    0D
                               00000320  00000001   262 PGMFLIH  EQU   *                 PGM Check Interruption Routine
00000320  5980 0384                      00000384   263          C     R8,=F'1'          Doing test 1?
00000324  4780 033C                      0000033C   264          BE    FAIL              FAIL, program check not allowed
00000328  5980 0388                      00000388   265          C     R8,=F'2'          Doing test 2?
0000032C  4780 033C                      0000033C   266          BE    FAIL              FAIL, program check not allowed
                                                    267 *
                                                    268 *                             Tests 3 & 4: PIC 02 is expected
00000330  9502 008F                      0000008F   269          CLI   PGMINTC+3,X'02'   priv-op exception?
00000334  4770 033C                      0000033C   270          BNE   FAIL             No, FAIL. Test # in R8.
00000338  8200 0028                      00000028   271          LPSW  PGMOPSW           Expected; resume execution
                                                    272 *
0000033C  8200 0378                      00000378   273 FAIL     LPSW  FAILPSW           Halt on unexpected pgm check.
                                                    274 *                             Failed test # is in R8
                                                    275 *
                                                    276 * HERE FOR SVCs
                                                    277 *
00000340                                            278          DS    0D
                               00000340  00000001   279 SVCFLIH  EQU   *                 SVC Interruption Routine
00000340  9500 008B                      0000008B   280          CLI   SVCINTC+3,X'00'   SVC 0? (switch to supervisor state)
00000344  4780 0354                      00000354   281          BE    SVC000            Yes
00000348  9501 008B                      0000008B   282          CLI   SVCINTC+3,X'01'   SVC 1? (switch to problem state)
0000034C  4780 035C                      0000035C   283          BE    SVC001            Yes
00000350  8200 0370                      00000370   284          LPSW  XSVCPSW           Halt on bad SVC
                                                    285 *
                               00000354  00000001   286 SVC000   EQU   *
00000354  94FE 0021                      00000021   287          NI    SVCOPSW+1,255-X'01' Turn OFF problem bit in old PSW
00000358  8200 0020                      00000020   288          LPSW  SVCOPSW           Resume execution in supv state
                                                    289 *
                               0000035C  00000001   290 SVC001   EQU   *
0000035C  9601 0021                      00000021   291          OI    SVCOPSW+1,X'01'   Turn ON problem bit in old PSW
00000360  8200 0020                      00000020   292          LPSW  SVCOPSW           Resume execution in problem state
                                                    293 *
00000368                                            294          DS    0D                Ensure correct alignment for PSW
00000368  000A0000 00000000                         295 GOODPSW  DC    X'000A000000000000' SUCCESS diabled wait PSW
00000370  000A0000 00000BAD                         296 XSVCPSW  DC    X'000A000000000BAD' Bad SVC # disabled wait PSW
00000378  000A0000 0000DEAD                         297 FAILPSW  DC    X'000A00000000DEAD' TEST FAILED disabled wait PSW
                                                    298 *                             (unexpected program check,
                                                    299 *                              or general test failure)
00000380                                            300          LTORG
00000380  00000000                                  301               =F'0'
00000384  00000001                                  302               =F'1'
00000388  00000002                                  303               =F'2'
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000038C                      0000038C  00000600   305          ORG   STRTLABL+X'600'
00000600  00000000                                 306 RESULTS1 DC    X'00000000'          Return code from test 1
00000604  00000000                                 307 RESULTS2 DC    X'00000000'          Return code from test 2
00000608  00000000                                 308 RESULTS3 DC    X'00000000'          Return code from test 3
0000060C  00000000                                 309 RESULTS4 DC    X'00000000'          Return code from test 4
                                                   310 *
00000610                      00000610  00000700   311          ORG   STRTLABL+X'700'
                                                   312 *
                                                   313 * The MPLP area below defines only the relevant part of the MPLP assist
                                                   314 * control block; in this case, the location at MPLP+X'34' (MPLPFAL)
                                                   315 * must contain the address of where the assist should begin execution
                                                   316 * at the completion of the X'E502' instruction.
                                                   317 *
00000700  00000000                                 318 MPLP     DC    A(0)           Relevant MPLP block definition
00000704  00000000                                 319          DC    A(0)           +4
00000708  00000000                                 320          DC    A(0)           +8
0000070C  00000000                                 321          DC    A(0)           +C
00000710  00000000                                 322          DC    A(0)           +10
00000714  00000000                                 323          DC    A(0)           +14
00000718  00000000                                 324          DC    A(0)           +18
0000071C  00000000                                 325          DC    A(0)           +1C
00000720  00000000                                 326          DC    A(0)           +20
00000724  00000000                                 327          DC    A(0)           +24
00000728  00000000                                 328          DC    A(0)           +28
0000072C  00000000                                 329          DC    A(0)           +2C
00000730  00000000                                 330          DC    A(0)           +30
00000734  00000000                                 331 MPLPFAL  DC    A(0)           +34
00000738  00000000                                 332          DC    A(0)           +38
                                                   333 *
0000073C  00002000                                 334 PGSTART  DC    X'00002000'    -> begin page to fix
00000740  00002000                                 335 PGEND    DC    X'00002000'    -> end page to fix
00000744  00002044                                 336 PGRADD   DC    X'00002044'    -> address within the page to be fixed
00000748  00000008                                 337 BADRC    DC    F'8'           Bad result code (test failed)
0000074C  00000000                                 338 GOODRC   DC    F'0'           Good result code (test success)
00000750  00000000                                 339 C6ZERO   DC    X'00000000'    CR6 init
00000754  00000004                                 340 C6ALLOW  DC    X'00000004'    CR6 Virtual Suprv state + 370E enabled
00000758  40000004                                 341 C6VPROB  DC    X'40000004'    CR6 Virtual Prob state + 370E enabled
0000075C  00000000                                 342 C6N370E  DC    X'00000000'    CR6 Virtual Suprv state but 370E Disabled
                                                   343 *
                                                   344          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
AMPLP	A	0000A4	4	117	144 174 205 232
BADRC	F	000748	4	337	147 177 212 239
C6ALLOW	X	000754	4	340	167
C6N370E	X	00075C	4	342	225
C6VPROB	X	000758	4	341	198
C6ZERO	X	000750	4	339	138
EOJ	U	0002F2	1	241	236
FAIL	I	00033C	4	273	247 249 251 253 264 266 270
FAIL1	U	000232	1	146	151
FAIL2	U	000270	1	176	181
FAIL3	U	0002BA	1	211	199
FAIL4	U	0002EC	1	238	226
FAILPSW	X	000378	8	297	273
FPA001	J	000000	1888	72	
GOODPSW	X	000368	8	295	255
GOODRC	F	00074C	4	338	156 186 208 235
IMAGE	1	000000	1888	0	
MPLP	A	000700	4	318	117
MPLPFAL	A	000734	4	331	140 154 169 184 200 227
PGEND	X	000740	4	335	
PGMFLIH	U	000320	1	262	110
PGMINTC	X	00008C	4	114	269
PGMNPSW	X	000068	4	110	
PGMOPSW	X	000028	4	104	271
PGRADD	X	000744	4	336	143 173 204 231
PGSTART	X	00073C	4	334	142 172 203 230
R0	U	000000	1	74	92 143 173 204 231
R1	U	000001	1	75	125 126 127 128 129 139 140 142 151 152 153 155 168 169 172 181 182 183 185 199 200 203 226 227 230
R10	U	00000A	1	84	
R11	U	00000B	1	85	
R12	U	00000C	1	86	
R13	U	00000D	1	87	
R14	U	00000E	1	88	152 182
R15	U	00000F	1	89	154 184
R2	U	000002	1	76	142 172 203 230
R3	U	000003	1	77	
R4	U	000004	1	78	
R5	U	000005	1	79	
R6	U	000006	1	80	
R7	U	000007	1	81	
R8	U	000008	1	82	137 166 197 224 263 265
R9	U	000009	1	83	
RESULTS1	X	000600	4	306	126 147 156 246
RESULTS2	X	000604	4	307	127 177 186 248
RESULTS3	X	000608	4	308	128 208 212 250
RESULTS4	X	00060C	4	309	129 235 239 252
START	H	000200	2	124	98
STRTLABL	U	000000	1	73	97 100 103 106 109 112 116 123 305 311
SUCCESS1	U	00023C	1	150	139
SUCCESS2	U	00027A	1	180	168
SUCCESS3	U	0002B0	1	207	
SUCCESS4	U	0002E2	1	234	
SVC000	U	000354	1	286	281
SVC001	U	00035C	1	290	283
SVCFLIH	U	000340	1	279	107

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SVCINTC	X	000088	4	113	280 282
SVCNPSW	X	000060	4	107	
SVCOPSW	X	000020	4	101	287 288 291 292
TEST1	U	000214	1	136	
TEST2	U	000250	1	165	148
TEST3	U	00028E	1	195	178
TEST4	U	0002C0	1	222	209
XSVCPSW	X	000370	8	296	284
=F'0'	F	000380	4	301	246 248 250 252
=F'1'	F	000384	4	302	263
=F'2'	F	000388	4	303	265

MACRO DEFN REFERENCES

No defined macros

```
   DESC    SYMBOL  SIZE    POS      ADDR

Entry: 0

Image      IMAGE   1888  000-75F  000-75F
  Region           1888  000-75F  000-75F
    CSECT  FPA001  1888  000-75F  000-75F
```

```
   STMT                                          FILE NAME
1     c:\Users\Fish\Documents\Visual Studio 2008\Projects\MyProjects\ASMA-0\fix-page\fix-page.asm

** NO ERRORS FOUND **
```