```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                        2 ************************************************************************
                                                        3 *
                                                        4 *Testcase IEEE DIVIDE
                                                        5 *  Test case capability includes IEEE exceptions trappable and
                                                        6 *  otherwise. Test results, FPCR flags, and any DXC are saved for all
                                                        7 *  tests.
                                                        8 *
                                                        9 *
                                                       10 *                       ********************
                                                       11 *                       **   IMPORTANT!   **
                                                       12 *                       ********************
                                                       13 *
                                                       14 *       This test uses the Hercules Diagnose X'008' interface
                                                       15 *       to display messages and thus your .tst runtest script
                                                       16 *       MUST contain a "DIAG8CMD ENABLE" statement within it!
                                                       17 *
                                                       18 *
                                                       19 ************************************************************************


                                                       21 ************************************************************************
                                                       22 *
                                                       23 *                          bfp-014-divide.asm
                                                       24 *
                                                       25 *       This assembly-language source file is part of the
                                                       26 *       Hercules Binary Floating Point Validation Package
                                                       27 *                          by Stephen R. Orso
                                                       28 *
                                                       29 * Copyright 2016 by Stephen R Orso.
                                                       30 * Runtest *Compare dependency removed by Fish on 2022-08-16
                                                       31 * PADCSECT macro/usage removed by Fish on 2022-08-16
                                                       32 *
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                                                       56 * PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY
```

```
 LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      57 * OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT
                                                      58 * (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE
                                                      59 * OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.
                                                      60 *
                                                      61 ********************************************************************************



                                                      63 ********************************************************************************
                                                      64 *
                                                      65 * Tests the following three conversion instructions
                                                      66 *   DIVIDE (short BFP, RRE)
                                                      67 *   DIVIDE (long BFP, RRE)
                                                      68 *   DIVIDE (extended BFP, RRE)
                                                      69 *   DIVIDE (short BFP, RXE)
                                                      70 *   DIVIDE (long BFP, RXE)
                                                      71 *
                                                      72 * Test data is compiled into this program.  The test script that runs
                                                      73 * this program can provide alternative test data through Hercules R
                                                      74 * commands.
                                                      75 *
                                                      76 * Test Case Order
                                                      77 * 1) Short BFP basic tests, including traps and NaN propagation
                                                      78 * 2) Short BFP finite number tests, incl. traps and scaling
                                                      79 * 3) Short BFP FPC-controlled rounding mode exhaustive tests
                                                      80 * 4) Long BFP basic tests, including traps and NaN propagation
                                                      81 * 5) Long BFP finite number tests, incl. traps and scaling
                                                      82 * 6) Long BFP FPC-controlled rounding mode exhaustive tests
                                                      83 * 7) Extended BFP basic tests, including traps and NaN propagation
                                                      84 * 8) Extended BFP finite number tests, incl. traps and scaling
                                                      85 * 9) Extended BFP FPC-controlled rounding mode exhaustive tests
                                                      86 *
                                                      87 * Three input test sets are provided each for short, long, and
                                                      88 *   extended BFP inputs.  Test values are the same for each precision
                                                      89 *   for most tests.  Overflow and underflow each require precision-
                                                      90 *   dependent test values.
                                                      91 *
                                                      92 * Also tests the following floating point support instructions
                                                      93 *   LOAD  (Short)
                                                      94 *   LOAD  (Long)
                                                      95 *   LFPC  (Load Floating Point Control Register)
                                                      96 *   SRNMB (Set BFP Rounding Mode 3-bit)
                                                      97 *   STORE (Short)
                                                      98 *   STORE (Long)
                                                      99 *   STFPC (Store Floating Point Control Register)
                                                     100 *
                                                     101 ********************************************************************************
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    103 *
                                                    104 *  Note: for compatibility with the z/CMS test rig, do not change
                                                    105 *  or use R11, R14, or R15.  Everything else is fair game.
                                                    106 *
                               00000000  00011513   107 BFPDIV   START 0
                               00000000  00000001   108 STRTLABL EQU   *
                               00000000  00000001   109 R0       EQU   0                   Work register for cc extraction
                               00000001  00000001   110 R1       EQU   1
                               00000002  00000001   111 R2       EQU   2                   Holds count of test input values
                               00000003  00000001   112 R3       EQU   3                   Points to next test input value(s)
                               00000004  00000001   113 R4       EQU   4                   Rounding tests inner loop control
                               00000005  00000001   114 R5       EQU   5                   Rounding tests outer loop control
                               00000006  00000001   115 R6       EQU   6                   Rounding tests top of inner loop
                               00000007  00000001   116 R7       EQU   7                   Pointer to next result value(s)
                               00000008  00000001   117 R8       EQU   8                   Pointer to next FPCR result
                               00000009  00000001   118 R9       EQU   9                   Rounding tests top of outer loop
                               0000000A  00000001   119 R10      EQU   10                  Pointer to test address list
                               0000000B  00000001   120 R11      EQU   11                  **Reserved for z/CMS test rig
                               0000000C  00000001   121 R12      EQU   12                  Holds number of test cases in set
                               0000000D  00000001   122 R13      EQU   13                  Mainline return address
                               0000000E  00000001   123 R14      EQU   14                  **Return address for z/CMS test rig
                               0000000F  00000001   124 R15      EQU   15                  **Base register on z/CMS or Hyperion
                                                    125 *
                                                    126 * Floating Point Register equates to keep the cross reference clean
                                                    127 *
                               00000000  00000001   128 FPR0     EQU   0
                               00000001  00000001   129 FPR1     EQU   1
                               00000002  00000001   130 FPR2     EQU   2
                               00000003  00000001   131 FPR3     EQU   3
                               00000004  00000001   132 FPR4     EQU   4
                               00000005  00000001   133 FPR5     EQU   5
                               00000006  00000001   134 FPR6     EQU   6
                               00000007  00000001   135 FPR7     EQU   7
                               00000008  00000001   136 FPR8     EQU   8
                               00000009  00000001   137 FPR9     EQU   9
                               0000000A  00000001   138 FPR10    EQU   10
                               0000000B  00000001   139 FPR11    EQU   11
                               0000000C  00000001   140 FPR12    EQU   12
                               0000000D  00000001   141 FPR13    EQU   13
                               0000000E  00000001   142 FPR14    EQU   14
                               0000000F  00000001   143 FPR15    EQU   15
                                                    144 *
00000000                       00000000             145          USING *,R15
00000000                       00011100             146          USING HELPERS,R12
                                                    147 *
                                                    148 * Above works on real iron (R15=0 after sysclear)
                                                    149 * and in z/CMS (R15 points to start of load module)
                                                    150 *


                                                    152 ************************************************************************
                                                    153 *
                                                    154 * Low core definitions, Restart PSW, and Program Check Routine.
                                                    155 *
                                                    156 ************************************************************************
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
00000000                     00000000  0000008E   158          ORG   STRTLABL+X'8E'      Program check interrution code
0000008E  0000                                   159 PCINTCD  DS    H
                                                 160 *
                             00000150  00000001  161 PCOLDPSW EQU   STRTLABL+X'150'     z/Arch Program check old PSW
                                                 162 *
00000090                     00000090  000001A0  163          ORG   STRTLABL+X'1A0'     z/Arch Restart PSW
000001A0  00000001 80000000                      164          DC    X'0000000180000000',AD(START)
                                                 165 *
000001B0                     000001B0  000001D0  166          ORG   STRTLABL+X'1D0'     z/Arch Program check NEW PSW
000001D0  00000000 00000000                      167          DC    X'0000000000000000',AD(PROGCHK)
                                                 168 *
                                                 169 * Program check routine.  If Data Exception, continue execution at
                                                 170 * the instruction following the program check.  Otherwise, hard wait.
                                                 171 * No need to collect data.  All interesting DXC stuff is captured
                                                 172 * in the FPCR.
                                                 173 *
000001E0                     000001E0  00000200  174          ORG   STRTLABL+X'200'
00000200                                         175 PROGCHK  DS    0H              Program check occured...
00000200  9507 F08F                    0000008F  176          CLI   PCINTCD+1,X'07'  Data Exception?
00000204  A774 0004                    0000020C  177          JNE   PCNOTDTA       ..no, hardwait (not sure if R15 is ok)
00000208  B2B2 F150                    00000150  178          LPSWE PCOLDPSW       ..yes, resume program execution

0000020C  900F F23C                    0000023C  180 PCNOTDTA STM   R0,R15,SAVEREGS  Save registers
00000210  58C0 F27C                    0000027C  181          L     R12,AHELPERS     Get address of helper subroutines
00000214  4DD0 C000                    00011100  182          BAS   R13,PGMCK        Report this unexpected program check
00000218  980F F23C                    0000023C  183          LM    R0,R15,SAVEREGS  Restore registers

0000021C  12EE                                   185          LTR   R14,R14        Return address provided?
0000021E  077E                                   186          BNZR  R14            Yes, return to z/CMS test rig.
00000220  B2B2 F228                    00000228  187          LPSWE PROGPSW        Not data exception, enter disabled wait
00000228  00020000 00000000                      188 PROGPSW  DC    0D'0',X'0002000000000000',XL6'00',X'DEAD' Abnormal end
00000238  B2B2 F2F8                    000002F8  189 FAIL     LPSWE FAILPSW        Not data exception, enter disabled wait
0000023C  00000000 00000000                      190 SAVEREGS DC    16F'0'          Registers save area
0000027C  00011100                               191 AHELPERS DC    A(HELPERS)      Address of helper subroutines
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                     193 ************************************************************************
                                                     194 *
                                                     195 *  Main program.  Enable Advanced Floating Point, process test cases.
                                                     196 *
                                                     197 ************************************************************************


00000280                                             199 START    DS    0H
00000280  B600 F308                        00000308  200          STCTL R0,R0,CTLR0    Store CR0 to enable AFP
00000284  9604 F309                        00000309  201          OI    CTLR0+1,X'04'  Turn on AFP bit
00000288  B700 F308                        00000308  202          LCTL  R0,R0,CTLR0    Reload updated CR0
                                                     203 *
0000028C  41A0 F314                        00000314  204          LA    R10,SHORTNF    Point to short BFP non-finite inputs
00000290  4DD0 F3A4                        000003A4  205          BAS   R13,SBFPNF     Divide short BFP non-finites
00000294  41A0 F324                        00000324  206          LA    R10,SHORTF     Point to short BFP finite inputs
00000298  4DD0 F42E                        0000042E  207          BAS   R13,SBFPF      Divide short BFP finites
0000029C  41A0 F334                        00000334  208          LA    R10,RMSHORTS   Point to short BFP rounding mode tests
000002A0  4DD0 F4A4                        000004A4  209          BAS   R13,SBFPRM     Divide short BFP for rounding tests
                                                     210 *
000002A4  41A0 F344                        00000344  211          LA    R10,LONGNF     Point to long BFP non-finite inputs
000002A8  4DD0 F50E                        0000050E  212          BAS   R13,LBFPNF     Divide long BFP non-finites
000002AC  41A0 F354                        00000354  213          LA    R10,LONGF      Point to long BFP finite inputs
000002B0  4DD0 F594                        00000594  214          BAS   R13,LBFPF      Divide long BFP finites
000002B4  41A0 F364                        00000364  215          LA    R10,RMLONGS    Point to long  BFP rounding mode tests
000002B8  4DD0 F60A                        0000060A  216          BAS   R13,LBFPRM     Divide long BFP for rounding tests
                                                     217 *
000002BC  41A0 F374                        00000374  218          LA    R10,XTNDNF     Point to extended BFP non-finite inputs
000002C0  4DD0 F670                        00000670  219          BAS   R13,XBFPNF     Divide extended BFP non-finites
000002C4  41A0 F384                        00000384  220          LA    R10,XTNDF      Point to ext'd BFP finite inputs
000002C8  4DD0 F6E2                        000006E2  221          BAS   R13,XBFPF      Divide ext'd BFP finites
000002CC  41A0 F394                        00000394  222          LA    R10,RMXTNDS    Point to ext'd BFP rounding mode tests
000002D0  4DD0 F740                        00000740  223          BAS   R13,XBFPRM     Divide ext'd BFP for rounding tests
                                                     224 *
                                                     225 ************************************************************************
                                                     226 *                    Verify test results...
                                                     227 ************************************************************************
                                                     228 *
000002D4  58C0 F27C                        0000027C  229          L     R12,AHELPERS     Get address of helper subroutines
000002D8  4DD0 C0A0                        000111A0  230          BAS   R13,VERISUB      Go verify results
000002DC  12EE                                       231          LTR   R14,R14          Was return address provided?
000002DE  077E                                       232          BNZR  R14              Yes, return to z/CMS test rig.
000002E0  B2B2 F2E8                        000002E8  233          LPSWE GOODPSW          Load SUCCESS PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
000002E8                                          235          DS    0D             Ensure correct alignment for PSW
000002E8  00020000 00000000                       236 GOODPSW  DC    X'0002000000000000',AD(0)  Normal end - disabled wait
000002F8  00020000 00000000                       237 FAILPSW  DC    X'0002000000000000',XL6'00',X'0BAD' Abnormal end
                                                  238 *
00000308  00000000                                239 CTLR0    DS    F
0000030C  00000000                                240 FPCREGNT DC    X'00000000'  FPCR, trap no IEEE exceptions, zero flags
00000310  F8000000                                241 FPCREGTR DC    X'F8000000'  FPCR, trap all IEEE exceptions, zero flags
                                                  242 *
                                                  243 * Input values parameter list, four fullwords for each test data set
                                                  244 *      1) Count,
                                                  245 *      2) Address of inputs,
                                                  246 *      3) Address to place results, and
                                                  247 *      4) Address to place DXC/Flags/cc values.
                                                  248 *
00000314                                          249 SHORTNF  DS    0F           Input pairs for short BFP non-finite tests
00000314  00000008                                250          DC    A(SBFPNFCT)
00000318  000007A0                                251          DC    A(SBFPNFIN)
0000031C  00001000                                252          DC    A(SBFPNFOT)
00000320  00001400                                253          DC    A(SBFPNFFL)
                                                  254 *
00000324                                          255 SHORTF   DS    0F           Input pairs for short BFP finite tests
00000324  00000006                                256          DC    A(SBFPCT)
00000328  000007C0                                257          DC    A(SBFPIN)
0000032C  00001800                                258          DC    A(SBFPOUT)
00000330  00001900                                259          DC    A(SBFPFLGS)
                                                  260 *
00000334                                          261 RMSHORTS DS    0F           Input pairs for short BFP rounding testing
00000334  00000004                                262          DC    A(SBFPRMCT)
00000338  000007F0                                263          DC    A(SBFPINRM)
0000033C  00001A00                                264          DC    A(SBFPRMO)
00000340  00001D00                                265          DC    A(SBFPRMOF)
                                                  266 *
00000344                                          267 LONGNF   DS    0F           Input pairs for long BFP non-finite testing
00000344  00000008                                268          DC    A(LBFPNFCT)
00000348  00000810                                269          DC    A(LBFPNFIN)
0000034C  00003000                                270          DC    A(LBFPNFOT)
00000350  00003800                                271          DC    A(LBFPNFFL)
                                                  272 *
00000354                                          273 LONGF    DS    0F           Input pairs for long BFP finite testing
00000354  00000006                                274          DC    A(LBFPCT)
00000358  00000850                                275          DC    A(LBFPIN)
0000035C  00003C00                                276          DC    A(LBFPOUT)
00000360  00003E00                                277          DC    A(LBFPFLGS)
                                                  278 *
00000364                                          279 RMLONGS  DS    0F           Input pairs for long BFP rounding testing
00000364  00000004                                280          DC    A(LBFPRMCT)
00000368  000008B0                                281          DC    A(LBFPINRM)
0000036C  00004000                                282          DC    A(LBFPRMO)
00000370  00004500                                283          DC    A(LBFPRMOF)
                                                  284 *
00000374                                          285 XTNDNF   DS    0F           Inputs for ext'd BFP non-finite testing
00000374  00000008                                286          DC    A(XBFPNFCT)
00000378  000008F0                                287          DC    A(XBFPNFIN)
0000037C  00005000                                288          DC    A(XBFPNFOT)
00000380  00005800                                289          DC    A(XBFPNFFL)
                                                  290 *
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00000384                                        291 XTNDF    DS    0F           Inputs for ext'd BFP finite testing
00000384  00000006                              292          DC    A(XBFPCT)
00000388  00000970                              293          DC    A(XBFPIN)
0000038C  00005C00                              294          DC    A(XBFPOUT)
00000390  00005E00                              295          DC    A(XBFPFLGS)
                                                296 *
00000394                                        297 RMXTNDS  DS    0F           Inputs for ext'd BFP non-finite testing
00000394  00000004                              298          DC    A(XBFPRMCT)
00000398  00000A30                              299          DC    A(XBFPINRM)
0000039C  00006000                              300          DC    A(XBFPRMO)
000003A0  00006A00                              301          DC    A(XBFPRMOF)
                                                302 *
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      304 ************************************************************************
                                                      305 *
                                                      306 * Perform Divide using provided short BFP inputs.  This set of tests
                                                      307 * checks NaN propagation, operations on values that are not finite
                                                      308 * numbers, and other basic tests.  This set generates results that can
                                                      309 * be validated against Figure 19-20 on page 19-27 of SA22-7832-10.
                                                      310 *
                                                      311 * Four results are generated for each input: one RRE with all
                                                      312 * exceptions non-trappable, a second RRE with all exceptions trappable,
                                                      313 * a third RXE with all exceptions non-trappable, a fourth RXE with all
                                                      314 * exceptions trappable,
                                                      315 *
                                                      316 * The quotient and FPCR are stored for each result.
                                                      317 *
                                                      318 ************************************************************************

000003A4                                              320 SBFPNF   DS    0H            BFP Short non-finite values tests
000003A4  9823 A000                   00000000    321           LM    R2,R3,0(R10)  Get count and address of divide values
000003A8  9878 A008                   00000008    322           LM    R7,R8,8(R10)  Get address of result area and flag area.
000003AC  1222                                    323           LTR   R2,R2         Any test cases?
000003AE  078D                                    324           BZR   R13           ..No, return to caller
000003B0  0DC0                                    325           BASR  R12,0         Set top of loop
                                                      326 *
000003B2  9845 A000                   00000000    327           LM    R4,R5,0(R10)  Get count and start of divisor values
                                                      328 *                         ..which are the same as the dividends
000003B6  0D60                                    329           BASR  R6,0          Set top of inner loop
                                                      330 *
000003B8  7880 3000                   00000000    331           LE    FPR8,0(,R3)   Get short BFP dividend
000003BC  7810 5000                   00000000    332           LE    FPR1,0(,R5)   Get short BFP divisor
000003C0  B29D F30C                   0000030C    333           LFPC  FPCREGNT      Set exceptions non-trappable
000003C4  B30D 0081                               334           DEBR  FPR8,FPR1     Divide FPR0/FPR1 RRE
000003C8  7080 7000                   00000000    335           STE   FPR8,0(,R7)   Store short BFP quotient
000003CC  B29C 8000                   00000000    336           STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                      337 *
000003D0  7880 3000                   00000000    338           LE    FPR8,0(,R3)   Get short BFP dividend
000003D4  7810 5000                   00000000    339           LE    FPR1,0(,R5)   Get short BFP divisor
000003D8  B29D F310                   00000310    340           LFPC  FPCREGTR      Set exceptions trappable
000003DC  B30D 0081                               341           DEBR  FPR8,FPR1     Divide FPR0/FPR1 RRE
000003E0  7080 7004                   00000004    342           STE   FPR8,4(,R7)   Store short BFP quotient
000003E4  B29C 8004                   00000004    343           STFPC 4(R8)         Store resulting FPCR flags and DXC
                                                      344 *
000003E8  7880 3000                   00000000    345           LE    FPR8,0(,R3)   Get short BFP dividend
000003EC  7810 5000                   00000000    346           LE    FPR1,0(,R5)   Get short BFP divisor
000003F0  B29D F30C                   0000030C    347           LFPC  FPCREGNT      Set exceptions non-trappable
000003F4  ED80 5000 000D              00000000    348           DEB   FPR8,0(,R5)   Divide FPR0/FPR1 RXE
000003FA  7080 7008                   00000008    349           STE   FPR8,8(,R7)   Store short BFP quotient
000003FE  B29C 8008                   00000008    350           STFPC 8(R8)         Store resulting FPCR flags and DXC
                                                      351 *
00000402  7880 3000                   00000000    352           LE    FPR8,0(,R3)   Get short BFP dividend
00000406  B29D F310                   00000310    353           LFPC  FPCREGTR      Set exceptions trappable
0000040A  ED80 5000 000D              00000000    354           DEB   FPR8,0(,R5)   Divide FPR0/FPR1 RXE
00000410  7080 700C                   0000000C    355           STE   FPR8,12(,R7)  Store short BFP quotient
00000414  B29C 800C                   0000000C    356           STFPC 12(R8)        Store resulting FPCR flags and DXC
                                                      357 *
00000418  4150 5004                   00000004    358           LA    R5,4(,R5)     Point to next divisor value
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000041C  4170 7010                    00000010   359          LA    R7,16(,R7)    Point to next Divide result area
00000420  4180 8010                    00000010   360          LA    R8,16(,R8)    Point to next Divide FPCR area
00000424  0646                                    361          BCTR  R4,R6         Loop through right-hand values
                                                  362 *
00000426  4130 3004                    00000004   363          LA    R3,4(,R3)     Point to next input dividend
0000042A  062C                                    364          BCTR  R2,R12        Convert next input value.
0000042C  07FD                                    365          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    367 ************************************************************************
                                                    368 *
                                                    369 * Perform Divide using provided short BFP input pairs.  This set of
                                                    370 * tests triggers IEEE exceptions Overflow, Underflow, and Inexact and
                                                    371 * collects results when the exceptions do not result in a trap and when
                                                    372 * they do.
                                                    373 *
                                                    374 * Four results are generated for each input: one RRE with all
                                                    375 * exceptions non-trappable, a second RRE with all exceptions trappable,
                                                    376 * a third RXE with all exceptions non-trappable, a fourth RXE with all
                                                    377 * exceptions trappable,
                                                    378 *
                                                    379 * The quotient and FPCR are stored for each result.
                                                    380 *
                                                    381 ************************************************************************

0000042E  9823 A000                 00000000    383 SBFPF    LM    R2,R3,0(R10)  Get count and address of test input values
00000432  9878 A008                 00000008    384          LM    R7,R8,8(R10)  Get address of result area and flag area.
00000436  1222                                  385          LTR   R2,R2         Any test cases?
00000438  078D                                  386          BZR   R13           ..No, return to caller
0000043A  0DC0                                  387          BASR  R12,0         Set top of loop
                                                    388 *
0000043C  B29D F30C                 0000030C    389          LFPC  FPCREGNT      Set exceptions non-trappable
00000440  7880 3000                 00000000    390          LE    FPR8,0(,R3)   Get short BFP dividend
00000444  7810 3004                 00000004    391          LE    FPR1,4(,R3)   Get short BFP divisor
00000448  B30D 0081                             392          DEBR  FPR8,FPR1     Divide FPR8/FPR1 RRE non-trappable
0000044C  7080 7000                 00000000    393          STE   FPR8,0(,R7)   Store short BFP quotient
00000450  B29C 8000                 00000000    394          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                    395 *
00000454  B29D F310                 00000310    396          LFPC  FPCREGTR      Set exceptions trappable
00000458  7880 3000                 00000000    397          LE    FPR8,0(,R3)   Reload short BFP dividend
                                                    398 *                        ..divisor is still in FPR1
0000045C  B30D 0081                             399          DEBR  FPR8,FPR1     Divide FPR8/FPR1 RRE trappable
00000460  7080 7004                 00000004    400          STE   FPR8,4(,R7)   Store short BFP quotient
00000464  B29C 8004                 00000004    401          STFPC 4(R8)         Store resulting FPCR flags and DXC
                                                    402 *
00000468  B29D F30C                 0000030C    403          LFPC  FPCREGNT      Set exceptions non-trappable
0000046C  7880 3000                 00000000    404          LE    FPR8,0(,R3)   Reload short BFP dividend
00000470  ED80 3004 000D            00000004    405          DEB   FPR8,4(,R3)   Divide FPR8 by divisor RXE non-trappable
00000476  7080 7008                 00000008    406          STE   FPR8,8(,R7)   Store short BFP quotient
0000047A  B29C 8008                 00000008    407          STFPC 8(R8)         Store resulting FPCR flags and DXC
                                                    408 *
0000047E  B29D F310                 00000310    409          LFPC  FPCREGTR      Set exceptions trappable
00000482  7880 3000                 00000000    410          LE    FPR8,0(,R3)   Reload short BFP dividend
00000486  ED80 3004 000D            00000004    411          DEB   FPR8,4(,R3)   Divide FPR8 by divisor RXE trappable
0000048C  7080 700C                 0000000C    412          STE   FPR8,12(,R7)  Store short BFP quotient
00000490  B29C 800C                 0000000C    413          STFPC 12(R8)        Store resulting FPCR flags and DXC
                                                    414 *
00000494  4130 3008                 00000008    415          LA    R3,8(,R3)     Point to next input value pair
00000498  4170 7010                 00000010    416          LA    R7,16(,R7)    Point to next quotient pair
0000049C  4180 8010                 00000010    417          LA    R8,16(,R8)    Point to next FPCR result area
000004A0  062C                                  418          BCTR  R2,R12        Convert next input value.
000004A2  07FD                                  419          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    421 ********************************************************************************
                                                    422 *
                                                    423 * Perform Divide using provided short BFP input pairs.  This set of
                                                    424 * tests exhaustively tests all rounding modes available for Divide.
                                                    425 * The rounding mode can only be specified in the FPC.
                                                    426 *
                                                    427 * All five FPC rounding modes are tested because the preceeding tests,
                                                    428 * using rounding mode RNTE, do not often create results that require
                                                    429 * rounding.
                                                    430 *
                                                    431 * Two results are generated for each input and rounding mode: one RRE
                                                    432 * and one RXE.  Traps are disabled for all rounding mode tests.
                                                    433 *
                                                    434 * The quotient and FPCR contents are stored for each test.
                                                    435 *
                                                    436 ********************************************************************************

000004A4  9823 A000                 00000000   438 SBFPRM   LM    R2,R3,0(R10)  Get count and address of test input values
000004A8  9878 A008                 00000008   439          LM    R7,R8,8(R10)  Get address of result area and flag area.
000004AC  1222                                 440          LTR   R2,R2         Any test cases?
000004AE  078D                                 441          BZR   R13           ..No, return to caller
000004B0  1711                                 442          XR    R1,R1         Zero register 1 for use in IC/STC/indexing
000004B2  0DC0                                 443          BASR  R12,0         Set top of test case loop
                                               444
000004B4  4150 0005                 00000005   445          LA    R5,FPCMCT     Get count of FPC modes to be tested
000004B8  0D90                                 446          BASR  R9,0          Set top of rounding mode outer loop
                                               447 *
000004BA  4315 F797                 00000797   448          IC    R1,FPCMODES-L'FPCMODES(R5)  Get next FPC mode
                                               449 *
000004BE  B29D F30C                 0000030C   450          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000004C2  B2B8 1000                 00000000   451          SRNMB 0(R1)         Set FPC Rounding Mode
000004C6  7880 3000                 00000000   452          LE    FPR8,0(,R3)   Get short BFP dividend
000004CA  7810 3004                 00000004   453          LE    FPR1,4(,R3)   Get short BFP divisor
000004CE  B30D 0081                            454          DEBR  FPR8,FPR1     Divide RRE FPR8/FPR1 non-trappable
000004D2  7080 7000                 00000000   455          STE   FPR8,0(,R7)   Store short BFP quotient
000004D6  B29C 8000                 00000000   456          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                               457 *
000004DA  B29D F30C                 0000030C   458          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
000004DE  B2B8 1000                 00000000   459          SRNMB 0(R1)         Set FPC Rounding Mode
000004E2  7880 3000                 00000000   460          LE    FPR8,0(,R3)   Get short BFP dividend
000004E6  ED80 3004 000D            00000004   461          DEB   FPR8,4(,R3)   Divide RXE FPR8 by divisor non-trappable
000004EC  7080 7004                 00000004   462          STE   FPR8,4(,R7)   Store short BFP quotient
000004F0  B29C 8004                 00000004   463          STFPC 4(R8)         Store resulting FPCR flags and DXC
                                               464 *
000004F4  4170 7008                 00000008   465          LA    R7,8(,R7)     Point to next quotient result set
000004F8  4180 8008                 00000008   466          LA    R8,8(,R8)     Point to next FPCR result area
                                               467 *
000004FC  0659                                 468          BCTR  R5,R9         Iterate to next FPC mode
                                               469 *
                                               470 * End of FPC modes to be tested.  Advance to next test case.
                                               471 *
000004FE  4130 3008                 00000008   472          LA    R3,8(,R3)     Point to next input value pair
00000502  4170 7008                 00000008   473          LA    R7,8(,R7)     Skip to start of next result area
00000506  4180 8008                 00000008   474          LA    R8,8(,R8)     Skip to start of next FPCR result area
0000050A  062C                                 475          BCTR  R2,R12        Divide next input value lots of times
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      476 *
0000050C  07FD                                        477          BR    R13           All converted; return.
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      479 ************************************************************************
                                                      480 *
                                                      481 * Perform Divide using provided long BFP inputs.  This set of tests
                                                      482 * checks NaN propagation, operations on values that are not finite
                                                      483 * numbers, and other basic tests.  This set generates results that can
                                                      484 * be validated against Figure 19-20 on page 19-27 of SA22-7832-10.
                                                      485 *
                                                      486 * Four results are generated for each input: one RRE with all
                                                      487 * exceptions non-trappable, a second RRE with all exceptions trappable,
                                                      488 * a third RXE with all exceptions non-trappable, a fourth RXE with all
                                                      489 * exceptions trappable,
                                                      490 *
                                                      491 * The quotient and FPCR are stored for each result.
                                                      492 *
                                                      493 ************************************************************************

0000050E                                              495 LBFPNF   DS    0H            BFP long non-finite values tests
0000050E  9823 A000                 00000000          496          LM    R2,R3,0(R10)  Get count and address of dividend values
00000512  9878 A008                 00000008          497          LM    R7,R8,8(R10)  Get address of result area and flag area.
00000516  1222                                        498          LTR   R2,R2         Any test cases?
00000518  078D                                        499          BZR   R13           ..No, return to caller
0000051A  0DC0                                        500          BASR  R12,0         Set top of loop
                                                      501 *
0000051C  9845 A000                 00000000          502          LM    R4,R5,0(R10)  Get count and start of divisor values
                                                      503 *                             ..which are the same as the dividends
00000520  0D60                                        504          BASR  R6,0          Set top of inner loop
                                                      505 *
00000522  6880 3000                 00000000          506          LD    FPR8,0(,R3)   Get long BFP dividend
00000526  6810 5000                 00000000          507          LD    FPR1,0(,R5)   Get long BFP divisor
0000052A  B29D F30C                 0000030C          508          LFPC  FPCREGNT      Set exceptions non-trappable
0000052E  B31D 0081                                   509          DDBR  FPR8,FPR1     Divide FPR0/FPR1 RRE
00000532  6080 7000                 00000000          510          STD   FPR8,0(,R7)   Store long BFP quotient
00000536  B29C 8000                 00000000          511          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                      512 *
0000053A  6880 3000                 00000000          513          LD    FPR8,0(,R3)   Get long BFP dividend
0000053E  6810 5000                 00000000          514          LD    FPR1,0(,R5)   Get long BFP divisor
00000542  B29D F310                 00000310          515          LFPC  FPCREGTR      Set exceptions trappable
00000546  B31D 0081                                   516          DDBR  FPR8,FPR1     Divide FPR0/FPR1 RRE
0000054A  6080 7008                 00000008          517          STD   FPR8,8(,R7)   Store long BFP remainder
0000054E  B29C 8004                 00000004          518          STFPC 4(R8)         Store resulting FPCR flags and DXC
                                                      519 *
00000552  6880 3000                 00000000          520          LD    FPR8,0(,R3)   Get long BFP dividend
00000556  B29D F30C                 0000030C          521          LFPC  FPCREGNT      Set exceptions non-trappable
0000055A  ED80 5000 001D            00000000          522          DDB   FPR8,0(,R5)   Divide FPR0/FPR1 RXE
00000560  6080 7010                 00000010          523          STD   FPR8,16(,R7)  Store long BFP quotient
00000564  B29C 8008                 00000008          524          STFPC 8(R8)         Store resulting FPCR flags and DXC
                                                      525 *
00000568  6880 3000                 00000000          526          LD    FPR8,0(,R3)   Get long BFP dividend
0000056C  B29D F310                 00000310          527          LFPC  FPCREGTR      Set exceptions trappable
00000570  ED80 5000 001D            00000000          528          DDB   FPR8,0(,R5)   Divide FPR0/FPR1 RXE
00000576  6080 7018                 00000018          529          STD   FPR8,24(,R7)  Store long BFP remainder
0000057A  B29C 800C                 0000000C          530          STFPC 12(R8)        Store resulting FPCR flags and DXC
                                                      531 *
0000057E  4150 5008                 00000008          532          LA    R5,8(,R5)     Point to next divisor value
00000582  4170 7020                 00000020          533          LA    R7,32(,R7)    Point to next Divide result area
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

00000586  4180 8010                       00000010   534          LA    R8,16(,R8)    Point to next Divide FPCR area
0000058A  0646                                       535          BCTR  R4,R6         Loop through right-hand values
                                                     536 *
0000058C  4130 3008                       00000008   537          LA    R3,8(,R3)     Point to next dividend value
00000590  062C                                       538          BCTR  R2,R12        Divide until all cases tested
00000592  07FD                                       539          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                    541 ************************************************************************
                                                    542 *
                                                    543 * Perform Divide using provided long BFP input pairs.  This set of
                                                    544 * tests triggers IEEE exceptions Overflow, Underflow, and Inexact and
                                                    545 * collects results when the exceptions do not result in a trap and when
                                                    546 * they do.
                                                    547 *
                                                    548 * Four results are generated for each input: one RRE with all
                                                    549 * exceptions non-trappable, a second RRE with all exceptions trappable,
                                                    550 * a third RXE with all exceptions non-trappable, a fourth RXE with all
                                                    551 * exceptions trappable,
                                                    552 *
                                                    553 * The result and FPCR are stored for each result.
                                                    554 *
                                                    555 ************************************************************************

00000594  9823 A000                 00000000    557 LBFPF    LM    R2,R3,0(R10)  Get count and address of test input values
00000598  9878 A008                 00000008    558          LM    R7,R8,8(R10)  Get address of result area and flag area.
0000059C  1222                                  559          LTR   R2,R2         Any test cases?
0000059E  078D                                  560          BZR   R13           ..No, return to caller
000005A0  0DC0                                  561          BASR  R12,0         Set top of loop
                                                    562 *
000005A2  B29D F30C                 0000030C    563          LFPC  FPCREGNT      Set exceptions non-trappable
000005A6  6880 3000                 00000000    564          LD    FPR8,0(,R3)   Get short BFP dividend
000005AA  6810 3008                 00000008    565          LD    FPR1,8(,R3)   Get short BFP divisor
000005AE  B31D 0081                             566          DDBR  FPR8,FPR1     Divide FPR8/FPR1 RRE non-trappable
000005B2  6080 7000                 00000000    567          STD   FPR8,0(,R7)   Store short BFP quotient
000005B6  B29C 8000                 00000000    568          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                    569 *
000005BA  B29D F310                 00000310    570          LFPC  FPCREGTR      Set exceptions trappable
000005BE  6880 3000                 00000000    571          LD    FPR8,0(,R3)   Reload short BFP dividend
                                                    572 *                        ..divisor is still in FPR1
000005C2  B31D 0081                             573          DDBR  FPR8,FPR1     Divide FPR8/FPR1 RRE trappable
000005C6  6080 7008                 00000008    574          STD   FPR8,8(,R7)   Store short BFP quotient
000005CA  B29C 8004                 00000004    575          STFPC 4(R8)         Store resulting FPCR flags and DXC
                                                    576 *
000005CE  B29D F30C                 0000030C    577          LFPC  FPCREGNT      Set exceptions non-trappable
000005D2  6880 3000                 00000000    578          LD    FPR8,0(,R3)   Reload short BFP dividend
000005D6  ED80 3008 001D            00000008    579          DDB   FPR8,8(,R3)   Divide FPR8/FPR1 RXE non-trappable
000005DC  6080 7010                 00000010    580          STD   FPR8,16(,R7)  Store short BFP quotient
000005E0  B29C 8008                 00000008    581          STFPC 8(R8)         Store resulting FPCR flags and DXC
                                                    582 *
000005E4  B29D F310                 00000310    583          LFPC  FPCREGTR      Set exceptions trappable
000005E8  6880 3000                 00000000    584          LD    FPR8,0(,R3)   Reload short BFP dividend
000005EC  ED80 3008 001D            00000008    585          DDB   FPR8,8(,R3)   Divide FPR8/FPR1 RXE trappable
000005F2  6080 7018                 00000018    586          STD   FPR8,24(,R7)  Store short BFP quotient
000005F6  B29C 800C                 0000000C    587          STFPC 12(R8)        Store resulting FPCR flags and DXC
                                                    588 *
000005FA  4130 3010                 00000010    589          LA    R3,16(,R3)    Point to next input value pair
000005FE  4170 7020                 00000020    590          LA    R7,32(,R7)    Point to next quotent result pair
00000602  4180 8010                 00000010    591          LA    R8,16(,R8)    Point to next FPCR result area
00000606  062C                                  592          BCTR  R2,R12        Convert next input value.
00000608  07FD                                  593          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    595 ************************************************************************
                                                    596 *
                                                    597 * Perform Divide using provided long BFP input pairs.  This set of
                                                    598 * tests exhaustively tests all rounding modes available for Divide.
                                                    599 * The rounding mode can only be specified in the FPC.
                                                    600 *
                                                    601 * All five FPC rounding modes are tested because the preceeding tests,
                                                    602 * using rounding mode RNTE, do not often create results that require
                                                    603 * rounding.
                                                    604 *
                                                    605 * Two results are generated for each input and rounding mode: one RRE
                                                    606 * and one RXE.  Traps are disabled for all rounding mode tests.
                                                    607 *
                                                    608 * The quotient and FPCR contents are stored for each test.
                                                    609 *
                                                    610 ************************************************************************

0000060A  9823 A000                 00000000    612 LBFPRM   LM    R2,R3,0(R10)  Get count and address of test input values
0000060E  9878 A008                 00000008    613          LM    R7,R8,8(R10)  Get address of result area and flag area.
00000612  1222                                  614          LTR   R2,R2         Any test cases?
00000614  078D                                  615          BZR   R13           ..No, return to caller
00000616  1711                                  616          XR    R1,R1         Zero register 1 for use in IC/STC/indexing
00000618  0DC0                                  617          BASR  R12,0         Set top of test case loop
                                                618
0000061A  4150 0005                 00000005    619          LA    R5,FPCMCT     Get count of FPC modes to be tested
0000061E  0D90                                  620          BASR  R9,0          Set top of rounding mode loop
                                                621 *
00000620  4315 F797                 00000797    622          IC    R1,FPCMODES-L'FPCMODES(R5)  Get next FPC mode
                                                623 *
00000624  B29D F30C                 0000030C    624          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000628  B2B8 1000                 00000000    625          SRNMB 0(R1)         Set FPC Rounding Mode
0000062C  6880 3000                 00000000    626          LD    FPR8,0(,R3)   Get long BFP dividend
00000630  6810 3008                 00000008    627          LD    FPR1,8(,R3)   Get long BFP divisor
00000634  B31D 0081                             628          DDBR  FPR8,FPR1     Divide RRE FPR8/FPR1 non-trappable
00000638  6080 7000                 00000000    629          STD   FPR8,0(,R7)   Store long BFP quotient
0000063C  B29C 8000                 00000000    630          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                631 *
00000640  B29D F30C                 0000030C    632          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
00000644  B2B8 1000                 00000000    633          SRNMB 0(R1)         Set FPC Rounding Mode
00000648  6880 3000                 00000000    634          LD    FPR8,0(,R3)   Reload long BFP dividend
0000064C  ED80 3008 001D            00000008    635          DDB   FPR8,8(,R3)   Divide RXE FPR8 by divisor non-trappable
00000652  6080 7008                 00000008    636          STD   FPR8,8(,R7)   Store long BFP quotient
00000656  B29C 8004                 00000004    637          STFPC 4(R8)         Store resulting FPCR flags and DXC
                                                638 *
0000065A  4170 7010                 00000010    639          LA    R7,16(,R7)    Point to next quotient result set
0000065E  4180 8008                 00000008    640          LA    R8,8(,R8)     Point to next FPCR result area
                                                641 *
00000662  0659                                  642          BCTR  R5,R9         Iterate to next FPC mode
                                                643 *
                                                644 * End of FPC modes to be tested.  Advance to next test case.
                                                645 *
00000664  4130 3010                 00000010    646          LA    R3,16(,R3)    Point to next input value pair
00000668  4180 8008                 00000008    647          LA    R8,8(,R8)     Skip to start of next FPCR result area
0000066C  062C                                  648          BCTR  R2,R12        Divide next input value lots of times
                                                649 *
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
0000066E  07FD                                650          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    652 ************************************************************************
                                                    653 *
                                                    654 * Perform Divide using provided extended BFP inputs.  This set of tests
                                                    655 * checks NaN propagation, operations on values that are not finite
                                                    656 * numbers, and other basic tests.  This set generates results that can
                                                    657 * be validated against Figure 19-20 on page 19-27 of SA22-7832-10.
                                                    658 *
                                                    659 * Two results are generated for each input: one RRE with all
                                                    660 * exceptions non-trappable, and a second RRE with all exceptions
                                                    661 * trappable.  Extended BFP Divide does not have an RXE format.
                                                    662 *
                                                    663 * The quotient and FPCR are stored for each result.
                                                    664 *
                                                    665 ************************************************************************


00000670                                            667 XBFPNF   DS    0H            BFP extended non-finite values tests
00000670  9823 A000                 00000000       668         LM    R2,R3,0(R10)  Get count and address of dividend values
00000674  9878 A008                 00000008       669         LM    R7,R8,8(R10)  Get address of result area and flag area.
00000678  1222                                      670         LTR   R2,R2         Any test cases?
0000067A  078D                                      671         BZR   R13           ..No, return to caller
0000067C  0DC0                                      672         BASR  R12,0         Set top of loop
                                                    673 *
0000067E  9845 A000                 00000000       674         LM    R4,R5,0(R10)  Get count and start of divisor values
                                                    675 *                           ..which are the same as the dividends
00000682  0D60                                      676         BASR  R6,0          Set top of inner loop
                                                    677 *
00000684  6880 3000                 00000000       678         LD    FPR8,0(,R3)   Get extended BFP dividend part 1
00000688  68A0 3008                 00000008       679         LD    FPR10,8(,R3)  Get extended BFP dividend part 2
0000068C  6810 5000                 00000000       680         LD    FPR1,0(,R5)   Get extended BFP divisor part 1
00000690  6830 5008                 00000008       681         LD    FPR3,8(,R5)   Get extended BFP divisor part 2
00000694  B29D F30C                 0000030C       682         LFPC  FPCREGNT      Set exceptions non-trappable
00000698  B34D 0081                                 683         DXBR  FPR8,FPR1     Divide FPR0/FPR1 RRE
0000069C  6080 7000                 00000000       684         STD   FPR8,0(,R7)   Store extended BFP quotient part 1
000006A0  60A0 7008                 00000008       685         STD   FPR10,8(,R7)  Store extended BFP quotient part 2
000006A4  B29C 8000                 00000000       686         STFPC 0(R8)         Store resulting FPCR flags and DXC
                                                    687 *
000006A8  6880 3000                 00000000       688         LD    FPR8,0(,R3)   Get extended BFP dividend part 1
000006AC  68A0 3008                 00000008       689         LD    FPR10,8(,R3)  Get extended BFP dividend part 2
000006B0  6810 5000                 00000000       690         LD    FPR1,0(,R5)   Get extended BFP divisor part 1
000006B4  6830 5008                 00000008       691         LD    FPR3,8(,R5)   Get extended BFP divisor part 2
000006B8  B29D F310                 00000310       692         LFPC  FPCREGTR      Set exceptions trappable
000006BC  B34D 0081                                 693         DXBR  FPR8,FPR1     Divide FPR0/FPR1 RRE
000006C0  6080 7010                 00000010       694         STD   FPR8,16(,R7)  Store extended BFP quotient part 1
000006C4  60A0 7018                 00000018       695         STD   FPR10,24(,R7) Store extended BFP quotient part 2
000006C8  B29C 8004                 00000004       696         STFPC 4(R8)         Store resulting FPCR flags and DXC
                                                    697 *
000006CC  4150 5010                 00000010       698         LA    R5,16(,R5)    Point to next divisor value
000006D0  4170 7020                 00000020       699         LA    R7,32(,R7)    Point to next Divide result area
000006D4  4180 8010                 00000010       700         LA    R8,16(,R8)    Point to next Divide FPCR area
000006D8  0646                                      701         BCTR  R4,R6         Loop through right-hand values
                                                    702 *
000006DA  4130 3010                 00000010       703         LA    R3,16(,R3)    Point to next dividend value
000006DE  062C                                      704         BCTR  R2,R12        Divide until all cases tested
000006E0  07FD                                      705         BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    707 ************************************************************************
                                                    708 *
                                                    709 * Perform Divide using provided extended BFP input pairs.  This set of
                                                    710 * tests triggers IEEE exceptions Overflow, Underflow, and Inexact and
                                                    711 * collects results when the exceptions do not result in a trap and when
                                                    712 * they do.
                                                    713 *
                                                    714 * Two results are generated for each input: one RRE with all
                                                    715 * exceptions non-trappable and a second RRE with all exceptions
                                                    716 * trappable.  There is no RXE format for Divide in extended precision.
                                                    717 *
                                                    718 * The result and FPCR are stored for each result.
                                                    719 *
                                                    720 ************************************************************************


000006E2  9823 A000                 00000000   722 XBFPF    LM    R2,R3,0(R10)  Get count and address of test input values
000006E6  9878 A008                 00000008   723          LM    R7,R8,8(R10)  Get address of result area and flag area.
000006EA  1222                                 724          LTR   R2,R2         Any test cases?
000006EC  078D                                 725          BZR   R13           ..No, return to caller
000006EE  0DC0                                 726          BASR  R12,0         Set top of loop
                                               727 *
000006F0  B29D F30C                 0000030C   728          LFPC  FPCREGNT      Set exceptions non-trappable
000006F4  68D0 3000                 00000000   729          LD    FPR13,0(,R3)  Get extended BFP dividend part 1
000006F8  68F0 3008                 00000008   730          LD    FPR15,8(,R3)  Get extended BFP dividend part 2
000006FC  6810 3010                 00000010   731          LD    FPR1,16(,R3)  Get extended BFP divisor part 1
00000700  6830 3018                 00000018   732          LD    FPR3,24(,R3)  Get extended BFP divisor part 2
00000704  B34D 00D1                            733          DXBR  FPR13,FPR1    Divide FPR8-10/FPR1-3 RRE non-trappable
00000708  60D0 7000                 00000000   734          STD   FPR13,0(,R7)  Store extended BFP quotient part 1
0000070C  60F0 7008                 00000008   735          STD   FPR15,8(,R7)  Store extended BFP quotient part 2
00000710  B29C 8000                 00000000   736          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                               737 *
00000714  B29D F310                 00000310   738          LFPC  FPCREGTR      Set exceptions trappable
00000718  68D0 3000                 00000000   739          LD    FPR13,0(,R3)  Reload extended BFP dividend part 1
0000071C  68F0 3008                 00000008   740          LD    FPR15,8(,R3)  Reload extended BFP dividend part 2
                                               741 *                            ..divisor is still in FPR1-FPR3
00000720  B34D 00D1                            742          DXBR  FPR13,FPR1    Divide FPR13-15/FPR1-3 RRE trappable
00000724  60D0 7010                 00000010   743          STD   FPR13,16(,R7) Store extended BFP quotient part 1
00000728  60F0 7018                 00000018   744          STD   FPR15,24(,R7) Store extended BFP quotient part 2
0000072C  B29C 8004                 00000004   745          STFPC 4(R8)         Store resulting FPCR flags and DXC
                                               746 *
00000730  4130 3020                 00000020   747          LA    R3,32(,R3)    Point to next input value pair
00000734  4170 7020                 00000020   748          LA    R7,32(,R7)    Point to next quotent result pair
00000738  4180 8010                 00000010   749          LA    R8,16(,R8)    Point to next FPCR result area
0000073C  062C                                 750          BCTR  R2,R12        Convert next input value.
                                               751 *
0000073E  07FD                                 752          BR    R13           All converted; return.
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    754 ************************************************************************
                                                    755 *
                                                    756 * Perform Divide using provided long BFP input pairs.  This set of
                                                    757 * tests exhaustively tests all rounding modes available for Divide.
                                                    758 * The rounding mode can only be specified in the FPC.
                                                    759 *
                                                    760 * All five FPC rounding modes are tested because the preceeding tests,
                                                    761 * using rounding mode RNTE, do not often create results that require
                                                    762 * rounding.
                                                    763 *
                                                    764 * Two results are generated for each input and rounding mode: one RRE
                                                    765 * and one RXE.  Traps are disabled for all rounding mode tests.
                                                    766 *
                                                    767 * The quotient and FPCR contents are stored for each test.
                                                    768 *
                                                    769 ************************************************************************

00000740  9823 A000                 00000000   771 XBFPRM   LM    R2,R3,0(R10)  Get count and address of test input values
00000744  9878 A008                 00000008   772          LM    R7,R8,8(R10)  Get address of result area and flag area.
00000748  1222                                 773          LTR   R2,R2         Any test cases?
0000074A  078D                                 774          BZR   R13           ..No, return to caller
0000074C  1711                                 775          XR    R1,R1         Zero register 1 for use in IC/STC/indexing
0000074E  0DC0                                 776          BASR  R12,0         Set top of test case loop
                                               777
00000750  4150 0005                 00000005   778          LA    R5,FPCMCT     Get count of FPC modes to be tested
00000754  0D90                                 779          BASR  R9,0          Set top of rounding mode loop
                                               780 *
00000756  4315 F797                 00000797   781          IC    R1,FPCMODES-L'FPCMODES(R5)  Get next FPC mode
                                               782 *
0000075A  B29D F30C                 0000030C   783          LFPC  FPCREGNT      Set exceptions non-trappable, clear flags
0000075E  B2B8 1000                 00000000   784          SRNMB 0(R1)         Set FPC Rounding Mode
00000762  6880 3000                 00000000   785          LD    FPR8,0(,R3)   Get extended BFP dividend part 1
00000766  68A0 3008                 00000008   786          LD    FPR10,8(,R3)  Get extended BFP dividend part 2
0000076A  6810 3010                 00000010   787          LD    FPR1,16(,R3)  Get extended BFP divisor part 1
0000076E  6830 3018                 00000018   788          LD    FPR3,24(,R3)  Get extended BFP divisor part 2
00000772  B34D 0081                            789          DXBR  FPR8,FPR1     Divide RRE FPR8/FPR1 non-trappable
00000776  6080 7000                 00000000   790          STD   FPR8,0(,R7)   Store extended BFP quotient part 1
0000077A  60A0 7008                 00000008   791          STD   FPR10,8(,R7)  Store extended BFP quotient part 2
0000077E  B29C 8000                 00000000   792          STFPC 0(R8)         Store resulting FPCR flags and DXC
                                               793 *
00000782  4170 7010                 00000010   794          LA    R7,16(,R7)    Point to next quotient result set
00000786  4180 8004                 00000004   795          LA    R8,4(,R8)     Point to next FPCR result area
                                               796 *
0000078A  0659                                 797          BCTR  R5,R9         Iterate to next FPC mode
                                               798 *
                                               799 * End of FPC modes to be tested.  Advance to next test case.
                                               800 *
0000078C  4130 3020                 00000020   801          LA    R3,32(,R3)    Point to next input value pair
00000790  4180 800C                 0000000C   802          LA    R8,12(,R8)    Skip to start of next FPCR result area
00000794  062C                                 803          BCTR  R2,R12        Divide next input value lots of times
                                               804 *
00000796  07FD                                 805          BR    R13           All converted; return.
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

                                                     807 ********************************************************************************
                                                     808 *
                                                     809 * Table of FPC rounding modes to test quotient rounding modes.
                                                     810 *
                                                     811 * The Set BFP Rounding Mode does allow specification of the FPC
                                                     812 * rounding mode as an address, so we shall index into a table of
                                                     813 * BFP rounding modes without bothering with Execute.
                                                     814 *
                                                     815 ********************************************************************************


                                                     817 *
                                                     818 * Rounding modes that may be set in the FPCR.  The FPCR controls
                                                     819 * rounding of the quotient.
                                                     820 *
                                                     821 * These are indexed directly by the loop counter, which counts down.
                                                     822 * So the modes are listed in reverse order here.
                                                     823 *
00000798                                             824 FPCMODES DS    0C
00000798  07                                         825          DC    AL1(7)              RFS, Round for shorter precision
00000799  03                                         826          DC    AL1(3)              RM, Round to -infinity
0000079A  02                                         827          DC    AL1(2)              RP, Round to +infinity
0000079B  01                                         828          DC    AL1(1)              RZ, Round to zero
0000079C  00                                         829          DC    AL1(0)              RNTE, Round to Nearest, ties to even
                            00000005  00000001     830 FPCMCT   EQU   *-FPCMODES          Count of FPC Modes to be tested
                                                     831 *
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      833 ********************************************************************************
                                                      834 *
                                                      835 * Short BFP test data sets for Divide testing.
                                                      836 *
                                                      837 * The first test data set is used for tests of basic functionality,
                                                      838 * NaN propagation, and results from operations involving other than
                                                      839 * finite numbers.
                                                      840 *
                                                      841 * The second test data set is used for testing boundary conditions
                                                      842 * using two finite non-zero values.  Each possible condition code
                                                      843 * and type of result (normal, scaled, etc) is created by members of
                                                      844 * this test data set.
                                                      845 *
                                                      846 * The third test data set is used for exhaustive testing of final
                                                      847 * results across the five rounding modes available for the Divide
                                                      848 * instruction.
                                                      849 *
                                                      850 ********************************************************************************


                                                      852 ********************************************************************************
                                                      853 *
                                                      854 * First input test data set, to test operations using non-finite or
                                                      855 * zero inputs.  Member values chosen to validate part 1 of Figure 19-21
                                                      856 * on page 19-29 of SA22-7832-10.  Each value in this table is tested
                                                      857 * against every other value in the table.
                                                      858 *
                                                      859 ********************************************************************************

000007A0                                              861 SBFPNFIN DS    0F                Inputs for short BFP non-finite tests
000007A0  FF800000                                    862          DC    X'FF800000'         -inf
000007A4  C0000000                                    863          DC    X'C0000000'         -2.0
000007A8  80000000                                    864          DC    X'80000000'         -0
000007AC  00000000                                    865          DC    X'00000000'         +0
000007B0  40000000                                    866          DC    X'40000000'         +2.0
000007B4  7F800000                                    867          DC    X'7F800000'         +inf
000007B8  FFCB0000                                    868          DC    X'FFCB0000'         -QNaN
000007BC  7F8A0000                                    869          DC    X'7F8A0000'         +SNaN
                          00000008  00000001         870 SBFPNFCT EQU   (*-SBFPNFIN)/4    Count of short BFP in list


                                                      872 ********************************************************************************
                                                      873 *
                                                      874 * Second input test data set.  These are finite pairs intended to
                                                      875 * trigger overflow, underflow, and inexact exceptions.  Each pair is
                                                      876 * divided twice, once non-trappable and once trappable.  Trappable
                                                      877 * overflow or underflow yields a scaled result.  Trappable inexact
                                                      878 * will show whether the Incremented DXC code is returned.
                                                      879 *
                                                      880 * The following test cases are required:
                                                      881 * 1. Overflow
                                                      882 * 2. Underflow
                                                      883 * 3. Inexact - incremented
                                                      884 * 4. Inexact - truncated
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                      885 *
                                                      886 ********************************************************************************


000007C0                                              888 SBFPIN   DS    0F                Inputs for short BFP finite tests
                                                      889 *
                                                      890 * Following forces quotient overflow.
                                                      891 *
000007C0  7F7FFFFF                                    892          DC    X'7F7FFFFF'         +maxvalue
000007C4  00000001                                    893          DC    X'00000001'         +minvalue (tiny)
                                                      894 *
                                                      895 * Divide the smallest possible normal by 2.0 to get the largest
                                                      896 * possible tiny, and get underflow in the process.
                                                      897 *
000007C8  00800000                                    898          DC    X'00800000'         smallest possible normal
000007CC  40000000                                    899          DC    X'40000000'         divide by 2.0, force underflow
                                                      900 *
                                                      901 * Divide 1.0 by 10.0 to get 0.1, a repeating fraction that must be
                                                      902 * rounded in any precision.  Inexact, Incremented.
                                                      903 *
000007D0  3F800000                                    904          DC    X'3F800000'         +1
000007D4  41200000                                    905          DC    X'41200000'         +10.0
                                                      906 *
                                                      907 * Divide 7.0 by 10.0 to get 0.7, a repeating fraction that must be
                                                      908 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                      909 *
000007D8  40100000                                    910          DC    X'40100000'         7.0
000007DC  41200000                                    911          DC    X'41200000'         +10.0
                                                      912 *
                                                      913 * Divide 1.0 by -10.0 to get -0.1, a repeating fraction that must be
                                                      914 * rounded in any precision.  Inexact, Incremented.
                                                      915 *
000007E0  3F800000                                    916          DC    X'3F800000'         +1
000007E4  C1200000                                    917          DC    X'C1200000'         -10.0
                                                      918 *
                                                      919 * Divide 7.0 by -10.0 to get 0.7, a repeating fraction that must be
                                                      920 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                      921 *
000007E8  40100000                                    922          DC    X'40100000'         7.0
000007EC  C1200000                                    923          DC    X'C1200000'         -10.0
                                                      924 *
                            00000006  00000001        925 SBFPCT   EQU   (*-SBFPIN)/4/2    Count of short BFP in list


                                                      927 ********************************************************************************
                                                      928 *
                                                      929 * Third input test data set.  These are finite pairs intended to
                                                      930 * test all combinations of rounding mode for the quotient and the
                                                      931 * remainder.  Values are chosen to create a requirement to round
                                                      932 * to the target precision after the computation
                                                      933 *
                                                      934 ********************************************************************************


000007F0                                              936 SBFPINRM DS    0F                Inputs for short BFP rounding testing
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                    937 *
                                                    938 * Divide 1.0 by 10.0 to get 0.1, a repeating fraction that must be
                                                    939 * rounded in any precision.  Inexact, Incremented.
                                                    940 *
000007F0  3F800000                                  941          DC    X'3F800000'         +1
000007F4  41200000                                  942          DC    X'41200000'         +10.0
                                                    943 *
                                                    944 * Divide 7.0 by 10.0 to get 0.7, a repeating fraction that must be
                                                    945 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                    946 *
000007F8  40100000                                  947          DC    X'40100000'         7.0
000007FC  41200000                                  948          DC    X'41200000'         +10.0
                                                    949 *
                                                    950 * Divide 1.0 by -10.0 to get -0.1, a repeating fraction that must be
                                                    951 * rounded in any precision.  Inexact, Incremented.
                                                    952 *
00000800  3F800000                                  953          DC    X'3F800000'         +1
00000804  C1200000                                  954          DC    X'C1200000'         -10.0
                                                    955 *
                                                    956 * Divide 7.0 by -10.0 to get 0.7, a repeating fraction that must be
                                                    957 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                    958 *
00000808  40100000                                  959          DC    X'40100000'         7.0
0000080C  C1200000                                  960          DC    X'C1200000'         -10.0
                                                    961 *
                          00000004  00000001      962 SBFPRMCT EQU   (*-SBFPINRM)/4/2  Count of short BFP rounding tests
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                      964 ********************************************************************
                                                      965 *
                                                      966 * Long BFP test data sets for Divide testing.
                                                      967 *
                                                      968 * The first test data set is used for tests of basic functionality,
                                                      969 * NaN propagation, and results from operations involving other than
                                                      970 * finite numbers.
                                                      971 *
                                                      972 * The second test data set is used for testing boundary conditions
                                                      973 * using two finite non-zero values.  Each possible condition code
                                                      974 * and type of result (normal, scaled, etc) is created by members of
                                                      975 * this test data set.
                                                      976 *
                                                      977 * The third test data set is used for exhaustive testing of final
                                                      978 * results across the five rounding modes available for the Divide
                                                      979 * instruction.
                                                      980 *
                                                      981 ********************************************************************


                                                      983 ********************************************************************
                                                      984 *
                                                      985 * First input test data set, to test operations using non-finite or
                                                      986 * zero inputs.  Member values chosen to validate part 1 of Figure 19-21
                                                      987 * on page 19-29 of SA22-7832-10.  Each value in this table is tested
                                                      988 * against every other value in the table.
                                                      989 *
                                                      990 ********************************************************************


00000810                                              992 LBFPNFIN DS    0F                Inputs for long BFP testing
00000810  FFF00000 00000000                          993          DC    X'FFF0000000000000'         -inf
00000818  C0000000 00000000                          994          DC    X'C000000000000000'         -2.0
00000820  80000000 00000000                          995          DC    X'8000000000000000'         -0
00000828  00000000 00000000                          996          DC    X'0000000000000000'         +0
00000830  40000000 00000000                          997          DC    X'4000000000000000'         +2.0
00000838  7FF00000 00000000                          998          DC    X'7FF0000000000000'         +inf
00000840  FFF8B000 00000000                          999          DC    X'FFF8B00000000000'         -QNaN
00000848  7FF0A000 00000000                         1000          DC    X'7FF0A00000000000'         +SNaN
                             00000008  00000001    1001 LBFPNFCT EQU   (*-LBFPNFIN)/8     Count of long BFP in list


                                                     1003 ********************************************************************
                                                     1004 *
                                                     1005 * Second input test data set.  These are finite pairs intended to
                                                     1006 * trigger overflow, underflow, and inexact exceptions.  Each pair is
                                                     1007 * divided twice, once non-trappable and once trappable.  Trappable
                                                     1008 * overflow or underflow yields a scaled result.  Trappable inexact
                                                     1009 * will show whether the Incremented DXC code is returned.
                                                     1010 *
                                                     1011 * The following test cases are required:
                                                     1012 * 1. Overflow
                                                     1013 * 2. Underflow
                                                     1014 * 3. Inexact - incremented
                                                     1015 * 4. Inexact - truncated
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                    1016 *
                                                    1017 ********************************************************************************


00000850                                            1019 LBFPIN   DS    0D                Inputs for long BFP finite tests
                                                    1020 *
                                                    1021 * Following forces quotient overflow.
                                                    1022 *
00000850  7FEFFFFF FFFFFFFF                         1023          DC    X'7FEFFFFFFFFFFFFF' +maxvalue
00000858  00000000 00000001                         1024          DC    X'0000000000000001' +minvalue (tiny)
                                                    1025 *
                                                    1026 * Divide the smallest possible normal by 2.0 to get the largest
                                                    1027 * possible tiny, and get underflow in the process.
                                                    1028 *
00000860  00100000 00000000                         1029          DC    X'0010000000000000' smallest possible normal
00000868  40000000 00000000                         1030          DC    X'4000000000000000' divide by 2.0, force underflow
                                                    1031 *
                                                    1032 * Divide 1.0 by 10.0 to get 0.1, a repeating fraction that must be
                                                    1033 * rounded in any precision.  Inexact, Incremented.
                                                    1034 *
00000870  3FF00000 00000000                         1035          DC    X'3FF0000000000000'         +1
00000878  40240000 00000000                         1036          DC    X'4024000000000000'         +10.0
                                                    1037 *
                                                    1038 * Divide 7.0 by 10.0 to get 0.7, a repeating fraction that must be
                                                    1039 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                    1040 *
00000880  401C0000 00000000                         1041          DC    X'401C000000000000'         7.0
00000888  40240000 00000000                         1042          DC    X'4024000000000000'         +10.0
                                                    1043 *
                                                    1044 * Divide 1.0 by -10.0 to get -0.1, a repeating fraction that must be
                                                    1045 * rounded in any precision.  Inexact, Incremented.
                                                    1046 *
00000890  3FF00000 00000000                         1047          DC    X'3FF0000000000000'         +1
00000898  C0240000 00000000                         1048          DC    X'C024000000000000'         -10.0
                                                    1049 *
                                                    1050 * Divide 7.0 by -10.0 to get -0.7, a repeating fraction that must be
                                                    1051 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                    1052 *
000008A0  401C0000 00000000                         1053          DC    X'401C000000000000'         7.0
000008A8  C0240000 00000000                         1054          DC    X'C024000000000000'         -10.0
                                                    1055 *
                            00000006  00000001      1056 LBFPCT   EQU   (*-LBFPIN)/8/2   Count of long BFP in list * 8


                                                    1058 ********************************************************************************
                                                    1059 *
                                                    1060 * Third input test data set.  These are finite pairs intended to
                                                    1061 * test all combinations of rounding mode for the quotient and the
                                                    1062 * remainder.  Values are chosen to create a requirement to round
                                                    1063 * to the target precision after the computation
                                                    1064 *
                                                    1065 ********************************************************************************


000008B0                                            1067 LBFPINRM DS    0F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    1068 *
                                                    1069 * Divide 1.0 by 10.0 to get 0.1, a repeating fraction that must be
                                                    1070 * rounded in any precision.  Inexact, Incremented.
                                                    1071 *
000008B0  3FF00000 00000000                         1072          DC    X'3FF0000000000000'         +1
000008B8  40240000 00000000                         1073          DC    X'4024000000000000'         +10.0
                                                    1074 *
                                                    1075 * Divide 7.0 by 10.0 to get 0.7, a repeating fraction that must be
                                                    1076 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                    1077 *
000008C0  401C0000 00000000                         1078          DC    X'401C000000000000'         7.0
000008C8  40240000 00000000                         1079          DC    X'4024000000000000'         +10.0
                                                    1080 *
                                                    1081 * Divide 1.0 by -10.0 to get -0.1, a repeating fraction that must be
                                                    1082 * rounded in any precision.  Inexact, Incremented.
                                                    1083 *
000008D0  3FF00000 00000000                         1084          DC    X'3FF0000000000000'         +1
000008D8  C0240000 00000000                         1085          DC    X'C024000000000000'         -10.0
                                                    1086 *
                                                    1087 * Divide 7.0 by -10.0 to get -0.7, a repeating fraction that must be
                                                    1088 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                    1089 *
000008E0  401C0000 00000000                         1090          DC    X'401C000000000000'         7.0
000008E8  C0240000 00000000                         1091          DC    X'C024000000000000'         -10.0
                                                    1092 *
                            00000004  00000001      1093 LBFPRMCT EQU   (*-LBFPINRM)/8/2  Count of long BFP rounding tests * 8
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                    1095 ********************************************************************
                                                    1096 *
                                                    1097 * Extended BFP test data sets for Divide testing.
                                                    1098 *
                                                    1099 * The first test data set is used for tests of basic functionality,
                                                    1100 * NaN propagation, and results from operations involving other than
                                                    1101 * finite numbers.
                                                    1102 *
                                                    1103 * The second test data set is used for testing boundary conditions
                                                    1104 * using two finite non-zero values.  Each possible condition code
                                                    1105 * and type of result (normal, scaled, etc) is created by members of
                                                    1106 * this test data set.
                                                    1107 *
                                                    1108 * The third test data set is used for exhaustive testing of final
                                                    1109 * results across the five rounding modes available for the Divide
                                                    1110 * instruction.
                                                    1111 *
                                                    1112 ********************************************************************



                                                    1114 ********************************************************************
                                                    1115 *
                                                    1116 * First input test data set, to test operations using non-finite or
                                                    1117 * zero inputs.  Member values chosen to validate part 1 of Figure 19-21
                                                    1118 * on page 19-29 of SA22-7832-10.  Each value in this table is tested
                                                    1119 * against every other value in the table.
                                                    1120 *
                                                    1121 ********************************************************************


000008F0                                            1123 XBFPNFIN DS    0F                Inputs for extended BFP testing
000008F0  FFFF0000 00000000                         1124          DC    X'FFFF0000000000000000000000000000'         -inf
00000900  C0000000 00000000                         1125          DC    X'C0000000000000000000000000000000'         -2.0
00000910  80000000 00000000                         1126          DC    X'80000000000000000000000000000000'         -0
00000920  00000000 00000000                         1127          DC    X'00000000000000000000000000000000'         +0
00000930  40000000 00000000                         1128          DC    X'40000000000000000000000000000000'         +2.0
00000940  7FFF0000 00000000                         1129          DC    X'7FFF0000000000000000000000000000'         +inf
00000950  FFFF8B00 00000000                         1130          DC    X'FFFF8B0000000000000000000000000000'       -QNaN
00000960  7FFF0A00 00000000                         1131          DC    X'7FFF0A0000000000000000000000000000'       +SNaN
                            00000008  00000001      1132 XBFPNFCT EQU   (*-XBFPNFIN)/16     Count of extended BFP in list


                                                    1134 ********************************************************************
                                                    1135 *
                                                    1136 * Second input test data set.  These are finite pairs intended to
                                                    1137 * trigger overflow, underflow, and inexact exceptions.  Each pair is
                                                    1138 * divided twice, once non-trappable and once trappable.  Trappable
                                                    1139 * overflow or underflow yields a scaled result.  Trappable inexact
                                                    1140 * will show whether the Incremented DXC code is returned.
                                                    1141 *
                                                    1142 * The following test cases are required:
                                                    1143 * 1. Overflow
                                                    1144 * 2. Underflow
                                                    1145 * 3. Inexact - incremented
                                                    1146 * 4. Inexact - truncated
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT
                                                    1147 *
                                                    1148 ********************************************************************************


00000970                                            1150 XBFPIN   DS    0F                Inputs for long BFP finite tests
                                                    1151 *
                                                    1152 * Following forces quotient overflow.
                                                    1153 *
00000970  7FFEFFFF FFFFFFFF                         1154          DC    X'7FFEFFFFFFFFFFFFFFFFFFFFFFFFFFFF' +maxvalue
00000980  00000000 00000000                         1155          DC    X'00000000000000000000000000000001' +minvalue (tiny)
                                                    1156 *
                                                    1157 * Divide the smallest possible normal by 2.0 to get the largest
                                                    1158 * possible tiny, and get underflow in the process.
                                                    1159 *
00000990  00010000 00000000                         1160          DC    X'00010000000000000000000000000000' smallest normal
000009A0  40000000 00000000                         1161          DC    X'40000000000000000000000000000000' divide by 2.0
                                                    1162 *
                                                    1163 * Divide 1.0 by 10.0 to get 0.1, a repeating fraction that must be
                                                    1164 * rounded in any precision.  Inexact, Incremented.
                                                    1165 *
000009B0  3FFF0000 00000000                         1166          DC    X'3FFF0000000000000000000000000000'  +1
000009C0  40024000 00000000                         1167          DC    X'40024000000000000000000000000000'  +10.0
                                                    1168 *
                                                    1169 * Divide 7.0 by 10.0 to get 0.7, a repeating fraction that must be
                                                    1170 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                    1171 *
000009D0  4001C000 00000000                         1172          DC    X'4001C0000000000000000000000000'  +7.0
000009E0  40024000 00000000                         1173          DC    X'40024000000000000000000000000000'  +10.0
                                                    1174 *
                                                    1175 * Divide 1.0 by -10.0 to get -0.1, a repeating fraction that must be
                                                    1176 * rounded in any precision.  Inexact, Incremented.
                                                    1177 *
000009F0  3FFF0000 00000000                         1178          DC    X'3FFF0000000000000000000000000000'  +1
00000A00  C0024000 00000000                         1179          DC    X'C0024000000000000000000000000000'  -10.0
                                                    1180 *
                                                    1181 * Divide 7.0 by -10.0 to get -0.7, a repeating fraction that must be
                                                    1182 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                    1183 *
00000A10  4001C000 00000000                         1184          DC    X'4001C0000000000000000000000000'  +7.0
00000A20  C0024000 00000000                         1185          DC    X'C0024000000000000000000000000000'  -10.0
                                                    1186 *
                            00000006  00000001      1187 XBFPCT   EQU   (*-XBFPIN)/16/2   Count of long BFP in list * 8


                                                    1189 ********************************************************************************
                                                    1190 *
                                                    1191 * Third input test data set.  These are finite pairs intended to
                                                    1192 * test all combinations of rounding mode for the quotient and the
                                                    1193 * remainder.  Values are chosen to create a requirement to round
                                                    1194 * to the target precision after the computation
                                                    1195 *
                                                    1196 ********************************************************************************


00000A30                                            1198 XBFPINRM DS    0D
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                   1199 *
                                                   1200 * Divide 1.0 by 10.0 to get 0.1, a repeating fraction that must be
                                                   1201 * rounded in any precision.  Inexact, Incremented.
                                                   1202 *
00000A30  3FFF0000 00000000                        1203          DC    X'3FFF0000000000000000000000000000'  +1
00000A40  40024000 00000000                        1204          DC    X'40024000000000000000000000000000'  +10.0
                                                   1205 *
                                                   1206 * Divide 7.0 by 10.0 to get 0.7, a repeating fraction that must be
                                                   1207 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                   1208 *
00000A50  4001C000 00000000                        1209          DC    X'4001C000000000000000000000000000'  +7.0
00000A60  40024000 00000000                        1210          DC    X'40024000000000000000000000000000'  +10.0
                                                   1211 *
                                                   1212 * Divide 1.0 by -10.0 to get -0.1, a repeating fraction that must be
                                                   1213 * rounded in any precision.  Inexact, Incremented.
                                                   1214 *
00000A70  3FFF0000 00000000                        1215          DC    X'3FFF0000000000000000000000000000'  +1
00000A80  C0024000 00000000                        1216          DC    X'C0024000000000000000000000000000'  -10.0
                                                   1217 *
                                                   1218 * Divide 7.0 by -10.0 to get -0.7, a repeating fraction that must be
                                                   1219 * rounded in any precision.  But this one rounds down.  Inexact only.
                                                   1220 *
00000A90  4001C000 00000000                        1221          DC    X'4001C000000000000000000000000000'  +7.0
00000AA0  C0024000 00000000                        1222          DC    X'C0024000000000000000000000000000'  -10.0
                                                   1223 *
                           00000004  00000001      1224 XBFPRMCT EQU   (*-XBFPINRM)/16/2  Count of long BFP rounding tests
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                          1226 ********************************************************************************
                                          1227 *                    ACTUAL results saved here
                                          1228 ********************************************************************************
                                          1229 *
                                          1230 *                 Locations for ACTUAL results
                                          1231 *
                                          1232 *
                          00001000  00000001 1233 SBFPNFOT EQU   STRTLABL+X'1000'    Integer short non-finite BFP results
                                          1234 *                                    ..room for 64 tests, 64 used
                          00001400  00000001 1235 SBFPNFFL EQU   STRTLABL+X'1400'    FPCR flags and DXC from short BFP
                                          1236 *                                    ..room for 64 tests, 64 used
                                          1237 *
                          00001800  00000001 1238 SBFPOUT  EQU   STRTLABL+X'1800'    Integer short BFP finite results
                                          1239 *                                    ..room for 16 tests, 6 used
                          00001900  00000001 1240 SBFPFLGS EQU   STRTLABL+X'1900'    FPCR flags and DXC from short BFP
                                          1241 *                                    ..room for 16 tests, 6 used
                                          1242 *
                          00001A00  00000001 1243 SBFPRMO  EQU   STRTLABL+X'1A00'    Short BFP rounding mode test results
                                          1244 *                                    ..Room for 16, 4 used.
                          00001D00  00000001 1245 SBFPRMOF EQU   STRTLABL+X'1D00'    Short BFP rounding mode FPCR results
                                          1246 *                                    ..Room for 16, 4 used.
                                          1247 *                                    ..next location starts at X'2000'
                                          1248 *
                          00003000  00000001 1249 LBFPNFOT EQU   STRTLABL+X'3000'    Integer long non-finite BFP results
                                          1250 *                                    ..room for 64 tests, 64 used
                          00003800  00000001 1251 LBFPNFFL EQU   STRTLABL+X'3800'    FPCR flags and DXC from long BFP
                                          1252 *                                    ..room for 64 tests, 64 used
                                          1253 *
                          00003C00  00000001 1254 LBFPOUT  EQU   STRTLABL+X'3C00'    Integer long BFP finite results
                                          1255 *                                    ..room for 16 tests, 6 used
                          00003E00  00000001 1256 LBFPFLGS EQU   STRTLABL+X'3E00'    FPCR flags and DXC from long BFP
                                          1257 *                                    ..room for 16 tests, 6 used
                                          1258 *
                          00004000  00000001 1259 LBFPRMO  EQU   STRTLABL+X'4000'    Long BFP rounding mode test results
                                          1260 *                                    ..Room for 16, 4 used.
                          00004500  00000001 1261 LBFPRMOF EQU   STRTLABL+X'4500'    Long BFP rounding mode FPCR results
                                          1262 *                                    ..Room for 16, 4 used.
                                          1263 *                                    ..next location starts at X'4800'
                                          1264 *
                          00005000  00000001 1265 XBFPNFOT EQU   STRTLABL+X'5000'    Integer ext'd non-finite BFP results
                                          1266 *                                    ..room for 64 tests, 64 used
                          00005800  00000001 1267 XBFPNFFL EQU   STRTLABL+X'5800'    FPCR flags and DXC from ext'd BFP
                                          1268 *                                    ..room for 64 tests, 64 used
                                          1269 *
                          00005C00  00000001 1270 XBFPOUT  EQU   STRTLABL+X'5C00'    Extended BFP finite results
                                          1271 *                                    ..room for 16 tests, 6 used
                          00005E00  00000001 1272 XBFPFLGS EQU   STRTLABL+X'5E00'    FPCR flags and DXC from ext'd BFP
                                          1273 *                                    ..room for 16 tests, 6 used
                                          1274 *
                          00006000  00000001 1275 XBFPRMO  EQU   STRTLABL+X'6000'    Ext'd BFP rounding mode test results
                                          1276 *                                    ..Room for 16, 4 used.
                          00006A00  00000001 1277 XBFPRMOF EQU   STRTLABL+X'6A00'    Ext'd BFP rounding mode FPCR results
                                          1278 *                                    ..Room for 16, 4 used.
                                          1279 *                                    ..next location starts at X'6D00'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   1281 ********************************************************************************
                                                   1282 *                       EXPECTED results
                                                   1283 ********************************************************************************
                                                   1284 *
00000AB0                      00000AB0  00007000   1285          ORG   STRTLABL+X'7000'   (past end of actual results)
                                                   1286 *
                              00007000  00000001   1287 SBFPNFOT_GOOD EQU *
00007000  C4C5C2D9 61C4C5C2                        1288  DC CL48'DEBR/DEB NF -inf/-inf'
00007030  7FC00000 FF800000                        1289  DC XL16'7FC00000FF8000007FC00000FF800000'
00007040  C4C5C2D9 61C4C5C2                        1290  DC CL48'DEBR/DEB NF -inf/-2'
00007070  7F800000 7F800000                        1291  DC XL16'7F8000007F8000007F8000007F800000'
00007080  C4C5C2D9 61C4C5C2                        1292  DC CL48'DEBR/DEB NF -inf/-0'
000070B0  7F800000 7F800000                        1293  DC XL16'7F8000007F8000007F8000007F800000'
000070C0  C4C5C2D9 61C4C5C2                        1294  DC CL48'DEBR/DEB NF -inf/+0'
000070F0  FF800000 FF800000                        1295  DC XL16'FF800000FF800000FF800000FF800000'
00007100  C4C5C2D9 61C4C5C2                        1296  DC CL48'DEBR/DEB NF -inf/+2'
00007130  FF800000 FF800000                        1297  DC XL16'FF800000FF800000FF800000FF800000'
00007140  C4C5C2D9 61C4C5C2                        1298  DC CL48'DEBR/DEB NF -inf/+inf'
00007170  7FC00000 FF800000                        1299  DC XL16'7FC00000FF8000007FC00000FF800000'
00007180  C4C5C2D9 61C4C5C2                        1300  DC CL48'DEBR/DEB NF -inf/-QNaN'
000071B0  FFCB0000 FFCB0000                        1301  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
000071C0  C4C5C2D9 61C4C5C2                        1302  DC CL48'DEBR/DEB NF -inf/+SNaN'
000071F0  7FCA0000 FF800000                        1303  DC XL16'7FCA0000FF8000007FCA0000FF800000'
00007200  C4C5C2D9 61C4C5C2                        1304  DC CL48'DEBR/DEB NF -2/-inf'
00007230  00000000 00000000                        1305  DC XL16'00000000000000000000000000000000'
00007240  C4C5C2D9 61C4C5C2                        1306  DC CL48'DEBR/DEB NF -2/-2'
00007270  3F800000 3F800000                        1307  DC XL16'3F8000003F8000003F8000003F800000'
00007280  C4C5C2D9 61C4C5C2                        1308  DC CL48'DEBR/DEB NF -2/-0'
000072B0  7F800000 C0000000                        1309  DC XL16'7F800000C00000007F800000C0000000'
000072C0  C4C5C2D9 61C4C5C2                        1310  DC CL48'DEBR/DEB NF -2/+0'
000072F0  FF800000 C0000000                        1311  DC XL16'FF800000C0000000FF800000C0000000'
00007300  C4C5C2D9 61C4C5C2                        1312  DC CL48'DEBR/DEB NF -2/+2'
00007330  BF800000 BF800000                        1313  DC XL16'BF800000BF800000BF800000BF800000'
00007340  C4C5C2D9 61C4C5C2                        1314  DC CL48'DEBR/DEB NF -2/+inf'
00007370  80000000 80000000                        1315  DC XL16'80000000800000008000000080000000'
00007380  C4C5C2D9 61C4C5C2                        1316  DC CL48'DEBR/DEB NF -2/-QNaN'
000073B0  FFCB0000 FFCB0000                        1317  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
000073C0  C4C5C2D9 61C4C5C2                        1318  DC CL48'DEBR/DEB NF -2/+SNaN'
000073F0  7FCA0000 C0000000                        1319  DC XL16'7FCA0000C00000007FCA0000C0000000'
00007400  C4C5C2D9 61C4C5C2                        1320  DC CL48'DEBR/DEB NF -0/-inf'
00007430  00000000 00000000                        1321  DC XL16'00000000000000000000000000000000'
00007440  C4C5C2D9 61C4C5C2                        1322  DC CL48'DEBR/DEB NF -0/-2'
00007470  00000000 00000000                        1323  DC XL16'00000000000000000000000000000000'
00007480  C4C5C2D9 61C4C5C2                        1324  DC CL48'DEBR/DEB NF -0/-0'
000074B0  7FC00000 80000000                        1325  DC XL16'7FC00000800000007FC0000080000000'
000074C0  C4C5C2D9 61C4C5C2                        1326  DC CL48'DEBR/DEB NF -0/+0'
000074F0  7FC00000 80000000                        1327  DC XL16'7FC00000800000007FC0000080000000'
00007500  C4C5C2D9 61C4C5C2                        1328  DC CL48'DEBR/DEB NF -0/+2'
00007530  80000000 80000000                        1329  DC XL16'80000000800000008000000080000000'
00007540  C4C5C2D9 61C4C5C2                        1330  DC CL48'DEBR/DEB NF -0/+inf'
00007570  80000000 80000000                        1331  DC XL16'80000000800000008000000080000000'
00007580  C4C5C2D9 61C4C5C2                        1332  DC CL48'DEBR/DEB NF -0/-QNaN'
000075B0  FFCB0000 FFCB0000                        1333  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
000075C0  C4C5C2D9 61C4C5C2                        1334  DC CL48'DEBR/DEB NF -0/+SNaN'
000075F0  7FCA0000 80000000                        1335  DC XL16'7FCA0000800000007FCA0000800000000'
00007600  C4C5C2D9 61C4C5C2                        1336  DC CL48'DEBR/DEB NF +0/-inf'
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00007630  80000000 80000000                         1337  DC XL16'80000000800000008000000080000000'
00007640  C4C5C2D9 61C4C5C2                         1338  DC CL48'DEBR/DEB NF +0/-2'
00007670  80000000 80000000                         1339  DC XL16'80000000800000008000000080000000'
00007680  C4C5C2D9 61C4C5C2                         1340  DC CL48'DEBR/DEB NF +0/-0'
000076B0  7FC00000 00000000                         1341  DC XL16'7FC00000000000007FC0000000000000'
000076C0  C4C5C2D9 61C4C5C2                         1342  DC CL48'DEBR/DEB NF +0/+0'
000076F0  7FC00000 00000000                         1343  DC XL16'7FC00000000000007FC0000000000000'
00007700  C4C5C2D9 61C4C5C2                         1344  DC CL48'DEBR/DEB NF +0/+2'
00007730  00000000 00000000                         1345  DC XL16'00000000000000000000000000000000'
00007740  C4C5C2D9 61C4C5C2                         1346  DC CL48'DEBR/DEB NF +0/+inf'
00007770  00000000 00000000                         1347  DC XL16'00000000000000000000000000000000'
00007780  C4C5C2D9 61C4C5C2                         1348  DC CL48'DEBR/DEB NF +0/-QNaN'
000077B0  FFCB0000 FFCB0000                         1349  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
000077C0  C4C5C2D9 61C4C5C2                         1350  DC CL48'DEBR/DEB NF +0/+SNaN'
000077F0  7FCA0000 00000000                         1351  DC XL16'7FCA0000000000007FCA000000000000'
00007800  C4C5C2D9 61C4C5C2                         1352  DC CL48'DEBR/DEB NF +2/-inf'
00007830  80000000 80000000                         1353  DC XL16'80000000800000008000000080000000'
00007840  C4C5C2D9 61C4C5C2                         1354  DC CL48'DEBR/DEB NF +2/-2'
00007870  BF800000 BF800000                         1355  DC XL16'BF800000BF800000BF800000BF800000'
00007880  C4C5C2D9 61C4C5C2                         1356  DC CL48'DEBR/DEB NF +2/-0'
000078B0  FF800000 40000000                         1357  DC XL16'FF800000400000007F80000040000000'
000078C0  C4C5C2D9 61C4C5C2                         1358  DC CL48'DEBR/DEB NF +2/+0'
000078F0  7F800000 40000000                         1359  DC XL16'7F800000400000007F80000040000000'
00007900  C4C5C2D9 61C4C5C2                         1360  DC CL48'DEBR/DEB NF +2/+2'
00007930  3F800000 3F800000                         1361  DC XL16'3F8000003F8000003F8000003F800000'
00007940  C4C5C2D9 61C4C5C2                         1362  DC CL48'DEBR/DEB NF +2/+inf'
00007970  00000000 00000000                         1363  DC XL16'00000000000000000000000000000000'
00007980  C4C5C2D9 61C4C5C2                         1364  DC CL48'DEBR/DEB NF +2/-QNaN'
000079B0  FFCB0000 FFCB0000                         1365  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
000079C0  C4C5C2D9 61C4C5C2                         1366  DC CL48'DEBR/DEB NF +2/+SNaN'
000079F0  7FCA0000 40000000                         1367  DC XL16'7FCA0000400000007FCA000040000000'
00007A00  C4C5C2D9 61C4C5C2                         1368  DC CL48'DEBR/DEB NF +inf/-inf'
00007A30  7FC00000 7F800000                         1369  DC XL16'7FC000007F8000007FC000007F800000'
00007A40  C4C5C2D9 61C4C5C2                         1370  DC CL48'DEBR/DEB NF +inf/-2'
00007A70  FF800000 FF800000                         1371  DC XL16'FF800000FF800000FF800000FF800000'
00007A80  C4C5C2D9 61C4C5C2                         1372  DC CL48'DEBR/DEB NF +inf/-0'
00007AB0  FF800000 FF800000                         1373  DC XL16'FF800000FF800000FF800000FF800000'
00007AC0  C4C5C2D9 61C4C5C2                         1374  DC CL48'DEBR/DEB NF +inf/+0'
00007AF0  7F800000 7F800000                         1375  DC XL16'7F8000007F8000007F8000007F800000'
00007B00  C4C5C2D9 61C4C5C2                         1376  DC CL48'DEBR/DEB NF +inf/+2'
00007B30  7F800000 7F800000                         1377  DC XL16'7F8000007F8000007F8000007F800000'
00007B40  C4C5C2D9 61C4C5C2                         1378  DC CL48'DEBR/DEB NF +inf/+inf'
00007B70  7FC00000 7F800000                         1379  DC XL16'7FC000007F8000007FC000007F800000'
00007B80  C4C5C2D9 61C4C5C2                         1380  DC CL48'DEBR/DEB NF +inf/-QNaN'
00007BB0  FFCB0000 FFCB0000                         1381  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
00007BC0  C4C5C2D9 61C4C5C2                         1382  DC CL48'DEBR/DEB NF +inf/+SNaN'
00007BF0  7FCA0000 7F800000                         1383  DC XL16'7FCA00007F8000007FCA00007F800000'
00007C00  C4C5C2D9 61C4C5C2                         1384  DC CL48'DEBR/DEB NF -QNaN/-inf'
00007C30  FFCB0000 FFCB0000                         1385  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
00007C40  C4C5C2D9 61C4C5C2                         1386  DC CL48'DEBR/DEB NF -QNaN/-2'
00007C70  FFCB0000 FFCB0000                         1387  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
00007C80  C4C5C2D9 61C4C5C2                         1388  DC CL48'DEBR/DEB NF -QNaN/-0'
00007CB0  FFCB0000 FFCB0000                         1389  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
00007CC0  C4C5C2D9 61C4C5C2                         1390  DC CL48'DEBR/DEB NF -QNaN/+0'
00007CF0  FFCB0000 FFCB0000                         1391  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
00007D00  C4C5C2D9 61C4C5C2                         1392  DC CL48'DEBR/DEB NF -QNaN/+2'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

00007D30  FFCB0000 FFCB0000                         1393  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
00007D40  C4C5C2D9 61C4C5C2                         1394  DC CL48'DEBR/DEB NF -QNaN/+inf'
00007D70  FFCB0000 FFCB0000                         1395  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
00007D80  C4C5C2D9 61C4C5C2                         1396  DC CL48'DEBR/DEB NF -QNaN/-QNaN'
00007DB0  FFCB0000 FFCB0000                         1397  DC XL16'FFCB0000FFCB0000FFCB0000FFCB0000'
00007DC0  C4C5C2D9 61C4C5C2                         1398  DC CL48'DEBR/DEB NF -QNaN/+SNaN'
00007DF0  7FCA0000 FFCB0000                         1399  DC XL16'7FCA0000FFCB00007FCA0000FFCB0000'
00007E00  C4C5C2D9 61C4C5C2                         1400  DC CL48'DEBR/DEB NF +SNaN/-inf'
00007E30  7FCA0000 7F8A0000                         1401  DC XL16'7FCA00007F8A00007FCA00007F8A0000'
00007E40  C4C5C2D9 61C4C5C2                         1402  DC CL48'DEBR/DEB NF +SNaN/-2'
00007E70  7FCA0000 7F8A0000                         1403  DC XL16'7FCA00007F8A00007FCA00007F8A0000'
00007E80  C4C5C2D9 61C4C5C2                         1404  DC CL48'DEBR/DEB NF +SNaN/-0'
00007EB0  7FCA0000 7F8A0000                         1405  DC XL16'7FCA00007F8A00007FCA00007F8A0000'
00007EC0  C4C5C2D9 61C4C5C2                         1406  DC CL48'DEBR/DEB NF +SNaN/+0'
00007EF0  7FCA0000 7F8A0000                         1407  DC XL16'7FCA00007F8A00007FCA00007F8A0000'
00007F00  C4C5C2D9 61C4C5C2                         1408  DC CL48'DEBR/DEB NF +SNaN/+2'
00007F30  7FCA0000 7F8A0000                         1409  DC XL16'7FCA00007F8A00007FCA00007F8A0000'
00007F40  C4C5C2D9 61C4C5C2                         1410  DC CL48'DEBR/DEB NF +SNaN/+inf'
00007F70  7FCA0000 7F8A0000                         1411  DC XL16'7FCA00007F8A00007FCA00007F8A0000'
00007F80  C4C5C2D9 61C4C5C2                         1412  DC CL48'DEBR/DEB NF +SNaN/-QNaN'
00007FB0  7FCA0000 7F8A0000                         1413  DC XL16'7FCA00007F8A00007FCA00007F8A0000'
00007FC0  C4C5C2D9 61C4C5C2                         1414  DC CL48'DEBR/DEB NF +SNaN/+SNaN'
00007FF0  7FCA0000 7F8A0000                         1415  DC XL16'7FCA00007F8A00007FCA00007F8A0000'
                            00000040  00000001     1416 SBFPNFOT_NUM EQU (*-SBFPNFOT_GOOD)/64
                                                    1417 *
                                                    1418 *
                            00008000  00000001     1419 SBFPNFFL_GOOD EQU *
00008000  C4C5C2D9 61C4C5C2                         1420  DC CL48'DEBR/DEB NF -inf/-inf FPCR'
00008030  00800000 F8008000                         1421  DC XL16'00800000F8008000008000000F8008000'
00008040  C4C5C2D9 61C4C5C2                         1422  DC CL48'DEBR/DEB NF -inf/-2 FPCR'
00008070  00000000 F8000000                         1423  DC XL16'00000000F8000000000000000F8000000'
00008080  C4C5C2D9 61C4C5C2                         1424  DC CL48'DEBR/DEB NF -inf/-0 FPCR'
000080B0  00000000 F8000000                         1425  DC XL16'00000000F8000000000000000F8000000'
000080C0  C4C5C2D9 61C4C5C2                         1426  DC CL48'DEBR/DEB NF -inf/+0 FPCR'
000080F0  00000000 F8000000                         1427  DC XL16'00000000F8000000000000000F8000000'
00008100  C4C5C2D9 61C4C5C2                         1428  DC CL48'DEBR/DEB NF -inf/+2 FPCR'
00008130  00000000 F8000000                         1429  DC XL16'00000000F8000000000000000F8000000'
00008140  C4C5C2D9 61C4C5C2                         1430  DC CL48'DEBR/DEB NF -inf/+inf FPCR'
00008170  00800000 F8008000                         1431  DC XL16'00800000F8008000008000000F8008000'
00008180  C4C5C2D9 61C4C5C2                         1432  DC CL48'DEBR/DEB NF -inf/-QNaN FPCR'
000081B0  00000000 F8000000                         1433  DC XL16'00000000F8000000000000000F8000000'
000081C0  C4C5C2D9 61C4C5C2                         1434  DC CL48'DEBR/DEB NF -inf/+SNaN FPCR'
000081F0  00800000 F8008000                         1435  DC XL16'00800000F8008000008000000F8008000'
00008200  C4C5C2D9 61C4C5C2                         1436  DC CL48'DEBR/DEB NF -2/-inf FPCR'
00008230  00000000 F8000000                         1437  DC XL16'00000000F8000000000000000F8000000'
00008240  C4C5C2D9 61C4C5C2                         1438  DC CL48'DEBR/DEB NF -2/-2 FPCR'
00008270  00000000 F8000000                         1439  DC XL16'00000000F8000000000000000F8000000'
00008280  C4C5C2D9 61C4C5C2                         1440  DC CL48'DEBR/DEB NF -2/-0 FPCR'
000082B0  00400000 F8004000                         1441  DC XL16'00400000F8004000004000000F8004000'
000082C0  C4C5C2D9 61C4C5C2                         1442  DC CL48'DEBR/DEB NF -2/+0 FPCR'
000082F0  00400000 F8004000                         1443  DC XL16'00400000F8004000004000000F8004000'
00008300  C4C5C2D9 61C4C5C2                         1444  DC CL48'DEBR/DEB NF -2/+2 FPCR'
00008330  00000000 F8000000                         1445  DC XL16'00000000F8000000000000000F8000000'
00008340  C4C5C2D9 61C4C5C2                         1446  DC CL48'DEBR/DEB NF -2/+inf FPCR'
00008370  00000000 F8000000                         1447  DC XL16'00000000F8000000000000000F8000000'
00008380  C4C5C2D9 61C4C5C2                         1448  DC CL48'DEBR/DEB NF -2/-QNaN FPCR'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000083B0  00000000 F8000000                       1449  DC XL16'00000000F800000000000000F8000000'
000083C0  C4C5C2D9 61C4C5C2                       1450  DC CL48'DEBR/DEB NF -2/+SNaN FPCR'
000083F0  00800000 F8008000                       1451  DC XL16'00800000F800800000800000F8008000'
00008400  C4C5C2D9 61C4C5C2                       1452  DC CL48'DEBR/DEB NF -0/-inf FPCR'
00008430  00000000 F8000000                       1453  DC XL16'00000000F800000000000000F8000000'
00008440  C4C5C2D9 61C4C5C2                       1454  DC CL48'DEBR/DEB NF -0/-2 FPCR'
00008470  00000000 F8000000                       1455  DC XL16'00000000F800000000000000F8000000'
00008480  C4C5C2D9 61C4C5C2                       1456  DC CL48'DEBR/DEB NF -0/-0 FPCR'
000084B0  00800000 F8008000                       1457  DC XL16'00800000F800800000800000F8008000'
000084C0  C4C5C2D9 61C4C5C2                       1458  DC CL48'DEBR/DEB NF -0/+0 FPCR'
000084F0  00800000 F8008000                       1459  DC XL16'00800000F800800000800000F8008000'
00008500  C4C5C2D9 61C4C5C2                       1460  DC CL48'DEBR/DEB NF -0/+2 FPCR'
00008530  00000000 F8000000                       1461  DC XL16'00000000F800000000000000F8000000'
00008540  C4C5C2D9 61C4C5C2                       1462  DC CL48'DEBR/DEB NF -0/+inf FPCR'
00008570  00000000 F8000000                       1463  DC XL16'00000000F800000000000000F8000000'
00008580  C4C5C2D9 61C4C5C2                       1464  DC CL48'DEBR/DEB NF -0/-QNaN FPCR'
000085B0  00000000 F8000000                       1465  DC XL16'00000000F800000000000000F8000000'
000085C0  C4C5C2D9 61C4C5C2                       1466  DC CL48'DEBR/DEB NF -0/+SNaN FPCR'
000085F0  00800000 F8008000                       1467  DC XL16'00800000F800800000800000F8008000'
00008600  C4C5C2D9 61C4C5C2                       1468  DC CL48'DEBR/DEB NF +0/-inf FPCR'
00008630  00000000 F8000000                       1469  DC XL16'00000000F800000000000000F8000000'
00008640  C4C5C2D9 61C4C5C2                       1470  DC CL48'DEBR/DEB NF +0/-2 FPCR'
00008670  00000000 F8000000                       1471  DC XL16'00000000F800000000000000F8000000'
00008680  C4C5C2D9 61C4C5C2                       1472  DC CL48'DEBR/DEB NF +0/-0 FPCR'
000086B0  00800000 F8008000                       1473  DC XL16'00800000F800800000800000F8008000'
000086C0  C4C5C2D9 61C4C5C2                       1474  DC CL48'DEBR/DEB NF +0/+0 FPCR'
000086F0  00800000 F8008000                       1475  DC XL16'00800000F800800000800000F8008000'
00008700  C4C5C2D9 61C4C5C2                       1476  DC CL48'DEBR/DEB NF +0/+2 FPCR'
00008730  00000000 F8000000                       1477  DC XL16'00000000F800000000000000F8000000'
00008740  C4C5C2D9 61C4C5C2                       1478  DC CL48'DEBR/DEB NF +0/+inf FPCR'
00008770  00000000 F8000000                       1479  DC XL16'00000000F800000000000000F8000000'
00008780  C4C5C2D9 61C4C5C2                       1480  DC CL48'DEBR/DEB NF +0/-QNaN FPCR'
000087B0  00000000 F8000000                       1481  DC XL16'00000000F800000000000000F8000000'
000087C0  C4C5C2D9 61C4C5C2                       1482  DC CL48'DEBR/DEB NF +0/+SNaN FPCR'
000087F0  00800000 F8008000                       1483  DC XL16'00800000F800800000800000F8008000'
00008800  C4C5C2D9 61C4C5C2                       1484  DC CL48'DEBR/DEB NF +2/-inf FPCR'
00008830  00000000 F8000000                       1485  DC XL16'00000000F800000000000000F8000000'
00008840  C4C5C2D9 61C4C5C2                       1486  DC CL48'DEBR/DEB NF +2/-2 FPCR'
00008870  00000000 F8000000                       1487  DC XL16'00000000F800000000000000F8000000'
00008880  C4C5C2D9 61C4C5C2                       1488  DC CL48'DEBR/DEB NF +2/-0 FPCR'
000088B0  00400000 F8004000                       1489  DC XL16'00400000F800400000400000F8004000'
000088C0  C4C5C2D9 61C4C5C2                       1490  DC CL48'DEBR/DEB NF +2/+0 FPCR'
000088F0  00400000 F8004000                       1491  DC XL16'00400000F800400000400000F8004000'
00008900  C4C5C2D9 61C4C5C2                       1492  DC CL48'DEBR/DEB NF +2/+2 FPCR'
00008930  00000000 F8000000                       1493  DC XL16'00000000F800000000000000F8000000'
00008940  C4C5C2D9 61C4C5C2                       1494  DC CL48'DEBR/DEB NF +2/+inf FPCR'
00008970  00000000 F8000000                       1495  DC XL16'00000000F800000000000000F8000000'
00008980  C4C5C2D9 61C4C5C2                       1496  DC CL48'DEBR/DEB NF +2/-QNaN FPCR'
000089B0  00000000 F8000000                       1497  DC XL16'00000000F800000000000000F8000000'
000089C0  C4C5C2D9 61C4C5C2                       1498  DC CL48'DEBR/DEB NF +2/+SNaN FPCR'
000089F0  00800000 F8008000                       1499  DC XL16'00800000F800800000800000F8008000'
00008A00  C4C5C2D9 61C4C5C2                       1500  DC CL48'DEBR/DEB NF +inf/-inf FPCR'
00008A30  00800000 F8008000                       1501  DC XL16'00800000F800800000800000F8008000'
00008A40  C4C5C2D9 61C4C5C2                       1502  DC CL48'DEBR/DEB NF +inf/-2 FPCR'
00008A70  00000000 F8000000                       1503  DC XL16'00000000F800000000000000F8000000'
00008A80  C4C5C2D9 61C4C5C2                       1504  DC CL48'DEBR/DEB NF +inf/-0 FPCR'
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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00008AB0  00000000 F8000000                         1505  DC XL16'00000000F800000000000000F8000000'
00008AC0  C4C5C2D9 61C4C5C2                         1506  DC CL48'DEBR/DEB NF +inf/+0 FPCR'
00008AF0  00000000 F8000000                         1507  DC XL16'00000000F800000000000000F8000000'
00008B00  C4C5C2D9 61C4C5C2                         1508  DC CL48'DEBR/DEB NF +inf/+2 FPCR'
00008B30  00000000 F8000000                         1509  DC XL16'00000000F800000000000000F8000000'
00008B40  C4C5C2D9 61C4C5C2                         1510  DC CL48'DEBR/DEB NF +inf/+inf FPCR'
00008B70  00800000 F8008000                         1511  DC XL16'00800000F800800000800000F8008000'
00008B80  C4C5C2D9 61C4C5C2                         1512  DC CL48'DEBR/DEB NF +inf/-QNaN FPCR'
00008BB0  00000000 F8000000                         1513  DC XL16'00000000F800000000000000F8000000'
00008BC0  C4C5C2D9 61C4C5C2                         1514  DC CL48'DEBR/DEB NF +inf/+SNaN FPCR'
00008BF0  00800000 F8008000                         1515  DC XL16'00800000F800800000800000F8008000'
00008C00  C4C5C2D9 61C4C5C2                         1516  DC CL48'DEBR/DEB NF -QNaN/-inf FPCR'
00008C30  00000000 F8000000                         1517  DC XL16'00000000F800000000000000F8000000'
00008C40  C4C5C2D9 61C4C5C2                         1518  DC CL48'DEBR/DEB NF -QNaN/-2 FPCR'
00008C70  00000000 F8000000                         1519  DC XL16'00000000F800000000000000F8000000'
00008C80  C4C5C2D9 61C4C5C2                         1520  DC CL48'DEBR/DEB NF -QNaN/-0 FPCR'
00008CB0  00000000 F8000000                         1521  DC XL16'00000000F800000000000000F8000000'
00008CC0  C4C5C2D9 61C4C5C2                         1522  DC CL48'DEBR/DEB NF -QNaN/+0 FPCR'
00008CF0  00000000 F8000000                         1523  DC XL16'00000000F800000000000000F8000000'
00008D00  C4C5C2D9 61C4C5C2                         1524  DC CL48'DEBR/DEB NF -QNaN/+2 FPCR'
00008D30  00000000 F8000000                         1525  DC XL16'00000000F800000000000000F8000000'
00008D40  C4C5C2D9 61C4C5C2                         1526  DC CL48'DEBR/DEB NF -QNaN/+inf FPCR'
00008D70  00000000 F8000000                         1527  DC XL16'00000000F800000000000000F8000000'
00008D80  C4C5C2D9 61C4C5C2                         1528  DC CL48'DEBR/DEB NF -QNaN/-QNaN FPCR'
00008DB0  00000000 F8000000                         1529  DC XL16'00000000F800000000000000F8000000'
00008DC0  C4C5C2D9 61C4C5C2                         1530  DC CL48'DEBR/DEB NF -QNaN/+SNaN FPCR'
00008DF0  00800000 F8008000                         1531  DC XL16'00800000F800800000800000F8008000'
00008E00  C4C5C2D9 61C4C5C2                         1532  DC CL48'DEBR/DEB NF +SNaN/-inf FPCR'
00008E30  00800000 F8008000                         1533  DC XL16'00800000F800800000800000F8008000'
00008E40  C4C5C2D9 61C4C5C2                         1534  DC CL48'DEBR/DEB NF +SNaN/-2 FPCR'
00008E70  00800000 F8008000                         1535  DC XL16'00800000F800800000800000F8008000'
00008E80  C4C5C2D9 61C4C5C2                         1536  DC CL48'DEBR/DEB NF +SNaN/-0 FPCR'
00008EB0  00800000 F8008000                         1537  DC XL16'00800000F800800000800000F8008000'
00008EC0  C4C5C2D9 61C4C5C2                         1538  DC CL48'DEBR/DEB NF +SNaN/+0 FPCR'
00008EF0  00800000 F8008000                         1539  DC XL16'00800000F800800000800000F8008000'
00008F00  C4C5C2D9 61C4C5C2                         1540  DC CL48'DEBR/DEB NF +SNaN/+2 FPCR'
00008F30  00800000 F8008000                         1541  DC XL16'00800000F800800000800000F8008000'
00008F40  C4C5C2D9 61C4C5C2                         1542  DC CL48'DEBR/DEB NF +SNaN/+inf FPCR'
00008F70  00800000 F8008000                         1543  DC XL16'00800000F800800000800000F8008000'
00008F80  C4C5C2D9 61C4C5C2                         1544  DC CL48'DEBR/DEB NF +SNaN/-QNaN FPCR'
00008FB0  00800000 F8008000                         1545  DC XL16'00800000F800800000800000F8008000'
00008FC0  C4C5C2D9 61C4C5C2                         1546  DC CL48'DEBR/DEB NF +SNaN/+SNaN FPCR'
00008FF0  00800000 F8008000                         1547  DC XL16'00800000F800800000800000F8008000'
                             00000040  00000001     1548 SBFPNFFL_NUM EQU (*-SBFPNFFL_GOOD)/64
                                                    1549 *
                                                    1550 *
                             00009000  00000001     1551 SBFPOUT_GOOD EQU *
00009000  C4C5C2D9 61C4C5C2                         1552  DC CL48'DEBR/DEB max/min'
00009030  7F800000 69FFFFFF                         1553  DC XL16'7F80000069FFFFFF7F80000069FFFFFF'
00009040  C4C5C2D9 61C4C5C2                         1554  DC CL48'DEBR/DEB min/2.0'
00009070  00400000 60000000                         1555  DC XL16'00400000600000000040000060000000'
00009080  C4C5C2D9 61C4C5C2                         1556  DC CL48'DEBR/DEB 1.0/10.0'
000090B0  3DCCCCCD 3DCCCCCD                         1557  DC XL16'3DCCCCCD3DCCCCCD3DCCCCCD3DCCCCCD'
000090C0  C4C5C2D9 61C4C5C2                         1558  DC CL48'DEBR/DEB 7.0/10.0'
000090F0  3E666666 3E666666                         1559  DC XL16'3E6666663E6666663E6666663E666666'
00009100  C4C5C2D9 61C4C5C2                         1560  DC CL48'DEBR/DEB 1.0/-10.0'
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  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

00009130  BDCCCCCD BDCCCCCD                        1561  DC XL16'BDCCCCCDBDCCCCCDBDCCCCCDBDCCCCCD'
00009140  C4C5C2D9 61C4C5C2                        1562  DC CL48'DEBR/DEB 7.0/-10.0'
00009170  BE666666 BE666666                        1563  DC XL16'BE666666BE666666BE666666BE666666'
                             00000006  00000001  1564 SBFPOUT_NUM EQU (*-SBFPOUT_GOOD)/64
                                                 1565 *
                                                 1566 *
                             00009180  00000001  1567 SBFPFLGS_GOOD EQU *
00009180  C4C5C2D9 61C4C5C2                        1568  DC CL48'DEBR/DEB max/min FPCR'
000091B0  00280000 F8002000                        1569  DC XL16'00280000F8002000028000F8002000'
000091C0  C4C5C2D9 61C4C5C2                        1570  DC CL48'DEBR/DEB min/2.0 FPCR'
000091F0  00000000 F8001000                        1571  DC XL16'00000000F8001000000000F8001000'
00009200  C4C5C2D9 61C4C5C2                        1572  DC CL48'DEBR/DEB 1.0/10.0 FPCR'
00009230  00080000 F8000C00                        1573  DC XL16'00080000F8000C0000080000F8000C00'
00009240  C4C5C2D9 61C4C5C2                        1574  DC CL48'DEBR/DEB 7.0/10.0 FPCR'
00009270  00080000 F8000800                        1575  DC XL16'00080000F8000800000800000F8000800'
00009280  C4C5C2D9 61C4C5C2                        1576  DC CL48'DEBR/DEB 1.0/-10.0 FPCR'
000092B0  00080000 F8000C00                        1577  DC XL16'00080000F8000C0000080000F8000C00'
000092C0  C4C5C2D9 61C4C5C2                        1578  DC CL48'DEBR/DEB 7.0/-10.0 FPCR'
000092F0  00080000 F8000800                        1579  DC XL16'00080000F8000800000800000F8000800'
                             00000006  00000001  1580 SBFPFLGS_NUM EQU (*-SBFPFLGS_GOOD)/64
                                                 1581 *
                                                 1582 *
                             00009300  00000001  1583 SBFPRMO_GOOD EQU *
00009300  C4C5C2D9 61C4C5C2                        1584  DC CL48'DEBR/DEB RM RNTE,RZ 1/10'
00009330  3DCCCCCD 3DCCCCCD                        1585  DC XL16'3DCCCCCD3DCCCCCD3DCCCCCC3DCCCCCC'
00009340  C4C5C2D9 61C4C5C2                        1586  DC CL48'DEBR/DEB RM RP,RM 1/10'
00009370  3DCCCCCD 3DCCCCCD                        1587  DC XL16'3DCCCCCD3DCCCCCD3DCCCCCC3DCCCCCC'
00009380  C4C5C2D9 61C4C5C2                        1588  DC CL48'DEBR/DEB RM RFS 1/10'
000093B0  3DCCCCCD 3DCCCCCD                        1589  DC XL16'3DCCCCCD3DCCCCCD0000000000000000'
000093C0  C4C5C2D9 61C4C5C2                        1590  DC CL48'DEBR/DEB RM RNTE,RZ 7/10'
000093F0  3E666666 3E666666                        1591  DC XL16'3E6666663E6666663E6666663E666666'
00009400  C4C5C2D9 61C4C5C2                        1592  DC CL48'DEBR/DEB RM RP,RM 7/10'
00009430  3E666667 3E666667                        1593  DC XL16'3E6666673E6666673E6666663E666666'
00009440  C4C5C2D9 61C4C5C2                        1594  DC CL48'DEBR/DEB RM RFS 7/10'
00009470  3E666667 3E666667                        1595  DC XL16'3E6666673E6666670000000000000000'
00009480  C4C5C2D9 61C4C5C2                        1596  DC CL48'DEBR/DEB RM RNTE,RZ 1/-10'
000094B0  BDCCCCCD BDCCCCCD                        1597  DC XL16'BDCCCCCDBDCCCCCDBDCCCCCCBDCCCCCC'
000094C0  C4C5C2D9 61C4C5C2                        1598  DC CL48'DEBR/DEB RM RP,RM 1/-10'
000094F0  BDCCCCCC BDCCCCCC                        1599  DC XL16'BDCCCCCCBDCCCCCCBDCCCCCDBDCCCCCD'
00009500  C4C5C2D9 61C4C5C2                        1600  DC CL48'DEBR/DEB RM RFS 1/-10'
00009530  BDCCCCCD BDCCCCCD                        1601  DC XL16'BDCCCCCDBDCCCCCD0000000000000000'
00009540  C4C5C2D9 61C4C5C2                        1602  DC CL48'DEBR/DEB RM RNTE,RZ 7/-10'
00009570  BE666666 BE666666                        1603  DC XL16'BE666666BE666666BE666666BE666666'
00009580  C4C5C2D9 61C4C5C2                        1604  DC CL48'DEBR/DEB RM RP,RM 7/-10'
000095B0  BE666666 BE666666                        1605  DC XL16'BE666666BE666666BE666667BE666667'
000095C0  C4C5C2D9 61C4C5C2                        1606  DC CL48'DEBR/DEB RM RFS 7/-10'
000095F0  BE666667 BE666667                        1607  DC XL16'BE666667BE6666670000000000000000'
                             0000000C  00000001  1608 SBFPRMO_NUM EQU (*-SBFPRMO_GOOD)/64
                                                 1609 *
                                                 1610 *
                             00009600  00000001  1611 SBFPRMOF_GOOD EQU *
00009600  C4C5C2D9 61C4C5C2                        1612  DC CL48'DEBR/DEB RM RNTE,RZ 1/10 FPCR'
00009630  00080000 00080000                        1613  DC XL16'00080000000800000008000100080001'
00009640  C4C5C2D9 61C4C5C2                        1614  DC CL48'DEBR/DEB RM RP,RM 1/10 FPCR'
00009670  00080002 00080002                        1615  DC XL16'00080002000800020008000300080003'
00009680  C4C5C2D9 61C4C5C2                        1616  DC CL48'DEBR/DEB RM RFS 1/10 FPCR'
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  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

000096B0  00080007 00080007                         1617  DC XL16'00080007000800070000000000000000'
000096C0  C4C5C2D9 61C4C5C2                         1618  DC CL48'DEBR/DEB RM RNTE,RZ 7/10 FPCR'
000096F0  00080000 00080000                         1619  DC XL16'00080000000800000008000100080001'
00009700  C4C5C2D9 61C4C5C2                         1620  DC CL48'DEBR/DEB RM RP,RM 7/10 FPCR'
00009730  00080002 00080002                         1621  DC XL16'00080002000800020008000300080003'
00009740  C4C5C2D9 61C4C5C2                         1622  DC CL48'DEBR/DEB RM RFS 7/10 FPCR'
00009770  00080007 00080007                         1623  DC XL16'00080007000800070000000000000000'
00009780  C4C5C2D9 61C4C5C2                         1624  DC CL48'DEBR/DEB RM RNTE,RZ 1/-10 FPCR'
000097B0  00080000 00080000                         1625  DC XL16'00080000000800000008000100080001'
000097C0  C4C5C2D9 61C4C5C2                         1626  DC CL48'DEBR/DEB RM RP,RM 1/-10 FPCR'
000097F0  00080002 00080002                         1627  DC XL16'00080002000800020008000300080003'
00009800  C4C5C2D9 61C4C5C2                         1628  DC CL48'DEBR/DEB RM RFS 1/-10 FPCR'
00009830  00080007 00080007                         1629  DC XL16'00080007000800070000000000000000'
00009840  C4C5C2D9 61C4C5C2                         1630  DC CL48'DEBR/DEB RM RNTE,RZ 7/-10 FPCR'
00009870  00080000 00080000                         1631  DC XL16'00080000000800000008000100080001'
00009880  C4C5C2D9 61C4C5C2                         1632  DC CL48'DEBR/DEB RM RP,RM 7/-10 FPCR'
000098B0  00080002 00080002                         1633  DC XL16'00080002000800020008000300080003'
000098C0  C4C5C2D9 61C4C5C2                         1634  DC CL48'DEBR/DEB RM RFS 7/-10 FPCR'
000098F0  00080007 00080007                         1635  DC XL16'00080007000800070000000000000000'
                            0000000C  00000001      1636 SBFPRMOF_NUM EQU (*-SBFPRMOF_GOOD)/64
                                                    1637 *
                                                    1638 *
                            00009900  00000001      1639 LBFPNFOT_GOOD EQU *
00009900  C4C4C2D9 40D5C640                         1640  DC CL48'DDBR NF -inf/-inf'
00009930  7FF80000 00000000                         1641  DC XL16'7FF8000000000000FFF0000000000000'
00009940  C4C4C240 40D5C640                         1642  DC CL48'DDB  NF -inf/-inf'
00009970  7FF80000 00000000                         1643  DC XL16'7FF8000000000000FFF0000000000000'
00009980  C4C4C2D9 40D5C640                         1644  DC CL48'DDBR NF -inf/-2'
000099B0  7FF00000 00000000                         1645  DC XL16'7FF00000000000007FF0000000000000'
000099C0  C4C4C240 40D5C640                         1646  DC CL48'DDB  NF -inf/-2'
000099F0  7FF00000 00000000                         1647  DC XL16'7FF00000000000007FF0000000000000'
00009A00  C4C4C2D9 40D5C640                         1648  DC CL48'DDBR NF -inf/-0'
00009A30  7FF00000 00000000                         1649  DC XL16'7FF00000000000007FF0000000000000'
00009A40  C4C4C240 40D5C640                         1650  DC CL48'DDB  NF -inf/-0'
00009A70  7FF00000 00000000                         1651  DC XL16'7FF00000000000007FF0000000000000'
00009A80  C4C4C2D9 40D5C640                         1652  DC CL48'DDBR NF -inf/+0'
00009AB0  FFF00000 00000000                         1653  DC XL16'FFF00000000000000FFF0000000000000'
00009AC0  C4C4C240 40D5C640                         1654  DC CL48'DDB  NF -inf/+0'
00009AF0  FFF00000 00000000                         1655  DC XL16'FFF00000000000000FFF0000000000000'
00009B00  C4C4C2D9 40D5C640                         1656  DC CL48'DDBR NF -inf/+2'
00009B30  FFF00000 00000000                         1657  DC XL16'FFF00000000000000FFF0000000000000'
00009B40  C4C4C240 40D5C640                         1658  DC CL48'DDB  NF -inf/+2'
00009B70  FFF00000 00000000                         1659  DC XL16'FFF00000000000000FFF0000000000000'
00009B80  C4C4C2D9 40D5C640                         1660  DC CL48'DDBR NF -inf/+inf'
00009BB0  7FF80000 00000000                         1661  DC XL16'7FF8000000000000FFF0000000000000'
00009BC0  C4C4C240 40D5C640                         1662  DC CL48'DDB  NF -inf/+inf'
00009BF0  7FF80000 00000000                         1663  DC XL16'7FF8000000000000FFF0000000000000'
00009C00  C4C4C2D9 40D5C640                         1664  DC CL48'DDBR NF -inf/-QNaN'
00009C30  FFF8B000 00000000                         1665  DC XL16'FFF8B00000000000FFF8B00000000000'
00009C40  C4C4C240 40D5C640                         1666  DC CL48'DDB  NF -inf/-QNaN'
00009C70  FFF8B000 00000000                         1667  DC XL16'FFF8B00000000000FFF8B00000000000'
00009C80  C4C4C2D9 40D5C640                         1668  DC CL48'DDBR NF -inf/+SNaN'
00009CB0  7FF8A000 00000000                         1669  DC XL16'7FF8A00000000000FFF0000000000000'
00009CC0  C4C4C240 40D5C640                         1670  DC CL48'DDB  NF -inf/+SNaN'
00009CF0  7FF8A000 00000000                         1671  DC XL16'7FF8A00000000000FFF0000000000000'
00009D00  C4C4C2D9 40D5C640                         1672  DC CL48'DDBR NF -2/-inf'
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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00009D30  00000000 00000000                       1673  DC XL16'00000000000000000000000000000000'
00009D40  C4C4C240 40D5C640                       1674  DC CL48'DDB  NF -2/-inf'
00009D70  00000000 00000000                       1675  DC XL16'00000000000000000000000000000000'
00009D80  C4C4C2D9 40D5C640                       1676  DC CL48'DDBR NF -2/-2'
00009DB0  3FF00000 00000000                       1677  DC XL16'3FF00000000000003FF0000000000000'
00009DC0  C4C4C240 40D5C640                       1678  DC CL48'DDB  NF -2/-2'
00009DF0  3FF00000 00000000                       1679  DC XL16'3FF00000000000003FF0000000000000'
00009E00  C4C4C2D9 40D5C640                       1680  DC CL48'DDBR NF -2/-0'
00009E30  7FF00000 00000000                       1681  DC XL16'7FF000000000000C000000000000000'
00009E40  C4C4C240 40D5C640                       1682  DC CL48'DDB  NF -2/-0'
00009E70  7FF00000 00000000                       1683  DC XL16'7FF000000000000C000000000000000'
00009E80  C4C4C2D9 40D5C640                       1684  DC CL48'DDBR NF -2/+0'
00009EB0  FFF00000 00000000                       1685  DC XL16'FFF000000000000C000000000000000'
00009EC0  C4C4C240 40D5C640                       1686  DC CL48'DDB  NF -2/+0'
00009EF0  FFF00000 00000000                       1687  DC XL16'FFF000000000000C000000000000000'
00009F00  C4C4C2D9 40D5C640                       1688  DC CL48'DDBR NF -2/+2'
00009F30  BFF00000 00000000                       1689  DC XL16'BFF0000000000000BFF0000000000000'
00009F40  C4C4C240 40D5C640                       1690  DC CL48'DDB  NF -2/+2'
00009F70  BFF00000 00000000                       1691  DC XL16'BFF0000000000000BFF0000000000000'
00009F80  C4C4C2D9 40D5C640                       1692  DC CL48'DDBR NF -2/+inf'
00009FB0  80000000 00000000                       1693  DC XL16'80000000000000008000000000000000'
00009FC0  C4C4C240 40D5C640                       1694  DC CL48'DDB  NF -2/+inf'
00009FF0  80000000 00000000                       1695  DC XL16'80000000000000008000000000000000'
0000A000  C4C4C2D9 40D5C640                       1696  DC CL48'DDBR NF -2/-QNaN'
0000A030  FFF8B000 00000000                       1697  DC XL16'FFF8B00000000000FFF8B00000000000'
0000A040  C4C4C240 40D5C640                       1698  DC CL48'DDB  NF -2/-QNaN'
0000A070  FFF8B000 00000000                       1699  DC XL16'FFF8B00000000000FFF8B00000000000'
0000A080  C4C4C2D9 40D5C640                       1700  DC CL48'DDBR NF -2/+SNaN'
0000A0B0  7FF8A000 00000000                       1701  DC XL16'7FF8A000000000000C000000000000000'
0000A0C0  C4C4C240 40D5C640                       1702  DC CL48'DDB  NF -2/+SNaN'
0000A0F0  7FF8A000 00000000                       1703  DC XL16'7FF8A000000000000C000000000000000'
0000A100  C4C4C2D9 40D5C640                       1704  DC CL48'DDBR NF -0/-inf'
0000A130  00000000 00000000                       1705  DC XL16'00000000000000000000000000000000'
0000A140  C4C4C240 40D5C640                       1706  DC CL48'DDB  NF -0/-inf'
0000A170  00000000 00000000                       1707  DC XL16'00000000000000000000000000000000'
0000A180  C4C4C2D9 40D5C640                       1708  DC CL48'DDBR NF -0/-2'
0000A1B0  00000000 00000000                       1709  DC XL16'00000000000000000000000000000000'
0000A1C0  C4C4C240 40D5C640                       1710  DC CL48'DDB  NF -0/-2'
0000A1F0  00000000 00000000                       1711  DC XL16'00000000000000000000000000000000'
0000A200  C4C4C2D9 40D5C640                       1712  DC CL48'DDBR NF -0/-0'
0000A230  7FF80000 00000000                       1713  DC XL16'7FF8000000000000800000000000000'
0000A240  C4C4C240 40D5C640                       1714  DC CL48'DDB  NF -0/-0'
0000A270  7FF80000 00000000                       1715  DC XL16'7FF8000000000000800000000000000'
0000A280  C4C4C2D9 40D5C640                       1716  DC CL48'DDBR NF -0/+0'
0000A2B0  7FF80000 00000000                       1717  DC XL16'7FF8000000000000800000000000000'
0000A2C0  C4C4C240 40D5C640                       1718  DC CL48'DDB  NF -0/+0'
0000A2F0  7FF80000 00000000                       1719  DC XL16'7FF8000000000000800000000000000'
0000A300  C4C4C2D9 40D5C640                       1720  DC CL48'DDBR NF -0/+2'
0000A330  80000000 00000000                       1721  DC XL16'80000000000000008000000000000000'
0000A340  C4C4C240 40D5C640                       1722  DC CL48'DDB  NF -0/+2'
0000A370  80000000 00000000                       1723  DC XL16'80000000000000008000000000000000'
0000A380  C4C4C2D9 40D5C640                       1724  DC CL48'DDBR NF -0/+inf'
0000A3B0  80000000 00000000                       1725  DC XL16'80000000000000008000000000000000'
0000A3C0  C4C4C240 40D5C640                       1726  DC CL48'DDB  NF -0/+inf'
0000A3F0  80000000 00000000                       1727  DC XL16'80000000000000008000000000000000'
0000A400  C4C4C2D9 40D5C640                       1728  DC CL48'DDBR NF -0/-QNaN'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000A430  FFF8B000 00000000                         1729  DC XL16'FFF8B00000000000FFF8B00000000000'
0000A440  C4C4C240 40D5C640                         1730  DC CL48'DDB  NF -0/-QNaN'
0000A470  FFF8B000 00000000                         1731  DC XL16'FFF8B00000000000FFF8B00000000000'
0000A480  C4C4C2D9 40D5C640                         1732  DC CL48'DDBR NF -0/+SNaN'
0000A4B0  7FF8A000 00000000                         1733  DC XL16'7FF8A000000000008000000000000000'
0000A4C0  C4C4C240 40D5C640                         1734  DC CL48'DDB  NF -0/+SNaN'
0000A4F0  7FF8A000 00000000                         1735  DC XL16'7FF8A000000000008000000000000000'
0000A500  C4C4C2D9 40D5C640                         1736  DC CL48'DDBR NF +0/-inf'
0000A530  80000000 00000000                         1737  DC XL16'80000000000000008000000000000000'
0000A540  C4C4C240 40D5C640                         1738  DC CL48'DDB  NF +0/-inf'
0000A570  80000000 00000000                         1739  DC XL16'80000000000000008000000000000000'
0000A580  C4C4C2D9 40D5C640                         1740  DC CL48'DDBR NF +0/-2'
0000A5B0  80000000 00000000                         1741  DC XL16'80000000000000008000000000000000'
0000A5C0  C4C4C240 40D5C640                         1742  DC CL48'DDB  NF +0/-2'
0000A5F0  80000000 00000000                         1743  DC XL16'80000000000000008000000000000000'
0000A600  C4C4C2D9 40D5C640                         1744  DC CL48'DDBR NF +0/-0'
0000A630  7FF80000 00000000                         1745  DC XL16'7FF8000000000000000000000000000'
0000A640  C4C4C240 40D5C640                         1746  DC CL48'DDB  NF +0/-0'
0000A670  7FF80000 00000000                         1747  DC XL16'7FF8000000000000000000000000000'
0000A680  C4C4C2D9 40D5C640                         1748  DC CL48'DDBR NF +0/+0'
0000A6B0  7FF80000 00000000                         1749  DC XL16'7FF8000000000000000000000000000'
0000A6C0  C4C4C240 40D5C640                         1750  DC CL48'DDB  NF +0/+0'
0000A6F0  7FF80000 00000000                         1751  DC XL16'7FF8000000000000000000000000000'
0000A700  C4C4C2D9 40D5C640                         1752  DC CL48'DDBR NF +0/+2'
0000A730  00000000 00000000                         1753  DC XL16'00000000000000000000000000000000'
0000A740  C4C4C240 40D5C640                         1754  DC CL48'DDB  NF +0/+2'
0000A770  00000000 00000000                         1755  DC XL16'00000000000000000000000000000000'
0000A780  C4C4C2D9 40D5C640                         1756  DC CL48'DDBR NF +0/+inf'
0000A7B0  00000000 00000000                         1757  DC XL16'00000000000000000000000000000000'
0000A7C0  C4C4C240 40D5C640                         1758  DC CL48'DDB  NF +0/+inf'
0000A7F0  00000000 00000000                         1759  DC XL16'00000000000000000000000000000000'
0000A800  C4C4C2D9 40D5C640                         1760  DC CL48'DDBR NF +0/-QNaN'
0000A830  FFF8B000 00000000                         1761  DC XL16'FFF8B00000000000FFF8B00000000000'
0000A840  C4C4C240 40D5C640                         1762  DC CL48'DDB  NF +0/-QNaN'
0000A870  FFF8B000 00000000                         1763  DC XL16'FFF8B00000000000FFF8B00000000000'
0000A880  C4C4C2D9 40D5C640                         1764  DC CL48'DDBR NF +0/+SNaN'
0000A8B0  7FF8A000 00000000                         1765  DC XL16'7FF8A000000000000000000000000000'
0000A8C0  C4C4C240 40D5C640                         1766  DC CL48'DDB  NF +0/+SNaN'
0000A8F0  7FF8A000 00000000                         1767  DC XL16'7FF8A000000000000000000000000000'
0000A900  C4C4C2D9 40D5C640                         1768  DC CL48'DDBR NF +2/-inf'
0000A930  80000000 00000000                         1769  DC XL16'80000000000000008000000000000000'
0000A940  C4C4C240 40D5C640                         1770  DC CL48'DDB  NF +2/-inf'
0000A970  80000000 00000000                         1771  DC XL16'80000000000000008000000000000000'
0000A980  C4C4C2D9 40D5C640                         1772  DC CL48'DDBR NF +2/-2'
0000A9B0  BFF00000 00000000                         1773  DC XL16'BFF0000000000000BFF0000000000000'
0000A9C0  C4C4C240 40D5C640                         1774  DC CL48'DDB  NF +2/-2'
0000A9F0  BFF00000 00000000                         1775  DC XL16'BFF0000000000000BFF0000000000000'
0000AA00  C4C4C2D9 40D5C640                         1776  DC CL48'DDBR NF +2/-0'
0000AA30  FFF00000 00000000                         1777  DC XL16'FFF0000000000004000000000000000'
0000AA40  C4C4C240 40D5C640                         1778  DC CL48'DDB  NF +2/-0'
0000AA70  FFF00000 00000000                         1779  DC XL16'FFF0000000000004000000000000000'
0000AA80  C4C4C2D9 40D5C640                         1780  DC CL48'DDBR NF +2/+0'
0000AAB0  7FF00000 00000000                         1781  DC XL16'7FF0000000000004000000000000000'
0000AAC0  C4C4C240 40D5C640                         1782  DC CL48'DDB  NF +2/+0'
0000AAF0  7FF00000 00000000                         1783  DC XL16'7FF0000000000004000000000000000'
0000AB00  C4C4C2D9 40D5C640                         1784  DC CL48'DDBR NF +2/+2'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000AB30  3FF00000 00000000                         1785  DC XL16'3FF00000000000003FF0000000000000'
0000AB40  C4C4C240 40D5C640                         1786  DC CL48'DDB  NF +2/+2'
0000AB70  3FF00000 00000000                         1787  DC XL16'3FF00000000000003FF0000000000000'
0000AB80  C4C4C2D9 40D5C640                         1788  DC CL48'DDBR NF +2/+inf'
0000ABB0  00000000 00000000                         1789  DC XL16'00000000000000000000000000000000'
0000ABC0  C4C4C240 40D5C640                         1790  DC CL48'DDB  NF +2/+inf'
0000ABF0  00000000 00000000                         1791  DC XL16'00000000000000000000000000000000'
0000AC00  C4C4C2D9 40D5C640                         1792  DC CL48'DDBR NF +2/-QNaN'
0000AC30  FFF8B000 00000000                         1793  DC XL16'FFF8B00000000000FFF8B00000000000'
0000AC40  C4C4C240 40D5C640                         1794  DC CL48'DDB  NF +2/-QNaN'
0000AC70  FFF8B000 00000000                         1795  DC XL16'FFF8B00000000000FFF8B00000000000'
0000AC80  C4C4C2D9 40D5C640                         1796  DC CL48'DDBR NF +2/+SNaN'
0000ACB0  7FF8A000 00000000                         1797  DC XL16'7FF8A00000000004000000000000000'
0000ACC0  C4C4C240 40D5C640                         1798  DC CL48'DDB  NF +2/+SNaN'
0000ACF0  7FF8A000 00000000                         1799  DC XL16'7FF8A00000000004000000000000000'
0000AD00  C4C4C2D9 40D5C640                         1800  DC CL48'DDBR NF +inf/-inf'
0000AD30  7FF80000 00000000                         1801  DC XL16'7FF80000000000007FF0000000000000'
0000AD40  C4C4C240 40D5C640                         1802  DC CL48'DDB  NF +inf/-inf'
0000AD70  7FF80000 00000000                         1803  DC XL16'7FF80000000000007FF0000000000000'
0000AD80  C4C4C2D9 40D5C640                         1804  DC CL48'DDBR NF +inf/-2'
0000ADB0  FFF00000 00000000                         1805  DC XL16'FFF0000000000000FFF0000000000000'
0000ADC0  C4C4C240 40D5C640                         1806  DC CL48'DDB  NF +inf/-2'
0000ADF0  FFF00000 00000000                         1807  DC XL16'FFF0000000000000FFF0000000000000'
0000AE00  C4C4C2D9 40D5C640                         1808  DC CL48'DDBR NF +inf/-0'
0000AE30  FFF00000 00000000                         1809  DC XL16'FFF0000000000000FFF0000000000000'
0000AE40  C4C4C240 40D5C640                         1810  DC CL48'DDB  NF +inf/-0'
0000AE70  FFF00000 00000000                         1811  DC XL16'FFF0000000000000FFF0000000000000'
0000AE80  C4C4C2D9 40D5C640                         1812  DC CL48'DDBR NF +inf/+0'
0000AEB0  7FF00000 00000000                         1813  DC XL16'7FF00000000000007FF0000000000000'
0000AEC0  C4C4C240 40D5C640                         1814  DC CL48'DDB  NF +inf/+0'
0000AEF0  7FF00000 00000000                         1815  DC XL16'7FF00000000000007FF0000000000000'
0000AF00  C4C4C2D9 40D5C640                         1816  DC CL48'DDBR NF +inf/+2'
0000AF30  7FF00000 00000000                         1817  DC XL16'7FF00000000000007FF0000000000000'
0000AF40  C4C4C240 40D5C640                         1818  DC CL48'DDB  NF +inf/+2'
0000AF70  7FF00000 00000000                         1819  DC XL16'7FF00000000000007FF0000000000000'
0000AF80  C4C4C2D9 40D5C640                         1820  DC CL48'DDBR NF +inf/+inf'
0000AFB0  7FF80000 00000000                         1821  DC XL16'7FF80000000000007FF0000000000000'
0000AFC0  C4C4C240 40D5C640                         1822  DC CL48'DDB  NF +inf/+inf'
0000AFF0  7FF80000 00000000                         1823  DC XL16'7FF80000000000007FF0000000000000'
0000B000  C4C4C2D9 40D5C640                         1824  DC CL48'DDBR NF +inf/-QNaN'
0000B030  FFF8B000 00000000                         1825  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B040  C4C4C240 40D5C640                         1826  DC CL48'DDB  NF +inf/-QNaN'
0000B070  FFF8B000 00000000                         1827  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B080  C4C4C2D9 40D5C640                         1828  DC CL48'DDBR NF +inf/+SNaN'
0000B0B0  7FF8A000 00000000                         1829  DC XL16'7FF8A000000000007FF0000000000000'
0000B0C0  C4C4C240 40D5C640                         1830  DC CL48'DDB  NF +inf/+SNaN'
0000B0F0  7FF8A000 00000000                         1831  DC XL16'7FF8A000000000007FF0000000000000'
0000B100  C4C4C2D9 40D5C640                         1832  DC CL48'DDBR NF -QNaN/-inf'
0000B130  FFF8B000 00000000                         1833  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B140  C4C4C240 40D5C640                         1834  DC CL48'DDB  NF -QNaN/-inf'
0000B170  FFF8B000 00000000                         1835  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B180  C4C4C2D9 40D5C640                         1836  DC CL48'DDBR NF -QNaN/-2'
0000B1B0  FFF8B000 00000000                         1837  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B1C0  C4C4C240 40D5C640                         1838  DC CL48'DDB  NF -QNaN/-2'
0000B1F0  FFF8B000 00000000                         1839  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B200  C4C4C2D9 40D5C640                         1840  DC CL48'DDBR NF -QNaN/-0'
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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000B230  FFF8B000 00000000                         1841  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B240  C4C4C240 40D5C640                         1842  DC CL48'DDB  NF -QNaN/-0'
0000B270  FFF8B000 00000000                         1843  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B280  C4C4C2D9 40D5C640                         1844  DC CL48'DDBR NF -QNaN/+0'
0000B2B0  FFF8B000 00000000                         1845  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B2C0  C4C4C240 40D5C640                         1846  DC CL48'DDB  NF -QNaN/+0'
0000B2F0  FFF8B000 00000000                         1847  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B300  C4C4C2D9 40D5C640                         1848  DC CL48'DDBR NF -QNaN/+2'
0000B330  FFF8B000 00000000                         1849  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B340  C4C4C240 40D5C640                         1850  DC CL48'DDB  NF -QNaN/+2'
0000B370  FFF8B000 00000000                         1851  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B380  C4C4C2D9 40D5C640                         1852  DC CL48'DDBR NF -QNaN/+inf'
0000B3B0  FFF8B000 00000000                         1853  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B3C0  C4C4C240 40D5C640                         1854  DC CL48'DDB  NF -QNaN/+inf'
0000B3F0  FFF8B000 00000000                         1855  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B400  C4C4C2D9 40D5C640                         1856  DC CL48'DDBR NF -QNaN/-QNaN'
0000B430  FFF8B000 00000000                         1857  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B440  C4C4C240 40D5C640                         1858  DC CL48'DDB  NF -QNaN/-QNaN'
0000B470  FFF8B000 00000000                         1859  DC XL16'FFF8B00000000000FFF8B00000000000'
0000B480  C4C4C2D9 40D5C640                         1860  DC CL48'DDBR NF -QNaN/+SNaN'
0000B4B0  7FF8A000 00000000                         1861  DC XL16'7FF8A00000000000FFF8B00000000000'
0000B4C0  C4C4C240 40D5C640                         1862  DC CL48'DDB  NF -QNaN/+SNaN'
0000B4F0  7FF8A000 00000000                         1863  DC XL16'7FF8A00000000000FFF8B00000000000'
0000B500  C4C4C2D9 40D5C640                         1864  DC CL48'DDBR NF +SNaN/-inf'
0000B530  7FF8A000 00000000                         1865  DC XL16'7FF8A000000000007FF0A00000000000'
0000B540  C4C4C240 40D5C640                         1866  DC CL48'DDB  NF +SNaN/-inf'
0000B570  7FF8A000 00000000                         1867  DC XL16'7FF8A000000000007FF0A00000000000'
0000B580  C4C4C2D9 40D5C640                         1868  DC CL48'DDBR NF +SNaN/-2'
0000B5B0  7FF8A000 00000000                         1869  DC XL16'7FF8A000000000007FF0A00000000000'
0000B5C0  C4C4C240 40D5C640                         1870  DC CL48'DDB  NF +SNaN/-2'
0000B5F0  7FF8A000 00000000                         1871  DC XL16'7FF8A000000000007FF0A00000000000'
0000B600  C4C4C2D9 40D5C640                         1872  DC CL48'DDBR NF +SNaN/-0'
0000B630  7FF8A000 00000000                         1873  DC XL16'7FF8A000000000007FF0A00000000000'
0000B640  C4C4C240 40D5C640                         1874  DC CL48'DDB  NF +SNaN/-0'
0000B670  7FF8A000 00000000                         1875  DC XL16'7FF8A000000000007FF0A00000000000'
0000B680  C4C4C2D9 40D5C640                         1876  DC CL48'DDBR NF +SNaN/+0'
0000B6B0  7FF8A000 00000000                         1877  DC XL16'7FF8A000000000007FF0A00000000000'
0000B6C0  C4C4C240 40D5C640                         1878  DC CL48'DDB  NF +SNaN/+0'
0000B6F0  7FF8A000 00000000                         1879  DC XL16'7FF8A000000000007FF0A00000000000'
0000B700  C4C4C2D9 40D5C640                         1880  DC CL48'DDBR NF +SNaN/+2'
0000B730  7FF8A000 00000000                         1881  DC XL16'7FF8A000000000007FF0A00000000000'
0000B740  C4C4C240 40D5C640                         1882  DC CL48'DDB  NF +SNaN/+2'
0000B770  7FF8A000 00000000                         1883  DC XL16'7FF8A000000000007FF0A00000000000'
0000B780  C4C4C2D9 40D5C640                         1884  DC CL48'DDBR NF +SNaN/+inf'
0000B7B0  7FF8A000 00000000                         1885  DC XL16'7FF8A000000000007FF0A00000000000'
0000B7C0  C4C4C240 40D5C640                         1886  DC CL48'DDB  NF +SNaN/+inf'
0000B7F0  7FF8A000 00000000                         1887  DC XL16'7FF8A000000000007FF0A00000000000'
0000B800  C4C4C2D9 40D5C640                         1888  DC CL48'DDBR NF +SNaN/-QNaN'
0000B830  7FF8A000 00000000                         1889  DC XL16'7FF8A000000000007FF0A00000000000'
0000B840  C4C4C240 40D5C640                         1890  DC CL48'DDB  NF +SNaN/-QNaN'
0000B870  7FF8A000 00000000                         1891  DC XL16'7FF8A000000000007FF0A00000000000'
0000B880  C4C4C2D9 40D5C640                         1892  DC CL48'DDBR NF +SNaN/+SNaN'
0000B8B0  7FF8A000 00000000                         1893  DC XL16'7FF8A000000000007FF0A00000000000'
0000B8C0  C4C4C240 40D5C640                         1894  DC CL48'DDB  NF +SNaN/+SNaN'
0000B8F0  7FF8A000 00000000                         1895  DC XL16'7FF8A000000000007FF0A00000000000'
                             00000080  00000001  1896 LBFPNFOT_NUM EQU (*-LBFPNFOT_GOOD)/64
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  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

                                                   1897 *
                                                   1898 *
                                0000B900  00000001 1899 LBFPNFFL_GOOD EQU *
0000B900  C4C4C2D9 61C4C4C2                        1900  DC CL48'DDBR/DDB NF -inf/-inf FPCR'
0000B930  00800000 F8008000                        1901  DC XL16'00800000F8008000008000000F8008000'
0000B940  C4C4C2D9 61C4C4C2                        1902  DC CL48'DDBR/DDB NF -inf/-2 FPCR'
0000B970  00000000 F8000000                        1903  DC XL16'00000000F8000000000000000F8000000'
0000B980  C4C4C2D9 61C4C4C2                        1904  DC CL48'DDBR/DDB NF -inf/-0 FPCR'
0000B9B0  00000000 F8000000                        1905  DC XL16'00000000F8000000000000000F8000000'
0000B9C0  C4C4C2D9 61C4C4C2                        1906  DC CL48'DDBR/DDB NF -inf/+0 FPCR'
0000B9F0  00000000 F8000000                        1907  DC XL16'00000000F8000000000000000F8000000'
0000BA00  C4C4C2D9 61C4C4C2                        1908  DC CL48'DDBR/DDB NF -inf/+2 FPCR'
0000BA30  00000000 F8000000                        1909  DC XL16'00000000F8000000000000000F8000000'
0000BA40  C4C4C2D9 61C4C4C2                        1910  DC CL48'DDBR/DDB NF -inf/+inf FPCR'
0000BA70  00800000 F8008000                        1911  DC XL16'00800000F8008000008000000F8008000'
0000BA80  C4C4C2D9 61C4C4C2                        1912  DC CL48'DDBR/DDB NF -inf/-QNaN FPCR'
0000BAB0  00000000 F8000000                        1913  DC XL16'00000000F8000000000000000F8000000'
0000BAC0  C4C4C2D9 61C4C4C2                        1914  DC CL48'DDBR/DDB NF -inf/+SNaN FPCR'
0000BAF0  00800000 F8008000                        1915  DC XL16'00800000F8008000008000000F8008000'
0000BB00  C4C4C2D9 61C4C4C2                        1916  DC CL48'DDBR/DDB NF -2/-inf FPCR'
0000BB30  00000000 F8000000                        1917  DC XL16'00000000F8000000000000000F8000000'
0000BB40  C4C4C2D9 61C4C4C2                        1918  DC CL48'DDBR/DDB NF -2/-2 FPCR'
0000BB70  00000000 F8000000                        1919  DC XL16'00000000F8000000000000000F8000000'
0000BB80  C4C4C2D9 61C4C4C2                        1920  DC CL48'DDBR/DDB NF -2/-0 FPCR'
0000BBB0  00400000 F8004000                        1921  DC XL16'00400000F8004000004000000F8004000'
0000BBC0  C4C4C2D9 61C4C4C2                        1922  DC CL48'DDBR/DDB NF -2/+0 FPCR'
0000BBF0  00400000 F8004000                        1923  DC XL16'00400000F8004000004000000F8004000'
0000BC00  C4C4C2D9 61C4C4C2                        1924  DC CL48'DDBR/DDB NF -2/+2 FPCR'
0000BC30  00000000 F8000000                        1925  DC XL16'00000000F8000000000000000F8000000'
0000BC40  C4C4C2D9 61C4C4C2                        1926  DC CL48'DDBR/DDB NF -2/+inf FPCR'
0000BC70  00000000 F8000000                        1927  DC XL16'00000000F8000000000000000F8000000'
0000BC80  C4C4C2D9 61C4C4C2                        1928  DC CL48'DDBR/DDB NF -2/-QNaN FPCR'
0000BCB0  00000000 F8000000                        1929  DC XL16'00000000F8000000000000000F8000000'
0000BCC0  C4C4C2D9 61C4C4C2                        1930  DC CL48'DDBR/DDB NF -2/+SNaN FPCR'
0000BCF0  00800000 F8008000                        1931  DC XL16'00800000F8008000008000000F8008000'
0000BD00  C4C4C2D9 61C4C4C2                        1932  DC CL48'DDBR/DDB NF -0/-inf FPCR'
0000BD30  00000000 F8000000                        1933  DC XL16'00000000F8000000000000000F8000000'
0000BD40  C4C4C2D9 61C4C4C2                        1934  DC CL48'DDBR/DDB NF -0/-2 FPCR'
0000BD70  00000000 F8000000                        1935  DC XL16'00000000F8000000000000000F8000000'
0000BD80  C4C4C2D9 61C4C4C2                        1936  DC CL48'DDBR/DDB NF -0/-0 FPCR'
0000BDB0  00800000 F8008000                        1937  DC XL16'00800000F8008000008000000F8008000'
0000BDC0  C4C4C2D9 61C4C4C2                        1938  DC CL48'DDBR/DDB NF -0/+0 FPCR'
0000BDF0  00800000 F8008000                        1939  DC XL16'00800000F8008000008000000F8008000'
0000BE00  C4C4C2D9 61C4C4C2                        1940  DC CL48'DDBR/DDB NF -0/+2 FPCR'
0000BE30  00000000 F8000000                        1941  DC XL16'00000000F8000000000000000F8000000'
0000BE40  C4C4C2D9 61C4C4C2                        1942  DC CL48'DDBR/DDB NF -0/+inf FPCR'
0000BE70  00000000 F8000000                        1943  DC XL16'00000000F8000000000000000F8000000'
0000BE80  C4C4C2D9 61C4C4C2                        1944  DC CL48'DDBR/DDB NF -0/-QNaN FPCR'
0000BEB0  00000000 F8000000                        1945  DC XL16'00000000F8000000000000000F8000000'
0000BEC0  C4C4C2D9 61C4C4C2                        1946  DC CL48'DDBR/DDB NF -0/+SNaN FPCR'
0000BEF0  00800000 F8008000                        1947  DC XL16'00800000F8008000008000000F8008000'
0000BF00  C4C4C2D9 61C4C4C2                        1948  DC CL48'DDBR/DDB NF +0/-inf FPCR'
0000BF30  00000000 F8000000                        1949  DC XL16'00000000F8000000000000000F8000000'
0000BF40  C4C4C2D9 61C4C4C2                        1950  DC CL48'DDBR/DDB NF +0/-2 FPCR'
0000BF70  00000000 F8000000                        1951  DC XL16'00000000F8000000000000000F8000000'
0000BF80  C4C4C2D9 61C4C4C2                        1952  DC CL48'DDBR/DDB NF +0/-0 FPCR'
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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000BFB0  00800000 F8008000                         1953  DC XL16'00800000F8008000800000F8008000'
0000BFC0  C4C4C2D9 61C4C4C2                         1954  DC CL48'DDBR/DDB NF +0/+0 FPCR'
0000BFF0  00800000 F8008000                         1955  DC XL16'00800000F8008000800000F8008000'
0000C000  C4C4C2D9 61C4C4C2                         1956  DC CL48'DDBR/DDB NF +0/+2 FPCR'
0000C030  00000000 F8000000                         1957  DC XL16'00000000F8000000000000F8000000'
0000C040  C4C4C2D9 61C4C4C2                         1958  DC CL48'DDBR/DDB NF +0/+inf FPCR'
0000C070  00000000 F8000000                         1959  DC XL16'00000000F8000000000000F8000000'
0000C080  C4C4C2D9 61C4C4C2                         1960  DC CL48'DDBR/DDB NF +0/-QNaN FPCR'
0000C0B0  00000000 F8000000                         1961  DC XL16'00000000F8000000000000F8000000'
0000C0C0  C4C4C2D9 61C4C4C2                         1962  DC CL48'DDBR/DDB NF +0/+SNaN FPCR'
0000C0F0  00800000 F8008000                         1963  DC XL16'00800000F8008000800000F8008000'
0000C100  C4C4C2D9 61C4C4C2                         1964  DC CL48'DDBR/DDB NF +2/-inf FPCR'
0000C130  00000000 F8000000                         1965  DC XL16'00000000F8000000000000F8000000'
0000C140  C4C4C2D9 61C4C4C2                         1966  DC CL48'DDBR/DDB NF +2/-2 FPCR'
0000C170  00000000 F8000000                         1967  DC XL16'00000000F8000000000000F8000000'
0000C180  C4C4C2D9 61C4C4C2                         1968  DC CL48'DDBR/DDB NF +2/-0 FPCR'
0000C1B0  00400000 F8004000                         1969  DC XL16'00400000F8004000040000F8004000'
0000C1C0  C4C4C2D9 61C4C4C2                         1970  DC CL48'DDBR/DDB NF +2/+0 FPCR'
0000C1F0  00400000 F8004000                         1971  DC XL16'00400000F8004000040000F8004000'
0000C200  C4C4C2D9 61C4C4C2                         1972  DC CL48'DDBR/DDB NF +2/+2 FPCR'
0000C230  00000000 F8000000                         1973  DC XL16'00000000F8000000000000F8000000'
0000C240  C4C4C2D9 61C4C4C2                         1974  DC CL48'DDBR/DDB NF +2/+inf FPCR'
0000C270  00000000 F8000000                         1975  DC XL16'00000000F8000000000000F8000000'
0000C280  C4C4C2D9 61C4C4C2                         1976  DC CL48'DDBR/DDB NF +2/-QNaN FPCR'
0000C2B0  00000000 F8000000                         1977  DC XL16'00000000F8000000000000F8000000'
0000C2C0  C4C4C2D9 61C4C4C2                         1978  DC CL48'DDBR/DDB NF +2/+SNaN FPCR'
0000C2F0  00800000 F8008000                         1979  DC XL16'00800000F8008000800000F8008000'
0000C300  C4C4C2D9 61C4C4C2                         1980  DC CL48'DDBR/DDB NF +inf/-inf FPCR'
0000C330  00800000 F8008000                         1981  DC XL16'00800000F8008000800000F8008000'
0000C340  C4C4C2D9 61C4C4C2                         1982  DC CL48'DDBR/DDB NF +inf/-2 FPCR'
0000C370  00000000 F8000000                         1983  DC XL16'00000000F8000000000000F8000000'
0000C380  C4C4C2D9 61C4C4C2                         1984  DC CL48'DDBR/DDB NF +inf/-0 FPCR'
0000C3B0  00000000 F8000000                         1985  DC XL16'00000000F8000000000000F8000000'
0000C3C0  C4C4C2D9 61C4C4C2                         1986  DC CL48'DDBR/DDB NF +inf/+0 FPCR'
0000C3F0  00000000 F8000000                         1987  DC XL16'00000000F8000000000000F8000000'
0000C400  C4C4C2D9 61C4C4C2                         1988  DC CL48'DDBR/DDB NF +inf/+2 FPCR'
0000C430  00000000 F8000000                         1989  DC XL16'00000000F8000000000000F8000000'
0000C440  C4C4C2D9 61C4C4C2                         1990  DC CL48'DDBR/DDB NF +inf/+inf FPCR'
0000C470  00800000 F8008000                         1991  DC XL16'00800000F8008000800000F8008000'
0000C480  C4C4C2D9 61C4C4C2                         1992  DC CL48'DDBR/DDB NF +inf/-QNaN FPCR'
0000C4B0  00000000 F8000000                         1993  DC XL16'00000000F8000000000000F8000000'
0000C4C0  C4C4C2D9 61C4C4C2                         1994  DC CL48'DDBR/DDB NF +inf/+SNaN FPCR'
0000C4F0  00800000 F8008000                         1995  DC XL16'00800000F8008000800000F8008000'
0000C500  C4C4C2D9 61C4C4C2                         1996  DC CL48'DDBR/DDB NF -QNaN/-inf FPCR'
0000C530  00000000 F8000000                         1997  DC XL16'00000000F8000000000000F8000000'
0000C540  C4C4C2D9 61C4C4C2                         1998  DC CL48'DDBR/DDB NF -QNaN/-2 FPCR'
0000C570  00000000 F8000000                         1999  DC XL16'00000000F8000000000000F8000000'
0000C580  C4C4C2D9 61C4C4C2                         2000  DC CL48'DDBR/DDB NF -QNaN/-0 FPCR'
0000C5B0  00000000 F8000000                         2001  DC XL16'00000000F8000000000000F8000000'
0000C5C0  C4C4C2D9 61C4C4C2                         2002  DC CL48'DDBR/DDB NF -QNaN/+0 FPCR'
0000C5F0  00000000 F8000000                         2003  DC XL16'00000000F8000000000000F8000000'
0000C600  C4C4C2D9 61C4C4C2                         2004  DC CL48'DDBR/DDB NF -QNaN/+2 FPCR'
0000C630  00000000 F8000000                         2005  DC XL16'00000000F8000000000000F8000000'
0000C640  C4C4C2D9 61C4C4C2                         2006  DC CL48'DDBR/DDB NF -QNaN/+inf FPCR'
0000C670  00000000 F8000000                         2007  DC XL16'00000000F8000000000000F8000000'
0000C680  C4C4C2D9 61C4C4C2                         2008  DC CL48'DDBR/DDB NF -QNaN/-QNaN FPCR'
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  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

0000C6B0  00000000 F8000000                        2009  DC XL16'00000000F800000000000000F8000000'
0000C6C0  C4C4C2D9 61C4C4C2                        2010  DC CL48'DDBR/DDB NF -QNaN/+SNaN FPCR'
0000C6F0  00800000 F8008000                        2011  DC XL16'00800000F800800000800000F8008000'
0000C700  C4C4C2D9 61C4C4C2                        2012  DC CL48'DDBR/DDB NF +SNaN/-inf FPCR'
0000C730  00800000 F8008000                        2013  DC XL16'00800000F800800000800000F8008000'
0000C740  C4C4C2D9 61C4C4C2                        2014  DC CL48'DDBR/DDB NF +SNaN/-2 FPCR'
0000C770  00800000 F8008000                        2015  DC XL16'00800000F800800000800000F8008000'
0000C780  C4C4C2D9 61C4C4C2                        2016  DC CL48'DDBR/DDB NF +SNaN/-0 FPCR'
0000C7B0  00800000 F8008000                        2017  DC XL16'00800000F800800000800000F8008000'
0000C7C0  C4C4C2D9 61C4C4C2                        2018  DC CL48'DDBR/DDB NF +SNaN/+0 FPCR'
0000C7F0  00800000 F8008000                        2019  DC XL16'00800000F800800000800000F8008000'
0000C800  C4C4C2D9 61C4C4C2                        2020  DC CL48'DDBR/DDB NF +SNaN/+2 FPCR'
0000C830  00800000 F8008000                        2021  DC XL16'00800000F800800000800000F8008000'
0000C840  C4C4C2D9 61C4C4C2                        2022  DC CL48'DDBR/DDB NF +SNaN/+inf FPCR'
0000C870  00800000 F8008000                        2023  DC XL16'00800000F800800000800000F8008000'
0000C880  C4C4C2D9 61C4C4C2                        2024  DC CL48'DDBR/DDB NF +SNaN/-QNaN FPCR'
0000C8B0  00800000 F8008000                        2025  DC XL16'00800000F800800000800000F8008000'
0000C8C0  C4C4C2D9 61C4C4C2                        2026  DC CL48'DDBR/DDB NF +SNaN/+SNaN FPCR'
0000C8F0  00800000 F8008000                        2027  DC XL16'00800000F800800000800000F8008000'
                            00000040  00000001   2028 LBFPNFFL_NUM EQU (*-LBFPNFFL_GOOD)/64
                                                 2029 *
                                                 2030 *
                            0000C900  00000001   2031 LBFPOUT_GOOD EQU *
0000C900  C4C4C2D9 409481A7                        2032  DC CL48'DDBR max/min'
0000C930  7FF00000 00000000                        2033  DC XL16'7FF0000000000000630FFFFFFFFFFFF'
0000C940  C4C4C240 9481A761                        2034  DC CL48'DDB max/min'
0000C970  7FF00000 00000000                        2035  DC XL16'7FF0000000000000630FFFFFFFFFFFF'
0000C980  C4C4C2D9 40948995                        2036  DC CL48'DDBR min/2.0'
0000C9B0  00080000 00000000                        2037  DC XL16'00080000000000006000000000000000'
0000C9C0  C4C4C240 94899561                        2038  DC CL48'DDB min/2.0'
0000C9F0  00080000 00000000                        2039  DC XL16'00080000000000006000000000000000'
0000CA00  C4C4C2D9 40F14BF0                        2040  DC CL48'DDBR 1.0/10.0'
0000CA30  3FB99999 9999999A                        2041  DC XL16'3FB999999999999A3FB999999999999A'
0000CA40  C4C4C240 F14BF061                        2042  DC CL48'DDB 1.0/10.0'
0000CA70  3FB99999 9999999A                        2043  DC XL16'3FB999999999999A3FB999999999999A'
0000CA80  C4C4C2D9 40F74BF0                        2044  DC CL48'DDBR 7.0/10.0'
0000CAB0  3FE66666 66666666                        2045  DC XL16'3FE66666666666663FE6666666666666'
0000CAC0  C4C4C240 F74BF061                        2046  DC CL48'DDB 7.0/10.0'
0000CAF0  3FE66666 66666666                        2047  DC XL16'3FE66666666666663FE6666666666666'
0000CB00  C4C4C2D9 40F14BF0                        2048  DC CL48'DDBR 1.0/-10.0'
0000CB30  BFB99999 9999999A                        2049  DC XL16'BFB999999999999ABFB999999999999A'
0000CB40  C4C4C240 F14BF061                        2050  DC CL48'DDB 1.0/-10.0'
0000CB70  BFB99999 9999999A                        2051  DC XL16'BFB999999999999ABFB999999999999A'
0000CB80  C4C4C2D9 40F74BF0                        2052  DC CL48'DDBR 7.0/-10.0'
0000CBB0  BFE66666 66666666                        2053  DC XL16'BFE6666666666666BFE6666666666666'
0000CBC0  C4C4C240 F74BF061                        2054  DC CL48'DDB 7.0/-10.0'
0000CBF0  BFE66666 66666666                        2055  DC XL16'BFE6666666666666BFE6666666666666'
                            0000000C  00000001   2056 LBFPOUT_NUM EQU (*-LBFPOUT_GOOD)/64
                                                 2057 *
                                                 2058 *
                            0000CC00  00000001   2059 LBFPFLGS_GOOD EQU *
0000CC00  C4C4C2D9 61C4C4C2                        2060  DC CL48'DDBR/DDB max/min FPCR'
0000CC30  00280000 F8002000                        2061  DC XL16'00280000F800200000280000F8002000'
0000CC40  C4C4C2D9 61C4C4C2                        2062  DC CL48'DDBR/DDB min/2.0 FPCR'
0000CC70  00000000 F8001000                        2063  DC XL16'00000000F800100000000000F8001000'
0000CC80  C4C4C2D9 61C4C4C2                        2064  DC CL48'DDBR/DDB 1.0/10.0 FPCR'
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  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

0000CCB0  00080000 F8000C00                         2065  DC XL16'00080000F8000C0000080000F8000C00'
0000CCC0  C4C4C2D9 61C4C4C2                         2066  DC CL48'DDBR/DDB 7.0/10.0 FPCR'
0000CCF0  00080000 F8000800                         2067  DC XL16'00080000F80008000080000F8000800'
0000CD00  C4C4C2D9 61C4C4C2                         2068  DC CL48'DDBR/DDB 1.0/-10.0 FPCR'
0000CD30  00080000 F8000C00                         2069  DC XL16'00080000F8000C0000080000F8000C00'
0000CD40  C4C4C2D9 61C4C4C2                         2070  DC CL48'DDBR/DDB 7.0/-10.0 FPCR'
0000CD70  00080000 F8000800                         2071  DC XL16'00080000F80008000080000F8000800'
                             00000006  00000001    2072 LBFPFLGS_NUM EQU (*-LBFPFLGS_GOOD)/64
                                                    2073 *
                                                    2074 *
                             0000CD80  00000001    2075 LBFPRMO_GOOD EQU *
0000CD80  C4C4C2D9 61C4C4C2                         2076  DC CL48'DDBR/DDB RM RNTE 1/10'
0000CDB0  3FB99999 9999999A                         2077  DC XL16'3FB999999999999A3FB999999999999A'
0000CDC0  C4C4C2D9 61C4C4C2                         2078  DC CL48'DDBR/DDB RM RZ 1/10'
0000CDF0  3FB99999 99999999                         2079  DC XL16'3FB99999999999993FB9999999999999'
0000CE00  C4C4C2D9 61C4C4C2                         2080  DC CL48'DDBR/DDB RM RP 1/10'
0000CE30  3FB99999 9999999A                         2081  DC XL16'3FB999999999999A3FB999999999999A'
0000CE40  C4C4C2D9 61C4C4C2                         2082  DC CL48'DDBR/DDB RM RM 1/10'
0000CE70  3FB99999 99999999                         2083  DC XL16'3FB99999999999993FB9999999999999'
0000CE80  C4C4C2D9 61C4C4C2                         2084  DC CL48'DDBR/DDB RM RFS 1/10'
0000CEB0  3FB99999 99999999                         2085  DC XL16'3FB99999999999993FB9999999999999'
0000CEC0  C4C4C2D9 61C4C4C2                         2086  DC CL48'DDBR/DDB RM RNTE 7/10'
0000CEF0  3FE66666 66666666                         2087  DC XL16'3FE666666666666663FE6666666666666'
0000CF00  C4C4C2D9 61C4C4C2                         2088  DC CL48'DDBR/DDB RM RZ 7/10'
0000CF30  3FE66666 66666666                         2089  DC XL16'3FE666666666666663FE6666666666666'
0000CF40  C4C4C2D9 61C4C4C2                         2090  DC CL48'DDBR/DDB RM RP 7/10'
0000CF70  3FE66666 66666667                         2091  DC XL16'3FE666666666666673FE6666666666667'
0000CF80  C4C4C2D9 61C4C4C2                         2092  DC CL48'DDBR/DDB RM RM 7/10'
0000CFB0  3FE66666 66666666                         2093  DC XL16'3FE666666666666663FE6666666666666'
0000CFC0  C4C4C2D9 61C4C4C2                         2094  DC CL48'DDBR/DDB RM RFS 7/10'
0000CFF0  3FE66666 66666667                         2095  DC XL16'3FE666666666666673FE6666666666667'
0000D000  C4C4C2D9 61C4C4C2                         2096  DC CL48'DDBR/DDB RM RNTE 1/-10'
0000D030  BFB99999 9999999A                         2097  DC XL16'BFB999999999999ABFB999999999999A'
0000D040  C4C4C2D9 61C4C4C2                         2098  DC CL48'DDBR/DDB RM RZ 1/-10'
0000D070  BFB99999 99999999                         2099  DC XL16'BFB99999999999993FB9999999999999'
0000D080  C4C4C2D9 61C4C4C2                         2100  DC CL48'DDBR/DDB RM RP 1/-10'
0000D0B0  BFB99999 99999999                         2101  DC XL16'BFB99999999999993FB9999999999999'
0000D0C0  C4C4C2D9 61C4C4C2                         2102  DC CL48'DDBR/DDB RM RM 1/-10'
0000D0F0  BFB99999 9999999A                         2103  DC XL16'BFB999999999999ABFB999999999999A'
0000D100  C4C4C2D9 61C4C4C2                         2104  DC CL48'DDBR/DDB RM RFS 1/-10'
0000D130  BFB99999 99999999                         2105  DC XL16'BFB99999999999993FB9999999999999'
0000D140  C4C4C2D9 61C4C4C2                         2106  DC CL48'DDBR/DDB RM RNTE 7/-10'
0000D170  BFE66666 66666666                         2107  DC XL16'BFE666666666666BFE6666666666666'
0000D180  C4C4C2D9 61C4C4C2                         2108  DC CL48'DDBR/DDB RM RZ 7/-10'
0000D1B0  BFE66666 66666666                         2109  DC XL16'BFE666666666666BFE6666666666666'
0000D1C0  C4C4C2D9 61C4C4C2                         2110  DC CL48'DDBR/DDB RM RP 7/-10'
0000D1F0  BFE66666 66666666                         2111  DC XL16'BFE666666666666BFE6666666666666'
0000D200  C4C4C2D9 61C4C4C2                         2112  DC CL48'DDBR/DDB RM RM 7/-10'
0000D230  BFE66666 66666667                         2113  DC XL16'BFE666666666666BFE6666666666667'
0000D240  C4C4C2D9 61C4C4C2                         2114  DC CL48'DDBR/DDB RM RFS 7/-10'
0000D270  BFE66666 66666667                         2115  DC XL16'BFE666666666666BFE6666666666667'
                             00000014  00000001    2116 LBFPRMO_NUM EQU (*-LBFPRMO_GOOD)/64
                                                    2117 *
                                                    2118 *
                             0000D280  00000001    2119 LBFPRMOF_GOOD EQU *
0000D280  C4C4C2D9 61C4C4C2                         2120  DC CL48'DDBR/DDB RM RNTE,RZ 1/10 FPCR'
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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000D2B0  00080000 00080000                         2121  DC XL16'00080000000800000008000100080001'
0000D2C0  C4C4C2D9 61C4C4C2                         2122  DC CL48'DDBR/DDB RM RP,RM 1/10 FPCR'
0000D2F0  00080002 00080002                         2123  DC XL16'00080002000800020008000300080003'
0000D300  C4C4C2D9 61C4C4C2                         2124  DC CL48'DDBR/DDB RM RFS 1/10 FPCR'
0000D330  00080007 00080007                         2125  DC XL16'00080007000800070000000000000000'
0000D340  C4C4C2D9 61C4C4C2                         2126  DC CL48'DDBR/DDB RM RNTE,RZ 7/10 FPCR'
0000D370  00080000 00080000                         2127  DC XL16'00080000000800000008000100080001'
0000D380  C4C4C2D9 61C4C4C2                         2128  DC CL48'DDBR/DDB RM RP,RM 7/10 FPCR'
0000D3B0  00080002 00080002                         2129  DC XL16'00080002000800020008000300080003'
0000D3C0  C4C4C2D9 61C4C4C2                         2130  DC CL48'DDBR/DDB RM RFS 7/10 FPCR'
0000D3F0  00080007 00080007                         2131  DC XL16'00080007000800070000000000000000'
0000D400  C4C4C2D9 61C4C4C2                         2132  DC CL48'DDBR/DDB RM RNTE,RZ 1/-10 FPCR'
0000D430  00080000 00080000                         2133  DC XL16'00080000000800000008000100080001'
0000D440  C4C4C2D9 61C4C4C2                         2134  DC CL48'DDBR/DDB RM RP,RM 1/-10 FPCR'
0000D470  00080002 00080002                         2135  DC XL16'00080002000800020008000300080003'
0000D480  C4C4C2D9 61C4C4C2                         2136  DC CL48'DDBR/DDB RM RFS 1/-10 FPCR'
0000D4B0  00080007 00080007                         2137  DC XL16'00080007000800070000000000000000'
0000D4C0  C4C4C2D9 61C4C4C2                         2138  DC CL48'DDBR/DDB RM RNTE,RZ 7/-10 FPCR'
0000D4F0  00080000 00080000                         2139  DC XL16'00080000000800000008000100080001'
0000D500  C4C4C2D9 61C4C4C2                         2140  DC CL48'DDBR/DDB RM RP,RM 7/-10 FPCR'
0000D530  00080002 00080002                         2141  DC XL16'00080002000800020008000300080003'
0000D540  C4C4C2D9 61C4C4C2                         2142  DC CL48'DDBR/DDB RM RFS 7/-10 FPCR'
0000D570  00080007 00080007                         2143  DC XL16'00080007000800070000000000000000'
                            0000000C  00000001    2144 LBFPRMOF_NUM EQU (*-LBFPRMOF_GOOD)/64
                                                  2145 *
                                                  2146 *
                            0000D580  00000001    2147 XBFPNFOT_GOOD EQU *
0000D580  C4E7C2D9 40D5E340                         2148  DC CL48'DXBR NT NF -inf/-inf'
0000D5B0  7FFF8000 00000000                         2149  DC XL16'7FFF8000000000000000000000000000'
0000D5C0  C4E7C2D9 40E39940                         2150  DC CL48'DXBR Tr NF -inf/-inf'
0000D5F0  FFFF0000 00000000                         2151  DC XL16'FFFF0000000000000000000000000000'
0000D600  C4E7C2D9 40D5E340                         2152  DC CL48'DXBR NT NF -inf/-2'
0000D630  7FFF0000 00000000                         2153  DC XL16'7FFF0000000000000000000000000000'
0000D640  C4E7C2D9 40E39940                         2154  DC CL48'DXBR Tr NF -inf/-2'
0000D670  7FFF0000 00000000                         2155  DC XL16'7FFF0000000000000000000000000000'
0000D680  C4E7C2D9 40D5E340                         2156  DC CL48'DXBR NT NF -inf/-0'
0000D6B0  7FFF0000 00000000                         2157  DC XL16'7FFF0000000000000000000000000000'
0000D6C0  C4E7C2D9 40E39940                         2158  DC CL48'DXBR Tr NF -inf/-0'
0000D6F0  7FFF0000 00000000                         2159  DC XL16'7FFF0000000000000000000000000000'
0000D700  C4E7C2D9 40D5E340                         2160  DC CL48'DXBR NT NF -inf/+0'
0000D730  FFFF0000 00000000                         2161  DC XL16'FFFF0000000000000000000000000000'
0000D740  C4E7C2D9 40E39940                         2162  DC CL48'DXBR Tr NF -inf/+0'
0000D770  FFFF0000 00000000                         2163  DC XL16'FFFF0000000000000000000000000000'
0000D780  C4E7C2D9 40D5E340                         2164  DC CL48'DXBR NT NF -inf/+2'
0000D7B0  FFFF0000 00000000                         2165  DC XL16'FFFF0000000000000000000000000000'
0000D7C0  C4E7C2D9 40E39940                         2166  DC CL48'DXBR Tr NF -inf/+2'
0000D7F0  FFFF0000 00000000                         2167  DC XL16'FFFF0000000000000000000000000000'
0000D800  C4E7C2D9 40D5E340                         2168  DC CL48'DXBR NT NF -inf/+inf'
0000D830  7FFF8000 00000000                         2169  DC XL16'7FFF8000000000000000000000000000'
0000D840  C4E7C2D9 40E39940                         2170  DC CL48'DXBR Tr NF -inf/+inf'
0000D870  FFFF0000 00000000                         2171  DC XL16'FFFF0000000000000000000000000000'
0000D880  C4E7C2D9 40D5E340                         2172  DC CL48'DXBR NT NF -inf/-QNaN'
0000D8B0  FFFF8B00 00000000                         2173  DC XL16'FFFF8B000000000000000000000000'
0000D8C0  C4E7C2D9 40E39940                         2174  DC CL48'DXBR Tr NF -inf/-QNaN'
0000D8F0  FFFF8B00 00000000                         2175  DC XL16'FFFF8B000000000000000000000000'
0000D900  C4E7C2D9 40D5E340                         2176  DC CL48'DXBR NT NF -inf/+SNaN'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000D930  7FFF8A00 00000000                         2177  DC XL16'7FFF8A000000000000000000000000'
0000D940  C4E7C2D9 40E39940                         2178  DC CL48'DXBR Tr NF -inf/+SNaN'
0000D970  FFFF0000 00000000                         2179  DC XL16'FFFF0000000000000000000000000000'
0000D980  C4E7C2D9 40D5E340                         2180  DC CL48'DXBR NT NF -2/-inf'
0000D9B0  00000000 00000000                         2181  DC XL16'00000000000000000000000000000000'
0000D9C0  C4E7C2D9 40E39940                         2182  DC CL48'DXBR Tr NF -2/-inf'
0000D9F0  00000000 00000000                         2183  DC XL16'00000000000000000000000000000000'
0000DA00  C4E7C2D9 40D5E340                         2184  DC CL48'DXBR NT NF -2/-2'
0000DA30  3FFF0000 00000000                         2185  DC XL16'3FFF0000000000000000000000000000'
0000DA40  C4E7C2D9 40E39940                         2186  DC CL48'DXBR Tr NF -2/-2'
0000DA70  3FFF0000 00000000                         2187  DC XL16'3FFF0000000000000000000000000000'
0000DA80  C4E7C2D9 40D5E340                         2188  DC CL48'DXBR NT NF -2/-0'
0000DAB0  7FFF0000 00000000                         2189  DC XL16'7FFF0000000000000000000000000000'
0000DAC0  C4E7C2D9 40E39940                         2190  DC CL48'DXBR Tr NF -2/-0'
0000DAF0  C0000000 00000000                         2191  DC XL16'C0000000000000000000000000000000'
0000DB00  C4E7C2D9 40D5E340                         2192  DC CL48'DXBR NT NF -2/+0'
0000DB30  FFFF0000 00000000                         2193  DC XL16'FFFF0000000000000000000000000000'
0000DB40  C4E7C2D9 40E39940                         2194  DC CL48'DXBR Tr NF -2/+0'
0000DB70  C0000000 00000000                         2195  DC XL16'C0000000000000000000000000000000'
0000DB80  C4E7C2D9 40D5E340                         2196  DC CL48'DXBR NT NF -2/+2'
0000DBB0  BFFF0000 00000000                         2197  DC XL16'BFFF0000000000000000000000000000'
0000DBC0  C4E7C2D9 40E39940                         2198  DC CL48'DXBR Tr NF -2/+2'
0000DBF0  BFFF0000 00000000                         2199  DC XL16'BFFF0000000000000000000000000000'
0000DC00  C4E7C2D9 40D5E340                         2200  DC CL48'DXBR NT NF -2/+inf'
0000DC30  80000000 00000000                         2201  DC XL16'80000000000000000000000000000000'
0000DC40  C4E7C2D9 40E39940                         2202  DC CL48'DXBR Tr NF -2/+inf'
0000DC70  80000000 00000000                         2203  DC XL16'80000000000000000000000000000000'
0000DC80  C4E7C2D9 40D5E340                         2204  DC CL48'DXBR NT NF -2/-QNaN'
0000DCB0  FFFF8B00 00000000                         2205  DC XL16'FFFF8B000000000000000000000000'
0000DCC0  C4E7C2D9 40E39940                         2206  DC CL48'DXBR Tr NF -2/-QNaN'
0000DCF0  FFFF8B00 00000000                         2207  DC XL16'FFFF8B000000000000000000000000'
0000DD00  C4E7C2D9 40D5E340                         2208  DC CL48'DXBR NT NF -2/+SNaN'
0000DD30  7FFF8A00 00000000                         2209  DC XL16'7FFF8A000000000000000000000000'
0000DD40  C4E7C2D9 40E39940                         2210  DC CL48'DXBR Tr NF -2/+SNaN'
0000DD70  C0000000 00000000                         2211  DC XL16'C0000000000000000000000000000000'
0000DD80  C4E7C2D9 40D5E340                         2212  DC CL48'DXBR NT NF -0/-inf'
0000DDB0  00000000 00000000                         2213  DC XL16'00000000000000000000000000000000'
0000DDC0  C4E7C2D9 40E39940                         2214  DC CL48'DXBR Tr NF -0/-inf'
0000DDF0  00000000 00000000                         2215  DC XL16'00000000000000000000000000000000'
0000DE00  C4E7C2D9 40D5E340                         2216  DC CL48'DXBR NT NF -0/-2'
0000DE30  00000000 00000000                         2217  DC XL16'00000000000000000000000000000000'
0000DE40  C4E7C2D9 40E39940                         2218  DC CL48'DXBR Tr NF -0/-2'
0000DE70  00000000 00000000                         2219  DC XL16'00000000000000000000000000000000'
0000DE80  C4E7C2D9 40D5E340                         2220  DC CL48'DXBR NT NF -0/-0'
0000DEB0  7FFF8000 00000000                         2221  DC XL16'7FFF8000000000000000000000000000'
0000DEC0  C4E7C2D9 40E39940                         2222  DC CL48'DXBR Tr NF -0/-0'
0000DEF0  80000000 00000000                         2223  DC XL16'80000000000000000000000000000000'
0000DF00  C4E7C2D9 40D5E340                         2224  DC CL48'DXBR NT NF -0/+0'
0000DF30  7FFF8000 00000000                         2225  DC XL16'7FFF8000000000000000000000000000'
0000DF40  C4E7C2D9 40E39940                         2226  DC CL48'DXBR Tr NF -0/+0'
0000DF70  80000000 00000000                         2227  DC XL16'80000000000000000000000000000000'
0000DF80  C4E7C2D9 40D5E340                         2228  DC CL48'DXBR NT NF -0/+2'
0000DFB0  80000000 00000000                         2229  DC XL16'80000000000000000000000000000000'
0000DFC0  C4E7C2D9 40E39940                         2230  DC CL48'DXBR Tr NF -0/+2'
0000DFF0  80000000 00000000                         2231  DC XL16'80000000000000000000000000000000'
0000E000  C4E7C2D9 40D5E340                         2232  DC CL48'DXBR NT NF -0/+inf'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000E030  80000000 00000000                       2233  DC XL16'80000000000000000000000000000000'
0000E040  C4E7C2D9 40E39940                       2234  DC CL48'DXBR Tr NF -0/+inf'
0000E070  80000000 00000000                       2235  DC XL16'80000000000000000000000000000000'
0000E080  C4E7C2D9 40D5E340                       2236  DC CL48'DXBR NT NF -0/-QNaN'
0000E0B0  FFFF8B00 00000000                       2237  DC XL16'FFFF8B000000000000000000000000'
0000E0C0  C4E7C2D9 40E39940                       2238  DC CL48'DXBR Tr NF -0/-QNaN'
0000E0F0  FFFF8B00 00000000                       2239  DC XL16'FFFF8B000000000000000000000000'
0000E100  C4E7C2D9 40D5E340                       2240  DC CL48'DXBR NT NF -0/+SNaN'
0000E130  7FFF8A00 00000000                       2241  DC XL16'7FFF8A000000000000000000000000'
0000E140  C4E7C2D9 40E39940                       2242  DC CL48'DXBR Tr NF -0/+SNaN'
0000E170  80000000 00000000                       2243  DC XL16'80000000000000000000000000000000'
0000E180  C4E7C2D9 40D5E340                       2244  DC CL48'DXBR NT NF +0/-inf'
0000E1B0  80000000 00000000                       2245  DC XL16'80000000000000000000000000000000'
0000E1C0  C4E7C2D9 40E39940                       2246  DC CL48'DXBR Tr NF +0/-inf'
0000E1F0  80000000 00000000                       2247  DC XL16'80000000000000000000000000000000'
0000E200  C4E7C2D9 40D5E340                       2248  DC CL48'DXBR NT NF +0/-2'
0000E230  80000000 00000000                       2249  DC XL16'80000000000000000000000000000000'
0000E240  C4E7C2D9 40E39940                       2250  DC CL48'DXBR Tr NF +0/-2'
0000E270  80000000 00000000                       2251  DC XL16'80000000000000000000000000000000'
0000E280  C4E7C2D9 40D5E340                       2252  DC CL48'DXBR NT NF +0/-0'
0000E2B0  7FFF8000 00000000                       2253  DC XL16'7FFF8000000000000000000000000000'
0000E2C0  C4E7C2D9 40E39940                       2254  DC CL48'DXBR Tr NF +0/-0'
0000E2F0  00000000 00000000                       2255  DC XL16'00000000000000000000000000000000'
0000E300  C4E7C2D9 40D5E340                       2256  DC CL48'DXBR NT NF +0/+0'
0000E330  7FFF8000 00000000                       2257  DC XL16'7FFF8000000000000000000000000000'
0000E340  C4E7C2D9 40E39940                       2258  DC CL48'DXBR Tr NF +0/+0'
0000E370  00000000 00000000                       2259  DC XL16'00000000000000000000000000000000'
0000E380  C4E7C2D9 40D5E340                       2260  DC CL48'DXBR NT NF +0/+2'
0000E3B0  00000000 00000000                       2261  DC XL16'00000000000000000000000000000000'
0000E3C0  C4E7C2D9 40E39940                       2262  DC CL48'DXBR Tr NF +0/+2'
0000E3F0  00000000 00000000                       2263  DC XL16'00000000000000000000000000000000'
0000E400  C4E7C2D9 40D5E340                       2264  DC CL48'DXBR NT NF +0/+inf'
0000E430  00000000 00000000                       2265  DC XL16'00000000000000000000000000000000'
0000E440  C4E7C2D9 40E39940                       2266  DC CL48'DXBR Tr NF +0/+inf'
0000E470  00000000 00000000                       2267  DC XL16'00000000000000000000000000000000'
0000E480  C4E7C2D9 40D5E340                       2268  DC CL48'DXBR NT NF +0/-QNaN'
0000E4B0  FFFF8B00 00000000                       2269  DC XL16'FFFF8B000000000000000000000000'
0000E4C0  C4E7C2D9 40E39940                       2270  DC CL48'DXBR Tr NF +0/-QNaN'
0000E4F0  FFFF8B00 00000000                       2271  DC XL16'FFFF8B000000000000000000000000'
0000E500  C4E7C2D9 40D5E340                       2272  DC CL48'DXBR NT NF +0/+SNaN'
0000E530  7FFF8A00 00000000                       2273  DC XL16'7FFF8A000000000000000000000000'
0000E540  C4E7C2D9 40E39940                       2274  DC CL48'DXBR Tr NF +0/+SNaN'
0000E570  00000000 00000000                       2275  DC XL16'00000000000000000000000000000000'
0000E580  C4E7C2D9 40D5E340                       2276  DC CL48'DXBR NT NF +2/-inf'
0000E5B0  80000000 00000000                       2277  DC XL16'80000000000000000000000000000000'
0000E5C0  C4E7C2D9 40E39940                       2278  DC CL48'DXBR Tr NF +2/-inf'
0000E5F0  80000000 00000000                       2279  DC XL16'80000000000000000000000000000000'
0000E600  C4E7C2D9 40D5E340                       2280  DC CL48'DXBR NT NF +2/-2'
0000E630  BFFF0000 00000000                       2281  DC XL16'BFFF0000000000000000000000000000'
0000E640  C4E7C2D9 40E39940                       2282  DC CL48'DXBR Tr NF +2/-2'
0000E670  BFFF0000 00000000                       2283  DC XL16'BFFF0000000000000000000000000000'
0000E680  C4E7C2D9 40D5E340                       2284  DC CL48'DXBR NT NF +2/-0'
0000E6B0  FFFF0000 00000000                       2285  DC XL16'FFFF0000000000000000000000000000'
0000E6C0  C4E7C2D9 40E39940                       2286  DC CL48'DXBR Tr NF +2/-0'
0000E6F0  40000000 00000000                       2287  DC XL16'40000000000000000000000000000000'
0000E700  C4E7C2D9 40D5E340                       2288  DC CL48'DXBR NT NF +2/+0'
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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000E730  7FFF0000 00000000                         2289  DC XL16'7FFF0000000000000000000000000000'
0000E740  C4E7C2D9 40E39940                         2290  DC CL48'DXBR Tr NF +2/+0'
0000E770  40000000 00000000                         2291  DC XL16'40000000000000000000000000000000'
0000E780  C4E7C2D9 40D5E340                         2292  DC CL48'DXBR NT NF +2/+2'
0000E7B0  3FFF0000 00000000                         2293  DC XL16'3FFF0000000000000000000000000000'
0000E7C0  C4E7C2D9 40E39940                         2294  DC CL48'DXBR Tr NF +2/+2'
0000E7F0  3FFF0000 00000000                         2295  DC XL16'3FFF0000000000000000000000000000'
0000E800  C4E7C2D9 40D5E340                         2296  DC CL48'DXBR NT NF +2/+inf'
0000E830  00000000 00000000                         2297  DC XL16'00000000000000000000000000000000'
0000E840  C4E7C2D9 40E39940                         2298  DC CL48'DXBR Tr NF +2/+inf'
0000E870  00000000 00000000                         2299  DC XL16'00000000000000000000000000000000'
0000E880  C4E7C2D9 40D5E340                         2300  DC CL48'DXBR NT NF +2/-QNaN'
0000E8B0  FFFF8B00 00000000                         2301  DC XL16'FFFF8B0000000000000000000000000'
0000E8C0  C4E7C2D9 40E39940                         2302  DC CL48'DXBR Tr NF +2/-QNaN'
0000E8F0  FFFF8B00 00000000                         2303  DC XL16'FFFF8B0000000000000000000000000'
0000E900  C4E7C2D9 40D5E340                         2304  DC CL48'DXBR NT NF +2/+SNaN'
0000E930  7FFF8A00 00000000                         2305  DC XL16'7FFF8A0000000000000000000000000'
0000E940  C4E7C2D9 40E39940                         2306  DC CL48'DXBR Tr NF +2/+SNaN'
0000E970  40000000 00000000                         2307  DC XL16'40000000000000000000000000000000'
0000E980  C4E7C2D9 40D5E340                         2308  DC CL48'DXBR NT NF +inf/-inf'
0000E9B0  7FFF8000 00000000                         2309  DC XL16'7FFF8000000000000000000000000000'
0000E9C0  C4E7C2D9 40E39940                         2310  DC CL48'DXBR Tr NF +inf/-inf'
0000E9F0  7FFF0000 00000000                         2311  DC XL16'7FFF0000000000000000000000000000'
0000EA00  C4E7C2D9 40D5E340                         2312  DC CL48'DXBR NT NF +inf/-2'
0000EA30  FFFF0000 00000000                         2313  DC XL16'FFFF0000000000000000000000000000'
0000EA40  C4E7C2D9 40E39940                         2314  DC CL48'DXBR Tr NF +inf/-2'
0000EA70  FFFF0000 00000000                         2315  DC XL16'FFFF0000000000000000000000000000'
0000EA80  C4E7C2D9 40D5E340                         2316  DC CL48'DXBR NT NF +inf/-0'
0000EAB0  FFFF0000 00000000                         2317  DC XL16'FFFF0000000000000000000000000000'
0000EAC0  C4E7C2D9 40E39940                         2318  DC CL48'DXBR Tr NF +inf/-0'
0000EAF0  FFFF0000 00000000                         2319  DC XL16'FFFF0000000000000000000000000000'
0000EB00  C4E7C2D9 40D5E340                         2320  DC CL48'DXBR NT NF +inf/+0'
0000EB30  7FFF0000 00000000                         2321  DC XL16'7FFF0000000000000000000000000000'
0000EB40  C4E7C2D9 40E39940                         2322  DC CL48'DXBR Tr NF +inf/+0'
0000EB70  7FFF0000 00000000                         2323  DC XL16'7FFF0000000000000000000000000000'
0000EB80  C4E7C2D9 40D5E340                         2324  DC CL48'DXBR NT NF +inf/+2'
0000EBB0  7FFF0000 00000000                         2325  DC XL16'7FFF0000000000000000000000000000'
0000EBC0  C4E7C2D9 40E39940                         2326  DC CL48'DXBR Tr NF +inf/+2'
0000EBF0  7FFF0000 00000000                         2327  DC XL16'7FFF0000000000000000000000000000'
0000EC00  C4E7C2D9 40D5E340                         2328  DC CL48'DXBR NT NF +inf/+inf'
0000EC30  7FFF8000 00000000                         2329  DC XL16'7FFF8000000000000000000000000000'
0000EC40  C4E7C2D9 40E39940                         2330  DC CL48'DXBR Tr NF +inf/+inf'
0000EC70  7FFF0000 00000000                         2331  DC XL16'7FFF0000000000000000000000000000'
0000EC80  C4E7C2D9 40D5E340                         2332  DC CL48'DXBR NT NF +inf/-QNaN'
0000ECB0  FFFF8B00 00000000                         2333  DC XL16'FFFF8B0000000000000000000000000'
0000ECC0  C4E7C2D9 40E39940                         2334  DC CL48'DXBR Tr NF +inf/-QNaN'
0000ECF0  FFFF8B00 00000000                         2335  DC XL16'FFFF8B0000000000000000000000000'
0000ED00  C4E7C2D9 40D5E340                         2336  DC CL48'DXBR NT NF +inf/+SNaN'
0000ED30  7FFF8A00 00000000                         2337  DC XL16'7FFF8A0000000000000000000000000'
0000ED40  C4E7C2D9 40E39940                         2338  DC CL48'DXBR Tr NF +inf/+SNaN'
0000ED70  7FFF0000 00000000                         2339  DC XL16'7FFF0000000000000000000000000000'
0000ED80  C4E7C2D9 40D5E340                         2340  DC CL48'DXBR NT NF -QNaN/-inf'
0000EDB0  FFFF8B00 00000000                         2341  DC XL16'FFFF8B0000000000000000000000000'
0000EDC0  C4E7C2D9 40E39940                         2342  DC CL48'DXBR Tr NF -QNaN/-inf'
0000EDF0  FFFF8B00 00000000                         2343  DC XL16'FFFF8B0000000000000000000000000'
0000EE00  C4E7C2D9 40D5E340                         2344  DC CL48'DXBR NT NF -QNaN/-2'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000EE30  FFFF8B00 00000000                         2345  DC XL16'FFFF8B0000000000000000000000000000'
0000EE40  C4E7C2D9 40E39940                         2346  DC CL48'DXBR Tr NF -QNaN/-2'
0000EE70  FFFF8B00 00000000                         2347  DC XL16'FFFF8B0000000000000000000000000000'
0000EE80  C4E7C2D9 40D5E340                         2348  DC CL48'DXBR NT NF -QNaN/-0'
0000EEB0  FFFF8B00 00000000                         2349  DC XL16'FFFF8B0000000000000000000000000000'
0000EEC0  C4E7C2D9 40E39940                         2350  DC CL48'DXBR Tr NF -QNaN/-0'
0000EEF0  FFFF8B00 00000000                         2351  DC XL16'FFFF8B0000000000000000000000000000'
0000EF00  C4E7C2D9 40D5E340                         2352  DC CL48'DXBR NT NF -QNaN/+0'
0000EF30  FFFF8B00 00000000                         2353  DC XL16'FFFF8B0000000000000000000000000000'
0000EF40  C4E7C2D9 40E39940                         2354  DC CL48'DXBR Tr NF -QNaN/+0'
0000EF70  FFFF8B00 00000000                         2355  DC XL16'FFFF8B0000000000000000000000000000'
0000EF80  C4E7C2D9 40D5E340                         2356  DC CL48'DXBR NT NF -QNaN/+2'
0000EFB0  FFFF8B00 00000000                         2357  DC XL16'FFFF8B0000000000000000000000000000'
0000EFC0  C4E7C2D9 40E39940                         2358  DC CL48'DXBR Tr NF -QNaN/+2'
0000EFF0  FFFF8B00 00000000                         2359  DC XL16'FFFF8B0000000000000000000000000000'
0000F000  C4E7C2D9 40D5E340                         2360  DC CL48'DXBR NT NF -QNaN/+inf'
0000F030  FFFF8B00 00000000                         2361  DC XL16'FFFF8B0000000000000000000000000000'
0000F040  C4E7C2D9 40E39940                         2362  DC CL48'DXBR Tr NF -QNaN/+inf'
0000F070  FFFF8B00 00000000                         2363  DC XL16'FFFF8B0000000000000000000000000000'
0000F080  C4E7C2D9 40D5E340                         2364  DC CL48'DXBR NT NF -QNaN/-QNaN'
0000F0B0  FFFF8B00 00000000                         2365  DC XL16'FFFF8B0000000000000000000000000000'
0000F0C0  C4E7C2D9 40E39940                         2366  DC CL48'DXBR Tr NF -QNaN/-QNaN'
0000F0F0  FFFF8B00 00000000                         2367  DC XL16'FFFF8B0000000000000000000000000000'
0000F100  C4E7C2D9 40D5E340                         2368  DC CL48'DXBR NT NF -QNaN/+SNaN'
0000F130  7FFF8A00 00000000                         2369  DC XL16'7FFF8A0000000000000000000000000000'
0000F140  C4E7C2D9 40E39940                         2370  DC CL48'DXBR Tr NF -QNaN/+SNaN'
0000F170  FFFF8B00 00000000                         2371  DC XL16'FFFF8B0000000000000000000000000000'
0000F180  C4E7C2D9 40D5E340                         2372  DC CL48'DXBR NT NF +SNaN/-inf'
0000F1B0  7FFF8A00 00000000                         2373  DC XL16'7FFF8A0000000000000000000000000000'
0000F1C0  C4E7C2D9 40E39940                         2374  DC CL48'DXBR Tr NF +SNaN/-inf'
0000F1F0  7FFF0A00 00000000                         2375  DC XL16'7FFF0A0000000000000000000000000000'
0000F200  C4E7C2D9 40D5E340                         2376  DC CL48'DXBR NT NF +SNaN/-2'
0000F230  7FFF8A00 00000000                         2377  DC XL16'7FFF8A0000000000000000000000000000'
0000F240  C4E7C2D9 40E39940                         2378  DC CL48'DXBR Tr NF +SNaN/-2'
0000F270  7FFF0A00 00000000                         2379  DC XL16'7FFF0A0000000000000000000000000000'
0000F280  C4E7C2D9 40D5E340                         2380  DC CL48'DXBR NT NF +SNaN/-0'
0000F2B0  7FFF8A00 00000000                         2381  DC XL16'7FFF8A0000000000000000000000000000'
0000F2C0  C4E7C2D9 40E39940                         2382  DC CL48'DXBR Tr NF +SNaN/-0'
0000F2F0  7FFF0A00 00000000                         2383  DC XL16'7FFF0A0000000000000000000000000000'
0000F300  C4E7C2D9 40D5E340                         2384  DC CL48'DXBR NT NF +SNaN/+0'
0000F330  7FFF8A00 00000000                         2385  DC XL16'7FFF8A0000000000000000000000000000'
0000F340  C4E7C2D9 40E39940                         2386  DC CL48'DXBR Tr NF +SNaN/+0'
0000F370  7FFF0A00 00000000                         2387  DC XL16'7FFF0A0000000000000000000000000000'
0000F380  C4E7C2D9 40D5E340                         2388  DC CL48'DXBR NT NF +SNaN/+2'
0000F3B0  7FFF8A00 00000000                         2389  DC XL16'7FFF8A0000000000000000000000000000'
0000F3C0  C4E7C2D9 40E39940                         2390  DC CL48'DXBR Tr NF +SNaN/+2'
0000F3F0  7FFF0A00 00000000                         2391  DC XL16'7FFF0A0000000000000000000000000000'
0000F400  C4E7C2D9 40D5E340                         2392  DC CL48'DXBR NT NF +SNaN/+inf'
0000F430  7FFF8A00 00000000                         2393  DC XL16'7FFF8A0000000000000000000000000000'
0000F440  C4E7C2D9 40E39940                         2394  DC CL48'DXBR Tr NF +SNaN/+inf'
0000F470  7FFF0A00 00000000                         2395  DC XL16'7FFF0A0000000000000000000000000000'
0000F480  C4E7C2D9 40D5E340                         2396  DC CL48'DXBR NT NF +SNaN/-QNaN'
0000F4B0  7FFF8A00 00000000                         2397  DC XL16'7FFF8A0000000000000000000000000000'
0000F4C0  C4E7C2D9 40E39940                         2398  DC CL48'DXBR Tr NF +SNaN/-QNaN'
0000F4F0  7FFF0A00 00000000                         2399  DC XL16'7FFF0A0000000000000000000000000000'
0000F500  C4E7C2D9 40D5E340                         2400  DC CL48'DXBR NT NF +SNaN/+SNaN'
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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000F530  7FFF8A00 00000000                       2401  DC XL16'7FFF8A000000000000000000000000'
0000F540  C4E7C2D9 40E39940                       2402  DC CL48'DXBR Tr NF +SNaN/+SNaN'
0000F570  7FFF0A00 00000000                       2403  DC XL16'7FFF0A000000000000000000000000'
                             00000080  00000001   2404 XBFPNFOT_NUM EQU (*-XBFPNFOT_GOOD)/64
                                                 2405 *
                                                 2406 *
                             0000F580  00000001   2407 XBFPNFFL_GOOD EQU *
0000F580  C4E7C2D9 40D5C640                       2408  DC CL48'DXBR NF -inf/-inf FPCR'
0000F5B0  00800000 F8008000                       2409  DC XL16'00800000F800800000000000000000'
0000F5C0  C4E7C2D9 40D5C640                       2410  DC CL48'DXBR NF -inf/-2 FPCR'
0000F5F0  00000000 F8000000                       2411  DC XL16'00000000F800000000000000000000'
0000F600  C4E7C2D9 40D5C640                       2412  DC CL48'DXBR NF -inf/-0 FPCR'
0000F630  00000000 F8000000                       2413  DC XL16'00000000F800000000000000000000'
0000F640  C4E7C2D9 40D5C640                       2414  DC CL48'DXBR NF -inf/+0 FPCR'
0000F670  00000000 F8000000                       2415  DC XL16'00000000F800000000000000000000'
0000F680  C4E7C2D9 40D5C640                       2416  DC CL48'DXBR NF -inf/+2 FPCR'
0000F6B0  00000000 F8000000                       2417  DC XL16'00000000F800000000000000000000'
0000F6C0  C4E7C2D9 40D5C640                       2418  DC CL48'DXBR NF -inf/+inf FPCR'
0000F6F0  00800000 F8008000                       2419  DC XL16'00800000F800800000000000000000'
0000F700  C4E7C2D9 40D5C640                       2420  DC CL48'DXBR NF -inf/-QNaN FPCR'
0000F730  00000000 F8000000                       2421  DC XL16'00000000F800000000000000000000'
0000F740  C4E7C2D9 40D5C640                       2422  DC CL48'DXBR NF -inf/+SNaN FPCR'
0000F770  00800000 F8008000                       2423  DC XL16'00800000F800800000000000000000'
0000F780  C4E7C2D9 40D5C640                       2424  DC CL48'DXBR NF -2/-inf FPCR'
0000F7B0  00000000 F8000000                       2425  DC XL16'00000000F800000000000000000000'
0000F7C0  C4E7C2D9 40D5C640                       2426  DC CL48'DXBR NF -2/-2 FPCR'
0000F7F0  00000000 F8000000                       2427  DC XL16'00000000F800000000000000000000'
0000F800  C4E7C2D9 40D5C640                       2428  DC CL48'DXBR NF -2/-0 FPCR'
0000F830  00400000 F8004000                       2429  DC XL16'00400000F800400000000000000000'
0000F840  C4E7C2D9 40D5C640                       2430  DC CL48'DXBR NF -2/+0 FPCR'
0000F870  00400000 F8004000                       2431  DC XL16'00400000F800400000000000000000'
0000F880  C4E7C2D9 40D5C640                       2432  DC CL48'DXBR NF -2/+2 FPCR'
0000F8B0  00000000 F8000000                       2433  DC XL16'00000000F800000000000000000000'
0000F8C0  C4E7C2D9 40D5C640                       2434  DC CL48'DXBR NF -2/+inf FPCR'
0000F8F0  00000000 F8000000                       2435  DC XL16'00000000F800000000000000000000'
0000F900  C4E7C2D9 40D5C640                       2436  DC CL48'DXBR NF -2/-QNaN FPCR'
0000F930  00000000 F8000000                       2437  DC XL16'00000000F800000000000000000000'
0000F940  C4E7C2D9 40D5C640                       2438  DC CL48'DXBR NF -2/+SNaN FPCR'
0000F970  00800000 F8008000                       2439  DC XL16'00800000F800800000000000000000'
0000F980  C4E7C2D9 40D5C640                       2440  DC CL48'DXBR NF -0/-inf FPCR'
0000F9B0  00000000 F8000000                       2441  DC XL16'00000000F800000000000000000000'
0000F9C0  C4E7C2D9 40D5C640                       2442  DC CL48'DXBR NF -0/-2 FPCR'
0000F9F0  00000000 F8000000                       2443  DC XL16'00000000F800000000000000000000'
0000FA00  C4E7C2D9 40D5C640                       2444  DC CL48'DXBR NF -0/-0 FPCR'
0000FA30  00800000 F8008000                       2445  DC XL16'00800000F800800000000000000000'
0000FA40  C4E7C2D9 40D5C640                       2446  DC CL48'DXBR NF -0/+0 FPCR'
0000FA70  00800000 F8008000                       2447  DC XL16'00800000F800800000000000000000'
0000FA80  C4E7C2D9 40D5C640                       2448  DC CL48'DXBR NF -0/+2 FPCR'
0000FAB0  00000000 F8000000                       2449  DC XL16'00000000F800000000000000000000'
0000FAC0  C4E7C2D9 40D5C640                       2450  DC CL48'DXBR NF -0/+inf FPCR'
0000FAF0  00000000 F8000000                       2451  DC XL16'00000000F800000000000000000000'
0000FB00  C4E7C2D9 40D5C640                       2452  DC CL48'DXBR NF -0/-QNaN FPCR'
0000FB30  00000000 F8000000                       2453  DC XL16'00000000F800000000000000000000'
0000FB40  C4E7C2D9 40D5C640                       2454  DC CL48'DXBR NF -0/+SNaN FPCR'
0000FB70  00800000 F8008000                       2455  DC XL16'00800000F800800000000000000000'
0000FB80  C4E7C2D9 40D5C640                       2456  DC CL48'DXBR NF +0/-inf FPCR'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

0000FBB0  00000000 F8000000                         2457  DC XL16'00000000F8000000000000000000000000'
0000FBC0  C4E7C2D9 40D5C640                         2458  DC CL48'DXBR NF +0/-2 FPCR'
0000FBF0  00000000 F8000000                         2459  DC XL16'00000000F8000000000000000000000000'
0000FC00  C4E7C2D9 40D5C640                         2460  DC CL48'DXBR NF +0/-0 FPCR'
0000FC30  00800000 F8008000                         2461  DC XL16'00800000F8008000000000000000000000'
0000FC40  C4E7C2D9 40D5C640                         2462  DC CL48'DXBR NF +0/+0 FPCR'
0000FC70  00800000 F8008000                         2463  DC XL16'00800000F8008000000000000000000000'
0000FC80  C4E7C2D9 40D5C640                         2464  DC CL48'DXBR NF +0/+2 FPCR'
0000FCB0  00000000 F8000000                         2465  DC XL16'00000000F8000000000000000000000000'
0000FCC0  C4E7C2D9 40D5C640                         2466  DC CL48'DXBR NF +0/+inf FPCR'
0000FCF0  00000000 F8000000                         2467  DC XL16'00000000F8000000000000000000000000'
0000FD00  C4E7C2D9 40D5C640                         2468  DC CL48'DXBR NF +0/-QNaN FPCR'
0000FD30  00000000 F8000000                         2469  DC XL16'00000000F8000000000000000000000000'
0000FD40  C4E7C2D9 40D5C640                         2470  DC CL48'DXBR NF +0/+SNaN FPCR'
0000FD70  00800000 F8008000                         2471  DC XL16'00800000F8008000000000000000000000'
0000FD80  C4E7C2D9 40D5C640                         2472  DC CL48'DXBR NF +2/-inf FPCR'
0000FDB0  00000000 F8000000                         2473  DC XL16'00000000F8000000000000000000000000'
0000FDC0  C4E7C2D9 40D5C640                         2474  DC CL48'DXBR NF +2/-2 FPCR'
0000FDF0  00000000 F8000000                         2475  DC XL16'00000000F8000000000000000000000000'
0000FE00  C4E7C2D9 40D5C640                         2476  DC CL48'DXBR NF +2/-0 FPCR'
0000FE30  00400000 F8004000                         2477  DC XL16'00400000F8004000000000000000000000'
0000FE40  C4E7C2D9 40D5C640                         2478  DC CL48'DXBR NF +2/+0 FPCR'
0000FE70  00400000 F8004000                         2479  DC XL16'00400000F8004000000000000000000000'
0000FE80  C4E7C2D9 40D5C640                         2480  DC CL48'DXBR NF +2/+2 FPCR'
0000FEB0  00000000 F8000000                         2481  DC XL16'00000000F8000000000000000000000000'
0000FEC0  C4E7C2D9 40D5C640                         2482  DC CL48'DXBR NF +2/+inf FPCR'
0000FEF0  00000000 F8000000                         2483  DC XL16'00000000F8000000000000000000000000'
0000FF00  C4E7C2D9 40D5C640                         2484  DC CL48'DXBR NF +2/-QNaN FPCR'
0000FF30  00000000 F8000000                         2485  DC XL16'00000000F8000000000000000000000000'
0000FF40  C4E7C2D9 40D5C640                         2486  DC CL48'DXBR NF +2/+SNaN FPCR'
0000FF70  00800000 F8008000                         2487  DC XL16'00800000F8008000000000000000000000'
0000FF80  C4E7C2D9 40D5C640                         2488  DC CL48'DXBR NF +inf/-inf FPCR'
0000FFB0  00800000 F8008000                         2489  DC XL16'00800000F8008000000000000000000000'
0000FFC0  C4E7C2D9 40D5C640                         2490  DC CL48'DXBR NF +inf/-2 FPCR'
0000FFF0  00000000 F8000000                         2491  DC XL16'00000000F8000000000000000000000000'
00010000  C4E7C2D9 40D5C640                         2492  DC CL48'DXBR NF +inf/-0 FPCR'
00010030  00000000 F8000000                         2493  DC XL16'00000000F8000000000000000000000000'
00010040  C4E7C2D9 40D5C640                         2494  DC CL48'DXBR NF +inf/+0 FPCR'
00010070  00000000 F8000000                         2495  DC XL16'00000000F8000000000000000000000000'
00010080  C4E7C2D9 40D5C640                         2496  DC CL48'DXBR NF +inf/+2 FPCR'
000100B0  00000000 F8000000                         2497  DC XL16'00000000F8000000000000000000000000'
000100C0  C4E7C2D9 40D5C640                         2498  DC CL48'DXBR NF +inf/+inf FPCR'
000100F0  00800000 F8008000                         2499  DC XL16'00800000F8008000000000000000000000'
00010100  C4E7C2D9 40D5C640                         2500  DC CL48'DXBR NF +inf/-QNaN FPCR'
00010130  00000000 F8000000                         2501  DC XL16'00000000F8000000000000000000000000'
00010140  C4E7C2D9 40D5C640                         2502  DC CL48'DXBR NF +inf/+SNaN FPCR'
00010170  00800000 F8008000                         2503  DC XL16'00800000F8008000000000000000000000'
00010180  C4E7C2D9 40D5C640                         2504  DC CL48'DXBR NF -QNaN/-inf FPCR'
000101B0  00000000 F8000000                         2505  DC XL16'00000000F8000000000000000000000000'
000101C0  C4E7C2D9 40D5C640                         2506  DC CL48'DXBR NF -QNaN/-2 FPCR'
000101F0  00000000 F8000000                         2507  DC XL16'00000000F8000000000000000000000000'
00010200  C4E7C2D9 40D5C640                         2508  DC CL48'DXBR NF -QNaN/-0 FPCR'
00010230  00000000 F8000000                         2509  DC XL16'00000000F8000000000000000000000000'
00010240  C4E7C2D9 40D5C640                         2510  DC CL48'DXBR NF -QNaN/+0 FPCR'
00010270  00000000 F8000000                         2511  DC XL16'00000000F8000000000000000000000000'
00010280  C4E7C2D9 40D5C640                         2512  DC CL48'DXBR NF -QNaN/+2 FPCR'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

000102B0  00000000 F8000000                        2513  DC XL16'00000000F8000000000000000000000000'
000102C0  C4E7C2D9 40D5C640                        2514  DC CL48'DXBR NF -QNaN/+inf FPCR'
000102F0  00000000 F8000000                        2515  DC XL16'00000000F8000000000000000000000000'
00010300  C4E7C2D9 40D5C640                        2516  DC CL48'DXBR NF -QNaN/-QNaN FPCR'
00010330  00000000 F8000000                        2517  DC XL16'00000000F8000000000000000000000000'
00010340  C4E7C2D9 40D5C640                        2518  DC CL48'DXBR NF -QNaN/+SNaN FPCR'
00010370  00800000 F8008000                        2519  DC XL16'00800000F8008000000000000000000000'
00010380  C4E7C2D9 40D5C640                        2520  DC CL48'DXBR NF +SNaN/-inf FPCR'
000103B0  00800000 F8008000                        2521  DC XL16'00800000F8008000000000000000000000'
000103C0  C4E7C2D9 40D5C640                        2522  DC CL48'DXBR NF +SNaN/-2 FPCR'
000103F0  00800000 F8008000                        2523  DC XL16'00800000F8008000000000000000000000'
00010400  C4E7C2D9 40D5C640                        2524  DC CL48'DXBR NF +SNaN/-0 FPCR'
00010430  00800000 F8008000                        2525  DC XL16'00800000F8008000000000000000000000'
00010440  C4E7C2D9 40D5C640                        2526  DC CL48'DXBR NF +SNaN/+0 FPCR'
00010470  00800000 F8008000                        2527  DC XL16'00800000F8008000000000000000000000'
00010480  C4E7C2D9 40D5C640                        2528  DC CL48'DXBR NF +SNaN/+2 FPCR'
000104B0  00800000 F8008000                        2529  DC XL16'00800000F8008000000000000000000000'
000104C0  C4E7C2D9 40D5C640                        2530  DC CL48'DXBR NF +SNaN/+inf FPCR'
000104F0  00800000 F8008000                        2531  DC XL16'00800000F8008000000000000000000000'
00010500  C4E7C2D9 40D5C640                        2532  DC CL48'DXBR NF +SNaN/-QNaN FPCR'
00010530  00800000 F8008000                        2533  DC XL16'00800000F8008000000000000000000000'
00010540  C4E7C2D9 40D5C640                        2534  DC CL48'DXBR NF +SNaN/+SNaN FPCR'
00010570  00800000 F8008000                        2535  DC XL16'00800000F8008000000000000000000000'
                            00000040  00000001   2536 XBFPNFFL_NUM EQU (*-XBFPNFFL_GOOD)/64
                                                 2537 *
                                                 2538 *
                            00010580  00000001   2539 XBFPOUT_GOOD EQU *
00010580  C4E7C2D9 40D5E340                        2540  DC CL48'DXBR NT max/min'
000105B0  7FFF0000 00000000                        2541  DC XL16'7FFF0000000000000000000000000000'
000105C0  C4E7C2D9 40E39940                        2542  DC CL48'DXBR Tr max/min'
000105F0  606CFFFF FFFFFFFF                        2543  DC XL16'606CFFFFFFFFFFFFFFFFFFFFFFFFFFFF'
00010600  C4E7C2D9 40D5E340                        2544  DC CL48'DXBR NT min/2.0'
00010630  00008000 00000000                        2545  DC XL16'00008000000000000000000000000000'
00010640  C4E7C2D9 40E39940                        2546  DC CL48'DXBR Tr min/2.0'
00010670  60000000 00000000                        2547  DC XL16'60000000000000000000000000000000'
00010680  C4E7C2D9 40D5E340                        2548  DC CL48'DXBR NT 1.0/10.0'
000106B0  3FFB9999 99999999                        2549  DC XL16'3FFB99999999999999999999999999A'
000106C0  C4E7C2D9 40E39940                        2550  DC CL48'DXBR Tr 1.0/10.0'
000106F0  3FFB9999 99999999                        2551  DC XL16'3FFB99999999999999999999999999A'
00010700  C4E7C2D9 40D5E340                        2552  DC CL48'DXBR NT 7.0/10.0'
00010730  3FFE6666 66666666                        2553  DC XL16'3FFE6666666666666666666666666666'
00010740  C4E7C2D9 40E39940                        2554  DC CL48'DXBR Tr 7.0/10.0'
00010770  3FFE6666 66666666                        2555  DC XL16'3FFE6666666666666666666666666666'
00010780  C4E7C2D9 40D5E340                        2556  DC CL48'DXBR NT 1.0/-10.0'
000107B0  BFFB9999 99999999                        2557  DC XL16'BFFB99999999999999999999999999A'
000107C0  C4E7C2D9 40E39940                        2558  DC CL48'DXBR Tr 1.0/-10.0'
000107F0  BFFB9999 99999999                        2559  DC XL16'BFFB99999999999999999999999999A'
00010800  C4E7C2D9 40D5E340                        2560  DC CL48'DXBR NT 7.0/-10.0'
00010830  BFFE6666 66666666                        2561  DC XL16'BFFE6666666666666666666666666666'
00010840  C4E7C2D9 40E39940                        2562  DC CL48'DXBR Tr 7.0/-10.0'
00010870  BFFE6666 66666666                        2563  DC XL16'BFFE6666666666666666666666666666'
                            0000000C  00000001   2564 XBFPOUT_NUM EQU (*-XBFPOUT_GOOD)/64
                                                 2565 *
                                                 2566 *
                            00010880  00000001   2567 XBFPFLGS_GOOD EQU *
00010880  C4E7C2D9 409481A7                        2568  DC CL48'DXBR max/min FPCR'
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

000108B0  00280000 F8002000                         2569  DC XL16'00280000F8002000000000000000000'
000108C0  C4E7C2D9 40948995                         2570  DC CL48'DXBR min/2.0 FPCR'
000108F0  00000000 F8001000                         2571  DC XL16'00000000F8001000000000000000000'
00010900  C4E7C2D9 40F14BF0                         2572  DC CL48'DXBR 1.0/10.0 FPCR'
00010930  00080000 F8000C00                         2573  DC XL16'00080000F8000C00000000000000000'
00010940  C4E7C2D9 40F74BF0                         2574  DC CL48'DXBR 7.0/10.0 FPCR'
00010970  00080000 F8000800                         2575  DC XL16'00080000F8000800000000000000000'
00010980  C4E7C2D9 40F14BF0                         2576  DC CL48'DXBR 1.0/-10.0 FPCR'
000109B0  00080000 F8000C00                         2577  DC XL16'00080000F8000C00000000000000000'
000109C0  C4E7C2D9 40F74BF0                         2578  DC CL48'DXBR 7.0/-10.0 FPCR'
000109F0  00080000 F8000800                         2579  DC XL16'00080000F8000800000000000000000'
                            00000006  00000001    2580 XBFPFLGS_NUM EQU (*-XBFPFLGS_GOOD)/64
                                                  2581 *
                                                  2582 *
                            00010A00  00000001    2583 XBFPRMO_GOOD EQU *
00010A00  C4E7C2D9 40D9D440                         2584  DC CL48'DXBR RM RNTE 1/10'
00010A30  3FFB9999 99999999                         2585  DC XL16'3FFB99999999999999999999999999A'
00010A40  C4E7C2D9 40D9D440                         2586  DC CL48'DXBR RM RZ 1/10'
00010A70  3FFB9999 99999999                         2587  DC XL16'3FFB99999999999999999999999999'
00010A80  C4E7C2D9 40D9D440                         2588  DC CL48'DXBR RM RP 1/10'
00010AB0  3FFB9999 99999999                         2589  DC XL16'3FFB99999999999999999999999999A'
00010AC0  C4E7C2D9 40D9D440                         2590  DC CL48'DXBR RM RM 1/10'
00010AF0  3FFB9999 99999999                         2591  DC XL16'3FFB99999999999999999999999999'
00010B00  C4E7C2D9 40D9D440                         2592  DC CL48'DXBR RM RFS 1/10'
00010B30  3FFB9999 99999999                         2593  DC XL16'3FFB99999999999999999999999999'
00010B40  C4E7C2D9 40D9D440                         2594  DC CL48'DXBR RM RNTE 7/10'
00010B70  3FFE6666 66666666                         2595  DC XL16'3FFE66666666666666666666666666'
00010B80  C4E7C2D9 40D9D440                         2596  DC CL48'DXBR RM RZ 7/10'
00010BB0  3FFE6666 66666666                         2597  DC XL16'3FFE66666666666666666666666666'
00010BC0  C4E7C2D9 40D9D440                         2598  DC CL48'DXBR RM RP 7/10'
00010BF0  3FFE6666 66666666                         2599  DC XL16'3FFE66666666666666666666666667'
00010C00  C4E7C2D9 40D9D440                         2600  DC CL48'DXBR RM RM 7/10'
00010C30  3FFE6666 66666666                         2601  DC XL16'3FFE66666666666666666666666666'
00010C40  C4E7C2D9 40D9D440                         2602  DC CL48'DXBR RM RFS 7/10'
00010C70  3FFE6666 66666666                         2603  DC XL16'3FFE66666666666666666666666667'
00010C80  C4E7C2D9 40D9D440                         2604  DC CL48'DXBR RM RNTE 1/-10'
00010CB0  BFFB9999 99999999                         2605  DC XL16'BFFB99999999999999999999999999A'
00010CC0  C4E7C2D9 40D9D440                         2606  DC CL48'DXBR RM RZ 1/-10'
00010CF0  BFFB9999 99999999                         2607  DC XL16'BFFB99999999999999999999999999'
00010D00  C4E7C2D9 40D9D440                         2608  DC CL48'DXBR RM RP 1/-10'
00010D30  BFFB9999 99999999                         2609  DC XL16'BFFB99999999999999999999999999'
00010D40  C4E7C2D9 40D9D440                         2610  DC CL48'DXBR RM RM 1/-10'
00010D70  BFFB9999 99999999                         2611  DC XL16'BFFB99999999999999999999999999A'
00010D80  C4E7C2D9 40D9D440                         2612  DC CL48'DXBR RM RFS 1/-10'
00010DB0  BFFB9999 99999999                         2613  DC XL16'BFFB99999999999999999999999999'
00010DC0  C4E7C2D9 40D9D440                         2614  DC CL48'DXBR RM RNTE 7/-10'
00010DF0  BFFE6666 66666666                         2615  DC XL16'BFFE66666666666666666666666666'
00010E00  C4E7C2D9 40D9D440                         2616  DC CL48'DXBR RM RZ 7/-10'
00010E30  BFFE6666 66666666                         2617  DC XL16'BFFE66666666666666666666666666'
00010E40  C4E7C2D9 40D9D440                         2618  DC CL48'DXBR RM RP 7/-10'
00010E70  BFFE6666 66666666                         2619  DC XL16'BFFE66666666666666666666666666'
00010E80  C4E7C2D9 40D9D440                         2620  DC CL48'DXBR RM RM 7/-10'
00010EB0  BFFE6666 66666666                         2621  DC XL16'BFFE66666666666666666666666667'
00010EC0  C4E7C2D9 40D9D440                         2622  DC CL48'DXBR RM RFS 7/-10'
00010EF0  BFFE6666 66666666                         2623  DC XL16'BFFE66666666666666666666666667'
                            00000014  00000001    2624 XBFPRMO_NUM EQU (*-XBFPRMO_GOOD)/64
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   2625 *
                                                   2626 *
                               00010F00  00000001  2627 XBFPRMOF_GOOD EQU *
00010F00  C4E7C2D9 40D9D440                        2628  DC CL48'DXBR RM RTNE,RZ,RP,RM 1/10 FPCR'
00010F30  00080000 00080001                        2629  DC XL16'00080000000800010008000200080003'
00010F40  C4E7C2D9 40D9D440                        2630  DC CL48'DXBR RM RFS 1/10 FPCR'
00010F70  00080007 00000000                        2631  DC XL16'00080007000000000000000000000000'
00010F80  C4E7C2D9 40D9D440                        2632  DC CL48'DXBR RM RTNE,RZ,RP,RM 7/10 FPCR'
00010FB0  00080000 00080001                        2633  DC XL16'00080000000800010008000200080003'
00010FC0  C4E7C2D9 40D9D440                        2634  DC CL48'DXBR RM RFS 7/10 FPCR'
00010FF0  00080007 00000000                        2635  DC XL16'00080007000000000000000000000000'
00011000  C4E7C2D9 40D9D440                        2636  DC CL48'DXBR RM RTNE,RZ,RP,RM 1/-10 FPCR'
00011030  00080000 00080001                        2637  DC XL16'00080000000800010008000200080003'
00011040  C4E7C2D9 40D9D440                        2638  DC CL48'DXBR RM RFS 1/-10 FPCR'
00011070  00080007 00000000                        2639  DC XL16'00080007000000000000000000000000'
00011080  C4E7C2D9 40D9D440                        2640  DC CL48'DXBR RM RTNE,RZ,RP,RM 7/-10 FPCR'
000110B0  00080000 00080001                        2641  DC XL16'00080000000800010008000200080003'
000110C0  C4E7C2D9 40D9D440                        2642  DC CL48'DXBR RM RFS 7/-10 FPCR'
000110F0  00080007 00000000                        2643  DC XL16'00080007000000000000000000000000'
                               00000008  00000001  2644 XBFPRMOF_NUM EQU (*-XBFPRMOF_GOOD)/64
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00011100                                            2646 HELPERS  DS    0H       (R12 base of helper subroutines)

                                                    2648 ************************************************************
                                                    2649 *                 REPORT UNEXPECTED PROGRAM CHECK
                                                    2650 ************************************************************

00011100                                            2652 PGMCK    DS    0H
00011100  F342 C072 F08E      00011172  0000008E    2653          UNPK  PROGCODE(L'PROGCODE+1),PCINTCD(L'PCINTCD+1)
00011106  926B C076                     00011176    2654          MVI   PGMCOMMA,C','
0001110A  DC03 C072 C178      00011172  00011278    2655          TR    PROGCODE,HEXTRTAB

00011110  F384 C07C F150      0001117C  00000150    2657          UNPK  PGMPSW+(0*9)(9),PCOLDPSW+(0*4)(5)
00011116  9240 C084                     00011184    2658          MVI   PGMPSW+(0*9)+8,C' '
0001111A  DC07 C07C C178      0001117C  00011278    2659          TR    PGMPSW+(0*9)(8),HEXTRTAB

00011120  F384 C085 F154      00011185  00000154    2661          UNPK  PGMPSW+(1*9)(9),PCOLDPSW+(1*4)(5)
00011126  9240 C08D                     0001118D    2662          MVI   PGMPSW+(1*9)+8,C' '
0001112A  DC07 C085 C178      00011185  00011278    2663          TR    PGMPSW+(1*9)(8),HEXTRTAB

00011130  F384 C08E F158      0001118E  00000158    2665          UNPK  PGMPSW+(2*9)(9),PCOLDPSW+(2*4)(5)
00011136  9240 C096                     00011196    2666          MVI   PGMPSW+(2*9)+8,C' '
0001113A  DC07 C08E C178      0001118E  00011278    2667          TR    PGMPSW+(2*9)(8),HEXTRTAB

00011140  F384 C097 F15C      00011197  0000015C    2669          UNPK  PGMPSW+(3*9)(9),PCOLDPSW+(3*4)(5)
00011146  9240 C09F                     0001119F    2670          MVI   PGMPSW+(3*9)+8,C' '
0001114A  DC07 C097 C178      00011197  00011278    2671          TR    PGMPSW+(3*9)(8),HEXTRTAB

00011150  4100 0042                     00000042    2673          LA    R0,L'PROGMSG     R0 <== length of message
00011154  4110 C05E                     0001115E    2674          LA    R1,PROGMSG       R1 --> the message text itself
00011158  4520 C27A                     0001137A    2675          BAL   R2,MSG           Go display this message
                                                    2676
0001115C  07FD                                      2677          BR    R13              Return to caller




0001115E                                            2679 PROGMSG  DS   0CL66
0001115E  D7D9D6C7 D9C1D440                         2680          DC    CL20'PROGRAM CHECK! CODE '
00011172  88888888                                  2681 PROGCODE DC    CL4'hhhh'
00011176  6B                                        2682 PGMCOMMA DC    CL1','
00011177  40D7E2E6 40                               2683          DC    CL5' PSW '
0001117C  88888888 88888888                         2684 PGMPSW   DC    CL36'hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh '
```

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  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

                                                    2686 ************************************************************************
                                                    2687 *                      VERIFICATION ROUTINE
                                                    2688 ************************************************************************

000111A0                                            2690 VERISUB  DS    0H
                                                    2691 *
                                                    2692 **       Loop through the VERIFY TABLE...
                                                    2693 *

000111A0  4110 C32C                 0001142C  2695          LA    R1,VERIFTAB      R1 --> Verify table
000111A4  4120 0012                 00000012  2696          LA    R2,VERIFLEN      R2 <== Number of entries
000111A8  0D30                                2697          BASR  R3,0             Set top of loop

000111AA  9846 1000                 00000000  2699          LM    R4,R6,0(R1)      Load verify table values
000111AE  4D70 C0C2                 000111C2  2700          BAS   R7,VERIFY        Verify results
000111B2  4110 100C                 0000000C  2701          LA    R1,12(,R1)       Next verify table entry
000111B6  0623                                2702          BCTR  R2,R3            Loop through verify table

000111B8  9500 C278                 00011378  2704          CLI   FAILFLAG,X'00'   Did all tests verify okay?
000111BC  078D                                2705          BER   R13              Yes, return to caller
000111BE  47F0 F238                 00000238  2706          B     FAIL             No, load FAILURE disabled wait PSW



                                                    2708 *
                                                    2709 **       Loop through the ACTUAL / EXPECTED results...
                                                    2710 *

000111C2  0D80                                      2712 VERIFY   BASR  R8,0             Set top of loop

000111C4  D50F 4000 5030      00000000  00000030  2714          CLC   0(16,R4),48(R5)  Actual results == Expected results?
000111CA  4770 C0DA                 000111DA  2715          BNE   VERIFAIL         No, show failure
000111CE  4140 4010                 00000010  2716 VERINEXT LA    R4,16(,R4)       Next actual result
000111D2  4150 5040                 00000040  2717          LA    R5,64(,R5)       Next expected result
000111D6  0668                                2718          BCTR  R6,R8            Loop through results

000111D8  07F7                                2720          BR    R7               Return to caller
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    2722 ************************************************************************
                                                    2723 *                      Report the failure...
                                                    2724 ************************************************************************

000111DA  9005 C250                      00011350  2726 VERIFAIL STM   R0,R5,SAVER0R5   Save registers
000111DE  92FF C278                      00011378  2727          MVI   FAILFLAG,X'FF'   Remember verification failure
                                                    2728 *
                                                    2729 **       First, show them the description...
                                                    2730 *
000111E2  D22F C1E0 5000      000112E0   00000000  2731          MVC   FAILDESC,0(R5)   Save results/test description
000111E8  4100 0044                      00000044  2732          LA    R0,L'FAILMSG1    R0 <== length of message
000111EC  4110 C1CC                      000112CC  2733          LA    R1,FAILMSG1      R1 --> the message text itself
000111F0  4520 C27A                      0001137A  2734          BAL   R2,MSG           Go display this message
                                                    2735 *
                                                    2736 **       Save address of actual and expected results
                                                    2737 *
000111F4  5040 C24C                      0001134C  2738          ST    R4,AACTUAL       Save A(actual results)
000111F8  4150 5030                      00000030  2739          LA    R5,48(,R5)       R5 ==> expected results
000111FC  5050 C248                      00011348  2740          ST    R5,AEXPECT       Save A(expected results)
                                                    2741 *
                                                    2742 **       Format and show them the EXPECTED ("Want") results...
                                                    2743 *
00011200  D205 C210 C408      00011310   00011508  2744          MVC   WANTGOT,=CL6'Want: '
00011206  F384 C216 C248      00011316   00011348  2745          UNPK  FAILADR(L'FAILADR+1),AEXPECT(L'AEXPECT+1)
0001120C  9240 C21E                      0001131E  2746          MVI   BLANKEQ,C' '
00011210  DC07 C216 C178      00011316   00011278  2747          TR    FAILADR,HEXTRTAB

00011216  F384 C221 5000      00011321   00000000  2749          UNPK  FAILVALS+(0*9)(9),(0*4)(5,R5)
0001121C  9240 C229                      00011329  2750          MVI   FAILVALS+(0*9)+8,C' '
00011220  DC07 C221 C178      00011321   00011278  2751          TR    FAILVALS+(0*9)(8),HEXTRTAB

00011226  F384 C22A 5004      0001132A   00000004  2753          UNPK  FAILVALS+(1*9)(9),(1*4)(5,R5)
0001122C  9240 C232                      00011332  2754          MVI   FAILVALS+(1*9)+8,C' '
00011230  DC07 C22A C178      0001132A   00011278  2755          TR    FAILVALS+(1*9)(8),HEXTRTAB

00011236  F384 C233 5008      00011333   00000008  2757          UNPK  FAILVALS+(2*9)(9),(2*4)(5,R5)
0001123C  9240 C23B                      0001133B  2758          MVI   FAILVALS+(2*9)+8,C' '
00011240  DC07 C233 C178      00011333   00011278  2759          TR    FAILVALS+(2*9)(8),HEXTRTAB

00011246  F384 C23C 500C      0001133C   0000000C  2761          UNPK  FAILVALS+(3*9)(9),(3*4)(5,R5)
0001124C  9240 C244                      00011344  2762          MVI   FAILVALS+(3*9)+8,C' '
00011250  DC07 C23C C178      0001133C   00011278  2763          TR    FAILVALS+(3*9)(8),HEXTRTAB

00011256  4100 0035                      00000035  2765          LA    R0,L'FAILMSG2    R0 <== length of message
0001125A  4110 C210                      00011310  2766          LA    R1,FAILMSG2      R1 --> the message text itself
0001125E  4520 C27A                      0001137A  2767          BAL   R2,MSG           Go display this message
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT
                                                   2769 *
                                                   2770 **       Format and show them the ACTUAL ("Got") results...
                                                   2771 *
00011262  D205 C210 C40E      00011310  0001150E  2772          MVC   WANTGOT,=CL6'Got:  '
00011268  F384 C216 C24C      00011316  0001134C  2773          UNPK  FAILADR(L'FAILADR+1),AACTUAL(L'AACTUAL+1)
0001126E  9240 C21E                     0001131E  2774          MVI   BLANKEQ,C' '
00011272  DC07 C216 C178      00011316  00011278  2775          TR    FAILADR,HEXTRTAB

00011278  F384 C221 4000      00011321  00000000  2777          UNPK  FAILVALS+(0*9)(9),(0*4)(5,R4)
0001127E  9240 C229                     00011329  2778          MVI   FAILVALS+(0*9)+8,C' '
00011282  DC07 C221 C178      00011321  00011278  2779          TR    FAILVALS+(0*9)(8),HEXTRTAB

00011288  F384 C22A 4004      0001132A  00000004  2781          UNPK  FAILVALS+(1*9)(9),(1*4)(5,R4)
0001128E  9240 C232                     00011332  2782          MVI   FAILVALS+(1*9)+8,C' '
00011292  DC07 C22A C178      0001132A  00011278  2783          TR    FAILVALS+(1*9)(8),HEXTRTAB

00011298  F384 C233 4008      00011333  00000008  2785          UNPK  FAILVALS+(2*9)(9),(2*4)(5,R4)
0001129E  9240 C23B                     0001133B  2786          MVI   FAILVALS+(2*9)+8,C' '
000112A2  DC07 C233 C178      00011333  00011278  2787          TR    FAILVALS+(2*9)(8),HEXTRTAB

000112A8  F384 C23C 400C      0001133C  0000000C  2789          UNPK  FAILVALS+(3*9)(9),(3*4)(5,R4)
000112AE  9240 C244                     00011344  2790          MVI   FAILVALS+(3*9)+8,C' '
000112B2  DC07 C23C C178      0001133C  00011278  2791          TR    FAILVALS+(3*9)(8),HEXTRTAB

000112B8  4100 0035                     00000035  2793          LA    R0,L'FAILMSG2    R0 <== length of message
000112BC  4110 C210                     00011310  2794          LA    R1,FAILMSG2      R1 --> the message text itself
000112C0  4520 C27A                     0001137A  2795          BAL   R2,MSG           Go display this message

000112C4  9805 C250                     00011350  2797          LM    R0,R5,SAVER0R5   Restore registers
000112C8  47F0 C0CE                     000111CE  2798          B     VERINEXT         Continue with verification...



000112CC                                          2800 FAILMSG1 DS    0CL68
000112CC  C3D6D4D7 C1D9C9E2                       2801          DC    CL20'COMPARISON FAILURE! '
000112E0  4D8485A2 83998997                       2802 FAILDESC DC    CL48'(description)'



00011310                                          2804 FAILMSG2 DS    0CL53
00011310  40404040 4040                           2805 WANTGOT  DC    CL6' '           'Want: ' -or- 'Got:  '
00011316  C1C1C1C1 C1C1C1C1                       2806 FAILADR  DC    CL8'AAAAAAAA'
0001131E  407E40                                  2807 BLANKEQ  DC    CL3' = '
00011321  88888888 88888888                       2808 FAILVALS DC    CL36'hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh '

00011348  00000000                                2810 AEXPECT  DC    F'0'             ==> Expected ("Want") results
0001134C  00000000                                2811 AACTUAL  DC    F'0'             ==> Actual ("Got") results
00011350  00000000 00000000                       2812 SAVER0R5 DC    6F'0'            Registers R0 - R5 save area
00011368  F0F1F2F3 F4F5F6F7                       2813 CHARHEX  DC    CL16'0123456789ABCDEF'
                             00011278  00000010   2814 HEXTRTAB EQU   CHARHEX-X'F0'    Hexadecimal translation table
00011378  00                                      2815 FAILFLAG DC    X'00'            FF = Fail, 00 = Success
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                          2817 ********************************************************************
                                          2818 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                          2819 ********************************************************************

0001137A  4900 C404                 00011504  2821 MSG      CH    R0,=H'0'                Do we even HAVE a message?
0001137E  07D2                               2822          BNHR  R2                      No, ignore

00011380  9002 C2B0                 000113B0  2824          STM   R0,R2,MSGSAVE           Save registers

00011384  4900 C406                 00011506  2826          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
00011388  47D0 C290                 00011390  2827          BNH   MSGOK                   Yes, continue
0001138C  4100 005F                 0000005F  2828          LA    R0,L'MSGMSG             No, set to maximum

00011390  1820                               2830 MSGOK    LR    R2,R0                   Copy length to work register
00011392  0620                               2831          BCTR  R2,0                    Minus-1 for execute
00011394  4420 C2BC                 000113BC  2832          EX    R2,MSGMVC               Copy message to O/P buffer

00011398  4120 200A                 0000000A  2834          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
0001139C  4110 C2C2                 000113C2  2835          LA    R1,MSGCMD               Point to true command

000113A0  83120008                           2837          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
000113A4  4780 C2AA                 000113AA  2838          BZ    MSGRET                  Return if successful
000113A8  0000                               2839          DC    H'0'                    CRASH for debugging purposes

000113AA  9802 C2B0                 000113B0  2841 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
000113AE  07F2                               2842          BR    R2                      Return to caller
```

```
000113B0  00000000 00000000                  2844 MSGSAVE  DC    3F'0'                   Registers save area
000113BC  D200 C2CB 1000      000113CB  00000000  2845 MSGMVC   MVC   MSGMSG(0),0(R1)      Executed instruction

000113C2  D4E2C7D5 D6C8405C                  2847 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
000113CB  40404040 40404040                  2848 MSGMSG   DC    CL95' '                 The message text to be displayed
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    2850 ********************************************************************************
                                                    2851 *                            VERIFY TABLE
                                                    2852 ********************************************************************************
                                                    2853 *
                                                    2854 *        A(actual results), A(expected results), A(#of results)
                                                    2855 *
                                                    2856 ********************************************************************************
0001142C                                            2858 VERIFTAB DC    0F'0'
0001142C  00001000                                  2859          DC    A(SBFPNFOT)
00011430  00007000                                  2860          DC    A(SBFPNFOT_GOOD)
00011434  00000040                                  2861          DC    A(SBFPNFOT_NUM)
                                                    2862 *
00011438  00001400                                  2863          DC    A(SBFPNFFL)
0001143C  00008000                                  2864          DC    A(SBFPNFFL_GOOD)
00011440  00000040                                  2865          DC    A(SBFPNFFL_NUM)
                                                    2866 *
00011444  00001800                                  2867          DC    A(SBFPOUT)
00011448  00009000                                  2868          DC    A(SBFPOUT_GOOD)
0001144C  00000006                                  2869          DC    A(SBFPOUT_NUM)
                                                    2870 *
00011450  00001900                                  2871          DC    A(SBFPFLGS)
00011454  00009180                                  2872          DC    A(SBFPFLGS_GOOD)
00011458  00000006                                  2873          DC    A(SBFPFLGS_NUM)
                                                    2874 *
0001145C  00001A00                                  2875          DC    A(SBFPRMO)
00011460  00009300                                  2876          DC    A(SBFPRMO_GOOD)
00011464  0000000C                                  2877          DC    A(SBFPRMO_NUM)
                                                    2878 *
00011468  00001D00                                  2879          DC    A(SBFPRMOF)
0001146C  00009600                                  2880          DC    A(SBFPRMOF_GOOD)
00011470  0000000C                                  2881          DC    A(SBFPRMOF_NUM)
                                                    2882 *
00011474  00003000                                  2883          DC    A(LBFPNFOT)
00011478  00009900                                  2884          DC    A(LBFPNFOT_GOOD)
0001147C  00000080                                  2885          DC    A(LBFPNFOT_NUM)
                                                    2886 *
00011480  00003800                                  2887          DC    A(LBFPNFFL)
00011484  0000B900                                  2888          DC    A(LBFPNFFL_GOOD)
00011488  00000040                                  2889          DC    A(LBFPNFFL_NUM)
                                                    2890 *
0001148C  00003C00                                  2891          DC    A(LBFPOUT)
00011490  0000C900                                  2892          DC    A(LBFPOUT_GOOD)
00011494  0000000C                                  2893          DC    A(LBFPOUT_NUM)
                                                    2894 *
00011498  00003E00                                  2895          DC    A(LBFPFLGS)
0001149C  0000CC00                                  2896          DC    A(LBFPFLGS_GOOD)
000114A0  00000006                                  2897          DC    A(LBFPFLGS_NUM)
                                                    2898 *
000114A4  00004000                                  2899          DC    A(LBFPRMO)
000114A8  0000CD80                                  2900          DC    A(LBFPRMO_GOOD)
000114AC  00000014                                  2901          DC    A(LBFPRMO_NUM)
                                                    2902 *
000114B0  00004500                                  2903          DC    A(LBFPRMOF)
000114B4  0000D280                                  2904          DC    A(LBFPRMOF_GOOD)
000114B8  0000000C                                  2905          DC    A(LBFPRMOF_NUM)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT
                                                    2906 *
000114BC  00005000                                  2907          DC    A(XBFPNFOT)
000114C0  0000D580                                  2908          DC    A(XBFPNFOT_GOOD)
000114C4  00000080                                  2909          DC    A(XBFPNFOT_NUM)
                                                    2910 *
000114C8  00005800                                  2911          DC    A(XBFPNFFL)
000114CC  0000F580                                  2912          DC    A(XBFPNFFL_GOOD)
000114D0  00000040                                  2913          DC    A(XBFPNFFL_NUM)
                                                    2914 *
000114D4  00005C00                                  2915          DC    A(XBFPOUT)
000114D8  00010580                                  2916          DC    A(XBFPOUT_GOOD)
000114DC  0000000C                                  2917          DC    A(XBFPOUT_NUM)
                                                    2918 *
000114E0  00005E00                                  2919          DC    A(XBFPFLGS)
000114E4  00010880                                  2920          DC    A(XBFPFLGS_GOOD)
000114E8  00000006                                  2921          DC    A(XBFPFLGS_NUM)
                                                    2922 *
000114EC  00006000                                  2923          DC    A(XBFPRMO)
000114F0  00010A00                                  2924          DC    A(XBFPRMO_GOOD)
000114F4  00000014                                  2925          DC    A(XBFPRMO_NUM)
                                                    2926 *
000114F8  00006A00                                  2927          DC    A(XBFPRMOF)
000114FC  00010F00                                  2928          DC    A(XBFPRMOF_GOOD)
00011500  00000008                                  2929          DC    A(XBFPRMOF_NUM)
                                                    2930 *
                            00000012  00000001    2931 VERIFLEN EQU   (*-VERIFTAB)/12    #of entries in verify table
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2     STMT

00011504                                            2933           END
00011504  0000                                    2934                =H'0'
00011506  005F                                    2935                =AL2(L'MSGMSG)
00011508  E68195A3 7A40                           2936                =CL6'Want: '
0001150E  C796A37A 4040                           2937                =CL6'Got:  '
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
AACTUAL	F	01134C	4	2811	2738 2773
AEXPECT	F	011348	4	2810	2740 2745
AHELPERS	A	00027C	4	191	181 229
BFPDIV	J	000000	70932	107	
BLANKEQ	C	01131E	3	2807	2746 2774
CHARHEX	C	011368	16	2813	2814
CTLR0	F	000308	4	239	200 201 202
FAIL	I	000238	4	189	2706
FAILADR	C	011316	8	2806	2745 2747 2773 2775
FAILDESC	C	0112E0	48	2802	2731
FAILFLAG	X	011378	1	2815	2704 2727
FAILMSG1	C	0112CC	68	2800	2732 2733
FAILMSG2	C	011310	53	2804	2765 2766 2793 2794
FAILPSW	X	0002F8	8	237	189
FAILVALS	C	011321	36	2808	2749 2750 2751 2753 2754 2755 2757 2758 2759 2761 2762 2763 2777 2778 2779 2781 2782 2783 2785 2786 2787 2789 2790 2791
FPCMCT	U	000005	1	830	445 619 778
FPCMODES	C	000798	1	824	830 448 622 781
FPCREGNT	X	00030C	4	240	333 347 389 403 450 458 508 521 563 577 624 632 682 728 783
FPCREGTR	X	000310	4	241	340 353 396 409 515 527 570 583 692 738
FPR0	U	000000	1	128	
FPR1	U	000001	1	129	332 334 339 341 346 391 392 399 453 454 507 509 514 516 565 566 573 627 628 680 683 690 693 731 733 742 787 789
FPR10	U	00000A	1	138	679 685 689 695 786 791
FPR11	U	00000B	1	139	
FPR12	U	00000C	1	140	
FPR13	U	00000D	1	141	729 733 734 739 742 743
FPR14	U	00000E	1	142	
FPR15	U	00000F	1	143	730 735 740 744
FPR2	U	000002	1	130	
FPR3	U	000003	1	131	681 691 732 788
FPR4	U	000004	1	132	
FPR5	U	000005	1	133	
FPR6	U	000006	1	134	
FPR7	U	000007	1	135	
FPR8	U	000008	1	136	331 334 335 338 341 342 345 348 349 352 354 355 390 392 393 397 399 400 404 405 406 410 411 412 452 454 455 460 461 462 506 509 510 513 516 517 520 522 523 526 528 529 564 566 567 571 573 574 578 579 580 584 585 586 626 628 629 634 635 636 678 683 684 688 693 694 785 789 790
FPR9	U	000009	1	137	
GOODPSW	X	0002E8	8	236	233
HELPERS	H	011100	2	2646	146 191
HEXTRTAB	U	011278	16	2814	2655 2659 2663 2667 2671 2747 2751 2755 2759 2763 2775 2779 2783 2787 2791
IMAGE	1	000000	70932	0	
LBFPCT	U	000006	1	1056	274
LBFPF	I	000594	4	557	214
LBFPFLGS	U	003E00	1	1256	277 2895
LBFPFLGS_GOOD	U	00CC00	1	2059	2072 2896
LBFPFLGS_NUM	U	000006	1	2072	2897
LBFPIN	D	000850	8	1019	1056 275
LBFPINRM	F	0008B0	4	1067	1093 281
LBFPNF	H	00050E	2	495	212
LBFPNFCT	U	000008	1	1001	268

```
     SYMBOL          TYPE  VALUE   LENGTH  DEFN  REFERENCES

LBFPNFFL              U    003800       1  1251   271  2887
LBFPNFFL_GOOD         U    00B900       1  1899  2028  2888
LBFPNFFL_NUM          U    000040       1  2028  2889
LBFPNFIN              F    000810       4   992  1001   269
LBFPNFOT              U    003000       1  1249   270  2883
LBFPNFOT_GOOD         U    009900       1  1639  1896  2884
LBFPNFOT_NUM          U    000080       1  1896  2885
LBFPOUT               U    003C00       1  1254   276  2891
LBFPOUT_GOOD          U    00C900       1  2031  2056  2892
LBFPOUT_NUM           U    00000C       1  2056  2893
LBFPRM                I    00060A       4   612   216
LBFPRMCT              U    000004       1  1093   280
LBFPRMO               U    004000       1  1259   282  2899
LBFPRMOF              U    004500       1  1261   283  2903
LBFPRMOF_GOOD         U    00D280       1  2119  2144  2904
LBFPRMOF_NUM          U    00000C       1  2144  2905
LBFPRMO_GOOD          U    00CD80       1  2075  2116  2900
LBFPRMO_NUM           U    000014       1  2116  2901
LONGF                 F    000354       4   273   213
LONGNF                F    000344       4   267   211
MSG                   I    01137A       4  2821  2675  2734  2767  2795
MSGCMD                C    0113C2       9  2847  2834  2835
MSGMSG                C    0113CB      95  2848  2828  2845  2826
MSGMVC                I    0113BC       6  2845  2832
MSGOK                 I    011390       2  2830  2827
MSGRET                I    0113AA       4  2841  2838
MSGSAVE               F    0113B0       4  2844  2824  2841
PCINTCD               H    00008E       2   159   176  2653
PCNOTDTA              I    00020C       4   180   177
PCOLDPSW              U    000150       1   161   178  2657  2661  2665  2669
PGMCK                 H    011100       2  2652   182
PGMCOMMA              C    011176       1  2682  2654
PGMPSW                C    01117C      36  2684  2657  2658  2659  2661  2662  2663  2665  2666  2667  2669  2670  2671
PROGCHK               H    000200       2   175   167
PROGCODE              C    011172       4  2681  2653  2655
PROGMSG               C    01115E      66  2679  2673  2674
PROGPSW               D    000228       8   188   187
R0                    U    000000       1   109   180   183   200   202  2673  2726  2732  2765  2793  2797  2821  2824  2826  2828
                                                2830  2841
R1                    U    000001       1   110   442   448   451   459   616   622   625   633   775   781   784  2674  2695  2699
                                                2701  2733  2766  2794  2835  2845
R10                   U    00000A       1   119   204   206   208   211   213   215   218   220   222   321   322   327   383   384
                                                438   439   496   497   502   557   558   612   613   668   669   674   722   723
                                                771   772
R11                   U    00000B       1   120
R12                   U    00000C       1   121   146   181   229   325   364   387   418   443   475   500   538   561   592   617
                                                648   672   704   726   750   776   803
R13                   U    00000D       1   122   182   205   207   209   212   214   216   219   221   223   230   324   365   386
                                                419   441   477   499   539   560   593   615   650   671   705   725   752   774
                                                805  2677  2705
R14                   U    00000E       1   123   185   186   231   232
R15                   U    00000F       1   124   145   180   183
R2                    U    000002       1   111   321   323   364   383   385   418   438   440   475   496   498   538   557   559
                                                592   612   614   648   668   670   704   722   724   750   771   773   803  2675
                                               2696  2702  2734  2767  2795  2822  2824  2830  2831  2832  2834  2841  2842
R3                    U    000003       1   112   321   331   338   345   352   363   383   390   391   397   404   405   410   411
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
					415 438 452 453 460 461 472 496 506 513 520 526 537 557
					564 565 571 578 579 584 585 589 612 626 627 634 635 646
					668 678 679 688 689 703 722 729 730 731 732 739 740 747
					771 785 786 787 788 801 2697 2702
R4	U	000004	1	113	327 361 502 535 674 701 2699 2714 2716 2738 2777 2781 2785 2789
R5	U	000005	1	114	327 332 339 346 348 354 358 445 448 468 502 507 514 522
					528 532 619 622 642 674 680 681 690 691 698 778 781 797
					2714 2717 2726 2731 2739 2740 2749 2753 2757 2761 2797
R6	U	000006	1	115	329 361 504 535 676 701 2699 2718
R7	U	000007	1	116	322 335 342 349 355 359 384 393 400 406 412 416 439 455
					462 465 473 497 510 517 523 529 533 558 567 574 580 586
					590 613 629 636 639 669 684 685 694 695 699 723 734 735
					743 744 748 772 790 791 794 2700 2720
R8	U	000008	1	117	322 336 343 350 356 360 384 394 401 407 413 417 439 456
					463 466 474 497 511 518 524 530 534 558 568 575 581 587
					591 613 630 637 640 647 669 686 696 700 723 736 745 749
					772 792 795 802 2712 2718
R9	U	000009	1	118	446 468 620 642 779 797
RMLONGS	F	000364	4	279	215
RMSHORTS	F	000334	4	261	208
RMXTNDS	F	000394	4	297	222
SAVER0R5	F	011350	4	2812	2726 2797
SAVEREGS	F	00023C	4	190	180 183
SBFPCT	U	000006	1	925	256
SBFPF	I	00042E	4	383	207
SBFPFLGS	U	001900	1	1240	259 2871
SBFPFLGS_GOOD	U	009180	1	1567	1580 2872
SBFPFLGS_NUM	U	000006	1	1580	2873
SBFPIN	F	0007C0	4	888	925 257
SBFPINRM	F	0007F0	4	936	962 263
SBFPNF	H	0003A4	2	320	205
SBFPNFCT	U	000008	1	870	250
SBFPNFFL	U	001400	1	1235	253 2863
SBFPNFFL_GOOD	U	008000	1	1419	1548 2864
SBFPNFFL_NUM	U	000040	1	1548	2865
SBFPNFIN	F	0007A0	4	861	870 251
SBFPNFOT	U	001000	1	1233	252 2859
SBFPNFOT_GOOD	U	007000	1	1287	1416 2860
SBFPNFOT_NUM	U	000040	1	1416	2861
SBFPOUT	U	001800	1	1238	258 2867
SBFPOUT_GOOD	U	009000	1	1551	1564 2868
SBFPOUT_NUM	U	000006	1	1564	2869
SBFPRM	I	0004A4	4	438	209
SBFPRMCT	U	000004	1	962	262
SBFPRMO	U	001A00	1	1243	264 2875
SBFPRMOF	U	001D00	1	1245	265 2879
SBFPRMOF_GOOD	U	009600	1	1611	1636 2880
SBFPRMOF_NUM	U	00000C	1	1636	2881
SBFPRMO_GOOD	U	009300	1	1583	1608 2876
SBFPRMO_NUM	U	00000C	1	1608	2877
SHORTF	F	000324	4	255	206
SHORTNF	F	000314	4	249	204
START	H	000280	2	199	164
STRTLABL	U	000000	1	108	158 161 163 166 174 1233 1235 1238 1240 1243 1245 1249 1251 1254
					1256 1259 1261 1265 1267 1270 1272 1275 1277 1285
VERIFAIL	I	0111DA	4	2726	2715

```
     SYMBOL         TYPE  VALUE   LENGTH  DEFN  REFERENCES

VERIFLEN             U    000012       1  2931  2696
VERIFTAB             F    01142C       4  2858  2931  2695
VERIFY               I    0111C2       2  2712  2700
VERINEXT             I    0111CE       4  2716  2798
VERISUB              H    0111A0       2  2690   230
WANTGOT              C    011310       6  2805  2744  2772
XBFPCT               U    000006       1  1187   292
XBFPF                I    0006E2       4   722   221
XBFPFLGS             U    005E00       1  1272   295  2919
XBFPFLGS_GOOD        U    010880       1  2567  2580  2920
XBFPFLGS_NUM         U    000006       1  2580  2921
XBFPIN               F    000970       4  1150  1187   293
XBFPINRM             D    000A30       8  1198  1224   299
XBFPNF               H    000670       2   667   219
XBFPNFCT             U    000008       1  1132   286
XBFPNFFL             U    005800       1  1267   289  2911
XBFPNFFL_GOOD        U    00F580       1  2407  2536  2912
XBFPNFFL_NUM         U    000040       1  2536  2913
XBFPNFIN             F    0008F0       4  1123  1132   287
XBFPNFOT             U    005000       1  1265   288  2907
XBFPNFOT_GOOD        U    00D580       1  2147  2404  2908
XBFPNFOT_NUM         U    000080       1  2404  2909
XBFPOUT              U    005C00       1  1270   294  2915
XBFPOUT_GOOD         U    010580       1  2539  2564  2916
XBFPOUT_NUM          U    00000C       1  2564  2917
XBFPRM               I    000740       4   771   223
XBFPRMCT             U    000004       1  1224   298
XBFPRMO              U    006000       1  1275   300  2923
XBFPRMOF             U    006A00       1  1277   301  2927
XBFPRMOF_GOOD        U    010F00       1  2627  2644  2928
XBFPRMOF_NUM         U    000008       1  2644  2929
XBFPRMO_GOOD         U    010A00       1  2583  2624  2924
XBFPRMO_NUM          U    000014       1  2624  2925
XTNDF                F    000384       4   291   220
XTNDNF               F    000374       4   285   218
=AL2(L'MSGMSG)       R    011506       2  2935  2826
=CL6'Got:  '         C    01150E       6  2937  2772
=CL6'Want: '         C    011508       6  2936  2744
=H'0'                H    011504       2  2934  2821
```

MACRO DEFN REFERENCES

No defined macros

```
   DESC    SYMBOL   SIZE      POS           ADDR

Entry: 0

Image      IMAGE   70932  00000-11513  00000-11513
  Region           70932  00000-11513  00000-11513
    CSECT  BFPDIV  70932  00000-11513  00000-11513
```

```
   STMT                                                FILE NAME
1     c:\Users\Fish\Documents\Visual Studio 2008\Projects\MyProjects\ASMA-0\bfp-014-divide\bfp-014-divide.asm

** NO ERRORS FOUND **
```