

```
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--  
-- Purpose:  
--  
--   D FlipFlop  
--  
-- Discussion:  
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--  
-- Licensing:  
--  
--   This code is distributed under the GNU LGPL license.  
--  
-- Modified:  
--  
--   2012.03.29  
--  
-- Author:  
--  
--   Young W. Lim  
--  
-- Parameters:  
--  
--   Input:  
--  
--   Output:  
-----
```

```
library STD;  
use STD.textio.all;  
  
library IEEE;  
use IEEE.std_logic_1164.all;  
use IEEE.numeric_std.all;  
  
entity dff is  
  generic (  
    WD      : in natural := 32);  
  
  port (  
    clk     : in  std_logic := '0';  
    clk     : in  std_logic := '0';  
    din     : in  std_logic_vector (WD-1 downto 0) := (others=>'0');  
    dq      : out std_logic_vector (WD-1 downto 0) := (others=>'0') );  
  
end dff;  
  
architecture rtl of dff is  
begin  
  Reg: process (clk, rst)  
  begin -- process Reg  
    if rst = '0' then -- asynchronous reset (active low)  
      dq <= (others=>'0');  
    elsif clk'event and clk = '1' then -- rising clock edge  
      dq <= din;  
    end if;  
  end process Reg;  
  
end rtl;
```