```
--------------------------------------------------------------------------------
--
--  Purpose:
--
--    some test pieces for data type conversion
--    real, integer, std_logic_vector
--
--  Discussion:
--
--
--  Licensing:
--
--    This code is distributed under the GNU LGPL license.
--
--  Modified:
--
--    2012.03.08
--
--  Author:
--
--    Young W. Lim
--
--  Parameters:
--
--    Input:
--
--    Output:
--------------------------------------------------------------------------------




library STD;
use STD.textio.all;

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity tt is
end tt;

architecture num of tt is
  constant x : real := 7.8539816339744830962E-01;
  constant k : std_logic_vector (31 downto 0) := X"7FFF_FFFF";

begin
  process
    variable my_line : line;
    variable n : std_logic_vector (31 downto 0);
    variable m : integer := 9999;
    variable y : real := 0.0;
  begin
    -- n <= integer(x * k);
    -- write(my_line, x);
    write(my_line, String'("test "));

    m := to_integer(signed(k));

    write(my_line, integer'(m));
    write(my_line, ' ');

    write(my_line, real'(x));
    write(my_line, ' ');

    y := x * real(m);

    write(my_line, real'(y));
    write(my_line, ' ');

    m := integer(y);

    write(my_line, integer'(m));
    write(my_line, ' ');

    writeline(output, my_line);
```

```
    n := std_logic_vector(to_signed(m, 32));

    m := to_integer(signed(n));

    write(my_line, integer'(m));
    write(my_line, ' ');

    writeline(output, my_line);


    wait;
  end process;


end num;
```