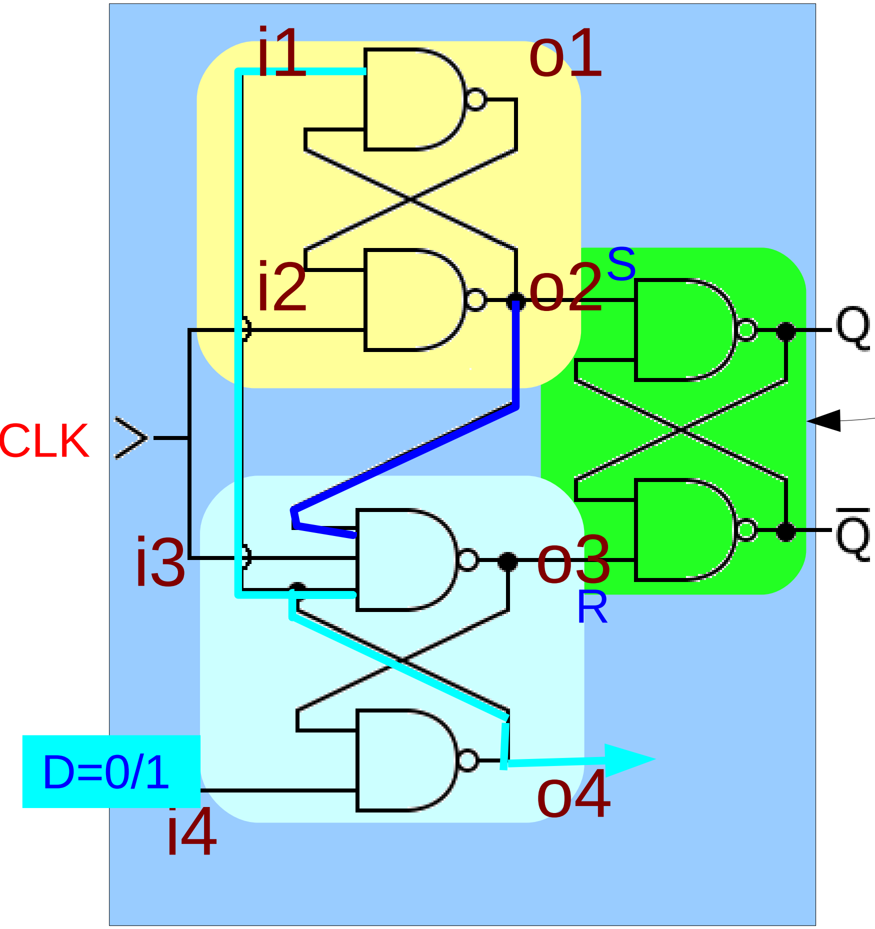
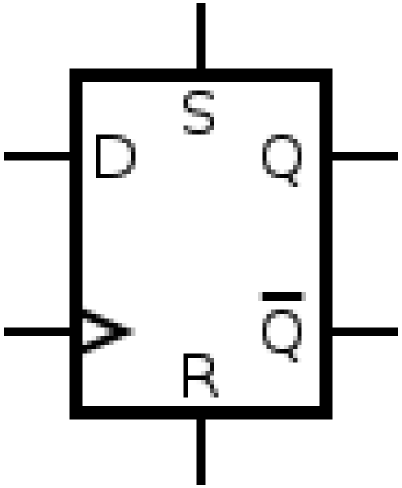
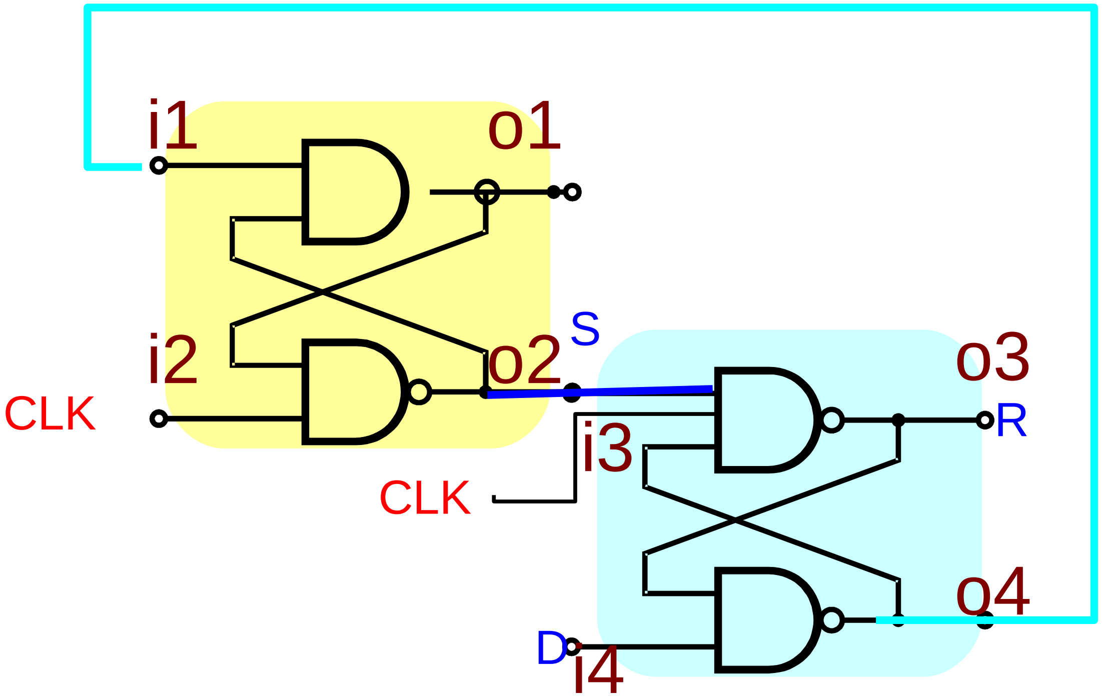
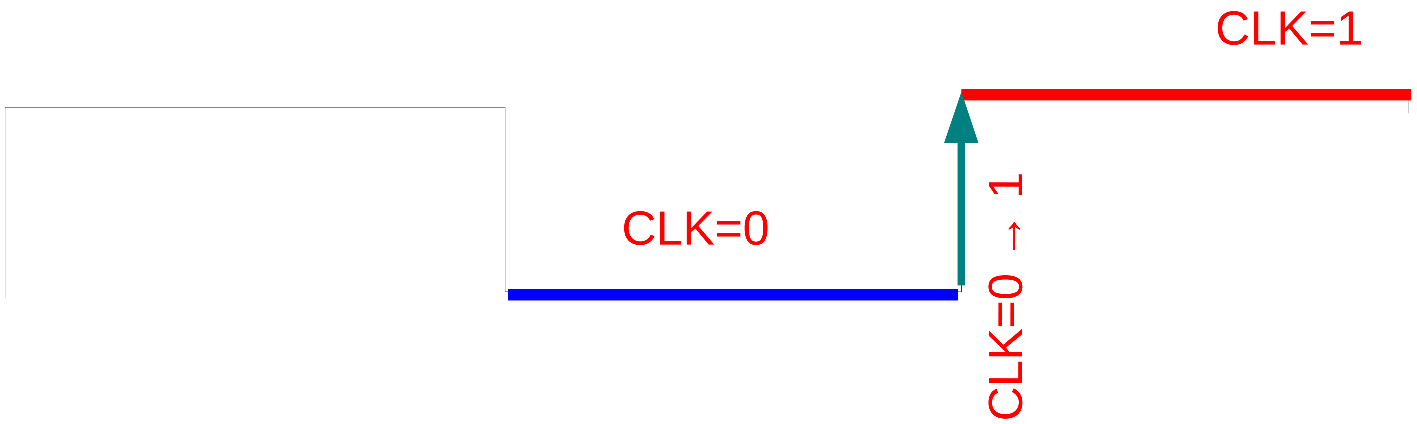


Output Stage Latch

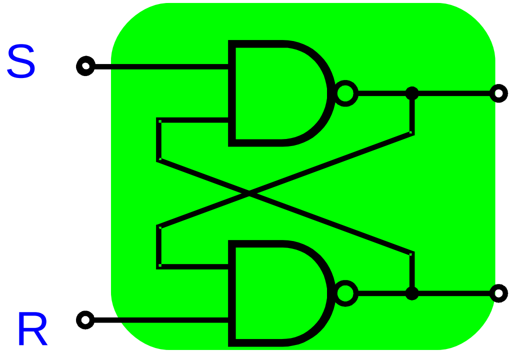


Input Stage Latch





Output Stage Latch



CLK=0

S=1
R=1

Maintain
output latch

CLK=0 → 1

When D=0
S=1
R=0
When D=1
S=0
R=1

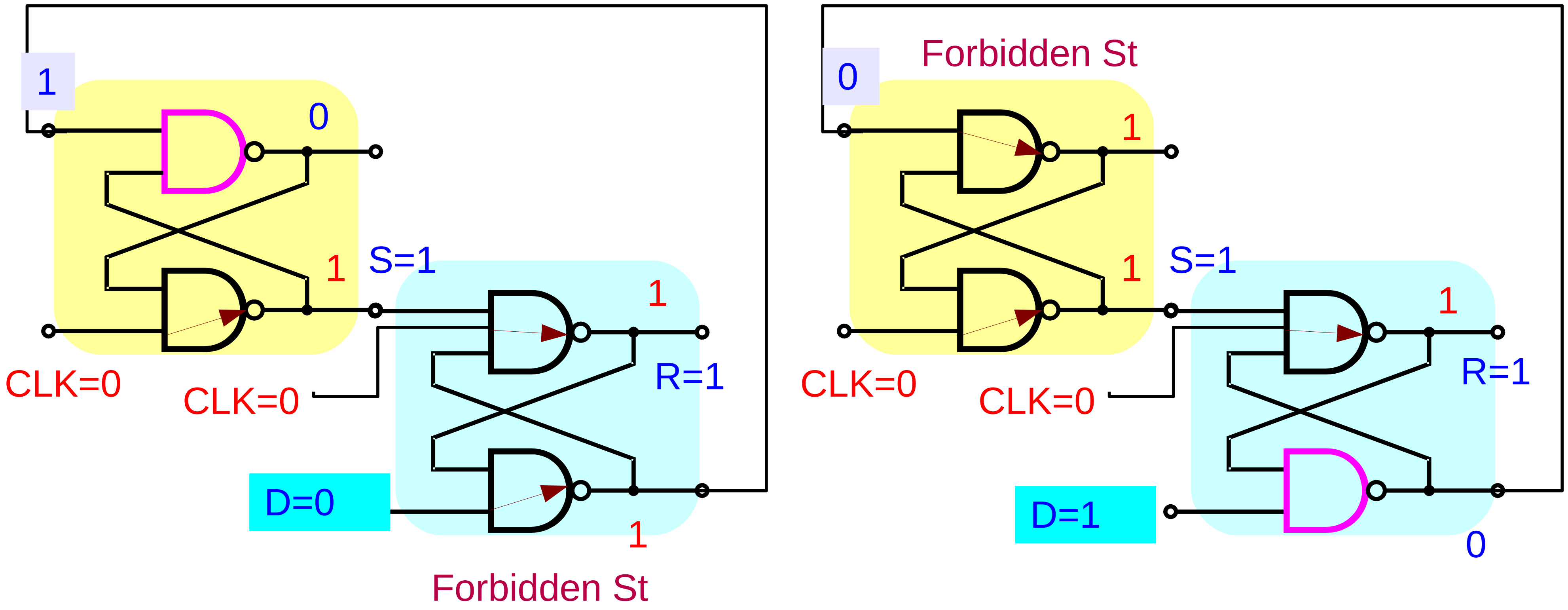
D=0/1 at the rising edge reset / set the output latch

CLK= 1

When D=0 → 1
S=1
R=0
When D=1 → 0
S=0
R=1

Maintain reset / set at the rising edge regardless of input changes

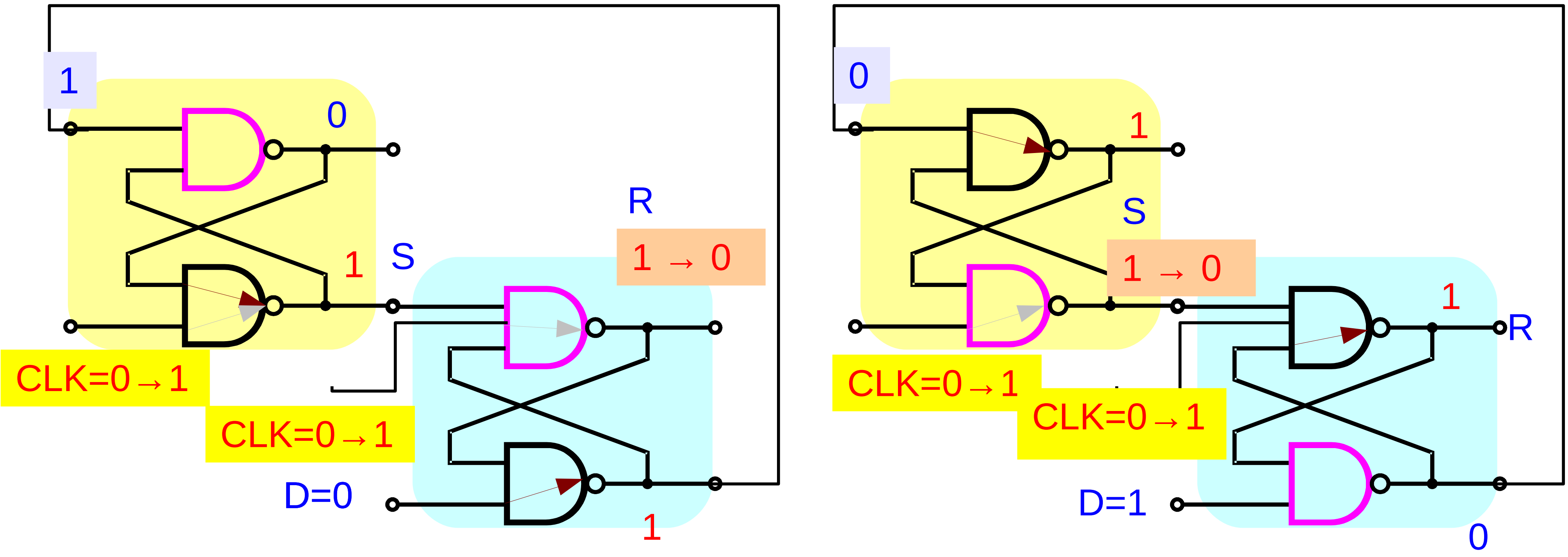
Input Stage Latch – CLK =0 SR=11



If the clock is low,
both the output signals of the input stage are high
regardless of the data input;
the output latch is unaffected
and it stores the previous state.

Input Stage Latch – Rising Edge

D=0 → SR=10
D=1 → SR=01



When the clock signal changes from low to high, (rising edge) only one of the output voltages (S or R) goes low (depending on the data signal D) and sets/resets the output latch:

(D=0 → SR = 10 → reset the output latch → Q= 0)

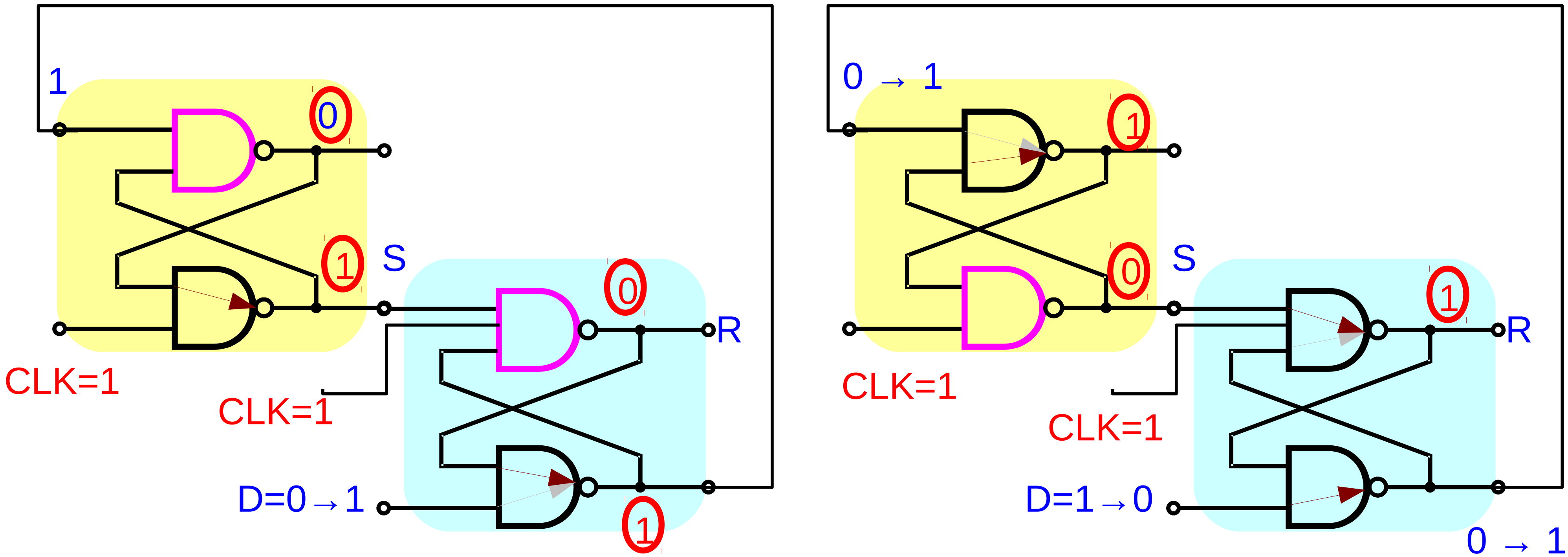
(D=1 → SR = 01 → set the output latch → Q = 1)

if D = 0, the lower output becomes low ; (Reset operation SR=10)

if D = 1, the upper output becomes low. (Set operation SR=01)

Input Stage Latch – CLK=1

D=(0→1) →SR=10
D=(1→0) →SR=01



If the clock signal continues staying **high**,
the outputs keep their states regardless of the data input
(D=0: SR=10, D=1: SR=01 at the rising edge)
and force the output latch to stay in the corresponding state
as the input logical zero remains active (SR=10: Reset, SR=01: Set)
while the clock is **high**.

If the clock signal continues staying high,
the outputs keep their states regardless of the data input
and force the output latch to stay in the corresponding state
as the input logical zero remains active
while the clock is high.

Hence the role of the output latch is
to store the data only while the clock is low.

The input stage (the two latches on the left)

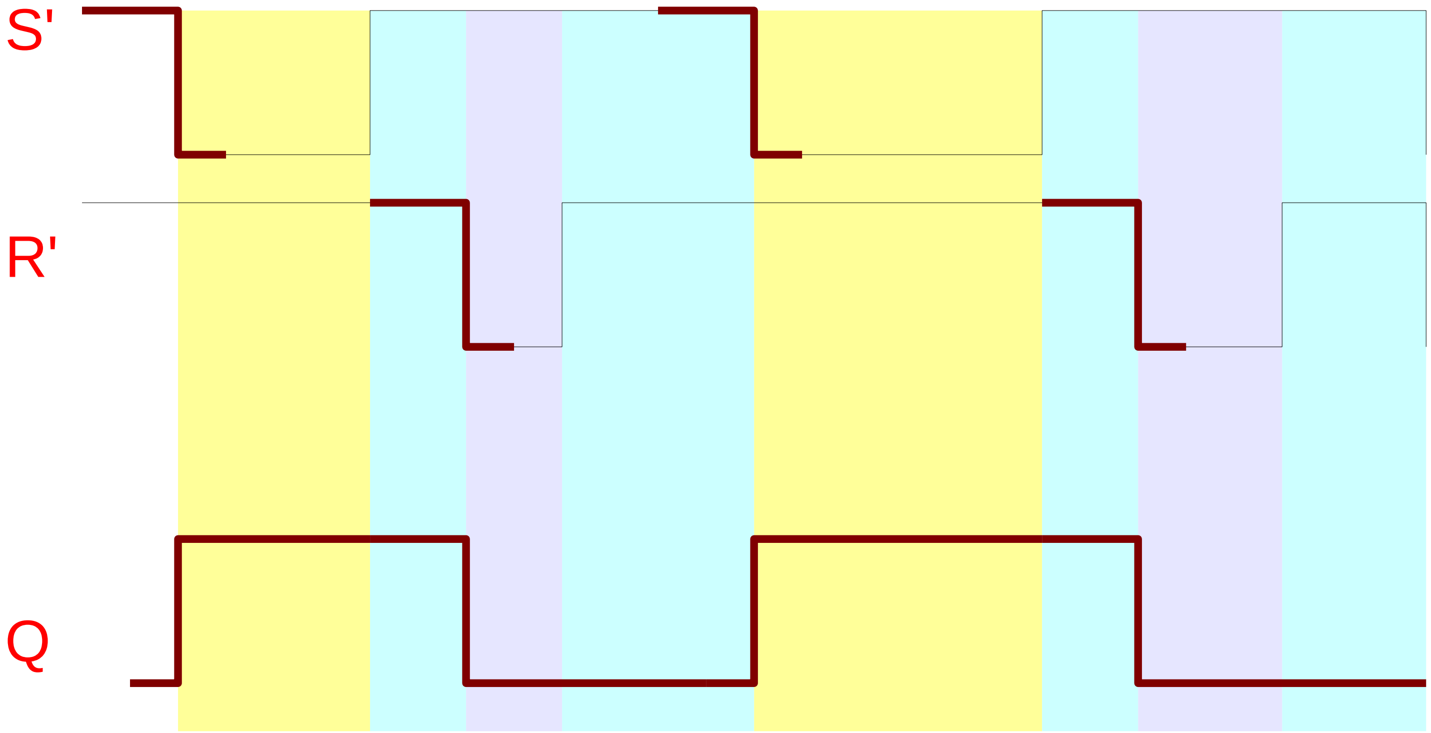
processes the clock and data signals

to ensure correct input signals

for the output stage (the single latch on the right).

The circuit is closely related to the gated D latch as both the circuits
convert the two D input states (0 and 1) D
to two input combinations (10 and 01) SR
for the output SR latch
by inverting the data input signal
(both the circuits split the single D signal
in two complementary S and R signals).
The difference is that
in the gated D latch, simple NAND logical gates are used
while in the positive-edge-triggered D flip-flop SR NAND latches are used for this purpose.
The role of these latches is to "lock" the active output producing low voltage (a logical zero); thus the positive-edge-triggered D flip-flop can be thought of as a gated D latch with latched input gates.

NAND RS Latch



S' = 0
R' = 1

S' = 1
R' = 1

S' = 1
R' = 0

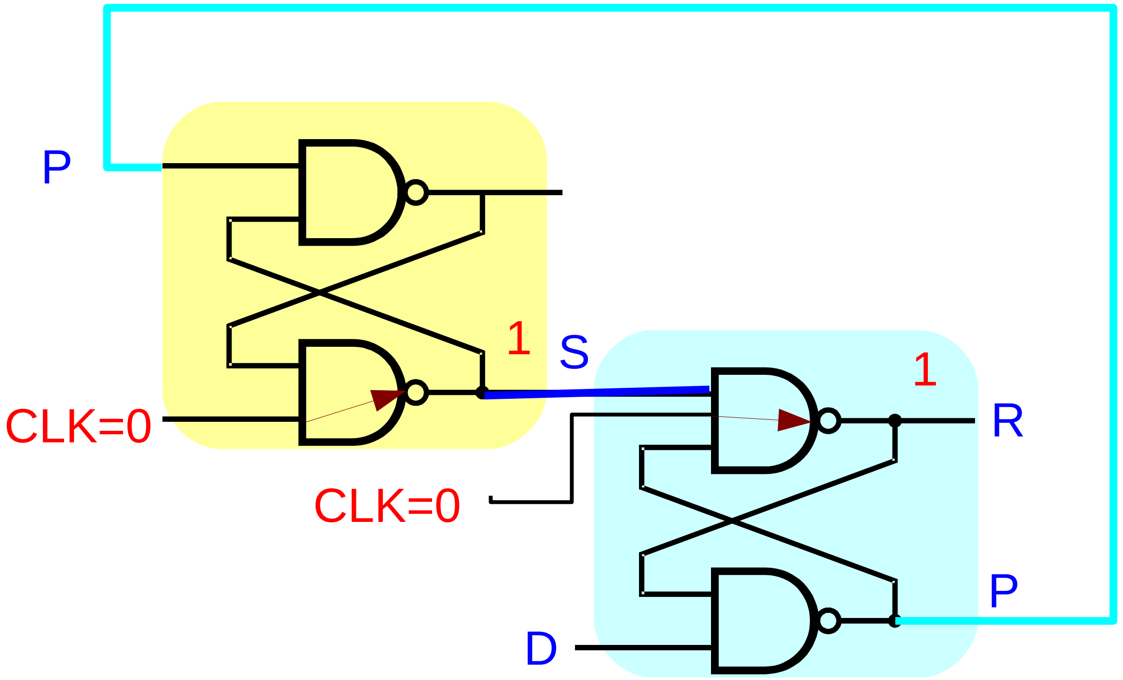
S' = 1
R' = 1

S' = 0
R' = 1

S' = 1
R' = 1

S' = 1
R' = 0

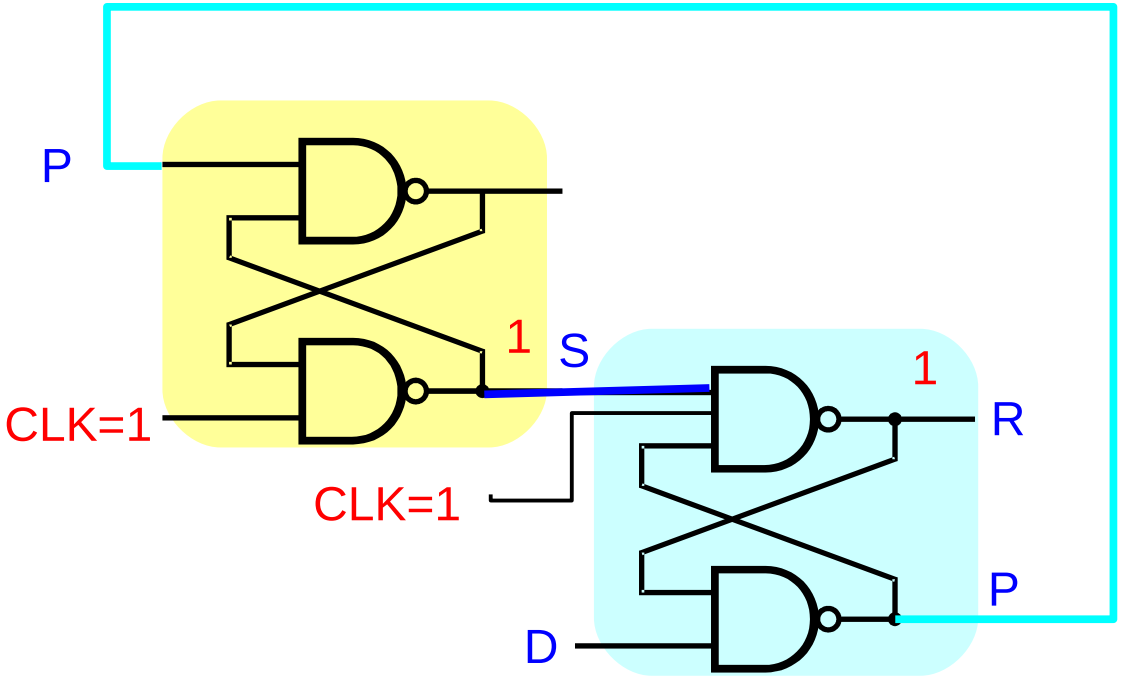
S' = 1
R' = 1



CLK=0		L1 in Reset if P=0	L1 in forbidden if P=1

L2 in Set	if D=1	S=1, R=1,
		P=0
			X

L2 in forbidden	if D=0	X	S=1, R=1,
			P=1

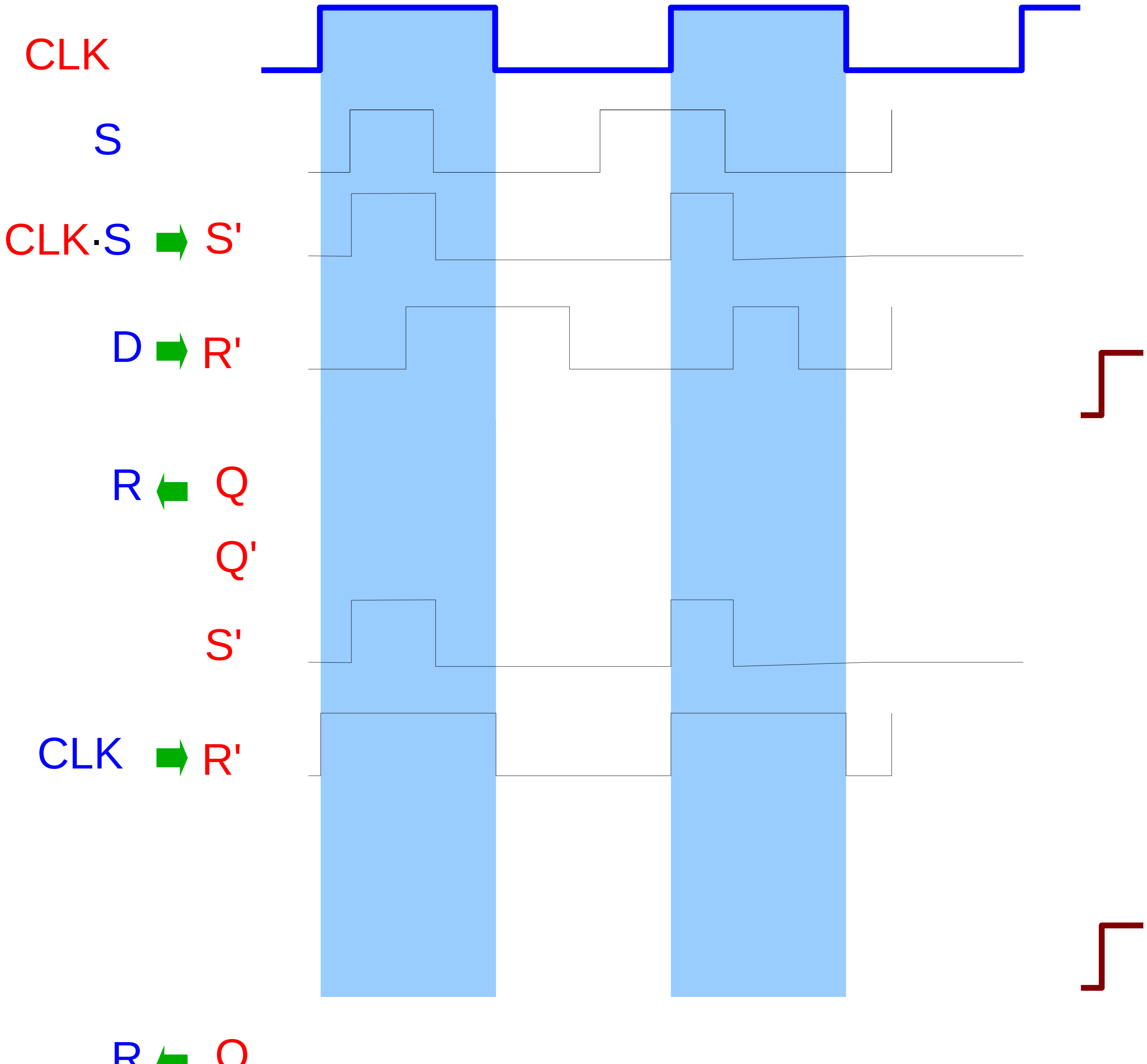


P=0 ← L2 in Set

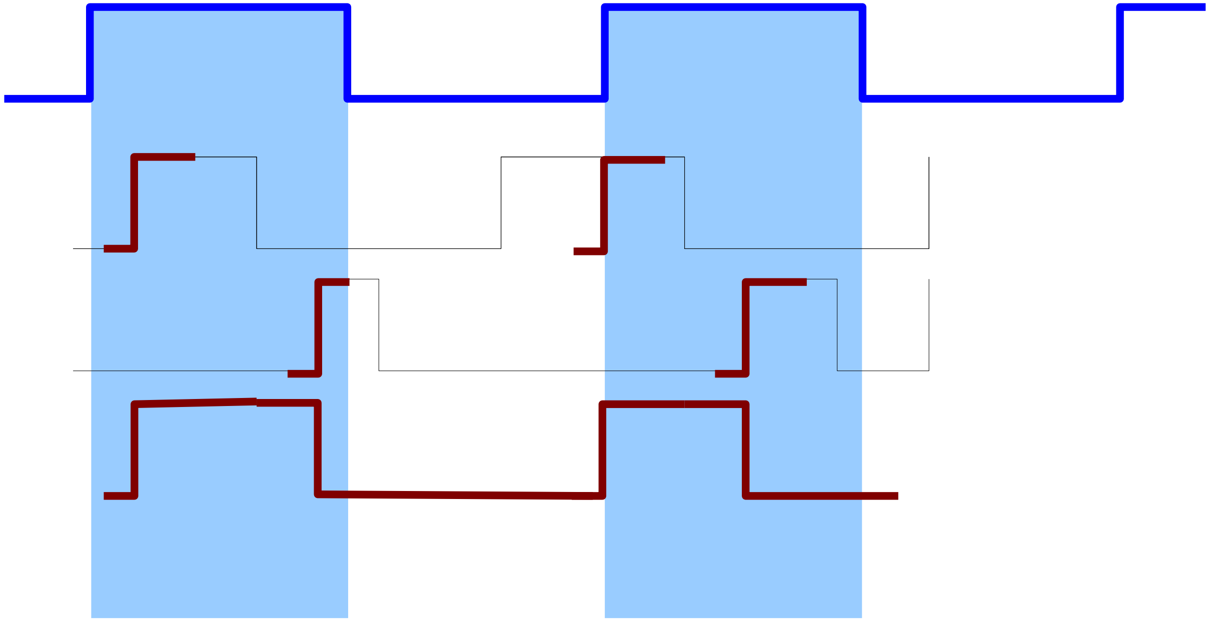
P=1 L2 in Reset, forbidden

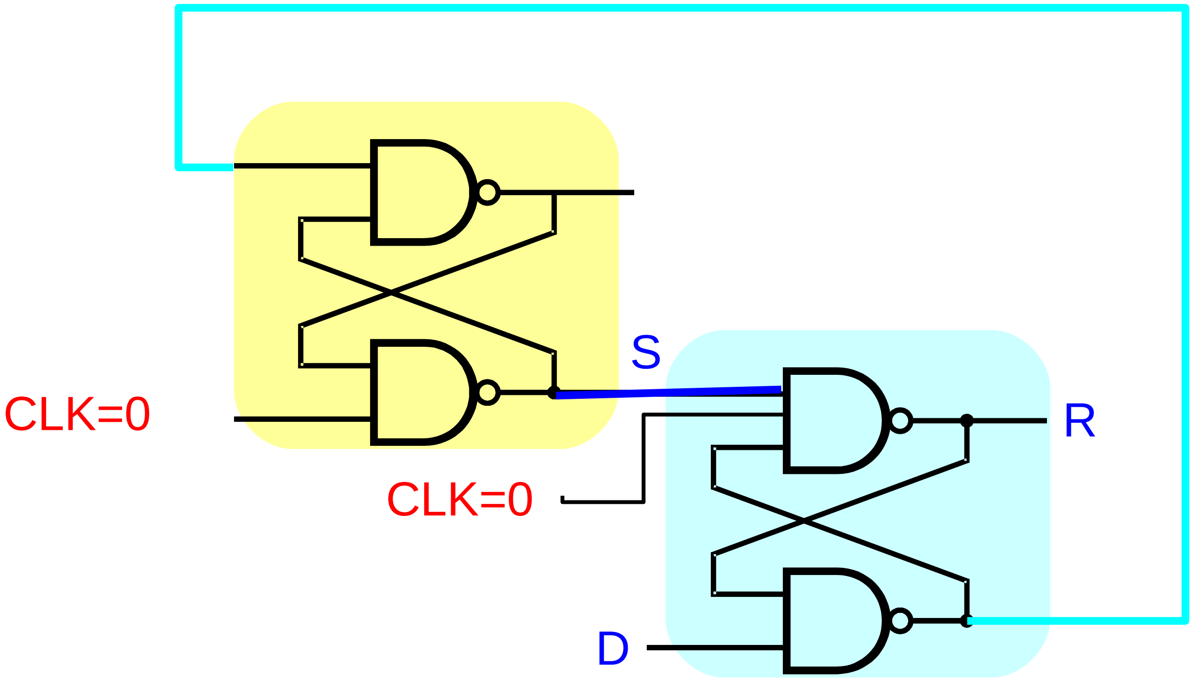
CLK=1		L1 in Set if P=0	L1 in Hold if P=1
L2 in Set	if S=0, D=1	S=0, R=1, P=0	X
L2 in Reset	if S=1, D=0	X	S=1, R=0, P=1
L2 in Hold	if S=1, D=1	X	S=1, R=0, P=1
L2 in Forbidden	if S=0, D=0	X	S=0, R=1, P=1

NAND RS Latch



Clocked NOR RS Latch




S
CLK=0
R
CLK=0
D