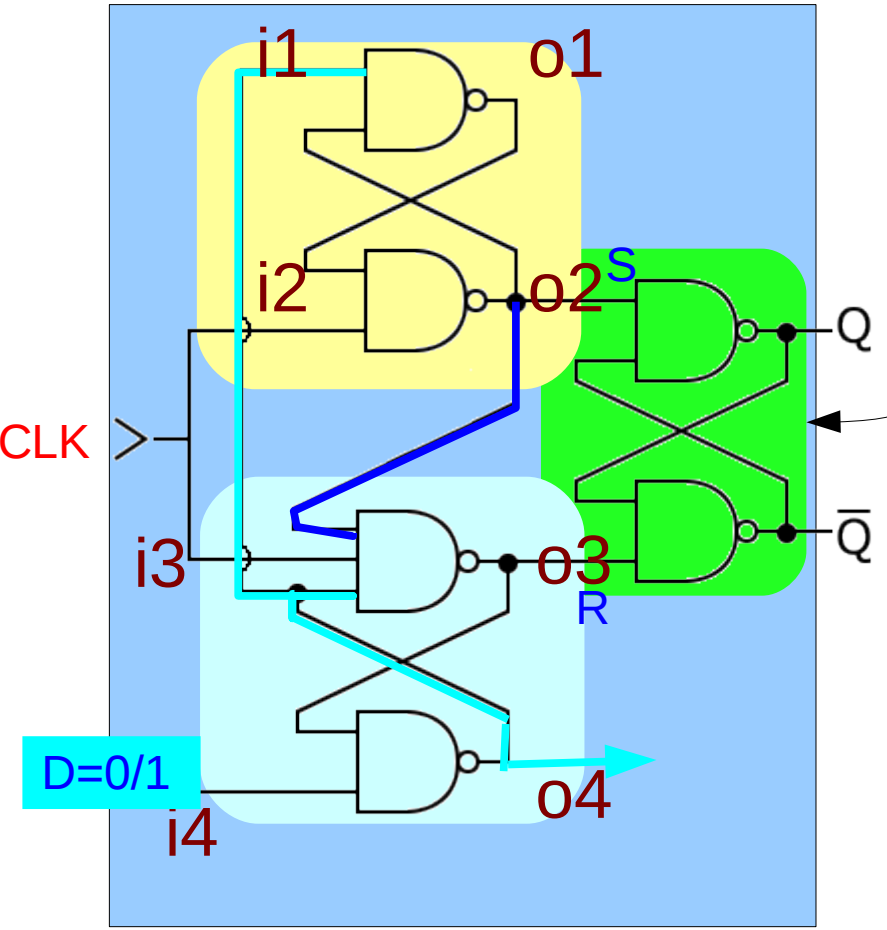
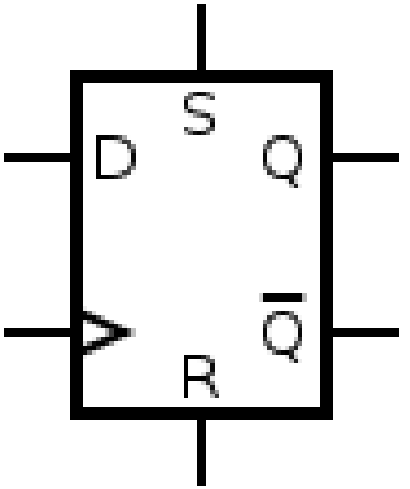
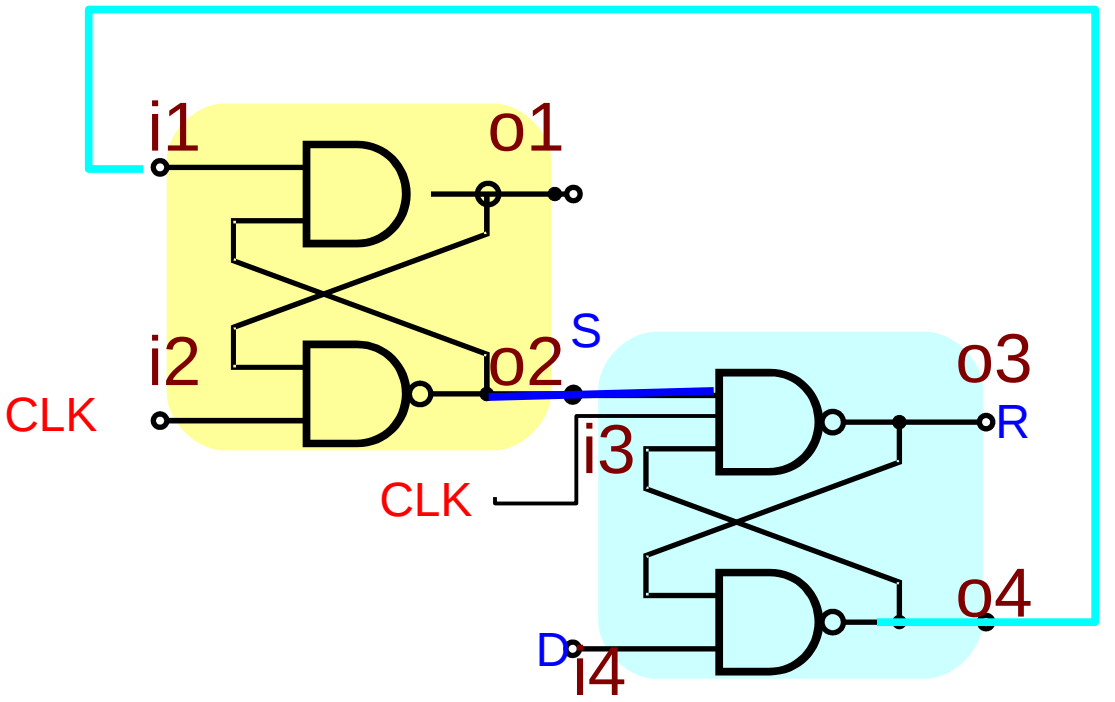
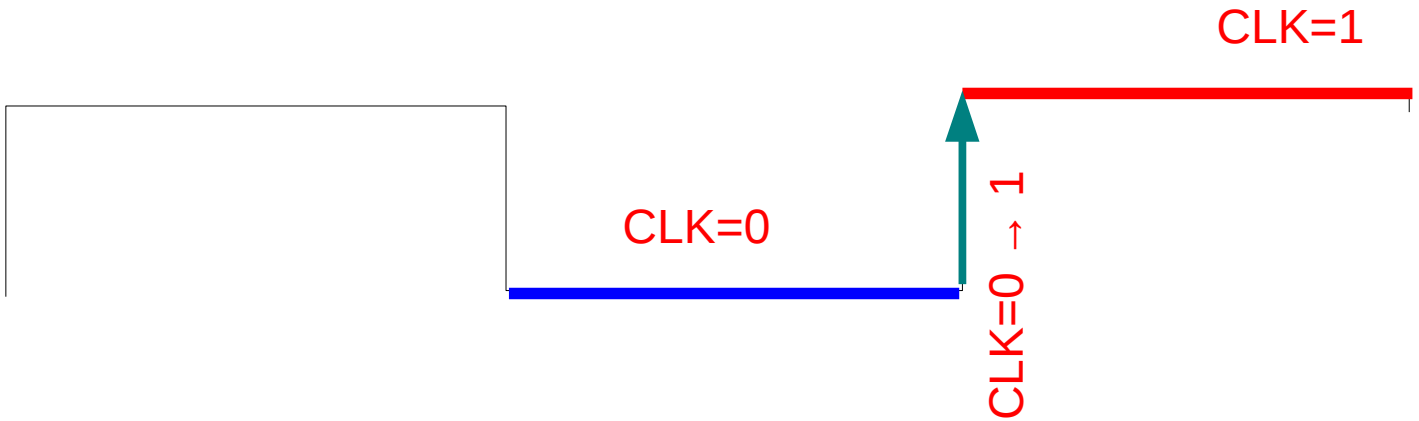


Output Stage Latch

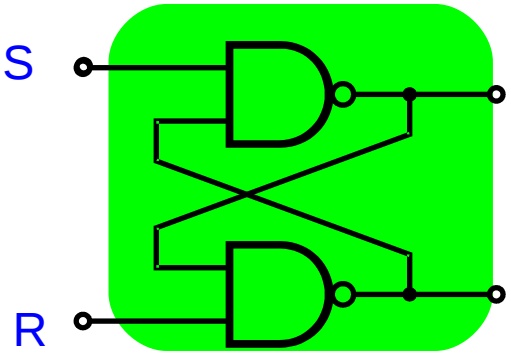


Input Stage Latch





Output Stage Latch



CLK=0

S=1
R=1

Maintain output latch

CLK=0 → 1

When D=0
S=1
R=0
When D=1
S=0
R=1

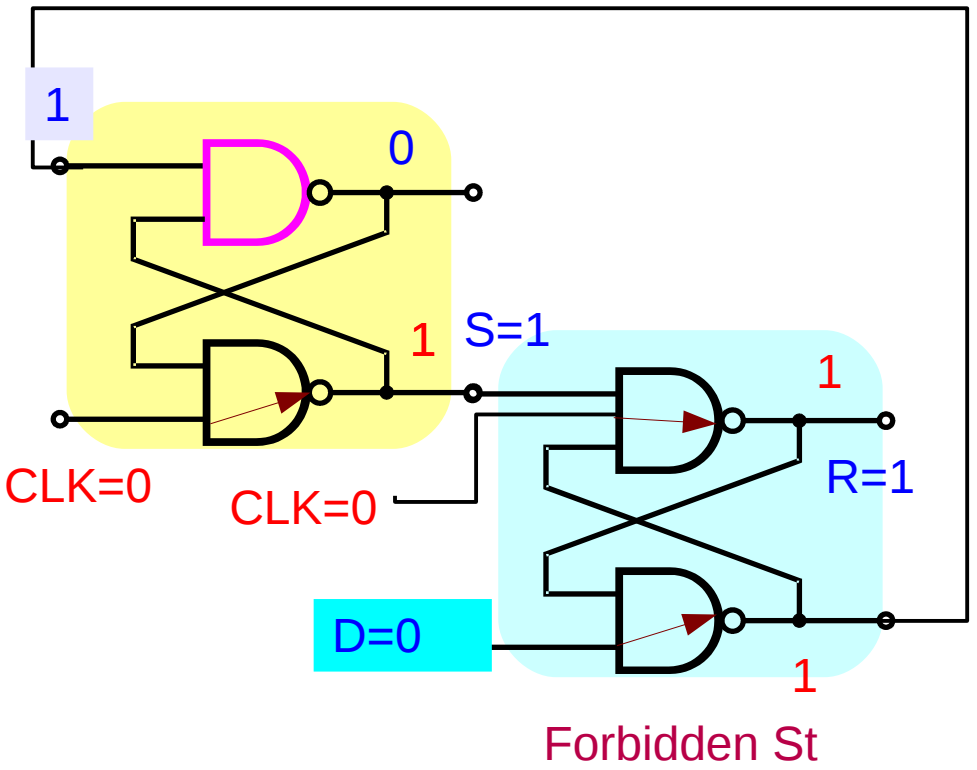
D=0/1 at the rising edge reset / set the output latch

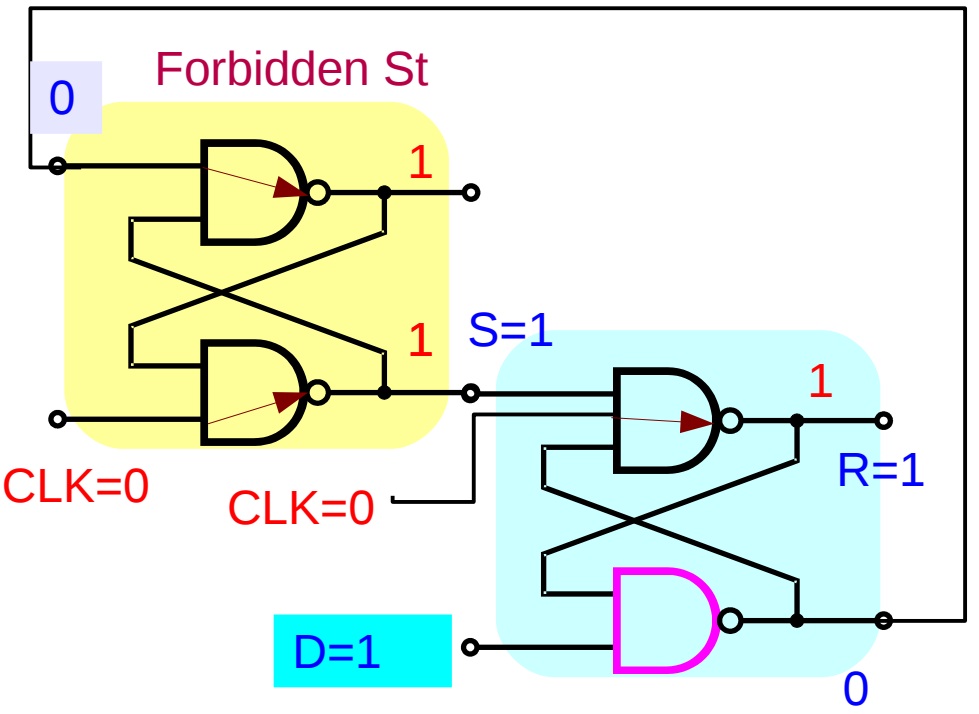
CLK= 1

When D=0 → 1
S=1
R=0
When D=1 → 0
S=0
R=1

Maintain reset / set at the rising edge regardless of input changes

Input Stage Latch – CLK =0 SR=11

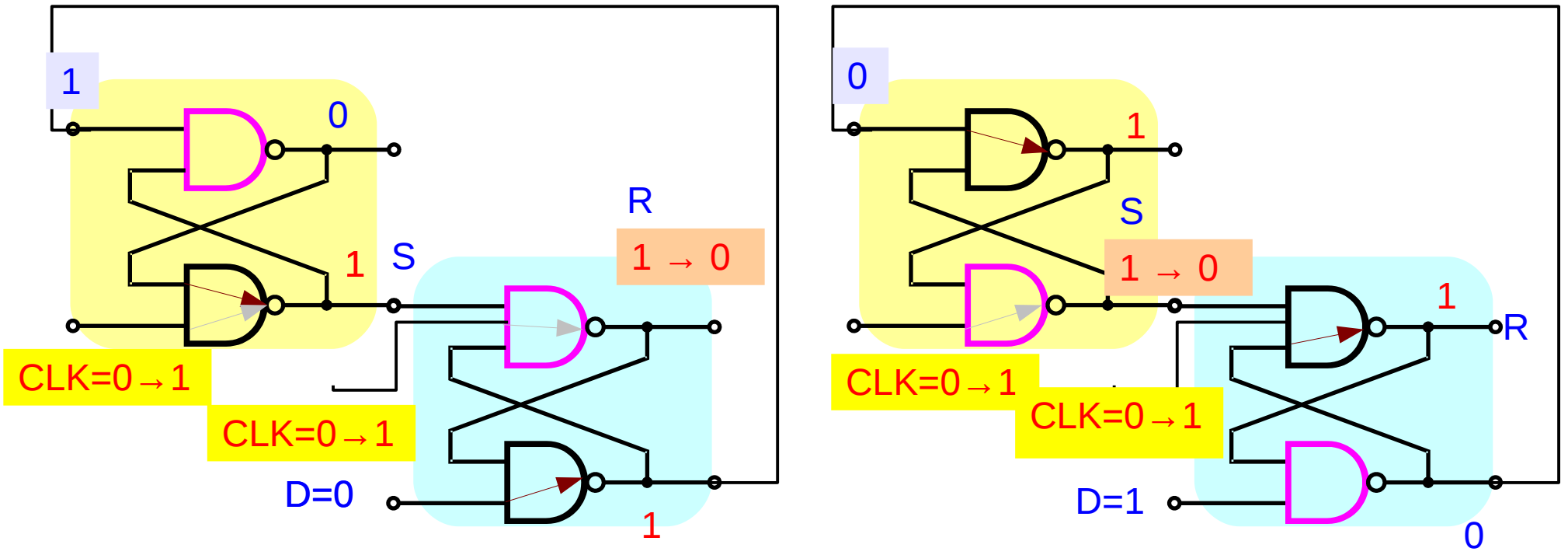




If the clock is low,
both the output signals of the input stage are high
regardless of the data input;
the output latch is unaffected
and it stores the previous state.

Input Stage Latch – Rising Edge

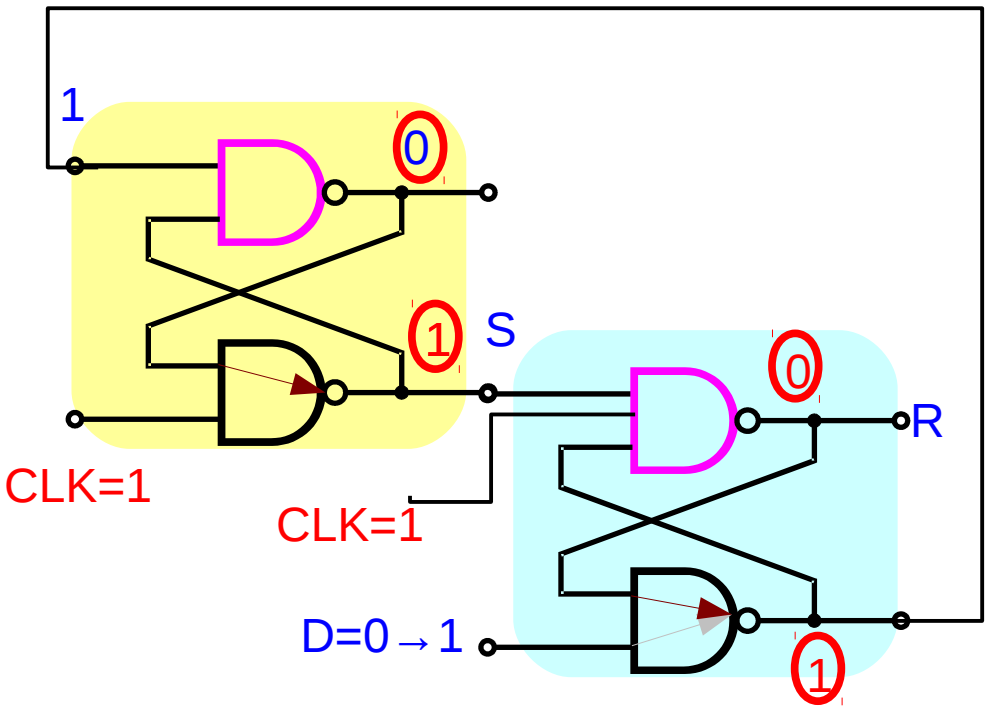
D=0 → SR=10
D=1 → SR=01

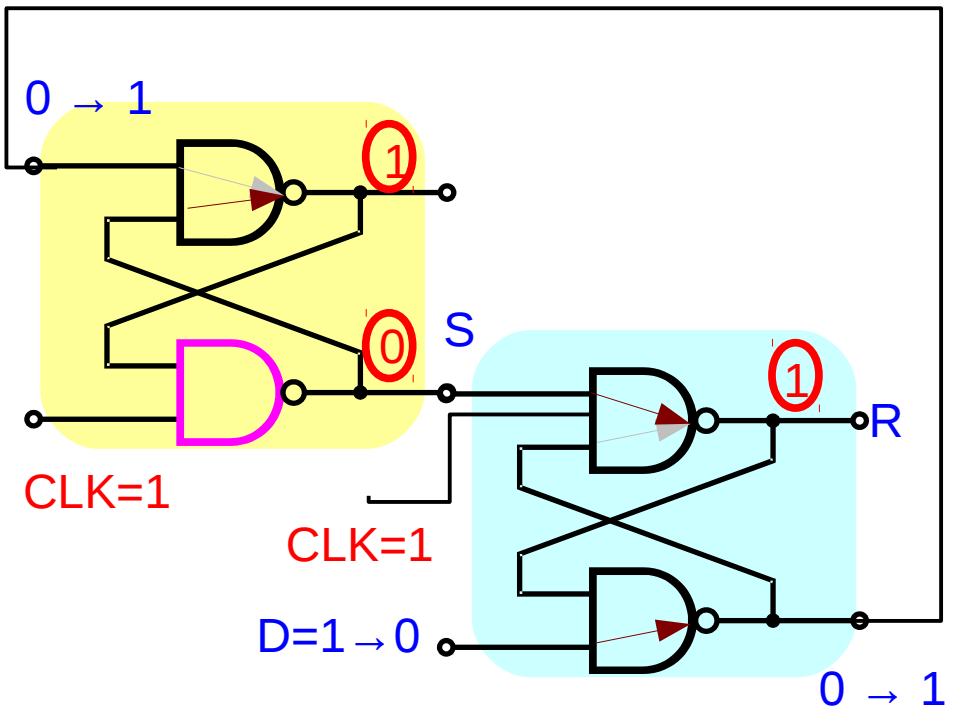


When the clock signal changes from low to high, (rising edge)
only one of the output voltages (S or R) goes low
(depending on the data signal D) and sets/resets the output latch:
(D=0 → SR = 10 → reset the output latch → Q= 0)
(D=1 → SR = 01 → set the output latch → Q = 1)
if D = 0, the lower output becomes low ; (Reset operation SR=10)
if D = 1, the upper output becomes low. (Set operation SR=01)

Input Stage Latch – CLK=1

D=(0 → 1) → SR=10
D=(1 → 0) → SR=01





If the clock signal continues staying **high**,
the outputs keep their states regardless of the data input
(D=0: SR=10, D=1: SR=01 at the rising edge)
and force the output latch to stay in the corresponding state
as the input logical zero remains active (SR=10: Reset, SR=01: Set)
while the clock is **high**.

The input stage processes the clock and data signals
to ensure correct input signals for the output stage.

The circuit is closely related to the gated D latch
as both the circuits convert the two D input states (D = 0 / 1)
to two input combinations (SR = 10 / 01) for the output SR latch
by inverting the data input signal
(both the circuits split the single D signal
in two complementary S and R signals).

The difference is that
in the gated D latch, simple NAND logical gates are used
while in the positive-edge-triggered D flip-flop,
SR NAND latches are used for this purpose.

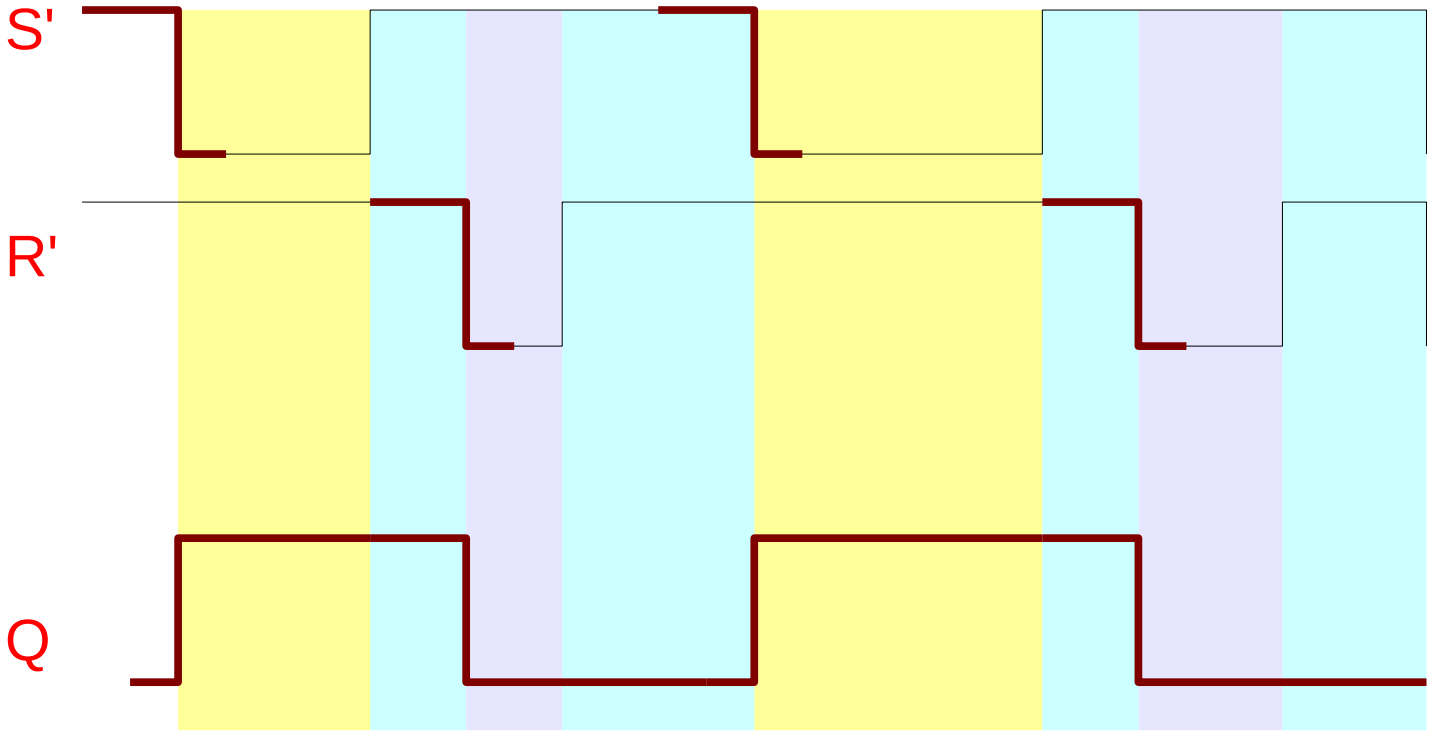
The role of these latches is to "lock" the active output
producing low voltage (a logical zero);
thus the positive-edge-triggered D flip-flop can be thought of
as a gated D latch with latched input gates.

SR = 11 is maintained when CLK = 0
→ output remains in its present state

At the rising edge (CLK=0 → 1),
if D=0 then R → 0 : RESET (Q=0)
After the rising edge (CLK=1),
R=0 is maintained even if D changes because Q = 0.
The FF is locked out and
is unresponsive to further changes in the input
At the falling edge (CLK=1 → 0),
R → 1 without changing output (HOLD state)

At the rising edge (CLK=0 → 1),
if D=1 then S → 0 : SET (Q=1)
After the rising edge (CLK=1),
S=0 is maintained even if D changes.
At the falling edge (CLK=1 → 0),
S → 1 without changing output (HOLD state)

NAND RS Latch



S' = 0
R' = 1

S' = 1
R' = 0

S' = 0
R' = 1

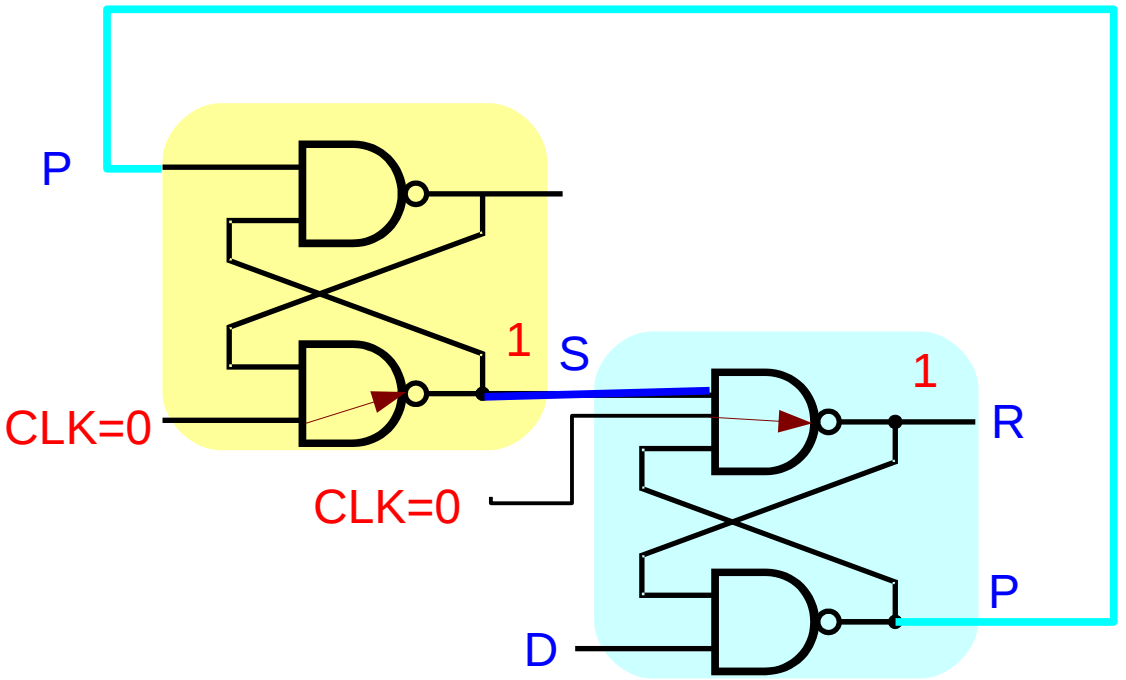
S' = 1
R' = 0

S' = 1
R' = 1

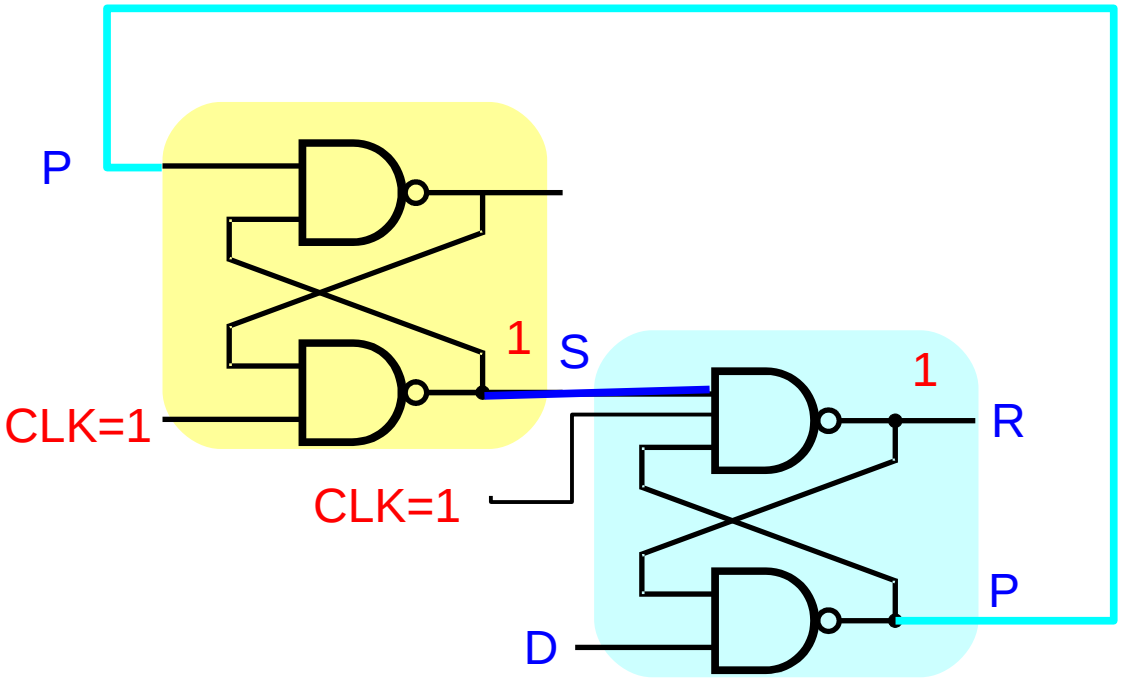
S' = 1
R' = 1

S' = 1
R' = 1

S' = 1
R' = 1



CLK=0		L1 in Reset if P=0	L1 in forbidden if P=1
L2 in Set	if D=1	S=1, R=1, P=0	X
L2 in forbidden	if D=0	X	S=1, R=1, P=1



P=0 ← L2 in Set

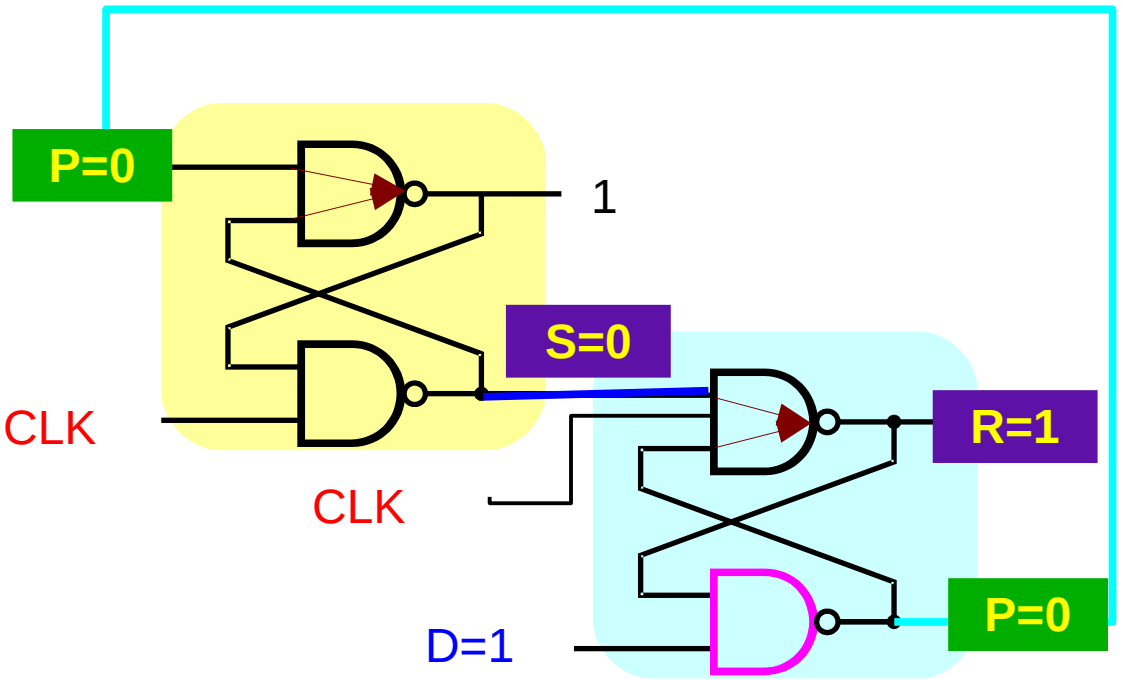
P=1 L2 in Reset, forbidden

CLK=1		L1 in Set if P=0	L1 in Hold if P=1
L2 in Set	if S=0, D=1	S=0, R=1, P=0	X
L2 in Reset	if S=1, D=0	X	S=1, R=0, P=1
L2 in Hold	if S=1, D=1	X	S=1, R=0, P=1
L2 in Forbidden	if S=0, D=0	X	S=0, R=1, P=1

SET op for the ouput latch

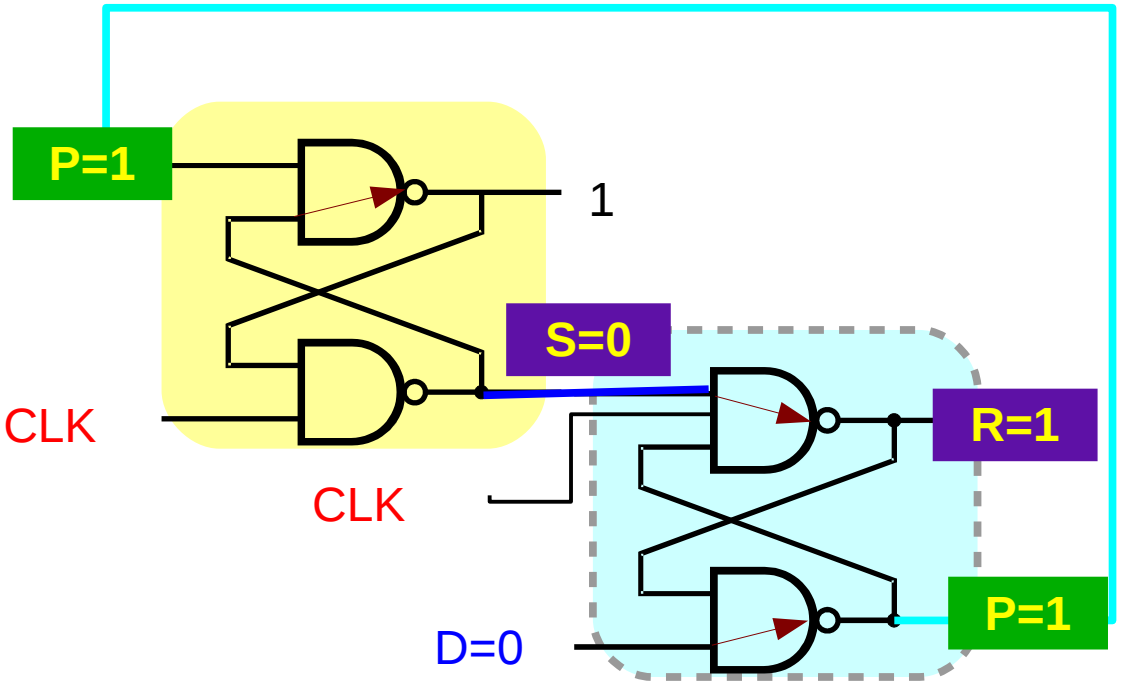
When CLK=1, regardless of D

S=0 **R=1**



CLK=0 → ~~S=1~~ ⇨ CLK=1

D=1 → P=0



CLK=0 → ~~S=1~~ ⇨ CLK=1

D=0 → P=1

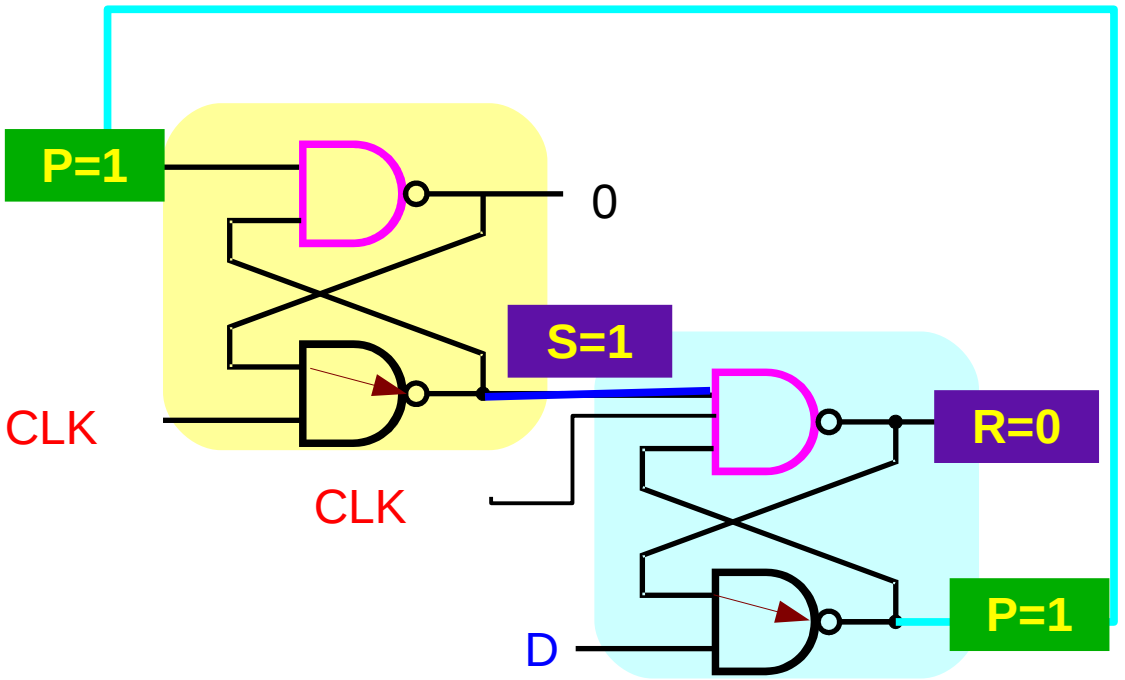
RESET op for the ouput latch

When CLK=1, regardless of D

S=1 **R=0**

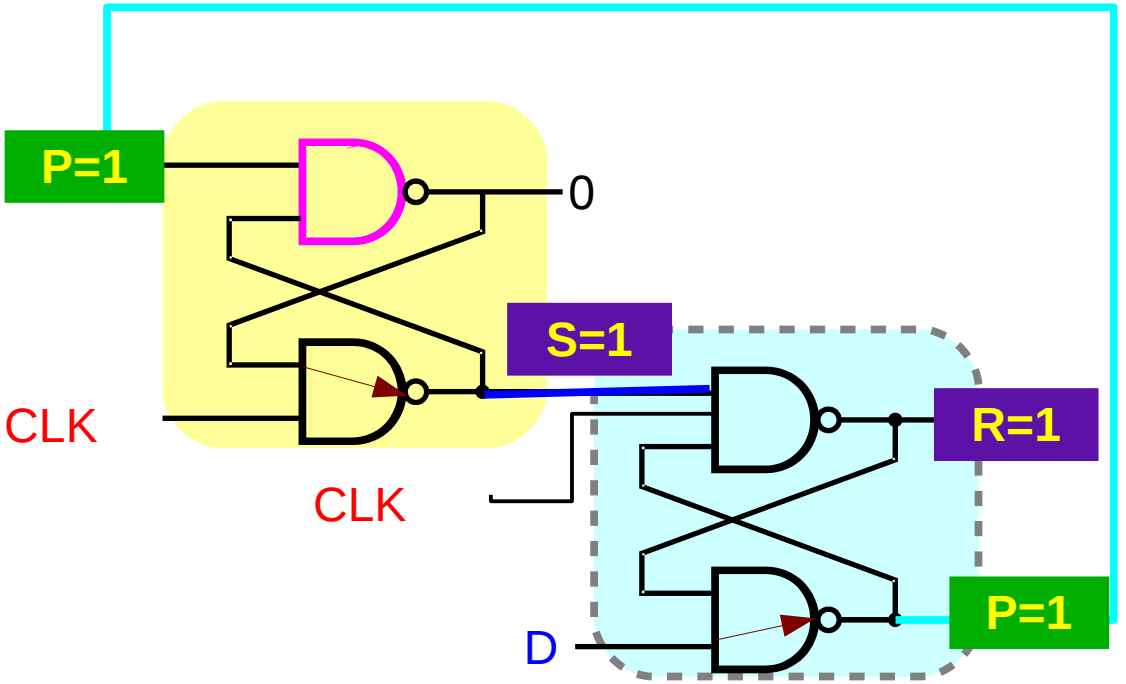
CLK=0 → ~~R=1~~ ⇨ CLK=1

D=0 / 1



HOLD op for the ouput latch

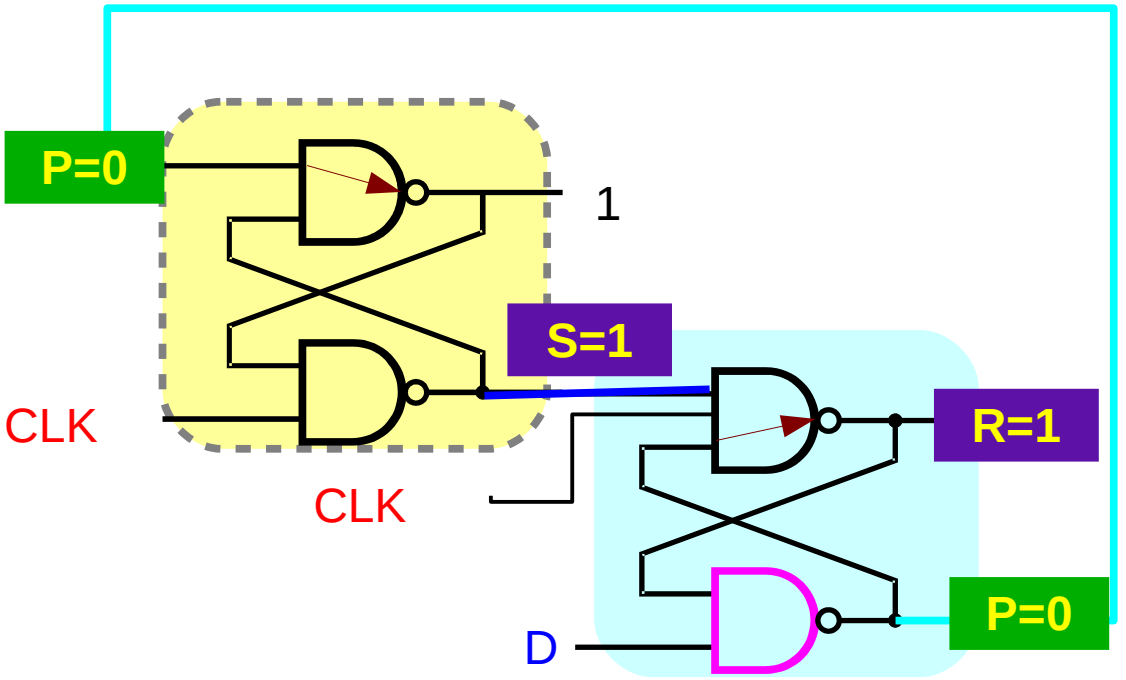
When CLK=0, regardless of D



S=1 R=1

CLK=1 → R=0 ⇨ CLK=0

D=0 → P=1

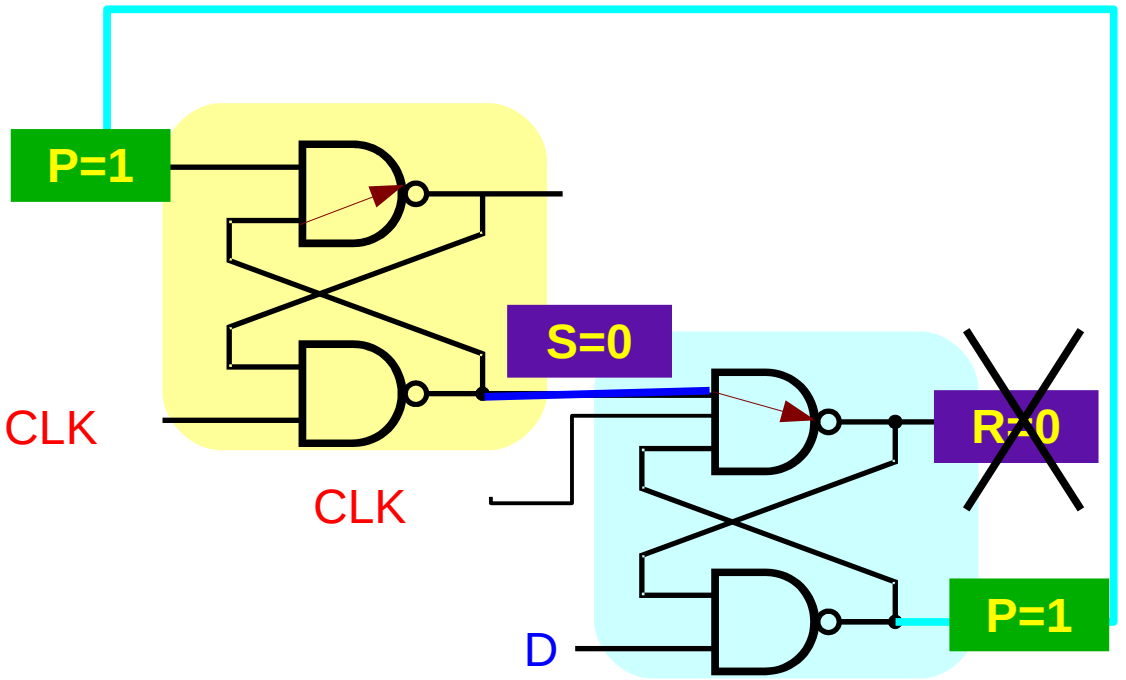


CLK=1 → S=0 ⇨ CLK=0

D=1 → P=1

Forbidden for the ouput latch

Impossible to enter

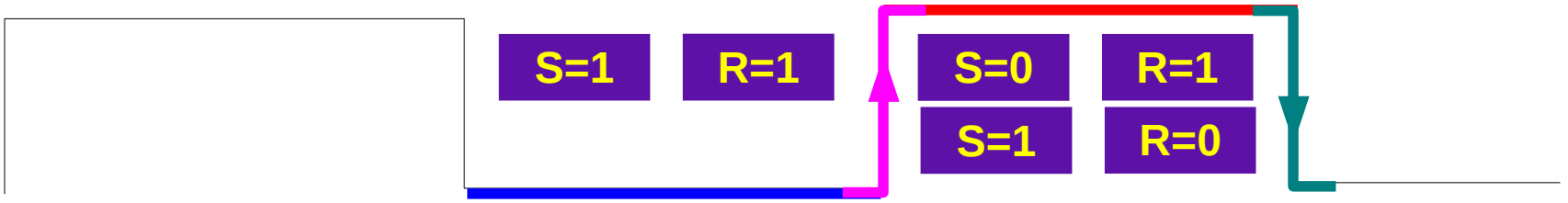


CLK=0

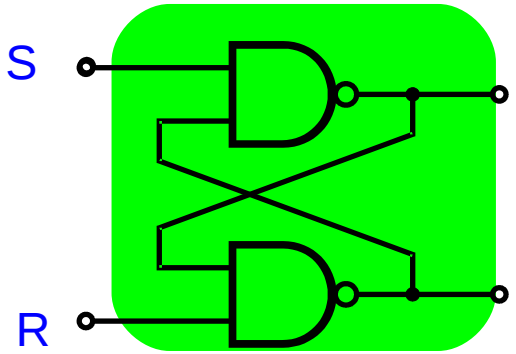
CLK=1

HOLD op for the ouput latch

SET, RESET op for the ouput latch



Output Stage Latch



CLK=0 → 1

When D=0
HOLD → RESET

When D=1
HOLD → SET

CLK=1 → 0

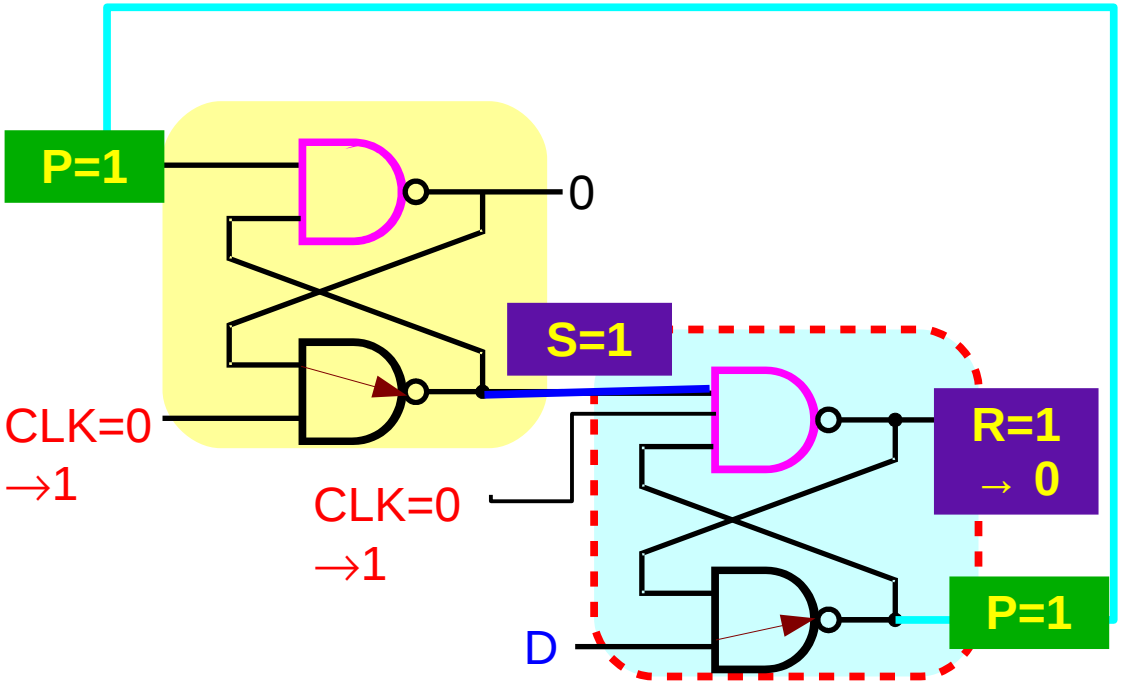
RESET → HOLD

SET → HOLD

Rising edge CLK=0→1

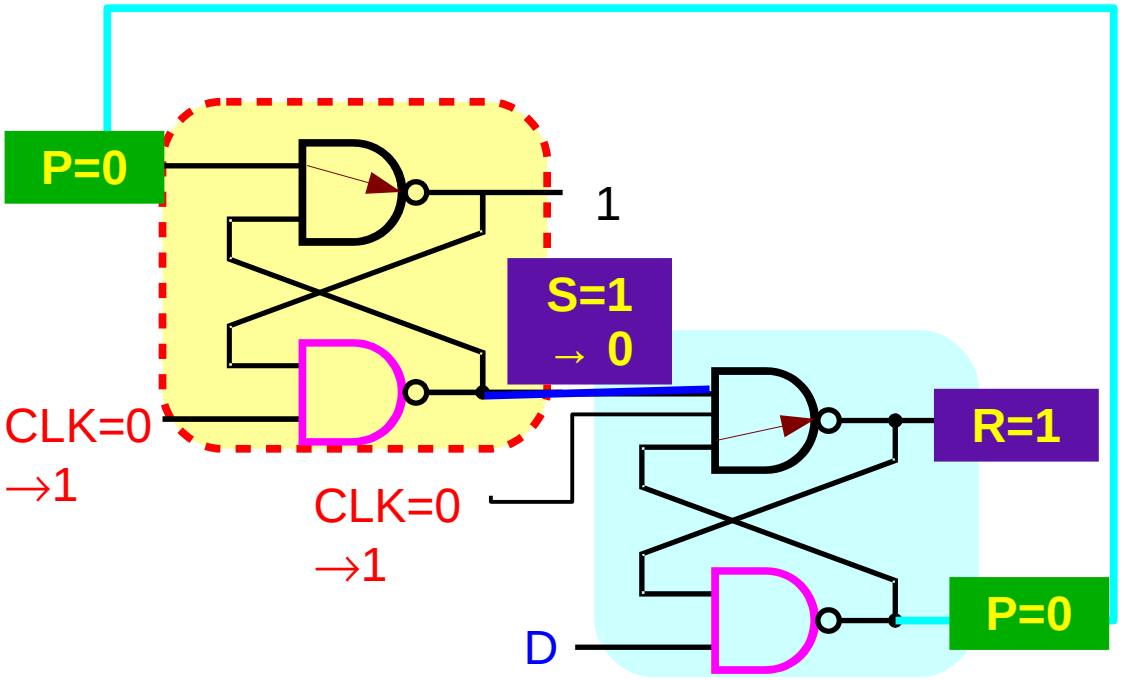
HOLD → RESET / SET

If D=0	SR=11	⇨	SR=10
If D=1	SR=11	⇨	SR=01



CLK=1 ⟶ R=0

D=0 ⟶ P=1



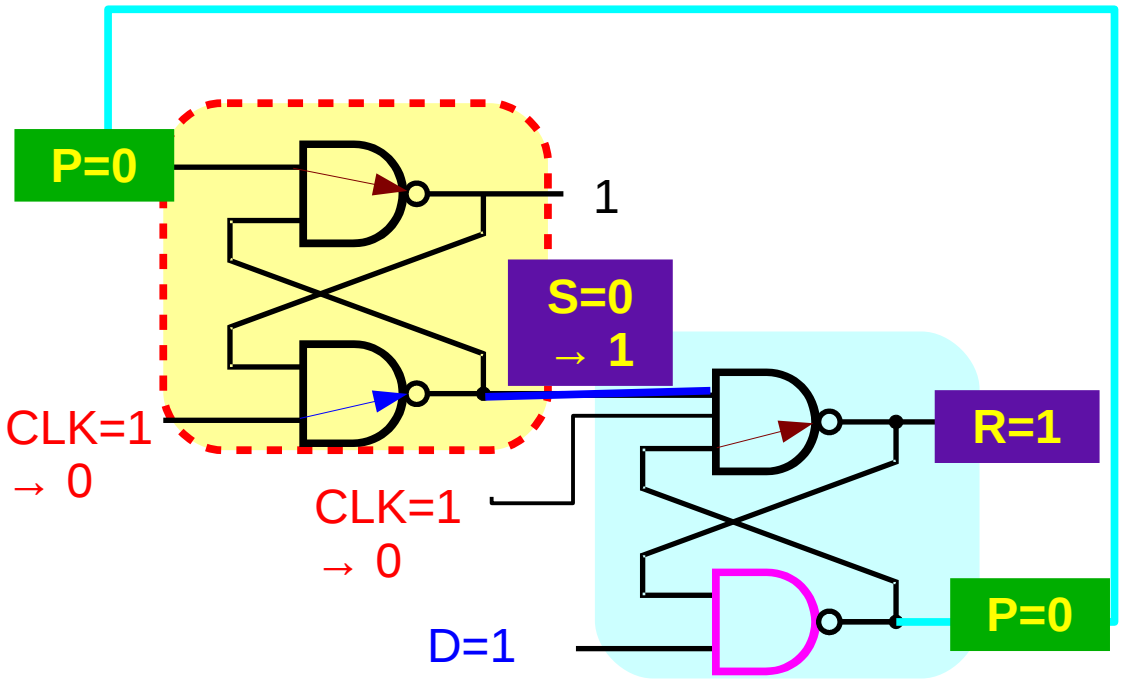
CLK=1 ⟶ S=0

D=1 ⟶ P=1

Falling edge CLK=1→0

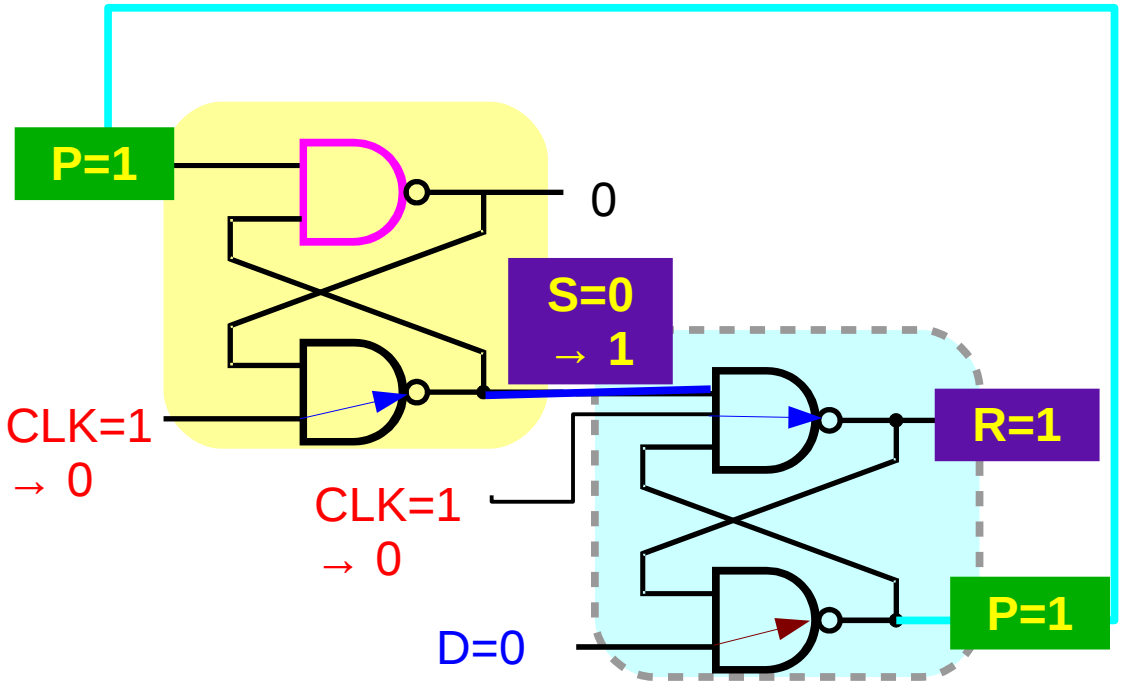
SET → HOLD

SR=01 ⇨ **SR=11**



CLK=0 → S=1

D=1 → P=0



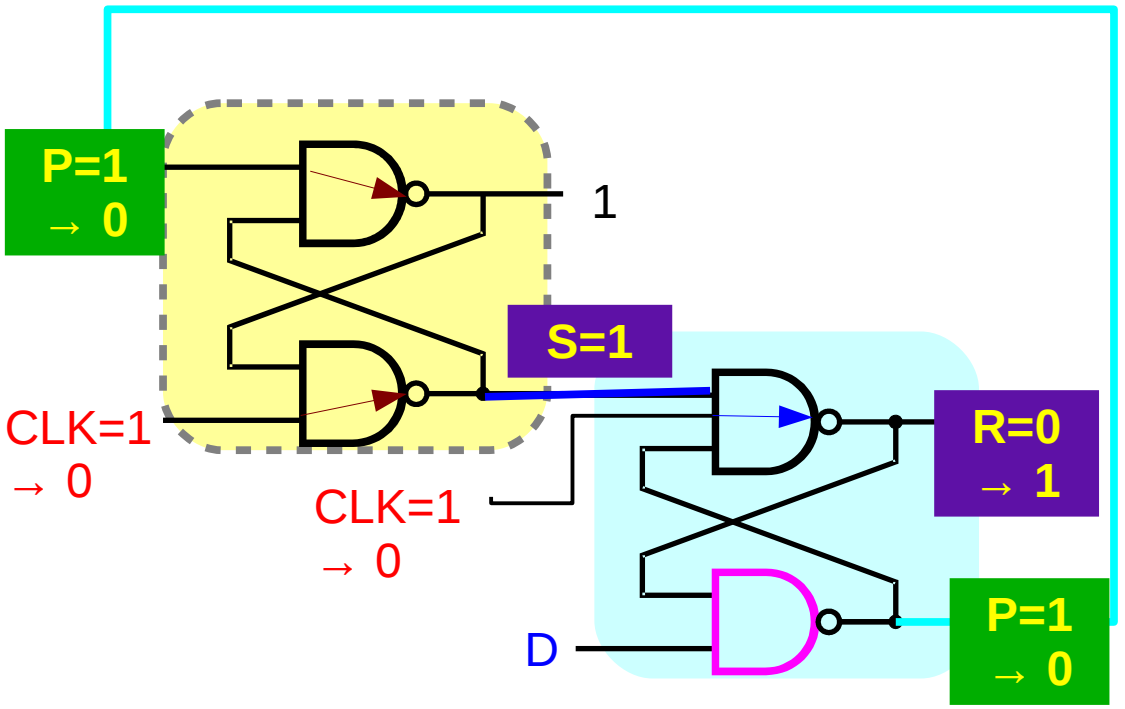
CLK=0 → S=1

D=0 → P=1

Falling edge CLK=1→0

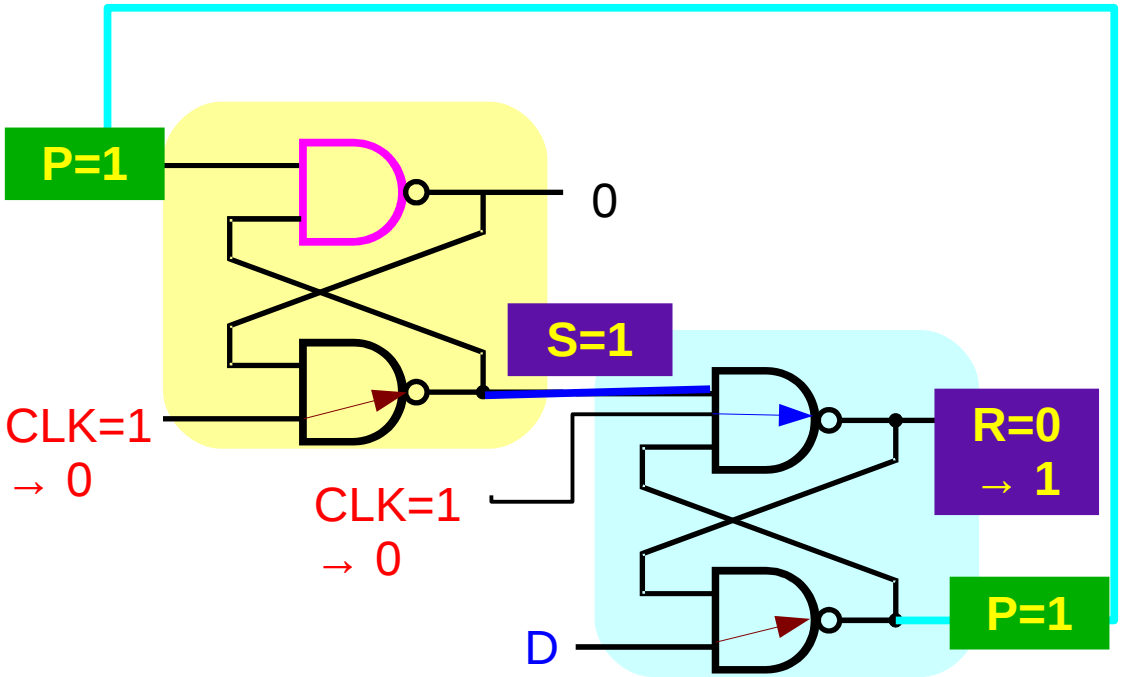
RESET → HOLD

SR=10 ⇨ **SR=11**



CLK=0 ⟶ R=1

D= 1



CLK=0 ⟶ R=1

D= 0